AM64x/AM243x Processors Silicon Revision 2.0 Texas Instruments Families of Products

Technical Reference Manual

TEXAS INSTRUMENTS

Literature Number: SPRUIM2I
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Table of Contents

Preface

Read This First

About This Manual

This Technical Reference Manual (TRM) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Related Documentation From Texas Instruments

For a complete listing of related documentation and development-support tools for the device, visit the Texas Instruments website at www.ti.com.

Additional Documentation

Below are some direct links to additional documentation:

- AM64x Software Build Sheet
- AM64x Datasheet
- AM64x/AM243x Schematic Checklist

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Chapter 1

Introduction

This chapter introduces the features, subsystems, and architecture of the AM64x/AM243xSitara Processor Platform high-performance System-on-Chip (SoC).

Note

This document describes the Superset architecture, processors and peripherals of the AM64x and AM243x Family of SoCs, which are part of the Sitara Processors Multicore SoC architecture platform. Not all features are available on each family of devices. The superset AM6442x and AM2434x devices are available for preproduction software development. Software should constrain the features used to match the intended production device. For more information on the specific features, processors and peripherals available on a particular device, refer to the Device Comparison table in the corresponding device-specific Data sheet.

The AM64x and AM2434x Sitara Processor Platforms are hereinafter commonly referred to as *AM64x*, *AM243x, platform*, *device*, or *SoC*.

1.1 Device Overview

This section gives overview

Below are some direct links to additional documentation:

- AM243x Datasheet
- AM64x Datasheet
- AM243x Software Build Sheet
- AM64x Software Build Sheet
- MCU-PLUS-SDK-AM243x
- MCU-PLUS-SDK-AM64x
- AM64x/AM243x Schematic Checklist

1.2 Functional Block Diagram

Figure 1-1 is functional block diagram for the device.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), search for the *AM64x Software Build Sheet* located in the Downloads tab option provided at Processor-SDK-AM64x.

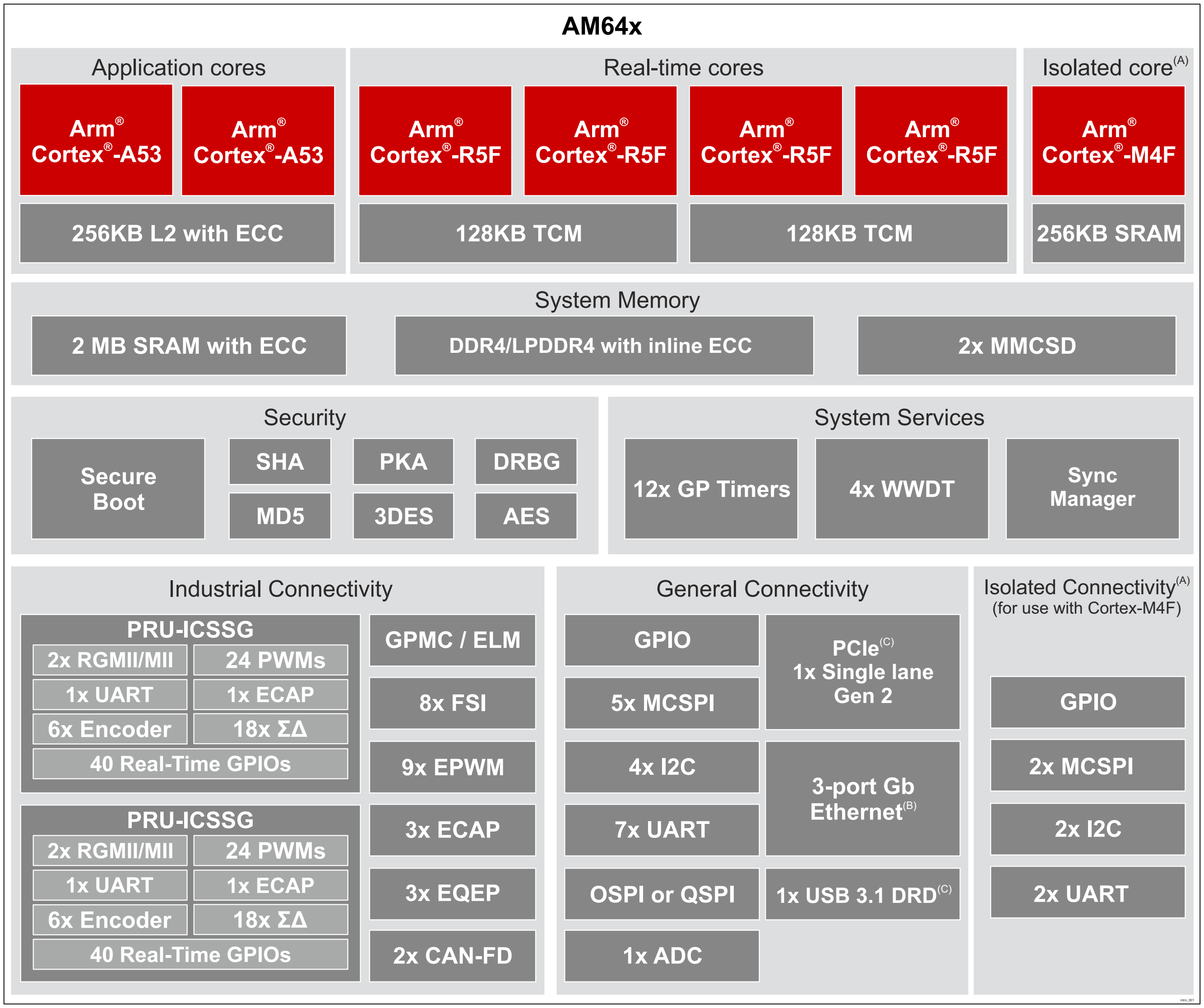

Note

Isolation of peripherals and M4F core is an optional feature.

Note

One port is internally connected only; not connected to any pins.

Note

USB SuperSpeed and PCIe share a common SerDes PHY. Therefore, USB will be limited to non-SuperSpeed modes when using the SerDes PHY for PCIe.

Figure 1-1. Functional Block Diagram

1.2.1 Module Allocation and Instances within Device Domains

Module Full Name	Module Abbreviation	Device Domain	
		MCU	MAIN
Dual-Core Arm Cortex A53 Subsystem	A53SS	-	1
Dual-Core Arm Cortex-R5F Subsystem	R5FSS	-	2
Arm Cortex-M4F Subsystem	M4FSS	1	-
Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit	PRU_ICSSG	-	2
Device Management and Security Controller	DMSC-L	-	1
Interprocessor Communication - Mailbox	Mailbox	-	1
Interprocessor Communication - Spinlock	Spinlock	-	1
Dual Data Rate Random Access Memory (16-Bit) Subsystem	DDRSS	-	1
Region-based Address Translation	RAT	-	1
Data Movement Subsystem	DMSS	-	1
Peripheral DMA	PDMA	-	2
Common Platform Time Sync Module	CPTS	-	1
Timer Manager Module	TIMERMANAGER	-	1
Analog to Digital Converter	ADC	-	1
General Purpose Input/Output	GPIO	1	2
Inter-Integrated Circuit	I2C	2	4
Multi-channel Serial Peripheral Interface	MCSPI	2	5
Universal Asynchronous Receiver/Transmitter	UART	2	7
2 Port Gigabit Ethernet Switch	CPSW3G	-	1
Peripheral Component Interconnect Express	PCIE	-	1
Serializer/Deserializer (1-Lane)	SERDES	-	1
Universal Serial Bus Subsystem	USB	-	1
Enhanced Pulse Width Modulation Module	EPWM	-	9
Enhanced Quadrature Encoder Pulse Module	EQEP	-	3
Enhanced Capture Module	ECAP	-	3
Fast Serial Interface Transmitter	FSI_TX	-	2
Fast Serial Interface Reciever	FSI_RX	-	6
Controller Area Network Interface	MCAN	-	2
Flast Memory Subsystem	FSS	-	1
Octal Serial Peripheral Interface	OSPI	-	1
General Purpose Memory Controller	GPMC	-	1
Error Location Module	ELM	-	1
Multi-Media Card/Secure Digital Interface	MMCSD	-	2
Global Time Counter	GTC	-	1
Real Time Interrupt/Windowed WatchDog Timer	RTI/WWDT	1	6
Dual-Mode Timer	TIMER	4	12
Dual Clock Comparator	DCC	1	6
Error Signaling Module	ESM	1	1

Module Full Name	Module Abbreviation	Device Domain	
		MCU	MAIN
Memory Cyclic Redundancy Check Controller	MCRC	1	-

1.3 Device MAIN Domain

This section describes the modules integrated in the device MAIN domain.

Device MAIN Domain Functional Block Diagram

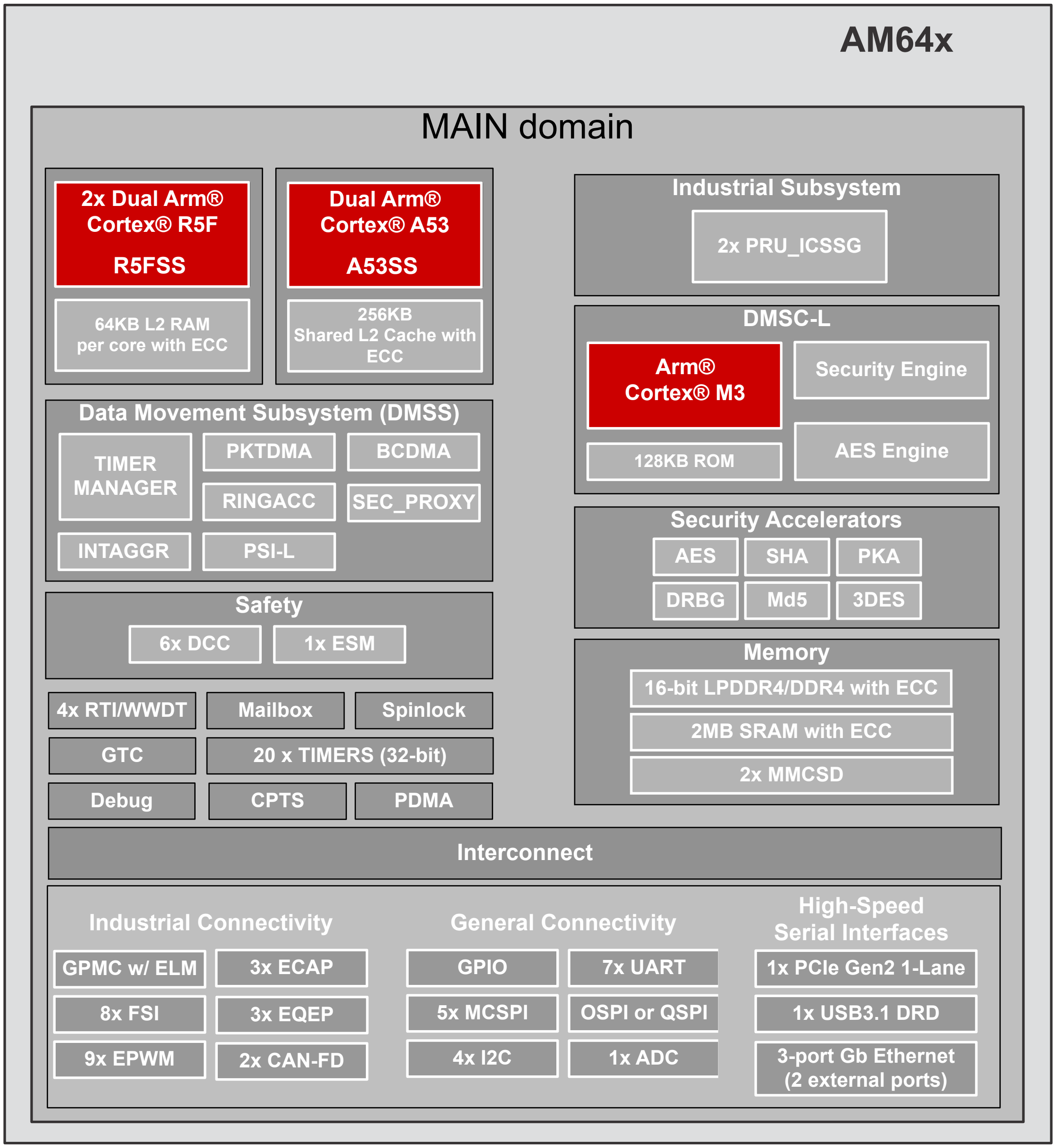

Figure 1-2. Main Domain Function Block Diagram

1.3.1 Arm® Cortex®-A53 Subsystem (A53SS)

The integrated 64-bit Arm® Cortex®-A53 subsystem (A53SS) supports the following main features:

- Two instances of dual-core Cortex-A53 MPCore processors (A53SS_CORE0 and A53SS_CORE1), each with L1 memory system and a single shared L2 cache
- Full Arm®v8-A architecture compliancy
- Advanced Single Instruction Multiple Data (SIMD) and floating point extension (Arm® Neon™)
- Floating-Point Unit (FPU) VFPv4
- Armv8 Cryptography Extensions
- Arm General Interrupt Controller (GICv3) architecture
- In-order pipeline with symmetric dual-issue of most instructions
- 32KB program and 32KB data Level 1 (L1) Cache
- 256KB shared Level 2 (L2) Cache
- Support for up to four timers within each Cortex-A53 core
- Arm® CoreSight™ Debug and Trace Architecture
- ECC protection for L1 data cache and L2 Cache
- Parity protection for L1 Instruction Cache
- 128-bit wide, synchronous or asynchronous VBUSM initiator interface
- Dedicated RTI windowed watchdog timer per core
- Support for Big-Endian (BE) and Little-Endian (LE) at core level
- Interface with Arm GIC-500 Interrupt Controller (SoC level, not part of A53SS)
- Advanced power management for low power optimization

Note

NOT SUPPORTED in AM243x platform. See device-specific Datasheet for additional details.

1.3.2 Arm Cortex-R5F Processor Sub System (R5FSS)

The ARM Dual-Core Cortex-R5F processor subsystem (R5FSS) supports the following main features:

- Armv7-R architecture
- Supported modes of operation (boot-time configurable):
  - Dual Core mode: two independent free-operating cores (Asymmetric Multi-Processing, no coherence)
  - Single Core mode: one free-operating core and one non-operating core
- R5FSS Memory System
  - 32KB Instruction Cache
    - 4x8KB ways
    - SECDED ECC protected per 64 bits
  - 32KB Data Cache
    - 4x8KB ways
    - SECDED ECC protected per 32 bits
  - 64KB tightly-coupled memory (TCM) per CPU
    - SECDED ECC protected per 32 bits
    - TCM hard error cache Implemented in CPU
    - Readable/writable from system
    - TCMs initialized (to 0's) at reset
    - 32KB TCMA (ATCM)
    - 16KB TCMB0 (B0TCM)
    - 16KB TCMB1 (B1TCM)
    - 128KB TCMA (ATCM) and 128KB TCMB (BTCM) for each core in Split-mode
- Full-precision Floating Point (VFPv3)
- 8 breakpoints, 8 watch points
- CoreSight Debug Access Port (DAP)
- CoreSight ETM-R5 interface (CTI, ETM, ATB)
- Performance Monitoring Unit (PMU)
- 32-bit to 36-bit Region-based Address Translation (RAT) on memory access initiators

- Integrated Vectored Interrupt Manager (VIM) per core with 256 Interrupt Inputs each
  - Programmable interrupt priority (4-bit)
  - Programmable interrupt enable mask
  - Software-generated interrupts
  - Synchronous clock domain crossing on all core interfaces

Note

The operating cores can be configured to use the full TCM memory space available to both cores.

In Dual Core mode, CORE0 and CORE1 each have 64KB of TCM:
- 32KB TCMA
- 16KB TCMB0 + 16KB TCMB1

In Single Core mode, CORE0 has 128KB of TCM :
- 64KB TCMA
- 64KB TCMB (32KB TCMB0 + 32KB TCMB1)

Note

These details describe a superset of the R5FSS memory configuration. For additional details on device memory availability, please refer to the device-specific data sheet.

1.3.3 Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)

Integrated in MAIN domain: Two instances of the Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG) allows implementation of various high-performance industrial control algorithms and industrial interface standards such as PROFINET™ and EtherCAT®.

MAIN domain encompasses two identical PRU_ICSSG subsystems, each supporting the following main features, among others:
- Two Programmable Real-time Unit Subsystems (PRUSS), each with 3 PRU's:
  - PRU:
    - Asynchronous capture (Serial Capture Unit (SCU)] with EnDat 2.2 protocol and Sigma-Delta demodulation support
    - 20 Enhanced General Purpose Inputs (EGPI) and 20 Enhanced General Purpose Outputs (EGPO)
    - 12 KB program memory with ECC
    - 2 KB Broadside RAM
    - MAC (multiplier with optional accumulation)
    - CRC16/CRC32 HW accelerator
    - Byte Swap for Little/Big Endian Conversion
    - SUM32 HW accelerator for UDP checksum
    - Task Manager (Preemption Support)
    - 128-Bit Wide PSI-L TX port
    - Broadside (32 Byte) connection to MII_G_RT, Filter Database (FDB), IPC SPAD, ScratchPad, Memory (SPAD), Spinlock, XFR2VBUS, AUX_PRU (RTU) and TX_PRU
  - AUX_PRU (RTU):
    - 8 KB program memory with ECC
    - 2 KB Broadside RAM
    - MAC (multiplier with optional accumulation)
    - CRC16/CRC32 HW accelerator
    - Byte Swap for Little/Big Endian Conversion
    - SUM32 HW accelerator for UDP checksum

    - Task Manager (Preemption Support)
    - 128-Bit Wide PSI-L 4RX / 1-TX
    - XFR2TR, for accelerating the internal memory copy of worklist from TRs (Transfer Requests)
    - Broadside (32 Byte) connection to MII_G_RT, Filter Database (FDB), IPC SPAD, ScratchPad, Memory (SPAD), Spinlock, PRU and TX_PRU
  - TX_PRU:
    - 6 KB program memory with ECC
    - 2 KB Broadside RAM
    - MAC (multiplier with optional accumulation)
    - CRC16/CRC32 HW accelerator
    - Byte Swap for Little/Big Endian Conversion
    - SUM32 HW accelerator for UDP checksum
    - Task Manager (Preemption Support)
    - Broadside (32 Byte) connection to MII_G_RT (L2), ScratchPad Memory (SPAD), Spinlock, PRU and AUX_PRU (RTU)
- 64KB shared general purpose RAM with ECC
- Two 8KB data memories with ECC (one per slice)
- Two 256-bit VBUSM Controller Ports
- Two Real-Time Ethernet MII_G_RT ports configurable to connect to each PRU to support multiple industrial communication protocols
- Two 10/100/1000 Ethernet Ports
- Two Industrial Ethernet Peripherals (IEP) to manage/generate Industrial Ethernet functions
- One Management Data Input/Output (MDIO) port to control external Ethernet PHY
- One UART 16550-compatible, with a dedicated 192 MHz to support 12 Mbps PROFIBUS
- Two industrial Ethernet 64-bit timers, each with 10 capture and 16 compare events, along with slow and fast compensation.
- One Enhanced Capture (ECAP) module
- One Pulse Width Modulation (PWM) module with flexible real time safety options and output behavior
  - Supports up to 4 sets of 3-phased motor control, with 12 primary and 12 complimentary programmable PWM outputs.
  - Up to 9 safety events with optional external trip I/O per PWM set with hardware glitch filter.
- One interrupt controller (INTC) with160 input events supported – 96 external, 64 internal
- ECC support for all internal memories
- Flexible power management support

Among the interfaces supported by the PRU_ICSSG are real-time industrial protocols used in controller and target mode, such as:

- EtherCAT®
- PROFINET™
- EtherNet/IP™
- PROFIBUS®
- Ethernet Powerlink™
- SERCOS®

1.3.4 DDR 16-bit Subsystem (DDR16)

Integrated in MAIN domain: One instance of DDR 16-bit Subsystem (DDR16) (also referred to as DDRSS) is used as an interface to external SDRAM devices which can be utilized for storing program or data. The DDRSS provides the following main features:

- Support of LPDDR4 memory type (up to 1600Mbps)
- Support of DDR4 memory type (up to 1600Mbps)
- 16-bit memory bus interface with in-line ECC ½ width
- Up to 8 GB memory address range
- Support of dual rank configuration

- Support of automatic idle power saving mode when no or low activity is detected
- Class of Service (CoS) - three latency classes supported
- Dynamic change of refresh reach via SW for extended temperatures
- Prioritized refresh scheduling
- Statistical counters for performance management

1.3.5 Region-based Address Translation Module (RAT)

Integrated in MAIN domain: One instance of the Region-based Address Translation (RAT) module to perform a region based address translation of a 32-bit input address into a 36-bit output address. The RAT module provides the following main features:

- 4 regions with dedicated registers for attributes configuration:
  - Region base address
  - Region size
  - Translated base address
- Address translation for only enabled regions
- Region boundary crossing transactions error generation

1.3.6 Data Movement Subsystem (DMSS)

Integrated in the MAIN domain:One Data Movement subsystem named DMSS can be used for efficient transfer of data support between software, firmware and hardware in all combinations. It consists of the following main modules:

- Packet DMA Controller
- Block Copy DMA Controller
- Ring Accelerator provides hardware acceleration to enable straightforward passing of work between a producer and a consumer and has the following main features:
  - Supports 1024 independent memory-mapped ring structures
  - Supports various modes for each ring based on usage and compatibility
  - Provides single-word deep shared incoming Transfer Response FIFO
  - Provides bit-wide source VBUSM read/write target interface for accesses from DMA controller entities
- Secure proxy module is a modified version of the proxy module and in addition has the following main features:
  - Supports a number of threads, where each has their own independent proxy function
  - Supports a programmable fixed queue for each proxy thread
  - Supports multiple producers all writing to the same queue
  - Supports programmable thresholds for when to generate events
  - Supports a max message count for outbound proxy threads limiting the number of messages a thread can produce
- Interrupt Aggregator modules provide a centralized machine which handles the termination of system events to that they can be coherently processed by the host(s) in the system. Main features are as follows:
  - 64-bit VBUSP target using 64-bit registers
  - Provide a set of TI Interrupt Architecture compliant interrupt status and mask registers which are used to pass specific event status to one or more host blocks.
  - Provide a set of Global Event Input (GEVI) counters which can count events delivered via an ingress Event Transport Lane (ETL)
  - Provides a set of Local Event Input (LEVI) to Global event registers which can be used to convert pulsed discrete interrupt inputs or clock synchronous rising edge events into Global events on an egress ETL
  - Provides a set of GEVI 'Multicast' registers which can take a Global event from an ingress ETL and generate two egress Global events on two egress ETL interfaces
- One Timer Manager module to support timing operations for the processes running on multiple processors, each with the following main features:
  - 1024 × 32-bit RAM-based independent timers (2048 in total)

  - Event interface to an interrupt aggregation module in the NAVSS subsystem with events triggering when a timer expires or when an expired timer is reset or deactivated
  - Host access to determine which timer(s) expired
  - 32 registers with individual timeout status (one bit per timer)
  - Groups of 16 timers separated into pages of 4-K address space
  - Timer bits within each page to read expiration status for each timer when software only has access to that page
  - 10 µs time to cycle through all of the timers
  - Host access to reset individual timers
  - Periodic hardware timers – a timer may be set to automatically reprogram itself upon expiration without software intervention.
- Time Sync modules to facilitate host control of time sync operations, each with the following main features:
  - Supports a selection of multiple external clock sources
  - Software control of time sync events via interrupt or polling
  - Supports 8 hardware timestamp push inputs
  - Supports timestamp counter compare output
  - Supports timestamp counter bit output
  - Supports 6 timestamp generator function outputs
  - 32-bit and 64-bit timestamp modes

1.3.7 Mailbox (MAILBOX)

Integrated in MAIN domain: One Mailbox (MAILBOX) module to facilitate the communication between the various on-chip processor cores of the device by providing a queued mailbox-interrupt mechanism with the following main features:

- 12x clusters
- 32-bit message width
- Message reception and queue-not-full notification using interrupts
- Non-intrusive emulation

1.3.8 Spinlock (SPINLOCK)

Integrated in MAIN domain: One Spinlock module with (256 hardware semaphores) for synchronizing the processes running on multiple cores in the device.

1.3.9 Analog-to-Digital Converter (ADC)

Integrated in MAIN domain: One instance of the Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels). The ADC provides the following main features:

- 4 MSPS rate with a 60 MHz sample clock
- Single-ended or differential input options
- ADC module can be configured and transformed into digital test inputs
- Programmable 16 steps Finite State Machine (FSM) sequencer

1.3.10 General Purpose Input/Output Interface (GPIO)

Integrated in MAIN domain: General Purpose Input/Output (GPIO) module that provide dedicated general-purpose pins that can be configured as either inputs or outputs. The GPIO module main features include:

- Support of 9 banks x 16 GPIO pins
- Support of up to 9 banks of interrupt capable GPIOs
- Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO pin
- Set/clear functionality per individual GPIO pin

1.3.11 Inter-Integrated Circuit Interface (I2C)

Integrated in MAIN domain: Seven instances of the multi-controller Inter-Integrated Circuit (I2C) interface module, each with the following main features:

- 2x Instances with open-drain voltage buffers in compliance with the Philips I2C-bus specification version 2.1
- Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Support of 7-bit and 10-bit device addressing modes
- 8-bit-wide data access
- Support of multi-controller transmitter/peripheral receiver and receiver/peripheral transmitter modes
- Built-in FIFOs with fixed size of 32 bytes.
- Support of Auto Idle, Idle Request/Idle Acknowledge handshake, and Asynchronous wake-up mechanisms
- Low power consumption

1.3.12 Serial Peripheral Interface (SPI)

Integrated in MAIN domain: Five instances of the Serial Peripheral Interface (SPI) module with the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four channels in controller mode, or single channel in receiver mode
- Support for various controller multichannel modes
- Single interrupt line for multiple interrupt source events
- Support of start-bit write command
- Support of start-bit pause and break sequence
- Built-in FIFO available for a single channel

1.3.13 Universal Asynchronous Receiver/Transmitter (UART)

Integrated in MAIN domain: Ten instances of the configurable Universal Asynchronous Receiver/Transmitter (UART) interface module with the following main features:

- 16C750-compatible interface
- Support of RS-485 external transceiver auto flow control
- Dual 64-byte FIFOs – one per each received and transmitted data paths
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode
- Baud-rate from 300 bits/s up to 3.6864 Mbits/s with 48 MHz functional clock
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Support of IrDA 1.4 Slow Infrared (SIR), Medium Infrared (MIR), and Fast Infrared (FIR) communications
- Support of Consumer Infrared Remote control mode (CIR) with programmable data encoding

1.3.14 3-port Gigabit Ethernet Switch (CPSW3G)

Integrated in MAIN domain: One instance of the 3-port Gigabit Ethernet Switch (CPSW3G) subsystem provides Ethernet packet communication for the device. The CPSW3G subsystem provides the following main features:

- Two external Ethernet ports with selectable RGMII and RMII interfaces and one internal Communications Port Programming Interface (CPPI) port.
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Support of eight priority level Quality Of Service (QOS) - 802.1p
- Support for Audio/Video Bridging (P802.1Qav/D6.0 and 802.1Qaz)
- Ethernet port reset isolation
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
- Differentiated Services Code Point (DSCP) Priority Mapping (IPv4 and IPv6)
- IPV4/IPV6 UDP/TCP checksum offload
- Priority Based Flow Control (801.1QBB) and Flow Control (802.3x) Support
- Wire rate switching (802.1d)
- Store and Forward Switching
- Non-Blocking switch fabric
- Support of Time Sensitive Network - IEEE P902.3br/D2.0 Interspersing Express Traffic and IEEE 802.1Qbv/D2.2 Enhancements for Scheduled Traffic

- Address Lookup Engine (ALE) with 512 ALE table entries
- EtherStats and 802.3 Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)
- Maximum frame size of 2020 bytes
- Management Data Input/Output (MDIO) module for PHY Management
- Host port CPPI Streaming Packet Interface
- Emulation support

1.3.15 Peripheral Component Interconnect Express Subsystem (PCIE)

Integrated in MAIN domain: One instance of the Peripheral Component Interconnect express (PCIe) subsystem module with shared SerDes lines, provides the following main features:

- Compliant to PCI-Express® Base Specification, Revision 4.0 (Version 0.7)
- 1-lane configuration with up to 5.0 Gbps/lane (Gen2). Can be used in 1x2 andS 1x1 modes
- Gen2 (5 Gbps 8/10-bit encoding), and Gen1 (2.5 Gbps 8/10-bit encoding) with auto-negotiation
- Dual mode: Root Port (RP) or End Point (EP) operation modes, selectable via bootstrap pins
- Dynamic PIPE width change when switching between Gen1/2/3 modes
- Constant 32-bit PIPE width for Gen1/2/3 modes
- Maximum payload size of 256 bytes
- Maximum remote read request size of 4KB
- Dual mode: Root Port (RP) or End Point (EP) operation modes
- Maximum number of non-posted outstanding transactions: 32
- Resizable Base Address Registers (BAR) capability
- Separate Reference Clock with Independent Spread (SRIS)
- Legacy, MSI and MSI-X Interrupt Support
- 32 outbound address translation regions
- Precision time measurement (PTM)

1.3.16 Serializer/Deserializer (SERDES)

Integrated in MAIN domain: One high-speed differential interface implemented with the Serializer/Deserializer (SERDES) Multi-protocol Multi-link module (shared between USB and PCIE) with the following main blocks:

- Quad lane PHY with common module for peripheral and Tx clocking handling
- PIPE Rev 4.2 Interface
- Physical coding sub-block for data translation from/to the parallel interface, as well as data encoding/decoding and symbol alignment
- MUX module for device interfaces multiplexing into a single SERDES lane (Tx and Rx)
- A wrapper for sending control and reporting status signals from the SerDes and muxes

1.3.17 Universal Serial Bus 3.1 Subsystem (USBSS)

Instantiated in MAIN domain: One instance of the Universal Serial Bus 3.1 subsystem (USBSS) with integrated USB2.0 PHY module has the following main features:

- Dual-Role Device (DRD) capability
- Compliant to the USB 3.1 Gen1 Specification
- Supports Peripheral/Device mode at High-Speed (HS at 480 Mbps), and Full-Speed (FS at 12 Mbps)
- Supports Host mode at Super-Speed (SS at 5 Gbps), High-Speed (HS at 480 Mbps), Full-Speed (FS at 12 Mbps), and Low-Speed (LS at 1.5 Mbps)
- Supports Host Negotiation Protocol (HNP)
- Supports USB3 low power protocol states (U1, U2, and U3)
- Single xHCI instance compliant to the xHCI 1.0 specification with internal DMA controller
- ECC on internal RAMs
- Embedded USB 2.0 PHY

1.3.18 General Purpose Memory Controller (GPMC)

Integrated in MAIN domain: One instance of the General-Purpose Memory Controller (GPMC) module. The GPMC is dedicated to interfacing with external memory devices and has the following main features:

- Support of 8- or 16-bit-wide data path to external memory devices
- Supports up to 4 independent chip-select regions of programmable size and programmable base addresses on 16MB, 32MB, 64MB, or 128MB boundary in a total address space of 1GB
- Support of the following wide range of external memories/devices:
  - Asynchronous or synchronous 8-bit wide memory or device (non-burst device)
  - Asynchronous or synchronous 16-bit wide memory or device
  - 16-bit non-multiplexed NOR flash device
  - 16-bit address and data multiplexed NOR flash device
  - 8-bit and 16-bit NAND flash device
  - 16-bit pseudo-SRAM (pSRAM) device
- Supports various interface protocols when communicating with external memory or external devices:
  - Asynchronous read/write access
  - Asynchronous read page access (4, 8, and 16 Word16)
  - Synchronous read/write access
  - Synchronous read burst access without wrap capability (4, 8, and 16 Word16)
  - Synchronous read burst access with wrap capability (4, 8, and 16 Word16)
- Supports up to 16-bit on-the-fly error code detection using the Bose-Chaudhuri-Hocquenghem (BCH) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)

1.3.19 Error Location Module (ELM)

Integrated in MAIN domain: One instance of the Error Location Module (ELM). The ELM module works in conjunction with the GPMC and has the following main features:

- ECC calculations (up to 16-bit) for NAND support and ability to work in both page-based and continuous modes
  - 4, 8, and 16 bits per 512-byte block error-location, based on BCH algorithms
  - Eight simultaneous processing contexts
  - Page-based and continuous modes
  - Interrupt generation on error-location process completion

1.3.20 Flash Subsystem (FSS) with Octal Serial Peripheral Interface (OSPI)

Integrated in MAIN domain: One instance of the Flash Subsystem (FSS) module provides access to external flash devices via Octal Serial Peripheral Interface (OSPI) along with encryption/decryption and in-line ECC protection. FSS supports the following main features:

- Provides one OSPI flash interfaces
- OSPI interface supports:
  - Execute in place (XIP) operation
  - 32-byte Block Copy (BC) operation
  - ECC
- OSPI supports up to 4 devices
- OSPI supports single, dual, quad, or octal SPI devices
- The OSPI interface has independent power management for low power operations

1.3.21 Multi-Media Card/Secure Digital Interface (MMCSD)

Integrated in MAIN domain: Two Multi-Media Card/Secure Digital (MMCSD) controller modules with the following main features:

- One controller with 8-bit wide data bus
- One controller with 4-bit wide data bus
- Support of eMMC5.1 Host Specification (JESD84-B51)
- Support of SD Host Controller Standard Specification - SDIO 3.00
- Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3
- eMMC Electrical Standard 5.1 (JESD84-B51)

- Multi-Media card features:
  - Backward compatible with earlier eMMC standards
  - Legacy MMC SDR: 1.8 V, 8/4/1-bit bus width, 0-25 MHz, 25/12.5/3.125 MB/s
  - High Speed SDR: 1.8 V, 8/4/1-bit bus width, 0-50 MHz, 50/25/6.25 MB/s
  - High Speed DDR: 1.8 V, 8/4-bit bus width, 0-50 MHz, 100/50 MB/s
  - HS200 SDR: 1.8 V, 0-200 MHz, 8/4-bit bus width, 200/100 MB/s
- SD card support: SDIO, SDR12, SDR25, SDR50, SDR104, DDR50
- System bus interface: CBA 4.0 VBUSM controller port with 64-bit data width and 64-bit address, little endian only
- Configuration bus interface: CBA 4.0 VBUSM with 32-bit data width, 32-bit aligned accesses only, linear incrementing addressing mode, little endian only

1.3.22 Enhanced Capture Module (ECAP)

Integrated in MAIN domain: Three Enhanced Capture (ECAP) modules provide accurate timing for different events. When not being used for event capture, its resources can be used to generate a single channel of asymmetrical PWM waveforms (configurable as either one capture input, or as one auxiliary PWM output). Each ECAP module supports the following main features:

- 32-bit time base counter
- 4 x 32 bits event time-stamp capture registers
- 4 stage sequencer (Mod4 counter), synchronized to external events
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- Interrupt capabilities on any of the four capture events
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or delta mode time-stamp capture)

1.3.23 Enhanced Pulse-Width Modulation Module (EPWM)

Integrated in MAIN domain: Nine Enhanced Pulse-Width Modulation (EPWM) modules, each with the following main features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs that can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

1.3.24 Enhanced Quadrature Encoder Pulse Module (EQEP)

Integrated in MAIN domain: Three 32-bit Enhanced Quadrature Encoder Pulse (EQEP) modules for position, speed, and frequency measurements support, each with the following main features:

- Input synchronization
- Three stage/six stage digital noise filter
- Quadrature decoder unit
- Position counter and control unit for position measurement
- Quadrature edge capture unit for low speed measurement
- Unit time base for speed/frequency measurement
- Watchdog timer for detecting stalls

1.3.25 Controller Area Network (MCAN)

Integrated in MAIN domain: Two Controller Area Network interfaces (MCAN) support both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications and have the following main features:

- Conforms with CAN Protocol version 2.0 part A, B and ISO 11898-1:2015
- Full CAN FD (up to 64 data bytes) support
- SAE J1939 support
- AUTOSAR support
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs, up to 64 elements each
- Configurable transmit FIFO, up to 32 elements
- Configurable transmit queue, up to 32 elements
- Configurable transmit event FIFO, up to 32 elements
- Up to 128 filter elements
- Maskable interrupts, two interrupt lines
- Timestamp Counter

1.3.26 Fast Serial Interface Receiver (FSI_RX)

Integrated in MAIN domain: Six Fast Serial Interface Receiver (FSI_RX) modules provide an interface to FSI-enabled C2000 devices, each FSI_RX supports the following features:

- Type 1 FSI Reciever
- Source Synchronous, Double Data Rate Protocol
- One or Two Data Lines (RXD0/RXD1)
- Skew Adjustment Block (Programmable delay lines on Clock and Data Inputs)
- Framing Error Detection
- CRC Protection
- Frame and Ping Watchdog
- Optional ECC Check / Correction (16 or 32 bit data)
- SPI Compatibility Signaling Mode

1.3.27 Fast Serial Interface Transmitter (FSI_TX)

Integrated in MAIN domain: Two instances of the Fast Serial Interface Transmitter (FSI_TX) module provide an interface to FSI-enabled C2000 devices, each FSI_TX supports the following features:

- Type 1 FSI Transmitter
- Source Synchronous, Double Data Rate Protocol
- One or Two Data Lines (TXD0/TXD1)
- CRC Protection
- Automatic Ping Frame Generation
- Optional ECC Syndrome Generator (16 or 32 bit data)
- SPI Compatibility Signaling Mode

1.3.28 Timers

Three different types of timer modules are instantiated in the MAIN domain:

- One instance of Global Time Counter (GTC) module that can be used for time synchronization and debug trace time stamping with the following main features:
  - 64-bit up counter
  - No rollover during the lifetime of the device
  - Compatible with Armv8 system counter requirements
  - Outputs reflected binary (Gray) encoded timer value for system timer bus distribution to other modules
  - Selectable counter bit output as a push event that can be used by CPTS modules, timers or interface protocols
- Four instances Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module providing timer functionality for operation systems and benchmarking code with the following main features:
  - Two independent 64 bit counter blocks
  - Four configurable compare registers for generating operating system ticks

  - Free running counter 0 can be incremented by either the internal pre-scale counter or by an external event
  - Selectable RTI clock input (derived from any of the available clock sources)
  - Fast enabling/disabling of events
- Twenty instances of the dual mode Timer (TIMER) module with support of the following main features:
  - Free running 32-bit upward counter
  - Generates a 1-ms tick with a 32.768-kHz functional clock sourced from the LFOSC
  - Interrupts generated on overflow, compare and capture
  - Supported modes of operation: compare and capture, auto-reload and start-stop
  - Programmable divider clock source (2^n, where n = [0-8])
  - Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
  - On-the-fly read/write register (while counting) for systems operation and benchmarking code

1.3.29 Internal Diagnostics Modules

Instantiated in MAIN domain are different internal diagnostics modules which provide monitoring and diagnostic functions required to achieve certain safety compliance levels:

- Six Dual Clock Comparator (DCC) modules, used to determine the accuracy of a clock signal during the time execution of an application, each having the following main features:
  - Two independent counter blocks count clock pulses from each clock source
  - Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
  - Configurable time base for error signal
  - Error signal generation when one of the clocks is out of spec
  - Clock frequency measurement
- One instance of Error Signaling Module (ESM) for safety-related events and/or errors aggregation from throughout the device into one location supports the following main features:
  - Up to 1024 level or pulse error event inputs
  - Selectable low and high priority interrupt error pin prioritization of each error event
  - Error signal routed out of device through MCU_ESM error signal
  - Configurable time base for error signal
  - Error forcing capability
  - Internal redundant flops on safety critical fields
- Multiple ECC aggregator modules supporting ECC mechanism for providing increased system reliability via reduction of memory software errors by allowing single bit errors to be detected and corrected (SEC) and double bit errors to be detected (DED). Applied to different memories in many of the subsystems, each of the ECC aggregators has the following main features:
  - Reduces memory software errors via single error correction (SEC) and double error detection (DED)
  - Provides a mechanism to control and monitor the ECC RAMs in a module or subsystem
  - Supports software readable status of ECC errors (single and double-bit) and associated info such as RAM address and data bit or bits that are in error
  - Aggregates level pending status from the ECC RAMs in two interrupts to the device CPU – interrupt for correctable error (SEC) and interrupt for uncorrectable error (DED)
  - Supports up to 256 ECC endpoints (either ECC RAM or interconnect ECC component)
  - Single bit error detection via parity checking results in a non-correctable error interrupt

1.4 Device MCU Domain

Device MCU Domain Functional Block Diagram

This section describes the modules integrated in the device MCU domain.

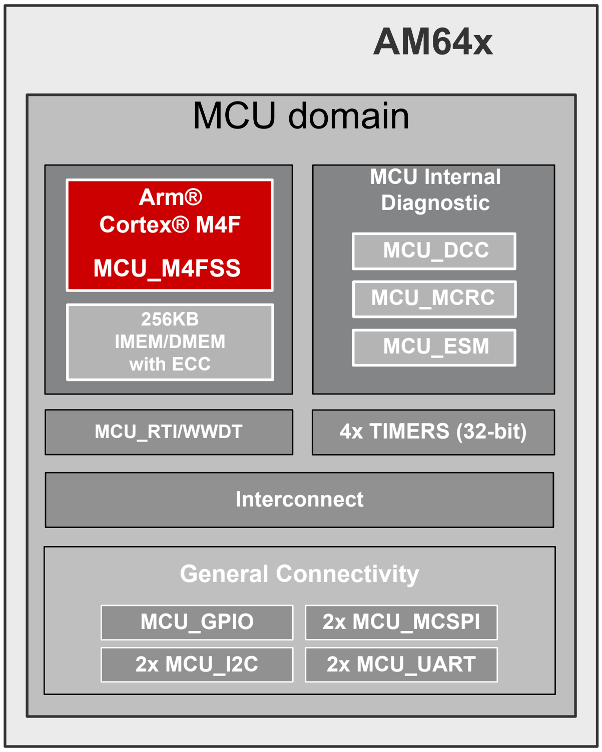

Figure 1-3. MCU Domain Function Block Diagram

Note

In TI documentation, the MCU Domain may be referred to as "M4FSS Island", "MCU Island", "MCU Channel", or "MCU Subsystem".

The Microcontroller Unit Domain (MCU Domain) is a “chip-in-a-chip” concept and it operates using separate clock sources and resets. This allows the MCU Domain to function continuously regardless of the state of the rest of the device, including periods in which the rest of the device is held in reset or powered down. The MCU island integrates communication peripherals such as SPI, I2C, and UART which are expected to be used for safety critical communication, so if the main SoC goes down, the MCU island can communicate this information to the rest of the system. Isolation of the MCU Arm Cortex-M4F Microcontroller Subsystem helps to provide Freedom From Interference (FFI).

1.4.1 MCU Arm Cortex M4F Subsystem (MCU_M4FSS)

Integrated in the MCU domain: One Arm Cortex-M4F Subsystem module. This processor core can be configured as an isolated safety MCU or general purpose MCU.

- Cortex M4F With Memory Protection Unit (MPU)
- ARMv7-M architecture
- Support for Nested Vectored Interrupt Controller (NVIC) with 64 inputs
- Ability to execute code from internal or external memories
- 192 KB of SRAM (I-Code)
- 64 KB of SRAM (D-Code)
- Debug Support Including:
  - DAP based Debug to the CPU Core
  - Full Debug Features of CPU Core are enabled
  - Standard ITM trace
  - CTM Cross Trigger
  - ETM Trace Support
- Fault Detection and Correction:

  - SECDED ECC protection on I-CODE
  - SECDED ECC protection on D-CODE
  - Fault Error Interrupt Output

1.4.2 MCU General Purpose Input/Output Interface (MCU_GPIO)

Integrated in MCU domain: One General Purpose Input/Output (MCU_GPIO) module provides dedicated general-purpose pins that can be configured as either inputs or outputs. the MCU_GPIO module includes these main features:

- Support of 9 banks x 16 GPIO pins
- Support of up to 9 banks of interrupt capable GPIOs
- Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO pin
- Set/clear functionality per individual GPIO pin

1.4.3 MCU Inter-Integrated Circuit Interface (MCU_I2C)

Integrated in MCU domain: Two multi-controller Inter-Integrated Circuit (MCU_I2C) interfaces, each with the following main features:

- Compliancy to the Philips I2C-bus specification version 2.1
- Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Support of 7-bit and 10-bit device addressing modes
- Support of multi-controller transmitter/peripheral receiver and receiver/peripheral transmitter modes
- Built-in FIFOs with programmable size of 8 to 64 bytes for buffered read or write
- 8-bit-wide data access
- Support of Auto Idle, Idle Request/Idle Acknowledge handshake, and Asynchronous Wakeup mechanisms
- Low power consumption

1.4.4 MCU Multi-channel Serial Peripheral Interface (MCU_SPI)

Integrated in MCU domain: Three Multi-channel Serial Peripheral Interface (MCU_SPI) modules where each have the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of MCSPI word lengths, ranging from 4 to 32 bits
- Up to four controller channels, or single channel in receiver mode
- Support of different controller multichannel modes
- Single interrupt line for multiple interrupt source events
- Support of start-bit write command
- Support of start-bit pause and break sequence
- Built-in FIFO available for a single channel

1.4.5 MCU Universal Asynchronous Receiver/Transmitter (MCU_UART)

Integrated in MCU domain: One configurable Universal Asynchronous Receiver/Transmitter (MCU_UART) interface with the following main features:

- Support of RS-485 external transceiver auto flow control
- Dual 64-byte FIFOs – one per each received and transmitted data paths
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode
- 16C750 compatible interface
- Baud rates up to 3.6 Mbps with 48 MHz functional clock
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Support of IrDA 1.4 Slow Infrared (SIR), Medium Infrared (MIR), and Fast Infrared (FIR) communications
- Support of Consumer Infrared Remote control mode (CIR) with programmable data encoding

1.4.6 MCU Timers

Two different types of timer modules are instantiated in the MCU domain:

- Two instances Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module providing timer functionality for operation systems and benchmarking code with the following main features:
  - Two independent 64 bit counter blocks
  - Four configurable compare registers for generating operating system ticks
  - Free running counter 0 can be incremented by either the internal pre-scale counter or by an external event
  - Selectable RTI clock input (derived from any of the available clock sources)
  - Windowed Watchdog Timer (WWDT) feature
  - Some RTI modules are pre-dedicated to specific processor cores
- Ten instances of Timer module with support of the following main features:
  - Free running 32-bit upward counter
  - Generates a 1-ms tick with a 32.768-kHz functional clock sourced from the LFOSC
  - Interrupts generated on overflow, compare and capture
  - Supported modes of operation: compare and capture, auto-reload and start-stop
  - Programmable divider clock source (2n, where n = [0-8])
  - Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
  - On-the-fly read/write register (while counting) for systems operation and benchmarking code
  - Each odd numbered timer instance may be optionally cascaded with the previous even numbered timer instance to form up to a 64-bit timer

1.4.7 MCU Internal Diagnostics Modules

Instantiated in MCU domain are different internal diagnostics modules which provide monitoring and diagnostic functions required to achieve certain safety compliance levels:

- One instance of the Dual Clock Comparator (MCU_DCC) module, used to determine the accuracy of a clock signal during the time execution of an application, each having the following main features:
  - Two independent counter blocks count clock pulses from each clock source
  - Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
  - Configurable time base for error signal
  - Error signal generation when one of the clocks is out of spec
  - Clock frequency measurement
- One instance of Error Signaling Module (MCU_ESM) for safety-related events and/or errors aggregation from throughout the device into one location supports the following main features:
  - Up to 1024 level or pulse error event inputs
  - Selectable low and high priority interrupt error pin prioritization of each error event
  - Single Error Pin output to signal severe device failure to outside world
  - Configurable time base for error signal
  - Triple Redundant Pulse Inputs
  - Two Priority Levels
  - Error Forcing capability
  - Internal redundant flops on safety critical fields
- Multiple ECC aggregator modules supporting ECC mechanism for providing increased system reliability via reduction of memory software errors by allowing single bit errors to be detected and corrected (SEC) and double bit errors to be detected (DED). Applied to different memories in many of the subsystems, each of the ECC aggregators has the following main features:
  - Reduces memory software errors via single error correction (SEC) and double error detection (DED)
  - Provides a mechanism to control and monitor the ECC RAMs in a module or subsystem
  - Supports software readable status of ECC errors (single and double-bit) and associated info such as RAM address and data bit or bits that are in error
  - Aggregates level pending status from the ECC RAMs in two interrupts to the device CPU – interrupt for correctable error (SEC) and interrupt for uncorrectable error (DED)
  - Supports up to 256 ECC endpoints (either ECC RAM or interconnect ECC component)

  - Single bit error detection via parity checking results in a non-correctable error interrupt
- Memory Cyclic Redundancy Check module used to perform CRC to verify the integrity of a memory system. The MCRC module has the following main feature:
  - Four Channels of CRC Compression based Signature Generation
  - 8, 16, 32, or 64-bit Data Size
  - Maximum Length PSA based on 64-bit Polynomial
  - Programmable 20 bit pattern counter per channel
  - Three Operating Modes: Auto, Semi-CPU, Full CPU
  - MCRC or CPU can perform signature verification for each Channel
  - Timeout Interrupt if CRC is not performed within the time limit

1.5 Device Identification

The device part number identification data can be read in the MAIN_CTRL_MMR_CFG0_JTAG_USER_ID register. See Table 1-1 for more information.

Table 1-1. Device Part Number Identifier

MAIN_CTRL_MMR_CFG0_JTAG_USER_ID Register Field	Value and Description	Comment
[31-13] DEVICE_ID	Base Part Number.	Refer to the Device Comparison section for the device specific Datasheet, for the DEVICE_ID value of a given part number.
[12] SAFETY	0 = Non Functional Safety 1 = Functional Safety	
[11] SECURITY	0 = Non-Secure 1 = Secure	
[10-6] SPEED	Device Speed Grade. 11 (0x0B) = K speed designator 13 (0x02) = S speed designator	Refer to the device-specific Datasheet for the supported speed grades and the definitions for a given device.
[5-3] TEMP	Temperature grade. 4 = -40°C to 105°C 5 = -40°C to 125°C Others = Reserved	Operating junction temperature range.
[2-0] PKG	Package 4 = ALV 5 = ALX Others = Reserved	Device Package type.

The manufacturer identity, the boundary scan part number, and the silicon revision of the device can be read in the MAIN_CTRL_MMR_CFG0_JTAGID register. See Table 1-2 and Table 1-3 tables for more information.

Table 1-2. Device JTAG ID

MAIN_CTRL_MMR_CFG0_JTAGID Register Field	Value	Comment
[31-28] VARIANT	See Table 1-3	Silicon Revision (SR) identifier.
[27-12] PARTNO	See Table 1-3	Part number for boundary scan.
[11-1] MFG	0x17	Manufacturer identity (TI).
[0] LSB	0x1	Always reads 1.

Table 1-3. Device JTAG ID Values

Silicon Type	VARIANT	PARTNO	MAIN_CTRL_MMR_CFG0_JTAGID Register Value
AM64x SR1.0	0x0	0xBB38	0x0BB3802F
AM243x SR1.0	0x0	0xBB38	0x0BB3802F
AM64x SR2.0	0x1	0xBB38	0x1BB3802F

Chapter 2

Memory Map

This chapter summarizes the memory map address regions for the device.

2.1 MAIN Memory Map

Table 2-1. MAIN Memory Map

Region Name	Start Address	End Address	Size
PSRAMECC0_RAM	0x0000000000	0x00000003FF	1KB
PADCFG_CTRL0_CFG0	0x00000F0000	0x00000F7FFF	32KB
CBASS_DBG0_ERR	0x0000200000	0x00002003FF	1KB
CBASS_INFRA1_ERR	0x0000210000	0x00002103FF	1KB
CBASS_FW0_ERR	0x0000220000	0x00002203FF	1KB
EFUSE0_MEM	0x0000300000	0x00003000FF	256B
PBIST0_PBIST	0x0000310000	0x00003103FF	1KB
COMPUTE_CLUSTER0_PBIST	0x0000330000	0x00003303FF	1KB
PSC0_PSC	0x0000400000	0x0000400FFF	4KB
PLLCTRL0_MEM	0x0000410000	0x00004101FF	512B
ESM0_CFG	0x0000420000	0x0000420FFF	4KB
DFTSS0_MEM	0x0000500000	0x00005003FF	1KB
DDPA0_K3_DDPA	0x0000580000	0x00005803FF	1KB
GPIO0	0x0000600000	0x00006000FF	256B
GPIO1	0x0000601000	0x00006010FF	256B
PLL0_CFG	0x0000680000	0x000068FFFF	64KB
PSRAMECC0_ECC_AGGR	0x0000700000	0x00007003FF	1KB
ECC_AGGR1_ECC_AGGR	0x0000701000	0x00007013FF	1KB
USB0_ECC_AGGR	0x0000703000	0x00007033FF	1KB
CPSW0_CPSW3_ECC	0x0000704000	0x00007043FF	1KB
MMCSD0_ECC_AGGR	0x0000706000	0x00007063FF	1KB
MMCSD0_ECC_AGGR	0x0000707000	0x00007073FF	1KB
MMCSD1_ECC_AGGR	0x0000708000	0x00007083FF	1KB
MMCSD1_ECC_AGGR	0x0000709000	0x00007093FF	1KB
SA2_UL0_ECC_AGGR	0x0000712000	0x00007123FF	1KB
FSS0_ECC_AGGR	0x0000716000	0x00007163FF	1KB
COMPUTE_CLUSTER0_ECC_AGGR	0x0000717000	0x00007173FF	1KB
COMPUTE_CLUSTER0_ECC_AGGR	0x0000717400	0x00007177FF	1KB
COMPUTE_CLUSTER0_ECC_AGGR	0x0000717800	0x0000717BFF	1KB
PCIE0_CORE_ECC_AGGR0	0x0000718000	0x00007183FF	1KB
PCIE0_CORE_ECC_AGGR1	0x0000719000	0x00007193FF	1KB
ADC0_ECC_REGS	0x000071A000	0x000071A3FF	1KB
DCC0_DCC2	0x0000800000	0x000080003F	64B
DCC1_DCC2	0x0000804000	0x000080403F	64B
DCC2_DCC2	0x0000808000	0x000080803F	64B
DCC3_DCC2	0x000080C000	0x000080C03F	64B
DCC4_DCC2	0x0000810000	0x000081003F	64B
DCC5_DCC2	0x0000814000	0x000081403F	64B
MAIN_GPIOMUX_INTROUTER0_INTR_ROUTER_CFG	0x0000A00000	0x0000A007FF	2KB
CMP_EVENT_INTROUTER0_INTR_ROUTER_CFG	0x0000A30000	0x0000A307FF	2KB
TIMESYNC_EVENT_INTROUTER0_INTR_ROUTER_CFG	0x0000A40000	0x0000A407FF	2KB
GTC0_CFG0	0x0000A80000	0x0000A803FF	1KB
GTC0_CFG1	0x0000A90000	0x0000A93FFF	16KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
GTC0_CFG2	0x0000AA0000	0x0000AA3FFF	16KB
GTC0_CFG3	0x0000AB0000	0x0000AB3FFF	16KB
VTM0_VTM_CFG1	0x0000B00000	0x0000B003FF	1KB
VTM0_VTM_CFG2	0x0000B01000	0x0000B013FF	1KB
VTM0_ECCAGGR_CFG	0x0000B02000	0x0000B023FF	1KB
PDMA0_REGS	0x0000C00000	0x0000C003FF	1KB
PDMA1_REGS	0x0000C01000	0x0000C013FF	1KB
GICSS0_GIC_TRANSLATER	0x0001000000	0x00013FFFFF	4MB
GICSS0_GIC	0x0001800000	0x00018FFFFF	1MB
TIMER0_CFG	0x0002400000	0x00024003FF	1KB
TIMER1_CFG	0x0002410000	0x00024103FF	1KB
TIMER2_CFG	0x0002420000	0x00024203FF	1KB
TIMER3_CFG	0x0002430000	0x00024303FF	1KB
TIMER4_CFG	0x0002440000	0x00024403FF	1KB
TIMER5_CFG	0x0002450000	0x00024503FF	1KB
TIMER6_CFG	0x0002460000	0x00024603FF	1KB
TIMER7_CFG	0x0002470000	0x00024703FF	1KB
TIMER8_CFG	0x0002480000	0x00024803FF	1KB
TIMER9_CFG	0x0002490000	0x00024903FF	1KB
TIMER10_CFG	0x00024A0000	0x00024A03FF	1KB
TIMER11_CFG	0x00024B0000	0x00024B03FF	1KB
UART0	0x0002800000	0x00028001FF	512B
UART1	0x0002810000	0x00028101FF	512B
UART2	0x0002820000	0x00028201FF	512B
UART3	0x0002830000	0x00028301FF	512B
UART4	0x0002840000	0x00028401FF	512B
UART5	0x0002850000	0x00028501FF	512B
UART6	0x0002860000	0x00028601FF	512B
PBIST3_PBIST	0x0003310000	0x00033103FF	1KB
PBIST2_PBIST	0x0003330000	0x00033303FF	1KB
MCU_PSC0_PSC	0x0004000000	0x0004000FFF	4KB
MCU_PLLCTRL0_MEM	0x0004020000	0x00040201FF	512B
MCU_PLL0_CFG	0x0004040000	0x0004040FFF	4KB
MCU_PADCFG_CTRL0_CFG0	0x0004080000	0x0004087FFF	32KB
MCU_ESM0_CFG	0x0004100000	0x0004100FFF	4KB
MCU_GPIO0	0x0004201000	0x00042010FF	256B
MCU_MCU_GPIOMUX_INTROUTER0_INTR_ROUTER_CFG	0x0004210000	0x00042101FF	512B
MCU_TIMEOUT0_CFG	0x0004300000	0x00043003FF	1KB
MCU_CTRL_MMR0_CFG0	0x0004500000	0x000451FFFF	128KB
MCU_ECC_AGGR0_ECC_AGGR	0x0004700000	0x00047003FF	1KB
MCU_CBASS0_ERR	0x0004720000	0x00047203FF	1KB
MCU_TIMER0_CFG	0x0004800000	0x00048003FF	1KB
MCU_TIMER1_CFG	0x0004810000	0x00048103FF	1KB
MCU_TIMER2_CFG	0x0004820000	0x00048203FF	1KB
MCU_TIMER3_CFG	0x0004830000	0x00048303FF	1KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
MCU_RTI0_CFG	0x0004880000	0x00048800FF	256B
MCU_I2C0_CFG	0x0004900000	0x00049000FF	256B
MCU_I2C1_CFG	0x0004910000	0x00049100FF	256B
MCU_UART0	0x0004A00000	0x0004A001FF	512B
MCU_UART1	0x0004A10000	0x0004A101FF	512B
MCU_MCSPI0_CFG	0x0004B00000	0x0004B003FF	1KB
MCU_MCSPI1_CFG	0x0004B10000	0x0004B103FF	1KB
MCU_DCC0_DCC2	0x0004C00000	0x0004C0003F	64B
MCU_MCRC64_0_MCRC64	0x0004D00000	0x0004D00FFF	4KB
MCU_M4FSS0_BLAZAR_IRAM	0x0005000000	0x000503FFFF	256KB
MCU_M4FSS0_IDRAM_SLV_RAM	0x0005040000	0x000504FFFF	64KB
MCU_M4FSS0_RAT	0x0005FF0000	0x0005FF0FFF	4KB
MCU_M4FSS0_ECC_AGGR	0x0005FF1000	0x0005FF13FF	1KB
CPSW0_CPSW3	0x0008000000	0x00081FFFFF	2MB
PCIE0_PCIE_RP_CORE	0x000D000000	0x000D7FFFFF	8MB
RTI0_CFG	0x000E000000	0x000E0000FF	256B
RTI1_CFG	0x000E010000	0x000E0100FF	256B
RTI8_CFG	0x000E080000	0x000E0800FF	256B
RTI9_CFG	0x000E090000	0x000E0900FF	256B
RTI10_CFG	0x000E0A0000	0x000E0A00FF	256B
RTI11_CFG	0x000E0B0000	0x000E0B00FF	256B
SERDES_10G0_WIZ16B2M4CT	0x000F000000	0x000F00FFFF	64KB
PCIE0_CORE_USER_CFG_USER_CFG	0x000F100000	0x000F1003FF	1KB
PCIE0_CORE_VMAP_OB_MMRS	0x000F101000	0x000F101FFF	4KB
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0x000F102000	0x000F102FFF	4KB
PCIE0_CORE_CPTS_CFG_CPTS_VBUSP	0x000F103000	0x000F1033FF	1KB
DDR16SS0_EMIF_SSCFG	0x000F300000	0x000F3001FF	512B
DDR16SS0_EMIF_CTLCFG	0x000F308000	0x000F30FFFF	32KB
USB0_VBP2APB_WRAP_CONTROLLER_VBP_CORE_ADDR_MAP	0x000F400000	0x000F43FFFF	256KB
USB0_MMR_MMRVBP_USBSS_CMN	0x000F900000	0x000F9000FF	256B
USB0_RAMS_INJ_CFG	0x000F901000	0x000F9013FF	1KB
USB0_PHY2	0x000F908000	0x000F9083FF	1KB
MMCSD1_MMC_CTLCFG	0x000FA00000	0x000FA00FFF	4KB
MMCSD1_MMC_SSCFG	0x000FA08000	0x000FA083FF	1KB
MMCSD0_MMC_CTLCFG	0x000FA10000	0x000FA10FFF	4KB
MMCSD0_MMC_SSCFG	0x000FA18000	0x000FA183FF	1KB
FSS0_FSS_GENREGS	0x000FC00000	0x000FC000FF	256B
FSS0_FSAS_GENREGS	0x000FC10000	0x000FC100FF	256B
FSS0_OTFA_CFG	0x000FC20000	0x000FC20FFF	4KB
FSS0_OSPI_FLASH_CFG	0x000FC40000	0x000FC400FF	256B
FSS0_OSPI_CFG	0x000FC44000	0x000FC441FF	512B
I2C0_CFG	0x0020000000	0x00200000FF	256B
I2C1_CFG	0x0020010000	0x00200100FF	256B
I2C2_CFG	0x0020020000	0x00200200FF	256B
I2C3_CFG	0x0020030000	0x00200300FF	256B

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
MCSPI0_CFG	0x0020100000	0x00201003FF	1KB
MCSPI1_CFG	0x0020110000	0x00201103FF	1KB
MCSPI2_CFG	0x0020120000	0x00201203FF	1KB
MCSPI3_CFG	0x0020130000	0x00201303FF	1KB
MCSPI4_CFG	0x0020140000	0x00201403FF	1KB
MCAN0_SS	0x0020700000	0x00207000FF	256B
MCAN0_CFG	0x0020701000	0x00207011FF	512B
MCAN0_MSGMEM_WRAP_MSGMEM_VBP_RAM	0x0020708000	0x002070FFFF	32KB
MCAN1_SS	0x0020710000	0x00207100FF	256B
MCAN1_CFG	0x0020711000	0x00207111FF	512B
MCAN1_MSGMEM_WRAP_MSGMEM_VBP_RAM	0x0020718000	0x002071FFFF	32KB
EPWM0_EPWM	0x0023000000	0x00230000FF	256B
EPWM1_EPWM	0x0023010000	0x00230100FF	256B
EPWM2_EPWM	0x0023020000	0x00230200FF	256B
EPWM3_EPWM	0x0023030000	0x00230300FF	256B
EPWM4_EPWM	0x0023040000	0x00230400FF	256B
EPWM5_EPWM	0x0023050000	0x00230500FF	256B
EPWM6_EPWM	0x0023060000	0x00230600FF	256B
EPWM7_EPWM	0x0023070000	0x00230700FF	256B
EPWM8_EPWM	0x0023080000	0x00230800FF	256B
ECAP0_CTL_STS	0x0023100000	0x00231000FF	256B
ECAP1_CTL_STS	0x0023110000	0x00231100FF	256B
ECAP2_CTL_STS	0x0023120000	0x00231200FF	256B
EQEP0_REG	0x0023200000	0x00232000FF	256B
EQEP1_REG	0x0023210000	0x00232100FF	256B
EQEP2_REG	0x0023220000	0x00232200FF	256B
FSIRX0_FSI_RX_CFG	0x0023500000	0x00235000FF	256B
FSIRX1_FSI_RX_CFG	0x0023510000	0x00235100FF	256B
FSIRX2_FSI_RX_CFG	0x0023520000	0x00235200FF	256B
FSIRX3_FSI_RX_CFG	0x0023530000	0x00235300FF	256B
FSIRX4_FSI_RX_CFG	0x0023540000	0x00235400FF	256B
FSIRX5_FSI_RX_CFG	0x0023550000	0x00235500FF	256B
FSITX0_FSI_TX_CFG	0x0023600000	0x00236000FF	256B
FSITX1_FSI_TX_CFG	0x0023610000	0x00236100FF	256B
MCAN0_ECC_AGGR	0x0024018000	0x00240183FF	1KB
MCAN1_ECC_AGGR	0x0024019000	0x00240193FF	1KB
ELM0	0x0025010000	0x0025010FFF	4KB
ADC0_FIFO	0x0028000000	0x00280003FF	1KB
ADC0	0x0028001000	0x00280013FF	1KB
MAILBOX0_REGS0	0x0029000000	0x00290001FF	512B
MAILBOX0_REGS1	0x0029010000	0x00290101FF	512B
MAILBOX0_REGS2	0x0029020000	0x00290201FF	512B
MAILBOX0_REGS3	0x0029030000	0x00290301FF	512B
MAILBOX0_REGS4	0x0029040000	0x00290401FF	512B
MAILBOX0_REGS5	0x0029050000	0x00290501FF	512B

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
MAILBOX0_REGS6	0x0029060000	0x00290601FF	512B
MAILBOX0_REGS7	0x0029070000	0x00290701FF	512B
SPINLOCK0_SPINLOCK	0x002A000000	0x002A007FFF	32KB
PRU_ICSSG0_DRAM0_SLV_RAM	0x0030000000	0x0030001FFF	8KB
PRU_ICSSG0_DRAM1_SLV_RAM	0x0030002000	0x0030003FFF	8KB
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_RAM	0x0030004000	0x0030005FFF	8KB
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_RAM	0x0030006000	0x0030007FFF	8KB
PRU_ICSSG0_RAT	0x0030008000	0x0030008FFF	4KB
PRU_ICSSG0_RAT	0x0030009000	0x0030009FFF	4KB
PRU_ICSSG0_PR1_PDSP_TX0_IRAM_RAM	0x003000A000	0x003000BFFF	8KB
PRU_ICSSG0_PR1_PDSP_TX1_IRAM_RAM	0x003000C000	0x003000DFFF	8KB
PRU_ICSSG0_RAM_SLV_RAM	0x0030010000	0x003001FFFF	64KB
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0x0030020000	0x0030021FFF	8KB
PRU_ICSSG0_PR1_PDSP0_IRAM	0x0030022000	0x00300220FF	256B
PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG	0x0030022400	0x00300224FF	256B
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0x0030023000	0x00300230FF	256B
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0x0030023400	0x00300234FF	256B
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0x0030023800	0x00300238FF	256B
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0x0030023C00	0x0030023CFF	256B
PRU_ICSSG0_PR1_PDSP1_IRAM	0x0030024000	0x00300240FF	256B
PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG	0x0030024400	0x00300244FF	256B
PRU_ICSSG0_PR1_PROTECT_SLV	0x0030024C00	0x0030024CFF	256B
PRU_ICSSG0_PR1_PDSP_TX0_IRAM	0x0030025000	0x00300250FF	256B
PRU_ICSSG0_PR1_PDSP_TX0_IRAM_DEBUG	0x0030025400	0x00300254FF	256B
PRU_ICSSG0_PR1_PDSP_TX1_IRAM	0x0030025800	0x00300258FF	256B
PRU_ICSSG0_PR1_PDSP_TX1_IRAM_DEBUG	0x0030025C00	0x0030025CFF	256B
PRU_ICSSG0_PR1_CFG_SLV	0x0030026000	0x00300261FF	512B
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_QSTAT	0x0030027000	0x00300277FF	2KB
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0x0030028000	0x003002803F	64B
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0x003002A000	0x003002A0FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0x003002A100	0x003002A1FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0x003002A200	0x003002A2FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0x003002A300	0x003002A3FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	0x003002A400	0x003002A4FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	0x003002A500	0x003002A5FF	256B
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_CSTAT	0x003002C000	0x003002C7FF	2KB
PRU_ICSSG0_PR1_IEP0_SLV	0x003002E000	0x003002EFFF	4KB
PRU_ICSSG0_PR1_IEP1_SLV	0x003002F000	0x003002FFFF	4KB
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0x0030030000	0x00300300FF	256B
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0x0030032000	0x00300320FF	256B
PRU_ICSSG0_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0x0030032100	0x00300321FF	256B
PRU_ICSSG0_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0x0030032200	0x00300322FF	256B
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0x0030032400	0x00300324FF	256B
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0x0030033000	0x0030033FFF	4KB
PRU_ICSSG0_PR1_PDSP0_IRAM_RAM	0x0030034000	0x0030037FFF	16KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
PRU_ICSSG0_PR1_PDSP1_IRAM_RAM	0x0030038000	0x003003BFFF	16KB
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	0x003003C000	0x003003C0FF	256B
PRU_ICSSG1_DRAM0_SLV_RAM	0x0030080000	0x0030081FFF	8KB
PRU_ICSSG1_DRAM1_SLV_RAM	0x0030082000	0x0030083FFF	8KB
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_RAM	0x0030084000	0x0030085FFF	8KB
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_RAM	0x0030086000	0x0030087FFF	8KB
PRU_ICSSG1_RAT	0x0030088000	0x0030088FFF	4KB
PRU_ICSSG1_RAT	0x0030089000	0x0030089FFF	4KB
PRU_ICSSG1_PR1_PDSP_TX0_IRAM_RAM	0x003008A000	0x003008BFFF	8KB
PRU_ICSSG1_PR1_PDSP_TX1_IRAM_RAM	0x003008C000	0x003008DFFF	8KB
PRU_ICSSG1_RAM_SLV_RAM	0x0030090000	0x003009FFFF	64KB
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0x00300A0000	0x00300A1FFF	8KB
PRU_ICSSG1_PR1_PDSP0_IRAM	0x00300A2000	0x00300A20FF	256B
PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG	0x00300A2400	0x00300A24FF	256B
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0x00300A3000	0x00300A30FF	256B
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0x00300A3400	0x00300A34FF	256B
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0x00300A3800	0x00300A38FF	256B
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0x00300A3C00	0x00300A3CFF	256B
PRU_ICSSG1_PR1_PDSP1_IRAM	0x00300A4000	0x00300A40FF	256B
PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG	0x00300A4400	0x00300A44FF	256B
PRU_ICSSG1_PR1_PROTECT_SLV	0x00300A4C00	0x00300A4CFF	256B
PRU_ICSSG1_PR1_PDSP_TX0_IRAM	0x00300A5000	0x00300A50FF	256B
PRU_ICSSG1_PR1_PDSP_TX0_IRAM_DEBUG	0x00300A5400	0x00300A54FF	256B
PRU_ICSSG1_PR1_PDSP_TX1_IRAM	0x00300A5800	0x00300A58FF	256B
PRU_ICSSG1_PR1_PDSP_TX1_IRAM_DEBUG	0x00300A5C00	0x00300A5CFF	256B
PRU_ICSSG1_PR1_CFG_SLV	0x00300A6000	0x00300A61FF	512B
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_QSTAT	0x00300A7000	0x00300A77FF	2KB
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0x00300A8000	0x00300A803F	64B
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0x00300AA000	0x00300AA0FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0x00300AA100	0x00300AA1FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0x00300AA200	0x00300AA2FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0x00300AA300	0x00300AA3FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	0x00300AA400	0x00300AA4FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	0x00300AA500	0x00300AA5FF	256B
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_CSTAT	0x00300AC000	0x00300AC7FF	2KB
PRU_ICSSG1_PR1_IEP0_SLV	0x00300AE000	0x00300AEFFF	4KB
PRU_ICSSG1_PR1_IEP1_SLV	0x00300AF000	0x00300AFFFF	4KB
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0x00300B0000	0x00300B00FF	256B
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0x00300B2000	0x00300B20FF	256B
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0x00300B2100	0x00300B21FF	256B
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0x00300B2200	0x00300B22FF	256B
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0x00300B2400	0x00300B24FF	256B
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0x00300B3000	0x00300B3FFF	4KB
PRU_ICSSG1_PR1_PDSP0_IRAM_RAM	0x00300B4000	0x00300B7FFF	16KB
PRU_ICSSG1_PR1_PDSP1_IRAM_RAM	0x00300B8000	0x00300BBFFF	16KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	0x00300BC000	0x00300BC0FF	256B
TIMERMGR0_TIMER_MGR_TIMERS	0x0037000000	0x003703FFFF	256KB
CPTS0_CPTS	0x0039000000	0x00390003FF	1KB
CBASS0_ERR	0x003A000000	0x003A0003FF	1KB
GPMC0_CFG	0x003B000000	0x003B0003FF	1KB
R5FSS0_ECC_AGGR	0x003C010000	0x003C0103FF	1KB
R5FSS0_EVNT_BUS_VBUSP_MMRS	0x003C018000	0x003C0180FF	256B
R5FSS1_ECC_AGGR	0x003C030000	0x003C0303FF	1KB
R5FSS1_EVNT_BUS_VBUSP_MMRS	0x003C038000	0x003C0380FF	256B
TIMERMGR0_CONFIG	0x003CD00000	0x003CD001FF	512B
MSRAM_256K0_ECC_AGGR	0x003F001000	0x003F0013FF	1KB
MSRAM_256K1_ECC_AGGR	0x003F002000	0x003F0023FF	1KB
MSRAM_256K2_ECC_AGGR	0x003F003000	0x003F0033FF	1KB
GICSS0_REGS	0x003F004000	0x003F0043FF	1KB
DMASS0_ECCAGGR	0x003F005000	0x003F0053FF	1KB
MSRAM_256K5_ECC_AGGR	0x003F006000	0x003F0063FF	1KB
MSRAM_256K4_ECC_AGGR	0x003F007000	0x003F0073FF	1KB
MSRAM_256K3_ECC_AGGR	0x003F008000	0x003F0083FF	1KB
DMSC0_ECC_AGGR	0x003F009000	0x003F0093FF	1KB
PRU_ICSSG0_ECC_AGGR	0x003F00A000	0x003F00A3FF	1KB
PRU_ICSSG1_ECC_AGGR	0x003F00B000	0x003F00B3FF	1KB
R5FSS0_ECC_AGGR	0x003F00D000	0x003F00D3FF	1KB
R5FSS1_ECC_AGGR	0x003F00E000	0x003F00E3FF	1KB
ECC_AGGR0_ECC_AGGR	0x003F00F000	0x003F00F3FF	1KB
MSRAM_256K6_ECC_AGGR	0x003F010000	0x003F0103FF	1KB
MSRAM_256K7_ECC_AGGR	0x003F011000	0x003F0113FF	1KB
PBIST1_PBIST	0x003F100000	0x003F1003FF	1KB
SA2_UL0_SA_UL_PRIMARY	0x0040900000	0x0040900FFF	4KB
SA2_UL0_SA_UL_UPDATES	0x0040901000	0x00409011FF	512B
SA2_UL0_SA_UL_RNG	0x0040910000	0x004091007F	128B
SA2_UL0_CP_ACE_PKA_EIP29T2	0x0040920000	0x004092FFFF	64KB
DEBUGSS0_SYS	0x0041000000	0x0041000FFF	4KB
ROM0_ROM	0x0041800000	0x004183FFFF	256KB
STM0_STIMULUS	0x0042000000	0x0042FFFFFF	16MB
CTRL_MMR0_CFG0	0x0043000000	0x004301FFFF	128KB
DMSC0_DMSC_SRAM0	0x0044040000	0x004404FFFF	64KB
DMSC0_DMSC_SRAM1	0x0044050000	0x004405FFFF	64KB
MSRAM_256K7_RAM	0x0044060000	0x004407FFFF	128KB
MSRAM_256K7_RAM	0x0044080000	0x004409FFFF	128KB
MSRAM_256K6_RAM	0x00440A0000	0x00440BFFFF	128KB
MSRAM_256K6_RAM	0x00440C0000	0x00440DFFFF	128KB
DMSC0_PWR	0x0044130000	0x00441307FF	2KB
DMSC0_DMTIMER0	0x0044133000	0x00441333FF	1KB
DMSC0_DMTIMER1	0x0044134000	0x00441343FF	1KB
DMSC0_RTI	0x0044135000	0x00441350FF	256B

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
DMSC0_RTI	0x0044135100	0x00441351FF	256B
DMSC0_DMSC_RAT_MMRS	0x0044200000	0x0044200FFF	4KB
DMSC0_SEC	0x0044230000	0x0044230FFF	4KB
DMSC0_SECMGR	0x0044234000	0x0044237FFF	16KB
DMSC0_DMTIMER2	0x0044238000	0x00442383FF	1KB
DMSC0_DMTIMER3	0x0044239000	0x00442393FF	1KB
DMSC0_AES	0x004423C000	0x004423DFFF	8KB
DMSC0_INTAGGR_INTR	0x0044300000	0x004437FFFF	512KB
DMSC0_INTAGGR_IMAP	0x0044400000	0x00444007FF	2KB
DMSC0_INTAGGR_CFG	0x0044410000	0x004441001F	32B
CBASS0_FW	0x0045000000	0x0045007FFF	32KB
DMSC0_DMSC_FW_VBUS_CFG	0x0045000000	0x0045FFFFFF	16MB
CBASS_INFRA1_FW	0x0045008000	0x0045008FFF	4KB
DMSC0_CBASS_FW	0x0045080000	0x004509FFFF	128KB
DMSC0_CBASS_ISC	0x0045808000	0x0045808FFF	4KB
CBASS_INFRA1_ISC	0x0045820000	0x0045820FFF	4KB
MCU_CBASS0_ISC	0x0045830000	0x00458303FF	1KB
DMASS0_CBASS_DMSC_ISC	0x0045840000	0x00458407FF	2KB
DMASS0_RINGACC_ISC	0x0045848000	0x00458483FF	1KB
CBASS0_ISC	0x0045880000	0x004588FFFF	64KB
MAIN_SEC_MMR0_CFG2	0x0045900000	0x004591FFFF	128KB
MAIN_SEC_MMR0_CFG0	0x0045A00000	0x0045A1FFFF	128KB
DMSC0_CBASS_GLB	0x0045B00000	0x0045B003FF	1KB
CBASS_INFRA1_GLB	0x0045B01000	0x0045B013FF	1KB
MCU_CBASS0_GLB	0x0045B02000	0x0045B023FF	1KB
DMASS0_CBASS_DMSC_GLB	0x0045B03000	0x0045B033FF	1KB
CBASS0_GLB	0x0045B08000	0x0045B083FF	1KB
CBASS_INFRA1_QOS	0x0045D20000	0x0045D20FFF	4KB
MCU_CBASS0_QOS	0x0045D30000	0x0045D303FF	1KB
DMASS0_CBASS_DMSC_QOS	0x0045D40000	0x0045D407FF	2KB
CBASS0_QOS	0x0045D80000	0x0045D8FFFF	64KB
DMASS0_INTAGGR_INTR	0x0048000000	0x00480FFFFF	1MB
DMASS0_INTAGGR_IMAP	0x0048100000	0x0048103FFF	16KB
DMASS0_INTAGGR_CFG	0x0048110000	0x004811001F	32B
DMASS0_INTAGGR_L2G	0x0048120000	0x00481203FF	1KB
DMASS0_PSILCFG_PROXY	0x0048130000	0x00481301FF	512B
DMASS0_PSILSS_MMRS	0x0048140000	0x0048140FFF	4KB
DMASS0_INTAGGR_UNMAP	0x0048180000	0x004819FFFF	128KB
DMASS0_INTAGGR_MCAST	0x0048210000	0x0048210FFF	4KB
DMASS0_INTAGGR_GCNTCFG	0x0048220000	0x0048221FFF	8KB
DMASS0_ETLSW_MMRS	0x0048230000	0x0048230FFF	4KB
DMASS0_RINGACC_GCFG	0x0048240000	0x00482403FF	1KB
DMASS0_SEC_PROXY_MMRS	0x0048250000	0x00482500FF	256B
DMASS0_BCDMA_CRED	0x0048400000	0x00484007FF	2KB
DMASS0_PKTDMA_CRED	0x0048410000	0x0048411FFF	8KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
DMASS0_BCDMA_BCHAN	0x0048420000	0x0048421FFF	8KB
DMASS0_PKTDMA_RFLOW	0x0048430000	0x0048433FFF	16KB
DMASS0_PKTDMA_TCHAN	0x00484A0000	0x00484A3FFF	16KB
DMASS0_BCDMA_TCHAN	0x00484A4000	0x00484A5FFF	8KB
DMASS0_PKTDMA_RCHAN	0x00484C0000	0x00484C1FFF	8KB
DMASS0_BCDMA_RCHAN	0x00484C2000	0x00484C3FFF	8KB
DMASS0_PKTDMA_GCFG	0x00485C0000	0x00485C00FF	256B
DMASS0_BCDMA_GCFG	0x00485C0100	0x00485C01FF	256B
DMASS0_PKTDMA_RING	0x00485E0000	0x00485FFFFF	128KB
DMASS0_BCDMA_RING	0x0048600000	0x0048607FFF	32KB
DMASS0_RINGACC_RT	0x0049000000	0x00493FFFFF	4MB
DMASS0_RINGACC_CFG	0x0049800000	0x004983FFFF	256KB
DMASS0_INTAGGR_GCNTRTI	0x004A000000	0x004A0FFFFF	1MB
DMASS0_SEC_PROXY_SCFG	0x004A400000	0x004A47FFFF	512KB
DMASS0_SEC_PROXY_RT	0x004A600000	0x004A67FFFF	512KB
DMASS0_PKTDMA_RCHANRT	0x004A800000	0x004A81FFFF	128KB
DMASS0_BCDMA_RCHANRT	0x004A820000	0x004A83FFFF	128KB
DMASS0_PKTDMA_TCHANRT	0x004AA00000	0x004AA3FFFF	256KB
DMASS0_BCDMA_TCHANRT	0x004AA40000	0x004AA5FFFF	128KB
DMASS0_PKTDMA_RINGRT	0x004B800000	0x004BBFFFFF	4MB
DMASS0_BCDMA_RINGRT	0x004BC00000	0x004BCFFFFF	1MB
DMASS0_BCDMA_BCHANRT	0x004C000000	0x004C01FFFF	128KB
DMASS0_SEC_PROXY_SRC_TARGET_DATA	0x004D000000	0x004D07FFFF	512KB
DMASS0_RINGACC_SRC_FIFOS	0x004E000000	0x004E3FFFFF	4MB
GPMC0_GPMC_DATA	0x0050000000	0x0057FFFFFF	128MB
FSS0_DAT_REG1	0x0060000000	0x0067FFFFFF	128MB
PCIE0_PCIE_RP_DAT0	0x0068000000	0x006FFFFFFF	128MB
MSRAM_256K0_RAM	0x0070000000	0x007003FFFF	256KB
MSRAM_256K1_RAM	0x0070040000	0x007007FFFF	256KB
MSRAM_256K2_RAM	0x0070080000	0x00700BFFFF	256KB
MSRAM_256K3_RAM	0x00700C0000	0x00700FFFFF	256KB
MSRAM_256K4_RAM	0x0070100000	0x007013FFFF	256KB
MSRAM_256K5_RAM	0x0070140000	0x007017FFFF	256KB
MSRAM_256K6_RAM	0x0070180000	0x00701BFFFF	256KB
MSRAM_256K7_RAM	0x00701C0000	0x00701FFFFF	256KB
R5FSS0_ICACHE0	0x0074000000	0x00747FFFFF	8MB
R5FSS0_DCACHE0	0x0074800000	0x0074FFFFFF	8MB
R5FSS0_ICACHE1	0x0075000000	0x00757FFFFF	8MB
R5FSS0_DCACHE1	0x0075800000	0x0075FFFFFF	8MB
R5FSS1_ICACHE0	0x0076000000	0x00767FFFFF	8MB
R5FSS1_DCACHE0	0x0076800000	0x0076FFFFFF	8MB
R5FSS1_ICACHE1	0x0077000000	0x00777FFFFF	8MB
R5FSS1_DCACHE1	0x0077800000	0x0077FFFFFF	8MB
R5FSS0_ATCM0(1)	0x0078000000	0x007800FFFF	64KB
R5FSS0_BTCM0(1)	0x0078100000	0x007810FFFF	64KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
R5FSS0_ATCM1(1)	0x0078200000	0x0078207FFF	32KB
R5FSS0_BTCM1(1)	0x0078300000	0x0078307FFF	32KB
R5FSS1_ATCM0(1)	0x0078400000	0x007840FFFF	64KB
R5FSS1_BTCM0(1)	0x0078500000	0x007850FFFF	64KB
R5FSS1_ATCM1(1)	0x0078600000	0x0078607FFF	32KB
R5FSS1_BTCM1(1)	0x0078700000	0x0078707FFF	32KB
DDR16SS0_EMIF_DDRDATA	0x0080000000	0x00FFFFFFFF	2GB
FSS0_DAT_REG0	0x0400000000	0x04FFFFFFFF	4GB
FSS0_DAT_REG3	0x0500000000	0x05FFFFFFFF	4GB
PCIE0_PCIE_RP_DAT1	0x0600000000	0x06FFFFFFFF	4GB
DEBUGSS_WRAP0_ROM_TABLE_0_0	0x0700000000	0x0700000FFF	4KB
DEBUGSS_WRAP0_RESV0_0	0x0700001000	0x0700001FFF	4KB
DEBUGSS_WRAP0_CFGAP_CFG_0	0x0700002000	0x07000020FF	256B
DEBUGSS_WRAP0_APBAP_CFG_0	0x0700002100	0x07000021FF	256B
DEBUGSS_WRAP0_AXIAP_CFG_0	0x0700002200	0x07000022FF	256B
DEBUGSS_WRAP0_PWRAP_CFG_0	0x0700002300	0x07000023FF	256B
DEBUGSS_WRAP0_PVIEW_CFG_0	0x0700002400	0x07000024FF	256B
DEBUGSS_WRAP0_JTAGAP_CFG_0	0x0700002500	0x07000025FF	256B
DEBUGSS_WRAP0_SECAP_CFG_0	0x0700002600	0x07000026FF	256B
DEBUGSS_WRAP0_CORTEX0_CFG_0	0x0700002700	0x07000027FF	256B
DEBUGSS_WRAP0_CORTEX1_CFG_0	0x0700002800	0x07000028FF	256B
DEBUGSS_WRAP0_CORTEX2_CFG_0	0x0700002900	0x07000029FF	256B
DEBUGSS_WRAP0_CORTEX3_CFG_0	0x0700002A00	0x0700002AFF	256B
DEBUGSS_WRAP0_CORTEX4_CFG_0	0x0700002B00	0x0700002BFF	256B
DEBUGSS_WRAP0_CORTEX5_CFG_0	0x0700002C00	0x0700002CFF	256B
DEBUGSS_WRAP0_CORTEX6_CFG_0	0x0700002D00	0x0700002DFF	256B
DEBUGSS_WRAP0_CORTEX7_CFG_0	0x0700002E00	0x0700002EFF	256B
DEBUGSS_WRAP0_CORTEX8_CFG_0	0x0700002F00	0x0700002FFF	256B
DEBUGSS_WRAP0_RESV1_0	0x0700003000	0x0700003FFF	4KB
DEBUGSS_WRAP0_RESV2_0	0x0700004000	0x0702003FFF	32MB
DEBUGSS_WRAP0_ROM_TABLE_1_0	0x0720000000	0x0720000FFF	4KB
DEBUGSS_WRAP0_CSCTI	0x0720001000	0x0720001FFF	4KB
DEBUGSS_WRAP0_DRM_CFG_0	0x0720002000	0x0720002FFF	4KB
DEBUGSS_WRAP0_RESV3_0	0x0720003000	0x0720003FFF	4KB
DEBUGSS_WRAP0_CSTPIU_CFG_0	0x0720004000	0x0720004FFF	4KB
DEBUGSS_WRAP0_CTF_CFG_0	0x0720005000	0x0720005FFF	4KB
DEBUGSS_WRAP0_RESV4_0	0x0720006000	0x0721005FFF	16MB
COMPUTE_CLUSTER0_APBADDR_ROMV8	0x0730000000	0x073000FFFF	64KB
DEBUGSS_WRAP0_EXT_APB_0	0x0730000000	0x073FFFFFFF	256MB
COMPUTE_CLUSTER0_APBADDR_DBG_CPU0	0x0730010000	0x073001FFFF	64KB
COMPUTE_CLUSTER0_APBADDR_CTI_CPU0	0x0730020000	0x073002FFFF	64KB
COMPUTE_CLUSTER0_APBADDR_PMU_CPU0	0x0730030000	0x073003FFFF	64KB
COMPUTE_CLUSTER0_APBADDR_ETM_CPU0	0x0730040000	0x073004FFFF	64KB
COMPUTE_CLUSTER0_APBADDR_DBG_CPU1	0x0730110000	0x073011FFFF	64KB
COMPUTE_CLUSTER0_APBADDR_PMU_CPU1	0x0730120000	0x073012FFFF	64KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
COMPUTE_CLUSTER0_APBADDR_ETM_CPU1	0x0730130000	0x073013FFFF	64KB
COMPUTE_CLUSTER0_APBADDR_CTI_CPU1	0x0730140000	0x073014FFFF	64KB
DEBUGSS0_DEBUG_CELL_ROM_SLV	0x073C020000	0x073C020FFF	4KB
DEBUGSS0_CTSET2_WRAP_CFG_CTSET2_CFG	0x073C022000	0x073C023FFF	8KB
DEBUGSS0_ATB_REPLICATOR_CFG_CXATBREPLICATOR_CFG	0x073C024000	0x073C024FFF	4KB
DEBUGSS0_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG	0x073C025000	0x073C025FFF	4KB
DEBUGSS0_CSCTI	0x073C026000	0x073C026FFF	4KB
DEBUGSS0_CSCTI	0x073C028000	0x073C028FFF	4KB
DEBUGSS0_CSCTI	0x073C029000	0x073C029FFF	4KB
DEBUGSS0_CSCTI	0x073C02A000	0x073C02AFFF	4KB
DEBUGSS0_CSCTI	0x073C02B000	0x073C02BFFF	4KB
DEBUGSS0_CSCTI	0x073C02C000	0x073C02CFFF	4KB
DEBUGSS0_CSCTI	0x073C02D000	0x073C02DFFF	4KB
DEBUGSS0_CSCTI	0x073C02E000	0x073C02EFFF	4KB
DEBUGSS0_CSCTI	0x073C02F000	0x073C02FFFF	4KB
STM0_CSSTM	0x073D200000	0x073D200FFF	4KB
STM0_CTI_CSCTI	0x073D201000	0x073D201FFF	4KB
DBGSUSPENDROUTER0_INTR_ROUTER_CFG	0x073D300000	0x073D3007FF	2KB
CPT2_AGGR0_MMR_SLV	0x073E100000	0x073E1000FF	256B
CPT2_AGGR0_VBUSP2APB_WRAP_STP2ATB_VBUS_CFG	0x073E100100	0x073E1001FF	256B
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM0	0x073E120000	0x073E120FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM1	0x073E121000	0x073E121FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM2	0x073E122000	0x073E122FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM3	0x073E123000	0x073E123FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM4	0x073E124000	0x073E124FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM5	0x073E125000	0x073E125FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM6	0x073E126000	0x073E126FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM7	0x073E127000	0x073E127FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM8	0x073E128000	0x073E128FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM9	0x073E129000	0x073E129FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM10	0x073E12A000	0x073E12AFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM11	0x073E12B000	0x073E12BFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM12	0x073E12C000	0x073E12CFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM13	0x073E12D000	0x073E12DFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM14	0x073E12E000	0x073E12EFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM15	0x073E12F000	0x073E12FFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM16	0x073E130000	0x073E130FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM17	0x073E131000	0x073E131FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM18	0x073E132000	0x073E132FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM19	0x073E133000	0x073E133FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM20	0x073E134000	0x073E134FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM21	0x073E135000	0x073E135FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM22	0x073E136000	0x073E136FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM23	0x073E137000	0x073E137FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM24	0x073E138000	0x073E138FFF	4KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM25	0x073E139000	0x073E139FFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM26	0x073E13A000	0x073E13AFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM27	0x073E13B000	0x073E13BFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM28	0x073E13C000	0x073E13CFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM29	0x073E13D000	0x073E13DFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM30	0x073E13E000	0x073E13EFFF	4KB
CPT2_AGGR0_CONT_READ_TRC_SRC_VBUS_MEM31	0x073E13F000	0x073E13FFFF	4KB
DEBUGSS_WRAP0_ROM_TABLE_0_1	0x0740000000	0x0740000FFF	4KB
DEBUGSS_WRAP0_RESV0_1	0x0740001000	0x0740001FFF	4KB
DEBUGSS_WRAP0_CFGAP_CFG_1	0x0740002000	0x07400020FF	256B
DEBUGSS_WRAP0_APBAP_CFG_1	0x0740002100	0x07400021FF	256B
DEBUGSS_WRAP0_AXIAP_CFG_1	0x0740002200	0x07400022FF	256B
DEBUGSS_WRAP0_PWRAP_CFG_1	0x0740002300	0x07400023FF	256B
DEBUGSS_WRAP0_PVIEW_CFG_1	0x0740002400	0x07400024FF	256B
DEBUGSS_WRAP0_JTAGAP_CFG_1	0x0740002500	0x07400025FF	256B
DEBUGSS_WRAP0_SECAP_CFG_1	0x0740002600	0x07400026FF	256B
DEBUGSS_WRAP0_CORTEX0_CFG_1	0x0740002700	0x07400027FF	256B
DEBUGSS_WRAP0_CORTEX1_CFG_1	0x0740002800	0x07400028FF	256B
DEBUGSS_WRAP0_CORTEX2_CFG_1	0x0740002900	0x07400029FF	256B
DEBUGSS_WRAP0_CORTEX3_CFG_1	0x0740002A00	0x0740002AFF	256B
DEBUGSS_WRAP0_CORTEX4_CFG_1	0x0740002B00	0x0740002BFF	256B
DEBUGSS_WRAP0_CORTEX5_CFG_1	0x0740002C00	0x0740002CFF	256B
DEBUGSS_WRAP0_CORTEX6_CFG_1	0x0740002D00	0x0740002DFF	256B
DEBUGSS_WRAP0_CORTEX7_CFG_1	0x0740002E00	0x0740002EFF	256B
DEBUGSS_WRAP0_CORTEX8_CFG_1	0x0740002F00	0x0740002FFF	256B
DEBUGSS_WRAP0_RESV1_1	0x0740003000	0x0740003FFF	4KB
DEBUGSS_WRAP0_RESV2_1	0x0740004000	0x0742003FFF	32MB
DEBUGSS_WRAP0_ROM_TABLE_1_1	0x0760000000	0x0760000FFF	4KB
DEBUGSS_WRAP0_CSCTI	0x0760001000	0x0760001FFF	4KB
DEBUGSS_WRAP0_DRM_CFG_1	0x0760002000	0x0760002FFF	4KB
DEBUGSS_WRAP0_RESV3_1	0x0760003000	0x0760003FFF	4KB
DEBUGSS_WRAP0_CSTPIU_CFG_1	0x0760004000	0x0760004FFF	4KB
DEBUGSS_WRAP0_CTF_CFG_1	0x0760005000	0x0760005FFF	4KB
DEBUGSS_WRAP0_RESV4_1	0x0760006000	0x0761005FFF	16MB
DEBUGSS_WRAP0_EXT_APB_1	0x0770000000	0x077FFFFFFF	256MB

(1) The SOC Memory region for external accesses to the R5F ATCM and BTCM memories are not accessible via the R5F AXI bus initiator. However, the R5F has direct access to ATCM and BTCM as tightly coupled memories and the R5F can also map the base address of the ATCM and BTCM to be the same as the SOC Memory Region Address if desired.

2.2 MCU_M4FSS0 Memory Map

Table 2-2. MCU_M4FSS0 Memory Map

Region Name	Start Address	End Address	Size
MCU_M4FSS0_RAM0	0x0000000000	0x000002FFFF	192KB
MCU_M4FSS0_DRAM	0x0000030000	0x000003FFFF	64KB

Table 2-2. MCU_M4FSS0 Memory Map (continued)

Region Name	Start Address	End Address	Size
MCU_M4FSS0_RAT_CFG	0x0044200000	0x0044200FFF	4KB
MCU_M4FSS0_ECC_AGGR	0x0044201000	0x00442013FF	1KB
MCU_M4FSS0_RAT_REGION0	0x0060000000	0x00DFFFFFFF	2GB
MCU_M4FSS0_ITM	0x00E0000000	0x00E0000FFF	4KB
MCU_M4FSS0_DWT	0x00E0001000	0x00E0001FFF	4KB
MCU_M4FSS0_FBP	0x00E0002000	0x00E0002FFF	4KB
MCU_M4FSS0_NVIC	0x00E000E000	0x00E000EFFF	4KB
MCU_M4FSS0_MPU	0x00E000ED90	0x00E000EDEF	96B
MCU_M4FSS0_ETM	0x00E0041000	0x00E0041FFF	4KB
MCU_M4FSS0_CSCTI	0x00E0042000	0x00E0042FFF	4KB
MCU_M4FSS0_REVID	0x00E0043000	0x00E0043003	4B
MCU_M4FSS0_ROMTABLE	0x00E00FF000	0x00E00FFFFF	4KB

2.3 R5FSS0 Memory Map

Table 2-3. R5FSS0 Memory Map

Region Name	Start Address	End Address	Size
R5FSS0_ATCM(1)	0x0000000000	0x000000FFFF	64KB
R5FSS0_RAT_REGION0	0x0000010000	0x001FFFFFFF	512MB
R5FSS0_NON_RAT_SOC_REGION0	0x0020000000	0x002FFFFFFF	256MB
R5FSS0_RAT_CFG	0x002FFE0000	0x002FFE0FFF	4KB
R5FSS0_VIC_CFG	0x002FFF0000	0x002FFF3FFF	16KB
R5FSS0_RAT_SOC_REGION1	0x0030000000	0x004100FFFF	272MB
R5FSS0_BTCM(1)	0x0041010000	0x004101FFFF	64KB
R5FSS0_RAT_REGION2	0x0041018000	0x007FFFFFFF	1008MB
R5FSS0_RAT_REGION3	0x0080000000	0x00FFFFFFFF	2GB

(1) The SOC Memory region for external accesses to the R5F ATCM and BTCM memories are not accessible via the R5F AXI bus initiator. However, the R5F has direct access to ATCM and BTCM as tightly coupled memories and the R5F can also map the base address of the ATCM and BTCM to be the same as the SOC Memory Region Address if desired.

2.4 R5FSS1 Memory Map

Table 2-4. R5FSS1 Memory Map

Region Name	Start Address	End Address	Size
R5FSS1_ATCM(1)	0x0000000000	0x000000FFFF	64KB
R5FSS1_RAT_REGION0	0x0000010000	0x001FFFFFFF	512MB
R5FSS1_NON_RAT_SOC_REGION0	0x0020000000	0x002FFFFFFF	256MB
R5FSS1_RAT_CFG	0x002FFE0000	0x002FFE0FFF	4KB
R5FSS1_VIC_CFG	0x002FFF0000	0x002FFF3FFF	16KB
R5FSS1_RAT_SOC_REGION1	0x0030000000	0x004100FFFF	272MB
R5FSS1_BTCM(1)	0x0041010000	0x004101FFFF	64KB
R5FSS1_RAT_REGION2	0x0041018000	0x007FFFFFFF	1008MB

Table 2-4. R5FSS1 Memory Map (continued)

Region Name	Start Address	End Address	Size
R5FSS1_RAT_REGION3	0x0080000000	0x00FFFFFFFF	2GB

(1) The SOC Memory region for external accesses to the R5F ATCM and BTCM memories are not accessible via the R5F AXI bus initiator. However, the R5F has direct access to ATCM and BTCM as tightly coupled memories and the R5F can also map the base address of the ATCM and BTCM to be the same as the SOC Memory Region Address if desired.

2.5 PRU_ICSSG0 Memory Map

Table 2-5. PRU_ICSSG0 Memory Map

Region Name	Start Address	End Address	Size
PRU_ICSSG0_DRAM0_SLV_RAM	0x0000000000	0x0000001FFF	8KB
PRU_ICSSG0_DRAM1_SLV_RAM	0x0000002000	0x0000003FFF	8KB
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_RAM	0x0000004000	0x0000005FFF	8KB
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_RAM	0x0000006000	0x0000007FFF	8KB
PRU_ICSSG0_RAT_SLICE0_CFG	0x0000008000	0x0000008FFF	4KB
PRU_ICSSG0_RAT_SLICE1_CFG	0x0000009000	0x0000009FFF	4KB
PRU_ICSSG0_PR1_PDSP_TX0_IRAM_RAM	0x000000A000	0x000000BFFF	8KB
PRU_ICSSG0_PR1_PDSP_TX1_IRAM_RAM	0x000000C000	0x000000DFFF	8KB
PRU_ICSSG0_RAM_SLV_RAM	0x0000010000	0x000001FFFF	64KB
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0x0000020000	0x0000021FFF	8KB
PRU_ICSSG0_PR1_PDSP0_IRAM	0x0000022000	0x00000220FF	256B
PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG	0x0000022400	0x00000224FF	256B
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0x0000023000	0x00000230FF	256B
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0x0000023400	0x00000234FF	256B
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0x0000023800	0x00000238FF	256B
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0x0000023C00	0x0000023CFF	256B
PRU_ICSSG0_PR1_PDSP1_IRAM	0x0000024000	0x00000240FF	256B
PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG	0x0000024400	0x00000244FF	256B
PRU_ICSSG0_PR1_PROT_SLV	0x0000024C00	0x0000024CFF	256B
PRU_ICSSG0_PR1_PDSP_TX0_IRAM	0x0000025000	0x00000250FF	256B
PRU_ICSSG0_PR1_PDSP_TX0_IRAM_DEBUG	0x0000025400	0x00000254FF	256B
PRU_ICSSG0_PR1_PDSP_TX1_IRAM	0x0000025800	0x00000258FF	256B
PRU_ICSSG0_PR1_PDSP_TX1_IRAM_DEBUG	0x0000025C00	0x0000025CFF	256B
PRU_ICSSG0_PR1_CFG_SLV	0x0000026000	0x00000261FF	512B
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_QSTAT	0x0000027000	0x00000277FF	2KB
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0x0000028000	0x000002803F	64B
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0x000002A000	0x000002A0FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0x000002A100	0x000002A1FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0x000002A200	0x000002A2FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0x000002A300	0x000002A3FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	0x000002A400	0x000002A4FF	256B
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	0x000002A500	0x000002A5FF	256B
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_CSTAT	0x000002C000	0x000002C7FF	2KB
PRU_ICSSG0_IEP0	0x000002E000	0x000002EFFF	4KB
PRU_ICSSG0_IEP1	0x000002F000	0x000002FFFF	4KB
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0x0000030000	0x00000300FF	256B

Table 2-5. PRU_ICSSG0 Memory Map (continued)

Region Name	Start Address	End Address	Size
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0x0000032000	0x00000320FF	256B
PRU_ICSSG0_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0x0000032100	0x00000321FF	256B
PRU_ICSSG0_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0x0000032200	0x00000322FF	256B
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0x0000032400	0x00000324FF	256B
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0x0000033000	0x0000033FFF	4KB
PRU_ICSSG0_PR1_PDSP0_IRAM_RAM	0x0000034000	0x0000037FFF	16KB
PRU_ICSSG0_PR1_PDSP1_IRAM_RAM	0x0000038000	0x000003BFFF	16KB
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	0x000003C000	0x000003C0FF	256B
PRU_ICSSG0_RAT_REGION0	0x0000040000	0x00FFFFFFFF	4GB

2.6 PRU_ICSSG1 Memory Map

Table 2-6. PRU_ICSSG1 Memory Map

Region Name	Start Address	End Address	Size
PRU_ICSSG1_DRAM0_SLV_RAM	0x0000000000	0x0000001FFF	8KB
PRU_ICSSG1_DRAM1_SLV_RAM	0x0000002000	0x0000003FFF	8KB
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_RAM	0x0000004000	0x0000005FFF	8KB
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_RAM	0x0000006000	0x0000007FFF	8KB
PRU_ICSSG1_RAT_SLICE0_CFG	0x0000008000	0x0000008FFF	4KB
PRU_ICSSG1_RAT_SLICE1_CFG	0x0000009000	0x0000009FFF	4KB
PRU_ICSSG1_PR1_PDSP_TX0_IRAM_RAM	0x000000A000	0x000000BFFF	8KB
PRU_ICSSG1_PR1_PDSP_TX1_IRAM_RAM	0x000000C000	0x000000DFFF	8KB
PRU_ICSSG1_RAM_SLV_RAM	0x0000010000	0x000001FFFF	64KB
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0x0000020000	0x0000021FFF	8KB
PRU_ICSSG1_PR1_PDSP0_IRAM	0x0000022000	0x00000220FF	256B
PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG	0x0000022400	0x00000224FF	256B
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0x0000023000	0x00000230FF	256B
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0x0000023400	0x00000234FF	256B
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0x0000023800	0x00000238FF	256B
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0x0000023C00	0x0000023CFF	256B
PRU_ICSSG1_PR1_PDSP1_IRAM	0x0000024000	0x00000240FF	256B
PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG	0x0000024400	0x00000244FF	256B
PRU_ICSSG1_PR1_PROT_SLV	0x0000024C00	0x0000024CFF	256B
PRU_ICSSG1_PR1_PDSP_TX0_IRAM	0x0000025000	0x00000250FF	256B
PRU_ICSSG1_PR1_PDSP_TX0_IRAM_DEBUG	0x0000025400	0x00000254FF	256B
PRU_ICSSG1_PR1_PDSP_TX1_IRAM	0x0000025800	0x00000258FF	256B
PRU_ICSSG1_PR1_PDSP_TX1_IRAM_DEBUG	0x0000025C00	0x0000025CFF	256B
PRU_ICSSG1_PR1_CFG_SLV	0x0000026000	0x00000261FF	512B
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_QSTAT	0x0000027000	0x00000277FF	2KB
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0x0000028000	0x000002803F	64B
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0x000002A000	0x000002A0FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0x000002A100	0x000002A1FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0x000002A200	0x000002A2FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0x000002A300	0x000002A3FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	0x000002A400	0x000002A4FF	256B
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	0x000002A500	0x000002A5FF	256B

Table 2-6. PRU_ICSSG1 Memory Map (continued)

Region Name	Start Address	End Address	Size
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_CSTAT	0x000002C000	0x000002C7FF	2KB
PRU_ICSSG1_IEP0	0x000002E000	0x000002EFFF	4KB
PRU_ICSSG1_IEP1	0x000002F000	0x000002FFFF	4KB
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0x0000030000	0x00000300FF	256B
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0x0000032000	0x00000320FF	256B
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0x0000032100	0x00000321FF	256B
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0x0000032200	0x00000322FF	256B
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0x0000032400	0x00000324FF	256B
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0x0000033000	0x0000033FFF	4KB
PRU_ICSSG1_PR1_PDSP0_IRAM_RAM	0x0000034000	0x0000037FFF	16KB
PRU_ICSSG1_PR1_PDSP1_IRAM_RAM	0x0000038000	0x000003BFFF	16KB
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	0x000003C000	0x000003C0FF	256B
PRU_ICSSG1_RAT_REGION0	0x0000040000	0x00FFFFFFFF	4GB

2.7 MCU_M4FSS0 Memory Map

Table 2-7. MCU_M4FSS0 Memory Map

Region Name	Start Address	End Address	Size
MCU_M4FSS0_RAM0	0x0000000000	0x000002FFFF	192KB
MCU_M4FSS0_DRAM	0x0000030000	0x000003FFFF	64KB
MCU_M4FSS0_RAT_CFG	0x0044200000	0x0044200FFF	4KB
MCU_M4FSS0_ECC_AGGR	0x0044201000	0x00442013FF	1KB
MCU_M4FSS0_RAT_REGION0	0x0060000000	0x00DFFFFFFF	2GB
MCU_M4FSS0_ITM	0x00E0000000	0x00E0000FFF	4KB
MCU_M4FSS0_DWT	0x00E0001000	0x00E0001FFF	4KB
MCU_M4FSS0_FBP	0x00E0002000	0x00E0002FFF	4KB
MCU_M4FSS0_NVIC	0x00E000E000	0x00E000EFFF	4KB
MCU_M4FSS0_MPU	0x00E000ED90	0x00E000EDEF	96B
MCU_M4FSS0_ETM	0x00E0041000	0x00E0041FFF	4KB
MCU_M4FSS0_CSCTI	0x00E0042000	0x00E0042FFF	4KB
MCU_M4FSS0_REVID	0x00E0043000	0x00E0043003	4B
MCU_M4FSS0_ROMTABLE	0x00E00FF000	0x00E00FFFFF	4KB

2.8 DMSC0 Memory Map

Table 2-8. DMSC0 Memory Map

Region Name	Start Address	End Address	Size
DMSC0_IROM__SLV__ROM	0x0000000000	0x000001FFFF	128KB
DMSC0_DMSC_SRAM0	0x0000040000	0x000004FFFF	64KB
DMSC0_DMSC_SRAM1	0x0000050000	0x000005FFFF	64KB
DMSC0_DMSC_PWR_MMR	0x0044130000	0x0044131FFF	8KB
DMSC0_DMSC_DMTIMER0	0x0044133000	0x00441333FF	1KB
DMSC0_DMSC_DMTIMER1	0x0044134000	0x00441343FF	1KB
DMSC0_DMSC_WDT_RTI	0x0044135000	0x00441350FF	256B
DMSC0_DMSC_RTI_MMR	0x0044135100	0x00441351FF	256B
DMSC0_DMSC_RAT_MMRS	0x0044200000	0x0044200FFF	4KB
DMSC0_DMSC_ECC_REGS	0x0044202000	0x00442023FF	1KB

Table 2-8. DMSC0 Memory Map (continued)

Region Name	Start Address	End Address	Size
DMSC0_DMSC_SEC_MMR	0x0044230000	0x0044230FFF	4KB
DMSC0_DMSC_DBGAUTH_REG	0x0044232000	0x0044232FFF	4KB
DMSC0_DMSC_SECMGR	0x0044234000	0x0044237FFF	16KB
DMSC0_DMSC_DMTIMER2	0x0044238000	0x00442383FF	1KB
DMSC0_DMSC_DMTIMER3	0x0044239000	0x00442393FF	1KB
DMSC0_DMSC_AES38T	0x004423C000	0x004423DFFF	8KB
DMSC0_DMSC_IA_INTR	0x0044300000	0x004437FFFF	512KB
DMSC0_DMSC_IA_IMAP	0x0044400000	0x00444007FF	2KB
DMSC0_DMSC_IA_CFG	0x0044410000	0x004441001F	32B
DMSC0_DMSC_FW_VBUS_CFG	0x0045000000	0x0045FFFFFF	16MB
DMSC0_EXT_MEM_REGION	0x0060000000	0x00DFFFFFFF	2GB
DMSC0_ITM	0x00E0000000	0x00E0000FFF	4KB
DMSC0_DWT	0x00E0001000	0x00E0001FFF	4KB
DMSC0_FBP	0x00E0002000	0x00E0002FFF	4KB
DMSC0_NVIC	0x00E000E000	0x00E000E4EF	1KB
DMSC0_SCS	0x00E000E000	0x00E000EFFF	4KB
DMSC0_CTI	0x00E0042000	0x00E0042FFF	4KB
DMSC0_ROM_TABLE	0x00E00FF000	0x00E00FFFFF	4KB

2.9 Region-based Address Translation

The SoC memory map view shown in *Memory Map* is used by A53SS0_CORE0 and A53SS0_CORE1 but there are processors which support only 32-bit addressing and cannot access higher address ranges. For these processors RAT modules are integrated to remap the 32-bit addresses to 48-bit addresses allowing higher address range accesses. The "RAT_REGION" regions shown in *R5FSS0/1 Memory Map* through *MCU_M4FSS) Memory Map* are dedicated to RAT remapping.

For more information about the RAT module, see *Region-based Address Translation (RAT) Module*.

Chapter 3

System Interconnect

This chapter describes the device system interconnect.

System interconnect provides a multi-layered crossbar network among initiators and targets within SoC. This mutli-layered crossbar network supports multiple in-flight transactions to improve both latency and throughput

3.1 Terminology

- **CBASS**: Crossbar module to provide physical connections among the initiators and targets
- **VBUSP Interface**: Single-issue interface
- **VBUSM Interface**: Multi-issue interface
- **Channel ID:** Channel ID for an interface indicates a logical flow. All transactions with the same channel ID and initiator are consider an orthogonal and independent flow.
- **Order ID**: 4 bit value associated with each transaction. All transactions with the same initiator, target end point, and Order ID are executed in order. Order ID is also to be used to select real-time and non-real time path for the transaction. Order ID 8-15 is reserved for real-time path.
- **ASEL:** Address Selection is an attribute associated with each transaction. ASEL can be either used to select a unique memory map or be used to indicate IO coherent transactions.
- **PrivID**: PrivID is an attribute associated with each transaction. The privID value indicates the security access group. PrivID is either assigned by the ISC block or DMA configuration.
- **Priv:**Priv is a transaction attribute to determine whether the transaction has supervisor privilege. Priv =1 indicates supervisor privilege. Priv=0 indicates user privilege.
- **Secure**: this is a single bit control signal carried with each transaction. If it is set to 1b1, it means this is a secure transaction. If it is set to 1b0, then it is a non-secure transaction.
- **ISC**: Initiator Security Control. ISC can add or overwrite the transaction attributes such as PrivID, Priv and Secure.
- **Region Based Firewall**: Firewall block based on address region. The minimal region granularity is 4KB. User can configure each the protection region and its access privilege.
- **Channelized firewall**: provide protection for a predefined region size, the predefined region size can be as small as 4B.
- **QoS**: Quality of Service allows user to add additional sideband signals to the transaction to fine tune system level performance.

3.2 System Interconnect Overview

The SoC is divided into two domains: MCU Domain and MAIN Domain. Inside each domain resides multiple CBASS crossbar IPs to provide connectivity among initiators and targets.

The MAIN Domain contains the following CBASS IPs:

- CBASS0
- CBASS_INFRA1
- CBASS_FW0
- CBASS_DBG0

The MCU Domain contains the following CBASS IP:

- MCU_CBASS0

CBASS_FW0 is dedicated to route the firewall, QoS Block and ISC Block configurations. CBASS_DBG0 is dedicated to route all debug configuration related transactions.

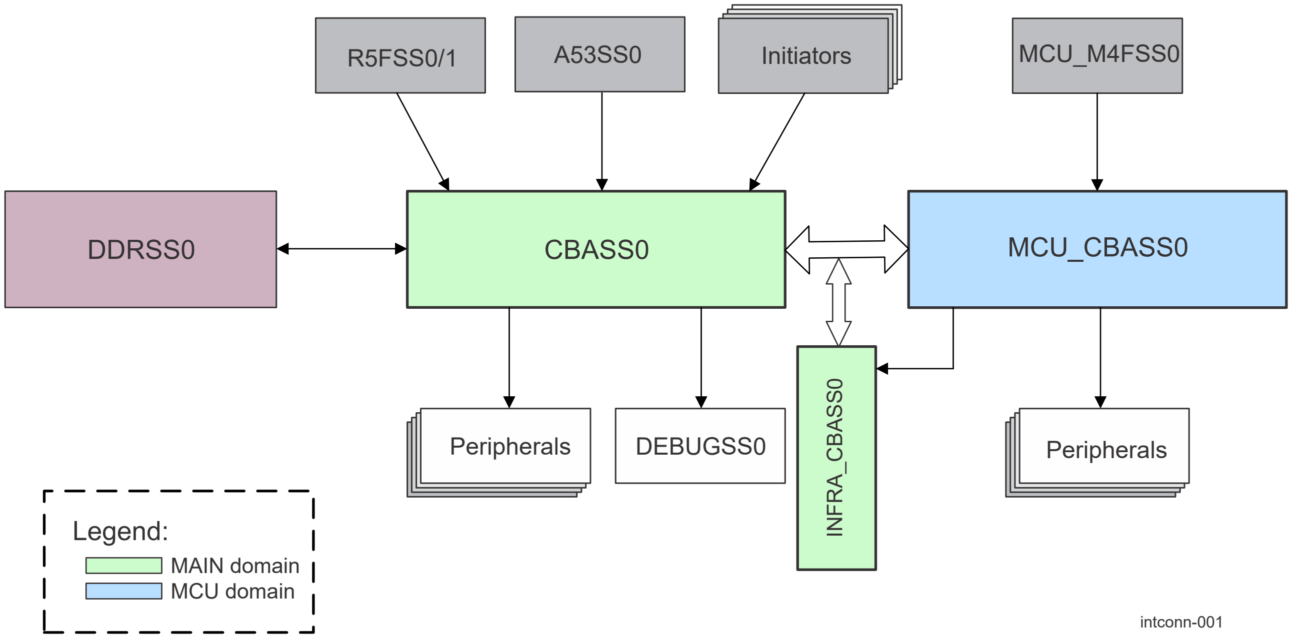

Figure 3-1. Device System Interconnect Overview

3.3 Initiator/Target Connectivity

All processors and DMA have the physical path to read from and write to any memory mapped end points listed in the SoC memory map.

The configuration of the crypto DMSS is only accessible by TIFS M4F core, and is not included in the SoC level memory map.

3.4 Interrupt Condition for Interconnect

Each CBASS crossbar IP may generate up to two interrupts:

- default_err_intr: the intent of this interrupt is for debug purposes. Any illegal transactions will trigger this interrupt and the illegal transaction information is logged by CBASS IP.
- default_exp: this interrupt is asserted whenever there is a firewall violation. Only the CBASS IP contains firewall module that can generate this interrupt.

The illegal transactions triggering default_err_intr can be caused by multiple reasons:

- The transaction is sent to a memory region not implemented in CBASS
- The target interface or target peripheral is in disabled state

When CBASS detects an illegal transaction, it terminates the transaction gracefully to avoid a system hang. In addition, the CBASS sends return status back to the initiator with error status. If this illegal transaction is a read transaction, the read data is returned with all zeros. If this illegal transaction is a write transaction, this write transaction is terminated and returns a write error back to initiator. The interrupt and illegal transaction logging can be found in the CBASS's err_regs region.

For any transaction blocked by the firewall, the transaction is terminated gracefully and the initiator will receive error status for the blocked transaction. If this blocked transaction is read, the read data is returned with all zeros. If this blocked transaction is a write transaction, this write transaction is terminated and returns a write error back to the initiator. The default_exp interrupt and the blocked transaction information can be found in the glb_regs region.

Table 3-1. CBASS Interrupt

CBASS Name	default_err_intr supported	default_exp Interrupt supported
CBASS0	Yes	Yes
MCU_CBASS0	Yes	No
CBASS_INFRA1	Yes	Yes
CBASS_FW0	Yes	No
CBASS_DBG0	Yes	No

3.4.1 Register MMR for default_err_intr

Each CBASS supports default_err_intr containing an err_regs region, which includes the following registers:

Address Offset	Register Mnemonic	Register Name
0x0	PID	Revision Register
0x4	DESTINATION_ID	Destination ID Register
0x24	EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register
0x28	EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register
0x2c	EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register
0x30	EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register
0x34	EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register
0x38	EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register
0x50	ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register
0x54	ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register
0x58	ERR_INTR_ENABLE_SET	Interrupt Enable Set Register
0x5c	ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register
0x60	ERR_EOI	EOI Register

PID (Revision Register) is located at offset 0x0. The following shows the definition of each field of this register.

The Revision Register contains the major and minor revisions for the module.

Bit	Name	Type	Reset	Description
31:30	scheme	r	0x1	PID register scheme
29:28	bu	r	0x2	Business Unit: 10 = Processors
27:16	func	r	0x600	Module ID
15:11	rtl	r	0x6	RTL revision. Will vary depending on release.
10:8	major	r	0x1	Major revision
7:6	custom	r	0x0	Custom
5:0	minor	r	0x2	Minor revision

DESTINATION_ID (Destination ID Register) has offset 0x4.

The Destination ID Register defines the destination ID value for error messages.

Bit	Name	Type	Reset	Description
31:8	reserved	r	0x0	Reserved
7:0	dest_id	rw	0x0	The destination ID.

EXCEPTION_LOGGING_HEADER0 (Exception Logging Header 0 Register), (0x24)

The Exception Logging Header 0 Register contains the first word of the header.

Bit	Name	Type	Reset	Description
31:24	type_f	r	0x0	Type. 7 = CBASS.
23:8	src_id	r	0x0	Source ID. Always 0.
7:0	dest_id	r	0x0	Destination ID.

EXCEPTION_LOGGING_HEADER1 (Exception Logging Header 1 Register) has offset 0x28.

The Exception Logging Header 1 Register contains the second word of the header.

Bit	Name	Type	Reset	Description
31:24	group	r	0x0	Group. Always 0.
23:16	code	r	0x0	Code. 0 = CBASS decode error.
15:0	reserved	r	0x0	Reserved

EXCEPTION_LOGGING_DATA0 (Exception Logging Data 0 Register) has offset 0x2c.

The Exception Logging Data 0 Register contains the first word of the data.

Bit	Name	Type	Reset	Description
31:0	addr_l	r	0x0	Address lower 32 bits.

EXCEPTION_LOGGING_DATA1 (Exception Logging Data 1 Register), (0x30)

The Exception Logging Data 1 Register contains the second word of the data.

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	addr_h	r	0x0	Address upper 16 bits.

EXCEPTION_LOGGING_DATA2 (Exception Logging Data 2 Register has offset 0x34.

The Exception Logging Data 2 Register contains the third word of the data.

Bit	Name	Type	Reset	Description
31:28	reserved	r	0x0	Reserved
27:16	routeid	r	0x0	Route ID.
15:14	reserved	r	0x0	Reserved
13	write	r	0x0	Write.
12	read	r	0x0	Read.
11	debug	r	0x0	Debug.
10	cacheable	r	0x0	Cacheable.
9	priv	r	0x0	Priv.
8	secure	r	0x0	Secure.
7:0	priv_id	r	0x0	Priv ID.

EXCEPTION_LOGGING_DATA3 (Exception Logging Data 3 Register) has offset 0x38.

The Exception Logging Data 3 Register contains the fourth word of the data.

Bit	Name	Type	Reset	Description
31:10	reserved	r	0x0	Reserved
9:0	bytecnt	r	0x0	Byte count.

ERR_INTR_RAW_STAT (Global Interrupt Raw Status Register), (0x50)

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	intr	rw1ts	0x0	Level Interrupt status

ERR_INTR_ENABLED_STAT (Global Interrupt Enabled Status Register), (0x54)

The interrupt status register is gated by the interrupt enable

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	enabled_intr	rw1tc	0x0	Level Enabled Interrupt status

ERR_INTR_ENABLE_SET (Interrupt Enable Set Register), (0x58)

Only when this register is set, null access will cause interrupt to be generated.

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	intr_enable_set	rw1ts	0x0	Interrupt Enable Set Register

ERR_INTR_ENABLE_CLR (Interrupt Enable Clear Register), (0x5c)

Setting this register disables the null interrupt generation

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	intr_enable_clr	rw1tc	0x0	Interrupt Enable Clear Register

ERR_EOI (EOI Register), (0x60)

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	eoi_wr	rw	0x0	End Of Interrupt Register

3.4.2 Register MMR for default_exp

All of the registers for default_exp_intr are located in the glb_regs region of the CBASS which supports this feature. For each glb_reg region, the following registers are supported.

Table 3-2. glb_regs for default_exp_intr

Address Offset	Register Mnemonic	Register Name
0x0	PID	Revision Register
0x4	DESTINATION_ID	Destination ID Register
0x20	EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register
0x24	EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register
0x28	EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register
0x2c	EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register
0x30	EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register

Table 3-2. glb_regs for default_exp_intr (continued)

Address Offset	Register Mnemonic	Register Name
0x34	EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register
0x38	EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register
0x40	EXCEPTION_PEND_SET	Exception Logging Pending Set Register
0x44	EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register

The Revision Register contains the major and minor revisions for the module.

Bit	Name	Type	Reset	Description
31:30	scheme	r	0x1	PID register scheme
29:28	bu	r	0x2	Business Unit: 10 = Processors
27:16	func	r	0x600	Module ID
15:11	rtl	r	0x6	RTL revision. Will vary depending on release.
10:8	major	r	0x1	Major revision
7:6	custom	r	0x0	Custom
5:0	minor	r	0x2	Minor revision

The Destination ID Register defines the destination ID value for error messages.

Bit	Name	Type	Reset	Description
31:8	reserved	r	0x0	Reserved
7:0	dest_id	rw	0x0	The destination ID.

The Exception Logging Control Register controls the exception logging.

Bit	Name	Type	Reset	Description
31:2	reserved	r	0x0	Reserved
1	disable_pend	rw	0x0	Disables logging pending when set.
0	disable_f	rw	0x0	Disables logging when set.

The Exception Logging Header 0 Register contains the first word of the header.

Bit	Name	Type	Reset	Description
31:24	type_f	r	0x0	Type.
23:8	src_id	r	0x0	Source ID.
7:0	dest_id	r	0x0	Destination ID.

The Exception Logging Header 1 Register contains the second word of the header.

Bit	Name	Type	Reset	Description
31:24	group	r	0x0	Group.
23:16	code	r	0x0	Code.
15:0	reserved	r	0x0	Reserved

The Exception Logging Data 0 Register contains the first word of the data.

Bit	Name	Type	Reset	Description
31:0	addr_l	r	0x0	Address lower 32 bits.

The Exception Logging Data 1 Register contains the second word of the data.

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	addr_h	r	0x0	Address upper 16 bits.

The Exception Logging Data 2 Register contains the third word of the data.

Bit	Name	Type	Reset	Description
31:28	reserved	r	0x0	Reserved
27:16	routeid	r	0x0	Route ID.
15:14	reserved	r	0x0	Reserved
13	write	r	0x0	Write.
12	read	r	0x0	Read.
11	debug	r	0x0	Debug.
10	cacheable	r	0x0	Cacheable.
9	priv	r	0x0	Priv.
8	secure	r	0x0	Secure.
7:0	priv_id	r	0x0	Priv ID.

The Exception Logging Data 3 Register contains the fourth word of the data.

Bit	Name	Type	Reset	Description
31:10	reserved	r	0x0	Reserved
9:0	bytecnt	r	0x0	Byte count.

The Exception Logging Pending Set Register allows to set the pend signal.

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	pend_set	rw1ts	0x0	Write a 1 to set the exception pend signal.

The Exception Logging Pending Clear Register allows to clear the pend signal.

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	pend_clr	rw1tc	0x0	Write a 1 to clear the exception pend signal.

3.5 IO Coherency Support

The SoC has limited IO Coherency support through the ACP interface of the MPU Cluster. Sending transactions to the ACP interface allows those transactions, outside of the MPU cluster, to directly go through the shared L2 cache controller. There are two types of cache operations supported through ACP: write allocation and write through. Read through ACP interface has no impact on the cache operation. The main function of the ACP interface is to allow write transactions from the SoC side to push data directly into the MPU's L2 cache. Therefore, the MPU can access this data much faster from the L2 cache rather than fetching it from system memory, while still maintaining the cache coherency.

Not all initiators have the capability to send transactions to ACP interface for IO coherency. This feature is limited to a subset of the initiators such as BCDMA, pktDMA, and some high-speed peripherals such as USB and EMMC. The transactions sent to the ACP interface must have the ASEL value set to either 14 or 15.

- Write transactions with ASEL=14 cause MPU L2 cache allocation: for cache warming feature
- Write transactions with ASEL=15 do not cause MPU A53SS L2 cache allocation
- Read transactions with ASEL=14 and 15 do not cause L2 cache allocation
  - All the transactions to ACP port can be protected by firewall if firewall is inserted by the SoC level interconnect

By default, all transactions have ASEL set to zero. For any transactions from pktDMA and BCDMA, the ASEL can be set as part of the DMA configuration. For all other transactions, the ASEL value can be set through QoS MMR. For more details, see Quality of Service (QoS) Block.

Not all initiators have a connection to the ACP interface. MPU A53SS, DebugSS and Security Manager do not have access to ACP interfaces even with the ASEL value set to 14 or 15.

3.6 Quality of Service (QoS) Block

CBASS arbitrates the transaction based on priority from high to low. If the transactions going to the same end point have the same priority, then the CBASS uses round robin method for these transactions.

In the CBASS with parallel paths, orderID is used to determine how the transactions are forwarded to those parallel paths. The parallel paths are defined as two target interfaces with the exact same memory map assignment.

By default, all the target interfaces have a certain address assigned and CBASS routes the transactions based on this address. However, some of the special target interfaces can be routed through a different mechanism using the ASEL signal, such as MPU A53SS's ACP interface and PCIe target interfaces.

By default, the majority of the transactions default to the lowest priority level, ASEL value to zero and orderID to zero. The transactions from BCDMA and pktDMA have those attributes as part of the DMA configuration. ASEL value is part of the address information passed to the DMA engine. It is normally specified in descriptors such as host packet descriptor and host buffer descriptor for pktDMA, and Transfer Request (TR) packet descriptor for BCDMA. The priority and orderID information can be configured through each DMA channel's priority control register.

For the rest of the initiators, the CBASS IP provides QoS block to allow the user to program the transaction's attributes such as priority level, ASEL coding and orderID.

The QoS block programming is through CBASS's qos_regs region. Each initiator, except the BCDMA, pktDMA, and debugss, has an MMR to allow the user to set the priority, ASEL, and orderID value. There is another exception on priority setting. The display IP implements dynamic priority schedule based on the FIFO threshold. The QoS block inside CBASS does not have the ability to overwrite the priority value coming from the display IP.

Section 3.6.2 shows the mapping between initiators and QoS block physical addresses.

Each QoS block has one 4B MAP register per channel that allows the user to program ASEL, orderID, and priority. The first MAP register is at offset 0x100 and the MAP register for channel X is located at offset 0x100+400x. See Section 3.6.1 .

For any write to address range 0x4500_0000 to 0x45FF_FFFF, it is recommended to read back the value after the write to make sure the write landed. The registers in this regions are mainly for firewall configuration, ISC/DMA credential configuration, QoS MMR configuration.

On QoS MMR configuration, in order to configure certain transaction to be the highest priority, the priority field needs to be set to zero for that transaction. In order to make sure that priority field is indeed to set to zero, the following sequence should be followed:

1. Read the priority field, if it is non-zero value, follow a write to overwrite priority field to be 0x0.

2. If read back priority field is zero, write to QoS MMR register to set priority field to be 0x7. Read back the same priority field. If the read back value is 0x7, write to QoS MMR register to set priority field to be 0x0. If the read back value is 0x0, it means this register is not implemented and priority setting is not working.

3.6.1 QoS Block MMR

Each QoS block has one 4B MAP register per channel. It defines ASEL, orderID and priority field user can program. The first MAP register is at offset 0x100 and the MAP register for channel X is located at offset 0x100+4*x.

Bit	Name	Type	Reset	Description
31:30	reserved	r	0x0	Reserved
29:28	atype	rw	0x0	atype signal for channel N. 0 = physical. 1 = intermediate. 2 = virtual. 3 = physical with coherence. Keep it as default value. Do not program it to different value.
27:16	virtid	rw	0x0	virtid signal for channel N. Shall be 0x0.
15	reserved	r	0x0	Reserved
14:12	epriority	rw	0x7	epriority signal for channel N. 0x7 is the lowest priority, 0x0 is the highest priority.
11:8	asel	rw	0x0	ASEL signal for channel N. Default to zero. Set to either 0xE or 0xF for IO coherency transactions.
7:4	orderid	rw	0x0	orderid signal for channel N. Default to zero and keep it to 0x0.
3	reserved	r	0x0	Reserved
2:0	qos	rw	0x0	qos signal for channel N. Not used. No impacted if it is programed to different value.

3.6.2 QoS Summary Table

Table 3-3. QoS Summary Table

Initiator	QoS Index	Channel Count	Virtual ID Capable	Order ID Capable	Transaction Priority Capable	Address Type Capable	Asel Capable	QoS Block Physical Address
R5FSS0_CPU0_PMST	128	1	N	Y	Y	N	Y	0x45D20000
R5FSS0_CPU1_PMST	129	1	N	Y	Y	N	Y	0x45D20400
R5FSS1_CPU0_PMST	130	1	N	Y	Y	N	Y	0x45D20800
R5FSS1_CPU1_PMST	131	1	N	Y	Y	N	Y	0x45D20C00
MCU_M4FSS0_VBUSP_M	192	1	N	N	Y	N	Y	0x45D30000
DMASS0_SEC_PROXY_0_DST	256	1	N	N	Y	Y	N	0x45D40000
DMASS0_RINGACC_0_DST	257	1	N	N	N	N	N	0x45D40400
COMPUTE_CLUSTER0_A53_DUAL_WRAP_CBA_AXI_R	513	1	N	Y	Y	N	Y	0x45D80400
COMPUTE_CLUSTER0_A53_DUAL_WRAP_CBA_AXI_W	514	1	N	Y	Y	N	Y	0x45D80800
MMCSD0_EMMCSS_WR	516	1	N	Y	Y	N	Y	0x45D81000
MMCSD0_EMMCSS_RD	517	1	N	Y	Y	N	Y	0x45D81400
GICSS0_MEM_WR_VBUSM	520	1	N	Y	Y	N	Y	0x45D82000
GICSS0_MEM_RD_VBUSM	521	1	N	Y	Y	N	Y	0x45D82400
R5FSS0_CPU0_RMST	522	1	N	Y	Y	N	Y	0x45D82800
R5FSS0_CPU0_WMST	523	1	N	Y	Y	N	Y	0x45D82C00
R5FSS0_CPU1_RMST	527	1	N	Y	Y	N	Y	0x45D83C00
R5FSS0_CPU1_WMST	528	1	N	Y	Y	N	Y	0x45D84000
R5FSS1_CPU0_RMST	532	1	N	Y	Y	N	Y	0x45D85000
R5FSS1_CPU0_WMST	533	1	N	Y	Y	N	Y	0x45D85400
R5FSS1_CPU1_RMST	537	1	N	Y	Y	N	Y	0x45D86400
R5FSS1_CPU1_WMST	538	1	N	Y	Y	N	Y	0x45D86800
PRU_ICSSG0_PR1_EXT_VBUSM	542	16	N	Y	Y	N	N	0x45D87800
PRU_ICSSG1_PR1_EXT_VBUSM	543	16	N	Y	Y	N	N	0x45D87C00
PCIE0_PCIE_MST_RD	544	8	N	Y	Y	N	Y	0x45D88000
PCIE0_PCIE_MST_WR	545	8	N	Y	Y	N	Y	0x45D88400
MMCSD1_EMMCSDSS_WR	546	1	N	Y	Y	N	Y	0x45D88800
MMCSD1_EMMCSDSS_RD	547	1	N	Y	Y	N	Y	0x45D88C00
SA2_UL0_CTXCACH_EXT_DMA	548	1	N	Y	Y	N	Y	0x45D89000
USB0_MSTR0	549	8	N	Y	Y	N	Y	0x45D89400
USB0_MSTW0	550	8	N	Y	Y	N	Y	0x45D89800
DEBUGSS_WRAP0_VBUSMR	552	1	N	Y	Y	N	Y	0x45D8A000
DEBUGSS_WRAP0_VBUSMW	553	1	N	Y	Y	N	Y	0x45D8A400

3.7 Route ID

The route ID is used by the interconnect to route return status and data back to the transaction initiator. Each initiator has one or multiple unique route IDs assigned to it. The route ID has no other usage. There are no software controls for the route ID. The initiator-to-route-ID assignment is shown in Section 3.7.1 .

3.7.1 Route ID Table

Table 3-4. Route ID Table

Module Name	Initiator Interface	Which CBASS it is connected to	Route ID	Physical Address
COMPUTE_CLUSTER0	A53_DUAL_WRAP_CBA_AXI_W	CBASS0	0 - 7	0x45D80800
COMPUTE_CLUSTER0	A53_DUAL_WRAP_CBA_AXI_R	CBASS0	16 - 23	0x45D80400
R5FSS0	CPU0_RMST	CBASS0	66	0x45D82800
R5FSS0	CPU0_WMST	CBASS0	67	0x45D82C00
R5FSS0	CPU1_RMST	CBASS0	69	0x45D83C00
R5FSS0	CPU1_WMST	CBASS0	70	0x45D84000
R5FSS1	CPU0_RMST	CBASS0	71	0x45D85000
R5FSS1	CPU0_WMST	CBASS0	72	0x45D85400
R5FSS1	CPU1_RMST	CBASS0	73	0x45D86400
R5FSS1	CPU1_WMST	CBASS0	74	0x45D86800
DMASS0_SEC_PROXY_0	DST	dmss_am64_ipcss_cbass	132	0x45D40000
DMASS0_RINGACC_0	DST	dmss_am64_ipcss_cbass	133	0x45D40400
MMCSD0	EMMCSS_WR	CBASS0	256	0x45D81000
MMCSD0	EMMCSS_RD	CBASS0	257	0x45D81400
DEBUGSS_WRAP0	VBUSMR	CBASS0	258	0x45D8A000
DEBUGSS_WRAP0	VBUSMW	CBASS0	259	0x45D8A400
PCIE0	PCIE_MST_RD	CBASS0	267	0x45D88000
PCIE0	PCIE_MST_WR	CBASS0	268	0x45D88400
MMCSD1	EMMCSDSS_WR	CBASS0	269	0x45D88800
MMCSD1	EMMCSDSS_RD	CBASS0	270	0x45D88C00
SA2_UL0	CTXCACH_EXT_DMA	CBASS0	271	0x45D89000
GICSS0	MEM_WR_VBUSM	CBASS0	302	0x45D82000
GICSS0	MEM_RD_VBUSM	CBASS0	303	0x45D82400
USB0	MSTR0	CBASS0	304	0x45D89400
USB0	MSTW0	CBASS0	305	0x45D89800
PRU_ICSSG0	PR1_EXT_VBUSM	CBASS0	384 - 415	0x45D87800
PRU_ICSSG1	PR1_EXT_VBUSM	CBASS0	416 - 447	0x45D87C00
R5FSS0	CPU0_PMST	CBASS_INFRA1	3000	0x45D20000
R5FSS0	CPU1_PMST	CBASS_INFRA1	3001	0x45D20400
R5FSS1	CPU0_PMST	CBASS_INFRA1	3002	0x45D20800
R5FSS1	CPU1_PMST	CBASS_INFRA1	3003	0x45D20C00
MCU_M4FSS0	VBUSP_M	MCU_CBASS0	4092	0x45D30000

3.8 ISC and Firewall

There are two basic building blocks to achieve security isolation on the SoC level: firewall block and ISC block.

3.8.1 Initiator-Side Security Controls (ISC)

The purpose of the ISC block is to provide a mechanism to either add or overwrite the attributes of the transaction, such as privID, priv, and secure. Each transaction in the system carries those attributes, either driven internally by the IP, or added/modified by the ISC block for that initiator.

All the transactions coming from pktDMA, BCDMA, and DMSS_crypto, the privID, priv, and secure attributes are driven internally by the DMA engine. There is no ISC block to override the values for these transactions. For the transactions from pktDMA, BCDMA, and XLCDMA, the secure, priv, and privID values are determined by the credential register for each DMA flow.

Transactions from all other initiators, attributes can be added or overridden by the ISC block.

The majority of the ISC blocks only contain one region, therefore all the transactions through that ISC block share the same ISC setting. There are a few ISC blocks supporting either multiple channels or multiple regions. The default setting for those ISC blocks with multiple channels, or multiple regions, are the same. However, the transaction attributes can be modified in a finer granularity by utilizing the multiple channel/region mode. If the channel mode is enabled, the starting address and the end address MMRs should be programmed to the starting and end channel number for that ISC region. If the region mode is enabled, the starting and end address MMRs are the address range the transactions are sent to.

Section 3.8.1.1 shows the default setting for privID/priv setting. It is recommended not to change those settings except some specific conditions.

3.8.1.1 ISC and Priv-ID

Table 3-5. ISC and Priv-ID

Default Priv ID	Inititator	ISC Interface	ISC ID	MMR Base Address	Region Count
4	COMPUTE_CLUSTER0	A53_DUAL_WRAP_CBA_AXI_R	513	0x45880400	1
		A53_DUAL_WRAP_CBA_AXI_W	514	0x45880800	1
64	DMASS0_SEC_PROXY_0	DST	256	0x45840000	1
65	DMASS0_RINGACC_0	DST	257	0x45840400	1
100	MCU_M4FSS0	VBUSP_M	192	0x45830000	1
128	MMCSD0	EMMCSS_WR	516	0x45881000	1
		EMMCSS_RD	517	0x45881400	1
129	MMCSD1	EMMCSDSS_WR	546	0x45888800	1
		EMMCSDSS_RD	547	0x45888C00	1
136	PRU_ICSSG0	PR1_EXT_VBUSM	542	0x45887800	16
137	PRU_ICSSG1	PR1_EXT_VBUSM	543	0x45887C00	16
152	SA2_UL0	CTXCACH_EXT_DMA	548	0x45889000	1
154	GICSS0	MEM_WR_VBUSM	520	0x45882000	1
		MEM_RD_VBUSM	521	0x45882400	1
155	USB0	MSTR0	549	0x45889400	8
		MSTW0	550	0x45889800	8
177	DEBUGSS_WRAP0	VBUSMR	552	0x4588A000	1
		VBUSMW	553	0x4588A400	1
179	PCIE0	PCIE_MST_RD	544	0x45888000	8
		PCIE_MST_WR	545	0x45888400	8
202	DMSC0_CBASS_0	IQUASAR_I_MST	32	0x45808000	1
		IQUASAR_D_MST	33	0x45808400	1
		IQUASAR_S_MST	34	0x45808800	1
212	R5FSS0	CPU0_PMST	128	0x45820000	1
		CPU0_RMST	522	0x45882800	1

Table 3-5. ISC and Priv-ID (continued)

Default Priv ID	Inititator	ISC Interface	ISC ID	MMR Base Address	Region Count
		CPU0_WMST	523	0x45882C00	1
213	R5FSS0	CPU1_PMST	129	0x45820400	1
		CPU1_RMST	527	0x45883C00	1
		CPU1_WMST	528	0x45884000	1
214	R5FSS1	CPU0_PMST	130	0x45820800	1
		CPU0_RMST	532	0x45885000	1
		CPU0_WMST	533	0x45885400	1
215	R5FSS1	CPU1_PMST	131	0x45820C00	1
		CPU1_RMST	537	0x45886400	1
		CPU1_WMST	538	0x45886800	1

3.8.1.2 ISC Registers

CBASS ISC Registers are described in Table 3-6.

Each ISC block contains a set of MMRs for each region/channel: Control MMR, start address, and end address. If an ISC block is configured to have x region/channels, this ISC block contains x+1 sets of MMRs.

Table 3-6. ISC Registers

Address Offset	Register Mnemonic	Register Name
(b*0x20), b=0..31	REGION[b]_CONTROL	ISC a Region b Control Register
(b*0x20)+0x10, b=0..31	REGION[b]_START_ADDR_L	ISC a Region b Start Address Low Register
(b*0x20)+0x14, b=0..31	REGION[b]_START_ADDR_H	ISC a Region b Start Address High Register
(b*0x20)+0x18, b=0..31	REGION[b]_END_ADDR_L	ISC a Region b End Address Low Register
(b*0x20)+0x1c, b=0..31	REGION[b]_END_ADDR_H	ISC a Region b End Address High Register

Each ISC can be configured in one of two modes: region mode and channel mode.

When the region mode is configured, the start and end address MMRs shall be programmed with an SoC address range.

When ISC is configured as channel mode, the start and end address MMRs shall be programmed using channel number.

Each region and channel can be configured to determine whether to overwrite or add values for priv, privID, and secure attributes. A default value for the control MMR, located at offset x*0x20, is used so that transactions do not map to a valid region.

The following is the SW sequence to modify the default ISC setting for region/channel b:

- If channel mode is needed, set ch_mode field to 0x1. Program the start and end address MMRs to be the channel ID
- If region mode is needed, set ch_mode field to be 0x0. Program the start and the end address MMRs to match the address range.
- Set enable field to be 0xA
- If lock field is set to 0x1, then this control MMR can’t be changed until it is reset to 0x0
- PrivID: if the transaction carries privID attribute, ISC can either direct use the privID attribute from the transaction by setting the pass field to 0x0, or overwrite it using the new value define in this control register by setting the pass field to be 0x1. If the transaction does not have privID attribute, the ISC will add the privID to this transaction, regardless of the value in the pass field.
- Secure attribute: the transaction can either be forced to be non-secure mode by setting nonsec field to be 0x1, or force the transaction to be secure by setting sec field to be 0xA, or just pass through the secure

attribute if the original transaction carries secure attribute. For an initiator which does not provide secure attributes, it is default set to non-secure.

- Priv attribute: by default priv attribute is not set. ISC can be used to overwrite priv attribute either to be user mode by setting nopri field to 0xF, or supervisor mode by setting priv field to be 0xF

3.8.2 Transaction Attributes for BCDMA and PktDMA Transactions

Section 3.6 and Section 3.8.1 provide information on how to set up the attributes on the generic transaction. But the BCDMA and pktDMA transactions do not rely on the ISC block and QoS block to set the transaction attributes. Instead, those attributes are determined by the various DMA configuration registers:

Table 3-7. BCDMA and PktDMA Transaction Attributes

	How to configure BCDMA/PktDMA Transactions	Link
ASEL	descriptors: host packet descriptor and host buffer descriptor for pktDMA and Transfer Request (TR) descriptors for BCDMA	See DMASS Transfer Request Descriptor
priority	channel priority control register	See Channel Priority Control Register
orderID	channel priority control register	
secure	flow credential registers	See Flow Credential Register
priv	flow credential registers	
privID	flow credential registers	
atype	channel configuration MMR. Fixed to 2b'00	

3.8.3 Firewall Block

There are two types of firewall: region based firewall and channelized firewall.

The channelized firewall is only implemented to protect the registers which control the power domain and LPSC for security enclave. User can’t modify the channelized firewall setting.

Region based firewalls are inserted at the target end point in the interconnect. Normally a group of the target interfaces share one region-based firewall. Each region-based firewall has its unique configuration of:

- FWID: this is a unique index of firewall block.
- Number of protected regions: this is to indicate how many protected regions users can define and program
- Memory regions behind this firewall: transactions sent to those memory regions will go through this firewall protection

Majority of the memory regions in the SoC are protected by region-based firewalls, except the public boot ROM, debug cell, and STM.

Section 3.8.3.1 shows the firewall summary on SoC.

3.8.3.1 Region Based Firewalls

Table 3-8. Region Based Firewalls

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	DDR16SS0	1	3	8	0x45000400	DDR16SS0	emif_ddrdata	0x80000000	0xFFFFFFFF	No
CBASS0	COMPUTE_CLUSTER0	2	3	8	0x45000800	COMPUTE_CLUSTER0				Yes
CBASS0	MSRAM_256K0	14	3	4	0x45003800	MSRAM_256K0	RAM	0x70000000	0x7003FFFF	No
CBASS0	MSRAM_256K1	15	3	4	0x45003C00	MSRAM_256K1	RAM	0x70040000	0x7007FFFF	No
CBASS0	MSRAM_256K2	16	3	4	0x45004000	MSRAM_256K2	RAM	0x70080000	0x700BFFFF	No
CBASS0	MSRAM_256K5	17	3	4	0x45004400	MSRAM_256K5	RAM	0x70140000	0x7017FFFF	No
CBASS0	MSRAM_256K4	18	3	4	0x45004800	MSRAM_256K4	RAM	0x70100000	0x7013FFFF	No
CBASS0	MSRAM_256K3	19	3	4	0x45004C00	MSRAM_256K3	RAM	0x700C0000	0x700FFFFF	No
CBASS0	DMASS0_SEC_PROXY_0	20	3	8	0x45005000	DMASS0_SEC_PROXY_0	SEC_PROXY_SRC_TARGET_DATA	0x4D000000	0x4D07FFFF	No
CBASS0	DMASS0_SEC_PROXY_0	20	3	8	0x45005000	DMASS0_RINGACC_0	RINGACC_SRC_FIFOS	0x4E000000	0x4E3FFFFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_PSC0	psc	0x04000000	0x04000FFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_PLLCTRL0	MEM	0x04020000	0x040201FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_PLL0	CFG	0x04040000	0x04040FFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_PADCFG_CTRL0	CFG0	0x04080000	0x04087FFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_ESM0	CFG	0x04100000	0x04100FFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_GPIO0	MEM	0x04201000	0x042010FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_MCU_GPIOMUX_INTROUTER0	intr_router_cfg	0x04210000	0x042101FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_TIMEOUT0	CFG	0x04300000	0x043003FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_CTRL_MMR0	CFG0	0x04500000	0x0451FFFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_ECC_AGGR0	REGS	0x04700000	0x047003FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_CBASS0	ERR	0x04720000	0x047203FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_TIMER0	CFG	0x04800000	0x048003FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_TIMER1	CFG	0x04810000	0x048103FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_TIMER2	CFG	0x04820000	0x048203FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_TIMER3	CFG	0x04830000	0x048303FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_RTI0	CFG	0x04880000	0x048800FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_I2C0	CFG	0x04900000	0x049000FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_I2C1	CFG	0x04910000	0x049100FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_UART0	MEM	0x04A00000	0x04A001FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_UART1	MEM	0x04A10000	0x04A101FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_MCSPI0	CFG	0x04B00000	0x04B003FF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_MCSPI1	CFG	0x04B10000	0x04B103FF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_DCC0	CFG	0x04C00000	0x04C0003F	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_MCRC64_0	mcrc64	0x04D00000	0x04D00FFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_M4FSS0_IRAM_0	blazar_iram	0x05000000	0x0503FFFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_M4FSS0_DRAM_0	idram_slv_ram	0x05040000	0x0504FFFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_M4FSS0_RAT_0	RAT	0x05FF0000	0x05FF0FFF	No
CBASS0	MCU_PSC0	21	3	8	0x45005400	MCU_M4FSS0_ECC_AGGR_0	ECC_AGGR	0x05FF1000	0x05FF13FF	No
CBASS0	GICSS0	22	3	16	0x45005800	GICSS0	GIC_TRANSLATER	0x01000000	0x013FFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	GICSS0	GIC	0x01800000	0x018FFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	DRAM0_SLV_RAM	0x30000000	0x30001FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	DRAM1_SLV_RAM	0x30002000	0x30003FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_RTU0_PR1_RTU0_IRAM_RAM	0x30004000	0x30005FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_RTU1_PR1_RTU1_IRAM_RAM	0x30006000	0x30007FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	rat	0x30008000	0x30008FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	rat	0x30009000	0x30009FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP_TX0_IRAM_RAM	0x3000A000	0x3000BFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP_TX1_IRAM_RAM	0x3000C000	0x3000DFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	RAM_SLV_RAM	0x30010000	0x3001FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	pr1_icss_intc_intc_slv	0x30020000	0x30021FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP0_IRAM	0x30022000	0x300220FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP0_IRAM_DEBUG	0x30022400	0x300224FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_RTU0_PR1_RTU0_IRAM	0x30023000	0x300230FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0x30023400	0x300234FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_RTU1_PR1_RTU1_IRAM	0x30023800	0x300238FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0x30023C00	0x30023CFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP1_IRAM	0x30024000	0x300240FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP1_IRAM_DEBUG	0x30024400	0x300244FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PROTECT_SLV	0x30024C00	0x30024CFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP_TX0_IRAM	0x30025000	0x300250FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP_TX0_IRAM_DEBUG	0x30025400	0x300254FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP_TX1_IRAM	0x30025800	0x300258FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP_TX1_IRAM_DEBUG	0x30025C00	0x30025CFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_CFG_SLV	0x30026000	0x300261FF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PA_STAT_WRAP_PA_SLV_QSTAT	0x30027000	0x300277FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	pr1_icss_uart_uart_slv	0x30028000	0x3002803F	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0x3002A000	0x3002A0FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0x3002A100	0x3002A1FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0x3002A200	0x3002A2FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0x3002A300	0x3002A3FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	0x3002A400	0x3002A4FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	0x3002A500	0x3002A5FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PA_STAT_WRAP_PA_SLV_CSTAT	0x3002C000	0x3002C7FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_IEP0_SLV	0x3002E000	0x3002EFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_IEP1_SLV	0x3002F000	0x3002FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_ICSS_ECAP0_ECAP_SLV	0x30030000	0x300300FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_MII_RT_PR1_MII_RT_CFG	0x30032000	0x300320FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0x30032100	0x300321FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0x30032200	0x300322FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_MDIO_V1P7_MDIO	0x30032400	0x300324FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0x30033000	0x30033FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP0_IRAM_RAM	0x30034000	0x30037FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PR1_PDSP1_IRAM_RAM	0x30038000	0x3003BFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	PA_STAT_WRAP_PA_SLV	0x3003C000	0x3003C0FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	DRAM0_SLV_RAM	0x30080000	0x30081FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	DRAM1_SLV_RAM	0x30082000	0x30083FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_RTU0_PR1_RTU0_IRAM_RAM	0x30084000	0x30085FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_RTU1_PR1_RTU1_IRAM_RAM	0x30086000	0x30087FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	rat	0x30088000	0x30088FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	rat	0x30089000	0x30089FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP_TX0_IRAM_RAM	0x3008A000	0x3008BFFF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP_TX1_IRAM_RAM	0x3008C000	0x3008DFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	RAM_SLV_RAM	0x30090000	0x3009FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	pr1_icss_intc_intc_slv	0x300A0000	0x300A1FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP0_IRAM	0x300A2000	0x300A20FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP0_IRAM_DEBUG	0x300A2400	0x300A24FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_RTU0_PR1_RTU0_IRAM	0x300A3000	0x300A30FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0x300A3400	0x300A34FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_RTU1_PR1_RTU1_IRAM	0x300A3800	0x300A38FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0x300A3C00	0x300A3CFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP1_IRAM	0x300A4000	0x300A40FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP1_IRAM_DEBUG	0x300A4400	0x300A44FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PROTECT_SLV	0x300A4C00	0x300A4CFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP_TX0_IRAM	0x300A5000	0x300A50FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP_TX0_IRAM_DEBUG	0x300A5400	0x300A54FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP_TX1_IRAM	0x300A5800	0x300A58FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP_TX1_IRAM_DEBUG	0x300A5C00	0x300A5CFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_CFG_SLV	0x300A6000	0x300A61FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PA_STAT_WRAP_PA_SLV_QSTAT	0x300A7000	0x300A77FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	pr1_icss_uart_uart_slv	0x300A8000	0x300A803F	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0x300AA000	0x300AA0FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0x300AA100	0x300AA1FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0x300AA200	0x300AA2FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0x300AA300	0x300AA3FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	0x300AA400	0x300AA4FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	0x300AA500	0x300AA5FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PA_STAT_WRAP_PA_SLV_CSTAT	0x300AC000	0x300AC7FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_IEP0_SLV	0x300AE000	0x300AEFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_IEP1_SLV	0x300AF000	0x300AFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_ICSS_ECAP0_ECAP_SLV	0x300B0000	0x300B00FF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_MII_RT_PR1_MII_RT_CFG	0x300B2000	0x300B20FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0x300B2100	0x300B21FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0x300B2200	0x300B22FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_MDIO_V1P7_MDIO	0x300B2400	0x300B24FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0x300B3000	0x300B3FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP0_IRAM_RAM	0x300B4000	0x300B7FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PR1_PDSP1_IRAM_RAM	0x300B8000	0x300BBFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	PA_STAT_WRAP_PA_SLV	0x300BC000	0x300BC0FF	No
CBASS0	GICSS0	22	3	16	0x45005800	TIMERMGR0	timer_mgr_timers	0x37000000	0x3703FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	CPTS0	cpts	0x39000000	0x390003FF	No
CBASS0	GICSS0	22	3	16	0x45005800	CBASS0	ERR	0x3A000000	0x3A0003FF	No
CBASS0	GICSS0	22	3	16	0x45005800	R5FSS0_COMMON0	REGS	0x3C010000	0x3C0103FF	No
CBASS0	GICSS0	22	3	16	0x45005800	R5FSS0_COMMON0	EVNT_BUS_VBUSP_MMRS	0x3C018000	0x3C0180FF	No
CBASS0	GICSS0	22	3	16	0x45005800	R5FSS1_COMMON0	REGS	0x3C030000	0x3C0303FF	No
CBASS0	GICSS0	22	3	16	0x45005800	R5FSS1_COMMON0	EVNT_BUS_VBUSP_MMRS	0x3C038000	0x3C0380FF	No
CBASS0	GICSS0	22	3	16	0x45005800	TIMERMGR0	CONFIG	0x3CD00000	0x3CD001FF	No
CBASS0	GICSS0	22	3	16	0x45005800	MSRAM_256K0	ecc_aggr	0x3F001000	0x3F0013FF	No
CBASS0	GICSS0	22	3	16	0x45005800	MSRAM_256K1	ecc_aggr	0x3F002000	0x3F0023FF	No
CBASS0	GICSS0	22	3	16	0x45005800	MSRAM_256K2	ecc_aggr	0x3F003000	0x3F0033FF	No
CBASS0	GICSS0	22	3	16	0x45005800	GICSS0	REGS	0x3F004000	0x3F0043FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_ECC_AGGR_0	ECCAGGR	0x3F005000	0x3F0053FF	No
CBASS0	GICSS0	22	3	16	0x45005800	MSRAM_256K5	ecc_aggr	0x3F006000	0x3F0063FF	No
CBASS0	GICSS0	22	3	16	0x45005800	MSRAM_256K4	ecc_aggr	0x3F007000	0x3F0073FF	No
CBASS0	GICSS0	22	3	16	0x45005800	MSRAM_256K3	ecc_aggr	0x3F008000	0x3F0083FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG0	ECC_AGGR	0x3F00A000	0x3F00A3FF	No
CBASS0	GICSS0	22	3	16	0x45005800	PRU_ICSSG1	ECC_AGGR	0x3F00B000	0x3F00B3FF	No
CBASS0	GICSS0	22	3	16	0x45005800	R5FSS0_COMMON0	ecc_aggr	0x3F00D000	0x3F00D3FF	No
CBASS0	GICSS0	22	3	16	0x45005800	R5FSS1_COMMON0	ecc_aggr	0x3F00E000	0x3F00E3FF	No
CBASS0	GICSS0	22	3	16	0x45005800	ECC_AGGR0	REGS	0x3F00F000	0x3F00F3FF	No
CBASS0	GICSS0	22	3	16	0x45005800	MSRAM_256K6	ecc_aggr	0x3F010000	0x3F0103FF	No
CBASS0	GICSS0	22	3	16	0x45005800	MSRAM_256K7	ecc_aggr	0x3F011000	0x3F0113FF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	GICSS0	22	3	16	0x45005800	PBIST1	MEM	0x3F100000	0x3F1003FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_INTAGGR_0	INTAGGR_INTR	0x48000000	0x480FFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_INTAGGR_0	INTAGGR_IMAP	0x48100000	0x48103FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_INTAGGR_0	INTAGGR_CFG	0x48110000	0x4811001F	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_INTAGGR_0	INTAGGR_L2G	0x48120000	0x481203FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PSILCFG_0	PSILCFG_PROXY	0x48130000	0x481301FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PSILSS_0	PSILSS_MMRS	0x48140000	0x48140FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_INTAGGR_0	INTAGGR_UNMAP	0x48180000	0x4819FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_INTAGGR_0	INTAGGR_MCAST	0x48210000	0x48210FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_INTAGGR_0	INTAGGR_GCNTCFG	0x48220000	0x48221FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PSILSS_0	ETLSW_MMRS	0x48230000	0x48230FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_RINGACC_0	RINGACC_GCFG	0x48240000(1)	0x482403FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_SEC_PROXY_0	SEC_PROXY_MMRS	0x48250000	0x482500FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_CRED	0x48400000	0x484007FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_CRED	0x48410000	0x48411FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_BCHAN	0x48420000	0x48421FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_RFLOW	0x48430000	0x48433FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_TCHAN	0x484A0000	0x484A3FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_TCHAN	0x484A4000	0x484A5FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_RCHAN	0x484C0000	0x484C1FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_RCHAN	0x484C2000	0x484C3FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_GCFG	0x485C0000	0x485C00FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_GCFG	0x485C0100	0x485C01FF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_RING	0x485E0000	0x485FFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_RING	0x48600000	0x48607FFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_RINGACC_0	RINGACC_RT	0x49000000	0x493FFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_RINGACC_0	RINGACC_CFG	0x49800000	0x4983FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_INTAGGR_0	INTAGGR_GCNTRTI	0x4A000000	0x4A0FFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_SEC_PROXY_0	SEC_PROXY_SCFG	0x4A400000	0x4A47FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_SEC_PROXY_0	SEC_PROXY_RT	0x4A600000	0x4A67FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_RCHANRT	0x4A800000	0x4A81FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_RCHANRT	0x4A820000	0x4A83FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_TCHANRT	0x4AA00000	0x4AA3FFFF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_TCHANRT	0x4AA40000	0x4AA5FFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_PKTDMA_0	PKTDMA_RINGRT	0x4B800000	0x4BBFFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_RINGRT	0x4BC00000	0x4BCFFFFF	No
CBASS0	GICSS0	22	3	16	0x45005800	DMASS0_BCDMA_0	BCDMA_BCHANRT	0x4C000000	0x4C01FFFF	No
CBASS0	MSRAM_256K6	23	3	8	0x45005C00	MSRAM_256K6	RAM	0x440A0000	0x440BFFFF	No
CBASS0	MSRAM_256K6	23	3	8	0x45005C00	MSRAM_256K6	RAM	0x440C0000	0x440DFFFF	No
CBASS0	MSRAM_256K6	23	3	8	0x45005C00	MSRAM_256K6	RAM	0x70180000	0x701BFFFF	No
CBASS0	MSRAM_256K7	24	3	8	0x45006000	MSRAM_256K7	RAM	0x44060000	0x4407FFFF	No
CBASS0	MSRAM_256K7	24	3	8	0x45006000	MSRAM_256K7	RAM	0x44080000	0x4409FFFF	No
CBASS0	MSRAM_256K7	24	3	8	0x45006000	MSRAM_256K7	RAM	0x701C0000	0x701FFFFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PSRAMECC0	RAM	0x00000000	0x000003FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PADCFG_CTRL0	CFG0	0x000F0000	0x000F7FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	CBASS_DBG0	ERR	0x00200000	0x002003FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	CBASS_FW0	ERR	0x00220000	0x002203FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	EFUSE0	MEM	0x00300000	0x003000FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PBIST0	MEM	0x00310000	0x003103FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	COMPUTE_CLUSTER0_PBIST_0	PBIST	0x00330000	0x003303FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PSC0	psc	0x00400000	0x00400FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PLLCTRL0	MEM	0x00410000	0x004101FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	ESM0	CFG	0x00420000	0x00420FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	DFTSS0	MEM	0x00500000	0x005003FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	DDPA0	k3_ddpa	0x00580000	0x005803FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	GPIO0	MEM	0x00600000	0x006000FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	GPIO1	MEM	0x00601000	0x006010FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PLL0	CFG	0x00680000	0x0068FFFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PSRAMECC0	REGS	0x00700000	0x007003FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	ECC_AGGR1	REGS	0x00701000	0x007013FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	USB0	ECC_AGGR	0x00703000	0x007033FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	CPSW0	cpsw3_ecc	0x00704000	0x007043FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MMCSD0	ecc_aggr	0x00706000	0x007063FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MMCSD0	ecc_aggr	0x00707000	0x007073FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MMCSD1	ecc_aggr	0x00708000	0x007083FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MMCSD1	ecc_aggr	0x00709000	0x007093FF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	FSS0_OSPI_0	ecc_aggr	0x00716000	0x007163FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	A53SS0	ecc_aggr	0x00717000	0x007173FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	A53SS0	ecc_aggr	0x00717400	0x007177FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	A53SS0	ecc_aggr	0x00717800	0x00717BFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PCIE0	CORE_ECC_AGGR0	0x00718000	0x007183FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PCIE0	CORE_ECC_AGGR1	0x00719000	0x007193FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MAIN_GPIOMUX_INTROUTER0	intr_router_cfg	0x00A00000	0x00A007FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	CMP_EVENT_INTROUTER0	intr_router_cfg	0x00A30000	0x00A307FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	TIMESYNC_EVENT_INTROUTER0	intr_router_cfg	0x00A40000	0x00A407FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	GTC0	CFG0	0x00A80000	0x00A803FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	GTC0	CFG1	0x00A90000	0x00A93FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	GTC0	CFG2	0x00AA0000	0x00AA3FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	GTC0	CFG3	0x00AB0000	0x00AB3FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	VTM0	VTM_CFG1	0x00B00000	0x00B003FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	VTM0	VTM_CFG2	0x00B01000	0x00B013FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	VTM0	ECCAGGR_CFG	0x00B02000	0x00B023FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PDMA0	REGS	0x00C00000	0x00C003FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PDMA1	REGS	0x00C01000	0x00C013FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PBIST3	MEM	0x03310000	0x033103FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PBIST2	MEM	0x03330000	0x033303FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	CPSW0	cpsw3	0x08000000	0x081FFFFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PCIE0	PCIE_RP_CORE	0x0D000000	0x0D7FFFFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	SERDES_10G0	wiz16b2m4ct	0x0F000000	0x0F00FFFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PCIE0	CORE_USER_CFG_USER_CFG	0x0F100000	0x0F1003FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PCIE0	CORE_VMAP_OB_MMRS	0x0F101000	0x0F101FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PCIE0	CORE_PCIE_INTD_CFG_INTD_CFG	0x0F102000	0x0F102FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	PCIE0	CORE_CPTS_CFG_CPTS_VBUSP	0x0F103000	0x0F1033FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	DDR16SS0	mmc_sscfg	0x0F300000	0x0F3001FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	DDR16SS0	emif_ctlcfg	0x0F308000	0x0F30FFFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	USB0	VBP2APB_WRAP_CONTROLLER_VBP_CORE_ADDR_MAP	0x0F400000	0x0F43FFFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	USB0	MMR_MMRVBP_USBSS_CMN	0x0F900000	0x0F9000FF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	USB0	RAMS_INJ_CFG	0x0F901000	0x0F9013FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	USB0	PHY2	0x0F908000	0x0F9083FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MMCSD1	mmc_ctlcfg	0x0FA00000	0x0FA00FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MMCSD1	mmc_sscfg	0x0FA08000	0x0FA083FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MMCSD0	mmc_ctlcfg	0x0FA10000	0x0FA10FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	MMCSD0	mmc_sscfg	0x0FA18000	0x0FA183FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	FSS0	fss_genregs	0x0FC00000	0x0FC000FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	FSS0_FSAS_0	fsas_genregs	0x0FC10000	0x0FC100FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	FSS0_FSAS_0	OTFA_CFG	0x0FC20000	0x0FC20FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	FSS0_OSPI_0	ospi_flash_cfg	0x0FC40000	0x0FC400FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	FSS0_OSPI_0	ospi_cfg	0x0FC44000	0x0FC441FF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	ELM0	MEM	0x25010000	0x25010FFF	No
CBASS_INFRA1	PSRAMECC0	34	3	8	0x45008800	CTRL_MMR0	CFG0	0x43000000	0x4301FFFF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	SA2_UL0	ECC_AGGR	0x00712000	0x007123FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	ADC0	ECC_REGS	0x0071A000	0x0071A3FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	UART0	MEM	0x02800000	0x028001FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	UART1	MEM	0x02810000	0x028101FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	UART2	MEM	0x02820000	0x028201FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	UART3	MEM	0x02830000	0x028301FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	UART4	MEM	0x02840000	0x028401FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	UART5	MEM	0x02850000	0x028501FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	UART6	MEM	0x02860000	0x028601FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	I2C0	CFG	0x20000000	0x200000FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	I2C1	CFG	0x20010000	0x200100FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	I2C2	CFG	0x20020000	0x200200FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	I2C3	CFG	0x20030000	0x200300FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCSPI0	CFG	0x20100000	0x201003FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCSPI1	CFG	0x20110000	0x201103FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCSPI2	CFG	0x20120000	0x201203FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCSPI3	CFG	0x20130000	0x201303FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCSPI4	CFG	0x20140000	0x201403FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCAN0	SS	0x20700000	0x207000FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCAN0	CFG	0x20701000	0x207011FF	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCAN0	msgmem_wrap_msgmem_vbp_ram	0x20708000	0x2070FFFF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCAN1	SS	0x20710000	0x207100FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCAN1	CFG	0x20711000	0x207111FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCAN1	msgmem_wrap_msgmem_vbp_ram	0x20718000	0x2071FFFF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCAN0	ECC_AGGR	0x24018000	0x240183FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	MCAN1	ECC_AGGR	0x24019000	0x240193FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	ADC0	FIFO	0x28000000	0x280003FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	ADC0	ADCREGS	0x28001000	0x280013FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	SA2_UL0	sa_ul_primary	0x40900000	0x40900FFF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	SA2_UL0	sa_ul_updates	0x40901000	0x409011FF	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	SA2_UL0	sa_ul_rng	0x40910000	0x4091007F	No
CBASS_INFRA1	SA2_UL0	35	3	8	0x45008C00	SA2_UL0	CP_ACE_PKA_EIP29T2	0x40920000	0x4092FFFF	No
DMSC0_CBASS_0	DMSC0_ROM_0	512	1	2	0x45080000	DMSC0_ROM_0	IROM__SLV__ROM	0x00000000	0x0001FFFF	No
DMSC0_CBASS_0	DMSC0_SRAM_0	513	3	8	0x45080400	DMSC0_SRAM_0	dmsc_sram0	0x44040000	0x4404FFFF	No
DMSC0_CBASS_0	DMSC0_SRAM_1	514	3	8	0x45080800	DMSC0_SRAM_1	dmsc_sram1	0x44050000	0x4405FFFF	No
DMSC0_CBASS_0	DMSC0_PWRCTRL_0	528	3	1	0x45084000	DMSC0_PWRCTRL_0	PWR	0x44130000	0x441307FF	No
DMSC0_CBASS_0	DMSC0_DMTIMER_0	536	3	1	0x45086000	DMSC0_DMTIMER_0	DMTIMER0	0x44133000	0x441333FF	No
DMSC0_CBASS_0	DMSC0_DMTIMER_1	537	3	1	0x45086400	DMSC0_DMTIMER_1	DMTIMER1	0x44134000	0x441343FF	No
DMSC0_CBASS_0	DMSC0_RTI_0	544	3	1	0x45088000	DMSC0_RTI_0	RTI	0x44135100	0x441351FF	No
DMSC0_CBASS_0	DMSC0_WDTCTRL_0	545	3	1	0x45088400	DMSC0_WDTCTRL_0	rti	0x44135000	0x441350FF	No
DMSC0_CBASS_0	DMSC0_RAT_0	552	3	1	0x4508A000	DMSC0_RAT_0	dmsc_rat_mmrs	0x44200000	0x44200FFF	No
DMSC0_CBASS_0	DMSC0_ECC_AGGR_0	562	3	2	0x4508C800	DMSC0_ECC_AGGR_0	ECC_AGGR	0x3F009000	0x3F0093FF	No
DMSC0_CBASS_0	DMSC0_SECCTRL_0	576	3	1	0x45090000	DMSC0_SECCTRL_0	SEC	0x44230000	0x44230FFF	No
DMSC0_CBASS_0	DMSC0_DBG_AUTH_0	578	3	1	0x45090800	DMSC0_DBG_AUTH_0	DMSC_DBGAUTH_REG	0x44232000	0x442320FF	No
DMSC0_CBASS_0	DMSC0_SEC_MGR_0	582	3	2	0x45091800	DMSC0_SEC_MGR_0	SECMGR	0x44234000	0x44237FFF	No
DMSC0_CBASS_0	DMSC0_DMTIMER_2	592	3	1	0x45094000	DMSC0_DMTIMER_2	DMTIMER2	0x44238000	0x442383FF	No
DMSC0_CBASS_0	DMSC0_DMTIMER_3	593	3	1	0x45094400	DMSC0_DMTIMER_3	DMTIMER3	0x44239000	0x442393FF	No
DMSC0_CBASS_0	DMSC0_AES_0	602	3	2	0x45096800	DMSC0_AES_0	aes	0x4423C000	0x4423DFFF	No
DMSC0_CBASS_0	DMSC0_INTAGGR_0	607	3	2	0x45097C00	DMSC0_INTAGGR_0	intaggr_intr	0x44300000	0x4437FFFF	No
DMSC0_CBASS_0	DMSC0_INTAGGR_0	607	3	2	0x45097C00	DMSC0_INTAGGR_0	intaggr_imap	0x44400000	0x444007FF	No
DMSC0_CBASS_0	DMSC0_INTAGGR_0	607	3	2	0x45097C00	DMSC0_INTAGGR_0	intaggr_cfg	0x44410000	0x4441001F	No

Table 3-8. Region Based Firewalls (continued)

IP	Target	Firewall ID	Number of Priv IDs per Region	Firewall Regions	Firewall Physical Address	Instance	Interface	Start Address	End Address	ASEL Capable
DMSC0_CBASS_0	DMSC0_FWMGR_0	639	3	8	0x4509FC00	DMSC0_FWMGR_0	dmsc_fw_vbus_cfg	0x45000000	0x45FFFFFF	No

(1) This region is used by DMSS to flush any in flight data during a channel teardown. It is a requirement that this firewall be configured to allow write access by DMSS initiators.

3.8.3.2 Region Based Firewall Programming

Each firewall block can be configured to support multiple regions and each region can be configured individually.

See Section 3.8.3.1 .

3.9 System Interconnect Integration

This section describes system interconnect integration in the device, including information about clocks, resets, and hardware requests.

3.9.1 Interconnect Integration in MAIN/MCU Domain

Table 3-9 through Table 3-11 summarize the integration of CBASS0 in device MAIN/MCU domain.

Table 3-9. CBASS0 Integration Attributes

Module Instance	Attributes		
	Power Sleep Controller	Power Domain	Module Domain
CBASS0 CBASS_INFRA1	PSC0	PD0	LPSC0
MCU_CBASS0	MCU_PSC0	PD0	LPSC0

Table 3-10. CBASS0 Clocks and Resets

Clocks			
Module Instance	**Source Clock Signal**	**Source**	**Description**
CBASS0 CBASS_INFRA1	MAIN_SYSCLK0/2	PLLCTRL0	CBASS0 and CBASS_INFRA1 clocks
	MAIN_SYSCLK0/4	PLLCTRL0	
MCU_CBASS0	MCU_SYSCLK0/2	MCU_PLLCTRL0	MCU_CBASS0 clocks
	MCU_SYSCLK0/4	MCU_PLLCTRL0	
Resets			
Module Instance	**Source Reset Signal**	**Source**	**Description**
CBASS0	MOD_G_RST	LPSC0	CBASS0 reset
CBASS_INFRA1	MOD_G_RST	LPSC2	CBASS_INFRA1 reset
MCU_CBASS0	ROD_G_RST	LPSC0	MCU_CBASS0 reset

Table 3-11. CBASS0 Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
CBASS0	CBASS0_default_exp_0	DMSC0_CORTEX_M3_0_sec_in_IN_0	DMSC0_CORTEX_M3_0	CBASS0 interrupt request	level
CBASS_FW0	CBASS_FW0_default_err_intr_0	DMSC0_CORTEX_M3_0_nvic_IN_202	DMSC0_CORTEX_M3_0	CBASS_FW0 interrupt request	level
CBASS_INFRA1	CBASS_INFRA1_default_exp_0	DMSC0_CORTEX_M3_0_sec_in_IN_1	DMSC0_CORTEX_M3_0	CBASS_INFRA1 interrupt request	level
MCU_CBASS0	MCU_CBASS0_default_err_intr_0	MCU_M4FSS0_CORE0_nvic_IN_31	MCU_M4FSS0_CORE0	MCU_CBASS0 interrupt request	level
CBASS0 CBASS_DBG0 CBASS_INFRA1 MCU_CBASS0	CBASS0_default_err_intr_0(1) CBASS_DBG0_default_err_intr_0(1) CBASS_INFRA1_default_err_intr_0(1) MCU_CBASS0_default_err_intr_0(1)	GICSS0_spi_IN_133	GICSS0	CBASS0 interrupt request	level
		R5FSS0_CORE0_intr_IN_133	R5FSS0_CORE0	CBASS0 interrupt request	level
		R5FSS0_CORE1_intr_IN_133	R5FSS0_CORE1	CBASS0 interrupt request	level

Table 3-11. CBASS0 Hardware Requests (continued)

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
		R5FSS1_CORE0_intr_IN_133	R5FSS1_CORE0	CBASS0 interrupt request	level
		R5FSS1_CORE1_intr_IN_133	R5FSS1_CORE1	CBASS0 interrupt request	level

(1) The interrupts are ORed together to generate a single interrupt before routing to the destination.

Note

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

Chapter 4

Initialization

This chapter describes the steps for non-secure device initialization.

4.1 Initialization Overview

Figure 4-1 is an overview of the initialization process and its steps:

- **Preinitialization:** Power, clock, and control connections must be present, and the boot configuration pins must be held at the desired logical levels.
- **Power, clock, reset ramp sequence:** Specific sequence that is applied by the power-management chip(s)
- **ROM code:** Responsible for finding, for downloading, and for executing the initial software (SBL)
- **Initial software:** Software that loads, prepares, and passes control to application software or to the high-level operating system (HLOS)
- **High-Level Operating System** or bare-metal application which runs on main processor(s)

Figure 4-1. Initialization Process

The first two steps in the initialization process are hardware-oriented; however, they require an understanding of the process of configuring these system interface pins (balls on the device), which have software-configurable functionality. This configuration is an essential part of the chip configuration and is application-dependent. This chapter discusses these system-interface pins, the associated configuration registers, and memory structures that are vital to the correct initialization of the device.

4.1.1 ROM Code Overview

ROM bootloader (or ROM Code) is a software that resides in a on-chip read-only memory (ROM) to assist the customer in transferring and executing their application code. The device has two ROM codes operating in tandem – the Public ROM code, and the DMSC ROM code.

In order to accommodate various system scenarios, the ROM Code supports several boot modes. These boot modes can be broadly classified as:

- Host boot modes
- Memory boot modes.

During a host boot, the device is configured to receive code from a host via the selected interface. Either the host writes the application code directly into internal memory or the ROM Code receives the application code on the selected interface and stores it in internal memory.

During a memory boot, the device transfers code from non-volatile memory to internal memory for execution.

In all boot modes, the entire boot operation can be partitioned into two sections:

1. Hardware initialization phase
2. Boot process.

During initialization, the ROM Code configures the device resources (PLLs, peripherals, pins) as needed to support the boot process. The resources used depend on the boot mode requirements.

During the boot process the boot image can be loaded into device memory and executed, or executed in place, depending on the boot peripheral. DMSC will perform code verification and allow, or forbid, the image execution.

Main configuration source for boot after power-up are the BOOTMODE pins sampled automatically after reset release and stored in device status registers. At ROM Code startup, these pin values are read from the registers to create the boot peripheral list and the boot configuration tables used later to initialize and startup the PLLs and boot peripherals.

4.1.2 Bootloader Modes

Table 4-1 shows the boot modes supported by ROM code.

Table 4-1. ROM Code Boot Modes

Boot Mode	Boot Media/Host	SoC Peripheral	Can be a Backup Mode?[1]	Notes
No-boot/Dev-boot	No media or host	None	N	No boot or development boot – debug modes
OSPI	OSPI flash	FSS0_OSPI0	N	On OSPI port
QSPI	QSPI flash/EEPROM	FSS0_OSPI0	N	On OSPI port
SPI	SPI EEPROM	FSS0_OSPI0	Y	On OSPI port
Ethernet	External host	CPSW0	Y	In BOOTP mode. RGMII or RMII PHY
I2C	I^2C EEPROM	I2C0	Y	I2C target boot is not supported
UART	External host	UART0	Y	XMODEM protocol
MMCSD	eMMC Flash or SD card	MMCSD0 (8bit) or MMCSD1 (4bit)	Y	Boot from User Data Area (UDA) in raw or file system mode
eMMC	eMMC flash	MMCSD0 (8bit)	N	Boot from boot partition
USB - target	USB boot from external host	USB0	Y	USB device mode boot using DFU (device firmware upgrade), Boot is running on USB2.0 speeds.
USB - host	USB mass storage	USB0	Y	USB2.0 host mode, boot from FAT32 filesystem
PCIe	External host	PCIE1	N	Gen2 enabled
xSPI	xSPI flash	FSS0_OSPI0	N	On OSPI port
GPMC	NOR flash, NAND flash	GPMC0	N	CSn0 connected, 8 bit NAND flash only, 16-bit non-mux NOR flash only

(1) The peripheral can be selected also as a backup boot mode. A backup mode is tried if primary boot mode fails.

Note

Because different devices support different sets of peripherals, see the *device-specific Datasheet* to obtain the list of peripherals supported in your device.

4.1.3 Boot Terminology

- **Boot Mode Pins:** Boot mode pins provide vital information to ROM code for boot. These pins must be properly set up before power ramp.
- **Bootstrap:** Initial software launched by the ROM code during the memory booting phase.
- **Boot Header:** Optional structure that precedes the initial software and allows the redefinition of the ROM code default settings.
- **Downloaded software:** Initial software downloaded into on-chip RAM by the ROM code during the peripheral booting phase.
- **eFuse:** A one-time programmable memory location usually set at the factory.
- **Flash loader:** Downloaded software launched by the ROM code during the preflashing stage and programs an image in external memories.
- **HS device:** HS-Security device (SoC)
- **HS-FS device:** (HS-Field Securable) - This is the HS device state before the customer keys are provisioned in the device (the state at which HS device leaves TI factory). In this state, secure features are not available and the device protects the ROM code, TI keys and certain security peripherals. In this state, the device does not force authentication for booting.

- **HS-SE device:** (HS-Security Enforced) - This is the HS device state after the customer keys are successfully provisioned in the device. In an HS-SE device, all security features are enabled, all secrets within the device are fully protected, all of the security goals are fully enforced, debug override sequence is supported and the device forces secure booting.
- **Initial software:** Software executed by any of the ROM code mechanisms (memory booting or peripheral booting). Initial software is a generic term for bootstrap and downloaded software. This can be the SBL (secondary bootloader) responsible for loading an OS.
- **Memory booting:** ROM code mechanism that consists of downloading initial software from external memory to OCSRAM and executing.
- **Controller CPU:** The Arm® Cortex® CPU for which CPU-ID is 0. This core configures the multicore platform and starts the ROM code to boot device from a mass storage memory (memory booting) or a peripheral interface (peripheral booting).
- **Peripheral booting:** ROM code mechanism that consists of polling selected interfaces, downloading, and executing initial software (in this case, downloaded software) in the internal RAM.
- **Preflashing:** A specific case of peripheral booting where the ROM code mechanism is used to program the external flash memory.
- **ROM Code:** or ROM bootloader (RBL), the on-chip software in device ROM that executes first and implements booting.
- **ROM Code-controlled Boot Phase:** This phase covers the sequence operations from the time the platform releases the reset to the time first user- or customer-owned software starts execution. This phase is fully controlled by the device ROM code.
- **Booting Parameter Table:** A logical structure stored in the on-chip RAM memory and contains information for the boot, such as the boot file name or an address to boot from.

4.2 Boot Process

4.2.1 Public ROM Code Architecture

The Public ROM code has the following components (see alsoPublic ROM Code Architecture):

- Main
- Buffer manager
- X.509
- Log and Trace
- System
- Protocol
- Driver

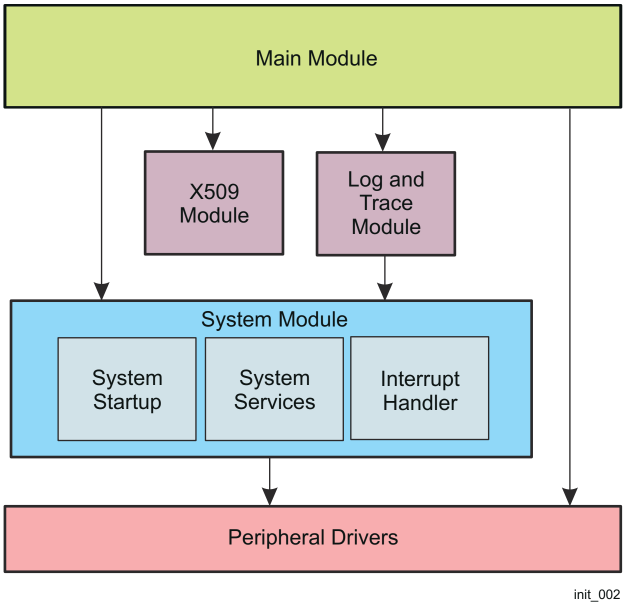

Figure 4-2. Public ROM Code Architecture

4.2.1.1 Main Module

The Main module contains the top level execution loop. This loop repeats until a boot image has been received or directed to sleep by the DMSC. The main loop has three different execution sub-paths based on the boot peripheral.

- **Image Path** This path is used by the USB-DFU, PCIe, OSPI, and QSPI boot modes. In these cases the image data can be directly read by both, MCU and DMSC, in place.
- **Block Path** This path is used by the SPI, I2C, UART, eMMC, Ethernet and MMCSD cards in raw mode. In this mode data is received from the peripheral in blocks. Blocks are accumulated in the boot buffer until a full X.509 certificate header has been received, at which point this full certificate and any subsequent blocks are passed to the DMSC as they arrive.
- **Filesystem Path** This path is used by the MMCSD cards in filesystem mode. This mode executes exactly like in the block path, except that the boot image location is defined by a filesystem.

The main level is able to detect if a received boot image is in the correct format and reject non-conforming images.

4.2.1.2 X509 Module

The X509 module parses the boot header. The boot header is an X.509 certificate as defined in RFC5280. Extensions specific to boot are described in Section 4.7.2 , *X.509 Certificate*.

This module also includes an OID decoder as well as defines OID values as C #define constants for any values that can be used during boot.

4.2.1.3 Buffer Manager Module

The buffer manager module is used to allocate buffers to hold boot data. The MCU code allocates a buffer when it is ready to read a block of data from the boot peripheral. Once the data is read the buffer ownership is passed to the DMSC. When the DMSC has completed processing the data in the buffer ownership is returned to the MCU, which then frees the buffer.

4.2.1.4 Log and Trace Module

The Log and Trace modules are not integral to the boot process. Instead, they provide ability to record operation of the ROM code and track unexpected occurrences.

Log and trace function is currently TI internal.

4.2.1.5 System Module

The system module provides services to other modules. These services are not directly related to boot drivers. The system module is the only module that operates in the supervisor mode of the MCU (a few services will run in user). The system module supports the following functions:

- Interrupt enable, disable, and service
- IPC
- Power
- Pinmux
- Clock
- Task switch

The main level is able to detect if a received boot image is in the correct format and reject non-conforming images.

4.2.1.6 Protocol Module

The protocol modules provide implementation of high-level data transfer protocols. The BOOTP/TFTP and XMODEM protocols reside in this layer. These modules provide services as defined in well-known standards.

4.2.1.7 Driver Module

The driver module implements the low level peripheral drivers.

4.2.2 DMSC ROM Description

In a general-purpose (GP) device, DMSC ROM performs the following functions:

- Device management
- Configures the boot vectors (in BOOT_CFG) and controls reset release of R5 core. That is, DMSC is the boot controller of R5 core.
- IPC configuration via Main DMSS rings and Secure Proxy
- PLL configuration (R5 and SA2UL)
- X509 certificate parsing
- SA2UL configuration to SHA512 for image integrity checks
- DMSC firmware loading

4.2.3 Boot Process Flow

The R5 boot process flow is shown in Figure 4-3.

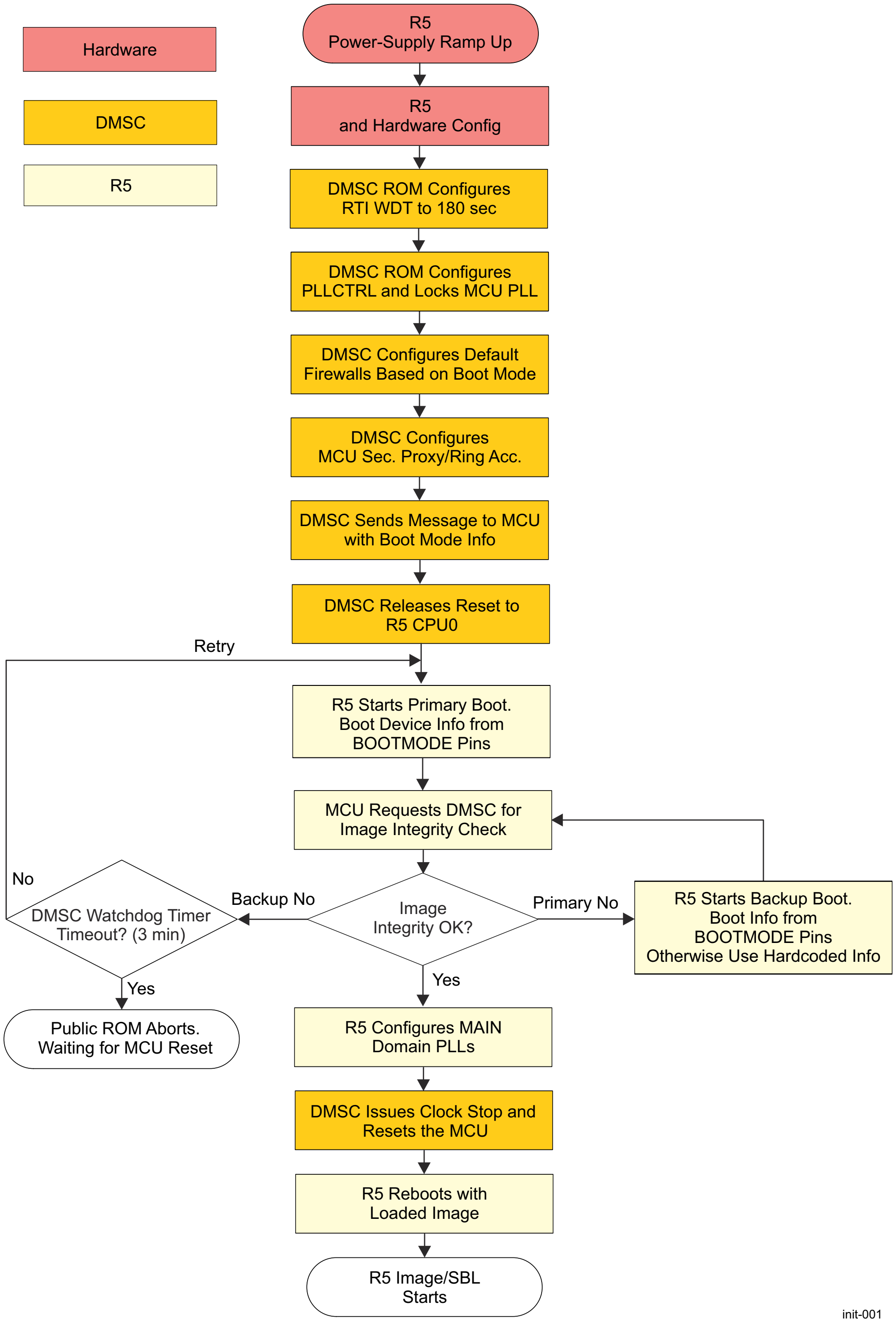

Figure 4-3. Boot Process

The values of BOOTMODE[15:0] pins are latched into the Device Status register CTRLMMR_MAIN_DEVSTAT[15:0] by hardware as the device comes out of global cold reset, sampled after MCU_PORz deassertion. For more information how to set BOOTMODE pins, see Section 4.3 , *Boot Mode Pins*.

The DMSC is the boot controller for the Public ROM. DMSC performs the necessary configurations and releases R5's reset for CPU0.

The R5 checks the boot mode pins and then configures the apropriate peripheral interface to get access to a boot image. A cursory check of the image is made, and the image is passed to DMSC. DMSC ROM then will perform code verification and route the boot image to the on-chip RAM. Once the image has been received, R5 enters a clean state and idles. DMSC ROM code will assert reset to the MCU, redirect the boot vector to the newly loaded image, and release the reset. This restarts the R5 with the Public ROM code fully disconnected.

The Public ROM code executes after a cold or warm reset.

Note

DMSC ROM sets up a 3-minute watchdog timer (MCU_RTI0) timeout. During this time, the MCU boot needs to get completed, otherwise a WDT reset will occur. Once the R5 image is loaded (SBL/SPL), DMSC ROM will restart the watchdog timer for additional 3 minutes upon entering the R5 SBL. The customer-provided MCU image needs to load and install the TI-provided SYSFW image into the DMSC, which will manage the watchdog timer during run time.

Note

The following system conditions must be met at POR to perform device boot:

- USB cable plug must be inserted
- Ethernet PHY is powered up and out of reset
- The SD card cage must be powered before entering the SD card boot mode. A SD/MMC card with pre-loaded image must be inserted
- Memory devices must be up and ready (power ramped up and reset completed) at device startup:
  - eMMC
  - OSPI/QSPI flash
  - SPI or I2C EEPROM
  - NOR flash

Failing to meet these requirements may result in boot fail and performing a backup boot (if available for that mode).

Figure 4-4 describes the external bootloader (SBL) typical tasks.

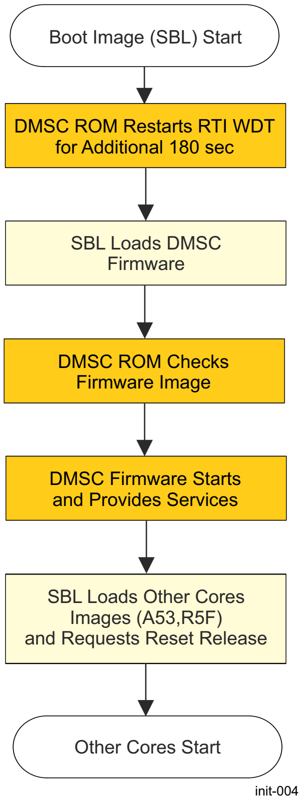

Figure 4-4. External Bootloader Tasks

Upon R5 reset and SBL execution start, DMSC ROM restarts the RTI watchdog timer for additional 180 seconds of timeout. During that time, SBL must load the DMSC firmware provided by TI otherwise a MCU reset will occur as a preventive measure against software misbehavior.

One of the SBL's main tasks is to load the DMSC firmware. Only after this task is performed, SBL can load the other processors' image and request a reset release from DMSC firmware for those cores.

4.3 Boot Mode Pins

Boot Mode pins provide means to select the boot mode and options before the device is powered up. After every POR, they are the main source to populate the Boot Parameter Tables. See Section 4.6 , *Boot Parameter Tables* for table list and description.

Boot mode pins can be divided into the following categories:

- **BOOTMODE[02:00]** – Denote system clock frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration.
- **BOOTMODE[06:03]** – Select the requested boot (primary) mode after POR, that is, the peripheral/memory to boot from.
- **BOOTMODE[09:07]** – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected.
- **BOOTMODE[12:10]** – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.
- **BOOTMODE[13]** – This pin provides optional configurations for the backup boot devices.
- **BOOTMODE[15:14]** – Reserved pins.

Note

It is user's responsibility to set the boot mode pins (via pullups or pulldowns, and jumpers/switches) depending on the desired boot scenario.

4.3.1 BOOTMODE Pin Mapping

The ROM execution is directed through the main boot mode pins. This provides more flexibility and more booting peripherals to boot from. The Main domain must be powered and functional.

Main boot mode pins are shown in Table 4-2.

Any Bootmode pins marked as Reserved or not used must be tied high or low with pull resistors. They should not be left floating.

Table 4-2. BOOTMODE Pin Mapping

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

Table 4-3 describes the BOOTMODE pins that need to be set according to the system clock provided to the device.

The ROM Code will configure any PLLs required during the boot process. The ROM Code does not have the ability to select HFOSC1 (in Main domain) during initial boot, however the selection can be done through the boot certificate (see Section 4.7 , *Boot Image Format*).

Note

Reference clock selections may be limited by the device. Please consult the device specific datasheet to determine which system clock frequencies are valid.

Table 4-3. PLL Reference Clock Selection

PLL Config Pins			Ref Clock (MHz)
B2	**B1**	**B0**	
0	1	1	25

4.3.1.1 Primary Boot Mode Selection and Configuration

The primary boot mode is the first mode attempted after reset. Table 4-4 lists all possible primary boot modes. All pins marked as reserved can be either 0 or 1. All boot mode signals must be pulled low or high through a pull resistor on the board, they must not be left floating

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Note

All BOOTMODE[15:00] signals must be pulled high through a resistor to VDDSHV3, or pulled low to ground, including Reserved signals. Reserved BOOTMODE signals must not be left floating.

Table 4-4. Primary Boot Mode Selection

Primary Boot Mode Config							Primary Boot Mode
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	
Reserved	Reserved	Reserved	0	0	0	0	Reserved
Reserved	Iclk	Csel	0	0	0	1	OSPI
Reserved	Iclk	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Clkout	0	Link Info	0	1	0	0	Ethernet RGMII
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)

Table 4-4. Primary Boot Mode Selection (continued)

Primary Boot Mode Config							Primary Boot Mode
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Reserved	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFDP	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	0(1)	No/Dev	1	1	1	1	No-boot/Dev boot

(1) Only applicable for Dev Boot Mode.

4.3.1.2 Backup Boot Mode Selection and Configuration

The backup boot mode is selected via pins within the main BOOTMODE map. Table 4-5 lists all possible backup boot modes.

Table 4-5. Backup Mode Selection

Backup Boot Config	Backup Boot Mode Selection			Backup Boot Mode Selected
B13	**B12**	**B11**	**B10**	
Reserved	0	0	0	None
Mode	0	0	1	USB
Reserved	0	1	0	Reserved
Reserved	0	1	1	UART
IF	1	0	0	Ethernet
Port	1	0	1	MMCSD Boot (SD Card Boot or eMMC Boot)
Reserved	1	1	0	SPI
Reserved	1	1	1	I2C

4.4 Boot Modes

4.4.1 Boot with OSPI Controller

The following apply to all or multiple boot modes that are SPI related.

- Octal SPI flash memories support various protocols, however, the OSPI boot mode of the device will only support a specific protocol defined in OSPI Bootloader Operation. If the flash memory is complaint with JEDEC xSPI standards JESD251 and JESD216D, then xSPI boot mode is additionally supported. Refer to the xSPI boot mode description for further details.
- When using a OSPI\xSPI\QSPI\SPI flash device greater than 128Mb which supports 3-byte and 4-byte addressing modes, a flash device package with a RESET signal must be used. The reason is that the ROM only uses 3-byte addressing mode (address is 24 bits). To address the full memory address range, software will typically switch to 4-byte addressing mode. If a reset to the processor occurs (for example, due to a warm reset), the ROM will execute expecting 3-byte addressing mode, but the flash will have been left in 4-byte addressing mode. For the flash device to return to 3-byte addressing mode, it must be reset using this signal. This typically can be achieved by using the RESET signal on the flash memory device. The ROM does not issue a software reset command.

4.4.1.1 OSPI Boot

Refer to Section 4.4.1 section for more information about all SPI boot modes.

OSPI Configuration Fields table shows configuration pins assignment to functions when boot mode is the Octal SPI. The BOOTMODE pin corresponding to the Iclk field determines the setting for LOOPCLK_SEL bit field in CTRLMMR_OSPI0_CLKSEL register

Table 4-6. OSPI Configuration Fields

BOOTMODE Pins	Field	Value	Description
8	Iclk	0	Iclock source external
		1	Iclock source internal (pad loopback)
7	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

OSPI Pin Usage table summarizes the OSPI pin configuration done by ROM code for OSPI boot device.

Table 4-7. OSPI Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
OSPI0_CLK	OSPI0_CLK	Disable	Up	0	Disable	Enable	0
OSPI0_LBCLKO	OSPI0_LBCLKO	Disable	Up	0	Enable	Enable	0
OSPI0_DQS	OSPI0_DQS	Disable	Up	0	Enable	Disable	0
OSPI0_D0	OSPI0_D0	Enable	Up	0	Enable	Enable	0
OSPI0_D1	OSPI0_D1	Enable	Up	0	Enable	Enable	0
OSPI0_D2	OSPI0_D2	Enable	Up	0	Enable	Enable	0
OSPI0_D3	OSPI0_D3	Enable	Up	0	Enable	Enable	0
OSPI0_D4	OSPI0_D4	Enable	Up	0	Enable	Enable	0
OSPI0_D5	OSPI0_D5	Enable	Up	0	Enable	Enable	0
OSPI0_D6	OSPI0_D6	Enable	Up	0	Enable	Enable	0
OSPI0_D7	OSPI0_D7	Enable	Up	0	Enable	Enable	0
OSPI0_CSn0(1)	OSPI0_CSn0	Enable	Up	0	Disable	Enable	0
OSPI0_CSn1(1)	OSPI0_CSn1	Enable	Up	0	Disable	Enable	0

(1) OSPI0_CSn0 and OSPI0_CSn1 are configured as chip select outputs from the OSPI0 host controller, but OSPI boot only uses the chip select output selected via BOOTMODE[7].

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

4.4.1.1.1 OSPI Bootloader Operation

The OSPI protocol is described according to bit-width (1 or 8) and data rate (Single Data Rate (S) or Double Data rate (D)) for the Command/Address/Data segments of the protocol. The OSPI boot mode supports 1S-1S-8S mode. The Command and Address issued are 8 bits and 24 bits respectively. The Read Command that is issued for OSPI mode is 0x8B followed by zero for address and 8 dummy cycles. The frequency of operation supported is 50 MHz

4.4.1.1.1.1 OSPI Initialization Process

In the OSPI boot mode, the ROM Code initializes the OSPI module and the image is read from the OSPI flash connected to the selected chip-select. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM. See Section 4.4.1.1 , *OSPI Boot Device Configuration* for OSPI port settings.

A detailed summary of the OSPI boot parameter table and the boot configuration definitions are listed in Section 4.6.3 , *OSPI Boot Parameter Table*.

4.4.1.1.1.2 OSPI Loading Process

OSPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

4.4.1.2 xSPI Boot

Refer to Section 4.4.1 section for more information about all SPI boot modes.

Table 4-8 shows configuration pins assignment to functions when boot mode is xSPI using the OSPI module.

Table 4-8. xSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	SFDP	0	SFDP disabled
		1	SFDP enabled
8	Read cmd	0	0x0B Read Command
		1	0xEE Read Command
7	Mode	0	1S-1S-1S mode @ 50MHz
		1	8D-8D-8D mode @ 25MHz

Table 4-9 summarizes the OSPI pin configuration done by ROM code for xSPI boot device on port 0.

Table 4-9. xSPI Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
OSPI0_CLK	OSPI0_CLK	Disable	Up	0	Disable	Enable	0
OSPI0_LBCLKO	OSPI0_LBCLKO	Disable	Up	0	Enable	Enable	0
OSPI0_DQS	OSPI0_DQS	Disable	Up	0	Enable	Disable	0
OSPI0_D0	OSPI0_D0	Enable	Up	0	Enable	Enable	0
OSPI0_D1	OSPI0_D1	Enable	Up	0	Enable	Enable	0
OSPI0_D2	OSPI0_D2	Enable	Up	0	Enable	Enable	0
OSPI0_D3	OSPI0_D3	Enable	Up	0	Enable	Enable	0
OSPI0_D4	OSPI0_D4	Enable	Up	0	Enable	Enable	0
OSPI0_D5	OSPI0_D5	Enable	Up	0	Enable	Enable	0
OSPI0_D6	OSPI0_D6	Enable	Up	0	Enable	Enable	0
OSPI0_D7	OSPI0_D7	Enable	Up	0	Enable	Enable	0
OSPI0_CSn0(1)	OSPI0_CSn0	Enable	Up	0	Disable	Enable	0
OSPI0_CSn1(1)	OSPI0_CSn1	Enable	Up	0	Disable	Enable	0
OSPI0_CSn2(1)	OSPI0_CSn2	Enable	Up	0	Disable	Enable	0
OSPI0_CSn3(1)	OSPI0_CSn3	Enable	Up	0	Disable	Enable	0

(1) OSPI0_CSn0, OSPI0_CSn1, OSPI0_CSn2 and OSPI0_CSn3 are configured as chip select outputs from the OSPI0 host controller, but xSPI boot only uses OSPI0_CSn0. It is not possible to select OSPI0_CSn1, OSPI0_CSn2 or OSPI0_CSn3 as a chip select option for xSPI boot.

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

4.4.1.2.1 xSPI Bootloader Operation

The xSPI protocol defines 1S-1S-1S mode for general backwards compatibility, and 8D-8D-8D for maximum throughput (where bit-width (1 or 8) and data rate (Single Data Rate or Double Data rate).

For 1S-1S-1S mode of operation (Bit-width =1, Single Data Rate). The Command and Address issued are 8 bits and 24 bits respectively. The Read Command that is issued is 0x0b.The frequency of operation supported is 50 MHz.

For 8D-8D-8D mode of operation (Bit-width =8, Double Data Rate). The Command and Address issued are 8 bits and 32 bits respectively. The Read Command that is issued is 0x0b or 0xee. The frequency of operation will be 25MHz for device silicon revisions that are affected by errata i2420, or 20MHz for device silicon revisions which are not affected by i2420. Please refer to device specific errata documentation for more information.

For SFDP mode ROM starts operation in 1S-1S-1S mode reads SFDP header from flash memory to get 8D-8D-8D switching sequence, Read Command, CMD Extension and Byte Order. SFDP parsing of ROM is described below and on successful parsing ROM will issue 8D-8D-8D command switching sequence and then will read the boot image in 8D-8D-8D mode with read command specified in SFDP header

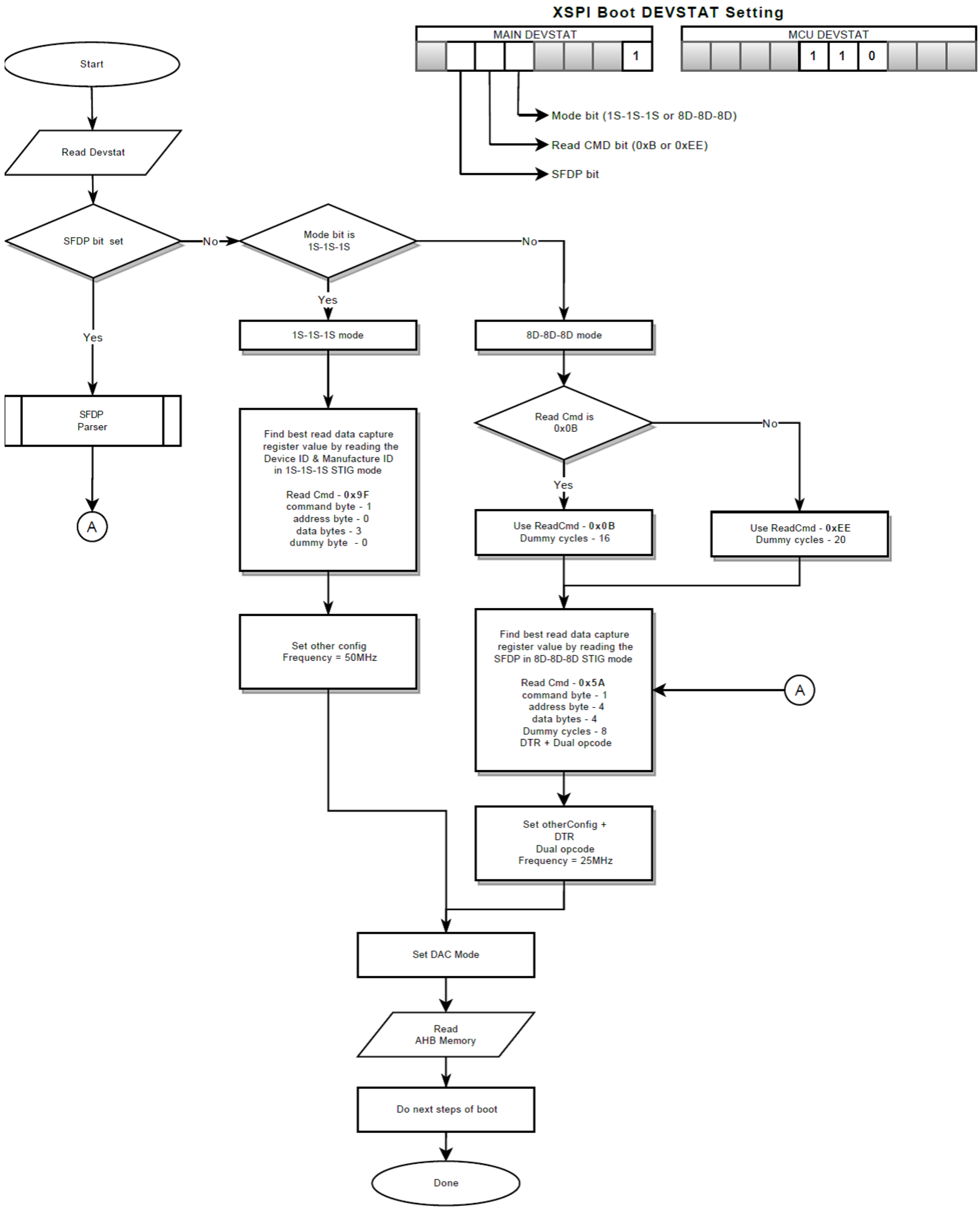

Figure 4-5. xSPI Flow Chart

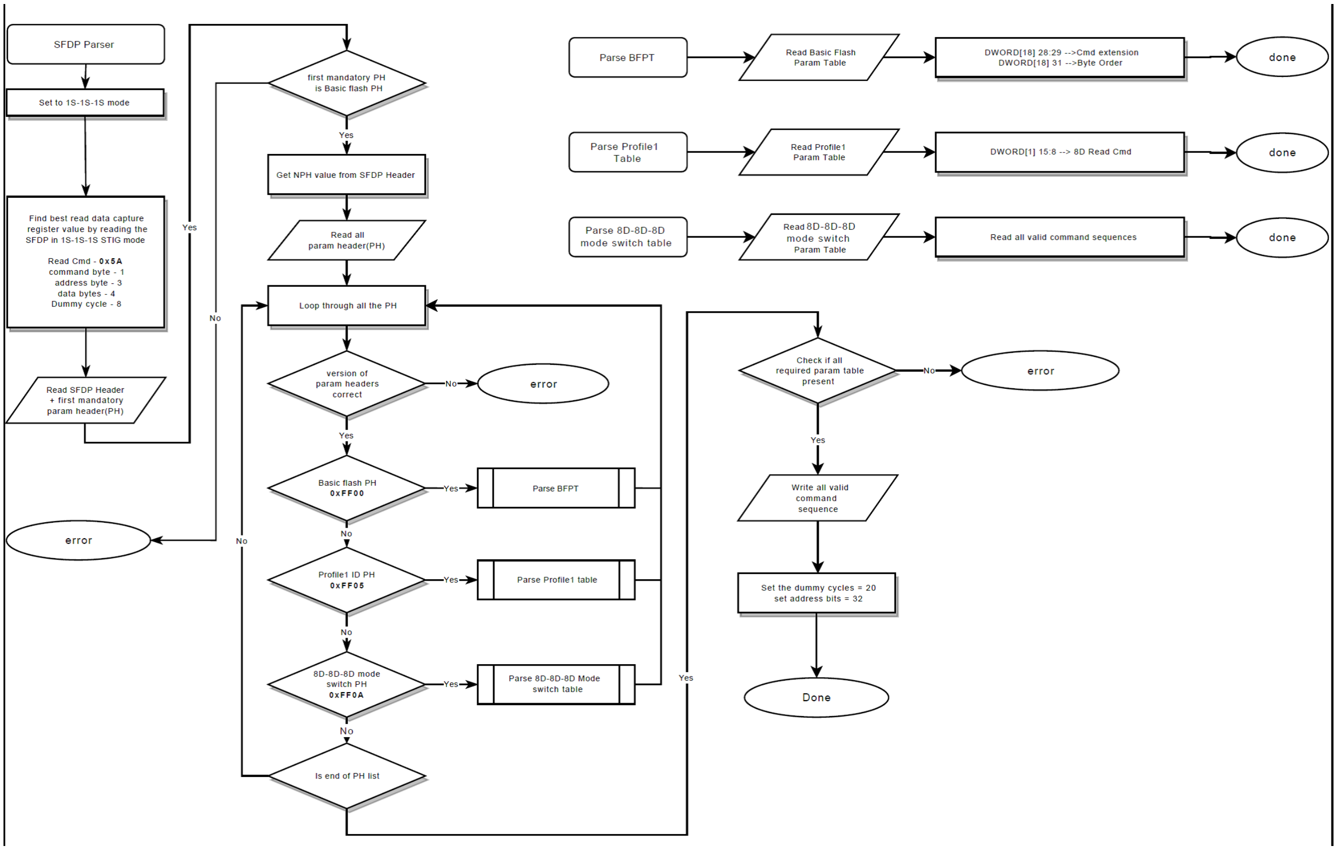

Figure 4-6. ROM SFDP Parser Flow

4.4.1.2.2 xSPI Initialization Process

In the xSPI boot mode, the ROM Code initializes the xSPI module and the image is read from the xSPI flash connected. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM.

4.4.1.3 QSPI Boot

Refer to Section 4.4.1 section for more information about all SPI boot modes.

Table 4-10 shows configuration pins assignment to functions when boot mode is QSPI using the OSPI module.

Table 4-10. QSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8	Iclk	0	Iclock source external
		1	Iclock source internal (pad loopback)
7	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 4-11 summarizes the OSPI pin configuration done by ROM code for QSPI boot device on port 0.

Table 4-11. QSPI Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
OSPI0_CLK	OSPI0_CLK	Disable	Up	0	Disable	Enable	0
OSPI0_LBCLKO	OSPI0_LBCLKO	Disable	Up	0	Enable	Enable	0
OSPI0_DQS	OSPI0_DQS	Disable	Up	0	Enable	Disable	0
OSPI0_D0	OSPI0_D0	Enable	Up	0	Enable	Enable	0
OSPI0_D1	OSPI0_D1	Enable	Up	0	Enable	Enable	0
OSPI0_D2	OSPI0_D2	Enable	Up	0	Enable	Enable	0
OSPI0_D3	OSPI0_D3	Enable	Up	0	Enable	Enable	0
OSPI0_CSn0(1)	OSPI0_CSn0	Enable	Up	0	Disable	Enable	0
OSPI0_CSn1(1)	OSPI0_CSn1	Enable	Up	0	Disable	Enable	0
OSPI0_CSn2(1)	OSPI0_CSn2	Enable	Up	0	Disable	Enable	0
OSPI0_CSn3(1)	OSPI0_CSn3	Enable	Up	0	Disable	Enable	0

(1) OSPI0_CSn0, OSPI0_CSn1, OSPI0_CSn2 and OSPI0_CSn3 are configured as chip select outputs from the OSPI0 host controller, but QSPI boot only provides the option of selecting OSPI0_CSn0 or OSPI0_CSn1 via BOOTMODE[7]. It is not possible to select OSPI0_CSn2 or OSPI0_CSn3 as a chip select option for QSPI boot.

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

4.4.1.3.1 QSPI Bootloader Operation

The QSPI boot mode supports the 1S-1S-4S mode only (Bit-width =1 or 4, Single Data Rate). The Command and Address issued are 8 bits and 24 bits respectively. The Read Command that is issued for QSPI is 0x6b followed by zero for address and 8 dummy cycles. The frequency of operation supported is 50 MHz.

4.4.1.3.1.1 QSPI Initialization Process

In the QSPI boot mode, the ROM Code initializes the OSPI module and the image is read from the QSPI flash connected to the selected chip-select. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM. See Section 4.4.1.3 , *QSPI Boot Device Configuration* for OSPI port settings.

A detailed summary of the QSPI boot parameter table and the boot configuration definitions are listed in Section 4.6.3 , *QSPI Boot Parameter Table*.

4.4.1.3.1.2 QSPI Loading Process

QSPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

4.4.1.4 SPI Boot

Refer to Section 4.4.1 section for more information about all SPI boot modes.

Table 4-12 shows configuration pins assignment to functions when boot mode is SPI using the OSPI module.

Table 4-12. SPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8	Mode	0	SPI Mode 0
		1	SPI Mode 3
7	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 4-13 summarizes the OSPI pin configuration done by ROM code for SPI boot device on port 0.

Table 4-13. SPI Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
OSPI0_CLK	OSPI0_CLK	Disable	Up	0	Disable	Enable	0
OSPI0_LBCLKO	OSPI0_LBCLKO	Disable	Up	0	Enable	Enable	0
OSPI0_DQS	OSPI0_DQS	Disable	Up	0	Enable	Disable	0
OSPI0_D0	OSPI0_D0	Enable	Up	0	Enable	Enable	0
OSPI0_D1	OSPI0_D1	Enable	Up	0	Enable	Enable	0
OSPI0_CSn0(1)	OSPI0_CSn0	Enable	Up	0	Disable	Enable	0
OSPI0_CSn1(1)	OSPI0_CSn1	Enable	Up	0	Disable	Enable	0
OSPI0_CSn2(1)	OSPI0_CSn2	Enable	Up	0	Disable	Enable	0
OSPI0_CSn3(1)	OSPI0_CSn3	Enable	Up	0	Disable	Enable	0

(1) OSPI0_CSn0, OSPI0_CSn1, OSPI0_CSn2 and OSPI0_CSn3 are configured as chip select outputs from the OSPI0 host controller, but SPI boot only provides the option of selecting OSPI0_CSn0 or OSPI0_CSn1 via BOOTMODE[7]. It is not possible to select OSPI0_CSn2 or OSPI0_CSn3 as a chip select option for SPI boot.

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

4.4.1.4.1 SPI Bootloader Operation

The SPI boot mode supports the 1S-1S-1S mode only (Bit-width =1, Single Data Rate). OSPI0_D0 will have data transfers **FROM** the processor **TO** the flash device, and OSPI0_D1 will have data transfers **TO** the processor **FROM** the flash device. The Command and Address issued are 8 bits and 24 bits respectively. The Read Command that is issued for SPI is 0x03. There are no dummy cycles issued after the read command. The frequency of operation supported is 6.250 MHz.

4.4.1.4.1.1 SPI Initialization Process

In the SPI boot mode, the ROM Code initializes the OSPI peripheral to SPI mode and the image is read from the flash memory connected to the corresponding OSPI port and chip-select. A detailed summary of the SPI boot parameter table and the boot configuration definitions are listed in Section 4.6.3 , *OSPI/QSPI/SPI Boot Parameter Table*. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM.

4.4.1.4.1.2 SPI Loading Process

SPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

4.4.2 I2C Boot

Table 4-14 shows configuration pins assignment to functions when boot mode is the I2C mode.

Table 4-14. I2C Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	Bus reset	0	Hung bus reset attempt after 1 ms
		1	No hung bus reset attempted
7	Address	0	EEPROM's address is 0x50
		1	EEPROM's address is 0x51

The I^2C bus is considered inactive if the data line is low and clock remains high for the specified timeout time. Recovery consists of driving the clock a stop condition is detected. A stop condition is a transition on the data line from 0 to 1 while the clock line is high. If the clock line is stuck low there is no way to take control of the bus.

Table 4-15 summarizes the I2C pin configuration done by ROM code for I^2C boot device.

Table 4-15. I2C Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
I2C0_SCL	I2C0_SCL	Enable	Up	0	Enable	Enable	0
I2C0_SDA	I2C0_SDA	Enable	Up	0	Enable	Enable	0

4.4.2.1 I2C Bootloader Operation

4.4.2.1.1 I2C Initialization Process

In the I2C boot mode, the ROM Code configures the Main Domain I2C0 in controller mode.

The boot controller drives the I^2C target device where the image is stored. The image is copied to internal RAM, and is executed from there. If the image is not recognized, the ROM will attempt to read the image at offset 0x8000. This is the only redundant image supported by the ROM.

A detailed summary of the I^2C boot parameter table and the BOOTMODE pins definitions are listed in Section 4.6.6 , *I2C Boot Parameter Table* and Section 4.4.2 , *I2C Boot Device Configuration*.

4.4.2.1.1.1 Block Size

ROM code will read 0x800 bytes before processing the data. The last block must be padded to the next 0x800 byte boundary and it must be padded with zeros.

4.4.2.1.1.2 Addressing

The boot code does not support byte address to bus address wrapping. So the maximum image size that can be access is 64 kbytes. For example, if the read address is 0xFF00, the read size is 0x200 and the I^2C bus address is 0x50, then 0x100 bytes will be read from 0xFF00 at bus address 0x50, followed by 0x100 bytes from 0x0000 at bus address 0x50. The bus address does not increment when the address rolls over.

4.4.2.1.2 I2C Loading Process

4.4.2.1.2.1 Loading a Boot Image From EEPROM

In this mode, the Main Domain I2C0 peripheral is configured as I^2C controller.

ROM Code will start reading from the I^2C EEPROM at the specified I^2C bus address. This read will be done beginning at the specified base address offset. Data will be read in 2-KB chunks. The data will be stored at the address specified in the boot header. It will continue reading image data until a complete image has been read. When the complete image has been read, the ROM Code will branch to the start address of the image.

4.4.3 SD Card Boot

Table 4-16 shows configuration pins assignment to functions when boot mode is the SD card mode.

Table 4-16. SD Card Boot Configuration Fields

SD Card Boot Configuration Fields			
BOOTMODE Pins	**Field**	**Value**	**Description**
9 (13[1])	Port	0	Reserved
		1	MMC Port 1 (4 bit width). This bit must be set to 1
7	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD is the backup mode.

Table 4-17 summarizes the MMCSD pin configuration done by ROM code for SD Card boot device on port1 (MMCSD1). SD Card boot on Port 0 (MMCSD0) is not supported.

Table 4-17. SD Card (MMCSD1) Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
MMC1_DAT3	MMC1_DAT3	Disable	NA	0	Enable	Enable	0
MMC1_DAT2	MMC1_DAT2	Disable	NA	0	Enable	Enable	0
MMC1_DAT1	MMC1_DAT1	Disable	NA	0	Enable	Enable	0
MMC1_DAT0	MMC1_DAT0	Disable	NA	0	Enable	Enable	0
MMC1_CLK	MMC1_CLK	Disable	NA	0	Disable	Enable	0
MMC1_CLKLB	MMC1_CLKLB	Disable	NA	0	Disable	Enable	0
MMC1_CMD	MMC1_CMD	Disable	NA	0	Enable	Enable	0
MMC1_SDCD	MMC1_SDCD	Disable	NA	0	Enable	Disable	0

Note

MMC1_CLKLB signal is not pinned out on the device. The pinmux configuration enables the input buffer of the internal loopback clock.

Note

MMC1_SDWP is not configured by ROM since the ROM never writes to the SD card.

4.4.3.1 SD Card Bootloader Operation

SD Card boot is only available on Port 1 of the MMCSD controller (MMCSD1). The IOs on this port support both 1.8V and 3.3V operation, as well as dynamic voltage change. Thus, this port can support initial operation at 3.3V and remain at this voltage for legacy SD Cards, or support initial operation at 3.3V and change to 1.8V after ROM boot for UHS-I SD Cards.

The ROM will boot from SD cards using one of these methods:

- User Data Area (UDA) in raw mode
- User Data Area (UDA) in filesystem mode

The ROM is capable of booting from any size SD card because the MMCSD controller is responsible for addressing. Only single data rate with backward compatible interface timing is supported.

The MMCSD module depends on proper voltage level on the SD card detect signal (SDCD). If SDCD=1, the ROM will assume the card is not present and will fail the boot mode.The SDCD must be 0 for the ROM to continue to attempt to boot. Card detect using DAT3 is not supported. If the card is detected, the initial discovery phase is performed:

1. Send CMD 0. (GO IDLE, both for MMC and SD)
2. Send CMD 55. If the card responds then the card type is assumed to be SD. On timeout the code sends CMD 1. If there is a response then the card type is MMC.

The ROM Code will start reading from the MMCSD memory boot sector, or filesystem, as specified by the BOOTMODE pins. Only FAT32 and FAT16 formats are supported in filesystem mode. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. In RAW mode only, the ROM supports a redundant image at offset 0x400000 in case the initial image fails to be recognized. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

When SD Card boot is used as a backup boot option, only User Data Area (UDA) in filesystem mode is supported. Raw mode is not supported. Additionally, boot will only occur in 1-bit mode during backup booting.

4.4.4 eMMC Boot

eMMC Boot Configuration Fields (UDA mode) shows configuration pins assignment to functions when boot mode is the eMMC Boot using a UDA boot mode (BOOTMODE[6:3]=1000b). Note that eMMC Boot using alternate eMMC Boot (BOOTMODE[6:3]=1001b) does not have any extra bootmode configuration fields. See eMMC Bootloader Operation for more information.

Table 4-18. eMMC Boot Configuration Fields (UDA mode)

eMMC Boot Configuration Fields			
BOOTMODE Pins	**Field**	**Value**	**Description**
9 (13[1])	Port	0	MMCSD Port 0 (8 bit width). This bit must be set to 0
		1	Reserved
7	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD Boot is the backup mode.

Note that eMMC with MMCSD0 has no pin mux options, thus no pinmux configuration is necessary

4.4.4.1 eMMC Bootloader Operation

Booting from an eMMC device is only available on Port 0 of the MMCSD controller (MMCSD0). Booting from an eMMC device is not available on Port1 (MMCSD1). The IOs associated with MMCSD0 port only support 1.8V eMMC operation

The ROM will boot from eMMC devices using one of these methods:

- User Data Area (UDA) in raw mode
- User Data Area (UDA) in filesystem mode
- eMMC bootmode (alternate)

To boot from UDA in either raw or filesystem mode, choose bootmode "MMCSD Boot" (see Table 4-4).

A special alternate boot mode is available with eMMC devices which allows the ROM to boot from an image that is in a separate boot partition in the eMMC. To boot from this mode, choose "eMMC Boot" (see Table 4-4).

The ROM Code will start reading from the memory boot sector, filesystem, or boot partition as specified by the BOOTMODE pins. Only FAT32 and FAT16 formats are supported in filesystem mode. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. In RAW mode only, the ROM supports a redundant image at offset 0x400000 in case the initial image fails to be recognized. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

When eMMC boot is used as a backup boot option, only User Data Area (UDA) in filesystem mode is supported. Raw mode is not supported. Additionally, boot will only occur in 1-bit mode during backup booting.

4.4.4.2 eMMC Flash

To support eMMC boot mode across a device warm reset, eMMC flash has the following requirements:

1. The reset line must be connected to the eMMC flash input reset pin.
2. The eMMC flash ext_csd[162] RST_n_ENABLE must be set to the expected configuration for the warm-reset signal to propagate to the flash device for the boot process to succeed. Possible configurations are shown in Table 4-19.

Note

For warm_reset eMMC boot to function correctly, 0x1 must be written to RST_n_ENABLE in the ext_csd[162] Register. This will enable the RST_n signal.

Table 4-19. ext_csd[162] Register

Bit	Field	Type	Description
7:2	Reserved		Reserved
1:0	RST_n_ENABLE	R/W	0x0: RST_n signal is temporarily disabled (default) 0x1: RST_n signal is permanently enabled 0x2 RST_n signal is permanently disabled 0x3: Reserved

4.4.5 Ethernet Boot

Table 4-20 shows configuration pins assignment to functions when boot mode is the Ethernet RGMII mode.

Table 4-20. Ethernet RGMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	Clkout	0	25 MHz clock not generated on CLKOUT0
		1	25 MHz clock generated on CLKOUT0
8	Delay	0	Must be set to 0 for RGMII with internal Tx delay
		1	Reserved
7	Link info	0	MDIO PHY scan used for link parameters.
		1	Link parameters programmed by software

Table 4-21 shows configuration pins assignment to functions when boot mode is the Ethernet RMII mode.

Table 4-21. Ethernet RMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	Clkout	0	50 MHz clock not generated on CLKOUT0
		1	50 MHz clock generated on CLKOUT0
8	Clk src	0	External clock source for RMII_REF_CLK
		1	Internal clock source for RMII_REF_CLK
7	RMII	0	This bit must be set to 0
		1	Reserved

Table 4-22. Ethernet RMII Clocking

BOOTMODE Pin 9 (Clk out)	BOOTMODE Pin 8 (Clk src)	Description
0	0	50MHz external source to RMII_REF_CLK and to external Ethernet PHY input clock (CLKOUT0 is unused)
0	1	Not a valid configuration
1	0	CLKOUT0 is configured to 50MHz and connect to both RMII_REF_CLK and to external Ethernet PHY input clock
1	1	Not a valid configuration

Table 4-23 shows configuration pins assignment to functions when the backup boot mode Ethernet. The Interface configuration field chooses which interface will be used (RGMII or RMII)

Table 4-23. Ethernet Backup Boot Configuration Field

BOOTMODE Pins	Field	Value	Description
13	Interface	0	RGMII with internal Tx delay
		1	RMII with external clock source

Table 4-24 summarizes the RGMII pin configuration done by ROM code for Ethernet boot device on RGMII port.

Table 4-24. RGMII Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
PRG1_PRU1_GPO0	RGMII2_RD0	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO1	RGMII2_RD1	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO2	RGMII2_RD2	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO3	RGMII2_RD3	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO4	RGMII2_RX_CTL	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO6	RGMII2_RXC	Disable	Down	0	Enable	Disable	4

Table 4-24. RGMII Pin Usage (continued)

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
PRG1_PRU1_GPO11	RGMII2_TD0	Disable	Down	0	Disable	Enable	4
PRG1_PRU1_GPO12	RGMII2_TD1	Disable	Down	0	Disable	Disable	4
PRG1_PRU1_GPO13	RGMII2_TD2	Disable	Down	0	Disable	Disable	4
PRG1_PRU1_GPO14	RGMII2_TD3	Disable	Down	0	Disable	Disable	4
PRG1_PRU1_GPO15	RGMII2_TX_CTL	Disable	Down	0	Disable	Disable	4
PRG1_PRU1_GPO16	RGMII2_TXC	Disable	Down	0	Disable	Disable	4
PRG1_MDIO0_MDIO	MDIO0_MDIO	Enable	Up?	0	Enable	Enable	4
PRG1_MDIO0_MDC	MDIO0_MDC	Enable	Up?	0	Disable	Enable	4

Table 4-25 summarizes the RMII pin configuration done by ROM code for Ethernet boot device on RMII port.

Table 4-25. RMII Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
PRG1_PRU1_GPO4	RMII2_RX_ER	Disable	Down	0	Enable	Disable	5
PRG1_PRU0_GPO10	RMII_REF_CLK	Disable	Down	0	Enable	Disable	5
PRG1_PRU1_GPO0	RMII2_RXD0	Disable	Down	0	Enable	Disable	5
PRG1_PRU1_GPO1	RMII2_RXD1	Disable	Down	0	Enable	Disable	5
PRG1_PRU1_GPO11	RMII2_TXD0	Disable	Down	0	Disable	Enable	5
PRG1_PRU1_GPO12	RMII2_TXD1	Disable	Down	0	Disable	Enable	5
PRG1_PRU1_GPO15	RMII2_TX_EN	Disable	Down	0	Disable	Enable	5
PRG1_PRU1_GPO13	RMII2_CRS_DV	Disable	Down	0	Enable	Disable	5
PRG1_PRU0_GPO7(1)	CLKOUT0	Disable	Down	0	Disable	Enable	5
PRG1_MDIO0_MDIO	MDIO0_MDIO	Enable	Up	0	Enable	Enable	4
PRG1_MDIO0_MDC	MDIO0_MDC	Enable	Up	0	Disable	Enable	4

(1) Enabled when CLKOUT0 option is selected from boot pin selection.

4.4.5.1 Ethernet Bootloader Operation

4.4.5.1.1 Ethernet Initialization Process

When the device is set to boot through the Ethernet mode, the ROM Code configures the Ethernet module and the interface mode (RMII, RGMII) according the the BOOTMODE pin settings, see Section 4.4.5 , *Ethernet Boot Device Configuration*. Also consult the boot parameter table for the Ethernet boot, see Section 4.6.8 , *Ethernet Boot Parameter Table*.

When Link Info = 0, the link parameters are read using MDIO scan. This is the typical setting when using an external PHY. When Link Info = 1, no MDIO scan is performed, and the link parameters are programmed by the ROM based on the RGMII status register.

Note that booting from RGMII requires that an attached PHY be configured for RGMII-ID Mode immediately upon exiting reset. The ROM will not make this configuration change to the PHY.

4.4.5.1.2 Ethernet Loading Process

After device configuration, the bootloader performs a standard BOOTP/TFTP boot. The device sends a BOOTP request with its MAC address to a host TFTP server to be assigned an IP from a pool of addresses. The timeout for each BOOTP packet is 4 seconds, and the ROM will attempt 10 BOOTP retries, after which the boot mode will fail. If the connection is established, the device initiates a TFTP download and is able to receive image data encapsulated in Ethernet packets, see Section 4.4.5.1.2.1 . There is a timeout of 1 second to receive a response for the READ request, and the ROM will retry the READ request 10 times, after which the boot mode will fail. If TFTP download is successful, data received is stripped of its network headers and the boot data is stored in internal RAM. When the transfer completes and the image is found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

4.4.5.1.2.1 Ethernet Boot Data Formats

Ethernet boot uses the BOOTP/TFTP protocol for downloads. Only IPv4 is supported.

4.4.5.1.2.1.1 Limitations

- Received packets cannot be IP fragmented (should not be a problem in most systems since the BOOTP/TFTP packets have fixed lengths of small size)
- Only DIX Ethernet headers are supported.
  - 802.3 with SNAP/LLC not supported
  - DIX Ethernet with VLAN not supported
  - 802.3 with VLAN and SNAP/LLC not supported

4.4.5.1.2.1.2 BOOTP Request

4.4.5.1.2.1.2.1 MAC Header (DIX)

- Destination MAC = value from parameter table (default is broadcast)
- Source MAC = value from parameter table (default is e-fuse value)
- Type = IPv4 (0x0800)

4.4.5.1.2.1.2.2 IPv4 Header

- Version = 4
- Header length = 0
- TOS = 0
- Len = computed during operation
- ID = 0x0001
- Flags + Fragment offset = 0
- TTL = 0x10
- Protocol = UDP (17)
- Header checksum = Computed during operation
- SRC IP = 0.0.0.0
- Dest IP = 255.255.255.255

4.4.5.1.2.1.2.3 UDP Header

- Source port = BOOTP client (68 decimal)
- Destination Port = BOOTP server (67 decimal)
- Length = computed during operation
- Checksum = computed during operation

4.4.5.1.2.1.2.4 BOOTP Payload

- Opcode = Request (1)
- HW Type = Ethernet (1)
- HW Addr Len = 6
- Hop Count = 0
- Transaction ID = 1
- Number of seconds = 0
- Client IP = 0.0.0.0
- Your IP = 0.0.0.0
- Server IP = 0.0.0.0
- Gateway IP = 0.0.0.0
- Client HW Address = Device MAC address (from parameter table)
- Server hostname = NULL

- Filename = NULL
- Option 60, Vendor ID string, from parameter table
- Option 61, Client ID string, from parameter table

4.4.5.1.2.1.2.5 TFTP

There are no ROM code specific TFTP configurations.

4.4.5.1.3 Ethernet Hand Over Process

Once the ROM Code receives the valid packet, it decodes it to get the image sections and loads them in the appropriate memory location. After the image is loaded and validated, the ROM Code starts the boot image execution.

4.4.6 USB Boot

Table 4-26 shows configuration pins assignment to functions when boot mode is the USB mode.

Table 4-26. USB Boot Configuration Fields

USB Configuration Fields for Primary Boot Mode			
BOOTMODE Pins	**Field**	**Value**	**Description**
8 (13[1])	Mode	0	DFU (USB device firmware upgrade)
		1	Host (MSC boot)
7	Lane Swap	0	D+/D- lines are not swapped
		1	D+/D- lines are swapped

(1) When USB is the backup mode.

Table 4-27 summarizes the USB pin configuration done by ROM code for USB boot device on port 0.

Table 4-27. USB Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
USB0_DRVVBUS	USB0_DRVVBUS	Enable	Down	0	Disable	Enable	0

Note

Note that other USB pins do not have pin mux options. USB_DRVVBUS is configured in DFU mode even though it is not used.

Note on USB backup boot

- Lane Swap (D+/D- lines) are not allowed

Configurability (pins) of these options do not exist in the USB backup boot mode.

4.4.6.1 USB Bootloader Operation

The USB boot mode is used to read the boot image from external USB host.

See Section 4.4.6 , *USB Boot Device Configuration* and Section 4.6.11 , *USB Boot Parameter Table* for the available configuration options.

More information about USB DFU protocol can be found at http://www.usb.org/sites/default/files/DFU_1.1.pdf.

In DFU mode, the ROM will attempt an enumeration for 60 seconds, after which the boot mode will fail. If a successful enumeration is achieved, the ROM Code will start reading from the external host as specified by the BOOTMODE pins. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

4.4.6.1.1 USB-Specific Attributes

4.4.6.1.1.1 DFU Device Mode

- Vendor ID = 0x451
- Product ID = 0x6165
- Device ID = 0

4.4.6.2 Limitations for USB DFU and PCIe boot modes

In USB DFU and PCIe boot modes, the boot image is processed in image mode, meaning that the image is entirely loaded in internal RAM at address 0x70001000 before the certificate is validated.

This introduces two limitations compared to the other boot modes:

1. Once the image is validated, it needs to be relocated by the DMSC to its final location to be ready for execution. Since the source and destination for the copy are both in internal RAM, the user needs to ensure the reloaction address is either in a lower address (0x70000000-0x71000000) or in a higher address beyond the end of the image (0x71000000 + size of image). If this is not followed, the image relocation will corrupt itself while copying, resulting in a boot failure. The relocation address is defined in the certificate.
2. Because the downloaded image is at offset 0x70001000 it also means that both DFU and PCIe maximum image size are 4Kbytes less than with the other boot mode.

4.4.7 PCIe Boot

Table 4-28 shows configuration pins assignment to functions when boot mode is the PCIe mode.

Table 4-28. PCIe Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
7	Clocking	0	PHY clock from external pins
		1	PHY clock from internal source

Table 4-29. PCIe Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
UART1_CTSn	PCIE0_CLKREQn	Enable	Down	0	Enable	Enable	3

Note

Note that PCIe (SERDES) pins do not have pin mux options.

4.4.7.1 PCIe Bootloader Operation

4.4.7.1.1 PCIe Initialization Process

In the PCIe boot mode, the ROM Code configures the PCIe and SerDes from information it obtains from the boot parameter table, see Section 4.6.5 , *PCIe Boot Parameter Table*

Table 4-30. PCIe Configuration Fields

Field	Value	Description
Physical Port	0	Single port available
Lanes (Bus width)	Single	No of PCIe lanes configurable
Line rate	5000Mbps	Gen2 only available
No of BARs	6	BAR0 to BAR5
BAR configuration		BAR 0 • 32 bit memory not prefetchable • 1MByte PCIe controller register access BAR1 • 32 bit memory prefetchable • 2MByte Internal memory where the image needs to be copied to BAR 2 • 64 bit memory prefetchable • Same as BAR1 but for 64 bit access • Size requested to RC is 32MB BAR 3 – • Used along with BAR2 to represent 64bit size BAR 4 • Same as BAR 2 BAR 5 - • Used along with BAR4 to represent 64bit size
Internal Resource mapped to BARs	internal RAM	2MB
iATU register access by remote Root complex	Yes	1MB

Table 4-30. PCIe Configuration Fields (continued)

Field	Value	Description
How could Vendor and Device ID change	By programming efuse registers	See CTRLMMR_PCI_DEVICE_IDx registers

4.4.7.1.2 PCIe Loading Process

PCIe boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

The image copied should be within the first 0x180000 bytes of the area. Once the Root Complex has finished copying the image, then it needs to write the PCIe boot data address to 0x701BCFE0

For example, if the Root Complex loads the image at offset 0x1000, then when it is done it would write 0x70001000 (Internal RAM memory base + offset) to 0x701BCFE0. This will let the ROM know that this image is ready to be authenticated and processed.

4.4.7.2 Limitations for USB DFU and PCIe boot modes

In USB DFU and PCIe boot modes, the boot image is processed in image mode, meaning that the image is entirely loaded in internal RAM at address 0x70001000 before the certificate is validated.

This introduces two limitations compared to the other boot modes:

1. Once the image is validated, it needs to be relocated by the DMSC to its final location to be ready for execution. Since the source and destination for the copy are both in internal RAM, the user needs to ensure the reloaction address is either in a lower address (0x70000000-0x71000000) or in a higher address beyond the end of the image (0x71000000 + size of image). If this is not followed, the image relocation will corrupt itself while copying, resulting in a boot failure. The relocation address is defined in the certificate.
2. Because the downloaded image is at offset 0x70001000 it also means that both DFU and PCIe maximum image size are 4Kbytes less than with the other boot mode.

4.4.8 UART Boot

ROM Code always configures the UART port to 115200 kbaud, 8-n-1 mode, and the XMODEM protocol is used to transfer the boot data.

Table 4-31 summarizes the UART pin configuration done by ROM code for UART host on port 0.

Table 4-31. UART Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
UART0_TXD	UART0_TXD	Enable	Up	0	Disable	Enable	0
UART0_RXD	UART0_RXD	Enable	Up	0	Enable	Disable	0

CAUTION

It is possible for ROM code execution to hang during UART boot. See advisory i2371 in SPRZ457.

4.4.8.1 UART Bootloader Operation

4.4.8.1.1 Initialization Process

In the UART boot mode, the selected UART module (port) is the only peripheral configured. The baud rate, data, parity, and stop bits are configured based on the information in the UART boot parameter table. The boot parameter table definitions and the boot configuration values that can be set are in Section 4.4.8 , *UART Boot Device Configuration* and Section 4.6.4 , *UART Boot Parameter Table*.

Once the ROM Code configures the UART, it sends the UART pings for few seconds, which can be seen in the host. The pings consist of an ASCII capital *C* character. The UART boot mode supports only the CRC mode of XMODEM and does not support CHECKSUM mode. Both 128 and 1024 byte block sizes are supported.

4.4.8.1.2 UART Loading Process

Before the ping from the device stops, load the boot image from the host using the XMODEM protocol.

4.4.8.1.2.1 UART XMODEM

The XMODEM protocol is used to transfer boot data. Only CRC mode is supported (not checksum), with both 128- and 1024-byte block sizes. The general, format of received frames is shown in Table 4-32 and Table 4-33.

Table 4-32. XMODEM 1024- and 128-byte Data Frames

STX	Block Num	Inv Block Num	1024 data bytes	CRC	CRC
SOH	Block Num	Inv Block Num	128 data bytes	CRC	CRC

Table 4-33. XMODEM Data Frame Fields

Field	Value	Description
STX	0x02	The start character for 1024-byte CRC data blocks
SOH	0x01	The start character for 128-byte CRC data block
Block Num	0x01-0xFF – 0x00	The block number. The first block has value 1, and the block number wraps around 0xFF to 0
Inv Block Num	0xFE-0x00	The inverse block number (bit inverse of the block number)
CRC	Calculated	The 16-bit CRC generated from the polynomial 0x1021

The XMODEM protocol is implemented as a half-duplex protocol as shown in Table 4-34.

Table 4-34. Example of XMODEM Transfer protocol

Transmitter Sends		Receiver Sends
	←	Ping (‘C’)
Frame 1	→	

Table 4-34. Example of XMODEM Transfer protocol (continued)

Transmitter Sends		Receiver Sends
	←	ACK (or NACK)
Frame 2	→	
	←	ACK (or NACK)
EOT	→	
	←	ACK (or NACK)

4.4.8.1.3 UART Hand-Over Process

Once the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

4.4.9 GPMC NOR Boot

GPMC NOR Boot Configuration Fields

AM64x ROM GPMC NOR boot only supports 16-bit non-mux memory.

GPMC NOR Boot non-muxed Pin Usage

This table summarizes the GPMC pin configuration done by ROM code for GPMC NOR boot.

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
GPMC0_AD0	GPMC0_AD0	Disable	Down	0	Enable	Enable	0
GPMC0_AD1	GPMC0_AD1	Disable	Down	0	Enable	Enable	0
GPMC0_AD2	GPMC0_AD2	Disable	Down	0	Enable	Enable	0
GPMC0_AD3	GPMC0_AD3	Disable	Down	0	Enable	Enable	0
GPMC0_AD4	GPMC0_AD4	Disable	Down	0	Enable	Enable	0
GPMC0_AD5	GPMC0_AD5	Disable	Down	0	Enable	Enable	0
GPMC0_AD6	GPMC0_AD6	Disable	Down	0	Enable	Enable	0
GPMC0_AD7	GPMC0_AD7	Disable	Down	0	Enable	Enable	0
GPMC0_AD8	GPMC0_AD8	Disable	Down	0	Enable	Enable	0
GPMC0_AD9	GPMC0_AD9	Disable	Down	0	Enable	Enable	0
GPMC0_AD10	GPMC0_AD10	Disable	Down	0	Enable	Enable	0
GPMC0_AD11	GPMC0_AD11	Disable	Down	0	Enable	Enable	0
GPMC0_AD12	GPMC0_AD12	Disable	Down	0	Enable	Enable	0
GPMC0_AD13	GPMC0_AD13	Disable	Down	0	Enable	Enable	0
GPMC0_AD14	GPMC0_AD14	Disable	Down	0	Enable	Enable	0
GPMC0_AD15	GPMC0_AD15	Disable	Down	0	Enable	Enable	0
PRG1_PRU0_GPO17	GPMC_A0	Disable	Down	0	Disable	Enable	8
PRG1_PRU0_GPO18	GPMC_A1	Disable	Down	0	Disable	Enable	8
PRG1_PRU0_GPO19	GPMC_A2	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO0	GPMC_A3	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO1	GPMC_A4	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO2	GPMC_A5	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO3	GPMC_A6	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO4	GPMC_A7	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO5	GPMC_A8	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO6	GPMC_A9	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO7	GPMC_A10	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO8	GPMC_A11	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO9	GPMC_A12	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO10	GPMC_A13	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO11	GPMC_A14	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO12	GPMC_A15	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO13	GPMC_A16	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO14	GPMC_A17	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO15	GPMC_A18	Disable	Down	0	Disable	Enable	8
PRG1_PRU1_GPO16	GPMC_A19	Disable	Down	0	Disable	Enable	4
GPMC0_CSn3	GPMC_A20	Disable	Down	0	Disable	Enable	0

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
GPMC0_ADVn_ALE	GPMC0_ADVn_ALE	Disable	Up	0	Disable	Enable	0
GPMC0_OEn_REN	GPMC0_OEn_Ren	Disable	Up	0	Disable	Enable	0
GPMC0_WEN	GPMC0_WEN	Disable	Up	0	Disable	Enable	0
GPMC0_BE0n_CLE	GPMC0_BEOn_CLE	Disable	Up	0	Disable	Enable	0
GPMC0_BE1n	GPMC0_BE1n	Disable	Up	0	Disable	Enable	0
GPMC_WAIT0	GPMC_WAIT0	Enable	Up	0	Enable	Disable	0
GPMC_WAIT1	GPMC_WAIT1	Enable	Down	0	Enable	Disable	0
GPMC0_WPn	GPMC0_WPn	Disable	Down	0	Disable	Enable	0
GPMC0_DIR	GPMC0_DIR	Disable	Up	0	Disable	Enable	0
GPMC0_CSn0	GPMC0_CSn0	Enable	Up	0	Disable	Enable	0
GPMC0_CSn1	GPMC0_CSn1	Enable	Up	0	Disable	Enable	0
GPMC0_CSn2	GPMC0_CSn2	Enable	Up	0	Disable	Enable	0

Note

Only 21 address lines (GPMC0_A0 – GPMC0_A20) are used because the GPMC0_A21 and GPMC0_A22 lines are muxed with GPMC0_WAIT1 and GPMC0_WPn respectively.

GPMC0_A20 is muxed with GPMC0_CSn3, and ROM uses GPMC0_A20 for this address line, and thus no CSn3 support for GPMC boot.

All signals in the table will be configured even though some may not be used by this particular boot mode.

4.4.9.1 GPMC NOR Bootloader Operation

4.4.9.1.1 GPMC NOR Initialization Process

In this mode, the ROM Code configures the GPMC interface based on the configuration parameters specified in the boot parameter table for the GPMC NOR boot mode. The boot parameter structure definition for the GPMC NOR boot mode and the parts of this table that can be configured by the BOOTMODE pins are detailed in Section 4.4.9 , *GPMC NOR Boot Device Configuration*.

4.4.9.1.2 GPMC NOR Loading Process

GPMC NOR boot mode is not executable-in-place (XIP). ROM code first copies boot image into on-chip RAM and then executes it. If the initial image at offset 0x0 is not recognized, the ROM will attempt to read a redundant image from offset 0x100000. This is the only redundant image supported by the ROM.

4.4.10 GPMC NAND Boot

GPMC NAND Boot Configuration Fields

AM64x ROM only supports boot from ONFI 1.0 compatible 8 bit parallel NAND memory up to 2Gbytes in size connected to GPMC CS0 with the following geometries:

- 2Kbyte page and spare area of at least 64 bytes or
- 4Kbyte page size and spare area of at least 128 bytes.

GPMC NAND Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
GPMC0_AD0	GPMC0_AD0	Disable	Down	0	Enable	Enable	0
GPMC0_AD1	GPMC0_AD1	Disable	Down	0	Enable	Enable	0

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
GPMC0_AD2	GPMC0_AD2	Disable	Down	0	Enable	Enable	0
GPMC0_AD3	GPMC0_AD3	Disable	Down	0	Enable	Enable	0
GPMC0_AD4	GPMC0_AD4	Disable	Down	0	Enable	Enable	0
GPMC0_AD5	GPMC0_AD5	Disable	Down	0	Enable	Enable	0
GPMC0_AD6	GPMC0_AD6	Disable	Down	0	Enable	Enable	0
GPMC0_AD7	GPMC0_AD7	Disable	Down	0	Enable	Enable	0
GPMC0_ADVn_ALE	GPMC0_ADVn_ALE	Disable	Up	0	Disable	Enable	0
GPMC0_OEn_Ren	GPMC0_OEn_Ren	Disable	Up	0	Disable	Enable	0
GPMC0_Wen	GPMC0_Wen	Disable	Up	0	Disable	Enable	0
GPMC0_BEOn_CLE	GPMC0_BEOn_CLE	Disable	Up	0	Disable	Enable	0
GPMC_WAIT0	GPMC_WAIT0	Enable	Up	0	Enable	Disable	0
GPMC0_WPn	GPMC0_WPn	Disable	Down	0	Disable	Enable	0
GPMC0_CSn0	GPMC0_CSn0	Enable	Up	0	Disable	Enable	0

4.4.10.1 GPMC NAND Bootloader Operation

4.4.11 No boot/Development boot

Table 4-35 shows configuration pins assignment to functions when boot mode is the No-boot mode.

Table 4-35. No-boot/Dev-boot Configuration Fields

Field	Value	Description
No/Dev	0	Development Boot
	1	No boot

These boot modes are useful for debugging purposes to preclude the execution of the ROM.

During the Development boot (BOOTMODE[7] = 0), the DMSC ROM code will act as if boot of the primary image has completed, and the DMSC ROM then will be waiting for a firmware load message from MCU R5. Thus the user can load a standard u-boot/SPL image to the R5 RAM. U-boot/SPL will then load the DMSC firmware and complete the full boot.

In No-boot (BOOTMODE[7] = 1), both the DMSC and MCU R5 ROMs are bypassed and both CPUs are held in a dummy branch-to-self loop. No-boot is the most minimal device touch state by the ROM - only minimal hardware configurations are done and none of the PLLs is locked/configured. No-boot is suitable if user wants to load his own PLL, Pad config, and other basic settings.

4.5 PLL Configuration

ROM code must be aware of the reference clock provided to PLLs. That is, the speed of the quartz crystal, or the clock supplied by an external clock oscillator. On how to indicate the PLL reference clock, see PLL Reference Clock Selection

ROM code configures only PLLs which are required during boot. Therefore, if a PLL is required for the backup boot mode but not the primary boot mode, and if the backup boot mode never executes, then the PLLs required for backup boot are not enabled.

The following tables show the HSDIV values that are programmed by the R5 ROM if a boot mode uses it. A value of NA means that the ROM does not program that HSDIV

Table 4-36. MAIN_PLL0 (MAIN PLL) (2000MHz)

PLL POSTDIV	HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
0	HSDIV0	4	500	MAIN SYSCLK0
0	HSDIV1	10	200	OSPI
0	HSDIV2	NA	NA	NA
0	HSDIV3	15	133	GPMC NOR/GPMC NAND
0	HSDIV4	8	250	CP_GEMAC(Ethernet)
1	HSDIV5	5	200	eMMC0
1	HSDIV6	NA	NA	NA
1	HSDIV7	4	250	DMTimer
1	HSDIV8	10	100	SERDES
1	HSDIV9	NA	NA	NA

Table 4-37. MAIN_PLL1 (PER0 PLL) (1920MHz)

PLL POSTDIV	HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
0	HSDIV0	10	192	UART
0	HSDIV1	12	160	UART
0	HSDIV2	5	384	SA2UL
0	HSDIV3	NA	NA	NA
0	HSDIV4	80	24	USB
1	HSDIV5	6	160	OSPI
1	HSDIV6	NA	NA	NA

Table 4-38. MAIN_PLL14 (PULSAR PLL) (2400MHz)

HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
HSDIV0	3	800	R5F cores

Note

All other PLLs are not used or programmed by the ROM

Note

The bringup and configuration of bootmode-specific PLLs by ROM code will result in a bootmode-specific device clocking setup which for example has an impact on which peripheral modules can readily be clocked and used by SBL/SPL prior to loading and bringing up System Firmware (SYSFW)

4.6 Boot Parameter Tables

The boot parameter tables direct the main module boot process. On cold boot the tables are created based on pin strapped values (see Section 4.3 , *Boot Mode Pins*) and built-in data. The ROM Code supports two parameter tables stored as an array in a fixed memory address in the MSRAM, each of size 512 bytes. The ROM will attempt to boot using the primary table. On boot failure, ROM Code will retry using the second table.

Using two tables handles two cases.

- The first is in initial board manufacture where the primary boot table specifies boot from a flash device, and the flash is blank. ROM Code would then switch to the secondary boot mode which would receive the image externally (Ethernet, USB, PCIe, UART) and this image would flash the boot image.
- The second case is failure due to total flash corruption. In flash parameter tables, there exists backup addresses within the primary boot mode. This covers the problem of a flash update failure with a backup image present on the same flash device. Note for SD Card/eMMC boot, the backup addresses are only applicable in raw boot mode

The boot tables reside at a fixed location in memory which is described in Section 4.8.2 , *Global Memory Addresses Used by ROM Code*.

4.6.1 Common Header

These boot parameter tables have certain parameters common across all the boot modes, while the rest of the parameters are unique to the boot modes. The common entries in the boot parameter table are shown in Table 4-39.

Table 4-39. Boot Parameter Table Common Header

Byte Offset	Size (bytes)	Name	Description
0	2	Length	The length of the table
2	2	Checksum	Ones complement checksum over length bytes in the table. If 0 the checksum is not validated.
4	2	Peripheral	Identifies the boot peripheral and format of the table after the common header. See Table 4-40
6	2	Reserved	Reserved
8	4	Timeout	Timeout for this boot mode, in milliseconds
12	4	Magic	Magic value 0x01AD0911
16	40	PLL Config 0	PLL Configuration 0. See Table 4-41
56	40	PLL Config 1	PLL Configuration 1
96	40	PLL Config 2	PLL Configuraiton 2
136	40	PLL Config 3	PLL Configuration 3
176	40	PLL Config 4	PLL Configuration 4
216	40	PLL Config 5	PLL Configuration 5

Table 4-40 lists the possible boot modes used in the boot parameter tables.

Table 4-40. Boot Peripheral Selection

Peripheral Field Value	Description
0	Sleep (No boot)
10	Ethernet Reserved
20	Ethernet BOOTP/TFTP (general)
21	Ethernet RGMII specific
22	Ethernet RMII specific
30	PCIe
31	PCIe 1-lane
32	PCIe 2-lane

Table 4-40. Boot Peripheral Selection (continued)

Peripheral Field Value	Description
40	I2C
50	SPI
60	UART
70	USB DFU
71	USB Reserved
72	USB Host MSC
80	QSPI
85	OSPI
90	Reserved
100	MMCSD Card (general)
101	eMMC (general)
102	MMC 1-bit
103	MMC 4-bit
104	MMC 8-bit
110	GPMC NOR
120	Reserved
130	xSPI
140	GPMC NAND

4.6.2 PLL Setup

Table 4-41 through Table 4-45 describe the PLL configuration fields.

Table 4-41. Boot Parameter Table PLL Configuration

Byte Offset	Size (bytes)	Name	Description
0	1	Domain/cfg	See Table 4-42
1	1	Pll number	PLL number indexed from 0.
2	1	Input source	See Table 4-44
3	1	Pll Type	This field must be 1 to indicate an SCPLL
4	4	Input Ref Clock	The PLL input clock, in Q16.16 format
8	4	Feed back divider, integer part	Integer value of feedback divider
12	4	Feed back divider, fractional part	Fractional portion of feedback divider. Total divider is the Integer part + (Fractional part / 2^{24})
16	1	Ref divider	Input clock pre-divider
17	1	Post divider 1	Output post divider 1
18	1	Post divider 2	Output post divider 2
19	1	Reserved	Reserved
20	2	Hsdiv Enable	Bit map. A set bit indicates that the corresponding hsdiv is enabled.
22	2	Reserved	Reserved
24	16	Hsdiv[16]	Array of hs divider values.

Table 4-42. PLL Domain and Enable Configuration

7	6	5	4	3	2	1	0
Reserved		Enable		Reserved			Domain

Table 4-43. PLL Domain and Enable Field Description

Field	Value	Description
Enable	0	PLL not configured

Table 4-43. PLL Domain and Enable Field Description (continued)

Field	Value	Description
	1	PLL enabled only if currently disabled or in bypass
	2	PLL is unconditionally enabled. If currently enabled with a different configuration the PLL is first disabled
	3	PLL is unconditionally disabled
Domain	0	PLL is in the MCU domain
	1	PLL is in the MAIN domain

Table 4-44. PLL Reference Source Bit Fields

7	6	5	4	3	2	1	0
Source Type				Source Index			

Table 4-45. PLL Reference Source Field Description

Field	Value	Description
Source Type	0	Source is HFOSC
	1	Source is external pin
	2	Reserved
	3-7	Reserved
Source Index	0-31	Source index (HFOSC[0-31] or pin[0-31], depending on Source Type) HFOSC[0] – WKUP_HFOSC0 HFOSC[1] – HFOSC1 (in MAIN domain) PIN[1] – EXT_REFCLK1 pin (not all PLLs, see *Clocking*

4.6.3 OSPI/QSPI/SPI Boot Parameter Table

Table 4-46 shows the boot parameter table for OSPI, QSPI, or SPI boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-46. OSPI/QSPI/SPI Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode on	From Pins	If non-zero, the mode byte will be sent
258	1	Instruct Width	From Pins	Number of pins used to send instructions (1, 2, 4, 8)
259	1	Address Width	From Pins	Number of pins used to send address (1, 2, 4, 8)
260	1	Data Width	From Pins	Number of pins used to received data (1, 2, 4, 8)
261	1	Address Size	24	24, and 32 bits are the valid address sizes
262	1	Mode	0	OSPI clock polarity and phase mode
263	1	CSEL	From Pins	Chip select number (0–3)
264	1	Read Cmd	From Pins	Command used to read read data
265	1	Mode byte	0	Value used for the mode byte (when active)
266	1	Dummy Cycles	From pins	Number of dummy cycles sent after the read command
267	1	clkRecovery	From pins	Clock recovery
268	1	dqsEnable	0	Enable DQS
269	1	Reserved	0	Reserved
270	2	Module Freq	0	The OSPI module frequency after PLL enable, in kHz. If 0, ROM code uses the value from the module clock tables.
272	4	Bus Frequency	From pins	The OSPI bus frequency, in kHz
276	4	Delay	0x08080808 or 0x01010101	The chip select read delays. Default value is based on the read command

Table 4-46. OSPI/QSPI/SPI Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
280	4	Tap Delay	0xFFFFFFFF	The read tap selection. If 0xFFFFFFFF, the ROM code will scan the taps to find the best delay. The result will then overwrite the value in this table.
284	4	Internal Clk	From pins	0 = external (dqs) 1 = internal
288	4	notDAC	From pins	When 0, DAC mode is used
292	4	Read Index	0	Index to the active read address (0-1)
296	4	Read Addr 0	0x000000	The initial flash read address
300	4	Read Addr 1	0x400000 (0x4000 SPI)	Backup read address
304	4	Reserved	0	Reserved
308	4	Reserved	0	Reserved

4.6.4 UART Boot Parameter Table

Table 4-47 shows the boot parameter table for UART boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-47. UART Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Magic	0x49	Required Magic value
257	1	Protocol	63 (0x3F)	Specifies the transfer protocol = XMODEM
258	2	Reserved	0	Reserved
260	1	Max error Count	10	Error count resulting in boot abort
261	1	Ack timeout	3	Timeout in seconds on ack
262	1	Char timeout	20	Inter-character timeout in milliseconds
263	1	Reserved	0	Reserved
264	4	Port	From Pins	Physical port number
268	4	Mod Ref Clk	48000	Module reference clock, in kHz
272	4	Data Rate	115200	Baud rate (bps)
276	1	Parity	0	0=none, 1=odd, 2=even
277	1	Data bits	8	Only 8 data bit width is supported
278	1	Stop bits	2	Stop bits in Q7.1 format (2 = 1 stop bit)
279	1	Flow Control	0	0=none, 1= RTS/CTS
280	1	Over sample	16	Only 16× and 13× oversample are supported
281	1	Magic 2	0xB7	Required magic value

4.6.5 PCIe Boot Parameter Table

Table 4-48 shows the boot parameter table for PCIe boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-48. PCIe Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	portNum	0	Physical port number
260	4	AddrWid	64	PCIe address width
264	4	LinkRate	5000	Link rate in MHz
268	4	RefClkkHz	100000	Serdes reference clock in kHz

Table 4-48. PCIe Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
272	4	Nlanes	1	Number of PCIe lanes configured (link width)
276	4	Rsvd	4	Reserved
280	4	Rsvd	256	Reserved
284	4	Rsvd	256	Reserved
288	4	Rsvd	0	Reserved
292	4	Rsvd	0	Reserved
296	4	Vendor ID	0x104C	PCIe Vendor ID value (read from control registers)
300	4	Device ID	0xB00D	PCIe Device ID value (read from control registers)
304	4	Class code/revision ID	0x04800001	PCIe class code and revision ID value
308	4	SerDes Clocking Mode	From Pin	0 = Received. 1 = Derived
312	4	SSC Enable	1	SSC is enabled in Derived Mode. SSC is disabled in Received Mode
316	4	RefSrc	2	SerDes reference clock source (SERDES0_CORE_REFCLK_SEL[1:0]

4.6.6 I2C Boot Parameter Table

Table 4-49 shows the boot parameter table for I2C boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-49. I2C Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode	From Pins	0x4E = I2C Controller, 0x72 = I2C target
258	1	Dev Addr	From Pins	I2C address when target mode (0x10 or 0x11)
259	1	Reserved	0	Reserved
260	4	Mod Clock	0	I2C Module input clock. If 0, it is computed by ROM code.
264	2	Bus Freq	400	I2C Controller mode bus frequency, in kHz
266	2	Bus Addr	From Pins	I2C Controller mode storage device's address (0x50 or 0x51)
268	2	Read Index	0	Index to the active read offset (0 or 1)
270	2	Read Offset 0	0x0000	I2C Controller mode read offset
272	2	Read Offset 1	0x8000	I2C Controller mode backup read offset
274	2	Reserved	0	Reserved
276	2	Reserved	0	Reserved
280	2	Busy Timeout	From pins	Number of µs before a bus recovery is attempted. In units of microseconds in Q3 number format. Value of 0 disables bus recovery attempts.

4.6.7 MMCSD/eMMC Boot Parameter Table

MMCSD/eMMC Boot Parameter Table shows the boot parameter table for eMMC, MMC or SD card boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-50. MMCSD/eMMC Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	From Pins	Physical port number
257	1	eMMC	From Pins	0 = SD/MMC, else eMMC

Table 4-50. MMCSD/eMMC Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
258	1	bootAck	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode the controller expects a boot ack from the eMMC
259	1	Media	1 for eMMC 0 for SD/MMC	0 = auto detect card type 1 = MMC 2 = SD
260	1	busWidth	8 for eMMC From Pins for SD/MMC	Number of data pins (1, 4, or 8). If 0, max supported pins of the port are used.
261	1	bootAlt	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode, the controller uses the alt boot method (CMD1 with arg 0xFFFF_FFFA) to initiate data transfer
262	1	sigVolt	0x18 for port0 0x33 for port1	Sets the signal voltage for the controller. 0x18 = 1.8V 0x33 = 3.3V
263	1	Reserved	0	Reserved
264	4	Max Bus Freq	0	Max bus frequency in kHz. If 0, the value is determined by reading the CSD register from the card (still maxes out at 25 MHz)
268	4	refClkkHz	0	Module reference clock frequency, in kHz. If 0, the ROM code computes the value.
272	4	respTimeout	40000	The timeout period on initial card read, in milli-seconds, Q3 number format
276	128	Filename	"\tiboot3.bin"	For SD/MMC, boot filename in 16-bit Unicode characters (max 64)
404	4	Mode	0x1144D091	0x1144D091 = file system boot 0x1144C180 = raw image boot
408	4	CardIsInit	0	0 = card not yet initialized 1 = card has been initialized
412	4	Rsvd	0	Reserved
416	4	RawIndex	0	Current active read offset (0 or 1)
420	4	Rsvd	0	Reserved
424	4	Raw Offset 0	0x000000	Raw read offset
428	4	Raw Offset 1	0x400000	Backup raw read offset
432	4	Rsvd	0	Reserved
436	4	Rsvd	0	Reserved

4.6.8 Ethernet Boot Parameter Table

Table 4-51 is shown segmented into four sections:

1. The first section contains information required to configure the device hardware
2. The second section contains information used by the top level Ethernet module to execute the boot
3. The third section contains information for the Ethernet stack code.
4. The fourth section contains information for creating the BOOTP packet (vendor string, ID string and debug string), and holds information returned in the BOOTP response (Default route and file name)

Table 4-51 shows the boot parameter table for Ethernet boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-51. Ethernet Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
Hardware Configuration Options				
256	2	Mod Freq	0	Module clock frequency, kHz. If 0, ROM code computes the value.
258	1	Port Num	0	Physical port number
259	1	Interface	From Pins	0 = RGMII with internal delay 1 = RGMII with external delay 2 = RMII
260	1	Init Level	0	0 = Initialize only not enabled modules 1 = Full ethernet sub-system initialization
261	1	Clock out enable	From pins	0x10 = CLKOUT0 enable 0x11 = CLKOUT0 disable
262	1	Clk out freq	From pins	0x20 = CLKOUT0 25 MHz (RGMII) 0x21 = CLKOUT0 50 MHz (RMII)
263	1	RMII Clk In	From pins	0x60 = RMII internal (SoC) clock 0x61 = RMII external clock
264	1	Port Enable	0x01	Bit map. A set bit indicates that the corresponding physical port will be enabled
265	1	Phy Query	From pins	0x30 = speed/duplex determined from RGMII status register 0x31 = MDIO used to query PHY 0x32 = Use fixed speed/duplex values from offset 266/267.
266	1	Speed		0x40 = full speed (1Gbit for RGMII, 100Mbit for RMII) 0x41 = slow speed (100Mbit for RGMII, 10Mbit for RMII)
267	1	Duplex		0x50 = full duplex 0x51 = half duplex
Main Level Boot Control				
268	1	Bootp enable	1	0 = Image information already in this structure 1 = Use BOOTP to get boot image information
269	1	Reserved	0	Reserved
270	2	Bootp Timeout	4000	BOOTP timeout in milli-seconds
272	2	TFTP timeout	1000	TFTP timeout in milli-seconds
274	2	Bootp retries	10	Number of BOOTP retries before fail
276	2	TFTP retries	10	Number of TFTP retries before fail
278	2	Reserved	0	Reserved
Network Stack Configuration (plus TFTP server ID)				
280	6	MAC Address	From E-fuse	MAC address of the device
286	2	Reserved	0	Reserved
288	4	Device IP	0	IP address of the device. Valid only if BOOTP not enabled
292	4	Net Mask	0	Net mask. Valid only if BOOTP not enabled
296	4	Tftp server IP	0	TFTP server IP. Valid only if BOOTP not enabled
BOOTP send and receive Information				
300	20	Vendor String	"TI K3 Bootp Boot"	BOOTP request vendor string. Valid only if BOOTP not enabled
320	9	Client ID	1-mac-address-0	Client ID. See RFC1700
329	1	ID len	7	Client ID length
330	45	Debug array	SOC ID up to size available	Debug array output
375	1	Debug len	Varies	The number of valid bytes in debug array

Table 4-51. Ethernet Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
376	4	Next hop	0	Next hop IP address. Valid only if bootp not enabled
380	4	Default Route	0	IP default route IP address. Valid only if bootp not enabled
384	128	Boot filename	0	Boot filename. Valid only if bootp not enabled

4.6.9 xSPI Boot Parameter Table

xSPI Boot Parameter Table shows the boot parameter table for xSPI boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-52. xSPI Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode on	From Pins	If non-zero, the mode byte will be sent
258	1	Instruct Width	From Pins	Number of pins used to send instructions (1, 8)
259	1	Address Width	From Pins	Number of pins used to send address (1, 8)
260	1	Data Width	From Pins	Number of pins used to received data (1, 8)
261	1	Address Size	24	24 and 32 bits are the valid address sizes
262	1	Mode	0	QSPI clock polarity and phase mode
263	1	CSEL	From Pins	Chip select number (0–3)
264	1	Read Cmd	From Pins	Command used to read read data
265	1	Mode byte	0	Value used for the mode byte (when active)
266	1	Dummy Cycles	From pins	Number of dummy cycles sent after the read command
267	1	clkRecovery	From pins	Clock recovery
268	1	dqsEnable	0	Enable DQS
269	1	ddrEnable	From pins	OSPI DDR mode operation
270	2	Module Freq	0	The QSPI module frequency after PLL enable, in kHz. If 0, ROM code uses the value from the module clock tables.
272	4	Bus Frequency	From pins	The QSPI bus frequency, in kHz
276	4	Delay	0x64641818	The chip select read delays. Default value is based on the read command
280	1	SFDP	From Pins	Enables SFDP parser for 1S-1S-1S to 8D-8D-8D switching
284	4	Tap Delay	0xFFFFFFFF	The read tap selection. If 0xFFFFFFFF, the ROM code will scan the taps to find the best delay. The result will then overwrite the value in this table.
288	4	Unused	Unused	
292	4	Read Index	0	Index to the active read address
296	4	Read Addr 0	0x000000	The initial flash read address
300	4	Read Addr 1	0x400000	Backup read address

4.6.10 USB DFU Boot Parameter Table

USB DFU Boot Parameter Table shows the boot parameter table for USB DFU boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-53. USB DFU Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Port	From pins	Physical port number. Always set to 0.
260	4	Base address 0	From pins (port)	Base address of USB subsystem (CMN)

Table 4-53. USB DFU Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
264	4	Base address 1	From pins (port)	Base address of controller
268	4	phyBaseAddress	From pins (port)	Base address of USB PHY module
272	4	modRefClkkHz	varies	Module reference clock, in kHz
276	2	Vendor ID	0x0451	USB vendor ID. Read from control registers.
278	2	Product ID	0x6165	USB product ID. Read from control registers.
280	2	BCD Device	0x200	Binary Coded Decimal device release number
284	4	String Table addr	0x4182A76C	Pointer to the string table in RAM
288	2	Vendor String offset	0	Offset to vendor string in string table
290	2	Prod string offset	32	Offset to product string in string table
292	2	Serial num string offset	64	Offset to serial number string in string table
294	2	Timeout	5000	USB timeout in milliseconds
296	2	Mode	1	1 = DFU ≠1 = MSC Mode 1 = backup DFU, 2 = backup MSC
298	1	Lane reverse	From pins	Set to non-zero for lane reverse
299	1	CoreVoltage	From pins	USB Core Voltage 0 = 0.85V, 1 = 0.75V
300	4	Block Size	4096	DFU Block Size

4.6.11 USB MSC Boot Parameter Table

USB MSC Boot Parameter Table shows the boot parameter table for USB boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-54. USB MSC Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Port	From pins	Physical port number. Always set to 0.
260	4	Base address 0	From pins (port)	Base address of USB subsystem (CMN)
264	4	Base address 1	From pins (port)	Base address of controller
268	4	phyBaseAddress	From pins (port)	Base address of USB PHY module
272	4	modRefClkkHz	varies	Module reference clock, in kHz
276	2	Vendor ID	0x0451	USB vendor ID. Read from control registers.
278	2	Product ID	0x6164	USB product ID. Read from control registers.
280	2	BCD Device	0	Binary Coded Decimal device release number
284	4	String Table addr	0x4182BCA8	Pointer to the string table in RAM
288	2	Vendor String offset	0	Offset to vendor string in string table
290	2	Prod string offset	0	Offset to product string in string table
292	2	Serial num string offset	0	Offset to serial number string in string table
294	2	Timeout	5000	USB timeout in milliseconds
296	2	Mode	1	1 = DFU ≠1 = MSC Mode 1 = backup DFU, 2 = backup MSC
298	1	Lane reverse	From pins	Set to non-zero for lane reverse
299	1	CoreVoltage	From pins	USB Core Voltage 0 = 0.85V, 1 = 0.75V
300	64	FileName	tiboot3.bin	Boot file name

4.6.12 GPMC NOR Boot Parameter Table

Table 4-55 shows the boot parameter table for GPMC NOR boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-55. GPMC NOR Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	refClkkHz	0	The module functional clock frequency, in kHz. 0 = ROM code computes the value.
260	4	csSizeMb	64	The size of each chip-select, in MB
264	1	Csel	From pins	The chip-select to use (0-3)
265	1	adMux	From pins	The address/data multiplexing used. 0 = A/D parallel, 1 = A/A/D mux, 2 = A/D mux
266	1	Width	16	Data bus width
267	1	Reserved	0	Reserved
268	4	Read index	0	The currently active read offset (0-1)
272	4	Read offset 0	0x000000	Read address offset 0
276	4	Read offset 1	0x400000	Backup read address offset 1
280	4	Reserved	0	Reserved
284	4	Reserved	0	Reserved

4.6.13 GPMC NAND Boot Parameter Table

GPMC NAND Boot Parameter Table shows the boot parameter table for GPMC NAND boot. Must be preceded with the common boot parameters described in Table 4-39.

Table 4-56. GPMC NAND Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Ref Clk kHz	From pins	Specifies the module ref clock.
260	4	Page Size	0	Page size in bytes 2048 or 4096
264	1	Chip Select	0	Chip Select
265	1	Ad Mux	0	Address/data multiplexing
266	1	Data Bus Width	8	Data bus width. Valid values are 8 and 16
267	1	AD rows	0	Number of Row address
268	1	AD columns	0	Number of Column address cycles
269	1	ECC Nibbles	0	Size of BCH remainder in nibbles. 0 if no ECC, 26 for BCH8
270	2	Current Valid Block	0xFFFF	Block number of last known good block
272	2	Pages per Block	0	Number of pages in a block
274	2	Reserved	0	Reserved
276	4	Current Read Index	0	Active read index
280	4	Read Offset[0]	0	Offsets from base of GPMC NAND memory
284	4	Read Offset[1]	0x400000	Offsets from base of GPMC NAND memory

4.7 Boot Image Format

4.7.1 Overall Structure

The boot image consists of an X.509 Certificate, which is optional for GP devices, followed immediately by a boot image blob.

X.509 Certificate (Variable Size) (Optional)
Boot Image Blob (Variable Size)

4.7.2 X.509 Certificate

The X.509 certificate is described in RFC5280. Section 4.1 of the specification describes the format.

The X.509 fields relevant to the public boot (taken from RFC5280) are shown below.

```
Certificate  ::=  SEQUENCE  {
        tbsCertificate       TBSCertificate,
        signatureAlgorithm   AlgorithmIdentifier,
        signatureValue       BIT STRING  }
   TBSCertificate  ::=  SEQUENCE  {
        version         [0]  EXPLICIT Version DEFAULT v1,
        serialNumber         CertificateSerialNumber,
        signature            AlgorithmIdentifier,
        issuer               Name,
        validity             Validity,
        subject              Name,
        subjectPublicKeyInfo SubjectPublicKeyInfo,
        issuerUniqueID  [1]  IMPLICIT UniqueIdentifier OPTIONAL,
                             -- If present, version MUST be v2 or v3
        subjectUniqueID [2]  IMPLICIT UniqueIdentifier OPTIONAL,
                             -- If present, version MUST be v2 or v3
        extensions      [3]  EXPLICIT Extensions OPTIONAL
                             -- If present, version MUST be v3
        }
  Extensions  ::=  SEQUENCE SIZE (1..MAX) OF Extension
   Extension  ::=  SEQUENCE  {
        extnID      OBJECT IDENTIFIER,
        critical    BOOLEAN DEFAULT FALSE,
        extnValue   OCTET STRING
                    -- contains the DER encoding of an ASN.1 value
                    -- corresponding to the extension type identified
                    -- by extnID
        }
```

In general, an X.509 certificate contains a public key which has been signed by a private key. The public ROM code does not directly use the keys. In non-secure devices, the public key value is in general a don’t care condition. The exception is certificates containing a degenerate RSA public key. GP devices with a degenerate RSA key allow for integrity checking of most (but not all) of the certificate.

The public ROM only needs to extract some of information from the X.509 formatted structure:

- The total size of the X.509 Certificate
- The total size of the boot image

The total size of the X.509 Certificate is determined by reading the length of the sequence containing the certificate. The length of the image is determined by parsing the certificate to find the extension field which holds the image length.

The ROM defines several extensions that are used only by TI for boot. These are placed in the extensions field of the TBS certificate.

4.7.3 Organizational Identifier (OID)

OID (organizational identifier) values are represented as a tree structure. TI has the following node registered:

1.3.6.1.4.1.294: iso(1), identified-organization(3), dod(6), internet(1), private(4), enterprise(1), Texas Instruments(294)

ROM code adds the following branch after *Texas Instruments*: *device-boot(1)*. The OID values shown in this section are leaves off the device boot branch.

4.7.4 X.509 Extensions Specific to Boot

These values are not defined in any standard, but created by TI for boot.

4.7.4.1 Boot Info (OID 1.3.6.1.4.1.294.1.1)

This extension must be present on all boot images. It is from this extension that the image length is extracted.

```
bootInfo ::=  SEQUENCE {
   cert_type: INTEGER,-- identifies the certificate type
   boot_core:INTEGER,-- identifies the boot core
   core_opts:INTEGER,-- 32 or 64 bit boot core target
   load_addr:OCTET STRING,-- Global address image destination
   image_size:INTEGER,-- Image size in bytes
}
```

Table 4-57. Certificate Type Values

Value	Description
0x0000_0001	Primary boot image
0x0000_0002	Firmware image

Table 4-58. Boot Core Values

Value	Description
0x00	Firmware (DMSC) image
0x08	DMSC certificate
0x10	MCU image
0x20	Reserved

Table 4-59. Core Options Bit Fields

31 2	1	0
Reserved	Split	Mode

Table 4-60. Core Options Field Description

Bits	Field	Value	Description
1	Split	0	Dual MCU set to lockstep (two cores in lockstep)
		1	Dual MCU set to split mode (two independent cores)
0	Mode	0	MCU starts execution in Arm® mode
		1	MCU starts execution in Thumb® mode

4.7.4.2 Image Integrity (OID 1.3.6.1.4.1.294.1.2)

```
imageIntegrity ::= SEQUENCE {
   sha_type:OID,-- Identifies the SHA type
   hash:OCTET STRING-- The SHA of the boot image
}
```

4.7.5 Extended Boot Info Extension

The ROM supports a combined boot image boot flow. In this flow, a boot binary blob has both Secondary bootloader (SBL) and System Firmware (SYS-FW) embedded in the boot image with a single X509 certificate. This method helps with the following situations:

- Allows ROM to load and run both the bootloader and SYS-FW in parallel without any dependency.
- Optimizes ROM boot time by minimizing different x509 certificate parsing and authentication.

To support this combined boot format, ROM employs a new X509 extension called: ext_boot_info. It supports multiple boot components with a single certificate. It allows up to 5 components as part of this extension:

- Component1: Mandatory and should point to info about SBL binary
- Component2: Optional and if present should point to SYS-FW binary in all device types
- Component3: Optional (Load section to SBL, new certType)
- Component4: Optional (Load section to SYS-FW, new certType)
- Component5:
  - HS-FS and HS-SE non Prime devices. Mandatory and should point to SYS-FW Inner certificate
  - GP and HS-SE Prime devices. Optional (Load Section to SBL or SYS-FW)

This extended boot info extension replaces boot_seq (boot_info) and image_integrity extensions from the previous sections, and these should be exclusive in any given certificate.

ROM supports other extensions, such as sw_rev and debug_info, in both formats.

ROM selects the combined image flow based on the presence of ext_boot_info extension in the certificate and skips boot_seq (boot_info) and image_integrity extensions boot flow.

Having one component in ext_boot_info is same as legacy flow (that is, flow using boot_seq and image_integrity); for two or more components, ROM starts both SBL and SYS-SW, the third and fourth components are loaded by ROM to the allowed loading memory range of SBL and SYS-FW if there is no overlap in load address with executable binary info.

Each of the components can independently specify hash value of the binary, and ROM validates the hash on HS and GP if RSA degenerate key is used for signing.

Additionally, ROM rejects the full image if hash of any single component mismatches.

4.7.5.1 Impact on HS Device

For HS devices, ROM supports encryption of images optionally when specified with the Encryption extenstion.

Encryption - Encryption of the components must be specified with a new extension called ext_boot_enc. This is an optional extension that must be specified only if any of the components are encrypted with a customer key set. Specify a component number followed by encryption extension details for ROM to decrypt the given components. This extension is used only with combined boot image format (that is, using Extended Boot Info Extension).

Prime vs Non-Prime - The main difference between HS prime and non-prime devices is the presence of the SYS-FW Inner certificate. Extended boot info extension supports both prime and non-prime devices. ROM supports SYS-FW binary as Comp#2 in all device types; for HS-SE non-prime and HS-FS devices, the SYS-FW inner certificate is expected as another optional component in #3, 4, or 5.

4.7.5.2 Extended Boot Info Details

```
1.3.6.1.4.1.294.1.9=ASN1:SEQUENCE:ext_boot_info
[ ext_boot_info ]
 extImgSize = INTEGER:470656
 numComp = INTEGER:4
 sbl=SEQUENCE:comp1
 fw=SEQUENCE:comp2
 bd1=SEQUENCE:comp3
 bd2=SEQUENCE:comp4

[ comp1 ]
 compType = INTEGER:1
 bootCore = INTEGER:16
 compOpts = INTEGER:0
 destAddr = FORMAT:HEX,OCT:41c00000
 compSize = INTEGER:237376
 shaType = OID:2.16.840.1.101.3.4.2.3
```

```
 shaValue =
FORMAT:HEX,OCT:6779fdb2b2c27169737c184085b97938bd77bdf698245840f166ca30c7125c29a6675139a25a0a2a3f00a
76d43d082df238c12cb6b293ec0eeb5990bcd603a23

[ comp2 ]
 compType = INTEGER:2
 bootCore = INTEGER:0
 compOpts = INTEGER:0
 destAddr = FORMAT:HEX,OCT:00040000
 compSize = INTEGER:196608
 shaType = OID:2.16.840.1.101.3.4.2.3
 shaValue =
FORMAT:HEX,OCT:47f27fb24b81927a928845a4c2b993e6a3d5bdfe5ed01c0ec4f96a7ead991c69bf4ed4b9b958fd36a75f3
3aba04d2c28602a85ca737ee75617d6a9a41f4353a3

[ comp3 ]
 compType = INTEGER:18
 bootCore = INTEGER:0
 compOpts = INTEGER:0
 destAddr = FORMAT:HEX,OCT:00072000
 compSize = INTEGER:16384
 shaType = OID:2.16.840.1.101.3.4.2.3
 shaValue =
FORMAT:HEX,OCT:2d165ec1d8a38acb977d9298e8a6a27491c62d6daa31f921db9135f9a68779b30b384573c6e4e8203de5f
0a47191c3ff9a35b52a911874e07615f10b4b2f5829

[ comp4 ]
 compType = INTEGER:17
 bootCore = INTEGER:16
 compOpts = INTEGER:0
 destAddr = FORMAT:HEX,OCT:41c40000
 compSize = INTEGER:20288
 shaType = OID:2.16.840.1.101.3.4.2.3
 shaValue =
FORMAT:HEX,OCT:12d5be5b2b9774d1b0cad21cbf1dbcdbd7c310657f4334902e3cc6228cf2d8fc844139dae4db6041c38cd
a502d6a900d57039322d360032268a13445021b04a7
```

4.7.5.3 Certificate / Component Types

ROM supports only the following component types; all other component types will be rejected.

- CompType 0x1 for SBL binary - compType = INTEGER:1
- CompType 0x2 for SYS_FW binary - compType = INTEGER:2
- CompType 0x3 for SYS_FW Inner Certificate - compType = INTEGER:3
- CompType 0x11 for SBL Memory load section - compType = INTEGER:17

Primary Image load section, that can be loaded in to SBL allowed memory range:

- CompType 0x12 for SYS_FW Memory load section - compType = INTEGER:18

SYS-FW load section, that can be loaded in to SYS-FW allowed memory range

4.7.5.4 Extended Boot Encryption Info

Extended Boot Encryption Info specifies the imageEncryption extension per component basis. This extension is not applicable for GP or HS-FS devices, and is optional for HS-SE devices if any components in the image are encrypted. In HS-FS and HS-SE non-prime devices, the SYS-FW binary encryption details are part of SYS-FW Inner certificate. This extension is applicable if either SBL, SYS-FW binary in HS-SE prime, or any binary blobs are encrypted in HS-SE devices.

```
1.3.6.1.4.1.294.1.10=ASN1:SEQUENCE:ext_enc_info

[ ext_enc_info ]
 numComp = INTEGER:2
 esbl=SEQUENCE:enc1
 efw=SEQUENCE:enc2

[ enc1 ]
 compNum = INTEGER:1
 iv = FORMAT:HEX,OCT:474bfd801866beecc7ab6d4c61490e1a
 randString = FORMAT:HEX,OCT:772fc5810fa36f516e595ad8adf19260f47a8461f193892746692fbb932727a1
 iterationCnt = INTEGER:0
```

```
 salt = FORMAT:HEX,OCT:42ea40851298339c8baa84f29d6b68d0

[ enc2 ]
 compNum = INTEGER:2
 iv = FORMAT:HEX,OCT:aaaaaaaaaaaaabeecc7ab6d4c61490e1a
 randString = FORMAT:HEX,OCT:bbbbbbbbbbbbbbbbbe595ad8adf19260f47a8461f193892746692fbb932727a1
 iterationCnt = INTEGER:2
 salt = FORMAT:HEX,OCT:ccccccccccccccccccaa84f29d6b68d0
```

4.7.5.5 Component Ordering

ROM supports fixed Component ordering for SBL- Binary and SYS-FW Cert and Binary.

For GP and HS-SE Prime devices, Comp#1 should be SBL binary, and Comp#2 should be SYS-FW binary.

For HS-FS and HS-SE non-Prime devices, Comp#1 should be SBL binary, Comp#2 should be SYS-FW Inner Certificate, and Comp#3 should be SYS-FW binary.

4.7.5.6 Memory Load Sections Overlap with Executable Components

Memory load sections for SBL and SYS-FW (CompType 0x11 and 0x12) the destination address and size should not overlap with the corresponding load and execute sections, and should also fall in the allowed memory range by ROM.

4.7.5.7 Device Type and Extended Boot Extension

X509 Extension	Component	GP Device	HS-FS	HS-SE non-prime	HS-SE Prime Device
ext_boot_info	Comp#1	SBL Binary	SBL Binary	SBL Binary	SBL Binary
	Comp#2	SYS-FW binary	SYS-FW binary	SYS-FW binary	SYS-FW binary
	Comp#3	SBL mem load section	SBL mem load section	SBL mem load section	SBL mem load section
	Comp#4	SysFW mem load section	SysFW mem load section	SysFW mem load section	SysFW mem load section
	Comp#5	N/A	SysFW inner certificate	SysFW inner certificate	N/A
ext_enc_info	Comp#1	N/A	N/A[1]	SBL encryption	SBL encryption
	Comp#2			N/A	SYS FW encryption
	Comp#3			SBL memory load Encryption	SBL memory load encryption
	Comp#4			Sys-FW memory load encryption	Sys-FW memory load encryption
	Comp#5			N/A[1]	NA

1. SYS-FW encryption in HS-FS and HS-SE (non Prime) are handled in SYS-FW Inner certificate and they are not part of the extended boot info extensions.

4.7.6 Generating X.509 Certificates

X.509 Certificates are generated using OpenSSL and a configuration script to supply values in the extension fields.

4.7.6.1 Key Generation

The SBL must always be signed with a given OpenSSL key - Secure and GP devices. Secure must have encryption and authentication, GP device must only have authentication. The key used for authentication can be random or specific. If a random key is generated and SBL is signed with this,the ROM will copy the SBL image for authentication using memcopy. With this key, ROM code will be directed to use DMA to load the SBL for authentication which saves boot time.

4.7.6.1.1 Degenerate RSA Keys

Degenerate RSA keys are valid RSA keys with the private exponent set to 1. This results in the signature field being equal to the digest, since in RSA:

$$\text{Signature} = \text{digestprivExp mod nprivExp mod } n^{privExp} \qquad (1)$$

Where n is the key size. Since the hash used is SHA-512 and the signature is an ASN.1 sequence containing the OID defining which has was used as well as the hash value, the degenerate RSA must have a value of n greater than the maximum digest size. Typically 1024-bit is chosen.

The following sequence is used to generate degenerate RSA keys:

1. Create a random RSA key:
   ```
   openssl genrsa -out key.pm 1024
   ```
2. Convert to text:
   ```
   openssl rsa -in key.pem -text -noout > key.txt
   ```
3. Create an asn1 template for the degenerate key called degenerateKey.txt. Simply copy the values for modulus, prime (listed as p in key.txt), prime 2 (listed as q), and coefficient (listed as coeff). Set the public and private key exponents to 1, as well as the values for e1 and e2. See the example below.
4. Convert the template to DER:
   ```
   openssl asn1parse -genconf degenerateKey.txt -out degenerateKey.der
   ```
5. Sanity check the key:
   ```
    openssl rsa -in degenerateKey.der -inform der -text -check
   ```
6. If there are no errors create the degenerate key pem file:
   ```
   openssl rsa -in degenerateKey.der -inform der -outform pem -out degenerateKey.pem
   ```

An example degenerateKey.txt file is shown.

```
asn1=SEQUENCE:rsa_key
[rsa_key]
version=INTEGER:0
modulus=INTEGER<copied from key.txt>
pubExp=INTEGER:1
privExp=INTEGER:1
p=INTEGER:<copied from key.txt>
q=INTEGER<copied from key.txt>
e1=INTEGER:1
e2=INTEGER:1
coeff=INTEGER<copied from key.txt>
```

Note that when copying the multi-byte fields from key.txt it is necessary to remove the colons, catenate the lines and add a preceding 0x.

4.7.6.2 Configuration Script

An example openssl configuration script is shown below. Not all extensions are required, but all possible are shown.

```
[ req ]
distinguished_name = req_distinguished_name
X509_extensions = v3_ca
prompt = no
dirstring_type = nobmp
[ req_distinguished_name ]
C = GB
ST = HI
L = Boston
O = Texas Instruments., Inc.
```

```
OU = DSP
CN = Bob
emailAddress = Bob@hou.ti.com
[ v3_ca ]
basicConstraints = CA:true
1.3.6.1.4.1.294.1.1 = ASN1:SEQUENCE:boot_seq
1.3.6.1.4.1.294.1.2 = ASN1:SEQUENCE:image_integrity
1.3.6.1.4.1.294.1.3 = ASN1:SEQUENCE:swrv
1.3.6.1.4.1.294.1.4 = ASN1:SEQUENCE:encryption
1.3.6.1.4.1.294.1.5 = ASN1:SEQUENCE:key_derivation
1.3.6.1.4.1.294.1.7 = ANSI:SEQUENCE:pllControl
1.3.6.1.4.1.294.1.8 = ANSI:SEQUENCE:debug
[ boot_seq ]
certType =INTEGER:1
bootCore = INTEGER:16
bootArchWidth = INTEGER:32
destAddr = FORMAT:HEX,OCT:bc934b00
imageSize = INTEGER:0x00004860
[ image_integrity ]
shaType = OID:1.3.14.3.2.26
shaValue = FORMAT:HEX,OCT:4cf4d59ef77b5d9ab28d2ceb3c9fe83cb52ae6d2
[ swrv ]
rollback = INTEGER:0x00010001
[ encryption ]
Iv =FORMAT:HEX,OCT:00112233445566778899aabbccddeeff
Rstring = FORMAT:HEX,OCT:00112233445566778899aabbccddeeff101112131415161718191a1b1c1d1e1f
Icount = INTEGER:1
Salt = FORMAT:HEX,OCT:00112233445566778899aabbccddeeff
[ pllControl ]
pll0_num = INTEGER:0
pll0_cfg = FORMAT:HEX,OCT:00345678900
pll1_num = INTEGER:1
pll0_cfg = FORMAT:HEX,OCT:00345678900
[ debug ]
uid = FORMAT:HEX,OCT:00345678900
type = INTEGER:1
dbgE = INTEGER:0
secDbgEn = INTEGER:0
```

The certificate is then generated using the following openssl command:

```
openssl req -new -x509 -key <private_key_pem_file> -nodes -out <output_X.509_pem_file> -config
<config_file> -sha512
```

If a delegate key is being signed, then add the option -signkey <sign_key_pem_file> to the command above.

4.7.6.3 Image Data

The image data (blob) is considered simply as a byte stream. On devices that are multiple bytes wide (for example, PCIe) the image must be formatted so that all multi-byte fields match the endianness of the device. The MCU will always run in little endian mode.

4.8 Boot Memory Maps

4.8.1 Memory Layout/MPU

Table 4-61 shows an overview of the MPU configuration. In the R5 MPU, higher numbered regions have priority, therefore in Table 4-61, where two regions overlap, the region on the right defines the memory attributes.

Table 4-61. Memory Layout/MPU

Memory Address	Regions			
0x0000_0000	Region 0 non-executable full access	Region 10		
0x0000_003F				
...				
0x4101_0000		Region 3 TCM User access	Region 4 TCM Priv access	
0x4101_0FFF				
0x4101_1000				
0x4101_7FFF				
...				
0x4180_0000		Region 1 ROM User access	Region 2 ROM Priv access	
0x4180_7FFF				
0x4180_8000				
0x4183_FFFF				
...				
0x6000_0000		Region 11 OSPI memory Cached memory		
...				
0x67FF_FFFF				
...				
0x7000_0000		Region 5 MSRAM All Access Non-cacheable		
0x7017_FFFF				
0x7018_0000			Region 6 non-cacheable	
0x701F_FFFF				
0x7020_0000				
...				
0xFFFF_FFFF				

4.8.2 Global Memory Addresses Used by ROM Code

The ROM code uses several global memory addresses that are useful for debugging. They are shown in Table 4-62.

Table 4-62. Global Memory Addresses

Group	Address	Size (bytes)	Content
Version	0x4182_FF80	0x40	ROM code version (stored in ROM)
Warning/Error Logs	0x701B_D000	0x200	Warning entries in warm boot
Warning/Error Logs	0x701B_D200	0x200	Severe entries in warm boot
Warning/Error Logs	0x701B_D400	0x100	Critical entries in warm boot
Message Logs	0x701B_D580	0x200	Circular message buffer
Message Logs	0x701B_D780	0x14	Circular message context log
Warning/Error Logs	0x701B_D800	0x200	Warning entries in cold boot
Warning/Error Logs	0x701B_DA00	0x200	Severe entries in cold boot
Warning/Error Logs	0x701B_DC00	0x100	Critical entries in cold boot
Warning/Error Logs	0x701B_DD00	0x28	Cold boot log context

Table 4-62. Global Memory Addresses (continued)

Group	Address	Size (bytes)	Content
Warning/Error Logs	0x701B_DD28	0x28	Warm boot log context
Warning/Error Logs	0x701B_DD50	0x4	Active context pointer (not index) to one of the cold or warm contexts
Trace	0x701B_DD80	0x18	Boot trace context
Trace	0x701B_DD98	0x400	Boot trace entry buffers
Parameter Tables	0x701B_EBFC	0x4	Parameter table index (currently active table, 0 or 1)
Parameter Tables	0x701B_EC00	0x200	Parameter table 0
Parameter Tables	0x701B_EE00	0x200	Parameter table 1
Free MSRAM	0x7000_0000	0x180000	Loadable space for SBL

The ROM code version information is a structure shown in Table 4-63

Table 4-63. ROM Code Version

Field	Address	Size (bytes)	Value for PG1
Version Number	0x4182_FF80	0x4	0x00010000 (1.0.0)
Version Date	0x4182_FF84	0x8	"09/12/20"
Device Name	0x4182_FF8C	0xC	"am64x"
Commit ID	0x4182_FF98	0x28	"5ad0da4ef87e4abedeb478cd430cbdb5e131e956"

Chapter 5
Device Configuration

This chapter describes the device configuration details including information related to Control MMR's, Power, Reset, and Clocking.

5.1 Control Module (CTRL_MMR)

The control module controls top-level device behavior in various states. It contains registers for configuration, bootstrap signals, I/O pad multiplexing, clock selection, and many others.

There are two CTRL_MMR modules in this device - CTRL_MMR0 which resides in VD_CORE and MCU_CTRL_MMR0 in VD_MCU voltage domain. There are also two other modules dedicated to pad configuration - PADCFG_CTRL0_CFG0 and MCU_PADCFG_CTRL0_CFG0. There is also one more module (SEC_MMR0) that has registers to control the configuration of the MAIN domain processors.

The following sections describe all these modules.

5.1.1 CTRL_MMR0 and PADCFG_CTRL0_CFG0

The following sections describe the CTRL_MMR0 and PADCFG_CTRL0_CFG0 modules.

5.1.1.1 CTRL_MMR0 and PADCFG_CTRL0_CFG0 Overview

The CTRL_MMR0 module has registers associated mainly with:

- Kick protection (register write protection)
- CTRL_MMR0 module interrupts
- EHRPWM/EQEP control and status
- Clock muxing and division
- Ethernet port operation control
- DDRSS dynamic frequency change
- Device features
- and a few other registers and register groups.

The PADCFG_CTRL0_CFG0 module has registers associated mainly with:

- Device pad configuration
- Kick protection (register write protection)
- PADCFG_CTRL0_CFG0 module interrupts

5.1.1.2 CTRL_MMR0 and PADCFG_CTRL0_CFG0 Integration

This section describes CTRL_MMR0, PADCFG_CTRL0_CFG0, and SEC_MMR0 integration in the device, including information about clocks, resets, and hardware requests.

One CTRL_MMR0, one PADCFG_CTRL0_CFG0, and one SEC_MMR0 modules are integrated in the device MAIN domain. Figure 5-1 shows their integration.

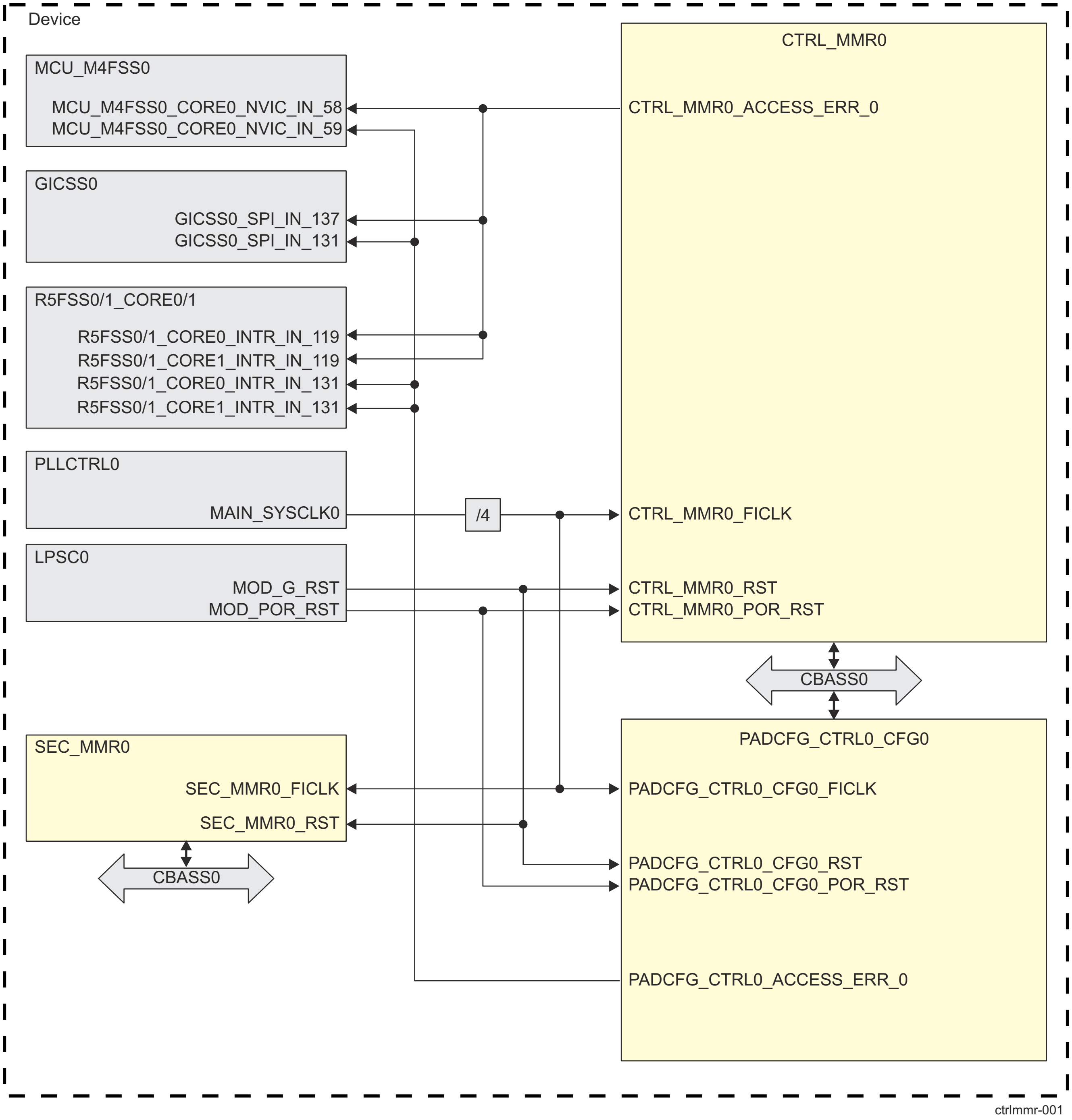

Figure 5-1. CTRL_MMR0, PADCFG_CTRL0_CFG0, and SEC_MMR0 Integration

Table 5-1 through Table 5-3 summarize the integration of the CTRL_MMR0, PADCFG_CTRL0_CFG0, and SEC_MMR0 modules in the device MAIN domain.

Table 5-1. CTRL_MMR0, PADCFG_CTRL0_CFG0, and SEC_MMR0 Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	**Power Domain**	**Module Domain**	**Interconnect**
CTRL_MMR0 PADCFG_CTRL0_CFG0 SEC_MMR0	PSC0	PD0	LPSC0	CBASS0

Table 5-2. CTRL_MMR0, PADCFG_CTRL0_CFG0, and SEC_MMR0 Clocks and Resets

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
CTRL_MMR0	CTRL_MMR0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	Functional and interface clock for the CTRL_MMR0 module with frequency equal to MAIN_SYSCLK0 divided by 4.
PADCFG_CTRL0_CFG0	PADCFG_CTRL0_CFG0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	Functional and interface clock for the PADCFG_CTRL0_CFG0 module with frequency equal to MAIN_SYSCLK0 divided by 4.
SEC_MMR0	SEC_MMR0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	Functional and interface clock for the SEC_MMR0 module with frequency equal to MAIN_SYSCLK0 divided by 4.
Resets				
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
CTRL_MMR0	CTRL_MMR0_RST	MOD_G_RST	LPSC0	Module level main reset
	CTRL_MMR0_POR_RST	MOD_POR_RST	LPSC0	Module power-on reset
PADCFG_CTRL0_CFG0	PADCFG_CTRL0_CFG0_RST	MOD_G_RST	LPSC0	Module level main reset
	PADCFG_CTRL0_CFG0_POR_RST	MOD_POR_RST	LPSC0	Module power-on reset
SEC_MMR0	SEC_MMR0_RST	MOD_G_RST	LPSC0	SEC_MMR0 module reset

Table 5-3. CTRL_MMR0 and PADCFG_CTRL0_CFG0 Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
CTRL_MMR0	CTRL_MMR0_ACCESS_ERR_0	MCU_M4FSS0_CORE0_NVIC_IN_58	MCU_M4FSS0	Interrupt indicating protection, addressing, lock violation.	Level
		GICSS0_SPI_IN_137	GICSS0		
		R5FSS0_CORE0_INTR_IN_119	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_119	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_119	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_119	R5FSS1_CORE1		
PADCFG_CTRL0_CFG0	PADCFG_CTRL0_ACCESS_ERR_0	MCU_M4FSS0_CORE0_NVIC_IN_59	MCU_M4FSS0	Interrupt indicating protection, addressing, lock violation.	Level
		GICSS0_SPI_IN_131	GICSS0		
		R5FSS0_CORE0_INTR_IN_131	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_131	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_131	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_131	R5FSS1_CORE1		

Table 5-3. CTRL_MMR0 and PADCFG_CTRL0_CFG0 Hardware Requests (continued)

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
DMA Events					
Module Instance	**Module DMA Event**	**Destination DMA Event Input**	**Destination**	**Description**	**Type**
CTRL_MMR0	-	-	-	-	-
PADCFG_CTRL0_CFG0	-	-	-	-	-

Note

For more information about CTRL_MMR0_ACCESS_ERR_0 and PADCFG_CTRL0_ACCESS_ERR_0, see Section 5.1.1.3.1.5 .

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

5.1.1.3 CTRL_MMR0 and PADCFG_CTRL0_CFG0 Functional Description

5.1.1.3.1 Description for CTRL_MMR0 and PADCFG_CTRL0_CFG0 Register Types

The following sub-sections provide summary and description for most of the registers which are part of the CTRL_MMR0 and PADCFG_CTRL0_CFG0 modules memory spaces. The rest of the registers are described in the corresponding chapters where the functionality associated with particular register is covered in more detail.

5.1.1.3.1.1 Pad Configuration Registers

The pad configuration registers are used to configure most of the device pads. Each pad configuration register (PADMMR_PADCONFIG0 to PADMMR_PADCONFIG181) is assotiated only with one pad and has bits as described in Table 5-4.

Table 5-4. Description Of The Pad Configuration Register Bits

Bit	Field(1)	Type	Description
31	LOCK	R/W	Pad configuration register lock bit. 0h - The corresponding pad configuration register is unlocked. Its value can be modified. Further writes are allowed. 1h - The corresponding pad configuration register is locked. Its value can not be modified. Further writes are not allowed.
30-22	RESERVED	R	Reserved
21	TX_DIS	R/W	Disables the driver for a pad 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	Reserved
18	RXACTIVE	R/W	Input enable for a pad 0h - Receiver disabled 1h - Receiver enabled
17-15	RESERVED	R	Reserved
14	ST_EN	R/W	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled

Table 5-4. Description Of The Pad Configuration Register Bits (continued)

Bit	Field(1)	Type	Description
13-11	DEBOUNCE_SEL	R/W	Selects the debouce period for a pad. For more information, see *I/O Debounce Registers*. 0h - Debounce period of 0 1h - Debounce period as specified via the CTRLMMR_MCU_DBOUNCE_CFG1[5-0] DB_CFG field 2h - Debounce period as specified via the CTRLMMR_MCU_DBOUNCE_CFG2[5-0] DB_CFG field 3h - Debounce period as specified via the CTRLMMR_MCU_DBOUNCE_CFG3[5-0] DB_CFG field 4h - Debounce period as specified via the CTRLMMR_MCU_DBOUNCE_CFG4[5-0] DB_CFG field 5h - Debounce period as specified via the CTRLMMR_MCU_DBOUNCE_CFG5[5-0] DB_CFG field 6h - Debounce period as specified via the CTRLMMR_MCU_DBOUNCE_CFG6[5-0] DB_CFG field 7h - Reserved
10-4	RESERVED	R	Reserved
3-0	MUXMODE	R/W	Selects the desired multiplexing mode for a pad 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

(1) Some bits may not be present in all PADCONFIGx registers.

Many of the device pads support pad multiplexing. This means that their function can be independently chosen from two or more options. The selection of functions available on each pad is enumerated in table "*Pin*

Multiplexing" of the device-specific Datasheet. The desired function is selected via the MUXMODE field of the associated pad configuration register.

The PADMMR_PADCONFIG0 to PADMMR_PADCONFIG181 registers control the signal multiplexing of modules in the device MAIN domain.

5.1.1.3.1.2 Kick Protection Registers

The CTRL_MMR0 memory space is divided into several partitions. There are Kick and Proxy registers associated with each partition. This section describes the Kick registers. For information about the Proxy registers see Section 5.1.1.3.1.4

The CTRL_MMR0 module has a protection mechanism which prevents spurious writes from changing the values of its registers. The LOCKi_KICK0 and LOCKi_KICK1 registers are used for this purpose. A write is required first to the LOCKi_KICK0[31-1] KEY field and then to the LOCKi_KICK1[31-0] KEY field with exact data values to unlock the protection mechanism. Once released then all registers within Partition "i" having write permissions can be written to. The read only registers are still read only. An indication for unlocked Partition "i" is when the LOCKi_KICK0[0] UNLOCKED bit is set to 1h. When the protection mechanism is locked (indicated by LOCKi_KICK0[0] UNLOCKED = 0h) none of the registers within Partition "i" can be written to. They can only be read.

Table 5-5 shows the values that must be written to the LOCKi_KICK0 and LOCKi_KICK1 registers to unlock each partition. Writing any other data value to either of these registers locks the protection mechanism and blocks any writes to the registers that reside in Partition "i".

The PADCFG_CTRL0_CFG0 module also has kick protection registers.

Table 5-5. Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Offset Range	Proxy1 Offset Range
MAIN_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	68EF 3490h	0000h to 1FFFh	2000h to 3FFFh
MAIN_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	D172 BC5Ah		
MAIN_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	68EF 3490h	4000h to 5FFFh	6000h to 7FFFh
MAIN_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	D172 BC5Ah		
MAIN_CTRL_MMR_CFG0_LOCK2_KICK0	Partition 2	68EF 3490h	8000h to 9FFFh	A000h to BFFFh
MAIN_CTRL_MMR_CFG0_LOCK2_KICK1	Partition 2	D172 BC5Ah		
MAIN_CTRL_MMR_CFG0_LOCK3_KICK0	Partition 3	68EF 3490h	C000h to DFFFh	E000h to FFFFh
MAIN_CTRL_MMR_CFG0_LOCK3_KICK1	Partition 3	D172 BC5Ah		
MAIN_CTRL_MMR_CFG0_LOCK5_KICK0	Partition 5	68EF 3490h	1 4000h to 1 5FFFh	1 6000h to 1 7FFFh
MAIN_CTRL_MMR_CFG0_LOCK5_KICK1	Partition 5	D172 BC5Ah		
MAIN_CTRL_MMR_CFG0_LOCK6_KICK0	Partition 6	68EF 3490h	1 8000h to 1 9FFFh	1 A000h to 1 BFFFh
MAIN_CTRL_MMR_CFG0_LOCK6_KICK1	Partition 6	D172 BC5Ah		
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	68EF 3490h	0000h to 1FFFh	2000h to 3FFFh

Table 5-5. Partition Unlock Values (continued)

Register	Partition	Unlock Value	Proxy0 Offset Range	Proxy1 Offset Range
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	D172 BC5Ah		
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	68EF 3490h	4000h to 5FFFh	6000h to 7FFFh
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	D172 BC5Ah		

- Not listed partitions are reserved and not used.

Note

In order to ensure that all registers from all partitions are write protected, software must always re-lock the protection mechanism after completing the register writes.

The kick protection registers described in this section are an exception and are not write protected by the protection mechanism.

5.1.1.3.1.3 I/O Debounce Control Registers

Some device pads have debounce logic. The following MCU_CTRL_MMR0 registers are used to configure the debounce period as shown in Table 5-6.

Table 5-6. Debounce period

MCU_CTRL_MMR Debounce Register	PADCONFIGx[13-11] DEBOUNCE_SEL setting
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1	1h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2	2h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3	3h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4	4h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5	5h
MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6	6h

Note

The debounce logic is not associated with all signals that can be multiplexed on a pad. Only certain signals can use it.

For information about each signal that has associated debounce logic, see Signal Descriptions in the device Datasheet.

Note

It is recommended to first configure the PADCONFIG and debounce, as well as the debounce counter values in the SoC MMR, prior to enabling the IP.

For information about the PADCONFIGx registers, see *Pad Configuration Registers*.

Table 5-7 shows the debounce period values to load in the MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5-0] DB_CFG field.

Note

The debounce clock selection should happen before the consumer of the debounced signals is enabled as the clock multiplexers for the debounce logic are NOT glitch-free.

Table 5-7. Debounce Period Values

MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5:0] DB_CFG Decimal Value	Slow Inputs (32.768kHz(1))	Fast Inputs (25MHz(1))	MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5:0] DB_CFG Decimal Value	Slow Inputs (25MHz(1))	Fast Inputs (250MHz(1))
	Delay[ms]	**Delay[µs]**		**Delay[µs]**	**Delay[ns]**
0	bypassed	n/a	32	0.04	4
1	1.95	2.56	33	0.08	8
2	2.93	3.84	34	0.12	12
3	3.91	5.12	35	0.16	16
4	4.88	6.40	36	0.20	20
5	5.86	7.68	37	0.24	24
6	6.84	8.96	38	0.28	28
7	7.81	10.24	39	0.32	32
8	8.79	11.52	40	0.36	36
9	9.77	12.80	41	0.40	40
10	10.74	14.08	42	0.44	44
11	11.72	15.36	43	0.48	48
12	12.7	16.64	44	0.52	52
13	13.67	17.92	45	0.56	56
14	14.65	19.20	46	0.60	60
15	15.63	20.48	47	0.64	64
16	16.6	21.76	48	0.68	68
17	17.58	23.04	49	0.72	72
18	18.55	24.32	50	0.76	76
19	19.53	25.60	51	0.80	80
20	20.51	26.88	52	0.84	84
21	21.48	28.16	53	0.88	88
	Delay[ms]	**Delay[µs]**		**Delay[µs]**	**Delay[µs]**
22	15.63	20.48	54	20.48	2.048
23	31.25	40.96	55	40.96	4.096
24	46.88	61.44	56	61.44	6.144
25	62.5	81.92	57	81.92	8.192
26	78.13	102.40	58	102.40	10.24
27	93.75	122.88	59	122.88	12.288
28	109.38	143.36	60	143.36	14.336
29	125	163.84	61	163.84	16.384
30	140.63	184.32	62	184.32	18.432
31	156.25	204.80	63	204.80	20.48

(1) These are the debounce logic clock frequencies.

5.1.1.3.1.4 Proxy Addressing Registers

The CTRL_MMR0 memory space is divided into several partitions. There are Kick and Proxy registers associated with each partition. This section describes the Proxy registers. For information about the Kick registers see Section 5.1.1.3.1.2 .

The CTRL_MMR0 module has several registers that provide proxy addressing. This means, each of its registers may be accessed through two different addresses - Proxy0 and Proxy1. The Proxy0 address is intended as the normal read and write access address. The Proxy1 address provides exclusive register write control. When a bit from the P**x**_CLAIM**y**[31-0] PROXY1_CLAIMED field is set to 1h, a register becomes read-only at its Proxy0 address and may only be written through its Proxy1 address. The Proxy registers themselves may always be read through their Proxy0 address but may only be written through their Proxy1 address.

The **x** and **y** indices can be calculated through the following equations:

- **x** = INT(HEX2DEC(address_offset)/16384))
- **y** = INT(MOD(HEX2DEC(address_offset),16384)/128)

where:

- INT() rounds down to the nearest integer
- HEX2DEC() converts from hexadecimal to decimal
- MOD() returns the reminder of HEX2DEC(address_offset)/16384

Table 5-8 shows the proxy registers and the partition they are associated with. Each partition is 16KB. The first 8KB are for Proxy0 addresses, and the second 8KB are for Proxy1 addresses.

The PADCFG_CTRL0_CFG0 module also has proxy addressing registers.

Table 5-8. Proxy Registers and Partitions

Proxy Register	Partition[1]	Proxy0 Offset Range	Proxy1 Offset Range
CTRLMMR_P0_CLAIM0 CTRLMMR_P0_CLAIM4	Partition 0	0000h to 1FFFh	2000h to 3FFFh
CTRLMMR_P1_CLAIM0 CTRLMMR_P1_CLAIM1 CTRLMMR_P1_CLAIM2 CTRLMMR_P1_CLAIM3 CTRLMMR_P1_CLAIM4 CTRLMMR_P1_CLAIM5 CTRLMMR_P1_CLAIM12 CTRLMMR_P1_CLAIM13 CTRLMMR_P1_CLAIM14	Partition 1	4000h to 5FFFh	6000h to 7FFFh
CTRLMMR_P2_CLAIM0 CTRLMMR_P2_CLAIM1 CTRLMMR_P2_CLAIM2 CTRLMMR_P2_CLAIM3 CTRLMMR_P2_CLAIM4 CTRLMMR_P2_CLAIM5 CTRLMMR_P2_CLAIM6 CTRLMMR_P2_CLAIM7 CTRLMMR_P2_CLAIM8 CTRLMMR_P2_CLAIM9 CTRLMMR_P2_CLAIM10	Partition 2	8000h to 9FFFh	A000h to BFFFh
CTRLMMR_P3_CLAIM6	Partition 3	C000h to DFFFh	E000h to FFFFh
CTRLMMR_P5_CLAIM0 CTRLMMR_P5_CLAIM1	Partition 5	1 4000h to 1 5FFFh	1 6000h to 1 7FFFh
CTRLMMR_P6_CLAIM2	Partition 6	1 8000h to 1 9FFFh	1 A000h to 1 BFFFh
PADMMR_P0_CLAIM0	Partition 0	0000h to 1FFFh	2000h to 3FFFh

Table 5-8. Proxy Registers and Partitions (continued)

Proxy Register	Partition[1]	Proxy0 Offset Range	Proxy1 Offset Range
PADMMR_P1_CLAIM0 PADMMR_P1_CLAIM1 PADMMR_P1_CLAIM2 PADMMR_P1_CLAIM3 PADMMR_P1_CLAIM4 PADMMR_P1_CLAIM5	Partition 1	4000h to 5FFFh	6000h to 7FFFh

(1) Not listed partitions are reserved and not used.

5.1.1.3.1.5 CTRL_MMR0 Module Interrupts

The CTRL_MMR0 module has one interrupt request, the CTRL_MMR0_ACCESS_ERR_0, which is associated with the following registers:

- MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS — interrupt raw status register
- MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR — interrupt status register
- MAIN_CTRL_MMR_CFG0_INTR_ENABLE — interrupt enable register
- MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR — interrupt disable register

The PADCFG_CTRL0_CFG0 module also has one interrupt request, the PADCFG_CTRL0_ACCESS_ERR_0, which is associated with the following registers:

- MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS — interrupt raw status register
- MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR — interrupt status register
- MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE — interrupt enable register
- MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR — interrupt disable register

The following applies for the interrupt behavior of the CTRL_MMR0 module:

- The CTRL_MMR0 module asserts its interrupt line only if the interrupts are enabled by setting to 1h the corresponding bits in the MAIN_CTRL_MMR_CFG0_INTR_ENABLE register. These interrupts can be disabled by setting to 1h the corresponding bits in the MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR register.
- After an interrupt has been serviced, software must clear the corresponding status flag. This is done by setting to 1h the corresponding bit in the MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR register which also clears the corresponding bit in the MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS register. The status flags in the MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS register are set even if the corresponding interrupt is disabled unlike those in the MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR register, which are set only if the corresponding interrupt is enabled.
- An interrupt is also generated by the CTRL_MMR0, if certain bit in the MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS register is set to 1h and the corresponding interrupt is enabled through the MAIN_CTRL_MMR_CFG0_INTR_ENABLE register. This feature is useful during user software debugging. In addition, even if interrupts are not enabled the corresponding raw flag in the MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS register is set to 1h when an IRQ condition occurs.
- Even if interrupts are not enabled, a status bit in the MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS register can also be cleared by setting to 1h the corresponding bit in the MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR register.

The same as previously described applies also for the interrupt behavior of the PADCFG_CTRL0_CFG0 module

Table 5-9 lists the interrupt events which can assert the CTRL_MMR0_ACCESS_ERR_0 interrupt line.

Table 5-10 lists the interrupt events which can assert the PADCFG_CTRL0_ACCESS_ERR_0 interrupt line.

Table 5-9. CTRL_MMR0 Events

Event Flag	Event Mask	Description
MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS[2] LOCK_ERR MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR[2] EN_LOCK_ERR	MAIN_CTRL_MMR_CFG0_INTR_ENABLE[2] LOCK_ERR_EN_SET MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR[2] LOCK_ERR_EN_CLR	Lock violation interrupt. Occurs when writing to a register in a locked CTRL_MMR0 partition.
MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS[1] ADDR_ERR MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR[1] EN_ADDR_ERR	MAIN_CTRL_MMR_CFG0_INTR_ENABLE[1] ADDR_ERR_EN_SET MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR[1] ADDR_ERR_EN_CLR	Addressing violation interrupt. Occurs when accessing an illegal address inside the CTRL_MMR0 module.
MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS[0] PROT_ERR MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR[0] EN_PROT_ERR	MAIN_CTRL_MMR_CFG0_INTR_ENABLE[0] PROT_ERR_EN_SET MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR[0] PROT_ERR_EN_CLR	Protection violation interrupt. Occurs when a register is accessed without the required secure/privilege level permissions.

Table 5-10. PADCFG_CTRL0_CFG0 Events

Event Flag	Event Mask	Description
MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS[2] LOCK_ERR MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR[2] EN_LOCK_ERR	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE[2] LOCK_ERR_EN_SET MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR[2] LOCK_ERR_EN_CLR	Lock violation interrupt. Occurs when writing to a register in a locked PADCFG_CTRL0_CFG0 partition.
MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS[1] ADDR_ERR MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR[1] EN_ADDR_ERR	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE[1] ADDR_ERR_EN_SET MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR[1] ADDR_ERR_EN_CLR	Addressing violation interrupt. Occurs when accessing an illegal address inside the PADCFG_CTRL0_CFG0 module.
MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS[0] PROT_ERR MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR[0] EN_PROT_ERR	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE[0] PROT_ERR_EN_SET MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR[0] PROT_ERR_EN_CLR	Protection violation interrupt. Occurs when a register is accessed without the required secure/privilege level permissions.

When an error event as described in Table 5-9 occurs, the error associated details are captured in the MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS, MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS and MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS registers. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS contains the address of the first fault access. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS and MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS contain status attributes associated with the first fault access. To clear the contents of these three registers and allow them to latch the attributes of the next fault the MAIN_CTRL_MMR_CFG0_FAULT_CLEAR[0] CLEAR bit must be set to 1h.

The same as previously described applies also for the PADCFG_CTRL0_CFG0 module. The corresponding registers are as follows:

- MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS
- MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS
- MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS
- MAIN_CTRL_MMR_CFG0_FAULT_CLEAR

5.1.1.3.1.6 EHRPWM/EQEP Control and Status Registers

The CTRL_MMR0 registers which provide control and status information for the EHRPWM/EQEP modules are shown in Table 5-11.

Table 5-11. Summary of the EHRPWM/EQEP Control and Status Registers

Register Name	Description	Associated Functionality Described in:
MAIN_CTRL_MMR_CFG0_EPWM0_CTRL MAIN_CTRL_MMR_CFG0_EPWM1_CTRL MAIN_CTRL_MMR_CFG0_EPWM2_CTRL MAIN_CTRL_MMR_CFG0_EPWM3_CTRL MAIN_CTRL_MMR_CFG0_EPWM4_CTRL MAIN_CTRL_MMR_CFG0_EPWM5_CTRL MAIN_CTRL_MMR_CFG0_EPWM6_CTRL MAIN_CTRL_MMR_CFG0_EPWM7_CTRL MAIN_CTRL_MMR_CFG0_EPWM8_CTRL	Time base clock, source of PWM synchronization input and other controls for the EHRPWM**x**[1] module	*EPWM*[1] *Modules Time Base Clock Gating* and *Daisy-Chain Connectivity between EPWM Modules* in *Enhanced Pulse Width Modulation (EPWM) Module*
MAIN_CTRL_MMR_CFG0_SOCA_SEL MAIN_CTRL_MMR_CFG0_SOCB_SEL	Start of Conversion output source	*ADC start of conversion signals (PWM_SOCA and PWM_SOCB)* in *Enhanced Pulse Width Modulation (EPWM) Module*
MAIN_CTRL_MMR_CFG0_EQEP_STAT	Provides EQEP**x** phase error status information	*Device Specific EQEP Features* in *Enhanced Quadrature Encoder Pulse (EQEP) Module*

(1) The terms "EPWM" and "EHRPWM" are interchangeable in this section.

5.1.1.3.1.7 Clock Muxing and Division Registers

There are registers within the CTRL_MMR0 module address space dedicated to clock muxing and division for some device modules. Table 5-12 summarizes these registers. Related information can also be found in Section 5.4 *Clocking*.

Table 5-12. Summary of the Clock Muxing and Division Registers

Register Name	Register Name	Register Name
MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL	MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL
MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL	MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL	MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL
MAIN_CTRL_MMR_CFG0_GTC_CLKSEL	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL
MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL	MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL
MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL
MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL	MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL
MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL	MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL
MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL	MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL
MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL	MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL

Table 5-12. Summary of the Clock Muxing and Division Registers (continued)

Register Name	Register Name	Register Name
MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL	MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL
MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL	MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL
MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL	MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL	MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL
MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL	MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL	MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL
MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL	MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL	MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL
MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL	MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL	MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL
MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL	MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL	MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL
MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL	MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL
MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL	MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL	MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL
MAIN_CTRL_MMR_CFG0_USB0_CLKSEL	MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL
MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL	MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL	MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL
MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL		

5.1.1.3.1.8 Ethernet Port Operation Control Registers

There are registers within the CTRL_MMR0 module address space that control the operation of each ethernet port in the device main domain. These registers are summarized in Table 5-13.

Table 5-13. Ethernet Port Operation Control Registers

Register Name	Register Name
CTRLMMR_ENET1_CTRL	CTRLMMR_ENET2_CTRL

5.1.1.3.1.9 DDRSS Dynamic Frequency Change Registers

There are registers within the CTRL_MMR0 module address space that are used to dynamically change the DDR clock frequency to support LPDDR4 Frequency Set Point (FSP). These registers are shown in Table 5-14. For more information, see Section 8.1.4.8 *DDRSS Dynamic Frequency Change Interface* in Chapter 8 *Memory Controllers*.

Table 5-14. DDRSS Dynamic Frequency Change Registers

Register Name	Register Name
MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ	MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ
MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK	MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK

5.1.1.3.1.10 Device Feature Registers

The following registers within the CTRL_MMR0 module address space provide status information regarding specific device features:

- MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0
- MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2
- MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6

5.1.2 MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0

The following sections describe the MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 modules.

5.1.2.1 MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Overview

The MCU_CTRL_MMR0 module has registers associated mainly with:

- Kick protection (register write protection)
- MCU_CTRL_MMR0 module interrupts
- Clock muxing and division
- I/O debounce control
- PRG Modules
- POK Modules
- and a few other registers and register groups.

The MCU_PADCFG_CTRL0_CFG0 module has registers associated mainly with:

- Device pad configuration
- Kick protection (register write protection)
- MCU_PADCFG_CTRL0_CFG0 module interrupts

5.1.2.2 MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Integration

This section describes MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 integration in the device, including information about clocks, resets, and hardware requests.

One MCU_CTRL_MMR0 and one MCU_PADCFG_CTRL0_CFG0 modules are integrated in the device MCU domain. Figure 5-2 shows their integration.

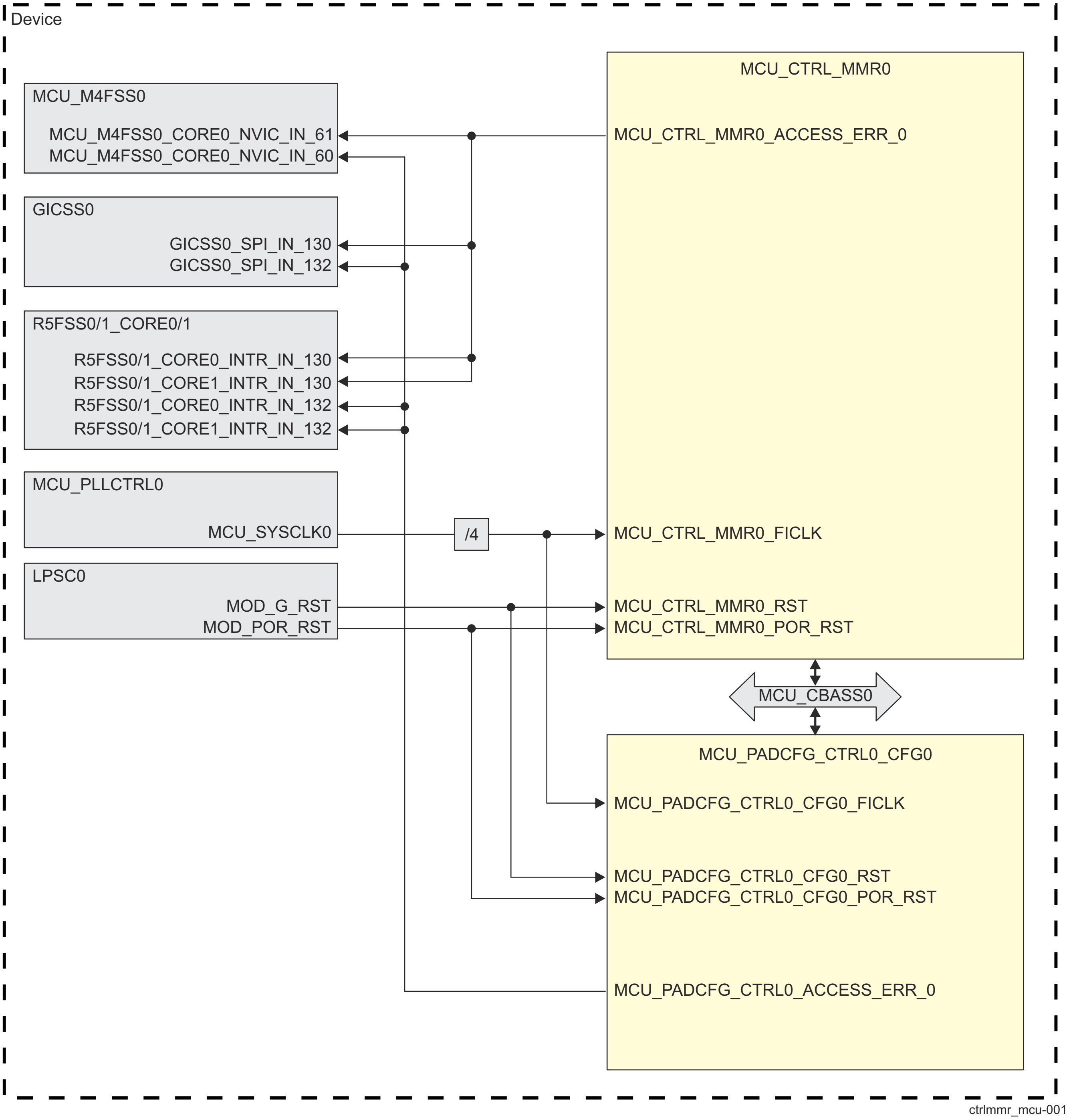

Figure 5-2. MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Integration

Table 5-15 through Table 5-17 summarize the integration of the MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 modules in the device MCU domain.

Table 5-15. MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_CTRL_MMR0 MCU_PADCFG_CTRL0_CFG0	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 5-16. MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Clocks and Resets

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
MCU_CTRL_MMR0	MCU_CTRL_MMR0_FICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	Functional and interface clock for the MCU_CTRL_MMR0 module with frequency equal to MCU_SYSCLK0 divided by 4.
MCU_PADCFG_CTRL0_CFG0	MCU_PADCFG_CTRL0_CFG0_FICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	Functional and interface clock for the MCU_PADCFG_CTRL0_CFG0 module with frequency equal to MCU_SYSCLK0 divided by 4.
Resets				
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
MCU_CTRL_MMR0	MCU_CTRL_MMR0_RST	MOD_G_RST	LPSC0	Module level main reset
	MCU_CTRL_MMR0_POR_RST	MOD_POR_RST	LPSC0	Module power-on reset
MCU_PADCFG_CTRL0_CFG0	MCU_PADCFG_CTRL0_CFG0_RST	MOD_G_RST	LPSC0	Module level main reset
	MCU_PADCFG_CTRL0_CFG0_POR_RST	MOD_POR_RST	LPSC0	Module power-on reset

Table 5-17. MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
MCU_CTRL_MMR0	MCU_CTRL_MMR0_ACCESS_ERR_0	MCU_M4FSS0_CORE0_NVIC_IN_61	MCU_M4FSS0	Interrupt indicating protection, addressing, lock violation.	Level
		GICSS0_SPI_IN_130	GICSS0		
		R5FSS0_CORE0_INTR_IN_130	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_130	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_130	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_130	R5FSS1_CORE1		
MCU_PADCFG_CTRL0_CFG0	MCU_PADCFG_CTRL0_ACCESS_ERR_0	MCU_M4FSS0_CORE0_NVIC_IN_60	MCU_M4FSS0	Interrupt indicating protection, addressing, lock violation.	Level
		GICSS0_SPI_IN_132	GICSS0		
		R5FSS0_CORE0_INTR_IN_132	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_132	R5FSS0_CORE1		

Table 5-17. MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Hardware Requests (continued)

		R5FSS1_CORE0_INTR_IN_132	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_132	R5FSS1_CORE1		
DMA Events					
Module Instance	**Module DMA Event**	**Destination DMA Event Input**	**Destination**	**Description**	**Type**
MCU_CTRL_MMR0	-	-	-	-	-
MCU_PADCFG_CTRL0_CFG0	-	-	-	-	-

Note

For more information about MCU_CTRL_MMR0_ACCESS_ERR_0 and MCU_PADCFG_CTRL0_ACCESS_ERR_0, see Section 5.1.2.3.1.3 .

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

5.1.2.3 MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Functional Description

5.1.2.3.1 Description for MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Register Types

The following sub-sections provide summary and description for most of the registers which are part of the MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 modules memory spaces. The rest of the registers are described in the corresponding chapters where the functionality associated with particular register is covered in more detail.

5.1.2.3.1.1 Pad Configuration Registers

The pad multiplexing scheme is same as described in Section 5.1.1.3.1.1 . For more details, refer to that section. The only difference is that the PADMMR_MCU_PADCONFIG0 to PADMMR_MCU_PADCONFIG32 registers control the signal multiplexing of modules in the device MCU domain.

5.1.2.3.1.2 Kick Protection Registers

The functionaliy of the MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 kick protection registers is same as described in Section 5.1.1.3.1.2 . For more details, refer to that section.

Table 5-18 summarizes the MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 kick protection registers.

Table 5-18. MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Partition Unlock Values

Register	Partition[1]	Unlock Value	Offset Range
CTRLMMR_MCU_LOCK0_KICK0	Partition 0	68EF 3490h	0000h to 1FFFh
CTRLMMR_MCU_LOCK0_KICK1	Partition 0	D172 BC5Ah	
CTRLMMR_MCU_LOCK1_KICK0	Partition 1	68EF 3490h	4000h to 5FFFh
CTRLMMR_MCU_LOCK1_KICK1	Partition 1	D172 BC5Ah	
CTRLMMR_MCU_LOCK2_KICK0	Partition 2	68EF 3490h	8000h to 9FFFh
CTRLMMR_MCU_LOCK2_KICK1	Partition 2	D172 BC5Ah	
CTRLMMR_MCU_LOCK3_KICK0	Partition 3	68EF 3490h	C000h to DFFFh
CTRLMMR_MCU_LOCK3_KICK1	Partition 3	D172 BC5Ah	
CTRLMMR_MCU_LOCK6_KICK0	Partition 6	68EF 3490h	1 8000h to 1 9FFFh
CTRLMMR_MCU_LOCK6_KICK1	Partition 6	D172 BC5Ah	
PADMMR_MCU_LOCK0_KICK0	Partition 0	68EF 3490h	0000h to 1FFFh
PADMMR_MCU_LOCK0_KICK1	Partition 0	D172 BC5Ah	
PADMMR_MCU_LOCK1_KICK0	Partition 1	68EF 3490h	4000h to 5FFFh
PADMMR_MCU_LOCK1_KICK1	Partition 1	D172 BC5Ah	

- Not listed partitions are reserved and not used.

5.1.2.3.1.3 MCU_CTRL_MMR0 and MCU_PADCFG_CTRL0_CFG0 Module Interrupts

The MCU_CTRL_MMR0 module has one interrupt request - the MCU_CTRL_MMR0_ACCESS_ERR_0. The interrupt behavior is same as described in Section 5.1.1.3.1.5 . For more details, refer to that section. When reading replace the corresponding registers with the following:

- CTRLMMR_MCU_INTR_RAW_STAT
- CTRLMMR_MCU_INTR_STAT_CLR
- CTRLMMR_MCU_INTR_EN_SET
- CTRLMMR_MCU_INTR_EN_CLR
- CTRLMMR_MCU_FAULT_ADDR
- CTRLMMR_MCU_FAULT_TYPE
- CTRLMMR_MCU_FAULT_ATTR
- CTRLMMR_MCU_FAULT_CLR

The MCU_PADCFG_CTRL0_CFG0 module also has one interrupt request - the MCU_PADCFG_CTRL0_ACCESS_ERR_0. The interrupt behavior is same as described in Section 5.1.1.3.1.5 . For more details, refer to that section. When reading replace the corresponding registers with the following:

- PADMMR_MCU_INTR_RAW_STAT
- PADMMR_MCU_INTR_STAT_CLR
- PADMMR_MCU_INTR_EN_SET
- PADMMR_MCU_INTR_EN_CLR
- PADMMR_MCU_FAULT_ADDR
- PADMMR_MCU_FAULT_TYPE
- PADMMR_MCU_FAULT_ATTR
- PADMMR_MCU_FAULT_CLR

5.1.2.3.1.4 Clock Muxing and Division Registers

There are registers within the MCU_CTRL_MMR0 module address space dedicated to clock muxing and division for some device modules. Table 5-19 summarizes these registers. Related information can also be found in Section 5.4 *Clocking*.

Table 5-19. Summary of the MCU_CTRL_MMR0 Clock Muxing and Division Registers

Register Name	Register Name
CTRLMMR_MCU_M4FSS_CLKSEL	CTRLMMR_MCU_TIMER3_CLKSEL
CTRLMMR_MCU_PLL_CLKSEL	CTRLMMR_MCU_SPI0_CLKSEL
CTRLMMR_MCU_TIMER0_CLKSEL	CTRLMMR_MCU_SPI1_CLKSEL
CTRLMMR_MCU_TIMER1_CLKSEL	CTRLMMR_MCU_WWD0_CLKSEL
CTRLMMR_MCU_TIMER2_CLKSEL	

5.1.2.3.1.5 I/O Debounce Control Registers

Some device pads have debounce logic. The following MCU_CTRL_MMR0 registers are used to configure the debounce period:

- CTRLMMR_MCU_DBOUNCE_CFG1
- CTRLMMR_MCU_DBOUNCE_CFG2
- CTRLMMR_MCU_DBOUNCE_CFG3
- CTRLMMR_MCU_DBOUNCE_CFG4
- CTRLMMR_MCU_DBOUNCE_CFG5
- CTRLMMR_MCU_DBOUNCE_CFG6

The CTRLMMR_MCU_DBOUNCE_CFG1 register contains the debounce period for pads with PADCONFIGx[13-11] DEBOUNCE_SEL fields set to 1h. The CTRLMMR_MCU_DBOUNCE_CFG2 register contains the debounce period for pads with PADCONFIGx[13-11] DEBOUNCE_SEL fields set to 2h and so on. The CTRLMMR_MCU_DBOUNCE_CFG6 register contains the debounce period for pads with PADCONFIGx[13-11] DEBOUNCE_SEL fields set to 6h.

Note

The debounce logic is not associated with all signals that can be multiplexed on a pad. Only certain signals can use it.

For information about each signal that has associated debounce logic, see the device Datasheet.

For information about the PADCONFIGx registers, see Section 5.1.2.3.1.1 and Section 5.1.1.3.1.1 .

Table 5-20 shows the debounce period values to load in the CTRLMMR_MCU_DBOUNCE_CFGx[5-0] DB_CFG field.

Note

The debounce clock selection should happen before the consumer of the debounced signals is enabled as the clock multiplexers for the debounce logic are NOT glitch-free.

Table 5-20. Debounce Period Values

CTRLMMR_MCU_DBOUNCE_CFGx[5-0] DB_CFG Decimal Value	GPIO Case (32.768 kHz(1))	EQEP Case (25 MHz(1))	CTRLMMR_MCU_DBOUNCE_CFGx[5-0] DB_CFG Decimal Value	GPIO Case (25 MHz(1))	EQEP Case (250 MHz(1))
	Delay[ms]	**Delay[µs]**		**Delay[µs]**	**Delay[ns]**
0	bypassed	bypassed	32	0.04	4
1	1.95	2.56	33	0.08	8
2	2.93	3.84	34	0.12	12
3	3.91	5.12	35	0.16	16
4	4.88	6.40	36	0.20	20
5	5.86	7.68	37	0.24	24
6	6.84	8.96	38	0.28	28
7	7.81	10.24	39	0.32	32
8	8.79	11.52	40	0.36	36
9	9.77	12.80	41	0.40	40
10	10.74	14.08	42	0.44	44
11	11.72	15.36	43	0.48	48
12	12.7	16.64	44	0.52	52
13	13.67	17.92	45	0.56	56
14	14.65	19.20	46	0.60	60
15	15.63	20.48	47	0.64	64
16	16.6	21.76	48	0.68	68
17	17.58	23.04	49	0.72	72
18	18.55	24.32	50	0.76	76
19	19.53	25.60	51	0.80	80
20	20.51	26.88	52	0.84	84
21	21.48	28.16	53	0.88	88
	Delay [ms]	Delay[µs]		Delay[µs]	Delay[µs]
22	15.63	20.48	54	20.48	2.048
23	31.25	40.96	55	40.96	4.096
24	46.88	61.44	56	61.44	6.144
25	62.5	81.92	57	81.92	8.192
26	78.13	102.40	58	102.40	10.24
27	93.75	122.88	59	122.88	12.288
28	109.38	143.36	60	143.36	14.336
29	125	163.84	61	163.84	16.384
30	140.63	184.32	62	184.32	18.432
31	156.25	204.80	63	204.80	20.48

(1) These are the debounce logic clock frequencies.

5.1.2.3.1.6 PRG Related Registers

The following are the PRG related registers within the MCU_CTRL_MMR0 module address space:

- CTRLMMR_MCU_PRG_PP_0_CTRL
- CTRLMMR_MCU_PRG_PP_0_STAT
- CTRLMMR_MCU_PRG_PP_1_CTRL
- CTRLMMR_MCU_PRG_PP_1_STAT

5.1.2.3.1.7 POK Module Registers

Table 5-21 summarizes the registers associated with the device POK modules.

Table 5-21. Summary of the POK Registers

Register Name	Register Name
CTRLMMR_MCU_POK_VDDA_MCU_UV_CTRL	CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_UV_CTRL
CTRLMMR_MCU_POK_VDDA_MCU_OV_CTRL	CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_OV_CTRL
CTRLMMR_MCU_POK_VDD_CORE_UV_CTRL	CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_UV_CTRL
CTRLMMR_MCU_POK_VDD_CORE_OV_CTRL	CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_OV_CTRL
CTRLMMR_MCU_POK_VDDR_CORE_UV_CTRL	CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_UV_CTRL
CTRLMMR_MCU_POK_VDDR_CORE_OV_CTRL	CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_OV_CTRL
CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_UV_CTRL	CTRLMMR_MCU_POK_VDDS_DDRIO_UV_CTRL
CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_OV_CTRL	CTRLMMR_MCU_POK_VDDS_DDRIO_OV_CTRL
CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_UV_CTRL	CTRLMMR_MCU_POK_VDDA_PMIC_IN_CTRL
CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_OV_CTRL	

5.1.2.4 MCU_PADCFG_CTRL0_CFG0 Registers

Table 5-23 lists the memory-mapped registers for the MCU_PADCFG_CTRL0_CFG0. All register offset addresses not listed in Table 5-23 should be considered as reserved locations and the register contents should not be modified.

Table 5-22. MCU_PADCFG_CTRL0_CFG0 Instances

Instance	Base Address
MCU_PADCFG_CTRL0_CFG0	0408 0000h

Table 5-23. MCU_PADCFG_CTRL0_CFG0 Registers

Offset	Acronym	Register Name	MCU_PADCFG_CTRL0_CFG0 Physical Address
0h	PADMMR_MCU_PID	Peripheral Identification Register	0408 0000h
8h	PADMMR_MCU_MMR_CFG1	Configuration register 1	0408 0008h
1008h	PADMMR_MCU_LOCK0_KICK0	Partition 0 Lock Key 0 Register	0408 1008h
100Ch	PADMMR_MCU_LOCK0_KICK1	Partition 0 Lock Key 1 Register	0408 100Ch
1010h	PADMMR_MCU_INTR_RAW_STAT	Interrupt Raw Status Register	0408 1010h
1014h	PADMMR_MCU_INTR_STAT_CLR	Interrupt Status and Clear Register	0408 1014h
1018h	PADMMR_MCU_INTR_EN_SET	Interrupt Enable Set Register	0408 1018h
101Ch	PADMMR_MCU_INTR_EN_CLR	Interrupt Enable Clear Register	0408 101Ch
1020h	PADMMR_MCU_EOI	End of Interrupt Register	0408 1020h
1024h	PADMMR_MCU_FAULT_ADDR	Fault Address Register	0408 1024h
1028h	PADMMR_MCU_FAULT_TYPE	Fault Type Register	0408 1028h
102Ch	PADMMR_MCU_FAULT_ATTR	Fault Attribute Register	0408 102Ch
1030h	PADMMR_MCU_FAULT_CLR	Fault Clear Register	0408 1030h
4000h	PADMMR_MCU_PADCONFIG0	PAD Configuration Register 0	0408 4000h
4004h	PADMMR_MCU_PADCONFIG1	PAD Configuration Register 1	0408 4004h
4008h	PADMMR_MCU_PADCONFIG2	PAD Configuration Register 2	0408 4008h
400Ch	PADMMR_MCU_PADCONFIG3	PAD Configuration Register 3	0408 400Ch
4010h	PADMMR_MCU_PADCONFIG4	PAD Configuration Register 4	0408 4010h
4014h	PADMMR_MCU_PADCONFIG5	PAD Configuration Register 5	0408 4014h
4018h	PADMMR_MCU_PADCONFIG6	PAD Configuration Register 6	0408 4018h
401Ch	PADMMR_MCU_PADCONFIG7	PAD Configuration Register 7	0408 401Ch
4020h	PADMMR_MCU_PADCONFIG8	PAD Configuration Register 8	0408 4020h
4024h	PADMMR_MCU_PADCONFIG9	PAD Configuration Register 9	0408 4024h
4028h	PADMMR_MCU_PADCONFIG10	PAD Configuration Register 10	0408 4028h
402Ch	PADMMR_MCU_PADCONFIG11	PAD Configuration Register 11	0408 402Ch
4030h	PADMMR_MCU_PADCONFIG12	PAD Configuration Register 12	0408 4030h
4034h	PADMMR_MCU_PADCONFIG13	PAD Configuration Register 13	0408 4034h
4038h	PADMMR_MCU_PADCONFIG14	PAD Configuration Register 14	0408 4038h
403Ch	PADMMR_MCU_PADCONFIG15	PAD Configuration Register 15	0408 403Ch
4040h	PADMMR_MCU_PADCONFIG16	PAD Configuration Register 16	0408 4040h
4044h	PADMMR_MCU_PADCONFIG17	PAD Configuration Register 17	0408 4044h
4048h	PADMMR_MCU_PADCONFIG18	PAD Configuration Register 18	0408 4048h
404Ch	PADMMR_MCU_PADCONFIG19	PAD Configuration Register 19	0408 404Ch
4050h	PADMMR_MCU_PADCONFIG20	PAD Configuration Register 20	0408 4050h
4054h	PADMMR_MCU_PADCONFIG21	PAD Configuration Register 21	0408 4054h

Table 5-23. MCU_PADCFG_CTRL0_CFG0 Registers (continued)

Offset	Acronym	Register Name	MCU_PADCFG_CTRL0_CFG0 Physical Address
4058h	PADMMR_MCU_PADCONFIG22	PAD Configuration Register 22	0408 4058h
405Ch	PADMMR_MCU_PADCONFIG23	PAD Configuration Register 23	0408 405Ch
4060h	PADMMR_MCU_PADCONFIG24	PAD Configuration Register 24	0408 4060h
4064h	PADMMR_MCU_PADCONFIG25	PAD Configuration Register 25	0408 4064h
4068h	PADMMR_MCU_PADCONFIG26	PAD Configuration Register 26	0408 4068h
406Ch	PADMMR_MCU_PADCONFIG27	PAD Configuration Register 27	0408 406Ch
4070h	PADMMR_MCU_PADCONFIG28	PAD Configuration Register 28	0408 4070h
4074h	PADMMR_MCU_PADCONFIG29	PAD Configuration Register 29	0408 4074h
4078h	PADMMR_MCU_PADCONFIG30	PAD Configuration Register 30	0408 4078h
407Ch	PADMMR_MCU_PADCONFIG31	PAD Configuration Register 31	0408 407Ch
4080h	PADMMR_MCU_PADCONFIG32	PAD Configuration Register 32	0408 4080h
5008h	PADMMR_MCU_LOCK1_KICK0	Partition 1 Lock Key 0 Register	0408 5008h
500Ch	PADMMR_MCU_LOCK1_KICK1	Partition 1 Lock Key 1 Register	0408 500Ch

1 PADMMR_MCU_PID Register (Offset = 0h) [reset = 61800000h]

PADMMR_MCU_PID is shown in Figure 5-3 and described in Table 5-25.

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Peripheral release details.

Table 5-24. PADMMR_MCU_PID Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 0000h

Figure 5-3. PADMMR_MCU_PID Register

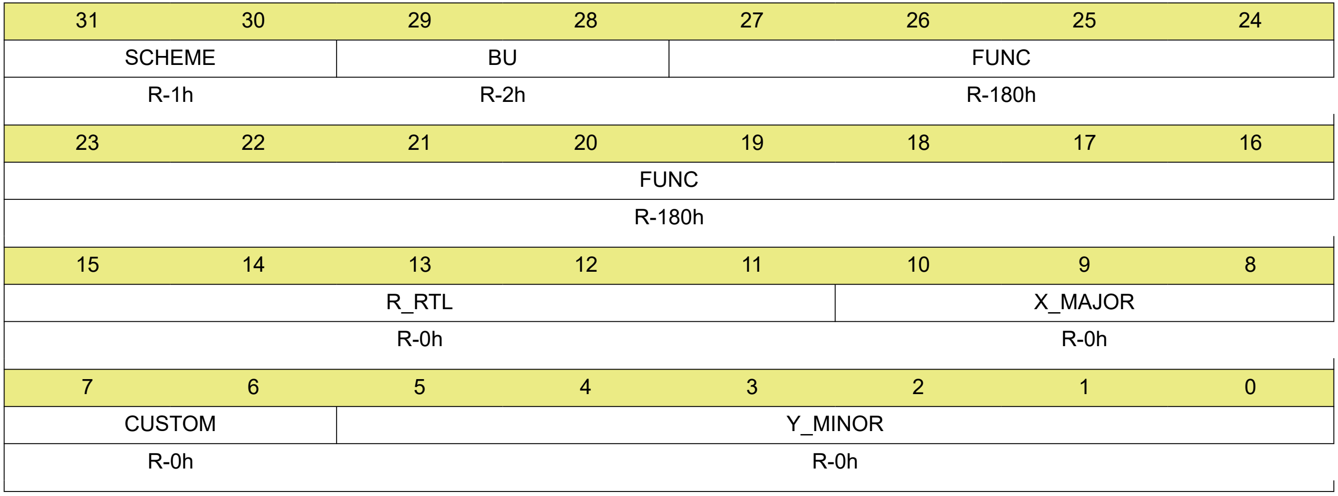

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R-1h		R-2h		R-180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R-180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_RTL					X_MAJOR		
R-0h					R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		Y_MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 5-26. PADMMR_MCU_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PADMMR_MCU_PID follows new scheme
29-28	BU	R	2h	Business unit - Processors
27-16	FUNC	R	180h	Module functional identifier - CTRL MMR
15-11	R_RTL	R	0h	RTL revision number
10-8	X_MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	Custom revision number
5-0	Y_MINOR	R	0h	Minor revision number

2 PADMMR_MCU_MMR_CFG1 Register (Offset = 8h) [reset = 800000BFh]

PADMMR_MCU_MMR_CFG1 is shown in Figure 5-4 and described in Table 5-27.

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Indicates the MMR configuration.

Table 5-27. PADMMR_MCU_MMR_CFG1 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 0008h

Figure 5-4. PADMMR_MCU_MMR_CFG1 Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PARTITIONS							
R-BFh							

LEGEND: R = Read Only; -*n* = value after reset

Table 5-29. PADMMR_MCU_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	1h	Reserved
30-8	RESERVED	R	0h	Reserved
7-0	PARTITIONS	R	BFh	Indicates present partitions

3 PADMMR_MCU_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

PADMMR_MCU_LOCK0_KICK0 is shown in Figure 5-5 and described in Table 5-29.

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Lower 32-bits of Partition0 write lock key. This register must be written with the designated key value followed by a write to PADMMR_MCU_LOCK0_KICK1 with its key value before write-protected Partition 0 registers can be written.

Table 5-30. PADMMR_MCU_LOCK0_KICK0 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 1008h

Figure 5-5. PADMMR_MCU_LOCK0_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-32. PADMMR_MCU_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

4 PADMMR_MCU_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

PADMMR_MCU_LOCK0_KICK1 is shown in Figure 5-6 and described in Table 5-31.

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Upper 32-bits of Partition 0 write lock key. This register must be written with the designated key value after a write to PADMMR_MCU_LOCK0_KICK0 with its key value before write-protected Partition 0 registers can be written.

Table 5-33. PADMMR_MCU_LOCK0_KICK1 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 100Ch

Figure 5-6. PADMMR_MCU_LOCK0_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 5-35. PADMMR_MCU_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers

5 PADMMR_MCU_INTR_RAW_STAT Register (Offset = 1010h) [reset = 0h]

PADMMR_MCU_INTR_RAW_STAT is shown in Figure 5-7 and described in Table 5-33.

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Shows the interrupt status (before enabling) and allows setting of the interrupt status (for test).

Table 5-36. PADMMR_MCU_INTR_RAW_STAT Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 1010h

Figure 5-7. PADMMR_MCU_INTR_RAW_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED				RESERVED	LOCK_ERR	ADDR_ERR	PROT_ERR
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 5-38. PADMMR_MCU_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RESERVED	W1TS	0h	Reserved
2	LOCK_ERR	W1TS	0h	Lock violation occurred (attempt to write a write-locked register with partition locked) Write 1 to set the status bit (for test) Writing 0 has no effect.
1	ADDR_ERR	W1TS	0h	Address violation occurred (attempt to read or write an invalid register address) Write 1 to set the status bit (for test) Writing 0 has no effect.
0	PROT_ERR	W1TS	0h	Protection violation occurred (attempt to read or write a register with insufficient security or privilege access rights) Write 1 to set the status bit (for test) Writing 0 has no effect.

6 PADMMR_MCU_INTR_STAT_CLR Register (Offset = 1014h) [reset = 0h]

PADMMR_MCU_INTR_STAT_CLR is shown in Figure 5-8 and described in Table 5-35.

Return to Summary Table.

Shows the enabled interrupt status and allows the interrupt to be cleared.

Table 5-39. PADMMR_MCU_INTR_STAT_CLR Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 1014h

Figure 5-8. PADMMR_MCU_INTR_STAT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	EN_LOCK_ERR	EN_ADDR_ERR	EN_PROT_ERR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; -*n* = value after reset

Table 5-41. PADMMR_MCU_INTR_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RESERVED	W1TC	0h	Reserved
2	EN_LOCK_ERR	W1TC	0h	Enabled lock interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
1	EN_ADDR_ERR	W1TC	0h	Enabled address interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
0	EN_PROT_ERR	W1TC	0h	Enabled protection interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.

7 PADMMR_MCU_INTR_EN_SET Register (Offset = 1018h) [reset = 0h]

PADMMR_MCU_INTR_EN_SET is shown in Figure 5-9 and described in Table 5-37.

Return to Summary Table.

Allows interrupt enables to be set.

Table 5-42. PADMMR_MCU_INTR_EN_SET Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 1018h

Figure 5-9. PADMMR_MCU_INTR_EN_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	LOCK_ERR_EN_SET	ADDR_ERR_EN_SET	PROT_ERR_EN_SET
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 5-44. PADMMR_MCU_INTR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RESERVED	W1TS	0h	Reserved
2	LOCK_ERR_EN_SET	W1TS	0h	Lock interrupt enable Write 1 to enable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_SET	W1TS	0h	Address interrupt enable Write 1 to enable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_SET	W1TS	0h	Protection interrupt enable Write 1 to enable protection interrupt events Writing 0 has no effect.

8 PADMMR_MCU_INTR_EN_CLR Register (Offset = 101Ch) [reset = 0h]

PADMMR_MCU_INTR_EN_CLR is shown in Figure 5-10 and described in Table 5-39.

Return to Summary Table.

Allows interrupt enables to be cleared.

Table 5-45. PADMMR_MCU_INTR_EN_CLR Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 101Ch

Figure 5-10. PADMMR_MCU_INTR_EN_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	LOCK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; -*n* = value after reset

Table 5-47. PADMMR_MCU_INTR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RESERVED	W1TC	0h	Reserved
2	LOCK_ERR_EN_CLR	W1TC	0h	Lock interrupt disable Write 1 to disable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_CLR	W1TC	0h	Address interrupt disable Write 1 to disable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_CLR	W1TC	0h	Protection interrupt disable Write 1 to disable protection interrupt events Writing 0 has no effect.

9 PADMMR_MCU_EOI Register (Offset = 1020h) [reset = 0h]

PADMMR_MCU_EOI is shown in Figure 5-11 and described in Table 5-41.

Return to Summary Table.

PADMMR_MCU_EOI Vector value This register should be written with interrupt distribution value required by the device architecture to indicate service completion of the MMR interrupt.

Table 5-48. PADMMR_MCU_EOI Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 1020h

Figure 5-11. PADMMR_MCU_EOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VECTOR							
R-0h																								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-50. PADMMR_MCU_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VECTOR	R/W	0h	PADMMR_MCU_EOI vector value

10 PADMMR_MCU_FAULT_ADDR Register (Offset = 1024h) [reset = 0h]

PADMMR_MCU_FAULT_ADDR is shown in Figure 5-12 and described in Table 5-43.

Return to Summary Table.

Indicates the address of the first transfer that caused a fault to occur.

Table 5-51. PADMMR_MCU_FAULT_ADDR Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 1024h

Figure 5-12. PADMMR_MCU_FAULT_ADDR Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">ADDRESS</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 5-53. PADMMR_MCU_FAULT_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Address of the faulted access

11 PADMMR_MCU_FAULT_TYPE Register (Offset = 1028h) [reset = 0h]

PADMMR_MCU_FAULT_TYPE is shown in Figure 5-13 and described in Table 5-45.

Return to Summary Table.

Indicates the access type of the first transfer that caused a fault to occur.

Table 5-54. PADMMR_MCU_FAULT_TYPE Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 1028h

Figure 5-13. PADMMR_MCU_FAULT_TYPE Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="26">RESERVED</td><td colspan="6">TYPE</td></tr>
<tr><td colspan="26">R-0h</td><td colspan="6">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 5-56. PADMMR_MCU_FAULT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	TYPE	R	0h	Type of access which faulted 0h - No fault 1h - User execute access 2h - User write access 4h - User read access 8h - Supervisor execute access 10h - Supervisor write access 20h - Supervisor read access

12 PADMMR_MCU_FAULT_ATTR Register (Offset = 102Ch) [reset = 0h]

PADMMR_MCU_FAULT_ATTR is shown in Figure 5-14 and described in Table 5-47.

Return to Summary Table.

Indicates the attributes of the first transfer that caused a fault to occur.

Table 5-57. PADMMR_MCU_FAULT_ATTR Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 102Ch

Figure 5-14. PADMMR_MCU_FAULT_ATTR Register

31	30	29	28	27	26	25	24
XID							
R-0h							
23	22	21	20	19	18	17	16
XID				ROUTEID			
R-0h				R-0h			
15	14	13	12	11	10	9	8
ROUTEID							
R-0h							
7	6	5	4	3	2	1	0
PRIVID							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 5-59. PADMMR_MCU_FAULT_ATTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	XID	R	0h	Transaction ID
19-8	ROUTEID	R	0h	Route ID
7-0	PRIVID	R	0h	Privilege ID

13 PADMMR_MCU_FAULT_CLR Register (Offset = 1030h) [reset = 0h]

PADMMR_MCU_FAULT_CLR is shown in Figure 5-15 and described in Table 5-49.

Return to Summary Table.

Allows software to clear the current fault Clearing the current fault allows the PADMMR_MCU_FAULT_ADDR, PADMMR_MCU_FAULT_TYPE, and PADMMR_MCU_FAULT_ATTR registers to latch the attributes of the next fault that occurs. This does not affect the fault interrupt event itself. The interrupt must be cleared using the appropriate INTR_STATUS_CLR register bits.

Table 5-60. PADMMR_MCU_FAULT_CLR Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 1030h

Figure 5-15. PADMMR_MCU_FAULT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLEAR
R-0h							W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; -*n* = value after reset

Table 5-62. PADMMR_MCU_FAULT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLEAR	W1TC	0h	Fault clear Write 1 to clear the current fault Writing 0 has no effect

14 PADMMR_MCU_PADCONFIG0 Register (Offset = 4000h) [reset = 214007h]

PADMMR_MCU_PADCONFIG0 is shown in Figure 5-16 and described in Table 5-51.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-63. PADMMR_MCU_PADCONFIG0 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4000h

Figure 5-16. PADMMR_MCU_PADCONFIG0 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-65. PADMMR_MCU_PADCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-65. PADMMR_MCU_PADCONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

15 PADMMR_MCU_PADCONFIG1 Register (Offset = 4004h) [reset = 214007h]

PADMMR_MCU_PADCONFIG1 is shown in Figure 5-17 and described in Table 5-53.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-66. PADMMR_MCU_PADCONFIG1 Instances

Instance	**Physical Address**
MCU_PADCFG_CTRL0_CFG0	0408 4004h

Figure 5-17. PADMMR_MCU_PADCONFIG1 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-68. PADMMR_MCU_PADCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-68. PADMMR_MCU_PADCONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

16 PADMMR_MCU_PADCONFIG2 Register (Offset = 4008h) [reset = 214007h]

PADMMR_MCU_PADCONFIG2 is shown in Figure 5-18 and described in Table 5-55.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-69. PADMMR_MCU_PADCONFIG2 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4008h

Figure 5-18. PADMMR_MCU_PADCONFIG2 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-71. PADMMR_MCU_PADCONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-71. PADMMR_MCU_PADCONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

17 PADMMR_MCU_PADCONFIG3 Register (Offset = 400Ch) [reset = 214007h]

PADMMR_MCU_PADCONFIG3 is shown in Figure 5-19 and described in Table 5-57.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-72. PADMMR_MCU_PADCONFIG3 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 400Ch

Figure 5-19. PADMMR_MCU_PADCONFIG3 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-74. PADMMR_MCU_PADCONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-74. PADMMR_MCU_PADCONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

18 PADMMR_MCU_PADCONFIG4 Register (Offset = 4010h) [reset = 214007h]

PADMMR_MCU_PADCONFIG4 is shown in Figure 5-20 and described in Table 5-59.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-75. PADMMR_MCU_PADCONFIG4 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4010h

Figure 5-20. PADMMR_MCU_PADCONFIG4 Register

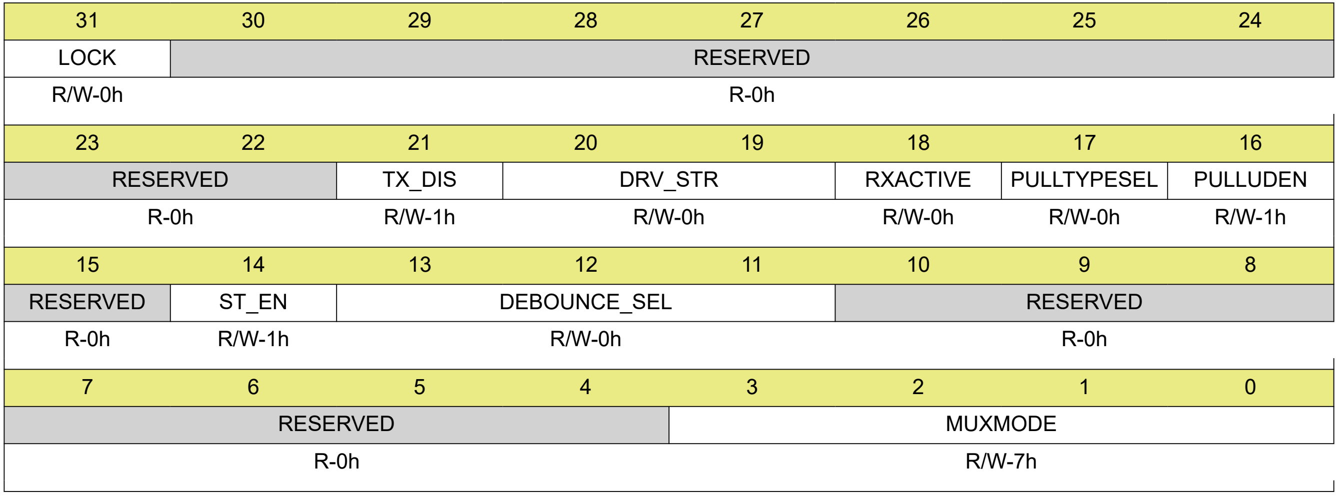

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-77. PADMMR_MCU_PADCONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-77. PADMMR_MCU_PADCONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

19 PADMMR_MCU_PADCONFIG5 Register (Offset = 4014h) [reset = 214007h]

PADMMR_MCU_PADCONFIG5 is shown in Figure 5-21 and described in Table 5-61.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-78. PADMMR_MCU_PADCONFIG5 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4014h

Figure 5-21. PADMMR_MCU_PADCONFIG5 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-80. PADMMR_MCU_PADCONFIG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-80. PADMMR_MCU_PADCONFIG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

20 PADMMR_MCU_PADCONFIG6 Register (Offset = 4018h) [reset = 214007h]

PADMMR_MCU_PADCONFIG6 is shown in Figure 5-22 and described in Table 5-63.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-81. PADMMR_MCU_PADCONFIG6 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4018h

Figure 5-22. PADMMR_MCU_PADCONFIG6 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-83. PADMMR_MCU_PADCONFIG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-83. PADMMR_MCU_PADCONFIG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

21 PADMMR_MCU_PADCONFIG7 Register (Offset = 401Ch) [reset = 214007h]

PADMMR_MCU_PADCONFIG7 is shown in Figure 5-23 and described in Table 5-65.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-84. PADMMR_MCU_PADCONFIG7 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 401Ch

Figure 5-23. PADMMR_MCU_PADCONFIG7 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-86. PADMMR_MCU_PADCONFIG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-86. PADMMR_MCU_PADCONFIG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

22 PADMMR_MCU_PADCONFIG8 Register (Offset = 4020h) [reset = 214007h]

PADMMR_MCU_PADCONFIG8 is shown in Figure 5-24 and described in Table 5-67.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-87. PADMMR_MCU_PADCONFIG8 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4020h

Figure 5-24. PADMMR_MCU_PADCONFIG8 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-89. PADMMR_MCU_PADCONFIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-89. PADMMR_MCU_PADCONFIG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

23 PADMMR_MCU_PADCONFIG9 Register (Offset = 4024h) [reset = 214007h]

PADMMR_MCU_PADCONFIG9 is shown in Figure 5-25 and described in Table 5-69.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-90. PADMMR_MCU_PADCONFIG9 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4024h

Figure 5-25. PADMMR_MCU_PADCONFIG9 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-92. PADMMR_MCU_PADCONFIG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-92. PADMMR_MCU_PADCONFIG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

24 PADMMR_MCU_PADCONFIG10 Register (Offset = 4028h) [reset = 214007h]

PADMMR_MCU_PADCONFIG10 is shown in Figure 5-26 and described in Table 5-71.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-93. PADMMR_MCU_PADCONFIG10 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4028h

Figure 5-26. PADMMR_MCU_PADCONFIG10 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-95. PADMMR_MCU_PADCONFIG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-95. PADMMR_MCU_PADCONFIG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

25 PADMMR_MCU_PADCONFIG11 Register (Offset = 402Ch) [reset = 214007h]

PADMMR_MCU_PADCONFIG11 is shown in Figure 5-27 and described in Table 5-73.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-96. PADMMR_MCU_PADCONFIG11 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 402Ch

Figure 5-27. PADMMR_MCU_PADCONFIG11 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-98. PADMMR_MCU_PADCONFIG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-98. PADMMR_MCU_PADCONFIG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

26 PADMMR_MCU_PADCONFIG12 Register (Offset = 4030h) [reset = 214007h]

PADMMR_MCU_PADCONFIG12 is shown in Figure 5-28 and described in Table 5-75.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-99. PADMMR_MCU_PADCONFIG12 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4030h

Figure 5-28. PADMMR_MCU_PADCONFIG12 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-101. PADMMR_MCU_PADCONFIG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-101. PADMMR_MCU_PADCONFIG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

27 PADMMR_MCU_PADCONFIG13 Register (Offset = 4034h) [reset = 214007h]

PADMMR_MCU_PADCONFIG13 is shown in Figure 5-29 and described in Table 5-77.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-102. PADMMR_MCU_PADCONFIG13 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4034h

Figure 5-29. PADMMR_MCU_PADCONFIG13 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-104. PADMMR_MCU_PADCONFIG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-104. PADMMR_MCU_PADCONFIG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

28 PADMMR_MCU_PADCONFIG14 Register (Offset = 4038h) [reset = 214007h]

PADMMR_MCU_PADCONFIG14 is shown in Figure 5-30 and described in Table 5-79.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-105. PADMMR_MCU_PADCONFIG14 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4038h

Figure 5-30. PADMMR_MCU_PADCONFIG14 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-107. PADMMR_MCU_PADCONFIG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-107. PADMMR_MCU_PADCONFIG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

29 PADMMR_MCU_PADCONFIG15 Register (Offset = 403Ch) [reset = 214007h]

PADMMR_MCU_PADCONFIG15 is shown in Figure 5-31 and described in Table 5-81.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-108. PADMMR_MCU_PADCONFIG15 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 403Ch

Figure 5-31. PADMMR_MCU_PADCONFIG15 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-110. PADMMR_MCU_PADCONFIG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-110. PADMMR_MCU_PADCONFIG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

30 PADMMR_MCU_PADCONFIG16 Register (Offset = 4040h) [reset = 214007h]

PADMMR_MCU_PADCONFIG16 is shown in Figure 5-32 and described in Table 5-83.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-111. PADMMR_MCU_PADCONFIG16 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4040h

Figure 5-32. PADMMR_MCU_PADCONFIG16 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-113. PADMMR_MCU_PADCONFIG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-113. PADMMR_MCU_PADCONFIG16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

31 PADMMR_MCU_PADCONFIG17 Register (Offset = 4044h) [reset = 214007h]

PADMMR_MCU_PADCONFIG17 is shown in Figure 5-33 and described in Table 5-85.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-114. PADMMR_MCU_PADCONFIG17 Instances

Instance	**Physical Address**
MCU_PADCFG_CTRL0_CFG0	0408 4044h

Figure 5-33. PADMMR_MCU_PADCONFIG17 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-116. PADMMR_MCU_PADCONFIG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-116. PADMMR_MCU_PADCONFIG17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

32 PADMMR_MCU_PADCONFIG18 Register (Offset = 4048h) [reset = 54007h]

PADMMR_MCU_PADCONFIG18 is shown in Figure 5-34 and described in Table 5-87.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-117. PADMMR_MCU_PADCONFIG18 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4048h

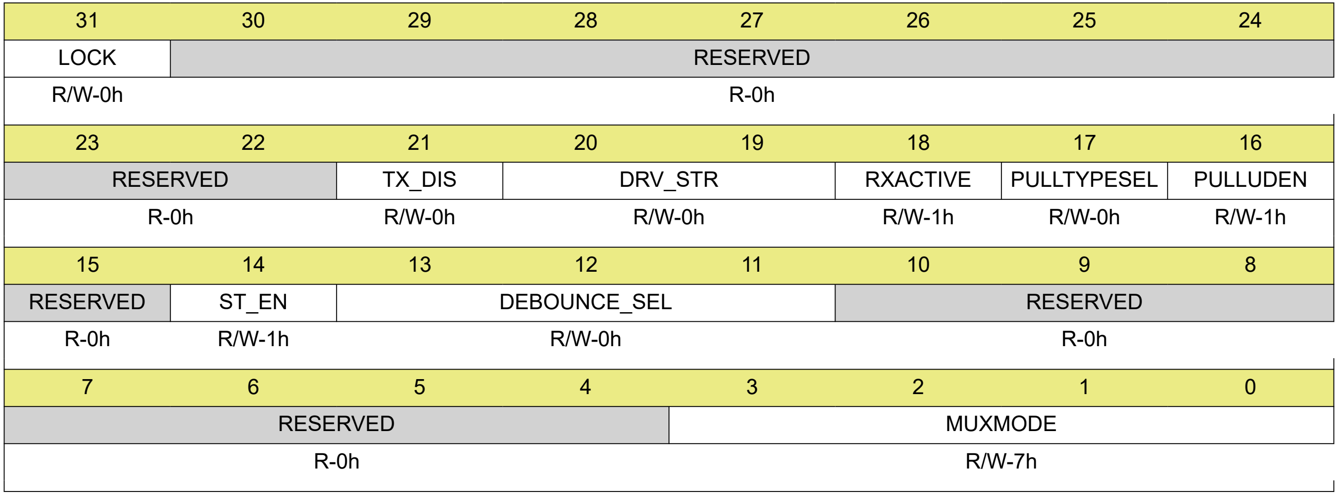

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-0h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

Figure 5-34. PADMMR_MCU_PADCONFIG18 Register

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-119. PADMMR_MCU_PADCONFIG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved

Table 5-119. PADMMR_MCU_PADCONFIG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

33 PADMMR_MCU_PADCONFIG19 Register (Offset = 404Ch) [reset = 54007h]

PADMMR_MCU_PADCONFIG19 is shown in Figure 5-35 and described in Table 5-89.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-120. PADMMR_MCU_PADCONFIG19 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 404Ch

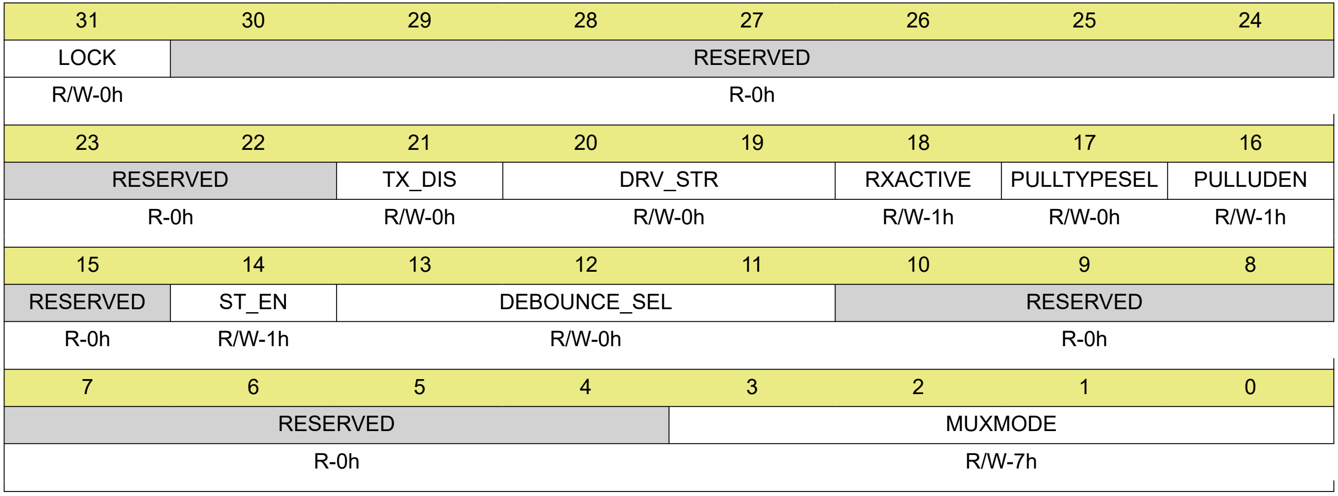

Figure 5-35. PADMMR_MCU_PADCONFIG19 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-0h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-122. PADMMR_MCU_PADCONFIG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15	RESERVED	R	0h	Reserved

Table 5-122. PADMMR_MCU_PADCONFIG19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

34 PADMMR_MCU_PADCONFIG20 Register (Offset = 4050h) [reset = 214007h]

PADMMR_MCU_PADCONFIG20 is shown in Figure 5-36 and described in Table 5-91.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-123. PADMMR_MCU_PADCONFIG20 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4050h

Figure 5-36. PADMMR_MCU_PADCONFIG20 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-125. PADMMR_MCU_PADCONFIG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-125. PADMMR_MCU_PADCONFIG20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

35 PADMMR_MCU_PADCONFIG21 Register (Offset = 4054h) [reset = 214007h]

PADMMR_MCU_PADCONFIG21 is shown in Figure 5-37 and described in Table 5-93.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-126. PADMMR_MCU_PADCONFIG21 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4054h

Figure 5-37. PADMMR_MCU_PADCONFIG21 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-128. PADMMR_MCU_PADCONFIG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-128. PADMMR_MCU_PADCONFIG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

36 PADMMR_MCU_PADCONFIG22 Register (Offset = 4058h) [reset = 264000h]

PADMMR_MCU_PADCONFIG22 is shown in Figure 5-38 and described in Table 5-95.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-129. PADMMR_MCU_PADCONFIG22 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4058h

Figure 5-38. PADMMR_MCU_PADCONFIG22 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-131. PADMMR_MCU_PADCONFIG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-131. PADMMR_MCU_PADCONFIG22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

37 PADMMR_MCU_PADCONFIG23 Register (Offset = 405Ch) [reset = 14000h]

PADMMR_MCU_PADCONFIG23 is shown in Figure 5-39 and described in Table 5-97.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-132. PADMMR_MCU_PADCONFIG23 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 405Ch

Figure 5-39. PADMMR_MCU_PADCONFIG23 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-134. PADMMR_MCU_PADCONFIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-134. PADMMR_MCU_PADCONFIG23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

38 PADMMR_MCU_PADCONFIG24 Register (Offset = 4060h) [reset = 14000h]

PADMMR_MCU_PADCONFIG24 is shown in Figure 5-40 and described in Table 5-99.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-135. PADMMR_MCU_PADCONFIG24 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4060h

Figure 5-40. PADMMR_MCU_PADCONFIG24 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUXMODE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-137. PADMMR_MCU_PADCONFIG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-137. PADMMR_MCU_PADCONFIG24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

39 PADMMR_MCU_PADCONFIG25 Register (Offset = 4064h) [reset = 44000h]

PADMMR_MCU_PADCONFIG25 is shown in Figure 5-41 and described in Table 5-101.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-138. PADMMR_MCU_PADCONFIG25 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4064h

Figure 5-41. PADMMR_MCU_PADCONFIG25 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>TX_DIS</td><td colspan="2">DRV_STR</td><td>RXACTIVE</td><td>PULLTYPESEL</td><td>PULLUDEN</td></tr>
<tr><td colspan="2">R-0h</td><td>R/W-0h</td><td colspan="2">R/W-0h</td><td>R/W-1h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>ST_EN</td><td colspan="3">DEBOUNCE_SEL</td><td colspan="3">RESERVED</td></tr>
<tr><td>R-0h</td><td>R/W-1h</td><td colspan="3">R/W-0h</td><td colspan="3">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MUXMODE</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-140. PADMMR_MCU_PADCONFIG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-140. PADMMR_MCU_PADCONFIG25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

40 PADMMR_MCU_PADCONFIG26 Register (Offset = 4068h) [reset = 264000h]

PADMMR_MCU_PADCONFIG26 is shown in Figure 5-42 and described in Table 5-103.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-141. PADMMR_MCU_PADCONFIG26 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4068h

Figure 5-42. PADMMR_MCU_PADCONFIG26 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUXMODE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-143. PADMMR_MCU_PADCONFIG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-143. PADMMR_MCU_PADCONFIG26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

41 PADMMR_MCU_PADCONFIG27 Register (Offset = 406Ch) [reset = 244000h]

PADMMR_MCU_PADCONFIG27 is shown in Figure 5-43 and described in Table 5-105.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-144. PADMMR_MCU_PADCONFIG27 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 406Ch

Figure 5-43. PADMMR_MCU_PADCONFIG27 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>TX_DIS</td><td colspan="2">DRV_STR</td><td>RXACTIVE</td><td>PULLTYPESEL</td><td>PULLUDEN</td></tr>
<tr><td colspan="2">R-0h</td><td>R/W-1h</td><td colspan="2">R/W-0h</td><td>R/W-1h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>ST_EN</td><td colspan="3">DEBOUNCE_SEL</td><td colspan="3">RESERVED</td></tr>
<tr><td>R-0h</td><td>R/W-1h</td><td colspan="3">R/W-0h</td><td colspan="3">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MUXMODE</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-146. PADMMR_MCU_PADCONFIG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-146. PADMMR_MCU_PADCONFIG27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

42 PADMMR_MCU_PADCONFIG28 Register (Offset = 4070h) [reset = 264000h]

PADMMR_MCU_PADCONFIG28 is shown in Figure 5-44 and described in Table 5-107.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-147. PADMMR_MCU_PADCONFIG28 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4070h

Figure 5-44. PADMMR_MCU_PADCONFIG28 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-149. PADMMR_MCU_PADCONFIG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-149. PADMMR_MCU_PADCONFIG28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

43 PADMMR_MCU_PADCONFIG29 Register (Offset = 4074h) [reset = 24000h]

PADMMR_MCU_PADCONFIG29 is shown in Figure 5-45 and described in Table 5-109.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-150. PADMMR_MCU_PADCONFIG29 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4074h

Figure 5-45. PADMMR_MCU_PADCONFIG29 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-0h	R/W-0h		R/W-0h	R/W-1h	R/W-0h

15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-152. PADMMR_MCU_PADCONFIG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-152. PADMMR_MCU_PADCONFIG29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

44 PADMMR_MCU_PADCONFIG30 Register (Offset = 4078h) [reset = 264000h]

PADMMR_MCU_PADCONFIG30 is shown in Figure 5-46 and described in Table 5-111.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-153. PADMMR_MCU_PADCONFIG30 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4078h

Figure 5-46. PADMMR_MCU_PADCONFIG30 Register

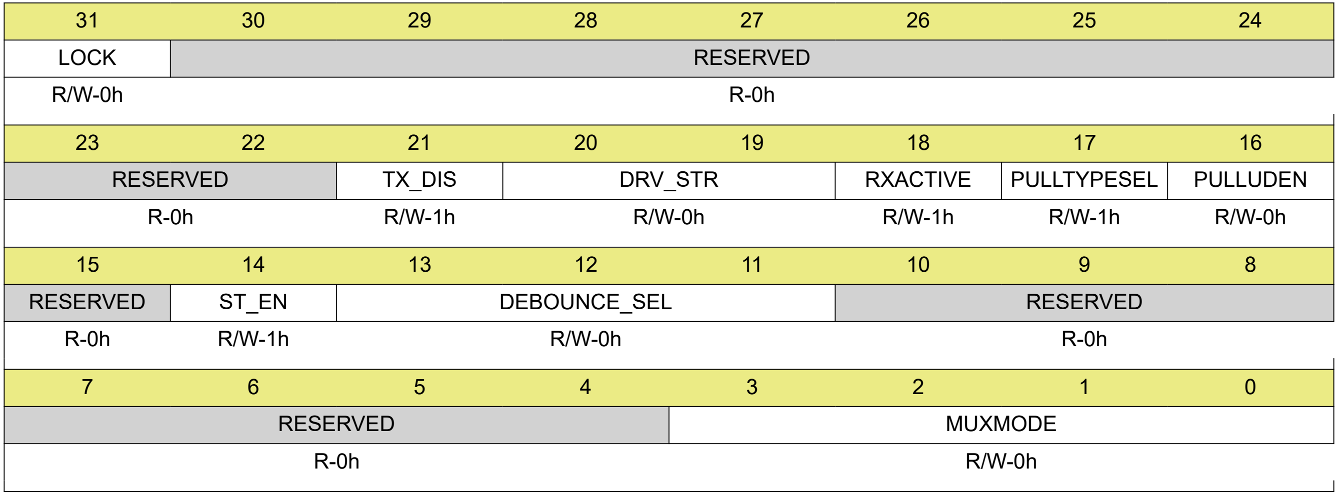

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUXMODE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-155. PADMMR_MCU_PADCONFIG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-155. PADMMR_MCU_PADCONFIG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

45 PADMMR_MCU_PADCONFIG31 Register (Offset = 407Ch) [reset = 264000h]

PADMMR_MCU_PADCONFIG31 is shown in Figure 5-47 and described in Table 5-113.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-156. PADMMR_MCU_PADCONFIG31 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 407Ch

Figure 5-47. PADMMR_MCU_PADCONFIG31 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED		TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R-0h		R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	ST_EN	DEBOUNCE_SEL			RESERVED		
R-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED				MUXMODE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-158. PADMMR_MCU_PADCONFIG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-158. PADMMR_MCU_PADCONFIG31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

46 PADMMR_MCU_PADCONFIG32 Register (Offset = 4080h) [reset = 264000h]

PADMMR_MCU_PADCONFIG32 is shown in Figure 5-48 and described in Table 5-115.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 5-159. PADMMR_MCU_PADCONFIG32 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 4080h

Figure 5-48. PADMMR_MCU_PADCONFIG32 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>TX_DIS</td><td colspan="2">DRV_STR</td><td>RXACTIVE</td><td>PULLTYPESEL</td><td>PULLUDEN</td></tr>
<tr><td colspan="2">R-0h</td><td>R/W-1h</td><td colspan="2">R/W-0h</td><td>R/W-1h</td><td>R/W-1h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>ST_EN</td><td colspan="3">DEBOUNCE_SEL</td><td colspan="3">RESERVED</td></tr>
<tr><td>R-0h</td><td>R/W-1h</td><td colspan="3">R/W-0h</td><td colspan="3">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MUXMODE</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-161. PADMMR_MCU_PADCONFIG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-22	RESERVED	R	0h	Reserved
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected

Table 5-161. PADMMR_MCU_PADCONFIG32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-4	RESERVED	R	0h	Reserved
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

47 PADMMR_MCU_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

PADMMR_MCU_LOCK1_KICK0 is shown in Figure 5-49 and described in Table 5-117.

Return to Summary Table.

Lower 32-bits of Partition1 write lock key. This register must be written with the designated key value followed by a write to PADMMR_MCU_LOCK1_KICK1 with its key value before write-protected Partition 1 registers can be written.

Table 5-162. PADMMR_MCU_LOCK1_KICK0 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 5008h

Figure 5-49. PADMMR_MCU_LOCK1_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 5-164. PADMMR_MCU_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

48 PADMMR_MCU_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

PADMMR_MCU_LOCK1_KICK1 is shown in Figure 5-50 and described in Table 5-119.

Return to Summary Table.

Upper 32-bits of Partition 1 write lock key. This register must be written with the designated key value after a write to PADMMR_MCU_LOCK1_KICK0 with its key value before write-protected Partition 1 registers can be written.

Table 5-165. PADMMR_MCU_LOCK1_KICK1 Instances

Instance	Physical Address
MCU_PADCFG_CTRL0_CFG0	0408 500Ch

Figure 5-50. PADMMR_MCU_LOCK1_KICK1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">KEY</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 5-167. PADMMR_MCU_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers

5.1.2.5 MCU_CTRL_MMR0 Registers

Table 5-121 lists the memory-mapped registers for the MCU_CTRL_MMR0. All register offset addresses not listed in Table 5-121 should be considered as reserved locations and the register contents should not be modified.

Table 5-168. MCU_CTRL_MMR0 Instances

Instance	Base Address
MCU_CTRL_MMR0	0450 0000h

Table 5-169. MCU_CTRL_MMR0 Registers

Offset	Acronym	Register Name	MCU_CTRL_ MMR0 Physical Address
0h	CTRLMMR_MCU_PID	Peripheral Identification Register	0450 0000h
8h	CTRLMMR_MCU_MMR_CFG1	Configuration register 1	0450 0008h
1008h	CTRLMMR_MCU_LOCK0_KICK0	Partition 0 Lock Key 0 Register	0450 1008h
100Ch	CTRLMMR_MCU_LOCK0_KICK1	Partition 0 Lock Key 1 Register	0450 100Ch
1010h	CTRLMMR_MCU_INTR_RAW_STAT	Interrupt Raw Status Register	0450 1010h
1014h	CTRLMMR_MCU_INTR_STAT_CLR	Interrupt Status and Clear Register	0450 1014h
1018h	CTRLMMR_MCU_INTR_EN_SET	Interrupt Enable Set Register	0450 1018h
101Ch	CTRLMMR_MCU_INTR_EN_CLR	Interrupt Enable Clear Register	0450 101Ch
1020h	CTRLMMR_MCU_EOI	End of Interrupt Register	0450 1020h
1024h	CTRLMMR_MCU_FAULT_ADDR	Fault Address Register	0450 1024h
1028h	CTRLMMR_MCU_FAULT_TYPE	Fault Type Register	0450 1028h
102Ch	CTRLMMR_MCU_FAULT_ATTR	Fault Attribute Register	0450 102Ch
1030h	CTRLMMR_MCU_FAULT_CLR	Fault Clear Register	0450 1030h
4084h	CTRLMMR_MCU_DBOUNCE_CFG1	Debounce Config Register	0450 4084h
4088h	CTRLMMR_MCU_DBOUNCE_CFG2	Debounce Config Register	0450 4088h
408Ch	CTRLMMR_MCU_DBOUNCE_CFG3	Debounce Config Register	0450 408Ch
4090h	CTRLMMR_MCU_DBOUNCE_CFG4	Debounce Config Register	0450 4090h
4094h	CTRLMMR_MCU_DBOUNCE_CFG5	Debounce Config Register	0450 4094h
4098h	CTRLMMR_MCU_DBOUNCE_CFG6	Debounce Config Register	0450 4098h
40A0h	CTRLMMR_MCU_TEMP_DIODE_TRIM	Temperature Diode Trim Register	0450 40A0h
40B0h	CTRLMMR_MCU_IO_VOLTAGE_STAT	I/O Voltage Status Register	0450 40B0h
4204h	CTRLMMR_MCU_TIMER1_CTRL	TIMER1 Control Register	0450 4204h
420Ch	CTRLMMR_MCU_TIMER3_CTRL	TIMER3 Control Register	0450 420Ch
42E0h	CTRLMMR_MCU_I2C0_CTRL	I2C0 Control Register	0450 42E0h
4600h	CTRLMMR_MCU_MTOG_CTRL	MCU to MAIN domain Timeout Gasket Control	0450 4600h
5008h	CTRLMMR_MCU_LOCK1_KICK0	Partition 1 Lock Key 0 Register	0450 5008h
500Ch	CTRLMMR_MCU_LOCK1_KICK1	Partition 1 Lock Key 1 Register	0450 500Ch
8000h	CTRLMMR_MCU_OBSCLK_CTRL	Observe Clock Output Control Register	0450 8000h
8010h	CTRLMMR_MCU_HFOSC0_CTRL	Oscillator0 Control Register	0450 8010h
8018h	CTRLMMR_MCU_HFOSC0_TRIM	Oscillator0 Trim Register	0450 8018h
8024h	CTRLMMR_MCU_RC12M_OSC_TRIM	12.5 MHz RC Oscillator Trim Register	0450 8024h
8030h	CTRLMMR_MCU_HFOSC0_CLKOUT_32K_CTRL	Control for 32K Clock Divider from HFOSC0	0450 8030h
8040h	CTRLMMR_MCU_M4FSS_CLKSEL	Clock Select for M4FSS CPU	0450 8040h
8044h	CTRLMMR_MCU_M4FSS_SYSTICK	System Tick Calibration Register	0450 8044h

Table 5-169. MCU_CTRL_MMR0 Registers (continued)

Offset	Acronym	Register Name	MCU_CTRL_ MMR0 Physical Address
8050h	CTRLMMR_MCU_PLL_CLKSEL	MCU PLL0 Source Clock Select Register	0450 8050h
8060h	CTRLMMR_MCU_TIMER0_CLKSEL	Timer0 Clock Select Register	0450 8060h
8064h	CTRLMMR_MCU_TIMER1_CLKSEL	Timer1 Clock Select Register	0450 8064h
8068h	CTRLMMR_MCU_TIMER2_CLKSEL	Timer2 Clock Select Register	0450 8068h
806Ch	CTRLMMR_MCU_TIMER3_CLKSEL	Timer3 Clock Select Register	0450 806Ch
80A0h	CTRLMMR_MCU_SPI0_CLKSEL	MCU_SPI Clock Select Register	0450 80A0h
80A4h	CTRLMMR_MCU_SPI1_CLKSEL	MCU_SPI Clock Select Register	0450 80A4h
80B0h	CTRLMMR_MCU_WWD0_CLKSEL	WWD0 Clock Select Register	0450 80B0h
80D0h	CTRLMMR_MCU_DDR16SS_PMCTRL	DDR16SS Power Management Control	0450 80D0h
9008h	CTRLMMR_MCU_LOCK2_KICK0	Partition 2 Lock Key 0 Register	0450 9008h
900Ch	CTRLMMR_MCU_LOCK2_KICK1	Partition 2 Lock Key 1 Register	0450 900Ch
C020h	CTRLMMR_MCU_M4FSS0_LBIST_CTRL	MCU_M4FSS0 Logic BIST Control Register	0450 C020h
C024h	CTRLMMR_MCU_M4FSS0_LBIST_PATCOUNT	MCU_M4FSS0 Logic BIST Pattern Count Register	0450 C024h
C028h	CTRLMMR_MCU_M4FSS0_LBIST_SEED0	MCU_M4FSS0 Logic BIST Seed0 Register	0450 C028h
C02Ch	CTRLMMR_MCU_M4FSS0_LBIST_SEED1	MCU_M4FSS0 Logic BIST Seed1 Register	0450 C02Ch
C030h	CTRLMMR_MCU_M4FSS0_LBIST_SPARE0	MCU_M4FSS0 Logic BIST Spare0 Register	0450 C030h
C034h	CTRLMMR_MCU_M4FSS0_LBIST_SPARE1	MCU_M4FSS0 Logic BIST Spare1 Register	0450 C034h
C038h	CTRLMMR_MCU_M4FSS0_LBIST_STAT	MCU_M4FSS0 Logic BIST Status Register	0450 C038h
C03Ch	CTRLMMR_MCU_M4FSS0_LBIST_MISR	MCU_M4FSS0 Logic BIST MISR Register	0450 C03Ch
D008h	CTRLMMR_MCU_LOCK3_KICK0	Partition 3 Lock Key 0 Register	0450 D008h
D00Ch	CTRLMMR_MCU_LOCK3_KICK1	Partition 3 Lock Key 1 Register	0450 D00Ch
18000h	CTRLMMR_MCU_POR_CTRL	Power-On Reset Module Control Register	0451 8000h
18004h	CTRLMMR_MCU_POR_STAT	Power-On Reset Module Status Register	0451 8004h
18100h	CTRLMMR_MCU_POR_BANDGAP_CTRL	Bandgap Control Register	0451 8100h
18110h	CTRLMMR_MCU_POK_VDDA_MCU_UV_CTRL	POK_VDDA_MCU Under-Voltage Control Register	0451 8110h
18114h	CTRLMMR_MCU_POK_VDDA_MCU_OV_CTRL	POK_VDDA_MCU Over-Voltage Control Register	0451 8114h
18118h	CTRLMMR_MCU_POK_VDD_CORE_UV_CTRL	POK_VDD_CORE Under-Voltage Control Register	0451 8118h
1811Ch	CTRLMMR_MCU_POK_VDD_CORE_OV_CTRL	POK_VDD_CORE Over-Voltage Control Register	0451 811Ch
18120h	CTRLMMR_MCU_POK_VDDR_CORE_UV_CTRL	POK_VDDR_CORE Under-Voltage Control Register	0451 8120h
18124h	CTRLMMR_MCU_POK_VDDR_CORE_OV_CTRL	POK_VDDR_CORE Over-Voltage Control Register	0451 8124h
18128h	CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_UV_CTRL	POK_VDDSHV_MCU_1P8 Under-Voltage Control Register	0451 8128h
1812Ch	CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_OV_CTRL	POK_VDDSHV_MCU_1P8 Over-Voltage Control Register	0451 812Ch
18130h	CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_UV_CTRL	POK_VDDSHV_MCU_3P3 Under-Voltage Control Register	0451 8130h
18134h	CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_OV_CTRL	POK_VDDSHV_MCU_3P3 Over-Voltage Control Register	0451 8134h
18138h	CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_UV_CTRL	POK_VMON_CAP_MCU_GENERAL Under-Voltage Control Register	0451 8138h

Table 5-169. MCU_CTRL_MMR0 Registers (continued)

Offset	Acronym	Register Name	MCU_CTRL_MMR0 Physical Address
1813Ch	CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_OV_CTRL	POK_VMON_CAP_MCU_GENERAL Over-Voltage Control Register	0451 813Ch
18140h	CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_UV_CTRL	POK_VDDSHV_MAIN_1P8 Under-Voltage Control Register	0451 8140h
18144h	CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_OV_CTRL	POK_VDDSHV_MAIN_1P8 Over-Voltage Control Register	0451 8144h
18148h	CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_UV_CTRL	POK_VDDSHV_MAIN_3P3 Under-Voltage Control Register	0451 8148h
1814Ch	CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_OV_CTRL	POK_VDDSHV_MAIN_3P3 Over-Voltage Control Register	0451 814Ch
18150h	CTRLMMR_MCU_POK_VDDS_DDRIO_UV_CTRL	POK_VDDS_DDRIO Under-Voltage Control Register	0451 8150h
18154h	CTRLMMR_MCU_POK_VDDS_DDRIO_OV_CTRL	POK_VDDS_DDRIO Over-Voltage Control Register	0451 8154h
18160h	CTRLMMR_MCU_POK_VDDA_PMIC_IN_CTRL	POK_VDDA_PMIC_IN Control Register	0451 8160h
18170h	CTRLMMR_MCU_RST_CTRL	Reset Control Register	0451 8170h
18174h	CTRLMMR_MCU_RST_STAT	Reset Status Register	0451 8174h
18178h	CTRLMMR_MCU_RST_SRC	Reset Source Register	0451 8178h
1817Ch	CTRLMMR_MCU_RST_MAGIC_WORD	Magic Word	0451 817Ch
18180h	CTRLMMR_MCU_ISO_CTRL	Isolation Control Register	0451 8180h
18190h	CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL	Core Voltage Glitch Detect Control Register	0451 8190h
181B0h	CTRLMMR_MCU_VDD_CORE_GLDTC_STAT	Core Voltage Core Glitch Detect Status Register	0451 81B0h
18200h	CTRLMMR_MCU_PRG_PP_0_CTRL	PRG_PP_0 Control Register	0451 8200h
18208h	CTRLMMR_MCU_PRG_PP_1_CTRL	PRG_PP_1 Control Register	0451 8208h
18284h	CTRLMMR_MCU_CLKGATE_CTRL	MCU Automatic Clock Gating Control Register	0451 8284h
18288h	CTRLMMR_MCU_MAIN_CLKGATE_CTRL0	MAIN Automatic Clock Gating Control Register	0451 8288h
19008h	CTRLMMR_MCU_LOCK6_KICK0	Partition 6 Lock Key 0 Register	0451 9008h
1900Ch	CTRLMMR_MCU_LOCK6_KICK1	Partition 6 Lock Key 1 Register	0451 900Ch

1 CTRLMMR_MCU_PID Register (Offset = 0h) [reset = 61800800h]

CTRLMMR_MCU_PID is shown in Figure 5-51 and described in Table 5-123.

Return to Summary Table.

Peripheral release details.

Table 5-170. CTRLMMR_MCU_PID Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 0000h

Figure 5-51. CTRLMMR_MCU_PID Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R-1h		R-2h		R-180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R-180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_RTL					X_MAJOR		
R-1h					R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		Y_MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 5-172. CTRLMMR_MCU_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	CTRLMMR_MCU_PID follows new scheme
29-28	BU	R	2h	Business unit - Processors
27-16	FUNC	R	180h	Module functional identifier - CTRL MMR
15-11	R_RTL	R	1h	RTL revision number
10-8	X_MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	Custom revision number
5-0	Y_MINOR	R	0h	Minor revision number

2 CTRLMMR_MCU_MMR_CFG1 Register (Offset = 8h) [reset = 800000DFh]

CTRLMMR_MCU_MMR_CFG1 is shown in Figure 5-52 and described in Table 5-125.

Return to Summary Table.

Indicates the MMR configuration.

Table 5-173. CTRLMMR_MCU_MMR_CFG1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 0008h

Figure 5-52. CTRLMMR_MCU_MMR_CFG1 Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PARTITIONS							
R-DFh							

LEGEND: R = Read Only; -*n* = value after reset

Table 5-175. CTRLMMR_MCU_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	1h	Reserved
30-8	RESERVED	R	0h	Reserved
7-0	PARTITIONS	R	DFh	Indicates present partitions

3 CTRLMMR_MCU_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

CTRLMMR_MCU_LOCK0_KICK0 is shown in Figure 5-53 and described in Table 5-127.

Return to Summary Table.

Lower 32-bits of Partition0 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK0_KICK1 with its key value before write-protected Partition 0 registers can be written.

Table 5-176. CTRLMMR_MCU_LOCK0_KICK0 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 1008h

Figure 5-53. CTRLMMR_MCU_LOCK0_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							

23	22	21	20	19	18	17	16
KEY							
R/W-0h							

15	14	13	12	11	10	9	8
KEY							
R/W-0h							

7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-178. CTRLMMR_MCU_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

4 CTRLMMR_MCU_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

CTRLMMR_MCU_LOCK0_KICK1 is shown in Figure 5-54 and described in Table 5-129.

Return to Summary Table.

Upper 32-bits of Partition 0 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK0_KICK0 with its key value before write-protected Partition 0 registers can be written.

Table 5-179. CTRLMMR_MCU_LOCK0_KICK1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 100Ch

Figure 5-54. CTRLMMR_MCU_LOCK0_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 5-181. CTRLMMR_MCU_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers

5 CTRLMMR_MCU_INTR_RAW_STAT Register (Offset = 1010h) [reset = 0h]

CTRLMMR_MCU_INTR_RAW_STAT is shown in Figure 5-55 and described in Table 5-131.

Return to Summary Table.

Shows the interrupt status (before enabling) and allows setting of the interrupt status (for test).

Table 5-182. CTRLMMR_MCU_INTR_RAW_STAT Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 1010h

Figure 5-55. CTRLMMR_MCU_INTR_RAW_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	LOCK_ERR	ADDR_ERR	PROT_ERR
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 5-184. CTRLMMR_MCU_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RESERVED	W1TS	0h	Reserved
2	LOCK_ERR	W1TS	0h	Lock violation occurred (attempt to write a write-locked register with partition locked) Write 1 to set the status bit (for test) Writing 0 has no effect.
1	ADDR_ERR	W1TS	0h	Address violation occurred (attempt to read or write an invalid register address) Write 1 to set the status bit (for test) Writing 0 has no effect.
0	PROT_ERR	W1TS	0h	Reserved (Protection) Error Condition. Not applicable or checked on this device, but still can be stimulated by a software write to this bit. Write 1 to set the status bit (for test) Writing 0 has no effect.

6 CTRLMMR_MCU_INTR_STAT_CLR Register (Offset = 1014h) [reset = 0h]

CTRLMMR_MCU_INTR_STAT_CLR is shown in Figure 5-56 and described in Table 5-133.

Return to Summary Table.

Shows the enabled interrupt status and allows the interrupt to be cleared.

Table 5-185. CTRLMMR_MCU_INTR_STAT_CLR Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 1014h

Figure 5-56. CTRLMMR_MCU_INTR_STAT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	EN_LOCK_ERR	EN_ADDR_ERR	EN_PROT_ERR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; -*n* = value after reset

Table 5-187. CTRLMMR_MCU_INTR_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RESERVED	W1TC	0h	Reserved
2	EN_LOCK_ERR	W1TC	0h	Enabled lock interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
1	EN_ADDR_ERR	W1TC	0h	Enabled address interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
0	EN_PROT_ERR	W1TC	0h	Enabled Reserved (protection) interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.

7 CTRLMMR_MCU_INTR_EN_SET Register (Offset = 1018h) [reset = 0h]

CTRLMMR_MCU_INTR_EN_SET is shown in Figure 5-57 and described in Table 5-135.

Return to Summary Table.

Allows interrupt enables to be set.

Table 5-188. CTRLMMR_MCU_INTR_EN_SET Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 1018h

Figure 5-57. CTRLMMR_MCU_INTR_EN_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED				RESERVED	LOCK_ERR_EN_SET	ADDR_ERR_EN_SET	PROT_ERR_EN_SET
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; *-n* = value after reset

Table 5-190. CTRLMMR_MCU_INTR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RESERVED	W1TS	0h	Reserved
2	LOCK_ERR_EN_SET	W1TS	0h	Lock interrupt enable Write 1 to enable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_SET	W1TS	0h	Address interrupt enable Write 1 to enable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_SET	W1TS	0h	Reserved (Protection) interrupt enable Write 1 to enable protection interrupt events Writing 0 has no effect.

8 CTRLMMR_MCU_INTR_EN_CLR Register (Offset = 101Ch) [reset = 0h]

CTRLMMR_MCU_INTR_EN_CLR is shown in Figure 5-58 and described in Table 5-137.

Return to Summary Table.

Allows interrupt enables to be cleared.

Table 5-191. CTRLMMR_MCU_INTR_EN_CLR Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 101Ch

Figure 5-58. CTRLMMR_MCU_INTR_EN_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED				RESERVED	LOCK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; -*n* = value after reset

Table 5-193. CTRLMMR_MCU_INTR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RESERVED	W1TC	0h	Reserved
2	LOCK_ERR_EN_CLR	W1TC	0h	Lock interrupt disable Write 1 to disable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_CLR	W1TC	0h	Address interrupt disable Write 1 to disable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_CLR	W1TC	0h	Reserved (Protection) interrupt disable Write 1 to disable protection interrupt events Writing 0 has no effect.

9 CTRLMMR_MCU_EOI Register (Offset = 1020h) [reset = 0h]

CTRLMMR_MCU_EOI is shown in Figure 5-59 and described in Table 5-139.

Return to Summary Table.

CTRLMMR_MCU_EOI Vector value This register should be written with interrupt distribution value required by the device architecture to indicate service completion of the MMR interrupt.

Table 5-194. CTRLMMR_MCU_EOI Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 1020h

Figure 5-59. CTRLMMR_MCU_EOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VECTOR							
R-0h																								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-196. CTRLMMR_MCU_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VECTOR	R/W	0h	CTRLMMR_MCU_EOI vector value

10 CTRLMMR_MCU_FAULT_ADDR Register (Offset = 1024h) [reset = 0h]

CTRLMMR_MCU_FAULT_ADDR is shown in Figure 5-60 and described in Table 5-141.

Return to Summary Table.

Indicates the address of the first transfer that caused a fault to occur.

Table 5-197. CTRLMMR_MCU_FAULT_ADDR Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 1024h

Figure 5-60. CTRLMMR_MCU_FAULT_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 5-199. CTRLMMR_MCU_FAULT_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Address of the faulted access

11 CTRLMMR_MCU_FAULT_TYPE Register (Offset = 1028h) [reset = 0h]

CTRLMMR_MCU_FAULT_TYPE is shown in Figure 5-61 and described in Table 5-143.

Return to Summary Table.

Indicates the access type of the first transfer that caused a fault to occur.

Table 5-200. CTRLMMR_MCU_FAULT_TYPE Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 1028h

Figure 5-61. CTRLMMR_MCU_FAULT_TYPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										TYPE					
R-0h																										R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 5-202. CTRLMMR_MCU_FAULT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	TYPE	R	0h	Type of access which faulted 0h - No fault 1h - User execute access 2h - User write access 4h - User read access 8h - Supervisor execute access 10h - Supervisor write access 20h - Supervisor read access

12 CTRLMMR_MCU_FAULT_ATTR Register (Offset = 102Ch) [reset = 0h]

CTRLMMR_MCU_FAULT_ATTR is shown in Figure 5-62 and described in Table 5-145.

Return to Summary Table.

Indicates the attributes of the first transfer that caused a fault to occur.

Table 5-203. CTRLMMR_MCU_FAULT_ATTR Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 102Ch

Figure 5-62. CTRLMMR_MCU_FAULT_ATTR Register

31	30	29	28	27	26	25	24
XID							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XID				ROUTEID			
R-0h				R-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ROUTEID							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIVID							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 5-205. CTRLMMR_MCU_FAULT_ATTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	XID	R	0h	Transaction ID
19-8	ROUTEID	R	0h	Route ID
7-0	PRIVID	R	0h	Privilege ID

13 CTRLMMR_MCU_FAULT_CLR Register (Offset = 1030h) [reset = 0h]

CTRLMMR_MCU_FAULT_CLR is shown in Figure 5-63 and described in Table 5-147.

Return to Summary Table.

Allows software to clear the current fault Clearing the current fault allows the CTRLMMR_MCU_FAULT_ADDR, CTRLMMR_MCU_FAULT_TYPE, and CTRLMMR_MCU_FAULT_ATTR registers to latch the attributes of the next fault that occurs. This does not affect the fault interrupt event itself. The interrupt must be cleared using the appropriate INTR_STATUS_CLR register bits.

Table 5-206. CTRLMMR_MCU_FAULT_CLR Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 1030h

Figure 5-63. CTRLMMR_MCU_FAULT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLEAR
R-0h							W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; -*n* = value after reset

Table 5-208. CTRLMMR_MCU_FAULT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLEAR	W1TC	0h	Fault clear Write 1 to clear the current fault Writing 0 has no effect

14 CTRLMMR_MCU_DBOUNCE_CFG1 Register (Offset = 4084h) [reset = 0h]

CTRLMMR_MCU_DBOUNCE_CFG1 is shown in Figure 5-64 and described in Table 5-149.

Return to Summary Table.

Configures IO debounce selections.

Table 5-209. CTRLMMR_MCU_DBOUNCE_CFG1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 4084h

Figure 5-64. CTRLMMR_MCU_DBOUNCE_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-211. CTRLMMR_MCU_DBOUNCE_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel1 enabled.

15 CTRLMMR_MCU_DBOUNCE_CFG2 Register (Offset = 4088h) [reset = 0h]

CTRLMMR_MCU_DBOUNCE_CFG2 is shown in Figure 5-65 and described in Table 5-151.

Return to Summary Table.

Configures IO debounce selections.

Table 5-212. CTRLMMR_MCU_DBOUNCE_CFG2 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 4088h

Figure 5-65. CTRLMMR_MCU_DBOUNCE_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-214. CTRLMMR_MCU_DBOUNCE_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel2 enabled.

16 CTRLMMR_MCU_DBOUNCE_CFG3 Register (Offset = 408Ch) [reset = 0h]

CTRLMMR_MCU_DBOUNCE_CFG3 is shown in Figure 5-66 and described in Table 5-153.

Return to Summary Table.

Configures IO debounce selections.

Table 5-215. CTRLMMR_MCU_DBOUNCE_CFG3 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 408Ch

Figure 5-66. CTRLMMR_MCU_DBOUNCE_CFG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-217. CTRLMMR_MCU_DBOUNCE_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel3 enabled.

17 CTRLMMR_MCU_DBOUNCE_CFG4 Register (Offset = 4090h) [reset = 0h]

CTRLMMR_MCU_DBOUNCE_CFG4 is shown in Figure 5-67 and described in Table 5-155.

Return to Summary Table.

Configures IO debounce selections.

Table 5-218. CTRLMMR_MCU_DBOUNCE_CFG4 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 4090h

Figure 5-67. CTRLMMR_MCU_DBOUNCE_CFG4 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="26">RESERVED</td><td colspan="6">DB_CFG</td></tr>
<tr><td colspan="26">R-0h</td><td colspan="6">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-220. CTRLMMR_MCU_DBOUNCE_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel4 enabled.

18 CTRLMMR_MCU_DBOUNCE_CFG5 Register (Offset = 4094h) [reset = 0h]

CTRLMMR_MCU_DBOUNCE_CFG5 is shown in Figure 5-68 and described in Table 5-157.

Return to Summary Table.

Configures IO debounce selections.

Table 5-221. CTRLMMR_MCU_DBOUNCE_CFG5 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 4094h

Figure 5-68. CTRLMMR_MCU_DBOUNCE_CFG5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-223. CTRLMMR_MCU_DBOUNCE_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel5 enabled.

19 CTRLMMR_MCU_DBOUNCE_CFG6 Register (Offset = 4098h) [reset = 0h]

CTRLMMR_MCU_DBOUNCE_CFG6 is shown in Figure 5-69 and described in Table 5-159.

Return to Summary Table.

Configures IO debounce selections.

Table 5-224. CTRLMMR_MCU_DBOUNCE_CFG6 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 4098h

Figure 5-69. CTRLMMR_MCU_DBOUNCE_CFG6 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="26">RESERVED</td><td colspan="6">DB_CFG</td></tr>
<tr><td colspan="26">R-0h</td><td colspan="6">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-226. CTRLMMR_MCU_DBOUNCE_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel6 enabled.

20 CTRLMMR_MCU_TEMP_DIODE_TRIM Register (Offset = 40A0h) [reset = X]

CTRLMMR_MCU_TEMP_DIODE_TRIM is shown in Figure 5-70 and described in Table 5-161.

Return to Summary Table.

Trims the silicon junction temperature diode calculation.

Table 5-227. CTRLMMR_MCU_TEMP_DIODE_TRIM Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 40A0h

Figure 5-70. CTRLMMR_MCU_TEMP_DIODE_TRIM Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="18">RESERVED</td><td colspan="14">TRIM</td></tr>
<tr><td colspan="18">R-0h</td><td colspan="14">R-X</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 5-229. CTRLMMR_MCU_TEMP_DIODE_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-0	TRIM	R	X	Sets the diode non-ideality factor (n), starting from 100th place decimal and going down

21 CTRLMMR_MCU_IO_VOLTAGE_STAT Register (Offset = 40B0h) [reset = X]

CTRLMMR_MCU_IO_VOLTAGE_STAT is shown in Figure 5-71 and described in Table 5-163.

Return to Summary Table.

Indicates the I/O voltage of each LVCMOS dual I/O group.

Table 5-230. CTRLMMR_MCU_IO_VOLTAGE_STAT Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 40B0h

Figure 5-71. CTRLMMR_MCU_IO_VOLTAGE_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						MAIN_GPMC	RESERVED
R-0h						R-X	R-0h
15	14	13	12	11	10	9	8
RESERVED		MAIN_PRG1	MAIN_PRG0	RESERVED	MAIN_MMC1	RESERVED	MAIN_GEN
R-0h		R-X	R-X	R-0h	R-X	R-0h	R-X
7	6	5	4	3	2	1	0
RESERVED						MCU_FLASH	MCU_GEN
R-0h						R-X	R-X

LEGEND: R = Read Only; -*n* = value after reset

Table 5-232. CTRLMMR_MCU_IO_VOLTAGE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	MAIN_GPMC	R	X	Indicates the voltage for the GPMC I/O group (VDDSHV3) 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
16-14	RESERVED	R	0h	Reserved
13	MAIN_PRG1	R	X	Indicates the voltage for the PRG1 I/O group (VDDSHV1) 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
12	MAIN_PRG0	R	X	Indicates the voltage for the PRG0 I/O group (VDDSHV2) 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
11	RESERVED	R	0h	Reserved
10	MAIN_MMC1	R	X	Indicates the voltage for the MMC1 I/O group (VDDSHV5) 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
9	RESERVED	R	0h	Reserved

Table 5-232. CTRLMMR_MCU_IO_VOLTAGE_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MAIN_GEN	R	X	Indicates the voltage for the General I/O group (VDDSHV0) 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
7-2	RESERVED	R	0h	Reserved
1	MCU_FLASH	R	X	Indicates the voltage for the Flash I/O group (VDDSHV4) 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
0	MCU_GEN	R	X	Indicates the voltage for the MCU General I/O group (VDDSHV0_MCU) 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V

22 CTRLMMR_MCU_TIMER1_CTRL Register (Offset = 4204h) [reset = 0h]

CTRLMMR_MCU_TIMER1_CTRL is shown in Figure 5-72 and described in Table 5-165.

Return to Summary Table.

Controls TIMER1 operation.

Table 5-233. CTRLMMR_MCU_TIMER1_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 4204h

Figure 5-72. CTRLMMR_MCU_TIMER1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-235. CTRLMMR_MCU_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER1 to TIMER0
7-0	RESERVED	R	0h	Reserved

23 CTRLMMR_MCU_TIMER3_CTRL Register (Offset = 420Ch) [reset = 0h]

CTRLMMR_MCU_TIMER3_CTRL is shown in Figure 5-73 and described in Table 5-167.

Return to Summary Table.

Controls TIMER3 operation.

Table 5-236. CTRLMMR_MCU_TIMER3_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 420Ch

Figure 5-73. CTRLMMR_MCU_TIMER3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-238. CTRLMMR_MCU_TIMER3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER3 to TIMER2
7-0	RESERVED	R	0h	Reserved

24 CTRLMMR_MCU_I2C0_CTRL Register (Offset = 42E0h) [reset = 0h]

CTRLMMR_MCU_I2C0_CTRL is shown in Figure 5-74 and described in Table 5-169.

Return to Summary Table.

Controls I2C0 operation for open drain I/Os.

Table 5-239. CTRLMMR_MCU_I2C0_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 42E0h

Figure 5-74. CTRLMMR_MCU_I2C0_CTRL Register

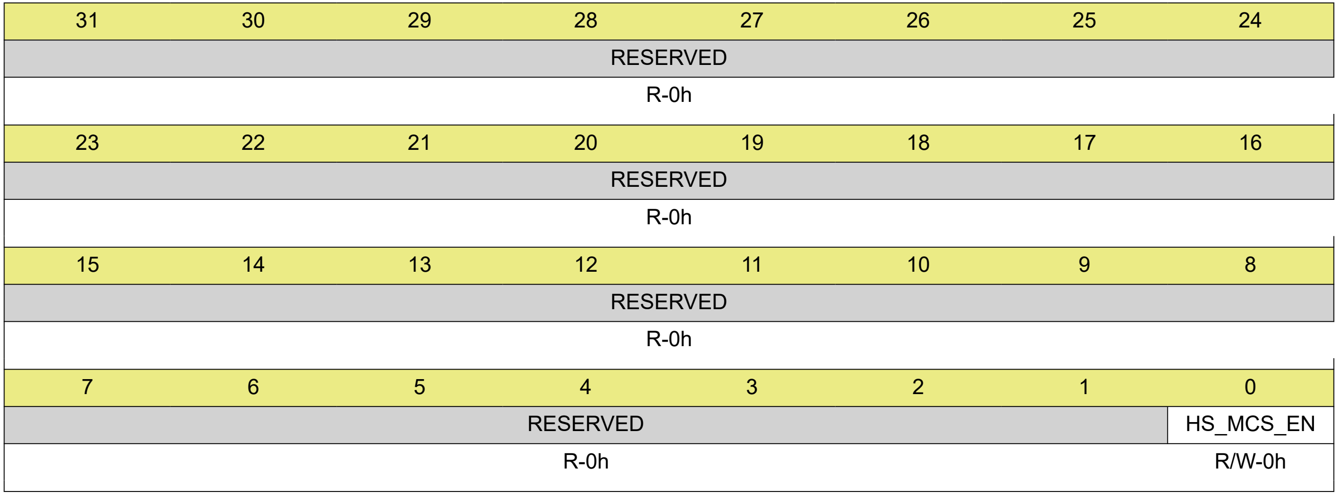

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							HS_MCS_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-241. CTRLMMR_MCU_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HS_MCS_EN	R/W	0h	HS Mode master current source enable. When set, enables the current-source pull-up on the SCL output. Only one master on the I2C bus should enable SCL current sourcing.

25 CTRLMMR_MCU_MTOG_CTRL Register (Offset = 4600h) [reset = X]

CTRLMMR_MCU_MTOG_CTRL is shown in Figure 5-75 and described in Table 5-171.

Return to Summary Table.

Controls timeout operation of read transactions from the MCU Domain.

Table 5-242. CTRLMMR_MCU_MTOG_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 4600h

Figure 5-75. CTRLMMR_MCU_MTOG_CTRL Register

31	30	29	28	27	26	25	24
IDLE_STAT	RESERVED						
R-X	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FORCE_TIMEOUT							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TIMEOUT_EN	RESERVED						
R/W-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TIMEOUT_VAL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-244. CTRLMMR_MCU_MTOG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE_STAT	R	X	Idle Status: When high, indicates MTOG0 is idle
30-24	RESERVED	R	0h	Reserved
23-16	FORCE_TIMEOUT	R/W	0h	Force Timout This is a fault tolerant bitfield. Forces a flush of the interface transactions. This bitfield is only relevant if timeout_en=1. After forcing a timeout by writing the encoded value, the force_timeout and timeout_en bitfields mut be cleared to clear the timeout before re-enabling the gasket. 8'h95 - Force a gasket timeout All others - Normal operation
15	TIMEOUT_EN	R/W	0h	Timeout Enable 0h - Disable the gasket. Clear the interrupt and reset the counter 1h - Enable the timeout gasket functions
14-3	RESERVED	R	0h	Reserved

Table 5-244. CTRLMMR_MCU_MTOG_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	TIMEOUT_VAL	R/W	0h	Gasket Timeout Value Selects the number of clock cycles before the interface is considered to have timed out 0h - 1024 clock cycles 1h - 4096 clock cycles 2h - 16,384 clock cycles 3h - 65,536 clock cycles 4h - 262,144 clock cycles 5h - 1,048,576 clock cycles 6h - 2,097,152 clock cycles 7h - 4,194,303 clock cycles

26 CTRLMMR_MCU_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

CTRLMMR_MCU_LOCK1_KICK0 is shown in Figure 5-76 and described in Table 5-173.

Return to Summary Table.

Lower 32-bits of Partition1 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK1_KICK1 with its key value before write-protected Partition 1 registers can be written.

Table 5-245. CTRLMMR_MCU_LOCK1_KICK0 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 5008h

Figure 5-76. CTRLMMR_MCU_LOCK1_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 5-247. CTRLMMR_MCU_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

27 CTRLMMR_MCU_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

CTRLMMR_MCU_LOCK1_KICK1 is shown in Figure 5-77 and described in Table 5-175.

Return to Summary Table.

Upper 32-bits of Partition 1 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK1_KICK0 with its key value before write-protected Partition 1 registers can be written.

Table 5-248. CTRLMMR_MCU_LOCK1_KICK1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 500Ch

Figure 5-77. CTRLMMR_MCU_LOCK1_KICK1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">KEY</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 5-250. CTRLMMR_MCU_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers

28 CTRLMMR_MCU_OBSCLK_CTRL Register (Offset = 8000h) [reset = 0h]

CTRLMMR_MCU_OBSCLK_CTRL is shown in Figure 5-78 and described in Table 5-177.

Return to Summary Table.

Controls which internal clock is made observable on the MCU_OBSCLK output pin.

Table 5-251. CTRLMMR_MCU_OBSCLK_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8000h

Figure 5-78. CTRLMMR_MCU_OBSCLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							OUT_MUX_SEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				CLK_DIV			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-253. CTRLMMR_MCU_OBSCLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	OUT_MUX_SEL	R/W	0h	MCU_OBSCLK pin output mux selection. Note, when HFOSC0_CLK is selected (1'b1) the MCU_OBSCLK_CTRL_clk_sel field must be programmed to 4'b0001. 0h - The output of the MCU_OBSCLK output divider is output on the pin 1h - HFOSC0_CLK is output on the pin
23-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-12	RESERVED	R	0h	Reserved
11-8	CLK_DIV	R/W	0h	MCU_OBSCLK pin clock selection output divider Output clock is divided by clk_div+1

Table 5-253. CTRLMMR_MCU_OBSCLK_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	MCU_OBSCLK pin clock selection 0h - CLK_12M_RC 1h - "0" 2h - MCU_PLL0_HSDIV0_CLKOUT 3h - MCU_PLL0_HSDIV4_CLKOUT 4h - MCU_PLLCTRL_OBSCLK 5h - CLK_32K 6h - HFOSC0_CLKOUT 7h - HFOSC0_CLKOUT_32K

29 CTRLMMR_MCU_HFOSC0_CTRL Register (Offset = 8010h) [reset = 0h]

CTRLMMR_MCU_HFOSC0_CTRL is shown in Figure 5-79 and described in Table 5-179.

Return to Summary Table.

Controls the operation of oscillator 0.

Table 5-254. CTRLMMR_MCU_HFOSC0_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8010h

Figure 5-79. CTRLMMR_MCU_HFOSC0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED			BP_C	RESERVED			
R-0h			R/W-0h	R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-256. CTRLMMR_MCU_HFOSC0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	BP_C	R/W	0h	Oscillator bypass control. When set oscillator is in bypass mode
3-0	RESERVED	R	0h	Reserved

30 CTRLMMR_MCU_HFOSC0_TRIM Register (Offset = 8018h) [reset = 131022h]

CTRLMMR_MCU_HFOSC0_TRIM is shown in Figure 5-80 and described in Table 5-181.

Return to Summary Table.

Provides frequency trimming for oscillator 0.

Table 5-257. CTRLMMR_MCU_HFOSC0_TRIM Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8018h

Figure 5-80. CTRLMMR_MCU_HFOSC0_TRIM Register

31	30	29	28	27	26	25	24
TRIM_EN	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED		HYST		RESERVED	I_MULT		
R-0h		R/W-1h		R-0h	R/W-3h		

15	14	13	12	11	10	9	8
RESERVED		R_REF					
R-0h		R/W-10h					

7	6	5	4	3	2	1	0
I_IBIAS_COMP				R_IBIAS_REF			
R/W-2h				R/W-2h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-259. CTRLMMR_MCU_HFOSC0_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRIM_EN	R/W	0h	Apply MMR values to OSC trim inputs instead of tie-offs
30-22	RESERVED	R	0h	Reserved
21-20	HYST	R/W	1h	Sets comparator hysterisis
19	RESERVED	R	0h	Reserved
18-16	I_MULT	R/W	3h	AGC AMP current multiplication gain
15-14	RESERVED	R	0h	Reserved
13-8	R_REF	R/W	10h	Sets the AMP AGC bias current
7-4	I_IBIAS_COMP	R/W	2h	Sets the COMP bias current
3-0	R_IBIAS_REF	R/W	2h	Sets the base IBIAS reference

31 CTRLMMR_MCU_RC12M_OSC_TRIM Register (Offset = 8024h) [reset = X]

CTRLMMR_MCU_RC12M_OSC_TRIM is shown in Figure 5-81 and described in Table 5-183.

Return to Summary Table.

Provides frequency trimming for the 12.5 MHz RC oscillator module.

Table 5-260. CTRLMMR_MCU_RC12M_OSC_TRIM Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8024h

Figure 5-81. CTRLMMR_MCU_RC12M_OSC_TRIM Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TRIMOSC_COARSE_DIR	TRIMOSC_COARSE			TRIMOSC_FINE		
R-0h	R/W-X	R/W-X			R/W-X		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-262. CTRLMMR_MCU_RC12M_OSC_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	TRIMOSC_COARSE_DIR	R/W	X	Coarse adjustment direction. If output is greater than 12.5 0h - Coarse adjustment decreases frequency 1h - Coarse adjustment increases frequency
5-3	TRIMOSC_COARSE	R/W	X	Coarse adjustment. Frequency is decreased or increased by 1.25 MHz per value based on the trimosc_coarse_dir value.
2-0	TRIMOSC_FINE	R/W	X	Fine adjustment. Decreases the frequency by 250 KHz per value.

32 CTRLMMR_MCU_HFOSC0_CLKOUT_32K_CTRL Register (Offset = 8030h) [reset = 8068h]

CTRLMMR_MCU_HFOSC0_CLKOUT_32K_CTRL is shown in Figure 5-82 and described in Table 5-185.

Return to Summary Table.

Controls the HSDIV that generates a 32KHz RT clock from the HFOSC0 Crystal.

Table 5-263. CTRLMMR_MCU_HFOSC0_CLKOUT_32K_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8030h

Figure 5-82. CTRLMMR_MCU_HFOSC0_CLKOUT_32K_CTRL Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-1h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R-0h	R/W-68h						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-265. CTRLMMR_MCU_HFOSC0_CLKOUT_32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	Asynchronous Divider Reset 1 = Divider is Reset, HFOSC0_CLKOUT32K reset. 0 = Divider out of reset, HFOSC0_CLKOUT_32K running.
30-16	RESERVED	R	0h	Reserved
15	CLKOUT_EN	R/W	1h	HFOSC0_CLKOUT_32K enable: 0 = Synchronously Disable HFOSC0_CLKOUT_32KHz 1 = Synchronously Enable HFOSC0_CKLKOUT_32KHz
14-9	RESERVED	R	0h	Reserved
8	SYNC_DIS	R/W	0h	HFOSC0_CLKOUT_32K Synchronize Disable 0 = Divider Updates are shadowed and take effect on counter reset. 1 = Divider Updates are immediate and hazardous Do not set this bit to 1'b1 during normal use.
7	RESERVED	R	0h	Reserved

Table 5-265. CTRLMMR_MCU_HFOSC0_CLKOUT_32K_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	HSDIV	R/W	68h	HFOSC0_CLKOUT_32K divider: HFOSC0_CLKKOUT_32K Frequency = HFOSC0 Frequency / [8 * (hsdiv + 1)] Ex. HFOSC0 Frequency = 27MHz. hsdiv = 104 (Default) HFOSC0_CLKOUT_32K = 27MHz / (8 * (104+1)) = 27MHz / 840 = 32.1 KHz

33 CTRLMMR_MCU_M4FSS_CLKSEL Register (Offset = 8040h) [reset = 0h]

CTRLMMR_MCU_M4FSS_CLKSEL is shown in Figure 5-83 and described in Table 5-187.

Return to Summary Table.

Controls the Clock Source for the M4FSS.

Table 5-266. CTRLMMR_MCU_M4FSS_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8040h

Figure 5-83. CTRLMMR_MCU_M4FSS_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							M4FSS_CLKSEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-268. CTRLMMR_MCU_M4FSS_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	M4FSS_CLKSEL	R/W	0h	Selects the Clock Divider for M4FSS 0 = MCU_SYSCLK0 1 = MCU_SYSCLK1 / 2

34 CTRLMMR_MCU_M4FSS_SYSTICK Register (Offset = 8044h) [reset = 23D08FFh]

CTRLMMR_MCU_M4FSS_SYSTICK is shown in Figure 5-84 and described in Table 5-189.

Return to Summary Table.

Settings to calibrate the SYSTICK interrupt to 100 Hz.

Table 5-269. CTRLMMR_MCU_M4FSS_SYSTICK Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8044h

Figure 5-84. CTRLMMR_MCU_M4FSS_SYSTICK Register

31	30	29	28	27	26	25	24
RESERVED						NOREF	SKEW
R-0h						R-1h	R/W-0h
23	22	21	20	19	18	17	16
TENMS							
R/W-3D08FFh							
15	14	13	12	11	10	9	8
TENMS							
R/W-3D08FFh							
7	6	5	4	3	2	1	0
TENMS							
R/W-3D08FFh							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-271. CTRLMMR_MCU_M4FSS_SYSTICK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	NOREF	R	1h	No External Reference Clock for SysTick is available
24	SKEW	R/W	0h	Indicates whether or not the M4FSS free running clock divided by TENMS produces a 100Hz tick exactly 0h - Divider produces exactly a 100 Hz SysTick 1h - The SysTick Frequency is not exactly 100 Hz
23-0	TENMS	R/W	3D08FFh	Integer Divider Value that produces a 100Hz SysTick from the M4FSS Clock Frequency. Default is 3,999,999 (4M - 1) to produce a 100Hz clock from a 400 MHz M4FSS Clock.

35 CTRLMMR_MCU_PLL_CLKSEL Register (Offset = 8050h) [reset = 800000h]

CTRLMMR_MCU_PLL_CLKSEL is shown in Figure 5-85 and described in Table 5-191.

Return to Summary Table.

Controls the clock source for MCU PLL.

Table 5-272. CTRLMMR_MCU_PLL_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8050h

Figure 5-85. CTRLMMR_MCU_PLL_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							CLKLOSS_SWTCH_EN
R-0h							R/W-0h

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-274. CTRLMMR_MCU_PLL_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a mcu_reset_z for MCU PLL[2:0]. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when an MCU warm reset occurs and will keep MCU PLL[2:0] in bypass mode after reset exit until cleared by software. 1'b0 = Exit bypass mode (based on MCU PLL[2:0]_CTRL_bypass_en bit value) 1'b1 = Maintain bypass mode.
22-9	RESERVED	R	0h	Reserved

Table 5-274. CTRLMMR_MCU_PLL_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CLKLOSS_SWTCH_EN	R/W	0h	When set, enables automatic switching of MCU PLL[2:0] clock source to CLK_12M_RC if HFOSC0 clock loss is detected
7-0	RESERVED	R	0h	Reserved

36 CTRLMMR_MCU_TIMER0_CLKSEL Register (Offset = 8060h) [reset = 0h]

CTRLMMR_MCU_TIMER0_CLKSEL is shown in Figure 5-86 and described in Table 5-193.

Return to Summary Table.

Timer0 functional clock selection control.

Table 5-275. CTRLMMR_MCU_TIMER0_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8060h

Figure 5-86. CTRLMMR_MCU_TIMER0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-277. CTRLMMR_MCU_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC1_CLK) 0h - HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 2 2h - CLK_12M_RC 3h - MCU_PLL0_HSDIV3_CLKOUT 4h - MCU_EXT_REFCLK0 5h - HFOSC0_CLKOUT_32K 6h - cpsw_genf0 7h - CLK_32K

37 CTRLMMR_MCU_TIMER1_CLKSEL Register (Offset = 8064h) [reset = 0h]

CTRLMMR_MCU_TIMER1_CLKSEL is shown in Figure 5-87 and described in Table 5-195.

Return to Summary Table.

Timer1 functional clock selection control.

Table 5-278. CTRLMMR_MCU_TIMER1_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8064h

Figure 5-87. CTRLMMR_MCU_TIMER1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-280. CTRLMMR_MCU_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC1_CLK) 0h - HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 2 2h - CLK_12M_RC 3h - MCU_PLL0_HSDIV3_CLKOUT 4h - MCU_EXT_REFCLK0 5h - HFOSC0_CLKOUT_32K 6h - cpsw_genf0 7h - CLK_32K

38 CTRLMMR_MCU_TIMER2_CLKSEL Register (Offset = 8068h) [reset = 0h]

CTRLMMR_MCU_TIMER2_CLKSEL is shown in Figure 5-88 and described in Table 5-197.

Return to Summary Table.

Timer2 functional clock selection control.

Table 5-281. CTRLMMR_MCU_TIMER2_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 8068h

Figure 5-88. CTRLMMR_MCU_TIMER2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-283. CTRLMMR_MCU_TIMER2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC1_CLK) 0h - HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 2 2h - CLK_12M_RC 3h - MCU_PLL0_HSDIV3_CLKOUT 4h - MCU_EXT_REFCLK0 5h - HFOSC0_CLKOUT_32K 6h - cpsw_genf0 7h - CLK_32K

39 CTRLMMR_MCU_TIMER3_CLKSEL Register (Offset = 806Ch) [reset = 0h]

CTRLMMR_MCU_TIMER3_CLKSEL is shown in Figure 5-89 and described in Table 5-199.

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Timer3 functional clock selection control.

Table 5-284. CTRLMMR_MCU_TIMER3_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 806Ch

Figure 5-89. CTRLMMR_MCU_TIMER3_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-286. CTRLMMR_MCU_TIMER3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC1_CLK) 0h - HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 2 2h - CLK_12M_RC 3h - MCU_PLL0_HSDIV3_CLKOUT 4h - MCU_EXT_REFCLK0 5h - HFOSC0_CLKOUT_32K 6h - cpsw_genf0 7h - CLK_32K

40 CTRLMMR_MCU_SPI0_CLKSEL Register (Offset = 80A0h) [reset = 0h]

CTRLMMR_MCU_SPI0_CLKSEL is shown in Figure 5-90 and described in Table 5-201.

Return to Summary Table.

MCU_SPI0 clock control.

Table 5-287. CTRLMMR_MCU_SPI0_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 80A0h

Figure 5-90. CTRLMMR_MCU_SPI0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-289. CTRLMMR_MCU_SPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

41 CTRLMMR_MCU_SPI1_CLKSEL Register (Offset = 80A4h) [reset = 0h]

CTRLMMR_MCU_SPI1_CLKSEL is shown in Figure 5-91 and described in Table 5-203.

Return to Summary Table.

MCU_SPI1 clock control.

Table 5-290. CTRLMMR_MCU_SPI1_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 80A4h

Figure 5-91. CTRLMMR_MCU_SPI1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-292. CTRLMMR_MCU_SPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

42 CTRLMMR_MCU_WWD0_CLKSEL Register (Offset = 80B0h) [reset = 0h]

CTRLMMR_MCU_WWD0_CLKSEL is shown in Figure 5-92 and described in Table 5-205.

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MCU Windowed Watchdog clock selection control.

Table 5-293. CTRLMMR_MCU_WWD0_CLKSEL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 80B0h

Figure 5-92. CTRLMMR_MCU_WWD0_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-295. CTRLMMR_MCU_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset.
30-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control 0h - HFOSC0_CLKOUT 1h - HFOSC0_CLKOUT_32K 2h - CLK_12M_RC 3h - CLK_32K

43 CTRLMMR_MCU_DDR16SS_PMCTRL Register (Offset = 80D0h) [reset = 0h]

CTRLMMR_MCU_DDR16SS_PMCTRL is shown in Figure 5-93 and described in Table 5-207.

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Control Sleep States of DDR16SS.

Table 5-296. CTRLMMR_MCU_DDR16SS_PMCTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 80D0h

Figure 5-93. CTRLMMR_MCU_DDR16SS_PMCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				DATA_RETENTION			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-298. CTRLMMR_MCU_DDR16SS_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	DATA_RETENTION	R/W	0h	DDR16SS Retention: This is a fault tolerant bit field 0x06 Asserts DDRSS 'data_retention' which will Hi-Z most of the phy output pins except for CKE/RESET# All others (Default 0) : data_retention is deasserted for normal DDR16SS Operation

44 CTRLMMR_MCU_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

CTRLMMR_MCU_LOCK2_KICK0 is shown in Figure 5-94 and described in Table 5-209.

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Lower 32-bits of Partition2 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK2_KICK1 with its key value before write-protected Partition 2 registers can be written.

Table 5-299. CTRLMMR_MCU_LOCK2_KICK0 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 9008h

Figure 5-94. CTRLMMR_MCU_LOCK2_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 5-301. CTRLMMR_MCU_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

45 CTRLMMR_MCU_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

CTRLMMR_MCU_LOCK2_KICK1 is shown in Figure 5-95 and described in Table 5-211.

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Upper 32-bits of Partition 2 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK2_KICK0 with its key value before write-protected Partition 2 registers can be written.

Table 5-302. CTRLMMR_MCU_LOCK2_KICK1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 900Ch

Figure 5-95. CTRLMMR_MCU_LOCK2_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 5-304. CTRLMMR_MCU_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers

46 CTRLMMR_MCU_M4FSS0_LBIST_CTRL Register (Offset = C020h) [reset = 0h]

CTRLMMR_MCU_M4FSS0_LBIST_CTRL is shown in Figure 5-96 and described in Table 5-213.

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Configures and enables LBIST operation.

Table 5-305. CTRLMMR_MCU_M4FSS0_LBIST_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 C020h

Figure 5-96. CTRLMMR_MCU_M4FSS0_LBIST_CTRL Register

31	30	29	28	27	26	25	24
BIST_RESET	RESERVED			BIST_RUN			
R/W-0h	R-0h			R/W-0h			
23	22	21	20	19	18	17	16
RESERVED			SUBCHIP_ID				
R-0h			R/W-0h				
15	14	13	12	11	10	9	8
RUNBIST_MODE				RESERVED		DC_DEF	
R/W-0h				R-0h		R/W-0h	
7	6	5	4	3	2	1	0
LOAD_DIV	RESERVED		DIVIDE_RATIO				
R/W-0h	R-0h		R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-307. CTRLMMR_MCU_M4FSS0_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_RESET	R/W	0h	This bitfield is not used. The bist_reset control for DMSC is generated by the POST state machine. The bitfield still reflects the efuse value.
30-28	RESERVED	R	0h	Reserved
27-24	BIST_RUN	R/W	0h	This bitfield is not used. The bist_run control for DMSC is generated by the POST state machine. The bitfield still reflects the efuse value.
23-21	RESERVED	R	0h	Reserved
20-16	SUBCHIP_ID	R/W	0h	Specifies which sub-chip is to be tested
15-12	RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1
11-10	RESERVED	R	0h	Reserved
9-8	DC_DEF	R/W	0h	Clock delay after scan_enable switching
7	LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1
6-5	RESERVED	R	0h	Reserved

Table 5-307. CTRLMMR_MCU_M4FSS0_LBIST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio

47 CTRLMMR_MCU_M4FSS0_LBIST_PATCOUNT Register (Offset = C024h) [reset = 0h]

CTRLMMR_MCU_M4FSS0_LBIST_PATCOUNT is shown in Figure 5-97 and described in Table 5-215.

Return to Summary Table.

Specifies the number of LBIST patterns to run.

Table 5-308. CTRLMMR_MCU_M4FSS0_LBIST_PATCOUNT Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 C024h

Figure 5-97. CTRLMMR_MCU_M4FSS0_LBIST_PATCOUNT Register

31	30	29	28	27	26	25	24
RESERVED		STATIC_PC_DEF					
R-0h		R/W-0h					

23	22	21	20	19	18	17	16
STATIC_PC_DEF							
R/W-0h							

15	14	13	12	11	10	9	8
RESERVED				SET_PC_DEF			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
RESET_PC_DEF				SCAN_PC_DEF			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-310. CTRLMMR_MCU_M4FSS0_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run
15-12	RESERVED	R	0h	Reserved
11-8	SET_PC_DEF	R/W	0h	Number of set patterns to run
7-4	RESET_PC_DEF	R/W	0h	Number of reset patterns to run
3-0	SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run

48 CTRLMMR_MCU_M4FSS0_LBIST_SEED0 Register (Offset = C028h) [reset = 0h]

CTRLMMR_MCU_M4FSS0_LBIST_SEED0 is shown in Figure 5-98 and described in Table 5-217.

Return to Summary Table.

Specifies the 32 LSBs of the PRPG seed.

Table 5-311. CTRLMMR_MCU_M4FSS0_LBIST_SEED0 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 C028h

Figure 5-98. CTRLMMR_MCU_M4FSS0_LBIST_SEED0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRPG_DEF																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 5-313. CTRLMMR_MCU_M4FSS0_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0)

49 CTRLMMR_MCU_M4FSS0_LBIST_SEED1 Register (Offset = C02Ch) [reset = 0h]

CTRLMMR_MCU_M4FSS0_LBIST_SEED1 is shown in Figure 5-99 and described in Table 5-219.

Return to Summary Table.

Specifies the 21 MSBs of the PRPG seed.

Table 5-314. CTRLMMR_MCU_M4FSS0_LBIST_SEED1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 C02Ch

Figure 5-99. CTRLMMR_MCU_M4FSS0_LBIST_SEED1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="11">RESERVED</td><td colspan="21">PRPG_DEF</td></tr>
<tr><td colspan="11">R-0h</td><td colspan="21">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-316. CTRLMMR_MCU_M4FSS0_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32)

50 CTRLMMR_MCU_M4FSS0_LBIST_SPARE0 Register (Offset = C030h) [reset = 0h]

CTRLMMR_MCU_M4FSS0_LBIST_SPARE0 is shown in Figure 5-100 and described in Table 5-221.

Return to Summary Table.

Spare LBIST control bits.

Table 5-317. CTRLMMR_MCU_M4FSS0_LBIST_SPARE0 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 C030h

Figure 5-100. CTRLMMR_MCU_M4FSS0_LBIST_SPARE0 Register

31	30	29	28	27	26	25	24
SPARE0							
R/W-0h							

23	22	21	20	19	18	17	16
SPARE0							
R/W-0h							

15	14	13	12	11	10	9	8
SPARE0							
R/W-0h							

7	6	5	4	3	2	1	0
SPARE0						PBIST_SELFTEST_EN	LBIST_SELFTEST_EN
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 5-319. CTRLMMR_MCU_M4FSS0_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	SPARE0	R/W	0h	LBIST spare bits
1	PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control
0	LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control

51 CTRLMMR_MCU_M4FSS0_LBIST_SPARE1 Register (Offset = C034h) [reset = 0h]

CTRLMMR_MCU_M4FSS0_LBIST_SPARE1 is shown in Figure 5-101 and described in Table 5-223.

Return to Summary Table.

Spare LBIST control bits.

Table 5-320. CTRLMMR_MCU_M4FSS0_LBIST_SPARE1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 C034h

Figure 5-101. CTRLMMR_MCU_M4FSS0_LBIST_SPARE1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 5-322. CTRLMMR_MCU_M4FSS0_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE1	R/W	0h	LBIST spare bits

52 CTRLMMR_MCU_M4FSS0_LBIST_STAT Register (Offset = C038h) [reset = X]

CTRLMMR_MCU_M4FSS0_LBIST_STAT is shown in Figure 5-102 and described in Table 5-225.

Return to Summary Table.

Indicates LBIST status and provides MISR selection control.

Table 5-323. CTRLMMR_MCU_M4FSS0_LBIST_STAT Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 C038h

Figure 5-102. CTRLMMR_MCU_M4FSS0_LBIST_STAT Register

31	30	29	28	27	26	25	24
BIST_DONE	RESERVED						
R-X	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIST_RUNNING	RESERVED					OUT_MUX_CTL	
R-X	R-0h					R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MISR_MUX_CTL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-325. CTRLMMR_MCU_M4FSS0_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_DONE	R	X	LBIST is done
30-16	RESERVED	R	0h	Reserved
15	BIST_RUNNING	R	X	LBIST is running
14-10	RESERVED	R	0h	Reserved
9-8	OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 0h - LBIST IP CTRLMMR_MCU_PID value 1h - LBIST CTRL ID value 1x - MISR value
7-0	MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR.

53 CTRLMMR_MCU_M4FSS0_LBIST_MISR Register (Offset = C03Ch) [reset = X]

CTRLMMR_MCU_M4FSS0_LBIST_MISR is shown in Figure 5-103 and described in Table 5-227.

Return to Summary Table.

Contains LBIST MISR output value.

Table 5-326. CTRLMMR_MCU_M4FSS0_LBIST_MISR Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 C03Ch

Figure 5-103. CTRLMMR_MCU_M4FSS0_LBIST_MISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_RESULT																															
R-X																															

LEGEND: R = Read Only; -*n* = value after reset

Table 5-328. CTRLMMR_MCU_M4FSS0_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl

54 CTRLMMR_MCU_LOCK3_KICK0 Register (Offset = D008h) [reset = 0h]

CTRLMMR_MCU_LOCK3_KICK0 is shown in Figure 5-104 and described in Table 5-229.

Return to Summary Table.

Lower 32-bits of Partition3 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK3_KICK1 with its key value before write-protected Partition 3 registers can be written.

Table 5-329. CTRLMMR_MCU_LOCK3_KICK0 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 D008h

Figure 5-104. CTRLMMR_MCU_LOCK3_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-331. CTRLMMR_MCU_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition3 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

55 CTRLMMR_MCU_LOCK3_KICK1 Register (Offset = D00Ch) [reset = 0h]

CTRLMMR_MCU_LOCK3_KICK1 is shown in Figure 5-105 and described in Table 5-231.

Return to Summary Table.

Upper 32-bits of Partition 3 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK3_KICK0 with its key value before write-protected Partition 3 registers can be written.

Table 5-332. CTRLMMR_MCU_LOCK3_KICK1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0450 D00Ch

Figure 5-105. CTRLMMR_MCU_LOCK3_KICK1 Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">KEY</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 5-334. CTRLMMR_MCU_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition3 registers

56 CTRLMMR_MCU_POR_CTRL Register (Offset = 18000h) [reset = 10h]

CTRLMMR_MCU_POR_CTRL is shown in Figure 5-106 and described in Table 5-233.

Return to Summary Table.

Configures POR module reset behavior.

Table 5-335. CTRLMMR_MCU_POR_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8000h

Figure 5-106. CTRLMMR_MCU_POR_CTRL Register

31	30	29	28	27	26	25	24
RESERVED		OVRD_SET5	OVRD_SET4	OVRD_SET3	OVRD_SET2	OVRD_SET1	OVRD_SET0
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		OVRD5	OVRD4	OVRD3	OVRD2	OVRD1	OVRD0
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIM_SEL	RESERVED		MASK_HHV	RESERVED			
R/W-0h	R-0h		R/W-1h	R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-337. CTRLMMR_MCU_POR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	OVRD_SET5	R/W	0h	Reserved override set
28	OVRD_SET4	R/W	0h	POKLVB override set
27	OVRD_SET3	R/W	0h	POKLVA override set
26	OVRD_SET2	R/W	0h	POKHV override set
25	OVRD_SET1	R/W	0h	BGOK override set
24	OVRD_SET0	R/W	0h	PORHV override set
23-22	RESERVED	R	0h	Reserved
21	OVRD5	R/W	0h	Reserved override enable
20	OVRD4	R/W	0h	POKLVB override enable
19	OVRD3	R/W	0h	POKLVA override enable
18	OVRD2	R/W	0h	POKHV override enable

Table 5-337. CTRLMMR_MCU_POR_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	OVRD1	R/W	0h	BGOK override enable
16	OVRD0	R/W	0h	PORHV override enable
15-8	RESERVED	R	0h	Reserved
7	TRIM_SEL	R/W	0h	POR Trim Select 0h - Trim selections for Bandgap and POKs come from HHV defaults 1h - Trim selections for Bandgap and POKs come from CTRLMMR_MCU_POR_BANDGAP_CTRL and POR_POKxxx_CTRL registers
6-5	RESERVED	R	0h	Reserved
4	MASK_HHV	R/W	1h	Mask HHV/SOC_PORz outputs when applying new trim values
3-0	RESERVED	R	0h	Reserved

57 CTRLMMR_MCU_POR_STAT Register (Offset = 18004h) [reset = X]

CTRLMMR_MCU_POR_STAT is shown in Figure 5-107 and described in Table 5-235.

Return to Summary Table.

Shows POR module status.

Table 5-338. CTRLMMR_MCU_POR_STAT Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8004h

Figure 5-107. CTRLMMR_MCU_POR_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							BGOK
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED			SOC_POR	RESERVED			
R-0h			R-X	R-0h			

LEGEND: R = Read Only; -*n* = value after reset

Table 5-340. CTRLMMR_MCU_POR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	BGOK	R	X	Bandgap OK status
7-5	RESERVED	R	0h	Reserved
4	SOC_POR	R	X	POR module status 0h - Module is in functional mode 1h - Module is in reset mode
3-0	RESERVED	R	0h	Reserved

58 CTRLMMR_MCU_POR_BANDGAP_CTRL Register (Offset = 18100h) [reset = X]

CTRLMMR_MCU_POR_BANDGAP_CTRL is shown in Figure 5-108 and described in Table 5-237.

Return to Summary Table.

POR Bandgap Reference Trims.

Table 5-341. CTRLMMR_MCU_POR_BANDGAP_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8100h

Figure 5-108. CTRLMMR_MCU_POR_BANDGAP_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				BGAPI			
R-0h				R/W-X			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BGAPV							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BGAPC							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-343. CTRLMMR_MCU_POR_BANDGAP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	BGAPI	R/W	X	Bandgap output current trim bits
15-8	BGAPV	R/W	X	Bandgap output voltage magnitude trim bits
7-0	BGAPC	R/W	X	Bandgap slope trim bits. Bit7 is used to calculate the offset

59 CTRLMMR_MCU_POK_VDDA_MCU_UV_CTRL Register (Offset = 18110h) [reset = X]

CTRLMMR_MCU_POK_VDDA_MCU_UV_CTRL is shown in Figure 5-109 and described in Table 5-239.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDA_MCU 1P8 Under/Over Voltage Monitors in POR (POKHV, POKLVA).

Table 5-344. CTRLMMR_MCU_POK_VDDA_MCU_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8110h

Figure 5-109. CTRLMMR_MCU_POK_VDDA_MCU_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-346. CTRLMMR_MCU_POK_VDDA_MCU_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

60 CTRLMMR_MCU_POK_VDDA_MCU_OV_CTRL Register (Offset = 18114h) [reset = X]

CTRLMMR_MCU_POK_VDDA_MCU_OV_CTRL is shown in Figure 5-110 and described in Table 5-241.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDA_MCU 1P8 Under/Over Voltage Monitors in POR (POKHV, POKLVA).

Table 5-347. CTRLMMR_MCU_POK_VDDA_MCU_OV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8114h

Figure 5-110. CTRLMMR_MCU_POK_VDDA_MCU_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-349. CTRLMMR_MCU_POK_VDDA_MCU_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

61 CTRLMMR_MCU_POK_VDD_CORE_UV_CTRL Register (Offset = 18118h) [reset = X]

CTRLMMR_MCU_POK_VDD_CORE_UV_CTRL is shown in Figure 5-111 and described in Table 5-243.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDD_CORE Under/Over Voltage Monitors in POR (POKLVB) and POK_VDD_CORE_UV.

Table 5-350. CTRLMMR_MCU_POK_VDD_CORE_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8118h

Figure 5-111. CTRLMMR_MCU_POK_VDD_CORE_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-352. CTRLMMR_MCU_POK_VDD_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

62 CTRLMMR_MCU_POK_VDD_CORE_OV_CTRL Register (Offset = 1811Ch) [reset = X]

CTRLMMR_MCU_POK_VDD_CORE_OV_CTRL is shown in Figure 5-112 and described in Table 5-245.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDD_CORE Under/Over Voltage Monitors in POR (POKLVB) and POK_VDD_CORE_UV.

Table 5-353. CTRLMMR_MCU_POK_VDD_CORE_OV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 811Ch

Figure 5-112. CTRLMMR_MCU_POK_VDD_CORE_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-355. CTRLMMR_MCU_POK_VDD_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

63 CTRLMMR_MCU_POK_VDDR_CORE_UV_CTRL Register (Offset = 18120h) [reset = X]

CTRLMMR_MCU_POK_VDDR_CORE_UV_CTRL is shown in Figure 5-113 and described in Table 5-247.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDR_CORE Under/Over Voltage Monitor.

Table 5-356. CTRLMMR_MCU_POK_VDDR_CORE_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8120h

Figure 5-113. CTRLMMR_MCU_POK_VDDR_CORE_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-358. CTRLMMR_MCU_POK_VDDR_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

64 CTRLMMR_MCU_POK_VDDR_CORE_OV_CTRL Register (Offset = 18124h) [reset = X]

CTRLMMR_MCU_POK_VDDR_CORE_OV_CTRL is shown in Figure 5-114 and described in Table 5-249.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDR_CORE Under/Over Voltage Monitor.

Table 5-359. CTRLMMR_MCU_POK_VDDR_CORE_OV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8124h

Figure 5-114. CTRLMMR_MCU_POK_VDDR_CORE_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-361. CTRLMMR_MCU_POK_VDDR_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

65 CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_UV_CTRL Register (Offset = 18128h) [reset = X]

CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_UV_CTRL is shown in Figure 5-115 and described in Table 5-251.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDSHV_MCU_1P8 Under/Over Voltage Monitor.

Table 5-362. CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8128h

Figure 5-115. CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 5-364. CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

66 CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_OV_CTRL Register (Offset = 1812Ch) [reset = X]

CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_OV_CTRL is shown in Figure 5-116 and described in Table 5-253.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDSHV_MCU_1P8 Under/Over Voltage Monitor.

Table 5-365. CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_OV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 812Ch

Figure 5-116. CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-367. CTRLMMR_MCU_POK_VDDSHV_MCU_1P8_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

67 CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_UV_CTRL Register (Offset = 18130h) [reset = X]

CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_UV_CTRL is shown in Figure 5-117 and described in Table 5-255.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDSHV_MCU_3P3 Under/Over Voltage Monitor.

Table 5-368. CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8130h

Figure 5-117. CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-370. CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

68 CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_OV_CTRL Register (Offset = 18134h) [reset = X]

CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_OV_CTRL is shown in Figure 5-118 and described in Table 5-257.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDSHV_MCU_3P3 Under/Over Voltage Monitor.

Table 5-371. CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_OV_CTRL Instances

Instance	**Physical Address**
MCU_CTRL_MMR0	0451 8134h

Figure 5-118. CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-373. CTRLMMR_MCU_POK_VDDSHV_MCU_3P3_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

69 CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register (Offset = 18138h) [reset = X]

CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_UV_CTRL is shown in Figure 5-119 and described in Table 5-259.

Return to Summary Table.

Hysterisis, Threshold, and Control of VMON_CAP_MCU_GENERAL Under/Over Voltage Monitor.

Table 5-374. CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8138h

Figure 5-119. CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-376. CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

70 CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register (Offset = 1813Ch) [reset = X]

CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_OV_CTRL is shown in Figure 5-120 and described in Table 5-261.

Return to Summary Table.

Hysterisis, Threshold, and Control of VMON_CAP_MCU_GENERAL Under/Over Voltage Monitor.

Table 5-377. CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 813Ch

Figure 5-120. CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 5-379. CTRLMMR_MCU_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

71 CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_UV_CTRL Register (Offset = 18140h) [reset = X]

CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_UV_CTRL is shown in Figure 5-121 and described in Table 5-263.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDSHV_MAIN_1P8 Under/Over Voltage Monitor.

Table 5-380. CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8140h

Figure 5-121. CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-382. CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

72 CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_OV_CTRL Register (Offset = 18144h) [reset = X]

CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_OV_CTRL is shown in Figure 5-122 and described in Table 5-265.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDSHV_MAIN_1P8 Under/Over Voltage Monitor.

Table 5-383. CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_OV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8144h

Figure 5-122. CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-385. CTRLMMR_MCU_POK_VDDSHV_MAIN_1P8_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

73 CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_UV_CTRL Register (Offset = 18148h) [reset = X]

CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_UV_CTRL is shown in Figure 5-123 and described in Table 5-267.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDSHV_MAIN_3P3 Under/Over Voltage Monitor.

Table 5-386. CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8148h

Figure 5-123. CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-388. CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

74 CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_OV_CTRL Register (Offset = 1814Ch) [reset = X]

CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_OV_CTRL is shown in Figure 5-124 and described in Table 5-269.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDSHV_MAIN_3P3 Under/Over Voltage Monitor.

Table 5-389. CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_OV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 814Ch

Figure 5-124. CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-391. CTRLMMR_MCU_POK_VDDSHV_MAIN_3P3_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

75 CTRLMMR_MCU_POK_VDDS_DDRIO_UV_CTRL Register (Offset = 18150h) [reset = X]

CTRLMMR_MCU_POK_VDDS_DDRIO_UV_CTRL is shown in Figure 5-125 and described in Table 5-271.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDS_DDRIO Under/Over Voltage Monitor.

Table 5-392. CTRLMMR_MCU_POK_VDDS_DDRIO_UV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8150h

Figure 5-125. CTRLMMR_MCU_POK_VDDS_DDRIO_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-394. CTRLMMR_MCU_POK_VDDS_DDRIO_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

76 CTRLMMR_MCU_POK_VDDS_DDRIO_OV_CTRL Register (Offset = 18154h) [reset = X]

CTRLMMR_MCU_POK_VDDS_DDRIO_OV_CTRL is shown in Figure 5-126 and described in Table 5-273.

Return to Summary Table.

Hysterisis, Threshold, and Control of VDDS_DDRIO Under/Over Voltage Monitor.

Table 5-395. CTRLMMR_MCU_POK_VDDS_DDRIO_OV_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8154h

Figure 5-126. CTRLMMR_MCU_POK_VDDS_DDRIO_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-397. CTRLMMR_MCU_POK_VDDS_DDRIO_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK Trim Bits

77 CTRLMMR_MCU_POK_VDDA_PMIC_IN_CTRL Register (Offset = 18160h) [reset = 80000000h]

CTRLMMR_MCU_POK_VDDA_PMIC_IN_CTRL is shown in Figure 5-127 and described in Table 5-275.

Return to Summary Table.

Hysterisis and Control of VDDA_PMIC_IN Under/Over Voltage Monitor.

Table 5-398. CTRLMMR_MCU_POK_VDDA_PMIC_IN_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8160h

Figure 5-127. CTRLMMR_MCU_POK_VDDA_PMIC_IN_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OVER_VOLT_DET	RESERVED						
R/W-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-400. CTRLMMR_MCU_POK_VDDA_PMIC_IN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-16	RESERVED	R	0h	Reserved
15	OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
14-0	RESERVED	R	0h	Reserved

78 CTRLMMR_MCU_RST_CTRL Register (Offset = 18170h) [reset = 20FFFh]

CTRLMMR_MCU_RST_CTRL is shown in Figure 5-128 and described in Table 5-277.

Return to Summary Table.

Controls Reset Assertion and Propogation.

Table 5-401. CTRLMMR_MCU_RST_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8170h

Figure 5-128. CTRLMMR_MCU_RST_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					MCU_RESET_ISO_DONE_Z	MCU_ESM_ERROR_RST_EN_Z	DMSC_COLD_RESET_EN_Z
R-0h					R/W-0h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				SW_MCU_WARMRST			
R-0h				R/W-Fh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW_MAIN_POR				SW_MAIN_WARMRST			
R/W-Fh				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-403. CTRLMMR_MCU_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	MCU_RESET_ISO_DONE_Z	R/W	0h	MCU can set this bit to block warm reset in the main domain which is useful when the MCU may be accessing main domain resources (peripherals, memory..). In this case, the MCU will be notified via an interrupt that there is an outstanding warm reset request for the main domain. Once notified, MCU needs to finish any outstanding operations in has with main domain resources and then clear this bit. After this bit is cleared, the main domain warm reset will unblocked and the warm reset sequence may continue. 0h - Reset of MAIN domain is not Blocked by MCU Domain 1h - Reset of MAIN domain is Blocked by MCU Domain
17	MCU_ESM_ERROR_RST_EN_Z	R/W	1h	Disable Reset of MCU by ESM 0h - Enabled 1h - Disabled

Table 5-403. CTRLMMR_MCU_RST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	DMSC_COLD_RESET_EN_Z	R/W	0h	Disable Reset of MCU by DMSC 0h - Enabled 1h - Disabled
15-12	RESERVED	R	0h	Reserved
11-8	SW_MCU_WARMRST	R/W	Fh	This is a fault tolerant bitfield. Causes MCU Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111
7-4	SW_MAIN_POR	R/W	Fh	This is a fault tolerant bitfield. Causes MAIN domain Power On Reset when set to 4'b0110, Bits will reset to 4'b1111
3-0	SW_MAIN_WARMRST	R/W	Fh	This is a fault tolerant bitfield. Causes MAIN domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111

79 CTRLMMR_MCU_RST_STAT Register (Offset = 18174h) [reset = X]

CTRLMMR_MCU_RST_STAT is shown in Figure 5-129 and described in Table 5-279.

Return to Summary Table.

Reset Status.

Table 5-404. CTRLMMR_MCU_RST_STAT Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8174h

Figure 5-129. CTRLMMR_MCU_RST_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							MAIN_RESETSTATZ
R-0h							R-X

LEGEND: R = Read Only; -*n* = value after reset

Table 5-406. CTRLMMR_MCU_RST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MAIN_RESETSTATZ	R	X	Status of MAIN domain Reset: 0 = Reset Asserted 1 = Reset Deasserted

80 CTRLMMR_MCU_RST_SRC Register (Offset = 18178h) [reset = 0h]

CTRLMMR_MCU_RST_SRC is shown in Figure 5-130 and described in Table 5-281.

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Captures Reason for Warm and MAIN domain Power On Resets.

Table 5-407. CTRLMMR_MCU_RST_SRC Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8178h

Figure 5-130. CTRLMMR_MCU_RST_SRC Register

31	30	29	28	27	26	25	24
SAFETY_ERROR	MAIN_ESM_ERROR	RESERVED				SW_MAIN_POR_FROM_MAIN	SW_MAIN_POR_FROM_MCU
W1TC-0h	W1TC-0h	R-0h				W1TC-0h	W1TC-0h
23	22	21	20	19	18	17	16
RESERVED		SW_MAIN_WARMRST_FROM_MAIN	SW_MAIN_WARMRST_FROM_MCU	RESERVED			SW_MCU_WARMRST
R-0h		W1TC-0h	W1TC-0h	R-0h			W1TC-0h
15	14	13	12	11	10	9	8
RESERVED		WARM_OUT_RST	COLD_OUT_RST	RESERVED			DEBUG_RST
R-0h		W1TC-0h	W1TC-0h	R-0h			W1TC-0h
7	6	5	4	3	2	1	0
RESERVED			THERMAL_RST	RESERVED	MAIN_RESET_REQ	RESERVED	MCU_RESET_PIN
R-0h			W1TC-0h	R-0h	W1TC-0h	R-0h	W1TC-0h

LEGEND: W1TC = Write 1 to Clear Bit; FEC = Falling Edge Capture; R = Read Only; REC = Rising Edge Capture-*n* = value after reset

Table 5-409. CTRLMMR_MCU_RST_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SAFETY_ERROR	W1TC	0h	Reset Caused by MCU ESM Error
30	MAIN_ESM_ERROR	W1TC	0h	Reset Caused by Main ESM Error
29-26	RESERVED	R	0h	Reserved
25	SW_MAIN_POR_FROM_MAIN	W1TC	0h	Software Main Power On Reset From MAIN CTRL MMR
24	SW_MAIN_POR_FROM_MCU	W1TC	0h	Software Main Power On Reset From MCU CTRL MMR
23-22	RESERVED	R	0h	Reserved
21	SW_MAIN_WARMRST_FROM_MAIN	W1TC	0h	Software Main Warm Reset from MAIN CTRL MMR
20	SW_MAIN_WARMRST_FROM_MCU	W1TC	0h	Software Main Warm Reset From MCU CTRL MMR
19-17	RESERVED	R	0h	Reserved
16	SW_MCU_WARMRST	W1TC	0h	Software Warm Reset

Table 5-409. CTRLMMR_MCU_RST_SRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	WARM_OUT_RST	W1TC	0h	DMSC Warm Reset
12	COLD_OUT_RST	W1TC	0h	DMSC Cold Reset
11-9	RESERVED	R	0h	Reserved
8	DEBUG_RST	W1TC	0h	Debug Subsystem Initiated Reset
7-5	RESERVED	R	0h	Reserved
4	THERMAL_RST	W1TC	0h	Thermal Reset
3	RESERVED	R	0h	Reserved
2	MAIN_RESET_REQ	W1TC	0h	Main Reset Pin
1	RESERVED	R	0h	Reserved
0	MCU_RESET_PIN	W1TC	0h	Rest Caused by MCU Reset Pin

81 CTRLMMR_MCU_RST_MAGIC_WORD Register (Offset = 1817Ch) [reset = 0h]

CTRLMMR_MCU_RST_MAGIC_WORD is shown in Figure 5-131 and described in Table 5-283.

Return to Summary Table.

After an MCU_PORz reset this bit field resets to 0x00000000. While this bit field remains 0x00000000 any warm reset from the MAIN domain also propagates through the MCU domain. If the application does not require reset isolation of the MCU domain, it may leave this bit field with a value of 0x00000000. If the application does require reset isolation of the MCU domain after the initial boot, then the M4FSS CPU must write a nonzero value to the magic word. The actual value is left to software and different values may be used to convey information, but in order to isolate the MCU domain from all MAIN domain warm reset sources that trigger main_resetz, the value must be non-zero. If the value is nonzero and one of the MAIN domain warm reset sources triggers main_resetz occurs in the main domain, the M4FSS will not be reset. The MAIN domain bootloader must read this value to determine that the M4FSS is already initialized, and has configured reset isolation. The MAIN domain bootloader then also skips any initialization steps involving bootstrapping the M4FSS as it is is already running. Note that MCU_PORz reset is never blocked by a nonzero magic word.

Table 5-410. CTRLMMR_MCU_RST_MAGIC_WORD Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 817Ch

Figure 5-131. CTRLMMR_MCU_RST_MAGIC_WORD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCU_MAGIC_WORD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 5-412. CTRLMMR_MCU_RST_MAGIC_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MCU_MAGIC_WORD	R/W	0h	After a MCU_PORz reset this bit field resets to 0x00000000. While this bit field remains 0x00000000 any reset from the MAIN domain also propagates through the MCU domain. If the application does not require reset isolation of the MCU domain, it shall leave this bit field with a value of 0x00000000. If the application does require reset isolation of the MCU domain after the initial boot, then the M4FSS CPU must write a nonzero value to the magic word. The actual value is left to software and different values may be used to convey information, but in order to isolate the MCU domain from any warm reset sources that triggers main_resetz, the value must be non-zero. If the value is nonzero and a Main domainMAIN domain warm reset that triggers main_resetz occurs in the main domain, the M4FSS will not be reset. The Main domainMAIN domain bootloader must read this value to determine that the M4FSS is already initialized, and has configured reset isolation. The Main domainMAIN domain bootloader then also skips any initialization steps involving bootstrapping the M4FSS (as it is is already running). Note that MCU_PORz reset is never blocked by a nonzero magic word.

82 CTRLMMR_MCU_ISO_CTRL Register (Offset = 18180h) [reset = 0h]

CTRLMMR_MCU_ISO_CTRL is shown in Figure 5-132 and described in Table 5-285.

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Controls isolation of M4FSS from MAIN domain logic: M4FSS shall always be configured with mcu_dbg_iso_en set when deployed in a safety MCU use case. M4FSS must set mcu_rst_iso_en must be set before asserting mcu_reset_iso_done_z CTRLMMR_MCU_RST_MAGIC_WORD mcu_dbg_iso_en mcu_rst_iso_en 0 x x M4FSS General Purpose Use Case: No Isolation 1 x x M4FSS Safety MCU Use Cases: 1 0 0 Not Isolated 1 0 1 For Development Only: Reset Isolated but Debuggable. 1 1 0 Debug Isolated, but not Reset Isolated 1 1 1 Deployment: M4FSS is Reset and Debug Isolated.

Table 5-413. CTRLMMR_MCU_ISO_CTRL Instances

Instance	**Physical Address**
MCU_CTRL_MMR0	0451 8180h

Figure 5-132. CTRLMMR_MCU_ISO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						MCU_DBG_ISO_EN	MCU_RST_ISO_EN
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-415. CTRLMMR_MCU_ISO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	MCU_DBG_ISO_EN	R/W	0h	Isolates the MCU domain from Debug 0h - M4FSS is not debug isolated 1h - M4FSS is isolated from debug if CTRLMMR_MCU_RST_MAGIC_WORD is also nonzero
0	MCU_RST_ISO_EN	R/W	0h	Isolates the MCU domain from Warm Reset initiated by Main 0h - M4FSS is not reset isolated 1h - M4FSS is isolated from main warm reset if CTRLMMR_MCU_RST_MAGIC_WORD is also nonzero

83 CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Register (Offset = 18190h) [reset = X]

CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL is shown in Figure 5-133 and described in Table 5-287.

Return to Summary Table.

Controls the voltage glitch detector circuit monitoring the VDD_CORE voltage domain.

Table 5-416. CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8190h

Figure 5-133. CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Register

31	30	29	28	27	26	25	24
PWDB	RSTB	RESERVED					
R/W-0h	R/W-0h	R-0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					LP_FILTER_SEL		
R-0h					R/W-X		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		THRESH_HI_SEL					
R-0h		R/W-X					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		THRESH_LO_SEL					
R-0h		R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-418. CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PWDB	R/W	0h	Power down - active low. 0h - Disable all functions 1h - Enable glitch detectors
30	RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must be not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0h - Reset glitch detector flags 1h - Glitch detection flags are enabled
29-19	RESERVED	R	0h	Reserved

Table 5-418. CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-16	LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth 0h - 150 kHz 1h - 125 kHz 2h - 100 kHz 3h - 80 kHz 4h - 60 kHz 5h - 45 kHz 6h - 30 kHz 7h - 15 kHz
15-14	RESERVED	R	0h	Reserved

Table 5-418. CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-8	THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage 0h - 93.5% of VDD 1h - 94.0% of VDD 2h - 94.5% of VDD 3h - 95.0% of VDD 4h - 95.5% of VDD 5h - 96.0% of VDD 6h - 96.5% of VDD 7h - 97.0% of VDD 8h - 97.5% of VDD 9h - 98.0% of VDD Ah - 98.5% of VDD Bh - 99.0% of VDD Ch - 99.5% of VDD Dh - 100.0% of VDD Eh - 100.5% of VDD Fh - 101.0% of VDD 10h - 101.5% of VDD 11h - 102.0% of VDD 12h - 102.5% of VDD 13h - 103.0% of VDD 14h - 103.5% of VDD 15h - 104.0% of VDD 16h - 104.5% of VDD 17h - 105.0% of VDD 18h - 105.5% of VDD 19h - 106.0% of VDD 1Ah - 106.5% of VDD 1Bh - 107.0% of VDD 1Ch - 107.5% of VDD 1Dh - 108.0% of VDD 1Eh - 108.5% of VDD 1Fh - 109.0% of VDD 20h - 109.5% of VDD 21h - 110.0% of VDD 22h - 111.0% of VDD

Table 5-418. CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				23h - 112.0% of VDD 24h - 113.0% of VDD 25h - 114.0% of VDD 26h - 115.0% of VDD 27h - 116.0% of VDD 28h - 117.0% of VDD 29h - 118.0% of VDD 2Ah - 119.0% of VDD 2Bh - 120.0% of VDD 2Ch - 121.0% of VDD 2Dh - 122.0% of VDD 2Eh - 123.0% of VDD 2Fh - 124.0% of VDD 30h - 125.0% of VDD 31h - 126.0% of VDD 32h - 127.0% of VDD 33h - 128.0% of VDD 34h - 129.0% of VDD 35h - 130.0% of VDD 36h - 131.0% of VDD 37h - 132.0% of VDD 38h - 133.0% of VDD 39h - 134.0% of VDD 3Ah - 135.0% of VDD 3Bh - 136.0% of VDD 3Ch - 137.0% of VDD 3Dh - 138.0% of VDD 3Eh - 139.0% of VDD 3Fh - 140.0% of VDD
7-6	RESERVED	R	0h	Reserved

Table 5-418. CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage 0h - 106.5% of VDD 1h - 106.0% of VDD 2h - 105.5% of VDD 3h - 105.0% of VDD 4h - 104.5% of VDD 5h - 104.0% of VDD 6h - 103.5% of VDD 7h - 103.0% of VDD 8h - 102.5% of VDD 9h - 102.0% of VDD Ah - 101.5% of VDD Bh - 101.0% of VDD Ch - 100.5% of VDD Dh - 100.0% of VDD Eh - 99.5% of VDD Fh - 99.0% of VDD 10h - 98.5% of VDD 11h - 98.0% of VDD 12h - 97.5% of VDD 13h - 97.0% of VDD 14h - 96.5% of VDD 15h - 96.0% of VDD 16h - 95.5% of VDD 17h - 95.0% of VDD 18h - 94.5% of VDD 19h - 94.0% of VDD 1Ah - 93.5% of VDD 1Bh - 93.0% of VDD 1Ch - 92.5% of VDD 1Dh - 92.0% of VDD 1Eh - 91.5% of VDD 1Fh - 91.0% of VDD 20h - 90.5% of VDD 21h - 90.0% of VDD 22h - 89.0% of VDD

Table 5-418. CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				23h - 88.0% of VDD 24h - 87.0% of VDD 25h - 86.0% of VDD 26h - 85.0% of VDD 27h - 84.0% of VDD 28h - 83.0% of VDD 29h - 82.0% of VDD 2Ah - 81.0% of VDD 2Bh - 80.0% of VDD 2Ch - 79.0% of VDD 2Dh - 78.0% of VDD 2Eh - 77.0% of VDD 2Fh - 76.0% of VDD 30h - 75.0% of VDD 31h - 74.0% of VDD 32h - 73.0% of VDD 33h - 72.0% of VDD 34h - 71.0% of VDD 35h - 70.0% of VDD 36h - 69.0% of VDD 37h - 68.0% of VDD 38h - 67.0% of VDD 39h - 66.0% of VDD 3Ah - 65.0% of VDD 3Bh - 64.0% of VDD 3Ch - 63.0% of VDD 3Dh - 62.0% of VDD 3Eh - 61.0% of VDD 3Fh - 60.0% of VDD

84 CTRLMMR_MCU_VDD_CORE_GLDTC_STAT Register (Offset = 181B0h) [reset = X]

CTRLMMR_MCU_VDD_CORE_GLDTC_STAT is shown in Figure 5-134 and described in Table 5-289.

Return to Summary Table.

Shows the status of the voltage glitch detector circuit monitoring the VDD_CORE voltage domain.

Table 5-419. CTRLMMR_MCU_VDD_CORE_GLDTC_STAT Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 81B0h

Figure 5-134. CTRLMMR_MCU_VDD_CORE_GLDTC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							THRESH_HI_FLAG
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED							THRESH_LOW_FLAG
R-0h							R-X

LEGEND: R = Read Only; -*n* = value after reset

Table 5-421. CTRLMMR_MCU_VDD_CORE_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. 0h - No high voltage detected 1h - Voltage above the high voltage threshold was detected.
7-1	RESERVED	R	0h	Reserved
0	THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. 0h - No low voltage detected 1h - Voltage below the low voltage threshold was detected.

85 CTRLMMR_MCU_PRG_PP_0_CTRL Register (Offset = 18200h) [reset = 2001Fh]

CTRLMMR_MCU_PRG_PP_0_CTRL is shown in Figure 5-135 and described in Table 5-291.

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Configures PRG_PP_0 - Fixed POKs (In POR, POKSA, and POK_VDD_CORE_OV).

Table 5-422. CTRLMMR_MCU_PRG_PP_0_CTRL Instances

Instance	**Physical Address**
MCU_CTRL_MMR0	0451 8200h

Figure 5-135. CTRLMMR_MCU_PRG_PP_0_CTRL Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">DEGLITCH_SEL</td></tr>
<tr><td colspan="6">R-0h</td><td colspan="2">R/W-2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>POK_EN_SEL</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>POK_VDDA_PMIC_IN_UV_EN</td><td>POK_VDD_MCU_OV_EN</td><td>POK_VDD_MCU_UV_EN</td><td>POK_VDDA_MCU_OV_EN</td><td>POK_VDDA_MCU_UV_EN</td></tr>
<tr><td colspan="3">R-0h</td><td>R/W-1h</td><td>R/W-1h</td><td>R/W-1h</td><td>R/W-1h</td><td>R/W-1h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-424. CTRLMMR_MCU_PRG_PP_0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	DEGLITCH_SEL	R/W	2h	Deglitch period for PRG_PP0 POKs: 0h - 5 us 1h -10 us 2h - 15 us 3h - 20us
15	POK_EN_SEL	R/W	0h	Select POK enable source 0h - POK enables come from hardware tie-offs 1h - POK enables come from PRG_PP0_CTRL register
14-5	RESERVED	R	0h	Reserved
4	POK_VDDA_PMIC_IN_UV_EN	R/W	1h	Enable VDDA_PMIC_IN undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
3	POK_VDD_MCU_OV_EN	R/W	1h	Enable VDD_MCU overvoltage POK detection 0h - POK detection disabled 1h - POK detection enabled

Table 5-424. CTRLMMR_MCU_PRG_PP_0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	POK_VDD_MCU_UV_EN	R/W	1h	Enable VDD_MCU undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
1	POK_VDDA_MCU_OV_EN	R/W	1h	Enable 1.8V VDDA_MCU overvoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
0	POK_VDDA_MCU_UV_EN	R/W	1h	Enable 1.8V VDDA_MCU undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled

86 CTRLMMR_MCU_PRG_PP_1_CTRL Register (Offset = 18208h) [reset = 2007Fh]

CTRLMMR_MCU_PRG_PP_1_CTRL is shown in Figure 5-136 and described in Table 5-293.

Return to Summary Table.

Configures PRG_PP_1 - Ping-Pong Capable POKs.

Table 5-425. CTRLMMR_MCU_PRG_PP_1_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8208h

Figure 5-136. CTRLMMR_MCU_PRG_PP_1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED				POK_PP_EN	RESERVED	DEGLITCH_SEL	
R-0h				R/W-0h	R-0h	R/W-2h	

15	14	13	12	11	10	9	8
POK_EN_SEL	POK_VDDS_DDRIO_OV_SEL	POK_VDDSHV_MAIN_3P3_OV_SEL	POK_VDDSHV_MAIN_1P8_OV_SEL	POK_VMON_CAP_MCU_GENERAL_OV_SEL	POK_VDDSHV_MCU_3P3_OV_SEL	POK_VDDSHV_MCU_1P8_OV_SEL	POK_VDDR_CORE_OV_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
RESERVED	POK_VDDS_DDRIO_EN	POK_VDDSHV_MAIN_3P3_EN	POK_VDDSHV_MAIN_1P8_EN	POK_VMON_CAP_MCU_GENERAL_EN	POK_VDDSHV_MCU_3P3_EN	POK_VDDSHV_MCU_1P8_EN	POK_VDDR_CORE_EN
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-427. CTRLMMR_MCU_PRG_PP_1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	POK_PP_EN	R/W	0h	POK ping-pong enable. When set, enablesautomatic switching between undervoltage andovervoltage detection on PRG_PP1 (POK_VDDR_CORE, POK_VDDSHV_MCU_1P8, POK_VDDSHV_MCU_3P3, POK_VMON_CAP_MCU_GENERAL, POK_VDDSHV_MAIN_1P8, POK_VDDSHV_MAIN_3P3, and POK_VDDS_DDRIO) POKs. This bit has no effect if the POK's ov_sel bit = 1. 0h - No pingpong operation. UV/OV operationselected by each POK ov_sel bit 1h - Pingpong operation enabled .
18	RESERVED	R	0h	Reserved

Table 5-427. CTRLMMR_MCU_PRG_PP_1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	DEGLITCH_SEL	R/W	2h	Deglitch period for PRG_PP1 POKs: 0h - 5 us 1h -10 us 2h - 15 us 3h - 20us
15	POK_EN_SEL	R/W	0h	Select POK enable source 0h - POK enables come from hardware tie-offs 1h - POK enables come from PRG_PP1_CTRL register
14	POK_VDDS_DDRIO_OV_SEL	R/W	0h	POK_VDDS_DDRIO mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x)
13	POK_VDDSHV_MAIN_3P3_OV_SEL	R/W	0h	POK_VDDSHV_MAIN_3P3 mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x)
12	POK_VDDSHV_MAIN_1P8_OV_SEL	R/W	0h	POK_VDDSHV_MAIN_1P8 mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x)
11	POK_VMON_CAP_MCU_GENERAL_OV_SEL	R/W	0h	POK_VMON_CAP_MCU_GENERAL mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x)
10	POK_VDDSHV_MCU_3P3_OV_SEL	R/W	0h	POK_VDDSHV_MCU_3P3 mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x)
9	POK_VDDSHV_MCU_1P8_OV_SEL	R/W	0h	POK_VDDSHV_MCU_1P8 mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x)
8	POK_VDDR_CORE_OV_SEL	R/W	0h	POK_VDDR_CORE Mode: 0 = Undervoltage (pok_pp_en = 0) Ping-Pong (pok_pp_en = 1) 1 = Overvoltage (pok_pp_en = x)
7	RESERVED	R	0h	Reserved
6	POK_VDDS_DDRIO_EN	R/W	1h	Enable POK_VDDS_DDRIO (if pok_en_sel = 1): 0 = POK Detection Disabled 1 = POK Detection Enabled

Table 5-427. CTRLMMR_MCU_PRG_PP_1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	POK_VDDSHV_MAIN_3P3_EN	R/W	1h	Enable POK_VDDSHV_MAIN_3P3 (if pok_en_sel = 1): 0 = POK Detection Disabled 1 = POK Detection Enabled
4	POK_VDDSHV_MAIN_1P8_EN	R/W	1h	Enable POK_VDDSHV_MAIN_1P8 (if pok_en_sel = 1): 0 = POK Detection Disabled 1 = POK Detection Enabled
3	POK_VMON_CAP_MCU_GENERAL_EN	R/W	1h	Enable POK_VMON_CAP_MCU_GENERAL (if pok_en_sel = 1): 0 = POK Detection Disabled 1 = POK Detection Enabled
2	POK_VDDSHV_MCU_3P3_EN	R/W	1h	Enable POK_VDDSHV_MCU_3P3 (if pok_en_sel = 1): 0 = POK Detection Disabled 1 = POK Detection Enabled
1	POK_VDDSHV_MCU_1P8_EN	R/W	1h	Enable POK_VDDSHV_MCU_1P8 (if pok_en_sel = 1): 0 = POK Detection Disabled 1 = POK Detection Enabled
0	POK_VDDR_CORE_EN	R/W	1h	Enable POK_VDDR_CORE (if pok_en_sel = 1): 0 = POK Detection Disabled 1 = POK Detection Enabled

87 CTRLMMR_MCU_CLKGATE_CTRL Register (Offset = 18284h) [reset = X]

CTRLMMR_MCU_CLKGATE_CTRL is shown in Figure 5-137 and described in Table 5-295.

Return to Summary Table.

Controls the power clock gating feature of MCU domain modules and busses.

Table 5-428. CTRLMMR_MCU_CLKGATE_CTRL Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8284h

Figure 5-137. CTRLMMR_MCU_CLKGATE_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							MCU_M4FSS_NOGATE
R-0h							R/W-X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						MCU_CBA_ECC_AGGR_NOGATE	MCU_CBA_NOGATE
R-0h						R/W-X	R/W-X

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-430. CTRLMMR_MCU_CLKGATE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	MCU_M4FSS_NOGATE	R/W	X	MCU domain M4FSS0 clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
7-2	RESERVED	R	0h	Reserved
1	MCU_CBA_ECC_AGGR_NOGATE	R/W	X	MCU domain Pulsar clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
0	MCU_CBA_NOGATE	R/W	X	MCU domain Data bus (mcu_cbass) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled

88 CTRLMMR_MCU_MAIN_CLKGATE_CTRL0 Register (Offset = 18288h) [reset = X]

CTRLMMR_MCU_MAIN_CLKGATE_CTRL0 is shown in Figure 5-138 and described in Table 5-297.

Return to Summary Table.

Controls the power clock gating feature of MAIN domain modules and busses.

Table 5-431. CTRLMMR_MCU_MAIN_CLKGATE_CTRL0 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 8288h

Figure 5-138. CTRLMMR_MCU_MAIN_CLKGATE_CTRL0 Register

31	30	29	28	27	26	25	24
MAIN_DMSC_NOGATE	RESERVED		MAIN_DBG_CBA_NOGATE	RESERVED	MAIN_R5FSS1_NOGATE	MAIN_R5FSS0_NOGATE	MAIN_TIMERMGR_NOGATE
R/W-X	R-0h		R/W-X	R-0h	R/W-X	R/W-X	R/W-X
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		MAIN_ICSSG1_NOGATE	MAIN_ICSSG0_NOGATE	RESERVED	MAIN_PDMA1_NOGATE	MAIN_PDMA0_NOGATE	MAIN_DMSS_NOGATE
R-0h		R/W-X	R/W-X	R-0h	R/W-X	R/W-X	R/W-X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAIN_GIC500_NOGATE	RESERVED				MAIN_A53_0_DBG_NOGATE	MAIN_A53_0_CFG_NOGATE	MAIN_A53_0_ACP_NOGATE
R/W-X	R-0h				R/W-X	R/W-X	R/W-X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAIN_A53_0_NOGATE	MAIN_CBA_ECC_AGG_NOGATE	MAIN_FW_CBA_NOGATE	MAIN_CBA_NOGATE	RESERVED	MAIN_INFRA_ECC_AGG_NOGATE	RESERVED	MAIN_INFRA_CBA_NOGATE
R/W-X	R/W-X	R/W-X	R/W-X	R-0h	R/W-X	R-0h	R/W-X

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-433. CTRLMMR_MCU_MAIN_CLKGATE_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_DMSC_NOGATE	R/W	X	MAIN domain DMSC (pwr_dis_nogate) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
30-29	RESERVED	R	0h	Reserved
28	MAIN_DBG_CBA_NOGATE	R/W	X	MAIN domain Debug bus clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
27	RESERVED	R	0h	Reserved
26	MAIN_R5FSS1_NOGATE	R/W	X	MAIN domain R5FSS1 clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled

Table 5-433. CTRLMMR_MCU_MAIN_CLKGATE_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	MAIN_R5FSS0_NOGATE	R/W	X	MAIN domain R5FSS0 clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
24	MAIN_TIMERMGR_NOGATE	R/W	X	MAIN domain TIMERMGR (pwr_dis_nogate) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
23-22	RESERVED	R	0h	Reserved
21	MAIN_ICSSG1_NOGATE	R/W	X	MAIN domain ICSSG1 clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
20	MAIN_ICSSG0_NOGATE	R/W	X	MAIN domain ICSSG0 clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
19	RESERVED	R	0h	Reserved
18	MAIN_PDMA1_NOGATE	R/W	X	MAIN domain PDMA1 (pwr_dis_nogate) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
17	MAIN_PDMA0_NOGATE	R/W	X	MAIN domain PDMA0 (pwr_dis_nogate) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
16	MAIN_DMSS_NOGATE	R/W	X	MAIN domain DMSS (pwr_dis_nogate) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
15	MAIN_GIC500_NOGATE	R/W	X	MAIN A53SS0 (gic500_1_2) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
14-11	RESERVED	R	0h	Reserved
10	MAIN_A53_0_DBG_NOGATE	R/W	X	MAIN A53SS0 Debug Port clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
9	MAIN_A53_0_CFG_NOGATE	R/W	X	MAIN A53SS0 Configuration Port clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
8	MAIN_A53_0_ACP_NOGATE	R/W	X	MAIN A53SS0 ACP clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
7	MAIN_A53_0_NOGATE	R/W	X	MAIN A53SS0 clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled

Table 5-433. CTRLMMR_MCU_MAIN_CLKGATE_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	MAIN_CBA_ECC_AGG_NOGATE	R/W	X	MAIN domain data bus ECC aggragator (main_cba_ecc_aggr_main_0) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
5	MAIN_FW_CBA_NOGATE	R/W	X	MAIN domain datal bus (main_fw_cbass) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
4	MAIN_CBA_NOGATE	R/W	X	MAIN domain data bus (main_cbass) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
3	RESERVED	R	0h	Reserved
2	MAIN_INFRA_ECC_AGG_NOGATE	R/W	X	MAIN domain Infrastructure ECC aggragator (main_infra_ecc_aggr) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled
1	RESERVED	R	0h	Reserved
0	MAIN_INFRA_CBA_NOGATE	R/W	X	MAIN domain Infrastructure bus (main_infra_cbass) clock gate disable. 0h - Clocks are gated on idle for power savings 1h - Clocks are not gated on idle, power saving disabled

89 CTRLMMR_MCU_LOCK6_KICK0 Register (Offset = 19008h) [reset = 0h]

CTRLMMR_MCU_LOCK6_KICK0 is shown in Figure 5-139 and described in Table 5-299.

Return to Summary Table.

Lower 32-bits of Partition6 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK6_KICK1 with its key value before write-protected Partition 6 registers can be written.

Table 5-434. CTRLMMR_MCU_LOCK6_KICK0 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 9008h

Figure 5-139. CTRLMMR_MCU_LOCK6_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 5-436. CTRLMMR_MCU_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition6 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

90 CTRLMMR_MCU_LOCK6_KICK1 Register (Offset = 1900Ch) [reset = 0h]

CTRLMMR_MCU_LOCK6_KICK1 is shown in Figure 5-140 and described in Table 5-301.

Return to Summary Table.

Upper 32-bits of Partition 6 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK6_KICK0 with its key value before write-protected Partition 6 registers can be written.

Table 5-437. CTRLMMR_MCU_LOCK6_KICK1 Instances

Instance	Physical Address
MCU_CTRL_MMR0	0451 900Ch

Figure 5-140. CTRLMMR_MCU_LOCK6_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 5-439. CTRLMMR_MCU_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition6 registers

5.2 Power

This chapter describes the power-management architecture implemented in the device.

The Power Management content is presented in several general sections:

- Power Management Subsystems (System and Control Modules)
- Device Power States
- Dynamic and Thermal Management

5.2.1 Power Management Overview

Power management architecture of the device is built over three levels of power controls: clock-, power-, and voltage supplies to the subsystem modules, referred to as domains. A domain is a group of modules or subsections of the device that share a common entity (for example, common clock source, common voltage source, or common power switch).

A set of Power Domains (PD) are defined for the device, where clock and power supplies to the domain may be controlled by Power Sleep Controllers (PSC), see *Power Sleep Controller and Local Power Sleep Controllers*. This section describes functionality of PSC, as well as list of power domains, control registers and hierarchical dependencies of PDs.

One or multiple power domains may share a single power supply, this level of grouping are referred as Voltage Domains (VD). Some voltage domains may be turned off by externally switching off the power supplies to these domains. *Device Power-Management Layout* provide a list of VDs and corresponding PDs.

Device power states are defined based on the combination of VD and PD ON/OFF states, as described in *Device Power States*.

Initial configuration of the device clocking tree and power domains, as well as power state transitions, may be complex due to hierarchical dependencies. Thus a Device Management and Security Controller (DMSC) is integrated to off-load some of these tasks from main controllers. DMSC also serves as a wake-up controller and generator, maintaining minimum hardware state machines when all programmable cores are turned off. Power management functions of the DMSC are described in *DMSC-L Power Management Overview*, for functional reference. Standard applications shall use the DMSC Firmware APIs to perform high-level power management functions.

Additional hardware modules for temperature sensing, thermal management, power monitoring, and reset functions related to power ramping, are described in *Power System Modules*.

Figure 5-141 shows the overview of the common power management of the device.

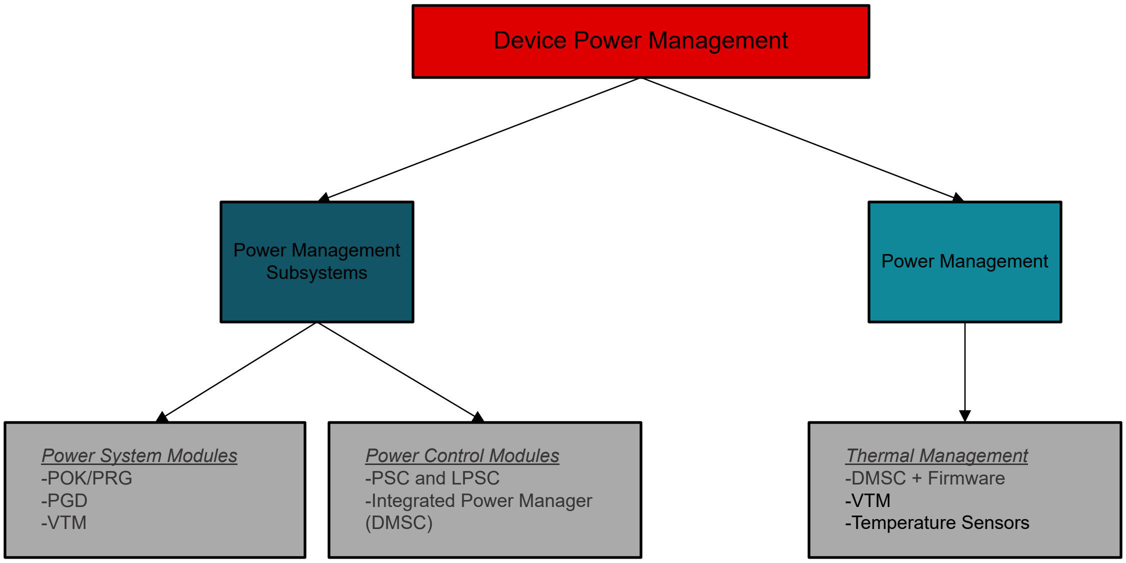

Figure 5-141. Overview of Common Power Management

5.2.2 Power Management Subsystems

5.2.2.1 Power Management Unit

The Power Management Unit in AM64x consists of a Safety system.

- **Safety System:**

  The Safety System contains the safety comparators and temperature sensor to monitor the system supplies and temperature. The glitch filtered output of the voltage monitors is connected to the Error Signaling Module (ESM) and provide an error signal if the supply is not within the voltage thresholds set for the individual monitored supplies.

5.2.2.1.1 Power OK (POK) Modules

Note

All POK modules are in MCU domain regardless of the domain of the voltage they monitor.

Note

In this family of devices, the Power-on-reset module is used only for voltage monitoring, as three additional POK modules. For more information about POK functionality in POR module - voltage being monitored and type (under voltage or over voltage), see *Power on Reset (POR) Module*.

POK modules are responsible for accurately detecting the voltage levels. Each module is trimmed to account for process and temperature variations. The trim values are provided by eFuse chains enabled by a POR/Reset Generator (PRG) module.

Two types of POK modules are implemented in this family of devices - POK and POK_SA. See Table 5-302 about the type of a POK and the voltage it is monitoring. More information about the two types of POKs is given further in this section.

Table 5-440. POK Module Overview

POK Module Instance Name	PRG Index	POK Index[1]	Voltage Monitored	Module Type	OV/UV[2]	Description
IPOK_VDDA_PMIC_IN	PRG0	3	VMON_VSYS	POK_SA	UV	Voltage Monitor for PMIC_IN
IPOK_VDD_CORE_OV	PRG0	4	VDD_CORE	POK_CORE	OV	Voltage Monitor for VDD_CORE
IPOK_VDDS_DDRIO	PRG1	6	VDDS_DDR	POK_CORE	UV/OV	Voltage Monitors for DDRIO
IPOK_VDDR_CORE	PRG1	5	VDDR_CORE	POK_CORE	UV/OV	Voltage Monitors for VDDR_CORE
IPOK_VDDSHV_MCU_3P3	PRG1	4	VMON_3P3_MCU	POK_3P3	UV/OV	Voltage Monitors for 3.3-V I/O supply in MCU
IPOK_VDDS_MCU_1P8	PRG1	3	VMON_1P8_MCU	POK_1P8	UV/OV	Voltage Monitors for 1.8-V I/O supply in MCU
IPOK_VDDS_CAP_MCU	PRG1	2	CAP_VDDS_MCU	POK_1P8	UV/OV	Voltage Monitors for MCU mid-rail
IPOK_VDDS_MAIN_1P8	PRG1	1	VMON_1P8_SOC	POK_1P8	UV/OV	Voltage Monitors for 1.8-V I/O/PLL supply
IPOK_VDDSHV_MAIN_3P3	PRG1	0	VMON_3P3_SOC	POK_3P3	UV/OV	Voltage Monitors for 3.3-V I/O/PLL supply

1. The POK Index also represents the mapping index for relevant under and overvoltage status and interrupts where applicable.
2. UV: POK is set for undervoltage detection. OV: POK is set for overvoltage detection. UV/OV: POK monitors both OV and UV through a Ping-Pong mechanism.

Figure 5-142 and Figure 5-143 represent the block diagrams of the two POK types.

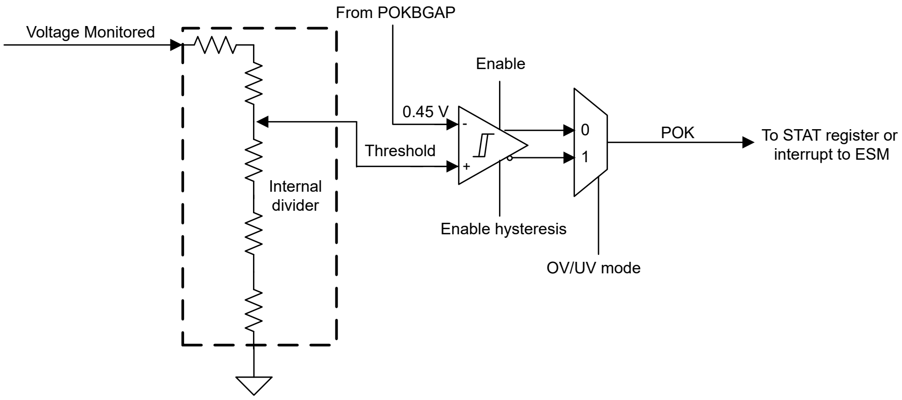

Figure 5-142. POK Block Diagram

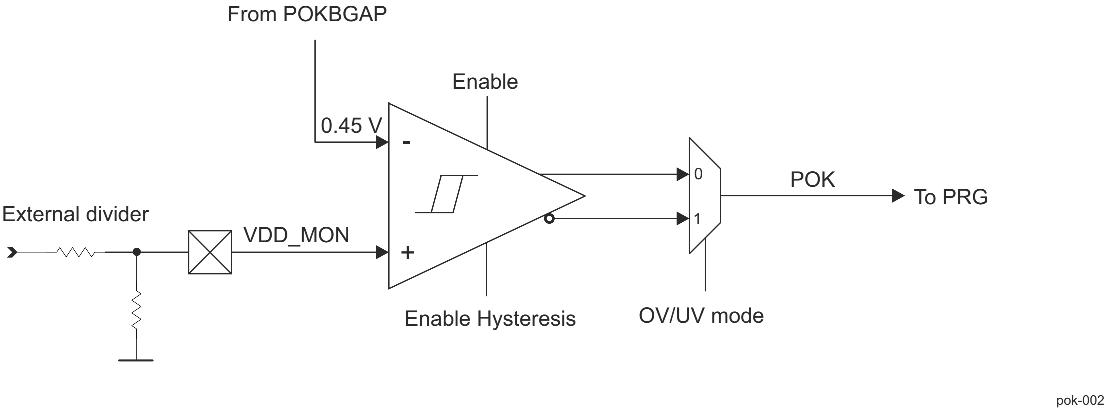

Figure 5-143. POK_SA Block Diagram

Vref for both POK and POK_SA types in Figure 5-142 and Figure 5-143 is supplied from POR module, see *Power on Reset (POR) Module*.

5.2.2.1.1.1 Configuration Registers

Configuration registers needed for POK (Supervisor Module) are given in Table 5-303. For each POK there is one comparator that is controlled through the registers. These registers decide the functionality of the POK Comparator. It decides if it is UV/OV mode and also the threshold voltages.

Comparator threshold levels and corresponding configuration register settings are given in the following tables:

- POK_CORE: Table 5-304
- POK_1P8: Table 5-305
- POK_3P3: Table 5-306

Table 5-441. POK Configuration Registers

Register Name	POK Type
MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL[7:0]	POK_1P8

Table 5-441. POK Configuration Registers (continued)

Register Name	POK Type
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL[7:0]	POK_3P3
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL[7:0]	POK_3P3
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL[7:0]	POK_3P3
MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL[7:0]	POK_3P3
MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL[7:0]	POK_CORE

Table 5-442. Bit Settings of POK_CORE with VMON Threshold Values

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Under Voltage Detection) hys_en=0	0	000 0000	0.4743
	0	000 0001	0.4875
	0	000 0010	0.5000
	0	000 0011	0.5125
	0	000 0100	0.5250
	0	000 0101	0.5375
	0	000 0110	0.5513
	0	000 0111	0.5631
	0	000 1000	0.5754
	0	000 1001	0.5883
	0	000 1010	0.6017
	0	000 1011	0.6122
	0	000 1100	0.6268
	0	000 1101	0.6382
	0	000 1110	0.6500
	0	000 1111	0.6623
	0	001 0000	0.6750
	0	001 0001	0.6882
	0	001 0010	0.7020
	0	001 0011	0.7115
	0	001 0100	0.7262
	0	001 0101	0.7363
	0	001 0110	0.7521
	0	001 0111	0.7630
	0	001 1000	0.7742
	0	001 1001	0.7858
	0	001 1010	0.7977
	0	001 1011	0.8100
	0	001 1100	0.8226
	0	001 1101	0.8356
	0	001 1110	0.8491
	0	001 1111	0.8630
	0	010 0000	0.8774
	0	010 0001	0.8848
	0	010 0010	0.8999
	0	010 0011	0.9155
	0	010 0100	0.9235
	0	010 0101	0.9400
	0	010 0110	0.9485
	0	010 0111	0.9659
	0	010 1000	0.9748
	0	010 1001	0.9839

Table 5-442. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Under Voltage Detection) hys_en=0	0	010 1010	1.0030
	0	010 1011	1.0120
	0	010 1100	1.0220
	0	010 1101	1.0320
	0	010 1110	1.0530
	0	010 1111	1.0630
	0	011 0000	1.0740
	0	011 0001	1.0850
	0	011 0010	1.0970
	0	011 0011	1.1140
	0	011 0100	1.1260
	0	011 0101	1.1380
	0	011 0110	1.1510
	0	011 0111	1.1630
	0	011 1000	1.1760
	0	011 1001	1.1900
	0	011 1010	1.1960
	0	011 1011	1.2100
	0	011 1100	1.2240
	0	011 1101	1.2380
	0	011 1110	1.2530
	0	011 1111	1.2610
	0	100 0000	1.2760
	0	100 0001	1.2920
	0	100 0010	1.3000
	0	100 0011	1.3160
	0	100 0100	1.3240
	0	100 0101	1.3410
	0	100 0110	1.3500
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	000 0000	0.7262
	1	000 0001	0.7363
	1	000 0010	0.7521
	1	000 0011	0.7630
	1	000 0100	0.7743
	1	000 0101	0.7858
	1	000 0110	0.7977
	1	000 0111	0.8100
	1	000 1000	0.8226
	1	000 1001	0.8357
	1	000 1010	0.8491
	1	000 1011	0.8630
	1	000 1100	0.8774

Table 5-442. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	000 1101	0.8848
	1	000 1110	0.8999
	1	000 1111	0.9155
	1	001 0000	0.9236
	1	001 0001	0.9400
	1	001 0010	0.9485
	1	001 0011	0.9659
	1	001 0100	0.9748
	1	001 0101	0.9839
	1	001 0110	1.0030
	1	001 0111	1.0120
	1	001 1000	1.0220
	1	001 1001	1.0320
	1	001 1010	1.0530
	1	001 1011	1.0630
	1	001 1100	1.0740
	1	001 1101	1.0850
	1	001 1110	1.0970
	1	001 1111	1.1140
	1	010 0000	1.1260
	1	010 0001	1.1380
	1	010 0010	1.1510
	1	010 0011	1.1630
	1	010 0100	1.1760
	1	010 0101	1.1900
	1	010 0110	1.1960
	1	010 0111	1.2100
	1	010 1000	1.2240
	1	010 1001	1.2380
	1	010 1010	1.2530
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	010 1011	1.2610
	1	010 1100	1.2760
	1	010 1101	1.2920
	1	010 1110	1.3000
	1	010 1111	1.3160
	1	011 0000	1.3240
	1	011 0001	1.3410
	1	011 0010	1.3500
	1	011 0011	1.3670
	1	011 0100	1.3760
	1	011 0101	1.3850
	1	011 0110	1.4040

Table 5-442. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	011 0111	1.4130
	1	011 1000	1.4230
	1	011 1001	1.4420
	1	011 1010	1.4520
	1	011 1011	1.4620
	1	011 1100	1.4720
	1	011 1101	1.4830
	1	011 1110	1.5040
	1	011 1111	1.5150
	1	100 0000	1.5260
	1	100 0001	1.5370
	1	100 0010	1.5480
	1	100 0011	1.5600
	1	100 0100	1.5710
	1	100 0101	1.5830
	1	100 0110	1.5950
	1	100 0111	1.6070
	1	100 1000	1.6200
	1	100 1001	1.6320
	1	100 1010	1.6450

Table 5-443. Bit Settings of POK_1P8 with VMON Threshold Values

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.44V - 2.173V**
Over Voltage Detection	**1**	**XXX XXXX**	**1.44V - 2.173V**
POK_1P8 (Under Voltage Detection) hys_en=0	0	010 0000	1.44
	0	010 0001	1.452
	0	010 0010	1.477
	0	010 0011	1.502
	0	010 0100	1.515
	0	010 0101	1.543
	0	010 0110	1.556
	0	010 0111	1.585
	0	010 1000	1.6
	0	010 1001	1.615
	0	010 1010	1.645
	0	010 1011	1.661
	0	010 1100	1.677
	0	010 1101	1.694
	0	010 1110	1.728
	0	010 1111	1.745
	0	011 0000	1.763
	0	011 0001	1.781
	0	011 0010	1.799
	0	011 0011	1.828
	0	011 0100	1.848
	0	011 0101	1.868
	0	011 0110	1.888
	0	011 0111	1.909
	0	011 1000	1.93
	0	011 1001	1.952
	0	011 1010	1.963
	0	011 1011	1.986
	0	011 1100	2.009
	0	011 1101	2.032
	0	011 1110	2.056
	0	011 1111	2.069
	0	100 0000	2.094
	0	100 0001	2.12
	0	100 0010	2.133
	0	100 0011	2.159
	0	100 0100	2.173
POK_1P8 (Under Voltage Detection) hys_en=0	1	000 1100	1.44
	1	000 1101	1.452
	1	000 1110	1.477
	1	000 1111	1.502
	1	001 0000	1.515

Table 5-443. Bit Settings of POK_1P8 with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.44V - 2.173V**
Over Voltage Detection	**1**	**XXX XXXX**	**1.44V - 2.173V**
POK_1P8 (Under Voltage Detection) hys_en=0	1	001 0001	1.543
	1	001 0010	1.556
	1	001 0011	1.585
	1	001 0100	1.6
	1	001 0101	1.615
	1	001 0110	1.645
	1	001 0111	1.661
	1	001 1000	1.677
	1	001 1001	1.694
	1	001 1010	1.728
	1	001 1011	1.745
	1	001 1100	1.763
	1	001 1101	1.781
	1	001 1110	1.799
	1	001 1111	1.828
	1	010 0000	1.848
	1	010 0001	1.868
	1	010 0010	1.888
	1	010 0011	1.909
	1	010 0100	1.93
	1	010 0101	1.952
	1	010 0110	1.963
	1	010 0111	1.986
	1	010 1000	2.009
	1	010 1001	2.032
	1	010 1010	2.056
	1	010 1011	2.069
	1	010 1100	2.094
	1	010 1101	2.12
	1	010 1110	2.133
	1	010 1111	2.159
	1	011 0000	2.173

Table 5-444. Bit Settings of POK_3P3 with VMON Threshold Values

POK Programmability	**POK Configuration Register bits**		**THRESHOLD (V)**
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Under Voltage Detection) hys_en=0	0	000 0000	1.427
	0	000 0001	1.466
	0	000 0010	1.501
	0	000 0011	1.545
	0	000 0100	1.576
	0	000 0101	1.616
	0	000 0110	1.658
	0	000 0111	1.694
	0	000 1000	1.731
	0	000 1001	1.769
	0	000 1010	1.81
	0	000 1011	1.841
	0	000 1100	1.885
	0	000 1101	1.919
	0	000 1110	1.955
	0	000 1111	1.992
	0	001 0000	2.03
	0	001 0001	2.07
	0	001 0010	2.111
	0	001 0011	2.14
	0	001 0100	2.184
	0	001 0101	2.215
	0	001 0110	2.262
	0	001 0111	2.295
	0	001 1000	2.329
	0	001 1001	2.363
	0	001 1010	2.399
	0	001 1011	2.436
	0	001 1100	2.474
	0	001 1101	2.513
	0	001 1110	2.554
	0	001 1111	2.596
	0	010 0000	2.639
	0	010 0001	2.661
	0	010 0010	2.706
	0	010 0011	2.753
	0	010 0100	2.778
	0	010 0101	2.827
	0	010 0110	2.853
	0	010 0111	2.905
	0	010 1000	2.932
	0	010 1001	2.959

Table 5-444. Bit Settings of POK_3P3 with VMON Threshold Values (continued)

POK Programmability	**POK Configuration Register bits**		**THRESHOLD (V)**
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Under Voltage Detection) hys_en=0	0	010 1010	3.015
	0	010 1011	3.044
	0	010 1100	3.074
	0	010 1101	3.104
	0	010 1110	3.166
	0	010 1111	3.198
	0	011 0000	3.231
	0	011 0001	3.264
	0	011 0010	3.298
	0	011 0011	3.35
	0	011 0100	3.386
	0	011 0101	3.423
	0	011 0110	3.46
	0	011 0111	3.498
	0	011 1000	3.538
	0	011 1001	3.577
	0	011 1010	3.598
	0	011 1011	3.639
	0	011 1100	3.681
	0	011 1101	3.724
	0	011 1110	3.769
	0	011 1111	3.791
	0	100 0000	3.837
	0	100 0001	3.884
	0	100 0010	3.908
	0	100 0011	3.957
	0	100 0100	3.982
POK_3P3 (Over Voltage Detection) hys_en=0	1	000 0000	2.184
	1	000 0001	2.215
	1	000 0010	2.262
	1	000 0011	2.295
	1	000 0100	2.329
	1	000 0101	2.363
	1	000 0110	2.399
	1	000 0111	2.436
	1	000 1000	2.474
	1	000 1001	2.513
	1	000 1010	2.554
	1	000 1011	2.596
	1	000 1100	2.639
	1	000 1101	2.661
	1	000 1110	2.707

Table 5-444. Bit Settings of POK_3P3 with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Over Voltage Detection) hys_en=0	1	000 1111	2.754
	1	001 0000	2.778
	1	001 0001	2.827
	1	001 0010	2.853
	1	001 0011	2.905
	1	001 0100	2.932
	1	001 0101	2.959
	1	001 0110	3.016
	1	001 0111	3.045
	1	001 1000	3.074
	1	001 1001	3.104
	1	001 1010	3.166
	1	001 1011	3.198
	1	001 1100	3.231
	1	001 1101	3.264
	1	001 1110	3.298
	1	001 1111	3.35
	1	010 0000	3.386
	1	010 0001	3.423
	1	010 0010	3.46
	1	010 0011	3.499
	1	010 0100	3.538
	1	010 0101	3.578
	1	010 0110	3.598
	1	010 0111	3.639
	1	010 1000	3.682
	1	010 1001	3.725
	1	010 1010	3.769
	1	010 1011	3.792
	1	010 1100	3.838
	1	010 1101	3.885
	1	010 1110	3.909
	1	010 1111	3.958

5.2.2.1.2 Power on Reset (POR) Module

This section describes the Power on Reset (POR) module.

5.2.2.1.2.1 POR Overview

POR module in this family of devices is responsible for detecting proper operating voltage levels on VDDA_MCU (under voltage), and both under and over voltages for analog supply in MCU domain.

Table 5-307 shows POR modules allocation within device domains.

Table 5-445. POR Modules Allocation within Device Domains

Module Instance	Domain	
	MCU	MAIN
POR0	✓	-

5.2.2.1.2.2 POR Integration

The device supports one instance of a Power on Reset (POR) module - MCU_POR0. MCU_POR0 is located in MCU domain. Figure 5-144 shows the integration of MCU_POR0.

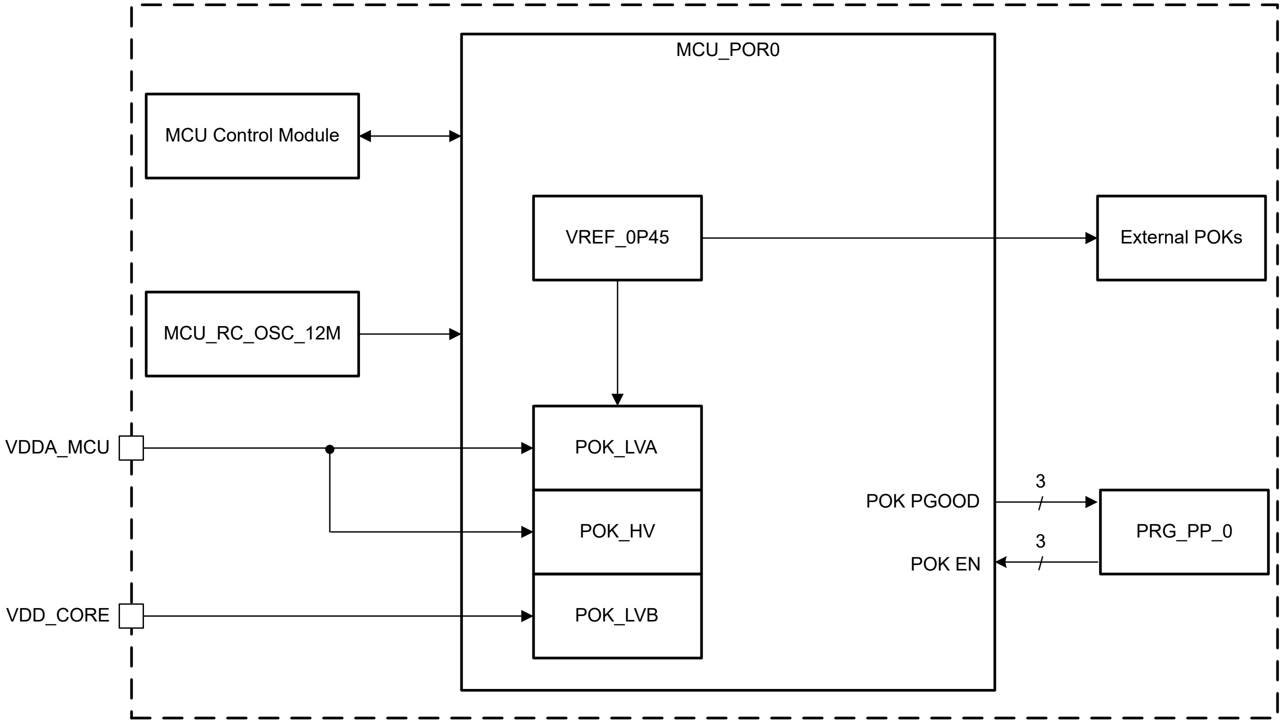

Figure 5-144. POR Integration

Table 5-446. POR Modules

POR Module Instance Name	PRG Index	POK Index	Voltage Monitored	Description	Module Type	OV/UV1
POKHV	PRG0	2	VDDA_MCU	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE	POR	UV

Table 5-446. POR Modules (continued)

POR Module Instance Name	PRG Index	POK Index	Voltage Monitored	Description	Module Type	OV/UV1
POKLVA	PRG0	1	VDDA_MCU	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE	POR	OV
POKLVB	PRG0	0	VDD_CORE	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE	POR	UV

1. UV: POK is set for under voltage detection. OV: POK is set for over voltagedetection. UV/OV: POK monitors both OV and UV via Ping-Pong mechanism.

5.2.2.1.3 PoR/Reset Generator (PRG) Modules

This device has two PoR/Reset Generator (PRG) modules – PRG_PP_0 and PRG_PP_1. Both of these modules are located in the MCU domain.

5.2.2.1.3.1 PRG Overview

A PRG module is responsible for implementing enable/disable controls and event/interrupt masking logic on all POK outputs.

Figure 5-145 shows the PRG module overview.

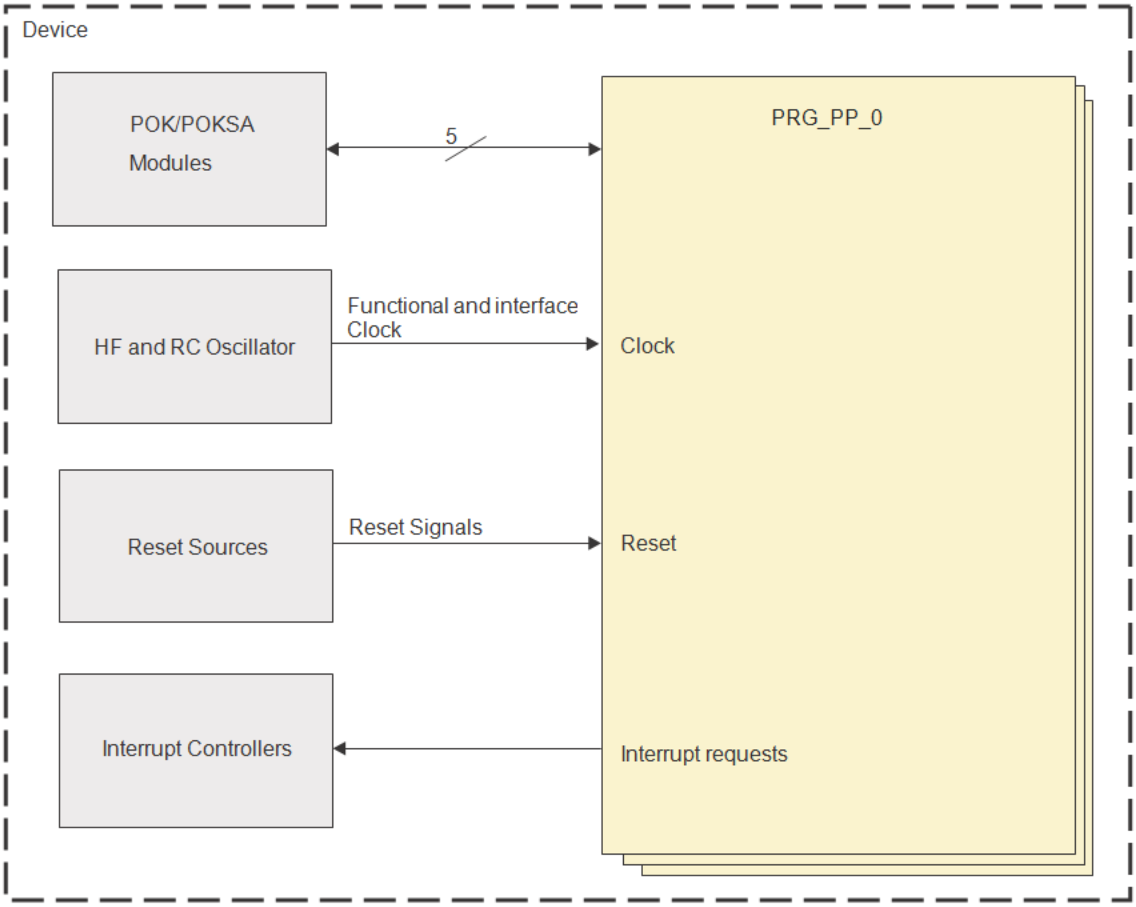

Figure 5-145. PRG0 Overview

Figure 5-146 shows the PRG module overview.

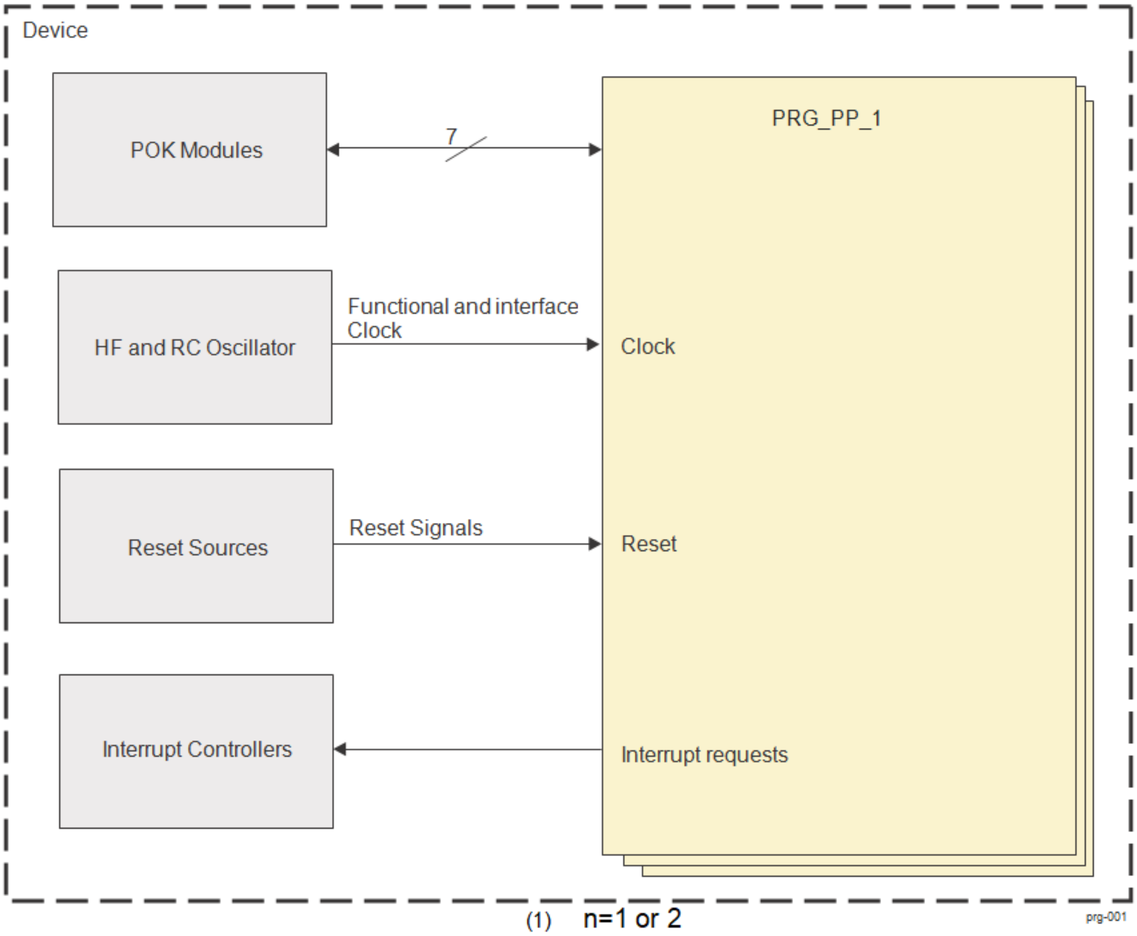

Figure 5-146. PRG1 Overview

5.2.2.1.4 Power Glitch Detect (PGD) Modules

A Power Glitch Detect (PGD) circuit is used to detect short duration “glitches” on the core and MPU power supplies. The PGD provides a low output when no glitch is detected and a high output when a glitch is detected.

Table 5-309 shows PGD modules allocation within device domains.

Table 5-447. PGD Modules Allocation within Device Domains

Module Instance	Domain		
	WKUP	MCU	MAIN
PGD0	-	-	✓

Figure 5-147 shows the PGD block diagram.

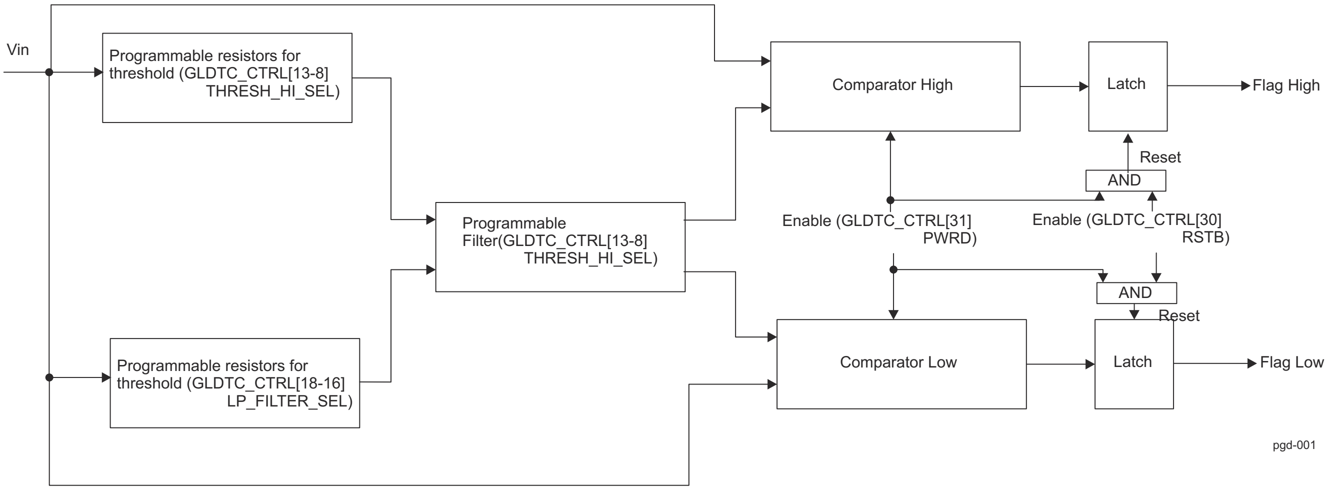

Figure 5-147. PGD Block Diagram

Table 5-310 summarize the PGD integration.

Table 5-448. PGD Integration Summary

Module Instance	Monitored Voltage	PGD Control Register	PGD Status Register
PGD0	VDD_CORE	CTRLMMR_MCU_VDD_CORE_GLDTC_CTRL	CTRLMMR_MCU_VDD_CORE_GLDTC_STAT

Table 5-449. PGD Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
PGD0	VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG	ESM_LVL_EVENT_IN_101	ESM0	PGD0 Threshold High flag level interrupt	Level
	VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG	ESM_LVL_EVENT_IN_102	ESM0	PGD0 Threshold Low flag level interrupt	Level

---

Note

A flag status bit in corresponding STAT register is cleared by clearing the [30] RSTB bit in the corresponding CTRL register, see for STAT and CTRL registers for a certain PGD module.

Note

For more information on the interconnects, see *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within *Device Configuration*.

For more information on the device interrupt controllers, see *Interrupt Controllers*.

5.2.2.1.5 Voltage and Thermal Manager (VTM)

5.2.2.1.5.1 VTM Overview

This section describes the Voltage and Thermal Manager (VTM) module in the device.

The VTM module on the AM64x supports voltage and thermal management of the device by providing control of on-chip temperature sensors.

The device supports a single VTM module, VTM0, which is located in the MAIN domain. VTM0 has two associated temperature monitors, ITemp_Sensor_Main_0, located near the A53 subsystem, and ITemp_Sensor_Main_1, located near the DDR Phy and controller.

Figure 5-148 shows VTM module allocation within device domains.

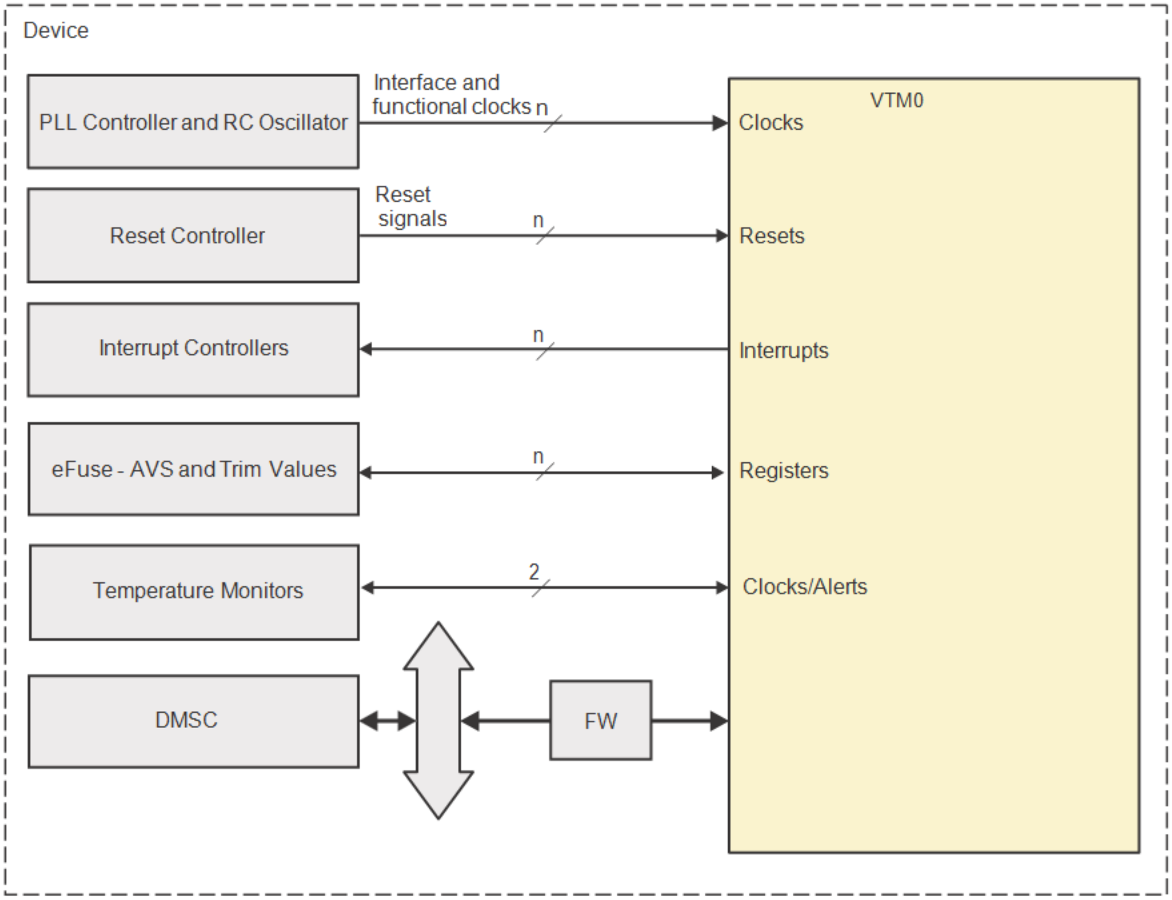

Figure 5-148. VTM Overview

5.2.2.1.5.1.1 VTM Features

VTM module supports the following features:

- Programming of temperature-crossing thresholds
- Signals when programed thresholds are exceeded - up to 3 alerts:
  - Three full reference 10-bit temperature threshold points, THPT1, THPT2 and THPT0.
  - Two relative 4-bit delta values vs THPT1 (one an increment and another a decrement), each able to set additional threshold point, THPT2 and THPT0.
- Supports up to 8 temperature monitors
- Allows resolution of 0.5°C for temperature reading and threshold point temperature alert/interrupt generation.
- Supports PMIC/LDO set-up with Class-0 VDD-VID settings
- Support of tentative customization of OPP voltage per device (in support of multiple OPPs)

- AVS-voltage or thermal management for up to 8 voltage domains
- Maximum temperature alert
- Supports one shot sampling mode and continuous monitoring mode for the sensors
- Contains registers with reset defaults from e-fuse values needed to supports SR-Class0 via e-fuse/ manufacturing calibration and firmware and/or software using those values to program the PMIC/LDO with the Class-0 VDD-VID setting.
- Contains registers with reset defaults from e-fuse values per SOC for a tentative customization of OPP voltage per device (in support of multiple OPPs/DVFS).
- Supports a group of regsiters for up to 8 core voltage domains that require AVS-voltage management or thermal management in a contiguous memory region to support access privilege control by Firewall within its address space.
- Core voltage domains that don't require any SR-Class0 or thermal management shall not be controlled or map to any of the MCU_VTM0 voltage domain group.
- Contains registers with reset defaults from e-fuse values or TIE-OFFs to provide control for temperature monitors and interrupt generation needed to support thermal management customized if necessary in a per voltage domain basis.
- Provides register control, status and interrupt generation, and alerts for up to 8 temperature monitors.
- Stores in the registers the defaults for temperature detection threshold points and other temperature monitor control values for Firmware usage.
- Samples, captures, and allows for register read of the on-die temperature monitor present reading.
- Provides interrupt and status for out of range temperature reading.
- Provides one full reference 10-bit temperature threshold point, THPT1.
- Provides 2 relative 3-bit delta values versus THPT1, one an increment and another a decrement, which yields 2 additional threshold points, THPT2 and THPT0, in close proximity to THPT1.
- Provides 3 temperature threshold point alert signals (level), GT_TH1_ALERT, GT_TH2_ALERT and LT_TH0_ALERT, for each one of the up to 8 temperature monitors.
- Provides 3 temperature threshold point interrupt flags, GT_TH1_INT, GT_TH2_INT and LT_TH0_INT, for each one of the up to 8 voltage domains.
- Provides 3 temperature threshold point interrupts (level-only) for the entire MCU_VTM0, GT_TH1_INT, GT_TH2_INT and LT_TH0_INT, which are driven out of MCU_VTM0 and are shared by the 8 voltage domains. The output port interrupts correspond to the OR function of the contributions of the 8 voltage domains.
- Software must read the corresponding flags in each of the 8 voltage domains to identify which voltage domain is active.
- Allows for temperature reading and threshold point temperature alert and interrupt generation with 0.5°C of resolution.

Note

The VTM in this family of devices implements two temperature monitors.

5.2.2.1.5.1.2 VTM Not Supported Features

- No support for AVS-Class0 with temperature compensation (AVS0 + TC)
- No support internal to MCU_VTM0 for any AVS Class technology other than Class0
- No support for K1 or K2 4/6-bit VCNTL/VID parallel or 2-step interfaces.
- No integrated I2C inside VTM
- No direct hardware triggering of I2C transactions by VTM. Only interrupt and event generation is supported.
- No support for voltage and thermal management of I/O voltage domains. Only core domain voltage/thermal management is supported.
- VTM0 does not contain or support register groups or control hooks for I/O voltage domains.
- Core voltage domains that do not require any voltage or thermal management are not controlled or mapped to any of the VTM0 voltage domain groups.
- Everything else not explicitly listed in Section 5.2.2.1.5.1.1 is not supported.
- No oversampling of the temperature reading

- No support for eFuse defaults of all register values

5.2.2.1.5.2 VTM Functional Description

5.2.2.1.5.2.1 VTM Temperature Status and Thermal Management

VTM module provides temperature reading and interrupt/alert information for thermal management.

VTM controls the temperature monitors in the die. A single VTM can control up to 8 monitors via its registers. The VTM enables the sensors periodically to keep the reported data continually updated becuase the device sensors are not periodical. The temperature value coming back from the monitor is captured and reported by the VTM registers. The VTM keeps the sensors in reset state when not enabled to save power and reduce sensor usage to maximize the sensor life.

Note

A temperature diode sensor is used to measure silicon junction temperature, for more information about temperature diode, see the device-specific Datasheet.

5.2.2.1.5.2.1.1 10-bit Temperature Values Versus Temperature

Table 5-312 shows a table lookup method for translating code to temperature from temperature monitors which correspond to the temperature measured read from the VTM0_VTM_TMPSENS_STAT_J [9-0] DATA_OUT bitfields. Table 5-312 also provides the values for the temperatures coded in VTM0_VTM_MISC_CTRL2 [25-16] MAXT_OUTRG_ALERT_THR0 and VTM0_VTM_MISC_CTRL2 [9-0] MAXT_OUTRG_ALERT_THR thresholds.

Table 5-450. Temperature Translation Table

Parameter Type	Value								
Temperature [°C] (rounded)	-40	-25	0	25	50	75	100	125	150
Temperature [°C] (unrounded)	-40.03	-24.95	0.01	25.02	49.94	75.03	100.02	124.97	150.00
DATA_OUT Code	28	77	164	260	366	485	620	773	949

Table 5-313 shows a table that gives coefficients of polynomial to calculate code or temperature. The equation to calculate code or temperature is:

$y = a4 \times x^4 + a3 \times x^3 + a2 \times x^2 + a1 \times x + a0$

Table 5-451. Equation Method to Calculate Code or Temperature

Function	Unit	Coefficient				
		a4	a3	a2	a1	a0
Code = f(Temperature)	Decimal value of code	4.9847E-08	1.6972E-05	6.8759E-03	3.6509E+00	1.6407E+02
Temperature = f(Code)	°C	-9.2627E-12	6.0373E-08	-1.7058E-04	3.2512E-01	-4.9002E+01

5.2.2.1.5.2.2 VTM Temperature Driven Alerts and Interrupts

Each temperature-monitor register group of VTM can be configured to sample the temperature of its corresponding temperature monitor and trigger up to 3 alert (level) signals:

- GT_TH1_ALERT (overtemperature alert comparator result) - generated by the 10-bit temperature threshold-point1 (THPT1). Set in VTM_TMPSENSx_TH[25-16] TH1_VAL.
- GT_TH2_ALERT (overtemperature alert comparator result) - 10-bit incremental poing generated by threshold-point2 (THPT2). Set in VTM_TMPSENSx_TH2[9-0] TH2_VAL.
- LT_TH0_ALERT (undertemperature alert comparator result) - 10-bit incremental poing generated by threshold-point0 (THPT0). Set in VTM_TMPSENSx_TH[9-0] TH0_VAL.

Note

The following inequality shall always be valid: THPT2 > THPT1 > THPT0.

Note

The device also supports absolute maximum alert (when the die temperature exceeds the programmed temperature in WKUP_VTM_MISC_CTRL2[9-0] MAXT_OUTRG_ALERT_THR) - THERM_MAXTEMP_OUTRANGE_ALERT. For more information about how to handle it, see Section 5.2.2.1.5.2.7.1 , *VTM Maximum Temperature Outrange Alert*.

The level interrupts can be used as follows:

- GT_TH1_INT: An early alert for firmware/software to start doing high-temperature thermal management.
- GT_TH2_INT: A late interrupt whose level high can be used to trigger a hardware-voltage domain reset.
- LT_TH0_INT: A follow-up interrupt to GT_TH1_INT which will report to the firmware/software that the temperature has drop to a safe level to eliminate the thermal-management actions triggered in GT_TH1_INT.

LT_TH0_INT, if enabled, will get triggered always when the temperature being read is less than THPT0, regardless of whether GT_TH1_INT and GT_TH2_INT are enabled, or have ever been triggered. And therefore if LT_TH0_INT has to be generated, then firmware/software is responsible to enable the LT_TH0_INT only as part of the interrupt service routine of GT_TH1_INT and GT_TH2_INT. Otherwise it will keep triggering when is not needed.

Each voltage-domain register group can be set to enable and generate the 3 interrupts related to that particular voltage domain. For enabling and disabling the three types of interrupts see the corresponding group of registers:

- for GT_TH1_INT - WKUP_VTM_GT_TH1_INT_RAW_STAT_SET, WKUP_VTM_GT_TH1_INT_EN_STAT_CLR, WKUP_VTM_GT_TH1_INT_EN_SET, WKUP_VTM_GT_TH1_INT_EN_CLR
- for GT_TH2_INT - WKUP_VTM_GT_TH2_INT_RAW_STAT_SET, WKUP_VTM_GT_TH2_INT_EN_STAT_CLR, WKUP_VTM_GT_TH2_INT_EN_SET, WKUP_VTM_GT_TH2_INT_EN_CLR
- for LT_TH0_INT - WKUP_VTM_LT_TH0_INT_RAW_STAT_SET, WKUP_VTM_LT_TH0_INT_EN_STAT_CLR, WKUP_VTM_LT_TH0_INT_EN_SET, WKUP_VTM_LT_TH0_INT_EN_CLR.

All 3 alerts from the 5 temperature monitors are available as inputs of the mask and alert merging logic block of each voltage domain, such that the temperature monitors that are relevant to each voltage domain can be selected as the contributors to the generation of the 3 combined interrupts in each voltage domain (5 shown in sketch; 3). This logic is presented in Figure 5-149. The THERM_MAXTEMP_OUTRANGE_ALERT is not shown in this figure. Notice that the same temperature sensor can contribute to more than one voltage domain and each voltage domain can have multiple sensors contributing to the interrupt generation in that VD, see VTM_CFG1_VD_EVT_SET_j and VTM_CFG1_VD_EVT_CLR_j registers.

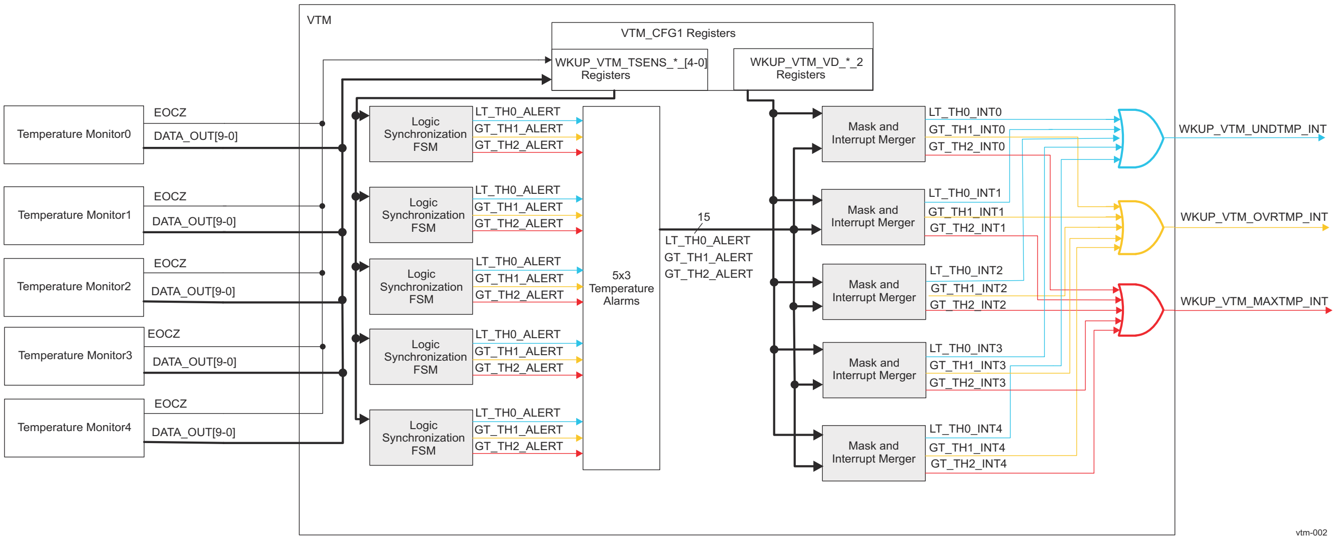

Figure 5-149. VTM Alert and Interrupt Generation

The interrupts need to be active even when the functional clock is off. In this mode they will be driven by the sensor clock.

Note

The interrupts are only active when the sensor is in continuous mode. A one-shot sampling of the sensor will not trigger any interrupts.

Table 5-314 presents the connection of VTM TEMPSENSOR registers groups to voltage domains.

Table 5-452. VTM TEMPSENSOR Register Groups Mapping to Voltage Domains

Register Group	Voltage Domain
WKUP_VTM_TMPSENS_*_0	Sensor in VD_WKUP.
WKUP_VTM_TMPSENS_*_1	Sensor in VD_CORE near near MPU region.
WKUP_VTM_TMPSENS2_*_2	Sensor in VD_CC near C7x region.
WKUP_VTM_TMPSENS_*_3	Sensor in VD_CORE near GPU region.
WKUP_VTM_TMPSENS_*_4	Sensor in VD_CORE near CPSW0 and R5FSS region.
WKUP_VTM_TMPSENS_*[7-6]	Not-used.

There are only 3 interrupts that come out of the VTM module: THERM_LVL_LT_TH0_INTR, THERM_LVL_GT_TH1_INTR, THERM_LVL_GT_TH2_INTR. The interrupt contributions of the 5 voltage domain groups are ORed together to only produce the 3 interrupts that go out. Once an interrupt is detected via DMSC/Compute_cluster, the firmware/software will check which of the 5 voltage domains is the source of the interrupt.

Note

Software shall read the corresponding flags in each of the connected voltage domains to identify which voltage domain is active.

5.2.2.1.5.2.3 VTM VID Voltage Domains

Table 5-315 presents the connection of VTM VD registers groups to voltage domains.

Table 5-453. VTM VD Register Groups Mapping to Voltage Domains

Register Group	Voltage Domain
WKUP_VTM_*_VD_*[1-0]	Not-used.
WKUP_VTM_*_VD_*_2	Maps to VD_CC
WKUP_VTM_*_VD_*_[7-3]	Not-used.

Table 5-316 shows the relation between the VID bit-field values and voltage.

Table 5-454. VID Bit-field Values and Their Corresponding Voltage

VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V	VID Bitfield Value, HEX	Voltage, V
0x0-0x1D	Invalid Values	0x3B	0.745	0x59	0.895	0x77	1.045
0x1E	0.6	0x3C	0.75	0x5A	0.9	0x78	1.05
0x1F	0.605	0x3D	0.755	0x5B	0.905	0x79	1.055
0x20	0.61	0x3E	0.76	0x5C	0.91	0x7A	1.06
0x21	0.615	0x3F	0.765	0x5D	0.915	0x7B	1.065
0x22	0.62	0x40	0.77	0x5E	0.92	0x7C	1.07
0x23	0.625	0x41	0.775	0x5F	0.925	0x7D	1.075
0x24	0.63	0x42	0.78	0x60	0.93	0x7E	1.08
0x25	0.635	0x43	0.785	0x61	0.935	0x7F	1.085
0x26	0.64	0x44	0.79	0x62	0.94	0x80	1.09
0x27	0.645	0x45	0.795	0x63	0.945	0x81	1.095
0x28	0.65	0x46	0.8	0x64	0.95	0x82	1.1
0x29	0.655	0x47	0.805	0x65	0.955	0x83	1.11
0x2A	0.66	0x48	0.81	0x66	0.96	0x84	1.12
0x2B	0.665	0x49	0.815	0x67	0.965	0x85	1.13
0x2C	0.67	0x4A	0.82	0x68	0.97	0x86	1.14
0x2D	0.675	0x4B	0.825	0x69	0.975	0x87	1.15
0x2E	0.68	0x4C	0.83	0x6A	0.98	0x88	1.16
0x2F	0.685	0x4D	0.835	0x6B	0.985	0x89	1.17
0x30	0.69	0x4E	0.84	0x6C	0.99	0x8A	1.18
0x31	0.695	0x4F	0.845	0x6D	0.995	0x8B	1.19
0x32	0.7	0x50	0.85	0x6E	1	0x8C	1.2
0x33	0.705	0x51	0.855	0x6F	1.005	0x8D	1.21
0x34	0.71	0x52	0.86	0x70	1.01	0x8E	1.22
0x35	0.715	0x53	0.865	0x71	1.015	0x8F	1.23
0x36	0.72	0x54	0.87	0x72	1.02	0x90	1.24
0x37	0.725	0x55	0.875	0x73	1.025	0x91	1.25
0x38	0.73	0x56	0.88	0x74	1.03	0x92-0xFF	Invalid Values
0x39	0.735	0x57	0.885	0x75	1.035		
0x3A	0.74	0x58	0.89	0x76	1.04		

5.2.2.1.5.2.4 VTM Clocking

The VTM has 2 reference clock inputs, WKUP_VTM0_FIX_REF_CLK and WKUP_VTM0_FIX_REF2_CLK. The WKUP_VTM0_FIX_REF_CLK is the high precision clock that is used for the sensors. The WKUP_VTM0_FIX_REF2_CLK is a lower precision clock that can be used during low power scenarios to keep the sensors running when the WKUP_VTM0_FIX_REF_CLK is shut off. WKUP_VTM_CLK_CTRL[31]

TSENS_CLK_SEL and WKUP_VTM_CLK_CTRL[4-0] TSENS_CLK_DIV are used to switch between the clocks and to choose the divider value. All the sensors in all VDs controlled by this VTM will run off of the same reference clock.

Note

Software must disable all sensors before switching the reference clock.

For more information about propagation sequence of the sensor changes, see Section 5.2.2.1.5.2.7.3 , *Sensors Programming Sequences*.

5.2.2.1.5.2.5 VTM Retention Interface

VTM has a general purpose retention interface, consistent of 16 sets of 3 signals that can operate totally independently in order to provide retention for 16 signals in the SoC:

- LPMODE_SLEEP_RETIN[15:0]
- LPMODE_SLEEP_RETEN[15:0]
- LPMODE_SLEEP_RETOUT[15:0]

The input LPMODE_SLEEP_RETIN[n] is sampled and synchronized continuously while LPMODE_SLEEP_RETEN[n] = 0. The synchronized output is send out via LPMODE_SLEEP_RETOUT[n]. Once LPMODE_SLEEP_RETEN[n] = 1, then the synchronizer will latch the value and continue providing that latched value via LPMODE_SLEEP_RETOUT[n].

5.2.2.1.5.2.6 VTM ECC Aggregator

Note

For more information about ECC Aggregator functionality, see *ECC Aggregator*.

5.2.2.1.5.2.7 VTM Programming Model

5.2.2.1.5.2.7.1 VTM Maximum Temperature Outrange Alert

THERM_MAXTEMP_OUTRANGE_ALERT is used at the device level in order to generate device warm reset. The alert is asserted when the device overheats and exceeds the maximum temperature limit specified for the device, namely 125°C.

The following is the sequence to assert the THERM_MAXTEMP_OUTRANGE_ALERT:

1. For the output to go active (‘1’), the VTM has to be configured to operate with at least one of its temperature sensors enabled, and VTM_CFG1_TMPSENS_CTRL_j[11] MAXT_OUTRG_EN = 1 for the corresponding enabled sensor.
2. In addition, VTM_CFG2_MISC_CTRL[0] ANYMAXT_OUTRG_ALERT_EN has to be set to ‘1’.
3. With the previous configuration set and at least one of the temperature sensors properly configured, and enabled, if the temperature of the die ever exceeds the programmed value in VTM_CFG2_MISC_CTRL2, the VTM output will be driven ‘1’ once the sensor detects the programmed maximum temperature.
4. At the device level the VTM output, THERM_MAXTEMP_OUTRANGE_ALERT, will drive the PLL controllers into warm reset state with the PLL controllers entering CHIP_0_RST condition, at the same time that all the PLLs go into clock bypass mode.
5. By the actions described in No.4, the device will considerably reduce its power consumption, which over the passing of a few seconds will cause the device to reduce its temperature.
6. The VTM sensor continues to read the temperature and once the code corresponding to the programmed value in VTM_CFG2_MISC_CTRL2[25-16] MAXT_OUTRG_ALERT_THR0 is detected the VTM drives THERM_MAXTEMP_OUTRANGE_ALERT = 0.
7. After No.6 is fulfilled, the PLL controllers no longer have the THERM_MAXTEMP_OUTRANGE_ALERT driving the CHIP_0_RST request and thus the PLL controllers bring the SoC out of reset and the boot

sequence re-starts. At the same time the PLLs get out of bypass mode and start with their target programmed frequencies for the boot process.

Note

THERM_MAXTEMP_OUTRANGE_ALERT output of VTM is mapped to VTM_CFG2_MISC_CTRL[0] ANY_MAXT_OUTRG_ALERT_EN.

Notice that exceeding of the programmed value in VTM_CFG2_MISC_CTRL2[9-0] MAXT_OUTRG_ALERT_THR boundary doesn't result in a PORz (cold reset) event, but instead a CHIP_0_RST event. Otherwise if cold reset is applied to the MCU/WKUP domains of the device, the VTM will be fully reset and the output THERM_MAXTEMP_OUTRANGE_ALERT will be cleared to '0' immediately.

5.2.2.1.5.2.7.2 Temperature Monitor during Low Power Modes

For more information about device Low Power Modes (LPM), see *Device Power States*.

The following sequence has to be follow in LPM:

1. During MCU_ONLY LPM VD_CORE is OFF and VD_MCU and VD_WKUP are ON, so:
    - WKUP_VTM_TMPSENS_CTRL_1[1] TMPSOFF needs to be programmed for the sensor to be disabled and WKUP_VTM_TMPSENS_CTRL_1, and VTM_TMPSENS_TRIM_1 registers settings for this sensor to go to its reset state.
2. If the exit from low power modes in the device results in the VD_CORE also being ON, then at that point the remaining TMPSENS modules can be enabled (WKUP_VTM_TMPSENS_CTRL_1, WKUP_VTM_TMPSENS_TRIM_1 registers).

5.2.2.1.5.2.7.3 Sensors Programming Sequences

Sensors Control Modifications Sequence:

1. Write changes to registers.
2. Wait for 900ns to 1us (long enough for sensor period of slowest 1.15 MHz sensor clock plus some extra).
3. New changes can be written to registers.

Sensors TRIM Pins Modifications Sequence:

1. Clear WKUP_VTM_TMPSENS_CTRL_j[6] CLRZ to disable the sensor, so that it has the ENA input low.
2. Wait for 900ns to 1us for the sensor clock to toggle and register the updated ENA pin .
3. Update the WKUP_VTM_TMPSENS_TRIM_j registers.
4. Wait for 900ns to 1us for the sensor clock to toggle and register to updated TRIM pins while ENA is low.
5. Now the sensor can be enabled normally.

Reset Sensors Sequence:

1. Set the WKUP_VTM_TMPSENS_CTRL_j[6] CLRZ bit to enable the sensor (so that it has the ENA input high).
2. Wait for 900ns to 1us for the sensor clock to toggle and register the updated ENA pin.
3. Clear WKUP_VTM_TMPSENS_CTRL_j[6] CLRZ to disable and reset the sensor (as it requires an ENA transition from 1 to 0 to reset initially) .
4. Wait for 900ns to 1us for the sensor clock to toggle and register the updated ENA pin.
5. Now the sensor can be configured and enabled normally.

5.2.2.1.5.2.8 AVS-Class0

Adaptive Voltage Scaling (AVS) Class 0 is a procedure for lowering the voltage on certain device power rails. AVS Class 0 attempts to normalize the power consumption across all devices. The optimal voltage for each AVS supported rail of each device is determined after analysis in the factory, based on the strength of the device during manufacturing. This value is written in the device eFuse where it can be read through dedicated registers.

AVS can be enabled by system software after primary boot. Refer to *AVS Support* on how to enable AVS based on these registers.

5.2.2.1.6 Integrated Low-dropout Regulator (LDO)

5.2.2.1.6.1 SDIO LDO Overview

A single SDIO_LDO module is integrated in the device MAIN domain - SDIO_LDO0.

Figure 5-150 shows module top-level overview.

Control of SDIO_LDO to enable 1.8 V signaling is based upon the V1P8_SIGNAL_ENA input value. SDIO_LDO generates a 1.8v or 3.3v output depending on V1P8_SIGNAL_ENA. When V1P8_SIGNAL_ENA = 0, CAP_VDDS_MMC1 = 3.3V (Switch Mode) and when V1P8_SIGNAL_ENA = 1, CAP_VDDS_MMC1 = 1.8V (LDO Mode). See MMCSD1_HOST_CONTROL2 Register.

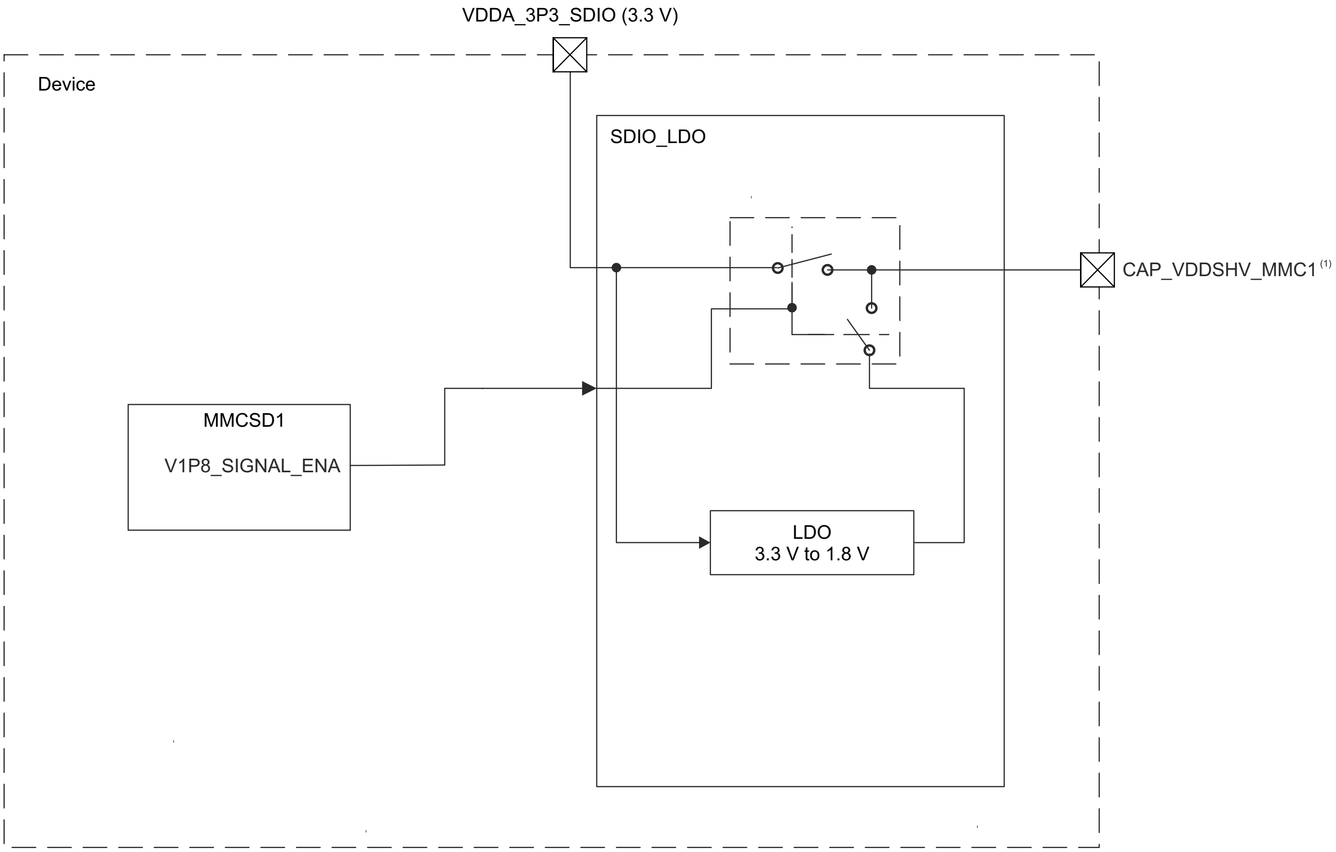

Note

(1) De-coupling capacitors are not shown. Refer to the specific-device Data Sheet for more information about them and the connection among these pads.

Figure 5-150. SDIO_LDO Top-Level Overview

5.2.2.2 Power Control Modules

The Power Control Modules are divided into two section, dependent on their functionality - Power Sleep Controller and Local Power Sleep section and Integrated Power Management (DMSC) section.

5.2.2.2.1 Power Sleep Controller and Local Power Sleep Controllers

The Power Sleep Controller (PSC) includes a Global Power Sleep Controller (GPSC) and a number of Local Power Sleep Controllers (LPSC) that control overall device power by turning off unused power domains and gating off clocks to individual peripherals and modules. The PSC provides the user with an interface to control important power and clock operations.

The device has two PSCs – one in the MCU domain (MCU_PSC), and one in the MAIN domain (MAIN_PSC).

5.2.2.2.1.1 PSC Terminology

Table 5-455. PSC Terminology

Term	Definition
LPSC	Local Power Sleep Controller; one per module (domain)
GPSC	Global Power/Sleep Controller; manages the LPSCs
PSC	Power Sleep Controller, including one GPSC and multiple LPSCs

5.2.2.2.1.2 PSC Features

Each PSC includes the following features:

- Provides a software interface to:
  - Control module power on or off
  - Control module clock on or off
- Supports emulation features: power, clock, and reset

Note

PSC functions are controlled through the DMSC. For more information how to use DMSC, see the TISCI API.

5.2.2.2.1.3 PSC: Device Power-Management Layout

The device is divided into a number of separate voltage domains, each containing specific processing cores and peripherals. This division enables the device to achieve lower power dissipation profiles by allowing the power supplies to unused domains to be completely turned off.

Each PSC in the device has several power domains that can be turned on for operation, or off to minimize power dissipation. The Global Power Sleep Controller (GPSC) is used to control the power gating of various power domains. Clock gating to each logic block is managed by the Local Power Sleep Controllers (LPSCs).

For modules with a dedicated clock or multiple clocks, the LPSC communicates with the PLL controller to enable and disable that module's clock at the source. For modules that share a clock with other modules, the LPSC controls the clock gating logic for each module.

5.2.2.2.1.3.1 Device Power-Management Layout

Section 5.2.2.2.1.3.2 provides the device-level view of the MAIN PSC with module associations to the clock, power, reset isolation, and voltage domains.

Section 5.2.2.2.1.3.3 provides the device-level view of the MCU PSC with module associations to the clock, power, reset isolation, and voltage domains.

Note

For information about LPSC Dependences, see Section 5.2.2.2.1.5 , *LPSC Dependences Overview*.

5.2.2.2.1.3.2 PSC0 LPSC Features

Table 5-456. PSC0 LPSC Features

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	CMP_EVENT_INTROUTER0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	CTRL_MMR0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAIN_GPIOMUX_INTROUTER0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PLL0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAIN_SEC_MMR0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMESYNC_EVENT_INTROUTER0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PADCFG_CTRL0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	CPT2_AGGR0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC4
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DCC5
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_BCDMA_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_CBASS_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_ECC_AGGR_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_INTAGGR_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_IPCSS_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_PKTDMA_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_PSILCFG_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_PSILSS_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_RINGACC_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DMASS0_SEC_PROXY_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER10
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER11
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER4
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER5
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER6
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER7
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER8
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMER9
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	ECAP0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	ECAP1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	ECAP2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EQEP0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EQEP1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EQEP2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	ESM0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSIRX0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSIRX1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSIRX2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSIRX3

Table 5-456. PSC0 LPSC Features (continued)

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSIRX4
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSIRX5
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSITX0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSITX1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSS0_FSAS_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	FSS0_OSPI_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	GICSS0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	GPIO0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	GPIO1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	GTC0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EFUSE0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	CPTS0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	DDPA0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM4
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM5
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM6
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM7
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	EPWM8
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	VTM0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAILBOX0_MAILBOX_CLUSTER_0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAILBOX0_MAILBOX_CLUSTER_1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAILBOX0_MAILBOX_CLUSTER_2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAILBOX0_MAILBOX_CLUSTER_3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAILBOX0_MAILBOX_CLUSTER_4
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAILBOX0_MAILBOX_CLUSTER_5
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAILBOX0_MAILBOX_CLUSTER_6
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MAILBOX0_MAILBOX_CLUSTER_7
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	I2C0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	I2C1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	I2C2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	I2C3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MSRAM_256K0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MSRAM_256K1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MSRAM_256K2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MSRAM_256K3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MSRAM_256K4
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MSRAM_256K5
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MSRAM_256K6
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MSRAM_256K7
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PDMA0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PDMA1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	PSRAMECC0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	ROM0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MCSPI0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MCSPI1

Table 5-456. PSC0 LPSC Features (continued)

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MCSPI2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MCSPI3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	MCSPI4
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	SPINLOCK0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	TIMERMGR0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	UART0
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	UART1
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	UART2
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	UART3
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	UART4
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	UART5
PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	0	ON	NO	UART6
PSC0	GP_CORE_CTL	LPSC_MAIN_TEST	1	ON	YES	DFTSS0
PSC0	GP_CORE_CTL	LPSC_MAIN_PBIST	2	ON	YES	PBIST0
PSC0	GP_CORE_CTL	LPSC_MAIN_PBIST	2	ON	YES	PBIST1
PSC0	GP_CORE_CTL	LPSC_MMC4B_0	4	OFF	YES	MMCSD1
PSC0	GP_CORE_CTL	LPSC_MMC8B_0	5	OFF	YES	MMCSD0
PSC0	GP_CORE_CTL	LPSC_USB	6	OFF	YES	USB0
PSC0	GP_CORE_CTL	LPSC_ADC	7	OFF	YES	ADC0
PSC0	GP_CORE_CTL	LPSC_DEBUGSS	8	ON	YES	DBGSUSPENDROUTER0
PSC0	GP_CORE_CTL	LPSC_DEBUGSS	8	ON	YES	STM0
PSC0	GP_CORE_CTL	LPSC_DEBUGSS	8	ON	YES	DEBUGSS_WRAP0
PSC0	GP_CORE_CTL	LPSC_DEBUGSS	8	ON	YES	DEBUGSS0
PSC0	GP_CORE_CTL	LPSC_GPMC	9	OFF	YES	ELM0
PSC0	GP_CORE_CTL	LPSC_GPMC	9	OFF	YES	GPMC0
PSC0	GP_CORE_CTL	LPSC_EMIF_CFG_0	10	OFF	YES	DDR16SS0
PSC0	GP_CORE_CTL	LPSC_MCAN_0	12	OFF	YES	MCAN0
PSC0	GP_CORE_CTL	LPSC_MCAN_1	13	OFF	YES	MCAN1
PSC0	GP_CORE_CTL	LPSC_SAUL	14	ON	YES	SA2_UL0
PSC0	GP_CORE_CTL	LPSC_SERDES_0	15	OFF	YES	SERDES_10G0
PSC0	GP_CORE_CTL	LPSC_PCIE_0	16	OFF	YES	PCIE0
PSC0	PD_A53_CLUSTER_0	LPSC_A53_CLUSTER_0	20	OFF	YES	A53SS0
PSC0	PD_A53_CLUSTER_0	LPSC_A53_CLUSTER_0_PBIST	21	OFF	YES	COMPUTE_CLUSTER0_PBIST_0
PSC0	PD_A53_0	LPSC_A53_0	22	OFF	YES	RTI0
PSC0	PD_A53_0	LPSC_A53_0	22	OFF	YES	A53SS0_CORE_0
PSC0	PD_A53_1	LPSC_A53_1	23	OFF	YES	RTI1
PSC0	PD_A53_1	LPSC_A53_1	23	OFF	YES	A53SS0_CORE_1
PSC0	PD_PULSAR_0	LPSC_PULSAR_0_R5_0	24	OFF	YES	R5FSS0_CORE0
PSC0	PD_PULSAR_0	LPSC_PULSAR_0_R5_0	24	OFF	YES	RTI8
PSC0	PD_PULSAR_0	LPSC_PULSAR_0_R5_1	25	OFF	YES	R5FSS0_CORE1
PSC0	PD_PULSAR_0	LPSC_PULSAR_0_R5_1	25	OFF	YES	RTI9
PSC0	PD_PULSAR_0	LPSC_PULSAR_PBIST_0	26	OFF	YES	PBIST2
PSC0	PD_PULSAR_1	LPSC_PULSAR_1_R5_0	27	OFF	YES	R5FSS1_CORE0
PSC0	PD_PULSAR_1	LPSC_PULSAR_1_R5_0	27	OFF	YES	RTI10
PSC0	PD_PULSAR_1	LPSC_PULSAR_1_R5_1	28	OFF	YES	R5FSS1_CORE1
PSC0	PD_PULSAR_1	LPSC_PULSAR_1_R5_1	28	OFF	YES	RTI11
PSC0	PD_PULSAR_1	LPSC_PULSAR_PBIST_1	29	OFF	YES	PBIST3
PSC0	PD_ICSSG_0	LPSC_ICSSG_0	30	OFF	YES	PRU_ICSSG0
PSC0	PD_ICSSG_1	LPSC_ICSSG_1	31	OFF	YES	PRU_ICSSG1

Table 5-456. PSC0 LPSC Features (continued)

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
PSC0	PD_CPSW	LPSC_CPSW3G	33	OFF	YES	CPSW0

5.2.2.2.1.3.3 MCU_PSC0 LPSC Features

Table 5-457. MCU_PSC0 LPSC Features

PSC	Power Domain Name	LPSC Name	LPSC Index	Default State	Software Controllable	Modules
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_CTRL_MMR0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_MCU_GPIOMUX_INTROUTER0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_PLL0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_PADCFG_CTRL0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_DCC0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_TIMER0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_TIMER1
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_TIMER2
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_TIMER3
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_ESM0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_GPIO0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_MCRC64_0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_I2C0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_I2C1
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_TIMEOUT0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_MCSPI0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_MCSPI1
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_UART0
MCU_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_UART1
MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	MCU_M4FSS0_CBASS_0
MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	MCU_M4FSS0_CORE0
MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	MCU_M4FSS0_CORTEX_M4F_SS_0
MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	MCU_M4FSS0_DRAM_0
MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	MCU_M4FSS0_ECC_AGGR_0
MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	MCU_M4FSS0_IRAM_0
MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	MCU_M4FSS0_RAT_0
MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	MCU_RTI0

5.2.2.2.1.4 PSC: Executing State Transitions

This section describes how to execute state transitions for power domains and modules. Examples show how to enable only power domains, only module domains, or a combination. Although the user has complete control of the sequencing, see Section 5.2.2.2.1.4.4 , *Recommendations for Power Domain/Module Sequencing* for recommendations.

5.2.2.2.1.4.1 Power Domain State Transitions

This section describes the basic procedure for transitioning the state of a power domain.

Note

The power domain is always in the ON state when the device is powered-on, and therefore it is not possible to transition this domain to the OFF state. Conversely, the other domains are in the OFF or ON state when the device is powered-on. Transitions between ON and OFF states need to follow the procedure below. See the device-specific Datasheet and respective module Technical Reference Manual chapter for any other considerations especially while turning off the power domain.

The procedure for power domain state transitions is shown below (x denotes the power domain number):

1. Wait for PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT to clear to 0. Wait for any previously initiated transitions to finish before initiating a new transition.
2. Set PSC0_PDCTL[0] NEXT or MCU_PSC0_PDCTL[0] NEXT for an ON (1) or OFF (0) transition. NOTE: When PSC0_PTCMD[x] GO or MCU_PSC0_PTCMD[x] GO is set to 1 in the next step, the PDCTL[0] NEXT field of this power domain and the PSC0_MDCTL[4-0] NEXT or MCU_PSC0_MDCTL[4-0] NEXT field of the module in this power domain are evaluated. Therefore, the PSC0_MDCTL[4-0] NEXT or MCU_PSC0_MDCTL[4-0] NEXT field may be set for multiple modules before executing this step.
3. Set PSC0_PTCMD[x] GO or MCU_PSC0_PTCMD[x] GO to 1 to initiate the state transition(s). The PSC turns on or off the logic/memory for that particular domain.
4. Wait for PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT to self-clear to 0. The domain is safely in the new state only after PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT is cleared to 0.

5.2.2.2.1.4.2 Module State Transitions

This section describes the procedure for transitioning the module state.

Note

The following procedure is applicable for all LPSC-controlled modules. To transition the module state, one must be aware of several system considerations. Transitions between Enable and Disable states need to follow the procedure below. See the device-specific Datasheet and peripheral chapter for any other considerations especially while transitioning a module to Disable state. Also, before transitioning a module to Enable, if the logic/memories are not in the power domain, they must be turned on before or in parallel with the transition. See Section 5.2.2.2.1.4.1 , *Power Domain State Transitions*.

The procedure for module state transitions is shown below (x denotes the power domain number):

1. Wait for PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT to clear to 0x0. Wait for any previously initiated transitions to finish before initiating a new transition.
2. Set PSC0_MDCTL[4-0] NEXT or MCU_PSC0_MDCTL[4-0] NEXT to Enable (0x3) or Disable (0x0). Note that transitions in multiple PSC0_MDCTL[4-0] NEXT or MCU_PSC0_MDCTL[4-0] NEXT fields may be set in this step as long as the corresponding power domain is on.
3. Set PSC0_PTCMD[x] GO or MCU_PSC0_PTCMD[x] GO to 1 to initiate the transition(s).
4. Wait for PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT to self-clear to 0. The module is safely in the new state only after PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT clears to 0.

5.2.2.2.1.4.3 Concurrent Power Domain/Module State Transitions

This section describes the basic procedure for transitioning the state of a power domain and module domain for modules that are not in the AlwaysOn domain. This may be done separately as described in the sections above, if desired.

The procedure for concurrent power domain/module state transitions is shown below (x denotes the power domain number):

1. Wait for PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT to clear to 0. Wait for any previously initiated transitions to finish before initiating a new transition.
2. Set PSC0_PDCTL[0] NEXT or MCU_PSC0_PDCTL[0] NEXT for an ON (1) transition.
3. Set PSC0_MDCTL[4-0] NEXT or MCU_PSC0_MDCTL[4-0] NEXT to Enable (0x3). Note that transitions in multiple PSC0_MDCTL[4-0] NEXT or MCU_PSC0_MDCTL[4-0] NEXT fields may be set in this step as long as the corresponding power domain is on.
4. Set PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT to 1 to initiate the state transition(s). The PSC will turn on the logic/memory for that particular domain, starts the module clock, then de-asserts the module reset.
5. Wait for PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT to self-clear to 0. The module is safely in the new state only after PSC0_PTSTAT[x] GOSTAT or MCU_PSC0_PTSTAT[x] GOSTAT clears to 0.

5.2.2.2.1.4.4 Recommendations for Power Domain/Module Sequencing

As noted in Section 5.2.2.2.1.4 , *Executing State Transitions*, a particular peripheral's power domain must be enabled before the module is enabled.

Unless there is a system-level reason to perform each function separately, the recommendation is to use the sequence listed in rather than individual sequencing. Even though a single write to the appropriate GO bit starts the power domain and module transition, it is still sequenced such that the memory/logic is certain to turn on before the module is enabled. Thus, there is no ill effect in performing these together.

It is important to know that when a power domain is enabled, all logic/memories for that module are immediately turned on and moved to an active state. This means that there will be a spike in current consumption at that particular time. In other words, di/dt will be affected. To minimize the effect on di/dt of enabling power domains, it is recommended to power up modules one at a time. It is also recommended that all modules be initialized early in the application to avoid a large spike in di/dt during normal operation where the application may already be drawing a substantial amount of current from the supply.

5.2.2.2.1.5 LPSC Dependencies Overview

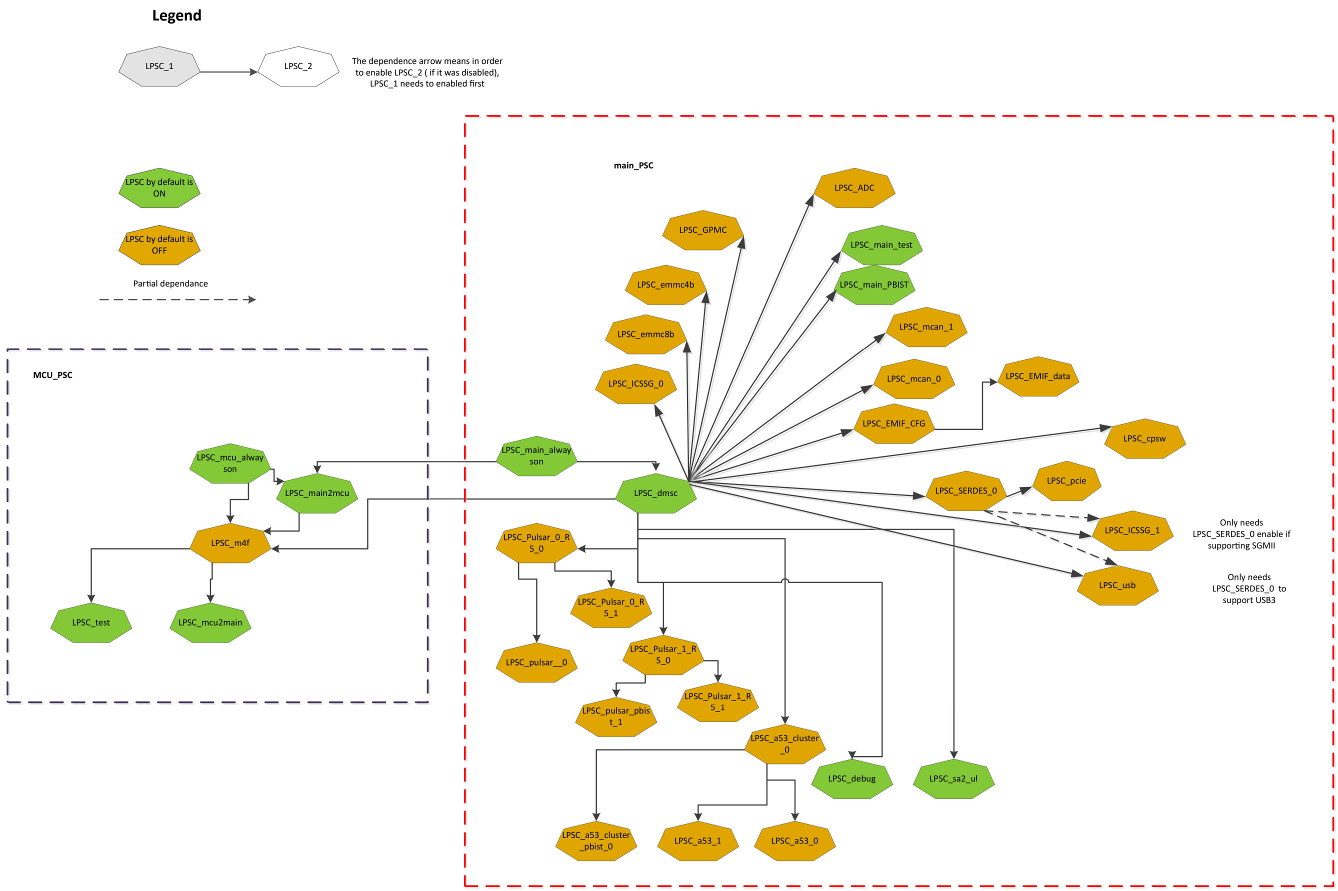

Figure 5-151. LPSC Dependencies

5.2.2.2.2 DMSC-L Power Management Overview

5.2.2.2.2.1 DMSC Power Management Features

DMSC power management supports:

- DMSC control:
  - Contains various control, configuration, and status registers for power management functions
- Main features of oscillators control:
  - Controls the main oscillator power down
  - Controls the gating of the POR RC oscillator root clock of the main oscillator, to avoid high frequency clock propagation during oscillator wake-up
- DMSC memory power management:
  - Power-off of ROM during sleep modes
  - RAM retention during sleep modes
- I/O power management:
  - Controls I/O isolation while going into standby mode
  - Controls I/O wake-up capability
- External signals for power control:
  - Support for 64 Cortex-M3 controlled general purpose outputs
  - Support for 64 general purpose inputs which can be used by Cortex-M3
  - Support for 64 hardware controlled outputs
  - Support for 64 hardware controlled inputs
- Target VBUSP port to directly connect to Power Sleep Controller (PSC)

Note

Power resource management of the device is controlled through the firmware running on the DMSC.

Note

For more information on how to use DMSC, see the TISCI API.

5.2.3 Device Power States

5.2.3.1 Overview of Device Low-Power Modes

The device supports multiple power modes described in the sections below. The lower power consumption comes at the cost of longer time for recovery to a running mode.

Figure 5-152 depicts the valid power modes for the device.

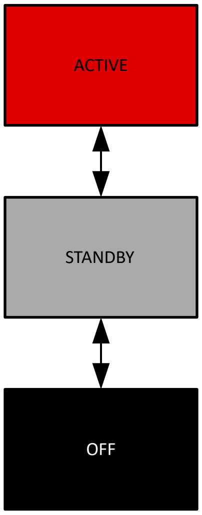

Figure 5-152. Power Modes

Device supports the following power states:

- ACTIVE: Main Status and Control registers are ON, processors and subsystems are ON, based on use cases.
- STANDBY: Main processor cores in WFI/WFE, rest of active subsystems idles.
- OFF: entire device is off by switching off voltage rails externally.

5.2.3.2 Device Power States and Transitions

The LPMs always transition from run state. If the device software decides to transition from one low power mode to another low power mode, it needs to go through the run state first.

Normally, the software initiates transition to low power mode and interrupts/events are the exit trigger.

Figure 5-153 shows the state diagram of transitions between LPMs.

Note

The state diagram represents higher layer logical requesters, as any actual operation are actualized by DMSC firmware.

This device supports three power states: OFF, ACTIVE, and STANDBY. The transitioning schemes are as follows:

- OFF → ACTIVE
- STANDBY → ACTIVE
- ACTIVE → OFF
- ACTIVE → STANDBY

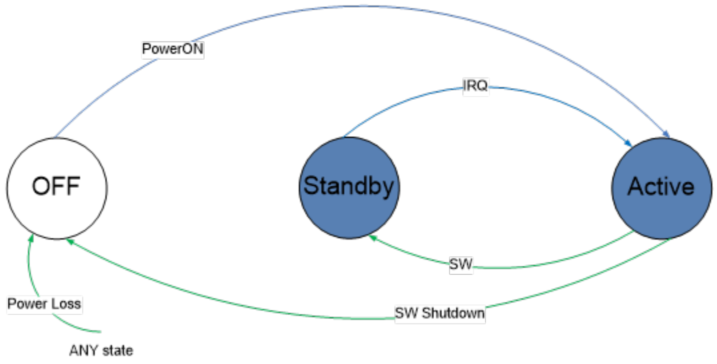

Figure 5-153. Transition between Power Modes

5.2.4 Thermal Management

The modules that perform thermal management are:

- On-die temperature Monitor with Integrated multiple sensors
- One thermal diode
- VTM
- DMSC firmware.

For information about VTM, see *Voltage and Thermal Manager (VTM)*.

For more information how to use DMSC, see the TISCI API.

5.3 Reset

This chapter describes the device reset signals and contains details on reset management.

5.3.1 Overview

Reset Introduction

A reset is designed to bring a device or subsystem into a known state. Resets occur after power up events, as well as software and hardware reset requests. This section introduces the device reset capabilities and functionality.

Device Resets

The Device Power-on-Reset (POR) is controlled by the external pin MCU_PORz. This pin is driven by an external (off-chip) "Power-Good" Circuit or Power Management IC (PMIC). The MCU_PORz pin should be held active LOW (0) during the entire power-up phase. The device should be held in reset until all power supplies are stable with an additional a delay for the High Frequency Oscillator (HFOSC0) clock to stabilize.

The SoC is divided into two separate functional Reset Domains: MCU Reset Domain and MAIN Reset Domain (each containing specific processing cores and peripherals).

- MCU Reset Domain: Managed by the MCU Domain PSC, this includes Arm Cortex-M4F MCU Processor (M4FSS).
- MAIN Reset Domain: Managed by the MAIN Domain PSC, this includes the high performance application Arm Cortex-A53 cores (A53SS), Device Management and Security Controller (DMSC-L), real-time performance Arm Cortex-R5 cores (R5FSS), and Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU_ICSSG) Cores.

The MCU and MAIN domains can be configured to have independent warm reset pins via software: MCU_RESETz and RESET_REQz. By default, these two pins have the same effect and will act as a warm reset source for both MAIN and MCU domains. When the MCU domain is configured for reset isolation, MAIN domain resets will only reset the MAIN domain and the MCU domain will remain unaffected by all MAIN domain resets.

High-Level Reset Flow

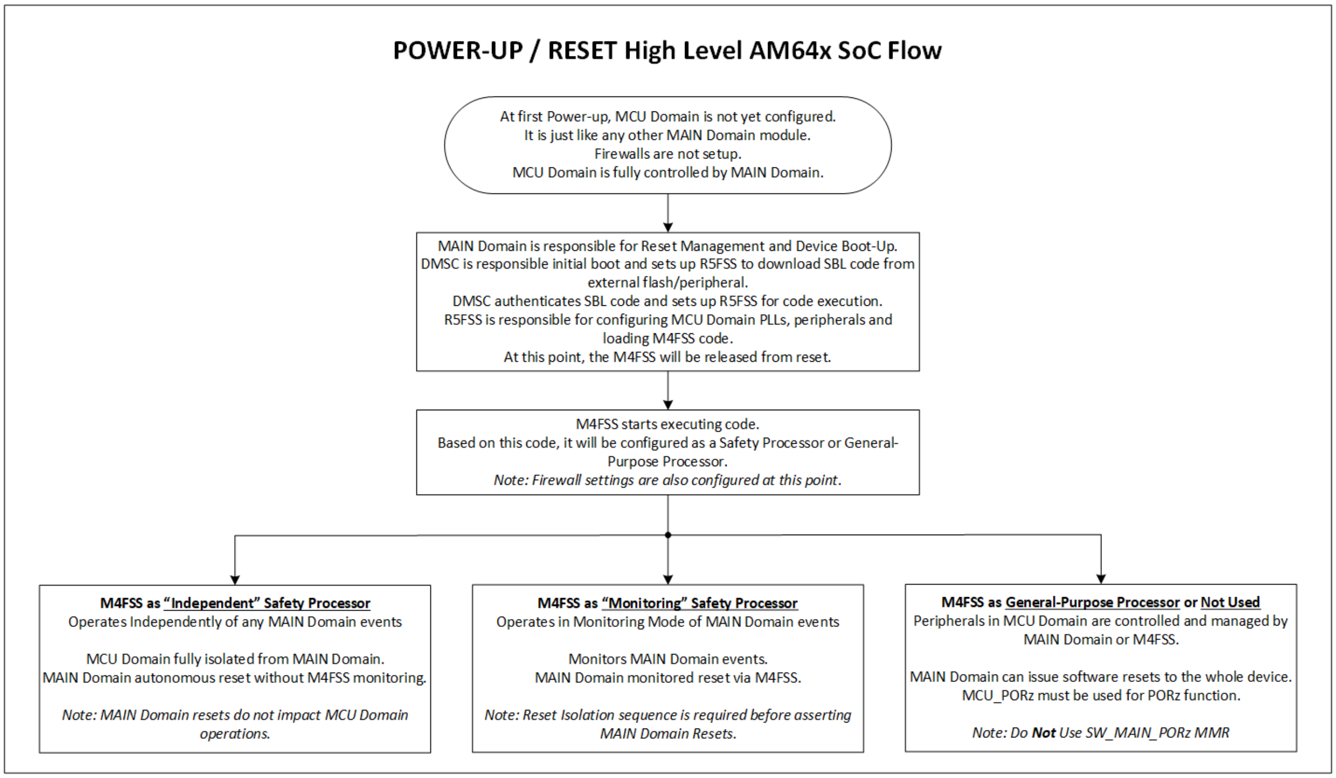

POWER-UP / RESET High Level AM64x SoC Flow

At first Power-up, MCU Domain is not yet configured.
It is just like any other MAIN Domain module.
Firewalls are not setup.
MCU Domain is fully controlled by MAIN Domain.

MAIN Domain is responsible for Reset Management and Device Boot-Up.
DMSC is responsible initial boot and sets up R5FSS to download SBL code from external flash/peripheral.
DMSC authenticates SBL code and sets up R5FSS for code execution.
R5FSS is responsible for configuring MCU Domain PLLs, peripherals and loading M4FSS code.
At this point, the M4FSS will be released from reset.

M4FSS starts executing code.
Based on this code, it will be configured as a Safety Processor or General-Purpose Processor.
Note: Firewall settings are also configured at this point.

M4FSS as “Independent” Safety Processor
Operates Independently of any MAIN Domain events

MCU Domain fully isolated from MAIN Domain.
MAIN Domain autonomous reset without M4FSS monitoring.

Note: MAIN Domain resets do not impact MCU Domain operations.

M4FSS as “Monitoring” Safety Processor
Operates in Monitoring Mode of MAIN Domain events

Monitors MAIN Domain events.
MAIN Domain monitored reset via M4FSS.

Note: Reset Isolation sequence is required before asserting MAIN Domain Resets.

M4FSS as General-Purpose Processor or Not Used
Peripherals in MCU Domain are controlled and managed by MAIN Domain or M4FSS.

MAIN Domain can issue software resets to the whole device.
MCU_PORz must be used for PORz function.

*Note: Do **Not** Use SW_MAIN_PORz MMR*

Figure 5-154. High Level Reset Flow

This flowchart explains the high-level reset use case.

5.3.1.1 MAIN Domain Supported Resets

- Power-On-Resets
  - MAIN domain software POR reset
- Warm Resets
  - RESET_REQz device pin
  - MAIN domain ESM error reset
  - MAIN domain software warm reset
  - DMSC-L warm reset
  - DMSC-L cold reset
- Local Module Resets
  - MAIN domain LPSC module local reset

5.3.1.2 MCU Domain Supported Resets

- Power-On-Resets
  - MCU_PORz device pin
- Warm Resets
  - MCU_RESETz device pin
  - MCU domain software warm reset
  - MCU domain ESM error reset
  - DMSC-L cold reset
- Local Module Resets
  - MCU domain LPSC module local reset

5.3.1.3 Reset Terminology

DMSC-L	Device Management Security Controller
POR	Power-On-Reset
ESM	Error Signaling Module
Reset Isolation	The module or domain is exempt from specific resets
PSC	Power Sleep Controller
LPSC	Local Power Sleep Controller
PD	Power Domain
VD	Voltage Domain
PRG	Power Reset Generator
POK	Power OK
PGD	Power Glitch Detector
PLLCTRL	PLL and Reset Controller
HHV	High Heating Value mode (IO Pin Fail-safe Control (Tri-State Output))
VTM	Voltage and Temperature Monitor
HFOSC	Internal Device High-Frequency Oscillator

5.3.1.4 Reset Architecture

Reset Architecture Block Diagram

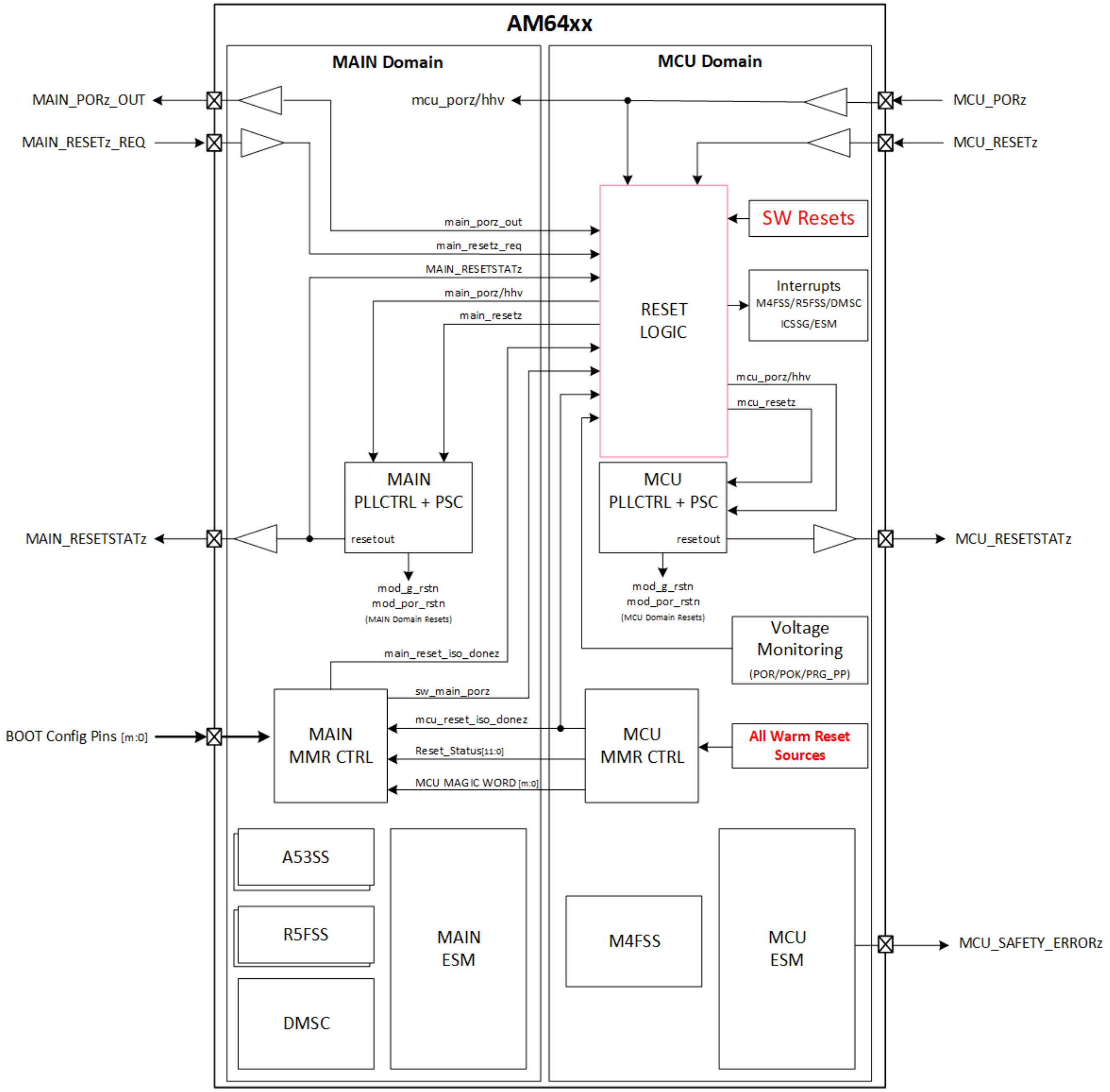

Figure 5-155. Reset Architecture Block Diagram

This is the device reset architecture block diagram. It describes the device reset sub-modules and critical internal signal interconnections.

SoC Reset Hardware Logic Diagram

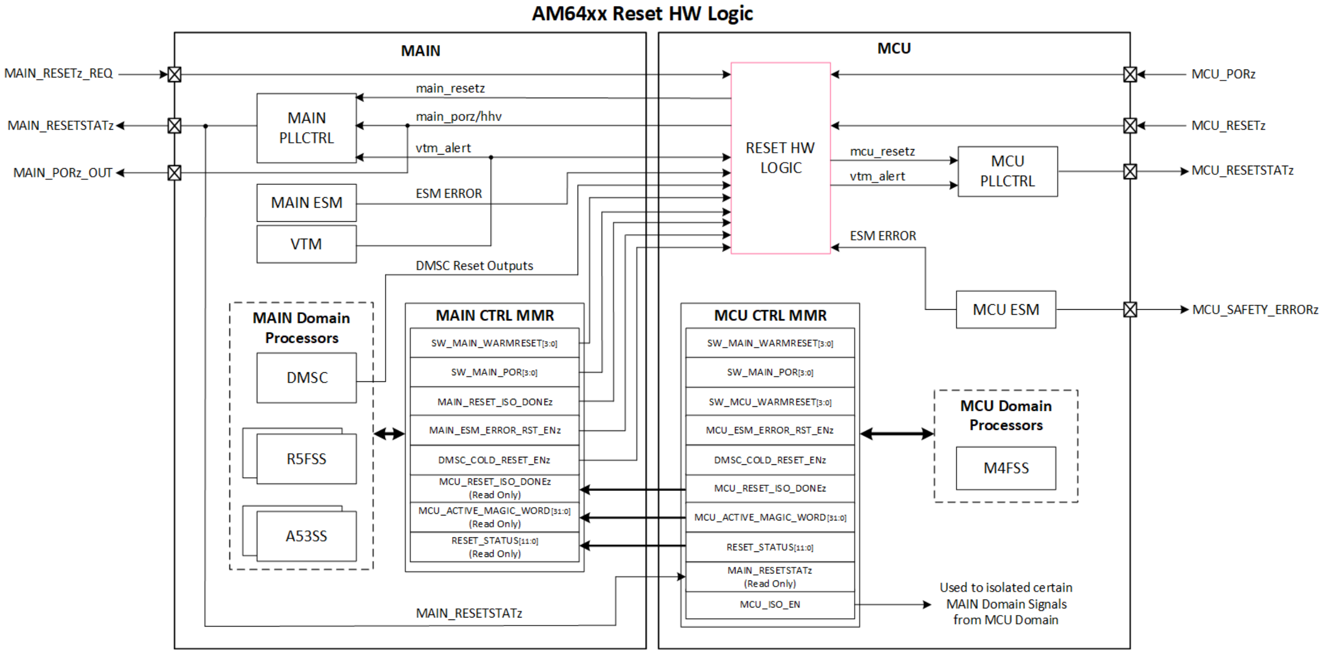

Figure 5-156. SoC Reset Hardware Logic Diagram

This is the reset hardware logic diagram. It describes the MAIN and MCU reset domains and processors connections as well as the available reset sources including reset pins and CTRLMMRs.

MCU Domain Reset Hardware Logic Diagram

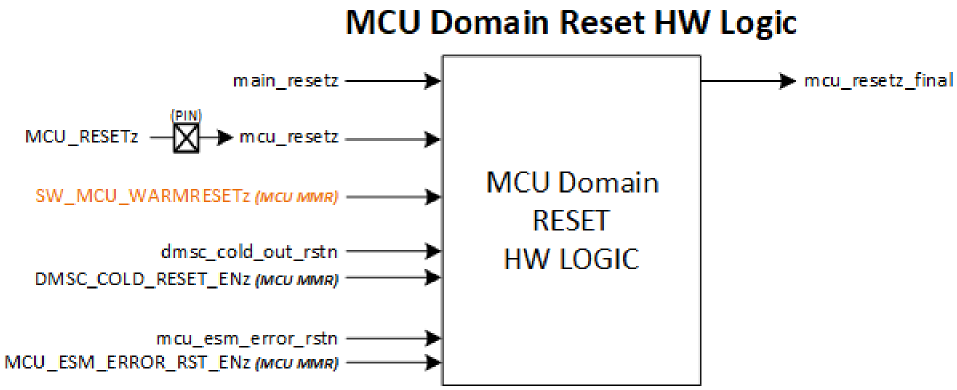

Figure 5-157. MCU Domain Reset Hardware Logic Diagram

This diagram shows the external and internal signals associated with the MCU domain resets.

MAIN Domain Reset Hardware Logic Diagram

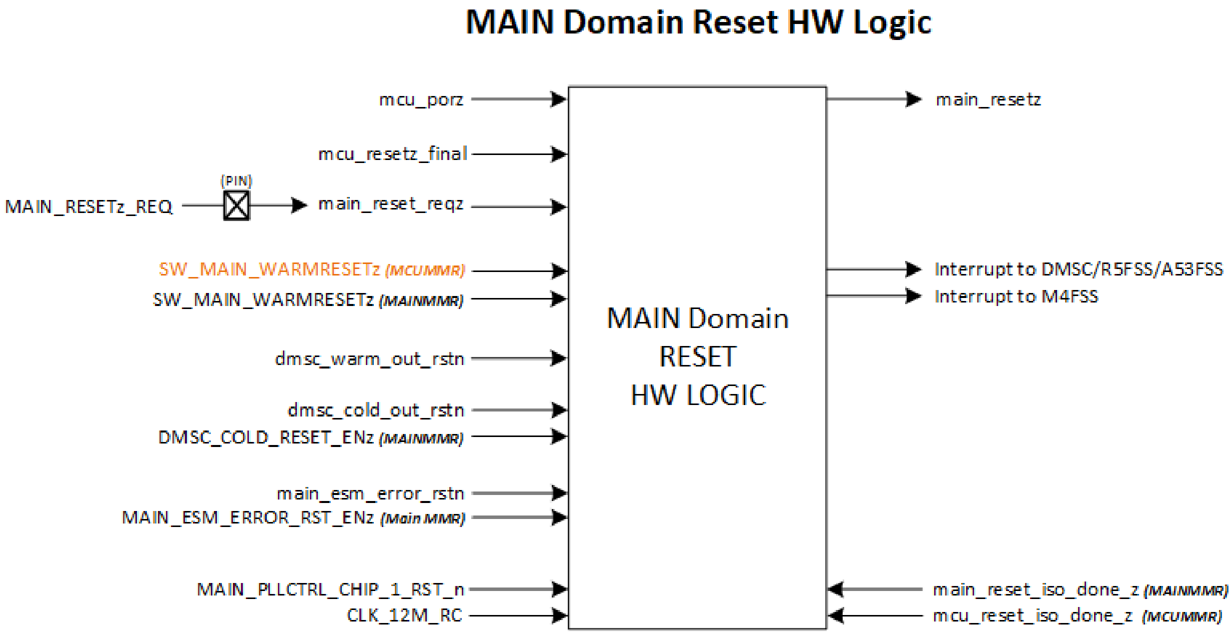

Figure 5-158. MAIN Domain Reset Hardware Logic Diagram

This diagram shows the external and internal signals associated with the MAIN domain resets.

5.3.2 Reset Sources

This table summarizes the available reset sources that are supported by the device.

Table 5-458. Device Reset Sources

Reset Name	Device Domain	Reset Type	Sync/ Async	Pin/ Register/ Internal	Details
MCU_PORz	MCU	Hardware POR	Async	MCU_PORz HW Pin	MCU_PORz Details
SW_MAIN_PORz	MAIN	Software POR	Sync	MAIN_CTRL_MMR_CFG0_RST_CTRL MCU_CTRL_MMR_CFG0_RST_CTRL	SW_MAIN_PORz Details
MCU_RESETz	MCU	Hardware warm reset	Async	MCU_RESETz HW Pin	MCU_RESETz Details
SW_MCU_WARMRSTz	MCU	Software warm reset	Sync	MCU_CTRL_MMR_CFG0_RST_CTRL	SW_MCU_WARMRSTz Details
MAIN_RESET_REQz	MAIN	Hardware warm reset	Sync	RESET_REQz HW Pin	MAIN_RESET_REQz Details
SW_MAIN_WARMRSTz	MAIN/MCU	Software warm reset	Sync	MAIN_CTRL_MMR_CFG0_RST_CTRL MCU_CTRL_MMR_CFG0_RST_CTRL	SW_MAIN_WARMRSTz Details
VTM Thermal Reset	MAIN/MCU	Thermal reset	Async	Internal Signal	VTM Thermal Alert Reset Details
ESM_ERRORz	MAIN/MCU	ESM error reset	Async	MAIN_CTRL_MMR_CFG0_RST_CTRL MCU_CTRL_MMR_CFG0_RST_CTRL	ESM_ERRORz Reset Details
DMSC_COLD_OUT_RST_n	MCU	DMSC-L cold reset	Async	Internal Signal	DMSC-L Reset Details
DMSC_WARM_OUT_RST_n	MAIN	DMSC-L warm reset	Async	Internal Signal	DMSC-L Reset Details

5.3.3 Reset Status

This section explains the Reset Status functionality. An output pin or software bit is used to represent the status of a specific individual reset.

Table 5-459. AM64x Reset Status

Reset Status Name	Reset Status Source	Reset Status Info	Signal Active Level	Reset Signal Details
MCU CTRLMMR Status Register	Register	4 bits in CTRLMMR on MCU warm reset status and assertion.	Status bits read active HIGH (1) when a particular reset is asserted.	MCU_CTRL_MMR_CFG0_RST_CTRL
MAIN CTRLMMR Status Register	Register	4 bits in CTRLMMR on MAIN warm reset status and assertion.	Status bits read active HIGH (1) when a particular reset is asserted.	MAIN_CTRL_MMR_CFG0_RST_CTRL
PORz_OUTz	Output Pin	On/Off pin status of MAIN PORz reset	Active LOW (0)	PORz_OUT Status Pin
RESETSTATz	Output Pin	On/Off pin status of MAIN warm reset	Active LOW (0)	RESETSTATz Status Pin
MCU_RESETSTATz	Output Pin	On/Off pin status of MCU PORz reset	Active LOW (0)	MCU_RESETSTATz Status Pin
MCU_SAFETY_ERRORn	Output Pin	On/Off pin status of MCU ESM_ERROR reset	Active LOW (0)	MCU_SAFETY_ERRORn Status Pin

5.3.3.1 Reset Source Status Registers

All warm reset sources which trigger a device/domain warm reset are captured in the MCU domain CTRLMMR reset status register MCU_CTRL_MMR_CFG0_RST_SRC. This register is only reset on MCU_PORz.

The MCU domain CTRLMMR MCU_CTRL_MMR_CFG0_RST_SRC register is shadowed in MAIN domain CTRLMMR MAIN_CTRL_MMR_CFG0_RST_SRC so that MAIN domain processors can read it without directly accessing the MCU domain CTRLMMR.

After recovery from warm reset, software can read the CTRLMMR reset source register MAIN_CTRL_MMR_CFG0_RST_SRC to identify the source of previous reset. After reading this reset source register, software must clear the register.

Reset status bits read active HIGH (1) when a particular reset is triggered.

The following reset sources, which cause MCU and MAIN domain resets, are captured in the MCU domain CTRLMMR reset source register:

- MCU_RESETz (Reset by Hardware Pin)
- SW_MCU_WARMRSTz (Reset by MCU domain CTRLMMR*)
- SW_MAIN_PORz_MCUMMR (Reset by MCU domain CTRLMMR*)
- SW_MAIN_PORz_MAINMMR (Reset by MAIN domain CTRLMMR*)
- MAIN_RESET_REQz (Reset by Hardware Pin)
- SW_MAIN_WARMRSTz_MCUMMR (Reset by MCU domain CTRLMMR*)
- SW_MAIN_WARMRSTz_MAINMMR (Reset by MAIN domain CTRLMMR*)
- COLD_OUT_RST_n (Reset by DMSC-L)
- WARM_OUT_RST_n (Reset by DMSC-L)
- THERM_MAXTEMP_OUTRANGE_ALERT (Reset by VTM Max Temperature Alert)
- SYSR_ASSERTRESET_n (Reset by DEBUGSS)
- SAFETY_ERROR_RST_n (Reset by ESM Error)
    - MCU ESM Error will reset entire device
    - MAIN ESM Error will only reset MAIN domain

Note

*MAIN domain software WARMRSTz and PORz control registers are defined in both MAIN domain CTRLMMR and MCU domain CTRLMMR.

When the MCU domain is isolated from MAIN domain, and the M4FSS processor can reset the MAIN domain, by programming the registers defined in the MCU domain CTRLMMR.

When a MAIN domain processors need to issue resets on error detection they will use the WARMRSTz and PORz MMR bits defined in the MAIN domain CTRLMMR.

5.3.3.2 MCU_RESETSTATz Status Pin

This pin indicates the internal warm reset status of the device (active LOW).

When LOW, it indicates that the MCU and MAIN domains are in warm reset state.

When HIGH, it indicates that the device is out of warm reset state.

5.3.3.3 MCU_SAFETY_ERRORn Status Pin

This pin indicates the MCU domain ESM status (active LOW).

When LOW, it indicates the MCU ESM module has registered an error.

When HIGH, it indicates that there are no MCU ESM errors.

Note

This signal can be used by external safety devices to determine the device status and assert MCU_PORz if necessary.

5.3.3.4 RESETSTATz Status Pin

This pin indicates warm reset status (active LOW) of the MAIN domain.

When LOW, it indicates that the MAIN domain is in a warm reset state.

When HIGH, it indicates that the MAIN domain is out of reset.

The status of this signal will be captured in CTRLMMR registers.

5.3.3.5 PORz_OUT Status Pin

This pin indicates the POR status of the MAIN domain (active LOW).

When LOW, it indicates the MAIN domain is in the POR state.

When HIGH, it indicates the MAIN domain is out of the POR state.

Note

PORz_OUT must be used to tri-sate Boot Mode pins which are mapped on MAIN IOs so that the Boot Mode, set by external pull-up/down resistors, can safely propagate into the device

5.3.4 Reset Controls

The reset control registers enable, disable, and adjust specific reset operations. This section explains how to control certain device resets.

5.3.4.1 Reset Control Registers

These are the CTRLMMR registers that are able to enable and disable reset abilities and options.

Table 5-460. MCU Domain Reset Control Registers

Control Name	Control Action	Control Register
MCU_ESM_ERROR_RST_ENz	Enable MCU ESM_ERRORz reset	MCU_CTRL_MMR_CFG0_RST_CTRL
DMSC_COLD_RESET_ENz	Enable DMSC-L cold reset of MCU domain	MCU_CTRL_MMR_CFG0_RST_CTRL

Table 5-461. MAIN Domain Reset Control Registers

Control Name	Control Action	Control Register
MAIN_ESM_ERROR_RST_ENz	Enable MAIN ESM_ERRORz Reset	MAIN_CTRL_MMR_CFG0_RST_CTRL
DMSC_COLD_RESET_ENz	Enable DMSC-L Cold Reset of MAIN Domain	MAIN_CTRL_MMR_CFG0_RST_CTRL

Note

For more information, see Control Module (CTRLMMR)

5.3.4.2 Reset Isolation

Reset Isolation Introduction

It is possible to isolate certain SoC modules and subsystems and prevent them from undergoing an arbitrarily generated warm reset. This is known as Reset Isolation. This section describes the device reset isolation capabilities.

Figure 5-159 shows a simple description of the device reset isolation sequence.

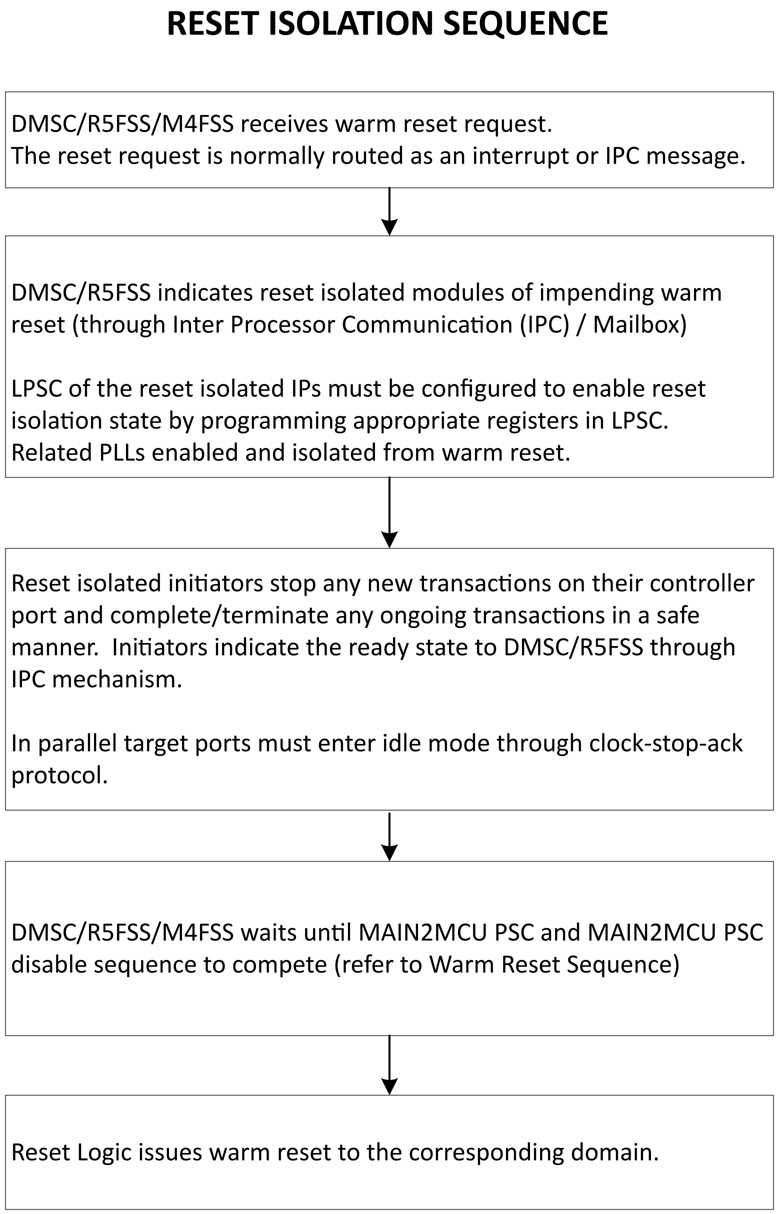

RESET ISOLATION SEQUENCE

DMSC/R5FSS/M4FSS receives warm reset request.
The reset request is normally routed as an interrupt or IPC message.

DMSC/R5FSS indicates reset isolated modules of impending warm reset (through Inter Processor Communication (IPC) / Mailbox)

LPSC of the reset isolated IPs must be configured to enable reset isolation state by programming appropriate registers in LPSC. Related PLLs enabled and isolated from warm reset.

Reset isolated initiators stop any new transactions on their controller port and complete/terminate any ongoing transactions in a safe manner. Initiators indicate the ready state to DMSC/R5FSS through IPC mechanism.

In parallel target ports must enter idle mode through clock-stop-ack protocol.

DMSC/R5FSS/M4FSS waits until MAIN2MCU PSC and MAIN2MCU PSC disable sequence to compete (refer to Warm Reset Sequence)

Reset Logic issues warm reset to the corresponding domain.

Figure 5-159. Simple Reset Isolation Sequence Diagram

Reset Isolation Details

Figure 5-160 shows a detailed description of the device reset isolation sequences.

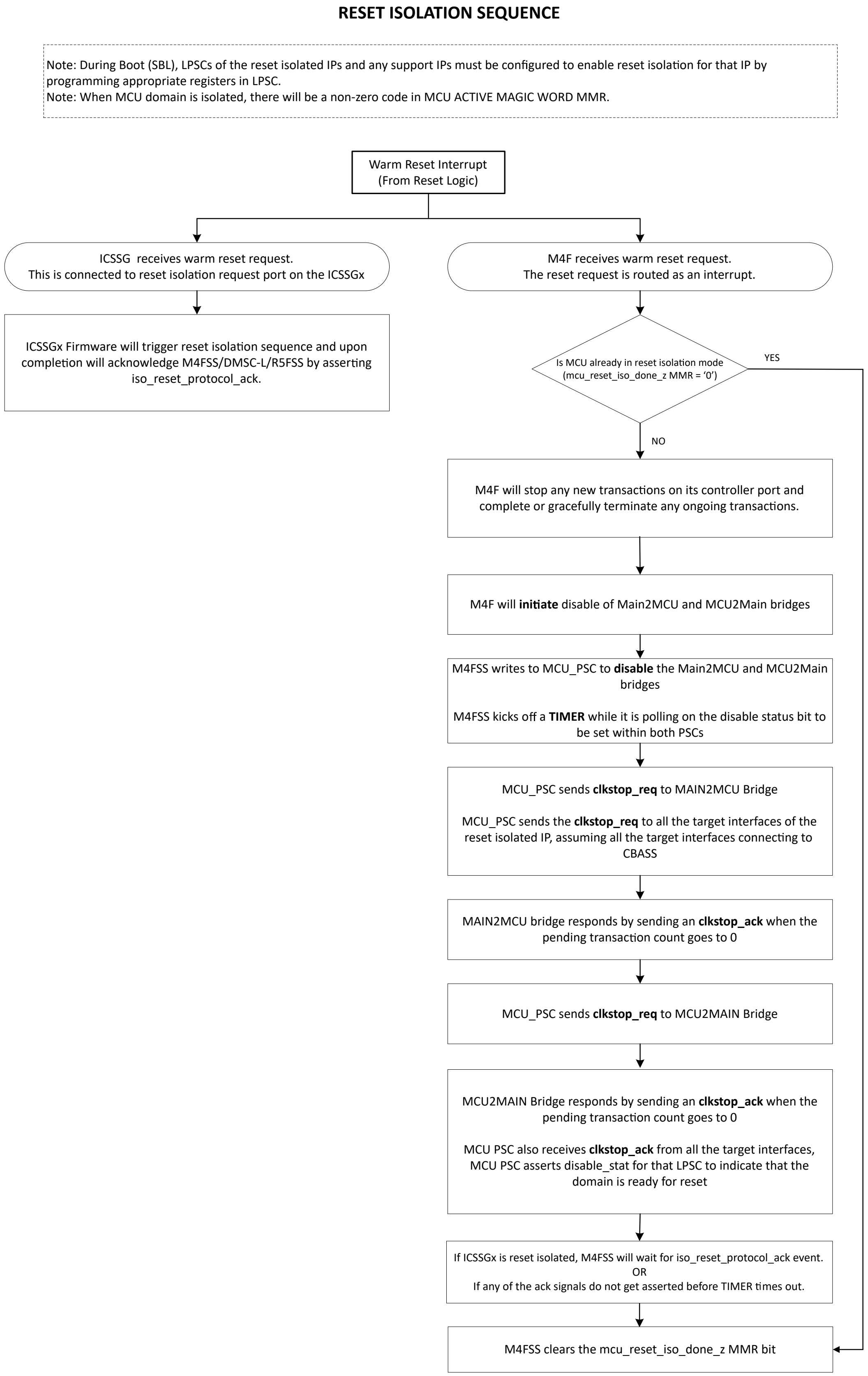

Figure 5-160. Detailed Reset Isolation Sequence Diagram

5.3.5 Reset Details

Reset Details Introduction

The Reset Details section will break down the available device resets and explain operating details such as sequencing and reset logic diagrams. It also includes any additional information related to the device resets.

5.3.5.1 POR Resets

5.3.5.1.1 SW_MAIN_PORz Reset

Reset Overview

This reset is a software controlled MAIN domain POR reset defined in MAIN_CTRL_MMR_CFG0_RST_CTRL and MCU_CTRL_MMR_CFG0_RST_CTRL.

This software reset will generate a MAIN domain PORz.

M4FSS processor will reset the MAIN domain, by writing to the MCU_CTRL_MMR_CFG0_RST_CTRL register.

MAIN domain processors will reset the MAIN domain, by writing to the MAIN_CTRL_MMR_CFG0_RST_CTRL register.

When the MCU domain is configured as a safety domain it must be isolated from SW_MAIN_PORz.

A reset isolation sequence for the MCU domain must be complete prior to reset propagation.

MAIN_CTRL_MMR_CFG0_RST_CTRL and MCU_CTRL_MMR_CFG0_RST_CTRL define a 4-bit field, SW_MAIN_POR[4:7], for generating a software controlled POR for the MAIN domain (SW_MAIN_PORz).

When SW_MAIN_POR [4:7] field is set to “0110”, the MAIN domain is in POR reset state (SW_MAIN_PORz = LOW).

When SW_MAIN_POR [4:7] is set to any other value, the MAIN domain is out of POR reset state (SW_MAIN_PORz = HIGH).

This bit field is reset to “1111” (Inactive State) by default.

MCU Domain Effect

Entire MCU domain is reset isolated.

MCU IOs are not effected.

MAIN Domain Effect

All modules in MAIN domain are reset (including reset isolated modules).

IOs will enter High-Heating-Value (HHV) mode while this reset is active.

MAIN domain CTRLMMR boot configuration register is reset.

Device Boot Mode pins will be re-latched after this reset is de-asserted.

Device will re-boot. During boot-up, R5FSS (secondary boot loader) will poll the CTRLMMR reset status and MCU ACTIVE MAGIC WORD registers and configure MCU domain/M4FSS processor accordingly.

Additional Details

PORz_OUT:

This pin indicates POR status output of the MAIN domain (active LOW).

When LOW, it indicates the MAIN domain is in POR state.

When HIGH, it indicates that the MAIN domain is out of POR state.

Note

PORz_OUT must be used to tri-state boot mode pins which are mapped on MAIN IOs so that boot modes set by external pull-up/down resistors can propagate safely into device.

Note

The boot mode pins are latched internally on the rising edge of MAIN_PORz and are reset isolated from all other device resets.

5.3.5.1.2 MCU_PORz Reset

Reset Overview

This is the POR reset signal (active LOW) for the entire device, controlled by the MCU_PORz HW Pin.

When LOW, it performs a POR reset on the entire device (MCU and MAIN domains) and puts all IOs in a safe state (Reset/HHV state).

MCU Domain Effect

All modules in MCU domain are reset.

MCU IOs are in High-Heating-Value (HHV) state (Reset State).

When MCU_PORz is de-asserted, MCU IOs will enter the default state defined in the device Datasheet. MCU domain will be reconfigured by the R5FSS (secondary boot loader).

MAIN Domain Effect

All modules in the MAIN domain are reset.

MAIN domain IOs are in HHV state (reset state).

When MCU_PORz is de-asserted, the MAIN domain IOs will enter default state as defined in the device Datasheet.

The R5FSS (secondary boot loader) will setup M4FSS as Safety or General-Purpose Processor.

Additional Details

No additional details for MCU_PORz Reset

5.3.5.2 Warm Resets

5.3.5.2.1 MAIN Domain Warm Reset Sequence Flow

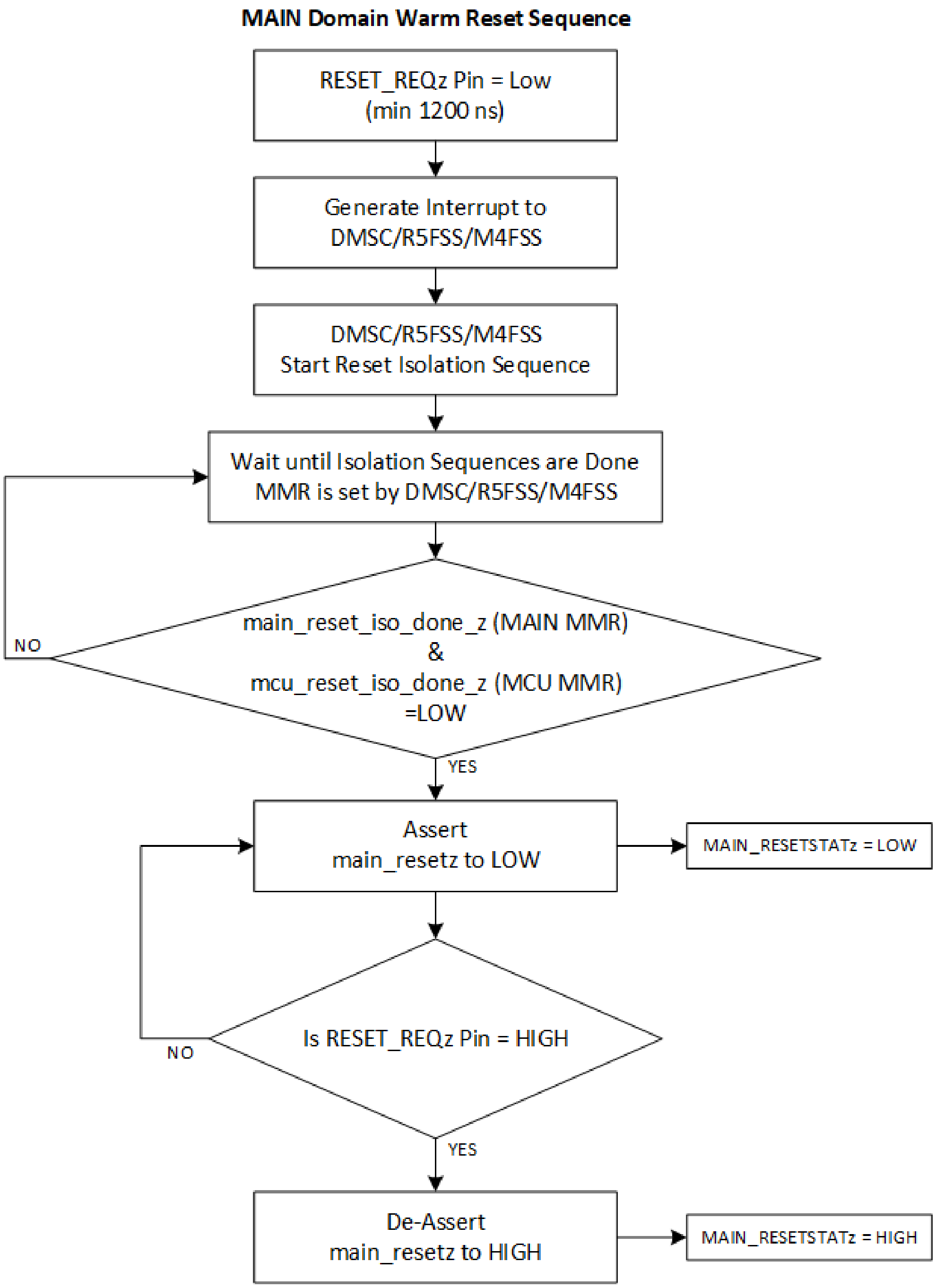

Figure 5-161. MAIN Domain Warm Reset Sequence Flowchart

This flowchart explains the process for a typical MAIN domain warm reset.

5.3.5.2.2 MAIN_RESET_REQz Reset

Reset Overview

This reset signal is the MAIN domain warm reset request (active LOW) controlled by the RESET_REQz HW pin.

When LOW is detected, reset hardware generates an interrupt to processors (A53SS/R5FSS/M4FSS/DMSC-L/ICSSG) so that they can complete the reset isolation sequence before reset is propagated.

This isolation sequence isolates the MCU domain from the MAIN domain so that it is protected against spurious glitches when the MAIN domain is reset.

This sequence also ensures that reset isolated-configured modules such as PRU_ICSSG are in reset isolation before propagating the warm reset to MAIN domain.

MCU Domain Effect

Entire MCU domain is reset isolated.

MCU IOs are not effected.

MAIN Domain Effect

This is a MAIN domain reset request. First, the reset isolation sequence is applied and then the reset is propagated.

All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR register bits which are reset only on MAIN_PORz.

IOs are not effected.

All processor cores are reset (A53SS, DMSC-L, and R5FSS).

Reason for this reset is captured in the CTRLMMR reset source register MAIN_CTRL_MMR_CFG0_RST_SRC. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS secondary boot loader will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/M4FSS processor accordingly.

Reset Sequence

The MAIN_RESET_REQz reset sequence is described below.

Note

The MAIN_RESET_REQz reset signal is equivalent to the RESET_REQz HW Pin.

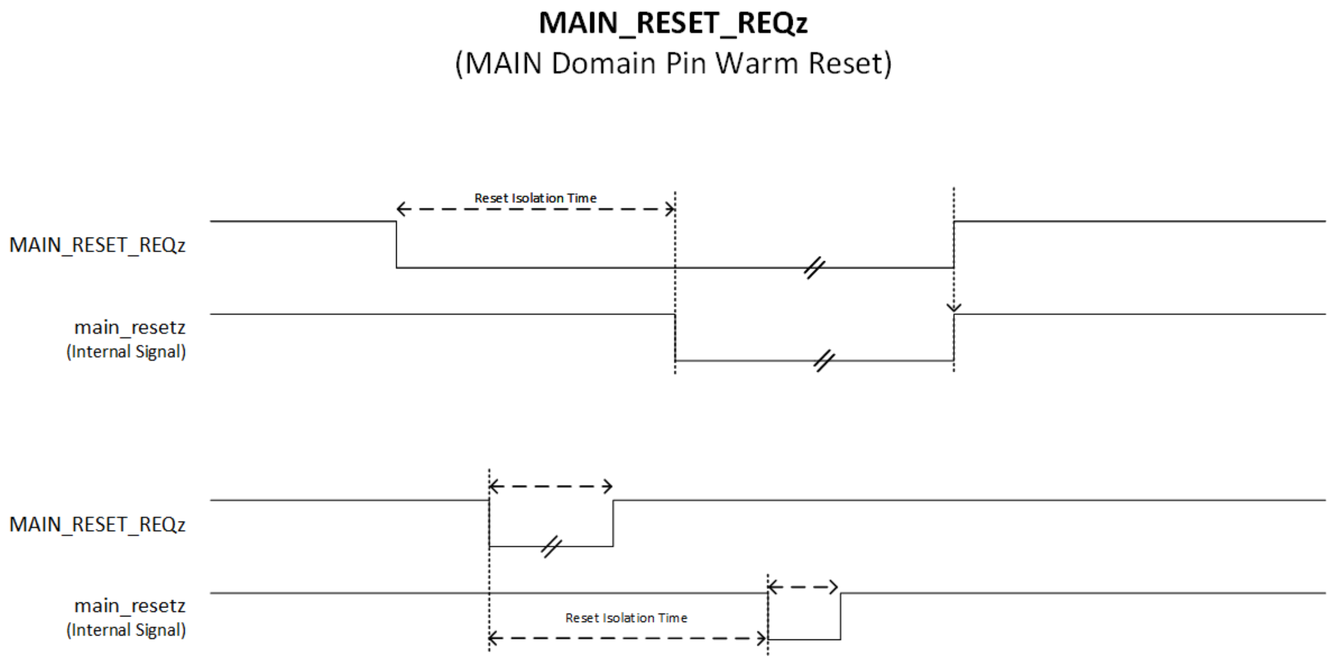

Figure 5-162. MAIN_RESET_REQz Sequence

This diagram shows the timing between the MAIN_RESET_REQz reset signal and the internal RESETz (MAIN domain warm reset) signal.

Additional Reset Details

RESETSTATz:

The RESETSTATz pin indicates the MAIN domain internal reset status (active LOW). This is a reflection of the reset status after the MAIN_RESET_REQz reset signal (RESET_REQz HW Pin) is asserted.

When LOW, it indicates that the MAIN domain is in internal reset state.

When HIGH, it indicates that the MAIN domain is out of internal reset state.

Note

For more details see RESETSTATz Status Pin.

5.3.5.2.3 SW_MAIN_WARMRSTz Reset

Reset Overview

This reset is software controlled MAIN domain warm reset defined in MAIN_CTRL_MMR_CFG0_RST_CTRL and MCU_CTRL_MMR_CFG0_RST_CTRL.

The M4FSS will issue a warm reset to the MAIN domain, by writing to the MCU domain CTRLMMR register.

The MAIN domain processors will issue a warm reset the MAIN domain, by writing to the MAIN domain CTRLMMR register.

Note

When M4FSS is configured as safety processor it must be reset isolated from this MAIN domain warm reset.

A reset isolation sequence for MCU domain has to be complete prior to this reset propagation.

MAIN domain CTRLMMR and MCU domainCTRLMMR registers define a 4-bit field, SW_MAIN_WARMRST[3:0] for generating a software controlled warm reset for the MAIN domain (SW_MAIN_WARMRSTz).

When SW_MAIN_WARMRST[3:0] field is set to “0110”, a MAIN domain warm reset is active (SW_MAIN_WARMRSTz = LOW).

When SW_MAIN_WARMRST[3:0] is set to any other value, the MAIN domain warm reset is inactive (SW_MAIN_WARMRSTz = HIGH).

This bit field is reset to “1111” (Inactive State) by default.

Note

This software reset is equivalent to MAIN_RESET_REQz reset signal (RESET_REQz HW Pin) functionality.

MCU Domain Effect

Entire MCU domain is reset isolated.

MCU IOs are not effected.

MAIN Domain Effect

This is a MAIN domain reset request. First, the reset isolation sequence is applied and then the reset is propagated.

All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR register bits which are reset only on MAIN_PORz.

IOs are not effected.

All processor cores are reset (A53SS, DMSC-L, and R5FSS).

Reason for this reset is captured in MAIN domain CTRLMMR reset status register MAIN_CTRL_MMR_CFG0_RST_STAT. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/M4FSS processor accordingly.

Additional Reset Details

No additional details for SW_MAIN_WARMRSTz reset.

5.3.5.2.4 MCU_RESETz Reset

Reset Overview

The MCU_RESETz signal is the warm reset input (active low) to the entire device, controlled by the MCU_RESETz HW Pin.

When active, it resets all modules in the MCU and MAIN domains.

MCU_RESETz will not reset selected MAIN_CTRL_MMR_CFG0_RST_CTRL and MCU_CTRL_MMR_CFG0_RST_CTRL register bits. These bits are only reset by PORz.

MCU Domain Effect

All modules in MCU domain are reset except for modules and MCU_CTRL_MMR_CFG0_RST_CTRL bits which are reset only on MCU_PORz.

IOs are not effected.

M4FSS is reset.

When MCU_RESETz is de-asserted, the MCU domain needs to be reconfigured by R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for modules and CTRLMMR bits which are reset only on MAIN_PORz.

IOs are not effected.

All processor cores are reset (A53SS, DMSC-L, and R5FSS).

When MCU_RESETz is de-asserted, the device goes through full boot. The reason for this reset is captured in the CTRLMMR reset source register MAIN_CTRL_MMR_CFG0_RST_SRC.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/M4FSS processor accordingly.

Additional Details

MCU_RESETSTATz:

This pin indicates internal MCU_RESETz reset status (active LOW).

When LOW, it indicates that the device, both MCU and MAIN domains, are in internal reset state.

When HIGH, it indicates that the device, both MCU and MAIN domains, are out of internal reset state.

Note

In order for the MAIN domain to come out of reset, MAIN_RESET_REQz (RESET_REQz HW Pin) must also be de-asserted.

Note

For more details see MCU_RESETSTATz Status Pin.

5.3.5.2.5 SW_MCU_WARMRSTz Reset

Reset Overview

This is a software MCU domain warm reset defined in MCU domain CTRLMMR.

CTRLMMR defines a 4-bit field, SW_MCU_WARMRST[8:11] for generating a software warm reset in the MCU domain (SW_MCU_WARMRSTz).

When SW_MCU_WARMRST[8:11] field is set to “0110”, MCU warm reset is active (SW_MCU_WARMRSTz = LOW).

When SW_MCU_WARMRST[8:11] is set to any other value, MCU warm reset is inactive (SW_MCU_WARMRSTz = HIGH).

This bit field is reset to “1111” (Inactive State) by default.

Note

This software reset is equivalent to MCU_RESETz warm reset signal (MCU_RESETz HW Pin) functionality.

MCU Domain Effect

All modules in the MCU domain are reset except for modules and MCU domain CTRLMMR bits which are reset only on MCU_PORz.

IOs are not effected.

M4FSS processor is reset.

When MCU_RESETz is de-asserted, the MCU domain needs to be reconfigured by the R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for modules and MAIN domain CTRLMMR bits which are reset only on MAIN_PORz.

IOs are not effected.

All processor cores are reset (A53SS, DMSC-L, and R5FSS).

When MCU_RESETz is de-asserted, the device goes through full boot. The reason for this reset is captured in CTRLMMR reset source registerMAIN_CTRL_MMR_CFG0_RST_SRC.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD and reconfigure the MCU domain/M4FSS processor accordingly.

Additional Details

No additional details for SW_MCU_WARMRSTz reset.

5.3.5.3 DMSC-L Resets

5.3.5.3.1 DMSC_COLD_OUT_RST_n MAIN Reset

Reset Overview

The DMSC-L will issue this reset upon a security error.

When this reset is enabled in MAIN Domain, it causes a MAIN domain warm reset.

This is an asynchronous reset type (takes effect immediately).

Note

This reset behavior is same as the MAIN_RESET_REQz reset signal (RESET_REQz HW Pin).

MCU Domain Effect

Entire MCU domain is reset isolated.

MCU IOs are not effected.

MAIN Domain Effect

This is a MAIN domain reset request. First, the reset isolation sequence is applied and then the reset is propagated.

All modules in MAIN domain are reset except for reset isolated modules and CTRLMMR register bits which are reset only on MAIN_PORz.

IOs are not effected.

All processor cores are reset (A53SS, DMSC-L, and R5FSS).

Reason for this reset is captured in CTRLMMR reset status register. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/M4FSS processor accordingly.

5.3.5.3.2 DMSC_WARM_OUT_RST_n MAIN Reset

Reset Overview

This reset is a MAIN domain warm reset that is executed from the DMSC-L.

This is an asynchronous reset type (takes effect immediately).

Note

This reset behavior is same as MAIN_RESET_REQz reset signal (RESET_REQz HW Pin).

MCU Domain Effect

Entire MCU domain is reset isolated.

MCU IOs are not effected.

MAIN Domain Effect

This is a MAIN domain reset request. First, the reset isolation sequence is applied and then the reset is propagated.

All modules in MAIN domain are reset except for modules and MAIN domain CTRLMMR register bits which are reset only on MAIN_PORz.

IOs are not effected.

All processor cores are reset (A53SS, DMSC-L, and R5FSS).

Reason for this reset is captured in CTRLMMR reset source status register MAIN_CTRL_MMR_CFG0_RST_SRC. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/M4FSS processor accordingly.

5.3.5.3.3 DMSC_COLD_OUT_RST_n MCU Reset

Reset Overview

The device DMSC-L will issue this reset upon a security error.

When this reset is enabled in MCU domain, it causes a whole device warm reset.

This DMSC-L reset of the MCU domain is enabled only when the DMSC_COLD_RESET_ENz bit in MCU domain CTRLMMR is '0'.

When the M4FSS is configured as a safety processor, it can block this reset from resetting the MCU domain.

This is an asynchronous reset type (takes effect immediately)

Note

This reset behavior is same as MCU_RESETz reset signal (MCU_RESETz HW Pin).

MCU Domain Effect

All modules in MCU domain are reset except for modules and MCU domain CTRLMMR bits which are reset only on MCU_PORz.

IOs are not effected.

M4FSS is reset.

When MCU_RESETz is de-asserted, the MCU domain will be reconfigured by R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for modules and CTRLMMR bits which are reset only on MAIN_PORz.

IOs are not effected.

All processor cores are reset (A53SS, DMSC-L, and R5FSS).

When MCU_RESETz is de-asserted, the device goes through full boot. The reason for this reset is captured in the CTRLMMR reset source register MAIN_CTRL_MMR_CFG0_RST_SRC.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD and reconfigure the MCU domain/M4FSS processor accordingly.

5.3.5.4 VTM Thermal Alert Reset

Reset Overview

The VTM module outputs an alert signal (THERM_MAXTEMP_OUTRANGE_ALERT), when the device temperature goes beyond a maximum threshold.

This reset signal creates a MCU domain warm reset.

VTM alert will be active as long as the error condition (Device Temperature > Maximum Temperature Threshold) is still TRUE.

When the error goes away, VTM alert will be de-asserted and device will come out of warm reset.

Note

This signal, when asserted HIGH, will cause a device warm reset similar to MCU_RESETz.

MCU Domain Effect

All modules in MCU domain are reset except for modules and MCU domain CTRLMMR bits which are reset only on MCU_PORz.

IOs are not effected.

This reset is active as long as the VTM alert is active.

When THERM_MAXTEMP_OUTRANGE_ALERT is de-asserted, the MCU domain needs to be reconfigured by R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for modules and CTRLMMR bits which are reset only on MAIN_PORz.

IOs are not effected.

All processor cores are reset (A53SS, DMSC-L, and R5FSS).

When THERM_MAXTEMP_OUTRANGE_ALERT is de-asserted, the device goes through full initialization procedure. The reason for this reset is captured in the CTRLMMR reset source register MAIN_CTRL_MMR_CFG0_RST_SRC.

Additional Reset Details

VTM alert use-case example:

VTM sends out a warning signal before generating the Max Temp Alert.

There are 2 different threshold settings for max temperature limits.

The first one has a lower threshold which will generate an interrupt to the processor for taking action to reduce frequency, turn-off power domains, etc. This should eventually lower the temperature and avoid the Max Temp Alert.

If the interrupt does not fix the rising temperature, then VTM will issue a Max Temp Alert. This will cause a device warm reset. The VTM Max Temp Alert will be active as long as die temperature is above the programmed threshold.

Device warm reset will default certain power domains to off mode (default at power-up). This should eventually lower the die temperature further.

Software can read the reset status register to poll on the cause of the warm reset. If it is from VTM, then it can wait for additional time before turning on the power domains.

5.3.5.5 MAIN ESM_ERRORz Reset

Reset Overview

This reset is issued when a MAIN domain processor (A53SS, DMSC-L, or R5FSS) detects a catastrophic software error or a MAIN domain WDT timeout event occurs.

Errors in the MAIN domain cause the MAIN ESM module to trigger ESM_ERRORz.

This is routed as internal MAIN domain warm reset when enabled by the MAIN domain CTRLMMR reset control bit (MAIN_ESM_ERROR_RST_ENz).

This is an asynchronous reset type (takes effect immediately).

Reset MCU Domain Effect

Entire MCU domain has been previously reset isolated.

MCU IOs are not effected.

Reset MAIN Domain Effect

All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR bits which are reset only on MAIN_PORz.

IOs are not effected.

The device will re-boot. During boot-up, the R5FSS (secondary boot loader) will poll the CTRLMMR reset registers and reconfigure the MCU domain/M4FSS processor accordingly.

Note

If the device boot fails, and the MCU_SAFETY_ERRORn level is still LOW, then an external safety device should issue the MCU_PORz Reset to allow the device to recover from this error.

5.3.5.6 MCU ESM_ERRORz Reset

Reset Overview

This reset is issued when the M4FSS detects a catastrophic safety error or a MCU WDT timeout occurs.

Errors in the MCU domain cause the MCU ESM module to trigger ESM_ERRORz.

This is routed as a device warm reset when enabled by the MCU domain CTRLMMR bit (MCU_ESM_ERROR_RST_ENz).

This is an asynchronous reset type (takes effect immediately).

MCU Domain Effect

All modules in MCU domain are reset except for reset isolated modules and MCU domain CTRLMMR bits which are reset only on PORz.

IOs are not effected.

Error is reported on MCU_SAFETY_ERRORn pin.

When SAFETY_ERROR_RST_n is de-asserted, the MCU domain needs to be reconfigured by the R5FSS (secondary boot loader) in the MAIN domain.

External hardware (PMIC or secondary MCU safety channel) must issue MCU_PORz to recover from this error.

MAIN Domain Effect

All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR bits which are reset only on PORz.

IOs are not effected.

Device will re-boot. During boot-up, the R5FSS (secondary boot loader) will poll the CTRLMMR reset source register and configure the MCU domain/M4FSS processor accordingly.

If the device boot fails, and MCU_SAFETY_ERRORn level is still LOW, then an external safety device should issue the MCU_PORz reset to allow the device to recover from the error.

5.3.5.7 Reset - High Heating Value (HHV)

IOs support HHV mode during power up. HHV is defined as a state when PORz signal is driven LOW.

HHV allows IO cells to be tri-stated and is an IO feature. All IO cells have HHV which is asserted (driven) by HHV generated during PORz assertion. There are default pull values during this HHV/PORz assertion specified in the device Datasheet for each pin. All HHV logic controlling the buffer high-impedance control and the associated default pull value will be asynchronous.

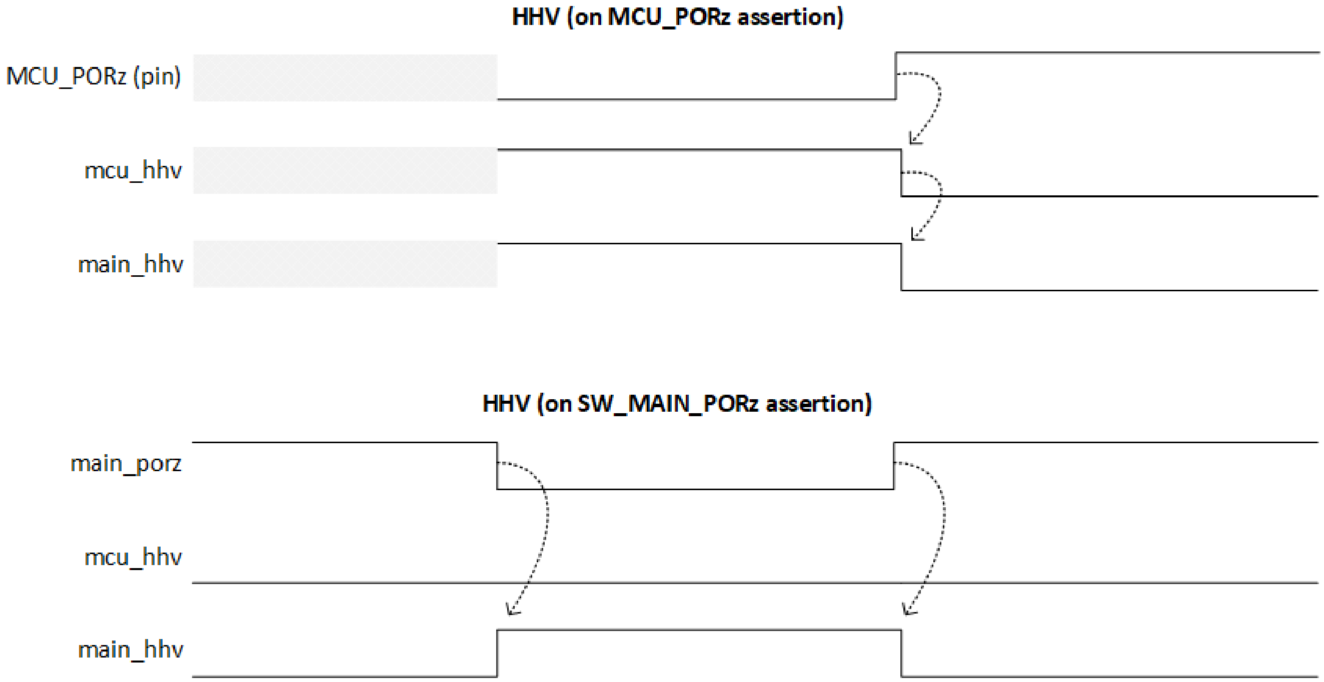

Figure 5-163. HHV Timing Diagram

This diagram demonstrates the timing sequence for the device HHV signals.

5.4 Clocking

This chapter describes the clock architecture of the device.

5.4.1 Overview

To satisfy the various subsystems requirements, the device features multiple clock sources and clock generators:

- External Crystal Driver
- Internal Oscillator
- Phase-Locked Loop circuits (PLLs)
- Dividers

Figure 5-164 shows the device top-level clock diagram. The clocking is divided into two clocking domains - MCU and MAIN.

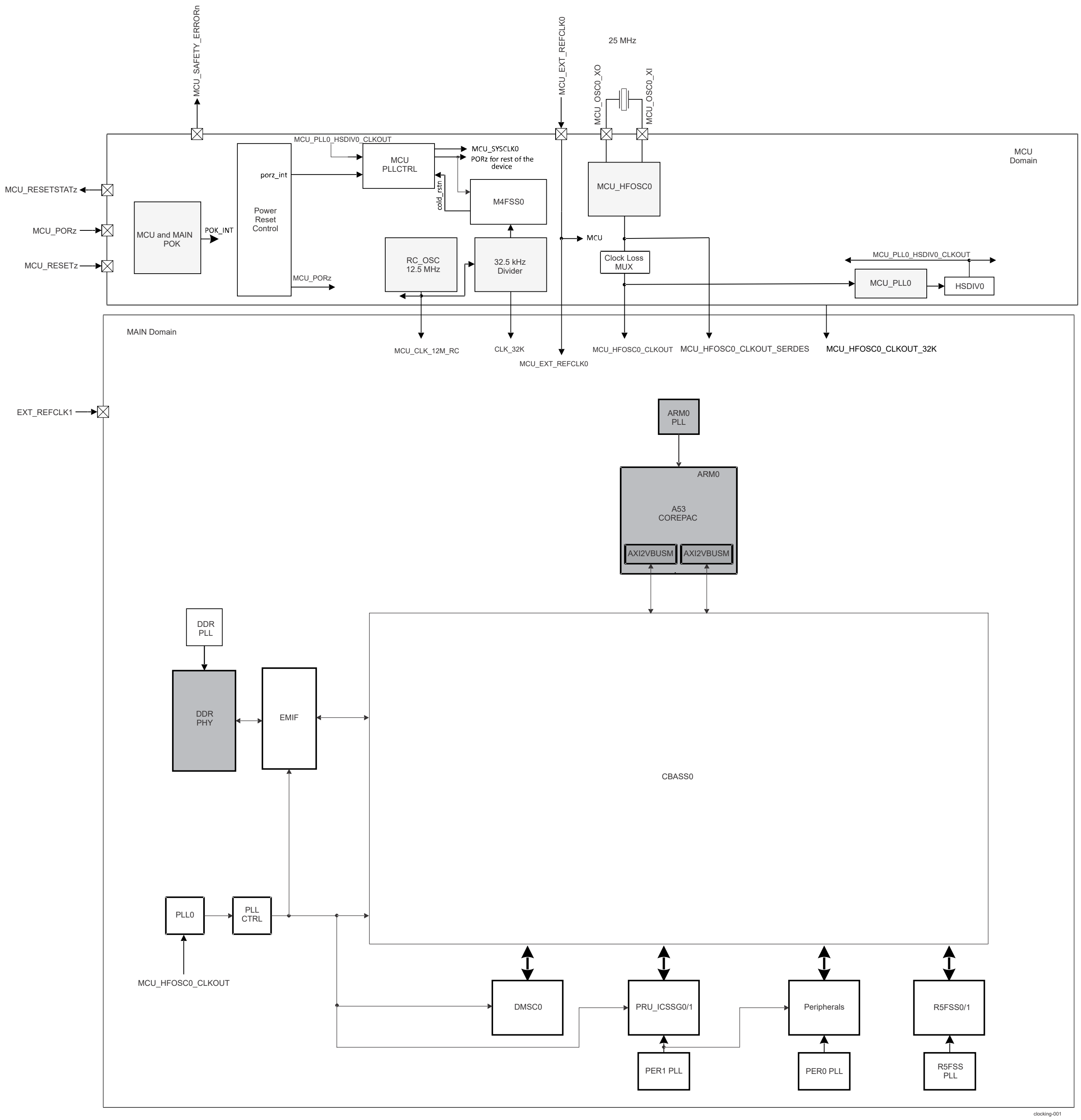

Figure 5-164. Top-Level Clock Diagram

5.4.2 Clock Inputs

5.4.2.1 Overview

Various external clock inputs are needed to drive the device. Summary of these input clock signals is as follows:

- High frequency oscillators
  - MCU_OSC0_XO/MCU_OSC0_XI — external main crystal interface pins of the internal oscillator which sources a reference clock. Provides reference clock to PLLs within MCU and MAIN domain.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — optional external system clock input (MCU domain).
  - EXT_REFCLK1— optional external system clock input (MAIN domain).
- External CPTS reference clock inputs
  - CPTS0_RFT_CLK — CPTS reference clock input for CPTS_RFT_CLK.

Note

Other clock inputs that are routed directly to the subsystems are described in the respective subsystem chapters.

Note

EXT_REFCLK1 clock pin is routed to clock muxes as one of the selectable input clock source to the Timer modules (DMTIMER/WDT), DMTIMER in SMS (Security Subsystem), MCAN and CPTS (Time Stamping Module). If an application needs a very specific clock frequency to be fed into these modules then they have an option to use the EXT_REFCLK1 (for example: time synchronization or for clock quality reasons).

5.4.2.2 Mapping of Clock Inputs

For additional details related to Clock Input Mapping, see device specific datasheet.

5.4.3 Clock Outputs

The device provides several system clock outputs. Summary of these output clock signals is as follows:

- MCU_SYSCLKOUT0
- MCU_OBSCLK0
- SYSCLKOUT0
- OBSCLK0

Other clock outputs, that are routed directly from subsystems to device pins, are described in the respective module chapter.

Observation clock pins - MCU_OBSCLK0 and OBSCLK0 serve the following purposes:

- During testing, PLLs on the device are configured to output all operating frequencies desired by each module to characterize PLL performance.
- System debug: during debug, clocks from various PLLs can be inspected for possible clues. Example clock glitches, lock loss etc.

Note

Maximum frequency supported on both MCU_OBSCLK0 and OBSCLK0 pins is 200 MHz. Hence the divider at the output of each OBSCLK mux must be programmed to meet this limitation.

Unlike the OBSCLK pins which can select several different clocks for output, system clock pins (MCU_SYSCLKOUT0 and SYSCLKOUT0) are hardwired to dedicated clock resources (see Section 5.4.3.2)

5.4.3.1 Observation Clock Pins

5.4.3.1.1 MCU_OBSCLK0 Pin

MCU_OBSCLK0 output is controlled by CTRLMMR_MCU_OBSCLK_CTRL register in the MCU_CTRL_MMR0 module; for more information about control registers, see Section 5.1 , *Control Module (CTRL_MMR)*. Two muxes are connected in series - MCU_OBSCLK0_MUX0 and MCU_OBSCLK0_MUX1, see Figure 5-165.

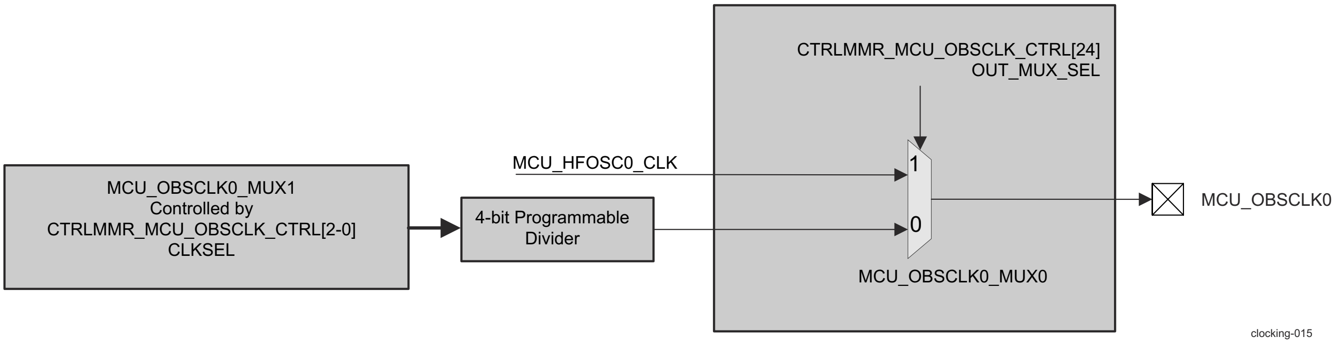

Figure 5-165. MCU_OBSCLK Muxes Diagram

How to select the output of MCU_OBSCLK0_MUX1 is described in Table 5-324.

Table 5-462. MCU_OBSCLK0_MUX1 Output Clock Selection

CTRLMMR_MCU_OBSCLK_CTRL[(2)][2-0] CLK_SEL	MCU_OBSCLK0_MUX1 Output Clock Selection[(1)]
0x0	MCU_CLK_12M_RC
0x1	0 (GND)[(3)]
0x2	MCU_PLL0_HSDIV0_CLKOUT
0x3	MCU_PLL0_HSDIV4_CLKOUT
0x4	MCU_PLLCTRL_OBSCLK
0x5	CLK_32K

Table 5-462. MCU_OBSCLK0_MUX1 Output Clock Selection (continued)

CTRLMMR_MCU_OBSCLK_CTRL[2][2-0] CLK_SEL	MCU_OBSCLK0_MUX1 Output Clock Selection[1]
0x6	MCU_HFOSC0_CLKOUT
0x7	MCU_HFOSC0_CLKOUT_32K

(1) Software-controlled 4-bit divider is used to obtain the divided versions of the clocks passed to MCU_OBSCLK1 mux
(2) For more information about control registers, see Section 5.1 , *Control Module (CTRL_MMR)*.
(3) GND - ground

The value of the software-controlled 4-bit divider is determined by the CTRLMMR_MCU_OBSCLK_CTRL[11-8] CLK _DIV field; for more information about control registers, see Section 5.1 , *Control Module (CTRL_MMR)*.

5.4.3.1.2

Note

MCU_OBSCLK1_MUX0 is provided as a low jitter output for MCU_HFOSC0_CLK. In this configuration, CTRLMMR_MCU_OBSCLK_CTRL[2-0] should be configured as 0x1 (1, selecting a logical low signal) and CTRLMMR_MCU_OBSCLK_CTRL[24] should be configured as 0x1.

5.4.3.1.3 OBSCLK0 Pin

The OBSCLK0 output pin is controlled by MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL register in the CTRL_MMR0 module; for more information about control registers, see Section 5.1 , *Control Module (CTRL_MMR)*. Figure 5-166 shows a block diagram of internal OBSCLK0 mux connections.

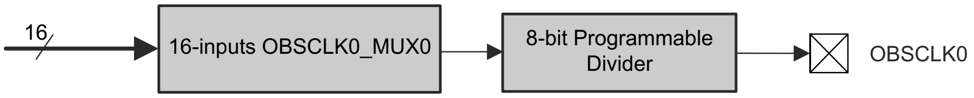

Figure 5-166. OBSCLK0 Muxes Diagram

Table 5-463. OBSCLK0 Clock Selection

MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL[2][3-0] CLK_SEL	OBSCLK0 Selection [1]
0x0	MAIN_PLL0_HSDIV0_CLKOUT
0x1	MAIN_PLL1_HSDIV0_CLKOUT
0x2	MAIN_PLL2_HSDIV0_CLKOUT
0x3	MAIN_PLL8_HSDIV0_CLKOUT
0x4	MAIN_PLL12_HSDIV0_CLKOUT
0x5	MCU_CLK_12M_RC
0x6	MCU_HFOSC0_CLKOUT_32K
0x7	PLLCTRL_OBSCLK
0x8	MCU_HFOSC0_CLKOUT
0x9	CLK_32K
0xA	0 (GND)[3]
0xB	0 (GND)[3]
0xC	CPTS_GENF1
0xD	CPTS_GENF2
0xE	CPTS_GENF3
0xF	MAIN_PLL14_HSDIV0_CLKOUT

Table 5-463. OBSCLK0 Clock Selection (continued)

MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL[2][3-0] CLK_SEL	OBSCLK0 Selection [1]
0x1A	CPTS_GENF3

(1) Software-controlled 8-bit divider is used to obtain the divided versions of the clocks passed to outpt pins

(2) For more information about control registers, see Section 5.1 , *Control Module (CTRL_MMR)*.

(3) GND - ground

The value of the software-controlled 8-bit divider is determined by register MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL[15-8] CLK_DIV; for more information about control registers, see Section 5.1 , *Control Module (CTRL_MMR)*.

5.4.3.2 System Clock Pins

5.4.3.2.1 MCU_SYSCLKOUT0

MCU_SYSCLK0 is divided by 4 and then send out of the device as a LVCMOS clock signal (MCU_SYSCLKOUT0).

Note

MCU_SYSCLKOUT0 cannot be used as a clock source for external devices on the board.

5.4.3.2.2 SYSCLKOUT0

SYSCLK0 is divided by 4 and then send out of the device as a LVCMOS clock signal (SYSCLKOUT0). This signal can be used to test if the specific device clock is functioning or not.

Note

SYSCLKOUT0 cannot be used as a clock source for external devices on the board.

5.4.4 Device Oscillators

The device has the possibility to source clocks of an external high-frequency oscillator - MCU_HFOSC0. The device has also one internal RC oscillator - MCU_RC_OSC_12M.

5.4.4.1 Device Oscillators Integration

5.4.4.1.1 Oscillator with External Crystal

By default, MCU_HFOSC0 is enabled after PORz. It supports a bypass mode. In this mode, an external clock can be driven on the XI Pin.

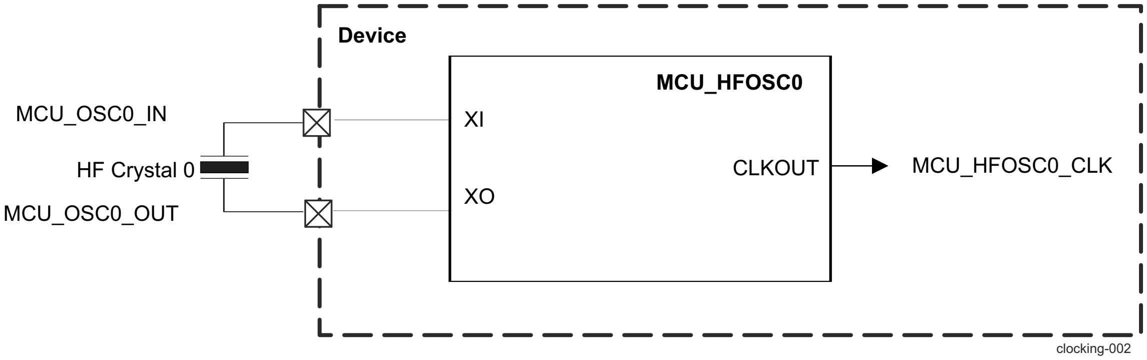

Figure 5-167. MCU_HFOSC0 Integration Diagram

5.4.4.1.2 Internal RC Oscillator

MCU_RC_OSC_12M in always oscillate mode.

The 12.5-MHz RC clock output (MCU_RC_OSC_12M) is used by the on-chip Reset Glue logic, Power Reset Generator (PRG) circuits, MCU_HFOSC0 Loss Circuits, Dual Clock Comparator (DCC) and Timer Modules.

Note

An output clock of MCU_RC_OSC_12M is further divided down to generate a 32-kHz clock (CLK_32K). This clock is used by DMSC0 and Timer Modules.

The actual value of the derived CLK_32K will vary with PVT variations. For more information, see the device-specific Datasheet.

5.4.4.2 Oscillator Clock Loss Detection

The device supports MCU_HFOSC0 clock loss circuitry to detect when MCU_HFOSC0_CLK stops toggling. If CTRLMMR_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN is set and MCU_HFOSC0_CLK stops toggling condition is detected, the reference clock is switched from MCU_HFOSC0_CLKOUT to MCU_CLK_12M_RC to allow the device to operate with a slower clock. The MCU_HFOSC0_CLK stops toggling condition is reported as an error to MCU_ESM0 regardless of the value of CTRLMMR_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN. Integration diagram of MCU_HFOSC0 clock loss detection is presented in Figure 5-168.

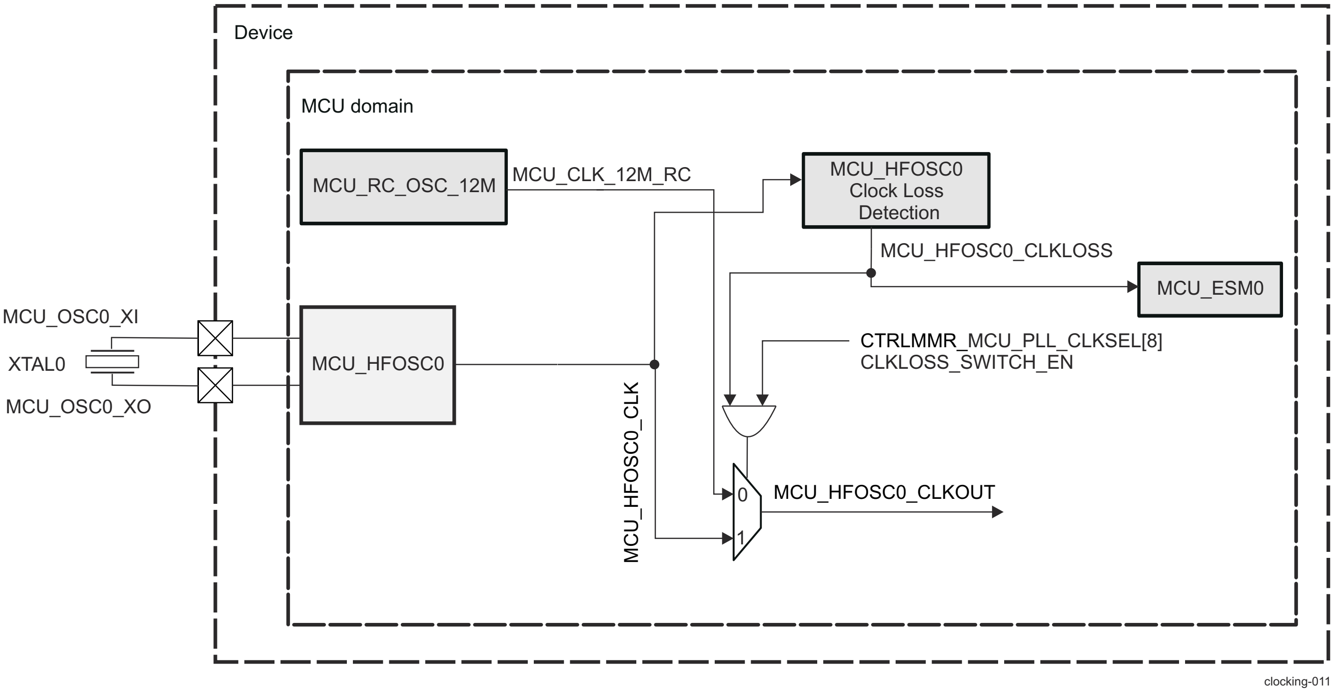

Figure 5-168. MCU_HFOSC0 Clock Loss Detection Integration Diagram

MCU_ESM0 can optionally generate an interrupt to R5FSS0/1 and MCU_M4FSS0 so they can save some critical contents such as error logging to scratch pad memory or external flash. ESM must also be configured to report this error on the MCU_SAFETY_ERRORn pin.

MCU_HFOSC0 clock loss is a catastrophic failure since this clock is the most critical system clock. During the clock loss condition an external system intervention is required.

The clock loss mux is not a glitch free mux. The mux control is synchronized to the MCU_CLK_12M_RC clock. Since MCU_HFOSC0_CLK has stopped switching the mux should transition to RC Clock without producing glitches.

Hence it is important to ensure that MCU_SAFETY_ERRORn is pulled low during this error condition. In clock-loss condition, the device reports the error to the external device through MCU_SAFETY_ERRORn pin - the pin is driven Low. The recovery mechanism is up to the external system (such as a PMIC to take action). For example, it can try a full system power cycle to see if the system recovers. If the system does not recover then, it has to take some other action such as to check system clocks, external crystal, supply rails.

PLL will lose the lock when clock loss is detected. During this time 12.5-MHz RC clock is output through the bypass muxes. The PLL will relock to a new frequency based on 12.5 MHz.

In an event of clock glitch which may potentially hang the device, then the DMSC0 watchdog timer will expire and will generate an internal reset for the whole device.

5.4.5 PLLs

Phase-Locked Loop circuits (PLLs) in the device are clock generator PLLs, which multiply the lower-frequency reference clock up to the operating frequency of the respective subsystem(s).

5.4.5.1 MCU Domain PLL Overview

MCU_PLL0 (MCU PLL) with MCU_PLLCTRL0 are present in the device in MCU domain. An overview is shown on Figure 5-169. For more specific information about PLLs see Section 5.4.5.5 , *PLLs Device-Specific Information*.

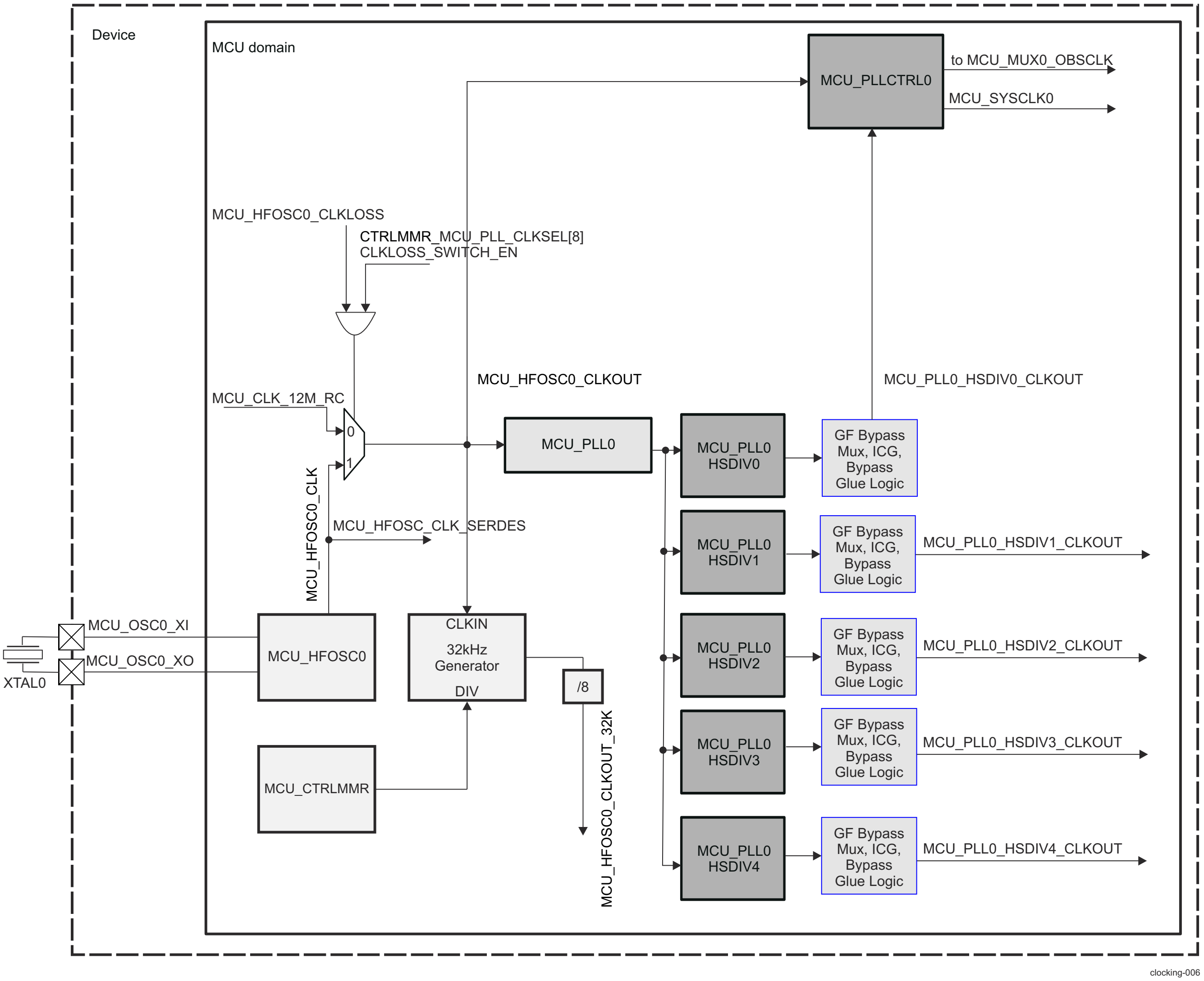

Figure 5-169. MCU Domain PLLs Integration

5.4.5.2 MAIN Domain PLLs Overview

The following are the PLLs in the device in MAIN domain:

- PLL0 (MAIN PLL) with PLLCTRL0
- PLL1 (PER0 PLL)
- PLL2 (PER1 PLL)
- PLL8 (ARM0 PLL)
- PLL12 (DDR PLL)
- PLL14 (R5FSS PLL)

Overview of the device PLLs with their reference clock options in MAIN domain is shown on Figure 5-170. For more specific information about PLLs see Section 5.4.5.5 , *PLLs Device-Specific Information*.

Note

The external muxes of choosing the reference clocks are glitch-free muxes.

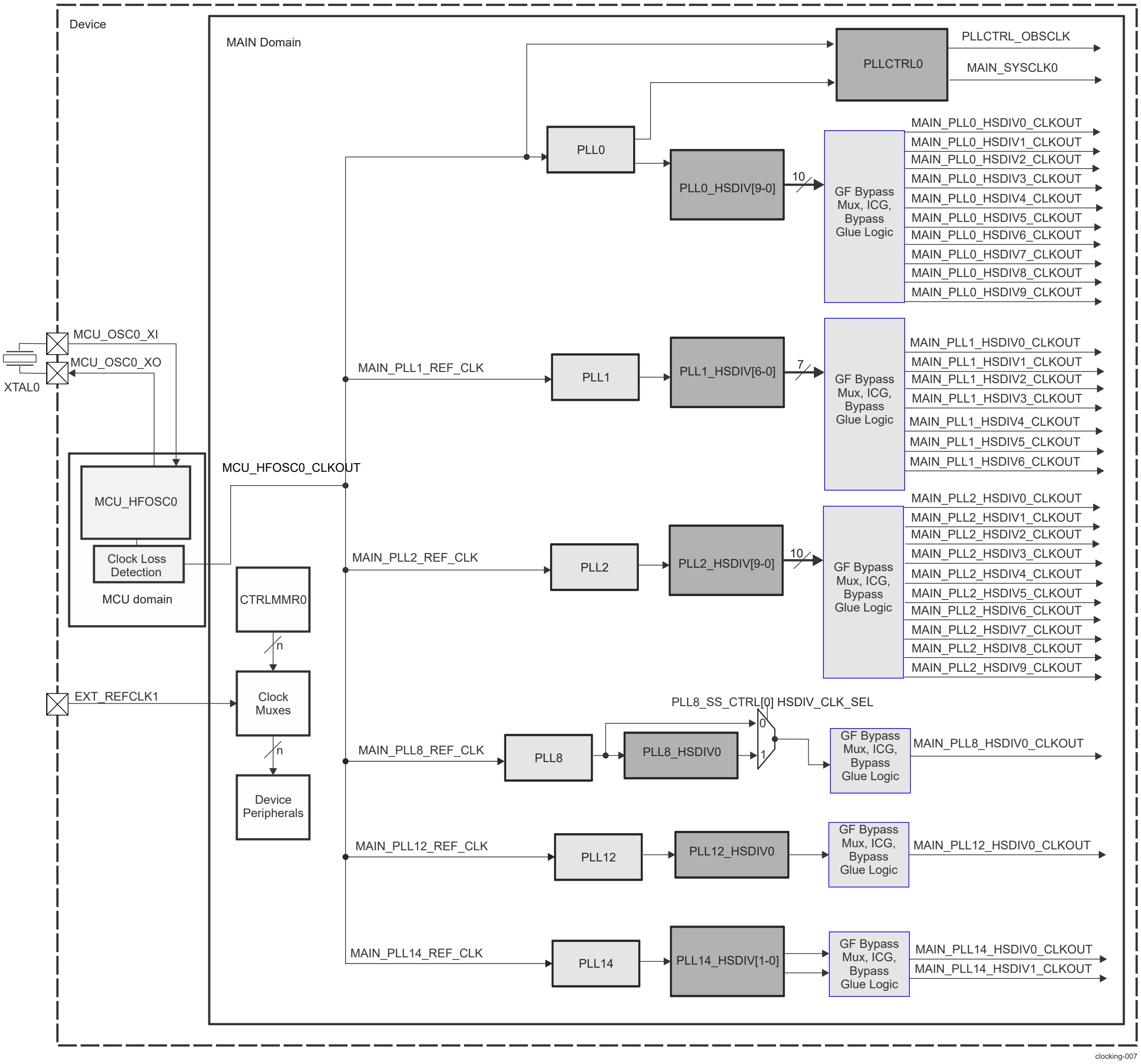

Figure 5-170. MAIN Domain PLLs Integration

5.4.5.3 PLL Reference Clocks

5.4.5.3.1 PLLs in MCU Domain

The reference clock MCU_PLL0_REF_CLK for the PLL in MCU domain is chosen between the internal high-frequency (HF) oscillator with external crystal (MCU_HFOSC0) and 12.5-MHz free-running RC oscillator. The selection is made through CTRLMMR_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN, see Table 5-326.

Table 5-464. PLL MCU Domain Reference Clock Selection - MCU_HFOSC0_CLKOUT Selection

CTRLMMR_MCU_PLL_CLKSEL[(1)][8] CLKLOSS_SWTCH_EN	MCU_PLL0_REF_CLK
0 (default)	MCU_HFOSC0_CLK
1	MCU_CLK_12M_RC if clock loss is detected or MCU_HFOSC0_CLK if clock loss is not detected

(1) For more information about control registers, see Section 5.1 , *Control Module (CTRL_MMR)*.

5.4.5.3.2 PLLs in MAIN Domain

Each PLL in MAIN domain has a dedicated register (MAIN_CTRL_MMR_CFG0_MAIN_PLLn_CLKSEL, n = 0 to 2, 8, 12, 14) in CTRL_MMR0 that contains associated control bits.

5.4.5.4 Generic PLL Overview

To generate high-frequency clocks, the device supports multiple on-chip PLLs controlled directly by the Top-level Clocking. Their type is Fractional PLL with Calibration (PLLTS16FFCLAFRACF).

Note

This chapter discusses only the PLLs that are directly controlled by the Top-level Clocking. The other PLLs embedded in and managed by other subsystems are described in their respective subsystems.

5.4.5.4.1 PLLs Output Clocks Parameters

Figure 5-171 shows the functional architecture of a generic PLL for PLLTS16FFCLAFRACF type.

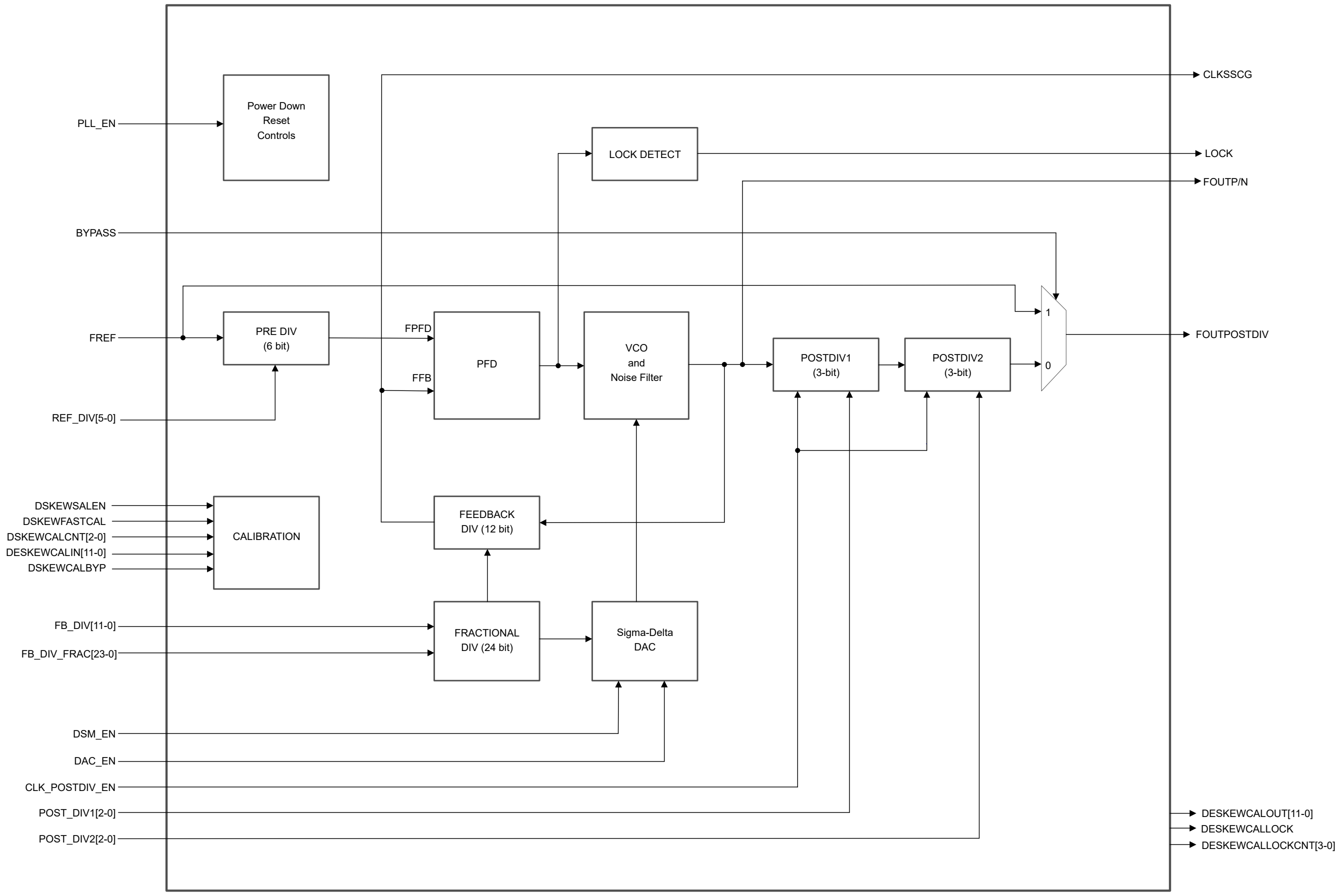

Figure 5-171. Generic PLL Functional Diagram for PLLTS16FFCLAFRACF Type

5.4.5.4.1.1 PLLs Input Clocks

As shown in Figure 5-171 the reference clock (FREF) input is used to generate the synthesized clock, but can also be used as the bypass clock for some outputs of the PLL whenever the PLL enters bypass mode. It is mandatory for the PLL clock synthesis.

5.4.5.4.1.2 PLL Output Clocks

5.4.5.4.1.2.1 PLLTS16FFCLAFRACF Type Output Clocks

Table 5-327 describes the output clocks of PLLTS16FFCLAFRACF.

Table 5-465. PLLTS16FFCLAFRACF Output Clocks

Output	Description	Frequency
FOUTP	Positive phase VCO output (no post divider)	(FREF / REF_DIV) * (FB_DIV + FB_DIV_FRAC)
FOUTN	Negative phase VCO output (no post divider)	(FREF / REF_DIV) * (FB_DIV + FB_DIV_FRAC)
FOUTPOSTDIV	VCO-divided clock output.	FOUTP / (POST_DIV1*POST_DIV2)

Where:

- REF_DIV is the software-configured division ratio binary value.
- FB_DIV is the software-configured division ratio binary value.
- FB_DIV_FRAC is the software-configured fractional division.
- POST_DIV1 is the software-configured division ratio binary value.

- POST_DIV2 is the software-configured division ratio binary value.

Note

POST_DIV1 and POST_DIV2 valid values are from 1 to 7. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater than POST_DIV2.

Note

For device-specific information about clock output parameters and syntesized clocks, see Table 5-331 and Table 5-332.

5.4.5.4.1.2.2 PLL Lock

PLL module outputs a lock status signal to indicate that the PLL has achieved frequency lock. When the PLL detects no cycle slips between the feedback clock (FFB) and reference clock FPFD (FREF/ REF_DIV[5-0]) for 128 consecutive cycles, it asserts the lock signal high. When the PLL detects any cycle slip, lock signal will go low and stays low until it detects no cycle slip for 128 consecutive cycles. This lock signal is captured in <PLL_name>_STAT[0] LOCK bit. Software can read this bit to determine if the PLL has achieved frequency lock before selecting the PLL clock through external bypass mux.

When PLL losses lock, there is a hardware mechanism to automatically bypass the PLL clock to the reference clock (FREF) using the external glitch free mux. BYP_ON_LOCKLOSS bit in <PLL_name>_CTRL register enables this automatic bypass mode on PLL lock loss. When the PLL re-locks, the glitch free mux switches to PLL clock out.

The PLL Lock signal is also routed to ESM module for error reporting. ESM can be configured to generate interrupts to MCU_M4FSS0 and R5FSS0/1 and assert Low on SAFETY_ERRORn pin on PLL Lock loss for further action.

5.4.5.4.1.2.3 HSDIVIDER

A PLL may contain up to 16 HSDIVIDER modules to produce more clocks with divided ratio based on the PLL synthesized clock frequency. HSDIVIDER provides only one output. The HSDIVIDER output clock frequency is given by the equations in Table 5-328.

Table 5-466. HSDIV_CLKOUT Frequency With PLL State

Equation	PLL Mode
HSDIV_CLKOUT = FOUTP / (HSDIV + 1)	Locked
HSDIV_CLKOUT = FREF	Before lock or during relock

Where:

- FOUTP is the PLL lock frequency.
- HSDIV is the software-configured division ratio binary value.

Figure 5-172 describes the connection between a HSDIV and a specific type of PLL. Signals related only to this connections are shown in both figures.

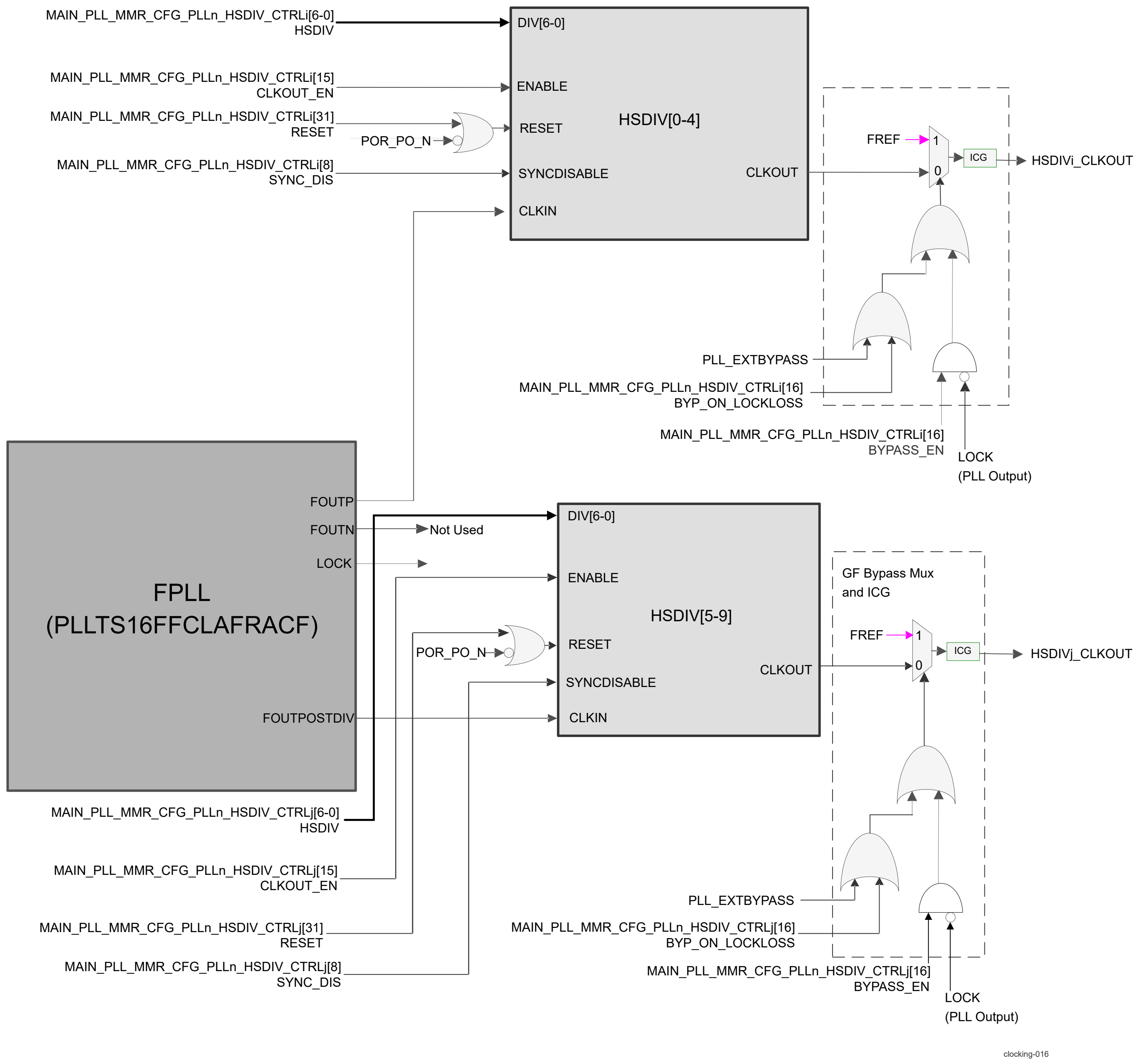

Note

(1)i = 0 to 4; j = 5 to 9

Figure 5-172. PLLTS16FFCLAFRACF and HSDIV Connection

5.4.5.4.1.2.4 ICG Module

ICG module ensures that when a particular HSDIV is not enabled the HSDIV clock output is gated off. This is a hardware module with no software control.

5.4.5.4.1.2.5 PLL Power Down

PLLTS16FFCLAFRACF is disabled with MCU_PLL0_CTRL [15] PLL_EN or PLLn_CTRL[15] PLL_EN.

5.4.5.4.1.2.6 PLL Calibration

PLLTS16FFCLAFRACF has calibration feature. The calibration settings are done via <PLL_Name>_CAL_CTRL register. The calibration status can be monitored by reading <PLL_Name>_CAL_STAT register. For more information about device-specific information about calibration feature, see Table 5-333.

5.4.5.5 PLLs Device-Specific Information

Table 5-329 lists the basic information of the MCU PLL.

Table 5-467. Basic Information of MCU_PLL0

PLL name	Type	HSDIV Available	Input clock	Comments
MCU_PLL0	PLLTS16FFCLAFRACF	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4	MCU_HFOSC0_CLKOUT	See (1), (2), and (3)

(1) See Figure 5-171, *Generic PLL Functional Diagram for PLLTS16FFCLAFRACF type* for overview of the PLL.
(2) See Section 5.4.5.5.1 for synthezised clock parameters.
(3) See Section 5.4.5.5.2 for clock output parameters.

Table 5-330 lists the basic information of each of the MAIN PLLs.

Table 5-468. Basic Information of MAIN Domain PLLs

PLL name	Type	HSDIV Available	Input clock	Comments
PLL0	PLLTS16FFCLAFRACF	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4, HSDIV5, HSDIV6, HSDIV7, HSDIV8, HSDIV9	MAIN_PLL0_REF_CLK	See (1), (2), and (3)
PLL1	PLLTS16FFCLAFRACF	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4, HSDIV5, HSDIV6	MAIN_PLL1_REF_CLK	See (1), (2), and (3)
PLL2	PLLTS16FFCLAFRACF	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4, HSDIV5, HSDIV6, HSDIV7, HSDIV8, HSDIV9	MAIN_PLL2_REF_CLK	See (1), (2), and (3)
PLL8	PLLTS16FFCLAFRACF	HSDIV0	MAIN_PLL8_REF_CLK	See (1), (2), and (3)
PLL12	PLLTS16FFCLAFRACF	HSDIV0	MAIN_PLL12_REF_CLK	See (1), (2), and (3)
PLL14	PLLTS16FFCLAFRACF	HSDIV0, HSDIV1	MAIN_PLL14_REF_CLK	See (1), (2), and (3)

(1) See Figure 5-171, *Generic PLL Functional Diagram for PLLTS16FFCLAFRACF type* for overview of the PLL.
(2) See Section 5.4.5.5.1 for synthezised clock parameters.
(3) See Section 5.4.5.5.2 for clock output parameters.

5.4.5.5.1 Clock Synthesis Inputs to the PLLs

Table 5-331 lists the clock synthesis parameters for PLLTS16FFCLAFRACF type.

Table 5-469. Clock synthesis Parameters for PLLTS16FFCLAFRACF Type

Parameter Name	Register
FB_DIV	<PLL_name>_FREQ_CTRL0[11-0] FB_DIV_INT (For example, MCU_PLL0 - MCU_PLL0_FREQ_CTRL0 [11-0] FB_DIV_INT)
FB_DIV_FRAC	<PLL_name>_FREQ_CTRL1[23-0] FB_DIV_FRAC (For example, MCU_PLL0 - MCU_PLL0_FREQ_CTRL1[23-0] FB_DIV_FRAC)
POST_DIV2	<PLL_name>_DIV_CTRL[26-24] POST_DIV2 (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[26-24] POST_DIV2)
POST_DIV1	<PLL_name>_DIV_CTRL[18-16] POST_DIV1 (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[18-16] POST_DIV1)
REF_DIV	<PLL_name>_DIV_CTRL[5-0] REF_DIV (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[5-0] REF_DIV)

Note

For PLLTS16FFCLAFRACF type - POST_DIV1 and POST_DIV2 values are from 1 to 7. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2.

5.4.5.5.2 Clock Output Parameter

Table 5-332 lists the control/status bit fields for output clocks.

Table 5-470. Clock Output Parameter for PLLTS16FFCLAFRACF Type

Clock Output/Divider	Parameter Name	Control/Status Bit Field
<PLL_name>_CLKOUT, <PLL_name>_HSDIVj_CLKOUT(1)	Control	<PLL_name>_CTRL[31] BYPASS_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL [31] BYPASS_EN)
<PLL_name>_HSDIVj_CLKOUT(1)	Control	<PLL_name>_HSDIV_CTRLj[15] CLKOUT_EN (For example, MCU_PLL0 - MCU_PLL0_HSDIV_CTRL0[15] CLKOUT_EN and MCU_PLL0_HSDIV_CTRL1[15] CLKOUT_EN)
<PLL_name>_HSDIVj_CLKOUT(1)	Divider control	<PLL_name>_HSDIV_CTRLj[6-0] HSDIV (For example, MCU_PLL0 - MCU_PLL0_HSDIV_CTRL0[6-0] HSDIV and MCU_PLL0_HSDIV_CTRL1[6-0] HSDIV)
PLL bypass mux	Control	<PLL_name>_CTRL[16] BYP_ON_LOCKLOSS (For example, MCU_PLL0 - MCU_PLL0_CTRL [16] BYP_ON_LOCKLOSS)
Enable 4-phase clock generator	Control	<PLL_name>_CTRL[5] CLK_4PH_EN (ignored if <PLL_name>_CTRL[4] CLK_POSTDIV_EN = 0) (For example, MCU_PLL0 - MCU_PLL0_CTRL[5] CLK_4PH_EN)
Post divide CLK enable	Control	<PLL_name>_CTRL[4] CLK_POSTDIV_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[4] CLK_POSTDIV_EN)
Delta-Sigma modulator enable	Control	<PLL_name>_CTRL[1] DSM_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[1] DSM_EN)

Table 5-470. Clock Output Parameter for PLLTS16FFCLAFRACF Type (continued)

Clock Output/Divider	Parameter Name	Control/Status Bit Field
Enable fractional noise canceling DAC	Control	<PLL_name>_CTRL[0] DAC_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[0] DAC_EN)

(1) j is the number of HSDIV for the current PLL.

5.4.5.5.3 Calibration Related Bitfields

Table 5-333 lists the calibration related bitfields/bits.

Table 5-471. Recalibration Feature Parameters

Recalibration feture	Parameter Name	Control/Status Bit Field
Calibration enable to actively adjust for input skew	Control	<PLL_name>_CAL_CTRL[31] CAL_EN (For example, PLL12 - PLL12_CAL_CTRL[31] CAL_EN)
Fast calibration enabled	Control	<PLL_name>_CAL_CTRL[20] FAST_CAL (For example, PLL12 - PLL12_CAL_CTRL[20] FAST_CAL)
Calibration loop programmable counter	Control	<PLL_name>_CAL_CTRL[18-16] CAL_CNT (For example, PLL12 - PLL12_CAL_CTRL[18-16] CAL_CNT)
Calibration bypass	Control	<PLL_name>_CAL_CTRL[15] CAL_BYP (For example, PLL12 - PLL12_CAL_CTRL[15] CAL_BYP)
Calibration input	Control	<PLL_name>_CAL_CTRL[11-0] CAL_IN (For example, PLL12 - PLL12_CAL_CTRL[11-0] CAL_IN)
Output of the calibration block	Status	<PLL_name>_CAL_STAT[11-0] CAL_OUT (For example, PLL12 - PLL12_CAL_STAT[11-0] CAL_OUT)

5.4.5.6 PLL and PLL Controller Connection

Two PLL Controllers are implemented in the device - PLLCTRL0 and MCU_PLLCTRL0. They are respectively related to PLL0 and MCU_PLL0. The PLL Controllers manage the clock ratios, alignment, and gating for the system clocks.

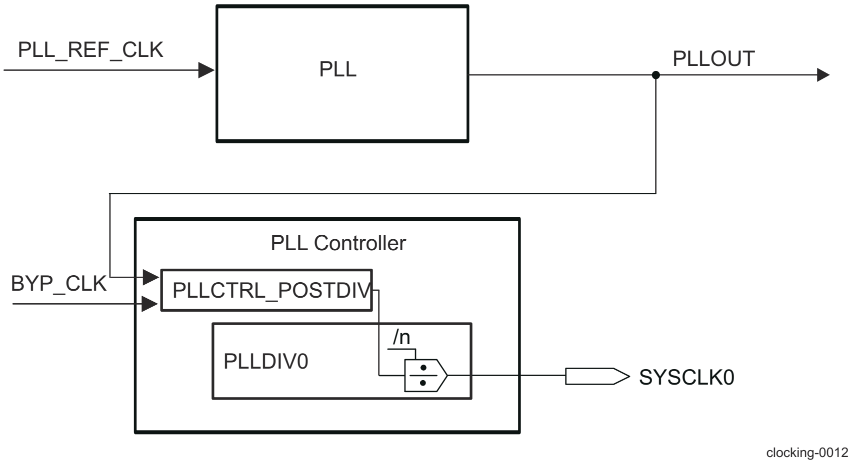

Figure 5-173. PLL and PLL Controller

Note

PLLCTRL_POSTDIV is not supported in this family of devices.

Note

The PLL Controllers registers can be accessed by any controller in the device.

A SYSCLK0 clock out of a PLLCTRL is the only synchronous clock in that domain. That means - MCU_SYSCLK0 out of MCU_PLLCTRL is the synchronous CBASS clock in MCU domain and SYSCLK0 out of Main PLLCTRL is the synchronous CBASS clock in Main domain.

5.4.5.7 PLL, PLLCTRL, and HSDIV Controllers Programming Guide

5.4.5.7.1 PLL Initialization

5.4.5.7.1.1 Kick Protection Mechanism

Note

PLL configuration registers are write-protected at power-up. Software must first un-lock the PLLn_LOCKKEY0 and PLLn_LOCKKEY1 registers prior to writing to any chip-level registers.

The un-lock process shall follow the steps:

1. Write value 0x68EF3490 to PLLn_LOCKKEY0 register.
2. Write value 0xD172BC5A to PLLn_LOCKKEY1 register.

After these two steps a write access to the PLL registers is allowed. Writing any other data value to either of these two registers locks the kicker mechanism and blocks any writes to the PLL registers.

Note

In order to ensure that all PLL registers are write protected, software must always re-lock the kicker mechanism after completing the register writes.

5.4.5.7.1.2 PLL Initialization to PLL Mode

Note

For validated set of parameters that can be programmed to PLLs, please refer to the device-specific Datasheet.

Initially, the device powers up in PLL bypass mode. The bypass mux is a glitch free mux and is located outside the PLL module. BYPASS_EN bit controls the bypass mux section. During Power-up, the bypass mux defaults to select FREF clock (PLL clock bypass mode).

During boot, DMSC0 ROM programs the MCU_PLL0 to a valid frequency based on the crystal frequency and BOOTMODE pin settings. DMSC0 then waits for PLL to be locked by checking the PLL LOCK status bit. DMSC0 ROM programs BYPASS_EN bit to ‘0’ to disable the bypass mode to propagate MCU_PLL0 clock to MCU_PLLCTRL0. At this point DMSC0 brings MCU_M4FSS out of reset to complete the reset of the boot process. M4FSS software configures the remaining PLLs and bring them out of bypass mode.

The following shows the PLL initialization sequence.

1. Wait until supplies are stable and PORz is de-asserted. By this time the reference clock source must be up and running.
2. Default controls settings:

   - By default PLL_EN signal is Low provided by <PLL_name>_CTRL register default state. This signal behaves like a reset control to the PLL.
   - By default INTL_BYP_EN signal is low provided by <PLL_name>_CTRL register default state.
   - By default BYPASS_EN signal is high provided by PLL MMR CTRL default state. PLL clock will be bypassed externally by a glitch free mux. The output of the mux will be the reference clock FREF.
   - LOCK output of PLL will be Low.
3. Program the PLL to a valid setting that runs the VCO within the specified range. The following bits/bitfields must be programmed appropriately by software: DSM_EN, DAC_EN, CLK_POSTDIV_EN, CLK_4PH_EN, REF_DIV[5-0], FB_DIV[11-0], FB_DIV_FRAC[23-0], POST_DIV1[2-0], POST_DIV2[2-0].
4. Wait for 1 µs to allow the PLL internal reset to complete (PLL powerdown switch pulls the loop filter voltage from rail-to-rail, which ensures the PLL will be completely powered down from any state).
5. Assert PLL_EN to a High (by writing a '1' into PLL_EN bit in <PLL_name>_CTRL register).
6. Wait for PLL Lock output to go high. Software can read the LOCK bit in <PLL_name>_STATS register to check if PLL has locked.
7. De-assert BYPASS_EN signal to a Low by writing 0 into BYPASS_EN bit in <PLL_name>_CTRL register.
8. Glitch free mux safely switches to the PLL clock output.

Changing PLL setting: During normal operation, before changing PLL settings, the PLL clock must be bypassed by setting BYPASS_EN control to a high. Then follow steps 2 to 8 from the above sequence.

5.4.5.7.1.3 PLL Programming Requirements

- A PLL VCO frequency must be set to > 1500 MHz
  - For best PLL performance, maximize VCO frequency where possible.
- A PLL must always operate in Fractional Mode (DAC_EN and DSM_EN set to ‘1’). This is true even when the FB_DIV is a integer.
- A PLL Reference clock frequency must be > 10 MHz.
- REF_DIV[5:0] must be set to “000001”.
- FRACF PLLs must always be used with continuous calibration mode turned on. FRACF PLLs must follow the calibration procedure.

5.4.5.7.2 HSDIV PLL Programming

<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 0 cleanly disables the HSDIV output clock

<PLL_Name>_HSDIV_CTRLk[6-0] HSDIV = <value> for divider

<PLL_Name>_HSDIV_CTRLk[8] SYNC_DIS = 0 insures that the divider changes occur synchronously to the internal divider of the HSDIV block.

when the clock is required,

<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 1 cleanly enables the HSDIV output clock

5.4.5.7.3 PLL Controllers Programming - Dividers PLLDIVn and GO Operation

The GO operation is required to change the divider ratios of the PLLDIVn registers. Section 5.4.5.7.3.1 , *GO Operation*, discusses the GO operation. Section 5.4.5.7.3.2 , *Software Steps to Modify PLLDIVn Ratios*, provides the software steps required to change the divider ratios.

5.4.5.7.3.1 GO Operation

The GO operation writes to the RATIO field in the PLLDIVn. Registers do not change the dividers' divide ratios immediately. The PLLDIV dividers change to the new RATIO rates only during a GO operation. This section discusses the GO operation and alignment of the SYSCLKs.

The PLL Controller clock align control register (ALNCTL) determines which SYSCLKs must be aligned. Before a GO operation, program ALNCTL so that the appropriate clocks are aligned during the GO operation.

A GO operation is initiated by setting the GOSET bit in PLLCMD to 1. During a GO operation:

- Any SYSCLK *n* with the corresponding ALN *n* bit in ALNCTL and SYS *n* bit in DCHANGE set to 1 is paused at the low edge. Then the PLL Controller restarts all these SYSCLKs simultaneously, aligned at the rising edge. When the SYSCLKs are restarted, SYSCLK *n* toggles at the rate programmed in the RATIO field in PLLDIVn.
- Any SYSCLK *n* with the corresponding ALN *n* bit in ALNCTL cleared and the SYS *n* bit in DCHANGE set immediately changes to the new rate programmed in the RATIO field.
- The GOSTAT bit in PLLSTAT is set throughout the duration of a GO operation.

CAUTION

To help prevent errors, all device operation must be stopped before the GO operation.

5.4.5.7.3.2 Software Steps to Modify PLLDIV Ratios

Perform the following steps to modify PLLDIV.

1. Check that the GOSTAT bit in PLLSTAT is cleared to show that no GO operation is currently in progress.
2. Program the RATIO field in PLLDIVn to the desired new divide-down rate. If the RATIO field changed, the PLL Controller will flag the change in the corresponding bit of DCHANGE.
3. Set the respective ALN *n* bits in ALNCTL to align any SYSCLKs after the GO operation.
4. Set the GOSET bit in PLLCMD to initiate the GO operation to change the divide values and align the SYSCLKs as programmed.
5. Read the GOSTAT bit in PLLSTAT to make sure the bit returns to 0 to indicate that the GO operation has completed.

5.4.5.7.4 Entire Sequence for Programming PLLCTRL, HSDIV, and PLL

Table 5-334 shows the entire sewuence of programming PLLCTRL, HSDIV, and PLL from an unknown state to a defined non-spread-spectrum state.

Table 5-472. Programming Sequence of PLLCTRL, HSDIV, and PLL

Step	Description
Unlock PLL registers	<PLL_Name>_LOCKKEY0 (= 0x68EF3490)
	<PLL_Name>_LOCKKEY1 (= 0xD172BC5A)
If PLL0	Configure PLLCTRL block into bypass mode
	PLLCTL [0]PLLEN = 0
	PLLCTL[5] PLLENSRC = 0
Configure external bypass so that no transient clock propagates	<PLL_Name>_CTRL[31] BYPASS_EN = 1
Delay	
Disable HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN =0
Delay	
Disable PLL	<PLL_Name>_CTRL[15] PLL_EN =0
Delay	
Reset HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[31] RESET = 1
If PLL0	Check PLLSTAT [0] GOSTAT to make sure that divider change is not currently in-progress GOSTAT should equal 0.
	Clear GOSET bit PLLCMD [0] GOSET = 0
	Configure divider in PLLCTRL to /1 PLLDIV1 = 0x8000 (enable divider and divide by 1) PLLDIV2 = 0x00 (disable divider and divide by 1)
	Set alignment control bits ALNCTL = 3

Table 5-472. Programming Sequence of PLLCTRL, HSDIV, and PLL (continued)

Step	Description
	Set GOSET bit to initiate the divider change PLLCMD [0] GOSET = 1
	Check PLLSTAT [0] GOSTAT to make sure that divider change has completed GOSTAT should equal 0.
Configure HSDIV(s) divider value	<PLL_Name>_HSDIV_CTRLk[6-0] HSDIV (=val)
Clear HSDIV(s) SYNC_DIS	<PLL_Name>_HSDIV_CTRLk[8] SYNC_DIS = 0
Delay	
Clear Reset HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[31] RESET = 0
Configure PLL multiplier	Integer portion of divider <PLL_Name>_FREQ_CTRL0[11-0] (=val) Fractional portion of divider <PLL_Name>_FREQ_CTRL1[23-0] (=val)
Configure PLL dividers	Reference clock divider <PLL_Name>_DIV_CTRL[5-0] REF_DIV = 1
	Post divider 1 <PLL_Name>_DIV_CTRL[18-16] POST_DIV1 = 1
	Post divider 2 <PLL_Name>_DIV_CTRL[26-24] POST_DIV2 = 1
Configure “random” PLL controls	<PLL_Name>_CTRL[8] INTL_BYP_EN = 0
	<PLL_Name>_CTRL[5] CLK_4PH_EN = 0
	<PLL_Name>_DIV_CTRL[26-24] POST_DIV2 = 1
	<PLL_Name>_DIV_CTRL[18-16] POST_DIV1 = 1
	<PLL_Name>_DIV_CTRL[5-0] REF_DIV = 1
	<PLL_Name>_CTRL[1] DSM_EN = 1
	<PLL_Name>_CTRL[0] DAC_EN = 1
	<PLL_Name>_CTRL[4] CLK_POSTDIV_EN – if PLL has more than 5 HSDIV blocks, 1; else 0.
	<PLL_Name>_CTRL[16] BYP_ON_LOCKLOSS (= {0, 1})
Delay	
Enable PLL	<PLL_Name>_CTRL[15] PLL_EN = 1
Wait for Lock	Wait for MCU_PLL0_STAT [0] LOCK = 1
Enable HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 1
Delay	
Configure external bypass to pass PLL	<PLL_Name>_CTRL[31] BYPASS_EN = 0
Delay	
If PLL0	Configure PLLCTRL block into PLL mode PLLCTL [0] PLLEN = 0
Lock PLL registers	<PLL_Name>_LOCKKEY0 (= any value)
	<PLL_Name>_LOCKKEY1 (= any value)

Chapter 6

Processors and Accelerators

This chapter describes the Processor and Accelerator modules in the device.

6.1 Arm Cortex-A53 Subsystem (A53SS)

This section describes the Arm®Cortex®-A53 Subsystem (A53SS) in the device.

Note

This module is not supported by the AM243x family of devices.

6.1.1 A53SS Overview

6.1.1.1 A53SS Introduction

The SoC implements one cluster of dual-core Arm Cortex A53 MPCore, with 32KB L1 instruction, 32KB L1 data, per core and 256KB L2 shared cache.

The Cortex-A53 cores are general-purpose processors that can be used for running customer applications.

Note

Notes on references used in this document:

- A53SS is also referred to as Arm CorePac.
- Cortex-A53 is often shortened to A53.

The A53SS is built around the Cortex-A53 MPCore (Arm A53 Cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus it delivers high performance and optimal power management, debug and emulation capabilities.

The A53 processor is a multi-issue out-of-order superscalar execution engine with integrated L1 Instruction and Data Caches, compatible with Arm®v8-A architecture. It delivers significantly more performance than its predecessors at a higher level of power efficiency.

The Arm®v8-A architecture brings a number of new features. These include 64-bit data processing, extended virtual addressing and 64-bit general purpose registers. The A53 processor is Arm's first Arm®v8-A processor aimed at providing power-efficient 64-bit processing. It features an in-order, 8-stage, dual-issue pipeline, and improved integer, Arm® Neon™, Floating-Point Unit (FPU) and memory performance.

The A53 CPU supports two execution states: AArch32 and AArch64. The AArch64 state gives the A53 CPU its ability to execute 64-bit applications, while the AArch32 state allows the processor to execute existing Arm®v7-A applications.

6.1.1.2 A53SS Features

The A53SS module supports the following features:

- Dual Core A53 Cluster
  - Full Arm®v8-A Architecture Compliant
    - AArch32 and AArch64 Execution States
    - All exception levels EL0-3
    - A32 Instruction Set (Previously Arm instruction set)
    - T32 instruction set (Previously Thumb instruction set)
    - A64 Instruction Set
  - Advanced SIMD and Floating Point Extensions (Arm® Neon™,)
  - Armv8 Cryptography Extensions
  - Arm GICv3 architecture
  - In-order pipeline with symmetric dual-issue of most instructions
  - Harvard L1 with system MMU
    - 32 KB Instruction Cache
    - 32 KB Data Cache
  - 256KB Shared L2 Cache
  - Generic Timer(s)
  - Debug
- 128-Bit VBUSM Initiator Interfaces (for axi_r and axi_r channels)
- 128-Bit VBUSM Target Interface (for Accelerator Coherency Port)
- 64-bit Grey-coded system input time
- 48-bit Grey-coded debug input time
- 48-bit Grey-coded debug input time
- Integrated PBIST controller with BISOR

6.1.2 A53SS Integration

This section describes the A53SS integration in the device, including information about clocks, resets, and hardware requests.

A53SS Integration shows the A53SS integration.

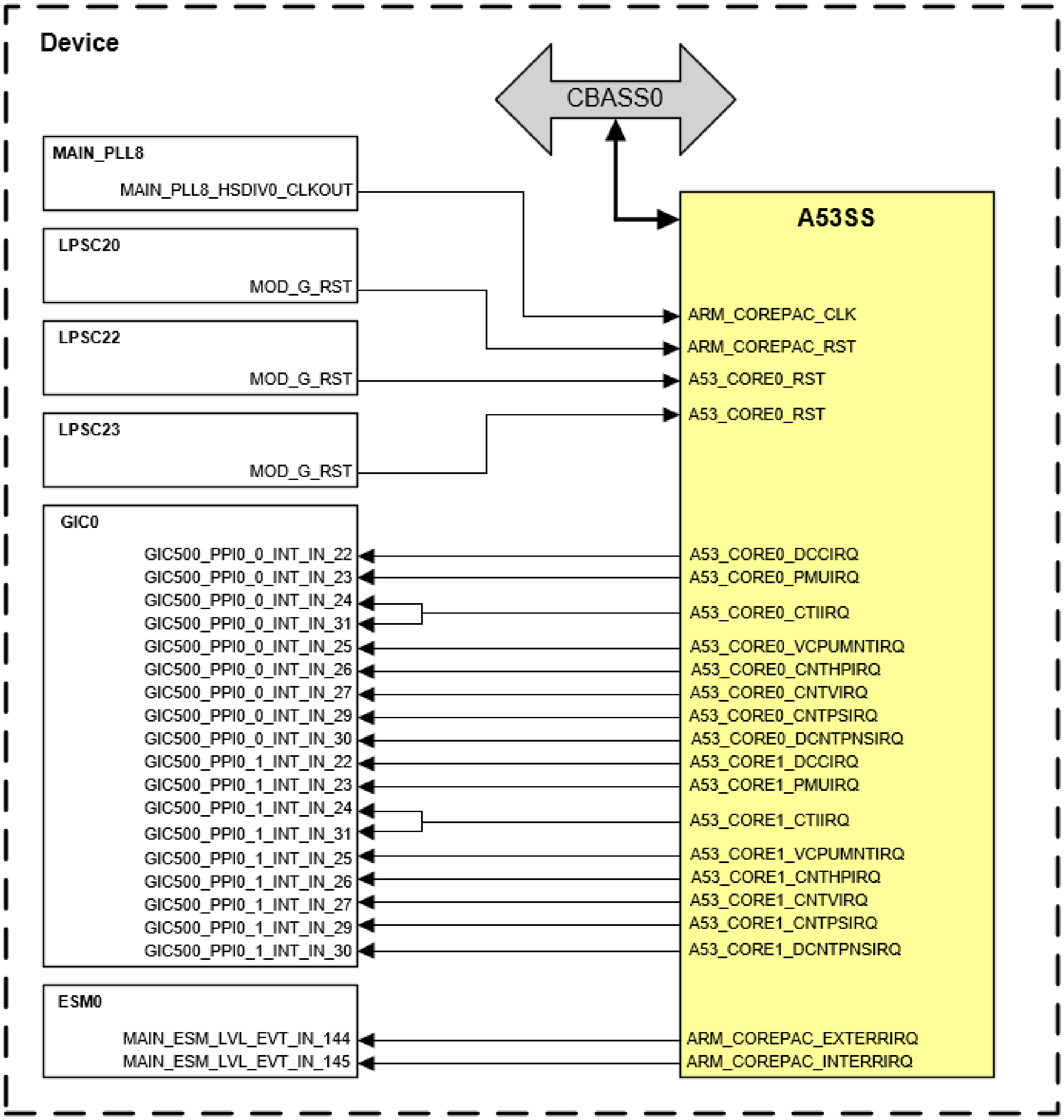

Figure 6-1. A53SS Integration

A53SS Integration Attributes through A53SS Hardware Request summarize the A53SS integration.

Table 6-1. A53SS Integration Attributes

Module Instance	Attributes

Table 6-1. A53SS Integration Attributes (continued)

		Power Sleep Controller	Power Domain	Module Domain	Interconnect
A53SS0	Arm A53 Cluster 0	MAIN_PSC	PD1	LPSC20	CBASS0
	Arm A53 Cluster 0 Core 0	MAIN_PSC	PD2	LPSC22	CBASS0
	Arm A53 Cluster 0 Core 1	MAIN_PSC	PD3	LPSC23	CBASS0

Table 6-2. A53SS Clocks

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
A53SS	ARM_COREPAC_CLK	MAIN_PLL8_HSDIV0_CLKOUT	MAIN_PLL8	A53SS clock

Table 6-3. A53SS Resets

Resets					
Module Instance		**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
A53SS0	Arm A53 Cluster 0	ARM_COREPAC_RST	MOD_G_RST	LPSC20	Arm A53 Cluster 0 reset
	Arm A53 Cluster 0 Core 0	A53_CORE0_RST	MOD_G_RST	LPSC22	Arm A53 Cluster 0 Core 0 reset
	Arm A53 Cluster 0 Core 1	A53_CORE1_RST	MOD_G_RST	LPSC23	Arm A53 Cluster 0 Core 1 reset

Table 6-4. A53SS Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
A53SS0	A53_CORE0_DCCIRQ	GIC500_PPI0_0_INT_IN_22	GIC0	A53 Cluster 0 Core 0 DCC Comms Channel interrupt	Level
	A53_CORE0_PMUIRQ	GIC500_PPI0_0_INT_IN_23	GIC0	A53 Cluster 0 Core 0 PMU Counter Overflow interrupt	Level
	A53_CORE0_CTIIRQ	GIC500_PPI0_0_INT_IN_24 GIC500_PPI0_0_INT_IN_31	GIC0	A53 Cluster 0 Core 0 Cross Trigger Interface interrupt	Level
	A53_CORE0_VCPUMNTIRQ	GIC500_PPI0_0_INT_IN_25	GIC0	A53 Cluster 0 Core 0 Virtual CPU Maintenance interrupt	Level
	A53_CORE0_CNTHPIRQ	GIC500_PPI0_0_INT_IN_26	GIC0	A53 Cluster 0 Core 0 Hypervisor Timer interrupt	Level
	A53_CORE0_CNTVIRQ	GIC500_PPI0_0_INT_IN_27	GIC0	A53 Cluster 0 Core 0 Virtual Timer interrupt	Level
	A53_CORE0_CNTPSIRQ	GIC500_PPI0_0_INT_IN_29	GIC0	A53 Cluster 0 Core 0 Secure Physical Timer interrupt	Level
	A53_CORE0_CNTPNSIRQ	GIC500_PPI0_0_INT_IN_30	GIC0	A53 Cluster 0 Core 0 Non-secure Physical Timer interrupt	Level
	A53_CORE1_DCCIRQ	GIC500_PPI0_1_INT_IN_22	GIC0	A53 Cluster 0 Core 1 DCC Comms Channel interrupt	Level
	A53_CORE1_PMUIRQ	GIC500_PPI0_1_INT_IN_23	GIC0	A53 Cluster 0 Core 1 PMU Counter Overflow interrupt	Level
	A53_CORE1_CTIIRQ	GIC500_PPI0_1_INT_IN_31 GIC500_PPI0_1_INT_IN_24	GIC0	A53 Cluster 0 Core 1 Cross Trigger Interface interrupt	Level
	A53_CORE1_VCPUMNTIRQ	GIC500_PPI0_1_INT_IN_25	GIC0	A53 Cluster 0 Core 1 Virtual CPU Maintenance interrupt	Level

Table 6-4. A53SS Hardware Requests (continued)

	A53_CORE1_CNTHPIRQ	GIC500_PPI0_1_INT_IN_26	GIC0	A53 Cluster 0 Core 1 Hypervisor Timer interrupt	Level
	A53_CORE1_CNTVIRQ	GIC500_PPI0_1_INT_IN_27	GIC0	A53 Cluster 0 Core 1 Virtual Timer interrupt	Level
	A53_CORE1_CNTPSIRQ	GIC500_PPI0_1_INT_IN_29	GIC0	A53 Cluster 0 Core 1 Secure Physical Timer interrupt	Level
	A53_CORE1_CNTPNSIRQ	GIC500_PPI0_1_INT_IN_30	GIC0	A53 Cluster 0 Core 1 Non-secure Physical Timer interrupt	Level
	ARM_COREPAC_EXTERRIRQ	MAIN_ESM_LVL_EVT_IN_144	ESM0	Arm Cluster 0 Cache ECC Error interrupt	Level
	ARM_COREPAC_INTERRIRQ	MAIN_ESM_LVL_EVT_IN_145	ESM0	Arm Cluster 0 Memory Bus Error interrupt	Level

Note

A53SS interrupts are further described in A53SS Interrupt Outputs, *A53SS Interrupt Outputs*

For more information on the interconnects, see *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within *Device Configuration*.

6.1.3 A53SS Functional Description

6.1.3.1 A53SS Block Diagram

Figure 6-2 shows the block diagram of the A53SS.

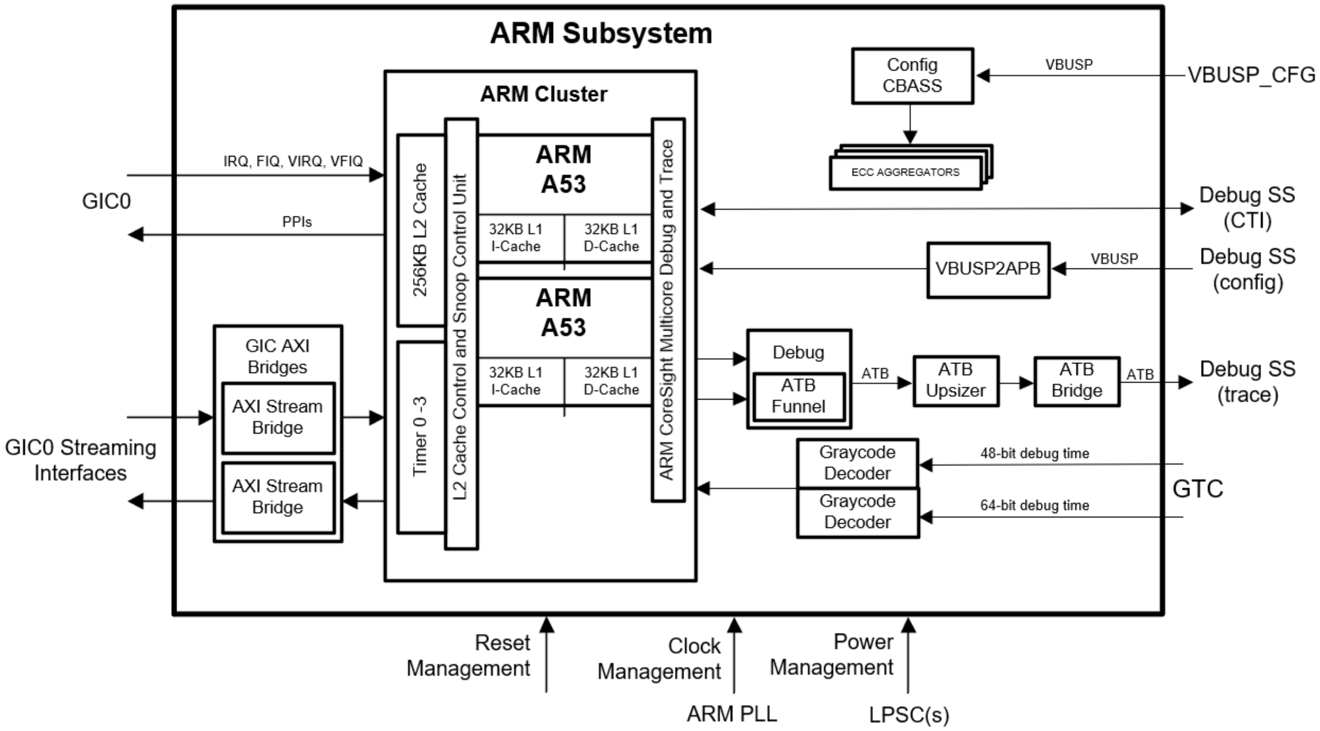

Figure 6-2. A53SS Block Diagram

6.1.3.2 Arm Cortex-A53 Cluster

The Arm Cortex-A53 Cluster is provided by Arm and configured by TI. Table 6-5 summarizes the configuration of the Arm Cortex-A53 Cluster on this SoC.

Table 6-5. Arm A53 Cluster Configuration

Parameter	Value
Core Type	A53
Core Revision	r0p4
Number of Cores	2
Bus Width	256
L1 Instruction Cache Size	32K
L1 Data Cache Size	32K
L2 Cache Size	256K
SCU-L2 Cache Protection	Included
Advanced SIMD and Floating Point Extension	Included
Cryptography Extension	Included
CPU Cache Protection	Included
AMBA5 CHI or AMBA4 ACE Interface	AMBA4 ACE (configured for AXI using tie-offs)
Accelerator Coherency Port (ACP)	Included

Table 6-5. Arm A53 Cluster Configuration (continued)

Parameter	Value
V7 or v8 Debug Memory Map	v8

Note

For a brief list of features supported by the Arm Cortex-A53 Cluster, see A53SS Features.

For detailed description of the Arm A53 Cluster, see the *ARM®Cortex®-A53 MPCore Processor Technical Reference Manual*.

6.1.3.3 A53SS Interfaces and Async Bridges

The A53SS has the following main interfaces:

- 64-bit graycoded system input time
  - Graycode value provided by Global Timebase Counter (GTC)
  - Dedicated decoder (64-bit input) for graycode-to-binary conversion
- 48-bit graycoded debug input time
  - Graycode value provided by GTC
  - Dedicated decoder (48-bit input) for graycode-to-binary conversion
- 32-bit VBUSP target interface for debug
  - Supported by VBUSP2APB Bridge, which performs VBUSP-to-APB conversion (for controlling the Arm A53 Cluster internal debug logic)
- 32-bit ATB output port for debug/trace
  - Supported by ATB Bridge, which performs clock and voltage level conversion on the combined ATB interface
  - Connected to the Debug Subsystem
- Cross Trigger Interface (CTI) for debug
  - Connected to the Debug Subsystem
- Interface(s) with Arm GIC-500 Interrupt Controller
  - Supported by GIC AXI Streaming Bridge, which performs clock and voltage level conversion on the AXI streaming protocol
  - Interrupts (PPIs) from Arm A53 Cluster to GIC-500
  - Interrupts (IRQ, FIQ, VIRQ, VFIQ) from GIC-500 to Arm A53 Cluster
- Power/clock interface(s)
  - Dedicated PLL for each Arm A53 Cluster
  - Dedicated LPSC for each Arm A53 Cluster, and also for each A53 core

6.1.3.4 A53SS Interrupts

6.1.3.4.1 A53SS Interrupt Inputs

The A53 CPU recieves interrupts at its inputs (IRQ, FIQ, VIRQ, VFIQ) via the dedicated Arm GIC-500 Interrupt Controller, which resides at the SoC level (MAIN Domain) and is integrated inside the GIC0 Subsystem. The GIC-500 supports all four A53 cores in the system.

The GIC-500 is compliant to the Arm GICv3 standard and supports four types of interrupts:

- *Software Generated Interrupts (SGI)*
  - There are 16 SGIs (ID0-ID15)
  - These are inter-processor interrupts
- *Private Peripheral Interrupts (PPI)*
  - There are 16 PPIs (ID16-ID31)
  - These are wired interrupts dedicated to a specific CPU
  - Many are reserved to specific functions via convention

- *Shared Peripheral Interrupts (SPIs)*
  - There are 256 SPIs (ID32-ID288)
  - These are wired interrupts that can be routed to any core or cluster, based on the programming of that interrupt in the GIC500
- *Locality-Specific Peripheral Interrupts (LPI)*
  - There are 57,344 LPIs
  - These interrupts are used for message-based interrupts from a peripheral

The mapping of PPIs and SPIs to the GIC-500 interrupt inputs can be found in Interrupt Sources.

Note

For a brief list of features supported by the GIC-500 module, see the *Interrupts* chapter.

For detailed description of the GIC-500 module, see the *Arm® CoreLink™ GIC-500 Generic Interrupt Controller Technical Reference Manual*.

6.1.3.4.2 A53SS Interrupt Outputs

A53SS Interrupt Outputs lists the interrupts generated by the A53SS.

Table 6-6. A53SS Interrupt Outputs

Interrupt Name (TI)(1)	Interrupt Name (Arm)	Interrupt Description
A53 Core Interrupts (PPIs)(2)		
A53_COREy_VCPUMNTIRQ	VCPUMNTIRQn	This interrupt indicates that a Virtual CPU Interface on the corresponding core needs serviced. This interrupt is serviced by software switching to the virtual CPU and finding what specific service needs done.
A53_COREy_CNTHPIRQ	CNTHPIRQn	This interrupt indicates a physical timer event at the EL2 (Hypervisor) exception level. Service of this interrupt is dependent on what the timer was set for. Software should take exception to EL2 and service accordingly.
A53_COREy_CNTPNSIRQ	CNTPNSIRQn	This interrupt indicates a physical timer event at the EL1 Non-Secure exception level. Service of this interrupt is dependent on what the timer was set for. Software should take exception to EL1 Non-Secure and service accordingly.
A53_COREy_CNTPSIRQ	CNTPSIRQn	This interrupt indicates a physical timer event at the EL1 Secure exception level. Service of this interrupt is dependent on what the timer was set for. Software should take exception to EL1 Secure and service accordingly.
A53_COREy_CNTVIRQ	CNTVIRQn	This interrupt indicates a Virtual timer event. Service of this interrupt is dependent on what the timer was set for. Software should take exception and service accordingly.
A53_COREy_PMUIRQ	PMUIRQn	This interrupt is generated by the Performance Monitor Unit (PMU). The PMU can generate an interrupt based on several conditions, depending on programming. Software should take exception and query the PMU as to the cause of the interrupt, and act accordingly.
A53_COREy_DCCIRQ	COMMIRQn	Communications Channel receive or transmit interrupt
A53_COREy_CTIIRQ	CTIIRQn	Cross Trigger Interface interrupt

(1) In this column, *y* is the A53 Core index (0 or 1)

(2) These are 'per core' interrupts

Note

The mapping of these interrupts in the system is summarized in A53SS Integration, and can also be found in *Interrupts*.

For more detailed description of these interrupts and their handling, see the *Arm® Cortex®-A53 MPCore Processor Technical Reference Manual*.

6.1.3.5 A53SS Power Management and Clocking

6.1.3.5.1 A53SS Power Management

Each Arm A53 Cluster and each A53 CPU reside in a separate power domain, as follows:

- PD2 (PD_A53_0): Power Domain of Arm A53 Cluster 0 Core 0
- PD3 (PD_A53_1): Power Domain of Arm A53 Cluster 0 Core 1
- PD1 (PD_A53_CLUSTER_0): Power Domain of Arm A53 Cluster 0

There is a dedicated Local Power Sleep Controller (LPSC) for each Arm A53 Cluster, and for each A53 core, as well. The LPSC assignment is as follows:

- LPSC22 (LPSC_A53_0): Dedicated for Arm A53 Cluster 0 Core 0
- LPSC23 (LPSC_A53_1): Dedicated for Arm A53 Cluster 0 Core 1
- LPSC20 (LPSC_A53_CLUSTER_0): Dedicated for Arm A53 Cluster 0

For more details on these LPSCs, including power-up/down sequences, see *Power*.

6.1.3.5.2 A53SS Clocking

There is a dedicated PLL for each Arm A53 Cluster. The PLL assignment is as follows:

- PLL8 (ARM0 PLL): Dedicated for Arm A53 Cluster 0

For more details on these PLLs, see *Clocking*.

6.1.3.6 A53SS Debug

The A53SS supports the standard Arm debug architecture. Details on Arm debug can be found in the *On-chip Debug* chapter and the relevant Arm specifications.

6.1.3.7 A53SS Global and Debug Timestamps

The A53SS has two timebase input interfaces:

- 64-bit global timestamp: Used for synchronizing the Arm internal timers (via the ARM CNTVALUEB [63:0] bus)
- 48-bit debug timestamp: Can be embedded in Arm trace streams at periodic and strategic locations, allowing the temporal relationship of different trace sources to be determined

Both of them are fed by the Global Timebase Counter (GTC), which provides a 64-bit graycode value.
The A53SS includes two graycode decoders (for global time and debug time, respectively), which take the asynchronous graycoded times, synchronize them to the appropriate clock, and convert them to binary time, as required by Arm.

Note

Both graycode decoders are 64-bit but the one dedicated to debug time has a 48-bit input (the upper 16 bits are tied to 0).

For more details on the GTC, see *Global Timebase Counter (GTC)*.

6.1.3.8 A53SS Watchdog

The A53SS does not have an integrated watchdog timer. Instead, this feature is provided externally by the Real Time Interrupt Module (RTI) module, which implements a windowed watchdog timer capable of issuing warm reset to the SoC, when necessary.

There are two RTI modules in the MAIN Domain, which are assigned to the A53 cores as follows:

- RTI0 is dedicated to the first A53 CPU core in the A53 cluster (A53SS0_CORE0)
- RTI1 is dedicated to the second A53 CPU core in the A53 cluster (A53SS0_CORE1)

For more details on the RTI windowed watchdog feature, see Section 12.5.2 , *Real Time Interrupt Module (RTI/WWDT)*.

6.1.3.9 A53SS Functional Safety - ECC Error Injection Support

In the dual A53 CBA subsystem, there are three ECC aggregators – one for each core and one for the corepac level. Debug domain is not safety critical.

No CBASS/Bridge interconnect safety is supported. Only RAM safety is supported.

The following A53SS ECC Aggregator instances are instantiated:

- A53SS0_ECC_AGGR0: ECC Aggregator for Arm A53 Cluster 0, Core 0
- A53SS0_ECC_AGGR1: ECC Aggregator for Arm A53 Cluster 0, Core 1
- A53SS0_ECC_AGGR_COREPAC: ECC Aggregator for Arm A53 Cluster 0

6.1.3.9.1 A53 ECC Aggregators During Low Power States

- When a cpu core is in WFI/WFE, the corresponding core ECC Aggregator MMR regions is not accessible and will return error status.
- Similarly when L2 is in WFI, the corepac ECC Aggregator MMR region is not accessible and will return error status.

6.1.3.9.2 Auto-initialization of Memories

All A53 L1 and L2 memory initialization is handled by the Arm core. The TI ECC aggregator is used in inject-only mode and this cannot be used for initialization. The Arm CPU will initialize the cache memories after reset.

There are no other memories in the A53 subsystem beside the cache memories

6.1.3.9.3 A53 SRAM Safety

The Arm A53 Cluster natively supports ECC/parity protection on A53 SRAMs and error injection on few memories. The A53SS adds error injection capability on all internal SRAM. This is a valuable TI addition to the Arm native implementation.

Table 6-7. A53 SRAM Safety Support

RAM	A53 Error Injection Support	TI Error Injection Support
L1 I-Cache Data	No	Single error injection
L1 I-Cache Tag	No	Single error injection
L1 D-Cache Data	Double error injection	Single and double error injection
L1 D-Cache Tag	No	Single error injection
L1 Data Dirty	No	Single error injection
TLB RAM	No	Single error injection
SCU Duplicate Tag	No	Single and double error injection
L2 Tag RAM	Double error injection	Single and double error injection
L2 Data RAM	Double error injection	Single and double error injection

The ECC Aggregator for the cores stimulates errors in the following RAMs:

- L1 I-Cache Data RAM

- L1 I-Cache Tag RAM
- L1 D-Cache Data RAM
- L1 D-Cache Tag RAM
- L1 D-Cache Dirty RAM
- TLB RAM
- L1 SCU L1-D Duplicate Tag RAM

The ECC Aggregator for the L2 cache stimulates errors in the following RAMs:

- L2 Data RAM
- L2 Tag RAM

6.1.3.9.4 A53 SRAM ECC Aggregator Configurations

There are several schemas of memory protection employed inside of the processors. The tables below describe the schema and arrangement. This describes what bits are protected, how they are protected, the behavior when an error is detected and what bits can be disturbed for ECC testing purposes. This also lists the RAMID associated with each memory to the corresponding ECC Aggregator.

The key for the protection schemes is as follows:

- Parity – Parity Bit(s) to protect data
- ECC – Error Correction Code to protect Data
- SED – Single Error Detection
- SECDED – Single Error Correction, Double Error Detection
- SEDSEC – Single Error Detection, Single Error Correction

Table 6-8. CPU Memories Safety Details

Memory	Protection	RAM Arrangement	CPU (Core ECC Aggr) Rams Ram ID	Notes
L1 I-Cache Data	Parity SED	41 – Parity for 40:21 40:21 – Instruction 20 – Parity for 19:0 19:0 – Instruction	0-3	Error detection results in both lines being invalidated then refetched from L2 or memory
L1 I-Cache Tag	Parity SED	31 – Parity for 30:0 30:0 – Data	4-5	Error detection results in both lines being invalidated, then line refetched from L2 or memory
L1 D-cache Data	ECC SECDED	38:32 – ECC 31:0 – Data	6-13	Error results in line being cleaned and invalidated from L1 with single bit errors corrected as part of eviction. Line refetched from L2 or memory
L1 D-Cache Tag	Parity SED	30 – Parity for 29:0 29:0 – Tag	14-17	Cache sizes makes LSB unnecessary (always 0) so they are removed from the actual RAM. Error results in line cleaned and invalidated from L1. SCU duplicate tags are used to get the correct address. Line refetched from L2 or memory
L1 D-cache Dirty	Parity SEDSEC	11:10 – Way 1/3 Dirty copy 2 and 1. Parity for 4 9:8 – Way 0/2 Dirty copy 2 and 1. Parity for 0 7 – Way 1/3 Outer Allocation Hint 6 – Way 1/3 Age 5:4 – Way 1/3 Partial MOESI 3 – Way 0/2 Outer Allocation Hint 2 – Way 0/2 Age 1:0 – Way 0/2 Partial MOESI	18	Error results in line cleaned and invalidated from L1 with single bit errors corrected as part of the eviction. Only dirty bit is protected. Other bits are just performance hints

Table 6-8. CPU Memories Safety Details (continued)

Memory	Protection	RAM Arrangement	CPU (Core ECC Aggr) Rams Ram ID	Notes
TLB	Parity SED	116 – parity for 113:62 115 – Parity for 61:31 114 – Parity for 30:0 113:62 – Page Attributes 61:31 – Entry Identifiers 30:0 – Address	19-22	Error detection results in entry invalidated, new pagewalk to refetch.
SCU L1 Duplicate Tag	ECC SECDED	37:31 - ECC for 30:0 30:0 - Duplicate Tag	23-26 (accessed by each Core's ecc_aggr)	Cache sizes makes LSB unnecessary (always 0) so they are removed from the actual RAM. Corretable Error – Tag rewritten with correct value, access retried Uncorrectable Error – Tag is invalidated

Table 6-9. L2 Memories Safety Details

Memory	Protection	RAM Arrangement	RAM_ID (L2 Cache RAMs)	Notes
L2 Tag	ECC SECDED	37:31 – ECC for 30:0 30:0 - Tag	0-15	Cache sizes makes LSB unnecessary (always 0) so they are removed from the actual RAM. Corretable Error – Tag rewritten with correct value, access retried. Uncorrectable Error – Tag is invalidated
L2 Victim	None	–	–	Performance Hint Only – Error has no functional impact
L2 Data	ECC SECDED	71:64 – ECC for 63:0 63:0 – Data	16-23	Error results in Data corrected inline, access may stall for 1-2 cycles. After correction, line might be evicted
Branch Predictor	None	–	–	Performance Hint Only – Error has no functional impact

6.1.3.10 A53SS Boot

For A53SS boot sequence and any other A53SS boot details, see *Control Module (CTRL_MMR)*.

6.1.3.11 A53SS Interprocessor Communication

The Arm A53 core(s) can communicate with other device cores (R5FSS, PRU_ICSSG PRU, DMSC-L M3) by supporting interrupt generation to and from these cores. The interprocessor communication (IPC) interrupts are assigned in the corresponding BOOTCFG0 memory-mapped registers (MMRs) called IPC_SETx / IPC_CLRx. For more information, see Section 5.1 , *Control Module (CTRL_MMR)*.

6.2 Arm Cortex R5F Subsystem (R5FSS)

This chapter describes the Arm Cortex R5F real-time microcontroller unit subsystem (R5FSS) in the device.

6.2.1 R5FSS Overview

The R5FSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for split or single-core operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm CoreSight™ debug and trace architecture, integrated vectored interrupt manager (VIM), ECC aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

> **Note**
>
> The Cortex-R5F processor is a Cortex-R5 processor that includes the optional floating point unit (FPU) extension. In this TRM, all references to the Cortex-R5 processor apply to the Cortex-R5F processor by default.

There are two R5FSS subsystems in the device. Table 6-10 shows R5FSS allocation across device domains.

Table 6-10. R5FSS Allocation Across Device Domains

Module Instance	Domain	
	MCU	MAIN
R5FSS0	–	✓
R5FSS1	–	✓

6.2.1.1 R5FSS Features

Each R5FSS supports the following features:

- Dual-core Arm Cortex-R5F
  - Core revision: r1p3
  - Armv7-R profile
  - Boot-time configurable to be in single- or dual-core (split) mode
    - Dual-core mode: Two independently operating cores (asymmetric multi processing, no coherence)
    - Single-core mode: Only one operating core (CPU0)
      - CPU0 uses TCM resources of both cores
      - CPU1 caches and interrupts are unused in this mode
  - L1 memory system
    - 32KB instruction cache
      - 4x8KB ways
      - SECDED ECC protected per 64 bits
    - 32KB data cache
      - 4x8KB ways
      - SECDED ECC protected per 32 bits
    - 64KB tightly-coupled memory (TCM) per CPU
      - SECDED ECC protected per 32 bits
      - TCM hard error cache Implemented in CPU
      - Readable/writable from system
      - TCMs initialized (to 0's) at reset
      - Split into A and B banks (with B further splitting into B0 and B1 interleaved banks)
        - 32KB TCMA (ATCM)
        - 16KB TCMB0 (B0TCM)
        - 16KB TCMB1 (B1TCM)
      - In dual-core mode, TCM is 64KB in total (per core):
        - 32KB TCMA
        - 16KB TCMB0 + 16KB TCMB1
      - In single-core mode, TCM is 128KB in total (per core):
        - 64KB TCMA
        - 32KB TCMB0 + 32KB TCMB1

  - Low interrupt latency with restartable instructions
  - Non-maskable interrupt (NMI)
  - Full-precision floating point (VFPv3)
  - 16 region memory protection unit (MPU)
  - 8 breakpoints
  - 8 watchpoints
  - Dynamic branch prediction with global history buffer and 4-entry return stack
  - CoreSight debug access port (DAP)
  - CoreSight embedded trace macrocell (ETM-R5) interface
  - Performance monitoring unit (PMU)
- Interfaces
  - 64-bit VBUSM initiator pair (1 read, 1 write) for L3 memory accesses (per core)
  - 64-bit VBUSM target for TCM access (per core)
    - Also allows access to cache for debug purposes
  - 32-bit VBUSP initiator for peripheral access (per core)
  - 32-bit VBUSP target configuration port (per core)
  - 32-bit VBUSP target debug port
    - Allows access to all R5FSS internal debug logic
- Synchronous clock domain crossing on all interfaces
  - Both CPU and interface clocks run at the same frequency (1:1 ratio)
- 32-bit to 36-bit region-based address translation (RAT) on memory access initiators
  - 4 regions
    - Base address + size
    - Must be size aligned
- Integrated vectored interrupt manager (VIM)
  - 256 interrupts per core
    - Only interrupts connected to R5F core 0 are available in single-core mode
    - Each interrupt programmable as either IRQ or FIQ
    - Each interrupt has a programmable enable mask
    - Each interrupt has a programmable 4-bit priority
  - Priority interrupt supported
  - Vectored interrupt interface
    - Compatible with R5F VIC port
    - Programmable 32-bit vector address per interrupt
      - Address is SECDED error protected
      - Default vector addresses provided on DED
    - Split or single-core capable
    - Software interrupt generation
- Integrated ECC aggregators
  - Support for error injection to all supported ECC memory blocks to test ECC functionality (add-on function from TI)
  - One ECC aggregator per core to cover all RAMs and caches associated with that core
- Standard Arm CoreSight debug and trace architecture at the R5FSS level
  - Cross triggering: Supported by cross trigger interface (CTI) (per CPU) and cross trigger matrix (CTM) components
  - Processor trace: Supported by embedded trace macrocell (ETM) (per CPU) and advanced trace bus (ATB) funnel components
- Boot
  - From ROM or external memory
  - From TCM

See Section 6.2.3 for a functional block diagram and more details on the R5FSS.

6.2.1.2 R5FSS Not Supported Features

The R5FSS does *not* support the following native R5F features in this device:

- ACP port (no coherence)
- Bus parity / ECC
- Multiple power domains

6.2.2 R5FSS Integration

This section describes the R5FSS integration in the device, including information about clocks, resets, and hardware requests.

6.2.2.1 R5FSS Integration in MAIN Domain

There are two R5FSS subsystems integrated in the device MAIN domain - R5FSS0 and R5FSS1. Figure 6-3 and Figure 6-4 show the integration of R5FSS0 and R5FSS1, respectively.

Table 6-14 describes which R5F is available in each configuration of cores.

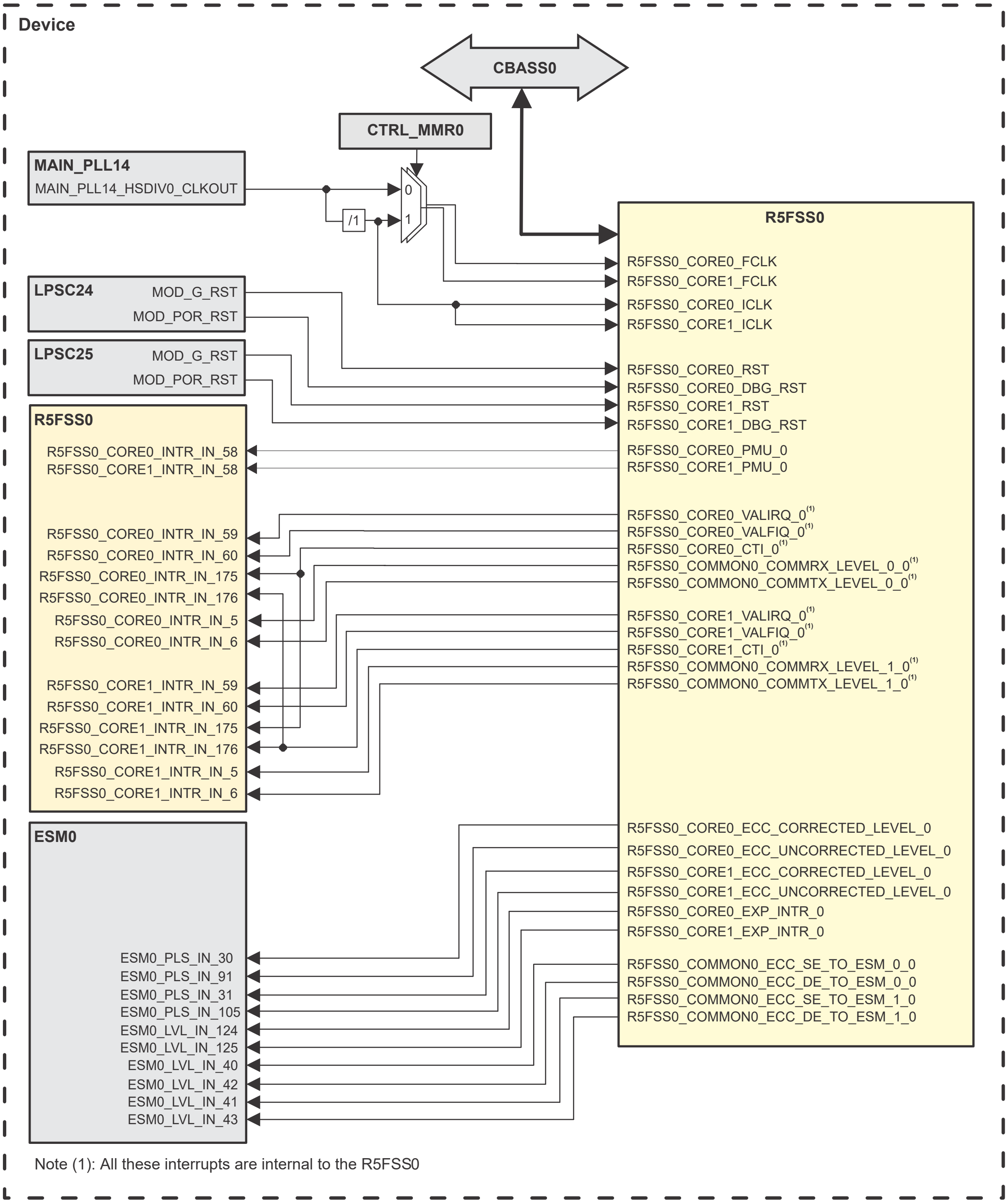

Note (1): All these interrupts are internal to the R5FSS0

Figure 6-3. R5FSS0 Integration

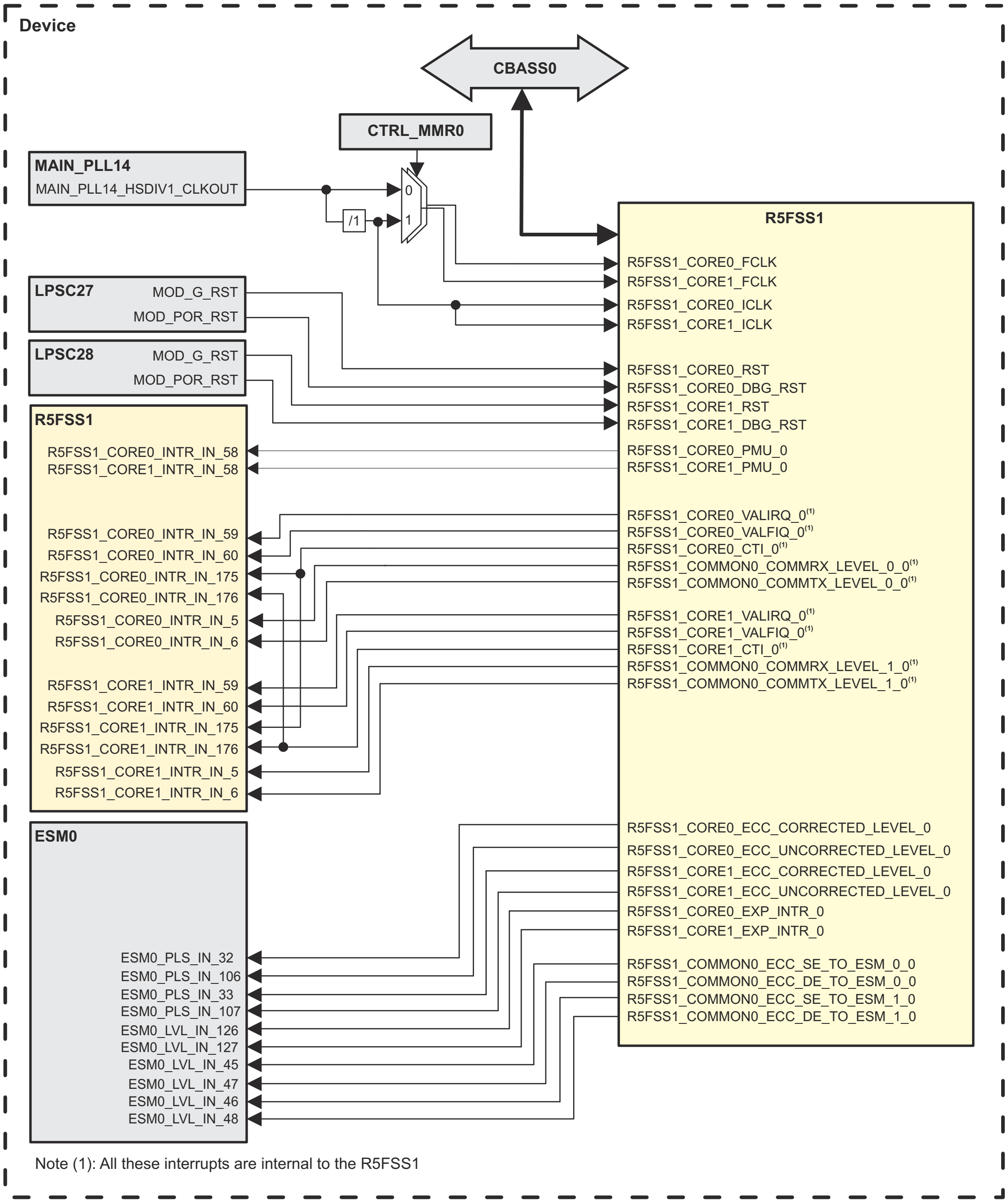

Figure 6-4. R5FSS1 Integration

Table 6-11. R5FSS0/1 Integration Attributes

Module Instance		Attributes			
		Power Sleep Controller	Power Domain	Module Domain	Interconnect
R5FSS0	R5FSS0_CORE0	PSC0	PD4	LPSC24	MCU_CBASS0
	R5FSS0_CORE1	PSC0	PD4	LPSC25	MCU_CBASS0
R5FSS1	R5FSS1_CORE0	PSC0	PD5	LPSC27	MCU_CBASS0
	R5FSS1_CORE1	PSC0	PD5	LPSC28	MCU_CBASS0

Table 6-12. R5FSS0/1 Clocks and Resets

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
R5FSS0	R5FSS0_CORE0_FCLK	MAIN_PLL14_HSDIV0_CLKOUT	MAIN_PLL14	R5FSS0_CORE0 functional clock
	R5FSS0_CORE0_ICLK	MAIN_PLL14_HSDIV0_CLKOUT/4	MAIN_PLL14	R5FSS0_CORE0 interface clock
	R5FSS0_CORE1_FCLK	MAIN_PLL14_HSDIV0_CLKOUT	MAIN_PLL14	R5FSS0_CORE1 functional clock
	R5FSS0_CORE1_ICLK	MAIN_PLL14_HSDIV0_CLKOUT/4	MAIN_PLL14	R5FSS0_CORE1 interface clock
R5FSS1	R5FSS1_CORE0_FCLK	MAIN_PLL14_HSDIV1_CLKOUT	MAIN_PLL14	R5FSS1_CORE0 functional clock
	R5FSS1_CORE0_ICLK	MAIN_PLL14_HSDIV1_CLKOUT/4	MAIN_PLL14	R5FSS1_CORE0 interface clock
	R5FSS1_CORE1_FCLK	MAIN_PLL14_HSDIV1_CLKOUT	MAIN_PLL14	R5FSS1_CORE1 functional clock
	R5FSS1_CORE1_ICLK	MAIN_PLL14_HSDIV1_CLKOUT/4	MAIN_PLL14	R5FSS1_CORE1 interface clock
Resets				
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
R5FSS0	R5FSS0_CORE0_RST	MOD_G_RST	LPSC24	R5FSS0_CORE0 main reset
	R5FSS0_CORE0_DBG_RST	MOD_DBG_POR_RST	LPSC24	R5FSS0_CORE0 debug reset (APB excluded)
	R5FSS0_CORE1_RST	MOD_G_RST	LPSC25	R5FSS0_CORE1 main reset
	R5FSS0_CORE1_DBG_RST	MOD_POR_RST	LPSC25	R5FSS0_CORE1 debug reset (APB excluded)
R5FSS1	R5FSS1_CORE0_RST	MOD_G_RST	LPSC27	R5FSS1_CORE0 main reset
	R5FSS1_CORE0_DBG_RST	MOD_POR_RST	LPSC27	R5FSS1_CORE0 debug reset (APB excluded)
	R5FSS1_CORE1_RST	MOD_G_RST	LPSC28	R5FSS1_CORE1 main reset
	R5FSS1_CORE1_DBG_RST	MOD_POR_RST	LPSC28	R5FSS1_CORE1 debug reset (APB excluded)

Table 6-13. R5FSS0/1 Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
R5FSS0		**R5FSS0_CORE0 interrupts**			
	R5FSS0_CORE0_PMU_0	R5FSS0_CORE0_INTR_IN_58	R5FSS0_CORE0	R5FSS0_CORE0 performance monitor interrupt	Level
	R5FSS0_CORE0_VALFIQ_0	R5FSS0_CORE0_INTR_IN_59	R5FSS0_CORE0	R5FSS0_CORE0 validation IRQ interrupt	Level
	R5FSS0_CORE0_VALIRQ_0	R5FSS0_CORE0_INTR_IN_60	R5FSS0_CORE0	R5FSS0_CORE0 validation FIQ interrupt	Level
	R5FSS0_CORE0_CTI_0	R5FSS0_CORE0_INTR_IN_175	R5FSS0_CORE0	R5FSS0_CORE0 cross trigger interrupt	Level
		R5FSS0_CORE1_INTR_IN_175	R5FSS0_CORE1		
	R5FSS0_COMMON0_COMMRX_LEVEL_0_0	R5FSS0_CORE0_INTR_IN_5	R5FSS0_CORE0	R5FSS0_CORE0 DTRRX full interrupt	Level
	R5FSS0_COMMON0_COMMTX_LEVEL_0_0	R5FSS0_CORE0_INTR_IN_6	R5FSS0_CORE0	R5FSS0_CORE0 DTRTX empty interrupt	Level

Table 6-13. R5FSS0/1 Hardware Requests (continued)

	R5FSS0_CORE0_ECC_CORRECTED_LEVEL_0	ESM0_LVL_IN_30	ESM0	R5FSS0_CORE0 SEC ECC interrupt	Level
	R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_0	ESM0_LVL_IN_91	ESM0	R5FSS0_CORE0 DED ECC interrupt	Level
	R5FSS0_CORE0_EXP_INTR_0	R5FSS0_CORE0_INTR_IN_4	R5FSS0_CORE0	R5FSS0_CORE0 RAT exception interrupt	Level
		ESM0_LVL_IN_124	ESM0		
	R5FSS0_COMMON0_ECC_DE_TO_ESM_0_0	ESM0_LVL_IN_40	ESM0	R5FSS0_CORE0 ECC single-bit error interrupt (cache and TCM RAMs)	Level
	R5FSS0_COMMON0_ECC_SE_TO_ESM_0_0	ESM0_LVL_IN_42	ESM0	R5FSS0_CORE0 ECC double-bit error interrupt (cache and TCM RAMs)	Level
	R5FSS0_CORE1 interrupts				
	R5FSS0_CORE1_PMU_0	R5FSS0_CORE1_INTR_IN_58	R5FSS0_CORE1	R5FSS0_CORE1 performance monitor interrupt	Level
	R5FSS0_CORE1_VALFIQ_0	R5FSS0_CORE1_INTR_IN_59	R5FSS0_CORE1	R5FSS0_CORE1 validation IRQ interrupt	Level
	R5FSS0_CORE1_VALIRQ_0	R5FSS0_CORE1_INTR_IN_60	R5FSS0_CORE1	R5FSS0_CORE1 validation FIQ interrupt	Level
	R5FSS0_CORE1_CTI_0	R5FSS0_CORE0_INTR_IN_176	R5FSS0_CORE0	R5FSS0_CORE1 cross trigger interrupt	Level
		R5FSS0_CORE1_INTR_IN_176	R5FSS0_CORE1		
	R5FSS0_COMMON0_COMMRX_LEVEL_1_0	R5FSS0_CORE1_INTR_IN_5	R5FSS0_CORE1	R5FSS0_CORE1 DTRRX full interrupt	Level
	R5FSS0_COMMON0_COMMTX_LEVEL_1_0	R5FSS0_CORE1_INTR_IN_6	R5FSS0_CORE1	R5FSS0_CORE1 DTRTX empty interrupt	Level
	R5FSS0_CORE1_ECC_CORRECTED_LEVEL_0	ESM0_LVL_IN_31	ESM0	R5FSS0_CORE1 SEC ECC interrupt	Level
	R5FSS0_CORE1_ECC_UNCORRECTED_LEVEL_0	ESM0_LVL_IN_105	ESM0	R5FSS0_CORE1 DED ECC interrupt	Level
	R5FSS0_CORE1_EXP_INTR_0	R5FSS0_CORE1_INTR_IN_4	R5FSS0_CORE0	R5FSS0_CORE1 RAT exception interrupt	Level
		ESM0_LVL_IN_125	ESM0		
	R5FSS0_COMMON0_ECC_DE_TO_ESM_1_0	ESM0_LVL_IN_41	ESM0	R5FSS0_CORE1 ECC single-bit error interrupt (cache and TCM RAMs)	Level
	R5FSS0_COMMON0_ECC_SE_TO_ESM_1_0	ESM0_LVL_IN_43	ESM0	R5FSS0_CORE1 ECC double-bit error interrupt (cache and TCM RAMs)	Level
R5FSS1	**R5FSS1_CORE0 interrupts**				
	R5FSS1_CORE0_PMU_0	R5FSS1_CORE0_INTR_IN_58	R5FSS1_CORE0	R5FSS1_CORE0 performance monitor interrupt	Level
	R5FSS1_CORE0_VALFIQ_0	R5FSS1_CORE0_INTR_IN_59	R5FSS1_CORE0	R5FSS1_CORE0 validation IRQ interrupt	Level
	R5FSS1_CORE0_VALIRQ_0	R5FSS1_CORE0_INTR_IN_60	R5FSS1_CORE0	R5FSS1_CORE0 validation FIQ interrupt	Level
	R5FSS1_CORE0_CTI_0	R5FSS1_CORE0_INTR_IN_175	R5FSS1_CORE0	R5FSS1_CORE0 cross trigger interrupt	Level
		R5FSS1_CORE1_INTR_IN_175	R5FSS1_CORE1		
	R5FSS1_COMMON0_COMMRX_LEVEL_0_0	R5FSS1_CORE0_INTR_IN_5	R5FSS1_CORE0	R5FSS1_CORE0 DTRRX full interrupt	Level

Table 6-13. R5FSS0/1 Hardware Requests (continued)

R5FSS1_COMMON0_COMMTX_LEVEL_0_0	R5FSS1_CORE0_INTR_IN_6	R5FSS1_CORE0	R5FSS1_CORE0 DTRTX empty interrupt	Level
R5FSS1_CORE0_ECC_CORRECTED_LEVEL_0	ESM0_LVL_IN_32	ESM0	R5FSS1_CORE0 SEC ECC interrupt	Level
R5FSS1_CORE0_ECC_UNCORRECTED_LEVEL_0	ESM0_LVL_IN_106	ESM0	R5FSS1_CORE0 DED ECC interrupt	Level
R5FSS1_CORE0_EXP_INTR_0	R5FSS1_CORE0_INTR_IN_4	R5FSS1_VIM0	R5FSS1_CORE0 RAT exception interrupt	Level
	ESM0_LVL_IN_126	ESM0		
R5FSS1_COMMON0_ECC_DE_TO_ESM_0_0	ESM0_LVL_IN_45	ESM0	R5FSS0_CORE1 ECC single-bit error interrupt (cache and TCM RAMs)	Level
R5FSS1_COMMON0_ECC_SE_TO_ESM_0_0	ESM0_LVL_IN_47	ESM0	R5FSS0_CORE1 ECC double-bit error interrupt (cache and TCM RAMs)	Level
R5FSS1_CORE1 interrupts				
R5FSS1_CORE1_PMU_0	R5FSS1_CORE1_INTR_IN_58	R5FSS1_CORE1	R5FSS1_CORE1 performance monitor interrupt	Level
R5FSS1_CORE1_VALFIQ_0	R5FSS1_CORE1_INTR_IN_59	R5FSS0_CORE1	R5FSS1_CORE1 validation IRQ interrupt	Level
R5FSS1_CORE1_VALIRQ_0	R5FSS1_CORE1_INTR_IN_60	R5FSS0_CORE1	R5FSS1_CORE1 validation FIQ interrupt	Level
R5FSS1_CORE1_CTI_0	R5FSS1_CORE0_INTR_IN_176	R5FSS0_CORE0	R5FSS1_CORE1 cross trigger interrupt	Level
	R5FSS1_CORE1_INTR_IN_176	R5FSS0_CORE1		
R5FSS1_COMMON0_COMMRX_LEVEL_1_0	R5FSS1_CORE1_INTR_IN_5	R5FSS0_CORE1	R5FSS1_CORE1 DTRRX full interrupt	Level
R5FSS1_COMMON0_COMMTX_LEVEL_1_0	R5FSS1_CORE1_INTR_IN_6	R5FSS0_CORE1	R5FSS1_CORE1 DTRTX empty interrupt	Level
R5FSS1_CORE1_ECC_CORRECTED_PULSE_0	ESM0_LVL_IN_33	ESM0	R5FSS1_CORE1 SEC ECC interrupt	Level
R5FSS1_CORE1_ECC_UNCORRECTED_PULSE_0	ESM0_LVL_IN_107	ESM0	R5FSS1_CORE1 DED ECC interrupt	Level
R5FSS1_CORE1_EXP_INTR_0	R5FSS1_CORE1_INTR_IN_4	R5FSS1_VIM0	R5FSS1_CORE1 RAT exception interrupt	Level
	ESM0_LVL_IN_127	ESM0		
R5FSS1_COMMON0_ECC_DE_TO_ESM_1_0	ESM0_LVL_IN_46	ESM0	R5FSS0_CORE1 ECC single-bit error interrupt (cache and TCM RAMs)	Level
R5FSS1_COMMON0_ECC_SE_TO_ESM_1_0	ESM0_LVL_IN_48	ESM0	R5FSS0_CORE1 ECC double-bit error interrupt (cache and TCM RAMs)	Level

Table 6-14. R5F Configuration

Number of Cores	R5FSS0_0	R5FSS0_1	R5FSS1_0	R5FSS1_1
4	Available	Available	Available	Available
2	Available	N/A	Available	N/A
1	Available	N/A		N/A

6.2.3 R5FSS Functional Description

6.2.3.1 R5FSS Block Diagram

Figure 6-5 shows the R5FSS block diagram.

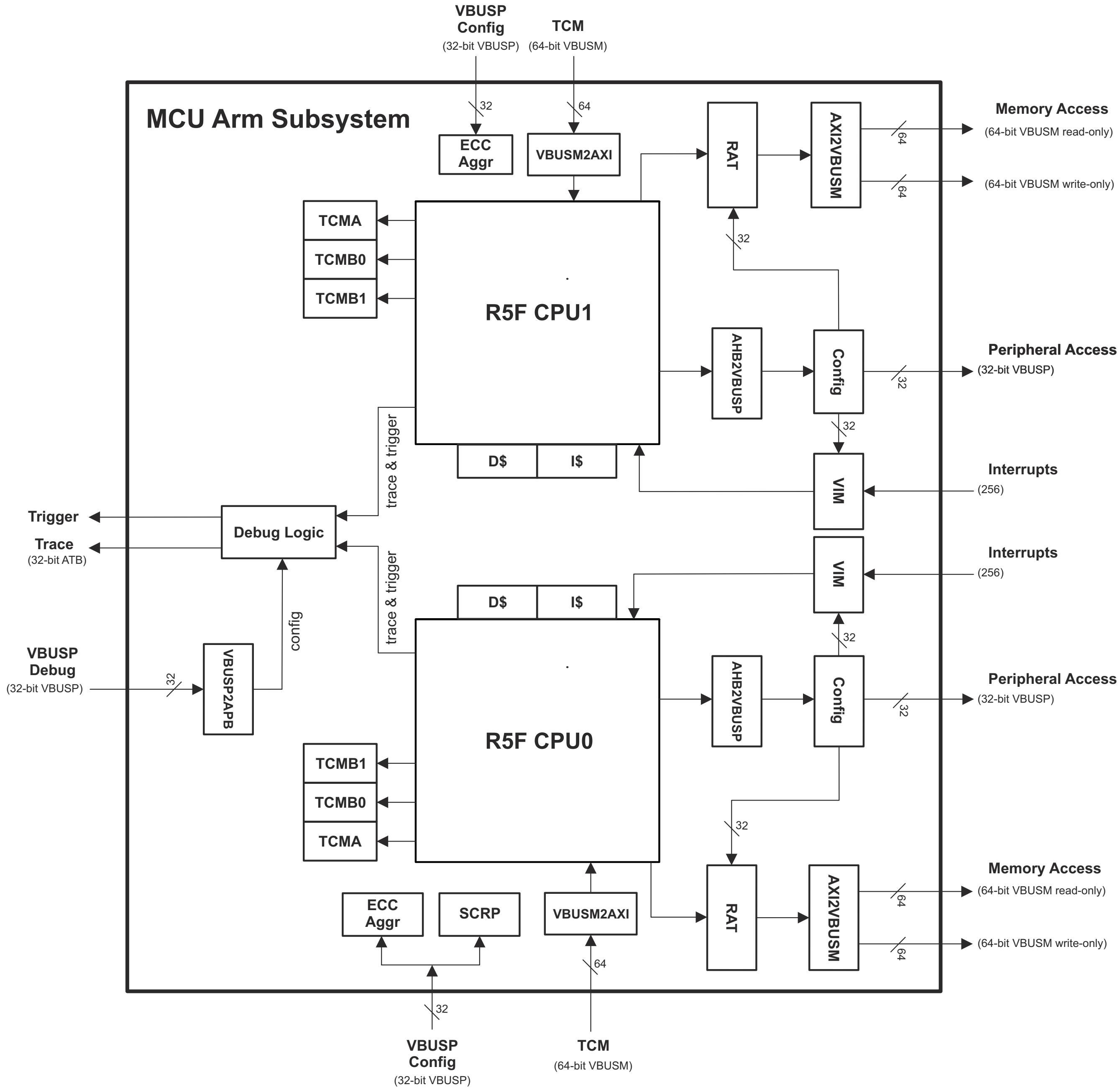

Figure 6-5. R5FSS Block Diagram

6.2.3.2 R5FSS Cortex-R5F Core

The Cortex-R5F is a processor from Arm, which is based on the Armv7-R profile. Each R5FSS implements two R5F cores, CPU0 and CPU1, each with their own RAMs and interfaces. While in reset, they can be bootstrapped to work in one of two modes: split or single-core.

In split mode, each R5F core works completely independent from the other (asymmetric multi-processing, or AMP). Each core uses its own RAMs and interfaces, with no coherence between the two cores. The only restriction is that CPU0 must be in a higher power/reset state than CPU1. For instance, CPU1 cannot be out of reset if CPU0 is not.

In single-core mode:

- CPU0 is the only operating core
- CPU1 TCMs are stacked on CPU0 TCMs and are accessible only by CPU0 and CPU0 TCM interface
- The TCM size for CPU0 is essentially doubled in this mode (128KB)
- CPU1 caches and interrupts are not used

For a brief list of features supported by the R5F processor in this device, see Section 6.2.1.1 . For more detailed description of this processor, see the *Arm Cortex-R5 Technical Reference Manual*.

6.2.3.2.1 L1 Caches

The R5F has a Harvard cache architecture, which means it has an independent L1 instruction cache (16KB) and L1 data cache (16KB). The instruction cache is protected by SECDED ECC per 64 bits. The data cache is protected by SECDED ECC per 32 bits.

6.2.3.2.2 Tightly-Coupled Memories (TCMs)

The R5F has two tightly-coupled memories (TCMs), ATCM and BTCM. The BTCM is further broken down into two interleaved banks, B0TCM and B1TCM.

TCMs are low-latency, tightly integrated memories for the R5F to use. Either TCM can be used for any combination of instruction and/or data. TCM performance is equal to performance on instructions/data that are in cache. However, TCMs have some additional advantages over cache. TCMs can be loaded with instructions that do not cache well (such as ISRs) or preloaded with code by an external source, before that code is needed, to save cache miss time. TCMs are also a good place for blocks of data for intense processing. They can be loaded (or pre-loaded by an external source) before the data is needed, saving cache miss time. The data can then be directly accessed by an external source, instead of needing to do cache evicts.

As mentioned, TCMs can be accessed (either read or written) by an external source over the TCM VBUSM target interface. This allows instructions or data to be preloaded, or for data to be read out after the R5F has processed it. The VBUSM target has a lower priority to accessing TCMs than the R5F but care must be taken to keep an external source from reading or writing TCM data that the R5F is working on. This handshaking is external to any of the R5FSS hardware.

TCMs are protected by ECC per 32 bits. For this to work, ECC must be enabled before data is written in to the TCMs (either externally or from the R5F). ECC is enabled via the following R5F system control bits: ACTLR.ATCMPCEN, ACTLR.B0TCMPCEN, and ACTLR.B1TCMPCEN, respectively.

Whether or not the TCMs are enabled is controlled by the ENABLE bit in the corresponding ATCM/BTCM region register. The default (reset) value of this bit is determined by the CPUn_INITRAMA and CPUn_INITRAMB bootstraps, respectively. Both ATCM and BTCM are configured for a size of 32KB in this device. Note that the BTCM size is the total of both B0TCM and B1TCM (16KB each).

If a TCM is not enabled, then it does not appear in the R5F's memory view, but it can be accessed by an external source. If a TCM is enabled, then its place in the R5F memory map is determined by a combination of bootstrap signal and system register. If the CPUn_LOCZRAMA bootstrap signal is high, then the initial base address of ATCM is 0x0000_0000 and the initial address of BTCM is 20'h41010. If the CPUn_LOCZRAMA bootstrap signal is low, then the initial base address of BTCM is 0x0000_0000 and the initial base address of ATCM is 20'h41010.

Note

This base address of 0x41010 for ATCM/BTCM based on the CPUn_LOCZRAMA bootstrap only affects the R5F's memory view. The SoC will see the ATCM/BTCM based on the TCM target interface regions, as defined in Section 6.2.3.3.2 . The base address of either TCM may be overwritten via the ATCM or BTCM region register. Care must be taken not to move the base address of a TCM when it may be being accessed.

It is possible to preload a TCM with instructions and boot from it. See Section 6.2.3.11 for details on TCM booting.

6.2.3.2.3 R5FSS Special Signals

Table 6-15 through Table 6-16 list some R5FSS features associated with special signals.

Table 6-15. R5FSS0 Special Features

Feature	Comment
Cluster affinity group ID	R5F Cluster 0 (ID = 0x0)
Exception handling state at reset 0 = Arm 1 = Thumb	Controlled via MAIN_SEC_MMR register setting. Defaults to Arm mode
Dual- or single-core mode 0 = Dual mode 1 = Single mode	Controlled via MAIN_SEC_MMR register setting. Defaults to a value defined by eFuse
CPUn execution halt when coming out of reset (CPUn_HALT)	Controlled via MAIN_SEC_MMR register setting. Defaults to halted state
CPUn exception vectors base address	Controlled via MAIN_SEC_MMR register setting. Defaults to Bootvector RAM address 0x0000_0000_0200
CPUn VIM base address	0x2FFF_0000
CPUn RAT base address	0x2FFE_0000
CPUn RAT accesses ID	0x4 (CPU0); 0x5 (CPU1)
CPUn ATCM enable at reset (CPUn_INITRAMA)	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn BTCM enable at reset (CPUn_INITRAMB)	Controlled via MAIN_SEC_MMR register setting. Defaults to enabled state
CPUn A/BTCM reset base address indicator (CPUn_LOCZRAMA) 0 = B at 0x0 1 = A at 0x0	Controlled via MAIN_SEC_MMR register setting. Defaults to 1
CPUn non-maskable fast interrupts enable	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn VBUSM peripheral port enabled at reset	Enabled
CPUn VBUSP peripheral port enable at reset	Enabled
CPUn VBUSP peripheral port base address	Mapped to 0x0_2000_0000 for low latency MAIN peripherals
CPUn VBUSP peripheral port size	64MB for MAIN peripherals (0x0_2000_0000 to 0x0_2FFF_FFFF)
CPUn VBUSM normal peripheral port base address	Not used
CPUn VBUSM normal peripheral port size	Not used
CPUn VBUSM virtual peripheral port base address	Not used
CPUn VBUSM virtual peripheral port size	Not used
CPUn clock stopped indication	Status logged into MAIN_SEC_MMR register bit
CPUn WFI state	Status logged into MAIN_SEC_MMR register bit
CPUn WFE state	Status logged into MAIN_SEC_MMR register bit
CPU clockstop behavior 0: CPU clocks stopped in standby 1: CPU clocks not stopped in standby	Controlled via MAIN_SEC_MMR register setting. Defaults to 0

Table 6-16. R5FSS1 Special Features

Feature	Comment
Cluster affinity group ID	R5F Cluster 1 (ID = 0x1)
Exception handling state at reset 0 = Arm 1 = Thumb	Controlled via MAIN_SEC_MMR register setting. Defaults to Arm mode
Dual- or single-core mode 0 = Dual mode 1 = Single mode	Controlled via MAIN_SEC_MMR register setting. Defaults to a value defined by eFuse
CPUn execution halt when coming out of reset (CPUn_HALT)	Controlled via MAIN_SEC_MMR register setting. Defaults to halted state
CPUn exception vectors base address	Controlled via MAIN_SEC_MMR register setting. Defaults to Bootvector RAM address 0x0000_0000_0200
CPUn VIM base address	0x2FFF_0000
CPUn RAT base address	0x2FFE_0000
CPUn RAT accesses ID	0x6 (CPU0); 0x7 (CPU1)
CPUn ATCM enable at reset (CPUn_INITRAMA)	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn BTCM enable at reset (CPUn_INITRAMB)	Controlled via MAIN_SEC_MMR register setting. Defaults to enabled state
CPUn A/BTCM reset base address indicator (CPUn_LOCZRAMA) 0 = B at 0x0 1 = A at 0x0	Controlled via MAIN_SEC_MMR register setting. Defaults to 1
CPUn non-maskable fast interrupts enable	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn VBUSM peripheral port enabled at reset	Enabled
CPUn VBUSP peripheral port enable at reset	Enabled
CPUn VBUSP peripheral port base address	Mapped to 0x0_2000_0000 for low latency MAIN peripherals
CPUn VBUSP peripheral port size	64MB for MAIN peripherals (0x0_2000_0000 to 0x0_2FFF_FFFF)
CPUn VBUSM normal peripheral port base address	Not used
CPUn VBUSM normal peripheral port size	Not used
CPUn VBUSM virtual peripheral port base address	Not used
CPUn VBUSM virtual peripheral port size	Not used
CPUn clock stopped indication	Status logged into MAIN_SEC_MMR register bit
CPUn WFI state	Status logged into MAIN_SEC_MMR register bit
CPUn WFE state	Status logged into MAIN_SEC_MMR register bit
CPU clockstop behavior 0: CPU clocks stopped in standby 1: CPU clocks not stopped in standby	Controlled via MAIN_SEC_MMR register setting. Defaults to 0

6.2.3.3 R5FSS Interfaces

6.2.3.3.1 Initiator Interfaces

The R5FSS has several initiator interfaces per core:

- 64-bit VBUSM initiator pair (1 read, 1 write) for L3 memory accesses; this is the main memory interface
  - Includes region-based address translation (RAT)
- 32-bit VBUSP initiator for peripheral access
  - Includes logic that provides the R5F CPU with a private access to VIM and RAT
  - Enabled at reset

6.2.3.3.2 Target Interfaces

The R5FSS has several target interfaces that define its internal memory space:

- 32-bit VBUSP configuration target (per core)
  - Region [0]: ECC aggregator block
- 64-bit TCM target (per core)
  - Region [0]: ATCM
  - Region [1]: BTCM
  - Region [2]: Instruction cache RAMs
  - Region [3]: Data cache RAMs
- 32-bit VBUSP debug target
  - Provides access to all R5FSS internal debug logic

Regions [0] and [1] of the TCM target interface provide direct access to the TCM RAMs. Access to the RAMs is arbitrated with access from the R5F's L1 memory system. Excessive access while the R5F is also attempting access will degrade performance.

Regions [2] and [3] of the TCM target interface provide access to the cache RAMs for testing purposes. Access to the cache RAMs can only be done while the caches are disabled and should only be done for test purposes.

In addition to the target interfaces, there are peripherals (RAT and VIM) that are only accessible by the R5F. The R5F has an access to these modules via the VBUSP peripheral interface.

6.2.3.4 R5FSS Power, Clocking and Reset

6.2.3.4.1 R5FSS Power

The following R5FSS power considerations should be noted:

- R5FSS has a single power domain for all its internal logic
- When operating in split mode, CPU0 must be in a higher power/reset state than CPU1.

For more details on R5FSS power management, including power-up and power-down sequences, see *Power*.

6.2.3.4.2 R5FSS Clocking

The R5FSS has four clock inputs:

- CPU0_CLK: This is the clock for CPU0 logic
- CPU1_CLK: This is the clock for CPU1 logic
- CPU0_ICLK: This is the clock for CPU0 interfaces
- CPU1_ICLK: This is the clock for CPU1 interfaces

CPU0_CLK and CPU1_CLK are the clocks for all of the internal CPU logic, while CPU0_ICLK and CPU1_ICLK are the clocks for all of the interfaces for their associated CPU (for example: VBUSM and VBUSP bridges, exception generation, debug and trace logic). CPU1 clocks are automatically gated in single-core mode.

The interface clock is an integer ratio of the CPU clock. The exact ratio for this device is 1:1.

6.2.3.4.3 R5FSS Reset

The R5FSS has four reset inputs:

- CPU0_RST: This is the reset for the non-debug logic of CPU0
- CPU0_DBG_RST: This resets the CPU0 debug logic, excluding the APB interface
- CPU1_RST: This is the reset for the non-debug logic of CPU1
- CPU1_DBG_RST: This resets the CPU1 debug logic, excluding the APB interface

In addition to the reset signals, there are two halt signals:

- CPU0_HALT
- CPU1_HALT

These halt signals keep the CPUs from fetching instructions when they come out of reset. The main use is to have the CPUs halted until the TCMs are loaded (when booting from TCM), though halt could be used for any other purpose.

6.2.3.5 R5FSS Vectored Interrupt Manager (VIM)

6.2.3.5.1 VIM Overview

The VIM aggregates device interrupts and sends them to the R5F CPU(s). It can be used in either split or single-core configuration.

The VIM module supports the following features:

- 256 interrupt inputs per R5F core
- Each interrupt has its own 4-bit programmable priority
  - Defined via the R5FSS_VIM_PRI_INT_j register
  - The VIM provides support for priority interruption of interrupts
- Each interrupt has its own enable mask
  - Interrupt enable is done via the R5FSS_VIM_INTR_EN_SET_j register
  - Interrupt disable is done via the R5FSS_VIM_INTR_EN_CLR_j register
- Each interrupt can be programmed as either an IRQ or FIQ
  - Defined via the R5FSS_VIM_INTMAP_j register
- Each interrupt has its own programmable 32-bit vector address associated with it
  - Defined via the R5FSS_VIM_VEC_INT_j register
  - Protected with SECDED
- One IRQn and one FIQn output per core
- Vectored interrupt interface
  - Compatible with R5F VIC port
- Default vector provided when a double-bit error is detected
- Split or single-core capable
  - In single-core mode, only interrupts connected to VIM interrupt core 0 are available
- Software interrupt generation

6.2.3.5.2 VIM Interrupt Inputs

The VIM supports 256 interrupt inputs per core. Each interrupt can be either a level or a pulse (both active-high). The interrupt mapping for the two R5F cores can be found in *Interrupt Sources*.

6.2.3.5.3 VIM Interrupt Outputs

The VIM has two interrupt outputs per core:

- *CoreN_IRQn*: This is a normal interrupt for core *N* (active-low level). It can be serviced via the VIC interface or through the MMR interface. Whenever an interrupt input goes high, if that interrupt is mapped as an IRQ (via the R5FSS_VIM_INTMAP_j register) and is enabled (via the R5FSS_VIM_INTR_EN_SET_j register), then it will cause an IRQ to assert
- *CoreN_FIQn*: This is a fast (or non-maskable) interrupt for core *N* (active-low level). FIQs always have priority over IRQs. An FIQ can be serviced through the MMR interface. Whenever an interrupt input goes high, if that interrupt is mapped as an FIQ and is enabled, then it will cause an FIQ to assert

6.2.3.5.4 VIM Interrupt Vector Table (VIM RAM)

For each VIM interrupt core, there is an associated interrupt vector table (VIM RAM) that is used to store the address of ISRs. During register vectored interrupt and hardware vectored interrupt, VIM accesses the interrupt vector table using the vector value to fetch the address of the corresponding ISR. Note that both interrupt vector tables are identical in their memory organization.

The VIM RAM is basically comprised of a set of interrupt vector registers (R5FSS_VIM_VEC_INT_j). Hence, the interrupt vector table is organized in 256 words of 30 bits, with a base address corresponding to the physical address of the first register in the group.

Note

The lower two bits of the 32-bit interrupt vector are always 0s.

Figure 6-6 shows the VIM RAM interrupt vector map.

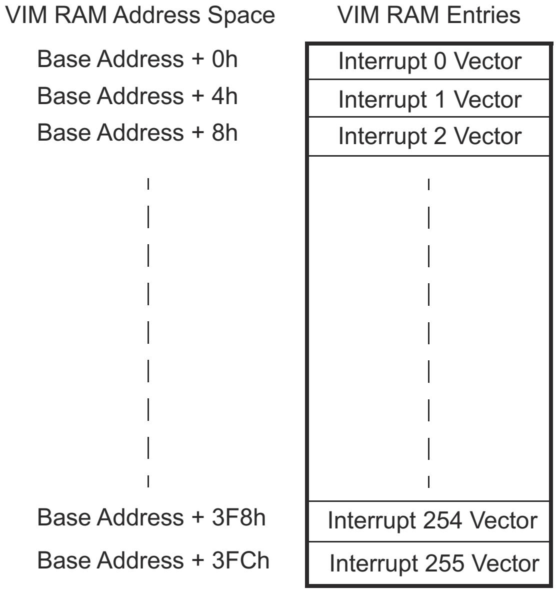

Figure 6-6. VIM RAM Interrupt Vector Map

The interrupt vector table has protection by ECC to indicate corruption due to soft errors. The ECC logic inside VIM supports SECDED. See Table 6-19 for the VIM RAM ID in the ECC aggregator map.

6.2.3.5.5 VIM Interrupt Prioritization

The VIM supports the interruption of the currently active interrupt by one with a higher priority. FIQs and IRQs are completely separate but both use the same mechanism.

When an interrupt goes from pending to active (FIQ: reading the R5FSS_VIM_FIQVEC register; IRQ: reading the R5FSS_VIM_IRQVEC register, or the *coreN_IRQACK* going high), then the interrupt is loaded into the corresponding active register (R5FSS_VIM_ACTFIQ / R5FSS_VIM_ACTIRQ), and all interrupts of an equal or lesser priority are masked (discarded). If prior to this interrupt being cleared (by writing to the R5FSS_VIM_FIQVEC register, or R5FSS_VIM_IRQVEC register) another interrupt of higher priority arrives, then the FIQn/IRQn will be asserted and that interrupt made pending as normal. If the CPU switches this interrupt to active (by reading the R5FSS_VIM_FIQVEC / R5FSS_VIM_IRQVEC register), then the currently active interrupt will be pushed onto a stack. When an interrupt is cleared by reading the R5FSS_VIM_FIQVEC / R5FSS_VIM_IRQVEC register, if there are any interrupts on the stack, the first entry is popped off and put back into the R5FSS_VIM_ACTFIQ / R5FSS_VIM_ACTIRQ register, so that software may continue where it left off.

6.2.3.5.6 VIM ECC Support

The memory that holds the interrupt vector for each interrupt is protected by SECDED ECC. Single-bit errors are corrected and written back. Double-bit errors are not corrected. If a double-bit error occurs while trying to load a vector, then the R5FSS_VIM_DEDVEC register is used to provide the default vector for the *coreN_IRQADDRV* signal, the R5FSS_VIM_IRQVEC register, and the R5FSS_VIM_FIQVEC register. The R5FSS_VIM_DEDVEC should point to an ISR that handles the fact that there was an uncorrectable error in the interrupt handling.

Some possible remediating actions would be to:

1. Reconstruct the vector table and re-start the application
    a. Potentially switch to a completely software interrupt handler in the mean time

2. Restart the application from scratch
3. Reset the device
4. Sit in a loop (or WFI) while something external (for example, the ESM) responds to the DED interrupt that will be generated

It is up to the user and the application to determine the appropriate action.

Note

An interrupt that has an uncorrectable vector error (and thus uses the DED vector) will still have the priority of the original interrupt . This makes it possible for a higher priority interrupt to supercede the handling of the error.

Control and reporting are done by the R5FSS ECC aggregator.

6.2.3.5.7 VIM IDLE State

The VIM will indicate IDLE when there are no pending unmasked interrupts or MMR accesses. The VIM does not have a clock stop interface.

6.2.3.5.8 VIM Interrupt Handling

There are multiple ways to service an interrupt depending on how much of the hardware assistance offered by the VIM the software wants to take advantage of.

For IRQs, it is recommended to use the procedure in Section 6.2.3.5.8.1 , but the procedures in Section 6.2.3.5.8.2 or Section 6.2.3.5.8.3 (if a user wants to implement a fully software prioritization scheme) may be used as alternatives.

For FIQs, it is recommended to use the procedure in Section 6.2.3.5.8.4 , but the procedure in Section 6.2.3.5.8.5 may be used as an alternative.

Note

These descriptions do not include steps such as stack pushes and state retention that software must take in order to return from the ISR. It is assumed that the programmer is aware of these steps.

6.2.3.5.8.1 Servicing IRQ Through Vector Interface

If the associated CPU has the vector (VIC) interface enabled, then the following method is used for servicing IRQs:

1. Hardware handshake
    a. CPU asserts *coreN_IRQACK* high
    b. VIM asserts *coreN_IRQADDRV* to indicate that the *coreN_IRQADDR* bus is stable with the correct vector address
    c. CPU reads *coreN_IRQADDR*, jumps to that address, and de-asserts *coreN_IRQACK* low
    d. VIM de-asserts *coreN_IRQn* and *coreN_IRQADDRV*, VIM masks (discards) all IRQs with the same or lower priority
    e. VIM loads the value from the R5FSS_VIM_PRIIRQ[9:0] NUM bit field (which corresponds to the vector address) into the R5FSS_VIM_ACTIRQ[9:0] NUM bit field, which causes the R5FSS_VIM_ACTIRQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (determined by reading the R5FSS_VIM_ACTIRQ[9:0] NUM bit field to determine number, and reading the appropriate bit in the R5FSS_VIM_INTTYPE_j register to determine type)
    a. Pulse

        1. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_IRQSTS_j register, or R5FSS_VIM_STS_j register
        2. Clear the interrupt at the source. This way, the source can generate another pulse, if it needs to, and the VIM will process this as a new interrupt
    - b. Level
        1. Clear the interrupt at the source
        2. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_IRQSTS_j register, or R5FSS_VIM_STS_j register. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt. If the source maintains the level, then it means there is another interrupt

4. Write any value to the R5FSS_VIM_IRQVEC register
    - a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    - b. This will also clear the R5FSS_VIM_ACTIRQ[31] VALID bit

6.2.3.5.8.2 Servicing IRQ Through MMR Interface

When an IRQ interrupt is received, the CPU should follow these steps if not using the vector interface:

1. Read the R5FSS_VIM_IRQVEC register and jump to that address to service the ISR
    - a. Reading this register will mask (discard) all interrupts of an equal or lower priority and de-assert the *coreN_IRQn* output. If another interrupt of a higher priority becomes available, the *coreN_IRQn* will re-assert, allowing priority interruption of an interrupt
    - b. Reading this register will cause the value from the R5FSS_VIM_PRIIRQ[9:0] NUM bit field to be loaded into the R5FSS_VIM_ACTIRQ[9:0] NUM bit field, and the R5FSS_VIM_ACTIRQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    - a. Pulse
        1. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
        2. Clear the interrupt at the source
    - b. Level
        1. Clear the interrupt at the source
        2. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register

4. Write any value to the R5FSS_VIM_IRQVEC register
    - a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    - b. This will also clear the R5FSS_VIM_ACTIRQ[31] VALID bit

6.2.3.5.8.3 Servicing IRQ Through MMR Interface (Alternative)

If a user does not want to use the R5FSS_VIM_IRQVEC register, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the R5FSS_VIM_IRQVEC register is never read). Software would be responsible for doing all priority operations.

1. Determine which interrupt to service
    - a. Read the R5FSS_VIM_PRIIRQ register to determine which interrupt is the highest priority IRQ currently asserted, OR

  b. Optionally read the R5FSS_VIM_IRQGSTS register to determine which groups have IRQs pending, then read the R5FSS_VIM_IRQSTS_j register and use a software prioritization scheme to determine which IRQ to service

2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
        ii. Clear the interrupt at the source.
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register

6.2.3.5.8.4 Servicing FIQ

When an FIQ interrupt is received, the CPU should follow these steps:

1. Read the R5FSS_VIM_FIQVEC register and jump to that address to service the ISR
    a. Reading this register will mask (discard) all interrupts of an equal or lower priority and de-assert the *coreN_FIQn* output. If another interrupt of a higher priority becomes available, the *coreN_FIQn* will re-assert, allowing priority interruption of an interrupt.
    b. Reading this register will cause the value from the R5FSS_VIM_PRIFIQ[9:0] NUM bit field to be loaded into the R5FSS_VIM_ACTFIQ[9:0] NUM bit field, and the R5FSS_VIM_ACTFIQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (determined by reading the R5FSS_VIM_ACTFIQ[9:0] NUM bit field to determine number, and reading the appropriate bit in the R5FSS_VIM_INTTYPE_j register to determine type)
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register
        ii. Clear the interrupt at the source. This way, the source can generate another pulse, if it needs to, and the VIM will process this as a new interrupt
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt. If the source maintains the level, then it means there is another interrupt
4. Write any value to the R5FSS_VIM_FIQVEC register
    a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    b. This will also clear the R5FSS_VIM_ACTFIQ[31] VALID bit

6.2.3.5.8.5 Servicing FIQ (Alternative)

If a user does not want to use the R5FSS_VIM_FIQVEC register, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the R5FSS_VIM_FIQVEC register is never read). Software would be responsible for doing all priority operations.

1. Determine which interrupt to service

    a. Read the R5FSS_VIM_FIQVEC register to determine which interrupt is the highest priority FIQ currently asserted, OR
    b. Optionally read the R5FSS_VIM_FIQGSTS register to determine which groups have IRQs pending, then read the R5FSS_VIM_FIQSTS_j register and use a software prioritization scheme to determine which FIQ to service
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register
        ii. Clear the interrupt at the source.
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register.

6.2.3.6 R5FSS Region Address Translation (RAT)

6.2.3.6.1 R5FSS Usage

R5 is a micro controller with 32b address, which is only able to access up to 4GB address space. However, Sitara SoC supports 36b address and majority of the memory region beyond lower 4GB are implemented. Region based address translation block, called RAT, is introduced to allow R5 core to access full 36b SoC memory map.

Each R5 core has its own RAT block, and only R5 core itself is able to program the RAT.

Figure 6-7 shows the main R5’s default 32b memory map view when main R5 is out of reset.

The full RAT functionality is described in Section 6.2.3.6.2 , *RAT Function*.

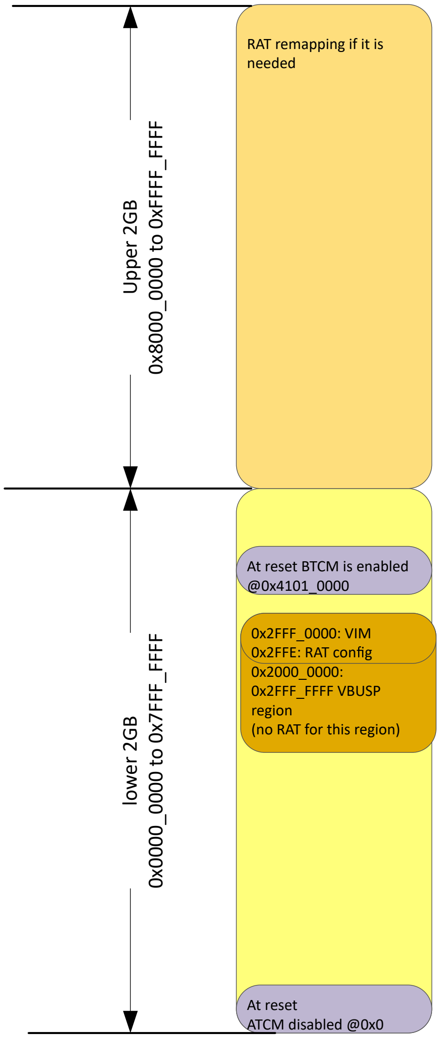

Figure 6-7. R5 Core Default Memory Map View

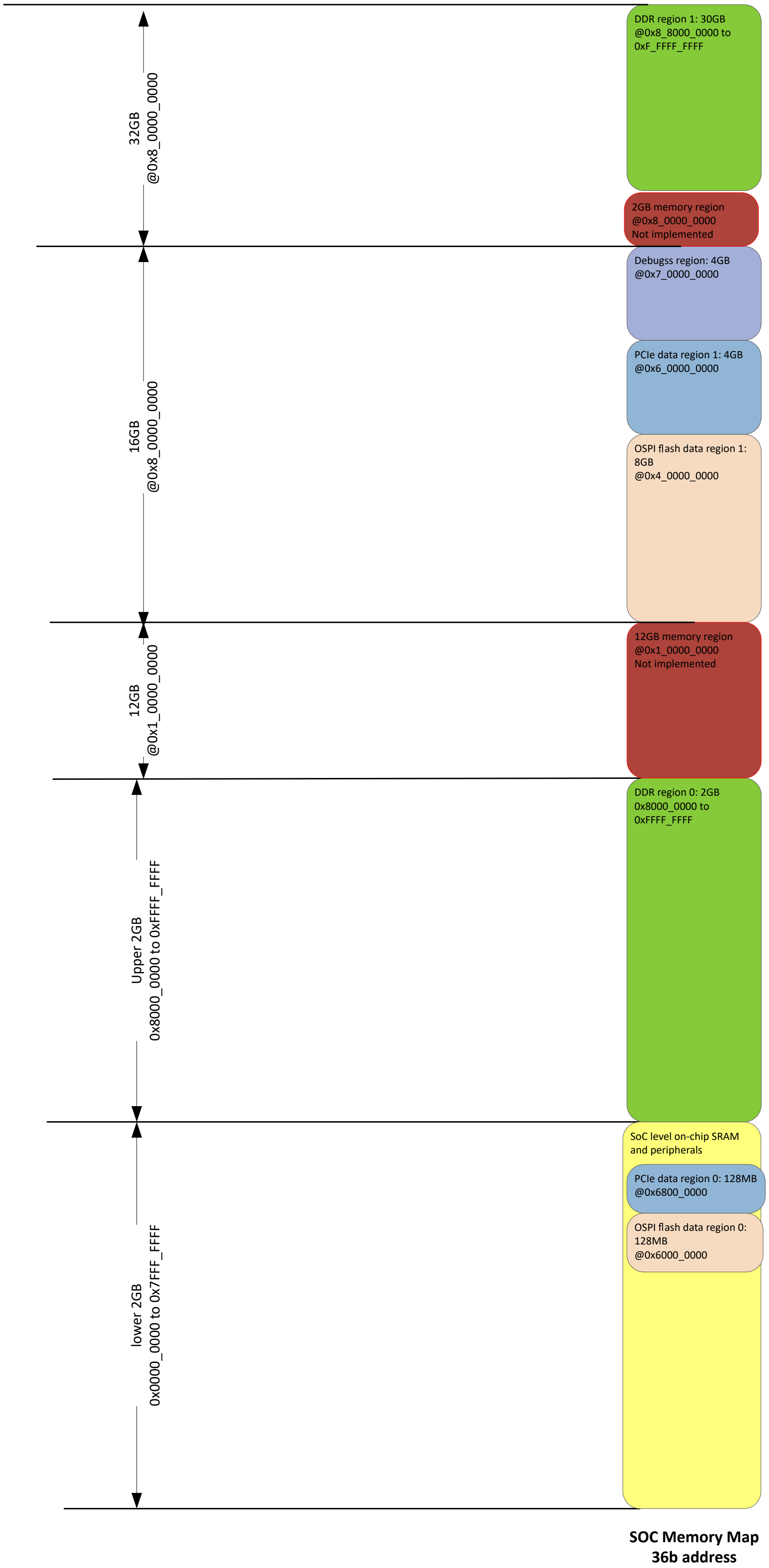

Figure 6-8. Typical Sitara SoC Memory Map View

RAT block enables R5 core to have full access on the SoC memory map including the memory region at and above 0x1_0000_0000.

Figure 6-9 shows how R5 access various end points, including its own ATCM, BTCM, VIM and SoC memory and peripherals. R5's ATCM is by default at address 0x0, and its BTCM is at address 0x4101_0000. R5 uses address 0x2FFF_0000 to access its VIM and 0x2FFE_0000 to access the RAT configuration region and all the other transactions between address range 0x2000_0000 to 0x2FFF_FFFF are sent to the 32b peripheral interface to access the peripherals in SoC. The transactions with the rest of address are sent to RAT block, which could go through address remapping function from original R5's 32b address to 36b SoC address.

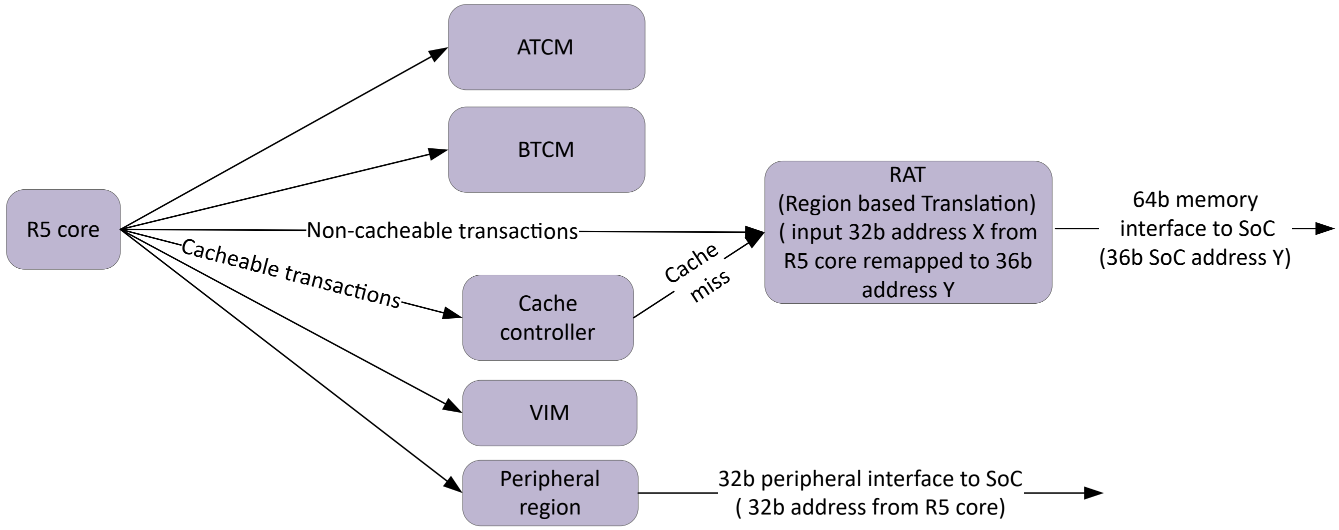

Figure 6-9. R5 Internal Address Decoding

6.2.3.6.2 RAT Function

RAT block is responsible to do a region based address translation. For each region, user can define the starting address and size of the region and remapping the transactions to use a new address range.

The starting address and region size need to be aligned. For example, if the region size is 16KB, the starting address for that region needs to be 16KB aligned. And region size should be minimum 4KB or larger to avoid transactions cross the region boundaries.

Each RAT block supports multiple programmable regions. And it is important that those regions are not overlapping with each other.

RAT block is by default disabled, which means RAT block does not do address remapping. The 32b address coming from R5 core is directly sent out to the SoC level. The user can program each RAT remapping region individually. For the transactions does not hit any remapping region, RAT block just simply forwards the transactions to the SoC level with its original address.

6.2.3.6.3 How to use RAT Block in R5

Table 6-17 shows the default R5 memory map view. Without enabling RAT function, all the regions beyond 4GB address space will not be accessible by R5.

Sitara™ SoC memory map is constructed the way to allow R5 and high level application processor such as A53 have similar memory map as possible. This methodology enables that R5 and ARM A53 core have a common memory map for all the SoC level memories and SoC level peripherals except a few exceptions:

- DDR's data space beyond 32b address, basically upper DDR data space beyond 2GB
- PCIe data space beyond 32b address
- OSPI data space beyond 32b address
- Debug configuration region

Table 6-17. R5 Memory map by Default

	R5 Memory Map(32b)	SoC Memory Map (36b)
SoC Level peripheral and on-chip SRAM	0x0 to 0x7FFF_FFFF Same address as SoC memory map	0x0 to 0x7FFF_FFFF
2GB DDR region	Same as SoC memory map: 0x8000_0000 to 0xFFFF_FFFF	0x80000_0000 to 0xFFFF_FFFF
Additional DDR region	Not accessible	0x8_8000_0000 (30GB)
Additional 8GB OSP Space	Not accessible	0x4_0000_0000 (4GB) 0x5_0000_0000 (4GB)
Additional PCIe data space	Not accessible	0x6_000_0000
Debug configuration region	Not accessible	0x7_0000_0000

Even though all the transactions other than going to ATCM/BTCM and transactions between address range 0x2000_0000 to 0x2FFF_FFFF could use RAT block to remap to different address, it is recommended that only use RAT block to remap the R5 transactions with address between 0x8000_0000 to 0xFFFF_FFFF.

- Any transactions from R5 with address between 0x0 to 0x7FFF_FFFF are sent out to SoC directly (unless it is targeted to its internal end points such as A/B TCM, its VIM and RAT configuration)
- Only enable RAT to remap the transactions with address between 0x8000_0000 to 0xFFFF_FFFF if R5 needs to access the following address space:
  - PCIe data space at address 0x6_0000_0000
  - OSPI data space address 0x4_0000_0000 and 0x5_0000_0000
  - Debug configuration region at address 0x7_0000_0000
  - DDR data space at address 0x8_8000_0000

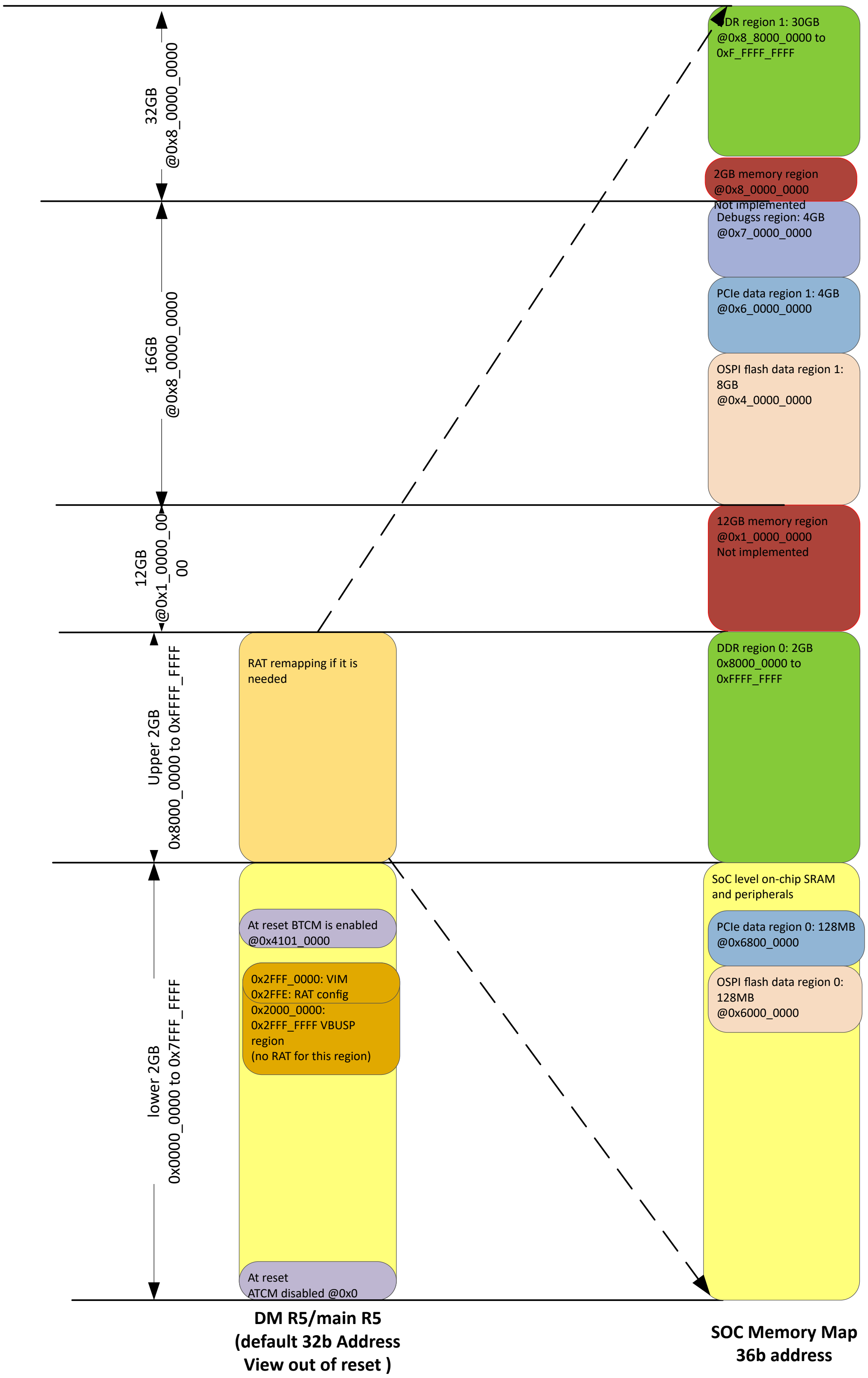

Figure 6-10. Example of Using RAT to Access Full 36b SoC Memory Map

6.2.3.6.4 Example of Using RAT to Access Full 36b SoC Memory Map

This section shows an example on how to utilize RAT block to allow R5 to access 36 SoC Memory Map. The RAT block inside R5 has up to 8 address remapping regions.

Assuming R5 needs to access the following region:

- All the SoC level on-chip SRAM
- All the SoC level peripherals
- Access 512MB OSPI region at address 0x4_0000_0000
- Access 1GB DDR region at address 0x9_0000_0000
- Access 512MB DDR region at address 0x8000_0000

First of all, we need to construct 32b R5 memory map as following and how those memory spaces are mapped to SoC level, shown in Table 6-18. Users can define where the OSPI and DDR data space placed inside R5's memory map and how they should be mapped to SoC level address map. Table 6-18 just shows one of the many possible ways to construct the memory map.

Table 6-18. Example of R5 Address Mapping

	R5 Memory Map(32b)	SoC Memory Map (36b)	RAT Remapping
SoC Level peripheral and on-chip SRAM (This is guaranteed by SoC Hardware design. No user configuration is needed)	0x0 to 0x7FFF_FFFF Same address as SoC memory map	0x0 to 0x7FFF_FFFF	Not RAT Remapping
512MB OSPI data region (user defined)	0x8000_0000 to 0x9FFF_FFFF	0x4_0000_0000 to 0x4_1FFF_FFFF	Using RAT remapping region 0
512MB DDR space (user defined)	0xA000_0000 to 0xBFFF_FFFF	0x8000_0000 to 0x9FFF_FFFF	Using RAT remapping region 1
Additional 1GB DDR Space (user defined)	0xC000_0000 to 0xFFFF_FFFF	0x9_0000_0000 to 0x9_3FFF_FFFF	Using RAT remapping region 2

In this example, only three RAT regions are needed:

- Region 0 is used to remap R5's address between 0x8000_0000 to 0x9FFF_FFFF to SoC level address 0x4_0000_0000 to 0x4_1FFF_FFFF
- Region 1 is used to remap R5's address between 0xA000_0000 to 0xBFFF_FFFF to 0x8000_0000 to 0x9FFF_FFFF
- Region 2 is used to remap R5's address 0xc000_0000 t0 0xFFFF_FFFF to 0x9_0000_0000 to 0x9_3FFF_FFFF.

In order achieving those mappings, those are the setting of the RAT configuration registers:

	Region 0	Region 1	Region 2	Other regions
Region control register	Enabled, size set to 512MB	Enabled, size set to 512MB	Enabled, size set to 1GB	disabled
Region base(32b)	0x8000_0000	0xA000_0000	0xc000_0000	Don't care
Region translated lower address(32b)	0x0000_0000	0x8000_0000	0x0000_0000	Don't care
Region translated upper address	0x4	0x0	0x9	Don't care

Figure 6-11 shows how RAT is remapping the address between R5’s 32b address to 36b SoC address.

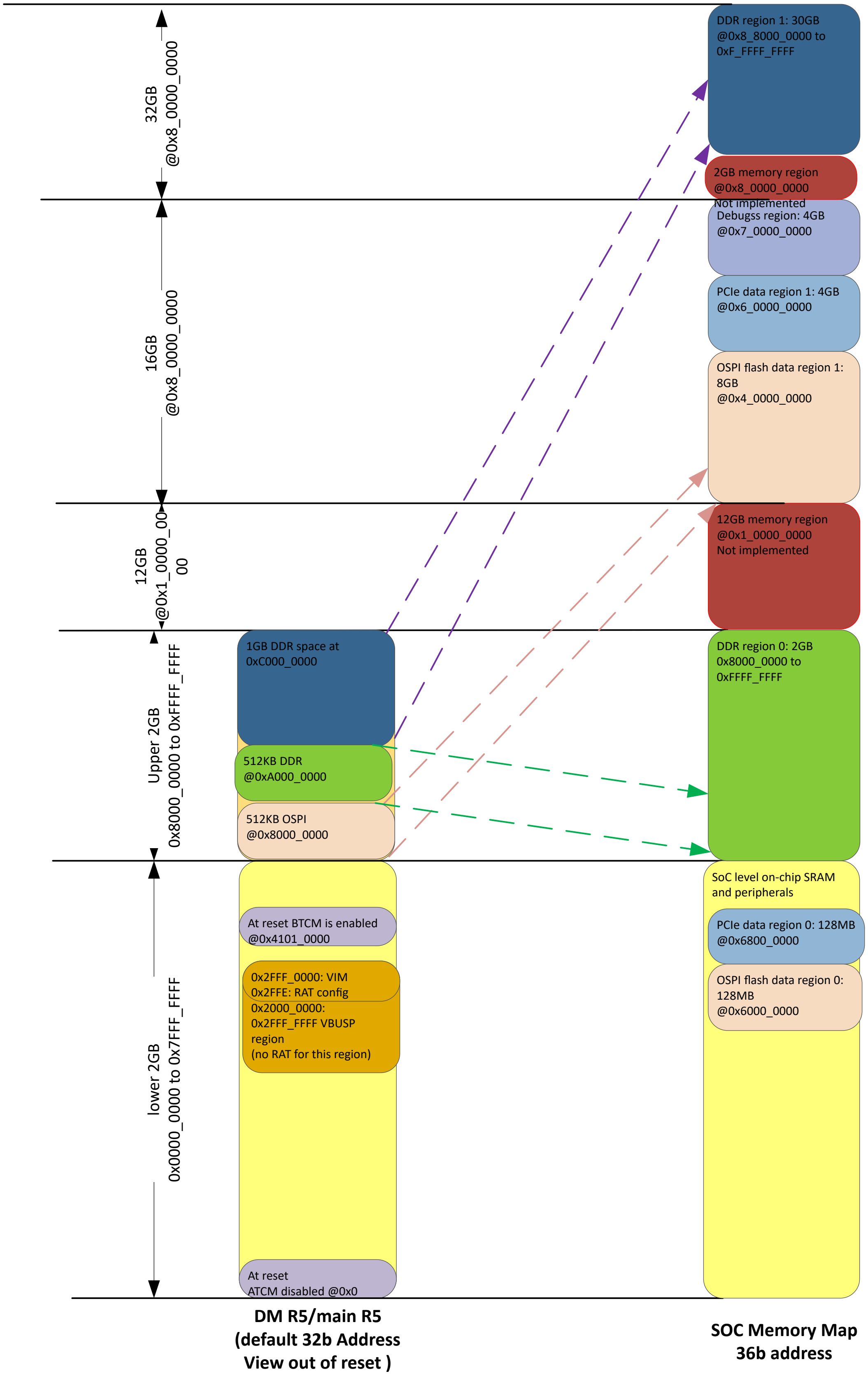

Figure 6-11. RAT Configuration Example

6.2.3.7 R5FSS ECC Support

The R5F provides native ECC and parity support on all related memories, generating and checking the redundancy automatically. The methods for checking and reporting errors are available in the *Arm Cortex-R5 Technical Reference Manual*.

The R5FSS adds the capability of testing this logic by allowing errors (single and double bit) to be injected into memories (for testing purposes) via an ECC aggregator (per core). Note that because the R5FSS ECC aggregator is only used in error-injection mode, it only supports a subset of the generic ECC aggregator functionality in the device.

For a detailed description of the generic ECC aggregator functionality, see *ECC Aggregator*. For register descriptions of R5FSS CPU0 and CPU1 ECC aggregators, see *R5FSS_CPU0_ECC_AGGR_CFG_REGS Registers* and *R5FSS_CPU1_ECC_AGGR_CFG_REGS Registers*, respectively.

Table 6-19 provides the RAM ID for each core. This is needed for bit field [10-0] ECC_VECTOR in the corresponding R5FSS_CPU0_VECTOR / R5FSS_CPU1_VECTOR register (part of the ECC aggregator register space).

Table 6-19. RAM ID Map for ECC Aggregator (Per Core)

RAM ID	Memory Name
0	CPU0/1 ITAG RAM0
1	CPU0/1 ITAG RAM1
2	CPU0/1 ITAG RAM2
3	CPU0/1 ITAG RAM3
4	CPU0/1 IDATA BANK0
5	CPU0/1 IDATA BANK1
6	CPU0/1 IDATA BANK2
7	CPU0/1 IDATA BANK3
8	CPU0/1 DTAG RAM0
9	CPU0/1 DTAG RAM1
10	CPU0/1 DTAG RAM2
11	CPU0/1 DTAG RAM3
12	CPU0/1 DDIRTY RAM
13	CPU0/1 DDATA RAM0
14	CPU0/1 DDATA RAM1
15	CPU0/1 DDATA RAM2
16	CPU0/1 DDATA RAM3
17	CPU0/1 DDATA RAM4
18	CPU0/1 DDATA RAM5
19	CPU0/1 DDATA RAM6
20	CPU0/1 DDATA RAM7
21	CPU0/1 ATCM BANK0
22	CPU0/1 ATCM BANK1
23	CPU0/1 B0TCM BANK0
24	CPU0/1 B0TCM BANK1
25	CPU0/1 B1TCM BANK0
26	CPU0/1 B1TCM BANK1
27	CPU0/1 VIM RAM

6.2.3.8 R5FSS Memory View

The memory view of each R5F (that is, the memory map as seen by each R5F) is a function of several things:

- Exception vector bootstrap: The R5F exception table (including boot vector) is always 32 bytes at address 0x00000000 as seen by the R5F. If not booting from a TCM, then boot is done over the main memory interface. The exception vector bootstrap is under software control, which allows these 32 bytes at address 0x00000000 to be remapped somewhere else in the SoC memory map.
- TCM locations: TCMs can be enabled or disabled and located at different places in the memory map, depending on bootstrap configuration. For more details, see Section 6.2.3.2.2 .
- Peripheral interface locatons: The RF5 natively supports three interfaces for peripheral access. Each can be enabled/disabled and located based on bootstrap configuration. Note that the VBUSP peripheral interface must be enabled in order to use RAT and VIM.
- RAT base address: This is determined by a bootstrap. This address is located within the VBUSP peripheral interface address space.
- VIM base address: This is determined by a bootstrap. This address is located within the VBUSP peripheral interface address space.
- RAT programming: The RAT can take regions of memory accessible by the main memory interface and map them to different addresses.

The combination of the above determines what the R5F sees where in the memory map, and over what interface different transactions come out. Every transaction that does not directly address a TCM or a peripheral interface comes over the main memory interface. Transactions on the main memory interface can be further remapped with the RAT.

See *Memory Map*, for the complete R5F memory view for this device.

6.2.3.9 R5FSS Interrupts

All interrupts that are generated by the R5FSS are summarized in *R5FSS0/1 Hardware Requests*, along with their mapping. They can be divided into the following groups:

- R5F CPU internal interrupts: These are described in *Arm Cortex-R5 Technical Reference Manual*.
- ECC aggregator interrupts: These are described in the *ECC Aggregator* chapter.
- RAT exception interrupt.

6.2.3.10 R5FSS Debug and Trace

The R5FSS supports standard Arm CoreSight debug and trace architecture. For more details, see the *On-chip Debug* chapter.

6.2.3.11 R5FSS Boot Options

There are two methods of booting the R5F, or rather, two methods of placing the exception vectors (of which the boot vector is one).

The first method is to have the exception vectors external to the R5F. The user can place the exception vectors at the address indicated by the exception vector bootstrap and then program the boot vector there. When the processor exits reset, it will fetch the boot vector from this location.

The second method is to boot from a TCM. To do this, software should take the following steps:

1. Assert the correct bootstraps
   a. To boot from ATCM, set CPUn_INITRAMA (or CPUn_INITRAMB to boot from BTCM)
   b. Assert CPUn_LOCZRAMA properly for the desired TCM
2. Assert CPUn_HALT
3. Release the CPU from reset
4. Load the desired code into the TCM via the TCM target port
   a. Exception vectors should be located at address 0x00000000 of the TCM
5. De-assert CPUn_HALT

6.2.3.12 R5FSS Core Memory ECC Events

The R5F core generates several events as part of event bus that can be monitored by the PMU for debugging. The memory ECC related events from the event bus are exported to ESM for monitoring.

There are four ECC interrupts to the ESM that aggregate different categories of ECC events – CPU0 single error, CPU0 multi error, CPU1 single error, and CPU1 multi error events. Each ECC event has a 2-bit event bus counter associated with it. Everytime an event occurs, the counter is incremented by 1 till it reaches the max value of 3. The interrupt is asserted if the bus counter of any event associated with the interrupt is non-zero.

Each event bus counter has a MMR decrement control to decrement the counter by 1. So, for example, if a counter value is 2, the MMR to decrement the counter would need to be written 2 times to decrement the counter to 0. The reason decrement control has been added instead of clear control is if a new error occurs between the time the status register is read and the clear MMR is written, the new error would be lost. Write-to-decrement ensures that this does not happen.

When all event bus counters of an associated interrupt are zero, the interrupt is cleared. It takes three clock cycles for the event bus counter to be decremented once the write to the decrement control MMR presents itself at the R5FSS boundary.

Since each of the four ECC interrupts have single bit control to set the interrupt but multiple bits for clearing it, note that once an interrupt is set using the R5FSS_EVNT_BUS_ESM_SET register, it can be cleared by setting all the bits of the R5FSS_EVNT_BUS_ESM_CLR register that correspond to that particular interrupt. For example, if bit [0] of the R5FSS_EVNT_BUS_ESM_SET register is set, it can be cleared by setting bits [7-0] of the R5FSS_EVNT_BUS_ESM_CLR register to clear the interrupt.

The R5 core event bus only signals event when it is enabled. Non-invasive or invasive debug mode needs to be enabled to enable the PMU counters.

The export of the events to the event bus can be enabled by setting the X bit in the Performance Monitor Control Register of the R5 core. For more details, refer to Arm R5 TRM.

Table 6-20. R5 Event Bus Single-Bit Error Events

Event Bus Bit #	Description	Associated Status Register
22	Instruction cache tag RAM parity or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS0 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS0
23	Instruction cache data RAM parity or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS1 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS1
24	Data cache tag or dirty RAM parity error or correctable ECC error, from data-side or ACP.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS2 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS2
25	Data cache data RAM parity error or correctable ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS3 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS3
40	ATCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS4 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS4
41	B0TCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS5 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS5
42	B1TCM single-bit ECC error.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS6 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS6
43	TCM correctable ECC error reported by load/ store unit.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS7 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS7
44	TCM correctable ECC error reported by prefetch unit.	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS8 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS8

Table 6-21. R5 Event Bus Multi-Bit Error Events

Event Bus Bit #	Description	Associated Status Register
26	TCM fatal ECC error reported from the prefetch unit.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS0 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS0

Table 6-21. R5 Event Bus Multi-Bit Error Events (continued)

Event Bus Bit #	Description	Associated Status Register
27	TCM fatal ECC error reported from the load/ store unit.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS1 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS1
33	Data cache data RAM fatal ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS2 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS2
34	Data caches tag/dirty RAM fatal ECC error, from data-side or ACP.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS3 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS3
37	ATCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS4 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS4
38	B0TCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS5 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS5
39	B1TCM multi-bit ECC error.	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS6 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS6

6.3 Cortex-M4F Subsystem (MCU_M4FSS)

This chapter describes the Arm Cortex-M4F based safety processing microcontroller unit (MCU_M4FSS) in the device.

6.3.1 MCU_M4FSS Overview

The MCU_M4FSS is an Arm Cortex-M4F based subsystem running safety processing. During the boot process, the MCU_M4FSS will be configured by an initial software running on a different core. Following configuration, software will release the safety processor (M4F) out of reset, and at this point safety processor code starts execution.

Note

The Cortex-M4F processor is a Cortex-M4 processor that includes the optional floating point unit (FPU) extension.

The MCU_M4FSS is designed to meet SIL-2 safety requirements. Safety is enabled for all major subsystem components that include ECC / EDC features:

- ECC: I-RAM, D-RAM
- EDC: I-RAM, D-RAM, ECC_AGGR, RAT, CBASS, AHB2VBUSP bridges

There is one MCU_M4FSS in the device. Table 6-22 shows MCU_M4FSS allocation across device domains.

Table 6-22. MCU_M4FSS Allocation Across Device Domains

Module Instance	Domain	
	MCU	MAIN
MCU_M4FSS0	✓	–

6.3.1.1 MCU_M4FSS Features

The M4FSS supports the following features:

- Arm Cortex-M4F RISC CPU
  - Single-core implementation
  - Core revision is r0p1
  - Armv7-M architecture
  - Memory protection unit (MPU)
  - Nested vectored interrupt controller (NVIC), to achieve low interrupt latency
    - 64 external interrupts
    - 3-bit priority (8 priority levels)
  - Bus interfaces
    - Three advanced high-performance bus-lite (AHB-Lite) interfaces: ICode, DCode, and system bus interfaces
    - Private peripheral bus (PPB) based on advanced peripheral bus (APB) interface
- 256KB SRAM memory system divided into two banks
  - 192KB of instruction code (I-RAM)
  - 64KB of data space (D-RAM)
- Ability to execute code from internal SRAMs or external memories
- External initiators can access internal SRAMs if allowed
- 32-bit to 36-bit region-based address translation (RAT)
- Fault detection and correction
  - SECDED ECC protection on I-RAM
  - SECDED ECC protection on D-RAM
  - Fault error interrupt generation
- Standard Arm debug and trace architecture

6.3.1.2 MCU_M4FSS Not Supported Features

The MCU_M4FSS does *not* support the following native M4F features in this device:

- No big-endian support

- No ROM is available
- No Firewall support for internal CBASS

6.3.2 MCU_M4FSS Integration

This section describes the MCU_M4FSS integration in the device, including information about clocks, resets, and hardware requests.

Figure 6-12 shows the MCU_M4FSS0 integration.

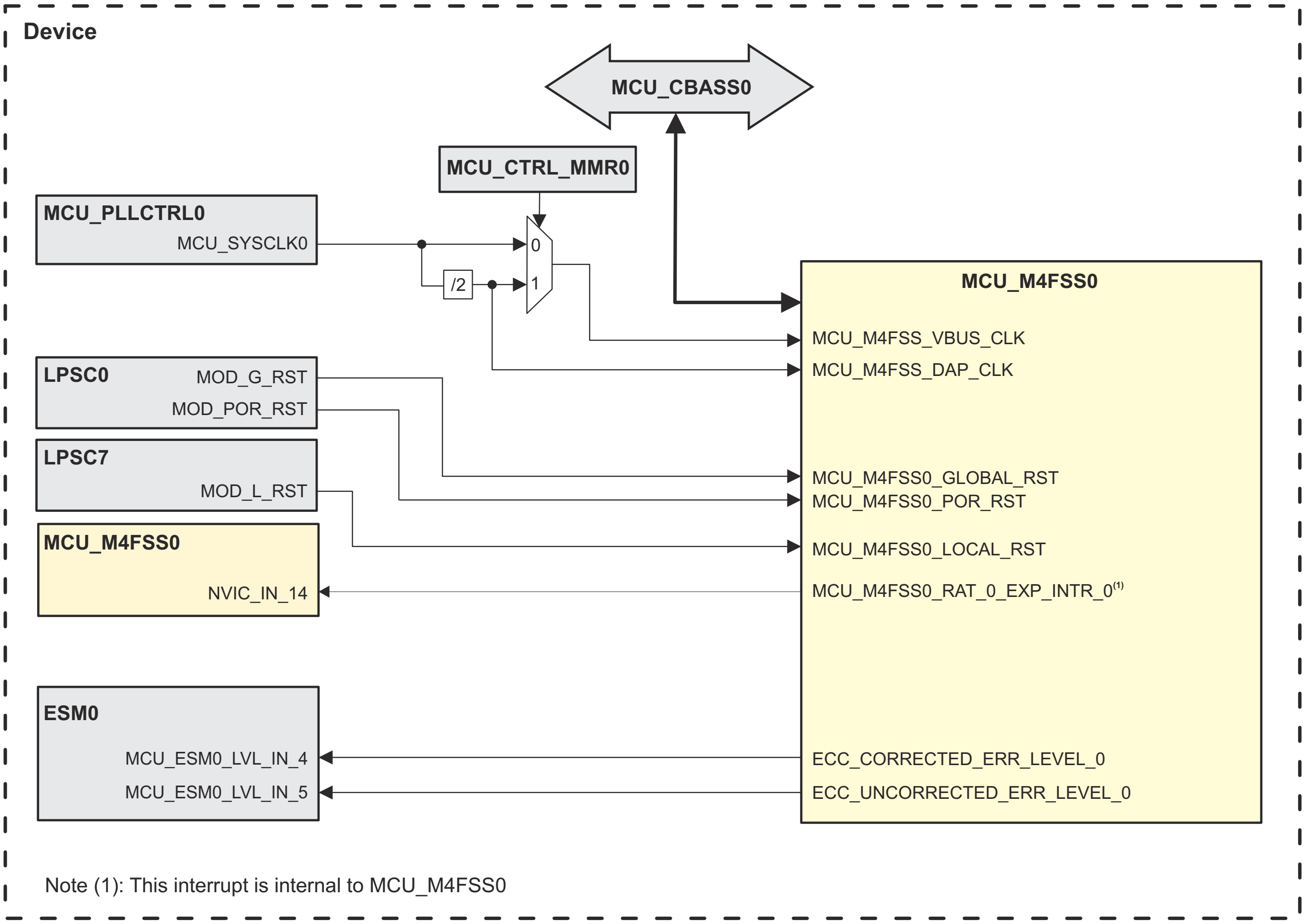

Figure 6-12. MCU_M4FSS0 Integration

Table 6-23. MCU_M4FSS0 Integration Attributes

Module Instance		Attributes			
		Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_M4FSS0	MCU_M4FSS0_CLUSTER	MCU_PSC0	PD0	LPSC0	MCU_CBASS0
	MCU_M4FSS0_CORE0	MCU_PSC0	PD1	LPSC7	MCU_CBASS0

Table 6-24. MCU_M4FSS0 Clocks and Resets

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
MCU_M4FSS0	MCU_M4FSS0_VBUS_CLK	MCU_SYSCLK0 or MCU_SYSCLK0/2[(1)]	MCU_PLLCTRL0	Main module clock that drive drives majority of blocks including M4F in functional mode.
	MCU_M4FSS0_DAP_CLK	MCU_SYSCLK0/2	MCU_PLLCTRL0	Module DAP clock.
Resets				

Table 6-24. MCU_M4FSS0 Clocks and Resets (continued)

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_M4FSS0	MCU_M4FSS0_POR_RST	MOD_POR_RST	LPSC0	Module POR reset
	MCU_M4FSS0_GLOBAL_RST	MOD_G_RST	LPSC0	Module global (main) reset
	MCU_M4FSS0_LOCAL_RST	MOD_L_RST	LPSC7	Module local reset (for M4F core)

(1) Clock selection is done during boot configuration by programming the MCU_M4FSS_CLKSEL register. This clock cannot be changed on the fly.

Table 6-25. MCU_M4FSS0 Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
MCU_M4FSS0	MCU_M4FSS0_RAT_0_EXP_INTR_0	MCU_M4FSS0_CORE0_NVIC_IN_14	MCU_M4FSS0	RAT exception error	Level
	MCU_M4FSS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_0	MCU_ESM0_LVL_IN_4	MCU_ESM0	ECC correctable error	Level
	MCU_M4FSS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_0	MCU_ESM0_LVL_IN_5	MCU_ESM0	ECC uncorrectable error	Level

---

Note

MCU_M4FSS interrupts are further described in Section 6.3.3.9 , *MCU_M4FSS Interrupts*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

6.3.3 MCU_M4FSS Functional Description

6.3.3.1 MCU_M4FSS Block Diagram

Figure 6-13 shows the MCU_M4FSS block diagram.

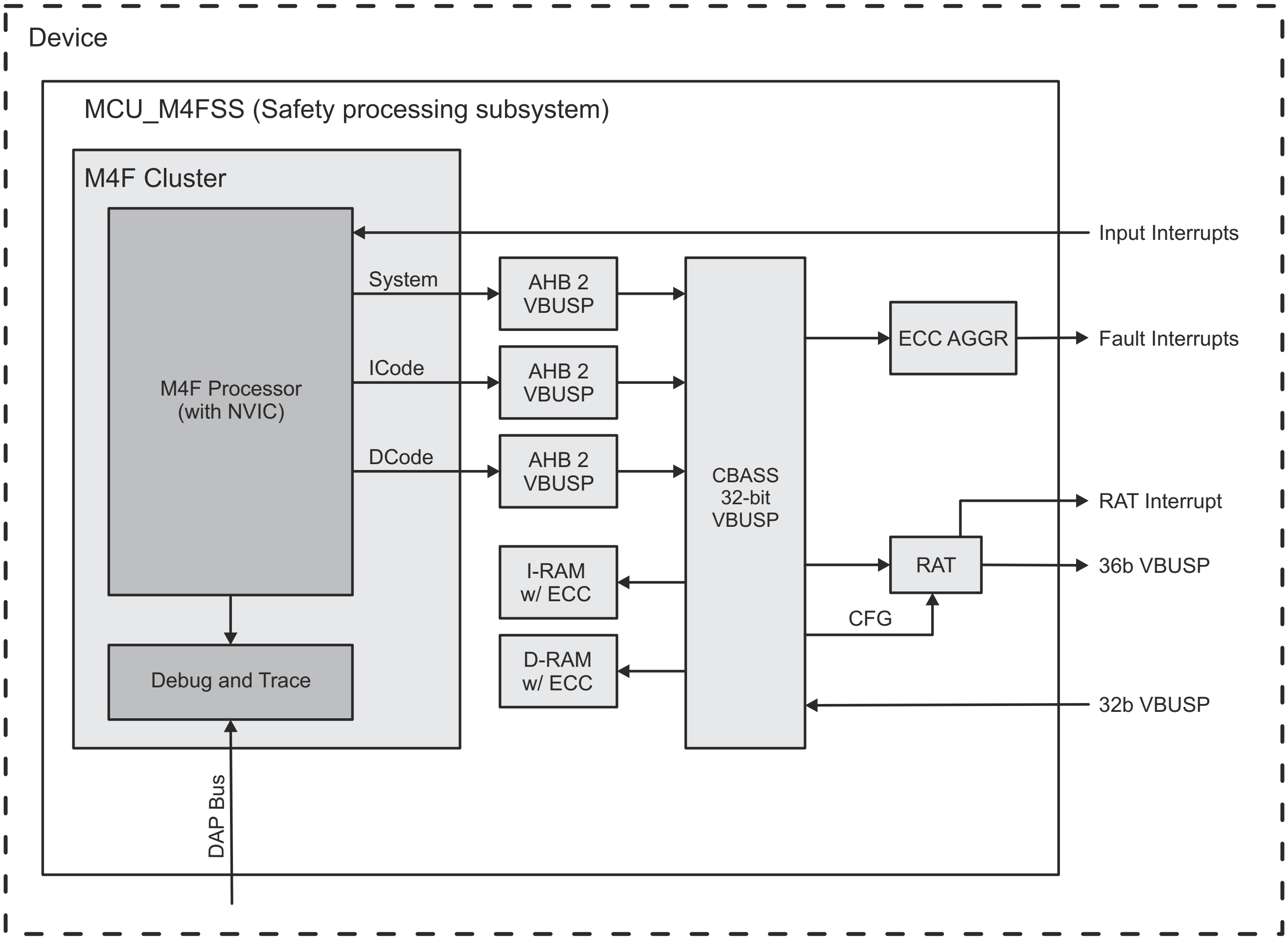

Figure 6-13. MCU_M4FSS Block Diagram

6.3.3.2 MCU_M4FSS Processor

The M4F is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require optimal interrupt response features. Some key features of the M4F processor core include:

- A subset of the Thumb instruction set, defined in the Armv7-M architecture
- Banked stack pointer (SP)
- Hardware integer divide instructions, SDIV and UDIV
- Handler and thread modes
- Thumb and debug states
- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency

A nested vectored interrupt controller (NVIC) is closely integrated with the processor core, to achieve low latency interrupt processing. NVIC features include:

- 64 external interrupts
- 3-bit priority (8 priority levels)
- Dynamic reprioritization of interrupts
- Priority grouping

  - This enables selection of preempting interrupt levels and non-preempting interrupt levels
- Support for tail-chaining and late arrival of interrupts
  - This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

The M4F processor also includes:

- Bus interfaces for memory access (ICode, DCode, system) and debug access (PPB APB)
- Memory protection unit (MPU)
- Various debug and trace units

For more details on the M4F processor, refer to the following documents:

- *Arm Cortex-M4 Processor Technical Reference Manual*
- *Arm Cortex-M4 Devices Generic User Guide*

6.3.3.3 MCU_M4FSS Internal RAMs

The MCU_M4FSS has a total of 256KB of SRAM divided into two banks: 192KB of I-RAM, and 64KB of D-RAM. The I-RAM memory is intended mainly for M4F's instruction code, and D-RAM for M4F's data. The M4F allows concurrent fetch for instruction code and data via dedicated buses (I-Code and D-Code, respectively).

The MCU_M4FSS supports unified memory for both banks (I-RAM and D-RAM), which means instruction code and data can be placed in any bank. In order to get optimal performance, it is highly recommend that instruction code be placed in I-RAM and data be placed in D-RAM; this allows the M4F to fetch in parallel instruction code and data from two different physical banks using two independent I-Code and D-Code buses. For instance, the D-RAM can be used to store instruction code in case the latter is spanning over the 192KB I-RAM.

Furthermore, the following applies:

- Both RAMs are organized in 32-bits words
- Both RAMs are initialized during reset - that is, there is no auto-initialization sequencing
- Both RAMs are ECC SECDED protected
  - Support for write-back upon single bit correction
- Data fetch is given higher priority over instruction fetch to avoid locking M4F

6.3.3.4 MCU_M4FSS Interfaces

6.3.3.5 MCU_M4FSS Power, Clocking and Reset

6.3.3.5.1 MCU_M4FSS Power

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCU_M4FSS0_CBASS_0	MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	LPSC_DMSC LPSC_MAIN2MCU LPSC_MCU_ALWAYSON
MCU_M4FSS0_CORE0	MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	LPSC_DMSC LPSC_MAIN2MCU LPSC_MCU_ALWAYSON
MCU_M4FSS0_CORTEX_M4F_SS_0	MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	LPSC_DMSC LPSC_MAIN2MCU LPSC_MCU_ALWAYSON

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCU_M4FSS0_DRAM_0	MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	LPSC_DMSC LPSC_MAIN2MCU LPSC_MCU_ALWAYSON
MCU_M4FSS0_ECC_AGGR_0	MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	LPSC_DMSC LPSC_MAIN2MCU LPSC_MCU_ALWAYSON
MCU_M4FSS0_IRAM_0	MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	LPSC_DMSC LPSC_MAIN2MCU LPSC_MCU_ALWAYSON
MCU_M4FSS0_RAT_0	MCU_PSC0	PD_M4F	LPSC_M4F	7	OFF	YES	LPSC_DMSC LPSC_MAIN2MCU LPSC_MCU_ALWAYSON

6.3.3.5.2 MCU_M4FSS Clocking

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_M4FSS0_CBASS_0	CLK	MCU_SYSCLK0	MCU_M4FSS_CLKSEL[0:0]	
		MCU_SYSCLK0/2	MCU_M4FSS_CLKSEL[0:0]	
MCU_M4FSS0_CORE0	DAP_CLK	MCU_SYSCLK0		MCU_M4FSS0_CORE0 Module DAP Clock
	VBUS_CLK	MCU_SYSCLK0	MCU_M4FSS_CLKSEL[0:0]	MCU_M4FSS0_CORE0 Main module clock that drives majority of blocks including M4F in functional mode.
		MCU_SYSCLK0/2	MCU_M4FSS_CLKSEL[0:0]	
MCU_M4FSS0_CORTEX_M4F_SS_0	DAP_CLK	MCU_SYSCLK0		MCU_M4FSS0_CORTEX_M4F_SS_0 Module DAP Clock
	VBUS_CLK	MCU_SYSCLK0	MCU_M4FSS_CLKSEL[0:0]	MCU_M4FSS0_CORTEX_M4F_SS_0 Main module clock that drives majority of blocks including M4F in functional mode.
		MCU_SYSCLK0/2	MCU_M4FSS_CLKSEL[0:0]	
MCU_M4FSS0_DRAM_0	CLK	MCU_SYSCLK0	MCU_M4FSS_CLKSEL[0:0]	
		MCU_SYSCLK0/2	MCU_M4FSS_CLKSEL[0:0]	
MCU_M4FSS0_ECC_AGGR_0	CLK	MCU_SYSCLK0	MCU_M4FSS_CLKSEL[0:0]	
		MCU_SYSCLK0/2	MCU_M4FSS_CLKSEL[0:0]	
MCU_M4FSS0_IRAM_0	CLK	MCU_SYSCLK0	MCU_M4FSS_CLKSEL[0:0]	
		MCU_SYSCLK0/2	MCU_M4FSS_CLKSEL[0:0]	

Module Instance	Module Clock Input	Source Clock	Source Control Register	Description
MCU_M4FSS0_RAT_0	CLK	MCU_SYSCLK0	MCU_M4FSS_CLKSEL[0:0]	
		MCU_SYSCLK0/2	MCU_M4FSS_CLKSEL[0:0]	

6.3.3.5.3 MCU_M4FSS Reset

Module Instance	Source	Description
MCU_M4FSS0	MCU_PSC0	MCU_M4FSS0 reset

6.3.3.6 MCU_M4FSS Memory View

The M4F processor has a fixed default memory map that provides up to 4GB of addressable memory. The predefined memory map allows the built-in peripherals, such as NVIC, MPU, SysTick and debug components, to be accessed by simple memory access instructions. Thus, most system features are accessible in program code. The M4F design has an internal bus infrastructure optimized for this memory usage.

The MCU_M4FSS memory map is presented in Chapter 2 , *Memory Map*. Note that bit-banding is not supported.

6.3.3.7 MCU_M4FSS RAT

The MCU_M4FSS uses a region-based address translation (RAT) to allow the M4F to access external memory space via initiator VBUSP port. Since the M4F processor can access only 2GB of space outside of MCU_M4FSS (0x6000_0000 to 0xDFFF_FFFF), this space can be mapped to a 36-bit address bus using the internal RAT module to give window view of external world. The MCU_M4FSS RAT is configured via target interface connected to the MCU_M4FSS internal CBASS interconnect. It supports 8 regions, with 4KB resolution each.

The full RAT functionality is described in Section 8.2 , *Region-based Address Translation (RAT) Module*.

6.3.3.7.1 Why RAT is needed for M4F

There are two reasons why Blazar M4F needs to have address remapping function to access some of the end points on the SoC side.

First of all, M4F has different memory map view compared to ARM MPU and DMA even within 32b address space. For example, M4F has some reserved address space at 0xE000_0000 to 0xFFFF_FFFF. However, this same address space is mapped to DDR data region. Table 6-26 summarizes the difference between Blazar native 32b address view vs the other SoC initiators such as ARM MPU and DMA view.

Table 6-26. Blazar M4F Address View

Memory Region Name	CortexM4 Start Address (32 bit)	CortexM4 End Address (32 bit)	Total Size	Description	SoC Controller View (36 b address)
I-RAM	0x0000_0000	0x0002_FFFF	192KB	Unified RAM embedded inside M4F subsystem	0x0500_0000
D-RaM	0x0003_0000	0x0003_FFFF	64KB	Unified RAM embedded inside M4F subsystem	0x0504_0000
Reserved	0x0004_0000	0x441F_FFFF		Reserved. Not implemented inside M4F subsystem	Not mapped on SoC side
RAT config	0x4420_0000	0x4420_0FFF	4KB	RAT config port (12-bits)	0x05FF_0000
Blazar ECC Aggregator	0x4420_1000	0x4420_13FF	1KB		0x05FF_1000
Reserved	0x4420_1400	0x5FFF_FFFF		Reserved. Not implemented inside M4F subsystem	Not mapped on SoC side
Memory Region external to M4F	0x6000_0000	0xDFFF_FFFF	~2GB	Can be mapped for CORTEX-M4 accesses outside of M4FE via RAT module	Can be mapped to any SoC memory region through RAT configuration
ITM	0xE000_0000	0xE000_0FFF	4KB	Only Visible by M4F core itself	Not accessible from Soc side

Table 6-26. Blazar M4F Address View (continued)

Memory Region Name	CortexM4 Start Address (32 bit)	CortexM4 End Address (32 bit)	Total Size	Description	SoC Controller View (36 b address)
DWT	0xE000_1000	0xE000_1FFF	4KB		
FBP	0xE000_2000	0xE000_2FFF	4KB		
SCS	0xE000_E000	0xE000_EFFF	4KB		
CTI	0xE004_2000	0xE004_2FFF	4KB		
NVIC config region	0xE000_E000	0xE000_E4EF	1.2KB		
ROM Table	0xE00F_F000				
Reserved	0xE010_0000	0xFFFF_FFFF			

Second, M4F is a micro controller with 32b address, which is only able to access up to 4GB address space. However, Sitara SoC supports 36b address and there are end points such as some of the flash is located at upper 4GB address space. M4F’s native 32b address map is not able to access those flash regions without address remapping function. Figure 6-14 shows the SoC 36b memory map.

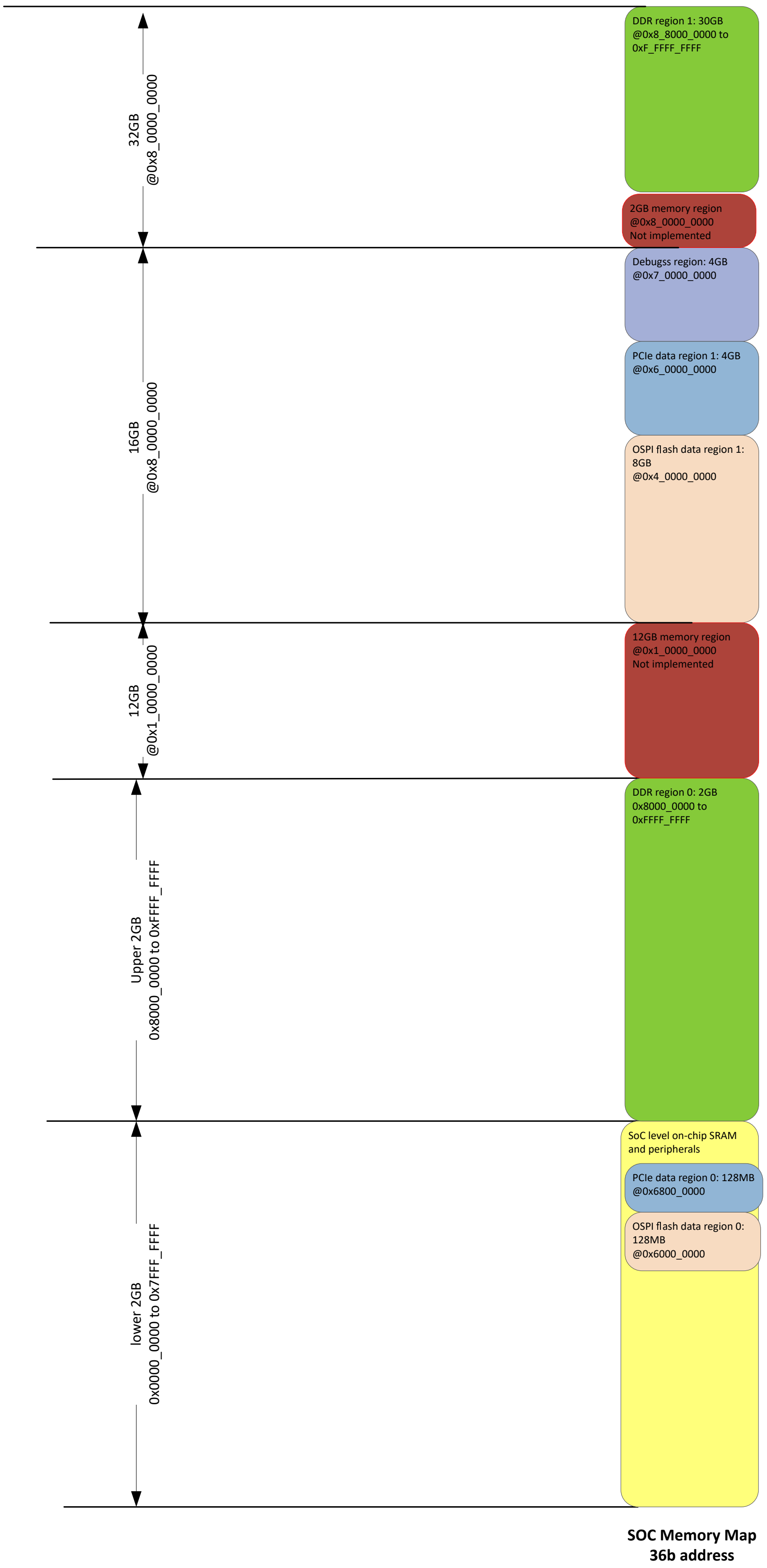

Figure 6-14. Typical Sitara SoC Memory Map View (36b address)

RAT block enables M4F core to have full access on the SoC memory map including the memory region at and above 0x1_0000_0000.

6.3.3.7.2 RAT Function

RAT block is responsible to do a region based address translation. For each region, user can define the starting address and size of the region and remapping the transactions to use a new address range. The starting address and region size need to be aligned. For example, if the region size is 16KB, the starting address for that region needs to be 16KB aligned. And region size should be minimum 4KB or larger to avoid transactions cross the region boundaries. Each RAT block supports multiple programmable regions. And it is important that those regions are not overlapping with each other.

Each RAT block supports multiple programmable regions and it is important that those regions are not overlapping with each other.

Table 6-27 shows the register definition for RAT module.

Table 6-27. RAT Module Register Definitions

Address Offset	Register Mnemonic	Register Name
0x0	PID	Revision Register
0x4	CONFIG	Config Register
0x20+(a*0x10), a=0..15	REGION[a]_CTRL	Region Control Register
0x20+(a*0x10)+0x4, a=0..15	REGION[a]_BASE	Region Base Register
0x20+(a*0x10)+0x8, a=0..15	REGION[a]_TRANS_L	Region Translated Lower Address
0x20+(a*0x10)+0xc, a=0..15	REGION[a]_TRANS_U	Region Translated Upper Address
0x804	DESTINATION_ID	Destination ID Register
0x820	EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register
0x824	EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register
0x828	EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register
0x82c	EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register
0x830	EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register
0x834	EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register
0x838	EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register
0x840	EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register
0x844	EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register
0x848	EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register
0x84c	EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register
0x850	EOI_REG	EOI Register

The PID Register contains the major and minor revisions for the module.

Table 6-28. PID Register (Offset = 0x0)

Bit	Name	Type	Reset	Description
31:30	scheme	r	0x1	PID register scheme
29:28	bu	r	0x2	Business Unit: 10 = Processors
27:16	func	r	0x680	Module ID
15:11	rtl	r	0x8	RTL revision. Will vary depending on release.
10:8	major	r	0x1	Major revision
7:6	custom	r	0x0	Custom

Table 6-28. PID Register (Offset = 0x0) (continued)

Bit	Name	Type	Reset	Description
5:0	minor	r	0x0	Minor revision

The CONFIG Register contains the configuration values for the module.

Table 6-29. CONFIG Register (Offset = 0x4)

Bit	Name	Type	Reset	Description
31:24	reserved	r	0x0	Reserved
23:16	addr_width	r	0x30	Number of address bits
15:8	addrs	r	0x1	Number of addresses
7:0	regions	r	0x10	Number of regions

REGION[a]_CTRL defines the Control for Region a.

Table 6-30. REGION[a]_CTRL Register (Offset = 0x20 + (a * 0x10))

Bit	Name	Type	Reset	Description
31	en	rw	0x0	Enable for the Region
30:6	reserved	r	0x0	Reserved
5:0	size	rw	0x0	Size of the Region in Address Bits. 0 = 1 byte, 1 = 2B, 2 = 4B, 3 = 8B, etc. up to 32 = 4GB.

REGION[a]_BASE Register defines the Base Address for Region a. This is the source address for matching to a region.

Table 6-31. REGION[a]_BASE Register (Offset = 0x20 + (a * 0x10))

Bit	Name	Type	Reset	Description
31:0	base	rw	0x0	Base Address for the Region. It must be aligned to the programmed size.

REGION[a]_TRANS_L Register defines the Translated Lower Address Bits for Region A.

Table 6-32. REGION[a]_TRANS_L Register ((Offset = 0x20 + (a * 0x10) + 0x8); a = 0..15)

Bit	Name	Type	Reset	Description
31:0	lower	rw	0x0	Translated Lower Address Bits for the Region. It must be aligned to the programmed size.

REGION[a]_TRANS_U Register defines the Translated Upper Address Bits for Region a.

Table 6-33. REGION[a]_TRANS_U Register (Offset = 0x20 + (a * 0x10) + 0xC)

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	upper	rw	0x0	Translated Upper Address Bits for the Region

DESTINATION_ID Register defines the destination ID for error messages.

Table 6-34. DESTINATION_ID Register (Offset = 0x804)

Bit	Name	Type	Reset	Description
31:8	reserved	r	0x0	Reserved
7:0	dest_id	rw	0x0	The destination ID.

The EXCEPTION_LOGGING_CONTROL Register controls the exception logging.

Table 6-35. EXCEPTION_LOGGING_CONTROL Register (Offset = 0x820)

Bit	Name	Type	Reset	Description
31:2	reserved	r	0x0	Reserved
1	disable_intr	rw	0x0	Disables logging interrupt when set. This will not disable logging, so if cleared the current log should also be cleared to guarantee the next log generates the interrupt.
0	disable_f	rw	0x0	Disables logging when set. This will also disable interrupts.

The EXCEPTION_LOGGING_HEADER0 Register contains the first word of the header.

Table 6-36. EXCEPTION_LOGGING_HEADER0 Register (Offset = 0x824)

Bit	Name	Type	Reset	Description
31:24	type_f	r	0x0	Type. 4 = RAT.
23:8	src_id	r	0x0	Source ID.
7:0	dest_id	r	0x0	Destination ID.

The EXCEPTION_LOGGING_HEADER1 Register contains the second word of the header.

Table 6-37. EXCEPTION_LOGGING_HEADER1 Register (Offset = 0x828)

Bit	Name	Type	Reset	Description
31:24	group	r	0x0	Group.
23:16	code	r	0x0	Code. 1 = Boundary crossing error.
15:0	reserved	r	0x0	Reserved

The EXCEPTION_LOGGING_DATA0 Register contains the first word of the data.

Table 6-38. EXCEPTION_LOGGING_DATA0 Register (Offset = 0x82C)

Bit	Name	Type	Reset	Description
31:0	addr_l	r	0x0	Address lower 32 bits.

The EXCEPTION_LOGGING_DATA1 Register contains the second word of the data.

Table 6-39. EXCEPTION_LOGGING_DATA1 Register (Offset = 0x830)

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	addr_h	r	0x0	Address upper 12 bits.

The EXCEPTION_LOGGING_DATA2 Register contains the third word of the data.

Table 6-40. EXCEPTION_LOGGING_DATA2 Register (Offset = 0x834)

Bit	Name	Type	Reset	Description
31:28	reserved	r	0x0	Reserved
27:16	routeid	r	0x0	Route ID.
15:14	reserved	r	0x0	Reserved
13	write	r	0x0	Write.
12	read	r	0x0	Read.
11	debug	r	0x0	Debug.
10	cacheable	r	0x0	Cacheable.
9	priv	r	0x0	Priv.
8	secure	r	0x0	Secure.
7:0	priv_id	r	0x0	Priv ID.

The EXCEPTION_LOGGING_DATA3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

Table 6-41. EXCEPTION_LOGGING_DATA3 Register (Offset = 0x838)

Bit	Name	Type	Reset	Description
31:10	reserved	r	0x0	Reserved
9:0	bytecnt	r	0x0	Byte count.

The EXCEPTION_PEND_SET Register allows to set the pend signal.

Table 6-42. EXCEPTION_PEND_SET Register (Offset 0x840)

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	pend_set	rw1ts	0x0	Write a 1 to set the exception pend signal.

The EXCEPTION_PEND_CLEAR Register allows to clear the pend signal.

Table 6-43. EXCEPTION_PEND_CLEAR Register (Offset = 0x844)

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	pend_clr	rw1tc	0x0	Write a 1 to clear the exception pend signal.

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

Table 6-44. EXCEPTION_ENABLE_SET Register (Offset = 0x848

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	enable_set	rw1ts	0x0	Write a 1 to set the exception interrupt enable signal.

The EXCEPTION_ENABLE_CLEAR Registerr allows to clear the interrupt enable signal.

Table 6-45. EXCEPTION_ENABLE_CLEAR Register (Offset = 0x84C)

Bit	Name	Type	Reset	Description
31:1	reserved	r	0x0	Reserved
0	enable_clr	rw1tc	0x0	Write a 1 to clear the exception interrupt enable signal.

EOI_REG Register defines the EOI Register.

Table 6-46. EOI_REG Register (Offset 0x850)

Bit	Name	Type	Reset	Description
31:16	reserved	r	0x0	Reserved
15:0	eoi_wr	rw	0x0	EOI Register

RAT block is by default disabled, which means RAT block does not do address remapping. The 32b address coming from M4F core is directly sent out to the SoC level. The user can program each RAT remapping region individually. For the transactions does not hit any remapping region, RAT block just simply forwards the transactions to the SoC level with its original address.

6.3.3.7.3 How to use RAT Block in Blazar M4F

Table 6-47 shows the default M4F 32b memory map view. Without enabling RAT function, M4F can’t access majority of the peripherals on the SoC level. From M4F point of view, only the address 0x6000_0000 to 0xDFFF_FFFF are sent to SoC level. Without RAT remapping the address, those transactions can only access various memory end points, such as flash, on-chip SRAM and DDR. In addition, M4F is not able to access the following memory region since these are beyond 4GB address space.

- DDR’s data space beyond 32b address, basically upper DDR data space beyond 2GB
- PCIe data space beyond 32b address
- OSPI data space beyond 32b address
- Debug configuration region

The RAT block for Blazar M4F supports 16 regions and there are many different ways to program those regions. It is recommended to configure the first 4 RAT regions to allow M4F access majority of the peripherals in the SoC and use the rest 12 regions to program the access to various memory end points based on the need.

Table 6-47. Recommended RAT Config

	Base	Size	translated address	Address remapping
RAT region 0	0x6000_0000	256MB	0x0000_0000	Re-map the address range from 0x6000_0000 to 0x6FFF_FFFF to 0x0000_0000 to 0x0FFF_FFFF
RAT region 1	0x7000_0000	256MB	0x2000_0000	Re-map the address range from 0x7000_0000 to 0x7FFF_FFFF to 0x2000_0000 to 0x2FFF_FFFF
RAT region 2	0x8000_0000	256MB	0x3000_0000	Re-map the address range from 0x8000_0000 to 0x8FFF_FFFF to 0x3000_0000 to 0x3FFF_FFFF
RAT region 3	0x9000_0000	256MB	0x4000_0000	Re-map the address range from 0x9000_0000 to 0x9FFF_FFFF to 0x4000_0000 to 0x4FFF_FFFF
RAT region 4	0xA000_0000	2MB	0x7000_0000	Re-map the M4F address range from 0x9000_0000 to 0x901F_FFFF to 0x7000_0000 to 0x701F_FFFF (on-chip SRAM)

M4F can use address 0xA000_0000 to 0xDFFF_FFFF to access various memory end point on the SoC level such as:

- GPMC
- OSPI flash
- DDR
- DebugSS config region
- PCIe data region

But due to the limitation of the M4F 32b address window, it is not possible that M4F access the full SoC address map at the same time. The above RAT configuration can guarantee that M4F can access all the peripherals in SoC, but it has limited access to the memory end point. User can partition the M4F address window and only program RAT configuration to allow M4F accessing a limited memory region based on need.

6.3.3.8 MCU_M4FSS ECC Support

The MCU_M4FSS includes an ECC aggregator module that combines ECC errors from various local sources, such as RAMs, interconnects and bridges. Table 6-48 provides the mapping of ECC errors within the MCU_M4FSS ECC aggregator. Two separate interrupts are generated for ECC error: correctable and non-correctable.

The full ECC aggregator functionality is described in Section 12.6.4 , *ECC Aggregator*.

Table 6-48. "Fault Detected" Interrupt Mapping for MCU_M4FSS ECC Aggregator

Interrupt Number (RAM ID)	Source
0	Iram_ramecc_pend
1	dram_ramecc_pend
2	Iram_busecc_pend
3	dram_busecc_pend

Table 6-48. "Fault Detected" Interrupt Mapping for MCU_M4FSS ECC Aggregator (continued)

Interrupt Number (RAM ID)	Source
4	blazar_rat_edc_ctrl_busecc_pend
5	blazar_cbass_vbusp_s_p2p_bridge_vbusp_s_bridge_busecc_pend
6	blazar_cbass_lecc_s_p2p_bridge_lecc_s_bridge_busecc_pend
7	blazar_cbass_blazar_scr_scr_blazar_cbass_blazar_scr_scr_edc_ctrl_busecc_pend
8	blazar_cbass_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
9	blazar_sys_scr_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
10	blazar_la2v_i_edc_ctrl_busecc
11	blazar_la2v_d_edc_ctrl_busecc
12	blazar_la2v_s_edc_ctrl_busecc

6.3.3.9 MCU_M4FSS Interrupts

All interrupts that are generated by the M4FSS are summarized in Table 6-49, along with their mapping.

Table 6-49. MCU_M4FSS0_CORE0_INTERRUPT_MAP Memory Map

Interrupt Input Line	Interrupt ID	Source Interrupt
MCU_M4FSS0_CORE0_NVIC_IN_0	0	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_4
MCU_M4FSS0_CORE0_NVIC_IN_1	1	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_5
MCU_M4FSS0_CORE0_NVIC_IN_2	2	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_6
MCU_M4FSS0_CORE0_NVIC_IN_3	3	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_7
MCU_M4FSS0_CORE0_NVIC_IN_4	4	MCU_TIMER0_INTR_PEND_0
MCU_M4FSS0_CORE0_NVIC_IN_5	5	MCU_TIMER1_INTR_PEND_0
MCU_M4FSS0_CORE0_NVIC_IN_6	6	MCU_TIMER2_INTR_PEND_0
MCU_M4FSS0_CORE0_NVIC_IN_7	7	MCU_TIMER3_INTR_PEND_0
MCU_M4FSS0_CORE0_NVIC_IN_8	8	MCU_MASTER_SAFETY_GASKET0_TIMED_OUT_0
MCU_M4FSS0_CORE0_NVIC_IN_9	9	GLUELOGIC_MAINRESET_REQUEST_GLUE_MAIN_RESETZ_SYNC_STRETCH_0
MCU_M4FSS0_CORE0_NVIC_IN_10	10	GLUELOGIC_MAINRESET_REQUEST_GLUE_MAIN_PORZ_SYNC_STRETCH_0
MCU_M4FSS0_CORE0_NVIC_IN_11	11	MCU_ESM0_ESM_INT_CFG_LVL_0
MCU_M4FSS0_CORE0_NVIC_IN_12	12	MCU_ESM0_ESM_INT_HI_LVL_0
MCU_M4FSS0_CORE0_NVIC_IN_13	13	MCU_ESM0_ESM_INT_LOW_LVL_0
MCU_M4FSS0_CORE0_NVIC_IN_14	14	MCU_M4FSS0_RAT_0_EXP_INTR_0
MCU_M4FSS0_CORE0_NVIC_IN_15	15	VTM0_THERM_LVL_GT_TH1_INTR_0
MCU_M4FSS0_CORE0_NVIC_IN_16	16	MCU_MCRC64_0_INT_MCRC_0
MCU_M4FSS0_CORE0_NVIC_IN_17	17	MCU_I2C0_POINTRPEND_0
MCU_M4FSS0_CORE0_NVIC_IN_18	18	MCU_I2C1_POINTRPEND_0
MCU_M4FSS0_CORE0_NVIC_IN_19	19	MCU_RTI0_INTR_WWD_0
MCU_M4FSS0_CORE0_NVIC_IN_20	20	MCU_PSC0_PSC_ALLINT_0
MCU_M4FSS0_CORE0_NVIC_IN_21	21	MCU_TIMEOUT0_TRANS_ERR_LVL_0
MCU_M4FSS0_CORE0_NVIC_IN_22	22	MCU_MCSPI0_INTR_SPI_0
MCU_M4FSS0_CORE0_NVIC_IN_23	23	MCU_MCSPI1_INTR_SPI_0
MCU_M4FSS0_CORE0_NVIC_IN_24	24	MCU_UART0_USART_IRQ_0
MCU_M4FSS0_CORE0_NVIC_IN_25	25	MCU_UART1_USART_IRQ_0
MCU_M4FSS0_CORE0_NVIC_IN_26	26	DMSC0_CORTEX_M3_0_SEC_OUT_0

Table 6-49. MCU_M4FSS0_CORE0_INTERRUPT_MAP Memory Map (continued)

Interrupt Input Line	Interrupt ID	Source Interrupt
MCU_M4FSS0_CORE0_NVIC_IN_27	27	DMSC0_CORTEX_M3_0_SEC_OUT_1
MCU_M4FSS0_CORE0_NVIC_IN_28	28	MCU_DCC0_INTR_DONE_LEVEL_0
MCU_M4FSS0_CORE0_NVIC_IN_29	29	DDPA0_DDPA_INTR_0
MCU_M4FSS0_CORE0_NVIC_IN_30	30	VTM0_THERM_LVL_GT_TH2_INTR_0
MCU_M4FSS0_CORE0_NVIC_IN_31	31	MCU_CBASS0_DEFAULT_ERR_INTR_0
MCU_M4FSS0_CORE0_NVIC_IN_32	32	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_168
MCU_M4FSS0_CORE0_NVIC_IN_33	33	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_169
MCU_M4FSS0_CORE0_NVIC_IN_34	34	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_170
MCU_M4FSS0_CORE0_NVIC_IN_35	35	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_171
MCU_M4FSS0_CORE0_NVIC_IN_36	36	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_172
MCU_M4FSS0_CORE0_NVIC_IN_37	37	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_173
MCU_M4FSS0_CORE0_NVIC_IN_38	38	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_174
MCU_M4FSS0_CORE0_NVIC_IN_39	39	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_175
MCU_M4FSS0_CORE0_NVIC_IN_40	40	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_176
MCU_M4FSS0_CORE0_NVIC_IN_41	41	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_177
MCU_M4FSS0_CORE0_NVIC_IN_42	42	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_178
MCU_M4FSS0_CORE0_NVIC_IN_43	43	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_179
MCU_M4FSS0_CORE0_NVIC_IN_44	44	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_180
MCU_M4FSS0_CORE0_NVIC_IN_45	45	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_181
MCU_M4FSS0_CORE0_NVIC_IN_46	46	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_182
MCU_M4FSS0_CORE0_NVIC_IN_47	47	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_183
MCU_M4FSS0_CORE0_NVIC_IN_48	48	DMSC0_AES_0_HIB_PUBLIC_0
MCU_M4FSS0_CORE0_NVIC_IN_49	49	DMSC0_AES_0_HIB_SECURE_0
MCU_M4FSS0_CORE0_NVIC_IN_50	50	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_0
MCU_M4FSS0_CORE0_NVIC_IN_51	51	PRU_ICSSG0_PR1_HOST_INTR_PEND_6
MCU_M4FSS0_CORE0_NVIC_IN_52	52	PRU_ICSSG0_PR1_HOST_INTR_PEND_7
MCU_M4FSS0_CORE0_NVIC_IN_53	53	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_0
MCU_M4FSS0_CORE0_NVIC_IN_54	54	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_0
MCU_M4FSS0_CORE0_NVIC_IN_55	55	VTM0_THERM_LVL_LT_TH0_INTR_0
MCU_M4FSS0_CORE0_NVIC_IN_56	56	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_3
MCU_M4FSS0_CORE0_NVIC_IN_57	57	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_3
MCU_M4FSS0_CORE0_NVIC_IN_58	58	CTRL_MMR0_ACCESS_ERR_0
MCU_M4FSS0_CORE0_NVIC_IN_59	59	PADCFG_CTRL0_ACCESS_ERR_0
MCU_M4FSS0_CORE0_NVIC_IN_60	60	MCU_PADCFG_CTRL0_ACCESS_ERR_0
MCU_M4FSS0_CORE0_NVIC_IN_61	61	MCU_CTRL_MMR0_ACCESS_ERR_0
MCU_M4FSS0_CORE0_NVIC_IN_62	62	PRU_ICSSG1_PR1_HOST_INTR_PEND_6
MCU_M4FSS0_CORE0_NVIC_IN_63	63	PRU_ICSSG1_PR1_HOST_INTR_PEND_7

6.3.3.10 MCU_M4FSS Debug and Trace

The MCU_M4FSS supports the following debug and trace features:

- Full debug, including data matching for watchpoint generation
- Full trace, including ITM, ETM and DWT
  - HTM port is not present
  - TPIU is not present
- DAP interface

- ITM and ETM interfaces
- CTM crossbar to map CTI triggers to CTM channels through a CS_CTI module
- Debug infrastructure is reset with POR reset

6.3.3.11 MCU_M4FSS Time Sync

The MCU_M4FSS supports a 48-bit input interface for synchronizing to the global time counter (GTC). The 48-bit timestamp can be appended with ITM messages. Timestamping is a mechanism whereby a global timestamp value is periodically inserted at strategic locations into the trace stream. Timestamps can be used to correlate trace from various sources. Each trace source samples the timestamp value and inserts it as an absolute value into the trace stream.

The global timestamp value coming to the MCU_M4FSS is gray-encoded. It is then internally converted to its binary value.

For more details on the device time synchronization, refer to the following sections:

- *Global Timebase Counter (GTC)*
- *Time Sync*

6.3.3.12 MCU_M4FSS SysTick

The MCU_M4FSS includes a 24-bit count-down system timer (SysTick) that can be used as a real time operating system (RTOS) tick timer or as a simple counter. The MCU_M4FSS_SYSTICK register in the MCU_CTRL_MMR module provides the calibration settings required for proper SysTick operation.

6.3.3.13 MCU_M4FSS Initialization

The MCU_M4FSS has a local reset input. This input is driven by PSC, but controlled by software (PSC MMRs, with programmable default state). This local reset resets just the M4F processor. When the PSC (controlled by software) brings the MCU_M4FSS out of reset, the M4F CPU is held in reset through this local reset, but everything else will be running (except debug logic). This allows to pre-load the RAMs in the MCU_M4FSS. Software then releases the local reset and M4F starts executing the pre-loaded code in the RAMs.

Software can repeat the initialization process over and over by following these steps:

1. Execute WFI instruction
2. Transition MCU_M4FSS to a DISABLE/OFF state through PSC (PSC will wait for MCU_M4FSS to be IDLE which includes MCU_M4FSS asserting WFI)
3. Transition MCU_M4FSS to an ENABLE/ON state through PSC (local reset will be held asserted)
4. Pre-load RAMs
5. Release local reset

6.4 Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)

This section describes the Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG) in the AM64 device.

6.4.1 PRU_ICSSG Overview

The Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU_ICSSG) consists of:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1)
- Two auxiliary 32-bit load/store RISC CPU cores — Auxiliary Programmable Real-Time Units (RTU_PRU0 and RTU_PRU1)
- Two 32-bit load/store RISC CPU cores — Transmit Programmable Real-Time Units (TX_PRU0 and TX_PRU1)
- Data RAMs per PRU core
- Instruction RAMs per PRU, per RTU_PRU and per TX_PRU cores
- Shared RAM
- Peripheral modules: UART0, ECAP0, PWM, IEP0 and IEP1
- Interrupt controller (INTC) and Task Manager per core

The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The PRU cores are programmed with a small, deterministic instruction set. Each PRU can operate independently or in coordination with each other and can also work in coordination with the device-level host CPU. This interaction between processors is determined by the nature of the firmware loaded into the PRU’s instruction memory.

Table 6-50 shows the PRU_ICSSG systems allocation within device domains.

Table 6-50. PRU_ICSSG Allocation within Device Domains

Module Instance	**Domain**	
	MCU	**MAIN**
PRU_ICSSG0	-	✓
PRU_ICSSG1	-	✓

PRU_ICSSG Overview shows an overview of the PRU_ICSSG subsystem.

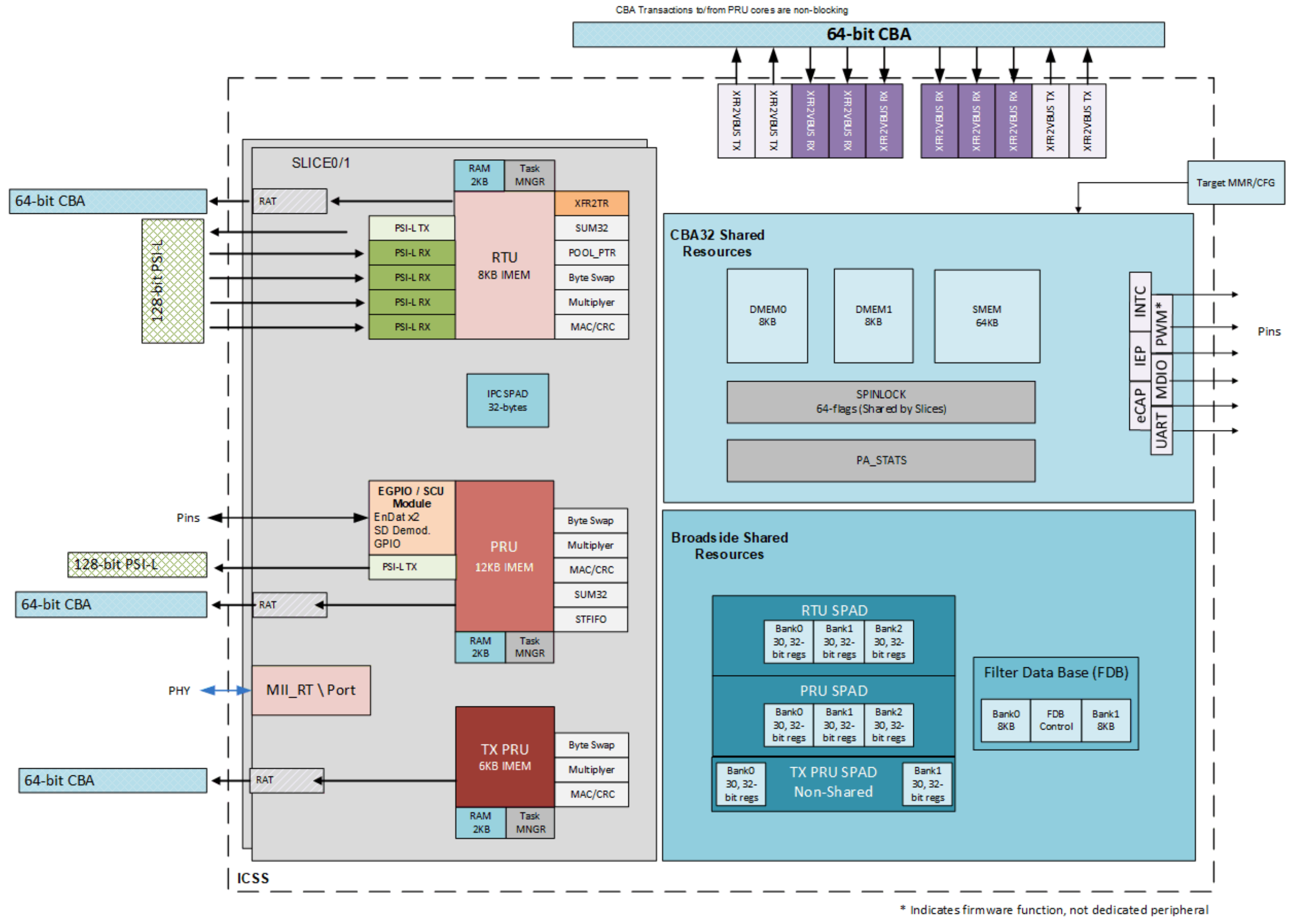

Figure 6-15. PRU_ICSSG Overview

6.4.1.1 PRU_ICSSG Key Features

The PRU_ICSSG subsystem includes the following main features:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1), each with:
  - 20 Enhanced General-Purpose Inputs (EGPI) and 20 Enhanced General-Purpose Outputs (EGPO)
  - Asynchronous capture [Serial Capture Unit (SCU)] with EnDat 2.2 protocol and Sigma-Delta demodulation support
  - 12KB program memory per PRU (PRU0_IRAM and PRU1_IRAM) with ECC
  - 2KB Broadside (BS) RAM
  - MAC (Multiplier with optional Accumulation)
  - CRC16/CRC32 hardware accelerator
  - Byte Swap, for Little/Big Endian conversion
  - SUM32 Hardware accelerator for UDP checksum
  - Task Manager (Preemption support)
  - Broadside (32 Byte) connection to MII_G_RTn (where n = 1 or 2), Filter Data Base (FDB), IPC SPAD Memory, Scratchpad Memory (SPAD), SPINLOCK, XFR2VBUS, RTU_PRUm and TX_PRUm (where m = 0 or 1)
- Two auxiliary Real-Time Transfer Units (RTU_PRU0 and RTU_PRU1), each with:
  - 8KB program memory with ECC
  - 2KB Broadside (BS) RAM
  - MAC (Multiplier with optional Accumulation)
  - CRC16/CRC32 Hardware accelerator

  - Byte Swap, for Little/Big Endian conversion
  - SUM32 Hardware accelerator for UDP checksum
  - Task Manager (Preemption support)
  - XFR2TR, for accelerating the internal memory copy of worklist from TRs (Transfer Requests)
  - Broadside (32 Byte) connection to MII_G_RTn (where n = 1 or 2), Filter Data Base (FDB), IPC SPAD Memory, Scratchpad Memory (SPAD), SPINLOCK, XFR2VBUS, PRUm and TX_PRUm (where m = 0 or 1)
- Two Transmit Real-Time Transfer Units (TX_PRU0 and TX_PRU1), each with:
  - 6KB program memory with ECC
  - 2KB Broadside (BS) RAM
  - MAC (Multiplier with optional Accumulation)
  - CRC16/CRC32 Hardware accelerator
  - Byte Swap, for Little/Big Endian conversion
  - Task Manager (Preemption support)
  - Broadside (32 Byte) connection to the TX L2 FIFO of MII_G_RTn port (where n = 1 or 2), TX_PRU Scratchpad Memory (SPAD), SPINLOCK, XFR2VBUS, PRUm and RTU_PRUm (where m= 0 or 1)
- Scratchpad Memory (SPAD) with 8 banks of 30 × 32-bit registers:
  - 3 banks for the PRU0 and PRU1 cores
  - 3 banks for the RTU_PRU0 and RTU_PRU1 cores
  - 2 banks for the TX_PRU0 and TX_PRU1 cores
- 64 KB Shared general purpose memory RAM with ECC (Data RAM2), shared between PRU0 and PRU1
- Two 8 KB (shared) Data Memories with ECC (Data RAM0 and Data RAM1)
- 64-bit VBUSM Controller Port:
  - Optional address translation for all transactions to External Host
- 16 Software Events generated by 2 PRUs
- Two Real-Time Ethernet ports (MII_G_RT1 and MII_G_RT2) configurable to connect to each PRUn (where n = 0 or 1) to support multiple industrial communication protocols.
  - Each of the Ethernet ports can be configured as MII/RGMII/SGMII ports
  - **NOTE: SGMII mode is not supported in this device.**
  - RX Classifier per port
- Two Industrial Ethernet Peripheral's (IEP0/IEP1) to manage/generate Industrial Ethernet functions such as time stamping.
  - Each of the Industrial Ethernet 64-bit timers support 10 capture and 16 compare events along with slow and fast compensation.
  - Supports up to 4 sets of 3-phased motor control with 12 primary and 12 complimentary programmable PWM outputs.
  - Up to 9 safety events with optional external trip IO per PWM set with hardware glitch filter.
- One MDIO port to control external Ethernet PHY
- One Enhanced Capture Module (ECAP0)
- 16550-compatible UART with a dedicated 192-MHz clock to support 12-Mbps PROFIBUS
- Interrupt Controller (INTC)
  - Up to 64 internal events, generated by modules, internal to the PRU_ICSSG
  - Up to 96 external events, generated by the system
  - Supports up to 20 interrupt channels
  - Generation of 20 Host interrupts:
    - 2 Host interrupts to PRU0, PRU1, TX_PRU0 and TX_PRU1
    - 2 Host interrupts to RTU_PRU0 and RTU_PRU1
    - 8 Host interrupts, exported from the PRU_ICSSG for signaling the Arm interrupt controllers (pulse and level provided)
    - 8 Host Interrupts for the Task Managers
  - Each system event can be enabled and disabled
  - Each host event can be enabled and disabled
  - Hardware prioritization of events
- One 32-bit VBUSP target port for memory mapped register and internal memories access

- Flexible power management support
- Integrated 32-bit Interconnect

6.4.1.2 Not Supported Features

The following PRU_ICSSG features are not supported:

- Only 4 of the IEP0 (and none of the IEP1) Ethernet Digital Data Input/Output's of each PRU_ICSSG are pinned out
- UART Modem interface (DTR, DSR, and RI) is not supported
- The following features are not supported for PRU_ICSSG0 and PRU_ICSSG1:
  - 12 Enhanced General-Purpose Inputs (pr<0/1>_pru0_r31_in[31:20]) are not pinned out
  - 12 Enhanced General-Purpose Outputs (pr<0/1>_pru0_r31_out[31:20]) are not pinned out
  - SGMII mode is not supported on PRU_ICSSG0 and PRU_ICSSG1

6.4.2 PRU_ICSSG Environment

The PRU_ICSSG[1-0] modules are hereinafter referred to as PRU_ICSSG module

This section describes the PRU_ICSSG external connections (environment).

6.4.2.1 PRU_ICSSG Internal Pinmux

The PRU_ICSSG0 and PRU_ICSSG1 external interface signals are described in Table 6-51 and Figure 6-17, Figure 6-18, respectively. The PRU_ICSSG has a large number of available I/O signals. Most of these are multiplexed with other functional signals at the device level.

The PRU_ICSSG0 and PRU_ICSSG1 also support an internal wrapper multiplexing that expands the device top-level multiplexing. This wrapper multiplexing is controlled by the GPCFGx_REG register (where x = 0 or 1) in the PRU_ICSSG CFG register space and allows MII_RT, 3 channel Peripheral Interface (with EnDAT capabilities), and Sigma Delta functionality to be muxed with the PRU GPI/O device signals, as shown in Figure 6-16. The PRU_ICSSG wrapper multiplexing is described with the device-level signals in Table 6-51. Note that the device top-level muxing has higher priority over the internal PRU_ICSSG muxing.

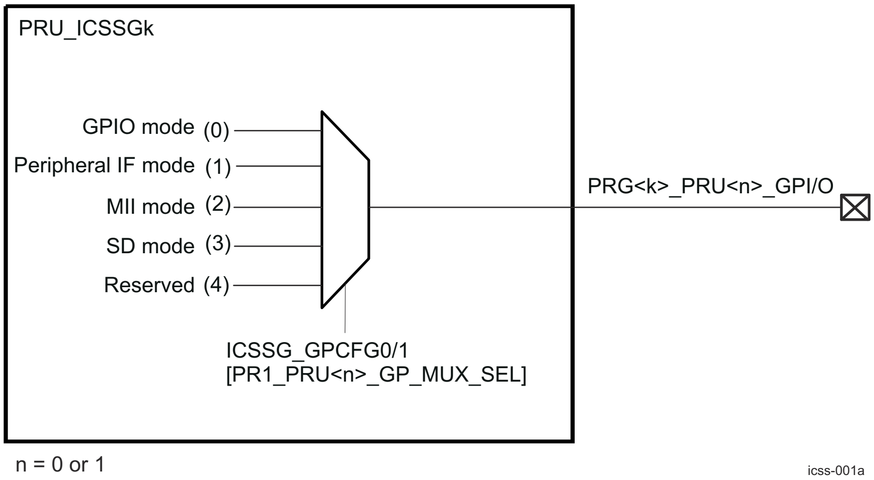

Figure 6-16. PRU_ICSSG Internal Wrapper Multiplexing

Note

Additionally to PRU_ICSSG wrapper multiplexing the device I/O logic maps the PRU_ICSSG signals to the different device pins by programming in the Control Module (CTRL_MMR0). For more information, refer to the *Pad Configuration Registers* in the *CTRL_MMR0 Registers*.

The below Figure 6-17 illustrates the PRU_ICSSG0 I/O interface signals.

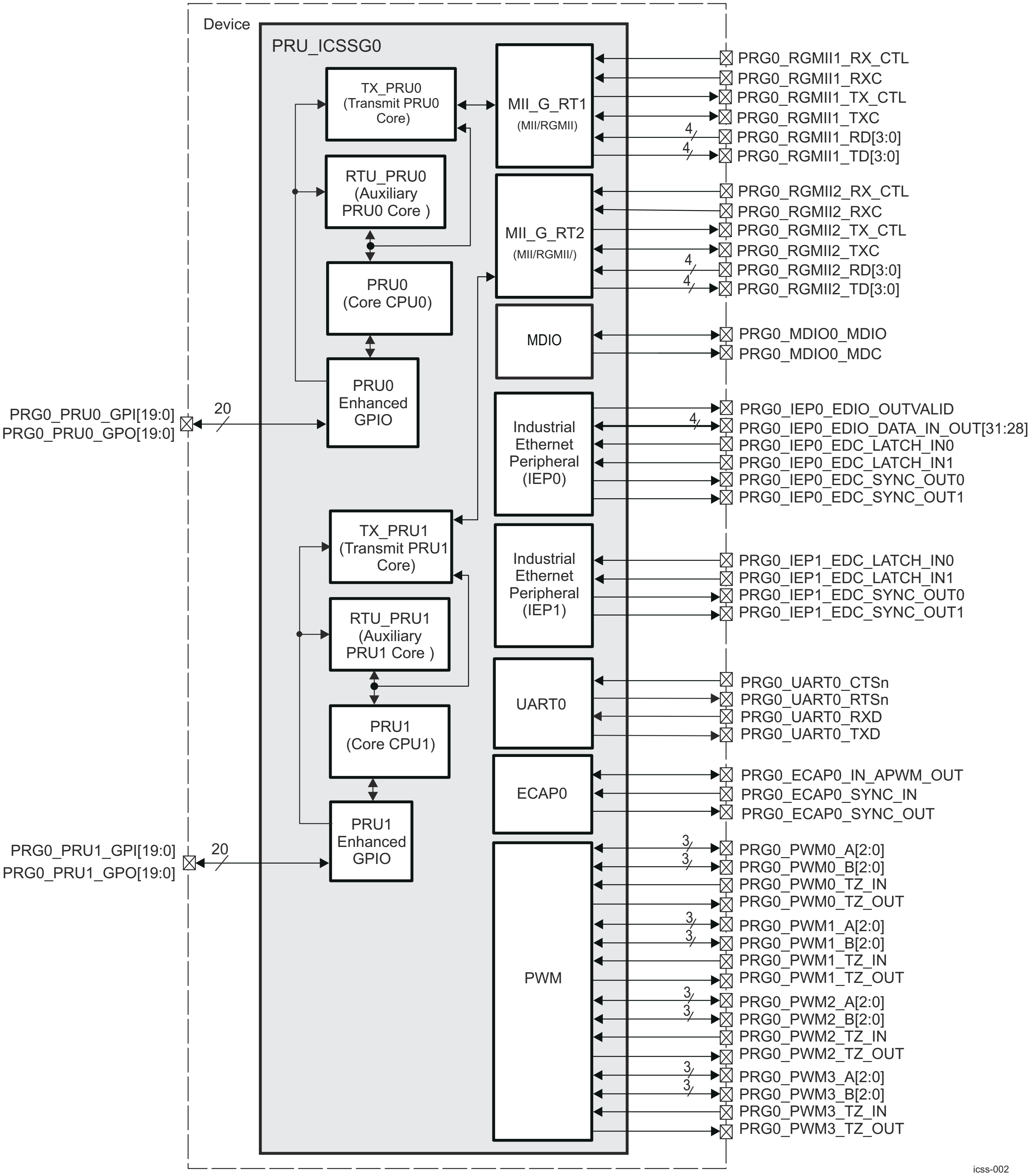

Figure 6-17. PRU_ICSSG0 External Interface I/Os

The Figure 6-18 illustrates the PRU_ICSSG1 I/O interface signals.

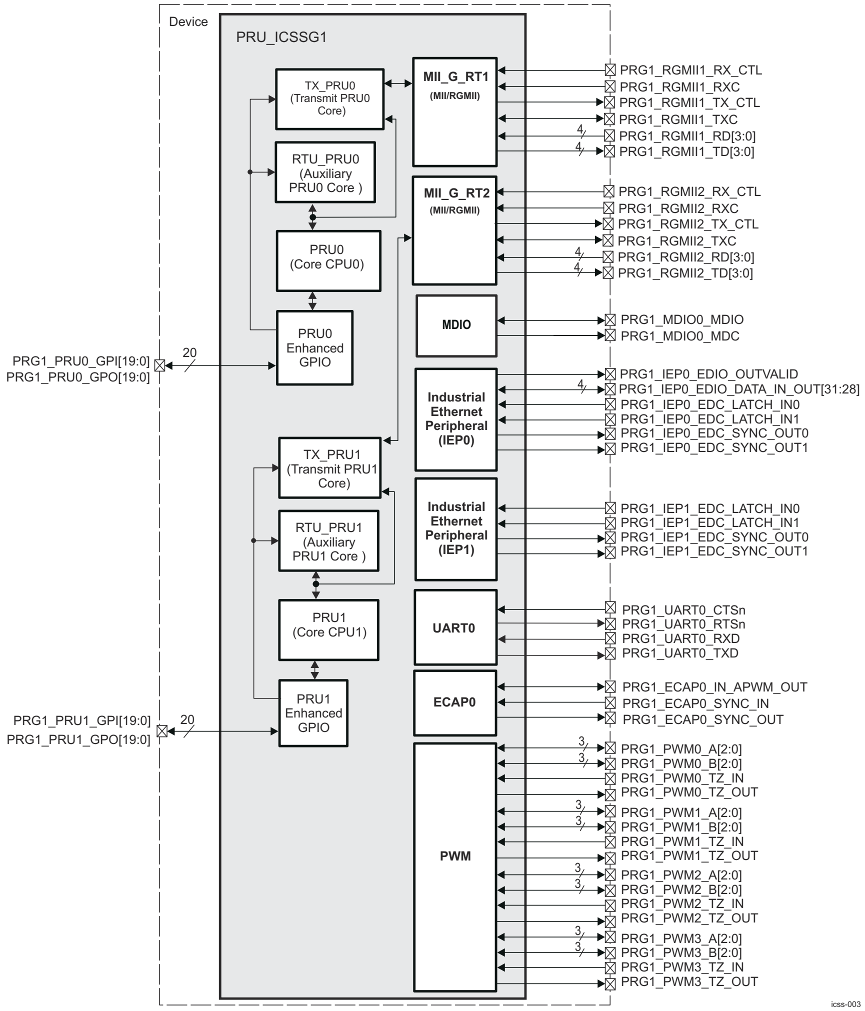

Figure 6-18. PRU_ICSSG1 External Interface I/Os

Note

PRGn_PWMm_A[2:0] = PRGn_PWMm_[2:0]_POS and PRGn_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG.

Table 6-51 describes the PRU_ICSSG0 I/O signals.

Table 6-51. PRU_ICSSG0 I/O Signals

Device Level Signal	Alternate Function via Internal Multiplexing				I/O[1]	Description	Pin Reset [2]
	ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL=						
PRU0 GP Signals	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG0_PRU0_GPO0	pr0_pru0_pru_r30_out[0]	pr0_pru0_perif0_clk			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO1	pr0_pru0_pru_r30_out[1]	pr0_pru0_perif0_out			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO2	pr0_pru0_pru_r30_out[2]	pr0_pru0_perif0_out_en			O	PRU0 R30 Outputs	0

Table 6-51. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing				I/O[1]	Description	Pin Reset [2]
PRG0_PRU0_GPO3	pr0_pru0_pru_r30_out[3]	pr0_pru0_perif1_clk			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO4	pr0_pru0_pru_r30_out[4]	pr0_pru0_perif1_out			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO5	pr0_pru0_pru_r30_out[5]	pr0_pru0_perif1_out_en			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO6	pr0_pru0_pru_r30_out[6]	pr0_pru0_perif2_clk			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO7	pr0_pru0_pru_r30_out[7]	pr0_pru0_perif2_out			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO8	pr0_pru0_pru_r30_out[8]	pr0_pru0_perif2_out_en			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO9	pr0_pru0_pru_r30_out[9]				O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO10	pr0_pru0_pru_r30_out[10]				O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO11	pr0_pru0_pru_r30_out[11]		pr0_mii1_txd[0]		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO12	pr0_pru0_pru_r30_out[12]	pr0_pru0_perif2_out[4]	pr0_mii1_txd[1]		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO13	pr0_pru0_pru_r30_out[13]		pr0_mii1_txd[2]		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO14	pr0_pru0_pru_r30_out[14]		pr0_mii1_txd[3]		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO15	pr0_pru0_pru_r30_out[15]		pr0_mii1_txen		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO16	pr0_pru0_pru_r30_out[16]				O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO17	pr0_pru0_pru_r30_out[17]				O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO18	pr0_pru0_pru_r30_out[18]				O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO19	pr0_pru0_pru_r30_out[19]				O	PRU0 R30 Outputs	0
PRG0_PRU0_GPI0	pr0_pru0_pru_r31_in[0]		pr0_mii0_rxd[0]	pr0_pru0_sd0_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI1	pr0_pru0_pru_r31_in[1]		pr0_mii0_rxd[1]	pr0_pru0_sd0_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI2	pr0_pru0_pru_r31_in[2]		pr0_mii0_rxd[2]	pr0_pru0_sd1_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI3	pr0_pru0_pru_r31_in[3]		pr0_mii0_rxd[3]	pr0_pru0_sd1_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI4	pr0_pru0_pru_r31_in[4]		pr0_mii0_rxdv	pr0_pru0_sd2_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI5	pr0_pru0_pru_r31_in[5]		pr0_mii0_rxer	pr0_pru0_sd2_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI6	pr0_pru0_pru_r31_in[6]		pr0_mii_mr0_clk	pr0_pru0_sd3_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI7	pr0_pru0_pru_r31_in[7]			pr0_pru0_sd3_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI8	pr0_pru0_pru_r31_in[8]		pr0_mii0_rxlink	pr0_pru0_sd4_clk	I	PRU0 R31 Inputs	HiZ

Table 6-51. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing				I/O(1)	Description	Pin Reset (2)
PRG0_PRU0_GPI9	pr0_pru0_pru_r31_in[9]	pr0_pru0_perif0_in	pr0_mii0_col	pr0_pru0_sd4_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI10	pr0_pru0_pru_r31_in[10]	pr0_pru0_perif1_in	pr0_mii0_crs	pr0_pru0_sd5_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI11	pr0_pru0_pru_r31_in[11]	pr0_pru0_perif2_in		pr0_pru0_sd5_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI12	pr0_pru0_pru_r31_in[12]			pr0_pru0_sd6_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI13	pr0_pru0_pru_r31_in[13]	pr0_pru0_perif0_in(4)		pr0_pru0_sd6_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI14	pr0_pru0_pru_r31_in[14]	pr0_pru0_perif1_in(4)		pr0_pru0_sd7_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI15	pr0_pru0_pru_r31_in[15]			pr0_pru0_sd7_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI16	pr0_pru0_pru_r31_in[16]		pr0_mii_mt1_clk	pr0_pru0_sd8_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI17	pr0_pru0_pru_r31_in[17]			pr0_pru0_sd8_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI18	pr0_pru0_pru_r31_in[18]			pr0_pru0_sd4_d(4)	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI19	pr0_pru0_pru_r31_in[19]			pr0_pru0_sd5_clk(4)	I	PRU0 R31 Inputs	HiZ
PRU1 GP Signals	ICSSG_GPCFG1_REG[29-26] PR1_PRU1_GP_MUX_SEL=						
	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG0_PRU1_GPO0	pr0_pru1_pru_r30_out[0]	pr0_pru1_perif0_clk			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO1	pr0_pru1_pru_r30_out[1]	pr0_pru1_perif0_out			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO2	pr0_pru1_pru_r30_out[2]	pr0_pru1_perif0_out_en			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO3	pr0_pru1_pru_r30_out[3]	pr0_pru1_perif1_clk			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO4	pr0_pru1_pru_r30_out[4]	pr0_pru1_perif1_out			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO5	pr0_pru1_pru_r30_out[5]	pr0_pru1_perif1_out_en			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO6	pr0_pru1_pru_r30_out[6]	pr0_pru1_perif2_clk			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO7	pr0_pru1_pru_r30_out[7]	pr0_pru1_perif2_out			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO8	pr0_pru1_pru_r30_out[8]	pr0_pru1_perif2_out_en			O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO9	pr0_pru1_pru_r30_out[9]				O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO10	pr0_pru1_pru_r30_out[10]				O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO11	pr0_pru1_pru_r30_out[11]		pr0_mii0_txd[0]		O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO12	pr0_pru1_pru_r30_out[12]	pr1_pru0_perif2_out(4)	pr0_mii0_txd[1]		O	PRU1 R30 Outputs	0

Table 6-51. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing				I/O(1)	Description	Pin Reset (2)
PRG0_PRU1_GPO13	pr0_pru1_pru_r30_out[13]		pr0_mii0_txd[2]		O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO14	pr0_pru1_pru_r30_out[14]		pr0_mii0_txd[3]		O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO15	pr0_pru1_pru_r30_out[15]		pr0_mii0_txen		O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO16	pr0_pru1_pru_r30_out[16]				O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO17	pr0_pru1_pru_r30_out[17]				O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO18	pr0_pru1_pru_r30_out[18]				O	PRU1 R30 Outputs	0
PRG0_PRU1_GPO19	pr0_pru1_pru_r30_out[19]				O	PRU1 R30 Outputs	0
PRG0_PRU1_GPI0	pr0_pru1_pru_r31_in[0]		pr0_mii1_rxd[0]	pr0_pru1_sd0_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI1	pr0_pru1_pru_r31_in[1]		pr0_mii1_rxd[1]	pr0_pru1_sd0_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI2	pr0_pru1_pru_r31_in[2]		pr0_mii1_rxd[2]	pr0_pru1_sd1_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI3	pr0_pru1_pru_r31_in[3]		pr0_mii1_rxd[3]	pr0_pru1_sd1_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI4	pr0_pru1_pru_r31_in[4]		pr0_mii1_rxdv	pr0_pru1_sd2_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI5	pr0_pru1_pru_r31_in[5]		pr0_mii1_rxer	pr0_pru1_sd2_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI6	pr0_pru1_pru_r31_in[6]		pr0_mii_mr1_clk	pr0_pru1_sd3_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI7	pr0_pru1_pru_r31_in[7]			pr0_pru1_sd3_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI8	pr0_pru1_pru_r31_in[8]		pr0_mii1_rxlink	pr0_pru1_sd4_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI9	pr0_pru1_pru_r31_in[9]	pr0_pru1_perif0_in	pr0_mii1_col	pr0_pru1_sd4_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI10	pr0_pru1_pru_r31_in[10]	pr0_pru1_perif1_in	pr0_mii1_crs	pr0_pru1_sd5_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI11	pr0_pru1_pru_r31_in[11]	pr0_pru1_perif2_in		pr0_pru1_sd5_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI12	pr0_pru1_pru_r31_in[12]			pr0_pru1_sd6_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI13	pr0_pru1_pru_r31_in[13]	pr0_pru0_perif0_in (4)		pr0_pru1_sd6_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI14	pr0_pru1_pru_r31_in[14]	pr0_pru0_perif1_in (4)		pr0_pru1_sd7_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI15	pr0_pru1_pru_r31_in[15]			pr0_pru1_sd7_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI16	pr0_pru1_pru_r31_in[16]	pr0_pru1_pru_r31_in[16]	pr0_mii_mt0_clk	pr0_pru1_sd8_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI17	pr0_pru1_pru_r31_in[17]			pr0_pru0_sd8_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI18	pr0_pru1_pru_r31_in[18]			pr0_pru0_sd4_d(4)	I	PRU1 R31 Inputs	HiZ

Table 6-51. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing		I/O[1]	Description	Pin Reset [2]
PRG0_PRU1_GPI19	pr0_pru1_pru_r31_in[19]	pr0_pru0_sd5_clk [4]	I	PRU1 R31 Inputs	HiZ
MII_G_RT1 (RGMII mode)					
PRG0_RGMII1_RX_CTL			I	RGMII1 Receive Control	-
PRG0_RGMII1_RXC			I	RGMII1 Receive Clock	-
PRG0_RGMII1_TX_CTL			O	RGMII1 Transmit Control	-
PRG0_RGMII1_TXC			I/O	RGMII1 Transmit Clock	-
PRG0_RGMII1_RD[3:0]			I	RGMII1 Receive Data	-
PRG0_RGMII1_TD[3:0]			O	RGMII1 Transmit Data	-
MII_G_RT2 (RGMII mode)					
PRG0_RGMII2_RX_CTL			I	RGMII2 Receive Control	-
PRG0_RGMII2_RXC			I	RGMII2 Receive Clock	-
PRG0_RGMII2_TX_CTL			O	RGMII2 Transmit Control	-
PRG0_RGMII2_TXC			I/O	RGMII2 Transmit Clock	-
PRG0_RGMII2_RD[3:0]			I	RGMII2 Receive Data	-
PRG0_RGMII2_TD[3:0]			O	RGMII2 Transmit Data	-
MDIO	MDIO				
PRG0_MDIO0_MDC	pr0_mdio_mdclk		O	MDIO Clock	0
PRG0_MDIO0_MDIO	pr0_mdio_data		I/O	MDIO Data	HiZ
Industrial Ethernet (IEP0)	Industrial Ethernet				
PRG0_IEP0_EDIO_OUTVALID	pr0_iep0_edio_outvalid		O	IEP0 Digital I/O Output Valid	0
PRG0_IEP0_EDIO_DATA_IN_OUT[31:28]	pr0_iep0_edio_data_in_out[31:28]		I/O	IEP0 Digital I/Os Data In/Out	HiZ
PRG0_IEP0_EDC_SYNC_OUT0	pr0_iep0_edc_sync_out0		O	IEP0 Distributed Clock Sync Out	0
PRG0_IEP0_EDC_SYNC_OUT1	pr0_iep0_edc_sync_out1		O	IEP0 Distributed Clock Sync Out	0
PRG0_IEP0_EDC_LATCH_IN0	pr0_iep0_edc_latch_in0		I	IEP0 Distributed Clock Latch In	HiZ

Table 6-51. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing	I/O(1)	Description	Pin Reset (2)
PRG0_IEP0_EDC_LATCH_IN1	pr0_iep0_edc_latch_in1	I	IEP0 Distributed Clock Latch In	HiZ
Industrial Ethernet (IEP1)	Industrial Ethernet			
PRG0_IEP1_EDC_SYNC_OUT0	pr0_iep1_edc_sync_out0	O	IEP1 Distributed Clock Sync Out	0
PRG0_IEP1_EDC_SYNC_OUT1	pr0_iep1_edc_sync_out1	O	IEP1 Distributed Clock Sync Out	0
PRG0_IEP1_EDC_LATCH_IN0	pr0_iep1_edc_latch_in0	I	IEP1 Distributed Clock Latch In	HiZ
PRG0_IEP1_EDC_LATCH_IN1	pr0_iep1_edc_latch_in1	I	IEP1 Distributed Clock Latch In	HiZ
UART0	UART0			
PRG0_UART0_CTSn	pr0_uart0_cts_n	I	UART0 Clear to Send	HiZ
PRG0_UART0_RTSn	pr0_uart0_rts_n	O	UART0 Request to Send	1
PRG0_UART0_RXD	pr0_uart0_rxd	I	UART0 Receive Data	HiZ
PRG0_UART0_TXD	pr0_uart0_txd	O	UART0 Transmit Data	1
ECAP0	ECAP0			
PRG0_ECAP0_IN_APWM_OUT	pr0_ecap0_ecap_capin_apwm_o	I/O	Enhanced capture (ECAP0) input or Auxiliary PWM out	HiZ
PRG0_ECAP0_SYNC_IN	pr0_ecap0_ecap_syncin	I	Enhanced capture (ECAP0) Sync In	0
PRG0_ECAP0_SYNC_OUT	pr0_ecap0_ecap_syncout	O	Enhanced capture (ECAP0) Sync Out	0
PWM				
PRG0_PWM0_A[2:0] (3)	pr0_pwm_pwm0_[2:0]_pos	I/O	PWM Set 0 Positive In/Out	-
PRG0_PWM0_B[2:0] (3)	pr0_pwm_pwm0_[2:0]_neg	I/O	PWM Set 0 Negative In/Out	-
PRG0_PWM0_TZ_IN	pr0_pwm_pwm0_trip_in	I	PWM Set 0 Tripzone Input	-
PRG0_PWM0_TZ_OUT	pr0_pwm_pwm0_trip_out	O	PWM Set 0 Tripzone Output	-
PRG0_PWM1_A[2:0] (3)	pr0_pwm_pwm1_[2:0]_pos	I/O	PWM Set 1 Positive In/Out	-

Table 6-51. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing	I/O(1)	Description	Pin Reset (2)
PRG0_PWM1_B[2:0] (3)	pr0_pwm_pwm1_[2:0]_neg	I/O	PWM Set 1 Negative In/Out	-
PRG0_PWM1_TZ_IN	pr0_pwm_pwm1_trip_in	I	PWM Set 1 Tripzone Input	-
PRG0_PWM1_TZ_OUT	pr0_pwm_pwm1_trip_out	O	PWM Set 1 Tripzone Output	-
PRG0_PWM2_A[2:0] (3)	pr0_pwm_pwm2_[2:0]_pos	I/O	PWM Set 2 Positive In/Out	-
PRG0_PWM2_B[2:0] (3)	pr0_pwm_pwm2_[2:0]_neg	I/O	PWM Set 2 Negative In/Out	-
PRG0_PWM2_TZ_IN	pr0_pwm_pwm2_trip_in	I	PWM Set 2 Tripzone Input	-
PRG0_PWM2_TZ_OUT	pr0_pwm_pwm2_trip_out	O	PWM Set 2 Tripzone Output	-
PRG0_PWM3_A[2:0] (3)	pr0_pwm_pwm3_[2:0]_pos	I/O	PWM Set 3 Positive In/Out	-
PRG0_PWM3_B[2:0] (3)	pr0_pwm_pwm3_[2:0]_neg	I/O	PWM Set 3 Negative In/Out	-
PRG0_PWM3_TZ_IN	pr0_pwm_pwm3_trip_in	I	PWM Set 3 Tripzone Input	-
PRG0_PWM3_TZ_OUT	pr0_pwm_pwm3_trip_out	O	PWM Set 3 Tripzone Output	-

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) NPRGn_PWMm_A[2:0] = PRGn_PWMm_[2:0]_POS and PRGn_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG
(4) When ICSSG_SA_MX_REG[7] G_MUX_EN = 1

Table 6-52 describes the PRU_ICSSG1 I/O signals.

Table 6-52. PRU_ICSSG1 I/O Signals

Device Level Signal	**Alternate Function via Internal Wrapper Multiplexing**				**I/O**[1]	**Description**	**Pin Reset** [2]
	ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL=						
PRU0 GP Signals	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG1_PRU0_GPO0	pr1_pru0_pru_r30_out[0]	pr1_pru0_perif0_clk			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO1	pr1_pru0_pru_r30_out[1]	pr1_pru0_perif0_out			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO2	pr1_pru0_pru_r30_out[2]	pr1_pru0_perif0_out_en			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO3	pr1_pru0_pru_r30_out[3]	pr1_pru0_perif1_clk			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO4	pr1_pru0_pru_r30_out[4]	pr1_pru0_perif1_out			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO5	pr1_pru0_pru_r30_out[5]	pr1_pru0_perif1_out_en			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO6	pr1_pru0_pru_r30_out[6]	pr1_pru0_perif2_clk			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO7	pr1_pru0_pru_r30_out[7]	pr1_pru0_perif2_out			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO8	pr1_pru0_pru_r30_out[8]	pr1_pru0_perif2_out_en			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO9	pr1_pru0_pru_r30_out[9]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO10	pr1_pru0_pru_r30_out[10]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO11	pr1_pru0_pru_r30_out[11]		pr1_mii1_txd[0]		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO12	pr1_pru0_pru_r30_out[12]	pr1_pru0_perif2_out[4]	pr1_mii1_txd[1]		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO13	pr1_pru0_pru_r30_out[13]		pr1_mii1_txd[2]		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO14	pr1_pru0_pru_r30_out[14]		pr1_mii1_txd[3]		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO15	pr1_pru0_pru_r30_out[15]		pr1_mii1_txen		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO16	pr1_pru0_pru_r30_out[16]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO17	pr1_pru0_pru_r30_out[17]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO18	pr1_pru0_pru_r30_out[18]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO19	pr1_pru0_pru_r30_out[19]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPI0	pr1_pru0_pru_r31_in[0]		pr1_mii0_rxd[0]	pr1_pru0_sd0_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI1	pr1_pru0_pru_r31_in[1]		pr1_mii0_rxd[1]	pr1_pru0_sd0_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI2	pr1_pru0_pru_r31_in[2]		pr1_mii0_rxd[2]	pr1_pru0_sd1_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI3	pr1_pru0_pru_r31_in[3]		pr1_mii0_rxd[3]	pr1_pru0_sd1_d	I	PRU0 R31 Inputs	HiZ

Table 6-52. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing				I/O(1)	Description	Pin Reset (2)
PRG1_PRU0_GPI4	pr1_pru0_pru_r31_in[4]		pr1_mii0_rxdv	pr1_pru0_sd2_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI5	pr1_pru0_pru_r31_in[5]		pr1_mii0_rxer	pr1_pru0_sd2_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI6	pr1_pru0_pru_r31_in[6]		pr1_mii_mr0_clk	pr1_pru0_sd3_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI7	pr1_pru0_pru_r31_in[7]			pr1_pru0_sd3_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI8	pr1_pru0_pru_r31_in[8]		pr1_mii0_rxlink	pr1_pru0_sd4_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI9	pr1_pru0_pru_r31_in[9]	pr1_pru0_perif0_in	pr1_mii0_col	pr1_pru0_sd4_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI10	pr1_pru0_pru_r31_in[10]	pr1_pru0_perif1_in	pr1_mii0_crs	pr1_pru0_sd5_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI11	pr1_pru0_pru_r31_in[11]	pr1_pru0_perif2_in		pr1_pru0_sd5_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI12	pr1_pru0_pru_r31_in[12]			pr1_pru0_sd6_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI13	pr1_pru0_pru_r31_in[13]	pr0_pru0_perif0_in (4)		pr1_pru0_sd6_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI14	pr1_pru0_pru_r31_in[14]	pr0_pru0_perif1_in (4)		pr1_pru0_sd7_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI15	pr1_pru0_pru_r31_in[15]			pr1_pru0_sd7_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI16	pr1_pru0_pru_r31_in[16]		pr1_mii_mt1_clk	pr1_pru0_sd8_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI17	pr1_pru0_pru_r31_in[17]			pr1_pru0_sd8_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI18	pr1_pru0_pru_r31_in[18]			pr0_pru0_sd4_d(4)	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI19	pr1_pru0_pru_r31_in[19]			pr0_pru0_sd5_clk (4)	I	PRU0 R31 Inputs	HiZ
PRU1 GP Signals	ICSSG_GPCFG1_REG[29-26] PR1_PRU1_GP_MUX_SEL=						
	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG1_PRU1_GPO0	pr1_pru1_pru_r30_out[0]	pr1_pru1_perif0_clk			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1	pr1_pru1_pru_r30_out[1]	pr1_pru1_perif0_out			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO2	pr1_pru1_pru_r30_out[2]	pr1_pru1_perif0_out_en			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO3	pr1_pru1_pru_r30_out[3]	pr1_pru1_perif1_clk			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO4	pr1_pru1_pru_r30_out[4]	pr1_pru1_perif1_out			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO5	pr1_pru1_pru_r30_out[5]	pr1_pru1_perif1_out_en			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO6	pr1_pru1_pru_r30_out[6]	pr1_pru1_perif2_clk			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO7	pr1_pru1_pru_r30_out[7]	pr1_pru1_perif2_out			O	PRU1 R30 Outputs	0

Table 6-52. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing				I/O[1]	Description	Pin Reset [2]
PRG1_PRU1_GPO8	pr1_pru1_pru_r30_out[8]	pr1_pru1_perif2_out_en			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO9	pr1_pru1_pru_r30_out[9]				O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO10	pr1_pru1_pru_r30_out[10]				O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO11	pr1_pru1_pru_r30_out[11]		pr1_mii0_txd[0]		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO12	pr1_pru1_pru_r30_out[12]	pr1_pru0_perif2_out[4]	pr1_mii0_txd[1]		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO13	pr1_pru1_pru_r30_out[13]		pr1_mii0_txd[2]		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO14	pr1_pru1_pru_r30_out[14]		pr1_mii0_txd[3]		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO15	pr1_pru1_pru_r30_out[15]		pr1_mii0_txen		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO16	pr1_pru1_pru_r30_out[16]				O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO17	pr1_pru1_pru_r30_out[17]				O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO18	pr1_pru1_pru_r30_out[18]				O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO19	pr1_pru1_pru_r30_out[19]				O	PRU1 R30 Outputs	0
PRG1_PRU1_GPI0	pr1_pru1_pru_r31_in[0]		pr1_mii1_rxd[0]	pr1_pru1_sd0_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI1	pr1_pru1_pru_r31_in[1]		pr1_mii1_rxd[1]	pr1_pru1_sd0_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI2	pr1_pru1_pru_r31_in[2]		pr1_mii1_rxd[2]	pr1_pru1_sd1_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI3	pr1_pru1_pru_r31_in[3]		pr1_mii1_rxd[3]	pr1_pru1_sd1_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI4	pr1_pru1_pru_r31_in[4]		pr1_mii1_rxdv	pr1_pru1_sd2_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI5	pr1_pru1_pru_r31_in[5]		pr1_mii1_rxer	pr1_pru1_sd2_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI6	pr1_pru1_pru_r31_in[6]		pr1_mii_mr1_clk	pr1_pru1_sd3_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI7	pr1_pru1_pru_r31_in[7]			pr1_pru1_sd3_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI8	pr1_pru1_pru_r31_in[8]		pr1_mii1_rxlink	pr1_pru1_sd4_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI9	pr1_pru1_pru_r31_in[9]	pr1_pru1_perif0_in	pr1_mii1_col	pr1_pru1_sd4_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI10	pr1_pru1_pru_r31_in[10]	pr1_pru1_perif1_in	pr1_mii1_crs	pr1_pru1_sd5_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI11	pr1_pru1_pru_r31_in[11]	pr1_pru1_perif2_in		pr1_pru1_sd5_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI12	pr1_pru1_pru_r31_in[12]			pr1_pru1_sd6_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI13	pr1_pru1_pru_r31_in[13]	pr0_pru0_perif0_in[4]		pr1_pru1_sd6_d	I	PRU1 R31 Inputs	HiZ

Table 6-52. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	**Alternate Function via Internal Wrapper Multiplexing**				**I/O**[1]	**Description**	**Pin Reset**[2]
PRG1_PRU1_GPI14	pr1_pru1_pru_r31_in[14]	pr0_pru0_perif1_in[4]		pr1_pru1_sd7_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI15	pr1_pru1_pru_r31_in[15]			pr1_pru1_sd7_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI16	pr1_pru1_pru_r31_in[16]	pr1_pru1_pru_r31_in[16]	pr1_mii_mt0_clk	pr1_pru1_sd8_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI17	pr1_pru1_pru_r31_in[17]			pr1_pru0_sd8_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI18	pr1_pru1_pru_r31_in[18]			pr0_pru0_sd4_d[4]	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI19	pr1_pru1_pru_r31_in[19]			pr0_pru0_sd5_clk[4]	I	PRU1 R31 Inputs	HiZ
MII_G_RT1 (RGMII mode)							
PRG1_RGMII1_RX_CTL					I	RGMII1 Receive Control	-
PRG1_RGMII1_RXC					I	RGMII1 Receive Clock	-
PRG1_RGMII1_TX_CTL					O	RGMII1 Transmit Control	-
PRG1_RGMII1_TXC					I/O	RGMII1 Transmit Clock	-
PRG1_RGMII1_RD[3:0]					I	RGMII1 Receive Data	-
PRG1_RGMII1_TD[3:0]					O	RGMII1 Transmit Data	-
MII_G_RT2 (RGMII mode)							
PRG1_RGMII2_RX_CTL					I	RGMII2 Receive Control	-
PRG1_RGMII2_RXC					I	RGMII2 Receive Clock	-
PRG1_RGMII2_TX_CTL					O	RGMII2 Transmit Control	-
PRG1_RGMII2_TXC					I/O	RGMII2 Transmit Clock	-
PRG1_RGMII2_RD[3:0]					I	RGMII2 Receive Data	-
PRG1_RGMII2_TD[3:0]					O	RGMII2 Transmit Data	-
MDIO	MDIO						
PRG1_MDIO0_MDC	pr1_mdio_mdclk				O	MDIO Clock	0
PRG1_MDIO0_MDIO	pr1_mdio_data				I/O	MDIO Data	HiZ
Industrial Ethernet (IEP0)	Industrial Ethernet						
PRG1_IEP0_EDIO_OUTVALID	pr1_iep0_edio_outvalid				O	IEP0 Digital I/O Output Valid	0

Table 6-52. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing	I/O[(1)]	Description	Pin Reset [(2)]
PRG1_IEP0_EDIO_DATA_IN_OUT[31:28]	pr1_iep0_edio_data_in_out[31:28]	I/O	IEP0 Digital I/Os Data In/Out	HiZ
PRG1_IEP0_EDC_SYNC_OUT0	pr1_iep0_edc_sync_out0	O	IEP0 Distributed Clock Sync Out	0
PRG1_IEP0_EDC_SYNC_OUT1	pr1_iep0_edc_sync_out1	O	IEP0 Distributed Clock Sync Out	0
PRG1_IEP0_EDC_LATCH_IN0	pr1_iep0_edc_latch_in0	I	IEP0 Distributed Clock Latch In	HiZ
PRG1_IEP0_EDC_LATCH_IN1	pr1_iep0_edc_latch_in1	I	IEP0 Distributed Clock Latch In	HiZ
Industrial Ethernet (IEP1)	Industrial Ethernet			
PRG1_IEP1_EDC_SYNC_OUT0	pr1_iep1_edc_sync_out0	O	IEP1 Distributed Clock Sync Out	0
PRG1_IEP1_EDC_SYNC_OUT1	pr1_iep1_edc_sync_out1	O	IEP1 Distributed Clock Sync Out	0
PRG1_IEP1_EDC_LATCH_IN0	pr1_iep1_edc_latch_in0	I	IEP1 Distributed Clock Latch In	HiZ
PRG1_IEP1_EDC_LATCH_IN1	pr1_iep1_edc_latch_in1	I	IEP1 Distributed Clock Latch In	HiZ
UART0	UART0			
PRG1_UART0_CTSn	pr1_uart0_cts_n	I	UART0 Clear to Send	HiZ
PRG1_UART0_RTSn	pr1_uart0_rts_n	O	UART0 Request to Send	1
PRG1_UART0_RXD	pr1_uart0_rxd	I	UART0 Receive Data	HiZ
PRG1_UART0_TXD	pr1_uart0_txd	O	UART0 Transmit Data	1
ECAP0	ECAP0			
PRG1_ECAP0_IN_APWM_OUT	pr1_ecap0_ecap_capin_apwm_o	I/O	Enhanced capture (ECAP0) input or Auxiliary PWM out	HiZ
PRG1_ECAP0_SYNC_IN	pr1_ecap0_ecap_syncin	I	Enhanced capture (ECAP0) Sync In	0
PRG1_ECAP0_SYNC_OUT	pr1_ecap0_ecap_syncout	O	Enhanced capture (ECAP0) Sync Out	0
PWM				

Table 6-52. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing	I/O(1)	Description	Pin Reset (2)
PRG1_PWM0_A[2:0] (3)	pr1_pwm_pwm0_[2:0]_pos	I/O	PWM Set 0 Positive In/Out	-
PRG1_PWM0_B[2:0] (3)	pr1_pwm_pwm0_[2:0]_neg	I/O	PWM Set 0 Negative In/Out	-
PRG1_PWM0_TZ_IN	pr1_pwm_pwm0_trip_in	I	PWM Set 0 Tripzone Input	-
PRG1_PWM0_TZ_OUT	pr1_pwm_pwm0_trip_out	O	PWM Set 0 Tripzone Output	-
PRG1_PWM1_A[2:0] (3)	pr1_pwm_pwm1_[2:0]_pos	I/O	PWM Set 1 Positive In/Out	-
PRG1_PWM1_B[2:0] (3)	pr1_pwm_pwm1_[2:0]_neg	I/O	PWM Set 1 Negative In/Out	-
PRG1_PWM1_TZ_IN	pr1_pwm_pwm1_trip_in	I	PWM Set 1 Tripzone Input	-
PRG1_PWM1_TZ_OUT	pr1_pwm_pwm1_trip_out	O	PWM Set 1 Tripzone Output	-
PRG1_PWM2_A[2:0] (3)	pr1_pwm_pwm2_[2:0]_pos	I/O	PWM Set 2 Positive In/Out	-
PRG1_PWM2_B[2:0] (3)	pr1_pwm_pwm2_[2:0]_neg	I/O	PWM Set 2 Negative In/Out	-
PRG1_PWM2_TZ_IN	pr1_pwm_pwm2_trip_in	I	PWM Set 2 Tripzone Input	-
PRG1_PWM2_TZ_OUT	pr1_pwm_pwm2_trip_out	O	PWM Set 2 Tripzone Output	-
PRG1_PWM3_A[2:0] (3)	pr1_pwm_pwm3_[2:0]_pos	I/O	PWM Set 3 Positive In/Out	-
PRG1_PWM3_B[2:0] (3)	pr1_pwm_pwm3_[2:0]_neg	I/O	PWM Set 3 Negative In/Out	-
PRG1_PWM3_TZ_IN	pr1_pwm_pwm3_trip_in	I	PWM Set 3 Tripzone Input	-
PRG1_PWM3_TZ_OUT	pr1_pwm_pwm3_trip_out	O	PWM Set 3 Tripzone Output	-

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) PRGn_PWMm_A[2:0] = PRGn_PWMm_[2:0]_POS and PRGn_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG

(4) When ICSSG_SA_MX_REG[7] G_MUX_EN = 1

PRU_ICSSG I/O Signals

PRU_ICSSG<k> I/O Signals describes the PRU_ICSSG<k> I/O signals.

Note

<k> is the number of PRU_ICSSG in the device. See the Datasheet for additional details.

Table 6-53. PRU_ICSSG<k> I/O Signals

Device Level Signal	Alternate Function via Internal Multiplexing				I/O(1)	Description	Pin Reset (2)
	ICSSG_GPCFG0_REG[29-26] PR<k_PRU0_GP_MUX_SEL=						
PRU0 GP Signals	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG<k>_PRU0_GPO0	pr<k>_pru0_pru_r30_out[0]	pr<k>_pru0_perif0_clk	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO1	pr<k>_pru0_pru_r30_out[1]	pr<k>_pru0_perif0_out	1(7)	pr<k>_pru0_pru_r30_out[1]	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO2	pr<k>_pru0_pru_r30_out[2]	pr<k>_pru0_perif0_out_en	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO3	pr<k>_pru0_pru_r30_out[3]	pr<k>_pru0_perif1_clk	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO4	pr<k>_pru0_pru_r30_out[4]	pr<k>_pru0_perif1_out	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO5	pr<k>_pru0_pru_r30_out[5]	pr<k>_pru0_perif1_out_en	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO6	pr<k>_pru0_pru_r30_out[6]	pr<k>_pru0_perif2_clk	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO7	pr<k>_pru0_pru_r30_out[7]	pr<k>_pru0_perif2_out	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO8	pr<k>_pru0_pru_r30_out[8]	pr<k>_pru0_perif2_out_en	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO9	pr<k>_pru0_pru_r30_out[9]	1(7)	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO10	pr<k>_pru0_pru_r30_out[10]	1(7)	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO11	pr<k>_pru0_pru_r30_out[11]	1(7)	pr<k>_mii1_txd[0](4)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO12	pr<k>_pru0_pru_r30_out[12]	pr<k>_pru0_perif2_out	pr<k>_mii1_txd[1](4)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO13	pr<k>_pru0_pru_r30_out[13]	1(7)	pr<k>_mii1_txd[2](4)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO14	pr<k>_pru0_pru_r30_out[14]	1(7)	pr<k>_mii1_txd[3](4)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO15	pr<k>_pru0_pru_r30_out[15]	1(7)	pr<k>_mii1_txen(4)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO16	pr<k>_pru0_pru_r30_out[16]	1(7)	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO17	pr<k>_pru0_pru_r30_out[17]	1(7)	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO18	pr<k>_pru0_pru_r30_out[18]	1(7)	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPO19	pr<k>_pru0_pru_r30_out[19]	1(7)	1(7)	1(7)	O	PRU0 R30 Outputs	0
PRG<k>_PRU0_GPI0	pr<k>_pru0_pru_r31_in[0]		pr<k>_mii0_rxd[0]	pr<k>_pru0_sd0_clk	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI1	pr<k>_pru0_pru_r31_in[1]		pr<k>_mii0_rxd[1]	pr<k>_pru0_sd0_d	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI2	pr<k>_pru0_pru_r31_in[2]		pr<k>_mii0_rxd[2]	pr<k>_pru0_sd1_clk	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI3	pr<k>_pru0_pru_r31_in[3]		pr<k>_mii0_rxd[3]	pr<k>_pru0_sd1_d	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI4	pr<k>_pru0_pru_r31_in[4]		pr<k>_mii0_rxdv	pr<k>_pru0_sd2_clk	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI5	pr<k>_pru0_pru_r31_in[5]		pr<k>_mii0_rxer	pr<k>_pru0_sd2_d	I	PRU0 R31 Inputs	HiZ

Table 6-53. PRU_ICSSG<k> I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing				I/O[1]	Description	Pin Reset[2]
PRG<k>_PRU0_GPI6	pr<k>_pru0_pru_r31_in[6]		pr<k>_mii_mr0_clk	pr<k>_pru0_sd3_clk	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI7	pr<k>_pru0_pru_r31_in[7]			pr<k>_pru0_sd3_d	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI8	pr<k>_pru0_pru_r31_in[8]		pr<k>_mii0_rxlink	pr<k>_pru0_sd4_clk	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI9	pr<k>_pru0_pru_r31_in[9]	pr<k>_pru0_perif0_in[5]	pr<k>_mii0_col	pr<k>_pru0_sd4_d[5]	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI10	pr<k>_pru0_pru_r31_in[10]	pr<k>_pru0_perif1_in[5]	pr<k>_mii0_crs	pr<k>_pru0_sd5_clk[5]	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI11	pr<k>_pru0_pru_r31_in[11]	pr<k>_pru0_perif2_in		pr<k>_pru0_sd5_d	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI12	pr<k>_pru0_pru_r31_in[12]			pr<k>_pru0_sd6_clk	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI13	pr<k>_pru0_pru_r31_in[13]	pr<k>_pru0_perif0_in[6]		pr<k>_pru0_sd6_d	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI14	pr<k>_pru0_pru_r31_in[14]	pr<k>_pru0_perif1_in[6]		pr<k>_pru0_sd7_clk	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI15	pr<k>_pru0_pru_r31_in[15]			pr<k>_pru0_sd7_d	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI16	pr<k>_pru0_pru_r31_in[16]	pr<k>_pru0_pru_r31_in[16]	pr<k>_mii_mt1_clk, pr<k>_pru0_pru_r31_in[16]	pr<k>_pru0_sd8_clk, pr<k>_pru0_pru_r31_in[16]	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI17	pr<k>_pru0_pru_r31_in[17]			pr<k>_pru0_sd8_d	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI18	pr<k>_pru0_pru_r31_in[18]			pr<k>_pru0_sd4_d[6]	I	PRU0 R31 Inputs	HiZ
PRG<k>_PRU0_GPI19	pr<k>_pru0_pru_r31_in[19]			pr<k>_pru0_sd5_clk[6]	I	PRU0 R31 Inputs	HiZ
PRU1 GP Signals	ICSSG_GPCFG1_REG[29-26] PR<k>_PRU1_GP_MUX_SEL=						
	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG<k>_PRU1_GPO0	pr<k>_pru1_pru_r30_out[0]	pr<k>_pru1_perif0_clk	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO1	pr<k>_pru1_pru_r30_out[1]	pr<k>_pru1_perif0_out	1[7]	pr<k>_pru1_pru_r30_out[1]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO2	pr<k>_pru1_pru_r30_out[2]	pr<k>_pru1_perif0_out_en	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO3	pr<k>_pru1_pru_r30_out[3]	pr<k>_pru1_perif1_clk	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO4	pr<k>_pru1_pru_r30_out[4]	pr<k>_pru1_perif1_out	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO5	pr<k>_pru1_pru_r30_out[5]	pr<k>_pru1_perif1_out_en	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO6	pr<k>_pru1_pru_r30_out[6]	pr<k>_pru1_perif2_clk	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO7	pr<k>_pru1_pru_r30_out[7]	pr<k>_pru1_perif2_out	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO8	pr<k>_pru1_pru_r30_out[8]	pr<k>_pru1_perif2_out_en	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO9	pr<k>_pru1_pru_r30_out[9]	1[7]	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO10	pr<k>_pru1_pru_r30_out[10]	1[7]	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO11	pr<k>_pru1_pru_r30_out[11]	1[7]	pr<k>_mii0_txd[0][4]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO12	pr<k>_pru1_pru_r30_out[12]	pr<k>_pru1_perif2_out	pr<k>_mii0_txd[1][4]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO13	pr<k>_pru1_pru_r30_out[13]	1[7]	pr<k>_mii0_txd[2][4]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO14	pr<k>_pru1_pru_r30_out[14]	1[7]	pr<k>_mii0_txd[3][4]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO15	pr<k>_pru1_pru_r30_out[15]	1[7]	pr<k>_mii0_txen[4]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO16	pr<k>_pru1_pru_r30_out[16]	1[7]	1[7]	1[7]	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO17	pr<k>_pru1_pru_r30_out[17]	1[7]	1[7]	1[7]	O	PRU1 R30 Outputs	0

Table 6-53. PRU_ICSSG<k> I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing				I/O(1)	Description	Pin Reset (2)
PRG<k>_PRU1_GPO18	pr<k>_pru1_pru_r30_out[18]	1(7)	1(7)	1(7)	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPO19	pr<k>_pru1_pru_r30_out[19]	1(7)	1(7)	1(7)	O	PRU1 R30 Outputs	0
PRG<k>_PRU1_GPI0	pr<k>_pru1_pru_r31_in[0]		pr<k>_mii1_rxd[0]	pr<k>_pru1_sd0_clk	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI1	pr<k>_pru1_pru_r31_in[1]		pr<k>_mii1_rxd[1]	pr<k>_pru1_sd0_d	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI2	pr<k>_pru1_pru_r31_in[2]		pr<k>_mii1_rxd[2]	pr<k>_pru1_sd1_clk	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI3	pr<k>_pru1_pru_r31_in[3]		pr<k>_mii1_rxd[3]	pr<k>_pru1_sd1_d	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI4	pr<k>_pru1_pru_r31_in[4]		pr<k>_mii1_rxdv	pr<k>_pru1_sd2_clk	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI5	pr<k>_pru1_pru_r31_in[5]		pr<k>_mii1_rxer	pr<k>_pru1_sd2_d	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI6	pr<k>_pru1_pru_r31_in[6]		pr<k>_mii_mr1_clk	pr<k>_pru1_sd3_clk	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI7	pr<k>_pru1_pru_r31_in[7]			pr<k>_pru1_sd3_d	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI8	pr<k>_pru1_pru_r31_in[8]		pr<k>_mii1_rxlink	pr<k>_pru1_sd4_clk	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI9	pr<k>_pru1_pru_r31_in[9]	pr<k>_pru1_perif0_in(5)	pr<k>_mii1_col	pr<k>_pru1_sd4_d(5)	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI10	pr<k>_pru1_pru_r31_in[10]	pr<k>_pru1_perif1_in(5)	pr<k>_mii1_crs	pr<k>_pru1_sd5_clk(5)	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI11	pr<k>_pru1_pru_r31_in[11]	pr<k>_pru1_perif2_in		pr<k>_pru1_sd5_d	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI12	pr<k>_pru1_pru_r31_in[12]			pr<k>_pru1_sd6_clk	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI13	pr<k>_pru1_pru_r31_in[13]	pr<k>_pru1_perif0_in(6)		pr<k>_pru1_sd6_d	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI14	pr<k>_pru1_pru_r31_in[14]	pr<k>_pru1_perif1_in(6)		pr<k>_pru1_sd7_clk	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI15	pr<k>_pru1_pru_r31_in[15]			pr<k>_pru1_sd7_d	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI16	pr<k>_pru1_pru_r31_in[16]	pr<k>_pru1_pru_r31_in[16]	pr<k>_mii_mt0_clk, pr<k>_pru1_pru_r31_in[16]	pr<k>_pru1_sd8_clk, pr<k>_pru1_pru_r31_in[16]	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI17	pr<k>_pru1_pru_r31_in[17]			pr<k>_pru1_sd8_d	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI18	pr<k>_pru1_pru_r31_in[18]			pr<k>_pru1_sd4_d(6)	I	PRU1 R31 Inputs	HiZ
PRG<k>_PRU1_GPI19	pr<k>_pru1_pru_r31_in[19]			pr<k>_pru1_sd5_clk(6)	I	PRU1 R31 Inputs	HiZ
MII_G_RT1 (RGMII mode)							
PRG<k>_RGMII1_RX_CTL					I	RGMII1 Receive Control	-
PRG<k>_RGMII1_RXC					I	RGMII1 Receive Clock	-
PRG<k>_RGMII1_TX_CTL					O	RGMII1 Transmit Control	-
PRG<k>_RGMII1_TXC					I/O	RGMII1 Transmit Clock	-
PRG<k>_RGMII1_RD[3:0]					I	RGMII1 Receive Data	-
PRG<k>_RGMII1_TD[3:0]					O	RGMII1 Transmit Data	-
MII_G_RT2 (RGMII mode)							
PRG<k>_RGMII2_RX_CTL					I	RGMII2 Receive Control	-
PRG<k>_RGMII2_RXC					I	RGMII2 Receive Clock	-
PRG<k>_RGMII2_TX_CTL					O	RGMII2 Transmit Control	-

Table 6-53. PRU_ICSSG<k> I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing	I/O(1)	Description	Pin Reset (2)
PRG<k>_RGMII2_TXC		I/O	RGMII2 Transmit Clock	-
PRG<k>_RGMII2_RD[3:0]		I	RGMII2 Receive Data	-
PRG<k>_RGMII2_TD[3:0]		O	RGMII2 Transmit Data	-
MDIO	MDIO			
PRG<k>_MDIO0_MDC	pr<k>_mdio_mdclk	O	MDIO Clock	0
PRG<k>_MDIO0_MDIO	pr<k>_mdio_data	I/O	MDIO Data	HiZ
Industrial Ethernet (IEP0)	Industrial Ethernet			
PRG<k>_IEP0_EDIO_OUTVALID	pr<k>_iep0_edio_outvalid	O	IEP0 Digital I/O Output Valid	0
PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28]	pr<k>_iep0_edio_data_in_out[31:28]	I/O	IEP0 Digital I/Os Data In/Out	HiZ
PRG<k>_IEP0_EDC_SYNC_OUT0	pr<k>_iep0_edc_sync_out0	O	IEP0 Distributed Clock Sync Out	0
PRG<k>_IEP0_EDC_SYNC_OUT1	pr<k>_iep0_edc_sync_out1	O	IEP0 Distributed Clock Sync Out	0
PRG<k>_IEP0_EDC_LATCH_IN0	pr<k>_iep0_edc_latch_in0	I	IEP0 Distributed Clock Latch In	HiZ
PRG<k>_IEP0_EDC_LATCH_IN1	pr<k>_iep0_edc_latch_in1	I	IEP0 Distributed Clock Latch In	HiZ
Industrial Ethernet (IEP1)	Industrial Ethernet			
PRG<k>_IEP1_EDC_SYNC_OUT0	pr<k>_iep1_edc_sync_out0	O	IEP1 Distributed Clock Sync Out	0
PRG<k>_IEP1_EDC_SYNC_OUT1	pr<k>_iep1_edc_sync_out1	O	IEP1 Distributed Clock Sync Out	0
PRG<k>_IEP1_EDC_LATCH_IN0	pr<k>_iep1_edc_latch_in0	I	IEP1 Distributed Clock Latch In	HiZ
PRG<k>_IEP1_EDC_LATCH_IN1	pr<k>_iep1_edc_latch_in1	I	IEP1 Distributed Clock Latch In	HiZ
UART0	UART0			
PRG<k>_UART0_CTSn	pr<k>_uart0_cts_n	I	UART0 Clear to Send	HiZ
PRG<k>_UART0_RTSn	pr<k>_uart0_rts_n	O	UART0 Request to Send	1
PRG<k>_UART0_RXD	pr<k>_uart0_rxd	I	UART0 Receive Data	HiZ
PRG<k>_UART0_TXD	pr<k>_uart0_txd	O	UART0 Transmit Data	1
ECAP0	ECAP0			
PRG<k>_ECAP0_IN_APWM_OUT	pr<k>_ecap0_ecap_capin_apwm_o	I/O	Enhanced capture (ECAP0) input or Auxiliary PWM out	HiZ
PRG<k>_ECAP0_SYNC_IN	pr<k>_ecap0_ecap_syncin	I	Enhanced capture (ECAP0) Sync In	0

Table 6-53. PRU_ICSSG<k> I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing	I/O[1]	Description	Pin Reset [2]
PRG<k>_ECAP0_SYNC_OUT	pr<k>_ecap0_ecap_syncout	O	Enhanced capture (ECAP0) Sync Out	0
PWM				
PRG<k>_PWM0_A[2:0][3]	pr<k>_pwm_pwm0_[2:0]_pos	I/O	PWM Set 0 Positive In/Out	-
PRG<k>_PWM0_B[2:0][3]	pr<k>_pwm_pwm0_[2:0]_neg	I/O	PWM Set 0 Negative In/Out	-
PRG<k>_PWM0_TZ_IN	pr<k>_pwm_pwm0_trip_in	I	PWM Set 0 Tripzone Input	-
PRG<k>_PWM0_TZ_OUT	pr<k>_pwm_pwm0_trip_out	O	PWM Set 0 Tripzone Output	-
PRG<k>_PWM1_A[2:0][3]	pr<k>_pwm_pwm1_[2:0]_pos	I/O	PWM Set 1 Positive In/Out	-
PRG<k>_PWM1_B[2:0][3]	pr<k>_pwm_pwm1_[2:0]_neg	I/O	PWM Set 1 Negative In/Out	-
PRG<k>_PWM1_TZ_IN	pr<k>_pwm_pwm1_trip_in	I	PWM Set 1 Tripzone Input	-
PRG<k>_PWM1_TZ_OUT	pr<k>_pwm_pwm1_trip_out	O	PWM Set 1 Tripzone Output	-
PRG<k>_PWM2_A[2:0][3]	pr<k>_pwm_pwm2_[2:0]_pos	I/O	PWM Set 2 Positive In/Out	-
PRG<k>_PWM2_B[2:0][3]	pr<k>_pwm_pwm2_[2:0]_neg	I/O	PWM Set 2 Negative In/Out	-
PRG<k>_PWM2_TZ_IN	pr<k>_pwm_pwm2_trip_in	I	PWM Set 2 Tripzone Input	-
PRG<k>_PWM2_TZ_OUT	pr<k>_pwm_pwm2_trip_out	O	PWM Set 2 Tripzone Output	-
PRG<k>_PWM3_A[2:0][3]	pr<k>_pwm_pwm3_[2:0]_pos	I/O	PWM Set 3 Positive In/Out	-
PRG<k>_PWM3_B[2:0][3]	pr<k>_pwm_pwm3_[2:0]_neg	I/O	PWM Set 3 Negative In/Out	-
PRG<k>_PWM3_TZ_IN	pr<k>_pwm_pwm3_trip_in	I	PWM Set 3 Tripzone Input	-
PRG<k>_PWM3_TZ_OUT	pr<k>_pwm_pwm3_trip_out	O	PWM Set 3 Tripzone Output	-

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) PRG<k>_PWMm_A[2:0] = PRG<k>_PWMm_[2:0]_POS and PRG<k>_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG

(4) The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configuraitons, this is not necessarily a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SoC integration and this convention was maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

(5) When ICSSG_SA_MX_REG[7] G_MUX_EN = 0

(6) When ICSSG_SA_MX_REG[7] G_MUX_EN = 1

(7) 1 = STATIC HIGH

6.4.2.2 PRU_ICSSG Fast GPIO pins

Each PRU_ICSSG PRU processor implements fast general purpose outputs (GPO) through its R30 register and fast general purpose inputs (GPI) through its R31 register. The device multiplexes all GPI signals and their corresponding GPO signals onto the same device pin using different device multiplexing modes. In some applications it may be necessary for the PRU to switch between GPO and GPI operation in a fast (or at least a deterministic) manner. This is not possible using SoC level pin muxing since each pin being switched requires a write to a separate pin configuration register located in Control Module (CTRL_MMR0).

In order to address the fast switching issue, special I/O pin connectivity for the PRU_ICSSG GPO/GPI pins is implemented. This feature makes use of the IEP EDIO signal controls to provide input/output switching using a single SoC level pin multiplexing mode.

The IEP EDIO interface has 32 data input (DATA_IN) and 32 data output (DATA_OUT) signals. It also has a set of 32 corresponding data output enable (DATA_OUT_EN) signals to be used as (active low) output driver enables to allow each DATA_OUT/DATA_IN to be implemented as a bidirectional pin. On this device, only 4 of the IEP0 EDIO (and none of the IEP1 EDIO) I/Os of each PRU_ICSSG module are pinned out (PRG[2:0]_IEP0_EDIO_DATA_IN_OUT[31:28]). This leaves a majority of the DATA_OUT_EN signals unused. The device allows these unused output enables to be optionally re-purposed for use as GPO enables. This allows each ICSSG GP pin to function as either a GPO or as a GPI when the I/O pin is configured for the GPO muxmode.

A set of SoC level registers (CTRLMMR_ICSSG[2:0]_CTRL[2:0]) are used to determine the behavior of each GPO mode pin. When a register’s [19-0]GPM_BIDI bit field is set to 0h (default value), the corresponding GPO pin operates only as an output when the GPO multiplexing mode is selected and is driven with the R30 bit value. The corresponding GPI signal (ICSSG GPI<n> input, where n = 0 to 19) is driven low. When a register’s [19-0]GPM_BIDI bit field is set to 1h, the corresponding ICSSG_DIGIO_DATA_OUT_EN_REG[31-0] DATA_OUT_EN bit field is used to control the GPO output buffer. If [31-0] DATA_OUT_EN bit field is set to 0h the output is driven and the pin acts as a GPO. If [31-0] DATA_OUT_EN bit field is set to 1h the output is disabled and the pin acts as a GPI.

Figure 6-19 shows the PRU_ICSSGm GPO/GPI pin connectivity. The PRU[1:0]_GPM[19:0] output signals are propagated to the PRG[2:0]_PRU[1:0]_GPO[19:0] pins using Muxmode 0 function and the PRU[1:0]_GPN[19:0] input signals are propagated to the PRG[2:0]_PRU[1:0]_GPI[19:0] pins using Muxmode 1 function. Any GPO (Muxmode 0 function) can be made bidirectional by setting the corresponding bit field [19-0]GPM_BIDI in CTRLMMR_ICSSG[2:0]_CTRL[2:0] register.

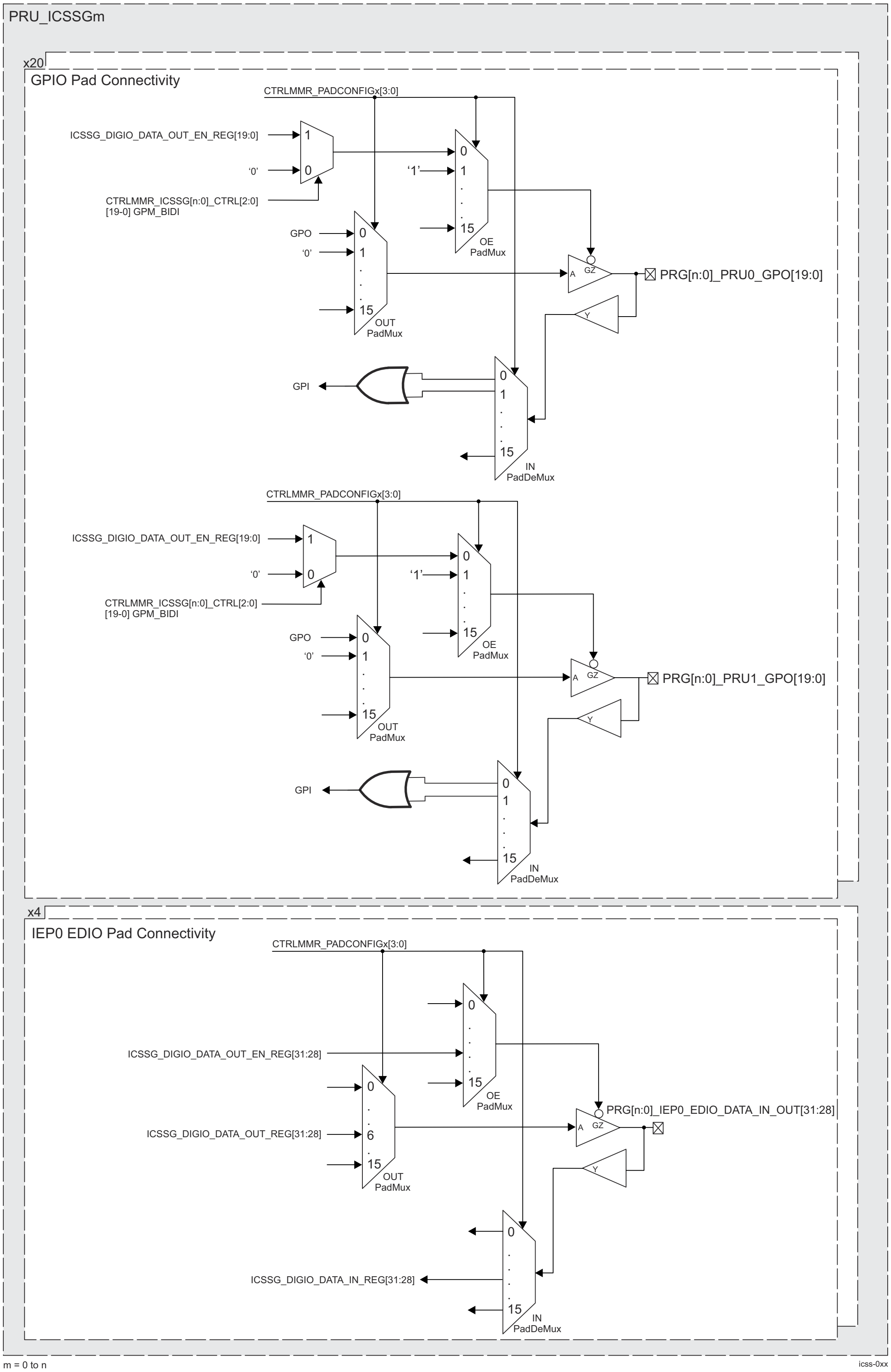

Figure 6-19. PRU_ICSSG GPO/GPI pin Connectivity

Note

n is the number of PRU_ISCCG in the device. See the Datasheet for additional details.

6.4.3 PRU_ICSSG Integration

The PRU_ICSSG0 and PRU_ICSSG1 subsystems integration in the device is shown in Figure 6-20 and Figure 6-21.

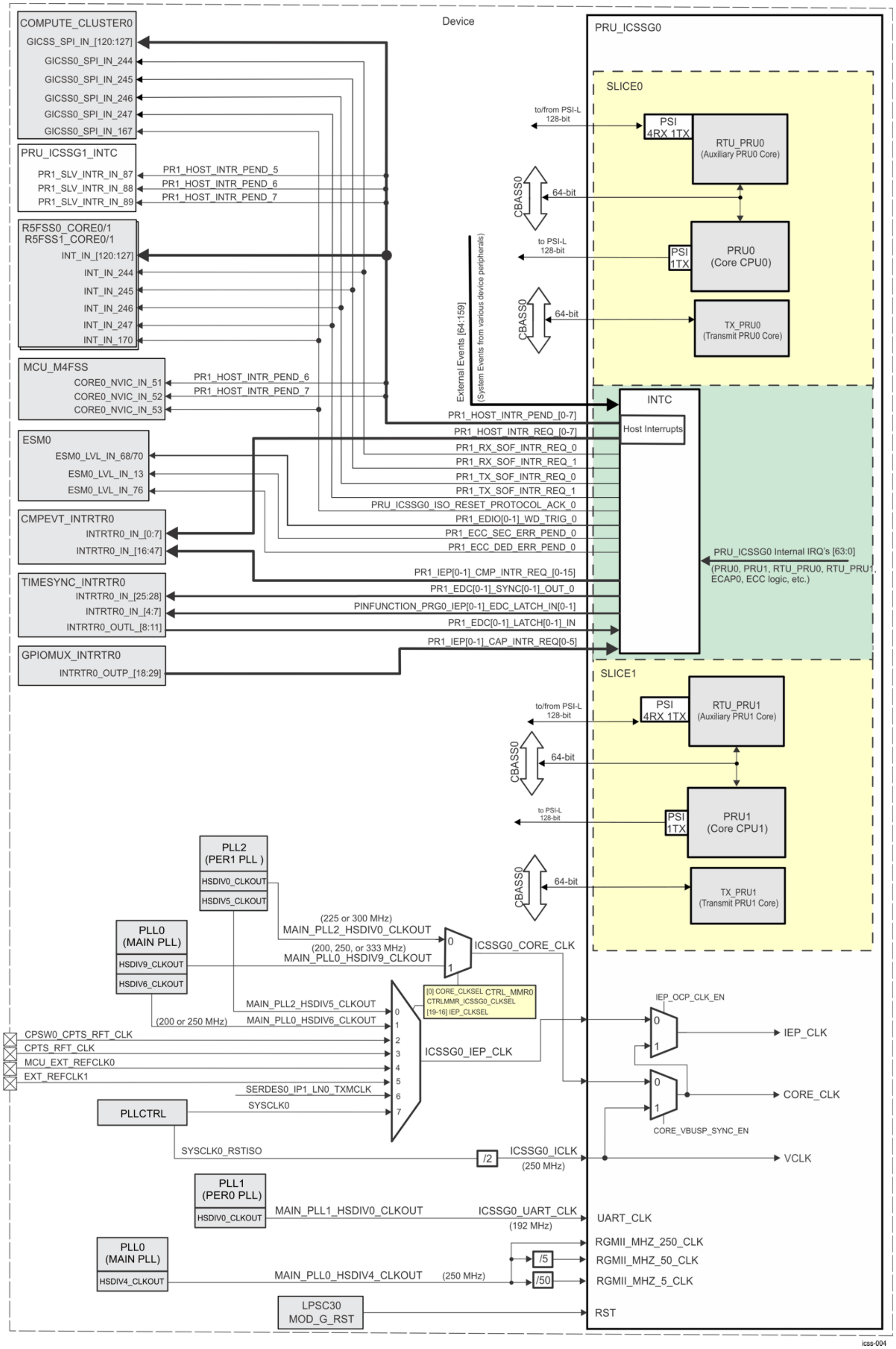

Figure 6-20. PRU_ICSSG0 Integration

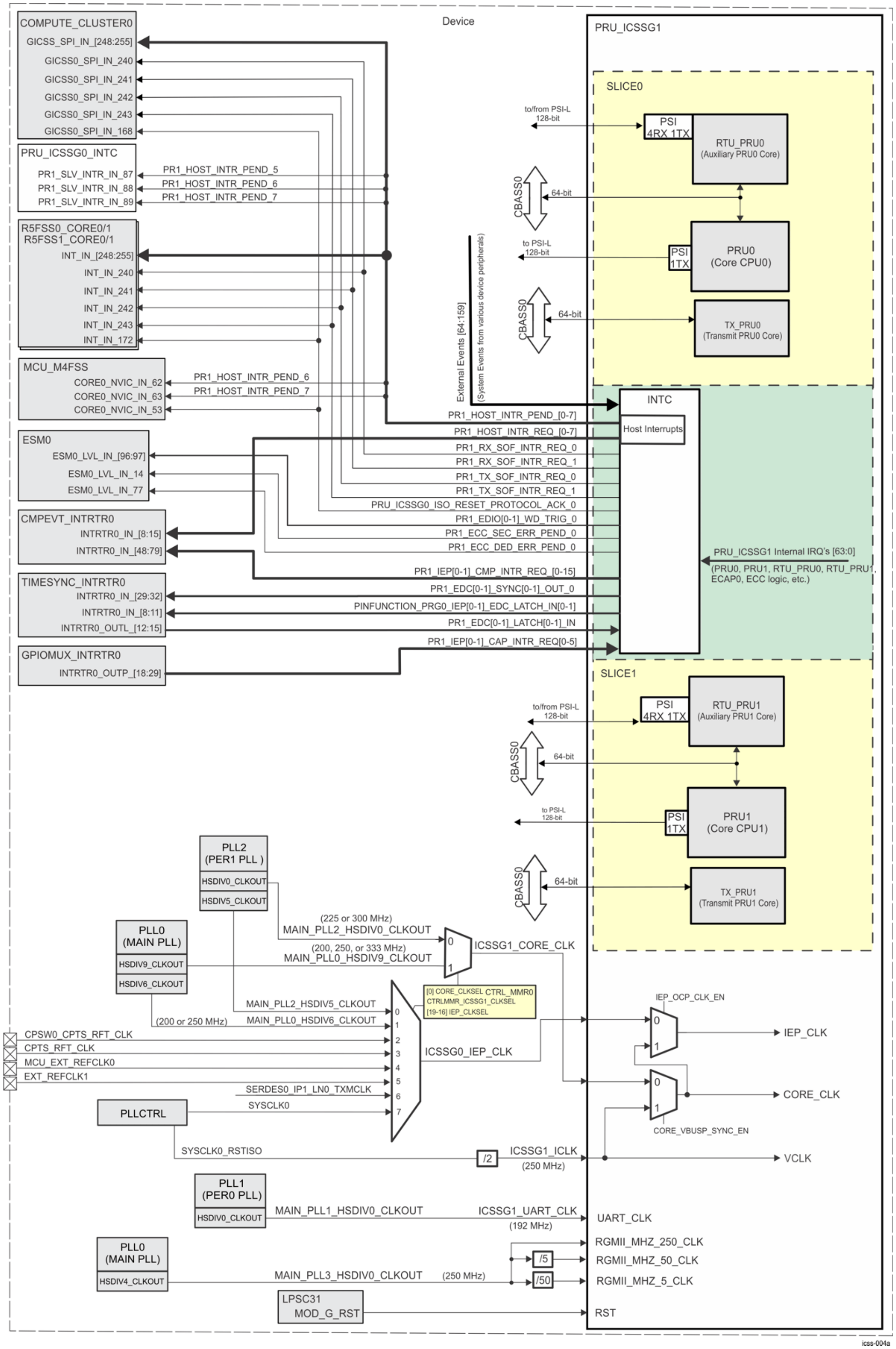

Figure 6-21. PRU_ICSSG1 Integration

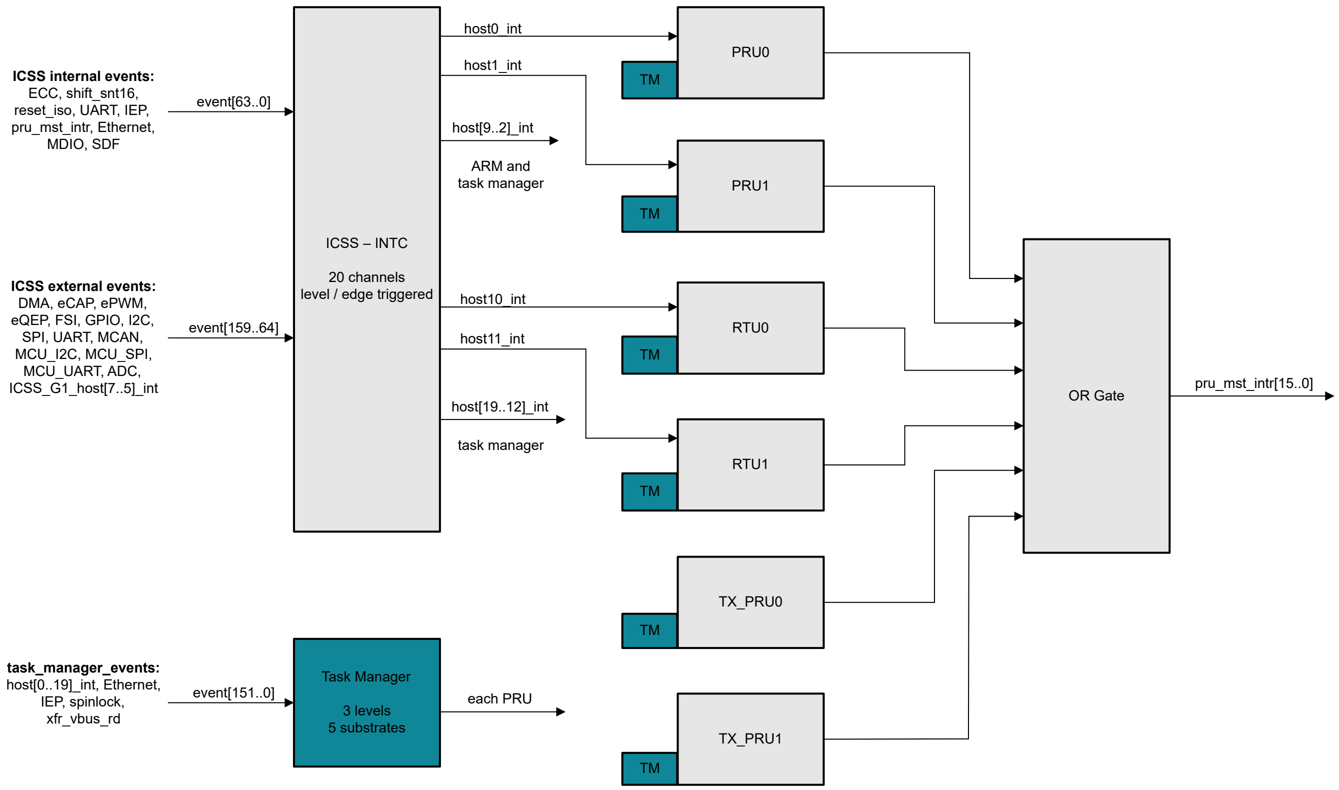

Figure 6-22. ICSS Interrupt and Task Manager Event Routing

The PRU_ICSSG0 and PRU_ICSSG1 integration in the device features:

- PD6 and PD7 power domains instantiation
- One controller port for each Slice (shared between PRU0/RTU_PRU0 and PRU1/RTU_PRU1 core initiators) on the device CBASS0 interconnect
- One target (configuration) port on the CBASS0 interconnect for device hosts (Compute cluster: dual Arm Cortex-A72) to access various memories and registers of PRU_ICSSG
- 20 output interrupt events from local interrupt controllers — INTC:
  - 2 events to each PRU and TX_PRU core (events 0 and 1)
  - 2 events (event 10 and 11) are connected to both auxiliary cores (RTU_PRU0 and RTU_PRU1)
  - 8 events (ICSSG_n_HOST_INTi, where n = 0 or 1 and i = 0 to 7), exported from PRU_ICSSGn (where n = 0 or 1) internal INTC's and mapped to the device interrupt controllers
  - 8 events (event 12 through 19) mapped to each of the 6 Task Managers
- A local software gating of clocks to several modules within PRU subsystem (local clock management protocol), as follows:
  - IEP0 and IEP1
  - ECAP0
  - UART0
  - INTC
  - SLICE0
  - SLICE1
- 7 input clocks obtained from device PLL0 (MAIN PLL), PLL1 (PER0 PLLL), PLL2 (PER1 PLL) and PLLCTRL :
  - a ICSSGn_CORE_CLK (where n = 0 or 1) core clock
  - a ICSSGn_IEP_CLK functional clock
  - a ICSSGn_ICLK interface clock
  - a ICSSGn_UART_CLK clock
  - a RGMII_MHZ_250_CLK reference clock
  - a RGMII_MHZ_50_CLK reference clock
  - a RGMII_MHZ_5_CLK reference clock
- Two input clocks: RGMII0_RXC_I and RGMII1_RXC_I and 2 output clocks: RGMII0_TXC_O and RGMII1_TXC_O, passed as external clocks on device I/Os
- One MDIO_MDCLK, passed as external clock on device I/Os
- One hardware non-retention (level sensitive) reset

Table 6-54 through Table 6-59 summarize the integration of PRU_ICSSG0 and PRU_ICSSG1 modules in the device.

Table 6-54. PRU_ICSSG Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
PRU_ICSSG0	PSC0	PD6	LPSC30	CBASS0
PRU_ICSSG1	PSC0	PD7	LPSC31	CBASS0

PRU_ICSSG Clocks

Table 6-55. PRU_ICSSG Clocks

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
PRU_ICSSG0	ICSSG0_CORE_CLK	MAIN_PLL2_HSDIV0_CLKOUT	HSDIV0 of PLL2 (PER1 PLL)	PRU_ICSSG0 Core clock. Selected through CTRLMMR_ICSSG0_CLKSEL[0] CORE_CLKSEL.
		MAIN_PLL0_HSDIV9_CLKOUT	HSDIV9 of PLL0 (MAIN PLL)	
	ICSSG0_IEP_CLK	MAIN_PLL2_HSDIV5_CLKOUT	HSDIV5 of PLL2 (PER1 PLL)	PRU_ICSSG0 Industrial Ethernet Peripheral functional clock. Selected through CTRLMMR_ICSSG0_CLKSEL[19-16] IEP_CLKSEL.
		MAIN_PLL0_HSDIV6_CLKOUT	HSDIV6 of PLL0 (MAIN PLL)	
		CPSW0_CPTS_RFT_CLK	CPSW0_CPTS_RFT_CLK pin	
		CPTS_RFT_CLK	CPTS_RFT_CLK pin	
		MCU_EXT_REFCLK0	MCU_EXT_REFCLK0 pin	
		EXT_REFCLK1	EXT_REFCLK1 pin	
		SERDES0_IP1_LN0_TXMCLK	SERDES0, Lane 0, PCIe0	
		SYSCLK0	PLLCTRL	
	ICSSG0_ICLK	SYSCLK0_RSTISO/2	PLLCTRL	PRU_ICSSG0 Interface clock. Clocks both VBUSP target and VBUSM controller ports.
	ICSSG0_UART_CLK	MAIN_PLL1_HSDIV0_CLKOUT	HSDIV0 of PLL1 (PER0 PLL)	PRU_ICSSG0 UART0 functional clock.
	RGMII_MHZ_250_CLK	MAIN_PLL0_HSDIV4_CLKOUT	HSDIV4 of PLL0 (MAIN PLL)	RGMII 250-MHz reference clock
	RGMII_MHZ_50_CLK	MAIN_PLL0_HSDIV4_CLKOUT/5	HSDIV4 of PLL0 (MAIN PLL)	RGMII 50-MHz reference clock
	RGMII_MHZ_5_CLK	MAIN_PLL0_HSDIV4_CLKOUT/50	HSDIV4 of PLL0 (MAIN PLL)	RGMII 5-MHz reference clock
PRU_ICSSG1	ICSSG1_CORE_CLK	MAIN_PLL2_HSDIV0_CLKOUT	HSDIV0 of PLL2 (PER1 PLL)	PRU_ICSSG1 Core clock. Selected through CTRLMMR_ICSSG1_CLKSEL[0] CORE_CLKSEL.
		MAIN_PLL0_HSDIV9_CLKOUT	HSDIV9 of PLL0 (MAIN PLL)	
	ICSSG1_IEP_CLK	MAIN_PLL2_HSDIV5_CLKOUT	HSDIV5 of PLL2 (PER1 PLL)	PRU_ICSSG1 Industrial Ethernet Peripheral functional clock. Selected through CTRLMMR_ICSSG1_CLKSEL[19-16] IEP_CLKSEL.
		MAIN_PLL0_HSDIV6_CLKOUT	HSDIV6 of PLL0 (MAIN PLL)	
		CPSW0_CPTS_RFT_CLK	CPSW0_CPTS_RFT_CLK pin	
		CPTS_RFT_CLK	CPTS_RFT_CLK pin	
		MCU_EXT_REFCLK0	MCU_EXT_REFCLK0 pin	
		EXT_REFCLK1	EXT_REFCLK1 pin	
		SERDES0_IP1_LN0_TXMCLK	SERDES0, Lane 0, PCIe0	
		SYSCLK0	PLLCTRL	
	ICSSG1_ICLK	SYSCLK0_RSTISO/2	PLLCTRL	PRU_ICSSG1 Interface clock. Clocks both VBUSP target and VBUSM controller ports.
	ICSSG1_UART_CLK	MAIN_PLL1_HSDIV0_CLKOUT	HSDIV0 of PLL1 (PER0 PLL)	PRU_ICSSG1 UART0 functional clock.
	RGMII_MHZ_250_CLK	MAIN_PLL0_HSDIV4_CLKOUT	HSDIV4 of PLL0 (MAIN PLL)	RGMII 250-MHz reference clock

Table 6-55. PRU_ICSSG Clocks (continued)

	RGMII_MHZ_50_CLK	MAIN_PLL0_HSDIV4_CLKOUT/5	HSDIV4 of PLL0 (MAIN PLL)	RGMII 50-MHz reference clock
	RGMII_MHZ_5_CLK	MAIN_PLL0_HSDIV4_CLKOUT/50	HSDIV4 of PLL0 (MAIN PLL)	RGMII 5-MHz reference clock

Table 6-56. PRU_ICSSG Resets

Resets				
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
PRU_ICSSG0	ICSSG0_RST	MOD_G_RST	LPSC30	Module Reset
PRU_ICSSG1	ICSSG1_RST	MOD_G_RST	LPSC31	Module Reset

Table 6-57. PRU_ICSSG Interrupt Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Type**	**Description**
PRU_ICSSG0	PRU_ICSSG0_PR1_HOST_INTR_PEND_0	GICSS0_SPI_IN_120	COMPUTE_CLUSTER0	Level	Host interrupt 0
		R5FSS0_CORE0_INTR_IN_120	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_120	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_120	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_120	R5FSS1_CORE1		
	PRU_ICSSG0_PR1_HOST_INTR_PEND_1	GICSS0_SPI_IN_121	COMPUTE_CLUSTER0	Level	Host interrupt 1
		R5FSS0_CORE0_INTR_IN_121	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_121	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_121	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_121	R5FSS1_CORE1		
	PRU_ICSSG0_PR1_HOST_INTR_PEND_2	GICSS0_SPI_IN_122	COMPUTE_CLUSTER0	Level	Host interrupt 2
		R5FSS0_CORE0_INTR_IN_122	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_122	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_122	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_122	R5FSS1_CORE1		
	PRU_ICSSG0_PR1_HOST_INTR_PEND_3	GICSS0_SPI_IN_123	COMPUTE_CLUSTER0	Level	Host interrupt 3
		R5FSS0_CORE0_INTR_IN_123	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_123	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_123	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_123	R5FSS1_CORE1		
	PRU_ICSSG0_PR1_HOST_INTR_PEND_4	GICSS0_SPI_IN_124	COMPUTE_CLUSTER0	Level	Host interrupt 4
		R5FSS0_CORE0_INTR_IN_124	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_124	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_124	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_124	R5FSS1_CORE1		

Table 6-57. PRU_ICSSG Interrupt Requests (continued)

PRU_ICSSG0_PR1_HOST_INTR_PEND_5	GICSS0_SPI_IN_125	COMPUTE_CLUSTER0	Level	Host interrupt 5
	R5FSS0_CORE0_INTR_IN_125	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_125	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_125	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_125	R5FSS1_CORE1		
	PRU_ICSSG1_PR1_SLV_IN_87	PRU_ICSSG1		
PRU_ICSSG0_PR1_HOST_INTR_PEND_6	GICSS0_SPI_IN_126	COMPUTE_CLUSTER0	Level	Host interrupt 6
	R5FSS0_CORE0_INTR_IN_126	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_126	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_126	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_126	R5FSS1_CORE1		
	MCU_M4FSS0_CORE0_NVIC_IN_51	MCU_M4FSS		
	PRU_ICSSG1_PR1_SLV_IN_88	PRU_ICSSG1		
PRU_ICSSG0_PR1_HOST_INTR_PEND_7	GICSS0_SPI_IN_127	COMPUTE_CLUSTER0	Level	Host interrupt 7
	R5FSS0_CORE0_INTR_IN_127	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_127	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_127	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_127	R5FSS1_CORE1		
	MCU_M4FSS0_CORE0_NVIC_IN_52	MCU_M4FSS		
	PRU_ICSSG1_PR1_SLV_IN_89	PRU_ICSSG1		
PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_0	GICSS0_SPI_IN_244	COMPUTE_CLUSTER0	Pulse	Receive SOF 0 interrupt
	R5FSS0_CORE0_INTR_IN_244	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_244	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_244	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_244	R5FSS1_CORE1		
PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_1	GICSS0_SPI_IN_245	COMPUTE_CLUSTER0	Pulse	Receive SOF 1 interrupt
	R5FSS0_CORE0_INTR_IN_245	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_245	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_245	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_245	R5FSS1_CORE1		
PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_0	GICSS0_SPI_IN_246	COMPUTE_CLUSTER0	Pulse	Transmit SOF 0 interrupt
	R5FSS0_CORE0_INTR_IN_246	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_246	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_246	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_246	R5FSS1_CORE1		
PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_1	GICSS0_SPI_IN_247	COMPUTE_CLUSTER0	Pulse	Transmit SOF 1 interrupt
	R5FSS0_CORE0_INTR_IN_247	R5FSS0_CORE0		

Table 6-57. PRU_ICSSG Interrupt Requests (continued)

		R5FSS0_CORE1_INTR_IN_247	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_247	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_247	R5FSS1_CORE1		
	PRU_ICSSG0_PR1_EDIO0_WD_TRIG_0	ESM0_LVL_IN_68	ESM0	Level	EDIO0 watchdog trigger interrupt
	PRU_ICSSG0_PR1_EDIO1_WD_TRIG_0	ESM0_LVL_IN_70	ESM0	Level	EDIO1 watchdog trigger interrupt
	PRU_ICSSG0_PR1_ECC_SEC_ERR_PEND_0	ESM0_LVL_IN_13	ESM0	Level	SEC ECC error interrupt
	PRU_ICSSG0_PR1_ECC_DED_ERR_PEND_0	ESM0_LVL_IN_76	ESM0	Level	DED ECC error interrupt
	PRU_ICSSG0_ISO_RESET_PROTOCOL_ACK_0	MCU_M4FSS0_CORE0_NVIC_IN_53	MCU_M4FSS	Pulse	ISO reset interrupt
		GICSS0_SPI_IN_167	COMPUTE_CLUSTER0		
		R5FSS0_CORE0_INTR_IN_170	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_170	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_170	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_170	R5FSS1_CORE1		
PRU_ICSSG1	PRU_ICSSG1_PR1_HOST_INTR_PEND_0	GICSS0_SPI_IN_248	COMPUTE_CLUSTER0	Level	Host interrupt 0
		R5FSS0_CORE0_INTR_IN_248	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_248	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_248	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_248	R5FSS1_CORE1		
	PRU_ICSSG1_PR1_HOST_INTR_PEND_1	GICSS0_SPI_IN_249	COMPUTE_CLUSTER0	Level	Host interrupt 1
		R5FSS0_CORE0_INTR_IN_249	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_249	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_249	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_249	R5FSS1_CORE1		
	PRU_ICSSG1_PR1_HOST_INTR_PEND_2	GICSS0_SPI_IN_250	COMPUTE_CLUSTER0	Level	Host interrupt 2
		R5FSS0_CORE0_INTR_IN_250	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_250	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_250	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_250	R5FSS1_CORE1		
	PRU_ICSSG1_PR1_HOST_INTR_PEND_3	GICSS0_SPI_IN_251	COMPUTE_CLUSTER0	Level	Host interrupt 3
		R5FSS0_CORE0_INTR_IN_251	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_251	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_251	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_251	R5FSS1_CORE1		
	PRU_ICSSG1_PR1_HOST_INTR_PEND_4	GICSS0_SPI_IN_252	COMPUTE_CLUSTER0	Level	Host interrupt 4
		R5FSS0_CORE0_INTR_IN_252	R5FSS0_CORE0		

Table 6-57. PRU_ICSSG Interrupt Requests (continued)

	R5FSS0_CORE1_INTR_IN_252	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_252	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_252	R5FSS1_CORE1		
PRU_ICSSG1_PR1_HOST_INTR_PEND_5	GICSS0_SPI_IN_253	COMPUTE_CLUSTER0	Level	Host interrupt 5
	R5FSS0_CORE0_INTR_IN_253	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_253	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_253	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_253	R5FSS1_CORE1		
	PRU_ICSSG0_PR1_SLV_IN_87	PRU_ICSSG0		
PRU_ICSSG1_PR1_HOST_INTR_PEND_6	GICSS0_SPI_IN_254	COMPUTE_CLUSTER0	Level	Host interrupt 6
	R5FSS0_CORE0_INTR_IN_254	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_254	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_254	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_254	R5FSS1_CORE1		
	MCU_M4FSS0_CORE0_NVIC_IN_62	MCU_M4FSS		
	PRU_ICSSG0_PR1_SLV_IN_88	PRU_ICSSG0		
PRU_ICSSG1_PR1_HOST_INTR_PEND_7	GICSS0_SPI_IN_255	COMPUTE_CLUSTER0	Level	Host interrupt 7
	R5FSS0_CORE0_INTR_IN_255	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_255	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_255	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_255	R5FSS1_CORE1		
	MCU_M4FSS0_CORE0_NVIC_IN_63	MCU_M4FSS		
	PRU_ICSSG0_PR1_SLV_IN_89	PRU_ICSSG0		
PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_0	GICSS0_SPI_IN_240	COMPUTE_CLUSTER0	Pulse	Receive SOF 0 interrupt
	R5FSS0_CORE0_INTR_IN_240	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_240	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_240	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_240	R5FSS1_CORE1		
PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_1	GICSS0_SPI_IN_241	COMPUTE_CLUSTER0	Pulse	Receive SOF 1 interrupt
	R5FSS0_CORE0_INTR_IN_241	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_241	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_241	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_241	R5FSS1_CORE1		
PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_0	GICSS0_SPI_IN_242	COMPUTE_CLUSTER0	Pulse	Transmit SOF 0 interrupt
	R5FSS0_CORE0_INTR_IN_242	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_242	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_242	R5FSS1_CORE0		

Table 6-57. PRU_ICSSG Interrupt Requests (continued)

	R5FSS1_CORE1_INTR_IN_242	R5FSS1_CORE1		
PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_1	GICSS0_SPI_IN_243	COMPUTE_CLUSTER0	Pulse	Transmit SOF 1 interrupt
	R5FSS0_CORE0_INTR_IN_243	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_243	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_243	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_243	R5FSS1_CORE1		
PRU_ICSSG1_PR1_EDIO0_WD_TRIG_0	ESM0_LVL_IN_96	ESM0	Level	EDIO0 watchdog trigger interrupt
PRU_ICSSG1_PR1_EDIO1_WD_TRIG_0	ESM0_LVL_IN_97	ESM0	Level	EDIO1 watchdog trigger interrupt
PRU_ICSSG1_PR1_ECC_SEC_ERR_PEND_0	ESM0_LVL_IN_14	ESM0	Level	SEC ECC error interrupt
PRU_ICSSG1_PR1_ECC_DED_ERR_PEND_0	ESM0_LVL_IN_77	ESM0	Level	DED ECC error interrupt
PRU_ICSSG1_ISO_RESET_PROTOCOL_ACK_0	MCU_M4FSS0_CORE0_NVIC_IN_54	MCU_M4FSS	Pulse	ISO reset interrupt
	GICSS0_SPI_IN_168	COMPUTE_CLUSTER0		
	R5FSS0_CORE0_INTR_IN_172	R5FSS0_CORE0		
	R5FSS0_CORE1_INTR_IN_172	R5FSS0_CORE1		
	R5FSS1_CORE0_INTR_IN_172	R5FSS1_CORE0		
	R5FSS1_CORE1_INTR_IN_172	R5FSS1_CORE1		

Table 6-58. PRU_ICSSG Compare Event Requests

	Compare Event Outputs			
Module Event	**Destination Event Input**	**Destination**	**Type**	**Description**
PRU_ICSSG0_PR1_HOST_INTR_REQ_0	CMPEVENT_INTRTR0_IN_0	CMPEVT_INTRTR0	Pulse	Host interrupt request 0
PRU_ICSSG0_PR1_HOST_INTR_REQ_1	CMPEVENT_INTRTR0_IN_1	CMPEVT_INTRTR0	Pulse	Host interrupt request 1
PRU_ICSSG0_PR1_HOST_INTR_REQ_2	CMPEVENT_INTRTR0_IN_2	CMPEVT_INTRTR0	Pulse	Host interrupt request 2
PRU_ICSSG0_PR1_HOST_INTR_REQ_3	CMPEVENT_INTRTR0_IN_3	CMPEVT_INTRTR0	Pulse	Host interrupt request 3
PRU_ICSSG0_PR1_HOST_INTR_REQ_4	CMPEVENT_INTRTR0_IN_4	CMPEVT_INTRTR0	Pulse	Host interrupt request 4
PRU_ICSSG0_PR1_HOST_INTR_REQ_5	CMPEVENT_INTRTR0_IN_5	CMPEVT_INTRTR0	Pulse	Host interrupt request 5
PRU_ICSSG0_PR1_HOST_INTR_REQ_6	CMPEVENT_INTRTR0_IN_6	CMPEVT_INTRTR0	Pulse	Host interrupt request 6
PRU_ICSSG0_PR1_HOST_INTR_REQ_7	CMPEVENT_INTRTR0_IN_7	CMPEVT_INTRTR0	Pulse	Host interrupt request 7
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_0	CMPEVENT_INTRTR0_IN_16	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 0 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_1	CMPEVENT_INTRTR0_IN_17	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 1 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_2	CMPEVENT_INTRTR0_IN_18	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 2 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_3	CMPEVENT_INTRTR0_IN_19	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 3 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_4	CMPEVENT_INTRTR0_IN_20	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 4 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_5	CMPEVENT_INTRTR0_IN_21	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 5 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_6	CMPEVENT_INTRTR0_IN_22	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 6 interrupt

Table 6-58. PRU_ICSSG Compare Event Requests (continued)

PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_7	CMPEVENT_INTRTR0_IN_23	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 7 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_8	CMPEVENT_INTRTR0_IN_24	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 8 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_9	CMPEVENT_INTRTR0_IN_25	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 9 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_10	CMPEVENT_INTRTR0_IN_26	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 10 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_11	CMPEVENT_INTRTR0_IN_27	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 11 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_12	CMPEVENT_INTRTR0_IN_28	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 12 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_13	CMPEVENT_INTRTR0_IN_29	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 13 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_14	CMPEVENT_INTRTR0_IN_30	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 14 interrupt
PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_15	CMPEVENT_INTRTR0_IN_31	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 15 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_0	CMPEVENT_INTRTR0_IN_32	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 0 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_1	CMPEVENT_INTRTR0_IN_33	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 1 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_2	CMPEVENT_INTRTR0_IN_34	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 2 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_3	CMPEVENT_INTRTR0_IN_35	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 3 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_4	CMPEVENT_INTRTR0_IN_36	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 4 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_5	CMPEVENT_INTRTR0_IN_37	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 5 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_6	CMPEVENT_INTRTR0_IN_38	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 6 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_7	CMPEVENT_INTRTR0_IN_39	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 7 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_8	CMPEVENT_INTRTR0_IN_40	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 8 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_9	CMPEVENT_INTRTR0_IN_41	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 9 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_10	CMPEVENT_INTRTR0_IN_42	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 10 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_11	CMPEVENT_INTRTR0_IN_43	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 11 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_12	CMPEVENT_INTRTR0_IN_44	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 12 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_13	CMPEVENT_INTRTR0_IN_45	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 13 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_14	CMPEVENT_INTRTR0_IN_46	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 14 interrupt
PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_15	CMPEVENT_INTRTR0_IN_47	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 15 interrupt
PRU_ICSSG1_PR1_HOST_INTR_REQ_0	CMPEVENT_INTRTR0_IN_8	CMPEVT_INTRTR0	Pulse	Host interrupt request 0
PRU_ICSSG1_PR1_HOST_INTR_REQ_1	CMPEVENT_INTRTR0_IN_9	CMPEVT_INTRTR0	Pulse	Host interrupt request 1
PRU_ICSSG1_PR1_HOST_INTR_REQ_2	CMPEVENT_INTRTR0_IN_10	CMPEVT_INTRTR0	Pulse	Host interrupt request 2
PRU_ICSSG1_PR1_HOST_INTR_REQ_3	CMPEVENT_INTRTR0_IN_11	CMPEVT_INTRTR0	Pulse	Host interrupt request 3
PRU_ICSSG1_PR1_HOST_INTR_REQ_4	CMPEVENT_INTRTR0_IN_12	CMPEVT_INTRTR0	Pulse	Host interrupt request 4
PRU_ICSSG1_PR1_HOST_INTR_REQ_5	CMPEVENT_INTRTR0_IN_13	CMPEVT_INTRTR0	Pulse	Host interrupt request 5
PRU_ICSSG1_PR1_HOST_INTR_REQ_6	CMPEVENT_INTRTR0_IN_14	CMPEVT_INTRTR0	Pulse	Host interrupt request 6
PRU_ICSSG1_PR1_HOST_INTR_REQ_7	CMPEVENT_INTRTR0_IN_15	CMPEVT_INTRTR0	Pulse	Host interrupt request 7
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_0	CMPEVENT_INTRTR0_IN_48	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 0 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_1	CMPEVENT_INTRTR0_IN_49	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 1 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_2	CMPEVENT_INTRTR0_IN_50	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 2 interrupt

Table 6-58. PRU_ICSSG Compare Event Requests (continued)

PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_3	CMPEVENT_INTRTR0_IN_51	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 3 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_4	CMPEVENT_INTRTR0_IN_52	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 4 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_5	CMPEVENT_INTRTR0_IN_53	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 5 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_6	CMPEVENT_INTRTR0_IN_54	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 6 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_7	CMPEVENT_INTRTR0_IN_55	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 7 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_8	CMPEVENT_INTRTR0_IN_56	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 8 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_9	CMPEVENT_INTRTR0_IN_57	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 9 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_10	CMPEVENT_INTRTR0_IN_58	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 10 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_11	CMPEVENT_INTRTR0_IN_59	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 11 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_12	CMPEVENT_INTRTR0_IN_60	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 12 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_13	CMPEVENT_INTRTR0_IN_61	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 13 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_14	CMPEVENT_INTRTR0_IN_62	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 14 interrupt
PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_15	CMPEVENT_INTRTR0_IN_63	CMPEVT_INTRTR0	Pulse	IEP0 Compare timer 15 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_0	CMPEVENT_INTRTR0_IN_64	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 0 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_1	CMPEVENT_INTRTR0_IN_65	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 1 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_2	CMPEVENT_INTRTR0_IN_66	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 2 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_3	CMPEVENT_INTRTR0_IN_67	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 3 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_4	CMPEVENT_INTRTR0_IN_68	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 4 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_5	CMPEVENT_INTRTR0_IN_69	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 5 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_6	CMPEVENT_INTRTR0_IN_70	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 6 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_7	CMPEVENT_INTRTR0_IN_71	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 7 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_8	CMPEVENT_INTRTR0_IN_72	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 8 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_9	CMPEVENT_INTRTR0_IN_73	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 9 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_10	CMPEVENT_INTRTR0_IN_74	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 10 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_11	CMPEVENT_INTRTR0_IN_75	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 11 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_12	CMPEVENT_INTRTR0_IN_76	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 12 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_13	CMPEVENT_INTRTR0_IN_77	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 13 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_14	CMPEVENT_INTRTR0_IN_78	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 14 interrupt
PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_15	CMPEVENT_INTRTR0_IN_79	CMPEVT_INTRTR0	Pulse	IEP1 Compare timer 15 interrupt
Capture Event Input				
Module Sync Input	**Sync Source Signal**	**Source**	**Type**	**Description**
PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ0	MAIN_GPIOMUX_INTRTR0_OUTP_18	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 0
PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ1	MAIN_GPIOMUX_INTRTR0_OUTP_19	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 1
PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ2	MAIN_GPIOMUX_INTRTR0_OUTP_20	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 2
PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ3	MAIN_GPIOMUX_INTRTR0_OUTP_21	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 3
PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ4	MAIN_GPIOMUX_INTRTR0_OUTP_22	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 4

Table 6-58. PRU_ICSSG Compare Event Requests (continued)

PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ5	MAIN_GPIOMUX_INTRTR0_OUTP_23	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 5
PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ0	MAIN_GPIOMUX_INTRTR0_OUTP_24	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 0
PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ1	MAIN_GPIOMUX_INTRTR0_OUTP_25	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 1
PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ2	MAIN_GPIOMUX_INTRTR0_OUTP_26	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 2
PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ3	MAIN_GPIOMUX_INTRTR0_OUTP_27	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 3
PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ4	MAIN_GPIOMUX_INTRTR0_OUTP_28	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 4
PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ5	MAIN_GPIOMUX_INTRTR0_OUTP_29	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 5
PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ0	MAIN_GPIOMUX_INTRTR0_OUTP_18	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 0
PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ1	MAIN_GPIOMUX_INTRTR0_OUTP_19	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 1
PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ2	MAIN_GPIOMUX_INTRTR0_OUTP_20	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 2
PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ3	MAIN_GPIOMUX_INTRTR0_OUTP_21	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 3
PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ4	MAIN_GPIOMUX_INTRTR0_OUTP_22	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 4
PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ5	MAIN_GPIOMUX_INTRTR0_OUTP_23	GPIOMUX_INTRTR0	Pulse	IEP0 Capture event 5
PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ0	MAIN_GPIOMUX_INTRTR0_OUTP_24	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 0
PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ1	MAIN_GPIOMUX_INTRTR0_OUTP_25	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 1
PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ2	MAIN_GPIOMUX_INTRTR0_OUTP_26	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 2
PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ3	MAIN_GPIOMUX_INTRTR0_OUTP_27	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 3
PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ4	MAIN_GPIOMUX_INTRTR0_OUTP_28	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 4
PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ5	MAIN_GPIOMUX_INTRTR0_OUTP_29	GPIOMUX_INTRTR0	Pulse	IEP1 Capture event 5

Table 6-59. PRU_ICSSG Time Sync Event Requests

Time Sync Event Inputs

Module Instance	Module Sync Input	Sync Source Signal	Source	Type	Description
PRU_ICSSG0	PRU_ICSSG0_PR1_EDC0_LATCH0_IN	TIMESYNC_INTRTR0_OUTL_8	TIMESYNC_INTRTR0	Level	Selectable time sync event 8
	PRU_ICSSG0_PR1_EDC0_LATCH1_IN	TIMESYNC_INTRTR0_OUTL_9	TIMESYNC_INTRTR0	Level	Selectable time sync event 9
	PRU_ICSSG0_PR1_EDC1_LATCH0_IN	TIMESYNC_INTRTR0_OUTL_10	TIMESYNC_INTRTR0	Level	Selectable time sync event 10
	PRU_ICSSG0_PR1_EDC1_LATCH1_IN	TIMESYNC_INTRTR0_OUTL_11	TIMESYNC_INTRTR0	Level	Selectable time sync event 11
PRU_ICSSG1	PRU_ICSSG1_PR1_EDC0_LATCH0_IN	TIMESYNC_INTRTR0_OUTL_12	TIMESYNC_INTRTR0	Level	Selectable time sync event 12
	PRU_ICSSG1_PR1_EDC0_LATCH1_IN	TIMESYNC_INTRTR0_OUTL_13	TIMESYNC_INTRTR0	Level	Selectable time sync event 13
	PRU_ICSSG1_PR1_EDC1_LATCH0_IN	TIMESYNC_INTRTR0_OUTL_14	TIMESYNC_INTRTR0	Level	Selectable time sync event 14
	PRU_ICSSG1_PR1_EDC1_LATCH1_IN	TIMESYNC_INTRTR0_OUTL_15	TIMESYNC_INTRTR0	Level	Selectable time sync event 15

Time Sync Event Outputs

Module Instance	Module Sync Output	Destination Sync Input	Destination	Type	Description
PRU_ICSSG0	PRU_ICSSG0_PR1_EDC0_SYNC0_OUT_0	TIMESYNC_INTRTR0_IN_25	TIMESYNC_INTRTR0	Pulse	IEP0 sync event 0
	PRU_ICSSG0_PR1_EDC0_SYNC1_OUT_0	TIMESYNC_INTRTR0_IN_26	TIMESYNC_INTRTR0	Pulse	IEP0 sync event 1
	PRU_ICSSG0_PR1_EDC1_SYNC0_OUT_0	TIMESYNC_INTRTR0_IN_27	TIMESYNC_INTRTR0	Pulse	IEP1 sync event 0
	PRU_ICSSG0_PR1_EDC1_SYNC1_OUT_0	TIMESYNC_INTRTR0_IN_28	TIMESYNC_INTRTR0	Pulse	IEP1 sync event 1
	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN0IN_PRG0_IEP0_EDC_LATCH_IN0_0	TIMESYNC_INTRTR0_IN_4	TIMESYNC_INTRTR0	Pulse	EDC0 Latch 0 input event (I/O pin)
	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN1IN_PRG0_IEP0_EDC_LATCH_IN1_0	TIMESYNC_INTRTR0_IN_5	TIMESYNC_INTRTR0	Pulse	EDC0 Latch 1 input event (I/O pin)
	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN0IN_PRG0_IEP1_EDC_LATCH_IN0_0	TIMESYNC_INTRTR0_IN_6	TIMESYNC_INTRTR0	Pulse	EDC1 Latch 0 input event (I/O pin)
	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN1IN_PRG0_IEP1_EDC_LATCH_IN1_0	TIMESYNC_INTRTR0_IN_7	TIMESYNC_INTRTR0	Pulse	EDC1 Latch 1 input event (I/O pin)
PRU_ICSSG1	PRU_ICSSG1_PR1_EDC0_SYNC0_OUT_0	TIMESYNC_INTRTR0_IN_29	TIMESYNC_INTRTR0	Pulse	IEP0 sync event 0
	PRU_ICSSG1_PR1_EDC0_SYNC1_OUT_0	TIMESYNC_INTRTR0_IN_30	TIMESYNC_INTRTR0	Pulse	IEP0 sync event 1
	PRU_ICSSG1_PR1_EDC1_SYNC0_OUT_0	TIMESYNC_INTRTR0_IN_31	TIMESYNC_INTRTR0	Pulse	IEP1 sync event 0
	PRU_ICSSG1_PR1_EDC1_SYNC1_OUT_0	TIMESYNC_INTRTR0_IN_32	TIMESYNC_INTRTR0	Pulse	IEP1 sync event 1
	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN0IN_PRG1_IEP0_EDC_LATCH_IN0_0	TIMESYNC_INTRTR0_IN_8	TIMESYNC_INTRTR0	Pulse	EDC0 Latch 0 input event (I/O pin)
	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN1IN_PRG1_IEP0_EDC_LATCH_IN1_0	TIMESYNC_INTRTR0_IN_9	TIMESYNC_INTRTR0	Pulse	EDC0 Latch 1 input event (I/O pin)
	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN0IN_PRG1_IEP1_EDC_LATCH_IN0_0	TIMESYNC_INTRTR0_IN_10	TIMESYNC_INTRTR0	Pulse	EDC1 Latch 0 input event (I/O pin)
	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN1IN_PRG1_IEP1_EDC_LATCH_IN1_0	TIMESYNC_INTRTR0_IN_11	TIMESYNC_INTRTR0	Pulse	EDC1 Latch 1 input event (I/O pin)

6.4.4 PRU_ICSSG Top Level Resources Functional Description

This section provides functional description of the device integrated PRU Subsystems modules.

The PRUn/RTU_PRUn (where n = 0 or 1) cores within each PRU_ICSSG have access to all resources on the SoC through the VBUSM Interface Controller port, and the external host processors can access the PRU_ICSSG resources through the VBUSP Interface Target port. The use of XFR2VBUS allows BroadSide 32Bytes of data transfer to/from SoC CBASS0 Interconnect at 256-bit bursts using the VBUSM Controller port. The 32-bit Internal CBASS Interconnect bus will be the primary interconnect between all components internal to the PRU_ICSSG. There are two equally symmetrical halves in each PRU_ICSSG known as SLICE0 and SLICE1. Each slice will share several resources while capable of working independently of each other. There are two sets of XFR2VBUS for each Slice. The XFR2VBUS hardware accelerator is shared between PRU0 and RTU_PRU0 for SLICE0 and the same configuration is valid for SLICE1. The TX_PRU0 and TX_PRU1 cores have also attached XFR2VBUS hardware accelerators. PRUs also has the ability to submit 32-bit bursts transitions, but this will require RAT configuration.

Each of the Slices contains one RAT (Region based Address Translation) module. For example, the RAT module in SLICE0 is shared between RTU_PRU0, PRU0 and TX_PRU0 cores and the same configuration is valid for SLICE1. The RAT module is used to translate 32-bit address of the PRU core to 48-bit physical address.

The PRU cores within the subsystems also have access to all resources on the SoC through the External CBASS0 Interconnect. A subsystem local Interrupt Controller — INTC handles system input events and posts events back to the device-level host CPUs.

Each slice has intergrated one Transmit PRUn core (TX_PRUn, where n = 0 or 1). This RISC cores are used to control the TX L2 FIFO if enabled.

Figure 6-23 shows an overview of the PRU_ICSSG Functional Block Diagram.

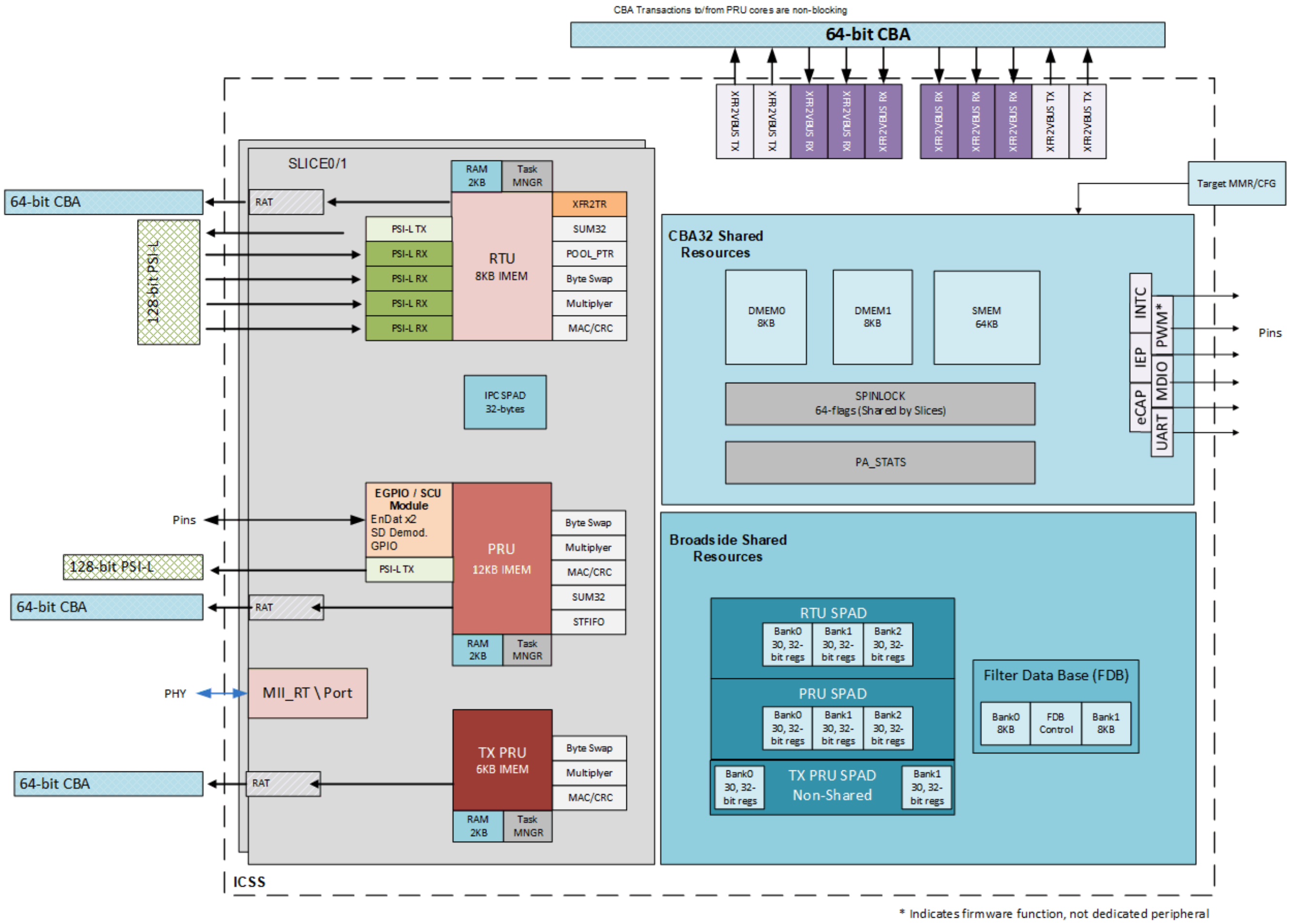

Figure 6-23. PRU_ICSSG Functional Block Diagram

Table 6-60 summarizes the mapping between hardware modules and PRU0/1, RTU_PRU0/1 or TX_PRU0/1 cores.

Table 6-60. Hardware Module Broadside ID Mapping

Hardware Module	Broadside ID	
MPY/MAC	00	6 copies: TX_PRU1/0 + RTU_PRU1/0 + PRU1/0
CRC16/32	01	6 copies: TX_PRU1/0 + RTU_PRU1/0 + PRU1/0 Note: TX_PRU1/0 do not have CRC FIFO
STITCH_FIFO64	08	2 copies: PRU1/0
QUEUE_PTR	09	2 copies: RTU_PRU1/0
SUM32	RTU_PRU MAP: 38 for SUM32 + RAM 39 for SUM32 ONLY PRU MAP: 49 for SUM32 + RAM 47 for SUM32 ONLY 02 for results	4 copies: 1 for each RTU_PRU1/0 1 for each PRU1/0
SPAD Bank0	10	1 copy: shared between PRU1/0 1 copy: shared between RTU_PRU1/0 2 copies: 1 for each TX_PRU1/0

Table 6-60. Hardware Module Broadside ID Mapping (continued)

Hardware Module	Broadside ID	
SPAD Bank1	11	1 copy: shared between PRU1/0 1 copy: shared between RTU_PRU1/0
SPAD Bank2	12	1 copy: shared between PRU1/0 1 copy: shared between RTU_PRU1/0
IPC SPAD	15	2 copies: 1 per slice
RX L2	20/21	2 copies: PRU1/0
RX Classifier	22	2 copies: 1 per slice (RTU_PRU0/PRU0 + RTU_PRU1/PRU1)
RX first 24 Bytes and 16 Bytes of TSN/pre	35	2 copies: RTU_PRU1/0
RX last 12 Bytes	15 RTU_PRU1/0 15 PRU1/0	4 copies: RTU_PRU1/0 PRU1/0 Mapped to upper PRU_RTU_SPAD IPC
FDB 16KB: 2 Banks of 8KB	30-35	1 copy: shared between PRU1/0 and RTU_PRU1/0
FDB results	32/33/34	1 copy: shared between RTU_PRU1/0 and PRU1/0
BS RAM	BS RAM only mode: 30 BS RAM + SUM32 snoop mode: 38	2 copies: RTU_PRU1/0
BS RAM	BS RAM only mode: 48 BS RAM + SUM32 snoop mode: 49	2 copies: PRU1/0 2 copies: TX_PRU1/0
TX L2	40	2 copies: PRU1/0 OR attached/own to TX_PRU1/0 (if register set to enable)
XFR2PSI	0x50/0x51/0x52/0x53	4 copies: RTU_PRU1/0 + PRU1/0
XFR2PSI Share	0x58 RTU_PRU1/0 Only 0x59 RTU_PRU1/0 Only	2 copies of special XFR2PSI which is attached to PRU1/0 The RTU_PRU1/0 can access it using 0x58/0x59 if MII_G_RT_ICSS_G_CFG[9] RTU_PRU_PSI_SHARE_EN bit is set
XFR2VBUSP	0x60 for RD_ID0 0x61 for RD_ID1 0x62 for WD_ID0 0x63 for WD_ID1 0x64 for TX_PRU1/0 RD	2 copies shared of RX per SLICE 2 copies shared of TX per SLICE 1 copy dedicated RX for TX_PRU only per SLICE
XFR2SHORT_DMA	0x70/71/72	2 copies: RTU_PRU1/0
XFR2SPIN	0x90	1 copy per PRU_ICSSG system
BSWAP	0xA0 for Byte Order Swap 0xA1 for 4_8 mode 0xA2 for 4_16 mode	6 copies: TX_PRU1/0 + RTU_PRU1/0 + PRU1/0
QUEUE_EMPTY	0xF0	Share XIN only all 6 PRU cores

6.4.4.1 PRU_ICSSG Reset Management

The device supports warm reset isolation (Hard/Soft Reset, Watchdog Reset) on PRU_ICSSG0 and PRU_ICSSG1.

6.4.4.2 PRU_ICSSG Power and Clock Management

The PRU_ICSSG supports two levels of clock gating. First level gates all clocks inside the PRU_ICSSG when requested by the PSC (Power Sleep Controller). The second level allows user software to enable/disable clocks in the clock gating register ICSSG_CGR_REG to some internal modules, as follows:

- IEP
- ECAP0
- UART0
- INTC

The appropriate configuration registers block controls its local module set inside PRU_ICSSG.

Note

PRU_ICSSG supports different clock speeds for CORE_CLK and IEP_CLK. Please refer to *PRU_ICSSG Integration*, for details.

6.4.4.2.1 PRU_ICSSG CORE Clock Generation

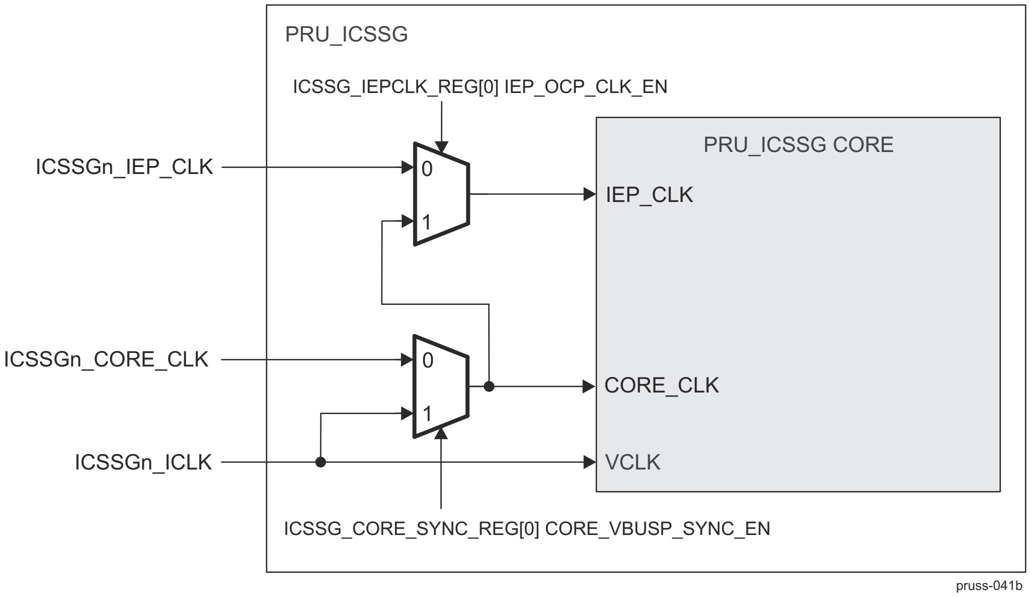

Figure 6-24. PRU_ICSSG CORE Clock Diagram

The CORE block uses two multiplexers to allow software to select one of three source clocks (ICSSGn_CORE_CLK, ICSSGn_ICLK or ICSSGn_IEP_CLK) for the final clock source of the CORE block. The user needs to configure ICSSG_CORE_SYNC_REG[0] CORE_VBUSP_SYNC_EN bit and ICSSG_IEPCLK_REG[0] IEP_OCP_CLK_EN bit to 1 if CORE_CLK and IEP_CLK respectively needs to be synchronous to ICLK (250 MHz).

6.4.4.2.2 PRU_ICSSG Idle State

The below lists the clock management settings applicable at PRU_ICSSG subsystem level (first level of local power management).

A transition from an ACTIVE/Normal state to an IDLE state is performed as per the sequence:

1. The host processor requests that the PRU firmware goes into IDLE state and waits for acknowledgement.
2. The host issues Clock Stop Request for each module in ICSSG_CGR_REG register with gateable clocks defined at second power management level (see Section 6.4.4.2)

3. The PRU_ICSSG acknowledges IDLE Request and send Clock Stop Acknowledge to the host processor.
4. The PSC can de-assert PWR_CLK_EN
5. The main clocks can get turned off

A transition from an IDLE state to an ACTIVE/ Normal state is performed as per the sequence:

1. Turn on the main external clocks
2. The PSC can assert PWR_CLK_EN
3. The host will need to de-assert Clock Stop Request for each module, defined in ICSSG_CGR_REG register,
4. The PRU_ICSSG firmware need to de-assert Clock Stop Acknowledge for each module defined in ICSSG_CGR_REG register and then wait for the Clock Stop Acknowledge de-assert
5. The PRU_ICSSG firmware will de-assert Clock Stop Acknowledge

6.4.4.2.3 PRU_ICSSG Protect

Write protect block allows software to enable safety protection to prevent corruption of key configuration and debug registers and the Instruction memories (IRAM's) of all six PRU cores (PRU0/PRU1, RTU_PRU0/RTU_PRU1 and TX_PRU0/TX_PRU1). Write protection is also supported for Data RAM0 and Data RAM1.

This is achived by blocking the byte enables during a write transaction if enabled. When enabled, it will prevent any unwanted write transaction to these elements. To Enable/Disable this feature, software will first need to unlock the write access to this block through the PROT_UNLOCK_KEY register then configure the protection through PROT_CFG register and relock.

6.4.4.2.4 Module Clock Configurations at PRU_ICSSG Top Level

IEP functional clock source selection: The clock source selection to the IEP module is done in register CTRLMMR_ICSSGn_CLKSEL[19-16] IEP_CLKSEL (where n = 0 or 1) in the CTRL_MMR0 location. For more information on these PRU_ICSSG level input clocks, refer to the *PRU_ICSSG Integration*.

Enhanced GPIO clock divider settings: In certain sample/shift clock settings of the PRU0 and PRU1 EGPIOs (when enabled in serial mode) two cascaded fractional dividers are done in the PR1_ICSSG_CFG top level configuration registers ICSSG_GPCFG0_REG and ICSSG_GPCFG1_REG. In addition, EGPIO clock active edge selection control can be exerted via the bit PRU0_GPI_CLK_MODE for PRU0 EGPIO and PRU1_GPI_CLK_MODE for the PRU1 EGPIO.

- For the serial PRU0's EGPOs:
  - ICSSG_GPCFG0_REG[24-20] PRU0_GPO_DIV1
  - ICSSG_GPCFG0_REG[19-15] PRU0_GPO_DIV0
- For the serial PRU0's EGPIs:
  - ICSSG_GPCFG0_REG[12-8] PRU0_GPI_DIV1
  - ICSSG_GPCFG0_REG[7-3] PRU0_GPI_DIV0
- For the serial PRU1's EGPOs:
  - ICSSG_GPCFG1_REG[24-20] PRU1_GPO_DIV1
  - ICSSG_GPCFG1_REG[19-15] PRU1_GPO_DIV0
- For the serial PRU1's EGPIs:
  - ICSSG_GPCFG1_REG[12-8] PRU1_GPI_DIV1
  - ICSSG_GPCFG1_REG[7-3] PRU1_GPI_DIV0

6.4.4.3 Other PRU_ICSSG Module Functional Registers at Subsystem Level

Enhanced GPIO. The other functional mode setting for PRUs EGPIOs at PRU_ICSSG top registers level are:

- ICSSG_GPCFG0_REG / ICSSG_GPCFG1_REG[14] PRU0_GPO_MODE (PRU0 or PRU1) — to select between direct or serial EGPO output mode of operation.
- ICSSG_GPCFG0_REG / ICSSG_GPCFG1_REG[25] PRU0_GPO_SH_SEL (PRU0 or PRU1) — to select between the EGPO shadow registers 0 and 1 used for output shifting. For more details, refer to the Section 6.4.5.2.2.3.4 , *Enhanced General-Purpose Module Outputs (R30)*.

- ICSSG_GPCFG0_REG / ICSSG_GPCFG1_REG[1-0] PRU0_GPI_MODE (PRU0 or PRU1) — selects the EGPI input mode of operation (selects between "direct input", "parallel capture", "28-bit shift" or "MII_RT" modes).
- ICSSG_GPCFG0_REG / ICSSG_GPCFG1_REG[13] PRU0_GPI_SB (PRU0 or PRU1) — start bit event status for 28-bit EGPI input shift mode. For more details, refer to the Section 6.4.5.2.2.3 , *Enhanced General-Purpose Module Inputs (R31)*.

PRUs scratchpad (SPAD) memory priority and configuration related bits are located in the ICSSG_SPP_REG register.

6.4.4.4 PRU_ICSSG Memory Maps

The PRU_ICSSG comprises various distinct addressable regions that are mapped to both a local and global memory map. The local memory maps are maps with respect to the PRU point of view. The global memory maps are maps with respect to the Host point of view, but can also be accessed by the PRU_ICSSG. Each PRU_ICSSG can also access the memories within the other PRU_ICSSG subsystem without going through an external port, thanks to PRU_ICSSG VBUSP expansion port.

6.4.4.4.1 PRU_ICSSG Local Memory Map

The PRU_ICSSG memory map is documented in Table 6-61 (Instruction Space) and in Table 6-62 (Data Space). Note that these two memory maps are implemented inside the PRU_ICSSG and are local to the components of the PRU_ICSSG.

6.4.4.4.1.1 PRU_ICSSG Local Instruction Memory Map

Each PRU (PRU0 and PRU1) has a dedicated 12KB of Instruction Memory (12KB for PRU_ICSSG0 and 12KB for PRU_ICSSG1) which needs to be initialized by an external to PRU_ICSSG Host processor before a PRU core executes any instructions.

Each RTU_PRU (Auxiliary PRU Cores: RTU_PRU0 and RTU_PRU1) has also a dedicated 8KB of Instruction Memory (8KB for PRU_ICSSG0 and 8KB for PRU_ICSSG1).

Each TX_PRU (Transmit PRU Cores: TX_PRU0 and TX_PRU1) has also a dedicated 6KB of Instruction Memory (6KB for PRU_ICSSG0 and 6KB for PRU_ICSSG1).

> **CAUTION**
>
> The PRU_ICSSG0 PRU0/1_IRAM regions are ONLY accessible from controllers, external to the PRU_ICSSG (like Arm) when the PRU0/PRU1 is NOT running. The access is via PRU_ICSSG target port on the device CBASS0 interconnect.

Table 6-61. PRU_ICSSG Local Instruction Memory Map

Start Address	PRU0/RTU_PRU0 TX_PRU0	PRU1/RTU_PRU1/TX_PRU1
0000 0000h	12 KB IRAM/8 KB IRAM/6 KB IRAM	12 KB IRAM/8 KB IRAM/6 KB IRAM

6.4.4.4.1.2 PRU_ICSSG Local Data Memory Map

The local data memory map in Table 6-62 allows each PRU core to access the PRU_ICSSG addressable regions (both its own subsystem and the other subsystem) and the external host's memory map.

Table 6-62. PRU_ICSSG Local Data Memory Map

Start Address	PRU0/ RTU_PRU0/ TX_PRU0	PRU1/ RTU_PRU1/ TX_PRU1
0000 0000h	PRU_ICSSG1 Data 8 KB RAM0	PRU_ICSSG1 Data 8 KB RAM1
0000 2000h	PRU_ICSSG1 Data 8 KB RAM1(1)	PRU_ICSSG1 Data 8 KB RAM0(1)
0000 4000h	Reserved	Reserved
0000 6000h	Reserved	Reserved
0000 8000h	RAT_SLICE0	RAT_SLICE0

Table 6-62. PRU_ICSSG Local Data Memory Map (continued)

Start Address	PRU0/ RTU_PRU0/ TX_PRU0	PRU1/ RTU_PRU1/ TX_PRU1
0000 9000h	RAT_SLICE1	RAT_SLICE1
0001 0000h	Data 64 KB RAM2 (Shared RAM)	Data 64 KB RAM2 (Shared RAM)
0002 0000h	PRU_ICSSG1 INTC	PRU_ICSSG1 INTC
0002 2000h	PRU0 Control	PRU0 Control
0002 3000h	RTU_PRU0 Control	RTU_PRU0 Control
0002 3400h	Reserved	Reserved
0002 3800h	RTU_PRU1 Control	RTU_PRU1 Control
0002 3C00h	Reserved	Reserved
0002 4000h	PRU1 Control	PRU1 Control
0002 4400h	Reserved	Reserved
0002 4800h	Reserved	Reserved
0002 4C00h	PROTECT	PROTECT
0002 5000h	TX_PRU0 Control	TX_PRU0 Control
0002 5800h	TX_PRU1 Control	TX_PRU1 Control
0002 6000h	PRU_ICSSG1 CFG	PRU_ICSSG1 CFG
0002 7000h	PA_STATS_QRAM	PA_STATS_QRAM
0002 8000h	PRU_ICSSG1 UART0	PRU_ICSSG1 UART0
0002 A000h	TM_CFG_PRU0 (Task Manager)	TM_CFG_PRU0 (Task Manager)
0002 A100h	TM_CFG_RTU0 (Task Manager)	TM_CFG_RTU0 (Task Manager)
0002 A200h	TM_CFG_PRU1 (Task Manager)	TM_CFG_PRU1 (Task Manager)
0002 A300h	TM_CFG_RTU1 (Task Manager)	TM_CFG_RTU1 (Task Manager)
0002 A400h	TM_CFG_TX_PRU0 (Task Manager)	TM_CFG_TX_PRU0 (Task Manager)
0002 A500h	TM_CFG_TX_PRU1 (Task Manager)	TM_CFG_TX_PRU1 (Task Manager)
0002 C000h	PA_STATS_CRAM	PA_STATS_CRAM
0002 E000h	IEP0	IEP0
0002 F000h	IEP1	IEP1
0003 0000h	ECAP0	ECAP0
0003 2000h	MII_RT_CFG	MII_RT_CFG
0003 2100h	SGMII0_CFG	SGMII0_CFG
0003 2200h	SGMII1_CFG	SGMII1_CFG
0003 2400h	MII_MDIO	MII_MDIO
0003 3000h	ICSS_G_CFG	ICSS_G_CFG
0003 4000h	Reserved	Reserved
0003 7000h	Reserved	Reserved
0003 8000h	Reserved	Reserved
0003 B000h	Reserved	Reserved
0003 C000h	PA_STATS_CFG	PA_STATS_CFG
0004 0000h	Reserved	Reserved
0008 0000h	Reserved	Reserved

(1) Direct access from PRU0 to Data RAM 1 and PRU1 to Data RAM 0.

6.4.4.4.2 PRU_ICSSG Global Memory Map

The global view of the PRU_ICSSG internal memories and control ports is shown in Table 6-63. The offset addresses of each region are implemented inside the PRU_ICSSG but the global device memory mapping places the PRU_ICSSG target port in the address range shown in the external PRU_ICSSG Host top-level memory map.

The global memory map is with respect to the Host point of view (that is, device Arm), but it can also be accessed by the PRU_ICSSG itself. Note that PRU0 and PRU1 can use either the local or global addresses to access their internal memories, but using the local addresses provides access time several cycles faster than using the global addresses. This is because when accessing via the global address the access has to be routed through the CBASS0 switch fabric outside PRU_ICSSG and back in through the PRU_ICSSG target port.

Each of the PRU cores can access the rest of the device memory (including memory mapped peripheral and configuration registers) using the global memory space addresses.

Table 6-63. PRU_ICSSG Global Memory Map

Offset Address	PRU_ICSSG Target
0000 0000h	Data 8 KB RAM0
0000 2000h	Data 8 KB RAM1
0000 4000h	RTU_PRU0 8 KB IRAM
0000 6000h	RTU_PRU1 8 KB IRAM
0000 8000h	RAT_SLICE0
0000 9000h	RAT_SLICE1
0000 A000h	TX_PRU0 6 KB IRAM
0000 C000h	TX_PRU1 6 KB IRAM
0001 0000h	Data 64 KB RAM2 (shared)
0002 0000h	PRU_ICSSG INTC
0002 2000h	PRU0 Control
0002 2400h	PRU0 Debug
0002 3000h	RTU_PRU0 Control
0002 3400h	RTU_PRU0 Debug
0002 3800h	RTU_PRU1 Control
0002 3C00h	RTU_PRU1 Debug
0002 4000h	PRU1 Control
0002 4400h	PRU1 Debug
0002 4C00h	PROTECT
0002 5000h	TX_PRU0 Control
0002 5400h	TX_PRU0 Debug
0002 5800h	TX_PRU1 Control
0002 5C00h	TX_PRU1 Debug
0002 6000h	PRU_ICSSG CFG
0002 7000h	PA_STATS_QRAM
0002 8000h	PRU_ICSSG UART0
0002 A000h	TM_CFG_PRU0 (Task Manager)
0002 A100h	TM_CFG_RTU0 (Task Manager)
0002 A200h	TM_CFG_PRU1 (Task Manager)
0002 A300h	TM_CFG_RTU1 (Task Manager)
0002 A400h	TM_CFG_TX_PRU0 (Task Manager)
0002 A500h	TM_CFG_TX_PRU1 (Task Manager)
0002 C000h	PA_STATS_CRAM
0002 E000h	IEP0
0002 F000h	IEP1

Table 6-63. PRU_ICSSG Global Memory Map (continued)

Offset Address	PRU_ICSSG Target
0003 0000h	ECAP0
0003 2000h	MII_RT_CFG
0003 2100h	SGMII0_CFG
0003 2200h	SGMII1_CFG
0003 2400h	MII_MDIO
0003 3000h	MII_G_RT_CFG
0003 4000h	PRU0 12 KB IRAM
0003 8000h	PRU1 12 KB IRAM
0003 C000h	PA_STATS_CFG
0004 0000h	Reserved

6.4.5 PRU_ICSSG PRU Cores

This section describes the functionality of the two Programmable Real-time Unit (PRU) processors (PRU0 and PRU1), RTU_PRU0/ RTU_PRU1 and TX_PRU0/ TX_PRU1 integrated in each of the device PRU_ICSSG.

6.4.5.1 PRU Cores Overview

The PRU is a processor optimized for performing embedded tasks that require manipulation of packed memory mapped data structures, handling of system events that have tight real-time constraints and interfacing with systems external to the SoC. The PRU is both very small and very efficient at handling such tasks.

The major attributes of the PRU are shown in Table 6-64.

Table 6-64. PRU Features

Attribute	Value
IO Architecture	Load/Store
Data Flow Architecture	Register to Register
Core Level Bus Architecture	
Type	4-Bus Harvard (1 Instruction, 3 Data)
Instruction I/F	32-Bit Modified VBUSP Controller
Memory I/F 0	32-Bit VBUSP Controller
Memory I/F 1	32-Bit VBUSP Controller
Execution Model	
Issue Type	Scalar
Pipelining	None (Purposefully)
Ordering	In Order
ALU Type	Unsigned Integer
Registers	
General Purpose (GP)	30 (R1 – R30)
External Status	0 (R31)
GP/Indexing	0 (R0)
Addressability in Instruction	Bit, Byte (8-bit), Half-word (16-bit), Word (32-bit), Pointer
Addressing Modes	
Load Immediate	16-bit Immediate
Load/Store – Memory	Register Base + Register Offset Register Base + 8-bit Immediate Offset Register Base with auto increment/decrement Constant Table Base + Register Offset Constant Table Base + 8-bit Immediate Offset Constant Table Base with auto increment/ decrement
Data Path Width	32-bit
Instruction Width	32-bit
Accessibility to Internal PRU Structures	Provides 32-bit VBUSP target with three regions: • Instruction RAM • Control/Status registers • Debug access to internal registers (R0-R31) and constant table

The processor is based on a four-bus architecture which allows instructions to be fetched and executed concurrently with data transfers. In addition, an input is provided in order to allow external status information to be reflected in the internal processor status register. Figure 6-25 shows a block diagram of the processing element and the associated instruction RAM/ROM that contains the code that is to be executed.

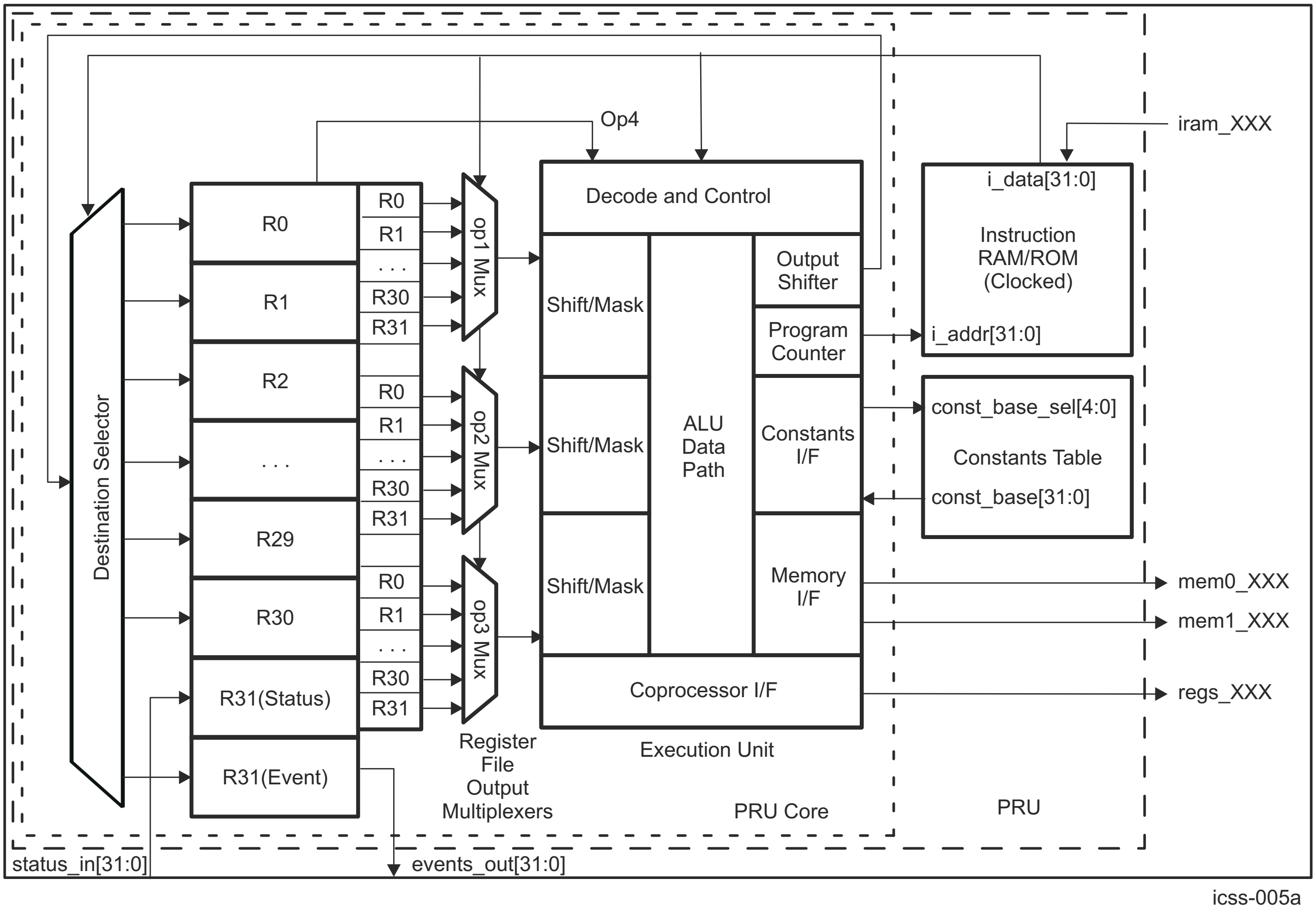

Figure 6-25. PRU Block Diagram

6.4.5.2 PRU Cores Functional Description

This section describes the PRU cores supported functionality by describing the constant table, module interface and enhanced GPIOs.

6.4.5.2.1 PRUs Constant Table

The PRU Constants Table is a structure of hard-coded memory addresses for commonly used peripherals and memories. The constants table is used for more efficiently load/store data to these commonly accessed addresses by:

- Eliminating the PRU instruction that pre-loads a hard-coded address into the internal register file.
- Maximizing the usage of the PRU register file for embedded processing applications by moving many of the commonly used constant or deterministically calculated base addresses from the internal register file to an external table.

Table 6-65. PRU0/1 Constant Table

Entry No.	Region Pointed To	Value [31:0]
0	PRU_ICSSG INTC (local)	0002_0000h
1	PRU_ICSSG IEP1 (local)	0002_F000h
2	PRU_ICSSG IEP1_0x100 (local)	0002_F100h
3	PRU_ICSSG ECAP0 (local)	0003_0000h

Table 6-65. PRU0/1 Constant Table (continued)

Entry No.	Region Pointed To	Value [31:0]
4	PRU_ICSSG CFG (local)	0002_6000h
5	PRU_ICSSG CFG_0x100 (local)	0002_6100h
6	PRU_ICSSG INTC_0x200 (local)	0002_0200h
7	PRU_ICSSG UART0 (local)	0002_8000h
8	PRU_ICSSG IEP0_0x100 (local)	0002_E100h
9	PRU_ICSSG0 CFG (local)	0003_3000h
10	TM_CFG_PRU0 (Local Task Manager) TM_CFG_RTU0 (Local Task Manager) TM_CFG_PRU1 (Local Task Manager) TM_CFG_RTU1 (Local Task Manager)	0002_A000h PRU0 0002_A100h RTU_PRU0 0002_A200h PRU1 0002_A300h RTU_PRU1
11	PRU_ICSSG PRU0 Control (local) PRU_ICSSG RTU_PRU0 Control (local) PRU_ICSSG RTU_PRU1 Control (local) PRU_ICSSG PRU1 Control (local)	0002_2000h PRU0 0002_3000h RTU_PRU0 0002_3800h RTU_PRU1 0002_4000h PRU1
12	PRU_ICSSG PA_STATS_QRAM (local)	0002 7000h
13	PRU_ICSSG PA_STATS_CRAM (local)	0002 C000h
14	Reserved	0002 4800h
15	Reserved	6000_0000h
16	Reserved	7000_0000h
17	Reserved	8000_0000h
18	Reserved	9000_0000h
19	Reserved	A000_0000h
20	Reserved	B000_0000h
21	MDIO (local)	0003_2400h
22	RAT SLICE0 (local) RAT SLICE1 (local)	0000_8000h PRU0/RTU_PRU0 0000_9000h PRU1/RTU_PRU1
23	Reserved	C000_0000h
24	PRU_ICSSG PRU0/PRU1 Data RAM (local)	0000_0n00h, n = c24_blk_index[3:0]
25	PRU_ICSSG PRU1/PRU0 Data RAM (local)	0000_2n00h, n = c25_blk_index[3:0]
26	PRU_ICSSG IEP (local)	0002_En00h, n = c26_blk_index[3:0]
27	PRU_ICSSG MII_RT/SGMII0_CFG/SGMII1_CFG (local)	0003_2n00h, n = c27_blk_index[3:0]
28	PRU_ICSSG Shared RAM (local)	00nn_nn00h, nnnn = c28_pointer[15:0]
29	Reserved	0Dnn_nn00h, nnnn = c29_pointer[15:0]
30	Reserved	0Enn_nn00h, nnnn = c30_pointer[15:0]
31	Reserved	0Fnn_nn00h, nnnn = c31_pointer[15:0]

Note

The addresses in constants entries 24–31 are partially programmable. Their programmable bit field (for example, c24_blk_index[3:0]) is programmable through the PRU CTRL register space. As a general rule, the PRU should configure this field before using the partially programmable constant entries.

6.4.5.2.2 PRU Module Interface

The PRU module interface consists of the PRU internal registers 30 and 31 (R30 and R31). Figure 6-26 shows the PRU module interface and the functionality of R30 and R31. The register R31 serves as an interface with the dedicated PRU general purpose input (GPI) pins and PRU_ICSSG INTC. Reading R31 returns status information from the GPI pins and PRU_ICSSG INTC via the PRU Real Time Status Interface. Writing to R31 generates PRU system events via the PRU Event Interface. The register R30 serves as an interface with the dedicated PRU general purpose output (GPO) pins.

Note

The below sections cover different functional modes of the PRUn cores, (where n=0,1), enhanced GPIO (EGPIO) interface. The register bits which control EGPIO functionalities are part of the (PRU_ICSSG CFG) space. For descriptions of these EGPIO register bitfield controls, refer to the Section 6.4.4.3 .

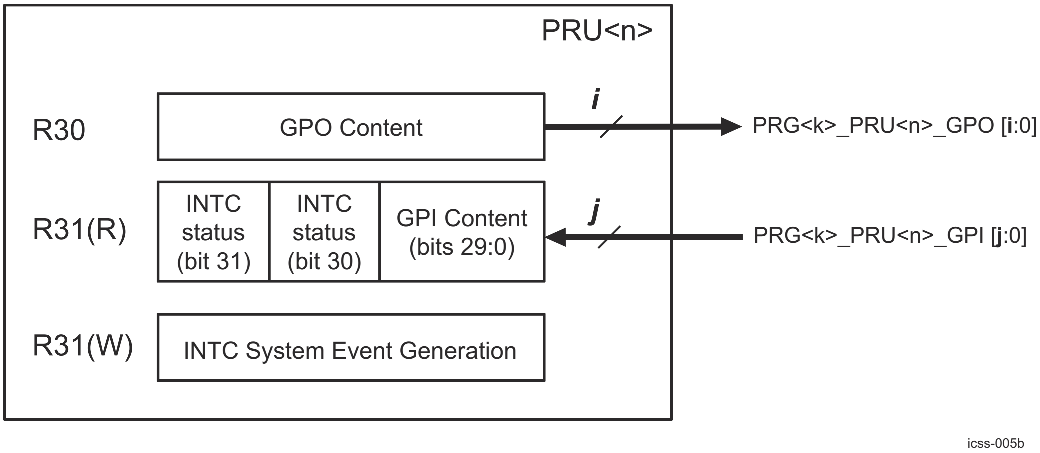

Figure 6-26. PRU Module Interface

6.4.5.2.2.1 Real-Time Status Interface Mapping (R31): Interrupt Events Input

The PRU Real Time Status Interface directly feeds information into register 31 (R31) of the PRU's internal register file. The firmware on the PRU uses the status information to make decisions during execution. The status interface is comprised of signals from different modules inside of the PRU_ICSSG which require some level of interaction with the PRU. More details on the Host interrupts imported into bit 30 and 31 of register R31 of both the PRUs is provided in the *PRU_ICSSG Local Interrupt Controller*.

Table 6-66. Real-Time Status Interface Mapping (R31) Field Descriptions

Bit	Field	Description
31	pru_intr_in[1]	PRU Host Interrupt 1 from local PRU_ICSSG INTC
30	pru_intr_in[0]	PRU Host Interrupt 0 from local PRU_ICSSG INTC
29-0	pru<n>_r31_status[29:0]	Status inputs from primary input via Enhanced GPI port

6.4.5.2.2.2 Event Interface Mapping (R31): PRU System Events

This PRU Event Interface directly feeds pulsed event information out of the PRU's internal ALU. These events are exported out of the PRU_ICSSG and need to be connected to the system interrupt controller at the SoC level. The event interface can be used by the firmware to create software interrupts from the PRU to the Host processor.

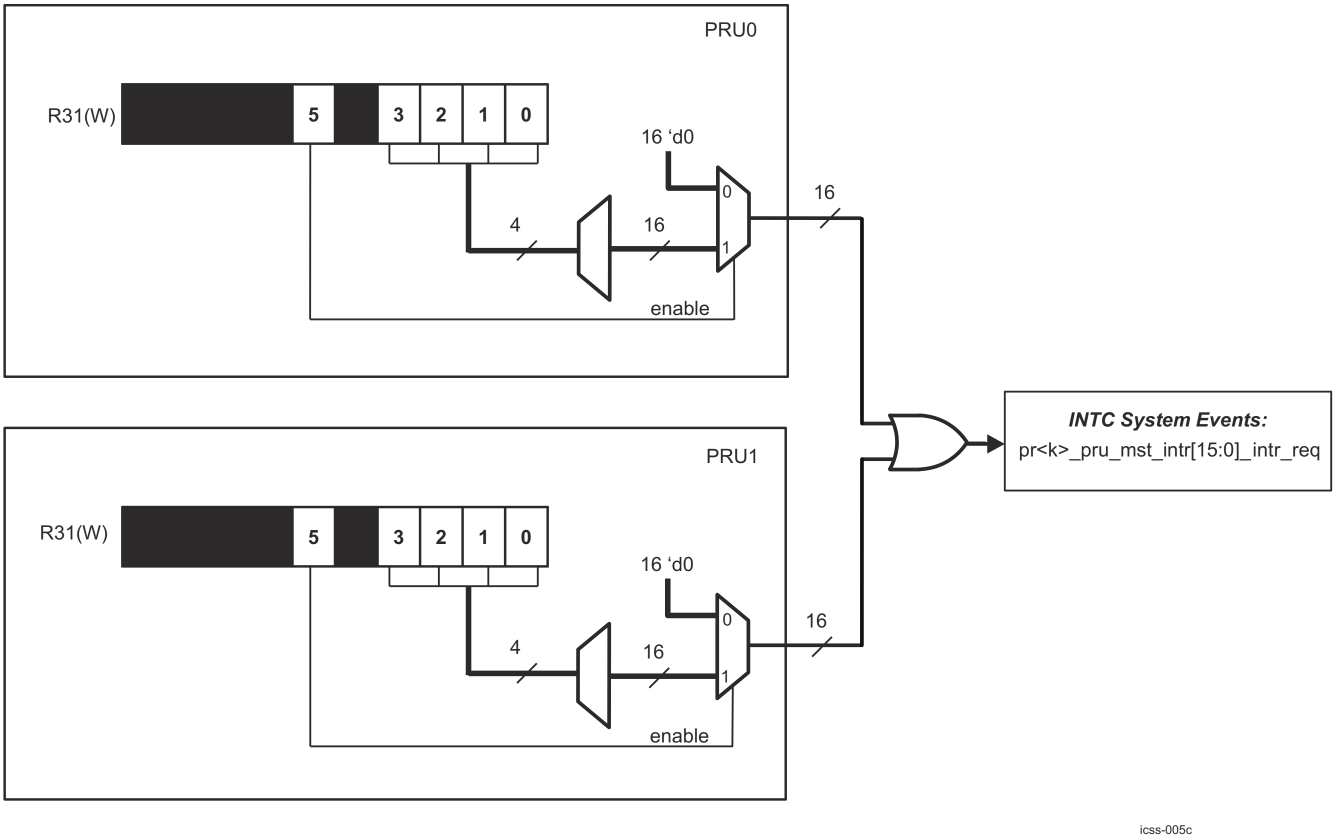

Figure 6-27. Event Interface Mapping (R31)

Table 6-67. Event Interface Mapping (R31) Field Descriptions

Bit	Field	Description
31-6	Reserved	
5	pru<n>_r31_vec_valid	Valid strobe for vector output
4	Reserved	
3-0	pru<n>_r31_vec[3:0]	Vector output

Simultaneously writing a '1' to pru<n>_r31_vec_valid (R31 bit 5) and a channel number from 0 to 15 to pru<n>_r31_vec[3:0] (R31 bits 3-0) creates a pulse on the output of the corresponding pr<k>_pru_mst_intr[x]_intr_req INTC system event. For example, writing '100000' will generate a pulse on prk_pru_mst_intr[0]_intr_req, writing '100001' will generate a pulse on prk_pru_mst_intr[1]_intr_req, and so on to where writing '101111' will generate a pulse on prk_pru_mst_intr[15]_intr_req and writing '0xxxxx' will not generate any system event pulses. The output values from both PRU cores in a subsystem are ORed together.

The output channels 0-15 are connected to the INTC system events 16-31, respectively. This allows the PRU to assert one of the system events 16-31 by writing to its own R31 register. The system event is used to either post a completion event to one of the host CPUs (Arm) or to signal the other PRU. The host to be signaled is determined by the system interrupt to interrupt channel mapping (programmable). The 16 events are named as prk_pru_mst_intr<15:0>_intr_req. See the *PRU_ICSSG Interrupt Requests Mapping,* in the section, *PRU_ICSSG Local Interrupt Controller*, for more details.

6.4.5.2.2.3 General-Purpose Inputs (R31): Enhanced PRU GP Module

The PRU_ICSSG implements an enhanced General Purpose Input/Output (GPIO) module with SCU that supports the following general-purpose input modes: direct input, 16-bit parallel capture, 28-bit serial shift in, and MII_RT. Register R31 serves as an interface with the general-purpose inputs. Table 6-68 describes the input modes in detail.

Note

Each PRU core can only be configured for one GPI mode at a time. Each mode uses the same R31 signals and internal register bits for different purposes. A summary is found in Table 6-69.

Note

The ICSSG_GPCFG0_REG register, bitfield [29-26] PR1_PRU0_GP_MUX_SEL (PRU0 or PRU1) in the PRU_ICSSG CFG register space needs to be set to 0h for GP mode. For a given PRU core, the following IO modes are mutually exclusive: GP mode, Sigma Delta mode, and 3 channel Peripheral I/F mode.

Table 6-68. PRU R31 (GPI) Modes

Mode	Function	Configuration
Direct input	GPI[19:0] feeds directly into the PRU R31	Default state
16-bit parallel capture	DATAIN[0:15] is captured by the posedge or negedge of CLOCKIN	• Enabled by ICSSG_GPCFG0_REG register (PRU0 or PRU1) • CLOCKIN edge selected by ICSSG_GPCFG0_REG register
28-bit shift in	DATAIN is sampled and shifted into a 28-bit shift register. • Shift Counter (Cnt_16) feature is mapped to pru<n>_r31_status[28]. • SB (Start Bit detection) feature is mapped to pru<n>_r31_status[29]	• Enabled and disabled by ICSSG_GPECFG0_REG register (PRU0 or PRU1) • Cnt_16 is self clearing and is connected to the PRU INTC • Start Bit (SB) is cleared by ICSSG_GPECFG0_REG register • Start Bit value (0h or 1h) selected by ICSSG_GPECFG0_REG register
MII_RT	mii_rt_r31_status [29:0] internally driven by the MII_RT module	Enabled by ICSSG_GPCFG0_REG[1-0] PRU0_GPI_MODE register (value: 3h), where n = 0 or 1

Table 6-69. PRU GPI Signals and Configurations

Pad Names at Device Level[(1)]	GPI Modes		
	Direct input	Parallel Capture	28-Bit Shift in
PRG<k>_PRU<n>_GPI0	GPI0	DATAIN0	DATAIN
PRG<k>_PRU<n>_GPI1	GPI1	DATAIN1	
PRG<k>_PRU<n>_GPI2	GPI2	DATAIN2	
PRG<k>_PRU<n>_GPI3	GPI3	DATAIN3	
PRG<k>_PRU<n>_GPI4	GPI4	DATAIN4	
PRG<k>_PRU<n>_GPI5	GPI5	DATAIN5	
PRG<k>_PRU<n>_GPI6	GPI6	DATAIN6	
PRG<k>_PRU<n>_GPI7	GPI7	DATAIN7	
PRG<k>_PRU<n>_GPI8	GPI8	DATAIN8	
PRG<k>_PRU<n>_GPI9	GPI9	DATAIN9	
PRG<k>_PRU<n>_GPI10	GPI10	DATAIN10	
PRG<k>_PRU<n>_GPI11	GPI11	DATAIN11	
PRG<k>_PRU<n>_GPI12	GPI12	DATAIN12	

Table 6-69. PRU GPI Signals and Configurations (continued)

Pad Names at Device Level[1]	GPI Modes		
	Direct input	Parallel Capture	28-Bit Shift in
PRG<k>_PRU<n>_GPI13	GPI13	DATAIN13	
PRG<k>_PRU<n>_GPI14	GPI14	DATAIN14	
PRG<k>_PRU<n>_GPI15	GPI15	DATAIN15	
PRG<k>_PRU<n>_GPI16	GPI16	CLOCKIN	
PRG<k>_PRU<n>_GPI17	GPI17		
PRG<k>_PRU<n>_GPI18	GPI18		
PRG<k>_PRU<n>_GPI19	GPI19		

(1) These pins are also used for Sigma Delta or Peripheral I/F mode.

6.4.5.2.2.3.1 PRU EGPIs Direct Input

The pru<n>_r31_status[0:19] bits of the internal PRU register file are mapped to device-level, general purpose input pins (PRU0_GPI[0:19]). In GPI Direct Input mode, PRU0_GPI[0:19] feeds directly to pru<n>_r31_status[0:19].

Each PRU of the PRU_ICSSG has a separate mapping to device input signals - PRGn_PRU0_GPI[19:0] for the PRU0 core and PRGn_PRU1_GPI[19:0] for the PRU1 core. There are 80 general purpose inputs in total. For more details, refer also to the *PRU_ICSSG Environment*. See the device's system reference guide or datasheet for device specific pin mapping.

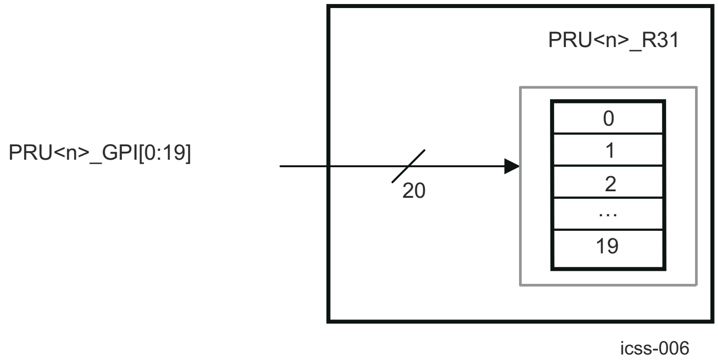

Figure 6-28. PRU R31 (EGPI) Direct Input Mode Block Diagram

6.4.5.2.2.3.2 PRU EGPIs 16-Bit Parallel Capture

The pru<n>_r31_status[0:15] and pru<n>_r31_status[16] bits of the internal PRU register file mapped to device-level, general purpose input pins (PRU0_DATAIN [0:15] and PRU0_CLOCKIN, respectively). PRU0_CLOCKIN is designated for an external strobe clock, and is used to capture PRU0_DATAIN [0:15].

The PRU<n>_DATAIN can be captured either by the positive or the negative edge of PRU<n>_CLOCK, programmable through the PRU_ICSSG CFG register space. If the clocking is configured through the PRU_ICSSG CFG register to be positive, then it will equal PRU<n>_CLOCK; however, if the clocking is configured to be negative, then it will equal PRU<n>_CLOCK inverted.

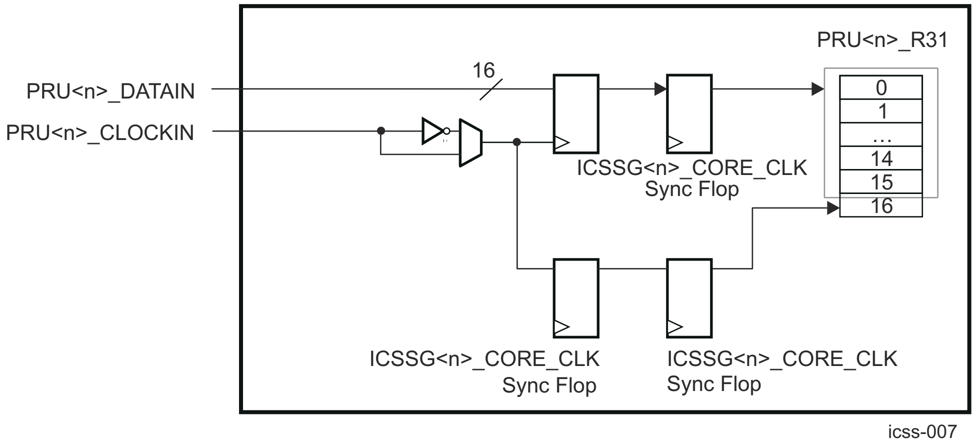

Figure 6-29. PRU R31 (EGPI) 16-Bit Parallel Capture Mode Block Diagram

6.4.5.2.2.3.3 PRU EGPIs 28-Bit Shift In

In 28-bit shift in mode, the device-level, general-purpose input pin PRU<n>_DATAIN is sampled and shifted into a 28-bit shift register on an internal clock pulse. The register fills in LSB order (from bit 0 to 27) and then overflows into a bit bucket. The 28-bit register is mapped to pru<n>_r31_status[0:27] and can be cleared in software through the ICSSG_GPCFG0_REG[13] PRU0_GPI_SB register (PRU0 or PRU1).

Note that by default, the PRU will continually capture and shift the DATAIN input when the GPI mode has been set. However, clearing the ICSSG_GPCFG0_REG[1] PRU0_GPI_SHIFT_EN bit will freeze the shift operation.

The shift rate is controlled by the effective divisor of two cascaded dividers applied to the ICSSG<n>_CORE_CLK clock. These cascaded dividers can each be configured through the PRU_ICSSG CFG register space to a value of {1, 1.5, …, 16}. Table 6-70 shows sample effective clock values and the divisor values that can be used to generate clocks from a 200MHz ICSSG<n>_CORE_CLK clock.

Table 6-70. PRU EGPIs Effective Clock Values

Generated clock	PRU0_GPI_DIV0	PRU0_GPI_DIV1
8-MHz	12.5 (17h)	2 (02h)
10-MHz	10 (12h)	2 (02h)
16-MHz	12.5 (17h)	1 (00h)
20-MHz	10 (12h)	1 (00h)

The 28-bit shift mode also supports the following features:

- SB (Start Bit detection) is mapped to pru<n>_r31_status[29] and is set when the first 1 (default) or 0 is captured on PRU<n>_DATAIN. The Start Bit value (1 or 0) is configured through the ICSSG_GPCFG0_REG[0] PRU0_GPI_SB_P bit (PRU0 or PRU1). The SB flag in pru<n>_r31_status[29] is cleared in software through the PRU_ICSSG CFG register space.
- Cnt_16 (Shift Counter) is mapped to pru<n>_r31_status[28] and is set on every 16 shift clock samples after the Start Bit has been received. CNT_16 is self clearing and is connected to the local PRU_ICSSG INTC. See the *PRU_ICSSG Local Interrupt Controller* for more details.
- The ICSSG_GPCFG0_REG[1] PRU0_GPI_SHIFT_EN bit can stop or freeze the current shift operation and disable the search for a new Start Bit, if an SB event has not occurred.

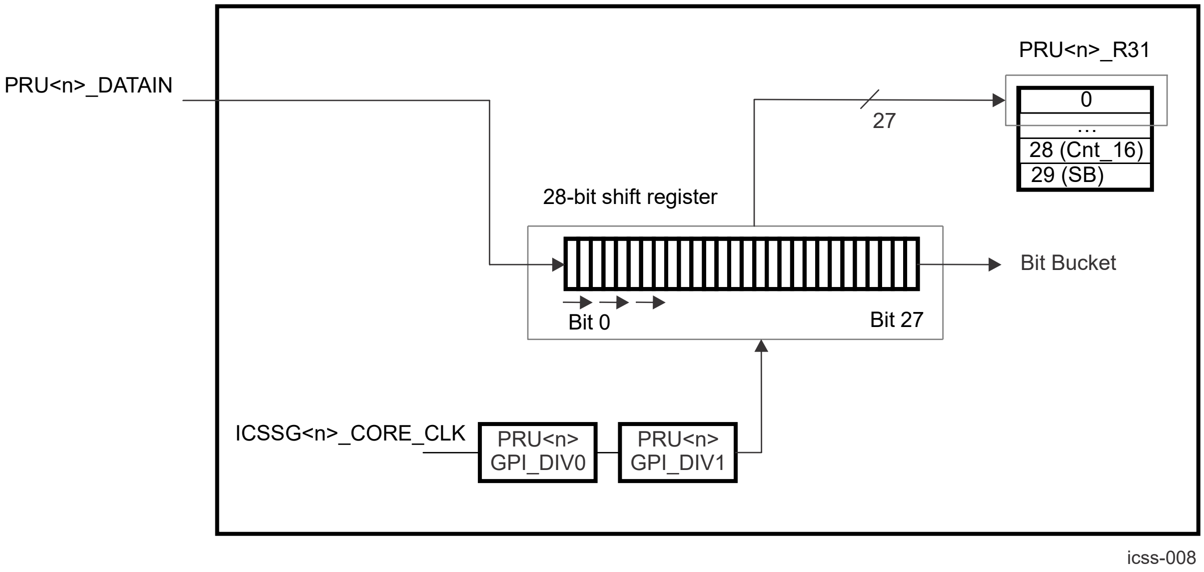

Figure 6-30. PRU R31 (EGPI) 28-Bit Shift Mode

6.4.5.2.2.3.3.1 PRU EGPI Programming Model

Follow this steps to configure the PRU EGPI in 28-bit shift input mode:

1. Clear ICSSG_GPECFG0_REG[1] PRU0_GPI_SHIFT_EN bit (PRU0 or PRU1)
2. Clear/Set ICSSG_GPECFG0_REG[0] PRU0_GPI_SB_P bit (PRU0 or PRU1)
3. Clear Start Bit by writing 1h to ICSSG_GPECFG0_REG[13] PRU0_GPI_SB bit
4. Program the dividers through:
   ICSSG_GPECFG0_REG[24-20] PRU0_GPI_DIV1 bit (PRU0 or PRU1)
   ICSSG_GPECFG0_REG[19-15] PRU0_GPI_DIV0 bit (PRU0 or PRU1)
5. Enable Shift Input Mode by writing to ICSSG_GPECFG0_REG[1] PRU0_GPI_SHIFT_EN bit

6.4.5.2.2.3.4 General-Purpose Outputs (R30): Enhanced PRU GP Module

The PRU_ICSSG implements an enhanced General Purpose Input/Output (GPIO) module that supports two general-purpose output modes: direct output and shift out.

Table 6-71 describes these modes in detail.

Note

Each PRU core can only be configured for one GPO mode at a time. Each mode uses the same R30 signals and internal register bits for different purposes. A summary is found in Table 6-71.

Note

The ICSSG_GPCFG0_REG register, bitfield [29-26] PR1_PRU0_GP_MUX_SEL (PRU0 or PRU1) in the PRU_ICSSG CFG register space needs to be set to 0h for GP mode. For a given PRU core, the following IO modes are mutually exclusive: GP mode, Sigma Delta mode, and 3 channel Peripheral I/F mode.

Table 6-71. PRU R30 (EGPO) Output Mode

Mode	Function	Configuration
Direct output	pru<n>_r30[19:0] feeds directly to GPO[19:0]	Default state

Table 6-71. PRU R30 (EGPO) Output Mode (continued)

Mode	Function	Configuration
Shift out	- pru<n>_r30[0] is shifted out on DATAOUT on every rising edge of pru<n>_r30[1] (CLOCKOUT). - LOAD_GPO_SH0 (Load Shadow Register 0) is mapped to pru<n>_r30[29]. - LOAD_GPO_SH1 (Load Shadow Register 1) is mapped to pru<n>_r30[30]. - ENABLE_SHIFT is mapped to pru<n>_r30[31].	Enabled by ICSSG_GPCFG0_REG register (PRU0 or PRU1) Free Running Clock or Fixed Clock Count Mode selected by ICSSG_GPECFG0_REG register.

Table 6-72. GPO Mode Descriptions

Pad Names at Device Level [1]	GPO Modes	
	Direct output	Shift out
PRG<k>_PRU<n>_GPO0	GPO0	DATAOUT
PRG<k>_PRU<n>_GPO1	GPO1	CLOCKOUT
PRG<k>_PRU<n>_GPO2	GPO2	
PRG<k>_PRU<n>_GPO3	GPO3	
PRG<k>_PRU<n>_GPO4	GPO4	
PRG<k>_PRU<n>_GPO5	GPO5	
PRG<k>_PRU<n>_GPO6	GPO6	
PRG<k>_PRU<n>_GPO7	GPO7	
PRG<k>_PRU<n>_GPO8	GPO8	
PRG<k>_PRU<n>_GPO9	GPO9	
PRG<k>_PRU<n>_GPO10	GPO10	
PRG<k>_PRU<n>_GPO11	GPO11	
PRG<k>_PRU<n>_GPO12	GPO12	
PRG<k>_PRU<n>_GPO13	GPO13	
PRG<k>_PRU<n>_GPO14	GPO14	
PRG<k>_PRU<n>_GPO15	GPO15	
PRG<k>_PRU<n>_GPO16	GPO16	
PRG<k>_PRU<n>_GPO17	GPO17	
PRG<k>_PRU<n>_GPO18	GPO18	
PRG<k>_PRU<n>_GPO19	GPO19	

(1) These pins are also used for Sigma Delta or Peripheral I/F mode.

6.4.5.2.2.3.4.1 PRU EGPOs Direct Output

The PRU0_r30 [19:0] bits of the internal PRU register files are mapped to device-level, general-purpose output pins (PRU0_GPO[0:19]). In GPO Direct Output mode, PRU0_r30[0:19] feed directly to PRU0_GPO[0:19]. Each PRU of the PRU_ICSSG has a separate mapping to pins, so that there are 40 total general-purpose outputs from the PRU_ICSSG. See the device's system reference guide or datasheet for device-specific pin mapping.

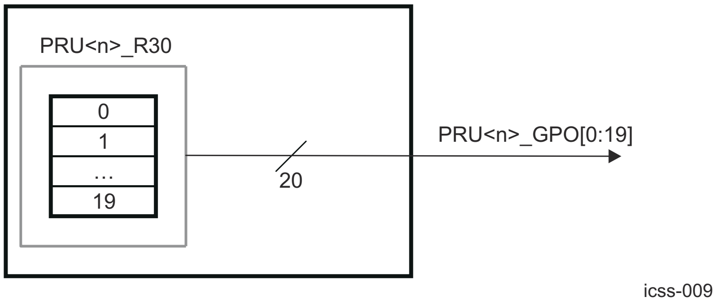

Figure 6-31. PRU R30 (EGPO) Direct Output Mode Block Diagram

Note

R30 is not initialized after reset. To avoid unintended output signals, R30 should be initialized before pinmux configuration of PRU signals.

6.4.5.2.2.3.4.2 PRU EGPO Shift Out

In shift out mode, data is shifted out of PRU0_r30[0] (PRU0_DATAOUT) on every rising edge of PRU0_r30[1] (PRU0_CLOCK). The shift rate is controlled by the effective divisor of two cascaded dividers applied to the ICSSG<n>_CORE_CLK clock. These cascaded dividers can each be configured through the PRU_ICSSG CFG register space to a value of {1, 1.5, …, 16}. Table 6-73 shows sample effective clock values and the divisor values that can be used to generate these clocks. Note that shift out mode supports two clocking submodes - Free Running Clock Mode (default) and Fixed Clock Count Mode. The clocking submode is selected through ICSSG_GPECFG0_REG[5] PRU0_GPO_SHIFT_CLK_FREE. In Free Running Clock Mode, PRU0_CLOCKOUT is a free running clock that starts when the PRU GPO mode is set to shift out mode.

Table 6-73. Effective Clock Values

Generated Clock	PRU0_GPO_DIV0	PRU0_GPO_DIV1
8 MHz	12.5 (17h)	2 (02h)
10 MHz	10 (12h)	2 (02h)
16 MHz	12.5 (17h)	1 (00h)
20 MHz	10 (12h)	1 (00h)

Shift out mode uses two 16-bit shadow registers (GPO_SH0 and GPO_SH1) to support ping-pong buffers. Each shadow register has independent load controls programmable through PRU0_r30[29:30] (PRU0_LOAD_GPO_SH[0:1]). While PRU0_LOAD_GPO_SH[0:1] is set, the contents of PRU<n>_R30[0:15] are loaded into GPO_SH0 and GPO_SH1 shadow registers.

The data shift will start from the LSB or MSB of GPO_SH0 when PRU<n>_R30[31] (PRU0_ENABLE_SHIFT) is set. The LSB or MSB setting is configurable through ICSSG_GPECFG0_REG[4] PRU0_GPO_SHIFT_SWAP. Note that if no new data is loaded into GPO_SH0/GPO_SH1 after shift operation, the shift operation will continue looping and shifting out the pre-loaded data.

For Free Running Clock Mode, the shift operation will continue until PRU0_ENABLE_SHIFT is cleared. When PRU0_ENABLE_SHIFT is cleared, the shift operation will finish shifting out the current shadow register, stop, and then reset.

For Fixed Clock Count Mode, the number of data bits to be shifted out is defined by ICSSG_GPECFG0_REG[15-8] PRU0_GPO_SHIFT_CNT. PRU<n>_CLOCKOUT will stop either high or low with the last data bit. The last data bit will remain persistent. However, the clock stop state is configurable through ICSSG_GPECFG0_REG[16] PRU0_GPO_SHIFT_CLK_HIGH.

The source of PRG<k>_PRU<n>_GPO[2:15] is configurable by ICSSG_GPECFG0_REG[6] PRU0_GPO_SHIFT_GP_EN. By default, if any device-level pins mapped to PRU<n>_R30[2-15] are configured for the PRG<k>_PRU<n>_GPO[2:15] pinmux mode, then these pins will reflect the shadow register value written to PRU<n>_R30. Any pin configured for a different pinmux setting will not reflect the shadow register value written to PRU<n>_R30. However, setting ICSSG_GPECFG0_REG[6] PRU0_GPO_SHIFT_GP_EN = 1h allows PRU<n>_R30[2:15] to be controlled by PRU<n>_R30_SHADOW[2-15], which is updated by PRU<n>_R30[2:15] when PRU<n>_R30[28] = 1h.

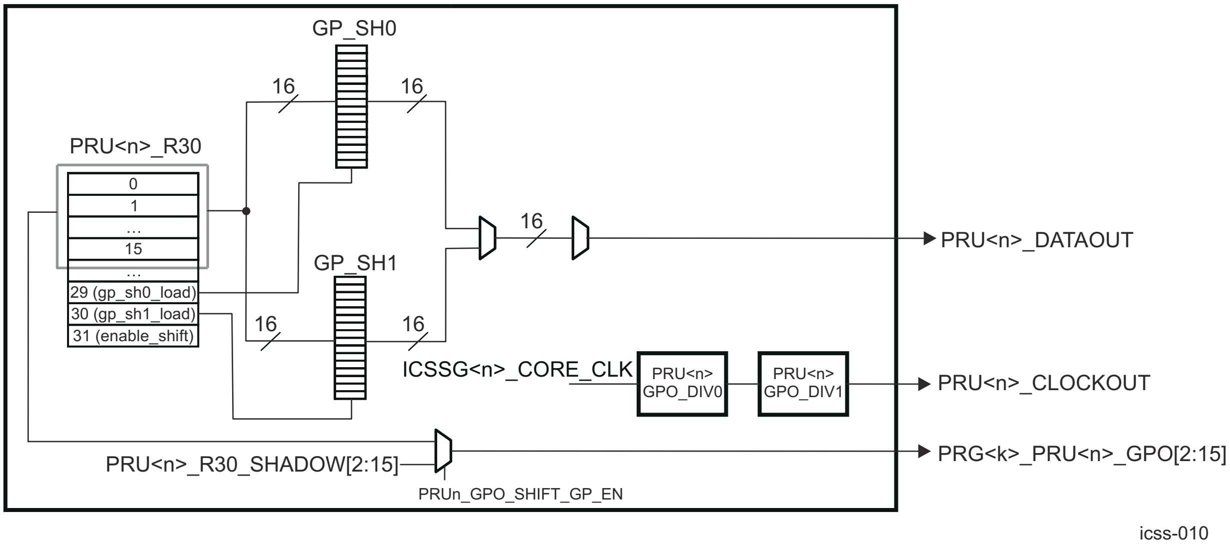

Figure 6-32. PRU R30 (GPO) Shift Out Mode Block Diagram

6.4.5.2.2.3.4.2.1 PRU EGPO Programming Model

After the PRU is intilized, the software should only enable Shift Out Mode configuration per intilization.

Follow these steps to use the GPO shift out mode:

Step 1: Initialization

1. Load 16-bits of data into GPO_SH0 shadow register:
    - GPO_SH0 = R30[29] (ICSSG_GPECFG0_REG[4] PRU0_GPO_SHIFT_SWAP (or CFG1, PRU1); R30[0-15] : R30[15-0]) : GPO_SH0)
2. Load 16-bits of data into GPO_SH1 shadow register:
    - GPO_SH1 = R30[30] (ICSSG_GPECFG0_REG[4] PRU0_GPO_SHIFT_SWAP (or CFG1, PRU1); R30[0-15] : R30[15-0]) : GPO_SH1)

Continous Mode (Free running clock mode) (ICSSG_GPECFG0_REG[5] PRU0_GPO_SHIFT_CLK_FREE = 1h):

1. R30[31] = 1h (enable shift)
2. Start Loop
3. Poll ICSSG_GPCFG0_REG[25] PRU0_GPO_SH1_SEL (or CFG1, PRU1)
    - If ICSSG_GPCFG0_REG[25] PRU0_GPO_SH1_SEL = 1h
        - Load new 16-bits of data into GPO_SH0 shadow register
4. Poll ICSSG_GPCFG0_REG[25] PRU0_GPO_SH1_SEL (or CFG1, PRU1)
    - If ICSSG_GPCFG0_REG[25] PRU0_GPO_SH1_SEL = 0h
        - Load new 16-bits of data into GPO_SH1 shadow register
5. If more data, loop to 2. Start Loop
6. If no more data, exit
7. R30[31] = 0h (enable shift)

Follow these steps to use the GPO Fixed Packet Length mode:

Fixed Packet Length Mode: (ICSSG_GPECFG0_REG[5] PRU0_GPO_SHIFT_CLK_FREE = 0h):

To enable this mode, the software should prepare the precondition to get the PRU<n>_CLOCKOUT and PRU<n>_DATAOUT in the correct defined state.

Precondition:

1. Clear ICSSG_GPCFG0_REG[14] PRU0_GPO_MODE
2. Configure the Shift Out dividers
3. Clear ICSSG_GPECFG0_REG[5] PRU0_GPO_SHIFT_CLK_FREE (PRU0 or PRU1)
4. Write ICSSG_GPECFG0_REG[16] PRU0_GPO_SHIFT_CLK_HIGH = 1h if Stop high or PRU0_GPO_SHIFT_CLK_HIGH = 0h if Stop low
5. Configure ICSSG_GPECFG0_REG[15-8] PRU0_GPO_SHIFT_CNT to 8h, in order to shift out 8-bits for precondition
6. Load data into GPO_SH0, load FFh (want one at end) or 0h (want zero at end)
7. Set R30[31] = 1h (enable shift)
8. Wait for ICSSG_GPECFG0_REG[17] PRU0_GPO_SHIFT_CLK_DONE = 1h (PRU0 or PRU1)
9. Clear R30[31] = 0h (enable shift)

After the precondition is executed, PRU<n>_CLOCKOUT and PRU<n>_DATAOUT are in the correct state, then the user can configure ICSSG_GPCFG0_REG[14] PRU0_GPO_MODE = 1h (Serial Mode).

After this operation is completed then the software controls the length of the packet along with the number of clock cycles in addition to the idle state of the clock.

ICSSG_GPECFG0_REG[15-8] PRU0_GPO_SHIFT_CNT bit field defines the number of bits shifted out.

- When it is configured to stop low (ICSSG_GPECFG0_REG[16] PRU0_GPO_SHIFT_CLK_HIGH = 0h), this equals the number of rising edge clocks minus one seen on shift clock (ICSSG<n>_CORE_CLK).
- When it is configured to stop high (ICSSG_GPECFG0_REG[16] PRU0_GPO_SHIFT_CLK_HIGH = 1h), this equals the number of rising edge clocks minus one seen on shift clock (ICSSG<n>_CORE_CLK).

This enables the software to fully control the state of shift data (PRU<n>_DATAOUT) for the first edge event. For stop low (PRU0_GPO_SHIFT_CLK_HIGH = 0h), the first edge event is rising edge, the first bit of new data is shifted 1 full clock cycle before the first rising edge seen on the shift clock (ICSSG<n>_CORE_CLK). For stop high (PRU0_GPO_SHIFT_CLK_HIGH = 1h), the first edge event is falling edge, the first bit of new data is shifted 1/2 full clock cycle before the first falling edge seen on shift clock (ICSSG<n>_CORE_CLK).

Send Data

1. Load Data into GPO_SH0/ GPO_SH1
2. Configure the ICSSG_GPECFG0_REG[15-8] PRU0_GPO_SHIFT_CNT to Nh (where N is the number of bits to be shifted out)
3. Set R30[31] = 1h (enable shift)

Active Data Loop:

1. Monitor when a shadow register has finished shifting out data and can be loaded with new data:

(a) Poll PRU0_GPO_SH1_SEL bit in the ICSSG_GPCFG0_REG register (PRU0 or PRU1)

(b) Load new 16-bits of data into GPO_SH0 if PRU0_GPO_SH1_SEL = 1h

(c) Exit loop if PRU0_GPO_SHIFT_CLK_DONE = 1h

2. If more data needs to be send, loop to Active Data Loop:

(a) Poll PRU0_GPO_SH1_SEL bit of the ICSSG_GPCFG0_REG register (PRU0 or PRU1)

(b) Load new 16-bits of data into GPO_SH1 if PRU0_GPO_SH1_SEL = 0h

(c) Jump to Active Data loop if PRU0_GPO_SHIFT_CLK_DONE = 0h

(d) Exit loop if PRU0_GPO_SHIFT_CLK_DONE = 1h

Exit:

1. Write 1h to PRU0_GPO_SHIFT_CLK_DONE bit to clear.
2. Clear R30[31] = 0h (enable shift)
3. If more data packets need to be send go to Send Data
4. If no more data, exit loop

Note: Idle time between packets must be greater than 4 clock cycles.

Note

Until the shift operation is disabled, the shift loop will continue looping and shifting out the pre-loaded data if no new data has been loaded into GPO_SH0/1.

6.4.5.2.2.3.5 Sigma Delta (SD) Decimation Filtering

Sigma-delta Sinc filtering is achieved by the combination of PRU hardware and firmware. PRU hardware provides hardware integrators that do the accumulation part of Sinc filtering, while the differentiation part is done in firmware.

The integrator serves to count the number of 1's per clock event. Each channel has three cascaded counters, which are the accumulators for the Sinc3 filter. Each counter is 28 bits, giving a maximum count of 268,435,456. Each channel has a free running rollover clock counter. This sample counter updates the count value on the effective clock event for that channel. Each channel also contains a programmable counter compare block, and the compare register has a size of 8 bits. However, the minimum value is 4 and maximum value is 256 due to the 28-bit accumulator. Once sample counter compare value is reached, the shadow register copy is updated and the shadow register copy flag is set.

Features of the integrators in PRUs SD Demodulator:

- Up to 9 channels concurrent counting
- Software can read all 3 stages accumulators
- Flexible clock source configuration for each channel; option of independent clock source for each channel or one clock source for three channels
- Programmable, 8-bit sample counter compare register; used to set the OSR of Sinc filter
- Three 28-bit cascaded counters per channel for accumulation, only Sinc3 and Sinc2 modes supported
- Common channel enable (all channels are active or none are active)
- Fast 1 and 0 min/max count sliding programmable window for each of the 9 channels
- Load sharing option which enables RTU to own channels SD0-SD2, PRU to own SD3-SD5, and TX_PRU to own SD6-SD8
- Manchester decode mode of operation per SD channel that removes the need of CLK. Controlled via ICSSG_PRU0_SD_CFG_REG

6.4.5.2.2.3.5.1 Sigma Delta Block Diagram and Signals

The Sigma Delta's I/Os are multiplexed with the PRU GPI/GPO signals, as shown in Table 6-74.

Note: The PR<k>_PRU<n>_GP_MUX_SEL bitfield in the ICSSG_GPCFG0_REG register (where k = 0 or 1 and n = 0 or 1) must be set to 3h for configure the GPI/GPO signals for SD mode.

Table 6-74. PRU GPI Signals and Configurations for Sigma Delta

Signal Names at Device Level (1)	Sigma Delta (SD) Mode	Function
PRG<k>_PRU<n>_GPI0	SD0_CLK	SD demodulator clock channel 0
PRG<k>_PRU<n>_GPI1	SD0_D	SD demodulator data channel 0
PRG<k>_PRU<n>_GPI2	SD1_CLK	SD demodulator clock channel 1

Table 6-74. PRU GPI Signals and Configurations for Sigma Delta (continued)

Signal Names at Device Level [1]	Sigma Delta (SD) Mode	Function
PRG<k>_PRU<n>_GPI3	SD1_D	SD demodulator data channel 1
PRG<k>_PRU<n>_GPI4	SD2_CLK	SD demodulator clock channel 2
PRG<k>_PRU<n>_GPI5	SD2_D	SD demodulator data channel 2
PRG<k>_PRU<n>_GPI6	SD3_CLK	SD demodulator clock channel 3
PRG<k>_PRU<n>_GPI7	SD3_D	SD demodulator data channel 3
PRG<k>_PRU<n>_GPI8	SD4_CLK	SD demodulator clock channel 4
PRG<k>_PRU<n>_GPI9	SD4_D	SD demodulator data channel 4
PRG<k>_PRU<n>_GPI10	SD5_CLK	SD demodulator clock channel 5
PRG<k>_PRU<n>_GPI11	SD5_D	SD demodulator data channel 5
PRG<k>_PRU<n>_GPI12	SD6_CLK	SD demodulator clock channel 6
PRG<k>_PRU<n>_GPI13	SD6_D	SD demodulator data channel 6
PRG<k>_PRU<n>_GPI14	SD7_CLK	SD demodulator clock channel 7
PRG<k>_PRU<n>_GPI15	SD7_D	SD demodulator data channel 7
PRG<k>_PRU<n>_GPI16	SD8_CLK	SD demodulator clock channel 8
PRG<k>_PRU<n>_GPI17	SD8_D	SD demodulator data channel 8
PRG<k>_PRU<n>_GPI18	-	
PRG<k>_PRU<n>_GPI19	-	

(1) Note: These signals are shared with the GP and Peripheral I/Fs. To configure for Sigma Delta, ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL (where k = 0 or 1 and n = 0 or 1) needs to be set to 3h for SD mode.

The PRG<k>_PRU0_GPI1 signal (muxed with SD0_D) can be used as SD_CLKOUT when PRU_ICSSG generates clock. This is a trade-off as PRU application will lose one SD channel. SD_CLKOUT needs to go through a clock generator chip if driving multiple sigma delta modulators and also be looped back into PRU_ICSSG as SD_CLKIN, typically pru_gpi16.

Note: To output the SD clock on PR<k>_PRU0_GPO1, this device requires that the PRU core be configured for both SD and shift out mode (ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL = 3h and ICSSG_GPCFG0_REG[14] PRU<n>_GPO_MODE = 1h). Be sure to configure the shift out mode's clock divisors before enabling shift out mode (ICSSG_GPCFG0_REG[14] PRU<n>_GPO_MODE = 1h). Additionally, the PRU_ICSSG0, PRU0 SD clock is routed to both PR0_PRU0_GPO1 and PR0_PRU1_GPO1. Figure 6-33 shows a block diagram of the Sigma Delta implementation. Full description of the PRU R30 and R31 registers are shown in Table 6-76 and Table 6-77.

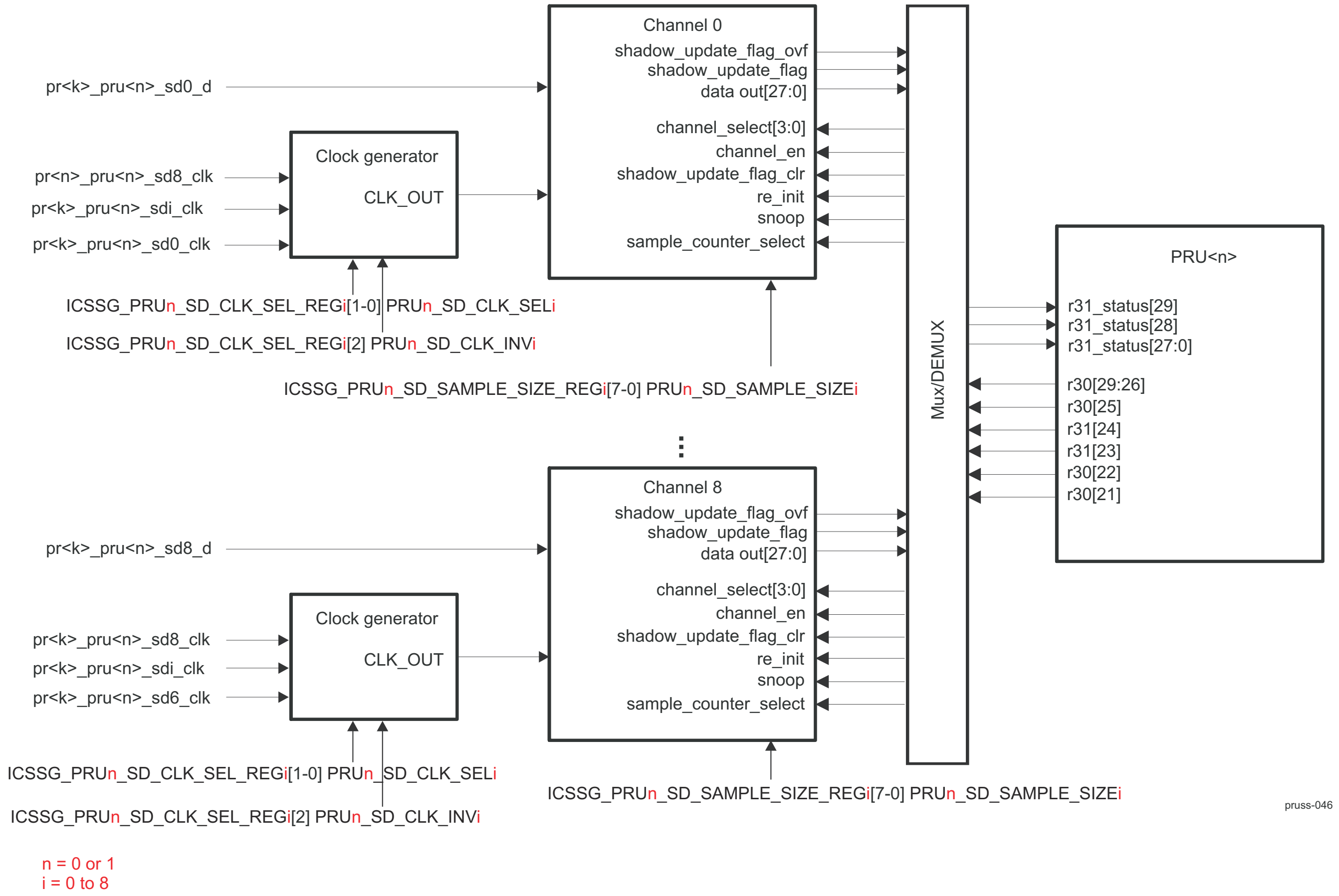

Figure 6-33. Sigma Delta Block Diagram

Note: Each channel can independently be configured to use one of three external clock sources. Table 6-75 shows the clock source options, selectable through ICSSG_PRU0_SD_CLK_SEL_REGi[1-0] PRU0_SD_CLK_SELi (where n = 0 or 1 and i = 0 to 8).

Table 6-75. Sigma Delta External Clock Sources

PRU0_SD_CLK_SELi value	Clock Source
0	pr<k>_pru<n>_sd8_clk
1	pr<k>_pru<n>_sd<i>_clk
2	pr<k>_pru<n>_sd0_clk for sd0, sd1, and sd2; pr<k>_pru<n>_sd3_clk for sd3, sd4, and sd5; pr<k>_pru<n>_sd6_clk for sd6, sd7, and sd8

6.4.5.2.2.3.5.2 PRU R30 / R31 Interface

The PRU uses the R30 and R31 registers to interface with the Sigma Delta interface. Table 6-76 and Table 6-77 shows the R31 and R30 interface for the Sigma Delta mode. Note that only the parameters and data for one channel can be viewed at a time. The channel to be viewed is determined by the r30[29-26] (channel_select).

Table 6-76. Sigma Delta PRU Registers: R31

Bits	Field Name	Description
31-30	Reserved	
29	shadow_update_flag_ovf	Shadow update flag overflow, set when over sample count equals over sample size and shadow_update_flag is still set. Set bit R31[24] to clear the flag.
28	shadow_update_flag	Shadow update flag, set when over sample count equals over sample size and shadow_update_flag is still set. Set bit R31[24] to clear the flag.

Table 6-76. Sigma Delta PRU Registers: R31 (continued)

Bits	Field Name	Description
27-0	data_out[27-0]/ shadow_update_flag_clr (R31[24]) / re_init (R31[23])	data_out[27] (read): most-significant bit of sample data shadow_update_flag_clr (write): re_init (write): Set to reset all counters, flags, and shadow copy. Updates over_sample_size based on the current ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[7-0] register (where n = 0 or 1 and i = 0 to 8) on the selected channel. shadow_update_flag_clr (write): Set to clear shadow_update_flag and shadow_update_flag_ovf (if set).

Table 6-77. Sigma Delta PRU Registers: R30

Bits	Field Name	Description
31-30	Reserved	
29-26	channel_select[3-0]	Channel select(1) 0h: Channel 0 ... 8h: Channel 8 9h: Reserved ... Fh: Reserved
25	channel_en	Global Channel enable (effects all 9 channels). 0h: All channels disabled. Counters/flags are cleared. 1h: All channels enabled.
24-23	Reserved	
22	snoop	Enable snoop (i.e. fetch data) on the selected channel. 0h: acc1/acc2/acc3 shadow copy 1h: current acc1/acc2/acc3
21	sample_counter_select	Read sample counter. 0h: Not selected 1h: Sample count selected
20-0	Reserved	

(1) If ICSSG_PRU0_SD_CFG_REG[8] SHARE_EN = 1, SD channels are shared between RTU, PRU, and TX_PRU, 3 channels per CPU.

The PRU_ICSSG CFG register space has additional registers for controlling the SD demodulator module:

- ICSSG_PRU0_SD_CLK_SEL_REGi[5-4] PRU0_SD_ACC_SELi (where n = 0 or 1, i = 0 to 8) - Selects accumulator 1, 2 or 3 as source (acc1/acc2/acc3).
- ICSSG_PRU0_SD_CLK_SEL_REGi[2] PRU0_SD_CLK_INVi (where n = 0 or 1, i = 0 to 8) - Inverts clock.
- ICSSG_PRU0_SD_CLK_SEL_REGi[1-0] PRU0_SD_CLK_SELi (where n = 0 or 1, i = 0 to 8) - Selects the clock source.
- ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[7-0] PRU0_SD_SAMPLE_SIZEi (where n = 0 or 1, i = 0 to 8) - Selects number of samples to read before giving output.

6.4.5.2.2.3.5.3 Sigma Delta Description

Figure 6-34 shows a block diagram of the Sigma Delta hardware integrators and integration with the PRU R30 / R31 interface for a single channel.

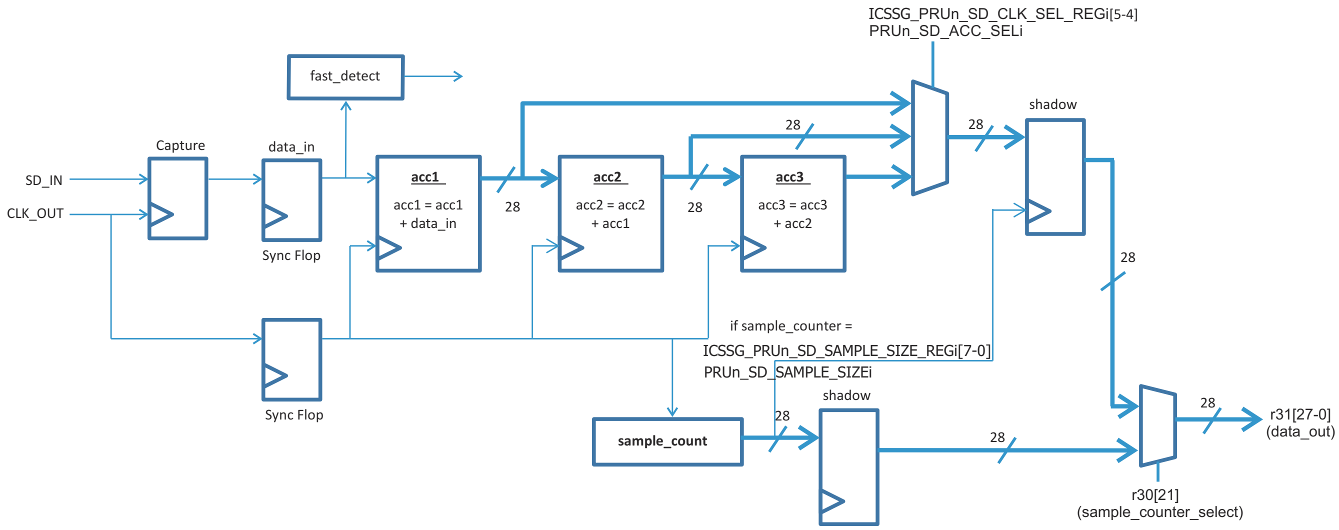

Figure 6-34. Sigma Delta Hardware Integrators Block Diagram (snoop = 0)

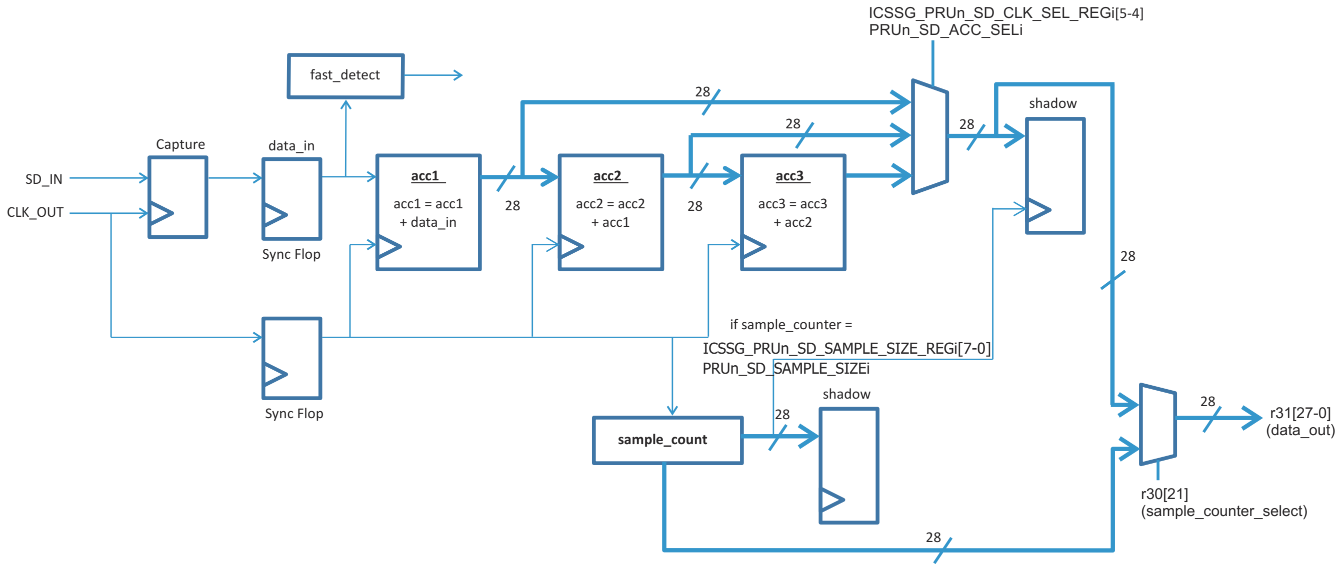

Figure 6-35. Sigma Delta Hardware Integrators Block Diagram (snoop = 1)

The three accumulators (acc1-acc3) for each channel are simple 28 bit adders. The input for acc1 is 1-bit, while the inputs for acc2 and acc3 are 28-bits. On each positive edge of the CLK_OUT, all three 28-bit counters (acc1-acc3) and the sample counter for each channel will get updated as follows:

```
acc1 = acc1 + data_in
acc2 = acc2 + acc1
acc3 = acc3 + acc2
sample_count = sample_count + 1
```

Each accumulator will rollover at 0xFF_FFFF. For example if acc2 = 0x10 and acc3 = 0xFF_FFFF, then acc3 will update to 0x00_0000F on the next clock event. Sample counter will rollover when it equals the defined sample size (ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[7-0] PRU0_SD_SAMPLE_SIZEi).

Note that while the channels are not enabled, no operations are performed and all flags and counters are cleared. If a new sample size is to be loaded, the PRU firmware should assert re_init (r31[23]), and all stored count values are cleared to 0.

Fast detect block is used to detect fast changes in the amount of ones, presented in a programmable sliding window of 4 to 32 bits. The sliding window is controlled by ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[10-8] PRU0_FD_WINDOW_SIZE_i bit field.

Fast detect must be enabled through the ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[23] PRU0_FD_EN_i register before SD is enabled. It will start the compare after the first 32 sample clocks. Fast detect block will remain active until a re_init (r31[23]) is asserted.

The Sigma Delta interface has two status flags:

- Shadow update flag (r31[28])
- Shadow update flag overflow (r31[29])

When sample_counter equals the defined sample size (ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[7-0] PRU0_SD_SAMPLE_SIZEi), then the acc1/acc2/acc3 shadow register copy will be updated, the shadow_update_flag (r31[28]) will be set, and sample_counter will rollover to 0. The PRU firmware can clear this flag by writing ‘1’ to shadow_update_flag_clr (r31[28]). If sample_count equals the defined sample size and the shadow_update_flag is still set, then shadow_update_flag_ovf (r31[29]) will be set. Similarly, the PRU firmware can clear this flag by writing ‘1’ to shadow_update_flag_ovf_clr (r31[29]). Note that the clear operation for both flags has a higher priority than the set event.

The PRU firmware can monitor the acc2/acc3 and sample_counter values through data_out[27-0] (r31[27-0]). Table 6-78 shows the configuration options for data_out[27-0].

Table 6-78. Data_out[27-0] Configuration Options

snoop (r30[22])	sample_counter_select (r30[21])	data_out (r31[27-0])
0	0	Reads acc1/acc2/acc3 shadow register copy. See Figure 6-34 *Sigma Delta Hardware Integrators Block Diagram (snoop = 0)*.
1	0	Reads acc1/acc2/acc3 directly. See Figure 6-35 *Sigma Delta Hardware Integrators Block Diagram (snoop = 1)*.
0	1	Reads sample_counter shadow register copy. See Figure 6-34 *Sigma Delta Hardware Integrators Block Diagram (snoop = 0)*.
1	1	Reads sample_counter directly. See Figure 6-35 *Sigma Delta Hardware Integrators Block Diagram (snoop = 1)*.

6.4.5.2.2.3.5.4 Sigma Delta Basic Programming Example

The following programming example assumes that the PRU is configured for Sigma Delta Mode (ICSSG_GPCFG0_REG[29-26] PR1_PRU<n>_GP_MUX_SEL = 3h).

1. Configure clock sources, accumulator source, and sample size:
    a. ICSSG_PRU0_SD_CLK_SEL_REGi[1-0] PRU0_SD_CLK_SELi (where n = 0 or 1, i = 0 to 8) for clock source
    b. ICSSG_PRU0_SD_CLK_SEL_REGi[2] PRU0_SD_CLK_INVi (where n = 0 or 1, i = 0 to 8) for clock polarity
    c. ICSSG_PRU0_SD_CLK_SEL_REGi[5-4] PRU0_SD_ACC_SELi (where n = 0 or 1, i = 0 to 8) - for accumulator source (acc1/acc2/acc3)
    d. ICSSG_PRUSS_SD_PRU0_SAMPLE_SIZE_REGISTERi[7-0] PRU0_SD_SAMPLE_SIZE for sample size

2. Reinitialize all channels whose sample size was configured
    a. Select channel by writing to channel_select (r30[29-26])
    b. Delay at least 1 PRU cycle before executing re_int in step 2c.
    c. Reinitialize selected channel by writing to re_init (r31[23])
    d. Repeat steps 2a & 2b for all configured channels

3. Enable all channels by writing ‘1’ to channel_en (r30[25])
4. Select channel by writing to channel_select (r30[29-26])

  a. Poll shadow_update_flag (r31[28]) to detect when acc1/acc2/acc3 shadow register copy data is ready to be read
  b. Delay at least 1 PRU cycle before polling shadow_update_flag in Step 4c.
  c. Read data_out[27-0] (r31[27-0])
  d. Clear shadow_update_flag by writing ‘1’ to r31[24]

5. Repeat step 4 for new channel

6.4.5.2.2.3.6 Three Channel Peripheral Interface

The 3 channel Peripheral Interface supports functionality for operations utilizing the EnDat 2.2 and BiSS protocols.

This module supports the following features:

- 3 channels with baud range from 100 kHz to 16 MHz
- ICSSGn_UART_CLK (default) or ICSSGn_CORE_CLK controller clock is an input to independent div16fr clock dividers to produce a 1X clock (PERIF<m>_CLK) and oversampling clock
- Half-duplex (TX and RX are not supported concurrently)
- TX FIFO size of 32 bits
- RX FIFO size of 4 bits
- Configurable shift size/oversampling on RX
- Optional RX frame size auto shut off
- Programmable HW delay 1 (wire delay, controlling when the clock signal is first driven low) and delay 2 (tst delay, controlling when the clock signal is first driven high) on TX operation
- Optional programmable TX termination
- Individual TX channel start trigger (tx_channel_go) or simultaneous TX start trigger for all channels (tx_global_go)
- Flexible HW assisted clock output generation to allow free running, stop high and stop low (after last RX data), or stop high (after last TX data) operation with optional software clock override feature
- Optional SW direct snoop of data input
- RX Start Bit of '1' or '0'

6.4.5.2.2.3.6.1 Peripheral Interface Block Diagram and Signal Configuration

The Peripheral Interface’s I/Os are multiplexed with the PRU GPI/GPO signals, as shown in Table 6-79. The PR1_PRU<n>_GP_MUX_SEL bitfield in the ICSSG_GPCFG0_REG register (PRU0 or PRU1) must be set to 1h for configure the GPI/GPO signals for Peripheral I/F mode.

Table 6-79. PRU GPI/GPO Signals and Configurations for Peripheral I/F(1)

Pad Names at Device Level(2)(3)	Peripheral I/F Mode (ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL = 1h)
PRG<k>_PRU<n>_GPI0	
PRG<k>_PRU<n>_GPI1	
PRG<k>_PRU<n>_GPI2	
PRG<k>_PRU<n>_GPI3	
PRG<k>_PRU<n>_GPI4	
PRG<k>_PRU<n>_GPI5	
PRG<k>_PRU<n>_GPI6	
PRG<k>_PRU<n>_GPI7	
PRG<k>_PRU<n>_GPI8	
PRG<k>_PRU<n>_GPI9	PERIF0_IN
PRG<k>_PRU<n>_GPI10	PERIF1_IN
PRG<k>_PRU<n>_GPI11	PERIF2_IN
PRG<k>_PRU<n>_GPI12	
PRG<k>_PRU<n>_GPI13	

Table 6-79. PRU GPI/GPO Signals and Configurations for Peripheral I/F[1] (continued)

Pad Names at Device Level[2][3]	**Peripheral I/F Mode (ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL = 1h)**
PRG<k>_PRU<n>_GPI14	
PRG<k>_PRU<n>_GPI15	
PRG<k>_PRU<n>_GPI16	
PRG<k>_PRU<n>_GPI17	
PRG<k>_PRU<n>_GPI18	
PRG<k>_PRU<n>_GPI19	
PRG<k>_PRU<n>_GPO0	PERIF0_CLK
PRG<k>_PRU<n>_GPO1	PERIF0_OUT
PRG<k>_PRU<n>_GPO2	PERIF0_OUT_EN
PRG<k>_PRU<n>_GPO3	PERIF1_CLK
PRG<k>_PRU<n>_GPO4	PERIF1_OUT
PRG<k>_PRU<n>_GPO5	PERIF1_OUT_EN
PRG<k>_PRU<n>_GPO6	PERIF2_CLK
PRG<k>_PRU<n>_GPO7	PERIF2_OUT
PRG<k>_PRU<n>_GPO8	PERIF2_OUT_EN
PRG<k>_PRU<n>_GPO9	
PRG<k>_PRU<n>_GPO10	
PRG<k>_PRU<n>_GPO11	
PRG<k>_PRU<n>_GPO12	
PRG<k>_PRU<n>_GPO13	
PRG<k>_PRU<n>_GPO14	
PRG<k>_PRU<n>_GPO15	
PRG<k>_PRU<n>_GPO16	
PRG<k>_PRU<n>_GPO17	
PRG<k>_PRU<n>_GPO18	
PRG<k>_PRU<n>_GPO19	

(1) Usage of the Peripheral Interface signals are not restricted to only ENDAT interfaces.

(2) These signals are shared with the GP, MII and Sigma Delta modes. To configure for Peripheral I/F, ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL needs to be set to 1h.

(3) Some devices may not pin out all 29 bits of R31 and all 32 bits of R30. For which pins are available on this device, see *PRU_ICSSG Environment*. See the device-specific Datasheet for device pin mapping.

A block diagram for the Peripheral I/F is included in Figure 6-36. As shown, each channel is composed of four I/Os:

- PERIF<m>_IN - RX input data
- PERIF<m>_CLK - Clock (CLK_OUT) generated by the 1x (or TX) clock. The default value is 1.
- PERIF<m>_OUT - TX output data. The default value is 0.
- PERIF<m>_OUT_EN - TX enable output (1 = TX mode, 0 = RX mode). The default value is 0. Note: This signal is auto controlled by hardware.

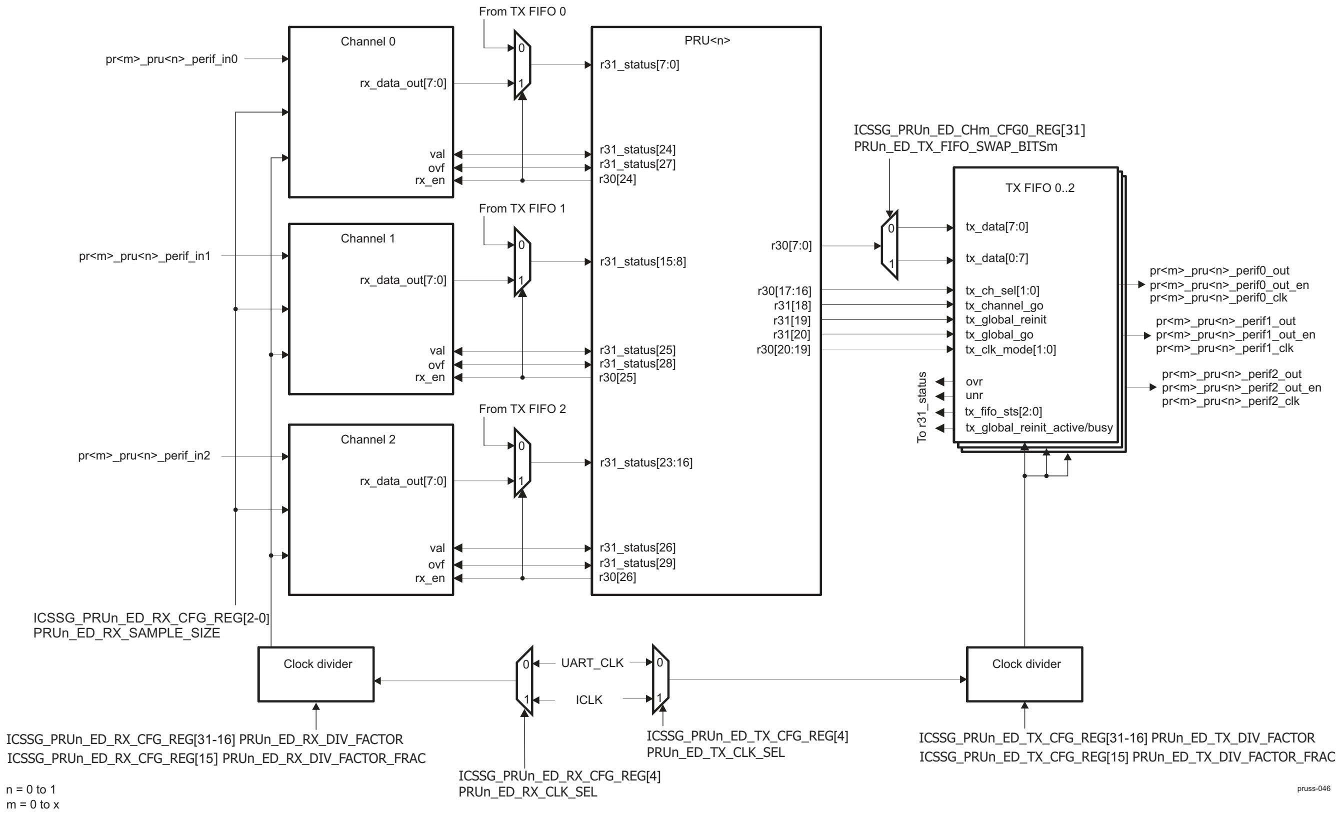

Figure 6-36. Peripheral I/F Block Diagram

Note

m is the number of PRU_ICSSG in the device. See the Datasheet for additional details.

6.4.5.2.2.3.6.2 PRU R30 and R31 Interface

The PRU uses the R30 and R31 registers to interface with the Peripheral I/F. Table 6-80 shows the R31 and R30 interface for the Peripheral I/F RX mode, and Table 6-81 shows the comparable interface for the TX mode.

Table 6-80. Peripheral I/F RX

Register	Bits	Field name	Description
R31	31-30	Reserved	PRU Host Interrupts 1/0 from local INTC
	29	ovf2	Overflow Flag for Channel 2. Write 1 to clear.
	28	ovf1	Overflow Flag for Channel 1. Write 1 to clear.
	27	ovf0	Overflow Flag for Channel 0. Write 1 to clear.
	26	val2	Valid Flag for Channel 2. Write 1 to clear.
	25	val1	Valid Flag for Channel 1. Write 1 to clear.
	24	val0	Valid Flag for Channel 0. Write 1 to clear.
	23-16	rx_data_out2	Oversampled Data Output for Channel 2. Note: These bits are shared with the TX Interface. When TX_FIFO has stopped transmission, RX data will be selected.
	15-8	rx_data_out1	Oversampled Data Output for Channel 1. Note: These bits are shared with the TX Interface. When TX_FIFO has stopped transmission, RX data will be selected.
	7:0	rx_data_out0	Oversampled Data Output for Channel 0. Note: These bits are shared with the TX Interface. When TX_FIFO has stopped transmission, RX data will be selected.
R30	31-27	Reserved	

Table 6-80. Peripheral I/F RX (continued)

Register	Bits	Field name	Description
	26	rx_en2	RX Enable for Channel 2. 0h: Channel not enabled, all counters/flags will get reset 1h: Channel is enabled
	25	rx_en1	RX Enable for Channel 1. 0h: Channel not enabled, all counters/flags will get reset 1h: Channel is enabled
	24	rx_en0	RX Enable for Channel 0. 0h: Channel not enabled, all counters/flags will get reset 1h: Channel is enabled
	23-0	Reserved	

Table 6-81. Peripheral I/F TX

Register	Bits	Field name	Description
R31	31-30	Reserved	
	29-22	Reserved	
	21	tx_global_reinit_active/ busy2	Tx_global_reinit action has some latency do to clocking. This status shows if action is completed. 1h: Active 0h: Done For non reinit case, this bit states that last bit is on tx wire. It does not mean the clock is off. 1h: Last bit is not done 0h: Last bit on tx wire Note that by using rx auto arm feature, the observation is lost at rx enable. This can be used to determine when to enable rx during non-auto arm case.
	20-18(1)	tx_fifo_sts2	TX FIFO occupancy status for Channel 2. 0 :0 Empty 1h: 1 word 2h: 2 words 3h: 3 words 4h: Full 5h-7h: Reserved
	20(2)	tx_global_go	TX global start of all channels. Note: FIFO must not be empty. If empty, transmit will not start.
	19(2)	tx_global_reinit	Reinit all channels into default mode. This clears all flags and state machines for all channels. Note: Sequence should be assert tx_global_reinit then de-assert rx_en. This will ensure TX and RX are in reset/default state. User must assert this after the frame has been sent and TX is not busy.
	18(2)	tx_channel_go	TX start the channel transmit (selected by tx_ch_sel). Note: FIFO must not be empty.
	17	unr2	Under Run Flag for Channel 2. This flag is only set when the tx_frame_count is nonzero and FIFO is empty at time to send data.
	16	ovr2	Over Run Flag for Channel 2
	15-14	Reserved	
	13	tx_global_reinit_active/ busy1	Tx_global_reinit action has some latency do to clocking. This status shows if action is completed. 1h: Active 0h: Done For non reinit case, this bit states that last bit is on tx wire. It does not mean the clock is off. 1h: Last bit is not done 0h: Last bit on tx wire Note that by using rx auto arm feature, the observation is lost at rx enable. This can be used to determine when to enable rx during non-auto arm case.

Table 6-81. Peripheral I/F TX (continued)

Register	Bits	Field name	Description
	12-10	tx_fifo_sts1	TX FIFO occupancy status for Channel 1. 0 :0 Empty 1h: 1 word 2h: 2 words 3h: 3 words 4h: Full 5h-7h: Reserved
	9	unr1	Under Run Flag for Channel 1. This flag is only set when the tx_frame_count is nonzero and FIFO is empty at time to send data.
	8	ovr1	Over Run Flag for Channel 1
	7-6	Reserved	
	5	tx_global_reinit_active/ busy0	Tx_global_reinit action has some latency do to clocking. This status shows if action is completed. 1h: Active 0h: Done For non reinit case, this bit states that last bit is on tx wire. It does not mean the clock is off. 1h: Last bit is not done 0h: Last bit on tx wire Note that by using rx auto arm feature, the observation is lost at rx enable. This can be used to determine when to enable rx during non-auto arm case.
	4-2	tx_fifo_sts0	TX FIFO occupancy status for Channel 0. 0h: Empty 1h: 1 word 2h: 2 words 3h: 3 words 4h: Full 5h-7h: Reserved
	1	unr0	Under Run Flag for Channel 0. This flag is only set when the tx_frame_count is nonzero and FIFO is empty at time to send data.
	0	ovr0	Over Run Flag for Channel 0
R30	31-21	Reserved	
	20-19	clk_mode	CLK_OUT mode. 0h: Free-running/stop-low. Clock will remain free-running until the receive module has received the number of bits indicated in rx_frame_counter and then the clock will stop low. 1h: Free-running/stop-high (default). Clock will remain free-running until the receive module has received the number of bits indicated in rx_frame_counter and then the clock will stop high. Note: This is the default/reset state, and a hardware reset or reinit will return clk_mode to this state. Note: The initial state of the clock will be high, but the clock will not start until TX GO event. 2h: Free-run. NOTE: You must do a reinit to get out of this clock mode then you can update clk_mode to a different mode. Also if you do multiple TX GO, the 2nd go should have tst_delay and wire_delay zero since the clock is free running after the first go. 3h: Stop high after transmit. Clock will run until the last TX bit is sent and stops high.
	18	Reserved	
	17-16	tx_ch_sel	TX channel select. 0h: Channel 0 1h: Channel 1 2h: Channel 2 3h: Reserved
	15-9	Reserved	

Table 6-81. Peripheral I/F TX (continued)

Register	Bits	Field name	Description
	7-0	tx_data	TX data for FIFO. Notes: FIFO transmits MSB first and is 32-bits deep. TX_FIFO_SWAP_BITS bit in the PRU_ICSSG CFG register space can be used to flip the load order of bits. The FIFO has 2 modes of operation: 1. Preload and Go. This should be done for EnDAT and frames less than 32-bits. 2. Continuous mode. This should be done for frames bigger than 32-bits. In continuous mode, software needs to keep up with the line rate and ensure that the FIFO is never empty. When the FIFO is at 2 byte level, software needs to load the next 2 bytes. If software waits till the end of the empty state, it is possible to get the TX into a bad state. The FIFO state can be recovered via re-init.

(1) When rx_en<n> = 0

(2) When rx_en<n> = 1

Note

The PRU_ICSSG CFG register space has additional registers for controlling the Peripheral I/F module.

6.4.5.2.2.3.6.3 Clock Generation

6.4.5.2.2.3.6.3.1 Configuration

The Peripheral I/F module has two source clock options, ICSSGn_UART_CLK (default) and ICSSGn_CORE_CLK. There are two independent clock dividers (div16) for the 1x and oversampling (OS) clocks, and each clock divider is configurable by two cascading dividers:

- [31-16] PRU0_ED_TX_DIV_FACTOR and [15] PRU0_ED_TX_DIV_FACTOR_FRAC for the 1x clock
- [31-16] PRU0_ED_RX_DIV_FACTOR and [15] PRU0_ED_RX_DIV_FACTOR_FRAC for the OS clock

The 1x clock is output on the PERIF<m>_CLK signal. In TX mode, the output data is read from the TX FIFO at this 1x clock rate. The default value of this clock is high and the start and stop conditions for this clock are described in Section 6.4.5.2.2.3.6.3.2 *Clock Output Start Conditions* and Section 6.4.5.2.2.3.6.3.3 *Stop Conditions*.

In RX mode, the input data is sampled at the OS clock rate. Note: The OS clock rate divided by the 1x clock rate must equal [2-0] PRU0_ED_RX_SAMPLE_SIZE.

Example clock rates and divisor values relative to the 192-MHz ICSSGn_UART_CLK source are shown in Table 6-82.

Table 6-82. Clock Rate Examples for 192-MHz PRUSSn_UART_GFCLK Clock Source

TX_DIV_FACTOR	1x Clock	RX_DIV_FACTOR	RX_DIV_FACTOR_FRAC	OS Clock	Oversample Factor
12	16 MHz	1	1.5	128 MHz	8x
16	12 MHz	2	1	96 MHz	8x
24	8 MHz	3	1	64 MHz	8x
32	6 MHz	4	1	48 MHz	8x
48	4 MHz	6	1	32 MHz	8x
96	2 MHz	12	1	16 MHz	8x
192	1 MHz	24	1	8 MHz	8x

6.4.5.2.2.3.6.3.2 Clock Output Start Conditions

This section describes the configurable start conditions for the PERIF<m>_CLK. The software can completely control via ICSSG_PRU0_ED_CHm_CFG0_REG when bit [29] PRU0_ED_CLK_OUT_OVR_ENm = 1h (where n = 0 or 1 and m = 0 to 2). By default however, the PRU hardware will control the clocks as described in the following sections.

6.4.5.2.2.3.6.3.2.1 TX Mode (RX_EN = 0)

In TX mode, the PERIF<m>_CLK begins after the firmware loads the TX FIFO and sets either r30[20] (tx_global_go) or r30[17-16] (tx_channel_go) to 1h. After the “go” bit is set, the delay1 (wire delay) compensation counter for each channel begins. After delay1 is complete, PERIF<m>_CLK is driven low and then the delay2 (tst) counter begins. After the delay2 counter expires, the PERIF<m>_CLK starts running (first low and then high). Therefore, first rising edge of PERIF<m>_CLK (measured from the go bit) = delay1 (tx wire delay) + delay2 (tst_counter delay) + half of the 1x clock frequency (since the clock starts low).

Figure 6-37 shows the start condition for TX mode. As shown in the figure, the default value of clock is high. The PRU_ICSSG CFG register space has additional registers for controlling the TX start timing delay values:

- Delay 1: ICSSG_PRU0_ED_CHm_CFG0_REG[10-0] PRU0_ED_TX_WDLYm (where n = 0 or 1 and m = 0 to 2)
- Delay 2: ICSSG_PRU0_ED_CHm_CFG1_REG[15-0] PRU0_ED_TST_DELAY_COUNTERm (where n = 0 or 1 and m = 0 to 2)

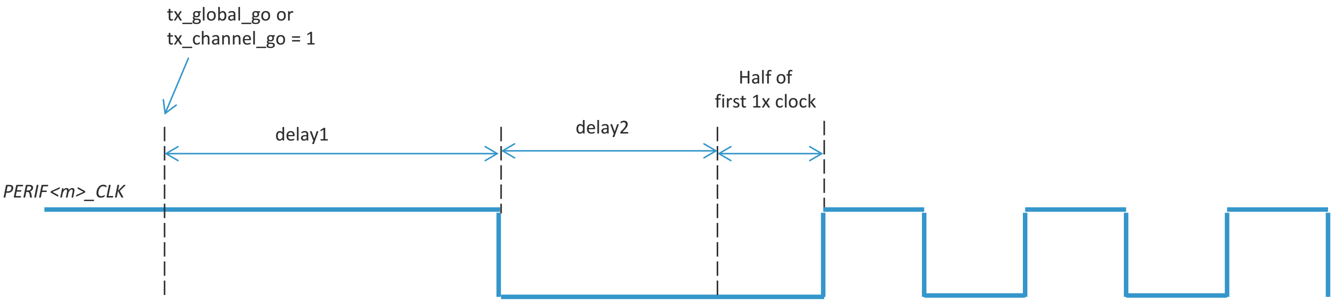

Figure 6-37. TX Mode Start Condition

6.4.5.2.2.3.6.3.2.2 RX Mode (RX_EN = 1)

In RX mode, the PERIF<m>_CLK will start running whenever the RX_EN is set. Note that the PRU firmware in this mode is responsible for any delay conditions.

The hardware can also auto-enable RX mode at the end of a TX transaction. The ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm (where n = 0 or 1 and m = 0 to 2) is used to program a delay between the last TX bit sent and when the RX_EN is set.

6.4.5.2.2.3.6.3.3 Stop Conditions

The r30[20-19] (clk_mode[1:0]) value determines the stop condition for PERIF<m>_CLK. There are 4 options available:

clk_mode_value	Description
0	Stop low on last RX frame
1	Stop high on last RX frame
2	Run continuously
3	Stop high on last TX bit

The last RX frame is configured by ICSSG_PRU0_ED_CHm_CFG0_REG[27-16] PRU0_ED_RX_FRAME_SIZEm, and the last TX bit is configured by ICSSG_PRU0_ED_CHm_CFG0_REG[15-11] PRU0_ED_TX_FRAME_SIZEm (where n = 0 or 1 and m = 0 to 2). Each stop condition is shown in Figure 6-38 through Figure 6-41.

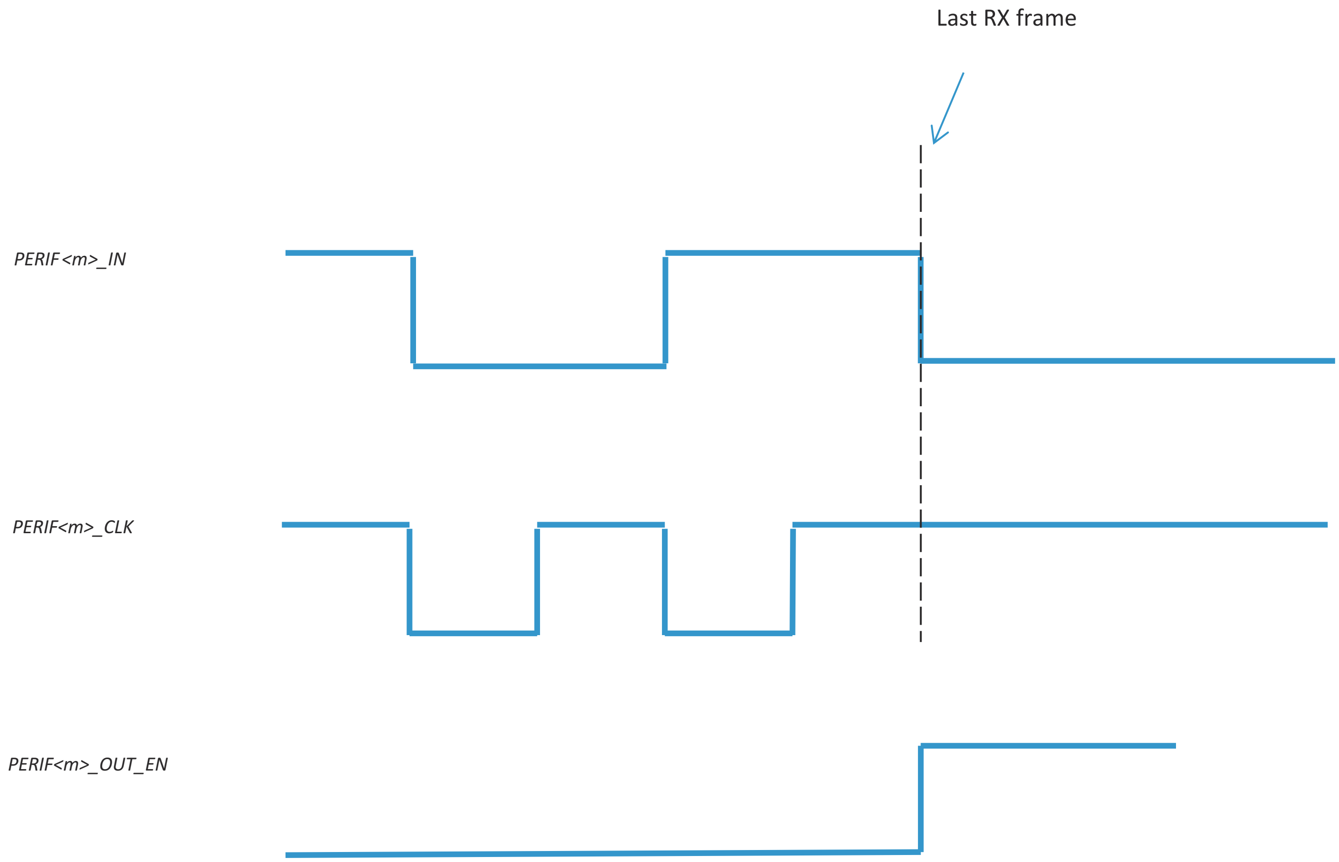

Figure 6-38. PERIF<m>_CLK Stop High on Last RX Frame

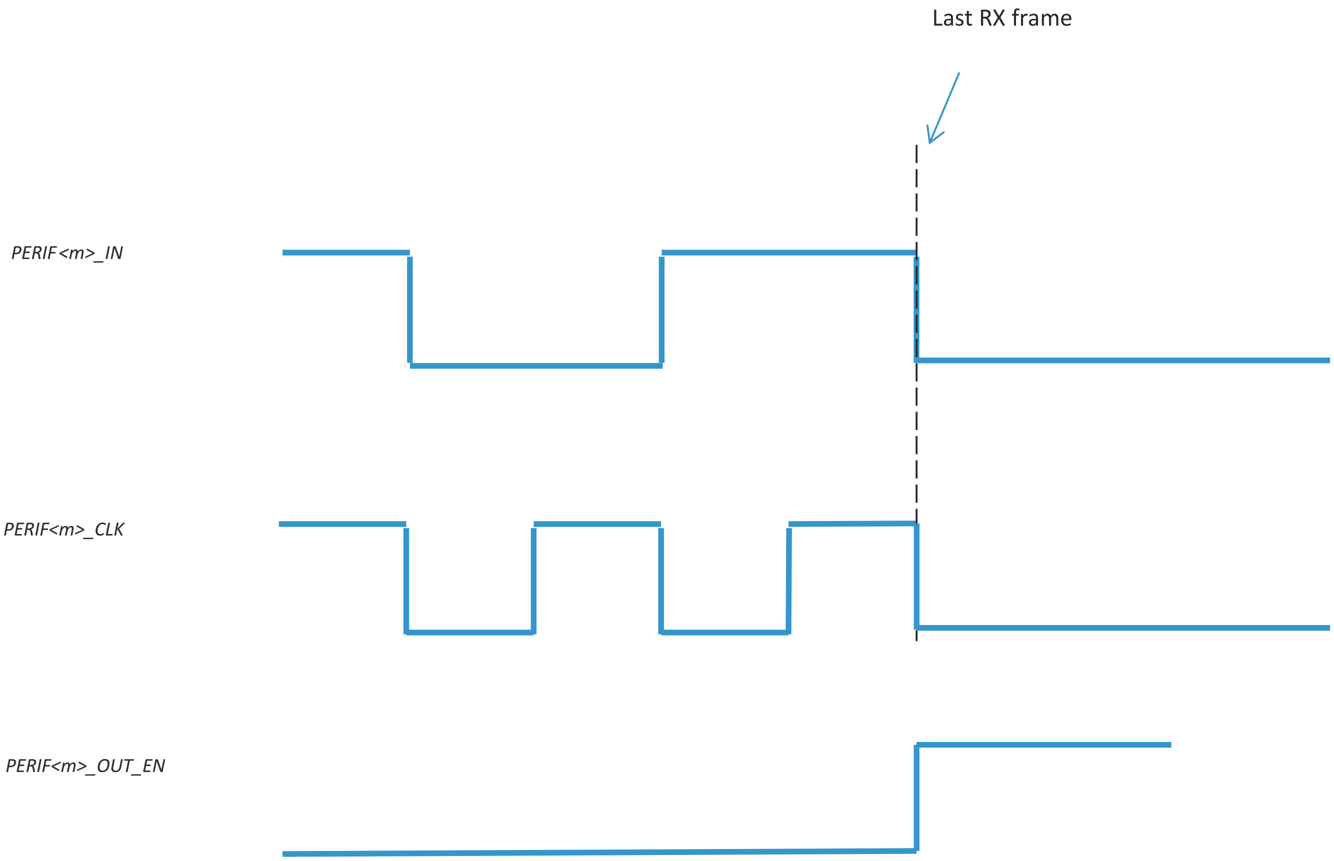

Figure 6-39. PERIF<m>_CLK Stop Low on Last RX Frame

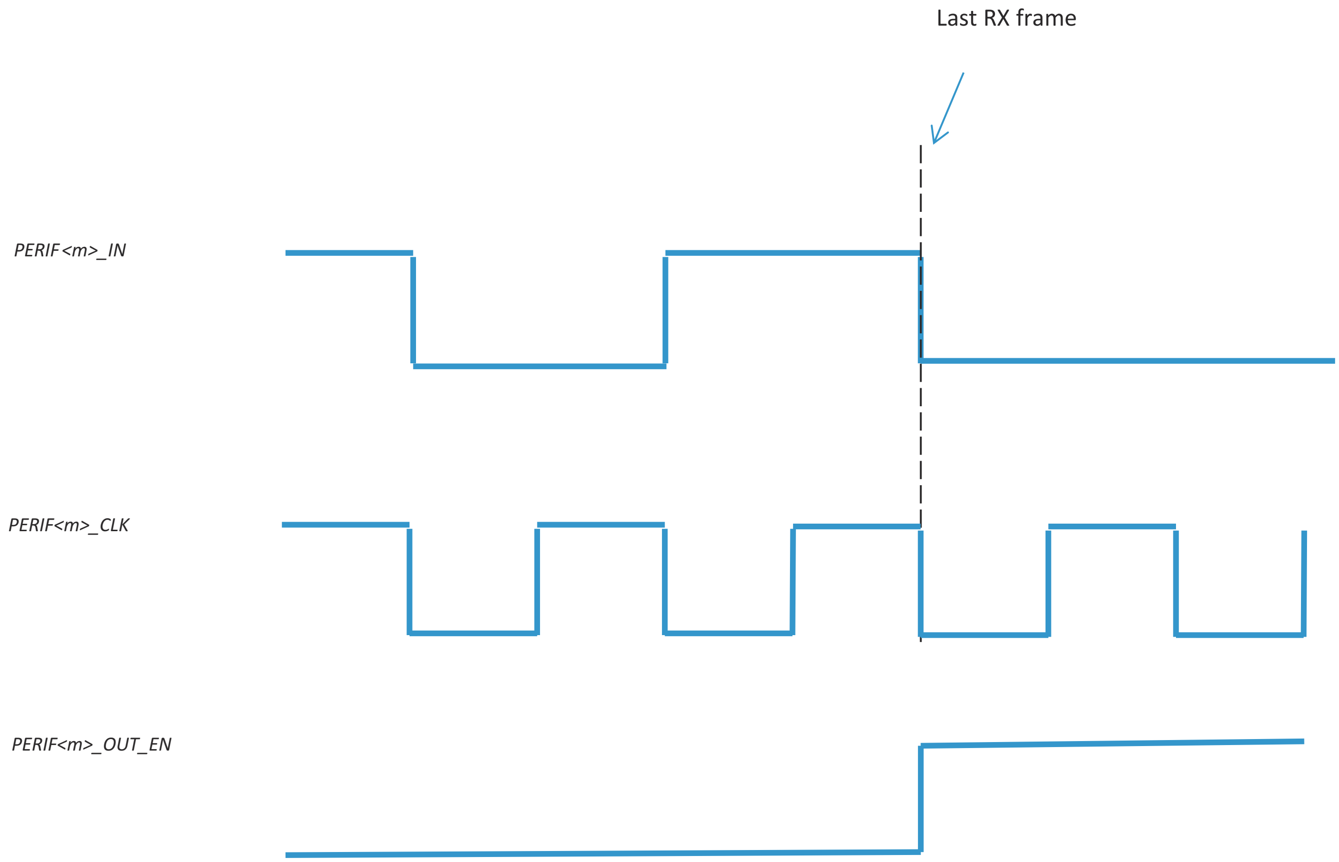

Figure 6-40. PERIF<m>_CLK Run Continuously

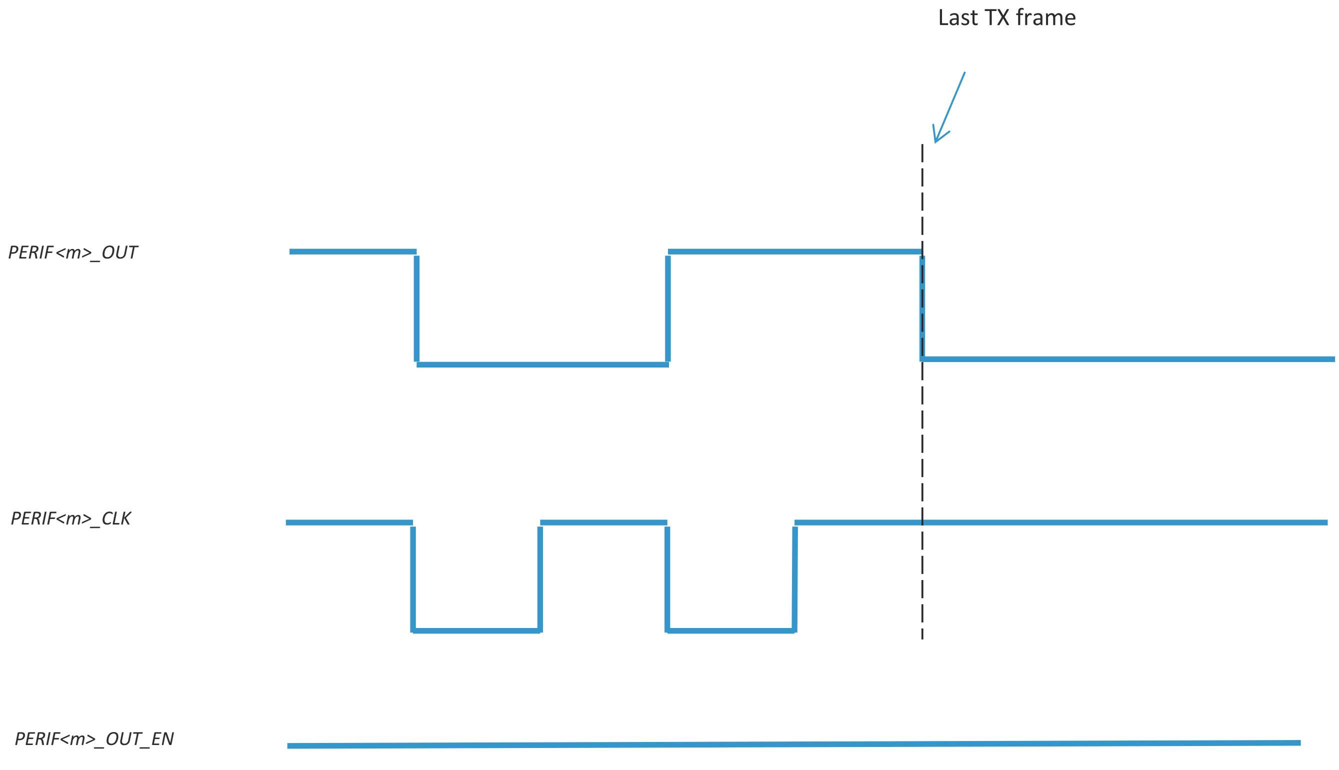

Figure 6-41. PERIF<m>_CLK Stop High on Last TX Bit

6.4.5.2.2.3.6.4 Three Peripheral Mode Basic Programming Model

The following programming models assume that the PRU is configured for 3 Peripheral Mode (ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL = 1h).

6.4.5.2.2.3.6.4.1 Clock Generation

Follow these steps to configure Peripheral I/F clocks using the HW control of the clock:

1. Select TX and RX clock sources:
    a. ICSSG_PRU0_ED_TX_CFG_REG[4] PRU0_ED_TX_CLK_SEL for the TX clock source
    b. ICSSG_PRU0_ED_RX_CFG_REG[4] PRU0_ED_RX_CLK_SEL for the RX clock source
2. Configure the 1x (TX) clock frequency:
    a. Write Division Factor to ICSSG_PRU0_ED_TX_CFG_REG[31-16] PRU0_ED_TX_DIV_FACTOR
    b. Write Fraction division factor to ICSSG_PRU0_ED_TX_CFG_REGISTER[15] PRU0_ED_TX_DIV_FACTOR_FRAC
3. Configure the oversampling (RX) frequency and oversample size:
    a. Write Division Factor to ICSSG_PRU0_ED_RX_CFG_REG[31-16] PRU0_ED_RX_DIV_FACTOR
    b. Write Fraction division factor to ICSSG_PRU0_ED_RX_CFG_REG[15] PRU0_ED_RX_DIV_FACTOR_FRAC
    c. Write RX oversample size to ICSSG_PRU0_ED_RX_CFG_REG[2-0] PRU0_ED_RX_SAMPLE_SIZE
4. Select the clk_mode to configure how the PERIF<m>_CLK signal ends after TX/RX:
    a. Write to r30[20-19] (clk_mode). Note: The clk_mode setting can also be changed per transaction.
5. Configure the wire, tst, and rx_en_counter delay values:
    a. ICSSG_PRU0_ED_CHm_CFG0_REG[10-0] PRU0_ED_TX_WDLYm for wire delay (where n = 0 or 1 and m = 0 to 2)

   b. ICSSG_PRU0_ED_CHm_CFG1_REG[15-0] PRU0_ED_TST_DELAY_COUNTERm for tst delay (where n = 0 or 1 and m = 0 to 2)
   c. ICSSG_PRUSS_ED_PRU0_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTER for auto-delay between TX and RX (where n = 0 or 1 and m = 0 to 2)

6.4.5.2.2.3.6.4.2 TX - Single Shot

Follow these steps to configure the Peripheral I/F channel(s) for a single shot transmission:

1. (Optional) Configure TX FIFO for MSB (default) or LSB:
   a. ICSSG_PRU0_ED_CHm_CFG0_REG[31] PRU0_ED_TX_FIFO_SWAP_BITSm (where n = 0 or 1 and m = 0 to 2)
2. Pre-load TX FIFO:
   a. Select TX channel by writing the desired channel number to R30[17-16] (tx_ch_sel)
   b. Write 1-4 bytes of data to r30[7-0] (tx_data). At each r30[7-0] write, data will be pushed into the FIFO.
   c. Repeat Steps 2a and 2b for all desired channels.
3. Configure TX frame size if less than 4 full bytes loaded into FIFO:
   a. ICSSG_PRU0_ED_CHm_CFG0_REG[15-11] PRU0_ED_TX_FRAME_SIZEm (where n = 0 or 1 and m = 0 to 2)
4. Push TX FIFO data to PERIF<m>_OUT (see Section 6.4.5.2.2.3.6.3.2 for the PERIF<m>_CLK and PERIF<m>_OUT start time relationship);
   a. To start TX on all channels, set r31[20] = 1 (tx_global_go).
   b. To start TX on individual channel:
      i. Select TX channel by writing the desired channel number to R30[17-16] (tx_ch_sel)
      ii. Set R31[18] = 1 (tx_channel_go)
5. If ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm > 0 (where n = 0 or 1 and m = 0 to 2), then the channel will automatically switch into RX mode. See Section 6.4.5.2.2.3.6.4.4 for an example of how to program and configure RX content.
6. If ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm = 0, poll either r31[21, 13, or 5] (tx_global_reinit_active/busy[2,1,0]) or ICSSG_PRU0_ED_TX_CFG_REG[7, 6, or 5] PRU0_ED_BUSY_m (where m = 0 to 2, indicates channel number) for when TX is complete

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Note

The PERIF<m>_CLK Peripheral I/F requires that PERIF<m>_CLK be in a high state at the beginning of a new transaction. If the clock ended the single shot transmission in low state, then the clock needs to be reset before sending more data. The steps to reset PERIF<m>_CLK are:

1. Set R31[19] = 1 (tx_global_reinit) to reset clock high
2. Wait until PRU0_ED_BUSY_m bit is cleared
3. Re-configure R30[20-19] (clk_mode), since reinit will reset the clk_mode to "Free-running/stop-high" mode

---

6.4.5.2.2.3.6.4.3 TX - Continuous FIFO Loading

Follow these steps to configure the Peripheral I/F channel(s) for a continuous loading transmission:

1. (Optional) Configure TX FIFO for MSB (default) or LSB:
   a. ICSSG_PRU0_ED_CHm_CFG0_REG[31] PRU0_ED_TX_FIFO_SWAP_BITSm
2. Pre-load TX FIFO:
   a. Select TX channel by writing the desired channel number to r30[17-16] (tx_ch_sel)
   b. Write 1-4 bytes of data to r30[7-0] (tx_data). At each r30[7-0] write, data will be pushed into the FIFO.

   c. Repeat Steps 2a and 2b for all desired channels.

3. Configure TX frame size to continuously transmit the TX FIFO until empty:
   a. Set ICSSG_PRU0_ED_CHm_CFG0_REG[15-11] PRU0_ED_TX_FRAME_SIZEm = 0h
4. Push TX FIFO data to PERIF<m>_OUT (see Section 6.4.5.2.2.3.6.3.2 for the PERIF<m>_CLK and PERIF<m>_OUT start time relationship):
   a. To start TX on all channels, set r31[20] = 1 (tx_global_go).
   b. To start TX on individual channel:
      i. Select TX channel by writing the desired channel number to r30[17-16] (tx_ch_sel)
      ii. Set r31[18] = 1 (tx_channel_go)
5. Monitor line rate and reload FIFO:
   a. Polling r31[20-18, 12-10, 4-2] (tx_fifo_sts<m>)
   b. When FIFO level is at 2 bytes, load next 2 bytes of data (see Step 2). Do not let the FIFO get close to 0. Once the FIFO runs empty, the hardware will assume the PRU has reached end of the last transmit. Any new writes to the FIFO will NOT be sent until the software sends another tx_channel_go bit. Note: There are also underrun and overrun error flags that can be monitored.
6. To end TX operation, do not send any new data to FIFO.
   a. If ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm > 0 (where n = 0 or 1 and m = 0 to 2), then the channel will automatically switch into RX mode. See Section 6.4.5.2.2.3.6.4.4 for an example of how to program and configure RX content.
   b. If ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm = 0, poll either r31[21, 13, or 5] (tx_global_reinit_active/busy[2,1,0]) or ICSSG_PRU0_ED_TX_CFG_REG[7, 6, or 5] PRU0_ED_BUSY_m (where m = 0 to 2, indicates channel number) for when TX is complete

---

Note

The PERIF<m>_CLK Peripheral I/F requires that PERIF<m>_CLK be in a high state at the beginning of a new transaction. If the clock ended the continuous loading transmission in low state, then the clock needs to be reset before sending more data. The steps to reset PERIF<m>_CLK are:

1. Set R31[19] = 1 (tx_global_reinit) to reset clock high
2. Wait until PRU0_ED_BUSY_m is cleared
3. Re-configure R30[20-19] (clk_mode), since reinit will reset the clk_mode to "Free-running/stop-high" mode

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6.4.5.2.2.3.6.4.4 RX - Auto Arm or Non-Auto Arm

Follow these steps to configure the Peripheral I/F channel(s) to receive data:

1. Configure RX and frame size:
   a. ICSSG_PRU0_ED_CHm_CFG0_REG[27-16] PRU0_ED_RX_FRAME_SIZEm (where n = 0 or 1 and m = 0 to 2)
2. Configure start bit polarity:
   a. ICSSG_PRU0_ED_RX_CFG_REG[3] RX_SB_POL (PRU0 or PRU1)
   b. For the non-auto arm use case, set r30[26, 25, 24] = 1 (rx_en<m>)
   c. For the auto arm use case, rx_en<m> will be automatically enabled at the end of a TX operation when ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm > 0 (where n = 0 or 1 and m = 0 to 2)
3. RX FIFO will start filling on the first start bit (PERIF<m>_IN = 1). The data will be captured on the positive edge of the PERIF<m>_CLK and shifted into the LSB position of the 8-bit shadow register.
4. Poll for r31[26, 25, 24] (val<m>) assertion. The valid flag will be asserted when n bits of data (determined by ICSSG_PRU0_ED_RX_CFG_REG[2-0] PRU0_ED_RX_SAMPLE_SIZE) have been collected.

5. Fetch data by reading r31[23-16, 15-8, 7-0] (rx_data_out<m>). The data will remain constant for one data frame, and PRU must read data and clear valid flag within this time. Otherwise, an overflow will occur – r31[29, 28, 27] (ovf<m>) = 1 - indicating that val<m> has been continuously asserted for longer than one data frame.
6. The clock will be stopped based on the r30[20-19] (clk_mode) configured before the start of the RX operation.
7. Clear r30[26, 25, 24] (rx_en<m>) to disable RX mode. All counters and flags will be reset.

6.4.5.3 PRU_ICSSG RAM Index Allocation

The PRU_ICSSG module includes integrated ECC Aggregator module to test ECC functionality.

Table 6-83 shows the mapping of the RAM IDs to the ECC RAMs serviced by the ECC Aggregator.

Table 6-83. Mapping of the RAM IDs to the ECC RAMs

RAM Index	ECC RAM Prefix	Description
0	pr<k>_dram0	Data RAM0 (8KB)
1	pr<k>_dram1	Data RAM1 (8KB)
2	pr<k>_pru0_iram	PRU0 Instruction Memory (12KB)
3	pr<k>_pru1_iram	PRU1 Instruction Memory (12KB)
4	pr<k>_ram	Shared Data RAM2 (64KB)
5	pr<k>_rtu0_iram	RTU0 Instruction Memory (8KB)
6	pr<k>_rtu1_iram	RTU1 Instruction Memory (8KB)
7	pr<k>_tx_pru0_iram	TX_PRU0 Instruction Memory (6KB)
8	pr<k>_tx_pru1_iram	TX_PRU1 Instruction Memory (6KB)

6.4.6 PRU_ICSSG Broadside Accelerators

6.4.6.1 PRU_ICSSG Broadside Accelerators Overview

The PRU_ICSSG supports a broadside interface, which uses the XFR (XIN, XOUT, or XCHG) instruction to transfer the contents of PRUn, RTU_PRUn or TX_PRUn (where n = 0 or 1) registers to or from accelerators. This interface enables up to 31 registers (R0-R30, or 124 bytes) to be transferred in a single instruction. This section details the various accelerators that are available to the PRUn and/or RTU_PRUn and TX_PRUn through the broadside interface.

Each of those functions have a unique XIN ID to determine which operation will occur. For more information see Table 6-60.

6.4.6.2 PRU_ICSSG Data Processing Accelerators Functional

6.4.6.2.1 PRU Multiplier with Accumulation (MPY/MAC)

This section describes the MAC (multiplier with accumulation) module integrated to PRU0/PRU1 cores, RTU_PRU0/RTU_PRU1 auxiliary cores and TX_PRU0/TX_PRU1 cores of PRU_ICSSGn (or CFG1, PRU1).

Each of the six PRU cores (PRU0/PRU1, RTU_PRU0/RTU_PRU1 auxiliary cores and TX_PRU0/TX_PRU1 transmit cores) has a designated unsigned multiplier with accumulation (MPY/MAC). The MAC supports two modes of operation: Multiply Only and Multiply and Accumulate.

The MAC is directly connected with the PRU internal registers R25-R29 and uses the broadside load/store PRU interface and XFR instructions to both control and mode of the MAC and import the multiplication results into the PRU.

The PRU MPY/MAC features are:

- Configurable Multiply Only and Multiply and Accumulate functionality via PRU register R25
- 32-bit operands with direct connection to PRU registers R28 and R29
- 64-bit result (with carry flag) with direct connection to PRU registers R26 and R27
- One clock cycle per operation
- PRU broadside interface and XFR instructions (XIN, XOUT) allow for importing multiplication results and initiating accumulate function
- Firmware can SEED the accumulator

6.4.6.2.1.1 PRU MAC Operations

6.4.6.2.1.1.1 PRU versus MAC Interface

The MAC directly connects with the PRU internal registers R25-R29 through use of the PRU broadside interface and XFR instructions. Figure 6-42 shows the functionality of each register.

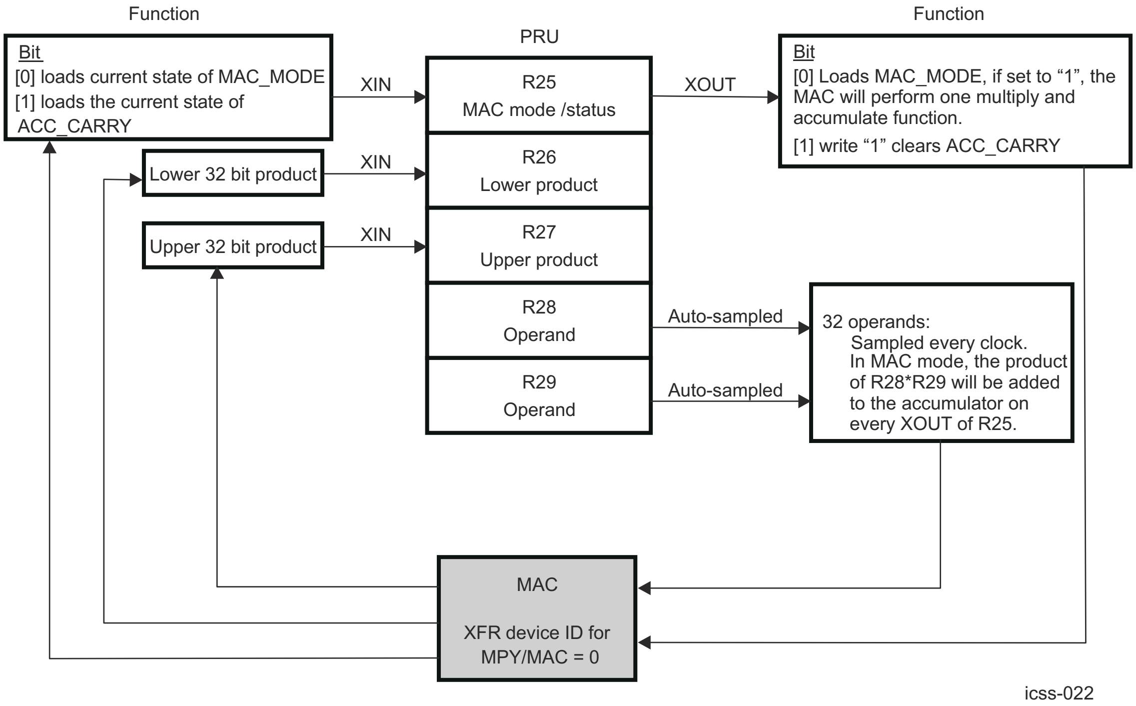

Figure 6-42. Integration of the PRU and MPY/MAC

The XFR instructions (XIN and XOUT) are used to load/store register contents between the PRU core and the MAC. These instructions define the start, size, direction of the operation, and device ID. The device ID number corresponding to the MPY/MAC is shown in Table 6-84.

Table 6-84. MPY/MAC XFR ID

Device ID	Function
0	Selects MPY/MAC

The PRU register R25 is mapped to the MAC_CTRL_STATUS register (Table 6-85). The MAC's current status (MAC_MODE and ACC_CARRY states) is loaded into R25 using the XIN command on R25. The PRU sets the MAC's mode and clears the ACC_CARRY using the XOUT command on R25.

Table 6-85. MAC_CTRL_STATUS Register (R25) Field Descriptions

Bit	Field	Description
7-2	RESERVED	Reserved
1	ACC_CARRY	Write 1 to clear. It is sticky. It is set 0 cycles after the event. 0h: 64-bit accumulator carry has not occurred 1h: 64-bit accumulator carry occurred
0	MAC_MODE	0h: Accumulation mode disabled and accumulator is cleared 1h: Accumulation mode enabled

The two 32-bit operands for the multiplication are loaded into R28 and R29. These registers have a direction connection with the MAC. Therefore, XOUT is not required to load the MAC. In multiply mode, the MAC samples these registers every clock cycle. In multiply and accumulate mode, the MAC samples these registers every XOUT R25[7-0] transaction when MAC_MODE = 1.

The product from the MAC is linked to R26 (lower 32 bits) and R27 (upper 32 bits). The product is loaded into register R26 and R27 using XIN.

6.4.6.2.1.1.2 Multiply only mode(default state), MAC_MODE = 0

The Figure 6-43 summarizes the MAC operation in "Multiply-only"mode, in which the MAC multiplies the contents of R28 and R29 on every clock cycle.

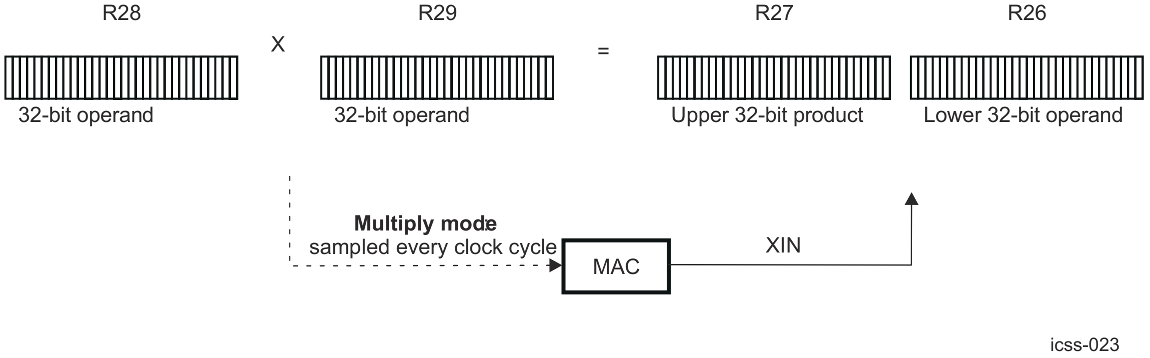

Figure 6-43. MAC Multiply-only Mode- Functional Diagram

6.4.6.2.1.1.2.1 Programming PRU MAC in "Multiply-ONLY" mode

The following steps are performed by the PRU firmware for multiply-only mode:

1. 1. Enable multiply only MAC_MODE.
    a. (a) Clear R25[0] for multiply only mode.
    b. (b) Store MAC_MODE to MAC using XOUT instruction with the following parameters:
        - Device ID = 0
        - Base register = R25
        - Size = 1
2. 2. Load operands into R28 and R29.
3. 3. Delay at least 1 PRU cycle before executing XIN in step 4.
4. 4. Load product into PRU using XIN instruction on R26, R27.

Repeat steps 2 and 4 for each new operand.

6.4.6.2.1.1.3 Multiply and Accumulate Mode, MAC_MODE = 1

The Figure 6-44 summarizes the MAC operation in "Multiply and Accumulate" mode. On every XOUT R25_REG[7-0] transaction, the MAC multiplies the contents of R28 and R29, adds the product to its accumulated result, and sets ACC_CARRY if an accumulation overflow occurs.

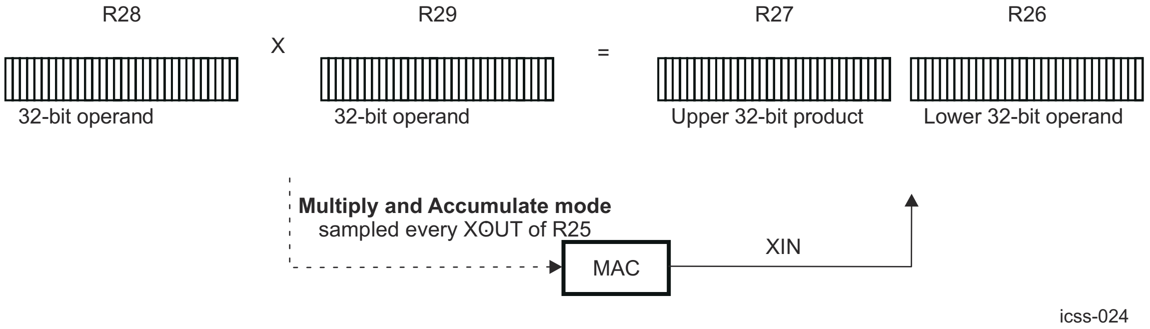

Figure 6-44. MAC Multiply and Accumulate Mode Functional Diagram

6.4.6.2.1.1.3.1 Programming PRU MAC in Multiply and Accumulate Mode

The following steps are performed by the PRU firmware for multiply and accumulate mode:

1. Enable multiply and accumulate MAC_MODE.

(a) Set R25[1-0] = 1 for accumulate mode.

(b) Store MAC_MODE to MAC using XOUT instruction with the following parameters:

- Device ID = 0

- Base register = R25

- Size = 1

2. Clear accumulator and carry flag.

(a) Set R25[1-0] = 2 to clear carry flag (R25[1]=1) and clear accumulator (R25[0]=0).

(b) Store accumulator to MAC using XOUT instruction on R25.

3. Load operands into R28 and R29.

4. Multiply and accumulate, XOUT R25[1-0] = 1

Repeat step 4 for each multiply and accumulate using same operands.

Repeat step 3 and 4 for each multiply and accumulate for new operands.

5. Load the accumulated product into R26, R27, and the ACC_CARRY status into R25 using the XIN instruction.

1.

Firmware can load/seed the accumulator by doing XOUT of R27:R26. This will also clear the carry flag.

Note

Steps one and two are required to set the accumulator mode and clear the accumulator and carry flag.

6.4.6.2.2 PRU CRC16/32 Module

Each of the PRU0/PRU1 cores, RTU_PRU0/RTU_PRU1 auxiliary cores and TX_PRU0/TX_PRU1 transmit cores have a designated CRC16/32 module.

In general, CRC adds error detection capability to communication systems. The CRC encoder appends redundant bits (or CRC bits) to the systematic data message. During reception of the data message, the received data is also encoded with the same CRC encoder. The 2 sets of CRC bits are compared together. If they match, there were no transmission errors; and if they don't match, a transmission error has been detected.

CRC16/32 supports the following features:

- Supports CRC32:
  - $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$
- Supports CRC16:
  - $x^{16}+x^{15}+x^{2}+1$
- Supports CRC16 - CCITT:
  - $x^{16}+x^{12}+x^{5}+1$
- PRU broadside interface and XFR instructions (XIN, XOUT) allow for importing CRC results and executing accumulate function

6.4.6.2.2.1 PRU and CRC16/32 Interface

The CRC16/32 module directly connects with the PRU internal registers R25-R29 through use of the PRU broadside interface and XFR instructions. Table 6-86 shows the functionality of each register.

The XFR instructions (XIN/XOUT/XCHG) are used to load/store register contents between the PRU core and the CRC16/32 module. These instructions define the start, size, direction of the operation, and device ID. The XFR device ID number corresponding to the CRC16/32 module is 1.

Table 6-86. CRC Register to PRU Port Mapping

CRC Register	R/W	Description	PRU Mapping
CRC_CFG	W	Always write all 4 bytes. bit [0] CRC32_ENABLE: 0: CRC16 mode is selected. Hardware will auto-set init state of CRC_SEED to 0000_0000h. However, for CRC16-CCITT software will need to write the init state of FFFF_FFFFh to CRC_SEED. Note: The CRC16 result value is only 16-bits. 1: CRC32 mode is selected. Hardware will auto-set init state of CRC_SEED will be FFFF_FFFFh. bit [1] CRC_32B_NOT_EMPTY: 0: CRC 32Byte buffer is empty 1: CRC 32Byte buffer is not empty bit [2] CRC16_MOD_ENABLE: 0: CRC16 ($x^{16}+x^{15}+x^{2}+1$) 1: CRC16-CCITT ($x^{16}+x^{12}+x^{5}+1$) - Note: CRC32_ENABLE field must = 0.	R25

CRC_DATA_8_BFLIP	R	8-bit flip of CRC_SEED. CRC_DATA_8_BFLIP has the same byte order as CRC_SEED[31-0], but each byte has all bits flipped.
		CRC_DATA_8_FLIP[7-0] = CRC_SEED[0-7]
		CRC_DATA_8_FLIP[15-8] = CRC_SEED[8-15]
		CRC_DATA_8_FLIP[23-16] = CRC_SEED[16-23]
		CRC_DATA_8_FLIP[31-24] = CRC_SEED[24-31]
		For CRC16, only CRC_DATA_8_BFLIP[15-0] are valid. No auto reset on CRC_DATA_8_BFLIP read.
		Example code:
		`; bit reversal widget - data is in r28 mov r28, r2`
		`xout 1,&r28,4 xin 1,&r27,4 ; bytes wise bit reversal`
		`xin 1,&r28,4 ; 32 bit wide bit reversal`
			R27

Table 6-86. CRC Register to PRU Port Mapping (continued)

CRC Register	R/W	Description	PRU Mapping
CRC_SEED	W	CRC SEED value. Hardware will auto-initialize the CRC_SEED value to 0000_0000h for CRC16 and FFFF_FFFFh for CRC32. Software only needs to initialize CRC_SEED if a different default value is required. For CRC16-CCITT, software needs to update initial CRC_SEED value to FFFF_FFFFh. Always write 4 bytes. Note: Reading the CRC_DATA register will reset the CRC value to the CRC_SEED state.	R28
CRC_DATA_32_BFLIP	R	Full 32-bit flip of CRC_DATA CRC_DATA_32_BFLIP[0] = CRC_DATA[31] … CRC_DATA_32_BFLIP[31] = CRC_DATA[0] For CRC16, only CRC_DATA_32_BFLIP[31-16] are valid. No auto reset on CRC_DATA_32_BFLIP read.	R28
CRC_DATA	RW	For Write, must use a fixed width throughout the session. The CRC module supports lower 8-bit, or lower 16-bit, or full 32-bit data widths. For Read, LSB or CRC_DATA[0] is first bit on the wire. For Read, reset the CRC_DATA back to CRC_SEED state. Note: Firmware must add 1 to 2 NOPs after the last XOUT to the XIN. For CRC16, only CRC_DATA[15-0] is valid.	R29

6.4.6.2.2.2 CRC Programming Model

The following steps are performed by the PRU firmware to use the CRC module:

Step1: Configuration (optional)

1. Configure CRC type:
   For CRC32 operation, set CRC32_ENABLE using XOUT instruction with the following parameters:
   - Device ID = 1
   - Base register = R25
   - Size = 1
2. Update CRC_SEED, if required using XOUT with the following parameters:
   - Device ID = 1
   - Base register = R28
   - Size = 1 to 4

Step 2:

1. Load new CRC data into R29
2. Push CRC data to the CRC16/32 module using XOUT with the following parameters:
   - Device ID = 1
   - Base register = R29
   - Size = 1 to 4
3. 1 or 2 NOPS
4. Load the accumulated CRC result into the PRU using the XIN instruction with the following parameters:
   - Device ID = 1
   - Base register = R29
   - Size = 4

Repeat Step 2, numbers 1 and 2 for each new CRC data.

Note

When a session starts, the PRU firmware must use the same write data width throughout the session.

6.4.6.2.2.3 PRU and CRC16/32 Interface (R9:R2)

The PRU_ICSSG system implements a new wide 32-Bytes data path. The firmware can perform one XOUT of 32-Bytes, the hardware will feed the CRC16/32 4-Bytes at a time. This will take 20 clock cycles for CRC16 and 12 clock cycles for CRC32 for a 32-Bytes XOUT.

Table 6-87. PRU Register to XFR Mapping

PRU Register	XFR ID	Domain/Function	Description
R9:R2 Data	1	Data	XOUT Only 1-Byte to 32-Bytes in size LSB packed and no gaps, for example: 32-Bytes push R9:R2 16-Bytes push R5:R2 4-Bytes push R2 7-Bytes push R3(b2.b0):R2 1-Bytes push R2(b0)

6.4.6.2.3 PRU_ICSSG Scratch Pad Memory

The PRU_ICSSG supports a scratch pad with up to four independent banks accessible by the PRU cores and two independent banks accessible by the RTU_PRU cores. The TX_PRU cores have a separate scratch pad memory with two independent banks. The PRU, RTU_PRU and TX_PRU cores interact with the scratch pad through broadside load/store PRU interface and XFR instructions. The scratch pad can be used as a temporary place holder for the register contents of the PRU, RTU_PRU or TX_PRU cores.

6.4.6.2.3.1 PRU0/1 Scratch Pad Overview

The PRU_ICSSG scratch pad supports the following features:

- PRU0 and PRU1 cores have three Scratch Pad banks of 30, 32-bit registers (R29 to R0)
- RTU_PRU0 and RTU_PRU1 auxiliary cores have three Scratch Pad banks of 30, 32-bit registers (R29 to R0)
- TX_PRU0 transmit core has one Scratch Pad bank of 30, 32-bit registers (R29 to R0)
- TX_PRU1 transmit core has one Scratch Pad bank of 30, 32-bit registers (R29 to R0)
- Flexible load/store options:
  - Load/store one byte of R<n> or load/store (R29 to R0) to Bank0, Bank1, Bank2 or Bank3
  - User-defined start byte and length of the transfer
  - Length of transfer ranges from one byte of a register to the entire register content (R29 to R0)
  - Simultaneous transaction supported between PRU0 <-> Bank<n> and PRU1 <-> Bank<m>
- XFR (XIN/XOUT/XCHG) instructions operate in one clock cycle
- Optional XIN/XOUT shift functionality allows remapping of registers (R<n> -> R<m>) during load store operation

Figure 6-45 shows a simplified model of the Scratch Pad and PRU cores integration.

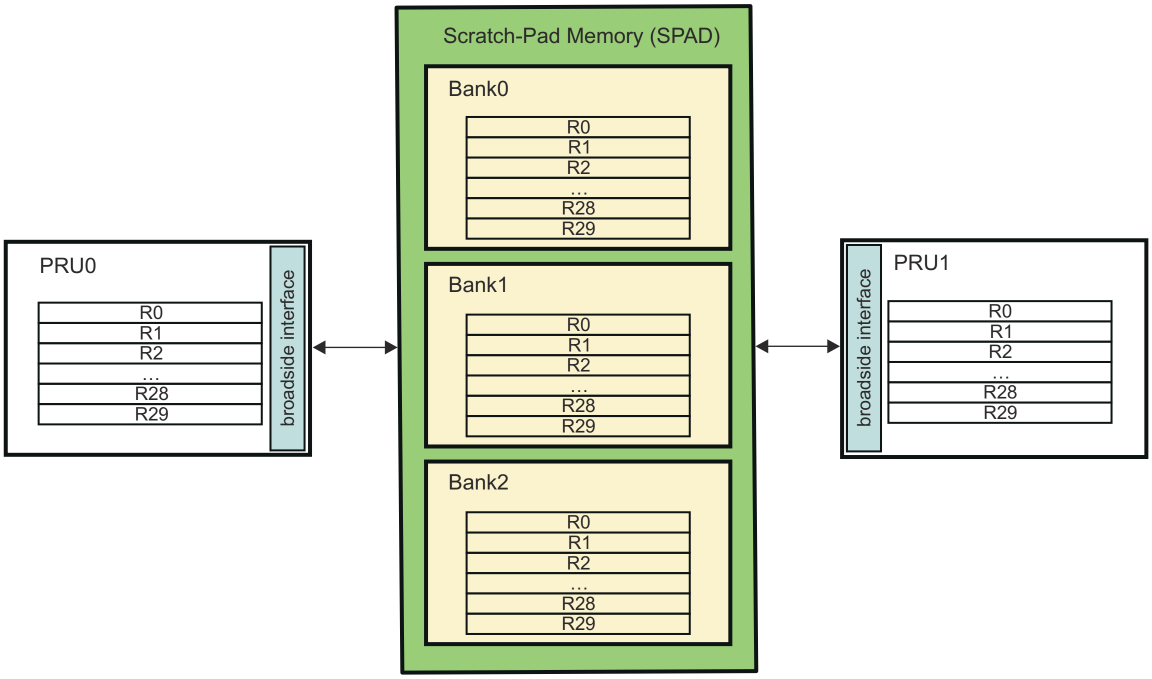

icss-025

Figure 6-45. Scratch Pad and PRU Integration

Figure 6-46 shows a simplified model of the Scratch Pad and RTU_PRU cores integration.

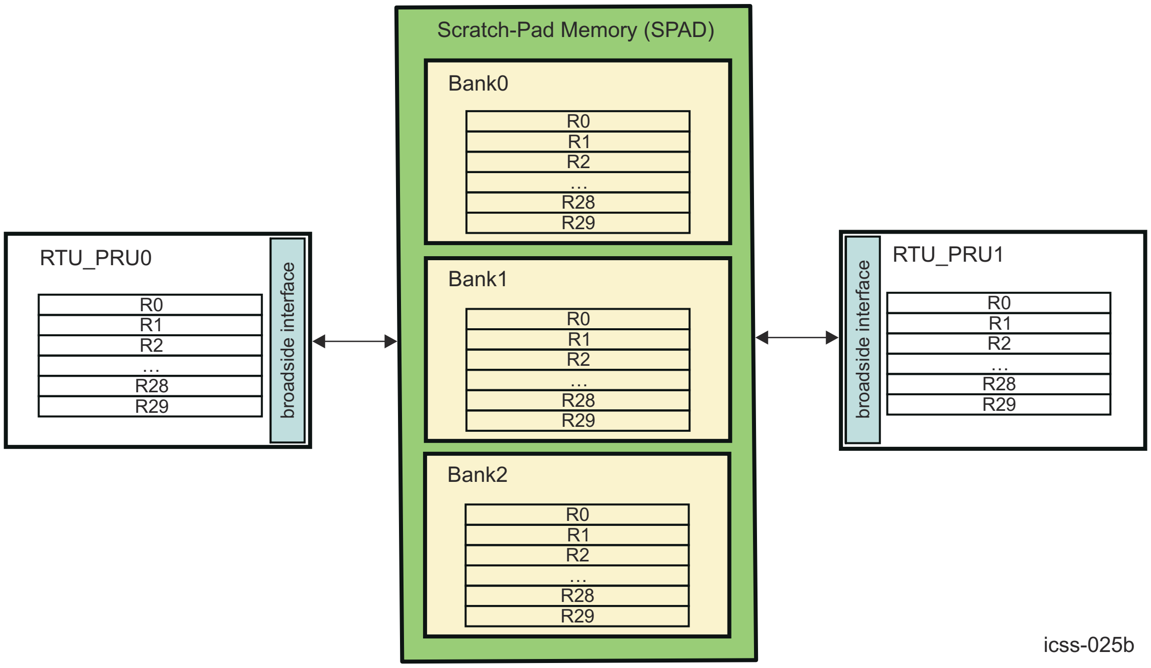

Figure 6-46. Scratch Pad and RTU_PRU Integration

Figure 6-47 shows a simplified model of the Scratch Pad and TX_PRU cores integration.

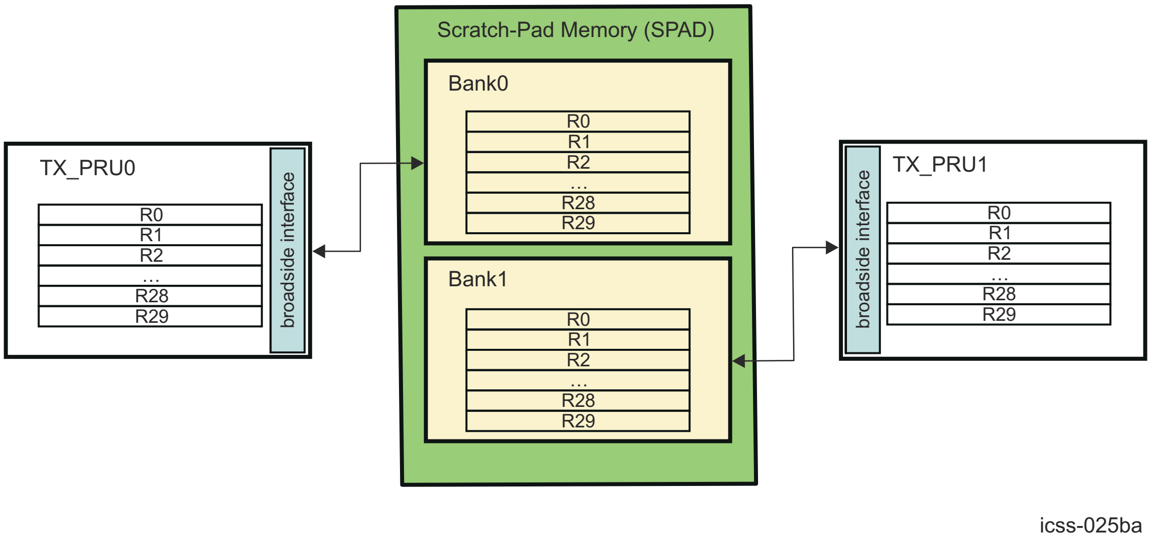

Figure 6-47. Scratch Pad and TX_PRU Integration

6.4.6.2.3.2 PRU0 /1 Scratch Pad Operations

XFR instructions are used to load/store register contents between the PRU cores and the scratch pad banks. These instructions define the start, size, direction of the operation, and device ID. The device ID corresponds to the external source or destination (either a scratch pad bank or the other PRU core). The device ID numbers are shown in Table 6-88.

Table 6-88. Scratch Pad XFR ID

Device ID	Function/Operation
10	Selects Bank0
11	Selects Bank1

Table 6-88. Scratch Pad XFR ID (continued)

Device ID	Function/Operation
12	Selects Bank2

A collision occurs when two XOUT commands simultaneously access the same asset or device ID. Table 6-89 shows the priority assigned to each operation when a collision occurs.

Table 6-89. Scratch Pad XFR Collision and Stall Conditions

Operation	Collision and Stall Handling
PRU<n> XOUT (->) bank[j]	If both PRU cores access the same bank simultaneously, PRU0 is given priority. PRU1 will temporarily stall until the PRU0 operation completes.
RTU_PRU<n> XOUT (->) bank[i]	If both RTU_PRU cores access the same bank simultaneously, RTU_PRU0 is given priority. RTU_PRU1 will temporarily stall until the RTU_PRU0 operation completes.

6.4.6.2.3.2.1 Optional XIN/XOUT Shift

The optional XIN/XOUT shift functionality allows register contents to be remapped or shifted within the destination’s register space. For example, the contents of PRU0 R6-R8 could be remapped to Bank1 R10-12.

The shift feature is enabled or disabled through the PRU subsystem level register ICSSG_SPP_REG[1] XFR_SHIFT_EN bit. When enabled, R0[4-0] (internal to the PRU) defines the number of 32-bit registers in which content is shifted in the scratch pad bank. Note that scratch pad banks do not have registers R30 or R31.

6.4.6.2.3.2.2 Scratch Pad Operations Examples

The following PRU firmware examples demonstrate the shift functionality. Note: These assume the XFR_SHIFT_EN bit of the ICSSG_SPP_REG register of the PRU_ICSSG CFG register space has been set.

XOUT Shift By 4 Registers

Store R4:R7 to R8:R11 in Bank0:

- Load 4 into R0.b0
- XOUT using the following parameters:
  - Device ID = 10
  - Base register = R4
  - Size = 16

XOUT Shift By 9 Registers, With Wrap Around

Store R25:R29 to R4:R9 in Bank1:

- Load 9 into R0.b0
- XOUT using the following parameters:
  - Device ID = 11
  - Base register = R25
  - Size = 20

XIN Shift By 10 Registers

Load R14:R16 from Bank2 to R4:R6:

- Load 10 into R0.b0
- XIN using the following parameters:
  - Device ID = 12
  - Base register = R4
  - Size = 12

6.4.6.2.4 PRU_ICSSG IPC Scratch Pad Memory

The IPC module is a 32 Byte wide Scratch Pad that connects together PRUn and RTU_PRUn (where n = 0 or 1) cores within a Slice. Figure 6-48 represents the mapping between IPC Scratch Pad (IPC SPAD), PRUn and RTU_PRUn cores..

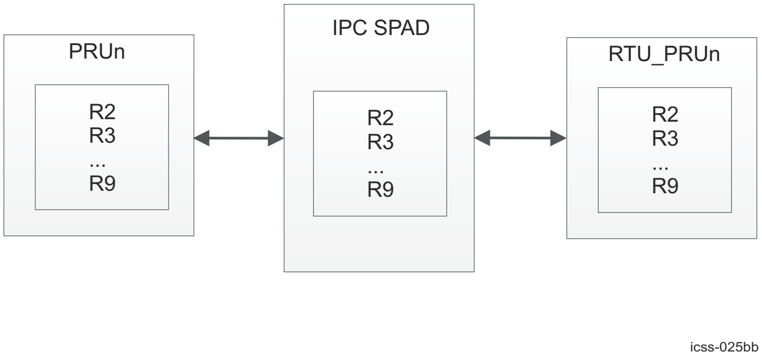

Figure 6-48. Integration of the PRU and IPC Scratch Pad

The firmware needs to define which bytes are owned by each of the PRUn/RTU_PRUn cores. There is no hardware arbitration.

Table 6-90. IPC Scratch Pad XFR ID

Register	Device ID	Domain/ Function	Description
R9:R2 Data	15	IPC[255:0]	32 byte wide register bank

6.4.6.2.5 PRU_ICSSG Broadside (BS) RAM

Each PRU core, RTU_PRU core, and TX_PRU core has a dedicated 2KB Broadside (BS) RAM, which is attached to the core (PRU0, PRU1, RTU_PRU0, RTU_PRU1, TX_PRU0, TX_PRU1).

The BS RAM directly connects with the PRU internal register R2-R10 through use of the PRU broadside interface and XFR instructions. Figure 6-49 shows the functionality of each register.

There are two modes of operation for the PRU to interact with the BS RAM:

1. BS RAM only (shown in Figure 6-49)
2. BS RAM + SUM32 snoop (described in Section 6.4.6.2.6)

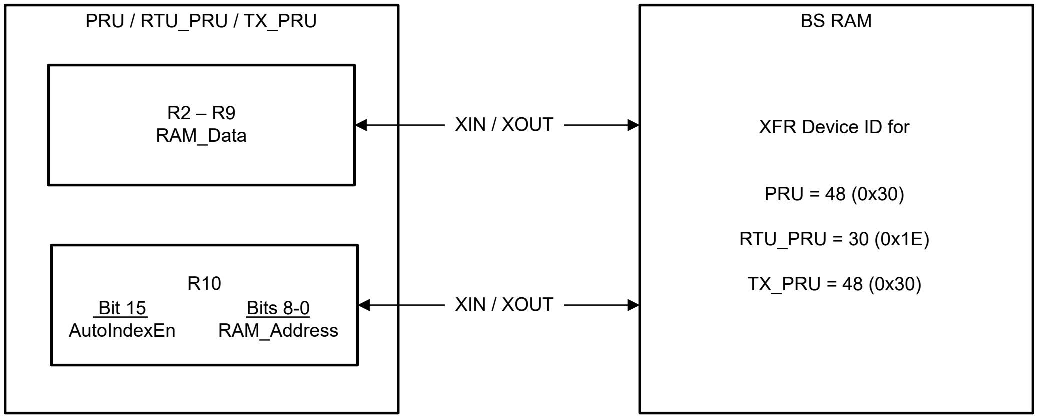

Figure 6-49. Integration of the PRU and BS RAM

The XFR instructions (XIN and XOUT) are used to load/store register contents between the PRU/ RTU_PRU core and the BS RAM. These instructions define the start, size, direction of the operation, and device ID. The device ID number corresponding to the BS RAM is shown in Table 6-91.

Table 6-91. BS RAM XFR ID

	Device ID	Function
BS RAM only mode The following IDs can be used to read/write the following registers to the BS RAM: • RAM Data (R2:R9) • AutoIndexEn and BS_RAM_Address (R10) Note that R10 must be treated as a 2 byte write.	48 (30h) 48 (30h) 30 (1Eh)	PRU TX_PRU RTU_PRU
BS RAM + SUM32 snoop mode The following IDs can be used to write (only) the following registers to the BS RAM and SUM32 module. This mode requires a 32 Byte write. • RAM Data (R2:R9)	49 (31h) 38 (26h)	PRU RTU_PRU

A description of the PRU register R10's functionality is shown in Table 6-92. Note that the firmware must do a 2 byte write of R10[15:0] when transmitting the content of this register to the BS RAM.

Table 6-92. Register (R10) Field Descriptions

Bit	Field	Description
15	AutoIndexEn	RAM Auto Increment the Index Enable 0h: Disable Auto Increment 1h: Enable Auto Increment When enabled, each PRU or RTU_PRU core's write or read to the BS RAM will cause the RAM_Address to increment by 1. Note: Each increment of the RAM_Address is the equivalent of 32 Bytes. The next read or write address will always be 32 Bytes later, regardless of the read or write data size. Rollovers of RAM_Address are not supported. Firmware must reset RAM_Address to zero. This mode must be set before RAM Data transaction.
8-0	RAM_Address	Index for PRU core Read/Write access of the RAM. Index is direct mapping to the 16KB RAM. Note: Max width is 256-bits or 32Bytes. 0h: 1st 32 Bytes 1h: 2nd 32 Bytes Note: For reading data, can be executed XOUT RAM_Address, XIN RAM_Data

6.4.6.2.5.1 Programming the BS RAM

The following steps are performed by the PRU firmware to write to the BS RAM:

1. Configure RAM_Address and AutoIndexEn
    a. Load RAM_Address and AutoIndexEn into R10
    b. Store RAM_Address and AutoIndexEn to BS RAM using XOUT instruction with the following parameters:

        - Device ID = 30h (PRU) or 1Eh (RTU_PRU)

        - Base register = R10

        - Size = 2

2. Write Data to BS RAM
    a. Load Data to be written into R2-R9
    b. Store Data to BS RAM using XOUT instruction with the following parameters:

        - Device ID = See Table 6-91, ID depends on mode.

        - Base register = Register with start of data (R2-R10)

        - Size = Data size (number of bytes)

3. If AutoIndexEn = 1h, repeat Step 2 to write additional data.
4. If AutoIndexEn = 0h,
    a. Load new address into R10
    b. Repeat Step 1b
    c. Repeat Step 2

The following steps are performed by the PRU firmware to read to the BS RAM:

1. Configure RAM_Address and AutoIndexEn
    a. Load RAM_Address and AutoIndexEn into R10
    b. Store RAM_Address and AutoIndexEn to BS RAM using XOUT instruction with the following parameters:

        - Device ID = 30h (PRU) or 1Eh (RTU_PRU)

        - Base register = R10

    - Size = 2

2. Read Data from BS RAM
    a. Load Data to be written into R2-R9
    b. Load Data to PRU/ RTU_PRU BS RAM using XIN instruction with the following parameters:

        - Device ID = See Table 6-91, ID depends on mode.

        - Base register = Register destination for start of data (R2-R10)

        - Size = Data size (number of bytes)

3. If AutoIndexEn = 1h, repeat Step 2 to read additional data.
4. If AutoIndexEn = 0,
    a. Load new address into R10
    b. Repeat Step 1b
    c. Repeat Step 2

6.4.6.2.6 PRU_ICSSG SUM32 Hardware Accelerator

The SUM32 module is a simple hardware accelerator which is used to help generate UDP checksum (User Datagram Protocol) for data integrity. The operation takes 2 clock cycles, read pipe is another 1 clock cycle. The operation is pipelined. The PRUn or RTU_PRUn core (where n = 0 or 1) will not see any hardware backpressure for back to back XOUT 32 Byte operations. The PRU or RTU_PRU core can see up to 2 cycle stall if there is no time between the last XOUT and the XIN to get the SUM value. The FW must insure you have 3 NOPs or 3 clock cycle delay between the last XOUT to the XIN to get the correct SUM value. The XIN operation self clears the SUM.

Figure 6-50 shows the SUM32 module integration. Each PRUn core (where n = 0 or 1) has a dedicated SUM32 module, used to snoop or continuously monitor the Broadside (BS) RAM and facilitate software to detect a UDP Checksum error. There are also two SUM32 modules attached to each auxiliary PRU core (RTU_PRU0 and RTU_PRU1).

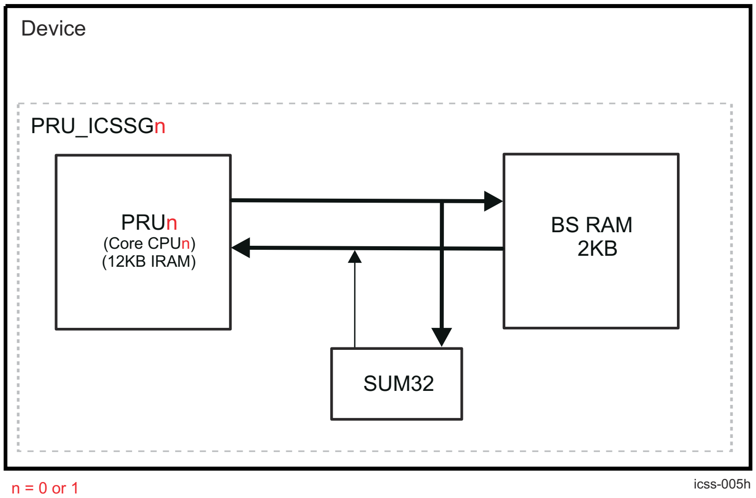

Figure 6-50. SUM32 Integration

Note that there are two modes of operation for the PRU to interact with the SUM32:

1. BS RAM + SUM32 snoop
2. SUM32 only

The Device ID for each mode is shown in Table 6-93. An XOUT with the BS RAM + XOUT SUM32 snoop Device ID will write the data to the Broadside (BS) RAM and the SUM32 at the same time. An XOUT with the SUM32 only Device ID will write the data only to SUM32. An XIN with either mode's Device ID will read the SUM32 value.

Table 6-93. SUM32 XFR ID

Mode	Device ID	PRU/ PRU_RTU core
XOUT (write) data to SUM32		
BS RAM + SUM32 snoop	49 (31h)	PRU
	38 (26h)	RTU_PRU
SUM32 only	47 (2Fh)	PRU
	39 (27h)	RTU_PRU
XIN (read) sum result		
	02 (2h)	Both PRU & RTU_PRU

The SUM32 directly connects with the PRU internal register R2-R10 and R29 through use of the PRU broadside interface and XFR instructions. Figure 6-51 and Table 6-94 shows the functionality of each register.

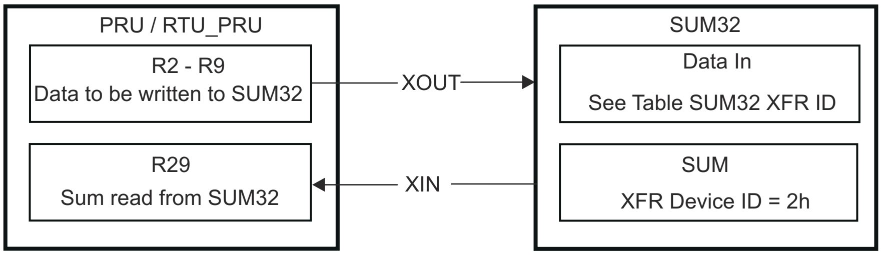

Figure 6-51. Integration of the PRU and SUM32 (Register View)

Table 6-94. Register (R2-R9, R29) Descriptions

Register	Function	Description
R2 – R9	Data	Write only. Always write 32 Bytes for SUM32 XFR IDs.
R29	Sum	Read only. Always read 4 Bytes. This will get the current 32-bit SUM value. The read event will self-clear the SUM.

6.4.6.2.7 PRU_ICSSG Byte Swap (BSWAP)

The Byte Swap (BSWAP) module enables any of the internal PRU registers (R0 to R29) to swap byte order in 1 clock cycle via XIN function.

This module supports three functions:

1. Byte Order Swap function, flipping the byte order within a given register
2. 4_8 function, swapping the contents of R2-R5 <-> R6-R9
3. 4_16 function, swapping the contents of R2-R5 <-> R14-R17 and R6-R9 <-> R10-R13

Each of those functions have a unique XIN ID to determine which operation will occur, as shown in Table 6-95.

Table 6-95. BSWAP XFR ID

Device ID[1]	Function	Access
160 (A0h)	Byte Order Swap	XIN
161 (A1h)	4_8	XIN
162 (A2h)	4_16	XIN

(1) Note: All PRU and RTU cores (PRU0, PRU1, RTU_PRU0, and RTU_PRU1 cores) have the same XFR ID mapping.

Note

The following sections use the syntax “Rn.bm.” This syntax is used to represent a byte field within the internal PRU register, Rn. For example, b0 represents “byte 0” (or bits 0-7) and b3 represents “byte 3” (or bits 24- 31) of a given register.

6.4.6.2.7.1 Byte Order Swap Function

The PRU core internal registers (R0 to R29) byte order will get flipped within each register. This is used by firmware to convert Little-Endian to Big-Endian or Big-Endian to Little-Endian. As shown in Table 6-95, this function corresponds to the XFR Device ID of A0h.

Within each Rn register after XIN instruction execution, the following will happen.

- Rn.b3 = Rn.b0
- Rn.b2 = Rn.b1
- Rn.b1 = Rn.b2
- Rn.b0 = Rn.b3

Example 1: XIN start of R2.b0 and 8 Bytes in length:

- R2.b3 = R2.b0
- R2.b2 = R2.b1
- R2.b1 = R2.b2
- R2.b0 = R2.b3
- R3.b3 = R3.b0
- R3.b2 = R3.b1
- R3.b1 = R3.b2
- R3.b0 = R3.b3

Example 2: XIN start of R2.b0 and 1 Byte in length:

- R2.b0 = R2.b3

Example 3: XIN start of R2.b0 and 2 bytes in length:

- R2.b0 = R2.b3
- R2.b1 = R2.b2

6.4.6.2.7.2 4_8 Function

The 4_8 function swaps the contents of R2-R5 <-> R6-R9. This function operates on the XIN instruction and must start at R2.b0 and cannot exceed R9. As shown in Table 6-95, this function corresponds to the XFR Device ID of A1h.

After XIN instruction execution, the following will happen.

- R2 = R6
- R3 = R7
- R4 = R8
- R5 = R9
- R6 = R2
- R7 = R3
- R8 = R4
- R9 = R5

6.4.6.2.7.3 4_16 Function

The 4_16 function swaps the contents of R2-R5 <-> R14-R17 and R6-R9 <-> R10-R13. This function operates on the XIN instruction and must start at R2.b0 and cannot exceed R17. As shown in Table 6-95, this function corresponds to the XFR Device ID of A2h.

After XIN instruction execution, the following will happen.

- R2 = R14
- R3 = R15
- R4 = R16
- R5 = R17
- R6 = R10
- R7 = R11
- R8 = R12
- R9 = R13
- R10 = R6
- R11 = R7
- R12 = R8
- R13 = R9
- R14 = R2
- R15 = R3
- R16 = R4
- R17 = R5

6.4.6.2.8 PRU_ICSSG Task Manager

The PRU_ICSSG system integrates 6 Task Managers used for efficient switching between tasks.

There is one dedicated task manager for each PRU, RTU and TX_PRU core (PRU0/ PRU1, RTU_PRU0/ RTU_PRU1 and TX_PRU0/ TX_PRU1 cores), which are described in the subsequent sections. Each task manager works independently from the others.

Figure 6-52 shows a block diagram of the Task Manager modules and the associated PRU0/ PRU1 (Core CPU0 and CPU1), RTU_PRU0/RTU_PRU1 (Aux CPU0 and Aux CPU1) cores and TX_PRU0/ TX_PRU1 (Transmit CPU0 and CPU1) cores.

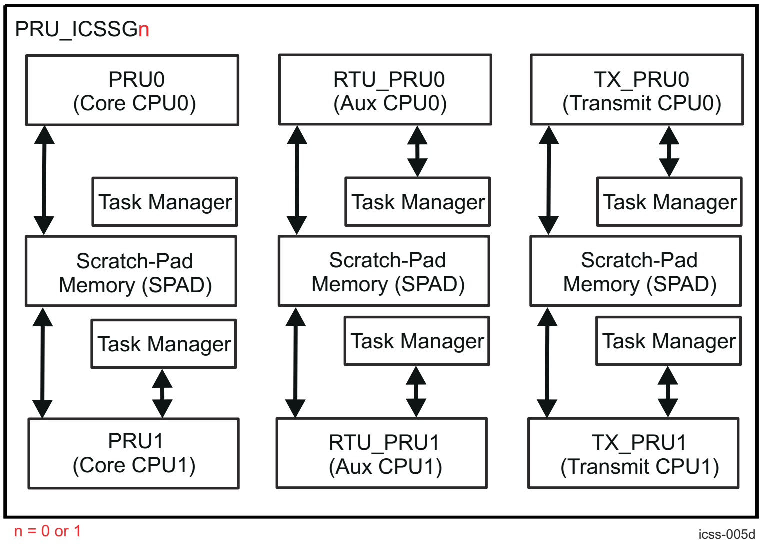

Figure 6-52. Task Manager Block Diagram

The Task Manager has two modes of operation:

- General purpose mode
- RX_TX mode

6.4.6.2.8.1 Task Manager General Purpose Mode

The General purpose mode is used to improve the firmware efficiency and performance. This feature enables software to get preempted to do another higher priority task.

It achieves this by preempting the current execution with a new hardware feature inside the PRU that causes the PRU to execute the XCHG instruction. The Task Manager will issue this hardware preemption and respond to the XCHG instruction by saving off the current program counter and ALU flags and providing a new program counter (PC) to start a new task. See section Section 6.4.6.2.8.1.2 for more details about hardware context switching. When the firmware completes this new task, it will terminate this task by issuing a XIN instruction. When the Task Manager sees this execution of the XIN instruction, it will return the state of the PRU from the last saved off task.

The General Purpose mode is enabled by the ICSSG_GLOBAL_CFG[1-0] TASKS_MGR_MODE register and is responsible for:

- Saving off the program counter (PC) and flags when switching a task
- Providing a new program counter for a new task
- Restoring the original program counter when the firmware yields

The General Purpose Task manager supports the following features:

- Software can enable/disable hardware preemption
- Allows up to 2 suspended tasks (Task0 and Task1) and 1 active task

6.4.6.2.8.1.1 Tasks and Sub-tasks

The General Purpose mode supports 3 tasks - Task0 (default, or background, task), Task1, and Task2. Figure 6-53 shows the basic state machine associated with these tasks.

Task2 has highest priority, Task1 has middle priority, and Task0 has lowest priority. As such, a Task2 event always preempts Task1 or Task0, if either is active. A Task1 event always preempts Task0, if active. To exit out of the current state or task, software must issue a “software completion of task” using XIN and a device ID of 252.

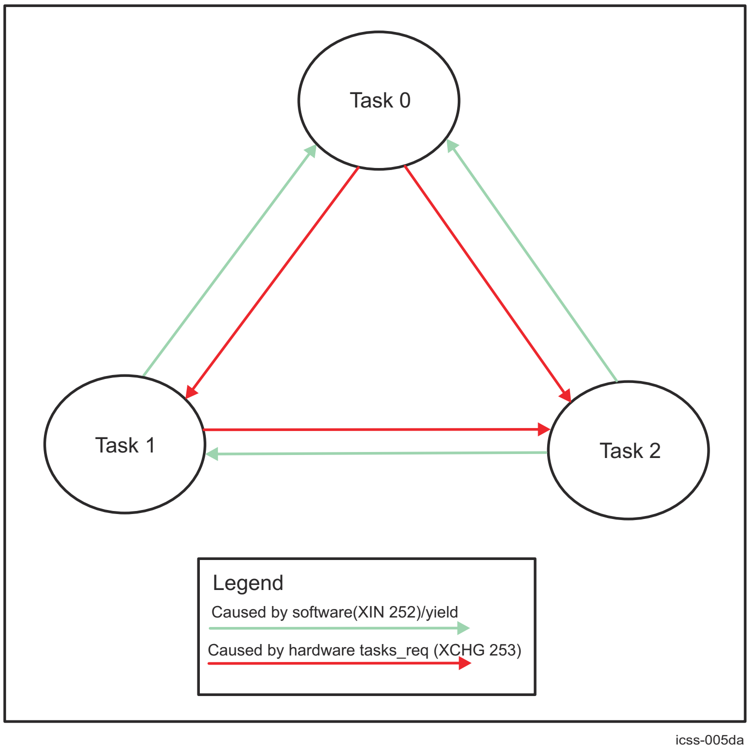

Figure 6-53. High Level Finite State Machine

Task2 and Task1 support up to five sub-tasks (S0-S4), which are enabled or disabled in the ICSSG_GLOBAL_CFG register. Figure 6-54 and Figure 6-55 show the state machines for entering into these sub-tasks, and the priority of these sub-tasks are as follows:

- Task2 sub-tasks order of priority is: T2_S0 (highest priority) -> T2_S1 -> T2_S2 -> T2_S3 -> T2_S4 (lowest priority).
- Task1 sub-tasks order of priority is: T1_S1 (highest priority) -> T1_S2 -> T1_S3 -> T1_S4 -> T1_S0 (lowest priority).

Note that the subtasks can only be preempted by a higher priority task. However, they cannot be preempted by another subtask within the same task. For example, T1_S4 can be preempted by T2_S3. However, T1_S4 cannot be preempted by T1_S3.

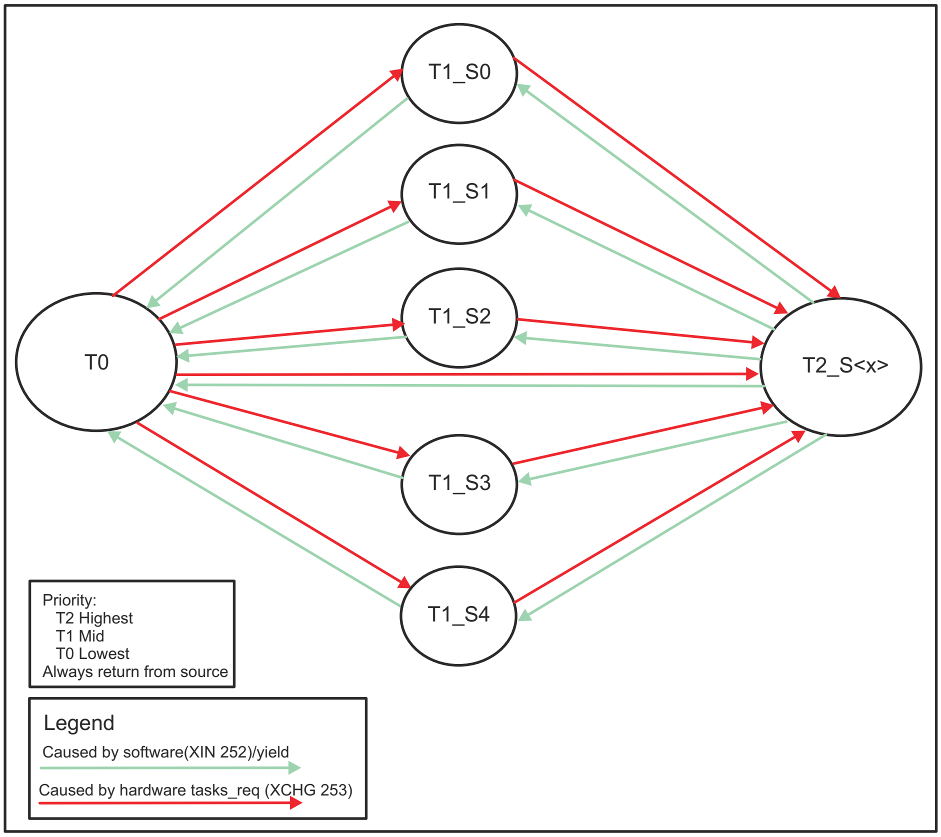

Figure 6-54. Task 1 Finite State Machine

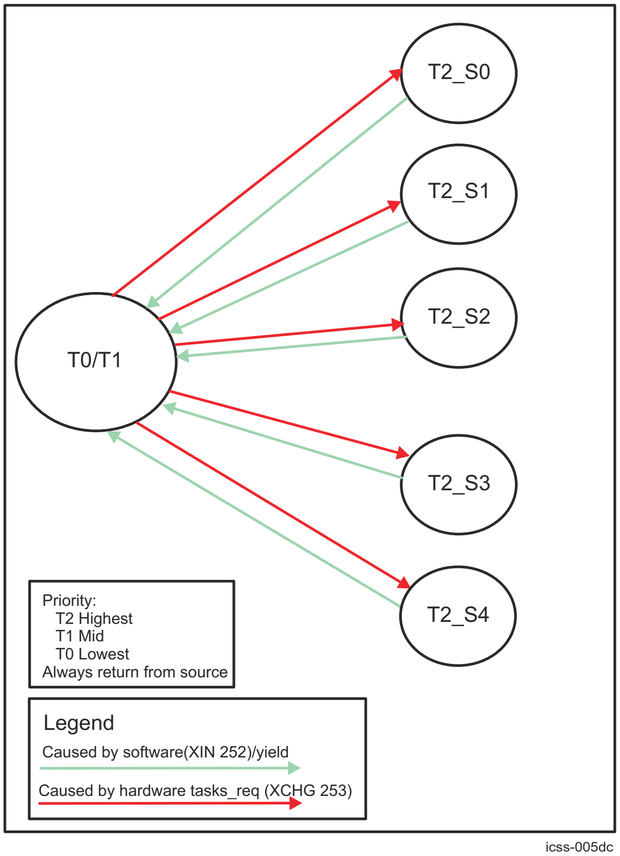

Figure 6-55. Task 2 Finite State Machine

In general purpose mode, the source event for each sub-task is ICSSG_TS1_GEN_CFG1/ ICSSG_TS1_GEN_CFG2 and ICSSG_TS2_GEN_CFG1/ ICSSG_TS2_GEN_CFG2 registers defines the source of the event which will trigger the Task1 and Task2 sub-tasks.

Table 6-96 shows the mapping.

Note

All source events should be cleared before any update to the mapping.

Table 6-96. Task to Event Mapping

ICSSG_TS1_GEN_CFG1/ ICSSG_TS1_GEN_CFG2 and ICSSG_TS2_GEN_CFG1/ ICSSG_TS2_GEN_CFG2	Source Event
0	RX_SOF
1	RX_BK1
2	RX_BK2
3	RX_BKN
4	RX_EOF
5	1h
6	TX_L1_L2_WM
7	TX_L2_EMPTY & TX_L2_EOF_PEND
8	TX_UNDER_RX_OVER_ERR
9	PR1_MDIO_LINKINT[0] (from MDIO)
10	PR1_MDIO_LINKINT[1] (from MDIO)

Table 6-96. Task to Event Mapping (continued)

ICSSG_TS1_GEN_CFG1/ ICSSG_TS1_GEN_CFG2 and ICSSG_TS2_GEN_CFG1/ ICSSG_TS2_GEN_CFG2	Source Event
11	PR1_EDC0_SYNC0_OUT
12	PR1_EDC0_SYNC1_OUT
13	PR1_EDC1_SYNC0_OUT
14	PR1_EDC1_SYNC1_OUT
15	1h
31-16	IEP0_CMP[15:0]
37-32	IEP0_CAPR[5:0]
39-38	IEP0_CAPRF[1:0]
55-40	IEP1_CMP[15:0]
61-56	IEP1_CAPR[5:0]
63-62	IEP1_CAPRF[1:0]
127-64	SPINLOCK_FEED_REQ[63:0](1)
135-128	INTC_HOST_OUT[7:0]
143-136	INTC_HOST_TASKMGR_REQ[7:0]
145-144	RTU_PDSP_INTR_IN[1:0] (2)
147-146	PR1_PDSP_INTR_IN[1:0]
148	xfr_vbus_rd_data_rx0_req (data rdy)
149	xfr_vbus_rd_data_rx1_req (data rdy)
150	xfr_vbus_rd_data_rx2_req (data rdy)
151	(tx_l2_empty & (tx_l1_occ[6:0] == (tx_wm_lvl + 7'b1))) | (tx_l2_empty & (tx_l1_occ[6:0] < (tx_wm_lvl + 7'b1)) & tx_l1_eof_pend)
255-148	Reserved

(1) SPINLOCK_FEED_REQ[63:0] is from the spinlock module. It will assert for 1 clock cycle when the clock goes from a 1 to 0, or freed.

(2) PDSP in source event names is equivalent to the PRU processor names.

6.4.6.2.8.1.2 Task Manager Hardware Context Switching

When switching between tasks, the Task Manager only saves and restores the program counter (PC) and flags, as shown in Figure 6-56. The firmware is responsible for saving and restoring any Rn internal registers that it will override during a task. The SPAD, Data RAM, or Shared RAM (Data RAM2) can be used to store the Rn register value.

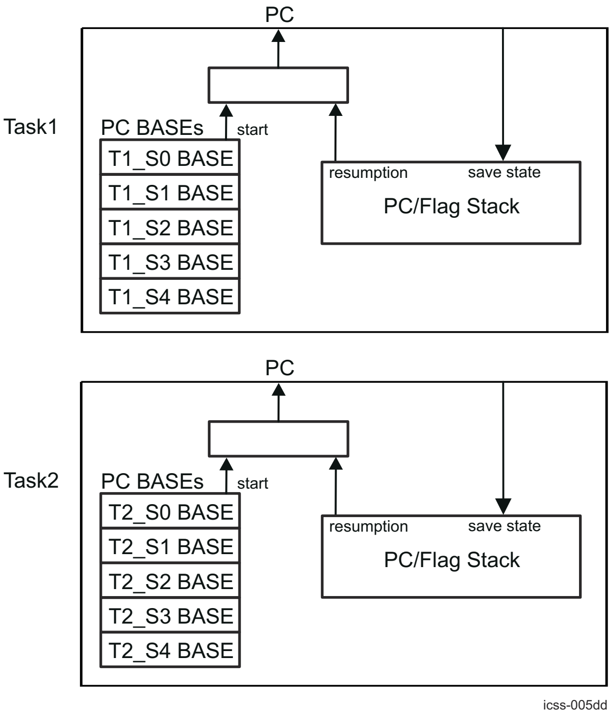

Figure 6-56. Hardware Context Switching Block Diagram

6.4.6.2.8.1.3 Task Manager Programming Guide

Figure 6-57 shows the basic programming steps within a given task or sub-task.

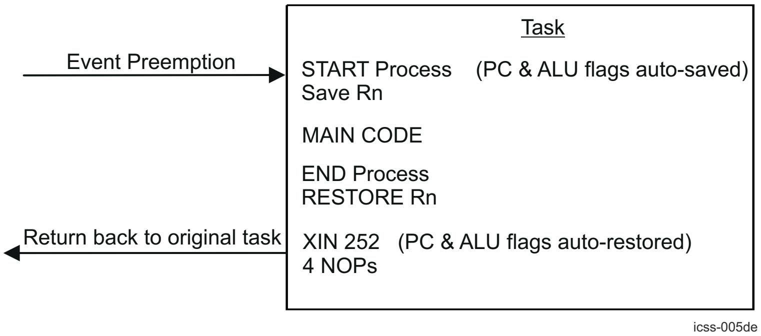

Figure 6-57. Task Programming

Note

The SAVE and RESTORE process can be preempted. It will resume at the next instruction after the higher priority task yields. To avoid preemption, the ICSSG_GLOBAL_CFG[TSm_ENn] bitfield (where m = 1 or 2 and n = 0 to 4) can be used to disable (and re-enable) preemption.

6.4.6.2.8.2 Task Manager RX_TX Mode

The RX_TX mode can be used for Ethernet use cases to improve the firmware efficiency and performance. This mode is enabled by the ICSSG_GLOBAL_CFG[1-0] TASKS_MGR_MODE register. In general, the RX_TX mode is similar to the General Purpose mode. Therefore, this section only covers the differences between General Purpose mode and RX_TX mode.

The RX_TX Task manager is responsible for:

- Preempting a lower priority task and providing a new program counter (PC)
- Storing the current program counter (PC) and flags
- Restoring the saved program counter (PC) and flags when the firmware yields
- Tracking the state of background, RX and TX states

6.4.6.2.8.2.1 RX_TX Task Manager Features

Task Manager features:

- Software can enable/disable RX or TX preemption or both
- Software can observe the state of task manager
- Software can read the time spent in the 3 domains
- Allows up to 2 suspended tasks (Background and RX) and 1 active task

6.4.6.2.8.2.2 Tasks and Sub-tasks

Unlike the General Purpose mode, the Task1 and Task2 sub-states in RX_TX mode have pre-defined source events, listed in Table 6-97.

Table 6-97. Task to Event Mapping

Sub-tasks	Source Event
Task1	
T1_S0	RX_SOF
T1_S1	Programmable size threshold, ranging from 1 Byte to 32 Bytes (ICSSG_RX_CFG[4-0] BK1_SIZE)
T1_S2	Programmable size threshold, ranging from 1 Byte to 32 Bytes (ICSSG_RX_CFG[9-5] BK2_SIZE)
T1_S3	Every 32 Bytes (ICSSG_RX_CFG[14-10] BKN_SIZE)
T1_S4	RX_EOF
Task2	
T2_S0	TX Enable based on IEP CMP SOF and TX Express Type is true
T2_S1	TX Enable based on IEP CMP SOF and TX Express Type is false
T2_S2	TX L2 FIFO WATER MARK event
T2_S3	TX_EOF
T2_S4	RX_TX_ERROR (either RX_L1_UNDERRUN or TX_L1_OVERRUN)

Note

The sub-task priorities are the same as General Purpose mode. For Task1, T1_S1 (highest priority) -> T1_S2 -> T1_S3 -> T1_S4 -> T1_S0 (lowest priority). T1_S0 is the lowest priority to prevent a RX_SOF starting before RX_EOF starts in the case RX_EOF is late. For Task2, T2_S0 (highest priority) -> T2_S1 -> T2_S2 -> T2_S3 -> T2_S4 (lowest priority).

The size threshold is a hardware dependency that must be met in order to switch to a given state. The size is based on the number of bytes that got pushed into the RX L2 FIFO. For example, assume T1_S1 and T1_S2 are both set to 16 Bytes. The task manager will issue a hardware preemption for T1_S1 after the first 16 Bytes got pushed into the RX L2 FIFO. The task manager will issue a hardware preemption for T1_S2 after the second 16 Bytes got pushed into the RX L2 FIFO. The task manager will issue a hardware preemption for T1_S3 after another 32 Bytes got pushed into the RX L2 FIFO. Note the task manager will continue to issue a new hardware preemption for T1_S3 for each new 32 Bytes block of data until a T1_S4 event occurs.

6.4.6.2.9 PRU_ICSSG Spinlock

Each PRU_ICSSG subsystems includes Spinlock controller/target interfaces to allow fast signaling and resource sharing within and between PRU_ICSSG subsystems.

Supported Features:

- 64 ownership flags (shared by SLICE0 and SLICE1 within an PRU_ICSSG subsystem) with support of 14 initiators, including:
  - 6 Internal PRU cores:
    - PRU0/1, RTU_PRU0/1 and TX_PRU0/1 cores
    - 2 clock cycle response of Spinlock status
  - 2 External Host register access:
    - Each with a separate address space (ICSSG_SPIN_LOCK0 and ICSSG_SPIN_LOCK1)
    - Enables 2 controllers: Host and DMA
  - 6 External PRU cores:
    - One External PRU_ICSSG with 6 PRU cores
    - With flexible external pipeline for SoC timing closer
    - Allows the sharing of flags across PRU_ICSSG systms
    - 4 to 6 clock cycle response
- Fixed arbitration
- Flag selection through ICSSG_SPIN_LOCK0/1[13-8] MMR_OWN_REQ_VECTOR_0/1 bit field:
  - PRU, RTU_PRU and TX_PRU cores use R1.b0 register, which is snooped or continually monitored by the Spinlock. XOUT of this register is not required. XIN of R1.b0 causes arbitration action.
  - Each Host uses one 32-bit addressable space
    - Vector write (through ICSSG_SPIN_LOCK0/1[13-8] MMR_OWN_REQ_VECTOR_0/1) or status read (through ICSSG_SPIN_LOCK0/1[0] MMR_OWN_REQ_STATUS_0/1) will cause arbitration action

6.4.6.2.9.1 PRU0/1 and RTU_PRU0/1 Spinlock Interface

Note: All PRU and RTU cores (PRU0, PRU1, RTU_PRU0, and RTU_PRU1 cores) have the same mapping.

Table 6-98. PRU registers to Spinlock Mapping

PRU Register	BS ID	Access	Type	HW port	Description
Internal/External					
R1.b0[5-0]	NA	NA Always exported	Flag selection	own_req_vector[5:0] input	Defines which flag to arbitrate
Internal					
R1.b3[0]	INT_SPIN_ID 0x90	XIN	Flag status and arbitration	own_req select control input own_req_status status output	own_req input will assert during this XIN transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status 0h: not owned/lost 1h: owned/won
R1.b0	INT_SPIN_ID 0x90	XOUT	Flag clear	own_req_clr control input	own_req_clr input will assert during the XOUT R1.b3 transaction. This assertion will clear the flag selected by R1.b0/ own_req_vector
External0					
R1.b3[0]	EXT_SPIN_ID0 0x91	XOUT	Flag status and arbitration		own_req input will assert during this XOUT transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status: 0h: not owned/lost 1h: owned/won **NOTE: Firmware must have 8 NOP before XIN after XOUT.**

Table 6-98. PRU registers to Spinlock Mapping (continued)

PRU Register	BS ID	Access	Type	HW port	Description
R1.b3[0]	EXT_SPIN_ID0 0x91	XIN	Flag status and arbitration	own_req_status status output	own_req input will assert during this XIN transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status: 0h: not owned/lost 1h: owned/won
R1.b0	EXT_SPIN_ID0 0x91	XOUT	Flag clear	own_req_clr control input	own_req_clr input will assert during the XOUT R1.b1 transaction. This assertion will clear the flag selected by R1.b0/ own_req_vector
External1					
R1.b3[0]	EXT_SPIN_ID1 0x92	XOUT	Flag status and arbitration		own_req input will assert during this XOUT transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status: 0h: not owned/lost 1h: owned/won **NOTE: Firmware must have 8 NOP before XIN after XOUT.**
R1.b3[0]	EXT_SPIN_ID1 0x92	XIN	Flag status and arbitration	own_req select control input own_req_status status output	own_req input will assert during this XIN transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status: 0h: not owned/lost 1h: owned/won **NOTE: Firmware must have 8 NOP before XIN after XOUT.**
R1.b0	EXT_SPIN_ID1 0x92	XOUT	Flag clear	own_req_clr control input	own_req_clr input will assert during the XOUT R1.b1 transaction. This assertion will clear the flag selected by R1.b0/ own_req_vector

6.4.6.2.10 PRU_ICSSG Filter Data Base (FDB)

The Filter Data Base (FDB) block performs hardware lookup and provides the port mapping to firmware. It operates on ingress of the 2 RX physical ports and 1 RX host port.

The Filtering Database (FDB) is used to help ensure efficient usage of a Bridged LAN's resources by only forwarding received frames to those LAN segments on which they need to be. To this end, the FDB aggregates information used to make filtering and forwarding decisions for received MAC frames. The information may be statically or dynamically configured via control plane protocols, or dynamically learned based on observed traffic. Conceptually, the FDB is queried upon reception of each potentially forwarded frame, and the FDB provides the Forwarding Process with a set of potential transmission ports.

FDB Supported Features:

- Optional VLAN -> FID hardware Lookup Table (LUT)
  - Configurable SMEM base address for VLAN to FID mapping
- Optional HSR_SEQ support when VLAN is disabled
- 256-bit 16KB broadside FDB hardware Lookup Table (LUT)
  - Configurable hash with index size (64, 128, 256, 512, 1024, 2048)
  - Configurable bucket sizes (2, 4, 8)
  - Auto hardware start/lookup for RX Port 0/RX Port 1
  - Software start/lookup for RX Host Port
  - General purpose mode, 16Byte compare operation in 1 clock cycle
  - Either PRU core (PRU0/ PRU1) can access the FDB block, but only one needs to own it; spinlock is required for XOUT
- The FDB block supports 3 modes of operation:
  - Generic broadside RAM (256-bit). Each PRU has its own address index.
  - FDB LUT mode:
    - Both PRU cores can access the Lookup Table (LUT)
  - General purpose mode, 16Byte compare (Always active)
- 2 physical banks of RAM, and each bank has 8KB memory size
  - One of the RAM's can operate in FDB LUT mode and the other in Generic broadside RAM/16Byte compare mode

Not Supported Features:

- Bucket size of 1

Figure 6-58 shows a high-level view of the FDB module.

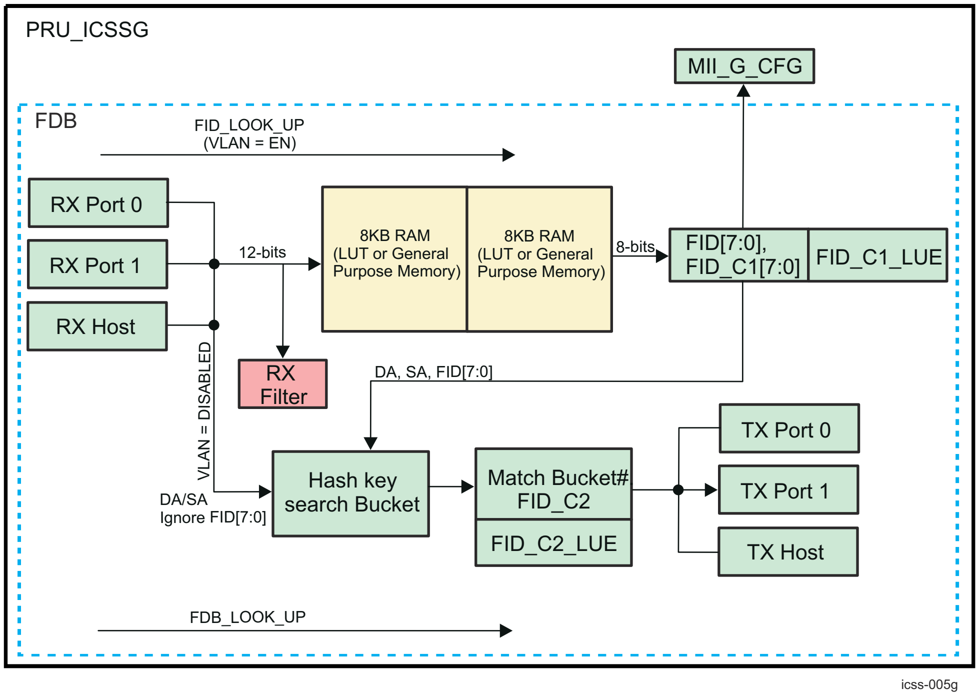

Figure 6-58. PRU_ICSSG FDB Block Diagram

PRU0 or PRU1 cores only can access the FDB RAM's. RTU_PRU0 or RTU_PRU1 auxiliary cores only gets the result of FDB lookup to its broadside access.

6.4.6.2.10.1 FDB Modes of operation

Each RAM bank of the FDB module supports 2 modes of operation:

- FDB LUT mode
- Generic broadside RAM (256-bit wide) and General purpose compare mode (16Byte compare)

The FDB block consist of 2 physical banks of RAM, each of 8KB size. The PRU core will always have the ability to read/write the broadside RAM in FDB LUT mode. If FDB LUT mode is disabled then 8KB of the broadside RAM will operate in Generic mode and General purpose compare mode. Table 6-99 shows the valid mode configurations for each FDB physical bank.

Table 6-99. Valid configurations of modes

Config1	FDB Bank0: FDB LUT mode enabled FDB Bank1: FDB LUT mode enabled	The FDB LUT uses the full 16KB memory for the operation. PRU core will write to the RAM entry to learn if the packet miss
Config2	FDB Bank0: FDB LUT mode enabled FDB Bank1: FDB LUT mode disabled	The FDB LUT uses the first bank only (Bank0), or 8KB of memory The second memory bank (Bank1) is disabled for LUT operation. Bank1 is used for general purpose compare mode.
Config3	FDB Bank0: FDB LUT mode disabled FDB Bank1: FDB LUT mode disabled	Bank0 and Bank1 are 16KB RAM and it is used in general purpose compare mode. No FDB LUT events.

Note

In all configurations only one of the PRU cores (PRU0 or PRU1) can access the FDB RAM. It is not legal to have PRU0 access at the same time when PRU1 core access the FDB RAM. This is valid for all modes of operation.

6.4.6.2.10.1.1 FDB LUT: Hardware operation (HSR Disabled: MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 0h)

The software needs to configure the FDB mode of operation.

If VLAN is enabled through MII_G_RT_FDB_GEN_CFG2[6] FDB_VLAN_EN bit, then first hardware LUT is to translate VLAN_ID[11-0] to FID[7-0] by calling the FID_LOOK_UP process. If VLAN is disabled, then first hardware LUT is to FDB_LOOK_UP.

6.4.6.2.10.1.2 FDB LUT: Hardware operation (HSR Enabled: MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 1h)

The user needs to configure the FDB mode of operation and set FDB_GEN_CFG2[5] FDB_HSR_EN = 1h bit.

Note

DA Lookup does not support HSR_SEQ. Only SA Lookup supports HSR_SEQ compare.

6.4.6.2.10.1.3 8KB/16KB Generic broadside RAM mode of operation

When FDB0/FDB1 LUT mode is disabled, then Generic 8KB/16KB broadside RAM mode is enabled. Both memory banks (Bank0 and Bank1) are used in this mode of operation. Either PRU core (PRU0 or PRU1) can access Bank0 or Bank1 via the FDB_Data/FDB_Address. RTU_PRU0 and RTU_PRU1 auxiliary cores only have access to the results of the lookup. The auxiliary cores (RTU_PRU0 and RTU_PRU1) can not write or read to the FDB memory banks.

6.4.6.2.10.1.3.1 Broadside (BS) Mapping

Table 6-100. Broadside (BS) Mapping

Register	XFR ID	Desc	Notes
R9:R2 (32 Bytes)	30/0x1E, PRUx	FDB_Data	No access restriction. 1 Byte upto 32 Byte access
R5:R2 (16 Bytes)	31/0x1F, PRUx	General Pattern	No access restriction. 1 Byte upto 16 Byte access
R10	30/0x1E, PRUx	AutoIndexEn, FDB_Address	Must do 2 byte R10[15:0]. Write Address rollover not supported
R12:R10	32/0x20, PRUx, RTUx	Port0_Result	No access restriction
R12:R10	33/0x21, PRUx, RTUx	Port1_Result	No access restriction
R12:R10	34/0x22, PRUx, RTUx	Host_Result	No access restriction
R10	35/0x23, PRUx	General_Results	No access restriction

Table 6-101. Broadside (BS) FDB_Data mapping with shift of zero

Local	Item
R2	FDB0_0
R3	FDB0_1
R4	FDB1_0
R5	FDB1_1

FDB Structure - HSR Disabled:
(MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 0h)
FDB = {FDB_1, FDB_0}
FDB_0 = {DA_SA3, DA_SA2, DA_SA1, DA_SA0}
FDB_1 = {FID_C2, FID, DA_SA5, DA_SA4}

FDB Structure - HSR Enabled:
(MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 1h)
FDB = {FDB_1, FDB_0}
FDB_0 = {DA_SA3, DA_SA2, DA_SA1, DA_SA0}
FDB_1 = {HSR_SEQ, DA_SA5, DA_SA4}

Note

Only SA Lookup supports HSR_SEQ compare.

Table 6-102. FDB Indexing

FDB RAM Address	Content	Bucket Size 2#	Bucket Size 4#	Bucket Size 8#
0	FDB3, FDB2, FDB1, FDB0	1,0	0	0
1	FDB7, FDB6, FDB5, FDB4	3,2	1	0
2	FDB11, FDB10, FDB9, FDB8	5,4	2	1
3	FDB15, FDB14, FDB13, FDB12	7,6	3	1

Table 6-103. FDB Index Configuration

Location	Name	Access Type	Reset State	Description
R10[8-0]	FDB_Address	R/W	9h	FID Index for PRU Read/Write access of the FDB. Index is direct mapping to the 16KB FDB RAM. Note: Width is 256-bits or 32Bytes 0h: 1st 32 Bytes 1h = 2nd 32 Bytes In general purpose mode, the compare always occurs R10[8] determines the Bank 0h: FDB0 (Bank0) 1h: FDB1 (Bank1)
R10[15]	AutoIndexEn	R/W	1h	FID Auto Increment the Index Enable. 0h: Disable Auto Increment 1h: Enable Auto Increment Each PRU Write or Read to the FDB Array will cause the FDB_Address by 1 Note: 1Byte write or a 32Byte will do the auto increment of 1 In general purpose mode, the compare always occurs after each access **Note: Address rollover is not supported**

Table 6-104. Port<1/0>_Result and Host

Location	Name	Access Type	Reset State	Description
R10[7-0]	FID	R	-	FID from the last VLAN_ID lookup Sticky /Persistence
R10[15-8]	FID_C1	R	-	FID_C1 from the last VLAN_ID lookup Sticky /Persistence. Valid when FID_C1_LUE is SET.
R10[23-16]	DA_FID_C2	R	-	**Valid only for HSR Disabled** (MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 0h) FID_C2 from the last DA FDB lookup Sticky /Persistence. Valid when DA_FID_C2_LUE is SET.
R10[31-24]	SA_FID_C2	R	-	**Valid only for HSR Disabled** (MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 0h) FID_C2 from the last SA FDB lookup Sticky /Persistence. Valid when SA_FID_C2_LUE is SET.
R11[8-0]	DA_FDB_Address	R	-	Address of the HIT Sticky /Persistence.Valid when DA_FID_C2_LUE. Always valid even if a SA match was not found. Used for learning. Always the physical address of the FDB RAM.
R11[9]	RESERVED	R	-	Reserved
R11[10]	DA_FDB_Offset	R	-	Offset only valid for bucket size 2. Used to determine start of the bucket.
R11[11]	RESERVED	R	-	Reserved

Table 6-104. Port<1/0>_Result and Host (continued)

Location	Name	Access Type	Reset State	Description
R11[14-12]	DA_Bucket#	R	-	Returns the Bucket# 0h: (#1) 3h: (#4) ... 7h: (#8) Valid when DA_FID_C2_LUE & DA_FDB_MATCH
R11[15]	RESERVED	R	-	Reserved
R11[24-16]	SA_FDB_Address	R	-	Address of the HIT Sticky /Persistence. Valid when SA_FID_C2_LUE. Always valid even if a SA match was not found. Used for learning. Always the physical address of the FDB RAM.
R11[25]	RESERVED	R	-	Reserved
R11[26]	SA_FDB_Offset	R	-	Offset only valid for bucket size 2. Used determine start of the bucket.
R11[27]	RESERVED	R	-	Reserved
R11[30-28]	SA_Bucket#	R	-	Returns the Bucket# 0h: (#1) 3h: (#4) ... 7h: (#8) Valid when SA_FID_C2_LUE & SA_FDB_MATCH
R12[0]	FID_C1_LUE	R	-	FID C1 LookUpEnd CLR ON SOF OR HOST MMR WRT SET ON After FID lookup, FID is valid and FID_C1 is valid
R12[1]	DA_FID_C2_LUE	R	-	FID C2 LookUpEnd CLR ON Port<1/> SOF OR HOST MMR WRT SET ON After DA FDB lookup and DA, FID & FID_MASK Match. After the first Match it will stop
R12[3]	SA_FID_C2_LUE	R	-	FID C2 LookUpEnd CLR ON Port<0/1> SOF OR HOST MMR WRT SET ON After SA FDB lookup completed
R12[4]	SA_FDB_MATCH	R	-	CLR ON Port<0/1> SOF OR HOST MMR WRT SET ON After SA FDB lookup and SA, FID & FID_MASK Match. After the first Match it will stop

Table 6-105. General Purpose Result

Location	Name	Access Type	Reset State	Description
R10[0]	MATCH	R	-	Default Read Mode of FDB RAM Set, when After XOUT of new Pattern or new Address must wait for 2 clock cycles. Before you can XIN MATCH value By default, below is the compare function XOUT of new pattern(optional). XOUT of new FDB Address(optional). Wait 2 clock cycles. GeneralPattern[gp_size:0] == FDB_RAM.Q[gp_size:0] Write Mode Set when XOUT of write data to the FDB RAM matches the GeneralPattern XOUT of new pattern(optional) XOUT of new FDB Address(optional) XOUT to new data to FDB RAM DATA to compare Wait 2 clock cycles. Before you can XIN MATCH value GeneralPattern[gp_size:0] == FDB_RAM.D[gp_size:0] gp_size is defined in FDB_GEN_CFG2 register. FDB_GEN_MODE_BYTE_EN bit field defines the FDB general mode byte compare size: from 1 Byte upto 16 Bytes The compare function is always active
R10[1]	DONE	R	-	CLR ON Any update on GeneralPattern SET ON After the compare has completed. Note: A new compare operation will occur on: Any update on GeneralPattern Any update on FDB_Address Any Write/Read of FDB_Data

6.4.6.2.10.1.4 FDB General purpose compare mode operation

When FDB0/FDB1 LUT is disabled, then General purpose compare mode of operation is enabled for that Bank through registers: MII_G_RT_FDB_GEN_CFG2[7] FDB_GEN_MODE_EN_BK0 (for Bank0) and [8] FDB_GEN_MODE_EN_BK1 (for Bank1).

Compare flow:

- XOUT GeneralPattern
- XOUT FDB_Address
- Delay 2 clock cycles
- XIN General_Results

Another method to perform the compare is:

- XOUT GeneralPattern
- XOUT FDB_Address, enable AutoIndex
- Delay 2 clock cycles
- XIN General_Results for Index
- XIN FDB_DATA (this advances the FDB Address)
- Delay 2 clock cycles
- XIN General_Results for Index + 1

6.4.6.3 PRU_ICSSG Data Movement Accelerators Functional

6.4.6.3.1 PRU_ICSSG XFR2VBUS Hardware Accelerator

RTU_PRU core can write and read data packets to and from port queues, located in the MSMC SRAM into PRU/RTU_PRU core registers via XFR2VBUS hardware accelerator. Each of the PRU_ICSSG Slices has implemented two sets of TX/RX XFR2VBUS hardware accelerators.

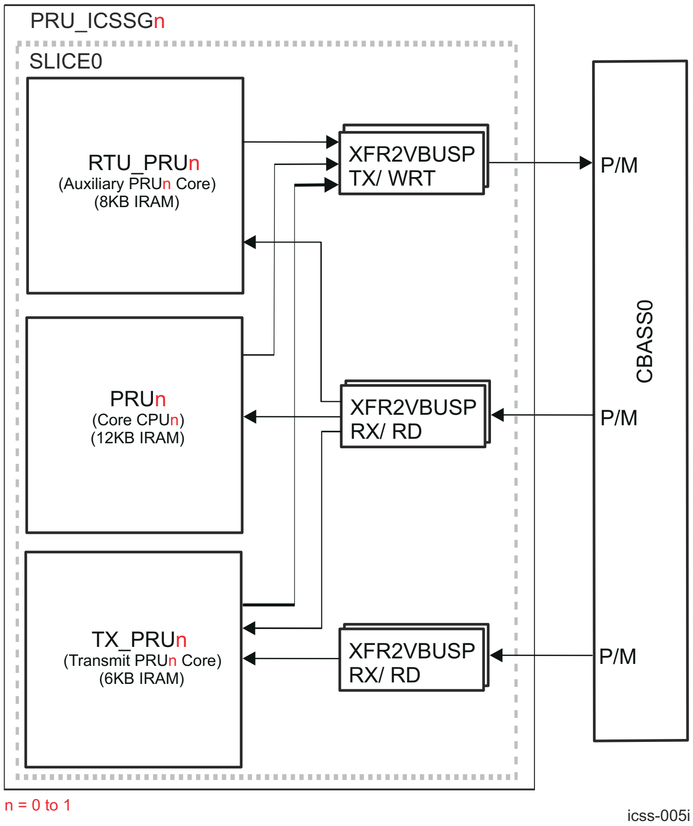

Figure 6-59. XFR2VBUS Hardware Accelerator

Supported features:

- 2 x XFR2VBUS RX threads
- 2 x XFR2VBUS TX threads
- 2 x XFR2VBUS RX only threads, attached to TX_PRU0 and TX_PRU1 Transmit cores

XFR2VBUS RX buffer features:

- 1 x 64 Byte deep RX/Read buffer
  - 4 Byte, 32 Byte, or 64 Byte read size per RD (read) command
  - Optional automatic read command with incrementing address on pop of read data
  - 32 Byte optimization mode available

XFR2VBUS TX buffer features:

- 1 x 64 Byte deep TX/Write buffer
  - 1 Byte up to 64 Byte write size per WRT (write) command

The ownership of commands and data is flexible. The XFR2VBUS accelerator is shared between RTU_PRU and PRU cores. Either RTU_PRU or PRU cores can own command or data. Status is available to both cores.

Note: The ownership should be preplanned and static per use model.

The XFR2VBUS is a simple hardware accelerator wich is used to get the lowest read round trip latency from MSMC and to decouple the latency seen by the PRU. Each XFR2VBUS instance is connected to the CBASS0.

The PRU_ICSSG system has a total of 4 XFR2VBUS TX/RX hardware accelerators and 2 extra XFR2VBUS RX only, attached to each of the TX_PRU cores.

The hardware has no protect nor arbitration between the 2 controllers, so it is the firmware responsibility to insure there is only one owner/access to a common address.

6.4.6.3.1.1 Blocking Conditions

The only blocking condition is caused when the VBUSM command/data FIFO is full. It is required that the external bandwidth is very high. All egress commands and data should get sent without head of line blocking. Based on arbitration some delay is possible.

6.4.6.3.1.2 Read Operation with Auto Disabled

The XFR2VBUS supports 1 command in its command FIFO, 1 XOUT to define the address and size (4 Byte, 32 Byte, 64 Byte, aligned). This will cause the VBUSP read command to be issued. Only 1 read command can be in flight. The read address defines the offset of the 64 Byte of read data. The read size defines the size of the transfer, 4 Byte, 32 Byte, 64 Byte, aligned Offset + size must be aligned to 32 Byte width of the bus. 1 XIN, the software can see the status of command FIFO and read data FIFO.

Note: XIN of the read data will fully pop the data, independent of XIN size.

6.4.6.3.1.3 Read Operation with Auto Enabled

The same features as Auto Disabled are valid with the following exceptions:

64 Byte mode:

- Address needs to be MOD 0x40/64 Byte aligned
- Size needs to be 64 Byte
- 1 XOUT to define the start address, which needs to be MOD 0x40/64 Byte aligned
- The XFR2VBUS will issue 1 new command every time this is 64 Bytes available in the read data FIFO
- 1 XIN of read data will cause a new command to be issued since, 64 Bytes are available
- To stop the issuing new read commands, disable auto mode

32 Byte mode:

- Size needs to be 32 Byte
- 1 XOUT to define the start address, which needs to be MOD 0x20/32 Byte aligned
- The XFR2VBUS will issue 1 new command every time this is 32 Bytes available in the read data FIFO
- 1 XIN of read data will cause a new command to be issued since, 32 Bytes are available
- To stop the issuing of new read command, disable auto mode

Note: XIN of the read data will fully pop the data, independent of XIN size.

6.4.6.3.1.4 Write Operation with Auto Disabled

The XFR2VBUS supports 1 command in the command FIFO.

- 1 XOUT to define the address, data and size (on the fly). 1 Byte, 4 Byte, 32 Byte, 64 Byte and must be aligned.
- Only 1 write command can be in flight since this is VBUSP
- 1 XIN the software can see the status of write command FIFO and write data FIFO

6.4.6.3.1.5 RTU_PRU/ PRU to XFR2VBUS Interface

WR_ID0 = 0x62

WR_ID1 = 0x63

Table 6-106. Write Commands

PRU Register	BS ID	Access Type	Register	Notes
64 Byte Mode (Implied if R17.b3 enable is true)				
R17-R2	WR_ID0/1	XOUT	WR_DATA	Write Data Only 1 XOUT is allowed per transfer including the address/data Must be atomic XOUT R19-R2

Table 6-106. Write Commands (continued)

PRU Register	BS ID	Access Type	Register	Notes
R19-R18	WR_ID0/1	XOUT	WR_ADDR	Write address 48-bits 2 options: Write the full 48-bits with one XOUT or Write the lower 32-bits with one XOUT Note, the one XOUT can set the address and data at the same time, but in this case data needs to be the full 64 bytes. The address can be the full 48-bits or just the lower 32-bits of the address, it will use the current state of the upper 16-bits. Address must be aligned
32 Byte Mode (Implied if R17.b3 enable is false)				
R9-R2	WR_ID0/1	XOUT	WR_DATA	Write Data Size restrictions 1 byte 4 bytes aligned with address, no holes 32 bytes aligned with address, no holes Only 1 XOUT is allowed per transfer including the address/data Only 1 byte and 4 bytes allow not aligned access if MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN is set.
R11-R10	WR_ID0/1	XOUT	WR_ADDR	Write address 48-bits 2 options: Write the full 48-bits with one XOUT or Write the lower 32-bits with one XOUT Note, the one XOUT can set the address and data at the same time, but in this case data needs to be the full 32 bytes. The address can be the full 48-bits or just the lower 32-bits of the address, it will use the current state of the upper 16-bits.
ALL modes				
R20[0]	WR_ID0/1	XIN	WR_BUSY	Write Busy Status 0h: Idle 1h: Active (WR CMD FIFO LEVEL !=0) or (WR DATA FIFO LEVEL !=0)

RD_ID0 = 0x60

RD_ID1 = 0x61

Table 6-107. Read Commands

PRU Register	BS ID	Access Type	Register	Notes
R17-R2	RD_ID1/0	XIN	RD_DATA	Read Data

Table 6-107. Read Commands (continued)

PRU Register	BS ID	Access Type	Register	Notes
R18[0]	RD_ID1/0	XOUT	RD_AUTO	Read Auto Mode If 0 -> 1, must write RD_ADDR If 1 -> 0, must not write RD_ADDR, must drain RD_DATA/RD_CMD If 0 -> 0, must write RD_ADDR When set, every RD_DATA pop will cause a new read command and read address to increment by 0x20 for the next read command if size is set to 32 Bytes 0x40 for the next read command if size is set to 64 Bytes In this case, user must set the address to be ether mod 0x20 or 0x40. 4 Byte mode is not supported.
R18[2-1]	RD_ID1/0	XOUT	RD_SIZE	Read Size 0h: 4 Bytes 1h: Reserved 2h: 32 Bytes 3h: 64 Bytes
R18[0]	RD_ID1/0	XIN	RD_BUSY	Read Busy Status 0h: Idle 1h: Active (RD CMD FIFO LEVEL !=0) or (RD DATA FIFO LEVEL !=0)
R18[1]	RD_ID1/0	XIN	RD_CMD_FL	Read command FIFO Level 0h: Empty 1h: Occupied Note: It only pop the read command FIFO after the read data has arrived
R18[2]	RD_ID1/0	XIN	RD_DATA_FL	Read data FIFO Level 0h: Empty 1h: Occupied 32 byte or 64 byte Note: In 64 byte mode, the user must wait for RD_MST_REQ = 0h before reading the FIFO.
R18[3]	RD_ID1/0	XIN	RD_MST_REQ	RD MST RED 0h = Last data has been latched 1h = Last data is still in flight Note: In Auto mode, the user must insure that this bit is 0h and wait an additional NOP before user disables Auto mode to prevent a race condition.
R20:R19	RD_ID1/0	XOUT	RD_ADDR	Read address 48-bits 0x20 for the next read command if size is set to 32 Bytes 0x40 for the next read command if size is set to 64 Bytes The address can be the full 48-bits or just the lower 32-bits of the address, it will use the current state of the upper 16-bits

6.4.6.3.1.6 XFR2VBUS Programming Model

Write:

- Wait WR_BUSY = 0h
- One XOUT 64 Byte data and (6 Byte address or 4 Byte address) at the same time OR
- One XOUT 32 Byte data and (6 Byte address or 4 Byte address) at the same time OR
- XOUT (6 Byte address or 4 Byte address) and then XOUT 64 Byte data OR
- XOUT (6 Byte address or 4 Byte address) then XOUT 32 Byte/ 8 Byte/ 4 Byte/ 1 Byte data

Read:
- Wait RD_BUSY = 0h
- XOUT R18 (configure RD_AUTO/ RD_SIZE); R19 (RD_ADDR)
- Wait WR_BUSY = 0h OR RD_DATA_FL = 1h
- XIN RD_DATA (Repeat if RD_AUTO is enabled and need new RD_DATA, must always check RD_DATA_FL before XIN RD_DATA)

6.4.6.3.2 PRU_ICSSG XFRDMA Functional Operation

The XFRDMA block performs a translation between an XFR bus and PSI-L busses that PRU core uses for packet traffic. This allows the PRU core to directly receive and transmit packets on PSI-L, using the wide busses that PSI-L and XFR provide.

Main supported features:
- Performs a translation between XFR and PSI busses for a PRU
- Supports a configurable number of PSI-L threads, up to 32.
- Supports a configurable data width, 64, 128, or 256 bits

6.4.6.3.2.1 XFRDMA: XFR Bus

The XFRDMA block has an XFR bus with a configured data width that matches the PSI-L data width with an extra 4 Bytes for the sideband signals and fields. The XID to the XFRDMA block is used to select the PSI-L thread to access. For example XFRDMA block XID 1 is for the first thread, and XID N is for the N-th thread. The XFRDMA block will allow interleaving between PSI-L threads.

6.4.6.3.2.1.1 XFRDMA: XFR Status

The XFRDMA block uses XID 0 to read status of the PSI-L bus. An XIN to XFRDMA XID 0 returns the following data:
- Rx_ready can be used to check when there is receive data ready on a PSI-L thread.
- Tx_ready can be used to check if the XFRDMA block is able to transmit the data to that PSI-L thread without stalling.

These bits are also available as outputs that can be used for PRU core status inputs.

Table 6-108 shows the device XFR status.

Table 6-108. XFR STATUS

Word	Bit	Signal	Description
0	31-0	rx_ready[3:0]	RX data ready, one bit per PSI-L thread
1	31-0	tx_ready[3:0]	Ready for TX data, one bit per PSI-L thread

6.4.6.3.2.1.2 XFRDMA: XFR Bus XOUT

The XFRDMA block will take XOUT data and translate into a transmit PSI-L packet. The first word of XFR data determines the sideband and fields for transmit and must always be present. The remaining bytes are the transmit data. The XFRDMA block assumes the contained data is correctly formatted. The XFRDMA block also assumes the data type is in the correct order, such as info words, then control, then payload, then status.

Table 6-109. XOUT STATUS

Word	Bit	Field	Description
0	0	tx_sop	Transmit has PSI-L sop signal.
0	1	tx_eop	Transmit has PSI-L eop signal.

Table 6-109. XOUT STATUS (continued)

Word	Bit	Field	Description
0	2	tx_sol	Transmit has PSI-L sol signal.
0	3	tx_eol	Transmit has PSI-L eol signal.
0	4	tx_lastw	Transmit has PSI-L lastw signal, meaning that is no more data for this data_type.
0	5	tx_drop	Transmit has PSI-L drop signal.
0	11-8	tx_pkt_error[3:0]	Transmit has PSI-L pkt_error signal.
0	23-16	tx_data_type[7:0]	Transmit has PSI-L data_type signal.
0	31-24	tx_xcnt[7:0]	Transmit byte count for XOUT, or for certain data types it is the worden[7:0] field.
1-N	31-0	tx_data	Transmit PSI-L data.

6.4.6.3.2.1.3 XFRDMA: XFR Bus XOUXFRDMA Functional Operation T Alignment

The XFRDMA block will correct for misaligned data. For a new data type value, the XFRDMA will shift the entire XFR data from the first enabled byte to the most significant byte on the PSI-L bus using big endian ordering. For continued data type values, the XFRDMA will pack the enabled bytes to the previous data until a full PSI-L line is formed and can be sent. The remaining data will start a new PSI-L line. Any leftover data when an EOP is written will be sent immediately in the next EOP data phase on the PSI-L. It is required that the XOUT have contiguous byte enables, as the XFRDMA will not account for any gaps. The XFRDMA block will update the xcnt locally for additional data, but it cannot update for data types that use the worden field, so that should be correct from the initial XOUT that started the data type.

6.4.6.3.2.1.4 XFRDMA: XFR Bus XIN

The XFRDMA block will take PSI-L packet receive data and translate it into XIN data. The first word of XFR data determines the sideband and fields for receive and must always be present. These fields also indicate how many bytes were valid, which could be 0 if there is no data present. If the PSI-L data does not fill the enabled bytes on the XFR, the remaining bytes are returned as 0s. The XFRDMA block will return all the PSI-L data in the same order as it was received. Receive data for different data_types will be returned on successive XINs and are not merged.

Table 6-110. XIN STATUS

Word	Bit	Field	Description
0	0	rx_sop	Receive has PSI-L sop signal.
0	1	rx_eop	Receive has PSI-L eop signal.
0	2	rx_sol	Receive has PSI-L sol signal.
0	3	rx_eol	Receive has PSI-L eol signal.
0	4	rx_lastw	Receive has PSI-L lastw signal, meaning that is no more data for this data_type.
0	5	rx_drop	Receive has PSI-L drop signal.
0	11-8	rx_pkt_error[3-0]	Receive has PSI-L pkt_error signal.
0	23-16	rx_data_type[7-0]	Receive has PSI-L data_type signal.
0	31-24	rx_xcnt[7-0]	Receive byte count for XIN, or for certain data types it is the worden[7:0] field.
1-N	31-0	rx_data	Receive PSI-L data.

6.4.6.3.2.1.4.1 XFRDMA: XFR Bus XIN Alignment

The source and the target entities advertise their availability to transfer data on a set of threads and the arbiter then selects one of the threads to transfer data on next. The arbiter outputs the thread ID that has been selected for transfer to both the source and target along with a request strobe to transfer data. Data is transferred in next cycle following the cycle in which the arbiter asserts the request strobe.

The XFRDMA block will correct for misaligned data. The next set of PSI-L data will be presented on the first enabled byte on the XFR bus using big endian ordering, and only the enabled number of bytes will be returned on the XFR bus. It is required that the XIN have contiguous byte enables, as the XFRDMA will not account for any gaps. The rx_xcnt will represent the valid bytes returned, and if the line is not complete then it will be 0. For data_types that use the worden signal the rx_xcnt will be the worden for the read data. The XFRDMA does not correct aligned in these worden types, so they should only be read in words.

6.4.6.3.2.2 XFRDMA: PSI-L Bus

The XFRDMA block has a pair of PSI-L busses, one for transmit and one for receive. They are using the configured data width and number of threads. The transmit PSI-L is drived by the XOUT data, while the receive PSI-L will feed the XIN data and status. When there is a transmit word ready, the XFRDMA block will assert the thread_mready for that thread. The PSI-L arbiter will determine when a thread can transmit and only then will the XFRDMA actually transmit data. The XFRDMA block will assert the thread_sready to accept receive data when the buffer for that thread is able to accept another data phase. Again, the PSI-L arbiter will determine when a thread will receive data and only then will the buffer store the received data. Any PSI-L sideband signals are transmitted with the data phase, or received with the data phase.

The packet streaming interface (PSI) is used to transfer words of packet data and control information between two peer entities in the system via arbiter.

Figure 6-60 shows a block diagram of the PRU_ICSSG PSI topology.

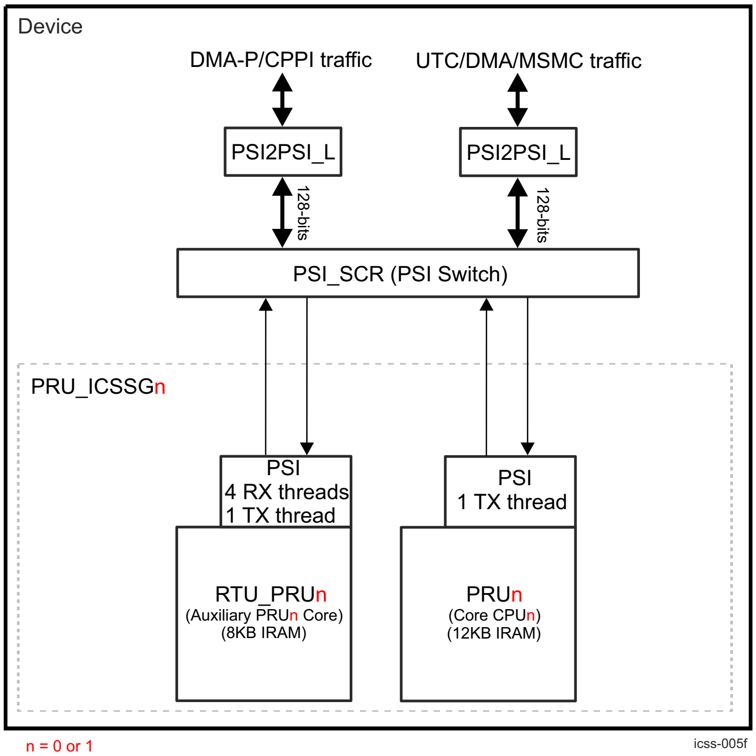

Figure 6-60. PRU_ICSSG PSI Topology

6.4.6.3.2.2.1 PRU XFRPSI Mapping

Table 6-111. PRU XFRPSI Mapping

RTU_PRUx/PRUx	xfrpsi_wgt	Note
R5:R1	[159:0] xfr_psi_wdata	R1 is metadata R2 is start of data
R5:R1	[159:0] xfr_psi_rdata	R1 is metadata R2 is start of data
bs_addr[7:4] = 4’h5	xfr_psi_req	Chip Select Decode
bs_addr[3:0]	xfr_psi_addr[3:0]	Direct Connect

6.4.6.3.2.3 XFRDMA: Temporary FIFOs

The XFRDMA block has two temporay FIFOs that store the data during the translation, one for transmit and one for receive. Each FIFO has a configurable number of data phases of storage per configured thread. Each FIFO can be accessed independently, and by both the XFR and PSI-L in the same cycle to maintain full bandwidth. For transmit the FIFO holds and packs the XOUT data until it can be sent on the PSI-L bus. For receive the FIFO holds the PSI-L data until it can be unpacked to the XIN data. A transmit FIFO that has a full data phase available or has reached the end of data for that data type is ready to transmit on the PSI-L bus. A receive FIFO that has a full data phase available or has reached the end of data for that data type is ready to receive on an XIN.

6.4.6.3.2.3.1 XFRDMA: FIFO Stalls

An XOUT to a transmit FIFO that does not have at least one empty line will result in a stall. Only when the PSI-L transmits some data for that thread, the stall will be released. An XIN to an receive FIFO that does not have a set of data will return blank data of all 0s, and the rx_bytes field will be set to 0. To avoid any transmit stalls, the associated status signal should be checked before sending the XOUT. Every XIN should check the rx_bytes field to determine the number of valid bytes, or the associated status signal should be checked to guarantee a full line of data.

6.4.6.3.3 PRU_ICSSG XFR2TR Ring Accelerator

XFR2TR ring is used for accelerating the internal memory copy of worklist from Tranfer Requests (TR).

One XFR2TR ring is attached to each of the RTU_PRU cores. XFR2TR creates a Send list by doing a local memory copy of fixed (preconfigured) TR receive list to the Send list. This is accompished by XOUT commands to define which predefined TRs to add to the list. In this case preconfigured list and Send list are stored in PRU_ICSSG shared RAM (Data RAM2).

Supported features:

- Upto 4KB of source Transfer Requests (TRs)
- 1 ring, with wrap around support along with observation of write pointer and reset write pointer
- Programmable TR size (8Bytes/ 64Bytes) and TR base for source TR queue
- Programmable TR size (8Bytes/ 64Bytes) and ring base for destination ring
- 8-level deep FIFO for TR IDs, upto 8 IDs per XOUT

Not supported features:

- External memory for TRs or Ring
- Hardware Door Bell (firmware will accomplish the Door Bell)
- Hardware Ring completion (managed by firmware)

Table 6-112. RTU_PRU to XFR2TR Ring Interface

RTU_PRU Register	BS ID	Access Type	Register	Notes
R6[17-0]	0x70	XOUT	tr_msrc_base[17-0] Needs to be mode 0x4	Controller TR list Base Address
R7[0]	0x70	XOUT	tr_size 0h: 8 Bytes 1h: 64 Bytes	Size of the TR element
R6[17-0]	0x71	XOUT	tr_rsrc_base[17-0] Needs to be mode 0x40 or 0x08 Size of TR element	Ring TR list Base Address
R7[0]	0x71	XOUT	Reserved	Reserved
R7[1]	0x71	XOUT	tr_rscr_reset	This reset the ring pointer

Table 6-112. RTU_PRU to XFR2TR Ring Interface (continued)

RTU_PRU Register	BS ID	Access Type	Register	Notes
R7[19-8]	0x71	XOUT	tr_rsrc_nums 0 = 1 TR 4095 = 4096 TRs	The number of the TRs in the ring. This defines the Ring size, which defines the wrap around. Note: It must be larger than maximum submitted TRs. For example, XOUT of 8 TRs then, tr_rsrc_nums >= 7(8)
R7[0]	0x71	XIN	tr_rsrc_busy 0h: Not Busy 1x: Busy	The busy status. It will be busy until the FIFO is empty AND the last write completed /data has landed.
R7[11-8]	0x71	XIN	tr_rscr_fifo_occ 0h: empty 1h: 1 ID 2h: 2 IDs	The number of elements in the submit FIFO.
R8[17-0]	0x71	XIN	tr_rsrc_wrt_ptr	This is the current Write pointer
R5:R2	0x72	XOUT	R2[11-0] = ID0[11-0] R2[27-16] = ID1[11-0] R3[11-0] = ID2[11-0] R3[27-16] = ID3[11-0] R4[11-0] = ID4[11-0] R4[27-16] = ID5[11-0] R5[11-0] = ID6[11-0] R5[27-16] = ID7[11-0]	Submit of TRs 1 to 8 IDs per XOUT Left packed ID0 ID1:0 ...... No holes or offsets

6.4.6.3.3.1 XFR2TR Programming Model

This section covers the low-level programming model of the XFR2TR ring accelerator.

Typical usage model.

Initial:
- Set number ot Transfer Requests (TRs)
- Set TR size
- Set source and destination address

Set A: N = 240, Size = 128B
- Loop N times, make sure that N is bigger ring size
- Push 8 TRs
- Wait for busy

New set, start fresh.

Hit reset.

Set B: N = 140, Size = 80B
- Loop N times, and make sure that N is bigger ring size
- Push 8 TRs
- Wait for busy

New set, start fresh.

Hit reset.

Set C: N = 440, Size = 120B
- Loop N times, and make sure that N is bigger ring size
- Push 8 TRs
- Wait for busy

Typical Ring size will be 100B, 120B, 250B, 512B, just defines when to wrap.

Source table linear table of 2^{12}

Source IDs, linear table

Address value
- 0<0>
- 1<1>
- 2<2>
- 3<3>
- 4<4>
- 5<5>

XOUT 0,1,2,6,3

RD Address value WR Address value
- 3<3> -> 0<3>
- 6<6> -> 1<6>
- 2<2> -> 2<2>
- 1<1> -> 3<1>
- 0<0> -> 4<0>

XOUT 20,4,7,0,1,2

RD Address value WR Address value
- 2<2> -> 5<2>
- 1<1> -> 6<1>
- 0<0> -> 7<0>
- 7<7> -> 8<7>
- 4<4> -> 9<4>
- 20<20> -> 10<20>

RD Address value WR Address value
- 2<2> -> 0<2>
- 1<1> -> 1<1>
- 0<0> -> 2<0>
- 7<7> -> 3<7>
- 4<4> -> 4<4>
- 20<20> -> 5<20>

6.4.7 PRU_ICSSG Local INTC

The PRU_ICSSG interrupt controller (INTC) maps interrupts coming from different parts of the device (mapped to PRU_ICSSGn, where n = 0 or 1) to a reduced set of PRU_ICSSG interrupt channels.

The interrupt controller has the following features:

- Capturing up to 160 Events (inputs):
  - Upper 96 are external events
  - Lower 64 are internal events
- Supports up to 20 output interrupt channels.
- Generation of 20 Host Interrupts
  - 2 Host Interrupts shared between the PRUs (PRU0 and PRU1) and TX_PRUs (TX_PRU0 and TX_PRU1).
  - 2 Host Interrupts for the RTU PRUs (RTU_PRU0 and RTU_PRU1).
  - 8 Host Interrupts exported from the PRU_ICSSG internal INTC for signaling the device level interrupt controllers (pulse and level provided).
  - 8 Host Interrupts (event 12 through 19) for the Task Managers.
- Each event can be enabled and disabled.
- Each host event can be enabled and disabled.
- Hardware prioritization of events.

6.4.7.1 PRU_ICSSG Interrupt Controller Functional Description

The PRU_ICSSG INTC supports up to 160 interrupts from different peripherals (including 64 internal interrupts from PRU_ICSSG located interrupt sources). The INTC maps these events to 20 channels inside the INTC (see Figure 6-61). Interrupts from these 20 channels are further mapped to 20 Host Interrupts.

- Any of the 160 internal interrupts can be mapped to any of the 20 channels.
- Multiple interrupts can be mapped to a single channel.
- An interrupt should not be mapped to more than one channel.
- Any of the 20 channels can be mapped to any of the 20 host interrupts. It is recommended to map channel “x” to host interrupt “x”, where x is from 0 to 19.
- A channel should not be mapped to more than one host interrupt
- For channels mapping to the same host interrupt, lower number channels have higher priority.
- For interrupts on same channel, priority is determined by the hardware interrupt number. The lower the interrupt number, the higher the priority.
- Host Interrupt 0 is connected to bit 30 in register 31 (R31) of PRU0, PRU1, TX_PRU0 and TX_PRU1 in parallel.
- Host Interrupt 1 is connected to bit 31 in register 31 (R31) for PRU0, PRU1, TX_PRU0 and TX_PRU1 in parallel.
- Host Interrupts 2 through 9 exported from PRU_ICSSG and mapped to device level interrupt controllers.
- Host Interrupt 10 is connected to bit 30 in register 31 (R31) to both RTU_PRU0 and RTU_PRU1 in parallel.
- Host Interrupt 11 is connected to bit 31 in register 31 (R31) to both RTU_PRU0 and RTU_PRU1 in parallel.
- Host Interrupts 12 through 19 are connected to each of the 6 Task Managers.

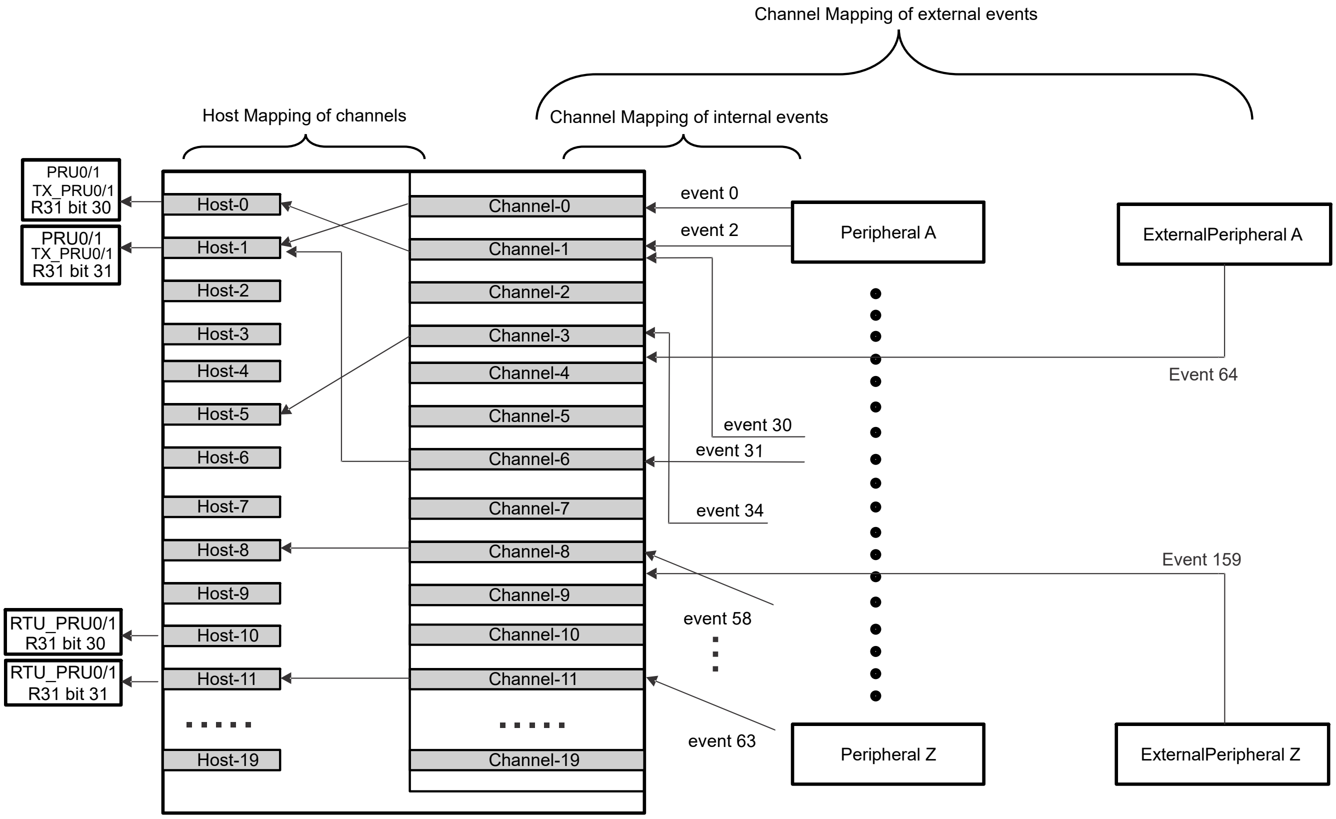

Figure 6-61. PRU_ICSSG Interrupt Controller Block Diagram

6.4.7.1.1 PRU_ICSSG Interrupt Controller Events

All 160 PRU_ICSSG system events are interrupt inputs. System events 64 through 159 are external and are generated from different peripherals. System events 0 through 63 are internal and are generated from internal for PRU_ICSSG sources.

6.4.7.1.2 PRU_ICSSG Interrupt Controller System Events Flow

The ICSS_INTC module controls the event mapping to the host interrupt interface. Events are generated by the device peripherals or PRUs. The INTC receives the internal interrupts and maps them to internal channels. The channels are used to group interrupts together and to prioritize them. These channels are then mapped onto the host interrupts. Interrupts from the system side are active high in polarity.

The INTC encompasses many functions to process the system interrupts and prepare them for the host interface. These functions are: processing, enabling, status, channel mapping, host interrupt mapping, prioritization, and host interfacing. Figure 6-62 illustrates the flow of interrupts through the functions to the host. The following subsections describe each part of the flow.

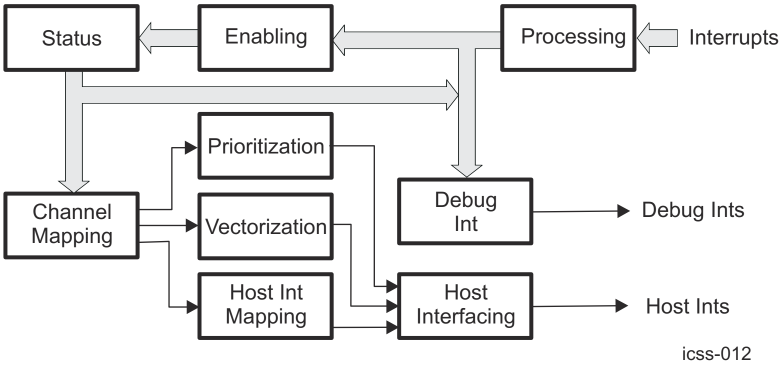

Figure 6-62. Flow of System Interrupts to Host

6.4.7.1.2.1 PRU_ICSSG Interrupt Processing

This block does following tasks:

- Synchronization of slower and asynchronous interrupts
- Conversion of polarity to active high
- Conversion of interrupt type to pulse interrupts

After the processing block, all interrupts will be active high pulses.

6.4.7.1.2.1.1 PRU_ICSSG Interrupt Enabling

The next stage of INTC is to enable interrupts based on programmed settings. The following sequence has to be followed to enable interrupts:

- Enable required interrupts: System interrupts that are required to get propagated to host are to be enabled individually by writing to [9-0] ENABLE_SET_INDEX bit field in the interrupt enable indexed set register (ICSS_INTC_ENABLE_SET_INDEX_REG). The interrupt to enable is the index value written. This sets the Enable Register bit of the given index.
- Enable required host interrupts: By writing 1h to the appropriate bit of the [9-0] HINT_ENABLE_SET_INDEX bit field in the host interrupt enable indexed set register (ICSS_INTC_HINT_ENABLE_SET_INDEX_REG), enable the required host interrupts. The host interrupt to enable is the index value written. This enables the host interrupt output or triggers the output again if that host interrupt is already enabled.
- Enable all host interrupts: By setting the [0] ENABLE_HINT_ANY bit in the global enable register (ICSS_INTC_GLOBAL_ENABLE_HINT_REG) to 1h, all host interrupts will be enabled. Individual host interrupts are still enabled or disabled from their individual enables and are not overridden by the global enable.

6.4.7.1.2.2 PRU_ICSSG Interrupt Status Checking

The next stage is to capture which interrupts are pending. There are two kinds of pending status: raw status and enabled status. Raw status is the pending status of the interrupt without regards to the enable bit for the interrupt. Enabled status is the pending status of the interrupts with the enable bits active. When the enable bit is inactive, the enabled status will always be inactive. The enabled status of interrupts is captured in interrupt status enabled/clear registers (ICSS_INTC_ENABLE_CLR_REG0 to ICSS_INTC_ENABLE_CLR_REG4).

Status of interrupt 'N' is indicated by the N-th bit of ICSS_INTC_ENABLE_CLR_REG0 to ICSS_INTC_ENABLE_CLR_REG4 . Since there are 160 interrupts, five 32-bit registers are used to capture the enabled status of interrupts. The pending status reflects whether the interrupt occurred since the last time the status register bit was cleared. Each bit in the status register can be individually cleared.

6.4.7.1.2.3 PRU_ICSSG Interrupt Channel Mapping

The INTC has 20 internal channels to which enabled interrupts can be mapped. Channel 0 has highest priority and channel 19 has the lowest priority. Channels are used to group the interrupts into a smaller number of priorities that can be given to a host interface with a very small number of interrupt inputs.

When multiple interrupts are mapped to the same channel their interrupts are ORed together so that when either is active the output is active. The channel map registers (ICSS_INTC_CH_MAP_REGi, where i=0 to 39) define the channel for each interrupt. There is one register per 4 interrupts; therefore, there are 40 channel map registers for a of 160 interrupts. The channel for each interrupt can be set using these registers.

6.4.7.1.2.3.1 PRU_ICSSG Host Interrupt Mapping

The hosts can be the local PRU processors (PRU0, PRU1, RTU_PRU0, RTU_PRU1, TX_PRU0, TX_PRU1) as well as device processors located outside PRU_ICSSG such as MPU Cortex-A53, etc. The 20 channels from the INTC can be mapped to any of the 20 Host interrupts. The Host map registers (ICSS_INTC_HINT_MAP_REG0 to ICSS_INTC_HINT_MAP_REG4) define the channel for each interrupt. There is one register per 4 channels; therefore, there are 5 host map registers for 20 channels. When multiple channels are mapped to the same host interrupt, then prioritization is done to select which interrupt is in the highest-priority channel and which should be sent first to the host.

6.4.7.1.2.3.2 PRU_ICSSG Interrupt Prioritization

The next stage of the INTC is prioritization. Since multiple interrupts can feed into a single channel and multiple channels can feed into a single host interrupt, it is necessary to read the status of all interrupts to determine the highest priority interrupt that is pending. The INTC provides hardware to perform this prioritization with a given scheme so that software does not have to do this. There are two levels of prioritizations:

- The first level of prioritization is between the active channels for a host interrupt. Channel 0 has the highest priority and channel 9 has the lowest. So the first level of prioritization picks the lowest numbered active channel.
- The second level of prioritization is between the active interrupts for the prioritized channel. The interrupt in position 0 has the highest priority and interrupt 159 has the lowest priority. So the second level of prioritization picks the lowest position active interrupt.

This is the final prioritized interrupt for the host interrupt and is stored in the global prioritized innterrupt register (ICSS_INTC_GLB_PRI_INTR_REG). The highest priority pending interrupt with respect to each host interrupts can be obtained using the host interrupt prioritized interrupt registers (ICSS_INTC_PRI_HINT_REGj where j = 0 to 19).

6.4.7.1.2.4 PRU_ICSSG Interrupt Nesting

The INTC can also perform a nesting function in its prioritization. Nesting is a method of disabling certain interrupts (usually lower-priority interrupts) when an interrupt is taken so that only those desired interrupts can trigger to the host while it is servicing the current interrupt. The typical usage is to nest on the current interrupt and disable all interrupts of the same or lower priority (or channel). Then the host will only be interrupted from a higher priority interrupt.

The nesting is done in one of three methods:

1. Nesting for all host interrupts, based on channel priority: When an interrupt is taken, the nesting level is set to its channel priority. From then, that channel priority and all lower priority channels will be disabled from generating host interrupts and only higher priority channels are allowed. When the interrupt is completely serviced, the nesting level is returned to its original value. When there is no interrupt being serviced, there are no channels disabled due to nesting. The global nesting level register (ICSS_INTC_GLB_NEST_LEVEL_REG) allows the checking and setting of the global nesting level across all host interrupts. The nesting level is the channel (and all of lower priority channels) that are nested out because of a current interrupt.
2. Nesting for individual host interrupts, based on channel priority: Always nest based on channel priority for each host interrupt individually. When an interrupt is taken on a host interrupt, then, the nesting level is set to its channel priority for just that host interrupt, and other host interrupts do not have their nesting affected. Then for that host interrupt, equal or lower priority channels will not interrupt the host but may on other host interrupts if programmed. When the interrupt is completely serviced the nesting level for the host interrupt is returned to its original value. The host interrupt nesting level registers (ICSS_INTC_NEST_LEVEL_REGj

where j = 0 to 19) display and control the nesting level for each host interrupt. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

3. Software manually performs the nesting of interrupts. When an interrupt is taken, the software will disable all the host interrupts, manually update the enables for any or all the interrupts, and then re-enables all the host interrupts. This now allows only the interrupts that are still enabled to trigger to the host. When the interrupt is completely serviced the software must reverse the changes to re-enable the nested out interrupts. This method requires the most software interaction but gives the most flexibility if simple channel based nesting mechanisms are not adequate.

6.4.7.1.2.5 PRU_ICSSG Interrupt Status Clearing

After servicing the interrupt (after execution of the ISR), interrupt status is to be cleared. If a interrupt status is not cleared, then another host interrupt may not be triggered or another host interrupt may be triggered incorrectly. It is also essential to clear all interrupts before the PRU is halted as the PRU does not power down unless all the interrupt status are cleared. For clearing the status of an interrupt, whose interrupt number is N, write a 1h to the Nth bit position in the interrupt status enabled/clear registers (ICSS_INTC_ENABLE_CLR_REG0 to ICSS_INTC_ENABLE_CLR_REG4). Interrupt N can also be cleared by writing the value N into the interrupt status indexed clear register (ICSS_INTC_STATUS_CLR_INDEX_REG).

6.4.7.1.3 PRU_ICSSG Interrupt Disabling

At any time, if any interrupt is not to be propagated to the host, then that interrupt should be disabled. For disabling an interrupt whose interrupt number is N, write a 1h to the Nth bit in the interrupt enable clear registers (ICSS_INTC_ENABLE_CLR_REG0 to ICSS_INTC_ENABLE_CLR_REG4). Interrupt N can also be disabled by writing the value N in the interrupt enable clear index register (ICSS_INTC_ENABLE_CLR_INDEX_REG).

6.4.7.2 PRU_ICSSG Interrupt Controller Basic Programming Model

Follow these steps to configure the interrupt controller.

1. Set polarity and type of event through the Interrupt Polarity Registers (ICSS_INTC_POLARITY_REG0 to ICSS_INTC_POLARITY_REG4) and the Interrupt Type Registers (ICSS_INTC_TYPE_REG0 to ICSS_INTC_TYPE_REG4). Polarity of all interrupts is always high. Type of all interrupts is always pulse (after the processing block).
2. Map event to INTC channel through ICSS_INTC_CH_MAP_REGi (where i=0 to 39) channel mapping registers.
3. Map channel to host interrupt through ICSS_INTC_HINT_MAP_REG0 to ICSS_INTC_HINT_MAP_REG4 registers. Recommended channel “x” to be mapped to host interrupt “x”.
4. Clear interrupt by writing 1h to ICSS_INTC_ENABLE_CLR_REG0 to ICSS_INTC_ENABLE_CLR_REG4 registers.
5. Enable host interrupt by writing index value to ICSS_INTC_HINT_ENABLE_SET_INDEX_REG register.
6. Enable interrupt nesting if desired.
7. Globally enable all interrupts through register ICSS_INTC_GLOBAL_ENABLE_HINT_REG[0] ENABLE_HINT_ANY bit.

6.4.7.3 PRU_ICSSG Interrupt Requests Mapping

The PRU_ICSSGn Interrupt Controller (where n = 0 or 1) lines 0 through 63 are mapped to internal events which are generated by PRU_ICSSG integrated modules. Table 6-113 shows mapping of the different PRU_ICSSG internally sourced IRQ events to PRU_ICSSG0 INTC and PRU_ICSSG1 INTC interrupt lines 0 through 63.

Table 6-113. PRU_ICSSG0 and PRU_ICSSG1 Internal Interrupts

Event Number	PRU_ICSSG Internal Interrupt Signal	Source
	PRU_ICSSG0 INTC	
63	Any sd_fd_zero/one_max/min(of 72)	
62	pr0_iep1_sync0_uint_intr_pend	PRU_ICSSG0 IEP1
61	pr0_iep1_sync1_uint_intr_pend	PRU_ICSSG0 IEP1
60	pr0_iep1_latch0_uint_intr_pend	PRU_ICSSG0 IEP1
59	pr0_iep1_latch1_uint_intr_pend	PRU_ICSSG0 IEP1
58	pr0_iep1_pdi_wd_exp_pend	PRU_ICSSG0 IEP1
57	pr0_iep1_pd_wd_exp_pend	PRU_ICSSG0 IEP1
56	pr0_iep1_any_cmp_cap_pend	PRU_ICSSG0 IEP1
55	pr0_mii1_col and pr0_mii1_txen (external)if rgmii_col_crs_en MMR is set then in RGMII mode rgmii1_col will be mapped	
54	PRU1_RX_EOF	
53	MDIO_MII_LINK[1]	
52	PORT1_TX_OVERFLOW	
51	PORT1_TX_UNDERFLOW	
50	PRU1_RX_OVERFLOW	
49	PRU1_RX_NIBBLE_ODD	
48	PRU1_RX_CRC	
47	PRU1_RX_SOF	
46	PRU1_RX_SFD	
45	PRU1_RX_ERR32	
44	PRU1_RX_ERR	
43	pr0_mii0_col and pr0_mii0_txen (external)if rgmii_col_crs_en MMR is set then in RGMII mode rgmii0_col will be mapped	
42	PRU0_RX_EOF	
41	MDIO_MII_LINK[0]	
40	PORT0_TX_OVERFLOW	
39	PORT0_TX_UNDERFLOW	
38	PRU0_RX_OVERFLOW	
37	PRU0_RX_NIBBLE_ODD	
36	PRU0_RX_CRC	
35	PRU0_RX_SOF	
34	PRU0_RX_SFD	
33	PRU0_RX_ERR32	PRU_ICSSG0 PRU0
32	PRU0_RX_ERR	PRU_ICSSG0 PRU0
31	pr0_pru_mst_intr[15]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
30	pr0_pru_mst_intr[14]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
29	pr0_pru_mst_intr[13]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
28	pr0_pru_mst_intr[12]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
27	pr0_pru_mst_intr[11]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1

Table 6-113. PRU_ICSSG0 and PRU_ICSSG1 Internal Interrupts (continued)

Event Number	PRU_ICSSG Internal Interrupt Signal	Source
26	pr0_pru_mst_intr[10]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
25	pr0_pru_mst_intr[9]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
24	pr0_pru_mst_intr[8]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
23	pr0_pru_mst_intr[7]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
22	pr0_pru_mst_intr[6]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
21	pr0_pru_mst_intr[5]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
20	pr0_pru_mst_intr[4]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
19	pr0_pru_mst_intr[3]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
18	pr0_pru_mst_intr[2]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
17	pr0_pru_mst_intr[1]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
16	pr0_pru_mst_intr[0]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
15	pr0_ecap_intr_req	PRU_ICSSG0 ECAP0
14	pr0_sync0_out_pend	PRU_ICSSG0 IEP0
13	pr0_sync1_out_pend	PRU_ICSSG0 IEP0
12	pr0_latch0_in (input to PRU_ICSSG0)	PRU_ICSSG0 IEP0
11	pr0_latch1_in (input to PRU_ICSSG0)	PRU_ICSSG0 IEP0
10	pr0_pdi_wd_exp_pend	PRU_ICSSG0 IEP0
9	pr0_pd_wd_exp_pend	PRU_ICSSG0 IEP0
8	pr0_digio_event_req	PRU_ICSSG0 IEP0
7	pr0_iep_tim_cap_cmp_pend	PRU_ICSSG0 IEP0
6	pr0_uart0_uint_intr_req	PRU_ICSSG0 UART0
5	pr0_uart0_utxevt_intr_req	PRU_ICSSG0 UART0
4	pr0_uart0_urxevt_intr_req	PRU_ICSSG0 UART0
3	pr0_rst_reset_iso_req	PRU_ICSSG0 Reset Isolation Requested
2	pr0_pru1_r31_status_cnt16	PRU_ICSSG0 PRU1 (Shift Capture)
1	pr0_pru0_r31_status_cnt16	PRU_ICSSG0 PRU0 (Shift Capture)
0	pr0_ecc_err_intr	PRU_ICSSG0 ECC Logic
	PRU_ICSSG1 INTC	
63	Any sd_fd_zero/one_max/min(of 72)	
62	pr1_iep1_sync0_uint_intr_pend	PRU_ICSSG1 IEP1
61	pr1_iep1_sync1_uint_intr_pend	PRU_ICSSG1 IEP1
60	pr1_iep1_latch0_uint_intr_pend	PRU_ICSSG1 IEP1
59	pr1_iep1_latch1_uint_intr_pend	PRU_ICSSG1 IEP1
58	pr1_iep1_pdi_wd_exp_pend	PRU_ICSSG1 IEP1
57	pr1_iep1_pd_wd_exp_pend	PRU_ICSSG1 IEP1
56	pr1_iep1_any_cmp_cap_pend	PRU_ICSSG1 IEP1
55	pr1_mii1_col and pr1_mii1_txen (external)if rgmii_col_crs_en MMR is set then in RGMII mode rgmii1_col will be mapped	
54	PRU1_RX_EOF	
53	MDIO_MII_LINK[1]	
52	PORT1_TX_OVERFLOW	
51	PORT1_TX_UNDERFLOW	
50	PRU1_RX_OVERFLOW	
49	PRU1_RX_NIBBLE_ODD	
48	PRU1_RX_CRC	

Table 6-113. PRU_ICSSG0 and PRU_ICSSG1 Internal Interrupts (continued)

Event Number	PRU_ICSSG Internal Interrupt Signal	Source
47	PRU1_RX_SOF	
46	PRU1_RX_SFD	
45	PRU1_RX_ERR32	
44	PRU1_RX_ERR	
43	pr1_mii0_col and pr1_mii0_txen (external)if rgmii_col_crs_en MMR is set then in RGMII mode rgmii0_col will be mapped	
42	PRU0_RX_EOF	
41	MDIO_MII_LINK[0]	
40	PORT0_TX_OVERFLOW	
39	PORT0_TX_UNDERFLOW	
38	PRU0_RX_OVERFLOW	
37	PRU0_RX_NIBBLE_ODD	
36	PRU0_RX_CRC	
35	PRU0_RX_SOF	
34	PRU0_RX_SFD	
33	PRU0_RX_ERR32	PRU_ICSSG1 PRU0
32	PRU0_RX_ERR	PRU_ICSSG1 PRU0
31	pr1_pru_mst_intr[15]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
30	pr1_pru_mst_intr[14]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
29	pr1_pru_mst_intr[13]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
28	pr1_pru_mst_intr[12]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
27	pr1_pru_mst_intr[11]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
26	pr1_pru_mst_intr[10]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
25	pr1_pru_mst_intr[9]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
24	pr1_pru_mst_intr[8]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
23	pr1_pru_mst_intr[7]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
22	pr1_pru_mst_intr[6]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
21	pr1_pru_mst_intr[5]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
20	pr1_pru_mst_intr[4]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
19	pr1_pru_mst_intr[3]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
18	pr1_pru_mst_intr[2]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
17	pr1_pru_mst_intr[1]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
16	pr1_pru_mst_intr[0]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
15	pr1_ecap_intr_req	PRU_ICSSG1 ECAP0
14	pr1_sync0_out_pend	PRU_ICSSG1 IEP0
13	pr1_sync1_out_pend	PRU_ICSSG1 IEP0
12	pr1_latch0_in (input to PRU_ICSSG1)	PRU_ICSSG1 IEP0
11	pr1_latch1_in (input to PRU_ICSSG1)	PRU_ICSSG1 IEP0
10	pr1_pdi_wd_exp_pend	PRU_ICSSG1 IEP0
9	pr1_pd_wd_exp_pend	PRU_ICSSG1 IEP0
8	pr1_digio_event_req	PRU_ICSSG1 IEP0
7	pr1_iep_tim_cap_cmp_pend	PRU_ICSSG1 IEP0
6	pr1_uart0_uint_intr_req	PRU_ICSSG1 UART0
5	pr1_uart0_utxevt_intr_req	PRU_ICSSG1 UART0
4	pr1_uart0_urxevt_intr_req	PRU_ICSSG1 UART0

Table 6-113. PRU_ICSSG0 and PRU_ICSSG1 Internal Interrupts (continued)

Event Number	PRU_ICSSG Internal Interrupt Signal	Source
3	pr1_rst_reset_iso_req	PRU_ICSSG1 Reset Isolation Requested
2	pr1_pru1_r31_status_cnt16	PRU_ICSSG1 PRU1 (Shift Capture)
1	pr1_pru0_r31_status_cnt16	PRU_ICSSG1 PRU0 (Shift Capture)
0	pr1_ecc_err_intr	PRU_ICSSG1 ECC Logic

The IRQ input lines 64 through 159 receive interrupts which come from various device peripherals located outside PRU_ICSSG system. They are delivered on the PRU_ICSSG Interrupt Controller inputs (64 through 159).

6.4.8 PRU_ICSSG UART Module

This section describes an Universal Asynchronous Receive and Transmit (UART) module integrated into each of the PRU_ICSSG subsystems, named respectively - PRU_ICSSG0_UART0 and PRU_ICSSG1_UART0. Hereinafter the module will be referred as PRU_ICSSG UART0.

6.4.8.1 PRU_ICSSG UART Overview

The PRU_ICSSG UART0 peripheral is based on the industry standard TL16C550 asynchronous communications element, which in turn is a functional upgrade of the TL16C450. The information in this chapter assumes that user is familiar with these standards.

Functionally similar to the TL16C450 on power up (single character or TL16C450 mode), the PRU_ICSSG UART0 can be placed in an alternate FIFO (TL16C550) mode. This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO.

The PRU_ICSSG UART0 performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. The CPU can read the PRU_ICSSG UART0 status at any time. The PRU_ICSSG UART0 includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The PRU_ICSSG UART0 includes a programmable baud generator capable of dividing the PRU_ICSSG UART0 input clock by divisors from 1 to 65535 and producing a 16× reference clock or a 13× reference clock for the internal transmitter and receiver logic.

6.4.8.2 PRU_ICSSG UART Environment

This section describes the PRU_ICSSG UART0 module interface to the device environment.

6.4.8.2.1 PRU_ICSSG UART Pin Multiplexing

Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. For more information on the PRU_ICSSG UART0 pin multiplexing, refer to the *Pad Configuration Registers* in the *CTRL_MMR0* chapter.

6.4.8.2.2 PRU_ICSSG UART Signal Descriptions

The PRU_ICSSG UART0 utilize a minimal number of signal connections to interface with external devices. The PRU_ICSSG UART0 signal descriptions are described in Table 6-114.

Table 6-114. PRUSS_UART0 Signal Descriptions

Signal Name	Signal Type	Function
UART0_TXD	Output	Serial data transmit
UART0_RXD	Input	Serial data receive
$\overline{\text{UART0\_CTS}}$	Input	Clear-to-Send handshaking signal
$\overline{\text{UART0\_RTS}}$	Output	Request-to-Send handshaking signal

6.4.8.2.3 PRU_ICSSG UART Protocol Description and Data Format

6.4.8.2.3.1 PRU_ICSSG UART Transmission Protocol

The PRU_ICSSG UART0 transmitter section includes a transmitter hold register (THR), memory mapped in the register ICSS_G_PR1_ICSS_UART_UART_SLV_THR[7-80] DATA bitfield and a transmitter shift register (TSR), which is NOT memory mapped. When the PRU_ICSSG UART0 is in the FIFO mode, THR is a 16-byte FIFO. Transmitter section control is a function of the PRU_ICSSG UART0 line control register ICSS_G_PR1_ICSS_UART_UART_SLV_LCR. Based on the settings chosen in this register, the PRU_ICSSG UART0 transmitter sends the following to the receiving device:

- 1 START bit
- 5, 6, 7, or 8 data bits
- 1 PARITY bit (optional)

- 1, 1.5, or 2 STOP bits

THR receives data from the internal data bus, and when TSR (transmitter shift register) is ready, the PRU_ICSSG UART0 moves the data from THR to TSR. The PRU_ICSSG UART0 serializes the data in TSR and transmits the data on the UART0_TXD pin.

In the non-FIFO mode, if THR is empty and the Transmitter Holding Register Empty interrupt (THRE) is enabled in the interrupt enable register (ICSS_G_PR1_ICSS_UART_UART_SLV_IER[1] ETBEI), an interrupt is generated. This interrupt is cleared when a character is loaded into THR or the interrupt identification register ICSS_G_PR1_ICSS_UART_UART_SLV_IIR bitfield [3-1] IIR_INTID is read. In the FIFO mode, the interrupt is generated when the transmitter FIFO is empty, and it is cleared when at least one byte is loaded into the FIFO or ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[3-1] IIR_INTID bitfield is read.

6.4.8.2.3.2 PRU_ICSSG UART Reception Protocol

The PRU_ICSSG UART0 receiver section includes a receiver shift register (RSR), that is not memory mapped, and a receiver buffer register (RBR), memory mapped as the register ICSS_G_PR1_ICSS_UART_UART_SLV_RBR[7-0] DATA bitfield. When the PRU_ICSSG UART0 is in the FIFO mode, RBR is a 16-byte FIFO. Receiver section control is a function of the PRU_ICSSG UART0 line control register - ICSS_G_PR1_ICSS_UART_UART_SLV_LCR. Based on the settings chosen in this register, the PRU_ICSSG UART0 receiver accepts the following from the transmitting device:

- 1 START bit
- 5, 6, 7, or 8 data bits
- 1 PARITY bit (optional)
- 1 STOP bit (any other STOP bits transferred with the above data are not detected)

RSR receives the data bits from the UART0_RXD pin. Then RSR concatenates the data bits and moves the resulting value into RBR (or the receiver FIFO), accessible in the RBR_TBR[7-0] RBR_DATA register bitfield. The PRU_ICSSG UART0 also stores three bits of error status information next to each received character, to record a parity error, framing error, or break.

In the non-FIFO mode, when a character is placed in RBR and the receiver data available interrupt is enabled in the interrupt enable register - ICSS_G_PR1_ICSS_UART_UART_SLV_IER[0] ERBI, an interrupt is generated. This interrupt is cleared when the character is read from RBR. In the FIFO mode, the interrupt is generated when the FIFO is filled to the trigger level selected in the FIFO control MSB part of the register ICSS_G_PR1_ICSS_UART_UART_SLV_IIR, and it is cleared when the FIFO contents drop below the trigger level.

6.4.8.2.3.3 PRU_ICSSG UART Data Format

The PRU_ICSSG UART0 transmits in the following format:

1 START bit + data bits (5, 6, 7, 8) + 1 PARITY bit (optional) + STOP bit (1, 1.5, 2)

It transmits 1 START bit; 5, 6, 7, or 8 data bits, depending on the data width selection; 1 PARITY bit, if parity is selected; and 1, 1.5, or 2 STOP bits, depending on the STOP bit selection.

The PRU_ICSSG UART0 receives in the following format:

1 START bit + data bits (5, 6, 7, 8) + 1 PARITY bit (optional) + 1 STOP bit

It receives 1 START bit; 5, 6, 7, or 8 data bits, depending on the data width selection; 1 PARITY bit, if parity is selected; and 1 STOP bit.

The protocol formats are shown in Figure 6-63.

Figure 6-63. PRU_ICSSG UART Protocol Formats

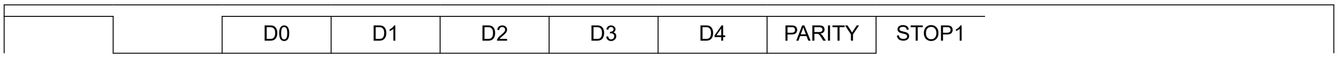

Transmit/Receive for 5-bit data, parity Enable, 1 STOP bit

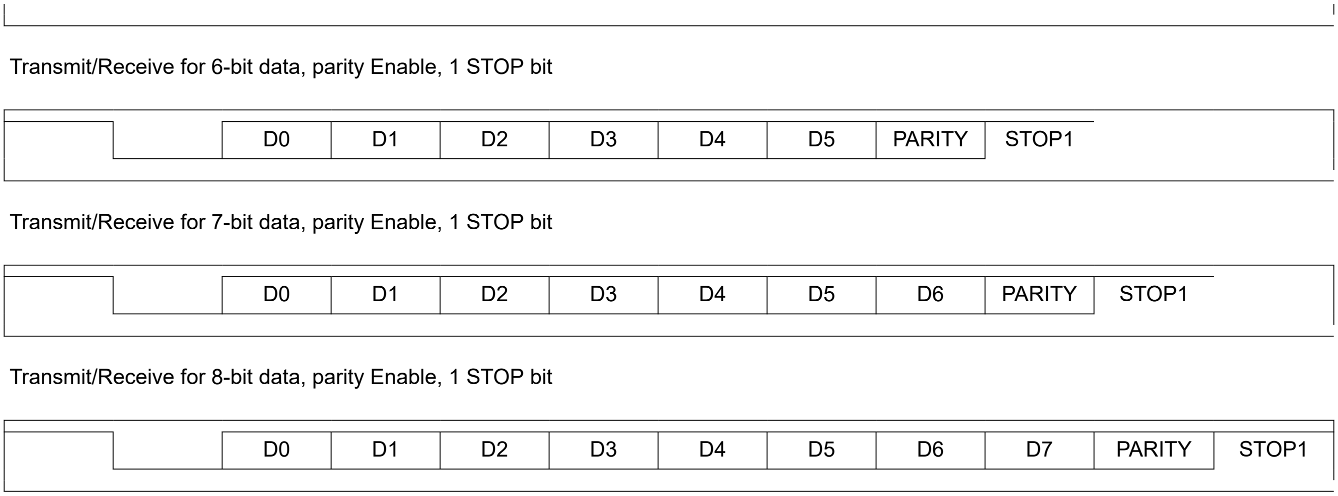
Transmit/Receive for 6-bit data, parity Enable, 1 STOP bit

Transmit/Receive for 7-bit data, parity Enable, 1 STOP bit

Transmit/Receive for 8-bit data, parity Enable, 1 STOP bit

6.4.8.2.3.3.1 Frame Formatting

Character length is specified using the ICSS_G_PR1_ICSS_UART_UART_SLV_LCR[0] WLS0 and ICSS_G_PR1_ICSS_UART_UART_SLV_LCR[1] WLS1 bits (see Table 6-116).

The number of stop-bits is specified using the ICSS_G_PR1_ICSS_UART_UART_SLV_LCR[2] STB bit (see Table 6-116).

The parity bit is programmed using the ICSS_G_PR1_ICSS_UART_UART_SLV_LCR[5] SP, ICSS_G_PR1_ICSS_UART_UART_SLV_LCR[4] EPS, and ICSS_G_PR1_ICSS_UART_UART_SLV_LCR[3] PEN bits (see Table 6-115).

Table 6-116. Relationship Between SP, EPS, and PEN Bits in LCTR

SP Bit	EPS Bit	PEN Bit	Parity Option
x	x	0	Parity disabled: No PARITY bit is transmitted or checked.
0	0	1	Odd parity selected: Odd number of logic 1s.
0	1	1	Even parity selected: Even number of logic 1s.
1	0	1	Stick parity selected with PARITY bit transmitted and checked as set.
1	1	1	Stick parity selected with PARITY bit transmitted and checked as cleared.

Table 6-117. Number of STOP Bits Generated

STB Bit	WLS Bit	Word Length Selected with WLS Bits	Number of STOP Bits Generated	Baud Clock (BCLK) Cycles
0	x	Any word length	1	16
1	0h	5 bits	1.5	24
1	1h	6 bits	2	32
1	2h	7 bits	2	32
1	3h	8 bits	2	32

6.4.8.2.4 PRU_ICSSG UART Clock Generation and Control

The PRU_ICSSG UART0 bit clock is derived from an input clock to the PRU_ICSSG UART0. See the device-specific Datasheet to check the maximum data rate supported by the PRU_ICSSG UART0.

Figure 6-64 is a conceptual clock generation diagram for the PRU_ICSSG UART0. The processor clock generator receives a signal from an external clock source and produces a PRU_ICSSG UART0 input clock with a programmed frequency. The PRU_ICSSG UART0 contains a programmable baud generator that takes an input clock and divides it by a divisor in the range between 1 and (2^{16} - 1) to produce a baud clock (BCLK). The frequency of BCLK is sixteen times (16×) the baud rate (each received or transmitted bit lasts 16 BCLK cycles) or thirteen times (13×) the baud rate (each received or transmitted bit lasts 13 BCLK cycles). When the

PRU_ICSSG UART0 is receiving, the bit is sampled in the 8th BCLK cycle for 16× over sampling mode and on the 6th BCLK cycle for 13× over-sampling mode. The 16× or 13× reference clock is selected by configuring the mode definition register: ICSS_G_PR1_ICSS_UART_UART_SLV_MDR[0] OSM_SEL bit. The formula to calculate the divisor is:

$$\text{Divisor} = \frac{\text{UART input clock frequency}}{\text{Desired baud rate} \times 16} \qquad [\text{MODE.OSM\_SEL} = 0\text{h}]$$

icss-13

$$\text{Divisor} = \frac{\text{UART input clock frequency}}{\text{Desired baud rate} \times 13} \qquad [\text{MODE.OSM\_SEL} = 1\text{h}]$$

icss-14

Two 8-bit register fields:

- ICSS_G_PR1_ICSS_UART_UART_SLV_DLH[7-0] DLH
- ICSS_G_PR1_ICSS_UART_UART_SLV_DLL[7-0] DLL,

called divisor latches, hold this 16-bit divisor. DLH holds the most significant bits of the divisor, and DLL holds the least significant bits of the divisor. For information about these register fields, see the PRU_ICSSG UART0 register descriptions in the *PRU_UART_UART0 Registers*. These divisor latches must be loaded during initialization of the PRU_ICSSG UART0 in order to ensure desired operation of the baud generator. Writing to the divisor latches results in two wait states being inserted during the write access while the baud generator is loaded with the new value.

Figure 6-65 summarizes the relationship between the transferred data bit, BCLK, and the PRU_ICSSG UART0 input clock. Note that the timing relationship depicted in Figure 6-65 shows that each bit lasts for 16 BCLK cycles. This is in case of 16x over-sampling mode. For 13× over-sampling mode each bit lasts for 13 BCLK cycles.

Example baud rates and divisor values relative to a 150 MHz PRU_ICSSG UART0 input clock and 16× over-sampling mode are shown in Table 6-117.

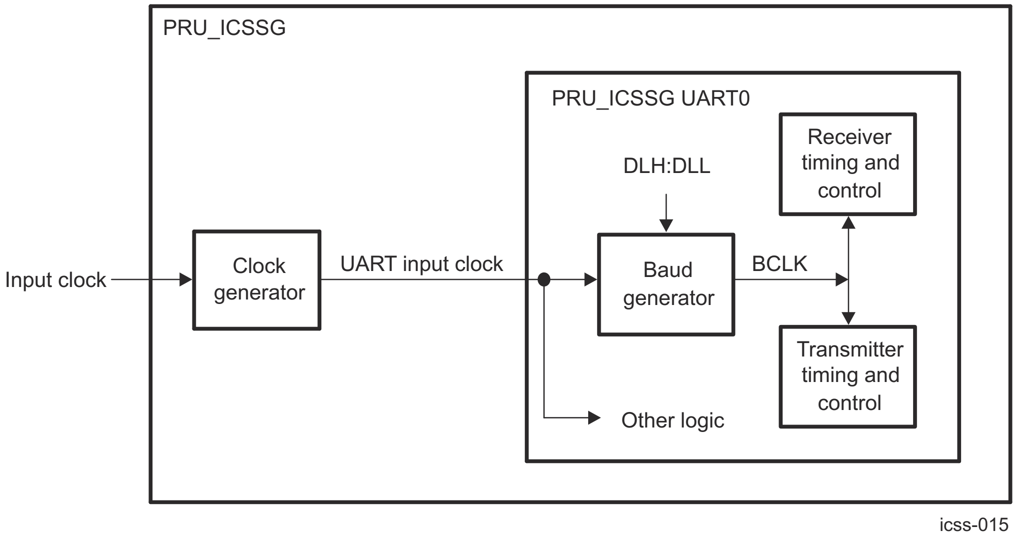

Figure 6-64. PRU_ICSSG UART Clock Generation Diagram

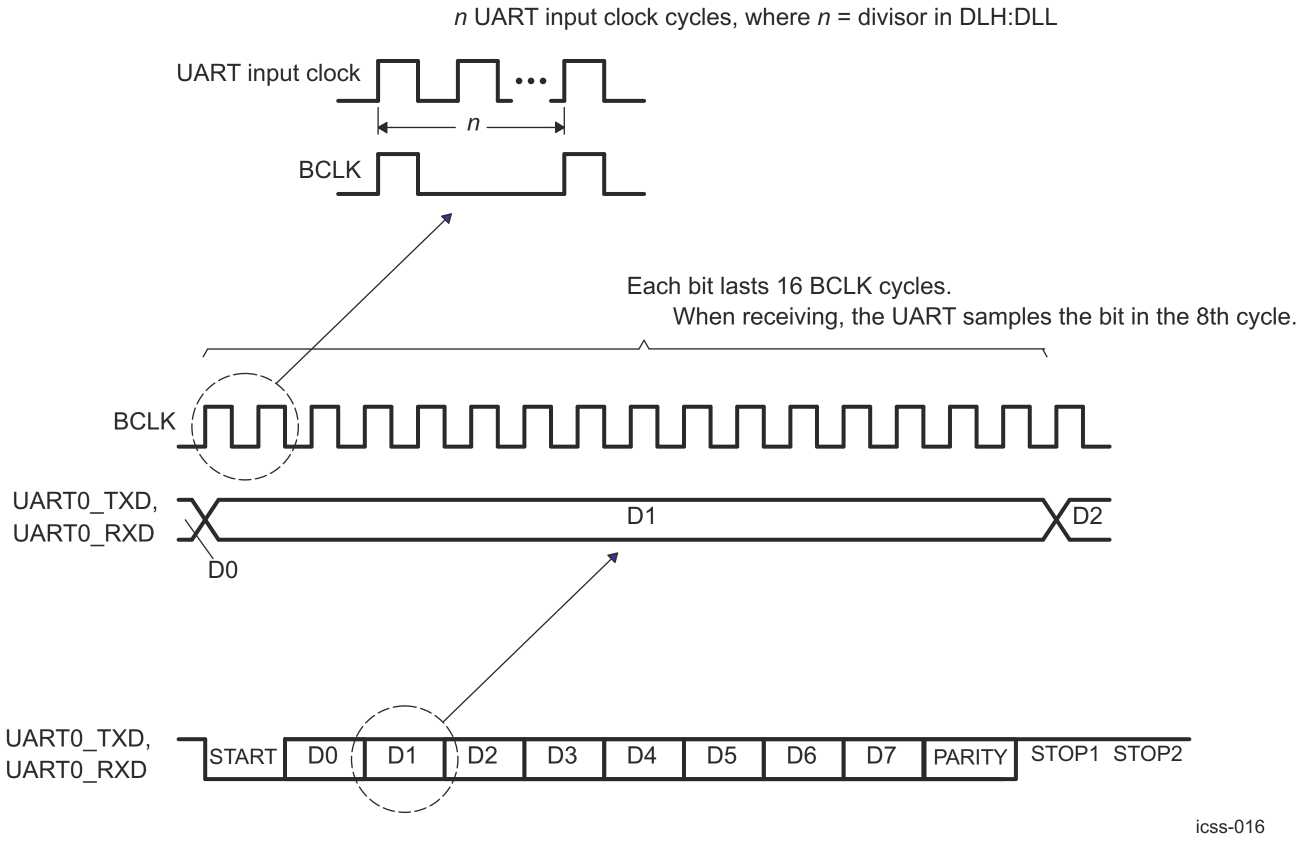

Figure 6-65. Relationships Between PRU_ICSSG UART Data Bit, BCLK, and Input Clock

Table 6-118. Baud Rate Examples for 192-MHZ PRU_ICSSG UART Input Clock and 16× Over-sampling Mode

Baud Rate	Divisor Value	Actual Baud Rate	Error (%)
2400	5000	2400	0.00
4800	2500	4800	0.00
9600	1250	9600	0.00
19200	625	19200	0.00
38400	313	38338.658	–0.16
56000	214	56074.766	0.13
115200	104	115384.6	0.16
128000	94	127659.574	–0.27
3000000	4	3000000	0.00
6000000	2	3000000	0.00
12000000	1	12000000	0.00

Table 6-119. Baud Rate Examples for 192-MHZ PRU_ICSSG UART Input Clock and 13× Over-sampling Mode

Baud Rate	Divisor Value	Actual Baud Rate	Error (%)
2400	6154	2399.940	–0.0025
4800	3077	4799.880	–0.0025
9600	1538	9602.881	0.03
19200	769	19205.762	0.03
38400	385	38361.638	–0.10

Table 6-119. Baud Rate Examples for 192-MHZ PRU_ICSSG UART Input Clock and 13× Over-sampling Mode (continued)

Baud Rate	Divisor Value	Actual Baud Rate	Error (%)
56000	264	55944.056	–0.10
115200	128	115384.6	0.16
128000	115	128428.094	0.33

6.4.8.3 PRU_ICSSG UART Functional Description

6.4.8.3.1 PRU_ICSSG UART Functional Block Diagram

A functional block diagram of the PRU_ICSSG UART0 is shown in Figure 6-66.

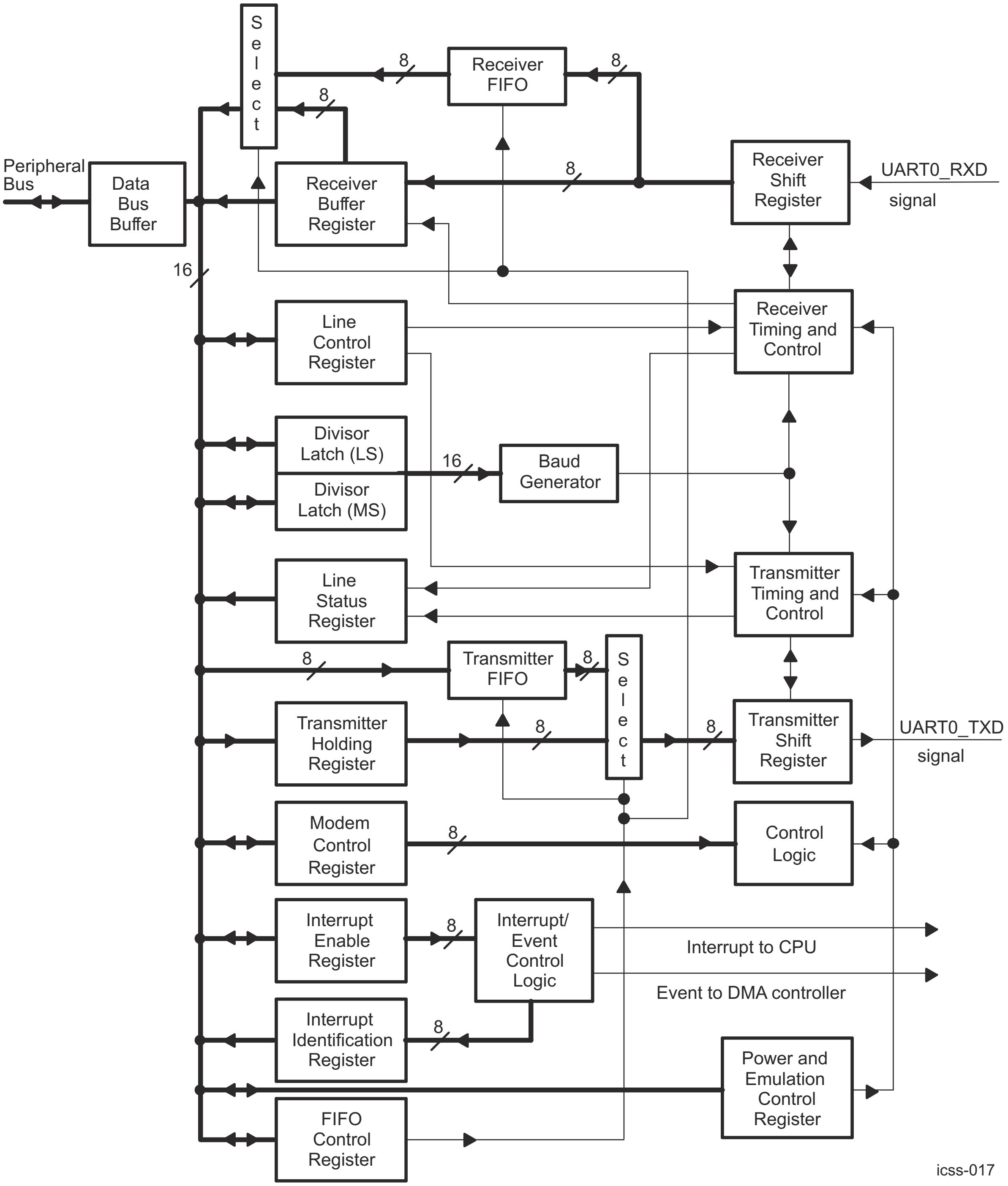

Note

NOTE: The value *n* indicates the applicable UART where there are multiple instances. For the PRU_ICSSG, there is only one instance and all UART signals should reflect this (e.g., UART0_TXD instead of UARTn_TXD).

Figure 6-66. PRU_ICSSG UART Block Diagram

6.4.8.3.2 PRU_ICSSG UART Reset Considerations

6.4.8.3.2.1 PRU_ICSSG UART Software Reset Considerations

Two bits in the power and emulation management register - ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT, control resetting the parts of the PRU_ICSSG UART0:

- The bit [14]UTRST controls resetting the transmitter only. If bit [14]UTRST = 1h, the transmitter is enabled and active;
  if bit [14]UTRST = 0h, the transmitter is disabled and in reset state.
- The bit [13]URRST controls resetting the receiver only. If [13]URRST = 1h, the receiver is enabled and active; if bit [13]URRST = 0h, the receiver is disabled and in reset state.

In each case, putting the receiver and/or transmitter in reset will reset the state machine of the affected portion but will not affect the PRU_ICSSG UART0 registers.

6.4.8.3.2.2 PRU_ICSSG UART Hardware Reset Considerations

When the processor RESET pin is asserted, the entire processor is reset and is held in the reset state until the RESET pin is released. As part of a device reset, the PRU_ICSSG UART0 state machine is reset and the PRU_ICSSG UART0 registers are forced to their default states. The default states of the registers are shown in .

6.4.8.3.3 PRU_ICSSG UART Power Management

The PRU_ICSSG UART0 peripheral can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the PRU_ICSSG UART0 peripheral and other PRU_ICSSG peripherals is controlled by the device Power Sleep Controller (PSC). The PSC acts as a controller for power management for all of the peripherals on the device. For more details on the power management procedures using the PSC, refer to the *Power Management.*

6.4.8.3.4 PRU_ICSSG UART Interrupt Support

6.4.8.3.4.1 PRU_ICSSG UART Interrupt Events and Requests

The PRU_ICSSG UART0 generates the interrupt requests described in Table 6-119. All requests are multiplexed through an arbiter to a single PRU_ICSSG UART0 interrupt request to the CPU, as shown in Figure 6-67. Each of the interrupt requests has an enable bit in the interrupt enable register (IER) - ICSS_G_PR1_ICSS_UART_UART_SLV_IER and is recorded in [3-1]IIR_INTID bitfield of ICSS_G_PR1_ICSS_UART_UART_SLV_IIR register.

If an interrupt occurs and the corresponding enable bit is set to 1h, the interrupt request is recorded in corresponding ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[3-1] IIR_INTID bitfield and is forwarded to the CPU. If an interrupt occurs and the corresponding enable bit is cleared to 0h, the interrupt request is blocked. The interrupt request is neither recorded in ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[3-1] IIR_INTID, nor forwarded to the CPU.

6.4.8.3.4.2 PRU_ICSSG UART Interrupt Multiplexing

The PRU_ICSSG UART0 have dedicated interrupt signals to the CPU and the interrupts are not multiplexed with any other interrupt source.

Table 6-120. PRU_ICSSG UART Interrupt Requests Descriptions

PRU_ICSSG UART0 Interrupt Request	Interrupt Source	Comment
THREINT	THR-empty condition: The transmitter holding register (THR) or the transmitter FIFO is empty. All of the data has been copied from THR, (i.e. ICSS_G_PR1_ICSS_UART_UART_SLV_RBR[7-0] DATA) to the transmitter shift register (TSR).	If THREINT is enabled in ICSS_G_PR1_ICSS_UART_UART_SLV_IER register by setting the [1]ETBEI bit, it is recorded in [3-1]IIR_INTID bitfield. As an alternative to using THREINT, the CPU can poll the THRE bit in the line status register ICSS_G_PR1_ICSS_UART_UART_SLV_LSR.

Table 6-120. PRU_ICSSG UART Interrupt Requests Descriptions (continued)

PRU_ICSSG UART0 Interrupt Request	Interrupt Source	Comment
RDAINT	Receive data available in non-FIFO mode or trigger level reached in the FIFO mode.	If RDAINT is enabled in ICSS_G_PR1_ICSS_UART_UART_SLV_IER register, by setting the [0]ERBI bit, it is recorded in INTID bitfield. As an alternative to using RDAINT, the CPU can poll the [0]DR bit in the line status register ICSS_G_PR1_ICSS_UART_UART_SLV_LSR. In the FIFO mode, this is not a functionally equivalent alternative because the [0]DR bit does not respond to the FIFO trigger level. The [0]DR bit only indicates the presence or absence of unread characters.
RTOINT	Receiver time-out condition (in the FIFO mode only): No characters have been removed from or input to the receiver FIFO during the last four character times (see Table 6-121), and there is at least one character in the receiver FIFO during this time.	The receiver time-out interrupt prevents the PRU_ICSSG UART0 from waiting indefinitely, in the case when the receiver FIFO level is below the trigger level and thus does not generate a receiver data-ready interrupt. If RTOINT is enabled in ICSS_G_PR1_ICSS_UART_UART_SLV_IER register, by setting the [0]ERBI bit, it is recorded in ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[3-1] IIR_INTID bitfield. There is no status bit to reflect the occurrence of a time-out condition.
RLSINT	Receiver line status condition: An overrun error, parity error, framing error, or break has occurred.	If RLSINT is enabled in INT_EN register, by setting the [2]ELSI bit, it is recorded in ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[3-1] IIR_INTID bitfield. As an alternative to using RLSINT, the CPU can poll the following bits in the line status register ICSS_G_PR1_ICSS_UART_UART_SLV_LSR: overrun error indicator (bit [1]OE), parity error indicator (bit [2]PE), framing error indicator ([3]FE), and break indicator ([4]BI).

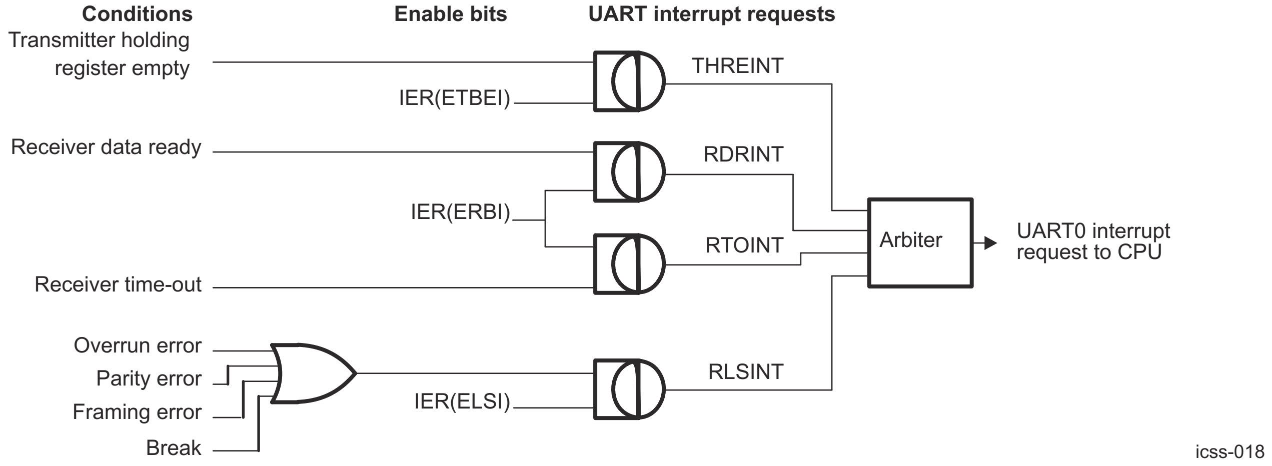

Figure 6-67. PRU_ICSSG UART Interrupt Request Enable Paths

6.4.8.3.5

Table 6-121. Interrupt Identification and Interrupt Clearing Information

Priority Level	IIR Bits				Interrupt Type	Interrupt Source	Event That Clears Interrupt
	3	2	1	0			
None	0	0	0	1	None	None	None
1	0	1	1	0	Receiver line status	Overrun error, parity error, framing error, or break is detected.	For an overrun error, reading the line status register ICSS_G_PR1_ICSS_UART_UART_SLV_LSR, clears the interrupt. For a parity error, framing error, or break, the interrupt is cleared only after all the erroneous data have been read.
2	0	1	0	0	Receiver data-ready	Non-FIFO mode: Receiver data is ready.	Non-FIFO mode: The receiver buffer register (RBR) is read.
						FIFO mode: Trigger level reached. If four character times pass with no access of the FIFO, the interrupt is asserted again.	FIFO mode: The FIFO drops below the trigger level. (1)
2	1	1	0	0	Receiver time-out	FIFO mode only: No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in the receiver FIFO during this time.	One of the following events: • A character is read from the receiver FIFO (1) • A new character arrives in the receiver FIFO • The [13]URRST bit in the power and emulation management register (ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT) is loaded with 0h.
3	0	0	1	0	Transmitter holding register empty	Non-FIFO mode: Transmitter holding register (THR) is empty. FIFO mode: Transmitter FIFO is empty.	A character is written to the transmitter holding register (ICSS_G_PR1_ICSS_UART_UART_SLV_THR) or the interrupt identification register (ICSS_G_PR1_ICSS_UART_UART_SLV_IIR) is read.

(1) In the FIFO mode, the receiver data-ready interrupt or receiver time-out interrupt is cleared by the CPU or by the DMA controller, whichever reads from the receiver FIFO first.

6.4.8.3.6 PRU_ICSSG UART DMA Event Support

In the FIFO mode, the PRU_ICSSG UART0 generates the following two DMA events:

- **Receive event (URXEVT):** The trigger level for the receiver FIFO (1, 4, 8, or 14 characters) is set with the FIFO control ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[7-6] IIR_FIFOEN bitfield. Every time the trigger level is reached or a receiver time-out occurs, the PRU_ICSSG UART0 sends a receive event to the DMA controller. In response, the DMA controller reads the data from the receiver FIFO by way of the receiver buffer register ICSS_G_PR1_ICSS_UART_UART_SLV_RBR[7-0] DATA. Note that the receive event is not asserted if the data at the top of the receiver FIFO is erroneous even if the trigger level has been reached.
- **Transmit event (UTXEVT):** When the transmitter FIFO is empty (when the last byte in the transmitter FIFO has been copied to the transmitter shift register), the PRU_ICSSG UART0 sends an UTXEVT signal to the DMA controller. In response, the DMA controller refills the transmitter FIFO by way of the transmitter holding register (THR) - ICSS_G_PR1_ICSS_UART_UART_SLV_RBR[7-0] DATA. The UTXEVT signal is also sent to the DMA controller when the PRU_ICSSG UART0 is taken out of reset using the [14]UTRST bit in the power and emulation management register (ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT).

Activity in DMA channels can be synchronized to these events. In the non-FIFO mode, the PRU_ICSSG UART0 generates no DMA events. Any DMA channel synchronized to either of these events must be enabled at the time the PRU_ICSSG UART0 event is generated. Otherwise, the DMA channel will miss the event and, unless the PRU_ICSSG UART0 generates a new event, no data transfer will occur.

6.4.8.3.7 PRU_ICSSG UART Operations

6.4.8.3.7.1 PRU_ICSSG UART FIFO Modes

The following two modes can be used for servicing the receiver and transmitter FIFOs:

- FIFO interrupt mode. The FIFO is enabled and the associated interrupts are enabled. Interrupts are sent to the CPU to indicate when specific events occur.

- FIFO poll mode. The FIFO is enabled but the associated interrupts are disabled. The CPU polls status bits to detect specific events.

Because the receiver FIFO and the transmitter FIFO are controlled separately, either one or both can be placed into the interrupt mode or the poll mode.

6.4.8.3.7.1.1 PRU_ICSSG UART FIFO Interrupt Mode

When the receiver FIFO is enabled in the FIFO control register (FCR), mapped in the MSB part of the register ICSS_G_PR1_ICSS_UART_UART_SLV_IIR, and the receiver interrupts are enabled in the interrupt enable register ICSS_G_PR1_ICSS_UART_UART_SLV_IER, the interrupt mode is selected for the receiver FIFO. The following are important points about the receiver interrupts:

- The receiver data-ready interrupt is issued to the CPU when the FIFO has reached the trigger level that is programmed in FCR. It is cleared when the CPU or the DMA controller reads enough characters from the FIFO such that the FIFO drops below its programmed trigger level.
- The receiver line status interrupt is generated in response to an overrun error, a parity error, a framing error, or a break. This interrupt has higher priority than the receiver data-ready interrupt. For details, see Section 6.4.8.3.4 .
- The data-ready ([0]DR) bit in the line status register - ICSS_G_PR1_ICSS_UART_UART_SLV_LSR, indicates the presence or absence of characters in the receiver FIFO. The [0]DR bit is set when a character is transferred from the receiver shift register (RSR) to the empty receiver FIFO. The [0]DR bit remains set until the FIFO is empty again.
- A receiver time-out interrupt occurs if all of the following conditions exist:
  - At least one character is in the FIFO,
  - The most recent character was received more than four continuous character times ago. A character time is the time allotted for 1 START bit, *n* data bits, 1 PARITY bit, and 1 STOP bit, where *n* depends on the word length selected with the WLS0 and WLS1 bits of the line control register ICSS_G_PR1_ICSS_UART_UART_SLV_LCR. See Table 6-121.
  - The most recent read of the FIFO has occurred more than four continuous character times before.
- Character times are calculated by using the baud rate.
- When a receiver time-out interrupt has occurred, it is cleared and the time-out timer is cleared when the CPU or the EDMA controller reads one character from the receiver FIFO. The interrupt is also cleared if a new character is received in the FIFO or if the URRST bit is cleared in the power and emulation management register - PWM.
- If a receiver time-out interrupt has not occurred, the time-out timer is cleared after a new character is received or after the CPU or EDMA reads the receiver FIFO.

When the transmitter FIFO is enabled in ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[0] IIR_IPEND bit and the transmitter holding register empty (THRE) interrupt is enabled in ICSS_G_PR1_ICSS_UART_UART_SLV_IER[1] ETBEI bit, the interrupt mode is selected for the transmitter FIFO. The THRE interrupt occurs when the transmitter FIFO is empty. It is cleared when the transmitter hold register (THR) ICSS_G_PR1_ICSS_UART_UART_SLV_RBR[7-0] DATA bitfield is loaded (1 to 16 characters may be written to the transmitter FIFO while servicing this interrupt) or the [3-1]IIR_INTID bitfield is read in the interrupt identification register ICSS_G_PR1_ICSS_UART_UART_SLV_IIR.

Table 6-122. Character Time for Word Lengths

Word Length (*n*)	Character Time	Four Character Times
5	Time for 8 bits	Time for 32 bits
6	Time for 9 bits	Time for 36 bits
7	Time for 10 bits	Time for 40 bits
8	Time for 11 bits	Time for 44 bits

6.4.8.3.7.1.2 PRU_ICSSG UART FIFO Poll Mode

When the receiver FIFO is enabled in the FIFO control register (via setting the ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[0] IIR_IPEND to 1h) and the receiver interrupts are disabled in the interrupt enable register (ICSS_G_PR1_ICSS_UART_UART_SLV_IER), the poll mode is selected for the receiver FIFO. Similarly, when the transmitter FIFO is enabled via setting the same bit (ICSS_G_PR1_ICSS_UART_UART_SLV_IIR[0] IIR_IPEND to 1h) and the transmitter interrupts are disabled, the transmitted FIFO is in the poll mode. In the poll mode, the CPU detects events by checking bits in the line status register - ICSS_G_PR1_ICSS_UART_UART_SLV_LSR:

- The ICSS_G_PR1_ICSS_UART_UART_SLV_LSR[7] RXFIFOE bit indicates whether there are any errors in the receiver FIFO.
- The ICSS_G_PR1_ICSS_UART_UART_SLV_LSR[6] TEMT bit indicates that both the transmitter holding register (THR) and the transmitter shift register (TSR) are empty.
- The ICSS_G_PR1_ICSS_UART_UART_SLV_LSR[5] THRE bit indicates when THR (mapped in the ICSS_G_PR1_ICSS_UART_UART_SLV_RBR[7-0] DATA bitfield) is empty.
- The following line status register - ICSS_G_PR1_ICSS_UART_UART_SLV_LSR bits specify which error or errors have occurred:
  - ICSS_G_PR1_ICSS_UART_UART_SLV_LSR[4] BI - Break Interrupt
  - ICSS_G_PR1_ICSS_UART_UART_SLV_LSR[3] FE – Framing Error
  - ICSS_G_PR1_ICSS_UART_UART_SLV_LSR[2] PE – Parity Error
  - ICSS_G_PR1_ICSS_UART_UART_SLV_LSR[1] OE – Overrun Error
- The ICSS_G_PR1_ICSS_UART_UART_SLV_LSR[0] DR (data-ready) bit is set as long as there is at least one byte in the receiver FIFO.

Also, in the FIFO poll mode:

- The interrupt identification ([3-1] IIR_INTID) bit field in register ICSS_G_PR1_ICSS_UART_UART_SLV_IIR are not affected by any events because the interrupts are disabled.
- The PRU_ICSSG UART0 does not indicate when the receiver FIFO trigger level is reached or when a receiver time-out occurs.

6.4.8.3.7.2 PRU_ICSSG UART Autoflow Control

The PRU_ICSSG UART0 can employ autoflow control by connecting the UART0_CTS and UART0_RTS signals. The UART0_CTS input must be active before the transmitter FIFO can transmit data. The UART0_RTS becomes active when the receiver needs more data and notifies the sending device. When UART0_RTS is connected to UART0_CTS, data transmission does not occur unless the receiver FIFO has space for the data. Therefore, when two UARTs are connected as shown in Figure 6-68 with autoflow enabled (ICSS_G_PR1_ICSS_UART_UART_SLV_MCR[5] AFE = 1h), overrun errors are eliminated.

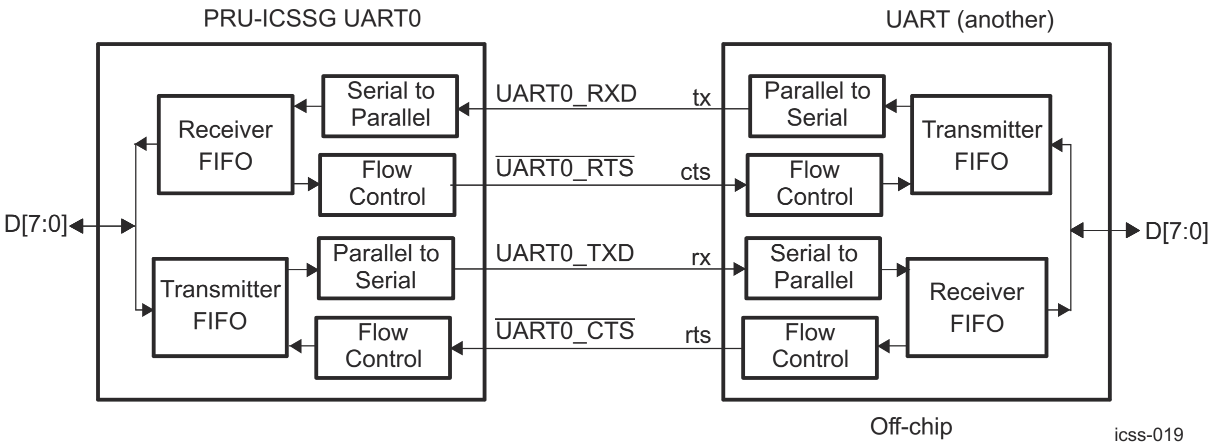

Figure 6-68. UART Interface Using Autoflow Diagram

6.4.8.3.7.2.1 PRU_ICSSG UART Signal UART0_RTS Behavior

UART0_RTS data flow control originates in the receiver block (see Figure 6-66). When the receiver FIFO level reaches a trigger level of 1, 4, 8, or 14 (see Figure 6-69), UART0_RTS is deasserted. The sending UART may send an additional byte after the trigger level is reached (assuming the sending UART has another byte to send), because it may not recognize the deassertion of UART0_RTS until after it has begun sending the additional byte. For trigger level 1, 4, and 8, UART0_RTS is automatically reasserted once the receiver FIFO is emptied. For trigger level 14, UART0_RTS is automatically reasserted once the receiver FIFO drops below the trigger level.

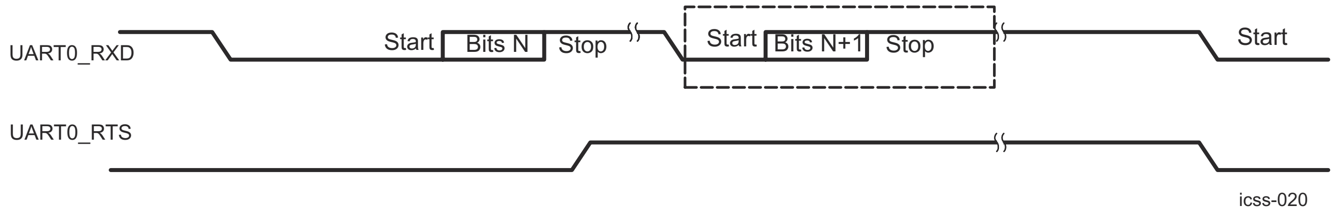

Note

N = Receiver FIFO trigger level.

Note

The two blocks in dashed lines cover the case where an additional byte is sent.

Figure 6-69. Autoflow Functional Timing Waveforms for UART0_RTS

6.4.8.3.7.2.2 PRU_ICSSG UART Signal UART0_CTS Behavior

The transmitter checks UART0_CTS before sending the next data byte. If UART0_CTS is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, UART0_CTS must be released before the middle of the last STOP bit that is currently being sent (see Figure 6-70). When flow control is enabled, UART0_CTS level changes do not trigger interrupts because the device automatically controls its own transmitter. Without autoflow control, the transmitter sends any data present in the transmitter FIFO and a receiver overrun error may result.

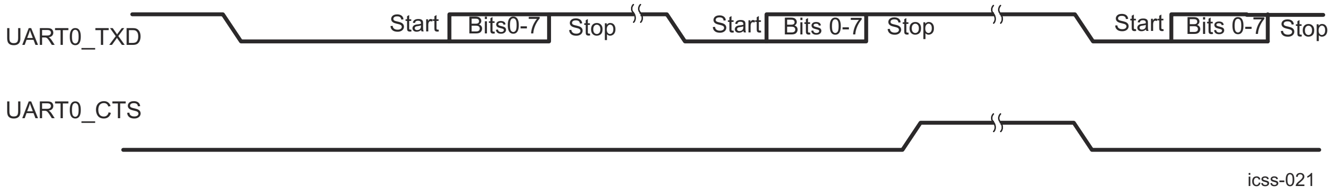

Note

When UART0_CTS is active (low), the transmitter keeps sending serial data out.

Note

When UART0_CTS goes high before the middle of the last STOP bit of the current byte, the transmitter finishes sending the current byte but it does not send the next byte.

Note

When UART0_CTS goes from high to low, the transmitter begins sending data again.

Figure 6-70. Autoflow Functional Timing Waveforms for UART0_CTS

6.4.8.3.7.3 PRU_ICSSG UART Loopback Control

The PRU_ICSSG UART0 can be placed in the diagnostic mode using the [4]LOOP bit in the modem control register - ICSS_G_PR1_ICSS_UART_UART_SLV_MCR, which internally connects the PRU_ICSSG UART0 output back to the PRU_ICSSG UART0's input. In this mode, the transmit and receive data paths, the transmitter and receiver interrupts, and the modem control interrupts can be verified without connecting to another UART.

6.4.8.3.8 PRU_ICSSG UART Emulation Considerations

The [0]FREE bit in the power and emulation management register (ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT) determines how the PRU_ICSSG UART0 responds to an emulation suspend event such as an emulator halt or breakpoint. If bit ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT[0] FREE = 0h and a transmission is in progress, the PRU_ICSSG UART0 halts after completing the one-word transmission; if bit ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT[0] FREE = 0h and a transmission is not in progress, the PRU_ICSSG UART0 halts immediately. If ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT[0] FREE = 1h, the PRU_ICSSG UART0 does not halt and continues operating normally.

Note also that most emulator accesses are transparent to PRU_ICSSG UART0 operation. Emulator read operations do not affect any register contents, status bits, or operating states, with the exception of the interrupt identification register (ICSS_G_PR1_ICSS_UART_UART_SLV_IIR). Emulator writes, however, may affect register contents and may affect PRU_ICSSG UART0 operation, depending on what register is accessed and what value is written.

The PRU_ICSSG UART0 registers can be read from or written to during emulation suspend events, even if the PRU_ICSSG activity has stopped.

6.4.8.3.9 PRU_ICSSG UART Exception Processing

6.4.8.3.9.1 PRU_ICSSG UART Divisor Latch Not Programmed

Since the processor reset signal has no effect on the divisor latch, the divisor latch will have an unknown value after power up. If the divisor latch is not programmed after power up, the baud clock (BCLK) will not operate and will instead be set to a constant logic 1 state.

The divisor latch values should always be reinitialized following a processor reset.

6.4.8.3.9.2 Changing Operating Mode During Busy Serial Communication of PRU_ICSSG UART

Since the serial link characteristics are based on how the control registers are programmed, the PRU_ICSSG UART0 module will expect the control registers to be static while it is busy engaging in a serial communication. Therefore, changing the control registers while the module is still busy communicating with another serial device will most likely cause an error condition and should be avoided.

6.4.9 PRU_ICSSG ECAP Module

6.4.9.1 PRU_ICSSG ECAP Functional Description

A single instance of an Enhanced Capture event module (ECAP0) is integrated in each device PRU_ICSSG0 and PRU_ICSSG1 subsystem.

For more details on the PRU_ICSSG0 and PRU_ICSSG1 ECAP0 I/O signals available at device level, refer to the *PRU_ICSSG Environment*.

For PRU_ICSSG0 and PRU_ICSSG1 ECAP0 integration details and functionalities, controlled at PRU_ICSSG top level (functional clock control, etc.), refer to the *PRU_ICSSG Integration* and the *PRU-ICSS Top Level Resources Functional Description*.

Note

The PRU_ICSSG0 and PRU_ICSSG1 ECAP0 "SYNC In" hardware event synchronization input and "SYNC Out" hardware synchronization output are implemented in the device PRU_ICSSG0 and PRU_ICSSG1 respectively. However, a software-forced synchronization via bit ECAP_ECCTL2_ECCTL1[24] SWSYNC, can be used as an alternative, provided that ECAP_ECCTL2_ECCTL1[21] SYNCI_EN bit is set to 1h.

For full description of the PRU_ICSSG0, PRU_ICSSG1 and PRU_ICSSG2 ECAP0 modules and functionalities, refer to the *Enhanced Capture (eCAP) Module.*

6.4.10 PRU_ICSSG PWM Module

Each of the PRU_ICSSG modules integrates one Pulse Width Modulation module (PWM). The PWM module uses IEP0 and IEP1 compare events to produce the PWM outputs.

6.4.10.1 PRU_ICSSG PWM Supported Features

PRU_ICSSG PWM module supports the following features:

- Supports up to 4 sets of 3 phased motor control with 12 primary and 12 complimentary programmable PWM outputs
- Very flexible Real Time options
  - Up to 9 events with optional external trip IO per PWM set with hardware glitch filter and programmable mask through ICSSG_PWMn[16-8] PWM0_TRIP_MASK (where n = 0 to 2)
  - Hardware compares from IO loopback with hardware glitch filter
  - Supports Sigma Delta (SD) fast detect circuit
- Very flexible PWM output behavior, configurable through state configuration registers: PWMn_0 to PWMn_2 (where n = 0 to 2):
  - Programmable Initial State
  - Programmable Trip State
  - Programmable Active State
- Hardware glitch filters can debounce a glitch from 1 to 255 ICSSG_CORE_CLK counts

Figure 6-71 and Figure 6-72 shows block diagrams of the PRU_ICSSG PWM.

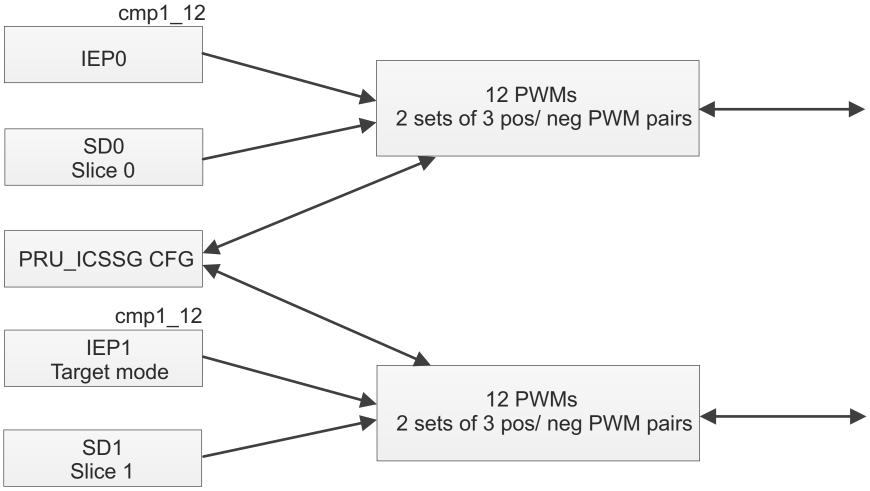

Figure 6-71. PRU_ICSSG PWM Block Diagram

Note

PRGn_PWMm_A[2:0] = PRGn_PWMm_[2:0]_POS and PRGn_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG.

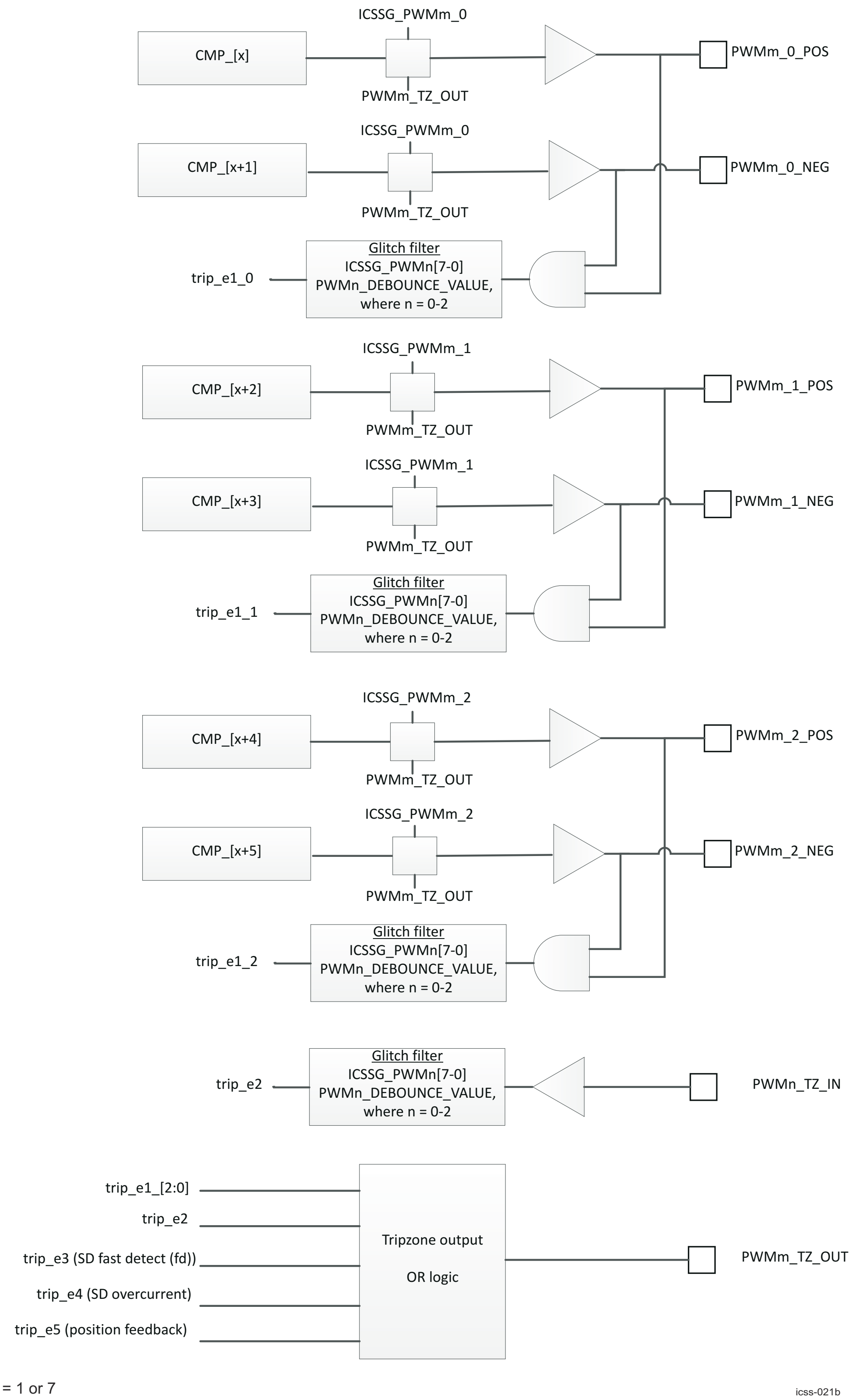

Figure 6-72. PRU_ICSSG PWM I/O Block Diagram

6.4.10.2 PRU_ICSSG PWM States Overview

The PWM module has three states (initial, active, and trip),which are shared between PRGn_PWMm_[2:0]_POS and PRGn_PWMm_[2:0]_NEG pins (where n = 0 to 2 and m = 0 to 3). The output value for each pin, however, is unique and is defined in the ICSSG CFG registers. Figure 6-73 shows the PWM module states.

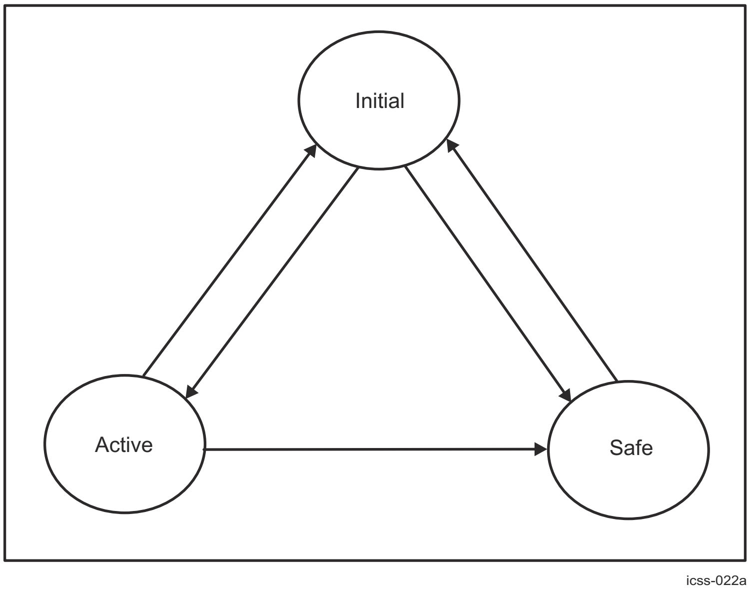

Figure 6-73. Three State Diagram

Each state supports different entry events. Table 6-122 shows a summary of the different entry options.

Table 6-123. Summary of Entry Events

State	Entry Event
Initial	• Hardware reset event • Trip reset event, ICSSG_PWMm[18] PWMm_TRIP_RESET (where m = 0 to 3) • IEP0.CMP0
Active	• CMPx event associated with the PWMm set (where m = 0 to 3), as shown in Table 6-124
Trip	• PRGn_PWM_m_TRIP_OUT (where n = 0 to 2 and m = 0 to 3) event of that PWMm set

Table 6-124. State Transition Mapping

Current State	Next State	Event causing transition
X	Initial	Hardware reset event
Trip	Initial	Trip reset event or IEP0.CMP0 (if enabled)
Active	Initial	Trip reset event or IEP0.CMP0 (if enabled)
Initial	Active	First CMPx event associated with the PWMm set
X	Safe	PRGn_PWM_m_TRIP_OUT (where n = 0 to 2 and m = 0 to 3) event

Table 6-125. PWM to IEP CMP Mapping

PWM	IEP CMP
PWM0_0_POS	IEP0 CMP1
PWM0_0_NEG	IEP0 CMP2
PWM0_1_POS	IEP0 CMP3
PWM0_1_NEG	IEP0 CMP4

Table 6-125. PWM to IEP CMP Mapping (continued)

PWM	IEP CMP
PWM0_2_POS	IEP0 CMP5
PWM0_2_NEG	IEP0 CMP6
PWM1_0_POS	IEP0 CMP7
PWM1_0_NEG	IEP0 CMP8
PWM1_1_POS	IEP0 CMP9
PWM1_1_NEG	IEP0 CMP10
PWM1_2_POS	IEP0 CMP11
PWM1_2_NEG	IEP0 CMP12
PWM2_0_POS	IEP1 CMP1
PWM2_0_NEG	IEP1 CMP2
PWM2_1_POS	IEP1 CMP3
PWM2_1_NEG	IEP1 CMP4
PWM2_2_POS	IEP1 CMP5
PWM2_2_NEG	IEP1 CMP6
PWM3_0_POS	IEP1 CMP7
PWM3_0_NEG	IEP1 CMP8
PWM3_1_POS	IEP1 CMP9
PWM3_1_NEG	IEP1 CMP10
PWM3_2_POS	IEP1 CMP11
PWM3_2_NEG	IEP1 CMP12

6.4.10.3 PRU_ICSSG PWM Trip State Logic

The trip logic is common for each set of PRGn_PWMm_[2:0]_POS and PRGn_PWMm_[2:0]_NEG pins (where n = 0 to 2 and m = 0 to 3). This logic is responsible for monitoring the “error” inputs and producing a PRGn_PWM_m_TRIP_OUT event, which is used to trip the I/O into a predefined trip state.

The I/O will remain in this trip state until the CMP0 event (if enabled) or trip software reset occurs. After clearing of these events (through ICSSG_PWM0[17] PWM0_TRIP_CMP0_EN bit or [18] PWMm_TRIP_RESET, where m = 0 to 3), then the I/Os will be in the initial state until the first IEP0/1_CMP_INTR_PEND_P[15:0] event occurs that corresponds to a particular PRGn_PWMm_[2:0]_POS or PRGn_PWMm_[2:0]_NEG set of pins. The first compare event occurrence corresponding to that PWMm set will cause all I/Os of that PWMm set to go into an active state. Subsequent compare events will cause the I/Os to toggle.

Note

The SoC pad is in default tristate and the internal weak pull-down resistor is enabled. Before PRU_ICSSG PWM to be exported, the software needs to execute initialization sequence along with the IEP0 and IEP1.

The following registers are used to configure the trip signals:

- ICSSG_PWM0
- ICSSG_PWM1
- ICSSG_PWM2
- ICSSG_PWM3

6.4.10.4 PRU_ICSSG PWM Glitch Filter

The glitch filter is a block which is used to reject pulses smaller than width, defined in the ICSSG_PWM0[7-0] PWMm_DEBOUNCE_VALUE. For example , if bit field [7-0] PWM0_DEBOUNCE_VALUE is set to 10h, a pulse which is less than 16 x ICSSG_CORE_CLK clock cycles will be filtered.

6.4.11 PRU_ICSSG MII_G_RT Module

6.4.11.1 PRU_ICSSG MII_G_RT Introduction

The Real-time Media Independent Interface (MII_G_RT) provides a programmable I/O interface for the PRUs to access and control up to two MII ports. The MII_G_RT module can also be configured to push and pull data independent of the PRU cores.

Note

In order to guarantee the MII_G_RT I/O timing values published in the device data sheet, the PRU_ICSSG ICSSGn_CORE_CLK (where n = 0 or 1) core clock must be configured for 200 MHz, 225 MHz or 250 MHz and the TX_CLK_DELAYn (where n = 0 or 1) bit field in the MII_RT_TXCFG0/1 register must be set to 0h (default value).

6.4.11.1.1 PRU_ICSSG MII_G_RT Features

The PRU_ICSSG MII_G_RT module supports:

- Two MII ports
  - Each MII port has:
    - 32-Bytes RX L1 FIFO
    - 64-Bytes RX L2 FIFO (two memory banks: Bank0 = 32-Bytes and Bank1 = 32-Bytes)
    - 40-Bytes TX L1 FIFO one per port
    - 64-Bytes TX L2 FIFO one per port
  - Rate decoupling on TX L1 FIFO
  - Configurable pre-amble removal on RX L1 FIFO and insertion on TX L1 FIFO
  - Sync frame delimiter detection
  - Configurable TX L1 FIFO trigger (10 bits with 40 ns ticks)
- MII port multiplexer per direction to support line/ring structure
  - Link detection through RX_ERR
- Cyclic redundancy check (CRC)
  - CRC32 generation on TX path
  - CRC32 checker on RX path

6.4.11.1.2 Unsupported Features

The PRU_ICSSG MII_G_RT module does not support:

- Auto padding in TX L1 FIFO
- Dynamic TX multiplexer switching during packet handling:
  - Can allow one PRU to handle both MII interfaces and a second PRU to manage the host and switch functions.

6.4.11.1.3 PRU_ICSSG MII_G_RT Block Diagram

Figure 6-74 shows the MII_G_RT in context of the PRU_ICSSG.

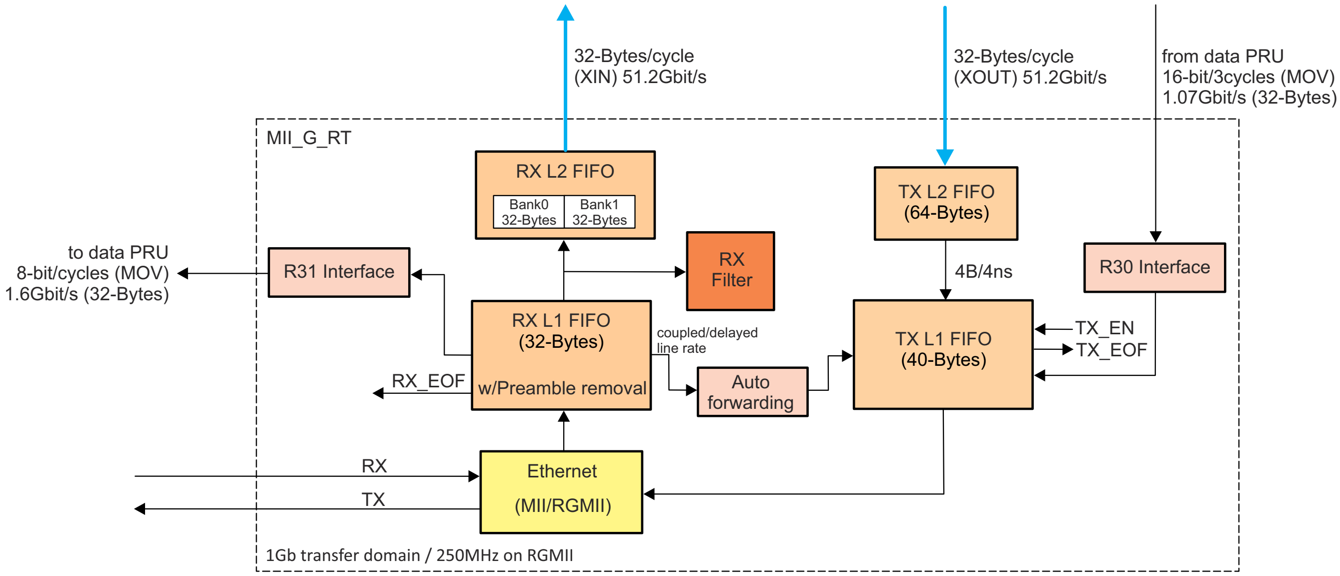

Figure 6-74. PRU_ICSSG MII_G_RT Block Diagram

6.4.11.2 MII_G_RT Functional Description

6.4.11.2.1 MII_G_RT Data Path Configuration

The MII_G_RT module supports three basic data path configurations. These configurations are compared in Table 6-125 and described in the following sections.

Table 6-126. MII_G_RT Data Path Configuration Comparison

Configuration	PRU Dependency	Data Servicing	Port-to-Port Latency
Auto-forward	Snoop only	One word in flight	Low
8- or 16-bit processing with on-the-fly modifications (RX L1)	Yes	One word or byte in flight	Low
32-byte double buffer or ping-pong processing (RX L2)	Yes	Multi-words in flight	Medium (application-dependent)

6.4.11.2.1.1 Auto-forward with Optional PRU Snoop

Data is automatically forwarded from the MII RX port to the MII TX port without manipulations, as shown in Figure 6-75. This configuration does not depend on the PRU core. However, it does support an option for PRU to snoop or monitor the received data through the RX L2, shown in Figure 6-76. The PRU does not access data and status bits through R31, and it does not modify and push data.

Figure 6-75. Auto-forward

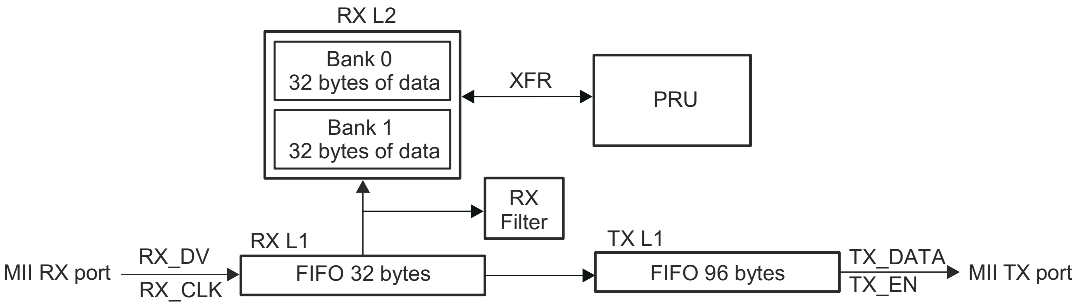

Figure 6-76. Auto-forward with PRU Snoop

6.4.11.2.1.2 8- or 16-bit Processing with On-the-Fly Modifications

This configuration services one byte or word in flight and has low latency. The PRU has the option to manipulate the received word and control popping data from the RX L1 FIFO and pushing it on the TX L1 FIFO.

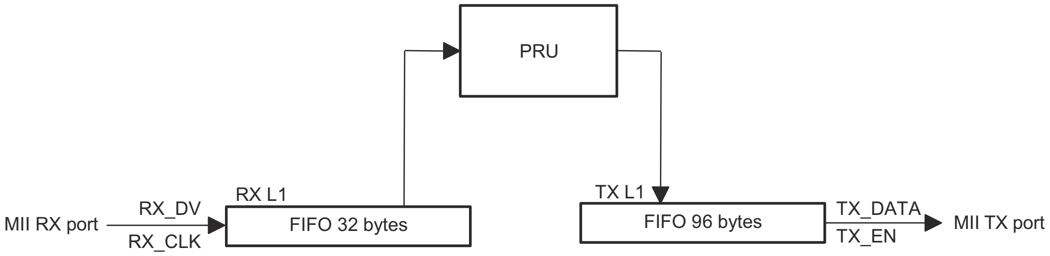

Figure 6-77. 8- or 16-bit Processing with On-the-Fly Modifications

6.4.11.2.1.3 32-byte Double Buffer or Ping-Pong Processing

This configuration supports high bandwidth, high efficiency transactions. Often implementations using this mode permit relaxed servicing requirements allowing the PRU to manipulate the received data before transmitting.

Data received in this configuration is passed into the RX L2 buffer. The PRU reads multiple bytes of data from one of the RX L2 banks through the high bandwidth broadside interface and XFR instructions. The PRU can then store or manipulate data before pushing it to the TX L1 FIFO for transmission on the MII TX port.

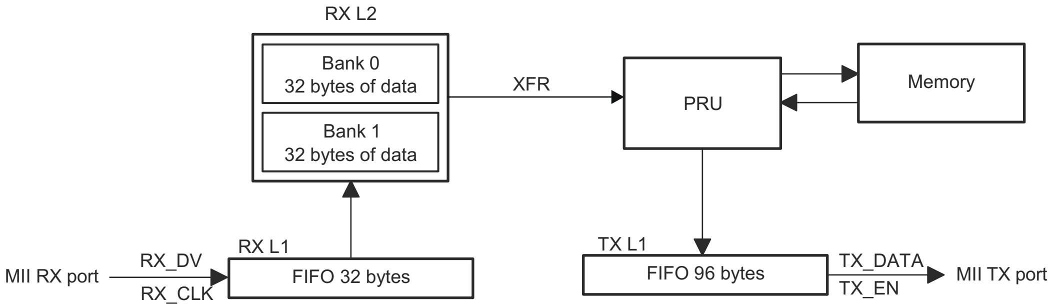

Figure 6-78. 32-byte Double Buffer or Ping-Pong Processing

6.4.11.2.2 MII_G_RT Definition and Terms

6.4.11.2.2.1 MII_G_RT Data Frame Structure

The data received and transmitted over MII conforms with the frame structure shown in Table 6-99.

Table 6-127. MII_G_RT Frame Structure

Inter-frame	Preamble	Start of Frame Delimiter (SFD)	Data	Cyclic Redundancy Check (CRC)

The data following the SFD is formatted in a 4-bit nibble structure. Figure 6-79 illustrates the nibble order. The MSB arriving first is on the LSB side of a nibble. When receiving data, the MII_G_RT receive logic will wait for the next nibble to arrive before constructing a byte and delivering to the PRU.

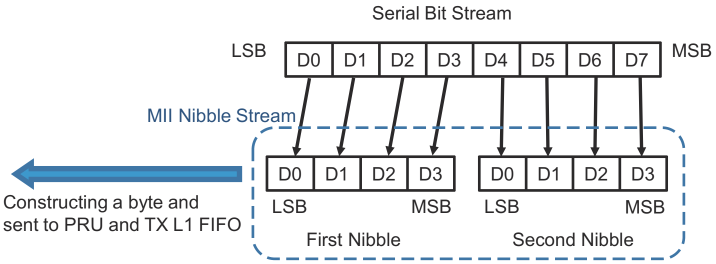

Figure 6-79. Data Nibble Structure

6.4.11.2.2.2 PRU R30 and R31

The PRU registers R30 and R31 are used to receive, transmit, and control the data for the PRU. As shown in Figure 6-80, the R31 is used to access data in the RX L1 FIFO, the R30 is used to transmit data from the PRU, and the R31 output is used the control the flow of receive and transmit. For more details about these registers, see the following sections.

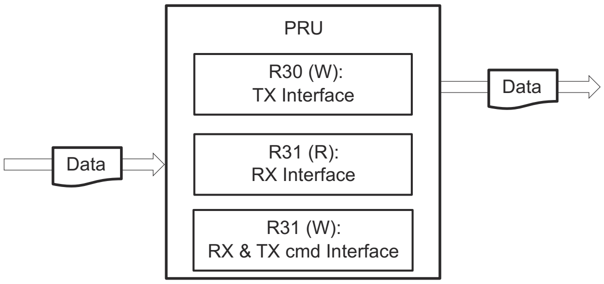

Figure 6-80. PRU R30, R31 Operations

6.4.11.2.2.3 RX and TX L1 FIFO Data Movement

To advance the next data byte seen by R31, the PRU must pop the data from the RX L1 FIFO. Likewise, the PRU can push the data from R30 to the TX L1 FIFO. These operations are illustrated in Figure 6-81.

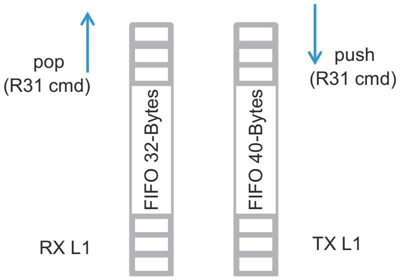

Figure 6-81. Reading and Writing FIFO Data

6.4.11.2.2.4 Receive CRC Computation

For the incoming data, the MII_G_RT calculates CRC32 and then compares against the value provided in the incoming frame. If there is a mismatch, the MII_G_RT signals ERROR_CRC to the PRU. If a previous node or Ethernet device appended an error nibble, the CRC calculation of received packet will be wrong because the longer frame and the frame length will end at a 4-bit boundary instead of the usual 8-bit boundary. When RX_DV goes inactive on the 4-bit boundary, the interface will assert DATA_RDY and BYTE_RDY flag with the ERROR NIBBLE. The error event is also mapped into the PRU_ICSSG INTC.

6.4.11.2.2.5 Transmit CRC Computation

For the outgoing data, the MII_G_RT calculates the CRC32 value and inserts it into outgoing packets. The CRC value computed on each MII transmit path is also available in memory map registers that can be read by the PRU and used primarily for debug and diagnostic purposes. The CRC is inserted into the outgoing packet based on the commands received through the R31 register of the PRU. The CRC will be inserted into the TX L1 FIFO, and there must be enough room to store the CRC value in the FIFO or else the FIFO will overflow. As Table 6-127 shows, the CRC programming model supports three sequences that provide more flexibility. Note: “cmdR31” indicates write to the mentioned bits of the R31 command interface.

Table 6-128. TX CRC Programming Models

Option 1	Step 1: cmdR31 [TX_CRC_HIGH + TX_CRC_LOW + TX_EOF]
Option 2	**Note: Only valid when TX L2 is disabled.** Step 1: cmdR31 [TX_CRC_HIGH] Step 2: wait > 6 clocks (PRU cycles) Step 3: cmdR31 [TX_CRC_LOW + TX_EOF]
Option 3	**Note: Only valid when TX L2 is disabled.** Step 1: cmdR31 [TX_CRC_HIGH] Step 2: wait > 6 clocks (PRU cycles) Step 3: read TX_CRC0[31-0] TX_CRC0 and TX_CRC1[31-0] TX_CRC1 Step 4: modify CRC[15-0] Step 5: cmdR31 [TX_PUSH16 + TX_EOF + TX_ERROR_NIBBLE]

6.4.11.2.2.6 Transmit CRC Computation for fragmented frames

Fragmented frames have a special CRC32. Each fragment CRC32 is based on the previous fragements, so a running total. In addition TX_CRC_HIGH is inverted for all fragments expect the last fragment. The final fragement has a normal CRC which is based on the full frame.

6.4.11.2.3 RX MII Interface

The RX MII interface is composed of multiple components that perform various tasks - latch received data, start of frame detection, start frame delimiter detection, CRC calculation and error detection, enhanced link detection through RX error detection and interface to PRU register R31.

Table 6-128 includes more details about the internal signals and output of these components

6.4.11.2.3.1 RX MII Receive Data Latch

The receive data from the MII interface is stored in the receive data FIFO which is 32 bytes. The PRU can access this data through the register R31. Depending on the configuration settings, the data can be latched on reception of one or two bytes. In each scheme, the configured number of nibbles is assembled before being copied into the PRU registers. Figure 6-82 shows the inputs and outputs of the data latch logic block.

The receiver logic in MII_RT can be programmed through the MII_RT MII_RT_RXCFG0 and MII_RT MII_RT_RXCFG1 registers to remove or retain the preamble + SFD from incoming frames.

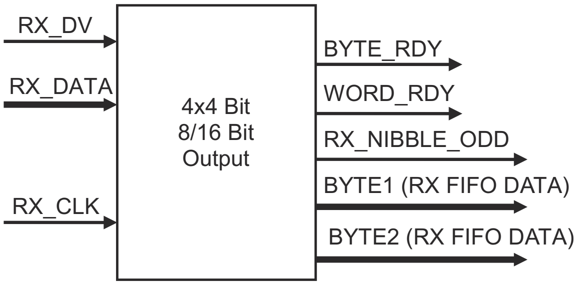

Figure 6-82. RX Data Latch

6.4.11.2.3.2 RX MII Start of Frame Detection

The start of frame detection logic tracks the frame boundaries and signals the beginning of a frame to other components of the PRU_ICSSG. This logic detects two events:

- Start of Frame (SOF) event that occurs when Receive Data Valid MII signal is sampled high.
- Start of Frame Delimiter (SFD) event is seen on MII Receive Data bus.

These event triggers can be used to add timestamp to the frames. The notification for these events is available through R31 as well as through INTC which is integrated in the PRU_ICSSG. Figure 6-83 shows the inputs and outputs of the start of frame detection logic block.

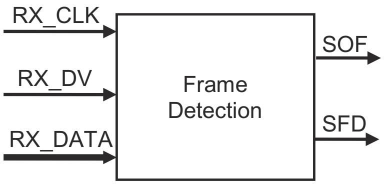

Figure 6-83. RX MII Start of Frame Detection

6.4.11.2.3.3 CRC Error Detection

For each incoming frame, the CRC is calculated by the MII_G_RT and compared against the CRC included in the frame. When the two values do not match, a CRC error is flagged. The ERROR_CRC indication is available in the register interface (PRU R31 Receive Interface) as well as in the FIFO interface (RX L2 Status Interface). It is also provided to the INTC which is integrated in the PRU_ICSSG. Figure 6-84 shows the inputs and outputs of CRC error detection logic block.

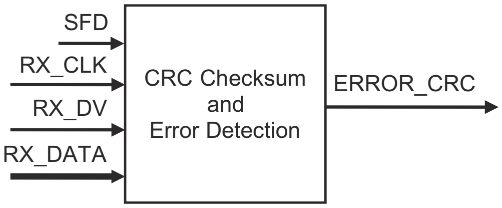

Figure 6-84. CRC Error Detection

6.4.11.2.3.4 RX Error Detection and Action

The RX error detection logic tracks the receive error signaled by the physical layer and informs the PRU_ICSSG INTC whenever an error is detected. Figure 6-85 shows the inputs and outputs of the RX error detection logic block. Note the following dependencies:

- RX_ERR signal is only sampled when RX_DV is asserted.
- All nibbles are discarded post RX_ERR event, including the nibble which had RX_ERR asserted. This state will remain until EOF occurs.

- Due to this fact, RX L1 FIFO and RX L2 FIFO will never receive any data with RX_ERR or post RX_ERR during that frame.

Note

RX error detection logic is supported only for MII mode and this feature is not supported for RGMII and SGMII modes of operation.

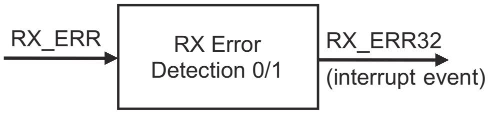

Figure 6-85. RX Error Detection

Note

Note for SGMII and RGMII modes, RX_ERR is sampled after SFD and during the payload if one occurs then it can be detected by R31 and/or INTC same as MII. The MII RX_ERR counter counts for every MII nibble.

This submodule also keeps track of a running count of receive error events within a 10 µs error detection window, as shown in Figure 6-86. The INTC is notified when 32 or more events have occurred in a 10 µs error detection window. The error detection window is not a sliding window but a non-overlapping window with no specific initialization time with respect to incoming traffic. The timer starts its 10 µs counts immediately after de-assertion of reset to the MII_G_RT module.

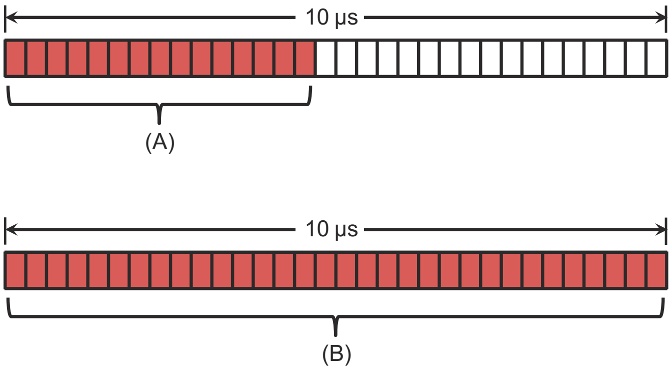

Note

There are fewer than 32 consecutive error events in the 10 µs window. The detection module will not forward to the interrupt controller (INTC).

Note

There are more or equal to 32 error events in the 10 µs window. The detection module will notify the interrupt controller (INTC).

Figure 6-86. Error Detection Window with Running Counter

6.4.11.2.3.5 RX Data Path Options to PRU

There are two data path options for delivering received data to the PRU, described further in the subsequent sections:

1. RX MII port → RX L1 FIFO → PRU (one word in flight)

2. RX MII port → RX L1 FIFO → RX L2 buffer → PRU (multi-word in flight)

Once the PRU has received RX data, the PRU can both manipulate received data or send data to the TX MII Interface.

6.4.11.2.3.6 RX MII Port → RX L1 FIFO → PRU

The RX L1 FIFO to PRU interface is depicted in Figure 6-87. In this mode, the data received from the MII interface is fed into the 32-byte RX L1 FIFO. The first data byte into the FIFO is automatically available in R31 of the PRU. Therefore, the PRU firmware can directly operate on this data without having to read it in a separate instruction. This allows the PRU to access receive data with low latency.

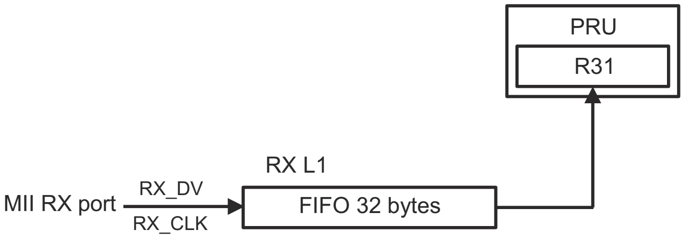

Figure 6-87. RX L1 to PRU Interface

When the new data is received, the PRU is provided with up to two bytes at a time in the R31 register, as shown in Figure 6-88. Once the PRU processes the incoming data, it instructs the MII_G_RT by writing to the R31 command interface bits to pop one or two bytes of data from the 32-byte RX FIFO. The pop operation causes current contents of R31 to be refreshed with new data from the incoming packet. Each time the data is popped, the status bits change to indicate so. If the pop is completed and there is no new data, the status bits immediately change to indicate no new data.

Note: The current R31 content, including data, will be lost after issuing the pop operation. If this information needs to be accessed later, the PRU should store the existing R31 content before popping new data.

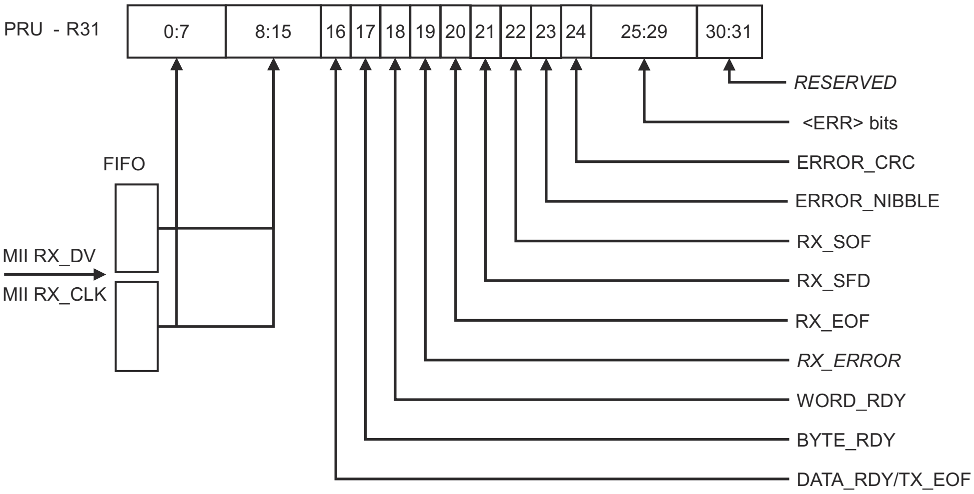

Figure 6-88. MII RX Data to PRU R31 (R) and RX FIFO

Table 6-128 describes the receive interface data and status contents provided by the R31 register. These contents are available when R31 is read. To configure this register, the PRU GPI mode should be set for MII_G_RT mode in the CFG register space. Note the following:

1. If the data from receive path is not read in time, it could cause an overflow event because the data is still continuously provided to the 32-byte receive FIFO. Due to the receive FIFO overflow, the data gets automatically discarded to avoid lack of space in the FIFO. At the same time, an interrupt is raised to the INTC through a system event (PRU<n>_RX_OVERFLOW). To detect an overflow condition, the PRU should

poll for this system event condition and a RX RESET command through the R31 command interface is required to clear out from this condition. Note that the received Ethernet frame is corrupted and should not be used for further processing as bytes have been dropped due to the overflow condition. A FIFO reset is recommended.

2. The receive data in the R31 register is available following synchronization to the PRU clock domain. So, there is a finite delay (120 ns) when data is available from MII interface and it is accessible to the PRU.
3. The receive FIFO also has the capability to be reset through software. When reset, all contents of receive FIFO are purged and it may result in the current frame not being received as expected. When a frame is being received and the PRU resets the RX FIFO, the remaining frame is not placed into the RX FIFO. However, any new frame arriving on the receive MII port will be stored in the FIFO.

Table 6-129. PRU R31: Receive Interface Data and Status (Read Mode)

Bits	Field Name	Description
31-30	RESERVED	In case of register interface, these bits are provided to PRU by other modules in PRU_ICSSG. From the MII_G_RT module point of view, these bits are always zero.
29	RX_MIN_FRM_CNT_ERR	RX_MIN_FRM_CNT_ERR is set to 1 when the count of total bytes of incoming frame is less than the value defined by RX_MIN_FRM_CNT. RX_MIN_FRM_CNT_ERR is cleared by RX_ERROR_CLR. Cleared by RX_ERROR_CLR or RX_L2_DONE. Note, during backpressure the status will not get updated by a new paket in L1 FIFO. The flag is valid for the current paket in L2 FIFO.
28	RX_MAX_FRM_CNT_ERR	RX_MAX_FRM_CNT_ERR is set to 1 when the count of total bytes of incoming frame is more than the value defined by RX_MAX_FRM_CNT_ERR. RX_MAX_FRM_CNT_ERR is cleared by RX_ERROR_CLR. Cleared by RX_ERROR_CLR or RX_L2_DONE. Note, during backpressure the status will not get updated by a new paket in L1 FIFO. The flag is valid for the current paket in L2 FIFO.
27	RX_EOF_ERROR	RX_EOF_ERROR is set to 1 when an RX_EOF event or RX_ERROR event occurs. RX_EOF_ERROR is cleared by RX_ EOF_CLR and/or RX_ ERROR_CLR.
26	RX_MAX_PRE_CNT_ERR	RX_MAX_PRE_CNT_ERR is set to 1 when the number of nibbles equaling 0x5 before SFD event (0xD5) is more than the value defined by PRUSS_MII_RT_RX_PCNT0/1 [RX_MAX_PCNT]. RX_MAX_PRE_CNT_ERR is cleared by RX_ERROR_CLR.
25	RX_ERR	RX_ERR is set to 1 when pr1_mii0/1_rxer is asserted while pr1_mii0/1_rxdv bit is set. RX_ERR is cleared by RX_ERROR_CLR.
24	ERROR_CRC	ERROR_CRC indicates that the frame has a CRC mismatch. This bit is valid when the RX_EOF bit is set. It should be noted that ERROR_CRC bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO. ERROR_CRC is cleared by RX_ERROR_CLR. Cleared by RX_ERROR_CLR or RX_L2_DONE. Note, during backpressure the status will not get updated by a new paket in L1 FIFO. The flag is valid for the current paket in L2 FIFO.
23	ERROR_NIBBLE	ERROR_NIBBLE indicates that the frame ended in odd nibble. It should be considered valid only when the RX_EOF bit and pr1_mii0/1_rxdv are set. Nibble counter is enabled post SFD event. It should be noted that ERROR_NIBBLE bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO. ERROR_NIBBLE is cleared by RX_ERROR_CLR.
22	RX_SOF	RX_SOF transitions from low to high when the frame data starts to arrive and pr1_mii0/1_rxdv is asserted. Note: There will be a small sync delay of 0ns – 5ns. The recommended time to clear this bit via RX_SOF_CLR is at the end of frame (EOF). It should be noted that RX_SOF bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO.
21	RX_SFD	RX_SFD transitions from low to high when the SFD sequence (0xD5) post RX_SOF is observed on the receive MII data. The recommended time to clear this bit via RX_SFD_CLR is at the end of frame (EOF). It should be noted that RX_SFD bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO.
20	RX_EOF	RX_EOF indicates that the frame has ended and pr1_mii0/1_rxdv is de-asserted. It also validates the CRC match bit. Note: There will be a small sync delay of 0ns – 5ns. It should be noted that RX_EOF bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO. Note: Also if RX_L2_EOF_SCLR_DIS is set, then this flag will remain asserted when RX_L2 is enabled until RX_EOF_CLR. Cleared by RX_ERROR_CLR or RX_L2_DONE. Note, during backpressure the status will not get updated by a new paket in L1 FIFO. The flag is valid for the current paket in L2 FIFO.

Table 6-129. PRU R31: Receive Interface Data and Status (Read Mode) (continued)

Bits	Field Name	Description
19	RX_ERROR	RX_ERROR indicates one or more of the following errors occurred: • RX_MAX/MIN_FRM_CNT_ERR • RX_MAX/MIN_PRE_CNT_ERR • RX_ERR RX_ERROR is cleared by RX_ERROR_CLR.
18	WORD_RDY	WORD_RDY indicates that all four nibbles in R31 have valid data. There is a 2 clock cycle latency from the command RX_POP16 to WORD_RDY update. Therefore, firmware needs to insure it does not read WORD_RDY until 2 clock cycles after RX_POP16.
17	BYTE_RDY	BYTE_RDY indicates that the lower two nibbles in R31 have valid data. There is a 2 clock cycle latency from the command RX_POP8 to BYTE_RDY update. Therefore, PRU firmware needs to insure it does not read BYTE_RDY until 2 clock cycles after RX_POP8.
16	DATA_RDY/ TX_EOF	When RX_DATA_RDY_MODE_DIS = 0: DATA_RDY indicates there is valid data in R31 ready to be read. This bit goes to zero when the PRU does a POP8/16 and there is no new data left in the receive MII port. This bit is high if there is more receive data for PRU to read. There is a 2 clock cycle latency from the command RX_POP16/8 to WORD_RDY/BYTE_RDY update. Therefore, PRU firmware needs to insure it does not read BYTE_RDY/ WORD_RDY until 2 clock cycles after RX_POP16/8. When RX_DATA_RDY_MODE_DIS = 1: TX_EOF indicates an TX EOF event (i.e. a 1 --> 0 transition on TX_EN) has occurred. This bit will clear when TX_RESET is set or when new data is first loaded. PRU firmware can wait until TX_EOF = 1, then start a new TX Frame by immediately loading new data.
15-8	BYTE1	Data Byte 1. This data is available such that it is safe to read by the PRU when the DATA_RDY/BYTE_RDY/WORD_RDY bits are asserted.
7-0	BYTE0	Data Byte 0. This data is available such that it is safe to read by the PRU when the DATA_RDY/BYTE_RDY/WORD_RDY bits are asserted.

6.4.11.2.3.7 RX MII Port → RX L1 FIFO → RX L2 Buffer → PRU

The RX L2 is an optional high performance buffer between the RX L1 FIFO and the PRU. Figure 6-89 illustrates the receive data path using RX L2 buffer. This data path is characterized by multi-word in flight transactions.

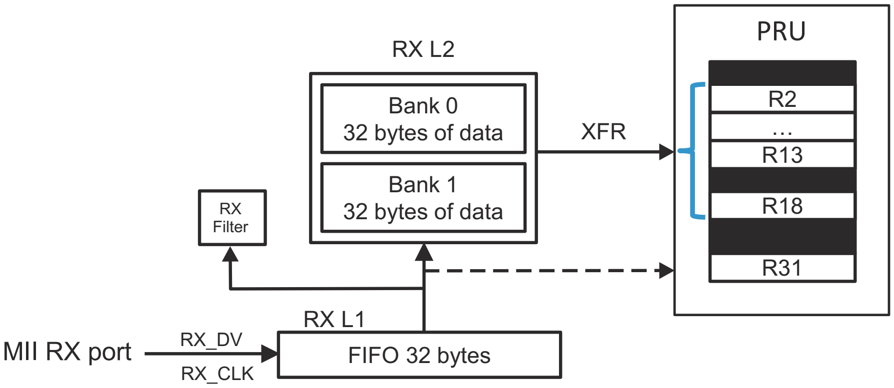

Figure 6-89. RX L2 to PRU Interface

The 64-byte RX L2 buffer is divided into two 32 byte banks, or ping/pong buffers. When the RX L2 is enabled, the incoming data from the MII RX port will transmit first to the 32 byte RX L1 FIFO. RX L1 pushes data into RX L2, starting when the first byte is ready until the final EOF marker. The RX L2 buffer will apply backpressure to the RX L1 FIFO after RX_L2_EOF event occur and until RX_L2_DONE event. Therefore, it is the PRU firmware's responsibility to fetch the data in RX L2 before it is overwritten by the cyclic buffer. The RX L1 will remain near empty, with only one byte (nibble) stored.

Each RX L2 bank holds up to 32 bytes of data, and every four nibbles (or 16 bits) of data has a corresponding 8-bit status. The data and status information are stored in packed arrays. In each bank, R2 to R9 contains the data packed array and R10 to R13 contains the status packed array. Figure 6-90 shows the relationship of the data registers and status registers. The RX L2 status registers record status information about the received data, such as ERROR_CRC, RX_ERROR, STATUS_RDY, etc. The RX L2 status register details are described in Table 6-129. Note: RX_RESET clears all Data and Status elements and resets R18.

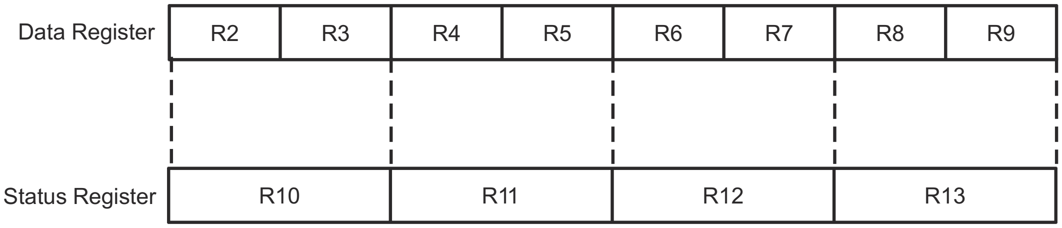

Figure 6-90. Data and Status Register Dependency

6.4.11.2.3.7.1 RX L2 Status in mode 0, none IET mode (when ICSS_G_CFG[2] RX_L2_G_EN= 0h)

Table 6-130. RX L2 Status in mode 0

Bit	Field Name	Description
7	ERROR_CRC	ERROR_CRC indicates that the frame has a CRC mismatch. This bit is valid when the RX_EOF bit is set. It should be noted that ERROR_CRC bit is ready in early status, which means it is calculated before data is available in RX L1 FIFO. ERROR_CRC will only be set for one entry, self clear on next entry.
6	ERROR_NIBBLE	ERROR_NIBBLE indicates that the frame ended in odd nibble. It should be considered valid only when the RX_EOF bit and pr1_mii0/1_rxdv are set. Nibble counter is enabled post SFD event. It should be noted that ERROR_NIBBLE bit is ready in early status, which means it is calculated before data is available in RX L1 FIFO. ERROR_NIBBLE will only be set for one entry, self clear on next entry.
5	RX_SOF	RX_SOF transitions from low to high when the frame data starts to arrive and pr1_mii0/1_rxdv is asserted. Note: There will be a small sync delay of 0ns – 5ns. It should be noted that RX_SOF bit is ready in early status, which means it is calculated before data is available in RX L1 FIFO. RX_SOF will only be set for one entry, self clear on next entry.
4	RX_SFD	RX_SFD transitions from low to high when the SFD sequence (0xD5) post RX_SOF is observed on the receive MII data. It should be noted that RX_SFD bit is ready in early status, which means it is calculated before data is available in RX + L1 FIFO. RX_SOF will only be set for one entry, self clear on next entry.
3	RX_EOF	RX_EOF indicates that the frame has ended and pr1_mii0/1_rxdv is de-asserted. It also validates the CRC match bit. Note: There will be a small sync delay of 0ns – 5ns. It should be noted that RX_EOF bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO. If RX_L2_EOF_SCLR_DIS = 1, then RX_EOF will remain set until RX_EOF_CLR event. Otherwise, RX_ERROR is self-clearing on next entry.
2	RX_ERROR	RX_ERROR indicates one or more of the following errors occurred: • RX_MAX/MIN_FRM_CNT_ERR • RX_MAX/MIN_PRE_CNT_ERR • RX_ERR RX_ERROR is cleared by RX_ERROR_CLR.

Table 6-130. RX L2 Status in mode 0 (continued)

Bit	Field Name	Description
1	STATUS_RDY	STATUS_RDY is set when RX_EOF or write pointer advanced by 2. This is a simple method for software to determine if RX_EOF event has occurred or new data is available. If RX_EOF is not set, all status bits are static.
0	RX_ERR	RX_ERR is set to 1 when pr1_mii0/1_rxer is asserted while pr1_mii0/1_rxdv bit is set. It will get set for first pr1_mii0/1_rxer event and self clear on SOF for the next FRAME.

6.4.11.2.3.7.2

Bank 0 and Bank 1 are used as ping/pong buffers. RX L2 supports the reading of a write pointer in R18 that allows software to determine which bank has active write transactions, as well as the specific write address within packed data arrays.

The PRU interacts with the RX L2 buffer using the high performance XFR read instructions and broadside interface. Table 6-130 shows the device XFR ID numbers for each bank.

Table 6-131. RX L2 XFR ID

Device ID	Function	Description
20	Selects RX L2 Bank0	R2:R9 Data packed array R10:R13 Status packed array mode 0
21	Selects RX L2 Bank1	R2:R9 Data packed array R10:R13 Status packed array mode 0
20/21	Byte pointer of current write	R18[5-0] Pointer indicating location of current write in data packed array. 0 = Bank0.R2.Byte0 (default and reset value) 1 = Bank0.R2.Byte1 2 = Bank0.R2.Byte2 3 = Bank0.R2.Byte3 4 = Bank0.R3.Byte0 … 63=Bank1.R9.Byte3

6.4.11.2.3.7.3 RX L2 Status for IET Type 1/Type 2 (when MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN = 1h)

Table 6-132. RX L2 XFR ID

Device ID	Function	Description
20	Selects RX L2 Bank0	R2:R9 Data packed array
21	Selects RX L2 Bank1	R2:R9 Data packed array
20/21	Meta Data	R10:R13 Meta Data

Table 6-132. RX L2 XFR ID (continued)

Device ID	Function	Description
20/21	Byte pointer of current write	R18[5-0] Pointer indicating location of current write in data packed array. 0 = Bank0.R2.Byte0 (default and reset value) 1 = Bank0.R2.Byte1 2 = Bank0.R2.Byte2 3 = Bank0.R2.Byte3 4 = Bank0.R3.Byte0 … 63=Bank1.R9.Byte3

Table 6-133. RX L2 IET mode Type 1/Type 2 (when MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN = 1h)

Rn	Field Name	Description
R10.b0	SMD	It will place the first byte to this location on first match of D5h or MII_G_RT_PREEMPT_CFG[15-8] EXP_SMD (default value: D5h) or MII_G_RT_SMDT1S_CFG [7-0] SMDT1S_0 MII_G_RT_SMDT1S_CFG [15-8] SMDT1S_1 MII_G_RT_SMDT1S_CFG [23-16] SMDT1S_2 MII_G_RT_SMDT1S_CFG [31-24] SMDT1S_3 MII_G_RT_SMDT1C_CFG [7-0] SMDT1C_0 MII_G_RT_SMDT1C_CFG [15-8] SMDT1C_1 MII_G_RT_SMDT1C_CFG [23-16] SMDT1C_2 MII_G_RT_SMDT1C_CFG [31-24] SMDT1C_3 MII_G_RT_PREEMPT_CFG[23-16] SMD_V or MII_G_RT_PREEMPT_CFG[[31-24] SMD_R The above is valid after RX_SOF and after the data write pointer advance or on RX_BLK1 event is asserted. It will get cleared when RX_L2_DONE event occurs.
R10.b1	FRAG_CNT	Fragment Count Byte Encoded FRAG_CNT will get cleared when RX_L2_DONE event occurs Only valid when SMD = SMDT1-Cx
R10.b2	SMD_Cx Next	This will always be the corresponding SMD_Cx which matches the last active SMD_Sx SMD_C0 when SMD = SMD_S0 SMD_C1 when SMD = SMD_S1 SMD_C2 when SMD = SMD_S2 SMD_C3 when SMD = SMD_S3 Only valid when SMD_Sx_ PRESENT is asserted
R10.b3	FRAG_CNT Next	This will always be the next possible FRAG_CNT FRAG_CNT1 when FRAG_CNT = FRAG_CNT0 FRAG_CNT2 when FRAG_CNT = FRAG_CNT1 FRAG_CNT3 when FRAG_CNT = FRAG_CNT2 FRAG_CNT0 when FRAG_CNT = FRAG_CNT3 Only valid when SMD = SMDT1-Cx
R11.b0[0]	MCRC_PRESENT	It will get set when MCRC is matched. This is valid after RX_EOF. It will get cleared when RX_L2_DONE event occurs.

Table 6-133. RX L2 IET mode Type 1/Type 2 (when MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN = 1h) (continued)

Rn	Field Name	Description
R11.b0[1]	SMD_Sx_ PRESENT	It will set if SMD matches one of SMDT1S[3:0] patterns: MII_G_RT_SMDT1S_CFG [7-0] SMDT1S_0 MII_G_RT_SMDT1S_CFG [15-8] SMDT1S_1 MII_G_RT_SMDT1S_CFG [23-16] SMDT1S_2 MII_G_RT_SMDT1S_CFG [31-24] SMDT1S_3 It will get cleared when RX_L2_DONE event occurs.
R11.b0[2]	SMD_Cx_ PRESENT	It will set if SMD matches one of SMDT1C[3:0] patterns: MII_G_RT_SMDT1C_CFG [7-0] SMDT1C_0 MII_G_RT_SMDT1C_CFG [15-8] SMDT1C_1 MII_G_RT_SMDT1C_CFG [23-16] SMDT1C_2 MII_G_RT_SMDT1C_CFG [31-24] SMDT1C_3 It will get cleared when RX_L2_DONE event occurs.
R12.b0	0x55 Byte0	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R12.b1	0x55 Byte1	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R12.b2	0x55 Byte2	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R12.b3	0x55 Byte3	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R13.b0	0x55 Byte4	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R13.b1	0x55 Byte5	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R13.b2	0x55/ SMDTx-Cx Byte6	Should be 0x55/SMDTx-Cx, but not required It will get cleared when RX_L2_DONE event occurs.
R13.b3	SMD/FRAG_CNTx Byte7	Should be SMD/FRAG_CNTx, but not required It will get cleared when RX_L2_DONE event occurs.

6.4.11.2.3.7.4

XFR read transactions are passive and have no effect on any status or other states in RX L2. The firmware can also read R18 to determine which Bank has active write transactions and the location of the transaction. With this information, the firmware can read multiple times the stable preserved data. Note: When RX L1 data is written to RX L2, the next status byte gets cleared at the same time the current status byte gets updated. The rest of the status buffer is persistent. When software is accessing any register of the ping/ pong buffer, software needs to issue an XFER read transaction to fetch the latest/current state of the ping/pong buffer. The PRU registers will not reflect the current snapshot of L2 unless an XFER is issued by software.

6.4.11.2.3.7.5 Broadside Stitch FIFO

A simple 2 deep by 32 Byte Wide broadside FIFO is attached to ID = 08 to enable the firmware to efficiently pack fragments into aligned data words.

Table 6-134. RX L2 XFR ID

Device ID	Function	Description
08	64 Bytes XOUT 1 Byte to 32 Bytes, LSB justify XIN 32 Bytes. Note: FIFO has less than 32 Bytes, it will only return the valid data LSB justified	R2:R9 Data packed array
08	It will subtract 4 bytes from the current wr_ptr	R10[0] Control
08	It will reset the rd and wr ptrs	R10[1] Reset

6.4.11.2.3.7.6 MII_G_RT RX Classifier

The RX Classifier block generates set of 16 class signals one set for each PRUn/RTU_PRUn core. It is composed of 3 subblocks:

1. RX L2 Filter block
2. RX Traffic Class Selector block
3. RX Rate Counter block

The software must configure MII_G_RT_RX_CLASS_CFG1_PRU0/1 to define the logic for the final class term. Each class is a function of filter flags which can get ORed or ANDed along with optional inversion. Each class has a set of registers (MII_G_RT_RX_CLASSm_AND_EN_PRUn, where m = 0 to 15 and n = 0 or 1) which determines if class is based on ORed or ANDed logic along with which of the 32 filters are part of the equation.

The final gate determine which of the terms will get factored to produce rx_class[15:0]. Each of the rx_class[15:0] can have different terms. It is fully programmable. Note: This logic will track fragemented frames based on the first segment of that frame. Only filters which will become valid on the intial fragement can get used for Traffic Class Selector, shown on Figure 6-91

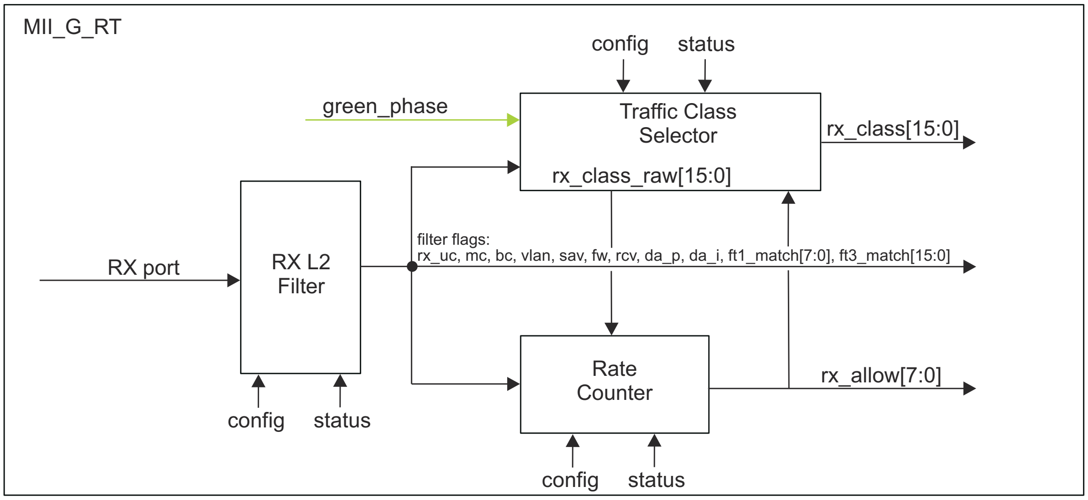

Figure 6-91. MII_G_RT RX Classifier

6.4.11.2.3.7.6.1 RX Rate Counter Block

The RX Rate Counter contains 8 independent rate monitors which determines if the rate of traffic of a given class exceedes the threshold set by MII_G_RT_RX_RATE_CFGm_PRUn[31-0] RX_RATE_CIR_IDLEm registers (where m = 0 to 7 and n = 0 or 1).

Each rate monitor has implemented PIR (Peak Information Rate) counter. The PIR counter in each monitor is a 37-bit internal counter where the monitor MII_G_RT_RX_RATE_CFGm_PRUn[31-0] RX_RATE_CIR_IDLEm is added on every clock and the frame size bytes less than 18 is subtracted at End Of Frame (EOF). If the count is negative at lookup time, the packet will be marked RED, else it can be GREEN.

6.4.11.2.3.7.6.2 RX Rate Hit Mapping

Each of the 8 RX Rate monitors can monitor 1 of the 0..48 possible data traffic types.

Table 6-134 defines the RX Rate Hit Mapping.

Table 6-135. RX Rate Hit Mapping

Bit Configuration	rx_rate_hit (n= 0 to 7)	Source
0	rx_rate_hit<n>	ft1_match0
1	rx_rate_hit<n>	ft1_match1
2	rx_rate_hit<n>	ft1_match2

Table 6-135. RX Rate Hit Mapping (continued)

Bit Configuration	rx_rate_hit (n= 0 to 7)	Source
3	rx_rate_hit<n>	ft1_match3
4	rx_rate_hit<n>	ft1_match4
5	rx_rate_hit<n>	ft1_match5
6	rx_rate_hit<n>	ft1_match6
7	rx_rate_hit<n>	ft1_match7
8	rx_rate_hit<n>	ft3_match0
9	rx_rate_hit<n>	ft3_match1
10	rx_rate_hit<n>	ft3_match2
11	rx_rate_hit<n>	ft3_match3
12	rx_rate_hit<n>	ft3_match4
13	rx_rate_hit<n>	ft3_match5
14	rx_rate_hit<n>	ft3_match6
15	rx_rate_hit<n>	ft3_match7
16	rx_rate_hit<n>	ft3_match8
17	rx_rate_hit<n>	ft3_match9
18	rx_rate_hit<n>	ft3_match10
19	rx_rate_hit<n>	ft3_match11
20	rx_rate_hit<n>	ft3_match12
21	rx_rate_hit<n>	ft3_match13
22	rx_rate_hit<n>	ft3_match14
23	rx_rate_hit<n>	ft3_match15
24	rx_rate_hit<n>	ft_rx_uc
25	rx_rate_hit<n>	ft_rx_mc
26	rx_rate_hit<n>	ft_rx_bc
27	rx_rate_hit<n>	ft_rx_sav
28	rx_rate_hit<n>	ft_rx_fw
29	rx_rate_hit<n>	ft_rx_rcv
30	rx_rate_hit<n>	ft_rx_vlan
31	rx_rate_hit<n>	ft_rx_da_p
32	rx_rate_hit<n>	ft_rx_da_i
33	rx_rate_hit<n>	rx_class_raw0
34	rx_rate_hit<n>	rx_class_raw1
35	rx_rate_hit<n>	rx_class_raw2
36	rx_rate_hit<n>	rx_class_raw3
37	rx_rate_hit<n>	rx_class_raw4
38	rx_rate_hit<n>	rx_class_raw5
39	rx_rate_hit<n>	rx_class_raw6
40	rx_rate_hit<n>	rx_class_raw7
41	rx_rate_hit<n>	rx_class_raw8
42	rx_rate_hit<n>	rx_class_raw9
43	rx_rate_hit<n>	rx_class_raw10
44	rx_rate_hit<n>	rx_class_raw11
45	rx_rate_hit<n>	rx_class_raw12
46	rx_rate_hit<n>	rx_class_raw13
47	rx_rate_hit<n>	rx_class_raw14

Table 6-135. RX Rate Hit Mapping (continued)

Bit Configuration	rx_rate_hit (n= 0 to 7)	Source
48	rx_rate_hit<n>	rx_class_raw15

To select which traffic type to be monitored register MII_G_RT_RX_STAT_CLASSm_HIT_PRUn[31-0] RX_STAT_CLASSm_PRUn (where m = 0 to 15 and n = 0 or 1) has to configured. If this class is a hit and at the EOF then the counter will get subtracted based on the packet size.

6.4.11.2.3.7.6.3 Traffic Class Selector Block

This logic block does simple logic reduction which operates on:

1. The green phase signal
2. All of the filter outputs along with basic filter flags
3. The outputs from the Rate Counter

The Traffic Class Selector module produces 2 sets of outputs:

- rx_class[15:0] - goes to broadside for observation
- rx_class_raw[15:0] - goes to the Rate Counter

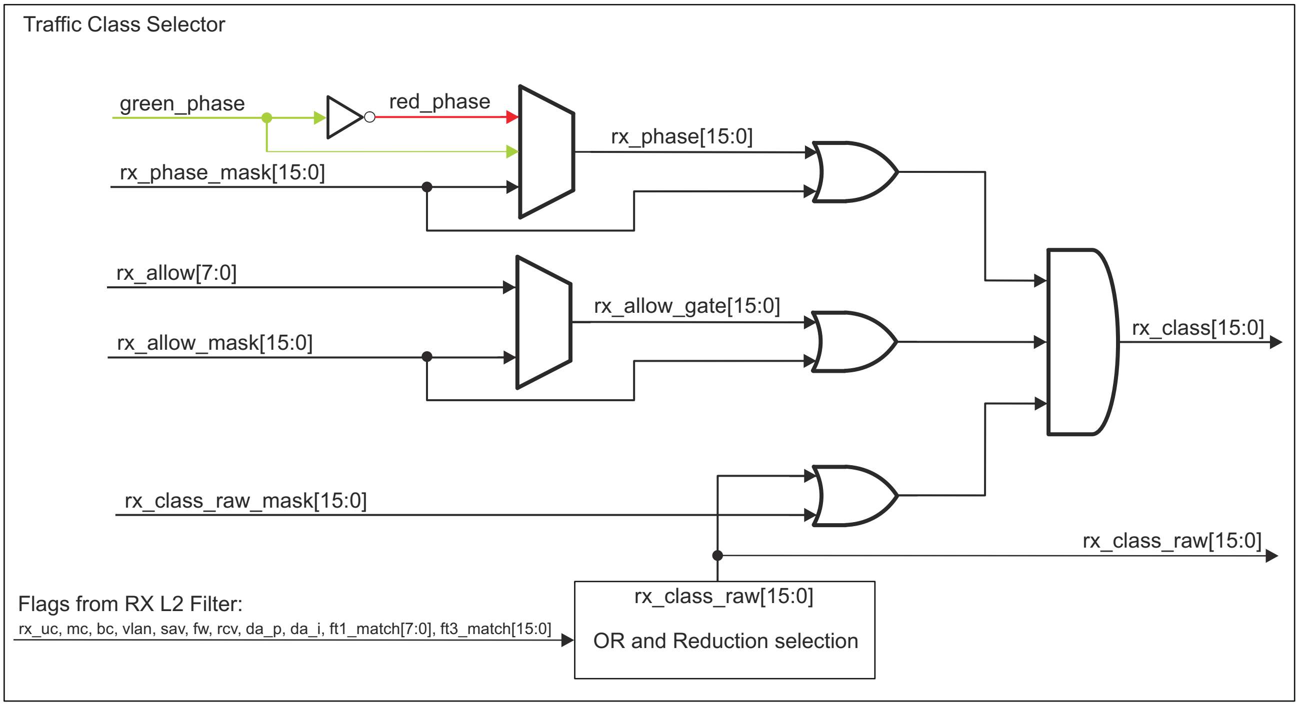

Figure 6-92. Traffic Class Selector

The logic reduction is controlled by a set of registers which controls the type of reduction and the selection of the inputs.

Table 6-135 defines the mapping and the reduction options.

Table 6-136. Traffic Class Data Mapping

rx_class_data	Source
rx_class_data[31]	ft_rx_sav
rx_class_data[30]	ft_rx_mc
rx_class_data[29]	ft_rx_bc
rx_class_data[28]	ft_rx_fw
rx_class_data[27]	ft_rx_rcv

Table 6-136. Traffic Class Data Mapping (continued)

rx_class_data	Source
rx_class_data[26]	ft_rx_vlan
rx_class_data[25]	ft_rx_da_p
rx_class_data[24]	ft_rx_da_i
rx_class_data[23:16]	ft1_match[7:0]
rx_class_data[15:8]	ft3_match[15:8]
rx_class_data[7:0]	ft3_match[7:0]

In order to select the source mapping, i.e. wich filter flag hit the rate logic, 1 of 8 RATE sources has to be configured through the following registers: MII_G_RT_RX_RATE_SRC_SEL0_PRU0 or MII_G_RT_RX_RATE_SRC_SEL1_PRU0 (for PRU0 core) and MII_G_RT_RX_RATE_SRC_SEL0_PRU1 or MII_G_RT_RX_RATE_SRC_SEL1_PRU1 (for PRU1 core). Note that only 1 of RX Rate classes can be asserted per frame.

6.4.11.2.3.7.6.4 PRU_ICSSG RX L2 Filter Block

There are 8 MAC filter instances implemented in the PRU_ICSSG system. Each of the MAC filters (RX L2 Filter - Type 1) has the following specific features, as is shown in Figure 6-93:

- 8 unique set of DA (Destination Address), 6 Bytes used to compare to DA, 6 Bytes mask, optional compare mode (equal, greater than, less than). These 6 Bytes reside in MAC_PRU0_0 and MAC_PRU0_1 registers (for PRU0 core) and in MAC_PRU1_0 and MAC_PRU1_1 registers (for PRU1 core).
- 1 common MAC_PORT0/1, 6 Bytes used to compare to SA (Source Address)
- 1 common MAC Host Interface, 6 Bytes used to compare to SA (Source Address). These 6 Bytes reside in MII_G_RT_MAC_INTERFACE_0[31-0] MAC_INF_0 and MII_G_RT_MAC_INTERFACE_1[15-0] MAC_INF_1 registers.
- Optional RX filter restart

16 Content filter instances (RX L2 Filter - Type 3). Each of the Content filters has the following specific features, as is shown also in Figure 6-94:

- 4 Byte Tag + 8 Byte content compare, 4+8 Byte mask, length, compare range
- Auto VLAN tag detection/shift
- IPV6 filter needs 2 content filters, each of a unquie start

8 x ingress rate limiters.

- Global status 2 rate limiter map, 256 bps steps, up to 16 bit window.
- Maximum Packet size is 10,000 bytes. It is software responsibility to insure that the packet size does not go beyond.

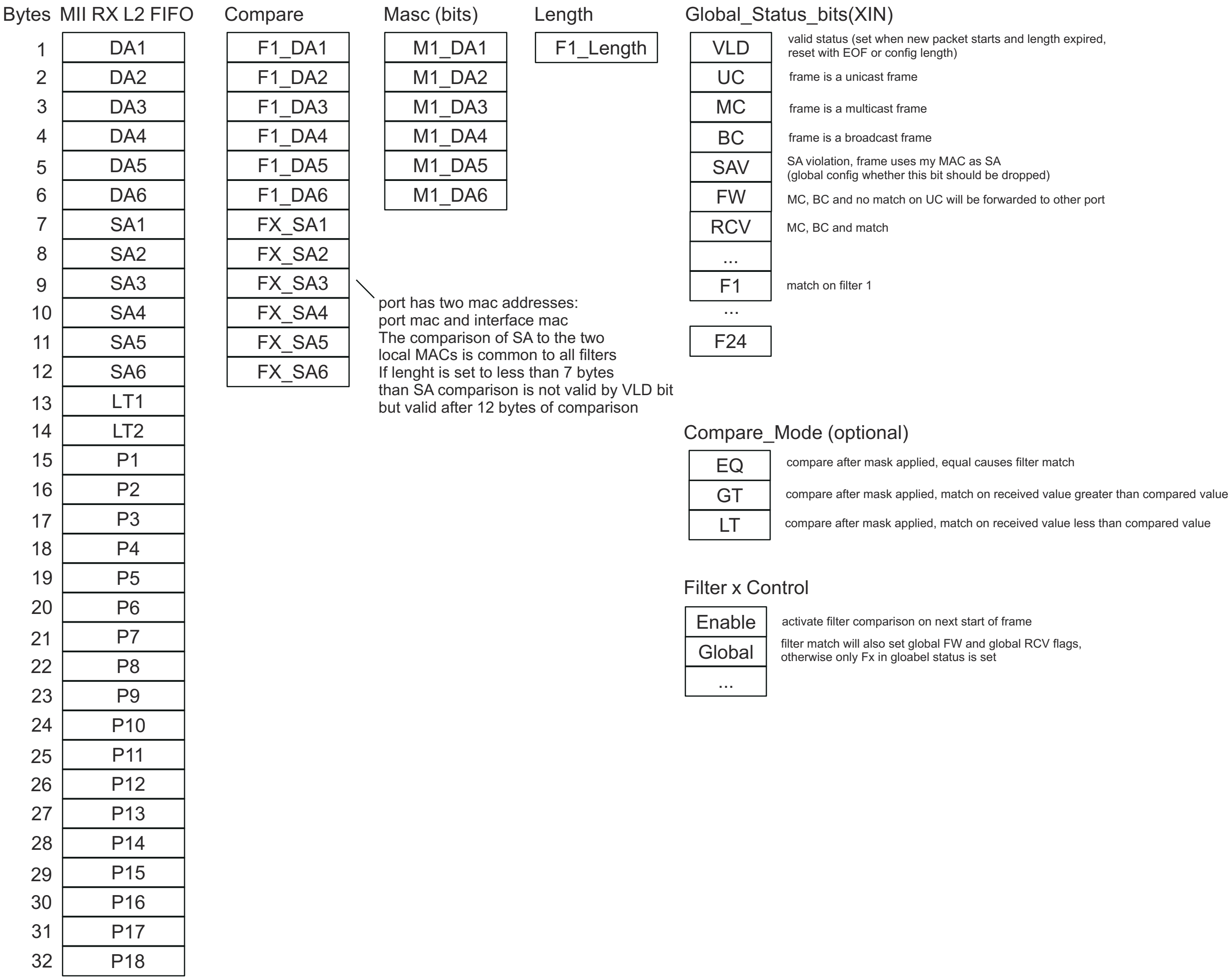

port has two mac addresses:
port mac and interface mac
The comparison of SA to the two
local MACs is common to all filters
If lenght is set to less than 7 bytes
than SA comparison is not valid by VLD bit
but valid after 12 bytes of comparison

Figure 6-93. PRU_ICSSG RX L2 Filter -Type 1 (MAC Filter)

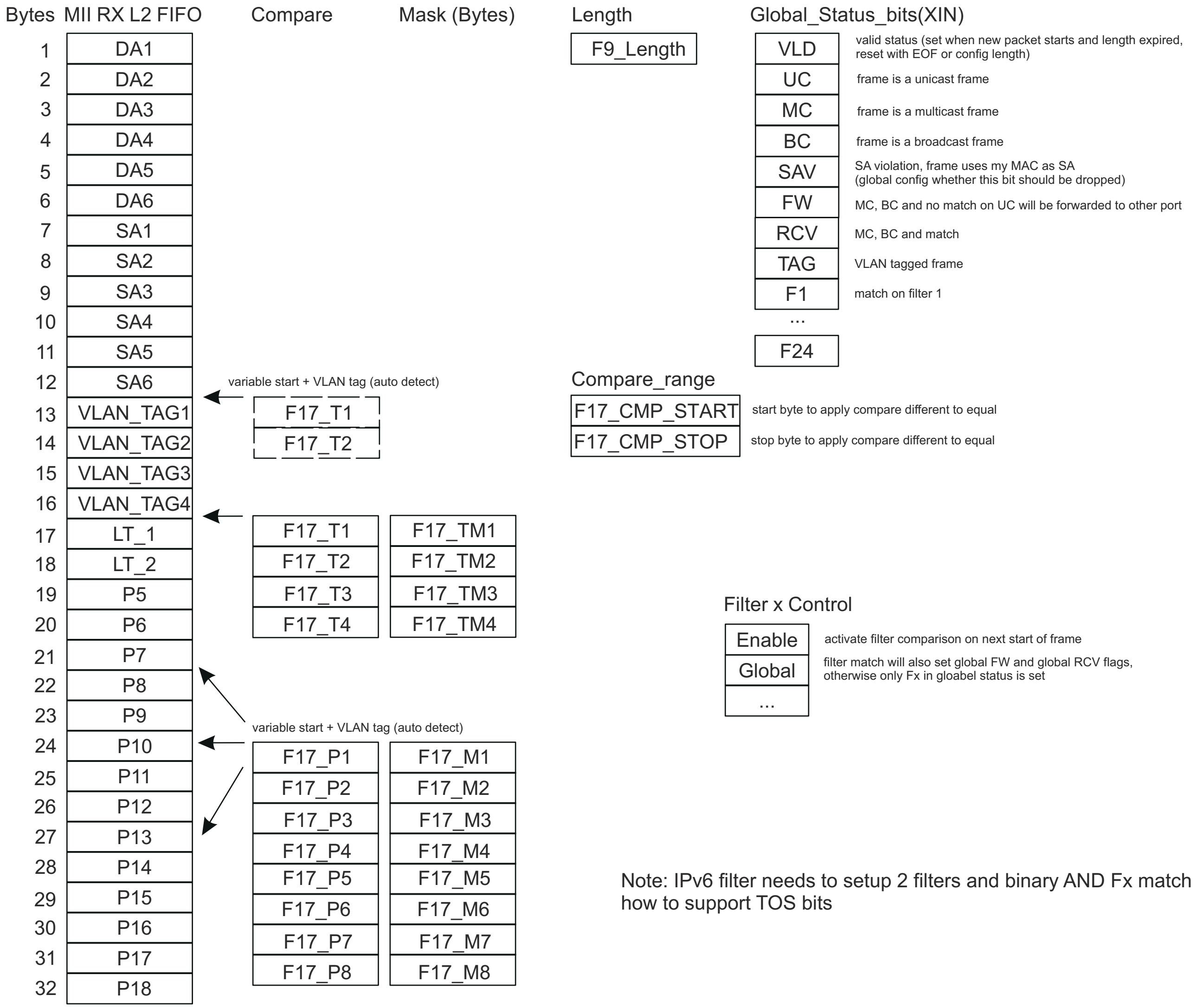

Figure 6-94. PRU_ICSSG RX L2 Filter - Type 3 (Content Filter)

6.4.11.2.3.7.6.4.1 PRU_ICSSG RX L2 Filter Operation

The RX L2 filter operates on the data packet when the data packet is pushed into RX L2 FIFO. The RX L2 FIFO will need to be enabled. The filters will work with ether enable or disable of the RX L2 features through MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN bit.

Note

Note that MII mode can operate with or without MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN bit to be enabled. For RGMII and SGMII modes must have MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN bit enabled.

The status of the flags is available in Broadside Map of RTU_PRU and PRU along with the poke mode if enabled. The flags are cleared on RX_L2_DONE event or a software update of MII_G_RT_FT3_m_START_PRUn[14-0] FT3_START bitfield (where m = 0 to 15 and n = 0 or 1). Note that these filters have no state information/context for pre-empted frames or fragements. All data packets are handled the same way, Byte 1 is Byte 1.

Table 6-136 defines the mapping between PRU or RTU_PRUn internal core registers and RX filter status flags

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Note

Note that both PRU and RTU_PRU cores get the same mapping.

The data is always stored in the RX L2 FIFO before the flag is set, i.e. the flag can be delayed.

Table 6-137. MII_G_RT RX Classifier Broadside Mapping

BS ID	BS R	Bit	Name	Type	Reset	Description
22	R10	14-0	FT_RX_PTR	R	0h	This shows the current byte that the filters are working on. The value remains persistent until a new packet starts. For example 0,1,2,3,….63,63,63,63,63,0,1,2,3…78
22	R11	8	FT_RX_UC	R	0h	Unicast frame defined by DA1[0]. Set on DA[0] = 0h. Clear on RX_L2_DONE event.
22	R11	9	FT_RX_MC	R	0h	Multicast frame defined by DA1[0]. Set on DA[0] = 1h. Clear on RX_L2_DONE event.
22	R11	10	FT_RX_BC	R	0h	Broadcast frame defined by DA6:DA1. Set on DA = FFFF_FFFF_FFFFh. Clear on RX_L2_DONE event.
22	R11	11	FT_RX_SAV	R	0h	Source Address Violation defined by SA and MAC. Set on when SA = MAC_I or MAC_PRU0 or MAC_PRU1. Clear on RX_L2_DONE event.
22	R11	12	FT_RX_FW	R	0h	Forward frame. Set on MC or BC or DA_I Clear on RX_L2_DONE event.
22	R11	13	FT_RX_RCV	R	0h	Receive frame. Set on MC or BC or DA_I Clear on RX_L2_DONE event.

Table 6-137. MII_G_RT RX Classifier Broadside Mapping (continued)

BS ID	BS R	Bit	Name	Type	Reset	Description
22	R11	14	FT_RX_VLAN	R	0h	VLAN frame. Set when Byte 14 and Byte 13 (16-bit field) == 0x8100 Clear on RX_L2_DONE event.
22	R11	15	FT_RX_DA_P	R	0h	Destination Address Match. Set on when DA = MAC_PRUn (where n is the index number of attached PRU core). Clear on RX_L2_DONE event.
22	R11	16	FT_RX_DA_I	R	0h	Destination Address Match. Set on when DA = MAC_I. Clear on RX_L2_DONE event.
22	R11	31	RX_L2_DONE	W	0h	RX L2 Done. Write 1h self-clearing. This will reset all flags and all RX L2 Filters. It can only get a set after the last byte gets posted to RX L2 or RX L2 EOF event. Once set, it will enable data from RX L1 FIFO to be filled into RX L2 FIFO. IF Packet less than 64B you also need to issue RX_RESET.
22	R12	0	FT1_VLD	R	0h	Valid Status of RX L2 Filter -Type 1 (MAC Filter). Set after MII_G_RT_FT1_START_LEN_PRU0/1[19-16] FT1_LEN (this bitfield defines the total numbers of Bytes, Filter 1 will check before Valid bit is set) with TBD additional latency. Clear on RX_L2_DONE event. Clear on MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START update.
22	R12	15-8	FT1_MATCH	R	0h	RX L2 Filter (Type 1) Match Vector Status. 0h: No Match 1h: Match Clear on RX_L2_DONE event. Clear on MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START update.
22	R13	7-0	FT3_VLD[7-0]	R	0h	Valid Status of RX L2 Filter-Type 3 (Content Filter). Clear on RX_L2_DONE event. Clear on MII_G_RT_FT3_m_START_PRU0/1[14-0] FT3_START update (where m = 0 to 15).
22	R13	15-8	FT3_MATCH[7-0]	R	0h	RX L2 Filter (Type 3) Match Vector Status. 0h: No Match 1h: Match Clear on RX_L2_DONE event. Clear on MII_G_RT_FT3_m_START_PRU0/1[14-0] FT3_START update (where m = 0 to 15).
22	R14	7-0	FT3_VLD[15-8]	R	0h	Valid Status of RX L2 Filter-Type 3 (Content Filter). Clear on RX_L2_DONE event. Clear on MII_G_RT_FT3_m_START_PRU0/1[14-0] FT3_START update (where m = 0 to 15).

Table 6-137. MII_G_RT RX Classifier Broadside Mapping (continued)

BS ID	BS R	Bit	Name	Type	Reset	Description
22	R14	15-8	FT3_MATCH[15-8]	R	0h	RX L2 Filter (Type 3) Match Vector Status. 0h: No Match 1h: Match Clear on RX_L2_DONE event. Clear on MII_G_RT_FT3_m_START_PRU0/1[14-0] FT3_START update (where m = 0 to 15).
22	R15	9-0	SA_HASH	R	0h	SA Hash Value. Hash of SA6:SA1
22	R15	16	SA_HASH_VLD	R	0h	SA Hash Valid. Set when SA Hash is completed.. Clear on RX_L2_DONE event.
22	R16	10-0	CONN_HASH	R	0h	Connection Hash Value. Hash CONN4:CONN1
22	R16	16	CONN_HASH_VLD	R	0h	Connection Hash Valid. Set when Connection Hash is completed. Note: controlled by MII_G_RT_CONN_HASH_PRU0/1[9-0] CONN_HASH_SEED Clear on RX_L2_DONE event.
22	R17	0	RX_RATE_STATUS0	R	0h	RX Rate Status0. 1h: Green 0h: Red
22	R17	1	RX_RATE_STATUS1	R	0h	RX Rate Status1. 1h: Green 0h: Red
22	R17	2	RX_RATE_STATUS2	R	0h	RX Rate Status2. 1h: Green 0h: Red
22	R17	3	RX_RATE_STATUS3	R	0h	RX Rate Status3. 1h: Green 0h: Red
22	R17	4	RX_RATE_STATUS4	R	0h	RX Rate Status4. 1h: Green 0h: Red
22	R17	5	RX_RATE_STATUS5	R	0h	RX Rate Status5. 1h: Green 0h: Red
22	R17	6	RX_RATE_STATUS6	R	0h	RX Rate Status6. 1h: Green 0h: Red

Table 6-137. MII_G_RT RX Classifier Broadside Mapping (continued)

BS ID	BS R	Bit	Name	Type	Reset	Description
22	R17	7	RX_RATE_STATUS7	R	0h	RX Rate Status7. 1h: Green 0h: Red
22	R17	31-16	RX_CLASS[15-0]	R	0h	RX Class Status.

6.4.11.2.3.7.6.4.2 PRU_ICSSG RX L2 Filter - Type 1 (MAC Filter) Operation

Rules:

- RX L2 Filter (Type 1) attributes can only get updated when the filter is not active
- All 8 × RX L2 Filters (Type 1) will always start at the same time (default is 1st Byte)

Operation:

- RX L2 Filter (Type 1) will have 8 compare functions active concurrently
- RX L2 Filter (Type 1) will start on Byte 1 of the RX Frame by default
- MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START bitfield (where n = 0 or 1) can be used by software to restart or delay the activation of the Type 1 filter.
- MII_G_RT_FT_RX_PTR_PRU0/1[31-0] FT_RX_PTR_PRUn bitfield (where n = 0 or 1) can be used by software to determine the current byte the filter is working on.

Example for initial setup of RX filter (Type 1):

- Write 1h to MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START bitfield
- Write 1h to MII_G_RT_FT_RX_PTR_PRU0/1[31-0] FT_RX_PTR_PRUn bitfield (where n = 0 or 1)
- After 22 Bytes, then MII_G_RT_FT_RX_PTR_PRU0/1[31-0] FT_RX_PTR_PRUn = 22 (where n = 0 or 1). The software can then set MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START = 36 (this action will clear all Type1 filter status bits)
- When MII_G_RT_FT_RX_PTR_PRU0/1[31-0] FT_RX_PTR_PRUn = 36 (where n = 0 or 1), the RX filter Type 1 will start again on Byte 36

6.4.11.2.3.7.6.4.3 PRU_ICSSG RX L2 Filter - Type 3 (Content Filter) Operation

Rules:

- RX L2 Filter (Type 3) attributes can only get updated when the filter is not active.
- RX L2 Filter (Type 3) must start on Byte 13 or later

Note: The MII_G_RT_FT3_0_START_PRUn[14-0] FT3_START bit field of “0” contains 1st Byte after preamble

Operation:

- RX L2 Filter (Type 3) will have 16 compare functions active concurrently
- This RX L2 Filter (Type 3) has no dependencies or interaction with RX L2 Filter Type1
- Each of the 16 RX L2 filters (Type 3) have unque start values. See registers MII_G_RT_FT3_0_START_PRU0/1 to MII_G_RT_FT3_15_START_PRU0/1.

RX L2 Filter (Type 3) can start operation on Byte 13 or Byte 17:

- The RX L2 Filter (Type 3) can start operation on Byte 13, if Byte 14 and Byte 13 (16-bit field) are different than value of 0x8100 (this is Tag Protocol Identifier (TPID) IEEE 802.1Q-tagged frame)
- The RX L2 Filter (Type 3) can start operation on Byte 17, if Byte 14 and Byte 13 (16-bit field) are equal to value of 0x8100 in order to identify the frame as IEEE 802.1Q-tagged frame (this is Tag Protocol Identifier (TPID) IEEE 802.1Q-tagged frame)

6.4.11.2.3.7.6.4.4 PRU_ICSSG RX L2 Filter - Type 3 (Content Filter) Auto Restart operation

The RX L2 Filter (type 3) have an optional auto offset adjust and continue the next comparision if not match has been found. It will continue to do this until the first hit is found. This mode is enabled when one or more bits is set in MII_G_RT_FT3_m_CFG_PRUn[31-16] FT3_m_TRIG_OR_EN (where m = 0 to 15 and n = 0 or 1). This function only works on RX L2 Filter (type 3) pattern compare function, which is 64-bit compare function.

Rules:

- Only EQ function is allowed and It uses the following configuration registers:
- MII_G_RT_FT3_m_CFG_PRUn[14-0] FT3_m_IJMP_OFFSET_PRUn (where m = 0 to 15 and n = 0 or 1) - relative byte offset jump used after first trigger hit
- MII_G_RT_FT3_m_CFG_PRUn[30-16] FT3_m_NJMP_OFFSET_PRUn (where m = 0 to 15 and n = 0 or 1) - relative byte offset jump used after the first auto compare function and beyond
- MII_G_RT_FT3_m_CFG_PRUn[31-16] FT3_m_TRIG_OR_EN (where m = 0 to 15 and n = 0 or 1) - Simple OR select to determine which FT3 match will cause the first intial jump and auto compare sequence to get enabled. Software can not enable same FT3 to cause its own trigger.
- MII_G_RT_FT3_m_LEN_PRUn[8-0] FT3_m_LEN_START_BIT_PRUn (where m = 0 to 15 and n = 0 or 1) - relative bit offset from the HIT byte location upto 512 bit offset
- MII_G_RT_FT3_m_LEN_PRUn[19-16] FT3_m_LEN_SIZE_BIT_PRUn (where m = 0 to 15 and n = 0 or 1) - used to determine where to end the exraction to determine the on the fly length byte offset

6.4.11.2.3.7.6.4.5 RX SA Hash

SA6:SA1 is hashed using the below polynomial providing a 10-bit value:

$x^{10} + x^7 + x^2 + 1$

This value can be read through MII_G_RT_SA_HASH_PRU0/1[9-0] SA_HASH_SEED registers.

By default the initial value of MII_G_RT_SA_HASH_PRU0/1[9-0] SA_HASH_SEED bitfield is set to 0h unless software updates it. Given a fixed set of addresses, changing the seed can drastically change the distribution of the result. Given random inputs, the distribution would be random as well.

6.4.11.2.3.7.6.4.6 RX Connection Hash

4 Bytes of the packet (P(n+3):Pn) are hashed using the below polynomial providing a 10-bit value.

$x^{10} + x^7 + x^2 + 1$

This 10-bit value can be read through MII_G_RT_CONN_HASH_PRU0/1[9-0] CONN_HASH_SEED registers.

By default the initial value of MII_G_RT_CONN_HASH_PRU0/1[9-0] CONN_HASH_SEED bitfield is set to 0h unless software updates it. Given a fixed set of addresses, changing the seed can drastically change the distribution of the result. Given random inputs, the distribution would be random as well.

6.4.11.2.4 PRU_ICSSG TX MII Interface

The PRU core directly drives the MII transmit interface via its R30 internal register. The contents of R30 register and RX Data from receive interface are taken and fed into a transmit FIFO (TX L2 FIFO - 64 Bytes).

Data to be transmitted is loaded into the TX L1 FIFO. The transmit FIFO (TX L1) stores up to 40 Bytes of transmit data. Note that this includes the preamble bytes. From the transmit FIFO (TX L1), the data is sent to the MII TX port of the PHY by the MII_RT transmit logic.

The transmit FIFO also has the capability to be reset through software (TX_RESET). When reset, all contents of transmit FIFO are purged and this may result in a frame not getting transmitted as expected, if the transmission is already ongoing. Any new data written in the transmit FIFO results in a new frame being composed and transmitted. An overflow event will require a TX_RESET to recover from this condition.

There are four dependencies that must be true for TX_EN to assert:

1. TX L1 FIFO not empty
2. Interpacket gap (IPG) timer expiration
3. RX_DV to TX_EN timer expiration
4. TX_EN compare timer expiration

The transmit interface also provides an underflow error signal in case there was no data loaded when TX_EN triggered. The transmit underflow signal is mapped to the INTC in PRU_ICSSG. The current FIFO fill level cannot be accessed by PRU firmware. The firmware can issue an R31 command via R31 bit 29 (TX_EOF) to indicate that the last byte has been written into the TX FIFO.

6.4.11.2.4.1 TX Data Path Options to TX L1 FIFO

There are two data path options for delivering data to the TX L1 FIFO and transmit port, described further in the subsequent sections:

1. PRU → TX L1 FIFO → TX MII port
2. RX L1 FIFO → TX L1 FIFO → TX MII port

6.4.11.2.4.1.1 PRU → TX L1 FIFO → TX MII Port

The PRU can be used to feed data into the TX L1 FIFO using the R30 and R31 registers, shown in Figure 6-95. The PRU has the option to write up two or four bytes of R30 and then pushes the data into the TX L1 FIFO by writing to the R31 command interface.

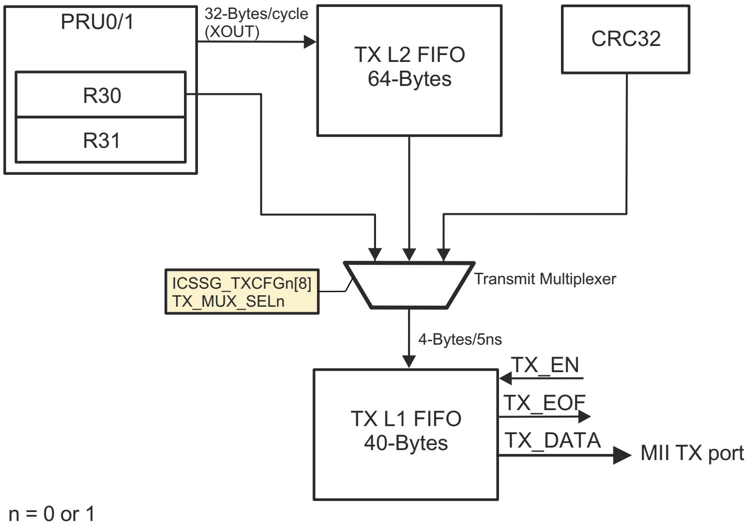

Figure 6-95. PRU to TX L1 FIFO Interface

6.4.11.2.4.1.1.1 TX L2 FIFO Features

- 64-Bytes deep TX L2 FIFO which feeds data into a 40-Bytes deep TX L1 FIFO
- Maximum of 64-Bytes Broad Side load, minimum of 1-Byte Broad Side load, R2.b0(start)
- **Note: MII_RT_TXCFG0/1[3] TX_BYTE_SWAPn bit (where n = 0 or 1) is not supported for TX L2 FIFO.**
- FIFO level status available through MII_RT_TX_FIFO_LEVEL0[7-0] TX_FIFO_LEVEL0 and MII_RT_TX_FIFO_LEVEL1[7-0] TX_FIFO_LEVEL1 registers
- 2 FIFO threshold events: 32-Bytes (available and empty) or 64-Bytes (available)
- Total bytes sent for a current/last frame is available for software
- New frame can start after TX L2 FIFO is empty, but before TX L1 FIFO is empty from an old frame
  - **Note: Only supported for RGMII and SGMII modes of operation**
  - New frame can start after 5 or more core clock cycles after it is drained, this is required to finish the CRC for the first frame

6.4.11.2.4.1.1.2

Table 6-138. TX L2 XFR Mapping

Device ID	Function	Description
40	Data	R17:R2 Data, XOUT Only 1-Byte to 64-Bytes in size LSB packed and no gaps, for example 64-Bytes push R17:R2 32-Bytes push R9:R2 16-Bytes push R5:R2 4-Bytes push R2 7-Bytes push R3(b2.b0):R2 1-Bytes push R2(b0) Can do back to back
40	Control	Control of TX L2 FIFO
40	Status	Status of TX L2 FIFO

Table 6-139. TX L2 Control

BS ID	BS R	Bit	Name	Type	Reset	Description
40	R18	1-0	TAG insertion mode	WO	0h	Sets the TAG mode for next frame or current frame. It will have a one time action per frame. After action, software must rearm for a new action 1 cmd per packet. MII_RT_TXCFG0/1[1] TX_AUTO_PREAMBLEn bit (where n = 0 or 1) must be set to 1h. Note: This bit is self cleared.
40	R18	2	VLAN removal	WO	0h	If set, it will remove 4-Bytes of VLAN. This is only valid when TX L2 FIFO is enabled through ICSS_G_CFG[1] TX_L2_ENABLE bit (value 1h) and MII_RT_TXCFG0/1[1] TX_AUTO_PREAMBLEn = 1h (where n = 0 or 1) then Byte13, Byte14, Byte15, Byte16 will get removed. Note: Byte1 is the first byte which is pushed by PRU core. Note that the first 2 bytes of the VLAN must match the value in MII_G_RT_TX_VLAN_TYPE_TAG_PORT0/1[15-0] TX_VLAN_TYPE_TAG bit field (reset state is 81h). If not, the 4-Bytes will NOT get removed. A RXVLANRemoval flag will get set if the action occurred Allow all combos of TAG + VLAN IN. Note: This will be defined in a matrix. Note: This bit is self cleared.
40	R18	4	EXP_FRAME	WO	0h	Must be set for all EXP_FRAME. We have 3 types of frames: • Implicit EXP_FRAME not set PRE_FRAME • Not set SMD == 0xd5 EXP_FRAME (use a SMD_EXP) • EXP_FRAME set PRE_FRAME not set. PRE_FRAME (use MII_G_RT_SMDT1S_CFG .SMDT1S_n for intial and MII_G_RT_SMDT1C_CFG .SMDT1C_n + MII_G_RT_FRAG_CNT_CFG .FRAG_CNT_n for non intial) EXP_FRAME set PRE_FRAME not set. Note: This bit is self cleared on EOF.
40	R18	6	RESERVED	R	0h	Reserved
40	R18	7	EOF_MCRC_REQ	WO		Set this bit before TX L1 FIFO is empty to generate a MCRC vs CRC. Note: This bit is self cleared on EOF.

Table 6-139. TX L2 Control (continued)

BS ID	BS R	Bit	Name	Type	Reset	Description
40	R18	11-8	RESERVED	R	0h	Reserved

Table 6-140. TX L2 Status

BS ID	BS R	Bit	Name	Type	Reset	Description
40	R19	11-0	TXL2ByteSentCount	R	0h	This bit field defines the number of bytes transmitted to TX L1 FIFO. The count will remain persistent until the next frame starts. This will get used to determine the number of bytes which got transmitted after a Preemption event. This includes all data pushed by the PRU core, which did get transmitted. It does not include the CRC.
40	R19	12	RESERVED	R	0h	Reserved
40	R19	13	RXVLAN Removal	R/W1C	0h	This bit will be set when VLAN removal occured. VLAN removal will only occur if TPID value is equal to the value in MII_G_RT_TX_VLAN_TYPE_TAG_PORT0/1[15-0] TX_VLAN_TYPE_TAG bit field (reset state is 81h). Software can clear sticky used for debug.
40	R19	14	RESERVED	R	0h	Reserved
40	R19	15	RESERVED	R	0h	Reserved
40	R19	22-16	TXL2Occ	R	0h	This bit field defines the current number of bytes in TX L2 FIFO. 0h: 0 bytes, or empty FIFO buffer 1h: 1 byte ... 64h = 64 bytes, or full FIFO buffer

Table 6-141. TX L2 TAG Modes

TAG Mode	At	What to Push/Add to the Frame
0	None	Nothing
1	Push TAG1	Byte 13 = VLAN_PORT<1/0>[7-0] Byte 14 = VLAN_PORT<1/0>[15-8] Byte 15 = VLAN_PORT<1/0>[23-16] Byte 16 = VLAN_PORT<1/0>[31-24] Used for Host. Host -> PRU_ICSSG -> add VLAN TAG -> Port SFD offset issues
2	Push TAG2	Byte 13 = HTAG_PORT<1/0>[7-0] Byte 14 = HTAG_PORT<1/0>[15-8] Byte 15 = HTAG_PORT<1/0>[23-16] Byte 16 = HTAG_PORT<1/0>[31-24] Byte 17 = SEQ_PORT<1/0>[7-0] Byte 18 = SEQ_PORT<1/0>[15-8]

Table 6-141. TX L2 TAG Modes (continued)

TAG Mode	At	What to Push/Add to the Frame
3	Push TAG3	Byte 13 = VLAN_PORT<1/0>[7-0] Byte 14 = VLAN_PORT<1/0>[15-8] Byte 15 = VLAN_PORT<1/0>[23-16] Byte 16 = VLAN_PORT<1/0>[31-24] Byte 17 = HTAG_PORT<1/0>[7-0] Byte 18 = HTAG_PORT<1/0>[15-8] Byte 19 = HTAG_PORT<1/0>[23-16] Byte 20 = HTAG_PORT<1/0>[31-24] Byte 21 = SEQ_PORT<1/0>[7-0] Byte 22 = SEQ_PORT<1/0>[15-8]

6.4.11.2.4.1.1.3 TX Insertion

There are 3 TAG Insertion modes that software can select. Note that the mode must be selected before the first byte is pushed into the TX FIFO. The values, pushed into the TX FIFO are defined in the MII_RT_TX_FIFO_LEVEL0/1[7-0] TX_FIFO_LEVELn registers (where n = 0 or 1).

Table 6-142. TX VLAN_TAG Cases

Case	RM VLAN	ADD VLAN	ADD HSR	In packet	Out packet
1	1	0	0	If pkt[B13:B14] == vlan_type_id	B16, B15, B14, B13 will be removed. If packet is less than 64-Bytes, 0s will get added before the CRC.
2	1	0	0	If pkt[B13:B14] != vlan_type_id	No effect.
3	0	1	0	X	VLAN_TAG added 4-Bytes. Start B13.
4	0	0	1	X	HSR_TAG added 6-Bytes. Start B13.
5	0	1	1	X	VLAN+TAG and HSR_TAG added 10-Bytes. Start B13.
6	1	1	0	If pkt[B13:B14] == vlan_type_id	B16, B15, B14, B13 will be replaced with VLAN_TAG.
7	1	1	0	If pkt[B13:B14] != vlan_type_id	No effect.
8	1	1	1	If pkt[B13:B14] == vlan_type_id	B16, B15, B14, B13 will be replaced with VLAN_TAG. Then HSR_TAG wil be added.
9	1	1	1	If pkt[B13:B14] != vlan_type_id	No effect.
10	1	0	1	If pkt[B13:B14] = vlan_type_id	B16, B15, B14, B13 will be removed and HSR_TAG added 6-Bytes. Start B13.
11	1	0	1	If pkt[B13:B14] != vlan_type_id	HSR_TAG added 6-Bytes. Start B13

6.4.11.2.4.1.1.4 TX Preemption

Case 1) Preemptible frame which got fragmented.

1. Idle -> preemptible frame when:
    - PRE_FRAME is set before first data push
2. preemptible -> frag when
    - EOF_MCRC_REQ is set after the last data is pushed into TX L2 FIFO and before TX L1 FIFO is empty

3. frag -> frag when
   - PRE_FRAME is set before first data push and EOF_MCRC_REQ is set after the last data is pushed into TX L2 FIFO and before TX L1 FIFO is empty
4. frag -> lfrag when:
   - PRE_FRAME is set before first data push and TX_EOF_REQ set after the last data is pushed into TX L2 FIFO and before TX L1 FIFO is empty
5. lfrag -> Idle when CRC is pushed into TX L1 FIFO

Case 2) Preemptible frame which did not get fragmented.

1. Idle -> preemptible frame when:
   - PRE_FRAME is set before first data push
2. preemptible -> Idle when
   - TX_EOF_REQ is set before TX L1 FIFO is empty

Note: Express frames can and will occur between the fragments.

Rules:

- Preemptible must get set before the first data is pushed into TX L2 FIFO
- EOF_MCRC_REQ is set after the last data is pushed into TX L2 FIFO and before TX L1 FIFO is empty
- TX_EOF_REQ can only get asserted on the last frag or preemptible frame which did not get fragmented. It can not get asserted in none last fragments.

Note: TX_EOF_REQ can not get asserted when EOF_MCRC_REQ is asserted.

6.4.11.2.4.1.1.4.1 TX Preemption Programming Model

Start a new frame.

1. Wait until R31.TX_EOF event
2. Load data into TX L2 FIFO until the full frame is completed
3. Issue a R30.TX_EOF + TX_CRC_HIGH + TX_CRC_LOW

Figure 6-96 shows the R30 transmit interface. The lower 16 bits of the R30 (or FIFO transmit word) contain transmit data nibbles. When MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h - default value (where n = 0 or 1), then the upper 16 bits contain mask information. Alternatively, when MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 1h (where n = 0 or 1), then the upper 16 bits contain transmit data nibbles. The operation to be performed on the transmit interface is controlled by PRU writes to the R31 command interface. Table 6-142 describes the supported configurations for 8, 16, and 32 bit TX push operations.

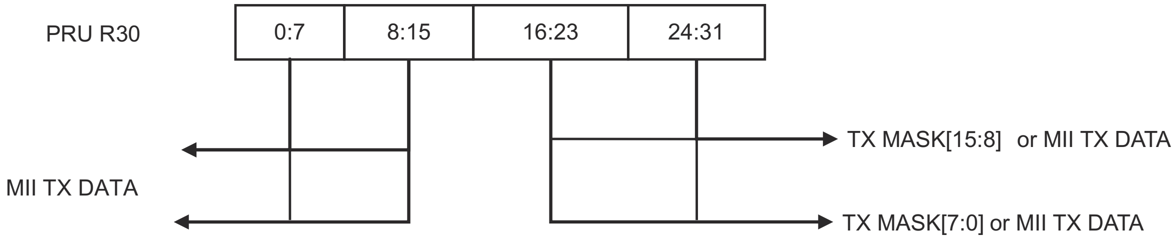

Figure 6-96. PRU to TX MII Interface

Table 6-143. TX Push

R31[25] TX_PUSH16/32	R31[24] TX_PUSH8/32	Supported R30 bits	TX_32_MODE_EN	TX_BYTE_SWAP	TX Push Action
0	1	X	0	X	8 bits of TXDATA (R30[7-0]) pushed post TX mask

Table 6-143. TX Push (continued)

R31[25] TX_PUSH16/32	R31[24] TX_PUSH8/32	Supported R30 bits	TX_32_MODE_EN	TX_BYTE_SWAP	TX Push Action
1	0	X	0	X	16 bits of TXDATA (R30[15-0]) pushed post TX mask
1	1	X	0	X	Illegal
X	X	0x000000FF	1	0	8 bits of TXDATA (R30[7-0]) pushed
X	X	0x0000FFFF	1	0	16 bits of TXDATA (R30[15-0]) pushed
X	X	0xFFFFFFFF	1	X	32 bits of TXDATA (R30[31-0]) pushed
X	X	All other - reserved	1	X	Reserved

Using MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h and the TX mask, the PRU can send a mix of R30 and RX L1 FIFO data to the TX L1 FIFO. Note the TX mask is only available when the PRU is fed one word or byte at a time by the RX L1 FIFO. It is not applicable when the RX L2 buffer is enabled. To disable TX mask, set TXMASK to 0xFFFF.

As shown in Figure 6-97, the PRU drives the MII transmit interface through its R30 register. The contents of R30 and RX data from the receive interface (RX L1 FIFO) are taken and fed into a 40-Bytes transmit FIFO (TX L1 FIFO).

If MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h (where n = 0 or 1), then before transmission, a mask is applied to the data portion of the R30 register. By using the mask, the PRU firmware can control whether received data from the RX L1 FIFO is sent to transmit, R30 data is sent to transmit, or a mix of the two is sent. The Boolean equation that is used by MII_RT to compose TX data is:

TXDATA[7/15-0] = (R30[7/15-0] & MASK[7/15-0]) | (RXDATA[7/15-0] & ~MASK [7/15-0])

As shown in the equation, a mask of FFh will lead to the R30[7:0] being transmitted in an 8-bit transmit operation. A mask of 0h will lead to receive data being sent out in a 16-bit transmit operation.

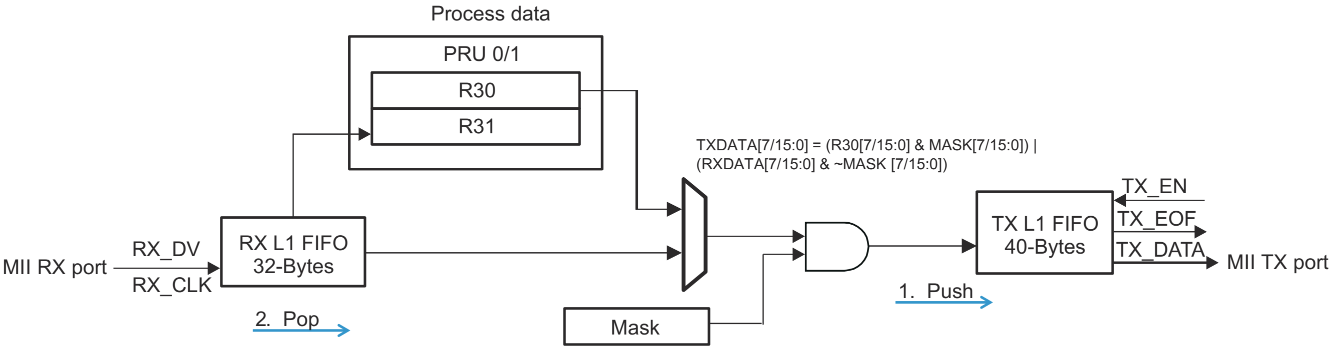

Figure 6-97. TX Mask Mode (MII_RT_TXCFG0/1[TX_32_MODE_ENn] = 0h)

6.4.11.2.4.1.2 RX L1 FIFO → TX L1 FIFO (Direct Connection) → TX MII Port

When MII_RT_TXCFG0/1[9] PRE_TX_AUTO_SEQUENCEn is set to 1h (where n = 0 or 1), the data frame is passed from the RX L1 FIFO to TX L1 FIFO without any interaction of the PRU. This mode of operations is shown in Figure 6-98. The RX L1 FIFO will push data into TX L1 FIFO as long as it is enabled and not full.

There is no PRU dependency in this mode and no option for the PRU to perform any operation to the TX L1 FIFO. RX_RESET clears all data and status elements.

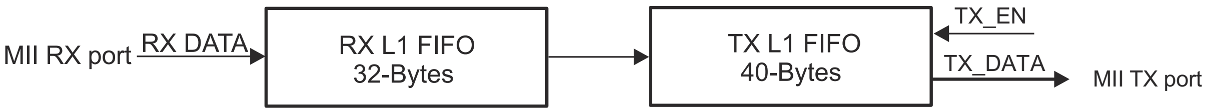

Figure 6-98. RX L1 to TX L1 Interface

For ESC protocols, software should enable [6]RX_AUTO_FWD_PRE0/1 and [4]RX_L2_EN0/1 bits in MII_RT_RXCFG0/1 registers.

For non ESC protocols, software can enable MII_RT_TXCFG0/1[1] TX_AUTO_PREAMBLEn and MII_RT_RXCFG0/1[2] RX_CUT_PREAMBLEn bit (where n = 0 or 1) to insure full preamble is generated for each TX frame.

The PRU core can read the passing through frame by polling the standard R31 register. In Direct mode, the PRU R31 Command is ignored and disabled, except for TX_RESET and RX_RESET.

The following are the legal configurations supported for Direct Connection:

- Configuration 1:
  - PORT1.RX -> PRU1 (snoop only)
  - PORT1.RX -> PORT0.TX
- Configuration 2:
  - PORT0.RX -> PRU0 (snoop only)
  - PORT0.RX -> PORT1.TX
- Configuration 3:
  - PORT1.RX -> PORT1.TX
- Configuration 4:
  - PORT0.RX -> PORT0.TX

6.4.11.2.5 PRU R31 Command Interface

The PRU uses writes to R31[31-16] to control the reception and transmission of packets in direct and register mode. Table 6-143 lists the available commands. Each bit in the table is a single clock pulse output from the PRU. When more than one action is to be performed in the same instant, the PRU firmware must set those command bits in one instruction.

Table 6-144. PRU R31: Command Interface (Write Mode)

Bit	Command	Description
31	TX_CRC_ERR	TX_CRC_ERR command when set will add 0xA5 byte to the TX L1 FIFO if the current FCS is valid. This bit can only be set with the TX_EOF command and optionally with the TX_ERROR_NIBBLE command. It cannot get set with any other commands, and the PRU firmware must wait > 2 clocks from the last command. Note: For proper operations auto-forward preamble must be enabled.
30	TX_RESET	TX_RESET command is used to reset the transmit FIFO and clear all its contents. This is required to recover from a TX FIFO overrun.
29	TX_EOF	TX_EOF command is used to indicate that the data loaded is considered last for the current frame
28	TX_ERROR_NIBBLE	TX_ERROR_NIBBLE command is used to insert an error nibble. This makes the frame invalid. Also, it will add 0x0 after the 32-bit CRC.
27	TX_CRC_HIGH	TX_CRC_HIGH command ends the CRC calculations and pushes CRC[31-16] to append to the outgoing frame in the TX L1 FIFO. Note: TX_CRC0/1 will become valid after 6 clock cycles.
26	TX_CRC_LOW	TX_CRC_LOW command pushes CRC[15-0] to append to the outgoing frame in the TX L1 FIFO.
25	TX_PUSH16	TX_PUSH16 command pushes R30[15-0] when MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h (where n = 0 or 1). See Table 6-142,*TX Push* for more details. Note: There are no restrictions on concurrent PUSH/POP nor R30 requirements to maintain data. Back to back PUSH is supported.

Table 6-144. PRU R31: Command Interface (Write Mode) (continued)

Bit	Command	Description
24	TX_PUSH8	TX_PUSH8 command pushes R30[7-0] when MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h (where n = 0 or 1). See Table 6-142,*TX Push* for more details. Note: There are no restrictions on concurrent PUSH/POP nor R30 requirements to maintain data. Back to back PUSH is supported.
23	RX_ ERROR_CLR	RX_ERROR_CLR command is used to clear RX_ ERROR indicator bit by writing 1h.
22	RX_EOF_CLR	RX_EOF_CLR command is used to clear RX_EOF status indicator bit by writing 1h.
21	RX_SFD_CLR	RX_SFD_CLR command is used to clear RX_SFD indicator bit by writing 1h.
20	RX_SOF_CLR	RX_SOF_CLR command is used to clear RX_SOF indicator bit by writing 1h.
19	Reserved	Reserved
18	RX_RESET	RX_RESET is used to reset the receive FIFO and clear all contents. This is required to recover from a RX FIFO overrun, if software does not want to undrain. The typical use case is assertion after RX_EOF. If asserted during an active frame, the following actions will occur: 1. Terminate the current frame 2. Block/terminate all new data 3. Flush/clear all FIFO elements 4. Cause RX state machine into an idle state 5. Cause EOF event 6. Cause minimum frame error, if you abort before minimum size reached
17	RX_POP16	RX_POP16 command advances the receive traffic by two bytes. This is only required when you are using R31 to read the data. After R31[15-0] is ready to read by PRU, it will set 1h to WORD_RDY, and the next new data will be allowed to advance. RX_POP16 to WORD_RDY update has 2 clock cycles latency. Firmware needs to insure it does not read WORD_RDY/BYTE_RDY until 2 clock cycles after RX_POP16.
16	RX_POP8	RX_POP8 command advances the receive traffic by one bytes. This is only required when you are using R31 to read the data. After R31[7-0] is ready to read by PRU, it will set 1h to BYTE_RDY, and the next new data will be allowed to advance. RX_POP8 to BYTE_RDY update has 2 clock cycles latency. Firmware needs to insure it does not read WORD_RDY/BYTE_RDY until 2 clock cycles after RX_POP8.

6.4.11.2.6 Other Configuration Options

6.4.11.2.6.1 Nibble and Byte Order

The PRU core is little endian. To support big endian, the MII_G_RT supports optional nibble swapping on both the RX and TX side.

On the receive side, the order of the two data bytes in RX R31 and the RX L2 buffer are configurable through the RX_BYTE_SWAP0/1 bit in the MII_RT_RXCFG0/1 registers, as shown in Table 6-144. Note: The Nibble0 is the first nibble received.

Table 6-145. RX Nibble and Byte Order

Configuration	Order
MII_RT_RXCFG0/1[5] RX_BYTE_SWAPn = 0h (default), where n = 0 or 1	R31[15-8] / RXL2[15-8] = Byte1{Nibble3,Nibble2} R31[7-0] / RXL2[7-0] = Byte0{Nibble1,Nibble0}
MII_RT_RXCFG0/1[5] RX_BYTE_SWAPn = 1h, where n = 0 or 1	R31[15-8] / RXL2[15-8] = Byte0{Nibble1,Nibble0} R31[7-0] / RXL2[7-0] = Byte1{Nibble3,Nibble2}

On the transmit side, the order of the two data bytes and mask bytes in TX R30 are configurable through the TX_BYTE_SWAP0/1 bit in the MII_RT_TXCFG0/1 registers, as shown in Table 6-145. Note the Nibble0 is the first nibble transmitted.

Table 6-146. TX Nibble and Byte Order

Configuration	Order
MII_RT_TXCFG0/1[3] TX_BYTE_SWAPn = 0h (default), where n = 0 or 1	If MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h, where n = 0 or 1 R30[15-8] = Byte1{Nibble3,Nibble2} R30[7-0] = Byte0{Nibble1,Nibble0} R30[31-24] = TX_MASK[15-8] R30[23-16] = TX_MASK[7-0] If MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 1h, R30[31-24] = Byte3{Nibble7,Nibble6} R30[23-16] = Byte2{Nibble5,Nibble4} R30[15-8] = Byte1{Nibble3,Nibble2} R30[7-0] = Byte0{Nibble1,Nibble0}
MII_RT_TXCFG0/1[3] TX_BYTE_SWAPn = 1h, where n = 0 or 1	If MII_RT_TXCFG0/1[11] TX_32_MODE_EN = 0h, R30[15-8] = Byte0{Nibble1,Nibble0} R30[7-0] = Byte1{Nibble3,Nibble2} R30[31-24] = TX_MASK[7-0] R30[23-16] = TX_MASK[15-8] If MII_RT_TXCFG0/1[11] TX_32_MODE_EN = 1h, Only 32-bit push is supported. R30[31-24] = Byte0{Nibble1,Nibble0} R30[23-16] = Byte1{Nibble3,Nibble2} R30[15-8] = Byte2{Nibble5,Nibble4} R30[7-0] = Byte3{Nibble7,Nibble6}

6.4.11.2.6.2 MII_G_RT Preamble Source

The MII_G_RT module has the option to preserve and forward a received preamble in the TX data stream, use a preamble provided by the PRU, or auto-generate a preamble. These configurations are highlighted in Table 6-146.

Table 6-147. Preamble Configuration Options

RX_CUT_PREAMBLE	Determines whether RX preamble is passed to the RX L1/L2 FIFO
RX_AUTO_FWD_PRE	Determines whether RX preamble is automatically passed to TX L1 FIFO
TX_AUTO_PREAMBLE	TX interface logic auto-generates and appends preamble to TX data stream with the first push of data into the TX L1 FIFO. Note that enabling this option does fill the TX FIFO with the preamble length, hence software has to consider this to not overrun the TX FIFO.

6.4.11.2.6.3 PRU and MII Port Multiplexer

The MII_G_RT module supports configurable PRU core to MII TXn / RXn port mapping. By default, PRU0 is mapped to TX1 and RX0 and PRU1 is mapped to TX0 and RX1. However, the system supports the flexibility to map any PRU core to any TX and RX port. For example, the input to PRU0 can be either RX_MII0 or RX_MII1. Similarly, the input to TX_MII0 can be either PRU0 or PRU1.

6.4.11.2.6.3.1 Receive Multiplexer

A multiplexer is provided to allow selecting either of the two MII interfaces (RX_MII0 or RX_MII1) for the receive data that is sent to PRU. Figure 6-99 shows a simple diagram of PRU receive multiplexer.

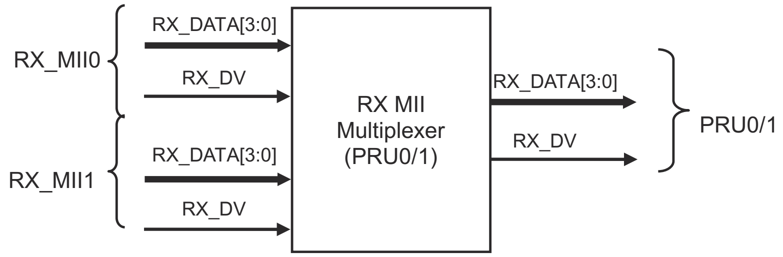

Figure 6-99. MII Receive Multiplexer

There are two receive multiplexer instances to enable selection of RX MII path for each PRU. The select lines of the RX multiplexers are driven from the PRU_ICSSG programmable registers (MII_RT_RXCFG0/1[3] RX_MUX_SELn, where n = 0 or 1).

6.4.11.2.6.3.2 Transmit Multiplexer

On the MII transmit ports, there is a multiplexer for each MII transmit port that enables selection of either the transmit data from the PRUs or from the RX MII interface of the other MII interface. Figure 6-100 shows a simple diagram of PRU transmit multiplexer.

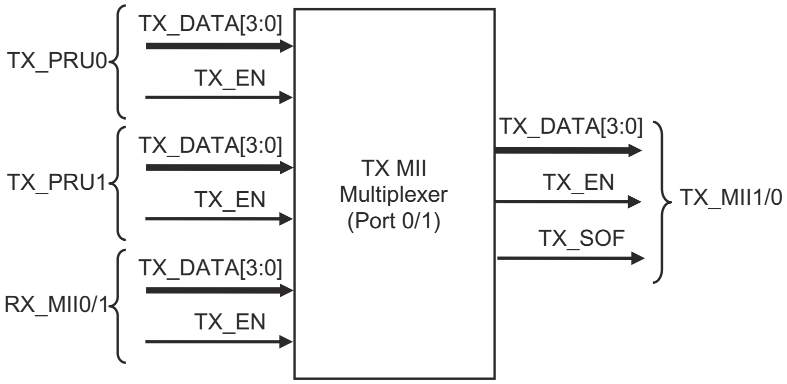

Figure 6-100. MII Transmit Multiplexer

The transmit multiplexers enable the PRU_ICSSG to either operate in a bypass mode where the PRU is not involved in processing MII traffic or use of one of the PRU cores for transmitting data into the MII interface. There are two instances of the TX MII multiplexer and the select lines for each TX multiplexer are provided by the PRU_ICSSG programmable registers (MII_RT_TXCFG0/1[8] TX_MUX_SELn, where n = 0 or 1). The select lines are common between register and FIFO interface. It is expected that the select lines will not change during the course of a frame so that can avoid data exchange error.

6.4.11.2.6.4 RX L2 Scratch Pad

When the RX L2 is disabled (MII_RT_RXCFG0/1[4] RX_L2_ENn = 0h, where n = 0 or 1), the RX L2 banks can be used as a generic scratch pad. In scratch pad mode, RX L2 Bank0 and RX L2 Bank1 operate like simple read/write memory mapped registers. All XFR size and start operations are supported. RX_RESET has no effect in this mode. This mode is shown in Figure 6-101.

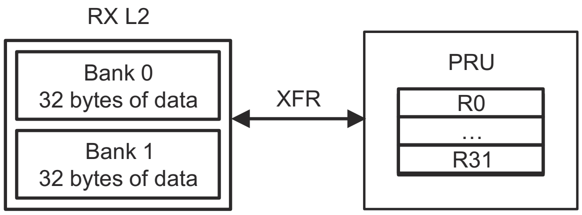

Figure 6-101. Scratch Pad Mode

6.4.11.3 PRU_ICSSG PA_STATS Module

The statistics engine module (PA_STATS) is used to accelerate the task of incrementing and collecting statistics of traffic inside Packet Accelerator subsystem.

Figure 6-102 shows an overview of the PA_STATS module.

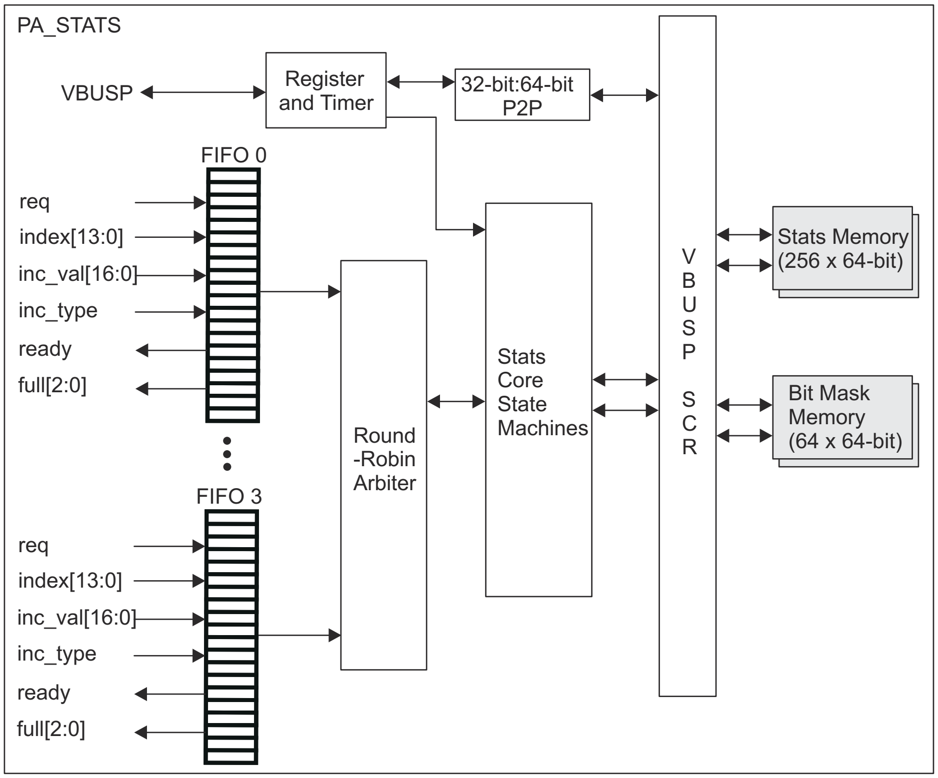

Figure 6-102. PRU_ICSSG PA_STATS Module Overview

The statistics engine has 4 PRU statistics ports, which allow 4 PRU cores or other modules to write statistics commands to the engine simultaneously. In order to allow the engine to accept multiple commands, each port has a 8 entry command FIFO, allowing for up to 8 statistics commands to be written per port before a command could be dropped due to lack of storage. Each PRU in the PA (Packet Accelerator) flow exports byte strobes for both R0 and R31 registers to the statistics engine, however, only a write to R31 register will trigger statistics operation. That trigger is the assertion of request for 1 cycle and at the same clock request is asserted index, inc_val and inc_type must be valid.

The below Table 6-147 shows statistic input ports.

Table 6-148. Statistic Input Ports

Statistic Input Ports			
Bit Field	**PRU Registers**	**Bits**	**Definition**
req	R31[15]	1	Asserted for 1 cycle for each stat increment.
inc_type	R31[14]	1	0h: indicates that the statistic should increment by 1. 1h: indicates that the statistic should increment by the 'inc_val' field.
index	R31[13:0]	14	Indicates which statistic in the memory will be incremented. Acceptable input range for this implementation is 1 … FFFh.
inc_val	R0[16:0]	17	Indicates the increment value if inc_type is 1. If inc_type is 0 this field is ignored.

The statistics engine outputs three status bits per statistics port, as shown in Table 6-148

Table 6-149. Statistics Port Status

Statistic Input Ports			
Bit Field	**PRU Registers**	**Bits**	**Definition**
2	R31[2]	1	Set when at least 8 entries in the statistics port FIFO are free.
1	R31[1]	1	Set when at least 4 entries in the statistics port FIFO are free.
0	R31[0]	1	Set when at least 1 entry in the statistics port FIFO is free.

The ‘ready’ output port is provided for future compatibility.

6.4.11.3.1 Statistics Page

The statistics counters are implemented in 2KB memory which can hold a maximum of 512 32-bit counters. These counters can be made into 64-bit counters by specifying the number of 64-bit counters in the Counter Allocation Register (address offset 8h). The default register configuration is 256 64-bit counters and 512 32-bit counters. The 64-bit counters are all placed before the 32-bit counters. The index for 64-bit counters is always an even number and starts from 0. For example if Counter Allocation Register (address offset 8h) is configured to be 5, then statistics at index 0, 2, 4, 6 and 8 are 64-bit stats; index 10,11,12,13,…,511 are all 32-bit stats. All counters are cleared to “0” upon hardware reset or software reset ([31-0] TRIGGER).

To allow both sending of statistics packet to the host and stats update happen simultaneously, the module has a second statistics page and the engine can ping-pong between them. The ‘Active’ label in Figure 6-103 indicates which page is currently processing new stat bumps. The ping-pong approach allows the engine to get snapshot of the active page and send them based on certain events (timer expiration, an input packet with ‘send update’ command), while the other page resumes processing of new increments. In Figure 6-103 page A is initially the active page, and page B is the page that will become the active page when the engine goes into output phase.

After the output phase, there is a ‘merging’ between the two pages to ensure the new active page reflects the latest stats count and the bit masks. This process occurs as a background task and runs at slow interval (every 8 cycles) to minimize bandwidth impact. After the merging process is complete, the state machine resets the applied bit mask to all 1s and reset the counters in the non-active page to all 0s (reset phase). The engine then goes back to a steady state in which new bumps are handled in the active page and the stats in the non-active page are all zero.

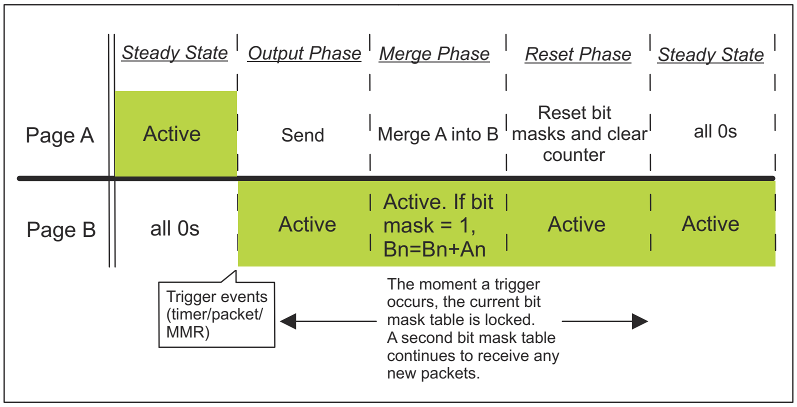

Figure 6-103. Merging between Two Pages

6.4.11.3.2 Statistics Collection Modes

There are two ways to collect the statistics: packet based and manual read to the register space. The most efficient and effective way of the getting the stats are by using packet. The advantage is that software has a global pointer that is always pointed to the ‘stats page’. When software receives a new packet with the latest stats, software keeps these stats where the CPPI DMA places them and change the global pointer to point to the new ‘stats page’. This way software benefits from having “free” stats delivery, and although the stats engine only sends to one host, the host can easily forward the statistics packet to other cores in multi-cores system.

6.4.11.3.2.1 Manual Read Mode

Host can issue read on specific counter and the read data comes from the active page. This is especially useful for debug purpose, or when the timer is disabled and the host manually reads the stats. The bit mask table has no effect on the counter on manual read. There are two register addresses for every statistics counter. One address is used for query mode (read and not clear), and another is used for collect mode (read and clear). Note that issuing two 32-bit reads through the 32-bit configuration bus for reading a 64-bit stat can be unreliable, because there may be latency between the two reads and a stat bump can occur in between. This may be unavoidable for Arm cores, but for cores that can issue burst read, such as DSPs, the statistics engine will ensure that reads on 64-bit counter value is treated as atomic operation. However, the module does not support read burst on multiple counters using collect (read and clear) mode.

When reading a 64-bit counter in collect mode through the 32-bit configuration bus, each 32-bit portion of the counter is cleared immediately after the read.

6.4.11.3.3 Clock Stop

To initiate clock stop procedure, CLKSTOP_REQ input needs to be asserted and stays asserted until the statistics engine acknowledges the clock stop request, which indicates that it is safe to turn off the clock (CLKSTOP_ACK output is 1). After CLKSTOP_REQ is asserted, no additional packet or configuration access should be sent to the stats engine. Stats engine will ensure that all pending stats bumps requests have been processed (all FIFOs are empty), before issuing CLKSTOP_ACK. In addition, to prevent timer interrupt, the timer is paused when CLKSTOP_REQ = 1.

6.4.12 PRU_ICSSG MII MDIO Module

This section describes the PRU_ICSSGn (where n = 0 or 1) integrated MII management interface (MII_MDIO module).

6.4.12.1 PRU_ICSSG MII MDIO Overview

The following features are supported:

- Clause 22 and Clause 45.
- Up to 32 PHY addresses.
- Two user access registers to control and monitor up to two PHYs simultaneously.
- Target interface for configuration and control (MII RT MDIO CFG)
- Each PHY can be individually enabled to be polled.
- The inter-poll gap between PHY polls can be changed.
- State Change Mode of operation to monitor up to 32 PHYs simultaneously.
- Manual control by software for GPIO operations.

The PRU_ICSSG MII MDIO management I/F module implements the *802.3 serial management interface* to interrogate and control two Ethernet PHYs simultaneously using a shared two-wire bus. Figure 6-104 shows a device with two MACs, each connected to an Ethernet PHY, being managed by the MII interface module using a shared bus.

The Figure 6-104 gives an overview of the MII MDIO management interface.

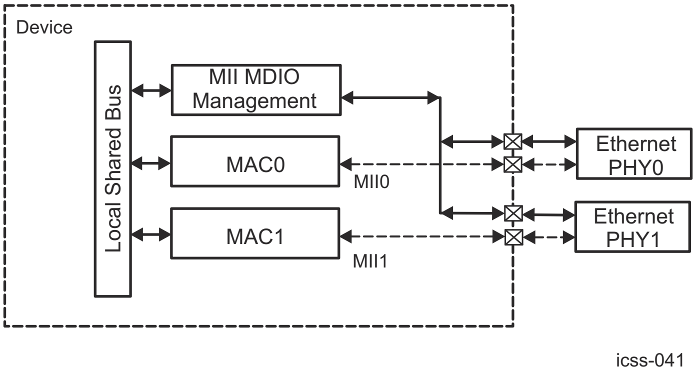

Figure 6-104. Device PRU_ICSSG MII MDIO Management Interface Overview

6.4.12.2 PRU_ICSSG MII MDIO Functional Description

The MII Management interface incorporates:

- *MDIO Registers* - The MDIO register block provides a VBUSP 3.0 compliant target interface to the MDIO module. Host interaction with this module is facilitated through the registers in this block.
- *Control and Schedule* - The control and register logic in the MDIO module contain the state machine and scheduling logic which control the wire side operation.
- *MDIO Interface* - The MDIO interface block provides the serial interface to the MDIO interface.

The MDIO logic is fully synchronous to the PRU_ICSSG local shared bus clock.

6.4.12.2.1 MDIO Clause 22 Frame Formats

The below Table 6-149 shows the read and write format of the Clause 22 Management interface frames.

Table 6-150. MDIO Clause 22 Frame Formats

Preamble	Start Delimiter	Operation Code	PHY Address	Register Address	Turnaround	Data
MDIO Clause 22 Read Frame Format						
FFFFFFFFh	01	10	AAAAA	RRRRR	Z0	DDDD.DDDD.DDDD.DDDD
MDIO Clause 22 Write Frame Format						

Table 6-150. MDIO Clause 22 Frame Formats (continued)

Preamble	Start Delimiter	Operation Code	PHY Address	Register Address	Turnaround	Data
FFFFFFFFh	01	01	AAAAA	RRRRR	10	DDDD.DDDD.DDDD.DDDD

The default or idle state of the two wire serial interface is a logic one. All tri-state drivers should be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic one. Prior to initiating any other transaction, the station management entity shall send a preamble sequence of 32 contiguous logic one bits on the MDIO line with 32 corresponding cycles on MDCLK to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding MDCLK cycles before it responds to any other transaction.

Preamble
The start of a frame is indicated by a preamble, which consists of a sequence of 32 contiguous bits all of which are a "1". This sequence provides the Ethernet PHY a pattern to use to establish synchronization.

Start Delimiter
The preamble is followed by the start delimiter which is indicated by a "01" pattern. The pattern assures transitions from the default logic one state to zero and back to one.

Operation Code
The operation code for a read is "10", while the operation code for a write is a "01".

Ethernet PHY Address
The PHY address is 5 bits allowing 32 unique values. The first bit transmitted is the MSB of the PHY address.

Register Address
The Register address is 5 bits allowing 32 registers to be addressed within each PHY.

Turnaround
An idle bit time during which no device actively drives the MDIO signal shall be inserted between the *Register Address* field and the *Data* field of a read frame in order to avoid contention. During a read frame, the PHY shall drive a zero bit onto MDIO for the first bit time following the idle bit and preceding the Data field. During a write frame, this field shall consist of a one bit followed by a zero bit.

Data
The Data field is 16 bits. The first bit transmitted and received is the MSB of the data word.

6.4.12.2.1.1 PRU-ICSSG MDIO Control and Interface Signals

The Table 6-150 shows the PRU_ICSSGn (where n = 0 to 2) MII MDIO signals and their availability at the device boundary.

Table 6-151. PRU_ICSSG MII MDIO Control and Interface Signals

MDIO Control Signals			
Pin Name	**Type**	**Available as device I/O**	**Function**
MDIO_LINKINT[1:0]	O	N.A.	Serial interface link change interrupt. Indicates a change in the state of the PHY link.
MDIO_USERINT[1:0]	O	N.A.	Serial interface user command event complete interrupt.
MDIO Interface Signals			
Pin Name	**Type**	**Available as device I/O**	**Function**
MDIO_I	I	device bidirectioanal **pr0_mdio_data**, and pr1_mdio_mdclk pin in input mode	Serial data input
MDIO_O	O	device bidirectional **pr0_mdio_data** and pr1_mdio_mdclk pin in output mode	Serial data output

Table 6-151. PRU_ICSSG MII MDIO Control and Interface Signals (continued)

MDIO Control Signals			
MDIO_OE_N	O	N.A.	Serial data output enable. Asserted "0" when data output is valid
MDCLK_O	O	device output - **pr0_mdio_mdclk** pr1_mdio_mdclk	Serial clock output
MLINK_I[1:0]	I	N.A.	Optional link status inputs from PHY. Each input is connected to a single PHY. Unused inputs are tied ‘0’.

6.4.12.2.2 MDIO Clause 45 Frame Formats

The below Table 6-151 shows the address frame format. Table 6-152 shows read, and write format of the supported Clause 45 frames. Post-increment accesses are not supported.

Table 6-152. MDIO Clause 45 Address Frame Formats

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Address
MDIO Clause 45 Address Frame Format						
FFFFFFFFh	00	00	AAAAA	RRRRR	10	AAAA.AAAA.AAAA.AAAA

Table 6-153. MDIO Clause 45 Frame Formats

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
MDIO Clause 45 Read Frame Format						
FFFFFFFFh	00	11	AAAAA	RRRRR	Z0	DDDD.DDDD.DDDD.DDDD
MDIO Clause 45 Write Frame Format						
FFFFFFFFh	00	01	AAAAA	RRRRR	10	DDDD.DDDD.DDDD.DDDD

The default or idle state of the two wire serial interface is a logic one. All tri-state drivers should be disabled and the PHY’s pull-up resistor should pull the MDIO line to a logic one. Prior to initiating any other transaction, the station management entity shall send a preamble sequence of 32 contiguous logic one bits on the MDIO line with 32 corresponding cycles on MDCLK to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding MDCLK cycles before it responds to any other transaction. The MDIO_USER_ADDR0_REG/ MDIO_USER_ADDR1_REG registers must be written before a read or write operation is performed to set the address used in the operation. Each read or write operation has a preceeding address frame.

Preamble
The start of a frame is indicated by a preamble, which consists of a sequence of 32 contiguous bits all of which are a “1”. This sequence provides the PHY a pattern to use to establish synchronization. The preamble is required in clause 45 operation.

Start Delimiter
The preamble is followed by the start delimiter which is indicated by a “00” pattern.

Operation Code
The operation code for address is “00". The operation code for a read is “11”, while the operation code for a write is a “01”.

Ethernet PHY Address
The PHY address is 5 bits allowing 32 unique values. The first bit transmitted is the MSB of the PHY address.

MMD Number
The MMD number is 5 bits allowing 32 unique values. The first bit transmitted is the MSB.

Turnaround
An idle bit time during which no device actively drives the MDIO signal shall be inserted between the **MMD Number** field and the **Data** field of a read frame in order to avoid contention. During a read frame, the PHY shall drive a zero bit onto MDIO for the first bit time following the idle bit and preceding the Data field. During a write frame, this field shall consist of a one bit followed by a zero bit.

Address
The address field is 16-bits on address operations. The first bit transmitted is the MSB of the address word. Each read/write operation initiated has an automatic address operation initiated first that uses the MDIO_USER_ADDR0_REG[15-0] USER_ADDR0 or MDIO_USER_ADDR1_REG[15-0] USER_ADDR1 register values as the 16-bit address.

Data
The Data field is 16 bits on read and write operations. The first bit transmitted and received is the MSB of the data word.

6.4.12.2.3 PRU_ICSSG MII MDIO Interractions

The MDIO module will remain idle until enabled by setting the [30] ENABLE bit in the MDIO MDIO_CONTROL_REG register. The MDIO will then continuously poll the link status from within the Generic Status Register of all possible 32 PHY addresses in turn recording the results in the MDIO MDIO_LINK_REG register. Individual PHY's can be enabled or disabled for polling through the associated bit in the MDIO MDIO_POLL_EN_REG register. The MDIO MDIO_LINK_REG and MDIO_ALIVE_REG register bit values are updated on the poll of each PHY. In *Normal Mode*, the link status of two of the 32 possible PHY addresses can also be determined using the MLINK pin inputs. The bit [7] LINKSEL in the MDIO MDIO_USER_PHY_SEL_REG_0/1 register determines the status input that is used. A change in the link status of the two PHYs being monitored will set the appropriate bit ([1-0] LINKINTRAW) in the MDIO MDIO_LINK_INT_RAW_REG register and the MDIO_LINK_INT_MASKED_REG[1-0] LINKINTMASKED register, if enabled by the [6] LINKINT_ENABLE bit in the MDIO MDIO_USER_PHY_SEL_REG_0/1 register. In *State Change Mode*, a change in any PHY status will be indicated on the MDIO_LINK_INT_RAW_REG[0] LINKINTRAW interrupt if enabled.

The MDIO MDIO_ALIVE_REG register is updated by the MDIO module if the PHY acknowledged the read of the generic status register. In addition, any PHY register read transactions initiated by the host also cause the MDIO MDIO_ALIVE_REG register to be updated.

At any time, the host can define a transaction for the MDIO module to undertake using the [15-0] DATA, [20-16] PHYADR, [25-21] REGADR, and [30] WRITE fields in a MDIO_USER_ACCESS_REG_0/1 register. When the host sets the [31] GO bit in this register, the MDIO interface module will begin the transaction without any further intervention from the host. Upon completion, the MDIO will clear the [31] GO bit and set the [1-0] USERINTRAW bit field in the MDIO_USER_INT_RAW_REG register corresponding to the MDIO_USER_ACCESS_REG_0/1 register being used. The corresponding bit in the MDIO_USER_INT_MASKED_REG register may also be set depending on the mask setting in the MDIO_USER_INT_MASK_SET_REG and MDIO_USER_INT_MASK_CLEAR_REG registers. A round-robin arbitration scheme is used to schedule transactions which may queued by the host in different MDIO_USER_ACCESS_REG_0/1 registers. The host should check the status of the [31] GO bit in the MDIO_USER_ACCESS_REG_0/1 register before initiating a new transaction to ensure that the previous transaction has completed. The host can use the [29] ACK bit in the MDIO_USER_ACCESS_REG_0/1 register to determine the status of a read transaction.

Software may use the MDIO module to set up the auto-negotiation parameters of each PHY attached to a MAC port, retrieve the negotiation results, and set up the MAC Control register in the corresponding MAC.

6.4.12.2.4 PRU_ICSSG MII MDIO Interrupts

6.4.12.2.4.1 Normal Mode ([30]STATECHANGEMODE = 0h)

The MDIO will assert the MDIO_LINKINT signals if there is a change in the link state of the Ethernet PHY corresponding to the address in the [4-0] PHYADR_MON field of the MDIO MDIO_USER_PHY_SEL_REG_j (where j = 0 or 1) registers and the corresponding [6] LINKINT_ENABLE bit is set. The MDIO_LINKINT event is also captured in the MDIO MDIO_LINK_INT_MASKED_REG register. MDIO_LINKINT[0] and MDIO_LINKINT[1] correspond to the MDIO MDIO_USER_PHY_SEL_REG_0 and MDIO_USER_PHY_SEL_REG_1 registers, respectively.

When the [31] GO bit in the MDIO_USER_ACCESS_REG_j (where j = 0 or 1) registers transitions from ‘1’ to ‘0’, indicating the completion of a user access, and the corresponding [1-0] USERINTMASKSET field in the

MDIO_USER_INT_MASK_SET_REG register is set, the MDIO_USERINT signal is asserted ‘1’. The MDIO_USERINT event is also captured in the MDIO_USER_INT_MASKED_REG register. MDIO_USERINT[0] and MDIO_USERINT[1] correspond to the MDIO_USER_ACCESS_REG_0 and MDIO_USER_ACCESS_REG_1 registers, respectively.

6.4.12.2.4.2 State Change Mode ([30]STATECHANGEMODE = 1h)

In *State Change Mode*, the MDIO will assert MDIO_LINKINT[0] when any bit in the MDIO MDIO_ALIVE_REG or MDIO MDIO_LINK_REG registers changes due to MDIO operations. The MDIO_LINKINT event is also captured in the MDIO MDIO_LINK_INT_MASKED_REG register. MDIO_LINKINT[1] output and the MDIO MDIO_USER_PHY_SEL_REG_j (where j = 0 or 1) registers are unused in *State Change Mode*.

6.4.12.2.5 Manual Mode

Manual Mode allows software to directly control the serial clock output (MDCLK_O), the serial data output enable (MDIO_OE_N), and the serial data output (MDIO_O). The serial data input can also be read (MDIO_I). This mode is enabled when the [31] MANUALMODE bit is set in the MDIO MDIO_POLL_REG register. *Manual Mode* is intended to be used by software for slow speed general purpose IO operations and not for MDIO PHY operations.

6.4.12.3 PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface

To facilitate transmission and reception of serial management frames, the host has to perform the following operations:

- Configure the [20] PREAMBLE and [15-0] CLKDIV fields in the MDIO MDIO_CONTROL_REG register.
- Enable the MDIO module by setting the [30] ENABLE bit in the MDIO MDIO_CONTROL_REG register. If Byte access is being used, the [30] ENABLE bit should be written last.
- The MDIO MDIO_ALIVE_REG register can be read after a delay to determine which Ethernet PHYs responded.
- Set up the appropriate PHY addresses in the MDIO MDIO_USER_PHY_SEL_REG_j[4-0] PHYADR_MON bits.
- Set up the appropriate [6] LINKINT_ENABLE bit in the MDIO MDIO_USER_PHY_SEL_REG_j registers.
- Set up the appropriate [7] LINKSEL bits in the MDIO MDIO_USER_PHY_SEL_REG_j registers.
- Set up the appropriate [1-0] USERINTMASKEDSET field in the MDIO MDIO_USER_INT_MASK_SET_REG register.
- To write to an Ethernet PHY register the host should first check to ensure that the [31] GO bit in a MDIO MDIO_USER_ACCESS_REG_j registers is cleared. The [31] GO, [30] WRITE, [25-21] REGADR, [20-16] PHYADR and data fields in that MDIO MDIO_USER_ACCESS_REG_j registers can then be updated to the appropriate value. If byte access is being used, the [31] GO bit should be written last. The write operation to the PHY will be scheduled and completed by the module. Completion of the write operation can be determined by examining the [31] GO bit in the MDIO MDIO_USER_ACCESS_REG_j registers. It also results in a transition on the appropriate MDIO_INT signal and the corresponding bit in the MDIO MDIO_USER_INT_MASKED_REG register based on the setting of the MDIO MDIO_USER_INT_MASK_SET_REG register.
- To read from an Ethernet PHY register the host should first check to ensure that the [31] GO bit in a MDIO MDIO_USER_ACCESS_REG_j registers is cleared. The [31] GO, [25-21] REGADR, and [20-16] PHYADR fields in that MDIO MDIO_USER_ACCESS_REG_j registers can then be updated to the appropriate value. The read data value will be available in the [15-0] DATA field of the MDIO MDIO_USER_ACCESS_REG_j registers after the module completes the read operation on the serial bus. The completion of the read operation can be determined by examining the [31] GO and [29] ACK bits in the

MDIO MDIO_USER_ACCESS_REG_j registers. It also results in a transition on the appropriate MDIO_INT signal and the corresponding bit in the MDIO MDIO_USER_INT_MASKED_REG register based on the setting of the MDIO MDIO_USER_INT_MASK_SET_REG register.

- The module de-asserts the MDIO_USERINT signal when the host writes to the appropriate [1-0] USERINTMASKED bit field in the MDIO MDIO_USER_INT_MASKED_REG register or the [1-0] USERINTRAW bit field in the MDIO MDIO_USER_INT_RAW_REG register.
- The host can poll the MDIO MDIO_LINK_REG register periodically or use the MDIO_LINKINT signals to determine the state of the serial interface to a particular Ethernet PHY.
- The module de-asserts the MDIO_LINKINT when the host writes to the appropriate [1-0] LINKINTRAW bit field in the MDIO_MDIO LINK_INT_RAW_REG register or the [1-0] LINKINTMASKED bit field in the MDIO_MDIO LINK_INT_MASKED_REG register.

Table 6-154. Summary of the PRU_ICSSG MII MDIO Functional Registers

Address Offset	Register Mnemonic	Register Name	Register Purpose
00h	**MDIOVer**	MDIO_MDIO_VERSION_REG	Module version register
04h	**MDIOControl**	MDIO_CONTROL_REG	Module control register
08h	**MDIOAlive**	MDIO_ALIVE_REG	Ethernet PHY acknowledge status register
0Ch	**MDIOLink**	MDIO_LINK_REG	Ethernet PHY link status register
10h	**MDIOLinkIntRaw**	MDIO_LINK_INT_RAW_REG	Link status change interrupt register (raw value)
14h	**MDIOLinkIntMasked**	MDIO_LINK_INT_MASKED_REG	Link status change interrupt register (masked value)
18h	**MDIOLinkIntMaskSet**	MDIO_LINK_INT_MASK_SET_REG	Link status change interrupt mask set register
1Ch	**MDIOLinkIntMaskClr**	MDIO_LINK_INT_MASK_CLEAR_REG	Link status change interrupt mask clear register
20h	**MDIOUserIntRaw**	MDIO_USER_INT_RAW_REG	User command complete interrupt register (raw value)
24h	**MDIOUserIntMasked**	MDIO_USER_INT_MASKED_REG	User command complete interrupt register (masked value)
28h	**MDIOUserIntMaskSet**	MDIO_USER_INT_MASK_SET_REG	User interrupt mask set register
2Ch	**MDIOUserIntMaskClr**	MDIO_USER_INT_MASK_CLEAR_REG	User interrupt mask clear register
30h	**MDIOManual_IF**	MDIO_MANUAL_IF_REG	Manual interface register
34h	**MDIOPoll_IPG**	MDIO_POLL_REG	Poll and IPG register
38h	**MDIOPoll_En**	MDIO_POLL_EN_REG	Poll Enable register
3Ch	**MDIOClause**	MDIO_CLAUS45_REG	Clause 22 or 45 enable register
40h	**MDIOUser_Addr0**	MDIO_USER_ADDR0_REG	User Address register 0
44h	**MDIOUser_Addr1**	MDIO_USER_ADDR1_REG	User Address register 1
48h – 7Ch	**Reserved**	-	Reserved
80h	**MDIOUserAccess0**	MDIO_USER_ACCESS_REG_0	User access register 0

Table 6-154. Summary of the PRU_ICSSG MII MDIO Functional Registers (continued)

Address Offset	Register Mnemonic	Register Name	Register Purpose
84h	**MDIOUserPhySel0**	MDIO_USER_PHY_SEL_REG_0	User PHY select register 0
88h	**MDIOUserAccess1**	MDIO_USER_ACCESS_REG_1	User access register 1
8Ch	**MDIOUserPhySel1**	MDIO_USER_PHY_SEL_REG_1	User PHY select register 1
90h – FFh	**Reserved**	-	Reserved

6.4.13 PRU_ICSSG IEP

This section describes the Industrial Ethernet Peripheral (IEP) Module which is part of the PRU_ICSSG.

6.4.13.1 PRU_ICSSG IEP Overview

The Industrial Ethernet Peripheral (IEP) performs hardware work required for Industrial Ethernet functions. The IEP module features an industrial ethernet timer with 16 compare events, industrial ethernet sync generator and latch capture, industrial ethernet watchdog timer, and a digital I/O port (DIGIO).

6.4.13.2 PRU_ICSSG IEP Functional Description

This section provides the functional description of the IEP components. The PRU_ICSSG module implements two Industrial Ethernet Peripherals (IEP0 and IEP1). Each of the IEP modules is fully independent with one exception, which is IEP1 controller counter [63:0] can come from IEP0 counter [63:0]. This dependency is called IEP1 target mode and this mode can be enabled through ICSSG_IEPCLK_REG[1] IEP1_SLV_EN bit. The IEP functional block diagram is shown in Figure 6-105.

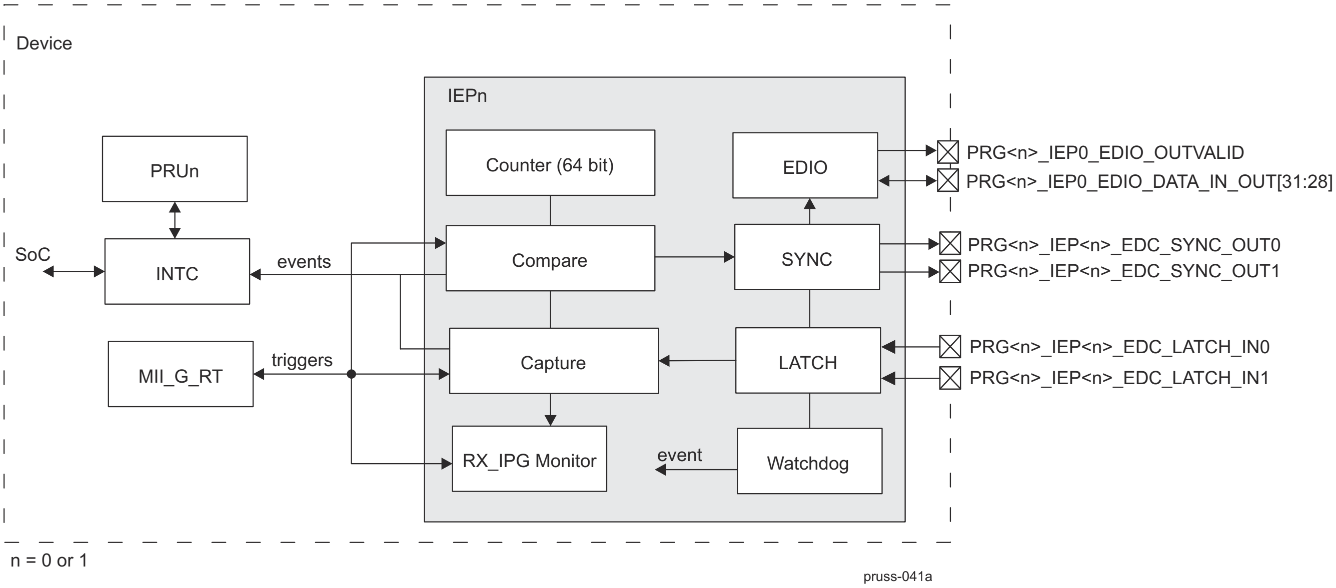

Figure 6-105. IEP Functional Block Diagram

6.4.13.2.1 PRU_ICSSG IEP Clock Generation

The IEP has a selectable module input clock (ICSSGn_IEP_CLK, see also *PRU_ICSSG Integration*). The clock source is selected by the state of the CTRLMMR_ICSSGn_CLKSEL[19-16] IEP_CLKSEL bit within the CTRL_MMR0 register space. Two clock sources are supported for the IEP input clock:

- ICSSGn_IEP_CLK (where n = 0 or 1): The source clock for IEP module can be selected through IEP Clock Multiplexer (see also *PRU_ICSSG Integration*). The default functional source clock for IEP is MAIN_PLL3_HSDIV1_CLKOUT, derived from PLL3 HSDIV1. The IEP functional clock (ICSSGn_IEP_CLK) runs at 200 or 250 MHz.
- ICSSGn_ICLK (where n = 0 or 1): The PRU_ICSSG interface clock is derived as divided version of the device PLLCTRL output clock (SYSCLK0/2).

Switching from ICSSGn_IEP_CLK to ICSSGn_ICLK is done by writing 1h to the ICSSG_IEPCLK_REG[0] IEP_OCP_CLK_EN bit. This is a one time configuration step before enabling the IEP function. Switching back from ICSSGn_ICLK to ICSSGn_IEP_CLK is only supported through a hardware reset of the PRU_ICSSG.

CAUTION

When software enables the clock (at PRU_ICSSG level) to the IEP module clock input via setting bit ICSSG_IEPCLK_REG[0] IEP_OCP_CLK_EN to 1h in the PRUSS_CFG space, there must be NO in-flight transactions to the IEP block.

CAUTION

Switching from ICSSGn_IEP_CLK (the IEP specific functional clock source) to the ICSSGn_CORE_CLK source is supported ONLY in software. Switching back from ICSSGn_CORE_CLK to ICSSGn_IEP_CLK is ONLY supported via assertion of a hardware reset to the PRU_ICSSG.

6.4.13.2.2 PRU_ICSSG IEP Timer

The IEP timer is a simple 64-bit timer. This timer is intended for use by industrial ethernet functions but can also be leveraged as a generic timer in other applications.

6.4.13.2.2.1 PRU_ICSSG IEP Timer Features

The IEP timer supports the following features:

- One controller 64-bit count-up counter with an overflow status bit.
  - Runs on ICSSG_IEP_CLK or ICSSG_ICLK clock.
  - Write 1h to clear status.
  - Supports a programmable increment value from 1 to 16 (default 5).
  - An optional compensation method allows the increment value to apply compensation increment value from 1 to 16 count up to 2^{24} ICSSG_IEP_CLK events with additional slow compensation mode.
- 10× 64-bit capture registers:
  - 8 capture inputs, with optional synchronous or asynchronous mode:
    - 6× rise capture registers: ICSSG_IEP_CAPRi_REG0/ IEP_CAPRi_REG1 (where i=0 to 5)
    - 2× rise and fall capture registers: IEP_CAPR6_REG0/ IEP_CAPR6_REG1 and IEP_CAPR7_REG0/ IEP_CAPR7_REG1, each combined with a fall capture - IEP_CAPF6_REG0/ IEP_CAPF6_REG1 and IEP_CAPF7_REG0/ IEP_CAPF7_REG1, respectively
    - One global event (any capture event) output for interrupt
- 16× 64-bit compare registers: IEP_CMPj_REG0/ IEP_CMPj_REG1 (where j = 0 to 15) and IEP_CMP_STATUS_REG[15-0] CMP_STATUS
  - 16 status bits, write 1h to clear
  - 16 individual event outputs
  - One global event output for interrupt generation triggered by any compare event
- 32 outputs, one high-level and one high-pulse for each compare hit event
- IEP_CMP_CFG_REG[0] CMP0_RST_CNT_EN, if enabled, will reset the controller counter on the next ICSSG_IEP_CLK/ ICSSG_ICLK cycle
- EHRPWM0_SYNCO/ EHRPWM3_SYNCO, if enabled, will reset the controller counter on the next ICSSG_IEP_CLK/ ICSSG_ICLK cycle
- Controller counter reset-state is programmable
- Optional 32-bit shadow mode of operation, which can be configured through IEP_CMP_CFG_REG[17] SHADOW_EN bit
- Self-clear CMP_STATUS_REG if ICSSG_SA_MX_REG[16] PWM_EFC_EN is set

6.4.13.2.3 32-Bit Shadow Mode

The IEP module can be configured in 32-bit shadow mode when IEP_CMP_CFG_REG[17] SHADOW_EN bit is set to 1h (default value is 0h, e.g. 64-bit mode of operation is enabled). In this mode, the controller counter will be in 32-bit mode of operation. This enables the shadow copy functionality of the compare registers.

Rules of operation:

1. Switching the state of the controller counter from 32-bit Shadow mode to 64-bit mode of operation, the counter should be disabled and bit IEP_CMP_CFG_REG[17] SHADOW_EN should be cleared to 0h (default value).
2. A new compare update (IEP_CMP_CFG_REG[16-1] CMP_EN = 1h - enables CMP[0:15] event, where [0]CMP_EN maps to CMP0) should be set 4 cycle counts before the next rollover or reset of the counter and to insure the correct shadow copy to active update is correct.

Sequence of operation:

1. Disable counter trough IEP_GLOBAL_CFG_REG[0] CNT_ENABLE = 0h (default value).
2. Clear controller counter through IEP_CMP_CFG_REG[17] SHADOW_EN = 0h (64-bit mode of operation)
3. Enable 32-bit Shadow mode through IEP_CMP_CFG_REG[17] SHADOW_EN bit (value: 1h)
4. Program IEP_CMPm_REGn (where m = 0 to 15 and n = 0 to 1); use the upper 32-bits (IEP_CMP0_REG1[31-0] CMP0_1) of the 64-bit CMP
   a. The lower 32-bits are the active compare value (IEP_CMPm_REG0[31-0] CMPm_0, where m = 0 to 15), software can only read this bits
   b. The upper 32-bits are the shadow copy (IEP_CMPm_REG1[31-0] CMPm_1, where m = 0 to 15), software can write and read this bits
5. Enable counter trough IEP_GLOBAL_CFG_REG[0] CNT_ENABLE = 1h

After the counter is enabled, then software can load a new set of CMP[0:15] without affecting the current active values of (IEP_CMPm_REG0[31-0] CMPm_0, where m = 0 to 15). Only when the counter is reset to 32-bit Shadow mode (IEP_CMP_CFG_REG[17] SHADOW_EN = 1h), it will load the shadow copy of IEP_CMPm_REG1[31-0] CMPm_1 into local copy.

Shadow compare value (IEP_CMPm_REG1[31-0] CMPm_1) is loaded into active register IEP_CMPm_REG0[31-0] CMPm_0 when the controller counter is configured in 32-bit Shadow mode. If IEP_CMP_CFG_REG[0] CMP0_RST_CNT_EN bit is enabled (value 1h) to reset the counter, the next reset event will be defined by the last CMP0 update.

6.4.13.2.4 PRU_ICSSG IEP Timer Basic Programming Sequence

Follow these basic steps to configure the IEP Timer.

Counter maintains/function:

1. Once enabled, the counter will count every ICSSG_IEP_CLK cycle, default rate of 200 MHz.
2. It is a free running counter with a sticky over flag status bit.
3. The counter over flow flag (IEP_GLOBAL_STATUS_REG[0] CNT_OVF) will get set when the counter switches/rollsover from 0xFFFF_FFFF to 0x0000_0000.
4. The counter will continue to count up. The software will need to read/clear the counter over flow flag and increment the MSB in software variable.

Compare function:

1. Initialize timer to known state (default values)
   - Disable counter (IEP_GLOBAL_CFG_REG[0] CNT_ENABLE = 0)
   - Reset Count Register (IEP_COUNT_REG0, IEP_COUNT_REG1) by writing FFFFFFFFh to clear
   - Clear overflow status register (IEP_GLOBAL_STATUS_REG[0] CNT_OVF = 1)
   - Clear compare status (IEP_CMP_STATUS_REG[15-0] CMP_STATUS) by writing FFFFFFFFh to clear
2. Set compare values IEP_CMPj_REG0, IEP_CMPj_REG1 (where j = 0 to 15)
3. Enable compare events (IEP_CMP_CFG_REG[16-1] CMP_EN = 1)
4. Set increment value (IEP_GLOBAL_CFG_REG[7-4] DEFAULT_INC)
5. Set compensation value (IEP_COMPEN_REG[22-0] COMPEN_CNT)
6. Enable counter (IEP_GLOBAL_CFG_REG[0] CNT_ENABLE = 1)

Capture function:

1. Update/Enable the counter if required
2. Program the enable the desired capture event
3. Wait for global capture event
4. Read/Clear the capture status to determine which capture event occurred
5. Read the capture count

6.4.13.2.5 Industrial Ethernet Mapping

Some of the capture inputs and compare registers are mapped to specific industrial Ethernet functions in hardware, shown in Table 6-154. All capture inputs are mapped to industrial Ethernet functions, and these inputs are not available for any other application. The CMP1 and CMP2 compare registers also function as the start time triggers for SYNC0 and SYNC1, respectively.

Table 6-155. IEP Timer Mode Mapping

Capture Input	IEP Line/Function
IEP_CAPR0_REG0/ IEP_CAPR0_REG1, rise only	If EXT_CAP_EN[0] = 0h (Internal source is selected)/ PRU0_RX_SOF If EXT_CAP_EN[0] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ0(1) ICSSG_n_IEP1_CAP_INTR_REQ0
IEP_CAPR1_REG0/ IEP_CAPR1_REG1, rise only	If EXT_CAP_EN[1] = 0h (Internal source is selected)/ PRU0_RX_SFD If EXT_CAP_EN[1] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ1 ICSSG_n_IEP1_CAP_INTR_REQ1
IEP_CAPR2_REG0/ IEP_CAPR2_REG1, rise only	If EXT_CAP_EN[2] = 0h (Internal source is selected)/ PRU1_RX_SOF If EXT_CAP_EN[2] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ2 ICSSG_n_IEP1_CAP_INTR_REQ2
IEP_CAPR3_REG0/ IEP_CAPR3_REG1, rise only	If EXT_CAP_EN[3] = 0h (Internal source is selected)/ PRU1_RX_SFD If EXT_CAP_EN[3] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ3 ICSSG_n_IEP1_CAP_INTR_REQ3
IEP_CAPR4_REG0/ IEP_CAPR4_REG1, rise only	If EXT_CAP_EN[4] = 0h (Internal source is selected)/ PORT0_TX_SOF; For MII mode uses loopback for lower jitter 40ns versus 4ns. If EXT_CAP_EN[4] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ4 ICSSG_n_IEP1_CAP_INTR_REQ4
IEP_CAPR5_REG0/ IEP_CAPR5_REG1, rise only	If EXT_CAP_EN[5] = 0h (Internal source is selected)/ PORT1_TX_SOF For MII mode uses loopback for lower jitter 40ns versus 4ns. If EXT_CAP_EN[5] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ5 ICSSG_n_IEP1_CAP_INTR_REQ5
IEP_CAPR6_REG0/ IEP_CAPR6_REG1 - rise and IEP_CAPF6_REG0/ IEP_CAPF6_REG1 - fall	PRGn_IEP0_EDC_LATCH_IN0 (IO inputs at SoC level) PRGn_IEP1_EDC_LATCH_IN0
IEP_CAPR7_REG0/ IEP_CAPR7_REG1 - rise and IEP_CAPF7_REG0/ IEP_CAPF7_REG1 - fall	PRGn_IEP0_EDC_LATCH_IN1 (IO inputs at SoC level) PRGn_IEP1_EDC_LATCH_IN1
IEP_CMP1_REG0/ IEP_CMP1_REG1	For SYNC0 trigger of start time
IEP_CMP2_REG0/ IEP_CMP2_REG1	For SYNC1 trigger of start time; only valid in the SYNC2 independent mode
IEP_CMP3_REG0/ IEP_CMP3_REG1	For MII TX0 start trigger, if MII register MII_RT_TXCFG0/1[2] TX_EN_MODEn is enabled (where n = 0 or 1). Note: MII_CFG defines which IEP is the source (IEP0 or IEP1).

Table 6-155. IEP Timer Mode Mapping (continued)

Capture Input	IEP Line/Function
IEP_CMP4_REG0/ IEP_CMP4_REG1	For MII TX1 start trigger, if MII register MII_RT_TXCFG0/1[2] TX_EN_MODEn is enabled (where n = 0 or 1). Note: MII_CFG defines which IEP is the source (IEP0 or IEP1).

(1) n = 0 to 1

6.4.13.2.6 PRU_ICSSG IEP Sync0/Sync1 Module

The industrial ethernet sync block supports the generation of two synchronization signals: SYNC0 and SYNC1. SYNC0 and SYNC1 can be directly mapped to output signals (pr<k>_iep<n>_edc_sync_out0 and pr<k>_iep<n>_edc_sync_out1) for external devices to use. They can also be used for internal synchronization within the PRU_ICSSG. These signals are also mapped as system events and can therefore be mapped to the Arm core's Host interrupts.

6.4.13.2.6.1 PRU_ICSSG IEP Sync0/Sync1 Features

The industrial ethernet sync block supports the following features:

- Two synchronize generation signals (SYNC0, SYNC1) with optional inversion
  - Activation time synchronized with IEP Timer
- IEP_CMP1_REG0/ IEP_CMP1_REG1 triggers SYNC0 activation time
- IEP_CMP2_REG0/ IEP_CMP2_REG1 triggers SYNC1 activation time (only valid in the SYNC2 independent mode)
  - Pulse width defined by registers or acknowledge mode (remain asserted until software acknowledged)
  - Cyclic or single-shot operation
  - Option to enable or disable sync generation
- Programmable number of clock cycles between the start of SYNC0 to the start of SYNC1

6.4.13.2.6.2 PRU_ICSSG IEP Sync0/Sync1 Generation Modes

There are four modes of operation for the sync signals: cyclic mode, single shot mode, cyclic with acknowledge mode, and single shot with acknowledge mode. Figure 6-106 shows examples of these modes. The start time is set by the IEP_SYNC_START_REG[31-0] SYNC_START bit field. The cycle time is configured by the IEP_SYNC0_PERIOD_REG[31-0] SYNC0_PERIOD bit field. The pulse length is defined by IEP_SYNC_PWIDTH_REG[31-0] SYNC_HPW bit field.

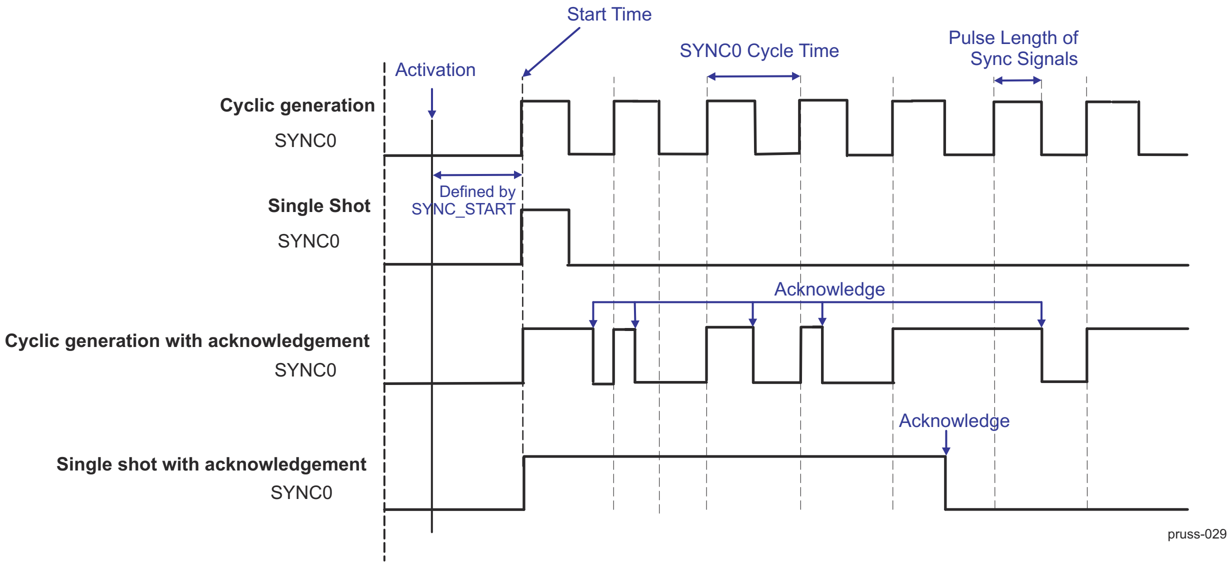

Figure 6-106. PRU_ICSSG IEP SYNC0 Signal Generation Modes

In SYNC1 dependent mode (IEP_SYNC_CTRL_REG[8] SYNC1_IND_EN = 0h), SYNC1 depends on SYNC0 and the start time of the SYNC1 can be defined by the IEP_SYNC1_DELAY_REG register. Figure 6-107 shows different examples when changing the value in the IEP_SYNC1_DELAY_REG register. Note: If the SYNC1 delay time is 0, SYNC1 reflects SYNC0. Cyclic generation cannot be used for network time synchronized applications because only the CMP1/CMP2 hit occurs in the compensated time domain.

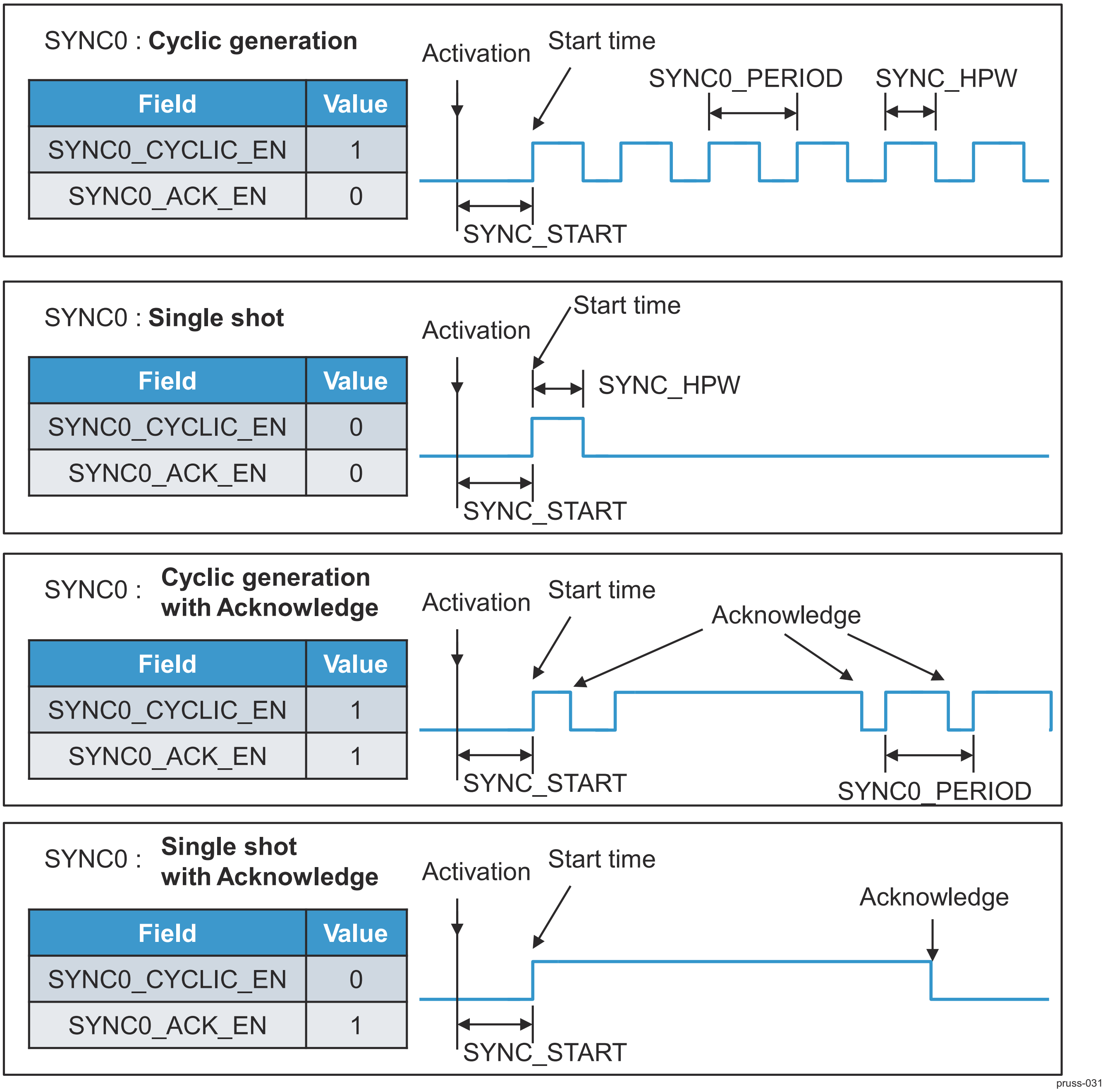

SYNC0 : **Cyclic generation**

Field	Value
SYNC0_CYCLIC_EN	1
SYNC0_ACK_EN	0

SYNC0 : **Single shot**

Field	Value
SYNC0_CYCLIC_EN	0
SYNC0_ACK_EN	0

SYNC0 : **Cyclic generation with Acknowledge**

Field	Value
SYNC0_CYCLIC_EN	1
SYNC0_ACK_EN	1

SYNC0 : **Single shot with Acknowledge**

Field	Value
SYNC0_CYCLIC_EN	0
SYNC0_ACK_EN	1

Figure 6-107. Examples of the Dependent Mode of SYNC1

6.4.13.2.7 PRU_ICSSG IEP WatchDog

In industrial ethernet applications, the watchdog timer (WD) is used to monitor process data communication and to turn off the outputs of the digital input/output (DIGIO) functional block after a set time. The WD will thereby protect the system from errors or faults by timeout or expiration. The expiration is used to initiate corrective action in order to keep the system in a safe state and restore normal operation based on configuration. Therefore, if the system is stable, the watchdog timer should be regularly reset or cleared to avoid timeout or expiration.

The IEP watchdog timer supports the following features:

- One 16-bit pre-divider for generating a WD clock (default 100µs) based on ICSSGn_IEP_CLK input
- Two 16-bit Watchdog Timers:
  - PDI_WD for Sync Managers WD, used in conjunction with digital input/output (DIGIO)
  - PD_WD for data link layer user WD, used in conjunction with data link layer or application layer interface actions

Note

For more details on the PRU_ICSSG Industrial Ethernet Watchdog timer, refer also to the Watchdog timer register descriptions covered in the *PRU_ICSSG IEP0 Registers* and *PRU_ICSSG IEP1 Registers*.

6.4.13.2.8 PRU_ICSSG IEP DIGIO

The IEP digital I/O (DIGIO) block provides dedicated I/Os for industrial ethernet protocols. The digital inputs can be sampled when specific events occur or continuously as a raw input. Likewise, driving the digital outputs can be triggered by specific events or controlled by software. The timing, delay cycle clocks, data sources, and data valid of the digital input and outputs are controlled by the IEP_DIGIO_CTRL_REG and IEP_DIGIO_EXP_REG registers. Additionally, the IEP DIGIO block can be used as generic I/Os in other applications.

6.4.13.2.8.1 PRU_ICSSG IEP DIGIO Features

The IEP digital I/O supports the following features:

- Digital data output:
  - 4 channels (PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28])
  - Five event options for driving output data output:
    - End of frame event (PRU0/1_RX_EOF)
    - SYNC0 events
    - SYNC1 events
    - Watchdog trigger
    - Software enable
- Digital data out enable (optional tri-state control)
- Digital data input:
  - 4 channels (PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28])
  - IEP_DIGIO_DATA_IN_RAW_REG supports direct sampling of PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28]
  - IEP_DIGIO_DATA_IN_REG supports four event options to trigger sampling of PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28]:
    - Start of frame event in start of frame (SOF) mode
    - pr<k>_iep<n>_edc_latch_in<0/1> event
    - SYNC0 events: pr<k>_iep<n>_edc_sync_out0
    - SYNC1 events: pr<k>_iep<n>_edc_sync_out1

6.4.13.2.8.2

The industrial digital I/Os supported by the PRU_ICSSG IEP peripheral are described in theTable 6-155:

Table 6-156. PRU_ICSSG IEP Digital IOs

Direction	Port	Mapped to Device I/Os	Notes
output	PRG<k>_IEP0_EDIO_DATA_IN_OUT[0:31]	PRG0_IEP0_EDIO_DATA_IN_OUT[31:28] PRG1_IEP0_EDIO_DATA_IN_OUT[31:28]	Only PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] are exported to device pins as a bidirectional.
output	PRG<k>_EDIO_DATA_OUT_EN[0:31]	No	Optional tri-state control for DATA_OUT
output	PRG<k>_IEP0_EDIO_OUTVALID	PRG0_IEP0_EDIO_OUTVALID PRG1_IEP0_EDIO_OUTVALID	Will pulse even same data
output	PRG<k>_EDIO_SOF	No	PRU<0/1>_RX_SOF defined by IEP_DIGIO_EXP_REG[12] SOF_SEL
input	PRG<k>_EDIO_OE_EXT	No	
output	PRG<k>_EDIO_WD_TRIG	No	Just export of IEP_WD_STATUS_REG[0] PD_WD_STAT
output	PRG<k>_EDIO_DATA_ENA	No	Reserved. Driven low.
input	PRG<k>_IEP<n>_EDC_LATCH_IN0	PRG0_IEP<n>_EDC_LATCH_IN0 PRG1_IEP<n>_EDC_LATCH_IN0	
input	PRG<k>_IEP<n>_EDC_LATCH_IN1	PRG0_IEP<n>_EDC_LATCH_IN1 PRG1_IEP<n>_EDC_LATCH_IN1	
output	PRG<k>_IEP<n>_EDC_SYNC_OUT0	PRG0_IEP<n>_EDC_SYNC_OUT0 PRG1_IEP<n>_EDC_SYNC_OUT0	
output	PRG<k>_IEP<n>_EDC_SYNC_OUT1	PRG0_IEP<n>_EDC_SYNC_OUT1 PRG1_IEP<n>_EDC_SYNC_OUT1	

6.4.13.2.8.3 PRU_ICSSG IEP DIGIO Block Diagrams

Figure 6-108 shows the signals and registers for capturing the DIGIO data in. Note that bit field [5-4]IN_MODE in the IEP_DIGIO_CTRL_REG register must be set to 1h for data to be latched on the external PRG<k>_IEP<n>_EDC_LATCH_IN0 signal. In PRU0/1_RX_SOF mode, the delay time of capturing PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] is programmable through the [11-8]SOF_DLY bit of the IEP_DIGIO_EXP_REG register.

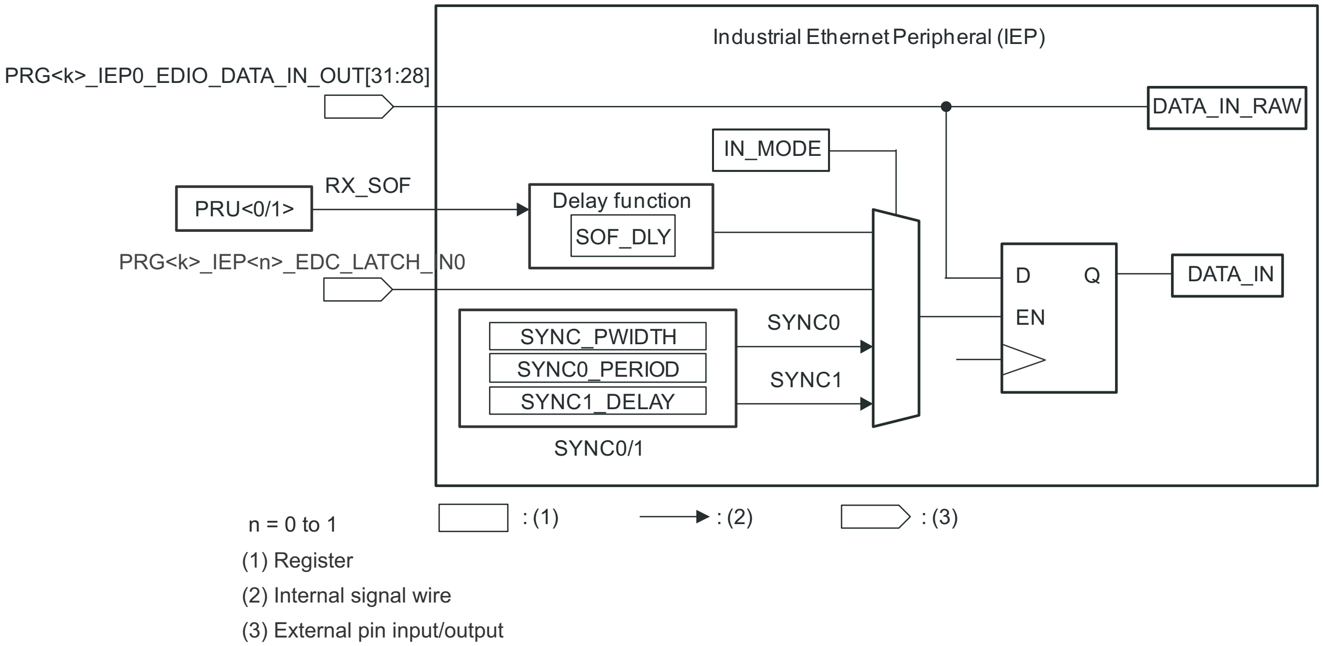

Figure 6-108. IEP DIGIO Data In

Figure 6-109 shows the signals and registers for driving the DIGIO data out.

The PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] is immediately forced to zero when IEP_DIGIO_CTRL_REG[1] OUTVALID_MODE = 1h, pr1_edio_oe_ext = 1h, and pd_wd_exp = 1h, or the next update hardware post pd_wd_exp. Delay assertion of PRG<k>_IEP0_EDIO_OUTVALID from PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] update events are controlled by software through IEP_DIGIO_EXP_REG[2] SW_OUTVALID.

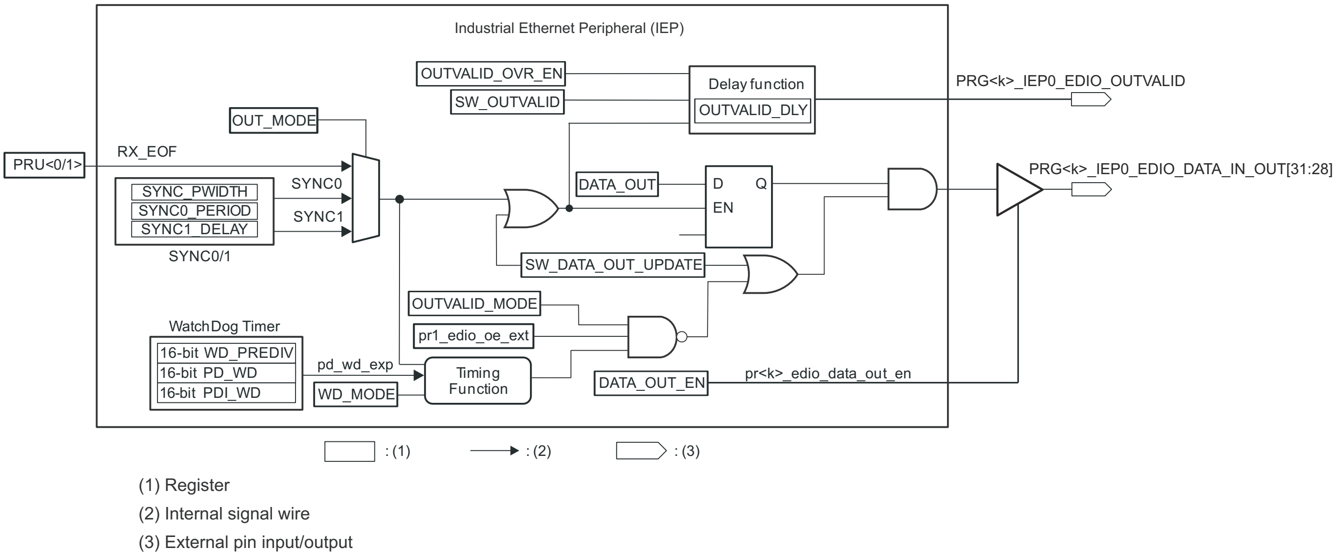

(1) Register
(2) Internal signal wire
(3) External pin input/output

Figure 6-109. IEP DIGIO Data Out

6.4.13.2.8.4 PRU_ICSSG IEP Basic Programming Model

Follow these steps to configure and read the DIGIO Data Input:

1. Read IEP_DIGIO_DATA_IN_RAW_REG for raw input data

or

1. Enable sampling of PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] by setting IEP_DIGIO_CTRL_REG[5-4] IN_MODE = 1h.
2. Read IEP_DIGIO_DATA_IN_REG for data sampled upon PRG<k>_IEP<n>_EDC_LATCH_IN0 posedge

Follow these steps to configure and write to the DIGIO Data Output:

1. Pre-configure DIGIO by setting IEP_DIGIO_EXP_REG[1] OUTVALID_OVR_EN and IEP_DIGIO_EXP_REG[0] SW_DATA_OUT_UP
2. Write to IEP_DIGIO_DATA_OUT_REG to configure output data.
3. To HiZ output, set corresponding IEP_DIGIO_DATA_OUT_EN_REG[31-0] DATA_OUT_EN bits to 1h (clear to 0h to drive value stored in IEP_DIGIO_DATA_OUT_REG).

Chapter 7

Interprocessor Communication (IPC)

This chapter describes the interprocessor communication (IPC) modules in the device.

7.1 Mailbox

This chapter describes the Mailbox module of the device.

7.1.1 Mailbox Overview

Mailbox module serves to facilitate the communication between the various on-chip processors of the device by providing a queued mailbox-interrupt mechanism.

The queued mailbox-interrupt mechanism allows the software to establish a communication channel between two processors (users) through a set of registers and associated interrupt signals.

The device implements the following:

- One system Mailbox module:
  - Number of clusters: 8
  - Used for communication between: Arm Cortex-A53 (A53SS), Arm Cortex-R5F (R5FSS), and Arm Cortex-M4F subsystems
  - Reference names: MAILBOX0

Table 7-1. Mailbox Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
MAILBOX0	-	✓

7.1.1.1 Mailbox Features

Each mailbox module supports the following features:

- Parameters configured at design time (see Table 7-2):
  - Number of mailbox clusters
    - Each mailbox cluster has the same configuration
    - Clusters are accessed via separate VBUS regions. Clusters can be treated as mailbox module instances.
  - Number of users
  - Number of mailbox message queues
  - Number of messages (FIFO depth) for each message queue
- 32-bit message width
- Partial writes do not advance the FIFO pointers
- Message reception and queue-not-full notification using interrupts
- Non-intrusive emulation

7.1.1.2 Mailbox Parameters

Table 7-2 shows the configuration of the mailbox module in the device.

Table 7-2. Mailbox Configuration Parameters

Module Instance	Parameters			
	Users (Processors)	Clusters(1)	Message Queues(2)	Number of Messages(3)
MAILBOX0	4	8	16	4

(1) Number of mailbox clusters
(2) Number of mailbox message queues (mailboxes per cluster)
(3) Number of messages (FIFO depth) for each message queue

7.1.1.3 Mailbox Not Supported Features

The following features are not supported by the module:

- Hardware protection to prevent users from reading FIFO mailboxes that it doesn't own as receiver or writing to FIFO mailboxes that it doesn't own as sender.

7.1.2 Mailbox Integration

This section describes the mailbox integration in the device, including information about clocks, resets, and hardware requests.

7.1.2.1 System Mailbox Integration

Figure 7-1 shows the MAILBOX integration in the MAIN domain. MAILBOX module contains a number of mailbox clusters. Each cluster generates one interrupt per user (processor).

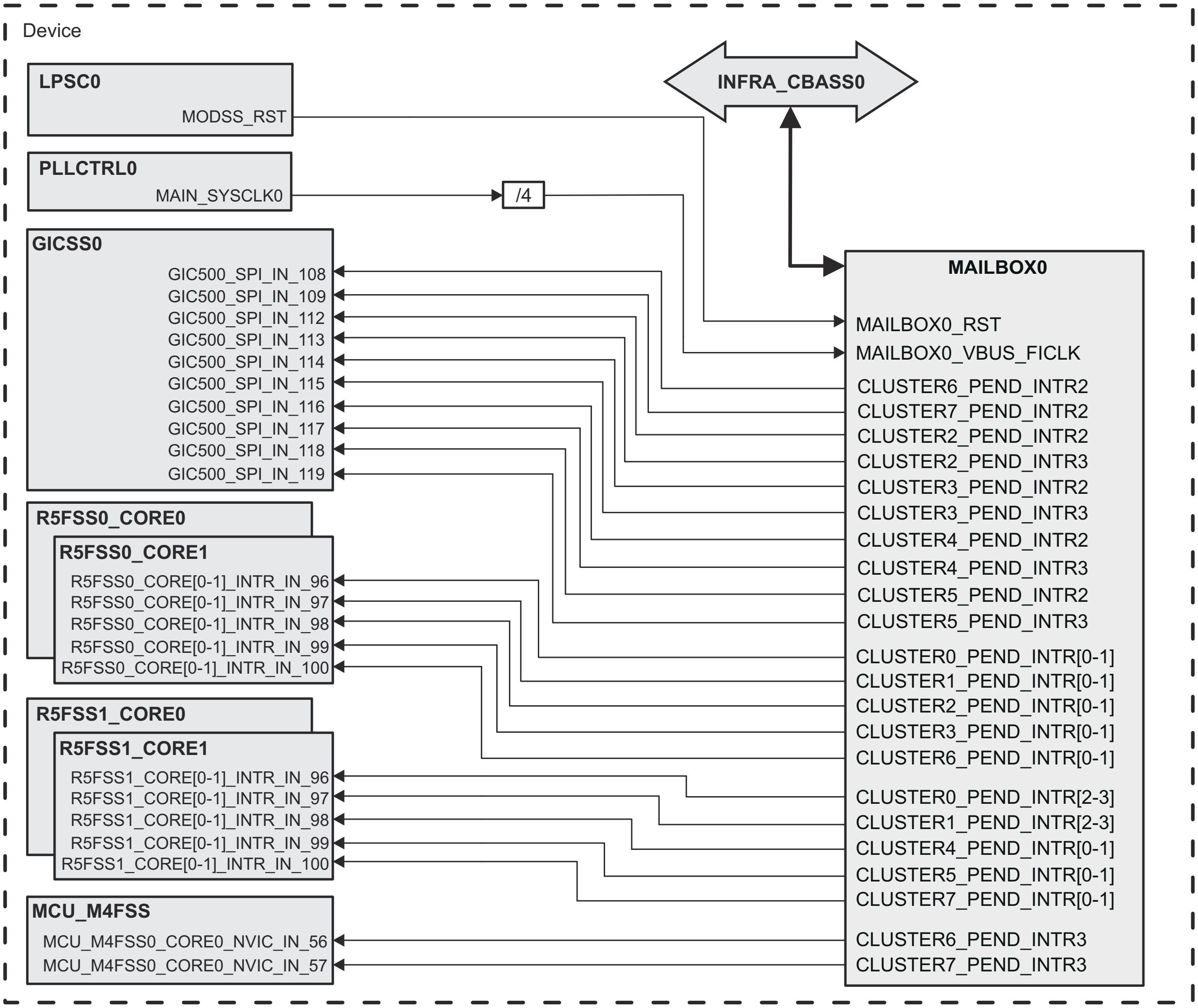

Figure 7-1. Mailbox Integration

Table 7-3 through Table 7-5 summarize the MAILBOX integration in the device.

Table 7-3. Mailbox Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MAILBOX0	PSC0	GP	LPSC0	INFRA_CBASS0

Table 7-4. Mailbox Clocks and Resets

Clocks

Table 7-4. Mailbox Clocks and Resets (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MAILBOX0	MAILBOX0_VBUS_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	MAILBOX0 clock. This clock is used for all interface and functional operations.
		Resets		
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
MAILBOX0	MAILBOX0_RST	MODSS_RST	LPSC0	MAILBOX0 hardware reset

Table 7-5. Mailbox Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
MAILBOX0	CLUSTER0_PEND_INTR3	R5FSS1_CORE1_INTR_IN_96	R5FSS1_CORE1	Cluster 0 user 3 interrupt request.	Level
	CLUSTER0_PEND_INTR2	R5FSS1_CORE0_INTR_IN_96	R5FSS1_CORE0	Cluster 0 user 2 interrupt request.	Level
	CLUSTER0_PEND_INTR1	R5FSS0_CORE1_INTR_IN_96	R5FSS0_CORE1	Cluster 0 user 1 interrupt request.	Level
	CLUSTER0_PEND_INTR0	R5FSS0_CORE0_INTR_IN_96	R5FSS0_CORE0	Cluster 0 user 0 interrupt request.	Level
	CLUSTER1_PEND_INTR3	R5FSS1_CORE1_INTR_IN_97	R5FSS1_CORE1	Cluster 1 user 3 interrupt request.	Level
	CLUSTER1_PEND_INTR2	R5FSS1_CORE0_INTR_IN_97	R5FSS1_CORE0	Cluster 1 user 2 interrupt request.	Level
	CLUSTER1_PEND_INTR1	R5FSS0_CORE1_INTR_IN_97	R5FSS0_CORE1	Cluster 1 user 1 interrupt request.	Level
	CLUSTER1_PEND_INTR0	R5FSS0_CORE0_INTR_IN_97	R5FSS0_CORE0	Cluster 1 user 0 interrupt request.	Level
	CLUSTER2_PEND_INTR3	GICSS0_SPI_IN_113	GICSS0	Cluster 2 user 3 interrupt request.	Level
	CLUSTER2_PEND_INTR2	GICSS0_SPI_IN_112	GICSS0	Cluster 2 user 2 interrupt request.	Level
	CLUSTER2_PEND_INTR1	R5FSS0_CORE1_INTR_IN_98	R5FSS0_CORE1	Cluster 2 user 1 interrupt request.	Level
	CLUSTER2_PEND_INTR0	R5FSS0_CORE0_INTR_IN_98	R5FSS0_CORE0	Cluster 2 user 0 interrupt request.	Level
	CLUSTER3_PEND_INTR3	GICSS0_SPI_IN_115	GICSS0	Cluster 3 user 3 interrupt request.	Level
	CLUSTER3_PEND_INTR2	GICSS0_SPI_IN_114	GICSS0	Cluster 3 user 2 interrupt request.	Level
	CLUSTER3_PEND_INTR1	R5FSS0_CORE1_INTR_IN_99	R5FSS0_CORE1	Cluster 3 user 1 interrupt request.	Level
	CLUSTER3_PEND_INTR0	R5FSS0_CORE0_INTR_IN_99	R5FSS0_CORE0	Cluster 3 user 0 interrupt request.	Level
	CLUSTER4_PEND_INTR3	GICSS0_SPI_IN_117	GICSS0	Cluster 4 user 3 interrupt request.	Level
	CLUSTER4_PEND_INTR2	GICSS0_SPI_IN_116	GICSS0	Cluster 4 user 2 interrupt request.	Level
	CLUSTER4_PEND_INTR1	R5FSS1_CORE1_INTR_IN_98	R5FSS0_CORE1	Cluster 4 user 1 interrupt request.	Level
	CLUSTER4_PEND_INTR0	R5FSS1_CORE0_INTR_IN_98	R5FSS0_CORE0	Cluster 4 user 0 interrupt request.	Level
	CLUSTER5_PEND_INTR3	GICSS0_SPI_IN_119	GICSS0	Cluster 5 user 3 interrupt request.	Level

Table 7-5. Mailbox Hardware Requests (continued)

	CLUSTER5_PEND_INTR2	GICSS0_SPI_IN_118	GICSS0	Cluster 5 user 2 interrupt request.	Level
	CLUSTER5_PEND_INTR1	R5FSS1_CORE1_INTR_IN_99	R5FSS0_CORE1	Cluster 5 user 1 interrupt request.	Level
	CLUSTER5_PEND_INTR0	R5FSS1_CORE0_INTR_IN_99	R5FSS0_CORE0	Cluster 5 user 3 interrupt request.	Level
	CLUSTER6_PEND_INTR3	MCU_M4FSS0_CORE0_NVIC_IN_56	MCU_M4FSS	Cluster 6 user 3 interrupt request.	Level
	CLUSTER6_PEND_INTR2	GICSS0_SPI_IN_108	GICSS0	Cluster 6 user 2 interrupt request.	Level
	CLUSTER6_PEND_INTR1	R5FSS0_CORE1_INTR_IN_100	R5FSS0_CORE1	Cluster 6 user 1 interrupt request.	Level
	CLUSTER6_PEND_INTR0	R5FSS0_CORE0_INTR_IN_100	R5FSS0_CORE0	Cluster 6 user 0 interrupt request.	Level
	CLUSTER7_PEND_INTR3	MCU_M4FSS0_CORE0_NVIC_IN_57	MCU_M4FSS	Cluster 7 user 3 interrupt request.	Level
	CLUSTER7_PEND_INTR2	GICSS0_SPI_IN_109	GICSS0	Cluster 7 user 2 interrupt request.	Level
	CLUSTER7_PEND_INTR1	R5FSS1_CORE1_INTR_IN_100	R5FSS0_CORE1	Cluster 7 user 1 interrupt request.	Level
	CLUSTER7_PEND_INTR0	R5FSS1_CORE0_INTR_IN_100	R5FSS0_CORE0	Cluster 7 user 0 interrupt request.	Level
DMA Events					
Module Instance	**Module DMA Event**	**Destination DMA Event Input**	**Destination**	**Description**	**Type**
MAILBOX0	-	-	-	No PDMA channels to external DMA engines	-

Note

For more information on the interconnects, see *System Interconnect*.

For more information on the power, reset, and clock management, see the corresponding sections within *Device Configuration*.

Note

For information about interrupt source description, see *Mailbox Interrupt Requests*.

7.1.3 Mailbox Functional Description

The mailbox module provides a means of communication through message queues among the users. The individual mailbox modules, or FIFOs, can associate (or de-associate) with any of the processors using the MAILBOX_IRQ_ENABLE_SET_j (or MAILBOX_IRQ_ENABLE_CLR_j) register.

Each user has a dedicated interrupt signal from the corresponding mailbox module instance and dedicated interrupt enabling and status registers.

Each MAILBOX_IRQ_STATUS_RAW_j/MAILBOX_IRQ_STATUS_CLR_j interrupt status register corresponds to a particular user.

7.1.3.1 Mailbox Block Diagram

Figure 7-2 shows the mailbox internal block diagram.

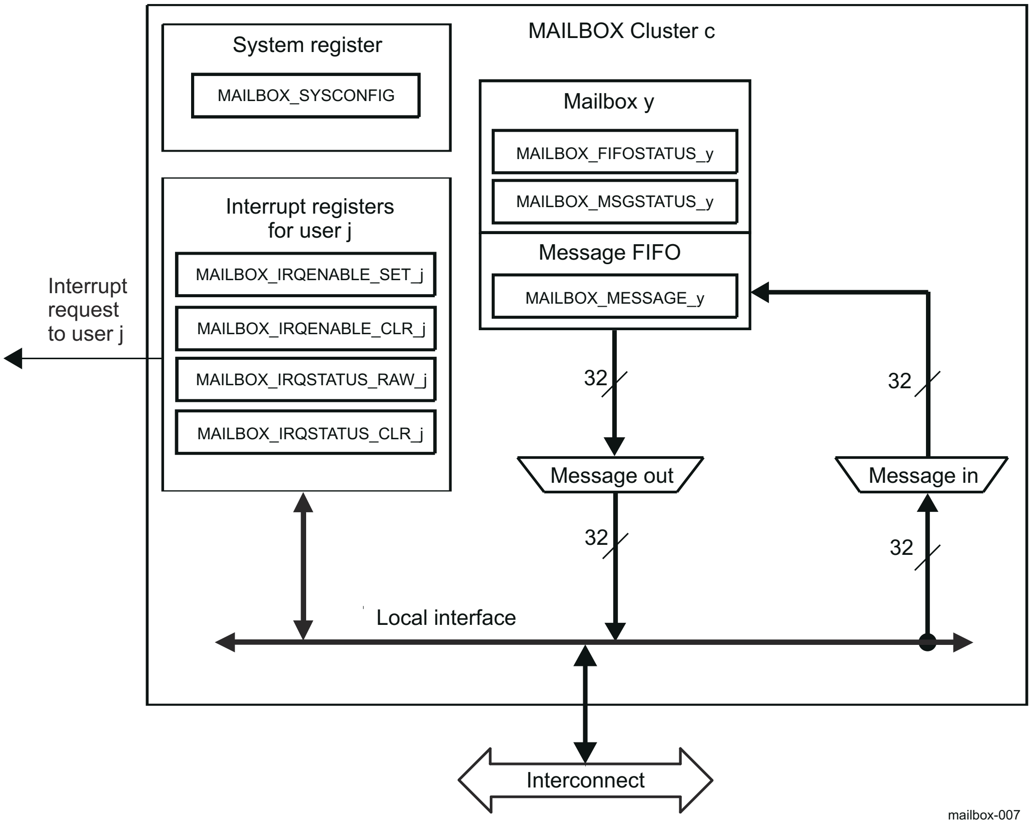

Figure 7-2. Mailbox Block Diagram

c = 0 to 11

j = 0 to 3

y = 0 to 15

7.1.3.2 Mailbox Software Reset

The mailbox module supports a software reset through the MAILBOX_SYSCONFIG[0] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. Reading the MAILBOX_SYSCONFIG[0] SOFTRESET bit gives the status of the software reset:

- Read 1: the software reset is on-going.
- Read 0: the software reset is complete.

The software must ensure that the software reset completes before doing mailbox operations.

7.1.3.3 Mailbox Power Management

The clkstop_idle will be asserted if all of the following are true:

- The VBUSP interface is inactive
- All mailboxes are empty
- There are no enabled events or outstanding interrupts

An enabled event means there is pending action required from one of the users, and it means one or more mailboxes still expect data.

7.1.3.4 Mailbox Interrupt Requests

An interrupt request allows the user of the mailbox to be notified when a message is received or when the message queue is not full. There is one interrupt per user.

Table 7-6 lists the event flags, and their mask, that can cause module interrupts.

Table 7-6. Interrupt Events

Non-Maskable Event Flag[1]	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
MAILBOX_IRQ_STATUS_RAW_j[0+y*2] NEWMSGSTATUSMBy	MAILBOX_IRQ_STATUS_CLR_j[0+y*2] NEWMSG_STATUSMBy	MAILBOX_IRQ_ENABLE_CLR_j[0+y*2] NEWMSG_STATUSMBy	MAILBOX_IRQ_ENABLE_SET_j[0+y*2] NEWMSG_STATUSMBy	Mailbox *y* receives a new message.
MAILBOX_IRQ_STATUS_RAW_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_STATUS_CLR_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_ENABLE_CLR_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_ENABLE_SET_j[1+y*2] NOTFULLSTATUSMBy	Mailbox *y* message queue is not full.

(1) MAILBOX_IRQ_STATUS_RAW_j register is mostly used for debug purposes.

> **CAUTION**
>
> Once an event generating the interrupt request has been processed by the software, it must be cleared by writing a logical 1 in the corresponding bit of the MAILBOX_IRQ_STATUS_CLR_j register.
>
> Writing a logical 1 in a bit of the MAILBOX_IRQ_STATUS_CLR_j register will also clear to 0 the corresponding bit in the appropriate MAILBOX_IRQ_STATUS_RAW_j register.

An event can generate an interrupt request when a logical 1 is written to the corresponding unmask bit in the MAILBOX_IRQ_ENABLE_SET_j register. Events are reported in the appropriate MAILBOX_IRQ_STATUS_CLR_j and MAILBOX_IRQ_STATUS_RAW_j registers.

An event stops generating interrupt requests when a logical 1 is written to the corresponding mask bit in the MAILBOX_IRQ_ENABLE_CLR_j register. Events are only reported in the appropriate MAILBOX_IRQ_STATUS_RAW_j register.

In case of the MAILBOX_IRQ_STATUS_RAW_j register, the event is reported in the corresponding bit even if the interrupt request generation is disabled for this event.

7.1.3.5 Mailbox Assignment

7.1.3.5.1 Description

To assign a receiver to a mailbox, set the new message interrupt enable bit corresponding to the desired mailbox in the MAILBOX_IRQ_ENABLE_SET_j register. The receiver reads the MAILBOX_MESSAGE_y register to retrieve a message from the mailbox.

An alternate method for the receiver that does not use the interrupts is to poll the MAILBOX_FIFO_STATUS_y and/or MAILBOX_MSG_STATUS_y registers to know when to send or retrieve a message to or from the mailbox. This method does not require assigning a receiver to a mailbox. Because this method does not include the explicit assignment of the mailbox, the software must avoid having multiple receivers use the same mailbox, which can result in incoherency.

To assign a sender to a mailbox, set the queue-not-full interrupt enable bit of the desired mailbox in the MAILBOX_IRQ_ENABLE_SET_j register, where *u* is the number of the sending user. However, direct allocation of a mailbox to a sender is not recommended because it can cause the sending processor to be constantly interrupted.

It is recommended that register polling be used to:

- Check the status of either the MAILBOX_FIFO_STATUS_y or MAILBOX_MSG_STATUS_y registers
- Write the message to the corresponding MAILBOX_MESSAGE_y register, if space is available.

The sender might use the queue-not-full interrupt when the initial mailbox status check indicates the mailbox is full. In this case, the sender can enable the queue-not-full interrupt for its mailbox in the appropriate MAILBOX_IRQ_ENABLE_SET_j register. This allows the sender to be notified by interrupt only when a FIFO queue has at least one available entry.

Reading the MAILBOX_IRQ_STATUS_CLR_j register determines the status of the new message and the queue-not-full interrupts for a particular user. Writing 1 to the corresponding bit in the MAILBOX_IRQ_STATUS_CLR_j register acknowledges, and subsequently clears, an interrupt.

CAUTION

Assigning multiple senders or multiple receivers to the same mailbox is not recommended.

7.1.3.6 Sending and Receiving Messages

7.1.3.6.1 Description

When a 32-bit message is written to the MAILBOX_MESSAGE_y register, the message is appended into the FIFO queue. This queue holds four messages. If the queue is full, the message is discarded.

Queue overflow can be avoided by first reading the MAILBOX_FIFO_STATUS_y register to check that the mailbox message queue is not full before writing a new message to it.

Reading the MAILBOX_MESSAGE_y register returns the message at the beginning of the FIFO queue and removes it from the queue. If the FIFO queue is empty when the MAILBOX_MESSAGE_y register is read, the value 0 is returned.

The new message interrupt is asserted when at least one message is in the mailbox message FIFO queue. To determine the number of messages in the mailbox message FIFO queue, read the MAILBOX_MSG_STATUS_y register.

7.1.3.7 Example of Communication

Figure 7-3 shows an example of communication between two processors.

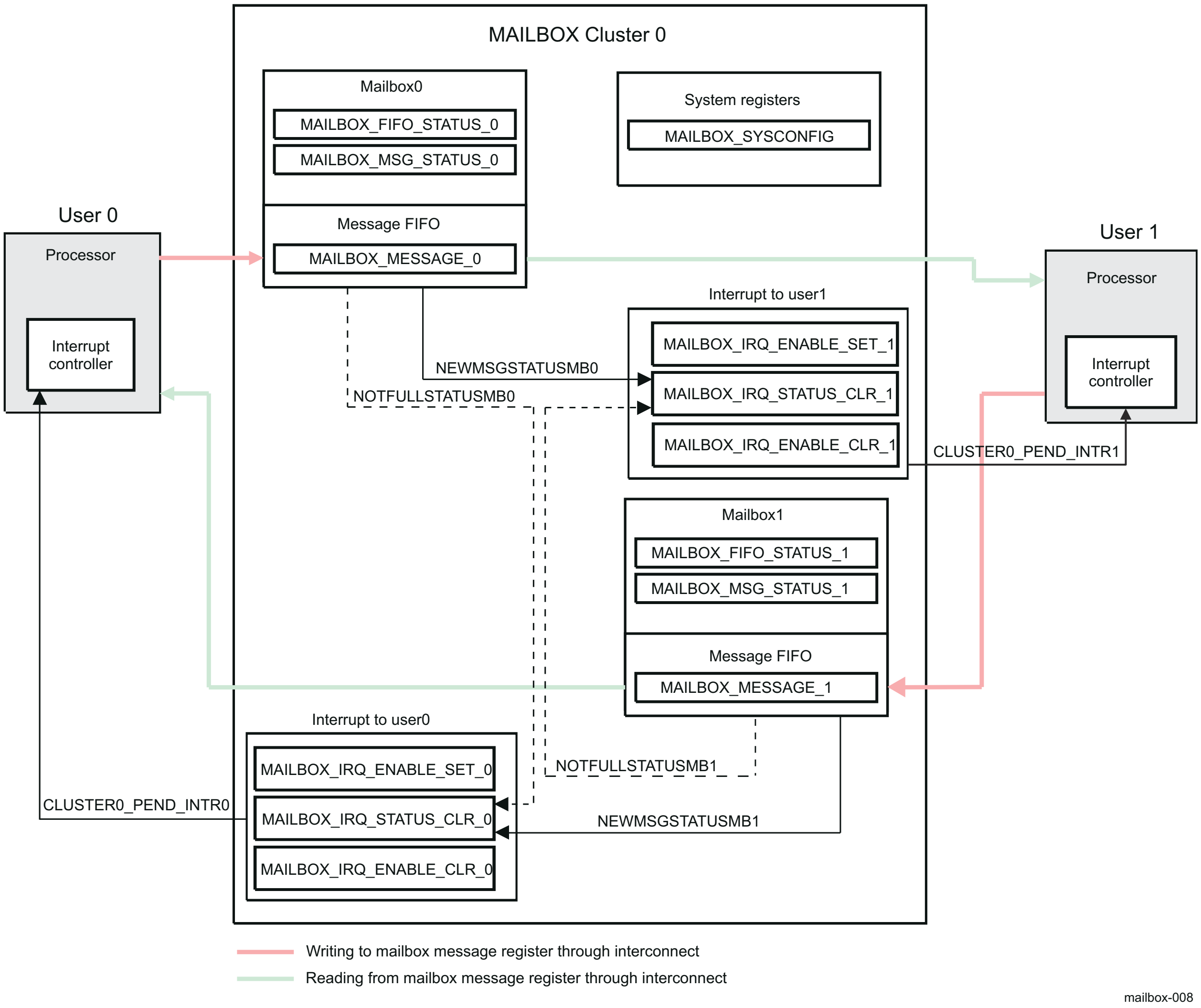

Figure 7-3. Example of Communication

7.1.4 Mailbox Programming Guide

7.1.4.1 Mailbox Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the mailbox module.

7.1.4.1.1 Global Initialization

7.1.4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the mailbox module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the mailbox.

See Section 7.1.2 , *Mailbox Integration*, for further information.

Table 7-7. Global Initialization of Surrounding Modules for MAILBOX

Surrounding Modules	Comments
LPSC	The MAILBOX functional and interface clock must be enabled.
Interrupt Controllers	Processor's (user's) interrupt controller must be configured to enable the interrupt request generation.
GICSS0	GICSS0 configuration must be done to allow module IRQs to be mapped to required INTC input. For more information see *Interrupt Routers*.
R5FSS0_CORE0/1	R5FSS0_CORE0/1 configuration must be done to allow module IRQs to be mapped to required INTC input. For more information see *Interrupt Routers*.
R5FSS1_CORE0/1	R5FSS1_CORE0/1 configuration must be done to allow module IRQs to be mapped to required INTC input. For more information see *Interrupt Routers*.
MCU_M4FSS	MCU_M4FSS configuration must be done to allow module IRQs to be mapped to required INTC input. For more information see *Interrupt Routers*.

7.1.4.1.1.2 Mailbox Global Initialization

7.1.4.1.1.2.1 Main Sequence - Mailbox Global Initialization

This procedure initializes the mailbox module after a power-on or software reset.

Table 7-8. Mailbox Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset	MAILBOX_SYSCONFIG[0] SOFT_RESET	0x1
Wait until reset is complete	MAILBOX_SYSCONFIG[0] SOFT_RESET	=0x0

7.1.4.1.2 Mailbox Operational Modes Configuration

7.1.4.1.2.1 Mailbox Processing modes

7.1.4.1.2.1.1 Main Sequence - Sending a Message (Polling Method)

Table 7-9. Sending a Message (Polling Method)

Step	Register/Bit Field/Programming Model	Value
IF: Is FIFO full?	MAILBOX_FIFO_STATUS_y[0] FULL	=0x1
Wait until at least one message slot is available	MAILBOX_FIFO_STATUS_y[0] FULL	=0x0
ELSE		
Write message	MAILBOX_MESSAGE_y[31:0] VALUE	0x-
ENDIF		

7.1.4.1.2.1.2 Main Sequence - Sending a Message (Interrupt Method)

Table 7-10. Sending a Message (Interrupt Method)

Step	Register/Bit Field/Programming Model	Value
IF: Is FIFO full?	MAILBOX_FIFO_STATUS_y[0] FULL	=0x1

Table 7-10. Sending a Message (Interrupt Method) (continued)

Step	Register/Bit Field/Programming Model	Value
Enable interrupt event	MAILBOX_IRQ_ENABLE_SET_j[1+ y*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 7.1.4.1.3.1 for interrupt handling in sending mode		
ELSE		
Write message	MAILBOX_MESSAGE_y[31:0] VALUE	0x-
ENDIF		

7.1.4.1.2.1.3 Main Sequence - Receiving a Message (Polling Method)

Table 7-11. Receiving a Message (Polling Method)

Step	Register/Bit Field/Programming Model	Value
IF: Number of messages is not equal to 0	MAILBOX_MSG_STATUS_y[2:0] NUM_MESSAGES	≠0x0
Read message	MAILBOX_MESSAGE_y[31:0] VALUE	0x-
ENDIF		

7.1.4.1.2.1.4 Main Sequence - Receiving a Message (Interrupt Method)

Table 7-12. Receiving a Message (Interrupt Method)

Step	Register/Bit Field/Programming Model	Value
Enable interrupt event	MAILBOX_IRQ_ENABLE_SET_j[0 + y*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 7.1.4.1.3.2 for interrupt handling in receiving mode		

7.1.4.1.3 Mailbox Events Servicing

7.1.4.1.3.1 Events Servicing in Sending Mode

Table 7-13 describes the events servicing in sending mode.

Table 7-13. Events Servicing in Sending Mode

Step	Register/Bit Field/Programming Model	Value
Read interrupt status bit	MAILBOX_IRQ_STATUS_CLR_j[1 + y*2]	0x1
Write message	MAILBOX_MESSAGE_y[31:0] VALUE	0x--
Write 1 to acknowledge interrupt	MAILBOX_IRQ_STATUS_CLR_j[1 + y*2]	0x1

7.1.4.1.3.2 Events Servicing in Receiving Mode

Table 7-14 describes the events servicing in receiving mode.

Table 7-14. Events Servicing in Receiving Mode

Step	Register/Bit Field/Programming Model	Value
Read interrupt status bit	MAILBOX_IRQ_STATUS_CLR_j[0 + y*2]	0x1
IF: Number of messages is not equal to 0?	MAILBOX_MSG_STATUS_y[2:0] NUM_MESSAGES	≠0x0
Read message	MAILBOX_MESSAGE_y[31:0] VALUE	0x--
ELSE		
Write 1 to acknowledge interrupt	MAILBOX_IRQ_STATUS_CLR_j[0 + y*2]	0x1
ENDIF		

7.2 Spinlock

This chapter describes the Spinlock module of the device.

7.2.1 Spinlock Overview

The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device.

The Spinlock module implements 256 spinlocks (or hardware semaphores), which provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need of a read-modify-write bus transfer that the programmable cores are not capable of.

Figure 7-4 shows an overview of the Spinlock module.

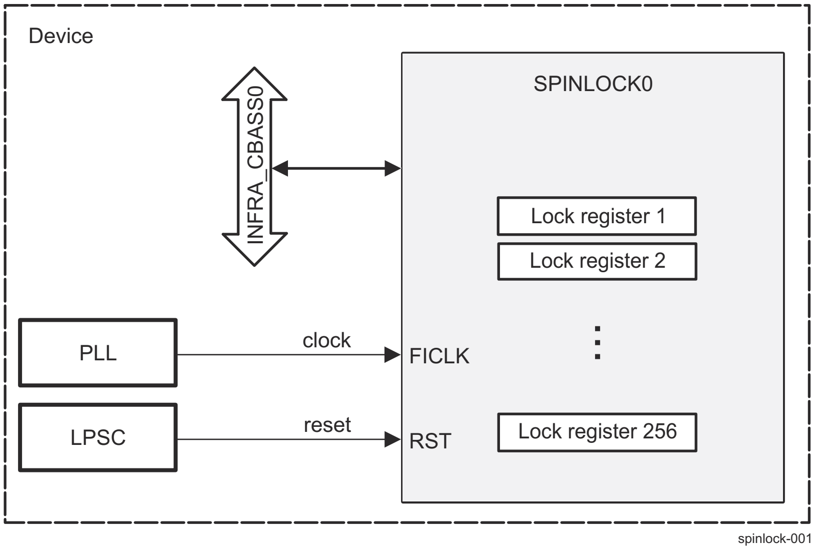

Figure 7-4. Spinlock Overview

Table 7-15. Spinlock Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
SPINLOCK0	-	✓

7.2.1.1 Spinlock Not Supported Features

The following features are not supported by the module:

- Ownership enforcement. There is no support to ensure that a lock register is locked and unlocked by the same process
- There is no support for checking that the same VBUS initiator that acquired the lock is the one that is freeing the lock
- There is no support for fairness or congestion control.

7.2.2 Spinlock Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 7-5 shows the Spinlock integration.

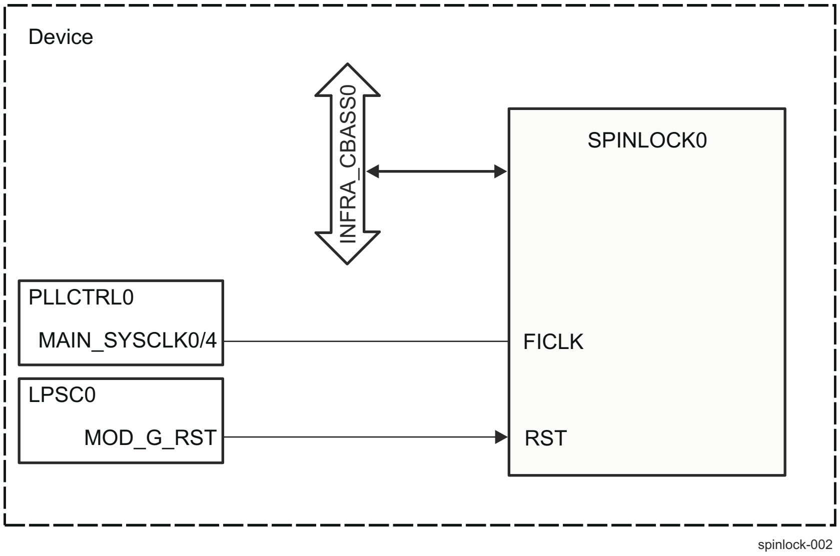

Figure 7-5. Spinlock Integration

Table 7-16 and Table 7-17 summarize the integration of the module in the device.

Table 7-16. Spinlock Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
SPINLOCK0	PSC0	GP	LPSC0	INFRA_CBASS0

Table 7-17. Spinlock Clocks and Resets

Clocks				
Module Instance	Module Clock Input	Source Clock Signal	Source	Description
SPINLOCK0	SPINLOCK0_VBUS_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	Spinlock clock. This clock is used for all interface and functional operations.
Resets				
Module Instance	Module Reset Input	Source Reset Signal	Source	Description
SPINLOCK0	SPINLOCK0_RST	MOD_G_RST	LPSC0	Spinlock hardware reset

Table 7-18. Spinlock Hardware Requests

Interrupt Requests					
Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
SPINLOCK0	-	-	-	No interrupts to external processors	-
DMA Events					
Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Description	Type
SPINLOCK0	-	-	-	No PDMA channels to external DMA engines	-

7.2.3 Spinlock Functional Description

7.2.3.1 Spinlock Software Reset

The Spinlock module can be reset by software through the SPINLOCK_SYSCONFIG[1] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. Note that reading back the value of SPINLOCK_SYSCONFIG[1] SOFTRESET bit will always return 0. The software must ensure that the software reset completes before doing Spinlock operations.

7.2.3.2 Spinlock Power Management

The Spinlock module supports the Power Idle interface. Software must arrange to only power off the Spinlock module when no locks would be lost. In general, the steps to powering down the Spinlock module are:

1. Software must check that all controllers that may be using the Spinlock module are either:
   a. Already powered off (all in-use flags are 0)
   b. Notified that Spinlock is not available and the notification is acknowledged
2. If desired, check that no locks are currently held in the Spinlock module. The status of each bank of 32 locks can be read from the SPINLOCK_SYSTATUS register. If any locks are held, they are orphaned because they are not held by any controller that is still active. Alternatively, you may decide to wait a timeout period to allow any active controller to clean up its locks before powering down.

The Spinlock module may now be powered off.

7.2.3.3 About Spinlocks

Spinlocks are present to solve the need for synchronization and mutual exclusion between heterogeneous processors and those not operating under a single, shared operating system. There is no alternative mechanism to accomplish these operations between processors in separate subsystems.

Spinlocks are not the best way to synchronize between tasks or threads on one CPU. Instead, spinlocks are for use in synchronization between different subsystems in the device that don't have any other means of hardware-based synchronization.

Spinlocks do not solve all system synchronization issues. They have limited applicability and should be used with care to implement higher level synchronization protocols.

A spinlock is appropriate for mutual exclusion for access to a shared data structure. It should be used only when:

1. The time to hold the lock is predictable and small (for example, a maximum hold time of less than 200 CPU cycles may be acceptable).
2. The locking task cannot be preempted, suspended, or interrupted while holding the lock (this would make the hold time large and unpredictable).
3. The lock is lightly contended, that is the chance of any other process (or processor) trying to acquire the lock while it is held is small.

If these conditions are met, then the locking code can retry a failed attempt to acquire the lock until success.

If the conditions are not met, then a spinlock is not a good candidate. One alternative is to use a spinlock for critical section control (engineered to meet the conditions) to implement a higher level semaphore that can support preemption, notification, timeout or other higher level properties.

7.2.3.4 Spinlock Functional Operation

The Spinlock module supports 256 spinlocks. It accepts only a single command at a time and processes the command fully before accepting the next command. A lock is requested by reading the SPINLOCK_LOCK_REG_i[0] TAKEN bit. There are two states: Taken (SPINLOCK_LOCK_REG_y[0] TAKEN = 1) or Not Taken (SPINLOCK_LOCK_REG_y[0] TAKEN = 0), where y = 0h to FFh.

When the status of lock *y* (where y = 0 to 255) is Not Taken (free), a read from the SPINLOCK_LOCK_REG_y register returns 0 and sets the lock to Taken (locked). When the status of lock *y* is Taken, a read returns 1 and does not change the state of the lock.

A write to the SPINLOCK_LOCK_REG_y register does not change the state of lock, unless when writing 0 when the lock is in Taken state. By doing this, the requester frees the lock.

Figure 7-6 shows the SPINLOCK_LOCK_REG_y register state diagram.

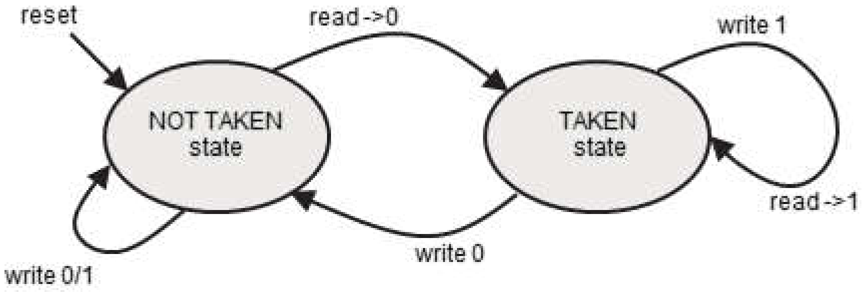

Figure 7-6. Lock Register State Diagram

Note

- There is no support to ensure that a lock register is locked and unlocked by the same process. This must be ensured in software.
- There is no support to check that the same initiator that acquired the lock is the one that is freeing the lock.

7.2.4 Spinlock Programming Guide

7.2.4.1 Spinlock Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

7.2.4.1.1 Surrounding Modules Global Initialization

This procedure initializes the surrounding modules when the Spinlock module is used for the first time after a device reset.

Table 7-19. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC	Spinlock functional and interface clock must be enabled. For more information, see *Clocking*

7.2.4.1.2 Basic Spinlock Operations

The main Spinlock operations are:

- Clear all the Taken spinlocks by writing 0 to SPINLOCK_LOCK_REG_y (only after a system bug recovery)
- Take a spinlock by reading the SPINLOCK_LOCK_REG_i[0] TAKEN bit
- Release spinlock by writing 0 to SPINLOCK_LOCK_REG_i[0] TAKEN bit

7.2.4.1.2.1 Spinlocks Clearing After a System Bug Recovery

Module initialization (after reset) is not needed, except after system bug recovery. The following table presents the Spinlock initialization after a system bug recovery. Software should store 0 into each of the SPINLOCK_LOCK_REG_y registers at system startup to insure that all locks are initialized to Not Taken.

Table 7-20. Spinlock System Bug Recovery

Step	Register	Value
IF: SPINLOCK_SYSTATUS[0] IU0 = 1?	SPINLOCK_SYSTATUS[0] IU0	=1
Free the 256 locks	SPINLOCK_LOCK_REG_y[0] TAKEN (y = 0 to 255)	0x0
END		

7.2.4.1.2.2 Take and Release Spinlock

This procedure configures the take and release (free) operations for the Spinlock module. A spinlock should only be held with interrupts disabled. So, before attempting to obtain the spinlock, software must disable interrupts. Then it must read the SPINLOCK_LOCK_REG_y[0] TAKEN bit to attempt to obtain the lock. If it succeeds, it must proceed directly through the critical section then unlock and re-enable interrupts. If the acquisition attempt fails, the acquisition must be reattempted. To prevent unknown interrupt disabled time, interrupts must be re-enabled and then disabled before reattempting to acquire the lock. Figure 7-7 shows the described above procedure.

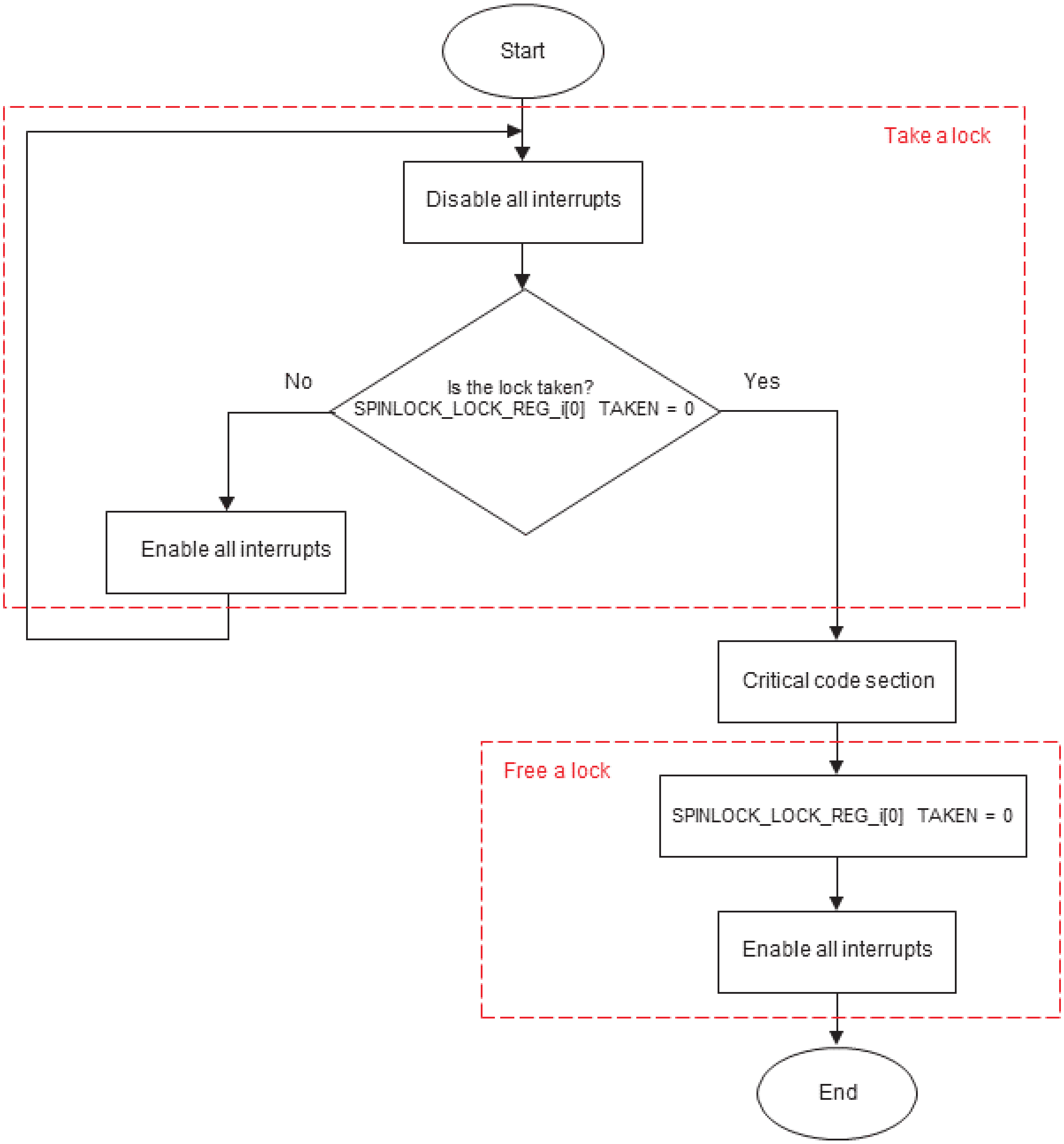

Figure 7-7. Take and Release Spinlock

Table 7-21. Register Call Summary

Register Name
SPINLOCK_LOCK_REG_y[0] TAKEN

Table 7-22. Subprocess Call Summary

Subprocess Name	Description
Disable (Mask) All Interrupts	For information about disabling/enabling all interrupts in an Arm® processor, refer to Arm *Technical Reference Manual*, available at infocenter.arm.com/help/index.jsp. For information about disabling/enabling all interrupts in other processors, refer to the corresponding processor chapter.
Enable (Unmask) All Interrupts	

Chapter 8

Memory Controllers

This chapter describes the memory controllers in the device.

8.1 DDR Subsystem (DDRSS)

This section describes the DDR Subsystem (DDRSS) for the device.

8.1.1 DDRSS Overview

The DDR subsystem in this device comprises DDR controller, DDR PHY and wrapper logic to integrate these blocks in the device. The DDR subsystem is referred to as DDRSS0 and is used to provide an interface to external SDRAM devices which can be utilized for storing program or data. DDRSS0 is accessed via MSMC, and not directly through the system interconnect.

Table 8-1 shows DDRSS allocation across device domains.

Table 8-1. DDRSS Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
DDRSS0	-	✓

Figure 8-1 shows an overview of the DDRSS0 and its surrounding modules.

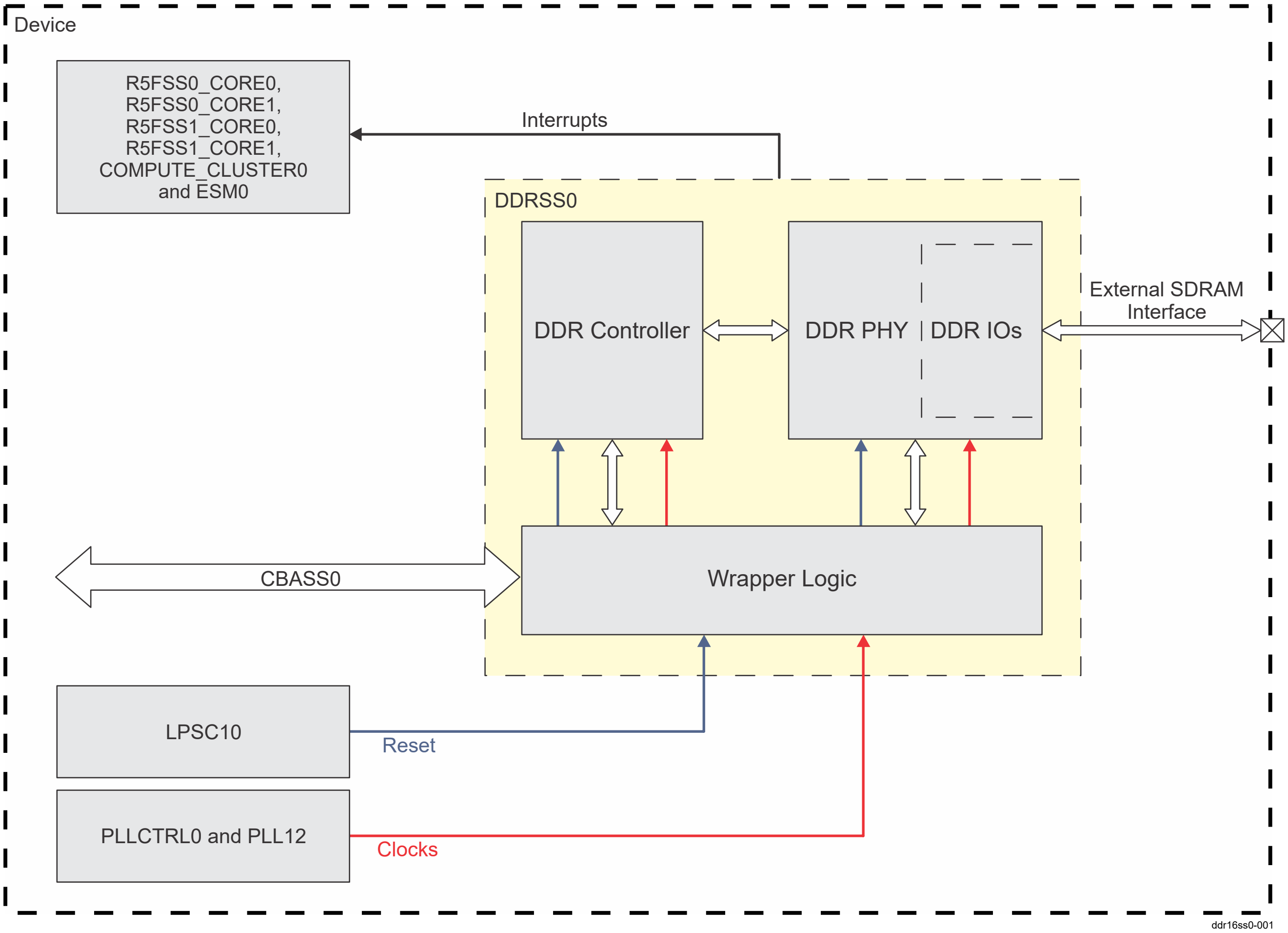

Figure 8-1. DDRSS Overview

The DDRSS0 supports:

- Memory Types:
  - DDR4 up to 1600Mbps
  - LPDDR4 up to 1600Mbps
- Memory Bus Features:

  - 16-bit width with in-line ECC
  - Up to 2 ranks
  - SDRAM address range up to 8 GB
- System Bus Interface:
  - 128-bit data width
  - Little endian only
  - Address aliasing prevention to block accesses to unpopulated SDRAM region
  - Clock asynchronous to DDR clock
- Configuration Bus Interface:
  - 32-bit data width
  - Linear incrementing addressing mode
  - 32-bit aligned accesses only
  - Little endian only
  - Clock asynchronous to DDR clock
- Key Features:
  - Full coherency across all commands
  - Bank interleaving
  - Priority based scheduling
  - Scheduling based on bank openness
  - Class of Service (CoS) - Three latency classes supported
  - Read/write scheduling to avoid turn-around time
  - Prioritized refresh scheduling
  - Dynamic change of refresh rate via software for extended temperatures
  - Statistical counters for performance management
- SDRAM ECC Features:
  - In-line ECC
  - 64-byte ECC calculated over 512-byte data
  - Read-modify-write ECC for sub-word writes
  - 32-byte ECC calculated over 256-byte data
  - Support ECC cache to improve in-line ECC performance
  - Support 64 cache-lines each 512-byte wide
  - ECC address error logging
  - Statistical counters for counting ECC errors
- Low Power Features:
  - Self-refresh entry and exit via software or hardware clock stop request
  - All power modes defined by JEDEC (clock stop for LPDDR4, self-refresh, power-down, etc.)
  - System bus clock stop via hardware clock stop request/acknowledge when controller is idle
  - Automatic idle power saving mode when no or low activity is detected
  - DDR and system bus clock frequency change using self-refresh via software or hardware clock stop request/acknowledge
  - Turning off SoC power after DDR is put into self-refresh (DDR reset and CKE I/O retention)
  - Tri-stating of all DDR I/O cells via software while driving CKE and RSTN pins during self-refresh
  - LPDDR4 Frequency Set Point (FSP)
- Functional Safety Features:
  - MSMC2DDR bridge AXI bus timeout
- DDR PHY Features:
  - Automatic and software controllable initialization and calibration (ZQ) for the DDR PHY and I/O cells
  - Automatic and software controllable delay line calibrations with Voltage and Temperature (VT) compensation
  - Automatic and software controllable write levelling with VT compensation
  - Automatic read DQS gate training per rank with VT compensation
  - Automatic and software controllable DQ/DQS eye training per rank

  - Automatic and software controllable read and write data bit deskew
  - Automatic and software controllable Command/Address (CA) levelling with VT compensation for LPDDR4
  - Automatic and software controllable CA bit deskew for LPDDR4
  - Refreshes to SDRAM during leveling and training
  - No seeding requirement based on board topology for any of the leveling and training algorithms
  - Dynamic/automatic I/O Receiver disable when read transfer is not on going
  - Capability of disabling data macros and I/O cells when not in use

8.1.1.1 DDRSS Not Supported Features

DDRSS0 does not support the following:

- DDR3 SDRAMs
- DDR3L SDRAMs
- DDR3U SDRAMs
- DIMM
- 1/2 width (8-bit) mode via software configuration
- Data bus obfuscation or any other kind of encryption
- Fail-safe reset I/O to maintain reset state during SoC power OFF
- Independent operation of dual 16-bit channels for LPDDR4
- The ECC engine of the DDR controller
- LPDDR4x SDRAMs
- Automatic periodic scrubbing of SDRAM for ECC
- Maximum of 17 row bits are supported for LPDDR4. LPDDR4 with 18 row bits are not supported
- Only 1 rank designs are supported
- Only address range of up to 2GBytes is supported
- LPDDR4 devices with byte mode die configurations
- 1T command timing (only 2T timing is supported)

8.1.2 DDRSS Environment

Please refer to the AM64x DDR Board Design and Layout Guidelines application note for detailed information on DDR interface connections to LPDDR4 and DDR4 memory devices

Table 8-2 describes the DDRSS0 I/O signals used for connection to SDRAM devices.

Table 8-2. DDRSS0 I/O signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
RESETN	DDR0_RESET0_n	O	SDRAM reset	0x0
CK	DDR0_CK0	O	SDRAM differential clock pair	0x0
CKN	DDR0_CK0_n	O		0x1
ALERTN	DDR0_ALERT_n	IO	SDRAM parity error output	HiZ
A[13-0]	DDR0_A[13-0]	O	SDRAM address and command bus	HiZ
WEN	DDR0_WE_n	O	SDRAM write enable	0x0
CASN	DDR0_CAS_n	O	SDRAM column address strobe	0x0
RASN	DDR0_RAS_n	O	SDRAM row address strobe	0x0
ACTN	DDR0_ACT_n	O	SDRAM activate	0x0
BA[1-0]	DDR0_BA[1-0]	O	SDRAM bank address	0x0
BG[1-0]	DDR0_BG[1-0]	O	SDRAM bank group	0x0
PAR	DDR0_PAR	O	SDRAM command parity	0x0
CSN[1-0]	DDR0_CS[1-0]_n	O	SDRAM chip select	0x0
ODT[1-0]	DDR0_ODT[1-0]	O	SDRAM on-die termination	0x0
CKE[1-0]	DDR0_CKE[1-0]	O	SDRAM CKE	0x0
DQ[15-0]	DDR0_DQ[15-0]	IO	SDRAM data bus	HiZ
DM[1-0]	DDR0_DM[1-0]	IO	SDRAM data and mask/DBI	HiZ
DQS[1-0]	DDR0_DQS[1-0]	IO	SDRAM data strobe	HiZ
DQSN[1-0]	DDR0_DQS[1-0]_n	IO	SDRAM data strobe invert	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

8.1.3 DDRSS Integration

This section describes DDRSS0 integration in the device, including information about clocks, resets, and hardware requests.

8.1.3.1 DDRSS Integration in MAIN Domain

A single DDRSS0 module is integrated in the device MAIN domain. Figure 8-2 shows the integration of DDRSS0.

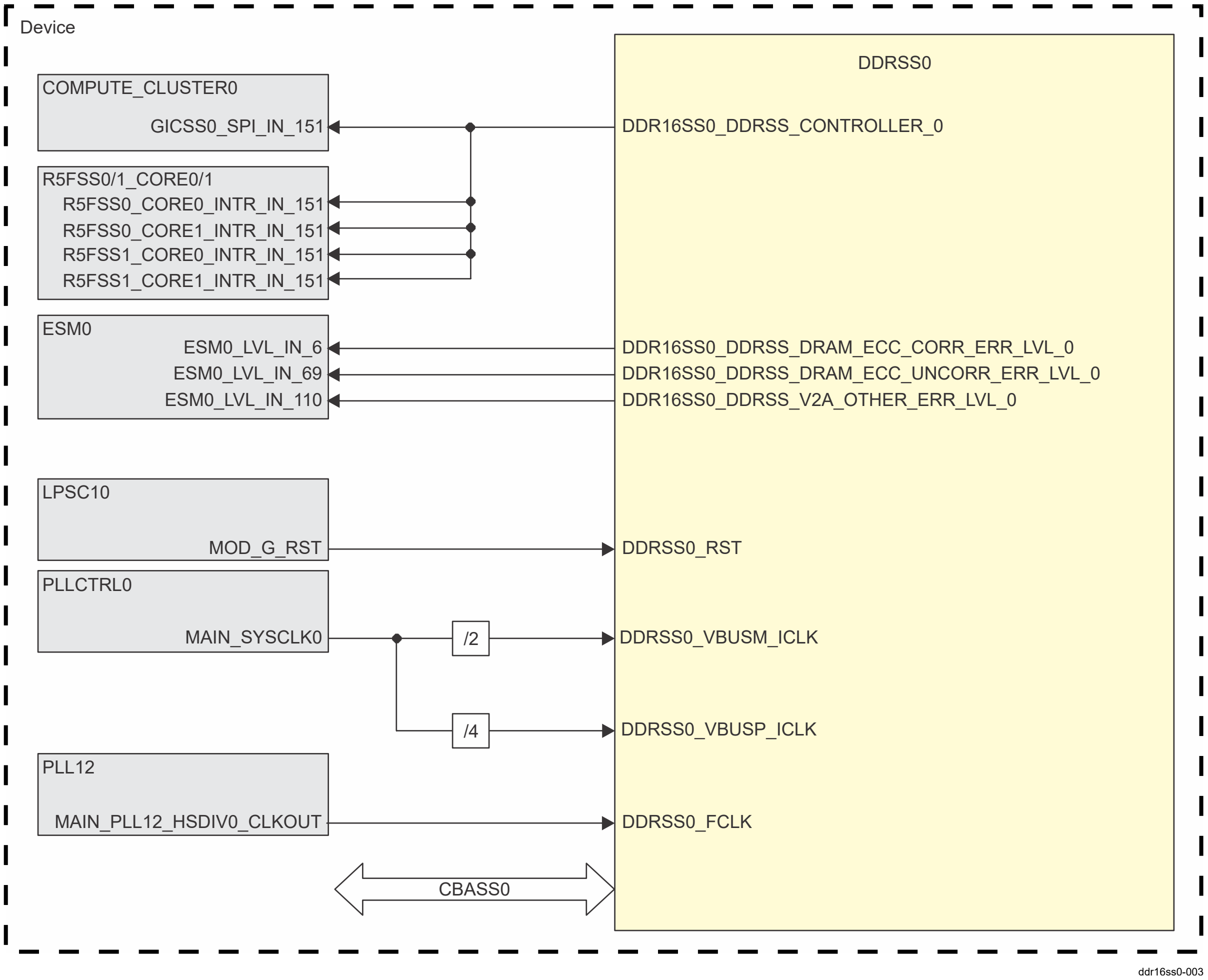

Figure 8-2. DDRSS0 Integration

Table 8-3 through Table 8-5 summarize the integration of DDRSS0 in device MAIN domain.

Table 8-3. DDRSS0 Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	**Power Domain**	**Module Domain**	**Interconnect**
DDRSS0	PSC0	PD0	LPSC10	CBASS0 (Accessed through MSMC)

Table 8-4. DDRSS0 Clocks and Resets

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
DDRSS0	DDRSS0_VBUSM_ICKL	MAIN_SYSCLK0/2	PLLCTRL0	DDRSS0 configuration interface clock
	DDRSS0_VBUSP_ICKL	MAIN_SYSCLK0/4	PLLCTRL0	DDRSS0 configuration interface clock
	DDRSS0_FCLK	MAIN_PLL12_HSDIV0_CLKOUT	PLL12	DDRSS0 functional clock. It supplies the SDRAM clock.
Resets				
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
DDRSS0	DDRSS0_RST	MOD_G_RST	LPSC10	DDRSS0 reset

Table 8-5. DDRSS0 Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
DDRSS0	DDR16SS0_DDRSS_DRAM_ECC_CORR_ERR_LVL_0	ESM0_LVL_IN_6	ESM0	DDRSS correctable error interrupt	Level
	DDR16SS0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_0	ESM0_LVL_IN_69	ESM0	DDRSS non-correctable error interrupt	Level
	DDR16SS0_DDRSS_CONTROLLER_0	GICSS0_SPI_IN_151	COMPUTE_CLUSTER0	DDR controller common interrupt	Level
		R5FSS0_CORE0_INTR_IN_151	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_151	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_151	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_151	R5FSS1_CORE1		
	DDR16SS0_DDRSS_V2A_OTHER_ERR_LVL_0	ESM0_LVL_IN_110	ESM0	MSMC2DDR bridge interrupt indicating: • Address out of range. See Section 8.1.4.4 . • Timeout counter expiry. See Section 8.1.4.5 .	Level
DMA Events					
Module Instance	**Module DMA Event**	**Destination DMA Event Input**	**Destination**	**Description**	**Type**
DDRSS0	-	-	-	-	-

Note

For more information about the DDRSS0 interrupts, see Section 8.1.4.6 .

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

8.1.4 DDRSS Functional Description

8.1.4.1 Class of Service (CoS)

Commands arriving to the DDRSS0 carry the VBUSM priority whereas the DDR controller uses another priority. The MSMC2DDR bridge has the following registers for flexible mapping of the VBUSM priority to DDR controllers's priority:

- Range match registers:
  - EMIF_SSCFG_V2A_R1_MAT_REG
  - EMIF_SSCFG_V2A_R2_MAT_REG
  - EMIF_SSCFG_V2A_R3_MAT_REG
- Priority map registers:
  - EMIF_SSCFG_V2A_DEF_PRI_MAP_REG
  - EMIF_SSCFG_V2A_R1_PRI_MAP_REG
  - EMIF_SSCFG_V2A_R2_PRI_MAP_REG
  - EMIF_SSCFG_V2A_R3_PRI_MAP_REG

This allows the system to essentially create different classes of service based on the initiator (Route ID) and the priority of the commands.

The priority map registers map the incoming priority to appropriate proirity for the DDR controller as shown in Figure 8-3.

Note

For information about Route ID, see Section 3.7 , *Route ID* in Chapter 3 , *System Interconnect*.

Figure 8-3. DDRSS CoS Mapping Diagram

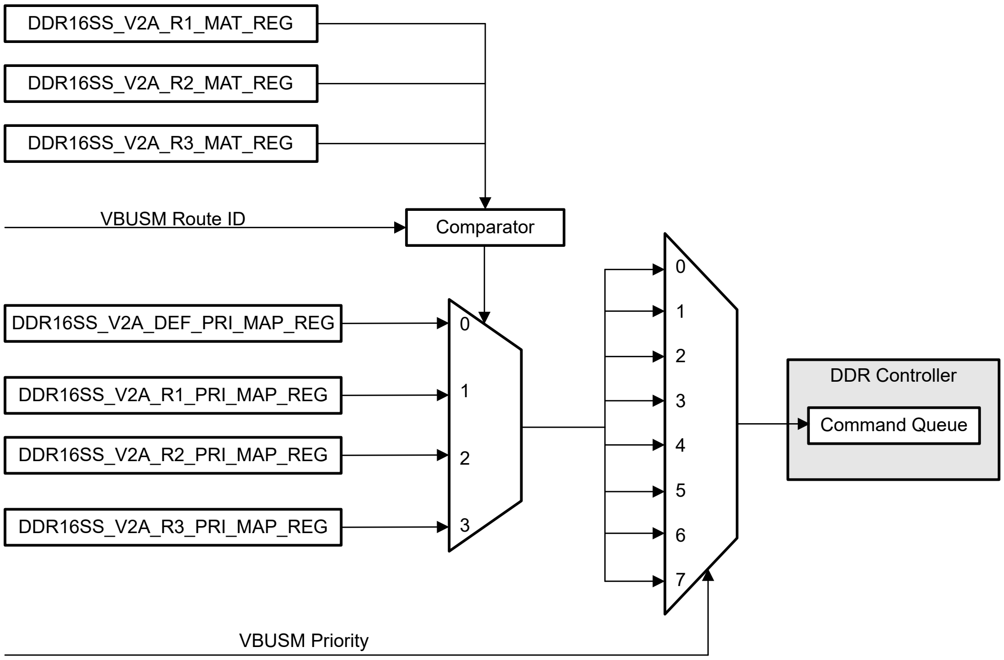

8.1.4.2 AXI Write Data All-Strobes

The DDR controller data path is connected to the MSMC2DDR bridge through AXI interface. To enable higher performance and lower latency, the bridge drives the AXI AWALLSTRB signal to a "1" when the AXI write data do not have any byte enable holes. This allows the DDR controller to accept and start processing the write command as soon as possible without waiting for all data. The AXI0_ALL_STROBES_USED_ENABLE bit in the DDR Controller must be set to a 0x1 to utilize this feature. The controller ignores the AWALLSTRB signal if AXI0_ALL_STROBES_USED_ENABLE is set to 0x0.

8.1.4.3 Inline ECC for SDRAM Data

For SDRAM data integrity, the MSMC2DDR bridge supports inline ECC on the data written to or read from the SDRAM. ECC is enabled by programming the bits in the EMIF_SSCFG_ECC_CTRL_REG register. ECC is stored together with the data so that a dedicated SDRAM device for ECC is not required.

8-bit single error correction double error detection (SECDED) ECC is calculated over 64-bit data quanta. For every 512-byte data block 64 bytes of ECC is stored inline. Thus 1/9th of the total SDRAM space is used for ECC storage and the rest 8/9th is available for system use. From system point of view that 8/9th of the SDRAM data space are seen as consecutive byte addresses. Even if there are non-ECC protected regions the previously described 1/9th-8/9th rule still applies and consecutive byte addresses are seen from system point of view. Note that 8/9 of the total SDRAM space is available for system use regardless of the size of the ECC region(s). In other words, only 8/9 of the memory is available even in non-ECC regions when ECC is enabled.

The ECC is calculated for all accesses that are within the address ranges protected by ECC. The address ranges are specified through the following registers:
- EMIF_SSCFG_ECC_R0_STR_ADDR_REG
- EMIF_SSCFG_ECC_R0_END_ADDR_REG
- EMIF_SSCFG_ECC_R1_STR_ADDR_REG
- EMIF_SSCFG_ECC_R1_END_ADDR_REG
- EMIF_SSCFG_ECC_R2_STR_ADDR_REG
- EMIF_SSCFG_ECC_R2_END_ADDR_REG

Note that the addresses in these address range registers should be in terms of the DDRSS address space, not the SoC memory space. Even though the SoC memory space for DDR may be split into multiple regions, the DDRSS address space is continuous.

For example, if the beginning of DDR is in SoC memory space 0x8000_0000 to 0xFFFF_FFFF, this corresponds to DDRSS address space 0x00000000 to 0x7FFFFFFF. If the SoC has greater DDR address reach, even at a discontinuous address, the address range for these registers would be continuous (eg, if the next DDR address at the SoC level is 0x880000000, the corresponding address would be continuous at 0x80000000)

Note that the value programmed in the ECC range start/end registers does not include the lower 16 bits of the address. For example, to represent an address of 0x40000000, the register contents would be 0x4000.

The ECC is read and verified during reads if both the EMIF_SSCFG_ECC_CTRL_REG[0] ECC_EN and EMIF_SSCFG_ECC_CTRL_REG[2] ECC_CK bits are set to 0x1. For 1-bit ECC error, the MSMC2DDR bridge corrects the data and returns it to the requestor. Although the error is corrected on the returned data, the SDRAM is not corrected. It is responsibility of the system software to correct the ECC error at that location.

It is also responsibility of the system software to pre-load the ECC protected region with known data before functional reads and writes are performed. This can be done by writing to the SDRAM with ECC enabled (EMIF_SSCFG_ECC_CTRL_REG[0] ECC_EN = 0x1 and EMIF_SSCFG_ECC_CTRL_REG[1] RMW_EN = 0x1) and ECC check disabled (EMIF_SSCFG_ECC_CTRL_REG[2] ECC_CK = 0x0). Once the data is loaded in the SDRAM, ECC check must be enabled (EMIF_SSCFG_ECC_CTRL_REG[2] ECC_CK = 0x1) before using the DDR interface.

8.1.4.3.1 ECC Cache

The MSMC2DDR bridge implements a 64-line deep ECC cache for improving inline ECC performance. Each cache line can be allocated to an initiator in the system based on its Route ID. The Route ID allocation to cache line can be done by writing to the EMIF_SSCFG_ECC_RID_INDX_REG and EMIF_SSCFG_ECC_RID_VAL_REG registers. Since the bridge uses unallocated cache lines for all read accesses without Route ID allocation, one or more locations in the cache should be kept unallocated for better performance. To ensure that at least one cache line remains unallocated, in the case all cache lines are allocated by software, the bridge automatically unallocates the 127th cache line. Write accesses without

Route ID allocation result in ECC and data writes to the SDRAM, when the EMIF_SSCFG_ECC_CTRL_REG[4] WR_ALLOC bit is set to 0x0. When EMIF_SSCFG_ECC_CTRL_REG[4] WR_ALLOC is set to 0x1, an unassigned cache-line is allocated to write accesses without Route ID allocation.

8.1.4.3.2 ECC Cache Flush

For low power modes, the bridge supports flushing the cache when DDRSS stop clock request is asserted. When a clock stop is requested, the bridge will start issuing writes to the DRAM until all dirty cache locations are written to the DRAM. Once the writes are complete, the bridge asserts an acknowledge signal to let the subsystem know that the operation is complete. The subsystem uses this acknowledge signal along with acknowledgments from other submodules to generate the final DDRSS stop clock acknowledge to the system.

8.1.4.3.3 ECC Statistics

For 1-bit ECC error, the MSMC2DDR bridge logs the address location for the error in an internal 2-level deep FIFO. It stores the first two 1-bit ECC errors. The EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG register shows the address on top of the internal FIFO. Software should write 0x1 to the EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG[29-0] ECC_1B_ERR_ADR field to pop the FIFO and display the next address stored. The FIFO is loaded with the address for the next 1-bit ECC error if it is not full. If a single address is associated with more than one ECC error, that address is logged twice.

The number of 1-bit ECC errors can be counted using the EMIF_SSCFG_ECC_1B_ERR_CNT_REG register. The MSMC2DDR bridge also supports programming a threshold in the EMIF_SSCFG_ECC_1B_ERR_THRSH_REG register. When the 1-bit error count is equal to or greater than the programmed threshold, the bridge sets the EMIF_SSCFG_V2A_INT_RAW_REG[3] ECC1BERR bit and also triggers the DDR0_DDRSS_DRAM_ECC_CORR_ERR_LVL_0 interrupt. When servicing the interrupt, software needs to clear the error count otherwise further interrupts will not be triggered. For 2-bit ECC errors, the bridge sets the EMIF_SSCFG_V2A_INT_RAW_REG[4] ECC2BERR bit and also triggers the DDR0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_0 interrupt. The bridge does not correct the data for these uncorrectable errors. Along with generating the interrupt, the bridge also reports an error to the requesting initiatior and sends all zeros for the data. The bridge also logs the address location for the error in the EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG register.

The MSMC2DDR bridge sets the EMIF_SSCFG_V2A_INT_RAW_REG[5] ECCM1BERR bit and triggers the DDR0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_0 interrupt whenever it receives multiple 1-bit errors in different data words of the same SDRAM burst. This is done because the probability of receiving multiple 1-bit errors in different data words of the same SDRAM burst is very low. If this occurs, the chances are that there were multi-bit errors in each data word. Therefore, for reliability, pessimistic approach is taken to report these as a fatal error. The threshold for the number of 1-bit errors that result in an uncorrected error, reporting can be set by writing to the EMIF_SSCFG_ECC_CTRL_REG[11-8] COR_ECC_THRESH field. For reliability, the threshold is always kept at 0/1 meaning 1-bit error in 2 or more data words is reported as a 2-bit error. For debug, the threshold can be changed to a higher value. Note that since these are multiple 1-bit errors, the statistic logging is done in the EMIF_SSCFG_ECC_1B_ERR_CNT_REG and EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG registers.

8.1.4.4 Address Alias Prevention

The MSMC2DDR bridge checks the VBUSM address received against the valid SDRAM address space programmed in the EMIF_SSCFG_V2A_CTL_REG register. If the VBUSM address for an access falls outside the programmed range the bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[1] AERR bit and also triggers the DDR0_DDRSS_V2A_OTHER_ERR_LVL_0 interrupt. The address and the Route ID for the command caused error are logged in the EMIF_SSCFG_V2A_AERR_LOG1_REG and EMIF_SSCFG_V2A_AERR_LOG2_REG registers.

For commands greater than 32 bytes with an address error, each fragment will report an error. This can cause multiple interrupts to be reported if software clears the error interrupt for the first fragment while other fragments are being executed. The address log register will always log the address for the fragment which caused the last interrupt.

The valid address range can be programmed using the EMIF_SSCFG_V2A_CTL_REG[9-5] SDRAM_IDX and EMIF_SSCFG_V2A_CTL_REG[4-0] REGION_IDX fields. Table 8-6 summarizes the scenarios for determining valid address range and interrupt generation.

Table 8-6. REGION_IDX and SDRAM_IDX Scenarios

Condition	Description
REGION_IDX = SDRAM_IDX	DDR region size is equal to the connected SDRAM size. It is SoC responsibility to ensure that the addresses received by the DDR subsystem do not fall outside the region size. No address error is generated if the address received falls outside the region size.
REGION_IDX < SDRAM_IDX	DDR region size is less than the connected SDRAM size. It is SoC responsibility to ensure that the addresses received by the DDR subsystem do not fall outside the region size. No address error is generated if the address received falls outside the region size.
REGION_IDX > SDRAM_IDX	DDR region size is greater than the connected SDRAM size. Address error is generated if the address received falls outside the connected SDRAM size.

A write access outside the programmed range is discarded. A write error associated status is sent back to the VBUSM interface.

A read access outside the programmed range is executed on the SDRAM interface as a normal read, but data will contain all zeroes before forwarding it to the VBUSM interface. A read error associated status is sent back to the VBUSM interface along with the read data containing all zeroes.

When inline ECC is enabled, the available SDRAM size is reduced by 1/9th of the size programmed in the SDRAM_IDX field. Therefore, the bridge reports an error if an access falls outside the reduced SDRAM size when inline ECC is enabled. The reduced SDRAM size limit applies to all accesses, both to the protected and non-protected ECC regions.

8.1.4.5 AXI Bus Timeout

The MSMC2DDR bridge has a timeout counter that expires when no AXI transaction can be sent to the DDR controller or no AXI response is received from the controller for a programmed time interval. The counter only counts when there are pending commands in the bridge and the AXI bus is idle. Therefore, the bridge will not time out during low-power modes. The time interval can be programmed by writing to the EMIF_SSCFG_V2A_BUS_TO[23-0] BUS_TIMER field.

Upon the expiry of the counter, the bridge terminates all pending commands in its internal FIFOs, returns error responses, sets the EMIF_SSCFG_V2A_INT_RAW_REG[2] TOERR bit and triggers the DDR0_DDRSS_V2A_OTHER_ERR_LVL_0 interrupt.

After a timeout occurs, the bridge terminates any new commands received and returns error response. Writing a value of 0x0 to the EMIF_SSCFG_V2A_BUS_TO[23-0] BUS_TIMER field exits the timeout mode. The other method to exit the timeout mode is to reset the DDRSS0, thus resetting the MSMC2DDR bridge, the DDR controller, and the DDR PHY.

8.1.4.6 DDRSS Interrupts

The MSMC2DDR bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[1] AERR bit, if the VBUSM address for an access that falls outside the DDR space programmed in the EMIF_SSCFG_V2A_CTL_REG register.

The MSMC2DDR bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[2] TOERR bit, if it detects a hang on its interface to the DDR controller.

The MSMC2DDR bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[3] ECC1BERR bit, if the threshold for 1-bit ECC errors is met.

The MSMC2DDR bridge sets to 0x1 the EMIF_SSCFG_V2A_INT_RAW_REG[4] ECC2BERR bit, in case of 2-bit errors for a read access performed within the SDRAM address range protected by ECC.

The DDRSS0 asserts particular interrupt line only if the interrupts are enabled by writing 0x1 to the corresponding bit in the EMIF_SSCFG_V2A_INT_SET_REG register. The interrupts can be disabled by writing 0x1 to the corresponding bit in the EMIF_SSCFG_V2A_INT_CLR_REG register.

When interrupts are enabled, the corresponding bits in the EMIF_SSCFG_V2A_INT_STAT_REG register are also set if an interrupt condition occurs. The interrupts can be cleared once serviced by writing 0x1 to the corresponding bit in the EMIF_SSCFG_V2A_INT_STAT_REG register as well as writing to the EMIF_SSCFG_V2A_EOI_REG register. The subsystem will send an interrupt pulse, if there are any bits set in the Interrupt Status register (EMIF_SSCFG_V2A_INT_STAT_REG) when the End of Interrupt register (EMIF_SSCFG_V2A_EOI_REG) is written.

Table 8-7 shows the events that are generated by the MSMC2DDR bridge.

Table 8-7. MSMC2DDR Bridge Events

Event Flag	Event Mask	Description
EMIF_SSCFG_V2A_INT_RAW_REG[4] ECC2BERR EMIF_SSCFG_V2A_INT_STAT_REG[4] ECC2BERR	EMIF_SSCFG_V2A_INT_SET_REG[4] ECC2BERR_EN EMIF_SSCFG_V2A_INT_CLR_REG[4] ECC2BERR_EN	Generated in case of 2-bit errors for a read access within the ECC protected SDRAM address range. For more information, see Section 8.1.4.3.3 .
EMIF_SSCFG_V2A_INT_RAW_REG[3] ECC1BERR EMIF_SSCFG_V2A_INT_STAT_REG[3] ECC1BERR	EMIF_SSCFG_V2A_INT_SET_REG[3] ECC1BERR_EN EMIF_SSCFG_V2A_INT_CLR_REG[3] ECC1BERR_EN	Generated in case of meeting the threshold for 1-bit ECC errors. For more information, see Section 8.1.4.3.3 .
EMIF_SSCFG_V2A_INT_RAW_REG[2] TOERR EMIF_SSCFG_V2A_INT_STAT_REG[2] TOERR	EMIF_SSCFG_V2A_INT_SET_REG[2] TOERR_EN EMIF_SSCFG_V2A_INT_CLR_REG[2] TOERR_EN	Generated in case of a hang of the interface between the MSMC2DDR bridge and the DDR controller. For more information, see Section 8.1.4.5 .
EMIF_SSCFG_V2A_INT_RAW_REG[1] AERR EMIF_SSCFG_V2A_INT_STAT_REG[1] AERR	EMIF_SSCFG_V2A_INT_SET_REG[1] AERR_EN EMIF_SSCFG_V2A_INT_CLR_REG[1] AERR_EN	Generated if the VBUSM address for an access falls outside the programmed range. For more information, see Section 8.1.4.4 .

8.1.4.7 DDRSS Memory Regions

Table 8-8 shows all memory regions associated with the DDRSS0.

Table 8-8. DDRSS0 Memory Regions

Region	Start Address	End Address	Region Size
DDRSS0 wrapper logic registers	0x00F300000	0x00F3001FF	512 B
DDR controller registers	0x00F308000	0x00F309FFF	8 KB
DDR PHY independent module registers	0x00F30A000	0x00F30BFFF	8 KB
DDR PHY registers	0x00F30C000	0x00F30FFFF	16 KB
External SDRAM data space	0x080000000	0x0FFFFFFFF	2 GB

8.1.4.8 DDRSS Dynamic Frequency Change Interface

This interface is used for handshaking between DDRSS0 and CTRL_MMR0 to dynamically change DDR clock frequency to support LPDDR4 Frequency Set Point (FSP). The frequency change can be initiated either by a SoC processor or by the DDRSS0.

The associated CTRL_MMR0 registers for processor initiated frequency change are:

- CTRLMMR_CHNG_DDR4_FSP_REQ
- CTRLMMR_CHNG_DDR4_FSP_ACK

The associated CTRL_MMR0 registers for DDRSS0 initiated frequency change are:

- CTRLMMR_DDR4_FSP_CLKCHNG_REQ
- CTRLMMR_DDR4_FSP_CLKCHNG_ACK

The sequence for an SoC processor initiated frequency change is as follows:

1. The processor writes the desired frequency to the CTRLMMR_CHNG_DDR4_FSP_REQ[1-0] REQ_TYPE field.
2. The processor sets to 0x1 the CTRLMMR_CHNG_DDR4_FSP_REQ[8] REQ bit to initiate frequency change.
3. The processor programs PLL12 according to the CTRLMMR_CHNG_DDR4_FSP_REQ[1-0] REQ_TYPE value.
4. The processor polls the CTRLMMR_CHNG_DDR4_FSP_ACK[7] ACK and CTRLMMR_CHNG_DDR4_FSP_ACK[0] ERROR bits to check if the frequency change has been completed successfully.

The sequence for DDRSS0 initiated frequency change is as follows:

1. DDRSS0 requests frequency change by asserting the CTRLMMR_DDR4_FSP_CLKCHNG_REQ[7] REQ bit and the CTRLMMR_DDR4_FSP_CLKCHNG_REQ[1-0] REQ_TYPE field. The REQ bit is also connected to the DDR0_DDRSS_PLL_FREQ_CHANGE_REQ_0 interrupt.
2. Software reads the CTRLMMR_DDR4_FSP_CLKCHNG_REQ[1-0] REQ_TYPE value and programs PLL12 accordingly.
3. After the DDRSS0_FCLK has been changed software should set to 0x1 the CTRLMMR_DDR4_FSP_CLKCHNG_ACK[0] ACK bit.

8.1.4.9 DDR Controller Functional Description

Figure 8-4 shows the DDR controller blocks along with the DDR PHY and MSMC2DDR bridge.

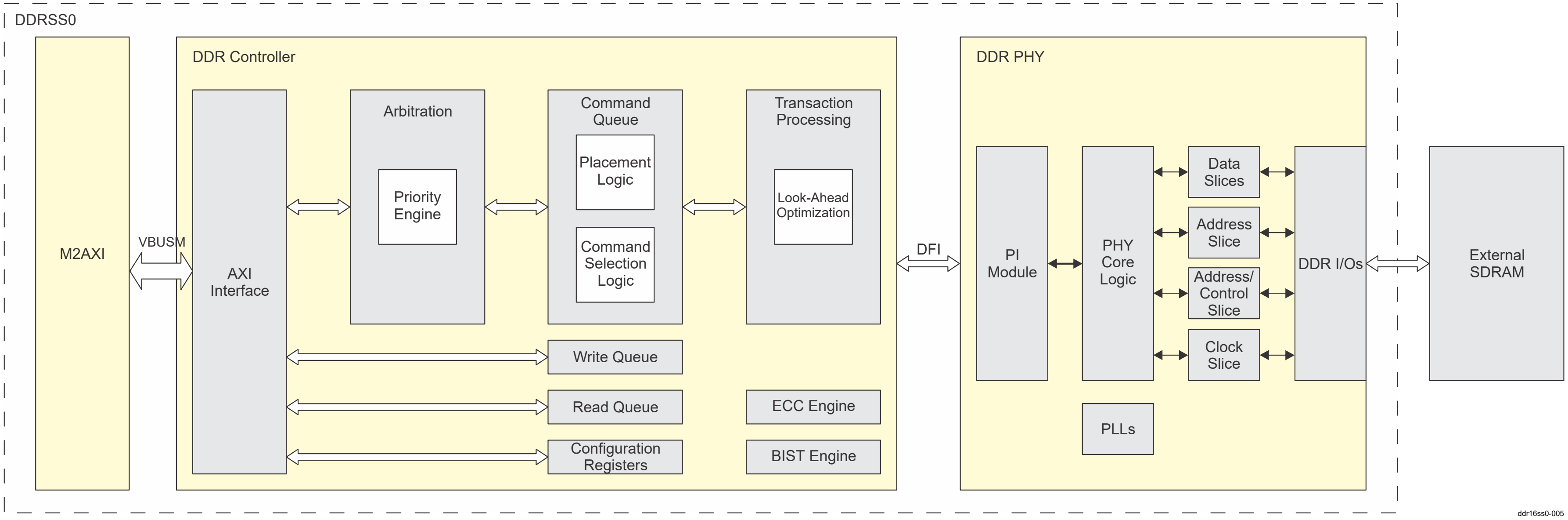

Note

The ECC Engine block of the DDR controller is not supported.

Figure 8-4. DDR Controller Functional Blocks

8.1.4.9.1 DDR PHY Interface (DFI)

The DDR controller and DDR PHY are connected via DDR PHY Interface (DFI) which is used for transferring control information and data between the PHY and the controller. For more information about DFI, see http://www.ddr-phy.org/.

8.1.4.9.2 Command Queue

The DDR controller contains a command queue which uses a placement algorithm to determine the order of commands to be placed into the command queue. The placement logic follows many rules to determine where new commands should be inserted into the queue, relative to the contents of the command queue at a time. Placement is determined by considering address collisions, source collisions, data collisions, command types and priorities. The placement logic also attempts to maximize efficiency of the DDR controller through command grouping and bank splitting.

8.1.4.9.2.1 Placement Logic

The placement logic is a 2-stage queue which determines the order of commands that run in the DDR controller. The placement logic follows rules for determining placement of new commands into the queue, relative to the contents of the command queue at that time. Placement is determined by considering coherency, address collisions, source collisions, data collisions, user assigned priority, latency, age, and command type to offer low latency for critical controllers while optimizing bandwidth for all controllers. A second reordering stage allows ready-to-run commands to start even if the head-of-queue command is not yet ready to run. In addition, the queue can be disabled completely, resulting in an in-line queue that services requests in the order that they arrive.

The DDR controller also has a full look-ahead facility that reduces the effect of page misses by pre-conditioning rows for upcoming requests by using “spare” cycles in preceding transactions.

8.1.4.9.2.2 Command Selection Logic

After a command is in the command queue, command selection logic determines the method of pulling commands from the queue for running. On each clock cycle, the selection logic scans the entries of the command queue for determining the command to run. Commands for running are based on bank readiness, availability of at least 1 burst of data (writes), availability of storage for at least 1 burst of data (reads), bus turnaround timing, and conflicts. Similar to the placement rules, a command does not run before a command that was placed ahead of it in the command queue if it conflicts with address, source ID, or bank commands. Lower priority commands can run ahead of higher priority commands if the higher priority commands are not ready to run, as long as they do not conflict with commands that are ahead in the command queue.

8.1.4.9.3 Transaction Processing

The transaction command processing logic is used to process the commands in the command queue. The logic organizes the commands to the memories in such a way that data throughput is maximized. Bank opening and closing cycles are used for data transfers. The logic reviews the entire command queue for look-ahead of which banks have to be accessed in the future and ensures that the programed memory timing conditions are met. This flexibility allows the controller to be tuned to extract the maximum performance out of memories. During processing, the controller examines the commands and issues the appropriate set of signals to the memory.

8.1.4.9.4 Paging Policy

The DDR controller offers a flexible paging policy that allows open page operation, closed page operation, or an auto-precharge-per-command option that allows both modes simultaneously. Auto-precharge-per-command allows marking a particular controller or transaction (for example, a CPU cache) as a closed-page transaction. This type of transaction reduces power and improves latency for the next transaction to a different row in the same SDRAM bank. Other transactions can be marked as open page transactions. This type of transaction reduces power and improves latency and bandwidth to the next transaction to the same row in the same SDRAM bank.

8.1.4.9.5 DDR Controller Initialization

Once the power to the SDRAM and SoC is stable, the DDR controller must be initialized. It then automatically initializes the external memory. Please refer to the Processor SDK for the software drivers to initalize the DDR registers and memory

Note

To facilitate the programming of these registers, refer to the device-specific DDR Subsystem Register Configuration Tool available at http://dev.ti.com/sysconfig.

8.2 Region-based Address Translation (RAT) Module

This section describes the RAT functionality.

8.2.1 RAT Functional Description

8.2.1.1 RAT Availability

Table 8-9 lists the device modules and subsystems which have RAT module.

Table 8-9. Device Modules and Subsystems with RAT Module

Module Instance	Domain	
	MCU	MAIN
MCU_M4FSS0	✓	-
DMSC0	-	✓
R5FSS0_CORE0	-	✓
R5FSS0_CORE1	-	✓
R5FSS1_CORE0	-	✓
R5FSS1_CORE1	-	✓
PRU_ICSSG0_CPU0	-	✓
PRU_ICSSG0_CPU1	-	✓
PRU_ICSSG1_CPU0	-	✓
PRU_ICSSG1_CPU1	-	✓

8.2.1.2 RAT Operation

The RAT module performs a region based address translation. It translates a 32-bit input address into a 48-bit output address. Any input transaction that starts inside of a programmed region will have its address translated, if the region is enabled. Any disabled region is ignored from the translation lookup.

RAT has 16 regions, with each region having dedicated registers that define its attributes:

- Base address of the region, via the RAT_BASE_k register.
- Size of the region, via the RAT_CTRL_k register.
- Translated base address (48-bit). It is defined by 32-bit lower address via the RAT_TRANS_L_k register, and 16-bit upper address via the RAT_TRANS_U_k register.

The input addresses are compared against all the enabled regions in parallel. The region size defines how many of the lowest address bits are included in the region space, starting from a 1B space to a 4GB space. Then the upper bits not part of the region are used for the lookup and comparison, matching those bits of the input addresses against the region base address. The region matches when it is enabled and the compare matches. The first region that matches has the output address set with the region translated base address upper bits. The lower bits that are part of the region size are copied from the input address to the output address. If there are no region matches then the input address is copied to the output address entirely.

RAT does not automatically correct transactions that cross region boundaries, that is, start inside of a region and end outside of it, or start outside of a region and end inside of it. If a boundary crossing transaction is detected, then RAT annuls the transaction as illegal, generates an interrupt and logs an error, as explained in Section 8.2.1.3 , *RAT Error Logging*.

Note

The region base address and translated base address must be aligned to the defined region size. For example, if the defined region size is 64KB, then the two addresses must be 64KB aligned. This is software responsibility as RAT does not perform such alignment check. Regions that are not aligned have unpredictable results.

Moreover, multiple region definitions must not overlap in their covered address space. RAT does not check for this, so it is software responsibility to take care of it. Overlapping regions may lead to unpredictable results.

8.2.1.3 RAT Error Logging

The error log consists of a series of registers that capture the details of the transaction, including the input address that caused the error. These registers are the following:

- RAT_EXCEPTION_LOGGING_HEADER0 and RAT_EXCEPTION_LOGGING_HEADER1
- RAT_EXCEPTION_LOGGING_DATA0 through RAT_EXCEPTION_LOGGING_DATA3

The RAT module can capture one error before it is cleared by software. The error logging is enabled by default, but can be disabled via the RAT_EXCEPTION_LOGGING_CONTROL[0] DISABLE_F bit. Upon error logging an interrupt is also generated. To clear the log, software must either read the final error logging register, or manually clear the RAT_EXCEPTION_PEND_CLEAR[0] PEND_CLR bit by setting it to 0x1. This will clear the error status, and not the actual log registers, but it does allow the next error to be captured into the log registers. If the status is not cleared and additional errors are detected, they are not logged.

After an error occurs and is cleared (whether by reading the final error logging register or by clearing the status bit), the RAT_EOI_REG register must be written to guarantee the next interrupt pulse will be produced.

Table 8-10 shows the RAT source ID mapping which is associated with the RAT_EXCEPTION_LOGGING_HEADER0[23-8] SRC_ID field.

Table 8-10. RAT Source ID Mapping

Module Instance	Source ID Value (Decimal)
DMSC0	0
MCU_M4FSS0	2
R5FSS0_CORE0	4
R5FSS0_CORE1	5
R5FSS1_CORE0	6
R5FSS1_CORE1	7
PRU_ICSSG0_CPU0	16
PRU_ICSSG0_CPU1	17
PRU_ICSSG1_CPU0	18
PRU_ICSSG1_CPU1	19

Chapter 9

Interrupts

This chapter describes the details related to device interrupts.

9.1 Interrupt Architecture

The SoC has many peripherals and a large number of event sources (interrupt, time sync or DMA). The use of events is completely dependent on a user's specific application, which drives a need for maximum flexibility in which event sources are used in the system. It is also completely up to software control as to how the events are serviced.

The SoC includes the following interrupt servicing modules (hosts):

- Safety-channel (or general-purpose) microcontroller unit (MCU_M4FSS)
  - Single Arm Cortex-M4F core
  - Nested vectored interrupt controller (NVIC)
- Microprocessor unit (A53SS0)
  - Dual-A53 cluster
  - SoC-level generic interrupt controller (GICSS0) supports both cores in the dual-A53 cluster
- Real-time microcontroller units (R5FSS0, R5FSS1), each supporting:
  - Dual-R5F cluster
  - Vectored interrupt manager (VIM)
- Industrial communications subsystems (PRU_ICSSG0, PRU_ICSSG1), each supporting:
  - Two programmable real-time units (PRUs)
  - Local interrupt controller (INTC)

Most of the system events are routed directly to the various proccesing elements but in some cases it is impractical to route all events of a certain group (for example, GPIO events) to each processing element. For this purpose, the SoC integrates several interrupt router (INTRTR) instances. Each interrupt router aggregates a number of system events and can route each event to a given processing element by using simple combinational logic (a set of multiplexors). Event selection is controlled through the associated registers within each interrupt router.

The following interrupt router instances are part of the SoC interrupt architecture:

- MCU domain GPIO interrupt router (MCU_GPIOMUX_INTRTR0):
  - Provides selection of active MCU_GPIO0 module interrupts
  - Supported by dedicated MCU domain GPIO muxing that provides virtualization
- MAIN domain GPIO interrupt router (GPIOMUX_INTRTR0):
  - Provides selection of active GPIO0 and GPIO1 module interrupts
  - Supported by dedicated MAIN domain GPIO muxing that provides virtualization

In addition, the following interrupt router instances are part of the SoC time sync architecture:

- Time sync event router (TIMESYNC_INTRTR0):
  - Provides selection of active common platform time synchronization (CPTS) events for routing to CPTS capable modules
- Compare event router (CMPEVT_INTRTR0):
  - Provides selection of active CPTS counter compare events for routing as processor interrupts or DMA events

For more details on time sync routers, see Section 10.3.2 , *Time Sync Routers*.

9.2 Interrupt Controllers

9.2.1 Generic Interrupt Controller (GICSS)

This section describes the Generic Interrupt Controller (GICSS) module in the device.

9.2.1.1 GICSS Overview

The device GICSS is a TI module that is based on the Arm GIC-500 interrupt controller. The Arm GIC-500 is a high-performance, area-optimized, built-time configurable interrupt controller which detects, manages, and distributes system interrupts to the Arm Cortex-A53 processors in the Compute Cluster.

The Arm GIC-500 is compliant to the Arm GICv3 standard. It only supports cores (such as A53) that implement the Armv8 architecture and the GIC CPU interface with the standard GIC Stream Protocol Interface. The GICSS includes additional logic (TI wrapper) to fully integrate the Arm GIC-500 into the SoC.

The device includes one GICSS instance. Table 9-1 shows GICSS allocation across device domains.

Table 9-1. GICSS Allocation Across Device Domains

Module Instance	Domain	
	MCU	MAIN
GICSS0	–	✓

9.2.1.1.1 GICSS Features

Note

This chapter provides only a brief description of the GICSS functionality and features. For more details on this module, refer to the *Arm®CoreLink™ GIC-500 Generic Interrupt Controller Technical Reference Manual*.

The Arm GIC-500 supports the following features in the device:

- Module revision: r1p1
- Supports both cores in the dual-A53 MPU cluster
- 16 software generated interrupts (SGIs) per core
- 16 private peripheral interrupts (PPIs) per core
- 256 shared peripheral interrupts (SPIs)
- Locality-specific peripheral interrupts (LPIs), used for message-based interrupts
- Interrupt translation service (ITS)
  - Device isolation
  - ID translation for message-based interrupts
  - This allows virtual machines to program devices directly
- Interrupt masking and prioritization
- Programmable, affinity-based interrupt routing
- 32 priorities for each interrupt
- Three different interrupt groups
  - Group 0
  - Non-secure group 1
  - Secure group 1

Additionally, the GICSS wrapper logic provides the following features:

- Synchronizes interrupt inputs to GICSS clock
- Implements AXI2VBUSM and VBUSM2AXI bridges
  - Used for bus protocol conversion (AXI-to-VBUSM and VBUSM-to-AXI, respectively)
- Implements an integrated ECC aggregator
  - Only used to inject errors (for testing purposes)

9.2.1.1.2 GICSS Not Supported Features

The GICSS does not support the following features:

- GICv2 backwards compatibility
- AWID-based LPI mapping

9.2.1.2 GICSS Integration

This section describes the GICSS module integration in the device, including information about clocks, resets, and hardware requests.

Figure 9-1 shows the GICSS module integration.

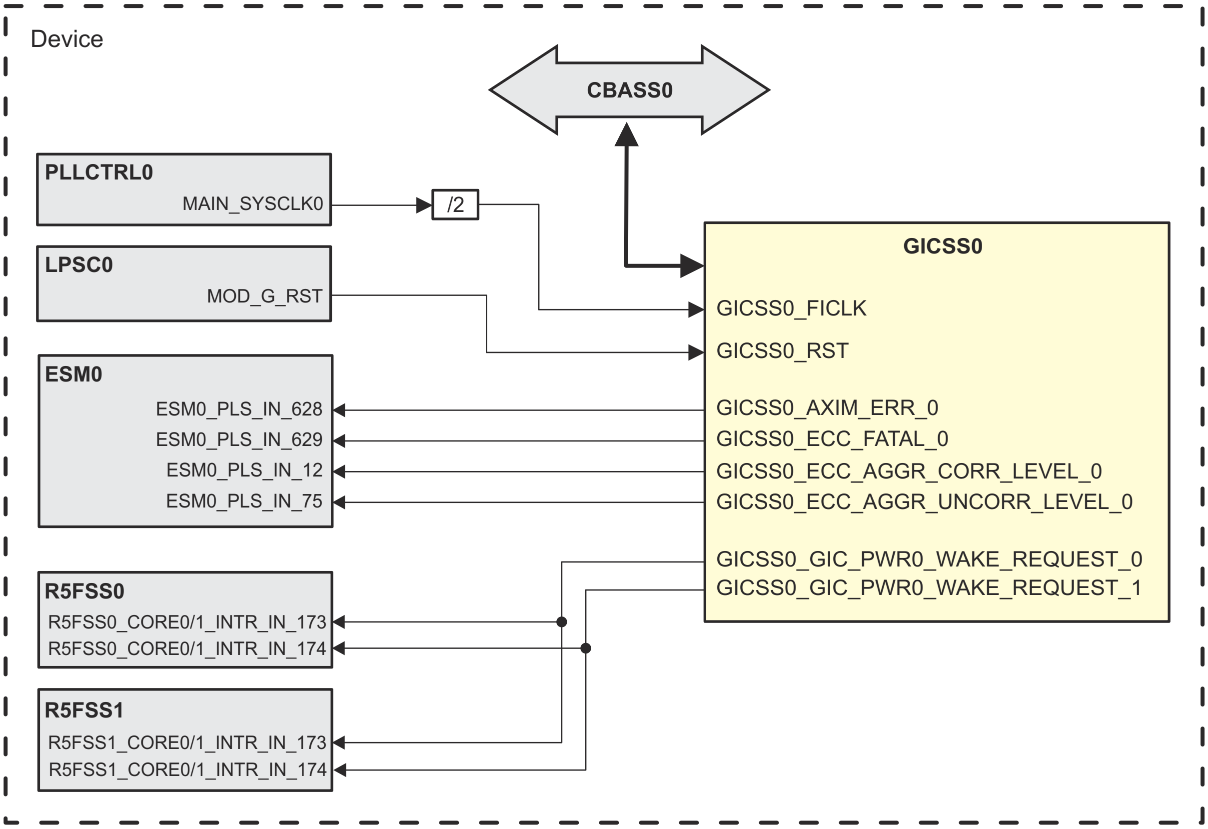

Figure 9-1. GICSS Integration

Table 9-2 through Table 9-4 summarize the GICSS integration.

Table 9-2. GICSS Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
GICSS0	PSC0	PD0	LPSC0	CBASS0

Table 9-3. GICSS Clocks and Resets

Clocks				
Module Instance	Module Clock Input	Source Clock Signal	Source	Description
GICSS0	GICSS0_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	GICSS0 functional and interface clock
Resets				
Module Instance	Module Reset Input	Source Reset Signal	Source	Description
GICSS0	GICSS0_RST	MOD_G_RST	LPSC0	GICSS0 hardware reset

Table 9-4. GICSS Hardware Requests

Interrupt Requests

Table 9-4. GICSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GICSS0	GICSS0_AXIM_ERR_0	ESM0_PLS_IN_166	ESM0	GICSS0 bus transaction error interrupt	Pulse
	GICSS0_ECC_FATAL_0	ESM0_PLS_IN_167	ESM0	GICSS0 ECC fatal error interrupt	Pulse
	GICSS0_ECC_AGGR_CORR_LEVEL_0	ESM0_LVL_IN_12	ESM0	GICSS0 correctable (SEC) error interrupt	Level
	GICSS0_ECC_AGGR_UNCORR_LEVEL_0	ESM0_LVL_IN_75	ESM0	GICSS0 uncorrectable (DED) error interrupt	Level
	GICSS0_GIC_PWR0_WAKE_REQUEST_0	R5FSS0_CORE0_INTR_IN_173	R5FSS0_CORE0	GICSS0 wake request for A53 core 0	Level
		R5FSS0_CORE1_INTR_IN_173	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_173	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_173	R5FSS1_CORE1		
	GICSS0_GIC_PWR0_WAKE_REQUEST_1	R5FSS0_CORE0_INTR_IN_174	R5FSS0_CORE0	GICSS0 wake request for A53 core 1	Level
		R5FSS0_CORE1_INTR_IN_174	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_174	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_174	R5FSS1_CORE1		

Note

Table 9-4 lists only the GICSS interrupt outputs. These GICSS interrupts are further described in Section 9.2.1.3.5 , *GICSS Interrupt Outputs*.

9.2.1.3 GICSS Functional Description

Note

This chapter provides only a brief description of the GICSS functionality and features. For more details on this module, refer to the *Arm® CoreLink™ GIC-500 Generic Interrupt Controller Technical Reference Manual*.

9.2.1.3.1 GICSS Block Diagram

Figure 9-2 shows the GICSS block diagram.

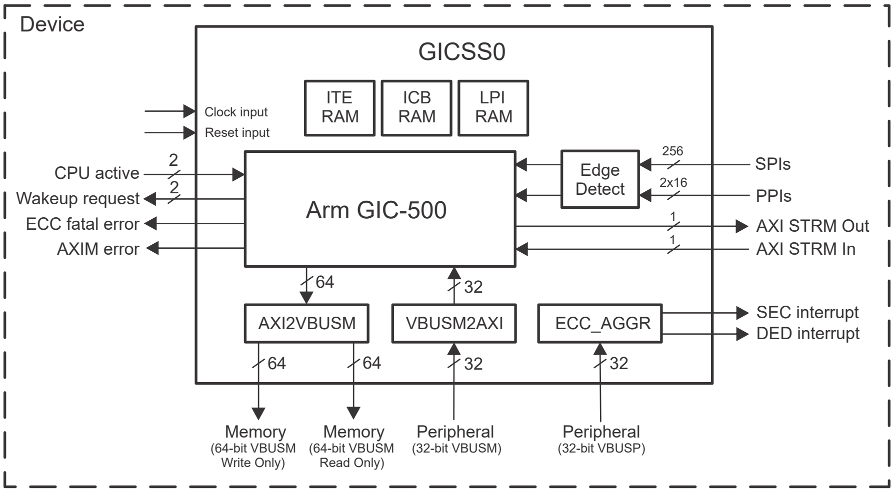

Figure 9-2. GICSS Block Diagram

9.2.1.3.2 Arm GIC-500

The Arm GIC-500 is responsible for detecting, managing and communicating system interrupts to the dual-core A53 cluster. The main difference between the Arm GIC-500 and previous Arm GIC versions is the direct communication with the CPU(s). Previously, an interrupt controller would set a pending bit to a CPU and that CPU would then have to query an interrupt controller MMR to find out what to do. Now, the Arm GIC-500 sends interrupts to a CPU via a dedicated message interface and the CPU communicates back about interrupts through the same interface. The CPU now uses writes and reads to system registers instead of over the memory interface. This leads to reduced latency and the ability to route interrupts to different CPUs based on a set of rules.

The Arm GIC-500 is divided into three main sections:

- **Distributor**: The Distributor receives interrupts from the wire interrupts and the programming interface. It is responsible for prioritizing these interrupts and sending them to the CPU interface via the GIC Stream Protocol Interface.
- **Redistributor**: There is one Redistributor per core. Each Redistributor holds the state that is individual to a particular core (such as the settings for PPIs and SGIs). It also stores the LPIs for that core after they have been generated using the ITS.
- **ITS**: The ITS is responsible for translating message-based interrupts from device peripherals into LPIs. The user can also use the ITS to manage existing LPIs. Note that the ITS is not used for other types of interrupt

9.2.1.3.3 GICSS Interrupt Types

The GICSS supports four types of interrupts:

- *Software Generated Interrupts (SGIs)*: There are 16 SGIs (ID0-ID15). These are inter-processor interrupts. SGIs can be sent using either Arm system registers or by writing to the Software Generated Interrupt Register (GICD_SGIR).

- *Private Peripheral Interrupts (PPIs)*: There are 16 PPIs (ID16-ID31). These are wired interrupts dedicated to a specific CPU. Many are reserved to specific functions via convention. These can be either active-low levels (by default), or rising edge triggered (software programmable).
- *Shared Peripheral Interrupts (SPIs)*: There are 256 SPIs (ID32-ID288). These are wired interrupts that can be routed to any core or cluster, based on the programming of that interrupt in the GICSS. These are active-high levels (by default), or rising edge triggered (software programmable).
- *Locality-Specific Peripheral Interrupts (LPIs)*: There are 57,344 of these. These interrupts are used for message-based interrupts from a peripheral. They are generated through writes to the GICSS peripheral interface. The information associated with these is located in memory. The GICSS keeps a small 64-entries cache on-board in order to reduce latency either for specific interrupts or for most-recently-used. LPIs can be routed to different CPUs based on programmed rules.

9.2.1.3.4 GICSS Interfaces

The GICSS has the following main interfaces:

- A pair of 64-bit VBUSM write-only and read-only controller interfaces
  - AXI2VBUSM bridge converts the standard 64-bit AXI4 controller interface into this pair of interfaces
  - The AXI4 controller interface allows the GICSS ITS and redistributors to access main memory
- 32-bit VBUSM peripheral interface
  - Provides access to Arm GIC-500 internal resources
  - Handles all message-based interrupts. Message-based interrupts can generate SPIs or LPIs, depending on the register that is written
  - VBUSM2AXI bridge converts this interface into an 32-bit AXI4 peripheral interface
- 32-bit VBUSP peripheral interface
  - Provides access to internal ECC aggregator
- Physical interrupt and power signals
  - Inputs: CPU active signals, SPIs and PPIs (can be programmed as either level-sensitive, or edge-triggered)
  - Outputs: Error signals and wake-up requests
- GIC Stream Protocol Interface
  - Consists of a pair of AXI4-Stream interfaces (one upstream and one downstream 16-bit AXI4-Stream interface) that the GICSS uses to send interrupts to the core and receive notifications when the core activates interrupts
  - There is a pair of physical interfaces, one in each direction, for each cluster

9.2.1.3.5 GICSS Interrupt Outputs

Table 9-5 lists the interrupts that are generated by the GICSS.

Table 9-5. GICSS Interrupt Outputs

Interrupt Name	Description
GICSS0_AXIM_ERR_0	GICSS bus error interrupt. This interrupt is triggered if the GICSS receives an error on a bus transaction, such as a decode or protection error. This is a pulse-high interrupt. If this interrupt occurs, the GICSS might lose interrupts and must be reset. If it is not reset, behavior becomes unpredictable.
GICSS0_ECC_FATAL_0	GICSS uncorrectable ECC error interrupt. Indicates an uncorrectable 2-bit error detected in one of the ITS cache memories. This is a pulse-high interrupt. If this interrupt occurs, the GICSS might lose interrupts and must be reset. If it is not reset, behavior becomes unpredictable.
GICSS0_ECC_AGGR_CORR_LEVEL_0	GICSS ECC aggregator correctable (SEC) error interrupt
GICSS0_ECC_AGGR_UNCORR_LEVEL_0	GICSS ECC aggregator uncorrectable (DED) error interrupt
GICSS0_GIC_PWR0_WAKE_REQUEST_0	GICSS wake requests for A53 cores. Asserted state indicates that an interrupt is pending for a processor that has set the PROCESSORSLEEP bit in the GICR_WAKER register. This bit indicates that the SoC should wake up the indicated CPU so that it can process the interrupt.
GICSS0_GIC_PWR0_WAKE_REQUEST_1	

9.2.1.3.6 GICSS ECC Support

The Arm GIC-500 has built-in SECDED ECC on its memories to protect against errors. The syndrome generation and checking is done internally.

Additionally, the GICSS wrapper integrates an ECC aggregator (GICSS0_ECC_AGGR) in order to allow errors to be injected for testing purposes. The generic ECC aggregator functionality is described in Section 12.6.4 , *ECC Aggregator*. Note that the GICSS0_ECC_AGGR supports only a subset of this functionality.

Table 9-6 shows the memory ID for each ECC endpoint. The corresponding memory ID needs to be written in the GICSS0_ECC_AGGR_VECTOR[10-0] ECC_VECTOR bit field for proper operation.

Table 9-6. GICSS0_ECC_AGGR Memory ID Mapping

ECC Aggregator	Memory ID	ECC Endpoint
GICSS0_ECC_AGGR	0	ICB RAM
	1	ITE RAM
	2	LPI RAM
	3	VBUSM2AXI bridge
	4	AXI2VBUSM read bridge
	5	AXI2VBUSM write bridge

9.2.1.3.7 GICSS AXI2VBUSM and VBUSM2AXI Bridges

The GICSS uses the AXI4 controller interface to allow the ITS and redistributors to access main memory. It is expected that the main memory (attached to a CBASS VBUSM port) holds the following:

- ITS translation tables
- ITS command queue, which is written by software in order to program the ITS
- LPI configuration table, which holds the priorities and enable bits for LPIs
- LPI pending tables, which can hold information on whether each LPI is pending on each core

The AXI2VBUSM bridge converts the standard 64-bit AXI4 controller interface into a pair of 64-bit VBUSM write-only and read-only controller interfaces. AXI4 has a separate command channel for read and write, and the AXI2VBUSM bridge keeps them separate, so that the system may prioritize or arbitrate the traffic between them as appropriate.

The GICSS uses the AXI4 peripheral interface to provide access to the programming interfaces of all its parts (distributor, redistributors, ITS). The VBUSM2AXI bridge converts the standard 32-bit VBUSM controller interface into an 32-bit AXI4 peripheral interface.

Note

The AXI2VBUSM and VBUSM2AXI bridges do not implement any MMRs.

9.2.1.4 GICSS Registers

The GICSS has three primary memory regions:

- Arm GIC-500 region 0
  - Used for normal (non-ITS) GICSS register accesses (GICD_* and GITS_* register spaces)
  - Referred to as GICSS0_GIC in this TRM
  - Referred to as **awuser_s[3]/aruser_s[3] = 0** in the Arm GIC-500 TRM
- Arm GIC-500 region 1
  - Used for ITS translation service register accesses (GITS_TRANSLATER)
  - Referred to as GICSS0_GIC_TRANSLATER in this TRM
  - Referred to as **awuser_s[3]/aruser_s[3] = 1** in the Arm GIC-500 TRM
- GICSS ECC aggregator region
  - Referred to as GICSS0_REGS in this TRM

9.2.1.4.1 Arm GIC-500 Registers

Table 9-7 and Table 9-8 show the Arm GIC-500 memory regions.

Table 9-7. Arm GIC-500 Memory Region 0

Instance	Base Address
Distributor registers (GICD_*)	0180 0000h
Distributor registers for message-based SPIs (GICD_*)	0181 0000h
ITS translation service control registers (GITS_*)	0182 0000h
Redistributor registers for control and physical LPIs for A53 core 0 (GICR_*)	0184 0000h
Redistributor registers for SGIs and PPIs for A53 core 0 (GICR_*)	0185 0000h
Redistributor registers for control and physical LPIs for A53 core 1 (GICR_*)	0186 0000h
Redistributor registers for SGIs and PPIs for A53 core 1 (GICR_*)	0187 0000h

Table 9-8. Arm GIC-500 Memory Region 1

Instance	Base Address
GICSS0_GIC_TRANSLATER(1)	0100 0000h

(1) Referred to as GITS_TRANSLATER in Arm documentation.

Note

According to the Arm GIC-500 TRM, the GITS_TRANSLATER region is supposed to start at offset 30000h in the Arm GIC-500 address map. However, because the SoC implementation uses address-based method of accessing the GITS_TRANSLATER, it is accessed through a SoC assigned address and not through the 30000h offset defined in the Arm GIC-500 TRM.

For detailed Arm GIC-500 register map and register descriptions, refer to the *Arm® CoreLink™ GIC-500 Generic Interrupt Controller Technical Reference Manual*.

9.2.1.4.2 GICSS0_ECC_AGGR Registers

Table 9-10 lists the memory-mapped registers for the GICSS0_ECC_AGGR registers. All register offset addresses not listed in Table 9-10 should be considered as reserved locations and the register contents should not be modified.

Table 9-9. GICSS0_ECC_AGGR Instances

Instance	Base Address
GICSS0_REGS	3F00 4000h

Table 9-10. GICSS0_ECC_AGGR Registers

Offset	Acronym	Register Name	GICSS0_REGS Physical Address
0h	GICSS0_ECC_AGGR_REV	Aggregator revision register	3F00 4000h
8h	GICSS0_ECC_AGGR_VECTOR	ECC vector register	3F00 4008h
Ch	GICSS0_ECC_AGGR_STAT	Misc status register	3F00 400Ch
3Ch	GICSS0_ECC_AGGR_SEC_EOI_REG	SEC EOI register	3F00 403Ch
40h	GICSS0_ECC_AGGR_SEC_STATUS_REG0	SEC interrupt status register 0	3F00 4040h
80h	GICSS0_ECC_AGGR_SEC_ENABLE_SET_REG0	SEC Interrupt enable set register 0	3F00 4080h
C0h	GICSS0_ECC_AGGR_SEC_ENABLE_CLR_REG0	SEC Interrupt enable clear register 0	3F00 40C0h
13Ch	GICSS0_ECC_AGGR_DED_EOI_REG	DED EOI register	3F00 413Ch
140h	GICSS0_ECC_AGGR_DED_STATUS_REG0	DED interrupt status register 0	3F00 4140h
180h	GICSS0_ECC_AGGR_DED_ENABLE_SET_REG0	DED Interrupt enable set register 0	3F00 4180h
1C0h	GICSS0_ECC_AGGR_DED_ENABLE_CLR_REG0	DED Interrupt enable clear register 0	3F00 41C0h
200h	GICSS0_ECC_AGGR_AGGR_ENABLE_SET	AGGR Interrupt enable set register	3F00 4200h
204h	GICSS0_ECC_AGGR_AGGR_ENABLE_CLR	AGGR Interrupt enable clear register	3F00 4204h
208h	GICSS0_ECC_AGGR_AGGR_STATUS_SET	AGGR interrupt status set register	3F00 4208h
20Ch	GICSS0_ECC_AGGR_AGGR_STATUS_CLR	AGGR interrupt status clear register	3F00 420Ch

1 GICSS0_ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

GIC_ECC_AGGR_REV is shown in Figure 9-3 and described in Table 9-12.

Return to Summary Table.

IP revision register.

Table 9-11. GICSS0_ECC_AGGR_REV Instances

Instance	Physical Address
GICSS0_REGS	3F00 4000h

Figure 9-3. GICSS0_ECC_AGGR_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66A0EA00h																															

Table 9-13. GICSS0_ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66A0EA00h	TI internal data. Identifies revision of peripheral.

2 GICSS0_ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

GIC_ECC_AGGR_VECTOR is shown in Figure 9-4 and described in Table 9-14.

Return to Summary Table.

ECC vector register.

Table 9-14. GICSS0_ECC_AGGR_VECTOR Instances

Instance	Physical Address
GICSS0_REGS	3F00 4008h

Figure 9-4. GICSS0_ECC_AGGR_VECTOR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W1C-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1S-0h</td><td colspan="4">R-0h</td><td colspan="3">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

Table 9-16. GICSS0_ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

3 GICSS0_ECC_AGGR_STAT Register (Offset = Ch) [reset = 6h]

GIC_ECC_AGGR_STAT is shown in Figure 9-5 and described in Table 9-16.

Return to Summary Table.

Misc status register.

Table 9-17. GICSS0_ECC_AGGR_STAT Instances

Instance	Physical Address
GICSS0_REGS	3F00 400Ch

Figure 9-5. GICSS0_ECC_AGGR_STAT Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="21">RESERVED</td><td colspan="11">NUM_RAMS</td></tr>
<tr><td colspan="21">R-0h</td><td colspan="11">R-13h</td></tr>
</table>

Table 9-19. GICSS0_ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	6h	Indicates the number of RAMs serviced by the ECC aggregator

4 GICSS0_ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

GIC_ECC_AGGR_SEC_EOI_REG is shown in Figure 9-6 and described in Table 9-18.

Return to Summary Table.

EOI register. The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 9-20. GICSS0_ECC_AGGR_SEC_EOI_REG Instances

Instance	Physical Address
GICSS0_REGS	3F00 403Ch

Figure 9-6. GICSS0_ECC_AGGR_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
R-0h							R/W1S-0h

Table 9-22. GICSS0_ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	EOI value

5 GICSS0_ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

GIC_ECC_AGGR_SEC_STATUS_REG0 is shown in Figure 9-7 and described in Table 9-20.

Return to Summary Table.

SEC interrupt status register 0.

Table 9-23. GICSS0_ECC_AGGR_SEC_STATUS_REG0 Instances

Instance	Physical Address
GICSS0_REGS	3F00 4040h

Figure 9-7. GICSS0_ECC_AGGR_SEC_STATUS_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRITE_PEND</td><td>READ_PEND</td><td>EDC_CTRL_PEND</td><td>LPI_RAMECC_PEND</td><td>ITE_RAMECC_PEND</td><td>ICB_RAMECC_PEND</td></tr>
<tr><td colspan="2">R-0h</td><td>R/W1S-0h</td><td>R/W1S-0h</td><td>R/W1S-0h</td><td>R/W1S-0h</td><td>R/W1S-0h</td><td>R/W1S-0h</td></tr>
</table>

Table 9-25. GICSS0_ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	WRITE_PEND	R/W1S	0h	Interrupt pending status for write_pend
4	READ_PEND	R/W1S	0h	Interrupt pending status for read_pend
3	EDC_CTRL_PEND	R/W1S	0h	Interrupt pending status for edc_ctrl_pend
2	LPI_RAMECC_PEND	R/W1S	0h	Interrupt pending status for lpi_ramecc_pend
1	ITE_RAMECC_PEND	R/W1S	0h	Interrupt pending status for ite_ramecc_pend
0	ICB_RAMECC_PEND	R/W1S	0h	Interrupt pending status for icb_ramecc_pend

6 GICSS0_ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

GIC_ECC_AGGR_SEC_ENABLE_SET_REG0 is shown in Figure 9-8 and described in Table 9-22.

Return to Summary Table.

SEC interrupt enable set register 0.

Table 9-26. GICSS0_ECC_AGGR_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
GICSS0_REGS	3F00 4080h

Figure 9-8. GICSS0_ECC_AGGR_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		WRITE_ENABLE_SET	READ_ENABLE_SET	EDC_CTRL_ENABLE_SET	LPI_RAMECC_ENABLE_SET	ITE_RAMECC_ENABLE_SET	ICB_RAMECC_ENABLE_SET
R-0h		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

Table 9-28. GICSS0_ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	WRITE_ENABLE_SET	R/W1S	0h	Interrupt enable set for write_pend
4	READ_ENABLE_SET	R/W1S	0h	Interrupt enable set for read_pend
3	EDC_CTRL_ENABLE_SET	R/W1S	0h	Interrupt enable set for edc_ctrl_pend
2	LPI_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set for lpi_ramecc_pend
1	ITE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set for ite_ramecc_pend
0	ICB_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set for icb_ramecc_pend

7 GICSS0_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

GIC_ECC_AGGR_SEC_ENABLE_CLR_REG0 is shown in Figure 9-9 and described in Table 9-24.

Return to Summary Table.

SEC interrupt enable clear register 0.

Table 9-29. GICSS0_ECC_AGGR_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
GICSS0_REGS	3F00 40C0h

Figure 9-9. GICSS0_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		WRITE_ENABLE_CLR	READ_ENABLE_CLR	EDC_CTRL_ENABLE_CLR	LPI_RAMECC_ENABLE_CLR	ITE_RAMECC_ENABLE_CLR	ICB_RAMECC_ENABLE_CLR
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 9-31. GICSS0_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	WRITE_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for write_pend
4	READ_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for read_pend
3	EDC_CTRL_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for edc_ctrl_pend
2	LPI_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for lpi_ramecc_pend
1	ITE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for ite_ramecc_pend
0	ICB_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for icb_ramecc_pend

8 GICSS0_ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

GIC_ECC_AGGR_DED_EOI_REG is shown in Figure 9-10 and described in Table 9-26.

Return to Summary Table.

DED EOI register. The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 9-32. GICSS0_ECC_AGGR_DED_EOI_REG Instances

Instance	Physical Address
GICSS0_REGS	3F00 413Ch

Figure 9-10. GICSS0_ECC_AGGR_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
R-0h							R/W1S-0h

Table 9-34. GICSS0_ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	EOI value

9 GICSS0_ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

GIC_ECC_AGGR_DED_STATUS_REG0 is shown in Figure 9-11 and described in Table 9-28.

Return to Summary Table.

DED interrupt status register 0.

Table 9-35. GICSS0_ECC_AGGR_DED_STATUS_REG0 Instances

Instance	Physical Address
GICSS0_REGS	3F00 4140h

Figure 9-11. GICSS0_ECC_AGGR_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		WRITE_PEND	READ_PEND	EDC_CTRL_PEND	LPI_RAMECC_PEND	ITE_RAMECC_PEND	ICB_RAMECC_PEND
R-0h		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

Table 9-37. GICSS0_ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	WRITE_PEND	R/W1S	0h	Interrupt pending status for write_pend
4	READ_PEND	R/W1S	0h	Interrupt pending status for read_pend
3	EDC_CTRL_PEND	R/W1S	0h	Interrupt pending status for edc_ctrl_pend
2	LPI_RAMECC_PEND	R/W1S	0h	Interrupt pending status for lpi_ramecc_pend
1	ITE_RAMECC_PEND	R/W1S	0h	Interrupt pending status for ite_ramecc_pend
0	ICB_RAMECC_PEND	R/W1S	0h	Interrupt pending status for icb_ramecc_pend

10 GICSS0_ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

GIC_ECC_AGGR_DED_ENABLE_SET_REG0 is shown in Figure 9-12 and described in Table 9-30.

Return to Summary Table.

DED interrupt enable set register 0.

Table 9-38. GICSS0_ECC_AGGR_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
GICSS0_REGS	3F00 4180h

Figure 9-12. GICSS0_ECC_AGGR_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED		WRITE_ENABLE_SET	READ_ENABLE_SET	EDC_CTRL_ENABLE_SET	LPI_RAMECC_ENABLE_SET	ITE_RAMECC_ENABLE_SET	ICB_RAMECC_ENABLE_SET
R-0h		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

Table 9-40. GICSS0_ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	WRITE_ENABLE_SET	R/W1S	0h	Interrupt enable set for write_pend
4	READ_ENABLE_SET	R/W1S	0h	Interrupt enable set for read_pend
3	EDC_CTRL_ENABLE_SET	R/W1S	0h	Interrupt enable set for edc_ctrl_pend
2	LPI_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set for lpi_ramecc_pend
1	ITE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set for ite_ramecc_pend
0	ICB_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set for icb_ramecc_pend

11 GICSS0_ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

GIC_ECC_AGGR_DED_ENABLE_CLR_REG0 is shown in Figure 9-13 and described in Table 9-32.

Return to Summary Table.

DED interrupt enable clear register 0.

Table 9-41. GICSS0_ECC_AGGR_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
GICSS0_REGS	3F00 41C0h

Figure 9-13. GICSS0_ECC_AGGR_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED		WRITE_ENABLE_CLR	READ_ENABLE_CLR	EDC_CTRL_ENABLE_CLR	LPI_RAMECC_ENABLE_CLR	ITE_RAMECC_ENABLE_CLR	ICB_RAMECC_ENABLE_CLR
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 9-43. GICSS0_ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	WRITE_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for write_pend
4	READ_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for read_pend
3	EDC_CTRL_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for edc_ctrl_pend
2	LPI_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for lpi_ramecc_pend
1	ITE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for ite_ramecc_pend
0	ICB_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt enable clear for icb_ramecc_pend

12 GICSS0_ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

GIC_ECC_AGGR_AGGR_ENABLE_SET is shown in Figure 9-14 and described in Table 9-34.

Return to Summary Table.

AGGR interrupt enable set register.

Table 9-44. GICSS0_ECC_AGGR_AGGR_ENABLE_SET Instances

Instance	Physical Address
GICSS0_REGS	3F00 4200h

Figure 9-14. GICSS0_ECC_AGGR_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

Table 9-46. GICSS0_ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

13 GICSS0_ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

GIC_ECC_AGGR_AGGR_ENABLE_CLR is shown in Figure 9-15 and described in Table 9-36.

Return to Summary Table.

AGGR interrupt enable clear register.

Table 9-47. GICSS0_ECC_AGGR_AGGR_ENABLE_CLR Instances

Instance	Physical Address
GICSS0_REGS	3F00 4204h

Figure 9-15. GICSS0_ECC_AGGR_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

Table 9-49. GICSS0_ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

14 GICSS0_ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

GIC_ECC_AGGR_AGGR_STATUS_SET is shown in Figure 9-16 and described in Table 9-38.

Return to Summary Table.

AGGR interrupt status set register.

Table 9-50. GICSS0_ECC_AGGR_AGGR_STATUS_SET Instances

Instance	Physical Address
GICSS0_REGS	3F00 4208h

Figure 9-16. GICSS0_ECC_AGGR_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wincr-0h		R/Wincr-0h	

Table 9-52. GICSS0_ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

15 GICSS0_ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

GIC_ECC_AGGR_AGGR_STATUS_CLR is shown in Figure 9-17 and described in Table 9-40.

Return to Summary Table.

AGGR interrupt status clear register.

Table 9-53. GICSS0_ECC_AGGR_AGGR_STATUS_CLR Instances

Instance	Physical Address
GICSS0_REGS	3F00 420Ch

Figure 9-17. GICSS0_ECC_AGGR_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wdecr-0h		R/Wdecr-0h	

Table 9-55. GICSS0_ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

9.2.2 Other Interrupt Controllers

All other device interrupt controllers are described in their respective chapters and/or third party documentation.

9.3 Interrupt Routers

9.3.1 INTRTR Overview

The interrupt router (INTRTR) module provides a mechanism to mux *M* interrupt inputs to *N* interrupt outputs, where all *M* inputs are selectable to be driven per *N* ouput. There is one register per output (MUXCNTL_N) that controls the selection.

The user should take the following into account when programming the MUXCNTL_N register:

- Avoid programming this register when input interrupts are active. This could lead to spurious asynchronous output toggles which may lead to unpredictable behavior.

The recommended general programming sequence is as follows:

1. Disable interrupt by writing '0' to the INT_ENABLE bit field. Do not change mux control configuration settings (ENABLE bit field) at this time.
2. Change the mux control configuration settings. INT_ENABLE needs to remain '0' at this time.
3. Enable interrupt by writing '1' to INT_ENABLE. Do not change mux control configuration settings at this time.

9.3.2 INTRTR Integration

This section describes the INTRTR integration in the device, including information about clocks, resets, and hardware requests.

9.3.2.1 MCU_GPIOMUX_INTRTR0 Integration

Figure 9-18 shows the MCU_GPIOMUX_INTRTR0 integration.

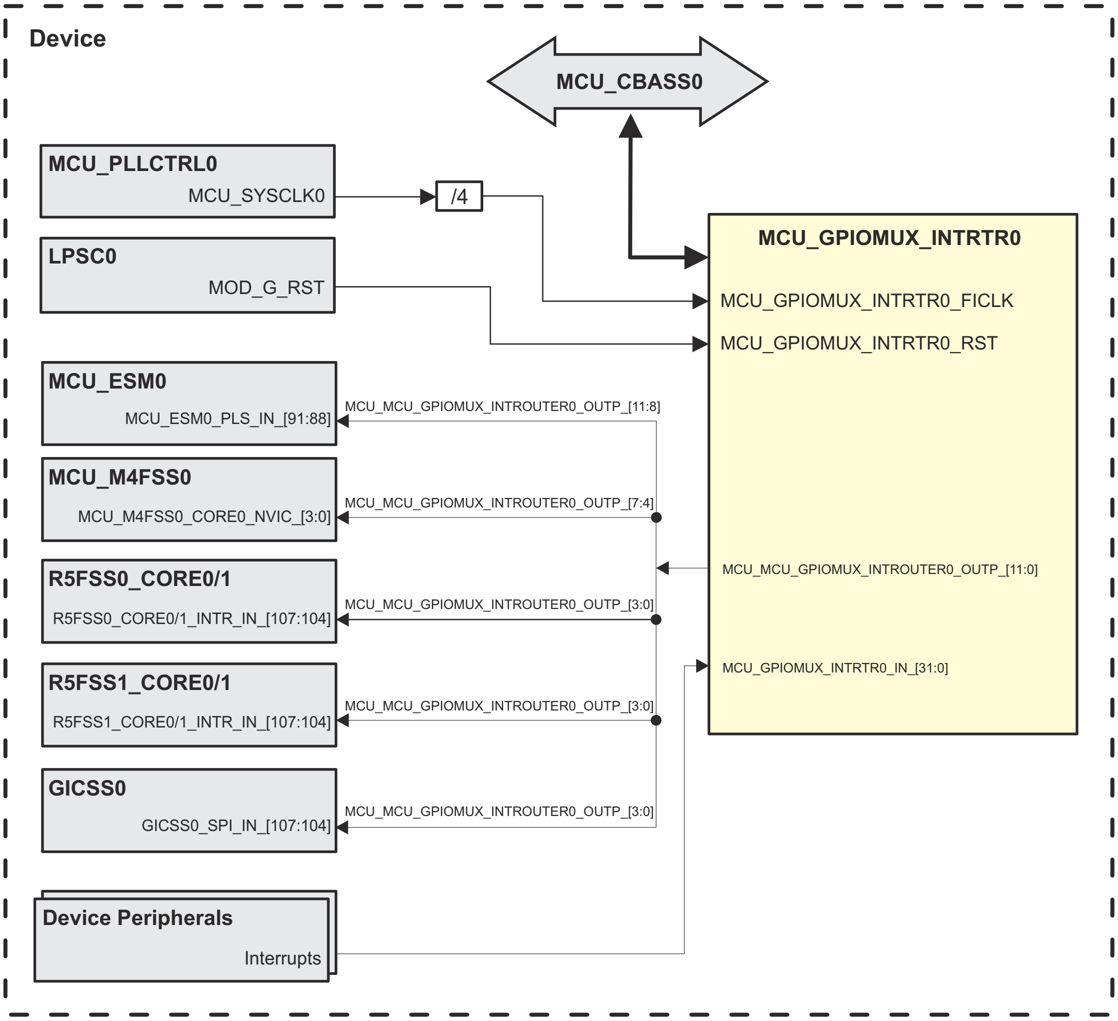

Figure 9-18. MCU_GPIOMUX_INTRTR0 Integration

Table 9-41 through Table 9-43 summarize the MCU_GPIOMUX_INTRTR0 integration.

Table 9-56. MCU_GPIOMUX_INTRTR0 Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_GPIOMUX_INTRTR0	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 9-57. MCU_GPIOMUX_INTRTR0 Clocks and Resets

Clocks				
Module Instance	Module Clock Input	Source Clock Signal	Source	Description

Table 9-57. MCU_GPIOMUX_INTRTR0 Clocks and Resets (continued)

MCU_GPIOMUX_INTRTR0	MCU_GPIOMUX_INTRTR0_FICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	Module functional and interface clock
		Resets		
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
MCU_GPIOMUX_INTRTR0	MCU_GPIOMUX_INTRTR0_RST	MOD_G_RST	LPSC0	Module hardware reset

Table 9-58. MCU_GPIOMUX_INTRTR0 Hardware Requests

		Interrupt Requests			
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
MCU_GPIOMUX_INTRTR0	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_[3:0]	GICSS0_SPI_IN_[107:104] R5FSS0_CORE0_INTR_IN_[107:104] R5FSS0_CORE1_INTR_IN_[107:104] R5FSS1_CORE0_INTR_IN_[107:104] R5FSS1_CORE1_INTR_IN_[107:104]	GICSS0 R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1	Module interrupt outputs [11:0]	Pulse
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_[7:4]	MCU_M4FSS0_CORE0_NVIC_IN_[3:0]	MCU_M4FSS0		
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_[11:8]	MCU_ESM0_PLS_IN_[91:88]	MCU_ESM0		

Note

Table 9-43 lists only the MCU_GPIOMUX_INTRTR0 interrupt outputs.

9.3.2.2 GPIOMUX_INTRTR0 Integration

Figure 9-19 shows the GPIOMUX_INTRTR0 integration.

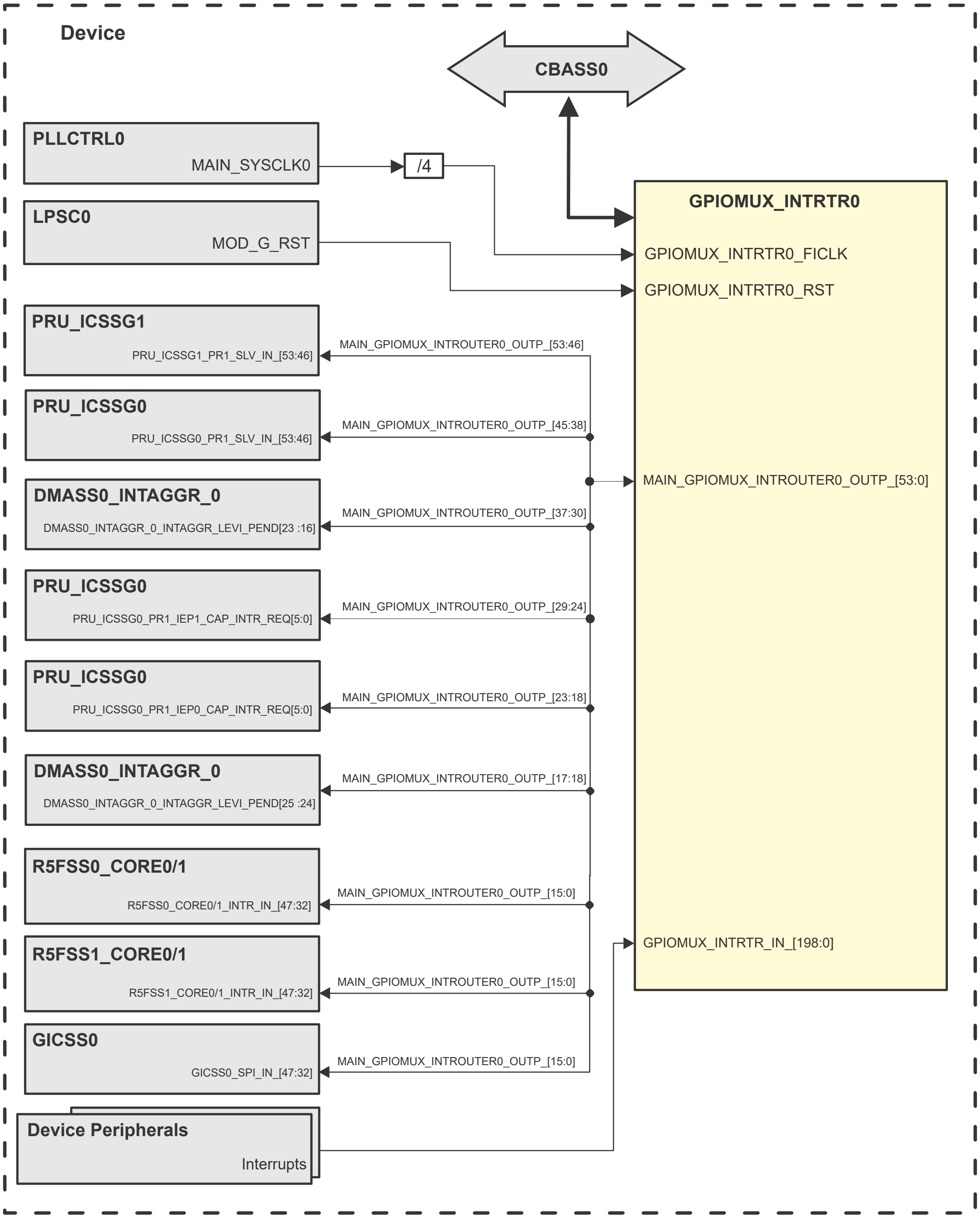

Figure 9-19. GPIOMUX_INTRTR0 Integration

Table 9-44 through Table 9-46 summarize the GPIOMUX_INTRTR0 integration.

Table 9-59. GPIOMUX_INTRTR0 Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
GPIOMUX_INTRTR0	PSC0	PD0	LPSC0	CBASS0

Table 9-60. GPIOMUX_INTRTR0 Clocks and Resets

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
GPIOMUX_INTRTR0	GPIOMUX_INTRTR0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	Module functional and interface clock
Resets				
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
GPIOMUX_INTRTR0	GPIOMUX_INTRTR0_RST	MOD_G_RST	LPSC0	Module hardware reset

Table 9-61. GPIOMUX_INTRTR0 Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
GPIOMUX_INTRTR0	MAIN_GPIOMUX_INTROUTER0_OUTP_[15:0]	GICSS0_SPI_IN_[47:32]	GICSS0	Module interrupt outputs [53:0]	Pulse
		R5FSS0_CORE0_INTR_IN_[47:32]	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_[47:32]	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_[47:32]	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_[47:32]	R5FSS1_CORE1		
	MAIN_GPIOMUX_INTROUTER0_OUTP_[17:16]	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND[25:24]	DMASS0_INTAGGR_0		
	MAIN_GPIOMUX_INTROUTER0_OUTP_[23:18]	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ[5:0]	PRU_ICSSG0		
	MAIN_GPIOMUX_INTROUTER0_OUTP_[29:24]	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ[5:0]	PRU_ICSSG0		
	MAIN_GPIOMUX_INTROUTER0_OUTP_[37:30]	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND[23:16]	DMASS0_INTAGGR_0		
	MAIN_GPIOMUX_INTROUTER0_OUTP_[45:38]	PRU_ICSSG0_PR1_SLV_IN_[53:46]	PRU_ICSSG0		
	MAIN_GPIOMUX_INTROUTER0_OUTP_[53:46]	PRU_ICSSG1_PR1_SLV_IN_[53:46]	PRU_ICSSG1		

Note

Table 9-46 lists only the GPIOMUX_INTRTR0 interrupt outputs.

9.4 Interrupt Sources

9.4.1 Interrupts (Inputs)

Table 9-62. Interrupts (Inputs)

Instance	Interrupt Input Line	Source Interrupt
PINFUNCTION_CPTS0_TS_COMPout	PINFUNCTION_CPTS0_TS_COMPOUT_CPTS0_TS_COMP_IN_0	CPTS0_CPTS_COMP_OUT_0
PINFUNCTION_CPTS0_TS_SYNCout	PINFUNCTION_CPTS0_TS_SYNCOUT_CPTS0_TS_SYNC_IN_0	CPTS0_CPTS_SYNC_OUT_0
PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPout	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPOUT_CP_GEMAC_CPTS0_TS_COMP_IN_0	CPSW0_CPTS_COMP_OUT_0
PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCout	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCOUT_CP_GEMAC_CPTS0_TS_SYNC_IN_0	CPSW0_CPTS_SYNC_OUT_0
PINFUNCTION_PRG0_IEP0_EDC_SYNC_OUT0out	PINFUNCTION_PRG0_IEP0_EDC_SYNC_OUT0OUT_PRG0_IEP0_EDC_SYNC_OUT0_IN_0	PRU_ICSSG0_PR1_EDC0_SYNC0_OUT_OUT_0
PINFUNCTION_PRG0_IEP0_EDC_SYNC_OUT1out	PINFUNCTION_PRG0_IEP0_EDC_SYNC_OUT1OUT_PRG0_IEP0_EDC_SYNC_OUT1_IN_0	PRU_ICSSG0_PR1_EDC0_SYNC1_OUT_OUT_0
PINFUNCTION_PRG0_IEP1_EDC_SYNC_OUT0out	PINFUNCTION_PRG0_IEP1_EDC_SYNC_OUT0OUT_PRG0_IEP1_EDC_SYNC_OUT0_IN_0	PRU_ICSSG0_PR1_EDC1_SYNC0_OUT_OUT_0
PINFUNCTION_PRG0_IEP1_EDC_SYNC_OUT1out	PINFUNCTION_PRG0_IEP1_EDC_SYNC_OUT1OUT_PRG0_IEP1_EDC_SYNC_OUT1_IN_0	PRU_ICSSG0_PR1_EDC1_SYNC1_OUT_OUT_0
PINFUNCTION_PRG1_IEP0_EDC_SYNC_OUT0out	PINFUNCTION_PRG1_IEP0_EDC_SYNC_OUT0OUT_PRG1_IEP0_EDC_SYNC_OUT0_IN_0	PRU_ICSSG1_PR1_EDC0_SYNC0_OUT_OUT_0
PINFUNCTION_PRG1_IEP0_EDC_SYNC_OUT1out	PINFUNCTION_PRG1_IEP0_EDC_SYNC_OUT1OUT_PRG1_IEP0_EDC_SYNC_OUT1_IN_0	PRU_ICSSG1_PR1_EDC0_SYNC1_OUT_OUT_0
PINFUNCTION_PRG1_IEP1_EDC_SYNC_OUT0out	PINFUNCTION_PRG1_IEP1_EDC_SYNC_OUT0OUT_PRG1_IEP1_EDC_SYNC_OUT0_IN_0	PRU_ICSSG1_PR1_EDC1_SYNC0_OUT_OUT_0
PINFUNCTION_PRG1_IEP1_EDC_SYNC_OUT1out	PINFUNCTION_PRG1_IEP1_EDC_SYNC_OUT1OUT_PRG1_IEP1_EDC_SYNC_OUT1_IN_0	PRU_ICSSG1_PR1_EDC1_SYNC1_OUT_OUT_0
PINFUNCTION_SYNC0_OUTout	PINFUNCTION_SYNC0_OUTOUT_SYNC0_OUT_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_24
PINFUNCTION_SYNC1_OUTout	PINFUNCTION_SYNC1_OUTOUT_SYNC1_OUT_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_25
PINFUNCTION_SYNC2_OUTout	PINFUNCTION_SYNC2_OUTOUT_SYNC2_OUT_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_26
PINFUNCTION_SYNC3_OUTout	PINFUNCTION_SYNC3_OUTOUT_SYNC3_OUT_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_27
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_IN_IN_0	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_1	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_1
	CMP_EVENT_INTROUTER0_IN_IN_2	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_2
	CMP_EVENT_INTROUTER0_IN_IN_3	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_3
	CMP_EVENT_INTROUTER0_IN_IN_4	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_4
	CMP_EVENT_INTROUTER0_IN_IN_5	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_5
	CMP_EVENT_INTROUTER0_IN_IN_6	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_6
	CMP_EVENT_INTROUTER0_IN_IN_7	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_7
	CMP_EVENT_INTROUTER0_IN_IN_8	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_9	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_1
	CMP_EVENT_INTROUTER0_IN_IN_10	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_2
	CMP_EVENT_INTROUTER0_IN_IN_11	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_3
	CMP_EVENT_INTROUTER0_IN_IN_12	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_4
	CMP_EVENT_INTROUTER0_IN_IN_13	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_5
	CMP_EVENT_INTROUTER0_IN_IN_14	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_6
	CMP_EVENT_INTROUTER0_IN_IN_15	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_7
	CMP_EVENT_INTROUTER0_IN_IN_16	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_IN_IN_17	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_1
	CMP_EVENT_INTROUTER0_IN_IN_18	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_2
	CMP_EVENT_INTROUTER0_IN_IN_19	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_3
	CMP_EVENT_INTROUTER0_IN_IN_20	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_4
	CMP_EVENT_INTROUTER0_IN_IN_21	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_5
	CMP_EVENT_INTROUTER0_IN_IN_22	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_6
	CMP_EVENT_INTROUTER0_IN_IN_23	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_7
	CMP_EVENT_INTROUTER0_IN_IN_24	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_8
	CMP_EVENT_INTROUTER0_IN_IN_25	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_9
	CMP_EVENT_INTROUTER0_IN_IN_26	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_10
	CMP_EVENT_INTROUTER0_IN_IN_27	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_11
	CMP_EVENT_INTROUTER0_IN_IN_28	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_12
	CMP_EVENT_INTROUTER0_IN_IN_29	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_13
	CMP_EVENT_INTROUTER0_IN_IN_30	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_14
	CMP_EVENT_INTROUTER0_IN_IN_31	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_15
	CMP_EVENT_INTROUTER0_IN_IN_32	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_33	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_1
	CMP_EVENT_INTROUTER0_IN_IN_34	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_2
	CMP_EVENT_INTROUTER0_IN_IN_35	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_3
	CMP_EVENT_INTROUTER0_IN_IN_36	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_4
	CMP_EVENT_INTROUTER0_IN_IN_37	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_5
	CMP_EVENT_INTROUTER0_IN_IN_38	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_6
	CMP_EVENT_INTROUTER0_IN_IN_39	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_7
	CMP_EVENT_INTROUTER0_IN_IN_40	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_8
	CMP_EVENT_INTROUTER0_IN_IN_41	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_9
	CMP_EVENT_INTROUTER0_IN_IN_42	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_10
	CMP_EVENT_INTROUTER0_IN_IN_43	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_11
	CMP_EVENT_INTROUTER0_IN_IN_44	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_12
	CMP_EVENT_INTROUTER0_IN_IN_45	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_13
	CMP_EVENT_INTROUTER0_IN_IN_46	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_14
	CMP_EVENT_INTROUTER0_IN_IN_47	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_15
	CMP_EVENT_INTROUTER0_IN_IN_48	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_49	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_1

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_IN_IN_50	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_2
	CMP_EVENT_INTROUTER0_IN_IN_51	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_3
	CMP_EVENT_INTROUTER0_IN_IN_52	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_4
	CMP_EVENT_INTROUTER0_IN_IN_53	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_5
	CMP_EVENT_INTROUTER0_IN_IN_54	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_6
	CMP_EVENT_INTROUTER0_IN_IN_55	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_7
	CMP_EVENT_INTROUTER0_IN_IN_56	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_8
	CMP_EVENT_INTROUTER0_IN_IN_57	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_9
	CMP_EVENT_INTROUTER0_IN_IN_58	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_10
	CMP_EVENT_INTROUTER0_IN_IN_59	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_11
	CMP_EVENT_INTROUTER0_IN_IN_60	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_12
	CMP_EVENT_INTROUTER0_IN_IN_61	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_13
	CMP_EVENT_INTROUTER0_IN_IN_62	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_14
	CMP_EVENT_INTROUTER0_IN_IN_63	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_15
	CMP_EVENT_INTROUTER0_IN_IN_64	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_65	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_1
	CMP_EVENT_INTROUTER0_IN_IN_66	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_2
	CMP_EVENT_INTROUTER0_IN_IN_67	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_3
	CMP_EVENT_INTROUTER0_IN_IN_68	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_4
	CMP_EVENT_INTROUTER0_IN_IN_69	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_5
	CMP_EVENT_INTROUTER0_IN_IN_70	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_6
	CMP_EVENT_INTROUTER0_IN_IN_71	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_7
	CMP_EVENT_INTROUTER0_IN_IN_72	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_8
	CMP_EVENT_INTROUTER0_IN_IN_73	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_9
	CMP_EVENT_INTROUTER0_IN_IN_74	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_10
	CMP_EVENT_INTROUTER0_IN_IN_75	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_11
	CMP_EVENT_INTROUTER0_IN_IN_76	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_12
	CMP_EVENT_INTROUTER0_IN_IN_77	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_13
	CMP_EVENT_INTROUTER0_IN_IN_78	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_14
	CMP_EVENT_INTROUTER0_IN_IN_79	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_15
	CMP_EVENT_INTROUTER0_IN_IN_80	CPSW0_CPTS_COMP_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_81	PCIE0_PCIE_CPTS_COMP_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_82	CPTS0_CPTS_COMP_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_0	GPIO0_GPIO_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_1	GPIO0_GPIO_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_2	GPIO0_GPIO_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_3	GPIO0_GPIO_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_4	GPIO0_GPIO_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_5	GPIO0_GPIO_OUT_5
	MAIN_GPIOMUX_INTROUTER0_IN_IN_6	GPIO0_GPIO_OUT_6
	MAIN_GPIOMUX_INTROUTER0_IN_IN_7	GPIO0_GPIO_OUT_7
	MAIN_GPIOMUX_INTROUTER0_IN_IN_8	GPIO0_GPIO_OUT_8
	MAIN_GPIOMUX_INTROUTER0_IN_IN_9	GPIO0_GPIO_OUT_9
	MAIN_GPIOMUX_INTROUTER0_IN_IN_10	GPIO0_GPIO_OUT_10
	MAIN_GPIOMUX_INTROUTER0_IN_IN_11	GPIO0_GPIO_OUT_11
	MAIN_GPIOMUX_INTROUTER0_IN_IN_12	GPIO0_GPIO_OUT_12
	MAIN_GPIOMUX_INTROUTER0_IN_IN_13	GPIO0_GPIO_OUT_13
	MAIN_GPIOMUX_INTROUTER0_IN_IN_14	GPIO0_GPIO_OUT_14
	MAIN_GPIOMUX_INTROUTER0_IN_IN_15	GPIO0_GPIO_OUT_15
	MAIN_GPIOMUX_INTROUTER0_IN_IN_16	GPIO0_GPIO_OUT_16
	MAIN_GPIOMUX_INTROUTER0_IN_IN_17	GPIO0_GPIO_OUT_17
	MAIN_GPIOMUX_INTROUTER0_IN_IN_18	GPIO0_GPIO_OUT_18
	MAIN_GPIOMUX_INTROUTER0_IN_IN_19	GPIO0_GPIO_OUT_19
	MAIN_GPIOMUX_INTROUTER0_IN_IN_20	GPIO0_GPIO_OUT_20
	MAIN_GPIOMUX_INTROUTER0_IN_IN_21	GPIO0_GPIO_OUT_21
	MAIN_GPIOMUX_INTROUTER0_IN_IN_22	GPIO0_GPIO_OUT_22
	MAIN_GPIOMUX_INTROUTER0_IN_IN_23	GPIO0_GPIO_OUT_23
	MAIN_GPIOMUX_INTROUTER0_IN_IN_24	GPIO0_GPIO_OUT_24
	MAIN_GPIOMUX_INTROUTER0_IN_IN_25	GPIO0_GPIO_OUT_25
	MAIN_GPIOMUX_INTROUTER0_IN_IN_26	GPIO0_GPIO_OUT_26
	MAIN_GPIOMUX_INTROUTER0_IN_IN_27	GPIO0_GPIO_OUT_27
	MAIN_GPIOMUX_INTROUTER0_IN_IN_28	GPIO0_GPIO_OUT_28
	MAIN_GPIOMUX_INTROUTER0_IN_IN_29	GPIO0_GPIO_OUT_29
	MAIN_GPIOMUX_INTROUTER0_IN_IN_30	GPIO0_GPIO_OUT_30
	MAIN_GPIOMUX_INTROUTER0_IN_IN_31	GPIO0_GPIO_OUT_31
	MAIN_GPIOMUX_INTROUTER0_IN_IN_32	GPIO0_GPIO_OUT_32

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_33	GPIO0_GPIO_OUT_33
	MAIN_GPIOMUX_INTROUTER0_IN_IN_34	GPIO0_GPIO_OUT_34
	MAIN_GPIOMUX_INTROUTER0_IN_IN_35	GPIO0_GPIO_OUT_35
	MAIN_GPIOMUX_INTROUTER0_IN_IN_36	GPIO0_GPIO_OUT_36
	MAIN_GPIOMUX_INTROUTER0_IN_IN_37	GPIO0_GPIO_OUT_37
	MAIN_GPIOMUX_INTROUTER0_IN_IN_38	GPIO0_GPIO_OUT_38
	MAIN_GPIOMUX_INTROUTER0_IN_IN_39	GPIO0_GPIO_OUT_39
	MAIN_GPIOMUX_INTROUTER0_IN_IN_40	GPIO0_GPIO_OUT_40
	MAIN_GPIOMUX_INTROUTER0_IN_IN_41	GPIO0_GPIO_OUT_41
	MAIN_GPIOMUX_INTROUTER0_IN_IN_42	GPIO0_GPIO_OUT_42
	MAIN_GPIOMUX_INTROUTER0_IN_IN_43	GPIO0_GPIO_OUT_43
	MAIN_GPIOMUX_INTROUTER0_IN_IN_44	GPIO0_GPIO_OUT_44
	MAIN_GPIOMUX_INTROUTER0_IN_IN_45	GPIO0_GPIO_OUT_45
	MAIN_GPIOMUX_INTROUTER0_IN_IN_46	GPIO0_GPIO_OUT_46
	MAIN_GPIOMUX_INTROUTER0_IN_IN_47	GPIO0_GPIO_OUT_47
	MAIN_GPIOMUX_INTROUTER0_IN_IN_48	GPIO0_GPIO_OUT_48
	MAIN_GPIOMUX_INTROUTER0_IN_IN_49	GPIO0_GPIO_OUT_49
	MAIN_GPIOMUX_INTROUTER0_IN_IN_50	GPIO0_GPIO_OUT_50
	MAIN_GPIOMUX_INTROUTER0_IN_IN_51	GPIO0_GPIO_OUT_51
	MAIN_GPIOMUX_INTROUTER0_IN_IN_52	GPIO0_GPIO_OUT_52
	MAIN_GPIOMUX_INTROUTER0_IN_IN_53	GPIO0_GPIO_OUT_53
	MAIN_GPIOMUX_INTROUTER0_IN_IN_54	GPIO0_GPIO_OUT_54
	MAIN_GPIOMUX_INTROUTER0_IN_IN_55	GPIO0_GPIO_OUT_55
	MAIN_GPIOMUX_INTROUTER0_IN_IN_56	GPIO0_GPIO_OUT_56
	MAIN_GPIOMUX_INTROUTER0_IN_IN_57	GPIO0_GPIO_OUT_57
	MAIN_GPIOMUX_INTROUTER0_IN_IN_58	GPIO0_GPIO_OUT_58
	MAIN_GPIOMUX_INTROUTER0_IN_IN_59	GPIO0_GPIO_OUT_59
	MAIN_GPIOMUX_INTROUTER0_IN_IN_60	GPIO0_GPIO_OUT_60
	MAIN_GPIOMUX_INTROUTER0_IN_IN_61	GPIO0_GPIO_OUT_61
	MAIN_GPIOMUX_INTROUTER0_IN_IN_62	GPIO0_GPIO_OUT_62
	MAIN_GPIOMUX_INTROUTER0_IN_IN_63	GPIO0_GPIO_OUT_63
	MAIN_GPIOMUX_INTROUTER0_IN_IN_64	GPIO0_GPIO_OUT_64
	MAIN_GPIOMUX_INTROUTER0_IN_IN_65	GPIO0_GPIO_OUT_65

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_66	GPIO0_GPIO_OUT_66
	MAIN_GPIOMUX_INTROUTER0_IN_IN_67	GPIO0_GPIO_OUT_67
	MAIN_GPIOMUX_INTROUTER0_IN_IN_68	GPIO0_GPIO_OUT_68
	MAIN_GPIOMUX_INTROUTER0_IN_IN_69	GPIO0_GPIO_OUT_69
	MAIN_GPIOMUX_INTROUTER0_IN_IN_70	GPIO0_GPIO_OUT_70
	MAIN_GPIOMUX_INTROUTER0_IN_IN_71	GPIO0_GPIO_OUT_71
	MAIN_GPIOMUX_INTROUTER0_IN_IN_72	GPIO0_GPIO_OUT_72
	MAIN_GPIOMUX_INTROUTER0_IN_IN_73	GPIO0_GPIO_OUT_73
	MAIN_GPIOMUX_INTROUTER0_IN_IN_74	GPIO0_GPIO_OUT_74
	MAIN_GPIOMUX_INTROUTER0_IN_IN_75	GPIO0_GPIO_OUT_75
	MAIN_GPIOMUX_INTROUTER0_IN_IN_76	GPIO0_GPIO_OUT_76
	MAIN_GPIOMUX_INTROUTER0_IN_IN_77	GPIO0_GPIO_OUT_77
	MAIN_GPIOMUX_INTROUTER0_IN_IN_78	GPIO0_GPIO_OUT_78
	MAIN_GPIOMUX_INTROUTER0_IN_IN_79	GPIO0_GPIO_OUT_79
	MAIN_GPIOMUX_INTROUTER0_IN_IN_80	GPIO0_GPIO_OUT_80
	MAIN_GPIOMUX_INTROUTER0_IN_IN_81	GPIO0_GPIO_OUT_81
	MAIN_GPIOMUX_INTROUTER0_IN_IN_82	GPIO0_GPIO_OUT_82
	MAIN_GPIOMUX_INTROUTER0_IN_IN_83	GPIO0_GPIO_OUT_83
	MAIN_GPIOMUX_INTROUTER0_IN_IN_84	GPIO0_GPIO_OUT_84
	MAIN_GPIOMUX_INTROUTER0_IN_IN_85	GPIO0_GPIO_OUT_85
	MAIN_GPIOMUX_INTROUTER0_IN_IN_86	GPIO0_GPIO_OUT_86
	MAIN_GPIOMUX_INTROUTER0_IN_IN_87	GPIO0_GPIO_OUT_87
	MAIN_GPIOMUX_INTROUTER0_IN_IN_88	GPIO0_GPIO_OUT_88
	MAIN_GPIOMUX_INTROUTER0_IN_IN_89	GPIO0_GPIO_OUT_89
	MAIN_GPIOMUX_INTROUTER0_IN_IN_90	GPIO1_GPIO_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_91	GPIO1_GPIO_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_92	GPIO1_GPIO_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_93	GPIO1_GPIO_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_94	GPIO1_GPIO_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_95	GPIO1_GPIO_OUT_5
	MAIN_GPIOMUX_INTROUTER0_IN_IN_96	GPIO1_GPIO_OUT_6
	MAIN_GPIOMUX_INTROUTER0_IN_IN_97	GPIO1_GPIO_OUT_7
	MAIN_GPIOMUX_INTROUTER0_IN_IN_98	GPIO1_GPIO_OUT_8

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_99	GPIO1_GPIO_OUT_9
	MAIN_GPIOMUX_INTROUTER0_IN_IN_100	GPIO1_GPIO_OUT_10
	MAIN_GPIOMUX_INTROUTER0_IN_IN_101	GPIO1_GPIO_OUT_11
	MAIN_GPIOMUX_INTROUTER0_IN_IN_102	GPIO1_GPIO_OUT_12
	MAIN_GPIOMUX_INTROUTER0_IN_IN_103	GPIO1_GPIO_OUT_13
	MAIN_GPIOMUX_INTROUTER0_IN_IN_104	GPIO1_GPIO_OUT_14
	MAIN_GPIOMUX_INTROUTER0_IN_IN_105	GPIO1_GPIO_OUT_15
	MAIN_GPIOMUX_INTROUTER0_IN_IN_106	GPIO1_GPIO_OUT_16
	MAIN_GPIOMUX_INTROUTER0_IN_IN_107	GPIO1_GPIO_OUT_17
	MAIN_GPIOMUX_INTROUTER0_IN_IN_108	GPIO1_GPIO_OUT_18
	MAIN_GPIOMUX_INTROUTER0_IN_IN_109	GPIO1_GPIO_OUT_19
	MAIN_GPIOMUX_INTROUTER0_IN_IN_110	GPIO1_GPIO_OUT_20
	MAIN_GPIOMUX_INTROUTER0_IN_IN_111	GPIO1_GPIO_OUT_21
	MAIN_GPIOMUX_INTROUTER0_IN_IN_112	GPIO1_GPIO_OUT_22
	MAIN_GPIOMUX_INTROUTER0_IN_IN_113	GPIO1_GPIO_OUT_23
	MAIN_GPIOMUX_INTROUTER0_IN_IN_114	GPIO1_GPIO_OUT_24
	MAIN_GPIOMUX_INTROUTER0_IN_IN_115	GPIO1_GPIO_OUT_25
	MAIN_GPIOMUX_INTROUTER0_IN_IN_116	GPIO1_GPIO_OUT_26
	MAIN_GPIOMUX_INTROUTER0_IN_IN_117	GPIO1_GPIO_OUT_27
	MAIN_GPIOMUX_INTROUTER0_IN_IN_118	GPIO1_GPIO_OUT_28
	MAIN_GPIOMUX_INTROUTER0_IN_IN_119	GPIO1_GPIO_OUT_29
	MAIN_GPIOMUX_INTROUTER0_IN_IN_120	GPIO1_GPIO_OUT_30
	MAIN_GPIOMUX_INTROUTER0_IN_IN_121	GPIO1_GPIO_OUT_31
	MAIN_GPIOMUX_INTROUTER0_IN_IN_122	GPIO1_GPIO_OUT_32
	MAIN_GPIOMUX_INTROUTER0_IN_IN_123	GPIO1_GPIO_OUT_33
	MAIN_GPIOMUX_INTROUTER0_IN_IN_124	GPIO1_GPIO_OUT_34
	MAIN_GPIOMUX_INTROUTER0_IN_IN_125	GPIO1_GPIO_OUT_35
	MAIN_GPIOMUX_INTROUTER0_IN_IN_126	GPIO1_GPIO_OUT_36
	MAIN_GPIOMUX_INTROUTER0_IN_IN_127	GPIO1_GPIO_OUT_37
	MAIN_GPIOMUX_INTROUTER0_IN_IN_128	GPIO1_GPIO_OUT_38
	MAIN_GPIOMUX_INTROUTER0_IN_IN_129	GPIO1_GPIO_OUT_39
	MAIN_GPIOMUX_INTROUTER0_IN_IN_130	GPIO1_GPIO_OUT_40
	MAIN_GPIOMUX_INTROUTER0_IN_IN_131	GPIO1_GPIO_OUT_41

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_132	GPIO1_GPIO_OUT_42
	MAIN_GPIOMUX_INTROUTER0_IN_IN_133	GPIO1_GPIO_OUT_43
	MAIN_GPIOMUX_INTROUTER0_IN_IN_134	GPIO1_GPIO_OUT_44
	MAIN_GPIOMUX_INTROUTER0_IN_IN_135	GPIO1_GPIO_OUT_45
	MAIN_GPIOMUX_INTROUTER0_IN_IN_136	GPIO1_GPIO_OUT_46
	MAIN_GPIOMUX_INTROUTER0_IN_IN_137	GPIO1_GPIO_OUT_47
	MAIN_GPIOMUX_INTROUTER0_IN_IN_138	GPIO1_GPIO_OUT_48
	MAIN_GPIOMUX_INTROUTER0_IN_IN_139	GPIO1_GPIO_OUT_49
	MAIN_GPIOMUX_INTROUTER0_IN_IN_140	GPIO1_GPIO_OUT_50
	MAIN_GPIOMUX_INTROUTER0_IN_IN_141	GPIO1_GPIO_OUT_51
	MAIN_GPIOMUX_INTROUTER0_IN_IN_142	GPIO1_GPIO_OUT_52
	MAIN_GPIOMUX_INTROUTER0_IN_IN_143	GPIO1_GPIO_OUT_53
	MAIN_GPIOMUX_INTROUTER0_IN_IN_144	GPIO1_GPIO_OUT_54
	MAIN_GPIOMUX_INTROUTER0_IN_IN_145	GPIO1_GPIO_OUT_55
	MAIN_GPIOMUX_INTROUTER0_IN_IN_146	GPIO1_GPIO_OUT_56
	MAIN_GPIOMUX_INTROUTER0_IN_IN_147	GPIO1_GPIO_OUT_57
	MAIN_GPIOMUX_INTROUTER0_IN_IN_148	GPIO1_GPIO_OUT_58
	MAIN_GPIOMUX_INTROUTER0_IN_IN_149	GPIO1_GPIO_OUT_59
	MAIN_GPIOMUX_INTROUTER0_IN_IN_150	GPIO1_GPIO_OUT_60
	MAIN_GPIOMUX_INTROUTER0_IN_IN_151	GPIO1_GPIO_OUT_61
	MAIN_GPIOMUX_INTROUTER0_IN_IN_152	GPIO1_GPIO_OUT_62
	MAIN_GPIOMUX_INTROUTER0_IN_IN_153	GPIO1_GPIO_OUT_63
	MAIN_GPIOMUX_INTROUTER0_IN_IN_154	GPIO1_GPIO_OUT_64
	MAIN_GPIOMUX_INTROUTER0_IN_IN_155	GPIO1_GPIO_OUT_65
	MAIN_GPIOMUX_INTROUTER0_IN_IN_156	GPIO1_GPIO_OUT_66
	MAIN_GPIOMUX_INTROUTER0_IN_IN_157	GPIO1_GPIO_OUT_67
	MAIN_GPIOMUX_INTROUTER0_IN_IN_158	GPIO1_GPIO_OUT_68
	MAIN_GPIOMUX_INTROUTER0_IN_IN_159	GPIO1_GPIO_OUT_69
	MAIN_GPIOMUX_INTROUTER0_IN_IN_160	GPIO1_GPIO_OUT_70
	MAIN_GPIOMUX_INTROUTER0_IN_IN_161	GPIO1_GPIO_OUT_71
	MAIN_GPIOMUX_INTROUTER0_IN_IN_162	GPIO1_GPIO_OUT_72
	MAIN_GPIOMUX_INTROUTER0_IN_IN_163	GPIO1_GPIO_OUT_73
	MAIN_GPIOMUX_INTROUTER0_IN_IN_164	GPIO1_GPIO_OUT_74

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_165	GPIO1_GPIO_OUT_75
	MAIN_GPIOMUX_INTROUTER0_IN_IN_166	GPIO1_GPIO_OUT_76
	MAIN_GPIOMUX_INTROUTER0_IN_IN_167	GPIO1_GPIO_OUT_77
	MAIN_GPIOMUX_INTROUTER0_IN_IN_168	GPIO1_GPIO_OUT_78
	MAIN_GPIOMUX_INTROUTER0_IN_IN_169	GPIO1_GPIO_OUT_79
	MAIN_GPIOMUX_INTROUTER0_IN_IN_170	GPIO1_GPIO_OUT_80
	MAIN_GPIOMUX_INTROUTER0_IN_IN_171	GPIO1_GPIO_OUT_81
	MAIN_GPIOMUX_INTROUTER0_IN_IN_172	GPIO1_GPIO_OUT_82
	MAIN_GPIOMUX_INTROUTER0_IN_IN_173	GPIO1_GPIO_OUT_83
	MAIN_GPIOMUX_INTROUTER0_IN_IN_174	GPIO1_GPIO_OUT_84
	MAIN_GPIOMUX_INTROUTER0_IN_IN_175	GPIO1_GPIO_OUT_85
	MAIN_GPIOMUX_INTROUTER0_IN_IN_176	GPIO1_GPIO_OUT_86
	MAIN_GPIOMUX_INTROUTER0_IN_IN_177	GPIO1_GPIO_OUT_87
	MAIN_GPIOMUX_INTROUTER0_IN_IN_178	GPIO1_GPIO_OUT_88
	MAIN_GPIOMUX_INTROUTER0_IN_IN_179	GPIO1_GPIO_OUT_89
	MAIN_GPIOMUX_INTROUTER0_IN_IN_180	GPIO1_GPIO_BANK_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_181	GPIO1_GPIO_BANK_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_182	GPIO1_GPIO_BANK_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_183	GPIO1_GPIO_BANK_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_184	GPIO1_GPIO_BANK_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_185	GPIO1_GPIO_BANK_OUT_5
	MAIN_GPIOMUX_INTROUTER0_IN_IN_186	GPIO1_GPIO_BANK_OUT_6
	MAIN_GPIOMUX_INTROUTER0_IN_IN_187	GPIO1_GPIO_BANK_OUT_7
	MAIN_GPIOMUX_INTROUTER0_IN_IN_188	GPIO1_GPIO_BANK_OUT_8
	MAIN_GPIOMUX_INTROUTER0_IN_IN_190	GPIO0_GPIO_BANK_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_191	GPIO0_GPIO_BANK_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_192	GPIO0_GPIO_BANK_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_193	GPIO0_GPIO_BANK_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_194	GPIO0_GPIO_BANK_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_195	GPIO0_GPIO_BANK_OUT_5
	MAIN_GPIOMUX_INTROUTER0_IN_IN_196	GPIO0_GPIO_BANK_OUT_6
	MAIN_GPIOMUX_INTROUTER0_IN_IN_197	GPIO0_GPIO_BANK_OUT_7
	MAIN_GPIOMUX_INTROUTER0_IN_IN_198	GPIO0_GPIO_BANK_OUT_8

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_MCU_GPIOMUX_INTROUTER0	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_0	MCU_GPIO0_GPIO_OUT_0
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_1	MCU_GPIO0_GPIO_OUT_1
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_2	MCU_GPIO0_GPIO_OUT_2
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_3	MCU_GPIO0_GPIO_OUT_3
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_4	MCU_GPIO0_GPIO_OUT_4
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_5	MCU_GPIO0_GPIO_OUT_5
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_6	MCU_GPIO0_GPIO_OUT_6
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_7	MCU_GPIO0_GPIO_OUT_7
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_8	MCU_GPIO0_GPIO_OUT_8
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_9	MCU_GPIO0_GPIO_OUT_9
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_10	MCU_GPIO0_GPIO_OUT_10
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_11	MCU_GPIO0_GPIO_OUT_11
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_12	MCU_GPIO0_GPIO_OUT_12
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_13	MCU_GPIO0_GPIO_OUT_13
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_14	MCU_GPIO0_GPIO_OUT_14
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_15	MCU_GPIO0_GPIO_OUT_15
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_16	MCU_GPIO0_GPIO_OUT_16
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_17	MCU_GPIO0_GPIO_OUT_17
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_18	MCU_GPIO0_GPIO_OUT_18
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_19	MCU_GPIO0_GPIO_OUT_19
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_20	MCU_GPIO0_GPIO_OUT_20
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_21	MCU_GPIO0_GPIO_OUT_21
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_22	MCU_GPIO0_GPIO_OUT_22
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_23	MCU_GPIO0_GPIO_OUT_23
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_24	MCU_GPIO0_GPIO_OUT_24
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_25	MCU_GPIO0_GPIO_OUT_25
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_26	MCU_GPIO0_GPIO_OUT_26
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_27	MCU_GPIO0_GPIO_OUT_27
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_28	MCU_GPIO0_GPIO_OUT_28
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_29	MCU_GPIO0_GPIO_OUT_29
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_30	MCU_GPIO0_GPIO_BANK_OUT_0
	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_31	MCU_GPIO0_GPIO_BANK_OUT_1
TIMESYNC_EVENT_INTROUTER0	TIMESYNC_EVENT_INTROUTER0_IN_IN_0	TIMER0_TIMER_PWM_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
TIMESYNC_EVENT_INTROUTER0	TIMESYNC_EVENT_INTROUTER0_IN_IN_1	TIMER1_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_2	TIMER2_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_3	TIMER3_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_4	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN0IN_PRG0_IEP0_EDC_LATCH_IN0_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_5	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN1IN_PRG0_IEP0_EDC_LATCH_IN1_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_6	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN0IN_PRG0_IEP1_EDC_LATCH_IN0_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_7	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN1IN_PRG0_IEP1_EDC_LATCH_IN1_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_8	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN0IN_PRG1_IEP0_EDC_LATCH_IN0_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_9	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN1IN_PRG1_IEP0_EDC_LATCH_IN1_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_10	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN0IN_PRG1_IEP1_EDC_LATCH_IN0_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_11	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN1IN_PRG1_IEP1_EDC_LATCH_IN1_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_12	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_13	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_14	PINFUNCTION_CPTS0_HW1TSPUSHIN_CPTS0_HW1TSPUSH_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_15	PINFUNCTION_CPTS0_HW2TSPUSHIN_CPTS0_HW2TSPUSH_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_16	CPTS0_CPTS_GENF0_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_17	CPTS0_CPTS_GENF1_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_18	CPTS0_CPTS_GENF2_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_19	CPTS0_CPTS_GENF3_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_20	CPTS0_CPTS_GENF4_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_21	CPSW0_CPTS_GENF0_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_22	CPSW0_CPTS_GENF1_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_23	PCIE0_PCIE_CPTS_GENF0_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_24	CPTS0_CPTS_GENF5_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_25	PRU_ICSSG0_PR1_EDC0_SYNC0_OUT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_26	PRU_ICSSG0_PR1_EDC0_SYNC1_OUT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_27	PRU_ICSSG0_PR1_EDC1_SYNC0_OUT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_28	PRU_ICSSG0_PR1_EDC1_SYNC1_OUT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_29	PRU_ICSSG1_PR1_EDC0_SYNC0_OUT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_30	PRU_ICSSG1_PR1_EDC0_SYNC1_OUT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_31	PRU_ICSSG1_PR1_EDC1_SYNC0_OUT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_32	PRU_ICSSG1_PR1_EDC1_SYNC1_OUT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_33	PCIE0_PCIE_CPTS_SYNC_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
TIMESYNC_EVENT_INTROUTER0	TIMESYNC_EVENT_INTROUTER0_IN_IN_34	CPSW0_CPTS_SYNC_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_35	CPTS0_CPTS_SYNC_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_36	GTC0_GTC_PUSH_EVENT_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_37	PCIE0_PCIE_CPTS_HW1_PUSH_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_38	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_39	EPWM0_EPWM_SYNCO_O_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_40	EPWM3_EPWM_SYNCO_O_OUT_0
	TIMESYNC_EVENT_INTROUTER0_IN_IN_41	EPWM6_EPWM_SYNCO_O_OUT_0
MCU_M4FSS0_CORE0	MCU_M4FSS0_CORE0_NVIC_IN_0	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_4
	MCU_M4FSS0_CORE0_NVIC_IN_1	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_5
	MCU_M4FSS0_CORE0_NVIC_IN_2	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_6
	MCU_M4FSS0_CORE0_NVIC_IN_3	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_7
	MCU_M4FSS0_CORE0_NVIC_IN_4	MCU_TIMER0_INTR_PEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_5	MCU_TIMER1_INTR_PEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_6	MCU_TIMER2_INTR_PEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_7	MCU_TIMER3_INTR_PEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_8	MCU_MASTER_SAFETY_GASKET0_TIMED_OUT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_11	MCU_ESM0_ESM_INT_CFG_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_12	MCU_ESM0_ESM_INT_HI_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_13	MCU_ESM0_ESM_INT_LOW_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_14	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_15	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_16	MCU_MCRC64_0_INT_MCRC_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_17	MCU_I2C0_POINTRPEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_18	MCU_I2C1_POINTRPEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_19	MCU_RTI0_INTR_WWD_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_20	MCU_PSC0_PSC_ALLINT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_21	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_22	MCU_MCSPI0_INTR_SPI_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_23	MCU_MCSPI1_INTR_SPI_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_24	MCU_UART0_USART_IRQ_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_25	MCU_UART1_USART_IRQ_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_26	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_M4FSS0_CORE0	MCU_M4FSS0_CORE0_NVIC_IN_27	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1
	MCU_M4FSS0_CORE0_NVIC_IN_28	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_29	DDPA0_DDPA_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_30	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_31	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_32	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168
	MCU_M4FSS0_CORE0_NVIC_IN_33	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169
	MCU_M4FSS0_CORE0_NVIC_IN_34	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170
	MCU_M4FSS0_CORE0_NVIC_IN_35	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171
	MCU_M4FSS0_CORE0_NVIC_IN_36	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172
	MCU_M4FSS0_CORE0_NVIC_IN_37	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173
	MCU_M4FSS0_CORE0_NVIC_IN_38	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174
	MCU_M4FSS0_CORE0_NVIC_IN_39	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175
	MCU_M4FSS0_CORE0_NVIC_IN_40	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_176
	MCU_M4FSS0_CORE0_NVIC_IN_41	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_177
	MCU_M4FSS0_CORE0_NVIC_IN_42	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_178
	MCU_M4FSS0_CORE0_NVIC_IN_43	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_179
	MCU_M4FSS0_CORE0_NVIC_IN_44	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_180
	MCU_M4FSS0_CORE0_NVIC_IN_45	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_181
	MCU_M4FSS0_CORE0_NVIC_IN_46	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_182
	MCU_M4FSS0_CORE0_NVIC_IN_47	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_183
	MCU_M4FSS0_CORE0_NVIC_IN_48	DMSC0_AES_0_HIB_PUBLIC_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_49	DMSC0_AES_0_HIB_SECURE_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_50	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_51	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6
	MCU_M4FSS0_CORE0_NVIC_IN_52	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	MCU_M4FSS0_CORE0_NVIC_IN_53	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_54	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_55	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_56	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_3
	MCU_M4FSS0_CORE0_NVIC_IN_57	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_3
	MCU_M4FSS0_CORE0_NVIC_IN_58	CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_59	PADCFG_CTRL0_ACCESS_ERR_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_M4FSS0_CORE0	MCU_M4FSS0_CORE0_NVIC_IN_60	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_61	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_62	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6
	MCU_M4FSS0_CORE0_NVIC_IN_63	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7
CPSW0	CPSW0_CPTS_HW1_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_30
	CPSW0_CPTS_HW2_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_31
	CPSW0_CPTS_HW3_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_32
	CPSW0_CPTS_HW4_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_33
	CPSW0_CPTS_HW5_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_34
	CPSW0_CPTS_HW6_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_35
	CPSW0_CPTS_HW7_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_36
	CPSW0_CPTS_HW8_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_37
DMSC0_CORTEX_M3_0	DMSC0_CORTEX_M3_0_NVIC_IN_8	DMSC0_DMTIMER_0_INTR_PEND_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_10	DMSC0_DMTIMER_1_INTR_PEND_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_11	DMSC0_RAT_0_EXP_INTR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_12	DMSC0_ECC_AGGR_0_ECC_CORRECTED_ERR_PULSE_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_13	DMSC0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_PULSE_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_16	DMSC0_RTI_0_INTR_WWD_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_17	DMSC0_RTI_0_INTR_RTI_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_18	DMSC0_RTI_0_INTR_RTI_OUT_1
	DMSC0_CORTEX_M3_0_NVIC_IN_19	DMSC0_RTI_0_INTR_RTI_OUT_2
	DMSC0_CORTEX_M3_0_NVIC_IN_20	DMSC0_RTI_0_INTR_RTI_OUT_3
	DMSC0_CORTEX_M3_0_NVIC_IN_32	DMSC0_DMTIMER_2_INTR_PEND_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_34	DMSC0_DMTIMER_3_INTR_PEND_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_36	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_38	DMSC0_AES_0_HIB_SECURE_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_39	DMSC0_AES_0_HIB_PUBLIC_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_46	DMSC0_CBASS_0_FW_INT_DMSC_EXP_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_47	DMSC0_CBASS_0_FW_COMBINED_EXP_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_48	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_49	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1
	DMSC0_CORTEX_M3_0_NVIC_IN_50	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2
	DMSC0_CORTEX_M3_0_NVIC_IN_51	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMSC0_CORTEX_M3_0	DMSC0_CORTEX_M3_0_NVIC_IN_52	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4
	DMSC0_CORTEX_M3_0_NVIC_IN_53	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5
	DMSC0_CORTEX_M3_0_NVIC_IN_54	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6
	DMSC0_CORTEX_M3_0_NVIC_IN_55	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7
	DMSC0_CORTEX_M3_0_NVIC_IN_56	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8
	DMSC0_CORTEX_M3_0_NVIC_IN_57	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9
	DMSC0_CORTEX_M3_0_NVIC_IN_58	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10
	DMSC0_CORTEX_M3_0_NVIC_IN_59	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11
	DMSC0_CORTEX_M3_0_NVIC_IN_60	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12
	DMSC0_CORTEX_M3_0_NVIC_IN_61	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13
	DMSC0_CORTEX_M3_0_NVIC_IN_62	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14
	DMSC0_CORTEX_M3_0_NVIC_IN_63	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15
	DMSC0_CORTEX_M3_0_NVIC_IN_64	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16
	DMSC0_CORTEX_M3_0_NVIC_IN_65	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17
	DMSC0_CORTEX_M3_0_NVIC_IN_66	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18
	DMSC0_CORTEX_M3_0_NVIC_IN_67	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19
	DMSC0_CORTEX_M3_0_NVIC_IN_68	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20
	DMSC0_CORTEX_M3_0_NVIC_IN_69	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21
	DMSC0_CORTEX_M3_0_NVIC_IN_70	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22
	DMSC0_CORTEX_M3_0_NVIC_IN_71	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23
	DMSC0_CORTEX_M3_0_NVIC_IN_72	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24
	DMSC0_CORTEX_M3_0_NVIC_IN_73	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25
	DMSC0_CORTEX_M3_0_NVIC_IN_74	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26
	DMSC0_CORTEX_M3_0_NVIC_IN_75	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27
	DMSC0_CORTEX_M3_0_NVIC_IN_76	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28
	DMSC0_CORTEX_M3_0_NVIC_IN_77	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29
	DMSC0_CORTEX_M3_0_NVIC_IN_78	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30
	DMSC0_CORTEX_M3_0_NVIC_IN_79	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31
	DMSC0_CORTEX_M3_0_NVIC_IN_80	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32
	DMSC0_CORTEX_M3_0_NVIC_IN_81	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33
	DMSC0_CORTEX_M3_0_NVIC_IN_82	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34
	DMSC0_CORTEX_M3_0_NVIC_IN_83	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35
	DMSC0_CORTEX_M3_0_NVIC_IN_84	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMSC0_CORTEX_M3_0	DMSC0_CORTEX_M3_0_NVIC_IN_85	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37
	DMSC0_CORTEX_M3_0_NVIC_IN_86	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38
	DMSC0_CORTEX_M3_0_NVIC_IN_87	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39
	DMSC0_CORTEX_M3_0_NVIC_IN_88	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40
	DMSC0_CORTEX_M3_0_NVIC_IN_89	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41
	DMSC0_CORTEX_M3_0_NVIC_IN_90	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42
	DMSC0_CORTEX_M3_0_NVIC_IN_91	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43
	DMSC0_CORTEX_M3_0_NVIC_IN_92	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44
	DMSC0_CORTEX_M3_0_NVIC_IN_93	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45
	DMSC0_CORTEX_M3_0_NVIC_IN_94	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46
	DMSC0_CORTEX_M3_0_NVIC_IN_95	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47
	DMSC0_CORTEX_M3_0_NVIC_IN_96	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48
	DMSC0_CORTEX_M3_0_NVIC_IN_97	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49
	DMSC0_CORTEX_M3_0_NVIC_IN_98	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50
	DMSC0_CORTEX_M3_0_NVIC_IN_99	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51
	DMSC0_CORTEX_M3_0_NVIC_IN_100	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52
	DMSC0_CORTEX_M3_0_NVIC_IN_101	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53
	DMSC0_CORTEX_M3_0_NVIC_IN_102	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54
	DMSC0_CORTEX_M3_0_NVIC_IN_103	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55
	DMSC0_CORTEX_M3_0_NVIC_IN_104	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56
	DMSC0_CORTEX_M3_0_NVIC_IN_105	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57
	DMSC0_CORTEX_M3_0_NVIC_IN_106	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58
	DMSC0_CORTEX_M3_0_NVIC_IN_107	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59
	DMSC0_CORTEX_M3_0_NVIC_IN_108	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60
	DMSC0_CORTEX_M3_0_NVIC_IN_109	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61
	DMSC0_CORTEX_M3_0_NVIC_IN_110	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62
	DMSC0_CORTEX_M3_0_NVIC_IN_111	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63
	DMSC0_CORTEX_M3_0_NVIC_IN_112	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64
	DMSC0_CORTEX_M3_0_NVIC_IN_113	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65
	DMSC0_CORTEX_M3_0_NVIC_IN_114	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66
	DMSC0_CORTEX_M3_0_NVIC_IN_115	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67
	DMSC0_CORTEX_M3_0_NVIC_IN_116	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68
	DMSC0_CORTEX_M3_0_NVIC_IN_117	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMSC0_CORTEX_M3_0	DMSC0_CORTEX_M3_0_NVIC_IN_118	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70
	DMSC0_CORTEX_M3_0_NVIC_IN_119	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71
	DMSC0_CORTEX_M3_0_NVIC_IN_120	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72
	DMSC0_CORTEX_M3_0_NVIC_IN_121	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73
	DMSC0_CORTEX_M3_0_NVIC_IN_122	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74
	DMSC0_CORTEX_M3_0_NVIC_IN_123	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75
	DMSC0_CORTEX_M3_0_NVIC_IN_124	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76
	DMSC0_CORTEX_M3_0_NVIC_IN_125	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77
	DMSC0_CORTEX_M3_0_NVIC_IN_126	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78
	DMSC0_CORTEX_M3_0_NVIC_IN_127	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79
	DMSC0_CORTEX_M3_0_NVIC_IN_128	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_80
	DMSC0_CORTEX_M3_0_NVIC_IN_129	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_81
	DMSC0_CORTEX_M3_0_NVIC_IN_130	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_82
	DMSC0_CORTEX_M3_0_NVIC_IN_131	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_83
	DMSC0_CORTEX_M3_0_NVIC_IN_132	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_84
	DMSC0_CORTEX_M3_0_NVIC_IN_133	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_85
	DMSC0_CORTEX_M3_0_NVIC_IN_134	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_86
	DMSC0_CORTEX_M3_0_NVIC_IN_135	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_87
	DMSC0_CORTEX_M3_0_NVIC_IN_136	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88
	DMSC0_CORTEX_M3_0_NVIC_IN_137	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89
	DMSC0_CORTEX_M3_0_NVIC_IN_138	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90
	DMSC0_CORTEX_M3_0_NVIC_IN_139	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91
	DMSC0_CORTEX_M3_0_NVIC_IN_140	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92
	DMSC0_CORTEX_M3_0_NVIC_IN_141	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93
	DMSC0_CORTEX_M3_0_NVIC_IN_142	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94
	DMSC0_CORTEX_M3_0_NVIC_IN_143	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95
	DMSC0_CORTEX_M3_0_NVIC_IN_144	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96
	DMSC0_CORTEX_M3_0_NVIC_IN_145	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97
	DMSC0_CORTEX_M3_0_NVIC_IN_146	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98
	DMSC0_CORTEX_M3_0_NVIC_IN_147	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99
	DMSC0_CORTEX_M3_0_NVIC_IN_148	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_100
	DMSC0_CORTEX_M3_0_NVIC_IN_149	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_101
	DMSC0_CORTEX_M3_0_NVIC_IN_150	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_102

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMSC0_CORTEX_M3_0	DMSC0_CORTEX_M3_0_NVIC_IN_151	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_103
	DMSC0_CORTEX_M3_0_NVIC_IN_152	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_104
	DMSC0_CORTEX_M3_0_NVIC_IN_153	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_105
	DMSC0_CORTEX_M3_0_NVIC_IN_154	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_106
	DMSC0_CORTEX_M3_0_NVIC_IN_155	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_107
	DMSC0_CORTEX_M3_0_NVIC_IN_156	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_108
	DMSC0_CORTEX_M3_0_NVIC_IN_157	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_109
	DMSC0_CORTEX_M3_0_NVIC_IN_158	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_110
	DMSC0_CORTEX_M3_0_NVIC_IN_159	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_111
	DMSC0_CORTEX_M3_0_NVIC_IN_160	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_112
	DMSC0_CORTEX_M3_0_NVIC_IN_161	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_113
	DMSC0_CORTEX_M3_0_NVIC_IN_162	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_114
	DMSC0_CORTEX_M3_0_NVIC_IN_163	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_115
	DMSC0_CORTEX_M3_0_NVIC_IN_164	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_116
	DMSC0_CORTEX_M3_0_NVIC_IN_165	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_117
	DMSC0_CORTEX_M3_0_NVIC_IN_166	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_118
	DMSC0_CORTEX_M3_0_NVIC_IN_167	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_119
	DMSC0_CORTEX_M3_0_NVIC_IN_168	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_120
	DMSC0_CORTEX_M3_0_NVIC_IN_169	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_121
	DMSC0_CORTEX_M3_0_NVIC_IN_170	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_122
	DMSC0_CORTEX_M3_0_NVIC_IN_171	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_123
	DMSC0_CORTEX_M3_0_NVIC_IN_172	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_124
	DMSC0_CORTEX_M3_0_NVIC_IN_173	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_125
	DMSC0_CORTEX_M3_0_NVIC_IN_174	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_126
	DMSC0_CORTEX_M3_0_NVIC_IN_175	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_127
	DMSC0_CORTEX_M3_0_NVIC_IN_176	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_136
	DMSC0_CORTEX_M3_0_NVIC_IN_177	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_137
	DMSC0_CORTEX_M3_0_NVIC_IN_178	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_138
	DMSC0_CORTEX_M3_0_NVIC_IN_179	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_139
	DMSC0_CORTEX_M3_0_NVIC_IN_180	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_140
	DMSC0_CORTEX_M3_0_NVIC_IN_181	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_141
	DMSC0_CORTEX_M3_0_NVIC_IN_182	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_142
	DMSC0_CORTEX_M3_0_NVIC_IN_183	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_143

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMSC0_CORTEX_M3_0	DMSC0_CORTEX_M3_0_NVIC_IN_184	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_144
	DMSC0_CORTEX_M3_0_NVIC_IN_185	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_145
	DMSC0_CORTEX_M3_0_NVIC_IN_186	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_146
	DMSC0_CORTEX_M3_0_NVIC_IN_187	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_147
	DMSC0_CORTEX_M3_0_NVIC_IN_188	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_148
	DMSC0_CORTEX_M3_0_NVIC_IN_189	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_149
	DMSC0_CORTEX_M3_0_NVIC_IN_190	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_150
	DMSC0_CORTEX_M3_0_NVIC_IN_191	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_151
	DMSC0_CORTEX_M3_0_NVIC_IN_194	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_195	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_196	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_197	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_198	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_199	ESM0_ESM_INT_CFG_LVL_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_200	ESM0_ESM_INT_HI_LVL_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_201	ESM0_ESM_INT_LOW_LVL_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_202	CBASS_FW0_DEFAULT_ERR_INTR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_203	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_204	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1
	DMSC0_CORTEX_M3_0_NVIC_IN_205	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_208	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_209	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	DMSC0_CORTEX_M3_0_NVIC_IN_210	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	DMSC0_CORTEX_M3_0_NVIC_IN_211	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	DMSC0_CORTEX_M3_0_NVIC_IN_212	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	DMSC0_CORTEX_M3_0_NVIC_IN_213	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	DMSC0_CORTEX_M3_0_NVIC_IN_214	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	DMSC0_CORTEX_M3_0_NVIC_IN_215	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	DMSC0_CORTEX_M3_0_NVIC_IN_224	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_227	FSS0_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_228	FSS0_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_229	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_230	CTRL_MMR0_ACCESS_ERR_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMSC0_CORTEX_M3_0	DMSC0_CORTEX_M3_0_NVIC_IN_231	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_232	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_233	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_234	PBIST0_DFT_PBIST_CPU_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_235	PBIST1_DFT_PBIST_CPU_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_236	PBIST2_DFT_PBIST_CPU_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_237	PBIST3_DFT_PBIST_CPU_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_238	PSC0_PSC_ALLINT_OUT_0
	DMSC0_CORTEX_M3_0_NVIC_IN_239	MCU_PSC0_PSC_ALLINT_OUT_0
	DMSC0_CORTEX_M3_0_SEC_IN_IN_0	CBASS0_DEFAULT_EXP_OUT_0
	DMSC0_CORTEX_M3_0_SEC_IN_IN_1	CBASS_INFRA1_DEFAULT_EXP_OUT_0
	DMSC0_CORTEX_M3_0_SEC_IN_IN_49	SA2_UL0_SECURITY_OUT_0
DMSC0_MISC_0	DMSC0_MISC_0_DEBUG_FORCEACTIVE_IN_0	DDPA0_DDPA_INTR_OUT_0
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_0	CMP_EVENT_INTROUTER0_OUTP_OUT_32
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_1	CMP_EVENT_INTROUTER0_OUTP_OUT_33
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_2	CMP_EVENT_INTROUTER0_OUTP_OUT_34
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_3	CMP_EVENT_INTROUTER0_OUTP_OUT_35
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_4	CMP_EVENT_INTROUTER0_OUTP_OUT_36
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_5	CMP_EVENT_INTROUTER0_OUTP_OUT_37
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_6	CMP_EVENT_INTROUTER0_OUTP_OUT_38
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_7	CMP_EVENT_INTROUTER0_OUTP_OUT_39
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_8	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_9	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_1
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_10	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_2
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_11	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_3
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_12	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_4
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_13	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_5
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_14	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_6
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_15	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_7
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_16	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_17	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_18	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_32
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_19	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_33

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_20	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_21	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_22	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_36
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_23	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_37
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_24	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_16
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_25	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_17
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_28	DEBUGSS0_DAVDMA_LEVEL_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_29	GPMC0_GPMC_SDMAREQ_OUT_0
ESM0	ESM0_ESM_LVL_EVENT_IN_0	ADC0_ECC_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_1	ECC_AGGR0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_2	ECC_AGGR1_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_3	CPSW0_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_4	DMSC0_RAT_0_EXP_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_5	DMSC0_RTI_0_INTR_WWD_OUT_0
	ESM0_ESM_LVL_EVENT_IN_6	DDR16SS0_DDRSS_DRAM_ECC_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_8	DMSC0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_9	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_11	FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_12	GICSS0_ECC_AGGR_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_13	PRU_ICSSG0_PR1_ECC_SEC_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_14	PRU_ICSSG1_PR1_ECC_SEC_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_15	PDMA0_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_16	MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_17	MCAN1_MCANSS_ECC_CORR_LVL_INT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_18	MSRAM_256K0_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_19	MSRAM_256K1_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_20	MSRAM_256K2_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_21	MSRAM_256K3_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_22	MSRAM_256K4_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_23	MSRAM_256K5_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_24	A53SS0_ECC_ECCAGGR0_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_25	A53SS0_ECC_ECCAGGR1_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_26	A53SS0_ECC_ECCAGGR_COREPAC_CORRECTED_ERR_LEVEL_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_27	PCIE0_PCIE_ECC0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_28	PDMA1_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_29	PSRAMECC0_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_30	R5FSS0_CORE0_ECC_CORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_31	R5FSS0_CORE1_ECC_CORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_32	R5FSS1_CORE0_ECC_CORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_33	R5FSS1_CORE1_ECC_CORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_34	SA2_UL0_SA_UL_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_35	USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_37	MCU_ESM0_ESM_INT_CFG_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_38	MCU_ESM0_ESM_INT_HI_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_39	MCU_ESM0_ESM_INT_LOW_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_40	R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0
	ESM0_ESM_LVL_EVENT_IN_41	R5FSS0_COMMON0_ECC_DE_TO_ESM_1_OUT_0
	ESM0_ESM_LVL_EVENT_IN_42	R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0
	ESM0_ESM_LVL_EVENT_IN_43	R5FSS0_COMMON0_ECC_SE_TO_ESM_1_OUT_0
	ESM0_ESM_LVL_EVENT_IN_44	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_45	R5FSS1_COMMON0_ECC_DE_TO_ESM_0_OUT_0
	ESM0_ESM_LVL_EVENT_IN_46	R5FSS1_COMMON0_ECC_DE_TO_ESM_1_OUT_0
	ESM0_ESM_LVL_EVENT_IN_47	R5FSS1_COMMON0_ECC_SE_TO_ESM_0_OUT_0
	ESM0_ESM_LVL_EVENT_IN_48	R5FSS1_COMMON0_ECC_SE_TO_ESM_1_OUT_0
	ESM0_ESM_LVL_EVENT_IN_50	DMSC0_DMTIMER_0_INTR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_51	DMSC0_DMTIMER_1_INTR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_52	DMSC0_DMTIMER_2_INTR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_53	DMSC0_DMTIMER_3_INTR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_54	MMCSD0_EMMCSS_RXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_55	MMCSD0_EMMCSS_RXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_56	MMCSD0_EMMCSS_TXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_57	MMCSD0_EMMCSS_TXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_58	MMCSD1_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_59	MMCSD1_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_60	MMCSD1_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_61	MMCSD1_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_62	MSRAM_256K6_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_63	MSRAM_256K7_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_64	ADC0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_65	ECC_AGGR0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_66	ECC_AGGR1_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_67	CPSW0_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_68	PRU_ICSSG0_PR1_EDIO0_WD_TRIIG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_69	DDR16SS0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_70	PRU_ICSSG0_PR1_EDIO1_WD_TRIIG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_71	DMSC0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_72	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_74	FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_75	GICSS0_ECC_AGGR_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_76	PRU_ICSSG0_PR1_ECC_DED_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_77	PRU_ICSSG1_PR1_ECC_DED_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_78	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_79	MCAN1_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_80	MSRAM_256K0_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_81	MSRAM_256K1_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_82	MSRAM_256K2_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_83	MSRAM_256K3_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_84	MSRAM_256K4_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_85	MSRAM_256K5_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_86	PCIE0_PCIE_ECC0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_87	PCIE0_PCIE_ECC1_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_88	PDMA0_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_89	PDMA1_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_90	PSRAMECC0_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_91	R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_92	SA2_UL0_SA_UL_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_93	A53SS0_ECC_ECCAGGR1_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_94	A53SS0_ECC_ECCAGGR0_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_95	A53SS0_ECC_ECCAGGR_COREPAC_UNCORRECTED_ERR_LEVEL_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_96	PRU_ICSSG1_PR1_EDIO0_WD_TRIIG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_97	PRU_ICSSG1_PR1_EDIO1_WD_TRIIG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_98	DFTSS0_DFT_SAFETY_123_OUT_0
	ESM0_ESM_LVL_EVENT_IN_99	DFTSS0_DFT_SAFETY_MULTI_OUT_0
	ESM0_ESM_LVL_EVENT_IN_100	DFTSS0_DFT_SAFETY_ONE_OUT_0
	ESM0_ESM_LVL_EVENT_IN_101	MAIN_16FF0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_102	MAIN_16FF0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_103	MSRAM_256K6_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_104	MSRAM_256K7_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_105	R5FSS0_CORE1_ECC_UNCORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_106	R5FSS1_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_107	R5FSS1_CORE1_ECC_UNCORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_110	DDR16SS0_DDRSS_V2A_OTHER_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_111	USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_112	DCC0_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_113	DCC1_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_114	DCC2_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_115	DCC3_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_116	DCC4_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_117	DCC5_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_124	R5FSS0_CORE0_EXP_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_125	R5FSS0_CORE1_EXP_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_126	R5FSS1_CORE0_EXP_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_127	R5FSS1_CORE1_EXP_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_128	PLLFRACF_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_129	PLLFRACF_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_130	PLLFRACF_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_131	PLLFRACF_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_132	PLLFRACF_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_133	PLLFRACF_SSMOD_16FFT14_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_134	MCU_PLLFRACF_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_136	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_137	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_138	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_139	VTM0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_140	VTM0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_141	FSS0_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_142	USB0_ASF_INT_FATAL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_143	USB0_ASF_INT_NONFATAL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_144	A53SS0_EXTERRIRQ_OUT_0
	ESM0_ESM_LVL_EVENT_IN_145	A53SS0_INTERRIRQ_OUT_0
	ESM0_ESM_LVL_EVENT_IN_156	PBIST3_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_157	PBIST2_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_158	PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_159	PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_160	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_161	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_162	RTI8_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_163	RTI9_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_164	RTI10_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_165	RTI11_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_166	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_167	GICSS0_ECC_FATAL_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_168	PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_170	PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_172	PBIST2_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_174	PBIST3_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_176	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_160	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_161	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_162	RTI8_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_163	RTI9_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_164	RTI10_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_165	RTI11_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_166	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_167	GICSS0_ECC_FATAL_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_PLS_EVENT1_IN_168	PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_170	PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_172	PBIST2_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_174	PBIST3_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_176	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_160	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_161	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_162	RTI8_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_163	RTI9_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_164	RTI10_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_165	RTI11_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_166	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_167	GICSS0_ECC_FATAL_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_168	PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_170	PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_172	PBIST2_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_174	PBIST3_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_176	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
MCU_ESM0	MCU_ESM0_ESM_LVL_EVENT_IN_0	ESM0_ESM_INT_CFG_LVL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_1	ESM0_ESM_INT_HI_LVL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_2	ESM0_ESM_INT_LOW_LVL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_3	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_4	MCU_M4FSS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_5	MCU_M4FSS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_8	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_9	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_10	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_11	VTM0_CORR_LEVEL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_12	VTM0_UNCORR_LEVEL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_14	MCU_ECC_AGGR0_CORR_LEVEL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_15	MCU_ECC_AGGR0_UNCORR_LEVEL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_26	MCU_MASTER_SAFETY_GASKET0_TIMED_OUT_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_27	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_ESM0	MCU_ESM0_ESM_LVL_EVENT_IN_36	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_37	MCU_DCC0_INTR_ERR_LEVEL_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_47	MCU_PLLFRACF_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_54	PLLFRACF_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_55	PLLFRACF_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_56	PLLFRACF_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_57	PLLFRACF_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_58	PLLFRACF_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0
	MCU_ESM0_ESM_LVL_EVENT_IN_59	PLLFRACF_SSMOD_16FFT14_LOCKLOSS_IPCFG_OUT_0
	MCU_ESM0_ESM_PLS_EVENT0_IN_64	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT0_IN_65	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	MCU_ESM0_ESM_PLS_EVENT0_IN_66	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT0_IN_67	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT0_IN_68	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT0_IN_69	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_5
	MCU_ESM0_ESM_PLS_EVENT0_IN_70	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_6
	MCU_ESM0_ESM_PLS_EVENT0_IN_71	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT0_IN_72	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	MCU_ESM0_ESM_PLS_EVENT0_IN_73	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT0_IN_74	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT0_IN_75	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT0_IN_76	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_5
	MCU_ESM0_ESM_PLS_EVENT0_IN_77	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_6
	MCU_ESM0_ESM_PLS_EVENT0_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT0_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	MCU_ESM0_ESM_PLS_EVENT0_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT0_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT0_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT0_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	MCU_ESM0_ESM_PLS_EVENT0_IN_88	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	MCU_ESM0_ESM_PLS_EVENT0_IN_89	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	MCU_ESM0_ESM_PLS_EVENT0_IN_90	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	MCU_ESM0_ESM_PLS_EVENT0_IN_91	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_ESM0	MCU_ESM0_ESM_PLS_EVENT1_IN_64	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT1_IN_65	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	MCU_ESM0_ESM_PLS_EVENT1_IN_66	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT1_IN_67	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT1_IN_68	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT1_IN_69	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_5
	MCU_ESM0_ESM_PLS_EVENT1_IN_70	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_6
	MCU_ESM0_ESM_PLS_EVENT1_IN_71	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT1_IN_72	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	MCU_ESM0_ESM_PLS_EVENT1_IN_73	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT1_IN_74	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT1_IN_75	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT1_IN_76	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_5
	MCU_ESM0_ESM_PLS_EVENT1_IN_77	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_6
	MCU_ESM0_ESM_PLS_EVENT1_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT1_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	MCU_ESM0_ESM_PLS_EVENT1_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT1_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT1_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT1_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	MCU_ESM0_ESM_PLS_EVENT1_IN_88	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	MCU_ESM0_ESM_PLS_EVENT1_IN_89	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	MCU_ESM0_ESM_PLS_EVENT1_IN_90	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	MCU_ESM0_ESM_PLS_EVENT1_IN_91	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
	MCU_ESM0_ESM_PLS_EVENT2_IN_64	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT2_IN_65	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	MCU_ESM0_ESM_PLS_EVENT2_IN_66	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT2_IN_67	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT2_IN_68	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT2_IN_69	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_5
	MCU_ESM0_ESM_PLS_EVENT2_IN_70	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_6
	MCU_ESM0_ESM_PLS_EVENT2_IN_71	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT2_IN_72	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_ESM0	MCU_ESM0_ESM_PLS_EVENT2_IN_73	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT2_IN_74	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT2_IN_75	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT2_IN_76	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_5
	MCU_ESM0_ESM_PLS_EVENT2_IN_77	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_6
	MCU_ESM0_ESM_PLS_EVENT2_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	MCU_ESM0_ESM_PLS_EVENT2_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	MCU_ESM0_ESM_PLS_EVENT2_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	MCU_ESM0_ESM_PLS_EVENT2_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	MCU_ESM0_ESM_PLS_EVENT2_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	MCU_ESM0_ESM_PLS_EVENT2_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	MCU_ESM0_ESM_PLS_EVENT2_IN_88	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	MCU_ESM0_ESM_PLS_EVENT2_IN_89	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	MCU_ESM0_ESM_PLS_EVENT2_IN_90	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	MCU_ESM0_ESM_PLS_EVENT2_IN_91	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
GICSS0	GICSS0_PPI0_0_IN_22	A53SS0_COMMIRQ0_OUT_0
	GICSS0_PPI0_0_IN_23	A53SS0_PMUIRQ0_OUT_0
	GICSS0_PPI0_0_IN_24	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_0_IN_25	A53SS0_VCPUMNTIRQ0_OUT_0
	GICSS0_PPI0_0_IN_26	A53SS0_CNTHPIRQ0_OUT_0
	GICSS0_PPI0_0_IN_27	A53SS0_CNTVIRQ0_OUT_0
	GICSS0_PPI0_0_IN_29	A53SS0_CNTPSIRQ0_OUT_0
	GICSS0_PPI0_0_IN_30	A53SS0_CNTPNSIRQ0_OUT_0
	GICSS0_PPI0_0_IN_31	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_1_IN_22	A53SS0_COMMIRQ1_OUT_0
	GICSS0_PPI0_1_IN_23	A53SS0_PMUIRQ1_OUT_0
	GICSS0_PPI0_1_IN_24	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_1_IN_25	A53SS0_VCPUMNTIRQ1_OUT_0
	GICSS0_PPI0_1_IN_26	A53SS0_CNTHPIRQ1_OUT_0
	GICSS0_PPI0_1_IN_27	A53SS0_CNTVIRQ1_OUT_0
	GICSS0_PPI0_1_IN_29	A53SS0_CNTPSIRQ1_OUT_0
	GICSS0_PPI0_1_IN_30	A53SS0_CNTPNSIRQ1_OUT_0
	GICSS0_PPI0_1_IN_31	A53SS0_CTIIRQ0_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	GICSS0_SPI_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	GICSS0_SPI_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	GICSS0_SPI_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	GICSS0_SPI_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	GICSS0_SPI_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	GICSS0_SPI_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	GICSS0_SPI_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
	GICSS0_SPI_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	GICSS0_SPI_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	GICSS0_SPI_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	GICSS0_SPI_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	GICSS0_SPI_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_4
	GICSS0_SPI_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_5
	GICSS0_SPI_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_6
	GICSS0_SPI_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_7
	GICSS0_SPI_IN_56	CMP_EVENT_INTROUTER0_OUTP_OUT_8
	GICSS0_SPI_IN_57	CMP_EVENT_INTROUTER0_OUTP_OUT_9
	GICSS0_SPI_IN_58	CMP_EVENT_INTROUTER0_OUTP_OUT_10
	GICSS0_SPI_IN_59	CMP_EVENT_INTROUTER0_OUTP_OUT_11
	GICSS0_SPI_IN_60	CMP_EVENT_INTROUTER0_OUTP_OUT_12
	GICSS0_SPI_IN_61	CMP_EVENT_INTROUTER0_OUTP_OUT_13
	GICSS0_SPI_IN_62	CMP_EVENT_INTROUTER0_OUTP_OUT_14
	GICSS0_SPI_IN_63	CMP_EVENT_INTROUTER0_OUTP_OUT_15
	GICSS0_SPI_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1
	GICSS0_SPI_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2
	GICSS0_SPI_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3
	GICSS0_SPI_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4
	GICSS0_SPI_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5
	GICSS0_SPI_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6
	GICSS0_SPI_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7
	GICSS0_SPI_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8
	GICSS0_SPI_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9
	GICSS0_SPI_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10
	GICSS0_SPI_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11
	GICSS0_SPI_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12
	GICSS0_SPI_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13
	GICSS0_SPI_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14
	GICSS0_SPI_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15
	GICSS0_SPI_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16
	GICSS0_SPI_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17
	GICSS0_SPI_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18
	GICSS0_SPI_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19
	GICSS0_SPI_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20
	GICSS0_SPI_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21
	GICSS0_SPI_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22
	GICSS0_SPI_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23
	GICSS0_SPI_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24
	GICSS0_SPI_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25
	GICSS0_SPI_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26
	GICSS0_SPI_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27
	GICSS0_SPI_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28
	GICSS0_SPI_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29
	GICSS0_SPI_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30
	GICSS0_SPI_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31
	GICSS0_SPI_IN_96	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32
	GICSS0_SPI_IN_97	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_98	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34
	GICSS0_SPI_IN_99	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35
	GICSS0_SPI_IN_100	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36
	GICSS0_SPI_IN_101	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37
	GICSS0_SPI_IN_102	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38
	GICSS0_SPI_IN_103	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39
	GICSS0_SPI_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_108	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_2
	GICSS0_SPI_IN_109	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_2
	GICSS0_SPI_IN_112	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_2
	GICSS0_SPI_IN_113	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_3
	GICSS0_SPI_IN_114	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_2
	GICSS0_SPI_IN_115	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_3
	GICSS0_SPI_IN_116	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_2
	GICSS0_SPI_IN_117	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_3
	GICSS0_SPI_IN_118	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_2
	GICSS0_SPI_IN_119	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_3
	GICSS0_SPI_IN_120	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0
	GICSS0_SPI_IN_121	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1
	GICSS0_SPI_IN_122	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2
	GICSS0_SPI_IN_123	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3
	GICSS0_SPI_IN_124	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4
	GICSS0_SPI_IN_125	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5
	GICSS0_SPI_IN_126	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6
	GICSS0_SPI_IN_127	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	GICSS0_SPI_IN_128	ADC0_GEN_LEVEL_OUT_0
	GICSS0_SPI_IN_129	CPTS0_EVNT_PEND_OUT_0
	GICSS0_SPI_IN_130	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_131	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_132	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_134	CPSW0_EVNT_PEND_OUT_0
	GICSS0_SPI_IN_135	CPSW0_MDIO_PEND_OUT_0
	GICSS0_SPI_IN_136	CPSW0_STAT_PEND_OUT_0
	GICSS0_SPI_IN_137	CTRL_MMR0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_138	GPMC0_GPMC_SINTERRUPT_OUT_0
	GICSS0_SPI_IN_139	MCU_I2C0_POINTRPEND_OUT_0
	GICSS0_SPI_IN_140	MCU_I2C1_POINTRPEND_OUT_0
	GICSS0_SPI_IN_141	MCSPI3_INTR_SPI_OUT_0
	GICSS0_SPI_IN_142	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0
	GICSS0_SPI_IN_143	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0
	GICSS0_SPI_IN_144	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1
	GICSS0_SPI_IN_145	ECAP0_ECAP_INT_OUT_0
	GICSS0_SPI_IN_146	ECAP1_ECAP_INT_OUT_0
	GICSS0_SPI_IN_147	ECAP2_ECAP_INT_OUT_0
	GICSS0_SPI_IN_148	EQEP0_EQEP_INT_OUT_0
	GICSS0_SPI_IN_149	EQEP1_EQEP_INT_OUT_0
	GICSS0_SPI_IN_150	EQEP2_EQEP_INT_OUT_0
	GICSS0_SPI_IN_151	DDR16SS0_DDRSS_CONTROLLER_OUT_0
	GICSS0_SPI_IN_152	TIMER0_INTR_PEND_OUT_0
	GICSS0_SPI_IN_153	TIMER1_INTR_PEND_OUT_0
	GICSS0_SPI_IN_154	TIMER2_INTR_PEND_OUT_0
	GICSS0_SPI_IN_155	TIMER3_INTR_PEND_OUT_0
	GICSS0_SPI_IN_156	TIMER4_INTR_PEND_OUT_0
	GICSS0_SPI_IN_157	TIMER5_INTR_PEND_OUT_0
	GICSS0_SPI_IN_158	TIMER6_INTR_PEND_OUT_0
	GICSS0_SPI_IN_159	TIMER7_INTR_PEND_OUT_0
	GICSS0_SPI_IN_160	TIMER8_INTR_PEND_OUT_0
	GICSS0_SPI_IN_161	TIMER9_INTR_PEND_OUT_0
	GICSS0_SPI_IN_162	TIMER10_INTR_PEND_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_163	TIMER11_INTR_PEND_OUT_0
	GICSS0_SPI_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	GICSS0_SPI_IN_165	MMCSD0_EMMCSS_INTR_OUT_0
	GICSS0_SPI_IN_166	MMCSD1_EMMCSDSS_INTR_OUT_0
	GICSS0_SPI_IN_167	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0
	GICSS0_SPI_IN_168	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0
	GICSS0_SPI_IN_169	RTI0_INTR_WWD_OUT_0
	GICSS0_SPI_IN_170	RTI1_INTR_WWD_OUT_0
	GICSS0_SPI_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	GICSS0_SPI_IN_172	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	GICSS0_SPI_IN_176	DMSC0_AES_0_HIB_PUBLIC_OUT_0
	GICSS0_SPI_IN_177	DDPA0_DDPA_INTR_OUT_0
	GICSS0_SPI_IN_178	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0
	GICSS0_SPI_IN_179	PCIE0_PCIE_ERROR_PULSE_OUT_0
	GICSS0_SPI_IN_180	ESM0_ESM_INT_CFG_LVL_OUT_0
	GICSS0_SPI_IN_181	ESM0_ESM_INT_HI_LVL_OUT_0
	GICSS0_SPI_IN_182	ESM0_ESM_INT_LOW_LVL_OUT_0
	GICSS0_SPI_IN_183	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	GICSS0_SPI_IN_184	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	GICSS0_SPI_IN_185	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	GICSS0_SPI_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	GICSS0_SPI_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	GICSS0_SPI_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	GICSS0_SPI_IN_189	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	GICSS0_SPI_IN_190	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	GICSS0_SPI_IN_191	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	GICSS0_SPI_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	GICSS0_SPI_IN_193	I2C0_POINTRPEND_OUT_0
	GICSS0_SPI_IN_194	I2C1_POINTRPEND_OUT_0
	GICSS0_SPI_IN_195	I2C2_POINTRPEND_OUT_0
	GICSS0_SPI_IN_196	I2C3_POINTRPEND_OUT_0
	GICSS0_SPI_IN_197	SA2_UL0_SECURITY_OUT_0
	GICSS0_SPI_IN_198	DMSC0_AES_0_HIB_SECURE_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_199	SA2_UL0_SA_UL_PKA_OUT_0
	GICSS0_SPI_IN_200	SA2_UL0_SA_UL_TRNG_OUT_0
	GICSS0_SPI_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	GICSS0_SPI_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	GICSS0_SPI_IN_203	PSC0_PSC_ALLINT_OUT_0
	GICSS0_SPI_IN_204	MCSPI0_INTR_SPI_OUT_0
	GICSS0_SPI_IN_205	MCSPI1_INTR_SPI_OUT_0
	GICSS0_SPI_IN_206	MCSPI2_INTR_SPI_OUT_0
	GICSS0_SPI_IN_207	MCSPI4_INTR_SPI_OUT_0
	GICSS0_SPI_IN_208	MCU_MCSPI0_INTR_SPI_OUT_0
	GICSS0_SPI_IN_209	MCU_MCSPI1_INTR_SPI_OUT_0
	GICSS0_SPI_IN_210	UART0_USART_IRQ_OUT_0
	GICSS0_SPI_IN_211	UART1_USART_IRQ_OUT_0
	GICSS0_SPI_IN_212	UART2_USART_IRQ_OUT_0
	GICSS0_SPI_IN_213	UART3_USART_IRQ_OUT_0
	GICSS0_SPI_IN_214	UART4_USART_IRQ_OUT_0
	GICSS0_SPI_IN_215	UART5_USART_IRQ_OUT_0
	GICSS0_SPI_IN_216	UART6_USART_IRQ_OUT_0
	GICSS0_SPI_IN_217	MCU_UART0_USART_IRQ_OUT_0
	GICSS0_SPI_IN_218	MCU_UART1_USART_IRQ_OUT_0
	GICSS0_SPI_IN_219	USB0_HOST_SYSTEM_ERROR_OUT_0
	GICSS0_SPI_IN_220	USB0_IRQ_OUT_0
	GICSS0_SPI_IN_221	USB0_IRQ_OUT_1
	GICSS0_SPI_IN_222	USB0_IRQ_OUT_2
	GICSS0_SPI_IN_223	USB0_IRQ_OUT_3
	GICSS0_SPI_IN_224	USB0_IRQ_OUT_4
	GICSS0_SPI_IN_225	USB0_IRQ_OUT_5
	GICSS0_SPI_IN_226	USB0_IRQ_OUT_6
	GICSS0_SPI_IN_227	USB0_IRQ_OUT_7
	GICSS0_SPI_IN_228	USB0_OTGIRQ_OUT_0
	GICSS0_SPI_IN_229	PCIE0_PCIE_CPTS_PEND_OUT_0
	GICSS0_SPI_IN_230	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0
	GICSS0_SPI_IN_231	PCIE0_PCIE_FLR_PULSE_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_232	PCIE0_PCIE_DPA_PULSE_OUT_0
	GICSS0_SPI_IN_233	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0
	GICSS0_SPI_IN_234	PCIE0_PCIE_LEGACY_PULSE_OUT_0
	GICSS0_SPI_IN_235	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0
	GICSS0_SPI_IN_236	PCIE0_PCIE_LOCAL_LEVEL_OUT_0
	GICSS0_SPI_IN_237	PCIE0_PCIE_PHY_LEVEL_OUT_0
	GICSS0_SPI_IN_238	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0
	GICSS0_SPI_IN_239	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0
	GICSS0_SPI_IN_240	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0
	GICSS0_SPI_IN_241	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1
	GICSS0_SPI_IN_242	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0
	GICSS0_SPI_IN_243	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1
	GICSS0_SPI_IN_244	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0
	GICSS0_SPI_IN_245	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1
	GICSS0_SPI_IN_246	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0
	GICSS0_SPI_IN_247	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1
	GICSS0_SPI_IN_248	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0
	GICSS0_SPI_IN_249	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1
	GICSS0_SPI_IN_250	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2
	GICSS0_SPI_IN_251	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3
	GICSS0_SPI_IN_252	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4
	GICSS0_SPI_IN_253	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5
	GICSS0_SPI_IN_254	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6
	GICSS0_SPI_IN_255	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7
	GICSS0_SPI_IN_256	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
PRU_ICSSG0	PRU_ICSSG0_PR1_EDC0_LATCH0_IN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_8
	PRU_ICSSG0_PR1_EDC0_LATCH1_IN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_9
	PRU_ICSSG0_PR1_EDC1_LATCH0_IN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_10
	PRU_ICSSG0_PR1_EDC1_LATCH1_IN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_11
	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18
	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_1	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19
	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_2	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20
	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_3	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PRU_ICSSG0	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_4	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22
	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_5	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23
	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24
	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_1	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25
	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_2	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26
	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_3	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27
	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_4	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28
	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_5	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29
	PRU_ICSSG0_PR1_SLV_INTR_IN_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_152
	PRU_ICSSG0_PR1_SLV_INTR_IN_1	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_153
	PRU_ICSSG0_PR1_SLV_INTR_IN_2	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_154
	PRU_ICSSG0_PR1_SLV_INTR_IN_3	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_155
	PRU_ICSSG0_PR1_SLV_INTR_IN_4	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_156
	PRU_ICSSG0_PR1_SLV_INTR_IN_5	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_157
	PRU_ICSSG0_PR1_SLV_INTR_IN_6	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_158
	PRU_ICSSG0_PR1_SLV_INTR_IN_7	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_159
	PRU_ICSSG0_PR1_SLV_INTR_IN_8	ECAP0_ECAP_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_9	ECAP1_ECAP_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_10	ECAP2_ECAP_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_12	EPWM0_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_13	EPWM0_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_14	EPWM1_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_15	EPWM1_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_16	EPWM2_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_17	EPWM2_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_18	EPWM3_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_19	EPWM3_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_20	EPWM4_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_21	EPWM4_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_22	EPWM5_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_23	EPWM5_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_24	EPWM6_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_25	EPWM6_EPWM_TRIPZINT_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PRU_ICSSG0	PRU_ICSSG0_PR1_SLV_INTR_IN_26	EPWM7_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_27	EPWM7_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_28	EPWM8_EPWM_ETINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_29	EPWM8_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_30	EQEP0_EQEP_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_31	EQEP1_EQEP_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_32	EQEP2_EQEP_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_33	FSIRX0_FSI_RX_OINT1_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_34	FSIRX0_FSI_RX_OINT2_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_35	FSIRX1_FSI_RX_OINT1_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_36	FSIRX1_FSI_RX_OINT2_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_37	FSIRX2_FSI_RX_OINT1_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_38	FSIRX2_FSI_RX_OINT2_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_39	FSIRX3_FSI_RX_OINT1_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_40	FSIRX3_FSI_RX_OINT2_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_41	FSIRX4_FSI_RX_OINT1_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_42	FSIRX4_FSI_RX_OINT2_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_43	FSIRX5_FSI_RX_OINT1_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_44	FSIRX5_FSI_RX_OINT2_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_45	FSITX0_FSI_TX_OINT1_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_38
	PRU_ICSSG0_PR1_SLV_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_39
	PRU_ICSSG0_PR1_SLV_INTR_IN_48	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_40
	PRU_ICSSG0_PR1_SLV_INTR_IN_49	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_41
	PRU_ICSSG0_PR1_SLV_INTR_IN_50	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_42
	PRU_ICSSG0_PR1_SLV_INTR_IN_51	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_43
	PRU_ICSSG0_PR1_SLV_INTR_IN_52	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_44
	PRU_ICSSG0_PR1_SLV_INTR_IN_53	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_45
	PRU_ICSSG0_PR1_SLV_INTR_IN_54	FSITX0_FSI_TX_OINT2_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_55	FSITX1_FSI_TX_OINT1_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_56	FSITX1_FSI_TX_OINT2_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_57	MCSPI0_INTR_SPI_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_58	MCSPI1_INTR_SPI_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PRU_ICSSG0	PRU_ICSSG0_PR1_SLV_INTR_IN_59	MCSPI3_INTR_SPI_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_60	MCSPI4_INTR_SPI_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_61	MCU_MCSPI0_INTR_SPI_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_62	MCU_MCSPI1_INTR_SPI_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_63	UART0_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_64	UART1_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_65	UART2_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_66	UART3_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_67	UART4_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_68	UART5_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_69	UART6_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_70	MCU_UART0_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_71	MCU_UART1_USART_IRQ_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_72	MCSPI2_INTR_SPI_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_75	I2C0_POINTRPEND_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_76	I2C1_POINTRPEND_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_77	I2C2_POINTRPEND_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_78	I2C3_POINTRPEND_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_79	MCU_I2C0_POINTRPEND_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_80	MCU_I2C1_POINTRPEND_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_81	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_82	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_83	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	PRU_ICSSG0_PR1_SLV_INTR_IN_84	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_85	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_86	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	PRU_ICSSG0_PR1_SLV_INTR_IN_87	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5
	PRU_ICSSG0_PR1_SLV_INTR_IN_88	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6
	PRU_ICSSG0_PR1_SLV_INTR_IN_89	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7
	PRU_ICSSG0_PR1_SLV_INTR_IN_90	GPMC0_GPMC_SINTERRUPT_OUT_0
	PRU_ICSSG0_PR1_SLV_INTR_IN_91	ADC0_GEN_LEVEL_OUT_0
PRU_ICSSG1	PRU_ICSSG1_PR1_EDC0_LATCH0_IN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_12
	PRU_ICSSG1_PR1_EDC0_LATCH1_IN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_13

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PRU_ICSSG1	PRU_ICSSG1_PR1_EDC1_LATCH0_IN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_14
	PRU_ICSSG1_PR1_EDC1_LATCH1_IN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_15
	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18
	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_1	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19
	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_2	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20
	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_3	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21
	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_4	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22
	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_5	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23
	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24
	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_1	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25
	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_2	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26
	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_3	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27
	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_4	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28
	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_5	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29
	PRU_ICSSG1_PR1_SLV_INTR_IN_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_160
	PRU_ICSSG1_PR1_SLV_INTR_IN_1	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_161
	PRU_ICSSG1_PR1_SLV_INTR_IN_2	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_162
	PRU_ICSSG1_PR1_SLV_INTR_IN_3	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_163
	PRU_ICSSG1_PR1_SLV_INTR_IN_4	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_164
	PRU_ICSSG1_PR1_SLV_INTR_IN_5	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_165
	PRU_ICSSG1_PR1_SLV_INTR_IN_6	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_166
	PRU_ICSSG1_PR1_SLV_INTR_IN_7	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_167
	PRU_ICSSG1_PR1_SLV_INTR_IN_8	ECAP0_ECAP_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_9	ECAP1_ECAP_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_10	ECAP2_ECAP_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_12	EPWM0_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_13	EPWM0_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_14	EPWM1_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_15	EPWM1_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_16	EPWM2_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_17	EPWM2_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_18	EPWM3_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_19	EPWM3_EPWM_TRIPZINT_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PRU_ICSSG1	PRU_ICSSG1_PR1_SLV_INTR_IN_20	EPWM4_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_21	EPWM4_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_22	EPWM5_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_23	EPWM5_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_24	EPWM6_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_25	EPWM6_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_26	EPWM7_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_27	EPWM7_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_28	EPWM8_EPWM_ETINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_29	EPWM8_EPWM_TRIPZINT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_30	EQEP0_EQEP_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_31	EQEP1_EQEP_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_32	EQEP2_EQEP_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_33	FSIRX0_FSI_RX_OINT1_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_34	FSIRX0_FSI_RX_OINT2_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_35	FSIRX1_FSI_RX_OINT1_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_36	FSIRX1_FSI_RX_OINT2_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_37	FSIRX2_FSI_RX_OINT1_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_38	FSIRX2_FSI_RX_OINT2_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_39	FSIRX3_FSI_RX_OINT1_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_40	FSIRX3_FSI_RX_OINT2_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_41	FSIRX4_FSI_RX_OINT1_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_42	FSIRX4_FSI_RX_OINT2_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_43	FSIRX5_FSI_RX_OINT1_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_44	FSIRX5_FSI_RX_OINT2_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_45	FSITX0_FSI_TX_OINT1_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_46
	PRU_ICSSG1_PR1_SLV_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_47
	PRU_ICSSG1_PR1_SLV_INTR_IN_48	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_48
	PRU_ICSSG1_PR1_SLV_INTR_IN_49	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_49
	PRU_ICSSG1_PR1_SLV_INTR_IN_50	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_50
	PRU_ICSSG1_PR1_SLV_INTR_IN_51	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_51
	PRU_ICSSG1_PR1_SLV_INTR_IN_52	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_52

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PRU_ICSSG1	PRU_ICSSG1_PR1_SLV_INTR_IN_53	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_53
	PRU_ICSSG1_PR1_SLV_INTR_IN_54	FSITX0_FSI_TX_OINT2_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_55	FSITX1_FSI_TX_OINT1_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_56	FSITX1_FSI_TX_OINT2_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_57	MCSPI0_INTR_SPI_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_58	MCSPI1_INTR_SPI_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_59	MCSPI3_INTR_SPI_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_60	MCSPI4_INTR_SPI_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_61	MCU_MCSPI0_INTR_SPI_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_62	MCU_MCSPI1_INTR_SPI_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_63	UART0_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_64	UART1_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_65	UART2_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_66	UART3_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_67	UART4_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_68	UART5_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_69	UART6_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_70	MCU_UART0_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_71	MCU_UART1_USART_IRQ_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_72	MCSPI2_INTR_SPI_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_75	I2C0_POINTRPEND_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_76	I2C1_POINTRPEND_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_77	I2C2_POINTRPEND_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_78	I2C3_POINTRPEND_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_79	MCU_I2C0_POINTRPEND_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_80	MCU_I2C1_POINTRPEND_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_81	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_82	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_83	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	PRU_ICSSG1_PR1_SLV_INTR_IN_84	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_85	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_86	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	PRU_ICSSG1_PR1_SLV_INTR_IN_87	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PRU_ICSSG1	PRU_ICSSG1_PR1_SLV_INTR_IN_88	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6
	PRU_ICSSG1_PR1_SLV_INTR_IN_89	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	PRU_ICSSG1_PR1_SLV_INTR_IN_90	GPMC0_GPMC_SINTERRUPT_OUT_0
	PRU_ICSSG1_PR1_SLV_INTR_IN_91	ADC0_GEN_LEVEL_OUT_0
CPTS0	CPTS0_CPTS_HW1_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_16
	CPTS0_CPTS_HW2_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_17
	CPTS0_CPTS_HW3_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_18
	CPTS0_CPTS_HW4_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_19
	CPTS0_CPTS_HW5_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_20
	CPTS0_CPTS_HW6_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_21
	CPTS0_CPTS_HW7_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_22
	CPTS0_CPTS_HW8_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_23
EPWM0	EPWM0_EPWM_SYNCIN_IN_0	PINFUNCTION_EHRPWM0_SYNCIIN_EHRPWM0_SYNCI_OUT_0
	EPWM0_EPWM_SYNCIN_IN_0	CMP_EVENT_INTROUTER0_OUTP_OUT_40
	EPWM0_EPWM_SYNCIN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_38
	EPWM0_EPWM_SYNCIN_IN_0	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6
	EPWM0_EPWM_SYNCIN_IN_0	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_6
EPWM1	EPWM1_EPWM_SYNCIN_IN_0	EPWM0_EPWM_SYNCOUT_OUT_0
EPWM2	EPWM2_EPWM_SYNCIN_IN_0	EPWM1_EPWM_SYNCOUT_OUT_0
EPWM3	EPWM3_EPWM_SYNCIN_IN_0	PINFUNCTION_EHRPWM3_SYNCIIN_EHRPWM3_SYNCI_OUT_0
	EPWM3_EPWM_SYNCIN_IN_0	CMP_EVENT_INTROUTER0_OUTP_OUT_41
	EPWM3_EPWM_SYNCIN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_39
	EPWM3_EPWM_SYNCIN_IN_0	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	EPWM3_EPWM_SYNCIN_IN_0	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_7
	EPWM3_EPWM_SYNCIN_IN_0	EPWM2_EPWM_SYNCOUT_OUT_0
EPWM4	EPWM4_EPWM_SYNCIN_IN_0	EPWM3_EPWM_SYNCOUT_OUT_0
EPWM5	EPWM5_EPWM_SYNCIN_IN_0	EPWM4_EPWM_SYNCOUT_OUT_0
EPWM6	EPWM6_EPWM_SYNCIN_IN_0	PINFUNCTION_EHRPWM6_SYNCIIN_EHRPWM6_SYNCI_OUT_0
	EPWM6_EPWM_SYNCIN_IN_0	CMP_EVENT_INTROUTER0_OUTP_OUT_42
	EPWM6_EPWM_SYNCIN_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_40
	EPWM6_EPWM_SYNCIN_IN_0	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	EPWM6_EPWM_SYNCIN_IN_0	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_7
	EPWM6_EPWM_SYNCIN_IN_0	EPWM5_EPWM_SYNCOUT_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
EPWM7	EPWM7_EPWM_SYNCIN_IN_0	EPWM6_EPWM_SYNCOUT_OUT_0
EPWM8	EPWM8_EPWM_SYNCIN_IN_0	EPWM7_EPWM_SYNCOUT_OUT_0
PCIE0	PCIE0_PCIE_CPTS_HW2_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_29
PDMA0	PDMA0_SPI_MAIN_0_RX_IN_0	MCSPI0_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_0_RX_IN_1	MCSPI0_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_0_RX_IN_2	MCSPI0_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_0_RX_IN_3	MCSPI0_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_0_TX_IN_0	MCSPI0_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_0_TX_IN_1	MCSPI0_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_0_TX_IN_2	MCSPI0_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_0_TX_IN_3	MCSPI0_DMA_WRITE_EVENT_OUT_3
	PDMA0_SPI_MAIN_1_RX_IN_0	MCSPI1_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_1_RX_IN_1	MCSPI1_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_1_RX_IN_2	MCSPI1_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_1_RX_IN_3	MCSPI1_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_1_TX_IN_0	MCSPI1_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_1_TX_IN_1	MCSPI1_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_1_TX_IN_2	MCSPI1_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_1_TX_IN_3	MCSPI1_DMA_WRITE_EVENT_OUT_3
	PDMA0_SPI_MAIN_2_RX_IN_0	MCSPI2_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_2_RX_IN_1	MCSPI2_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_2_RX_IN_2	MCSPI2_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_2_RX_IN_3	MCSPI2_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_2_TX_IN_0	MCSPI2_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_2_TX_IN_1	MCSPI2_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_2_TX_IN_2	MCSPI2_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_2_TX_IN_3	MCSPI2_DMA_WRITE_EVENT_OUT_3
	PDMA0_SPI_MAIN_3_RX_IN_0	MCSPI3_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_3_RX_IN_1	MCSPI3_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_3_RX_IN_2	MCSPI3_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_3_RX_IN_3	MCSPI3_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_3_TX_IN_0	MCSPI3_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_3_TX_IN_1	MCSPI3_DMA_WRITE_EVENT_OUT_1

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PDMA0	PDMA0_SPI_MAIN_3_TX_IN_2	MCSPI3_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_3_TX_IN_3	MCSPI3_DMA_WRITE_EVENT_OUT_3
	PDMA0_USART_MAIN_0_RX_IN_0	UART0_USART_DMA_OUT_1
	PDMA0_USART_MAIN_0_TX_IN_0	UART0_USART_DMA_OUT_0
	PDMA0_USART_MAIN_1_RX_IN_0	UART1_USART_DMA_OUT_1
	PDMA0_USART_MAIN_1_TX_IN_0	UART1_USART_DMA_OUT_0
PDMA1	PDMA1_ADC12_MAIN_0_RX_IN_0	ADC0_FIFO0_LEVEL_OUT_0
	PDMA1_ADC12_MAIN_0_RX_IN_1	ADC0_FIFO1_LEVEL_OUT_0
	PDMA1_MCANSS_0_FE_IN_0	MCAN0_MCANSS_FE_OUT_0
	PDMA1_MCANSS_0_FE_IN_1	MCAN0_MCANSS_FE_OUT_1
	PDMA1_MCANSS_0_FE_IN_2	MCAN0_MCANSS_FE_OUT_2
	PDMA1_MCANSS_1_FE_IN_0	MCAN1_MCANSS_FE_OUT_0
	PDMA1_MCANSS_1_FE_IN_1	MCAN1_MCANSS_FE_OUT_1
	PDMA1_MCANSS_1_FE_IN_2	MCAN1_MCANSS_FE_OUT_2
	PDMA1_MCANSS_MAIN_0_TX_IN_0	MCAN0_MCANSS_TX_DMA_OUT_0
	PDMA1_MCANSS_MAIN_0_TX_IN_1	MCAN0_MCANSS_TX_DMA_OUT_1
	PDMA1_MCANSS_MAIN_0_TX_IN_2	MCAN0_MCANSS_TX_DMA_OUT_2
	PDMA1_MCANSS_MAIN_1_TX_IN_0	MCAN1_MCANSS_TX_DMA_OUT_0
	PDMA1_MCANSS_MAIN_1_TX_IN_1	MCAN1_MCANSS_TX_DMA_OUT_1
	PDMA1_MCANSS_MAIN_1_TX_IN_2	MCAN1_MCANSS_TX_DMA_OUT_2
	PDMA1_SPI_MAIN_4_RX_IN_0	MCSPI4_DMA_READ_EVENT_OUT_0
	PDMA1_SPI_MAIN_4_RX_IN_1	MCSPI4_DMA_READ_EVENT_OUT_1
	PDMA1_SPI_MAIN_4_RX_IN_2	MCSPI4_DMA_READ_EVENT_OUT_2
	PDMA1_SPI_MAIN_4_RX_IN_3	MCSPI4_DMA_READ_EVENT_OUT_3
	PDMA1_SPI_MAIN_4_TX_IN_0	MCSPI4_DMA_WRITE_EVENT_OUT_0
	PDMA1_SPI_MAIN_4_TX_IN_1	MCSPI4_DMA_WRITE_EVENT_OUT_1
	PDMA1_SPI_MAIN_4_TX_IN_2	MCSPI4_DMA_WRITE_EVENT_OUT_2
	PDMA1_SPI_MAIN_4_TX_IN_3	MCSPI4_DMA_WRITE_EVENT_OUT_3
	PDMA1_USART_MAIN_2_RX_IN_0	UART2_USART_DMA_OUT_1
	PDMA1_USART_MAIN_2_TX_IN_0	UART2_USART_DMA_OUT_0
	PDMA1_USART_MAIN_3_RX_IN_0	UART3_USART_DMA_OUT_1
	PDMA1_USART_MAIN_3_TX_IN_0	UART3_USART_DMA_OUT_0
	PDMA1_USART_MAIN_4_RX_IN_0	UART4_USART_DMA_OUT_1

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PDMA1	PDMA1_USART_MAIN_4_TX_IN_0	UART4_USART_DMA_OUT_0
	PDMA1_USART_MAIN_5_RX_IN_0	UART5_USART_DMA_OUT_1
	PDMA1_USART_MAIN_5_TX_IN_0	UART5_USART_DMA_OUT_0
	PDMA1_USART_MAIN_6_RX_IN_0	UART6_USART_DMA_OUT_1
	PDMA1_USART_MAIN_6_TX_IN_0	UART6_USART_DMA_OUT_0
R5FSS0_CORE0	R5FSS0_CORE0_INTR_IN_0	RTI8_INTR_WWD_OUT_0
	R5FSS0_CORE0_INTR_IN_1	DMSC0_AES_0_HIB_PUBLIC_OUT_0
	R5FSS0_CORE0_INTR_IN_2	DMSC0_AES_0_HIB_SECURE_OUT_0
	R5FSS0_CORE0_INTR_IN_3	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_4	R5FSS0_CORE0_EXP_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_5	R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0
	R5FSS0_CORE0_INTR_IN_6	R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0
	R5FSS0_CORE0_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72
	R5FSS0_CORE0_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73
	R5FSS0_CORE0_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74
	R5FSS0_CORE0_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75
	R5FSS0_CORE0_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76
	R5FSS0_CORE0_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77
	R5FSS0_CORE0_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78
	R5FSS0_CORE0_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79
	R5FSS0_CORE0_INTR_IN_16	FSIRX0_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE0_INTR_IN_17	FSIRX0_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE0_INTR_IN_18	FSIRX1_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE0_INTR_IN_19	FSIRX1_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE0_INTR_IN_20	FSIRX2_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE0_INTR_IN_21	FSIRX2_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE0_INTR_IN_22	FSIRX3_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE0_INTR_IN_23	FSIRX3_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE0_INTR_IN_24	FSIRX4_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE0_INTR_IN_25	FSIRX4_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE0_INTR_IN_26	FSIRX5_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE0_INTR_IN_27	FSIRX5_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE0_INTR_IN_28	FSITX0_FSI_TX_OINT1_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE0	R5FSS0_CORE0_INTR_IN_29	FSITX0_FSI_TX_OINT2_OUT_0
	R5FSS0_CORE0_INTR_IN_30	FSITX1_FSI_TX_OINT1_OUT_0
	R5FSS0_CORE0_INTR_IN_31	FSITX1_FSI_TX_OINT2_OUT_0
	R5FSS0_CORE0_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	R5FSS0_CORE0_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	R5FSS0_CORE0_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	R5FSS0_CORE0_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	R5FSS0_CORE0_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	R5FSS0_CORE0_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	R5FSS0_CORE0_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	R5FSS0_CORE0_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	R5FSS0_CORE0_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	R5FSS0_CORE0_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	R5FSS0_CORE0_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	R5FSS0_CORE0_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
	R5FSS0_CORE0_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	R5FSS0_CORE0_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	R5FSS0_CORE0_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	R5FSS0_CORE0_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	R5FSS0_CORE0_INTR_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_16
	R5FSS0_CORE0_INTR_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_17
	R5FSS0_CORE0_INTR_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_18
	R5FSS0_CORE0_INTR_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_19
	R5FSS0_CORE0_INTR_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_20
	R5FSS0_CORE0_INTR_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_21
	R5FSS0_CORE0_INTR_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_22
	R5FSS0_CORE0_INTR_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_23
	R5FSS0_CORE0_INTR_IN_56	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0
	R5FSS0_CORE0_INTR_IN_57	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1
	R5FSS0_CORE0_INTR_IN_58	R5FSS0_CORE0_PMU_OUT_0
	R5FSS0_CORE0_INTR_IN_59	R5FSS0_CORE0_VALFIQ_OUT_0
	R5FSS0_CORE0_INTR_IN_60	R5FSS0_CORE0_VALIRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_61	MCU_I2C0_POINTRPEND_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE0	R5FSS0_CORE0_INTR_IN_62	MCU_I2C1_POINTRPEND_OUT_0
	R5FSS0_CORE0_INTR_IN_63	MCSPI3_INTR_SPI_OUT_0
	R5FSS0_CORE0_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40
	R5FSS0_CORE0_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41
	R5FSS0_CORE0_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42
	R5FSS0_CORE0_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43
	R5FSS0_CORE0_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44
	R5FSS0_CORE0_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45
	R5FSS0_CORE0_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46
	R5FSS0_CORE0_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47
	R5FSS0_CORE0_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48
	R5FSS0_CORE0_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49
	R5FSS0_CORE0_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50
	R5FSS0_CORE0_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51
	R5FSS0_CORE0_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52
	R5FSS0_CORE0_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53
	R5FSS0_CORE0_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54
	R5FSS0_CORE0_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55
	R5FSS0_CORE0_INTR_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56
	R5FSS0_CORE0_INTR_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57
	R5FSS0_CORE0_INTR_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58
	R5FSS0_CORE0_INTR_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59
	R5FSS0_CORE0_INTR_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60
	R5FSS0_CORE0_INTR_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61
	R5FSS0_CORE0_INTR_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62
	R5FSS0_CORE0_INTR_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63
	R5FSS0_CORE0_INTR_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64
	R5FSS0_CORE0_INTR_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65
	R5FSS0_CORE0_INTR_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66
	R5FSS0_CORE0_INTR_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67
	R5FSS0_CORE0_INTR_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68
	R5FSS0_CORE0_INTR_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69
	R5FSS0_CORE0_INTR_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE0	R5FSS0_CORE0_INTR_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71
	R5FSS0_CORE0_INTR_IN_96	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_97	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_98	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_99	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_100	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_103	PCIE0_PCIE_DPA_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	R5FSS0_CORE0_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	R5FSS0_CORE0_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	R5FSS0_CORE0_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	R5FSS0_CORE0_INTR_IN_108	EPWM0_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_109	EPWM0_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_110	EPWM1_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_111	EPWM1_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_112	EPWM2_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_113	EPWM2_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_114	EPWM3_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_115	EPWM3_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_116	EPWM4_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_117	EPWM4_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_118	EPWM5_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_119	CTRL_MMR0_ACCESS_ERR_OUT_0
	R5FSS0_CORE0_INTR_IN_120	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_121	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1
	R5FSS0_CORE0_INTR_IN_122	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2
	R5FSS0_CORE0_INTR_IN_123	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3
	R5FSS0_CORE0_INTR_IN_124	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4
	R5FSS0_CORE0_INTR_IN_125	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5
	R5FSS0_CORE0_INTR_IN_126	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6
	R5FSS0_CORE0_INTR_IN_127	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	R5FSS0_CORE0_INTR_IN_128	ADC0_GEN_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_129	CPTS0_EVNT_PEND_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE0	R5FSS0_CORE0_INTR_IN_130	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	R5FSS0_CORE0_INTR_IN_131	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	R5FSS0_CORE0_INTR_IN_132	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	R5FSS0_CORE0_INTR_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_133	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_137	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_139	EPWM5_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_140	ECAP0_ECAP_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_141	ECAP1_ECAP_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_142	ECAP2_ECAP_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_143	EQEP0_EQEP_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_144	EQEP1_EQEP_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_145	EQEP2_EQEP_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_146	EPWM6_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_147	EPWM6_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_148	EPWM7_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_149	EPWM7_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_150	EPWM8_EPWM_ETINT_OUT_0
	R5FSS0_CORE0_INTR_IN_151	DDR16SS0_DDRSS_CONTROLLER_OUT_0
	R5FSS0_CORE0_INTR_IN_152	TIMER0_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_153	TIMER1_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_154	TIMER2_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_155	TIMER3_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_156	TIMER4_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_157	TIMER5_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_158	TIMER6_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_159	TIMER7_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_160	TIMER8_INTR_PEND_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE0	R5FSS0_CORE0_INTR_IN_161	TIMER9_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_162	TIMER10_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_163	TIMER11_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	R5FSS0_CORE0_INTR_IN_165	MMCSD0_EMMCSS_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_166	MMCSD1_EMMCSDSS_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
	R5FSS0_CORE0_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
	R5FSS0_CORE0_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
	R5FSS0_CORE0_INTR_IN_170	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0
	R5FSS0_CORE0_INTR_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_172	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0
	R5FSS0_CORE0_INTR_IN_173	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0
	R5FSS0_CORE0_INTR_IN_174	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1
	R5FSS0_CORE0_INTR_IN_175	R5FSS0_CORE0_CTI_OUT_0
	R5FSS0_CORE0_INTR_IN_176	R5FSS0_CORE1_CTI_OUT_0
	R5FSS0_CORE0_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_178	EPWM8_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE0_INTR_IN_180	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0
	R5FSS0_CORE0_INTR_IN_181	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	R5FSS0_CORE0_INTR_IN_182	DCC0_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_182	DCC1_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_182	DCC2_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_182	DCC3_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_182	DCC4_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_182	DCC5_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_183	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_184	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_185	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	R5FSS0_CORE0_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	R5FSS0_CORE0_INTR_IN_189	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE0	R5FSS0_CORE0_INTR_IN_190	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	R5FSS0_CORE0_INTR_IN_191	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	R5FSS0_CORE0_INTR_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	R5FSS0_CORE0_INTR_IN_193	I2C0_POINTRPEND_OUT_0
	R5FSS0_CORE0_INTR_IN_194	I2C1_POINTRPEND_OUT_0
	R5FSS0_CORE0_INTR_IN_195	I2C2_POINTRPEND_OUT_0
	R5FSS0_CORE0_INTR_IN_196	I2C3_POINTRPEND_OUT_0
	R5FSS0_CORE0_INTR_IN_197	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_198	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	R5FSS0_CORE0_INTR_IN_199	SA2_UL0_SA_UL_PKA_OUT_0
	R5FSS0_CORE0_INTR_IN_200	SA2_UL0_SA_UL_TRNG_OUT_0
	R5FSS0_CORE0_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_203	PSC0_PSC_ALLINT_OUT_0
	R5FSS0_CORE0_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
	R5FSS0_CORE0_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
	R5FSS0_CORE0_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
	R5FSS0_CORE0_INTR_IN_207	MCSPI4_INTR_SPI_OUT_0
	R5FSS0_CORE0_INTR_IN_208	MCU_MCSPI0_INTR_SPI_OUT_0
	R5FSS0_CORE0_INTR_IN_209	MCU_MCSPI1_INTR_SPI_OUT_0
	R5FSS0_CORE0_INTR_IN_210	UART0_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_211	UART1_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_212	UART2_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_213	UART3_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_214	UART4_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_215	UART5_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_216	UART6_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_217	MCU_UART0_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_218	MCU_UART1_USART_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_219	USB0_HOST_SYSTEM_ERROR_OUT_0
	R5FSS0_CORE0_INTR_IN_220	USB0_IRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_221	USB0_IRQ_OUT_1
	R5FSS0_CORE0_INTR_IN_222	USB0_IRQ_OUT_2

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE0	R5FSS0_CORE0_INTR_IN_223	USB0_IRQ_OUT_3
	R5FSS0_CORE0_INTR_IN_224	USB0_IRQ_OUT_4
	R5FSS0_CORE0_INTR_IN_225	USB0_IRQ_OUT_5
	R5FSS0_CORE0_INTR_IN_226	USB0_IRQ_OUT_6
	R5FSS0_CORE0_INTR_IN_227	USB0_IRQ_OUT_7
	R5FSS0_CORE0_INTR_IN_228	USB0_OTGIRQ_OUT_0
	R5FSS0_CORE0_INTR_IN_229	PCIE0_PCIE_CPTS_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_230	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_231	PCIE0_PCIE_FLR_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_232	PCIE0_PCIE_ERROR_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_233	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_234	PCIE0_PCIE_LEGACY_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_235	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_236	PCIE0_PCIE_LOCAL_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_237	PCIE0_PCIE_PHY_LEVEL_OUT_0
	R5FSS0_CORE0_INTR_IN_238	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0
	R5FSS0_CORE0_INTR_IN_239	GPMC0_GPMC_SINTERRUPT_OUT_0
	R5FSS0_CORE0_INTR_IN_240	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0
	R5FSS0_CORE0_INTR_IN_241	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1
	R5FSS0_CORE0_INTR_IN_242	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0
	R5FSS0_CORE0_INTR_IN_243	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1
	R5FSS0_CORE0_INTR_IN_244	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0
	R5FSS0_CORE0_INTR_IN_245	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1
	R5FSS0_CORE0_INTR_IN_246	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0
	R5FSS0_CORE0_INTR_IN_247	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1
	R5FSS0_CORE0_INTR_IN_248	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0
	R5FSS0_CORE0_INTR_IN_249	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1
	R5FSS0_CORE0_INTR_IN_250	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2
	R5FSS0_CORE0_INTR_IN_251	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3
	R5FSS0_CORE0_INTR_IN_252	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4
	R5FSS0_CORE0_INTR_IN_253	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5
	R5FSS0_CORE0_INTR_IN_254	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6
	R5FSS0_CORE0_INTR_IN_255	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE1	R5FSS0_CORE1_INTR_IN_0	RTI9_INTR_WWD_OUT_0
	R5FSS0_CORE1_INTR_IN_1	DMSC0_AES_0_HIB_PUBLIC_OUT_0
	R5FSS0_CORE1_INTR_IN_2	DMSC0_AES_0_HIB_SECURE_OUT_0
	R5FSS0_CORE1_INTR_IN_3	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_4	R5FSS0_CORE1_EXP_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_5	R5FSS0_COMMON0_COMMRX_LEVEL_1_OUT_0
	R5FSS0_CORE1_INTR_IN_6	R5FSS0_COMMON0_COMMTX_LEVEL_1_OUT_0
	R5FSS0_CORE1_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_80
	R5FSS0_CORE1_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_81
	R5FSS0_CORE1_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_82
	R5FSS0_CORE1_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_83
	R5FSS0_CORE1_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_84
	R5FSS0_CORE1_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_85
	R5FSS0_CORE1_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_86
	R5FSS0_CORE1_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_87
	R5FSS0_CORE1_INTR_IN_16	FSIRX0_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE1_INTR_IN_17	FSIRX0_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE1_INTR_IN_18	FSIRX1_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE1_INTR_IN_19	FSIRX1_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE1_INTR_IN_20	FSIRX2_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE1_INTR_IN_21	FSIRX2_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE1_INTR_IN_22	FSIRX3_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE1_INTR_IN_23	FSIRX3_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE1_INTR_IN_24	FSIRX4_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE1_INTR_IN_25	FSIRX4_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE1_INTR_IN_26	FSIRX5_FSI_RX_OINT1_OUT_0
	R5FSS0_CORE1_INTR_IN_27	FSIRX5_FSI_RX_OINT2_OUT_0
	R5FSS0_CORE1_INTR_IN_28	FSITX0_FSI_TX_OINT1_OUT_0
	R5FSS0_CORE1_INTR_IN_29	FSITX0_FSI_TX_OINT2_OUT_0
	R5FSS0_CORE1_INTR_IN_30	FSITX1_FSI_TX_OINT1_OUT_0
	R5FSS0_CORE1_INTR_IN_31	FSITX1_FSI_TX_OINT2_OUT_0
	R5FSS0_CORE1_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	R5FSS0_CORE1_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE1	R5FSS0_CORE1_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	R5FSS0_CORE1_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	R5FSS0_CORE1_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	R5FSS0_CORE1_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	R5FSS0_CORE1_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	R5FSS0_CORE1_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	R5FSS0_CORE1_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	R5FSS0_CORE1_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	R5FSS0_CORE1_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	R5FSS0_CORE1_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
	R5FSS0_CORE1_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	R5FSS0_CORE1_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	R5FSS0_CORE1_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	R5FSS0_CORE1_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	R5FSS0_CORE1_INTR_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_16
	R5FSS0_CORE1_INTR_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_17
	R5FSS0_CORE1_INTR_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_18
	R5FSS0_CORE1_INTR_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_19
	R5FSS0_CORE1_INTR_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_20
	R5FSS0_CORE1_INTR_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_21
	R5FSS0_CORE1_INTR_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_22
	R5FSS0_CORE1_INTR_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_23
	R5FSS0_CORE1_INTR_IN_56	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0
	R5FSS0_CORE1_INTR_IN_57	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1
	R5FSS0_CORE1_INTR_IN_58	R5FSS0_CORE1_PMU_OUT_0
	R5FSS0_CORE1_INTR_IN_59	R5FSS0_CORE1_VALFIQ_OUT_0
	R5FSS0_CORE1_INTR_IN_60	R5FSS0_CORE1_VALIRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_61	MCU_I2C0_POINTRPEND_OUT_0
	R5FSS0_CORE1_INTR_IN_62	MCU_I2C1_POINTRPEND_OUT_0
	R5FSS0_CORE1_INTR_IN_63	MCSPI3_INTR_SPI_OUT_0
	R5FSS0_CORE1_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40
	R5FSS0_CORE1_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41
	R5FSS0_CORE1_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE1	R5FSS0_CORE1_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43
	R5FSS0_CORE1_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44
	R5FSS0_CORE1_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45
	R5FSS0_CORE1_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46
	R5FSS0_CORE1_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47
	R5FSS0_CORE1_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48
	R5FSS0_CORE1_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49
	R5FSS0_CORE1_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50
	R5FSS0_CORE1_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51
	R5FSS0_CORE1_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52
	R5FSS0_CORE1_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53
	R5FSS0_CORE1_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54
	R5FSS0_CORE1_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55
	R5FSS0_CORE1_INTR_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56
	R5FSS0_CORE1_INTR_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57
	R5FSS0_CORE1_INTR_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58
	R5FSS0_CORE1_INTR_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59
	R5FSS0_CORE1_INTR_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60
	R5FSS0_CORE1_INTR_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61
	R5FSS0_CORE1_INTR_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62
	R5FSS0_CORE1_INTR_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63
	R5FSS0_CORE1_INTR_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64
	R5FSS0_CORE1_INTR_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65
	R5FSS0_CORE1_INTR_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66
	R5FSS0_CORE1_INTR_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67
	R5FSS0_CORE1_INTR_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68
	R5FSS0_CORE1_INTR_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69
	R5FSS0_CORE1_INTR_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70
	R5FSS0_CORE1_INTR_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71
	R5FSS0_CORE1_INTR_IN_96	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_1
	R5FSS0_CORE1_INTR_IN_97	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_1
	R5FSS0_CORE1_INTR_IN_98	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_1
	R5FSS0_CORE1_INTR_IN_99	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_1

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE1	R5FSS0_CORE1_INTR_IN_100	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_1
	R5FSS0_CORE1_INTR_IN_103	PCIE0_PCIE_DPA_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	R5FSS0_CORE1_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	R5FSS0_CORE1_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	R5FSS0_CORE1_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	R5FSS0_CORE1_INTR_IN_108	EPWM0_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_109	EPWM0_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_110	EPWM1_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_111	EPWM1_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_112	EPWM2_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_113	EPWM2_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_114	EPWM3_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_115	EPWM3_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_116	EPWM4_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_117	EPWM4_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_118	EPWM5_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_119	CTRL_MMR0_ACCESS_ERR_OUT_0
	R5FSS0_CORE1_INTR_IN_120	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_121	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1
	R5FSS0_CORE1_INTR_IN_122	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2
	R5FSS0_CORE1_INTR_IN_123	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3
	R5FSS0_CORE1_INTR_IN_124	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4
	R5FSS0_CORE1_INTR_IN_125	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5
	R5FSS0_CORE1_INTR_IN_126	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6
	R5FSS0_CORE1_INTR_IN_127	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	R5FSS0_CORE1_INTR_IN_128	ADC0_GEN_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_129	CPTS0_EVNT_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_130	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	R5FSS0_CORE1_INTR_IN_131	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	R5FSS0_CORE1_INTR_IN_132	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	R5FSS0_CORE1_INTR_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE1	R5FSS0_CORE1_INTR_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_133	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_137	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_139	EPWM5_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_140	ECAP0_ECAP_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_141	ECAP1_ECAP_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_142	ECAP2_ECAP_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_143	EQEP0_EQEP_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_144	EQEP1_EQEP_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_145	EQEP2_EQEP_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_146	EPWM6_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_147	EPWM6_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_148	EPWM7_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_149	EPWM7_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_150	EPWM8_EPWM_ETINT_OUT_0
	R5FSS0_CORE1_INTR_IN_151	DDR16SS0_DDRSS_CONTROLLER_OUT_0
	R5FSS0_CORE1_INTR_IN_152	TIMER0_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_153	TIMER1_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_154	TIMER2_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_155	TIMER3_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_156	TIMER4_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_157	TIMER5_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_158	TIMER6_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_159	TIMER7_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_160	TIMER8_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_161	TIMER9_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_162	TIMER10_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_163	TIMER11_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	R5FSS0_CORE1_INTR_IN_165	MMCSD0_EMMCSS_INTR_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE1	R5FSS0_CORE1_INTR_IN_166	MMCSD1_EMMCSDSS_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
	R5FSS0_CORE1_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
	R5FSS0_CORE1_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
	R5FSS0_CORE1_INTR_IN_170	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0
	R5FSS0_CORE1_INTR_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_172	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0
	R5FSS0_CORE1_INTR_IN_173	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0
	R5FSS0_CORE1_INTR_IN_174	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1
	R5FSS0_CORE1_INTR_IN_175	R5FSS0_CORE0_CTI_OUT_0
	R5FSS0_CORE1_INTR_IN_176	R5FSS0_CORE1_CTI_OUT_0
	R5FSS0_CORE1_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_178	EPWM8_EPWM_TRIPZINT_OUT_0
	R5FSS0_CORE1_INTR_IN_180	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0
	R5FSS0_CORE1_INTR_IN_181	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	R5FSS0_CORE1_INTR_IN_182	DCC0_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_182	DCC1_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_182	DCC2_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_182	DCC3_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_182	DCC4_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_182	DCC5_INTR_DONE_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_183	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_184	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_185	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	R5FSS0_CORE1_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	R5FSS0_CORE1_INTR_IN_189	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_190	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	R5FSS0_CORE1_INTR_IN_191	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	R5FSS0_CORE1_INTR_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	R5FSS0_CORE1_INTR_IN_193	I2C0_POINTRPEND_OUT_0
	R5FSS0_CORE1_INTR_IN_194	I2C1_POINTRPEND_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE1	R5FSS0_CORE1_INTR_IN_195	I2C2_POINTRPEND_OUT_0
	R5FSS0_CORE1_INTR_IN_196	I2C3_POINTRPEND_OUT_0
	R5FSS0_CORE1_INTR_IN_197	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_198	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	R5FSS0_CORE1_INTR_IN_199	SA2_UL0_SA_UL_PKA_OUT_0
	R5FSS0_CORE1_INTR_IN_200	SA2_UL0_SA_UL_TRNG_OUT_0
	R5FSS0_CORE1_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_203	PSC0_PSC_ALLINT_OUT_0
	R5FSS0_CORE1_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
	R5FSS0_CORE1_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
	R5FSS0_CORE1_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
	R5FSS0_CORE1_INTR_IN_207	MCSPI4_INTR_SPI_OUT_0
	R5FSS0_CORE1_INTR_IN_208	MCU_MCSPI0_INTR_SPI_OUT_0
	R5FSS0_CORE1_INTR_IN_209	MCU_MCSPI1_INTR_SPI_OUT_0
	R5FSS0_CORE1_INTR_IN_210	UART0_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_211	UART1_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_212	UART2_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_213	UART3_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_214	UART4_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_215	UART5_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_216	UART6_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_217	MCU_UART0_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_218	MCU_UART1_USART_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_219	USB0_HOST_SYSTEM_ERROR_OUT_0
	R5FSS0_CORE1_INTR_IN_220	USB0_IRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_221	USB0_IRQ_OUT_1
	R5FSS0_CORE1_INTR_IN_222	USB0_IRQ_OUT_2
	R5FSS0_CORE1_INTR_IN_223	USB0_IRQ_OUT_3
	R5FSS0_CORE1_INTR_IN_224	USB0_IRQ_OUT_4
	R5FSS0_CORE1_INTR_IN_225	USB0_IRQ_OUT_5
	R5FSS0_CORE1_INTR_IN_226	USB0_IRQ_OUT_6
	R5FSS0_CORE1_INTR_IN_227	USB0_IRQ_OUT_7

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS0_CORE1	R5FSS0_CORE1_INTR_IN_228	USB0_OTGIRQ_OUT_0
	R5FSS0_CORE1_INTR_IN_229	PCIE0_PCIE_CPTS_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_230	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_231	PCIE0_PCIE_FLR_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_232	PCIE0_PCIE_ERROR_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_233	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_234	PCIE0_PCIE_LEGACY_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_235	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_236	PCIE0_PCIE_LOCAL_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_237	PCIE0_PCIE_PHY_LEVEL_OUT_0
	R5FSS0_CORE1_INTR_IN_238	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0
	R5FSS0_CORE1_INTR_IN_239	GPMC0_GPMC_SINTERRUPT_OUT_0
	R5FSS0_CORE1_INTR_IN_240	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0
	R5FSS0_CORE1_INTR_IN_241	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1
	R5FSS0_CORE1_INTR_IN_242	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0
	R5FSS0_CORE1_INTR_IN_243	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1
	R5FSS0_CORE1_INTR_IN_244	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0
	R5FSS0_CORE1_INTR_IN_245	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1
	R5FSS0_CORE1_INTR_IN_246	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0
	R5FSS0_CORE1_INTR_IN_247	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1
	R5FSS0_CORE1_INTR_IN_248	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0
	R5FSS0_CORE1_INTR_IN_249	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1
	R5FSS0_CORE1_INTR_IN_250	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2
	R5FSS0_CORE1_INTR_IN_251	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3
	R5FSS0_CORE1_INTR_IN_252	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4
	R5FSS0_CORE1_INTR_IN_253	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5
	R5FSS0_CORE1_INTR_IN_254	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6
	R5FSS0_CORE1_INTR_IN_255	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_0	RTI10_INTR_WWD_OUT_0
	R5FSS1_CORE0_INTR_IN_1	DMSC0_AES_0_HIB_PUBLIC_OUT_0
	R5FSS1_CORE0_INTR_IN_2	DMSC0_AES_0_HIB_SECURE_OUT_0
	R5FSS1_CORE0_INTR_IN_3	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_4	R5FSS1_CORE0_EXP_INTR_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_5	R5FSS1_COMMON0_COMMRX_LEVEL_0_OUT_0
	R5FSS1_CORE0_INTR_IN_6	R5FSS1_COMMON0_COMMTX_LEVEL_0_OUT_0
	R5FSS1_CORE0_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_120
	R5FSS1_CORE0_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_121
	R5FSS1_CORE0_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_122
	R5FSS1_CORE0_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_123
	R5FSS1_CORE0_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_124
	R5FSS1_CORE0_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_125
	R5FSS1_CORE0_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_126
	R5FSS1_CORE0_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_127
	R5FSS1_CORE0_INTR_IN_16	FSIRX0_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE0_INTR_IN_17	FSIRX0_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE0_INTR_IN_18	FSIRX1_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE0_INTR_IN_19	FSIRX1_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE0_INTR_IN_20	FSIRX2_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE0_INTR_IN_21	FSIRX2_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE0_INTR_IN_22	FSIRX3_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE0_INTR_IN_23	FSIRX3_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE0_INTR_IN_24	FSIRX4_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE0_INTR_IN_25	FSIRX4_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE0_INTR_IN_26	FSIRX5_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE0_INTR_IN_27	FSIRX5_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE0_INTR_IN_28	FSITX0_FSI_TX_OINT1_OUT_0
	R5FSS1_CORE0_INTR_IN_29	FSITX0_FSI_TX_OINT2_OUT_0
	R5FSS1_CORE0_INTR_IN_30	FSITX1_FSI_TX_OINT1_OUT_0
	R5FSS1_CORE0_INTR_IN_31	FSITX1_FSI_TX_OINT2_OUT_0
	R5FSS1_CORE0_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	R5FSS1_CORE0_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	R5FSS1_CORE0_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	R5FSS1_CORE0_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	R5FSS1_CORE0_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	R5FSS1_CORE0_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	R5FSS1_CORE0_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	R5FSS1_CORE0_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	R5FSS1_CORE0_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	R5FSS1_CORE0_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	R5FSS1_CORE0_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
	R5FSS1_CORE0_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	R5FSS1_CORE0_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	R5FSS1_CORE0_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	R5FSS1_CORE0_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	R5FSS1_CORE0_INTR_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_24
	R5FSS1_CORE0_INTR_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_25
	R5FSS1_CORE0_INTR_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_26
	R5FSS1_CORE0_INTR_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_27
	R5FSS1_CORE0_INTR_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_28
	R5FSS1_CORE0_INTR_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_29
	R5FSS1_CORE0_INTR_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_30
	R5FSS1_CORE0_INTR_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_31
	R5FSS1_CORE0_INTR_IN_56	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0
	R5FSS1_CORE0_INTR_IN_57	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1
	R5FSS1_CORE0_INTR_IN_58	R5FSS1_CORE0_PMU_OUT_0
	R5FSS1_CORE0_INTR_IN_59	R5FSS1_CORE0_VALFIQ_OUT_0
	R5FSS1_CORE0_INTR_IN_60	R5FSS1_CORE0_VALIRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_61	MCU_I2C0_POINTRPEND_OUT_0
	R5FSS1_CORE0_INTR_IN_62	MCU_I2C1_POINTRPEND_OUT_0
	R5FSS1_CORE0_INTR_IN_63	MCSPI3_INTR_SPI_OUT_0
	R5FSS1_CORE0_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88
	R5FSS1_CORE0_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89
	R5FSS1_CORE0_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90
	R5FSS1_CORE0_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91
	R5FSS1_CORE0_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92
	R5FSS1_CORE0_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93
	R5FSS1_CORE0_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94
	R5FSS1_CORE0_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96
	R5FSS1_CORE0_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97
	R5FSS1_CORE0_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98
	R5FSS1_CORE0_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99
	R5FSS1_CORE0_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_100
	R5FSS1_CORE0_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_101
	R5FSS1_CORE0_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_102
	R5FSS1_CORE0_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_103
	R5FSS1_CORE0_INTR_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_104
	R5FSS1_CORE0_INTR_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_105
	R5FSS1_CORE0_INTR_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_106
	R5FSS1_CORE0_INTR_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_107
	R5FSS1_CORE0_INTR_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_108
	R5FSS1_CORE0_INTR_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_109
	R5FSS1_CORE0_INTR_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_110
	R5FSS1_CORE0_INTR_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_111
	R5FSS1_CORE0_INTR_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_112
	R5FSS1_CORE0_INTR_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_113
	R5FSS1_CORE0_INTR_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_114
	R5FSS1_CORE0_INTR_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_115
	R5FSS1_CORE0_INTR_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_116
	R5FSS1_CORE0_INTR_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_117
	R5FSS1_CORE0_INTR_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_118
	R5FSS1_CORE0_INTR_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_119
	R5FSS1_CORE0_INTR_IN_96	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_2
	R5FSS1_CORE0_INTR_IN_97	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_2
	R5FSS1_CORE0_INTR_IN_98	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_99	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_100	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_103	PCIE0_PCIE_DPA_PULSE_OUT_0
	R5FSS1_CORE0_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	R5FSS1_CORE0_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	R5FSS1_CORE0_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	R5FSS1_CORE0_INTR_IN_108	EPWM0_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_109	EPWM0_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_110	EPWM1_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_111	EPWM1_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_112	EPWM2_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_113	EPWM2_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_114	EPWM3_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_115	EPWM3_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_116	EPWM4_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_117	EPWM4_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_118	EPWM5_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_119	CTRL_MMR0_ACCESS_ERR_OUT_0
	R5FSS1_CORE0_INTR_IN_120	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_121	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1
	R5FSS1_CORE0_INTR_IN_122	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2
	R5FSS1_CORE0_INTR_IN_123	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3
	R5FSS1_CORE0_INTR_IN_124	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4
	R5FSS1_CORE0_INTR_IN_125	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5
	R5FSS1_CORE0_INTR_IN_126	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6
	R5FSS1_CORE0_INTR_IN_127	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	R5FSS1_CORE0_INTR_IN_128	ADC0_GEN_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_129	CPTS0_EVNT_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_130	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	R5FSS1_CORE0_INTR_IN_131	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	R5FSS1_CORE0_INTR_IN_132	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	R5FSS1_CORE0_INTR_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_133	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_136	CPSW0_STAT_PEND_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_137	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_139	EPWM5_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_140	ECAP0_ECAP_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_141	ECAP1_ECAP_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_142	ECAP2_ECAP_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_143	EQEP0_EQEP_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_144	EQEP1_EQEP_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_145	EQEP2_EQEP_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_146	EPWM6_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_147	EPWM6_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_148	EPWM7_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_149	EPWM7_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_150	EPWM8_EPWM_ETINT_OUT_0
	R5FSS1_CORE0_INTR_IN_151	DDR16SS0_DDRSS_CONTROLLER_OUT_0
	R5FSS1_CORE0_INTR_IN_152	TIMER0_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_153	TIMER1_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_154	TIMER2_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_155	TIMER3_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_156	TIMER4_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_157	TIMER5_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_158	TIMER6_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_159	TIMER7_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_160	TIMER8_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_161	TIMER9_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_162	TIMER10_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_163	TIMER11_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	R5FSS1_CORE0_INTR_IN_165	MMCSD0_EMMCSS_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_166	MMCSD1_EMMCSDSS_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
	R5FSS1_CORE0_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
	R5FSS1_CORE0_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
	R5FSS1_CORE0_INTR_IN_170	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_172	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0
	R5FSS1_CORE0_INTR_IN_173	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0
	R5FSS1_CORE0_INTR_IN_174	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1
	R5FSS1_CORE0_INTR_IN_175	R5FSS1_CORE0_CTI_OUT_0
	R5FSS1_CORE0_INTR_IN_176	R5FSS1_CORE1_CTI_OUT_0
	R5FSS1_CORE0_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_178	EPWM8_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE0_INTR_IN_180	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0
	R5FSS1_CORE0_INTR_IN_181	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	R5FSS1_CORE0_INTR_IN_182	DCC0_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_182	DCC1_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_182	DCC2_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_182	DCC3_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_182	DCC4_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_182	DCC5_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_183	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_184	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_185	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	R5FSS1_CORE0_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	R5FSS1_CORE0_INTR_IN_189	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_190	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	R5FSS1_CORE0_INTR_IN_191	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	R5FSS1_CORE0_INTR_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	R5FSS1_CORE0_INTR_IN_193	I2C0_POINTRPEND_OUT_0
	R5FSS1_CORE0_INTR_IN_194	I2C1_POINTRPEND_OUT_0
	R5FSS1_CORE0_INTR_IN_195	I2C2_POINTRPEND_OUT_0
	R5FSS1_CORE0_INTR_IN_196	I2C3_POINTRPEND_OUT_0
	R5FSS1_CORE0_INTR_IN_197	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0
	R5FSS1_CORE0_INTR_IN_198	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	R5FSS1_CORE0_INTR_IN_199	SA2_UL0_SA_UL_PKA_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_200	SA2_UL0_SA_UL_TRNG_OUT_0
	R5FSS1_CORE0_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_203	PSC0_PSC_ALLINT_OUT_0
	R5FSS1_CORE0_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
	R5FSS1_CORE0_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
	R5FSS1_CORE0_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
	R5FSS1_CORE0_INTR_IN_207	MCSPI4_INTR_SPI_OUT_0
	R5FSS1_CORE0_INTR_IN_208	MCU_MCSPI0_INTR_SPI_OUT_0
	R5FSS1_CORE0_INTR_IN_209	MCU_MCSPI1_INTR_SPI_OUT_0
	R5FSS1_CORE0_INTR_IN_210	UART0_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_211	UART1_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_212	UART2_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_213	UART3_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_214	UART4_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_215	UART5_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_216	UART6_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_217	MCU_UART0_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_218	MCU_UART1_USART_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_219	USB0_HOST_SYSTEM_ERROR_OUT_0
	R5FSS1_CORE0_INTR_IN_220	USB0_IRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_221	USB0_IRQ_OUT_1
	R5FSS1_CORE0_INTR_IN_222	USB0_IRQ_OUT_2
	R5FSS1_CORE0_INTR_IN_223	USB0_IRQ_OUT_3
	R5FSS1_CORE0_INTR_IN_224	USB0_IRQ_OUT_4
	R5FSS1_CORE0_INTR_IN_225	USB0_IRQ_OUT_5
	R5FSS1_CORE0_INTR_IN_226	USB0_IRQ_OUT_6
	R5FSS1_CORE0_INTR_IN_227	USB0_IRQ_OUT_7
	R5FSS1_CORE0_INTR_IN_228	USB0_OTGIRQ_OUT_0
	R5FSS1_CORE0_INTR_IN_229	PCIE0_PCIE_CPTS_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_230	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0
	R5FSS1_CORE0_INTR_IN_231	PCIE0_PCIE_FLR_PULSE_OUT_0
	R5FSS1_CORE0_INTR_IN_232	PCIE0_PCIE_ERROR_PULSE_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE0	R5FSS1_CORE0_INTR_IN_233	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0
	R5FSS1_CORE0_INTR_IN_234	PCIE0_PCIE_LEGACY_PULSE_OUT_0
	R5FSS1_CORE0_INTR_IN_235	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0
	R5FSS1_CORE0_INTR_IN_236	PCIE0_PCIE_LOCAL_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_237	PCIE0_PCIE_PHY_LEVEL_OUT_0
	R5FSS1_CORE0_INTR_IN_238	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0
	R5FSS1_CORE0_INTR_IN_239	GPMC0_GPMC_SINTERRUPT_OUT_0
	R5FSS1_CORE0_INTR_IN_240	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0
	R5FSS1_CORE0_INTR_IN_241	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1
	R5FSS1_CORE0_INTR_IN_242	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0
	R5FSS1_CORE0_INTR_IN_243	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1
	R5FSS1_CORE0_INTR_IN_244	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0
	R5FSS1_CORE0_INTR_IN_245	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1
	R5FSS1_CORE0_INTR_IN_246	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0
	R5FSS1_CORE0_INTR_IN_247	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1
	R5FSS1_CORE0_INTR_IN_248	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0
	R5FSS1_CORE0_INTR_IN_249	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1
	R5FSS1_CORE0_INTR_IN_250	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2
	R5FSS1_CORE0_INTR_IN_251	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3
	R5FSS1_CORE0_INTR_IN_252	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4
	R5FSS1_CORE0_INTR_IN_253	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5
	R5FSS1_CORE0_INTR_IN_254	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6
	R5FSS1_CORE0_INTR_IN_255	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_0	RTI11_INTR_WWD_OUT_0
	R5FSS1_CORE1_INTR_IN_1	DMSC0_AES_0_HIB_PUBLIC_OUT_0
	R5FSS1_CORE1_INTR_IN_2	DMSC0_AES_0_HIB_SECURE_OUT_0
	R5FSS1_CORE1_INTR_IN_3	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_4	R5FSS1_CORE1_EXP_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_5	R5FSS1_COMMON0_COMMRX_LEVEL_1_OUT_0
	R5FSS1_CORE1_INTR_IN_6	R5FSS1_COMMON0_COMMTX_LEVEL_1_OUT_0
	R5FSS1_CORE1_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_128
	R5FSS1_CORE1_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_129
	R5FSS1_CORE1_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_130

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_131
	R5FSS1_CORE1_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_132
	R5FSS1_CORE1_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_133
	R5FSS1_CORE1_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_134
	R5FSS1_CORE1_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_135
	R5FSS1_CORE1_INTR_IN_16	FSIRX0_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE1_INTR_IN_17	FSIRX0_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE1_INTR_IN_18	FSIRX1_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE1_INTR_IN_19	FSIRX1_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE1_INTR_IN_20	FSIRX2_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE1_INTR_IN_21	FSIRX2_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE1_INTR_IN_22	FSIRX3_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE1_INTR_IN_23	FSIRX3_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE1_INTR_IN_24	FSIRX4_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE1_INTR_IN_25	FSIRX4_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE1_INTR_IN_26	FSIRX5_FSI_RX_OINT1_OUT_0
	R5FSS1_CORE1_INTR_IN_27	FSIRX5_FSI_RX_OINT2_OUT_0
	R5FSS1_CORE1_INTR_IN_28	FSITX0_FSI_TX_OINT1_OUT_0
	R5FSS1_CORE1_INTR_IN_29	FSITX0_FSI_TX_OINT2_OUT_0
	R5FSS1_CORE1_INTR_IN_30	FSITX1_FSI_TX_OINT1_OUT_0
	R5FSS1_CORE1_INTR_IN_31	FSITX1_FSI_TX_OINT2_OUT_0
	R5FSS1_CORE1_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	R5FSS1_CORE1_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	R5FSS1_CORE1_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	R5FSS1_CORE1_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	R5FSS1_CORE1_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	R5FSS1_CORE1_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	R5FSS1_CORE1_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	R5FSS1_CORE1_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	R5FSS1_CORE1_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	R5FSS1_CORE1_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	R5FSS1_CORE1_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	R5FSS1_CORE1_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	R5FSS1_CORE1_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	R5FSS1_CORE1_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	R5FSS1_CORE1_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	R5FSS1_CORE1_INTR_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_24
	R5FSS1_CORE1_INTR_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_25
	R5FSS1_CORE1_INTR_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_26
	R5FSS1_CORE1_INTR_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_27
	R5FSS1_CORE1_INTR_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_28
	R5FSS1_CORE1_INTR_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_29
	R5FSS1_CORE1_INTR_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_30
	R5FSS1_CORE1_INTR_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_31
	R5FSS1_CORE1_INTR_IN_56	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0
	R5FSS1_CORE1_INTR_IN_57	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1
	R5FSS1_CORE1_INTR_IN_58	R5FSS1_CORE1_PMU_OUT_0
	R5FSS1_CORE1_INTR_IN_59	R5FSS1_CORE1_VALFIQ_OUT_0
	R5FSS1_CORE1_INTR_IN_60	R5FSS1_CORE1_VALIRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_61	MCU_I2C0_POINTRPEND_OUT_0
	R5FSS1_CORE1_INTR_IN_62	MCU_I2C1_POINTRPEND_OUT_0
	R5FSS1_CORE1_INTR_IN_63	MCSPI3_INTR_SPI_OUT_0
	R5FSS1_CORE1_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88
	R5FSS1_CORE1_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89
	R5FSS1_CORE1_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90
	R5FSS1_CORE1_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91
	R5FSS1_CORE1_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92
	R5FSS1_CORE1_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93
	R5FSS1_CORE1_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94
	R5FSS1_CORE1_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95
	R5FSS1_CORE1_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96
	R5FSS1_CORE1_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97
	R5FSS1_CORE1_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98
	R5FSS1_CORE1_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99
	R5FSS1_CORE1_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_100

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_101
	R5FSS1_CORE1_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_102
	R5FSS1_CORE1_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_103
	R5FSS1_CORE1_INTR_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_104
	R5FSS1_CORE1_INTR_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_105
	R5FSS1_CORE1_INTR_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_106
	R5FSS1_CORE1_INTR_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_107
	R5FSS1_CORE1_INTR_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_108
	R5FSS1_CORE1_INTR_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_109
	R5FSS1_CORE1_INTR_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_110
	R5FSS1_CORE1_INTR_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_111
	R5FSS1_CORE1_INTR_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_112
	R5FSS1_CORE1_INTR_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_113
	R5FSS1_CORE1_INTR_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_114
	R5FSS1_CORE1_INTR_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_115
	R5FSS1_CORE1_INTR_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_116
	R5FSS1_CORE1_INTR_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_117
	R5FSS1_CORE1_INTR_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_118
	R5FSS1_CORE1_INTR_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_119
	R5FSS1_CORE1_INTR_IN_96	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_3
	R5FSS1_CORE1_INTR_IN_97	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_3
	R5FSS1_CORE1_INTR_IN_98	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_1
	R5FSS1_CORE1_INTR_IN_99	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_1
	R5FSS1_CORE1_INTR_IN_100	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_1
	R5FSS1_CORE1_INTR_IN_103	PCIE0_PCIE_DPA_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	R5FSS1_CORE1_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	R5FSS1_CORE1_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	R5FSS1_CORE1_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	R5FSS1_CORE1_INTR_IN_108	EPWM0_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_109	EPWM0_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE1_INTR_IN_110	EPWM1_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_111	EPWM1_EPWM_TRIPZINT_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_112	EPWM2_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_113	EPWM2_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE1_INTR_IN_114	EPWM3_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_115	EPWM3_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE1_INTR_IN_116	EPWM4_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_117	EPWM4_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE1_INTR_IN_118	EPWM5_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_119	CTRL_MMR0_ACCESS_ERR_OUT_0
	R5FSS1_CORE1_INTR_IN_120	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_121	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1
	R5FSS1_CORE1_INTR_IN_122	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2
	R5FSS1_CORE1_INTR_IN_123	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3
	R5FSS1_CORE1_INTR_IN_124	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4
	R5FSS1_CORE1_INTR_IN_125	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5
	R5FSS1_CORE1_INTR_IN_126	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6
	R5FSS1_CORE1_INTR_IN_127	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7
	R5FSS1_CORE1_INTR_IN_128	ADC0_GEN_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_129	CPTS0_EVNT_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_130	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	R5FSS1_CORE1_INTR_IN_131	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	R5FSS1_CORE1_INTR_IN_132	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	R5FSS1_CORE1_INTR_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_133	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_137	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_139	EPWM5_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE1_INTR_IN_140	ECAP0_ECAP_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_141	ECAP1_ECAP_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_142	ECAP2_ECAP_INT_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_143	EQEP0_EQEP_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_144	EQEP1_EQEP_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_145	EQEP2_EQEP_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_146	EPWM6_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_147	EPWM6_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE1_INTR_IN_148	EPWM7_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_149	EPWM7_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE1_INTR_IN_150	EPWM8_EPWM_ETINT_OUT_0
	R5FSS1_CORE1_INTR_IN_151	DDR16SS0_DDRSS_CONTROLLER_OUT_0
	R5FSS1_CORE1_INTR_IN_152	TIMER0_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_153	TIMER1_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_154	TIMER2_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_155	TIMER3_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_156	TIMER4_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_157	TIMER5_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_158	TIMER6_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_159	TIMER7_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_160	TIMER8_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_161	TIMER9_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_162	TIMER10_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_163	TIMER11_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	R5FSS1_CORE1_INTR_IN_165	MMCSD0_EMMCSS_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_166	MMCSD1_EMMCSDSS_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
	R5FSS1_CORE1_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
	R5FSS1_CORE1_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
	R5FSS1_CORE1_INTR_IN_170	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0
	R5FSS1_CORE1_INTR_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_172	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0
	R5FSS1_CORE1_INTR_IN_173	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0
	R5FSS1_CORE1_INTR_IN_174	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1
	R5FSS1_CORE1_INTR_IN_175	R5FSS1_CORE0_CTI_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_176	R5FSS1_CORE1_CTI_OUT_0
	R5FSS1_CORE1_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_178	EPWM8_EPWM_TRIPZINT_OUT_0
	R5FSS1_CORE1_INTR_IN_180	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0
	R5FSS1_CORE1_INTR_IN_181	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	R5FSS1_CORE1_INTR_IN_182	DCC0_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_182	DCC1_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_182	DCC2_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_182	DCC3_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_182	DCC4_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_182	DCC5_INTR_DONE_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_183	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_184	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_185	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	R5FSS1_CORE1_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	R5FSS1_CORE1_INTR_IN_189	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_190	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	R5FSS1_CORE1_INTR_IN_191	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	R5FSS1_CORE1_INTR_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	R5FSS1_CORE1_INTR_IN_193	I2C0_POINTRPEND_OUT_0
	R5FSS1_CORE1_INTR_IN_194	I2C1_POINTRPEND_OUT_0
	R5FSS1_CORE1_INTR_IN_195	I2C2_POINTRPEND_OUT_0
	R5FSS1_CORE1_INTR_IN_196	I2C3_POINTRPEND_OUT_0
	R5FSS1_CORE1_INTR_IN_197	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_198	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	R5FSS1_CORE1_INTR_IN_199	SA2_UL0_SA_UL_PKA_OUT_0
	R5FSS1_CORE1_INTR_IN_200	SA2_UL0_SA_UL_TRNG_OUT_0
	R5FSS1_CORE1_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_203	PSC0_PSC_ALLINT_OUT_0
	R5FSS1_CORE1_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
	R5FSS1_CORE1_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
	R5FSS1_CORE1_INTR_IN_207	MCSPI4_INTR_SPI_OUT_0
	R5FSS1_CORE1_INTR_IN_208	MCU_MCSPI0_INTR_SPI_OUT_0
	R5FSS1_CORE1_INTR_IN_209	MCU_MCSPI1_INTR_SPI_OUT_0
	R5FSS1_CORE1_INTR_IN_210	UART0_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_211	UART1_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_212	UART2_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_213	UART3_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_214	UART4_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_215	UART5_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_216	UART6_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_217	MCU_UART0_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_218	MCU_UART1_USART_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_219	USB0_HOST_SYSTEM_ERROR_OUT_0
	R5FSS1_CORE1_INTR_IN_220	USB0_IRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_221	USB0_IRQ_OUT_1
	R5FSS1_CORE1_INTR_IN_222	USB0_IRQ_OUT_2
	R5FSS1_CORE1_INTR_IN_223	USB0_IRQ_OUT_3
	R5FSS1_CORE1_INTR_IN_224	USB0_IRQ_OUT_4
	R5FSS1_CORE1_INTR_IN_225	USB0_IRQ_OUT_5
	R5FSS1_CORE1_INTR_IN_226	USB0_IRQ_OUT_6
	R5FSS1_CORE1_INTR_IN_227	USB0_IRQ_OUT_7
	R5FSS1_CORE1_INTR_IN_228	USB0_OTGIRQ_OUT_0
	R5FSS1_CORE1_INTR_IN_229	PCIE0_PCIE_CPTS_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_230	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_231	PCIE0_PCIE_FLR_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_232	PCIE0_PCIE_ERROR_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_233	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_234	PCIE0_PCIE_LEGACY_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_235	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_236	PCIE0_PCIE_LOCAL_LEVEL_OUT_0
	R5FSS1_CORE1_INTR_IN_237	PCIE0_PCIE_PHY_LEVEL_OUT_0

Table 9-62. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_INTR_IN_238	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0
	R5FSS1_CORE1_INTR_IN_239	GPMC0_GPMC_SINTERRUPT_OUT_0
	R5FSS1_CORE1_INTR_IN_240	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0
	R5FSS1_CORE1_INTR_IN_241	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1
	R5FSS1_CORE1_INTR_IN_242	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0
	R5FSS1_CORE1_INTR_IN_243	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1
	R5FSS1_CORE1_INTR_IN_244	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0
	R5FSS1_CORE1_INTR_IN_245	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1
	R5FSS1_CORE1_INTR_IN_246	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0
	R5FSS1_CORE1_INTR_IN_247	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1
	R5FSS1_CORE1_INTR_IN_248	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0
	R5FSS1_CORE1_INTR_IN_249	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1
	R5FSS1_CORE1_INTR_IN_250	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2
	R5FSS1_CORE1_INTR_IN_251	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3
	R5FSS1_CORE1_INTR_IN_252	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4
	R5FSS1_CORE1_INTR_IN_253	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5
	R5FSS1_CORE1_INTR_IN_254	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6
	R5FSS1_CORE1_INTR_IN_255	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7

9.4.2 Interrupts (Outputs)

Table 9-63. Interrupts (Outputs)

Instance	Interrupt Output Line	Destination Interrupt
PINFUNCTION_CPTS0_HW1TSPUSHin	PINFUNCTION_CPTS0_HW1TSPUSHIN_CPTS0_HW1TSPUSH_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_14
PINFUNCTION_CPTS0_HW2TSPUSHin	PINFUNCTION_CPTS0_HW2TSPUSHIN_CPTS0_HW2TSPUSH_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_15
PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHin	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_12
PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHin	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_13
PINFUNCTION_EHRPWM0_SYNCIin	PINFUNCTION_EHRPWM0_SYNCIIN_EHRPWM0_SYNCI_OUT_0	EPWM0_EPWM_SYNCIN_IN_0
PINFUNCTION_EHRPWM3_SYNCIin	PINFUNCTION_EHRPWM3_SYNCIIN_EHRPWM3_SYNCI_OUT_0	EPWM3_EPWM_SYNCIN_IN_0
PINFUNCTION_EHRPWM6_SYNCIin	PINFUNCTION_EHRPWM6_SYNCIIN_EHRPWM6_SYNCI_OUT_0	EPWM6_EPWM_SYNCIN_IN_0
PINFUNCTION_EXTINTnin	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	GICSS0_SPI_IN_256
	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	R5FSS0_CORE0_INTR_IN_198
	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	R5FSS0_CORE1_INTR_IN_198
	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	R5FSS1_CORE0_INTR_IN_198
	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	R5FSS1_CORE1_INTR_IN_198
PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN0in	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN0IN_PRG0_IEP0_EDC_LATCH_IN0_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_4
PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN1in	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN1IN_PRG0_IEP0_EDC_LATCH_IN1_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_5
PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN0in	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN0IN_PRG0_IEP1_EDC_LATCH_IN0_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_6
PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN1in	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN1IN_PRG0_IEP1_EDC_LATCH_IN1_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_7
PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN0in	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN0IN_PRG1_IEP0_EDC_LATCH_IN0_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_8
PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN1in	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN1IN_PRG1_IEP0_EDC_LATCH_IN1_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_9
PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN0in	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN0IN_PRG1_IEP1_EDC_LATCH_IN0_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_10
PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN1in	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN1IN_PRG1_IEP1_EDC_LATCH_IN1_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_11
ADC0	ADC0_ECC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_0
	ADC0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_64
	ADC0_FIFO0_LEVEL_OUT_0	PDMA1_ADC12_MAIN_0_RX_IN_0
	ADC0_FIFO1_LEVEL_OUT_0	PDMA1_ADC12_MAIN_0_RX_IN_1
	ADC0_GEN_LEVEL_OUT_0	GICSS0_SPI_IN_128
	ADC0_GEN_LEVEL_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_91
	ADC0_GEN_LEVEL_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_91
	ADC0_GEN_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_128
	ADC0_GEN_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_128
	ADC0_GEN_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_128
	ADC0_GEN_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_128
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_49

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_4	GICSS0_SPI_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_5	GICSS0_SPI_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_6	GICSS0_SPI_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_7	GICSS0_SPI_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_8	GICSS0_SPI_IN_56
	CMP_EVENT_INTROUTER0_OUTP_OUT_9	GICSS0_SPI_IN_57
	CMP_EVENT_INTROUTER0_OUTP_OUT_10	GICSS0_SPI_IN_58
	CMP_EVENT_INTROUTER0_OUTP_OUT_11	GICSS0_SPI_IN_59
	CMP_EVENT_INTROUTER0_OUTP_OUT_12	GICSS0_SPI_IN_60
	CMP_EVENT_INTROUTER0_OUTP_OUT_13	GICSS0_SPI_IN_61
	CMP_EVENT_INTROUTER0_OUTP_OUT_14	GICSS0_SPI_IN_62
	CMP_EVENT_INTROUTER0_OUTP_OUT_15	GICSS0_SPI_IN_63
	CMP_EVENT_INTROUTER0_OUTP_OUT_16	R5FSS0_CORE0_INTR_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_16	R5FSS0_CORE1_INTR_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_17	R5FSS0_CORE0_INTR_IN_49
	CMP_EVENT_INTROUTER0_OUTP_OUT_17	R5FSS0_CORE1_INTR_IN_49
	CMP_EVENT_INTROUTER0_OUTP_OUT_18	R5FSS0_CORE0_INTR_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_18	R5FSS0_CORE1_INTR_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_19	R5FSS0_CORE0_INTR_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_19	R5FSS0_CORE1_INTR_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_20	R5FSS0_CORE0_INTR_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_20	R5FSS0_CORE1_INTR_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_21	R5FSS0_CORE0_INTR_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_21	R5FSS0_CORE1_INTR_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_22	R5FSS0_CORE0_INTR_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_22	R5FSS0_CORE1_INTR_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_23	R5FSS0_CORE0_INTR_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_23	R5FSS0_CORE1_INTR_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_24	R5FSS1_CORE0_INTR_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_24	R5FSS1_CORE1_INTR_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_25	R5FSS1_CORE0_INTR_IN_49

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_OUTP_OUT_25	R5FSS1_CORE1_INTR_IN_49
	CMP_EVENT_INTROUTER0_OUTP_OUT_26	R5FSS1_CORE0_INTR_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_26	R5FSS1_CORE1_INTR_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_27	R5FSS1_CORE0_INTR_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_27	R5FSS1_CORE1_INTR_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_28	R5FSS1_CORE0_INTR_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_28	R5FSS1_CORE1_INTR_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_29	R5FSS1_CORE0_INTR_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_29	R5FSS1_CORE1_INTR_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_30	R5FSS1_CORE0_INTR_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_30	R5FSS1_CORE1_INTR_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_31	R5FSS1_CORE0_INTR_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_31	R5FSS1_CORE1_INTR_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_32	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_0
	CMP_EVENT_INTROUTER0_OUTP_OUT_33	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_1
	CMP_EVENT_INTROUTER0_OUTP_OUT_34	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_2
	CMP_EVENT_INTROUTER0_OUTP_OUT_35	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_3
	CMP_EVENT_INTROUTER0_OUTP_OUT_36	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_4
	CMP_EVENT_INTROUTER0_OUTP_OUT_37	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_5
	CMP_EVENT_INTROUTER0_OUTP_OUT_38	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_6
	CMP_EVENT_INTROUTER0_OUTP_OUT_39	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_7
	CMP_EVENT_INTROUTER0_OUTP_OUT_40	EPWM0_EPWM_SYNCIN_IN_0
	CMP_EVENT_INTROUTER0_OUTP_OUT_41	EPWM3_EPWM_SYNCIN_IN_0
	CMP_EVENT_INTROUTER0_OUTP_OUT_42	EPWM6_EPWM_SYNCIN_IN_0
CBASS0	CBASS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_133
	CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_133
	CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_133
	CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_133
	CBASS0_DEFAULT_EXP_OUT_0	DMSC0_CORTEX_M3_0_SEC_IN_IN_0
CTRL_MMR0	CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_58
	CTRL_MMR0_ACCESS_ERR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_230
	CTRL_MMR0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_137

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CTRL_MMR0	CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_119
	CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_119
	CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_119
	CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_119
CBASS_DBG0	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_133
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_133
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_133
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_133
CBASS_FW0	CBASS_FW0_DEFAULT_ERR_INTR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_202
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_208
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	R5FSS0_CORE0_INTR_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	R5FSS0_CORE1_INTR_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	R5FSS1_CORE0_INTR_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	R5FSS1_CORE1_INTR_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	DMSC0_CORTEX_M3_0_NVIC_IN_209
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	R5FSS0_CORE0_INTR_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	R5FSS0_CORE1_INTR_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	R5FSS1_CORE0_INTR_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	R5FSS1_CORE1_INTR_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	DMSC0_CORTEX_M3_0_NVIC_IN_210
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	R5FSS0_CORE0_INTR_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	R5FSS0_CORE1_INTR_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	R5FSS1_CORE0_INTR_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	R5FSS1_CORE1_INTR_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	DMSC0_CORTEX_M3_0_NVIC_IN_211
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_35
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	R5FSS0_CORE0_INTR_IN_35
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	R5FSS0_CORE1_INTR_IN_35
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	R5FSS1_CORE0_INTR_IN_35

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	R5FSS1_CORE1_INTR_IN_35
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	DMSC0_CORTEX_M3_0_NVIC_IN_212
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	GICSS0_SPI_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	R5FSS0_CORE0_INTR_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	R5FSS0_CORE1_INTR_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	R5FSS1_CORE0_INTR_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	R5FSS1_CORE1_INTR_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	DMSC0_CORTEX_M3_0_NVIC_IN_213
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	GICSS0_SPI_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	R5FSS0_CORE0_INTR_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	R5FSS0_CORE1_INTR_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	R5FSS1_CORE0_INTR_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	R5FSS1_CORE1_INTR_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	DMSC0_CORTEX_M3_0_NVIC_IN_214
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	GICSS0_SPI_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	R5FSS0_CORE0_INTR_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	R5FSS0_CORE1_INTR_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	R5FSS1_CORE0_INTR_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	R5FSS1_CORE1_INTR_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	DMSC0_CORTEX_M3_0_NVIC_IN_215
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	GICSS0_SPI_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	R5FSS0_CORE0_INTR_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	R5FSS0_CORE1_INTR_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	R5FSS1_CORE0_INTR_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	R5FSS1_CORE1_INTR_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	GICSS0_SPI_IN_40
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	R5FSS0_CORE0_INTR_IN_40
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	R5FSS0_CORE1_INTR_IN_40
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	R5FSS1_CORE0_INTR_IN_40
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	R5FSS1_CORE1_INTR_IN_40
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	GICSS0_SPI_IN_41
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	R5FSS0_CORE0_INTR_IN_41
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	R5FSS0_CORE1_INTR_IN_41

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	R5FSS1_CORE0_INTR_IN_41
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	R5FSS1_CORE1_INTR_IN_41
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	GICSS0_SPI_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	R5FSS0_CORE0_INTR_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	R5FSS0_CORE1_INTR_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	R5FSS1_CORE0_INTR_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	R5FSS1_CORE1_INTR_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	GICSS0_SPI_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	R5FSS0_CORE0_INTR_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	R5FSS0_CORE1_INTR_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	R5FSS1_CORE0_INTR_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	R5FSS1_CORE1_INTR_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	GICSS0_SPI_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	R5FSS0_CORE0_INTR_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	R5FSS0_CORE1_INTR_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	R5FSS1_CORE0_INTR_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	R5FSS1_CORE1_INTR_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	GICSS0_SPI_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	R5FSS0_CORE0_INTR_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	R5FSS0_CORE1_INTR_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	R5FSS1_CORE0_INTR_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	R5FSS1_CORE1_INTR_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	GICSS0_SPI_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	R5FSS0_CORE0_INTR_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	R5FSS0_CORE1_INTR_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	R5FSS1_CORE0_INTR_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	R5FSS1_CORE1_INTR_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	GICSS0_SPI_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	R5FSS0_CORE0_INTR_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	R5FSS0_CORE1_INTR_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	R5FSS1_CORE0_INTR_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	R5FSS1_CORE1_INTR_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_16	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_24

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_17	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_25
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_0
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_0
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_1
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_1
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_2
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_2
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_3
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_3
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_4
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_4
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23	PRU_ICSSG0_PR1_IEP0_CAP_INTR_REQ_IN_5
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23	PRU_ICSSG1_PR1_IEP0_CAP_INTR_REQ_IN_5
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_0
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_0
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_1
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_1
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_2
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_2
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_3
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_3
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_4
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_4
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29	PRU_ICSSG0_PR1_IEP1_CAP_INTR_REQ_IN_5
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29	PRU_ICSSG1_PR1_IEP1_CAP_INTR_REQ_IN_5
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_16
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_17
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_32	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_18
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_33	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_19
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_20
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_21
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_36	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_22
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_37	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_23

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_38	PRU_ICSSG0_PR1_SLV_INTR_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_39	PRU_ICSSG0_PR1_SLV_INTR_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_40	PRU_ICSSG0_PR1_SLV_INTR_IN_48
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_41	PRU_ICSSG0_PR1_SLV_INTR_IN_49
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_42	PRU_ICSSG0_PR1_SLV_INTR_IN_50
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_43	PRU_ICSSG0_PR1_SLV_INTR_IN_51
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_44	PRU_ICSSG0_PR1_SLV_INTR_IN_52
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_45	PRU_ICSSG0_PR1_SLV_INTR_IN_53
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_46	PRU_ICSSG1_PR1_SLV_INTR_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_47	PRU_ICSSG1_PR1_SLV_INTR_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_48	PRU_ICSSG1_PR1_SLV_INTR_IN_48
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_49	PRU_ICSSG1_PR1_SLV_INTR_IN_49
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_50	PRU_ICSSG1_PR1_SLV_INTR_IN_50
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_51	PRU_ICSSG1_PR1_SLV_INTR_IN_51
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_52	PRU_ICSSG1_PR1_SLV_INTR_IN_52
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_53	PRU_ICSSG1_PR1_SLV_INTR_IN_53
CBASS_INFRA1	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_133
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_133
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_133
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_133
	CBASS_INFRA1_DEFAULT_EXP_OUT_0	DMSC0_CORTEX_M3_0_SEC_IN_IN_1
MCU_CBASS0	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_133
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_133
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_133
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_133
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_31
MCU_CTRL_MMR0	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_61
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_231
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_130
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_130
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_130

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_CTRL_MMR0	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_130
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_130
MCU_MCU_GPIOMUX_INTROUTER0	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_104
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	R5FSS0_CORE0_INTR_IN_104
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	R5FSS0_CORE1_INTR_IN_104
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	R5FSS1_CORE0_INTR_IN_104
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	R5FSS1_CORE1_INTR_IN_104
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_105
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	R5FSS0_CORE0_INTR_IN_105
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	R5FSS0_CORE1_INTR_IN_105
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	R5FSS1_CORE0_INTR_IN_105
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	R5FSS1_CORE1_INTR_IN_105
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_106
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	R5FSS0_CORE0_INTR_IN_106
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	R5FSS0_CORE1_INTR_IN_106
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	R5FSS1_CORE0_INTR_IN_106
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	R5FSS1_CORE1_INTR_IN_106
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_107
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	R5FSS0_CORE0_INTR_IN_107
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	R5FSS0_CORE1_INTR_IN_107
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	R5FSS1_CORE0_INTR_IN_107
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	R5FSS1_CORE1_INTR_IN_107
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_4	MCU_M4FSS0_CORE0_NVIC_IN_0
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_5	MCU_M4FSS0_CORE0_NVIC_IN_1
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_6	MCU_M4FSS0_CORE0_NVIC_IN_2
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_7	MCU_M4FSS0_CORE0_NVIC_IN_3
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	MCU_ESM0_ESM_PLS_EVENT0_IN_88
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	MCU_ESM0_ESM_PLS_EVENT1_IN_88
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	MCU_ESM0_ESM_PLS_EVENT2_IN_88
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	MCU_ESM0_ESM_PLS_EVENT0_IN_89
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	MCU_ESM0_ESM_PLS_EVENT1_IN_89
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	MCU_ESM0_ESM_PLS_EVENT2_IN_89
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	MCU_ESM0_ESM_PLS_EVENT0_IN_90

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_MCU_GPIOMUX_INTROUTER0	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	MCU_ESM0_ESM_PLS_EVENT1_IN_90
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	MCU_ESM0_ESM_PLS_EVENT2_IN_90
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	MCU_ESM0_ESM_PLS_EVENT0_IN_91
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	MCU_ESM0_ESM_PLS_EVENT1_IN_91
	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	MCU_ESM0_ESM_PLS_EVENT2_IN_91
TIMESYNC_EVENT_INTROUTER0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_8
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_1	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_9
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_2	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_10
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_3	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_11
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_4	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_12
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_5	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_13
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_6	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_14
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_7	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_15
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_8	PRU_ICSSG0_PR1_EDC0_LATCH0_IN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_9	PRU_ICSSG0_PR1_EDC0_LATCH1_IN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_10	PRU_ICSSG0_PR1_EDC1_LATCH0_IN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_11	PRU_ICSSG0_PR1_EDC1_LATCH1_IN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_12	PRU_ICSSG1_PR1_EDC0_LATCH0_IN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_13	PRU_ICSSG1_PR1_EDC0_LATCH1_IN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_14	PRU_ICSSG1_PR1_EDC1_LATCH0_IN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_15	PRU_ICSSG1_PR1_EDC1_LATCH1_IN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_16	CPTS0_CPTS_HW1_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_17	CPTS0_CPTS_HW2_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_18	CPTS0_CPTS_HW3_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_19	CPTS0_CPTS_HW4_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_20	CPTS0_CPTS_HW5_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_21	CPTS0_CPTS_HW6_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_22	CPTS0_CPTS_HW7_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_23	CPTS0_CPTS_HW8_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_24	PINFUNCTION_SYNC0_OUTOUT_SYNC0_OUT_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_25	PINFUNCTION_SYNC1_OUTOUT_SYNC1_OUT_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_26	PINFUNCTION_SYNC2_OUTOUT_SYNC2_OUT_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_27	PINFUNCTION_SYNC3_OUTOUT_SYNC3_OUT_IN_0

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
TIMESYNC_EVENT_INTROUTER0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_29	PCIE0_PCIE_CPTS_HW2_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_30	CPSW0_CPTS_HW1_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_31	CPSW0_CPTS_HW2_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_32	CPSW0_CPTS_HW3_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_33	CPSW0_CPTS_HW4_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_34	CPSW0_CPTS_HW5_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_35	CPSW0_CPTS_HW6_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_36	CPSW0_CPTS_HW7_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_37	CPSW0_CPTS_HW8_PUSH_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_38	EPWM0_EPWM_SYNCIN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_39	EPWM3_EPWM_SYNCIN_IN_0
	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_40	EPWM6_EPWM_SYNCIN_IN_0
PADCFG_CTRL0	PADCFG_CTRL0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_59
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_232
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_131
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_131
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_131
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_131
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_131
MCU_PADCFG_CTRL0	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_60
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_233
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_132
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_132
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_132
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_132
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_132
MCU_M4FSS0_ECC_AGGR_0	MCU_M4FSS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_4
	MCU_M4FSS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_5
MCU_M4FSS0_RAT_0	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_14
	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_3
CPSW0	CPSW0_CPTS_COMP_OUT_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPOUT_CP_GEMAC_CPTS0_TS_COMP_IN_0
	CPSW0_CPTS_COMP_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_80
	CPSW0_CPTS_GENF0_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_21

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CPSW0	CPSW0_CPTS_GENF1_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_22
	CPSW0_CPTS_SYNC_OUT_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCOUT_CP_GEMAC_CPTS0_TS_SYNC_IN_0
	CPSW0_CPTS_SYNC_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_34
	CPSW0_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_67
	CPSW0_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_3
	CPSW0_EVNT_PEND_OUT_0	GICSS0_SPI_IN_134
	CPSW0_EVNT_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_134
	CPSW0_EVNT_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_134
	CPSW0_EVNT_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_134
	CPSW0_EVNT_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_134
	CPSW0_MDIO_PEND_OUT_0	GICSS0_SPI_IN_135
	CPSW0_MDIO_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_135
	CPSW0_MDIO_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_135
	CPSW0_MDIO_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_135
	CPSW0_MDIO_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_135
	CPSW0_STAT_PEND_OUT_0	GICSS0_SPI_IN_136
	CPSW0_STAT_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_136
	CPSW0_STAT_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_136
	CPSW0_STAT_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_136
	CPSW0_STAT_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_136
DCC0	DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_182
	DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_182
	DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_182
	DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_182
	DCC0_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_112
DCC1	DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_182
	DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_182
	DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_182
	DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_182
	DCC1_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_113
DCC2	DCC2_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_182
	DCC2_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_182
	DCC2_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_182

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DCC2	DCC2_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_182
	DCC2_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_114
DCC3	DCC3_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_182
	DCC3_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_182
	DCC3_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_182
	DCC3_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_182
	DCC3_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_115
DCC4	DCC4_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_182
	DCC4_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_182
	DCC4_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_182
	DCC4_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_182
	DCC4_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_116
DCC5	DCC5_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_182
	DCC5_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_182
	DCC5_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_182
	DCC5_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_182
	DCC5_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_117
MCU_DCC0	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_28
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_36
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_137
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_137
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_137
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_137
	MCU_DCC0_INTR_ERR_LEVEL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_37
DMSC0_AES_0	DMSC0_AES_0_HIB_PUBLIC_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_48
	DMSC0_AES_0_HIB_PUBLIC_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_39
	DMSC0_AES_0_HIB_PUBLIC_OUT_0	GICSS0_SPI_IN_176
	DMSC0_AES_0_HIB_PUBLIC_OUT_0	R5FSS0_CORE0_INTR_IN_1
	DMSC0_AES_0_HIB_PUBLIC_OUT_0	R5FSS0_CORE1_INTR_IN_1
	DMSC0_AES_0_HIB_PUBLIC_OUT_0	R5FSS1_CORE0_INTR_IN_1
	DMSC0_AES_0_HIB_PUBLIC_OUT_0	R5FSS1_CORE1_INTR_IN_1
	DMSC0_AES_0_HIB_SECURE_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_49
	DMSC0_AES_0_HIB_SECURE_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_38

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMSC0_AES_0	DMSC0_AES_0_HIB_SECURE_OUT_0	GICSS0_SPI_IN_198
	DMSC0_AES_0_HIB_SECURE_OUT_0	R5FSS0_CORE0_INTR_IN_2
	DMSC0_AES_0_HIB_SECURE_OUT_0	R5FSS0_CORE1_INTR_IN_2
	DMSC0_AES_0_HIB_SECURE_OUT_0	R5FSS1_CORE0_INTR_IN_2
	DMSC0_AES_0_HIB_SECURE_OUT_0	R5FSS1_CORE1_INTR_IN_2
DMSC0_CORTEX_M3_0	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_26
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0	GICSS0_SPI_IN_143
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0	R5FSS0_CORE0_INTR_IN_56
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0	R5FSS0_CORE1_INTR_IN_56
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0	R5FSS1_CORE0_INTR_IN_56
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_0	R5FSS1_CORE1_INTR_IN_56
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1	MCU_M4FSS0_CORE0_NVIC_IN_27
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1	GICSS0_SPI_IN_144
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1	R5FSS0_CORE0_INTR_IN_57
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1	R5FSS0_CORE1_INTR_IN_57
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1	R5FSS1_CORE0_INTR_IN_57
	DMSC0_CORTEX_M3_0_SEC_OUT_OUT_1	R5FSS1_CORE1_INTR_IN_57
DMSC0_DBG_AUTH_0	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_50
	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_36
	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0	GICSS0_SPI_IN_239
	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_3
	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_3
	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_3
	DMSC0_DBG_AUTH_0_DEBUG_AUTH_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_3
DMSC0_CBASS_0	DMSC0_CBASS_0_FW_COMBINED_EXP_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_47
	DMSC0_CBASS_0_FW_INT_DMSC_EXP_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_46
DMSC0_DMTIMER_0	DMSC0_DMTIMER_0_INTR_PEND_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_8
	DMSC0_DMTIMER_0_INTR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_50
DMSC0_DMTIMER_1	DMSC0_DMTIMER_1_INTR_PEND_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_10
	DMSC0_DMTIMER_1_INTR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_51
DMSC0_DMTIMER_2	DMSC0_DMTIMER_2_INTR_PEND_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_32
	DMSC0_DMTIMER_2_INTR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_52
DMSC0_DMTIMER_3	DMSC0_DMTIMER_3_INTR_PEND_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_34

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMSC0_DMTIMER_3	DMSC0_DMTIMER_3_INTR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_53
DMSC0_ECC_AGGR_0	DMSC0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_8
	DMSC0_ECC_AGGR_0_ECC_CORRECTED_ERR_PULSE_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_12
	DMSC0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_71
	DMSC0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_PULSE_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_13
DMSC0_INTAGGR_0	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_48
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1	DMSC0_CORTEX_M3_0_NVIC_IN_49
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2	DMSC0_CORTEX_M3_0_NVIC_IN_50
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3	DMSC0_CORTEX_M3_0_NVIC_IN_51
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4	DMSC0_CORTEX_M3_0_NVIC_IN_52
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5	DMSC0_CORTEX_M3_0_NVIC_IN_53
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6	DMSC0_CORTEX_M3_0_NVIC_IN_54
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7	DMSC0_CORTEX_M3_0_NVIC_IN_55
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8	DMSC0_CORTEX_M3_0_NVIC_IN_56
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9	DMSC0_CORTEX_M3_0_NVIC_IN_57
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10	DMSC0_CORTEX_M3_0_NVIC_IN_58
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11	DMSC0_CORTEX_M3_0_NVIC_IN_59
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12	DMSC0_CORTEX_M3_0_NVIC_IN_60
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13	DMSC0_CORTEX_M3_0_NVIC_IN_61
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14	DMSC0_CORTEX_M3_0_NVIC_IN_62
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15	DMSC0_CORTEX_M3_0_NVIC_IN_63
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16	DMSC0_CORTEX_M3_0_NVIC_IN_64
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17	DMSC0_CORTEX_M3_0_NVIC_IN_65
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18	DMSC0_CORTEX_M3_0_NVIC_IN_66
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19	DMSC0_CORTEX_M3_0_NVIC_IN_67
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20	DMSC0_CORTEX_M3_0_NVIC_IN_68
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21	DMSC0_CORTEX_M3_0_NVIC_IN_69
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22	DMSC0_CORTEX_M3_0_NVIC_IN_70
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23	DMSC0_CORTEX_M3_0_NVIC_IN_71
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24	DMSC0_CORTEX_M3_0_NVIC_IN_72
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25	DMSC0_CORTEX_M3_0_NVIC_IN_73
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26	DMSC0_CORTEX_M3_0_NVIC_IN_74
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27	DMSC0_CORTEX_M3_0_NVIC_IN_75

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMSC0_INTAGGR_0	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28	DMSC0_CORTEX_M3_0_NVIC_IN_76
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29	DMSC0_CORTEX_M3_0_NVIC_IN_77
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30	DMSC0_CORTEX_M3_0_NVIC_IN_78
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31	DMSC0_CORTEX_M3_0_NVIC_IN_79
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32	DMSC0_CORTEX_M3_0_NVIC_IN_80
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33	DMSC0_CORTEX_M3_0_NVIC_IN_81
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34	DMSC0_CORTEX_M3_0_NVIC_IN_82
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35	DMSC0_CORTEX_M3_0_NVIC_IN_83
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36	DMSC0_CORTEX_M3_0_NVIC_IN_84
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37	DMSC0_CORTEX_M3_0_NVIC_IN_85
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38	DMSC0_CORTEX_M3_0_NVIC_IN_86
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39	DMSC0_CORTEX_M3_0_NVIC_IN_87
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40	DMSC0_CORTEX_M3_0_NVIC_IN_88
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41	DMSC0_CORTEX_M3_0_NVIC_IN_89
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42	DMSC0_CORTEX_M3_0_NVIC_IN_90
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43	DMSC0_CORTEX_M3_0_NVIC_IN_91
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44	DMSC0_CORTEX_M3_0_NVIC_IN_92
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45	DMSC0_CORTEX_M3_0_NVIC_IN_93
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46	DMSC0_CORTEX_M3_0_NVIC_IN_94
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47	DMSC0_CORTEX_M3_0_NVIC_IN_95
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48	DMSC0_CORTEX_M3_0_NVIC_IN_96
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49	DMSC0_CORTEX_M3_0_NVIC_IN_97
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50	DMSC0_CORTEX_M3_0_NVIC_IN_98
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51	DMSC0_CORTEX_M3_0_NVIC_IN_99
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52	DMSC0_CORTEX_M3_0_NVIC_IN_100
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53	DMSC0_CORTEX_M3_0_NVIC_IN_101
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54	DMSC0_CORTEX_M3_0_NVIC_IN_102
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55	DMSC0_CORTEX_M3_0_NVIC_IN_103
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56	DMSC0_CORTEX_M3_0_NVIC_IN_104
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57	DMSC0_CORTEX_M3_0_NVIC_IN_105
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58	DMSC0_CORTEX_M3_0_NVIC_IN_106
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59	DMSC0_CORTEX_M3_0_NVIC_IN_107
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60	DMSC0_CORTEX_M3_0_NVIC_IN_108

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMSC0_INTAGGR_0	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61	DMSC0_CORTEX_M3_0_NVIC_IN_109
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62	DMSC0_CORTEX_M3_0_NVIC_IN_110
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63	DMSC0_CORTEX_M3_0_NVIC_IN_111
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64	DMSC0_CORTEX_M3_0_NVIC_IN_112
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65	DMSC0_CORTEX_M3_0_NVIC_IN_113
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66	DMSC0_CORTEX_M3_0_NVIC_IN_114
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67	DMSC0_CORTEX_M3_0_NVIC_IN_115
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68	DMSC0_CORTEX_M3_0_NVIC_IN_116
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69	DMSC0_CORTEX_M3_0_NVIC_IN_117
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70	DMSC0_CORTEX_M3_0_NVIC_IN_118
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71	DMSC0_CORTEX_M3_0_NVIC_IN_119
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72	DMSC0_CORTEX_M3_0_NVIC_IN_120
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73	DMSC0_CORTEX_M3_0_NVIC_IN_121
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74	DMSC0_CORTEX_M3_0_NVIC_IN_122
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75	DMSC0_CORTEX_M3_0_NVIC_IN_123
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76	DMSC0_CORTEX_M3_0_NVIC_IN_124
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77	DMSC0_CORTEX_M3_0_NVIC_IN_125
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78	DMSC0_CORTEX_M3_0_NVIC_IN_126
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79	DMSC0_CORTEX_M3_0_NVIC_IN_127
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_80	DMSC0_CORTEX_M3_0_NVIC_IN_128
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_81	DMSC0_CORTEX_M3_0_NVIC_IN_129
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_82	DMSC0_CORTEX_M3_0_NVIC_IN_130
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_83	DMSC0_CORTEX_M3_0_NVIC_IN_131
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_84	DMSC0_CORTEX_M3_0_NVIC_IN_132
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_85	DMSC0_CORTEX_M3_0_NVIC_IN_133
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_86	DMSC0_CORTEX_M3_0_NVIC_IN_134
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_87	DMSC0_CORTEX_M3_0_NVIC_IN_135
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88	DMSC0_CORTEX_M3_0_NVIC_IN_136
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89	DMSC0_CORTEX_M3_0_NVIC_IN_137
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90	DMSC0_CORTEX_M3_0_NVIC_IN_138
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91	DMSC0_CORTEX_M3_0_NVIC_IN_139
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92	DMSC0_CORTEX_M3_0_NVIC_IN_140
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93	DMSC0_CORTEX_M3_0_NVIC_IN_141

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMSC0_INTAGGR_0	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94	DMSC0_CORTEX_M3_0_NVIC_IN_142
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95	DMSC0_CORTEX_M3_0_NVIC_IN_143
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96	DMSC0_CORTEX_M3_0_NVIC_IN_144
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97	DMSC0_CORTEX_M3_0_NVIC_IN_145
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98	DMSC0_CORTEX_M3_0_NVIC_IN_146
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99	DMSC0_CORTEX_M3_0_NVIC_IN_147
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_100	DMSC0_CORTEX_M3_0_NVIC_IN_148
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_101	DMSC0_CORTEX_M3_0_NVIC_IN_149
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_102	DMSC0_CORTEX_M3_0_NVIC_IN_150
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_103	DMSC0_CORTEX_M3_0_NVIC_IN_151
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_104	DMSC0_CORTEX_M3_0_NVIC_IN_152
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_105	DMSC0_CORTEX_M3_0_NVIC_IN_153
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_106	DMSC0_CORTEX_M3_0_NVIC_IN_154
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_107	DMSC0_CORTEX_M3_0_NVIC_IN_155
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_108	DMSC0_CORTEX_M3_0_NVIC_IN_156
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_109	DMSC0_CORTEX_M3_0_NVIC_IN_157
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_110	DMSC0_CORTEX_M3_0_NVIC_IN_158
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_111	DMSC0_CORTEX_M3_0_NVIC_IN_159
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_112	DMSC0_CORTEX_M3_0_NVIC_IN_160
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_113	DMSC0_CORTEX_M3_0_NVIC_IN_161
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_114	DMSC0_CORTEX_M3_0_NVIC_IN_162
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_115	DMSC0_CORTEX_M3_0_NVIC_IN_163
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_116	DMSC0_CORTEX_M3_0_NVIC_IN_164
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_117	DMSC0_CORTEX_M3_0_NVIC_IN_165
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_118	DMSC0_CORTEX_M3_0_NVIC_IN_166
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_119	DMSC0_CORTEX_M3_0_NVIC_IN_167
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_120	DMSC0_CORTEX_M3_0_NVIC_IN_168
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_121	DMSC0_CORTEX_M3_0_NVIC_IN_169
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_122	DMSC0_CORTEX_M3_0_NVIC_IN_170
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_123	DMSC0_CORTEX_M3_0_NVIC_IN_171
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_124	DMSC0_CORTEX_M3_0_NVIC_IN_172
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_125	DMSC0_CORTEX_M3_0_NVIC_IN_173
	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_126	DMSC0_CORTEX_M3_0_NVIC_IN_174

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMSC0_INTAGGR_0	DMSC0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_127	DMSC0_CORTEX_M3_0_NVIC_IN_175
DMSC0_RAT_0	DMSC0_RAT_0_EXP_INTR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_11
	DMSC0_RAT_0_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_4
DMSC0_RTI_0	DMSC0_RTI_0_INTR_RTI_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_17
	DMSC0_RTI_0_INTR_RTI_OUT_1	DMSC0_CORTEX_M3_0_NVIC_IN_18
	DMSC0_RTI_0_INTR_RTI_OUT_2	DMSC0_CORTEX_M3_0_NVIC_IN_19
	DMSC0_RTI_0_INTR_RTI_OUT_3	DMSC0_CORTEX_M3_0_NVIC_IN_20
	DMSC0_RTI_0_INTR_WWD_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_16
	DMSC0_RTI_0_INTR_WWD_OUT_0	ESM0_ESM_LVL_EVENT_IN_5
DMASS0_ECC_AGGR_0	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_9
	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_72
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0	GICSS0_SPI_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1	GICSS0_SPI_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2	GICSS0_SPI_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3	GICSS0_SPI_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4	GICSS0_SPI_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5	GICSS0_SPI_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6	GICSS0_SPI_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7	GICSS0_SPI_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8	GICSS0_SPI_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9	GICSS0_SPI_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10	GICSS0_SPI_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11	GICSS0_SPI_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12	GICSS0_SPI_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13	GICSS0_SPI_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14	GICSS0_SPI_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15	GICSS0_SPI_IN_79
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16	GICSS0_SPI_IN_80
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17	GICSS0_SPI_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18	GICSS0_SPI_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19	GICSS0_SPI_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20	GICSS0_SPI_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21	GICSS0_SPI_IN_85

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22	GICSS0_SPI_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23	GICSS0_SPI_IN_87
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24	GICSS0_SPI_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25	GICSS0_SPI_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26	GICSS0_SPI_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27	GICSS0_SPI_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28	GICSS0_SPI_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29	GICSS0_SPI_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30	GICSS0_SPI_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31	GICSS0_SPI_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32	GICSS0_SPI_IN_96
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33	GICSS0_SPI_IN_97
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34	GICSS0_SPI_IN_98
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35	GICSS0_SPI_IN_99
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36	GICSS0_SPI_IN_100
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37	GICSS0_SPI_IN_101
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38	GICSS0_SPI_IN_102
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39	GICSS0_SPI_IN_103
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40	R5FSS0_CORE0_INTR_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40	R5FSS0_CORE1_INTR_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41	R5FSS0_CORE0_INTR_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41	R5FSS0_CORE1_INTR_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42	R5FSS0_CORE0_INTR_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42	R5FSS0_CORE1_INTR_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43	R5FSS0_CORE0_INTR_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43	R5FSS0_CORE1_INTR_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44	R5FSS0_CORE0_INTR_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44	R5FSS0_CORE1_INTR_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45	R5FSS0_CORE0_INTR_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45	R5FSS0_CORE1_INTR_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46	R5FSS0_CORE0_INTR_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46	R5FSS0_CORE1_INTR_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47	R5FSS0_CORE0_INTR_IN_71

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47	R5FSS0_CORE1_INTR_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48	R5FSS0_CORE0_INTR_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48	R5FSS0_CORE1_INTR_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49	R5FSS0_CORE0_INTR_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49	R5FSS0_CORE1_INTR_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50	R5FSS0_CORE0_INTR_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50	R5FSS0_CORE1_INTR_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51	R5FSS0_CORE0_INTR_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51	R5FSS0_CORE1_INTR_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52	R5FSS0_CORE0_INTR_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52	R5FSS0_CORE1_INTR_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53	R5FSS0_CORE0_INTR_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53	R5FSS0_CORE1_INTR_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54	R5FSS0_CORE0_INTR_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54	R5FSS0_CORE1_INTR_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55	R5FSS0_CORE0_INTR_IN_79
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55	R5FSS0_CORE1_INTR_IN_79
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56	R5FSS0_CORE0_INTR_IN_80
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56	R5FSS0_CORE1_INTR_IN_80
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57	R5FSS0_CORE0_INTR_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57	R5FSS0_CORE1_INTR_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58	R5FSS0_CORE0_INTR_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58	R5FSS0_CORE1_INTR_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59	R5FSS0_CORE0_INTR_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59	R5FSS0_CORE1_INTR_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60	R5FSS0_CORE0_INTR_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60	R5FSS0_CORE1_INTR_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61	R5FSS0_CORE0_INTR_IN_85
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61	R5FSS0_CORE1_INTR_IN_85
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62	R5FSS0_CORE0_INTR_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62	R5FSS0_CORE1_INTR_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63	R5FSS0_CORE0_INTR_IN_87
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63	R5FSS0_CORE1_INTR_IN_87

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64	R5FSS0_CORE0_INTR_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64	R5FSS0_CORE1_INTR_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65	R5FSS0_CORE0_INTR_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65	R5FSS0_CORE1_INTR_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66	R5FSS0_CORE0_INTR_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66	R5FSS0_CORE1_INTR_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67	R5FSS0_CORE0_INTR_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67	R5FSS0_CORE1_INTR_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68	R5FSS0_CORE0_INTR_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68	R5FSS0_CORE1_INTR_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69	R5FSS0_CORE0_INTR_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69	R5FSS0_CORE1_INTR_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70	R5FSS0_CORE0_INTR_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70	R5FSS0_CORE1_INTR_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71	R5FSS0_CORE0_INTR_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71	R5FSS0_CORE1_INTR_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72	R5FSS0_CORE0_INTR_IN_8
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73	R5FSS0_CORE0_INTR_IN_9
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74	R5FSS0_CORE0_INTR_IN_10
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75	R5FSS0_CORE0_INTR_IN_11
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76	R5FSS0_CORE0_INTR_IN_12
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77	R5FSS0_CORE0_INTR_IN_13
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78	R5FSS0_CORE0_INTR_IN_14
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79	R5FSS0_CORE0_INTR_IN_15
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_80	R5FSS0_CORE1_INTR_IN_8
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_81	R5FSS0_CORE1_INTR_IN_9
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_82	R5FSS0_CORE1_INTR_IN_10
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_83	R5FSS0_CORE1_INTR_IN_11
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_84	R5FSS0_CORE1_INTR_IN_12
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_85	R5FSS0_CORE1_INTR_IN_13
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_86	R5FSS0_CORE1_INTR_IN_14
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_87	R5FSS0_CORE1_INTR_IN_15
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88	R5FSS1_CORE0_INTR_IN_64

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88	R5FSS1_CORE1_INTR_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89	R5FSS1_CORE0_INTR_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89	R5FSS1_CORE1_INTR_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90	R5FSS1_CORE0_INTR_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90	R5FSS1_CORE1_INTR_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91	R5FSS1_CORE0_INTR_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91	R5FSS1_CORE1_INTR_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92	R5FSS1_CORE0_INTR_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92	R5FSS1_CORE1_INTR_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93	R5FSS1_CORE0_INTR_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93	R5FSS1_CORE1_INTR_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94	R5FSS1_CORE0_INTR_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94	R5FSS1_CORE1_INTR_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95	R5FSS1_CORE0_INTR_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95	R5FSS1_CORE1_INTR_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96	R5FSS1_CORE0_INTR_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96	R5FSS1_CORE1_INTR_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97	R5FSS1_CORE0_INTR_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97	R5FSS1_CORE1_INTR_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98	R5FSS1_CORE0_INTR_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98	R5FSS1_CORE1_INTR_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99	R5FSS1_CORE0_INTR_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99	R5FSS1_CORE1_INTR_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_100	R5FSS1_CORE0_INTR_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_100	R5FSS1_CORE1_INTR_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_101	R5FSS1_CORE0_INTR_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_101	R5FSS1_CORE1_INTR_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_102	R5FSS1_CORE0_INTR_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_102	R5FSS1_CORE1_INTR_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_103	R5FSS1_CORE0_INTR_IN_79
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_103	R5FSS1_CORE1_INTR_IN_79
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_104	R5FSS1_CORE0_INTR_IN_80
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_104	R5FSS1_CORE1_INTR_IN_80

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_105	R5FSS1_CORE0_INTR_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_105	R5FSS1_CORE1_INTR_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_106	R5FSS1_CORE0_INTR_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_106	R5FSS1_CORE1_INTR_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_107	R5FSS1_CORE0_INTR_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_107	R5FSS1_CORE1_INTR_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_108	R5FSS1_CORE0_INTR_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_108	R5FSS1_CORE1_INTR_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_109	R5FSS1_CORE0_INTR_IN_85
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_109	R5FSS1_CORE1_INTR_IN_85
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_110	R5FSS1_CORE0_INTR_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_110	R5FSS1_CORE1_INTR_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_111	R5FSS1_CORE0_INTR_IN_87
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_111	R5FSS1_CORE1_INTR_IN_87
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_112	R5FSS1_CORE0_INTR_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_112	R5FSS1_CORE1_INTR_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_113	R5FSS1_CORE0_INTR_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_113	R5FSS1_CORE1_INTR_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_114	R5FSS1_CORE0_INTR_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_114	R5FSS1_CORE1_INTR_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_115	R5FSS1_CORE0_INTR_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_115	R5FSS1_CORE1_INTR_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_116	R5FSS1_CORE0_INTR_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_116	R5FSS1_CORE1_INTR_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_117	R5FSS1_CORE0_INTR_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_117	R5FSS1_CORE1_INTR_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_118	R5FSS1_CORE0_INTR_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_118	R5FSS1_CORE1_INTR_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_119	R5FSS1_CORE0_INTR_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_119	R5FSS1_CORE1_INTR_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_120	R5FSS1_CORE0_INTR_IN_8
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_121	R5FSS1_CORE0_INTR_IN_9
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_122	R5FSS1_CORE0_INTR_IN_10

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_123	R5FSS1_CORE0_INTR_IN_11
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_124	R5FSS1_CORE0_INTR_IN_12
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_125	R5FSS1_CORE0_INTR_IN_13
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_126	R5FSS1_CORE0_INTR_IN_14
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_127	R5FSS1_CORE0_INTR_IN_15
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_128	R5FSS1_CORE1_INTR_IN_8
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_129	R5FSS1_CORE1_INTR_IN_9
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_130	R5FSS1_CORE1_INTR_IN_10
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_131	R5FSS1_CORE1_INTR_IN_11
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_132	R5FSS1_CORE1_INTR_IN_12
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_133	R5FSS1_CORE1_INTR_IN_13
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_134	R5FSS1_CORE1_INTR_IN_14
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_135	R5FSS1_CORE1_INTR_IN_15
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_136	DMSC0_CORTEX_M3_0_NVIC_IN_176
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_137	DMSC0_CORTEX_M3_0_NVIC_IN_177
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_138	DMSC0_CORTEX_M3_0_NVIC_IN_178
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_139	DMSC0_CORTEX_M3_0_NVIC_IN_179
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_140	DMSC0_CORTEX_M3_0_NVIC_IN_180
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_141	DMSC0_CORTEX_M3_0_NVIC_IN_181
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_142	DMSC0_CORTEX_M3_0_NVIC_IN_182
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_143	DMSC0_CORTEX_M3_0_NVIC_IN_183
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_144	DMSC0_CORTEX_M3_0_NVIC_IN_184
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_145	DMSC0_CORTEX_M3_0_NVIC_IN_185
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_146	DMSC0_CORTEX_M3_0_NVIC_IN_186
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_147	DMSC0_CORTEX_M3_0_NVIC_IN_187
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_148	DMSC0_CORTEX_M3_0_NVIC_IN_188
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_149	DMSC0_CORTEX_M3_0_NVIC_IN_189
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_150	DMSC0_CORTEX_M3_0_NVIC_IN_190
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_151	DMSC0_CORTEX_M3_0_NVIC_IN_191
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_152	PRU_ICSSG0_PR1_SLV_INTR_IN_0
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_153	PRU_ICSSG0_PR1_SLV_INTR_IN_1
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_154	PRU_ICSSG0_PR1_SLV_INTR_IN_2
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_155	PRU_ICSSG0_PR1_SLV_INTR_IN_3

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_156	PRU_ICSSG0_PR1_SLV_INTR_IN_4
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_157	PRU_ICSSG0_PR1_SLV_INTR_IN_5
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_158	PRU_ICSSG0_PR1_SLV_INTR_IN_6
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_159	PRU_ICSSG0_PR1_SLV_INTR_IN_7
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_160	PRU_ICSSG1_PR1_SLV_INTR_IN_0
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_161	PRU_ICSSG1_PR1_SLV_INTR_IN_1
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_162	PRU_ICSSG1_PR1_SLV_INTR_IN_2
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_163	PRU_ICSSG1_PR1_SLV_INTR_IN_3
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_164	PRU_ICSSG1_PR1_SLV_INTR_IN_4
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_165	PRU_ICSSG1_PR1_SLV_INTR_IN_5
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_166	PRU_ICSSG1_PR1_SLV_INTR_IN_6
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_167	PRU_ICSSG1_PR1_SLV_INTR_IN_7
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168	MCU_M4FSS0_CORE0_NVIC_IN_32
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169	MCU_M4FSS0_CORE0_NVIC_IN_33
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170	MCU_M4FSS0_CORE0_NVIC_IN_34
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171	MCU_M4FSS0_CORE0_NVIC_IN_35
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172	MCU_M4FSS0_CORE0_NVIC_IN_36
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173	MCU_M4FSS0_CORE0_NVIC_IN_37
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174	MCU_M4FSS0_CORE0_NVIC_IN_38
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175	MCU_M4FSS0_CORE0_NVIC_IN_39
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_176	MCU_M4FSS0_CORE0_NVIC_IN_40
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_177	MCU_M4FSS0_CORE0_NVIC_IN_41
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_178	MCU_M4FSS0_CORE0_NVIC_IN_42
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_179	MCU_M4FSS0_CORE0_NVIC_IN_43
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_180	MCU_M4FSS0_CORE0_NVIC_IN_44
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_181	MCU_M4FSS0_CORE0_NVIC_IN_45
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_182	MCU_M4FSS0_CORE0_NVIC_IN_46
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_183	MCU_M4FSS0_CORE0_NVIC_IN_47
TIMER0	TIMER0_INTR_PEND_OUT_0	GICSS0_SPI_IN_152
	TIMER0_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_152
	TIMER0_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_152
	TIMER0_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_152
	TIMER0_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_152

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
TIMER0	TIMER0_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_0
TIMER1	TIMER1_INTR_PEND_OUT_0	GICSS0_SPI_IN_153
	TIMER1_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_153
	TIMER1_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_153
	TIMER1_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_153
	TIMER1_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_153
	TIMER1_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_1
TIMER10	TIMER10_INTR_PEND_OUT_0	GICSS0_SPI_IN_162
	TIMER10_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_162
	TIMER10_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_162
	TIMER10_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_162
	TIMER10_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_162
TIMER11	TIMER11_INTR_PEND_OUT_0	GICSS0_SPI_IN_163
	TIMER11_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_163
	TIMER11_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_163
	TIMER11_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_163
	TIMER11_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_163
TIMER2	TIMER2_INTR_PEND_OUT_0	GICSS0_SPI_IN_154
	TIMER2_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_154
	TIMER2_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_154
	TIMER2_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_154
	TIMER2_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_154
	TIMER2_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_2
TIMER3	TIMER3_INTR_PEND_OUT_0	GICSS0_SPI_IN_155
	TIMER3_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_155
	TIMER3_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_155
	TIMER3_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_155
	TIMER3_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_155
	TIMER3_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_3
TIMER4	TIMER4_INTR_PEND_OUT_0	GICSS0_SPI_IN_156
	TIMER4_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_156
	TIMER4_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_156
	TIMER4_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_156

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
TIMER4	TIMER4_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_156
TIMER5	TIMER5_INTR_PEND_OUT_0	GICSS0_SPI_IN_157
	TIMER5_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_157
	TIMER5_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_157
	TIMER5_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_157
	TIMER5_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_157
TIMER6	TIMER6_INTR_PEND_OUT_0	GICSS0_SPI_IN_158
	TIMER6_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_158
	TIMER6_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_158
	TIMER6_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_158
	TIMER6_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_158
TIMER7	TIMER7_INTR_PEND_OUT_0	GICSS0_SPI_IN_159
	TIMER7_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_159
	TIMER7_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_159
	TIMER7_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_159
	TIMER7_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_159
TIMER8	TIMER8_INTR_PEND_OUT_0	GICSS0_SPI_IN_160
	TIMER8_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_160
	TIMER8_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_160
	TIMER8_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_160
	TIMER8_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_160
TIMER9	TIMER9_INTR_PEND_OUT_0	GICSS0_SPI_IN_161
	TIMER9_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_161
	TIMER9_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_161
	TIMER9_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_161
	TIMER9_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_161
MCU_TIMER0	MCU_TIMER0_INTR_PEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_4
MCU_TIMER1	MCU_TIMER1_INTR_PEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_5
MCU_TIMER2	MCU_TIMER2_INTR_PEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_6
MCU_TIMER3	MCU_TIMER3_INTR_PEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_7
MCU_MASTER_SAFETY_GASKET0	MCU_MASTER_SAFETY_GASKET0_TIMED_OUT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_8
	MCU_MASTER_SAFETY_GASKET0_TIMED_OUT_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_26
ECAP0	ECAP0_ECAP_INT_OUT_0	GICSS0_SPI_IN_145

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
ECAP0	ECAP0_ECAP_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_8
	ECAP0_ECAP_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_8
	ECAP0_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_140
	ECAP0_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_140
	ECAP0_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_140
	ECAP0_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_140
ECAP1	ECAP1_ECAP_INT_OUT_0	GICSS0_SPI_IN_146
	ECAP1_ECAP_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_9
	ECAP1_ECAP_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_9
	ECAP1_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_141
	ECAP1_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_141
	ECAP1_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_141
	ECAP1_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_141
ECAP2	ECAP2_ECAP_INT_OUT_0	GICSS0_SPI_IN_147
	ECAP2_ECAP_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_10
	ECAP2_ECAP_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_10
	ECAP2_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_142
	ECAP2_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_142
	ECAP2_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_142
	ECAP2_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_142
ELM0	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	GICSS0_SPI_IN_164
	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_164
	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_164
	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_164
	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_164
MMCSD0	MMCSD0_EMMCSS_INTR_OUT_0	GICSS0_SPI_IN_165
	MMCSD0_EMMCSS_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_165
	MMCSD0_EMMCSS_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_165
	MMCSD0_EMMCSS_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_165
	MMCSD0_EMMCSS_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_165
	MMCSD0_EMMCSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_54
	MMCSD0_EMMCSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_55
	MMCSD0_EMMCSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_56

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MMCSD0	MMCSD0_EMMCSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_57
MMCSD1	MMCSD1_EMMCSDSS_INTR_OUT_0	GICSS0_SPI_IN_166
	MMCSD1_EMMCSDSS_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_166
	MMCSD1_EMMCSDSS_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_166
	MMCSD1_EMMCSDSS_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_166
	MMCSD1_EMMCSDSS_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_166
	MMCSD1_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_58
	MMCSD1_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_59
	MMCSD1_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_60
	MMCSD1_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_61
EQEP0	EQEP0_EQEP_INT_OUT_0	GICSS0_SPI_IN_148
	EQEP0_EQEP_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_30
	EQEP0_EQEP_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_30
	EQEP0_EQEP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_143
	EQEP0_EQEP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_143
	EQEP0_EQEP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_143
	EQEP0_EQEP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_143
EQEP1	EQEP1_EQEP_INT_OUT_0	GICSS0_SPI_IN_149
	EQEP1_EQEP_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_31
	EQEP1_EQEP_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_31
	EQEP1_EQEP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_144
	EQEP1_EQEP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_144
	EQEP1_EQEP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_144
	EQEP1_EQEP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_144
EQEP2	EQEP2_EQEP_INT_OUT_0	GICSS0_SPI_IN_150
	EQEP2_EQEP_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_32
	EQEP2_EQEP_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_32
	EQEP2_EQEP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_145
	EQEP2_EQEP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_145
	EQEP2_EQEP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_145
	EQEP2_EQEP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_145
ESM0	ESM0_ESM_INT_CFG_LVL_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_199
	ESM0_ESM_INT_CFG_LVL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_0

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
ESM0	ESM0_ESM_INT_CFG_LVL_OUT_0	GICSS0_SPI_IN_180
	ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_167
	ESM0_ESM_INT_HI_LVL_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_200
	ESM0_ESM_INT_HI_LVL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_1
	ESM0_ESM_INT_HI_LVL_OUT_0	GICSS0_SPI_IN_181
	ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_168
	ESM0_ESM_INT_LOW_LVL_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_201
	ESM0_ESM_INT_LOW_LVL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_2
	ESM0_ESM_INT_LOW_LVL_OUT_0	GICSS0_SPI_IN_182
	ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_169
MCU_ESM0	MCU_ESM0_ESM_INT_CFG_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_11
	MCU_ESM0_ESM_INT_CFG_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_37
	MCU_ESM0_ESM_INT_HI_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_12
	MCU_ESM0_ESM_INT_HI_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_38
	MCU_ESM0_ESM_INT_LOW_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_13
	MCU_ESM0_ESM_INT_LOW_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_39
FSIRX0	FSIRX0_FSI_RX_OINT1_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_33
	FSIRX0_FSI_RX_OINT1_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_33
	FSIRX0_FSI_RX_OINT1_OUT_0	R5FSS0_CORE0_INTR_IN_16
	FSIRX0_FSI_RX_OINT1_OUT_0	R5FSS0_CORE1_INTR_IN_16
	FSIRX0_FSI_RX_OINT1_OUT_0	R5FSS1_CORE0_INTR_IN_16
	FSIRX0_FSI_RX_OINT1_OUT_0	R5FSS1_CORE1_INTR_IN_16
	FSIRX0_FSI_RX_OINT2_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_34
	FSIRX0_FSI_RX_OINT2_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_34

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
FSIRX0	FSIRX0_FSI_RX_OINT2_OUT_0	R5FSS0_CORE0_INTR_IN_17
	FSIRX0_FSI_RX_OINT2_OUT_0	R5FSS0_CORE1_INTR_IN_17
	FSIRX0_FSI_RX_OINT2_OUT_0	R5FSS1_CORE0_INTR_IN_17
	FSIRX0_FSI_RX_OINT2_OUT_0	R5FSS1_CORE1_INTR_IN_17
FSIRX1	FSIRX1_FSI_RX_OINT1_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_35
	FSIRX1_FSI_RX_OINT1_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_35
	FSIRX1_FSI_RX_OINT1_OUT_0	R5FSS0_CORE0_INTR_IN_18
	FSIRX1_FSI_RX_OINT1_OUT_0	R5FSS0_CORE1_INTR_IN_18
	FSIRX1_FSI_RX_OINT1_OUT_0	R5FSS1_CORE0_INTR_IN_18
	FSIRX1_FSI_RX_OINT1_OUT_0	R5FSS1_CORE1_INTR_IN_18
	FSIRX1_FSI_RX_OINT2_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_36
	FSIRX1_FSI_RX_OINT2_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_36
	FSIRX1_FSI_RX_OINT2_OUT_0	R5FSS0_CORE0_INTR_IN_19
	FSIRX1_FSI_RX_OINT2_OUT_0	R5FSS0_CORE1_INTR_IN_19
	FSIRX1_FSI_RX_OINT2_OUT_0	R5FSS1_CORE0_INTR_IN_19
	FSIRX1_FSI_RX_OINT2_OUT_0	R5FSS1_CORE1_INTR_IN_19
FSIRX2	FSIRX2_FSI_RX_OINT1_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_37
	FSIRX2_FSI_RX_OINT1_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_37
	FSIRX2_FSI_RX_OINT1_OUT_0	R5FSS0_CORE0_INTR_IN_20
	FSIRX2_FSI_RX_OINT1_OUT_0	R5FSS0_CORE1_INTR_IN_20
	FSIRX2_FSI_RX_OINT1_OUT_0	R5FSS1_CORE0_INTR_IN_20
	FSIRX2_FSI_RX_OINT1_OUT_0	R5FSS1_CORE1_INTR_IN_20
	FSIRX2_FSI_RX_OINT2_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_38
	FSIRX2_FSI_RX_OINT2_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_38
	FSIRX2_FSI_RX_OINT2_OUT_0	R5FSS0_CORE0_INTR_IN_21
	FSIRX2_FSI_RX_OINT2_OUT_0	R5FSS0_CORE1_INTR_IN_21
	FSIRX2_FSI_RX_OINT2_OUT_0	R5FSS1_CORE0_INTR_IN_21
	FSIRX2_FSI_RX_OINT2_OUT_0	R5FSS1_CORE1_INTR_IN_21
FSIRX3	FSIRX3_FSI_RX_OINT1_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_39
	FSIRX3_FSI_RX_OINT1_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_39
	FSIRX3_FSI_RX_OINT1_OUT_0	R5FSS0_CORE0_INTR_IN_22
	FSIRX3_FSI_RX_OINT1_OUT_0	R5FSS0_CORE1_INTR_IN_22
	FSIRX3_FSI_RX_OINT1_OUT_0	R5FSS1_CORE0_INTR_IN_22

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
FSIRX3	FSIRX3_FSI_RX_OINT1_OUT_0	R5FSS1_CORE1_INTR_IN_22
	FSIRX3_FSI_RX_OINT2_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_40
	FSIRX3_FSI_RX_OINT2_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_40
	FSIRX3_FSI_RX_OINT2_OUT_0	R5FSS0_CORE0_INTR_IN_23
	FSIRX3_FSI_RX_OINT2_OUT_0	R5FSS0_CORE1_INTR_IN_23
	FSIRX3_FSI_RX_OINT2_OUT_0	R5FSS1_CORE0_INTR_IN_23
	FSIRX3_FSI_RX_OINT2_OUT_0	R5FSS1_CORE1_INTR_IN_23
FSIRX4	FSIRX4_FSI_RX_OINT1_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_41
	FSIRX4_FSI_RX_OINT1_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_41
	FSIRX4_FSI_RX_OINT1_OUT_0	R5FSS0_CORE0_INTR_IN_24
	FSIRX4_FSI_RX_OINT1_OUT_0	R5FSS0_CORE1_INTR_IN_24
	FSIRX4_FSI_RX_OINT1_OUT_0	R5FSS1_CORE0_INTR_IN_24
	FSIRX4_FSI_RX_OINT1_OUT_0	R5FSS1_CORE1_INTR_IN_24
	FSIRX4_FSI_RX_OINT2_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_42
	FSIRX4_FSI_RX_OINT2_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_42
	FSIRX4_FSI_RX_OINT2_OUT_0	R5FSS0_CORE0_INTR_IN_25
	FSIRX4_FSI_RX_OINT2_OUT_0	R5FSS0_CORE1_INTR_IN_25
	FSIRX4_FSI_RX_OINT2_OUT_0	R5FSS1_CORE0_INTR_IN_25
	FSIRX4_FSI_RX_OINT2_OUT_0	R5FSS1_CORE1_INTR_IN_25
FSIRX5	FSIRX5_FSI_RX_OINT1_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_43
	FSIRX5_FSI_RX_OINT1_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_43
	FSIRX5_FSI_RX_OINT1_OUT_0	R5FSS0_CORE0_INTR_IN_26
	FSIRX5_FSI_RX_OINT1_OUT_0	R5FSS0_CORE1_INTR_IN_26
	FSIRX5_FSI_RX_OINT1_OUT_0	R5FSS1_CORE0_INTR_IN_26
	FSIRX5_FSI_RX_OINT1_OUT_0	R5FSS1_CORE1_INTR_IN_26
	FSIRX5_FSI_RX_OINT2_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_44
	FSIRX5_FSI_RX_OINT2_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_44
	FSIRX5_FSI_RX_OINT2_OUT_0	R5FSS0_CORE0_INTR_IN_27
	FSIRX5_FSI_RX_OINT2_OUT_0	R5FSS0_CORE1_INTR_IN_27
	FSIRX5_FSI_RX_OINT2_OUT_0	R5FSS1_CORE0_INTR_IN_27
	FSIRX5_FSI_RX_OINT2_OUT_0	R5FSS1_CORE1_INTR_IN_27
FSITX0	FSITX0_FSI_TX_OINT1_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_45
	FSITX0_FSI_TX_OINT1_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_45

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
FSITX0	FSITX0_FSI_TX_OINT1_OUT_0	R5FSS0_CORE0_INTR_IN_28
	FSITX0_FSI_TX_OINT1_OUT_0	R5FSS0_CORE1_INTR_IN_28
	FSITX0_FSI_TX_OINT1_OUT_0	R5FSS1_CORE0_INTR_IN_28
	FSITX0_FSI_TX_OINT1_OUT_0	R5FSS1_CORE1_INTR_IN_28
	FSITX0_FSI_TX_OINT2_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_54
	FSITX0_FSI_TX_OINT2_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_54
	FSITX0_FSI_TX_OINT2_OUT_0	R5FSS0_CORE0_INTR_IN_29
	FSITX0_FSI_TX_OINT2_OUT_0	R5FSS0_CORE1_INTR_IN_29
	FSITX0_FSI_TX_OINT2_OUT_0	R5FSS1_CORE0_INTR_IN_29
	FSITX0_FSI_TX_OINT2_OUT_0	R5FSS1_CORE1_INTR_IN_29
FSITX1	FSITX1_FSI_TX_OINT1_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_55
	FSITX1_FSI_TX_OINT1_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_55
	FSITX1_FSI_TX_OINT1_OUT_0	R5FSS0_CORE0_INTR_IN_30
	FSITX1_FSI_TX_OINT1_OUT_0	R5FSS0_CORE1_INTR_IN_30
	FSITX1_FSI_TX_OINT1_OUT_0	R5FSS1_CORE0_INTR_IN_30
	FSITX1_FSI_TX_OINT1_OUT_0	R5FSS1_CORE1_INTR_IN_30
	FSITX1_FSI_TX_OINT2_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_56
	FSITX1_FSI_TX_OINT2_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_56
	FSITX1_FSI_TX_OINT2_OUT_0	R5FSS0_CORE0_INTR_IN_31
	FSITX1_FSI_TX_OINT2_OUT_0	R5FSS0_CORE1_INTR_IN_31
	FSITX1_FSI_TX_OINT2_OUT_0	R5FSS1_CORE0_INTR_IN_31
	FSITX1_FSI_TX_OINT2_OUT_0	R5FSS1_CORE1_INTR_IN_31
FSS0_FSAS_0	FSS0_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_228
	FSS0_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_141
	FSS0_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_227
FSS0_OSPI_0	FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_11
	FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_74
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_224
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	GICSS0_SPI_IN_171
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_171
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_171
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_171
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_171

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GICSS0	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT0_IN_166
	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT1_IN_166
	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT2_IN_166
	GICSS0_ECC_AGGR_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_12
	GICSS0_ECC_AGGR_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_75
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT0_IN_167
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT1_IN_167
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT2_IN_167
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_203
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0	R5FSS0_CORE0_INTR_IN_173
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0	R5FSS0_CORE1_INTR_IN_173
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0	R5FSS1_CORE0_INTR_IN_173
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0	R5FSS1_CORE1_INTR_IN_173
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1	DMSC0_CORTEX_M3_0_NVIC_IN_204
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1	R5FSS0_CORE0_INTR_IN_174
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1	R5FSS0_CORE1_INTR_IN_174
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1	R5FSS1_CORE0_INTR_IN_174
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1	R5FSS1_CORE1_INTR_IN_174
GPIO0	GPIO0_GPIO_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_0
	GPIO0_GPIO_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_1
	GPIO0_GPIO_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_2
	GPIO0_GPIO_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_3
	GPIO0_GPIO_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_4
	GPIO0_GPIO_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_5
	GPIO0_GPIO_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_6
	GPIO0_GPIO_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_7
	GPIO0_GPIO_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_8
	GPIO0_GPIO_OUT_9	MAIN_GPIOMUX_INTROUTER0_IN_IN_9
	GPIO0_GPIO_OUT_10	MAIN_GPIOMUX_INTROUTER0_IN_IN_10
	GPIO0_GPIO_OUT_11	MAIN_GPIOMUX_INTROUTER0_IN_IN_11
	GPIO0_GPIO_OUT_12	MAIN_GPIOMUX_INTROUTER0_IN_IN_12
	GPIO0_GPIO_OUT_13	MAIN_GPIOMUX_INTROUTER0_IN_IN_13
	GPIO0_GPIO_OUT_14	MAIN_GPIOMUX_INTROUTER0_IN_IN_14

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_15	MAIN_GPIOMUX_INTROUTER0_IN_IN_15
	GPIO0_GPIO_OUT_16	MAIN_GPIOMUX_INTROUTER0_IN_IN_16
	GPIO0_GPIO_OUT_17	MAIN_GPIOMUX_INTROUTER0_IN_IN_17
	GPIO0_GPIO_OUT_18	MAIN_GPIOMUX_INTROUTER0_IN_IN_18
	GPIO0_GPIO_OUT_19	MAIN_GPIOMUX_INTROUTER0_IN_IN_19
	GPIO0_GPIO_OUT_20	MAIN_GPIOMUX_INTROUTER0_IN_IN_20
	GPIO0_GPIO_OUT_21	MAIN_GPIOMUX_INTROUTER0_IN_IN_21
	GPIO0_GPIO_OUT_22	MAIN_GPIOMUX_INTROUTER0_IN_IN_22
	GPIO0_GPIO_OUT_23	MAIN_GPIOMUX_INTROUTER0_IN_IN_23
	GPIO0_GPIO_OUT_24	MAIN_GPIOMUX_INTROUTER0_IN_IN_24
	GPIO0_GPIO_OUT_25	MAIN_GPIOMUX_INTROUTER0_IN_IN_25
	GPIO0_GPIO_OUT_26	MAIN_GPIOMUX_INTROUTER0_IN_IN_26
	GPIO0_GPIO_OUT_27	MAIN_GPIOMUX_INTROUTER0_IN_IN_27
	GPIO0_GPIO_OUT_28	MAIN_GPIOMUX_INTROUTER0_IN_IN_28
	GPIO0_GPIO_OUT_29	MAIN_GPIOMUX_INTROUTER0_IN_IN_29
	GPIO0_GPIO_OUT_30	MAIN_GPIOMUX_INTROUTER0_IN_IN_30
	GPIO0_GPIO_OUT_31	MAIN_GPIOMUX_INTROUTER0_IN_IN_31
	GPIO0_GPIO_OUT_32	MAIN_GPIOMUX_INTROUTER0_IN_IN_32
	GPIO0_GPIO_OUT_33	MAIN_GPIOMUX_INTROUTER0_IN_IN_33
	GPIO0_GPIO_OUT_34	MAIN_GPIOMUX_INTROUTER0_IN_IN_34
	GPIO0_GPIO_OUT_35	MAIN_GPIOMUX_INTROUTER0_IN_IN_35
	GPIO0_GPIO_OUT_36	MAIN_GPIOMUX_INTROUTER0_IN_IN_36
	GPIO0_GPIO_OUT_37	MAIN_GPIOMUX_INTROUTER0_IN_IN_37
	GPIO0_GPIO_OUT_38	MAIN_GPIOMUX_INTROUTER0_IN_IN_38
	GPIO0_GPIO_OUT_39	MAIN_GPIOMUX_INTROUTER0_IN_IN_39
	GPIO0_GPIO_OUT_40	MAIN_GPIOMUX_INTROUTER0_IN_IN_40
	GPIO0_GPIO_OUT_41	MAIN_GPIOMUX_INTROUTER0_IN_IN_41
	GPIO0_GPIO_OUT_42	MAIN_GPIOMUX_INTROUTER0_IN_IN_42
	GPIO0_GPIO_OUT_43	MAIN_GPIOMUX_INTROUTER0_IN_IN_43
	GPIO0_GPIO_OUT_44	MAIN_GPIOMUX_INTROUTER0_IN_IN_44
	GPIO0_GPIO_OUT_45	MAIN_GPIOMUX_INTROUTER0_IN_IN_45
	GPIO0_GPIO_OUT_46	MAIN_GPIOMUX_INTROUTER0_IN_IN_46
	GPIO0_GPIO_OUT_47	MAIN_GPIOMUX_INTROUTER0_IN_IN_47

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_48	MAIN_GPIOMUX_INTROUTER0_IN_IN_48
	GPIO0_GPIO_OUT_49	MAIN_GPIOMUX_INTROUTER0_IN_IN_49
	GPIO0_GPIO_OUT_50	MAIN_GPIOMUX_INTROUTER0_IN_IN_50
	GPIO0_GPIO_OUT_51	MAIN_GPIOMUX_INTROUTER0_IN_IN_51
	GPIO0_GPIO_OUT_52	MAIN_GPIOMUX_INTROUTER0_IN_IN_52
	GPIO0_GPIO_OUT_53	MAIN_GPIOMUX_INTROUTER0_IN_IN_53
	GPIO0_GPIO_OUT_54	MAIN_GPIOMUX_INTROUTER0_IN_IN_54
	GPIO0_GPIO_OUT_55	MAIN_GPIOMUX_INTROUTER0_IN_IN_55
	GPIO0_GPIO_OUT_56	MAIN_GPIOMUX_INTROUTER0_IN_IN_56
	GPIO0_GPIO_OUT_57	MAIN_GPIOMUX_INTROUTER0_IN_IN_57
	GPIO0_GPIO_OUT_58	MAIN_GPIOMUX_INTROUTER0_IN_IN_58
	GPIO0_GPIO_OUT_59	MAIN_GPIOMUX_INTROUTER0_IN_IN_59
	GPIO0_GPIO_OUT_60	MAIN_GPIOMUX_INTROUTER0_IN_IN_60
	GPIO0_GPIO_OUT_61	MAIN_GPIOMUX_INTROUTER0_IN_IN_61
	GPIO0_GPIO_OUT_62	MAIN_GPIOMUX_INTROUTER0_IN_IN_62
	GPIO0_GPIO_OUT_63	MAIN_GPIOMUX_INTROUTER0_IN_IN_63
	GPIO0_GPIO_OUT_64	MAIN_GPIOMUX_INTROUTER0_IN_IN_64
	GPIO0_GPIO_OUT_65	MAIN_GPIOMUX_INTROUTER0_IN_IN_65
	GPIO0_GPIO_OUT_66	MAIN_GPIOMUX_INTROUTER0_IN_IN_66
	GPIO0_GPIO_OUT_67	MAIN_GPIOMUX_INTROUTER0_IN_IN_67
	GPIO0_GPIO_OUT_68	MAIN_GPIOMUX_INTROUTER0_IN_IN_68
	GPIO0_GPIO_OUT_69	MAIN_GPIOMUX_INTROUTER0_IN_IN_69
	GPIO0_GPIO_OUT_70	MAIN_GPIOMUX_INTROUTER0_IN_IN_70
	GPIO0_GPIO_OUT_71	MAIN_GPIOMUX_INTROUTER0_IN_IN_71
	GPIO0_GPIO_OUT_72	MAIN_GPIOMUX_INTROUTER0_IN_IN_72
	GPIO0_GPIO_OUT_73	MAIN_GPIOMUX_INTROUTER0_IN_IN_73
	GPIO0_GPIO_OUT_74	MAIN_GPIOMUX_INTROUTER0_IN_IN_74
	GPIO0_GPIO_OUT_75	MAIN_GPIOMUX_INTROUTER0_IN_IN_75
	GPIO0_GPIO_OUT_76	MAIN_GPIOMUX_INTROUTER0_IN_IN_76
	GPIO0_GPIO_OUT_77	MAIN_GPIOMUX_INTROUTER0_IN_IN_77
	GPIO0_GPIO_OUT_78	MAIN_GPIOMUX_INTROUTER0_IN_IN_78
	GPIO0_GPIO_OUT_79	MAIN_GPIOMUX_INTROUTER0_IN_IN_79
	GPIO0_GPIO_OUT_80	MAIN_GPIOMUX_INTROUTER0_IN_IN_80

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_81	MAIN_GPIOMUX_INTROUTER0_IN_IN_81
	GPIO0_GPIO_OUT_82	MAIN_GPIOMUX_INTROUTER0_IN_IN_82
	GPIO0_GPIO_OUT_83	MAIN_GPIOMUX_INTROUTER0_IN_IN_83
	GPIO0_GPIO_OUT_84	MAIN_GPIOMUX_INTROUTER0_IN_IN_84
	GPIO0_GPIO_OUT_85	MAIN_GPIOMUX_INTROUTER0_IN_IN_85
	GPIO0_GPIO_OUT_86	MAIN_GPIOMUX_INTROUTER0_IN_IN_86
	GPIO0_GPIO_OUT_87	MAIN_GPIOMUX_INTROUTER0_IN_IN_87
	GPIO0_GPIO_OUT_88	MAIN_GPIOMUX_INTROUTER0_IN_IN_88
	GPIO0_GPIO_OUT_89	MAIN_GPIOMUX_INTROUTER0_IN_IN_89
	GPIO0_GPIO_BANK_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_190
	GPIO0_GPIO_BANK_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_191
	GPIO0_GPIO_BANK_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_192
	GPIO0_GPIO_BANK_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_193
	GPIO0_GPIO_BANK_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_194
	GPIO0_GPIO_BANK_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_195
	GPIO0_GPIO_BANK_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_196
	GPIO0_GPIO_BANK_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_197
	GPIO0_GPIO_BANK_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_198
GPIO1	GPIO1_GPIO_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_90
	GPIO1_GPIO_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_91
	GPIO1_GPIO_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_92
	GPIO1_GPIO_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_93
	GPIO1_GPIO_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_94
	GPIO1_GPIO_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_95
	GPIO1_GPIO_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_96
	GPIO1_GPIO_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_97
	GPIO1_GPIO_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_98
	GPIO1_GPIO_OUT_9	MAIN_GPIOMUX_INTROUTER0_IN_IN_99
	GPIO1_GPIO_OUT_10	MAIN_GPIOMUX_INTROUTER0_IN_IN_100
	GPIO1_GPIO_OUT_11	MAIN_GPIOMUX_INTROUTER0_IN_IN_101
	GPIO1_GPIO_OUT_12	MAIN_GPIOMUX_INTROUTER0_IN_IN_102
	GPIO1_GPIO_OUT_13	MAIN_GPIOMUX_INTROUTER0_IN_IN_103
	GPIO1_GPIO_OUT_14	MAIN_GPIOMUX_INTROUTER0_IN_IN_104

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO1	GPIO1_GPIO_OUT_15	MAIN_GPIOMUX_INTROUTER0_IN_IN_105
	GPIO1_GPIO_OUT_16	MAIN_GPIOMUX_INTROUTER0_IN_IN_106
	GPIO1_GPIO_OUT_17	MAIN_GPIOMUX_INTROUTER0_IN_IN_107
	GPIO1_GPIO_OUT_18	MAIN_GPIOMUX_INTROUTER0_IN_IN_108
	GPIO1_GPIO_OUT_19	MAIN_GPIOMUX_INTROUTER0_IN_IN_109
	GPIO1_GPIO_OUT_20	MAIN_GPIOMUX_INTROUTER0_IN_IN_110
	GPIO1_GPIO_OUT_21	MAIN_GPIOMUX_INTROUTER0_IN_IN_111
	GPIO1_GPIO_OUT_22	MAIN_GPIOMUX_INTROUTER0_IN_IN_112
	GPIO1_GPIO_OUT_23	MAIN_GPIOMUX_INTROUTER0_IN_IN_113
	GPIO1_GPIO_OUT_24	MAIN_GPIOMUX_INTROUTER0_IN_IN_114
	GPIO1_GPIO_OUT_25	MAIN_GPIOMUX_INTROUTER0_IN_IN_115
	GPIO1_GPIO_OUT_26	MAIN_GPIOMUX_INTROUTER0_IN_IN_116
	GPIO1_GPIO_OUT_27	MAIN_GPIOMUX_INTROUTER0_IN_IN_117
	GPIO1_GPIO_OUT_28	MAIN_GPIOMUX_INTROUTER0_IN_IN_118
	GPIO1_GPIO_OUT_29	MAIN_GPIOMUX_INTROUTER0_IN_IN_119
	GPIO1_GPIO_OUT_30	MAIN_GPIOMUX_INTROUTER0_IN_IN_120
	GPIO1_GPIO_OUT_31	MAIN_GPIOMUX_INTROUTER0_IN_IN_121
	GPIO1_GPIO_OUT_32	MAIN_GPIOMUX_INTROUTER0_IN_IN_122
	GPIO1_GPIO_OUT_33	MAIN_GPIOMUX_INTROUTER0_IN_IN_123
	GPIO1_GPIO_OUT_34	MAIN_GPIOMUX_INTROUTER0_IN_IN_124
	GPIO1_GPIO_OUT_35	MAIN_GPIOMUX_INTROUTER0_IN_IN_125
	GPIO1_GPIO_OUT_36	MAIN_GPIOMUX_INTROUTER0_IN_IN_126
	GPIO1_GPIO_OUT_37	MAIN_GPIOMUX_INTROUTER0_IN_IN_127
	GPIO1_GPIO_OUT_38	MAIN_GPIOMUX_INTROUTER0_IN_IN_128
	GPIO1_GPIO_OUT_39	MAIN_GPIOMUX_INTROUTER0_IN_IN_129
	GPIO1_GPIO_OUT_40	MAIN_GPIOMUX_INTROUTER0_IN_IN_130
	GPIO1_GPIO_OUT_41	MAIN_GPIOMUX_INTROUTER0_IN_IN_131
	GPIO1_GPIO_OUT_42	MAIN_GPIOMUX_INTROUTER0_IN_IN_132
	GPIO1_GPIO_OUT_43	MAIN_GPIOMUX_INTROUTER0_IN_IN_133
	GPIO1_GPIO_OUT_44	MAIN_GPIOMUX_INTROUTER0_IN_IN_134
	GPIO1_GPIO_OUT_45	MAIN_GPIOMUX_INTROUTER0_IN_IN_135
	GPIO1_GPIO_OUT_46	MAIN_GPIOMUX_INTROUTER0_IN_IN_136
	GPIO1_GPIO_OUT_47	MAIN_GPIOMUX_INTROUTER0_IN_IN_137

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO1	GPIO1_GPIO_OUT_48	MAIN_GPIOMUX_INTROUTER0_IN_IN_138
	GPIO1_GPIO_OUT_49	MAIN_GPIOMUX_INTROUTER0_IN_IN_139
	GPIO1_GPIO_OUT_50	MAIN_GPIOMUX_INTROUTER0_IN_IN_140
	GPIO1_GPIO_OUT_51	MAIN_GPIOMUX_INTROUTER0_IN_IN_141
	GPIO1_GPIO_OUT_52	MAIN_GPIOMUX_INTROUTER0_IN_IN_142
	GPIO1_GPIO_OUT_53	MAIN_GPIOMUX_INTROUTER0_IN_IN_143
	GPIO1_GPIO_OUT_54	MAIN_GPIOMUX_INTROUTER0_IN_IN_144
	GPIO1_GPIO_OUT_55	MAIN_GPIOMUX_INTROUTER0_IN_IN_145
	GPIO1_GPIO_OUT_56	MAIN_GPIOMUX_INTROUTER0_IN_IN_146
	GPIO1_GPIO_OUT_57	MAIN_GPIOMUX_INTROUTER0_IN_IN_147
	GPIO1_GPIO_OUT_58	MAIN_GPIOMUX_INTROUTER0_IN_IN_148
	GPIO1_GPIO_OUT_59	MAIN_GPIOMUX_INTROUTER0_IN_IN_149
	GPIO1_GPIO_OUT_60	MAIN_GPIOMUX_INTROUTER0_IN_IN_150
	GPIO1_GPIO_OUT_61	MAIN_GPIOMUX_INTROUTER0_IN_IN_151
	GPIO1_GPIO_OUT_62	MAIN_GPIOMUX_INTROUTER0_IN_IN_152
	GPIO1_GPIO_OUT_63	MAIN_GPIOMUX_INTROUTER0_IN_IN_153
	GPIO1_GPIO_OUT_64	MAIN_GPIOMUX_INTROUTER0_IN_IN_154
	GPIO1_GPIO_OUT_65	MAIN_GPIOMUX_INTROUTER0_IN_IN_155
	GPIO1_GPIO_OUT_66	MAIN_GPIOMUX_INTROUTER0_IN_IN_156
	GPIO1_GPIO_OUT_67	MAIN_GPIOMUX_INTROUTER0_IN_IN_157
	GPIO1_GPIO_OUT_68	MAIN_GPIOMUX_INTROUTER0_IN_IN_158
	GPIO1_GPIO_OUT_69	MAIN_GPIOMUX_INTROUTER0_IN_IN_159
	GPIO1_GPIO_OUT_70	MAIN_GPIOMUX_INTROUTER0_IN_IN_160
	GPIO1_GPIO_OUT_71	MAIN_GPIOMUX_INTROUTER0_IN_IN_161
	GPIO1_GPIO_OUT_72	MAIN_GPIOMUX_INTROUTER0_IN_IN_162
	GPIO1_GPIO_OUT_73	MAIN_GPIOMUX_INTROUTER0_IN_IN_163
	GPIO1_GPIO_OUT_74	MAIN_GPIOMUX_INTROUTER0_IN_IN_164
	GPIO1_GPIO_OUT_75	MAIN_GPIOMUX_INTROUTER0_IN_IN_165
	GPIO1_GPIO_OUT_76	MAIN_GPIOMUX_INTROUTER0_IN_IN_166
	GPIO1_GPIO_OUT_77	MAIN_GPIOMUX_INTROUTER0_IN_IN_167
	GPIO1_GPIO_OUT_78	MAIN_GPIOMUX_INTROUTER0_IN_IN_168
	GPIO1_GPIO_OUT_79	MAIN_GPIOMUX_INTROUTER0_IN_IN_169
	GPIO1_GPIO_OUT_80	MAIN_GPIOMUX_INTROUTER0_IN_IN_170

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO1	GPIO1_GPIO_OUT_81	MAIN_GPIOMUX_INTROUTER0_IN_IN_171
	GPIO1_GPIO_OUT_82	MAIN_GPIOMUX_INTROUTER0_IN_IN_172
	GPIO1_GPIO_OUT_83	MAIN_GPIOMUX_INTROUTER0_IN_IN_173
	GPIO1_GPIO_OUT_84	MAIN_GPIOMUX_INTROUTER0_IN_IN_174
	GPIO1_GPIO_OUT_85	MAIN_GPIOMUX_INTROUTER0_IN_IN_175
	GPIO1_GPIO_OUT_86	MAIN_GPIOMUX_INTROUTER0_IN_IN_176
	GPIO1_GPIO_OUT_87	MAIN_GPIOMUX_INTROUTER0_IN_IN_177
	GPIO1_GPIO_OUT_88	MAIN_GPIOMUX_INTROUTER0_IN_IN_178
	GPIO1_GPIO_OUT_89	MAIN_GPIOMUX_INTROUTER0_IN_IN_179
	GPIO1_GPIO_BANK_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_180
	GPIO1_GPIO_BANK_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_181
	GPIO1_GPIO_BANK_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_182
	GPIO1_GPIO_BANK_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_183
	GPIO1_GPIO_BANK_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_184
	GPIO1_GPIO_BANK_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_185
	GPIO1_GPIO_BANK_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_186
	GPIO1_GPIO_BANK_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_187
	GPIO1_GPIO_BANK_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_188
MCU_GPIO0	MCU_GPIO0_GPIO_OUT_0	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_0
	MCU_GPIO0_GPIO_OUT_1	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_1
	MCU_GPIO0_GPIO_OUT_2	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_2
	MCU_GPIO0_GPIO_OUT_3	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_3
	MCU_GPIO0_GPIO_OUT_4	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_4
	MCU_GPIO0_GPIO_OUT_5	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_5
	MCU_GPIO0_GPIO_OUT_6	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_6
	MCU_GPIO0_GPIO_OUT_7	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_7
	MCU_GPIO0_GPIO_OUT_8	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_8
	MCU_GPIO0_GPIO_OUT_9	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_9
	MCU_GPIO0_GPIO_OUT_10	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_10
	MCU_GPIO0_GPIO_OUT_11	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_11
	MCU_GPIO0_GPIO_OUT_12	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_12
	MCU_GPIO0_GPIO_OUT_13	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_13
	MCU_GPIO0_GPIO_OUT_14	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_14

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_GPIO0	MCU_GPIO0_GPIO_OUT_15	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_15
	MCU_GPIO0_GPIO_OUT_16	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_16
	MCU_GPIO0_GPIO_OUT_17	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_17
	MCU_GPIO0_GPIO_OUT_18	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_18
	MCU_GPIO0_GPIO_OUT_19	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_19
	MCU_GPIO0_GPIO_OUT_20	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_20
	MCU_GPIO0_GPIO_OUT_21	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_21
	MCU_GPIO0_GPIO_OUT_22	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_22
	MCU_GPIO0_GPIO_OUT_23	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_23
	MCU_GPIO0_GPIO_OUT_24	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_24
	MCU_GPIO0_GPIO_OUT_25	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_25
	MCU_GPIO0_GPIO_OUT_26	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_26
	MCU_GPIO0_GPIO_OUT_27	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_27
	MCU_GPIO0_GPIO_OUT_28	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_28
	MCU_GPIO0_GPIO_OUT_29	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_29
	MCU_GPIO0_GPIO_BANK_OUT_0	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_30
	MCU_GPIO0_GPIO_BANK_OUT_1	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_31
GPMC0	GPMC0_GPMC_SDMAREQ_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_29
	GPMC0_GPMC_SINTERRUPT_OUT_0	GICSS0_SPI_IN_138
	GPMC0_GPMC_SINTERRUPT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_90
	GPMC0_GPMC_SINTERRUPT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_90
	GPMC0_GPMC_SINTERRUPT_OUT_0	R5FSS0_CORE0_INTR_IN_239
	GPMC0_GPMC_SINTERRUPT_OUT_0	R5FSS0_CORE1_INTR_IN_239
	GPMC0_GPMC_SINTERRUPT_OUT_0	R5FSS1_CORE0_INTR_IN_239
	GPMC0_GPMC_SINTERRUPT_OUT_0	R5FSS1_CORE1_INTR_IN_239
GTC0	GTC0_GTC_PUSH_EVENT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_36
PRU_ICSSG0	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_53
	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_194
	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0	GICSS0_SPI_IN_167
	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0	R5FSS0_CORE0_INTR_IN_170
	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0	R5FSS0_CORE1_INTR_IN_170
	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0	R5FSS1_CORE0_INTR_IN_170
	PRU_ICSSG0_ISO_RESET_PROTCOL_ACK_OUT_0	R5FSS1_CORE1_INTR_IN_170

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PRU_ICSSG0	PRU_ICSSG0_PR1_ECC_DED_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_76
	PRU_ICSSG0_PR1_ECC_SEC_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_13
	PRU_ICSSG0_PR1_EDC0_SYNC0_OUT_OUT_0	PINFUNCTION_PRG0_IEP0_EDC_SYNC_OUT0OUT_PRG0_IEP0_EDC_SYNC_OUT0_IN_0
	PRU_ICSSG0_PR1_EDC0_SYNC0_OUT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_25
	PRU_ICSSG0_PR1_EDC0_SYNC1_OUT_OUT_0	PINFUNCTION_PRG0_IEP0_EDC_SYNC_OUT1OUT_PRG0_IEP0_EDC_SYNC_OUT1_IN_0
	PRU_ICSSG0_PR1_EDC0_SYNC1_OUT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_26
	PRU_ICSSG0_PR1_EDC1_SYNC0_OUT_OUT_0	PINFUNCTION_PRG0_IEP1_EDC_SYNC_OUT0OUT_PRG0_IEP1_EDC_SYNC_OUT0_IN_0
	PRU_ICSSG0_PR1_EDC1_SYNC0_OUT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_27
	PRU_ICSSG0_PR1_EDC1_SYNC1_OUT_OUT_0	PINFUNCTION_PRG0_IEP1_EDC_SYNC_OUT1OUT_PRG0_IEP1_EDC_SYNC_OUT1_IN_0
	PRU_ICSSG0_PR1_EDC1_SYNC1_OUT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_28
	PRU_ICSSG0_PR1_EDIO0_WD_TRIIG_OUT_0	ESM0_ESM_LVL_EVENT_IN_68
	PRU_ICSSG0_PR1_EDIO1_WD_TRIIG_OUT_0	ESM0_ESM_LVL_EVENT_IN_70
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0	GICSS0_SPI_IN_120
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_120
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_120
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_120
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_120
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1	GICSS0_SPI_IN_121
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1	R5FSS0_CORE0_INTR_IN_121
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_121
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1	R5FSS1_CORE0_INTR_IN_121
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_1	R5FSS1_CORE1_INTR_IN_121
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2	GICSS0_SPI_IN_122
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2	R5FSS0_CORE0_INTR_IN_122
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2	R5FSS0_CORE1_INTR_IN_122
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2	R5FSS1_CORE0_INTR_IN_122
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_2	R5FSS1_CORE1_INTR_IN_122
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3	GICSS0_SPI_IN_123
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3	R5FSS0_CORE0_INTR_IN_123
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3	R5FSS0_CORE1_INTR_IN_123
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3	R5FSS1_CORE0_INTR_IN_123
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_3	R5FSS1_CORE1_INTR_IN_123
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4	GICSS0_SPI_IN_124

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PRU_ICSSG0	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4	R5FSS0_CORE0_INTR_IN_124
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4	R5FSS0_CORE1_INTR_IN_124
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4	R5FSS1_CORE0_INTR_IN_124
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_4	R5FSS1_CORE1_INTR_IN_124
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5	GICSS0_SPI_IN_125
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5	PRU_ICSSG1_PR1_SLV_INTR_IN_87
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5	R5FSS0_CORE0_INTR_IN_125
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5	R5FSS0_CORE1_INTR_IN_125
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5	R5FSS1_CORE0_INTR_IN_125
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_5	R5FSS1_CORE1_INTR_IN_125
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6	EPWM0_EPWM_SYNCIN_IN_0
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6	MCU_M4FSS0_CORE0_NVIC_IN_51
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6	GICSS0_SPI_IN_126
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6	PRU_ICSSG1_PR1_SLV_INTR_IN_88
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6	R5FSS0_CORE0_INTR_IN_126
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6	R5FSS0_CORE1_INTR_IN_126
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6	R5FSS1_CORE0_INTR_IN_126
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_6	R5FSS1_CORE1_INTR_IN_126
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	EPWM3_EPWM_SYNCIN_IN_0
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	EPWM6_EPWM_SYNCIN_IN_0
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	MCU_M4FSS0_CORE0_NVIC_IN_52
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	GICSS0_SPI_IN_127
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	PRU_ICSSG1_PR1_SLV_INTR_IN_89
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	R5FSS0_CORE0_INTR_IN_127
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	R5FSS0_CORE1_INTR_IN_127
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	R5FSS1_CORE0_INTR_IN_127
	PRU_ICSSG0_PR1_HOST_INTR_PEND_OUT_7	R5FSS1_CORE1_INTR_IN_127
	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_0
	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_1	CMP_EVENT_INTROUTER0_IN_IN_1
	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_2	CMP_EVENT_INTROUTER0_IN_IN_2
	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_3	CMP_EVENT_INTROUTER0_IN_IN_3
	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_4	CMP_EVENT_INTROUTER0_IN_IN_4
	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_5	CMP_EVENT_INTROUTER0_IN_IN_5

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PRU_ICSSG0	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_6	CMP_EVENT_INTROUTER0_IN_IN_6
	PRU_ICSSG0_PR1_HOST_INTR_REQ_OUT_7	CMP_EVENT_INTROUTER0_IN_IN_7
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_16
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_1	CMP_EVENT_INTROUTER0_IN_IN_17
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_2	CMP_EVENT_INTROUTER0_IN_IN_18
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_3	CMP_EVENT_INTROUTER0_IN_IN_19
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_4	CMP_EVENT_INTROUTER0_IN_IN_20
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_5	CMP_EVENT_INTROUTER0_IN_IN_21
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_6	CMP_EVENT_INTROUTER0_IN_IN_22
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_7	CMP_EVENT_INTROUTER0_IN_IN_23
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_8	CMP_EVENT_INTROUTER0_IN_IN_24
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_9	CMP_EVENT_INTROUTER0_IN_IN_25
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_10	CMP_EVENT_INTROUTER0_IN_IN_26
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_11	CMP_EVENT_INTROUTER0_IN_IN_27
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_12	CMP_EVENT_INTROUTER0_IN_IN_28
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_13	CMP_EVENT_INTROUTER0_IN_IN_29
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_14	CMP_EVENT_INTROUTER0_IN_IN_30
	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_OUT_15	CMP_EVENT_INTROUTER0_IN_IN_31
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_32
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_1	CMP_EVENT_INTROUTER0_IN_IN_33
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_2	CMP_EVENT_INTROUTER0_IN_IN_34
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_3	CMP_EVENT_INTROUTER0_IN_IN_35
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_4	CMP_EVENT_INTROUTER0_IN_IN_36
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_5	CMP_EVENT_INTROUTER0_IN_IN_37
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_6	CMP_EVENT_INTROUTER0_IN_IN_38
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_7	CMP_EVENT_INTROUTER0_IN_IN_39
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_8	CMP_EVENT_INTROUTER0_IN_IN_40
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_9	CMP_EVENT_INTROUTER0_IN_IN_41
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_10	CMP_EVENT_INTROUTER0_IN_IN_42
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_11	CMP_EVENT_INTROUTER0_IN_IN_43
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_12	CMP_EVENT_INTROUTER0_IN_IN_44
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_13	CMP_EVENT_INTROUTER0_IN_IN_45
	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_14	CMP_EVENT_INTROUTER0_IN_IN_46

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PRU_ICSSG0	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_OUT_15	CMP_EVENT_INTROUTER0_IN_IN_47
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0	GICSS0_SPI_IN_244
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0	R5FSS0_CORE0_INTR_IN_244
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0	R5FSS0_CORE1_INTR_IN_244
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0	R5FSS1_CORE0_INTR_IN_244
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_0	R5FSS1_CORE1_INTR_IN_244
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1	GICSS0_SPI_IN_245
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1	R5FSS0_CORE0_INTR_IN_245
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1	R5FSS0_CORE1_INTR_IN_245
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1	R5FSS1_CORE0_INTR_IN_245
	PRU_ICSSG0_PR1_RX_SOF_INTR_REQ_OUT_1	R5FSS1_CORE1_INTR_IN_245
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0	GICSS0_SPI_IN_246
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0	R5FSS0_CORE0_INTR_IN_246
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0	R5FSS0_CORE1_INTR_IN_246
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0	R5FSS1_CORE0_INTR_IN_246
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_0	R5FSS1_CORE1_INTR_IN_246
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1	GICSS0_SPI_IN_247
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1	R5FSS0_CORE0_INTR_IN_247
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1	R5FSS0_CORE1_INTR_IN_247
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1	R5FSS1_CORE0_INTR_IN_247
	PRU_ICSSG0_PR1_TX_SOF_INTR_REQ_OUT_1	R5FSS1_CORE1_INTR_IN_247
PRU_ICSSG1	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_54
	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_195
	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0	GICSS0_SPI_IN_168
	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0	R5FSS0_CORE0_INTR_IN_172
	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0	R5FSS0_CORE1_INTR_IN_172
	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0	R5FSS1_CORE0_INTR_IN_172
	PRU_ICSSG1_ISO_RESET_PROTCOL_ACK_OUT_0	R5FSS1_CORE1_INTR_IN_172
	PRU_ICSSG1_PR1_ECC_DED_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_77
	PRU_ICSSG1_PR1_ECC_SEC_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_14
	PRU_ICSSG1_PR1_EDC0_SYNC0_OUT_OUT_0	PINFUNCTION_PRG1_IEP0_EDC_SYNC_OUT0OUT_PRG1_IEP0_EDC_SYNC_OUT0_IN_0
	PRU_ICSSG1_PR1_EDC0_SYNC0_OUT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_29
	PRU_ICSSG1_PR1_EDC0_SYNC1_OUT_OUT_0	PINFUNCTION_PRG1_IEP0_EDC_SYNC_OUT1OUT_PRG1_IEP0_EDC_SYNC_OUT1_IN_0

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PRU_ICSSG1	PRU_ICSSG1_PR1_EDC0_SYNC1_OUT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_30
	PRU_ICSSG1_PR1_EDC1_SYNC0_OUT_OUT_0	PINFUNCTION_PRG1_IEP1_EDC_SYNC_OUT0OUT_PRG1_IEP1_EDC_SYNC_OUT0_IN_0
	PRU_ICSSG1_PR1_EDC1_SYNC0_OUT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_31
	PRU_ICSSG1_PR1_EDC1_SYNC1_OUT_OUT_0	PINFUNCTION_PRG1_IEP1_EDC_SYNC_OUT1OUT_PRG1_IEP1_EDC_SYNC_OUT1_IN_0
	PRU_ICSSG1_PR1_EDC1_SYNC1_OUT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_32
	PRU_ICSSG1_PR1_EDIO0_WD_TRIIG_OUT_0	ESM0_ESM_LVL_EVENT_IN_96
	PRU_ICSSG1_PR1_EDIO1_WD_TRIIG_OUT_0	ESM0_ESM_LVL_EVENT_IN_97
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0	GICSS0_SPI_IN_248
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_248
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_248
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_248
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_248
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1	GICSS0_SPI_IN_249
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1	R5FSS0_CORE0_INTR_IN_249
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_249
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1	R5FSS1_CORE0_INTR_IN_249
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_1	R5FSS1_CORE1_INTR_IN_249
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2	GICSS0_SPI_IN_250
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2	R5FSS0_CORE0_INTR_IN_250
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2	R5FSS0_CORE1_INTR_IN_250
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2	R5FSS1_CORE0_INTR_IN_250
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_2	R5FSS1_CORE1_INTR_IN_250
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3	GICSS0_SPI_IN_251
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3	R5FSS0_CORE0_INTR_IN_251
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3	R5FSS0_CORE1_INTR_IN_251
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3	R5FSS1_CORE0_INTR_IN_251
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_3	R5FSS1_CORE1_INTR_IN_251
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4	GICSS0_SPI_IN_252
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4	R5FSS0_CORE0_INTR_IN_252
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4	R5FSS0_CORE1_INTR_IN_252
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4	R5FSS1_CORE0_INTR_IN_252
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_4	R5FSS1_CORE1_INTR_IN_252
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5	GICSS0_SPI_IN_253

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PRU_ICSSG1	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5	PRU_ICSSG0_PR1_SLV_INTR_IN_87
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5	R5FSS0_CORE0_INTR_IN_253
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5	R5FSS0_CORE1_INTR_IN_253
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5	R5FSS1_CORE0_INTR_IN_253
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_5	R5FSS1_CORE1_INTR_IN_253
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6	MCU_M4FSS0_CORE0_NVIC_IN_62
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6	GICSS0_SPI_IN_254
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6	PRU_ICSSG0_PR1_SLV_INTR_IN_88
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6	R5FSS0_CORE0_INTR_IN_254
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6	R5FSS0_CORE1_INTR_IN_254
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6	R5FSS1_CORE0_INTR_IN_254
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_6	R5FSS1_CORE1_INTR_IN_254
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7	MCU_M4FSS0_CORE0_NVIC_IN_63
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7	GICSS0_SPI_IN_255
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7	PRU_ICSSG0_PR1_SLV_INTR_IN_89
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7	R5FSS0_CORE0_INTR_IN_255
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7	R5FSS0_CORE1_INTR_IN_255
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7	R5FSS1_CORE0_INTR_IN_255
	PRU_ICSSG1_PR1_HOST_INTR_PEND_OUT_7	R5FSS1_CORE1_INTR_IN_255
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_8
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_1	CMP_EVENT_INTROUTER0_IN_IN_9
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_2	CMP_EVENT_INTROUTER0_IN_IN_10
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_3	CMP_EVENT_INTROUTER0_IN_IN_11
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_4	CMP_EVENT_INTROUTER0_IN_IN_12
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_5	CMP_EVENT_INTROUTER0_IN_IN_13
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_6	EPWM0_EPWM_SYNCIN_IN_0
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_6	CMP_EVENT_INTROUTER0_IN_IN_14
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_7	EPWM3_EPWM_SYNCIN_IN_0
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_7	EPWM6_EPWM_SYNCIN_IN_0
	PRU_ICSSG1_PR1_HOST_INTR_REQ_OUT_7	CMP_EVENT_INTROUTER0_IN_IN_15
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_48
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_1	CMP_EVENT_INTROUTER0_IN_IN_49
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_2	CMP_EVENT_INTROUTER0_IN_IN_50

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PRU_ICSSG1	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_3	CMP_EVENT_INTROUTER0_IN_IN_51
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_4	CMP_EVENT_INTROUTER0_IN_IN_52
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_5	CMP_EVENT_INTROUTER0_IN_IN_53
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_6	CMP_EVENT_INTROUTER0_IN_IN_54
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_7	CMP_EVENT_INTROUTER0_IN_IN_55
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_8	CMP_EVENT_INTROUTER0_IN_IN_56
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_9	CMP_EVENT_INTROUTER0_IN_IN_57
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_10	CMP_EVENT_INTROUTER0_IN_IN_58
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_11	CMP_EVENT_INTROUTER0_IN_IN_59
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_12	CMP_EVENT_INTROUTER0_IN_IN_60
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_13	CMP_EVENT_INTROUTER0_IN_IN_61
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_14	CMP_EVENT_INTROUTER0_IN_IN_62
	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_OUT_15	CMP_EVENT_INTROUTER0_IN_IN_63
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_64
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_1	CMP_EVENT_INTROUTER0_IN_IN_65
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_2	CMP_EVENT_INTROUTER0_IN_IN_66
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_3	CMP_EVENT_INTROUTER0_IN_IN_67
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_4	CMP_EVENT_INTROUTER0_IN_IN_68
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_5	CMP_EVENT_INTROUTER0_IN_IN_69
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_6	CMP_EVENT_INTROUTER0_IN_IN_70
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_7	CMP_EVENT_INTROUTER0_IN_IN_71
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_8	CMP_EVENT_INTROUTER0_IN_IN_72
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_9	CMP_EVENT_INTROUTER0_IN_IN_73
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_10	CMP_EVENT_INTROUTER0_IN_IN_74
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_11	CMP_EVENT_INTROUTER0_IN_IN_75
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_12	CMP_EVENT_INTROUTER0_IN_IN_76
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_13	CMP_EVENT_INTROUTER0_IN_IN_77
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_14	CMP_EVENT_INTROUTER0_IN_IN_78
	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_OUT_15	CMP_EVENT_INTROUTER0_IN_IN_79
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0	GICSS0_SPI_IN_240
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0	R5FSS0_CORE0_INTR_IN_240
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0	R5FSS0_CORE1_INTR_IN_240
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0	R5FSS1_CORE0_INTR_IN_240

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PRU_ICSSG1	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_0	R5FSS1_CORE1_INTR_IN_240
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1	GICSS0_SPI_IN_241
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1	R5FSS0_CORE0_INTR_IN_241
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1	R5FSS0_CORE1_INTR_IN_241
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1	R5FSS1_CORE0_INTR_IN_241
	PRU_ICSSG1_PR1_RX_SOF_INTR_REQ_OUT_1	R5FSS1_CORE1_INTR_IN_241
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0	GICSS0_SPI_IN_242
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0	R5FSS0_CORE0_INTR_IN_242
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0	R5FSS0_CORE1_INTR_IN_242
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0	R5FSS1_CORE0_INTR_IN_242
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_0	R5FSS1_CORE1_INTR_IN_242
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1	GICSS0_SPI_IN_243
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1	R5FSS0_CORE0_INTR_IN_243
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1	R5FSS0_CORE1_INTR_IN_243
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1	R5FSS1_CORE0_INTR_IN_243
	PRU_ICSSG1_PR1_TX_SOF_INTR_REQ_OUT_1	R5FSS1_CORE1_INTR_IN_243
DFTSS0	DFTSS0_DFT_SAFETY_123_OUT_0	ESM0_ESM_LVL_EVENT_IN_98
	DFTSS0_DFT_SAFETY_MULTI_OUT_0	ESM0_ESM_LVL_EVENT_IN_99
	DFTSS0_DFT_SAFETY_ONE_OUT_0	ESM0_ESM_LVL_EVENT_IN_100
MAIN_16FF0	MAIN_16FF0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_101
	MAIN_16FF0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_102
CPTS0	CPTS0_CPTS_COMP_OUT_0	PINFUNCTION_CPTS0_TS_COMPOUT_CPTS0_TS_COMP_IN_0
	CPTS0_CPTS_COMP_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_82
	CPTS0_CPTS_GENF0_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_16
	CPTS0_CPTS_GENF1_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_17
	CPTS0_CPTS_GENF2_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_18
	CPTS0_CPTS_GENF3_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_19
	CPTS0_CPTS_GENF4_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_20
	CPTS0_CPTS_GENF5_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_24
	CPTS0_CPTS_SYNC_OUT_0	PINFUNCTION_CPTS0_TS_SYNCOUT_CPTS0_TS_SYNC_IN_0
	CPTS0_CPTS_SYNC_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_35
	CPTS0_EVNT_PEND_OUT_0	GICSS0_SPI_IN_129
	CPTS0_EVNT_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_129

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CPTS0	CPTS0_EVNT_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_129
	CPTS0_EVNT_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_129
	CPTS0_EVNT_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_129
DDPA0	DDPA0_DDPA_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_29
	DDPA0_DDPA_INTR_OUT_0	DMSC0_MISC_0_DEBUG_FORCEACTIVE_IN_0
	DDPA0_DDPA_INTR_OUT_0	GICSS0_SPI_IN_177
	DDPA0_DDPA_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_177
	DDPA0_DDPA_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_177
	DDPA0_DDPA_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_177
	DDPA0_DDPA_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_177
EPWM0	EPWM0_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_12
	EPWM0_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_12
	EPWM0_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_108
	EPWM0_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_108
	EPWM0_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_108
	EPWM0_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_108
	EPWM0_EPWM_SYNCO_O_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_39
	EPWM0_EPWM_SYNCOUT_OUT_0	EPWM1_EPWM_SYNCIN_IN_0
	EPWM0_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_13
	EPWM0_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_13
	EPWM0_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_109
	EPWM0_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_109
	EPWM0_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_109
	EPWM0_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_109
EPWM1	EPWM1_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_14
	EPWM1_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_14
	EPWM1_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_110
	EPWM1_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_110
	EPWM1_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_110
	EPWM1_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_110
	EPWM1_EPWM_SYNCOUT_OUT_0	EPWM2_EPWM_SYNCIN_IN_0
	EPWM1_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_15
	EPWM1_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_15

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
EPWM1	EPWM1_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_111
	EPWM1_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_111
	EPWM1_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_111
	EPWM1_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_111
EPWM2	EPWM2_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_16
	EPWM2_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_16
	EPWM2_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_112
	EPWM2_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_112
	EPWM2_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_112
	EPWM2_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_112
	EPWM2_EPWM_SYNCOUT_OUT_0	EPWM3_EPWM_SYNCIN_IN_0
	EPWM2_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_17
	EPWM2_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_17
	EPWM2_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_113
	EPWM2_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_113
	EPWM2_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_113
	EPWM2_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_113
EPWM3	EPWM3_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_18
	EPWM3_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_18
	EPWM3_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_114
	EPWM3_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_114
	EPWM3_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_114
	EPWM3_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_114
	EPWM3_EPWM_SYNCO_O_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_40
	EPWM3_EPWM_SYNCOUT_OUT_0	EPWM4_EPWM_SYNCIN_IN_0
	EPWM3_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_19
	EPWM3_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_19
	EPWM3_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_115
	EPWM3_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_115
	EPWM3_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_115
	EPWM3_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_115
EPWM4	EPWM4_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_20
	EPWM4_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_20

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
EPWM4	EPWM4_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_116
	EPWM4_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_116
	EPWM4_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_116
	EPWM4_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_116
	EPWM4_EPWM_SYNCOUT_OUT_0	EPWM5_EPWM_SYNCIN_IN_0
	EPWM4_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_21
	EPWM4_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_21
	EPWM4_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_117
	EPWM4_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_117
	EPWM4_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_117
	EPWM4_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_117
EPWM5	EPWM5_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_22
	EPWM5_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_22
	EPWM5_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_118
	EPWM5_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_118
	EPWM5_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_118
	EPWM5_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_118
	EPWM5_EPWM_SYNCOUT_OUT_0	EPWM6_EPWM_SYNCIN_IN_0
	EPWM5_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_23
	EPWM5_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_23
	EPWM5_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_139
	EPWM5_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_139
	EPWM5_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_139
	EPWM5_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_139
EPWM6	EPWM6_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_24
	EPWM6_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_24
	EPWM6_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_146
	EPWM6_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_146
	EPWM6_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_146
	EPWM6_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_146
	EPWM6_EPWM_SYNCO_O_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_41
	EPWM6_EPWM_SYNCOUT_OUT_0	EPWM7_EPWM_SYNCIN_IN_0
	EPWM6_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_25

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
EPWM6	EPWM6_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_25
	EPWM6_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_147
	EPWM6_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_147
	EPWM6_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_147
	EPWM6_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_147
EPWM7	EPWM7_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_26
	EPWM7_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_26
	EPWM7_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_148
	EPWM7_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_148
	EPWM7_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_148
	EPWM7_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_148
	EPWM7_EPWM_SYNCOUT_OUT_0	EPWM8_EPWM_SYNCIN_IN_0
	EPWM7_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_27
	EPWM7_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_27
	EPWM7_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_149
	EPWM7_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_149
	EPWM7_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_149
	EPWM7_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_149
EPWM8	EPWM8_EPWM_ETINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_28
	EPWM8_EPWM_ETINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_28
	EPWM8_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_150
	EPWM8_EPWM_ETINT_OUT_0	R5FSS0_CORE1_INTR_IN_150
	EPWM8_EPWM_ETINT_OUT_0	R5FSS1_CORE0_INTR_IN_150
	EPWM8_EPWM_ETINT_OUT_0	R5FSS1_CORE1_INTR_IN_150
	EPWM8_EPWM_TRIPZINT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_29
	EPWM8_EPWM_TRIPZINT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_29
	EPWM8_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_178
	EPWM8_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_178
	EPWM8_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_178
	EPWM8_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_178
PBIST0	PBIST0_DFT_PBIST_CPU_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_234
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_168
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_168

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PBIST0	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_168
	PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_159
PBIST1	PBIST1_DFT_PBIST_CPU_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_235
	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_170
	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_170
	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_170
	PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_158
PBIST2	PBIST2_DFT_PBIST_CPU_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_236
	PBIST2_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_172
	PBIST2_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_172
	PBIST2_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_172
	PBIST2_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_157
PBIST3	PBIST3_DFT_PBIST_CPU_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_237
	PBIST3_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_174
	PBIST3_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_174
	PBIST3_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_174
	PBIST3_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_156
VTM0	VTM0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_139
	VTM0_CORR_LEVEL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_11
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_15
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_196
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_137
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_8
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	GICSS0_SPI_IN_183
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_183
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_183
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_183
	VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_183
	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_30
	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_198
	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_138
	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_10
	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	GICSS0_SPI_IN_184

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
VTM0	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_184
	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_184
	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_184
	VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_184
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_55
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_197
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_136
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_9
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	GICSS0_SPI_IN_185
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_185
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_185
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_185
	VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_185
	VTM0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_140
	VTM0_UNCORR_LEVEL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_12
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_96
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_96
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_2	R5FSS1_CORE0_INTR_IN_96
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_3	R5FSS1_CORE1_INTR_IN_96
MAILBOX0_MAILBOX_CLUSTER_1	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_97
	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_97
	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_2	R5FSS1_CORE0_INTR_IN_97
	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_3	R5FSS1_CORE1_INTR_IN_97
MAILBOX0_MAILBOX_CLUSTER_2	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_98
	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_98
	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_2	GICSS0_SPI_IN_112
	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_3	GICSS0_SPI_IN_113
MAILBOX0_MAILBOX_CLUSTER_3	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_99
	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_99
	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_2	GICSS0_SPI_IN_114
	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_3	GICSS0_SPI_IN_115
MAILBOX0_MAILBOX_CLUSTER_4	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_98
	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS1_CORE1_INTR_IN_98

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAILBOX0_MAILBOX_CLUSTER_4	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_2	GICSS0_SPI_IN_116
	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_3	GICSS0_SPI_IN_117
MAILBOX0_MAILBOX_CLUSTER_5	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_99
	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS1_CORE1_INTR_IN_99
	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_2	GICSS0_SPI_IN_118
	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_3	GICSS0_SPI_IN_119
MAILBOX0_MAILBOX_CLUSTER_6	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_100
	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_100
	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_2	GICSS0_SPI_IN_108
	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_3	MCU_M4FSS0_CORE0_NVIC_IN_56
MAILBOX0_MAILBOX_CLUSTER_7	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_100
	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS1_CORE1_INTR_IN_100
	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_2	GICSS0_SPI_IN_109
	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_3	MCU_M4FSS0_CORE0_NVIC_IN_57
MCAN0	MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_16
	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_78
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	GICSS0_SPI_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_81
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_81
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_186
	MCAN0_MCANSS_FE_OUT_0	PDMA1_MCANSS_0_FE_IN_0
	MCAN0_MCANSS_FE_OUT_1	PDMA1_MCANSS_0_FE_IN_1
	MCAN0_MCANSS_FE_OUT_2	PDMA1_MCANSS_0_FE_IN_2
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	GICSS0_SPI_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_82
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_82
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_187

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCAN0	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	GICSS0_SPI_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	PRU_ICSSG0_PR1_SLV_INTR_IN_83
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	PRU_ICSSG1_PR1_SLV_INTR_IN_83
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE0_INTR_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE1_INTR_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE0_INTR_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE1_INTR_IN_188
	MCAN0_MCANSS_TX_DMA_OUT_0	PDMA1_MCANSS_MAIN_0_TX_IN_0
	MCAN0_MCANSS_TX_DMA_OUT_1	PDMA1_MCANSS_MAIN_0_TX_IN_1
	MCAN0_MCANSS_TX_DMA_OUT_2	PDMA1_MCANSS_MAIN_0_TX_IN_2
MCAN1	MCAN1_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_17
	MCAN1_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_79
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	GICSS0_SPI_IN_189
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_84
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_84
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_189
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_189
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_189
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_189
	MCAN1_MCANSS_FE_OUT_0	PDMA1_MCANSS_1_FE_IN_0
	MCAN1_MCANSS_FE_OUT_1	PDMA1_MCANSS_1_FE_IN_1
	MCAN1_MCANSS_FE_OUT_2	PDMA1_MCANSS_1_FE_IN_2
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	GICSS0_SPI_IN_190
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_85
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_85
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_190
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_190
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_190
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_190
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	GICSS0_SPI_IN_191
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	PRU_ICSSG0_PR1_SLV_INTR_IN_86
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	PRU_ICSSG1_PR1_SLV_INTR_IN_86
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE0_INTR_IN_191

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCAN1	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE1_INTR_IN_191
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE0_INTR_IN_191
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE1_INTR_IN_191
	MCAN1_MCANSS_TX_DMA_OUT_0	PDMA1_MCANSS_MAIN_1_TX_IN_0
	MCAN1_MCANSS_TX_DMA_OUT_1	PDMA1_MCANSS_MAIN_1_TX_IN_1
	MCAN1_MCANSS_TX_DMA_OUT_2	PDMA1_MCANSS_MAIN_1_TX_IN_2
MCU_MCRC64_0	MCU_MCRC64_0_INT_MCRC_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_16
	MCU_MCRC64_0_INT_MCRC_OUT_0	GICSS0_SPI_IN_192
	MCU_MCRC64_0_INT_MCRC_OUT_0	R5FSS0_CORE0_INTR_IN_192
	MCU_MCRC64_0_INT_MCRC_OUT_0	R5FSS0_CORE1_INTR_IN_192
	MCU_MCRC64_0_INT_MCRC_OUT_0	R5FSS1_CORE0_INTR_IN_192
	MCU_MCRC64_0_INT_MCRC_OUT_0	R5FSS1_CORE1_INTR_IN_192
I2C0	I2C0_POINTRPEND_OUT_0	GICSS0_SPI_IN_193
	I2C0_POINTRPEND_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_75
	I2C0_POINTRPEND_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_75
	I2C0_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_193
I2C1	I2C1_POINTRPEND_OUT_0	GICSS0_SPI_IN_194
	I2C1_POINTRPEND_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_76
	I2C1_POINTRPEND_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_76
	I2C1_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_194
I2C2	I2C2_POINTRPEND_OUT_0	GICSS0_SPI_IN_195
	I2C2_POINTRPEND_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_77
	I2C2_POINTRPEND_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_77
	I2C2_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_195

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
I2C3	I2C3_POINTRPEND_OUT_0	GICSS0_SPI_IN_196
	I2C3_POINTRPEND_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_78
	I2C3_POINTRPEND_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_78
	I2C3_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_196
MCU_I2C0	MCU_I2C0_POINTRPEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_17
	MCU_I2C0_POINTRPEND_OUT_0	GICSS0_SPI_IN_139
	MCU_I2C0_POINTRPEND_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_79
	MCU_I2C0_POINTRPEND_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_79
	MCU_I2C0_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_61
	MCU_I2C0_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_61
	MCU_I2C0_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_61
	MCU_I2C0_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_61
MCU_I2C1	MCU_I2C1_POINTRPEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_18
	MCU_I2C1_POINTRPEND_OUT_0	GICSS0_SPI_IN_140
	MCU_I2C1_POINTRPEND_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_80
	MCU_I2C1_POINTRPEND_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_80
	MCU_I2C1_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_62
	MCU_I2C1_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_62
	MCU_I2C1_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_62
	MCU_I2C1_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_62
MSRAM_256K0	MSRAM_256K0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_18
	MSRAM_256K0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_80
MSRAM_256K1	MSRAM_256K1_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_19
	MSRAM_256K1_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_81
MSRAM_256K2	MSRAM_256K2_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_20
	MSRAM_256K2_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_82
MSRAM_256K3	MSRAM_256K3_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_21
	MSRAM_256K3_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_83
MSRAM_256K4	MSRAM_256K4_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_22
	MSRAM_256K4_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_84

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MSRAM_256K5	MSRAM_256K5_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_23
	MSRAM_256K5_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_85
MSRAM_256K6	MSRAM_256K6_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_62
	MSRAM_256K6_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_103
MSRAM_256K7	MSRAM_256K7_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_63
	MSRAM_256K7_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_104
PCIE0	PCIE0_PCIE_CPTS_COMP_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_81
	PCIE0_PCIE_CPTS_GENF0_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_23
	PCIE0_PCIE_CPTS_HW1_PUSH_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_37
	PCIE0_PCIE_CPTS_PEND_OUT_0	GICSS0_SPI_IN_229
	PCIE0_PCIE_CPTS_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_229
	PCIE0_PCIE_CPTS_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_229
	PCIE0_PCIE_CPTS_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_229
	PCIE0_PCIE_CPTS_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_229
	PCIE0_PCIE_CPTS_SYNC_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_33
	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0	GICSS0_SPI_IN_230
	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_230
	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_230
	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_230
	PCIE0_PCIE_DOWNSTREAM_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_230
	PCIE0_PCIE_DPA_PULSE_OUT_0	GICSS0_SPI_IN_232
	PCIE0_PCIE_DPA_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_103
	PCIE0_PCIE_DPA_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_103
	PCIE0_PCIE_DPA_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_103
	PCIE0_PCIE_DPA_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_103
	PCIE0_PCIE_ECC0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_27
	PCIE0_PCIE_ECC0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_86
	PCIE0_PCIE_ECC1_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_87
	PCIE0_PCIE_ERROR_PULSE_OUT_0	GICSS0_SPI_IN_179
	PCIE0_PCIE_ERROR_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_232
	PCIE0_PCIE_ERROR_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_232
	PCIE0_PCIE_ERROR_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_232
	PCIE0_PCIE_ERROR_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_232

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PCIE0	PCIE0_PCIE_FLR_PULSE_OUT_0	GICSS0_SPI_IN_231
	PCIE0_PCIE_FLR_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_231
	PCIE0_PCIE_FLR_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_231
	PCIE0_PCIE_FLR_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_231
	PCIE0_PCIE_FLR_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_231
	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0	GICSS0_SPI_IN_233
	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_233
	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_233
	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_233
	PCIE0_PCIE_HOT_RESET_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_233
	PCIE0_PCIE_LEGACY_PULSE_OUT_0	GICSS0_SPI_IN_234
	PCIE0_PCIE_LEGACY_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_234
	PCIE0_PCIE_LEGACY_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_234
	PCIE0_PCIE_LEGACY_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_234
	PCIE0_PCIE_LEGACY_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_234
	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0	GICSS0_SPI_IN_235
	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_235
	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_235
	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_235
	PCIE0_PCIE_LINK_STATE_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_235
	PCIE0_PCIE_LOCAL_LEVEL_OUT_0	GICSS0_SPI_IN_236
	PCIE0_PCIE_LOCAL_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_236
	PCIE0_PCIE_LOCAL_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_236
	PCIE0_PCIE_LOCAL_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_236
	PCIE0_PCIE_LOCAL_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_236
	PCIE0_PCIE_PHY_LEVEL_OUT_0	GICSS0_SPI_IN_237
	PCIE0_PCIE_PHY_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_237
	PCIE0_PCIE_PHY_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_237
	PCIE0_PCIE_PHY_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_237
	PCIE0_PCIE_PHY_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_237
	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_38
	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0	GICSS0_SPI_IN_238
	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_238

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
PCIE0	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_238
	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_238
	PCIE0_PCIE_PTM_VALID_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_238
	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0	GICSS0_SPI_IN_178
	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0	R5FSS0_CORE0_INTR_IN_197
	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0	R5FSS0_CORE1_INTR_IN_197
	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0	R5FSS1_CORE0_INTR_IN_197
	PCIE0_PCIE_PWR_STATE_PULSE_OUT_0	R5FSS1_CORE1_INTR_IN_197
PDMA0	PDMA0_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_88
	PDMA0_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_15
PDMA1	PDMA1_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_89
	PDMA1_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_28
pllfracf_ssmod_16fft0	PLLFRACF_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_128
	PLLFRACF_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_54
pllfracf_ssmod_16fft1	PLLFRACF_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_129
	PLLFRACF_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_55
pllfracf_ssmod_16fft12	PLLFRACF_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_132
	PLLFRACF_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_58
pllfracf_ssmod_16fft14	PLLFRACF_SSMOD_16FFT14_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_133
	PLLFRACF_SSMOD_16FFT14_LOCKLOSS_IPCFG_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_59
pllfracf_ssmod_16fft2	PLLFRACF_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_130
	PLLFRACF_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_56
pllfracf_ssmod_16fft8	PLLFRACF_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_131
	PLLFRACF_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_57
MCU_pllfracf_ssmod_16fft0	MCU_PLLFRACF_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_134
	MCU_PLLFRACF_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_47
PSRAMECC0	PSRAMECC0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_29
	PSRAMECC0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_90
R5FSS0_CORE0	R5FSS0_CORE0_CTI_OUT_0	R5FSS0_CORE0_INTR_IN_175
	R5FSS0_CORE0_CTI_OUT_0	R5FSS0_CORE1_INTR_IN_175
	R5FSS0_CORE0_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_30
	R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_91
	R5FSS0_CORE0_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_124

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
R5FSS0_CORE0	R5FSS0_CORE0_EXP_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_4
	R5FSS0_CORE0_PMU_OUT_0	R5FSS0_CORE0_INTR_IN_58
	R5FSS0_CORE0_VALFIQ_OUT_0	R5FSS0_CORE0_INTR_IN_59
	R5FSS0_CORE0_VALIRQ_OUT_0	R5FSS0_CORE0_INTR_IN_60
R5FSS0_CORE1	R5FSS0_CORE1_CTI_OUT_0	R5FSS0_CORE0_INTR_IN_176
	R5FSS0_CORE1_CTI_OUT_0	R5FSS0_CORE1_INTR_IN_176
	R5FSS0_CORE1_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_31
	R5FSS0_CORE1_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_105
	R5FSS0_CORE1_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_125
	R5FSS0_CORE1_EXP_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_4
	R5FSS0_CORE1_PMU_OUT_0	R5FSS0_CORE1_INTR_IN_58
	R5FSS0_CORE1_VALFIQ_OUT_0	R5FSS0_CORE1_INTR_IN_59
	R5FSS0_CORE1_VALIRQ_OUT_0	R5FSS0_CORE1_INTR_IN_60
R5FSS0_COMMON0	R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0	R5FSS0_CORE0_INTR_IN_5
	R5FSS0_COMMON0_COMMRX_LEVEL_1_OUT_0	R5FSS0_CORE1_INTR_IN_5
	R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0	R5FSS0_CORE0_INTR_IN_6
	R5FSS0_COMMON0_COMMTX_LEVEL_1_OUT_0	R5FSS0_CORE1_INTR_IN_6
	R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_40
	R5FSS0_COMMON0_ECC_DE_TO_ESM_1_OUT_0	ESM0_ESM_LVL_EVENT_IN_41
	R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_42
	R5FSS0_COMMON0_ECC_SE_TO_ESM_1_OUT_0	ESM0_ESM_LVL_EVENT_IN_43
R5FSS1_CORE0	R5FSS1_CORE0_CTI_OUT_0	R5FSS1_CORE0_INTR_IN_175
	R5FSS1_CORE0_CTI_OUT_0	R5FSS1_CORE1_INTR_IN_175
	R5FSS1_CORE0_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_32
	R5FSS1_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_106
	R5FSS1_CORE0_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_126
	R5FSS1_CORE0_EXP_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_4
	R5FSS1_CORE0_PMU_OUT_0	R5FSS1_CORE0_INTR_IN_58
	R5FSS1_CORE0_VALFIQ_OUT_0	R5FSS1_CORE0_INTR_IN_59
	R5FSS1_CORE0_VALIRQ_OUT_0	R5FSS1_CORE0_INTR_IN_60
R5FSS1_CORE1	R5FSS1_CORE1_CTI_OUT_0	R5FSS1_CORE0_INTR_IN_176
	R5FSS1_CORE1_CTI_OUT_0	R5FSS1_CORE1_INTR_IN_176
	R5FSS1_CORE1_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_33

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
R5FSS1_CORE1	R5FSS1_CORE1_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_107
	R5FSS1_CORE1_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_127
	R5FSS1_CORE1_EXP_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_4
	R5FSS1_CORE1_PMU_OUT_0	R5FSS1_CORE1_INTR_IN_58
	R5FSS1_CORE1_VALFIQ_OUT_0	R5FSS1_CORE1_INTR_IN_59
	R5FSS1_CORE1_VALIRQ_OUT_0	R5FSS1_CORE1_INTR_IN_60
R5FSS1_COMMON0	R5FSS1_COMMON0_COMMRX_LEVEL_0_OUT_0	R5FSS1_CORE0_INTR_IN_5
	R5FSS1_COMMON0_COMMRX_LEVEL_1_OUT_0	R5FSS1_CORE1_INTR_IN_5
	R5FSS1_COMMON0_COMMTX_LEVEL_0_OUT_0	R5FSS1_CORE0_INTR_IN_6
	R5FSS1_COMMON0_COMMTX_LEVEL_1_OUT_0	R5FSS1_CORE1_INTR_IN_6
	R5FSS1_COMMON0_ECC_DE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_45
	R5FSS1_COMMON0_ECC_DE_TO_ESM_1_OUT_0	ESM0_ESM_LVL_EVENT_IN_46
	R5FSS1_COMMON0_ECC_SE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_47
	R5FSS1_COMMON0_ECC_SE_TO_ESM_1_OUT_0	ESM0_ESM_LVL_EVENT_IN_48
RTI0	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_160
	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_160
	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_160
	RTI0_INTR_WWD_OUT_0	GICSS0_SPI_IN_169
RTI1	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_161
	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_161
	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_161
	RTI1_INTR_WWD_OUT_0	GICSS0_SPI_IN_170
RTI8	RTI8_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_162
	RTI8_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_162
	RTI8_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_162
	RTI8_INTR_WWD_OUT_0	R5FSS0_CORE0_INTR_IN_0
RTI9	RTI9_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_163
	RTI9_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_163
	RTI9_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_163
	RTI9_INTR_WWD_OUT_0	R5FSS0_CORE1_INTR_IN_0
RTI10	RTI10_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_164
	RTI10_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_164
	RTI10_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_164

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
RTI10	RTI10_INTR_WWD_OUT_0	R5FSS1_CORE0_INTR_IN_0
RTI11	RTI11_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_165
	RTI11_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_165
	RTI11_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_165
	RTI11_INTR_WWD_OUT_0	R5FSS1_CORE1_INTR_IN_0
MCU_RTI0	MCU_RTI0_INTR_WWD_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_19
	MCU_RTI0_INTR_WWD_OUT_0	MCU_ESM0_ESM_PLS_EVENT0_IN_85
	MCU_RTI0_INTR_WWD_OUT_0	MCU_ESM0_ESM_PLS_EVENT1_IN_85
	MCU_RTI0_INTR_WWD_OUT_0	MCU_ESM0_ESM_PLS_EVENT2_IN_85
SA2_UL0	SA2_UL0_SA_UL_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_34
	SA2_UL0_SA_UL_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_92
	SA2_UL0_SA_UL_PKA_OUT_0	GICSS0_SPI_IN_199
	SA2_UL0_SA_UL_PKA_OUT_0	R5FSS0_CORE0_INTR_IN_199
	SA2_UL0_SA_UL_PKA_OUT_0	R5FSS0_CORE1_INTR_IN_199
	SA2_UL0_SA_UL_PKA_OUT_0	R5FSS1_CORE0_INTR_IN_199
	SA2_UL0_SA_UL_PKA_OUT_0	R5FSS1_CORE1_INTR_IN_199
	SA2_UL0_SA_UL_TRNG_OUT_0	GICSS0_SPI_IN_200
	SA2_UL0_SA_UL_TRNG_OUT_0	R5FSS0_CORE0_INTR_IN_200
	SA2_UL0_SA_UL_TRNG_OUT_0	R5FSS0_CORE1_INTR_IN_200
	SA2_UL0_SA_UL_TRNG_OUT_0	R5FSS1_CORE0_INTR_IN_200
	SA2_UL0_SA_UL_TRNG_OUT_0	R5FSS1_CORE1_INTR_IN_200
	SA2_UL0_SECURITY_OUT_0	DMSC0_CORTEX_M3_0_SEC_IN_IN_49
	SA2_UL0_SECURITY_OUT_0	GICSS0_SPI_IN_197
A53SS0	A53SS0_CNTHPIRQ0_OUT_0	GICSS0_PPI0_0_IN_26
	A53SS0_CNTHPIRQ1_OUT_0	GICSS0_PPI0_1_IN_26
	A53SS0_CNTPNSIRQ0_OUT_0	GICSS0_PPI0_0_IN_30
	A53SS0_CNTPNSIRQ1_OUT_0	GICSS0_PPI0_1_IN_30
	A53SS0_CNTPSIRQ0_OUT_0	GICSS0_PPI0_0_IN_29
	A53SS0_CNTPSIRQ1_OUT_0	GICSS0_PPI0_1_IN_29
	A53SS0_CNTVIRQ0_OUT_0	GICSS0_PPI0_0_IN_27
	A53SS0_CNTVIRQ1_OUT_0	GICSS0_PPI0_1_IN_27
	A53SS0_COMMIRQ0_OUT_0	GICSS0_PPI0_0_IN_22
	A53SS0_COMMIRQ1_OUT_0	GICSS0_PPI0_1_IN_22

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
A53SS0	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_0_IN_24
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_1_IN_31
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_0_IN_31
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_1_IN_24
	A53SS0_ECC_ECCAGGR0_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_24
	A53SS0_ECC_ECCAGGR0_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_94
	A53SS0_ECC_ECCAGGR1_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_25
	A53SS0_ECC_ECCAGGR1_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_93
	A53SS0_ECC_ECCAGGR_COREPAC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_26
	A53SS0_ECC_ECCAGGR_COREPAC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_95
	A53SS0_EXTERRIRQ_OUT_0	ESM0_ESM_LVL_EVENT_IN_144
	A53SS0_INTERRIRQ_OUT_0	ESM0_ESM_LVL_EVENT_IN_145
	A53SS0_PMUIRQ0_OUT_0	GICSS0_PPI0_0_IN_23
	A53SS0_PMUIRQ1_OUT_0	GICSS0_PPI0_1_IN_23
	A53SS0_VCPUMNTIRQ0_OUT_0	GICSS0_PPI0_0_IN_25
	A53SS0_VCPUMNTIRQ1_OUT_0	GICSS0_PPI0_1_IN_25
COMPUTE_CLUSTER0_PBIST_0	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_229
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_176
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_176
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_176
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_44
DDR16SS0	DDR16SS0_DDRSS_CONTROLLER_OUT_0	GICSS0_SPI_IN_151
	DDR16SS0_DDRSS_CONTROLLER_OUT_0	R5FSS0_CORE0_INTR_IN_151
	DDR16SS0_DDRSS_CONTROLLER_OUT_0	R5FSS0_CORE1_INTR_IN_151
	DDR16SS0_DDRSS_CONTROLLER_OUT_0	R5FSS1_CORE0_INTR_IN_151
	DDR16SS0_DDRSS_CONTROLLER_OUT_0	R5FSS1_CORE1_INTR_IN_151
	DDR16SS0_DDRSS_DRAM_ECC_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_6
	DDR16SS0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_69
	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_205
	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	GICSS0_SPI_IN_172
	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	R5FSS0_CORE0_INTR_IN_181
	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	R5FSS0_CORE1_INTR_IN_181
	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	R5FSS1_CORE0_INTR_IN_181

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DDR16SS0	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	R5FSS1_CORE1_INTR_IN_181
	DDR16SS0_DDRSS_V2A_OTHER_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_110
DEBUGSS0	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	GICSS0_SPI_IN_201
	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_201
	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_201
	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_201
	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_201
	DEBUGSS0_CTM_LEVEL_OUT_0	GICSS0_SPI_IN_202
	DEBUGSS0_CTM_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_202
	DEBUGSS0_CTM_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_202
	DEBUGSS0_CTM_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_202
	DEBUGSS0_CTM_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_202
	DEBUGSS0_DAVDMA_LEVEL_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_28
ECC_AGGR1	ECC_AGGR1_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_2
	ECC_AGGR1_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_66
PSC0	PSC0_PSC_ALLINT_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_238
	PSC0_PSC_ALLINT_OUT_0	GICSS0_SPI_IN_203
	PSC0_PSC_ALLINT_OUT_0	R5FSS0_CORE0_INTR_IN_203
	PSC0_PSC_ALLINT_OUT_0	R5FSS0_CORE1_INTR_IN_203
	PSC0_PSC_ALLINT_OUT_0	R5FSS1_CORE0_INTR_IN_203
	PSC0_PSC_ALLINT_OUT_0	R5FSS1_CORE1_INTR_IN_203
MCU_ECC_AGGR0	MCU_ECC_AGGR0_CORR_LEVEL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_14
	MCU_ECC_AGGR0_UNCORR_LEVEL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_15
MCU_PSC0	MCU_PSC0_PSC_ALLINT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_20
	MCU_PSC0_PSC_ALLINT_OUT_0	DMSC0_CORTEX_M3_0_NVIC_IN_239
ECC_AGGR0	ECC_AGGR0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_1
	ECC_AGGR0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_65
MCU_PRG_MCU_7POKS0	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT0_IN_64
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT1_IN_64
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT2_IN_64
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT0_IN_65
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT1_IN_65
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT2_IN_65

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_PRG_MCU_7POKS0	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT0_IN_66
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT1_IN_66
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT2_IN_66
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT0_IN_67
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT1_IN_67
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT2_IN_67
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT0_IN_68
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT1_IN_68
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT2_IN_68
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_5	MCU_ESM0_ESM_PLS_EVENT0_IN_69
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_5	MCU_ESM0_ESM_PLS_EVENT1_IN_69
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_5	MCU_ESM0_ESM_PLS_EVENT2_IN_69
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_6	MCU_ESM0_ESM_PLS_EVENT0_IN_70
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_6	MCU_ESM0_ESM_PLS_EVENT1_IN_70
	MCU_PRG_MCU_7POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_6	MCU_ESM0_ESM_PLS_EVENT2_IN_70
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT0_IN_71
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT1_IN_71
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT2_IN_71
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT0_IN_72
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT1_IN_72
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT2_IN_72
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT0_IN_73
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT1_IN_73
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT2_IN_73
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT0_IN_74
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT1_IN_74
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT2_IN_74
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT0_IN_75
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT1_IN_75
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT2_IN_75
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_5	MCU_ESM0_ESM_PLS_EVENT0_IN_76
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_5	MCU_ESM0_ESM_PLS_EVENT1_IN_76
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_5	MCU_ESM0_ESM_PLS_EVENT2_IN_76

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_PRG_MCU_7POKS0	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_6	MCU_ESM0_ESM_PLS_EVENT0_IN_77
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_6	MCU_ESM0_ESM_PLS_EVENT1_IN_77
	MCU_PRG_MCU_7POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_6	MCU_ESM0_ESM_PLS_EVENT2_IN_77
MCU_PRG_MCU0	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT0_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT1_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	MCU_ESM0_ESM_PLS_EVENT2_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT0_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT1_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	MCU_ESM0_ESM_PLS_EVENT2_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT0_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT1_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	MCU_ESM0_ESM_PLS_EVENT2_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT0_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT1_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	MCU_ESM0_ESM_PLS_EVENT2_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT0_IN_82
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT1_IN_82
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	MCU_ESM0_ESM_PLS_EVENT2_IN_82
MCU_TIMEOUT0	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_21
	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0	MCU_ESM0_ESM_LVL_EVENT_IN_27
MCSPI0	MCSPI0_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_0_RX_IN_0
	MCSPI0_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_0_RX_IN_1
	MCSPI0_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_0_RX_IN_2
	MCSPI0_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_0_RX_IN_3
	MCSPI0_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_0_TX_IN_0
	MCSPI0_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_0_TX_IN_1
	MCSPI0_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_0_TX_IN_2
	MCSPI0_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_0_TX_IN_3
	MCSPI0_INTR_SPI_OUT_0	GICSS0_SPI_IN_204
	MCSPI0_INTR_SPI_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_57
	MCSPI0_INTR_SPI_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_57
	MCSPI0_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_204
	MCSPI0_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_204

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCSPI0	MCSPI0_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_204
	MCSPI0_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_204
MCSPI1	MCSPI1_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_1_RX_IN_0
	MCSPI1_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_1_RX_IN_1
	MCSPI1_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_1_RX_IN_2
	MCSPI1_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_1_RX_IN_3
	MCSPI1_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_1_TX_IN_0
	MCSPI1_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_1_TX_IN_1
	MCSPI1_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_1_TX_IN_2
	MCSPI1_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_1_TX_IN_3
	MCSPI1_INTR_SPI_OUT_0	GICSS0_SPI_IN_205
	MCSPI1_INTR_SPI_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_58
	MCSPI1_INTR_SPI_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_58
	MCSPI1_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_205
MCSPI2	MCSPI2_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_2_RX_IN_0
	MCSPI2_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_2_RX_IN_1
	MCSPI2_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_2_RX_IN_2
	MCSPI2_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_2_RX_IN_3
	MCSPI2_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_2_TX_IN_0
	MCSPI2_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_2_TX_IN_1
	MCSPI2_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_2_TX_IN_2
	MCSPI2_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_2_TX_IN_3
	MCSPI2_INTR_SPI_OUT_0	GICSS0_SPI_IN_206
	MCSPI2_INTR_SPI_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_72
	MCSPI2_INTR_SPI_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_72
	MCSPI2_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_206
MCSPI3	MCSPI3_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_3_RX_IN_0

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCSPI3	MCSPI3_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_3_RX_IN_1
	MCSPI3_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_3_RX_IN_2
	MCSPI3_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_3_RX_IN_3
	MCSPI3_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_3_TX_IN_0
	MCSPI3_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_3_TX_IN_1
	MCSPI3_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_3_TX_IN_2
	MCSPI3_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_3_TX_IN_3
	MCSPI3_INTR_SPI_OUT_0	GICSS0_SPI_IN_141
	MCSPI3_INTR_SPI_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_59
	MCSPI3_INTR_SPI_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_59
	MCSPI3_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_63
	MCSPI3_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_63
	MCSPI3_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_63
	MCSPI3_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_63
MCSPI4	MCSPI4_DMA_READ_EVENT_OUT_0	PDMA1_SPI_MAIN_4_RX_IN_0
	MCSPI4_DMA_READ_EVENT_OUT_1	PDMA1_SPI_MAIN_4_RX_IN_1
	MCSPI4_DMA_READ_EVENT_OUT_2	PDMA1_SPI_MAIN_4_RX_IN_2
	MCSPI4_DMA_READ_EVENT_OUT_3	PDMA1_SPI_MAIN_4_RX_IN_3
	MCSPI4_DMA_WRITE_EVENT_OUT_0	PDMA1_SPI_MAIN_4_TX_IN_0
	MCSPI4_DMA_WRITE_EVENT_OUT_1	PDMA1_SPI_MAIN_4_TX_IN_1
	MCSPI4_DMA_WRITE_EVENT_OUT_2	PDMA1_SPI_MAIN_4_TX_IN_2
	MCSPI4_DMA_WRITE_EVENT_OUT_3	PDMA1_SPI_MAIN_4_TX_IN_3
	MCSPI4_INTR_SPI_OUT_0	GICSS0_SPI_IN_207
	MCSPI4_INTR_SPI_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_60
	MCSPI4_INTR_SPI_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_60
	MCSPI4_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_207
	MCSPI4_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_207
	MCSPI4_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_207
	MCSPI4_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_207
MCU_MCSPI0	MCU_MCSPI0_INTR_SPI_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_22
	MCU_MCSPI0_INTR_SPI_OUT_0	GICSS0_SPI_IN_208
	MCU_MCSPI0_INTR_SPI_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_61
	MCU_MCSPI0_INTR_SPI_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_61

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_MCSPI0	MCU_MCSPI0_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_208
	MCU_MCSPI0_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_208
	MCU_MCSPI0_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_208
	MCU_MCSPI0_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_208
MCU_MCSPI1	MCU_MCSPI1_INTR_SPI_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_23
	MCU_MCSPI1_INTR_SPI_OUT_0	GICSS0_SPI_IN_209
	MCU_MCSPI1_INTR_SPI_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_62
	MCU_MCSPI1_INTR_SPI_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_62
	MCU_MCSPI1_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_209
	MCU_MCSPI1_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_209
	MCU_MCSPI1_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_209
	MCU_MCSPI1_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_209
UART0	UART0_USART_DMA_OUT_0	PDMA0_USART_MAIN_0_TX_IN_0
	UART0_USART_DMA_OUT_1	PDMA0_USART_MAIN_0_RX_IN_0
	UART0_USART_IRQ_OUT_0	GICSS0_SPI_IN_210
	UART0_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_63
	UART0_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_63
	UART0_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_210
	UART0_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_210
	UART0_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_210
	UART0_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_210
UART1	UART1_USART_DMA_OUT_0	PDMA0_USART_MAIN_1_TX_IN_0
	UART1_USART_DMA_OUT_1	PDMA0_USART_MAIN_1_RX_IN_0
	UART1_USART_IRQ_OUT_0	GICSS0_SPI_IN_211
	UART1_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_64
	UART1_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_64
	UART1_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_211
	UART1_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_211
	UART1_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_211
	UART1_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_211
UART2	UART2_USART_DMA_OUT_0	PDMA1_USART_MAIN_2_TX_IN_0
	UART2_USART_DMA_OUT_1	PDMA1_USART_MAIN_2_RX_IN_0
	UART2_USART_IRQ_OUT_0	GICSS0_SPI_IN_212

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
UART2	UART2_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_65
	UART2_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_65
	UART2_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_212
	UART2_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_212
	UART2_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_212
	UART2_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_212
UART3	UART3_USART_DMA_OUT_0	PDMA1_USART_MAIN_3_TX_IN_0
	UART3_USART_DMA_OUT_1	PDMA1_USART_MAIN_3_RX_IN_0
	UART3_USART_IRQ_OUT_0	GICSS0_SPI_IN_213
	UART3_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_66
	UART3_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_66
	UART3_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_213
	UART3_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_213
	UART3_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_213
	UART3_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_213
UART4	UART4_USART_DMA_OUT_0	PDMA1_USART_MAIN_4_TX_IN_0
	UART4_USART_DMA_OUT_1	PDMA1_USART_MAIN_4_RX_IN_0
	UART4_USART_IRQ_OUT_0	GICSS0_SPI_IN_214
	UART4_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_67
	UART4_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_67
	UART4_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_214
	UART4_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_214
	UART4_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_214
	UART4_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_214
UART5	UART5_USART_DMA_OUT_0	PDMA1_USART_MAIN_5_TX_IN_0
	UART5_USART_DMA_OUT_1	PDMA1_USART_MAIN_5_RX_IN_0
	UART5_USART_IRQ_OUT_0	GICSS0_SPI_IN_215
	UART5_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_68
	UART5_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_68
	UART5_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_215
	UART5_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_215
	UART5_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_215
	UART5_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_215

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
UART6	UART6_USART_DMA_OUT_0	PDMA1_USART_MAIN_6_TX_IN_0
	UART6_USART_DMA_OUT_1	PDMA1_USART_MAIN_6_RX_IN_0
	UART6_USART_IRQ_OUT_0	GICSS0_SPI_IN_216
	UART6_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_69
	UART6_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_69
	UART6_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_216
	UART6_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_216
	UART6_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_216
	UART6_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_216
MCU_UART0	MCU_UART0_USART_IRQ_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_24
	MCU_UART0_USART_IRQ_OUT_0	GICSS0_SPI_IN_217
	MCU_UART0_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_70
	MCU_UART0_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_70
	MCU_UART0_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_217
	MCU_UART0_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_217
	MCU_UART0_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_217
	MCU_UART0_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_217
MCU_UART1	MCU_UART1_USART_IRQ_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_25
	MCU_UART1_USART_IRQ_OUT_0	GICSS0_SPI_IN_218
	MCU_UART1_USART_IRQ_OUT_0	PRU_ICSSG0_PR1_SLV_INTR_IN_71
	MCU_UART1_USART_IRQ_OUT_0	PRU_ICSSG1_PR1_SLV_INTR_IN_71
	MCU_UART1_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_218
	MCU_UART1_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_218
	MCU_UART1_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_218
	MCU_UART1_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_218
USB0	USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_35
	USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_111
	USB0_ASF_INT_FATAL_OUT_0	ESM0_ESM_LVL_EVENT_IN_142
	USB0_ASF_INT_NONFATAL_OUT_0	ESM0_ESM_LVL_EVENT_IN_143
	USB0_HOST_SYSTEM_ERROR_OUT_0	GICSS0_SPI_IN_219
	USB0_HOST_SYSTEM_ERROR_OUT_0	R5FSS0_CORE0_INTR_IN_219
	USB0_HOST_SYSTEM_ERROR_OUT_0	R5FSS0_CORE1_INTR_IN_219
	USB0_HOST_SYSTEM_ERROR_OUT_0	R5FSS1_CORE0_INTR_IN_219

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
USB0	USB0_HOST_SYSTEM_ERROR_OUT_0	R5FSS1_CORE1_INTR_IN_219
	USB0_IRQ_OUT_0	GICSS0_SPI_IN_220
	USB0_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_220
	USB0_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_220
	USB0_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_220
	USB0_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_220
	USB0_IRQ_OUT_1	GICSS0_SPI_IN_221
	USB0_IRQ_OUT_1	R5FSS0_CORE0_INTR_IN_221
	USB0_IRQ_OUT_1	R5FSS0_CORE1_INTR_IN_221
	USB0_IRQ_OUT_1	R5FSS1_CORE0_INTR_IN_221
	USB0_IRQ_OUT_1	R5FSS1_CORE1_INTR_IN_221
	USB0_IRQ_OUT_2	GICSS0_SPI_IN_222
	USB0_IRQ_OUT_2	R5FSS0_CORE0_INTR_IN_222
	USB0_IRQ_OUT_2	R5FSS0_CORE1_INTR_IN_222
	USB0_IRQ_OUT_2	R5FSS1_CORE0_INTR_IN_222
	USB0_IRQ_OUT_2	R5FSS1_CORE1_INTR_IN_222
	USB0_IRQ_OUT_3	GICSS0_SPI_IN_223
	USB0_IRQ_OUT_3	R5FSS0_CORE0_INTR_IN_223
	USB0_IRQ_OUT_3	R5FSS0_CORE1_INTR_IN_223
	USB0_IRQ_OUT_3	R5FSS1_CORE0_INTR_IN_223
	USB0_IRQ_OUT_3	R5FSS1_CORE1_INTR_IN_223
	USB0_IRQ_OUT_4	GICSS0_SPI_IN_224
	USB0_IRQ_OUT_4	R5FSS0_CORE0_INTR_IN_224
	USB0_IRQ_OUT_4	R5FSS0_CORE1_INTR_IN_224
	USB0_IRQ_OUT_4	R5FSS1_CORE0_INTR_IN_224
	USB0_IRQ_OUT_4	R5FSS1_CORE1_INTR_IN_224
	USB0_IRQ_OUT_5	GICSS0_SPI_IN_225
	USB0_IRQ_OUT_5	R5FSS0_CORE0_INTR_IN_225
	USB0_IRQ_OUT_5	R5FSS0_CORE1_INTR_IN_225
	USB0_IRQ_OUT_5	R5FSS1_CORE0_INTR_IN_225
	USB0_IRQ_OUT_5	R5FSS1_CORE1_INTR_IN_225
	USB0_IRQ_OUT_6	GICSS0_SPI_IN_226
	USB0_IRQ_OUT_6	R5FSS0_CORE0_INTR_IN_226

Table 9-63. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
USB0	USB0_IRQ_OUT_6	R5FSS0_CORE1_INTR_IN_226
	USB0_IRQ_OUT_6	R5FSS1_CORE0_INTR_IN_226
	USB0_IRQ_OUT_6	R5FSS1_CORE1_INTR_IN_226
	USB0_IRQ_OUT_7	GICSS0_SPI_IN_227
	USB0_IRQ_OUT_7	R5FSS0_CORE0_INTR_IN_227
	USB0_IRQ_OUT_7	R5FSS0_CORE1_INTR_IN_227
	USB0_IRQ_OUT_7	R5FSS1_CORE0_INTR_IN_227
	USB0_IRQ_OUT_7	R5FSS1_CORE1_INTR_IN_227
	USB0_OTGIRQ_OUT_0	GICSS0_SPI_IN_228
	USB0_OTGIRQ_OUT_0	R5FSS0_CORE0_INTR_IN_228
	USB0_OTGIRQ_OUT_0	R5FSS0_CORE1_INTR_IN_228
	USB0_OTGIRQ_OUT_0	R5FSS1_CORE0_INTR_IN_228
	USB0_OTGIRQ_OUT_0	R5FSS1_CORE1_INTR_IN_228
SERDES_10G0	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0	GICSS0_SPI_IN_142
	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_180
	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_180
	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_180
	SERDES_10G0_PHY_PWR_TIMEOUT_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_180

9.5 Time Sync and Compare Interrupt Events

9.5.1 CMPEVT_INTRTR0 Interrupt Map

Table 9-64. CMPEVT_INTRTR0 Interrupt Map

Interrupt Input Line	Interrupt ID	Source Interrupt
CMPEVT_INTRTR0_IN_0	0	PRU_ICSSG0_PR1_HOST_INTR_REQ_0
CMPEVT_INTRTR0_IN_1	1	PRU_ICSSG0_PR1_HOST_INTR_REQ_1
CMPEVT_INTRTR0_IN_2	2	PRU_ICSSG0_PR1_HOST_INTR_REQ_2
CMPEVT_INTRTR0_IN_3	3	PRU_ICSSG0_PR1_HOST_INTR_REQ_3
CMPEVT_INTRTR0_IN_4	4	PRU_ICSSG0_PR1_HOST_INTR_REQ_4
CMPEVT_INTRTR0_IN_5	5	PRU_ICSSG0_PR1_HOST_INTR_REQ_5
CMPEVT_INTRTR0_IN_6	6	PRU_ICSSG0_PR1_HOST_INTR_REQ_6
CMPEVT_INTRTR0_IN_7	7	PRU_ICSSG0_PR1_HOST_INTR_REQ_7
CMPEVT_INTRTR0_IN_8	8	PRU_ICSSG1_PR1_HOST_INTR_REQ_0
CMPEVT_INTRTR0_IN_9	9	PRU_ICSSG1_PR1_HOST_INTR_REQ_1
CMPEVT_INTRTR0_IN_10	10	PRU_ICSSG1_PR1_HOST_INTR_REQ_2
CMPEVT_INTRTR0_IN_11	11	PRU_ICSSG1_PR1_HOST_INTR_REQ_3
CMPEVT_INTRTR0_IN_12	12	PRU_ICSSG1_PR1_HOST_INTR_REQ_4
CMPEVT_INTRTR0_IN_13	13	PRU_ICSSG1_PR1_HOST_INTR_REQ_5
CMPEVT_INTRTR0_IN_14	14	PRU_ICSSG1_PR1_HOST_INTR_REQ_6
CMPEVT_INTRTR0_IN_15	15	PRU_ICSSG1_PR1_HOST_INTR_REQ_7
CMPEVT_INTRTR0_IN_16	16	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_0
CMPEVT_INTRTR0_IN_17	17	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_1
CMPEVT_INTRTR0_IN_18	18	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_2
CMPEVT_INTRTR0_IN_19	19	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_3
CMPEVT_INTRTR0_IN_20	20	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_4
CMPEVT_INTRTR0_IN_21	21	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_5
CMPEVT_INTRTR0_IN_22	22	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_6
CMPEVT_INTRTR0_IN_23	23	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_7
CMPEVT_INTRTR0_IN_24	24	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_8
CMPEVT_INTRTR0_IN_25	25	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_9
CMPEVT_INTRTR0_IN_26	26	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_10
CMPEVT_INTRTR0_IN_27	27	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_11
CMPEVT_INTRTR0_IN_28	28	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_12
CMPEVT_INTRTR0_IN_29	29	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_13
CMPEVT_INTRTR0_IN_30	30	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_14
CMPEVT_INTRTR0_IN_31	31	PRU_ICSSG0_PR1_IEP0_CMP_INTR_REQ_15
CMPEVT_INTRTR0_IN_32	32	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_0
CMPEVT_INTRTR0_IN_33	33	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_1
CMPEVT_INTRTR0_IN_34	34	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_2
CMPEVT_INTRTR0_IN_35	35	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_3
CMPEVT_INTRTR0_IN_36	36	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_4
CMPEVT_INTRTR0_IN_37	37	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_5
CMPEVT_INTRTR0_IN_38	38	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_6
CMPEVT_INTRTR0_IN_39	39	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_7
CMPEVT_INTRTR0_IN_40	40	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_8
CMPEVT_INTRTR0_IN_41	41	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_9

Table 9-64. CMPEVT_INTRTR0 Interrupt Map (continued)

Interrupt Input Line	Interrupt ID	Source Interrupt
CMPEVT_INTRTR0_IN_42	42	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_10
CMPEVT_INTRTR0_IN_43	43	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_11
CMPEVT_INTRTR0_IN_44	44	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_12
CMPEVT_INTRTR0_IN_45	45	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_13
CMPEVT_INTRTR0_IN_46	46	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_14
CMPEVT_INTRTR0_IN_47	47	PRU_ICSSG0_PR1_IEP1_CMP_INTR_REQ_15
CMPEVT_INTRTR0_IN_48	48	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_0
CMPEVT_INTRTR0_IN_49	49	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_1
CMPEVT_INTRTR0_IN_50	50	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_2
CMPEVT_INTRTR0_IN_51	51	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_3
CMPEVT_INTRTR0_IN_52	52	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_4
CMPEVT_INTRTR0_IN_53	53	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_5
CMPEVT_INTRTR0_IN_54	54	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_6
CMPEVT_INTRTR0_IN_55	55	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_7
CMPEVT_INTRTR0_IN_56	56	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_8
CMPEVT_INTRTR0_IN_57	57	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_9
CMPEVT_INTRTR0_IN_58	58	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_10
CMPEVT_INTRTR0_IN_59	59	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_11
CMPEVT_INTRTR0_IN_60	60	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_12
CMPEVT_INTRTR0_IN_61	61	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_13
CMPEVT_INTRTR0_IN_62	62	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_14
CMPEVT_INTRTR0_IN_63	63	PRU_ICSSG1_PR1_IEP0_CMP_INTR_REQ_15
CMPEVT_INTRTR0_IN_64	64	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_0
CMPEVT_INTRTR0_IN_65	65	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_1
CMPEVT_INTRTR0_IN_66	66	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_2
CMPEVT_INTRTR0_IN_67	67	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_3
CMPEVT_INTRTR0_IN_68	68	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_4
CMPEVT_INTRTR0_IN_69	69	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_5
CMPEVT_INTRTR0_IN_70	70	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_6
CMPEVT_INTRTR0_IN_71	71	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_7
CMPEVT_INTRTR0_IN_72	72	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_8
CMPEVT_INTRTR0_IN_73	73	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_9
CMPEVT_INTRTR0_IN_74	74	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_10
CMPEVT_INTRTR0_IN_75	75	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_11
CMPEVT_INTRTR0_IN_76	76	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_12
CMPEVT_INTRTR0_IN_77	77	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_13
CMPEVT_INTRTR0_IN_78	78	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_14
CMPEVT_INTRTR0_IN_79	79	PRU_ICSSG1_PR1_IEP1_CMP_INTR_REQ_15
CMPEVT_INTRTR0_IN_80	80	CPSW0_CPTS_COMP_0
CMPEVT_INTRTR0_IN_81	81	PCIE0_PCIE_CPTS_COMP_0
CMPEVT_INTRTR0_IN_82	82	CPTS0_CPTS_COMP_0

9.5.2 TIMESYNC_INTRTR0 Interrupt Map

Table 9-65. TIMESYNC_INTRTR0 Interrupt Map

Interrupt Input Line	ID	Source Interrupt
TIMESYNC_INTRTR0_IN_0	0	TIMER0_TIMER_PWM_0
TIMESYNC_INTRTR0_IN_1	1	TIMER1_TIMER_PWM_0
TIMESYNC_INTRTR0_IN_2	2	TIMER2_TIMER_PWM_0
TIMESYNC_INTRTR0_IN_3	3	TIMER3_TIMER_PWM_0
TIMESYNC_INTRTR0_IN_4	4	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN0IN_PRG0_IEP0_EDC_LATCH_IN0_0
TIMESYNC_INTRTR0_IN_5	5	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN1IN_PRG0_IEP0_EDC_LATCH_IN1_0
TIMESYNC_INTRTR0_IN_6	6	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN0IN_PRG0_IEP1_EDC_LATCH_IN0_0
TIMESYNC_INTRTR0_IN_7	7	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN1IN_PRG0_IEP1_EDC_LATCH_IN1_0
TIMESYNC_INTRTR0_IN_8	8	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN0IN_PRG1_IEP0_EDC_LATCH_IN0_0
TIMESYNC_INTRTR0_IN_9	9	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN1IN_PRG1_IEP0_EDC_LATCH_IN1_0
TIMESYNC_INTRTR0_IN_10	10	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN0IN_PRG1_IEP1_EDC_LATCH_IN0_0
TIMESYNC_INTRTR0_IN_11	11	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN1IN_PRG1_IEP1_EDC_LATCH_IN1_0
TIMESYNC_INTRTR0_IN_12	12	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_0
TIMESYNC_INTRTR0_IN_13	13	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_0
TIMESYNC_INTRTR0_IN_14	14	PINFUNCTION_CPTS0_HW1TSPUSHIN_CPTS0_HW1TSPUSH_0
TIMESYNC_INTRTR0_IN_15	15	PINFUNCTION_CPTS0_HW2TSPUSHIN_CPTS0_HW2TSPUSH_0
TIMESYNC_INTRTR0_IN_16	16	CPTS0_CPTS_GENF0_0
TIMESYNC_INTRTR0_IN_17	17	CPTS0_CPTS_GENF1_0
TIMESYNC_INTRTR0_IN_18	18	CPTS0_CPTS_GENF2_0
TIMESYNC_INTRTR0_IN_19	19	CPTS0_CPTS_GENF3_0
TIMESYNC_INTRTR0_IN_20	20	CPTS0_CPTS_GENF4_0
TIMESYNC_INTRTR0_IN_21	21	CPSW0_CPTS_GENF0_0
TIMESYNC_INTRTR0_IN_22	22	CPSW0_CPTS_GENF1_0
TIMESYNC_INTRTR0_IN_23	23	PCIE0_PCIE_CPTS_GENF0_0
TIMESYNC_INTRTR0_IN_24	24	CPTS0_CPTS_GENF5_0
TIMESYNC_INTRTR0_IN_25	25	PRU_ICSSG0_PR1_EDC0_SYNC0_OUT_0
TIMESYNC_INTRTR0_IN_26	26	PRU_ICSSG0_PR1_EDC0_SYNC1_OUT_0
TIMESYNC_INTRTR0_IN_27	27	PRU_ICSSG0_PR1_EDC1_SYNC0_OUT_0
TIMESYNC_INTRTR0_IN_28	28	PRU_ICSSG0_PR1_EDC1_SYNC1_OUT_0
TIMESYNC_INTRTR0_IN_29	29	PRU_ICSSG1_PR1_EDC0_SYNC0_OUT_0
TIMESYNC_INTRTR0_IN_30	30	PRU_ICSSG1_PR1_EDC0_SYNC1_OUT_0
TIMESYNC_INTRTR0_IN_31	31	PRU_ICSSG1_PR1_EDC1_SYNC0_OUT_0
TIMESYNC_INTRTR0_IN_32	32	PRU_ICSSG1_PR1_EDC1_SYNC1_OUT_0
TIMESYNC_INTRTR0_IN_33	33	PCIE0_PCIE_CPTS_SYNC_0
TIMESYNC_INTRTR0_IN_34	34	CPSW0_CPTS_SYNC_0
TIMESYNC_INTRTR0_IN_35	35	CPTS0_CPTS_SYNC_0
TIMESYNC_INTRTR0_IN_36	36	GTC0_GTC_PUSH_EVENT_0
TIMESYNC_INTRTR0_IN_37	37	PCIE0_PCIE_CPTS_HW1_PUSH_0
TIMESYNC_INTRTR0_IN_38	38	PCIE0_PCIE_PTM_VALID_PULSE_0
TIMESYNC_INTRTR0_IN_39	39	EPWM0_EPWM_SYNCO_O_0
TIMESYNC_INTRTR0_IN_40	40	EPWM3_EPWM_SYNCO_O_0
TIMESYNC_INTRTR0_IN_41	41	EPWM6_EPWM_SYNCO_O_0

Chapter 10

Time Sync

This chapter describes the time sync modules in the device.

10.1 Time Sync Module (CPTS)

This chapter describes the Time Synchronization (CPTS) module.

10.1.1 CPTS Overview

The Common Platform Time Sync (CPTS) module is used to facilitate host control of time sync operations.

Table 10-1. CPTS Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
CPTS0	-	✓
PCIE0_CPTS0	-	✓ (PCIE0)
CPSW0_CPTS0	-	✓ (CPSW0)

Figure 10-1 shows an overview of the CPTS0 module.

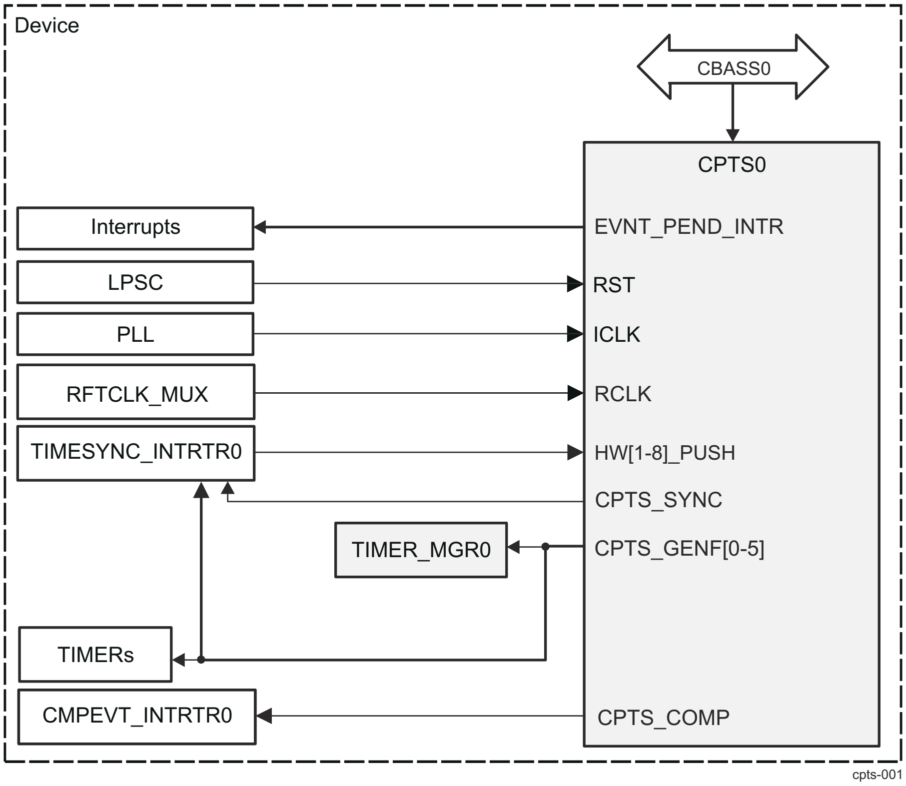

Figure 10-1. CPTS0 Overview

10.1.1.1 CPTS Features

Main features of CPTS module are:

- Supports the selection of multiple external clock sources
- Software control of time sync events via interrupt or polling
- Supports 8 hardware timestamp push inputs
- Supports timestamp counter compare output (CPTS_COMP)
- Supports timestamp counter bit output (CPTS_SYNC)
- Supports 6 timestamp Generator function outputs (CPTS_GENF0 to CPTS_GENF5)
- 32-bit and 64-bit timestamp modes.

10.1.1.2 CPTS Not Supported Features

The following features are not supported by the module:

- Oscillator adjustment by module

- Ethernet transmit or receive ports

10.1.2 CPTS Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Note

This section describes the CPTS in the MAIN domain

For CPTS in PCIe integration, see Section 12.2.2.4.9 , *PCIe Subsystem Precision Time Measurement (PTM)* in Section 12.2.2 , *Peripheral Component Interconnect Express (PCIe) Subsystem*.

For CPTS in CPSW integration, refer to Section 12.2.1.3 in Section 12.2.1 , *Gigabit Ethernet Switch (CPSW0)*.

Figure 10-2 shows the CPTS0 integration.

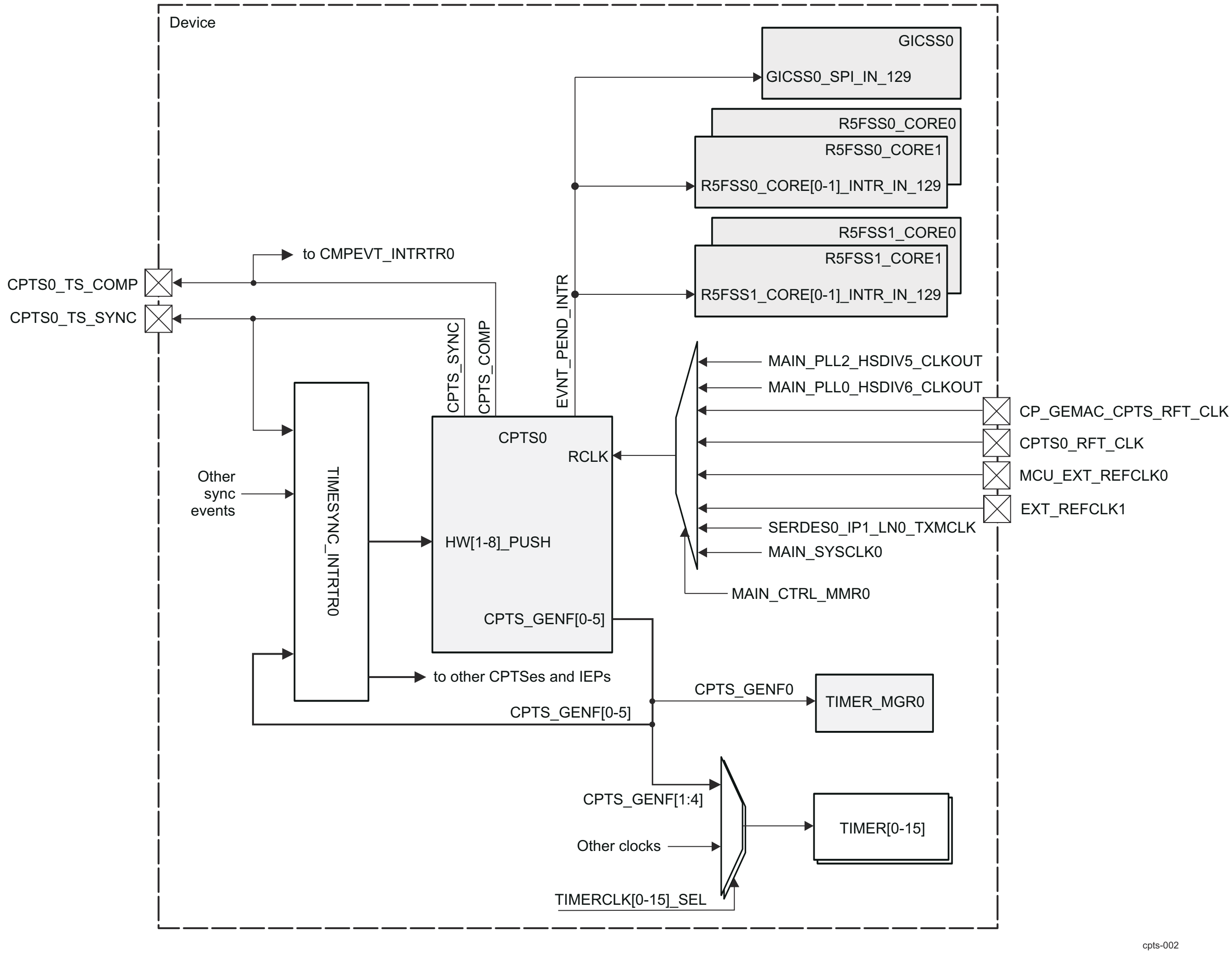

Figure 10-2. CPTS0 Integration

Table 10-2 and Table 10-3 summarize the integration of the module in the device.

Table 10-2. CPTS0 Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect

Table 10-2. CPTS0 Integration Attributes (continued)

CPTS0	PSC0	GP	LPSC0	CBASS0

Table 10-3. CPTS0 Clocks and Resets

Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
CPTS0	CPTS0_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	CPTS0 interface clock
	CPTS0_RCLK	MAIN_PLL2_HSDIV5_CLKOUT	MAIN_PLL2	CPTS0 reference clock. Selectable in CTRL_MMR CTRLMMR_CPTS_CLKSEL register. The recommended RCLK frequency is greater than or equal to VBUS clock frequency.
		MAIN_PLL0_HSDIV6_CLKOUT	MAIN_PLL0	
		CP_GEMAC_CPTS_RFT_CLK	Pin	
		CPTS0_RFT_CLK	Pin	
		MCU_EXT_REFCLK0	Pin	
		EXT_REFCLK1	Pin	
		SERDES0_IP1_LN0_TXMCLK[1]	SERDES0	
		MAIN_SYSCLK0	PLLCTRL0	

Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
CPTS0	CPTS0_RST	MODSS_RST	LPSC0	CPTS0 hardware reset

(1) IP1 in SERDES clock names corresponds to PCIe.

Table 10-4. CPTS0 Hardware Requests

Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CPTS0	CPTS0_EVNT_PEND_INTR	GICSS0_SPI_IN_129	GICSS0	Event pending interrupt	Level
		R5FSS0_CORE0_INTR_IN_129	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_129	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_129	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_129	R5FSS1_CORE1		

DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Description	Type
CPTS0	-	-	-	No PDMA channels to external DMA engines	-

Time Sync Event Inputs

Module Instance	Module Sync Input	Sync Source Signal	Source	Description	Type
CPTS0	CPTS0_HW1_PUSH	TIMESYNC_INTRTR0_OUTL_16	TIMESYNC_INTRTR0	Asynchronous hardware timestamp 1 push input	Level
	CPTS0_HW2_PUSH	TIMESYNC_INTRTR0_OUTL_17	TIMESYNC_INTRTR0	Asynchronous hardware timestamp 2 push input	Level
	CPTS0_HW3_PUSH	TIMESYNC_INTRTR0_OUTL_18	TIMESYNC_INTRTR0	Asynchronous hardware timestamp 3 push input	Level

Table 10-4. CPTS0 Hardware Requests (continued)

	CPTS0_HW4_PUSH	TIMESYNC_INTRTR0_OUTL_19	TIMESYNC_INTRTR0	Asynchronous hardware timestamp 4 push input	Level
	CPTS0_HW5_PUSH	TIMESYNC_INTRTR0_OUTL_20	TIMESYNC_INTRTR0	Asynchronous hardware timestamp 5 push input	Level
	CPTS0_HW6_PUSH	TIMESYNC_INTRTR0_OUTL_21	TIMESYNC_INTRTR0	Asynchronous hardware timestamp 6 push input	Level
	CPTS0_HW7_PUSH	TIMESYNC_INTRTR0_OUTL_22	TIMESYNC_INTRTR0	Asynchronous hardware timestamp 7 push input	Level
	CPTS0_HW8_PUSH	TIMESYNC_INTRTR0_OUTL_23	TIMESYNC_INTRTR0	Asynchronous hardware timestamp 8 push input	Level
Time Sync Event Outputs					
Module Instance	**Module Sync Output**	**Destination Sync Input**	**Destination**	**Description**	**Type**
CPTS0	CPTS0_CPTS_GENF0_0	TIMESYNC_INTRTR0_IN_16	TIMESYNC_INTRTR0	Generation Function Output 0	Edge
		EON_TICK_EVT	TIMER_MGR0		
	CPTS0_CPTS_GENF1_0	TIMESYNC_INTRTR0_IN_17	TIMESYNC_INTRTR0	Generation Function Output 1	Edge
			TIMERCLK[0:15] MUX		
	CPTS0_CPTS_GENF2_0	TIMESYNC_INTRTR0_IN_18	TIMESYNC_INTRTR0	Generation Function Output 2	Edge
			TIMERCLK[0:15] MUX		
	CPTS0_CPTS_GENF3_0	TIMESYNC_INTRTR0_IN_19	TIMESYNC_INTRTR0	Generation Function Output 3	Edge
			TIMERCLK[0:15] MUX		
	CPTS0_CPTS_GENF4_0	TIMESYNC_INTRTR0_IN_20	TIMESYNC_INTRTR0	Generation Function Output 4	Edge
			TIMERCLK[0:15] MUX		
	CPTS0_CPTS_GENF5_0	TIMESYNC_INTRTR0_IN_24	TIMESYNC_INTRTR0	Generation Function Output 5	Edge
	CPTS0_CPTS_SYNC_0	TIMESYNC_INTRTR0_IN_35	TIMESYNC_INTRTR0	Sync Output	Edge
		CPTS0_CPTS_SYNC_0	Pin		
Compare Event Outputs					
Module Instance	**Module Comp Output**	**Destination Comp Input**	**Destination**	**Description**	**Type**
CPTS0	CPTS0_CPTS_COMP_0	CMPEVT_INTRTR0_IN_82	CMPEVT_INTRTR0	Comparison Output	Edge
		CPTS0_CPTS_COMP_0	Pin		

Note

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset, and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the time sync and compare events routers, see Section 10.3 , *Time Sync and Compare Events*.

10.1.3 CPTS Functional Description

10.1.3.1 CPTS Architecture

Figure 10-3 shows the architecture of the CPTS module.

The CPTS module is used to facilitate host control of time sync operations. The CPTS collects time sync events and then presents them to the host for processing. The types of time sync events are as follows:

- Host Transmit Event (CPSW CPTS)
- Ethernet receive event (CPSW CPTS)
- Ethernet transmit event (CPSW CPTS)
- Time stamp push event
- Time stamp counter rollover event (32-bit mode only)
- Time stamp counter half-rollover event (32-bit mode only)
- Hardware Time Stamp Push Event
- Time Stamp Compare Event

The reference clock used for the time stamp (RCLK) can be derived from several sources.

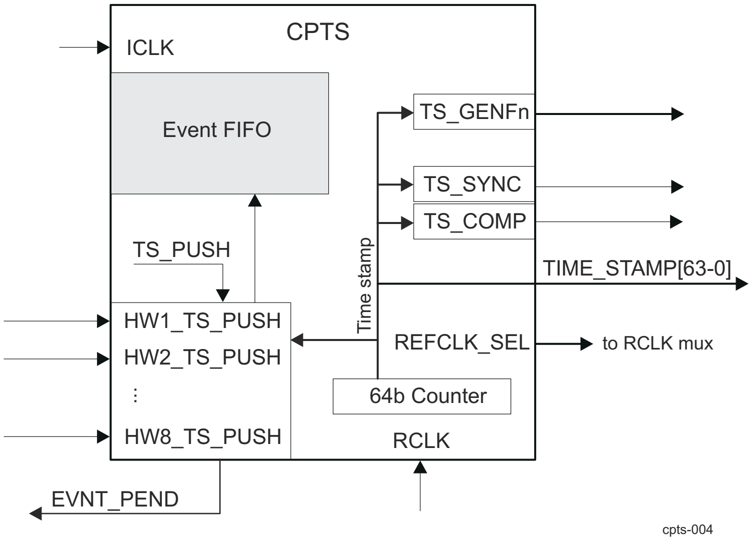

Figure 10-3. CPTS Block Diagram

Note

This section describes the CPTS in the main domain. For CPTS in PCIe integration, please see *PCIe Subsystem Precision Time Measurement (PTM)* in *Peripheral Component Interconnect Express (PCIe) Subsystem*.

For CPTS in CPSW integration, please refer to *CPSW0 Integration* in *Gigabit Ethernet Switch (CPSW)*.

10.1.3.2 CPTS Initialization

The CPTS module must be configured as follows:

1. Reset the CPTS module
2. Clear the CPTS_EN bit in the CPTS_CONTROL_REG
3. Write the RFTCLK_SEL value in the CPTS_RFTCLK_SEL_REG with the desired reference clock selection
4. Set the CPTS_EN bit in the CPTS_CONTROL_REG
5. If using interrupts and not polling, enable the interrupt by setting the TS_PEND_EN bit in the CPTS_INT_ENABLE_REG

10.1.3.3 32-bit Time Stamp Value

The time stamp value is a 32-bit value that increments on each RCLK rising edge when CPTS_EN is set to 1. When CPTS_EN is cleared to 0, the time stamp value is reset to 0.

If more than 32-bits of time stamp are required by the application, the host software must maintain the necessary number of upper bits. The upper time stamp value should be incremented by the host when the rollover event is detected.

For test purposes, the time stamp can be written via the time stamp load function (CPTS_TS_LOAD_VAL_REG and CPTS_TS_LOAD_EN_REG).

The TS_INC_VAL[2:0] value must be zero in 32-bit mode. Nudge and PPM adjustments are not supported in 32-bit mode.

10.1.3.4 64-bit Time Stamp Value

The time stamp value is a 64-bit value that increments on each RCLK rising edge when CPTS_EN is set to 1. When CPTS_EN is cleared to 0, the time stamp value is reset to 0.

64-bit mode is selected via CPTS_CONTROL_REG[5] MODE_64BIT bit set to 1.

For test purposes, the time stamp can be written via the time stamp load function (CPTS_TS_LOAD_VAL_REG, CPTS_TS_LOAD_HIGH_VAL_REG, and CPTS_TS_LOAD_EN_REG).

The TS_ADD_VAL feature is included to allow 1-ns timestamp operations with an RCLK rate less than 1 GHz. Table 10-5 shows the RCLK and TS_ADD_VAL values for 1-ns operations. The highest RCLK frequency possible should be used as allowed by the silicon technology.

Table 10-5. TS_ADD_VAL

RCLK (MHz)	TS_ADD_VAL
1000	0
500	1
333.33	2
250	3
200	4
166.66	5
142.85714	6
125	7

10.1.3.4.1 64-Bit Timestamp Nudge

The 64-bit TIME_STAMP value can be adjusted by writing the CPTS_TS_NUDGE_VAL_REG[7:0] register value which is a two's complement value. A value of 0xFF will subtract one RCLK clock from the next incremented TIME_STAMP[63:0] value. A nudge value of 0x01 will add one RCLK clock to the next incremented TIME_STAMP[63:0] value. For example, if the current TIME_STAMP value is 0x0F06, and TS_ADD_VAL[2:0]=3, the next incremented timestamp value would be 0x0F0A without a nudge and 0x0F0A +/- TS_NUDGE[7:0] with a nudge. The TS_NUDGE value is cleared to zero when the nudge has occurred.

10.1.3.4.2 64-bit Timestamp PPM

The 64-bit TIME_STAMP can be adjusted by parts per million (PPM) or by parts per hour (PPH). Writing a non-zero value to the TS_PPM[41:0] value enables PPM operations. The adjustment is up or down depending on the TS_PPM_DIR bit. The TIME_STAMP value is increased by the PPM value when TS_PPM_DIR is cleared and decreased by the PPM value when TS_PPM_DIR is set.

- To adjust for 100 parts per million the configured value for TS_PPM[41:0] is:
  1 000 000/100 = 10 000 (DEC)
- To adjust for 1 part per hour at 1 GHz RCLK, the configured value for TS_PPM[41:0] is:
  (1 000 000 000Hz/1pph) × (3600 seconds/hour) = 346 30B8 A000 (HEX)

10.1.3.5 Event FIFO

All time sync events are push onto the Event FIFO. No overrun indication supported. Software must service the event FIFO in a timely manner to prevent FIFO overrun.

10.1.3.6 Timestamp Compare Output

CPTS features one Time Stamp Compare (TS_COMP) output.

Note

64-bit mode operation is identical to 32-bit mode except that all 64 bits of the TIME_STAMP[63-0] are used instead of only the lower 32 bits.

10.1.3.6.1 Non-Toggle Mode

The TS_COMP output is asserted for CPTS_TS_COMP_LEN_REG[31-0] RCLK periods when the TIME_STAMP[31-0] value compares with the CPTS_TS_COMP_VAL_REG[31-0] and the length value is non-zero. The TS_COMP rising edge occurs three RCLK periods after the values compare. A timestamp compare event is pushed into the event FIFO when TS_COMP is asserted. The polarity of the TS_COMP output is determined by the CPTS_CONTROL_REG[2] TS_POLARITY bit. The output is asserted low when the polarity bit is 0.

10.1.3.6.2 Toggle Mode

The TS_COMP output is asserted for CPTS_TS_COMP_LEN_REG RCLK periods when the TIME_STAMP[31-0] value compares with the CPTS_TS_COMP_VAL_REG[31-0] and the length value is non-zero. The TS_COMP toggles thereafter on CPTS_TS_COMP_LEN_REG[31-0] RCLK periods. The length high or low can be adjusted by writing the CPTS_TS_COMP_NUDGE_REG[7-0] register value which is a two's complement value. A value of 0xFF will subtract one RCLK from the CPTS_TS_COMP_LEN_REG value. A value of 0x01 will add one RCLK to the CPTS_TS_COMP_LEN_REG value. Only a single high or low time is adjusted (nudged) and the CPTS_TS_COMP_NUDGE_REG value is cleared to zero when the nudge has occurred. The TS_COMP output is asserted low when the CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit is 0.

No compare events and no CPTS_EVNT interrupts are generated in toggle mode.

The CPTS_CONTROL_REG[6] TS_COMP_TOG bit must be set for toggle mode, and must be set before writing a non-zero value to CPTS_TS_COMP_LEN_REG.

10.1.3.7 Timestamp Sync Output

The TS_SYNC output is a selected bit of the TIME_STAMP counter value. One of the counter bits 17-31 can be selected in CPTS_CONTROL_REG[31-28] TS_SYNC_SEL. The TS_SYNC output is disabled when CPTS_CONTROL_REG[31-28] TS_SYNC_SEL is zero.

If the selected counter bit is 1 at the time when TS_SYNC_SEL value is written then a rising edge will not occur on the TS_SYNC output. A rising edge will occur on the TS_SYNC output upon the next transition-to-1 of the selected counter bit. The TS_SYNC_SEL value must be written to zero before changing to a different non-zero value. No events are generated due to the TS_SYNC operation. The TS_SYNC output is two RCLK periods after the actual count value.

10.1.3.8 Timestamp GENF Output

There are six TS Generate Function (TS_GENFn) outputs (n = 0 to 5). The TS_GENFn outputs have a programmable cycle (frequency) with a PPM feature and a software nudge feature. The TS_GENFn output cycle is CPTS_LENGTH_REG_j[31:0] RCLK periods (which is different than TS_COMP operation).

The TS_GENFn output cycle is CPTS_LENGTH_REG_j[31:0] RCLK periods beginning when the TIME_STAMP[63:0] value compares with the CPTS_COMP_LOW_REG_j[63:0] and the length value is non-zero. The TS_GENFn output cycle repeats thereafter every CPTS_LENGTH_REG_j[31:0] RCLK periods. The upper 32-bit word should be written first for 64-bit values. The length should be zero while the comparison value and other configuration parameters are being configured. The length should be written non-zero to enable operations last. The first cycle after comparison is active high when the TS_GENFn_POLARITY bit is low. No compare events and no CPTS_EVNT interrupts are generated.

10.1.3.8.1 GENFn Nudge

The cycle length can be adjusted by writing the CPTS_NUDGE_REG_j[7:0] register value which is a two's complement value. A value of 0xFF will subtract one RCLK clock from the CPTS_LENGTH_REG_j[31:0] value. A value of 0x01 will add one RCLK clock to the CPTS_LENGTH_REG_j value. The CPTS_NUDGE_REG_j value is cleared to zero when the nudge has occurred.

10.1.3.8.2 GENFn PPM

The TS_GENFn output cycle can be adjusted by parts per million (PPM) or by parts per hour (PPH). Writing a non-zero CPTS_PPM_LOW_REG_j/CPTS_PPM_HIGH_REG_j value enables PPM operations. The PPM counter continually loads and decrements to zero and then loads again. A single RCLK adjustment is made when the PPM counter decrements to zero. The adjustment is up or down depending on the CPTS_CONTROL_REG_j[0] PPM_DIR bit. When PPM_DIR is set a single RCLK time is subtracted from the generate function counter which has the effect of increasing the generate function frequency by the PPM amount. When PPM_DIR is clear a single RCLK time is added to the generate function counter which has the effect of decreasing the generate function frequency by the PPM amount.

- To adjust for 100 parts per million the configured value for TS_GENFn_PPM[41:0] is:
  1 000 000/100 = 10 000 (DEC)
- To adjust for 1 part per hour at 1 GHz RCLK the configured value for TS_GENFn_PPM[41:0] is:
  (1 000 000 000Hz/1pph) × (3600 seconds/hour) = 346 30B8 A000 (HEX)

10.1.3.9 Time Sync Events

Time Sync events are 96-bit or 128-bit (for 32-bit and 64-bit time stamp respectively) values that are pushed onto the event FIFO and read by software in 32-bit reads. Four 32-bit registers, CPTS_EVENT_0_REG throught CPTS_EVENT_3_REG hold the data of a time sync event.

10.1.3.9.1 Time Stamp Push Event

Software can obtain the current time stamp value (at the time of the write) by initiating a time stamp push event. The push event is initiated by setting the TS_PUSH bit of the CPTS_TS_PUSH_REG. The time stamp value is returned in the event, along with a time stamp push event code.

10.1.3.9.2 Time Stamp Counter Rollover Event (32-bit mode only)

The CPTS module contains a 32-bit time stamp value. The counter upper bits are maintained by host software. The rollover event indicates to software that the time stamp counter has rolled over from 0xFFFF FFFF to 0x0000 0000 and the software-maintained upper count value should be incremented.

10.1.3.9.3 Time Stamp Counter Half-rollover Event (32-bit mode only)

The CPTS includes a time stamp counter half-rollover event. The half-rollover event indicates to software that the time stamp value has incremented from 0x7FFF FFFF to 0x8000 0000. The half-rollover event is included to enable software to correct a misaligned event condition. The half-rollover event is included to enable software to determine the correct time for each event that contains a valid time stamp value, such as an Ethernet event. If an Ethernet event occurs around a counter rollover (full rollover), the rollover event could possibly be loaded into the event FIFO before the Ethernet event, even though the Ethernet event time was actually taken before the rollover. Figure 10-4 shows a misalignment condition.

Host software must detect and correct for misaligned event conditions. For every event after a rollover and before a half-rollover, software must examine the time stamp most significant bit. If bit 31 of the time stamp value is low (0x0000 0000 through 0x7FFF FFFF), then the event time stamp was taken after the rollover and no correction is required. If the value is high (0x8000 0000 through 0xFFFF FFFF), the time stamp value was taken before the rollover and a misalignment is detected. The misaligned case indicates to software that it must subtract one from the upper count value stored in software to calculate the correct time for the misaligned event.

The misaligned event occurs only on the rollover boundary and not on the half-rollover boundary. Software only needs to check for misalignment from a rollover event to a half-rollover event.

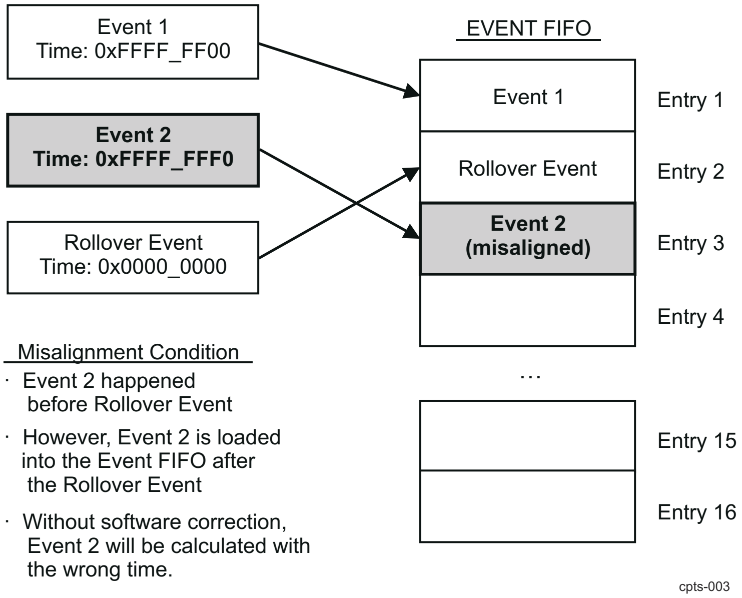

Figure 10-4. Event FIFO Misalignment Condition

10.1.3.9.4 Hardware Time Stamp Push Event

There are eight hardware time stamp inputs (HW[1-8]_TS_PUSH) that can cause hardware time stamp push events to be loaded into the Event FIFO. Each time stamp input is mapped in the device as shown in *CPTS Integration*.

The event is loaded into the event FIFO on the rising edge of the timer, and the PORT_NUMBER field in the CPTS_EVENT_1_REG register indicates the hardware time stamp input that caused the event.

Each hardware time stamp input must be asserted for at least 10 periods of the selected RCLK clock. Each input can be enabled or disabled by setting the respective bits in the CPTS_CONTROL_REG register.

Hardware time stamps are intended to be an extremely low frequency signals, such that the event FIFO does not overrun. Software must keep up with the event FIFO and ensure that there is no overrun, or events will be lost.

10.1.3.10 Timestamp Compare Event

Note

Timestamp compare events are generated for non-toggle mode only.

The CPTS can generate an event for a time stamp comparison in 32-bit or 64-bit mode. The TS_COMP output is also asserted when the event is generated. The event is generated when the TIME_STAMP value compares with the CPTS_TS_COMP_VAL_REG/CPTS_TS_COMP_HIGH_VAL_REG and the CPTS_TS_COMP_LEN_REG value is non-zero. The CPTS_TS_COMP_LEN_REG value should be written by software after the CPTS_TS_COMP_VAL_REG/CPTS_TS_COMP_HIGH_VAL_REG is written and should be zero when the comparison value is written.

10.1.3.11 CPTS Interrupt Handling

When an event is push onto the Event FIFO, an interrupt can be generated to indicate to software that a time sync event occurred. The following steps should be taken to process time sync events using interrupts:

1. Enable the TS_PEND interrupt by setting the TS_PEND_EN bit of the CPTS_INT_ENABLE_REG.
2. Upon interrupt, read the CPTS_EVENT_0_REG through CPTS_EVENT_3_REG register values.

3. Set the CPTS_EVENT_POP_REG[0] EVENT_POP bit to 1 to pop the previously read value off of the event FIFO.
4. Process the interrupt as required by the application software.

Software has the option of processing more than a single event from the event FIFO in the interrupt service routine in the following way:

1. Enable the TS_PEND interrupt by setting the TS_PEND_EN bit of the CPTS_INT_ENABLE_REG.
2. Upon interrupt, read the CPTS_EVENT_0_REG through CPTS_EVENT_3_REG register values.
3. Set the CPTS_EVENT_POP_REG[0] bit to 1 to pop the previously read value off of the event FIFO.
4. Wait for an amount of time greater than four RCLK periods plus four ICLK periods.
5. Read the TS_PEND_RAW bit in the CPTS_INTSTAT_RAW_REG register to determine if another valid event is in the event FIFO. If it is asserted, go to step 2; otherwise, proceed to step 6.
6. Process the interrupt(s) as required by the application software.

Software also has the option of disabling the interrupt and polling the TS_PEND_RAW bit of the CPTS_INTSTAT_RAW_REG to determine if a valid event is on the event FIFO.

10.2 Timer Manager

This chapter describes the Timer Manager module of the device.

10.2.1 Timer Manager Overview

The Timer Manager module provides timers for timing operations for the processes running on multiple processors in the device. The device support one instance of Timer Manager.

Table 10-6. TIMER_MGR Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
TIMER_MGR0	-	✓

Figure 10-5 shows an overview of the Timer Manager module.

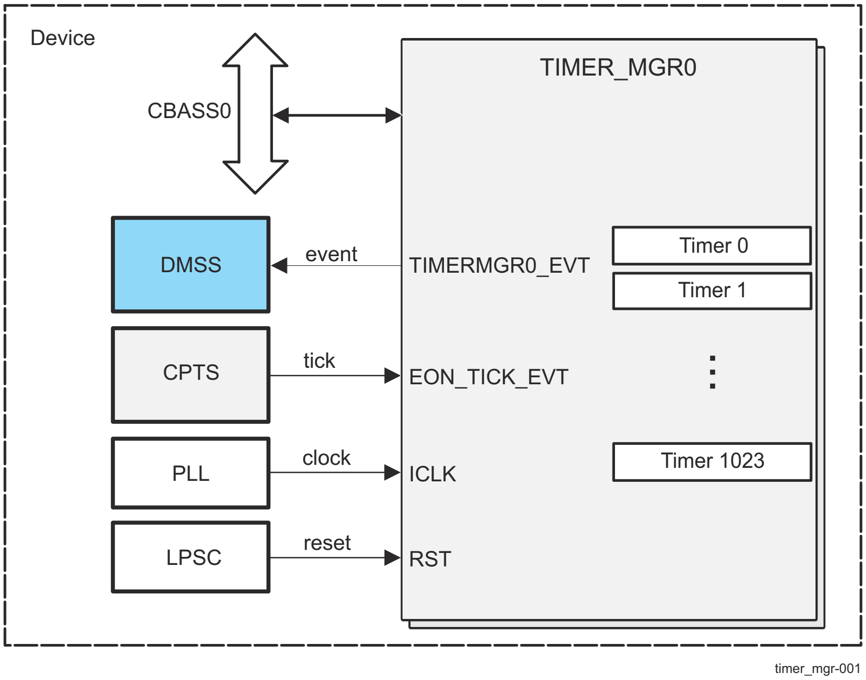

Figure 10-5. Timer Manager Overview

10.2.1.1 Timer Manager Features

Timer Manager has the following features:

- 1024 × 32-bit RAM-based independent timers (1024 in total for the one Timer Manager)
- Events are triggered when a timer expires or when an expired timer is reset or deactivated
- Host access to determine which timer(s) expired
- 32 registers with individual timeout status (one bit per timer)
- A pair of quick-read registers with the number of timers that have expired and the ids of the first timers to expire
- A bank timeout register with the banks that have expired timers – to avoid having to read all timeout status registers when only a few timers have expired
- Groups of 16 timers separated into pages of 4-K address space
- Timer bits within each page to read expiration status for each timer when software only has access to that page
- 10 µs time to cycle through all of the timers
- Host access to reset individual timers
  - Reset values are preprogramed for each timer
  - Timers may all be programmed before the timer manager is enabled, or programmed after enabled.

10.2.1.2 Timer Manager Not Supported Features

The following features are not supported by the module:

- Tunable GENF CPTS output is an input to this module. The timer bank doesn't manage the divider or the rate/offset compensation. It takes the output of a tuner module as a single input EON_TICK event.

10.2.2 Timer Manager Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 10-6 shows the Timer Manager integration.

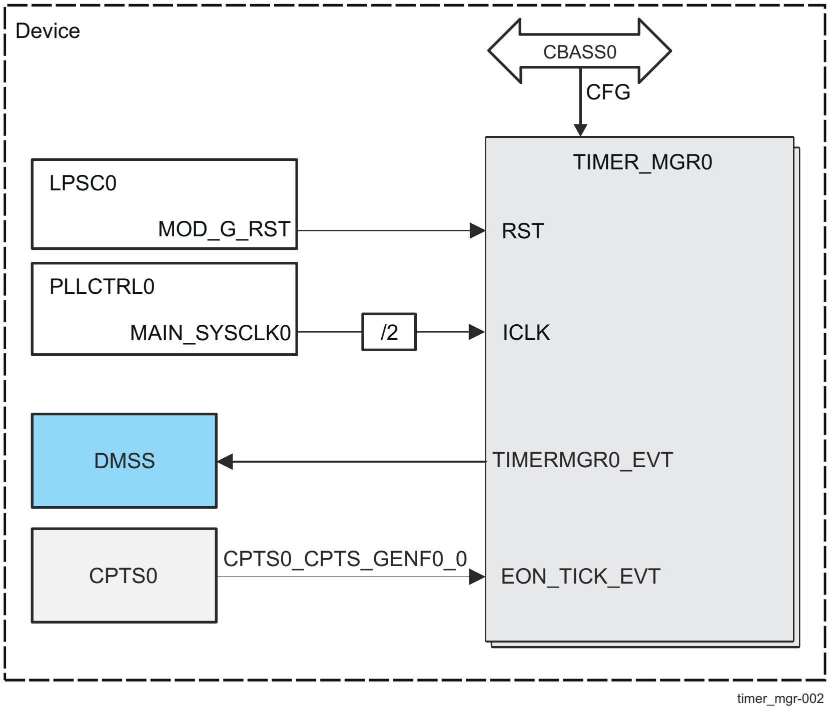

Figure 10-6. Timer Manager Integration

Table 10-7 and Table 10-8 summarize the integration of the module in the device.

Table 10-7. Timer Manager Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
TIMER_MGR0	PSC0	GP	LPSC0	CBASS0

Table 10-8. Timer Manager Clocks and Resets

Clocks				
Module Instance	Module Clock Input	Source Clock Signal	Source	Description
TIMER_MGR0	TIMER_MGR0_ICLK	MAIN_SYSCLK0/2	PLLCTRL0	Timer Manager0 interface clock
	EON_TICK_EVT	CPTS0_CPTS_GENF0_0	CPTS0	Timer Manager0 asynchronous tick event
Resets				
Module Instance	Module Reset Input	Source Reset Signal	Source	Description
TIMER_MGR0	TIMER_MGR0_RST	MODSS_RST	LPSC0	Timer Manager0 hardware reset

Table 10-9. Timer Manager Hardware Requests

Interrupt Requests					
Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER_MGR0	TIMERMGR0_EVT	DMSS EVENT	DMSS	Timer expiration events ×1024	ETL
DMA Events					

Table 10-9. Timer Manager Hardware Requests (continued)

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Description	Type
TIMER_MGR0	-	-	-	No PDMA channels to external DMA engines	-

10.2.3 Timer Manager Functional Description

10.2.3.1 Timer Manager Function Overview

Figure 10-7 shows the Timer Manager diagram.

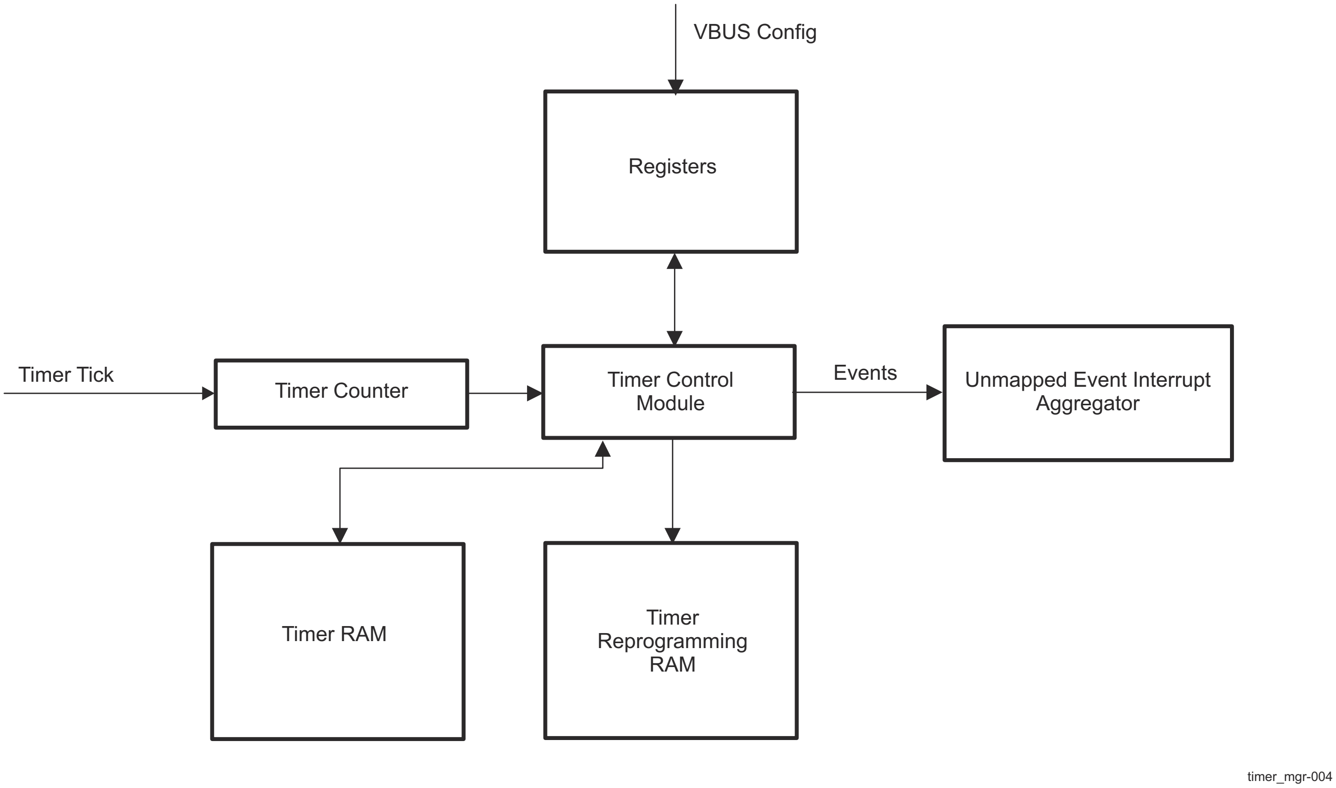

Figure 10-7. Timer Manager Block Diagram

The 1024 timers in the timer manager are organized as the Timer RAM in Figure 10-7. When the timer manager is enabled, the timer counter will increment with the input timer tick, and the control module continuously loops over the Timer RAM, comparing the values against this timer count. When the timer count is greater than a timer value, the timer control module will generate a timer expiration event.

Based on software writes, the timer control module will update the values in the Timer RAM to setup or cancel active timers. Whenever a new value is written to a TIMERMGR_SETUP_j_k memory address, the corresponding timer is touched/setup with the current sum of the timer count and the written value; written values are relative to the current timer count. These values are stored in the Timer Reprogramming RAM, so the software may also write to the TIMERMGR_CONTROL_j_k registers to flag a timer for reprogramming, using the previously stored reprogramming value. The latter method is preferred when the timer setup value is not changing, as it does not interrupt the RAM state machine.

10.2.3.2 Timer Counter

The Timer Manager takes an input timer tick to control the timer rate. All timers share a time base. On each rising edge of this tick event, the timer counter increments. The value of the timer counter may be read by software via the TIMERMGR_COUNTER register.

10.2.3.2.1 Timer Counter Rollover

A rollover bit is maintained for each timer, such that when reprogrammed, it is the carry bit from the sum of the current time (counter) and the relative reprogramming value for that timer. This has the effect that any timer whose rollover bit is currently set to a 1 will not expire in the current epoch.

When the counter transitions from 0xFFFF FFFF to 0x0000 0000, the timer control module changes the rollover bit for all timers from a 1 to a 0. All timers that previously did not have the rollover bit set, will expire when they are next visited by the state machine, as their timeout value was for the previous epoch.

The overall effect is that the timers continue to expire as expected, regardless of when the counter rollover occurs relative to the state machine.

10.2.3.3 Timer Control Module (FSM)

The timer control module controls the RAM accesses for reading and writing. It controls the loops over the timer RAM, checks the values in the RAM to observe expiring timers, flagging timeouts so that events may be triggered and reported. It also takes as input any software-written updates to setup, clear, and touch the timers.

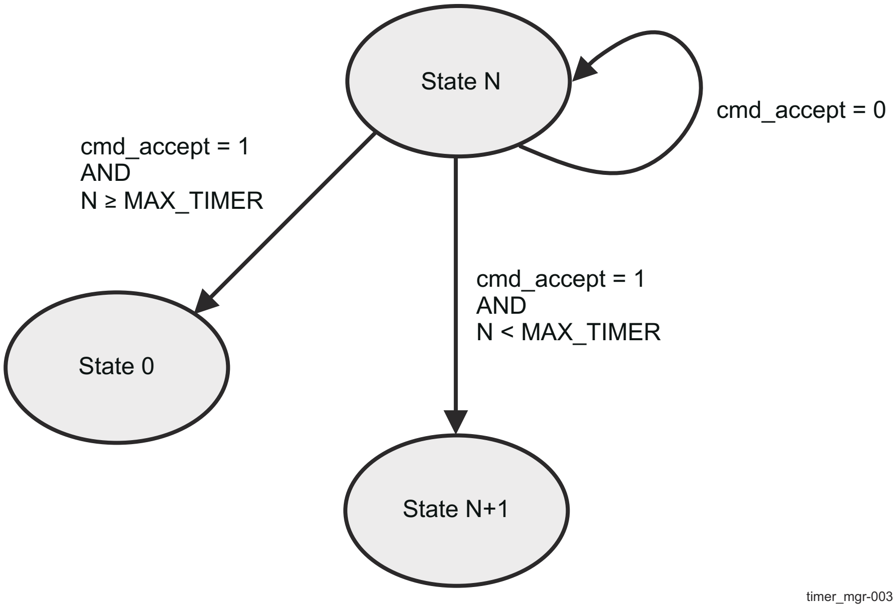

Figure 10-8. Timer State Machine

The timer states are sequential, that is, Timer 0 is checked, then Timer 1 is checked, then Timer 2, and so on. The Timer Control FSM will stall in a given state if the cmd_accept signal from the ksdw_spram_ecc module goes low, and will remain there until the ECC RAM will accept a command.

The timer state always transitions from N to N+1, unless N meets or exceeds the programmed MAX_TIMER value, in which case the system will start over at state 0.

10.2.3.4 Timer Reprogramming

There is a reprogramming module that runs in lock step with the FSM, always one state ahead – the FSM exports its next_state for use by the reprogramming RAM.

This RAM keeps track of the setup values for the timers as programmed by the TIMERMGR_SETUP_j_k memory mapped locations. There is a SET flag for each timer outside of the RAM – if this SET flag is true for the next_state timer, the VBUS ready signals are deasserted; if there is a pending timer setup, there cannot be a read or write to the memory, as this would interrupt the Timer FSM state machine and, with enough accesses, potentially cause the system to exceed the 10-µs window for timer accuracy.

10.2.3.4.1 Periodic Hardware Timers

By default, timers remain expired until they are either disabled or reset by software. However, by setting the TIMERMGR_CONTROL_j_k[8] AUTORESET bit for a timer, it will be treated as a periodic hardware timer by the timer manager.

A periodic hardware timer automatically resets itself after expiration. When a periodic hardware timer expires, it is flagged so that on the next pass of the timer control loop, the timer is reprogrammed with the stored TIMERMGR_SETUP_j_k value, allowing a timer to repeatedly timeout at intervals equal to the setup value. No software writes are required to clear a periodic hardware timer after it is expired.

There are no *down* events for a periodic hardware timer. A periodic hardware timer pushes an *up* event to the event FIFO when it expires and then resets itself, but does not push any *down* events.

10.2.3.5 Event FIFO

As the subsystem event aggregator requires more than one cycle to process events, there is an internal FIFO to store the generated events. Events may be generated by expiring timers or by activity on the CBA interface, as disabled timers or reset timers must send an event deactivation if the timer was previously expired.

This has an impact on performance, as if there are too many timer expirations in a given window, it potentially violates the 10-µs requirement (this is true without the event FIFO as well, given that the system cannot keep up with a timer expiring every cycle, in the worst case).

10.2.3.6 Timer Manager Unmapped Events mapping

The timer manager generates unmapped events which are routed to Interrupt Aggregator (IA) inside the main DMSS (steering logic for unmapped events) and then it is routed back to PSILSS to its proper place, either used as a DMA trigger or routed to IA core function to generate interrupt.

The registers in DMSS programs the OES (Output Event Source) for Timer Manager. The registers are unmap0[x], x = 0,1…1023 and its address is expressed as 48180000h + x*8 (x*8 is in decimal). For more information on the unmap register see INTAGGR_UNMAP_UNMAP0_MAP_j

10.2.4 Timer Manager Programming Guide

10.2.4.1 Timer Manager Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

10.2.4.1.1 Surrounding Modules Global Initialization

This procedure initializes the surrounding modules when the Timer Manager module is used for the first time after a device reset.

Table 10-10. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC	Timer Manager interface clock must be enabled. For more information, see *Clocking*
CPTS	CPTS0 configuration must be performed as CPTS0 is the tick source for Timer manager timers. See *CPTS*

10.2.4.1.2 Initialization Sequence

Initialization of the Timer Manager must include the following steps:

1. Set the number of timers to be used. TIMER_MGR_CNTL[10-1] MAX_TIMER
    - This controls the loop over the timer RAM and is the highest ID timer that will be used in the operation of the Timer Manager (MAX_TIMER + 1 is the total number of timers in use)
    - This number must not change during the course of operation; it can only be changed when TIMER_MGR_CNTL[0] ENABLE = 0. It is assumed that the user will set the MAX_TIMER value as required.
    - This step can be skipped if using all timers. MAX_TIMER defaults to 1024 (that is, all timers in use).
2. Write output event mapping for all timers to the DMSS. This must be done before enabling timer manager and must not be done again once the timer manager has been enabled.
3. Write initial setup values to the TIMER_MGR_TIMERS_PAGE_ENTRY_SETUP_J_K registers. All timers that will be used initially must have a setup value before the Timer Manager is enabled.
4. Enable individual timers. There are two ways to do this.
    - To enable all timers, use the TIMER_MGR_CNTL[12] MASS_ENABLE bit. This will enable all timers from 0 to MAX_TIMER.
        - Note that MAX_TIMER and MASS_ENABLE should be set in successive writes, or the previous value of MAX_TIMER will be used for MASS_ENABLE
        - MASS_ENABLE must only be used during initialization.
    - Alternately, individual timers can be enabled or disabled with TIMER_MGR_TIMERS_PAGE_ENTRY_CONTROL_J_K
        - It is therefore faster to set the individual TIMER_MGR_TIMERS_PAGE_ENTRY_CONTROL_J_K bits if more than half of the in-use timers are to be enabled initially. If more than half of the in-use timers are to be enabled initially, it is faster to use MASS_ENABLE and then disable specific timers with the TIMER_MGR_TIMERS_PAGE_ENTRY_CONTROL_J_K bits.
5. Enable the timer manager. Set TIMER_MGR_CNTL[0] ENABLE to 1.

10.2.4.1.3 Real-time Operating Requirements

While running, a CPU can take the following actions to enable, disable, or touch the timers:

10.2.4.1.3.1 Timer Touch

When a timer needs to be updated – indicating that an interface or function is still alive and timeout should be delayed – there are two means of touching a timer:

- If the timer's respective TIMERMGR_SETUP_j_k has the appropriate value for its function, the timer can be set again by writing a 1 to the SET bit of the TIMERMGR_CONTROL_j_k register.
    - As the timer should remain enabled, this effectively means writing a 3 to the TIMERMGR_CONTROL_j_k register for the timer to be touched

- If the timer's respective TIMERMGR_SETUP_j_k needs a new value, writing this value has the side effect of also setting the timer – there is no need to also write to the SET bit of TIMERMGR_CONTROL_j_k. This should be relatively infrequent during operation, as the setup values for all timers must be written during initialization.

The preferred method for touching timers is using the SET bit of TIMERMGR_CONTROL_j_k. It is considerably more efficient. The reprogramming RAM is a single port RAM, and repeated writes to the TIMERMGR_SETUP_j_k registers will impact overall timer performance and may result in longer periods before a valid timeout is observed.

10.2.4.1.3.2 Timer Disable

When a timer is no longer in use, the timer should be disabled with the respective TIMERMGR_CONTROL_j_k enable bit.

A disabled timer does not stop the time for that timer relative to the counter, and its current value is considered invalid once disabled. A timer should not be disabled and then subsequently re-enabled without reprogramming/re-setting, as it may timeout unexpectedly.

10.2.4.1.3.3 Timer Enable

To enable a timer while the Timer Manager is running, the timer must first be setup again.

- If the current TIMERMGR_SETUP_j_k is appropriate for the timer's intended use, the timer can be re-enabled by writing a 3 to the TIMERMGR_CONTROL_j_k register. (ENABLE = 1, SET = 1)
- If the current TIMERMGR_SETUP_j_k needs to be changed, write to the TIMERMGR_SETUP_j_k before re-enabling the timer. After this value is changed, the timer can be re-enabled by writing 0x3 to the TIMERMGR_CONTROL_j_k register (ENABLE = 1, SET = 1)
  - While TIMERMGR_SETUP_j_k implies SET, it must still be set as the timer is enabled.

10.2.4.1.4 Power Up/Power Down Sequence

The timer manager must be disabled (clear TIMERMGR_CNTL[0] ENABLE to 0) before the timer manager is powered down. The timer manager will only be idle if it is not enabled and the event FIFO is empty – an enabled Timer Manager means the state machine is running and the timer manager is waiting for expired timers.

To power up the Timer Manager if it has been powered down but not reset, the timer values in the timer RAM must be assumed to be invalid. Any timers must either be reprogrammed (TIMER_SET) before the timer is re-enabled. If this is not done, the Timer Manager may report timeouts as soon as it is enabled.

Additionally, all timers that have expired must be cleared before disabling the Timer Manager, otherwise there will be no Event Down generated on the event interface to clear the expired timers from the interrupt aggregator. This effectively means that software must disable all timers before writing a 0 to TIMERMGR_CNTL[0] ENABLE.

The event FIFO will continue to drive pending events even if the Timer Manager is disabled, so the remaining Event Down actions will still occur – software only needs to disable the timers to ensure that the Event Down commands are pushed into the event FIFO but does not need to wait for the event FIFO to flush before disabling the timer manager.

10.3 Time Sync and Compare Events

10.3.1 Time Sync Architecture

This section provides a high-level overview of the SoC time synchronization architecture.

10.3.1.1 Time Sync Architecture Overview

Table 10-11 shows the network time synchronization functions supported by the device.

Table 10-11. Network Time Synchronization Functions in the SoC

Interface	Time Sync Functions	Supported by
2×PRU-ICSSG	IEEE 1588-2008 (1/2-step), 802.1AS, TSN	PRU-ICSSG firmware
1×PCIE	Precision time measurement (PTM)	PCIe controller hardware
1×CPSW	IEEE 1588-2008 (2-step), 802.1AS	CPTS in CPSW
External input reference clock	External time/clock reference	CPTS in SoC

Note

These time sync functions are described in detail in their respective chapters.

Any of these functions can be a time sync source in the system. A sync router (TIMESYNC_INTRTR0) provides flexibility for each time domain to choose its synch source independently. In addition, there is also a router (CMPEVT_INTRTR0) that provides selection of active counter compare events for routing as CPU or DMA events.

Figure 10-9 shows a high-level overview of the SoC time sync architecture.

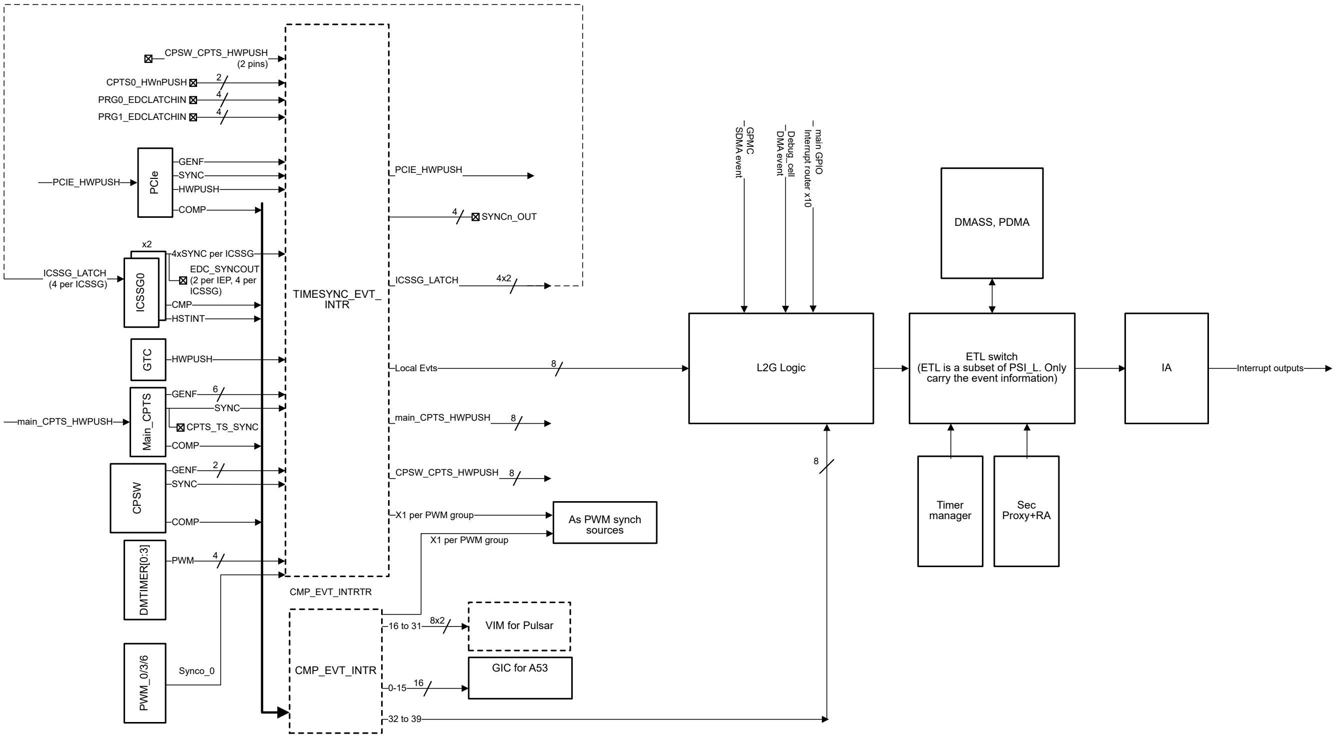

Figure 10-9. SoC Time Sync Architecture

10.3.2 Time Sync Routers

10.3.2.1 Time Sync Routers Overview

The timesync event router (TIMESYNC_INTRTR0) and compare event router (CMPEVT_INTRTR0) are instantiations of the generic interrupt router module in the device.

The TIMESYNC_INTRTR0 implements a set of multiplexers to provide selection of active CPTS time sync events for routing to CPTS capable modules. There is one register per output that controls the selection (TIMESYNC_INTRTR0_MUXCNTL_y).

The CMPEVT_INTRTR0 implements a set of multiplexers to provide selection of active CPTS counter compare events for routing as CPU or DMA events. There is one register per output that controls the selection (CMPEVT_INTRTR0_MUXCNTL_y).

Table 10-12 summarizes the configuration details for TIMESYNC_INTRTR0 and CMPEVT_INTRTR0.

Table 10-12. TIMESYNC_INTRTR0 and CMPEVT_INTRTR0 Configuration

Module	Number of Inputs	Number of Outputs	Input Interrupt Type
TIMESYNC_INTRTR0	42	41	Level
CMPEVT_INTRTR0	83	43	Pulse

Refer to *INTRTR Overview* for the general programming sequence that is recommended to be followed for all interrupt routers in the device.

10.3.2.2 Time Sync Routers Integration

This section describes the time sync routers integration in the device, including information about clocks, resets and hardware requests.

10.3.2.2.1 TIMESYNC_INTRTR0 Integration

Figure 10-10 below shows the integration of TIMESYNC_EVENT_INTRTR0 in the device

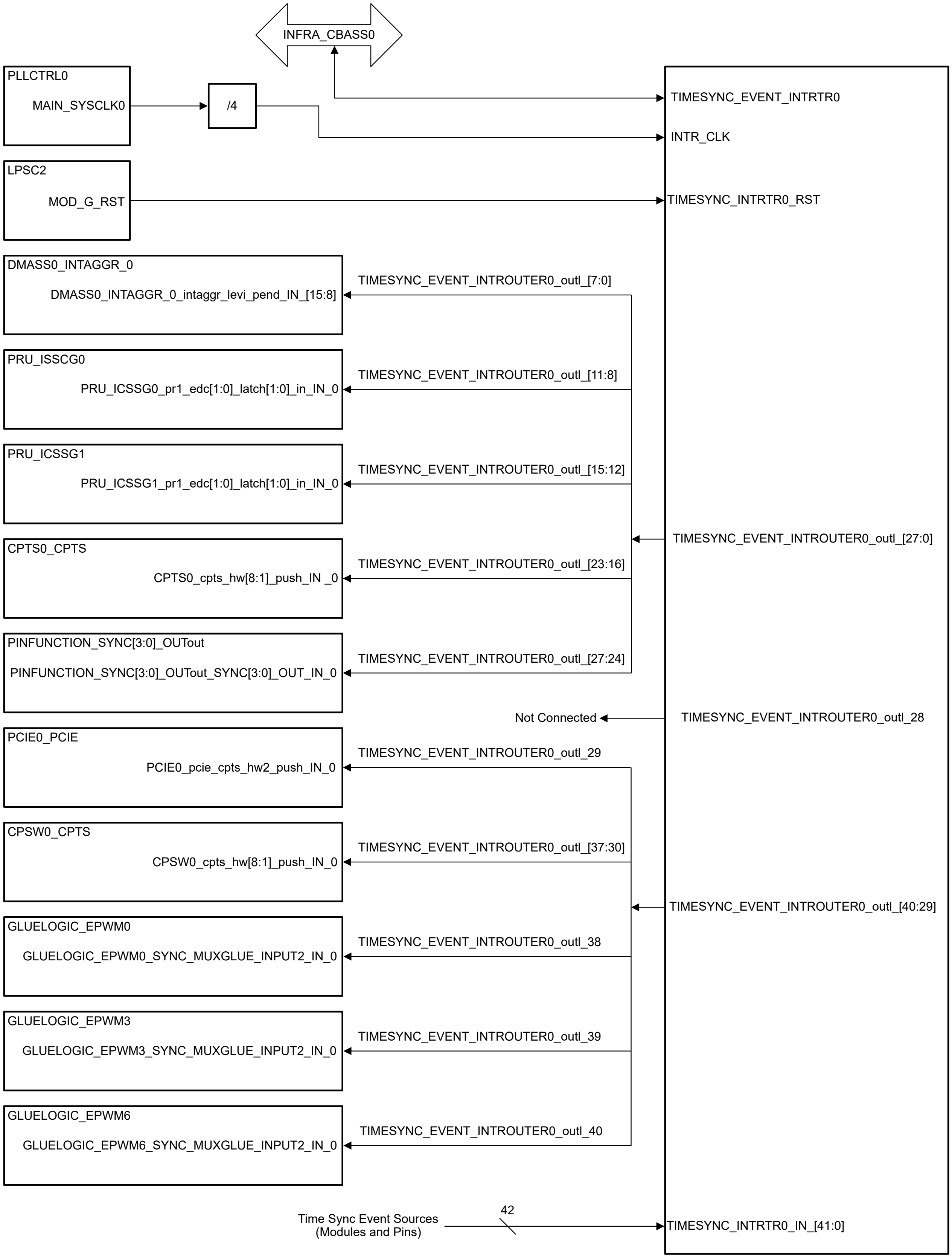

Figure 10-10. TIMESYNC_INTRTR0 Integration

TIMESYNC_INTRTR0 Integration Attributes through TIMESYNC_INTRTR0 Hardware Requests (Outputs) summarize the TIMESYNC_INTRTR0 integration.

Table 10-13. TIMESYNC_INTRTR0 Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
TIMESYNC_EVENT_INTRTR0	PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	INFRA_CBASS0

Table 10-14. TIMESYNC_INTRTR0 Clocks

Clocks				
Module Instance	Module Clock Input	Source Signal	Source	Description
TIMESYNC_EVENT_INTRTR0	INTR_CLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMESYNC_INTRTR0 functional and interface clock

Table 10-15. TIMESYNC_INTRTR0 Resets

Resets				
Module Instance	Module Reset Input	Source Signal	Source	Description
TIMESYNC_EVENT_INTRTR0	TIMESYNC_INTRTR0_RST	MOD_G_RST	LPSC2	TIMESYNC_INTRTR0 reset

Table 10-16. TIMESYNC_INTRTR0 Hardware Requests (Outputs)

Module Time Sync Events (Outputs)					
Module Instance	Module Sync Output	Destination Sync Signal	Destination	Description	Type
TIMESYNC_EVENT_INTROUTER0	TIMESYNC_EVENT_INTROUTER0_outl_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_8	DMASS0_INTAGGR_0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_1	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_9	DMASS0_INTAGGR_0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_2	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_10	DMASS0_INTAGGR_0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_3	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_11	DMASS0_INTAGGR_0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_4	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_12	DMASS0_INTAGGR_0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_5	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_13	DMASS0_INTAGGR_0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_6	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_14	DMASS0_INTAGGR_0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_7	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_15	DMASS0_INTAGGR_0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_8	PRU_ICSSG0_pr1_edc0_latch0_in_IN_0	PRU_ICSSG0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_9	PRU_ICSSG0_pr1_edc0_latch1_in_IN_0	PRU_ICSSG0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_10	PRU_ICSSG0_pr1_edc1_latch0_in_IN_0	PRU_ICSSG0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_11	PRU_ICSSG0_pr1_edc1_latch1_in_IN_0	PRU_ICSSG0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_12	PRU_ICSSG1_pr1_edc0_latch0_in_IN_0	PRU_ICSSG1	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_13	PRU_ICSSG1_pr1_edc0_latch1_in_IN_0	PRU_ICSSG1	TIMESYNC_EVENT_INTROUTER0 interrupt request	level

Table 10-16. TIMESYNC_INTRTR0 Hardware Requests (Outputs) (continued)

Module Time Sync Events (Outputs)					
Module Instance	**Module Sync Output**	**Destination Sync Signal**	**Destination**	**Description**	**Type**
	TIMESYNC_EVENT_INTROUTER0_outl_14	PRU_ICSSG1_pr1_edc1_latch0_in_IN_0	PRU_ICSSG1	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_15	PRU_ICSSG1_pr1_edc1_latch1_in_IN_0	PRU_ICSSG1	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_16	CPTS0_cpts_hw1_push_IN_0	CPTS0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_17	CPTS0_cpts_hw2_push_IN_0	CPTS0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_18	CPTS0_cpts_hw3_push_IN_0	CPTS0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_19	CPTS0_cpts_hw4_push_IN_0	CPTS0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_20	CPTS0_cpts_hw5_push_IN_0	CPTS0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_21	CPTS0_cpts_hw6_push_IN_0	CPTS0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_22	CPTS0_cpts_hw7_push_IN_0	CPTS0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_23	CPTS0_cpts_hw8_push_IN_0	CPTS0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_24	PINFUNCTION_SYNC0_OUTout_SYNC0_OUT_IN_0	PINFUNCTION_SYNC0_OUTout	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_25	PINFUNCTION_SYNC1_OUTout_SYNC1_OUT_IN_0	PINFUNCTION_SYNC1_OUTout	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_26	PINFUNCTION_SYNC2_OUTout_SYNC2_OUT_IN_0	PINFUNCTION_SYNC2_OUTout	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_27	PINFUNCTION_SYNC3_OUTout_SYNC3_OUT_IN_0	PINFUNCTION_SYNC3_OUTout	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_28	Not Connected			
	TIMESYNC_EVENT_INTROUTER0_outl_29	PCIE0_pcie_cpts_hw2_push_IN_0	PCIE0_PCIE	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_30	CPSW0_cpts_hw1_push_IN_0	CPSW0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_31	CPSW0_cpts_hw2_push_IN_0	CPSW0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_32	CPSW0_cpts_hw3_push_IN_0	CPSW0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_33	CPSW0_cpts_hw4_push_IN_0	CPSW0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_34	CPSW0_cpts_hw5_push_IN_0	CPSW0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_35	CPSW0_cpts_hw6_push_IN_0	CPSW0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_36	CPSW0_cpts_hw7_push_IN_0	CPSW0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_37	CPSW0_cpts_hw8_push_IN_0	CPSW0_CPTS	TIMESYNC_EVENT_INTROUTER0 interrupt request	level

Table 10-16. TIMESYNC_INTRTR0 Hardware Requests (Outputs) (continued)

Module Time Sync Events (Outputs)					
Module Instance	**Module Sync Output**	**Destination Sync Signal**	**Destination**	**Description**	**Type**
	TIMESYNC_EVENT_INTROUTER0_outl_38	GLUELOGIC_EPWM0_SYNC_MUXGLUE_INPUT2_IN_0	GLUELOGIC_EPWM0	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_39	GLUELOGIC_EPWM3_SYNC_MUXGLUE_INPUT2_IN_0	GLUELOGIC_EPWM3	TIMESYNC_EVENT_INTROUTER0 interrupt request	level
	TIMESYNC_EVENT_INTROUTER0_outl_40	GLUELOGIC_EPWM6_SYNC_MUXGLUE_INPUT2_IN_0	GLUELOGIC_EPWM6	TIMESYNC_EVENT_INTROUTER0 interrupt request	level

Table 10-17. TIMESYNC_INTRTR0 Hardware Requests (Inputs)

Module Time Sync Events (Inputs)		
Module Instance	**Module Sync Input**	**Time Sync Event Sources**
TIMESYNC_EVENT_INTRTR0	TIMESYNC_INTRTR0_IN_[0:41]	See Section 9.5.2 for mapping of time sync events to TIMESYNC_INTRTR0 inputs

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Note

For more information on the interconnects, see *System Interconnect* .

For more information on the power, reset and clock management, see the corresponding sections within *Device Configuration* .

10.3.2.2.2 CMPEVT_INTRTR0 Integration

Figure 10-11 below shows the integration of CMP_EVENT_INTROUTER0 in the device

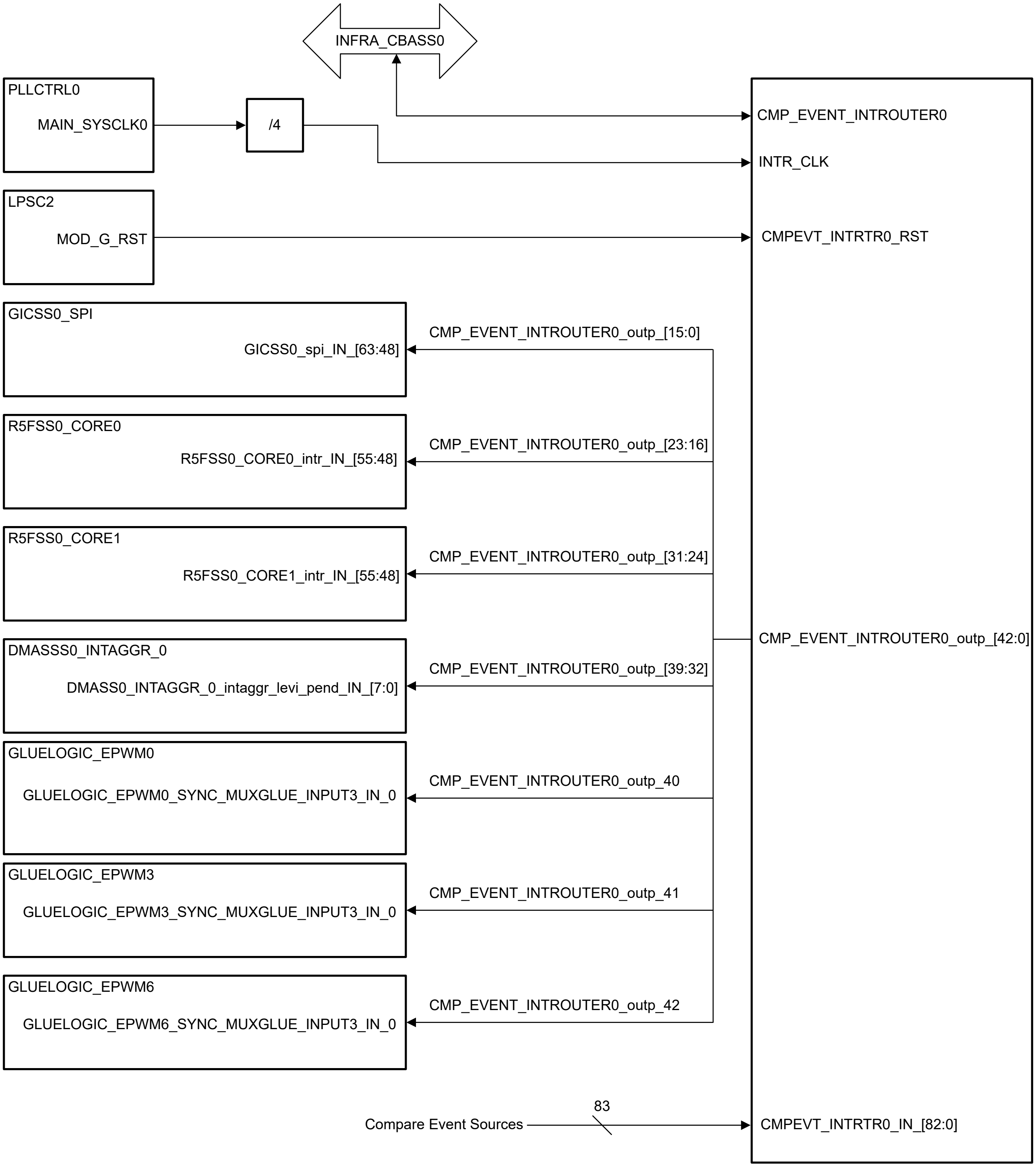

Figure 10-11. CMPEVT_INTRTR0 Integration

CMPEVT_INTRTR0 Integration Attributes through CMPEVT_INTRTR0 Hardware Requests (Outputs) summarize the CMPEVT_INTRTR0 integration.

Table 10-18. CMPEVT_INTRTR0 Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
CMP_EVENT_INTROUTER0	PSC0	GP_CORE_CTL	LPSC_MAIN_ALWAYSON	INFRA_CBASS0

Table 10-19. CMPEVT_INTRTR0 Clocks

Clocks				
Module Instance	Module Clock Input	Source Signal	Source	Description
CMP_EVENT_INTROUTER0	INTR_CLK	MAIN_SYSCLK0/4	PLLCTRL0	CMPEVT_INTRTR0 functional and interface clock

Table 10-20. CMPEVT_INTRTR0 Resets

Resets				
Module Instance	Module Reset Input	Source Signal	Source	Description
CMP_EVENT_INTROUTER0	CMPEVT_INTRTR0_RST	MOD_G_RST	LPSC2	CMPEVT_INTRTR0 reset

Table 10-21. CMPEVT_INTRTR0 Hardware Requests (Outputs)

Module Compare Events (Outputs)					
Module Instance	Module Compare Event Output	Destination Input	Destination	Description	Type
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_outp_0	GICSS0_spi_IN_48	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_1	GICSS0_spi_IN_49	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_2	GICSS0_spi_IN_50	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_3	GICSS0_spi_IN_51	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_4	GICSS0_spi_IN_52	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_5	GICSS0_spi_IN_53	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_6	GICSS0_spi_IN_54	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_7	GICSS0_spi_IN_55	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_8	GICSS0_spi_IN_56	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_9	GICSS0_spi_IN_57	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_10	GICSS0_spi_IN_58	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_11	GICSS0_spi_IN_59	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_12	GICSS0_spi_IN_60	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_13	GICSS0_spi_IN_61	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_14	GICSS0_spi_IN_62	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse

Table 10-21. CMPEVT_INTRTR0 Hardware Requests (Outputs) (continued)

Module Compare Events (Outputs)					
Module Instance	**Module Compare Event Output**	**Destination Input**	**Destination**	**Description**	**Type**
	CMP_EVENT_INTROUTER0_outp_15	GICSS0_spi_IN_63	GICSS0_SPI	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_16	R5FSS0_CORE0_intr_IN_48	R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_17	R5FSS0_CORE0_intr_IN_49	R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_18	R5FSS0_CORE0_intr_IN_50	R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_19	R5FSS0_CORE0_intr_IN_51	R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_20	R5FSS0_CORE0_intr_IN_52	R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_21	R5FSS0_CORE0_intr_IN_53	R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_22	R5FSS0_CORE0_intr_IN_54	R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_23	R5FSS0_CORE0_intr_IN_55	R5FSS0_CORE0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_24	R5FSS0_CORE1_intr_IN_48	R5FSS0_CORE1	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_25	R5FSS0_CORE1_intr_IN_49	R5FSS0_CORE1	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_26	R5FSS0_CORE1_intr_IN_50	R5FSS0_CORE1	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_27	R5FSS0_CORE1_intr_IN_51	R5FSS0_CORE1	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_28	R5FSS0_CORE1_intr_IN_52	R5FSS0_CORE1	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_29	R5FSS0_CORE1_intr_IN_53	R5FSS0_CORE1	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_30	R5FSS0_CORE1_intr_IN_54	R5FSS0_CORE1	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_31	R5FSS0_CORE1_intr_IN_55	R5FSS0_CORE1	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_32	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_0	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_33	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_1	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_34	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_2	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_35	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_3	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_36	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_4	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_37	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_5	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_38	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_6	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_39	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_7	DMASS0_INTAGGR_0	CMP_EVENT_INTROUTER0 interrupt request	pulse

Table 10-21. CMPEVT_INTRTR0 Hardware Requests (Outputs) (continued)

Module Compare Events (Outputs)					
Module Instance	**Module Compare Event Output**	**Destination Input**	**Destination**	**Description**	**Type**
	CMP_EVENT_INTROUTER0_outp_40	GLUELOGIC_EPWM0_SYNC_MUXGLUE_INPUT3_IN_0	GLUELOGIC_EPWM0	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_41	GLUELOGIC_EPWM3_SYNC_MUXGLUE_INPUT3_IN_0	GLUELOGIC_EPWM3	CMP_EVENT_INTROUTER0 interrupt request	pulse
	CMP_EVENT_INTROUTER0_outp_42	GLUELOGIC_EPWM6_SYNC_MUXGLUE_INPUT3_IN_0	GLUELOGIC_EPWM6	CMP_EVENT_INTROUTER0 interrupt request	pulse

Table 10-22. CMPEVT_INTRTR0 Hardware Requests (Inputs)

Module Compare Events (Inputs)		
Module Instance	**Module Compare Input**	**Compare Event Sources**
CMP_EVENT_INTROUTER0	CMPEVT_INTRTR0_IN_[0:82]	See Section 9.5.1 for mapping of compare events to CMPEVT_INTRTR0 inputs

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Note

For more information on the interconnects, see *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within *Device Configuration*.

10.3.3 Time Sync Event Sources

Chapter 11

Data Movement Architecture

This chapter describes the data movement architecture of the device.

11.1 Data Movement Architecture Overview

This chapter is a high-level summary of the data movement architecture implemented in the device.

11.1.1 Overview

The primary goal of the device Data Movement Architecture and related Subsystems is to ensure that data can be efficiently transferred from a producer to a consumer while meeting the real time requirements of the system can be met.

The Data Movement Subsystem (DMSS) aims to facilitate direct memory access (DMA) and provides a consistent Application Programming Interface (API) to the host software.

Data movement tasks are commonly offloaded from the host processor to peripheral hardware to increase system performance. Significant performance gains may result from careful design of the interface between the host software and the underlying acceleration hardware. In networking applications, packet transmission and reception are critical tasks. In general purpose compute, ping pong buffer prefetch and store are critical tasks as well as general mis-aligned block copy operations.

The design goals for the device Data Movement Architecture and are as follows:

- Minimize cost
- Minimize host overhead
- Maximize memory use efficiency
- Maximize bus burst efficiency
- Maximize symmetry between transmit/receive operations
- Maximize scalability for number of connections / buffer sizes / queue sizes / protocols supported
- Minimize protocol specific features
- Minimize complexity

11.1.1.1 Ring Accelerator (RINGACC)

The ring accelerator (RINGACC or RA) is a hardware module that is responsible for accelerating management of various types of queues in the system. The RINGACC accelerates passing of packets between a producer and consumer in normal system memory (including cached memory). The RINGACC is capable of accelerating the read/write pointer maintenance and occupancy tracking operations.

The ring accelerator operates like a bus infrastructure bridge in that it passes transactions through it between a source and destination interface. As transactions are passed, the RINGACC modifies the address, byte count, and transaction identifiers and internally updates the occupancies/pointers.

Each queue that the RINGACC provides can operate in either exposed-ring-mode or private-queue-mode.

- The exposed ring mode allows software to directly access the underlying ring structure to add or remove items from the tail or head of the ring respectively. Whenever items are added or removed from a ring, the host software is required to write to a corresponding doorbell register (RINGRT[a]_RT_DB) to increment or decrement the ring occupancy. When using the exposed ring mode, no proxy is required between the software and the RINGACC but all queue add operations require a memory fence to be performed to ensure that the data has landed in a snoopable cache before the doorbell register is written.
- The private queue mode provides an abstract view of the ring so that the host software does not need to know the actual physical address location or current read or write indexes of the ring. The private queue mode provides a memory window for each ring which when written redirects the write to the address pointed to by the write pointer and when read redirects the read to the address pointed to by the read pointer. The same address range is always used to push or pop elements from a given queue.

Rings are an implementation of a logical queue with the following limitations:

- Each ring has a finite size. When rings are used in exposed ring mode the following conditions apply:
  - A separate operation is required to write/read the contents of a ring and to update the occupancy of the ring
  - It is not straightforward to allow multiple producers to write to a ring or multiple consumers to read from a ring. Additional synchronization and pointer passing is required since rings require software to manage one of the pointers for the queue.

  - An exposed ring cannot be used when software or hardware needs to both read and write the same queue (such as for a DMA RX free queue where errors can have the DMA write the element back onto the same RX free queue). Since software owns one side of the pointers and hardware owns the other, they cannot be kept coherent if either side needs to update either at any time.

The RINGACC allows each ring to be configured to a different primary element size. Element sized chunks of data are placed onto and retrieved from rings when queuing or de-queueing occurs. Element sizes can be as small as 4 bytes or as large as 256 bytes.

11.1.1.2 Secure Proxy (SEC_PROXY)

A proxy provides a mechanism for software to access the RINGACC coherently when the processor does not support large bursts. The RINGACC requires a single burst for each operation so that it maintains atomicity and coherence by relying on the atomicity of the bursts on the bus interconnect fabric, since it only delivers a single burst to the RINGACC before the next. Since processors are usually limited in the size of a burst they can deliver natively, such as 32 to 128 bits, they cannot be used directly with the data access region of the RINGACC for larger element sizes. The proxy solves this gap by providing a temporary space for the software to form a larger burst of data before it is sent to the RINGACC. The proxy allows smaller processor accesses to the data and only forwards to the RINGACC when the entire data burst is complete, as directed by the software.

Each proxy hardware can support multiple threads of software (whether on the same or different processors) operating on bursts at the same time, and they do not interfere with each other, as long as each thread of software only operates on its thread in the proxy. Each proxy thread also supports access to any RINGACC queue via different offsets similar to how the RINGACC provides access to the queues via different offsets.

A special version of a proxy is the Secure Proxy that provides secured access to RINGACC queues for communication to the security initiator of the system. It provides basically the same function as a normal proxy. The data burst size is fixed for message sizes to the security initiator, so there is no support for all the element sizes of the RINGACC. The security initiator locks down the RINGACC queue to access and direction for each proxy thread so that the software cannot access anything they shouldn’t, so the software only sees a single queue (unlike the normal proxy), and any attempts to access another queue or access it in violation of how the security initiator defined and an error will be flagged. This allows for a much more controlled setup for passing messages to the security initiator.

11.1.1.3 Interrupt Aggregator (INTAGGR)

The interrupt aggregator (INTAGGR or INTA) is a hardware module which provides a persistent view of the real time status of various DMA components within the overall SoC DMA system. The main function of the module is to convert between 'global events' (assertion and de-assertion events transmitted on the event-transport-lane bus) and 'local events' (level sensitive signals on output, and level or edge sensitive signals on input).

The INTA block provides the following functions:

- Conversion of local event signal lines into global events
- Performing an 'Y-split' operation of global events
- Counting global events
- Steering and aggregation of global events into specified bit positions in one of N interrupt cause registers
- SoC interrupt-achitecture-compliant set/clear and mask set/clear functionality to cover interrupt cause registers

11.1.1.4 Packet DMA (PKTDMA)

The PKTDMA module supports the transmission and reception of various packet types. The PKTDMA is architected to facilitate the segmentation and reassembly of DMA data structure compliant packets to/from smaller data blocks that are natively compatible with the specific requirements of each connected peripheral. Multiple Tx and Rx channels are provided within the DMA which allow multiple segmentation or reassembly operations to be ongoing. The DMA controller maintains state information for each of the channels which allows packet segmentation and reassembly operations to be time division multiplexed between channels in order to share the underlying DMA hardware. An internal DMA scheduler is used to control the ordering and rate at which this multiplexing occurs for Transmit operations. The ordering and rate of Receive operations is indirectly controlled by the order in which blocks are pushed into the DMA on the Rx PSI-L interface.

A block diagram of the PKTDMA Controller is shown below:

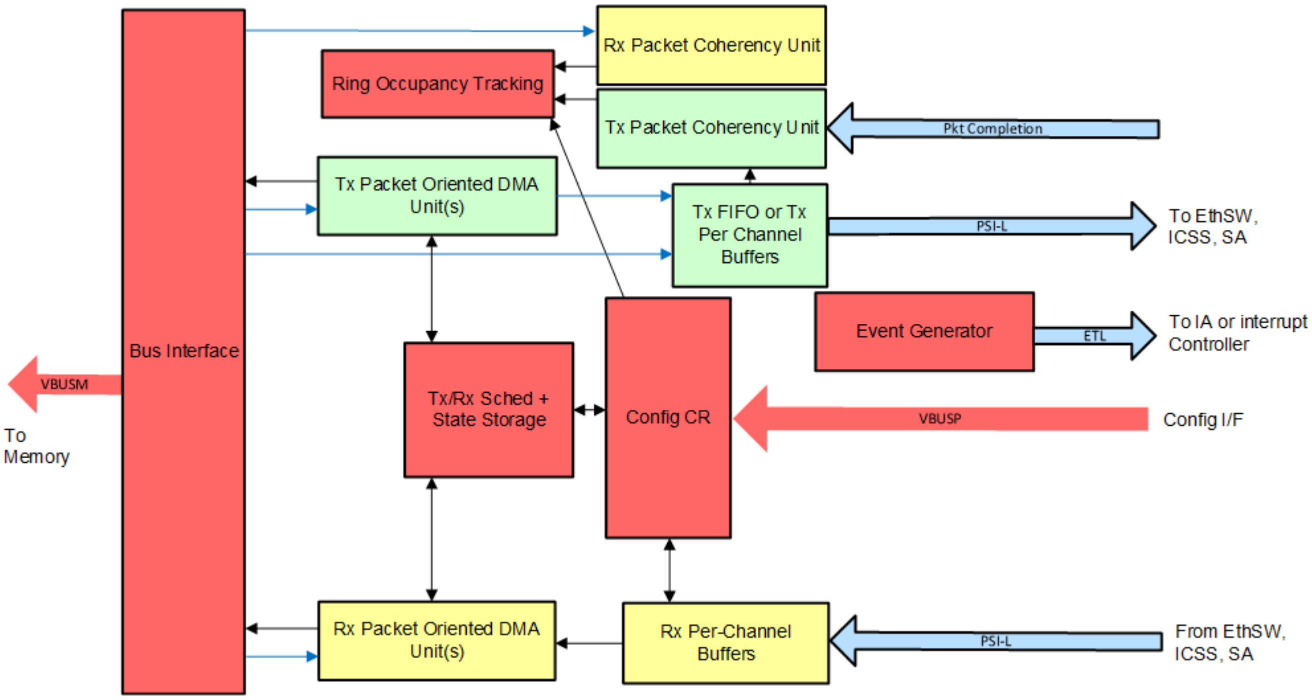

Figure 11-1. PKTDMA Block Diagram

11.1.1.4.1 PKTDMA Submodule Descriptions

11.1.1.4.1.1 Bus Interface Unit

The Bus Interface Unit is reponsible for merging and buffering all of the transactions that originate from the various initiator blocks inside the DMA controller into the 4 seperate VBUSM initiator interfaces. Arbitration between the blocks to a given VBUSM interface is round robin within a single priority level. A 2 word deep retiming buffer is provided on each sub interface of each provided VBUSM bus.

11.1.1.4.1.2 Config CR

The function of the Config CR is to switch transactions which arrive on the configuration interface to the various configuration targets within the DMA. The Config CR also provides a retiming buffer on the configuration bus primary interface ports.

11.1.1.4.1.3 Configuration Registers

The Configuration Registers block is responsible for monitoring the fullness level of the Tx Per Channel FIFOs, monitoring data transfer work which is pending, maintaining data movement thread state information, arbitrating which channel will be allowed to perform work next, issuing scheduler commands to the Tx PKTDMA core blocks, and writing back the updated state returned from those same DMA core blocks.

The Configuration Registers block is also responsible for providing memory mapped registers for configuration of the Rx DMA functions including the default settings for the free descriptor and destination queues. For modularity and high speed pipelining reasons, the Rx traffic is looped through the Configuration Registers block where the original stream information is merged with information from the configuration registers on its way to the Rx DMA unit module. This prevents the Rx DMA Core from having to spend cycles accessing the channel configuration information for the channel.

11.1.1.4.1.3.1 RX State Mapping

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
sop_descriptor_ptr[35:4]																															
0x80																															
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
sop_descriptor_ptr[35:4]												sop_descriptor_asel				curr_descriptor_ptr															
0x84																															
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
curr_descriptor_ptr																												curr_descriptor_asel			
0x88																															
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
curr_buffer_ptr																															
0x8C																															
128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
curr_buffer_ptr																curr_buffer_asel				curr_buffer_length											
0x90																															
160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
curr_buffer_length										curr_buffer_offset																					
0x94																															
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
curr_buffer_eop	pkt_length																					flush	ps_wordcnt						flowid_is_default	drop_flush	
0x98																															
224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
ps offset							ps_flags				pktid_data													orderid				priority			
0x9C																															

Table 11-1. RX State Mapping Table

Total Bits	Bits	Register Offset	Field	Description
31 - 0	31 - 0	0x80	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
43 - 32	11 - 0	0x84	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
47 - 44	15 - 12	0x84	sop_descriptor_asel	The asel for descriptor pointer at start of packet
63 - 48	31 - 16	0x84	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
91 -64	27 - 0	0x88	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
95 - 92	31 - 28	0x88	curr_descriptor_asel	The asel of the current descriptor
127 - 96	31 - 0	0x8C	curr_buffer_ptr	The pointer for the current buffer
143 - 128	15 - 0	0x90	curr_buffer_ptr	The pointer for the current buffer
147 - 144	19 - 16	0x90	curr_buffer_asel	The asel for the current buffer
159 - 148	9 - 0	0x90	curr_buffer_length	The length of the current buffer
169 - 160	31 - 20	0x90	curr_buffer_length	The length of the current buffer
191 - 170	31 - 10	0x94	curr_buffer_offset	The offset inside the current buffer
192	0	0x98	curr_buffer_eop	The end of packet flag for the current buffer
213 - 193	21 - 1	0x98	pkt_length	The size of the packet length
214	22	0x98	flush	The packet is being flushed
220 - 215	28 - 23	0x98	ps_wordcnt	protocol specific word count
221	29	0x98	flowid_is_default	Use default flow id
223 - 222	31 - 30	0x98	drop_flush	The flush is a drop condition
230 - 224	6 - 0	0x9C	ps offset	protocol specific offset
234 - 231	10 - 7	0x9C	ps_flags	protocol specific flags
247 - 235	23 - 11	0x9C	pktid_data	The pktid number for scoreboard
251 - 248	27 - 24	0x9C	orderid	The orderid of the packet
254 - 252	30 - 28	0x9C	priority	The priority of the packet

11.1.1.4.1.3.2 TX State Mapping

<table>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td colspan="32">sop_descriptor_ptr[35:4]</td></tr>
<tr><td colspan="32">0x80</td></tr>
<tr><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td><td>48</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr>
<tr><td colspan="12">sop_descriptor_ptr[35:4]</td><td colspan="4">sop_descriptor_asel</td><td colspan="16">curr_descriptor_ptr</td></tr>
<tr><td colspan="32">0x84</td></tr>
<tr><td>64</td><td>65</td><td>66</td><td>67</td><td>68</td><td>69</td><td>70</td><td>71</td><td>72</td><td>73</td><td>74</td><td>75</td><td>76</td><td>77</td><td>78</td><td>79</td><td>80</td><td>81</td><td>82</td><td>83</td><td>84</td><td>85</td><td>86</td><td>87</td><td>88</td><td>89</td><td>90</td><td>91</td><td>92</td><td>93</td><td>94</td><td>95</td></tr>
<tr><td colspan="28">curr_descriptor_ptr</td><td colspan="4">curr_descriptor_asel</td></tr>
<tr><td colspan="32">0x88</td></tr>
<tr><td>96</td><td>97</td><td>98</td><td>99</td><td>100</td><td>101</td><td>102</td><td>103</td><td>104</td><td>105</td><td>106</td><td>107</td><td>108</td><td>109</td><td>110</td><td>111</td><td>112</td><td>113</td><td>114</td><td>115</td><td>116</td><td>117</td><td>118</td><td>119</td><td>120</td><td>121</td><td>122</td><td>123</td><td>124</td><td>125</td><td>126</td><td>127</td></tr>
<tr><td colspan="32">curr_buffer_ptr</td></tr>
<tr><td colspan="32">0x8C</td></tr>
<tr><td>128</td><td>129</td><td>130</td><td>131</td><td>132</td><td>133</td><td>134</td><td>135</td><td>136</td><td>137</td><td>138</td><td>139</td><td>140</td><td>141</td><td>142</td><td>143</td><td>144</td><td>145</td><td>146</td><td>147</td><td>148</td><td>149</td><td>150</td><td>151</td><td>152</td><td>153</td><td>154</td><td>155</td><td>156</td><td>157</td><td>158</td><td>159</td></tr>
<tr><td colspan="16">curr_buffer_ptr</td><td colspan="4">curr_buffer_asel</td><td colspan="12">curr_buffer_length</td></tr>
<tr><td colspan="32">0x90</td></tr>
<tr><td>160</td><td>161</td><td>162</td><td>163</td><td>164</td><td>165</td><td>166</td><td>167</td><td>168</td><td>169</td><td>170</td><td>171</td><td>172</td><td>173</td><td>174</td><td>175</td><td>176</td><td>177</td><td>178</td><td>179</td><td>180</td><td>181</td><td>182</td><td>183</td><td>184</td><td>185</td><td>186</td><td>187</td><td>188</td><td>189</td><td>190</td><td>191</td></tr>
<tr><td colspan="10">curr_buffer_length</td><td colspan="22">curr_buffer_offset</td></tr>
<tr><td colspan="32">0x94</td></tr>
<tr><td>192</td><td>193</td><td>194</td><td>195</td><td>196</td><td>197</td><td>198</td><td>199</td><td>200</td><td>201</td><td>202</td><td>203</td><td>204</td><td>205</td><td>206</td><td>207</td><td>208</td><td>209</td><td>210</td><td>211</td><td>212</td><td>213</td><td>214</td><td>215</td><td>216</td><td>217</td><td>218</td><td>219</td><td>220</td><td>221</td><td>222</td><td>223</td></tr>
<tr><td>curr_buffer_eop</td><td colspan="22">rem_length</td><td>info_present</td><td>truncated_non_eop</td><td colspan="7">psbytes_rem</td></tr>
<tr><td colspan="32">0x98</td></tr>
<tr><td>224</td><td>225</td><td>226</td><td>227</td><td>228</td><td>229</td><td>230</td><td>231</td><td>232</td><td>233</td><td>234</td><td>235</td><td>236</td><td>237</td><td>238</td><td>239</td><td>240</td><td>241</td><td>242</td><td>243</td><td>244</td><td>245</td><td>246</td><td>247</td><td>248</td><td>249</td><td>250</td><td>251</td><td>252</td><td>253</td><td>254</td><td>255</td></tr>
<tr><td>psbytes_rem</td><td colspan="8">psbytes_off</td><td colspan="13">wptr_data</td><td colspan="2">pktid_data</td><td colspan="4">orderid</td><td colspan="3">priority</td><td></td></tr>
<tr><td colspan="32">0x9C</td></tr>
</table>

Table 11-2. TX State Mapping Table

Total Bits	Bits	Register Offset	Field	Description
31 - 0	31 - 0	0x80	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
43 - 32	11 - 0	0x84	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
47 - 44	15 - 12	0x84	sop_descriptor_asel	The asel for descriptor pointer at start of packet
63 - 48	31 - 16	0x84	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
91 -64	27 - 0	0x88	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
95 - 92	31 - 28	0x88	curr_descriptor_asel	The asel of the current descriptor
127 - 96	31 - 0	0x8C	curr_buffer_ptr	The pointer for the current buffer
143 - 128	15 - 0	0x90	curr_buffer_ptr	The pointer for the current buffer
147 - 144	19 - 16	0x90	curr_buffer_asel	The asel for the current buffer
159 - 148	9 - 0	0x90	curr_buffer_length	The length of the current buffer
169 - 160	31 - 20	0x90	curr_buffer_length	The length of the current buffer
191 - 170	31 - 10	0x94	curr_buffer_offset	The offset inside the current buffer
192	0	0x98	curr_buffer_eop	The end of packet flag for the current buffer
214 - 193	22 - 1	0x98	rem_length	The remaining length in the buffer
215	23	0x98	info_present	The packet has info present
216	24	0x98	truncated_non_eop	Eop if packet length is greater than the total buffer length
223 - 217	31 - 25	0x98	psbytes_rem	Number of protocol specific bytes remaining
224	0	0x9C	psbytes_rem	Number of protocol specific bytes remaining
232 - 225	8 - 1	0x9C	psbytes_off	The offset of the protocol specific bytes
245 - 233	21 - 9	0x9C	wptr_data	The current write pointer in the data fifo
247 - 246	23 - 22	0x9C	pktid_data	The pktid number for scoreboard
251 - 248	27 - 24	0x9C	orderid	The orderid of the packet
254 - 252	30 - 28	0x9C	priority	The priority of the packet

11.1.1.4.1.4 Tx Packet DMA Unit

The Tx Packet DMA Unit block implements all of the state machine functionality necessary to implement the KS3 DMA Host Tx protocol. The Tx Packet DMA unit initiates VBUSM transactions in order to read descriptor pointers from the memory mapped Tx ring, read descriptors from memory, and read data from buffers in memory.

11.1.1.4.1.5 Tx Packet Coherency Unit

The Tx Packet Coherency Unit is responsible for ensuring that all control structures and data have been read (and updated if applicable) by the Tx DMA unit(s) and that all previous packets on that channel/flow have also completed prior to incrementing the reverse ring occupancy for the channel/flow.

11.1.1.4.1.6 Tx Per Channel Buffers

The Tx Per Channel Buffers implement a FIFO for each Tx DMA channel that is used for buffering packet control and payload data that has been fetched by the Tx Packet DMA units. The buffers are byte oriented on write so that the data from the DMA units which may not be full words can be packed properly. The buffers are block oriented on read and each Tx (source) channel in the PKTDMA controller maps directly onto a thread in the Tx PSI interface. The Tx Per Channel Buffer block outputs queue fullness information to the Tx Scheduler block which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Tx Per Channel Buffer will initiate transfers to the target whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block will simultaneously monitor the status of all of the threads and will perform a round robin arbitration between the different threads for the use of the Transmit PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer will be included in the arbitration.

11.1.1.4.1.7 Rx Per Channel Buffers

The Rx Per Channel Buffers implement a FIFO for each Rx DMA channel that is used for buffering packet control and payload data that has been pushed into the DMA from the Rx PSI-L interface. The Rx Per Channel Buffers also includes an arbitration unit which determines which Rx DMA channel should be serviced next.

11.1.1.4.1.8 Rx Packet DMA Unit

The Rx Packet DMA Unit block implements all of the state machine functionality necessary to implement the KS3 DMA Rx protocol for Host descriptor types. The Rx Packet DMA Unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read buffer descriptor information, write descriptors to memory, and write data to buffers in memory.

11.1.1.4.1.9 Rx Packet Coherency Unit

The Rx Packet Coherency Unit is responsible for ensuring that all control structures and data have been written by the Rx DMA unit(s) and that all previous packets on that channel/flow have completed prior to incrementing the reverse ring occupancy for the channel/flow. This unit ensures that the ordering of the Packet Descriptor pointer writes to the return queue directly matches the ordering in which those packets were fetched from the Rx free queues. Writes are not considered complete by this unit until the entire write status has been returned for all outstanding transactions for a given packet ID.

11.1.1.4.1.10 Event Handler

The Event Handler block is responsible for generating channel completion and error events.

11.1.1.4.2 Channel Classes

Not all channels within the PKTDMA require the same performance capabilities. Raw bandwidth and latency tolerance requirements will vary greatly between data transfers at various points in the system. Due to area concerns, several different classes of DMA channels are provided in the PKTDMA and are described as follows:

Class Name	Description
Normal Capacity	Provides baseline amount of descriptor prefetch and Tx/Rx control and data buffering. Suitable for most peripheral transfers which are communicating with on-chip memories and DDR
High Capacity	Provides an elevated amount of descriptor prefetch and custom Tx/Rx control and data buffering. Suitable for applications which require moderate per-channel bandwidth with significantly increased latency (ex. Transferring data to/from PCIe)
Ultra-High Capacity	Provides identical descriptor and TR prefetch as High Capacity but with increased Tx data buffering to allow for more read data in flight. Suitable for applications requiring high per-channel bandwidth with significantly increased latency (ex. 16+Gbps transfers to/from PCIe).

PKTDMA instances may provide support for any or all of the above channel classes through design time configuration parameters.

11.1.1.5 Block Copy DMA (BCDMA)

The Block Copy DMA is intended to perform similar functions as an Embedded DMA (EDMA) and the DMA-P. The BCDMA module moves data from a memory mapped source address set to a corresponding memory mapped address. The BCDMA maintains state information for each of the channels which allows data copy operations to be time division multiplexed between channels in order to share the underlying DMA hardware. An internal DMA scheduler is used to control the ordering and rate at which this multiplexing occurs.

A block diagram of the Block Copy DMA Controller is shown below:

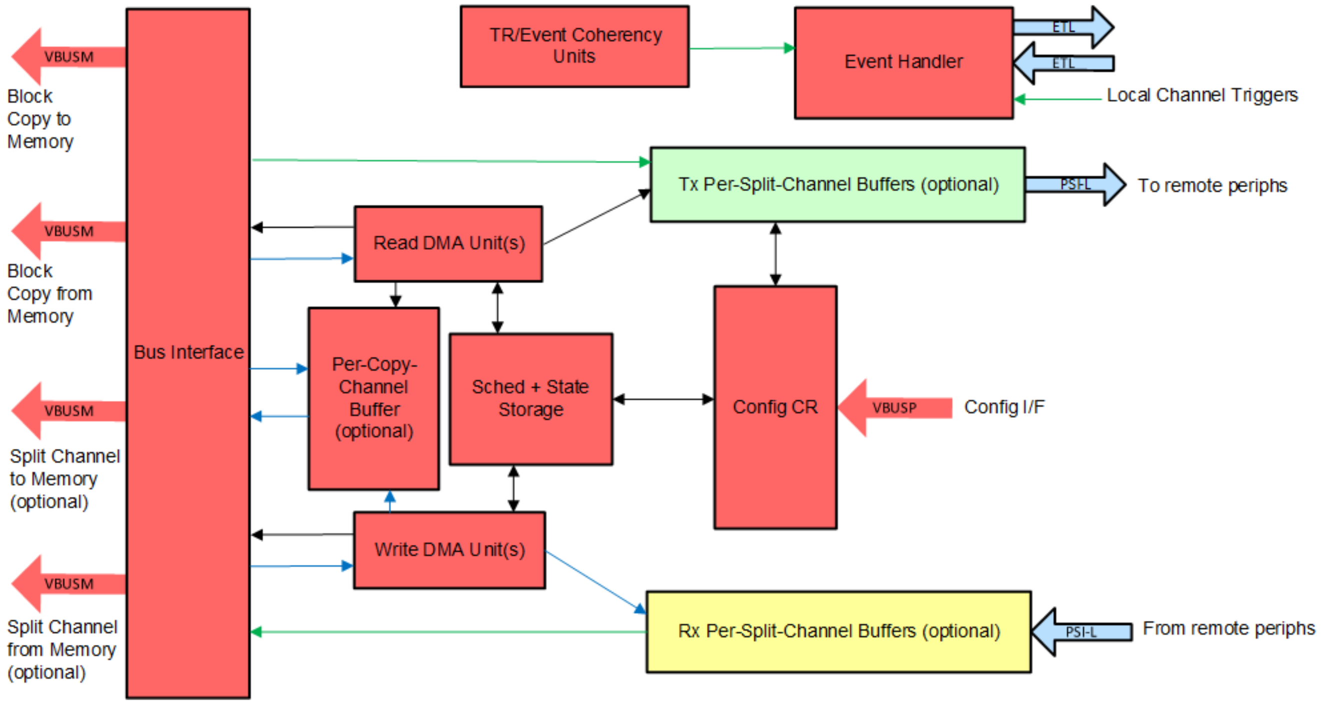

Figure 11-2. Block Copy DMA Block Diagram

11.1.1.5.1 BCDMA Submodule Descriptions

11.1.1.5.1.1 Bus Interface Unit

The Bus Interface Unit is reponsible for merging and buffering all of the transactions that originate from the various controller blocks inside the DMA controller into the 4 seperate VBUSM controller interfaces. Arbitration between the blocks to a given VBUSM interface is round robin within a single priority level. A 2 word deep retiming buffer is provided on each sub interface of each provided VBUSM bus.

11.1.1.5.1.2 Config CR

The function of the Config CR is to switch transactions which arrive on the configuration interface to the various configuration targets within the DMA. The Config CR also provides a retiming buffer on the configuration bus primary interface ports.

11.1.1.5.1.3 Configuration Registers

The Configuration Registers block is responsible for monitoring the fullness level of the Per Channel FIFOs, monitoring data transfer work which is pending, maintaining data movement thread state information, arbitrating which channel will be allowed to perform work next, issuing scheduler commands to the Read and Write DMA units, and writing back the updated state returned from those same DMA units.

The Configuration Registers block is also responsible for providing memory mapped registers for configuration of the DMA channels.

11.1.1.5.1.3.1 BCDMA Mapping Table

Table 11-3 applies to TX, RX and BC Mapping.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
reload_count				waitcomp	event_size		trigger0		trigger0_type		trigger1_type		trigger1_type		spflags				eop	eol			reload_count								
0x80																															
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
tr_dim1																															
0x84																															
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
tr_dim2																															
0x88																															
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
tr_dim3																															
0x8C																															
128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
tr_icnt0																tr_icnt1															
0x90																															
160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
tr_icnt2																tr_icnt3															
0x94																															
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
icnt1																icnt2															
0x98																															
224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
icnt3																rem_icnt0															
0x9C																															
256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
tr_addr																															
0xA0																															
288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
tr_addr				tr_asel				descriptor_ptr																							
0xA4																															
320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
descriptor_ptr												RVSD				curr_index														last_index	
0xA8																															
352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
last_index												nom_elsize			reload_index						curr_wptr										
0xAC																															
384		385		386		387		388		389		390		391		392		393		394		395		396		397		398		399	

curr_wptr	pktid	orderid	priority	trid	evtid	sot
0xB0						

Table 11-3. BCDMA Mapping Table

Total Bits	Bits	Register Offset	Field	Description
3 - 0	3 - 0	0x80	reload_count	
4	4	0x80	waitcomp	
6 - 5	6 - 5	0x80	event_size	
8 - 7	8 - 7	0x80	trigger0	
10 - 9	10 - 9	0x80	trigger0_type	
12 - 11	12 - 11	0x80	trigger1_type	
14 - 13	14 - 13	0x80	trigger1_type	
18 - 15	18 - 15	0x80	spflags	
19	19	0x80	eop	
22 - 20	22 - 20	0x80	eol	
31 - 23	31 - 23	0x80	reload_count	
63 - 32	31 - 0	0x84	tr_dim1	
95 - 64	31 - 0	0x88	tr_dim2	
127 - 96	31 - 0	0x8C	tr_dim3	
143 - 128	15 - 0	0x90	tr_icnt0	
159 - 144	31 - 16	0x90	tr_ictn1	
175 - 160	15 - 0	0x94	tr_ictn2	
191 - 176	31 - 16	0x94	tr_icnt3	
207 - 192	15 - 0	0x98	icnt1	
223 - 208	31 - 16	0x98	icnt2	
239 - 224	15 - 0	0x9C	icnt3	
255 - 240	31 - 16	0x9C	rem_icnt0	
287 - 256	31 - 0	0xA0	tr_addr	
291 - 288	3 - 0	0xA4	tr_addr	
295 - 292	7 - 4	0xA4	tr_asel	
319 - 296	31 - 8	0xA4	descriptor_ptr	
331 - 320	11 - 0	0xA8	descriptor_ptr	
349 - 336	29 - 16	0xA8	curr_index	
363 - 350	11 - 30	0xA8	last_index	
366 - 364	14 - 12	0xAC	nom_elsize	
372 - 367	20 - 15	0xAC	reload_index	
385 - 373	1 - 21	0xAC	curr_wptr	
387 - 386	3 - 2	0xB0	pktid	
391 - 388	7 - 4	0xB0	orderid	
394 - 392	10 - 8	0xB0	priority	
396 - 395	12 - 11	0xB0	trid	
398 - 397	14 - 13	0xB0	evtid	

Table 11-3. BCDMA Mapping Table (continued)

Total Bits	Bits	Register Offset	Field	Description
399	15	0xB0	sot	

11.1.1.5.1.4 Read Unit(s)

The Read Units implement all of the state machine functionality necessary to perform the read transfers defined in the SW supplied Transfer Request records. The read DMA unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read descriptors, Transfer Request records, and payload data from memory.

11.1.1.5.1.5 TR Coherency Unit

The TR Coherency Unit is responsible for ensuring that all control structures and data have been read (and updated if applicable) by the BCDMA unit(s) and all prior TRs have completed prior to incrementing the reverse ring occupancy for the flow/channel.

11.1.1.5.1.6 Per-Copy-Channel Buffers

The Per-Copy-Channel Buffers implement a FIFO for each BCDMA generic block copy channel and is used for buffering payload data that has been fetched by read DMA unit modules. The write DMA units issue write transfers from the Per Channel Buffers to specified addresses in memory. The buffers are byte oriented on both write and read so that the data from the DMA units which may not be full words can be packed and unpacked properly. This unit is optional and is only present if one or more generic block copy channels are configured in the BCDMA instance.

11.1.1.5.1.7 Tx Per-Split-Channel Buffers

The Tx Per-Split-Channel Buffers implement a FIFO for each BCDMA Tx split mode channel and is used for buffering payload data that has been fetched by read DMA unit modules. Data is transferred from the buffer to the remote peripheral via a PSI-L interface. This unit is optional and is only present if one or more Tx split mode channels are configured in the BCDMA instance.

11.1.1.5.1.8 Rx Per-Split-Channel Buffers

The Rx Per-Split-Channel Buffers implement a FIFO for each BCDMA Rx split mode channel and is used for buffering payload data that has been received from remote peripherals via a PSI-L interface. Data is read from these FIFOs and written out to memory as directed by the write DMA unit modules. This unit is optional and is only present if one or more Rx split mode channels are configured in the BCDMA instance.

11.1.1.5.1.9 Write Unit(s)

The Write Units implement all of the state machine functionality necessary to perform the write transfers defined in the SW supplied Transfer Request records. The write DMA unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read descriptors and/or Transfer Request records from memory mapped rings, read descriptor and Transfer Request records, and write payload data to memory.

11.1.1.5.1.10 Event Coherency Unit

The Event Coherency Unit is responsible for ensuring that all writes have completed prior to signaling an output event for a channel/flow.

11.1.1.5.1.11 Event Handler

The Event Handler block is responsible for generating channel completion and error events and for accepting and tracking channel triggering.

11.1.1.5.2 Channel Classes

Not all channels within a DMA controller require the same performance capabilities. Raw bandwidth and latency tolerance requirements will vary greatly between data transfers at various points in the system. Due to area concerns, several different classes of DMA channels are provided in the BCDMA and are described as follows:

Class Name	Description
Normal Capacity	Provides baseline amount of descriptor and TR prefetch and Tx/Rx control and data buffering. Suitable for most peripheral transfers which are communicating with on-chip memories and DDR
High Capacity	Provides an elevated amount of descriptor and TR prefetch and custom Tx/Rx control and data buffering. Suitable for applications which require moderate per-channel bandwidth with significantly increased latency (ex. Transferring data to/from PCIe)
Ultra-High Capacity	Provides identical descriptor and TR prefetch as High Capacity but with increased Tx data buffering to allow for more read data in flight. Suitable for applications requiring high per-channel bandwidth with significantly increased latency (ex. 16+Gbps transfers to/from PCIe).

BCDMA instances may provide support for any or all of the above channel classes through design time configuration parameters.

11.1.2 Definition of Terms

Channel— A channel refers to the sub-division of information (flows) that is transported across a DMA engine. Each channel has associated state information. Channels are used to segregate information flows based on the protocol used, scheduling requirements (for example, CBR, VBR, ABR), or concurrency requirements (that is, blocking avoidance). Information flow within a channel is a stream of strongly ordered information.

Data Buffer— A data buffer is a single data structure that contains payload information for transmission to or reception from a channel.

Buffer Descriptor— A buffer descriptor is a single data structure that contains information about one or more data buffers.

Packet Descriptor— A packet descriptor is another name for the first buffer descriptor within a packet. Some fields within a data buffer descriptor are only valid when it is a packet descriptor including the tags, packet length, packet type, and flags. All Monolithic type descriptors are packet descriptors (and are also a Data Buffer).

Queue— A queue is a list of strongly ordered entries which is typically used to pass work between a producer and a consumer. Queue entries in most cases are references to a work payload which is being passed but in some cases (Transfer Request Packets for example) queue entries may actually contain data which is being transferred. Queues are used throughout DMA whenever communication is required between entities. Queues can have multiple different implementations and DMA uses two of the most common: linked lists and rings.

Linked list— A linked list is a data structure in which each entry stores not only the entry data but also a chaining pointer to the next entry in the list. The last entry in each list has its chaining pointer set to NULL (typically encoded as 0x0). The list manager maintains a pointer to the head element on the list and to the tail element on the list. Since the chaining pointer is stored with the entry data, linked lists have a length which is dynamically changeable and limited only by the ability to allocate additional entries which are to be queued/de-queued. Linked lists are present in Host Descriptors to chain multiple descriptors to form a packet.

Ring— A ring is a data structure in which a contiguous memory block defined by M N-byte entries (total size is M × N bytes) is statically allocated and sequentially written/read in order to pass data or data references. Rings are also referred to as circular buffers because when the last element in the contiguous memory array is written, the pointers wrap back to the beginning address for the ring and start the process all over again. The Ring Accelerator component uses rings in order to implement logical queues.

Memory— Memory is an area of data storage managed by the host. This area is visible to the port as a 64-bit addressable area.

Device Driver— A device driver is application independent software that runs on the host for purposes abstracting the low level hardware so that upper level software can use the hardware without knowing every bit field location or initialization sequence.. General device driver functions include port initialization, transmit packet queuing, and receive packet processing.

SOP— Start of Packet. This refers to the descriptor/buffer that is the first buffer in a packet.

MOP— Middle of Packet. This refers to the descriptors/buffers that are neither the first or last buffers in a packet.

EOP— End of Packet. This refers to the descriptor/buffer that is the last buffer in a packet.

11.1.3 DMSS Hardware/Software Interface

The intent of the Data Movement architecture is to provide a uniform HW/SW interface which includes a rich set of mechanisms that SW can make use of to transfer data with low overhead and reasonable complexity. To this goal, the number of components which SW is required to interact with on an ongoing real time basis has been kept to a minimum and is as follows (in order of anticipated frequency of access):

- Interrupt Aggregator
- Packet DMA
- Block Copy DMA

When interrupts are used, the interrupt aggregator will provide the vast majority of interrupt sources from all DMA components in the system. Each non-exception/non-debug packet and TR completion signaling originates from the Interrupt Aggregator and the IA provides a uniform set of MMRs that can be queried to quickly determine the cause of a specific interrupt. Events from PSI-L/ETL components are all routed to the host via the Interrupt Aggregator.

Each PKTDMA and BCDMA instance includes an inbuilt ring control mechanism which is the primary means by which work is sent to or received from these DMAs. Each DMA instance also includes both static configuration type memory mapped registers and some real-time accessible memory mapped registers for monitoring and control of each individual channel.

Memory mapped data structures are used anytime information needs to be passed between components in the system. These components may be hardware or software. The following sections describe the data structures which are used within the DMSS for passing information. These data structures include data buffers, packet descriptors, buffer descriptors, queues (including transmit queues, transmit completion queues, and receive queues) and the configuration MMRs that are provided in the various components. The following sections provide a detailed description of these data structures.

11.1.3.1 Data Buffers

A data buffer is a byte aligned contiguous block of memory used to store payload data. Each buffer is described in an entry in either a packet descriptor or in a buffer descriptor. A data buffer may hold any portion of a packet and may be linked together (via descriptors) with other buffers to form packets. Data buffers may be allocated anywhere within the 64-bit memory space.

The Buffer Length field of the packet/buffer descriptor indicates the number of valid data bytes in the buffer. There may be from 1 to 4M-1 valid data bytes in each buffer.

11.1.3.2 Descriptors

Descriptors are so named because their primary function is to describe other data structures.

The PKTDMA architecture provides for 2 basic types of descriptors whose characteristics are shown in Table 11-4.

Table 11-4. PKTDMA Descriptor Types and Attributes

Descriptor Type	Includes Valid Packet Info	Provided # of Slots to Link In External Data	Provides Local Protocol Specific Storage	Provides Slot to Link Additional Descriptors Within Same Packet	Description
Host Packet Descriptor	✓	1	✓	✓	Used to describe packet and SOP buffer in applications that require Host OS compatible data structures (i.e. applications where the descriptors and buffers cannot be managed independently but must instead be pre-linked by the Host software). These applications inherently require a separate descriptor for each buffer.
Host Buffer Descriptor		1		✓	Used to describe non-SOP buffers in applications that require Host OS compatible data structures

As the above table shows, the Host Packet Descriptor provides packet level information that is useful to both the ports and the Host in order to properly process the packet. These descriptors are referred to as Packet Descriptors and will always appear as the first descriptor within a packet.

The PKTDMA allows descriptors to be allocated on 16-byte address boundaries. This is intended to allow for better memory utilization by allowing on-chip descriptors which are not a power of 2 in length to be packed into arrays with little wasted memory space.

Even though descriptors and buffers may be allocated on any 16-byte alignment, careful consideration of the alignment effects should be made based on the storage location and any cache related affects that may exist. If data structures are placed in off-chip SDRAM the burst size and alignment restrictions of the memory devices must be considered in order to avoid performance issues related to continually fetching mis-aligned blocks. In this case, the memory efficiency can be reduced to 50% because 2 memory bank lines are read for every line sized data fetch. Similarly, placing more than one descriptor or buffer object within a single cache line can cause the adjacent object to become corrupted during cache line writeback operations.

Software/application specific control information may be added to the end of any of the packet descriptor types using as many extra words as necessary but the above alignment rules still apply.

The Block Copy DMA architecture provides a single descriptor type whose characteristics are shown in Table 11-5.

Table 11-5. Block Copy DMA Descriptor Types and Attributes

Descriptor Type	Includes Valid Packet Info	Provided # of Slots to Link In External Data	Provides Local Protocol Specific Storage	Provides Slot to Link Additional Descripto Within Same Packet	Description
Transfer Request Packet Descriptor		0			Used to feed transfer request sequences to the BCDMA

11.1.3.2.1 Host Packet Descriptor

Host Packet Descriptors are designed to be used when the application requires support for true, unlimited fragment count scatter/gather type operations. The Host Packet Descriptor contains the following information:

- Indicator which identifies the descriptor as a Host Packet Descriptor
- Source and Destination Tags
- Packet Type
- Packet Length
- Protocol Specific Region Size
- Protocol Specific Control / Status Bits
- Pointer to the first valid byte in the SOP data buffer
- Length of the SOP data buffer
- Pointer to the next buffer descriptor in the packet
- Software specific information

Host Packet Descriptors always contain 48 bytes of required information and may also contain optional software specific information and protocol specific information. How much optional information (and therefore the allocated size of the descriptors) is required is application dependent.

The Host Packet descriptor layout is shown below.

Table 11-6. Host Packet Descriptor Layout

Packet Info (16 bytes)
Linking Info (8 bytes)
Buffer Info (12 bytes)
Original Buffer Info (12 bytes)
Extended Packet Info Block (Optional) Includes Timestamp and Software Data (16 bytes)
Protocol Specific Data (Optional) (0 to M bytes where M is a multiple of 4)
Other SW Data (Optional and User Defined)

Host Packet Descriptors may be linked with zero or more additional Host Buffer Descriptors in a singly linked list fashion to form packets. Each Host Packet consists of a single Host Packet Descriptor followed by a chain of zero or more Host Buffer Descriptors linked together using the Next Descriptor Pointer fields in the descriptors. The last descriptor in a Host packet has a zero Next Descriptor Pointer.

The 'Other SW Data' portion of the descriptor exists after all of the defined words and is reserved for use by the host software to store completely private data. This region is not used in any way by HW components in a PKTDMA system and these modules will not modify any bytes within this region.

The contents of the Host Packet Descriptor words are detailed in Table 11-7 through Table 11-23.

Table 11-7. Host Packet Descriptor Packet Information Word 0 (PD Word 0)

Bits	Name	Description	Rx Overwrite
31:30	2'd1	64-bit Host Packet Descriptor Type Identifier	Yes
29	Extended Packet Info Block Present	This field indicates the presence of the Extended Packet Info Block in the descriptor. 0 = EPIB is not present 1 = 16 byte EPIB is present	Yes
28	RESERVED	-	*Yes*
27:22	Protocol Specific Valid Word Count	This field indicates the valid # of 32-bit words in the protocol specific region. This is encoded in increments of 4 bytes as follows: 0 = 0 bytes 1 = 4 bytes … 16 = 64 bytes ... 32 = 128 bytes 33-63 = RESERVED	Yes
21:0	Packet Length	The length of the packet in bytes. If the Packet Length is less than the sum of the buffer lengths, then the packet data will be truncated. A Packet Length greater than the sum of the buffers is an error. The valid range for an exact packet length is 0 to 4M-1 bytes. If the packet length is set to 0, the port will not actually transmit any information.	Yes

Table 11-8. Host Packet Descriptor Packet Information Word 1 (PD Word 1)

Bits	Name	Description	Rx Overwrite
31:28	Error Flags	This field contains error flags that can be assigned based on the packet type	Yes
27:24	Protocol Specific Flags	This field contains protocol specific flags / information that can be assigned based on the packet type.	Yes
23:14	RESERVED	-	Yes
13:0	Flow ID	Flow ID within which this packet is being transported. The FlowID is used by downstream blocks to make decisions about packet steering and resource allocations. FlowIDs are also used to allow specific packets to be received into specific sets of buffers.	Yes

Table 11-9. Host Packet Descriptor Packet Information Word 2 (PD Word 2)

Bits	Name	Description	Rx Overwrite
31:27	Packet Type	This field indicates the type of this packet and is encoded as follows: 0-31 = Application specific	Yes
26:16	RESERVED	-	Yes
15:0	RESERVED	-	Yes

Table 11-10. Host Packet Descriptor Packet Information Word 3 (PD Word 3)

Bits	Name	Description	Rx Overwrite
31:24	Source Tag – Hi	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L src_tag field bits 15:8.	Yes
23:16	Source Tag – Lo	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L src_tag field bits 7:0.	Yes

Table 11-10. Host Packet Descriptor Packet Information Word 3 (PD Word 3) (continued)

Bits	Name	Description	Rx Overwrite
15:8	Dest Tag – Hi	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L dst_tag field bits 15:8.	Yes
7:0	Dest Tag – Lo	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L dst_tag field bits 7:0	Yes

Table 11-11. Host Packet Descriptor Linking Word 0 (PD Word 4)

Bits	Name	Description	Rx Overwrite
31:0	Next Descriptor Pointer LSB	The 32 LSBs of the 48-bit word aligned memory address of the next buffer descriptor in the packet. If the value of this pointer is zero then the current buffer is the last buffer in the packet. The host sets the Next Descriptor Pointer.	No

Table 11-12. Host Packet Descriptor Linking Word 1 (PD Word 5)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
19:16	Next Descriptor Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.	No

Table 11-12. Host Packet Descriptor Linking Word 1 (PD Word 5) (continued)

Bits	Name	Description	Rx Overwrite
15:0	Next Descriptor Pointer MSB	The 16 MSBs of the 48-bit next descriptor pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-13. Host Packet Descriptor Buffer 0 Info Word 0 (PD Word 6)

Bits	Name	Description	Rx Overwrite
31:0	Buffer 0 Pointer LSB	The Buffer Pointer is the byte aligned memory address of the buffer associated with the buffer descriptor. This value will be written during reception. These are the 32 LSBs of the 48-bit buffer pointer. **THIS Value along with the MSB bits cannot be 0 or the buffer will be seen as a NULL PTR**	Yes

Table 11-14. Host Packet Descriptor Buffer 0 Info Word 1 (PD Word 7)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		Yes
19:16	Buffer 0 Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.	Yes
15:0	Buffer 0 Pointer MSB	The 16 MSBs of the 48-bit buffer pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	Yes

Table 11-15. Host Packet Descriptor Buffer 0 Info Word 2 (PD Word 8)

Bits	Name	Description	Rx Overwrite
31:22	RESERVED	Written to 0	Yes
21:0	Buffer 0 Length	The Buffer Length field indicates how many valid data bytes are in the buffer.	Yes

Table 11-16. Host Packet Descriptor Reserved Word 0 (PD Word 9)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-17. Host Packet Descriptor Reserved Word 1 (PD Word 10)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-18. Host Packet Descriptor Reserved Word 2 (PD Word 11)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
15:0	RESERVED		No

This word is only present if the Extended Packet Info Block present bit is set in Word 0

Table 11-19. Host Packet Descriptor Extended Packet Info Block Word 0 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Timestamp Info	This field contains an application specific timestamp which can be used for traffic shaping in a QoS enabled system.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-20. Host Packet Descriptor Extended Packet Info Block Word 1 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 0	This field stores software centric information that needs to travel with the packet through the stack. . This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-21. Host Packet Descriptor Extended Packet Info Block Word 2 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 1	This field stores software centric information that needs to travel with the packet through the stack. . This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-22. Host Packet Descriptor Extended Packet Info Block Word 3 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 2	This field stores software centric information that needs to travel with the packet through the stack. . This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

Table 11-23. Host Packet Descriptor Protocol Specific Word N (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Protocol Specific Data N	This field stores information which varies depending on the block and packet type.	Configurable

11.1.3.2.2 Host Buffer Descriptor

The Host Buffer Descriptor is identical in size and organization to a Host Packet Descriptor but does not include valid information in the packet level fields and does not include a populated region for protocol specific information. Host Buffer Descriptors are designed to be linked onto a Host Packet Descriptor or another Host Buffer Descriptor to provide support for unlimited scatter / gather type operations. Host Buffer Descriptors provide information about a single corresponding data buffer. Every Host buffer descriptor stores the following information:

- Pointer to the first valid byte in the data buffer
- Length of the data buffer
- Pointer to the next buffer descriptor in the packet

Host Buffer Descriptors always contain 48 bytes of required information. Since it is a requirement that it is possible to convert a Host descriptor between a Buffer Descriptor and a Packet Descriptor (by filling in the appropriate fields) in practice, Host Buffer Descriptors will be allocated using the same sizes as Host Packet Descriptors. The Host Buffer Descriptor layout is shown below.

Table 11-24. Host Buffer Descriptor Layout

Buffer Reclamation Info (16 bytes)
Linking Info (8 bytes)
Buffer Info (12 bytes)
Original Buffer Info (12 bytes)

A Host Packet Descriptor and zero or more Host Buffer Descriptors may be linked together using the Next Descriptor Pointer fields to form packets. The last descriptor in a packet has a zero Next Descriptor Pointer. Each Host Buffer descriptor also points to a single data buffer.

The contents of the Host Buffer Descriptor words are detailed in Table 11-25 through Table 11-33.

Table 11-25. Host Buffer Descriptor Reserved Word 0 (BD Word 0)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED	-	No

Table 11-26. Host Buffer Descriptor Reserved Word 1 (BD Word 1)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED	-	No

Table 11-27. Host Buffer Descriptor Reserved Word 2 (BD Word 2)

Bits	Name	Description	Rx Overwrite
31:16	RESERVED	-	No
15:0	RESERVED	-	No

Table 11-28. Host Buffer Descriptor Reserved Word 3 (BD Word 3)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-29. Host Buffer Descriptor Linking Word 0 (BD Word 4)

Bits	Name	Description	Rx Overwrite
31:0	Next Descriptor Pointer LSB	The 32 LSBs of the 48-bit word aligned memory address of the next buffer descriptor in the packet. If the value of this pointer is zero then the current buffer is the last buffer in the packet. The host sets the Next Descriptor Pointer.	No

Table 11-30. Host Buffer Descriptor Linking Word 1 (BD Word 5)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
19:16	Next Descriptor Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.	No
15:0	Next Descriptor Pointer MSB	The 16 MSBs of the 48-bit next descriptor pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-31. Host Buffer Descriptor Buffer N Info Word 1 (BD Word 6)

Bits	Name	Description	Rx Overwrite
31:0	Buffer 0 Pointer LSB	The Buffer Pointer is the byte aligned memory address of the buffer associated with the buffer descriptor. This value will be written during reception.These are the 32 LSBs of the 48-bit buffer pointer.	No

Table 11-32. Host Buffer Descriptor Buffer N Info Word 1 (BD Word 7)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
19:16	Buffer 0 Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.	No
15:0	Buffer 0 Pointer MSB	The MSBs of the 48-bit buffer pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-33. Host Buffer Descriptor Buffer N Info Word 2 (BD Word 8)

Bits	Name	Description	Rx Overwrite
31:22	RESERVED		No
21:0	Buffer N Length	The Buffer Length field indicates how many valid data bytes are in the buffer. Unused or protocol specific bytes at the beginning of the buffer are not counted in the Buffer Length field. This value will be overwritten during reception.	No

Table 11-34. Host Buffer Descriptor Original Buffer Info Word 0 (BD Word 9)

Bits	Name	Description	Rx Overwrite
31:28	RESERVED		No

Table 11-34. Host Buffer Descriptor Original Buffer Info Word 0 (BD Word 9) (continued)

Bits	Name	Description	Rx Overwrite
27:0	Original Buffer 0 Length	The Buffer Length field indicates the original size of the buffer in bytes. Data bytes are in the buffer. This value will not be overwritten during reception. This value is read by the Rx DMA to determine the actual buffer size as allocated by the host at initialization. Since the buffer length in BD Word 8 is overwritten by the Rx port during reception, this field is necessary to permanently store the buffer size information.	No

Table 11-35. Host Buffer Descriptor Original Buffer Info Word 1 (BD Word 10)

Bits	Name	Description	Rx Overwrite
31:0	Original Buffer 0 Pointer LSB	The Buffer Pointer is the byte aligned memory address of the buffer associated with the buffer descriptor. This value will not be overwritten during reception. This value is read by the RX DMA to determine the actual buffer location as allocated by the host at initialization. Since the buffer pointer in BD Words 6/7 is overwritten by the Rx port during reception, this field is necessary to permanently store the buffer pointer information. This field contains the 32 LSBs of the 48-bit original buffer pointer	No

Table 11-36. Host Buffer Descriptor Original Buffer Info Word 2 (BD Word 11)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		Yes

Table 11-36. Host Buffer Descriptor Original Buffer Info Word 2 (BD Word 11) (continued)

Bits	Name	Description	Rx Overwrite
19:16	Original Buffer 0 Pointer Address Space Select	Effectively bits 51:48 of the address – treated special by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.	Yes
15:0	Original Buffer 0 Pointer MSB	The 16 MSBs of the 48-bit original buffer pointer	No

11.1.3.2.3 Transfer Request Descriptor

The Transfer Request Descriptor contains the following information:

- Indicator which identifies the descriptor as a TR Descriptor
- Set of one or more Transfer Request Records
- Set of one or more Transfer Response Records

Transfer Request Packet Descriptors always contain 16 bytes of required information and a variable number of Transfer Request / Transfer Response Records (request and response counts match).

The Transfer Request descriptor layout is shown below.

Table 11-37. Transfer Request Packet Descriptor Layout

Packet Info Given via Transfer Request Packet Descriptor Word 0-3 (16 bytes)
Null (0-102 bytes to bring start of TR request array into natural alignment for memory fetch efficiency)
Array of Transfer Request Records
Array of Transfer Response Records

Table 11-38. Transfer Request Packet Descriptor Word 0

Bits	Name	Description	Rx Overwrite
31:30	2’d3	TR Packet Descriptor type.	No
29	RESERVED		No
28:20	Reload Count	Specifies what to do when the last entry is processed in this packet. This field specifies how many times to return to the Reload Index upon reaching the Last Entry. When an internal count is incremented to this value and the TR indicated by the Last Entry has been processed, this packet will be considered complete and the descriptor will be placed back on the return queue specified in Word 2. A value of 0x1FF indicates that a perpetual loop is desired. In this case, the loop count is considered infinite and the internal count will not be incremented. A teardown operation on the channel will cause the loop to be broken at the nearest iteration boundary.	No

Table 11-38. Transfer Request Packet Descriptor Word 0 (continued)

Bits	Name	Description	Rx Overwrite
19:14	Reload Index	Specifies the value to set the current processing index to when the last entry is processed and the Reload Enable is set to 1. This is basically an absolute index to jump to on the 2**nd** and following passes through the TR packet.	No
13:0	Last Entry	Specifies the index of the last valid entry in this packet	No

Table 11-39. Transfer Request Packet Descriptor Word 1

Bits	Name	Description	Rx Overwrite
31:28	RESERVED	-	No
27	RESERVED		No
26:24	Transfer Request Nominal Element Size	Specifies the stride between TR entries. The value in this field must be set large enough that any TR in the buffer will fit within the given dimension. TRs are expected to be placed on boundaries as given in this dimension. This field is also used to calculate the location where the Transfer Responses will be written back. This field is encoded as follows: 0 = 16 byte Transfer Request record size 1 = 32-byte Transfer Request record size 2 = 64-byte Transfer Request record size 3 = 128-byte Transfer Request record size 4-7 = RESERVED	No
23:14	RESERVED	-	No
13:0	RESERVED	-	No

Table 11-40. Transfer Request Packet Descriptor Word 2

Bits	Name	Description	Rx Overwrite
31:17	RESERVED		Yes
16	RESERVED	-	Yes
15:0	RESERVED	-	Yes

Table 11-41. Transfer Request Packet Descriptor Word 3

Bits	Name	Description	Rx Overwrite
31:24	RESERVED	-	No
15:0	RESERVED	-	No

Table 11-42. Transfer Request Packet Descriptor Payload Words 0-N

Bits	Name	Description	Rx Overwrite
31:0	Transfer Control Record Array	Transfer Control Records. This is an array of records which encapsulate the Transfer Request and Transfer Response messages which are used by the BCDMA	Yes (partial)

11.1.3.3 Transfer Request Record

11.1.3.3.1 Overview

This section describes the standard transfer request (TR) format to initiate a DMA transfer. The TRs can support both half and full duplex with multiple dimensions. Each TR will also generate a TR response. A TR can be sent to the BCDMA either through a TR descriptor using a pass-by-reference ring or as a Direct TR submission using a pass-by-value ring.

Table 11-43. Terms and Definitions

Term	Definition
TR	A transfer request to move data.
CR	A cache operation request. A request to send messages to a specified cache controller to prepare the cache for a future operation.

11.1.3.3.2 Addressing Algorithm

For a basic TR request the same algorithm is used. The innermost loop always consumes physically contiguous elements from memory. Its implicit dimension is 1 byte. The pointer itself moves from fetch to fetch on the maximum byte alignments specified for the BCDMA, in increasing order. In each level outside the inner loop, the loop moves the pointer to a new location based on the size of that loop level's dimension.

11.1.3.3.2.1 Linear Addressing (Forward)

The following code illustrates the basic algorithm for a 4 level loop nest block move. This model assumes that it transfers data 1 byte at a time and the input and output block are the same size in all dimensions.

```
// sptr is a byte pointer.
// dptr is a byte pointer.
// Source address is indirect
if (TR_ISA) {
    sptr = *sptr;
}
// Destination address is indirect
if (TR_IDA) {
    dptr = *dptr;
}
// TR_TRIGX can be selected to come from Global events, Local event, or none.
// Check for trigger of TYPE0
if (TR_TRIG0_TYPE == TYPE0) while(!TR_TRIG0);
if (TR_TRIG1_TYPE == TYPE0) while(!TR_TRIG1);
for (i3 = 0; i3 < ICNT3; i3++)
{
    sptr3 = sptr; // save current position before entering next level
    dptr3 = dptr; // save current position before entering next level
    // Check for trigger of TYPE1
    if (TR_TRIG0_TYPE == TYPE1) while(!TR_TRIG0);
    if (TR_TRIG1_TYPE == TYPE1) while(!TR_TRIG1);
    for (i2 = 0; i2 < ICNT2; i2++) {
        sptr2 = sptr; // save current position before entering next level
        dptr2 = dptr; // save current position before entering next level
        // Check for trigger of TYPE2
        if (TR_TRIG0_TYPE == TYPE2) while(!TR_TRIG0);
        if (TR_TRIG1_TYPE == TYPE2) while(!TR_TRIG1);
        for (i1 = 0; i1 < ICNT1; i1++) {
            sptr1 = sptr; // save current position before entering next level
            dptr1 = dptr; // save current position before entering next level
            // Check for trigger of TYPE3
            if(TR_TRIG0_TYPE == TYPE3) while(!TR_TRIG0);
            if(TR_TRIG1_TYPE == TYPE3) while(!TR_TRIG1);
            for (i0 = 0; i0 < ICNT0; i0++) {
                // BCDMA can combine these in optimized burst aligned accesses.
                *dptr = *sptr;
                sptr = sptr++;
                dptr = dptr++;
            }
        // Update based on saved pointer for this level
        sptr = sptr1 + SDIM1;
        dptr = dptr1 + DDIM1;
        }
    // Update based on saved pointer for this level
    sptr = sptr2 + SDIM2;
    dptr = dptr1 + DDIM2;
    }
```

This form of addressing allows programs to specify regular paths through memory in a small number of parameters. Additionally, it allows for various stall points through the loop to allow for hardware or software induced pausing of the transfer. The following section defines these parameters in detail.

11.1.3.3.3 Transfer Request Formats

The BCDMA defines a four-level loop nest for addressing elements within the TR, using the algorithms described in the Addressing algorithm. Most of the fields in the TR template map directly to the parameters in those algorithms.

Table 11-44. Transfer Request Fields

Field Name	Description	Size
FLAGS	TR flags that specify type of TR and how the TR should be handled. It also supports the TR triggering and output events.	32 bits

Table 11-44. Transfer Request Fields (continued)

Field Name	Description	Size
ICNT0	Total loop iteration count for level 0 (innermost)	16 bits
ICNT1	Total loop iteration count for level 1	16 bits
ADDR	Starting address for the source data or destination data if it is a half duplex write.	64 bits
DIM1	Signed dimension for loop level 1 for the source data	32 bits
ICNT2	Total loop iteration count for level 2	16 bits
ICNT3	Total loop iteration count for level 3 (outermost)	16 bits
DIM2	Signed dimension for loop level 2	32 bits
DIM3	Signed dimension for loop level 3	32 bits
DDIM1	Signed dimension for loop level 1 for the destination data	32 bits
DADDR	Starting address for the destination of the data	64 bits
DDIM2	Signed dimension for loop level 2 for the destination data	32 bits
DDIM3	Signed dimension for loop level 3 for the destination data	32 bits
DICNT0	Total loop iteration count for level 0 (innermost) used for destination	16 bits
DICNT1	Total loop iteration count for level 1 used for destination	16 bits
DICNT2	Total loop iteration count for level 2used for destination	16 bits
DICNT3	Total loop iteration count for level 3 used for destination	16 bits

The TR assumes all iteration counts as unsigned integers, and all dimensions as signed integers representing byte offsets.

The template above fully specifies the type of elements, length, and dimensions of the transfer.

Since all transfers will not require all the fields the TRs have the type field which allow the number of words required to be sent for the TR to be reduced.

11.1.3.3.4 Flags Field Definition

The next diagram expands the 32-bit FLAGS field. The numbers above each field here indicate bit numbers within the field.

Table 11-45. Transfer Request Template FLAGS Field

31	30	29	28	27	26	25	24
CONFIGURATION SPECIFIC FLAGS							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
TRIGGER1_TYPE		TRIGGER1		TRIGGER0_TYPE		TRIGGER0	
7	6	5	4	3	2	1	0
EVENT_SIZE		WAIT	RESERVED	TYPE			

The flags field fills in the remaining details about the stream, as follows:

Table 11-46. FLAGS Field Descriptions

Bit	Field	Description
0-3	**TYPE**	The TYPE of TR that is being sent 0: One dimensional data move 1: Two dimensional data move 2: Three dimensional data move 3: Four dimensional data move 4: Four dimensional data move with data formatting 5: Four dimensional Cache Warm 6-7: Reserved 8: Four Dimensional Block Move 9: Four Dimensional Block Move with Repacking 10: Two Dimensional Block Move 11: Two Dimensional Block Move with Repacking 12-14: Reserved 15 Four Dimensional Block Move with Repacking and Indirection
4	Reserved	Reserved for Future use.
5	**WAIT**	This field is only valid on Type 15 TRs. This field indicates whether or not this TR should ensure it completes before allowing the next TR to start on this channel. The encoding is as follows: 0 = Allow next TR to start immediately 1 = Wait for this TR to complete before allowing next TR to start When set, the next TR will not be considered triggered (regardless of any other trigger conditions) until all write status responses for the current TR have landed.

Table 11-46. FLAGS Field Descriptions (continued)

Bit	Field	Description
6-7	**EVENT_SIZE**	This is how often the TR will generate an output event. 0: Event is only generated with the TR is complete 1: Event is generated when the second inner most loop (ICNT1) is decremented by 1. 2: Event is generated when the third inner most loop (ICNT2) is decremented by 1. 3: Event is generated when the outer most loop (ICNT3) is decremented by 1.
8-9	**TRIGGER0**	This is one of two selectable triggers. The receipt of this trigger will enable the TR to be active for enough data transfer as specified by the TRIGGER0_TYPE Field. 0: No Trigger 1: Global Trigger 0 for the channel 2: Global Trigger 1 for the channel 3: Local Event for the channel
10-11	**TRIGGER0_TYPE**	This is the type of data transfer that will be enabled by receiving a trigger. 0: The second inner most loop (ICNT1) will be decremented by 1. 1: The third inner most loop (ICNT2) will be decremented by 1. 2: The outer most loop (ICNT3) will be decremented by 1. 3: The entire TR will be allowed to complete.
12-13	**TRIGGER1**	This is one of two selectable triggers. The receipt of this trigger will enable the TR to be active for enough data transfer as specified by the TRIGGER1_TYPE Field. 0: No Trigger 1: Global Trigger 0 for the channel 2: Global Trigger 1 for the channel 3: Local Event for the channel This field is reserved for a Direct TR.
14-15	**TRIGGER1_TYPE**	This is the type of data transfer that will be enabled by receiving a trigger. 0: The second inner most loop (ICNT1) will be decremented by 1. 1: The third inner most loop (ICNT2) will be decremented by 1. 2: The outer most loop (ICNT3) will be decremented by 1. 3: The entire TR will be allowed to complete.
16-23	Reserved	Reserved for Future use.
24-31	**Configuration Specific Flags**	These are flag bits that can be specified by the specific BCDMA configuration. These bits will remain undefined in the global TR format to allow for customization requirements that might be required in the specific BCDMA implementation.

The following sections expand on each of these fields.

11.1.3.3.4.1 Type: TR Type Field

The TR Type field gives the size of the TR and which fields are expected in the TR. Based on the type the number of words required to be sent to complete the TR can be decreased. The tables below shows the minimum size for each TR as well if any fields will be treated as reserved.

Table 11-47. Transfer Request Minimum Size Type 0 One Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0	ADDR		RESERVED/NOT REQUIRED											

Table 11-48. Transfer Request Minimum Size Type 1 Two Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/ 1	ADDR		DIM1	RESERVED/NOT REQUIRED										

Table 11-49. Transfer Request Minimum Size Type 2 Three Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/ 1	ADDR		DIM1	ICNT2	DIM2	RESERVED/NOT REQUIRED								

Table 11-50. Transfer Request Minimum Size Type 3 Four Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/ 1	ADDR		DIM1	ICNT2/ 3	DIM2	DIM3	RESERVED/NOT REQUIRED							

Table 11-51. Transfer Request Minimum Size Type 15 Four Dimensional Block Copy with Repacking and Indirection Support

w0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/ 1	ADDR		DIM1	ICNT2/ 3	DIM2	DIM3	RESE RVED	DDIM1	DADDR		DDIM2	DDIM3	DICNT 0/1	DICNT 2/3

11.1.3.3.4.2 EVENT_SIZE: Event Generation Definition

The BCDMA allows for an event to be generated at specified intervals for each TR. As the TR passes through the various loops in the addressing algorithm it will generate an event that then can be routed to other event receivers, such as other channels or interrupts to processors.

Table 11-52. Event Size Encoding

Value	Event Type	When it Fires
0	Completion Event	When the TR is complete and all status for the TR has been received.
1	ICNT1 Decrement	Type 0: When the last data transaction is sent for the TR. Type 1-11: When ICNT1 is decremented
2	ICNT2 Decrement	Type 0 – 1,10-11: When the last transaction is sent for the TR. All Other Types: When ICNT2 is decremented
3	ICNT3 Decrement	Type 0 – 2,10-11: When the last transaction is sent for the TR. All Other Types: When ICNT3 is decremented

11.1.3.3.4.3 TRIGGER_INFO: TR Triggers

The TR allows for two different triggers to be set to allow for the data transfer to be prevented or halted through the process of transferring the data. The triggers are specified by selecting a type of trigger and the size of the transfer that can be allowed for the receipt of a given trigger. The triggers themselves in the BCDMA are collected on a per channel basis and for each of three sources. Anytime the trigger event is received the internal counter is incremented. The trigger event will not be cleared until the specified block has started its transfer and it will **only** clear the triggers that are active.

CAUTION

This does allow for one TR in the channel to use global event 0 and the next TR to use global event 1. If while the first TR is running global event 0 can increment and will decrement each time the TR reaches the specified level. At the same time global event 1 will be incremented whenever it is received but it will not decrement until the next TR runs. If the global event 1 counter reaches overflows then an error event will NOT be generated but the event will be lost.

11.1.3.3.4.4 TRIGGERX_TYPE: Trigger Type

The trigger type sets the value of TR_TRIGX as shown in the addressing algorithm description. The TR_TRIGX value allows for the temporary halting of the TR until the expected event has been received. After the given loop has been entered the selected trigger will be decremented.

11.1.3.3.4.5 TRIGGERX: Trigger Selection

The TR is able to select up to 2 of 3 trigger sources for a given TR. The events can come from the dedicated local event on the BCDMA itself or from two assigned global events that come from the PSI-L interface on the BCDMA. The trigger counters are always enabled so that events can be received prior to the TR getting loaded. The trigger counters are only decremented when the trigger is active and the TR has scheduled the first transfer of the transaction.

11.1.3.3.4.6 Configuration Specific Flags Definition

The configuration specific flags are specific to a given TR type. If a TR type does not require additional flags the field should be filled with 0's. Currently only Types 0-4 and Type 15 support the following configuration specific flags:

Bit	Field	Description
0	**ISA**	Indirect Source Address 0: Source address in TR is a directly usable pointer to the data 1: Source address in TR is a pointer to a 64-bit location that contains the actual pointer to the data
1	**IDA**	Indirect Destination Address 0: Destination address in TR is a directly usable pointer to the data 1: Destination address in TR is a pointer to a 64-bit location that contains the actual pointer to the data
2	**SUPR_EVT**	Suppress Event Output: 0 = Output events will be generated according to FLAGS.EVENT_SIZE field 1 = No output events will be generated for the duration of this TR execution This field is only valid on split and type 15 TRs (Type 0-3,15)
3	**Reserved**	Reserved for Future use.

Bit	Field	Description
6:4	**EOL**	This field is only valid on split TRs (Type 0-3). On source (Read) split TRs, this field specifies whether or not the EOL delimiters should be produced on the Tx PSI-L bus. The encodings of this field for source split TRs is as follows: 0 = SOL/EOL match SOP/EOP 1 = SOL/EOL boundaries are each ICNT0 bytes 2 = SOL/EOL boundaries are each ICNT0*ICNT1 bytes 3 = SOL/EOL boundaries are each ICNT0*ICNT1*ICNT2 bytes 4 = SOL/EOL boundaries are each ICNT0*ICNT1*ICNT2*ICNT3 bytes On destination (Write) split TRs, this field specifies how to handle EOL delimiters when they are encountered on the Rx (write) side of a TR. EOL delimiters can be produced from the Tx (read) side of a block copy operation or from a remotely paired peripheral when operating in split TR mode. The encodings of this field are as follows: 0: Ignore EOL 1: Line length is icnt0 bytes. Clear any remaining ICNT0 bytes and increment ICNT1 by 1 2: Line length is icnt0*icnt1 bytes. Clear any remaining ICNT0/1 bytes and increment ICNT2 by 1 3: Line length is icnt0*icnt1*icnt2 bytes. Clear any remaining ICNT0/1/2 bytes and increment ICNT3 by 1 4: Line length is icnt0*icnt1*icnt2*icnt3 bytes. Move on to next TR 5-7: RESERVED

Bit	Field	Description
7	**EOP**	This TR should generate an EOP on the streaming interface for any downstream packet oriented consumers to denote that a 'packet' of data is complete 0: No EOP flag will accompany the last PSI-L data phase associated with transfers from this TR 1: On egress the DMA will set the EOP flag coincident with transferring the last of the data for this TR. If the TR data does not complete an entire PSI-L data phase then the remaining bytes in the data phase will be skipped and the internal FIFO pointer will be updated to begin packing new data on a new data phase boundary.

11.1.3.3.5 TR Address and Size Attributes

The fields described below all describe the data transfer that needs to be made as described in the Linear Memory Addressing Block Move Algorithm.

11.1.3.3.5.1 ICNT0

The ICNT0 is the number of elements to transfer in the inner loop of the TR. If the TR type does not contain a FMTFLAGS field then this count is assumed to be the number of bytes to transfer. If the FMTFLAGS field is included in the types then the number of bytes to be transferred will be ICNT0 times the Element size rounded up to the nearest byte.

11.1.3.3.5.2 ICNT1

The ICNT1 field is the loop count for the second innermost loop count as defined in the Addressing algorithm.

11.1.3.3.5.3 ADDR

The address location is the initial address that will be accessed at the start of the transfer. All of the dimensions will also be based off of this value. This address can either physical or virtual based upon settings in the DMA channel Configuration register.

While the ADDR field is 64 bits wide, the usable extent of the address is up to 48 bits of absolute offset plus a 4-bit address space selector which indicates 1 of 16 different orthogonal address spaces that the pointer is referencing within. The format of the ADDR field is given as follows:

Bits	Subfield	Description
63:52	Reserved	Reserved

Bits	Subfield	Description
51:48	Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.
47:0	Address	The 48-bit source or source starting address for the transfer. This address is assumed to be a physical address. The actual width implemented for the address field on any given DMA instance may be adjusted to the needs of each specific KSLC SoC. 48 bits is just the maximum size which is envisioned to be supported. Some systems may have address widths as low as 32 or 36 bits. The HW implementation may choose to provide address width configurability in order to reduce costs.

11.1.3.3.5.4 DIM1

This is the offset of the address from the initial address for the first access of the second loop. This will be added to the address from the loop before. This is a signed value so that the address can be both above and below the initial address.

11.1.3.3.5.5 ICNT2

This is the count for the third innermost loop in the addressing algorithm.

11.1.3.3.5.6 ICNT3

This is the count for the outermost loop in the addressing.

11.1.3.3.5.7 DIM2

This is the offset of the address from the initial address to the next address in the third innermost loop. This is a signed value so that the address can be both above and below the previous address.

11.1.3.3.5.8 DIM3

This is the offset of the address from the initial address to the next address in the outermost loop. This is a signed values so that the address can be both above and below the previous address.

11.1.3.3.5.9 DDIM1

This is the offset of the destination address from the initial destination address for the first access of the second loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.10 DADDR

The destination address location is the initial destination address that will be accessed at the start of the transfer. All of the dimensions will also be based off of this value. This address can either physical or virtual based upon settings in the DMA channel Configuration register

While the DADDR field is 64 bits wide, the usable extent of the address on a KSLC system is up to 48 bits of absolute offset plus a 4 bit address space selector which indicates 1 of 16 different orthogonal address spaces that the pointer is referencing within. The format of the DADDR field is given as follows:

Bits	Subfield	Description
63:52	Reserved	Reserved
51:48	Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.
47:0	Address	The 48-bit starting destination address for the transfer. This address is assumed to be a physical address. The actual width implemented for the address field on any given DMA instance may be adjusted to the needs of each specific KSLC SoC. 48 bits is just the maximum size which is envisioned to be supported. Some systems may have address widths as low as 32 or 36 bits. The HW implementation may choose to provide address width configurability in order to reduce costs.

11.1.3.3.5.11 DDIM2

This is the offset of the destination address from the initial destination address for the first access of the third loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.12 DDIM3

This is the offset of the destination address from the initial destination address for the first access of the outer loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.13 DICNT0

This is the number of elements to use in the destination if the TR is repacking the data. This number reflects the number of elements to be transferred.

11.1.3.3.5.14 DICNT1

This is the number of times to execute the second loop to use in the destination transfer.

11.1.3.3.5.15 DICNT2

This is the number of times to execute the third loop to use in the destination transfer.

11.1.3.3.5.16 DICNT3

This is the number of times to execute the fourth loop to use in the destination transfer. The value of DICNT0 x DICNT1 x DICNT2 x DICNT3 must equal ICNT0 x ICNT1 x ICNT2 x ICNT3. If any of the values are zero they are NOT included in the multiplication.

11.1.3.4 Transfer Response Record

Upon completing a TR the BCDMA will send back a TR Response. The BCDMA TR response format is a single 32 bit word as shown in Table 11-53.

Table 11-53. Transfer Request Response Template STATUS FLAGS Field

<table>
<tr><td>31</td><td>24</td><td>23</td><td></td><td></td><td>16</td></tr>
<tr><td colspan="2">CONFIGURATION SPECIFIC STATUS</td><td colspan="4">RESERVED</td></tr>
<tr><td>15</td><td>8</td><td>7</td><td>4</td><td>3</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">STATUS_FIELD</td><td colspan="2">STATUS_TYPE</td></tr>
</table>

Table 11-54. STATUS FLAGS Field Descriptions

Bit	Field	Description
3:0	**STATUS_TYPE**	The completion status of the TR.
7:4	**STATUS_INFO**	Information that is unique based on the STATUS_TYPE returned
15:8	**Reserved**	Reserved for Future use
23:16	**Reserved**	Reserved for Future use
31:24	**Configuration Specific Flags**	These are flag bits that can be specified by the specific BCDMA configuration. These bits will remain undefined in the global TR format to allow for customization requirements that might be required in the specific BCDMA implementation. For BCDMA channels which are capable of interfacing to endpoint peripherals (or via a PDMA) the format of these flags are as follows: 31:28 error_flags – the error_flags field as is provided across PSI-L 27:24 ps_flags – the ps_flags field as is provided across PSI-L

11.1.3.4.1 STATUS Field Definition

The Status field is made up of two sub-fields STATUS_TYPE and STATUS_INFO. A value of 0 means it completed as requested any other value means an error has occurred. The Table below states the legal STATUS_TYPEs and the use of the STATUS_INFO in each case.

11.1.3.4.1.1 STATUS_TYPE Definitions

The STATUS_TYPE field is used to determine what type of status is being returned. Depending on the type of Status it might additionally have information in the STATUS_FIELD to give more details about the specific reason why the status was returned.

Table 11-55. STATUS_TYPE Encoded Values

Value	Error Type	Completion	STATUS FIELD Definition
0	None	Complete	None
1	Transfer Error	None to Partial	CBA Non-Complete Status Received
2	Aborted Error	None to Partial	None
3	Submission Error	None	Submission Error Type
4	Unsupported Feature	None	Feature Type
5	Transfer Exception	Partial	Exception Type
6	Teardown Flush	None	None
7-15	Reserved	Unknown	Reserved

11.1.3.4.1.1.1 Transfer Error

A transfer ERROR occurs anytime that one of the CBA transactions performed by the BCDMA returns a status other than complete. The BCDMA may continue the transfer or may abort the transfer and return back to an IDLE state. Once the transfer is finished (aborted or complete) the BCDMA will send back the TR Response with the STATUS TYPE of Transfer Error. The STATUS FIELD will contain the 3 bit CBA Status field the upper bit specifies if it was a read status (1) or a write status (0).

11.1.3.4.1.1.2 Aborted Error

An aborted error occurs if the PSI-L interface asserts the drop signal prior to the completion of the TR. The BCDMA will return back to an IDLE state and send back the TR Response with the STATUS TYPE. If the BCDMA receives a transfer error after receiving the abort the transfer error should be reported instead of the Abort Error.

11.1.3.4.1.1.3 Submission Error

A submission error is returned for a TR that is received that cannot be run. The STATUS_INFO field specifies the type of submission errors.

Table 11-56. Submission Error STATUS_INFO Encodings

Value	Submission Error Type
0	ICNT0 was 0
1	Channel FIFO was full when TR received

Table 11-56. Submission Error STATUS_INFO Encodings (continued)

Value	Submission Error Type
2	Channel is not owned by the submitter. Either CC submitting to Direct or Direct submitting to a CC channel
3	Bad descriptor type
4	Illegal TR
5-15	Reserved

11.1.3.4.1.1.4 Unsupported Feature

An unsupported feature error is returned for a TR that is received that cannot be run because it specifies a feature that is optional and not supported by the BCDMA that received the TR. The STATUS FIELD specifies the feature that was not supported. If it specifies multiple features that were not supported the BCDMA implementation can determine which type it wants to return.

Table 11-57. Unsupported Feature STATUS_INFO Encodings

Value	Submission Error Type
0	TR Type not supported
1	STATIC not supported
2	EOL not supported
3	CONFIGURATION SPECIFIC not supported
4	AMODE not supported
5	ELTYPE not supported
6	DFMT not supported
7	SECTR not supported
8	AMODE SPECIFIC Field not supported
9-15	Reserved

11.1.3.4.1.1.5 Transfer Exception

A transfer exception is returned for a TR that completed but experienced a known exception during reception. The STATUS_INFO field specifies the type of transfer exception that was encountered.

Table 11-58. Transfer Exception STATUS_INFO Encodings

Value	Transfer Exception Type
0	EOP on incoming data stream was encountered prematurely (short packet)
1	EOP on incoming data stream was encountered late (long packet)

Table 11-58. Transfer Exception STATUS_INFO Encodings (continued)

Value	Transfer Exception Type
2-15	Reserved

11.1.3.4.1.1.6 Teardown Flush

Split mode BCDMA Rx channels (write channels) can respond with a teardown flush in the case that they have received a teardown message, all data has been transferred , and TRs have been prefetched (in anticipation of more data being received). In this case, the BCDMA will simply return the prefetched TR to the completion queue with the status type set to teardown flush.

11.1.3.5 Channels

Each DMA controller instance contains one or more channels. A channel represents a single thread of strongly ordered operations whose purpose is to move data from one interface to another. Operations between channels are orthogonal and have no assumption of ordering but operations within a channel must be completed in order. The DMA controller uses time division multiplexing to allow work from channels to momentarily use shared data transfer units and datapaths.

11.1.3.6 Flows

Each DMA channel will provide one or more flows which allow communication with one or more SW hosts. Each flow contains a single queue pair implemented within a shared circular buffer (ring) in memory. One queue provides uni-directional communication from SW to the DMA while the other queue provides uni-directional communication from the DMA back to SW. Flows are intended to allow traffic which is produced or consumed by a different Host SW process or traffic which is on different priorities to share a single physical DMA channel. A DMA channel will perform time division multiplexing between flows on specific work boundaries. Once a channel is in work on a specific flow, that entire unit of work will be completed before allowing work from a different flow to begin.

11.1.3.7 Queues

Queues are used to hold either values or references that need to be passed between SW and HW components in the system. Queues are implemented in the PKTDMA and BCDMA modules using memory mapped rings. Each ring is comprised of a single contiguous memory block which contains an array of elements. Each element is 8 bytes. The size of the ring is selectable from 1 entry up to 64K entries with single entry granularity. Each ring is used to implement a forward and a reverse queue which share the same data elements but which have independent pointers and occupancies. The forward queue is used to pass work from SW to HW and the reverse queue is used to pass completed work back from HW to SW. A doorbell MMR is provided per ring to allow SW to add elements to the forward queue. A separate doorbell MMR is provided per ring to allow SW to acknowledge the popping of elements from the reverse queue. An occupancy MMR is provided for the reverse queue so that SW can know how many entries are currently completed. Entries are returned on the reverse queue in the exact same order and in the exact same index as the work was provided on the forward queue and because of this, the DMA controllers do not actually modify the ring entry for completion operations (the only exception being for acknowledgement of a teardown operation). Completion is indicated by incrementing of the reverse occupancy only.

11.1.3.7.1 Queue Types

11.1.3.7.1.1 Transmit Queues

Tx channels use packet queues referred to as “transmit queues” to store the packets that are waiting to be transmitted. Tx Queues only pass a pointer to a descriptor. For the PKTDMA, Tx Queues contain pointers to Host descriptors. For the BCDMA, pass Tx Queues contain a pointer to a TR packet descriptor. Transmit Queues are implemented as the forward queue on the shared ring structure for a Tx flow.

11.1.3.7.1.2 Transmit Completion Queues

Tx channels also use packet queues referred to as “transmit completion queues” to return packets to the host after they are transmitted. A Tx Completion Queue is provided for each Tx Queue. The DMA controllers do not actually write anything back to completion queues (except for a teardown acknowledgement) but instead just increment the reverse occupancy. Transmit completion queues are implemented as the reverse queue on the shared ring structure for a Tx flow.

11.1.3.7.1.3 Free Descriptor / Buffer Queues

Free descriptor/buffer queues pass an empty list of pre-chained descriptors, each pointing to a single buffer, from SW to the DMA to use for receiving incoming packets. Free Descriptor/Buffer Queues are implemented as the forward queue on the shared ring structure for an Rx flow.

11.1.3.7.1.4 Receive Queues

Rx queues pass a packet which has been received from the DMA back to the SW. Receive queues are implemented as the reverse queue on the shared ring structure for an Rx flow.

11.1.3.7.1.5 Ring Based Queues Implementation

Work packets which are stored in a queue are shown in the following diagram:

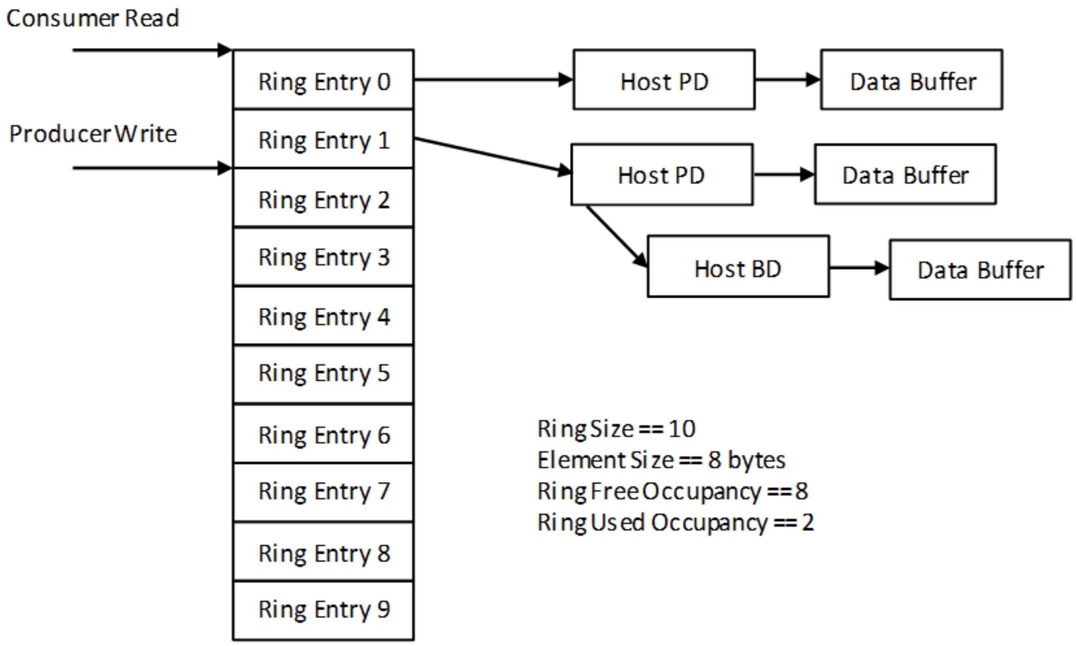

Figure 11-3. Ring Based Queue Structure

11.1.4 Operational Description

11.1.4.1 Resource Allocation

Rings, memory, interrupts, DMA channels, and flow table entries are shared resources within the data movement architecture and their ownership and use must be managed in order to provide stable, safe, and secure operation. The DMSS provides channelized firewalls which can be used to protect arrayed resources (like rings, channel control MMRs, etc.) from unwanted/unauthorized use as well as restricted access to the firewall configurations themselves. It is outside the scope of this document to define how the resource management system functions but it is assumed that all of these resources are isolate-able and secure-able.

11.1.4.2 PKTDMA/BCDMA - Ring Operation

11.1.4.2.1 Queue Initialization

The base address and size for each ring must be initialized via the provided MMRs prior to using the ring. Ring initialization is typically done only on channel / flow setup as once initialized the rings can be used indefinitely.

11.1.4.2.2 Queueing Entries

Entries can only be queued by SW onto the forward queue of a ring. To queue an entry the producer will write the entry contents (typically a pointer to the Packet Descriptor or a TR) to the memory location pointed to by the current write pointer and will decrement its internally maintained free entry occupancy. After the producer has confirmed that the data has actually landed it memory, it will then write to the forward doorbell register (RINGRT[a]_RT_FDB) for the ring to increment the pending forward occupancy count for the ring.

More than one entry can be queued with a single doorbell write as the entry count in the doorbell write indicates how many entries have been queued.

11.1.4.2.3 De-queueing Entries

Entries can only be de-queued by SW from the reverse queue of a ring. The consumer (entity which is going to de-queue an entry from the ring) maintains a current read pointer for each ring it controls. To de-queue an entry the consumer will read the occupancy from the reverse occupancy register (RINGRT[a]_RT_ROCC) and will then read the entry contents from the memory location pointed to by the current read pointer. The consumer will then write a decrement value to the reverse doorbell register (RINGRT[a]_RT_ROCC) for the ring to decrement the waiting occupancy count for the reverse queue within the ring and will increment its internally maintained free entry occupancy for the ring.

11.1.4.3 PKTDMA/BCDMA - Output Event Generation

Each channel and flow within a DMA has the ability to generate specific types of events which can be routed to the IA in the system and from there re-routed to any event consumer. Events are output from the DMA controllers using a simple integer encoding. Up to 4 events can be generated from any given channel but only event types which have functional value are supported on each specific type of channel. The DMA channel event types are listed as follows:

Table 11-59. Per-Channel/Flow Event Support and Encoding

Name	Description	Per	BCDMA BC	BCDMA Tx	BCDMA Rx	PKTDMA Tx	PKTDMA Rx
Ring Entry Zero/Non-zero	Asserts an up event anytime the ring transitions to a non-zero occupancy / teardown state. Asserts a down event anytime the ring transitions to a zero occupancy / teardown state.	Flow	X	X	X	X	X

Table 11-59. Per-Channel/Flow Event Support and Encoding (continued)

Name	Description	Per	BCDMA BC	BCDMA Tx	BCDMA Rx	PKTDMA Tx	PKTDMA Rx
Channel Error	Asserts an up event anytime an error occurs on the channel. Asserts a down event when the channel error bit is cleared.	Channel	First flow in channel only	First flow in channel only	First flow in channel only	First flow in channel only	First flow in channel only
Rx Starvation	Asserts an up event when starvation occurs on a flow. Asserts a down event when entries are added to the ring for that flow.	Flow					First flow in channel only
RX Flow FW Error	Asserts an up event when a flow id arrives on the RX interface that is not between the flowid_start and flowid end values for the channel. Asserts a down event when the RX Flow ID Firewall Status Register pend bit is cleared	Pktdma					X
Data Events	Asserts an up event when the selected loop counter has decremented. If the suppress event bit is not set in the TR	Channel	X	X	X		

Each BCDMA/PKTDMA instance will provide an event transport-lane (ETL) interface to pass outgoing events. The index field on this ETL will be calculated based on the event type and channel or flow offset. Each PKTDMA or BCDMA instance is configured with base values to which a channel or flow index is added for each type of event which can be generated. These base index values are listed in the specification for that specific instantiation of each DMA and are named as follows:

Table 11-60. BCDMA/PKTDMA Event Base Index Parameters

DMA	Event Base Parameter Name	Function	Offset
PKTDMA	tcomp_evtbase	Base index for Tx flow reverse ring completion events	Tx flow number
	rcomp_evtbase	Base index for Rx flow reverse ring completion events	Rx flow number
	terr_evtbase	Base index for Tx channel error events	Tx channel number
	rerr_evtbase	Base index for Rx channel error events	Rx channel number
	rstarve_evtbase	Base index for Rx flow starvation events	Rx flow number
	rflowfw_evtbase	Base index for Rx Flow Firewall event	None
BCDMA	tcomp_evtbase	Base index for split Tx flow reverse ring completion events	Tx flow number
	rcomp_evtbase	Base index for split Rx flow reverse ring completion events	Rx flow number
	bcomp_evtbase	Base index for normal Block Copy flow reverse ring completion events	BC flow number
	terr_evtbase	Base index for split Tx channel error events	Tx channel number
	rerr_evtbase	Base index for split Rx channel error events	Rx channel number
	berr_evtbase	Base index for normal Block Copy channel error events	BC channel number
	tdcomp_evtbase	Base index for Tx channel TR data completion events	Tx channel number
	rdcomp_evtbase	Base index for Rx channel TR data completion events	Tx channel number
	bdcomp_evtbase	Base index for Block Copy channel TR data completion events	BC channel number

Example:

The producer event map is set up so that the Tx flows from a PKTDMA instance are to start at 64 and proceed upward from there. The tcomp_evtbase for that PKTDMA instance is set to 64. In this configuration, the reverse ring entry completion event for flow 0 will produce an event on index 64, flow 1 will produce an event on index 65, etc. The terr_evtbase for the same PKTDMA instance is set to 128. In this configuration, error events for channel 2 would produce events with an index of 130.

11.1.4.4 PKTDMA - Transmit Channel Setup

This section describes the setup procedure for Tx channels within the PKTDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel's Tx Port DMA State. The host initializes the channel Tx Port DMA State by configuring all of the Tx flow entries for the channel and then writing to the Tx Channel Configuration Register A (TCHAN[a]_TCFG). The Host may choose to write the enable bit in the Tx Channel Configuration Register A (TCHAN[a]_TCFG) at the same time or after it has written all of the channel parameters but note that every write to the Tx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a Transmit channel has been set up, packets can be added to the Queues for the channel to begin the transmit operation. The following sections describe how the transmit operations are performed for the various descriptor types.

11.1.4.5 PKTDMA - Transmit Channel Pause

Setting the tx_pause bit in the Tx Channel N Realtime Control Register (<TCHANRT[a]_TRT_CTL > [29] TX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potential underrun/overrun conditions from a downstream data sink or upstream data source.

11.1.4.6 PKTDMA - Transmit Channel Teardown

This section describes the teardown procedure for internal Tx channels within the PKTDMA. A Tx channel teardown is initiated by the host by writing the tx_teardown bit in the Tx Channel N Realtime Control Register (<TCHANRT[a]_TRT_CTL > [30] TX_TEARDOWN).

Once the host has written the tx_teardown bit, the PKTDMA will do the following:

1. Stops performing any additional descriptor fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/TR fetch has already been performed.
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.
4. Clears the channel enable in the Tx Channel N Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
7. If the current Tx reverse ring occupancy is 0, issues an Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current TX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
9. The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not.

The Host can determine that a teardown is complete by using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel

2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.7 PKTDMA - Transmit Operation

After a channel has been set up it can begin to be used to transmit packets. Packet transmission involves the following steps:

1. The Host is made aware of one or more chunks of data in memory that need to be transmitted as a packet. This may involve directly sourcing data from the Host or it may involve data which has been forwarded from another data source in the system.
2. The Host allocates and populates a host packet descriptor. The host will initialize the following fields within the packet descriptor:
   a. Descriptor Type (set to Host).
   b. Packet Length indicating the total number of bytes that are to be read from all of the buffers for this packet.
   c. Source Tag.
   d. Destination Tag.
   e. Packet Type.
   f. Any protocol specific flags for the given packet type.
   g. Buffer Pointer with the byte aligned address of the first chunk of buffer data.
   h. Buffer Length with the number of bytes in the first chunk of buffer data.
   i. The Next Descriptor Pointer with the 16-byte aligned address of the next descriptor in this packet. If this is the last chunk of data in the packet, this field must be set to zero.
   j. Any protocol specific descriptor sections that are required for the given packet type or system configuration.
3. The Host allocates and populates host buffer descriptors as necessary to point to any remaining chunks of data that belong to this packet. The host will initialize the following fields within the host buffer descriptor:
   a. Buffer Pointer with the byte aligned address of the given chunk of buffer data.
   b. Buffer Length with the number of bytes in the given chunk of buffer data.
   c. The Next Descriptor Pointer with the 16-byte aligned address of the next descriptor in this packet. If this is the last chunk of data in the packet, this field must be set to zero.
4. The Host writes queues the packet onto one of the Transmit Queues for the desired DMA channel. Channels may provide more than one Tx Queue (if more than 1 flow is provided) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller / scheduler implementation.
5. The PKTDMA internally generates a level sensitive status signal for the queue which indicates if any packets are currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
6. The PKTDMA Tx engine is eventually brought into context for the corresponding channel and begins to process the packet.
7. The PKTDMA reads the packet descriptor pointer from the memory mapped ring for that channel/flow.
8. The PKTDMA reads the packet descriptor from memory.
9. The PKTDMA empties each buffer in sequence by transmitting the contents in one or more block data moves. The size of these blocks is application specific. The PKTDMA module specification is intended to document the block size used by a given implementation. As each buffer is emptied, the PKTDMA will read the next buffer descriptor to obtain the pointer and size of the data buffer as well as the pointer to the next descriptor in the chain.
10. When all data for the packet has been transmitted as specified in the packet size field, the DMA will increment the occupancy of the reverse queue (Tx Completion Queue).
11. After the occupancy is incremented, the PKTDMA will indicate the status of the Tx Completion Queue by sending an up event.

12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_STATUS_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the PKTDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.
15. The PKTDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS) and potentially de-assert the interrupt line.

11.1.4.8 PKTDMA - Receive Free Descriptor / Buffer Queue Setup

The Host is ultimately responsible for providing all of the free descriptors and buffers that the port uses as it receives packets. Each entry on the Rx Free Descriptor/Buffer Queue consists of one or more descriptors chained together with each descriptor also pointing to a single contiguous buffer. Each entry on the Rx Free Descriptor/Buffer queue is intended to receive one packet of data. All chaining of descriptors within a packet is performed prior to placing the Rx resources onto the free queues.

Before the Host adds each Rx buffer descriptor chain to the queue, it must first initialize the Rx buffer descriptor values as follows:

- Write the Buffer Pointer with the byte aligned address of the buffer data
- Write the Buffer Size
- Write the next descriptor pointer to the next descriptor in the chain (non-eop) or to 0x0 (eop)

All other fields in the Descriptor do not need to be initialized as they will be overwritten by the Port on reception.

11.1.4.9 PKTDMA - Receive Channel Setup

After a reset or a previous teardown operation but before receiving packets on a channel the host must initialize the channel’s Rx Port DMA State. The host initializes the channel Rx Port DMA State by writing to the Rx Channel Configuration Registers. The Host may choose to write the enable bit in the Rx Global Channel Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Rx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

11.1.4.10 PKTDMA - Receive Channel Teardown

An Rx channel teardown is intended to be initiated at the data source (the source thread). Initiation is commanded by the host by writing the teardown bit in the PSI-L source thread register DMASS0_PKTDMA_0_RCHANRT_ctl_j . This will cause the source of the data to gracefully terminate any packet that is in flight and send a PSI-L data phase with the tdown signal asserted. When the PKTDMA receives a data phase with the tdown attribute asserted it will immediately set the internal rx_teardown bit in the Rx Channel N Realtime Control Register (<RCHANRT[a]_RRT_CTL> [30] RX_TEARDOWN).

Once a teardown has been initiated, the PKTDMA will do the following:

1. Completes any packets normally which may be pending in the ingress port buffers (what the port considers as pending packets is application specific).
2. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL> [31] RX_ENABLE)**>**.
3. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
4. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register to indicate that a teardown has completed (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE).
5. If the current Rx reverse ring occupancy is 0, issues an Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

6. If the current RX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not. The normally intended method of issuing a teardown on a packet mode channel is to initiate the teardown at the remote PSI-L data source and allow it to flow into the PKTDMA. If that is not possible, the host may write the rx_teardown bit directly to a 1.

The Host determines that a teardown is complete by using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.11 PKTDMA - Receive Channel Pause

Setting the rx_pause bit in the Rx Channel N Control Register (<RCHANRT[a]_TRT_CTL> [29] RX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potential underrun/overrun conditions from a downstream data sink or upstream data source.

11.1.4.12 PKTDMA - Receive Operation

When packet reception begins on a given channel, the port will begin by fetching the descriptor and buffer from the ring for the channel / flow. If the SOP Buffer Offset in the Rx Flow Table entry is nonzero, then the port will begin writing data after the offset number of bytes in the SOP buffer. The port will then continue filling that buffer and will fill additional descriptors + buffers as needed using the pre-linked buffers in the packet.

A detailed summary is as follows:

1. Host allocates, populates, and places pointers to free descriptor/buffer structures onto Rx Free Descriptor/ Buffer Queues
2. PKTDMA fetches packet descriptor pointer from forward queue of ring for specified channel.
3. PKTDMA reads the packet descriptor to obtain the packet info, buffer pointer, buffer size, and next descriptor pointer.
4. PKTDMA fills the buffer with received data

If packet is not complete and the rx_chan_type field in the Rx Channel Configuration Register (<RCHAN[a]_RCFG> [19:16] RX_CHAN_TYPE) is set to 2 (Normal Rx Host Mode). The machine will proceed to step 5 and will repeat steps 5-6 until all packet data is received at which point the Rx engine proceeds to step 8. If the rx_desc_type is set to 3 (Single Buffer Packet Host Mode) the Rx engine will proceed directly to step 7 regardless of whether or not an end of packet terminator has been reached on the incoming data stream. The current packet will be completed following the sequence through step 12 and a new packet will be started back at step 1.

5. PKTDMA fetches next buffer descriptor using next descriptor pointer obtained from previous descriptor.

6. PKTDMA fills the buffer with received data.

The PKTDMA performs the following operations when the entire packet has been received:

7. PKTDMA writes the packet descriptor to memory. This includes the following fields:

a. Descriptor Type (set to Host)

b. Packet Length indicating the total number of bytes that are to be read from all of the buffers for this packet.

c. Source Tag

d. Destination Tag

e. Packet Type

f. Any protocol specific flags for the given packet type

g. Any protocol specific words that are required for the given packet type

h. Extended Packet Information (optional)

8. PKTDMA increments the occupancy of the reverse queue for the channel / flow.

9. Once the occupancy is incremented it will send an up event to the Interrupt Aggregator

10. The Interrupt Aggregator upon receiving the up event will set the appropriate bit in the Interrupt Status Register (VINT[a]_STATUS_SET) indicated by the interrupt mapping table which will cause an interrupt to be asserted to the Host

11.The Host will pop the packet pointer from the Rx Queue by reading the ring contents and then pushing a decrement to the reverse occupancy for the ring.

12. If the pop causes the queue to become empty, the PKTDMA will send a down event to the Interrupt Aggregator thus causing the associated bit to be cleared and also potentially clearing the interrupt to the Host.

11.1.4.13 BCDMA - Block Copy Channel Setup

This section describes the setup procedure for channels within the BCDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel's Port DMA State. The host initializes the channel Port DMA State by initializing all of the channel flow entries and then writing to the Channel Configuration Register A (CHANRT[a]_TRT_CTL). The Host may choose to write the enable bit in the Channel Configuration Register A (<CHANRT[a]_TRT_CTL> [31] TX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a channel has been set up, packets can be added to the Queues for the channel to begin the copy operation.

For general purpose block copy channels, only the Tx DMA configuration, flow, and realtime registers will be present. For split mode channels, separate Tx and Rx configuration, flow, and realtime registers are provided. In all cases, configuration of all fields must be completed before a channel is enabled.

11.1.4.14 BCDMA - Block Copy Channel Pause

Setting the pause bit in the Channel N Control Register (<CHANRT[a]_TRT_CTL> [29] TX_PAUSE]) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.15 BCDMA - Block Copy Channel Teardown

This section describes the teardown procedure for generic block copy channels within the BCDMA. A channel teardown is initiated by the host by writing the teardown bit in the Channel N Realtime Control Register (<CHANRT[a]_TRT_CTL> [30] TX_TEARDOWN). When the host initiates teardown, it can choose to perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the forced_teardown bit in the Channel N Realtime Control Register (<CHANRT[a]_TRT_CTL> [28] TX_FORCED_TEARDOWN).

If the forced_teardown bit is clear, a normal teardown has been initiated. In this case, the BCDMA will do the following:

1. Stops performing any additional fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/data fetch has already been performed
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.

4. Clears the channel enable in the Channel N Global Configuration Register (<CHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the BC Flow Reverse Ring Occupancy register to indicate that a teardown has completed.
7. If the current BC reverse ring occupancy is 0, issues an BC reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current BC Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
9. If the forced_teardown bit is set, a destructive teardown has been initiated. In this case, the BCDMA will do the following:
   a. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
   b. Completes any packets which have been fetched with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation).
   c. Clears the channel enable in the Channel Global Configuration Register.
   d. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
   e. Sets bit 31 of the BC Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
   f. If the current BC reverse ring occupancy is 0, issues an BC reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively transferring data or not.

The Host determines that a teardown using either of the following methods:

a. Periodically polling the teardown and enable bits for the channel
b. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

Note that the teardown message will actually be written to the next available location in the ring following the last completed packet.

11.1.4.16 BCDMA - Block Copy Operation (TR Packet)

Packet transmission in TR Packet mode involves the following steps:

1. The Host allocates and populates a type 15 TR packet descriptor. The host will initialize the following fields within the packet descriptor:
   a. Descriptor Type (set to TR)
   b. Reload Enable to 1 if looping is required, otherwise 0
   c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
   d. Last Entry to TR count minus 1
   e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
   f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Transmit Queues for the desired BCDMA channel. Channels may provide more than one Queue (1 queue per provided flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller/scheduler implementation.
3. The BCDMA internally provides a level sensitive status signal for the queue which indicates if any work is currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.

4. The DMA controller is eventually brought into context for the corresponding read channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller sequentially empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves. As a TR is read from the descriptor, it is stored in the internal state of the DMA channel until it is completed.
8. All of the data transfers specified in a TR will be completed as a series of reads followed later on by a set of corresponding writes (which may or may not be the same size based on the parameters in the block copy TR).
9. The BCDMA will wait until write status returns for the final write operation that was initiated for each TR. When the final write status is returned within each TR, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.
10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the BCDMA will increment the reverse occupancy for the channel/flow.
11. After the occupancy is incremented, the BCDMA will indicate the status of the Tx Completion Queue by sending an up event.
12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_STATUS_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the BCDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.
15. The BCDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS) and potentially de-assert the interrupt line

11.1.4.17 BCDMA - Block Copy Error/Exception Handling

There are 3 specific errors which may be encountered during generic block copy operation and which are trapped by the BCDMA. The following table lists the errors and how the BCDMA will process them:

Table 11-61. BCDMA Generic Block Copy Mode Error / Exception Handling

Condition	Pauses Channel	Error Flag Set in Channel	Data Transfer	TR Flush	Outputs Transfer Events
TR null icnt0	Selectable[1]	Yes	No	Just that TR	No
Unsupported TR Type	Selectable[1]	Yes	No	Just that TR	No
Bus Errors	Selectable[1]	Yes	Yes	No	Yes

[1] If pause_on_error bit is set in channel configuration

11.1.4.17.1 Null Icnt0 Error

The icnt0 parameter in a TR is never allowed to be 0 as this would cause zero byte count transactions to be issued on the bus and is unproductive wrt completion of any useful work. The Tx engine in the BCDMA will trap any TR for which the icnt0 is zero and will immediately return a transfer response with the TR icnt0 error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.17.2 Unsupported TR Type

If a TR is provided to a channel which is of a type which is not supported by the channel, the Tx engine in the BCDMA will trap that TR and immediately return a transfer response with the Unsupported TR error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.17.3 Bus Errors

If a bus error is encountered during transmit the BCDMA will log the error by asserting the tx_error bit for the channel (and optionally sending an error event if enabled) but the DMA will continue to attempt to complete the transfer using the returned (and potentially incorrect) data.

11.1.4.18 BCDMA - Split Transmit Channel Setup

This section describes the setup procedure for split Tx channels within the BCDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel's Tx Port DMA State. The host initializes the channel Tx Port DMA State by configuring all of the Tx flow entries for the channel and then writing to the Tx Channel Configuration Register A (TCHANRT[a]_TRT_CTL). The Host may choose to write the enable bit in the Tx Channel Configuration Register A (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Tx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a Transmit channel has been set up, packets can be added to the Queues for the channel to begin the transmit operation. The following sections describe how the transmit operations are performed for the various descriptor types.

11.1.4.19 BCDMA - Split Transmit Operation Pause

Setting the pause bit in the Channel N Control Register (<TCHANRT[a]_TRT_CTL> [29] TX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.20 BCDMA - Split Transmit Channel Teardown

This section describes the teardown procedure for split mode Tx channels within the BCDMA. A Tx channel teardown is initiated by the host by writing the tx_teardown bit in the Tx Channel N Realtime Control Register (<TCHANRT[a]_TRT_CTL> [30] TX_TEARDOWN). When the host initiates teardown, it can choose to perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the tx_forced_teardown bit in the Tx Channel N Realtime Control Register (<TCHANRT[a]_TRT_CTL> [28] TX_FORCED_TEARDOWN) .

If the tx_forced_teardown bit is clear, a normal teardown has been initiated. In this case, the DMA will do the following:

1. Stops performing any additional descriptor fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/TR fetch has already been performed
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.
4. Clears the channel enable in the Tx Channel N Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
7. If the current Tx reverse ring occupancy is 0, issues a Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current TX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.

9. If the tx_forced_teardown bit is set (only valid on BCDMA), a destructive teardown has been initiated. In this case, the BCDMA will do the following:

1. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
2. Completes any packets which have been prefetched with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation).
3. Clears the channel enable in the Tx Channel Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
4. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
5. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
6. If the current Tx reverse ring occupancy is 0, issues a Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not.

The Host determines that a teardown using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (RINGRT[a]_RT_ROCC) for the channel.

11.1.4.21 BCDMA - Split Transmit Operation (TR Packet)

Packet transmission in TR Packet mode involves the following steps:

1. The Host allocates and populates a TR packet descriptor. The host will initialize the following fields within the packet descriptor:
    a. Descriptor Type (set to TR)
    b. Reload Enable to 1 if looping is required, otherwise 0
    c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
    d. Last Entry to TR count minus 1
    e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
    f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Transmit Queues for the desired BCDMA channel. Channels may provide more than one Queue (1 queue per provided flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller/ scheduler implementation.
3. The BCDMA internally provides a level sensitive status signal for the queue which indicates if any work is currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
4. The DMA controller is eventually brought into context for the corresponding read channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller sequentially empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves. As a TR is read from the descriptor, it is stored in the internal state of the DMA channel until it is completed.
8. All of the data transfers specified in a TR will be completed as a series of reads.
9. The BCDMA will wait until data returns for each read operation that has been initiated. When the final read operation is returned within each TR, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.

10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the BCDMA will increment the reverse occupancy for the channel / flow.
11. After the occupancy is incremented, the BCDMA will indicate the status of the Tx Completion Queue by sending an up event.
12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_ENABLE_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the BCDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.
15. The BCDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS)and potentially de-assert the interrupt line.

11.1.4.22 BCDMA - Split Transmit Error / Exception Handling

There are 3 specific errors which may be encountered during Tx split operation and which are trapped by the BCDMA. The following table lists the errors and how the BCDMA will process them:

Table 11-62. BCDMA Tx Error / Exception Handling

Condition	Pauses Channel	Error Flag Set in Channel	Data Transfer	TR Flush	Outputs Transfer Events
TR null icnt0	Selectable[1]	Yes	No	Just that TR	No
Unsupported TR Type	Selectable[1]	Yes	No	Just that TR	No
Bus Errors	Selectable[1]	Yes	Yes	No	Yes

[1] If pause_on_error bit is set in channel configuration

11.1.4.22.1 Null Icnt0 Error

The icnt0 parameter in a TR is never allowed to be 0 as this would cause zero byte count transactions to be issued on the bus and is unproductive wrt completion of any useful work. The Tx engine in the BCDMA will trap any TR for which the icnt0 is zero and will immediately return a transfer response with the TR icnt0 error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.22.2 Unsupported TR Type

If a TR is provided to a channel which is of a type which is not supported by the channel, the Tx engine in the BCDMA will trap that TR and immediately return a transfer response with the Unsupported TR error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.22.3 Bus Errors

If a bus error is encountered during transmit the BCDMA will log the error by asserting the tx_error bit for the channel (and optionally sending an error event if enabled) but the DMA will continue to attempt to complete the transfer using the returned (and potentially incorrect) data.

11.1.4.23 BCDMA - Split Receive Channel Setup

After a reset or a previous teardown operation but before receiving packets on a channel the host must initialize the channel's Rx Port DMA State. The host initializes the channel Rx Port DMA State by writing to the Rx Channel Configuration Registers. The Host may choose to write the enable bit in the Rx Global Channel Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Rx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

11.1.4.24 BCDMA - Split Receive Channel Pause

Setting the pause bit in the Channel N Control Register (<RCHANRT[a]_RRT_CTL > [29] RX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.25 BCDMA - Split Receive Channel Teardown

An Rx channel teardown is intended to be initiated at the data source (the source thread).
Initiation is commanded by the host by writing the teardown bit in the PSI-L source thread register DMASS0_BCDMA_0_RCHANRT_ctl_j. This will cause the source of the data to gracefully terminate any packet that is in flight and send a PSI-L data phase with the tdown signal asserted. When the BCDMA receives a data phase with the tdown attribute asserted it will immediately set the internal rx_teardown bit in the Rx Channel N Realtime Control Register (<RCHANRT[a]_RRT_CTL > [30] RX_TEARDOWN).

Upon seeing the rx_teardown bit asserted the port can perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the rx_forced_teardown bit in the Rx Channel N Realtime Control Register (<RCHANRT[a]_RRT_CTL > [28] RX_FORCED_TEARDOWN).

If the rx_forced_teardown bit is clear, a normal teardown has been initiated. In this case, the BCDMA will do the following:

1. Stops performing any additional prefetches for the channel (TR mode channels)
2. Completes any packets normally which may be pending in the ingress port buffers (what the port considers as pending packets is application specific).
3. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE).
4. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
5. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
6. If the current Rx reverse ring occupancy is 0, issues an Rx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
7. If the current RX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
8. If the rx_forced_teardown bit is set, a destructive teardown has been initiated. In this case, the BCDMA will do the following:

    a. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
    b. Completes any packets which may be pending in the ingress port buffers with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation) . Packets will be drained from the Rx FIFO either using ‘null’ write transfers or real transfers and the Packet Descriptors will be returned with an accurate accounting of actual bytes transferred.
    c. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE).
    d. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
    e. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
    f. If the current Rx reverse ring occupancy is 0, issues an Rx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not. The normally intended method of issuing a teardown on a packet mode channel is to initiate the teardown at the remote PSI-L data source and allow it to flow into the BCDMA. If that is not possible, the host may write the rx_teardown bit directly to a 1.

The Host determines that a teardown using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.26 BCDMA - Split Receive Operation (TR Packet)

Packet reception in TR Packet mode involves the following steps:

1. The Host allocates and populates a TR packet descriptor. The host will initialize the following fields within the packet descriptor:
    a. Descriptor Type (set to TR)
    b. Reload Enable to 1 if looping is required, otherwise 0
    c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
    d. Last Entry to TR count minus 1
    e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
    f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Rx TR Queues for the desired BCDMA channel. Channels may provide more than one Rx TR Queue (one per flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller / scheduler implementation.
3. The Ring Accelerator provides a level sensitive status signal for the queue which indicates if any packets are currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
4. The DMA controller is eventually brought into context for the corresponding channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves.
8. All of the data transfers specified in a TR will be completed as a series of writes and a Transfer Response will be returned indicating the completion and status of the transfer.
9. The BCDMA will wait until Transfer Responses have been returned for each Transfer Request that it issued. As each Transfer Response is returned, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.
10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the DMSS will write the pointer to the packet descriptor to the queue specified in the return queue number fields of the packet descriptor.
11. After the Packet Descriptor pointer has been written, the Ring Accelerator indicates the status of the Rx Completion Queues to other ports / processors / prefetcher blocks using events sent to the Interrupt Aggregator. These events are then converted into standard interrupts.

11.1.4.27 BCDMA - Split Receive Error / Exception Handling

Several types of errors/exceptions may be encountered during reception of split Rx data. The following table outlines the various errors and exceptions that can occur:

Table 11-63. Rx Error / Exception Handling

Condition	Channel Type	Severity	Pauses Channel	Error Flag Set	Data Transfer	Data Flush	TR Flush	Event Output
Descriptor Starvation	All Packet	Exception	No	No	Option	Option	-	No
Protocol Errors	All Packet	Info	No	No	Normal	No	-	No
Drop	Host – normal	Exception	No	No	Partial[3]	Until EOP	-	No
EOP Asserted Late (Long Packet)	BCDMA – single ended	Exception	No	No	Partial	Excess	No	Yes
TR null icnt0	All BCDMA	Error	Selectable[3]	Yes	No	No	Just that TR	No
Unsupported TR Type	All BCDMA	Error	Selectable[3]	Yes	No	No	Just that TR	No

[1] If pause_on_error bit is set in channel configuration

[2] If destination event index in channel Error Output Event Steering register is not 0xFFFF

[3] Data will not be transferred after drop is detected. All data after that point is guaranteed to be flushed and some data prior to the exact data phase on PSI-L where drop was asserted may also be flushed since data is constantly accumulated so it can be transferred in chunks.

[4] EOP will only occur when in single buffer mode when teardown is initiated. The data is a (never ending) stream. Drop is never supposed to be asserted during this mode of operation.

[5] EOP on TR is true for all PBV TRs, the final TR in a PBR, or if the user specified EOP in the TR flags

11.1.4.27.1 PKTDMA Exception Conditions

There are a few cases which can occur when processing incoming packets which are not considered errors but which will require handling in order to avoid locking up the PKTDMA engines.

Packet mode channel exceptions include:

- Descriptor Starvation
- Protocol Errors
- Dropped Packets
- Long Packets

11.1.4.27.1.1 Descriptor Starvation

Descriptor starvation occurs when the Port needs to fetch a free descriptor fromthe RX ring and none are available. When the port detects that descriptor starvation has occurred it will react based on the value of the rx_error_handling bit which was programmed into the Rx Flow N Configuration Register A (<RFLOW[a]_RFA> [28] RX_ERROR_HANDLING).

If the rx_error_handling bit is cleared:

- The Port will increment an internal per-channel starvation counter and will then flush the packet.

If the rx_error_handling bit is set:

- The Port will assert a RX descriptor starvation event (which may cause an interrupt to the Host) and will then wait for the doorbell for the selected flow to be written with a positive value. Note that the intention is that the port will wait for an entry to be added to the ring. It is assumed that when in this mode, if data loss is not desired that the host will guarantee that a chain of buffers will be provided that can receive the entire packet.

11.1.4.27.1.2 Protocol Errors

Protocol errors occur when the port logic detects that the received packet did not pass protocol specific criteria that was checked during reception of the packet. Examples of protocol errors include packet length errors, CRC errors, or alignment errors.

When protocol errors are detected, the port may choose whether or not it will drop the packet. The mechanism that is used to determine which packets to drop and which to forward is application specific. If the port determines that it needs to forward the packet to the Host, it will set the Packet Error bit in the Descriptor indicating that this is a packet which experienced a protocol related error. The type of protocol related error is generally indicated in either the Protocol Specific bits in the Host descriptor or in the Protocol Specific bytes region. The packet length information and certain portions of the Protocol Specific region may not be correct for packets which encounter errors.

11.1.4.27.1.3 Dropped Packets

Packets can be dropped within an Rx Port for any number for reasons which with the exception of the starvation case which was covered above are application specific.

When a Port determines that it needs to drop a packet after reception of the packet has begun, it must flush the remainder of the packet, increment the dropped packets statistic, and rewind any fetched descriptor/buffer chain so that the it can be use the same descriptor/buffer chain on the next packet.

11.1.4.27.1.4 Long Packet

For Rx channels which are not configured in single buffer mode, if the host provides a buffer chain whose total length is insufficient to receive the entire packet, whatever portion of the packet which has not been received will be flushed until an end of packet indicator is received on the PSI-L interface. This behavior will occur regardless of which error handling mode has been selected for the channel.

11.1.4.27.2 BCDMA Exception Conditions

Since the TR mode engine performs transfer sequencing using a count based mechanism it is susceptible to becoming out of synchronization if the source of the data and the destination for the data do not exactly match in their expectations for how much data will be transferred. The following sections outline these scenarios.

TR mode channel exceptions include:

- Reception of EOL delimiter
- Short Packets
- Long Packets
- Descriptor Starvation

11.1.4.27.2.1 Reception of EOL Delimiter

If an end of line delimiter is received by the Rx (write) side of the BCDMA the EOL_ADV field in the TR application specific flags field is used to advance the appropriate indices of the TR to the next level. Each EOL that is received will cause the TR to advance to the next specified loop iteration breaking as many intermediate loops as are required.

11.1.4.27.2.2 EOP Asserted Prematurely (Short Packet)

Split TR mode channels can experience an incoming packet whose length is shorter than what was expected based on one or more TRs which form the control description for the expected packet. If an EOP is received for a TR and the TR has not been completely executed, the port is required to receive as much data as is actually provided in the incoming data placing it in accordance with the instructions in the TR and the to continue executing any remaining TR(s) such that the required events are produced to keep downstream consumers in sync. In this case, no data will be transferred to the buffers described by the TR beyond what was provided in the incoming packet.

11.1.4.27.2.3 EOP Asserted Late (Long Packets)

Split TR mode channels can experience an incoming packet whose length is longer than what was expected based on one or more TRs which form the control description for the expected packet. If a TR completes and is marked as EOP but the incoming packet is not finished, then the port must throw away any additional received data until the incoming packet reaches an EOP condition. At this point, reception will start with a new TR and a new incoming packet.

11.1.4.27.2.4 Descriptor Starvation

Descriptor starvation occurs when the Port receives enough data for a burst but the ring for the channel is currently empty. This causes push back on the receive port and can cause lost data.

The Port will assert a starvation bit in the RX Receive Channel Status register (RCHANRT[a]_RRT_STATUS[1-0]). When the doorbell register (RINGRT[a]_RT_DB) is written to populate the ring the starvation bit will clear. Note that the intention is that the port will wait for an entry to be added to the ring. It is assumed that if data loss is not desired that the host will guarantee that a descriptor is present.

11.2 Data Movement Subsystem (DMSS)

This chapter describes the Data Movement Subsystem (DMSS) module in the device.

11.2.1 Data Movement Subsystem (DMSS)

This chapter describes the features and functions of the Data Movement Subsystem (DMSS) hardware modules in the device.

11.2.1.1 DMSS Overview

The DMSS module on AM64x provides data movement (DMA) and bridges between the CBA switched interconnect and the packet streaming fabric (network on chip) on the device.

The Data Movement Subsystem (DMSS) consists of DMA/Queue Management components and Peripherals:

- Packet DMA
- Block Copy DMA
- Ring Accelerator
- Packet Streaming Interface (PSILSS)
- Infrastructure components such as CBASS, secure proxy, and an interrupt aggregator

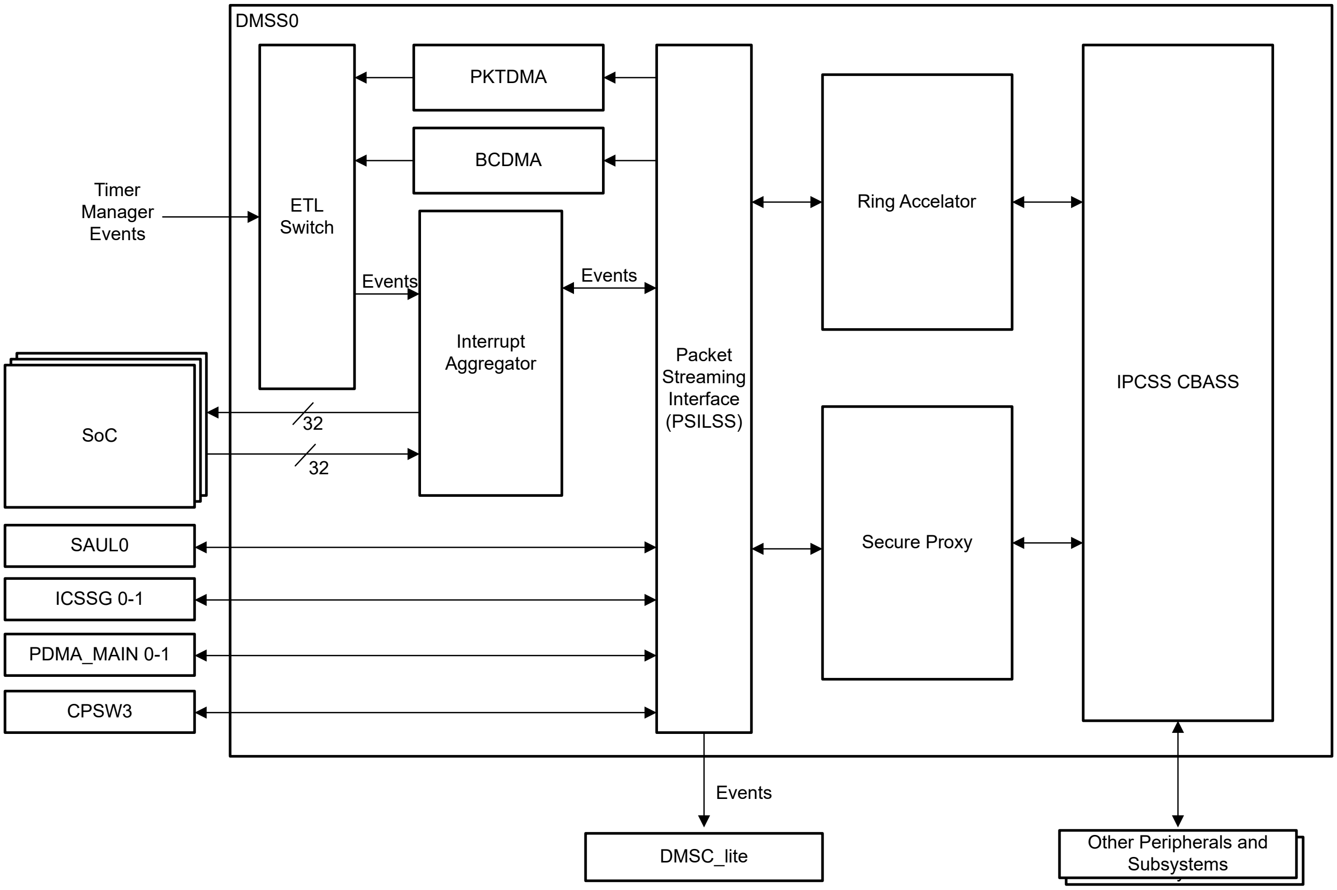

Figure 11-4. DMSS Top-Level Block Diagram

Table 11-64. DMSS Allocation Within Device Domains

Module Instance	Domain	
	MCU	MAIN
DMSS0	-	✓(DMSS)

11.2.1.2 DMSS Integration

Figure 11-5 shows the integration of the DMSS in the device

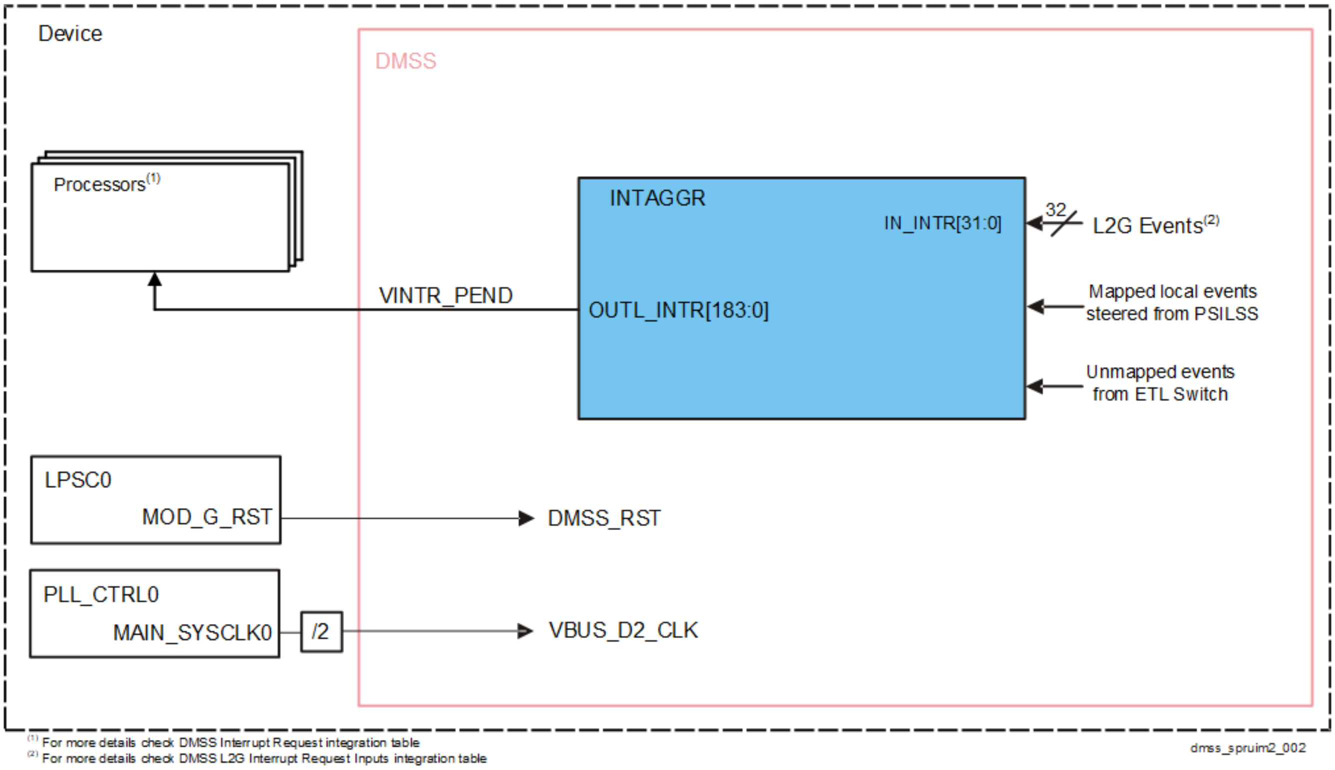

Figure 11-5. DMSS Clocks, Resets, and Interrupts

11.2.1.2.1 DMSS Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Local Power Sleep Controller (Module Domain)	SoC Interconnect
DMSS0	PSC0	PD0(GP)	LPSC0	CBASS0

11.2.1.2.2 DMSS Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
DMSS0	*DMA*_CLK	VBUS_D2_CLK	MAIN_SYSCLK0/2	DMA config interface clock. This clock is used for most of the DMSS modules

11.2.1.2.3 DMSS Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
DMSS0	*DMSS*_RST	MOD_G_RST	LPSC0	DMSS hardware reset

11.2.1.2.4 DMSS Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
DMSS0	VINTR_PEND[183:168]	NVIC_IN[47:32]	MCU_M4FSS0_CORE0	Level	VINTR_PEND[183:168] interrupts to NVIC_IN
	VINTR_PEND[39:0]	SPI_IN[103:64]	GICSS0	Level	VINTR_PEND[39:0] interrupts to GIC SPI
	VINTR_PEND[71:40]	INTR_IN[95:64]	R5FSS0_CORE0	Level	VINTR_PEND[79:40] interrupts to R5FSS0 CORE0
	VINTR_PEND[79:72]	INTR_IN[15:8]			
	VINTR_PEND[87:80]	INTR_IN[15:8]	R5FSS0_CORE1	Level	VINTR_PEND[87:80][71:40] interrupts to R5FSS0 CORE1
	VINTR_PEND[71:40]	INTR_IN[95:64]			
	VINTR_PEND[127:120]	INTR_IN[16:8]	R5FSS1_CORE0	Level	VINTR_PEND[127:88] interrupts to R5FSS1 CORE0
	VINTR_PEND[119:88]	INTR_IN[95:64]			
	VINTR_PEND[135:128]	INTR_IN[15:8]	R5FSS1_CORE1	Level	VINTR_PEND[135:128][119:88] interrupts to R5FSS1 CORE1
	VINTR_PEND[119:88]	INTR_IN[95:64]			
	VINTR_PEND[151:136]	DMSC_lite[15:0]	DMSC_lite	Level	VINTR_PEND[151:136] interrupts to DMSC_lite
	VINTR_PEND[159:152]	PR1_SLV_IN[7:0]	PRU_ICSSG0	Level	VINTR[159:152] interrupts to PRU_ICSSG0 PR1
	VINTR_PEND[167:160]	PR1_SLV_IN[7:0]	PRU_ICSSG1	Level	VINTR[167:160] interrupts to PRU_ICSSG1 PR1
	ECC_CORRECTED_ERR_LEVEL[0]	LVL_IN[9]	ESM0	Level	SEC interrupt from ECC_AGGR0
	ECC_CORRECTED_ERR_PULSE[0]	LVL_IN[10]		Pulse	SEC interrupt from ECC_AGGR0
	ECC_UNCORRECTED_ERR_LEVEL[0]	LVL_IN[72]		Level	DED interrupt from ECC_AGGR0
	ECC_UNCORRECTED_ERR_PULSE[0]	LVL_IN[73]		Pulse	DED interrrupt from ECC_AGGR0

11.2.1.2.5 DMSS L2G Interrupt Inputs

Module Instance	Module Interrupt Signal	Source Interrupt Input	Source	Interrupt Type	Description
DMSS0	L2G_EVENT_PEND[7:0]	CMPEVT_INTRTR0_OUTL[39:32]	CMPEVT_INTRTR0	Level	Interrupts from CMPEVT_INTRTR0
	L2G_EVENT_PEND[15:8]	TIMESYNC_INTRTR0_OUTL[7:0]	TIMESYNC_INTRTR0	Level	Interrupts from TIMESYNC_INTRTR0
	L2G_EVENT_PEND[23:16]	GPIOMUX_INTRTR0_OUTL[37:30]	GPIOMUX_INTRTR0	Level	Interrupts from GPIOMUX_INTRTR0
	L2G_EVENT_PEND[25:24]	GPIOMUX_INTRTR0_OUTL[17:16]			

Module Instance	Module Interrupt Signal	Source Interrupt Input	Source	Interrupt Type	Description
	L2G_EVENT_PEND_28	DEBUG_CELL_LEVEL_0	SAM64_DAVDMA_LEVEL0	Level	Interrupts from DAVDMA_LEVEL
	L2G_EVENT_PEND_29	GPMC_SDMAREQ_0	GPMC	Level	Interrupts from GPMC

11.2.1.2.6 DMSS DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Event Type	Description
DMSS0	-	-	-	-	No PDMA channels to external DMA engines

Note

For more infotmation about interconnects, see Chapter 3, System Interconnect.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5, Device Configuration.

For more information on the device interrupt controllers, see Section 9.2, Interrupt Controllers.

For more information on the time sync and compare events routers, see Section 11.3, Time Sync and Compare Events.

11.2.1.2.7 Global Event Map

The gobal event map for all dmss events is shown in Table 11-65.

Table 11-65. Global Event Map

Destination		Offset	PSIL Routed Slots	Actual Slots
DMSS Instance or External	Port			
DMSS	INTAGGR SEVI	0 (0k)	8192 (8k)	1536
DMSS	INTAGGR MEVI	8192 (8k)	2048 (2k)	128
DMSS	INTAGGR GEVI	10240 (10k)	2048 (2k)	256
external	DMSC IA SEVI	18432 (18k)	2048 (2k)	-
DMSS	INTAGGR LEVI	32768 (32k)	32 (0.03k)	32
external	PDMA_MAIN0 LEVI	41984 (41.000k)	128	-
external	PDMA_MAIN1 LEVI	42112 (41.125k)	128	-
DMSS	BCDMA Triggers	50176 (49k)	1024 (1k)	136 (0.133k)

11.2.1.2.8 PSI-L System Thread Map

The Thread MAP for DMSS is shown in the table below

Table 11-66. System Thread Map for All PSI-L Threads

Thread Number	NAV Instance	Endpoint
0x0000	DMSS	PSILCFG CFGSTRM
0x0020	DMSS	PKTDMA CFGSTRM
0x0021	DMSS	BCDMA CFGSTRM
0x1000-0x1FFF	DMSS	PKTDMA Threads

Table 11-66. System Thread Map for All PSI-L Threads (continued)

Thread Number	NAV Instance	Endpoint
0x2000-0x2FFF	DMSS	BCDMA Threads
0x3000-0x3FFF	DMSS	reserved
0x4000-0x40FF	DMSS	SAUL0
0x4100-0x41FF	DMSS	ICSS_G0
0x4200-0x42FF	DMSS	ICSS_G1
0x4300-0x43FF	DMSS	PDMA_MAIN0
0x4400-0x44FF	DMSS	PDMA_MAIN1
0x4500-0x45FF	DMSS	CPSW3

11.2.1.3 DMSS Functional Description

See Section 11.1 , Data Movement Architecture Overview, for the TI AM64x Data Movement Architecture (DMA) specification.

See the following sections for the respective module description:

- Packet DMA (PKTDMA)
- Block Copy DMA (BCDMA)
- Ring Accelerator (RINGACC)
- Infrastructure Components:
  - CBASS in System Interconnect
  - Secure Proxy (SEC_PROXY)
  - Interrupt Aggregator (INTAGGR)

11.2.1.4 DMSS Interrupt Configuration

This section describes the actions needed to configure interrupts within the DMSS.

Table 11-67. DMSS Parameters

Parameter	Value DMSS	Description
RA_RING_CNT	32	Number of total rings supported (specific to each ring accelerator)
IA_SEVI	1536	Interrupt Aggregator Source Event Input (SEVI) count (specific to each interrupt aggregator)
IS_VINTR	184	Interrupt Aggregator Virtual Interrupt (VINTR) count (specific to each interrupt aggregator)
EO	See Table 10-98, Global Event Map	Event offset

Table 11-68 lists software-configurable variables used in the examples and descriptions.

Table 11-68. DMSS Software Variables

Variable	Valid Range	Description
R#	0 – RA_RING_CNT-1	Ring number
E#	0 – (destination module specific)	Event number

Table 11-68. DMSS Software Variables (continued)

Variable	Valid Range	Description
GE#	= EO + E#	Global event number
SB#	0 – IA_SEVI-1	Interrupt aggregator status bit number
VI#	0 – IA_VINTR-1	Virtual interrupt number

Table 11-69. BCDMA Ring Mapping

Mapping	Channel Type	Rings	Description
chan_cnt	Block Copy (tx/rx pair)	ring[0:27]	28 BC channel count
tchan_cnt	Tx	ring[28:47]	20 Tx split channel count
rchan_cnt	Rx	ring[48:67]	20 Rx split channel count

11.2.1.4.1 DMSS Event and Interrupt Flow

Figure 11-6 illustrates the event and interrupt flow within the DMSS and output interrupts to a CPU.

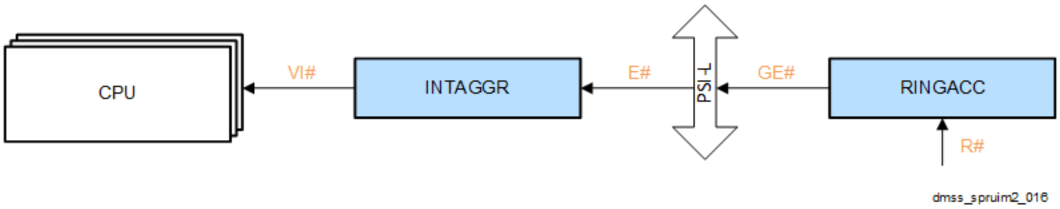

Figure 11-6. DMSS Interrupt Flow

11.2.1.4.1.1 DMSS Interrupt Description

This section describes the interrupt-related information that flows within DMSS and how this information is configured or generated.

1. Ring Number (R#)
   - Data is read from and written to a specific Ring Accelerator ring using direct ring-mode, or secure proxy access
   - The Ring Accelerator has specific ring number ranges for specific purposes. The R# must match the intended purpose of the ring. see Table 11-69 for details.
2. Global Event and Event Numbers (GE# and E#)
   - GE# = EO + E#
   - EO determines the destination module for the event. The PSILSS will route the GE# to the destination module per the DMSS event mapping, removing EO in the process. The destination module sees only E#. See Global Event Map for details.
   - For the INTAGGR module, E# ranges from 0 to (IA_SEVI - 1)
3. Virtual Interrupt (VI#)
   - The INTAGGR maps E# (via software configuration) to any SB#
   - ranges from 0 to (IA_SEVI - 1)
   - Each VI# (0 – (IA_VINTR-1)) is driven by a group of 64 contiguous SB# numbers (VI# driven by SB#'s VI#×64 – (VI#×64)+63)

11.2.2 Ring Accelerator (RINGACC)

This chapter describes the RINGACC module, part of the DMSS.

Note

Not all of the RINGACC Functions specified in the document are supported in the device. Updates will be included in the next revision to reflect only supported modes of operation.

11.2.2.1 RINGACC Overview

The Ring Accelerator (RINGACC or RA) provides hardware acceleration to enable straightforward passing of work between a producer and a consumer.

Table 11-70. RINGACC Allocation Within Device Domains

Module Instance	Domain	
	MCU	MAIN
DMSS0_RINGACC0	-	✓(DMSS)

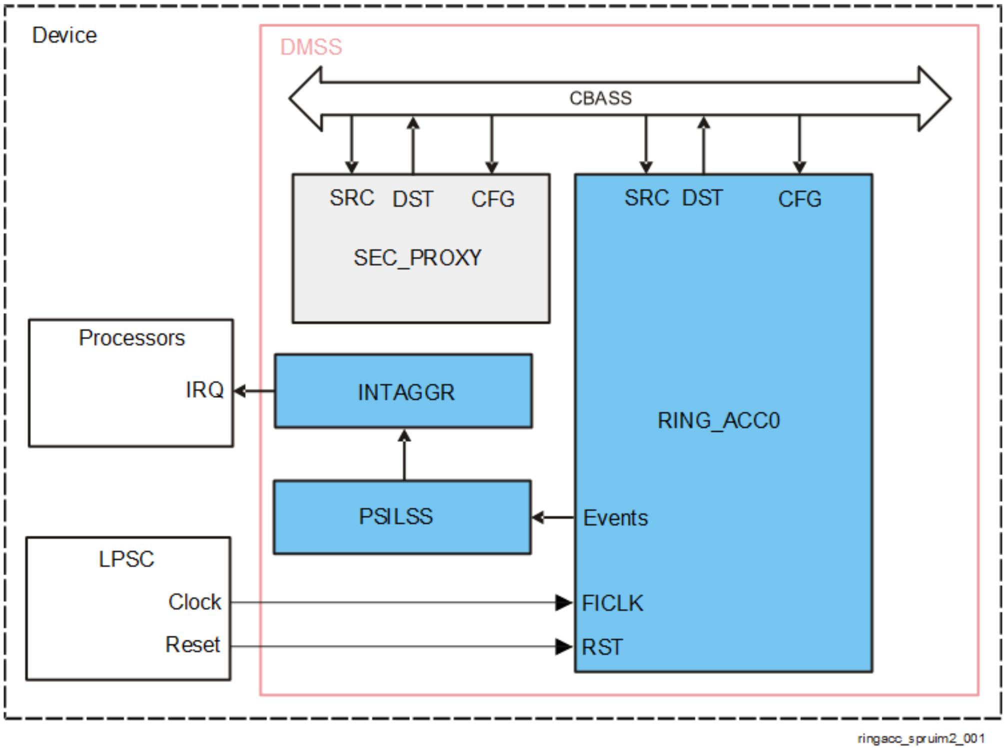

Figure 11-7. RINGACC Overview

11.2.2.1.1 RINGACC Features

- Ring Accelerator implementation
  - Supports up to 32 independent memory mapped ring structure
  - Supports various modes for each ring based on usage and compatability
  - Provides single word deep shared incoming Transfer Response FIFO
  - Optionally supports dynamic clock gating
  - Provides bit wide source VBUSM read/write target interface for accesses from DMA controller entities

- Provides 2 word deep command FIFO
- Provides 2 word deep write data FIFO
- Provides 2 word deep read data FIFO
- Provides 2 word deep write status FIFO
- Provides bit wide destination VBUSM read/write initiator interface for accesses to ring structures in memory
- Supports up to 16 outstanding writes
- Supports up to 16 outstanding reads
- Provides 2 word deep command FIFO
- Provides 2 word deep write data FIFO
- Provides 2 word deep read data FIFO
- Provides 2 word deep write status FIFO
- Source interface provides an array of 32x512-byte long address windows (four for each ring) which are packed into a single contiguous address range.
  - Read and write addresses which target a specific window are mangled to redirect the read or write transaction to an effective address calculated from the base address for the ring plus current ring offset.
  - Each read or write access presented on VBUSM target interface is modified and bridged onto the VBUSM initiator interface.

11.2.2.1.2 RINGACC Not Supported Features

- Queue manager mode, which makes the queue act like a traditional queue-manager (QM) queue, is not supported.
- Peeks from tail

11.2.2.1.3 RINGACC Parameters

Table 11-71 shows the RINGACC configuration parameters in this SoC

Table 11-71. RINGACC Configuration Parameters

Module Instance	Parameters		
	Ring Count	Number of Monitors	Proxy Target Base
DMSS0_RINGACC0	32	0	0x4e000000

11.2.2.2 RINGACC Integration

This section describes module integration in the device, including information about clocks, resets, and hardware request.

Figure 11-8 shows the RINGACC integration in the device.

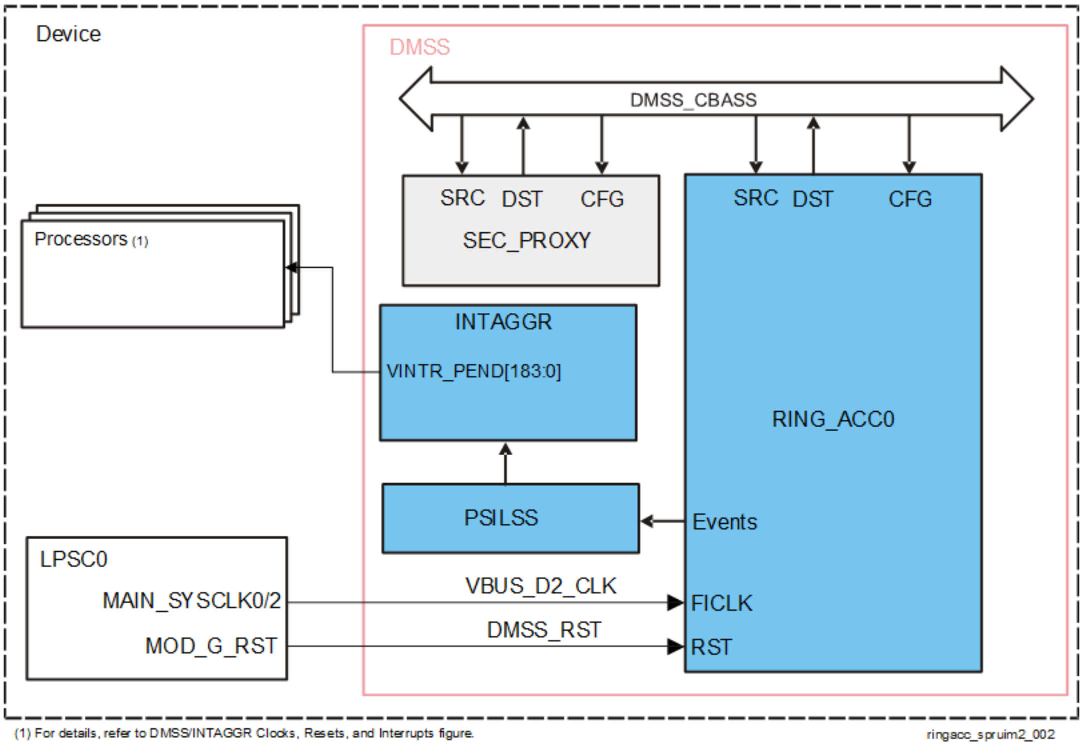

(1) For details, refer to DMSS/INTAGGR Clocks, Resets, and Interrupts figure.

Figure 11-8. DMSS0_RINGACC0 Integration

11.2.2.2.1 RINGACC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Local Power Sleep Controller (Module Domain)	SoC Interconnect
DMSS0_RINGACC0	PSC0	PD0(GP)	LPSC0	CBASS0

11.2.2.2.2 RINGACC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
DMSS0_RINGACC0	RINGACC_FICLK	VBUS_D2_CLK	MAIN_SYSCLK0/2	RINGACC clock. This clock is used for all interface and functional operations

11.2.2.2.3 RINGACC Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
DMSS0_RINGACC0	*RINGACC_RST*	MOD_G_RST	LPSC0	RINGACC hardware reset

11.2.2.2.4 RINGACC Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
DMSS0_RINGACC0	-	-	-	-	The module does not generate traditional interrupts

11.2.2.2.5 RINGACC Outbound Events

Module Instance	Module Event	Destination Event Input	Destination	Outbound Event Type	Description
DMSS0_RINGACC0	RING[0:31]_EVT	SEVI	DMSS_INTAGGR	ETL Push	Ring events. Can be used by an external host for statistics or interrupts.
	ERROR_EVT	SEVI	DMSS_INTAGGR	ETL Push	Bus error event for host interrupts

11.2.2.3 RINGACC Functional Description

The Ring Accelerator (RINGACC) converts constant-address read and write accesses to equivalent read or write accesses to a circular data structure in memory. The RINGACC eliminates the need for each DMA controller which needs to access ring elements from having to know the current state of the ring (base address, current offset). The DMA controller performs a read or write access to a specific address range (which maps to the source interface on the RINGACC) and the RINGACC replaces the address for the transaction with a new address which corresponds to the head or tail element of the ring (head for reads, tail for writes). Since the RINGACC maintains the state, multiple DMA controllers or channels are allowed to coherently share the same rings as applicable. The RINGACC serves a very similar function to the Queue Manager in the earlier SoCs. The RINGACC uses less memory and is able to place data which is destined towards software into cached memory directly.

For more information on ring operation, please check section *PKTDMA/BCDMA - Ring Operation*

11.2.2.3.1 Block Diagram

Figure 11-9 shows ring accelerator's main internal components.

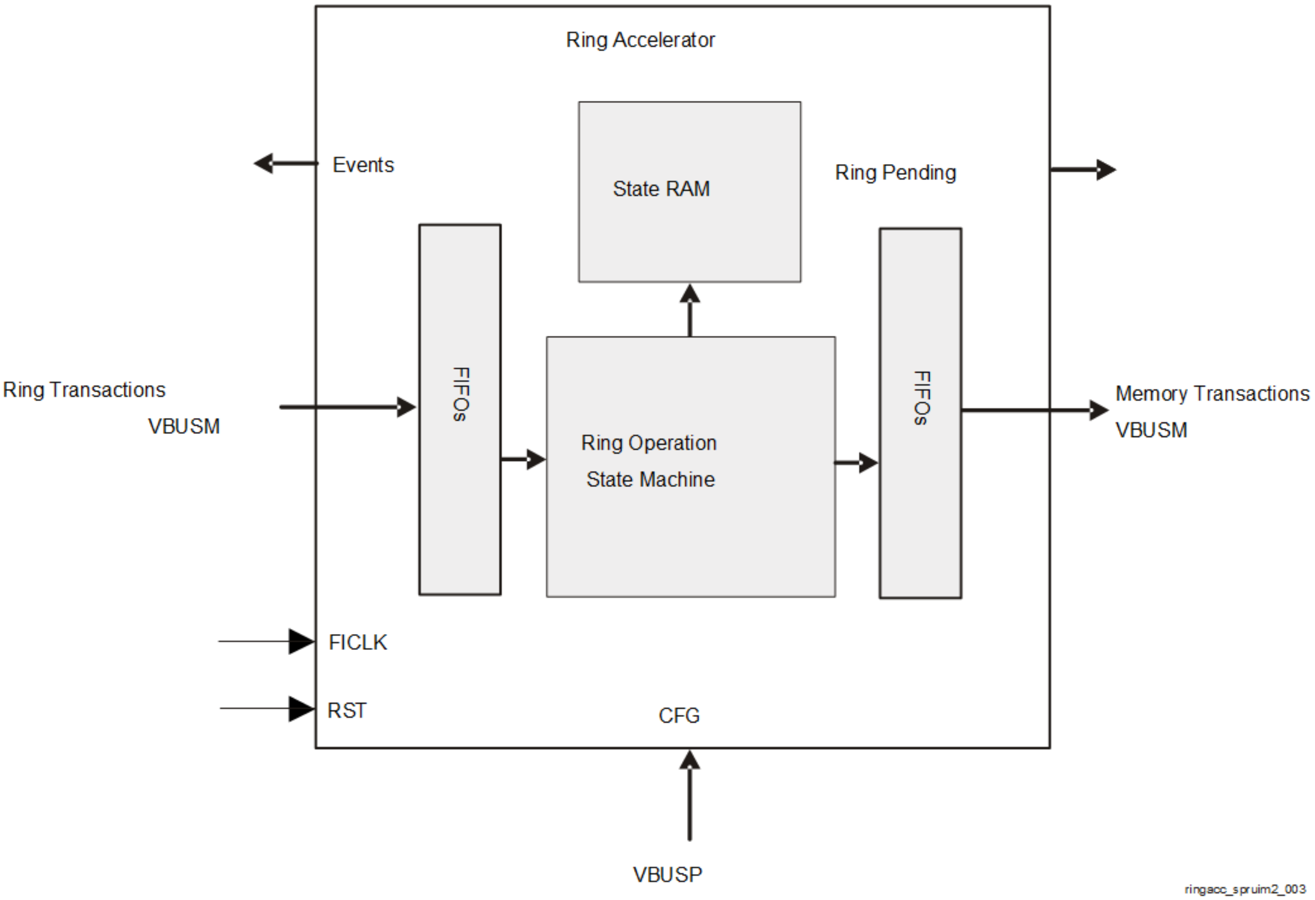

Figure 11-9. Ring Accelerator Block-Diagram

11.2.2.3.1.1 Configuration Registers

The Configuration Registers block is responsible for providing memory mapped registers for configuration of the RINGACC functions. The configuration registers are divided into:

- Static configuration fields (RINGACC_GCFG), which are typically initialized and then left at specified values for long time periods (or until a reset occurs)

- Real-time (RT) registers (RINGACC_RT), which are modified frequently during runtime. Configuration registers are listed and described in RINGACC_RT Registers.

11.2.2.3.1.2 Source Command FIFO

The Source Command FIFO buffers VBUSM command phases which are accepted from the VBUSM source interface.

11.2.2.3.1.3 Source Write Data FIFO

The Source Write Data FIFO buffers VBUSM write data phases which are accepted from the VBUSM source interface.

11.2.2.3.1.4 Source Read Data FIFO

The Source Read Data FIFO buffers VBUSM read data phases which have been returned from the VBUSM destination interface (via the main state machine) and which are to be output on the VBUSM source interface.

11.2.2.3.1.5 Source Write Status FIFO

The Source Write Status FIFO buffers VBUSM write status data phases which have been returned from the VBUSM destination interface and which are to be output on the VBUSM source interface.

11.2.2.3.1.6 Main State Machine

The Main State Machine (MSM) block implements all of the control logic which is necessary to accept a command from the source interface, perform a lookup into the ring state RAM, determine the effective address for the destination interface transaction, modify the address (and byte count for reads) for the transaction, and place that modified transaction into the outgoing destination FIFOs. The MSM block is also responsible for updating the ring index and occupancy values and for producing output status to inidicate changes to the ring state. The MSM also modifies the ring state whenever the read data or write status for a previous ring transaction return and forwards those responses back to the originating initiator.

11.2.2.3.1.7 Destination Command FIFO

The Destination Command FIFO stores VBUSM transaction commands which are output from the MSM as modified versions of transactions that were popped fromt the Source Command FIFO. The Destination command FIFO allocates a new command ID for each read or write command that is pushed to the FIFO. Read IDs are allocated from a scoreboard maintained in the Destination Read Data FIFO. Write IDs are allocated from a scoreboard maintained in the Destination Write Status FIFO. When a new command is allocated, the Destination Command FIFO also pushes the original cid and crouteid values from the source side transaction into a scoreboard in either the Destination Read Data or Destination Write Status FIFOs depending on the applicable transaction direction. The read interface of the Destination Command FIFO directly drives commands onto the destination VBUSM command interface.

11.2.2.3.1.8 Destination Write Data FIFO

The Destination Write Data FIFO stores write data phases for write commands that are passing through the RINGACC towards memory. The write interface of the Destination Write Data FIFO is directly connected to the read interface of the Source Write Data FIFO and the read interface directly drives write data onto the destination VBUSM write data interface.

11.2.2.3.1.9 Destination Read Data FIFO

The Destination Read Data FIFO provides a read command translation scoreboard and also stores read data phases that are passing through the RINGACC towards the originating DMA controller. The write interface of the Destination Read Data FIFO is directly connected to the destination VBUSM read data interface. As read data passes through the Destination Read Data FIFO, the *rid* and *rrouteid* are changed back to their original values using information which was stored in read command translation scoreboard.

11.2.2.3.1.10 Destination Write Status FIFO

The Destination Write Status FIFO provides a write command translation scoreboard and also stores write status phases that are passing through the RINGACC towards the originating DMA controller. The write interface of the

Destination Writes Status FIFO is directly connected to the destination VBUSM write status interface. As write status words pass through the Destination Write Status FIFO, the *sid* and *srouteid* are changed back to their original values using information which was stored in the write command translation scoreboard.

11.2.2.3.2 Events

The module outputs events about queue levels that can be used by an external module for statistics or interrupts.

Each queue has:

- an up event when the queue goes from 0 elements to 1 or more elements
- and a down event when the queue goes from 1 or more elements to 0 elements. The event number is programmable per queue in the RING[a]_EVT register. This event occurs when the state machine updates the final occupancy for the queue. In ring mode this is when the response from the memory access returns, while in other queue modes this is when the operation is processed.

An event number programmed to 0xFFFF indicates to not produce an event for that ring when an event is not necessary. The register event number fields reset to 0xFFFF, so they must be programmed to a valid value before events will be generated. This applies to the monitor event number fields as well.

11.2.2.3.3 Bus Error Handling

If a bus error is detected on a response to a ring memory transaction, an error event is triggered to alert software. Since the ring contents may be corrupted as the push or pop was not completed correctly, software should consider resetting the ring and any software or hardware elements using the ring. A log register (RINGACC_ERROR_LOG) captures the ring that had the error and whether it was from a push or pop, and an error up event is sent to the programmed event number. After an error is logged, another will not be captured until the first is read out. When read, if an error is pending an error down event is sent to clear any interrupt, and then the next bus error log can be captured. A read of the RINGACC_ERROR_LOG register when there is no error log pending will not produce any down events. The event that is triggered is also programmable. Only legal push and pop operations will capture this error, and not for any peek, emudbg read, flush command, or any operations that is illegal and causes the resulting memory access to be flushed.

11.2.2.3.4 Monitors

Monitors can be configured that allow various functions to be tracked of programmed queues. Each monitor is programmed to monitor a particular queue, the function to provide, and the data source to operate on. The supported functions are: to check the queue against programmed thresholds, to keep track of watermarks of the queue, to keep track of starvation occurrences (a read of an empty queue), or statistics capture. The supported data sources are: the queue element count, the head element size value, or the accumulated size value. Each monitor can also be programmed to produce an event should it have a triggering condition.

11.2.2.3.4.1 Threshold Monitor

A threshold monitor uses a programmed low threshold value and a programmed high threshold value to track the data source in the queue and cause an interrupt or status when a threshold is broken, either below the low value or above the high value. This is useful for software to replenish empty buffers when a queue has too few, or for a queue to accumulate enough elements so that software must start processing them, or for debug. The threshold being broken will cause the up or down event.

11.2.2.3.4.2 Watermark Monitor

A watermark monitor tracks the low and high values of the data source since the last read of the monitor. After initial setup or clearing, the watermark values will load the current value of the data source as the low and high. Then for successive operations if the resulting data source of the queue is below the low watermark, or above the high watermark, the associated watermark will be updated. When the monitor value registers are read, the value is cleared and starts tracking again using the current data source value. This can be useful for tracking low and high values of queue element counts or sizes for data tracking, debug or future optimizations, such as allocating items to a queue or buffer sizes based on counts.

11.2.2.3.4.3 Starvation Monitor

A starvation monitor tracks the number of starvation events (a read to an empty queue) that occurred on the queue. The data source is ignored, and the starvation count is always incremented whenever there is a read to the queue and the queue is empty. The count is cleared when the monitor value is read. This can be useful to trigger if any starvation event occurs, or to track how many of these events occur in a timeframe, and can be used for future optimizations or debug.

11.2.2.3.4.4 Statistics Monitor

The statistics monitor can track some simple statistics on the queue operations. The data source is ignored. The first value is the count of the number of writes to the queue, and the second value is the count of the number of reads from the queue. The counts are cleared when the monitor values are read. This can be useful to track the activity on a queue, and can be used for future optimizations or debug.

11.2.2.3.4.5 Overflow

RINGACC provides an overflow function where a push to a full ring will result in a push to a special overflow ring, rather than just losing the pushed data. The overflow ring is defined through RINGACC_OVERFLOW register, and that ring must be defined with a large enough element size to cover the element size of any other ring, as well as enough elements to hold enough overflow data (as an overflow to the overflow ring will be lost). When there is a push to a full ring, there will be two elements written to the overflow ring, first the push data, and then the ring number that was full. A supervisor entity can own the overflow ring and perform what actions are needed from the overflow data. The size of the overflow ring must be an even number since two elements will be pushed for each overflow event. The overflow ring must be configured in ring or message modes.

An overflow queue value of 0xFFFF will disable the overflow function and will not record queue overflows. (SR2.0)

11.2.2.3.4.6 Ring Update Port

To enhance performance for DMAs, the RINGACC provides a bus that indicates when ring updates occur, allowing the DMA to track their own rings and detect updates before the responses arrive. The bus will go valid whenever there is an update to the state of a ring, which can be from a push, pop, or doorbell write. It will not go valid for a peek, a emudbg pop, a push to a full ring, as those do not update the ring state. When the bus is valid, the other signals are valid and indicate whether the operation was a push or a pop, whether the resulting state of the ring is empty, the ring number, and the number of elements updated to the ring (the push determines whether it is subtracted or added to the current count). One special case is a pop from an empty ring, which indicates an update but the element count is 0 since no items were actually popped, but a DMA using the cnt to add or subtract must handle this correctly by default. The bus will go valid once the operation command has been completed, and not after the response has been recevied, even for ring mode rings, allowing the DMA to see the update as soon as it is known by the RINGACC even before it is known to software.

11.2.2.3.4.7 Tracing

This module provides a trace output of all operations so that the traffic can be viewed at a later time. The trace uses a simple write-only 32-bit VBUSP bus, with a defined packet header. The msgtype field defines the type of operation, and the message data is simply the data involved in the operation. It is likely the trace output will be read slower than new operations could provide data, so there will be a trace buffer able to hold two complete messages plus trace headers. If a new operation starts while the trace buffer does not have enough space, then that trace message will not be sent. And RINGACC_TRACE_CTL register controls whether to enable the trace output, whether to trace a single queue or all queues, and whether to include the message data in the trace output.

Table 11-72 shows the trace message for a push.

Table 11-72. Trace Message for a Push

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware
1	15:9	0x1	Msgtype for push
1	8:0	0x009	Standard Trace Header
2	31	push_to_head	Push to head flag, 0 = to tail, 1 = to head
2	30:16	0x0	Unused
2	15:0	queue	Queue for push
3-N	31:0	message data	Optional message data for push, length dependent on message size

Table 11-73 shows the trace message for a pop.

Table 11-73. Trace Message for a Pop

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware
1	15:9	0x2	Msgtype for pop
1	8:0	0x009	Standard Trace Header
2	31	empty	empty pop, 0 = valid message, 1 = empty
2	30:16	0x0	unused
2	15:0	queue	queue for pop
3-N	31:0	message data	Optional message Data for pop, length dependent on message size

Table 11-74 shows the trace message for a peek

Table 11-74. Trace Message for a Peek

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware
1	15:9	0x3	Msgtype for peek
1	8:0	0x009	Standard Trace Header

Table 11-74. Trace Message for a Peek (continued)

Word	Bits	Data	Comment
2	31	empty	empty peek, 0 = valid message, 1 = empty
2	30:16	0x0	unused
2	15:0	queue	queue for peek
3-N	31:0	message data	Optional message Data for peek, length dependent on message size

11.2.3 Secure Proxy (SEC_PROXY)

This chapter describes the Secure Proxy (SEC_PROXY) module in the DMSS.

11.2.3.1 Secure Proxy Overview

The Secure Proxy module provides proxy buffers for hosts that need to create large data bursts but can only perform small accesses.

11.2.3.1.1 Secure Proxy Features

Secure Proxy supports the following features:

- Provides proxy function to store large data bursts that a host can only access in smaller amounts
- Supports a configurable number of threads, where each has their own independent proxy function
- Keeps the large data burst coherent until the complete data has been accessed
- Allows for interleaved access between multiple hosts or tasks using multiple proxy threads
- Supports a configurable target resource. The target has a configurable number of channels, size of each channel and base address
- Supports a programmable fixed queue for each proxy thread
- Supports multiple producers all writing to the same queue
- Supports a max message count for outbound proxy threads limiting the number of messages a thread can produce
- Supports programmable thresholds for when to generate events
- Optionally supports dynamic clock gating

Table 11-75. Secure Proxy Allocation Within Device Domains

Module Instance	Domain	
	MCU	MAIN
DMSS0_SEC_PROXY0	-	✓(DMSS)

11.2.3.1.2 Secure Proxy Parameters

Table 11-76 shows the Secure Proxy configuration parameters set during SoC design.

Table 11-76. Secure Proxy Configuration Parameters

Module Instance	Parameters				
	Proxies[1]	Message Size[2]	Target	Channels[3]	Sizes[4]
DMSS0_SEC_PROXY0	76	64	DMSS0_RINGACC	20	4096

(1) Number of proxy threads supported. Can be read off from the SEC_PROXY_CONFIG read-only register

(2) Number of bytes for message. Can be read off from the SEC_PROXY_CONFIG read-only register

(3) Number of channels for the target

(4) Number of bytes per channel supported for the target

11.2.3.1.3 Secure Proxy Not Supported Features

The following features are not supported by the module:

- Does not support proxy thread sharing. Each host or task must use its own proxy thread within the module if they can access simultaneously or independently. This includes when the task can be interrupted by another task that also uses the proxy

- In the system, a proxy must be the only method to access messages that use the same set of queues (to keep credits local), which means all hosts using the same set of message queues must also use the same proxy IP for access and not local proxys
- Does not support multiple proxy threads reading from the same queue. For tracking purposes, there can be only 1 consumer proxy thread per queue

11.2.3.2 Secure Proxy Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 11-10 shows the Secure Proxy integration in the DMSS.

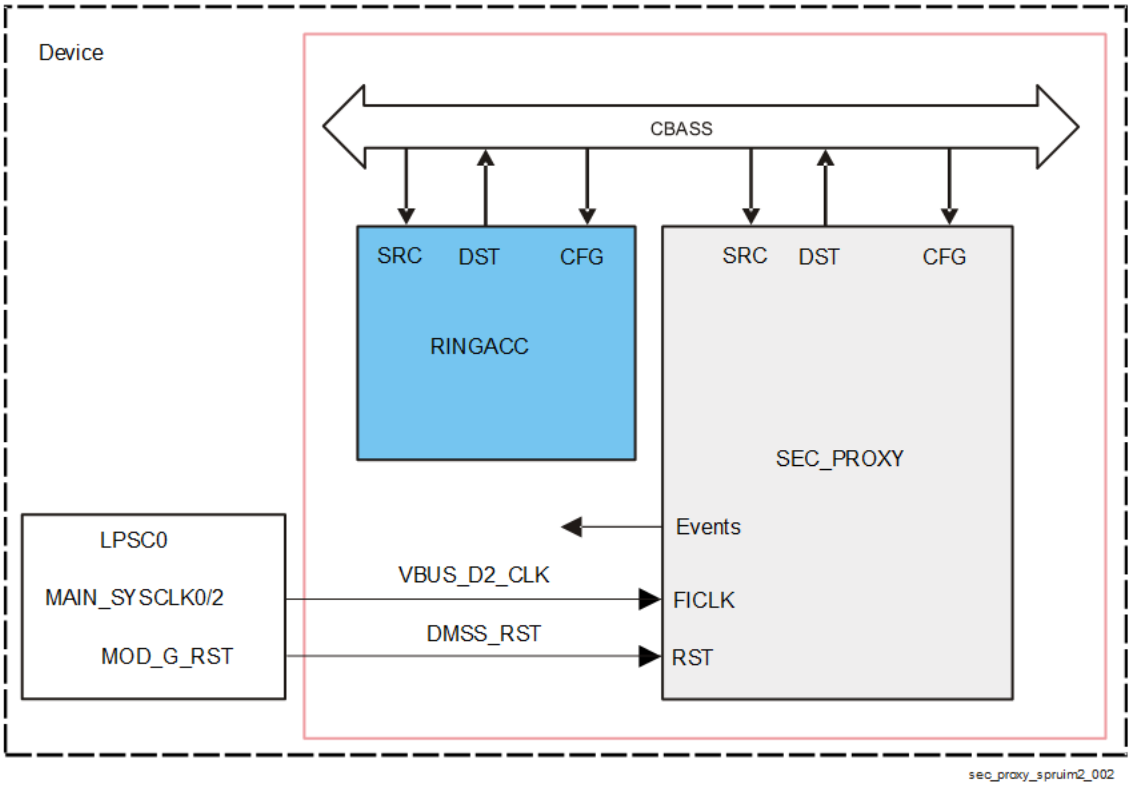

Figure 11-10. Secure Proxy Integration

11.2.3.2.1 Secure Proxy Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Local Power Sleep Controller (Module Domain)	SoC Interconnect
DMSS0_SEC_PROXY0	PSC0	PD0	LPSC0	CBASS0

11.2.3.2.2 Secure Proxy Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
DMSS0_SEC_PROXY0	SEC_PROXY_FICLK	VBUS_D2_CLK	MAIN_SYSCLK0/2	Proxy clock. This clock is used for all interface and functional operations

11.2.3.2.3 Secure Proxy Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
DMSS0_SEC_PROXY0	SEC_PROXY_RST	MOD_G_RST	LPSC0	Proxy hardware reset

11.2.3.2.4 Secure Proxy Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
DMSS0_SEC_PROXY0	-	-	-	-	No interrupts to external interrupt controllers

11.2.3.2.5 Secure Proxy DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Type	Description
DMSS0_SEC_PROXY0	-	-	-	-	No PDMA channels to extrernal DMA engines

11.2.3.3 Secure Proxy Functional Description

This module provides proxy functions for hosts that need to create large data bursts but can only perform small accesses. Examples of this need are:

- large messages (for power control, security control, or IPC)
- data descriptors that are more than a pointer
- DMA Transfer Requests (TR)

All of these require larger data sets, from 12 to 128 bytes, and the storage hardware requires the entire data on the bus in a single burst. Unfortunately, many CPUs cannot produce bursts to device memory, such as registers, and the largest CPU access is typically 8 bytes. So the proxy provides the ability to access the hardware with a single burst, and at the same time allows the CPU to access the same data in smaller accesses. The proxy itself does not contain the resources, but will front other hardware that do contain the resources. The proxy will access these other hardware with the entire data in a single burst, once the host has completed the data.

Figure 11-11 describes Secure Proxy major building block

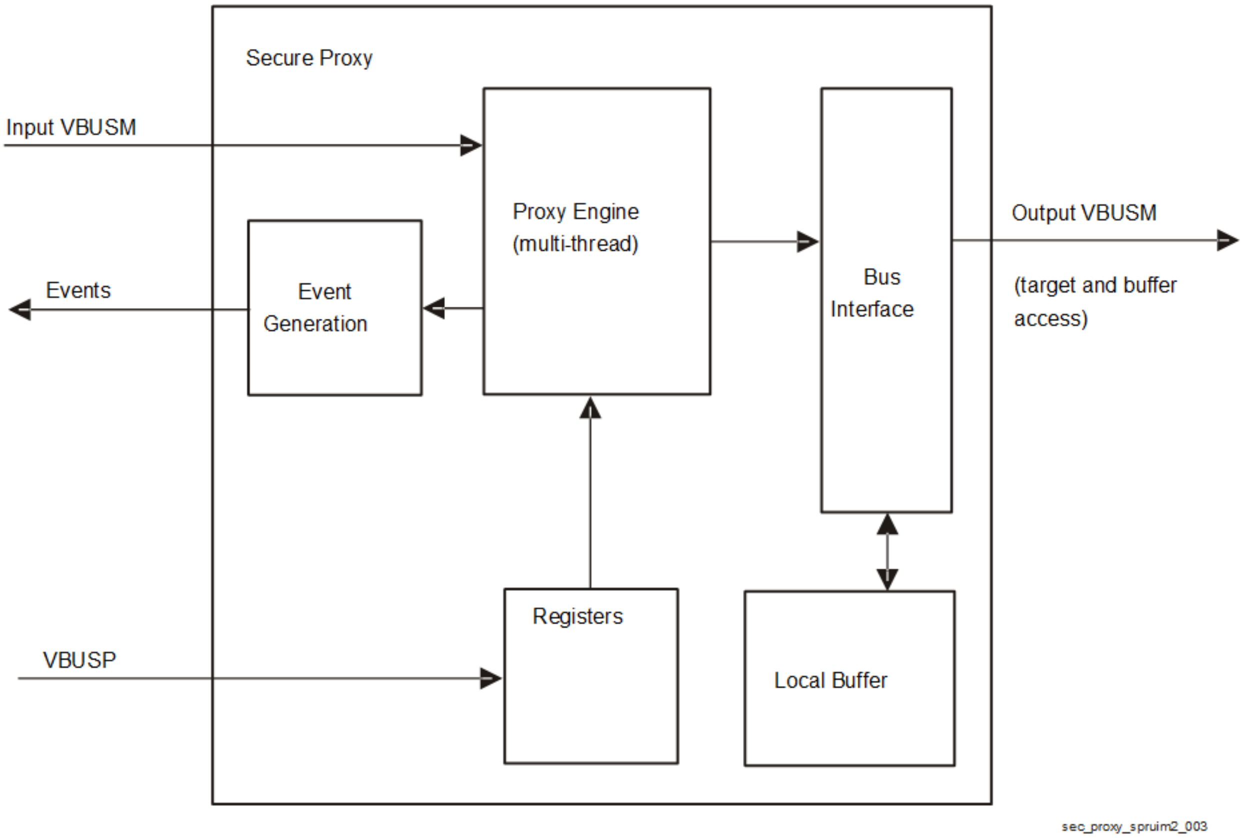

Figure 11-11. Secure Proxy Block Diagram

11.2.3.3.1 Targets

11.2.3.3.1.1 Ring Accelerator

The RINGACC provides four distinct offsets to use per ring/queue shown in Table 11-77, totaling 4 KB space per ring/queue.

Secure Proxy always writes to tail, which is the offsets from 0x200 to 0x3FF. Secure Proxy always reads from the head, which is the offsets from 0x000 to 0x1FF. The latter two offsets in RINGACC are not used by this proxy. And if the proxy message size is less than 512 bytes, then it always access the upper bytes of those regions, so that the message always ends on the last byte of each region, byte 511.

Table 11-77. RINGACC Offsets per Ring/Queue

Offset	Operation
0x0 - 0x1FF	Reads pop from head. Writes push to head.
0x200 - 0x3FF	Writes push to tail. Reads pop from tail.
0x400 - 0x5FF	Reads peek from head. Writes ignored.
0x600 - 0x7FF	Reads peek from tail. Writes ignored.
0x800 - 0xFFF	Reserved.

This means that target writes will use the following calculation:

target base address + (queue × 4KB) + 0x400 - msg_size (17), and burst until offset 0x3FF.

And target reads will use the following calculation:

target base address + (queue × 4KB) + 0x200 - msg_size (18), and burst until offset 0x1FF.

11.2.3.3.2 Buffers

The proxy does not store all the buffers internally. It is programmed with a buffer base address (SEC_PROXY_BUFFER_L, SEC_PROXY_BUFFER_H), and all accesses to the buffer are made through the output VBUSM port using that base. The external buffer must be enough to store one msg_size per proxy thread. The proxy only includes a small temporary buffer to save one entire message when accessing the target. Otherwise all host accesses are made to the external buffer. This buffer storage must be considered private for the proxy hardware, so any other access can cause unpredictable results.

11.2.3.3.2.1 Proxy Credits

To support outbound proxy limits, the proxy will use internal credits for tracking resource usage. SEC_PROXY_THREAD[a]_CTL register sets the max credits each outbound proxy thread contains. When a proxy thread sends a message, the current credit count (SEC_PROXY_THREAD[a]_STATUS) decrements by 1. If the current credit count is 0, then the proxy thread is not allowed to send any more messages, and they just remain inside the proxy (so that the host can come back later when a credit has become available and quickly send the same message). When a message that was sent by this proxy thread is read by an inbound proxy thread then the credit is returned to this proxy thread and the current credit count increments by 1.

For inbound proxy threads, the credits are used to track pending messages. When an outbound proxy thread sends a message that is read by this proxy thread, then the current credit count of this proxy thread is incremented by 1. A current credit count that is non zero indicates a message is pending and can be read. When the proxy thread completes the read of a message the current credit count is decremented by 1. If the current credit count is zero, then the proxy thread will read an empty message where all the data is 0s. The credit count saturates at 255, so if there can be more messages in the system for that proxy thread than 255 then multiple proxy threads should be used, or the count can become mismatched after a saturate.

11.2.3.3.2.2 Proxy Private Word

To support tracking of credits from each proxy thread, the proxy will extract the first word from the total message size for private tracking usage. This will include saving the proxy thread ID used within the proxy. This is necessary so that when a proxy reads a new message from the target it can inspect this word and return the credit to the source proxy thread. This allows the outbound proxy threads to have a set number of message credits, which decrement when a new message is written, and increment when a message from that proxy thread is read, thus keeping the credits in the system coherent. Any data written to this first word of the message will be ignored, so software should not write to the first word of messages through the proxy. Consumer software can use the first word to identify the source proxy thread of the message (SEC_PROXY_DATA_j).

11.2.3.3.2.3 Completion Byte

The proxy completes a message when the completion byte is accessed. This completion byte is the final byte in the full size of the message. This byte can be written by any size access, whether byte, 32-bit, or 64-bit word. The write of a message is not complete until this final byte of the message is written, and only then will the message be sent to the target. The read of a message is not complete until this final byte of the message is read by the host, and only then will reading a new message be allowed. Even if the final byte of the message is not needed, it must be accessed to complete the message inside the proxy hardware.

11.2.3.3.3 Proxy Thread Sizes

There are a configurable number of proxy threads in the module. Each thread has its own address space to the module and determining which proxy thread is being accessed is simply based on the address bits above the final size of each proxy thread space. Since each proxy thread will be programmed to a single resource, the only space requirement is that for using 4 KB to match typically used MMU page sizes. Only the first N bytes, matching the target channel size, is usable.

11.2.3.3.4 Proxy Thread Interleaving

Each proxy thread must have a single owner, as each proxy thread only has a single buffer to work on the current data. If there are multiple owners in the system, they must each use their own proxy thread. Then they will have their own buffer and each can access a different resource at the same time. Each proxy thread is completely independent and kept coherent regardless of accesses to other proxy threads or regardless of the order of accesses. So the proxy support interleaving of multiple hosts' accesses.

11.2.3.3.5 Proxy States

Each proxy thread uses a simple state machine to track the current usage by that host. This state machine is used to track when a proxy thread is in use or not, but also for error detection. The proxy thread always starts in idle state, when there is no current activity. There is a write state for when the proxy thread has been written and contains data that has yet to be written to a resource. There is a read state for when the proxy thread has read data from a resource and that entire data has not been fully read by the host. When a proxy thread access completes, final write or final read, then the state will go back to idle. The following sections show the utilization of these states.

11.2.3.3.6 Proxy Host Access

A proxy thread begins in an idle state, where there is no data in the buffer. In this state the proxy thread will accept an access to the resource.

11.2.3.3.6.1 Proxy Host Writes

The first write to an idle proxy thread puts the proxy thread into write mode for the selected channel. Further legal writes are stored in the buffer for the enabled bytes and offset within the buffer. A write to a previously written location will overwrite the previous data. The buffer is not cleared initially, so if a byte is not written, the message will include previous buffer data. When there is a legal write to the last byte of the resource, then the entire data is written by the proxy to the target and channel as a single write burst. The proxy will wait for the write status from the target write before it sends the write status for this final byte host write. This allows the host to use the write status to guarantee the entire write data from the proxy has landed at the target. The proxy thread is then put back into idle state. A write completion when there are no credits available results in the message not being written to the resource and the proxy thread remains in write mode (so that the message can be quickly completed when a credit becomes available).

11.2.3.3.6.2 Proxy Host Reads

When in idle state, the first read to the proxy thread will put the proxy into read state, and the proxy will read the target and channel requested in a single burst of the target's channel size. When the data is returned it is stored in the buffer and the accessed part is returned to the host. Further legal reads are allowed and return the accessed data in the buffer. When there is a legal read to the last byte of the resource, the accessed data is returned, and the proxy thread is put back into idle state. If an initial read is made and there are no pending messages, the proxy thread will return an empty message, where the data is all 0s.

11.2.3.3.6.3 Buffer Accesses

Each read or write will actually trigger a read or write to the external buffer space allocated for that proxy thread, where the real message data is stored. In addition, when a write message completes, the external buffer will be read for the entire message for that proxy thread so that it can then be written to the target. Similarly, after a read causes a read from the target to get a new message, the entire message is written to the external buffer to store the message to the buffer.

11.2.3.3.6.4 Target Access

After the write has completed and the external buffer read for the entire message, the entire message is then written to the target as a single burst. Similarly, for a read that needs a new message, the target is read for a full message as a single burst.

11.2.3.3.6.5 Error State

If an error is detected in a proxy thread, the proxy will put that proxy thread into error state, and the current buffer will be lost. A status bit will be set that indicates the proxy thread is in error. All accesses to that proxy thread will be ignored until the status bit is cleared. Once cleared the proxy thread is put back into idle state. Errors are: an access to an offset beyond the length of the message, or a mismatch in the direction of access against what was programmed such as reading an outbound thread or writing an inbound thread.

11.2.3.3.7 Permission Inheritance

The proxy will automatically inherit the permissions from the access and pass these to the target upon the target burst access. The exact transactions that are inherited from are the final byte write or the first read, and these exact permissions are used on the output bus transaction that accesses the target.

11.2.3.3.8 Resource Association

Each proxy thread has a register (SEC_PROXY_THREAD[a]_CTL) to define the resource within the target that the proxy thread is mapped to. The host has no ability to access any other resource in the target. This allows the setup of the proxy to determine the resources that all the hosts use.

11.2.3.3.9 Direction

Each proxy thread has a register (SEC_PROXY_THREAD[a]_CTL) to define the direction for access. It can either be an outbound proxy thread for writing messages to resources. Or it can be an inbound proxy thread for reading messages from resources. The host must match the direction programmed or it will result in a proxy thread error.

11.2.3.3.10 Threshold Events

Each proxy thread can produce events based on the state of the resource it uses. For outbound proxy threads, a threshold can be set so that an event is produced when there are now at least N messages available to write. For inbound proxy threads, a threshold can be set so that an event is produced when there are now at least N messages available to read. These threshold values are programmed in SEC_PROXY_EVT_MAP_j, allowing the host to determine how often it gets events. Programming the count values while the threshold is set to 0 will not trigger events, but if the threshold is not 0 then programming the counts will trigger events based on whether the threshold is reached or not. No event is generated if the event is programmed to 0xFFFF.

11.2.3.3.11 Error Events

Each proxy thread can produce an event when it has detected an error. This error occurs when the host violates the programmed setup of the proxy thread or accesses beyond the message size. There is a separate status bit per proxy thread for these errors. No event is generated if the event is programmed to 0xFFFF.

11.2.3.3.12 Bus Error and Credits

If a target read for a message returns a bus error, this indicates the read was bad and the data is corrupt and usually 0s. Because the private word in contained in the message, if the private word is corrupted then the source proxy thread is not valid and the credit return will not be correct. Since the data is usually 0, this means the credit would be returned to proxy thread 0 incorrectly most of the time. And the credit will be lost for the actual source proxy thread of the message that was not read correctly. The hardware has no way to correct for this, as the message from the target is corrupt so it does not know the correct owner of the credit. If software detects that a read message is corrupt, it can attempt to correct the situation by resetting the affected proxy threads using that queue, to restore their credit counts back to the default. Software may also want to reset proxy thread 0 since it may be getting extra credits.

11.2.3.3.13 Debug

When the transaction has the emudbg set for a read, all side effects will not occur. This means that the read will not cause a target read since that would affect the target, and instead current buffer will be read even if the previous message has completed.

11.2.4 Interrupt Aggregator (INTAGGR)

This chapter describes the INTAGGR module, part of DMSS

11.2.4.1 INTAGGR Overview

The Interrupt Aggregator (INTAGGR or INTA) provides a centralized machine which handles the termination of system events to that they can be coherently processed by the host(s) in the system. The main function of the module is to convert between 'global events' (assertion and de-assertion events transmitted on the event-transport-lane (ETL) bus) and 'local events' (level sensitive signals on output, and level or edge sensitive signals on input).

Table 11-78. INTAGGR Allocation Within Device Domains

Module Instance	Parameters	
	MCU	MAIN
DMSS0_INTAGGR0	-	✓(DMSS)

11.2.4.1.1 INTAGGR Features

The DMSS0_INTAGGR0 supports the following features:

- 64-bit VBUSP target using 64-bit registers
- Provides a set of TI Interrupt Architecture compliant interrupt status and mask register sets which are used to pass specific event status to one or more Host blocks.
  - Maps a collection of DMA Messaged Events which are input through an Event Transport Lane into specific bit locations in one or more interrupt cause registers
  - Mapping is performed based on a programmable table which provides a single location for each ordinal input event number (0 through sevt_cnt-1)
    - Table specifies a specific bit in a specific cause register that the event should set or clear depending on the type of event (up vs down)
    - Tracks a single 'event up' / 'event down' condition. There is no event counting. (The 'cnt' field of the ETL is ignored.)
  - Tracked status interrupts are presented to the user through a standard interrupt register interface.
    - Provides separate 'enable set' and 'enable clear' registers.
    - Provides both masked and unmasked interrupt status.
    - Interrupt status bits can be manually cleared using 'write 1 to clear'.
- Provides an optional set of Unmapped Event (UNMAP) which can take an 'unmapped' event from the ingress ETL and generate a Global event on the egress Event Transport Lane (ETL) interface.
  - Each ingress event can generate an egress Global event on the egress ETL, controllable through a mapping register.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.
- Provides an optional set of Global Event Input (GEVI) counters which can count events which were delivered via an ingress Event Transport Lane (ETL).
  - Each counted event provides an MMR by which the count can be read and an MMR by which a specified amount can be decremented by the host.
  - Each counted event generates an egress Global event on a zero to non-zero and non-zero to zero transition, controllable through a mapping register.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.
- Provides an optional set of Global Event Input (GEVI) 'Multicast' registers which can take a Global event from an ingress ETL and generate two egress Global events on the egress ETL interface.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.

- Provides an optional set of Local Event Input (LEVI) to Global event registers which can be used to convert pulsed discrete interrupt inputs or clock synchronous rising edge events into Global events on an egress ETL.
  - Each ingress event index provides a configurable 'pulse' or 'rising edge' bit, plus the configurable index of the generated Global event.
- Supports dynamic clock gating via

11.2.4.1.2 INTAGGR Parameters

Table 11-79 shows the Interrupt Aggregator 0, parameters set during design time.

Table 11-79. Interrupt Aggregators Parameters

Module Instance	Parameters				
	VINTR[1]	SEVI[2]	GEVI[3]	LEVI[4]	MEVI[5]
DMSS0_INTAGGR0	184	1536	256	32	128

(1) VINTR – Number of Virtual Interrupt outputs. These are connected to the interrupt router inputs. Value can be read from INTAGGR_INTCAP register.

(2) SEVI – Number of Main (Steerable) Events. Value can be read from INTAGGR_INTCAP register.

(3) GEVI – Number of Countable Events. Value can be read from INTAGGR_AUXCAP register.

(4) LEVI – Number of Local Event inputs. Value can be read from INTAGGR_AUXCAP register.

(5) MEVI – Number of Multicast Events. Value can be read from INTAGGR_AUXCAP register.

11.2.4.2 INTAGGR Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

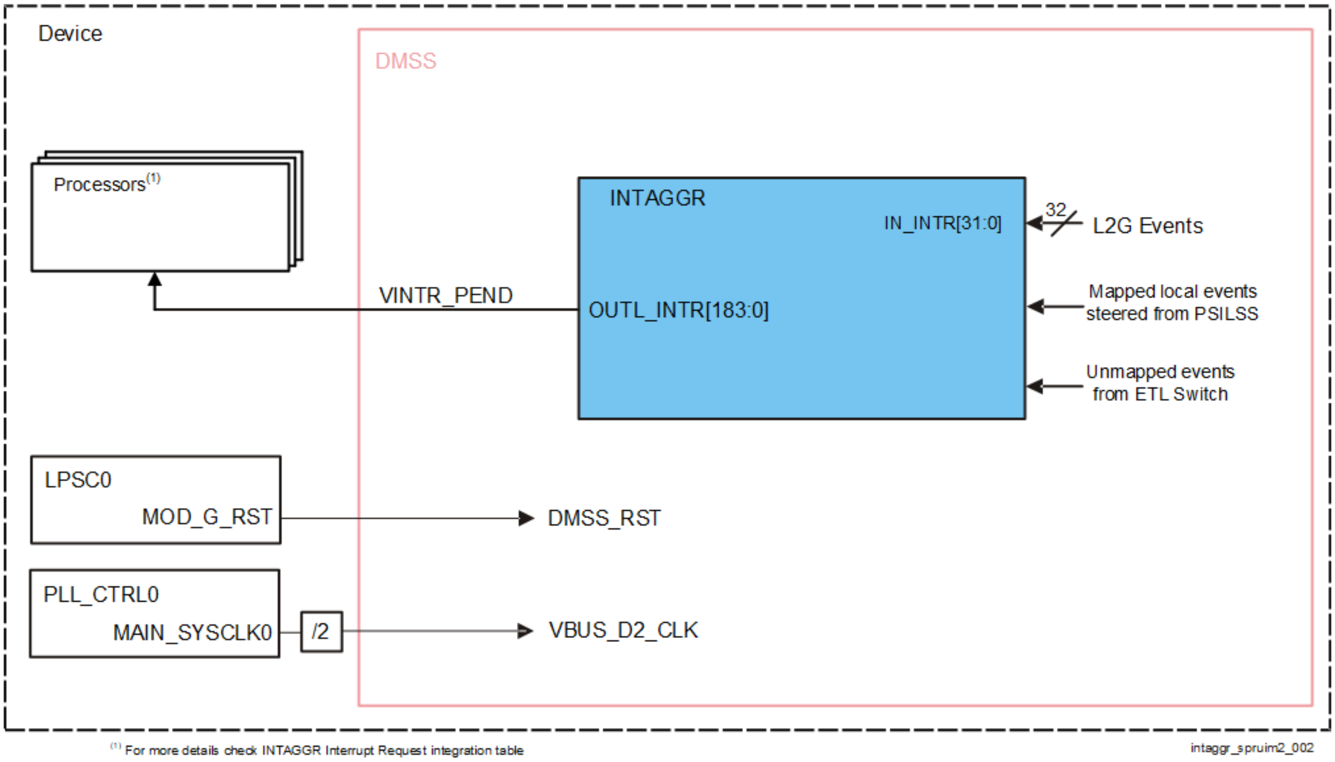

Figure 11-12. DMSS0_INTAGGR0 Integration

11.2.4.2.1 INTAGGR Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Local Power Sleep Controller (Module Domain)	SoC Interconnect
DMSS0_INTRAGGR0	PSC0	PD0(GP)	LPSC0	CBASS0

11.2.4.2.2 INTAGGR Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
DMSS0_INTRAGGR0	INTAGGR_FICLK	VBUS_D2_CLK	MAIN_SYSCLK0/2	INTAGGR clock. This clock is used for all interface and functional operations.

11.2.4.2.3 INTAGGR Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
DMSS0_INTRAGGR0	INTAGGR_RST	MOD_G_RST	LPSC0	INTAGGR hardware reset

11.2.4.2.4 INTAGGR Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
DMSS0_INTAGGR0	VINTR_PEND[183:168]	NVIC_IN[47:32]	MCU_M4FSS0_CORE0	Level	VINTR_PEND[183:168] interrupts to NVIC_IN
	VINTR_PEND[39:0]	SPI_IN[103:64]	GICSS0	Level	VINTR_PEND[39:0] interrupts to GIC SPI
	VINTR_PEND[71:40]	INTR_IN[95:64]	R5FSS0_CORE0	Level	VINTR_PEND[79:40] interrupts to R5FSS0 CORE0
	VINTR_PEND[79:72]	INTR_IN[15:8]			
	VINTR_PEND[87:80]	INTR_IN[15:8]	R5FSS0_CORE1	Level	VINTR_PEND[87:80][71:40] interrupts to R5FSS0 CORE1
	VINTR_PEND[71:40]	INTR_IN[95:64]			
	VINTR_PEND[127:120]	INTR_IN[16:8]	R5FSS1_CORE0	Level	VINTR_PEND[127:88] interrupts to R5FSS1 CORE0
	VINTR_PEND[119:88]	INTR_IN[95:64]			
	VINTR_PEND[135:128]	INTR_IN[15:8]	R5FSS1_CORE1	Level	VINTR_PEND[135:128][119:88] interrupts to R5FSS1 CORE1
	VINTR_PEND[119:88]	INTR_IN[95:64]			
	VINTR_PEND[151:136]	DMSC_lite[15:0]	DMSC_lite	Level	VINTR_PEND[151:136] interrupts to DMSC_lite
	VINTR_PEND[159:152]	PR1_SLV_IN[7:0]	PRU_ICSSG0	Level	VINTR[159:152] interrupts to PRU_ICSSG0 PR1
	VINTR_PEND[167:160]	PR1_SLV_IN[7:0]	PRU_ICSSG1	Level	VINTR[167:160] interrupts to PRU_ICSSG1 PR1

11.2.4.2.5 INTAGGR DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Type	Description
DMSS0_INTRAGGR0	-	-	-	-	No PDMA channels to extrernal DMA engines

11.2.4.3 INTAGGR Functional Description

The Interrupt Aggregator (INTAGGR) provides a centralized machine which handles the termination of system events to that they can be coherently processed by the Host(s) in the system. Both the signaling and content of TI system events are incompatible with standard interrupt controllers. The INTAGGR provides mechanisms which convert the TI proprietary system events to standard level sensitive pending bits which can be used by all downstream interrupt infrastructure. Events can be presented to the INTAGGR in two different forms:

- Events may be active high pulses, or clock synchronous rising edges, which are input on separate orthogonal pins. These are called 'Local Events'.
  - Local event signals that are used in pulse counting mode must be sourced by the same clock as the interrupt aggregator.
  - Local event signals that are used in edge counting mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the interrupt aggregator clock, and they must remain high for at least 1 'slow' clock cycle.
- Events may be messages which are input in time division multiplexed sequential order from an Event Transport Lane. These are called 'Global Events'.

In both cases, these events need to be conditioned to transition them from a transient indicator that something occurred to a persistent and reliable indication of the current state of the system. The IA is architected to perform this conversion in an efficient and cost effective manner.

11.2.4.3.1 Submodule Descriptions

1.7.3.1.1 Status/Mask Registers

The Status and Mask Registers block is responsible for providing persistent storage for the interrupt status and mask bits and for formatting those in a way that is compliant to the TI Interrupt Architecture requirements. These requirements include the ability to set and clear bits orthogonally and to provide a masked version of the status register that corresponds to the supplied bit mask for each register.

1.7.3.1.2 Interrupt Mapping Block

The Interrupt Mapping Block accepts ordinally numbered events (0-N) and converts those ordinal event numbers into a status register number and bit number pair that is then used to manipulate the specified bit in the Status Registers block.

1.7.3.1.3 Global Event Input (GEVI) Counters

The GEVI Counters block is responsible for accepting an Event Transport Lane events and summing the total message counts for each received event index. The module creates global egress events for zero to non-zero count up' events and non-zero to zero 'count down' events. The egress global event index is configured via GEVI[a]_MCMAP register, so count status egress events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

1.7.3.1.4 Local Event Input (LEVI) to Global Event Conversion

The Local to Global event block is responsible for accepting an array of input pins and independently counting the number of cycles for which those pins are asserted high, or by counting individual clock synchronous rising edge events. The counting mode is configurable on a 'per pin' basis. The events are converted to egress Global events on an egress ETL. Global events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

1.7.3.1.5 Global Event Multicast

The Global event multicast block takes an ingress global event from an ingress ETL, and maps it into two egress Global events on two egress ETL interfaces. Global events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

11.2.4.3.2 General Functionality

1.7.3.2.1 Event to Interrupt Bit Steering

Each time an event message is received on the Main Event Transport Lane interface, the interrupt mapping block performs a direct lookup into an SRAM using the event number as the address. The SRAM stores a corresponding interrupt status (INTR_STATUSM) register and bit number within that register (VINT[a]_STATUS_MSKD) which are to be manipulated anytime a message is received indicating something occurred on that specific event. When an up event is received, the specified bit in the [a] Status register will be set. When a down event is received, that same bit will be cleared. This block is what allows flexible aggregation of various system events into an array of bits in the interrupt status registers. It is intended that this mapping is essentially static - set up when a resource is allocated and left untouched until the resource is no longer needed. Note that the 'cnt' field of the ETL is ignored and no interrupt counting is performed here. When 'UpDn=1', the interrupt flag bit is set, and when 'UpDn=0', the flag bit is cleared.

1.7.3.2.2 Interrupt Status

The event messages which are generated from the event to interrupt bit steering logic are input to the Interrupt Status registers. Each time an event is received, the interrupt status registers machine will assert or de-assert the specified bit in the specified register. The assertion and de-assertion in the interrupt status register is unaffected by the interrupt enable state. When an up event is received, the corresponding bit is set and when a down event is received, the corresponding bit is cleared. Some sources of input events will not include the ability to send a down event. In these cases, the interrupt router provides the ability to clear the status bits through the Interrupt Source Clear register (VINT[a]_STATUS). The host will write a one to the specific bit in the register which is to be cleared and the interrupt status machine will clear the bit internally. It is not intended that the Host directly clear bits which are automatically cleared via down events from the source itself.

1.7.3.2.3 Interrupt Masked Status

Interrupt enable bits are used in conjunction with the interrupt status bits to create the interrupt masked status register values. The interrupt masked status register (VINT[a]_STATUS_MSKD) contains the value of the interrupt status ANDed with the value of the interrupt enable register (VINT[a]_ENABLE_SET). Each time a new event message is received from the event to interrupt bit steering logic or the interrupt enable register is modified, the interrupt masked status register is re-evaluated.

1.7.3.2.4 Enabling/Disabling Individual Interrupt Source Bits

Separate (VINT[a]_ENABLE_SET and VINT[a]_ENABLE_CLR) registers are provided to allow individual enable bits to be enabled or disabled without the need for a read-modify-write operation. When the VINT[a]_ENABLE_SET register is written, all bits within written bytes which are 1 will cause corresponding bits in the internal enable register to be set. When the VINT[a]_ENABLE_CLEAR register is written, all bits within written bytes which are 1 will cause corresponding bits in the internal enable register to be cleared.

1.7.3.2.5 Interrupt Output Generation

Each interrupt masked status register (VINT[a]_STATUS_MSKD) is accompanied by a single pending bit which indicates if any enabled interrupt source within the corresponding interrupt status register is currently asserted. These pending bits from the interrupt masked status registers are collectively output from the INTRAGGR as the VINTR_PEND bus. The interrupt status outputs will always be updated to reflect the current values of the VINT[a]_STATUS_MSKD register. This is accomplished by triggering output updates on write operations to the internal RAM that holds the current raw status and enable masks.

1.7.3.2.6 Global Event Counting

When enabled, the INTAGGR will provide a set of counters which will track how many outstanding messages have been observed for each ingress event index from the ingress Counted Global Event Transport Lane (ETL) interface. For each message received where the 'UpDn' flag is set, the corresponding counter will be incremented by value of the 'cnt' field of ingress message. Events where the 'UpDn' flag is cleared are ignored. The counter is made visible to software in the GEVI[a]_COUNT register. When software has read the count, it can acknowledge that count has been seen and processed by writing back an integer value specifying the amount by which the counter should be decremented, and the counter will subtract that value from the current count (which may have updated since it was read). The count will saturate at a value of 0xFFFFFFFF. Writing a count 'ack' value higher than the one read is not supported and will produce non-deterministic results.

When a count transitions from zero to a non-zero value, a Global Up 'UpDn=1' event is sent out an egress ETL interface. When a count transitions from a non-zero value to zero, a down 'UpDn=0' event will be sent. The index of the Global event is mappable on a 'per-counter' basis, using the GEVI[a]_MAP register. The event may be mapped such that it then re-enters INTAGGR's 'Event to Interrupt Bit Steering Block' to generate an interrupt to the host. The event routing is handled by an external event switch fabric. Note that writing a new egress event index via the GEVI[a]_MAP register does not alter the stored event count for the ingress event register index.

1.7.3.2.7 Local Event to Global Event Conversion

When enabled, the INTAGGR will provide a set of Local to Global event conversion registers. Local events may be discrete clock synchronous pulses or clock synchronous rising edges. The counting mode is configurable on a 'per pin' basis. In pulsed mode, the module will track how many outstanding clock cycle long pulses have been observed on each of the provided levi interface pins. For each cycle in which a LEVI input pending bit is asserted the corresponding counter will be incremented by 1. In 'rising edge' mode, the number of rising edge transitions on the pin is counted.

The module will generate egress Global events on its egress ETL, with a different global index configured for each ingress LEVI pin. The LEVI pins numbers (1-N) are converted to arbitrary global event indices via the global event mapping LEVI[a]_MAP registers. The egress Global events can themselves be mapped to re-enter the INTAGGR's Global Event Counting block, so that the counts can then be made visible to software in the GEVI count registers as described in Section 10.2.7.3.1.3. The event routing is handled by an external event switch fabric.

1.7.3.2.8 Global Event Multicast

In DMSS0_INTAGGR0, the INTAGGR will provide a set of Global event multicast (GEVI[a]_MCMAP) registers. These registers allow an ingress Global event on its ingress ETL interface to be mapped into two egress Global events on two separate egress ETL interfaces. A set of registers map the ingress Global event index (1-N) into two arbitrary egress event indices.

11.2.5 Packet Streaming Interface Link (PSI-L)

This section describes the Packet Streaming Interface Link (PSI-L) for the device.

11.2.5.1 PSI-L Overview

PSI-L is a packet based protocol used to transfer data between several device modules. Each transaction is routed based on thread ID value instead of physical address. All PSI-L interfaces are point to point direct connections to DMSS0. All switching functions among the PSI-L based interfaces are done inside DMSS0.

The PSI-L also has an event interface referred to as ETL, which is purely used to transfer event information.

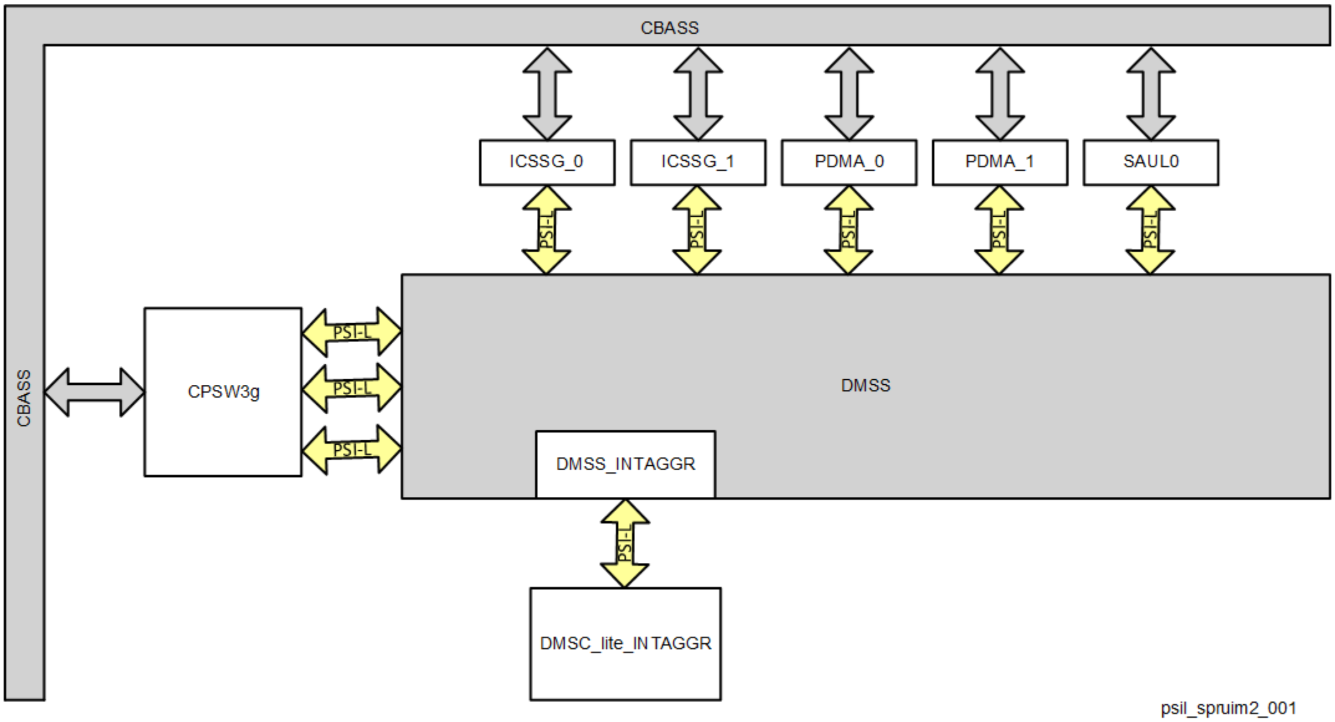

Figure 11-13. PSI-L Overview

11.2.5.2 PSI-L Functional Description

11.2.5.2.1 PSI-L Introduction

The PSI-L is used to transfer words of packet data and control information between two peer entities via direct connection. There are credits used for flow control to guarantee that blocking does not occur between threads. Multiple packet transfers can be ongoing simultaneously across a PSI-L interface each on a separate logical thread but all sharing a single datapath through time division multiplexing. Each packet which is transferred is accompanied by a destination thread ID which indicates the logical destination thread to which the packet is being sent.

There is low level hardware handshake between PSI-L initiator and target used for transfering data. As it is blocking by nature, a higher level protocol is also used in which credits are maintained for each thread connection. Moments of non-readiness are allowed on the interface but there is no possibility that one thread can block another for an indefinite time since a thread must have credit for the destination before it is allowed to use the interface.

Figure 11-14 illustrates the point to point PSI-L connection.

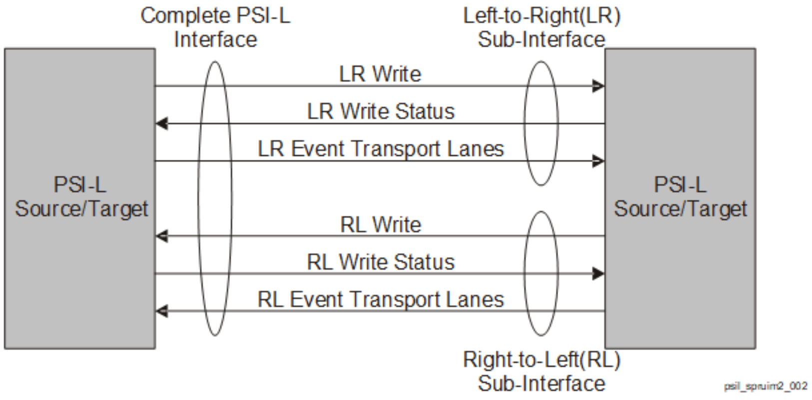

Figure 11-14. PSI-L Connection

PSI-L is intended to be a versatile interface which can carry various types of communications. The following table describes several types of threads which have been defined.

Table 11-80. Types of PSI-L Threads

Type	Description	Example Endpoints
Queue Management (QM) Messaging	Provides transport for queue push, pop, and divert messages to support distributed queue based work passing	Centralized queue manager or message manager and distributed DMA clients
Direct IO	Allows for tunneling CBASS compatible bus transactions through a PSI interconnect	Module which has no CBASS initiator to a remote proxy block
DMA Control Transport	Provides transport for DMA transfer descriptions from a source thread to a destination thread	DMA channel controller to DMA transfer controller
DMA Data Transport	Provides transport for packed data from a source thread to a destination thread	Packet oriented module like networking adapters to or from centralized DMA

Each thread on PSI-L is established between a single thread initiator and a single thread target using a connection oriented transfer mechanism. A thread initiator and a thread target are "paired" to create a logical connection between them referred to as a thread. Pairing is accomplished using a Pair Configuration Message which is valid in all thread types. Pairing can only occur between a thread initiator and a thread target of the same type.

11.2.5.2.2 PSI-L Operation

The PSI-L allows multiple independent streams of packet data (threads) to share a single interface using data phase granularity time division multiplexing. This time division multiplexing is accomplished by dividing each stream into single data transfers. In this way a stream is comprised of a sequence of strongly ordered data transfers but packet transfers between different streams are allowed to be interleaved. Each data phase is qualified with a type identifier which indicates whether the data is packet info, direct IO write or read info, timestamp, software info, control data, payload data, or status.

Event Transport

PSI-L provides a mechanism by which events can be transported within one or more optional subinterfaces on a link. These sub-interfaces are referred to as event transport lanes (ETLs) and are independent of any PSI-L packet or message transfers which may be ongoing on the other interfaces within the PSI-L. A maximum of one event can be transferred on each event transport lane in each clock cycle. The event transport protocol is a simple request-ready type of hwardware handshake.

Threads

A thread is a complete flow-controlled stream of communication. The PSI-L thread space is divided into a 32K contiguous region representing all of the source threads (0x0000 - 0x7FFF) and a 32K contiguous region representing all of the destination threads (0x8000 - 0x8FFF).

Source threads are responsible for sending request transactions, accepting response transactions, and sending data transfer transactions. Destination threads are responsible for accepting request transactions, sending response transactions, and accepting data transfer transactions. A given thread generally performs only a single class of transactions (see *Types of PSI-L Threads*). Both source and destination threads may act as initiators for transfers on one of the PSI-L write sub-interfaces but in this case source threads are actually initiating data transfers while destination threads are only responding to a previous request issued by a source request. Source threads only transfer to destination threads and destination threads only transfer to source threads. Transfers between same thread types do not occur.

The following types of message transfers always originate from source threads and terminate in destination threads:

- Configuration write message
- Configuration read message
- QM push message
- QM pop message
- QM divert message
- Direct read operation message
- Direct write operation message
- DMA transfer request message
- DMA data message

The following types of message transfers always originate in destination threads and terminate in source threads:

- Configuration write response message
- Configuration read response message
- QM push response message
- QM pop response message
- QM divert response message
- DMA transfer response message

Arbitration Protocol

On each cycle, an arbiter built into the initiator side of each interface decides on which thread to transfer data in the next clock cycle. Both forward (from source threads) and reverse (from destination threads) direction transfers can occur across the same physical interface so the arbiter must ensure that sustained blocking of any thread can occur.

The decision about which thread to allow using the interface is based on the following factors:

1. Whether data is ready at the source to be sent
2. Whether credit exists for the thread such that it is guaranteed there is a place for the data to land in the destination endpoint. For reverse direction transfers (response messages), it is assumed that credit always exists.
3. The relative priority of the traffic that the thread is carrying for the given packet duration
4. Whether the transfer is for a forward or reverse direction thread (requests versus responses).

No thread can be considered for inclusion in arbitration unless both data is available and credit exists in the destination endpoint. For each thread which can be considered in the current arbitration cycle, the arbiter should then pick the thread with the highest priority. Reverse transfers should be considered higher priority than forward transfers.

Thread Configuration

Each source thread has programmable registers for configuring the pairing with a corresponding destination thread and for enabling data flow. Each destination thread has programmable registers for reporting the buffering capability of the thread and for enabling data flow. These registers are accessed using configuration read and write messages from a configuration host.

Each configuration write message sent from a configuration host is acknowledged with a configuration write response message from the addressed endpoint. Each configuration read message sent from a configuration host is acknowledged with a configuration read response message from the addressed endpoint.

Thread Pairing

Depending on the type of traffic that each source thread carries it may or may not have a fixed pairing with a destination thread.

Configuration Transaction Pairing

Configuration write and read transactions are only initiated by a special module called configuration proxy (PSILCFG_PROXY). Each configuration proxy in the system uses a single source thread which can initiate configuration write and read transactions to the configuration registers of every other source and destination thread in the PSI-L system. The PSILCFG_PROXY registers are described in DMASS_PSILCFG_0 Registers.

Each source thread routes to a single target thread and this pairing is specified by programming a required pairing register set for each thread. A source has no ability to change what target thread it talks to. If a source must be able to talk to different targets (or target threads), then it can either have multiple threads or a streaming switch that can be programmed to route the transfers appropriately based on specific packet fields.

Configuration Registers Region

The configuration registers region contains static configuration information including the settings for linking a thread source to a thread destination. These registers are described in **PSI-L Configuration Registers**. The thread ID mapping is shown in *System Thread Map for All PSI-L Threads*

11.3 Peripheral DMA (PDMA)

This chapter describes the PDMA architecture in the device.

11.3.1 PDMA Controller

11.3.1.1 PDMA Overview

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers (MMRs) accessed via a standard non-coherent bus fabric. The PDMA module is located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured transfer request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer DMSS destination channel which then performs the movement of the data into memory. Likewise, a remote DMSS source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (DMSS + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

There are two PDMA modules in the device. Table 11-81 shows PDMA allocation across device domains.

Table 11-81. PDMA Allocation across Device Domains

PDMA Instance	Serviced Peripherals	Domain	
		MCU	MAIN
PDMA0	SPI0 through SPI3, UART0, UART1	–	✓
PDMA1	SPI4, UART2 through UART6, MCAN0, MCAN1, ADC0	–	✓

The PDMA is linked to the DMSS through a direct PSI-L connection. For more details, refer to *Packet Streaming Interface Link (PSI-L)*.

11.3.1.1.1 PDMA Features

11.3.1.1.1.1 PDMA0 Features

The PDMA0 module supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit (write unit 0)
  - Provides a 32-bit wide VBUSP write-only initiator interface for peripheral accesses
  - Supports write burst up to 64 bytes (on selected channel types)
- Provides 1 memory read access unit (read unit 0)
  - Provides a 32-bit wide VBUSP read-only initiator interface for peripheral accesses
  - Supports read burst up to 64 bytes (on selected channel types)
  - Supports 1 outstanding read
- Supports up to 18 simultaneous destination (Tx) channels
- Supports up to 18 simultaneous source (Rx) channels
- Supports static transfer requests (TR) only
- Supports X-Y transfer mode only (does not support MCAN and AASRC modes)
- Provides per-channel buffering:
  - Provides 8×128-bit word deep data FIFO for each destination channel
  - Provides 8×128-bit word deep data FIFO for each source channel
- Provides 128-bit wide PSI-L compliant data interface to and from DMSS endpoints and remote peripherals

- Provides ECC support

11.3.1.1.1.2 PDMA1 Features

The PDMA1 module supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit (write unit 0):
  - Provides a 32-bit wide VBUSP write-only initiator interface for peripheral accesses.
  - Supports write bursts up to 64 bytes (on selected channel types)
- Provides 1 memory read access unit (read unit 0)
  - Provides a 32-bit wide VBUSP read-only initiator interface for peripheral accesses
  - Supports read burst up to 64 bytes (on selected channel types)
  - Supports 1 outstanding read
- Supports up to 15 simultaneous destination (Tx) channels
- Supports up to 17 simultaneous source (Rx) channels
- Supports static transfer requests (TR) only
- Supports X-Y and MCAN transfer modes (does not support AASRC)
- Provides per-channel buffering:
  - Provides 8×128-bit word deep data FIFO for each destination channel
  - Provides 8×128-bit word deep data FIFO for each source channel
- Provides 128-bit wide PSI-L compliant data interface to and from DMSS endpoints and remote peripherals
- Provides ECC support

11.3.1.2 PDMA Integration

This section describes the PDMA integration in the device, including information about clocks, resets, and hardware requests.

11.3.1.2.1 PDMA Integration in MAIN Domain

Figure 11-15 shows the integration of the PDMA modules in the device MAIN domain.

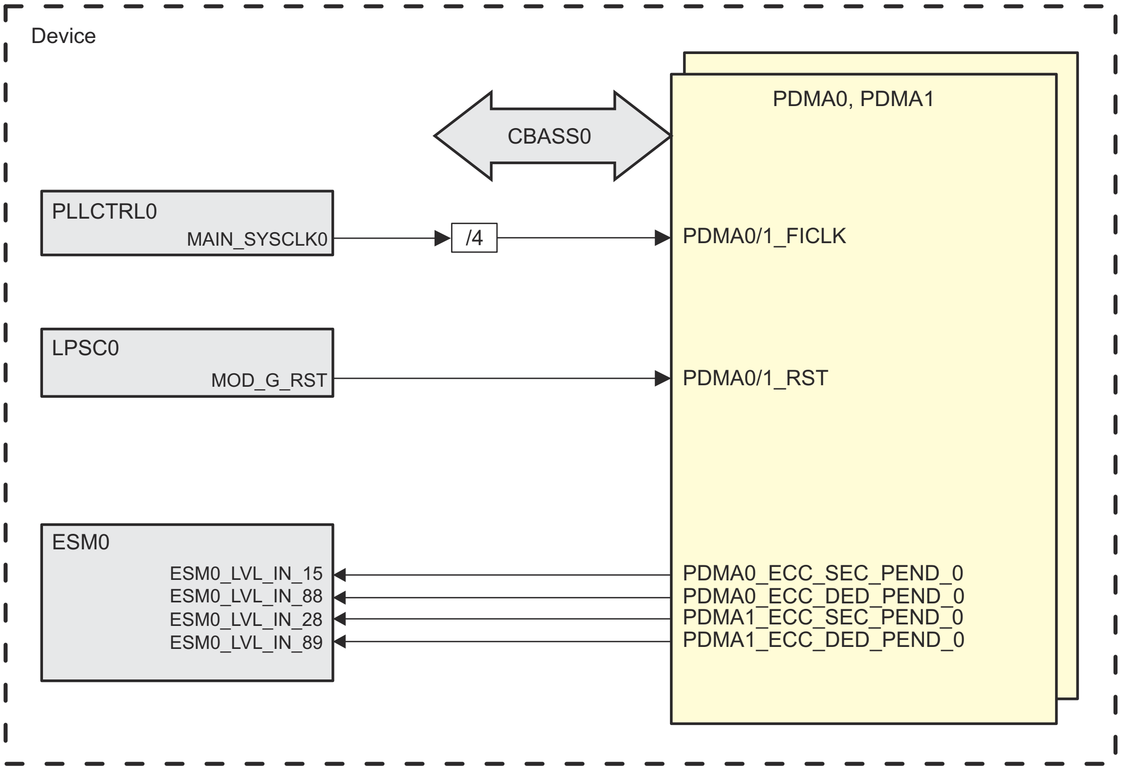

Figure 11-15. MAIN Domain PDMA Integration

Table 11-82 through Table 11-86 summarize the integration of the PDMA modules in the device MAIN domain.

Table 11-82. PDMA Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
PDMA0	PSC0	PD0	LPSC0	CBASS0
PDMA1	PSC0	PD0	LPSC0	CBASS0

Table 11-83. PDMA Clocks

Clocks				
Module Instance	Module Clock Input	Source Clock Signal	Source	Description
PDMA0	PDMA0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	PDMA0 functional and interface clock
PDMA1	PDMA1_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	PDMA1 functional and interface clock

Table 11-84. PDMA Resets

Resets				
Module Instance	Module Reset Input	Source Reset Signal	Source	Description
PDMA0	PDMA0_RST	MOD_G_RST	LPSC0	PDMA0 hardware reset
PDMA1	PDMA1_RST	MOD_G_RST	LPSC0	PDMA1 hardware reset

Table 11-85. PDMA Interrupt Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Type**	**Description**
PDMA0	PDMA0_ECC_SEC_PEND_0	ESM0_LVL_IN_15	ESM0	Level	PDMA0 SEC ECC error interrupt
	PDMA0_ECC_DED_PEND_0	ESM0_LVL_IN_88		Level	PDMA0 DED ECC error interrupt
PDMA1	PDMA1_ECC_SEC_PEND_0	ESM0_LVL_IN_28	ESM0	Level	PDMA1 SEC ECC error interrupt
	PDMA1_ECC_DED_PEND_0	ESM0_LVL_IN_89		Level	PDMA1 DED ECC error interrupt

Table 11-86. PDMA DMA Event Requests

DMA Input Events	
PDMA0	See for mapping of DMA events to PDMA0 inputs
PDMA1	See for mapping of DMA events to PDMA1 inputs
PDMA_DEBUG	See for mapping of DMA events to PDMA_DEBUG inputs

Note

For a description of the interrupt source, see *Interrupt and DMA Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

For more information on the device DMA controllers, see *DMA Controllers*.

11.3.1.3 PDMA Functional Description

11.3.1.3.1 PDMA Functional Blocks

Figure 11-16 shows the PDMA block diagram.

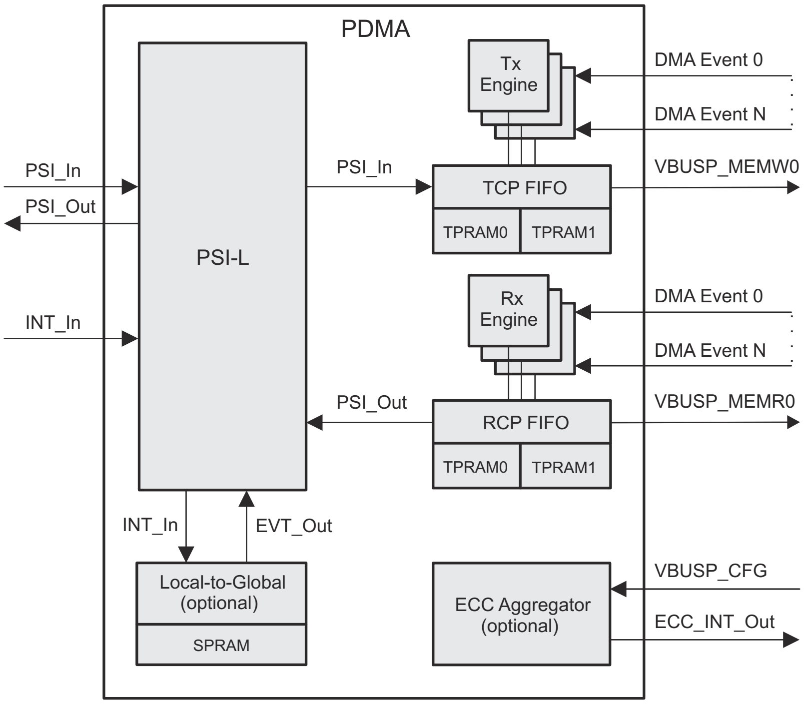

Figure 11-16. PDMA Block Diagram

Note

For detailed description of the PSI-L interface, see *Packet Streaming Interface Link (PSI-L)*.

11.3.1.3.1.1 Scheduler

The scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low-level read or write operation.

11.3.1.3.1.2 Tx Per-Channel Buffers (TCP FIFO)

The Tx per-channel buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx per-channel buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.3.1.3 Tx DMA Unit (Tx Engine)

The Tx DMA unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming DMA event and then writes data from the Tx per-channel data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters, which have been programmed via PSI-L into the static TR for the channel.

11.3.1.3.1.4 Rx Per-Channel Buffers (RCP FIFO)

The Rx per-channel buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte-oriented on write so that the data from the Rx DMA units, which may not be full words, can be packed properly. The buffers are word-oriented on read in accordance with the transport mechanism outlined in the PSI-L interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface.

The Rx per-channel buffers block outputs queue fullness information to the scheduler block, which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Rx per-channel buffers will initiate transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block will simultaneously monitor the status of all of the threads and will perform a round-robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer will be included in the arbitration.

11.3.1.3.1.5 Rx DMA Unit (Rx Engine)

The Rx DMA unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx per-channel data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters, which have been programmed via PSI-L into the static TR for the channel.

11.3.1.3.2 PDMA General Functionality

11.3.1.3.2.1 Operational States

At any given time the PDMA can be in one of three different states as follows:

- INIT: This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the INIT state, the DMA will de-assert all 'ready' signals on all applicable target interfaces and will de-assert all 'request' signals on all applicable controller interfaces. The PDMA will automatically transition out of the INIT state into the IDLE state when all of the RAM initialization has been completed.
- IDLE: Once the PDMA leaves the INIT state, it enters the IDLE state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The IDLE state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. As channels have work queued on them and transactions begin flowing into the system, the PDMA transitions to the ACTIVE state. When no more work is pending, or when the host pauses/disables active channels, or when the power management complex on the SoC desires to shut down the PDMA and asserts 'clock stop request', the PDMA will account for any outstanding transactions and will re-enter the IDLE state. The PDMA leaves the IDLE state anytime it generates or receives a transactions that requires a return response as those protocols dictate that the clock must remain running to avoid faulting the handshaking protocol.
- ACTIVE: The PDMA enters the ACTIVE state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent), the PDMA transitions to the IDLE state.

11.3.1.3.2.2 Clock Stop

The clock stop interface is a request/acknowledge interface used to coordinate the handshaking of properly stopping the main clock to the IP. Before attempting to perform a clock stop operation, software is required to teardown all active channels (via 'real time' registers in the BCDMA/PKTDMA, or PSIL register 0x408 in PSIL based peripherals), and after this is complete, also clear the global enable bit for all channels (via PSIL register 0x2 in BCDMA/PKTDMA and PSIL based peripherals). Attempting a clock stop on the IP without first performing the channel teardowns or clearing of global enable bits will result in IP specific behavior that may be UNDEFINED.

The PDMA will not drive clock stop IDLE or clock stop ACK while the global enable (PSIL register 0x2) is set for any channel.

11.3.1.3.2.3 Emulation Control

The emulation control input (EMUSUSP) and the per-channel emulation control FREE bit allow PDMA operation to be suspended on a per-channel basis. When the emulation suspend state is entered, the PDMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR.

Emulation control is implemented for compatibility with other peripherals. Each source and desintaion channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is conrolled via the PDMA_PSILCFG_TX_RT_ENABLE / PDMA_PSILCFG_RX_RT_ENABLE[0] FREE bit.

11.3.1.3.3 PDMA Events and Flow Control

The following sections describe the simplified mechanism that is provided on the PDMA for triggering and completion event generation.

11.3.1.3.3.1 Channel Types

Each channel in the PDMA is configured at design time (and cannot be changed by software) to be either standard X-Y FIFO mode or MCAN channel or AASRC channel. Either of these two sections provide information about the channel type support in the device: *PDMA Features* and *PDMA Sources*.

When reading the sections below, ignore any information that concerns unsupported channel type.

11.3.1.3.3.1.1 X-Y FIFO Mode

Most peripherals which are serviced by the PDMA follow the pattern of transferring 'X' bytes from a fixed, non-changing address in a burst 'Y' times for each triggering event that is received. The 'X' parameter is typically 1-16 bytes and the 'Y' parameter can be any integer up to 2048.

11.3.1.3.3.1.2 MCAN Mode

The MCAN module is found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the PDMA will start out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, there is an MCAN packet fragmentation requirement to place an 8-byte header on each 64-byte chunk that is transmitted and to remove the header from each 64-byte chunk (other than the first block) that is received.

11.3.1.3.3.2 Channel Triggering

Channels must be triggered in order for them to perform work. A local event input bus is provided on the PDMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, etc.).

The PDMA provides a 2-bit counter per event input to accommodate startup latency in the channel.

11.3.1.3.3.3 Completion Events

All transfers on PDMA are split TRs in that they have a paired-DMA half and a (static) PDMA half. Completion events are designed to be triggered from the paired-DMA half of the split TR.

11.3.1.3.4 PDMA Transmit Operation

11.3.1.3.4.1 Destination (Tx) Channel Allocation

A total of *N* destination channels are provided within the PDMA for concurrent transfers from Tx per-channel buffers to the various attached peripherals, where *N* is a design-time configurable paramater. Each Tx channel requires a single PSI-L thread. See *PDMA Sources* for Tx channel allocation for each PDMA.

11.3.1.3.4.2 Destination (Tx) Channel Out-of-Band Signals

Table 11-87 shows how PSIL signals are handled for destination channels.

Table 11-87. Tx Channel Out-of-Band Signals

PSI-L Signal	XY/AASRC Mode	MCAN Mode
SOP	Ignored	Ignored
EOP	Ignored	Closes current MCAN packet
SOL	Ignored	Ignored
EOL	Ignored	Ignored
DROP	Ignored	Ignored
PKT_ERROR	Ignored	Ignored
PAUSE	Ignored	Ignored
TDOWN	Reflect in status; teardown when data marker reached	Reflect in status; teardown when data marker reached

11.3.1.3.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the host will need to first pair the channel with a remote data source (normally a paired-DMA channel), setup the static TR for the channel, and enable the thread.

11.3.1.3.4.3.1 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The host will pair each destination PDMA channel with (typically) a corresponding source channel in the paired-DMA. The PDMA thread is configured to point to the paired-DMA thread and the paired DMA thread is configured to point to the PDMA thread. Once paired, the source channels in the paired-DMA will send all their data to the destination channel in the PDMA and the destination channel in the PDMA will never see any data other than data from the source channel in the paired-DMA.

The following PSI-L registers are related to destination thread pairing:

- PDMA_PSILCFG_TX_ENABLE
- PDMA_PSILCFG_TX_CAPABILITIES
- PDMA_PSILCFG_TX_BYTE_COUNT
- PDMA_PSILCFG_TX_RT_ENABLE

Refer to their descriptions for further details.

11.3.1.3.4.3.2 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the host will send configuration transactions across PSI-L and will setup the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of 'X' and 'Y' parameters, but the field interpretation varies somewhat. The following PSI-L register bit fields are used to setup the static TR:

- PDMA_PSILCFG_TX_STATIC_TR[26-24] X
- PDMA_PSILCFG_TX_STATIC_TR[11-0] Y

Refer to their descriptions for further details.

11.3.1.3.4.3.3 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled in order to accept data. Threads are enabled or disabled by setting or clearing the ENABLE bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.3.4.4 Data Transfer

Packet transmission is accomplished within the PDMA by unpacking and moving data from the Tx per-channel FIFOs which were filled via the transmit PSI-L interface to specified memory mapped address ranges via the VBUSP controller interfaces. On the Tx side of the PDMA, these transfers are always writes. Each write transfer which is performed by the Tx DMA unit is to a destination address that is hardcoded in the channel at design time and of a size as specified in the static transfer request.

The sequences of logical transactions that are performed by the PDMA on the memory interface during transmit is dependent on the channel type. The following sections describe what will happen for the two different channel types.

11.3.1.3.4.4.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter writes of 'X' parameter bytes to the data FIFO address specified for the channel. Each write that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The write transfers that are performed will be accomplished as quickly as possible given availability of data in the Tx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.3.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting the PDMA_PSILCFG_TX_STATIC_TR[31] BURST bit enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2×32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.3.4.4.2 MCAN Mode Channel

The PDMA channel will remain idle until data is received from the paired-DMA over the PSIL interface. At this time, the PDMA will imediately start copying packet bytes into the MCAN TX buffer corresponding the PDMA/ MCAN channel. The number of bytes copied is smaller of the remaining bytes in the packet or the value of the 'Y' parameter. Once a TX buffer has been filled, the PDMA will transfer ownership of the buffer to MCAN by performing an MCAN register write. The PDMA will then wait to regain ownership of the TX buffer by waiting for the corresponding MCAN TX event. At this time, the PDMA will continue with refilling the TX buffer for the next packet fragment. On subsequent fills (until the end of packet is reached), the PDMA will skip over the 8-byte MCAN header, leaving the original contents from the intial fragment copy in place.

11.3.1.3.4.4.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.3.4.4.3 AASRC Mode Channel

The AASRC channel is controlled primarily via the PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG register for the channel. This register holds three basic pieces of information:

- Whether the channel uses AASRC stream mode or group mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG setting. The pulses for the individual events are latched and held by the PDMA until they all arrive. Once the channel activates, it will start reading FIFO index values from TX order table (PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE0, PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE1), starting at the configured FIRSTSLOT and ending with the LASTSLOT. The actual FIFO indices used are obtained from the ordering table. For example, say FIRSTSLOT=3 and LASTSLOT=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs written for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width written to the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel. Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The write transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.3.4.5 Tx Pause

The host initiates a channel pause by setting the PDMA_PSILCFG_TX_RT_ENABLE[9] PAUSE bit. The paused channel can be resumed by clearing the register bit.

11.3.1.3.4.6 Tx Teardown

The host initiates a channel teardown by setting the TDOWN bit in the paired-DMA (BCDMA/PKTDMA) channel that is paired with the PDMA. The paired-DMA communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous paired-DMA data for the channel has been flushed. At this time, the teardown state will be reflected in the PDMA_PSILCFG_TX_RT_ENABLE[30] TDOWN bit. Note that a non-synchronized teardown can also be initiated by directly clearing the PDMA_PSILCFG_TX_RT_ENABLE[31] ENABLE.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel will be cleared in the PDMA_PSILCFG_TX_RT_ENABLE register, but the teardown bit will remain high. Upon completion, no further packet processing will occur until the host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the paired-DMA transmission stops on a data boundary that is not compatible with the static TR configuration, the PDMA_PSILCFG_TX_RT_ENABLE[28] FLUSH bit can be set to guarantee that all data can be properly flushed from the internal pipe.

11.3.1.3.4.7 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the PDMA_PSILCFG_TX_ENABLE[31] ENABLE bit. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the paired-DMA peer. Resetting the paired-DMA peer is also required before re-initializing and re-pairing the channel.

11.3.1.3.4.8 Tx Debug/State Registers

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. These registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as follows:

- PDMA_PSILCFG_TX_DEBUG_1

- PDMA_PSILCFG_TX_DEBUG_2

Refer to their descriptions for further details.

11.3.1.3.5 PDMA Receive Operation

11.3.1.3.5.1 Source (Rx) Channel Allocation

A total of *M* destination channels are provided within the PDMA for concurrent transfers from the various attached peripherals into the Rx per-channel buffers and on to the PSI-L Rx Interface, where *M* is a design-time configurable paramater. Each Rx channel requires a single PSI-L thread. See *PDMA Sources* for Rx channel allocation for each PDMA.

11.3.1.3.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the host will need to first pair the channel with a remote data source (normally a paired-DMA channel), setup the static TR for the channel, and enable the thread.

11.3.1.3.5.2.1 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The host will pair each source PDMA channel with (typically) a corresponding destination channel in the paired-DMA. The PDMA thread is configured to point to the paired-DMA thread and the paired-DMA thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA will send all their data to the source channel in the paired-DMA and the destination channel in the paired-DMA will never see any data other than data from the source channel in the PDMA.

The following PSI-L registers are related to source thread pairing:

- PDMA_PSILCFG_RX_PEER_THREAD_ID
- PDMA_PSILCFG_RX_PEER_CREDIT
- PDMA_PSILCFG_RX_ENABLE
- PDMA_PSILCFG_RX_BYTE_COUNT
- PDMA_PSILCFG_RX_RT_ENABLE

Refer to their descriptions for further details.

11.3.1.3.5.2.2 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of 'X', 'Y', and 'Z' parameters, but the field interpretation varies somewhat. The following PSI-L register bit fields are used to setup the static TR:

- PDMA_PSILCFG_RX_STATIC_TR[26-24] X
- PDMA_PSILCFG_RX_STATIC_TR[11-0] Y
- PDMA_PSILCFG_RX_STATIC_TR_Z[11-0] Z

Refer to their descriptions for further details.

11.3.1.3.5.2.3 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.3.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the receive PSI-L interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx per-channel buffer for that channel. At a later time, the data is moved from the Rx per-channel FIFO to a remote peer DMA entity via the Rx PSI-L interface.

The sequences of logical transactions that are performed by the PDMA on the memory interface during receive is dependent on the channel type. The following sections describe what will happen for the two different channel types.

11.3.1.3.5.3.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter reads of 'X' parameter bytes from the data FIFO address specified for the channel. Each read that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the Rx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.3.5.3.2 MCAN Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA will start copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN will skip the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as shown in Table 11-88.

Table 11-88. Mapping of MCAN Filter Events to MCAN Channels

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping-pong buffer for a particular RX packet ID. For example, the following two filter entries will setup a ping-pong using RX buffers 0 and 1 for packet ID = 5 on CAN RX channel 0 (Table 11-89).

Table 11-89. Ping-Pong Buffer Example in MCAN Mode

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.3.5.3.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.3.5.3.3 AASRC Mode Channel

The AASRC channel is controlled primarily via the PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG register for the channel. This register holds three basic pieces of information:

- Whether the channel uses AASRC stream mode or group mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG setting. The pulses for the individual events are latched and held by the PDMA until they all arrive. Once the channel activates, it will start reading FIFO index values from RX order table (PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0, PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1), starting at the configured FIRSTSLOT and ending with the LASTSLOT. The actual FIFO indices used are obtained from the ordering table. For example, say FIRSTSLOT=3 and LASTSLOT=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel. Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.3.5.4 Rx Pause

The host initiates a channel pause by setting the PDMA_PSILCFG_RX_RT_ENABLE[29] PAUSE bit. The paused channel can be resumed by clearing the register bit.

11.3.1.3.5.5 Rx Teardown

The host initiates a RX channel teardown by setting the PDMA_PSILCFG_RX_RT_ENABLE[30] TDOWN bit for the target RX channel. The PDMA communicates the teardown state to the paired-DMA through the PSI-L data channel, to ensure that the teardown is not seen by the paired-DMA until all the previous PDMA data for the channel has been flushed.

The PDMA will not stop reading peripheral data until it reaches a FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. It will always attempt to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA will then clear the ENABLE bit in the pairing register, however the TDOWN bit will remain set. No further packet processing will occur until the host re-configures the channel. The teardown process will propagate to the paired-DMA and its final status can be checked there.

11.3.1.3.5.6 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the PDMA_PSILCFG_RX_ENABLE[31] ENABLE bit. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the paired-DMA peer. Resetting the paired-DMA peer is also required before re-initializing and re-pairing the channel.

11.3.1.3.5.7 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular opteration, but which may be useful in debug situations. These registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as follows:

- PDMA_PSILCFG_RX_DEBUG_1
- PDMA_PSILCFG_RX_DEBUG_2
- PDMA_PSILCFG_RX_DEBUG_3

Refer to their descriptions for further details.

11.3.1.3.6 PDMA ECC Support

The PDMA optionally integrates an ECC aggregator module that consolidates the ECC configuration and status bits for all the ECC-supported memories within the PDMA. The ECC aggregator provides a single end-of-interrupt (EOI) handshake based interrupt to the host (for both single and double error detections), and a standard 32-bit VBUSP interface for configuring and querying the various ECC wrappers via their respective register set.

In this device, only PDMA5, PDMA9 and PDMA10 include an ECC aggregator.

For detailed description of the generic ECC aggregator functionality, see *ECC Aggregator*. For register descriptions of PDMA ECC aggregators, see *PDMA Registers*.

11.3.2 PDMA Sources

11.3.2.1 PDMA0 Event Map

Table 11-90. PDMA0 Tx Channel Allocation

Tx PDMA Channel	Event Name	Function	Channel Type	Trigger Type	Data FIFO Address
8000	SPI_MAIN_0_TX_MCSPI0_DMA_WRITE_EVENT_0	SPI0 Tx Channel 0	XY	Edge	2010 0138h
8001	SPI_MAIN_0_TX_MCSPI0_DMA_WRITE_EVENT_1	SPI0 Tx Channel 1	XY	Edge	2010 014Ch
8002	SPI_MAIN_0_TX_MCSPI0_DMA_WRITE_EVENT_2	SPI0 Tx Channel 2	XY	Edge	2010 0160h
8003	SPI_MAIN_0_TX_MCSPI0_DMA_WRITE_EVENT_3	SPI0 Tx Channel 3	XY	Edge	2010 0174h
8004	SPI_MAIN_1_TX_MCSPI1_DMA_WRITE_EVENT_0	SPI1 Tx Channel 0	XY	Edge	2011 0138h
8005	SPI_MAIN_1_TX_MCSPI1_DMA_WRITE_EVENT_1	SPI1 Tx Channel 1	XY	Edge	2011 014Ch
8006	SPI_MAIN_1_TX_MCSPI1_DMA_WRITE_EVENT_2	SPI1 Tx Channel 2	XY	Edge	2011 0160h
8007	SPI_MAIN_1_TX_MCSPI1_DMA_WRITE_EVENT_3	SPI1 Tx Channel 3	XY	Edge	2011 0174h
8008	SPI_MAIN_2_TX_MCSPI2_DMA_WRITE_EVENT_0	SPI2 Tx Channel 0	XY	Edge	2012 0138h
8009	SPI_MAIN_2_TX_MCSPI2_DMA_WRITE_EVENT_1	SPI2 Tx Channel 1	XY	Edge	2012 014Ch
800A	SPI_MAIN_2_TX_MCSPI2_DMA_WRITE_EVENT_2	SPI2 Tx Channel 2	XY	Edge	2012 0160h
800B	SPI_MAIN_2_TX_MCSPI2_DMA_WRITE_EVENT_3	SPI2 Tx Channel 3	XY	Edge	2012 0174h
800C	SPI_MAIN_3_TX_MCSPI3_DMA_WRITE_EVENT_0	SPI3 Tx Channel 0	XY	Edge	2013 0138h
800D	SPI_MAIN_3_TX_MCSPI3_DMA_WRITE_EVENT_1	SPI3 Tx Channel 1	XY	Edge	2013 014Ch
800E	SPI_MAIN_3_TX_MCSPI3_DMA_WRITE_EVENT_2	SPI3 Tx Channel 2	XY	Edge	2013 0160h
800F	SPI_MAIN_3_TX_MCSPI3_DMA_WRITE_EVENT_3	SPI3 Tx Channel 3	XY	Edge	2013 0174h
8010	USART_MAIN_0_TX_UART0_USART_DMA_0	UART0 Tx Channel 0	XY	Edge	0280 0000h
8011	USART_MAIN_1_TX_UART1_USART_DMA_0	UART1 Tx Channel 0	XY	Edge	0281 0000h

Table 11-91. PDMA0 Rx Channel Allocation

Rx PDMA Channel	Event Name	Function	Channel Type	Trigger Type	Data FIFO Address
0	SPI_MAIN_0_RX_MCSPI0_DMA_READ_EVENT_0	SPI0 Rx Channel 0	XY	Edge	2010 013Ch
1	SPI_MAIN_0_RX_MCSPI0_DMA_READ_EVENT_1	SPI0 Rx Channel 1	XY	Edge	2010 0150h
2	SPI_MAIN_0_RX_MCSPI0_DMA_READ_EVENT_2	SPI0 Rx Channel 2	XY	Edge	2010 0164h
3	SPI_MAIN_0_RX_MCSPI0_DMA_READ_EVENT_3	SPI0 Rx Channel 3	XY	Edge	2010 0178h
4	SPI_MAIN_1_RX_MCSPI1_DMA_READ_EVENT_0	SPI1 Rx Channel 0	XY	Edge	2011 013Ch
5	SPI_MAIN_1_RX_MCSPI1_DMA_READ_EVENT_1	SPI1 Rx Channel 1	XY	Edge	2011 0150h
6	SPI_MAIN_1_RX_MCSPI1_DMA_READ_EVENT_2	SPI1 Rx Channel 2	XY	Edge	2011 0164h
7	SPI_MAIN_1_RX_MCSPI1_DMA_READ_EVENT_3	SPI1 Rx Channel 3	XY	Edge	2011 0178h
8	SPI_MAIN_2_RX_MCSPI2_DMA_READ_EVENT_0	SPI2 Rx Channel 0	XY	Edge	2012 013Ch
9	SPI_MAIN_2_RX_MCSPI2_DMA_READ_EVENT_1	SPI2 Rx Channel 1	XY	Edge	2012 0150h
10	SPI_MAIN_2_RX_MCSPI2_DMA_READ_EVENT_2	SPI2 Rx Channel 2	XY	Edge	2012 0164h
11	SPI_MAIN_2_RX_MCSPI2_DMA_READ_EVENT_3	SPI2 Rx Channel 3	XY	Edge	2012 0178h
12	SPI_MAIN_3_RX_MCSPI3_DMA_READ_EVENT_0	SPI3 Rx Channel 0	XY	Edge	2013 013Ch
13	SPI_MAIN_3_RX_MCSPI3_DMA_READ_EVENT_1	SPI3 Rx Channel 1	XY	Edge	2013 0150h
14	SPI_MAIN_3_RX_MCSPI3_DMA_READ_EVENT_2	SPI3 Rx Channel 2	XY	Edge	2013 0164h
15	SPI_MAIN_3_RX_MCSPI3_DMA_READ_EVENT_3	SPI3 Rx Channel 3	XY	Edge	2013 0178h
16	USART_MAIN_0_RX_UART0_USART_DMA_1	UART0 Rx Channel 0	XY	Edge	0280 0000h
17	USART_MAIN_1_RX_UART1_USART_DMA_1	UART1 Rx Channel 0	XY	Edge	0281 0000h

11.3.2.2 PDMA1 Event Map

Table 11-92. PDMA1 Tx Channel Allocation

Tx PDMA Channel	Event Name	Function	Channel Type	Trigger Type	Data FIFO Address
8000	SPI_MAIN_4_TX_MCSPI4_DMA_WRITE_EVENT_0	SPI4 Tx Channel 0	XY	Edge	2014 0138h
8001	SPI_MAIN_4_TX_MCSPI4_DMA_WRITE_EVENT_1	SPI4 Tx Channel 1	XY	Edge	2014 014Ch
8002	SPI_MAIN_4_TX_MCSPI4_DMA_WRITE_EVENT_2	SPI4 Tx Channel 2	XY	Edge	2014 0160h
8003	SPI_MAIN_4_TX_MCSPI4_DMA_WRITE_EVENT_3	SPI4 Tx Channel 3	XY	Edge	2014 0174h
8004	USART_MAIN_2_TX_UART2_USART_DMA_0	UART2 Tx Channel 0	XY	Edge	0282 0000h
8005	USART_MAIN_3_TX_UART3_USART_DMA_0	UART3 Tx Channel 0	XY	Edge	0283 0000h
8006	USART_MAIN_4_TX_UART4_USART_DMA_0	UART4 Tx Channel 0	XY	Edge	0284 0000h
8007	USART_MAIN_5_TX_UART5_USART_DMA_0	UART5 Tx Channel 0	XY	Edge	0285 0000h
8008	USART_MAIN_6_TX_UART6_USART_DMA_0	UART6 Tx Channel 0	XY	Edge	0286 0000h
8009	MCANSS_MAIN_0_TX_MCAN0_MCANSS_TX_DMA_0	MCAN0 Tx Channel 0	MCAN	Pulse	2070 8000h
800A	MCANSS_MAIN_0_TX_MCAN0_MCANSS_TX_DMA_1	MCAN0 Tx Channel 1	MCAN	Pulse	2070 8048h
800B	MCANSS_MAIN_0_TX_MCAN0_MCANSS_TX_DMA_2	MCAN0 Tx Channel 2	MCAN	Pulse	2070 8090h
800C	MCANSS_MAIN_1_TX_MCAN1_MCANSS_TX_DMA_0	MCAN1 Tx Channel 0	MCAN	Pulse	2071 8000h
800D	MCANSS_MAIN_1_TX_MCAN1_MCANSS_TX_DMA_1	MCAN1 Tx Channel 1	MCAN	Pulse	2071 8048h
800E	MCANSS_MAIN_1_TX_MCAN1_MCANSS_TX_DMA_2	MCAN1 Tx Channel 2	MCAN	Pulse	2071 8090h

Table 11-93. PDMA1 Rx Channel Allocation

Rx PDMA Channel	Event Name	Function	Channel Type	Trigger Type	Data FIFO Address
0	SPI_MAIN_4_RX_MCSPI4_DMA_READ_EVENT_0	SPI4 Rx Channel 0	XY	Edge	2014 013Ch
1	SPI_MAIN_4_RX_MCSPI4_DMA_READ_EVENT_1	SPI4 Rx Channel 1	XY	Edge	2014 0150h
2	SPI_MAIN_4_RX_MCSPI4_DMA_READ_EVENT_2	SPI4 Rx Channel 2	XY	Edge	2014 0164h
3	SPI_MAIN_4_RX_MCSPI4_DMA_READ_EVENT_3	SPI4 Rx Channel 3	XY	Edge	2014 0178h
4	USART_MAIN_2_RX_UART2_USART_DMA_1	UART2 Rx Channel 0	XY	Edge	0282 0000h
5	USART_MAIN_3_RX_UART3_USART_DMA_1	UART3 Rx Channel 0	XY	Edge	0283 0000h
6	USART_MAIN_4_RX_UART4_USART_DMA_1	UART4 Rx Channel 0	XY	Edge	0284 0000h
7	USART_MAIN_5_RX_UART5_USART_DMA_1	UART5 Rx Channel 0	XY	Edge	0285 0000h
8	USART_MAIN_6_RX_UART6_USART_DMA_1	UART6 Rx Channel 0	XY	Edge	0286 0000h
9	MCANSS_MAIN_0_FE_MCAN0_MCANSS_FE_0	MCAN0 Rx Channel 0	MCAN	Pulse	2070 8900h
10	MCANSS_MAIN_0_FE_MCAN0_MCANSS_FE_1	MCAN0 Rx Channel 1	MCAN	Pulse	2070 8990h
11	MCANSS_MAIN_0_FE_MCAN0_MCANSS_FE_2	MCAN0 Rx Channel 2	MCAN	Pulse	2070 8A20h
12	MCANSS_MAIN_1_FE_MCAN1_MCANSS_FE_0	MCAN1 Rx Channel 0	MCAN	Pulse	2071 8900h
13	MCANSS_MAIN_1_FE_MCAN1_MCANSS_FE_1	MCAN1 Rx Channel 1	MCAN	Pulse	2071 8990h
14	MCANSS_MAIN_1_FE_MCAN1_MCANSS_FE_2	MCAN1 Rx Channel 2	MCAN	Pulse	2071 8A20h
15	ADC12_MAIN_0_RX_ADC0_FIFO0_LEVEL_0	ADC0 Rx Channel 0	XY	Edge	2800 0100h
16	ADC12_MAIN_0_RX_ADC0_FIFO0_LEVEL_1	ADC0 Rx Channel 1	XY	Edge	2800 0200h

Chapter 12

Peripherals

This chapter describes the various peripheral modules instantiated in the device.

12.1 General Connectivity Peripherals

This section describes the general connectivity peripherals in the device.

12.1.1 Analog-to-Digital Converter (ADC)

This chapter describes the Analog-to-Digital Converter (ADC) in the device.

12.1.1.1 ADC Overview

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels).

There is one ADC module in the device.

Table 12-1 shows ADC module allocation within device domains.

Table 12-1. ADC Module Allocation within Device Domains

Module Instance	Domain	
	MCU	MAIN
ADC0	-	✓

Figure 12-1 presents an overview of the ADC module.

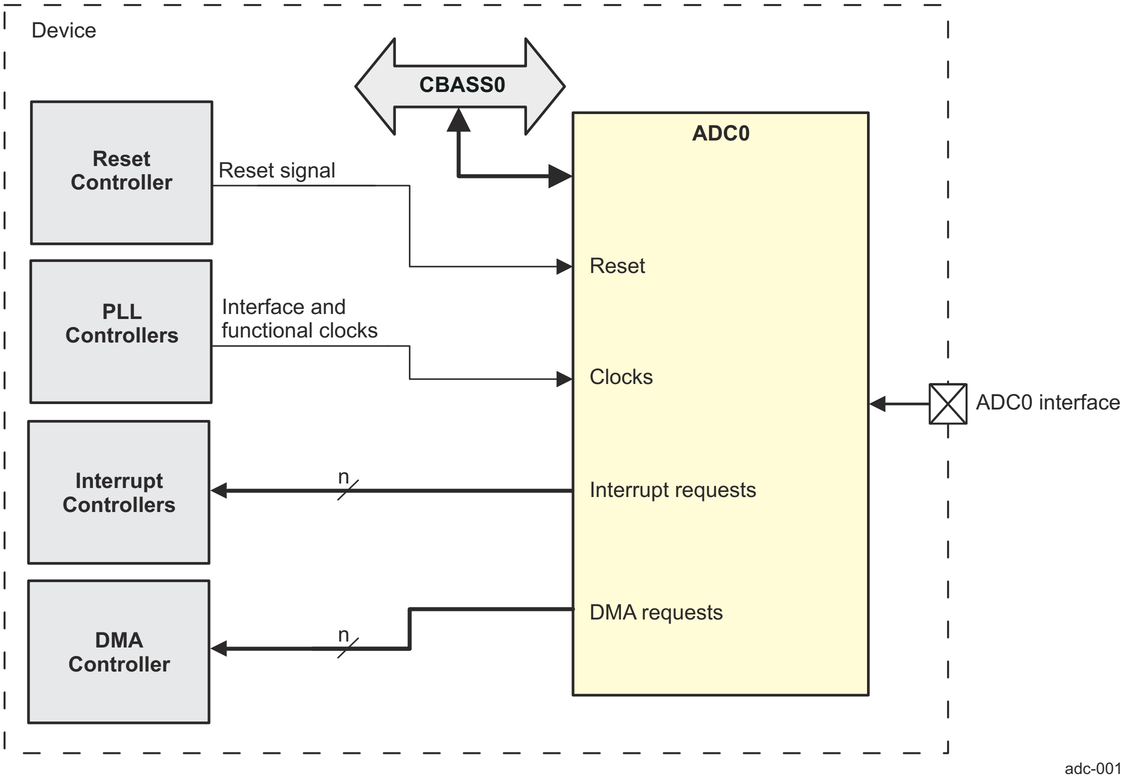

Figure 12-1. ADC Module Overview

12.1.1.1.1 ADC Features

Each ADC module has the following features:

- 4 MSPS rate with a 60 MHz SMPL_CLK
- Functional Internal Diagnostic Debug Mode
- Single-ended or differential input options
- Each ADC module can be configured and transformed into a digital test inputs
- Programmable Finite State Machine (FSM) sequencer that supports the following:
  - Software initiated start of conversion
  - Optional hardware start of conversion (SOC), synchronized to external hardware event
  - Single conversion (one-shot mode)
  - Continuous conversions (continuous mode)

  - Sequence through all enabled steps based on a mask
  - Programmable open delay before executing each step
  - Programmable sampling delay for each step
  - Programmable averaging (16, 8, 4, 2, or 1) of input samples for each step
  - Store data in either of two FIFOs – 256-word × 16-bit
  - Option to encode input (channel) number with data
  - Support for servicing FIFOs via DMA or processor
  - Programmable DMA request event (for each FIFO)
- Support for the following interrupts and status, with masking:
  - Interrupt if AFE fails to return end of conversion (EOC)
  - Interrupt after a sequence of conversions (all non-masked steps)
  - Interrupt for FIFO threshold levels
  - Interrupt if sampled data is out of a programmable range
  - Interrupt for FIFO overflow and underflow conditions
  - Status bit to indicate if ADC is busy converting

12.1.1.1.2 ADC Not Supported Features

- No packing of 16-bit FIFO data onto 32-bit DMA bus
- Big endian
- Support only 32-bit aligned read/write accesses on the CBASS0/DMA ports
- Simultaneous sampling

12.1.1.2 ADC Environment

The ADC0 module is hereinafter referred to as ADC module.

This section describes the ADC external connections (environment).

12.1.1.2.1 ADC Interface Signals

Figure 12-2 shows the ADC signals.

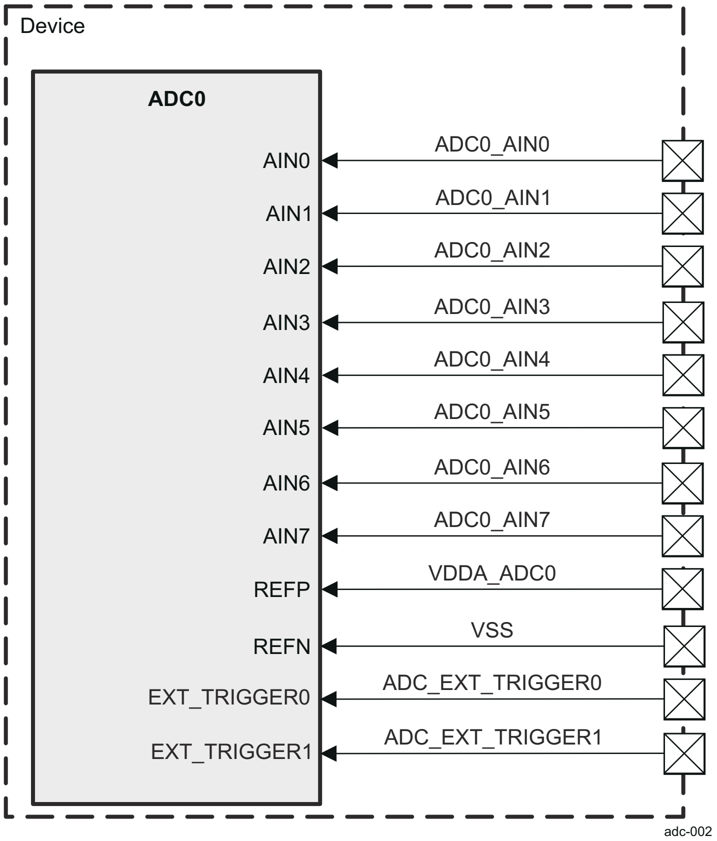

Figure 12-2. ADC Signals

Table 12-2 describes the ADC I/O signals.

Table 12-2. ADC I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
		ADC0		
AIN0	ADC0_AIN0	A/I	Analog input 0	HiZ
AIN1	ADC0_AIN1	A/I	Analog input 1	HiZ
AIN2	ADC0_AIN2	A/I	Analog input 2	HiZ
AIN3	ADC0_AIN3	A/I	Analog input 3	HiZ
AIN4	ADC0_AIN4	A/I	Analog input 4	HiZ
AIN5	ADC0_AIN5	A/I	Analog input 5	HiZ
AIN6	ADC0_AIN6	A/I	Analog input 6	HiZ
AIN7	ADC0_AIN7	A/I	Analog input 7	HiZ
REFP	VDDA_ADC0	PWR	Reference voltage input positive	-
REFN	VSS	GND	Reference voltage input negative	-
EXT_TRIGGER0	ADC_EXT_TRIGGER0	I	External trigger for ADC	HiZ

Table 12-2. ADC I/O Signals (continued)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
EXT_TRIGGER1	ADC_EXT_TRIGGER1	I	External trigger for ADC	HiZ

(1) I = Input; A = Analog
(2) HiZ = High Impedance

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.1.1.3 ADC Integration

This section describes ADC integration in the device, including information about clocks, resets, and hardware requests.

12.1.1.3.1 ADC Integration in MAIN Domain

There is one ADC module integrated in the device MAIN domain - ADC0. Figure 12-3 shows the integration of ADC0.

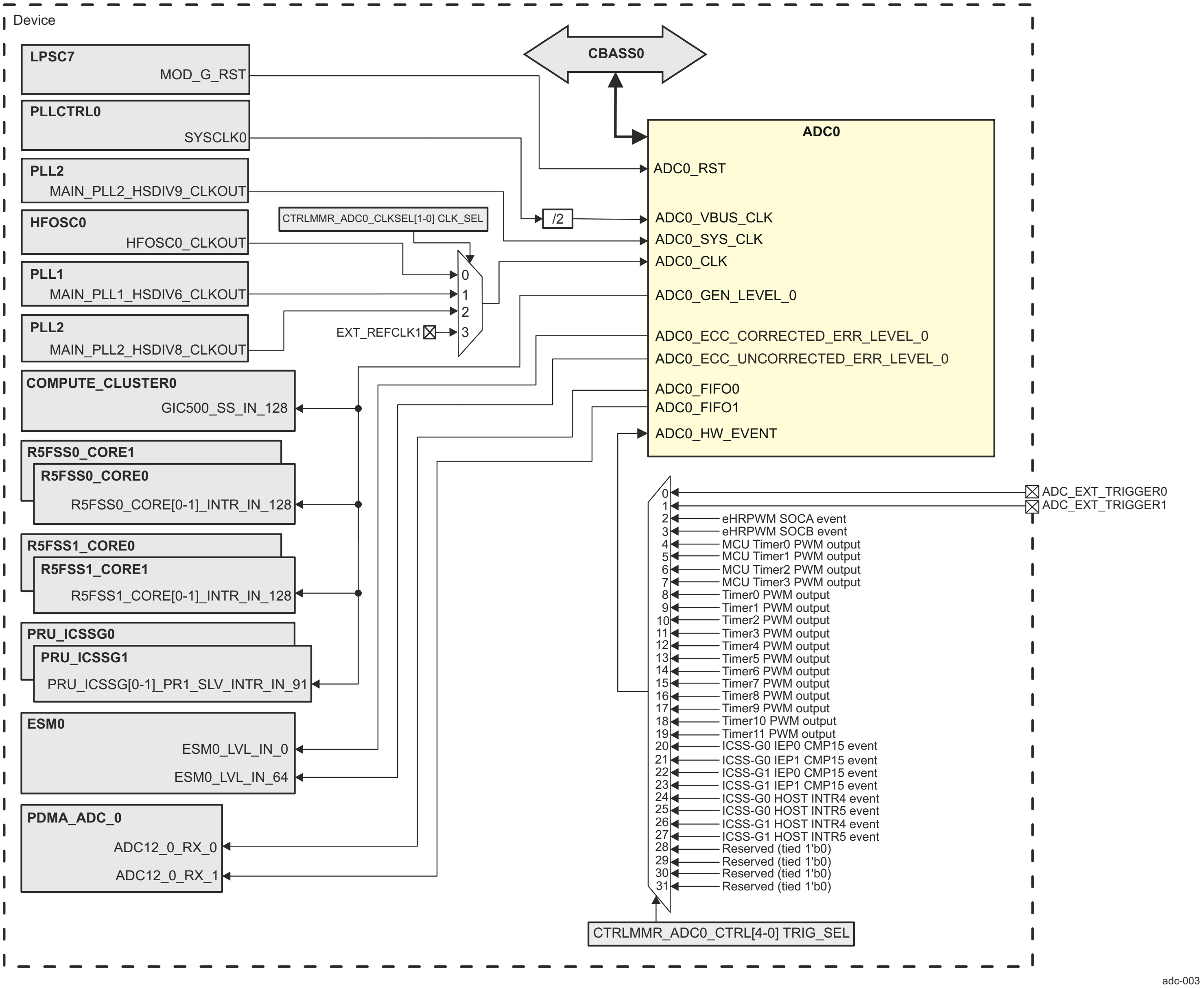

Figure 12-3. ADC0 Integration

Table 12-3 through Table 12-6 summarize the integration of ADC0 in device MAIN domain.

Table 12-3. ADC0 Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
ADC0	PSC0	PD0	LPSC7	CBASS0

Table 12-4. ADC0 Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
ADC0	ADC0_VBUS_CLK	SYSCLK0/2	PLLCTRL0	ADC0 interface clock
	ADC0_SYS_CLK	MAIN_PLL2_HSDIV9_CLKOUT	PLL2	ADC0 system clock
	ADC0_CLK	HFOSC0_CLKOUT[(1)]	HFOSC0	ADC0 clock. Output of multiplexer, see Figure 12-3, *ADC Integration*. Multiplexer control is provided via MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL[1-0] CLK_SEL bit field. Default state is HFOSC0_CLKOUT.
		MAIN_PLL1_HSDIV6_CLKOUT	PLL1	
		MAIN_PLL2_HSDIV8_CLKOUT	PLL2	
		EXT_REFCLK1	I/O pin	

(1) Input HFOSC0_CLKOUT is not a valid option for ADC.

> **WARNING**
>
> The only valid option for the ADC is 60MHz, which should originate from EXT_REFCLK1 or one of the two PLL inputs.

Table 12-5. ADC0 Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
ADC0	ADC0_RST	MOD_G_RST	LPSC7	ADC0 reset

Table 12-6. ADC0 Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Type	Description
ADC0	ADC0_GEN_LEVEL_0	GIC500_SS_IN_128	COMPUTE_CLUSTER0	Level	ADC0 interrupt request
		R5FSS0_CORE0_INTR_IN_128	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_128	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_128	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_128	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_INTR_IN_91	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_INTR_IN_91	PRU_ICSSG1		
	ADC0_ECC_CORRECTED_ERR_LEVEL_0	ESM0_LVL_IN_0	ESM0	Level	ADC0 ECC corrected error interrupt request
	ADC0_ECC_UNCORRECTED_ERR_LEVEL_0	ESM0_LVL_IN_64	ESM0	Level	ADC0 ECC uncorrected error interrupt request

Table 12-7. ADC0 DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Type	Description
ADC0	ADC0_FIFO0	ADC12_0_RX_0	PDMA_ADC_0	Pulse	ADC0 receive request line
	ADC0_FIFO1	ADC12_0_RX_1	PDMA_ADC_0	Pulse	ADC0 receive request line

Note

ADC interrupts are further described in Chapter 9 , *Interrupts*.

ADC DMA events are further described in Section 12.1.1.4.1.6 , *DMA Requests* and Section 11.1 , *DMA*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

For more information on the DMA controllers, see Section 11.1 , *Data Movement Architecture (DMA)*.

12.1.1.4 ADC Functional Description

12.1.1.4.1 ADC FSM Sequencer Functional Description

The FSM sequencer supports up to 16 steps that can be configured to perform analog-to-digital conversions. Each of the 16 steps can individually be enabled and configured to operate as software enabled steps or hardware enabled steps. Each step has its own programmable step configuration (ADC_STEPCONFIG_j) and step delay (ADC_STEPDELAY_j) registers that allow users to configure the ADC operation on a per-step basis.

The FSM sequencer enters Idle immediately after the ADC is enabled and remains in Idle while waiting for any of the 16 programmable steps to be enabled. When one or more step is enabled, the FSM sequencer will begin executing or skipping each step starting with the lowest and incrementing up through each step until the highest step has been executed or skipped. The FSM sequencer will execute enabled steps and skip disabled steps. Once all of the steps have been executed or skipped, the FSM sequencer will return to Idle or immediately begin repeating steps configured for continuous mode.

An ENDOFEQUENCE interrupt can be generated after the last enabled step has been executed. If any software enabled steps are configured for continuous operation and they are still enabled when the FSM sequencer has incremented through all the steps, the FSM sequencer will start the sequence again with the first enabled step. Hardware enabled steps are mapped to a hardware event and will need the hardware event to occur before being scheduled.

Figure 12-4 illustrates how the FSM sequencer works. Each shaded box represents a FSM state.

Note

Figure 12-4 does not represent the number of SMPL_CLK cycles required by each state since some states implement user programmable delays that may require more than one SMPL_CLK cycle to complete.

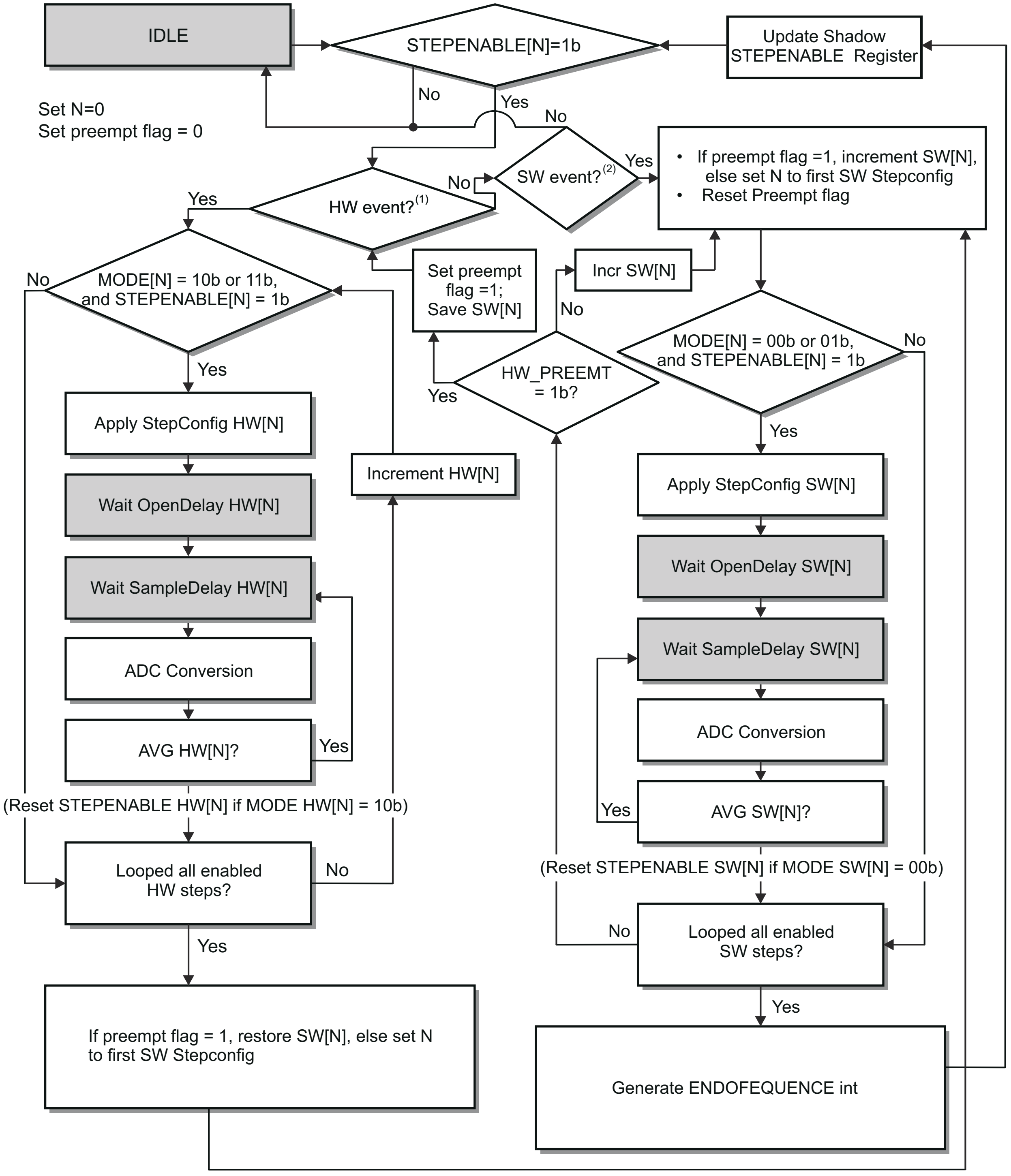

(1) MODE[N] = 10b or 11b, STEPENABLE[N] = 1b, and HW Event = 1

(2) MODE[N] = 00b or 01b and STEPENABLE[N] = 1b

Figure 12-4. Sequencer FSM

12.1.1.4.1.1 Step Enable

A step is enabled or disabled via the ADC_STEPENABLE register. The system software should only write to the ADC_STEPENABLE register when the ADC is disabled or the FSM sequencer is idle. Therefore, it may be necessary to disable the ADC before updating the ADC_STEPENABLE register if the FSM sequencer is executing back-to-back steps where it never enters idle.

12.1.1.4.1.2 Step Configuration

12.1.1.4.1.2.1 One-Shot (Single) or Continuous Mode

Each step can be configured to operate in one-shot or continuous mode via the least significant bit of the MODE bit-field of the respective ADC_STEPCONFIG_j register. Steps configured for one-shot mode will perform a single conversion before being disabled by the FSM sequencer. Steps configured for continuous mode will automatically be re-enabled by the FSM sequencer after each conversion until disabled by software.

12.1.1.4.1.2.2 Software- or Hardware-Enabled Steps

Each step can be configured to operate in SW Enabled mode or HW Enabled mode independently via the most significant bit of the MODE bit-field in the respective ADC_STEPCONFIG_j register. However, the hardware event source is applied globally to all HW Enabled steps and configured via the ADC_CONTROL register.

The user can configure each step to begin immediately after the step is enabled by software (SW Enabled), or wait for a hardware event to occur (HW Enabled).

The EXT_TRIGGER0/1 input signals are used by HW Enabled steps. The trigger inputs have the option of being sourced from a device input pin or several on-device peripherals via a multiplexer controlled by TRIG_SEL of the respective CTRLMMR_ADC0_CTRL register. When this option is selected, the hardware event will be triggered after the EXT_TRIGGER0/1 input signals transitions from low to high and is held high for a period greater than two cycles of SYS_CLK. This hardware event will only schedule one complete sequence, even for continuous mode. If HW Enabled steps need to be executed again, a new hardware event must be generated after the previously triggered sequence has completed.

SW Enabled steps can be preempted by HW Enabled steps when the HW_PREEMPT bit in the ADC_CONTROL register is set.

12.1.1.4.1.2.3 Averaging of Samples

Each step can be configured, via the respective ADC_STEPCONFIG_j register, to sample an input 1, 2, 4, 8, or 16 times and provide an average data value. If a step is configured to sample more than once, the additional samples are taken back-to-back immediately after the first sample. However, open delay is only applied to the first sample while sample delay is applied to all samples. Once the last sample has been taken the average data value will be stored in the FIFO.

12.1.1.4.1.2.4 Analog Multiplexer Input Select

The AFE contains two 9-to-1 analog multiplexers which are used to select the source connected to the positive input (INP) and negative input (INM) of the ADC. Each step can be configured, via the respective ADC_STEPCONFIG_j register, to select the appropriate input sources. For more information, refer to Section 12.1.1.4.2.1 and the ADC_STEPCONFIG_j register field descriptions.

12.1.1.4.1.2.5 Differential Control

The ADC supports differential inputs and each step can be configured, via the respective ADC_STEPCONFIG_j register, to select single-ended input mode or differential input mode.

Note

The ADC INM input must be sourced from REFN for any steps configured to operate in single-ended mode.

12.1.1.4.1.2.6 FIFO Select

The ADC contains two FIFOs and each step can be configured, via the respective ADC_STEPCONFIG_j register, to store its ADC data into either FIFO.

12.1.1.4.1.2.7 Range Check Interrupt Enable

Each step can be configured, via the respective ADC_STEPCONFIG_j register, to compare the value of ADC data to high and low limits programmed in the ADC_RANGE register. The out-of-range interrupt is generated if the value of ADC data is greater than the value of HIRANGE or less than the value of LOWRANGE. Refer to the ADC_RANGE register field descriptions for information related to setting the high and low limits that trigger an out-of-range interrupt.

12.1.1.4.1.3 Open Delay and Sample Delay

The FSM sequencer provides two programmable delays for each step. The value of OPENDELAY is used to control when the acquisition begins after the step starts and the value of SAMPLEDELAY is used to control the acquisition period. Delays for each of the 16 steps can be configured independently via the respective ADC_STEPDELAY_j register.

12.1.1.4.1.3.1 Open Delay

OPENDELAY defaults to a value of zero which causes the acquisition period to begin as soon as the step starts. The start of the acquisition period can be delayed one SMPL_CLK clock period for each incremental value of OPENDELAY.

12.1.1.4.1.3.2 Sample Delay

SAMPLEDELAY defaults to a value of zero which causes the acquisition period to be equal to two SMPL_CLK clock periods. The acquisition period can be extended one SMPL_CLK clock for each incremental value of SAMPLEDELAY.

The value of SAMPLEDELAY should be configured to provide enough time for the respective external voltage source to completely charge the AFE input capacitance during the acquisition period.

12.1.1.4.1.4 Interrupts

The ADC has 9 internal events that can trigger an interrupt to the processor. These events are logically or'ed together to produce a single interrupt to the processor. The user can individually enable or disable each interrupt source via the ADC_ENABLE_SET and ADC_ENABLE_CLR registers. Once an interrupt is generated, the ADC_STATUS register can be read to determine which interrupt source(s) interrupted the processor. The interrupt source(s) can be cleared by writing a ‘1’ to the corresponding bit of the ADC_STATUS register.

The following interrupts are supported by the device ADC:

- An ENDOFEQUENCE interrupt is generated after the FSM sequencer completes the last enabled step.
- FIFO0UNFL/FIFO1UNFL or FIFO0OVFL/FIFO1OVFL interrupts. Each FIFO also has the ability to generate overrun and underflow interrupts. The ADC does not recover from overrun or underflow conditions automatically. Therefore, software will need to disable and re-enable the ADC after this occurs. The FSM sequencer must be Idle before turning the ADC module back on. This can be confirmed by reading the ADC_SEQUENCER_STAT register, when FSM_BUSY = 0x0 and STEP_IDLE = 0x10000.
- FIFO0THRS and FIFO1THRS interrupts. Each FIFO has the ability to generate an interrupt when the FIFO word count has reached a programmable threshold value. The FIFO0THRS and FIFO1THRS interrupt is generated when the value of NUMWDS in the respective ADC_FIFO0WC or ADC_FIFO1WC register equals the word count threshold value programmed in THRESHOLD of the respective ADC_FIFO0THRESHOLD or ADC_FIFO1THRESHOLD register.
- OUTOFRANGE interrupt. This interrupt can be enabled or disabled on each step. If enabled, the ADC data value is compared to the low and high thresholds programmed in the global ADC_RANGE register. The OUTOFRANGE interrupt is generated if the ADC data value is greater than the value programmed in HIRANGE or less than the value programmed in LOWRANGE.
- AFE_EOC_MISSING interrupt. This interrupt is generated when the FSM sequencer does not receive an expected EOC from the AFE.

12.1.1.4.1.5 Power Management

The software also has the option to turn off the AFE power by writing to the ADC_CONTROL[4] PD bit. By default, after the initial power on the AFE is powered down and software is responsible for turning it on. Software must wait minimum 4 µs after a AFE power up and before starting a conversion (must be followed every time the AFE is powered up). It is the software's responsibility to empty the FIFO before requesting the ADC to enter sleep state.

12.1.1.4.1.6 DMA Requests

Each FIFO can be serviced by the processor or DMA. The user can individually enable or disable each FIFO DMA request via the ADC_DMAENABLE_SET and ADC_DMAENABLE_CLR registers.

12.1.1.4.2 ADC AFE Functional Description

The AFE contains a single 12-bit successive approximation ADC which can be connected to one of eight user selectable analog inputs for each step executed by the FSM sequencer. There is also an option to configure the ADC to operate in differential mode where it samples the differential voltage applied to two of eight user selectable analog inputs.

The ADC sits idle until the FSM sequencer sends a Start of Conversion (SOC) pulse. Once the FSM sequencer sends a SOC pulse to the ADC, it begins sampling the analog input signal on the rising edge of SOC and continues sampling the analog input signal one cycle of SMPL_CLK after the falling edge of SOC. The SOC pulse width will be the value of SAMPLEDELAY plus one SMPL_CLK periods, so the total ADC acquisition time will be the value of SAMPLEDELAY plus two SMPL_CLK periods. The ADC captures the analog input signal at the end of the acquisition period and starts conversion, which requires thirteen SMPL_CLK periods to digitize the sampled input. An EOC signal is returned to the FSM sequencer to indicate the digital data is ready.

The ADC output is positive binary weighted data ranging from 0 to (2^{12} - 1). When configured for single-ended mode, ADC output data values 0 to (2^{12} - 1) represents a corresponding input voltage that ranges from the ADC negative reference (REFN) voltage to the ADC positive reference (REFP) voltage. When configured for differential mode, ADC output data values 0 to ((2^{12}/2) - 1) represents a corresponding negative differential input voltage that ranges from the REFP voltage to the REFN voltage and output data values (2^{12}/2) to (2^{12} - 1) represents a corresponding positive differential input voltage that ranges from the REFN voltage to the REFP voltage.

Using the minimum values of OPENDELAY and SAMPLEDELAY, the ADC can sample an analog input every 15 SMPL_CLK periods.

Figure 12-5 illustrates the operation of the FSM sequencer and ADC AFE, with indicators showing when the hardware configuration defined by ADC_STEPCONFIG_j and ADC_STEPDELAY_j registers are applied.

Note

Figure 12-5 assumes both steps shown are software enabled with averaging turned off, an OPENDELAY value of 1, and SAMPLEDELAY value of 0. The analog input is sampled for the duration of the SOC pulse plus one cycle of the SMPL_CLK. If the value of OPENDELAY were 0, it would appear as if the time associated with the Open portion of the FSM waveform would be removed from all the waveforms.

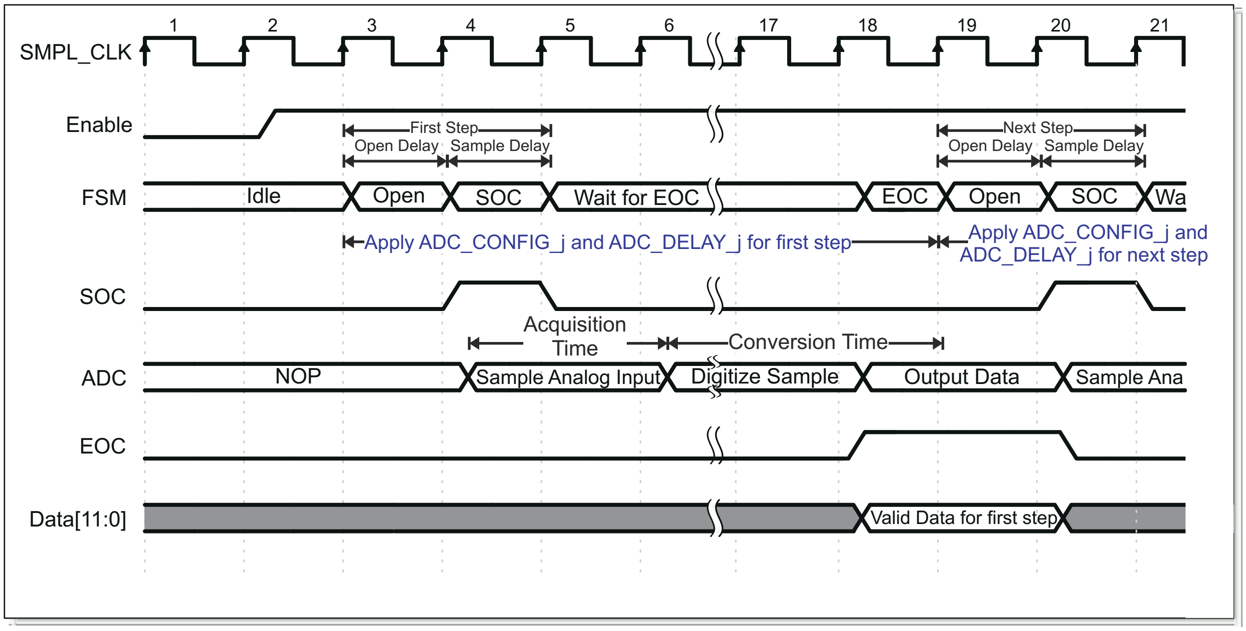

Figure 12-5. Example Timing Diagram for Sequencer

12.1.1.4.2.1 AFE Functional Block Diagram

The AFE has 8 analog inputs which can be configured as either singled-ended or differential inputs to the ADC. The user may configure a step to use any 1 of the 8 inputs when operating in single-ended mode or any 2 of the 8 inputs when operating in differential mode. For more information, refer to Figure 12-6 and the ADC_STEPCONFIG_j register field descriptions.

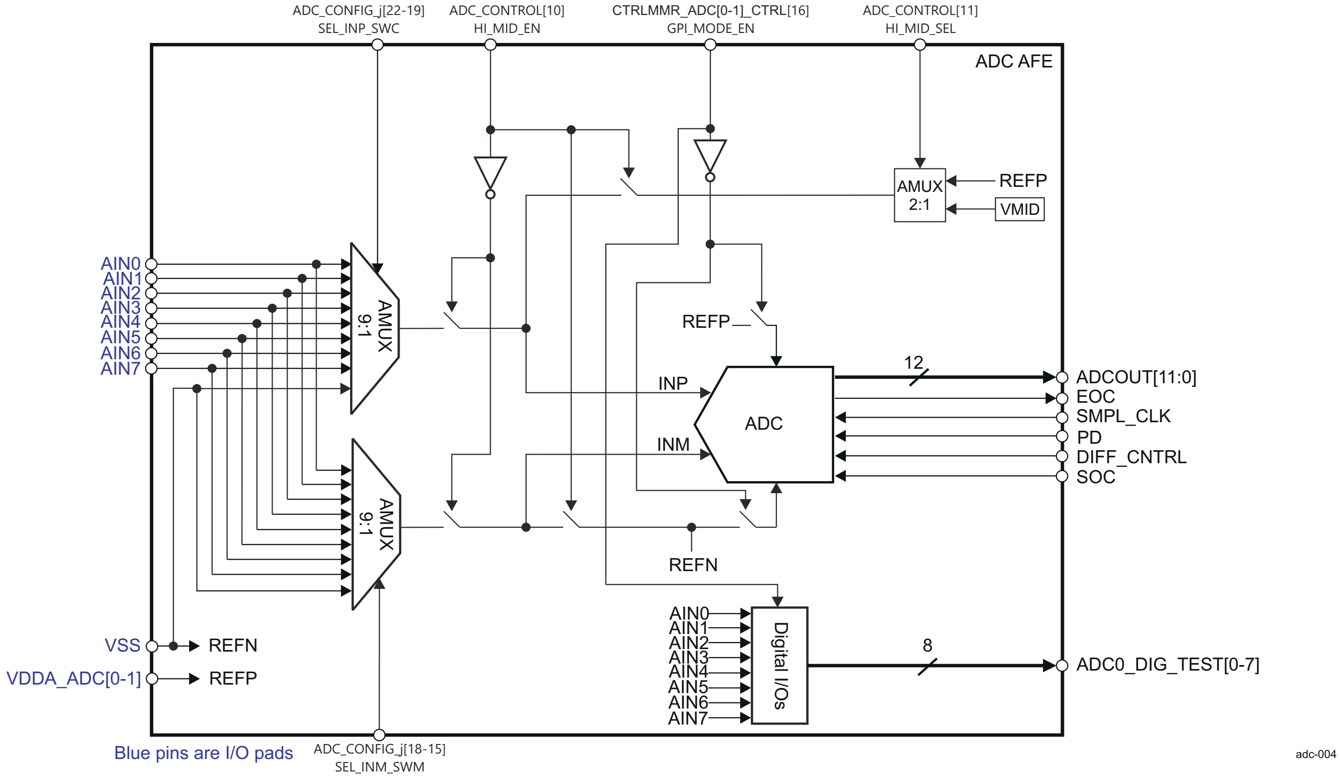

Figure 12-6. Functional Block Diagram

12.1.1.4.2.2 ADC GPI Integration

The ADC module can be configured to be used as a general digital test block which can generate 8 VDDA domain digital signals ADC0_DIG_TEST[0-7]. These digital outputs are made available to the device PinMux, where are used as general purpose digital inputs with some restrictions. The CTRLMMR_ADC0_CTRL[16] GPI_MODE_EN is the enable bit.

When GPI_MODE_EN bit is '0', the ADC is in normal operation.

When GPI_MODE_EN bit is '1', the ADC multiplexes the 8 analog inputs to 8 VDDA domain digital I/O block and outputs the signals to DIG_TEST[7-0] pins.

Restrictions on this usage are:
- The GPI_MODE_EN bit is not switched dynamically.
- ADC supports only 1.8V logic level.
- All ADC inputs on each ADC function either can be configured as digital or analog inputs.
- These are GPI only, not GPIO (no output buffer).

12.1.1.4.3 ADC FIFOs and DMA

12.1.1.4.3.1 FIFOs

There are two sample FIFOs (ADC_FIFO0 and ADC_FIFO1), which store sample data from the AFE. Can be configured, via the respective ADC_STEPCONFIG_j register.

The processor can read ADC data directly from the FIFO by using the respective ADC_FIFO0DATA or ADC_FIFO1DATA register. The internal logic will pop the next data from the FIFO and increment the FIFO read pointers.

The FIFO data will no longer be accessible after the ADC is disabled because the FIFO pointers are reset. Therefore, it is important to read all FIFO data before disabling the ADC.

12.1.1.4.3.2 DMA

The ADC has a dedicated target port for the DMA which allows it to perform continuous burst reads when accessing the FIFOs.

Each FIFO has its own DMA request which can be enabled via the ADC_DMAENABLE_SET register and disabled via the ADC_DMAENABLE_CLR register.

The first DMA request is generated after the FIFO leaves the EMPTY state and fills to the level programmed in DMAREQLEVEL of the respective ADC_FIFO0DMAREQ or ADC_FIFO1DMAREQ register.

Subsequently, a new DMA request is automatically generated on the next clock cycle after the current DMA access completes if the previous DMA access did not empty the FIFO.

12.1.1.4.4 ADC Error Correcting Code (ECC)

The Error Correcting Code (ECC) is a mechanism for providing increased system reliability (via reduction of memory soft errors) by allowing single bit errors to be detected and corrected and double bit errors to be detected.

The ECC Aggregator provides a single EOI-handshake based interrupt to the host (for both single and double error detections).

The ECC Aggregator will write 0’s to all of memory after reset is released. The ADC_SEQUENCER_STAT[6] MEM_INIT_DONE bit will be 0 during this period and will be set to 1 upon completion.

For more information about the ECC Aggregator, see *ECC Aggregator* and *ADC ECC Registers*.

See also *Testing ECC Error Injection* and *ADC ECC Registers*.

12.1.1.4.4.1 Testing ECC Error Injection

The read enable (REN) input to the RAMs instantiated in this module are constantly tied to 1’b1. As a result, read is continuously in progress.

In order to test ECC single error injection on a particular RAM row, the following conditions have to be maintained before setting the ADC_ECC_CTRL[3] FORCE_SEC bit:

- ADC_ECC_CTRL[5] FORCE_N_ROW bit has to be clear. This is required in order to configure required row in
- ADC_ECC_CTRL[6] ERROR_ONCE bit has to be clear. If this bit is set, the ECC error occurs immediately after setting ADC_ECC_CTRL[3] FORCE_SEC bit since REN is always set
- ADC_ECC_ERR_CTRL1[31-0] ECC_ROW bit field has to be point to the required row address

12.1.1.4.5 ADC Functional Internal Diagnostic Debug Mode

The ADC function can be validated by measuring known reference voltage sources. This feature provides register control that connects the AFE to known reference voltage sources. However, it does not automatically configure the FSM to perform conversions to measure these sources. Software will need to configure the FSM to perform a measurement after selecting this mode of operation.

ADC_CONTROL[10] HI_MID_EN is used to disconnect the AFE from all analog inputs and connect it to one of two known reference voltage sources. ADC_CONTROL[11] HI_MID_SEL is used to select REFP or VMID as the known reference voltage source.

The conversion results is expected to produce a full scale value when the AFE is connected to REFP and approximate half scale value when the AFE is connected to VMID.

The steps are:

- Disable the ADC if previously enabled and wait until the FSM is not busy.
- Put the AFE in a functional internal diagnostic debug mode by setting the ADC_CONTROL[10] HI_MID_EN bit to 1.
- Select one of the two reference voltage sources by setting the ADC_CONTROL[11] HI_MID_SEL bit.
  - 0 selects VMID
  - 1 selects REFP
- Configure the FSM to measure the selected reference voltage source.
- Enable the ADC and evaluate the results.
- When debug is complete, disable the ADC and wait until the FSM is not busy, re-program the FSM for functional operation, then re-enable the ADC.

12.1.1.5 ADC Programming Guide

12.1.1.5.1 ADC Low-Level Programming Models

12.1.1.5.1.1 Global Initialization

12.1.1.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the module is to be used for the first time after a device reset.

Table 12-8. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC7	Module reset must be enabled. For more information about the module configuration, see *Reset*.
PLLCTRL0	PLLCTRL0 configuration must be done to enable the clocks to the ADC module, see *Clocking*.
HFOSC0	HFOSC0 configuration must be done to enable the clocks to the ADC module, see *Clocking*.
PLL1	PLL1 configuration must be done to enable the clocks to the ADC module, see *Clocking*.
PLL2	PLL2 configuration must be done to enable the clocks to the ADC module, see *Clocking*.
COMPUTE_CLUSTER0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling COMPUTE_CLUSTER0 interrupts, see *Interrupts*.
R5FSS0_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS0_CORE0/1 interrupts, see *Interrupts*.
R5FSS1_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS1_CORE0/1 interrupts, see *Interrupts*.
PRU_ICSSG0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling PRU_ICSSG0 interrupts, see *Interrupts*.
ESM0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling ESM0 interrupts, see *Interrupts*.
PDMA_ADC_0	PDMA_ADC_0 controllers configuration must be done to enable the module PDMA_ADC_0 input request, see *Data Movement Architecture (DMA)*.
Interconnect	For information about the CBASS0 interconnect configuration, see *System Interconnect*.

12.1.1.5.1.1.2 General Programming Model

Table 12-9. General Programming Model

Step	Register/Bit Field/Programming Model	Value
Power up the AFE	ADC_CONTROL[4] PD	0
If using DMA, set the DMA threshold and enable the appropriate DMA request(s); or set the processor threshold and enable the appropriate threshold interrupt(s) as part of the next step.	ADC_DMAENABLE_SET/ADC_FIFO0DMAREQ/ ADC_FIFO1DMAREQ/ ADC_FIFO0THRESHOLD/ ADC_FIFO1THRESHOLD	0x-
Setup or mask the appropriate interrupts.	ADC_ENABLE_SET	0x-
Configure each step being used to perform an ADC conversion.	ADC_STEPCONFIG_j	0x-
Configure the delays for each step being used to perform an ADC conversion.	ADC_STEPDELAY_j	0x-
Enable each step being used to perform an ADC conversion.	ADC_STEPENABLE	0x-
Wait minimum 4 µs before starting a conversion to provide time for the AFE to power-up. (referenced from POWER_DOWN write to 0)		
Enable the ADC module	ADC_CONTROL[0] MODULE_ENABLE	1

12.1.1.5.1.2 During Operation

Table 12-10. Turn-Off

Step	Register/Bit Field/Programming Model	Value
Turn off ADC module enable bit when finished. This will stop the ADC after the current step is complete.	ADC_CONTROL[0] MODULE_ENABLE	0

Table 12-11. Turn-On After Turn-Off

Step	Register/Bit Field/Programming Model	Value
Enable the ADC module enable bit	ADC_CONTROL[0] MODULE_ENABLE	1

12.1.2 General-Purpose Interface (GPIO)

This chapter describes the General-Purpose Input/Output (GPIO) for the device.

12.1.2.1 GPIO Overview

The General-Purpose Input/Output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

The device has three instances of GPIO modules. The GPIO pins are grouped into banks (16 pins per bank and 9 banks per module), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Since MCU_GPIO0_[23:143], GPIO0_[87:143], and GPIO1_[88:143] are reserved in this device, general purpose interface supports up to 198 pins.

Table 12-12 shows GPIO modules allocation within device domains.

Table 12-12. GPIO Modules Allocation within Device Domains

Module Instance	Domain	
	MCU	MAIN
MCU_GPIO0	✓	-
GPIO0	-	✓
GPIO1	-	✓

Figure 12-7 presents the GPIO modules overview.

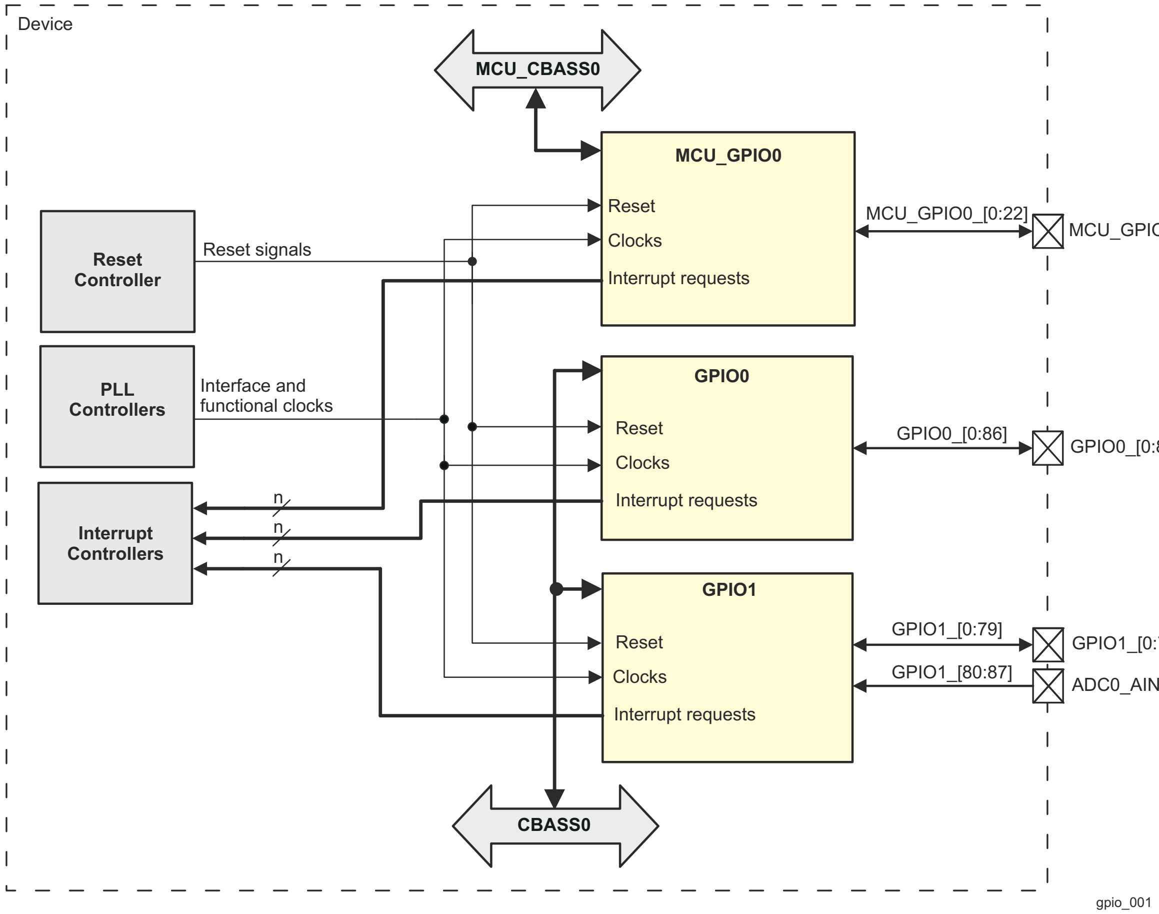

Figure 12-7. GPIO Modules Overview

12.1.2.1.1 GPIO Features

Each channel in the GPIO modules has the following features:

- Supports 9 banks of 16 GPIO signals
- Supports up to 9 banks of interrupt capable GPIOs
- Interrupts:
  - Can enable interrupts for each bank of 16 GPIO signals
  - Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO signal
- Set/clear functionality:
  - Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to another process during GPIO programming).
- Separate Input/Output registers:
  - If preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s) in addition to set/clear.
  - Output register, when read in, reflects output drive status. This, in addition to the input register reflecting pin status this allows wired logic to be implemented.

12.1.2.1.2 GPIO Not Supported Features

- The following apply to MCU_GPIO0:
  - MCU_GPIO0_[23:143] are not pinned out.

  - Interrupts [23:143] are not pinned out.
  - Bank Interrupts [8:2] are not pinned out.
- The following apply to GPIO0:
  - GPIO0_[87:143] are not pinned out.
  - Interrupts [87:143] are not pinned out.
  - Bank Interrupts [8:6] are not pinned out.
- The following apply to GPIO1:
  - GPIO1_[88:143] are not pinned out.
  - Interrupts [88:143] are not pinned out.
  - Bank Interrupts [8:6] are not pinned out.

12.1.2.2 GPIO Environment

The MCU_GPIO0, GPIO[0-1] modules are hereinafter referred to as GPIO module.

This section describes the GPIO external connections (environment).

The general-purpose interface combines three GPIO modules for a flexible, user-programmable, general-purpose input/output (I/O) controller. The general-purpose interface implements functions that are not implemented with the dedicated controllers in the device and require simple input and/or output software-controlled signals. The GPIO allows a variety of custom connections and expands the I/O capabilities of the system to the real world.

The general-purpose interface can physically connect the device to a keyboard matrix and peripheral integrated circuits (ICs).

Figure 12-8 shows a typical application using the general-purpose interface.

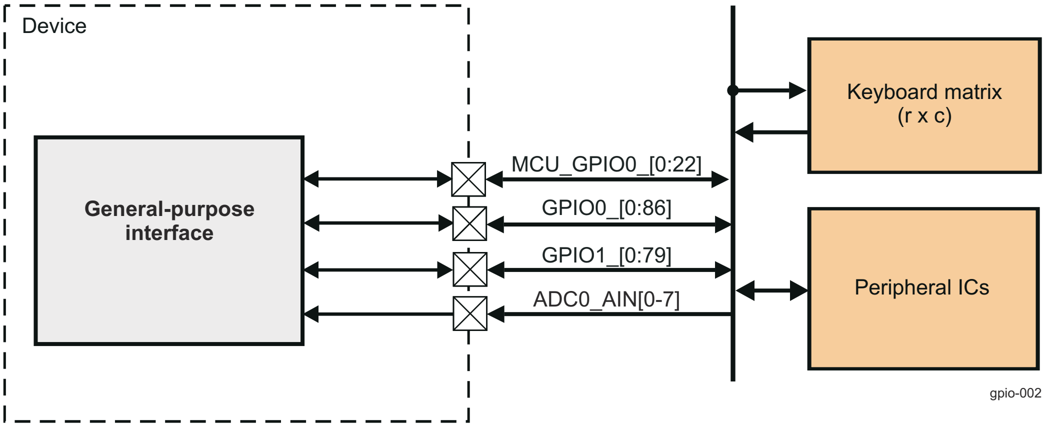

Figure 12-8. GPIO Typical Application

12.1.2.2.1 GPIO Interface Signals

Figure 12-9 shows all of the GPIO interface signals.

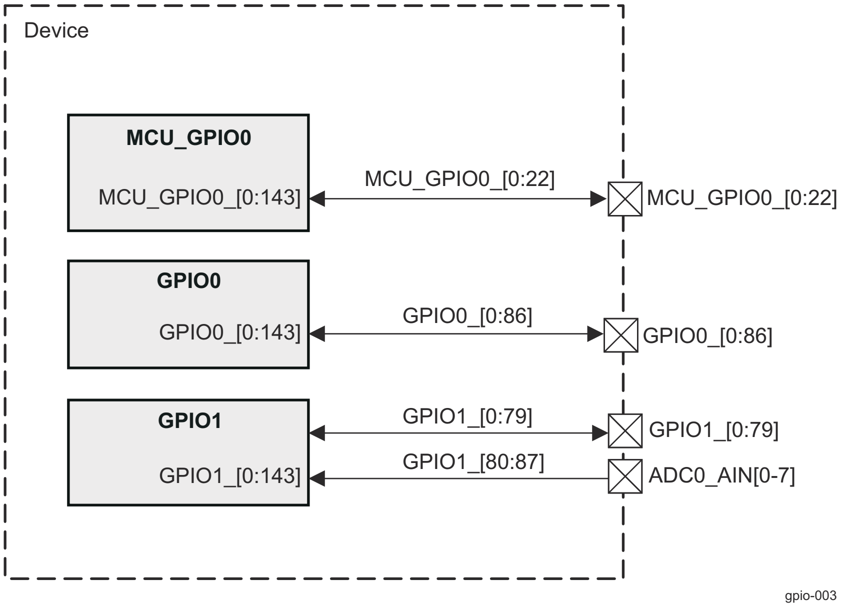

Figure 12-9. GPIO Interface Signals

Table 12-13 describes the GPIO I/O signals.

Table 12-13. GPIO I/O Signals

Module	Module Pin	Device Pin(3)	I/O(1)	Description	Module Pin Reset Value(2)
MCU_GPIO0	GPIO_BANK0_[0-15]	MCU_GPIO0_[0:15]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK1_[0-6]	MCU_GPIO0_[16:22]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK1_[7-15]	NC			
	GPIO_BANK[2-8]_[0-15]	NC			
GPIO0	GPIO_BANK0_[0-15]	GPIO0_[0:15]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK1_[0-15]	GPIO0_[16:31]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK2_[0-15]	GPIO0_[32:47]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK3_[0-15]	GPIO0_[48:63]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK4_[0-15]	GPIO0_[64:79]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK5_[0-6]	GPIO0_[80:86]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK5_[7-15]	NC			
	GPIO_BANK[6-8]_[0-15]	NC			
GPIO1	GPIO_BANK0_[0-15]	GPIO1_[0:15]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK1_[0-15]	GPIO1_[16:31]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK2_[0-15]	GPIO1_[32:47]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK3_[0-15]	GPIO1_[48:63]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK4_[0-12]	GPIO1_[64:79]	I/O	General-purpose input/output. (4)	HiZ
	GPIO_BANK5_[0-7]	GPIO1_[80:87]	I	General-purpose input/output. (4) Signal from ADC0 module ADC0_DIG_TEST[0-7]. (5)(6)	HiZ
	GPIO_BANK5_[8-15]	NC			
	GPIO_BANK[6-8]_[0-15]	NC			

(1) I = Input; O = Output; I/O = Bidirectional

(2) HiZ = High Impedance

(3) NC = Not Connected

(4) Only GPIOs enabled through from the CTRLMMR_MCU_PADCONFIG0 to CTRLMMR_MCU_PADCONFIG24 or from the CTRLMMR_PADCONFIG0 to CTRLMMR_PADCONFIG179 registers for a particular instance can operate on I/O pins. For more information see *Pad Configuration Registers*.

(5) GPIO1_[80-87] input signals are from ADC0 in GPI mode. For more information see *AFE Functional Block Diagram*.

(6) Registers from CTRLMMR_PADCONFIG172[5-4] VGPIO_SEL to CTRLMMR_PADCONFIG179[5-4] VGPIO_SEL are for configuration ADC0_AIN[0-7] inputs.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Data sheet.

12.1.2.3 GPIO Integration

This section describes modules integration in the device, including information about clocks, resets, and hardware requests.

12.1.2.3.1 GPIO Integration in MCU Domain

A single MCU_GPIO0 module is integrated in the device MCU domain. Figure 12-10 shows the integration of MCU_GPIO0.

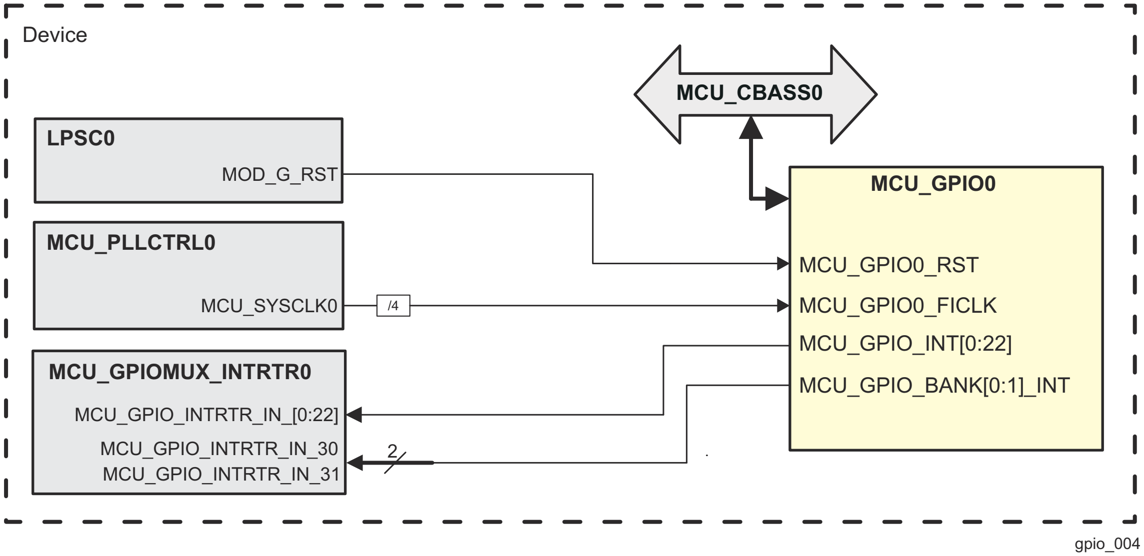

Figure 12-10. MCU_GPIO0 Integration

Table 12-14 through Table 12-17 summarize the integration of MCU_GPIO0 in the device MCU domain.

Table 12-14. MCU_GPIO0 Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_GPIO0	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-15. MCU_GPIO0 Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_GPIO0	MCU_GPIO0_FICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_GPIO0 Functional and Interface clock

Table 12-16. MCU_GPIO0 Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_GPIO0	MCU_GPIO0_RST	MOD_G_RST	LPSC0	MCU_GPIO0 Reset

Table 12-17. MCU_GPIO0 Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_GPIO0	MCU_GPIO_INT[0:22]	MCU_GPIO_INTRTR_IN_[0:22]	MCU_GPIOMUX_INTRTR0	MCU_GPIO0 pins[0:22] interrupt request	Pulse
	MCU_GPIO_BANK0_INT	MCU_GPIO_INTRTR_IN_30	MCU_GPIOMUX_INTRTR0	MCU_GPIO0 bank0 interrupt request	Pulse
	MCU_GPIO_BANK1_INT	MCU_GPIO_INTRTR_IN_31	MCU_GPIOMUX_INTRTR0	MCU_GPIO0 bank1 interrupt request	Pulse

Note

GPIO interrupts are further described in Section 12.1.2.4.3 , *Interrupt and Event Generation*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.1.2.3.2 GPIO Integration in MAIN Domain

There are two GPIO modules integrated in the device MAIN domain - GPIO0, GPIO1. Figure 12-11 shows the integration of GPIO.

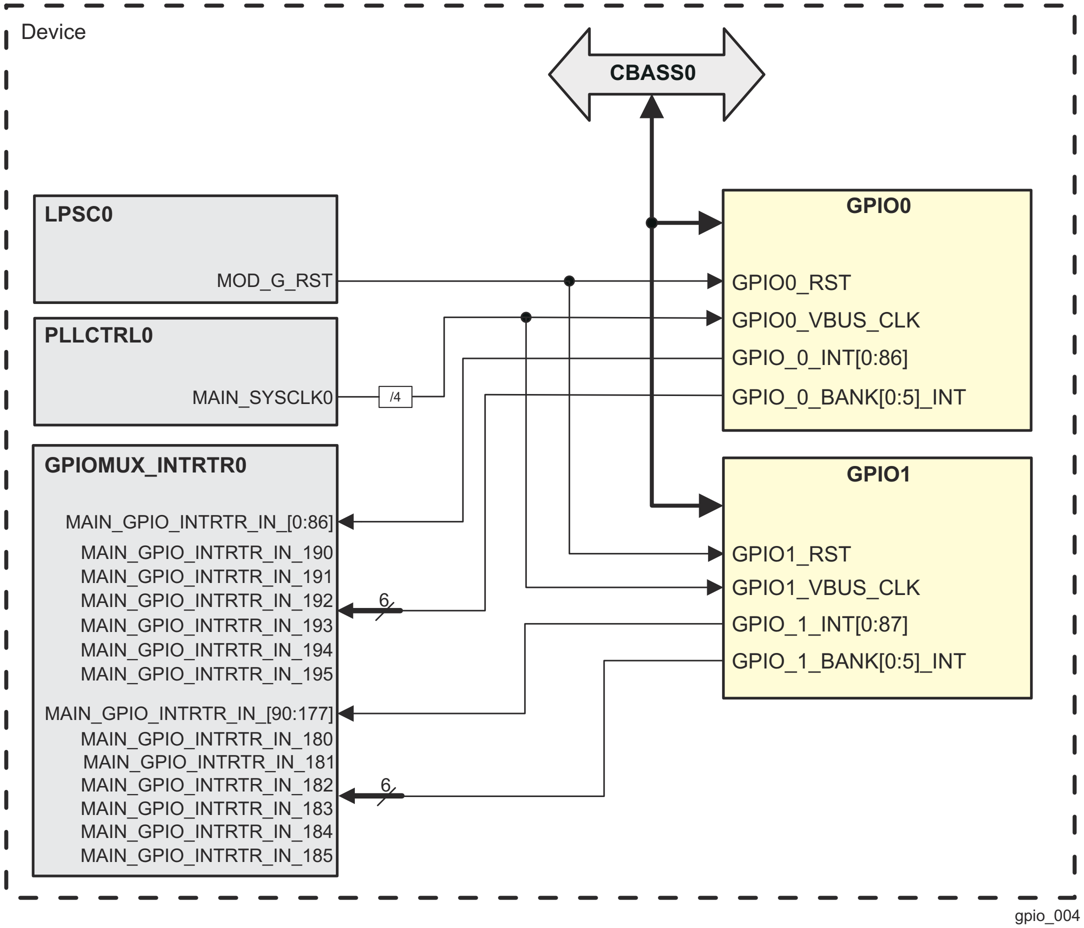

Figure 12-11. GPIO Integration

Table 12-18 through Table 12-21 summarize the integration of GPIO0, GPIO1 in the device MAIN domain.

Table 12-18. GPIO Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
GPIO0	PSC0	PD0	LPSC0	CBASS0

Table 12-18. GPIO Integration Attributes (continued)

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
GPIO1	PSC0	PD0	LPSC0	CBASS0

Table 12-19. GPIO Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
GPIO0	GPIO0_VBUS_FICLK	SYSCLK0/4	PLLCTRL0	GPIO0 Functional and Interface clock
GPIO1	GPIO1_VBUS_FICLK	SYSCLK0/4	PLLCTRL0	GPIO1 Functional and Interface clock

Table 12-20. GPIO Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
GPIO0	GPIO0_RST	MOD_G_RST	LPSC0	GPIO0 Reset
GPIO1	GPIO1_RST	MOD_G_RST	LPSC0	GPIO1 Reset

Table 12-21. GPIO Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO0	GPIO_0_INT[0:86]	MAIN_GPIO_INTRTR_IN_[0:86]	GPIOMUX_INTRTR0	GPIO0 pins[0:86] interrupt request	Pulse
	GPIO_0_BANK0_INT	MAIN_GPIO_INTRTR_IN_190	GPIOMUX_INTRTR0	GPIO0 bank0 interrupt request	Pulse
	GPIO_0_BANK1_INT	MAIN_GPIO_INTRTR_IN_191	GPIOMUX_INTRTR0	GPIO0 bank1 interrupt request	Pulse
	GPIO_0_BANK2_INT	MAIN_GPIO_INTRTR_IN_192	GPIOMUX_INTRTR0	GPIO0 bank2 interrupt request	Pulse
	GPIO_0_BANK3_INT	MAIN_GPIO_INTRTR_IN_193	GPIOMUX_INTRTR0	GPIO0 bank3 interrupt request	Pulse
	GPIO_0_BANK4_INT	MAIN_GPIO_INTRTR_IN_194	GPIOMUX_INTRTR0	GPIO0 bank4 interrupt request	Pulse
	GPIO_0_BANK5_INT	MAIN_GPIO_INTRTR_IN_195	GPIOMUX_INTRTR0	GPIO0 bank5 interrupt request	Pulse
GPIO1	GPIO_1_INT[0:87]	MAIN_GPIO_INTRTR_IN_[90:177]	GPIOMUX_INTRTR0	GPIO1 pins[0:87] interrupt request	Pulse
	GPIO_1_BANK0_INT	MAIN_GPIO_INTRTR_IN_180	GPIOMUX_INTRTR0	GPIO1 bank0 interrupt request	Pulse
	GPIO_1_BANK1_INT	MAIN_GPIO_INTRTR_IN_181	GPIOMUX_INTRTR0	GPIO1 bank1 interrupt request	Pulse
	GPIO_1_BANK2_INT	MAIN_GPIO_INTRTR_IN_182	GPIOMUX_INTRTR0	GPIO1 bank2 interrupt request	Pulse
	GPIO_1_BANK3_INT	MAIN_GPIO_INTRTR_IN_183	GPIOMUX_INTRTR0	GPIO1 bank3 interrupt request	Pulse
	GPIO_1_BANK4_INT	MAIN_GPIO_INTRTR_IN_184	GPIOMUX_INTRTR0	GPIO1 bank4 interrupt request	Pulse
	GPIO_1_BANK5_INT	MAIN_GPIO_INTRTR_IN_185	GPIOMUX_INTRTR0	GPIO1 bank5 interrupt request	Pulse

Note

GPIO interrupts are further described in Section 12.1.2.4.3 , *Interrupt and Event Generation*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.1.2.4 GPIO Functional Description

12.1.2.4.1 GPIO Block Diagram

Figure 12-12 shows the general-purpose interface block diagram.

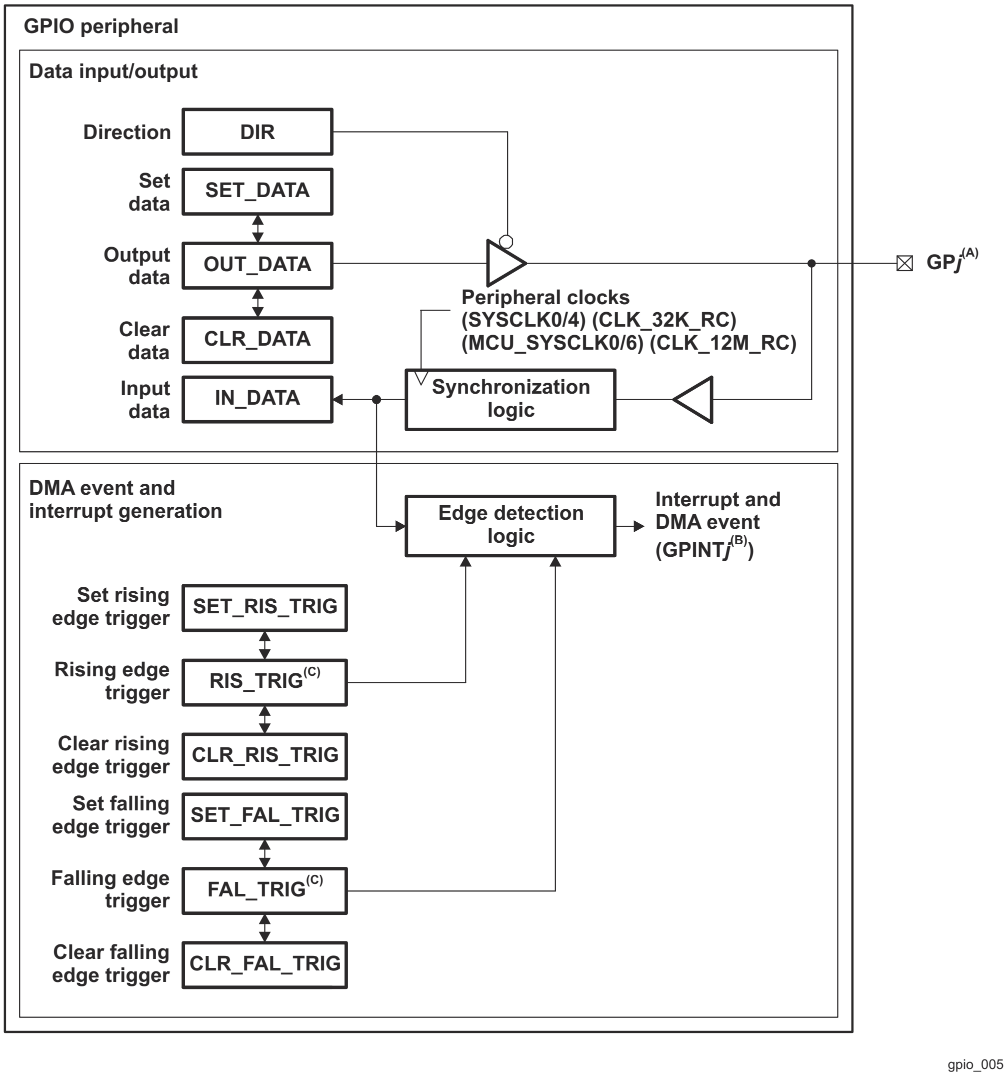

Note

Some of the GPj pins are muxed with other device signals. For details, see the device-specific Data sheet.

Note

All GPINTj can be used as host CPU interrupts and synchronization events to the DMA.

Note

The RIS_TRIG and FAL_TRIG registers are internal to the GPIO module and are not visible to the host CPU.

Note

The synchronization logic and tristate buffer are present in the SoC pinmux logic.

Figure 12-12. GPIO Block Diagram

12.1.2.4.2 GPIO Function

Each GPIO pin (GPj) can be independently configured as either an input or an output using the GPIO direction registers. The GPIO direction register (DIR) specifies the direction of each GPIO signal. Logic 0 indicates the GPIO pin is configured as output, and logic 1 indicates input.

When configured as output, writing a 0x1 to a bit in the set data register drives the corresponding GPj to a logic-high state. Writing a 0x1 to a bit in the clear data register drives the corresponding GPj to a logic-low state. The output state of each GPj can also be directly controlled by writing to the output data register.

For example, to set GP8 to a logic-high state, the software can perform one of the following:

- Write 100h to the GPIO_SET_DATA01 register.
- Write 0h to the GPIO_DIR01 register to configure as output pin.
- Read in GPIO_OUT_DATA01 register, change bit 8 to 0x1, and write the new value back to GPIO_OUT_DATA01.

To set GP8 to a logic-low state, the software can perform one of the following:

- Write 100h to the GPIO_CLR_DATA01 register.
- Write 0h to the GPIO_DIR01 register to configure as output pin.
- Read in GPIO_OUT_DATA01 register, change bit 8 to 0x0, and write the new value back to GPIO_OUT_DATA01.

Note that writing a 0x0 to bits in the set data and clear data registers does not affect the GPIO pin state.

Also, for GPIO pins configured as input, writing to the set data, clear data, or output data registers does not affect the pin state.

For a GPIO pin configured as input, reading the input data register (IN_DATA) will return the pin state. Reading the SET_DATA register or the CLR_DATA data register will return the value in OUT_DATA, not the actual pin state. The pin state is available by reading the input data register. Note that when the direction is configured as input, the output state is determined by software's programming set/clear/output registers, and may not agree with the pin state, which is driven by an external device.

12.1.2.4.3 GPIO Interrupt and Event Generation

Each GPIO pin (GPj) can be configured to generate a host CPU interrupt (GPINTj) or a synchronization event to the DMA (GPINTj). Configuration is on per-bank basis. Each bit of the BINTEN parameter dictates YES/NO option for each bank. Bit 0 controls bank 0, bit 1 controls bank 1, and so on.

The interrupt and DMA event can be generated on the rising-edge, falling-edge, or on both edges of the GPIO signal . The edge detection logic is synchronized to the GPIO peripheral clock.

The direction of the GPIO pin does not need to be input when using the pin to generate the interrupt or DMA event. When the GPIO pin is configured as input, transitions on the pin trigger interrupts or DMA events. When the GPIO pin is configured as output, software can toggle the GPIO output register to change the pin state and in turn trigger the interrupt or DMA event.

Note that the direction of the pin need not be input for interrupt generation to work. When the GPIO pin is configured as input, transitions on the pin trigger interrupts. When the GPIO pin is configured as output, firmware can toggle the GPIO output register to change the pin state, and in turn trigger interrupts.

Each interrupt output of GPIO signal are available at the module boundary. Each group of 16 GPIO_INTR_INTj signals also has their masked interrupt outputs ORed together to generate a per bank interrupt, available at the module boundary. The idea is to either connect individual interrupts or per bank interrupts to the system interrupt controller.

12.1.2.4.3.1 Interrupt Enable (per Bank)

The GPIO_BINTEN register provides interrupt enable/disable feature for each bank of 16 GPINT signals.

12.1.2.4.3.2 Trigger Configuration (per Bit)

Two internal registers, RIS_TRIG and FAL_TRIG, specify which edge of the GPj signal generates an interrupt or DMA event. Each bit in these two registers corresponds to a GPj pin. Table 12-22 describes the host CPU interrupt and DMA event generation of GPj pin based on the bit settings of the RIS_TRIG and FAL_TRIG registers.

Table 12-22. GPIO Interrupt and DMA Event Configuration Options

RIS_TRIG Bit n	FAL_TRIG Bit n	Host CPU Interrupt and DMA Event Generation
0	0	GPINTj interrupt and DMA event is disabled
0	1	GPINTj interrupt and DMA event is triggered on falling edge of GPj signal
1	0	GPINTj interrupt and DMA event is triggered on rising edge of GPj signal
1	1	GPINTj interrupt and DMA event is triggered on both rising and falling edge of GPj signal

The RIS_TRIG and FAL_TRIG registers are not directly accessible or visible to the host CPU. These registers are accessed indirectly through four registers: SET_RIS_TRIG, CLR_RIS_TRIG, SET_FAL_TRIG, and CLR_FAL_TRIG. Writing 1 to a bit on the SET_RIS_TRIG register sets the corresponding bit on the RIS_TRIG register. Writing 1 to a bit of the CLR_RIS_TRIG register clears the corresponding bit on the RIS_TRIG register. Writing to the SET_FAL_TRIG and CLR_FAL_TRIG registers works the same way on the FAL_TRIG register.

Reading the SET_RIS_TRIG or CLR_RIS_TRIG register returns the value of the RIS_TRIG register. Reading from the SET_FAL_TRIG or CLR_FAL_TRIG register returns the value of the FAL_TRIG register.

To use the GPIO pins as sources for host CPU interrupts and DMA events, the associated bank interrupt enable register bit in GPIO_BINTEN must also be set to 1. For example, to enable GPIO0_19 (which is in bank 1), GPIO_BINTEN[1] = 1 should be set to enable interrupts for bank 1.

12.1.2.4.3.3 Interrupt Status and Clear (per Bit)

The INTSTAT registers provide interrupt status upon reading, and interrupt clear feature upon writing 1 to the corresponding bit position(s). Upon receiving an interrupt, the ISR can examine the interrupt status and clear the processed interrupts.

Note

The GPIO module generates an interrupt pulse on the individual GPINT interrupt in response to each occurrence of the specified edge condition. Therefore, for GPINT signals having their interrupts routed directly to the interrupt controller, it is not necessary to clear the status bits in this module. The interrupt status and clear register is a facility for the per-bank interrupt connection.

12.1.2.4.4 GPIO Interrupt Connectivity

Because this device muxes GPIO signals with other functional signals, the availability of any particular GPIO, and hence the usability of the associated interrupt, changes based on the use case pin muxing. Due to the large number of possible GPIO interrupt sources, routing all interrupt events to each processing element is impractical. Since most applications do not typically require a large number of GPIO interrupts, the interrupt uncertainty is resolved by mapping all GPIO interrupts to a series of event muxes implemented using Interrupt Router (IntRouter) modules. These muxes allow any one of the available GPIO interrupts to be selected and passed on as an event to the various processor interrupt controllers and DMA controllers. Event selection is controlled through associated registers within each IntRouter.

The GPIO bank interrupts already represent a consolidation of the 16 GPIO interrupts associated with each bank and are routed directly to various interrupt controllers rather than through the GPIO IntRouters.

Figure 12-13 and Figure 12-14 shows the GPIO Interrupt Routers connectivity. Refer to *Interrupt Routers* for more details on the GPIO Interrupt Routers connectivity.

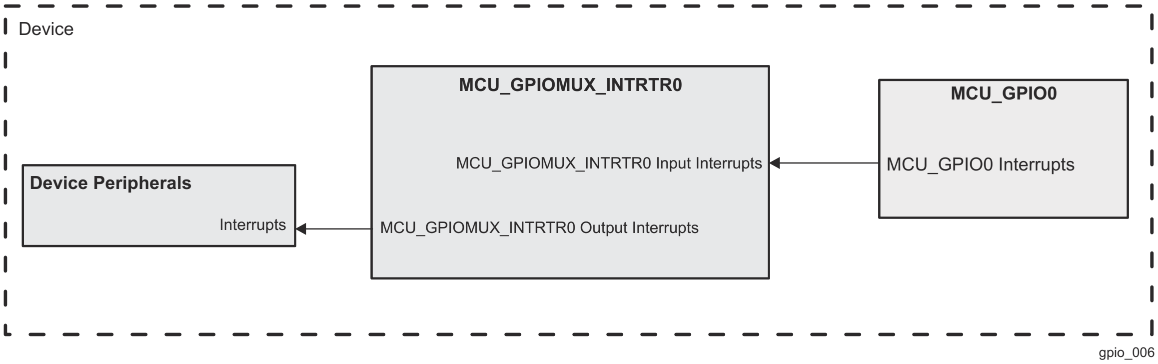

Figure 12-13. MCU_GPIO Interrupt Router Connectivity

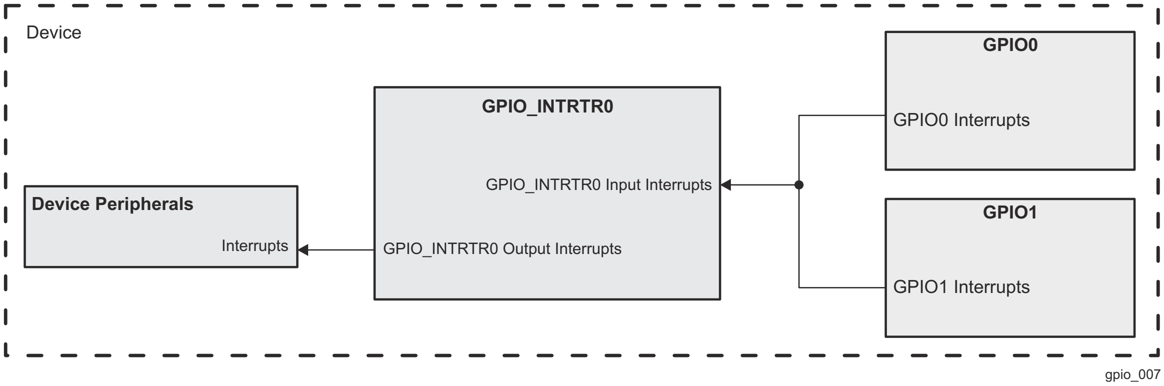

Figure 12-14. GPIO Interrupt Router Connectivity

12.1.2.4.5 GPIO Emulation Halt Operation

The GPIO peripheral is not affected by emulation halts.

12.1.2.5 GPIO Programming Guide

12.1.2.5.1 GPIO Low-Level Programming Models

12.1.2.5.1.1 Global Initialization

12.1.2.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the general-purpose interface module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the environment and integration of the general-purpose interface. For more information, see *GPIO Environment*, and *GPIO Integration*.

Table 12-23. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC0	Module reset must be enabled. For more information about the module configuration, see *Reset*
PLLCTRL0	Interface and functional clocks must be enabled. For more information about the module configuration, see *Clocking*
MCU_PLLCTRL0	Interface and functional clocks must be enabled. For more information about the module configuration, see *Clocking*.
GPIOMUX_INTRTR0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling GPIOMUX_INTRTR0 interrupts, see *Interrupts*.
MCU_GPIOMUX_INTRTR0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MCU_GPIOMUX_INTRTR0 interrupts, see *Interrupts*.
Interconnects	For information about the MCU_CBASS0, and CBASS0 interconnects configuration, see *System Interconnect*.

12.1.2.5.1.1.2 GPIO Module Global Initialization

This procedure initializes the general-purpose Interface module after a power-on reset (POR) or software reset.

Table 12-24. GPIO Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure GPIO channels as input or output of the corresponding bank	DIR	-h
Interrupt requests configuration		
Configure detection events	SET_RIS_TRIG and/or SET_FAL_TRIG	-h
Clear interrupt status	INTSTAT	FFFFh
Enable interrupts for desired banks [0:8]	GPIO_BINTEN[8-0]	-h

12.1.2.5.1.2 GPIO Operational Modes Configuration

12.1.2.5.1.2.1 GPIO Read Input Register

Table 12-25. GPIO Read Input Register

Step	Register/Bit Field/Programming Model	Value
Read interrupt status of the corresponding bank	INTSTAT	-h
Read input register value	IN_DATA	-h
Clear interrupt status	INTSTAT	FFFF FFFFh

12.1.2.5.1.2.2 GPIO Set Bit Function

Table 12-26. GPIO Set Bit Function

Step	Register/Bit Field/Programming Model	Value
Write 1h to set desired bit(s) in SET_DATA register.	SET_DATA	-h

12.1.2.5.1.2.3 GPIO Clear Bit Function

Table 12-27. GPIO Clear Bit Function

Step	Register/Bit Field/Programming Model	Value
Write 1h to clear desired bit(s) in CLR_DATA register.	CLR_DATA	-h

12.1.3 Inter-Integrated Circuit (I2C) Interface

This section describes the Inter-Integrated Circuit (I2C) module in the device.

12.1.3.1 I2C Overview

The device contains six multicontroller Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm and any I^2C-bus-compatible device that connects via the I^2C serial bus. External components attached to the I^2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I^2C interface.

Each multicontroller I2C module can be configured to act like a target or controller I^2C-compatible device.

The MCU_I2C0, and I2C0 controllers have dedicated I^2C compliant open drain buffers and support high speed mode (up to 3.4 Mbps in 1.8 V mode and up to 400 kbps in 3.3 V mode). The MCU_I2C1, I2C1, I2C2, I2C3 controllers are multiplexed with standard LVCMOS I/O, connected to emulate open drain, and support fast mode (up to 400 kbps in 1.8 V/3.3 V mode). The I^2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic 1.

For the specific I/O timing characteristics of the different I2C instances, see the device-specific Datasheet.

Table 12-28 shows I2C modules allocation within device domains.

Table 12-28. I2C Modules Allocation within Device Domains

Module Instance	Domain	
	MCU	MAIN
MCU_I2C0	✓	-
MCU_I2C1	✓	-
I2C0	-	✓
I2C1	-	✓
I2C2	-	✓
I2C3	-	✓

Figure 12-15 shows the I2C modules overview.

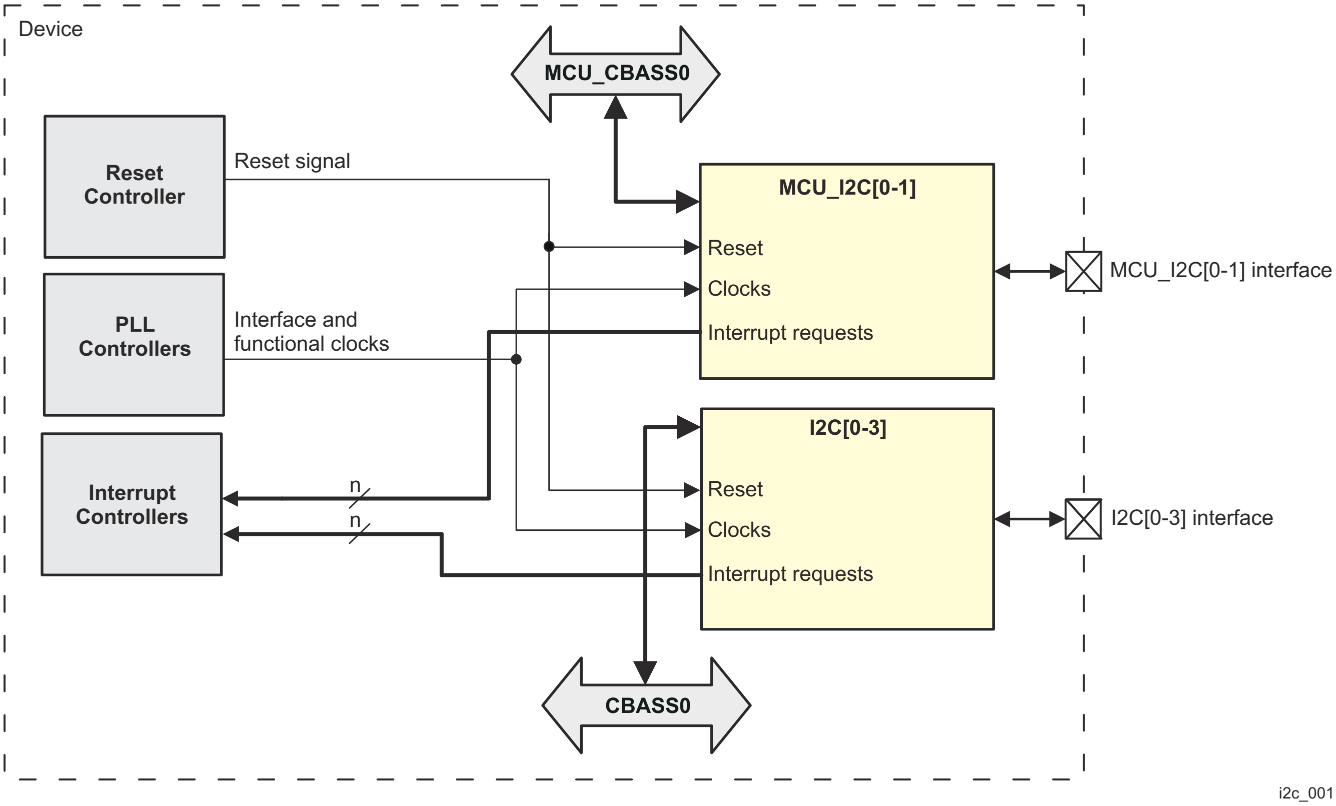

Figure 12-15. I2C Modules Overview

12.1.3.1.1 I2C Features

Each multicontroller I2C module has the following features:

- Compliant with Philips I^{2}C-bus specification version 2.1
- Supports a standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- 7-bit and 10-bit device addressing modes
- General call
- Start/Restart/Stop
- Multicontroller transmitter/target receiver mode
- Multicontroller receiver/target transmitter mode
- Combined controller transmit/receive and receive/transmit mode
- Built-in FIFO for buffered read
  - FIFO depth has a fixed size of 32 Bytes
- Module enable/disable capability
- Programmable multitarget channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Low power consumption
- Support Auto Idle mechanism
- Support Idle Request/Idle Acknowledge handshake mechanism
- Support for asynchronous wakeup mechanism
- Wide interrupt capability

12.1.3.1.2 I2C Not Supported Features

- Serial Camera Control Bus (SCCB) Protocol
- DMA Mode

- Full I^{2}C electrical compliance for I2C modules using device pins with LVCMOS voltage buffers (Refer to chapter 4 of the device-specific Datasheet for details related to device *Terminal Configuration and Functions*)
- Local power management of clock activity
- Debug suspend mode
- Asynchronous wakeup

12.1.3.2 I2C Environment

The MCU_I2C[0-1], and I2C[0-3] modules are hereinafter referred to as I2C module.

This section describes the I2C external connections (environment).

12.1.3.2.1 I2C Typical Application

Figure 12-16 shows the multicontroller I2C controller and their related connections with I^{2}C-compliant devices.

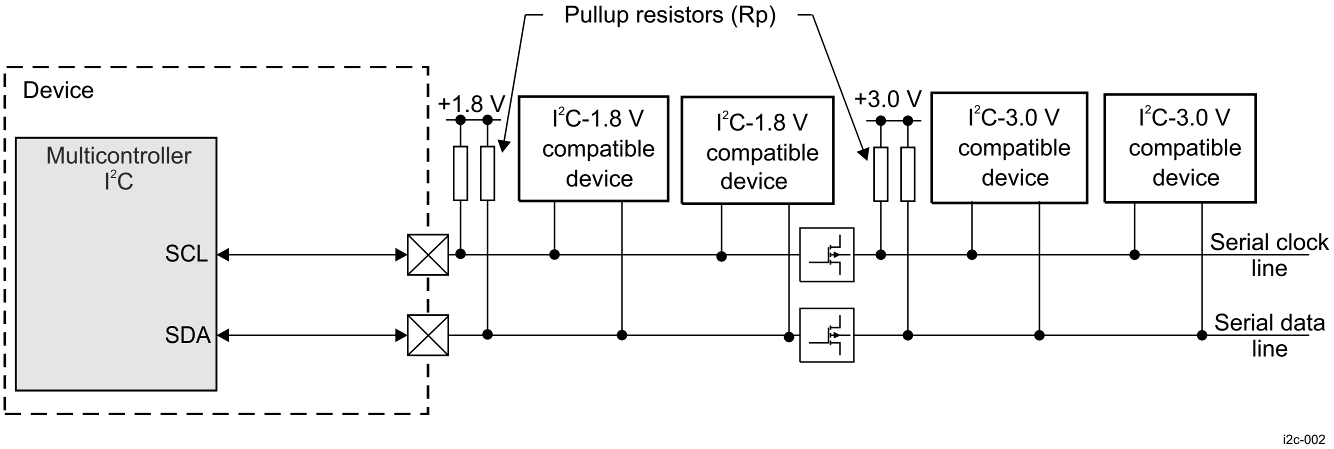

Figure 12-16. I2C and Typical Connections to I2C Devices

12.1.3.2.1.1 I2C Pins for Typical Connections in I2C Mode

Figure 12-17 shows the multicontroller I2C pins used for typical connections with I^{2}C devices.

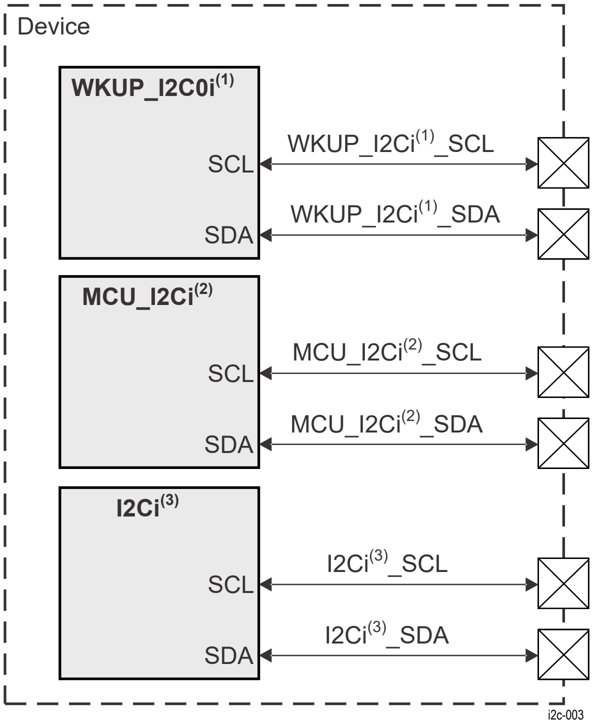

1. i = 0 to (number of devices - 1) in WKUP Domain, if applicable
2. i = 0 to (number of devices - 1) in MCU Domain, if applicable
3. i = 0 to (number of devices - 1) in MAIN Domain, if applicable

Figure 12-17. I2C Interface Signals

12.1.3.2.1.2 I2C Interface Typical Connections

Table 12-29 describes the I2C I/O signals.

Table 12-29. I2C I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value
			WKUP_I2Ci(2)	
SCL	WKUP_I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	WKUP_I2Ci(2)_SDA	I/O	I^2C serial data line.	1
			MCU_I2Ci(2)	
SCL	MCU_I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	MCU_I2Ci(2)_SDA	I/O	I^2C serial data line.	1
			I2Ci(2)	
SCL	I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	I2Ci(2)_SDA	I/O	I^2C serial data line.	1

(1) I = Input; O = Output; I/O = Bidirectional

(2) i represents an I2C instance. See the device datasheet for available domains and I2C instances.

12.1.3.2.1.3

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.1.3.2.2 I2C Typical Connection Protocol and Data Format

12.1.3.2.2.1 I2C Serial Data Format

The I2C controller operates in 8-bit word data format (byte write access supported for the last access). Each byte transmitted or received on the serial data line is 8 bits long. The number of bytes that can be transmitted or received is not restricted. The data is transferred with the most-significant bit (MSB) first. In receiver mode, each byte is followed by an acknowledge bit from the I2C module.

Figure 12-18 shows a typical I^2C communication format.

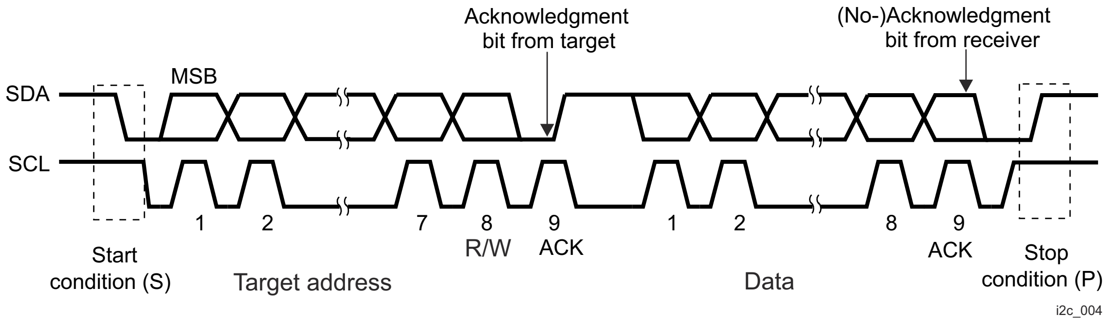

Figure 12-18. I2C Data Transfer

12.1.3.2.2.2 I2C Data Validity

The data on the serial data line (SDA) must be stable during the high period of the serial clock line. The high and low states of the data line can change only when the clock signal on the serial clock line (SCL) is low.

Figure 12-19 is an example of data validity requirements.

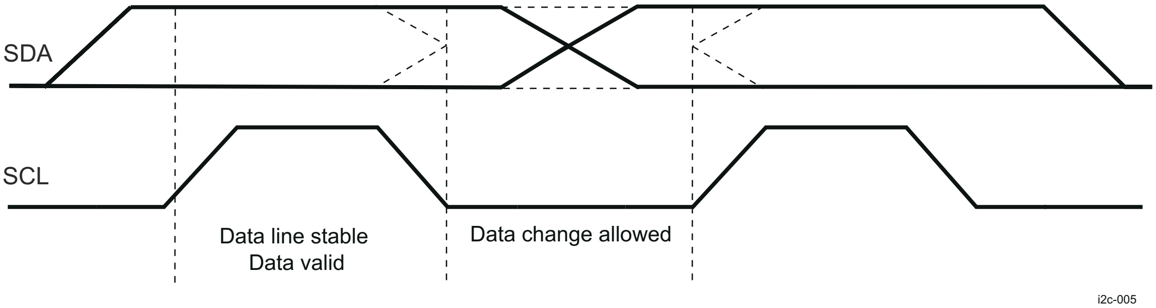

Figure 12-19. I2C Bit Transfer on the I2C Bus

12.1.3.2.2.3 I2C Start and Stop Conditions

The I2C module generates start (S) and stop (P) conditions when it is configured as a controller.

- An S condition is a high-to-low transition on the serial data line while serial clock line is high.
- A P condition is a low-to-high transition on the serial data line while serial clock line is high.

The bus is considered busy after the S condition (the I2C_IRQSTATUS_RAW [12] BB bit is 1 to indicate that the bus is busy) and free after the P condition (the I2C_IRQSTATUS_RAW [12] BB bit is 0 to indicate that the bus is free).

Figure 12-20 shows the waveforms that occur during an S and a P condition.

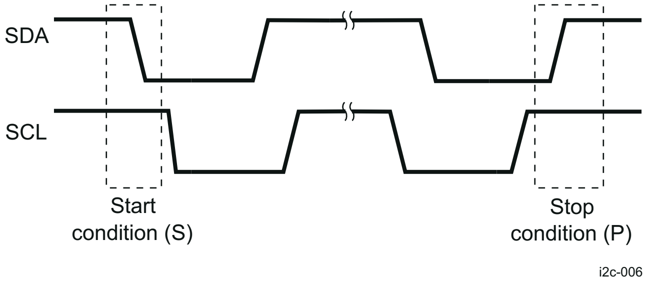

Figure 12-20. I2C S and P Condition Events

Note

I2C controller does not support messages non-compliant with I^{2}C standard. Void messages are non-standard I^{2}C messages and will lockup the controller. A void message is a START condition followed by a STOP condition, in other words, while the bus is free the SDA line is pulled low (START) and then released (STOP). This would result in a timeout (software) of the next controller transfer which would never complete. A soft reset of the controller is recommended for recovery.

12.1.3.2.2.4 I2C Addressing

The I2C module supports two data formats in fast/standard (F/S) mode:

- 7-bit/10-bit addressing format
- 7-bit/10-bit addressing format with repeated start (Sr) condition

12.1.3.2.2.4.1 Data Transfer Formats in F/S Mode

Figure 12-21 shows the I2C data transfer formats in F/S mode.

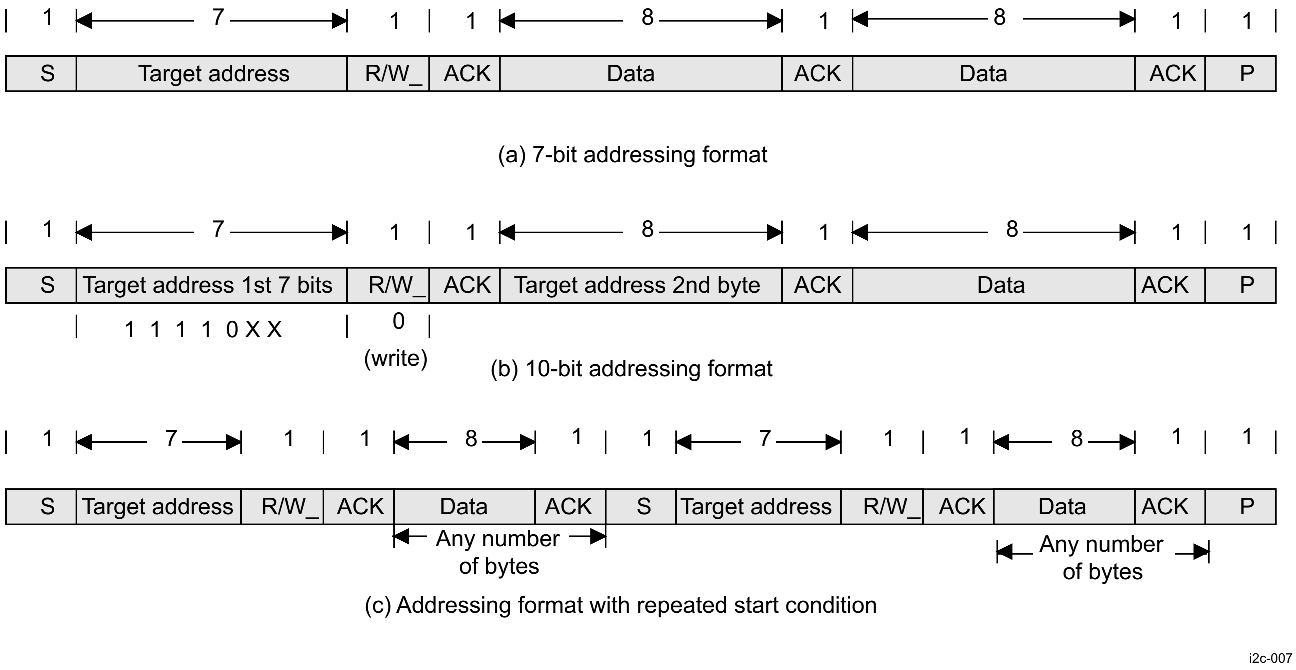

Figure 12-21. I2C Data Transfer Formats in F/S Mode

The first word after an S condition consists of 8 bits. In acknowledge mode, an extra dedicated acknowledgment bit is inserted after each byte.

In addressing formats with 7-bit addresses, the first byte is composed of 7 MSB target address bits and 1 least-significant bit (LSB) R/W_ bit.

The LSB R/W_ bit of the address byte indicates the transmission direction of the data bytes that follow it. If R/W_ is 0, the controller writes data to the selected target; if it is 1, the controller reads data from the target.

In addressing formats with 10-bit addresses, the structure of the first byte is 11110XXY, where XX is the two MSBs of the 10-bit addresses, and Y is the R/W_ bit. If the R/W_ bit is 0, the next byte contains the last 8 bits of the target address. If the R/W_ bit is 1, the next byte contains data transmitted from the target to the controller.

12.1.3.2.2.4.2 Data Transfer Format in HS Mode

Figure 12-22 shows the I2C data transfer format in HS mode.

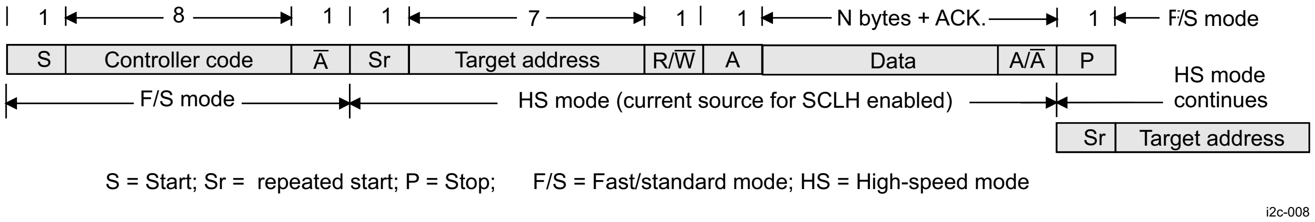

Figure 12-22. HS I2C Data Transfer in HS Mode

Each multicontroller I2C controller can also operate in HS mode. In this case, after the S condition, the module, which is in F/S mode, writes the controller code address (0x00001XXX, where XXX is the variable portion of the controller code) on the bus. No device connected on the same bus acknowledges this address. The module switches the clock to the HS clock and after an Sr condition, and sends the target address and the data, as shown in Figure 12-22.

12.1.3.2.2.5 I2C Controller Transmitter

In controller transmitter mode, data assembled in one of the previously described data formats is shifted out on the serial data line SDA in sync with the self-generated clock pulses on the serial clock line SCL. The clock pulses are inhibited and SCL is held low when the intervention of the processor is required (XUDF) after a byte is transmitted.

12.1.3.2.2.6 I2C Controller Receiver

Controller receiver mode can be entered only from controller transmitter mode. With any of the address formats (a), (b), or (c) (see Figure 12-21), if R/W_ is high, the module enters controller receiver mode after the target address byte and bit R/W_ are transmitted. Serial data bits received on bus line SDA are shifted in synchronization with the self-generated clock pulses on SCL.

12.1.3.2.2.7 I2C Target Transmitter

Target transmitter mode can be entered only from target receiver mode. With any of the address formats (a), (b), or (c) (see Figure 12-21), the target transmitter is entered if the target address byte is the same as its own address and bit R/W_ is transmitted, if R/W_ is high. The target transmitter shifts the serial data out on the data line SDA in sync with the clock pulses that are generated by the controller device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (XUDF).

12.1.3.2.2.8 I2C Target Receiver

In this mode, serial data bits received on the bus line SDA are shifted-in in sync with the clock pulses on SCL that are generated by the controller device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (ROVR) after a byte is received.

12.1.3.2.2.9 I2C Bus Arbitration

If two or more controller transmitters start a transmission on the same bus almost simultaneously, an arbitration procedure is invoked. The arbitration procedure uses the data presented on the serial bus by the competing transmitters. When a transmitter senses that a high signal it has presented on the bus has been overruled by a low signal, it switches to the target receiver mode, sets the arbitration lost (I2C_IRQSTATUS_RAW[0] AL) flag, and generates the arbitration lost interrupt. Figure 12-23 shows the arbitration procedure between two devices. The arbitration procedure gives priority to the device that transmits the serial data stream with the lowest binary value. If two or more devices send identical first bytes, arbitration continues on the subsequent bytes.

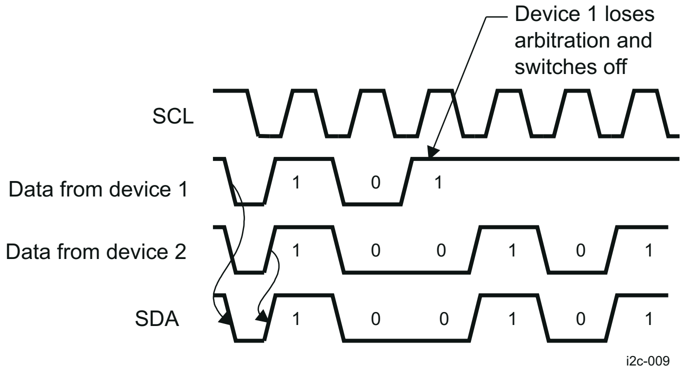

Figure 12-23. I2C Arbitration Between Controller Transmitters

12.1.3.2.2.10 I2C Clock Generation and Synchronization

Under normal conditions, only one controller device generates the clock signal - SCL. However, there are two or more controller devices during the arbitration procedure, and the clock must be synchronized so that the data output can be compared. The wired-AND property of the clock line means that a device that first generates a low period of the clock line overrules the other devices. At this high/low transition, the clock generators of the other devices are forced to start generation of their own low period. The clock line is then held low by the device with the longest low period, while the other devices that finish their low periods must wait for the clock line to be released before starting their high periods. A synchronized signal on the clock line is thus obtained, where the slowest device determines the length of the low period and the fastest device determines the length of the high period. If a device pulls down the clock line for a longer time, the result is that all clock generators must enter the WAIT-state. In this way a target can slow down a fast controller and the slow device can create enough time to store a received byte or prepare a byte to be transmitted (clock stretching).

Note

In case the SCL or SDA lines are stuck low, a bus clearing operation is supported:

- If the clock line (SCL) is stuck low, the preferential procedure is to reset the bus using the hardware reset signal if the I^{2}C devices have hardware reset inputs. If the I^{2}C devices do not have hardware reset inputs, cycle power to the devices to activate the mandatory internal power-on reset (POR) circuit.
- If the data line (SDA) is stuck low, the controller should send nine clock pulses. The device that held the bus low should release it sometime within those nine clocks. If not, then use the hardware reset or cycle power to clear the bus.

Figure 12-24 shows clock synchronization.

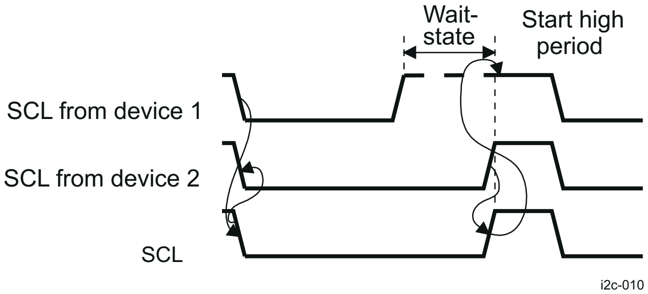

Figure 12-24. I2C Clock Generators Synchronization

12.1.3.3 I2C Integration

This section describes I2C integration in the device, including information about clocks, resets, and hardware requests.

12.1.3.3.1 I2C Integration in MCU Domain

There are two I2C modules integrated in the device MCU domain - MCU_I2C0 and MCU_I2C1. Figure 12-25 shows the integration of MCU_I2C0 and MCU_I2C1.

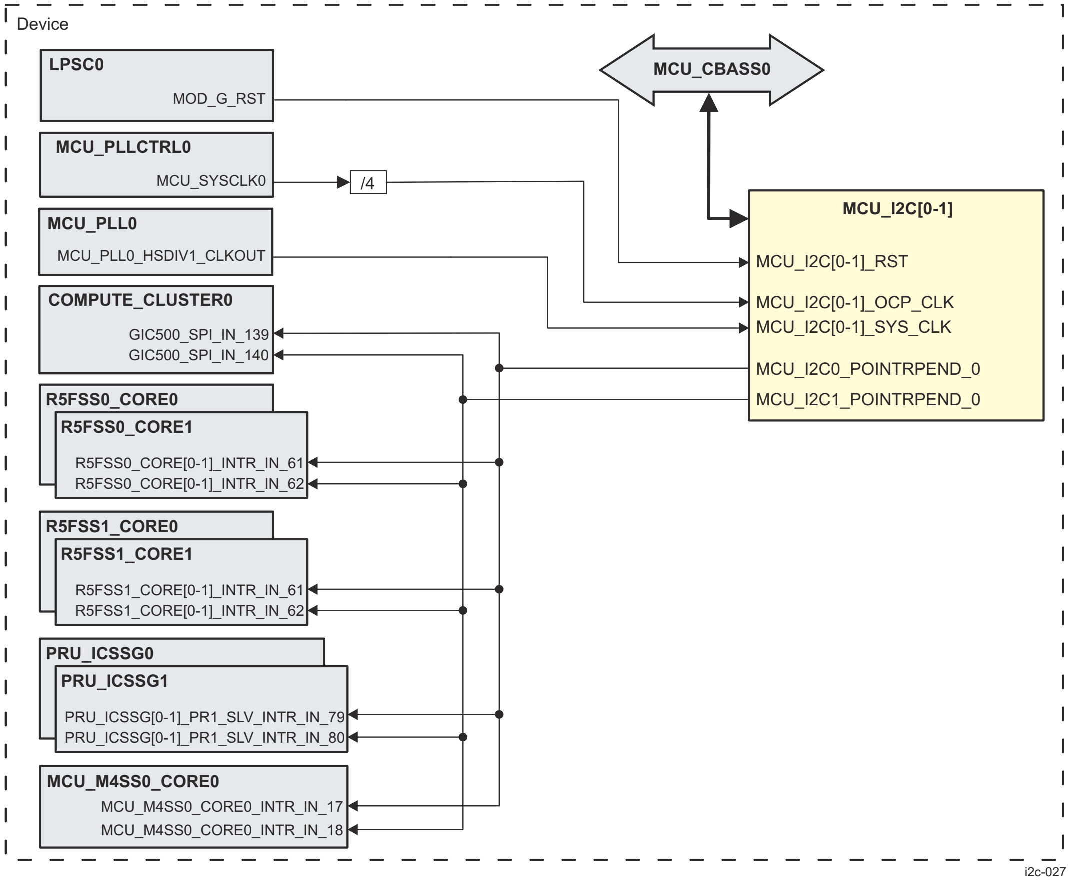

Figure 12-25. MCU_I2C[0-1] Integration

Table 12-30 through Table 12-33 summarize the integration of MCU_I2C[0-1] in device MCU domain.

Table 12-30. MCU_I2C[0-1] Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_I2C0	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-30. MCU_I2C[0-1] Integration Attributes (continued)

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_I2C1	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-31. MCU_I2C[0-1] Clocks (1)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_I2C0	MCU_I2C0_OCP_CLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_I2C0 interface clock
	MCU_I2C0_SYS_CLK	MCU_PLL0_HSDIV1_CLKOUT	MCU_PLL0	MCU_I2C0 functional clock
MCU_I2C1	MCU_I2C1_OCP_CLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_I2C1 interface clock
	MCU_I2C1_SYS_CLK	MCU_PLL0_HSDIV1_CLKOUT	MCU_PLL0	MCU_I2C1 functional clock

(1) When 3.4Mbps mode is needed, MCU_I2C0_SYS_CLK or MCU_I2C1_SYS_CLK must be set to 96MHz. In this case UART IrDA mode cannot be supported since it requires 48MHz clock.

Table 12-32. MCU_I2C[0-1] Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_I2C0	MCU_I2C0_RST	MOD_G_RST	LPSC0	MCU_I2C0 reset
MCU_I2C1	MCU_I2C1_RST	MOD_G_RST	LPSC0	MCU_I2C1 reset

Table 12-33. MCU_I2C[0-1] Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_I2C0	MCU_I2C0_POINTRPEND_0	GIC500_SPI_IN_139	COMPUTE_CLUSTER0	MCU_I2C0 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_61	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_61	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_61	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_61	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_INTR_IN_79	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_INTR_IN_79	PRU_ICSSG1		
		MCU_M4SS0_CORE0_INTR_IN_17	MCU_M4SS0_CORE0		
MCU_I2C1	MCU_I2C1_POINTRPEND_0	GIC500_SPI_IN_140	COMPUTE_CLUSTER0	MCU_I2C1 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_62	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_62	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_62	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_62	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_INTR_IN_80	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_INTR_IN_80	PRU_ICSSG1		

Table 12-33. MCU_I2C[0-1] Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		MCU_M4SS0_CORE0_INTR_IN_18	MCU_M4SS0_CORE0		

Note

I2C interrupts are further described in Section 12.1.3.4.5 , *I2C Interrupt Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.1.3.3.2 I2C Integration in MAIN Domain

There are four I2C modules integrated in the device MAIN domain - I2C0, I2C1, I2C2, and I2C3. Figure 12-26 shows the integration of I2C0, I2C1, I2C2, and I2C3.

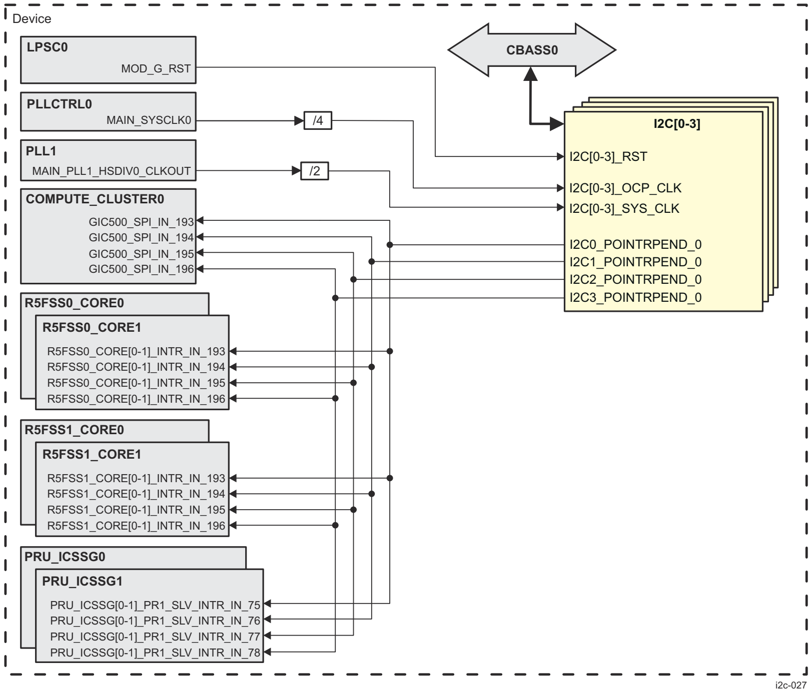

Figure 12-26. I2C[0-3] Integration

Table 12-34 through Table 12-37 summarize the integration of I2C[0-3] in the device MAIN domain.

Table 12-34. I2C[0-3] Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
I2C0	PSC0	PD0	LPSC0	CBASS0
I2C1	PSC0	PD0	LPSC0	CBASS0
I2C2	PSC0	PD0	LPSC0	CBASS0
I2C3	PSC0	PD0	LPSC0	CBASS0

Table 12-35. I2C[0-3] Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
I2C0	I2C0_OCP_CLK	MAIN_SYSCLK0/4	PLLCTRL0	I2C0 interface clock
	I2C0_SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2	PLL1	I2C0 functional clock
I2C1	I2C1_OCP_CLK	MAIN_SYSCLK0/4	PLLCTRL0	I2C1 interface clock
	I2C1_SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2	PLL1	I2C1 functional clock
I2C2	I2C2_OCP_CLK	MAIN_SYSCLK0/4	PLLCTRL0	I2C2 interface clock
	I2C2_SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2	PLL1	I2C2 functional clock
I2C3	I2C3_OCP_CLK	MAIN_SYSCLK0/4	PLLCTRL0	I2C3 interface clock
	I2C3_SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2	PLL1	I2C3 functional clock

Table 12-36. I2C[0-3] Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
I2C0	I2C0_RST	MOD_G_RST	LPSC0	I2C0 reset
I2C1	I2C1_RST	MOD_G_RST	LPSC0	I2C1 reset
I2C2	I2C2_RST	MOD_G_RST	LPSC0	I2C2 reset
I2C3	I2C3_RST	MOD_G_RST	LPSC0	I2C3 reset

Table 12-37. I2C[0-3] Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
I2C0	I2C0_POINTRPEND_0	GIC500_SPI_IN_193	COMPUTE_CLUSTER0	I2C0 Interrupt request	Level
		R5FSS0_CORE0_INTR_IN_193	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_193	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_193	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_193	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_INTR_IN_75	PRU-ICSSG0		
		PRU_ICSSG1_PR1_SLV_INTR_IN_75	PRU-ICSSG1		
I2C1	I2C1_POINTRPEND_0	GIC500_SPI_IN_194	COMPUTE_CLUSTER0	I2C1 Interrupt request	Level
		R5FSS0_CORE0_INTR_IN_194	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_194	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_194	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_194	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_INTR_IN_76	PRU-ICSSG0		
		PRU_ICSSG1_PR1_SLV_INTR_IN_76	PRU-ICSSG1		
I2C2	I2C2_POINTRPEND_0	GIC500_SPI_IN_195	COMPUTE_CLUSTER0	I2C2 Interrupt request	Level

Table 12-37. I2C[0-3] Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
I2C3	I2C3_POINTRPEND_0	R5FSS0_CORE0_INTR_IN_195	R5FSS0_CORE0	I2C3 Interrupt request	Level
		R5FSS0_CORE1_INTR_IN_195	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_195	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_195	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_INTR_IN_77	PRU-ICSSG0		
		PRU_ICSSG1_PR1_SLV_INTR_IN_77	PRU-ICSSG1		
		GIC500_SPI_IN_196	COMPUTE_CLUSTER0		
		R5FSS0_CORE0_INTR_IN_196	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_196	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_196	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_196	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_INTR_IN_78	PRU-ICSSG0		
		PRU_ICSSG1_PR1_SLV_INTR_IN_78	PRU-ICSSG1		

Note

I2C interrupts are further described in Section 12.1.3.4.5 , *I2C Interrupt Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.1.3.4 I2C Functional Description

12.1.3.4.1 I2C Block Diagram

Note

DMA mode and SCCB Protocol are not supported on this family of devices.

Figure 12-27 presents the multicontroller I2C block diagram.

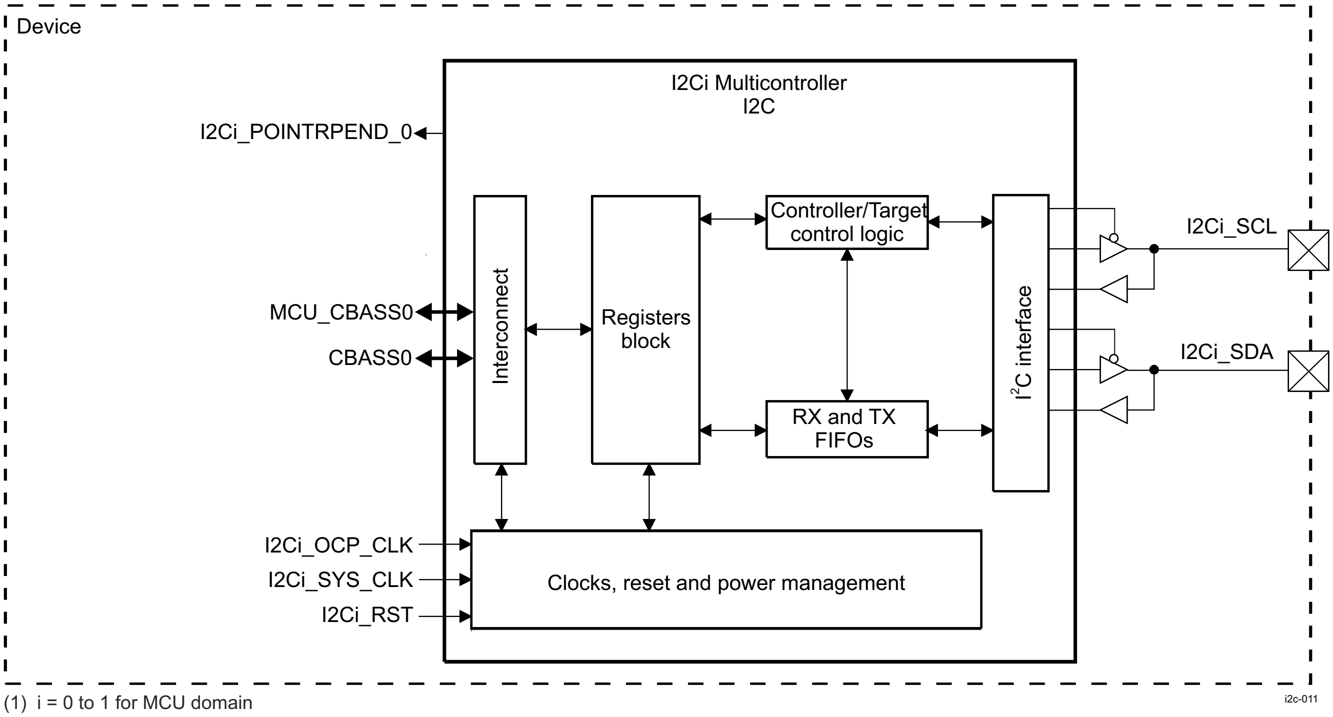

(1) i = 0 to 1 for MCU domain

(2) i = 0 to 3 for MAIN domain

Figure 12-27. I2C Block Diagram

The ten multicontroller I2C can be configured in F/S I^{2}C mode or HS I^{2}C mode. The operation mode is selected by configuring the I2C_CON[13-12] OPMODE bit field.

Table 12-38 lists the available operation modes.

Table 12-38. I^{2}C Operation Mode Selection

Operation Mode	Value of I2C_CON[13-12] OPMODE
F/S I^{2}C	0x0
HS I^{2}C	0x1
SCCB	0x2
Reserved (not used)	0x3

12.1.3.4.2 I2C Clocks

12.1.3.4.2.1 I2C Clocking

Figure 12-28 shows the I^{2}C clock generation of the I2C controllers.

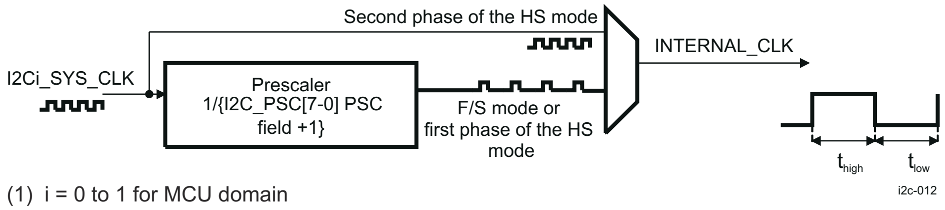

(1) i = 0 to 1 for MCU domain
(2) i = 0 to 3 for MAIN domain

Figure 12-28. I2C Clock Generation

Each multicontroller I2C uses the SYS_CLK functional clock in the Device Configuration section. The internal sampling clock INTERNAL_CLK is generated by dividing the functional clock by the I2C_PSC[7-0] PSC bit field value + 1 in F/S mode, or in the first phase of HS mode; or by directly using the functional clock in the second phase of HS mode (prescaler is bypassed).

The low time of the SCLL signal is determined by the I2C_SCLL[7-0] SCLL bit field in F/S mode and in the first phase of HS mode; or by the I2C_SCLL[15-8] HSSCLL bit field in the second phase of HS mode.

The high time of the SCLH signal is determined by the I2C_SCLH[7-0] SCLH bit field in F/S mode and in the first phase of HS mode; or by the I2C_SCLH[15-8] HSSCLH bit field in the second phase of HS mode.

Table 12-39 lists the t_{LOW} and t_{high} values in controller mode only (in target mode, the I2C controller does not generate the I^2C clock).

Table 12-39. I^2C t_{LOW} and t_{high} Values of the I^2C Clock

Mode	Clock	t_{LOW}	t_{high}
F/S or HS first phase	INTERNAL_CLK = SYS_CLK / (I2C_PSC[7-0] PSC bit field + 1)	(I2C_SCLL[7-0] SCLL bit field value + 7) × INTERNAL_CLK period	(I2C_SCLH [7-0] SCLH bit field value + 5) × I2Ci_INTERNAL_CLK period
HS second phase	SYS_CLK	(I2C_SCLL[15-8] HSSCLL bit field value + 7) × SYS_CLK period	(I2CSCLL [15-8] HSSCLH bit field value + 5) × I2Ci_SYS_CLK period

---

Note

For HS mode, the I2C_SCLL[15-8] HSSCLL and I2C_SCLL[7-0] SCLL bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

For HS mode, the I2C_SCLH[15-8] HSSCLH and I2C_SCLH[7-0] SCLH bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

Note

The equations in Table 12-39 give the SCLL timing values for SCLL/SCLH/HSSCLL/HSSCLH at I2C controller outputs. Actual t_{low} and thigh periods may vary depending on the board (the load capacitance on the SCLL signal). If necessary, any adjustments to the SCLL/SCLH/HSSCLL/HSSCLH values must be determined by measurements of actual SCL signal on the board.

CAUTION

During active mode (the I2C_CON[15] I2C_EN bit is set to 1), make no changes to the I2C_SCLL and I2C_SCLH registers. Changes may result in unpredictable behavior.

Table 12-40 lists the register values for obtaining the maximum I^{2}C bit rates and the maximum period of the filtered spikes in F/S mode and HS mode.

Table 12-40. I2C Register Values for Maximum I2C Bit Rates in I2C F/S, I2C HS Modes(1)

	I^{2}C Mode for			**Description**
	Standard Mode	**Fast Mode**	**High-Speed Mode(2)**	
SYS_CLK frequency (MHz)	96			
OCP_CLK frequency (MHz)	133			
I2C_PSC**[7-0] PSC**	**23**	**9**	**1**	Prescaler value for F/S and HS modes
INTERNAL_CLK frequency (MHz)	4	9.6	96	
I2C_SCLL**[7-0] SCLL**	**13**	**7**	**115**	Value for F/S mode and first phase of HS mode
I2C_SCLH**[7-0] SCLH**	**15**	**5**	**113**	Value for F/S mode and first phase of HS mode
Maximum bit rate (Mbps)	0.1	0.4	0.4	F/S mode and first phase in HS mode maximum bit rate
Maximum filter period (ns)	250	104.2	10	
I2C_SCLL**[15-8] HSSCLL**			**12**	Values for second phase of HS mode
I2C_SCLH**[15-8] HSSCLH**			**5**	Values for second phase of HS mode
HS mode maximum bit rate (Mbps)			3.31	HS mode maximum bit rate
Maximum filter period (ns)			10	

(1) Programmable fields are in bold.

(2) HS mode is not supported on this family of devices.

Note

This table presents informative values only for the configuration parameters and the I^{2}C bus performance obtained according to these values. The delays added by the analog pads are not considered in these figures.

Note

For MCU_I2C[0-1]

For I2C[0-3]

I2Ci_INTERNAL_CLK freq = I2Ci_SYS_CLK / (PSC +1)

F/S filter period = 1 / I2Ci_INTERNAL_CLK

HS filter period = 1 / I2Ci_SYS_CLK freq

HS bit rate = I2Ci_SYS_CLK freq / (HSSCLL+ 7 + HSSCLH + 5)

FS bit rate = I2Ci_INTERNAL_CLK / (SCLL+ 7 + SCLH + 5)

12.1.3.4.2.2 I2C Automatic Blocking of the I2C Clock Feature

This feature offers the possibility for the LH to command the blocking of the I^{2}C clock after the target addressing phase, when the I2C controller is addressed by an external controller device using a certain Own Address.

The release of the I^2C clock can be performed independently for each Own Address (I2C_OA, and I2C_OAx registers, where x = 1, 2, 3) by deasserting the corresponding bit in the I2C_SBLOCK register.

12.1.3.4.3 I2C Software Reset

Each multicontroller I2C supports the software reset by accessing the I2C_SYSC[1] SRST bit (1: reset; 0: normal mode).

The software reset status can be checked by accessing the I2C_SYSS[0] RDONE bit (1: reset is done; 0: reset is ongoing).

To do a software reset, the following steps must be done:
1. Ensure that the module is disabled (clear the I2C_CON[15] I2C_EN bit to 0).
2. Set the I2C_SYSC[1] SRST bit to 1.
3. Enable the module by setting I2C_CON[15] I2C_EN bit to 1.
4. Check the I2C_SYSS[0] RDONE bit until it is set to 1 to indicate the software reset is complete.

Note

The I2C_CON[15] I2C_EN bit can hold the functional clock domain of the multicontroller I2C in reset after the device reset has been released. When the system bus reset is removed, this bit remains cleared. The functional part of the I2C controller is held in reset state while this bit is 0, and all configuration registers can be accessed.

The I2C_CON[15] I2C_EN bit must be set to 1 to enable the functional part of the I2C controller.

The I2C_SYSS[0] RDONE bit is asserted only after the module is enabled by setting the I2C_CON[15] I2C_EN bit to 1.

12.1.3.4.4 I2C Power Management

Table 12-41 describes power-management features available for the multicontroller I2C.

Note

For information about source clock gating, see Section 5.2 , *Power*, in the Chapter 5 , *Device Configuration*.

Note

Some of the I2C features described in this section may not be supported on this family of devices. For more information, see Section 12.1.3.1.2 , *I2C Not Supported Features*.

Table 12-41. I2C Local Power-Management Features

Feature	Registers	Description
Clock auto gating	I2C_SYSC[0] AUTOIDLE	This bit allows a local power optimization inside the module.
Target idle modes	I2C_SYSC[4-3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Clock activity	I2C_SYSC[9-8] CLOCKACTIVITY	For configuration details, see Table 12-42.
Global wake-up enable	I2C_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.

Table 12-42. I2C Clock Activity Settings

I2C_SYSC[9-8] CLOCKACTIVITY	Clock State When Module is in IDLE State		Features Available/Unavailable When Module is in IDLE State
	OCP_CLK	SYS_CLK	
00	OFF	OFF	Both clocks are disabled.
10	OFF	ON	Interface clock is disabled; Functional clock is enabled

Table 12-42. I2C Clock Activity Settings (continued)

I2C_SYSC[9-8] CLOCKACTIVITY	Clock State When Module is in IDLE State		Features Available/Unavailable When Module is in IDLE State
	OCP_CLK	SYS_CLK	
01	ON	OFF	Functional clock is disabled; Interface clock is enabled
11	ON	ON	Both clocks are enabled.

12.1.3.4.5 I2C Interrupt Requests

The I2C controller must allocate a minimum of five registers for interrupts.

- Interrupt Raw Status (I2C_IRQSTATUS_RAW)
- Interrupt Enabled Status (I2C_IRQSTATUS)
- Interrupt Enable Set (I2C_IRQENABLE_SET)
- Interrupt enable Clear (I2C_IRQENABLE_CLR)
- End of interrupt (I2C_EOI)

End of Interrupt (I2C_EOI) is used by software to trigger an interrupt service completion.

Table 12-43 lists the event flags, and their mask, that can cause module interrupts.

Table 12-43. I2C Events

Event Flag	Event Unmask	Event Mask	Description
I2C_IRQSTATUS[0] AL	I2C_IRQENABLE_SET[0] AL_IE	I2C_IRQENABLE_CLR[0] AL_IE	Arbitration lost. This bit is automatically set by the hardware when it loses the arbitration in controller transmit mode, an interrupt is signaled to the host.
I2C_IRQSTATUS[1] NACK	I2C_IRQENABLE_SET[1] NACK_IE	I2C_IRQENABLE_CLR[1] NACK_IE	No acknowledgement. Bit is set when No Acknowledge is received, an interrupt is signaled to the host.
I2C_IRQSTATUS[2] ARDY	I2C_IRQENABLE_SET[2] ARDY_IE	I2C_IRQENABLE_CLR[2] ARDY_IE	Register access ready. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to the host.
I2C_IRQSTATUS[3] RRDY	I2C_IRQENABLE_SET[3] RRDY_IE	I2C_IRQENABLE_CLR[3] RRDY_IE	Receive data ready. Set to 1 by core when in receiver mode, a new data can be read. An interrupt is signaled to the host.
I2C_IRQSTATUS[4] XRDY	I2C_IRQENABLE_SET[4] XRDY_IE	I2C_IRQENABLE_CLR[4] XRDY_IE	Transmit data ready. Set to 1 by core when transmitter is ready for new data. An interrupt is signaled to the host.
I2C_IRQSTATUS[5] GC	I2C_IRQENABLE_SET[5] GC_IE	I2C_IRQENABLE_CLR[5] GC_IE	General call. Set to 1 by core when General Call address was detected. An interrupt is signaled to the host.
I2C_IRQSTATUS[6] STC	I2C_IRQENABLE_SET[6] STC_IE	I2C_IRQENABLE_CLR[6] STC_IE	Start condition detected. An interrupt is signaled to the host.
I2C_IRQSTATUS[7] AERR	I2C_IRQENABLE_SET[7] AERR_IE	I2C_IRQENABLE_CLR[7] AERR_IE	Bus Access Error. An interrupt is signaled to the host.
I2C_IRQSTATUS[8] BF	I2C_IRQENABLE_SET[8] BF_IE	I2C_IRQENABLE_CLR[8] BF_IE	Bus free. An interrupt is signaled to the host.
I2C_IRQSTATUS[9] AAS	I2C_IRQENABLE_SET[9] AAS_IE	I2C_IRQENABLE_CLR[9] AAS_IE	Address recognized as target. An interrupt is signaled to the host.
I2C_IRQSTATUS[10] XUDF	I2C_IRQENABLE_SET [10] XUDF_IE	I2C_IRQENABLE_CLR[10] XUDF_IE	Transmit underflow. An interrupt is signaled to the host.
I2C_IRQSTATUS[11] ROVR	I2C_IRQENABLE_SET [11] ROVR_IE	I2C_IRQENABLE_CLR[11] ROVR_IE	Receive overrun. An interrupt is signaled to the host.
I2C_IRQSTATUS[12] BB	N/A	N/A	Bus busy indicator

Table 12-43. I2C Events (continued)

Event Flag	Event Unmask	Event Mask	Description
I2C_IRQSTATUS[13] RDR	I2C_IRQENABLE_SET [13] RDR_IE	I2C_IRQENABLE_CLR[13] RDR_IE	Receive draining. An interrupt is signaled to the host.
I2C_IRQSTATUS[14] XDR	I2C_IRQENABLE_SET [14] XDR_IE	I2C_IRQENABLE_CLR[14] XDR_IE	Transmit draining. An interrupt is signaled to the host.

12.1.3.4.6 I2C Programmable Multitarget Channel Feature

This feature allows each multicontroller I2C to be addressed using four separate Own Addresses configured in the I2C_OA and I2C_OAx registers (where x = 1, 2, 3). An additional register (I2C_ACTOA) is used to indicate to the LH which address is used by the external controller to communicate with the I2C controller.

Each Own Address can be independently configured in 7-bit or 10-bit mode by setting the corresponding bit (I2C_CON[7] XOA0, I2C_CON[6] XOA1, I2C_CON[5] XOA2, or I2C_CON[4] XOA3).

12.1.3.4.7 I2C FIFO Management

Each multicontroller I2C implements two internal 8-bit FIFOs, the RX and TX FIFOs.

The depth of the RX and TX FIFOs can be checked by reading the I2C_BUFSTAT[15-14] FIFODEPTH bit field (0x0: 8 bytes, 0x1: 16 bytes, 0x2: 32 bytes, and 0x3: 64 bytes).

12.1.3.4.7.1 I2C FIFO Interrupt Mode

In FIFO interrupt mode (relevant interrupts enabled by the I2C_IRQENABLE_SET register), an interrupt signal informs the processor of the receiver and transmitter status. These interrupts are raised when the RX/TX FIFO thresholds (defined by the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX FIFO or the I2C_BUF[5-0] TXTRSH bit field value + 1 for the TX FIFO) are reached; the interrupt signals instruct the LH to transfer data to the destination (from the I2C controller in receive mode and/or from any source to the I2C controller FIFO in transmit mode).

Figure 12-29 and Figure 12-30 show receive and transmit operations, respectively, from a FIFO management point of view.

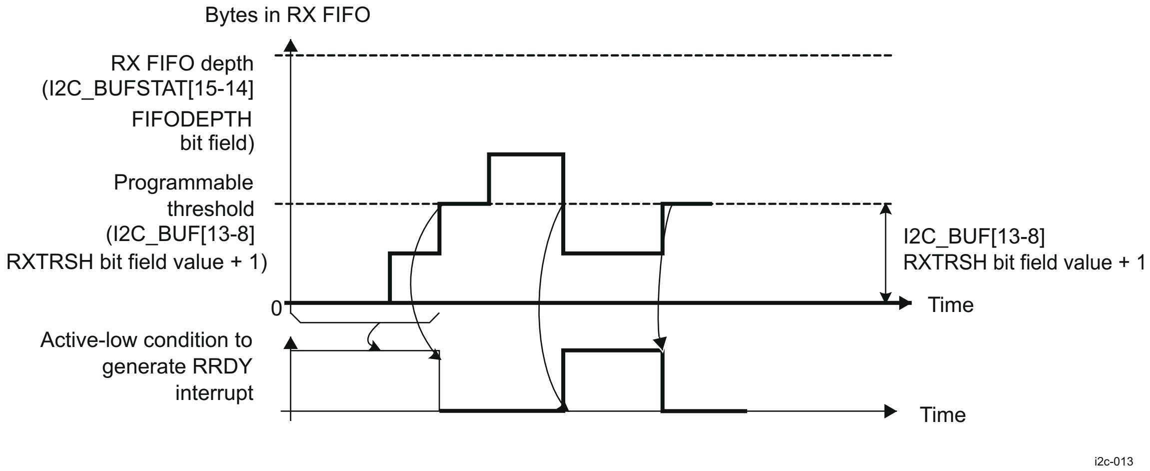

Figure 12-29. I2C Receive FIFO Interrupt Request Generation

In Figure 12-29 , the RRDY interrupt condition shows that the condition for generating an RRDY interrupt is achieved. The interrupt request is generated when this signal is active, and it can be cleared only by the LH by writing 1 in the corresponding bit. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In receive mode, an RRDY interrupt is generated as soon as the FIFO reaches its receive threshold (I2C_BUF[13-8] RXTRSH bit field value + 1). The interrupt can be deasserted only when the LH has handled enough bytes to make the number of bytes in the RX FIFO lower than the programmed threshold. For each interrupt, the LH can be configured to read a number of bytes equal to the value of the RX FIFO threshold.

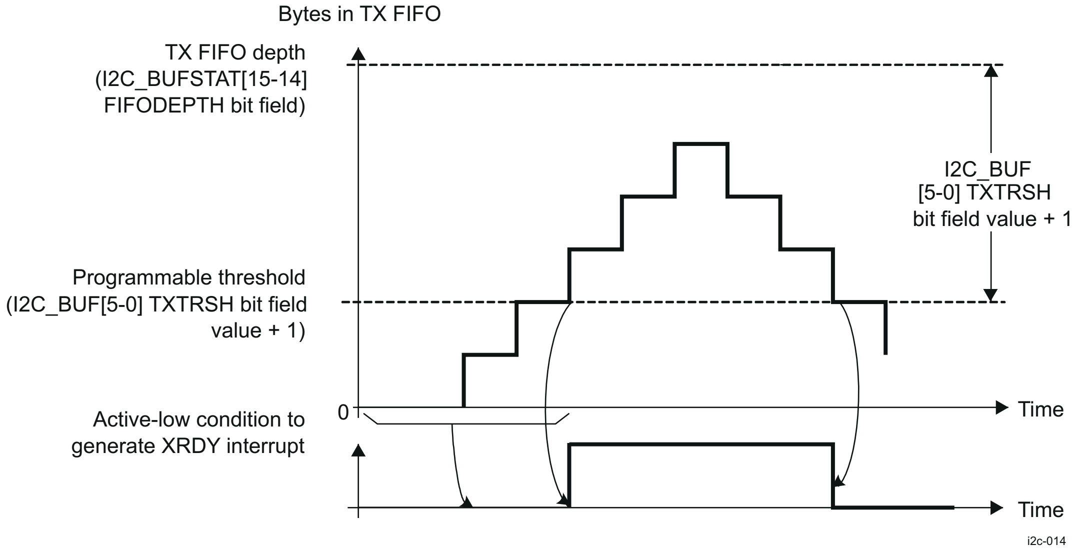

Figure 12-30. I2C Transmit FIFO Interrupt Request Generation

In Figure 12-30 , the XRDY interrupt condition shows that the condition for generating an XRDY interrupt is achieved. The interrupt request is generated when TX FIFO is empty or when the TX FIFO threshold is not reached, and the LH can clear the XRDY status bit by setting the I2C_IRQENABLE_CLR [4] XRDY_IE bit to 1 after transmitting the configured number of bytes. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In interrupt mode, the module offers two options for the LH application to handle the interrupts:

- When detecting an interrupt request (XRDY or RRDY type), the LH can write/read 1 data byte to/from the TX/RX FIFO and then clear the interrupt. The module reasserts the interrupt until the interrupt condition is not met.
- When detecting an interrupt request (XRDY or RRDY type), the LH can be programmed to write/read the amount of data bytes specified by the corresponding FIFO threshold (I2C_BUF[5-0] TXTRSH + 1 or I2C_BUF[5-0] RXTRSH + 1). In this case, the interrupt condition is cleared and the next interrupt is asserted again when the XRDY or RRDY condition is met again.

If the second-interrupt-serving approach is used, an additional mechanism (draining feature) is implemented for cases where the transfer length is not a multiple of the FIFO threshold value (see Section 12.1.3.4.7.3 , *Draining Feature [I2C Mode Only]*).

Note

In target transmit mode (the I2C_CON[10] MST bit is cleared and the I2C_CON[9] TRX bit is set to 1), the draining feature must not be used, because the transfer length is not known at configuration time, and the external controller can end the transfer at any point by not acknowledging 1 data byte. If the draining feature is used in target transmit mode, data can remain in the TX FIFO without being transmitted over the I^2C bus. In this case, the TX FIFO must be cleared by setting the I2C_BUF[6] TXFIFO_CLR bit.

12.1.3.4.7.2 I2C FIFO Polling Mode

In FIFO polling mode (the I2C_IRQENABLE_SET[4] XRDY_IE and I2C_IRQENABLE_SET[3] RRDY_IE bits are disabled), the status of the module (receiver or transmitter) can be checked by polling the I2C_IRQSTATUS_RAW[4] XRDY and the I2C_IRQSTATUS_RAW[3] RRDY bits (the I2C_IRQSTATUS_RAW[13]

RDR and I2C_IRQSTATUS_RAW[14] XDR bits can also be polled if the draining feature is enabled). The I2C_IRQSTATUS_RAW[4] XRDY and I2C_IRQSTATUS_RAW[3] RRDY bits accurately reflect the interrupt conditions described in the discussion of FIFO interrupt mode.

12.1.3.4.7.3 I2C Draining Feature

Note

DMA mode and SCCB Protocol are not supported on this family of devices.

The draining feature is implemented to handle the end of a transfer whose length is not a multiple of the FIFO threshold values (the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX threshold and the I2C_BUF[5-0] TXTRSH field value + 1 for the TX threshold). It can also transfer the remaining number of bytes (because the threshold is not reached).

This feature prevents the LH or the DMA controller from trying more FIFO accesses than necessary (for example, to generate at the end of a transfer a DMA RX request having fewer bytes in the FIFO than the configured DMA transfer length). Otherwise, an AERR interrupt is generated by the I2C_IRQSTATUS_RAW[7] AERR bit.

The draining mechanism generates an interrupt using the I2C_IRQSTATUS_RAW[13] RDR or I2C_IRQSTATUS_RAW[14] XDR bit at the end of the transfer, informing the LH that it must check the amount of data left to be transferred (the I2C_BUFSTAT[13-8] RXSTAT or I2C_BUFSTAT[5-0] TXSTAT bit fields) and enable the draining feature of the DMA controller by reconfiguring the DMA transfer length according to this value (when the DMA mode is enabled) or perform only the required number of data accesses (when the DMA mode is disabled).

In receive mode (controller or target), if the RX FIFO threshold (the I2C_BUF[13-8] RXTRSH bit field value + 1) is not reached, but the transfer ends on the I^{2}C bus and data remains in the RX FIFO (less than the threshold), the receive draining interrupt (the I2C_IRQSTATUS_RAW[13] RDR bit) is asserted to inform the LH that it can read the amount of data in the RX FIFO (the I2C_BUFSTAT[13-8] RXSTAT bit field). The LH performs a number of data read accesses equal to the I2C_BUFSTAT[13-8] RXSTAT bit field (interrupt or polling mode), or reconfigures the DMA controller with the required value to drain the FIFO.

In controller transmit mode, if the TX FIFO threshold (the I2C_BUF[5-0] TXTRSH bit field value + 1) is not reached, but the amount of data remaining to be written in the TX FIFO is less than the threshold, the transmit draining interrupt (the I2C_IRQSTATUS_RAW[14] XDR bit) is asserted to inform the LH that it can read the amount of data remaining to be written in the TX FIFO (the I2C_BUFSTAT[5-0] TXSTAT bit field). The LH must write the required number of data bytes specified by the I2C_BUFSTAT[5-0] TXSTAT bit field value or reconfigure the DMA controller with the value required to transfer the last bytes to the FIFO.

In controller mode, the LH can alternately not check the values of the I2C_BUFSTAT[5-0] TXSTAT and I2C_BUFSTAT[13-8] RXSTAT bit fields, because it can obtain this information internally (by computing the I2C_CNT[15-0] DATACOUNT bit field value modulo I2C_BUF[13-8] RXTRSH or I2C_BUF[5-0] TXTRSH).

By default, the draining feature is disabled; it can be enabled using the I2C_IRQENABLE_SET[14] XDR_IE or I2C_IRQENABLE_SET[13] RDR_IE bits (default disabled) only for transfers with lengths not equal to the threshold values (I2C_BUF[5-0] TXTRSH bit field value + 1 for the TX threshold or the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX threshold).

12.1.3.4.8 I2C Noise Filter

The noise filter is used to suppress any noise that is 50 ns or less in case of F/S operation modes, and any noise that is 10 ns or less in case of HS mode operation. The noise filter is always one period of the INTERNAL_CLK clock. This way, for HS mode operation (prescaler bypassed), the filter suppresses spikes of less than 10.4 ns.

For standard mode (for example, the I2C_PSC[7-0] PSC bit field = 4), the maximum width of suppressed spikes is 46.1 ns.

To ensure correct filtering, the prescaler must be programmed accordingly by the I2C*i*.I2C_PSC[7-0] PSC bit field.

12.1.3.4.9 I2C System Test Mode

A system test mode is available for multicontroller I2C module testing. This mode is enabled by setting the I2C_SYSTEST[15] ST_EN bit to 1. When this bit is cleared to 0, the I2C controller is configured in normal operation mode.

In system test mode, the I2C_SYSTEST[13-12] TMODE bit field selects the type of test. Table 12-44 lists the tests available for the multicontroller HS I2C controllers.

Table 12-44. I2C List of Tests

I2C_SYSTEST[13-12] TMODE	Test	Description
00	Functional mode	Normal operation mode
01	Reserved (not used)	
10	Test of SCL serial clock line	The SCL line is driven with a permanent clock as if controlled with the parameters set in the I2C_PSC, I2C_SCLL, and I2C_SCLH registers.
11	Loop-back mode + SCL/SDA I/O	In controller transmit mode only, data transmitted out of the I2C_DATA register (write action) is received in the same I2C_DATA register through an internal path through the FIFO buffers. The interrupt request is normally generated if it is enabled. Moreover, the SCL and SDA are controlled with the I2C_SYSTEST[3-0] bits.

Note

When the I2C_SYSTEST[13-12] TMODE bit field is set to 11, the I2C controller must be configured in I^2C F/S (I2C_CON[13-12] OPMODE set to 00) or I^2C HS mode (I2C_CON[13-12] OPMODE set to 01).

Note

In normal operation mode (the I2C_SYSTEST[15] ST_EN bit cleared to 0), the I2C_SYSTEST[3-0] bits that control the SCL, SDA lines in system test mode are read-only bits.

In system test mode (the I2C_SYSTEST[15] ST_EN bit set to 1), the I2C_IRQSTATUS_RAW[4] XRDY, I2C_IRQSTATUS_RAW[3] RRDY, I2C_IRQSTATUS_RAW[10] XUDF, I2C_IRQSTATUS_RAW[11] ROVR, I2C_IRQSTATUS_RAW[2] ARDY and I2C_IRQSTATUS_RAW[1] NACK status bits can be set to 1 when the I2C_SYSTEST[11] SSB bit is set to 1. Clearing the I2C_SYSTEST[11] SSB bit to 0 does not clear the I2C_IRQSTATUS_RAW bits to 0. The I2C_IRQSTATUS_RAW bit field can be cleared to 0 only by writing 1 in the corresponding bits.

12.1.3.5 I2C Programming Guide

12.1.3.5.1 I2C Low-Level Programming Models

12.1.3.5.1.1 I2C Programming Model

This section describes the programming model of the multicontroller I2C configured in I^{2}C mode.

12.1.3.5.1.1.1 Main Program

12.1.3.5.1.1.1.1 Configure the Module Before Enabling the I2C Controller

Before enabling the I2C controller, perform the following steps:

1. Enable the functional and interface clocks (see , Table 12-31, and Table 12-35).
2. Program the prescaler to obtain an approximately 12-MHz internal sampling clock by programming the corresponding value in the I2C_PSC[7-0] PSC bit field. This value depends on the frequency of the functional clock (SYS_CLK).
3. Program the I2C_SCLL[7-0] SCLL and I2C_SCLH[7-0] SCLH bit fields to obtain a bit rate of 100 kbps or 400 kbps. These values depend on the internal sampling clock frequency (see Table 12-39).
4. (Optional) Program the I2C_SCLL[15-8] HSSCLL and I2C_SCLH[15-8] HSSCLH bit fields to obtain a bit rate of 400 kbps or 3.4 Mbps (for the second phase of HS mode). These values depend on the internal sampling clock frequency (see Table 12-39).
5. Configure the Own Address of the I2C controller by storing it in the I2C_OA register. Up to four Own Addresses can be programmed in the I2C_OA and I2C_OAx registers (where x = 1, 2, 3) for each I2C controller.

Note

For a 10-bit address, set the corresponding expand Own Address bit in the I2C_CON register.

6. Set the TX threshold (in transmitter mode) and the RX threshold (in receiver mode) by setting the I2C_BUF[5-0] TXTRSH bit field to (TX threshold – 1) and the I2C_BUF[13-8] RXTRSH bit field to (RX threshold – 1), where the TX and RX thresholds are greater than or equal to 1.
7. Take the I2C controller out of reset by setting the I2C_CON[15] I2C_EN bit to 1.

12.1.3.5.1.1.1.2 Initialize the I2C Controller

To initialize the I2C controller, perform the following steps:

1. Configure the I2C_CON register:
   - For controller or target mode, set the I2C_CON[10] MST bit (0: target; 1: controller).
   - For transmitter or receiver mode, set the I2C_CON[9] TRX bit (0: receiver; 1: transmitter).
2. If using an interrupt to transmit and receive data, set the corresponding bit in the I2C_IRQENABLE_SET register to 1 (the I2C_IRQENABLE_SET [4] XRDY_IE bit for the transmit interrupt, the I2C_IRQENABLE_SET [3] RRDY bit for the receive interrupt).

12.1.3.5.1.1.1.3 Configure Target Address and the Data Control Register

In controller mode, configure the target address register by programming the I2C_SA[9-0] SA bit field and the number of data bytes (I^{2}C data payload) associated with the transfer by programming the I2C_CNT[15-0] DCOUNT bit field.

Note

For a 10-bit address, set the I2C_CON[8] XSA bit to 1.

12.1.3.5.1.1.1.4 Initiate a Transfer

Poll the I2C_IRQSTATUS_RAW [12] BB bit. If it is cleared to 0 (bus not busy), configure the I2C_CON[0] STT and I2C_CON[1] STP bits. To initiate a transfer, the I2C_CON[0] STT bit must be set to 1, and it is not mandatory to set the I2C_CON[1] STP bit to 1.

12.1.3.5.1.1.1.5 Receive Data

Poll the I2C_IRQSTATUS_RAW [3] RRDY bit, or use the RRDY interrupt (the I2C_IRQENABLE_SET [3] RRDY_IE bit must be set to 1) to read the receive data in the I2C_DATA register.

If the transfer length does not equal the RX FIFO threshold (the I2C_BUF[13-8] RTRSH bit field + 1), use the draining feature (enable the RDR interrupt by setting the I2C_IRQENABLE_SET [13] RDR_IE bit to 1).

Note

In receive mode only, the I2C_IRQSTATUS_RAW [11] ROVR (receive overrun) bit indicates whether the receiver has experienced overrun. An overrun condition occurs when the shift register and the RX FIFO are full. An overrun condition does not result in data loss; the I2C controller simply holds SCL to low to prevent other bytes from being received.

The I2C_IRQSTATUS_RAW[7] AERR bit is set to 1 when a read access is performed in the I2C_DATA register while the RX FIFO is empty. The corresponding interrupt can be enabled by setting the I2C_IRQENABLE_SET [7] AERR_IE bit to 1.

12.1.3.5.1.1.1.6 Transmit Data

Poll the I2C_IRQSTATUS_RAW [4] XRDY bit, or use the XRDY interrupt (the I2C_IRQENABLE_SET [4] XRDY_IE bit must be set to 1) to write data to the I2C_DATA register.

If the transfer length does not equal the TX FIFO threshold (the I2C_BUF[5-0] TXTRSH bit field + 1), use the draining feature (enable the XDR interrupt by setting the I2C_IRQENABLE_SET [14] XDR_IE bit to 1).

Note

In transmit mode only, the I2C_IRQSTATUS_RAW [10] XUDF bit indicates whether the transmitter has experienced underflow.

In controller transmit mode, underflow occurs when the shift register and the TX FIFO are empty and there are still some bytes to transmit (the value of the I2C_CNT[15-0] DCOUNT bit field is not 0).

In target transmit mode, underflow occurs when the shift register and the TX FIFO are empty and the external I^{2}C controller device still requests data bytes to be read.

The I2C_IRQSTATUS_RAW [7] AERR bit is set to 1 when a write access is performed in the I2C_DATA register while the TX FIFO is full. The corresponding interrupt can be enabled by setting the I2C_IRQENABLE_SET [7] AERR_IE bit to 1.

12.1.3.5.1.1.2 Interrupt Subroutine Sequence

1. Test for arbitration lost (the I2C_IRQSTATUS_RAW [0] AL bit) and resolve accordingly.
2. Test for no acknowledgment (the I2C_IRQSTATUS_RAW [1] NACK bit) and resolve accordingly.
3. Test for register access ready (the I2C_IRQSTATUS_RAW [2] ARDY bit) and resolve accordingly.
4. Test for receive data ready (the I2C_IRQSTATUS_RAW [3] RRDY bit) and resolve accordingly.
5. Test for transmit data ready (the I2C_IRQSTATUS_RAW [4] XRDY bit) and resolve accordingly.
6. Test for general call (the I2C_IRQSTATUS_RAW [5] GC bit) and resolve accordingly.
7. Test for start (S) condition (the I2C_IRQSTATUS_RAW [6] STC bit) and resolve accordingly. For this test, the functional clock must be inactive.
8. Test for access error (the I2C_IRQSTATUS_RAW [7] AERR bit) and resolve accordingly.
9. Test for bus free (the I2C_IRQSTATUS_RAW [8] BF bit) and resolve accordingly.

12.1.3.5.1.1.3 Programming Flow-Diagrams

Figure 12-31 through Figure 12-37 are procedure flow charts for programming the F/S and HS I^{2}C modes.

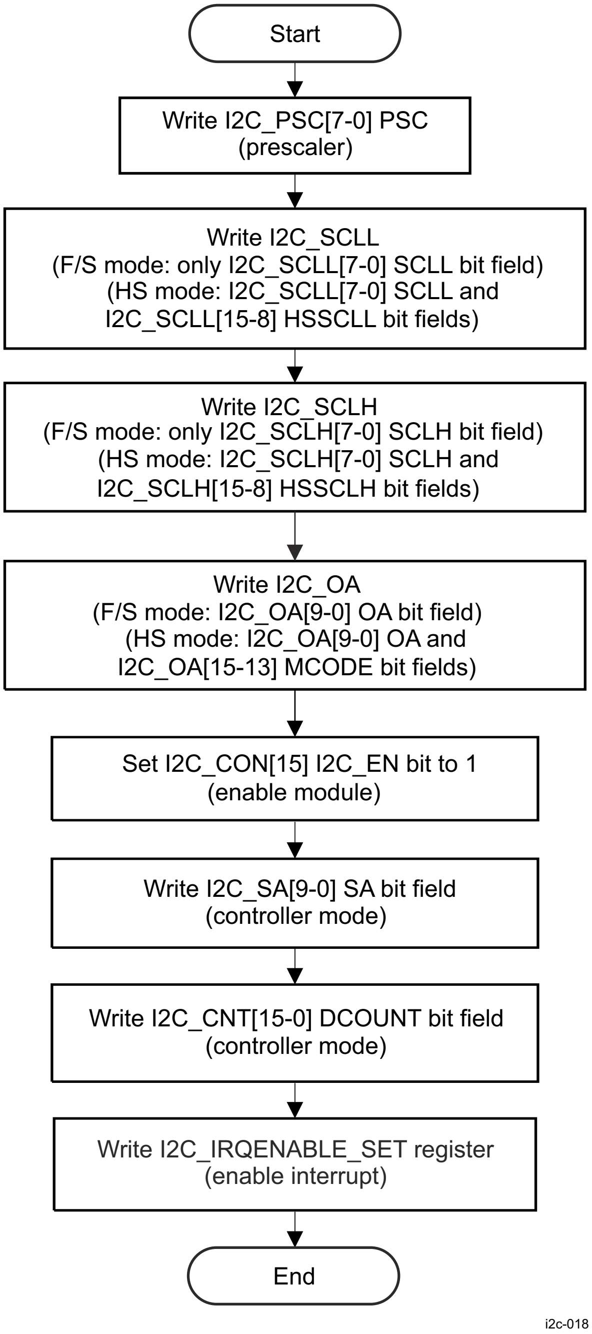

Figure 12-31. I2C Setup Procedure

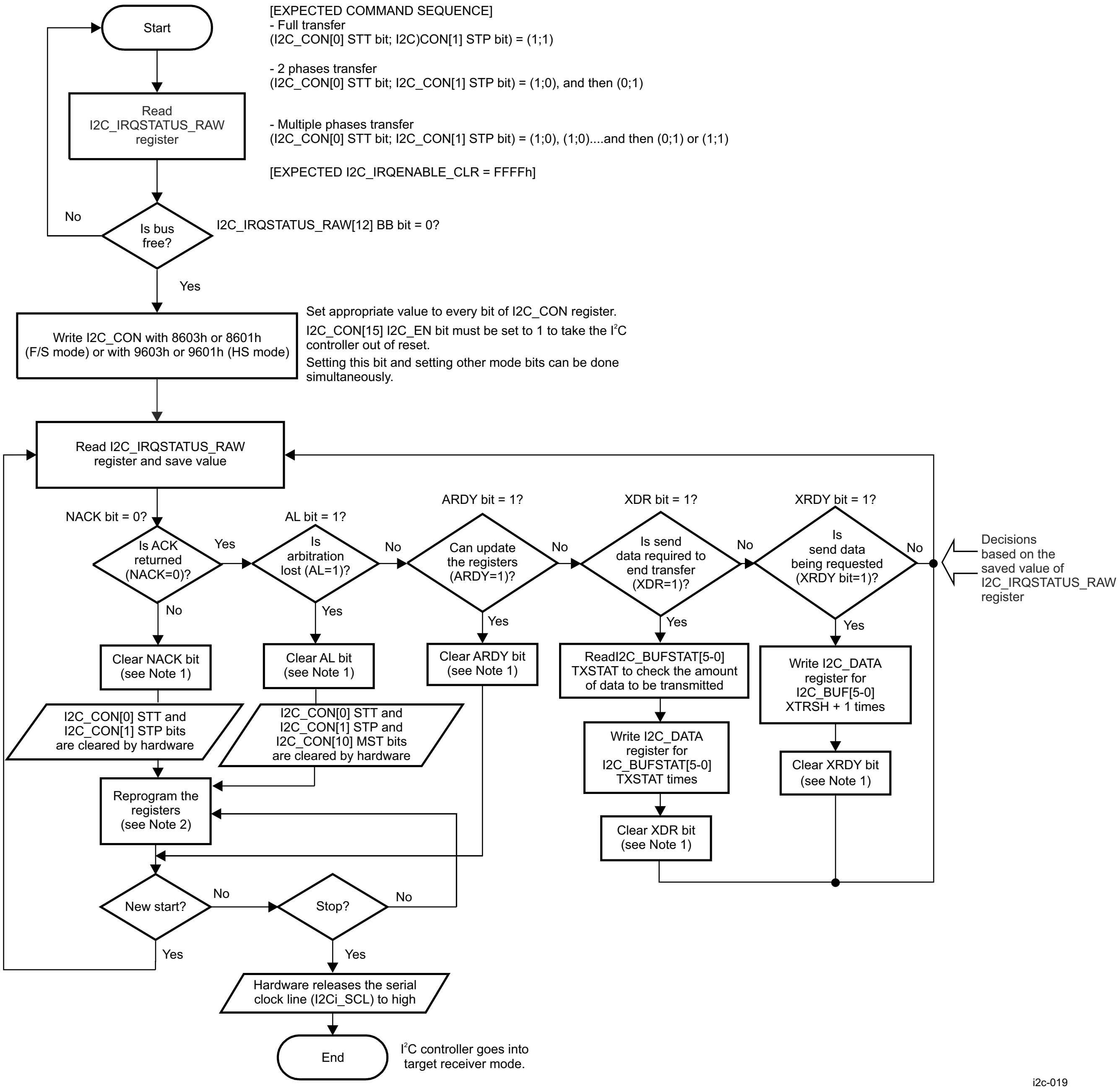

Note

The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

Reprogram the registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-32. I2C Controller Transmitter Mode, Polling Method, in F/S and HS Modes

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Note

The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

Note

In HS mode, the Sr condition and clock frequency switching are automatically generated by the multicontroller I2C.

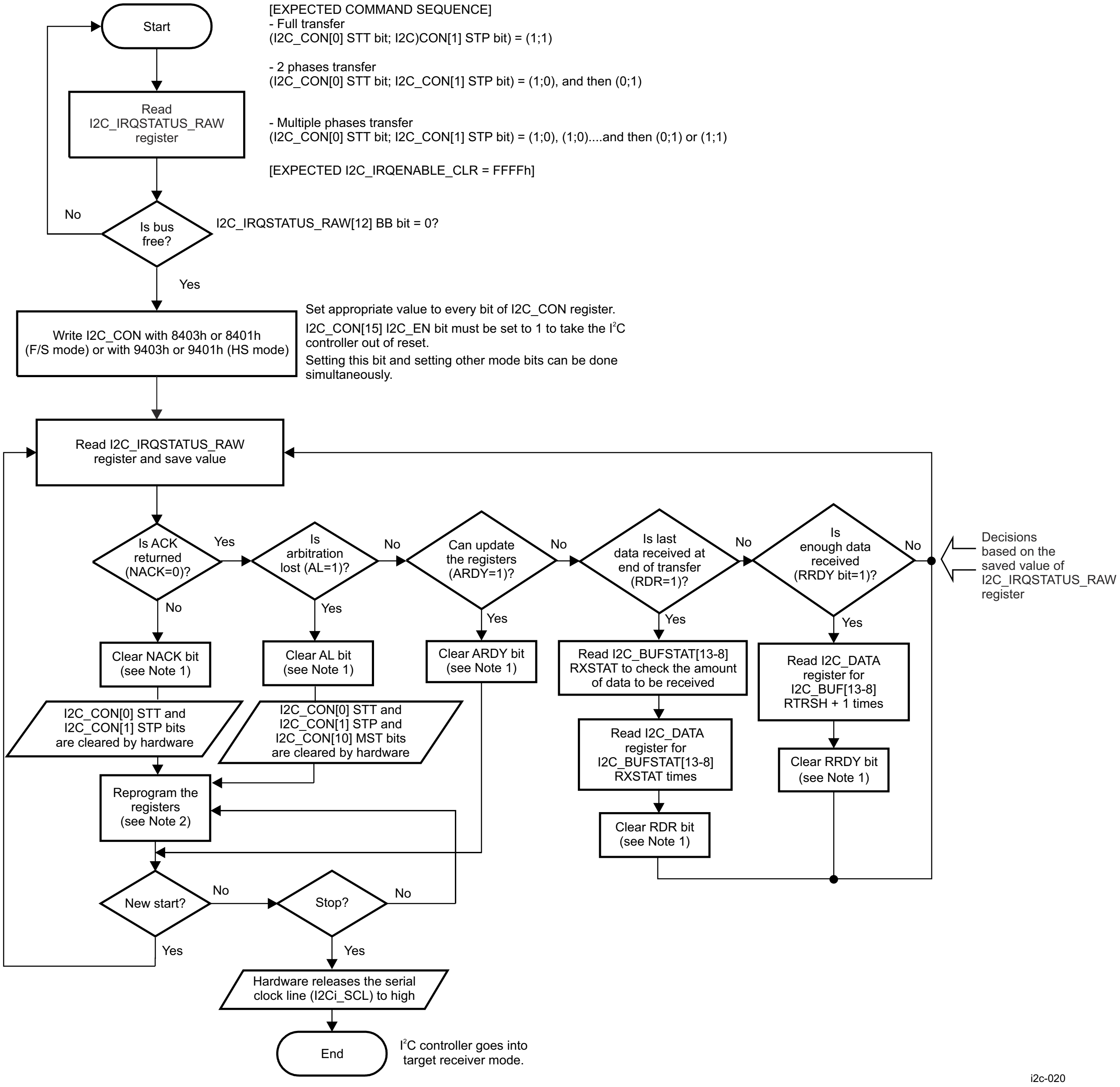

Note

The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-33. I2C Controller Receiver Mode, Polling Method, in F/S and HS Modes

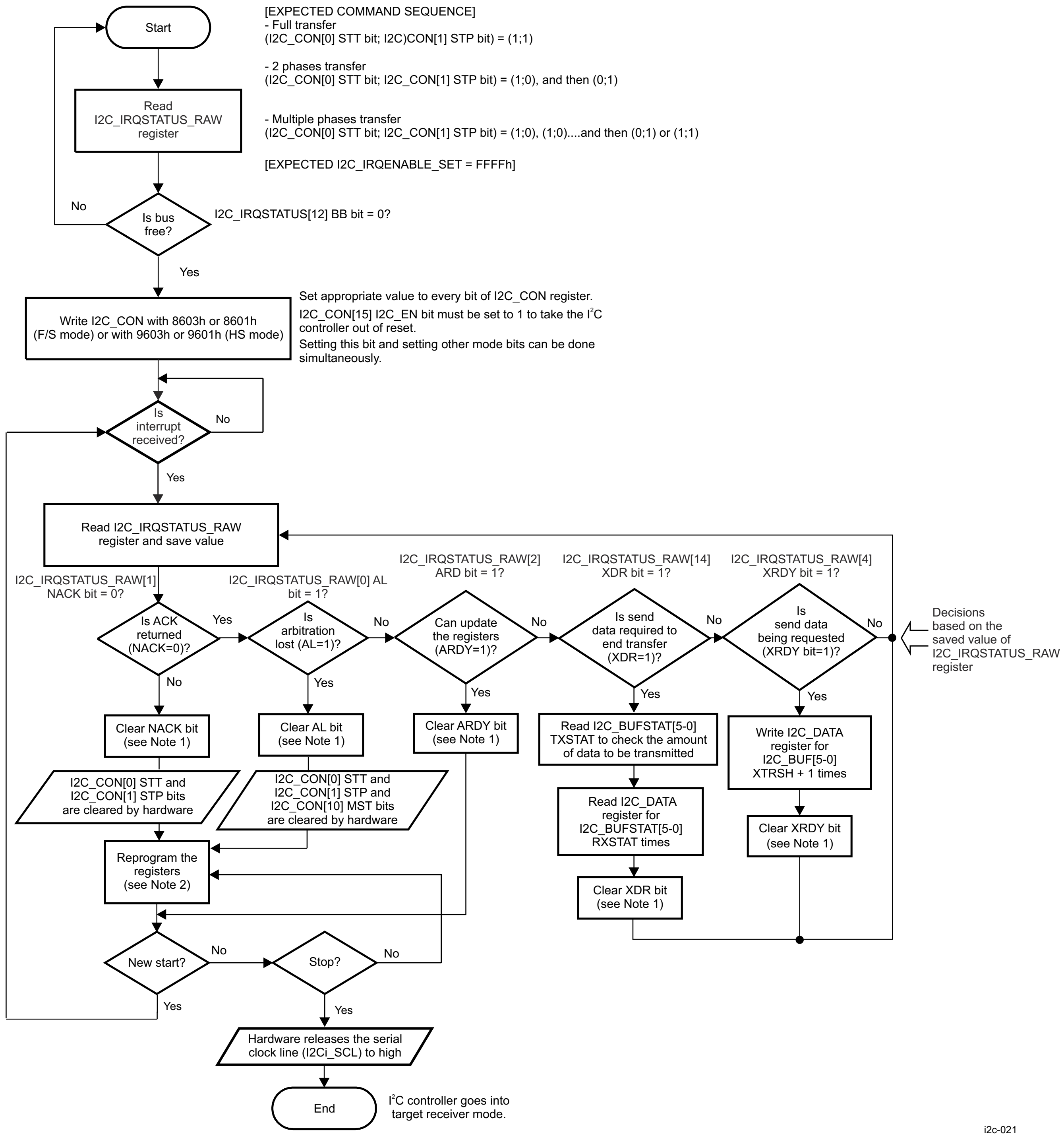

Note

The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-34. I2C Controller Transmitter Mode, Interrupt Method, in F/S and HS Modes

Note

The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

Note

In HS mode, the Sr condition and clock frequency switching are automatically generated by the multicontroller I2C.

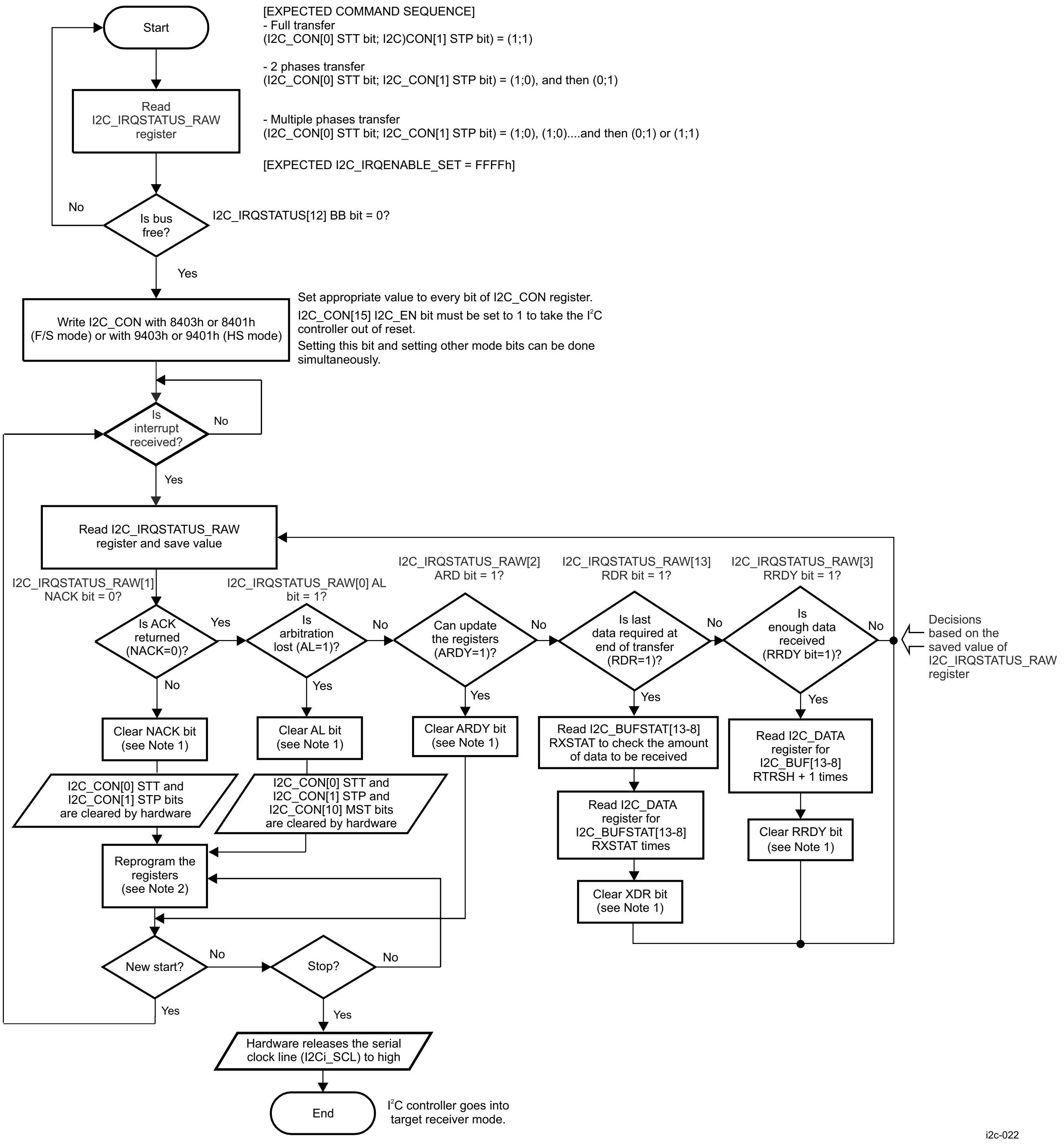

Note

The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-35. I2C Controller Receiver Mode, Interrupt Method, in F/S and HS Modes

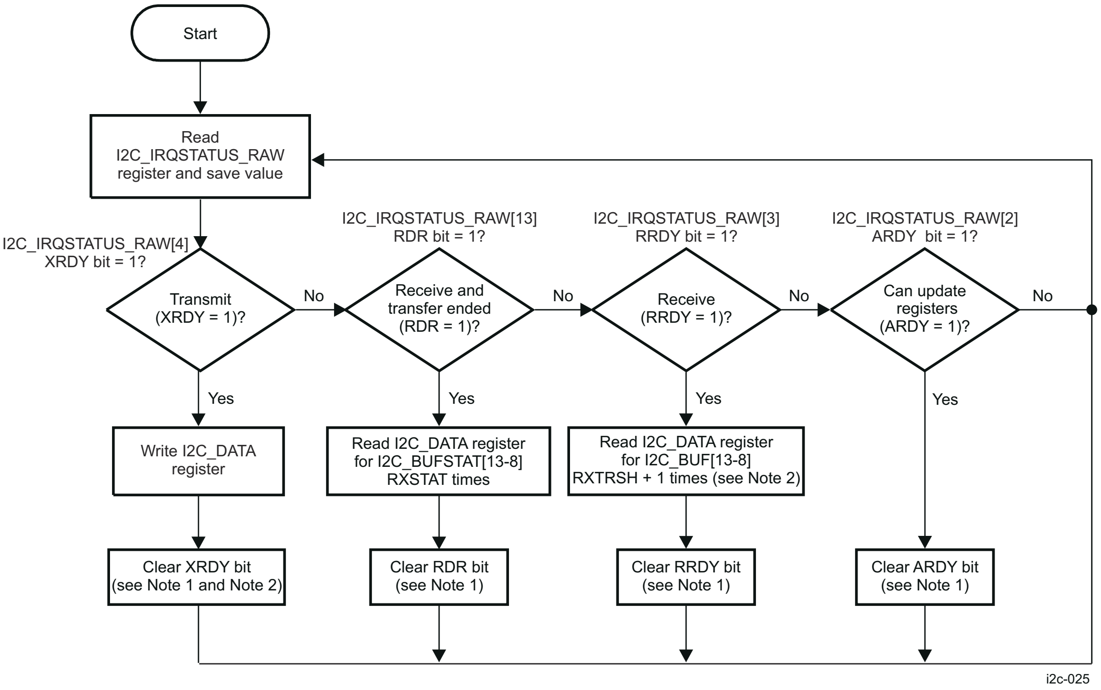

Note

The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

In target transmitter mode, the amount of data requested by the external controller I^{2}C device is unknown; thus, the I2C_BUF[5-0] XTRSH bit field must be configured to 0x0 (TX threshold = 1).

Figure 12-36. I2C Target Transmitter/Receiver Mode, Polling

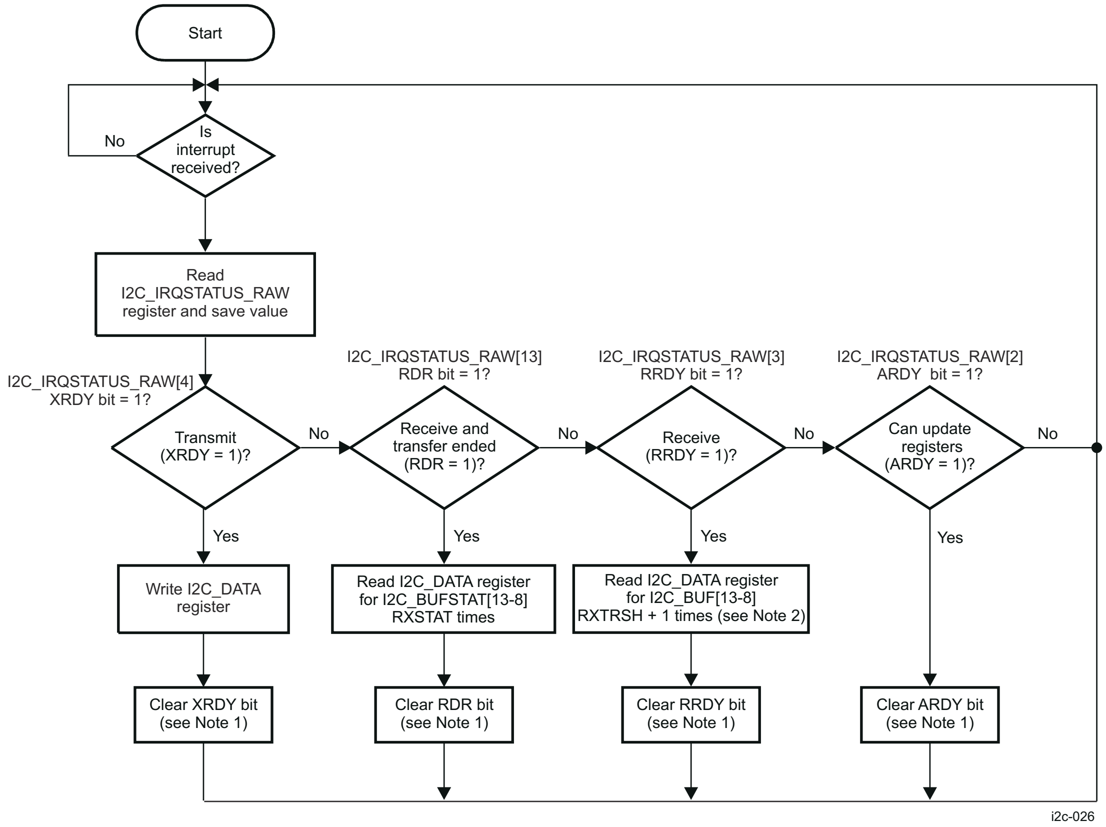

Note

The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

Note

In target transmitter mode, the amount of data requested by the external controller I^{2}C device is unknown; thus, the I2C_BUF[5-0] XTRSH bit field must be configured to 0x0 (TX threshold = 1).

Figure 12-37. I2C Target Transmitter/Receiver Mode, Interrupt

12.1.4 Multichannel Serial Peripheral Interface (MCSPI)

This section describes the Multichannel Serial Peripheral Interface (MCSPI) modules for the device.

12.1.4.1 MCSPI Overview

The MCSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

Table 12-45 shows the MCSPI allocation across device domains.

Table 12-45. MCSPI Allocation Across Device Domains

Instance	Domain	
	MCU	**MAIN**
MCU_MCSPI0	✓	-
MCU_MCSPI1	✓	-
MCSPI0	-	✓
MCSPI1	-	✓
MCSPI2	-	✓
MCSPI3	-	✓
MCSPI4	-	✓

Figure 12-38 shows the MCSPI overview.

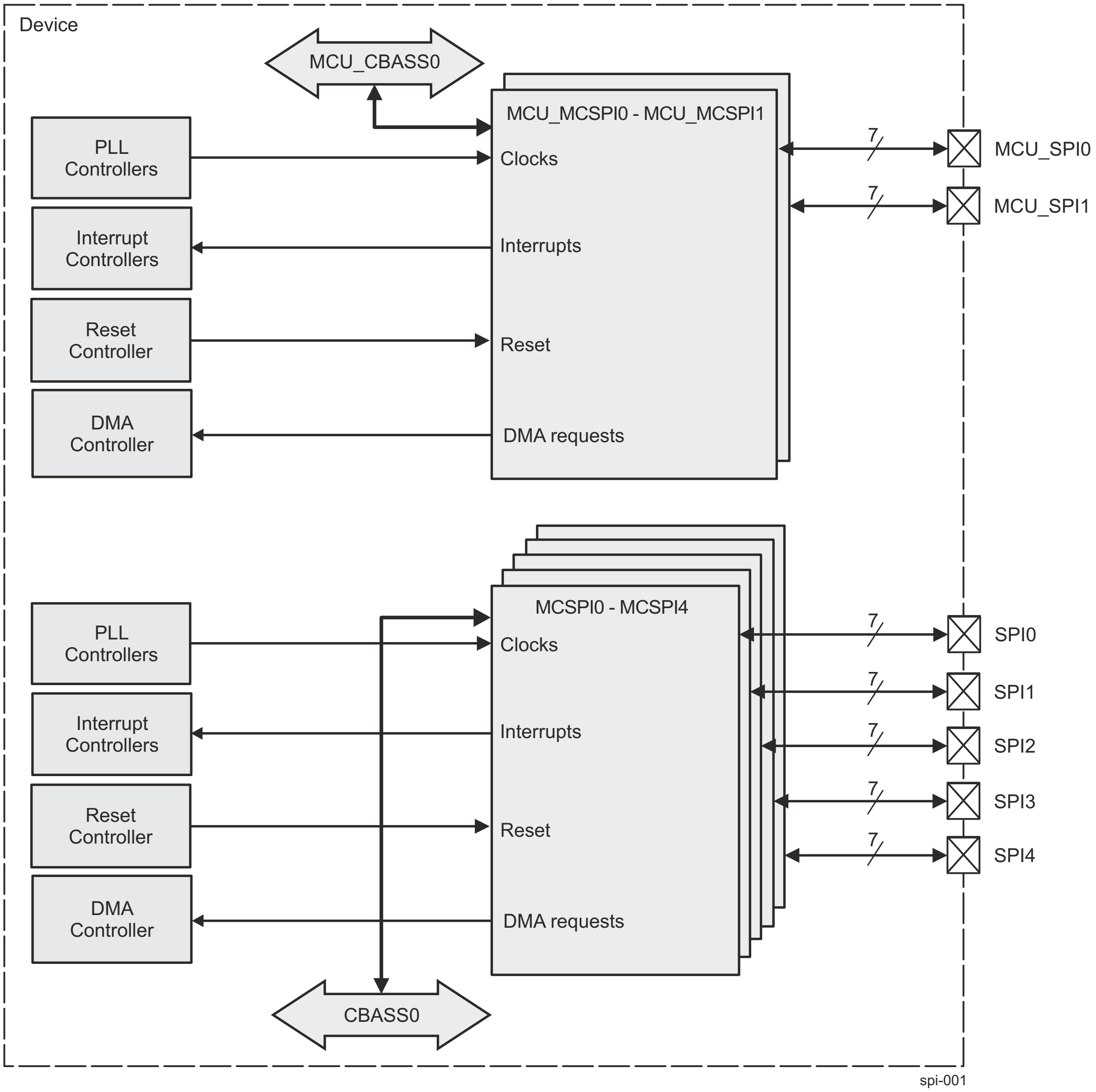

Figure 12-38. MCSPI Overview

12.1.4.1.1 SPI Features

The SPI module includes the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four channels in controller mode, or single channel in receive mode
- Controller multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - Per channel configuration for clock definition, polarity enabling, and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for MCSPI transfer per channel (start-bit mode)

- Supports start-bit write command
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel

12.1.4.1.2 SPI Not Supported Features

The following features are not supported on this family of devices:

- Peripheral mode wake-up
- Retention during power down
- In peripheral mode only channel 0 is used
- Local power management of clock activity

12.1.4.2 MCSPI Environment

The MCU_MCSPI[1-0] and MCSPI[4-0] modules are hereinafter referred to as MCSPI module.

This section describes the MCSPI external connections (environment).

12.1.4.2.1 Basic MCSPI Pins for Controller Mode

Figure 12-39 shows all of the MCSPI interface signals in controller mode.

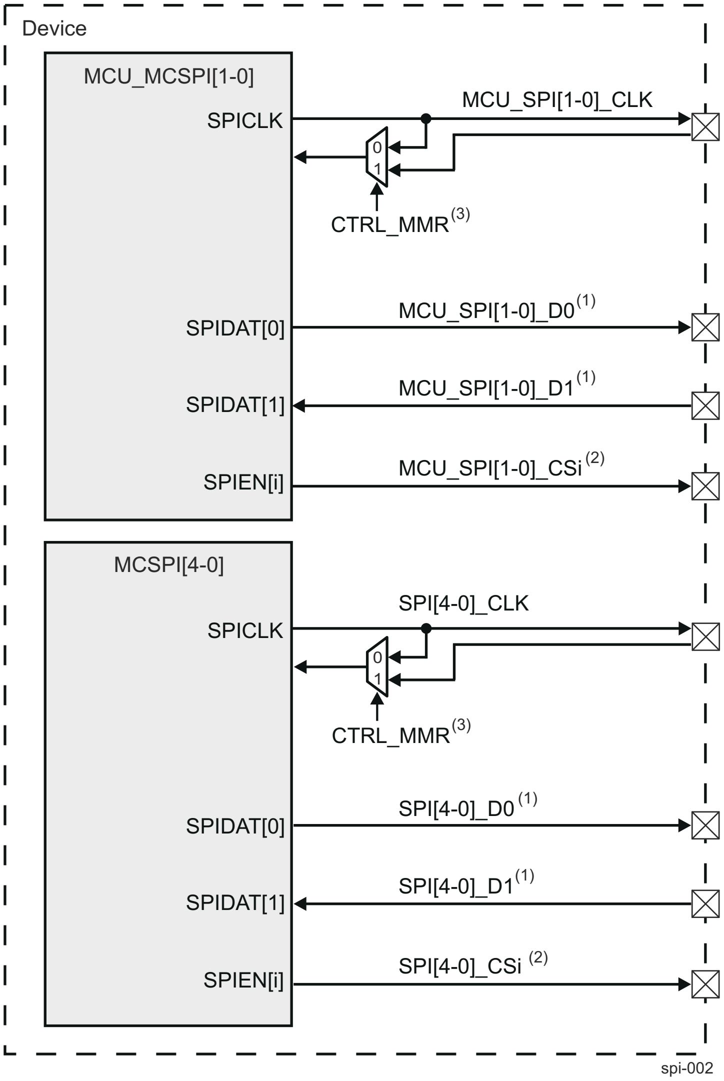

Note

Direction depends on MCSPI_CH0CONF/1/2/3[16] DPE0, MCSPI_CH0CONF/1/2/3[17] DPE1 and MCSPI_CH0CONF/1/2/3[18] IS bits

Note

i = 0 to 3

Note

The source of the loopback clock is defined by MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL[16] MSTR_LB_CLKSEL bit (and the respective register for MCU_MCSPI1) and MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY[16] MSTR_LB_CLKSEL bit (and the respective for MCSPI[4-1]) in Section 5.1 , *Control Module (CTRL_MMR)*.

Figure 12-39. MCSPI Interface Signals in Controller Mode

Table 12-46 describes the MCSPI I/O signals in controller mode.

Table 12-46. MCSPI I/O Signals (Controller Mode)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
			MCU_MCSPI[1-0]	
SPICLK	MCU_SPI[1-0]_CLK	O	MCSPI Serial clock output for controller mode.	HiZ
SPIDAT[0]	MCU_SPI[1-0]_D0	O(3)	MCSPI Data I/O for controller mode.	HiZ
SPIDAT[1]	MCU_SPI[1-0]_D1	I(4)	MCSPI Data I/O for controller mode.	HiZ
SPIEN[i]	MCU_SPI[1-0]_CSi	O	MCSPI Chip-select i output for controller mode	HiZ
			MCSPI[4-0]	
SPICLK	SPI[4-0]_CLK	O	MCSPI Serial clock output for controller mode.	HiZ
SPIDAT[0]	SPI[4-0]_D0	O(3)	MCSPI Data I/O for controller mode.	HiZ
SPIDAT[1]	SPI[4-0]_D1	I(4)	MCSPI Data I/O for controller mode.	HiZ
SPIEN[i]	SPI[4-0]_CSi	O	MCSPI Chip-select i output for controller mode	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH0CONF/1/2/3[18] IS and MCSPI_CH0CONF/1/2/3[16] DPE0.

(4) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH0CONF/1/2/3[18] IS and MCSPI_CH0CONF/1/2/3[17] DPE1.

Note

For SPI[4-0]_CLK and MCU_SPI[1-0]_CLK signals to work properly, the RXACTIVE bit of the appropriate CTRLMMR_MCU_PADCONFIGx/ CTRLMMR_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.1.4.2.2 Basic MCSPI Pins for Peripheral Mode

Figure 12-40 shows all of the MCSPI interface signals in peripheral mode.

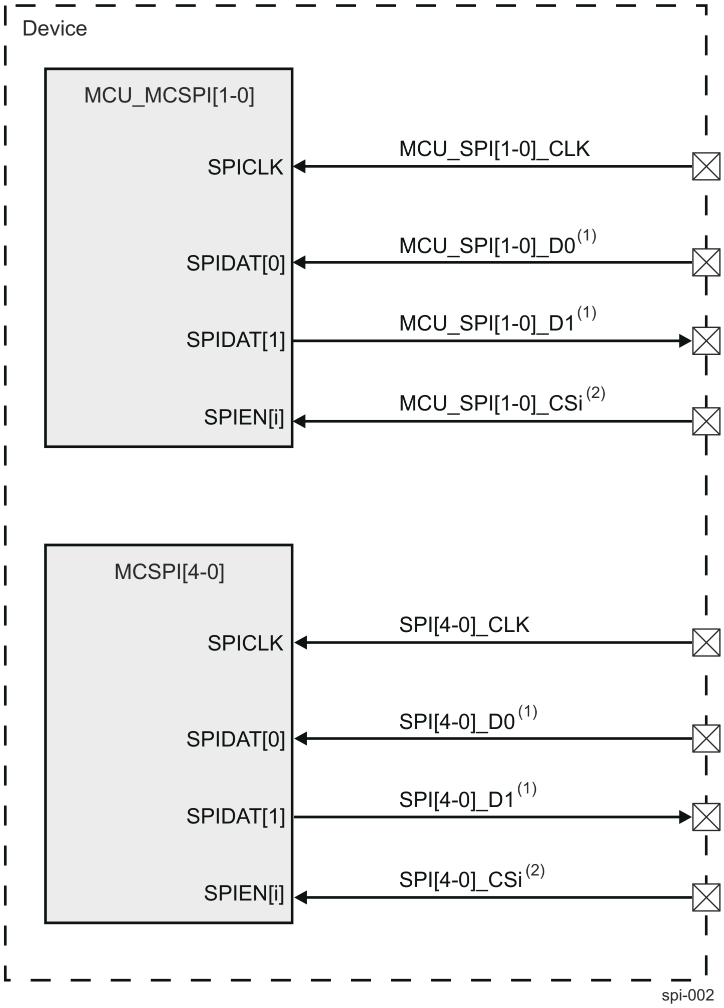

Note

Direction depends on MCSPI_CH0CONF/1/2/3[16] DPE0, MCSPI_CH0CONF/1/2/3[17] DPE1 and MCSPI_CH0CONF/1/2/3[18] IS bits

Note

i = 0 to 3

Figure 12-40. MCSPI Interface Signals in Peripheral Mode

Table 12-47 describes the MCSPI I/O signals in peripheral mode.

Table 12-47. MCSPI I/O Signals (Peripheral Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[1]
		MCU_MCSPI[1-0]		
SPICLK	MCU_SPI[1-0]_CLK	I	MCSPI serial clock input for peripheral mode.	HiZ
SPIDAT[0]	MCU_SPI[1-0]_D0	I[2]	MCSPI Data I/O for peripheral mode.	HiZ
SPIDAT[1]	MCU_SPI[1-0]_D1	O[3]	MCSPI Data I/O for peripheral mode.	HiZ
SPIEN[i]	MCU_SPI[1-0]_CSi	I[4]	MCSPI chip-select i input for peripheral mode.	HiZ
		MCSPI[4-0]		
SPICLK	SPI[4-0]_CLK	I	MCSPI serial clock input for peripheral mode.	HiZ

Table 12-47. MCSPI I/O Signals (Peripheral Mode) (continued)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[1]
SPIDAT[0]	SPI[4-0]_D0	I[2]	MCSPI Data I/O for peripheral mode.	HiZ
SPIDAT[1]	SPI[4-0]_D1	O[3]	MCSPI Data I/O for peripheral mode.	HiZ
SPIEN[i]	SPI[4-0]_CSi	I[4]	MCSPI chip-select i input for peripheral mode.	HiZ

(1) HiZ = High Impedance

(2) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH0CONF/1/2/3[18] IS and MCSPI_CH0CONF/1/2/3[16] DPE0.

(3) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH0CONF/1/2/3[18] IS and MCSPI_CH0CONF/1/2/3[17] DPE1.

(4) The chip-select input in peripheral mode can be selected through the MCSPI_CH0CONF/1/2/3[22-21] SPIENSLV bit field.

Note

For SPI[4-0]_CLK and MCU_SPI[1-0]_CLK signals to work properly, the RXACTIVE bit of the appropriate CTRLMMR_MCU_PADCONFIGx/ CTRLMMR_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.1.4.2.3 MCSPI Protocol and Data Format

The synchronous MCSPI protocol allows a controller device to initiate serial data transfers to a peripheral device. A peripheral select line (SPIEN[i]) allows selection of an individual peripheral MCSPI device. Peripheral devices that are not selected do not interfere with MCSPI bus activities.

MCSPI offers the flexibility to modify the following parameters to adapt to the device features:

- Word length

  MCSPI supports any MCSPI word ranging from 4 bits to 32 bits long (the MCSPI_CHCONF_0/1/2/3[11-7] WL bit field).

  MCSPI word length can be changed between transmissions to allow the controller device to communicate with peripheral peripherals that have different requirements.
- MCSPI enable (SPIEN[i], for channel i)

  The polarity of the MCSPI enable signals is programmable (the MCSPI_CHCONF_0/1/2/3[6] EPOL bit). SPIEN[i] signals can be active high or low.

  Assertion of the SPIEN[i] signals is programmable and can be done manually or automatically. The manual assertion mode is available in single controller mode only. SPIEN[i] can be kept active between words with the MCSPI_CHCONF_0/1/2/3[20] FORCE bit.

  Two consecutive words for two different peripheral devices can go along with active SPIEN[i] signals with different polarity.
- Programmable start-bit

  In start-bit mode a start-bit is added before the MCSPI word length to indicate how the next MCSPI word must be handled. The start-bit is enabled by setting the MCSPI_CHCONF_0/1/2/3[23] SBE bit to 1. The MCSPI_CHCONF_0/1/2/3[24] SBPOL bit defines the polarity of the start-bit.
- Programmable MCSPI clock

- Bit rate

  In controller mode, the baud rate of the MCSPI serial clock is programmable using the 50-MHz reference clock (from the device clock management module). Table 12-48 lists the SPICLK bit rates obtained for data transfer when programming the clock divider (the MCSPI_CHCONF_0/1/2/3[5-2] CLKD bit field). This is valid when MCSPI_CHCONF_0/1/2/3[29] CLKD bit field is 0.

Table 12-48. MCSPI Controller Clock Rates

Divider	Clock Rate
1	50 MHz(1)
2	25 MHz(1)
4	12.5 MHz
8	6.25 MHz
16	3.125 MHz
32	1.5625 MHz
64	781.25 kHz
128	390.625 kHz
256	~195 kHz
512	~97.7 kHz
1024	~48.8 kHz
2048	~24.4 kHz
4096	~12.2 kHz

(1) These frequencies are not necessarily supported by all MCSPI modules. For more information, see the *Timing Requirements and Switching Characteristics* chapter in the device-specific Data sheet.

- Polarity and phase

  The polarity (the MCSPI_CHCONF_0/1/2/3[1] POL bit) and the phase (the MCSPI_CHCONF_0/1/2/3[0] PHA bit) of the MCSPI serial clock (SPICLK) are configurable to offer four combinations. Software selects the right combination, depending on the device. See Table 12-49 and Figure 12-41.

Table 12-49. Phase and Polarity Combinations

Polarity (POL)	Phase (PHA)	MCSPI Mode	Description
0	0	Mode 0	SPICLK is inactive low and sampling occurs at the rising edge.
0	1	Mode 1	SPICLK is inactive low and sampling occurs at the falling edge.
1	0	Mode 2	SPICLK is inactive high and sampling occurs at the falling edge.
1	1	Mode 3	SPICLK is inactive high and sampling occurs at the rising edge.

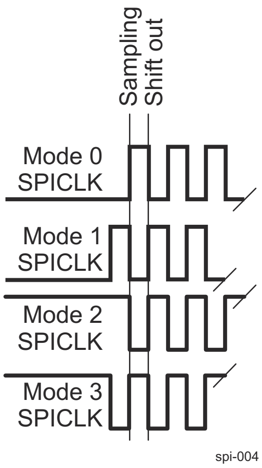

Figure 12-41. Phase and Polarity Combinations

12.1.4.2.3.1 Transfer Format

In controller and peripheral modes, the MCSPI drives the data lines when SPIEN[i] is asserted.

Each word is transmitted starting with the most-significant bit (MSB).

This section explains the two cases of data transmission determined by the clock phase (PHA) and the type of data transmission using a start-bit (SBE) called the start-bit mode:

- Transmission in mode 0 and mode 2 (PHA = 0)

  When PHA = 0, the first bit of the MCSPI word to transmit (on the controller or the peripheral data output pin) is valid one-half cycle of SPICLK after the assertion of SPIEN[i].

  Therefore, the first edge of the SPICLK line is used by the controller to sample the first data bit sent by the peripheral. On the same edge, the first data bit sent by the controller is sampled by the peripheral.

  On the next SPICLK edge, the received data bit is shifted into the receive shift register and a new data bit is transmitted on the serial data line.

  This process continues for a number of pulses on the SPICLK line defined by the MCSPI word length programmed in the controller device, with data being latched on odd-numbered edges and shifted on even-numbered edges, see Figure 12-42.

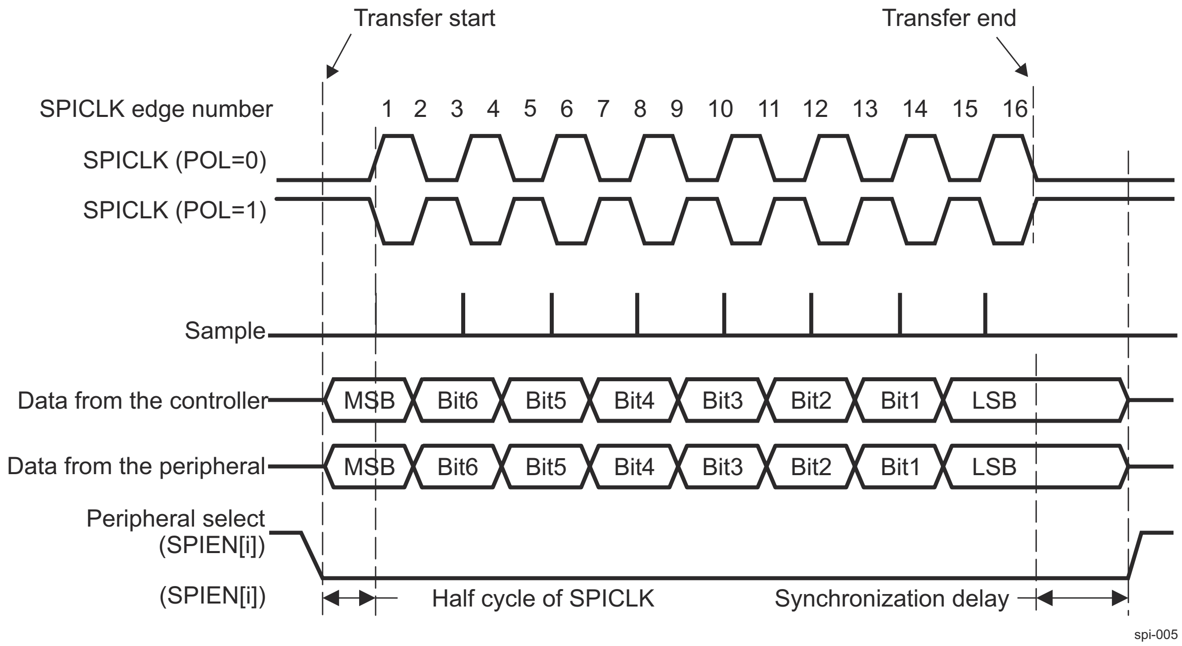

Figure 12-42. Full-Duplex Transfer Format With PHA = 0

- Transmission in mode 1 and mode 3 (PHA = 1)

  When PHA = 1, the first bit of the MCSPI word to transmit (on the controller or the peripheral data output pin) is valid on the following SPICLK edge (one-half cycle later). This is the sampling edge for the controller and peripheral. A synchronization delay is added between the activation of SPIEN[i] and the first SPICLK edge.

  The received data bit is shifted into the shift register on the third SPICLK edge.

  This process continues for a number of pulses on the SPICLK line defined by the MCSPI word length programmed in the controller device, with data being latched on even-numbered edges and shifted on odd-numbered edges.

  Note

  The minimum synchronization delay is one cycle of SPICLK, if the frequency of SPICLK equals the frequency of MCSPI_FCLK (MCSPI functional clock) in controller mode. The minimum synchronization delay is one-half cycle of SPICLK, if the frequency of SPICLK is lower than the frequency of MCSPI_FCLK in the controller and peripheral modes.

- Transmission with a start-bit (SBE = 1)

  When the MCSPI_CHCONF_0/1/2/3[23] SBE bit is set to 1, a start-bit is added before the MSB to indicate whether the next MCSPI word must be handled as a command or as data.

  Figure 12-43 shows an example of a data transfer with an extra start-bit.

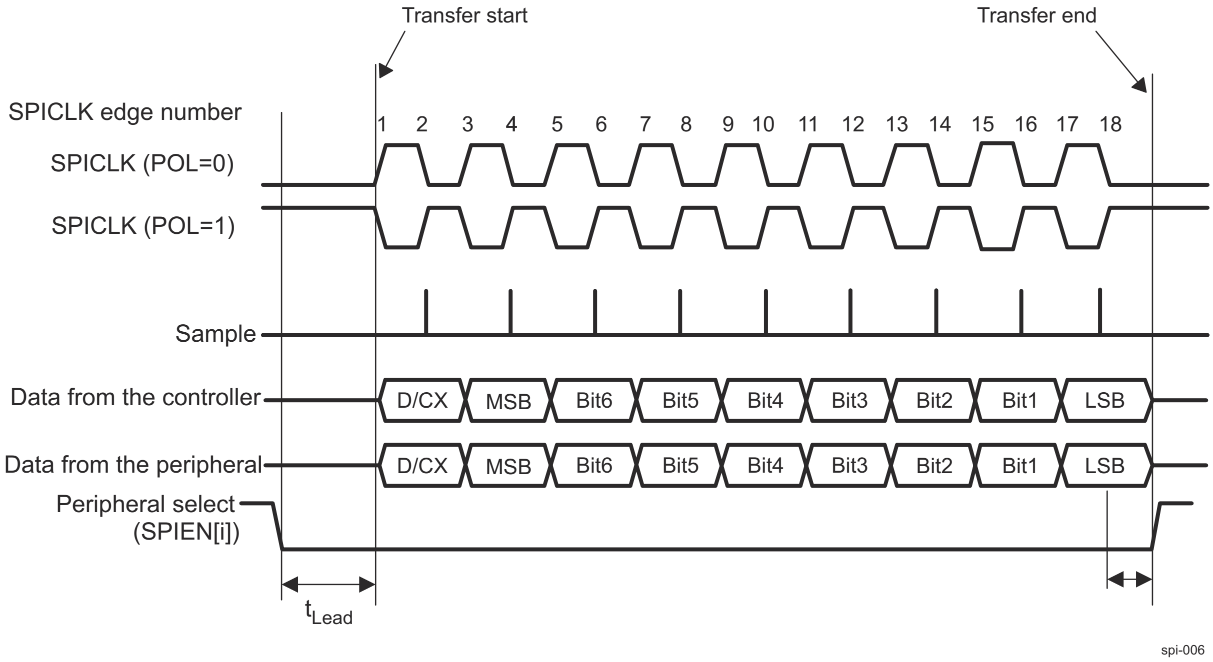

Figure 12-43. Extended MCSPI Transfer With a Start-Bit (SBE = 1)

12.1.4.2.4 MCSPI in Controller Mode

Figure 12-44 shows a case in controller mode (full-duplex) where the MCSPI module is connected with two peripheral devices.

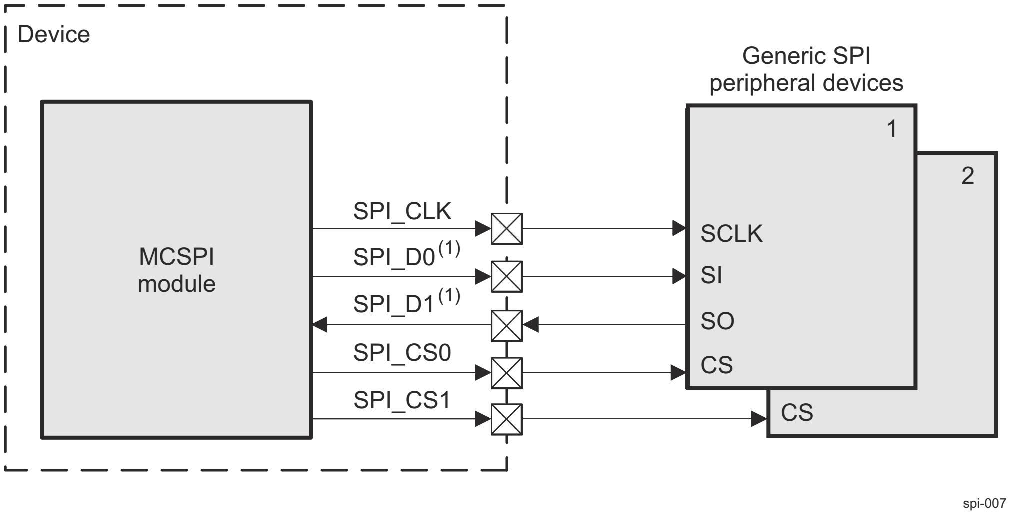

Note

Direction depends on MCSPI_CHCONF_0/1/2/3[16] DPE0, MCSPI_CHCONF_0/1/2/3[17] DPE1 and MCSPI_CHCONF_0/1/2/3[18] IS bits

Figure 12-44. MCSPI Controller Mode (Full Duplex)

Figure 12-45 shows the controller single mode, which can also be configured in receive-only mode.

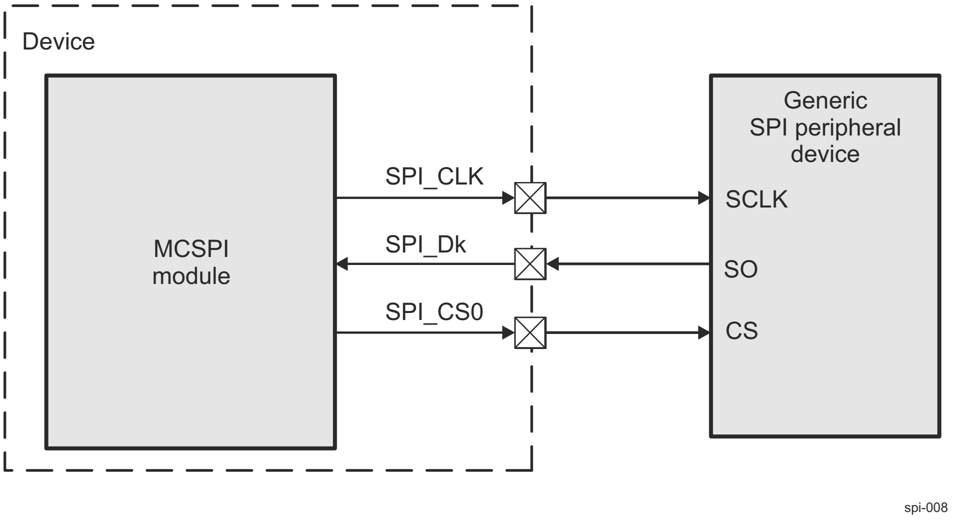

Note

k = 0 or 1 depending on MCSPI_CHCONF_0/1/2/3[16] DPE0, MCSPI_CHCONF_0/1/2/3[17] DPE1 and MCSPI_CHCONF_0/1/2/3[18] IS bits

---

Figure 12-45. MCSPI Controller Single Mode (Receive Only)

12.1.4.2.5 MCSPI in Peripheral Mode

Figure 12-46 shows a case in peripheral mode (full-duplex).

Note

Only channel 0 can be configured as peripheral, but the chip-enable signal can be connected to any SPIEN[i] pin and then rerouted internally to channel 0 (the MCSPI_CHCONF_0[22-21] SPIENSLV bit field). For more information, see Section 12.1.4.4.4 , *MCSPI Peripheral Mode*.

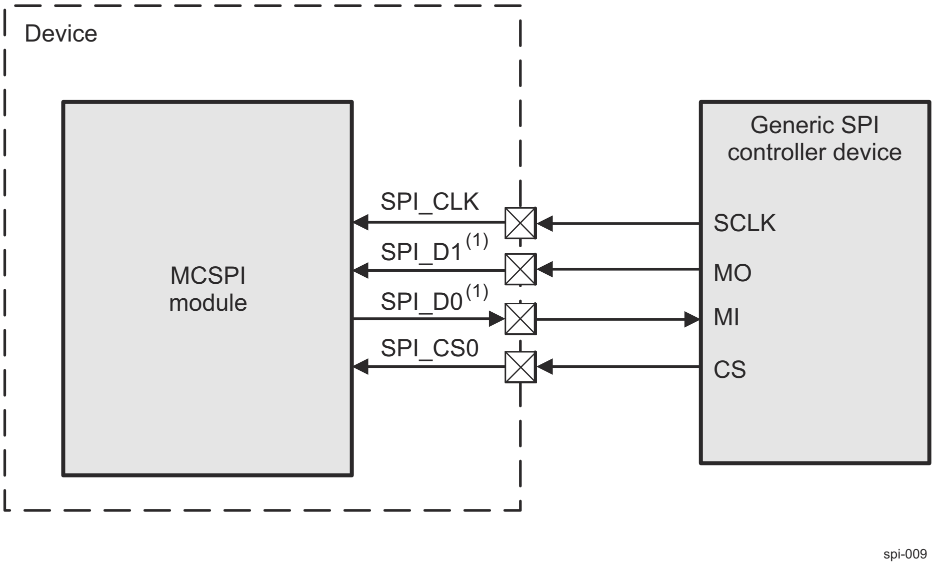

Note

Direction depends on MCSPI_CHCONF_0/1/2/3[16] DPE0, MCSPI_CHCONF_0/1/2/3[17] DPE1 and MCSPI_CHCONF_0/1/2/3[18] IS bits

Figure 12-46. MCSPI Peripheral Mode (Full Duplex)

Figure 12-47 shows the peripheral single mode, which can also be configured in transmit-only mode.

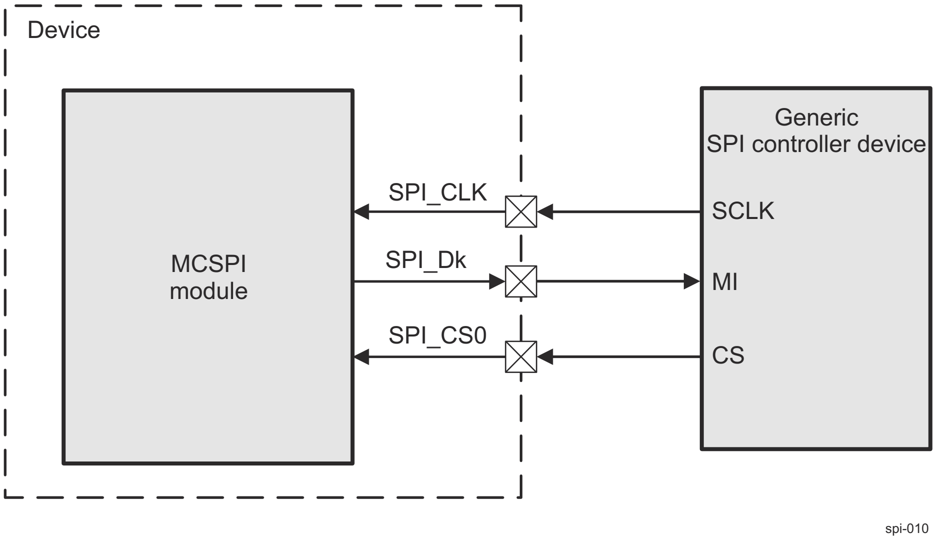

Note

k = 0 or 1 depending on MCSPI_CHCONF_0/1/2/3[16] DPE0, MCSPI_CHCONF_0/1/2/3[17] DPE1 and MCSPI_CHCONF_0/1/2/3[18] IS bits

Figure 12-47. MCSPI Peripheral Single Mode (Transmit Only)

12.1.4.3 MCSPI Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

12.1.4.3.1 MCSPI Integration in MCU Domain

There are two MCSPI modules integrated in the device MCU domain - MCU_MCSPI0 and MCU_MCSPI1. Figure 12-48 shows their integration in the device.

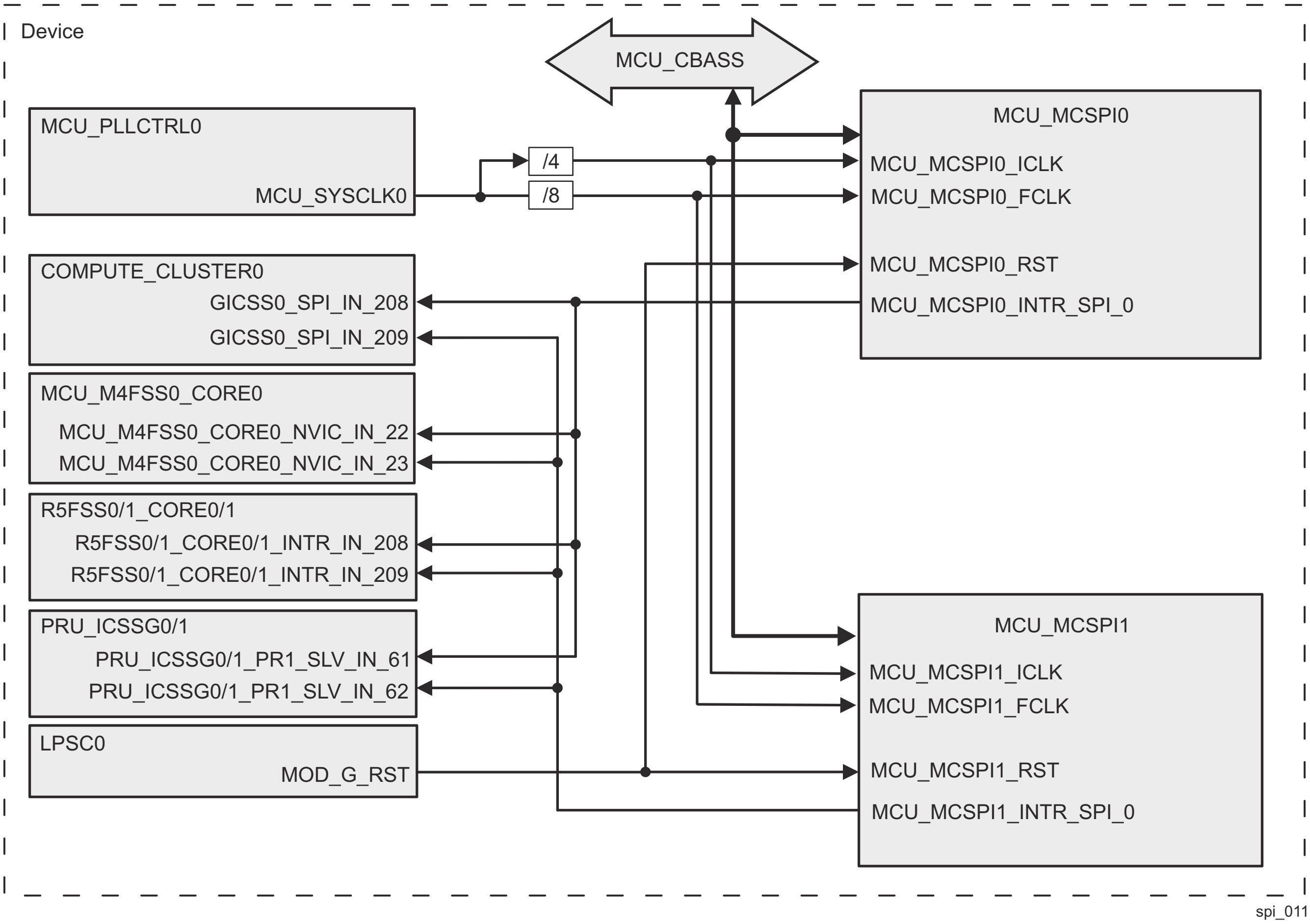

Figure 12-48. MCU_MCSPI Integration

Table 12-50 through Table 12-53 summarize the integration of MCU_MCSPI0 and MCU_MCSPI1 in device MCU domain.

Table 12-50. MCU_MCSPI Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_MCSPI0	MCU_PSC0	PD0	LPSC0	MCU_CBASS0
MCU_MCSPI1	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-51. MCU_MCSPI Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_MCSPI0	MCU_MCSPI0_ICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_MCSPI0 Interface Clock
	MCU_MCSPI0_FCLK	MCU_SYSCLK0/8		MCU_MCSPI0 Functional Clock
MCU_MCSPI1	MCU_MCSPI1_ICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_MCSPI1 Interface Clock
	MCU_MCSPI1_FCLK	MCU_SYSCLK0/8		MCU_MCSPI1 Functional Clock

Table 12-52. MCU_MCSPI Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_MCSPI0	MCU_MCSPI0_RST	MOD_G_RST	LPSC0	MCU_MCSPI0 Asynchronous Reset
MCU_MCSPI1	MCU_MCSPI1_RST	MOD_G_RST	LPSC0	MCU_MCSPI1 Asynchronous Reset

Table 12-53. MCU_MCSPI Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_MCSPI0	MCU_MCSPI0_INTR_SPI_0	GICSS0_SPI_IN_208	COMPUTE_CLUSTER0	MCU_MCSPI0 Interrupt Request	Level
		MCU_M4FSS0_CORE0_NVIC_IN_22	MCU_M4FSS0_CORE0	MCU_MCSPI0 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_208	R5FSS0_CORE0	MCU_MCSPI0 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_208	R5FSS0_CORE1	MCU_MCSPI0 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_208	R5FSS1_CORE0	MCU_MCSPI0 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_208	R5FSS1_CORE1	MCU_MCSPI0 Interrupt Request	Level
		PRU_ICSSG0_PR1_SLV_IN_61	PRU_ICSSG0	MCU_MCSPI0 Interrupt Request	Level
		PRU_ICSSG1_PR1_SLV_IN_61	PRU_ICSSG1	MCU_MCSPI0 Interrupt Request	Level
MCU_MCSPI1	MCU_MCSPI1_INTR_SPI_0	GICSS0_SPI_IN_209	COMPUTE_CLUSTER0	MCU_MCSPI1 Interrupt Request	Level
		MCU_M4FSS0_CORE0_NVIC_IN_23	MCU_M4FSS0_CORE0	MCU_MCSPI1 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_209	R5FSS0_CORE0	MCU_MCSPI1 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_209	R5FSS0_CORE1	MCU_MCSPI1 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_209	R5FSS1_CORE0	MCU_MCSPI1 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_209	R5FSS1_CORE1	MCU_MCSPI1 Interrupt Request	Level
		PRU_ICSSG0_PR1_SLV_IN_62	PRU_ICSSG0	MCU_MCSPI1 Interrupt Request	Level
		PRU_ICSSG1_PR1_SLV_IN_62	PRU_ICSSG1	MCU_MCSPI1 Interrupt Request	Level

12.1.4.3.2 MCSPI Integration in MAIN Domain

There are five MCSPI modules integrated in the device MAIN domain - MCSPI0, MCSPI1, MCSPI2, MCSPI3, and MCSPI4. Figure 12-49 shows their integration in the device.

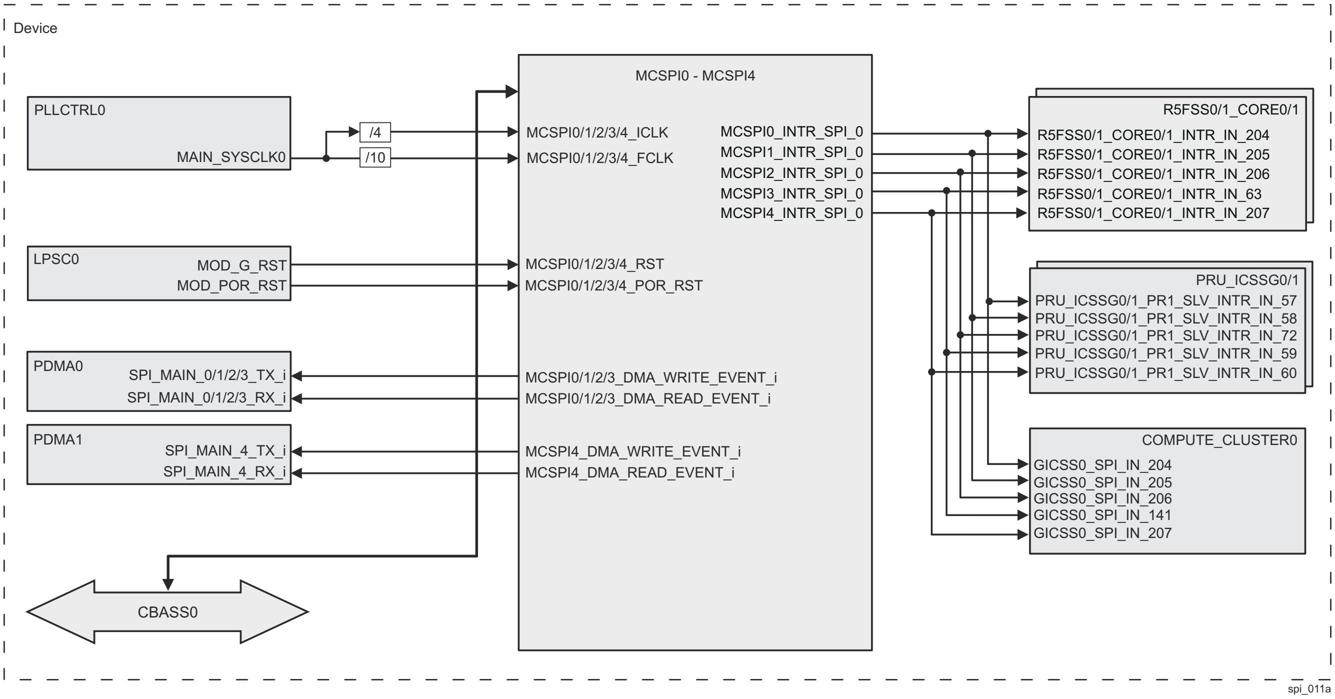

Note

i = 0, 1, 2, 3

Figure 12-49. MCSPI Integration

Table 12-54 through Table 12-57 summarize the integration of MCSPI0, MCSPI1, MCSPI2, MCSPI3, and MCSPI4 in device MAIN domain.

Table 12-54. MCSPI Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCSPI0	PSC0	PD0	LPSC0	CBASS0
MCSPI1	PSC0	PD0	LPSC0	CBASS0
MCSPI2	PSC0	PD0	LPSC0	CBASS0
MCSPI3	PSC0	PD0	LPSC0	CBASS0
MCSPI4	PSC0	PD0	LPSC0	CBASS0

Table 12-55. MCSPI Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCSPI0	MCSPI0_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	MCSPI0 Interface Clock
	MCSPI0_FCLK	MAIN_SYSCLK0/10		MCSPI0 Functional Clock
MCSPI1	MCSPI1_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	MCSPI1 Interface Clock
	MCSPI1_FCLK	MAIN_SYSCLK0/10		MCSPI1 Functional Clock
MCSPI2	MCSPI2_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	MCSPI2 Interface Clock
	MCSPI2_FCLK	MAIN_SYSCLK0/10		MCSPI2 Functional Clock
MCSPI3	MCSPI3_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	MCSPI3 Interface Clock
	MCSPI3_FCLK	MAIN_SYSCLK0/10		MCSPI3 Functional Clock

Table 12-55. MCSPI Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCSPI4	MCSPI4_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	MCSPI4 Interface Clock
	MCSPI4_FCLK	MAIN_SYSCLK0/10		MCSPI4 Functional Clock

Table 12-56. MCSPI Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCSPI0	MCSPI0_RST	MOD_G_RST	LPSC0	MCSPI0 Asynchronous Reset
	MCSPI0_POR_RST	MOD_POR_RST	LPSC0	MCSPI0 Power-On Reset
MCSPI1	MCSPI1_RST	MOD_G_RST	LPSC0	MCSPI1 Asynchronous Reset
	MCSPI1_POR_RST	MOD_POR_RST	LPSC0	MCSPI1 Power-On Reset
MCSPI2	MCSPI2_RST	MOD_G_RST	LPSC0	MCSPI2 Asynchronous Reset
	MCSPI3_POR_RST	MOD_POR_RST	LPSC0	MCSPI2 Power-On Reset
MCSPI3	MCSPI3_RST	MOD_G_RST	LPSC0	MCSPI3 Asynchronous Reset
	MCSPI3_POR_RST	MOD_POR_RST	LPSC0	MCSPI3 Power-On Reset
MCSPI4	MCSPI4_RST	MOD_G_RST	LPSC0	MCSPI4 Asynchronous Reset
	MCSPI4_POR_RST	MOD_POR_RST	LPSC0	MCSPI4 Power-On Reset

Table 12-57. MCSPI Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI0	MCSPI0_INTR_SPI_0	GICSS0_SPI_IN_204	COMPUTE_CLUSTER0	MCSPI0 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_204	R5FSS0_CORE0	MCSPI0 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_204	R5FSS0_CORE1	MCSPI0 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_204	R5FSS1_CORE0	MCSPI0 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_204	R5FSS1_CORE1	MCSPI0 Interrupt Request	Level
		PRU_ICSSG0_PR1_SLV_IN_57	PRU_ICSSG0	MCSPI0 Interrupt Request	Level
		PRU_ICSSG1_PR1_SLV_IN_57	PRU_ICSSG1	MCSPI0 Interrupt Request	Level
MCSPI1	MCSPI1_INTR_SPI_0	GICSS0_SPI_IN_205	COMPUTE_CLUSTER0	MCSPI1 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_205	R5FSS0_CORE0	MCSPI1 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_205	R5FSS0_CORE1	MCSPI1 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_205	R5FSS1_CORE0	MCSPI1 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_205	R5FSS1_CORE1	MCSPI1 Interrupt Request	Level
		PRU_ICSSG0_PR1_SLV_IN_58	PRU_ICSSG0	MCSPI1 Interrupt Request	Level
		PRU_ICSSG1_PR1_SLV_IN_58	PRU_ICSSG1	MCSPI1 Interrupt Request	Level
MCSPI2	MCSPI2_INTR_SPI_0	GICSS0_SPI_IN_206	COMPUTE_CLUSTER0	MCSPI2 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_206	R5FSS0_CORE0	MCSPI2 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_206	R5FSS0_CORE1	MCSPI2 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_206	R5FSS1_CORE0	MCSPI2 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_206	R5FSS1_CORE1	MCSPI2 Interrupt Request	Level
		PRU_ICSSG0_PR1_SLV_IN_72	PRU_ICSSG0	MCSPI2 Interrupt Request	Level
		PRU_ICSSG1_PR1_SLV_IN_72	PRU_ICSSG1	MCSPI2 Interrupt Request	Level
MCSPI3	MCSPI3_INTR_SPI_0	GICSS0_SPI_IN_141	COMPUTE_CLUSTER0	MCSPI3 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_63	R5FSS0_CORE0	MCSPI3 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_63	R5FSS0_CORE1	MCSPI3 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_63	R5FSS1_CORE0	MCSPI3 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_63	R5FSS1_CORE1	MCSPI3 Interrupt Request	Level
		PRU_ICSSG0_PR1_SLV_IN_59	PRU_ICSSG0	MCSPI3 Interrupt Request	Level
		PRU_ICSSG1_PR1_SLV_IN_59	PRU_ICSSG1	MCSPI3 Interrupt Request	Level

Table 12-57. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI4	MCSPI4_INTR_SPI_0	GICSS0_SPI_IN_207	COMPUTE_CLUSTER0	MCSPI4 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_207	R5FSS0_CORE0	MCSPI4 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_207	R5FSS0_CORE1	MCSPI4 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_207	R5FSS1_CORE0	MCSPI4 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_207	R5FSS1_CORE1	MCSPI4 Interrupt Request	Level
		PRU_ICSSG0_PR1_SLV_IN_60	PRU_ICSSG0	MCSPI4 Interrupt Request	Level
		PRU_ICSSG1_PR1_SLV_IN_60	PRU_ICSSG1	MCSPI4 Interrupt Request	Level
DMA Events					
Module Instance	**Module DMA Event**	**Destination DMA Event Input**	**Destination**	**Description**	**Type**
MCSPI0	MCSPI0_DMA_WRITE_EVENT_0	SPI_MAIN_0_TX_0	PDMA0	MCSPI0 Channel 0 Transmit (Write) Request Line	Pulse
	MCSPI0_DMA_READ_EVENT_0	SPI_MAIN_0_RX_0	PDMA0	MCSPI0 Channel 0 Receive (Read) Request Line	Pulse
	MCSPI0_DMA_WRITE_EVENT_1	SPI_MAIN_0_TX_1	PDMA0	MCSPI0 Channel 1 Transmit (Write) Request Line	Pulse
	MCSPI0_DMA_READ_EVENT_1	SPI_MAIN_0_RX_1	PDMA0	MCSPI0 Channel 1 Receive (Read) Request Line	Pulse
	MCSPI0_DMA_WRITE_EVENT_2	SPI_MAIN_0_TX_2	PDMA0	MCSPI0 Channel 2 Transmit (Write) Request Line	Pulse
	MCSPI0_DMA_READ_EVENT_2	SPI_MAIN_0_RX_2	PDMA0	MCSPI0 Channel 2 Receive (Read) Request Line	Pulse
	MCSPI0_DMA_WRITE_EVENT_3	SPI_MAIN_0_TX_3	PDMA0	MCSPI0 Channel 3 Transmit (Write) Request Line	Pulse
	MCSPI0_DMA_READ_EVENT_3	SPI_MAIN_0_RX_3	PDMA0	MCSPI0 Channel 3 Receive (Read) Request Line	Pulse
MCSPI1	MCSPI1_DMA_WRITE_EVENT_0	SPI_MAIN_1_TX_0	PDMA0	MCSPI1 Channel 0 Transmit (Write) Request Line	Pulse
	MCSPI1_DMA_READ_EVENT_0	SPI_MAIN_1_RX_0	PDMA0	MCSPI1 Channel 0 Receive (Read) Request Line	Pulse
	MCSPI1_DMA_WRITE_EVENT_1	SPI_MAIN_1_TX_1	PDMA0	MCSPI1 Channel 1 Transmit (Write) Request Line	Pulse
	MCSPI1_DMA_READ_EVENT_1	SPI_MAIN_1_RX_1	PDMA0	MCSPI1 Channel 1 Receive (Read) Request Line	Pulse
	MCSPI1_DMA_WRITE_EVENT_2	SPI_MAIN_1_TX_2	PDMA0	MCSPI1 Channel 2 Transmit (Write) Request Line	Pulse
	MCSPI1_DMA_READ_EVENT_2	SPI_MAIN_1_RX_2	PDMA0	MCSPI1 Channel 2 Receive (Read) Request Line	Pulse
	MCSPI1_DMA_WRITE_EVENT_3	SPI_MAIN_1_TX_3	PDMA0	MCSPI1 Channel 3 Transmit (Write) Request Line	Pulse
	MCSPI1_DMA_READ_EVENT_3	SPI_MAIN_1_RX_3	PDMA0	MCSPI1 Channel 3 Receive (Read) Request Line	Pulse
MCSPI2	MCSPI2_DMA_WRITE_EVENT_0	SPI_MAIN_2_TX_0	PDMA0	MCSPI2 Channel 0 Transmit (Write) Request Line	Pulse
	MCSPI2_DMA_READ_EVENT_0	SPI_MAIN_2_RX_0	PDMA0	MCSPI2 Channel 0 Receive (Read) Request Line	Pulse

Table 12-57. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
	MCSPI2_DMA_WRITE_EVENT_1	SPI_MAIN_2_TX_1	PDMA0	MCSPI2 Channel 1 Transmit (Write) Request Line	Pulse
	MCSPI2_DMA_READ_EVENT_1	SPI_MAIN_2_RX_1	PDMA0	MCSPI2 Channel 1 Receive (Read) Request Line	Pulse
	MCSPI2_DMA_WRITE_EVENT_2	SPI_MAIN_2_TX_2	PDMA0	MCSPI2 Channel 2 Transmit (Write) Request Line	Pulse
	MCSPI2_DMA_READ_EVENT_2	SPI_MAIN_2_RX_2	PDMA0	MCSPI2 Channel 2 Receive (Read) Request Line	Pulse
	MCSPI2_DMA_WRITE_EVENT_3	SPI_MAIN_2_TX_3	PDMA0	MCSPI2 Channel 3 Transmit (Write) Request Line	Pulse
	MCSPI2_DMA_READ_EVENT_3	SPI_MAIN_2_RX_3	PDMA0	MCSPI2 Channel 3 Receive (Read) Request Line	Pulse
MCSPI3	MCSPI3_DMA_WRITE_EVENT_0	SPI_MAIN_3_TX_0	PDMA0	MCSPI3 Channel 0 Transmit (Write) Request Line	Pulse
	MCSPI3_DMA_READ_EVENT_0	SPI_MAIN_3_RX_0	PDMA0	MCSPI3 Channel 0 Receive (Read) Request Line	Pulse
	MCSPI3_DMA_WRITE_EVENT_1	SPI_MAIN_3_TX_1	PDMA0	MCSPI3 Channel 1 Transmit (Write) Request Line	Pulse
	MCSPI3_DMA_READ_EVENT_1	SPI_MAIN_3_RX_1	PDMA0	MCSPI3 Channel 1 Receive (Read) Request Line	Pulse
	MCSPI3_DMA_WRITE_EVENT_2	SPI_MAIN_3_TX_2	PDMA0	MCSPI3 Channel 2 Transmit (Write) Request Line	Pulse
	MCSPI3_DMA_READ_EVENT_2	SPI_MAIN_3_RX_2	PDMA0	MCSPI3 Channel 2 Receive (Read) Request Line	Pulse
	MCSPI3_DMA_WRITE_EVENT_3	SPI_MAIN_3_TX_3	PDMA0	MCSPI3 Channel 3 Transmit (Write) Request Line	Pulse
	MCSPI3_DMA_READ_EVENT_3	SPI_MAIN_3_RX_3	PDMA0	MCSPI3 Channel 3 Receive (Read) Request Line	Pulse
MCSPI4	MCSPI4_DMA_WRITE_EVENT_0	SPI_MAIN_4_TX_0	PDMA1	MCSPI4 Channel 0 Transmit (Write) Request Line	Pulse
	MCSPI4_DMA_READ_EVENT_0	SPI_MAIN_4_RX_0	PDMA1	MCSPI4 Channel 0 Receive (Read) Request Line	Pulse
	MCSPI4_DMA_WRITE_EVENT_1	SPI_MAIN_4_TX_1	PDMA1	MCSPI4 Channel 1 Transmit (Write) Request Line	Pulse
	MCSPI4_DMA_READ_EVENT_1	SPI_MAIN_4_RX_1	PDMA1	MCSPI4 Channel 1 Receive (Read) Request Line	Pulse
	MCSPI4_DMA_WRITE_EVENT_2	SPI_MAIN_4_TX_2	PDMA1	MCSPI4 Channel 2 Transmit (Write) Request Line	Pulse
	MCSPI4_DMA_READ_EVENT_2	SPI_MAIN_4_RX_2	PDMA1	MCSPI4 Channel 2 Receive (Read) Request Line	Pulse
	MCSPI4_DMA_WRITE_EVENT_3	SPI_MAIN_4_TX_3	PDMA1	MCSPI4 Channel 3 Transmit (Write) Request Line	Pulse
	MCSPI4_DMA_READ_EVENT_3	SPI_MAIN_4_RX_3	PDMA1	MCSPI4 Channel 3 Receive (Read) Request Line	Pulse

Note

MCSPI interrupts are further described in Section 12.1.4.4.7 , *MCSPI Interrupts*.

MCSPI DMA events are further described in Section 12.1.4.4.8 , *MCSPI DMA Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

For more information on the DMA controllers, see Section 11.1 , *Data Movement Architecture (DMA)*.

12.1.4.4 MCSPI Functional Description

12.1.4.4.1 SPI Block Diagram

Figure 12-50 shows the SPI module.

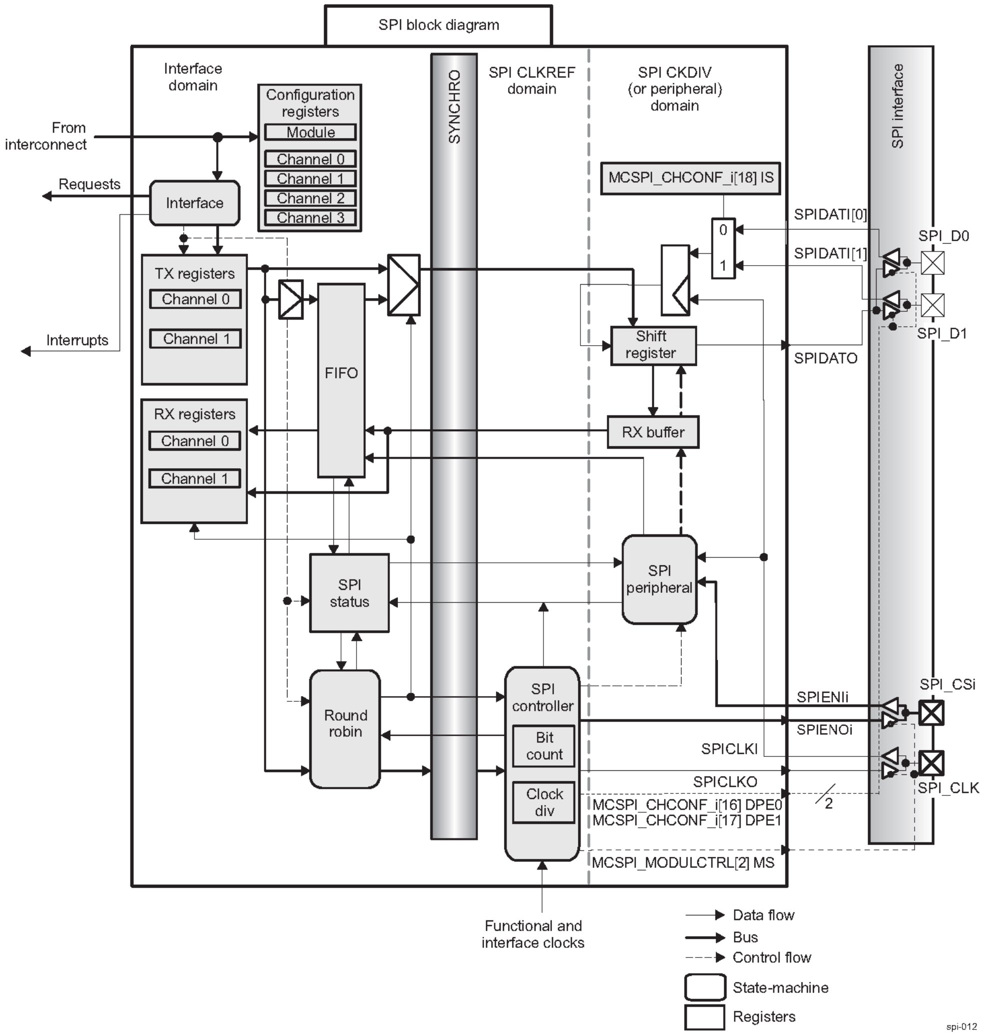

Note

For single channel operation (i=0 or i=1), MCSPI_CHiCON[20]FORCE is asserted over the SPIENIi and SPIENOi lines.

Figure 12-50. SPI Block Diagram

12.1.4.4.2 MCSPI Reset

The MCSPI module can be reset either by hardware or by software reset. All configuration registers and all state machines are reset by the hardware reset signal (MCSPI_RST). MCSPI can be reset by software through the MCSPI_SYSCONFIG[1] SOFTRESET bit. This bit has the same impact on the module as the hardware reset signal. The only exception is that the MCSPI_SYSCONFIG register is not affected by that software reset.

12.1.4.4.3 MCSPI Controller Mode

12.1.4.4.3.1 Controller Mode Features

The MCSPI controller mode supports multichannel communication with up to four independent MCSPI communication channel contexts. The MCSPI initiates a data transfer on the data lines (SPIDAT[0] and SPIDAT[1]) and generates clock (SPICLK) and control (SPIEN[i]) signals.

Connected to multiple external devices, the MCSPI exchanges data with one MCSPI device at a time through two main modes (available in peripheral mode):

- Two-data-pins interface mode (transmit-and-receive mode for full-duplex transmission)
- Single-data-pin interface mode (recommended for half-duplex transmission)

Note

There is a fixed chip select line allocation in multichannel controller mode. Channel i is mapped to SPIEN[i].

Two DMA request events (read and write) allow synchronized accesses of the DMA controller with the activity of MCSPI.

Three interrupt events can be used for data transmission and reception in controller mode (for more information about interrupts, see Section 13.1.3.4.7.1, *Interrupt Events in Controller Mode*).

12.1.4.4.3.2 Controller Transmit-and-Receive Mode (Full Duplex)

In full-duplex transmission, data is transmitted (shifted out serially on SPIDAT[0]) and received (shifted in serially on SPIDAT[1]) simultaneously on separate data lines.

The controller transmit-and-receive mode is programmable per channel (the MCSPI_CHCONF_0/1/2/3[13-12] TRM bit field).

Channel access to the shift registers for transmission/reception is based on the MCSPI_TX_0/1/2/3 transmitter register state, the MCSPI_RX_0/1/2/3 receiver register state, and round-robin arbitration.

Channels that meet the following rules are included in the round-robin list of active channels scheduled for transmission and/or reception. The arbiter skips channels that do not meet the rules and searches in the rotation for the next enabled channel.

- Rule 1: Only enabled channels (the MCSPI_CHCTRL_0/1/2/3[0] EN bit) can be scheduled for transmission and/or reception.
- Rule 2: If its MCSPI_TX_0/1/2/3 transmitter register is not empty (the MCSPI_CHSTAT_0/1/2/3[1] TXS bit), an enabled channel can be scheduled when the shift register is assigned. If the MCSPI_TX_0/1/2/3 register is empty when the shift register is assigned, the TXx_UNDERFLOW event is activated, and the next enabled channel with new data to transmit is scheduled (see also transmit-only mode).
- Rule 3: An enabled channel can be scheduled if its receive register is not full (the MCSPI_CHSTAT_0/1/2/3[0] RXS bit) when the shift register is assigned (see also receive-only mode). Therefore, the MCSPI_RX_0/1/2/3 register cannot be overwritten. The MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set to this mode.

When MCSPI word transfer completes (the MCSPI_CHSTAT_0/1/2/3[2] EOT bit is set), the updated MCSPI_TX_0/1/2/3 register of the next scheduled channel is loaded into the shift register. The serialization (transmit-and-receive) starts depending on the channel communication configuration. When serialization completes, the received data transfers to the channel receive register.

The serial clock (SPICLK) synchronizes shifting and sampling of the information on the two serial data lines (SPIDAT[0] and SPIDAT[1]). Each time a bit transfers out from the controller, 1 bit transfers in from the peripheral.

Figure 12-51 shows an example of a full-duplex system with a controller device on the left and a peripheral device on the right. After eight cycles of the serial clock SPICLK, WordA transfers from the controller to the peripheral. At the same time, WordB transfers from the peripheral to the controller.

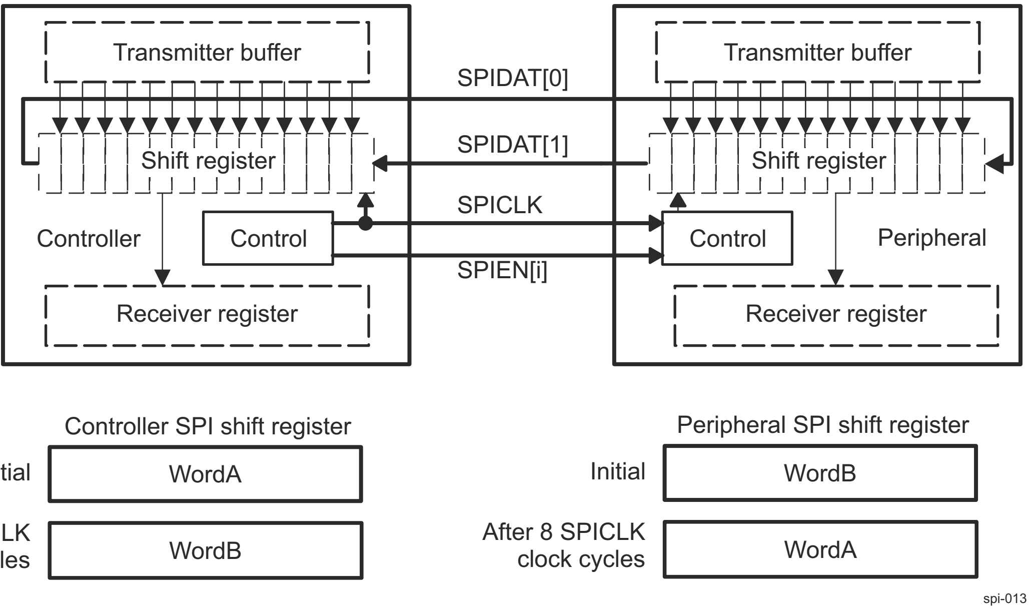

Figure 12-51. MCSPI Full-Duplex Transmission (Example)

12.1.4.4.3.3 Controller Transmit-Only Mode (Half Duplex)

The controller transmit-only mode prevents the processor from reading the MCSPI_RX_0/1/2/3 register (minimizing data movement) when only transmission is meaningful.

The controller transmit-only mode is programmable per channel (the MCSPI_CHCONF_0/1/2/3[13-12] TRM bit field). Transmission starts only after data is loaded into the MCSPI_TX_0/1/2/3 register.

Rule 1 and Rule 2, defined in Section 12.1.4.4.3.2 , apply in this mode.

Rule 3, defined in Section 12.1.4.4.3.2 , does not apply.

In controller transmit-only mode, the MCSPI_RX_0/1/2/3 register state FULL does not prevent transmission and the MCSPI_RX_0/1/2/3 register is always overwritten with the new MCSPI word. This event is not significant when only transmission is meaningful. Thus, the RX0_OVERFLOW bit in the MCSPI_IRQSTATUS register is never set in this mode.

The hardware automatically disables the RX_FULL interrupt and the DMA read requests.

The transfer status is given by the MCSPI_CHSTAT_0/1/2/3[2] EOT bit.

12.1.4.4.3.4 Controller Receive-Only Mode (Half Duplex)

The controller receive mode prevents the processor from refilling the MCSPI_TX_0/1/2/3 register (minimizing data movement) when only reception is meaningful.

The controller receive mode is programmable per channel (the MCSPI_CHCONF_0/1/2/3[13-12] TRM bit field).

The controller receive-only mode enables channel scheduling only on the empty state of the MCSPI_RX_0/1/2/3 register.

Rule 1 and Rule 3, defined in Section 12.1.4.4.3.2 , apply in this mode.

Rule 2, defined in Section 12.1.4.4.3.2 , does not apply.

In the controller receive-only mode, software must write dummy data to the MCSPI_TX_0/1/2/3 register. Only one dummy write is enough to receive any number of words from the peripheral. Software must ensure that the MCSPI_TX_0/1/2/3 register is always full (the TXx_EMPTY bits of MCSPI_IRQSTATUS) when receiving. The content of the MCSPI_TX_0/1/2/3 register is always loaded into the shift register when the shift register is assigned. After writing the dummy data to the MCSPI_TX_0/1/2/3 register, the TXx_EMPTY and TXx_UNDERFLOW bits in the MCSPI_IRQSTATUS register are never set in receive-only mode.

The MCSPI_CHSTAT_0/1/2/3[2] EOT bit gives the status of serialization. The RXx_FULL bits of the MCSPI_IRQSTATUS register are set when received data is loaded from the shift register to the corresponding MCSPI_RX_0/1/2/3 register. The MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

12.1.4.4.3.5 Single-Channel Controller Mode

When the MCSPI is configured as a controller device with a single enabled channel (MCSPI_MODULCTRL[2] MS = 0 and MCSPI_MODULCTRL[0] SINGLE = 1), the assertion of the SPIEN[i] signal is optional depending on device connected to the controller. In 3-pin mode (MCSPI_MODULCTRL[1] PIN34 = 1) the controller starts transmitting data when a write to the MCSPI_TX_0/1/2/3 register or the FIFO is performed. In 4-pin mode (MCSPI_MODULCTRL[1] PIN34 = 0) the assertion and de-assertion of SPIEN[i] is controlled by software using the MCSPI_CHCONF_0/1/2/3[20] FORCE bit.

12.1.4.4.3.5.1 Programming Tips When Switching to Another Channel

When a single channel is enabled and data transfer is ongoing:

- Wait for the MCSPI word transfer to complete (wait until the MCSPI_CHSTAT_0/1/2/3[2] EOT bit is set to 1) before disabling the current channel and enabling a different channel.
- Disable the current channel, and then enable the other channel.

12.1.4.4.3.5.2 Force SPIEN[i] Mode

Continuous transfers are allowed manually by keeping the SPIEN[i] signal active for successive MCSPI words transfer. Several sequences (configuration/enable/disable of the channel) can be run without deactivating the SPIEN[i] line. This mode is supported by all channels and any controller sequence can be used (transmit-receive, transmit-only, receive-only).

Keeping the SPIEN[i] active mode is supported when:

- A single channel is used (with the MCSPI_MODULCTRL[0] SINGLE bit set to 1).
- Transfer parameters are loaded in the configuration register of the appropriate channel (MCSPI_CHCONF_0/1/2/3).

  The state of the SPIEN[i] signal is programmable:
  - Writing 1 to the MCSPI_CHCONF_0/1/2/3[20] FORCE bit drives the SPIEN[i] line high when the MCSPI_CHCONF_0/1/2/3[6] EPOL bit is set to 0. SPIEN[i] is driven low when the MCSPI_CHCONF_0/1/2/3[6] EPOL bit is set to 1.
  - Writing 0 to the MCSPI_CHCONF_0/1/2/3[20] FORCE bit drives the SPIEN[i] line low when the MCSPI_CHCONF_0/1/2/3[6] EPOL bit is set to 0. SPIEN[i] is driven high when the MCSPI_CHCONF_0/1/2/3[6] EPOL bit is set to 1.
- A single channel is enabled (the MCSPI_CHCTRL_0/1/2/3[0] EN bit is set to 1). The first enabled channel activates the SPIEN[i] line.

When the channel is enabled, the SPIEN[i] signal activates with the programmed polarity. As in the multichannel controller mode, the transfer start depends on the status of the MCSPI_TX_0/1/2/3 register (the MCSPI_CHSTAT_0/1/2/3[1] TXS bit), the status of the MCSPI_RX_0/1/2/3 register (the MCSPI_CHSTAT_0/1/2/3[1] RXS bit), and the defined mode (the MCSPI_CHCONF_0/1/2/3[13-12] TRM bit field) of the channel enabled.

The MCSPI_CHSTAT_0/1/2/3[2] EOT bit gives the transfer status of each MCSPI word. The RXx_FULL bit in the MCSPI_IRQSTATUS register is set when received data is loaded from the shift register to the MCSPI_RX_0/1/2/3 register.

A change in the configuration parameters is propagated directly on the MCSPI interface. If the SPIEN[i] signal is activated, ensure that the configuration is changed only between MCSPI words to avoid corrupting the current transfer.

Note

To avoid data corruption, SPIEN[i] polarity and SPICLK phase and SPICLK polarity must not be modified when the SPIEN[i] signal is activated.

A delay between MCSPI words that requires the connected MCSPI peripheral device to switch from one configuration to another (for instance, from transmit-only to receive-only) must be handled by software.

At the end of the last MCSPI word, the channel must be deactivated (the MCSPI_CHCTRL_0/1/2/3[0] EN bit set to 0) and SPIEN[i] can be forced to its INACTIVE state using the MCSPI_CHCONF_0/1/2/3[20] FORCE bit.

Figure 12-52 and Figure 12-53 show successive transfers with SPIEN[i] maintained active low with a different configuration for each MCSPI word in single-data-pin and dual-data-pin interface modes, respectively.

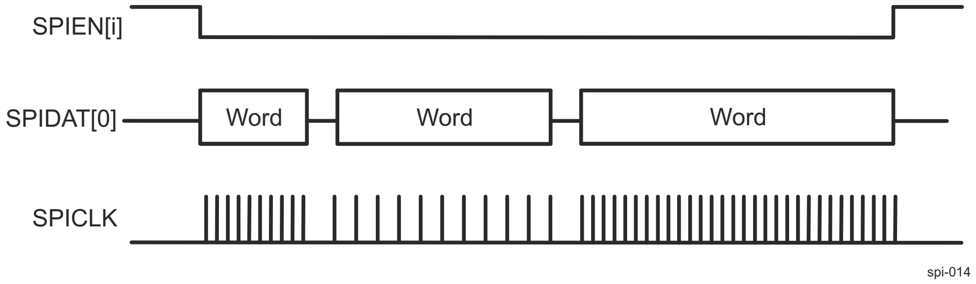

Figure 12-52. Continuous Transfers With SPIEN[i] Maintained Active (Single-Data-Pin Interface Mode)

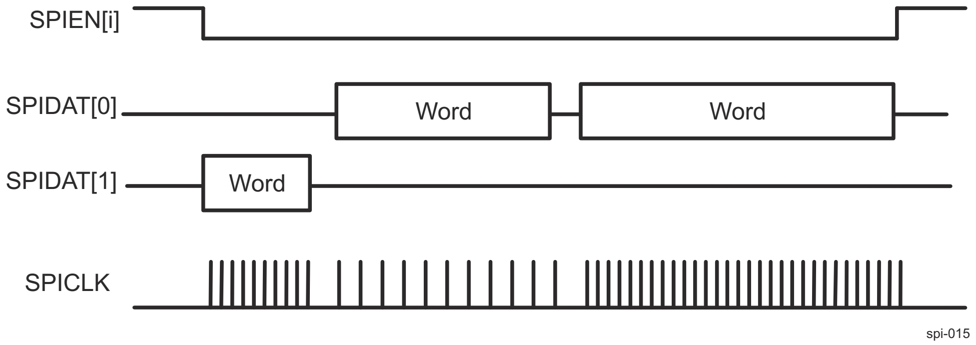

Figure 12-53. Continuous Transfers With SPIEN[i] Maintained Active (Dual-Data-Pin Interface Mode)

Note

The SPIEN[i] signal can be maintained active via software using the MCSPI_CHCONF_0/1/2/3[20] FORCE bit only when the MCSPI_MODULCTRL[0] SINGLE bit is set to 0x1.

12.1.4.4.3.5.3 Turbo Mode

Turbo mode improves the throughput of the MCSPI interface when a single channel is enabled by allowing transfers until the shift register and the MCSPI_RX_0/1/2/3 register are full. Turbo mode is time saving when a transfer exceeds two words. This mode is programmable per channel (through the MCSPI_CHCONF_0/1/2/3[9] TURBO bit).

When several channels are enabled, the TURBO bit has no effect and the channel access to the shift registers remains as previously described.

In turbo mode, Rule 1 and Rule 2 apply, but Rule 3 does not (see Section 12.1.4.4.3.2 , *Controller Transmit-and-Receive Mode (Full Duplex)*). An enabled channel can be scheduled if its receive register is full (the MCSPI_CHSTAT_0/1/2/3[0] RXS bit) when the shift-register is assigned until the shift register is full.

The MCSPI_RX_0/1/2/3 register cannot be overwritten in turbo mode. Consequently, the MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

12.1.4.4.3.6 Start-Bit Mode

In start-bit mode, an extended bit is added before the MCSPI word to indicate whether the next MCSPI word must be handled as a command or as data. This feature is available only in controller mode. Start-bit mode cannot be used at the same time as turbo mode and/or force SPIEN[i] mode. In this case, only one channel can be used; round-robin arbitration is not possible.

This mode is programmable per channel by setting the MCSPI_CHCONF_0/1/2/3[23] SBE bit to 1. The polarity of the extended bit is programmable per channel. When the MCSPI_CHCONF_0/1/2/3[24] SBPOL bit is set to 0, the MCSPI word must be handled as a command. When the MCSPI_CHCONF_0/1/2/3[24] SBPOL bit is set to 1, the MCSPI word must be handled as data. Moreover, start-bit polarity can be changed dynamically during start-bit transfer without disabling the channel for reconfiguration; in this case, users must configure the MCSPI_CHCONF_0/1/2/3[24] SBPOL bit before writing the MCSPI word to be transmitted to the TX register.

12.1.4.4.3.7 Chip-Select Timing Control

The chip-select (CS) timing control is available only in controller mode with automatic CS generation (the MCSPI_MODULCTRL[0] SINGLE bit set to 0) to add a programmable delay between CS assertion and first clock edge, or CS removal and last clock edge. This option is available only in 4-pin mode when MCSPI_MODULCTRL[1] PIN34 set to 0.

This mode is programmable per channel through the MCSPI_CHCONF_0/1/2/3[26-25] TCS0 bit field.

Figure 12-54 shows the CS SPIEN timing controls.

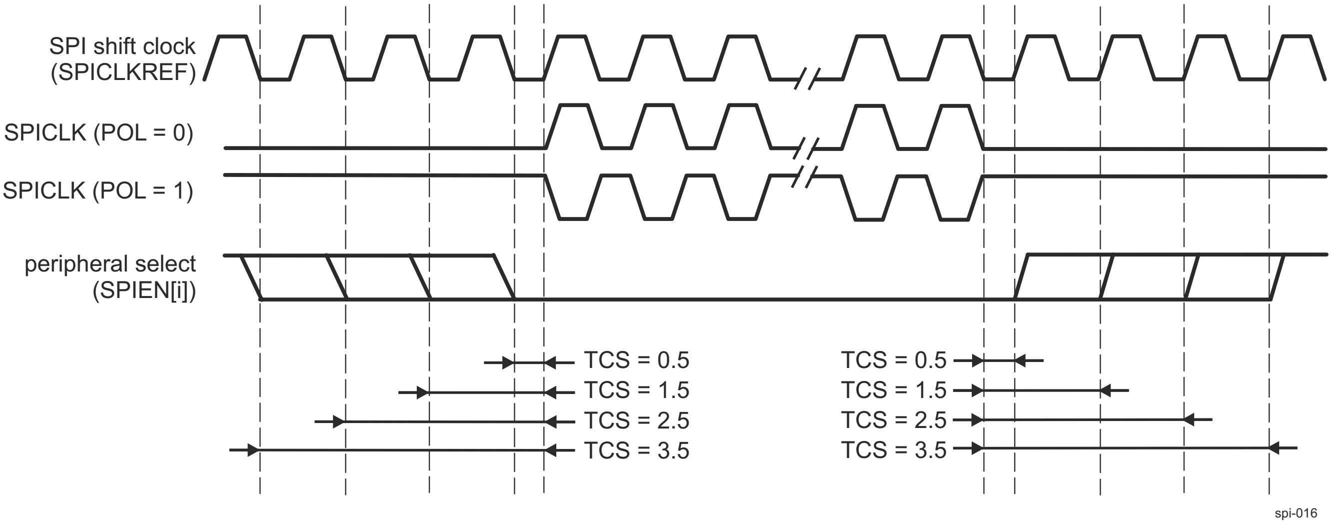

Figure 12-54. CS SPIEN Timing Controls

Note

Because of the design implementation for transfers using a clock divider ratio set to 1 (clock bypassed), a half cycle must be added to the value between CS assertion and the first clock edge with PHA = 1 or between CS removal and the last clock edge with PHA = 0.

12.1.4.4.3.8 Programmable MCSPI Clock (SPICLK)

In controller mode, the baud rate of the MCSPI serial clock is programmable.

An internal reference clock, SPICLKREF, is used as input of a programmable divider (the MCSPI_CHCONF_0/1/2/3[5-2] CLKD bit field) to generate the bit rate of the serial output clock SPICLK. Table 12-58 summarizes the supported divisor values.

Table 12-58. MCSPI Controller Clock Rates

Divider	Clock Rate
1	50 MHz(1)
2	25 MHz(1)
4	12.5 MHz
8	6.25 MHz
16	3.125 MHz
32	1.5625 MHz
64	781.25 kHz
128	390 kHz(2)
256	195 kHz(2)
512	97.7 kHz(2)
1024	48.8 kHz(2)
2048	24.4 kHz(2)
4096	12.2 kHz(2)
8192 and higher: Division not supported	–

(1) These frequencies are not necessarily supported by all MCSPI modules. For more information, see the *Timing Requirements and Switching Characteristics* chapter in the device-specific Data sheet.

(2) Approximate Frequency

12.1.4.4.3.8.1 Clock Ratio Granularity

By default, the clock division ratio is defined by the MCSPI_CHCONF_0/1/2/3[5-2] CLKD bit field with power-of-2 granularity leading to a clock division in the range 1 to 4096; in this case, the duty cycle is always 50 percent. With the MCSPI_CHCONF_0/1/2/3[29] CLKG bit, clock division granularity can be changed to one clock cycle; in that case the MCSPI_CHCTRL_0/1/2/3[15-8] EXTCLK bit field is concatenated with the MCSPI_CHCONF_0/1/2/3[5-2] CLKD bit field to give a 12-bit-wide division ratio in the range 1 to 4096.

When granularity is one clock cycle (the CLKG bit set to 1), for the odd value of the clock ratio, the clock high level lasts one clock cycle more than the low level, depending on the MCSPI_CHCONF_0/1/2/3[1] POL and MCSPI_CHCONF_0/1/2/3[0] PHA bits (see Table 12-59).

Table 12-59. CLKSPIO High/Low Time Computation

Clock Ratio F_{RATIO}	CLKSPIO High Time	CLKSPIO Low Time
1	T_{HIGH_REF}	T_{LOW_REF}
Even >= 2	T_ref * (F_{RATIO}/2)	T_ref * (F_{RATIO}/2)
Odd >= (POL = PHA)	T_ref * (F_{RATIO}– 1)/2	T_ref * (F_{RATIO} + 1)/2
Odd >= (POL =! PHA)	T_ref * (F_{RATIO}+ 1)/2	T_ref * (F_{RATIO} – 1)/2

Note

F_{RATIO} = SPICLK frequency (F_{OUT}) division ratio
T_{HIGH} = SPICLK high time period
T_{LOW} = SPICLK low time period
T_ref = MCSPI_FCLK period
T_{HIGH_REF} = MCSPI_FCLK high time period
T_{LOW_REF} = MCSPI_FCLK low time period

If the CLKG bit is set to 1; F_{RATIO} = EXTCLK concatenated with CLKD + 1.

For odd ratio values, the duty cycle is calculated as follows:

Duty_cycle = $(1 – 1/F_{RATIO})/2$

Table 12-60 shows examples of clock granularity with a clock source frequency of 50 MHz.

Table 12-60. Clock Granularity Examples

EXTCLK	CLKD	CLKG	F_{RATIO}	PHA	POL	T_{HIGH} (ns)	T_{LOW} (ns)	T_{PERIOD} (ns)	Duty Cycle	F_{OUT} (MHz)
X	0	0	1	X	X	10.0	10.0	20.0	50–50	50
X	1	0	2	X	X	20.0	20.0	40.0	50–50	25
X	2	0	4	X	X	40.0	40.0	80.0	50–50	12.5
X	3	0	8	X	X	80.0	80.0	160.0	50–50	6.2
0	0	1	1	X	X	10.0	10.0	20.0	50–50	50
0	1	1	2	X	X	20.0	20.0	40.0	50–50	25
0	2	1	3	1	0	40.0	20.0	60.0	66–33	16.6
0	2	1	3	1	1	20.0	40.0	60.0	33–66	16.6
0	3	1	4	X	X	40.0	40.0	80.0	50–50	12.5
5	0	1	81	1	0	820.0	800.0	1620.0	50.6–49.4	0.617
5	7	1	88	X	X	880.0	880.0	1760.0	50–50	0.568

12.1.4.4.4 MCSPI Peripheral Mode

To select the MCSPI peripheral mode, set the MCSPI_MODULCTRL[2] MS bit.

A MCSPI peripheral device can be connected to up to four external MCSPI controller devices but handles transactions with one MCSPI controller device at a time.

In peripheral mode, the MCSPI initiates data transfer on the data lines (SPIDAT[0] and SPIDAT[1]) when it is selected by an active control signal (SPIEN[i]) and receives an MCSPI clock (SPICLK) from the external MCSPI controller device. Only channel 0 can be configured as a peripheral but through the MCSPI_CHCONF_0[22-21] SPIENSLV bit field any of the SPIEN[i] signals can be used to select the MCSPI module. In peripheral mode and when the MCSPI_MODULCTRL[1] PIN34 is set to 0x0 (default behaviour), the MCSPI uses the edge of SPIEN[i] to detect word length. For this reason, SPIEN[i] must become inactive between each word.

When the MCSPI_MODULCTRL[1] PIN34 is set to 0x0, the MCSPI does not support SPIEN[i] active between MCSPI words. In this case, the MCSPI uses the edge to detect word length.

When the MCSPI_MODULCTRL[1] PIN34 is set to 0x1, a multiword transfer can be performed without needing the external MCSPI controller to deactivate SPIEN[i] between each word as in this case the MCSPI module works in 3-pin peripheral mode and SPIEN[i] is not needed.

12.1.4.4.4.1 Dedicated Resources

Only channel 0 can be enabled in peripheral mode.

Figure 12-55 shows an example of four peripherals wired on a single controller device.

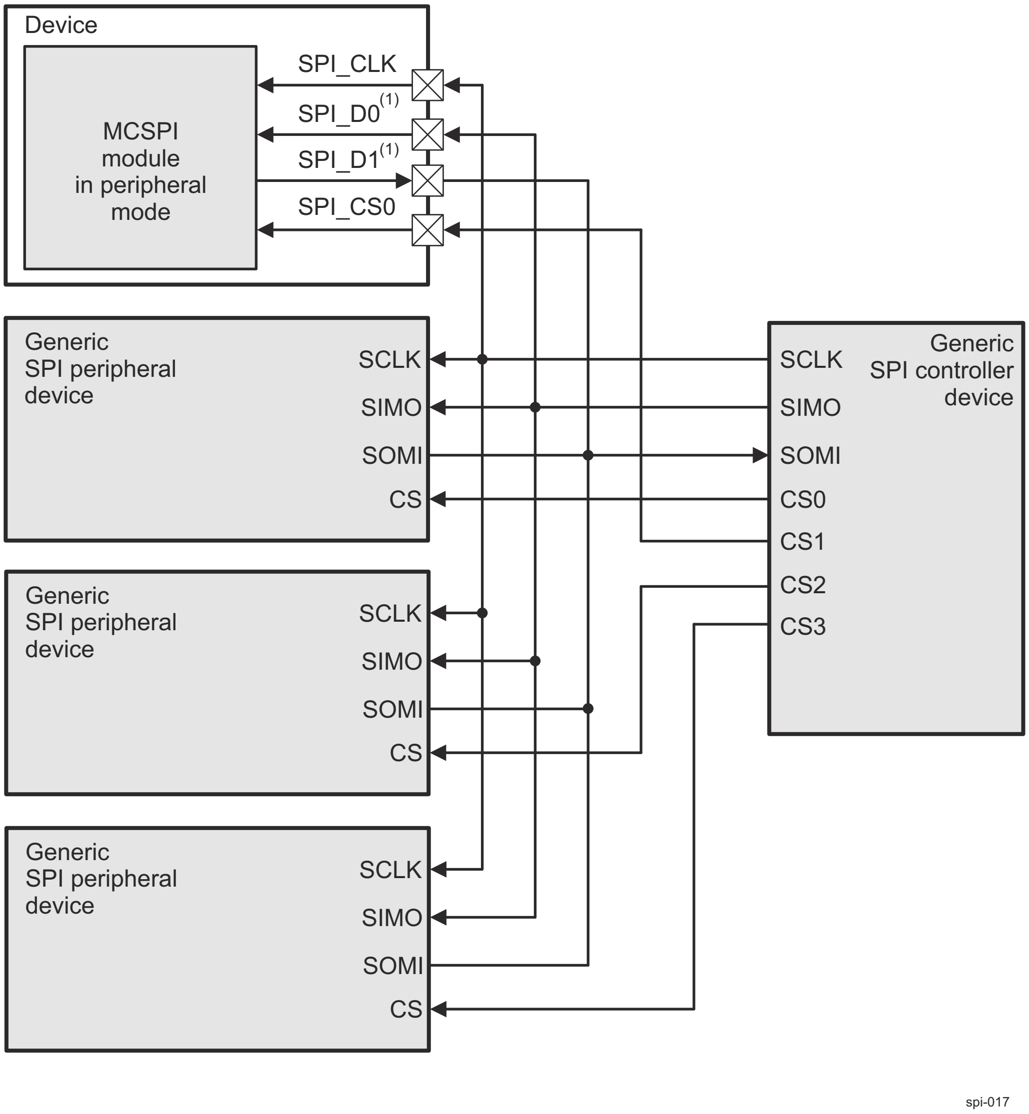

Note

Direction depends on MCSPI_CHCONF_0/1/2/3[16] DPE0, MCSPI_CHCONF_0/1/2/3[17] DPE1 and MCSPI_CHCONF_0/1/2/3[18] IS bits

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Figure 12-55. Example of MCSPI Peripheral With One Controller and Multiple Peripheral Devices on Channel 0

Channel 0 in peripheral mode has the following resources:

- Its own channel enable, programmable with the MCSPI_CHCTRL_0[0] EN bit. This channel must be enabled before transmission and reception.
- For this mode, the peripheral-select signal can be detected on any of the SPIEN[i] ports. This is programmable with the MCSPI_CHCONF_0[22-21] SPIENSLV bit field.
- Its own transmitter register, MCSPI_TX_0, on top of the common transmit shift register. If the MCSPI_TX_0 register is empty, the MCSPI_CHSTAT_0[1] TXS bit is set. If MCSPI is selected by an external controller (the active signal on the SPIEN[i] port assigned to channel 0), the MCSPI_TX_0 register content of channel 0 is always loaded into the shift register, whether its content is updated or not. The MCSPI_TX_0 register must be loaded before MCSPI is selected by a controller.

- Its own receiver register, MCSPI_RX_0, on top of the common receive shift register. If the MCSPI_RX_0 register is full, the MCSPI_CHSTAT_0[0] RXS bit is set.

Note

The MCSPI_TX_1/2/3 and MCSPI_RX_1/2/3 registers are not used. Reading from or writing to a channel register other than channel 0 has no effect.

- Its own communication configuration with the following parameters through the MCSPI_CHCONF_0:
  - Transmit and receive modes, programmable with the TRM field
  - Interface mode (two data pins or single data pin) and data pins assignment, both programmable with the IS and DPE bits. (The MCSPI modules are in peripheral mode after reset and must be properly configured for the modules to act in controller mode.)
  - MCSPI word length, programmable with the WL bit
  - SPIEN[i] polarity, programmable with the EPOL bit
  - SPICLK polarity, programmable with the POL bit
  - SPICLK phase, programmable with the PHA bit

  The SPICLK frequency of a transfer is controlled by the external MCSPI controller connected to the MCSPI peripheral device. The MCSPI_CHCONF_0[5-2] CLKD bit field is not used in peripheral mode.

Note

The configuration of the channel can be loaded in the MCSPI_CHCONF_0 only when the channel is disabled.

- Two DMA request events, read and write, synchronize read/write accesses of the DMA controller with the activity of MCSPI. DMA requests are asserted using the MCSPI_CHCONF_0[15] DMAR bit for reading and the MCSPI_CHCONF_0[14] DMAW bit for writing.
- Four interrupt events (see Section 12.1.4.4.7.2 , *Interrupt Events in Peripheral Mode*).

12.1.4.4.4.2 Peripheral Transmit-and-Receive Mode

The peripheral receive mode is programmable (set the MCSPI_CHCONF_0[13-12] TRM bit field to 0x0).

In peripheral transmit-and-receive mode, the MCSPI_TX_0 register must be loaded before MCSPI is selected by an external MCSPI controller device.

After a channel is enabled, transmission and reception proceed with interrupt and DMA request events.

The MCSPI_TX_0 register content is always loaded in the shift register whether it is updated or not. The event TX0_UNDERFLOW is activated accordingly and does not prevent transmission.

When the MCSPI word transfer completes (the MCSPI_CHSTAT_0[2] EOT bit is set to 1), the received data is transferred to the channel receive register.

To use MCSPI as a peripheral transmit-only device, the RX0_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the state of the MCSPI_RX_0 register (see Section 12.1.4.4.7.2 , *Interrupt Events in Peripheral Mode*).

12.1.4.4.4.3 Peripheral Transmit-Only Mode

The peripheral transmit-only mode is programmable (set the MCSPI_CHCONF_0[13-12] TRM bit field to 0x2) and avoids the requirement for the processor to read the MCSPI_RX_0 register (minimizing data movement) only when transmission is meaningful.

To use the MCSPI as a peripheral transmit-only device, the RX0_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the state of the MCSPI_RX_0 register.

When the MCSPI word transfer completes, the MCSPI_CHSTAT_0[2] EOT bit is set.

Figure 12-56 shows a half-duplex system with a controller device on the left and a transmit-only peripheral device on the right. Each time a bit transfers out from the peripheral, 1 bit transfers in the controller. After eight cycles of the serial clock SPICLK, WordB transfers from the peripheral to the controller.

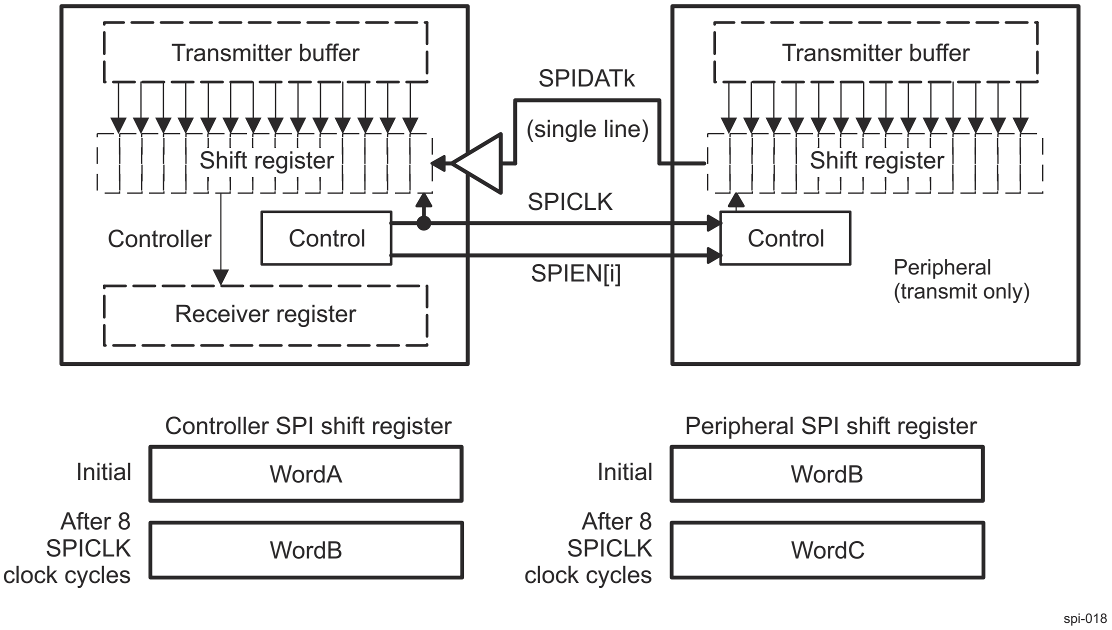

Note

k = 0 or 1 depending on MCSPI_CHCONF_0/1/2/3[16] DPE0, MCSPI_CHCONF_0/1/2/3[17] DPE1 and MCSPI_CHCONF_0/1/2/3[18] IS bits

Figure 12-56. MCSPI Half-Duplex Transmission (Transmit-Only peripheral)

12.1.4.4.4.4 Peripheral Receive-Only Mode

The peripheral receive mode is programmable (set the MCSPI_CHCONF_0[13-12] TRM bit field to 0x1).

In receive-only mode, the MCSPI_TX_0 register must be loaded before the MCSPI is selected by an external MCSPI controller device. The MCSPI_TX_0 register content is always loaded into the shift register whether it is updated or not. The TX0_UNDERFLOW event is activated accordingly and does not prevent transmission.

When the MCSPI word transfer completes (the MCSPI_CHSTAT_0[2] EOT bit is set to 1), the received data is transferred to the channel receive register.

To use the MCSPI as a peripheral receive-only device, the TX0_EMPTY and TX0_UNDERFLOW interrupts and the DMA write requests must be disabled due to the state of the MCSPI_TX_0 register.

For a full-duplex transmission, the serial clock (SPICLK) synchronizes shifting and sampling of the information on the two serial data lines. If SPICLK synchronizes on a single serial data line, the data line should be half-duplex.

Figure 12-57 shows a half-duplex system with a controller device on the left and a receive-only peripheral device on the right. Each time a bit transfers out from the controller, 1 bit transfers in from the peripheral. After eight cycles of the serial clock SPICLK, WordA transfers from the controller to the peripheral.

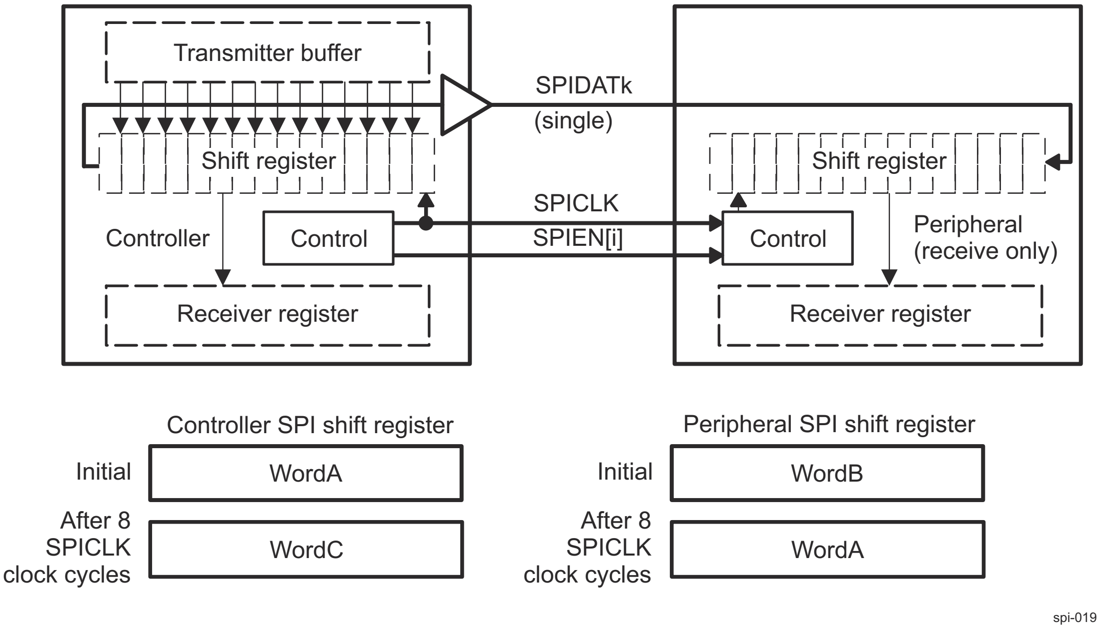

Note

k = 0 or 1 depending on MCSPI_CHCONF_0/1/2/3[16] DPE0, MCSPI_CHCONF_0/1/2/3[17] DPE1 and MCSPI_CHCONF_0/1/2/3[18] IS bits

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Figure 12-57. MCSPI Half-Duplex Transmission (Receive-Only Peripheral)

12.1.4.4.5 MCSPI 3-Pin or 4-Pin Mode

Depending on targeted application the MCSPI interface can be configured to use 3 or 4 pins through the MCSPI_MODULCTRL[1] PIN34 bit. If this bit is set to 0, MCSPI is in 4-pin mode using the SPICLK, SPIDAT[0], SPIDAT[1] and SPIEN[i] signals. If PIN34 is set to 1 the controller is in 3-pin mode and SPIEN[i] is not used. In this mode all options related to chip select management are useless (EPOL, FORCE and TCS0 bits of MCSPI_CHCONF_0/1/2/3). 3-pin and 4-pin operation applies to both controller and peripheral modes.

12.1.4.4.6 MCSPI FIFO Buffer Management

The MCSPI controller has a built-in 64-byte buffer to unload the DMA or interrupt handler and improve data throughput.

This buffer can be used by only one channel at a time and is selected by setting the MCSPI_CHCONF_0/1/2/3[28] FFER or MCSPI_CHCONF_0/1/2/3[27] FFEW bit to 1. If several channels are selected and several FIFO enable bit fields are set to 1, the controller forces the buffer not to be used; the driver must set only one FIFO enable bit field.

The buffer can be used in the following modes:

- Controller or peripheral mode
- Transmit-only, receive-only, or transmit-and-receive mode
- Single channel or turbo mode, or normal round-robin mode. In round-robin mode the buffer is used by only one channel.

Every word length (MCSPI_CHCONF_0/1/2/3[11-7] WL) is supported.

In transmit-and-receive mode, the buffer can be used in transmit (see Figure 12-58) or receive (see Figure 12-59) directions, or in both directions. If only one direction is chosen in transmit-and-receive mode, the full buffer is used for this direction. In both directions, the buffer is split into two halves, one for each direction (see Figure 12-60).

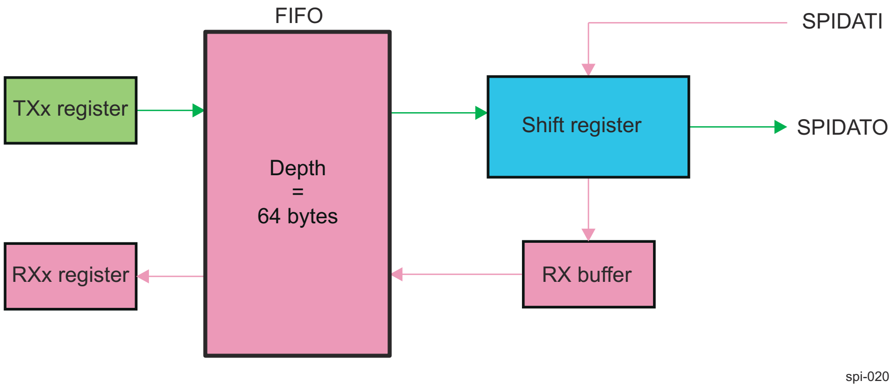

Figure 12-58. Buffer Used in Transmit Direction Only

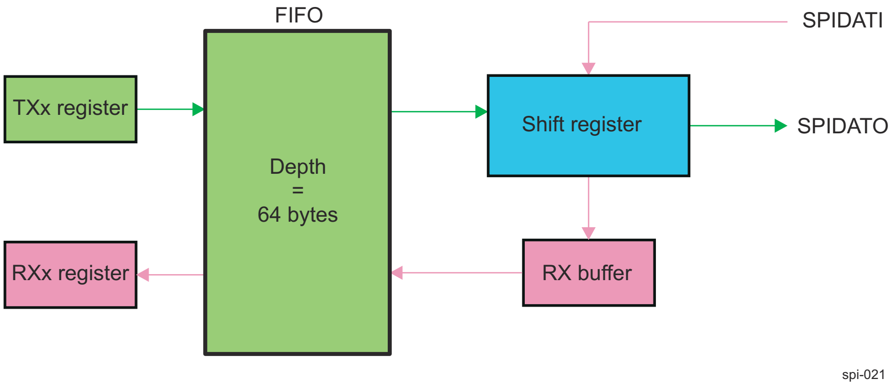

Figure 12-59. Buffer Used in Receive Direction Only

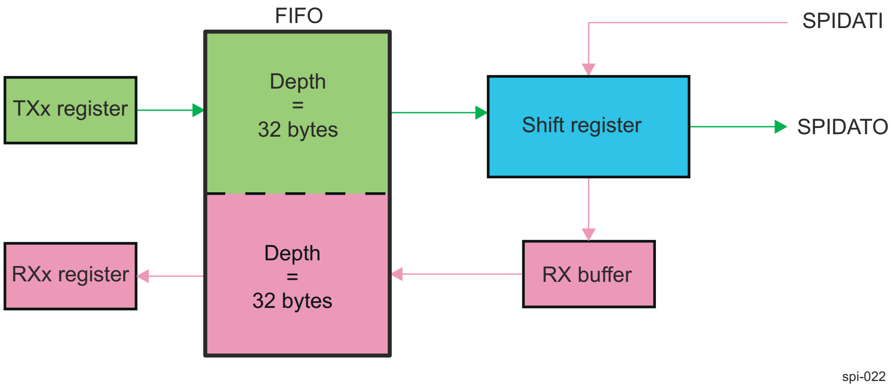

Figure 12-60. Buffer Used for Transmit and Receive Directions

Two levels (MCSPI_XFERLEVEL[5-0] AEL and MCSPI_XFERLEVEL[13-8] AFL) rule the buffer management. The granularity of these levels is 1 byte; it is not aligned with the MCSPI word length. The driver must set these values as a multiple of the MCSPI word length defined in WL. Table 12-61 lists the number of bytes written in the FIFO, depending on the word length.

Table 12-61. FIFO Writes, Word Length Relationship

	MCSPI Word Length (WL)		
	3 ≤ WL≤ 7	**8 ≤ WL ≤ 15**	**16 ≤ WL ≤ 31**
Number of bytes written in the FIFO	1 byte	2 bytes	4 bytes

The FIFO buffer pointers are reset when the corresponding channel is enabled or the FIFO configuration changes.

12.1.4.4.6.1 Buffer Almost Full

The MCSPI_XFERLEVEL[15-8] AFL bit field is needed when the buffer is used to receive an MCSPI word from a peripheral (the MCSPI_CHCONF_0/1/2/3[28] FFER bit must be set to 1). It defines the almost-full buffer status. See Figure 12-61.

When the FIFO pointer reaches this level, an interrupt or a DMA request is sent to the processor to enable the system to read AFL + 1 bytes from the receive register.

Note

AFL + 1 must correspond to a multiple value of the MCSPI_CHCONF_0/1/2/3[11-7] WL bit field.

When DMA is used, the request is de-asserted after the first receive register read.

No new request is asserted again as long as the system has not performed the correct number of read accesses.

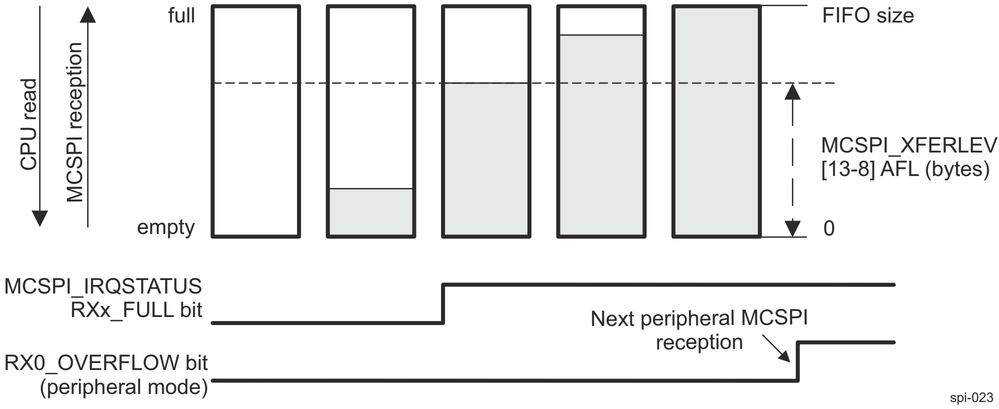

Figure 12-61. Buffer Almost Full Level (AFL)

Note

The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the request is asserted on the same conditions as the MCSPI_IRQSTATUS RXx_FULL flag.

12.1.4.4.6.2 Buffer Almost Empty

The MCSPI_XFERLEVEL[7-0] AEL bit field is needed when the buffer is used to transmit an MCSPI word to a peripheral (the MCSPI_CHCONF_0/1/2/3[27] FFEW bit must be set to 1). It defines the almost-empty buffer status. See Figure 12-62.

When the FIFO pointer does not reach this level, an interrupt or a DMA request is sent to the processor to enable the system to write AEL + 1 bytes to the transmit register.

Note

AEL + 1 must correspond to a multiple value of the MCSPI_CHCONF_0/1/2/3[11-7] WL bit field.

When DMA is used, the request is de-asserted after the first transmit register write.

No new request is asserted again as long as the system has not performed the correct number of write accesses.

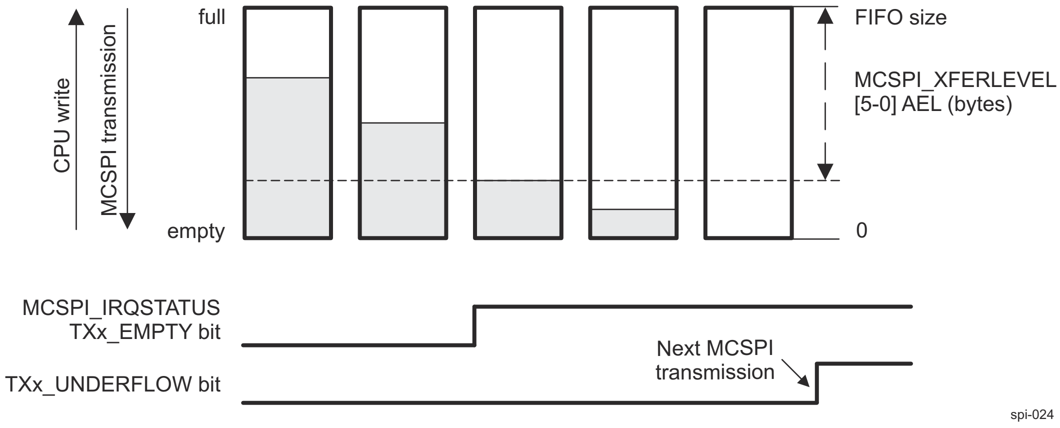

Figure 12-62. Buffer Almost Empty Level (AEL)

Note

The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the request is asserted on the same conditions as the MCSPI_IRQSTATUS TXx_EMPTY flag.

12.1.4.4.6.3 End of Transfer Management

When the FIFO buffer is enabled for a channel, the user must previously configure in the MCSPI_XFERLEVEL register the AEL and AFL levels and especially the MCSPI_XFERLEVEL[31-16] WCNT bit field to define the number of MCSPI words to be transferred using the FIFO before enabling the channel.

This counter lets the controller stop the transfer correctly after a defined number of MCSPI word transfers. If WNCT is set to 0x0000, the counter is not used and the user must stop the transfer manually by disabling the channel; in this case, the user does not know how many MCSPI transfers have been done. For received words, software must poll the MCSPI_CHSTAT_i[5] RXFFE bit and read the MCSPI_RX_0/1/2/3 receive register to empty the FIFO buffer.

When the end-of-word count interrupt is generated (the MCSPI_IRQSTATUS[17] EOW bit is set), the user can disable the channel and poll the MCSPI_CHSTAT_0/1/2/3[5] RXFFE bit to know the last MCSPI words in the FIFO buffer and read them.

12.1.4.4.6.4 Multiple MCSPI Word Access

The processor has the ability to perform multiple MCSPI word access to the receive or transmit registers within a single 32-bit interface access by setting the MCSPI_MODULCTRL[7] MOA to 1 under specific conditions:

- The channel selected has the FIFO enable.
- Only FIFO sense enabled support the kind of access.
- MCSPI_MODULCTRL[7] MOA is set to 1.
- Only 32-bit interface access and data width can be performed to receive or transmit registers, for other kind of access the processor must de-assert MCSPI_MODULCTRL[7] MOA bit.
- The level MCSPI_XFERLEVEL[7-0] AEL and MCSPI_XFERLEVEL[15-8] AFL must be 32-bit aligned, it means that AEL[0] = AEL[1] = 1 or AFL[0] = AFL[1] = 1.
- If MCSPI_XFERLEVEL[31-16] WCNT is used it must be configured according to MCSPI word length.
- The word length of MCSPI words allows to perform multiple MCSPI access, that means that MCSPI_CHCONF_0/1/2/3[11-7] WL is <16.

The number of MCSPI word access depends on MCSPI word length:

- 3 ≤ WL ≤ 7, MCSPI word length smaller or equal to byte length, 4 MCSPI words accessed per 32-bit interface read/write. If word count is used (MCSPI_XFERLEVEL[31-16] WCNT), set the bit field to WCNT[0] = WCNT[1] = 0.
- 8 ≤ WL ≤ 15, MCSPI word length greater than byte or equal to 16-bit length, 2 MCSPI words accessed per 32-bit interface read/write. If word count is used (MCSPI_XFERLEVEL[31-16] WCNT]), set the bit field to WCNT[0] = 0.
- 16 ≤ WL Multiple MCSPI word access is not applicable.

12.1.4.4.6.5 First MCSPI Word Delay

Figure 12-63 shows the MCSPI controller ability to delay the first MCSPI word transfer to give time for system to complete some parallel processes or fill the FIFO in order to improve transfer bandwidth. This delay is applied only on first MCSPI word after MCSPI channel enabled and first write in transmit register. It is based on output clock frequency.

This option is meaningful in controller mode and single channel mode asserted through MCSPI_MODULCTRL[0] SINGLE.

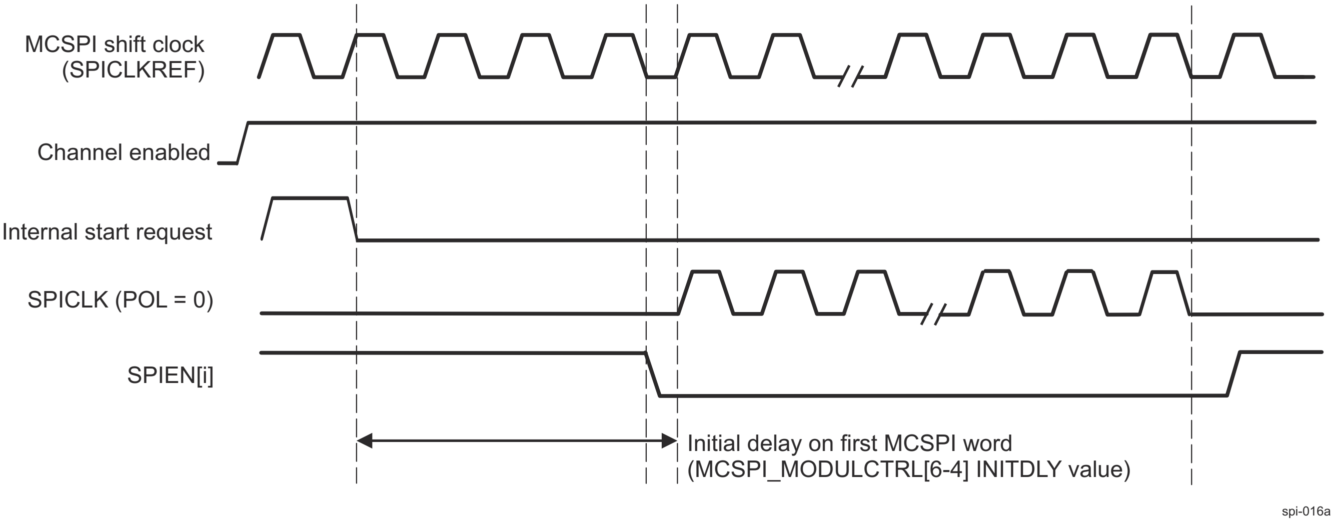

Figure 12-63. Controller Single Channel Initial Delay

Few delay values are available: No delay, 4/8/16/32 MCSPI cycles.

Its accuracy is half cycle in clock bypass mode and depends on clock polarity and phase.

12.1.4.4.7 MCSPI Interrupts

Each channel can issue interrupt events.

Each interrupt event has status bits in the MCSPI_IRQSTATUS register (RXx_FULL, TXx_UNDERFLOW, TXx_EMPTY, etc.) (where x = 0, 3) that indicate whether service is required. Each status bit has an interrupt enable bit (a mask) in the MCSPI_IRQENABLE register (RXx_FULL_ENABLE, TXx_UNDERFLOW_ENABLE, TXx_EMPTY_ENABLE, etc.).

When an interrupt occurs and a mask is later applied on it, the interrupt line is not asserted again, even if the interrupt source is not serviced.

The MCSPI supports interrupt-driven and polling operations.

12.1.4.4.7.1 Interrupt Events in Controller Mode

In controller mode, the interrupt events related to the state of the MCSPI_TX_0/1/2/3 register are TXx_EMPTY and TXx_UNDERFLOW. The interrupt event related to the state of the MCSPI_RX_0/1/2/3 register is RXx_FULL.

12.1.4.4.7.1.1 TXx_EMPTY

The TXx_EMPTY event is activated when a channel is enabled and its MCSPI_TX_0/1/2/3 register is empty (transient event). Enabling a channel automatically triggers this event, except in controller receive-only mode (see Section 12.1.4.4.3.4 , *Controller Receive-Only Mode*). When the FIFO buffer is enabled (the MCSPI_CHCONF_0/1/2/3[27] FFEW bit is set to 1), the MCSPI_IRQSTATUS TXx_EMPTY bit is set as soon as there is enough space in the buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5-0] AEL bit field.

The MCSPI_TX_0/1/2/3 register must be loaded with data to remove the source of the interrupt; the MCSPI_IRQSTATUS TXx_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXx_EMPTY event is asserted as long as the processor has not performed the number of writes into the MCSPI_TX_0/1/2/3 register defined by the MCSPI_XFERLEVEL[5-0] AEL bit field. The processor must perform the correct number of writes.

12.1.4.4.7.1.2 TXx_UNDERFLOW

The event TXx_UNDERFLOW is activated when the channel is enabled and if the MCSPI_TX_0/1/2/3 register or the FIFO is empty (not updated with new data) when an external controller device starts a data transfer with the MCSPI (transmit and receive).

The TXx_UNDERFLOW is a harmless warning in controller mode.

To avoid having a TXx_UNDERFLOW event at the beginning of a transmission, the TXx_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TX_0/1/2/3 register, because the channel is enabled. To avoid having a TXx_UNDERFLOW event, the MCSPI_TX_0/1/2/3 register must seldom be loaded.

The MCSPI_IRQSTATUS TXx_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.1.4.4.7.1.3 RXx_ FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RX_0/1/2/3 register becomes filled (transient event). When the FIFO buffer is enabled (the MCSPI_CHCONF_0/1/2/3[28] FFER bit is set to 1), RXx_ FULL is asserted as soon as the number of bytes held in the FIFO to be read reaches the MCSPI_XFERLEVEL[13-8] AFL threshold.

The MCSPI_RX_0/1/2/3 register must be read to remove the source of the interrupt; the MCSPI_IRQSTATUS RXx_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXx_FULL event is asserted as long as the processor has not performed AFL + 1 reads into MCSPI_RX_0/1/2/3. The processor must perform the correct number of reads.

12.1.4.4.7.1.4 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31-16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the MCSPI transfer is halted on the channel using the FIFO buffer as soon as MCSPI_XFERLEVEL[31-16] WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.1.4.4.7.2 Interrupt Events in Peripheral Mode

In peripheral mode, the interrupt events related to the state of the MCSPI_TX_0/1/2/3 register are TX0_EMPTY and TX0_UNDERFLOW. The interrupt events related to the state of the MCSPI_RX_0/1/2/3 are RX0_FULL and RX0_OVERFLOW (channels 1, 2, and 3 do not have a receiver overflow status bit). See the MCSPI_IRQSTATUS register.

12.1.4.4.7.2.1 TXx_EMPTY

The TXx_EMPTY event is activated when a channel is enabled and its MCSPI_TX_0/1/2/3 register is empty. Enabling the channel automatically raises this event. If the FIFO buffer is enabled (the MCSPI_CHCONF_0/1/2/3[27] FFEW bit is set to 1), the TXx_EMPTY event is asserted as soon as there is enough space in buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5-0] AEL bit field.

The MCSPI_TX_0/1/2/3 register must be loaded with data to remove the source of the interrupt; the MCSPI_IRQSTATUS TXx_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXx_EMPTY event is asserted as long as the processor has not performed the number of writes into the MCSPI_TX_0/1/2/3 register defined by MCSPI_XFERLEVEL[5-0] AEL bit field. The processor must perform the correct number of writes.

12.1.4.4.7.2.2 TXx_UNDERFLOW

The TXx_UNDERFLOW event is activated when a channel is enabled and if the MCSPI_TX_0/1/2/3 register is empty (not updated with new data) when an external controller device starts a data transfer with the MCSPI (transmit and receive).

When FIFO is enabled, the data emitted while the underflow event is raised is not the last data written in the FIFO but the old data in the FIFO (an old transmitted value or a dummy data in the FIFO has been reset).

TXx_UNDERFLOW indicates an error (data loss) in peripheral mode.

To avoid having a TXx_UNDERFLOW event at the beginning of a transmission, the TXx_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TX_0/1/2/3 register because the channel is enabled.

The MCSPI_IRQSTATUS TXx_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.1.4.4.7.2.3 RXx_FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RX_0/1/2/3 register is being filled (transient event). When the FIFO buffer is enabled (the MCSPI_CHCONF_0/1/2/3[28] FFER bit is set to 1), RXx_FULL is asserted as soon as the number of bytes held in the buffer to read defined by the MCSPI_XFERLEVEL[13-8] AFL bit field.

The MCSPI_RX_0/1/2/3 register must be read to remove the source of the interrupt; the MCSPI_IRQSTATUS RXx_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXx_FULL event is asserted as long as the processor has not performed AFL + 1 reads into MCSPI_RX_0/1/2/3. The processor must perform the correct number of reads.

12.1.4.4.7.2.4 RX0_OVERFLOW

The RX0_OVERFLOW event is activated in peripheral mode in transmit-and-receive mode or receive-only mode when a channel is enabled and the MCSPI_RX_0/1/2/3 register or FIFO is full when a new MCSPI word is received. The MCSPI_RX_0/1/2/3 register is always overwritten with the new MCSPI word. If the FIFO is enabled, data within the FIFO are overwritten; it must be considered as corrupted. The RX0_OVERFLOW event should not appear in peripheral mode using the FIFO.

The RX0_OVERFLOW event indicates an error (data loss) in peripheral mode.

The MCSPI_IRQSTATUS[3] RX0_OVERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.1.4.4.7.2.5 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31-16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the MCSPI transfer is halted on the channel using the FIFO buffer as soon as WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.1.4.4.7.3 Interrupt-Driven Operation

An interrupt enable bit in the MCSPI_IRQENABLE register can be set to enable each event to generate interrupt requests when the corresponding event occurs. Status bits are automatically set by hardware logic conditions.

When an event occurs (the single interrupt line is asserted), the processor must:

1. Read the MCSPI_IRQSTATUS register to identify which event occurred.
2. Read the MCSPI_RX_0/1/2/3 register that corresponds to the event to remove the source of an RXx_FULL event or write into the MCSPI_TX_0/1/2/3 register that corresponds to the event to remove the source of a TXx_EMPTY event. No action is required to remove the source of the TXx_ UNDERFLOW and RX0_OVERFLOW events.
3. Set the corresponding bit of the MCSPI_IRQSTATUS register to 1 to clear an interrupt status and then release the interrupt line.

The interrupt status bit must always be reset after channel enabling and before events are enabled as interrupt sources.

12.1.4.4.7.4 Polling

When the interrupt capability of an event is disabled in the MCSPI_IRQENABLE register, the interrupt line is not asserted, but the status bits in the MCSPI_IRQSTATUS register can be polled by software to detect when the corresponding event occurs.

Once the expected event occurs:

- RXx_FULL: To remove the source of the event, the processor must read the corresponding MCSPI_RX_0/1/2/3 register.
- TXx_EMPTY: To remove the source of the event, the processor must write into the corresponding MCSPI_TX_0/1/2/3 register.
- TXx_UNDERFLOW and RX0_OVERFLOW: No action is required to remove the source of the event.

To clear an interrupt, set the corresponding status bit of the MCSPI_IRQSTATUS register to 1. This does not affect the interrupt line state.

12.1.4.4.8 MCSPI DMA Requests

Each MCSPI channel, if enabled, can issue DMA requests. There are two DMA request lines per MCSPI channel (one for read and one for write).

The DMA read request line is asserted when the MCSPI channel is enabled and new data is available in the receive register of the MCSPI channel. A DMA read request can be individually masked with the MCSPI_CHCONF_0/1/2/3[15] DMAR bit. The DMA read request line is de-asserted when reading of the MCSPI_RX_0/1/2/3 register of the MCSPI channel completes.

The DMA write request line is asserted when the MCSPI channel is enabled and the MCSPI_TX_0/1/2/3 register of the MCSPI channel is empty. A DMA write request can be individually masked with the MCSPI_CHCONF_0/1/2/3[14] DMAW bit. The DMA write request line is de-asserted when loading of the MCSPI_TX_0/1/2/3 register of the channel completes.

12.1.4.4.9 MCSPI Power Saving Management

Power consumption can be optimized by switching off internal clocks (interface and functional clock) when there is no activity.

12.1.4.4.9.1 Normal Mode

In normal mode, internal MCSPI module clocks are automatically switched off (autogated) when there is no activity in peripheral or controller mode.

Autogating of the module interface clock and functional clock occurs when the following conditions are met:

- The MCSPI_SYSCONFIG[0] AUTOIDLE bit is set.
- In controller mode, there is no data to transmit or receive in all channels.
- In peripheral mode, the MCSPI is not selected by the external controller and there are no register accesses.

Autogating of the module interface clock and functional clock stops when the following conditions are met:

- In controller mode, an internal access occurs.
- In peripheral mode, an internal access occurs or the MCSPI is selected by the external controller.

12.1.4.4.9.2 Idle Mode

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

At the power management level, when all conditions to shut off the MCSPI_FCLK or MCSPI_ICLK clocks are met, the corresponding LPSC asserts a clock stop request to the MCSPI. Although this procedure is completely hardware-oriented and out of software control, the method in which the MCSPI module acknowledges the clock stop request can be configured through the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field.

The settings of the SIDLEMODE bit field and the related acknowledgement modes are:

- Force-idle mode (the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field is set to 0x0): The MCSPI module acknowledges unconditionally the clock stop request, regardless of its internal operations. This mode must be used carefully in this case because it does not prevent the loss of data when the clock is switched off.
- No-idle mode (the SIDLEMODE bit field is set to 0x1): The MCSPI never acknowledges the clock stop request and is safe from a module point of view because it ensures that the clocks remain active. However, it is not efficient to save power because it does not allow shut off of MCSPI_FCLK and MCSPI_ICLK.
- Smart-idle mode (the SIDLEMODE bit field is set to 0x2): The MCSPI acknowledges the clock stop request, depending on its internal activity. MCSPI acknowledges the shut off of MCSPI_FCLK and MCSPI_ICLK only when all pending transactions, IRQs, or DMA requests are treated. This is the best approach for efficient system power management.

When configured in smart-idle mode, the MCSPI also offers an additional feature to control gating of MCSPI_FCLK or MCSPI_ICLK. The MCSPI_SYSCONFIG[9-8] CLOCKACTIVITY bit field determines which clock shuts down (MCSPI_FCLK, MCSPI_ICLK, neither clock, or both clocks).

The setting of the CLOCKACTIVITY bit field is used internally to the MCSPI to determine on which part of the module the conditions to acknowledge the clock stop request are tested. For example, if MCSPI_FCLK is not shut off on clock stop request, the MCSPI considers only MCSPI_ICLK and the associated pending activities before acknowledging the request.

Some MCSPI features are associated with MCSPI_ICLK and others with MCSPI_FCLK. Using the CLOCKACTIVITY bit field with the smart-idle mode ensures that the features associated with the clock that remains active are always enabled, even if MCSPI acknowledges the clock stop request.

12.1.4.4.9.2.1 Force-Idle Mode

Force-idle mode is enabled and exited as follows:

- Force-idle mode is enabled when the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field is set to 0x0.
  - In force-idle mode, the MCSPI responds unconditionally to the clock stop request by de-asserting unconditionally the interrupt and DMA request lines, if asserted.
  - The transition from normal mode to idle mode does not affect the interrupt event bits of the MCSPI_IRQSTATUS register.
  - In force-idle mode, because the module must be disabled, the interrupt and DMA request lines are likely de-asserted. The interface clock and MCSPI clock provided to the MCSPI can be switched off.
  - A clock stop request during an MCSPI data transfer can lead to an unexpected and unpredictable result. Software must avoid such a request.

12.1.4.5 MCSPI Programming Guide

This section describes the low-level hardware programming sequences for the configuration and use of the MCSPI module.

12.1.4.5.1 MCSPI Global Initialization

12.1.4.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the MCSPI module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MCSPI. For further information, see *MCSPI Integration* and *MCSPI Environment*.

Table 12-62 lists the information on the global initialization of the surrounding modules.

Table 12-62. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
COMPUTE_CLUSTER0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling COMPUTE_CLUSTER0 interrupts, see *Interrupts*.
MCU_M4FSS0_CORE0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MCU_M4FSS0_CORE0 interrupts, see *Interrupts*.
R5FSS0/1_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS0/1_CORE0/1 interrupts, see *Interrupts*.
PRU_ICSSG0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling PRU_ICSSG0 and PRU_ICSSG1 interrupts, see *Interrupts*.
PDMA0 and PDMA1	Device INTCs must be configured to enable the interrupt request generation.
MCU_PLLCTRL0 and PLLCTRL0	PLL controller's configuration must be done to enable the module clocks. For more information, see Section 5.4 , *Clocking*.

12.1.4.5.1.2 MCSPI Global Initialization

12.1.4.5.1.2.1 Main Sequence – MCSPI Global Initialization

The procedure in Table 12-63 can be used to initialize MCSPI when performing software reset.

Table 12-63. MCSPI Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	MCSPI_SYSCONFIG[1] SOFTRESET	1
Wait until reset is finished?	MCSPI_SYSSTATUS[0] RESETDONE	=1
Configure static settings (such as SPI controller or peripheral) as required.	MCSPI_MODULCTRL[8-0]	0x-
Write MCSPI_SYSCONFIG	MCSPI_SYSCONFIG	0x-

12.1.4.5.2 MCSPI Operational Mode Configuration

12.1.4.5.2.1 MCSPI Operational Modes

The selection of the working mode is done with the MCSPI_CHCONF_0/1/2/3 register.

Table 12-64. MCSPI Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set receive mode for the channel.	MCSPI_CHCONF_0/1/2/3[13-12] TRM	0x1
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CHCONF_0/1/2/3	0x-
Reset the status bits.	MCSPI_IRQSTATUS	0x0

Table 12-65. MCSPI Transmit Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit mode for the channel.	MCSPI_CHCONF_0/1/2/3[13-12] TRM	0x2

Table 12-65. MCSPI Transmit Mode Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CHCONF_0/1/2/3	0x-
Reset the status bits.	MCSPI_IRQSTATUS	0x0

Table 12-66. MCSPI Transmit-and-Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit and receive mode for the channel.	MCSPI_CHCONF_0/1/2/3[13-12] TRM	0x0
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CHCONF_0/1/2/3	0x-
Reset the status bits.	MCSPI_IRQSTATUS	0x0

12.1.4.5.2.1.1 Common Transfer Sequence

MCSPI module allows the transfer of one or several words, according to different modes:

- CONTROLLER Normal, CONTROLLER Turbo, PERIPHERAL
- TRANSMIT–RECEIVE, TRANSMIT-ONLY, RECEIVE-ONLY
- Write and Read requests: Interrupts, DMA
- SPIEN[i] lines assertion/deassertion: automatic, manual

For all these sequences, the host process contains the main process and the interrupt routines.

The interrupt routines are called on the interrupt signals or by an internal call if the module is used in polling mode.

Table 12-67 represents the main sequence which is common to all transfers.

In multi-channel controller mode, the sequences of different channels can be run simultaneously.

Table 12-67. Common Transfer Sequence (Main Process)

Step	Register/Bit Field/Programming Model	Value
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
Write MCSPI_IRQENABLE to enable interrupts	MCSPI_IRQENABLE	0x-
Write MCSPI_CHCONF_0/1/2/3 to configure the channel	MCSPI_CHCONF_0/1/2/3	0x-
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait for the first write request (TX empty or DMA write)		
Write the transmitter register with data	MCSPI_TX_0/1/2/3	0x-
Wait for the host event for end of transfer		
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0

12.1.4.5.2.1.2 End of Transfer Sequences

The end of transfer depends on the transfer mode. Table 12-68 summarizes the type of end of transfer per transfer mode and gives a reference to the appropriate section for details.

Table 12-68. End of Transfer Sequences

		TRANSMIT-AND-RECEIVE		TRANSMIT-ONLY		RECEIVE-ONLY	
		INTERRUPT	DMA	INTERRUPT	DMA	INTERRUPT	DMA
CONTROLLER Normal	End of transfer sequence	See Section 12.1.4.5.2.1.3		See Section 12.1.4.5.2.1.4.1	See Section 12.1.4.5.2.1.4.2	See Section 12.1.4.5.2.1.5.1	See Section 12.1.4.5.2.1.5.2
	Minimum number of word	1	1	1	1	1	2
	DMA transfer size		N		N		N-1

Table 12-68. End of Transfer Sequences (continued)

		TRANSMIT-AND-RECEIVE		TRANSMIT-ONLY		RECEIVE-ONLY	
		INTERRUPT	**DMA**	**INTERRUPT**	**DMA**	**INTERRUPT**	**DMA**
CONTROLLER Turbo	End of transfer sequence	See Section 12.1.4.5.2.1.3		See Section 12.1.4.5.2.1.4.1	See Section 12.1.4.5.2.1.4.2	See Section 12.1.4.5.2.1.6.1	See Section 12.1.4.5.2.1.6.2
	Minimum number of word	1	1	1	1	2	3
	DMA transfer size		N		N		N-2
PERIPHERAL	End of transfer sequence	See Section 12.1.4.5.2.1.3		See Section 12.1.4.5.2.1.4.1	See Section 12.1.4.5.2.1.4.2	See Section 12.1.4.5.2.1.7	
	Minimum number of word	1	1	1	1	1	1
	DMA transfer size		N		N	N	N

The transfer to execute has a size of N words.

The different sequences can be merged in one process to manage transfers of several types. The end of transfer sequences are described from the start of the channel.

In these sequences, some soft variables are used:

- write_count = 0
- read_count = 0
- channel_enable = FALSE
- last_transfer = FALSE
- last_request = FALSE

They are initialized before starting the channel.

12.1.4.5.2.1.3 Transmit-and-Receive (Controller and Peripheral)

If the requests are configured in DMA, write_count and read_count are assigned with 'N' when the DMA handlers have completed their 'N' CBASS0 accesses.

Table 12-69. Transmit-and-Receive (Controller and Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait for write_count = N **AND** read_count = N		
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0

Table 12-70. Transmit-and-Receive (Controller and Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXx_EMPTY		
Write the transmitter register with data	MCSPI_TX_0/1/2/3	0x-
Increment write_count +1		
IF: RXx_FULL		
Read the receiver register	MCSPI_RX_0/1/2/3	
Increment read_count +1		
ENDIF		

12.1.4.5.2.1.4 Transmit-Only (Controller and Peripheral)

12.1.4.5.2.1.4.1 Based on Interrupt Requests

Table 12-71. Transmit-Only With Interrupts (Controller and Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait until last transfer = TRUE		
Wait for end of transfer	MCSPI_CHSTAT_0/1/2/3[2] EOT	=1
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0

Table 12-72. Transmit-Only With Interrupts (Controller and Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXx_EMPTY **AND** write_count < N		
Write the transmitter register with data	MCSPI_TX_0/1/2/3	0x-
Increment write_count +1		
ELSEIF: write_count ≥ N		
last_transfer = TRUE		
ENDIF		

12.1.4.5.2.1.4.2 Based on DMA Write Requests

When the DMA handler has completed its ‘N’ CBASS0 accesses, write_count is assigned with ‘N’.

Table 12-73. Transmit-Only With DMA (Controller and Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait until write_count = N		
Disable DMA write request	MCSPI_CHCONF_0/1/2/3[14] DMAW	0
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CHSTAT_0/1/2/3[2] EOT	=1
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0

Table 12-74. Transmit-Only With DMA (Controller and Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXx_EMPTY **AND** write_count = N		
last_transfer = TRUE		
ENDIF		

12.1.4.5.2.1.5 Controller Normal Receive-Only

12.1.4.5.2.1.5.1 Based on Interrupt Requests

Table 12-75. Receive-Only With Interrupt (Controller Normal) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait until last_request = TRUE		
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0
Read the receiver register	MCSPI_RX_0/1/2/3	0x-

Table 12-75. Receive-Only With Interrupt (Controller Normal) (Main Process) (continued)

Step	Register/Bit Field/Programming Model	Value
Increment read_count +1		

Table 12-76. Receive-Only With Interrupt (Controller Normal) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXx_FULL **AND** read_count = N - 1		
last_request = TRUE		
ELSEIF: read_count ≠ N - 1		
Read the receiver register	MCSPI_RX_0/1/2/3	0x-
Increment read_count +1		
ENDIF		

12.1.4.5.2.1.5.2 Based on DMA Read Requests

When the DMA handler has completed its ‘N-1’ CBASS0 accesses, read_count is assigned with ‘N-1’.

Table 12-77. Receive-Only With DMA (Controller Normal) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait until read_count = N - 1		
Disable DMA read request	MCSPI_CHCONF_0/1/2/3[15] DMAR	0
Wait until last_transfer = TRUE		
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0
Read the receiver register	MCSPI_RX_0/1/2/3	0x-
Increment read_count +1		

Table 12-78. Receive-Only With DMA (Controller Normal) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXx_FULL **AND** read_count = N-1		
last_transfer = TRUE		
ENDIF		

12.1.4.5.2.1.6 Controller Turbo Receive-Only

12.1.4.5.2.1.6.1 Based on Interrupt Requests

Table 12-79. Receive-Only With Interrupt (Controller Turbo) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait until channel_enable = TRUE		
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CHSTAT_0/1/2/3[2] EOT	=1
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0
Wait until channel_enable = FALSE		

Table 12-80. Receive-Only With Interrupt (Controller Turbo) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXx_FULL		
IF: read_count = N - 2		
last_transfer = TRUE		
channel_enable = FALSE		
ENDIF		
IF: read_count < N		
Read the receiver register	MCSPI_RX_0/1/2/3	0x-
Increment read_count +1		
ENDIF		
ENDIF		

12.1.4.5.2.1.6.2 Based on DMA Read Requests

When the DMA handler has completed its ‘N-2’ CBASS0 accesses read_count is assigned with ‘N-2‘.

Table 12-81. Receive-Only With DMA (Controller Turbo) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait until channel_enable = TRUE		
Wait until read_count = N-2		
Disable DMA read request	MCSPI_CHCONF_0/1/2/3[15] DMAR	0
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CHSTAT_0/1/2/3[2] EOT	=1
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0
Wait until channel_enable = FALSE		

Table 12-82. Receive-Only With DMA (Controller Turbo) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXx_FULL		
IF: read_count = N - 2		
last_transfer = TRUE		
channel_enable = FALSE		
ENDIF		
IF: read_count < N		
Read the receiver register	MCSPI_RX_0/1/2/3	0x-
Increment read_count +1		
ENDIF		
ENDIF		

12.1.4.5.2.1.7 Peripheral Receive-Only

If the requests are configured in DMA, read_count is assigned with ‘N’ when the DMA handler has completed its ‘N‘ CBASS0 accesses.

Table 12-83. Receive-Only (Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait until read_count = N		
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0

Table 12-84. Receive-Only (Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXx_FULL		
Read the receiver register	MCSPI_RX_0/1/2/3	0x-
Increment read_count +1		
ENDIF		

12.1.4.5.2.1.8 Transfer Procedures With FIFO

These flows describe the transfer with FIFO.

The MCSPI module allows the transfer of one or several words, according to different modes:

- CONTROLLER Normal, CONTROLLER Turbo, PERIPHERAL
- TRANSMIT–RECEIVE, TRANSMIT-ONLY, RECEIVE-ONLY
- Write and Read requests: IRQ, DMA

For all these flows, the host process contains the main process and the interrupt routine. This routine is called on the IRQ signals or by an internal call if the module is used in polling mode.

For more information, see Section 12.1.4.4.6 , *MCSPI FIFO Buffer Management*.

Table 12-85. FIFO Mode Common Sequence (Controller) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS	1
Write MCSPI_IRQENABLE to enable interrupts	MCSPI_IRQENABLE	1
Write MCSPI_CHCONF_0/1/2/3 to configure the channel	MCSPI_CHCONF_0/1/2/3	0x-
Write MCSPI_XFERLEVEL	MCSPI_XFERLEVEL	0x-
Start the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	1
IF: Receive only		
Wait for the write request (TX empty or DMA write)		
Write for the transmitter register with data	MCSPI_TX_0/1/2/3	0x-
ENDIF		
Wait for the host event for end of transfer		
Stop the channel	MCSPI_CHCTRL_0/1/2/3[0] EN	0

12.1.4.5.2.1.8.1 Common Transfer Sequence in FIFO Mode

This flow describes the host sequence for a transfer of any type defined in Section 12.1.4.5.2.1.8 , *Transfer Procedures With FIFO*.

In multi-channel, only one channel can use the FIFO.

Before enabling the FIFO for a channel (MCSPI_CHCONF_0/1/2/3[28] FFER and MCSPI_CHCONF_0/1/2/3[27] FFEW bits), the host must check that the FIFO is not enabled for another channel, even if these channels are not used.

In transmit-and-receive mode, the FIFO can be enabled for write or read request only, without FIFO for the other request.

In Peripheral mode, the channel 0 only can be activated. The correct SPIEN line is chosen in MCSPI_CHCONF_0[22-21] SPIENSLV bits.

The MCSPI module can start the transfer only when the first write request has been released by writing the MCSPI_TX_0/1/2/3 register, even in receive-only mode (only one write request occurs in this case).

12.1.4.5.2.1.8.2 End of Transfer Sequences in FIFO Mode

Table 12-86 summarizes the type of end of transfer per transfer mode and gives a reference to the appropriate section for details.

Table 12-86. End of Transfer Sequences in FIFO Mode

Word count	TRANSMIT AND RECEIVE	TRANSMIT-ONLY	RECEIVE-ONLY
Yes	See Figure 12-64	See Figure 12-66	See Figure 12-67
No	See Figure 12-65	See Figure 12-66	See Figure 12-68

The end of transfer sequences are described from the start of the channel.

In these sequences, some soft variables are used:

- write_count = N
- read_count = N
- last_request = FALSE

They are initialized before starting the channel.

12.1.4.5.2.1.8.3 Transmit-and-Receive With Word Count

Figure 12-64 shows the flow of a transfer in transmit-and-receive mode, with word count.

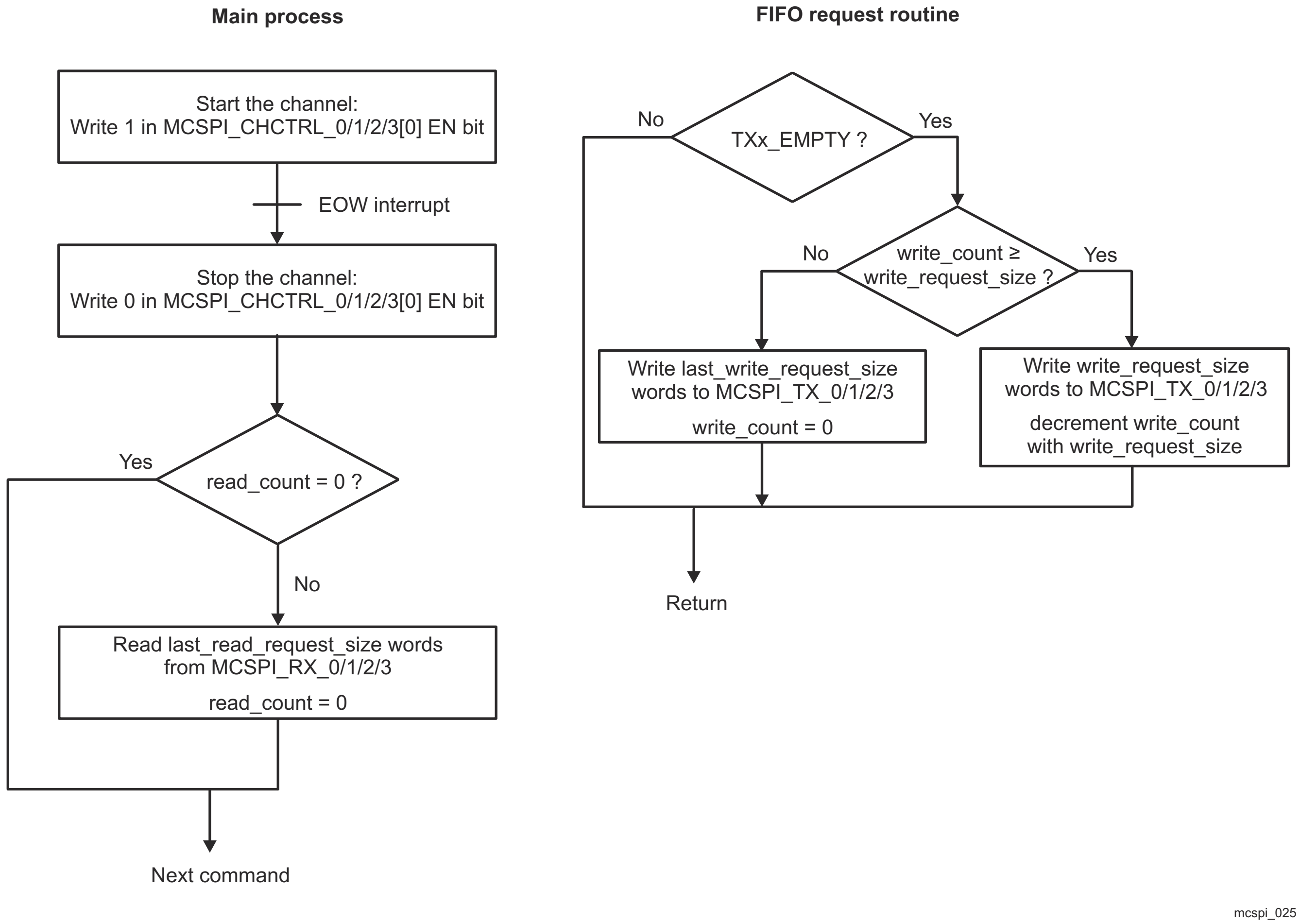

Figure 12-64. FIFO Mode Transmit-and-Receive With Word Count (Controller)

12.1.4.5.2.1.8.4 Transmit-and-Receive Without Word Count

Figure 12-65 shows the flow of a transfer in transmit-and-receive mode, without word count.

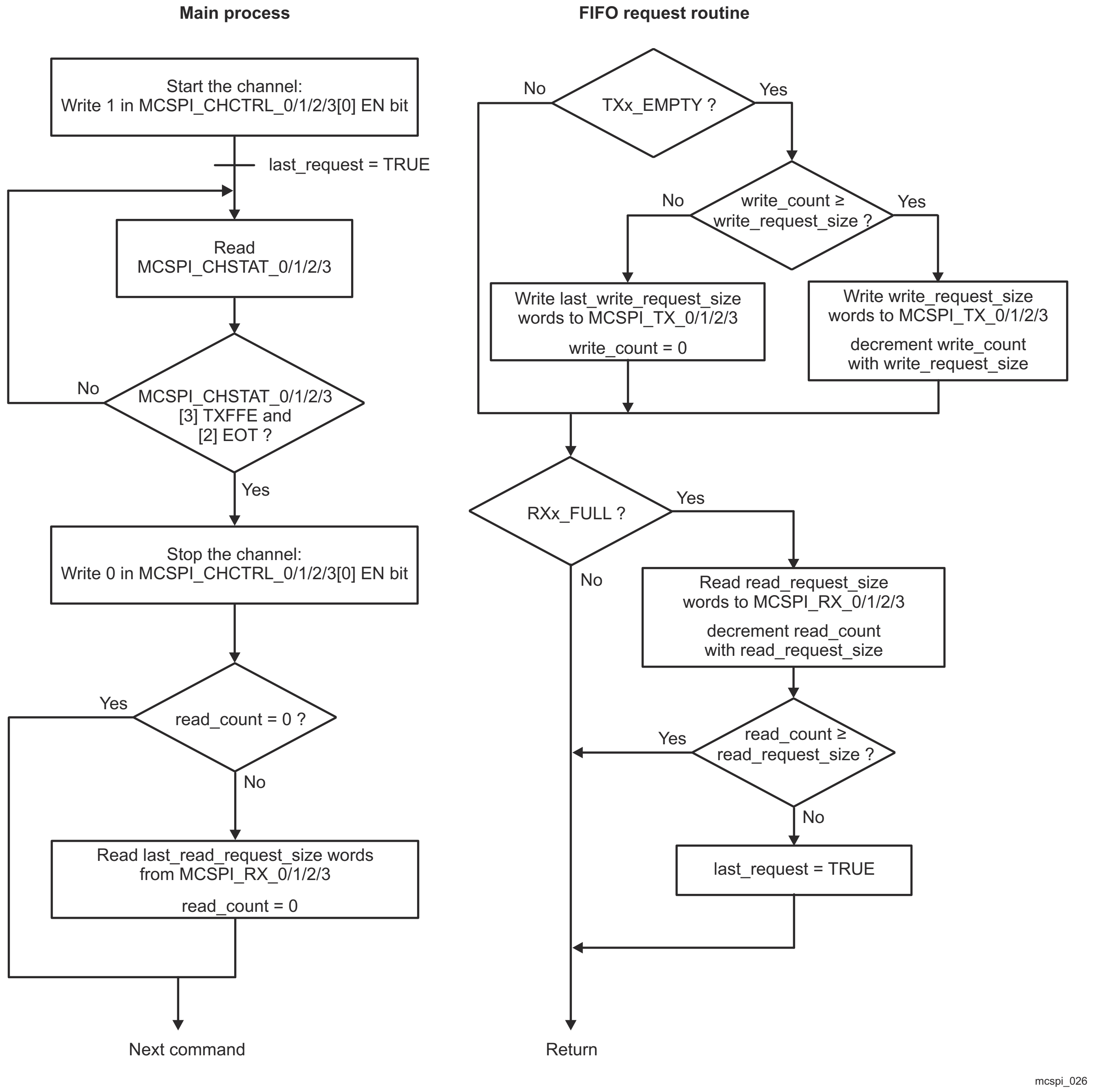

Figure 12-65. FIFO Mode Transmit-and-Receive Without Word Count (Controller)

12.1.4.5.2.1.8.5 Transmit-Only

Figure 12-66 shows the flow of a transfer in transmit-only mode, with or without word count. The difference between word count enabled or not is just on the condition after starting the channel:

- word count enable: wait for EOW interrupt
- word count disable: wait for write_count = 0

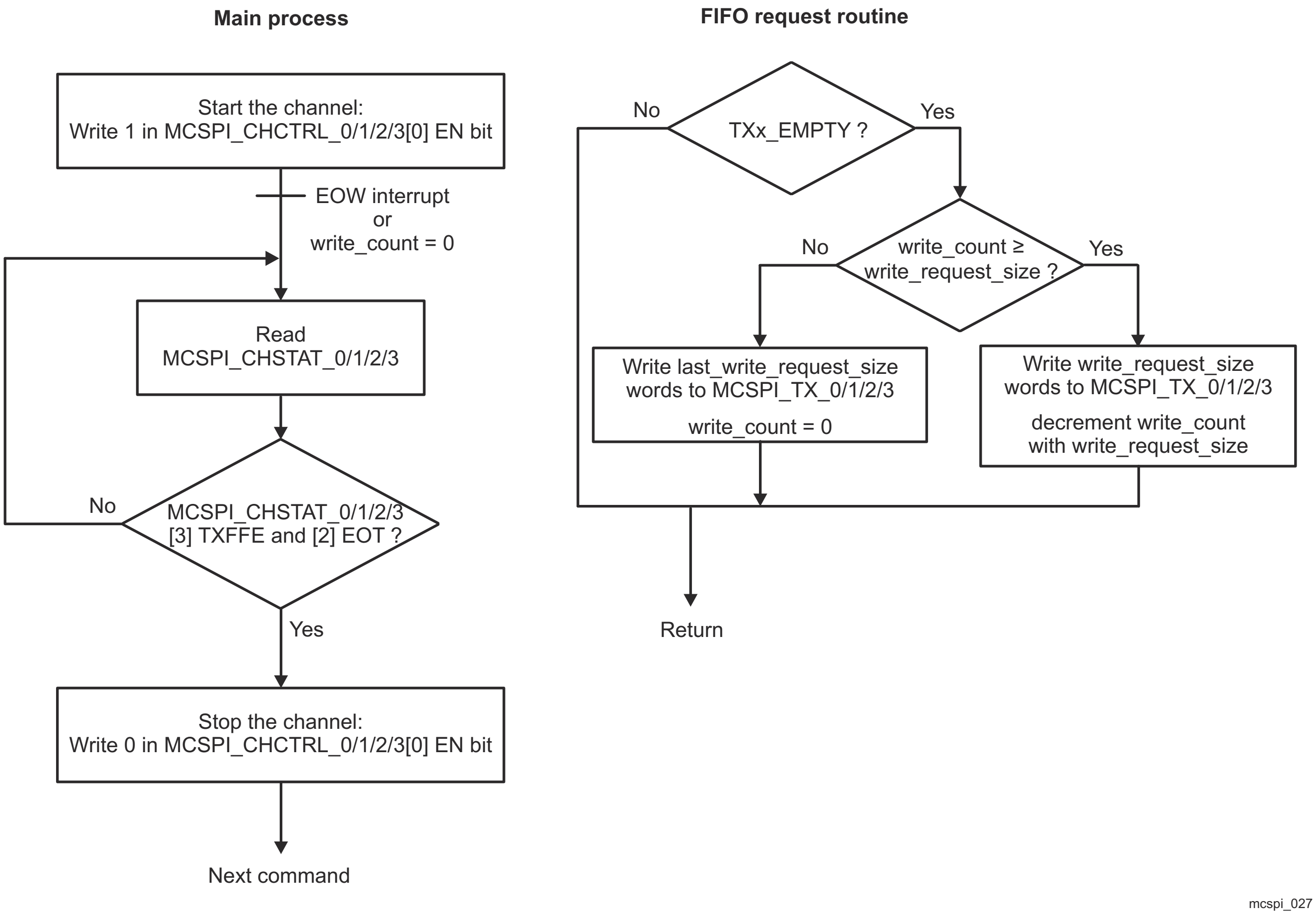

Figure 12-66. FIFO Mode Transmit-Only (Controller)

12.1.4.5.2.1.8.6 Receive-Only With Word Count

Figure 12-67 shows the flow of a transfer in receive-only mode, with word count.

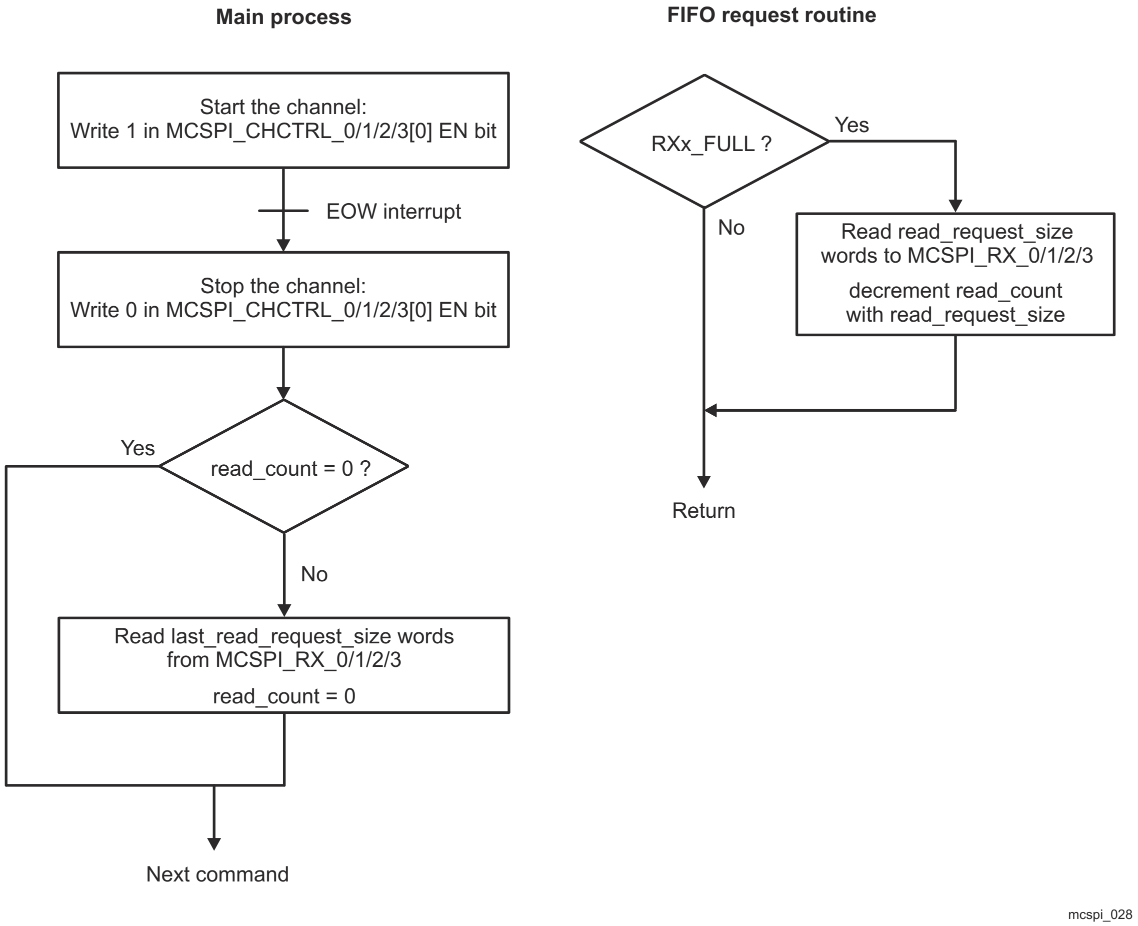

Figure 12-67. FIFO Mode Receive-Only With Word Count (Controller)

12.1.4.5.2.1.8.7 Receive-Only Without Word Count

Figure 12-68 shows the flow of a transfer in receive-only mode, with word count.

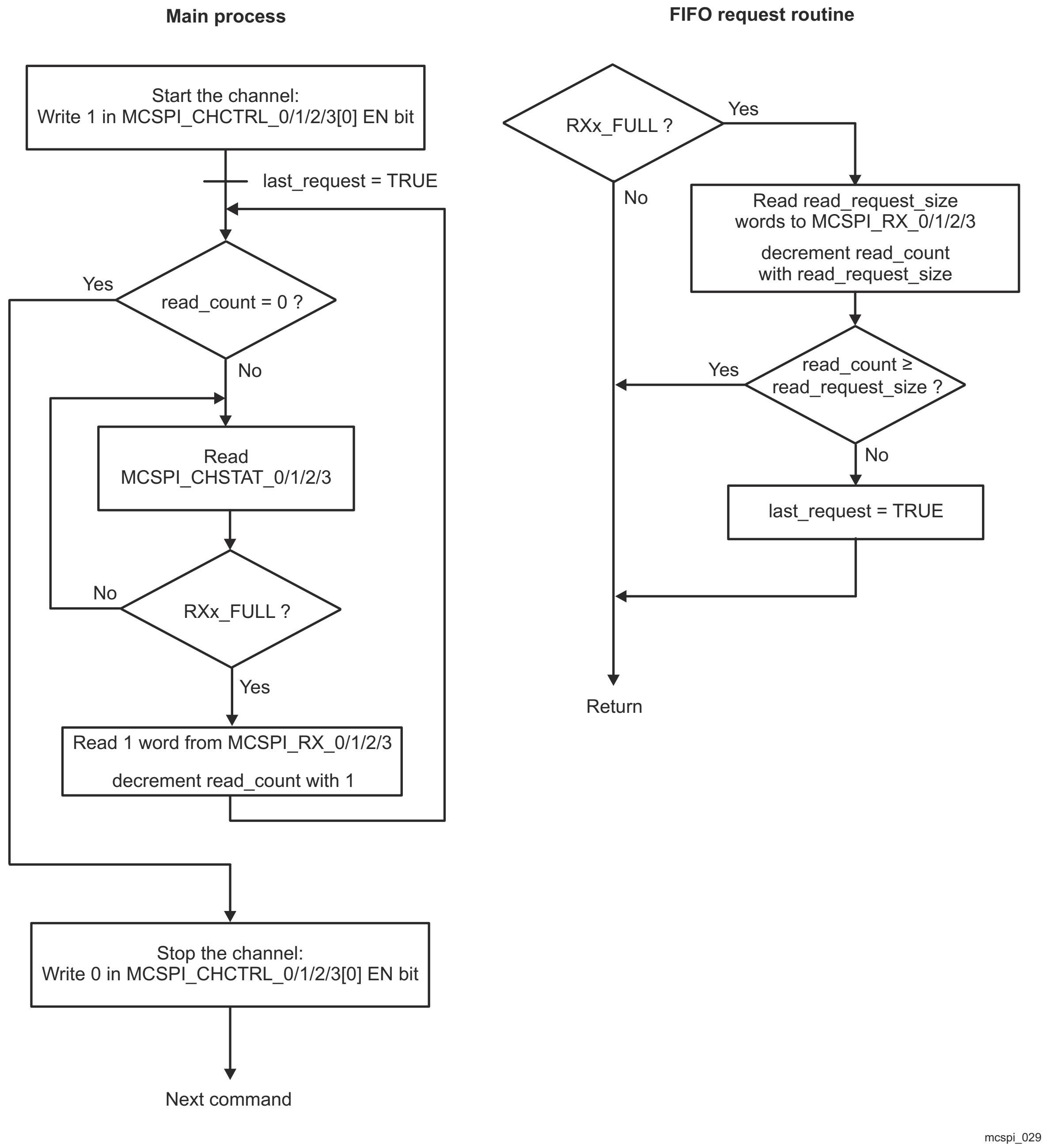

Figure 12-68. FIFO Mode Receive-Only Without Word Count (Controller)

12.1.4.5.2.1.9 Common Transfer Procedures Without FIFO – Polling Method

12.1.4.5.2.1.9.1 Receive-Only Procedure – Polling Method

Table 12-87 lists the receive-only procedure using the polling method.

Table 12-87. Receive-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-64.	
Start the channel.	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Wait for end-of-transfer.	MCSPI_CHSTAT_0/1/2/3[2] EOT	=1
Read the receiver register.	MCSPI_RX_0/1/2/3	0x-

Table 12-87. Receive-Only Procedure – Polling Method (continued)

Step	Register/Bit Field/Programming Model	Value
Stop the channel if no more data is expected.	MCSPI_CHCTRL_0/1/2/3[0] EN	0

12.1.4.5.2.1.9.2 Receive-Only Procedure – Interrupt Method

Table 12-88 lists the receive-only procedure using the interrupt method.

Table 12-88. Receive-Only Procedure – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-64.	
Start the channel.	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Enable the interrupt for the receiver register.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	1
Wait for interrupt.		
Read the status register.	MCSPI_IRQSTATUS[2] RX_FULL	1
Disable the interrupt if no more data is expected.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0
Stop the channel if no more data is expected.	MCSPI_CHCTRL_0/1/2/3[0] EN	0
Read the receiver register.	MCSPI_RX_0/1/2/3	0x-

12.1.4.5.2.1.9.3 Transmit-Only Procedure – Polling Method

Table 12-89 lists the transmit-only procedure using the polling method.

Table 12-89. Transmit-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-65.	
Start the channel.	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Write the transmitter register with data.	MCSPI_TX_0/1/2/3	0x-
Wait until end of transfer?	MCSPI_CHSTAT_0/1/2/3[2] EOT	=1
Stop the channel.	MCSPI_CHCTRL_0/1/2/3[0] EN	0

12.1.4.5.2.1.9.4 Transmit-and-Receive Procedure – Polling Method

Table 12-90 lists the transmit-and-receive procedure using the polling method.

Table 12-90. Transmit-and-Receive Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-66.	
Start the channel.	MCSPI_CHCTRL_0/1/2/3[0] EN	1
Write the transmitter register with data.	MCSPI_TX_0/1/2/3	0x-
Wait until transmit/receive word?	MCSPI_CHSTAT_0/1/2/3[2] EOT	=1
Stop the channel.	MCSPI_CHCTRL_0/1/2/3[0] EN	0
Read the receiver register.	MCSPI_RX_0/1/2/3	0x-

12.1.5 Universal Asynchronous Receiver/Transmitter (UART)

This chapter describes the function, operation, and configuration of the Universal Asynchronous Receiver/ Transmitter (UART)/RS-485/Infrared Data Association (IrDA)/Consumer Infrared (CIR)/ISO 7816 module in the device.

Note

UART and USART acronyms are used interchangeably in this section.

12.1.5.1 UART Overview

The UART is a peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. There are nine UART modules in the device. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

Table 12-91 shows UART modules allocation across device domains.

Table 12-91. UART Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
MCU_UART0	✓	-
MCU_UART1	✓	-
UART0	-	✓
UART1	-	✓
UART2	-	✓
UART3	-	✓
UART4	-	✓
UART5	-	✓
UART6	-	✓

Figure 12-69 shows the UART modules overview.

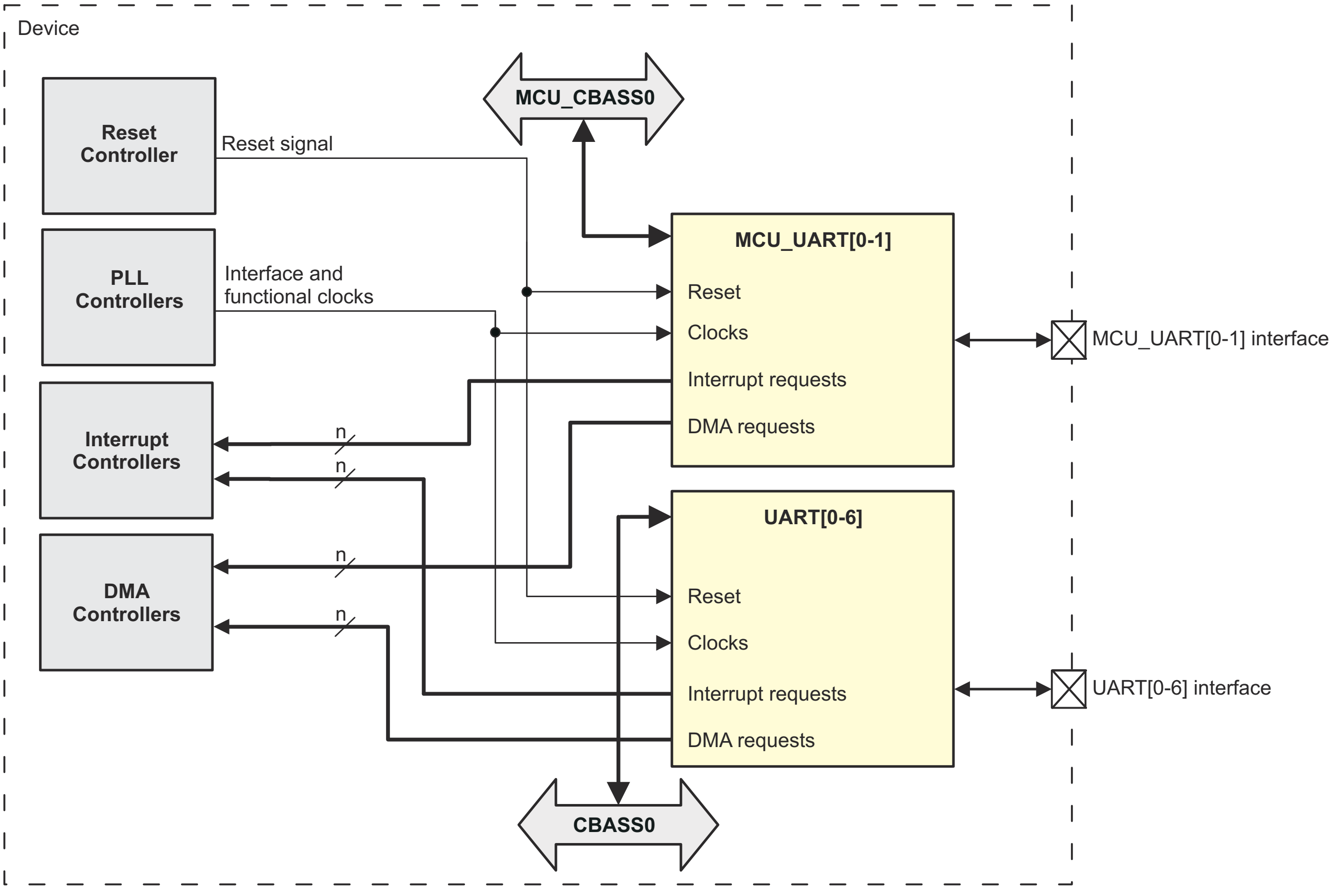

Figure 12-69. UART Modules Overview

12.1.5.1.1 UART Features

The UART includes the following features:

- 16C750-compatible
- RS-485 external transceiver auto flow control support
- 64-byte FIFO buffer for receiver and 64-byte FIFO buffer for transmitter
- Programmable interrupt trigger levels for FIFOs
- Programmable sleep mode
- The 48 MHz functional clock is default option and allows baud rates up to 3.6 Mbps
- Optional 192 MHz and 160 MHz functional clocks support baud rates up to 12 Mbps
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Optional multi-drop transmission
- Configurable time-guard feature
- Configurable data format:
  - Parity bit: Even, Odd, None
  - Stop-bit: 1, 1.5, 2 bit
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- False start bit detection
- Line break generation and detection
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities
- Modem control functions (CTS, RTS)
- Only module instance in MAIN domain has extended modem control signals (DCD, RI, DTR, DSR)

12.1.5.1.2 IrDA Features

The IrDA includes the following features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications:
  - Slow infrared (SIR 115.2 KBAUD), medium infrared (MIR 0.576 MBAUD) and fast infrared (FIR 4.0 MBAUD) operations (very fast infrared (VFIR) is not supported)
  - Frame formatting: addition of variable beginning-of-frame (xBOF) characters and end-of-frame (EOF) characters
  -
  - Asynchronous transparency (automatic insertion of break character)
  - Eight-entry status FIFO (with selectable trigger levels) to monitor frame length and frame errors
  - Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection
- IrDA mode when 48 MHz function clock is used

12.1.5.1.3 CIR Features

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on a user-definable frame structure and packet content.

The CIR includes the following features to provide CIR support for remote-control applications:

- Transmit and receive mode
- Free data format (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency
- 1/2, 5/12, 1/3, or 1/4 carrier duty cycle
- CIR mode when 48 MHz function clock is used

12.1.5.1.4 UART Not Supported Features

- Synchronous mode
- ISO7816 mode
- DMA mode 2

- Full modem handshaking is not available on all instances - see device datasheet for details
- Multi-drop transmission
- 9-bit mode
- Baud rate above 3.6Mbps are not supported by UARTs in MCU domain (MCU_UART*)

12.1.5.2 UART Environment

The MCU_UART[0-1],UART[0-6] modules are hereinafter referred to as UART module.

This section describes the UART/RS-485/IrDA/CIR external connections (environment).

- The UART interface is described in Section 12.1.5.2.1 , *UART Functional Interfaces*.
- The RS-485 interface is described in Section 12.1.5.2.2 , *RS-485 Functional Interfaces*.
- The IrDA interface is described in Section 12.1.5.2.3 , *IrDA Functional Interfaces*.
- The CIR interface is described in Section 12.1.5.2.4 , *CIR Functional Interfaces*.

12.1.5.2.1 UART Functional Interfaces

12.1.5.2.1.1 System Using UART Communication With Hardware Handshake

Each UART instance can be easily connected to the UART port of an external IC (see Figure 12-70).

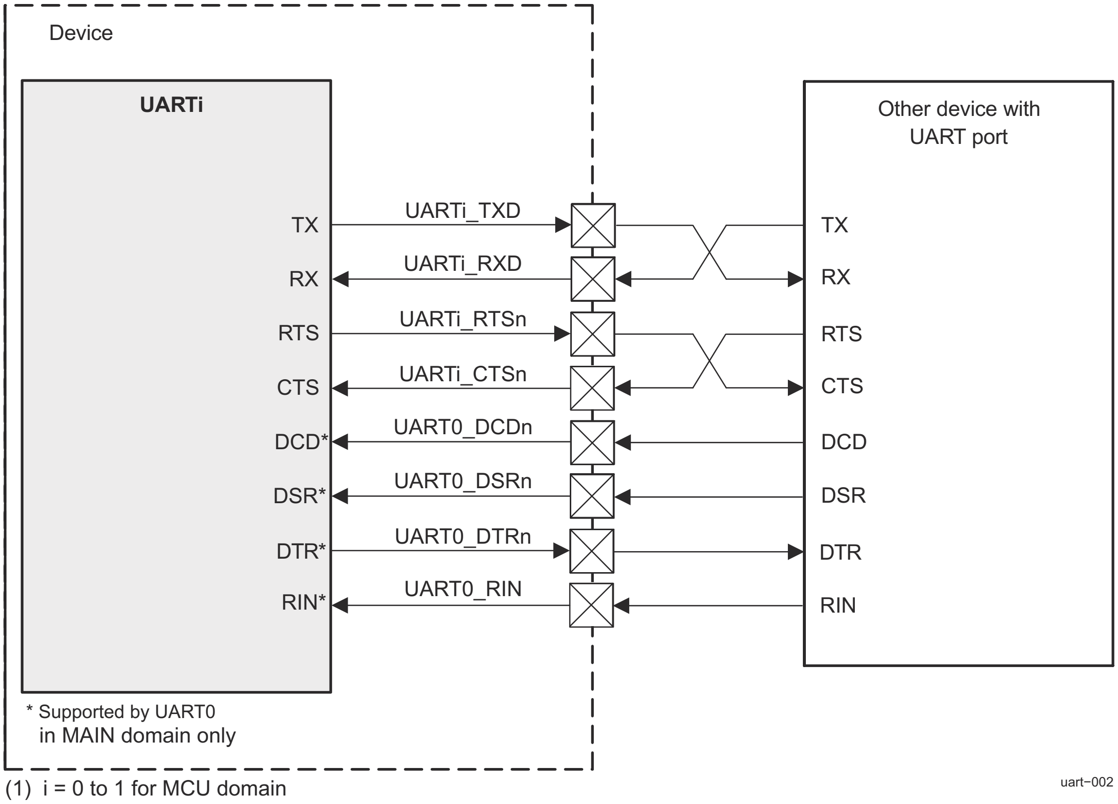

(1) i = 0 to 1 for MCU domain
(2) i = 0 to 6 for MAIN domain

Figure 12-70. UART Mode Interface Signals

12.1.5.2.1.2 UART Interface Description

Table 12-92 lists the UART interface input/output (I/O) signals.

Table 12-92. UART I/O Signals

Module Pin Name	Device Level Signal Name	I/O[1]	Description	Module Pin Reset Value[2]
		UART[0-6]		
RX	UART[0-6]_RXD	I	Serial data input	HiZ
TX	UART[0-6]_TXD	O	Serial data output[3]	1
CTS	UART[0-6]_CTSn	I	Clear to send[4]	HiZ
RTS	UART[0-6]_RTSn	O	Request to send[5]	1
DCD		I	Data Carrier Detect[6]	HiZ
DSR		I	Data Set Ready[7]	HiZ
DTR		O	Data Terminal Ready[8]	1
RIN		I	Ring Indicator[9]	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) Because this pin is active high in IrDA mode and the output is muxed, this pin is set to low on reset (when the UART_MDR1[2-0] bit field is set to 0x7) and takes the defined inactive level of that signal corresponding to when and how the UART_MDR1 register is programmed; that is, the output is 1 (inactive for UART modem modes) and 0 (inactive for IrDA modes).

(4) Active-low modem status signal. Reading the UART_MSR[4] NCTS_STS bit checks the condition of CTS. Reading the UART_MSR[0] CTS_STS bit checks a change of state of CTS since the last read of the modem status register. The auto-CTS mode uses CTS to control the transmitter.

(5) When active (low), the module is ready to receive data. Setting the UART_MCR[1] RTS bit activates RTS signal, which becomes inactive as the result of a module reset, loopback mode, or clearing the UART_MCR[1] RTS bit. In auto-RTS mode, RTS signal becomes inactive as a result of the receiver threshold logic.

(6) Active-low modem status signal. The condition of DCD can be checked by reading the UART_MSR[7] NCD_STS bit. Any change in its state can be detected by reading the UART_MSR[3] DCD_STS bit.

(7) Active-low modem status signal. Reading the UART_MSR[5] NDSR_STS bit checks the condition of DSR. Reading the UART_MSR[1] DSR_STS bit checks a change of state of DSR since the last read of the UART_MSR register.

(8) When active (low), this signal informs the modem that the module is ready to communicate. It is activated by setting the UART_MCR[0] DTR bit.

(9) Active-low modem status signal. The condition of RIN can be checked by reading the UART_MSR[6] NRI_STS bit. Any change in its state can be detected by reading the UART_MSR[2] RI_STS bit.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Data sheet.

12.1.5.2.1.3 UART Protocol and Data Format

The UART device operates in three modes:

- UART 16× (<= 230.4 kbps)
- UART 16× with autobauding (>= 1200 bps and <= 115.2 kbps)
- UART 13× (>= 460.8 kbps)

CAUTION

To be used as a UART, the operating mode must be programmed appropriately in the UART_MDR1[2-0] MODE_SELECT bit field to select UART, IrDA, or CIR mode, and the UART_MDR3[4] DIR_EN bit field to select RS-485 mode.

The UART uses a wired interface for serial communication with a remote device.

The UART is functionally compatible with the TL16C750 UART and earlier designs such as the TL16C550.

Figure 12-71 shows the UART frame data format.

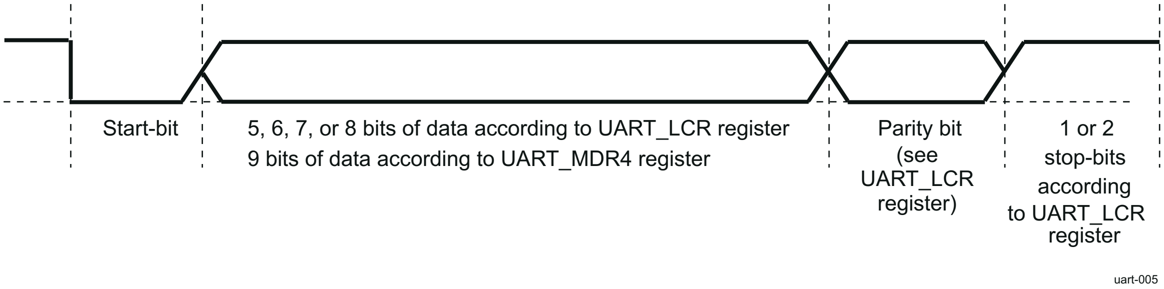

Figure 12-71. UART Frame Data Format

Note

Not all operating modes are described in the diagram. The UART module is capable of supporting a 9-bit mode that is not shown in the diagram.

12.1.5.2.1.4 UART 9-bit Mode Data Format

The UART is capable of full 9-bit operation when configured so in UART_MDR4[6] MODE9 bit. The full 9-bit data can only be written and read through the UART_ETHR / UART_ERHR registers. The data can be accessed either with a single or two accesses using appropriate OCP byte enables. In case two accesses are used, make sure to read/write the higher byte first, as reading/writing the lower one will advance the FIFO.

The UART_RHR / UART_ERHR and UART_THR / UART_ETHR registers point to the same location and either can be used as preferred, in regards to the lower 8 bits.

12.1.5.2.2 RS-485 Functional Interfaces

12.1.5.2.2.1 System Using RS-485 Communication

The RS-485 network physical layer consists of two-wire differential bus, usually twisted pair. External RS-485 transceiver IC is needed to access a RS-485 bus by the RS-485 mode. Figure 12-72 shows an example connection of UART in RS-485 mode.

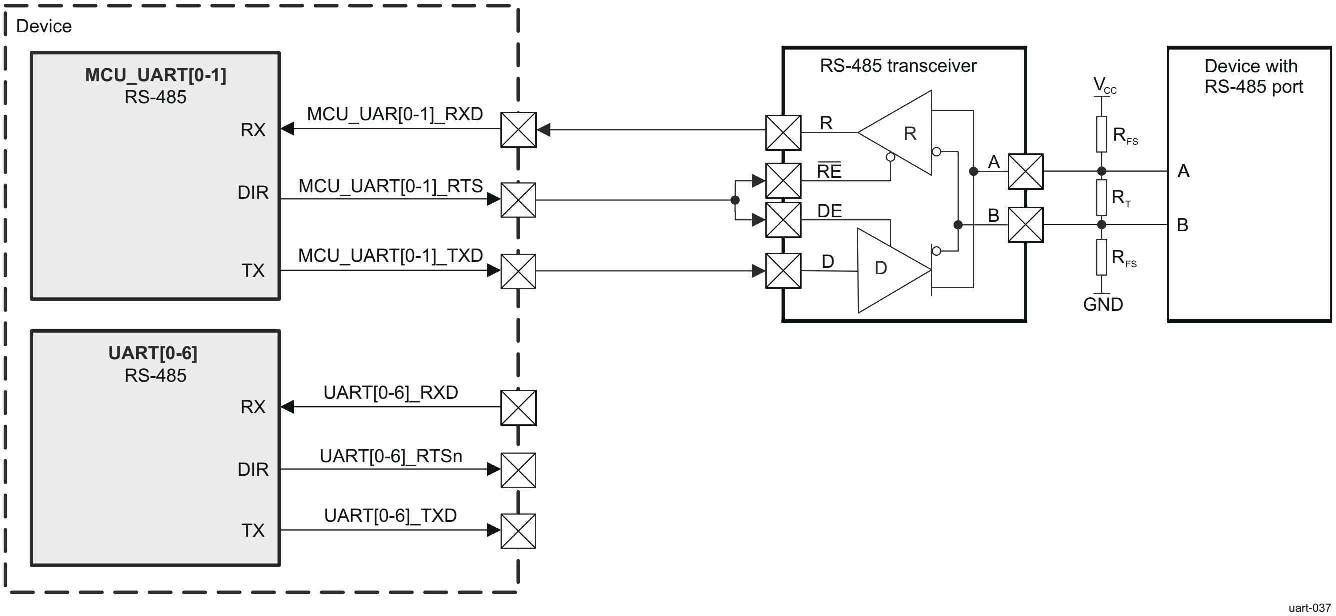

Figure 12-72. RS-485 Mode Interface Signals

12.1.5.2.2.2 RS-485 Interface Description

Table 12-93 lists the RS-485 interface input/output (I/O) signals.

Table 12-93. UART I/O Signals (RS-485 Mode)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
			MCU_UART[0-1]	
RX	MCU_UART[0-1]_RXD	I	Serial data input	HiZ
TX	MCU_UART[0-1]_TXD	O	Serial data output	1
DIR	MCU_UART[0-1]_RTS	O	RS-485 Direction	1
			UART[0-6]	
RX	UART[0-6]_RXD	I	Serial data input	HiZ
TX	UART[0-6]_TXD	O	Serial data output	1
DIR	UART[0-6]_RTSn	O	RS-485 Direction	1

(1) I = Input; O = Output

(2) HiZ = High Impedance

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Data sheet.

12.1.5.2.3 IrDA Functional Interfaces

12.1.5.2.3.1 System Using IrDA Communication Protocol

Figure 12-73 shows an example connection of MCU_UART0 to an external infrared transceiver in the IrDA modes (FIR, SIR, and MIR).

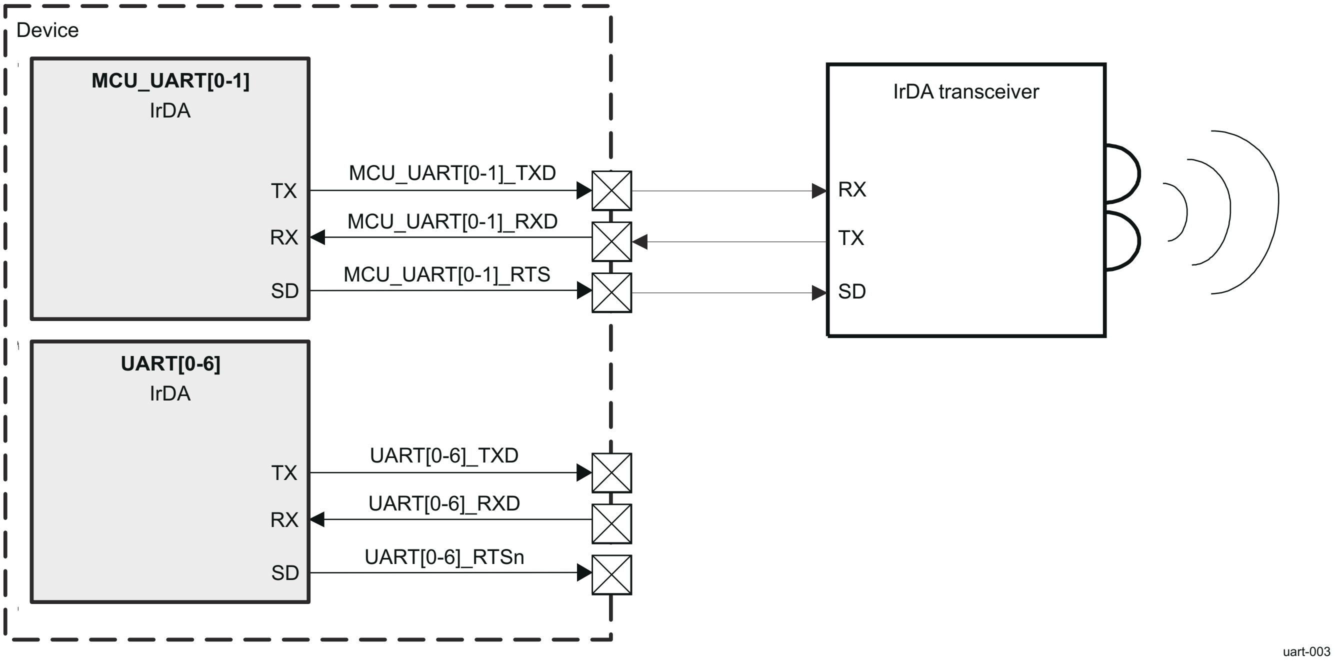

Figure 12-73. IrDA Mode Interface Signals

12.1.5.2.3.2 IrDA Interface Description

Table 12-94 lists the IrDA interface I/O signals.

Table 12-94. UART I/O Signals (IrDA Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
			MCU_UART[0-1]	
RX	MCU_UART[0-1]_RXD	I	Serial data input	HiZ
TX	MCU_UART[0-1]_TXD	O	Serial data output in IrDA modes (SIR, MIR, and FIR).[3]	0
SD	MCU_UART[0-1]_RTS	O	SD mode is used to configure the transceivers.[4]	1
			UART[0-6]	
RX	UART[0-6]_RXD	I	Serial data input	HiZ
TX	UART[0-6]_TXD	O	Serial data output in IrDA modes (SIR, MIR, and FIR).[3]	0
SD	UART[0-6]_RTSn	O	SD mode is used to configure the transceivers.[4]	1

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) In other modes, this pin is set to the reset value (inactive state).
(4) The SD pinout (see UART_ACREG[6] SD_MOD bit).

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Data sheet.

12.1.5.2.3.3 IrDA Protocol and Data Format

12.1.5.2.3.3.1 SIR Mode

In SIR mode, data is transferred between the Host CPU and peripheral devices at speeds of up to 115200 baud. A SIR transmit frame begins with start flags (a single 0xC0, a multiple 0xC0, or a single 0xC0 preceded by a number of 0xFF flags), followed by frame data and a CRC-16, and ends with a stop flag (0xC1).

The bit format for a single word uses 1 start-bit, 8 data bits, and 1 stop-bit, and is unaffected by the use and settings of the UART_LCR register.

The UART_BLR[6] XBOF_TYPE bit selects whether the 0xC0 or 0xFF start patterns are used when multiple start flags are required.

The SIR transmit state-machine attaches start flags, CRC-16, and stop flags, and checks the outgoing data to establish whether data transparency is required.

The SIR transparency is carried out if the outgoing data between the start and stop flags contains 0xC0, 0xC1, or 0x7D. If one of these start flags is about to be transmitted, the SIR state-machine sends an escape character (0x7D), inverts the fifth bit of the real data to be sent, and then sends this data immediately after the 0x7D character.

The SIR receive state-machine recovers the receive clock, removes the start flags and any transparency from the incoming data, and determines the frame boundary with reception of the stop flag. The SIR state-machine also checks for errors such as a frame abort (0x7D character followed immediately by a 0xC1 stop flag without transparency), a CRC error, or a frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to find possible errors of the received frame.

Note

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. See the description of the UART_ACREG[5] DIS_IR_RX bit. This applies to all three modes: SIR, MIR, and FIR.

Infrared output in SIR mode can be 1.6-µs or 3/16 encoding, selected by the UART_ACREG[7] PULSE_TYPE bit. In 1.6-µs encoding, the infrared pulse width is 1.6 µs; and in 3/16th encoding, the infrared pulse width is 3/16th of a bit duration (1/baud rate).

For back-to-back frames, the transmitting device must send at least two start flags at the start of each frame.

Note

Reception supports variable-length stop-bits.

12.1.5.2.3.3.1.1 Frame Format

Figure 12-74 shows the IrDA SIR frame format.

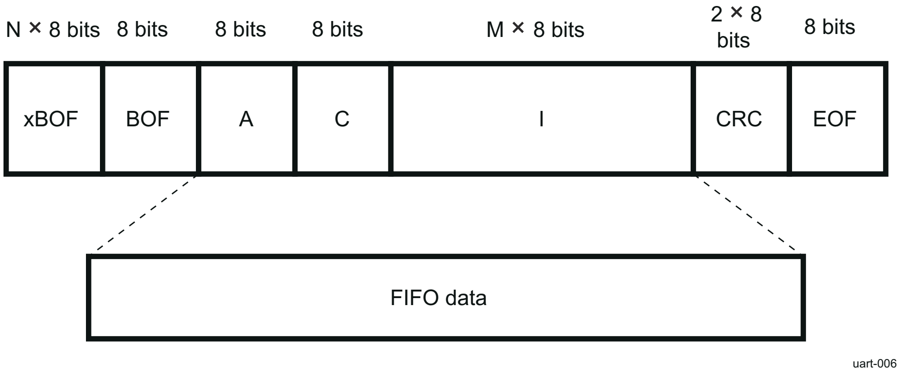

Figure 12-74. IrDA SIR Frame Format

The CRC is applied on the address (A), control (C), and information (I) bytes.

Note

The two words of CRC are written to the FIFO in reception.

12.1.5.2.3.3.1.2 Asynchronous Transparency

Before transmitting a byte, the UART IrDA controller examines each byte of the payload and the CRC field (between BOF and EOF). For each byte equal to 0xC0 (BOF), 0xC1 (EOF), or 0x7D (control escape), the controller performs certain tasks:

- In transmission:
  - Inserts a control escape (CE) byte preceding the byte
  - Complements bit 5 of the byte (that is, exclusive ORs the byte with 0x20)

  The byte sent for the CRC computation is the initial byte written in the TX FIFO (before the XOR with 0x20).
- In reception:

  For the A, C, I, and CRC fields:
  - Compares the byte with the CE byte; if they are not equal, sends the byte to the CRC detector and stores it in the RX FIFO.

- If the byte is equal to the CE byte, discards the CE byte
- Complements bit 5 of the byte following the CE
- Sends the complemented byte to the CRC detector and stores it in the RX FIFO

12.1.5.2.3.3.1.3 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

When a 0x7D character that is followed immediately by a 0xC1 character is received without transparency, the receiver treats the frame as an aborted frame.

12.1.5.2.3.3.1.4 Pulse Shaping

The SIR mode supports the 3/16 and the 1.6-µs pulse duration methods. The UART_ACREG[7] PULSE_TYPE bit selects the pulse-width method in transmit mode.

12.1.5.2.3.3.1.5 Encoder

Serial data from the transmit state-machine are encoded to transmit data to the optoelectronics. While the TX FIFO output is high, the TX line is always low, and the counter used to form a pulse on TX is cleared continuously.

After the TX FIFO output resets to 0, TX rises on the falling edge of the seventh 16XCLK. On the falling edge of the tenth 16XCLK pulse, TX falls, creating a 3-clock-wide pulse. While the TX FIFO output stays low, a pulse is transmitted during the seventh clock to the tenth clock of each 16-clock bit cycle.

Figure 12-75 shows the IrDA SIR encoding mechanism.

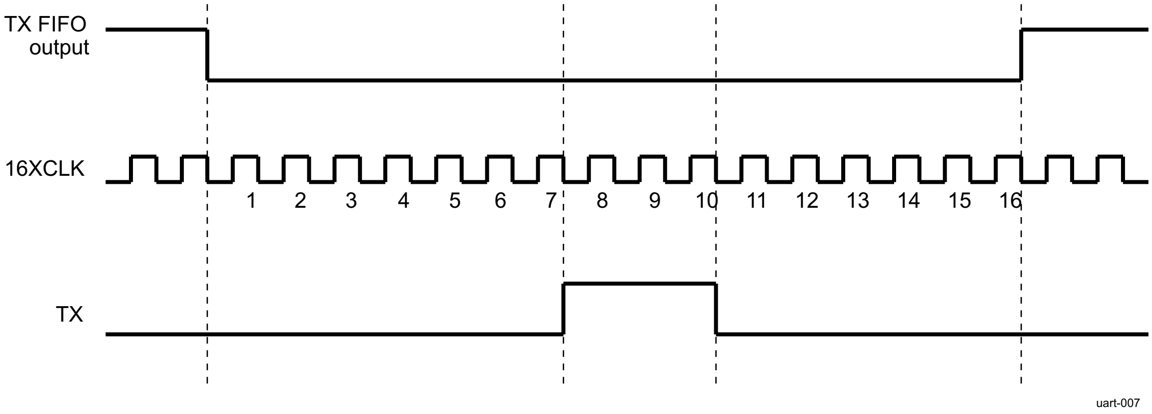

Figure 12-75. IrDA SIR Encoding Mechanism

12.1.5.2.3.3.1.6 Decoder

After reset, the RX FIFO input is high and the 4-bit counter is cleared. When a rising edge is detected on RX, the RX FIFO input falls on the next rising edge of 16XCLK with sufficient setup time. The RX FIFO input stays low for 16 cycles (16XCLK) and then returns to high as required by the IrDA specification. As long as no pulses (rising edges) are detected on the RX, the RX FIFO input remains high.

Figure 12-76 shows the IrDA SIR decoding mechanism.

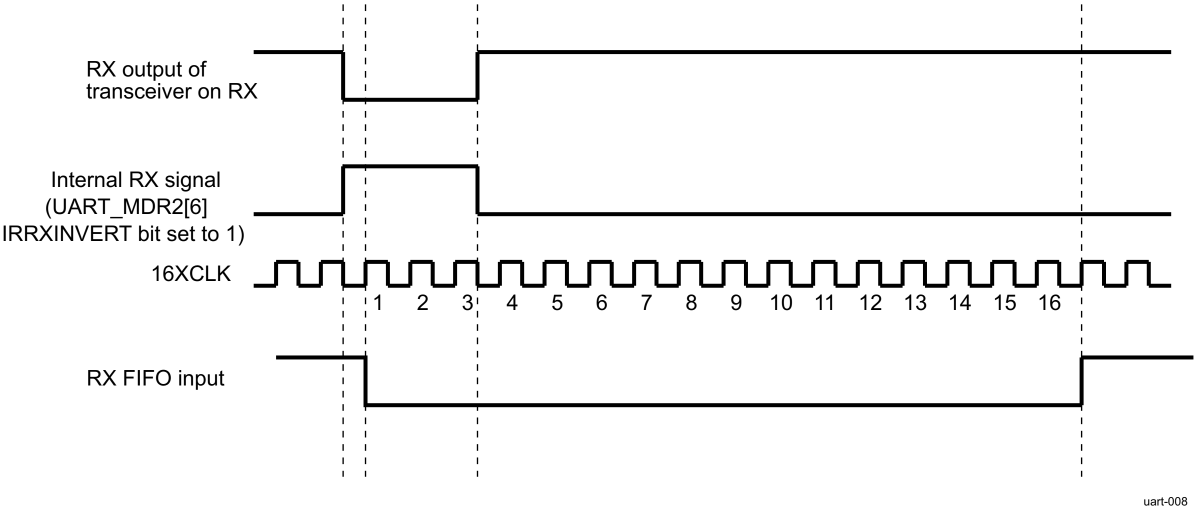

Figure 12-76. IrDA SIR Decoding Mechanism

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. The operation of the RX input can be disabled using the UART_ACREG[5] DIS_IR_RX bit. The UART_MDR2[6] IRRXINVERT bit can invert the signal from the transceiver (RX) pin to the IR RX logic in the UART. This inversion is performed by default.

12.1.5.2.3.3.1.7 IR Address Checking

In all IR modes, when address checking is enabled by setting the UART_EFR[1-0] bit field (see Table 12-95), only frames intended for the device are written to the RX FIFO. This is to avoid receiving frames not meant for this device in a multipoint infrared environment. To program two frame addresses that the UARTi receives in IrDA mode, use the UART_XON1_ADDR1[7-0] and UART_XON2_ADDR2[7-0] bit fields.

Table 12-95. UART_EFR[1-0] IR Address Checking Options

UART_EFR[1]	UART_EFR[0]	IR Address Checking
0	0	All address-checking operations disabled
0	1	Only address 1 checking enabled
1	0	Only address 2 checking enabled
1	1	All address-checking operations enabled

12.1.5.2.3.3.2 SIR Free-Format Mode

To allow complete software flexibility when transmitting and receiving infrared data packets, the SIR free-format (FF) mode is a subfunction of the existing SIR mode. In FF mode, all frames going to and from the FIFO buffers are untouched with respect to appending and removing control characters and CRC values.

The FF mode corresponds to a UART mode with a pulse modulation of 3/16 of baud rate pulse width.

For example, a normal SIR packet has BOF control and CRC error-checking data appended (transmitting) or removed (receiving) from the data going to and from the FIFOs.

Figure 12-77 shows SIR FF mode.

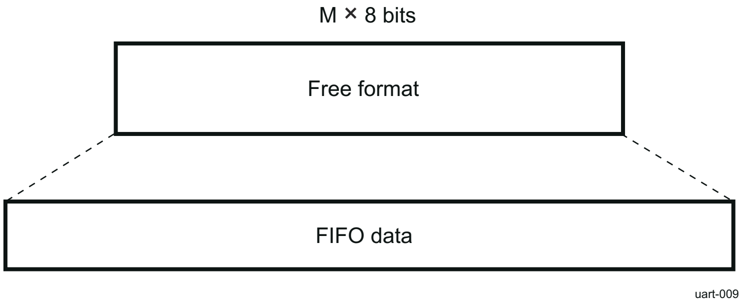

Figure 12-77. SIR FF Mode

In SIR FF mode, the Host CPU software must construct (that is, encode and decode) the entire FIFO data packet.

The SIR Free Format mode is selected by setting the module in UART mode (MDR1[2:0] = 000) and the MDR2[3] register bit to one to allow the pulse shaping. As the bit format is to remain the same, some UART mode configuration registers need to be set at specific value:

- LCR[1:0] = "11" (8 data bits)
- LCR[2] = 0 (2 stop bit)
- LCR[3] = 0 (no parity)
- ACREG[7] = 0 (3/16 of baud-rate pulse width)

The features defined through MDR2[6] and ACREG[5] are also supported, however:

- All other configuration registers need to be at the reset value
- The same UART mode interrupts used for the SIR FF mode are not necessarily relevant (XOFF, RTS, CETS, Modem Status Register)

12.1.5.2.3.3.3 MIR Mode

In MIR mode, data is transferred between the Host CPU and the peripheral devices at 0.576 Mbps or 1.152 Mbps. A MIR transmit frame starts with at least two start flags, followed by a frame data and a CRC-16, and ends with a stop flag (see Figure 12-78).

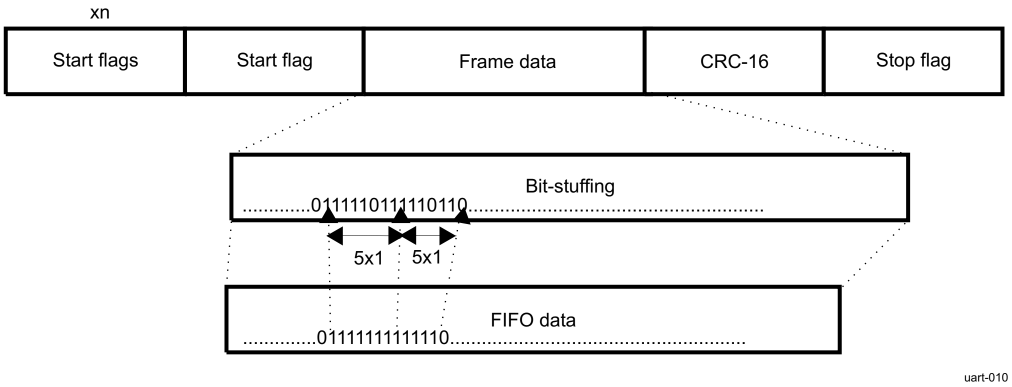

Figure 12-78. MIR Transmit Frame Format

On transmit, the MIR state-machine attaches start flags, a CRC-16, and stop flags, as in SIR mode. All fields are transmitted least-significant bit (LSB) of each byte first.

In MIR mode:

- The state-machine looks for consecutive 1s in the frame data and automatically inserts 0 after five consecutive 1s (this is called bit-stuffing).
- 0x7E is used for start and stop flags (unambiguously, not data, because of bit-stuffing).

- An abort sequence requires a minimum of seven consecutive 1s (unambiguously, not data, because of bit-stuffing).
- Back-to-back frames are allowed with three or more stop flags between them. If two consecutive frames are not back to back, the gap between the last stop flag of the first frame and the start flag of the second frame must be separated by at least seven bit durations.

On receive, the MIR receive state-machine recovers the receive clock, removes the start flags, destuffs the incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as frame abort, CRC error, and frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

12.1.5.2.3.3.3.1 MIR Encoder/Decoder

To meet the MIR baud rate tolerance of 0.1 percent with a 48-MHz clock input, a 42-41-42 encoding/decoding adjustment is performed. The reference start point is the first start flag, and the 42-41-42 cyclic pattern is repeated until the stop flag is sent or detected.

The jitter created this way is within MIR tolerances. The pulse width is not exactly 1/4, but it is within the tolerances defined by IrDA specifications.

Figure 12-79 shows the MIR baud rate adjustment mechanism.

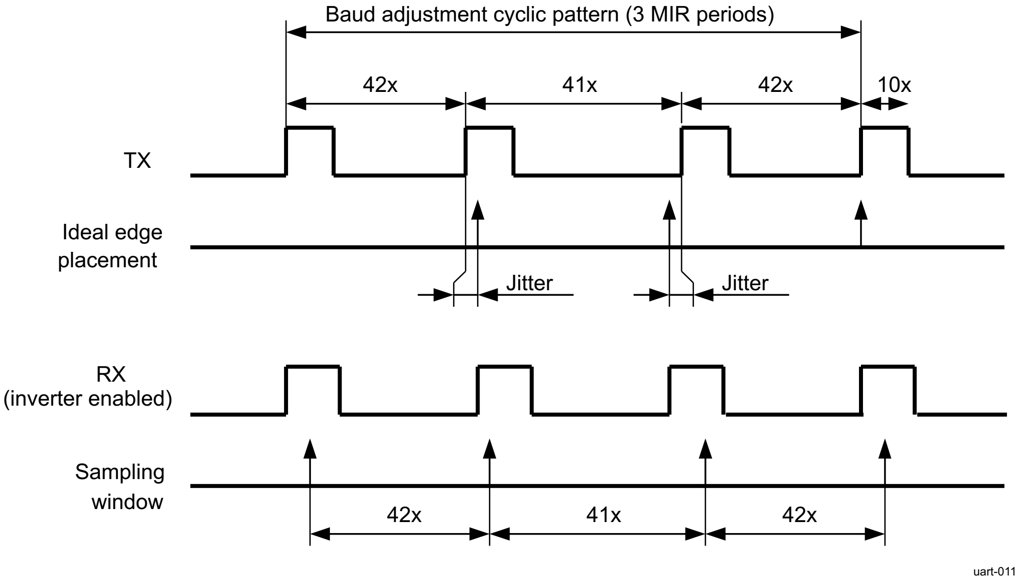

Figure 12-79. MIR Baud Rate Adjustment Mechanism

12.1.5.2.3.3.3.2 SIP Generation

In the MIR and FIR operation modes, the transmitter must send a serial infrared interaction pulse (SIP) at least once every 500 ms. The SIP informs slow devices (operating in SIR mode) that the medium is occupied.

Figure 12-80 shows the SIP.

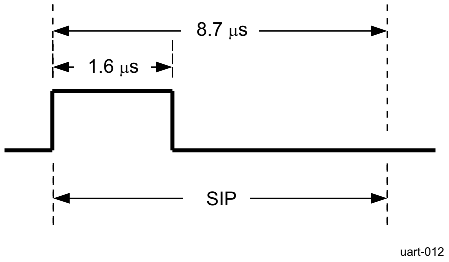

Figure 12-80. SIP

When the SIP_MODE bit of the Mode Definition Register 1 is equal to 1 (MDR1[6]), the TX state machine will always send one SIP at the end of the transmission frame. When MDR1[6] is equal to 0, the transmission of the SIP depends on the SEND_SIP bit of the Auxiliary Control Register (ACREG[3]). The system (Host CPU) can set ACREG[3] at least once every 500ms. The advantage of this approach over the default approach is that the TX state machine does not need to send the SIP at the end of each frame, which may reduce the overhead required.

12.1.5.2.3.3.4 FIR Mode

In FIR mode, data is transferred between the Host CPU and the peripheral devices at 4 Mbps. A FIR transmit frame starts with a preamble that is followed by a start flag, frame data, CRC-32, and ends with a stop flag.

Figure 12-81 shows the FIR transmit frame format.

Figure 12-81. FIR Transmit Frame Format

Preamble (16x)	Start flag	Frame data	CRC-32	Stop flag

On transmit, the FIR transmit state-machine attaches the preamble, start flag, CRC-32, and stop flag. An abort sequence requires at least two transmissions of 0000. Back-to-back frames are allowed, but each frame must be complete.

The state-machine also encodes the transmit data into 4-PPM format (see Table 12-96) and generates the SIP (see Section 12.1.5.2.3.3.2 , *SIP Generation*).

Table 12-96. 4-PPM Format

Data Bit Pair (Bin)	4-PPM Data Symbol (Bin)
00	1000
01	0100
10	0010
11	0001

The four symbols described in Table 12-96 are the legal, encoded data symbols. All other combinations are illegal for encoding data. Some of these illegal symbols are used in the definition of the preamble, start flag, and stop flag because they are unambiguously not data (see Table 12-97).

Table 12-97. FIR Preamble, Start Flag, and Stop Flag

Frame Part	Transmitted Frame (Bin)
Preamble	1000 0000 1010 1000 (16 repeated transmissions)
Start flag	0000 1100 0000 1100 0110 0000 0110 0000
Stop flag	0000 1100 0000 1100 0000 0110 0000 0110

All fields are transmitted LSBs of each byte first (see Table 12-98).

Table 12-98. FIR Data Byte Transmission Order Example

Data Byte (Hex)	Data Byte Pair (Bin)	4-PPM Data Symbol (Bin)	Transmission Order
0x0B	00	1000	4
	00	1000	3
	10	0010	2
	11	0001	1

On receive, the FIR receive state-machine recovers the receive clock, removes the preamble and the start flag, decodes the 4-PPM incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as illegal symbol, CRC error, and frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

12.1.5.2.4 CIR Functional Interfaces

12.1.5.2.4.1 System Using CIR Communication Protocol With Remote Control

All UART modules can be connected to an external infrared transceiver in CIR mode. Figure 12-82 shows an example connection of MCU_UART0 in CIR mode.

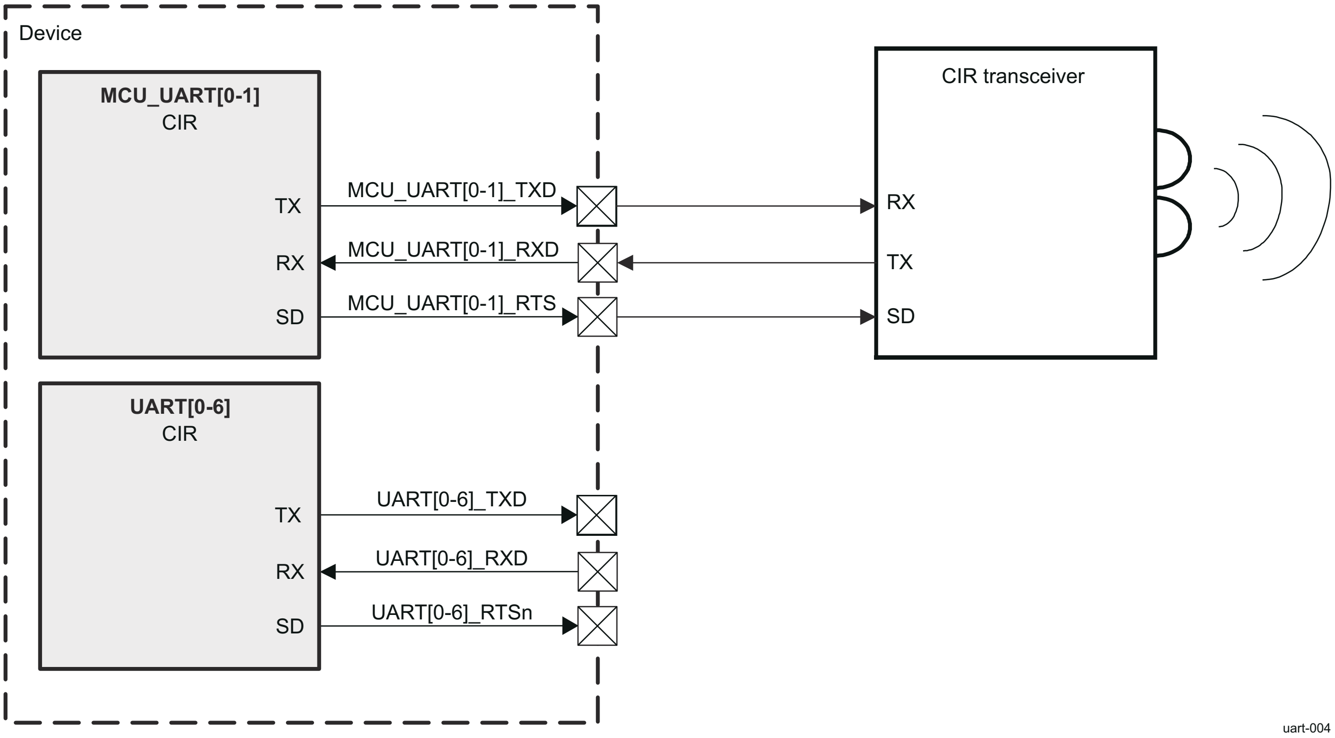

Figure 12-82. CIR Mode Interface Signals

12.1.5.2.4.2 CIR Interface Description

Table 12-99 lists the CIR interface I/O signals.

Table 12-99. UART I/O Signals (CIR Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
			MCU_UART[0-1]	

Table 12-99. UART I/O Signals (CIR Mode) (continued)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
RX	MCU_UART[0-1]_RXD	I	Serial data input	HiZ
TX	MCU_UART[0-1]_TXD	O	Serial data output in CIR mode. [3]	0
SD	MCU_UART[0-1]_RTS	O	SD mode is used to configure the transceivers.[4]	1
			UART[0-6]	
RX	UART[0-6]_RXD	I	Serial data input	HiZ
TX	UART[0-6]_TXD	O	Serial data output in CIR mode. [3]	0
SD	UART[0-6]_RTSn	O	SD mode is used to configure the transceivers.[4]	1

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) In other modes, this pin is set to the reset value (inactive state).
(4) The SD pinout is an inverted value of the UART_ACREG[6] SD_MOD bit.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Data sheet.

12.1.5.2.4.3 CIR Protocol and Data Format

In CIR mode, the infrared operation functions as a programmable (universal) remote control.

The CIR mode uses a variable PWM technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on user-defined frame structure and packet content.

12.1.5.2.4.3.1 Carrier Modulation

Each modulated pulse that constitutes a digit is a train of on/off pulses (see Figure 12-83).

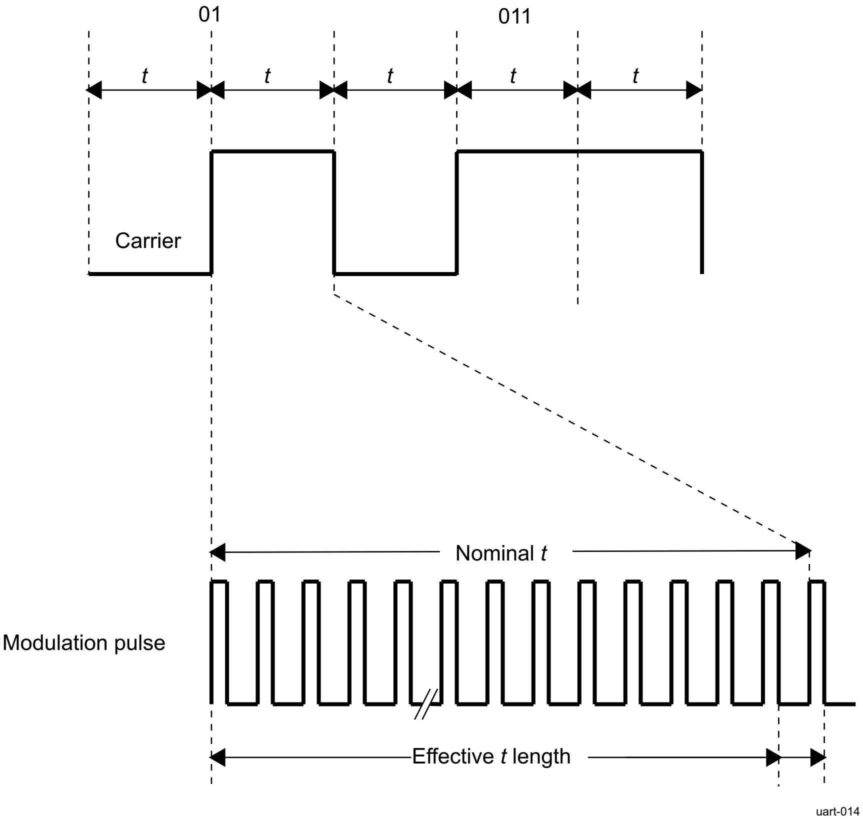

Figure 12-83. CIR Pulse Modulation

12.1.5.2.4.3.2 Pulse Duty Cycle

The programmer can choose one of four duty cycles for modulation pulses by setting the appropriate value in the UART_MDR2[5-4] CIR_PULSE_MODE bit field (1/4, 1/3, 5/12, or 1/2).

Figure 12-84 shows the CIR modulation duty cycles.

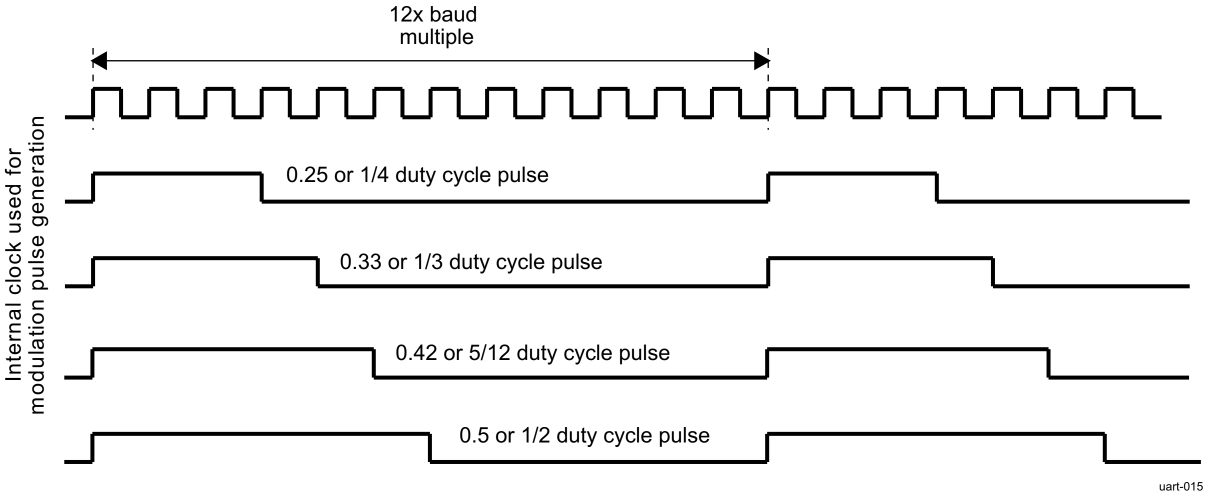

Figure 12-84. CIR Modulation Duty Cycle

The transmission logic ensures that all pulses are transmitted completely (no cutoff during transmission). While transmitting continuous bytes back-to-back, no delay is inserted between 2 transmitted bytes. Thus, software must handle the delay between consecutively transmitted bytes if the receiving end requires it.

12.1.5.2.4.3.3 Consumer IR Encoding/Decoding

There are two methods of encoding for remote-control applications:

- Pulse duration encoding (time-extended bit forms): A variable pulse distance, or duration, in which the difference between logic 1 and logic 0 is the length of the pulse width
- Biphase encoding: The encoding of logic 0 and logic 1 is in the change of signal level from 1 to 0 or 0 to 1, respectively.

Japanese manufacturers favor pulse duration encoding; European manufacturers favor biphase encoding.

CIR mode uses a completely flexible free-format encoding in which 1 is transmitted from the TX FIFO as a modulated pulse with duration *t*.

Similarly, 0 is transmitted as a blank duration T. The Host CPU constructs and deciphers the protocol of the data. For example, the RC-5 protocol using Manchester encoding can be emulated as using a 01 pair for 1 and a 10 pair for 0 (see Figure 12-85).

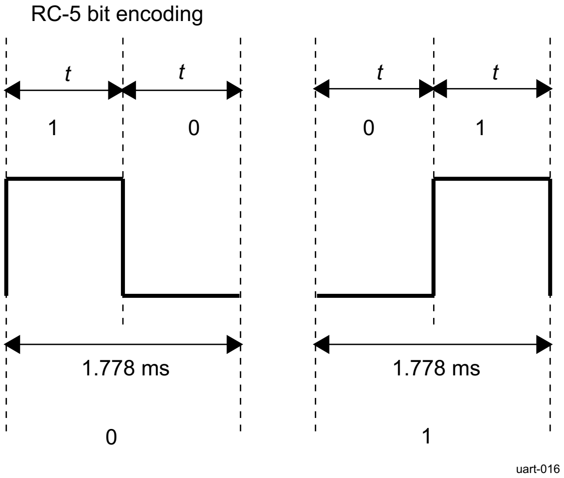

Figure 12-85. UART RC-5 Bit Encoding

Because CIR mode logic does not impose a fixed format for infrared packets of data, the Host CPU software can define the format using simple data structures that are then modulated into an industry standard, such as RC-5 or SIRC. To send a sequence of 0101 in RC-5, the Host CPU software must write an 8-bit binary character of 10011001 to the data FIFO of the UART.

For SIRC, the modulation length (multiples of *t*) is used to distinguish between 1 and 0. The subsequent SIRC digits show the difference in encoding between this and, for example, RC-5. The pulse width is extended for one digit.

Figure 12-86 shows SIRC bit encoding.

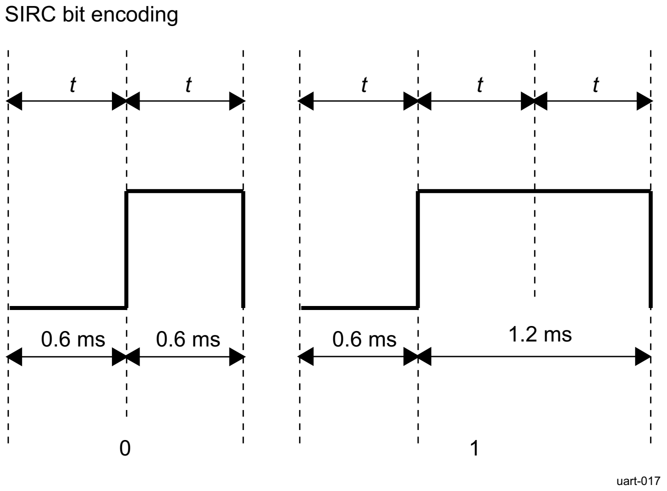

Figure 12-86. UART SIRC Bit Encoding

To construct comprehensive packets constituting remote-control commands, the Host CPU software must combine a number of 8-bit data characters in a sequence that follows one of the universally accepted formats.

Figure 12-87 shows a standard RC-5 frame as detected by UART in CIR mode (the SIRC format follows this). Each field in RC-5 can be considered as two *t* pulses (digital bits) from the TX FIFO.

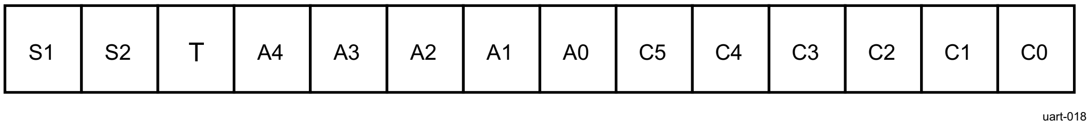

S1	S2	T	A4	A3	A2	A1	A0	C5	C4	C3	C2	C1	C0

Figure 12-87. UART RC-5 Standard Packet Format

Where:

S1, S2:	Start-bits (always 1)
T:	Toggle bit
A4..A0:	Address (or system) bits
C5..C0:	Command bits

The toggle bit T changes when a new command is transmitted to detect when the same key is pressed twice (effectively receiving the same data from the host consecutively). A brief delay in the transmission of the same command is detected by the use of the toggle bit because a code is sent while the Host CPU transmits characters to the UART for transmission. The address bits define the machine or device for which the infrared transmission is intended, and the command defines the operation.

To accommodate an extended RC-5 format, the S2 bit is replaced by an additional command bit (C6) that lets the command range increase to 7 bits. This format is known as the extended RC-5 format.

The SIRC encoding uses the duration of modulation for mark and space; therefore, the duration of data bits in the standard frame length varies.

Figure 12-88 shows the packet format and bit encoding. As Figure 12-89 shows, 1 start-bit of 2.4 ms and control codes are followed by data that constitute the entire frame.

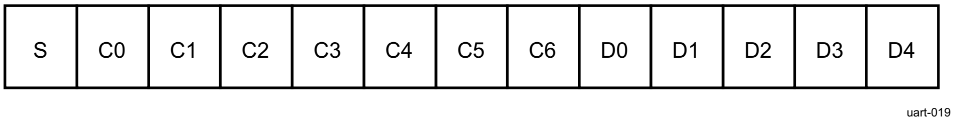

S	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4

Figure 12-88. UART SIRC Packet Format

Note

The encoding must take a standard duration, but the contents of the data can vary. This implies that the control software for sending and receiving data packets must exercise a scheme of interpacket delay, where successive packets can be sent only after a real-time delay expires.

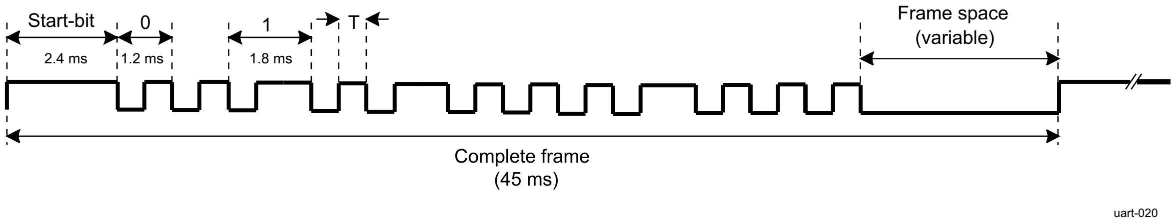

Figure 12-89. UART SIRC Bit Transmission Example

Note

This document does not describe all encoding methods and techniques; the previous information discusses the considerations required to employ different encoding methods for different industry-standard protocols. See industry-standard documentation for specific methods of encoding and protocol use.

12.1.5.3 UART Integration

This section describes UART integration in the device, including information about clocks, resets, and hardware requests.

12.1.5.3.1 UART Integration in MCU Domain

There are two UART modules integrated in the device MCU domain. Figure 12-90 shows the integration of MCU_UART[0-1].

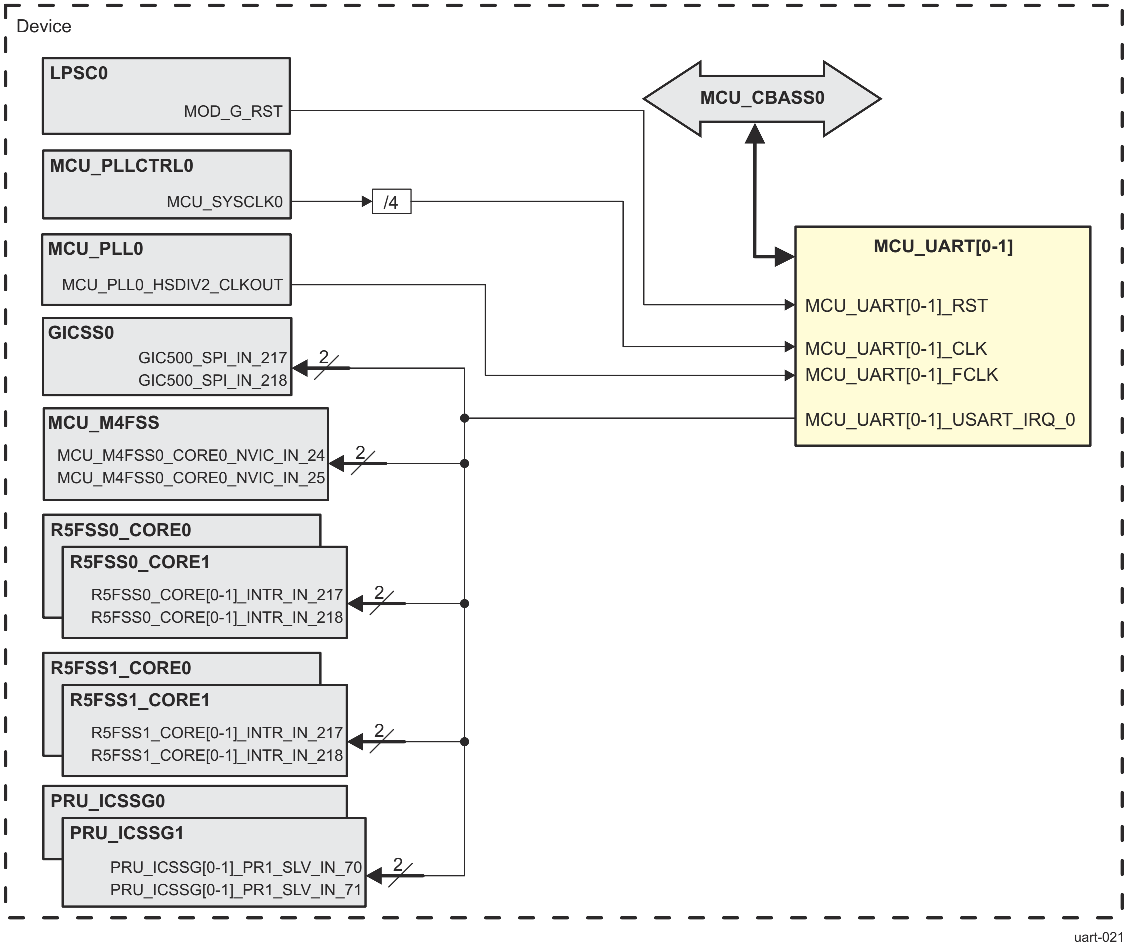

Figure 12-90. MCU_UART[0-1] Integration

Table 12-100 through Table 12-102 summarize the integration of MCU_UART[0-1] in the device MCU domain.

Table 12-100. MCU_UART[0-1] Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect

Table 12-100. MCU_UART[0-1] Integration Attributes (continued)

MCU_UART0	MCU_PSC0	PD0	LPSC0	MCU_CBASS0
MCU_UART1	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-101. MCU_UART[0-1] Clocks and Resets

Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_UART0	MCU_UART0_CLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_UART0 interface clock
	MCU_UART0_FCLK	MCU_PLL0_HSDIV2_CLKOUT	MCU_PLL0	MCU_UART0 functional clock.
MCU_UART1	MCU_UART1_CLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_UART1 interface clock
	MCU_UART1_FCLK	MCU_PLL0_HSDIV2_CLKOUT	MCU_PLL0	MCU_UART1 functional clock.

Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_UART0	MCU_UART0_RST	MOD_G_RST	LPSC0	MCU_UART0 reset
MCU_UART1	MCU_UART1_RST	MOD_G_RST	LPSC0	MCU_UART1 reset

Table 12-102. MCU_UART[0-1] Hardware Requests

Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_UART0	MCU_UART0_USART_IRQ_0	GIC500_SPI_IN_217	GICSS0	MCU_UART0 interrupt request	Level
		MCU_M4FSS0_CORE0_NVIC_IN_24	MCU_M4FSS		
		R5FSS0_CORE0_INTR_IN_217	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_217	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_217	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_217	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_70	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_70	PRU_ICSSG1		
MCU_UART1	MCU_UART1_USART_IRQ_0	GIC500_SPI_IN_218	GICSS0	MCU_UART1 interrupt request	Level
		MCU_M4FSS0_CORE0_NVIC_IN_25	MCU_M4FSS		
		R5FSS0_CORE0_INTR_IN_218	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_218	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_218	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_218	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_71	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_71	PRU_ICSSG1		

DMA Events

Table 12-102. MCU_UART[0-1] Hardware Requests (continued)

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Description	Type
MCU_UART0	-	-	-	No PDMA channels are implemented in the MCU domain.	-
MCU_UART1	-	-	-	No PDMA channels are implemented in the MCU domain.	-

12.1.5.3.2 UART Integration in MAIN Domain

There are seven UART modules integrated in the device MAIN domain - UART0, UART1, UART2, UART3, UART4, UART5, UART6. Figure 12-91 shows the integration of UART[0-6].

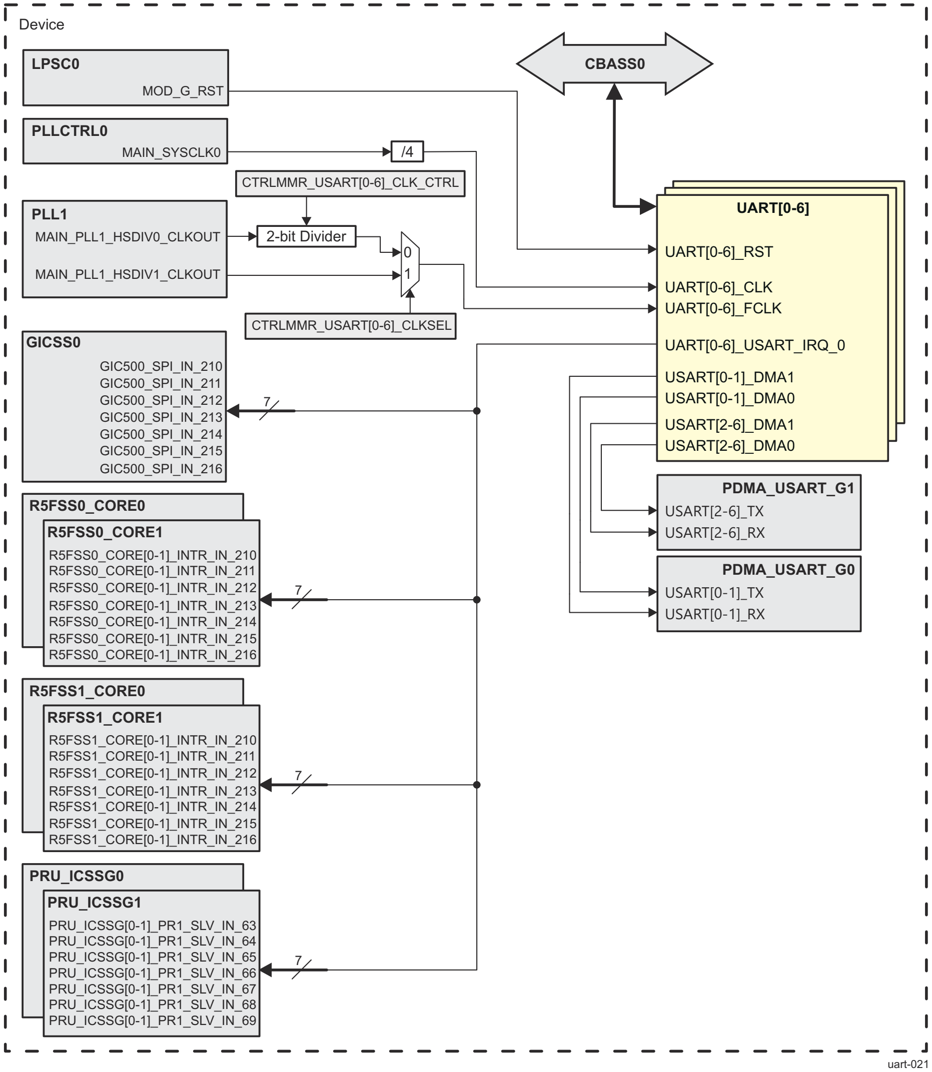

Figure 12-91. UART[0-6] Integration

Table 12-103 through Table 12-105 summarize the integration of UART[0-6] in the device MAIN domain.

Table 12-103. UART Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
UART0	PSC0	PD0	LPSC0	CBASS0
UART1	PSC0	PD0	LPSC0	CBASS0
UART2	PSC0	PD0	LPSC0	CBASS0
UART3	PSC0	PD0	LPSC0	CBASS0
UART4	PSC0	PD0	LPSC0	CBASS0
UART5	PSC0	PD0	LPSC0	CBASS0
UART6	PSC0	PD0	LPSC0	CBASS0

Table 12-104. UART Clocks and Resets

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
UART0	UART0_CLK	MAIN_SYSCLK0/4	PLLCTRL0	UART0 interface clock
	UART0_FCLK	MAIN_PLL1_HSDIV0_CLKOUT/DIV(1)	PLL1	UART0 functional clock. Output of multiplexer, see Figure 12-91, *UART[0-6] Integration*. Multiplexer control is provided via CTRLMMR_USART0_CLKSEL[0] CLK_SEL bit field.
		MAIN_PLL1_HSDIV1_CLKOUT		
UART1	UART1_CLK	MAIN_SYSCLK0/4	PLLCTRL0	UART1 interface clock
	UART1_FCLK	MAIN_PLL1_HSDIV0_CLKOUT/DIV(1)	PLL1	UART1 functional clock. Output of multiplexer, see Figure 12-91, *UART[0-6] Integration*. Multiplexer control is provided via CTRLMMR_USART1_CLKSEL[0] CLK_SEL bit field.
		MAIN_PLL1_HSDIV1_CLKOUT		
UART2	UART2_CLK	MAIN_SYSCLK0/4	PLLCTRL0	UART2 interface clock
	UART2_FCLK	MAIN_PLL1_HSDIV0_CLKOUT/DIV(1)	PLL1	UART2 functional clock. Output of multiplexer, see Figure 12-91, *UART[0-6] Integration*. Multiplexer control is provided via CTRLMMR_USART2_CLKSEL[0] CLK_SEL bit field.
		MAIN_PLL1_HSDIV1_CLKOUT		
UART3	UART3_CLK	MAIN_SYSCLK0/4	PLLCTRL0	UART3 interface clock
	UART3_FCLK	MAIN_PLL1_HSDIV0_CLKOUT/DIV(1)	PLL1	UART3 functional clock. Output of multiplexer, see Figure 12-91, *UART[0-6] Integration*. Multiplexer control is provided via CTRLMMR_USART3_CLKSEL[0] CLK_SEL bit field.
		MAIN_PLL1_HSDIV1_CLKOUT		

Table 12-104. UART Clocks and Resets (continued)

UART4	UART4_CLK	MAIN_SYSCLK0/4	PLLCTRL0	UART4 interface clock
	UART4_FCLK	MAIN_PLL1_HSDIV0_CLKOUT/DIV[1] MAIN_PLL1_HSDIV1_CLKOUT	PLL1	UART4 functional clock. Output of multiplexer, see Figure 12-91, *UART[0-6] Integration*. Multiplexer control is provided via CTRLMMR_USART4_CLKSEL[0] CLK_SEL bit field.
UART5	UART5_CLK	MAIN_SYSCLK0/4	PLLCTRL0	UART5 interface clock
	UART5_FCLK	MAIN_PLL1_HSDIV0_CLKOUT/DIV[1] MAIN_PLL1_HSDIV1_CLKOUT	PLL1	UART5 functional clock. Output of multiplexer, see Figure 12-91, *UART[0-6] Integration*. Multiplexer control is provided via CTRLMMR_USART5_CLKSEL[0] CLK_SEL bit field.
UART6	UART6_CLK	MAIN_SYSCLK0/4	PLLCTRL0	UART6 interface clock
	UART6_FCLK	MAIN_PLL1_HSDIV0_CLKOUT/DIV[1] MAIN_PLL1_HSDIV1_CLKOUT	PLL1	UART6 functional clock. Output of multiplexer, see Figure 12-91, *UART[0-6] Integration*. Multiplexer control is provided via CTRLMMR_USART6_CLKSEL[0] CLK_SEL bit field.

Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
UART0	UART0_RST	MOD_G_RST	LPSC0	UART0 reset
UART1	UART1_RST	MOD_G_RST	LPSC0	UART1 reset
UART2	UART2_RST	MOD_G_RST	LPSC0	UART2 reset
UART3	UART3_RST	MOD_G_RST	LPSC0	UART3 reset
UART4	UART4_RST	MOD_G_RST	LPSC0	UART4 reset
UART5	UART5_RST	MOD_G_RST	LPSC0	UART5 reset
UART6	UART6_RST	MOD_G_RST	LPSC0	UART6 reset

(1) Programmable 2-bit divider. Default set to DIV by 4 (“11”) to get 48 MHz clock.

Table 12-105. UART Hardware Requests

Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART0	UART0_USART_IRQ_0	GIC500_SPI_IN_210	GICSS0	UART0 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_210	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_210	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_210	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_210	R5FSS1_CORE1		

Table 12-105. UART Hardware Requests (continued)

		PRU_ICSSG0_PR1_SLV_IN_63	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_63	PRU_ICSSG1		
UART1	UART1_USART_IRQ_0	GIC500_SPI_IN_211	GICSS0	UART1 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_211	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_211	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_211	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_211	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_64	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_64	PRU_ICSSG1		
UART2	UART2_USART_IRQ_0	GIC500_SPI_IN_212	GICSS0	UART2 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_212	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_212	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_212	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_212	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_65	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_65	PRU_ICSSG1		
UART3	UART3_USART_IRQ_0	GIC500_SPI_IN_213	GICSS0	UART3 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_213	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_213	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_213	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_213	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_66	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_66	PRU_ICSSG1		
UART4	UART4_USART_IRQ_0	GIC500_SPI_IN_214	GICSS0	UART4 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_214	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_214	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_214	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_214	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_67	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_67	PRU_ICSSG1		
UART5	UART5_USART_IRQ_0	GIC500_SPI_IN_215	GICSS0	UART5 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_215	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_215	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_215	R5FSS1_CORE0		

Table 12-105. UART Hardware Requests (continued)

		R5FSS1_CORE1_INTR_IN_215	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_68	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_68	PRU_ICSSG1		
UART6	UART6_USART_IRQ_0	GIC500_SPI_IN_216	GICSS0	UART6 interrupt request	Level
		R5FSS0_CORE0_INTR_IN_216	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_216	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_216	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_216	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_69	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_69	PRU_ICSSG1		
DMA Events					
Module Instance	**Module DMA Event**	**Destination DMA Event Input**	**Destination**	**Description**	**Type**
UART0	USART0_DMA0	USART0_TX	PDMA_USART_G0	UART0 transmit request line	Level
	USART0_DMA1	USART0_RX	PDMA_USART_G0	UART0 receive request line	Level
UART1	USART1_DMA0	USART1_TX	PDMA_USART_G0	UART1 transmit request line	Level
	USART1_DMA1	USART1_RX	PDMA_USART_G0	UART1 receive request line	Level
UART2	USART2_DMA0	USART2_TX	PDMA_USART_G1	UART2 transmit request line	Level
	USART2_DMA1	USART2_RX	PDMA_USART_G1	UART2 receive request line	Level
UART3	USART3_DMA0	USART3_TX	PDMA_USART_G1	UART3 transmit request line	Level
	USART3_DMA1	USART3_RX	PDMA_USART_G1	UART3 receive request line	Level
UART4	USART4_DMA0	USART4_TX	PDMA_USART_G1	UART4 transmit request line	Level
	USART4_DMA1	USART4_RX	PDMA_USART_G1	UART4 receive request line	Level
UART5	USART5_DMA0	USART5_TX	PDMA_USART_G1	UART5 transmit request line	Level
	USART5_DMA1	USART5_RX	PDMA_USART_G1	UART5 receive request line	Level
UART6	USART6_DMA0	USART6_TX	PDMA_USART_G1	UART6 transmit request line	Level
	USART6_DMA1	USART6_RX	PDMA_USART_G1	UART6 receive request line	Level

12.1.5.4 UART Functional Description

12.1.5.4.1 UART Block Diagram

The UART module can be divided into three main blocks:

- FIFO management
- Mode selection
- Protocol formatting

FIFO management is common to all functions and enables the transmission and reception of data from the host processor point of view.

There are two modes:

- Function mode: Routes the data to the chosen function (UART, RS-485, IrDA, or CIR) and enables the mechanism corresponding to the chosen function.
- Register mode: Enables conditional access to registers.

For more information about mode configuration, see *Mode Selection*.

Protocol formatting has three subcategories:

- Clock generation: The 48-MHz input clock generates all necessary clocks.
- Data formatting: Each function uses a dedicated state-machine that is responsible for the transition between FIFO data and the associated frame data.
- Interrupt management: Different interrupt types are generated depending on the chosen function. In each mode, when an interrupt is generated, the UART_IIR_UART register indicates the interrupt type.
  - UART mode interrupts: Seven interrupts prioritized in six different levels
  - IrDA mode interrupts: Eight interrupts. The interrupt line is activated when any interrupt is generated (there is no priority).
  - CIR mode interrupts: A subset of existing IrDA mode interrupts is used.

In parallel with these functional blocks, a power-saving strategy exists for each function.

The UART block diagram is shown below.

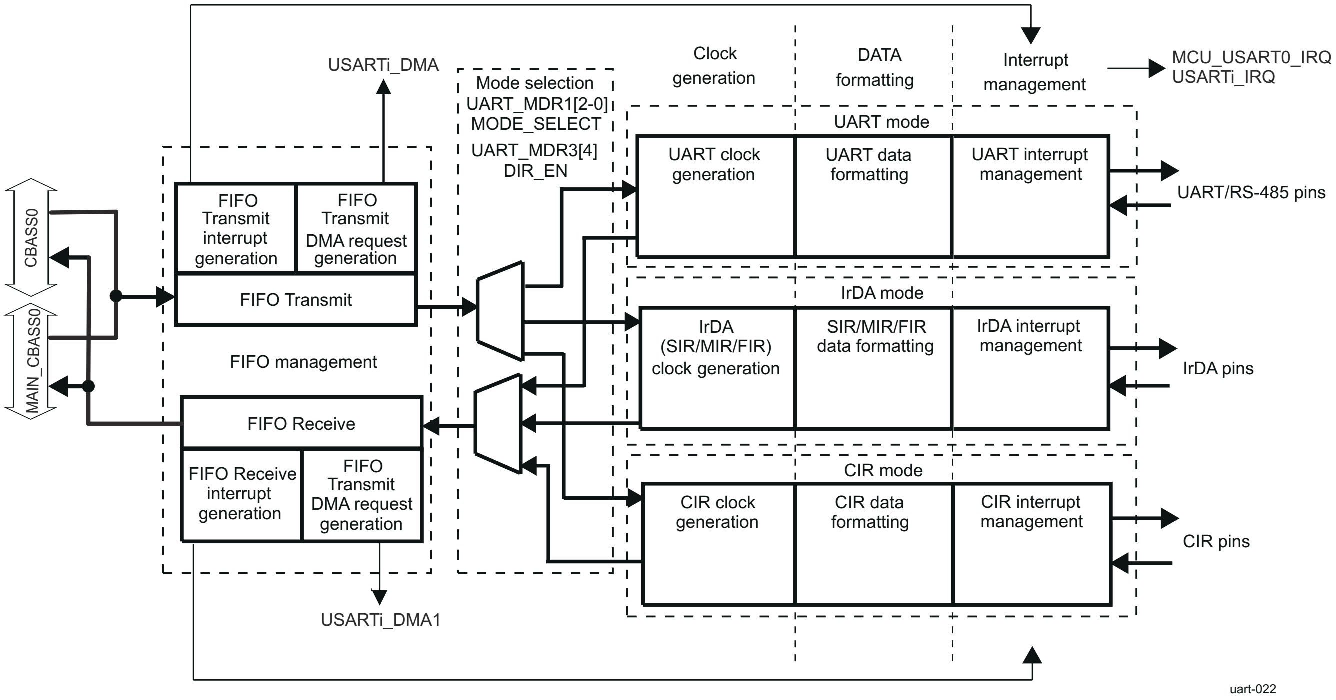

Figure 12-92. UART Functional Block Diagram

12.1.5.4.2 UART Clock Configuration

Each UART uses a 48-MHz functional clock for its logic and to generate external interface signals. Each UART uses an interface clock for register accesses.

12.1.5.4.3 UART Software Reset

The UART_SYSC[1] SOFTRESET bit controls the software reset; setting this bit to 1 triggers a software reset functionally equivalent to hardware reset.

12.1.5.4.3.1 Independent TX/RX

The receiver and transmitter are enabled by default after reset. Software can choose to disable, re-enable or to reset either the RX or the TX side independently of the other through the UART_ECR register.

12.1.5.4.4 UART Power Management

12.1.5.4.4.1 UART Mode Power Management

12.1.5.4.4.1.1 Module Power Saving

In UART modes, sleep mode is enabled by setting the UART_IER_UART[4] SLEEP_MODE bit to 1 (when the UART_EFR[4] ENHANCED_EN bit is set to 1).

Sleep mode is entered when all of the following conditions exist:

- The serial data input line, RX, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.
- The only pending interrupts are THR interrupts.

Sleep mode is a good way to lower UART power consumption, but this state can be achieved only when the UART is set to modem mode. Therefore, even if the UART has no key role functionally, it must be initialized in a functional mode to take advantage of sleep mode.

In sleep mode, the module clock and baud rate clock are stopped internally. Because most registers are clocked by these clocks, this greatly reduces power consumption. The module wakes up when a change is detected on the RX line, when data is written to the TX FIFO, and when there is a change in the state of the modem input pins.

An interrupt can be generated on a wake-up event by setting the UART_SCR[4] RX_CTS_WU_EN bit to 1. To understand how to manage the interrupt, see Section 12.1.5.4.5.1.2 , *Wake-Up Interrupt*.

Note

There must be no writing to the divisor latches, UART_DLL and UART_DLH, to set the baud clock (BCLK) while in sleep mode. It is advisable to disable sleep mode using the UART_IER_UART[4] SLEEP_MODE bit before writing to the UART_DLL or UART_DLH register.

12.1.5.4.4.1.2 System Power Saving

Sleep and auto-idle modes are embedded power-saving features. Power-reduction techniques can be applied at the system level by shutting down certain internal clock and power domains of the device.

For more information, see *Power*, in the *Device Configuration*.

12.1.5.4.4.2 IrDA Mode Power Management

12.1.5.4.4.2.1 Module Power Saving

In IrDA modes, sleep mode is enabled by setting the UART_MDR1[3] IR_SLEEP bit to 1.

Sleep mode is entered when all of the following conditions exist:

- The serial data input line, RXD, is idle.
- The TX FIFO and TX shift register are empty.

- The RX FIFO is empty.
- No interrupts are pending except THR interrupts.

The module wakes up when a change is detected on the RXD line or when data is written to the TX FIFO.

12.1.5.4.4.2.2 System Power Saving

System power saving for the IrDA mode has the same function as for the UART mode (see Section 12.1.5.4.4.1.2 , *System Power Saving*).

12.1.5.4.4.3 CIR Mode Power Management

12.1.5.4.4.3.1 Module Power Saving

Module power saving for the CIR mode has the same function as for the IrDA mode (see Section 12.1.5.4.4.2.1 , *Module Power Saving*).

12.1.5.4.4.3.2 System Power Saving

System power saving for the CIR mode has the same function as for the UART mode (see Section 12.1.5.4.4.1.2 , *System Power Saving*).

12.1.5.4.4.4 Local Power Management

Table 12-106 describes power-management features available for the UART.

> **Note**
>
> For information about source clock gating and the sleep/wake-up transitions description, see *Power*, in the *Device Configuration*.

Table 12-106. UART Local Power-Management Features

Feature	Registers	Description
Clock autogating		
Peripheral idle modes		
Clock activity	N/A	Feature not available
Controller standby modes	N/A	Feature not available
Global wake-up enable	UART_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.
Wake-Up sources enable	N/A	Feature not available

12.1.5.4.5 UART Interrupt Requests

12.1.5.4.5.1 UART Mode Interrupt Management

12.1.5.4.5.1.1 UART Interrupts

The UART mode includes seven possible interrupts prioritized to six levels.

When an interrupt is generated, the interrupt identification register (UART_IIR_UART) sets the UART_IIR_UART[0] IT_PENDING bit to 0 to indicate that an interrupt is pending, and indicates the type of interrupt through the UART_IIR_UART[5-1] bit field. Table 12-107 summarizes the interrupt control functions.

Table 12-107. UART Mode Interrupts

IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
000001	N/A	No Interrupt	N/A	N/A
000110	1	Receiver line status	OE, FE, PE, or BI errors occur in characters in the RX FIFO.	FE, PE, BI: Read the UART_RHR register. OE: Read the UART_LSR_UART register.

Table 12-107. UART Mode Interrupts (continued)

IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
001100	2	RX time-out	Stale data in RX FIFO	Read the UART_RHR register if using the default timeout behavior: EFR2[6]=0 Cleared by reading its value (IIR) if using the periodic timeout behavior: EFR2[6]=1
000100	2	RHR interrupt	DRDY (data ready) (FIFO disabled) RX FIFO above trigger level (FIFO enabled)	Read the UART_RHR register until the interrupt condition disappears
000010	3	THR interrupt	TFE (THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR until the interrupt condition disappears
000000	4	Modem status	See the UART_MSR register.	Read the MSR register
010000	5	XOFF interrupt/ special character interrupt	Receive XOFF characters/special character	Receive XON character(s), if XOFF interrupt/read of the UART_IIR_UART register, if special character interrupt
100000	6	CTS, RTS	RTS pin or CTS pin change state from active (low) to inactive (high)	Read the UART_IIR_UART register

For the receiver-line status interrupt, the UART_LSR_UART[7] RX_FIFO_STS bit generates the interrupt.

For the XOFF interrupt, if an XOFF flow character detection caused the interrupt, the interrupt is cleared by an XON flow character detection. If special character detection caused the interrupt, the interrupt is cleared by a read of the UART_IIR_UART register.

12.1.5.4.5.1.2 Wake-Up Interrupt

Wake-up interrupt is a special interrupt that works differently from other interrupts. This interrupt is enabled when the RX_CTS_DSR_WAKE_UP_ENABLE bit of the Supplementary Control Register (SCR[4]) is set to 1. The IIR register is not modified when it occurs, SSR[1] must be checked to detect a wake-up event. When a wake-up event occurs, the only way to clear it is to reset SCR[4] to 0. Wake-up can also occur if the WER[7] TX_WAKEUP_EN is set to 1 and one of the following events occurs:

1. THR interrupt is enabled and occurs (omitted if TX DMA request is enabled)
2. TX DMA request is enabled and occurs
3. TX_STATUS_IT is enabled and occurs (only IrDA and CIR modes). Cannot be used with THR Interrupt.

12.1.5.4.5.2 IrDA Mode Interrupt Management

12.1.5.4.5.2.1 IrDA Interrupts

The IrDA function generates interrupts. All interrupts can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART_IER_IRDA). The interrupt status of the device can be checked by reading the interrupt identification register (UART_IIR_IRDA).

The UART, IrDA, and CIR modes have different interrupts in the UART module and, therefore, different UART_IER_IRDA and UART_IIR_IRDA mappings, depending on the selected mode.

The IrDA modes have eight possible interrupts (see Table 12-108). The interrupt line is activated when any interrupt is generated (there is no priority).

Table 12-108. IrDA Mode Interrupts

IIR_IRDA Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	RHR interrupt	DRDY (data ready) (FIFO disabled) RX FIFO above trigger level (FIFO enabled)	Read the UART_RHR register until the interrupt condition disappears.
1	THR interrupt	TFE (UART_THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR until the interrupt condition disappears.

Table 12-108. IrDA Mode Interrupts (continued)

IIR_IRDA Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
2	Last byte in RX FIFO	Last byte of frame in RX FIFO is available to be read at the UART_RHR port.	Read the UART_RHR register.
3	RX overrun	Write to the UART_RHR register when the RX FIFO is full.	Read UART_RESUME register.
4	Status FIFO interrupt	Status FIFO triggers level reached.	Read STATUS FIFO.
5	TX status	UART_THR empty before EOF sent. Last bit of transmission of the IrDA frame occurred, but with an underrun error OR Transmission of the last bit of the IrDA frame completed successfully.	Read the UART_RESUME register OR Read the UART_IIR_IRDA register.
6	Receiver line status interrupt	CRC, ABORT, or frame-length error is written into the STATUS FIFO.	Read the STATUS FIFO (read until empty - maximum of eight reads required).
7	Received EOF	Received end-of-frame	Read the UART_IIR_IRDA register.

12.1.5.4.5.2.2 Wake-Up Interrupts

The wake-up interrupt for IrDA mode has the same function as that for UART mode (see Section 12.1.5.4.5.1.2 , *Wake-Up Interrupt*).

12.1.5.4.5.3 CIR Mode Interrupt Management

12.1.5.4.5.3.1 CIR Interrupts

The CIR function generates interrupts that can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART_IER_CIR). The interrupt status of the device can be checked by reading the interrupt identification register (UART_IIR_CIR).

The UART, IrDA, and CIR modes have different interrupts in the UART module and, therefore, different UART_IER_CIR and UART_IIR_CIR mappings, depending on the selected mode.

Table 12-109 lists the interrupt modes to be maintained. In CIR mode, the sole purpose of the UART_IIR_CIR[5] TX_STATUS_IT bit is to indicate that the last bit of infrared data was passed to the TX pin.

Table 12-109. CIR Mode Interrupts

IIR_CIR Bit Number	Interrupt Type	Interrupt Source	Interrupt Reset Method
0			
1	THR interrupt	TFE (THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR register until the interrupt condition disappears
2			
3			
4	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
5	TX status	Transmission of the last bit of the frame is complete successfully	Read the UART_IIR_CIR register
6	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
7	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode

12.1.5.4.5.3.2 Wake-Up Interrupts

The wake-up interrupt for CIR mode has the same function as that for UART mode (see Section 12.1.5.4.5.1.2 , *Wake-Up Interrupt*).

12.1.5.4.6 UART FIFO Management

The FIFO is accessed by reading and writing the UART_RHR and UART_THR registers. Parameters are controlled using the FIFO control register (UART_FCR) and supplementary control register (UART_SCR). Reading the UART_SSR[0] TX_FIFO_FULL bit at 1 means the FIFO is full.

The UART_TLR register controls the FIFO trigger level, which enables DMA and interrupt generation. After reset, transmit (TX) and receive (RX) FIFOs are disabled; thus, the trigger level is the default value of 1 byte. Figure 12-93 shows the FIFO management registers.

Note

Data in the UART_RHR register is not overwritten when an overflow occurs.

Note

The UART_SFLSR, UART_SFREGL, and UART_SFREGH status registers are used in IrDA mode only. For information about their use, see Section 12.1.5.4.8.3.3 , *IrDA Data Formatting*.

Note

Bits UART_FCR[2] TX_FIFO_CLEAR and UART_FCR[1] RX_FIFO_CLEAR are automatically cleared by hardware after 4 × UARTi_CLK + 5 × UARTi_FCLK clock cycles. This delay is needed to finish the resetting of the corresponding FIFO and DMA control registers.

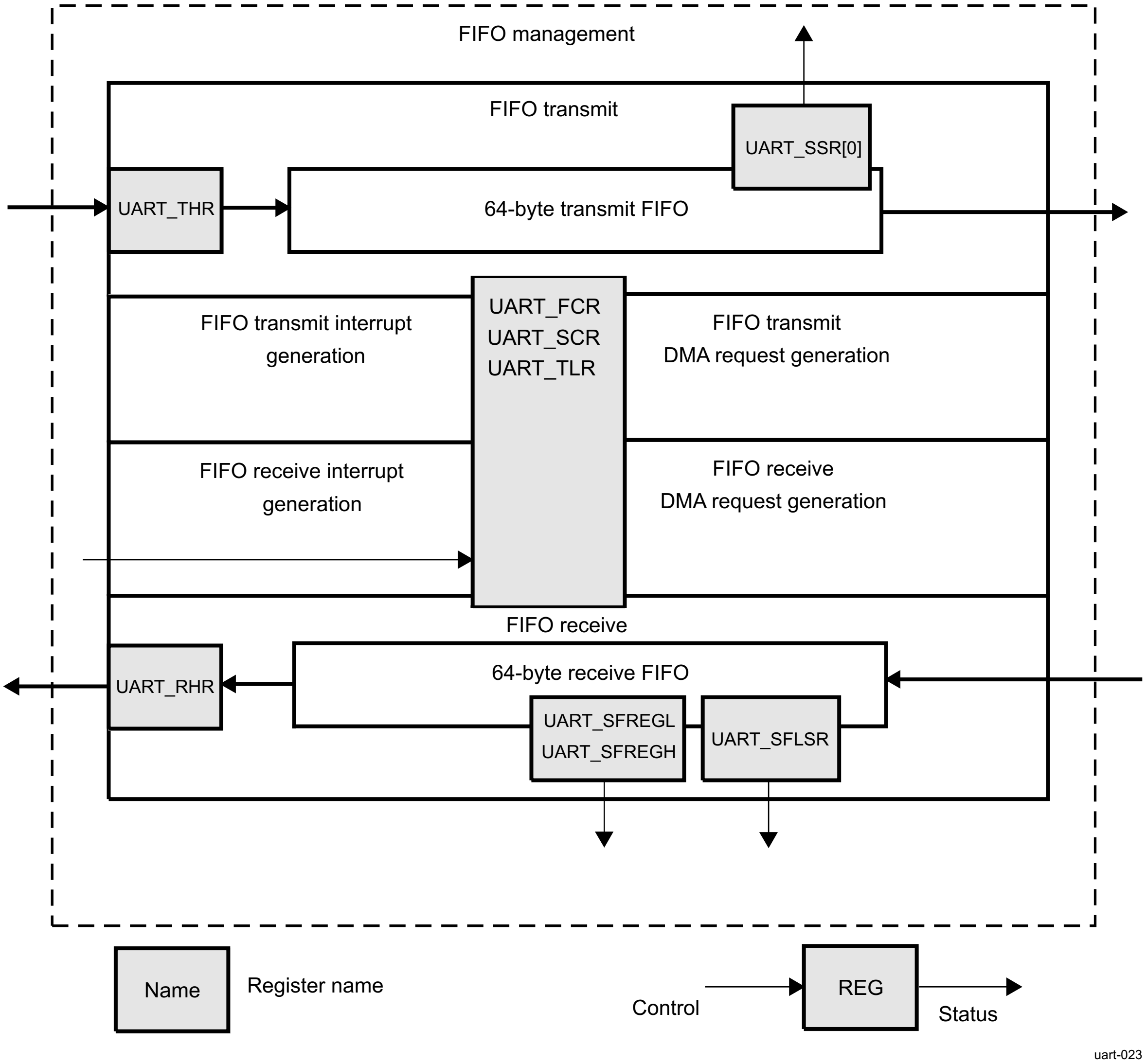

Figure 12-93. UART FIFO Management Registers

12.1.5.4.6.1 FIFO Trigger

12.1.5.4.6.1.1 Transmit FIFO Trigger

Table 12-110 lists the TX FIFO trigger level settings.

Table 12-110. UART TX FIFO Trigger Level Setting Summary

SCR[6]	TLR[3:0]	TX FIFO Trigger Level
0	= 0x0	Defined by the UART_FCR[5-4] TX_FIFO_TRIG bit field (8,16, 32, or 56 spaces)
0	!= 0x0	Defined by the UART_TLR[3-0] TX_FIFO_TRIG_DMA bit field (from 4 to 60 spaces with a granularity of 4 spaces)
1	Value	Defined by the concatenated value of TLR[3:0] (higher bits) and FCR[5:4] (lower bits) from 1 to 63 spaces with a granularity of 1 space. **Note:** The combination of TLR[3:0]=0000 and FCR[5:4]=00 (all zeros) is not supported (min 1 space required). All zeros will result in unsupported behavior.

12.1.5.4.6.1.2 Receive FIFO Trigger

Table 12-111 lists the RX FIFO trigger-level settings.

Table 12-111. UART RX FIFO Trigger-Level Setting Summary

SCR[7]	TLR[7:4]	RX FIFO Trigger Level
0	= 0x0	Defined by the UART_FCR[7-6] RX_FIFO_TRIG bit field (8,16, 56, or 60 characters)
0	!= 0x0	Defined by the UART_TLR[7-4] RX_FIFO_TRIG_DMA bit field (from 4 to 60 characters with a granularity of 4 characters)
1	Value	Defined by the concatenated value of TLR[7:4] and FCR[7:6] from 1 to 63 characters with a granularity of one character. **Note:** The combination of TLR[7:4]=0000 and FCR[7:6]=00 (all zeros) is not supported (min 1 character required). All zeros will result in unsupported behavior.

The receive threshold is programmed using the UART_TCR[7-4] RX_FIFO_TRIG_START and UART_TCR[3-0] RX_FIFO_TRIG_HALT bit fields:

- Trigger levels from 0 to 60 bytes are available with a granularity of 4 (trigger level = 4 × [4-bit register value]).
- To ensure correct device operation, ensure that RX_FIFO_TRIG_HALT > RX_FIFO_TRIG when auto-RTS is enabled.

  Delay = [4 + 16 × (1 + CHAR_LENGTH + Parity + Stop – 0.5)] × Baud_rate + 4 × FCLK

  Note

  The RTS signal is deasserted after the UART module receives the data over RX_FIFO_TRIG_HALT. Delay means how long the UART module takes to deassert the RTS signal after reaching RX_FIFO_TRIG_HALT.

- In FIFO interrupt mode with flow control, ensure that the trigger level to HALT transmission is greater than or equal to the RX FIFO trigger level (the UART_TCR[7-4] RX_FIFO_TRIG_START bit field or the UART_FCR[7-6] RX_FIFO_TRIG bit field); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist, because a DMA request is sent when a byte is received.

12.1.5.4.6.2 FIFO Interrupt Mode

In FIFO interrupt mode (the FIFO control register UART_FCR[0] FIFO_EN bit is set to 1 and relevant interrupts are enabled by the UART_IER_UART register), an interrupt signal informs the processor of the status of the receiver and transmitter. These interrupts are raised when the RX/TX FIFO threshold (the UART_TLR[7-4] RX_FIFO_TRIG_DMA and UART_TLR[3-0] TX_FIFO_TRIG_DMA bit fields or the UART_FCR[7-6] RX_FIFO_TRIG and UART_FCR[5-4] TX_FIFO_TRIG bit fields, respectively) is reached.

The interrupt signals instruct the Host CPU to transfer data to the destination (from the UART in receive mode and/or from any source to the UART FIFO in transmit mode).

When UART flow control is enabled with interrupt capabilities, the UART flow control FIFO threshold (the UART_TCR[3-0] RX_FIFO_TRIG_HALT bit field) must be greater than or equal to the RX FIFO threshold.

Figure 12-94 shows the generation of the RX FIFO interrupt request.

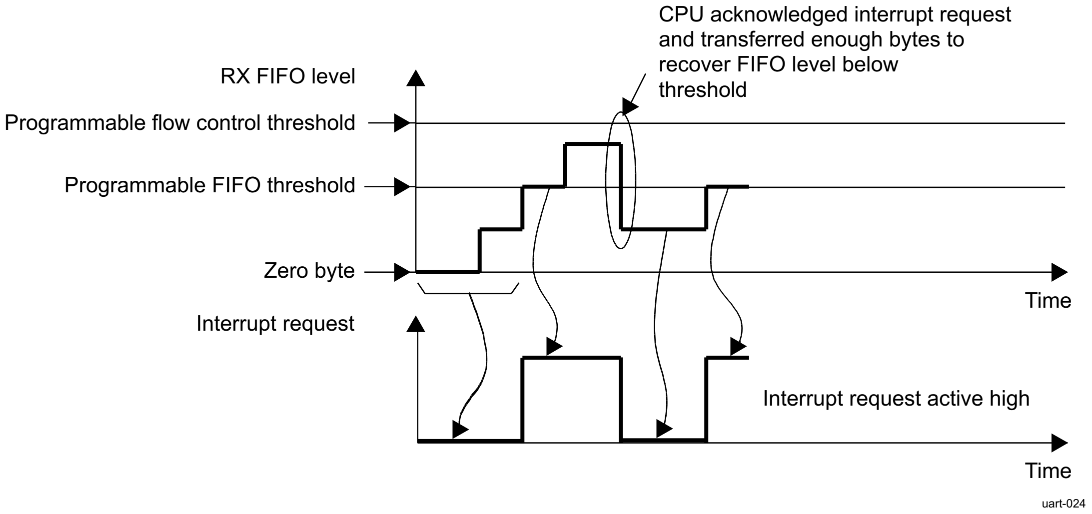

Figure 12-94. UART RX FIFO Interrupt Request Generation

In receive mode, no interrupt is generated until the RX FIFO reaches its threshold. Once low, the interrupt can be deasserted only when the Host CPU has handled enough bytes to put the FIFO level below threshold. The flow control threshold is set at a higher value than the FIFO threshold.

Figure 12-95 shows the generation of the TX FIFO interrupt request.

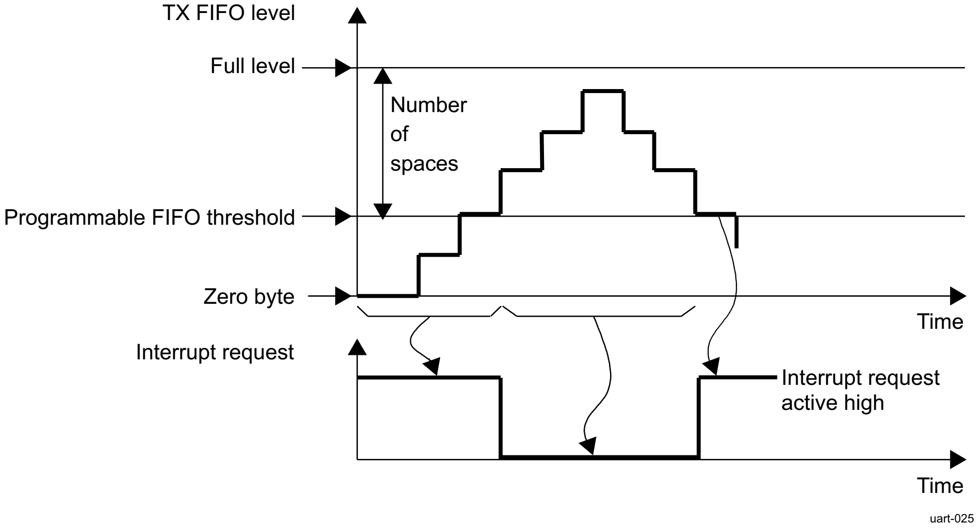

Figure 12-95. UART TX FIFO Interrupt Request Generation

In transmit mode, an interrupt request is automatically asserted when the TX FIFO is empty. This request is deasserted when the TX FIFO crosses the threshold level. The interrupt line is deasserted until a sufficient number of elements is transmitted to go below the TX FIFO threshold.

12.1.5.4.6.3 FIFO Polled Mode Operation

In FIFO polled mode (the UART_FCR[0] FIFO_EN bit is set to 0 and the relevant interrupts are disabled by the UART_IER_UART register), the status of the receiver and transmitter can be checked by polling the line status register (UART_LSR_UART).

This mode is an alternative to the FIFO interrupt mode of operation in which the status of the receiver and transmitter is automatically determined by sending interrupts to the Host CPU.

12.1.5.4.6.4 FIFO DMA Mode Operation

Although the DMA operation includes four modes (DMA modes 0 through 3), the information in *UART Hardware Requests*, assumes that mode 1 is used. (Mode 2 and mode 3 are legacy modes that use only one DMA request for each module.)

In mode 2, the remaining DMA request is used for RX. In mode 3, the remaining DMA request is used for TX.

DMA requests in mode 2 and mode 3 use the USARTi_DMA0 signals (where i = 0 to 6.

The USARTi_DMA1 (where i = 0 to 6)

The DMA mode and signals usage can be selected as follows:

- When SCR[0]=0:
  - Setting FCR[3] to 0 enables DMA mode 0
  - Setting FCR[3] to 1 enables DMA mode 1
- When SCR[0]=1:
  - SCR[2:1] determines DMA mode 0 to 3 according to the Supplementary Control Register (SCR) description.

For example:

- If no DMA operation is desired: set SCR[0] to 1 and SCR[2:1] to 00 (FCR[3] is discarded)
- If DMA mode 1 is desired: either set SCR[0] to 0 and FCR[3] to 1 or set SCR[0] to 1 and SCR[2:1] to 01 (FCR[3] is discarded)

If the FIFOs are disabled (FCR[0]=0), DMA operations occur in single character transfers.

Note that when DMA Mode 0 has been programmed, the signals associated with DMA operation are not active.

Depending on UART_MDR3[2] SET_DMA_TX_THRESHOLD, the threshold can be programmed different ways:

- SET_TX_DMA_THRESHOLD = 1:

  The threshold value will be the value of the UART_TX_DMA_THRESHOLD register. If SET_TX_DMA_THRESHOLD + TX trigger spaces 64, then the default method of threshold is used: threshold value = TX FIFO size.
- SET_TX_DMA_THRESHOLD = 0:

  The threshold value = TX FIFO size TX trigger space. The TX DMA line is asserted if the TX FIFO level is lower then the threshold. It remains asserted until TX trigger spaces number of bytes are written into the FIFO. The DMA line is then deasserted and the FIFO level is compared with the threshold value.

12.1.5.4.6.4.1 DMA sequence to disable TX DMA

In order to disable TX DMA if it is not needed anymore (e.g. all transfers are done and UART idle mode is desired), the following sequence must be use

1. DMA mode 1 is set (both TX/RX DMA) by registers UART_SCR[0] DMA_MODE_CTL = 0 and UART_FCR[3] DMA_MODE = 1:
   a. Set the UART_SCR[2-1] DMA_MODE_2 bit fields to 01 (DMA mode 1)
   b. Set the UART_SCR[0] DMA_MODE_CTL bit to1 (this setting of UART_SCR[0] DMA_MODE-CTL will ignores UART_FCR[3] DMA_MODE_CTL bit)

   Note

   It is strongly suggested to do steps ‘a’ and ‘b’ in two separate write in order to avoid malfunction of the device.

   c. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

---

Note

There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

---

d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
f. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
g. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.

2. DMA mode 1 is set (both TX/RX DMA) by registers UART_FCR[3] DMA_MODE = 0 and UART_SCR[0] DMA_MODE_CTL = 1, UART_SCR[2-1] DMA_MODE_2 = 01. It is almost the same as above, but steps ‘a’, and ‘b’ can be skipped:
   a. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

---

Note

There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

---

   b. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
   c. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
   d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
   e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.
3. DMA mode 3 is set (TX DMA only) by registers UART_FCR[3] DMA_MODE = 0 and UART_SCR[0] DMA_MODE_CTL = 1, UART_SCR[2-1] DMA_MODE_2 = 11. It is the same as above:
   a. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

---

Note

There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

---

   b. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
   c. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
   d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
   e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.

12.1.5.4.6.4.2 DMA Transfers (DMA Mode 1, 2, or 3)

Figure 12-96 through Figure 12-99 show the supported DMA operations.

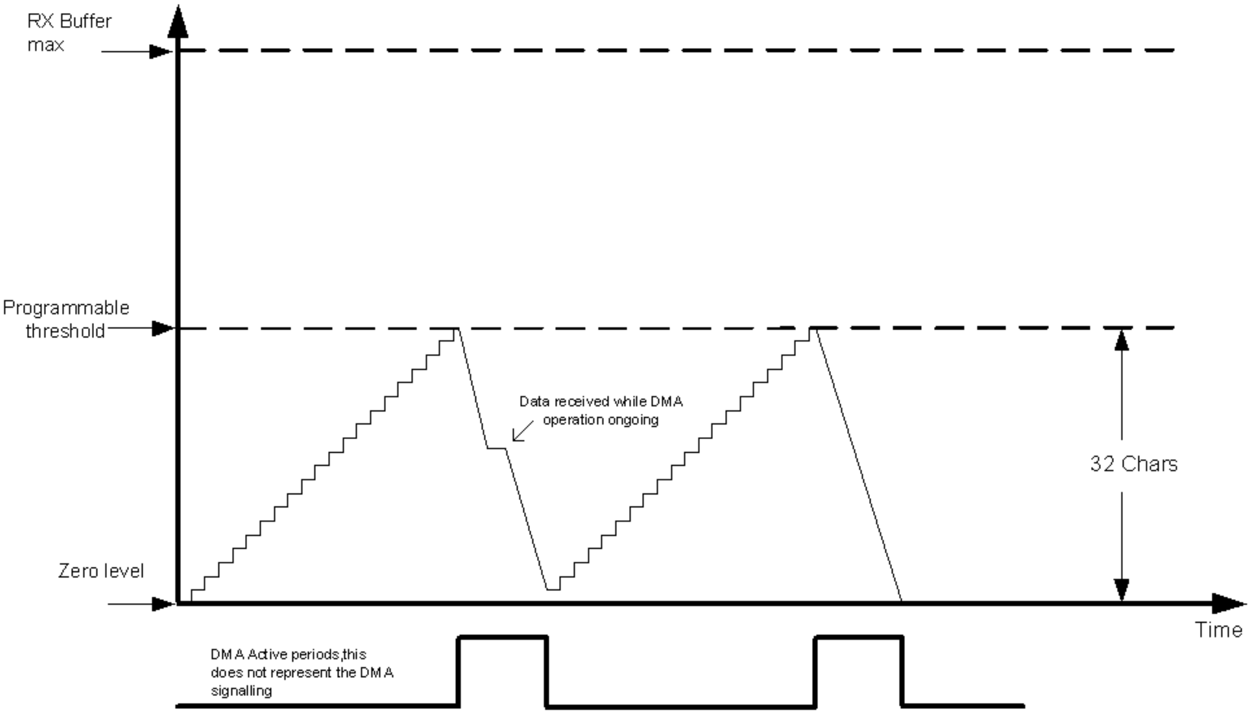

Figure 12-96. UART Receive FIFO DMA Request Generation (32 Characters)

In receive mode, a DMA request is generated when the RX FIFO reaches its threshold level defined in the trigger level register (UART_TLR). This request is deasserted when the number of bytes defined by the threshold level is read by the device DMA controllers.

In transmit mode, a DMA request is automatically asserted when the TX FIFO is empty. This request is deasserted when the number of bytes defined by the number of spaces in the UART_TLR register is written by the device DMA controllers. If an insufficient number of characters is written, the DMA request stays active.

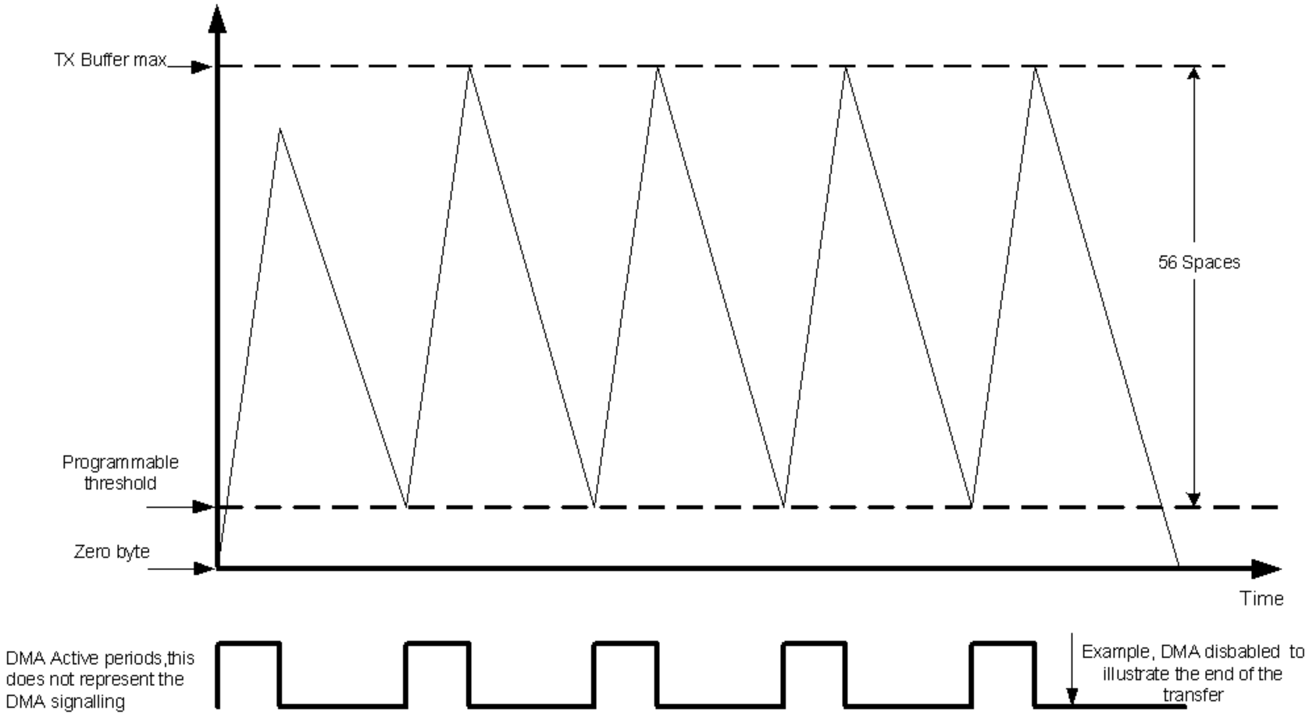

Figure 12-97. UART Transmit FIFO DMA Request Generation (56 Spaces)

The DMA request is again asserted if the FIFO can receive the number of bytes defined by the UART_TLR register.

The threshold can be programmed in a number of ways. Figure 12-97 shows a DMA transfer operating with a space setting of 56 that can arise from using the auto settings in the UART_FCR[5-4] TX_FIFO_TRIG bit field or the UART_TLR[3-0] TX_FIFO_TRIG_DMA bit field concatenated with the TX_FIFO_TRIG bit field.

The setting of 56 spaces in the UART module must correlate with the settings of the device DMA controllers, so that the buffer does not overflow (program the DMA request size of the LH controller to equal the number of spaces in the UART module).

Figure 12-98 shows an example with eight spaces to show the buffer level crossing the space threshold. The LH DMA controller settings must correspond to those of the UART module.

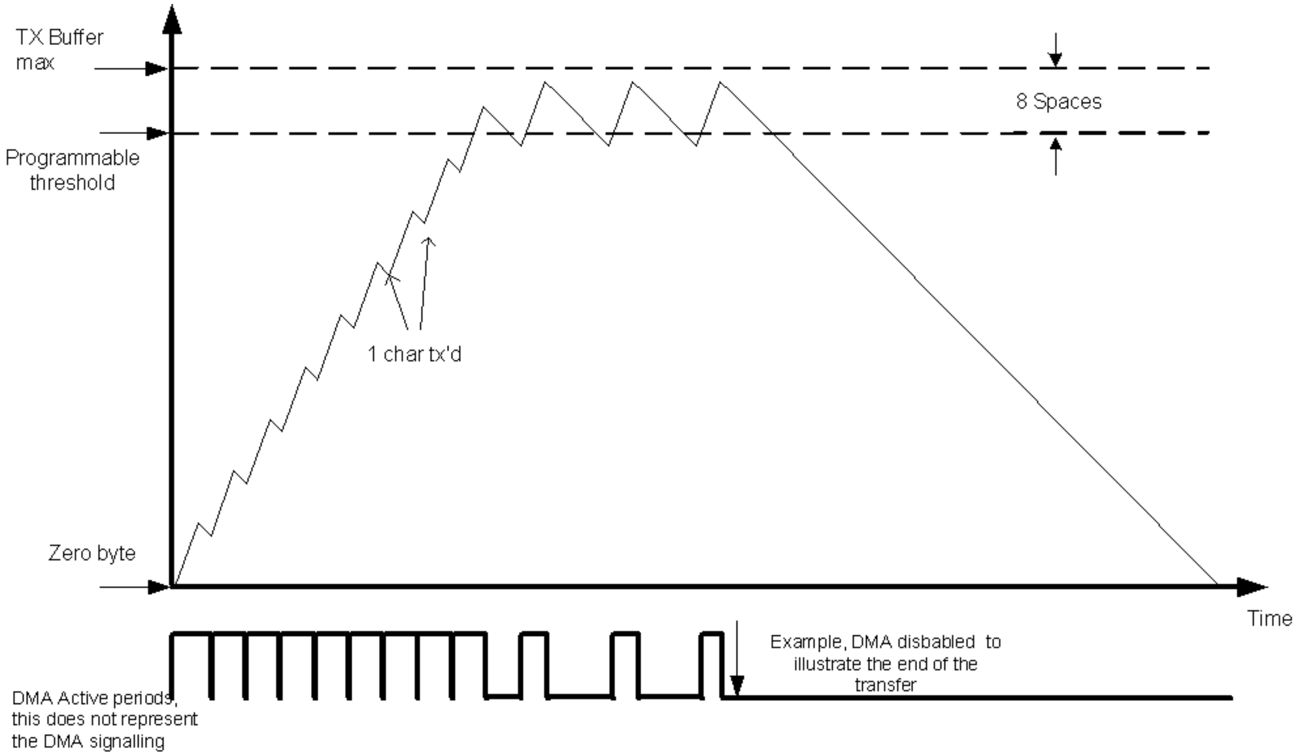

Figure 12-98. UART Transmit FIFO DMA Request Generation (8 Spaces)

The next example shows the setting of one space that uses the DMA for each transfer of one character to the transmit buffer (see Figure 12-99). The buffer is filled faster than the baud rate at which data is transmitted to the TX pin. Eventually, the buffer is completely full and the DMA operations stop transferring data to the transmit buffer.

On two occasions, the buffer holds the maximum amount of data words; shortly after this, the DMA is disabled to show the slower transmission of the data words to the TX pin. Eventually, the buffer is emptied at the rate specified by the baud rate settings of the UART_DLL and UART_DLH registers.

The DMA settings must correspond to the system LH DMA controller settings to ensure correct operation of this logic.

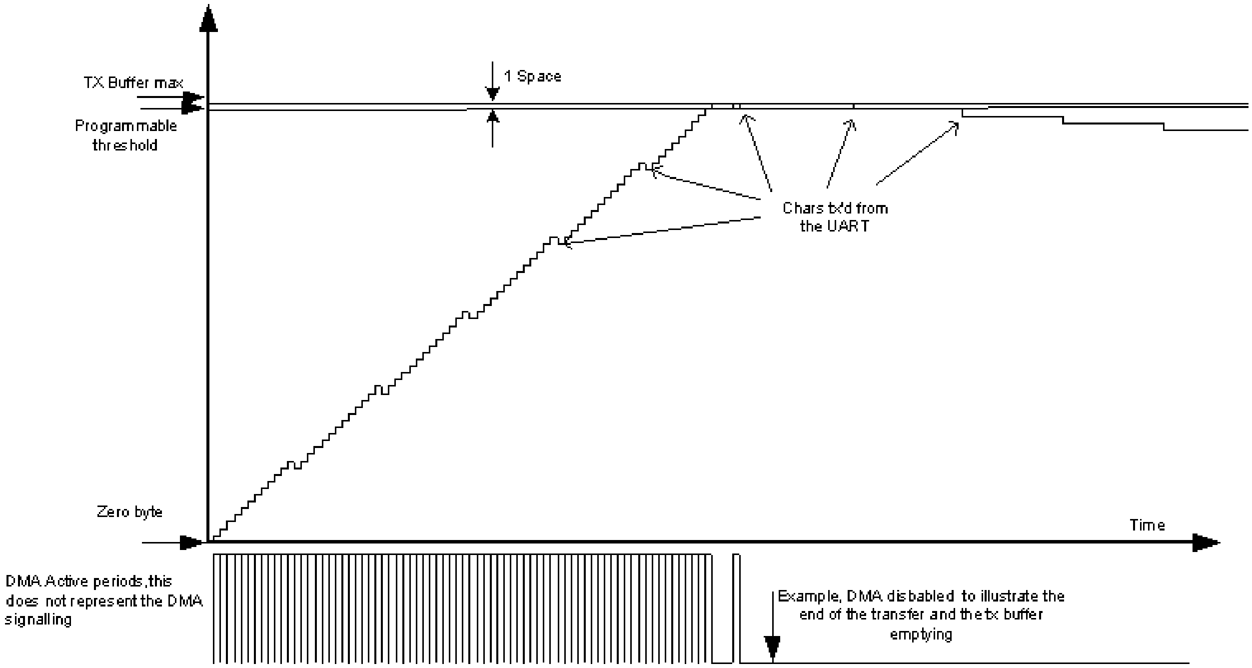

Figure 12-99. UART Transmit FIFO DMA Request Generation (1 Space)

The final example illustrates the setting of eight spaces but setting the TX DMA threshold directly by setting UART_MDR3[1] NONDEFAULT_FREQ bit and UART_TX_DMA_THRESHOLD register (see Figure 12-100). In the example, the UART_TX_DMA_THRESHOLD[5-0] TX_DMA_THRESHOLD = 3 and the trigger level is 8. The buffer is filled at a faster rate than the BAUD rate transmits data to the TX pin. The buffer is filled with 8 bytes and the DMA operations stop transferring data to the transmit buffer. When the buffer is emptied to the threshold level by transmission, the DMA operation activates again to fill the buffer with 8 bytes.

Eventually, the buffer will be emptied at the rate specified by the BAUD Rate settings of the UART_DLL and UART_DLH registers.

If the selected threshold level + trigger level exceeds max buffer size, then the original TX DMA threshold method is used to prevent TX overrun, regardless of the UART_MDR3[1] NONDEFAULT_FREQ value.

The DMA settings should correspond to the system Local Host DMA controller settings in order to ensure the correct operation of this logic.

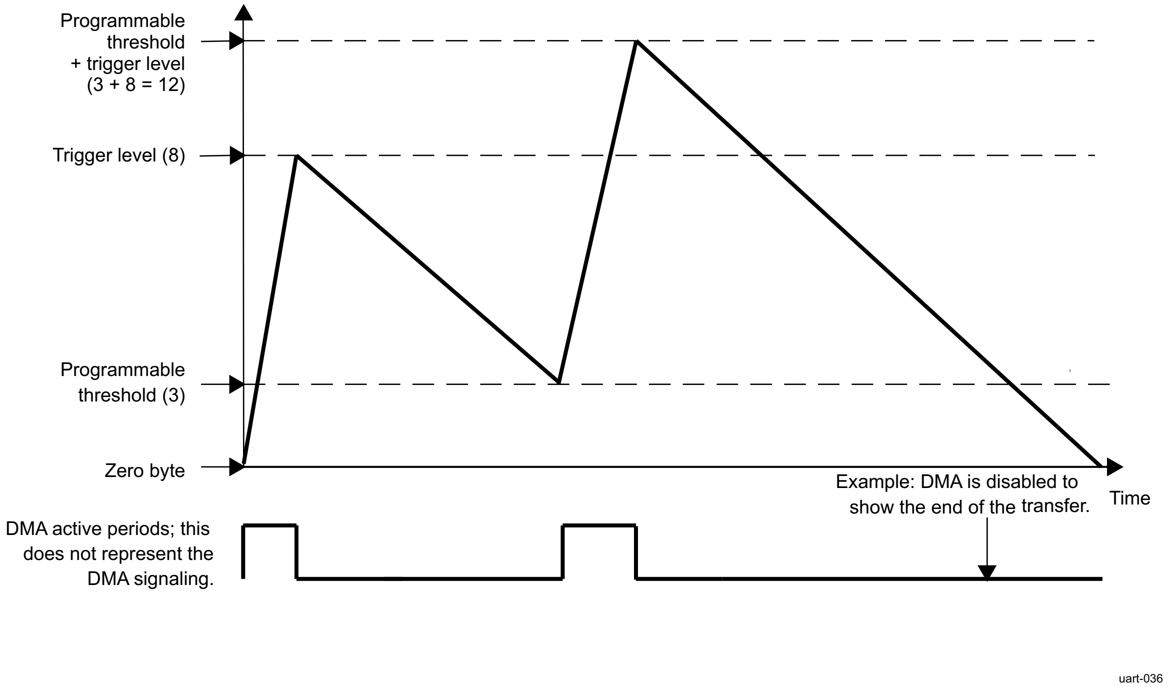

Figure 12-100. UART Transmit FIFO DMA Request Generation Using Direct TX DMA Threshold Programming. (Threshold = 3; Spaces = 8)

12.1.5.4.6.4.3 DMA Transmission

Figure 12-101 shows DMA transmission.

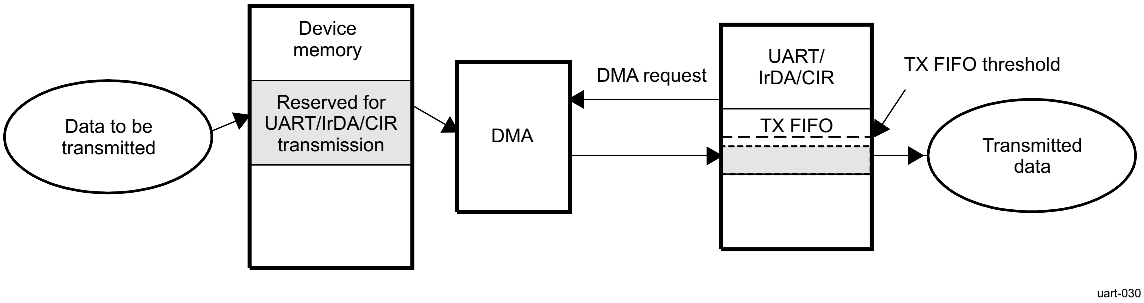

Figure 12-101. DMA Transmission

1. Data to be transmitted are put in the device memory reserved for UART transmission by the DMA:
    a. Until the TX FIFO trigger level is not reached, a DMA request is generated
    b. An element (1 byte) is transferred from the SDRAM to the TX FIFO at each DMA request (DMA element synchronization).
2. Data in the TX FIFO are automatically transmitted.
3. The end of the transmission is signaled by the UART_THR empty (TX FIFO empty).

Note

In IrDA mode, the transmission does not end immediately after the TX FIFO empties, at which point the last data byte, the CRC field, and the stop flag still must be transmitted; thus, the end of transmission occurs a few milliseconds after the UART_THR register empties.

12.1.5.4.6.4.4 DMA Reception

Figure 12-102 shows DMA reception.

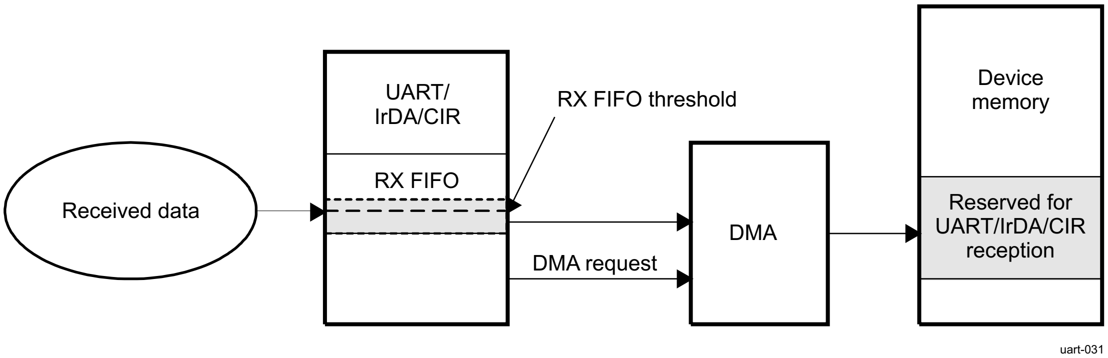

Figure 12-102. DMA Reception

1. Enable the reception.
2. Received data are put in the RX FIFO.
3. Data are transferred from the RX FIFO to the device memory by the DMA:
    a. At each received byte, the RX FIFO trigger level (one character) is reached and a DMA request is generated.
    b. An element (1 byte) is transferred from the RX FIFO to the SDRAM at each DMA request (DMA element synchronization).
4. The end of the reception is signaled by the EOF interrupt.

12.1.5.4.7 UART Mode Selection

12.1.5.4.7.1 Register Access Modes

12.1.5.4.7.1.1 Operational Mode and Configuration Modes

Register access depends on the register access mode, although register access modes are not correlated to functional mode selection. Three different modes are available:

- Operational mode
- Configuration mode A
- Configuration mode B

Operational mode is the selected mode when the function is active; serial data transfer can be performed in this mode.

Configuration mode A and configuration mode B are used during module initialization steps. These modes enable access to configuration registers, which are hidden in the operational mode. The modes are used when the module is inactive (no serial data transfer processed) and only for initialization or reconfiguration of the module.

The value of the UART_LCR register determines the register access mode (see Table 12-112).

Table 12-112. UART Register Access Mode Programming (Using UART_LCR)

Mode	Condition
Configuration mode A	UART_LCR[7] = 0x1 and UART_LCR[7-0] != 0xBF
Configuration mode B	UART_LCR[7] = 0x1 and UART_LCR[7-0] = 0xBF
Operational mode	UART_LCR[7] = 0x0

12.1.5.4.7.1.2 Register Access Submode

In each access register mode (operational mode or configuration mode A/B), some register accesses are conditional on the programming of a submode (MSR_SPR, TCR_TLR, and XOFF). These registers are identified in Table 12-136, *UART Load FIFO Triggers Defined by the Concatenated Value*.

Table 12-113 through Table 12-115 summarize the register access submodes.

Table 12-113. UART Subconfiguration Mode A Summary

Mode	Condition
MSR_SPR	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

Table 12-114. UART Subconfiguration Mode B Summary

Mode	Condition
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1
XOFF	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)

Table 12-115. UART Suboperational Mode Summary

Mode	Condition
MSR_SPR	UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

12.1.5.4.7.1.3 Registers Available for the Register Access Modes

Table 12-116 lists the names of the register bits in each access register mode. Gray shading indicates that the register does not depend on the register access mode (available in all modes).

Table 12-116. UART Register Access Mode Overview

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART	UART_IER_UART
0x008	UART_IIR_UART	UART_FCR	UART_EFR	UART_EFR	UART_IIR_UART	UART_FCR
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR_UART	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART	–
0x018	UART_MSR / UART_TCR	UART_TCR	UART_TCR / UART_XOFF1	UART_TCR / UART_XOFF1	UART_MSR / UART_TCR	UART_TCR
0x01C	UART_SPR / UART_TLR	UART_SPR / UART_TLR	UART_TLR / UART_XOFF2	UART_TLR / UART_XOFF2	UART_SPR / UART_TLR	UART_SPR / UART_TLR
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	UART_UASR	–	UART_UASR	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR

Table 12-116. UART Register Access Mode Overview (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

12.1.5.4.7.2 UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection

To select a mode, set the UART_MDR1[2:0] MODE_SELECT bit field (see Table 12-117).

Table 12-117. UART Mode Selection

Value	Mode
0x0:	UART 16× mode
0x1:	SIR mode
0x2:	UART 16× auto-baud
0x3:	UART 13× mode
0x4:	MIR mode
0x5:	FIR mode
0x6:	CIR mode
0x7:	Disable (default state)

MODE_SELECT is effective when the module is in operational mode (see Section 12.1.5.4.7.1 , *Register Access Modes*).

To select a RS-485 mode, set the UART_MDR3[4] DIR_EN bit field to 0x1.

12.1.5.4.7.2.1 Registers Available for the UART Function

Only the registers listed in Table 12-118 are used for the UART function.

Table 12-118. UART Mode Register Overview

Address Offset	Registers(1)(2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (UART)	UART_IER_UART (UART)

Table 12-118. UART Mode Register Overview (continued)

Address Offset	Registers[1][2]					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x008	UART_IIR_UART	UART_FCR	UART_EFR [4]	UART_EFR [4]	UART_IIR_UART (UART)	UART_FCR (UART)
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR_UART (UART)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART (UART)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_XOFF1/UART_TCR	UART_XOFF1/UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR/UART_XOFF2	UART_TLR/UART_XOFF2	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	–	–	–	–	–	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	UART_UASR	–	UART_UASR	–	–	–
0x03C	–	–	–	–	–	–
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	–	–
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	–	–	–	–	–	–
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in *UART Registers*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

12.1.5.4.7.2.2 Registers Available for the IrDA Function

Only the registers listed in Table 12-119 are used for the IrDA function.

Table 12-119. IrDA Mode Register Overview

Address Offset	Registers(1)(2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (IrDA)	UART_IER_UART (IrDA)
0x008	UART_IIR_UART	UART_FCR	UART_EFR [4]	UART_EFR [4]	UART_IIR_UART (IrDA)	UART_FCR (IrDA)
0x00C	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]
0x010	–	–	UART_XON1_ADDR1	UART_XON1_ADDR1	–	–
0x014	UART_LSR_UART (IrDA)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART (IrDA)	–
0x018	UART_MSR/ UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/ UART_TCR	UART_TCR
0x01C	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR	UART_TLR	UART_TLR	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	–	–	–	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]
0x060	–	–	–	–	–	–
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(IrDA) notation indicates that the register exists for other functions (UART or CIR), but fields have different meanings for other functions (described separately in *UART Registers*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the IrDA function.

12.1.5.4.7.2.3 Registers Available for the CIR Function

Only the registers listed in Table 12-120 are used for the CIR function.

Table 12-120. CIR Mode Register Overview

Address Offset	Registers (1)(2)					
	Configuration Mode A		**Configuration Mode B**		**Operational Mode**	
	Read	**Write**	**Read**	**Write**	**Read**	**Write**
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	–	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (CIR)	UART_IER_UART (CIR)
0x008	UART_IIR_UART	UART_FCR	UART_EFR	UART_EFR	UART_IIR_UART (CIR)	UART_FCR (CIR)
0x00C	UART_LCR	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]
0x010	–	–	–	–	–	–
0x014	UART_LSR_UART (CIR)	–	–	–	UART_LSR_UART (CIR)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR	UART_TLR	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	UART_RESUME	–	UART_RESUME	–	UART_RESUME	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	–	–	–	–	–	–
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(CIR) notation indicates that the register exists for other functions (IrDA or UART), but fields have different meanings for other functions (described separately in *UART Registers*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the CIR function.

12.1.5.4.8 UART Protocol Formatting

12.1.5.4.8.1 UART Mode

12.1.5.4.8.1.1 UART Clock Generation: Baud Rate Generation

The UART function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 12-103 shows the baud rate generator and associated controls.

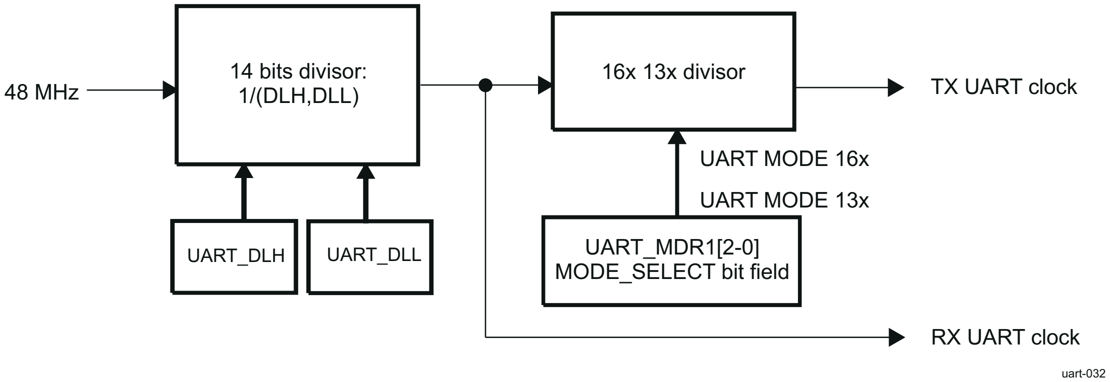

Figure 12-103. UART Baud Rate Generation

> **CAUTION**
>
> Before initializing or modifying clock parameter controls (UART_DLH, UART_DLL), UART_MDR1[2-0] MODE_SELECT = DISABLE must be set to 0x7. Failure to observe this rule can result in unpredictable module behavior.

12.1.5.4.8.1.2 Choosing the Appropriate Divisor Value

Two divisor values are:

- UART 16× mode: Divisor value = Operating frequency / (16× baud rate)
- UART 13× mode: Divisor value = Operating frequency / (13× baud rate)

Table 12-121 describes the UART baud rate settings.

Table 12-121. UART Baud Rate Settings (48-MHz, 160-MHz, 192-MHz Clock)

Baud Rate	Baud Multiple	Source Clock(MHz)	DLH, DLL (Decimal)	DLH, DLL (Hex)	Actual Baud Rate	Error (%)
0.3 kbps	16x	48	10000	0x27, 0x10	0.3 kbps	0
0.6 kbps	16x	48	5000	0x13, 0x88	0.6 kbps	0
1.2 kbps	16x	48	2500	0x09, 0xC4	1.2 kbps	0
2.4 kbps	16x	48	1250	0x04, 0xE2	2.4 kbps	0
4.8 kbps	16x	48	625	0x02, 0x71	4.8 kbps	0
9.6 kbps	16x	48	312	0x01, 0x38	9.615385 kbps	-0.16
9.6 kbps[1]	16x	192	1250	0x01, 0x38	9.6 kbps	0
14.4 kbps	16x	48	208	0x00, 0xD0	14.42308 kbps	-0.16
19.2 kbps[1]	16x	192	625	0x00, 0x9C	19.2kbps	0
28.8 kbps	16x	48	104	0x00, 0x68	28.84615 kbps	-0.16
38.4 kbps	16x	48	78	0x00, 0x4E	38.46154 kbps	-0.16
57.6 kbps	16x	48	52	0x00, 0x34	57.69231 kbps	-0.16
115.2 kbps	16x	48	26	0x00, 0x1A	115.3846 kbps	-0.16

Table 12-121. UART Baud Rate Settings (48-MHz, 160-MHz, 192-MHz Clock) (continued)

Baud Rate	Baud Multiple	Source Clock(MHz)	DLH, DLL (Decimal)	DLH, DLL (Hex)	Actual Baud Rate	Error (%)
230.4 kbps	16x	48	13	0x00, 0x0D	230.7692 kbps	-0.16
460.8 kbps	13x	48	8	0x00, 0x08	461.5385 kbps	-0.16
921.6 kbps	13x	48	4	0x00, 0x04	923.0769 kbps	-0.16
1.843 Mbps	13x	48	2	0x00, 0x02	1.846154 Mbps	-0.17
2.5 Mbps[2]	16x	160	4	0x00, 0x01	2.5 Mbps	0
3.0 Mbps	16x	48	1	0x00, 0x01	3.0 Mbps	0
3.6884 Mbps	13x	48	1	0x00, 0x01	3.692308 Mbps	-0.11
4 Mbps[2]	16x	192	3	0x00, 0x01	4 Mbps	0
5 Mbps[2]	16x	160	2	0x00, 0x02	5 Mbps	0
10 Mbps[2]	16x	160	1	0x00, 0x01	10 Mbps	0
12 Mbps[2]	16x	192	1	0x00, 0x01	12 Mbps	0

1. Indicates improved accuracy settings for an existing baud rate.
2. Indicates new baud rates
3. 1 and 2 can be achieved with a 192MHz or 160MHz source clock.

12.1.5.4.8.1.3 UART Data Formatting

The UART can use hardware flow control to manage transmission and reception. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the RTS output and CTS input signals.

The UART is enhanced with the autobauding function. In control mode, autobauding lets the speed, the number of bits per character, and the parity selected be set automatically.

12.1.5.4.8.1.3.1 Frame Formatting

When autobauding is not used, frame format attributes must be defined in the UART_LCR register.

Character length is specified using the UART_LCR[1-0] CHAR_LENGTH bit field.

The number of stop-bits is specified using the UART_LCR[2] NB_STOP bit.

The parity bit is programmed using the UART_LCR[5-3] PARITY_EN, UART_LCR[5-3] PARITY_TYPE_1, and UART_LCR[5-3] PARITY_TYPE_2 bit fields (see Table 12-122).

Table 12-122. UART Parity Bit Encoding

PARITY_EN	PARITY_TYPE_1	PARITY_TYPE_2	Parity
0	N/A	N/A	No parity
1	0	0	Odd parity
1	1	0	Even parity
1	0	1	Forced 1
1	1	1	Forced 0

12.1.5.4.8.1.3.2 Hardware Flow Control

Hardware flow control is composed of auto-CTS and auto-RTS. Auto-CTS and auto-RTS can be enabled and disabled independently by programming the UART_EFR[7] AUTO_CTS_EN and UART_EFR[6] AUTO_RTS_EN bit fields, respectively.

With auto-CTS, CTS signal must be active before the module can transmit data.

Auto-RTS activates the RTS output only when there is enough room in the RX FIFO to receive data. It deactivates the RTS output when the RX FIFO is sufficiently full. The HALT and RESTORE trigger levels in the UART_TCR register determine the levels at which RTS is activated and deactivated.

If auto-CTS and auto-RTS are enabled, data transmission does not occur unless the RX FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If auto-CTS and auto-RTS are not enabled, overrun errors occur if the transmit data rate exceeds the RX FIFO latency.

- Auto-RTS:

  Auto-RTS data flow control originates in the receiver block. The RX FIFO trigger levels used in auto-RTS are stored in the UART_TCR register. RTS is active if the RX FIFO level is below the HALT trigger level in the UART_TCR[3-0] RX_FIFO_TRIG_HALT bit field. When the RX FIFO HALT trigger level is reached, RTS is deasserted. The sending device (for example, another UART) can send an additional byte after the trigger level is reached because it may not recognize the deassertion of RTS until it begins sending the additional byte.

  RTS is automatically reasserted when the RX FIFO reaches the RESUME trigger level programmed by the UART_TCR[7-4] RX_FIFO_TRIG_START bit field. This reassertion requests the sending device to resume transmission.

  In this case, RTS is an active-low signal.
- Auto-CTS:

  The transmitter circuitry checks CTS before sending the next data byte. When CTS is active, the transmitter sends the next byte. To stop the transmitter from sending the next byte, CTS must be deasserted before the middle of the last stop-bit currently sent.

  The auto-CTS function reduces interrupts to the host system. When auto-CTS flow control is enabled, the CTS state changes do not have to trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO, and a receiver overrun error can result.

  In this case, CTS is an active-low signal.

12.1.5.4.8.1.3.3 Software Flow Control

Software flow control is enabled through the enhanced feature register (UART_EFR) and the modem control register (UART_MCR). Different combinations of software flow control can be enabled by setting different combinations of the UART_EFR[3-0] bit field (see Table 12-123).

Two other enhanced features relate to software flow control:

- XON-any function (UART_MCR[5] XON_EN): Operation resumes after receiving any character after the XOFF character is recognized. If special character detect is enabled and special character is received after XOFF1, it does not resume transmission. The special character is stored in the RX FIFO.

Note

The XON-any character is written into the RX FIFO even if it is a software flow character.

- Special character (UART_EFR[5] SPECIAL_CHAR_DETEC T): Incoming data is compared to XOFF2. When the special character is detected, the XOFF interrupt (UART_IIR_UART) is set, but it does not halt transmission. The XOFF interrupt is cleared by a read of UART_IIR_UART. The special character is transferred to the RX FIFO. Special character does not work with XON2, XOFF2, or sequential XOFFs.

Table 12-123. UART_EFR[3:0] Software Flow Control Options

Bit 3	Bit 2	Bit 1	Bit 0	TX, RX Software Flow Controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit XON1, XOFF1
0	1	X	X	Transmit XON2, XOFF2
1	1	X	X	Transmit XON1, XON2: XOFF1, XOFF2(1)
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares XON1, XOFF1

Table 12-123. UART_EFR[3:0] Software Flow Control Options (continued)

Bit 3	Bit 2	Bit 1	Bit 0	TX, RX Software Flow Controls
X	X	0	1	Receiver compares XON2, XOFF2
X	X	1	1	Receiver compares XON1, XON2: XOFF1, XOFF2(1)

(1) In these cases, the XON1 and XON2 characters or the XOFF1 and XOFF2 characters must be transmitted/received sequentially with XON1/XOFF1 followed by XON2/XOFF2.
XON1 is defined in the UART_XON1_ADDR1[7-0] XON_WORD1 bit field. XON2 is defined in the UART_XON2_ADDR2[7-0] XON_WORD2 bit field.
XOFF1 is defined in the UART_XOFF1[7-0] XOFF_WORD1 bit field. XOFF2 is defined in the UART_XOFF2[7-0] XOFF_WORD2 bit field.

12.1.5.4.8.1.3.3.1 Receive (RX)

When software flow control operation is enabled, the UART compares incoming data with XOFF1/2 programmed characters (in certain cases, XOFF1 and XOFF2 must be received sequentially). When the correct XOFF characters are received, transmission stops after transmission of the current character completes. Detection of XOFF also sets the UART_IIR_UART[4] bit (if enabled by UART_IER_UART[5]) and causes the interrupt line to go low.

To resume transmission, an XON1/2 character must be received (in certain cases, XON1 and XON2 must be received sequentially). When the correct XON characters are received, the UART_IIR_UART[4] bit is cleared and the XOFF interrupt disappears.

Note

When a parity, framing, or break error occurs while receiving a software flow control character, this character is treated as normal data and is written to the RX FIFO.

When XON-any and special character detect are disabled and software flow control is enabled, no valid XON or XOFF characters are written to the RX FIFO. For example, when UART_EFR[1-0] = 0x2, if XON1 and XOFF1 characters are received, they are not written to the RX FIFO.

When pairs of software flow characters are programmed to be received sequentially (UART_EFR[1-0] = 0x3), the software flow characters are not written to the RX FIFO if they are received sequentially. However, received XON1/XOFF1 characters must be written to the RX FIFO if the subsequent character is not XON2/XOFF2.

12.1.5.4.8.1.3.3.2 Transmit (TX)

Two XOFF1 characters are transmitted when the RX FIFO passes the trigger level programmed by UART_TCR[3-0] RX_FIFO_TRIG_HALT. As soon as the RX FIFO reaches the trigger level programmed by UART_TCR[7-4] RX_FIFO_TRIG_START, two XON1 characters are sent, so the data transfer recovers.

Note

If software flow control is disabled after an XOFF character is sent, the module transmits XON characters automatically to enable normal transmission.

The transmission of XOFF(s)/XON(s) follows the same protocol as transmission of an ordinary byte from the TX FIFO. This means that even if the word length is 5, 6, or 7 characters, the 5, 6, or 7 LSBs of XOFF1/2 and XON1/2 are transmitted. The 5, 6, or 7 bits of a character are seldom transmitted, but this function is included to maintain compatibility with earlier designs.

It is assumed that software flow control and hardware flow control are never enabled simultaneously.

12.1.5.4.8.1.3.4 Autobauding Modes

In autobauding mode, the UART can extract transfer characteristics (speed, length, and parity) from an "at" (AT) command (ASCII code). These characteristics are used to receive data after an AT and to send data.

The following AT commands are valid:

AT	DATA	<CR>
at	DATA	<CR>
A/		
a/		

A line break during the acquisition of the sequence AT is not recognized, and an echo function is not implemented in hardware.

A/ and a/ are not used to extract characteristics, but they must be recognized because of their special meaning. A/ or a/ is used to instruct the software to repeat the last received AT command; therefore, an a/ always follows an AT, and transfer characteristics are not expected to change between an AT and an a/.

When a valid AT is received, AT and all subsequent data, including the final <CR> (0x0D), are saved to the RX FIFO. The autobaud state-machine waits for the next valid AT command. If an a/ (A/) is received, the a/ (A/) is saved in the RX FIFO and the state-machine waits for the next valid AT command.

On the first successful detection of the baud rate, the UART activates an interrupt to signify that the AT (upper or lower case) sequence is detected. The UART_UASR register reflects the correct settings for the baud rate detected. Interrupt activity can continue in this fashion when a subsequent character is received. Therefore, it is recommended that the software enable the RHR interrupt when using the autobaud mode.

The following settings are detected in autobaud mode with a module clock of 48 MHz:

- Speed:
  - 115.2K baud
  - 57.6K baud
  - 38.4K baud
  - 28.8K baud
  - 19.2K baud
  - 14.4K baud
  - 9.6K baud
  - 4.8K baud
  - 2.4K baud
  - 1.2K baud
- Length: 7 or 8 bits
- Parity: Odd, even, or space

Note

The combination of 7-bit character plus space parity is not supported.

Autobauding mode is selected when the UART_MDR1[2-0] MODE_SELECT bit field is set to 0x2. In UART autobauding mode, UART_DLL, UART_DLH, and UART_LCR[5-0] bit field settings are not used; instead, the UART_UASR register is updated with the configuration detected by the autobauding logic.

UASR Autobauding Status Register Use

This register is used to set up transmission according to the characteristics of the previous reception instead of the UART_LCR, UART_DLL, and UART_DLH registers when the UART is in autobauding mode.

To reset the autobauding hardware (to start a new AT detection) or to set the UART in standard mode (no autobaud), the UART_MDR1[2-0] MODE_SELECT bit field must be set to reset state (0x7) and then to the UART in autobauding mode (0x2) or to the UART in standard mode (0x0).

Use limitation:

- Only 7- and 8-bit characters (5- and 6-bit not supported)
- 7-bit character with space parity not supported
- Baud rate between 1200 and 115.2 bps (10 possibilities)

12.1.5.4.8.1.3.5 Error Detection

When the UART_LSR_UART register is read, the UART_LSR_UART[4:2] bit field reflects the error bits (BI: break condition, FE: framing error, PE: parity error) of the character at the top of the RX FIFO (the next character to be read). Therefore, reading the UART_LSR_UART register and then reading the UART_RHR register identifies errors in a character.

Reading the UART_RHR register updates the BI, FE, and PE bits (see Table 12-107 for the UART mode interrupts).

The UART_LSR_UART[7] RX_FIFO_STS bit is set when there is an error in the RX FIFO and is cleared only when no errors remain in the RX FIFO.

Note

Reading the UART_LSR_UART register does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the UART_RHR register.

Reading the UART_LSR_UART register clears the OE bit if it is set (see Table 12-107 for the UART mode interrupts).

12.1.5.4.8.1.3.6 Overrun During Receive

Overrun during receive occurs if the RX state-machine tries to write data into the RX FIFO when it is already full. When overrun occurs, the device interrupts the Host CPU with the UART_IIR_UART[5-1] IT_TYPE bit field set to 0x3 (receiver line status error) and discards the remaining portion of the frame.

Overrun also causes an internal flag to be set, which disables further reception. Before the next frame can be received, the Host CPU must:

- Reset the RX FIFO.
- Read the UART_RESUME register, which clears the internal flag.

12.1.5.4.8.1.3.7 Time-Out and Break Conditions

12.1.5.4.8.1.3.7.1 Time-Out Counter

An RX idle condition is detected when the receiver line (RX) is high for a time that equals 4x the programmed word length + 12 bits or manually configured amount of baud clocks, if a value other zero is set in the timeout register. RX is sampled midway through each bit.

For sleep mode, the counter is reset when there is activity on RX.

There are two modes of operation:

- In default operation on the UART_EFR2[6] TIMEOUT_BEHAVE is set to 0. For the time-out interrupt, the counter counts only when there is data in the RX FIFO, and the count is reset when there is activity on RX or when the UART_RHR register is read.
- Optionally, for choose to enable the timeout counter even if no character has been received by setting UART_EFR2[6] TIMEOUT_BEHAVE bit. This will generate periodic interrupts if the RX line remains idle. In this mode the counter will auto-reset when a timeout has been reached. Reading the UART_IIR_UART will clear the interrupt, but not the counter.

12.1.5.4.8.1.3.7.2 Break Condition

When a break condition occurs, TX is pulled low. A break condition is activated by setting the UART_LCR[6] BREAK_EN bit. The break condition is not aligned on word stream (a break condition can occur in the middle of a character). The only way to send a break condition on a full character is:

1. Reset the TX FIFO (if enabled).
2. Wait for the transmit shift register to empty (the UART_LSR_UART[6] TX_SR_E bit is set to 1).
3. Take a guard time according to stop-bit definition.
4. Set the BREAK_EN bit to 1.

The break condition is asserted while the BREAK_EN bit is set to 1.

The time-out counter and break condition apply only to UART modem operation and not to IrDA/CIR mode operation.

12.1.5.4.8.2 RS-485 Mode

12.1.5.4.8.2.1 RS-485 External Transceiver Direction Control

The UART_MDR3[4] DIR_EN bit enables hardware control over an external transceiver to support RS-485. The direction signal comes across the DIR port. The direction polarity is controlled by the UART_MDR3[3] DIR_POL bit. The direction is determined by the hardware monitoring the TX FIFO and the TX shift register. When both are empty the transceiver is set to RX. There is a guard band delay counter of 3 bit clock cycles after the TX shift register is going empty to allow time for the stop bit to transition through the transceiver before a direction change to receive might be applied.

Figure 12-104 shows the direction control.

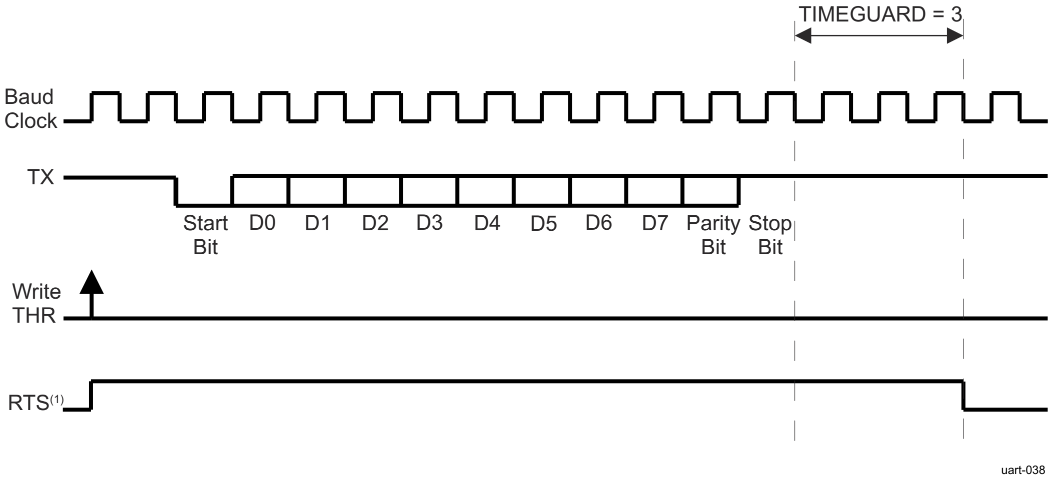

(1) Assumes DIR_POL = 1

Figure 12-104. RS-485 External Transceiver Direction Control

12.1.5.4.8.3 IrDA Mode

12.1.5.4.8.3.1 IrDA Clock Generation: Baud Generator

The IrDA function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 12-105 shows the baud rate generator and associated controls.

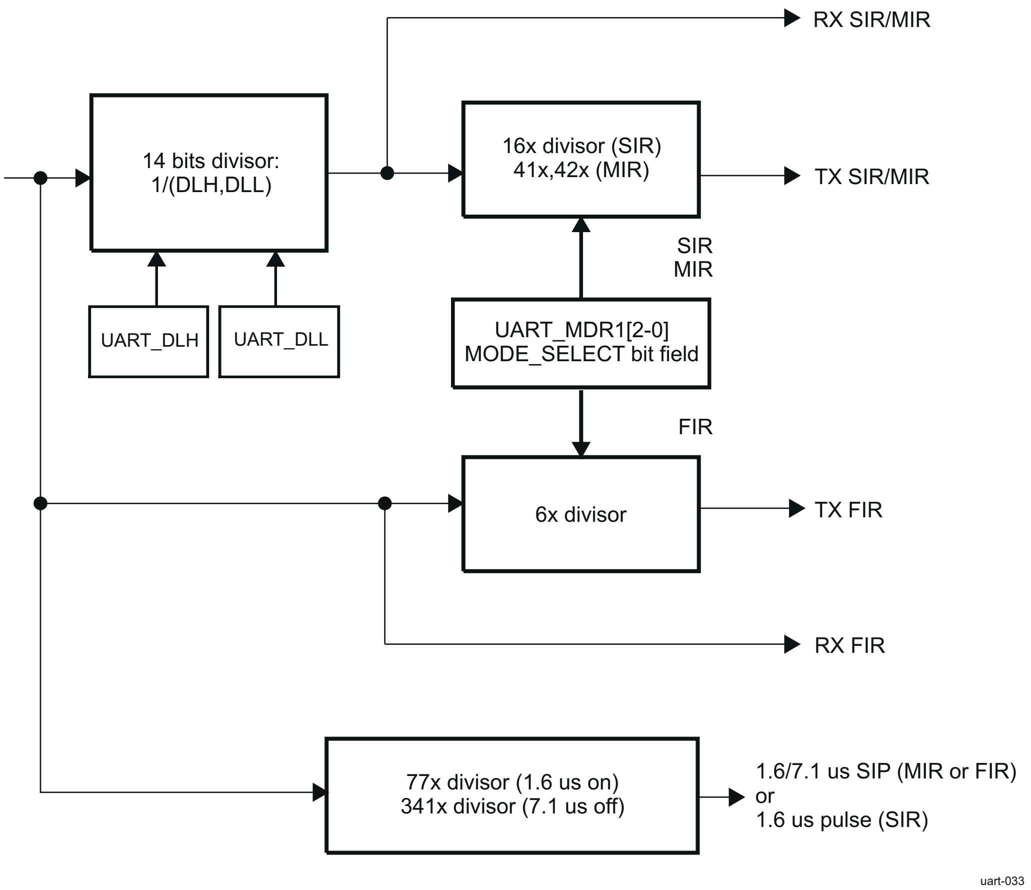

Figure 12-105. IrDA Baud Rate Generator

CAUTION

Before initializing or modifying clock parameter controls (UART_DLH, UART_DLL), MODE_SELECT=DISABLE (UART_MDR1[2-0] MODE_SELECT) must be set to 0x7). Failure to observe this rule can result in unpredictable module behavior.

12.1.5.4.8.3.2 Choosing the Appropriate Divisor Value

Three divisor values are:

- SIR mode: Divisor value = Operating frequency/(16× baud rate)
- MIR mode: Divisor value = Operating frequency/(41×/42× baud rate)
- FIR mode: Divisor value = None

Table 12-124 lists the IrDA baud rate settings.

Table 12-124. IrDA Baud Rate Settings

Baud Rate	IR Mode	Baud Multiple	Encoding	DLH, DLL (Decimal)	Actual Baud Rate	Error (%)	Source Jitter (%)	Pulse Duration
2.4 kbps	SIR	16x	3/16	1250	2.4 kbps	0	0	78.1 µs
9.6 kbps	SIR	16x	3/16	312	9.6153 kbps	+0.16	0	19.5 µs
19.2 kbps	SIR	16x	3/16	156	19.231 kbps	+0.16	0	9.75 µs
38.4 kbps	SIR	16x	3/16	78	38.462 kbps	+0.16	0	4.87 µs
57.6 kbps	SIR	16x	3/16	52	57.692 kbps	+0.16	0	3.25 µs
115.2 kbps	SIR	16x	3/16	26	115.38 kbps	+0.16	0	1.62 µs

Table 12-124. IrDA Baud Rate Settings (continued)

Baud Rate	IR Mode	Baud Multiple	Encoding	DLH, DLL (Decimal)	Actual Baud Rate	Error (%)	Source Jitter (%)	Pulse Duration
0.576 Mbps	MIR	41×/42×	1/4	2	0.5756 Mbps(1)	0	+1.63/-0.80	416 ns
1.152 Mbps	MIR	41×/42×	1/4	1	1.1511 Mbps(1)	0	+1.63/-0.80	208 ns
4 Mbps	FIR	6×	4 PPM	–	4 Mbps	0	0	125 ns

(1) Average value

Note

Baud rate error and source jitter table values do not include 48-MHz reference clock error and jitter.

12.1.5.4.8.3.3 IrDA Data Formatting

The methods described in this section apply to all IrDA modes (SIR, MIR, and FIR).

12.1.5.4.8.3.3.1 IR RX Polarity Control

The UART_MDR2[6] IRRXINVERT bit provides the flexibility to invert the RX pin in the UART to ensure that the protocol at the output of the transceiver has the same polarity at module level. By default, the RX pin is inverted because most transceivers invert the IR receive pin.

12.1.5.4.8.3.3.2 IrDA Reception Control

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

Operation of the RX input can be disabled by the UART_ACREG[5] DIS_IR_RX bit.

12.1.5.4.8.3.3.3 IR Address Checking

In all IR modes, when address checking is enabled, only frames intended for the device are written to the RX FIFO. This restriction avoids receiving frames not meant for this device in a multipoint infrared environment. It is possible to program two frame addresses that the UART IrDA receives, with the UART_XON1_ADDR1[7-0] XON_WORD1 and UART_XON2_ADDR2[7-0] XON_WORD2 bit fields.

Setting the UART_EFR[0] bit to 1 selects address1 checking. Setting the UART_EFR[1] bit to 1 selects address2 checking. Setting the UART_EFR[1-0] bit field to 0 disables all address checking operations. If both bits are set, the incoming frame is checked for private and public addresses.

If address checking is disabled, all received frames write to the RX FIFO.

12.1.5.4.8.3.3.4 Frame Closing

A transmission frame can be terminated in two ways:

- Frame-length method: Set the UART_MDR1[7] FRAME_END_MODE bit to 0. The Host CPU writes the value of the frame length to the UART_TXFLH and UART_TXFLL registers. The device automatically attaches end flags to the frame when the number of bytes transmitted equals the value of the frame length.
- Set-EOT bit method: Set the UART_MDR1[7] FRAME_END_MODE bit to 1. The Host CPU writes 1 to the UART_ACREG[0] EOT bit just before it writes the last byte to the TX FIFO. When the Host CPU writes the last byte to the TX FIFO, the device internally sets the tag bit for that character in the TX FIFO. As the TX state-machine reads data from the TX FIFO, it uses this tag-bit information to attach end flags and correctly terminate the frame.

12.1.5.4.8.3.3.5 Store and Controlled Transmission

In store and controlled transmission (SCT) mode, the Host CPU starts writing data to the TX FIFO. Then, after writing a part of a frame (for a bigger frame) or an entire frame (a small frame; that is, a supervisory frame), the Host CPU writes 1 to the UART_ACREG[2] SCTX_EN bit (deferred TX start) to start transmission.

SCT mode is enabled by setting the UART_MDR1[5] SCT bit to 1. This transmission method differs from normal mode, in which data transmission starts immediately after data is written to the TX FIFO. SCT mode is useful for sending short frames without TX underrun.

12.1.5.4.8.3.3.6 Error Detection

When the UART_LSR_UART register is read, the UART_LSR_UART[4-2] bit field reflects the error bits [FL, CRC, ABORT] of the frame at the top of the STATUS FIFO (the next frame status to be read).

The error is triggered by an interrupt (for IrDA mode interrupts, see Table 12-108). The STATUS FIFO must be read until empty (a maximum of eight reads is required).

12.1.5.4.8.3.3.7 Underrun During Transmission

Underrun during transmission occurs when the TX FIFO is empty before the end of the frame is transmitted. When underrun occurs, the device closes the frame with end flags but attaches an incorrect CRC value. The receiving device detects a CRC error and discards the frame; it can then ask for a retransmission.

Underrun also causes an internal flag to be set, which disables additional transmissions. Before the next frame can be transmitted, the Host CPU must:

- Reset the TX FIFO.
- Read the UART_RESUME register, which clears the internal flag.

This function can be disabled by the UART_ACREG[4] DIS_TX_UNDERRUN bit, compensated by the extension of the stop-bit in transmission if the TX FIFO is empty.

12.1.5.4.8.3.3.8 Overrun During Receive

Overrun during receive for the IrDA mode has the same function as that for the UART mode (see Section 12.1.5.4.8.1.3.6 , *Overrun During Receive*).

12.1.5.4.8.3.3.9 Status FIFO

In IrDA modes, a status FIFO records the received frame status. When a complete frame is received, the length of the frame and the error bits associated with the frame are written to the status FIFO.

Reading the UART_SFREGH[3-0] MSB and UART_SFREGL[3-0] (LSB) bit fields obtains the frame length. The frame error status is read in the UART_SFLSR register. Reading the UART_SFLSR register increments the status FIFO read pointer. Because the status FIFO is eight entries deep, it can hold the status of eight frames.

The Host CPU uses the frame-length information to locate the frame boundary in the received frame data. The Host CPU can screen bad frames using the error status information and can later request the sender to resend only the bad frames.

This status FIFO can be used effectively in DMA mode because the Host CPU must be interrupted only when the programmed status FIFO trigger level is reached, not each time a frame is received.

12.1.5.4.8.3.3.10 Multi-drop Parity Mode with Address Match

Multi-drop mode is enabled in the UART_EFR2 register.

Address matching mode is only available with 8 bit character length setting. UART_LCR[1-0] CHAR_LENGTH bit fields should always be set to 0x11 (8 bits) prior to enabling the feature.

This mode allows the transmitter to send data on a line where multiple receivers are connected, when supported. In this mode, a set parity bit is used to mark an address, and a parity of 0 denotes data.

This setting affects how the parity is generated. Writing a 0x1 into the UART_ECR[0] A_MULTIDROP bit will set the parity bit for the next byte to be sent, which will then be considered an address, for sending a data frame, the UART_ECR[0] A_MULTIDROP bit has to be cleared.

On reception if the feature is enabled by setting the UART_EFR2[2] MULTIDROP bit to 0x1 incoming frames with parity set to 0x1 are treated as address frames and with parity set to 0x0 as data frames. The receiver will drop all data frames until a matching address frame was found.

The matching address is determined by the values set in UART_MAR, UART_MMR and UART_MBR registers and the value set in UART_EFR2[7] BROADCAST bit.

Table 12-125 summarizes the operation of address matching based on the mentioned values.

Table 12-125. Details of address matching

Received frame	Received parity	Frame type	UART_MAR	UART_MMR	UART_MBR	UART_EFR2[7] BROADCAST	Operation of receiver	Address matching
0xXX(2)	0	DATA	X(1)	X(1)	0xXX(2)	X(1)	Drops data until matching address found	N/A
0xXX(2)	1	ADDRESS	0xXX(2)	0x00	0xXX(2)	0	Matches any address	Yes
0xEF	1	ADDRESS	0xXX(2)	0xXX(2)	0xEF	1	Matches broadcast address	Yes
0x1A	1	ADDRESS	0x1A	0xFF	0xXX(2)	0	Single address match	Yes
0xF5	1	ADDRESS	0xF3	0xF9	0xXX(2)	0	Group address match	Yes

(1) X indicates a do not care bit value

(2) 0xXX indicates a do not care 8 bit hexadecimal value

The possible values for matching address can be calculated in the following way:

- Single and Group addresses can be formed by masking the UART_MAR registers value with the value set in the UART_MMR register, bits set to 0x0 in the UART_MMR register result in do not care values.
- Broadcast addresses can be set in the UART_MBR register if broadcast address is enabled in the UART_EFR2[7] BROADCAST bit, the module will match on received address frames containing the broadcast address.
- For more details, see example below:
  - UART_MAR: 0xF3, UART_MMR: 0xF9, UART_MBR: 0xFF
  - Single and Group addresses: 0xF1, 0xF3, 0xF5, 0xF7
  - Broadcast addresses: 0xFF

If an address match occurred the matching address value can be obtained from the UART_RHR register in the following way:

- If the FIFO is disabled or the threshold is set to 0x1, the matching address can be directly read from UART_RHR as the FIFO will not be overwritten.
- If the FIFO is enabled or the threshold is greater than 0x1, the matching address will be the latest frame in the FIFO with a parity error bit set.

For received data, the parity error bit in the UART_LSR_UART register is set when a bit with a parity of 0x1 is received indicating an address frame and the received address matches based on the values of UART_MAR, UART_MMR, UART_MBR and UART_EFR2[2] MULTIDROP bit.

In Multi-drop mode no parity is used, as the parity bit is used to differentiate address and data frames. The parity error bit is used for indicating an address match.

For enabling the interrupt generation for address matching UART_IER_UART[2] LINE_STS_IT bit has to be set to 0x1.

An interrupt for the matching address can be identified by reading the UART_IIR_UART[5-1] IT_TYPE bit fields, a value of 0x00011 indicates a receiver line status error. After the UART_LSR_UART[2] RX_PE bit has to be read, a value of 0x1 indicates that an address match occurred. The reception of a frame is indicated with a value of 0x1 in the UART_LSR_UART[0] RX_FIFO_E bit as the matching value is written into the FIFO regardless of the frame type (data or address). UART_LSR_UART[7] RX_FIFO_STS bit will also be set to 0x1 as the parity error bit is used to indicate a matching address.

Note that the operation of the UART_LSR_UART[2] RX_PE bit depends on the value set in UART_EFR2[2] MULTIDROP bit. If UART_EFR2[2] MULTIDROP bit is set to 0x0, UART_LSR_UART[2] RX_PE bit is used to indicate a received parity error. If UART_EFR2[2] MULTIDROP bit is set to 0x1, the receiver is in Multi-drop Address Match mode, thus the value in UART_LSR_UART[2] RX_PE bit is used to indicate an address match.

The interrupt is cleared the same way in both operation modes: reading the UART_LSR_UART register updates the values.

This feature is available in UART and synchronous modes. The ISO7816 has not defined Multidrop Parity Mode, so the feature should be left off.

12.1.5.4.8.3.3.11 Time-guard

The time-guard feature enables the UART interface to operate with slow remote devices.

When set, it will insert a number of idle states between transmitting two characters, the length of which can be set in the UART_TIMEGUARD register. The value in the register defines the number of baud clocks of idle period to insert.

This idle state essentially acts like a long stop bit. In UART and synchronous modes, a Timeguard is added in addition to the stop bit. In ISO7816 there is a waiting period rather than an actual stop bit. Software should set 1-2 or more Timeguard cycles according to the protocol used and the card requirements.

12.1.5.4.8.3.4 SIR Mode Data Formatting

This section provides specific instructions for SIR mode programming.

12.1.5.4.8.3.4.1 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

A transmission frame can be aborted by setting the UART_ACREG[1] ABORT_EN bit to 1. When this bit is set to 1, 0x7D and 0xC1 are transmitted and the frame is not terminated with CRC or stop flags.

When a 0x7D character followed immediately by a 0xC1 character is received without transparency, the receiver treats a frame as an aborted frame.

> **CAUTION**
>
> When the TX FIFO is not empty and the UART_MDR1[5] SCT bit is set to 1, the UART IrDA starts a new transfer with data of a previous frame when the aborted frame is sent. Therefore, the TX FIFO must be reset before sending an aborted frame.

12.1.5.4.8.3.4.2 Pulse Shaping

SIR mode supports the 3/16 or the 1.6-μs pulse duration methods. The UART_ACREG[7] PULSE_TYPE bit selects the pulse width method in the transmit mode.

12.1.5.4.8.3.4.3 SIR Free Format Programming

The SIR FF mode is selected by setting the module in the UART mode (UART_MDR1[2-0] MODE_SELECT = 0x0) and the UART_MDR2[3] PULSE bit to 1 to allow pulse shaping.

Because the bit format stays the same, some UART mode configuration registers must be set at specific values:

- UART_LCR[1-0] CHAR_LENGTH bit field = 0x3 (8 data bits)
- UART_LCR[2] NB_STOP bit = 0x0 (1 stop-bit)
- UART_LCR[3] PARITY_EN bit = 0x0 (no parity)

The UART mode interrupts are used for the SIR FF mode, but many are not relevant (XOFF, RTS, CTS, modem status register, etc.).

12.1.5.4.8.3.5 MIR and FIR Mode Data Formatting

This section describes common instructions for FIR and MIR mode programming.

At the end of a frame reception, the CPU reads the line status register (UART_LSR_UART) to detect errors in the received frame.

When the UART_MDR1[6] SIP_MODE bit is set to 1, the TX state-machine always sends one SIP at the end of a transmission frame. However, when the SIP_MODE bit is set to 0, SIP transmission depends on the UART_ACREG[3] SEND_SIP bit.

The CPU can set the SEND_SIP bit at least once every 500 ms. The advantage of this approach over the default approach is that the TX state-machine does not have to send the SIP at the end of each frame, thus reducing the overhead required.

12.1.5.4.8.4 CIR Mode

12.1.5.4.8.4.1 CIR Mode Clock Generation

Depending on the encoding method (variable pulse distance/biphase), the Host CPU must develop a data structure that combines 1 and 0 with a *t* period to encode the complete frame to transmit. This can then be transmitted to the infrared output with a modulation method, as shown in Figure 12-106.

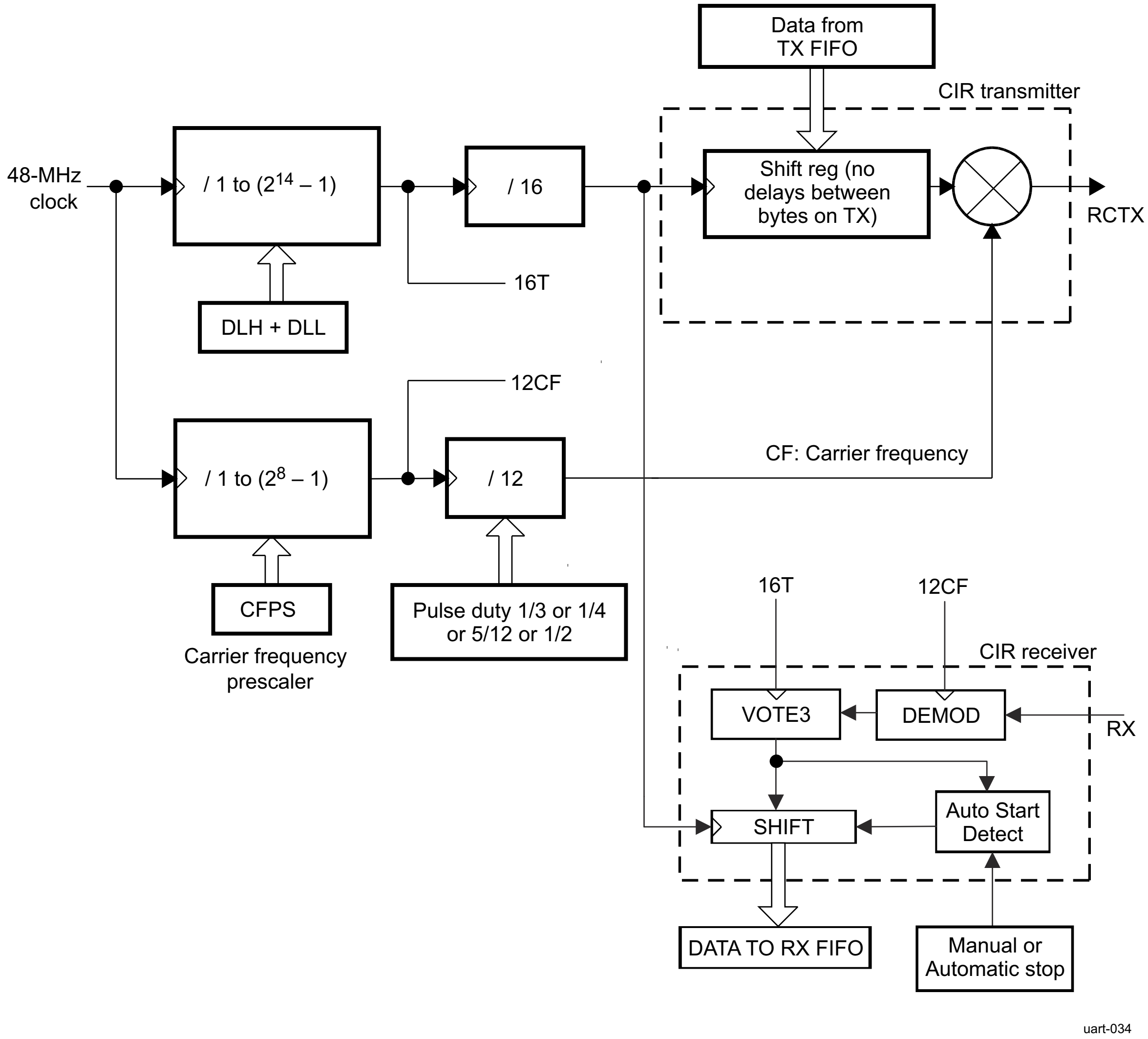

Figure 12-106. CIR Mode Block Components

Based on the requested modulation frequency, the UART_CFPS register must be set with the correct dividing value to provide an accurate pulse frequency:

Dividing value = (FCLK / 12) / MODfreq

Where:

FCLK = System clock frequency (48 MHz)

12 = Real value of baud multiple

MODfreq = Effective frequency of the modulation (MHz)

Example: For a targeted modulation frequency of 36 kHz, the value of CFPS must be set to 0x7 (decimal), which provides a modulation frequency of 36.04 kHz.

Note

The UART_CFPS register starts with a reset value of 105 (decimal), which translates to a frequency of 38.1 kHz.

The duty cycle of these pulses is user-defined by the pulse duty register bits in the UART_MDR2 register. Table 12-126 shows the duty cycle.

Table 12-126. CIR Duty Cycle

UART_MDR2[5-4] CIR_PULSE_MODE	Duty Cycle (High-Level)
00	1/4
01	1/3
10	5/12
11	1/2

12.1.5.4.8.4.2 CIR Data Formatting

The methods described in this section apply to all CIR modes.

12.1.5.4.8.4.2.1 IR RX Polarity Control

The IR RX polarity control for CIR mode has the same function as that for IrDA mode (see Section 12.1.5.4.8.3.3.1 , *IR RX Polarity Control*).

12.1.5.4.8.4.2.2 CIR Transmission

In transmission, the Host CPU software must exercise an element of real-time control to transmit data packets, each of which must be emitted at a constant delay from the start-bits of each individual packet. Thus, when sending a series of packets, the packet-to-packet delay must respect a specific delay. Two methods can be used to control this delay:

- Filling the TX FIFO with a number of zero bits that are transmitted with a *t* period
- Using an external system timer to control the delay between each start-of-frame or between the end of a frame and the start of the next one. This can be performed by:
  - Controlling the start of the frame using the UART_MDR1[5] SCT bit and the UART_ACREG[2] SCTX_EN bit, depending on the timer status
  - Using the UART_IIR_UART[5] TX_STATUS_IT interrupt bit to preload the next frame in the TX FIFO and to control the start of the timer (in case of control delay between the end of a frame and the start of the next frame)

12.1.5.4.8.4.2.3 CIR Reception

There are 2 ways to stop a CIR reception:

- The Host CPU can disable the reception by setting the UART_ACREG[5] DIS_IR_RX bit to 1. When it considers that the reception is finished because a large number of 0 has been received. To receive a new frame, the UART_ACREG[5] DIS_IR_RX bit must be set to 0.
- An automatic stop mechanism can configured by setting a value in the BOF length register (UART_EBLR). If the value set in the UART_EBLR register is different than 0, this features is enabled and the number of bits received will begin counting from 0. When the counter reaches the value defined in the UART_EBLR register, reception is automatically disabled and UART_IIR_CIR[2] RX_STOP_IT bit is set. When a 1 is detected on the RX pin, reception is automatically re-enabled.

There is a limitation when receiving data in UART CIR mode. Certain IrDA transceivers on the market have a characteristic that causes shrinking of the received modulation pulse hold-time. The UART receive filtering schema is based on the same encoding mechanism used for transmission.

For the following scenario:

- Shift register period: 0.9μs
- Modulation frequency: 36kHz
- Duty cycle: 1/4 of a modulation frequency period

Data sent with these conditions would contains 7µs pulses within a 28µs period. The UART expects to receive similar incoming data on receive, but various transceiver timing characteristics typically only send 2µs modulated pulses. These 2µs pulses will be filtered out and RX FIFO will not receive data. This does not affect UART CIR mode in transmission.

CIR RX demodulation can be bypassed by setting the UART_MDR3[0] DISABLE_CIR_RX_DEMOD bit.

12.1.5.5 UART Programming Guide

This section describes the procedure for operating the UART with FIFO and DMA or interrupts. This three-part procedure ensures the quick start of the UART. It does not cover every UART feature.

The first programming model covers software reset of the UART. The second programming model describes FIFO and DMA configuration. The last programming model describes protocol, baud rate, and interrupt configuration.

Note

Each programming model can be used independently of the other two; for instance, reconfiguring the FIFOs and DMA settings only.

Each programming model can be executed starting from any UART register access mode (register modes, submodes, and other register dependencies). However, if the UART register access mode is known before executing the programming model, some steps that enable or restore register access are optional. For more information, see Section 12.1.5.4.7.1 , *Register Access Modes*.

12.1.5.5.1 UART Global Initialization

12.1.5.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the UART module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the UART.

For more information, see .

Table 12-127. UART Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC0	Module reset must be enabled. For more information about the module configuration, see *Reset*.
PLLCTRL0	PLLCTRL0 configuration must be done to enable the clocks to the UART modules, see *Clocking*.
MCU_PLLCTRL0	MCU_PLLCTRL0 configuration must be done to enable the clocks to the UART modules, see *Clocking*.
PLL0	PLL0 configuration must be done to enable the clocks to the UART modules, see *Clocking*.
PLL1	PLL1 configuration must be done to enable the clocks to the UART modules, see *Clocking*.
GICSS0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling GICSS0 interrupts, see *Interrupts*.
MCU_M4FSS	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MCU_M4FSS interrupts, see *Interrupts*.
PRU-ICSSG0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling PRU_ICSSG0/1 interrupts, see *Interrupts*.
R5FSS0_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS0_CORE0/1 interrupts, see *Interrupts*.
R5FSS1_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS1_CORE0/1 interrupts, see *Interrupts*.
PDMA_USART_G0	PDMA_USART_G0 controllers configuration must be done to enable the module PDMA_USART_G0 channel request, see *Data Movement Architecture (DMA)*.
PDMA_USART_G1	PDMA_USART_G1 controllers configuration must be done to enable the module PDMA_USART_G1 channel request, see *Data Movement Architecture (DMA)*.
Interconnects	For information about the MCU_CBASS0, and CBASS0 interconnects configuration, see *System Interconnect*.

12.1.5.5.1.2 UART Module Global Initialization

The procedure in Table 12-128 can be used to initialize UART when performing software reset.

Table 12-128. UART Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	UART_SYSC[1] SOFTRESET	1
Wait until reset is finished.	UART_SYSS[0] RESETDONE	=1

12.1.5.5.2 UART Mode selection

Table 12-129 describes how to set different register access mode.

Table 12-129. UART Configure Register Access Mode

Step	Register/Bit Field/Programming Model	Value
Set the register access mode A	UART_LCR[7] DIV_EN	1
	UART_LCR[7-0]	≠0xBF
Set the register access mode B	UART_LCR[7-0]	0xBF
Set the operational mode	UART_LCR[7] DIV_EN	0

12.1.5.5.3 UART Submode selection

This section describes how to set different register access submode.

Table 12-130. UART Configure Register Access Submode TCR_TLR

Step	Register/Bit Field/Programming Model	Value
Configure the submode TCR_TLR		
Configure mode B	see Table 12-129	
Enable writing to register bits UART_MCR[7-5]	UART_EFR[4] ENHANCED_EN	1
Configure mode A	see Table 12-129	0x1
Set the submode TCR_TLR	UART_MCR[6] TCR_TLR	1

Table 12-131. UART Configure Register Access Submode MSR_SPR

Step	Register/Bit Field/Programming Model	Value
First option: configure the submode MSR_SPR		
Configure mode B	see Table 12-129	
Set the submode MSR_SPR	UART_EFR[4] ENHANCED_EN	0
Second option: configure the submode MSR_SPR		
Configure mode B	see Table 12-129	
Enable writing to register bits UART_MCR[7-5]	UART_EFR[4] ENHANCED_EN	1
Set the submode MSR_SPR	UART_MCR[6] TCR_TLR	0

Table 12-132. UART Configure Register Access Submode XOFF

Step	Register/Bit Field/Programming Model	Value
Configure of the XOFF		
Configure B	see Table 12-129	
Set the submode XOFF	UART_EFR[4] ENHANCED_EN	0

12.1.5.5.4 UART Load FIFO trigger and DMA mode settings

12.1.5.5.4.1 DMA mode Settings

To enable and configure program the DMA mode, perform the following steps:

Table 12-133. DMA Mode Settings

Step	Register/Bit Field/Programming Model	Value
Set the option of DMA mode configuration	UART_SCR[0] DMA_MODE_CTL	-
IF Configure DMA mode 0 and 1	UART_SCR[0] DMA_MODE_CTL	=0

Table 12-133. DMA Mode Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Select the DMA mode, for more information see Section 12.1.5.4.6.4	UART_FCR[3] DMA_MODE	-
IF Configure DMA mode from 0 to 3	UART_SCR[0] DMA_MODE_CTL	=1
Select the DMA mode, for more information see Section 12.1.5.4.6.4	UART_SCR[2-1] DMA_MODE_2	-

12.1.5.5.4.2 FIFO Trigger Settings

In this section is described configuration and settings of FIFO trigger level, which enable DMA and interrupt generation.

Table 12-134. Load FIFO Triggers Defined by the FCR

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-130	0x-
Set the desire RX FIFO trigger level	UART_FCR[5-4] TX_FIFO_TRIG	0x-
Set the desire TX FIFO trigger level	UART_FCR[7-6] RX_FIFO_TRIG	0x-

Table 12-135. Load FIFO Triggers Defined by the TLR

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-130	0x-
Set the desire RX FIFO trigger level	UART_TLR[7-4] RX_FIFO_TRIG_DMA	0x-
Set the desire TX FIFO trigger level	UART_TLR[3-0] TX_FIFO_TRIG_DMA	0x-

Table 12-136. Load FIFO Triggers Defined by the Concatenated Value

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-130	0x-
Set the register bit	UART_SCR[7] RX_TRIG_GRANU1	1
Set the desire RX FIFO trigger level	UART_TLR[7-4] RX_FIFO_TRIG_DMA UART_FCR[7-6] RX_FIFO_TRIG	0x-
Set the register bit	UART_SCR[6] TX_TRIG_GRANU1	1
Set the desire TX FIFO trigger level	UART_TLR[3-0] TX_FIFO_TRIG_DMA UART_FCR[5-4] TX_FIFO_TRIG	0x-

12.1.5.5.5 UART Protocol, Baud rate and interrupt settings

12.1.5.5.5.1 Baud rate settings

Table 12-137. UART Baud Rate Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Switch to register configuration mode B	see Table 12-129	
Enable access to UART_IER_UART[7-4]	UART_EFR[4] ENHANCED_EN	1
Switch register operational mode	see Table 12-129	
Disable sleep mode	UART_IER_UART[4] SLEEP_MODE	0
Switch to register configuration mode A or B	see Table 12-129	
Set the appropriate divisor value	UART_DLL[7-0] CLOCK_LSB UART_DLH[5-0] CLOCK_MSB	0x-

12.1.5.5.5.2 Interrupt settings

Table 12-138. UART Interrupt Settings

Step	Register/Bit Field/Programming Model	Value
Switch to register configuration mode B	see Table 12-129	0x7
Enable access to UART_IER_UART[7-4]	UART_EFR[4] ENHANCED_EN	1
Switch register operational mode	see Table 12-129	
Set the desired interrupt configuration (0: Disable the interrupt; 1: Enable the interrupt)	UART_IER_UART[7] CTS_IT UART_IER_UART[6] RTS_IT UART_IER_UART[5] XOFF_IT UART_IER_UART[4] SLEEP_MODE UART_IER_UART[3] MODEM_STS_IT UART_IER_UART[2] LINE_STS_IT UART_IER_UART[1] THR_IT UART_IER_UART[0] RHR_IT	0x-

12.1.5.5.5.3 Protocol settings

Load the desired protocol formatting (parity, stop-bit, character length) and switch to register operational mode.

Table 12-139. UART Protocol Settings

Step	Register/Bit Field/Programming Model	Value
Load desired protocol formatting, see Section 12.1.5.4.8.1.3.1 , *Frame Formatting*	UART_LCR[5] PARITY_TYPE_2 UART_LCR[4] PARITY_TYPE_1 UART_LCR[3] PARITY_EN UART_LCR[2] NB_STOP UART_LCR[1-0] PARITY_LENGTH	0x-
Switch to register operational mode	UART_LCR[7] DIV_EN UART_LCR[6] BREAK_EN	0

12.1.5.5.5.4 UART/RS-485/IrDA(SIR/MIR/FIR)/CIR

Table 12-140. UART Mode Selection

Step	Register/Bit Field/Programming Model	Value
Load the desired UART/IrDA (SIR, MIR, FIR)/CIR modes, see Section 12.1.5.4.7.2 , *UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection*	UART_MDR1[2-0] MODE_SELECT	0x-
Load the desire RS-485 mode, see Section 12.1.5.4.7.2 , *UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection*	UART_MDR3[4] DIR_EN	0x1

12.1.5.5.5.5 UART Multi-drop Parity Address Match Mode Configuration

Table 12-141. UART Multi-drop Parity Address Match Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Disable receive mode	UART_ECR[3] RX_EN	0
Enable Multi-drop parity Address match mode	UART_EFR2[2] MULTIDROP	1
Set the matching device address	UART_MAR[7-0] ADDRESS	0x-
Set the address match masking	UART_MMR[7-0] MASK	0x-
Set the broadcast address match	UART_MBR[7-0] BROADCAST_ADDRESS	0x-
Enable broadcast address matching if needed	UART_EFR2[7] BROADCAST	1
Enable receive mode	UART_ECR[3] RX_EN	1

12.1.5.5.6 UART Hardware and Software Flow Control Configuration

This section describes the programming steps to enable and configure hardware and software flow control. Hardware and software flow control cannot be used at the same time.

12.1.5.5.6.1 Hardware Flow Control Configuration

Table 12-142. UART Hardware Flow Control Configuration

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-130	0x7
Load the start and halt trigger value.	UART_TCR[7-4] AUTO_RTS_START UART_TCR[3-0] AUTO_RTS_HALT	0x-
Enable or disable receive and transmit hardware flow control mode.	UART_EFR[7] AUTO_CTS_EN UART_EFR[6] AUTO_RTS_EN	0x-

12.1.5.5.6.2 Software Flow Control Configuration

Table 12-143. UART Software Flow Control Configuration

Step	Register/Bit Field/Programming Model	Value
Set the register access submode XOFF	see Table 12-132	
Load the software control characters	UART_XON1_ADDR1[7-0] XON_WORD1 UART_XON2_ADDR2[7-0] XON_WORD2 UART_XOFF1[7-0] XOFF_WORD1 UART_XOFF2[7-0] XOFF_WORD2	0x-
Set the register access submode TCR_TLR	see Table 12-130	
Enable or disable XON any function (0: Disable; 1: Enable).	UART_MCR[5] XON_EN	--
Load start and halt trigger value for software flow control	UART_TCR[7-4] AUTO_RTS_START UART_TCR[3-0] AUTO_RTS_HALT	0x-
Enable or disable special character function (0: Disable; 1: Enable)	UART_EFR[5] SPEC_CHAR	0x-
Set the software flow control mode	UART_EFR[3-0] SW_FLOW_CONTROL	0x-

12.1.5.5.7 IrDA Programming Model

12.1.5.5.7.1 SIR mode

12.1.5.5.7.1.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with parity forced to 1, baud rate = 115.2 kbps, FIFOs disabled, 2 stop-bits, and 8-bit word length:

Table 12-144. SIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate(115.2 Kbps)	UART_DLL[7-0] CLOCK_LSB	0x1A
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.1.5.5.7.1.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 6-byte frame with no parity, baud rate = 115.2 kbps, FIFOs disabled, 3/16 encoding, 2 stop-bits, and 7-bit word length:

Table 12-145. SIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (115.2 Kbps)	UART_DLL[7-0] CLOCK_LSB	0x1A
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force output DTR to active	UART_MCR[0] DTR	1
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	0x1
Set transmit frame length to 6 bytes	UART_TXFLL[7-0] TXFLL	0x06
Set the seven starts of frame transmission	UART_EBLR[7-0] EBLR	0x08
Set SIR pulse width to be 1.6 µs	UART_ACREG[7] PULSE_TYPE	1

12.1.5.5.7.2 MIR mode

12.1.5.5.7.2.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled.

Table 12-146. MIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (1.152 bps)	UART_DLL[7-0] CLOCK_LSB	0x01
	UART_DLH[5-0] CLOCK_MSB	0x00
Set MIR mode	UART_MDR1[2-0] MODE_SELECT	0x4
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force outputs DTR and RTS to active	UART_MCR[1-0]	0x3
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.1.5.5.7.2.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 60-byte frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled.

Table 12-147. MIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (115.2 kbps)	UART_DLL[7-0] CLOCK_LSB	0x01
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x4
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force output DTR to active	UART_MCR[0] DTR	1

Table 12-147. MIR Mode Transmit Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	0x1
Set transmit frame length to 60 bytes	UART_TXFLL[7-0] TXFLL	0x3C
Set the eight additional starts of frame transmission	UART_EBLR[7-0] EBLR	0x08
SIP is sent at the end of transmission	UART_ACREG[3] SEND_SIP	1

12.1.5.5.7.3 FIR mode

12.1.5.5.7.3.1 Receive

The following programming model explains how to program the module to receive the IrDA frame with no parity, baud rate = 4 Mbps, FIFOs enabled, 8-bit word length.

Table 12-148. FIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Enable access to change UART_FCR[0]	UART_DLL[7-0] CLOCK_LSB	0x0
	UART_DLH[7-0] CLOCK_MSB	
FIFO clear and enable	UART_FCR[2-0]	0x7
Set the FIFO trigger level	see Section 12.1.5.5.4 , *Load FIFO trigger and DMA mode settings*	
Set FIR mode	UART_MDR1[2-0] MODE_SELECT	0x5
Set frame length	UART_RXFLL[7-0] RXFLL	0xA
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.1.5.5.7.3.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 4-byte frame with no parity, baud rate = 4 Mbps, FIFOs enabled, and 8-bit word length.

Table 12-149. FIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Enable access to change UART_FCR[0]	UART_DLL[7-0] CLOCK_LSB	0x0
	UART_DLH[5-0] CLOCK_MSB	
FIFO clear and enable	UART_FCR[2-0]	0x7
Set the FIFO trigger level	see Section 12.1.5.5.4 , *Load FIFO trigger and DMA mode settings*	
Set FIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Set FIR mode and enable auto-SIP mode	UART_MDR1[7-0]	0x45
Set frame length	UART_TXFLL[7-0] TXFLL	0x4
	UART_TXFLH[7-0] TXFLH	0x0
Force output DTR to active	UART_MCR[0] DTR	1
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	1
Set the eight additional starts of frame transmission	UART_EBLR[7-0] EBLR	0x08

Table 12-149. FIR Mode Transmit Settings (continued)

Step	Register/Bit Field/Programming Model	Value
SIP is sent at the end of transmission	UART_ACREG[3] SEND_SIP	1

12.2 High-speed Serial Interfaces

This section describes the high-speed serial interfaces in the device.

12.2.1 Gigabit Ethernet Switch (CPSW3G)

This chapter describes the Gigabit Ethernet Switch (CPSW3G) subsystem in the device.

12.2.1.1 CPSW0 Overview

The 3-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch.

The device has integrated one 3-port Gigabit Ethernet Switch subsystem into device MAIN domain named CPSW0. Table 12-150 shows the CPSW0 module allocation within device domains.

Table 12-150. CPSW0 Module Allocation within Device Domains

Module Instance	Domain	
	MCU	MAIN
CPSW0	-	✓

Figure 12-107 shows the CPSW0 module overview.

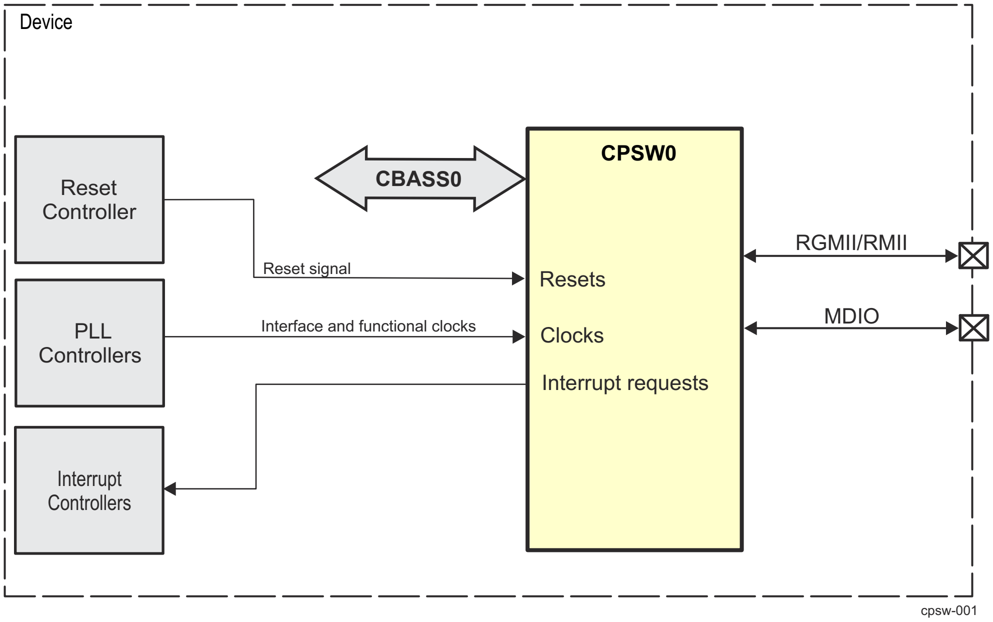

Figure 12-107. CPSW0 Overview

12.2.1.1.1 CPSW0 Features

The 3-port CPSW0 subsystem provides the following features:

- Two Ethernet ports (port 1 and 2) with selectable RGMII and RMII interfaces and an internal Communications Port Programming Interface (CPPI) port (port 0)
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Cut through switch support
- Eight priority level Quality Of Service (QOS) support (802.1p)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
  - Timestamp module capable of time stamping external timesync events like Pulse-Per-Second and also generating Pulse-Per-Second outputs
  - CPTS module that supports time stamping for IEEE1588 with support for 4 hardware push events and generation of compare output pulses
- DSCP Priority Mapping (IPv4 and IPv6)
- Energy Efficient Ethernet (EEE) support (802.3az)
- Flow Control Support (802.3x)
- Wire rate switching (802.1d)

- Non-Blocking switch fabric
- Time Sensitive Network Support
  - IEEE P802.3br Interspersing Express Traffic
  - IEEE 802.1Qbv Enhancements for Scheduled Traffic
- Address Lookup Engine (ALE)
  - 512 ALE table entries
  - Configurable number of addresses plus VLANs
  - Wire rate lookup
  - Host controlled time-based aging and/or auto-aging
  - Spanning tree support
  - L2 address lock and L2 filtering support
  - MAC authentication (802.1x)
  - Receive-based or destination-based Multicast and Broadcast rate limits
  - MAC address blocking
  - Source port locking
  - OUI (Vendor ID) host accept/deny feature
  - Configurable number of classifier/policers (32)
  - VLAN support
    - 802.1Q compliant
      - Auto add port VLAN for untagged frames on ingress
      - Auto VLAN removal on egress and auto pad to minimum frame size
- EtherStats and 802.3Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)
- Ethernet Mac transmit to Ethernet Mac receive Loopback mode (digital loopback) supported
- CPSGMII Loopback Modes (transmit to receive)
- Maximum frame size of 2024 bytes
- Management Data Input/Output (MDIO) module for PHY Management with Clause 45 support
- Programmable interrupt control with selected interrupt pacing
- Host port CPPI Streaming Packet Interface (CPPI_GCLK)
- Digital loopback and FIFO loopback modes supported
- Emulation support
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps modes only.
- RAM Error Detection and Correction (SECDED)

12.2.1.1.2 CPSW0 Not Supported Features

The following features are not supported by the CPSW0 switch:

- Maximum frame size of 9600 bytes
- MII and GMII Mode
- SGMII Mode
- MACSEC
- Synchronous Ethernet
- Cut through with any form of flow control
- Cut through with 10/100 half-duplex

12.2.1.1.3 CPSW Terminology

AVB	Audio Video Bridging
AVBTP	Audio Video Bridging Transport Protocol
BCCA	Best Controller Clock Algorithm
CFI	Canonical Format Indicator
CPPI	Communications Port Programming Interface
CPSW	Common Platform Switch

DLR	Device Level Ring
DSCP	Differentiated Services Code Point
EEE	Energy Efficient Ethernet
EMAC	Ethernet Media Access Control
EOP	End of Packet
EOQ	End of Queue
IPG	Inter-Packet Gap
LPI	Low Power Indicator
MDIO	Management Data Input/Output
MOF	Middle of Frame
OUI	Organizationally Unique Identifier
PFC	Priority based Flow Control
PTP	Precision Time Protocol
RMON	Remote Monitoring
RTCP	RTP Control Protocol
RTP	Real-time Transport Protocol
SCR	Switched Central Resource
SRP	Stream Reservation Protocol
TOS	Type of Service
VLAN	Virtual Local Area Network

12.2.1.2 CPSW0 Environment

This section describes the CPSW0 external connections (environment).

12.2.1.2.1 CPSW0 RMII Interface

Figure 12-108 shows a device with integrated EMAC and MDIO interfaced via a RMII connection in a typical system. The individual CPSW0 and MDIO signals for the RMII interface are summarized in Table 12-151.

The CPSW0 module integrated in the device supports internal and external clock sources in RMII mode. Figure 12-108 shows the internal clock source for RMII_MHZ_50_CLK clock. It is 50 MHz clock source that is provided on the CLKOUT0 device pin. This clock has to be routed on the PCB to the RMII_REF_CLK device pin and the external PHY, RMII clock input.

For more information, refer to either the IEEE 802.3 standard or ISO/IEC 8802-3:2000(E).

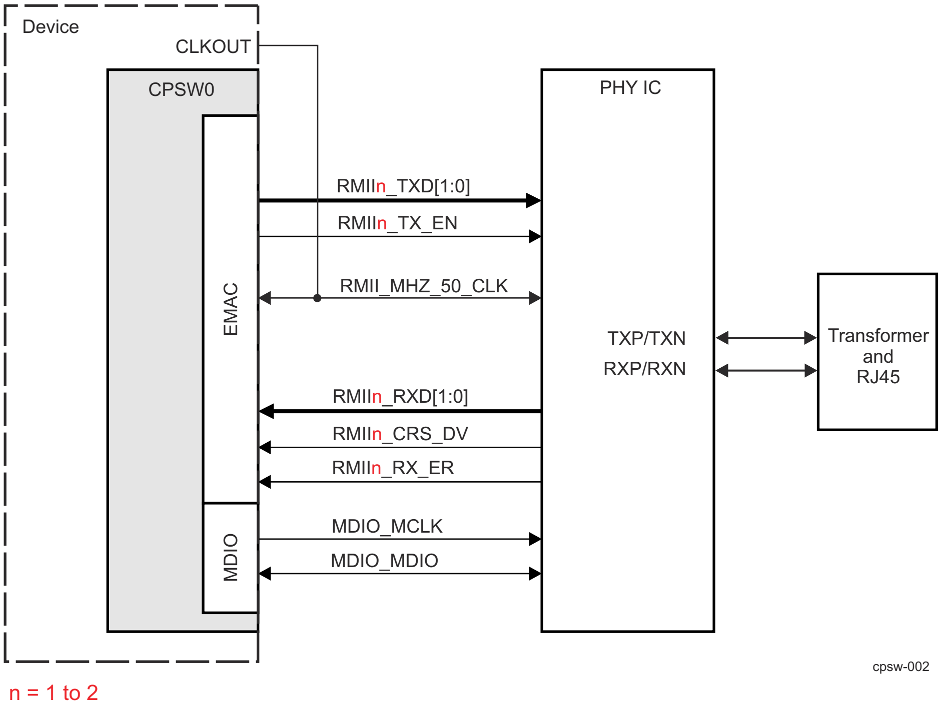

Figure 12-108. RMII Interface Typical Application (Internal Clock Source)

Figure 12-109 shows the external clock source for RMII_MHZ_50_CLK clock. In this case a 50 MHz clock is available on the PCB and it can be sourced from an oscillator or from the Ethernet PHY. This externally generated clock should be routed to both RMII_REF_CLK device pin and the external PHY, RMII clock input.

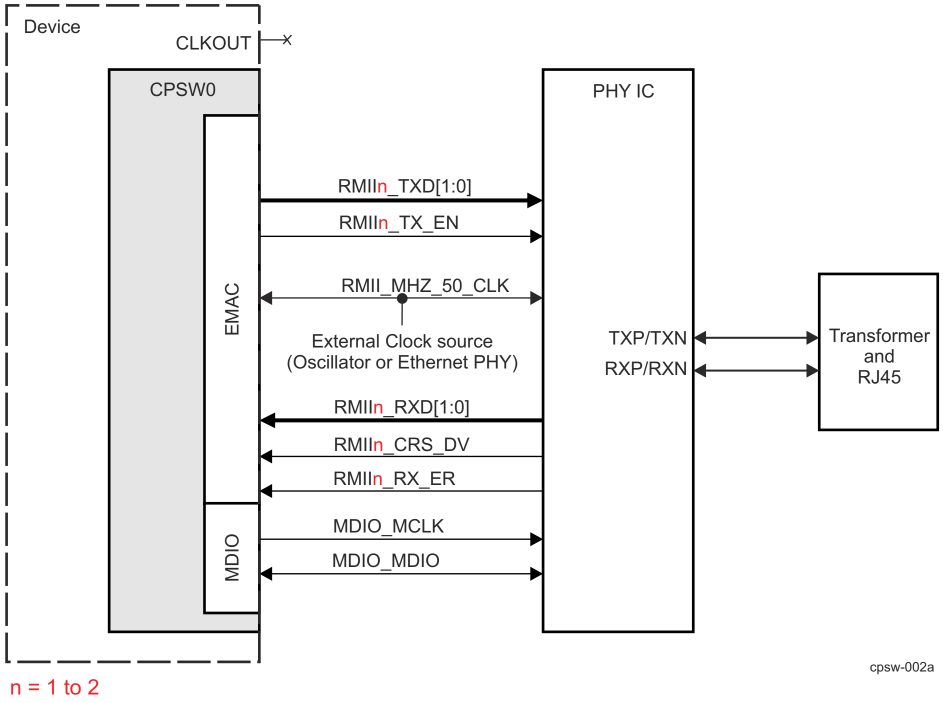

Figure 12-109. RMII Interface Typical Application (External Clock Source)

Table 12-151. RMII I/O Description

Signal[2]	Device Pin(s)	I/O[1]	Description
RMIIn_TXD[1:0]	RMIIn_TXD[1:0]	O	Transmit data. The transmit data pins are a collection of 2 bits of data. TXD0 is the least-significant bit (LSB). The signals are synchronized by RMII_MHZ_50_CLK and valid only when RMIIn_TX_EN is asserted.
RMIIn_TX_EN	RMIIn_TX_EN	O	RMII transmit enable. The transmit enable signal indicates that the RMIIn_TXD[1:0] pins are generating data for use by the PHY. RMIIn_TX_EN is synchronous to RMII_MHZ_50_CLK.
RMII_MHZ_50_CLK	RMII_REF_CLK	I	RMII 50MHz reference clock. The reference clock is used to synchronize all RMII signals. RMII_MHZ_50_CLK must be continuous and fixed at 50 MHz.
RMIIn_RXD[1:0]	RMIIn_RXD[1:0]	I	Receive data. The receive data pins are a collection of 2 bits of data. RXD0 is the least-significant bit (LSB). The signals are synchronized by RMII_MHZ_50_CLK and valid only when RMIIn_CRS_DV is asserted and RMIIn_RX_ER is de-asserted.
RMIIn_CRS_DV	RMIIn_CRS_DV	I	Carrier sense/receive data valid. Multiplexed signal between carrier sense and receive data valid.
RMIIn_RX_ER	RMIIn_RX_ER	I	Receive error. The receive error signal is asserted to indicate that an error was detected in the received frame.
MDIO_MCLK	MDIO0_MDC	O	Management data clock (MDIO_MCLK). The MDIO data clock is sourced by the MDIO module on the system. It is used to synchronize MDIO data access operations done on the MDIO0_MDIO data pin.
MDIO_MDIO	MDIO0_MDIO	I/O	MDIO data pin drives PHY management data into and out of the PHY by way of an access frame consisting of start of frame, read/write indication, PHY address, register address, and data bit cycles. The MDIO0_MDIO pin acts as an output for all but the data bit cycles at which time it is an input for read operations.

(1) I = Input; O = Output

(2) n 1 to 2

12.2.1.2.2 CPSW0 RGMII Interface

Figure 12-110 shows a device with integrated EMAC and MDIO interfaced via a RGMII connection in a typical system. The individual CPSW0 and MDIO signals for the RGMII interface are summarized in Table 12-152.

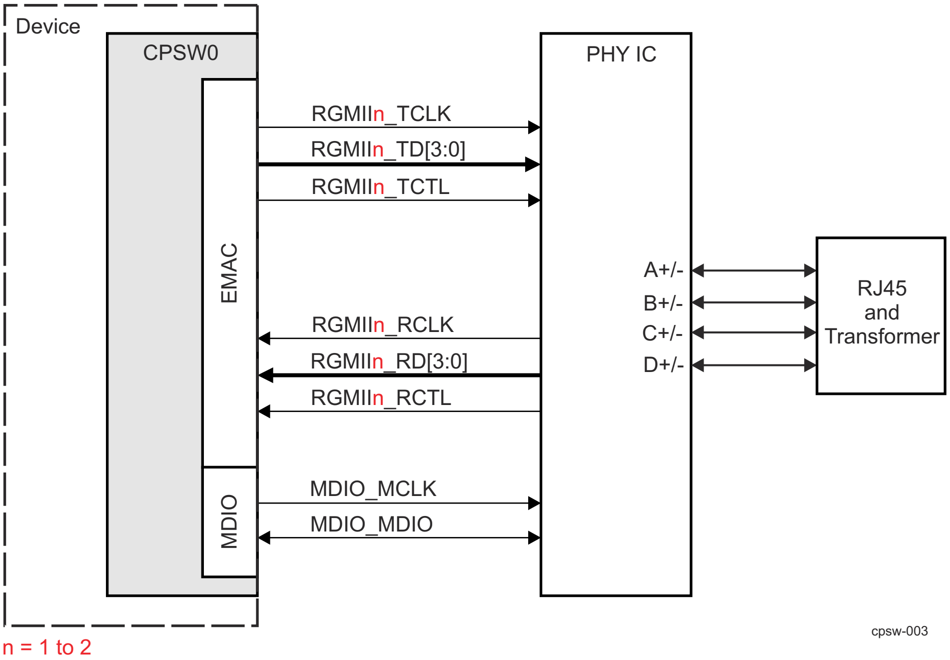

Figure 12-110. RGMII Interface Typical Application

Table 12-152. RGMII I/O Description

Signal[2]	Device Pin(s)	I/O[1]	Description
RGMIIn_TD[3:0]	RGMIIn_TD[3:0]	O	The transmit data pins are a collection of 4 bits of data. TD0 is the least-significant bit (LSB). The signals are valid only when RGMIIn_TCTL is asserted.
RGMIIn_TCTL	RGMIIn_TX_CTL	O	Transmit Control/enable. The transmit enable signal indicates that the TD pins are generating data for use by the PHY.
RGMIIn_TCLK	RGMIIn_TXC	O	The transmit reference clock. The clock is 2.5 MHz at 10 Mbps operation, 25 MHz at 100 Mbps operation, and 125 MHz at 1000 Mbps of operation.
RGMIIn_RD[3:0]	RGMIIn_RD[3:0]	I	The receive data pins are a collection of 4 bits of data. RD0 is the least-significant bit (LSB). The signals are valid only when RGMIIn_RX_CTL is asserted
RGMIIn_RCTL	RGMIIn_RX_CTL	I	The receive data valid/control signal indicates that the RD pins are nibble data for use by the EMAC.
RGMIIn_RCLK	RGMIIn_RXC	I	The receive clock is a continuous clock that provides the timing reference for receive operations. The clock is generated by the PHY and is 2.5 MHz at 10 Mbps operation, 25 MHz at 100 Mbps operation, 125 MHz at 1000 Mbps of operation.
MDIO_MCLK	MDIO0_MDC	O	Management data clock (MDIO_MCLK). The MDIO data clock is sourced by the MDIO module on the system. It is used to synchronize MDIO data access operations done on the MDIO0_MDIO pin.
MDIO_MDIO	MDIO0_MDIO	I/O	The MDIO0_MDIO pin drives PHY management data into and out of the PHY by way of an access frame consisting of start of frame, read/write indication, PHY address, register address, and data bit cycles. The MDIO0_MDIO pin acts as an output for all but the data bit cycles at which time it is an input for read operations.

(1) I = Input; O = Output

(2) n 1 to 2

Note

The Control Module registers assign the specific function to the device pads. For more information on Control Module settings, see Pad Configuration Registers in *Control Module (CTRL_MMR)* and the device-specific Datasheet.

12.2.1.3 CPSW0 Integration

Figure 12-111 shows the integration of the CPSW0 module in the device.

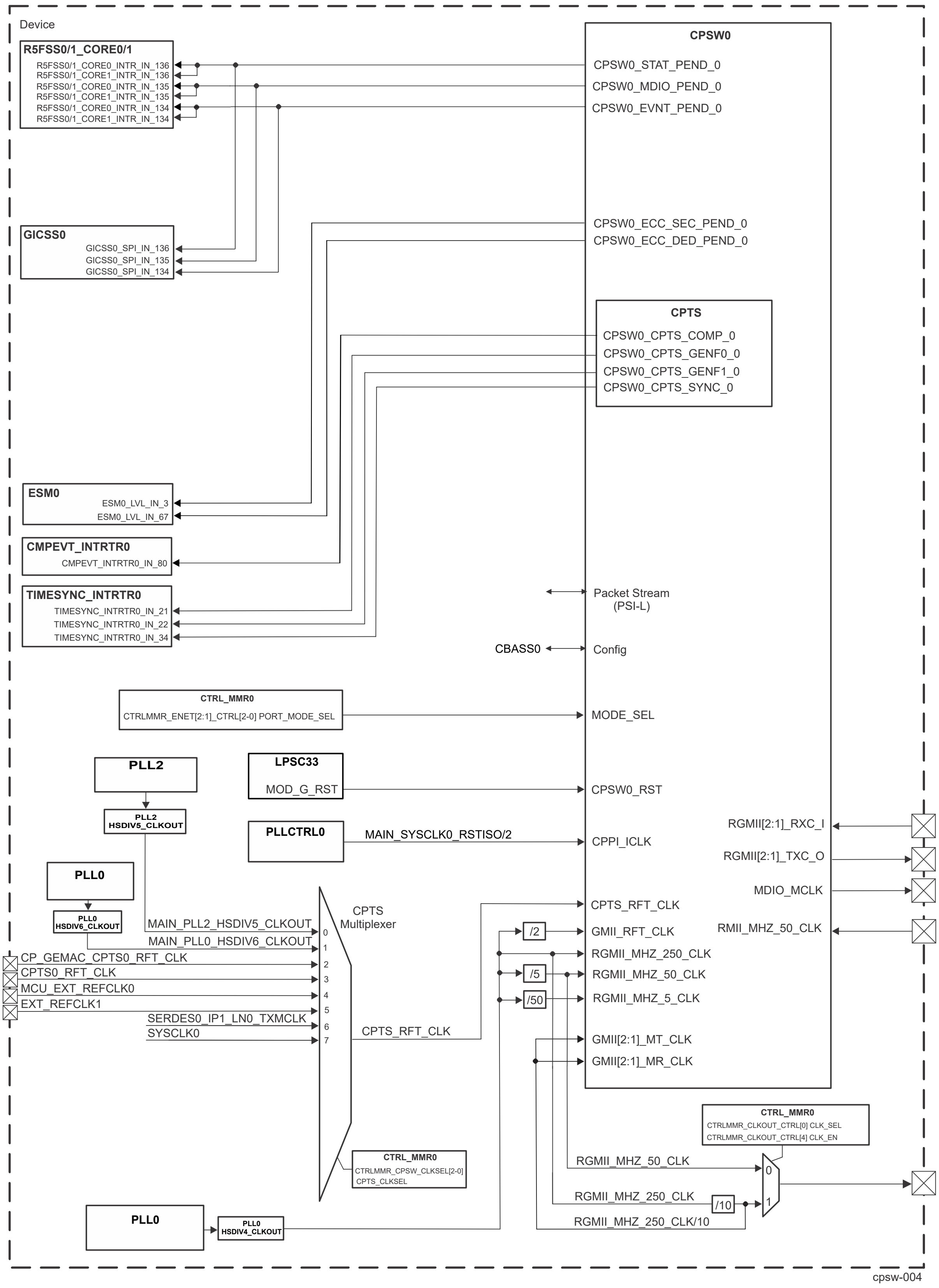

Figure 12-111. CPSW0 Integration

The following CPSW0 control registers are located in CTRL_MMR0 module: CTRLMMR_ENET1_CTRL, CTRLMMR_ENET2_CTRL, CTRLMMR_CPTS_CLKSEL.

Table 12-153 through Table 12-156 summarize the integration of the CPSW0 module in the device.

Table 12-153. CPSW0 Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
CPSW0	PSC0	PD9	LPSC33	CBASS0

Table 12-154. CPSW0 Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
CPSW0	CPPI_ICLK	MAIN_SYSCLK0_RSTISO/2	PLLCTRL0	CPPI packet streaming interface clock (250-MHz). Main clock for CPSW0.
	GMII_RFT_CLK	PLL0_HSDIV4_CLKOUT/2	PLL0	125-MHz GMII Gigabit mode clock.
	RGMII_MHZ_5_CLK	PLL0_HSDIV4_CLKOUT/50	PLL0	5-MHz RGMII reference clock.
	RGMII_MHZ_50_CLK	PLL0_HSDIV4_CLKOUT/5	PLL0	50-MHz RGMII reference clock.
	RGMII_MHZ_250_CLK	PLL0_HSDIV4_CLKOUT	PLL0	250-MHz RGMII reference clock.
	RMII_MHZ_50_CLK	RMII_REF_CLK	RMII_REF_CLK pad	50-MHz RMII reference clock. This clock is derived from the RMII_REF_CLK pad.
	CPTS_RFT_CLK	MAIN_PLL2_HSDIV5_CLKOUT	HSDIV5 of PLL2, selected through CPTS Multiplexer (225-MHz clock)	CPTS IEEE 1588 clock. Selected through the CTRLMMR_CPTS_CLKSEL register.
		MAIN_PLL0_HSDIV6_CLKOUT	HSDIV6 of PLL0, selected through CPTS Multiplexer (200 or 250-MHz clock)	
		CP_GEMAC_CPTS0_RFT_CLK pad	CP_GEMAC_CPTS0_RFT_CLK pad, selected through CPTS Multiplexer (200-MHz clock)	
		CPTS0_RFT_CLK pad	CPTS0_RFT_CLK pad, selected through CPTS Multiplexer (200-MHz clock)	
		MCU_EXT_REFCLK0 pad	MCU_EXT_REFCLK0 pad, selected through CPTS Multiplexer (100-MHz clock)	
		EXT_REFCLK1 pad	EXT_REFCLK1 pad, selected through CPTS Multiplexer (100-MHz clock)	
		SERDES0_IP1_LN0_TXMCLK	SERDES0 Lane0 (250-MHz clock)	
		SYSCLK0	PLLCTRL (500-MHz clock)	
	GMII[2:1]_MT_CLK	RGMII_MHZ_250_CLK/10	RGMII_MHZ_250_CLK	~~Note: GMII mode is not supported on this device. GMII[2:1]_MT_CLK transmit reference clock is needed to enable clock-stop protocol on this module.~~
	GMII[2:1]_MR_CLK	RGMII_MHZ_250_CLK/10	RGMII_MHZ_250_CLK	~~Note: GMII mode is not supported on this device. GMII[2:1]_MR_CLK receive reference clock is needed to enable clock-stop protocol on this module.~~

Table 12-154. CPSW0 Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
	RGMII[2:1]_RXC_I	RGMII[2:1]_RXC	RGMII[2:1]_RXC pad	RGMII reference clock that provides the timing reference for receive operations.
	RGMII[2:1]_TXC_O	RGMII[2:1]_TXC	RGMII[2:1]_TXC pad	RGMII transmit reference clock.
	MDIO_MCLK	MDIO_MCLK	MDIO0_MDC pad	Management data clock (MDIO_MCLK). The MDIO data clock is sourced by the MDIO module on the system. It is used to synchronize MDIO data access operations done on the MDIO pin.

Table 12-155. CPSW0 Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
CPSW0	CPSW0_RST	MOD_G_RST	LPSC33	Module Reset

Table 12-156. CPSW0 Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CPSW0	CPSW0_STAT_PEND_0	GICSS0_SPI_IN_136	GICSS0	CPSW0 statistic pending interrupt 0	Level
		R5FSS0_CORE0_INTR_IN_136	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_136	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_136	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_136	R5FSS1_CORE1		
	CPSW0_MDIO_PEND_0	GICSS0_SPI_IN_135	GICSS0	CPSW0 MDIO interrupt	Level
		R5FSS0_CORE0_INTR_IN_135	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_135	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_135	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_135	R5FSS1_CORE1		
	CPSW0_EVNT_PEND_0	GICSS0_SPI_IN_134	GICSS0	CPSW0 event pending interrupt	Level
		R5FSS0_CORE0_INTR_IN_134	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_134	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_134	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_134	R5FSS1_CORE1		
	CPSW0_ECC_SEC_PEND_0	ESM0_LVL_IN_3	ESM0	CPSW0 SEC ECC error interrupt	Level

Table 12-156. CPSW0 Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
	CPSW0_ECC_DED_PEND_0	ESM0_LVL_IN_67	ESM0	CPSW0 DED ECC error interrupt	Level

Table 12-157. CPSW0 Time Sync and Compare Events

Module Instance	Module Event	Destination Event Input	Destination	Description	Type
CPSW0	CPSW0_CPTS_COMP_0	CMPEVT_INTRTR0_IN_80	CMPEVT_INTRTR0	CPSW0 compare event interrupt	Edge
	CPSW0_CPTS_GENF0_0	TIMESYNC_INTRTR0_IN_21	TIMESYNC_INTRTR0	CPSW0 CPTS generator function event interrupt 0	Edge
	CPSW0_CPTS_GENF1_0	TIMESYNC_INTRTR0_IN_22	TIMESYNC_INTRTR0	CPSW0 CPTS generator function event interrupt 1	Edge
	CPSW0_CPTS_SYNC_0	TIMESYNC_INTRTR0_IN_34	TIMESYNC_INTRTR0	CPSW0 CPTS sync event interrupt	Edge

Note

For more information about interrupts, see *Local Interrupt Controller*.

For more information on the interconnects, see *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within *Device Configuration*.

For more information on the device interrupt controllers, see *Interrupt Controllers*.

For more information on the time sync and compare events routers, see *Time Sync and Compare Events*.

12.2.1.4 CPSW0 Functional Description

The three-port switch Ethernet subsystem module (CPSW) is compliant to the IEEE Std 802.3 Specification. CPSW top level functional block diagram is shown in Figure 12-112.

12.2.1.4.1 Functional Block Diagram

The three-port Ethernet subsystem consists of:

- CPSW3G Peripheral Core
- One RGMIIn (where n = 1 to 2) interface module
- One RMIIn (where n = 1 to 2) interface module
- One MIIn (where n = 1 to 2) interface module
- One Host Port 0 CPPI Packet Streaming Interface
- CPSW subsystem control registers (REG)
- One MDIO interface module
- One Interrupt Controller module

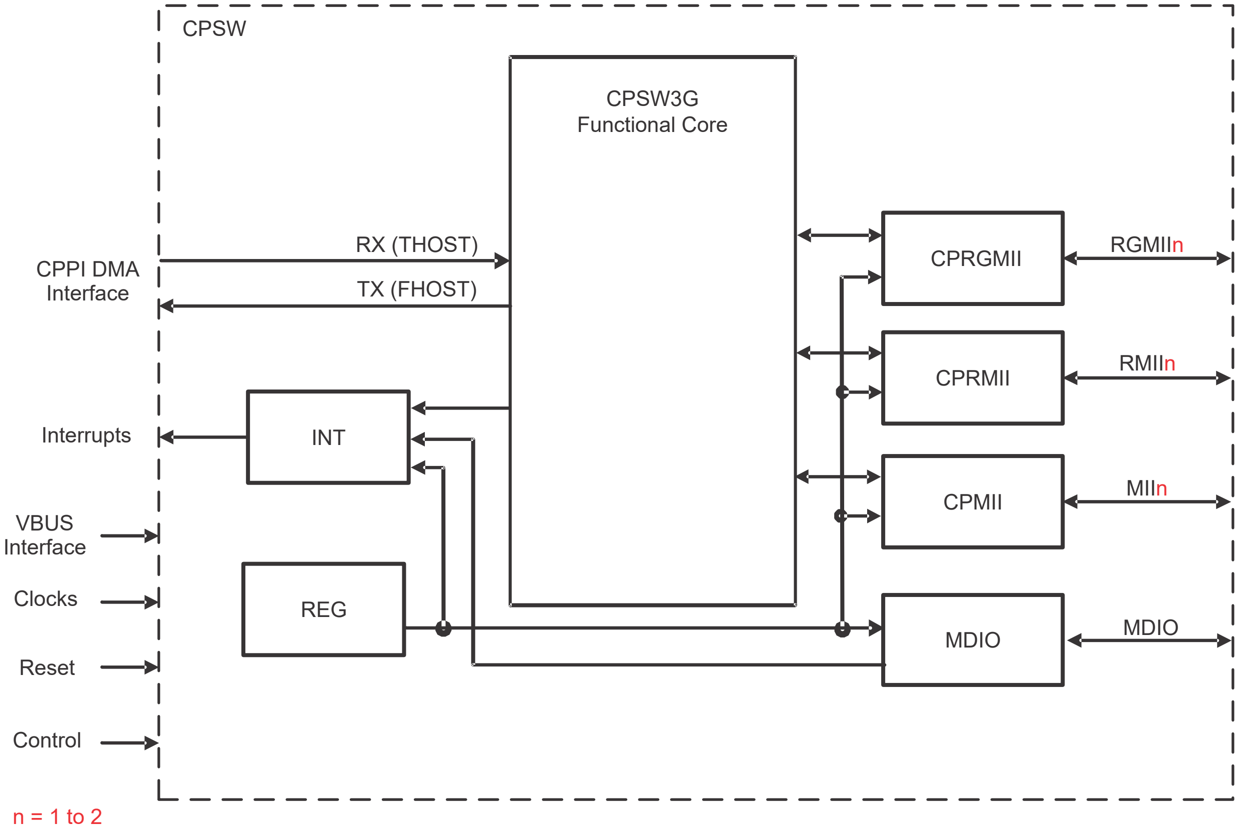

Figure 12-112. CPSW Top Level Block Diagram

12.2.1.4.2 CPSW Ports

The Ethernet Subsystem has three ports. Port 0 is the Host port (internal to the Subsystem). Port 1 and 2 are the external ports connected to RGMII, RMII, MII interfaces as per the interface selected.

Naming conventions followed in this chapter:

- Port0 is referred to the CPPI Host Port
- Port1 and 2 are referred to the interfaces RGMII/RMII/MII

12.2.1.4.2.1 Interface Mode Selection

The three-port switch (CPSW) Ethernet Subsystem has one 10/100/1000 Ethernet port with selectable RMII, RGMII, and MII interfaces.

The interface modes for all 2 Ethernet ports are selected by configuring the Ethernet interface mode selection bitfield (PORT_MODE_SEL) in the CTRLMMR_ENET1_CTRL and CTRLMMR_ENET2_CTRL registers.

See the device-specific Datasheet for configuring the pin mux mode as per the interface selected.

12.2.1.4.3 Clocking

12.2.1.4.3.1 Subsystem Clocking

CPSW clocking summary is shown in *CPSW Integration*.

12.2.1.4.3.2 Interface Clocking

Data is transmitted and received with respect to the reference clocks of the interface pins.

12.2.1.4.3.2.1 RGMII Interface Clocking

RGMII_RXC, RGMII_TXC frequencies are:

- 2.5 MHz at 10 Mbps
- 25 MHz at 100 Mbps
- 125 MHz at 1000 Mbps

Note

RGMII has ID_MODE for TX internal delay that can be controlled in register MSS_CTRL:CPSW_CONTROL

12.2.1.4.3.2.2 RMII Interface Clocking

RMII interface clock RMII_50MHZ_CLK frequency is:

- 50 MHz at 10 Mbps
- 50 MHz at 100 Mbps

For more details on RMII clocking, please see *CPSW0 Integration*

CTRLMMR_CLKOUT_CTRL[4]CLK_EN and CTRLMMR_CLKOUT_CTRL[0]CLK_SEL bits are used to enable and select the clock source for CLKOUT device pin.

12.2.1.4.3.2.3 MDIO Clocking

The MDIO clock is based on a divide-down of the interface (CPPI_ICLK) clock. The application software or driver must control the divide-down value.

See the CPSW_MDIO_CONTROL_REG register for configuring the Clock Divider ([15-0]CLKDIV) value.

12.2.1.4.4 Software IDLE

The submodule software idle register bits enable CPSW operation to be completely or partially suspended by software control. There are two CPSW submodules that contain software idle register bits. Each of the two submodules may be individually commanded to enter the idle state. The idle state is entered at packet boundaries, and no further packet operations will occur on an idled submodule until the idle command is removed. The CPSW module enters the idle state when all two submodules are commanded to enter and have entered the idle state. Idle status is determined by reading or polling the two submodule idle bits. The CPSW_3G is in the idle state when all two submodules are in the idle state. The CPSW_SOFT_IDLE_REG[0] SOFT_IDLE bit may be set if desired after the submodules are in the idle state. The SOFT_IDLE bit causes packets to not be transferred from one FIFO to another FIFO internal to the switch.

12.2.1.4.5 Interrupt Functionality

CPSW Ethernet Subsystem has six interrupt outputs:

- Cn_FH_PEND_INTR - FHost (from host to Ethernet) level interrupt
- Cn_TH_PEND_INTR - THost (from Ethernet to host) level interrupt
- Cn_TH_THRESH_PEND_INTR - THost (from Ethernet to host) non-paced level interrupt
- Cn_MISC_PEND_INTR - Miscellaneous non-paced pending interrupt
- ECC_SEC_PEND_INTR: ECC SEC pending interrupt - from CPSW ECC module. This interrupt is also included in the C0_MISC_PEND_INTR if enabled or can be used separately if desired.
- ECC_DED_PEND_INTR: ECC DED pending interrupt - from CPSW ECC module. This interrupt is also included in the C0_MISC_PEND_INTR if enabled or can be used separately.
- STAT_PEND_INTR - Statistics level interrupt
- HOST_PEND_INTR - CPDMA host error level interrupt

Note

n = 0 to $num_cores-1

12.2.1.4.5.1 EVNT_PEND Interrupt

See Section 12.2.1.4.7 , *Common Platform Time Sync (CPTS)* for more details on this interrupt.

12.2.1.4.5.2 Statistics Interrupt (STAT_PEND0)

The statistics level interrupt (STAT_PEND0) will be asserted, if enabled when any statistics value is greater than or equal to 8000 0000h. The statistics interrupt is cleared by writing to decrement any statistics values greater than 8000 0000h (such that their new values are less than 8000 0000h). The statistics are mapped into internal memory space and are 32-bits wide. The raw and masked statistics interrupt status may be read by reading the CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG and CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG registers, respectively.

The statistics interrupt is enabled by setting to 1h the TS_PEND_EN bit in the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG register.

12.2.1.4.5.3 ECC DED Level Interrupt (ECC_DED_INT)

Level interrupt (ECC_DED_INT) indicating an ECC double error has been detected.

12.2.1.4.5.4 ECC SEC Level Interrupt (ECC_SEC_INT)

Level interrupt (ECC_SEC_INT) indicating an ECC single error has been detected and corrected.

12.2.1.4.5.5 MDIO Interrupts

Normal Mode: (CPSW3_MDIO_POLL_REG[30] STATECHANGEMODE = 0h)

MDIO_LINKINT event is set if there is a change in the link state of the PHY corresponding to the address in the PHYADR_MON field of the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j register and the corresponding LINKINT_ENABLE bit is set. The MDIO_LINKINT event is also captured in the MDIO CPSW3_MDIO_LINK_INT_MASKED_REG register. When the GO bit in the CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j register transitions from 1 to 0, indicating the completion of a user access, and the corresponding USERINTMASKSET bit in the CPSW3_MDIO_USER_INT_MASK_SET_REG register is set, the MDIO_USERINT signal is asserted. The MDIO_USERINT event is also captured in the CPSW3_MDIO_LINK_INT_MASKED_REG register.

State Change Mode: (CPSW3_MDIO_POLL_REG[30] STATECHANGEMODE = 1h)

In State Change Mode, the MDIO will assert MDIO_LINKINT[0] when any bit in the MDIO CPSW3_MDIO_ALIVE_REG or CPSW3_MDIO_LINK_REG registers changes due to MDIO operations. The MDIO_LINKINT event is also captured in the CPSW3_MDIO_LINK_INT_MASKED_REG register. MDIO_LINKINT[1] output is unused in State Change Mode. The CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j registers are unused in state change mode.

Manual Mode: (CPSW3_MDIO_POLL_REG[31] MANUALMODE = 1h)

Manual Mode allows software to directly control the MDIO serial clock output (CPSW3_MDIO_MANUAL_IF_REG[2] MDIO_MDCLK_O) and the MDIO serial data output enable (CPSW3_MDIO_MANUAL_IF_REG[1] MDIO_OE). Manual Interface Mode is enabled when the MANUALMODE bit is set in the CPSW3_MDIO_POLL_REG register. Manual Mode is intended to be used by software for slow speed general purpose IO operations and not for MDIO PHY operations.

12.2.1.4.6 CPSW_3G

The CPSW_3G RMII/ RGMII interface is compliant to the IEEE Std 802.3 Specification.

The CPSW_3G contains two Ethernet port interfaces (Ethernet port 1 and 2), one CPPI packet streaming interface host port (port 0), Common Platform Time Sync (CPTS), ALE Engine and Statistics (STATS). A top-level block diagram of the CPSW_3G is shown in Figure 12-113.

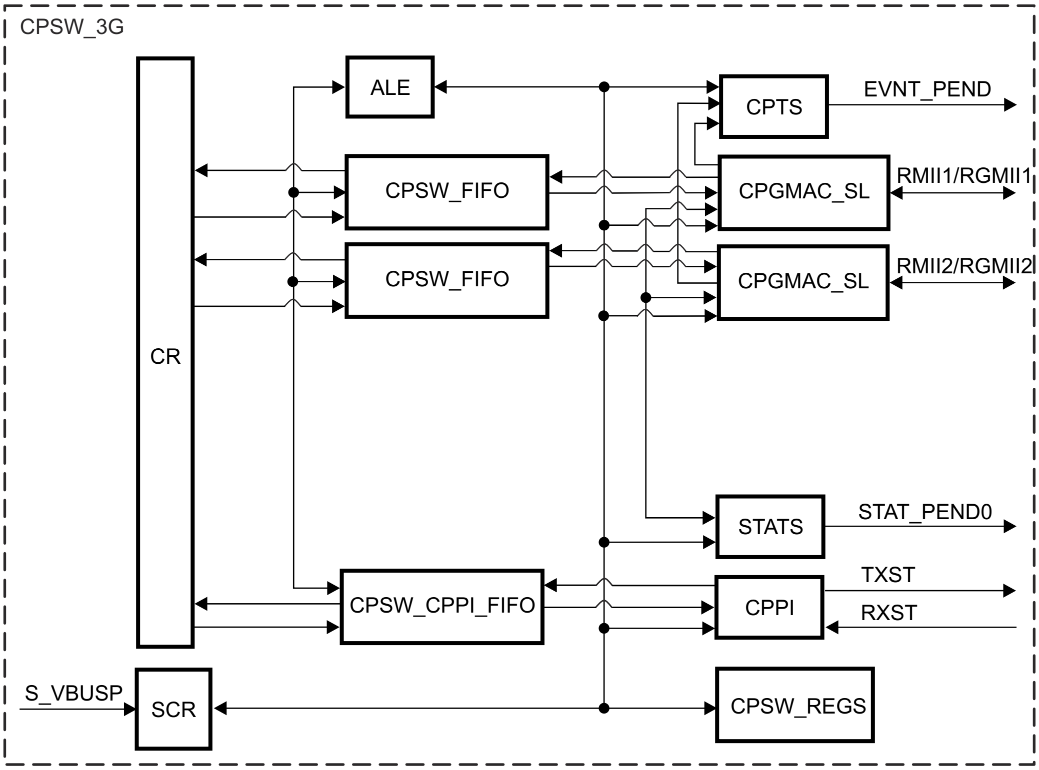

Figure 12-113. CPSW_3G Block Diagram

12.2.1.4.6.1 Address Lookup Engine (ALE)

The Address Lookup Engine (ALE) is a sub-block of the CPSW Switch and it processes all received packets and determines to which port(s) the packet should be forwarded. The ALE uses the incoming packet received port number, destination address, source address, length/type, and VLAN information to determine how the packet should be forwarded. The ALE outputs the port mask to the switch fabric that indicates the port(s) the packet should be forwarded to. The ALE is enabled when the ENABLE_ALE bit in the CPSW_ALE_CONTROL register is set. All packets are dropped when the ENABLE bit is cleared to 0.

12.2.1.4.6.1.1 Error Handling

In normal operation, the Ethernet port modules are configured drop received packages that contain errors (runt, frag, oversize, jabber, crc, alignment, code etc.). However, when the CPSW_PN_MAC_CONTROL_REG_k configuration bit(s) RX_CEF_EN, RX_CSF_EN, or RX_CMF_EN are set, received Ethernet packages with errors are transferred to the host. When the ALE receives a packet that contains errors (due to a set header error bit), or a MAC control frame and does not receive an abort, the packet will be forwarded only to the host port (port 0). Packets with errors that are forwarded to the host have no VLAN untagging or drop due to rate limiting. No ALE learning occurs on packets with errors or mac control frames. Learning is based on source address and lookup is based on destination address. Directed packets from the host are not learned, updated, or touched.

12.2.1.4.6.1.2 Bypass Operations

The ALE may be configured to operate in bypass mode by setting the ENABLE_BYPASS bit in the CPSW_ALE_CONTROL register. When in bypass mode, all Ethernet port received packets are forwarded only to the host port (port 0). In bypass mode, the ALE processes host port transmit packets the same as in normal mode. In general, packets would be directed by the host in bypass mode.

12.2.1.4.6.1.3 OUI Deny or Accept

The ALE may be configured to operate in OUI deny mode by setting the ENABLE_OUI_DENY bit in the CPSW_ALE_CONTROL register. When in OUI deny mode, a packet with a non-matching OUI source address will be dropped unless the destination address matches a multicast table entry with the SUPER bit set. When ENABLE_OUI_DENY bit is cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory address table entry. Broadcast packets will be dropped unless the broadcast address is entered into the table with the SUPER bit set. Unicast packets will be dropped unless the unicast address is in the table with BLOCK and SECURE both set (supervisory unicast packet).

12.2.1.4.6.1.4 Statistics Counting

ALE sends many statistics along with the frame routing so the CPSW can count them on a per port basis. There are many reasons to drop frames the below drop events are individually counted in CPSW per port statistics counters. For more infomraiton on ALE statistics please refer to the *CPSW Network Statistics* section.

12.2.1.4.6.1.5 Automotive Security Features

The ALE has many automotive security features that most enterprise switches do not require.

- VLANs can be configured to not allow fragmented IPv4 frames. That is a VLAN can be configured to not allow fragmented IPv4 traffic.
- VLANs can be configured to only allow up to four different IPv4 Protocols or IPv6. Next Header values, for example a VLAN can be configured to only allow TCP traffic in both IPv4 and IPv6 packets.
- Drop invalid Source Addresses, that is drop Source Addresses with bit 40 set (Multicast/Broadcast indicator on Destination Addresses)
- IEEE802.3 Length Check, drop frames that the IEEE802.3 Length is not contained within the frame. (Ether Types 0-1500)
- Any Source Address can be secured to a port dropping any attempts from other ports to masquerade as a service.
- Any source or destination address can be blocked.
- Per Port or Per VLAN ingress checking, dropping traffic from non-member ports.
- Classification, Policing on L2 and L3 information.

12.2.1.4.6.1.6 CPSW Switching Solutions

The host port can operate in many different modes as well depending on the functionality of the host. It is important to understand the modes and configure them properly.

The ALE Table is designed to maximize the modes without compromise of the system functionality as well.

12.2.1.4.6.1.6.1 Basics of 3-port Switch Type

The 3-port switch has a host port, and that port can operate in two fundamental modes. Bridge mode allows the host to extent the switched domain to another network like Wi-Fi or another multi-port switch. In this case the host must be able to see unknown unicast addresses so they can be broadcast to the other network. In Port mode the host need not see any unknown unicast traffic. The CPSW_ALE_CONTROL[8] EN_HOST_UNI_FLOOD bit determines the host mode for unknown unicast traffic. This bit should only be set if the user is bridging two or more networks together.

The 3-port switch can operate like a two-port switch using the ALE table just for the host info, the only adder is now other VLANs need to be supported for transit traffic between the external ports. This can easily be done using the default VLAN rules so no ALE table entries are used.

The 3-port switch can also operate in a fully authenticated environment where all network nodes are registered via the 802.1x based protocols. In this case the ALE table is filled with network node addresses that have been authenticated

12.2.1.4.6.1.7 VLAN Routing and OAM Operations

12.2.1.4.6.1.7.1 InterVLAN Routing

The CPSW module supports wire rate InterVLAN routing for a small number of routes, that is the host will setup an ALE classifier with an associated egress operation that will cause the CPSW to perform particular egress operations. The ALE can optionally check time to live validity as well.

The ALE uses the classifier along with an egress opcode, destination port mask and TTL check field to tell the CPSW to manipulate the packet on the egress. The CPSW will use the opcode along with a per port operation table to process the packet. By setting up the CPSW egress operation table you can replace the DA, SA and VLAN along with optionally updating the time to live IP header field. This allows the CPSW to perform the routing function for a small set of routes without getting the local host/CPU involved.

The Egress opcode will only be use for a classifier match and the packet would normally be sent only to the host. That is the host would have routed the packet but the CPSW has been configured to do the work instead. In the event that the time-to-live check feature is enabled and the time-to-live is either 0 or 1, the packet will not get the egress opcode and instead be sent to the host as if the route is not setup. This allows the host to deal with invalid TTL fields.

12.2.1.4.6.1.7.2 OAM Operations

The ALE supports OAM loopback on ports so that a remote link can be tested. That is a port placed in OAM loopback will echo packets received on a port back to the port with an egress op of 0xFF which will swap the SA and DA on egress in the CPSW.

Any supervisory packet will not be affected, so the spanning tree and other bridging functions are not affected.

Packets will only be echoed if the port is in OAM loopback mode, the received packet is not a supervisor packet. The port is in a forwarding state and the packet received DA!=SA and there are no errors in the packet.

When a port is in OAM loopback the port will not egress traffic from other ports, no address for loop backed traffic will be learned if enabled. Any packet received on the OAM loopback port with an error will be process as if the port is not in OAM. That is if the host has enabled copy errored frames the errored frames will be sent to the host instead.

12.2.1.4.6.1.8 Supervisory packets

Multicast supervisory packets are designated by the SUPER bit in the table entry. Unicast supervisory packets are indicated when BLOCK and SECURE are both set. Supervisory packets are not dropped due to rate limiting, OUI, or VLAN processing. The purpose of supervisory packets is to allow packets that would be otherwise blocked to be forwaded for special purposes.

12.2.1.4.6.1.9 Address Table Entry

The ALE table contains multiple table entry types. Each table entry represents a free entry, an address, a VLAN, an address/VLAN pair, or an OUI address. Software should ensure that there are not double address entries in the table. The double entry used would be indeterminate. Reserved table bits must be written with zeroes.

Source Address learning occurs for packets with a unicast, multicast or broadcast destination address and a unicast or multicast (including broadcast) source address. Multicast source addresses have the group bit (bit 40) cleared before ALE processing begins, changing the multicast source address to a unicast source address. A multicast address of all ones is the broadcast address which may be added to the table. A learned unicast source address is added to the table with the following control bits:

Table 12-158. Learned Address Control Bits

Bit(s)	Value
Ageable	1
Touch	1
BLOCK	0
SECURE	0

If a received packet has a source address that is equal to the destination address then the following occurs:

- The address is learned if the address is not found in the table.
- The address is updated if the address is found.
- The packet is dropped.

Table Entry Type

00 - Free Entry

01 - Address Entry : unicast or multicast determined by destination **address bit 40.**

10 - VLAN entry

11 - VLAN Address Entry : unicast or multicast determined by **address bit 40.**

12.2.1.4.6.1.9.1 Multicast Address Table Entry

Table 12-159. Multicast Address Table Entry Bit Values

70:68	67:66	65	64	63:62	61:60	59:48	47:0
Reserved	PORT_MASK	SUPER	Reserved	MCAST_FWD_STATE	ENTRY_TYPE (01)	Reserved	MULTICAST_ADDRESS

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Port Mask(1:0) (PORT_MASK)

This 2-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Multicast Forward State (MCAST_FWD_STATE)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state in order to forward the packet. If the transmit PORT_MASK has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

00 - Forwarding

01 - Blocking/Forwarding/Learning

10 - Forwarding/Learning

11 - Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.2.1.4.6.1.9.2 OUI Unicast Address Table Entry

Table 12-160. OUI Unicast Address Table Entry Bit Values

70:64	63:62	61:60	59:48	47:24	23:0
Reserved	UNICAST_TYPE (10)	ENTRY_TYPE (01)	Reserved	UNICAST_OUI	Reserved

Unicast Type (UNICAST_TYPE)

This field indicates the type of unicast address the table entry contains.

00 - Unicast address that is not ageable.

01 - Ageable unicast address that has not been touched.

10 - OUI address - lower 24-bits are don't cares (not ageable).

11 - Ageable unicast address that has been touched.

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (UNICAST_OUI)

For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup.

12.2.1.4.6.1.9.3 Unicast Address Table Entry (Bit 40 == 0)

Table 12-161. Unicast Address Table Entry Bit Values

70:69	68	67:66	65	64	63	62	61:60	59:48	47:0
RESERVED	TRUNK	PORT_NUMBER	BLOCK	SECURE	TOUCH	AGEABLE	ENTRY_TYPE (3h)	RESERVED	UNICAST_ADDRESS

Trunk Indicator (TRUNK)

0h = The port bits in the entry are the port number

1h = The port bits in the entry are the trunk number

Port Number (PORT_NUMBER)

This field indicates the port number (not port mask) that the packet with a unicast destination address may be forwarded to. Packets with unicast destination addresses are forwarded only to a single port (but not the receiving port).]

Block (BLOCK)

The block bit indicates that a packet with a matching source or destination address should be dropped (block the address).

0h = Address is not blocked.

1h = Drop a packet with a matching source or destination address (secure must be zero)

If block and secure are both set, then they no longer mean block and secure. When both are set, the block and secure bits indicate that the packet is a unicast supervisory (super) packet and they determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state.

Secure (SECURE)

This bit indicates that a packet with a matching source address should be dropped if the received port number is not equal to the table entry PORT_NUMBER.

0h = Received port number is a don't care.

1h = Drop the packet if the received port is not the secure port for the source address and do not update the address (block must be zero)

Touch Indicator (TOUCH)

Only valid when AGEABLE is a 1h.

0h = Ageable unicast address has not been touched

1h = Ageable unicast address that has been touched

Ageable (AGEABLE)

This bit indicates that the address is ageable.

0h = Unicast address that is not ageable

1h = Unicast address that is ageable

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (UNICAST_ADDRESS)

This is the 48-bit packet MAC address. All 48-bits are used in the lookup.

12.2.1.4.6.1.9.4 Multicast Address Table Entry (Bit 40==1)

Table 12-162. Multicast Address Table Entry Bit Values

70:69	68:66	65	64	63:62	61:60	59:48	47:0
RESERVED	PORT_MASK	SUPER	IGNMBITS	FWDSTLVL	ENTRY_TYPE (1h)	RESERVED	MULTICAST_ADDRESS

Port Mask(2:0) (PORT_MASK)

This 3-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Forward State Level (FWDSTLVL)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s).

A transmit port must be in the Forwarding state in order to forward the packet. If the transmit port_mask has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

0h = Forwarding

1h = Blocking/Forwarding/Learning

2h = Forwarding/Learning

3h = Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.2.1.4.6.1.9.5 VLAN/Unicast Address Table Entry (Bit 40 == 0)

Table 12-163. Unicast Address Table Entry Bit Values

70:69	68	67:66	65	64	63	62	61:60	59:48	47:0
RESERVED	TRUNK	PORT_NUMBER	BLOCK	SECURE	TOUCH	AGEABLE	ENTRY_TYPE (3h)	VLAN_ID	UNICAST_ADDRESS

Trunk Indicator (TRUNK)

0h = The port bits in the entry are the port number

1h = The port bits in the entry are the trunk number

Port Number (PORT_NUMBER)

This field indicates the port number (not port mask) that the packet with a unicast destination address may be forwarded to. Packets with unicast destination addresses are forwarded only to a single port (but not the receiving port).]

Block (BLOCK)

The block bit indicates that a packet with a matching source or destination address should be dropped (block the address).

0h = Address is not blocked.

1h = Drop a packet with a matching source or destination address (secure must be zero)

If block and secure are both set, then they no longer mean block and secure. When both are set, the block and secure bits indicate that the packet is a unicast supervisory (super) packet and they determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state.

Secure (SECURE)

This bit indicates that a packet with a matching source address should be dropped if the received port number is not equal to the table entry PORT_NUMBER.

0h = Received port number is a don't care.

1h = Drop the packet if the received port is not the secure port for the source address and do not update the address (block must be zero)

Touch Indicator (TOUCH)

Only valid when AGEABLE is a 1h.

0h = Ageable unicast address has not been touched

1h = Ageable unicast address that has been touched

Ageable (AGEABLE)

This bit indicates that the address is ageable.

0h = Unicast address that is not ageable

1h = Unicast address that is ageable

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

3h: VLAN address entry. Unicast or multicast determined by address bit 40.

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

Packet Address (UNICAST_ADDRESS)

This is the 48-bit packet MAC address. All 48-bits are used in the lookup.

12.2.1.4.6.1.9.6 VLAN/Multicast Address Table Entry (Bit 40==1)

Table 12-164. VLAN/Multicast Address Table Entry Bit Values

70:69	68:66	65	64	63:62	61:60	59:48	47:0
RESERVED	PORT_MASK	SUPER	IGNMBITS	FWDSTLVL	ENTRY_TYPE (11)	VLAN_ID	MULTICAST_ADDRESS

Port Mask(2:0) (PORT_MASK)

This 3-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Forward State Level (FWDSTLVL)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s).

A transmit port must be in the Forwarding state in order to forward the packet. If the transmit port_mask has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

0h = Forwarding

1h = Blocking/Forwarding/Learning

2h = Forwarding/Learning

3h = Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

11: VLAN address entry. Unicast or multicast determined by address bit 40.

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.2.1.4.6.1.9.7 Inner VLAN Table Entry

Table 12-165. Inner VLAN Table Entry

70:69	68:66	65	64:62	61:60	59:48	47	46:39	38:36
RESERVED	NO_LEARN_MASK	VLAN_FORCE_INGRESS_CHECK	0h	ENTRY_TYPE (1h)	VLAN_ID	NOFRAG	RESERVED	REG_MCAST_FLOOD_INDEX

35:27	26:24	23	22:15	14:12	11:3	2:0
RESERVED	FORCE_UNTAGGED_EGRESS	LMTNXTHDR	RESERVED	UREGMSK	RESERVED	VLAN_MEMBER_LIST

No Learn Mask (NO_LEARN_MASK)

When a bit is set in this mask, a packet with an unknown source address received on the associated port will not be learned (i.e. When a VLAN packet is received and the source address is not in the table, the source address will not be added to the table).

VLAN Force Ingress Check (VLAN_FORCE_INGRESS_CHECK)

If the receive port is not a member of this VLAN then the packet is dropped. This is similar to the Iy_REG_Py_VID_INGRESS_CHECK bit in the CPSW_Iy_ALE_PORTCTL0_y registers except this check is for this VLAN only (not all VLANs).

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

(NOFRAG)

VLAN No IPv4 Fragmented frames Control - Causes IPv4 fragmented IP frames to be dropped.

Registered Multicast Flood Index (REG_MCAST_FLOOD_INDEX)

This field indicates which port(s) are the registered multicast flood mask.

Force Untagged Packet Egress (FORCE_UNTAGGED_EGRESS)

This field causes the packet VLAN tag to be removed on egress for the specified port(s) (except on port 0).

VLAN Limit Next Header Control (LMTNXTHDR)

This bit causes frames to be dropped if the Protocol/Nxt Header does not match the CPSW_ALE_NXT_HDR register values.

VLAN Unregister Multicast Mask (UREGMSK)

This field indicates which port(s) are the unregistered multicast flood mask.

VLAN Member List (VLAN_MEMBER_LIST)

This field indicates which port(s) are members of the associated VLAN. One bit per port.

12.2.1.4.6.1.9.8 Outer VLAN Table Entry

Table 12-166. Outer VLAN Table Entry

70:69	68:66	65	64:62	61:60	59:48	47	46:39	38:36
RESERVED	NO_LEARN_MASK	VLAN_FORCE_INGRESS_CHECK	2h	ENTRY_TYPE (2h)	VLAN_ID	NOFRAG	RESERVED	REG_MCAST_FLOOD_INDEX

35:27	26:24	23	22:15	14:12	11:3	2:0
RESERVED	FORCE_UNTAGGED_EGRESS	LMTNXTHDR	RESERVED	UREGMSK	RESERVED	VLAN_MEMBER_LIST

No Learn Mask (NO_LEARN_MASK)

When a bit is set in this mask, a packet with an unknown source address received on the associated port will not be learned (i.e. When a VLAN packet is received and the source address is not in the table, the source address will not be added to the table).

VLAN Force Ingress Check (VLAN_FORCE_INGRESS_CHECK)

If the receive port is not a member of this VLAN then the packet is dropped. This is similar to the Iy_REG_Py_VID_INGRESS_CHECK bit in the CPSW_Iy_ALE_PORTCTL0_y registers except this check is for this VLAN only (not all VLANs).

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

(NOFRAG)

VLAN No IPv4 Fragmented frames Control - Causes IPv4 fragmented IP frames to be dropped.

Registered Multicast Flood Index (REG_MCAST_FLOOD_INDEX)

Index into CPSW_ALE_MSK_MUX0 to CPSW_Ix_ALE_MSK_MUXx register array that is used to create the registered multicast flood mask.

Force Untagged Packet Egress (FORCE_UNTAGGED_EGRESS)

This field causes the packet VLAN tag to be removed on egress for the specified port(s) (except on port 0).

VLAN Limit Next Header Control (LMTNXTHDR)

This bit causes frames to be dropped if the Protocol/Nxt Header does not match the CPSW_ALE_NXT_HDR register values.

VLAN Unregister Multicast Mask (UREGMSK)

This field indicates which port(s) are the unregistered multicast flood mask.

VLAN Member List (VLAN_MEMBER_LIST)

This field indicates which port(s) are members of the associated VLAN. One bit per port.

12.2.1.4.6.1.9.9 EtherType Table Entry

Table 12-167. EtherType Table Entry

70:65	64:62	61:60	59:16	15:0
RESERVED	4h	ENTRY_TYPE (2h)	RESERVED	ETHERTYPE

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

Ether Type (ETHERTYPE)

16-bits Ether Type field.

12.2.1.4.6.1.9.10 IPv4 Table Entry

Table 12-168. IPv4 Table Entry

70	69:65	64:62	61:60	59:32	31:0
RESERVED	IGNMBITS	6h	ENTRY_TYPE (2h)	RESERVED	IPV4ADR

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv4 Address (IPV4ADR)

32-bit IPv4 Address. Any ignored bits must be zero value in the table entry.

12.2.1.4.6.1.9.11 IPv6 Table Entry High

Table 12-169. IPv6 Table Entry High

70:64	63	62	61:60	59:0
IGNMBITS	RESERVED	(1h)	ENTRY_TYPE (2h)	IPV6ADR[127:68]

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv6 Address - upper 64 bits (IPV6ADR[127:68])

This address is plit into three fields in the IPv6 High and IPv6 Low table entry. Any ignored bits must be zero in the table entry(s).

12.2.1.4.6.1.9.12 IPv6 Table Entry Low

Table 12-170. IPv6 Table Entry Low

70:63	62	61:60	59:0
IPV6ADR[67:60]	1h	ENTRY_TYPE (2h)	IPV6ADR[59:0]

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv6 Address - upper 8 bits (IPV6ADR[67:60])

IPv6 Address - upper 60 bits (IPV6ADR[59:0])

This address is plit into three fields in the IPv6 High and IPv6 Low table entry. Any ignored bits must be zero in the table entry(s).

Note: IPV6 table address entries operate differently than all other table entry types. IPV6 table entries have a high entry concatenated with a low entry. The high entry must have an entry_pointer value of the low entry_pointer plus 0x40. Bit six of the entry_pointer must be set for the high entry and must be zero for the low entry.

12.2.1.4.6.1.10 Multicast Address

Multicast addresses are addresses with bit 40 set. Only destination addresses can be Multicast addresses. The group bit (bit 40) of the source address is reserved in the IEEE standard.

A multicast address of all ones is the broadcast address which can be added to the lookup table if forwarding of broadcast packets need be modified.

12.2.1.4.6.1.10.1 Multicast Ranges

Added IgnMbits to indicate at least one bit of the multicast address is ignored. Up to 10 bits of the multicast address can be ignored to provide the ability to create multiple multicast address ranges.

if ((IgnMbits)&(MultiCastAddress[0] ==0x000)) { MultiCastAddress[0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[1:0]==0x001)) { MultiCastAddress[1:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[2:0]==0x003)) { MultiCastAddress[2:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[3:0]==0x007)) { MultiCastAddress[3:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[4:0]==0x00F)) { MultiCastAddress[4:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[5:0]==0x01F)) { MultiCastAddress[5:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[6:0]==0x03F)) { MultiCastAddress[6:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[7:0]==0x07F)) { MultiCastAddress[7:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[8:0]==0x0FF)) { MultiCastAddress[8:0] is ignored in compare}

if ((IgnMbits)&(MultiCastAddress[9:0]==0x1FF)) { MultiCastAddress[9:0] is ignored in compare}

Below is 'C' code to modify ALE MultiCastAddress and IgnMbits when iNumOfBitsToIgnore is greater than zero. Where fGenMask(iOffset,iBitsToMask) creates a Mask for the value provided. For example fGenMast(0,5) will return 0x1F.

```
if(iNumOfBitsToIgnore)
{
int iIgnClrMsk,iIgnSetMsk;
iIgnClrMsk=fGenMask(0, iNumOfBitsToIgnore);
iIgnSetMsk=fGenMask(0, iNumOfBitsToIgnore -1);
MultiCastAddress &= ~iIgnClrMsk;
MultiCastAddress |= iIgnSetMsk;
IgnMbits = 1;
}
else
{
IgnMbits = 0;
}
```

Multicast Addresses or Ranges can overlap, in the event of an overlap; the higher ALE index will be used.

12.2.1.4.6.1.11 Aging and Auto Aging

The ALE supports software control or automatic aging of agable addresses.

Any time an agable address is seen as a source address entering from a port the source address entry will be marked as touched.

If the aging timer expires or the software sets the [29] AGE_OUT_NOW bit in the CPSW_ALE_CONTROL, the aging process will be started.

The aging process will read each ALE entry and for all entries that are an address with or without VLAN that is also agable, the touch check process will be done.

The touch check process will test the TOUCH bit and if clear, the entry will be marked as free, else the TOUCH bit will be cleared.

What this means is that if the aging interval was programmed as one second, any unused entry could stay in the ALE table for 1.000001 to 1.999999 seconds

12.2.1.4.6.1.12 ALE Policing and Classification

The ALE has a number of configurable classifier engines (policers) that can be used for classification. Classification is a subset of the policing function and uses a policer without the color marking or rate limiting functions. A policer is a hardware engine that is used for policing. The POLCNTDIV8 field in the CPSW_ALE_STATUS register indicates the number of policers available to be used for classification. Each policer can be enabled to match on one or more of any of the below packet fields for classification. All but Port and Priority are index references to the ALE table entries.

- Port Number
- Priority extracted from VLAN, mapped from DSCP if enabled, or Default Port Priority
- Organization Network Unique identifier - ONU
- Destination Address - DA
- Source Address - SA
- Outer VLANID -S-VLANID

- Inner VLANID -C-VLANID
- Ether Type
- IP Source Address - IPSA with full CIDR masking for IPv4 and IPv6
- IP Destination Address - IPSA with full CIDR masking for IPv4 and IPv6
- Support Host Thread/Flow ID mapping based on any packet classification above

12.2.1.4.6.1.12.1 ALE Policing

The policing function on each policer engine is implemented as dual-counter three-color marking engine as described in the IETF RFC2698. The first counter is the Committed Information Rate (CIR) counter and the second counter is the Peak Information Rate (PIR) counter. The policing function can use either or both counters. Based on the counter values the packet color is determined. The color is used to determine whether the packet is dropped or forwarded. The ALE has a local feature that can drop packets regardless of queue state.

The policing rates are determined by the below equations:

CIR policing rate in Mbit/s = ((ALE frequency in Mhz) * CPSW_ALE_POLICECFG7[31-0] CIR_IDLE_INC_VAL) / 32768

PIR policing rate in Mbit/s = ((ALE frequency in Mhz) * CPSW_ALE_POLICECFG6[31-0] PIR_IDLE_INC_VAL) / 32768

Each policer has 10 different match operations (see Section 12.2.1.4.6.1.12). Since multiple policing entries can be hit on a single packet this provides the ability to create precise traffic stream control.

Packets are colored at ALE lookup time. Packets can be colored RED, YELLOW, or GREEN. If multiple policers are configured for a packet stream then the packet color is merged from all matching (hit) policers. If any policer is RED then the packet is marked RED. Else if any policer is YELLOW then the packet is marked YELLOW. Otherwise the packet is marked GREEN.

The Policing engine supports several modes such that packets that don't hit a policing/classifier match can be treated as RED, YELLOW, GREEN or policer 0 color. Using policer 0 allows for a system to regulate unregulated traffic.

12.2.1.4.6.1.12.2 Classifier to Host Thread Mapping

The ALE module allows Host Thread mapping based on any packet classification. That is the ALE can generate a thread ID used by the host based on ALE classifier matches.

When enabled the highest classifier match can map to a particular thread ID value.

The ALE also supports an optional default Thread ID value in the event that no classifier match.

Each Thread ID, including the default thread ID, has an enable functionality such that, if no classifier matches occur the default value is used, if the default is not enabled, the switch will use the {port,priority} value instead. If multiple classifier matches occur, the highest matching entry with a thread enable bit set will be used.

Three registers are used for ALE classification thread mapping configuration (CPSW_ALE_THREADMAPDEF, CPSW_ALE_THREADMAPCTL and CPSW_ALE_THREADMAPVAL). The three thread mapping registers are used independently and are separate from the other ALE policing registers. The CPSW_ALE_THREADMAPCTL register allows the CPSW_ALE_THREADMAPVAL register contents to be written to the selected classifier. There is a CPSW_ALE_THREADMAPDEF register that is used for all classifiers. The thread mapping registers can be written or changed at any time but any packets that are already processed will not have their thread altered.

12.2.1.4.6.1.12.3 ALE Classification

When the policers are configured as classifiers, the color marking and policing functions of the policing/classifier engines are not used. One or multiple classifiers can be configured to match on a single packet. For example, a classifier can be enabled to match on priority while another classifier could match IP address.

12.2.1.4.6.1.12.3.1 Classifier to CPPI Transmit Flow ID Mapping

The ALE can generate a 6-bit transmit CPPI Flow ID based on classifier matches that can be used instead of the switch default transmit Flow ID mapping. The switch default flow ID is the remapped received packet priority (0 to 7). Thread and flow ID are used interchangeably for this since there is a single hardware thread (TXST_THREAD_MREADY) but there are 6-bits of FLOW_ID in the transmit CPPI INFO word 0. When enabled, the highest classifier match can map to a particular 6-bit flow ID value that is associated with the classifier. The ALE also supports an optional ALE default thread/flow ID value in the event that no classifiers match. Each thread/flow ID, including the ALE default thread/flow ID, has an enable such that the ALE default thread/Flow ID is used if enabled and if no matches occur (instead of the remapped received packet priority). If the ALE default is not enabled and no matches occur then the switch default value will be used. If multiple classifier matches occur, the highest match with a thread enable bit set will be used. The resultant flow ID has the CPSW_P0_FLOW_ID_OFFSET_REG register value added to it to determine the actual value in the INFO 0 Flow ID field.

Three registers are used for ALE classification thread/flow ID mapping configuration (CPSW_ALE_THREADMAPDEF, CPSW_ALE_THREADMAPCTL and CPSW_ALE_THREADMAPVAL). The three thread mapping registers are used independently and are separate from the other ALE policing registers. The CPSW_ALE_THREADMAPCTL register allows the CPSW_ALE_THREADMAPVAL register contents to be written to the selected classifier. There is a single CPSW_ALE_THREADMAPDEF that is used for all classifiers. The thread mapping registers can be written or changed at any time but any packets that are already processed will not have their thread altered.

12.2.1.4.6.1.13 Mirroring

The ALE supports three mirroring modes: destination port, source port and or table entry.

Destination port mirroring allows packets from any ingress port or trunk which ends up switching to a particular egress destination port or trunk to be mirrored to yet another egress destination port or trunk. For example any traffic from any port that is switched to port 'A' can be also mirrored to port 'B'. (MIRROR_DP=A, MIRROR_DEN=1h, MIRROR_TOP=B in the CPSW_ALE_CONTROL register).

Source port mirroring allows packets received on any enabled ingress source port or trunk to be switched to the mirror egress port as well as the actual egress destination ports. For example traffic received on ingress port 'A' can be switched to egress port 'B' as well as the intended egress destination port.(Iy_REG_Py_MIRROR_SP=1h in the CPSW_Iy_ALE_PORTCTL0_y register, MIRROR_SEN=1h, MIRROR_TOP=B in the CPSW_ALE_CONTROL register).

Table entry mirroring allows for any MAC Address, MAC Address with VLAN, ONU Address or VLAN entry that matches on ingress to be switched to the egress destination as well as the actual egress destination. For example all traffic for VLAN ID of 35 can be mirrored to port 'B'. That is any traffic switched on VLAN ID of 35 will be mirrored. ({VLAN ID of 35 in ALE Table entry index=C}, MIRROR_MIDX=C, MIRROR_MEN=1h, MIRROR_TOP=B)

In the event that mirrored packets are mirrored to or from a port that is also the mirror port the packet will not be duplicated or marked as a mirror packet since the packet has already been on the port as ingress or egress. The packet sent to the mirror port may have modified VLAN info based on the port and VLAN lookup table entries. The mirror port need not be a member of the VLAN ID it is mirroring, the ALE will forward traffic to the mirror port after ingress and egress filters are applied.

The switch may decide to drop any mirror traffic based on switch buffer thresholds as to prevent required traffic from becoming congested.

Port mirroring is controlled by register fields in CPSW_ALE_CONTROL, CPSW_ALE_CTRL2 and the port control registers.

- MIRROR_DP - The destination port that will have its traffic mirrored (CPSW_ALE_CONTROL register).
- MIRROR_TOP - The port to which mirrored traffic is sent (CPSW_ALE_CONTROL register).

- MIRROR_MEN - The enable for mirroring traffic that matches a supported lookup table entry (CPSW_ALE_CONTROL register).
- MIRROR_DEN - The Enable for destination port mirroring (CPSW_ALE_CONTROL register).
- MIRROR_SEN - The Enable for source port mirroring (CPSW_ALE_CONTROL register).
- MIRROR_MIDX - The index of a lookup table entry that will be mirrored CPSW_ALE_CTRL2 register).
- Iy_REG_Py_MIRROR_SP - The enable for the Source port to be mirrored. Although multiple source ports can be mirrored concurrently, a mirror traffic bandwidth issue may occur on the mirror egress port (CPSW_Iy_ALE_PORTCTL0_y register).

12.2.1.4.6.1.14 Trunking

The ALE supports port trunking of any port in any of four trunk groups. That is, four trunk groups can be supported with up to eight ports in each trunk group. There are no port adjacency rules for trunk groups. When ports are a member of a trunk group, addresses added and used in the lookup table will refer to the trunk group rather than port as indicated in the lookup table entries. If ports are removed from a trunk group, the ALE will redistribute the traffic based on the crc polynomial of enabled fields and the remaining ports within the trunk group. A trunk group may contain only one port. Packet priority, DA, SA, C-VLAN ID, IPv4SA, IPv4DA, IPv6SA, and/or IPv6DA can be used in the hash to generate destination port within the trunk group. If all hash enables are disabled, the packet can be directed to a particular port within the trunk group which allows for testing paths etc. A host directed frame is directed to the directed port regardless of trunk group settings.

Trunking is controlled through fields in the CPSW_ALE_CTRL2 register and in each ALE CPSW_Iy_ALE_PORTCTL0_y register:

- TRK_EN_DST - Enable destination address hashing for trunk port calculation.
- TRK_EN_SRC - Enable source address hashing for trunk port calculation.
- TRK_EN_PRI - Enable priority hashing for trunk port calculation.
- TRK_EN_IVLAN - Enable inner C-VLAN ID hashing for trunk port calculation.
- TRK_EN_SIP - Enable source IP address hashing for trunk port calculation.
- TRK_EN_DIP - Enable destination IP address hashing for trunk port calculation.
- TRK_BASE - Hashing formula starting value and test port offset.
- Iy_REG_Py_TRUNKEN - Enable this port as a trunk group
- Iy_REG_Py_TRUNKNUM - Trunk group number defines this port as a member of a particular trunk group.

12.2.1.4.6.1.15 DSCP

The ALE can map DSCP field to priority prior to classification matching. When enabled the DSCP is mapped via 64 priority entries such that any DSCP value can be mapped to any of the eight priorities. When a packet is received without a VLAN priority this remapped priority can be used instead of the default Port VLAN priority field. See CPSW_P0_RX_DSCP_MAP_REG_y and CPSW_PN_RX_DSCP_MAP_REG_y registers in the Register Manual section for DSCP mapping.

12.2.1.4.6.1.16 Packet Forwarding Processes

There are four processes that an incoming received packet may go through to determine packet forwarding. The processes are *Ingress Filtering*, *VLAN_Aware Lookup*, and *Egress.*

Packet processing begins in the Ingress Filtering process. Each port has an associated packet forwarding state that can be one of four values (Disabled, Blocked, Learning, or Forwarding). The default state for all ports is Disabled. The host sets the packet forwarding state for each port.

In the packet ingress process (receive packet process), there is a forward state test for unicast destination addresses and a forward state test for multicast addresses. The multicast forward state test indicates the port states required for the receiving port in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state for the packet to be forwarded for transmission. The MCAST_FWD_STATE indicates the required port state for the receiving port as indicated in the preceding table. The unicast forward state test indicates the port state required for the receiving port in order to forward the unicast packet. The transmit port must be in the Forwarding state in order to forward the packet. The BLOCK and SECURE bits determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state. The transmit port must be in the Forwarding state regardless. The forward state test used in the ingress process is determined by the destination address packet type (multicast/unicast).

In general, packets received with errors are dropped by the address lookup engine without learning, updating, or touching the address. The error condition and the abort are indicated by the Ethernet port to the ALE. Packets with errors may be passed to the host (not aborted) by a Ethernet port, if the port has the RX_CMF_EN, RX_CEF_EN, or RX_CSF_EN bit(s) set in the CPSW_PN_MAC_CONTROL_REG register. Error packets that are passed to the host by the Ethernet port are considered to be bypass packets by the ALE and are sent only to the host. Error packets do not learn, update, or touch addresses regardless of whether they are aborted or sent to the host. Packets with long or short errors received by the host are dropped. Packets with errors received by the host are forwarded as normal.

The following control bits are in the CPSW_PN_MAC_CONTROL_REG register:

- [22] RX_CEF_EN - enables frames that are fragments, long, jabber, CRC, code, and alignment errors to be forwarded
- [23] RX_CSF_EN - enables short frames to be forwarded
- [24] RX_CMF_EN - enables MAC control frames to be forwarded.

12.2.1.4.6.1.16.1 Ingress Filtering Process

Condition and action
If ((ALE BYPASS) and (host port is not the receive port)) then use host portmask and go to Egress process
if (directed packet) then use directed port number and go to Egress process
If (Rx ly_REG_Py_PORTSTATE is Disabled) then discard the packet
if ((ALE BYPASS or error packet) and (host port is not the receive port)) then use host portmask and go to Egress process
if (((BLOCK) and (unicast source address found)) or ((BLOCK) and (unicast destination address found))) then discard the packet
if ((ENABLE_RATE_LIMIT) and (rate limit exceeded) and (not BCAST_MCAST_CTL) then if (((Multicast/Broadcast destination address found) and (not SUPER)) or (Multicast/Broadcast destination address not found)) then discard the packet
if ((not forward state test valid) and (destination address found)) then discard the packet to any port not meeting the requirements • Unicast destination addresses use the unicast forward state test and multicast destination addresses use the multicast forward state test.
if ((destination address not found) and ((not transmit port forwarding) or (not receive port forwarding))) then discard the packet to any ports not meeting the above requirements

if (source address found) and (secure) and (not block) and (receive port number != port_number)) then discard the packet
if ((not super) and (drop_untagged) and ((non-tagged packet) or ((priority tagged) and not(en_vid0_mode)) then discard the packet

If (VLAN_Unaware)
CPSW_ALE_UVLAN_UNTAG = “000”
CPSW_ALE_UVLAN_RMCAST = “111”
CPSW_ALE_UVLAN_URCAST = “111”
CPSW_ALE_UVLAN_MEMBER = “111”
else if (VLAN not found)
CPSW_ALE_UVLAN_UNTAG = CPSW_ALE_UVLAN_UNTAG
CPSW_ALE_UVLAN_RMCAST = CPSW_ALE_UVLAN_RMCAST
CPSW_ALE_UVLAN_URCAST = CPSW_ALE_UVLAN_URCAST
CPSW_ALE_UVLAN_MEMBER = CPSW_ALE_UVLAN_MEMBER
else
CPSW_ALE_UVLAN_UNTAG = found CPSW_ALE_UVLAN_UNTAG
CPSW_ALE_UVLAN_URCAST = found CPSW_ALE_UVLAN_URCAST
CPSW_ALE_UVLAN_RMCAST = found CPSW_ALE_UVLAN_RMCAST
CPSW_ALE_UVLAN_MEMBER = found CPSW_ALE_UVLAN_MEMBER

if ((not SUPER) and (Iy_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member)) then discard the packet
if ((ENABLE_AUTH_MODE) and (source address not found) and not(destination address found and (SUPER))) then discard the packet
if (destination address equals source address) then discard the packet
if (VLAN_AWARE) goto VLAN_Aware_Lookup process else goto VLAN_Unaware_Lookup process

12.2.1.4.6.1.16.2 VLAN_Aware Lookup Process

Condition and action
if ((unicast packet) and (destination address found with or without VLAN) and (not SUPER) then portmask is the logical "AND" of the PORT_NUMBER and UVLAN_MEMBER_LIST less the host port and goto Egress process
if ((unicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical “AND” of the PORT_NUMBER and the UVLAN_MEMBER_LIST and goto Egress process

if ((unicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_NUMBER and goto Egress process
if (Unicast packet) # destination address not found then portmask is VLAN member LIST less host port and goto Egress process
if ((Multicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical "AND" of CPSW_ALE_UVLAN_URCAST and found destination address/VLAN portmask (PORT_MASK) and UVLAN_MEMBER_LIST and goto Egress process
if ((Multicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_MASK and goto Egress process
if (Multicast packet) # destination address not found then portmask is the logical "AND" of CPSW_ALE_UVLAN_URCAST and UVLAN_MEMBER_LIST then goto Egress process
if (Broadcast packet) then use found UVLAN_MEMBER_LIST and goto Egress process

Note

The UVLAN_MEMBER_LIST, UVLAN_UNREG_MCAST_FLOOD_MASK, UVLAN_REG_MCAST_FLOOD_MASK and UVLAN_FORCE_UNTAGGED_EGRESS are set in the Section 12.2.1.4.6.1.16.1 *Ingress Filtering Process*, based on VLAN_Unaware, Unknown_VLAN rules and VLAN table entries.

12.2.1.4.6.1.16.3 Egress Process

Condition and action
Clear Rx port from portmask (don't send packet to Rx port).
Clear disabled ports from portmask.
if ((ENABLE_OUI_DENY) and (OUI source address not found) and (not ALE BYPASS) and (not error packet) and ((not mcast destination address) and (SUPER))) then Clear host port from portmask
if ((not ENABLE_OUI_DENY) and (OUI source address found) and (not ALE BYPASS) and (not error packet) and not ((mcast destination address) and (SUPER))) then Clear host port from portmask
if ((ENABLE_RATE_LIMIT) and (BCAST_MCAST_CTL)) then if (not SUPER) and (rate limit exceeded on any tx port) then clear rate limited tx port from portmask If address not found then SUPER cannot be set.
If portmask is zero then discard packet

Send packet to portmask ports.

12.2.1.4.6.1.16.4 Learning/Updating/Touching Processes

The learning, updating, and touching processes are applied to each receive packet that is not aborted. The processes are concurrent with the packet forwarding process. In addition to the following, a packet must be received without error in order to learn/update/touch an address.

12.2.1.4.6.1.16.4.1 Learning Process

The learning process is applied to each receive packet that is not aborted. The learning process is a concurrent process with the packet forwarding process.

Condition and action
If (directed) then do not learn, update, or set touched else continue
If (not (Learning or Forwarding) or (ENABLE_AUTH_MODE) or (packet error) or (Iy_REG_Py_NO_LEARN)) then do not learn address
if ((Non-tagged packet) and (Iy_REG_Py_DROP_UN_TAGGED)) then do not learn address
if ((VLAN_AWARE) and (VLAN not found) and (unknown UVLAN_MEMBER_LIST = “000”)) then do not learn address
if ((Iy_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member) and (VLAN found)) then do not learn address
if ((source address found) and (receive port_number != PORT_NUMBER) and (SECURE or BLOCK)) then do not update address else continue
if ((source address found) and (receive port number != PORT_NUMBER)) then update address else continue
if ((source address not found) and (VLAN_AWARE) and not (LEARN_NO_VLANID)) then learn address with VLAN
if ((source address not found) and ((not VLAN_AWARE) or (VLAN_AWARE and LEARN_NO_VLANID))) then learn address without VLAN

12.2.1.4.6.1.16.4.2 Updating Process

Condition and action
if (dlr_unicast) then do not update address
If (not(Learning or Forwarding) or (ENABLE_AUTH_MODE) or (packet error) or (Iy_REG_Py_NO_SA_UPDATE)) then do not update address
if ((Non-tagged packet) and (Iy_REG_Py_DROP_UN_TAGGED)) then do not update address

```
if ((VLAN_AWARE) and (VLAN not found) and (unknown UVLAN_MEMBER_LIST = “000”))
    then do not update address
```

```
if ((Iy_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member) and (VLAN found))
    then do not update address
```

```
if ((source address found) and (receive port number != PORT_NUMBER) and (SECURE or BLOCK))
    then do not update address
```

```
if ((source address found) and (receive port number != PORT_NUMBER))
    then update address
```

12.2.1.4.6.1.16.4.3 Touching Process

```
if ((source address found) and (ageable) and (not touched))
    then set touched
```

12.2.1.4.6.1.17 VLAN Aware Mode

The CPSW is in VLAN aware mode when the VLAN_AWARE bit is set in the CPSW_CONTROL_REG register.

In VLAN aware mode, transmitted packet data is changed depending on the packet type (PKT_TYPE), packet priority (PKT_PRI), and VLAN information.

The VLAN_LTYPE_SEL value is selected by the S_CN_SWITCH bit in the CPSW_CONTROL_REG register and is either the VLAN_LTYPE_INNER (8100h default) or VLAN_LTYPE_OUTER (88A8h default) value.

12.2.1.4.6.1.18 VLAN Unaware Mode

An egress port is operating in the VLAN unaware mode when the VLAN_AWARE bit in the CPSW_CONTROL_REG register is cleared to 0h. In VLAN unaware mode, transmit (egress) packets are not modified on egress.

12.2.1.4.6.2 Packet Priority Handling

Packets are received on two ports, one Ethernet port and one CPPI host port. Received packets have a received packet priority (0 to 7, with 7 being the highest priority).

The received packet priority is determined as follows:

1. If the first packet LTYPE = VLAN_LTYPE_SEL then the received packet priority is the packet priority (VLAN tagged and priority tagged packets).
2. Else if the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW_P0_CONTROL_REG or CPSW_PN_CONTROL_REG, then the received packet priority is the 6-bit TOS field in byte 15 (upper 6 bits) mapped through the port’s DSCP priority mapping registers (IPv4 packet).
3. Else if the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in CPSW_P0_CONTROL_REG or CPSW_PN_CONTROL_REG, then the received packet priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port’s DSCP priority mapping registers (IPv6 packet).
4. Else the received packet priority is the source (ingress) port priority.

The received packet priority is mapped through the receive ports associated packet-priority-to-header-packet-priority-mapping register (CPSW_PN_RX_PRI_MAP_REG) to obtain the header packet priority. The header packet priority is the hardware switch priority. The header packet priority is also used as the actual transmit packet priority if the VLAN information is to be sent on egress.

The header packet priority is mapped at each destination FIFO through the CPSW_PN_TX_PRI_MAP_REG register (header priority to switch priority mapping register) to obtain the hardware switch priority (hardware queue 0 through 7).

12.2.1.4.6.2.1 Priority Mapping and Transmit VLAN Priority

There are three priorities that are used inside the Gigabit Ethernet Switch: **packet priority**, **header packet priority**, and **switch priority**. The **header packet priority** is used as the outgoing VLAN priority if the packet is egressing from the switch with a VLAN tag. The **switch priority** determines which of the 8 FIFO priority queues the packet uses during egress.

Figure 12-114 below, as well as the corresponding explanation that follows, explains each of the priorities, how they are determined, and how they are used. A number in parentheses in the figure indicates a process (Ethernet port ingress, host port egress, etc.). Each bullet in the text following the diagram explains one of the 5 processes pointed out in the figure.

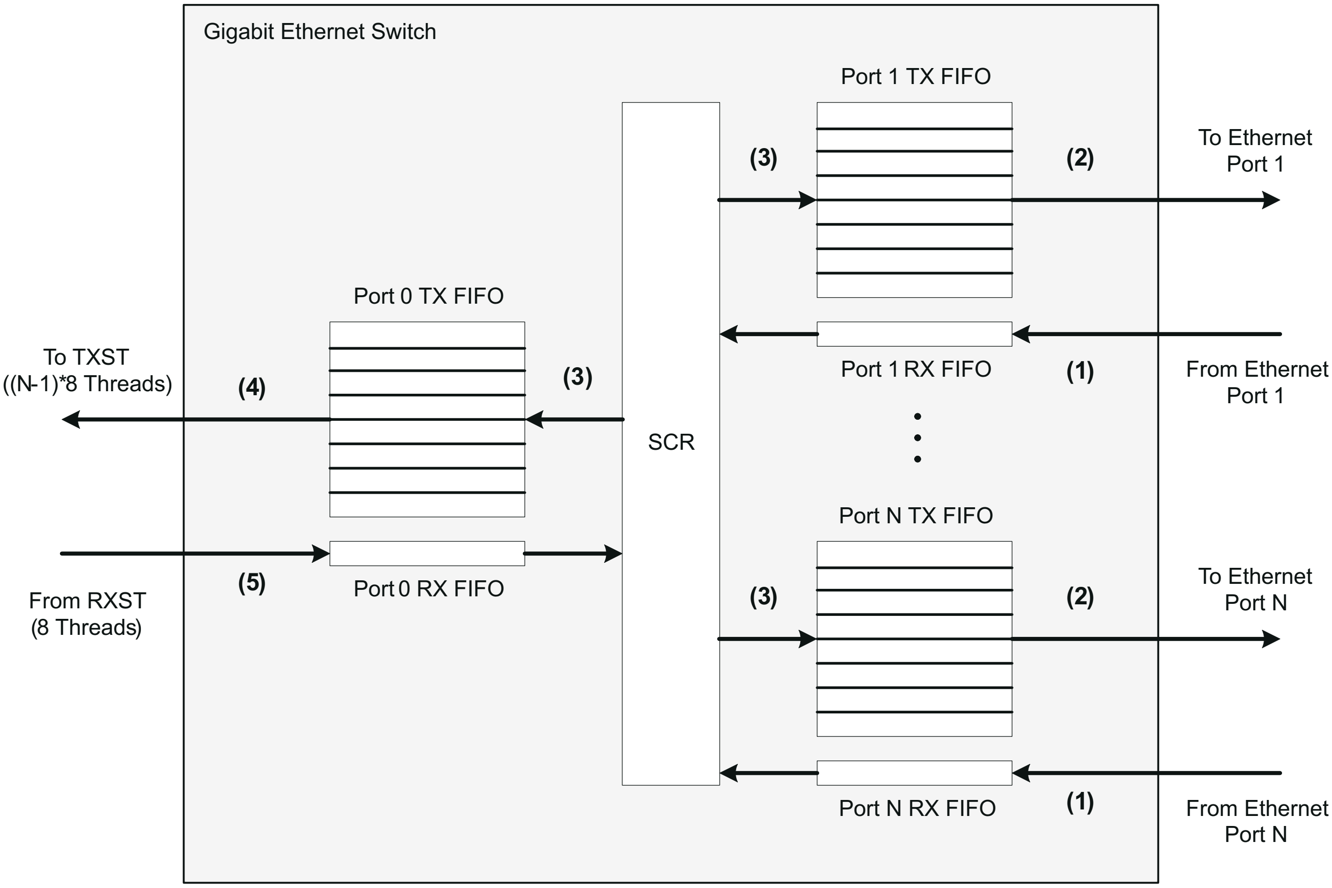

Figure 12-114. Gigabit Ethernet Switch Priority Mapping and Transmit VLAN Processing

From Figure 12-114 above:

- (1) is the ingress process that occurs at the external Ethernet ports
  - The incoming packet is assigned a **packet priority** based on either its VLAN priority, IPv4 or IPv6 DSCP value, or the ingress port's priority. This **packet priority** is then mapped to a **header packet priority** using the CPSW_PN_RX_PRI_MAP_REG register where N is the port where the packet entered the switch. This process is explained in further detail in Section 12.2.1.4.6.2 .
- (2) is the egress process that occurs at the external Ethernet ports
  - If the switch is in VLAN Aware mode then the VLAN header may be added, replaced, or removed during the egress process. If the VLAN header is to be added or replaced, the VLAN priority will come from the **header packet priority** that was determined in process (1) or (5). Transmit VLAN processing is the same for both the host port and the external Ethernet ports and is described in Section 12.2.1.4.6.4.1 .
- (3) is the process by which it is decided which priority TX queue to place the packet on in the Port N TX FIFO during egress
  - Each Port's TX FIFO has 8 queues that each correspond to a priority that is used when determining which packet will egress from the switch next at that port. The **header packet priority** (Ethernet port ingress, process (1)) or the receive packet thread (host port 0 ingress, process (5)) gets mapped through the CPSW_PN_RX_PRI_MAP_REG register (where N is the egress port number) to determine the **switch priority** of the packet. The **switch priority** determines which TX FIFO queue to place the packet in. The FIFO architecture is described in Section 12.2.1.4.6.10.5 . The header packet priority to switch priority mapping is discussed in Section 12.2.1.4.6.2 .
- (4) is the egress process that occurs at Host Port 0 toward the transmit streaming interface (TXST)
  - The TXST has 8 egress threads for each external Ethernet port (32 threads in a 5-port switch and 64 threads in a 9-port switch). The TX thread that is selected for a packet is determined by the Ethernet port of ingress and the **switch priority** of the packet that was determined in process (3).
  - If the switch is in VLAN Aware mode then the VLAN header may be added, replaced, or removed during the egress process. If the VLAN header is to be added or replaced, the VLAN priority will come from the **header packet priority** that was determined in process (1). Transmit VLAN processing is the same for both the host port and the external Ethernet ports and is described in Section 12.2.1.4.6.4.1 .
- (5) is the ingress process that occurs at Host Port 0
  - The incoming packet is assigned a **packet priority** based on either its VLAN priority, IPv4 or IPv6 DSCP value, or the host port's priority. This packet priority is then mapped to a **header packet priority** using the CPSW_PN_RX_PRI_MAP_REG register.
  - Host port 0 also has a received packet thread. The receive packet thread is based on either the packet's VLAN priority, IPv4 or IPv6 DSCP value, or the streaming interface (RXST) thread that the packet entered host port 0 on.

12.2.1.4.6.3 CPPI Port Ingress

Packets received on the CPPI host port have a received packet priority (0 to 7 with 7 being the highest priority).

The received packet priority is determined as follows:

1. If the first packet LTYPE = VLAN_LTYPE_SEL then the received packet priority is the packet priority (VLAN tagged and priority tagged packets).
2. Else if the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW_P0_CONTROL_REG or CPSW_PN_CONTROL_REG register, then the received packet priority is the 6-bit TOS field in byte 15 (upper 6 bits) mapped through the port's DSCP priority mapping registers (IPv4 packet).
3. Else if the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in CPSW_P0_CONTROL_REG or CPSW_PN_CONTROL_REG register, then the received packet priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port's DSCP priority mapping registers (IPv6 packet).
4. Else the received packet priority is the source (ingress) port priority

The CPPI Port (port 0) also has a received packet thread. The received packet thread is determined exactly as the received packet priority except for untagged packets. For untagged packets, the received packet thread is the packet streaming interface thread that the packet was received on (instead of the port VLAN priority or DSCP priority). The received packet thread is the hardware switch priority. The received packet thread only determines which hardware switch priority the packet should be sent to, the egress VLAN rules are identical to packets that were received on Ethernet ports (as determined by the header packet priority).

For CPPI ingress packets, the destination port hardware switch priority is the below selected value remapped through CPSW_PN_RX_PRI_MAP_REG:

1. If the ingress packet is priority tagged or vlan tagged:
   - If RX_REMAP_VLAN in CPSW_P0_CONTROL_REG register is clear then the the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_VLAN in CPSW_P0_CONTROL_REG register is set then the the destination hardware switch priority is the packet priority value. Port transmit remapping (CPSW_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
2. Else if the ingress packet has the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW_P0_CONTROL_REG register:
   - If RX_REMAP_DSCP_V4 bit in CPSW_P0_CONTROL_REG register is clear then the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_DSCP_V4 bit in CPSW_P0_CONTROL_REG register is set then the destination hardware switch priority is the 6-bit TOS field in byte 15 (upper 6-bits) mapped through the port's DSCP priority mapping registers (IPV4 packet). Port 1 transmit remapping (CPSW_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
3. Else if the ingress packet has the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in P0_CONTROL_REG register:
   - If RX_REMAP_DSCP_V6 bit in CPSW_P0_CONTROL_REG register is clear then the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_DSCP_V6 bit in CPSW_P0_CONTROL_REG register is set then the destination hardware switch priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port's DSCP priority mapping registers (IPV6 packet). Port 1 transmit remapping (CPSW_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
4. Else the ingress packet is non-tagged and the destination hardware switch priority is the CPPI receive thread number.

12.2.1.4.6.4 Packet CRC Handling

The P0_TX_CRC_REMOVE bit in the CPSW_CONTROL_REG register determines if host port egress packets have CRC included or not. If P0_TX_CRC_REMOVE is set to 1h then all packets that are transmitted from port 0 do not contain CRC. If P0_TX_CRC_REMOVE bit is cleared to 0h then all packets that are transmitted from port 0 contain CRC. The CRC type, if present, is determined by the CRC_TYPE bit in the CPSW_PN_MAC_CONTROL_REG register. If the CRC_TYPE bit is cleared to 0h then the CRC present in each packet after host port egress is Ethernet CRC. If the CRC_TYPE bit is set to 1h then the CRC present in each packet after host port egress is Castagnoli CRC.

Note

The CRC type present in the packet after host port egress is determined solely by the CRC_TYPE bit in the CPSW_PN_MAC_CONTROL_REG register regardless of the CRC type present in the packet during Ethernet port ingress.

12.2.1.4.6.4.1 Transmit VLAN Processing

Transmit packets are NOT modified during switch egress when the VLAN_AWARE bit in the CPSW_CONTROL_REG register is cleared to 0h. This means that the switch is not in VLAN-aware mode.

The next three sections cover transmit processing when the switch is in VLAN-aware mode for different packet types. The Gigagibit Ethernet switch is in VLAN-aware mode when the VLAN_AWARE bit is set in the CPSW_CONTROL_REG register. While in VLAN-aware mode, VLAN is added, removed, or replaced according to the type of packet as well as the CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header as explained below.

12.2.1.4.6.4.1.1 Untagged Packets (No VLAN or Priority Tag Header)

Untagged packets are all packets that are not a VLAN packet or a priority tagged packet. According to the CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header the packet may exit the switch with a VLAN tag inserted or the packet may leave the switch unchanged. The two cases are discussed below.

- Insert VLAN Case:

  Untagged input packets have the header packet VLAN inserted when the CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the transmit packet header is de-asserted. For untagged packets, the VLAN EtherType = 0x8100 is inserted after the source address followed by the two byte header packet VLAN. The header packet VLAN is composed of the header packet priority along with the PORT_CFI and and PORT_VID values from the CPSW_PN_PORT_VLAN_REG register (where N is the port that the untagged packet entered the switch) through. The packet length/type field is output four bytes later than it is input and is not removed or replaced. If the CRC is present in the packet data (PASS_CRC is asserted), then the packet CRC is replaced with a hardware generated CRC.

- No Change Case:

  Untagged input packets are output unchanged when the CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS transmit packet header bit is asserted.

12.2.1.4.6.4.1.2 Priority Tagged Packets (VLAN VID == 0 && EN_VID0_MODE ==0h)

Priority tagged packets are packets that contain a VLAN header with VID = 0. According to the CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header, priority tagged packets may exit the switch with their VLAN ID and priority replaced or they may have their priority tag completely removed. The two cases are discussed below.

Note

In order for a priority tagged packet to fall into this category the ENABLE_VID0_MODE bit in the CPSW_ALE_CONTROL register must also be set to 0h. If the ENABLE_VID0_MODE bit in the CPSW_ALE_CONTROL register is set to 1h, then packets with a VLAN VID of 0 will fall into the VLAN Tagged Packets category in Section 12.2.1.4.6.4.1.3 below.

- Replace Priority and VLAN ID Case:

  Priority tagged input packets have the packet VLAN ID and the packet priority replaced with the header packet VLAN ID and the header packet priority when the transmit packet header CPSW_FORCE_UNTAGGED_EGRESS_REG[1-0] MASK bit is de-asserted. The header packet VLAN ID comes from the PORT_VID bits in the CPSW_PN_PORT_VLAN_REG register (where N is the port where the packet entered the switch). The header packet priority is based on the packet priority to header packet priority mapping in the CPSW_PN_RX_PRI_MAP_REG register (where N is the port where the packet entered the switch).

- Remove VLAN Header Case:

Priority tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is asserted. The 0x8100 EtherType is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the PASS_CRC input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority-tagged packets use all four input CRC bytes as pad, input 65-byte priority-tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the PASS_CRC input bit is not asserted - input 64-67 byte (on the wire) priority-tagged packets go out as 60-63 byte packets. The output CRC is replaced with a generated CRC when the VLAN is removed.

12.2.1.4.6.4.1.3 VLAN Tagged Packets (VLAN VID != 0 || (EN_VID0_MODE ==1h && VLAN VID ==0))

VLAN tagged packets are packets that contain a VLAN header specifying the VLAN the packet belongs to (VID), the packet priority (PRI), and the drop eligibility indicator (CFI). According to the CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header, VLAN tagged packets may exit the switch with their VLAN priority replaced or they may have their VLAN header completely removed. The two cases are discussed below.

- Replace Priority Case:

  VLAN tagged input packets are output with the packet priority replaced with the header packet priority when the transmit packet header CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is deasserted. The header packet priority is based on the packet priority to header packet priority mapping in the CPSW_PN_RX_PRI_MAP_REG register (where N is the port where the packet entered the switch). If the CRC is present in the packet data (PASS_CRC is asserted), then the packet CRC is replaced with a generated CRC.

- Remove VLAN Header Case:

  VLAN tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header CPSW_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is asserted. The 0x8100 EtherType is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the PASS_CRC input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority tagged packets use all four input CRC bytes as pad, input 65-byte priority tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the PASS_CRC input bit is not asserted - input 64-67 byte (on the wire) priority tagged packets go out as 60-63 byte packets. The output CRC is replaced with a generated CRC when the VLAN is removed.

12.2.1.4.6.4.2 Ethernet Port Ingress Packet CRC

All Ethernet ports check the ingress packet CRC in all modes/speeds. The receive port can check either Ethernet CRC or Castagnoli CRC as determined by the CRC_TYPE bit in the CPSW_PN_MAC_CONTROL_REG register.

12.2.1.4.6.4.3 Ethernet Port Egress Packet CRC

Ethernet ports transmit each egress packet with the CRC selected by the CRC_TYPE bit in the CPSW_PN_MAC_CONTROL_REG register, regardless of the type of CRC that the packet had on ingress to the switch. At the egress port after passing through the switch, the packet CRC is checked for correctness and if the CRC is correct then the packet is output with the generated selected output CRC. If the packet CRC is incorrect, due either to a bit flip in a memory or an error CRC passed in on host ingress, then the generated egress CRC type is used with at least a single byte of the CRC inverted to indicate the error. If the packet length including CRC is divisible by 4 then all 4 CRC bytes will be inverted on error. If there are three bytes remainder after dividing the packet length by 4 then three bytes will be inverted (and so on down to one byte remainder).

12.2.1.4.6.4.4 CPPI Port Ingress Packet CRC

CPPI port ingress packets can be passed in with or without a CRC. The host port is Ethernet CRC only. CPPI ingress packets are not checked for CRC correctness on CPPI ingress, however they are checked for correctness on Ethernet egress and are output with a CRC error if they came in with a CRC error. If a CPPI ingress packet does not have the INFO0 PASSED_CRC bit set then a CRC will be generated for the packet on CPPI ingress. If the PASSED_CRC bit is set then the packet is received and forwarded unchanged. The CRC type is input in the INFO0 word CRC_TYPE bit and must be Ethernet CRC.

12.2.1.4.6.4.5 CPPI Port Egress Packet CRC

The P0_TX_CRC_REMOVE bit in the CPSW_CONTROL_REG register determines if CPPI egress packet have an Ethernet CRC included or not.

12.2.1.4.6.5 FIFO Memory Control

Each of the two CPSW_3G ports has an identical associated FIFO. Each FIFO contains a single logical receive queue and eight logical transmit queues (priority 0 through 7 with 7 the highest priority). Each FIFO memory contains 20,480 bytes (20k) total organized as 2560 by 64-bit words contained in a single memory instance. The FIFO memory is used for the associated port transmit and receive queues. The TX_MAX_BLKS field in the FIFOs associated CPSW_PN_MAX_BLKS_REG register determines the maximum number of 1k FIFO memory blocks to be allocated to the eight logical transmit queues (transmit total). The RX_MAX_BLKS field in the FIFO's associated CPSW_PN_MAX_BLKS_REG register determines the maximum number of 1k memory blocks to be allocated to the logical receive queue. The TX_MAX_BLKS value plus the RX_MAX_BLKS value must sum to 20 (the total number of blocks in the FIFO). If the sum were less than 20, then some memory blocks would be unused. The default is 17 (decimal) transmit blocks and three receive blocks. The FIFOs follow the naming convention of the Ethernet ports. Host Port is Port0 and External Ports is Port1.

Each transmit FIFO contains a configurable number of blocks (20 max) that are either 1k or 4k byte blocks that can be allocated to any priority.

12.2.1.4.6.6 FIFO Transmit Queue Control

There are eight transmit queues in the Ethernet port transmit FIFO. Software has some flexibility in determining how packets are loaded into the queues and on how packet priorities are selected for transmission (how packets are removed and transmitted from queues).

12.2.1.4.6.6.1 CPPI Port Receive Rate Limiting

Port 0 receive operations can be configured to rate limit the host ingress data for each receive thread (priority). CPPI Receive has 8 threads for QOS. There is a committed information rate (CPSW_P0_PRI_CIR_REG_y, where y = 0 to 7) and an excess information rate for each thread (CPSW_P0_PRI_EIR_REG_y, where y = 0 to 7). Rate limiting is enabled for a thread when the committed information rate for the thread is non-zero. The excess information rate for a priority is enabled when the excess information rate for the priority is non-zero. The committed information rate must be non-zero if the excess information rate is configured to be non-zero. That is, there must be a configured non-zero committed information rate for there to be a configured non-zero excess information rate. Bulk traffic on other non-rate limited priorities does not impact the committed information traffic on a priority. However, bulk traffic on other non-rate limited threads does impact the excess information rates. No bulk thread will be enabled to send unless there are CPSW_PN_PRI_CTL_REG[15-12] TX_HOST_BLKS_REM number of unused blocks remaining in each of the Ethernet port transmit FIFOs. The “blocks remaining check” ensures that bulk traffic from the host will not block rate-limited traffic from the host. Rate limited channels must be the highest priority channels. For example, if two rate limited channels are required then threads 7 and 6 should be configured for committed information (and excess information if desired). When any channels are configured to be rate-limited, the priority type must be fixed for receive. Round-robin priority type is not allowed when rate-limiting is configured for any thread. The configured transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is configured to receive is controlled by the below equation. If the configured excess information rate is zero, then only the committed information rate is transferred:

Priority Transfer rate [Mbit/s] = ((((Frequency in MHZ) * CPSW_P0_PRI_CIR_REG_y) / 32768) + (((Frequency in MHZ) * CPSW_P0_PRI_EIR_REG_y) / 32768))

Where the *frequency* is the CPPI_ICLK frequency (in MHz) and priority 0 to 7.

For example, 10Mbps on priority 7 would give the below:

10Mbps = ~ ((350 * 936) / 32768), at 350Mhz and CPSW_P0_PRI_CIR_REG_y[27-0] PRI_CIR value = 936 (no excess information rate)

12.2.1.4.6.6.2 Ethernet Port Transmit Rate Limiting

Ethernet port transmit operations can be configured to rate limit egress data for each egress priority. There is a committed information rate (CPSW_P0_PRI_CIR_REG_y, where y = 0 to 7) and an excess information rate for each priority (CPSW_P0_PRI_EIR_REG_y, where y = 0 to 7). Rate limiting is enabled for a priority when the committed information rate for the priority is non-zero. The excess information rate for a priority is enabled when the excess information rate for the priority is non-zero. The committed information rate must be non-zero if the excess information rate is configured to be non-zero. That is, there must be a configured non-zero committed information rate for there to be a configured non-zero excess information rate. Bulk traffic on other non-rate limited priorities does not impact the committed information traffic on a priority. However, bulk traffic on other non-rate limited threads does impact the excess information rates. Rate limited channels must be the highest priority channels. For example, if two rate limited channels are required then priorities 7 and 6 should be configured for committed information (and excess information if desired). The configured transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is configured to send is controlled by the below equation. If the excess information rate is disabled then the committed information rate only is transferred:

Priority Transfer rate [Mbit/s] = ((((Frequency in MHZ) * CPSW_P0_PRI_CIR_REG_y) / 32768) + (((Frequency in MHZ) * CPSW_P0_PRI_EIR_REG_y) / 32768))

Where the *frequency* is the CPPI_ICLK frequency (in MHz) and priority 0 to 7.

12.2.1.4.6.7 Interspersed Express Traffic (IET – P802.3br/D2.0)

When IET is enabled through CPSW3_CONTROL_REG[17] IET_ENABLE = 1h and configured, IET allows premptable traffic on selected transmit priorities to be prempted by express traffic on selected express priorities. Received traffic is separated onto express and prempt receive queues. When IET is disabled (IET_ENABLE = 0h), all Ethernet traffic is express traffic and switch operation is as if IET does not exist. Traffic is only intended to be moved to the prempt queue after premption is verified and enabled.

12.2.1.4.6.7.1 IET Configuration

1. Using the prempt receive queue requires more blocks to be allocate to the ports receive FIFO. Write a value of decimal 7 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG[7-0] RX_MAX_BLKS bit field, and a value of decimal 13 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG[15-8] TX_MAX_BLKS register for every port to be enabled for IET.
2. Write the [23-0]MAC_VERIFY_CNT bit field in the Ethernet port CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG register to set the verify/response timeout count. The default is 10ms for Gigabit mode. For other time values or link speeds the verify count should be updated. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG[2] MAC_DISABLEVERIFY bit is to be set (this is forced mode) then this step is unneeded.
3. The receive FIFO block allocation is insufficient if CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j [31-0] COUNT is nonzero, indicating that receive packets are being dropped due to FIFO block allocation.
4. Write the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG register in the Ethernet port as below:
   - Set the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG[16] IET_PORT_EN bit. The port will not actually be enabled until bit IET_ENABLE is set in the CPSW3_CONTROL_REG.
   - The CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG[0] MAC_PENABLE bit can be set as desired. No effect will occur until IET_ENABLE is set. This bit enables premptable packets to be prempted by express traffic but does not preclude packets from being sent to the prempt queue.

  - If verify/response is desired then CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG[3] MAC_LINKFAIL should be cleared by software to enable verify and response packets. Otherwise, MAC_DISABLEVERIFY bit should be set for forced mode. Verification and response will occur immediately after clearing this bit.
  - Configure the remaining CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG register bits as desired.
5. Set the IET_ENABLE bit in the CPSW3_CONTROL_REG register to enable IET operations.
6. After preemption has been verified, the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG[23-16] MAC_PREMPT field is written to configure the FIFO priorities to be sent to the prempt queue (the other priorities with cleared bits go to the express queue). The hardware switch for each queue from express to prempt happens only when there are no packets queued on the priority.

12.2.1.4.6.8 Enhanced Scheduled Traffic (EST – P802.1Qbv/D2.2)

12.2.1.4.6.8.1 Enhanced Scheduled Traffic Overview

- When enabled and configured, EST allows express queue traffic to be scheduled (placed) on the wire at specific repeatable time intervals.
- EST operates on a repeating time interval generated by the CPTS EST function generator. For example, a 125us repeating time interval can be configured.
- Each Ethernet port has 128 EST fetch commands maximum in the global EST fetch RAM.
- Each 22-bit fetch command consists of a 14-bit fetch count (14 MSB’s) and an 8-bit priority fetch allow (8 LSB’s) that will be applied for the fetch count time in wireside clocks.
- The configured port fetch commands are executed in sequence, beginning at port address zero each time through the time interval beginning at cycle start.
- EST allows non-scheduled express and prempt queue traffic to be cleared from the wire to ensure that the scheduled traffic is transmitted at the proper time (zero allow).
- EST can be used with or without premption. The CPSW_PN_IET_CONTROL_REG[23-16] MAC_PREMPT value determines whether the priority is enabled on the express or prempt queue. Whether a priority is on the express or prempt queue only effects the wire clear time from an EST operation perspective.
- Software should not move priorities to the prempt queue unless preemption is configured, enabled, and verified allowing preemption to occur.
- Express packet time stamp events can be enabled to assist software in configuring and timing EST operations.

12.2.1.4.6.8.2 Enhanced Scheduled Traffic Fetch RAM

- The EST fetch RAM is read/writable in the CPSW configuration address space.
- The Ethernet transmit port has 128 locations in the global EST fetch RAM.
  - Ethernet port 1 has EST fetch RAM addresses 0x000-0x07F.
- **One buffer operation:** When CPSW_PN_EST_CONTROL_REG[0] EST_ONEBUF is set to 1h, the 128 port locations operate as one buffer. The EST_BUFACT bit in CPSW_PN_FIFO_STATUS_REG register is the upper address bit of the port’s fetch RAM address indicating whether operation is currently in the upper or lower 64 locations of the port’s fetch RAM.
- **Two buffer operation:** When CPSW_PN_EST_CONTROL_REG[0] EST_ONEBUF is cleared there are two 64-location buffers with CPSW_PN_EST_CONTROL_REG[1] EST_BUFSEL selecting the buffer to be used. When the buffer is switched by changing the CPSW_PN_EST_CONTROL_REG[1] EST_BUFSEL value, the actual switch occurs on cycle start. The actual buffer being used is indicated by the EST_BUFACT bit in CPSW_PN_FIFO_STATUS_REG. Software should avoid writing the switched out buffer fetch RAM locations until it detects that the actual switch has occurred.
- The first address location in the port’s fetch RAM space (location zero) is read at the beginning of each EST time interval (cycle start). Addresses are then read in ascending order for the duration of the interval. The port address zero is then read again at the beginning of the next cycle repeating the time interval packet operations.

12.2.1.4.6.8.3 Enhanced Scheduled Traffic Time Interval

- Each Ethernet port has an Enhanced Scheduled Traffic Function (ESTF) generator in the CPTS submodule.
- The EST function generator generates the EST time interval as a configured number of CPTS reference clocks (CPTS_RFT_CLK).
- The EST function generator rising edge is the cycle start time and the cycle repeats (cycle start occurs) after every time interval.
- The first fetch allowed value is at the port base address zero in the EST fetch RAM and is actually applied 16 wireside clocks after cycle start. The 16 clock cycle delay allows the first fetch value time to be fetched from the EST fetch RAM (prefetch time at cycle start).
- Each successive fetch allow is applied for the associated fetch count thereafter. The minimum non-zero fetch count is 16. The minimum value of 16 guarantees that the next fetch value has time to be fetched before the current fetch count is over. There are 64 maximum fetch values when CPSW_PN_EST_CONTROL_REG[0] EST_ONEBUF = 0h, and 128 maximum fetch values when CPSW_PN_EST_CONTROL_REG[0] EST_ONEBUF = 1h.
- The next cycle start then causes the fetch to once again start at the port address zero.

12.2.1.4.6.8.4 Enhanced Scheduled Traffic Fetch Values

- The 22-bit fetch value is made up of the 14-bit fetch count and the 8-bit fetch allow.
- The fetch time indicates the number of wireside clocks that the fetch allow will be active.
- The fetch count is in Ethernet wireside clocks which is bytes in Gigabit mode (CPSW_PN_MAC_CONTROL_REG[7] GIG = 1h) and nibbles in 10/100Mbps mode.
- When a fetch allow bit is set, the corresponding priority is enabled to begin packet transmission on an allowed priority subject to rate limiting. The actual packet transmission on the wire may carry over into the next fetch count and is the reason for the wire clear time in the fetch zero allow.
- When a fetch allow bit is cleared, the corresponding priority is not enabled to transmit for the fetch count time.
- A non-zero fetch allow value with a non-zero fetch count causes the fetch allow value to be applied for the fetch count number of wireside clocks.
- A zero fetch count causes the associated fetch allow to be held for the duration of the cycle (until the next cycle start).
- A zero fetch allow with a non-zero fetch count is intended to clear the wire for a scheduled (timed) express packet in the next fetch. A zero fetch allow indicates that no packet can be started for transmission for the associated fetch count. The associated fetch count must be sufficient to guarantee that the wire is cleared given that a packet on an allowed priority in the previous fetch could have been started on the previous clock and that there is hardware latency in the clear time. The timed packet should be sent on a priority that is enabled in the next fetch but disabled in the current zero allow fetch. The fetch allow previous to a zero allow should have only prempt priorities enabled or only express priorities enabled but not both.
- The number of clocks required to clear the wire varies depending Ethernet wire speed and on whether express or prempt priorities were allowed in the previous fetch command.

12.2.1.4.6.8.5 Enhanced Scheduled Traffic Packet Fill

Packet fill can be enabled (CPSW_PN_EST_CONTROL_REG[8] EST_FILL_EN = 1h) to occur in the fetch count time associated with a fetched zero allow. The intention with fill is that a smaller packet on a non-timed priority might be able to be inserted on the wire during the wire clear time which would increase wire utilization. Fill is intended to be used with either only express priorities in the previous non-zero fetched allow, or only prempt priorities in the previous non-zero fetched allow but not both. Fill must be configured to ensure that any fill packet does not conflict with the timed express packet allowed in the next fetch.

- **Express fill:**
  1. CPSW_PN_EST_CONTROL_REG[8] EST_FILL_EN is set and
  2. A fetch contains a non-zero fetch count with a zero fetch allow, and
  3. The previous allow contained only express priorities.

  4. The fetch count loaded should be at least TBD clocks and the CPSW_PN_EST_CONTROL_REG[25-16] EST_FILL_MARGIN should be at least TBD clocks in Gigabit mode to ensure that the wire is cleared for the timed express packet allowed in the next fetch.
  5. The fetch count loaded should be at least TBD clocks and the CPSW_PN_EST_CONTROL_REG[25-16] EST_FILL_MARGIN should be at least TBD clocks in 10/100Mbps mode to ensure that the wire is cleared for the timed express packet allowed in the next fetch.

- **Prempt fill:**
  1. CPSW_PN_EST_CONTROL_REG[8] EST_FILL_EN is set and
  2. A fetch contains a non-zero fetch count with a zero fetch allow, and
  3. The previous allow contained only prempt priorities
  4. The fetch count loaded should be at least TBD clocks in Gigabit mode to ensure that the wire is cleared for the timed express packet allowed in the next fetch.
  5. The fetch count loaded should be at least TBD clocks in 10/100Mbps mode to ensure that the wire is cleared for the timed express packet allowed in the next fetch.

- **Express non-fill:**
  1. CPSW_PN_EST_CONTROL_REG[8] EST_FILL_EN is clear and
  2. The previous allow contained only express priorities.
  3. The fetch count loaded should be at least TBD clocks in Gigabit mode to ensure that the wire is cleared for the timed express packet allowed in the next fetch.
  4. The fetch count loaded should be at least TBD clocks in 10/100Mbps mode to ensure that the wire is cleared for the timed express packet allowed in the next fetch.

- **Prempt non-fill:**
  1. CPSW_PN_EST_CONTROL_REG[8] EST_FILL_EN is clear and
  2. The previous allow contained only prempt priorities.
  3. The fetch count loaded should be at least TBD clocks in Gigabit mode to ensure that the wire is cleared for the timed express packet allowed in the next fetch.
  4. The fetch count loaded should be at least TBD clocks in 10/100Mbps mode to ensure that the wire is cleared for the timed express packet allowed in the next fetch.

12.2.1.4.6.8.6 Enhanced Scheduled Traffic Time Stamp

The EST can be configured to generate CPTS timestamp events for selected express traffic. The EST timestamp events use the CPTS host event type (CPSW_CPTS_EVENT_1_REG[23-20] EVENT_TYPE = 7 decimal. The EST timestamps will not override host sent timestamps for packets that were sent from the host with an enabled host timestamp.

- EST Events (host events) contain the below information:
  - Time Stamp of the selected express packet.
  - The event CPSW_CPTS_EVENT_1_REG[28-24] PORT_NUMBER indicates the transmit port number.
  - The event CPSW_CPTS_EVENT_1_REG[23-20] EVENT_TYPE is decimal 7 (host event).
  - The event CPSW_CPTS_EVENT_1_REG[23-20] MESSAGE_TYPE indicates the packet transmit hardware switch priority.
  - The event CPSW_CPTS_EVENT_1_REG[15-0] SEQUENCE_ID upper nibble indicates the packet receive port number.
  - The event CPSW_CPTS_EVENT_1_REG[15-0] SEQUENCE_ID lower byte indicates the sequence number of the express packet in numerical order. The first event is event one, the second is event two and so on. The sequence ID rolls over to zero after 0xFF (8-bits).
  - The event domain is the value from the CPSW_EST_TS_DOMAIN_REG[7-0] EST_TS_DOMAIN register.
- When CPSW_PN_EST_CONTROL_REG[2] EST_TS_EN is set, timestamp events will be generated on selected express traffic.
- When CPSW_PN_EST_CONTROL_REG[3] EST_TS_FIRST is also set, events will be generated only on the first express packet in each time interval. If CPSW_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is

also set then the event will only be on the first CPSW_PN_EST_CONTROL_REG[7-5] EST_TS_PRI express packet in the time interval. If CPSW_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is clear then the event will be generated on the first express packet in the time interval on any priority.

- When CPSW_PN_EST_CONTROL_REG[3] EST_TS_FIRST is clear, events will be generated on every express packet. If CPSW_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is set then the event will be generated on every CPSW_PN_EST_CONTROL_REG[7-5] EST_TS_PRI express packet. If CPSW_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is clear then event will be generated on every express packet on any priority.

12.2.1.4.6.8.7 Enhanced Scheduled Traffic Packets Per Priority

The number of packets allowed in a transmit FIFO priority can be selected by writing a non-zero value to CPSW_P0_RX_PKTS_PRI_REG register (packet priority 0 to 7). Then port 0 receive gap should then be enabled by setting the corresponding priority through CPSW_P0_RX_GAP_REG[7-0] RX_GAP_EN bit field. The receive gap allows a packet to land in the transmit FIFO before another packet is allowed in which guarantees that only the selected number (max) of packets is allowed in on the specified priority. If the receive gap is not enabled, then there might be one or two more packets allowed in on the priority/thread than the packets per priority value has selected (through CPSW_P0_RX_PKTS_PRI_REG register).

12.2.1.4.6.9 Audio Video Bridging

Audio Video Bridging is an ongoing project of IEEE 802.1 concerned with enabling low-latency streaming of time-sensitive audiovisual data over networks. Devices are designated as talkers (transmitters), bridges, or listeners (receivers). It is suggested that the maximum latency could be 2 ms over 7 hops for Class A devices and 20 ms over 7 hops for Class B devices. A hop is essentially a single local area network stage in the journey of a packet. Every time a bridge is encountered between one network section and another a hop is involved. One of the performance goals is that AVB streams will not use more than 75 percent of a link's bandwidth, leaving the remaining capacity for non-AVB streams.

The goal of developing AVB is simply--extend Ethernet's data-networking capabilities to the realm of reliable real-time audio/video networking.

An "Audio Video Bridging" network is one that implements a set of protocols being developed by the IEEE 802.1 Audio/Video Bridging Task Group. There are four primary differences between the proposed Audio Video Bridging architecture and existing 802 architectures (from now on the term "AVB" will be used instead of "Audio Video Bridging"):

1. Precise synchronization - IEEE 802.1AS: "*Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks.* "a.k.a Precision Time Protocol (PTP).
2. Traffic shaping for media streams - IEEE 802.1Qav: "*Virtual Bridged Local Area Networks:* Forwarding and Queuing for Time-Sensitive Streams."
3. Admission controls - IEEE 802.1Qat: "*Virtual Bridged Local Area Networks - Amendment 9:* Stream Reservation Protocol (SRP)."
4. Identification of non-participating devices - IEEE 802.1BA: "Audio/Video Bridging (AVB) Systems"

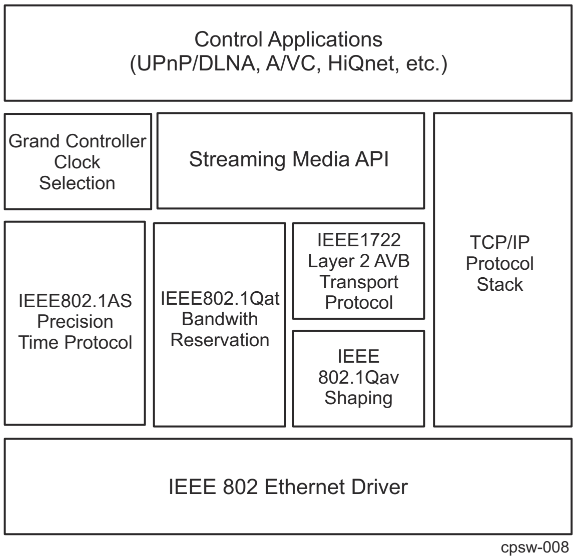

Figure 12-115. The Network Static with AVB

The following sections describe the media transport protocols that work within the AVB framework.

12.2.1.4.6.9.1 IEEE 802.1AS: Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks (Precision Time Protocol (PTP))

The protocol defined by 802.1AS automatically selects a device to be the controller clock, and then distributes this clock throughout the bridged LAN / IP subnet to all other network devices using link-specific transmit/receive time-stamping. However, we only use a two-step solution only on transmit. That is, we do not modify a packet with the timestamp on the way out. The timestamp packet is sent out and then a separate message with the timestamp is sent by the host afterward. Receive can be one or two step.

Note

The 802.1AS-distributed clock is not used as a media clock. Rather, the shared 802.1AS clock reference is used to regenerate the media clock at the listener/renderer. Such a reference removes the need to force the latency of the network to be constant, or compute long running averages in order to estimate the actual media rate of the transmitter in the presence of substantial network jitter. IEEE 802.1AS is based on the ratified IEEE 1588 standard.

Based on IEEE 1588:2002,A PTP devices exchange standard Ethernet messages that synchronize network nodes to a common time reference by defining clock controller selection and negotiation algorithms, link delay measurement and compensation, and clock rate matching and adjustment mechanisms.

Designed as a simplified profile of IEEE 1588, a primary difference between 1588 and IEEE 802.1AS is that PTP is a layer 2-in other words, a non-IP routable protocol. Like IEEE 1588, PTP defines an automatic method for negotiating the network clock controller, the Best Controller Clock Algorithm (BCCA). PTP nodes can be assigned one of eight priority levels, presumably based on clock quality. BMCA defines the underlying negotiation and signaling mechanism whose purpose is to identify the AVB LAN Grandcontroller. Once a Grandcontroller has been selected, synchronization automatically begins.

At the core of 802.1AS synchronization is time-stamping. In short, during PTP message ingress/egress from the 802.1AS-capable MAC, the PTP Ether type triggers the sampling of the value of a local real-time counter (RTC). Target nodes compare the value of their RTC against the PTP Grandcontroller and, by use of link delay measurement and compensation techniques, match their RTC value to the time of the AVB LAN PTP domain. After network time throughout the AVB LAN has converged, periodic SYNC and FOLLOW_UP messages provide the information that enables the PTP rate matching adjustment algorithms. The result is all PTP nodes are then synchronized to the same "Wall Clock" time. PTP assures 1-µs accuracy over seven network hops.

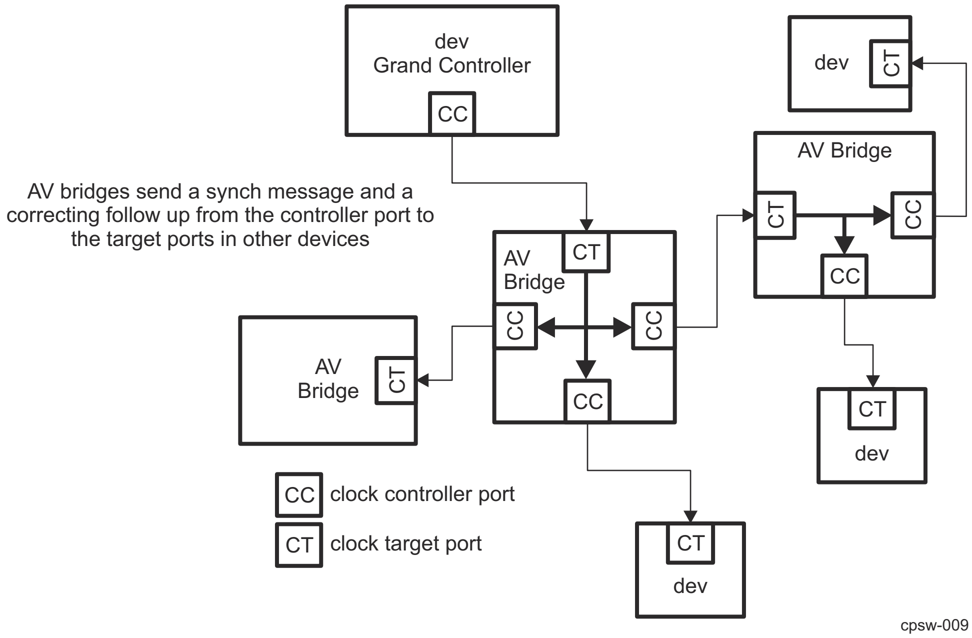

Figure 12-116. AVB Network & PTP Clock Entities

The media transport protocols that work within the AVB framework are:

12.2.1.4.6.9.1.1 IEEE 1722: "Layer 2 Transport Protocol for Time-Sensitive Streams"

AVBTP or 1722 sits above the IEEE 802.1 AVB plumbing and below the application layer. It acts as the conduit between an Ethernet MAC and a streaming application. AVBTP abstracts the underlying network transmission channel to enable the virtual connection of distributed audio and video CODECs over reliable Ethernet networks. A complete AVBTP Ethernet packet is shown in Figure 12-117 and illustrates how IEC 61883-6 AM824 uncompressed audio samples are encapsulated in an Ethernet frame.

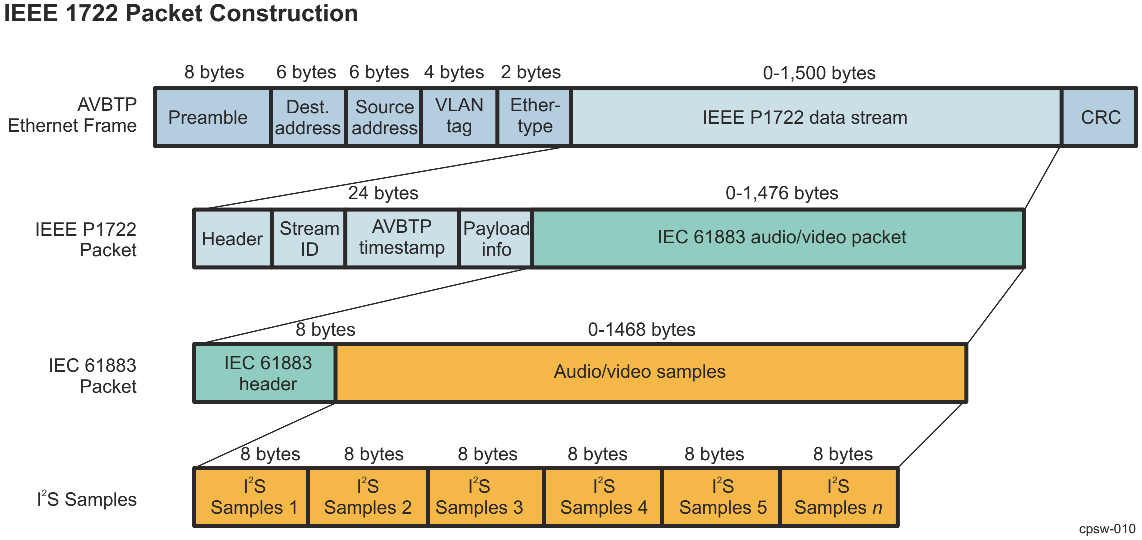

Figure 12-117. IEEE 1722 Packets

1722 or AVBTP Presentation Time and Synchronization:

Synchronization in an AVB network starts with the Precision Time Protocol but ends with synchronized media clocks. PTP is responsible for synchronizing all nodes in an AVB network to identical wall clock time; not for synchronizing media clocks. In other words, PTP does not actually transport synchronized media clocks but instead provides a low-level building block crucial for managing a distributed media synchronization system.

A crucial benefit of this approach is coexistence of multiple, independent media clock domains on an AVB network. Unrelated audio and video streams can simultaneously exist in the same LAN.

12.2.1.4.6.9.1.1.1 Cross-timestamping and Presentation Timestamps

AVBTP assumes that AVB node media clocks are clocked by free-running oscillators. It is also assumed that the node's internal concept of wall clock time has been synchronized to the PTP Grandcontroller. AVBTP media clock sources embed "AVBTP Presentation Timestamps" in AVBTP streaming packets. Figure 12-118 illustrates the relationship between PTP network time and AVBTP Presentation Timestamps.

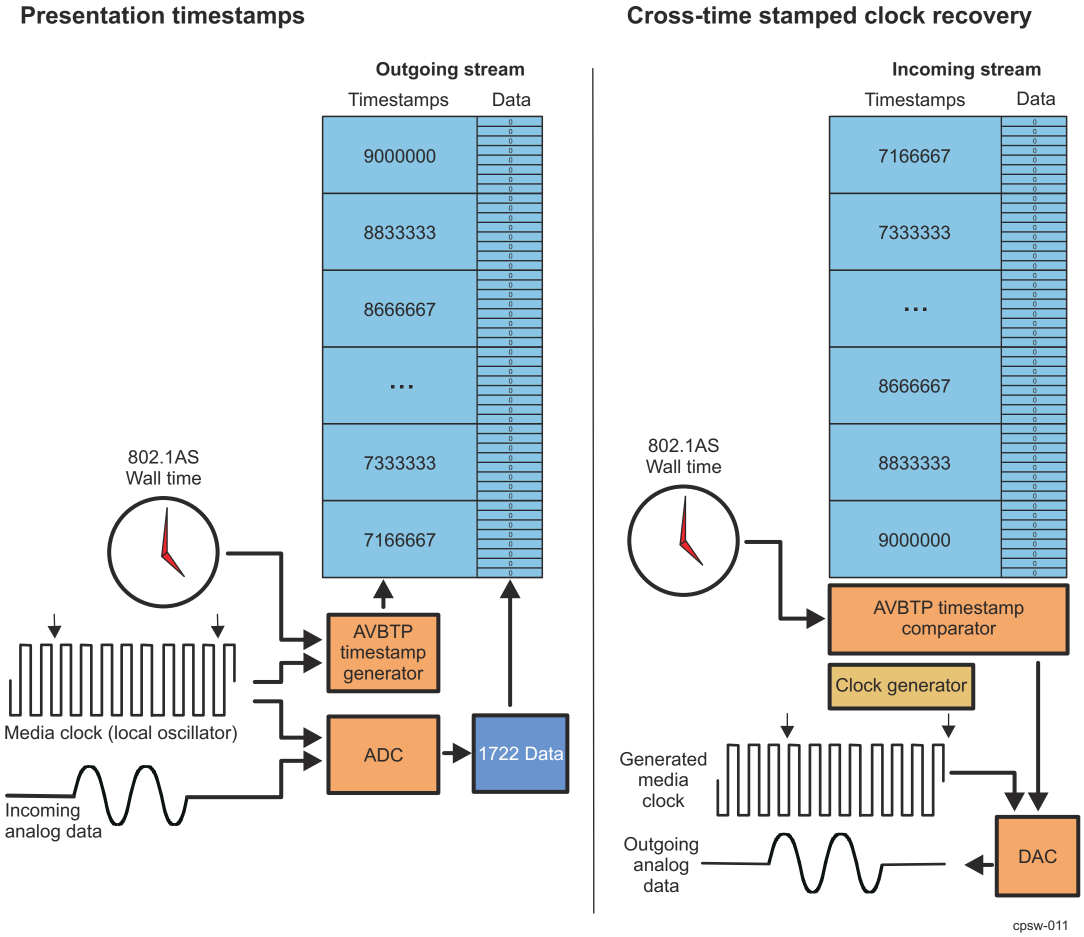

Figure 12-118. Cross Time Stamping and Presentation Timestamps

12.2.1.4.6.9.1.2 IEEE 1733: Extends RTCP for RTP Streaming over AVB-supported Networks

This standard specifies the protocol, data encapsulations, connection management and presentation time procedures used to ensure interoperability between audio and video based end stations that use standard networking services provided by all IEEE 802 networks meeting QoS requirements for time-sensitive applications by leveraging the Real-time Transport Protocol (RTP) family of protocols and IEEE 802.1 Audio/ Video Bridging (AVB) protocols.

12.2.1.4.6.9.2 IEEE 802.1Qav: "Virtual Bridged Local Area Networks: Forwarding and Queuing for Time-Sensitive Streams"

This standard allows bridges to provide guarantees for time-sensitive (that is, bounded latency and delivery variation), loss-sensitive real-time audio video (AV) data transmission (AV traffic). It specifies per priority ingress metering, priority regeneration, and timing-aware queue draining algorithms. This standard uses the timing derived from IEEE 802.1AS. Virtual Local Area Network (VLAN) tag encoded priority values are allocated, in aggregate, to segregate frames among controlled and non-controlled queues, allowing simultaneous support of both AV traffic and other bridged traffic over and between wired and wireless Local Area Networks (LANs).

Such a guarantee in bandwidth is provided by two functional entities:

- A registration protocol, which registers the service and its maximum network utilization with a device or switch (IEEE 802.1Qat: "Virtual Bridged Local Area Networks - Amendment 9: Stream Reservation Protocol (SRP)")
- A hardware bandwidth management service.
  - Receive policing
  - Transmit rate control.

End Station Behavior

In order for an end station to successfully participate in the transmission and reception of time-sensitive streams, it is necessary for their behavior to be compatible with the operation of the forwarding and queuing mechanisms employed in bridges.

The requirements for end stations that participate as "talkers" i.e., sources of time-sensitive streams are different from the requirements that apply to "listeners", the destination station(s) for the streams.

Talker Behavior

In order for Talker-originated data streams to make use of the credit-based shaper behavior in Bridges, it is a requirement for a Talker to use the priorities that the Bridges in the network recognize as being associated with SR classes exclusively for transmitting stream data.

It is also necessary for the Talker and the Bridges in the path to the Listener(s), to have a common view of the bandwidth required in order to transmit the Talker's streams, and for that bandwidth to be reserved along the path to the Listener(s). This latter requirement can be met by means of stream reservation mechanisms, such as defined in SRP, or by other management means.

End stations that are Talkers shall exhibit transmission behavior for frames that are part of "time-sensitive streams" that is consistent with the operation of the credit-based shaper algorithm, both in terms of the way they transmit frames that are part of an individual data stream, and in terms of the way they transmit stream data frames from a Port.

In effect, the queuing model for a Talker Port (and a Listener port), and for given priorities, can be considered to look like Figure 12-119.

Listener Behavior

The primary requirement for a listener station is that it is capable of buffering the amount of data that could be transmitted for a stream during a time period equivalent to the accumulated maximum jitter that could be experienced by stream data frames in transmission between Talker and Listener.

From the point of view of the specification of the forwarding and queuing requirements for time-sensitive streams, it is assumed that the listener will assess the buffering required for a stream as part of the stream bandwidth reservation mechanisms employed by the implementation.

The credit-based shaper's operation details are beyond the scope of this document.

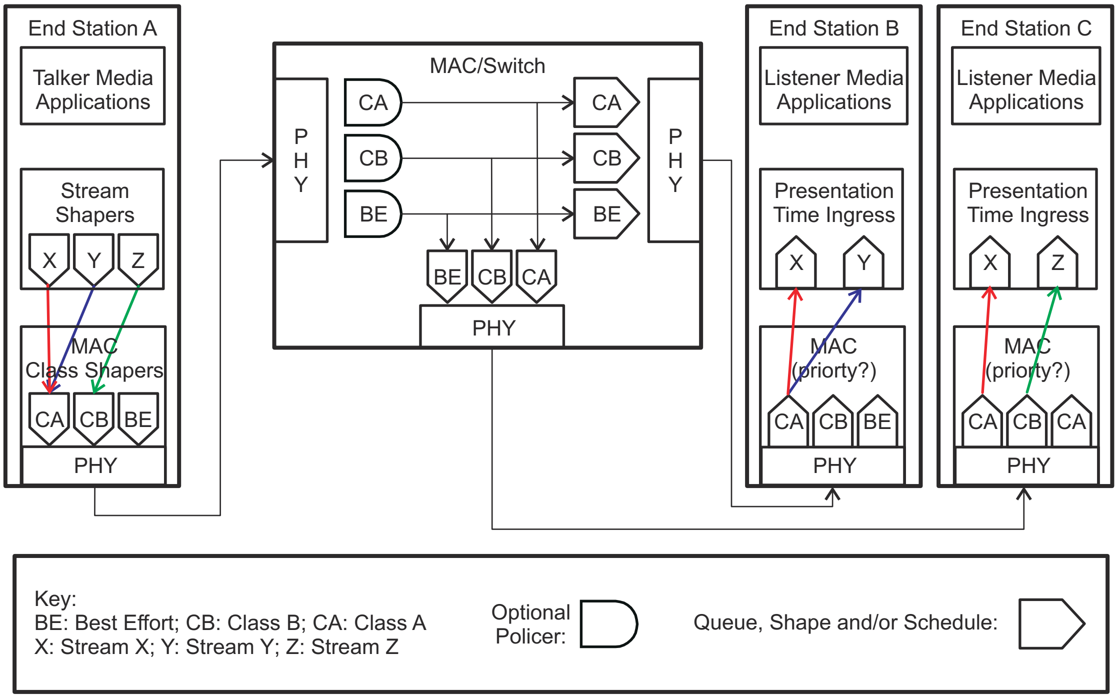

Figure 12-119. AV Stream Queuing/Policing

12.2.1.4.6.9.2.1 Configuring the Device for 802.1Qav Operation

There is no dedicated register-set to be configured for the time-sensitive stream handling. The list of functional features of CPSW that will have to be configured are:

- DESCRIPTORS and CHANNEL CONFIGURATIONS:
  - CPPI TX and RX descriptors
  - VLAN and Priority tags

Table 12-171. Example of TX Configuration

TX DMA CHANNEL	Packet Priority	Switch Queue Priority
7	7	3
6	5	2
5	3	1
4	1	0

Table 12-172. Example of RX Configuration

RX DMA CHANNEL	Packet Priority	Switch Queue Priority
0	7	0
0	5	0
0	3	0
0	1	0

- ALE Configuration:
  - ALE in VLAN-ware mode, Non-ALE in bypass mode.

12.2.1.4.6.10 Ethernet MAC Sliver

The Ethernet port peripheral is compliant to the IEEE Std 802.3 Specification. Half-duplex mode is supported in 10/100 Mbps mode, but not in 1000 Mbps (gigabit) mode.

Features:

- Synchronous 10/100/1000 Mbit operation
- RMII/RGMII Interface
- Hardware Error handling including CRC
- Full-Duplex Gigabit operation (half-duplex gigabit is not supported)
- EtherStats and 802.3Stats RMON statistics gathering support for external statistics collection module
- Transmit CRC generation selectable on a per channel basis
- Emulation Support
- VLAN Aware Mode Support
- Hardware flow control
- Programmable Inter Packet Gap (IPG).

12.2.1.4.6.10.1 Ethernet MAC Sliver Overview

12.2.1.4.6.10.1.1 CRC Insertion

The MAC generates and appends a 32-bit Ethernet CRC onto the transmitted data, if the transmit packet header PASS_CRC bit is 0h. For the Ethernet port generated CRC case, a CRC at the end of the input packet data is not allowed.

If the header word PASS_CRC bit is set, then the last four bytes of the TX data are transmitted as the frame CRC. The four CRC data bytes should be the last four bytes of the frame and should be included in the packet byte count value. The MAC performs no error checking on the outgoing CRC when the PASS_CRC bit is set.

12.2.1.4.6.10.1.2 MTXER

The MTXER signal is only used for EEE. If an underflow condition occurs on a transmitted frame, the frame CRC will be inverted to indicate the error to the network. Underflow is a hardware error.

12.2.1.4.6.10.1.3 Adaptive Performance Optimization (APO)

The Ethernet MAC port incorporates Adaptive Performance Optimization (APO) logic that may be enabled by setting the TX_PACE bit in the CPSW_PN_MAC_CONTROL_REG register. Transmission pacing to enhance performance is enabled when set. Adaptive performance pacing introduces delays into the normal transmission of frames, delaying transmission attempts between stations, reducing the probability of collisions occurring during heavy traffic (as indicated by frame deferrals and collisions) thereby increasing the chance of successful transmission.

When a frame is deferred, suffers a single collision, multiple collisions or excessive collisions, the pacing counter is loaded with an initial value of 31. When a frame is transmitted successfully (without experiencing a deferral, single collision, multiple collision or excessive collision) the pacing counter is decremented by one, down to zero.

With pacing enabled, a new frame is permitted to immediately (after one IPG) attempt transmission only if the pacing counter is zero. If the pacing counter is non zero, the frame is delayed by the pacing delay, a delay of approximately four inter-packet gap delays. APO only affects the IPG preceding the first attempt at transmitting a frame. It does not affect the back-off algorithm for re-transmitted frames.

12.2.1.4.6.10.1.4 Inter-Packet-Gap Enforcement

The measurement reference for the IPG of 96-bit times is changed depending on frame traffic conditions. If a frame is successfully transmitted without collision, and MCRS is de-asserted within approximately 48-bit times of MTXEN being de-asserted, then 96-bit times is measured from MTXEN. If the frame suffered a collision, or if MCRS is not de-asserted until more than approximately 48-bit times after MTXEN is de-asserted, then 96-bit times (approximately, but not less) is measured from MCRS.

The Ethernet port transmit inter-packet gap (IPG) may be shortened by eight bit times when short gap is enabled and triggered. Setting the [10] TX_SHORT_GAP_ENABLE bit in the CPSW_PN_MAC_CONTROL_REG register enables the gap to be shortened when triggered. The condition is triggered when the ports associated transmit packet FIFO has a user defined number of FIFO blocks used. The associated transmit FIFO blocks used value determines if the gap is shortened, and so on. The CPSW_GAP_THRESH_REG register value determines the short gap threshold. If the FIFO blocks used is greater than or equal to the GAP_THRESH value then short gap is triggered.

12.2.1.4.6.10.1.5 Back Off

The Gigabit Ethernet Mac Sliver implements the 802.3 binary exponential back-off algorithm.

12.2.1.4.6.10.1.6 Programmable Transmit Inter-Packet Gap

The transmit inter-packet gap (IPG) is programmable through the CPSW_PN_MAC_CONTROL_REG register. The default value is decimal 12. The transmit IPG may be increased to the maximum value of 1FFh. Increasing the IPG is not compatible with transmit pacing. The short gap feature will override the increased gap value, so the short gap feature may not be compatible with an increased IPG.

12.2.1.4.6.10.1.7 Speed, Duplex and Pause Frame Support Negotiation

The Ethernet port can operate in half duplex or full duplex in 10/100 Mbit modes, and can operate in full duplex only in 1000 Mbit mode. Pause frame support is included in 10/100/1000 Mbit modes as configured by the host.

12.2.1.4.6.10.2 RMII Interface

The CPRMII peripheral is compliant to the RMII specification document.

12.2.1.4.6.10.2.1 Features

- Source Synchronous 10/100 Mbit operation
- Full and Half Duplex support

12.2.1.4.6.10.2.2 RMII Receive (RX)

The CPRMII receive (RX) interface converts the input data from the external RMII PHY (or switch) into the required MII (CPGMAC) signals. The carrier sense and collision signals are determined from the RMII input data stream and transmit inputs as defined in the RMII specification.

An asserted RMII_RXER on any di-bit in the received packet will cause an MII_RXER assertion to the CPGMAC during the packet. In 10Mbps mode, the error is not required to be duplicated on 10 successive clocks. Any di-bit which has an asserted RMII_RXER during any of the 10 replications of the data will cause the error to be propagated.

Any received packet that ends with an improper nibble boundary aligned RMII_CRS_DV toggle will issue an MII_RXER during the packet to the CPGMAC. Also, a change in speed or duplex mode during packet operations will cause packet corruption.

The CPRMII can accept receive packets with shortened preambles, but 0x55 followed by a 0x5D is the shortest preamble that will be recognized (1 preamble byte with the start of frame byte). At least one byte of preamble with the start of frame indicator is required to begin a packet. An asserted RMII_CRS_DV without at least a single correct preamble byte followed by the start of frame indicator will be ignored.

12.2.1.4.6.10.2.3 RMII Transmit (TX)

The CPRMII transmit (TX) interface converts the CPGMAC MII input data into the RMII transmit format. The data is then output to the external RMII PHY.

The CPGMAC does not source the transmit error (MII_TXERR) signal. Any transmit frame from the CPGMAC with an error (underrun) will be indicated as an error by an error CRC. Transmit error is assumed to be de-asserted at all times and is not an input into the CPRMII module. Zeroes are output on RMII_TXD[1:0] for each clock that RMII_TXEN is de-asserted.

12.2.1.4.6.10.3 RGMII Interface

The CPRGMII peripheral is compliant to the RGMII specification document.

12.2.1.4.6.10.3.1 Features

- Supports 1000/100/10 Mbps speed
- Full and Half Duplex support (CPGMAC supports only Full duplex in Gigabit mode).

- MII mode support
- Energy Efficient Ethernet Support

12.2.1.4.6.10.3.2 RGMII Receive (RX)

The CPRGMII receive (RX) interface converts the source synchronous DDR input data from the external RGMII PHY into the required G/MII (CPGMAC) signals.

12.2.1.4.6.10.3.3 In-Band Mode of Operation

The CPRGMII is operating in the in-band mode of operation when the RGMII_RX_INBAND input is asserted. RGMII_RX_INPUT is asserted by configuring the EXT_EN bit to 1h of the CPSW_PN_MAC_CONTROL_REG register. The link status, duplexity, and speed are determined from the RGMII input data stream RXD[3:0] when RX_CTL is deasserted, as defined in the RGMII specification. The PHY might need to be configured beforehand to output in-band data. The in-band data is indicated as shown in Table 12-173.

Table 12-173. In-Band Data

RXD3	RXD[2:1]		RXD0
Duplex status:	Link Speed:	RXC_CLK Speed:	Link Status:
0h: half-duplex	0h: 10-Mbps mode	2.5 MHz	0h: Link is down
1h: full-duplex	1h: 100-Mbps mode	25 MHz	1h: Link is up
	2h: 1000-Mbps mode	125 MHz	
	3h: Reserved	Reserved	

12.2.1.4.6.10.3.4 Forced Mode of Operation

The CPRGMII is operating in the forced mode of operation when the RGMII_RX_INBAND input is deasserted by setting to 0h bit EXT_EN of the CPSW_PN_MAC_CONTROL_REG register. In the forced mode of operation, the in-band data is ignored if present. The link status is forced high, and the duplexity and speed are determined from the CPSW_PN_MAC_CONTROL_REG[0] FULLDUPLEX and CPSW_PN_MAC_CONTROL_REG[7] GIG bits. If bit [7] GIG = 1h, then CPRGMII is operating in Gigabit mode. If bit [7] GIG is cleared (0h), then CPRGMII is operating in 100 Mbps mode.

12.2.1.4.6.10.3.5 RGMII Transmit (TX)

The CPRGMII transmit (TX) interface converts the CPGMAC G/MII input data into the DDR RGMII format. The DDR data is then output to the external PHY.

The CPGMAC does not source the transmit error (TXERR) signal. Any transmit frame from the CPGMAC with an error (underrun) will be indicated as an error by an error CRC. Transmit error is assumed to be deasserted at all times and is not an input into the CPRGMII module.

In 10/100 Mbps mode, the TXD[7:0] data bus uses only the lower nibble. The CPRGMII will output the lower nibble twice in 10/100 Mbps mode to avoid unnecessary signal switching.

Packets will be precluded from transmission through the CPRGMII module for 4096 transmit clocks after the rising edge of RGMII_LINK. Packet transmission will begin on the first TX_CTL rising edge after the 4096 transmit clock count has expired.

12.2.1.4.6.10.4 Frame Classification

Received frames are proper (good) frames if they are between 64 and CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN in length (inclusive) and contain no errors (code/align/CRC).

Received frames are long frames if their frame count exceeds the value in the CPSW_P0_RX_MAXLEN_REG/CPSW_PN_RX_MAXLEN_REG register. The register reset (default) value is 1518 (decimal). Long received frames are either oversized or jabber frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment errors are jabber frames.

Received frames are short frames if their frame count is less than 64 bytes. Short frames that contain no errors are undersized frames. Short frames with CRC, code, or alignment errors are fragment frames. If RX_CSF_EN bit in CPSW_PN_MAC_CONTROL_REG is set to 1h, undersized frames from 33 to 63 bytes will be forwarded only to the host on a best effort basis (meaning that the ALE may or may not be able to keep up with the packet rate and the short packet may be dropped due to bandwidth limitations). If RX_CSF_EN and RX_CEF_EN in CPSW_PN_MAC_CONTROL_REG are set, fragment frames from 33 to 63 bytes will also be forwarded only to the host on a best effort basis. Ethernet port received frames shorter than 33 bytes are dropped in all cases.

A received long packet will always contain RX_MAXLEN number of bytes transferred to memory (if CPSW_PN_MAC_CONTROL_REG[22]RX_CEF_EN = 1h). An example with RX_MAXLEN = 1518 is:

- If the frame length is 1518, then the packet is not a long packet and there will be 1518 bytes transferred to memory.
- If the frame length is 1519, there will be 1518 bytes transferred to memory. The last three bytes will be the first three CRC bytes.
- If the frame length is 1520, there will be 1518 bytes transferred to memory. The last two bytes will be the first two CRC bytes.
- If the frame length is 1521, there will be 1518 bytes transferred to memory. The last byte will be the first CRC byte.

If the frame length is 1522, there will be 1518 bytes transferred to memory. The last byte will be the last data byte.

12.2.1.4.6.10.5 Receive FIFO Architecture

This section describes the architecture of the Ethernet port's receive FIFOs. Internal to the Gigabit Ethernet switch, all Ethernet ports have an identical associated packet FIFO. Each transmit packet FIFO contains eight logical transmit queues (priority 0 through 7 with 7 the highest priority). Each transmit FIFO memory contains 81,920 bytes total organized as 2560 by 256-bit words. Each FIFO also contains a single memory for the receive queue. Each receive FIFO memory contains a total of 32768 bytes total organized as 1024 by 256-bit words.

12.2.1.4.6.11 Embedded Memories

Table 12-174. Embedded Memories

Memory Type Description	Number of Instances	
Single-port 3072-word × 64 RAM	1	(Combined FIFO RAM)
Single-port 128-word × 28-bit RAM	1	1 (EST)

12.2.1.4.6.12 Memory Error Detection and Correction

The CPSW error detection and correction logic uses the ECC Aggregator Module.

The ECC CPSW_ECC_VECTOR register is used to select which ECC RAM's status and control registers are currently being read or written as shown in Table 12-175. The CPSW FIFO RAMs implement ECC only on packet headers. The packet data is protected by Ethernet CRC. The ALE and EST RAMs have complete ECC as normal.

Table 12-175. ECC RAM to CPSW RAM Mapping

ECC RAM Number	CPSW RAM
0	ALE RAM
1	Port 0 FIFO RAM

12.2.1.4.6.12.1 Packet Header ECC

Only packet headers bits are protected by ECC in the FIFO RAMs. The ECC_ERR_CTRL1[31-0] ECC_ROW bit is used to activate a row address where force single-bit error or force double-bit error needs to be applied. ECC_ERR_CTRL2 [15-0] ECC_BIT1 is implemented to determine which bit of the header is flipped for an SEC error when the ECC_CRC_MODE bit is cleared in the CPSW_CONTROL_REG register. The ECC status registers return the RAM row address where the single or double-bit error has occured (ECC_ERR_STAT2[31-0] ECC_ROW) along with the bit position in the RAM data that is in error (ECC_ERR_STAT1[31-16] ECC_BIT1 value). Forcing double-bit errors in testing can cause indeterminate operation if multiple used packet header bits are flipped given that only single-bit errors are fixed by the ECC logic. Header bits 207 down to 200 are not currently used in the CPSW and may be used to test double bit errors without the possibility of requiring a reset for the switch to recover from the double bit error. No header bits are flipped when ECC_CRC_MODE is set to 1h. Either the RX_ECC_ERR_EN (enable receive ECC error operations) or the TX_ECC_ERR_EN (enable transmit ECC error operations) bits must be set in the CPSW_P0_CONTROL_REG register to test ECC header errors.

The header ECC code is stored in bits 255 down to 208. If any bit is flipped in the ECC code, the flipped bit will be corrected, but the index of the flipped bit will be reported as bit zero. This implies that when the aggregator reports that there is a SEC on bit 0, it can mean two things: either SEC on data bit 0 or SEC somewhere inside the ECC code. Any packet header with ECC error issues a pulse interrupt (ECC_PULSE_INTR) as does an ALE RAM ECC error.

12.2.1.4.6.12.2 Packet Protect CRC

Each packet received without error is passed through the CPSW_3G memories with a generated Ethernet protect CRC. The protect CRC is checked on egress for correctness and removed. If the CRC is correct (no RAM bit errors), then the packet is output with the selected port CRC type. If a protect CRC error is detected on host egress then the TXST_DROP signal will be asserted so that the packet is dropped to the host. If a protect CRC error is detected on Ethernet egress then the egress CRC will be generated on the packet and at least one byte of the CRC will be inverted on output. CRC memory protect errors do not assert the ECC_PULSE_INTR signal. CRC memory protect errors are counted in the associated port statistics registers and issue an interrupt on STAT_PEND_INTR if any CRC memory protect error occurs (and the statistics for that port are enabled). When the ECC_CRC_MODE bit in the CPSW_CONTROL_REG register is set, the ECC_ERR_CTRL2 [15-0] ECC_BIT1 bit field will flip the associated column bit in any FIFO memory read operation, inducing a CRC protect error when the protect CRC is checked. No header bits are flipped when ECC_CRC_MODE is set. Either the RX_ECC_ERR_EN or the TX_ECC_ERR_EN bits must be set in the CPSW_P0_CONTROL_REG register to test packet CRC errors.

12.2.1.4.6.12.3 Aggregator RAM Control

The ECC logic for each FIFO RAM (receive and transmit) is divided into eight separate ECC encoders/decoders that encode/decode 26-bits of data each. Each of the 8 encoders (0 to 7) generates 6-bits of ECC code (48 code bits total), and each of the eight decoders (0 to 7) checks 6-bits of ECC code across the 26-bits of data (208 data bits total). The 48-bits of ECC code are passed through the RAM in the upper 48 unused bits in the header word.

The header data bits and ECC code bits are shown in Table 12-176. The [15-0] ECC_BIT1 value returned on error is a 16-bit value that is the concatenation of 5 bits of zero, 3 bits of the encoder/decoder number (0 to 7), 3 bits of zero, and 5 bits of index into the indicated 26-bit encoder/decoder.

For example, an ECC_BIT1 value of 0x0308 is bit 8 of encoder/decoder 3, which is header bit 86 (that is, (26×3) + 8).

Table 12-176. ECC Submodule Header Data Bit to Encoder/Decoder Mapping

Header Data Bits	Encoder/Decoder
25:0	Encoder/Decoder 0 Data
51:26	Encoder/Decoder 1 Data
77:52	Encoder/Decoder 2 Data
103:78	Encoder/Decoder 3 Data
129:104	Encoder/Decoder 4 Data
155:130	Encoder/Decoder 5 Data
181:156	Encoder/Decoder 6 Data
207:182	Encoder/Decoder 7 Data
213:208	Encoder/Decoder 0 ECC
219:214	Encoder/Decoder 1 ECC
225:220	Encoder/Decoder 2 ECC
231:226	Encoder/Decoder 3 ECC
237:232	Encoder/Decoder 4 ECC
243:238	Encoder/Decoder 5 ECC
249:244	Encoder/Decoder 6 ECC
255:250	Encoder/Decoder 7 ECC

12.2.1.4.6.13 Ethernet Port Flow Control

The Ethernet port have flow control available for transmit and receive. Transmit flow control stops the Ethernet port from transmitting packets to the wire (switch egress) in response to a received pause frame. Transmit flow control does not depend on FIFO usage.

The Ethernet port have flow control available for receive operations (packet ingress). Ethernet port receive flow control is initiated when enabled and triggered. Packets received on an Ethernet port can be sent to the CPPI port. The destination port can trigger the receive Ethernet port flow control. An Ethernet destination port triggers another Ethernet receive flow control when the destination port is full.

When a packet is received on an Ethernet port interface with enabled flow control the below occurs:

- The packet will be sent to all ports that currently have room to take the entire packet.
- The packet will be retried until successful to all ports that indicate they don't have room for the packet.

The flow control trigger to the Ethernet port will be asserted until the packet has been sent, and there is room in the logical receive FIFO for packet runout from another flow control trigger (RX_BLK_CNT = 0h). Ethernet port receive flow control is disabled by default on reset. Ethernet port receive flow control requires that the RX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG be set to 1h. When receive flow control is enabled on a port, the port's associated FIFO block allocation must be adjusted. The port RX allocation must increase from the default three blocks to accommodate the flow control runout. A corresponding decrease in the TX block allocation is required. If a sending port ignores a pause frame then packets may overrun on receive (and be dropped) but will not be dropped on transmit.

12.2.1.4.6.13.1 Ethernet Receive Flow Control

For every Ethernet port to be configured for fullduplex receive flow control, write a value of decimal 7 to the CPSW_PN_MAX_BLKS_REG[7-0] RX_MAX_BLKS bit field, and a value of decimal 13 to the CPSW_PN_MAX_BLKS_REG[15-8] TX_MAX_BLKS register. This re-allocation allows for flow control runout on the receive FIFO at the expense of FIFO memory on the Ethernet transmit side. 10/100Mbps half-duplex collision based receive flow control does not need this re-allocation. Receive flow control is enabled by the RX_FLOW_EN bit in the CPSW_PN_MAC_CONTROL_REG register.

12.2.1.4.6.13.1.1 Collision Based Receive Buffer Flow Control

Collision-based receive buffer flow control provides a means of preventing frame reception when the port is operating in half-duplex mode (FULLDUPLEX is cleared in CPSW_PN_MAC_CONTROL_REG). When receive flow control is enabled and triggered, the port will generate collisions for received frames. The jam sequence transmitted will be the twelve byte sequence C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3 (hex). The jam sequence will begin no later than approximately as the source address starts to be received. Note that these forced collisions will not be limited to a maximum of 16 consecutive collisions, and are independent of the normal back-off algorithm. Receive flow control does not depend on the value of the incoming frame destination address. A collision will be generated for any incoming packet, regardless of the destination address.

12.2.1.4.6.13.1.2 IEEE 802.3X Based Receive Flow Control

IEEE 802.3x based receive flow control provides a means of preventing frame reception when the port is operating in full-duplex mode (FULLDUPLEX bit is set in the CPSW_PN_MAC_CONTROL_REG register). When receive flow control is enabled and triggered, the port will transmit a pause frame to request that the sending station stop transmitting for the period indicated within the transmitted pause frame.

The Ethernet port will transmit a pause frame to the reserved multicast address at the first available opportunity (immediately if currently idle, or following the completion of the frame currently being transmitted). The pause frame will contain the maximum possible value for the pause time (FFFFh). The MAC will count the receive pause frame time (decrements FF00h down to 0) and retransmit an outgoing pause frame if the count reaches zero. When the flow control request is removed, the MAC will transmit a pause frame with a zero pause time to cancel the pause request.

Note that transmitted pause frames are only a request to the other end station to stop transmitting. Frames that are received during the pause interval will be received normally (provided the RX FIFO is not full at which time the receive FIFO will overrun and CPSW_STAT0_RX_BOTTOM_OF_FIFO_DROP/ CPSW_STAT1_RX_BOTTOM_OF_FIFO_DROP[31-0] COUNT value will increment).

Pause frames will be transmitted if enabled and triggered regardless of whether or not the port is observing the pause time period from an incoming pause frame.

The Ethernet port will transmit pause frames as described below:

- The 48-bit reserved multicast destination address 01.80.C2.00.00.01.
- The 48-bit source address - from SL_SA[47-0] input.
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit pause time value FF.FF. A pause-quantum is 512 bit-times. Pause frames sent to cancel a pause request will have a pause time value of 00.00.
- Zero padding to 64-byte data length (The Ethernet port will transmit only 64 byte pause frames).
- The 32-bit frame-check sequence (CRC word).

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

If CPSW_PN_MAC_CONTROL_REG[3] RX_FLOW_EN is cleared to 0h while the pause time is nonzero, then the pause time will be cleared to 0h and a 0 count pause frame will be sent.

12.2.1.4.6.13.2 Flow Control Trigger

Receive flow control is triggered (when enabled), when the number of words in the receive FIFO is greater than or equal to the value writen in the CPSW_PN_RX_FLOW_THRESH_REG[8-0] COUNT bit field. The flow control packet runout is then contained in the remainder of the receive FIFO.

12.2.1.4.6.13.3 Ethernet Transmit Flow Control

Incoming pause frames are acted upon, when enabled, to prevent the Ethernet port from transmitting any further frames. Incoming pause frames are only acted upon when the [0] FULLDUPLEX and [4] TX_FLOW_EN bits in the CPSW_PN_MAC_CONTROL_REG register are set. Pause frames are not acted upon in half-duplex mode. Pause frame action will be taken if enabled, but normally the frame will be filtered and not transferred to memory. MAC control frames will be transferred to memory if the [24] RX_CMF_EN (RX Copy MAC Control Frames Enable) bit in the CPSW_PN_MAC_CONTROL_REG register is set. The [4] TX_FLOW_EN and [0] FULLDUPLEX bits effect whether or not MAC control frames are acted upon, but they have no effect upon whether or not MAC control frames are transferred to memory or filtered.

Pause frames are a subset of MAC Control Frames with an opcode field = 0001h. Incoming pause frames will only be acted upon by the port if:

- [4] TX_FLOW_EN is set in CPSW_PN_MAC_CONTROL_REG register, and
- the RX maximum frame length is 64 bytes inclusive (CPSW_PN_RX_MAXLEN_REG[13-0] RX_MAXLEN), and
- the frame contains no CRC error or align/code errors.

The pause time value from valid frames will be extracted from the two bytes following the opcode. The pause time will be loaded into the port's transmit pause timer and the transmit pause time period will begin.

If a valid pause frame is received during the transmit pause time period of a previous transmit pause frame then:

- if the destination address is not equal to the reserved multicast address or any enabled or disabled unicast address, then the transmit pause timer will immediately expire, or
- if the new pause time value is zero then the transmit pause timer will immediately expire, else the port transmit pause timer will immediately be set to the new pause frame pause time value. (Any remaining pause time from the previous pause frame will be discarded).

If [4] TX_FLOW_EN in CPSW_PN_MAC_CONTROL_REG register is cleared, then the pause-timer will immediately expire.

The port will not start the transmission of a new data frame any sooner than 512-bit times after a pause frame with a non-zero pause time has finished being received (MRXDV going inactive). No transmission will begin until the pause timer has expired (the port may transmit pause frames in order to initiate outgoing flow control). Any frame already in transmission when a pause frame is received will be completed and unaffected.

Incoming pause frames consist of the below:

- A 48-bit destination address equal to:
  - The reserved multicast destination address 01.80.C2.00.00.01, or the Ethernet port SL_SA [47:0] input.
- The 48-bit source address of the transmitting device.
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit CPSW_PN_MAC_TX_PAUSETIMER_REG[15-0] TX_PAUSETIMER. A pause-quantum is 512 bit-times.
- Padding to 64-byte data length.
- The 32-bit frame-check sequence (CRC word).

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

The padding is required to make up the frame to a minimum of 64 Bytes. The standard allows pause frames longer than 64 Bytes to be discarded or interpreted as valid pause frames. The Ethernet port will recognize any pause frame between 64 Bytes and CPSW_PN_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes in length.

12.2.1.4.6.14 Energy Efficient Ethernet Support (802.3az)

Energy Efficient Ethernet (EEE) allows the LPSC to turn off the module clock during inactive periods as determined by network and host traffic. The module can then be awakened by host queued transmit packet(s) or by a port's external Ethernet PHY. The module EEE clock stop interface is used by the external controller to control module EEE operations. EEE operations are configured as shown below:

1. The 12-bit EEE clock pre-scale value is written to the CPSW_EEE_PRESCALE_REG register. The pre-scaler is used to clock all EEE-related counters
2. The port Idle to LPI count values (CPSW_PN_IDLE2LPI_REG[23-0] COUNT) are written with the desired values
3. The port LPI to Wake count values (CPSW_PN_LPI2WAKE_REG[23-0] COUNT) are written with the desired values
4. The [0] EEE_EN bit is set in the switch CPSW_SS_CONTROL_REG register

EEE operation can begin after configuration. The host allows (through LPSC) the CPSW to enter a low power state by asserting the EEE_CLKSTOP_REQ signal. There are no requirements on host queues or traffic in order for the host to assert or de-assert EEE_CLKSTOP_REQ to the CPSW.

Each Ethernet port has a transmit and a receive LPI (low power indicate) state. The PHY indicates LPI by asserting MRXER with a MRXD[7:0] value of 0x01 while MRXDV is deasserted (inter-packet gap). The Ethernet transmit port indicates LPI after the CPSW_PN_IDLE2LPI_REG value has been counted (the transmit port has gone idle for the configured amount of time). If another packet is received for transmit during the count then the count is restarted. When the transmit port has been idle for the Idle to LPI time, the transmit port enters the LPI state and indicates LPI to the associated PHY. The LPI is indicated to the external PHY by an asserted MTXER with a MTXD[7:0] while MTXEN is deasserted (inter-packet gap). The CPPI (port 0) LPI state includes transmit and receive. The CPPI LPI state is entered when the CPPI transmit and receive have both been idle for the Idle to LPI time (CPSW_P0_IDLE2LPI_REG). The Idle to LPI time value for all ports must be large relative to the switch latency to ensure that the count is not able to complete between successive packets.

Note

External PHY signaling has the following conditions:

- RGMII is a DDR interface. TXEN and TXER are the sampled values of TX_CTL at the rising and the falling TXC edges, respectively. RXDV and RXER are the sampled values of RX_CTL at the rising and the falling RXC clock edges, respectively
- In RMII mode, EEE is not supported.

When all transmit and receive ports are in the LPI state (CPSW LPI state), the EEE_CLKSTOP_ACK signal is asserted, and the LPSC is allowed to stop the module clock. When EEE_CLKSTOP_ACK is asserted, the clock may be turned on and off as desired by the host. The host is allowed to restart the clock, perform target read/write operations to the CPSW memory address space, and then turn off the clock again while EEE_CLKSTOP_ACK is asserted.

The software can remove and disable from re-entering the CPSW LPI state by restarting the module clock and then de-asserting EEE_CLKSTOP_REQ. There must be at least one rising edge of the clock before EEE_CLKSTOP_REQ is de-asserted. The module EEE_CLKSTOP_ACK output signal will be deasserted on the clock after the de-assertion of EEE_CLKSTOP_REQ. The host may queue CPPI receive packets at any time without regard to the CPSW module LPI state. The Host must deassert EEE_CLKSTOP_REQ on wakeup for a minimum of two clock periods. If EEE_CLKSTOP_REQ is deasserted for less than 5 clock periods for a wakeup event from the host to a particular Ethernet port (or visa versa), then the wakeup event will not cause the other Ethernet port to awaken.

The external Ethernet PHY’s can also wakeup the LPSC by removing the Ethernet receive LPI indication. If the CPSW module is in Idle state with EEE_CLKSTOP_ACK asserted and the receive LPI indication is removed, the EEE_CLKSTOP_WAKEUP signal will be asynchronously asserted. On wakeup, the LPSC restarts the clock and de-assert the EEE_CLKSTOP_REQ signal. The EEE_CLKSTOP_WAKEUP signal will be synchronously deasserted with EEE_CLKSTOP_ACK. Upon the deassertion of EEE_CLKSTOP_REQ, the Ethernet ports will count the CPSW_PN_LPI2WAKE_REG time for each port at which time the port is available for transmit.

12.2.1.4.6.15 Ethernet Switch Latency

When CPSW is configured as a store and forward switch, the switch latency is defined as the amount of time between the end of packet reception of the received packet to the start of the output packet transmit.

The store and forward latency is shown in Table 12-177:

Table 12-177. Switch Latency

Mode	Latency
Gig (1000)	880 ns
100	1.3 µs
10	6.5 µs

12.2.1.4.6.16 MAC Emulation Control

The emulation control input (EMUSUSP) and submodule emulation control registers allow CPSW operation to be completely or partially suspended. Each Ethernet port has associated emulation control registers (CPSW_EM_CONTROL_REG and CPSW_PN_MAC_EMCONTROL_REG). The submodule emulation control registers must be accessed to facilitate CPSW emulation control. The CPSW module enters the emulation suspend state if all three submodules are configured for emulation suspend and the emulation suspend input is asserted. A partial emulation suspend state is entered if one or two submodules is configured for emulation suspend and the emulation suspend input is asserted. Emulation suspend occurs at packet boundaries. The emulation control feature is implemented for compatibility with other peripherals.

Ethernet port Emulation Control

The emulation control input (TBEMUSUP) and register bits (SOFT and FREE bits in the CPSW_PN_MAC_EMCONTROL_REG register) allow Ethernet port operation to be suspended. When the emulation suspend state is entered, the Ethernet port will stop processing receive and transmit frames at the next frame boundary. Any frame currently in reception or transmission will be completed normally without suspension. For receive, frames that are detected by the Ethernet port after the suspend state is entered are ignored.

Table 12-178 shows the operations of the emulation control input and register bits.

Table 12-178. Emulation Control Input

EMUSUSP	SOFT	FREE	Description
0	X	X	Normal Operation
1	0	0	Normal Operation
1	1	0	Emulation Suspend
1	X	1	Normal Operation

12.2.1.4.6.17 MAC Command IDLE

The CMD_IDLE bit in the CPSW_PN_MAC_CONTROL_REG register allows MAC operation to be suspended. When the idle state is commanded, the MAC will stop processing receive and transmit frames at the next frame boundary. Any frame currently in reception or transmission will be completed normally without suspension. For transmission, any complete or partial frame in the TX cell FIFO will be transmitted. For receive, frames that are detected by the MAC after the suspend state is entered are ignored. No statistics will be kept for ignored frames. Commanded idle is similar in operation to emulation control and clock stop.

12.2.1.4.6.18 CPSW Network Statistics

The CPSW has a set of statistics that record events associated with frame traffic on selected switch ports. The statistics values are cleared to zero 38 clocks after the rising edge of CPSW0_RST. When one ore more port enable (Pn_STAT_EN) bits in the CPSW_STAT_PORT_EN_REG register are set, all statistics registers are write to decrement. The value written will be subtracted from the register value with the result being stored in the register. If a value greater than the statistics value is written, then zero will be written to the register (writing 0xFFFF FFFF clears a statistics location). When all port enable bits are cleared to zero, all statistics registers are read/write (normal write direct, so writing 0x0000 0000 clears a statistics location). All write accesses must be 32-bit accesses.

The statistics interrupt (STAT_PEND0) will be issued if enabled when any statistics value is greater than or equal to 0x8000 0000. The statistics interrupt is removed by writing to decrement any statistics value greater than 0x8000 0000. The statistics are mapped into internal memory space and are 32-bits wide. All statistics rollover from 0xFFFF FFFF to 0x0000 0000.

Table 12-179 and Table 12-180 summarize network statistics.

12.2.1.4.6.18.1 Rx-only Statistics Descriptions

12.2.1.4.6.18.1.1 Good Rx Frames (Offset = 3A000h)

All ports

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.2 Broadcast Rx Frames (Offset = 3A004h)

All ports

The total number of good broadcast frames received on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for address FF.FF.FF.FF.FF.FF
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.3 Multicast Rx Frames (Offset = 3A008h)

All ports

The total number of good multicast frames received on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than FF.FF.FF.FF.FF.FF
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.4 Pause Rx Frames (Offset = 3A00Ch)

Ethernet port N where N = 1 to 2

The total number of IEEE 802.3X pause frames received by the port (whether acted upon or not). Such a frame:

- Contained any unicast, broadcast, or multicast address
- Contained the length/type field value 88.08 (hex) and the opcode 0x0001
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error
- Pause-frames had been enabled on the port (TX_FLOW_EN = 1h).

The port could have been in either half or full-duplex mode.

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.5 Rx CRC Errors (Offset = 3A010h)

All ports

The total number of frames received on the port that experienced a CRC error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no code/align error
- Had a CRC error

Overruns have no effect upon this statistic.

A CRC error is defined to be:

- A frame containing an even number of nibbles, and
- Failing the Frame Check Sequence test.

12.2.1.4.6.18.1.6 Rx Align/Code Errors (Offset = 3A014h)

Ethernet port N where N = 1 to 2

The total number of frames received on the port that experienced an alignment error or code error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had either an alignment error, or a code error.

Overruns have no effect upon this statistic.

An alignment error is defined to be:

- A frame containing an odd number of nibbles
- Failing the Frame Check Sequence test if the final nibble is ignored

A code error is defined to be a frame which has been discarded because the port's MRXER pin driven with a one for at least one bit-time's duration at any point during the frame's reception.

Note

RFC 1757 etherStatsCRCAlignErrors Ref. 1.5 can be calculated by summing Rx Align/Code Errors and Rx CRC errors.

12.2.1.4.6.18.1.7 Oversize Rx Frames (Offset = 3A018h)

All ports

The total number of oversized frames received on the port. An oversized frame is defined to be:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than RX_MAXLEN in bytes
- Had no CRC error, alignment error, or code error.

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.8 Rx Jabbers (Offset = 3A01Ch)

All ports

The total number of jabber frames received on the port. A jabber frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than RX_MAXLEN in bytes
- Had a CRC error, alignment error or code error

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.9 Undersize (Short) Rx Frames (Offset = 3A020h)

All ports

The total number of undersized frames received on the port. An undersized frame is defined to be:

- Was any data frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was less than 64 bytes
- Had no CRC error, alignment error, or code error

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.10 Rx Fragments (Offset = 3A024h)

Ethernet port N where N = 1 to 2

The total number of frame fragments received on the port. A frame fragment is defined to be:

- Any data frame (address matching does not matter)
- Less than 64 bytes long
- Having a CRC error, an alignment error, or a code error
- Not the result of a collision caused by half-duplex, collision-based flow control

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.11 RX IPG Error (Offset = 3A05Ch)

The total number of 10G frames received on a port that had a correct preamble but did not have at least five bytes of IDLE preceding the frame. This does not indicate if the frame with the IPG error was kept or ignored.

12.2.1.4.6.18.1.12 ALE Drop (Offset = 3A028h)

All ports

The total number of frames received on a port such that the destination address was not equal to the source address and the packet was not destined to the port it was received on, but the frame was not forwarded to any port (the PORT_MASK was zero).

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the destination address was not equal to the source address
- the packet was not destined for the port it was receive on
- had a zero PORT_MASK

12.2.1.4.6.18.1.13 ALE Overrun Drop (Offset = 3A02Ch)

All ports (non cut-thru mode)

The total number of frames received on a port that were dropped (zero PORT_MASK) due to exceeding the maximum ALE lookup rate (Port 0 should not have ALE Overrun Drops because the ingress rate is controlled to prevent it). This statistic should be zero and when non-zero indicates a system clock issue or indicates that short packets were sent with RX_CSF_EN at a rate that exceeded the maximum lookup rate.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- The port has no receive priorities enabled for cut-thru, and
- the maximum ALE lookup rate was exceeded so the lookup was aborted and the packet was dropped.

Ethernet Ports (cut-thru mode)

The total number of received frames on a port that were dropped due to packet errors. This statistic does not count error frames that are sent to the host with a set CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN or CPSW_PN_MAC_CONTROL_REG_k[24] RX_CMF_EN.

- was any data or MAC control frame, and
- the port has at least one receive priority enabled for cut thru, and
- the received packet was long, mac_control, code, align, crc error, and
- was dropped on receive (not transferred to the host due to error enable bits).

12.2.1.4.6.18.1.14 Rx Octets (Offset = 3A030h)

All ports

The total number of bytes in all good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the Section 12.2.1.4.6.18.1.6 , *Rx Align/Code Errors* and Section 12.2.1.4.6.18.1.5 , *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.2.1.4.6.18.1.15 Rx Bottom of FIFO Drop (Offset = 3A084h)

Ethernet port N where N = 1 to 2

The total number of frames received on a port that overran the port's receive FIFO and were dropped (bottom of receive FIFO). Port 0 (CPPI receive port) should not drop packets on receive because port 0 receive flow control should be enabled. The Ethernet ports will only drop packets in the receive FIFO when receive flow control is enabled and the sending port ignores sent pause frame and then overruns the receive FIFO. An overrun frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- Was dropped on port 0 due to a lack of memory space in the receive FIFO.

Note

This statistic should be zero if proper flow control is being followed.

Host port 0

This statistic also counts frames dropped on port 0 that were 17 to 63 bytes (only for port 0). For Ethernet ports, the drop count for frames shorter than 33 bytes is included in the undersized or fragment count. Port 0 simply gives an indication that a packet was dropped. No other statistics are counted for frames shorter than 33 bytes.

12.2.1.4.6.18.1.16 Portmask Drop (Offset = 3A088h)

All ports

The total number of frames received on a port that were dropped by the ALE (the ALE did not forward the packet to any port). Port mask drop frame is defined to be:

- Any data or MAC control frame
- Any length greater than 32 bytes
- Was dropped by the ALE due to PORT_MASK=0 (was not sent to any destination port)
- Was not a long or error packet with the port in cut-thru mode
- The frame could have been dropped due to error or other counted reason, so it could be counted elsewhere also.

Note

This statistic does not count in the overall total as it includes every packet received greater than 32 bytes that had a zero PORT_MASK.

12.2.1.4.6.18.1.17 Rx Top of FIFO Drop (Offset = 3A08Ch)

All ports

The total number of frames received on a port that had a start-of-frame (SOF) overrun on any destination port egress (when attempting to load the packet from the top of the ingress port receive FIFO into any other port's transmit FIFO). If a multicast/broadcast packet is dropped by multiple destination ports then this statistic will increment by the number of ports that dropped the packet. Rx Top Of FIFO Drop is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error or code error
- had a SOF of frame overrun on another port egress.

12.2.1.4.6.18.1.18 ALE Rate Limit Drop (Offset = 3A090h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to receive rate limiting on this port or due to transmit rate limiting on any destination port (not sent to all expected destination ports if transmit rate limiting).

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the receive rate was exceeded and the packet was dropped, or the transmit rate was exceeded to any destination port and the packet was dropped to one or more expected destination ports (indicates that the destinations were reduced due to rate limiting).

12.2.1.4.6.18.1.19 ALE VLAN Ingress Check Drop (Offset = 3A094h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to VLAN ingress check failure.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the VLAN ID ingress check failed (the receive port was not in the group)
- The address lookup did not return a match with the SUPER bit set.

12.2.1.4.6.18.1.19.1 ALE DA=SA Drop (Offset = 3A098h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to destination address equal to source address.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the destination address was equal to the source address
- the source address was not an entry in the table.

12.2.1.4.6.18.1.19.2 Block Address Drop (Offset = 3A09Ch)

The total number of frames received on a port that were dropped (zero PORT_MASK) due to the destination or source address being blocked.

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error, and
- the source or destination address matched a table entry with the block bit set.

12.2.1.4.6.18.1.19.3 ALE Secure Drop (Offset = 3A0A0h)

The total number of frames received on a port that were dropped (zero port_mask) due to a secure violation (the source address is owned by a different receive port).

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)

- had no CRC error, alignment error, or code error, and
- the source address is an entry in the table with the SECURE bit set and a port number for a different receive port.

12.2.1.4.6.18.1.19.4 ALE Authentication Drop (Offset = 3A0A4h)

The total number of frames received on a port that were dropped (zero port_mask) due to authentication failure.

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error, and
- CPSW_ALE_CONTROL[1] ENABLE_AUTH_MODE is set to 1h, and
- the source address is not equal to the destination address, and
- the source address is not a table entry, and
- the destination address is not a table entry with the SUPER bit set.

12.2.1.4.6.18.1.19.5 ALE Unknown Unicast (Offset = 3A0A8h)

All ports

The total number of frames received on a port that had a unicast destination address with an unknown source address.

- was any data frame with a unicast destination address
- the source address was not a table entry
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

Note: The ALE Unknown Unicast Bytecount statistic is the number of bytes contained in the ALE Unknown Unicast frames.

12.2.1.4.6.18.1.19.6 ALE Unknown Unicast Bytecount (Offset = 3A0ACh)

The total number of bytes received on a port that had a unicast destination address with an unknown source address.

12.2.1.4.6.18.1.19.7 ALE Unknown Multicast (Offset = 3A0B0h)

The total number of frames received on a port that had a multicast destination address with an unknown source address. The frame is defined to be:

- was any data frame with a unicast destination address
- the source address was not a table entry, and
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error or code error

Note: The ALE Unknown Multicast Bytecount statistic is the number of bytes contained in the ALE Unknown Multicast frames.

12.2.1.4.6.18.1.19.8 ALE Unknown Multicast Bytecount (Offset = 3A0B4h)

The total number of bytes received on a port that had a multicast destination address with an unknown source address.

12.2.1.4.6.18.1.19.9 ALE Unknown Broadcast (Offset = 3A0B8h)

The total number of frames received on a port that had a broadcast destination address with an unknown source address. The frame is defined to be:

- was any data frame with a unicast destination address
- the source address was not a table entry, and
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error or code error

Note: The ALE Unknown Broadcast Bytecount statistic is the number of bytes contained in the ALE Unknown Broadcast frames.

12.2.1.4.6.18.1.19.10 ALE Unknown Broadcast Bytecount (Offset = 3A0BCh)

The total number of bytes received on a port that had a broadcast destination address with an unknown source address.

12.2.1.4.6.18.1.19.11 ALE Policer/Classifier Match (Offset = 3A0C0h)

All ports

The total number of frames received on a port that matched a policer. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.2.1.4.6.18.2 ALE Policer Match Red (Offset = 3A0C4h)

The total number of frames received on a port that had matched a policer and the condition was red. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.2.1.4.6.18.3 ALE Policer Match Yellow (Offset = 3A0C8h)

The total number of frames received on a port that had matched a policer and the condition was red. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.2.1.4.6.18.4 IET Receive Assembly Error (Offset = 3A140h)

The total number of premptable received frames with IET assembly errors.

- any frame received
- was any size, and
- was a non-initial fragment that mismatched the frame count or fragment count (went to the assembly error state in the IET receive state machine)

12.2.1.4.6.18.5 IET Receive Assembly OK (Offset = 3A144h)

The total number of correctly received and re-assembled premptable frames.

- any premptable frame received
- was any size, and
- was correctly received and re-assembled without error

12.2.1.4.6.18.6 IET Receive SMD Error (Offset = 3A148h)

The total number of received frames rejected due to an unknown SMD value or received frames rejected with an SMD-C when no frame is in progress.

- any frame received
- was any size, and
- was rejected because of an unknown SMD value or SMD-C with no frame in progress.

Note: If IET_ENABLE is not set, this statistic counts any received frame with any non express SMD.

12.2.1.4.6.18.7 IET Receive Merge Fragment Count (Offset = 3A14Ch)

The total number of received non-initial fragments that did not have an assembly error. The IET stat CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j is derived by adding the Receive Assembly Error count to this value.

- any frame received
- was any size, and
- was a non-initial fragment that did not contain an assembly error

12.2.1.4.6.18.8 Rx Cut Thru with No Delay

The total number of frames received on the port and subsequently sent cut-thru to all internal destination port FIFOs with no delay. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port to all destination ports without delay.

12.2.1.4.6.18.9 Rx Cut Thru with Delay

The total number of frames received on the port and subsequently sent cut-thru to all destination ports with some amount of delay. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port to all destination ports with some amount of delay.

12.2.1.4.6.18.10 Rx Cut Thru Store-and-Forward

The total number of frames received on the port were attempted to be sent cut-thru to all destination ports but were held off due to configuration or traffic conditions. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was attempted to be sent cut-thru by the receive port to all destination ports but was sent store-and-forward.

12.2.1.4.6.18.11 Tx-only Statistics Descriptions

The maximum and minimum transmit frame size is software controllable.

12.2.1.4.6.18.11.1 Good Tx Frames (Offset = 3A034h)

All ports

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

Note

A nonzero CPSW_STATN_TXDEFERREDFRAMES_k value should be subtracted from this value to obtain the actual good frames value (the good frames statistic also increments on a transmitted CRC error).

12.2.1.4.6.18.11.2 Broadcast Tx Frames (Offset = 3A038h)

All ports

The total number of good broadcast frames transmitted on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address FF.FF.FF.FF.FF.FF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

12.2.1.4.6.18.11.3 Multicast Tx Frames (Offset = 3A03Ch)

All ports

The total number of good multicast frames transmitted on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than FF.FF.FF.FF.FF.FF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

12.2.1.4.6.18.11.4 Pause Tx Frames (Offset = 3A040h)

Ethernet port N where N = 1 to 2

This statistic indicates the number of IEEE 802.3X pause frames transmitted by the port.

Pause frames cannot contain a CRC error because they are created in the transmitting MAC, so these error conditions have no effect upon the statistic. Pause frames sent by software will not be included in this count.

Since pause frames are only transmitted in full duplex, carrier loss and collisions have no effect upon this statistic.

Transmitted pause frames are always 64-byte multicast frames so will appear in the *Tx Multicast Frames* and *64octet Frames* statistics.

12.2.1.4.6.18.11.5 Deferred Tx Frames (Offset = 3A044h)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that first experienced deferment. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced no collisions before being successfully transmitted
- Found the medium busy when transmission was first attempted, so had to wait.

CRC errors have no effect upon this statistic.

12.2.1.4.6.18.11.6 Collisions (Offset = 3A048h)

Ethernet port N where N = 1 to 2

This statistic records the total number of times that the port experienced a collision. Collisions occur under two circumstances.

1. When a transmit data or MAC control frame:
    - Was destined for any unicast, broadcast or multicast address
    - Was any size
    - Had no carrier loss and no underrun
    - Experienced a collision. A jam sequence is sent for every non-late collision, so this statistic will increment on each occasion if a frame experiences multiple collisions (and increments on late collisions)

    CRC errors have no effect upon this statistic.
2. When the port is in half-duplex mode, flow control is active, and a frame reception begins.

12.2.1.4.6.18.11.7 Single Collision Tx Frames (Offset = 3A04Ch)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that experienced exactly one collision. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced one collision before successful transmission. The collision was not late.

CRC errors have no effect upon this statistic.

12.2.1.4.6.18.11.8 Multiple Collision Tx Frames (Offset = 3A050h)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that experienced multiple collisions. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 2 to 15 collisions before being successfully transmitted. None of the collisions were late.

CRC errors have no effect upon this statistic.

12.2.1.4.6.18.11.9 Excessive Collisions (Offset = 3A054h)

Ethernet port N where N = 1 to 2

The total number of frames for which transmission was abandoned due to excessive collisions. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 16 collisions before abandoning all attempts at transmitting the frame. None of the collisions were late.

CRC errors have no effect upon this statistic.

12.2.1.4.6.18.11.10 Late Collisions (Offset = 3A058h)

Ethernet port N where N = 1 to 2

The total number of frames on the port for which transmission was abandoned because they experienced a late collision. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Experienced a collision later than 512 bit-times into the transmission. There may have been up to 15 previous (non-late) collisions which had previously required the transmission to be re-attempted. The *Late Collisions* statistic dominates over the single-, multiple- , and excessive- collision statistics. If a late collision occurs, the frame will not be counted in any of these other three statistics.

CRC errors have no effect upon this statistic.

12.2.1.4.6.18.11.11 Carrier Sense Errors (Offset = 3A060h)

Ethernet port N where N = 1 to 2

The total number of frames on the port that experienced carrier loss. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- The carrier sense condition was lost or never asserted when transmitting the frame (the frame is not retransmitted). This is a transmit only statistic. Carrier Sense is a don’t care for received frames. Transmit frames with carrier sense errors are sent until completion and are not aborted.

CRC errors have no effect upon this statistic.

12.2.1.4.6.18.11.12 Tx Octets (Offset = 3A064h)

All ports

The total number of bytes in all good frames transmitted on the port. A good frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Was any size
- Had no late or excessive collisions, no carrier loss and no underrun.

12.2.1.4.6.18.11.13 Transmit Priority 0-7 (Offset = 3A180h to 3A1A8h)

The total number of frames transmitted on the port from transmit FIFO priority 0-7. Collision retries do not affect this statistic. Pause frames do not affect this statistic.

- Any frame transmitted from priority 0-7, and
- Was less than or equal to CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG
- Collision retries are not counted in this statistic.
- Pause frames are not counted in this statistic.
- Carrier sense errors do not affect this statistic.

Note: The Transmit Priority 0-7 Bytecount statistic is the number of bytes contained in the frames of the Transmit Priority 0-7 statistic.

12.2.1.4.6.18.11.14 Transmit Priority 0-7 Drop (Offset = 3A1C0h to 3A1E8)

The total number of transmit frames on the port that overran the transmit FIFO priority 0-7 and were dropped. This count includes frames dropped due to CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG.

- Any frame destined to be transmitted from priority 0-7, and
- Was any size, and
- Was dropped due to priority 0-7 FIFO overrun (Start of packet overrun).
- Was dropped due to frame size larger than CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG.

Note: The Transmit Priority 0-7 Drop Bytecount statististic is the number of bytes contained in the frames of the Transmit Priority 0-7 Drop statistic.

12.2.1.4.6.18.11.15 Tx Memory Protect Errors (Offset = 3A17Ch)

All ports

The total number of transmit frames on the port that had a memory protect CRC error on egress:

- Any frame destined to be transmitted,
- Was any size
- Had a memory protect CRC error on egress.

Note

1. Frames to the host with memory protect errors are dropped via TXST_DROP. Ethernet frames will have at least one byte of the generated port type CRC inverted on egress.
2. This statistic is 8-bits wide only and will not rollover but will limit at 0xFF.
3. A non-zero value in this statistic will issue a STAT_PEND0 interrupt for the associated port.

12.2.1.4.6.18.11.16 IET Transmit Merge Hold Count (Offset = 3A150h)

The total number of premptable frames that were prempted and reassembled by the assertion of MAC_HOLD in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG register or were prempted by Enhanced Scheduled Traffic (EST). The IET statistic can be derived and maintained by software.

- Any frame destined to be transmitted on the premptable port, and

- was any size, and
- was prempted by the assertion of MAC_HOLD.
- was prempted by Enhanced Scheduled Traffic (EST).

12.2.1.4.6.18.11.17 IET Transmit Merge Fragment Count (Offset = 3A14Ch)

The total number of non-initial premptable transmit fragments on premptable transmit.

- Any frame destined to be transmitted on the premptable port, and
- Was any size, and
- was a non-initial fragment.

12.2.1.4.6.18.11.18 Tx CRC Errors

The total number of frames transmitted on the port with a CRC error. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size, and
- was sent cut-thru by the receive port and was received with a CRC error, or
- was a transmitted frame that also had a memory protect error (counted also in CPSW_STATN_TX_MEMORY_PROTECT_ERROR_k).

Note

For port0 this statistics location (CPSW_STAT0_TXDROP) counts the number of drops to the host due to a memory protect error, or due to a cut-thru packet having an error on reception but was forwarded with the error. The Ethernet port receive error could be long, CRC, jabber, or code. For Ethernet ports, the receive error could be the same but the packet is transmitted with at least one byte of the actual outgoing packet CRC inverted to indicate the error.

Note

A nonzero CPSW_STATN_TXDEFERREDFRAMES_k value should be subtracted from the CPSW_STATN_TXGOODFRAMES_k value to obtain the actual good frames value (the good frames statistic also increments on a transmitted CRC error).

12.2.1.4.6.18.11.19 Tx Cut Thru

The total number of cut-thru frames transmitted on the port with or without delay. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port.
- was transmitted cut-thru with or without delay.

12.2.1.4.6.18.11.20 Tx Cut Thru Store-and-Forward

The total number of cut-thru frames transmitted store and forward. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port.
- was transmitted store-and-forward due to traffic congestion.

12.2.1.4.6.18.12 Rx- and Tx (Shared) Statistics Descriptions

12.2.1.4.6.18.12.1 Rx + Tx 64 Octet Frames (Offset = 3A068h)

All ports

The total number of 64-byte frames received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address

- Did not experience late collisions, excessive collisions, or carrier sense error
- Was exactly 64 bytes long. (If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic).

CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

12.2.1.4.6.18.12.2 Rx + Tx 65–127 Octet Frames (Offset = 3A06Ch)

All ports

The total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 65 to 127 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.2.1.4.6.18.12.3 Rx + Tx 128–255 Octet Frames (Offset = 3A070h)

All ports

The total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 128 to 255 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.2.1.4.6.18.12.4 Rx + Tx 256–511 Octet Frames (Offset = 3A074h)

All ports

The total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 256 to 511 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.2.1.4.6.18.12.5 Rx + Tx 512–1023 Octet Frames (Offset = 3A078h)

All ports

The total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 512 to 1023 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.2.1.4.6.18.12.6 Rx + Tx 1024_Up Octet Frames (Offset = 3A07Ch)

All ports

The total number of frames of size 1024 to RX_MAXLEN bytes for receive or 1024 up for transmit on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 1024 to RX_MAXLEN bytes long on receive, or any size on transmit

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.2.1.4.6.18.12.7 Net Octets (Offset = 3A080h)

All ports

The total number of bytes of frame data received and transmitted on the port. Each frame counted:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address (address match does not matter)
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)

Also counted in this statistic is:

- Every byte transmitted before a carrier-loss was experienced
- Every byte transmitted before each collision was experienced, (that is, multiple retries are counted each time)
- Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting)

Error conditions such as alignment errors, CRC errors, code errors, overruns and underruns do not affect the recording of bytes by this statistic.

The objective of this statistic is to give a reasonable indication of Ethernet utilization.

12.2.1.4.6.18.13

Table 12-179. Rx Statistics Summary

Rx Statistic	Frame/ Oct	Rx/ Rx+ Tx	Frame Type					Frame Size (bytes)								Event				
			MAC control		Data(5)															
			Pause frame	Non-pause(4)	Multi cast	Broad cast	Uni cast	<64	64	65-127	128-255	256-511	512-1023	1024-rx_ max len	>rx_ max len	Flow Coll.(8)	CRC Error	Align/ Code	Overrun	Addr. Disc.
Good Rx Frames	F	Rx	(y|(1)	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-(2)	n	n	-	n
Broadcast Rx Frames	F	Rx	(%|(6)	%|	n	y)	n	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	n
Multicast Rx Frames	F	Rx	(%|	%|	y)	n	n	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	n
Pause Rx Frames	F	Rx	y	n	n	n	n	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	-
Rx CRC Errors	F	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	y	n	-	n
Rx Align/Code Errors	F	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	-	y	-	n
Oversized Rx Frames	F	Rx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	n	y	-	n	n	-	n
Rx Jabbers	F	Rx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	n	y	-	(y|	y)	-	n
Undersized Rx Frames	F	Rx	n	n	(y|	y|	y)	y	n	n	n	n	n	n	n	-	n	n	-	n
Rx Fragments	F	Rx	n	n	(y|	y|	y)	y^(7)	n	n	n	n	n	n	n	-	(y|	y)	-	-
Rx Overruns(9)	F	Rx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y|	y)	-	-	-	y	n
64octet Frames	F	Rx+ Tx(3)	(y|	y|	y|	y|	y)	n	y	n	n	n	n	n	n	-	-	-	-	n
65-127octet Frames	F	Rx+ Tx	(y|	y|	y|	y|	y)	n	n	y	n	n	n	n	n	-	-	-	-	n
128-255octet Frames	F	Rx+ Tx	(y|	y|	y|	y|	y)	n	n	n	y	n	n	n	n	-	-	-	-	n

Table 12-179. Rx Statistics Summary (continued)

Rx Statistic	Frame/Oct	Rx/Rx+Tx	Frame Type					Frame Size (bytes)								Event				
			MAC control		Data(5)															
			Pause frame	Non-pause(4)	Multicast	Broadcast	Unicast	<64	64	65-127	128-255	256-511	512-1023	1024-rx_maxlen	>rx_maxlen	Flow Coll.(8)	CRC Error	Align/Code	Overrun	Addr. Disc.
256-511octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	y	n	n	n	-	-	-	-	n
512-1023octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	y	n	n	-	-	-	-	n
1024-UPoctet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	y	n	-	-	-	-	n
Rx Octets	O	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	n
Net Octets	O	Rx+Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y|	y|	y)	-	-	-	-

(1) "AND" is assumed horizontally across the table between all conditions which form the statistic (marked y or n) except where (y|y), meaning "OR" is indicated. Parentheses are significant.

(2) "-" indicates conditions which are ignored in the formations of the statistic.

(3) Statistics marked "Rx+Tx" are formed by summing the Rx and Tx statistics, each of which is formed independently.

(4) The non-pause column refers to all MAC control frames (for example, frames with length/type=88.08) with opcodes other than 0x0001. The pauseframe column refers to MAC frames with the opcode=0x0001.

(5) The multicast, broadcast and unicast columns in the table refer to non-MAC Control/non-pause frames (i.e. data frames).

(6) "%" If either a MAC control frame or pause frame has a multicast or broadcast destination address then the appropriate statistics will be updated.

(7) "y^" Frame fragments are not counted if less than 8 bytes.

(8) Flow coll. are half-duplex collisions forced by the MAC to achieve flow-control. A collision will be forced during the first 8 bytes so should not show in frame fragments. Some of the '-'s in this column might in reality be 'n's.

(9) The rx_overruns stat is for RX_MOF_OVERRUNS and RX_SOF_OVERRUNS added together.

Table 12-180. Tx Statistics Summary

Tx Statistic(9)	Frame/Oct	Tx/Rx+Tx	Frame Type					Frame Size (bytes)							Event									
			MAC control(4)		Data											Collision Type								
			Pause-MAC	Any-CPU	Multicast	Broadcast	Unicast	64	65-127	128-255	256-511	512-1023	1024-1535	>1535	CRC Error	Flow(8)	1	2-15	16	Late	No Carrier	Queued	Deferred	Underrun
Good Tx Frames	F	Tx	(y|(1)	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-(2)	-	-	-	n	n	n	-	-	n
Broadcast Tx Frames	F	Tx	n	(%|(5)	n	y)	n	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Multicast Tx Frames	F	Tx	(y|	%|	y)	n	n	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Pause Tx Frames	F	Tx	y	n	n	n	n	y	n	n	n	n	n	n	-	-	-	-	-	-	-	-	-	-
Collisions	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	(+(6)	+	+	+	+)	n	-	-	-
Single Collision Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	y	n	n	n	n	-	-	-

Table 12-180. Tx Statistics Summary (continued)

Tx Statistic[9]	Frame/Oct	Tx/Rx+Tx	Frame Type					Frame Size (bytes)							Event									
			MAC control[4]	Data												Collision Type								
			Pause-MAC	Any-CPU	Multicast	Broadcast	Unicast	64	65-127	128-255	256-511	512-1023	1024-1535	>1535	CRC Error	Flow[8]	1	2-15	16	Late	No Carrier	Queued	Deferred	Underrun
Multiple Collision Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	y	n	n	n	-	-	-
Excessive Collisions	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	n	y	n	n	-	-	-
Late Collisions	F	Tx	n	(y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	-	-	-	-	-	y	-	-	-	-
Deferred Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	n	n	n	n	-	y	n
Carrier Sense Errors	F	Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	-	-	y	-	-	-
64octet Frames	F	Rx+Tx (3)	(y|	y|	y|	y|	y)	y	n	n	n	n	n	n	-	-	-	-	n	n	n	-	-	-
65-127octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	y	n	n	n	n	n	-	-	-	-	n	n	n	-	-	-
128-255octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	y	n	n	n	n	-	-	-	-	n	n	n	-	-	-
256-511octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	y	n	n	n	-	-	-	-	n	n	n	-	-	-
512-1023octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	y	n	n	-	-	-	-	n	n	n	-	-	-
1024-UPoctet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	y	y	-	-	-	-	n	n	n	-	-	-
Tx Octets	O	Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Net Octets	O	Rx+Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	$[7]	$	$	$	$	-	-	-

(1) "AND" is assumed horizontally across the table between all conditions which form the statistic (marked y or n) except where (y|y), meaning "OR" is indicated. Parentheses are significant.

(2) "-" indicates conditions which are ignored in the formations of the statistic.

(3) Statistics marked "Rx+Tx" are formed by summing the Rx and Tx statistics, each of which is formed independently.

(4) Pause (MAC) frames are issued in the MAC as perfect (no CRC error) 64 byte frames in full duplex only, so they cannot collide.

(5) "%" If a CPU sourced MAC control frame has a multicast or broadcast destination address then the appropriate statistics will be updated.

(6) "+" indicates collisions which are "summed" (i.e. every collision is counted in the Collisions statistic). Jam sequences used for halfduplex flow control are also counted.

(7) "$" Every byte written on the wire during each retry attempt is also counted in addition to frames which experience no collisions or carrier loss.

(8) The flow collision type is for half-duplex collisions forced by the MAC to achieve flow control. Some of the '-'s in this column might in reality be 'n's. To prevent double-counting, Net Octets are unaffected by the jam sequence – the 'received' bytes, however, are counted. (See Table 12-179.)

(9) When the transmit Tx FIFO is drained due to the MAC being disabled or link being lost, then the frames being purged will not appear in the Tx statistics.

12.2.1.4.7 Common Platform Time Sync (CPTS)

The Common Platform Time Sync (CPTS) module is used to facilitate host control of time sync operations. It enables compliance with the IEEE 1588-2008 standard for a precision clock synchronization protocol.

Main features of CPTS module are:

- Supports the selection of multiple external clock sources
- Software control of time sync events via interrupt or polling
- Supports up to 8 hardware timestamp push inputs
- Supports timestamp counter compare output (CPTS_COMP)
- Supports timestamp counter bit output (CPTS_SYNC)
- Supports a configurable number of timestamp Generator bit outputs (CPTS_GENFn).
- Supports Ethernet Enhanced Scheduled Traffic Operations (CPTS_ESTFn).
- 32-bit and 64-bit timestamp modes with PPM and nudge adjustment.

12.2.1.4.7.1 CPSW0 CPTS Integration

This section describes CPTS module integration in the CPSW0 module, including information about clocks, resets, and hardware requests.

Figure 12-120 shows CPTS integration in the device CPSW0 module.

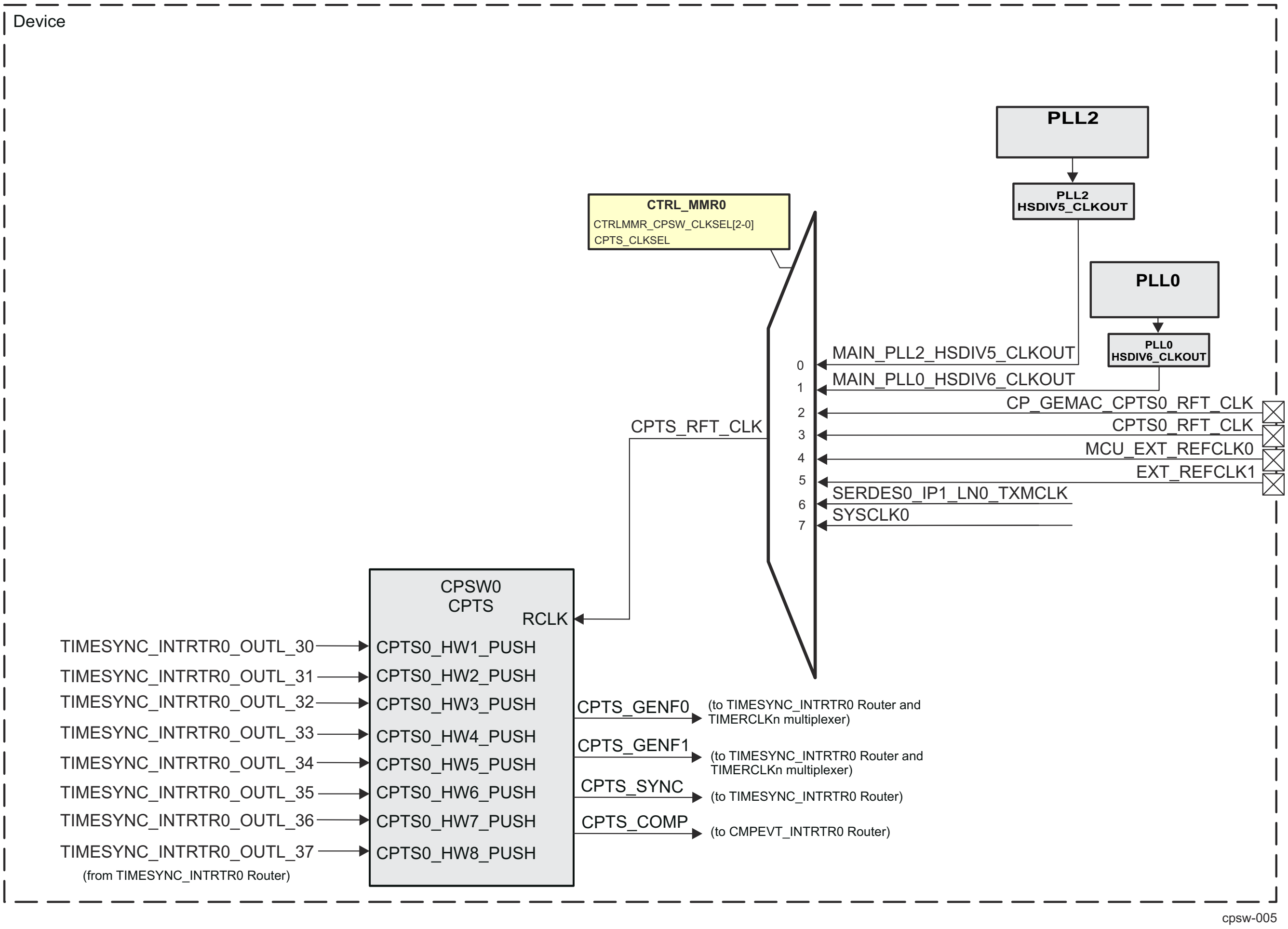

Figure 12-120. CPSW0 CPTS Integration

CPTS IEEE 1588 clock (RCLK) is selected through the MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL register.

Note

For more information about CPTS clocks and resets, see Table 12-154 in Section 12.2.1.3 *CPSW0 Integration*.

12.2.1.4.7.2 CPTS Architecture

Figure 12-121 shows the architecture of the CPTS module inside the CPSW Ethernet Subsystem. Time stamp values for every packet transmitted or received on external port of the CPSW are recorded. At the same time, each packet is decoded to determine if it is a valid time sync event. If so, an event is loaded into the Event FIFO for processing containing the recorded time stamp value when the packet was transmitted or received.

In addition, both hardware (HWn_TS_PUSH) and software (TS_PUSH) can be used to read the current time stamp value though the Event FIFO. The reference clock used for the time stamp (CPTS_RFT_CLK) can be derived from several sources.

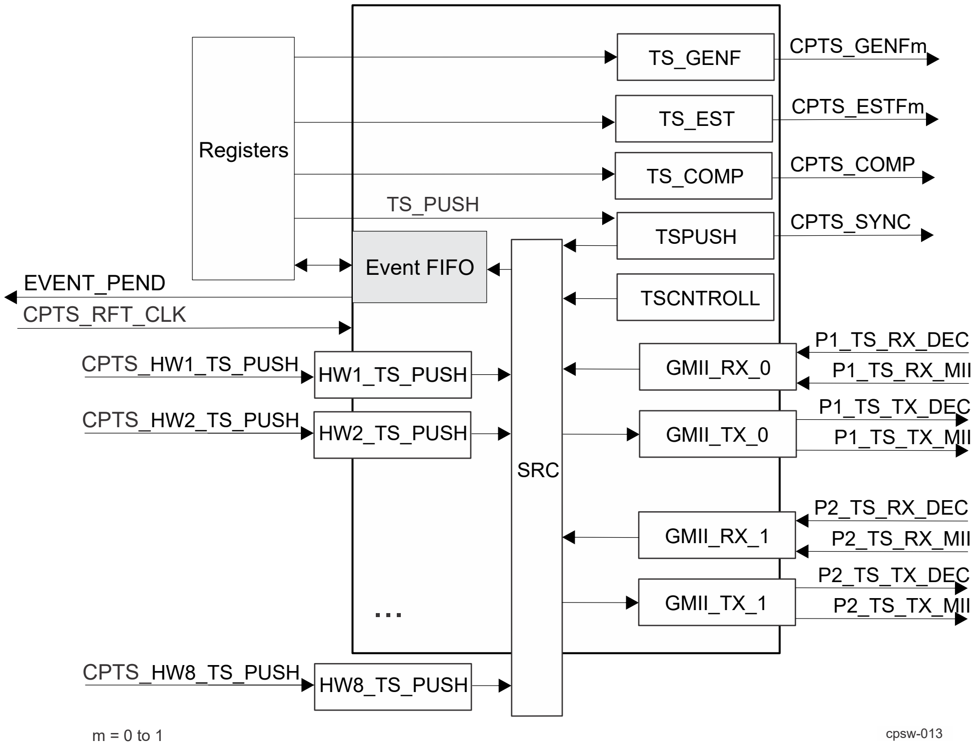

Figure 12-121. CPTS Block Diagram

Note

See *CPSW0 CPTS Integration* for CPTS integration in the device CPSW0 module.

12.2.1.4.7.3 CPTS Initialization

The CPTS module should be configured as follows:

1. Reset the CPTS module.
2. Write the CPTS_CLKSEL value in the CTRLMMR_CPTS_CLKSEL register with the desired reference clock selection. This value is allowed to be written only when the CPTS_EN bit in the CPSW_CPTS_CONTROL_REG register is cleared to zero.
3. Set the CPTS_EN bit in the CPSW_CPTS_CONTROL_REG register.

4. If using interrupts and not polling, enable the interrupt by setting the TS_PEND_EN bit in the CPSW_CPTS_INT_ENABLE_REG register.

12.2.1.4.7.4 32-bit Time Stamp Value

The time stamp value is a 32-bit value that increments on each CPTS_RFT_CLK rising edge when CPTS_EN bit is set to 1h. When CPTS_EN bit is cleared to 0h, the time stamp value is reset to 0h.

If more than 32-bits of time stamp are required by the application, the host software must maintain the necessary number of upper bits. The upper time stamp value should be incremented by the host when the rollover event is detected.

For test purposes, the time stamp can be written via the time stamp load function (CPSW_CPTS_TS_LOAD_VAL_REG / CPSW_CPTS_TS_LOAD_HIGH_VAL_REG and CPSW_CPTS_TS_LOAD_EN_REG registers).

12.2.1.4.7.5 64-bit Time Stamp Value

The time stamp value is a 64-bit value that increments on each CPTS_RFT_CLK rising edge when CPTS_EN bit is set to 1h. When CPTS_EN bit is cleared to 0h, the time stamp value is reset to 0h.

64-bit mode is selected when CPSW_CPTS_CONTROL_REG[5] MODE bit set to 1h.

For test purposes, the time stamp value can be written via the time stamp load function (CPSW_CPTS_TS_LOAD_EN_REG, CPSW_CPTS_TS_LOAD_VAL_REG, and CPSW_CPTS_TS_LOAD_HIGH_VAL_REG registers). The CPSW_CPTS_TS_ADD_VAL_REG feature is included to allow 1ns timestamp operations with an CPTS_RFT_CLK rate less than 1Ghz. Table 12-181 shows the CPTS_RFT_CLK and CPSW_CPTS_TS_ADD_VAL_REG values for 1ns operations.

Table 12-181. ADD_VAL feature

CPTS_RFT_CLK (MHz)	CPSW_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL
1 GHz	0
500 MHz	1
333.33 MHz	2
250 MHz	3
200 MHz	4
166.66 MHz	5
142.85714 MHz	6
125 MHz	7

12.2.1.4.7.6 64-Bit Timestamp Nudge

The 64-bit TIME_STAMP value can be adjusted by writing the CPSW_CPTS_TS_NUDGE_VAL_REG[7-0] TS_NUDGE_VAL bit field value which is a two's complement value. A value of FFh will subtract 1 clock cycle from the next incremented 64-bit time stamp value (CPSW_CPTS_EVENT_0_REG[31-0] TIME_STAMP and CPSW_CPTS_EVENT_3_REG[31-0] TIME_STAMP value). A nudge value of 1h will add 1 clock cycle to the next incremented TIME_STAMP[63-0] value. For example, if the current TIME_STAMP value is F06h, and CPSW_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL = 3h, the next incremented timestamp value would be F0Ah without a nudge and F0Ah +/- [7-0] TS_NUDGE_VAL with a nudge. The [7-0] TS_NUDGE_VAL value is cleared to zero when the nudge has occurred.

12.2.1.4.7.7 64-bit Timestamp PPM

The 64-bit TIME_STAMP can be adjusted by parts per million or by parts per hour. Writing a non-zero value to the CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL (Time stamp PPM Low value) and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL (Time stamp PPM High value) enables PPM operations. The adjustment is up or down depending on the [7] TS_PPM_DIR bit in the CPSW_CPTS_CONTROL_REG register. The TIME_STAMP value is increased by the PPM value when [7]

TS_PPM_DIR bit is cleared. The TIME_STAMP value is decreased by the PPM value when [7] TS_PPM_DIR bit is set.

Parts Per Million example:
To adjust for 100 parts per million the configured value for TS_PPM[41-0] (through CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL) is:
1,000,000/100 = 10,000(decimal)

Parts Per Hour example:
To adjust for 1 part per hour at 1 GHz CPTS_RFT_CLK the configured value for TS_PPM[41-0] (through CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL) is:
(1,000,0000,000Hz/1pph) * (3600 seconds/hour) = 34630B8A000 (hex)

12.2.1.4.7.8 Event FIFO

All time sync events are pushed onto the Event FIFO. There are 32 locations in the event FIFO with no overrun indication supported. Software must service the event FIFO in a timely manner to prevent FIFO overrun.

12.2.1.4.7.9 Timestamp Compare Output

CPTS features one Time Stamp Compare (CPTS_COMP) output. The CPTS_COMP function is a software oriented feature that is intended to be replaced going forward by the hardware oriented GENF function. CPTS_COMP is not compatible with timepstamp PPM or a non-zero CPSW_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL value.

12.2.1.4.7.9.1 Non-Toggle Mode: 32-bit

The CPTS_COMP output is asserted for CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH periods when the CPSW_CPTS_EVENT_0_REG[31-0] TIME_STAMP value (lowe 32-bits) compares with the CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL and the length value is non-zero. The CPTS_COMP rising edge occurs three CPTS_RFT_CLK clock periods after the values compare. A timestamp compare event is pushed into the event FIFO when CPTS_COMP is asserted. The polarity of the CPTS_COMP output is determined by the CPSW_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit. The output is asserted low when the polarity bit is 0h.

12.2.1.4.7.9.2 Non-Toggle Mode: 64-bit

64-bit mode operation is identical to 32-bit mode except that all 64-bits of the TIME_STAMP are used (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG). In 32-bit mode only the lower 32-bits (CPSW_CPTS_EVENT_0_REG) are used.

12.2.1.4.7.9.3 Toggle Mode: 32-bit

The CPTS_COMP output is asserted (CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH) for CPTS_RFT_CLK clock periods when the TIME_STAMP[31:0] value compares with the CPSW_CPTS_TS_COMP_VAL_REG and the length value is non-zero. The CPTS_COMP toggles thereafter on CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_LENGTH for CPTS_RFT_CLK periods. The length high or low can be adjusted by writing the CPSW_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE bit field value which is a two's complement value. A value of FFh will subtract one CPTS_RFT_CLK period from the CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_LENGTH value. A value of 0x01h will add one CPTS_RFT_CLK period to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH value. Only a single high or low time is adjusted (nudged) and the CPSW_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE value is cleared to zero when the nudge has occurred. The CPTS_COMP output is asserted low when the CPSW_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit is 0h. No compare events and no CPTS_EVNT interrupts are generated in toggle mode. The CPSW_CPTS_CONTROL_REG[6] TS_COMP_TOG bit must be set for toggle mode (value 1h). Note this bit must be set before writing a non-zero value to CPSW_CPTS_TS_COMP_VAL_REG register.

12.2.1.4.7.9.4 Toggle Mode: 64-bit

64-bit mode operation is identical to 32-bit mode except that all 64-bits of the TIMESTAMP are used (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG). In 32-bit mode only the lower 32-bits (CPSW_CPTS_EVENT_0_REG) are used.

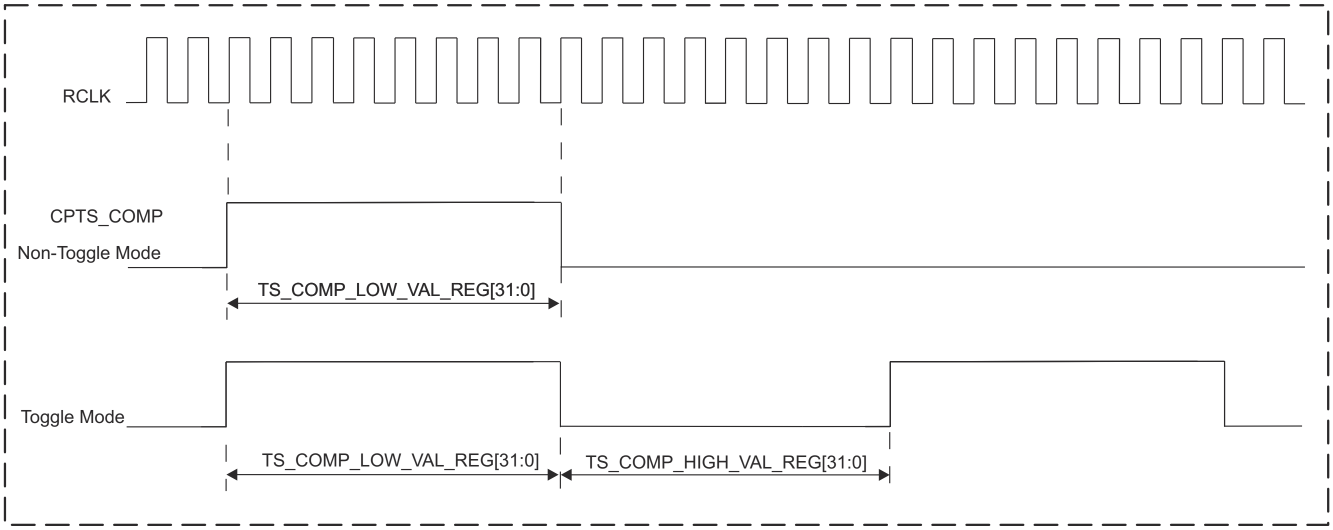

cpsw-0013a

Figure 12-122. CPTS_COMP Output in Toggle and Non-Toggle Mode

12.2.1.4.7.10 Timestamp Sync Output

The CPTS_SYNC output is a selected bit of the [31-0]TIME_STAMP counter value. One of bits 17-31 can be selected in CPSW_CPTS_CONTROL_REG[31-28] TS_SYNC_SEL. The CPTS_SYNC output is disabled when CPSW_CPTS_CONTROL_REG[31-28] TS_SYNC_SEL is zero.

If the selected counter bit is 1 at the time when TS_SYNC_SEL value is written then a rising edge will not occur on the CPTS_SYNC output. A rising edge will occur on the CPTS_SYNC output upon the next transition to 1 of the selected counter bit. The TS_SYNC_SEL value must be written to zero before changing to a different non-zero value. No events are generated due to the CPTS_SYNC operation. The CPTS_SYNC output is two CPTS_RFT_CLK periods after the actual count value.

12.2.1.4.7.11 Timestamp GENFn Output

The CPTS_GENFn outputs have a programmable cycle (frequency) with a PPM feature and software nudge feature. The CPTS_GENFn output cycle is CPSW_GENF0_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods (which is different than CPTS_COMP operation). Figure 12-123 represents the CPTS_GENFn output signal.

The CPTS_GENFn output cycle is CPSW_GENF0_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods beginning when the 64-bit TIME_STAMP value compares with the 64-bit GENFn_COMP value (CPSW_GENF0_COMP_LOW_REG_L and CPSW_GENF0_COMP_HIGH_REG_L registers) and the length value is non-zero. The CPTS_GENFn output cycle repeats thereafter every CPSW_GENF0_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods. The upper 32-bit word should be written first for 64-bit values. The length should be zero while the comparison value and other configuration parameters are being configured. The length should be written non-zero to enable operations last. The first cycle after comparison is active high when the CPSW_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit is low. No compare events and no CPTS_EVNT interrupts are generated.

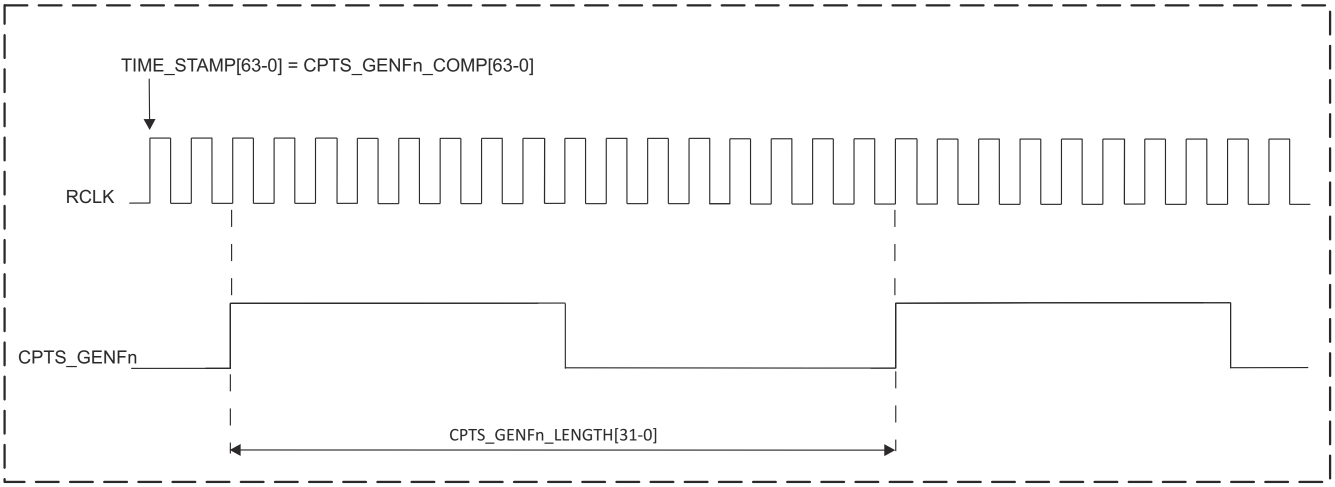

Figure 12-123. CPTS_GENFn Output Signal Diagram

12.2.1.4.7.11.1 GENFn Nudge

The cycle length can be adjusted by writing the CPSW_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE register value which is a two's complement value. A value of FFh will subtract 1 CPTS_RFT_CLK from the CPSW_GENF0_LENGTH_REG_L[31-0] value. A value of 1h will add 1 CPTS_RFT_CLK to the CPSW_GENF0_LENGTH_REG_L[31-0] value. The CPSW_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE value is cleared to zero when the nudge has occurred.

12.2.1.4.7.11.2 GENFn PPM

The CPTS_GENFn output cycle can be adjusted by parts per million or by parts per hour. Writing a non-zero value to CPSW_GENF0_PPM_LOW_REG_L/ CPSW_GENF0_PPM_HIGH_REG_L enables PPM operations. The PPM counter continually loads and decrements to zero and then loads again. A single CPTS_RFT_CLK adjustment is made when the PPM counter decrements to zero. The adjustment is up or down depending on the CPSW_GENF0_TS_GENF_CONTROL_REG[0] PPM_DIR bit. When PPM_DIR bit is set a single CPTS_RFT_CLK time is subtracted from the generate function counter which has the effect of increasing the generate function frequency by the PPM amount. When PPM_DIR bit is cleared a single CPTS_RFT_CLK time is added to the generate function counter which has the effect of decreasing the generate function frequency by the PPM amount.

Parts Per Million example:
To adjust for 100 parts per million the configured value for GENF_PPM[41-0] (through CPSW_GENF0_PPM_LOW_REG_L and CPSW_GENF0_PPM_HIGH_REG_L) is:
1,000,000/100 = 10,000(decimal)

Parts Per Hour example:
To adjust for 1 part per hour at 1 GHz CPTS_RFT_CLK the configured value for GENF_PPM[41-0] (through CPSW_GENF0_PPM_LOW_REG_L and CPSW_GENF0_PPM_HIGH_REG_L) is:
(1,000,0000,000Hz/1pph) * (3600 seconds/hour) = 34630B8A000 (hex)

12.2.1.4.7.12 Timestamp ESTFn

Each Ethernet port has a dedicated ESTFn generator which operates identically to the GENFn function.

12.2.1.4.7.13 Time Sync Events

Time Sync events are 96-bit values that are pushed onto the event FIFO and read by software in 32-bit reads. Four 32-bit registers, CPSW_CPTS_EVENT_0_REG through CPSW_CPTS_EVENT_3_REG hold the data of a time sync event. There are eight types of sync events:

- Time Stamp Push Event

- Time Stamp Counter Rollover Event (32-bit mode only)
- Time Stamp Counter Half-rollover Event (32-bit mode only)
- Hardware Time Stamp Push Event
- Ethernet Receive Event
- Ethernet Transmit Event
- Time Stamp Compare Event
- Host Transmit Event

12.2.1.4.7.13.1 Time Stamp Push Event

Software can obtain the current time stamp value (at the time of the write) by initiating a time stamp push event. The push event is initiated by setting the [0]TS_PUSH bit of the CPSW_CPTS_TS_PUSH_REG register. The time stamp value is returned in the event, along with a time stamp push event code. The upper 32-bits (CPSW_CPTS_EVENT_3_REG register) of the timestamp are zero in 32-bit mode.

12.2.1.4.7.13.2 Time Stamp Counter Rollover Event (32-bit mode only)

The CPTS module contains a 32-bit time stamp value (CPSW_CPTS_EVENT_0_REG). The counter upper bits are maintained by host software. The rollover event indicates to software that the time stamp counter has rolled over from 0xFFFF FFFF to 0x0000 0000 and the software-maintained upper count value should be incremented. This event occurs only in 32-bit mode.

12.2.1.4.7.13.3 Time Stamp Counter Half-rollover Event (32-bit mode only)

The CPTS includes a time stamp counter half-rollover event. The half-rollover event indicates to software that the time stamp value (CPSW_CPTS_EVENT_0_REG[31-0] TIME_STAMP) has incremented from 0x7FFF FFFF to 0x8000 0000. The half-rollover event is included to enable software to correct a misaligned event condition. This event occurs only in 32-bit mode.

The half-rollover event is included to enable software to determine the correct time for each event that contains a valid time stamp value, such as an Ethernet event. If an Ethernet event occurs around a counter rollover (full rollover), the rollover event could possibly be loaded into the event FIFO before the Ethernet event, even though the Ethernet event time was actually taken before the rollover. Figure 12-124 shows a misalignment condition. This misaligned event condition arises because an Ethernet event time stamp occurs at the beginning of a packet and time passes before the packet is determined to be a valid synchronization packet. The misaligned event condition occurs if the rollover occurs in the middle, after the packet time stamp has been taken, but before the packet has been determined to be a valid time sync packet.

Host software must detect and correct for misaligned event conditions. For every event time stamp after a rollover and before a half-rollover, software must examine the time stamp most significant bit. If bit 31 of the time stamp value is low (0x0000 0000 through 0x7FFF FFFF), then the event time stamp was taken after the rollover and no correction is required. If the value is high (0x8000 0000 through 0xFFFF FFFF), the time stamp value was taken before the rollover and a misalignment is detected. The misaligned case indicates to software that it must subtract one from the upper count value stored in software to calculate the correct time for the misaligned event. The misaligned event occurs only on the rollover boundary and not on the half-rollover boundary. Software only needs to check for misalignment from a rollover event to a half-rollover event.

When a rollover occurs, software increments the software time stamp upper value. The misaligned case indicates to software that the misaligned event time stamp has a valid upper value that is pre-increment, so one must be subtracted from the upper value to allow software to calculate the correct time for the misaligned event.

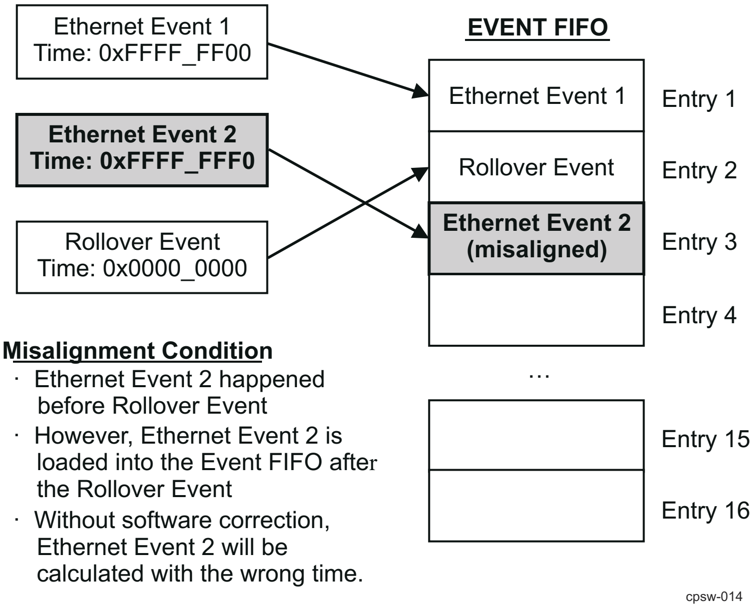

Figure 12-124. Event FIFO Misalignment Condition

12.2.1.4.7.13.4 Hardware Time Stamp Push Event

There are four hardware time stamp inputs (CPTS_HW[1:4]_TS_PUSH events) that can cause hardware time stamp push events to be loaded into the Event FIFO. Each time stamp input is mapped in the device as shown in *CPSW0 CPTS Integration*. The event is loaded into the event FIFO on the rising edge of the timer, and the PORT_NUMBER field in the CPSW_CPTS_EVENT_1_REG register indicates the hardware push input that caused the event (encoded).

The hardware time stamp inputs are asynchronous and are low frequency signals. The CPTS logic synchronizes and performs a rising edge detect on the incoming asynchronous input.

Each hardware time stamp input must be asserted for at least 10 periods of the selected CPTS_RFT_CLK clock. Each input can be enabled or disabled by setting the respective bits in the CPSW_CPTS_CONTROL_REG register.

Hardware time stamps are intended to be an extremely low frequency signals, such that the event FIFO does not overrun. Software must keep up with the event FIFO and ensure that there is no overrun, or events will be lost.

12.2.1.4.7.13.5 Ethernet Port Events

Packets transmitted or received on each Ethernet port can generate Ethernet Transmit Events or Ethernet Receive Events, respectively. The CPTS hardware will decode each packet to determine if it is a valid CPTS time sync event.

According to the IEEE 802.3 Ethernet standard, each Ethernet frame contains a 2-octet EtherType field to indicate which protocol is encapsulated in the PayLoad field, as shown in Figure 12-125. For standard time sync packets, this will contain the EtherType for the Precision Time Protocol (IEEE 1588), which is defined as 0x88F7. The CPTS hardware will compare this field to the TS_LTYPE1 field in the CPSW_PN_TS_SEQ_LTYPE_REG or the TS_LTYPE2 field in CPSW_PN_TS_CTL_LTYPE2_REG register (depending on which enable bit was set) , which should also be programmed to 88F7h.

When a virtual LAN is used, an additional 4-octet 802.1Q tag is inserted in the Ethernet frame before the EtherType field, as shown in Figure 12-125. To indicate to the CPTS hardware that a virtual LAN is in use, the TS_TX_VLAN_LTYPE1_EN (or TS_TX_VLAN_LTYPE2_EN) enable bit must be set in the

CPSW_PN_TS_CTL_REG register. The EtherType for the 802.1Q tag is defined as 0x8100, and the CPTS hardware will compare this value to the TS_VLAN_LTYPE1 (or TS_VLAN_LTYPE2 depending on which enable bit was set) field in the CPSW_PN_TS_VLAN_LTYPE_REG register, which should also be programmed to 0x8100.

When two stacked VLANs are used, two additional 4-octet 801.Q tags are inserted in the Ethernet frame before the EtherType field, as shown in Figure 12-125. In this case, both TS_VLAN_LTYPE1 and TS_VLAN_LTYPE2 must be enabled. The outer tag must match the value of the TS_VLAN_LTYPE1 field, and the inner tag must match the value of the TS_VLAN_LTYPE2 field.

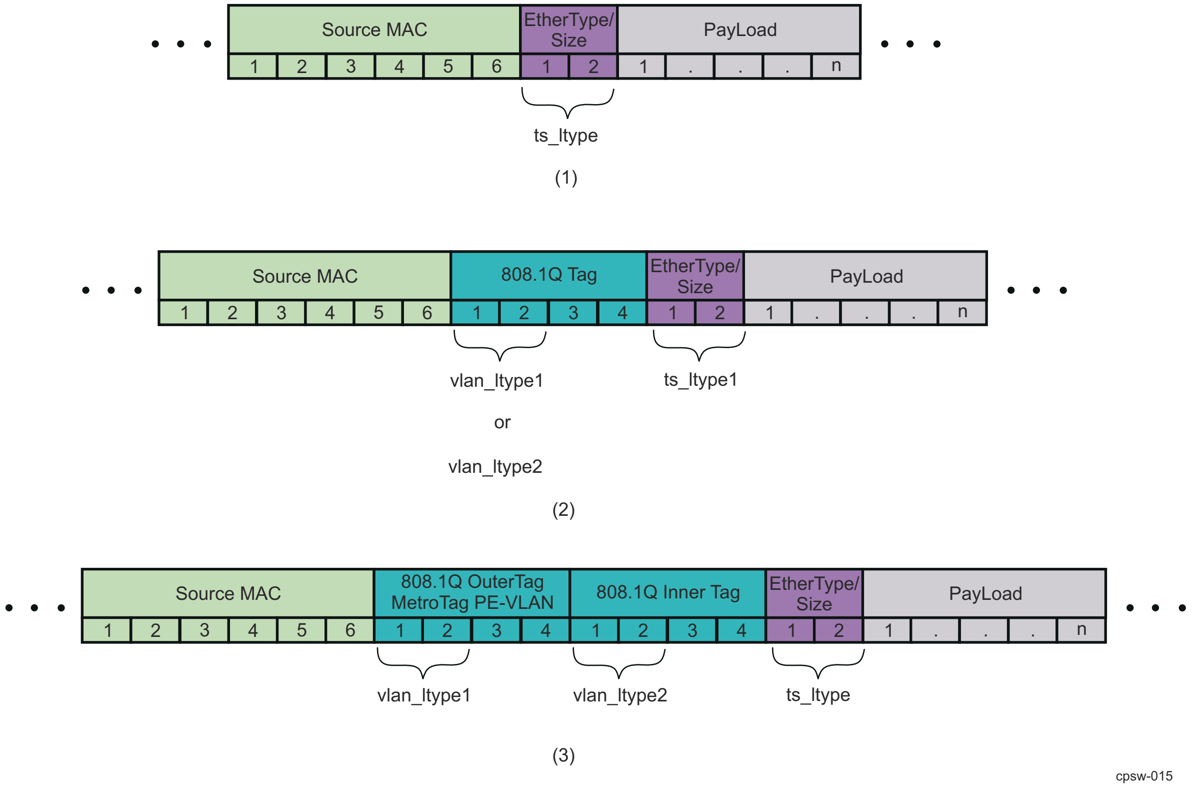

Figure 12-125. Partial Ethernet-II Frames Showing Register Mapping of EtherTypes for a Simple Frame (1), a Single 1Q Tag Added (2), and Two 1Q Tags Added (3)

12.2.1.4.7.13.5.1 Ethernet Port Receive Event

This section describes Ethernet port receive events. Ethernet port generates time synchronization events for valid received time sync packets. For every packet received on the Ethernet port, a timestamp will be captured by the receive module inside the CPTS for the corresponding port. The time stamp will be captured by the receive module regardless of whether or not the packet is a time synchronization packet to make sure that the time stamp is captured as soon as possible. The packet is sampled on both the rising and falling edges of the CPTS_RFT_CLK, and the time stamp will be captured once the start of frame delimiter for the receive packet is detected.

After the time stamp has been captured, the receive interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The CPSW decoder determines if the packet is a valid Ethernet receive time synchronization event. The receive interface for the port will use the following criteria to determine if the packet is a valid Annex D, Annex E, or Annex F time synchronization Ethernet receive event:

Annex D (IPv4)

1. Receive annex D time sync is enabled (TS_RX_ANNEX_D_EN is set in the CPSW_PN_TS_CTL_REG register).

2. One of the sequences below is true.
   1. The first packet LTYPE matches 0x0800
   2. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   3. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   4. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the third packet LTYPE matches 0x0800
3. Byte 14 (the byte after the LTYPE) contains 0x45 (IPv4).

Note

The byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes.

---

4. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)
5. Byte 22 contains 0x01 (HOP Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 22 contains any value if CPSW_PN_TS_CTL_LTYPE2_REG is set to 1h. Byte 22 is the TTL/HOP field.
6. Byte 23 contains 0x11 (Next Header UDP Fixed).
7. The TS_UNI_EN bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is cleared to 0h and Bytes 30 through 33 contain:
   1. Decimal 224.0.1.129 and the TS_129 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   2. Decimal 224.0.1.130 and the TS_130 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   3. Decimal 224.0.1.131 and the TS_131 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   4. Decimal 224.0.1.132 and the TS_132 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   5. Decimal 224.0.0.107 and the TS_107 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set

   -OR-

   The TS_UNI_EN bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set and Bytes 30 through 33 contain any values.
8. Bytes 36 and 37 contain:
   1. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set -OR-
   2. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set.
9. The PTP message begins in byte 42.
10. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW_PN_TS_CTL_REG register.
11. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

Annex E (IPv6)

1. Receive annex E time sync is enabled (TS_RX_ANNEX_E_EN bit is set in the switch CPSW_PN_TS_CTL_REG register).
2. One of the sequences below is true.
   1. The first packet LTYPE matches 0x86dd.

   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the third packet LTYPE matches 0x86dd

3. Byte 14 (the byte after the LTYPE) contains 0x6X (IPv6).
4. Byte 20 contains 0x11 (UDP Fixed Next Header).
5. Byte 21 contains 0x01 (Hop Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 21 contains any value if TS_TTL_NONZERO is set to 1h. Byte 21 is the TTL/HOP field.
6. The TS_UNI_EN bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is cleared to 0 and Bytes 38 through 53 contain:
   a. FF0M:0:0:0:0:0:0:0181 and the TS_129 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   b. FF0M:0:0:0:0:0:0:0182 and the TS_130 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   c. FF0M:0:0:0:0:0:0:0183 and the TS_131 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   d. FF0M:0:0:0:0:0:0:0184 and the TS_132 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   e. FF0M:0:0:0:0:0:0:006B and the TS_107 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set

   Note

   All values above are 16-bit hex numbers where M is enabled in the TS_MCAST_TYPE_EN field in the CPSW_PN_TS_CTL2_REG register.

   -OR-

   The TS_UNI_EN bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set to 1h and Bytes 38 through 53 contain any value.

7. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):
   a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW_PN_TS_CTL2_REG register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW_PN_TS_CTL2_REG register is set.
8. The PTP message begins in byte 62.
9. The packet message type is enabled in the MSG_TYPE_EN field in the CPSW_PN_TS_CTL2_REG register.
10. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

Annex F (IEEE 802.3)

1. Receive Annex F time sync is enabled (TS_RX_ANNEX_F_EN is set in the switch CPSW_PN_TS_CTL_REG register).
2. One of the sequences below is true:
   a. The first packet LTYPE matches TS_LTYPE1 in the CPSW_PN_TS_SEQ_LTYPE_REG/ CPSW_PN_TS_SEQ_LTYPE_REG register. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.
   b. The first packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register and LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register.

   c. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW_PN_TS_SEQ_LTYPE_REG register
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register.
   e. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW_PN_TS_SEQ_LTYPE_REG register.
   f. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register.
   g. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE1 in the CPSW_PN_TS_SEQ_LTYPE_REG register.
   h. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register

3. The PTP message begins in the byte after the LTYPE.
4. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW_PN_TS_CTL_REG register.
5. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

If all of the criteria described above are met for either Annex D, Annex E, or Annex F, and the packet is determined to be a valid time synchronization packet, then the RX interface will push an Ethernet receive event into the event FIFO.

12.2.1.4.7.13.5.2 Ethernet Port Transmit Event

This section describes Ethernet port transmit events. For every packet transmitted on the Ethernet ports, the port transmit interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The CPTS transmit interface for the port will use to the following criteria to determine if the packet is a valid time synchronization Ethernet transmit event. The CPSW decoder determines if the packet is a valid ethernet receive time synchronization event. To be a valid Ethernet transmit time synchronization event, the conditions listed below must be true for either Annex D, Annex E, or Annex F:

Annex D (IPv4)

1. Transmit time sync is enabled (TS_TX_ANNEX_D_EN is set in the CPSW_PN_TS_CTL_REG register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x0800
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second

packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the third packet LTYPE matches 0x0800

3. Byte 14 (the byte after the LTYPE) contains 0x45 (IPv4).

Note

The byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes.

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4. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)
5. Byte 22 contains 0x01 (HOP Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 22 contains any value if TS_TTL_NONZERO is set to 1h. Byte 22 is the TTL/HOP field.
6. Byte 23 contains 0x11 (Next Header UDP Fixed).
7. The TS_UNI_EN bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is cleared to 0h and Bytes 30 through 33 contain:
   a. Decimal 224.0.1.129 and the TS_129 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 224.0.1.130 and the TS_130 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   c. Decimal 224.0.1.131 and the TS_131 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   d. Decimal 224.0.1.132 and the TS_132 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   e. Decimal 224.0.0.107 and the TS_107 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   f. The TS_UNI_EN bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set and Bytes 30 through 33 contain any values.
8. Bytes 36 and 37 contain:
   a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set.
9. The PTP message begins in byte 42.
10. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW_PN_TS_CTL_REG register.
11. The packet was sent by host port 0.

Annex E (IPv6)

1. Transmit annex E time sync is enabled (TS_TX_ANNEX_E_EN bit is set in the switch CPSW_PN_TS_CTL_REG register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x86dd.
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the third packet LTYPE matches 0x86dd
3. Byte 14 (the byte after the LTYPE) contains 0x6X (IPv6).
4. Byte 20 contains 0x11 (UDP Fixed Next Header).

5. Byte 21 contains 0x01 (Hop Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 21 contains any value if TS_TTL_NONZERO is set to 1h. Byte 21 is the TTL/HOP field..
6. The TS_UNI_EN bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is cleared to 0 and Bytes 38 through 53 contain:
   a. FF0M:0:0:0:0:0:0:0181 and the TS_129 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   b. FF0M:0:0:0:0:0:0:0182 and the TS_130 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   c. FF0M:0:0:0:0:0:0:0183 and the TS_131 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   d. FF0M:0:0:0:0:0:0:0184 and the TS_132 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   e. FF0M:0:0:0:0:0:0:006B and the TS_107 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set

   Note

   All values above are 16-bit hex numbers where M is enabled in the TS_MCAST_TYPE_EN field in the CPSW_PN_TS_CTL2_REG register.

   -OR-

   The TS_UNI_EN bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set to 1h and Bytes 38 through 53 contain any value.
7. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):
   a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW_PN_TS_CTL_LTYPE2_REG register is set.
8. The PTP message begins in byte 62.
9. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW_PN_TS_CTL_REG register.
10. The packet was sent by host port 0.

Annex F (IEEE 802.3)

1. Transmit time sync is enabled (TS_TX_ANNEX_F_EN is set in the switch CPSW_PN_TS_CTL_REG register).
2. One of the sequences below is true:
   a. The first packet LTYPE matches TS_LTYPE1 in the CPSW_PN_TS_SEQ_LTYPE_REG register. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.
   b. The first packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register.
   c. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register.
   d. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW_PN_TS_SEQ_LTYPE_REG register.
   e. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register.
   f. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register.
   g. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second

packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register.

   h. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW_PN_TS_CTL_REG register

3. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW_PN_TS_CTL_REG register.
4. The packet was sent by host port 0.

If all of the criteria described above are met, and the packet is determined to be a valid time synchronization packet, then the time stamp for the transmit event will not be generated until the start of frame delimiter of the packet is actually transmitted. The start of frame delimiter will be sampled on every rising and falling edge of the CPTS_RFT_CLK. Once the packet is transmitted, then the TX interface will push an Ethernet transmit event into the event FIFO.

Table 12-182. Values of Message Type Field

Message Type	Value (hex)
Sync	0
Delay_Req	1
Pdelay_Req	2
Pdelay_Resp	3
Reserved	4:7
Follow_Up	8
Delay_Resp	9
Pdelay_Resp_Follow_Up	A
Announce	B
Signaling	C
Management	D
Reserved	E:F

Once a transmitted or received packet is determined to be a valid time sync packet, the Ethernet Transmit Event or Ethernet Receive Event is loaded onto the Event FIFO.

The CPSW_CPTS_EVENT_1_REG register contains the Message Type and Sequence ID values from the original time sync packet. The CPSW_CPTS_EVENT_0_REG (and CPSW_CPTS_EVENT_3_REG) register contains the time stamp value when the packet arrived at the corresponding port.

Table 12-183. Values of Message Type Field

Message Type	Value (hex)
Sync	0
Delay_Req	1
Pdelay_Req	2
Pdelay_Resp	3
Reserved	4:7
Follow_Up	8
Delay_Resp	9
Pdelay_Resp_Follow_Up	A
Announce	B

Table 12-183. Values of Message Type Field (continued)

Message Type	Value (hex)
Signaling	C
Management	D
Reserved	E:F

Once a transmitted or received packet is determined to be a valid time sync packet, the Ethernet Transmit Event or Ethernet Receive Event is loaded onto the Event FIFO.

The CPSW_CPTS_EVENT_1_REG register contains the Message Type and Sequence ID values from the original time sync packet. The CPSW_CPTS_EVENT_0_REG (and CPSW_CPTS_EVENT_3_REG) register contains the time stamp value when the packet arrived at the corresponding port.

12.2.1.4.7.13.5.3

Table 12-184. Values of Message Type Field

Message Type	Value (hex)
Sync	0
Delay_Req	1
Pdelay_Req	2
Pdelay_Resp	3
Reserved	4:7
Follow_Up	8
Delay_Resp	9
Pdelay_Resp_Follow_Up	A
Announce	B
Signaling	C
Management	D
Reserved	E:F

Once a transmitted or received packet is determined to be a valid time sync packet, the Ethernet Transmit Event or Ethernet Receive Event is loaded onto the Event FIFO.

The CPSW_CPTS_EVENT_1_REG register contains the Message Type and Sequence ID values from the original time sync packet. The CPSW_CPTS_EVENT_0_REG (and CPSW_CPTS_EVENT_3_REG) register contains the time stamp value when the packet arrived at the corresponding port.

12.2.1.4.7.14 Timestamp Compare Event

Note

Timestamp compare events are generated for non-toggle mode only.

The CPTS can generate an event for a time stamp comparison in 32-bit or 64-bit mode.

12.2.1.4.7.14.1 32-Bit Mode

The CPTS_COMP output is also asserted when the event is generated. The event is generated when the 32-bit time stamp value (CPSW_CPTS_EVENT_0_REG) compares with the CPSW_CPTS_TS_COMP_VAL_REG register and the CPSW_CPTS_TS_COMP_LEN_REG value is non-zero. The CPSW_CPTS_TS_COMP_LEN_REG value should be written by software after the CPSW_CPTS_TS_COMP_VAL_REG register is written and should be zero when the comparison value is written.

12.2.1.4.7.14.2 64-Bit Mode

The CPTS_COMP output is also asserted when the event is generated. The event is generated when the 64-bit time stamp value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG) compares with the CPSW_CPTS_TS_COMP_VAL_REG and CPSW_CPTS_TS_COMP_HIGH_VAL_REG registers and the CPSW_CPTS_TS_COMP_LEN_REG value is non-zero. The CPSW_CPTS_TS_COMP_LEN_REG value should be written by software after the CPSW_CPTS_TS_COMP_VAL_REG register is written and should be zero when the comparison value is written.

12.2.1.4.7.15 Host Transmit Event

The host can send a packet to be transmitted on an Ethernet port that will generate a time synchronization event. The host sets the TSTAMP_EN bit and sends the DOMAIN, MESSAGE_TYPE, and SEQUENCE_ID in the additional control information that resides in the protocol specific section of the descriptor that is transmitted to the CPSW_3G. An event is then generated and placed on the event FIFO once the packet is transmitted. Host events allow the user to timestamp exactly when a software generated packet exits the device.

12.2.1.4.7.16 CPTS Interrupt Handling

When an event is push onto the Event FIFO, an interrupt can be generated to indicate to software that a time sync event occurred. The following steps should be taken to process time sync events using interrupts:

1. Enable the TS_PEND interrupt by setting the TS_PEND_EN bit of the CPSW_CPTS_INT_ENABLE_REG register.
2. Upon interrupt, read the CPSW_CPTS_EVENT_0_REG through CPSW_CPTS_EVENT_3_REG registers values.
3. Set the CPSW_CPTS_EVENT_POP_REG[0] EVENT_POP bit to 1h to pop the previously read value off of the event FIFO.
4. Process the interrupt as required by the application software.

Software has the option of processing more than a single event from the event FIFO in the interrupt service routine in the following way:

1. Enable the TS_PEND interrupt by setting the TS_PEND_EN bit of the CPSW_CPTS_INT_ENABLE_REG
2. Upon interrupt, enter the CPTS service routine.
3. Read the CPSW_CPTS_EVENT_0_REG through CPSW_CPTS_EVENT_3_REG registers values.
4. Set the CPSW_CPTS_EVENT_POP_REG[0] EVENT_POP bit to 1h to pop the previously read value off of the event FIFO.
5. Wait for an amount of time greater than four CPTS_RFT_CLK periods plus four CPPI_ICLK periods.
6. Read the TS_PEND_RAW bit in the CPSW_CPTS_INTSTAT_RAW_REG register to determine if another valid event is in the event FIFO. If bit TS_PEND_RAW is asserted, go to step 3. If bit TS_PEND_RAW is not asserted proceed with step 7.
7. Process the interrupt(s) as required by the application software.

Software also has the option of disabling the interrupt and polling the TS_PEND_RAW bit of the CPSW_CPTS_INTSTAT_RAW_REG register to determine if a valid event is on the event FIFO.

12.2.1.4.8 CPPI Streaming Packet Interface

The receive streaming interface on port 0 of the CPSW is responsible for receiving packet for Ethernet egress data from the packet streaming switch in the DMSS. The CPPI receive port is equivalent to an Ethernet port with the difference being that the data is provided to the CPSW in the 128-bit streaming interface data format instead RGMII data format.

In addition to the packet data, the receive streaming interface also can provide additional control information that resides in the information words of the descriptor that was transmitted to the CPSW.

The tables below show the information that may be passed along with which descriptor information word to put it in.

12.2.1.4.8.1 Port 0 CPPI Transmit Packet Streaming Interface (CPSW_3G Egress)

The CPSW3G has a single transmit packet streaming interface. All Ethernet packet data destined for the host (Port 0) is transferred on the transmit packet streaming interface. The transmit packet streaming interface is equivalent to an Ethernet MAC output with the difference being that 128-bit streaming interface data is output. Egress packet data is packed on the 128-bit data bus with all words having 16-bytes except possibly the last packet data word which is the word previous to the EOP word. INFO Word 0–3 is transferred on SOP. The EOP word contains the packet status 0–3 (data type 24) which includes the timestamp and checksum data. Packets are not dropped on the transmit streaming interface due to pushback, but packets may be dropped in the associated priority FIFO.

INFO Word 0–3 and Status Data Word 0–3 (on EOP) are the only non-payload data word types that are transferred. Long packets are truncated at the CPSW_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN byte value of the ingress port (only the CPSW_PN_RX_MAXLEN_REG_k number of bytes are kept if long packets are transferred due to CPSW_PN_MAC_CONTROL_REG_k register copy error frames set - RX_CEF_EN). MAC control frames are only transferred if the receiving Ethernet port has the CPSW_PN_MAC_CONTROL_REG_k[24] RX_CMF_EN bit set.

The error encoding on the TXST_PKT_ERR[3:0] output is shown in Table 12-185:

Table 12-185. Error Encoding on the TXST_PKT_ERR[3:0] Output

TXST_PKT_ERR[3:0]	Description
0000	No Error
0001	CRC Error
0010	Code or alignment error
0011	Short (no code/align/crc error)
0100	FragCRC (short with crc error)
0101	Frag Code/Align (short with code/align error)
0110	Long
0111	Jabber CRC (long with crc error)
1000	Jabber Code/Align (long with code/align error)
1001	Mac ontrol packet (CPSW_PN_MAC_CONTROL_REG_k[24] RX_CMF_EN set on ingress Ethernet port)
1010	Mac control CRC
1011	Mac control Code/Align
1100	Mac control short/frag (short MAC control frame with CRC/Code/Align)
1101	Mac control long/jabber (long MAC control frame with CRC/Code/Align)
1110	Reserved
1111	Reserved

The CPPI Port 0 transmit packet streaming interface has a single output thread. If a packet transmission has begun then the entire packet will be transmitted before the next packet is sent (packet data from multiple packets are not interleaved on the transmit streaming interface). The default egress flow is the port number minus 1, concatenated with the 3-bit Port 0 transmit FIFO hardware switch priority. For example, a packet that was received on port 4 with a Port 0 transmit FIFO hardware switch priority of 5 would be sent on flow 29 (decimal) or flow 0b0011101 (binary). Priority remapping on ingress and Port 0 transmit egress effects the output flow.

INFO Words are a contiguous block of four 32-bit data words aligned on a 32-bit word boundary.

Figure 12-126. TX INFO Word 0 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PKT_TYPE					RESERVED			PASS_CRC	CRC_TYPE	RESERVED					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 12-126. TX INFO Word 0 Format (continued)

RESERVED	FLOW_ID

Bit	Field	Description
31-27	PKT_TYPE	Always set to 0b00111. Host PD (Packet Descriptor) Word 2. Packet Type: bits[31-27].
26-24	RESERVED	Reserved.
23	PASS_CRC	This bit is cleared to zero (no CRC passed) when the P0_TX_CRC_REMOVE bit in the CPSW_CONTROL_REG register is set (and the egress packet has no errors). When the remove bit is cleared to zero then this bit is cleared and no CRC is passed with the output packet. The packet length includes the CRC if it is present.
22	CRC_TYPE	The packet CRC type. The type of CRC passed is determined by CRC_TYPE field in the CPSW_PN_MAC_CONTROL_REG_k register (not by the type of CRC the packet had on Ethernet port ingress). Host PD Word 1. Protocol Specific Flags: bits[27-24]. 0h: Ethernet CRC 1h: Castagnoli CRC
21-8	RESERVED	Reserved.
7-0	FLOW_ID	This is the packet output transmit streaming interface flow. The default flow ID can be overridden by ALE classification (Thread mapping). The switch default flow is the 3-bit “From Port” value concatenated with the 3-bit “Switch Priority” {From_Port[2:0], Switch_Priority[2:0]} as shown below: Host PD (Packet Descriptor) Word 1. Flow ID: bits[13-0]. 0h: The packet was received on Ethernet port 1 Switch Priority – The actual hardware switch priority that the packet was stored in on the CPPI transmit FIFO.

Figure 12-127. TX INFO Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x4 (fixed_ps_size)												0			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		PKT_LENGTH													

Bit	Field	Description
31-20	FIXED_PS_SIZE	Fixed packet size: 0x4
19-14	RESERVED	Reserved.

Bit	Field	Description
13-0 (Host PD (Packet Descriptor) Word 1. Packet Length: bits[21-0])	PKT_LENGTH	Specifies the number of bytes in the entire packet. Offset bytes are not included. Valid only on SOP. The packet length must be greater than zero. The packet data will be truncated to the packet length if the packet length is shorter than the sum of the packet buffer descriptor buffer lengths. A host error occurs if the packet length is greater than the sum of the packet buffer descriptor buffer lengths.

Figure 12-128. TX INFO Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xFFFF															

Figure 12-129. TX INFO Word 3 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SRC_ID							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															

Bit	Field	Description
31-24	RESERVED	Reserved.
23-16	SRC_ID	The packet SRC_ID value comes from the PORT1/PORT2 field in the CPSW_P0_SRC_ID_A_REG register. (src_tag) PD (Packet Descriptor) Word 3. Source Tag Low bits[23-16] if RFLOW[a]_RFC.rx_src_tag_lo_sel = 0x4 or (src_tag) PD (Packet Descriptor) Word 3. Source Tag High bits[31-24] if RFLOW[a]_RFC.rx_src_tag_hi_sel = 0x4
15-0	RESERVED	Reserved.

Note

TX Status Data Word [0..3] are mapped to Host Packet Descriptor Protocol Specific Words if RFLOW[a]_RFA.rx_psinfo_present = 1 and RFLOW[a]_RFA.rx_ps_location = 0

Figure 12-130. TX Status Data Word 0 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMESTAMP[31:0]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP[31:0]															

Bit	Field	Description
31-0	TIMESTAMP[31:0]	Contains the lower 32-bits of the time stamp value.

Figure 12-131. TX Status Data Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Figure 12-131. TX Status Data Word 1 Format (continued)

TIMESTAMP[63:32]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP[63:32]															

Bit	Field	Description
31-0	TIMESTAMP[63:32]	Contains the upper 32-bits of the time stamp value.

Figure 12-132. TX Status Data Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											IPV4_VALID	IPV6_VALID	TCP_UDP_N	FRAGMENT	CHECKSUM_ERROR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHECKSUM_ADD															

Bit	Field	Description
31-21	RESERVED	Reserved.
20	IPV4_VALID	An IPV4 TCP or UDP Packet was detected.
19	IPV6_VALID	An IPV6 TCP or UDP Packet was detected.
18	TCP_UDP_N	Valid only when either the IPV4_VALID or IPV6_VALID bits are set. 0h: Indicates UDP packet was detected. 1h: Indicates TCP packet was detected.
17	FRAGMENT	Indicates that an IP fragment was detected. Valid only when when either the IPV4_VALID or IPV6_VALID bits are set.
16	CHECKSUM_ERROR	Valid only when either the IPV4_VALID or IPV6_VALID bits are set.
15-0	CHECKSUM_ADD	This is the value that was summed during the checksum computation. This value is FFFFh for IPV4/6 UDP/TCP packets with no checksum error.

Figure 12-133. TX Status Data Word 3 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															

Bit	Field	Description
31-0	RESERVED	Reserved.

12.2.1.4.8.2 Port 0 CPPI Receive Packet Streaming Interface (CPSW_3G Ingress)

Info Word 0/1/2/3 (INFO1 and INFO3 are ignored) are transferred on SOP. If a timestamp word (Extended Packet Info Word 0/1/2/3) is to be transferred it must be after SOP and before any packet data is transferred. Any following non-data type words will be dropped. The EOP word must be payload data.

Input receive packets cannot be aborted by the host. The INFO Word bit descriptions and Extended Packet INFO Word bit descriptions are shown below. The PASS_CRC bit indicates that the CRC is passed with the packet data. Packets that have a passed CRC that is an error CRC will be output on the Ethernet port with at least one CRC byte inverted to indicate the error if P0_RX_PASS_CRC_ERR bit is set, otherwise they are dropped. The packet is a directed packet when any of the TO_PORT bits are nonzero. A packet may be directed only to a single port. The packet will be sent to the port number indicated. For directed packets the lookup process is skipped to determine the destination. However, in vlan aware mode (when VLAN_AWARE bit in the CPSW_CONTROL_REG register is set to 1h) the lookup is performed to determine untagged egress. Packets longer then the value in CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bit field are dropped. Packets shorter than 60-Bytes are padded to 64-Bytes (after adding pad and CRC) if P0_RX_PAD bit in the CPSW_CONTROL_REG register is set and if PASS_CRC is clear, otherwise they are dropped. This means that packets shorter than 64-Bytes are dropped if the PASS_CRC info bit is set regardless of P0_RX_PAD bit (packets are padded only if they are short and do not have CRC).

A RX INFO word is a contiguous block of four 32-bit data words aligned on a 32-bit word boundary.

Note

RX Control Data Words [0..2] are mapped to Host Packet Descriptor Protocol Specific Words if (TCHAN[a]_TCFG.tx_filt_pswords = 0) and (Host PD Word 1.Protocol Specific Region Location.bit[28] = 0h) and (Host PD Word 1.Protocol Specific Valid Word Count.bits[22-27] = 4h)

Figure 12-134. RX INFO Word 0 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PASS_CRC	CRC_TYPE	RESERVED					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															

Bit	Field	Description
31-24	RESERVED	Reserved.
23	PASS_CRC	The PASS_CRC bit indicates that the CRC is passed with the packet data. 0h: CRC is not passed with packet (CRC_TYPE is don't care) 1h: CRC of type CRC_TYPE is passed with the packet.
22 (Host PD (Packet Descriptor) Word 1. Protocol Specific Flags: bits[27-24])	CRC_TYPE	CRC Type 0h: Ethernet CRC 1h: Castagnoli CRC
21-0	RESERVED	Reserved.

Figure 12-135. RX INFO Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											TO_PORT				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 12-135. RX INFO Word 2 Format (continued)

RESERVED

Bit	Field	Description
31-21	RESERVED	Reserved.
20-16 (Host PD (Packet Descriptor) Word 3. Dest Tag Low bits[8-0])	TO_PORT	Port number to send the directed packet to. This field is set by the host. This field is valid on SOP. Directed packets go to the directed port, but an ALE lookup is performed to determine untagged egress in VLAN_AWARE mode. 0h: Not directed 1h: Send the packet to port 1. 2h: Send the packet to port 2.
15-0	RESERVED	Reserved.

Figure 12-136. RX Control Data Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMESTAMP_EN	RESERVED			DOMAIN								MSG_TYPE			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQUENCE_ID															

Bit	Field	Description
31	TIMESTAMP_EN	When set, this bit indicates that the packet will generate a timesync event on Ethernet egress (if the CPTS is configured properly) with the associated DOMAIN, MSG_TYPE, and SEQUENCE_ID.
30-28	RESERVED	Reserved.
27-20	DOMAIN	Timesync domain.
19-16	MSG_TYPE	Timesync message type.
15-0	SEQUENCE_ID	Timesync sequence ID.

Figure 12-137. RX Control Data Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHECKSUM_RESULT								CHECKSUM_START_BYTE							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHECKSUM_INV	RESERVED	CHECKSUM_BYTECOUNT													

Bit	Field	Description
31-24	CHECKSUM_RESULT	This is the packet byte number where the checksum result will be placed in the egress packet. The first packet byte which is the first byte of the destination address is Byte 1 (not byte zero).
23-16	CHECKSUM_START_BYTE	This is the packet byte number to start the checksum calculation on. The first packet byte is Byte 1.

Bit	Field	Description
15	CHECKSUM_INV	When set, a zero checksum value will be inverted and sent as FFFFh.
14	RESERVED	Reserved.
13-0	CHECKSUM_BYTECOUNT	This is the number of bytes to calculate the checksum on. The outgoing Ethernet packet will have a checksum inserted when this value is non-zero.

Other INFO words are not taken into account.

12.2.1.4.8.3 Cut-Thru

An Ethernet port received packet can be sent cut-thru to all destination ports when the following is true:

- The CPSW_CONTROL_REG[19] CUT_THRU_ENABLE bit is set, and
- The receive port is full duplex, and
- The Ethernet receive port speed is non-zero, and
- The packet was received on an express priority, and
- The Ethernet receive port has the remapped received packet priority enabled via the CPSW_PN_CUT_THRU_REG_k[15-8] RX_PRI_CUT_THRU_EN field, and
- All Ethernet destination ports have the remapped packet priority enabled via the CPSW_PN_CUT_THRU_REG_k[7-0] TX_PRI_CUT_THRU_EN field, and
- All Ethernet destination ports are full duplex, and
- All Ethernet destination ports are express priorities, and
- All Ethernet destination ports have a non-zero CPSW_PN_SPEED_REG_k[3-0] SPEED, and
- All Ethernet destination ports are equal to or slower in speed than the Ethernet receive port, and
- The host port is not in the destination port list unless the CPSW_P0_CONTROL_REG[19] CUT_MODE_ETH bit is set.

Whether or not a packet actually egresses cut-thru (with or without delay) on an Ethernet destination port depends on traffic congestion on that port. Cut-thru is compatible with Enhanced Scheduled Traffic (EST).

12.2.1.4.8.3.1 Host Port Cut-Thru Operations

Packets received (CPSW ingress) on the host port are sent store-and-forward to all Ethernet destination ports. Setting the CPSW_P0_CONTROL_REG[19] CUT_MODE_ETH bit enables Ethernet received packets to be sent cut-thru to a destination port mask that includes the host port. The packet can egress cut-thru on Ethernet ports, but the packet will not actually egress cut-thru on the host port. Setting CPSW_P0_CONTROL_REG[19] CUT_MODE_ETH can cause head of line blocking on the host priority if multiple Ethernet ports are sending to the same host port priority. The head of line blocking issue is worsened if there are differing Ethernet port speeds. Clearing the CPSW_P0_CONTROL_REG[19] CUT_MODE_ETH bit causes packets with the host port in the destination mask to egress store-and-forward on all egress ports.

12.2.1.4.8.3.2 Cut-Thru Error Packets

Any received packets with errors sent cut-thru from an Ethernet receive port to any Ethernet transmit port(s) will egress with at least one byte of the generated outgoing packet CRC inverted to indicate the error. This is due to the fact that cut-thru operations begin before the end of packet when the receive port determines that the packet had an error (long/code/align/CRC).

Any packet also sent cut-thru with the host included in the destination port mask will be dropped to the host (TXST_PKT_DROP) with the packet error indicated on TXST_PKT_ERR[3:0].

Any long/Jabber/Code/Align/CRC errored Ethernet received packet that is not actually sent cut-thru by the receive port will dropped unless CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is set (which if set will cause the packet to be sent to the host port with the error indicated on TXST_PKT_ERR[3:0]. If a long/Jabber/Code/Align/CRC errored Ethernet received packet is sent cut-thru by the received port then a set CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN will not cause the errored packet to be sent to the host port since the packet has already been transferred to the destination ports.

The following cut-thru notes are valid:

- Any Ethernet received packet and that is sent cut-thru to any destination port will not be dropped at any destination port due to priority maximum lengths (CPSW_TX_PRIx_MAXLEN).
- Any Ethernet received packet that is decoded as a timesync packet will be sent store-and-forward to all destination ports.
- Cut-Thru is full duplex only.
- Cut-Thru is not compatible with any form of flow control.
- Cut-Thru should not be enabled for any receive port that is in ALE bypass mode.

12.2.1.4.8.4 Port Speed

Cut-thru operations require that the Ethernet port speeds be known. Port speed can be set manually by software or be automatically determined by the hardware. A zero port speed causes the port to be disabled for cut-thru operations, but does not disable the port. The port speed values are as follows:

- 0000 – Port speed operations disabled (not a port disable)
- 0001 – 10Mpbs
- 0010 – 100Mbps
- 0011 – 1G
- 0100 – 2.5G
- 0101 – 5G
- 0110 – 10G
- 0111 through 1111 Reserved

When the CPSW_PN_SPEED_REG_k[8] AUTO_SPEED_EN bit is cleared, the port speed is written by software. When the CPSW_PN_SPEED_REG_k[8] AUTO_SPEED_EN bit is set, the port speed is automatically detected by the hardware.

12.2.1.4.8.5 CPPI Checksum Offload

The CPPI host port can be enabled to perform checksum offload on host port packet ingress and egress. UDP (User Datagram Protocol) and TCP (Transmission Control Protocol) over IPV4 and IPV6 are supported. For the purposes of checksum description, the first packet byte (the first byte of the destination address) is byte 1 (not byte 0). That is, a 64 byte packet goes from byte 1 to byte 64. For all packet types, the S_CN_SWITCH bit in the CPSW_CONTROL_REG register must be set for the Outer VLAN L type to be supported.

12.2.1.4.8.5.1 CPPI Transmit Checksum Offload

IPV4 and IPV6 UDP and TCP packets that are received on any Ethernet port and destined for port 0 egress are checked for correct checksum as described below. The byte counts below are shown for packets with no VLAN’s. The byte counts vary with one or two packet VLAN's. Packets received on an Ethernet port with errors are not checked for a correct checksum if they are passed to the host.

12.2.1.4.8.5.1.1 IPV4 UDP

- Byte 15 Upper Nibble = 4 for IPV4
- Byte 15 Lower Nibble = IHL - Nibble with number of 32-bit words in IPV4 header (5 to 15 supported).
- Bytes 20-21 = fragment[15-0] – Bit 13 is the MF bit and bits [12-0] are the Fragment offset. A packet is a fragment if the MF bit is set or if the fragment offset is non-zero. The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets have MF=0 and a zero offset. A count is output for packet fragments but no errors are reported. First fragments have the UDP header included in the count. Middle and last fragments have only data included in the count (there is no UDP header).
- Byte 24 = 0x11 for UDP protocol.
- Received packet UDP checksum of zero means that there is no IPV4 checksum sent with the packet so no error will be issued.
- Received packet UDP checksum of 0xFFFF means that the checksum was calculated to be 0xFFFF or 0x0000 but was sent in the transmitted packet as 0xFFFF by the sending originating entity.

12.2.1.4.8.5.1.2 IPV4 TCP

- Byte 15 Upper Nibble = 4 for IPV4
- Byte 15 Lower Nibble = IHL - Nibble with number of 32-bit words in IPV4 header (5 to 15 supported).
- Bytes 20-21 = fragment[15-0] – Bit 13 is the MF bit and bits [12-0] are the Fragment offset. A packet is a fragment if the MF bit is set or if the fragment offset is non-zero. The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets have MF=0 and a zero offset. A count is output for packet fragments but no errors are reported. First fragments have the UDP header included in the count. Middle and last fragments have only data included in the count (there is no TCP header).
- Byte 24 = 0x06 for TCP protocol.

12.2.1.4.8.5.1.3 IPV6 UDP

- Byte 15 upper nibble = 6 for IPV6.
- Byte 21 = 0x11 for UDP protocol as next header.
- Fragment extension headers are supported. First fragments have a fragment extension header (byte 21 = 0x2C) followed by a UDP header (byte 55 = 0x11). Middle and last fragments have a fragment extension header followed by data only (no UDP header). The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets do not have a fragment extension header. A count is output for packet fragments but no errors are reported.
- Received packet UDP checksum of zero means that there is no IPV6 checksum sent with the packet so no error will be issued.
- Received packet UDP checksum of 0xFFFF means that the checksum was calculated to be 0xFFFF or 0x0000 but was sent in the transmitted packet as 0xFFFF by the sending originating entity.

12.2.1.4.8.5.1.4 IPV6 TCP

- Byte 15 upper nibble = 6 for IPV6.
- Byte 21 = 0x06 for TCP protocol as next header.
- Fragment extension headers are supported. First fragments have a fragment extension header (byte 21 = 0x2C) followed by a UDP header (byte 55 = 0x06). Middle and last fragments have a fragment extension header followed by data only (no TCP header). The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets do not have a fragment extension header. A count is output for packet fragments but no errors are reported.

12.2.1.4.8.6 CPPI Receive Checksum Offload

Packets sent from host port 0 (switch ingress) to any Ethernet port can have a checksum calculated and inserted into the Ethernet egress packet. The RX_CHECKSUM_EN bit in the CPSW_P0_CONTROL_REG register must be set for receive checksum operation to be enabled. When bit RX_CHECKSUM_EN is enabled, Control Data Word 2 input on CPPI receive PSI interface determines how the checksum is calculated. The CHECKSUM_RESULT field in Control Data Word 2 determines where the checksum is inserted. The checksum result location is adjusted by the egress port if a VLAN is to be inserted or removed on Ethernet port egress.

12.2.1.4.8.7 Egress Packet Operations

Each CPSW egress port (Ethernet and Host) is capable of performing egress packet processing operations (CPSW_ALE_EGRESSOP). IntraVLAN processing either adds, removes, or replaces VLAN information or does nothing. InterVLAN routing allows hardware routing between a limited number of VLANs - thereby allowing high-bandwidth or other routing operations to be offloaded from software to the CPSW (hardware). IntraVLAN processing and InterVLAN routing operations are mutually exclusive. In addition, the packet source and destination addresses can be swapped on egress to facilitate OAM or generic testing operations.

12.2.1.4.9 MII Management Interface (MDIO)

The MII Management interface module implements the 802.3 serial management interface to interrogate and control external Ethernet PHY using a two-wire bus.

12.2.1.4.9.1 MDIO Frame Formats

Table 12-186 shows the address, Table 12-187 shows the read format and Table 12-188 shows the write format of the supported Clause 45 MII Management interface frames. Post-increment accesses are not supported.

Table 12-198. MDIO Clause 45 Address Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	00	AAAAA	RRRRR	10	AAAA.AAAA.AAAA.AAAA

Table 12-199. MDIO Clause 45 Read Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	11	AAAAA	RRRRR	Z0	DDDD.DDDD.DDDD.DDDD

Table 12-200. MDIO Clause 45 Write Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	01	AAAAA	RRRRR	10	DDDD.DDDD.DDDD.DDDD

The default or idle state of the two wire serial interface is a logic one. All tri-state drivers should be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic 1. Prior to initiating any other transaction, the station management entity shall send a preamble sequence of 32 contiguous logic 1 bits on the MDIO line with 32 corresponding cycles on MDCLK to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding MDCLK cycles before it responds to any other transaction. The MDIO CPSW_MDIO_USER_ADDR0_REG register must be written before a read or write operation is performed to set the address used in the operation. Each read or write operation has a preceeding address frame.

Preamble

The start of a frame is indicated by a preamble, which consists of a sequence of 32 contiguous bits all of which are a 1. This sequence provides the PHY a pattern to use to establish synchronization. The preamble is required in clause 45 operation.

Start Delimiter

The preamble is followed by the start delimiter which is indicated by a 00 pattern.

Operation Code

The operation code for an address transaction is 00. The operation code for a read is 11, while the operation code for a write is a 01.

PHY Address

The PHY address is 5 bits allowing 32 unique values. The first bit transmitted is the MSB of the PHY address.

MMD Number

The MMD number is the 5 bits allowing 32 unique values. The first bit transmitted is the MSB.

Turnaround

An idle bit time during which no device actively drives the MDIO signal shall be inserted between the register address field and the data field of a read frame in order to avoid contention. During a read frame, the PHY shall drive a zero bit onto MDIO for the first bit time following the idle bit and preceding the Data field. During a write frame, this field shall consist of a one bit followed by a zero bit.

Address

The address field is 16 bits on address operations. The first bit transmitted is the MSB of the address word. Each read/write operation initiated has an automatic address operation initiated first that uses the MDIO CPSW_MDIO_USER_ADDR0_REG/ CPSW_MDIO_USER_ADDR1_REG register values as the 16-bit address.

Data

The Data field is 16 bits on read and write operations. The first bit transmitted and received is the MSB of the data word.

12.2.1.4.9.2 MDIO Functional Description

The MII Management I/F will remain idle until enabled by setting the ENABLE bit in the CPSW_MDIO_CONTROL_REG register. The MII Management I/F will then continuously poll the link status from within the Generic Status Register of all possible 32 PHY addresses in turn recording the results in the MDIO CPSW_MDIO_LINK_REG register. Individual PHY's can be enabled or disabled for polling the associated bit in the CPSW_MDIO_POLL_EN_REG register. The CPSW_MDIO_LINK_REG and CPSW_MDIO_ALIVE_REG register bit values are updated on the poll of each PHY. The LINKSEL bit in the CPSW_MDIO_USER_PHY_SEL_REG_k register determines the status input that is used. A change in the link status of the two PHYs being monitored will set the appropriate bit in the MDIO CPSW_MDIO_LINK_INT_RAW_REG register and the MDIO CPSW_MDIO_LINK_INT_MASKED_REG register, if enabled by the LINKINT_ENABLE bit in the CPSW_MDIO_USER_PHY_SEL_REG_k register.

The MDIO CPSW_MDIO_ALIVE_REG register is updated by the MII Management I/F module if the PHY acknowledged the read of the generic status register. In addition, any PHY register read transactions initiated by the host also cause the MDIO CPSW_MDIO_ALIVE_REG register to be updated.

At any time, the host can define a transaction for the MII Management interface module to undertake using the DATA, PHYADR, REGADR, and WRITE fields in a CPSW_MDIO_USER_ACCESS_REG_k register. When the host sets the GO bit in this register, the MII Management interface module will begin the transaction without any further intervention from the host. Upon completion, the MII Management interface will clear the GO bit and set the USERINTRAW field in the CPSW_MDIO_USER_INT_RAW_REG register corresponding to the CPSW_MDIO_USER_ACCESS_REG_k register being used. The corresponding bit in the CPSW_MDIO_USER_INT_MASKED_REG register may also be set depending on the mask setting in the MDIO CPSW_MDIO_USER_INT_MASK_SET_REG and CPSW_MDIO_USER_INT_MASK_CLEAR_REG registers. A round-robin arbitration scheme is used to schedule transactions that may be queued by the host in different CPSW_MDIO_USER_ACCESS_REG_k registers. The host should check the status of the GO bit in the MDIO CPSW_MDIO_USER_ACCESS_REG_k register before initiating a new transaction to ensure that the previous transaction has completed. The host can use the ACK bit in the MDIO CPSW_MDIO_USER_ACCESS_REG_k register to determine the status of a read transaction.

It is necessary for software to use the MII Management interface module to setup the auto-negotiation parameters of each PHY attached to a MAC port, retrieve the negotiation results, and setup the CPSW_PN_MAC_CONTROL_REG register in the corresponding MAC.

12.2.1.5 CPSW0 Programming Guide

12.2.1.5.1 Initialization and Configuration of CPSW Subsystem

To configure the CPSW Ethernet Subsystem for operation, the host must perform the following:

1. Select the Interface (RMII, or RGMII) Mode. See the CTRLMMR_ENET1_CTRL and CTRLMMR_ENET2_CTRL[2-0] PORT_MODE_SEL fields.
2. Configure pads (pin muxing), as per the interface selected. Refer to *Pad Configuration Registers* and the device-specific Datasheet.
3. Enable the CPSW Ethernet Subsystem clocks. See *CPSW Integration*
4. Ensure that at least 2000 CPPI_ICLK periods are run after reset is de-asserted.

5. Configure the CPSW_CONTROL_REG register
6. Configure the Ethernet Port Source Address registers (CPSW_PN_SA_L_REG_k and CPSW_PN_SA_H_REG_k)
7. Configure the CPSW statistic port enable register CPSW_STAT_PORT_EN_REG
8. Configure the ALE (Section 12.2.1.4.6.1 , *Address Lookup Engine*)
9. Configure the MDIO (Section 12.2.1.5.3.1 , *Initializing the MDIO Module*)
10. Configure Ethernet port, as per the desired mode of operations

12.2.1.5.2 CPSW Reset

To reset the Ethernet port, the host must perform the following:

1. Set CMD_IDLE bit to 1h in the Ethernet port control register: CPSW_PN_MAC_CONTROL_REG.
2. Wait for IDLE bit to be set to 1h, which is indicated in the Ethernet port status register: CPSW_PN_MAC_STATUS_REG.
3. Set SOFT_RESET bit to 1h in the Ethernet port software reset register: CPSW_PN_MAC_SOFT_RESET_REG.
4. Wait for SOFT_RESET bit in the CPSW_PN_MAC_SOFT_RESET_REG registers to be cleared to confirm reset completion.
5. Configure the Ethernet ports.
6. Re-configure registers reset to default value by CPSW_PN_MAC_SOFT_RESET_REG.

12.2.1.5.3 MDIO Software Interface

12.2.1.5.3.1 Initializing the MDIO Module

The following steps are performed by the application software or device driver to initialize the MDIO device:

1. Configure the PREAMBLE and CLKDIV bits in the MDIO Control register (CPSW_MDIO_CONTROL_REG).
2. Enable the MDIO module by setting the ENABLE bit in CPSW_MDIO_CONTROL_REG.
3. The MDIO PHY alive status register (MDIO CPSW_MDIO_ALIVE_REG) can be read in polling fashion until a PHY connected to the system responded, and the MDIO PHY link status register (MDIO CPSW_MDIO_LINK_REG) can determine whether this PHY already has a link.
4. Set the appropriate PHY addresses in the MDIO user PHY select register (CPSW_MDIO_USER_PHY_SEL_REG_k, where k = 0 or 1), and set the LINKINT_ENABLE bit to enable a link change event interrupt if desirable.
5. Set the appropriate LINKSEL bit in the CPSW_MDIO_USER_PHY_SEL_REG_k register (where k = 0 or 1).
6. Set the appropriate USERINTMASKSET bit field in the CPSW_MDIO_USER_INT_MASK_SET_REG register.
7. If an interrupt on general MDIO register access is desired, set the corresponding bit in the MDIO user command complete interrupt mask set register (MDIO CPSW_MDIO_USER_INT_MASK_SET_REG) to use the MDIO user access register (MDIO CPSW_MDIO_USER_ACCESS_REG_k, where k = 0 or 1).

12.2.1.5.3.2 Writing Data To a PHY Register

The MDIO module includes a user access register (MDIO CPSW_MDIO_USER_ACCESS_REG_k, where k = 0 or 1) to directly access a specified PHY device.To write a PHY register, perform the following:

1. Check to ensure that the GO bit in the MDIO user access register (MDIO CPSW_MDIO_USER_ACCESS_REG_k) is cleared.
2. Write to the GO, WRITE, REGADR, PHYADR, and DATA bits in MDIO CPSW_MDIO_USER_ACCESS_REG_k corresponding to the PHY and PHY register SW wants to write.
3. The write operation to the PHY is scheduled and completed by the MDIO module. Completion of the write operation can be determined by polling the GO bit in MDIO CPSW_MDIO_USER_ACCESS_REG_k for a 0.
4. Completion of the operation sets the corresponding USERINTRAW bit (0 or 1) in the MDIO user command complete interrupt register (CPSW_MDIO_USER_INT_RAW_REG) corresponding to MDIO CPSW_MDIO_USER_ACCESS_REG_k used. If interrupts have been enabled on this bit using the MDIO user command complete interrupt mask set register (CPSW_MDIO_USER_INT_MASK_SET_REG),

then the bit is also set in the MDIO user command complete interrupt register (CPSW_MDIO_USER_INT_MASKED_REG) and an interrupt is triggered on the host processor.

12.2.1.5.3.3 Reading Data From a PHY Register

The MDIO module includes a user access register (MDIO CPSW_MDIO_USER_ACCESS_REG_k, where k = 0 or 1) to directly access a specified PHY device. To read a PHY register, perform the following:

1. Check to ensure that the GO bit in the MDIO user access register (CPSW_MDIO_USER_ACCESS_REG_k, where k = 0 or 1) is cleared.
2. Write to the GO, REGADR, and PHYADR bits in the CPSW_MDIO_USER_ACCESS_REG_k register corresponding to the PHY and PHY register SW wants to read.
3. The read data value is available in the DATA bit field in MDIO CPSW_MDIO_USER_ACCESS_REG_k register after the module completes the read operation on the serial bus. Completion of the read operation can be determined by polling the GO and ACK bits in CPSW_MDIO_USER_ACCESS_REG_k register. After the GO bit has cleared, the ACK bit is set on a successful read.
4. Completion of the operation sets the corresponding USERINTRAW bit (0 or 1) in the MDIO user command complete interrupt register (CPSW_MDIO_USER_INT_RAW_REG) corresponding to MDIO CPSW_MDIO_USER_ACCESS_REG_k used. If interrupts have been enabled on this bit using the MDIO user command complete interrupt mask set register (CPSW_MDIO_USER_INT_MASK_SET_REG), then the bit is also set in the MDIO user command complete interrupt register (CPSW_MDIO_USER_INT_MASKED_REG) and an interrupt is triggered on the host processor.

12.2.2 Peripheral Component Interconnect Express (PCIe) Subsystem

This chapter describes the features and functions of the device Peripheral Component Interconnect Express (PCIe) subsystem.

12.2.2.1 PCIe Subsystem Overview

The Peripheral Component Interconnect Express (PCIe) subsystem is built around a single-lane dual-mode PCIe controller that provides low pin-count, high reliability, and high-speed data transfers at rates of up to 5.0 Gbps per lane for serial links on backplanes and printed wiring boards.

The device includes one instantiation the of PCIe subsystem - PCIE0. Table 12-189 shows the PCIe subsystem allocation across device domains.

Table 12-201. PCIe Subsystem Allocation Across Device Domains

Module Instance	Domain	
	MCU	MAIN
PCIE0	-	✓

Figure 12-138 provides PCIe subsystem overview.

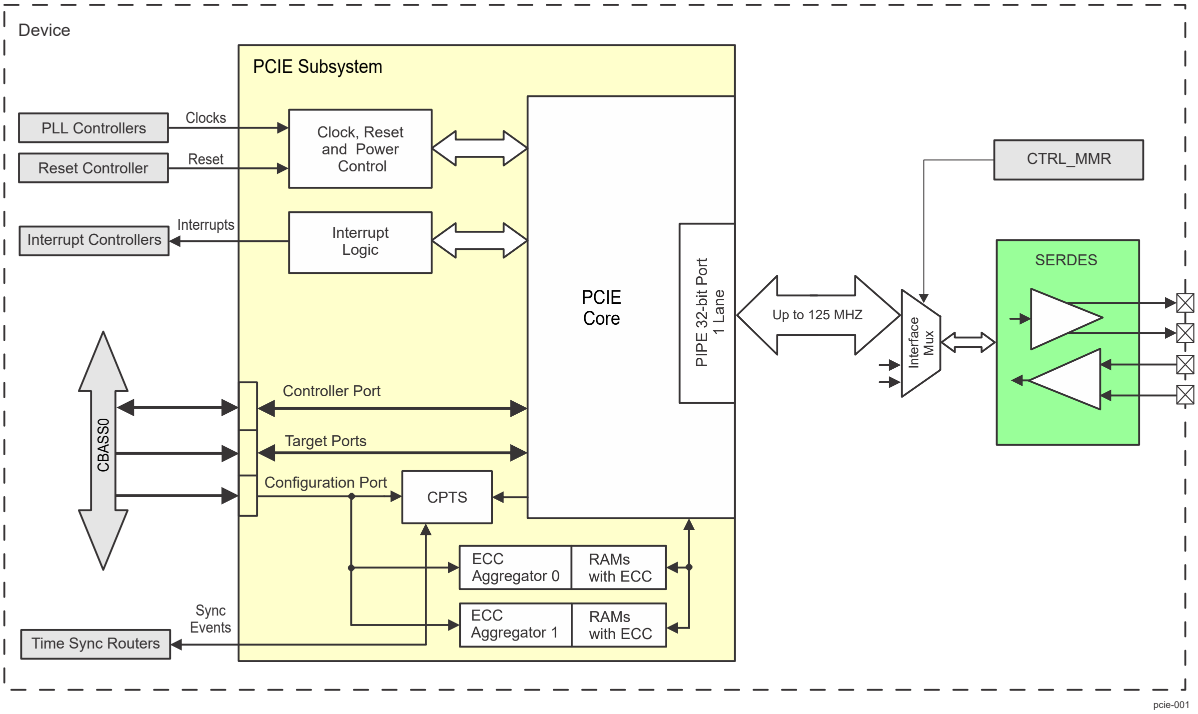

Figure 12-138. PCIe Subsystem Overview

12.2.2.1.1 PCIe Subsystem Features

Each PCIe subsystem supports the following main features:

- Compliance to PCIe® Base Specification, Revision 4.0 (Version 0.7)
- 1-lane configuration with up to 5.0 Gbps/lane (Gen2). Can be used in 1x2 andS 1x1 modes
- Gen2 (5 Gbps 8/10-bit encoding), and Gen1 (2.5 Gbps 8/10-bit encoding) with auto-negotiation
- 62.5/125 MHz operation on PIPE interface for Gen1/Gen2, respectively
- Constant 32-bit PIPE width for Gen1/2 modes
- Dual mode of operation: Root Complex (RC) or End Point (EP)
- Maximum payload size of 128 bytes
- Maximum remote read request size of 4K bytes
- Maximum Number of non-posted outstanding transactions: 8
- Single Physical Function in End Point (EP) mode
- Four virtual channels (VC)
- Four traffic classes (TC)

- PCI Power Management states:
  - L1 Power Management sub-state support
  - Device Power Management states D0, D1, D3Hot
- Resizable BAR capability
- Functional Level Reset (FLR) support
- Separate Reference Clock with Independent Spread (SRIS) support
- Legacy, MSI and MSI-X Interrupt Support
- 32 outbound address translation regions
- Precision Time Measurement (PTM) for both RC and EP modes in combination with internal Common Platform Time Sync (CPTS) module
- PCIe compliant PHY (PIPE 4.0) interface for connection to a SERDES-based PHY

12.2.2.1.2 PCIe Subsystem Not Supported Features

The PCIe subsystem does not support the following features:

- PCIe beacon for in-band wake
- Vendor Messaging
- I/O access in inbound direction in RC or EP mode
- Addressing modes other than incremental for burst transactions. As a result, the PCIe addresses cannot be in cacheable memory space.
- Single-root I/O virtualization (SR-IOV)
- Address Translation Services (ATS) capability to support virtualization in RC mode
- L2 power state
- PCI Device Power Management state D3Cold
- Hot-plug
- 48-bit address on VBUSM controller and target interfaces. Only 36-bit address is supported for these interfaces.
- Parity checking on VBUSM and VBUSP interfaces

12.2.2.2 PCIe Subsystem Environment

This section describes the PCIe subsystem and related application fields from an external system environment point of view.

CAUTION

The PCIe subsystem does not have any direct external interface pins. PCIe data transactions are implemented through the corresponding SERDES interface pins.

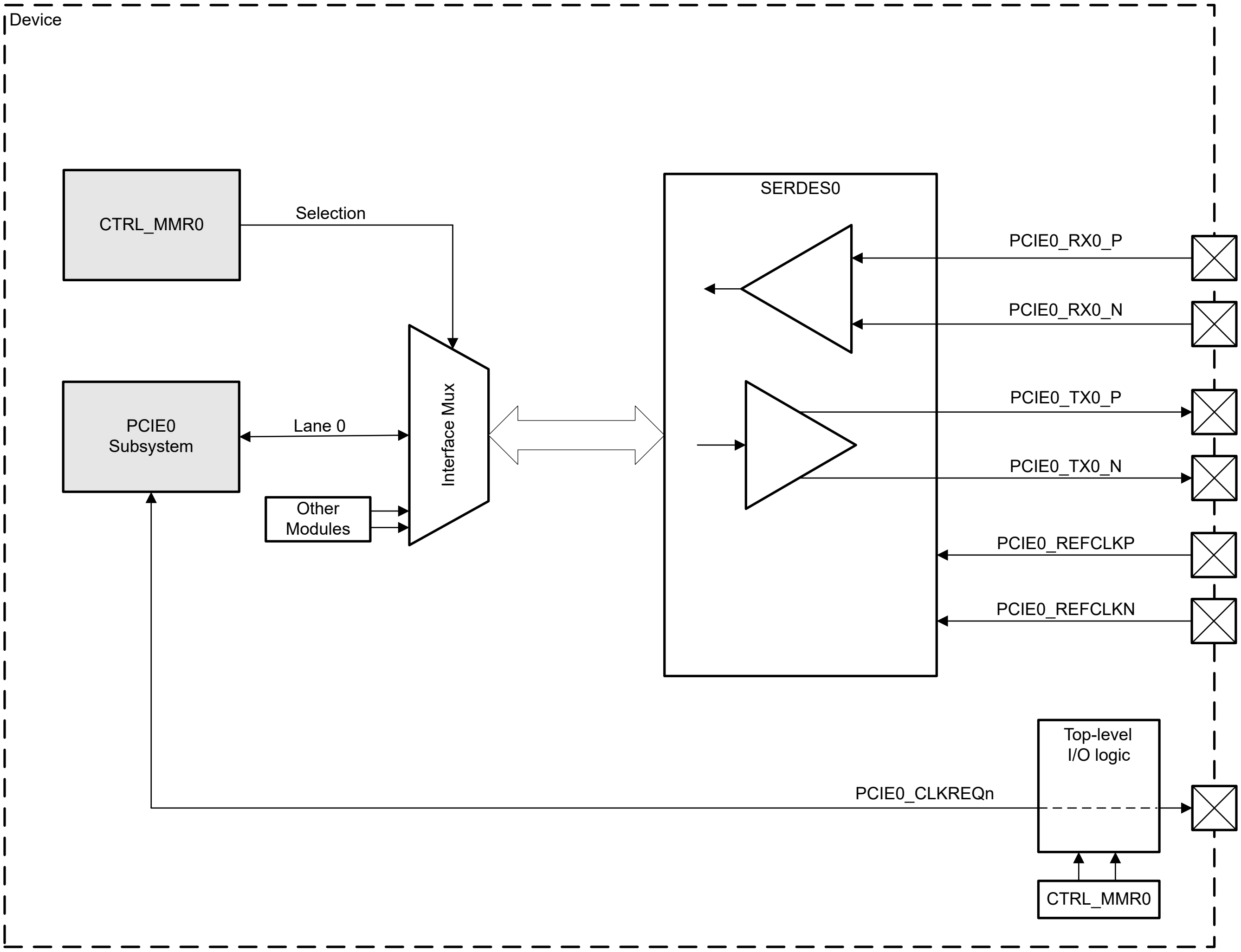

Figure 12-139. PCIe Subsystem Environment

Table 12-190 describes the SERDES signal names at device level related to PCIe subsystem and specifies their functions. For more information on the SERDES operation and interface signals, refer to Section 12.2.3 , *Serializer/Deserializer (SerDes)*.

Table 12-202. PCIe Subsystem I/O Signals

Device Level Signal	I/O[1]	Description
PCIE1 Subsystem		
PCIE0_RX0_N	I	PCIe Lane 0 Receive Differential Data (-)
PCIE0_RX0_P	I	PCIe Lane 0 Receive Differential Data (+)
PCIE0_TX0_N	O	PCIe Lane 0 Transmit Differential Data (-)
PCIE0_TX0_P	O	PCIe Lane 0 Transmit Differential Data (+)
PCIE0_REFCLKP	I	PCIe Differential Reference Clock (+)
PCIE_REFCLKN	I	PCIe Differential Reference Clock (-)
PCIE0_CLKREQn	I/O[2]	PCIe sideband signal for negotiation of L1 Substate entry/exit. The CLKREQn pin operates as an active low open-drain bi directional reference clock request pin. 1 = no request for clock; 0 = request for clock

(1) I = Input; O = Output.

(2) 3.3-V LVCMOS input/open-drain output

Note

The PCIe interface signals are implemented through additional use of a SERDES*n* interface. For more information on the SERDES operation and interface signals, refer to Section 12.2.3 , *Serializer/ Deserializer (SerDes)*.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.2.3 PCIe Subsystem Integration

This section describes PCIe subsystem integration in the device MAIN domain, including information about clocks, resets, and hardware requests.

There is one PCIe subsystem integrated in the device MAIN domain - PCIE0. Figure 12-140 shows the integration of PCIE0.

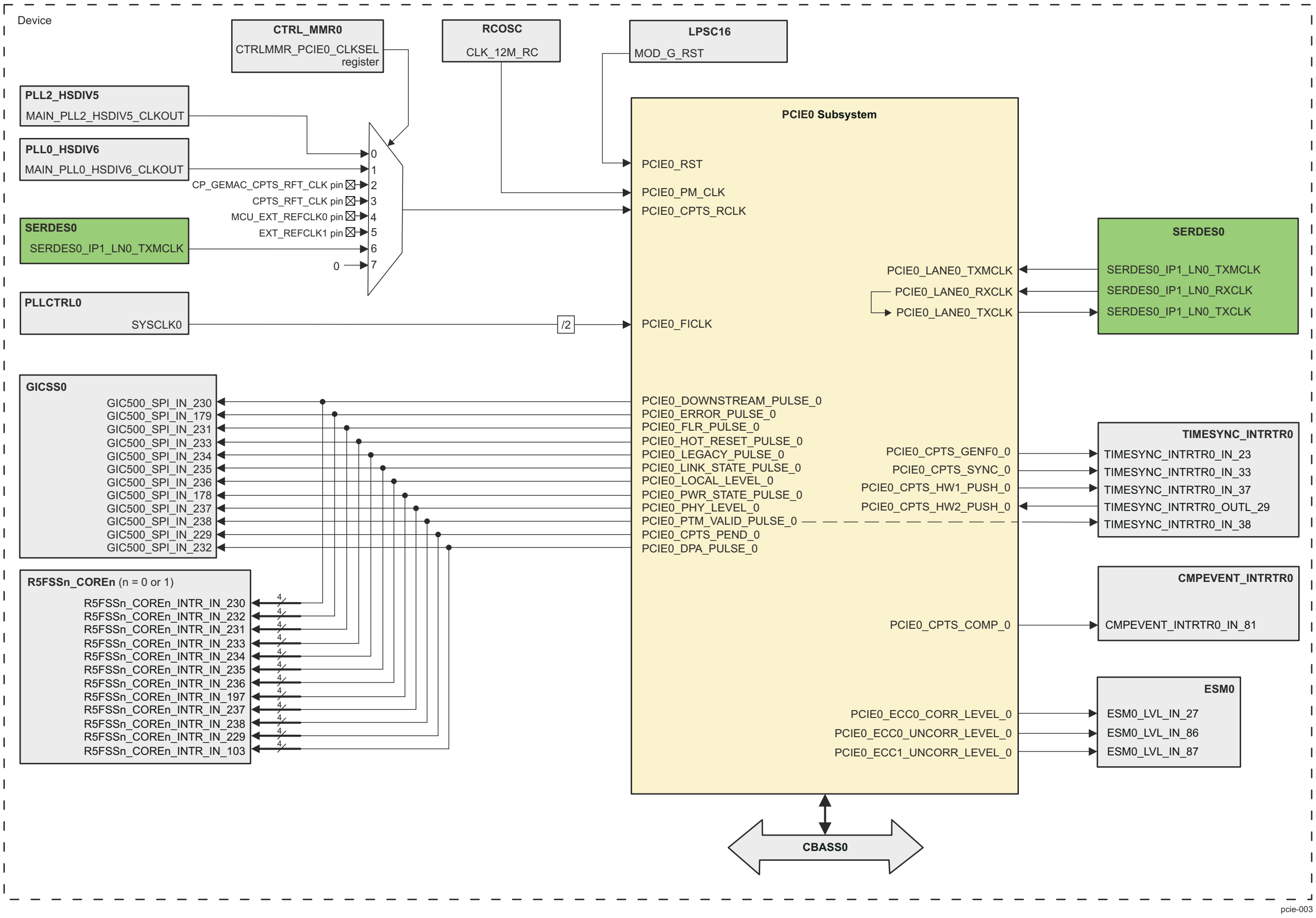

Figure 12-140. PCIe Subsystem Integration

Table 12-191 through Table 12-194 summarize the integration of PCIE0 in the device MAIN domain.

Table 12-203. PCIe Subsystem Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
PCIE0	PSC0	PD0	LPSC16	CBASS0

Table 12-204. PCIe Subsystem Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
PCIE0	PCIE0_FICLK	SYSCLK0 / 2	PLLCTRL0	PCIE0 interface bus clock (CBA_CLK).
	PCIE0_PM_CLK	CLK_12M_RC	RCOSC	PCIE0 core free-running clock used for low power state transitions and clock control generation. Used only if L1s power state is supported (see *PCIe Subsystem Features*).

Table 12-204. PCIe Subsystem Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
	PCIE0_CPTS_RCLK	MAIN_PLL2_HSDIV5_CLKOUT	PLL2_HSDIV5	PCIE0 CPTS reference clock (RCLK). Up to 250 MHz. The CPTS RCLK clock frequency should be greater than or equal to the PCIE CBA_CLK clock frequency. Otherwise, the software will have to add some wait cycles before a correct event is generated by the CPTS module. Additionally, the CPTS RCLK should be set to same frequency as the PCIe core clock. The selection of the source signal (see *PCIe Subsystem Integration*) can be done via the CTRLMMR_PCIE0_CLKSEL[2-0] CPTS_CLKSEL register field in the device Control Module.
		MAIN_PLL0_HSDIV6_CLKOUT	PLL0_HSDIV6	
		CP_GEMAC_CPTS_RFT_CLK	I/O pin	
		CPTS_RFT_CLK	I/O pin	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		SERDES0_IP1_LN0_TXMCLK	SERDES0	
	PCIE0_LANE0_TXMCLK	SERDES0_IP1_LN0_TXMCLK	SERDES0	PCIE0 core clock (CORE_CLK) driven by SERDES via lane 0.
	PCIE0_LANE0_RXCLK	SERDES0_IP1_LN0_RXCLK	SERDES0	PCIE0 PIPE interface clock driven by SERDES via lane 0.
SERDES0	SERDES0_IP1_LN0_TXCLK	PCIE1_LANE0_TXCLK	PCIE0	PCIE0 lane 0 PIPE/RAW TX return clock.

Table 12-205. PCIe Subsystem Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
PCIE0	PCIE0_RST	MOD_G_RST	LPSC16	PCIE0 reset

Table 12-206. PCIe Subsystem Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Type	Description
PCIE0	PCIE0_DOWNSTREAM_PULSE_0	GIC500_SPI_IN_230	GICSS0	Pulse	PCIE0 downstream interrupt
		R5FSS0_CORE0_INTR_IN_230	R5FSS0_CORE0	Pulse	
		R5FSS0_CORE1_INTR_IN_230	R5FSS0_CORE1	Pulse	
		R5FSS1_CORE0_INTR_IN_230	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_230	R5FSS1_CORE1	Pulse	
	PCIE0_ERROR_PULSE_0	GIC500_SPI_IN_179	GICSS0	Pulse	PCIE0 error interrupt
		R5FSS0_CORE0_INTR_IN_232	R5FSS0_CORE0	Pulse	
		R5FSS0_CORE1_INTR_IN_232	R5FSS0_CORE1	Pulse	
		R5FSS1_CORE0_INTR_IN_232	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_232	R5FSS1_CORE1	Pulse	
	PCIE0_FLR_PULSE_0	GIC500_SPI_IN_231	GICSS0	Pulse	PCIE0 function level interrupt
		R5FSS0_CORE0_INTR_IN_231	R5FSS0_CORE0	Pulse	

Table 12-206. PCIe Subsystem Interrupt Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Type	Description
		R5FSS0_CORE1_INTR_IN_231	R5FSS0_CORE1	Pulse	
		R5FSS1_CORE0_INTR_IN_231	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_231	R5FSS1_CORE1	Pulse	
	PCIE0_HOT_RESET_PULSE_0	GIC500_SPI_IN_233	GICSS0	Pulse	PCIE0 hot reset interrupt
		R5FSS0_CORE0_INTR_IN_233	R5FSS0_CORE0	Pulse	
		R5FSS0_CORE1_INTR_IN_233	R5FSS0_CORE1	Pulse	
		R5FSS1_CORE0_INTR_IN_233	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_233	R5FSS1_CORE1	Pulse	
	PCIE0_LEGACY_PULSE_0	GIC500_SPI_IN_234	GICSS0	Pulse	PCIE0 legacy interrupt
		R5FSS0_CORE0_INTR_IN_234	R5FSS0_CORE0	Pulse	
		R5FSS0_CORE1_INTR_IN_234	R5FSS0_CORE1	Pulse	
		R5FSS1_CORE0_INTR_IN_234	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_234	R5FSS1_CORE1	Pulse	
	PCIE0_LINK_STATE_PULSE_0	GIC500_SPI_IN_235	GICSS0	Pulse	PCIE0 link state interrupt
		R5FSS0_CORE0_INTR_IN_235	R5FSS0_CORE0	Pulse	
		R5FSS0_CORE1_INTR_IN_235	R5FSS0_CORE1	Pulse	
		R5FSS1_CORE0_INTR_IN_235	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_235	R5FSS1_CORE1	Pulse	
	PCIE0_LOCAL_LEVEL_0	GIC500_SPI_IN_236	GICSS0	Level	PCIE0 local interrupt
		R5FSS0_CORE0_INTR_IN_236	R5FSS0_CORE0	Level	
		R5FSS0_CORE1_INTR_IN_236	R5FSS0_CORE1	Level	
		R5FSS1_CORE0_INTR_IN_236	R5FSS1_CORE0	Level	
		R5FSS1_CORE1_INTR_IN_236	R5FSS1_CORE1	Level	
	PCIE0_PWR_STATE_PULSE_0	GIC500_SPI_IN_178	GICSS0	Pulse	PCIE0 power state interrupt
		R5FSS0_CORE0_INTR_IN_197	R5FSS0_CORE0	Pulse	
		R5FSS0_CORE1_INTR_IN_197	R5FSS0_CORE1	Pulse	

Table 12-206. PCIe Subsystem Interrupt Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Type	Description
		R5FSS1_CORE0_INTR_IN_197	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_197	R5FSS1_CORE1	Pulse	
	PCIE0_PHY_LEVEL_0	GIC500_SPI_IN_237	GICSS0	Level	PCIE0 PHY interrupt
		R5FSS0_CORE0_INTR_IN_237	R5FSS0_CORE0	Level	
		R5FSS0_CORE1_INTR_IN_237	R5FSS0_CORE1	Level	
		R5FSS1_CORE0_INTR_IN_237	R5FSS1_CORE0	Level	
		R5FSS1_CORE1_INTR_IN_237	R5FSS1_CORE1	Level	
	PCIE0_PTM_VALID_PULSE_0	GIC500_SPI_IN_238	GICSS0	Pulse	PCIE0 PTM valid interrupt
		R5FSS0_CORE0_INTR_IN_238	R5FSS0_CORE0	Pulse	
		R5FSS0_CORE1_INTR_IN_238	R5FSS0_CORE1	Pulse	
		R5FSS1_CORE0_INTR_IN_238	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_238	R5FSS1_CORE1	Pulse	
	PCIE0_ECC0_CORR_LEVEL_0	ESM0_LVL_IN_27	ESM0	Level	PCIE0 ECC AGGR 0 correctable error interrupt
	PCIE0_ECC0_UNCORR_LEVEL_0	ESM0_LVL_IN_86		Level	PCIE0 ECC AGGR 0 uncorrectable error interrupt
	PCIE0_ECC1_UNCORR_LEVEL_0	ESM0_LVL_IN_87		Level	PCIE0 ECC AGGR 1 uncorrectable error interrupt
	PCIE0_CPTS_PEND_0	GIC500_SPI_IN_229	GICSS0	Level	PCIE0 timesync interrupt
		R5FSS0_CORE0_INTR_IN_229	R5FSS0_CORE0	Level	
		R5FSS0_CORE1_INTR_IN_229	R5FSS0_CORE1	Level	
		R5FSS1_CORE0_INTR_IN_229	R5FSS1_CORE0	Level	
		R5FSS1_CORE1_INTR_IN_229	R5FSS1_CORE1	Level	
	PCIE0_DPA_PULSE_0	GIC500_SPI_IN_232	GICSS0	Pulse	PCIE0 dynamic power allocation interrupt
		R5FSS0_CORE0_INTR_IN_103	R5FSS0_CORE0	Pulse	
		R5FSS0_CORE1_INTR_IN_103	R5FSS0_CORE1	Pulse	
		R5FSS1_CORE0_INTR_IN_103	R5FSS1_CORE0	Pulse	
		R5FSS1_CORE1_INTR_IN_103	R5FSS1_CORE1	Pulse	

Table 12-207. PCIe Subsystem DMA events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Type	Description
PCIE0	-	-	-	-	The PCIe subsystem does not provide built-in DMA capabilities

Table 12-208. PCIe Subsystem Time Sync and Compare Events (Output)

Module Instance	Module Event	Destination Event Input	Destination	Type	Description
PCIE0	PCIE0_CPTS_HW1_PUSH_0	TIMESYNC_INTRTR0_IN_37	TIMESYNC_INTRTR0	Level	PCIE0 CPTS hardware push event (HW1_TS_PUSH)
	PCIE0_CPTS_COMP_0	CMPEVENT_INTRTR0_IN_81	CMPEVENT_INTRTR0	Pulse	PCIE0 CPTS compare output interrupt
	PCIE0_CPTS_SYNC_0	TIMESYNC_INTRTR0_IN_33	TIMESYNC_INTRTR0	Level	PCIE0 CPTS sync output interrupt
	PCIE0_CPTS_GENF0_0	TIMESYNC_INTRTR0_IN_23	TIMESYNC_INTRTR0	Level	PCIE0 CPTS GENF0 output interrupt
	PCIE0_PTM_VALID_PULSE_0	TIMESYNC_INTRTR0_IN_38	TIMESYNC_INTRTR0	Level	PCIE0 PTM valid interrupt

Table 12-209. PCIe Subsystem Time Sync and Compare Events (Input)

Module Instance	Module Event	Source Event Output	Source	Type	Description
PCIE0	PCIE0_CPTS_HW2_PUSH_0	TIMESYNC_INTRTR0_OUTL_29	TIMESYNC_INTRTR0	Level	PCIE0 CPTS hardware time stamp push event (HW2_TS_PUSH)

12.2.2.4 PCIe Subsystem Functional Description

12.2.2.4.1 PCIe Subsystem Block Diagram

The block diagram of PCIe subsystem is shown in Figure 12-141. The subsystem id comprised of these major components – the PCIe Core with AXI interfaces, bridges to connect to the system CBASS0 interconnect controller and target interfaces, bridges to connect the system CBASS0 configuration interfaces, additional logic to implement the Precision Time Measurement (PTM), user configuration and interrupt, and RAM to support the controller FIFOs.

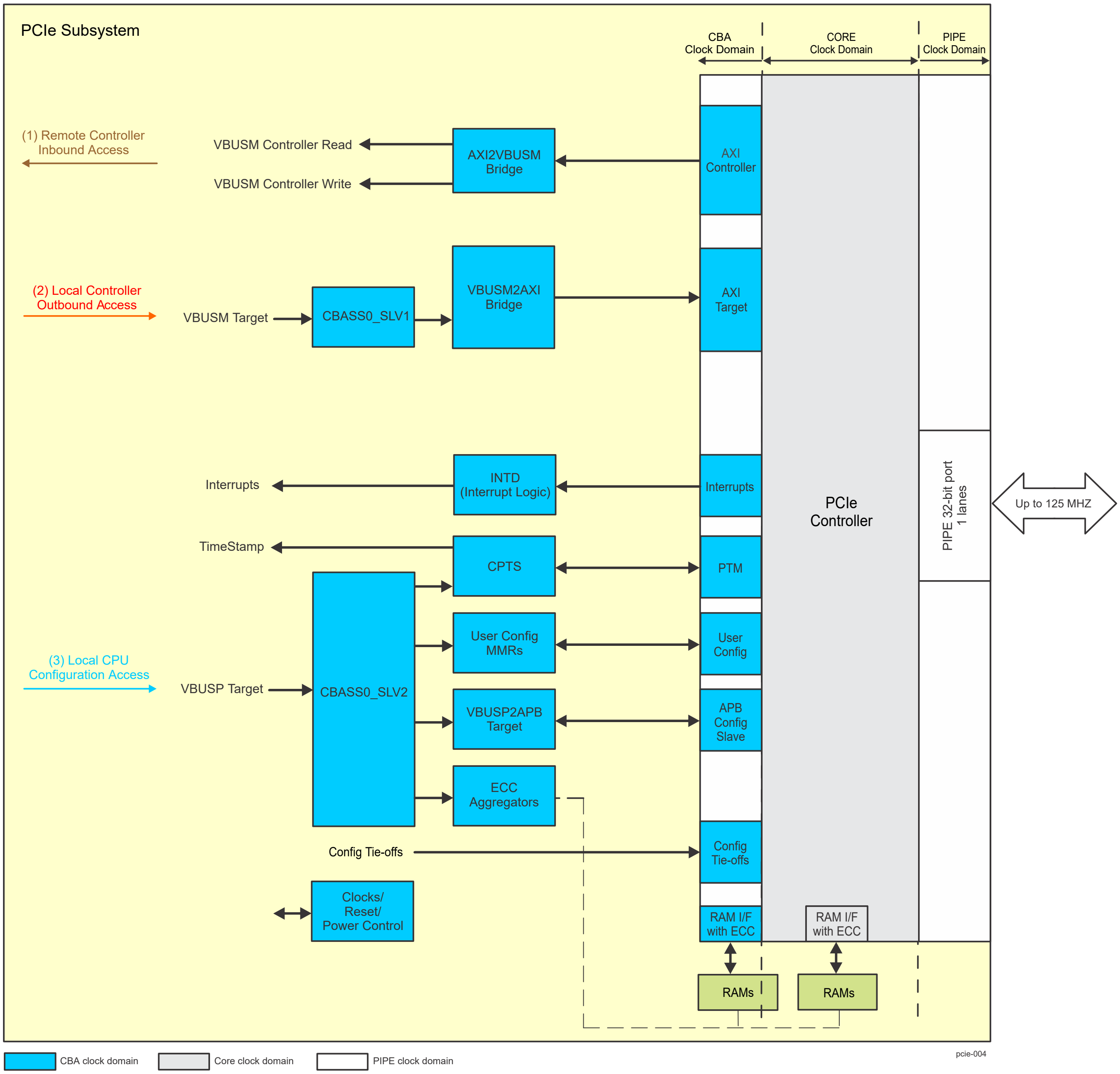

Figure 12-141. PCIe Subsystem Block Diagram

Figure 12-141 also shows some example data flows in the PCIe subsystem, such as:

1. A remote controller issues a read or write access over PCIe to the local device. This will create a command to be issued on the PCIe VBUSM controller read or write interface.

2. A controller in the local device issues a read or write access over PCIe to the remote device. This will create a command to be issued on the PCIe VBUSM target read or write interface.
3. A controller in the local device wants to access the local PCIe configuration registers, the ECC aggregator registers, or the CPTS registers. This will create a transaction over the PCIe VBUSP target interface.

12.2.2.4.1.1 PCIe PHY Interface

The PCIe subsystem incorporates a 1-lane PCIe compliant PHY (PIPE) interface to connect to a SERDES-based PHY. The PCIe PHY module consist of a SERDES module and a PCIe PCS (Physical Coding Sub-block) module. The SERDES module converts parallel data into PCIe serial signals and the PCIe PCS module provides an industry standard PIPE Interface to PCIe MAC. The frequency of the PIPE interface can be 62.5MHz or 125MHz depending on whether the system is operating in Gen1 or Gen2 mode. The width of the PIPE interface remains constant at 32-bits for all modes of operation. For more information on the SERDES module, see Section 12.2.3 , *Serializer/Deserializer (SerDes)*.

12.2.2.4.1.1.1 PCIe Core Module

The PCIe Core module supports dual mode of operation - it can be configured as an End Point (EP) and also as a Root Complex (RC). The operational mode is selected with the CTRLMMR_PCIE0_CTRL[7] MODE_SEL register bit within the device Control Module (CTRL_MMR). It is expected that the MODE_SEL bit is programmed during initial power up based on settings in the SoC boot configuration or a non-volatile storage such as eFuse or Flash memory.

It is not expected that the MODE_SEL setting would have to change during a full power cycle of the device. It is more likely that the operational mode of a SoC will stay as EP or RC for a particular end product’s life cycle. It is not expected to switch back and forth during operation without a reset cycle.

The PCIe core module supports four virtual channels (VC) and four transfer classes (TC). The VCs can be used to implement Quality-of-Service (QoS) mechanism by enabling priority or round-robin arbitration. Typically, the highest numbered enabled VC is assigned the highest priority.

There is one iinitiator port and one target port in the PCIe core. All ingress data traffic regardless of the VC assigned will be delivered on the initiator port. Similarly, all egress data that is presented on target port of the PCIe core will be assigned VCs through the outbound address translation registers.

12.2.2.4.1.2 Custom Logic

The PCIe subsystem includes custom logic to implement Precision Time Management (PTM), interrupts and user configuration registers.

12.2.2.4.2 PCIe Subsystem Reset Schemes

This section describes the reset schemes supported by PCIe Base Specification and the way these resets are supported by the PCIe Subsystem. PCIe Base Specification specifies two mechanisms for performing reset – Conventional Reset mechanism and Functional Level Reset mechanism.

12.2.2.4.2.1 PCIe Conventional Reset

There are three distinct types of Conventional Reset and each of these causes the hardware state machines, hardware logic, port states and configuration registers to be initialized to their default values.

1. Cold Reset – The reset occurring at power-up of the device is referred to as Cold Reset. Cold Reset is triggered by the PERSTn signal being asserted. PERSTn signal is an auxiliary signal in PCIe Specification and can be used at power on reset for the device that has PCIe as its primary bus interface to rest of the system. The device is allowed to generate its own power-on reset as long as the PCIe requirements for PERSTn are met. See PCIe Base Specifications for details.
2. Warm Reset – A reset can be triggered by the hardware without the removal of power from the device. This reset is referred to as Warm Reset. The hardware implementation is not specified by the PCIe Specification.
3. Hot Reset – The PCIe Specifications provides an in-band mechanism to propagate a Conventional Reset across a Link. This reset, called the Hot Reset, propagates via the transmission of TS1 Ordered Sets. In

general, Hot Reset is software controlled procedure and can only be issued by Root Complex in a PCIe network as the propagation is downstream only. PCIe subsystem translates the received in-band hot reset into an interrupt that can then be used by software to reset the PCIe subsystem.

After a conventional reset, the software must wait at least 100 ms before attempting any PCIe transaction on the device that has been reset. If the downstream device does not respond to transaction packets, it must not give up until 1 second plus an additional 50% (0.5 second) time is lapsed.

12.2.2.4.2.2 PCIe Function Level Reset

The Function Level Reset (FLR) is an optional in-band reset mechanism that is used to reset one particular function in a PCIe device. The PCIe core will initate the appropriate function level reset process when it receives the FLR message. The PCIe subsystem will raise an interrupt to the SoC, based on the FLR_IN_PROGRESS[0] status output from the PCIe core. Software can update the PCIE_USER_FLR_DONE[5-0] FLR_DONE register bits to signal to the PCIe core that the application layer FLR processing is complete.

12.2.2.4.2.3 PCIe Reset Isolation

It can be important to isolate reset of PCIe subsystem from reset of the rest of the device. The procedure to implement this depends upon what functionality the PCIe subsystem is providing – Root Complex or End Point.

12.2.2.4.2.3.1 Root Complex Reset with Device Not Reset

When PCIe subsystem is operating as a Root Complex, it is the controller controller on the PCIe subsystem. When PCIe subsystem is to be reset in this operating mode, the link to the downstream device will get disconnected. To accomplish this reset, the PCIe subsystem RC should issue a hot reset to End Point or Switch downstream. It should also stop any ongoing transactions. Then, a PCIe subsystem reset can be issued. The sequence of events is outlined below:

1. Stop transactions at system and application level. This is recommended for graceful suspension of activity at system level. It is not required by PCIe subsystem though. Not choosing to gracefully stop transaction would cause some of the outstanding transactions to complete in error and it may be harmful from software stability standpoint.
2. Disable “Bus Controller Enable” for End Points (see Section 12.2.2.4.6.2 , *PCIe Transaction Limitations*). Note that a hand shake with EP Software may be required as not all End Point application software will automatically become aware of this disable action from RC.
3. Optionally, issue Hot Reset to End Point devices via PCIE_USER_RSTCMD[0] INIT_HOT_RESET bit . Note that the link will be getting disconnected. So, a reset may be happening regardless of the Hot Reset command from RC. It depends on the architecture of the other (external) device. In devices with PCIe subsystem, link disconnection automatically results in a reset request interrupt. A PCIe subsystem reset is required to get the memory buffers out of internal flush modes.
4. Initiate Clock Stop sequence and wait for Acknowledgement. For more information, see Section 12.2.2.4.3.1 , *CBA Power Management.*
5. Issue reset to PCIe subsystem (local reset).
6. Reinitialize PCIe subsystem and downstream devices. PCIe bus enumeration must be performed again.

Note that it is possible for Root Complex to occasionally see the downstream device going down for some reason and disconnecting. Such events typically occur due to an internal error condition in the End Point. When such an event occurs, the sequence of events for the Root Complex will be as follows:

1. The PCIe subsystem in RC mode will issue the “Reset Request” interrupt when it detects link getting disconnected unexpectedly.
2. The PCIe subsystem will flush all controller transactions and any completion data from pending transactions. It will also start completing target transactions with error completions.
3. After servicing the interrupt and disabling further interrupts, the system software must reset PCIe subsystem Root Complex (see steps #4 and later specified previously in this section).

12.2.2.4.2.3.2 Device Reset with Root Complex Not Reset

As a Root Complex, PCIe core is the controller of PCIe subsystem. If the device hardware and the software is reset and re-initialized, the system does not get additional benefit of keeping the PCIe subsystem alive as all context information is lost. So, this mode is not supported.

12.2.2.4.2.3.3 End Point Device Reset with Root Complex Not Reset

It may be desirable to isolate the reset only to PCIe subsystem when it is operating as an End Point. Such resets may be implemented when a Hot Reset command is received from upstream device (Root Complex or Switch). The sequence to be followed is as outlined below.

1. Hot Reset is received. The “Request Reset” interrupt is triggered.
2. The PCIe subsystem will automatically enter Flush Mode. The PCIe Link Training and Status State Machine (LTSSM) will be disabled automatically.
3. PCIe subsystem will complete all controller transactions and any completion data from pending transactions will be accepted and discarded. It will also start issuing error response for new target transactions.
4. Upon receipt of the reset interrupt from PCIe subsystem, the system software must immediately start preparing for shut down of PCIe subsystem. The DMA or software process accessing PCIe subsystem should gracefully suspend operations. Otherwise, step #3 may continue for unduly long time and Root Complex may assume that the EP is non-responsive to its link re-training attempts.
5. Read the Reset Command register (PCIE_USER_RSTCMD) to check if the bridge activity flush bit is zero. This indicates that it is safe to issue warm reset to PCIe subsystem.
6. Initiate Clock Stop sequence. This will ensure no outstanding transactions exist.
7. Issue a PCIe subsystem Reset.
8. Resume initialization sequence.

12.2.2.4.2.3.4 Device Reset with End Point Device Not Reset

As an End Point, the PCIe subsystem does not need to stay operational when the device reset is happening. Upon detecting the link disconnection, the upstream port will re-train the link when Root Port issues a link retrain command to itself or to a switch port next to the EP.

If it is required that the PCIe subsystem be operational (without any transactions though), the End Point must negotiate with the other devices (primarily Root Port) to stop activity. Otherwise, if the End Point goes into force idle/standby or clock stop modes without properly managing the process, there will be timeouts or errors on incoming read transactions and writes will be completely lost. In such situation, the Root Port will encounter excessive errors and may issue a hot reset to the End Point anyway.

12.2.2.4.2.4 PCIe Reset Limitations

Once a reset situation occurs, the PCIe subsystem prepares for reset assertion from the device level reset controller. In this mode, all outbound write transactions are discarded and all outbound reads are returned with error. Similarly, all inbound reads/writes are discarded and any pending reads are completed but data is discarded. Additionally, any register reads on local or remote registers regions are returned in error even through data may be correct. Register writes on local registers are executed correctly.

Whenever the reset interrupt is asserted by PCIe subsystem, the host controller should clear the interrupt, perform a clock stop request/ack sequence and issue a local reset to PCIe subsystem.

12.2.2.4.2.5 PCIe Reset Requirements

Whenever link goes from connected to disconnected state, the PCIe subsystem requires re-initialization based on the events occurring in PCIe core. A request for reset is typically going to be issued and will manifest as a reset request interrupt. Since loopback requires transitions through link connect and disconnect, it will generate reset request interrupts. Typically, issuing the warm reset (module reset for CBA) would be sufficient.

12.2.2.4.3 PCIe Subsystem Power Management

PCIe has multiple power management protocols. Some of them are invoked by the hardware, such as Active State Power Management (ASPM), while others are activated at higher levels via software.

The PCIe core supports D0, D1 and D3-Hot power states.

Link power states L0, L0s, L1, L1s are supported.

L0s entry and exit is managed by the PCIe core if ASPM L0s is enabled.

L1 entry and exit is also managed by the PCIe core if ASPM L1 is enabled. Software can force the exit from L1 by writing to the PCIE_USER_PMCMD[0] CLIENT_REQ_EXIT_L1 bit in the PCIe subsystem. Entry into L1 can also be blocked by setting the PCIE_USER_PMCMD[0] CLIENT_REQ_EXIT_L1 bit.

L1s support requires that the CLKREQ pin be connected to the remote peer. L1s power state is entered when the link is in L1 and CLKREQ pin is de-asserted. Software can force the exit from L1s by writing to either the PCIE_USER_PMCMD[0] CLIENT_REQ_EXIT_L1 or PCIE_USER_PMCMD[1] CLIENT_REQ_EXIT_L1_SUBSTATE bits in the PCIe subsystem.

12.2.2.4.3.1 CBA Power Management

The power management for PCIe subsystem with CBA interface is primarily accomplished through the clock stop protocol. Any time the clock stop protocol is initiated, the PCIe subsystem will acknowledge after making sure that there are no outstanding transactions. If there are any pending transactions in the subsystem, then the clock stop acknowledgement procedure cannot be completed. Therefore, it is necessary that the system software first suspend activity on the serial link as well as on the CBA interface. To do so, it is expected that the devices communicating with the device on which clock stop procedure is to be performed agree to stop transactions targeted to the device in question. Similarly, it is required that the outgoing transactions also be stopped to successfully complete the clock stop sequence. The PCIe subsystem will guarantee that in the event there are pending transactions that are still in process of draining will prevent the clock-stop acknowledgement to be issued to CBA subsystem power management logic.

Note

The PCIe subsystem does not have ability to terminate the clock stop state. Therefore, any wakeup sequence can only be initiated through other means such as software driven timers or software detected events occurring outside of PCIe subsystem.

12.2.2.4.4 PCIe Subsystem Interrupts

The PCIe subsystem provides a mix of interrupts from the PCIe controller interrupt, CPTS interrupts, and interrupts generated in the subsystem using the internal Interrupt Distributor (CP_INTD) module.

The CP_INTD module is used to generate and aggregate interrupts from various status signals of the PCIe core. Interrupts from the PCIe core and CPTS module are ported out directly to the PCIe subsystem boundary without any aggregation. Table 12-198 shows the details on the PCIe subsystem interrupt outputs.

Table 12-210. PCIe Subsystem Interrupt Events

Interrupt Name	Clock Dependency	Description
PCIE_LEGACY_PULSE	CBA_CLK	PCIe legacy interrupt. INTA_OUT, INTB_OUT, INTC_OUT and INTD_OUT status outputs from the PCIe core are aggregated. Note: Valid in RC mode only.
PCIE_ERROR_PULSE	CBA_CLK	PCIe error interrupt. FATAL_ERROR_OUT, NON_FATAL_ERROR_OUT and CORRECTABLE_ERROR_OUT status outputs from the PCIe core are aggregated. Note: Valid in both RC and EP modes.
PCIE_FLR_PULSE	CBA_CLK	PCIe Function Level interrupt. FLR_IN_PROGRESS[0] status outputs from the PCIe core is used to generate this interrupt. Note: Valid in EP mode only.
PCIE_DOWNSTREAM_PULSE	CBA_CLK	PCIe downstream interrupt. • F0_VSEC_INTERRUPT_OUT, status output from the PCIe controller is used to generate this interrupt. Note: Valid in EP mode only

Table 12-210. PCIe Subsystem Interrupt Events (continued)

Interrupt Name	Clock Dependency	Description
PCIE_HOT_RESET_PULSE	CBA_CLK	PCIe hot reset interrupt. HOT_RESET_OUT status output from the PCIe controller is aggregated. Note: Valid in EP mode only.
PCIE_LINK_STATE_PULSE	CBA_CLK	PCIe link state interrupt. LINK_DOWN_RESET_OUT status from the PCIe core is is used to generate this interrupt. Note: Valid in both RC and EP modes.
PCIE_PWR_STATE_PULSE	CBA_CLK	PCIe power state interrupt. POWER_STATE_CHANGE and DPA_INTERRUPT[0] status output from the PCIe core are used to generate this interrupt Note: Valid in both EP and RC modes.
PCIE_DPA_PULSE	CBA_CLK	PCIe dynamic power allocation interrupt. DPA_INTERRUPT[0] status output from the PCIe core is used to generate this interrupt. Note: Valid in both EP and RC modes.
PCIE_LOCAL_LEVEL	CBA_CLK	PCIe local interrupt. The LOCAL_INTERRUPT from the PCIe controller is brought out directly without any aggregation. Note: Valid in both RC and EP modes.
PCIE_PHY_LEVEL	CBA_CLK	PCIe PHY interrupt. The PHY_INTERRUPT_OUT from the PCIe controller is brought out directly without any aggregation. Note: Valid in both RC and EP modes.
PCIE_PTM_VALID_PULSE	CBA_CLK	PCIe PTM valid interrupt. PTM_LOCAL_TIMER_OUT_VALID status output from the PCIe controller is used to generate this interrupt. Note: Valid only in EP mode.
PCIE_ECC0_UNCORR_PULSE	CBA_CLK	PCIe ECC Aggregator0 uncorrected pulse interrupt.
PCIE_ECC0_UNCORR_LEVEL	CBA_CLK	PCIe ECC Aggregator0 uncorrected level interrupt.
PCIE_ECC0_CORR_PULSE	CBA_CLK	PCIe ECC Aggregator0 corrected pulse interrupt.
PCIE_ECC0_CORR_LEVEL	CBA_CLK	PCIe ECC Aggregator0 corrected level interrupt.
PCIE_ECC1_UNCORR_PULSE	LANE0_TXMCLK	PCIe ECC Aggregator1 uncorrected pulse interrupt.
PCIE_ECC1_UNCORR_LEVEL	LANE0_TXMCLK	PCIe ECC Aggregator1 uncorrected level interrupt.
PCIE_CPTS_PEND_INTR	CBA_CLK	PCIe CPTS level interrupt.

12.2.2.4.4.1 Interrupts Aggregation

The PCIe subsystem includes the CP_INTD module to aggregate some of the PCIe controller signals into the subsystem interrupts indicated in Table 12-198. The interrupt aggregator takes both level and pulse signals from the PCIe core and produces the aggregated pulse interrupt outputs.

The aggregator also supports the End of Interrupt (EOI) feature. EOI can be used to re-trigger a pulse interrupt output, if a PCIe controller level signal is still asserted at the end of interrupt processing. The re-triggering of the the pulse interrupt can be achieved by writing the specified EOI vector value to the PCIE_USER_EOI_VECTOR register.

Table 12-211. PCIe Controller Interrupts Aggregation - 1

Aggregated Interrupt	CP_INTD Registers and Bits Mapping		EOI_VECTOR	PCIe Controller Signal	Description
	PCIE_INTD_ENABLE_REG_SYS_0 PCIE_INTD_ENABLE_CLR_REG_SYS_0 PCIE_INTD_STATUS_REG_SYS_0 PCIE_INTD_STATUS_CLR_REG_SYS_0(1)				
PCIE_DOWNSTREAM_PULSE	0	pcie_downstream_0	0	down_pf0_intr_out	Downstream PF0 interrupt (EP mode only)
-	31-1	Reserved	-	-	-

(1) Register is not used since all PCIe controller signals being aggregated are of type 'level'.

Table 12-212. PCIe Controller Interrupts Aggregation - 2

Aggregated Interrupt	CP_INTD Registers and Bits Mapping		EOI_VECTOR	PCIe Controller Signal	Description
	PCIE_INTD_ENABLE_REG_SYS_1 PCIE_INTD_ENABLE_CLR_REG_SYS_1 PCIE_INTD_STATUS_REG_SYS_1 PCIE_INTD_STATUS_CLR_REG_SYS_1				
PCIE_FLR_PULSE	0	pcie_flr_0	1	flr_in_progress	PF0 function-level reset (EP mode only)
-	21-1	Reserved	-	-	-
PCIE_LEGACY_PULSE	22	pcie_legacy_0	2	inta_out	Legacy interrupt A (RC mode only)
	23	pcie_legacy_1		intb_out	Legacy interrupt B (RC mode only)
	24	pcie_legacy_2		intc_out	Legacy interrupt C (RC mode only)
	25	pcie_legacy_3		intd_out	Legacy interrupt D (RC mode only)
PCIE_PWR_STATE_PULSE	26	pcie_pwr_state	3	power_state_change_intr	Power state change to D1 or D3
-	31-27	Reserved	-	-	-

Table 12-213. PCIe Controller Interrupts Aggregation - 3

Aggregated Interrupt	CP_INTD Registers and Bits Mapping		EOI_VECTOR	PCIe Controller Signal	Description
	PCIE_INTD_ENABLE_REG_SYS_2 PCIE_INTD_ENABLE_CLR_REG_SYS_2 PCIE_INTD_STATUS_REG_SYS_2 PCIE_INTD_STATUS_CLR_REG_SYS_2				
PCIE_DPA_PULSE	0	pcie_dpa	N/A(1)	dpa_intr	PF0 DPA power state change (EP mode only)
-	5-1	Reserved	-	-	-
PCIE_ERROR_PULSE	6	pcie_error_0	N/A(1)	correctable_error	Correctable error
	7	pcie_error_1		non_fatal_error	Non-Fatal error
	8	pcie_error_2		fatal_error	Fatal error
PCIE_HOT_RESET_PULSE	9	pcie_hot_reset	N/A(1)	c_hot_reset_out_sync	Hot reset (EP mode only)
PCIE_LINK_STATE_PULSE	10	pcie_link_state	N/A(1)	link_down_reset_out	Link down reset
PCIE_PTM_VALID_PULSE	11	pcie_ptm	N/A(1)	ptm_local_timer_out_valid_sync	PTM local timer valid (EP mode only)
-	31-12	Reserved	-	-	-

(1) EOI is not used since the input signal is of type 'pulse'.

12.2.2.4.4.2 Interrupt Generation in EP Mode

When PCIe subsystem is operating as an End Point (EP), either the legacy interrupts, MSI or MSI-X interrupts can be triggered to the upstream ports (eventually leading to an interrupt in RC device). As per PCIe Specifications, each PCIe function may generate only one of the Legacy or MSI interrupt types as decided during configuration period.

12.2.2.4.4.2.1 Legacy Interrupt Generation in EP Mode

The End Point (EP) can trigger generation of a PCI Legacy Interrupt at the Root Complex via an in-band Assert_INTx / Deassert_INTx messages (where x = A, B, C, or D). Software can write to the PCIE_USER_LEGACY_INTR_SET register to trigger the required INTx (where x = A, B, C, or D) assert and de-assert message from the PCIe core. Once an assert message has been generated, it cannot be generated again until a deassert message is generated. Thus, only one interrupt can be pending at a time.

There is no hardware input port provided that will allow generation of legacy interrupts on the EP port.

Note

The interrupt messaging mechanism makes it unfeasible to guarantee a time of delivery of the interrupt unlike in conventional designs where the interrupt line is often electrically connected to the final destination.

12.2.2.4.4.2.2 MSI and MSI-X Interrupt Generation

In the case of MSI interrupts signaling, the interrupt conditions are communicated from the EP to the RC via messages. Thus, upon the occurrence of an interrupt condition, a message is sent by the EP with information that identifies the origin of the interrupt. Each message is in the form of a memory write request, containing an address and a data value to be written. Each PCI function supported by a device can be assigned a separate memory address, thus providing separate virtual channels for signaling interrupts generated by each function. In addition, the MSI mechanism allows a maximum of 32 distinct data patterns in the messages generated by each PCI function, and each pattern can be assigned to an interrupt condition within the function.

In the case of MSI-X interrupts signaling, the operation is similar to the MSI mode, except that the mechanism allows a much larger number of distinct interrupt conditions as many as 2048 per function to be communicated, and enables a distinct address to be defined for each of these conditions. This mechanism requires two tables to be stored in the EP memory. The MSI-X table contains the address/data patterns to be used for each interrupt condition (as many as 2048 per function) as well as individual enable/mask bits, and the Pending Bit Array (PBA) stores the status of each interrupt condition. Interrupt conditions are communicated from the EP to the RC via messages (write requests), as in the case of the MSI mode.

12.2.2.4.4.3 Interrupt Reception in EP Mode

The PCIe specification does not have provision for End Points to receive legacy interrupts. As a result, only events other than these are used to map to interrupts.

12.2.2.4.4.3.1 PCIe Core Downstream Interrupts

The Vendor Specific Capability signal of the PCIe core, F0_VSEC_INTERRUPT_OUT, is used to generate interrupts to the EP from the RP. The F0_VSEC_INTERRUPT_OUT represents the interrupt for the EP Physical Function 0. This signal is used to generate the PCIE_DOWNSTREAM_PULSE interrupt to the local host.

The RP can write to the Vendor Specific Control registers (PCIE_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_REG) to assert this signal at the EP and this will trigger the PCIE_DOWNSTREAM_PULSE interrupt to the EP host.

12.2.2.4.4.3.2 PCIe Core Function Level Reset Interrupts

The PCIE_FLR_PULSE interrupt is asserted to indicate to the host that the PCIe controller has received a function-level reset request from the remote side. The PCIE_FLR_PULSE interrupt is an aggregation of the

FLR_IN_PROGRESS[0] signal from the PCIe core. The FLR_IN_PROGRESS[0] represents Physical Function 0.

Upon assertion of the function level reset interrupt, software will need to write to the PCIE_USER_FLR_DONE[5-0] FLR_DONE bit field within 100ms to acknowledge to the PCIe core that all the application level processing related to the function level reset is complete.

12.2.2.4.4.3.3 PCIe Core Power Management Event Interrupts

The PCIE_PWR_STATE_PULSE interrupt is generated to let the software know of the power management events. The PCIE_PWR_STATE_PULSE interrupt is generated by the POWER_STATE_CHANGE_INTERRUPT output of the PCIe core. This interrupt is asserted when the power state of a physical is being changed to D1 or D3 state by writing into their Power Management Control register (PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP).

Software can check the PCIE_USER_LINKSTATUS[23-16] POWER_STATE_CHANGE_FUNCTION_NUM register field to determine the physical function for which power state change occurred. The PCIE_USER_PMCMD[2] POWER_STATE_CHANGE_ACK register bit can be used to acknowledge the POWER_STATE_CHANGE_INTERRUPT.

The PCIE_DPA_PULSE interrupt is generated by aggregating the PCIe controller DPA_INTR0 interrupt status output. This interrupt is asserted in EP mode when there is a configuration write to the dynamic power allocation control register (PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG) to modify the DPA power state of the device. The DPA_INTR0 is asserted for such an event for PF0.

12.2.2.4.4.3.4 PCIe Core Hot Reset Request Interrupt

When the link is down, the Root Complex may request reset of the End Point. This request is terminated as a PCIE_HOT_RESET_PULSE interrupt to the End Point host software. All outstanding transactions are completed in error on target port and further transactions are not generated on the controller port. Once the transactions are completely stopped, the software should issue a local reset to PCIe subsystem. The re-initialization process may then be started.

The PCIE_HOT_RESET_PULSE interrupt is generated from the HOT_RESET_OUT output of the PCIe core.

12.2.2.4.4.3.5 PTM Valid Interrupt

In EP mode, the PCIe subsystem will generate the PCIE_PTM_VALID_PULSE interrupt to the local CPU after a PTM dialog between the PTM requester (EP) and the PTM responser (RP). The PTM valid interrupt indicates to the CPU in the EP that the local timers have been updated with the timestamp data obtained from the RP. The CPU can read the timer registers inside the EP to determine the current timebase.

The PCIE_PTM_VALID_PULSE interrupt is generated from the PTM_LOCAL_TIMER_OUT_VALID signal from the PCIe core.

12.2.2.4.4.4 Interrupt Generation in RC Mode

As per PCIe Base Specifications, Root Complex ports only receive interrupts. There is no mechanism to generate interrupts from RC port to EP mode as per PCIe specification.

However, PCIe subsystem does support generation of interrupts from RC to EP. The downstream interrupts described in Section 12.2.2.4.4.3.1 , *PCIe Core Downstream Interrupts* provides a mechanism for the RC to generate software triggered interrupts to the EP.

12.2.2.4.4.5 Interrupt Reception in RC Mode

12.2.2.4.4.5.1 PCIe Legacy Interrupt Reception in RC Mode

The RC can receive any of the four legacy INTx interrupts from the EP. These will trigger the PCIE_LEGACY_PULSE interrupt to the host CPU.

The PCIE_LEGACY_PULSE interrupt is an aggregation INTA_OUT, INTB_OUT, INTC_OUT and INTD_OUT signals from the PCIe core.

12.2.2.4.4.5.2 MSI/MSI-X Interrupt Reception in RC Mode

The PCIe core decodes all MSI and MSI-X messages received from the link and forwards them as a 32-bit write transaction on the AXI controller interface.

The destination address for MSI/MSI-X write transactions should be the ARM GIC. The GIC will process the write transaction and create an interrupt to the ARM Ax CPU core in the device.

12.2.2.4.4.5.3 Advanced Error Reporting Interrupt

If enabled by software at the time of enumeration, PCIe subsystem will generate this interrupt to indicate occurrence of errors of various levels of severity. The software can choose not to enable Advanced Error Reporting but if it enables, it must process the interrupt as per PCIe Specifications.

The advanced error reporting interrupt is signaled by the PCIE_ERROR_PULSE interrupt. The PCIE_ERROR_PULSE is an aggregation of the FATAL_ERROR_OUT, NON_FATAL_ERROR_OUT and CORRECTABLE_ERROR_OUT from the PCIe core.

12.2.2.4.4.6 Common Interrupt Reception in RC and EP Modes

These interrupts are common to both RC and EP modes of operation.

12.2.2.4.4.6.1 PCIe Local Interrupt

The LOCAL_INTERRUPT from the PCIe controller is ported out directly to the PCIe subsystem boundary. For more details, see the PCIe specification

12.2.2.4.4.6.2 PHY Interrupt

The PHY_INTERRUPT_OUT from the PCIe controller is ported out directly to the PCIe subsystem boundary. For more details, see the PCIe specification

12.2.2.4.4.6.3 Link down Interrupt

If the PHY link is disconnected, the PCIE_LINK_STATE_PULSE interrupt will be generated. The expected course of action is to reset the entire PCIe subsystem and restart. All application states must also be initialized so that the operations can resume following the reset and renegotiation of the link.

The PCIE_LINK_STATE_PULSE interrupt is generated from the LINK_DOWN_RESET_OUT output of the PCIe core.

12.2.2.4.4.6.4 Transaction Error Interrupts

If there is a timeout on PCIe or an abort, PCIE_PHY_LOCAL_LEVEL interrupt will be issued. The PCIE_PHY_LOCAL_LEVEL interrupt is generated by the aggregation of the LOCAL_INTERRUPT and PHY_INTERRUPT_OUT signals from the PCIe core. For more details, see the PCIe specification.

12.2.2.4.4.6.5 Power Management Event Interrupt

This PCIE_PWR_STATE_PULSE interrupt is generated to let the software know of the power management events.The PCIE_PWR_STATE_PULSE interrupt is generated by aggregating the POWER_STATE_CHANGE_INTERRUPT and DPA_INTERRUPT outputs of the PCIe core.

In EP mode, software can check the PCIE_USER_LINKSTATUS[23-16] POWER_STATE_CHANGE_FUNCTION_NUM bit field to determine the physical function for which power state change occurred.

The PCIE_USER_PMCMD[2] POWER_STATE_CHANGE_ACK bit can be used to acknowledge the POWER_STATE_CHANGE_INTERRUPT.

12.2.2.4.4.7 ECC Aggregator Interrupts

The PCIE_ECC0_UNCORR_PULSE/PCIE_ECC0_UNCORR_LEVEL and PCIE_ECC0_CORR_PULSE/PCIE_ECC0_CORR_LEVEL interrupts are asserted by the CBA clock domain ECC Aggregator. The PCIE_ECC1_UNCORR_PULSE/PCIE_ECC1_UNCORR_LEVEL interrupts are asserted by the Core clock domain ECC Aggregator. The Core clock domain ECC Aggregator correctable interrupts are not exported since this aggregator is only connected to the error injection logic and the correctable interrupts for this module will never fire.

12.2.2.4.4.8 CPTS Interrupt

The PCIE CPTS_PEND_INT interrupt is asserted by the CPTS module in the PCIe subsystem to signal a TimeStamp event.

12.2.2.4.5 PCIe Subsystem DMA Support

The PCIe Subsystem has different requirements based upon whether it is operated in Root Complex (RC) or End Point (EP) mode. The PCIe subsystem does not have DMA capabilities built into it. It has internal target and controller ports connected to the device-level interconnect.

An external DMA engine can make burst data read/writes on the target port and the controller port on PCIe subsystem can initiate reads/writes to memory on behalf of a remote PCIe device.

The PCIe subsystem does not specify the DMA protocol that is used for data transfers. The software implementations on the two ends of the PCIe link implement a data transfer protocol that is compatible with each other.

As a result, there will be several software drivers required – one driver that will manage the PCIe subsystem in RC mode and another set of drivers that will run on the RC side and will manage each of the End Points connected to the PCIe subsystem RC.

Similarly, when PCIe subsystem is operating as an End Point, there are two drivers – one to manage the PCIe subsystem from the device side and another driver that will run on the device operating as the Root Complex.

12.2.2.4.5.1 PCIe DMA Support in RC Mode

When operating in Root Complex mode, a DMA controller internal to the device (outside PCIe subsystem) can perform DMA to and from any remote device located on the PCIe subsystem. The memory address of such devices is available to the software via the PCIe bus enumeration procedure. In addition, the PCIe subsystem has a provision to perform memory address translation on outbound requests. Thus, the software is able to map different memory regions in its memory map to correspond to different addresses (and different access types) on the PCIe side.

12.2.2.4.5.2 PCIe DMA Support in EP Mode

When operating as a PCIe End Point, the device will be located in PCIe memory map at location programmed in the Base Address Registers by the PCIe Root device. Any PCIe transactions destined for the device from the upstream ports will get transferred to the controller port on the PCIe subsystem. Similarly, any transactions originating from the software will be sent over to PCIe link.

In End Point mode, the PCIe subsystem provides address translation functionality. It is possible to map memory accesses originating on PCIe side to memory accesses with different address on the CBA bus side. These address ranges are configurable through application registers.

12.2.2.4.6 PCIe Subsystem Transactions

12.2.2.4.6.1 PCIe Supported Transactions

PCIe subsystem supports the following transactions:

1. Memory Read/Write in inbound/outbound direction in Root Complex (RC) and End Point (EP) modes.
2. I/O Read/Write in outbound direction in RC mode.
3. Configuration Read/Write in outbound direction in RC mode.
4. Configuration Read/Write in inbound direction in EP mode.
5. Message Transactions for interrupts and power management in RC and EP modes.

The following transactions are not supported:

1. Locked Read transactions and associated messages.
2. Inbound I/O Transaction Layer Packets (TLPs).

3. User defined messages.

12.2.2.4.6.2 PCIe Transaction Limitations

There are some limitations that must be adhered to while issuing transactions to PCIe subsystem internal bus interface.

- System Initialization

The PCIe subsystem operation is completely dependent upon the availability of the clock from the PLL that is inside the SERDES. All registers in the PCIe controller located in the core clock domain need the PLL to be in lock and properly configured. Register access transactions that are initiated before ensuring that the PLL is locked will result in a status error.

- Remote Configuration and I/O Requests

Since the remote configuration and I/O transaction windows are directly mapped to internal bus space, the software must care to not access these spaces when there is no operational PCIe link. No response may be generated for such transactions. It is recommended that checks be built into software to avoid remote accesses in the absence of an operational link.

- Byte Strobe Limitations

For any type of write transactions, the byte enables can only have a single unbroken string of 1s. In other words, in a transaction, if a byte’s write strobe is set, then all following bytes must have write strobe set until the last byte with write enabled. "Holes" or "Zeros" in between the byte enables are not allowed.

Since the internal bus width is greater that 32-bit, the TLP (Transaction Layer Packets) size will not be 1 (PCIe counts in 32-bit units) and therefore, it is through the FBE/LBE (First/Last Byte Enable) that the actual data transfer size is controlled.

- Burst Type Limitations

The PCIe core and respectively the PCIe subsystem does not support ‘fixed’ or ‘wrap’ burst types on its Target or Controller port. Transactions that require any burst type other than incremental burst type will result in unspecified behavior, possibly bus lock up.

- Transaction Address Alignment

The PCIe subsystem imposes a limitation of a maximum of 128-byte outbound read/write command. However, if the starting address is not aligned to an 8-byte boundary, then the maximum transaction size is reduced to 120 bytes. This limitation is placed to avoid arithmetic overflow in computing transaction length from CBA to AXI. Unspecified behavior will occur, if misaligned transactions in outbound direction are not limited to a maximum of 120 bytes.

- Read Interleaving

Read interleaving refers to the process of returning split read responses from multiple transactions. This implies that read data is not guaranteed to be sent in sequential order (data for one transaction to be sent completely before the next). The PCIe core will not interleave read responses, if the outbound read command/transaction size does not exceed the maximum transaction size configured in the PCIe core.

12.2.2.4.7 PCIe Subsystem Address Translation

The PCIe subsystem uses the address translation registers in the PCIe core to translate outbound system addresses to PCIe space and inbound PCIe address to a valid system address.

12.2.2.4.7.1 PCIe Inbound Address Translation

12.2.2.4.7.1.1 Root Complex Inbound PCIe to AXI Address Translation

The Root Complex inbound PCIe to AXI address translation is performed on memory and IO TLPs. The selection of which address translation registers to use in the translation process is dependent on the BAR match of the incoming TLP. In Root Complex mode there are 2 bars, so BAR0 and BAR1 registers are implemented. There is a BAR7 register which is used as a no match BAR address translation register. In Root Complex mode there are 2 bars but a BAR value of 7 will be indicated by HAL2AXI when BAR matching is disabled.

Any address that does not match the Root Complex BARs will be sent out as a BAR7 TLP. Each BAR register is implemented as two 32-bit registers which are named addr0 and addr1. The 'Root Complex Inbound PCIe to AXI Address Translation Logic' takes the upper bits from the 'Root Complex Inbound PCIe to AXI Address Translation Registers' and the lower bits are taken from the inbound PCIe address to form the AXI address. An addr0 [5:0] + 1 number of lower bits are passed from the inbound PCIe address to AXI address. In other words, the number of bits taken from inbound PCIe address is given by the addr0[5:0] + 1 value.

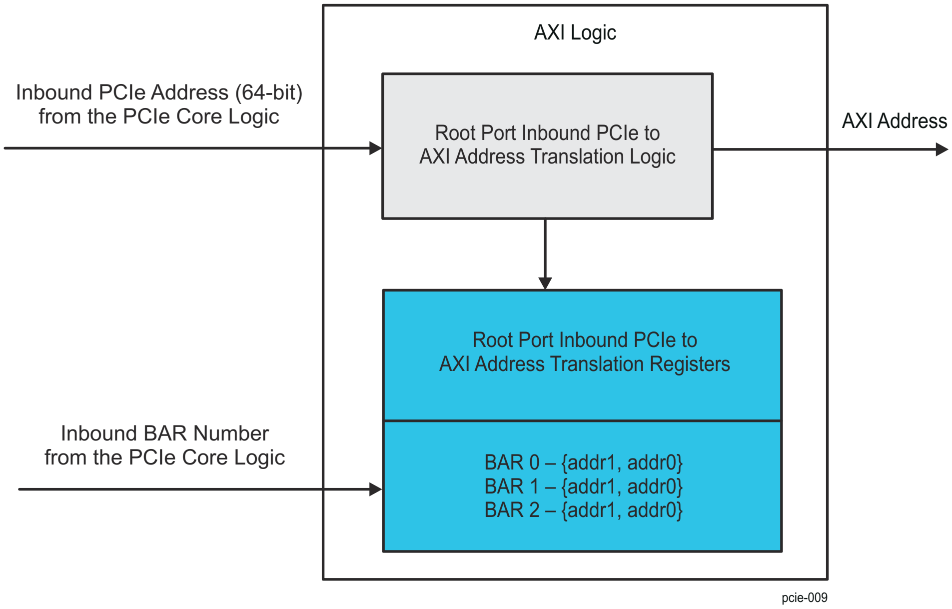

Figure 12-142. PCIE Root Complex Inbound PCIe to AXI Address Translation

A set of registers corresponding to one Root Complex BAR is shown in Table 12-202.

Table 12-214. PCIE Root Complex Inbound PCIe to AXI Address Translation Registers for one BAR

Register Name	Bits	Description	Default Value
addr1	31:0	Upper [63:32] bits of the AXI address.	32'd0
addr0	31:8	Lower [31:8] bits of the AXI address.	24'd0
	7:6	Reserved	2'd0
	5:0	Number of address bits passed through from PCIe to AXI. The PCIe controller passes the programmed value + 1 bits from PCIe to AXI. Minimum value to be programmed into this field is 7 as the lower 8 bits of the base address programmed in these registers (AXI) are replaced by zeros by the 'Root Complex Inbound PCIe to AXI Address Translation Logic'.	6'd0

12.2.2.4.7.1.2 End Point Inbound PCIe to AXI Address Translation

The End Point Inbound PCIe to AXI address translation is performed on memory and IO TLPs. The selection of which address translation registers to use in the translation process is dependent on the function number and BAR match of the incoming TLP. In End Point mode there are 7 bars per function, so 7 sets of registers are implemented per function, each BAR having two 32-bit registers (addr0 and addr1). The "End Point Inbound PCIe to AXI Address Translation Logic' takes the upper bits from the 'End Point Inbound PCIe to AXI Address Translation Registers' and the lower bits are taken from the Inbound PCIe Address to form the AXI address. The number of bits to pass from Inbound PCIe Address to AXI is decided by the Inbound BAR aperture.

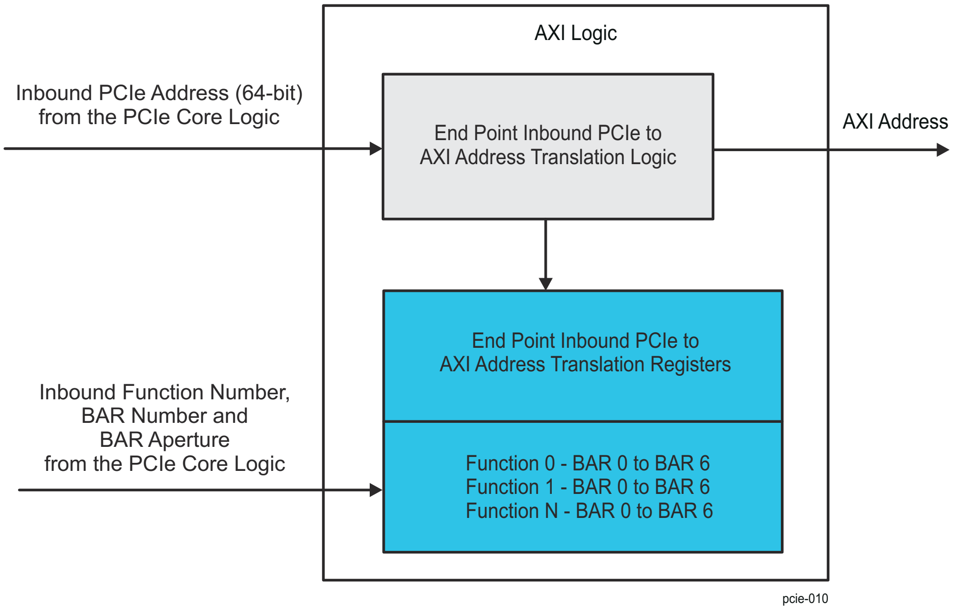

Figure 12-143. PCIE End Point Inbound PCIe to AXI Address Translation

A set of registers corresponding to one End Point BAR is shown in Table 12-203.

Table 12-215. PCIE End Point Inbound PCIe to AXI Address Translation Registers for one BAR

Register Name	Bits	Description	Default Value
[PF]_ib_ep_[BAR]_addr1 (where BAR can be bar0, bar1, bar2,...bar7, and PF can be pf0, pf1, pf2,... pf21)	31:0	Upper [63:32] bits of the AXI address.	32'd0
[PF]_ib_ep_[BAR]_addr0 (where BAR can be bar0, bar1, bar2,...bar7, and PF can be pf0, pf1, pf2,... pf21)	31:0	Lower [31:0] bits of the AXI address.	32'd0

12.2.2.4.7.2 PCIe Outbound Address Translation

The PCIe Subsystem allows mapping of PCIe addresses to/from the internal bus addresses of the device. This is accomplished by using internal address translation unit (iATU) in the PCIe core. For each outbound read/write request, the address translation module within PCIe subsystem can convert a VBUSM address to a PCIe address of memory Read/Write type.

If a transaction is large enough that it goes past the address translation region, unspecified behavior may occur. The address translation only works at the time a command is issued. So, a memory write, for example, will not automatically go to next translation region, if it starts in the previous one and is bigger than the remaining size in the starting translation region.

The “Dynamic Method: Sideband Descriptor Based” outbound address translation mechanism is used to bypass the outbound address translation unit under certain conditions. For more details on the bypass operation, see Section 12.2.2.4.7.2.1 , *PCIe Outbound Address Translation Bypass*.

12.2.2.4.7.2.1 PCIe Outbound Address Translation Bypass

The PCIe subsystem supports bypassing the outbound address translation in the PCIe controller when the *casel* value on the VBUSM target interface is non-zero.

The device DMA has the ability to send transactions to alternate address maps which are external to the local device. This is achieved by using casel identifier in the DMA descriptors. There are three requirements that need to be met in the PCIe subsystem when using this mode in the DMA, namely:

- Block transactions based on initiator credentials to support FFI (Freedom from Interference)
- Bypass the Address Translation Unit (ATU) inside the PCIe controller since the transaction address is external to the local device
- Assign the correct Bus, Device, Function (BDF) and Traffic Class (TC) values to the transaction

To meet these requirements, the PCIe subsystem uses the *cvirtid* values on the VBUSM target interface to filter transactions based on initiator credentials. The VMAP block in the PCIe subsystem has a *virtid* match register (PCIE_VMAP_OB_VIRTID_MATCH) and a set of 32 registers that can be used to program the descriptor fields when the ATU logic in the PCIe controller is bypassed.

The PCIe subsystem will filter outbound VBUSM target transactions that have a non-zero casel value. If the *cvirtid[11:5]* attribute of the VBUSM target transaction matches the value programmed in the PCIE_VMAP_OB_VIRTID_MATCH register, the credentials of the transaction initiator are verified. The *cvirtid[11:5]* value should also be non-zero for a successful match.

When the credentials match, the ATU of the PCIe controller is bypassed . The *cvirtid[4:0]* is used to select one of the 32 PCIE_VMAP_DESC_j descriptor registers. These registers can be programmed to assign the BDF and TC values to the outbound PCIe transaction. If the PCIE_VMAP_DESC_j[16] BD_EN0 register bit is set, then the bus, device and function numbers are all set from the external descriptor registers. If the BD_EN bit is not set, then the bus and device numbers are assigned by the PCIe controller using the values captured during enumeration. If ARI mode is enabled (in the PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG register), the function number uses the PCIE_VMAP_DESC_j[7:0] DEV_FUNC_NUM register field. If ARI mode is not enabled, the device number uses PCIE_VMAP_DESC_j[7:4] DEV_FUNC_NUM field and the function number uses the [3:0] DEV_FUNC_NUM field. The ARI mode is a PCIe controller hardware configuration option that is enabled for PCIe endpoints that support SR-IOV.

If the credentials of the initiator fail to match the programmed value in the PCIE_VMAP_OB_VIRTID_MATCH register, the VBUSM target transaction is then flushed by the bridge and is not submitted to the PCIe controller. The VBUSM2AXI2 bridge will return a protection error status for both read and write transactions. In addition, the write data is discarded and the correct number of read data phases with data value of zero are returned.

12.2.2.4.8 PCIe Subsystem Quality-of-Service (QoS)

The Virtual Channel/Transfer Class (VC/TC) feature in the PCIe core, in conjunction with the device system CBASS Quality-of-Service (QOS) capabilities, provide a mechanism for supporting differentiated QOS within the PCIe subsystem. The policy for traffic differentiation is determined by the Transfer Class (TC) and Virtual Channel (VC) mapping and VC-based arbitration mechanism.

A Virtual Channel is established when one or more TCs are associated with a physical resource designated by a VC ID. Every Traffic Class that is supported on a given path within the subsystem must be mapped to one of the enabled Virtual Channels. Every Port must support the default TC0/VC0 pair – this is “hardwired.” Any additional TC mapping or additional VC resource enablement is optional. The number of VC resources provisioned within a component or enabled within a given subsystem may vary due to implementation and usage model requirements.

The PCIe core in the PCIe subsystem is configured to support four virtual channels (4VC/4TC). For both ingress and egress traffic, VC3, the highest numbered virtual channel, has the highest priority.

For ingress traffic, the TC information from each transaction on the AXI controller information is mapped to the CCHANID signal of the VBUSM controller interface. The system level interconnect can use the CCHANID along with the ORDERID for QoS purposes. Table 12-204 shows the TC mapping to the 12-bit CCHANID of each VBUSM controller interface.

Table 12-216. PCIe Subsystem QoS Ingress CCHANID Mapping

TC Value	CCHANID[11:0]
0	{9’d0, 3’b000}
1	{9’d0, 3’b001}
2	{9’d0, 3’b010}

Table 12-216. PCIe Subsystem QoS Ingress CCHANID Mapping (continued)

TC Value	CCHANID[11:0]
3	{9’d0, 3’b011}
4	{9’d0, 3’b110}
5	{9’d0, 3’b101}
6	{9’d0, 3’b110}
7	{9’d0, 3’b111}

For egress traffic requiring the highest priority it should be mapped to VC=3 in the PCIe controller. The VC mapping is done using the AXI outbound descriptor registers in the PCIe controller.

12.2.2.4.9 PCIe Subsystem Precision Time Measurement (PTM)

The Precision Time Measurement (PTM) enables precise coordination of events across multiple components with independent local time clocks. Ordinarily, such precise coordination would be difficult given that individual time clocks have differing notions of the value and rate of change of time. To work around this limitation, PTM enables components to calculate the relationship between their local times and a shared PTM Controller Time: an independent time domain associated with a PTM Root.

The PTM defines the following components:

- PTM Requester - A Function capable of using PTM as a consumer associated with an Endpoint.
- PTM Responder - A Function capable of using PTM to supply PTM Controller Time associated with a RC.
- Time Source - A local clock associated with a PTM Responder.
- PTM Root – The source of PTM Controller Time for a PTM hierarchy. A PTM Root must also be a Time Source and is typically also a PTM Responder.

When using PTM between two components on a Link, the EP sends PTM requests to the RC on the same link. During each dialog, the RC populates the PTM Response message based on timestamps stored during previous PTM dialogs. Once each component has historical timestamps from the preceding dialog, the EP can combine its timestamps with those passed in the PTM Response message to calculate the PTM Controller Time.

The PCIe core implements all of the features required to handle the PTM conversation between the requestor and responder in hardware. In addition, an internal TimeStamp module (CPTS) is connected to the timestamp interface of the PCIe core so that events can be logged.

The Precision Time Measurement (PTM) support in the PCIe subsystem is handled by the combination of the PCIe core and the CPTS module.

The PCIe core controller handles the PCIe conversation to exchange timestamps between the RC and EP. It also includes logic to calculate the timestamp differences as specified in the PCIe standard. A 64-bit timer that is the controller clock is included in the PCIe core. The PCIe controller can be programmed to initiate the PTM conversation automatically by setting the [0] PTMRQM bit in the PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG register.

In EP mode, there are two methods to register a CPTS HW1 push timestamp that is needed to transfer the PCIe PTM timebase to the local system time base.

1. The first method involves the PTM_LOCAL_TIMER_OUT_VALID and PTM_EP_TIMER. The PTM_LOCAL_TIMER_OUT_VALID output from the PCIe controller will be asserted when the PTM conversation is complete and the EP local timer has been updated. The adjusted value of the EP 64-bit timer is available in the PTM_LOCAL_TIMER_OUT output of the controller. A second 64-bit free running timer, PTM_EP_TIMER, is used to shadow the value of the EP timebase. The PTM_EP_TIMER is loaded with the value of the PTM_LOCAL_TIMER_OUT[63:0] when PTM_LOCAL_TIMER_OUT_VALID is high. When PTM_LOCAL_TIMER_OUT_VALID is low, PTM_EP_TIMER will be free running based on the same PCIE CORE_CLK that drives the PTM_LOCAL_TIMER_OUT. The increment value of PTM_EP_TIMER can be adjusted by writing to the PCIE_USER_PTM_CFG[10-8] PTM_EP_TIMER_ADJ register field. The increment value is one by default. The value of the PTM_EP_TIMER will not be updated to the RC timebase until the first PTM dialog has occurred. Software can set the PCIE_USER_PTM_CFG[6-0] PTM_CLK_SEL register

field value between 0 and 63 to choose a particular bit of the PTM_EP_TIMER as the source for the CPTS HW1 time stamp push event.

2. The second method to register the CPTS HW1 push timestamp involves only the PTM_LOCAL_TIMER_OUT_VALID output from the PCIe controller. Software can set the PCIE_USER_PTM_CFG[6-0] PTM_CLK_SEL register field value to 64 to select the PTM_LOCAL_TIMER_OUT_VALID as the source of the CPTS HW1 time stamp push event. This will create a CPTS HW1 timestamp when there is a PTM dialog between the PCIe End Point and Root Complex. The actual value of the EP PTM local timer can be read from the PCIE_USER_PTM_TIMER_LOW and PCIE_USER_PTM_TIMER_HIGH registers.

In RC mode, the CPTS can take control of the PTM controller time. The 64-bit CPTS timer is continuously loaded into the PCIe PTM controller clock by tying high the PTM_TIMER_IN_VALID input of the PCIe controller. This allows for software to adjust the PCIe PTM controller clock as necessary using the CPTS module and maintain the PTM controller time by monotonically increasing it as required by the PCIe standard. The CPTS HW1_PUSH timestamp input is driven by the particular bit of the PTM_LOCAL_TIMER_IN counter, as selected by the value in the PCIE_USER_PTM_CFG[6-0] PTM_CLK_SEL register field.

The reference clock (RCLK) for the CPTS can be controlled via the CTRLMMR_PCIE0_CLKSEL[2-0] CPTS_CLKSEL register field in the device Control Module. This enables the SoC flexibility in choosing the CPTS reference clock input. In RC mode, the RCLK needs to be connected to the SERDES PIPE clock since the CPTS will be driving the PTM controller clock. For more information on the RCLK source clock selection, see *PCIe Subsystem Integration*.

Table 12-217. PHY Latency Parameters for PTM

	PHY Logic Latency	PHY Analog Latency	Total PHY Latency
Gen1 Transmit Latency	112ns	26.8ns	138.8ns
Gen2 Transmit Latency	56ns	13.4ns	69.4ns
Gen1 Receive Latency	160ns	25.2ns	185.2ns
Gen2 Receive Latency	80ns	12.6ns	92.6ns

Figure 12-144 shows the PTM support logic in the PCIe subsystem.

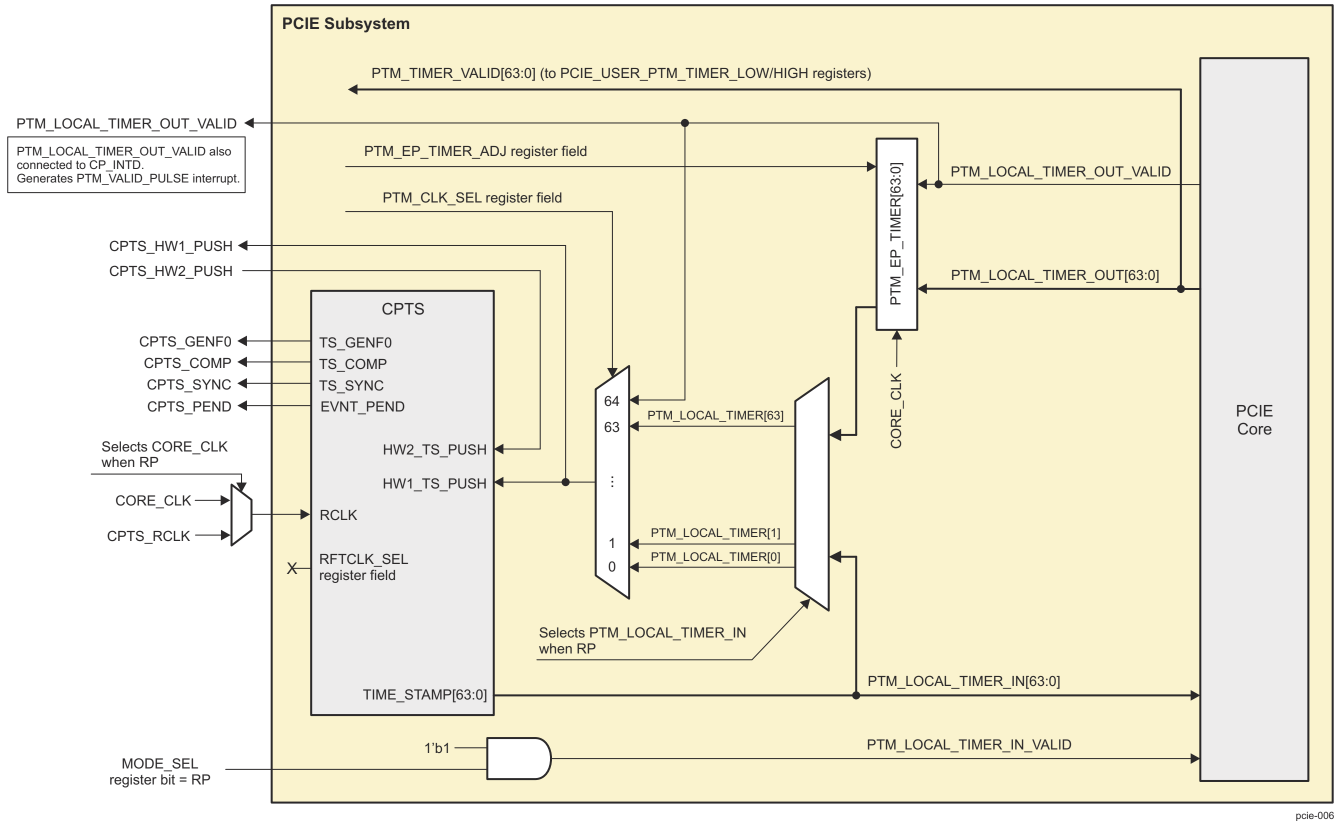

Figure 12-144. PCIe Subsystem PTM Implementation

12.2.2.4.10 PCIe Subsystem Loopback

The PCIe subsystem provides loopback support through PIPE interface (Link Layer).

12.2.2.4.10.1 PCIe Loopback

The procedure depends upon whether the device is operating in RC or EP Mode. In either case, the PCIe subsystem can be loopback initiator or loopback target as outlined in PCIe specifications. A loopback initiator is the component requesting loopback and transmitting the data. A loopback target is the component looping back the data.

12.2.2.4.10.1.1 PCIe Loopback Initiator Mode

The loopback path when PCIe subsystem is loopback initiator is:

PCIe subsystem (loopback initiator) -> PIPE (TX) -> PCIe Link -> Loopback -> PCIe Link -> PIPE (RX) -> PCIe subsystem

12.2.2.4.10.1.2 PCIe Loopback Target Mode

The loopback path when PCIe subsystem is loopback target is:

Remote device -> PCIe Link -> PIPE (RX) -> Loopback -> PIPE (TX) -> PCIe Link -> Remote device

If the PCIe subsystem is a loopback target, then the incoming serial data is routed back to the originating device from the PIPE interface as per PCIe loopback requirements. Typically, PCIe test equipment will be used as loopback initiator and it will transition PCIe subsystem into loopback target state following which, the inbound transactions will be looped back to the test equipment.

12.2.2.4.11 PCIe Subsystem Error Handling

As an End Point, PCIe subsystem reports errors to root complex so that corrective action may be taken. These messages become error interrupts on the Root Complex side. In addition, the errors that are detected by the PCIe subsystem locally are also reported to software via interrupts.

Note that for several errors of the same type that are detected in close succession, the PCIe subsystem will not necessarily send as many error messages to Root Complex. It is guaranteed to send at least one such error message.

12.2.2.4.12 PCIe Subsystem Internal Diagnostics Features

12.2.2.4.12.1 ECC Aggregators

The PCIe subsystem instantiates two ECC Aggregators: AXI_ECC_AGGR and CORE_ECC_AGGR.

AXI_ECC_AGGR is connected to the RAMs in PCIe CBA Clock Domain and CORE_ECC_AGGR is connected to the RAMs in the PIPE Clock Domain.

The ECC Aggregator modules integrated within the PCIe subsystem provide a mechanism to control and monitor the ECC RAMs via Single Error Correction (SEC) and Double Error Detection (DED) functions. Each ECC Aggregator module gathers level pending status from the ECC RAMs into two interrupts to system level. One interrupt is for correactable errors (SEC) and the other one for uncorrectable errors (DED). The ECC Aggregator supports software readable status of ECC single/double-bit errors and associated information such as RAM address and data bit(s) that are in error. Write back correction for async read RAMs is not supported.

For more information on the ECC Aggregator operation, see *ECC Aggregator*.

12.2.2.4.12.2 RAM ECC Inversion

The RAM ECC logic inside the PCIe controller can be tested using the ECC inversion logic.

12.2.2.5 PCIe Subsystem Registers

This section describes the PCIe Subsystem registers.

12.2.3 Serializer/Deserializer (SerDes)

This section describes the Serializer/Deserializer (SerDes) in the device.

12.2.3.1 SerDes Overview

SerDes'es goal is to convert device (SoC) parallel data into serialized data that can be output over a high-speed electrical interface. In the opposite direction, SerDes converts high-speed serial data into parallel data that can be processed by the device. To this end, the SerDes contains a variety of functional blocks to handle both the external analog interface as well as the internal digital logic.

Most important building blocks of SerDes are:

- Physical Media Attachment (PMA):
  - Lanes: The lanes handle all inputs and outputs from the serial interface, and contain the Tx/Rx I/Os, serializer/deserializer, and Clock and Data Recovery (CDR) unit.
  - Common module (CMN): The CMN handles peripheral and Tx clocking of the SerDes. It consists of internal PLLs and external reference clock input buffer, reset, and startup circuitry.
- Physical Coding Sub-block (PCS): The PCS is responsible for translating data from/to the parallel interface, as well as data encoding/decoding and symbol alignment.
- WIZ: The WIZ acts as a wrapper for the SerDes, and can both send control signals to and report status signals from the SerDes, and muxes SerDes to peripherals.

The device contains these SerDeses:

Table 12-218. SerDes Allocation Within Device Domains

Module Instance	Domain	
	MCU	MAIN
SERDES0	-	✓

Figure 12-145 shows SERDES0 highlights.

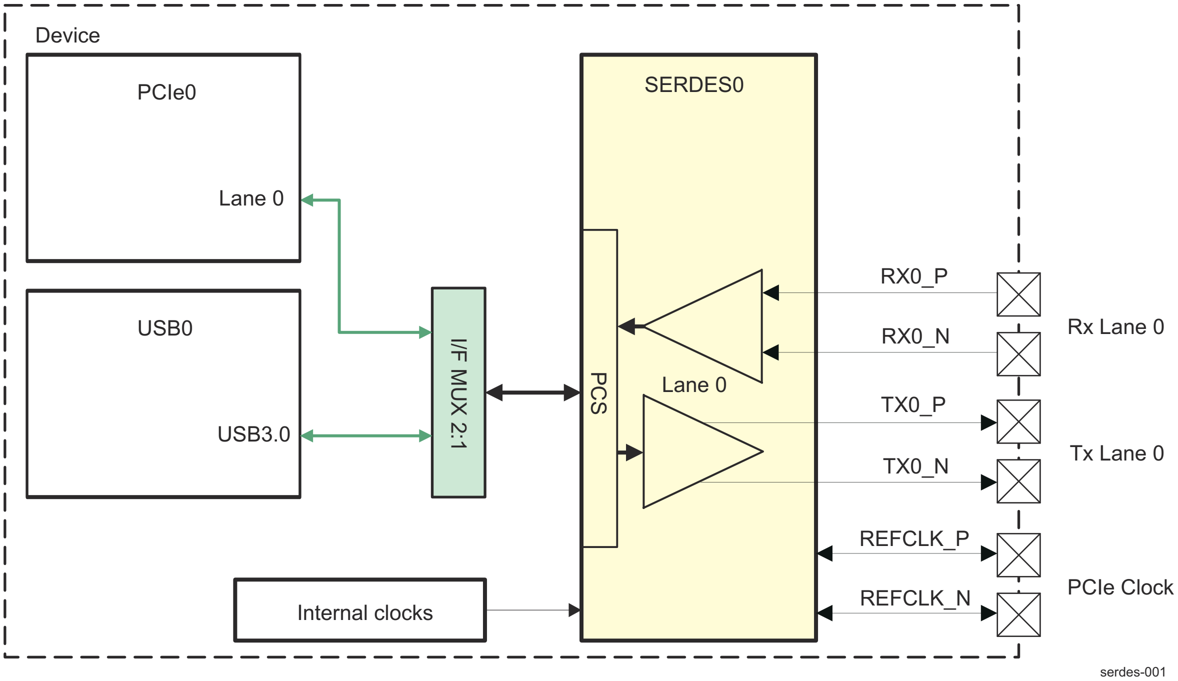

Figure 12-145. SERDES0 Overview

12.2.3.1.1 SerDes Features

The SERDES module features include:

- Single lane PHY containing:
  - Transmit and Receive I/Os

  - Serializer
  - Deserializer
  - Clock and data recovery (CDR) unit
- Common Module (CMN)
  - PLLs
  - Controller bias
  - Automatic calibration of pin termination resistors
  - Reference clock input buffers
  - Reset and startup management
- Physical Coding Sub-block (PCS)
  - USB3.1 Gen 1 (5 Gbps)
  - PCIe Gen 1 (2.5 Gbps), Gen 2 (5 Gbps)
  - QSGMII Specification revision 1.2
  - Symbol alignment
  - Selectable serial pin polarity reversal for both transmit and receive paths
  - Bit stream reordering
- Physical Media Attachment (PMA) layer
  - Transmit equalization
  - Receive equalization
  - Supports on-the-fly eye and bathtub curve diagramming with 8-bit voltage amplitude resolution and up to 1/64 UI time resolution
  - Data path BIST with programmable pattern generation and error detection
  - Serial bit stream and parallel word loopback for both line and parallel side
  - 8-bit ADC provides digitized ATB measurement results
  - Supports DC and AC JTAG (boundary scan) per IEEE 1149.6

The SERDES mux (WIZ) module supports the following features:

- Multiplexes device interfaces onto a single SERDES lane (Tx and Rx)
- Provides registers to implement SERDES control and status functions and alignment delays
- Clock generator block for providing MAC transmit clock
- Rx comma align block
  - Performs de-stuffing the Rx data stream in the event that the Rx rate is different from the Tx rate
  - Supports comma detection that is not sensitive to false commas using all 8b/10b character combinations

12.2.3.1.2 Not Supported Features

All features described in this chapter are supported.

12.2.3.1.3 Industry Standards Compatibility

All SerDes interfaces are configured as point-to-point connections. It is assumed that the connection is made between the SoC and another device that is compliant to the appropriate industry standard. The list of supported standards is given below.

This chapter deals with the physical layer and, therefore, it is the electrical specifications in these standards that are relevant. For more information regarding protocol compliance [1], see the device-specific Datasheet.

- PCIe is electrically compliant with Base specification revision 4.0.
- USB is electrically compliant with USB 3.1.

Table 12-219. SerDes Supported Standards

Standard	Bit Rate (Gbps)	Reference Clock Frequency (MHz)	Bus Width (bits)
PCI Express 4.0 Gen1	2.5	19.2, 20, 24, 25, 26, 27, 100	8
PCI Express 4.0 Gen2	5.0	19.2, 20, 24, 25, 26, 27, 100	16
USB 3.1 Gen1 SuperSpeed	5.0	19.2, 20, 24, 25, 26, 27, 100	16

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[1] Electrical compatibility does not guarantee interoperability with devices

12.2.3.2 SerDes Environment

12.2.3.2.1 SerDes I/Os

Figure 12-146 shows the I/O interface signals of SERDES.

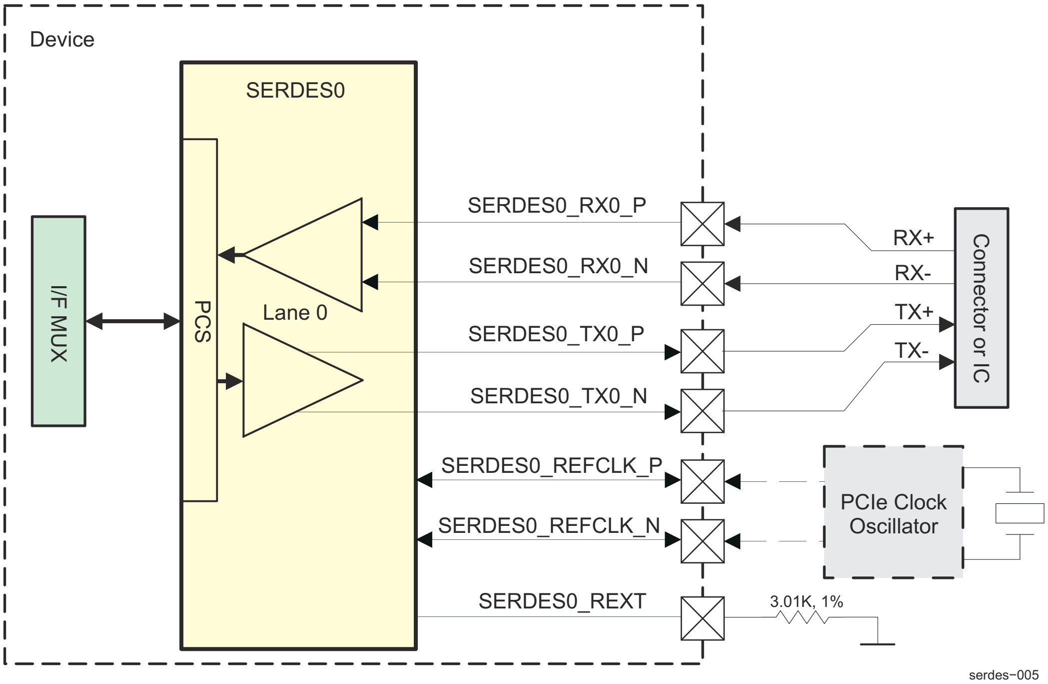

Figure 12-146. SerDes Environment

Note

Although containing some of the basic external components, Figure 12-146 must not be considered as an exhaustive guide for the PCB designer. TI provides additional documents for those who are willing to design PCBs and/or fine tune the SerDes.

Table 12-208 describes the external signals of SERDES0 module.

Table 12-220. SERDES0 Input/Output Description

Device Pin	Module Signal	I/O(1)	Description	Value at Reset
SERDES0_RX0_P	RX_P_LN0	I	SerDes differential data receive pins	HiZ
SERDES0_RX0_N	RX_M_LN0	I		HiZ
SERDES0_TX0_P	TX_P_LN0	O	SerDes differential data transmit pins	HiZ
SERDES0_TX0_N	TX_M_LN0	O		HiZ
SERDES0_REFCLK0P	CMN_REFCLK_P	I/O	SerDes external PCIe reference clock	HiZ
SERDES0_REFCLK0N	CMN_REFCLK_N	I/O		HiZ
SERDES0_REXT	CMN_REXT	A/I	PMA external calibration resistor. Requires a 3.01 kOhm ±1% accurate off-chip resistor connected from this pin to ground.	HiZ

(1) I = Input; O = Output; A = Analog

12.2.3.3 SerDes Integration

Figure 12-147 shows the integration of the SERDES0 module in the device.

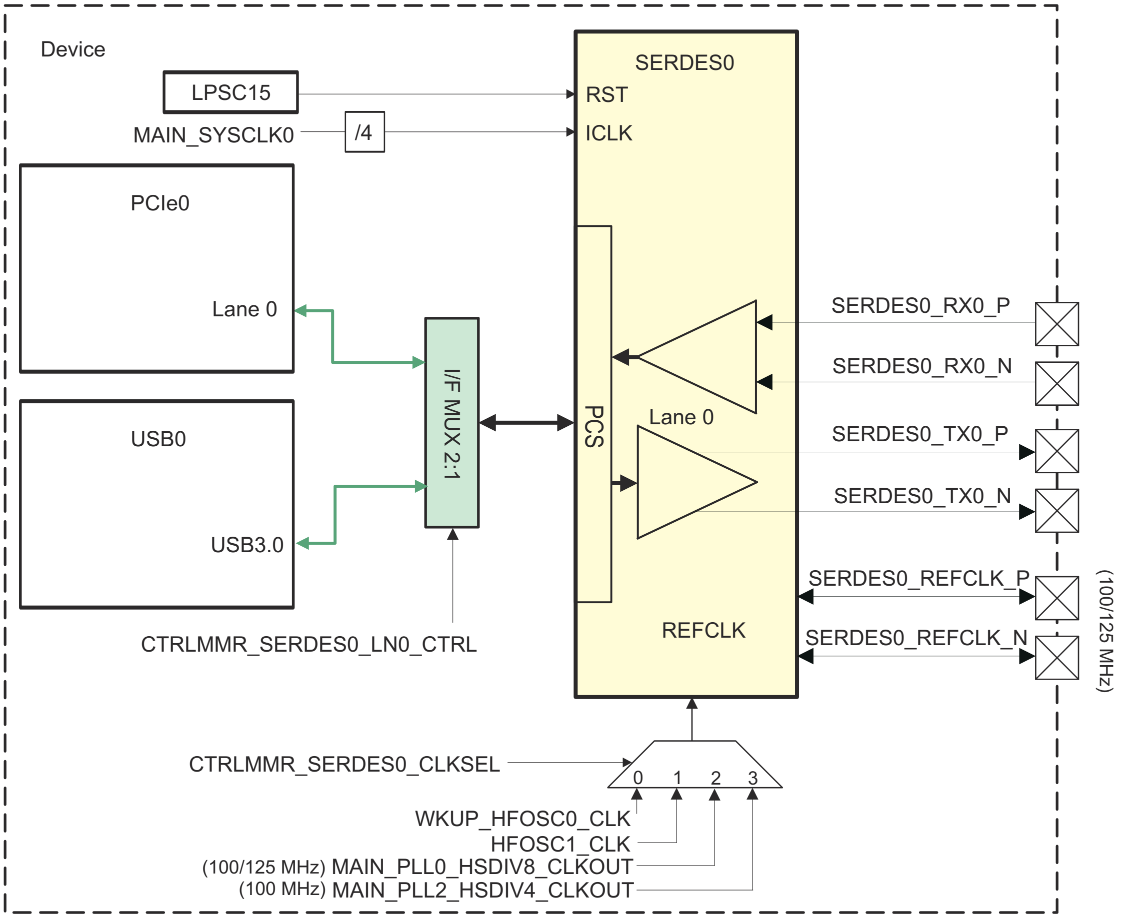

serdes–006

Figure 12-147. SERDES0 Integration

Table 12-209 through Table 12-212 summarizes the integration of SerDes in device MAIN domain.

Table 12-221. SerDes Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
SERDES0	PSC0	PD0	LPSC15	CBASS0

Table 12-222. SerDes Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
SERDES0	SERDES0_ICLK	MAIN_SYSCLK0/4	PLL_CTRL0	VBUS interface clock
	CMN_REFCLK_INT	WKUP_HFOSC0_CLKOUT	WKUP_HFOSC0	Internal reference clock from device sources. Software selectable. See Section 12.2.3.3.1.2
		HFOSC1_CLKOUT	HFOSC1	
		MAIN_PLL0_HSDIV8_CLKOUT	PLL0	
		MAIN_PLL2_HSDIV4_CLKOUT	PLL2	

Table 12-223. SerDes Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
SERDES0	SERDES0_RST	MOD_G_RST	LPSC15	Serdes LPSC reset

Table 12-224. SerDes Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
SERDES0	PHY_PWR_TIMEOUT_LVL_0	GICSS0_SPI_IN_142	GICSS0	Lane power timeout interrupt	Level
		R5FSS0_CORE0_INTR_IN_180	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_180	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_180	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_180	R5FSS1_CORE1		

Table 12-225. SerDes DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Description	Type
SERDES0	-	-	-	No PDMA channels to external DMA engines	-

12.2.3.3.1 WIZ Settings

This section describes the quazi-static settings that software must perform after global resets. These settings are made via registers in the CTRL_MMR0 module. For CTRL_MMR0 description, please refer to *Control Module (CTRL_MMR)*.

12.2.3.3.1.1 Interface Selection

SerDeses provide PHY functions for the following high-speed interfaces:

- PCIe0 (one lane)
- USBSS0 (USB3.1 Gen 1)

Table 12-214 describes the interface combinations supported by SERDES0.

Table 12-226. SERDES0 Supported Configurations

Interface Alias	CTRLMMR_SERDES0_LN0_CTRL [1:0]	
	LANE_FUNC_SEL	Interface on Lane 0
IP1	0x0	PCIe0 Lane 0
IP2	0x1	USBSS0
IP3	0x2	-
IP4	0x3	-

12.2.3.3.1.2 Internal Reference Clock Selection

Table 12-215 describes the internal reference clock options for SERDES0.

Table 12-227. SerDes Internal Reference Clock Selection

CTRLMMR_SERDES0_CLKSEL	
[1:0] CLK_SEL	Internal Clock to SERDES Core
0x0	WKUP_HFOSC0_CLKOUT
0x1	HFOSC1_CLKOUT
0x2	MAIN_PLL0_HSDIV8_CLKOUT
0x3	MAIN_PLL2_HSDIV4_CLKOUT

12.2.3.4 SerDes Functional Description

12.2.3.4.1 SerDes Block Diagram

Figure 12-148 is a top-level, non-exhaustive diagram of SerDes and WIZ wrapper. Note that only one (Tx + Rx) lane is shown.

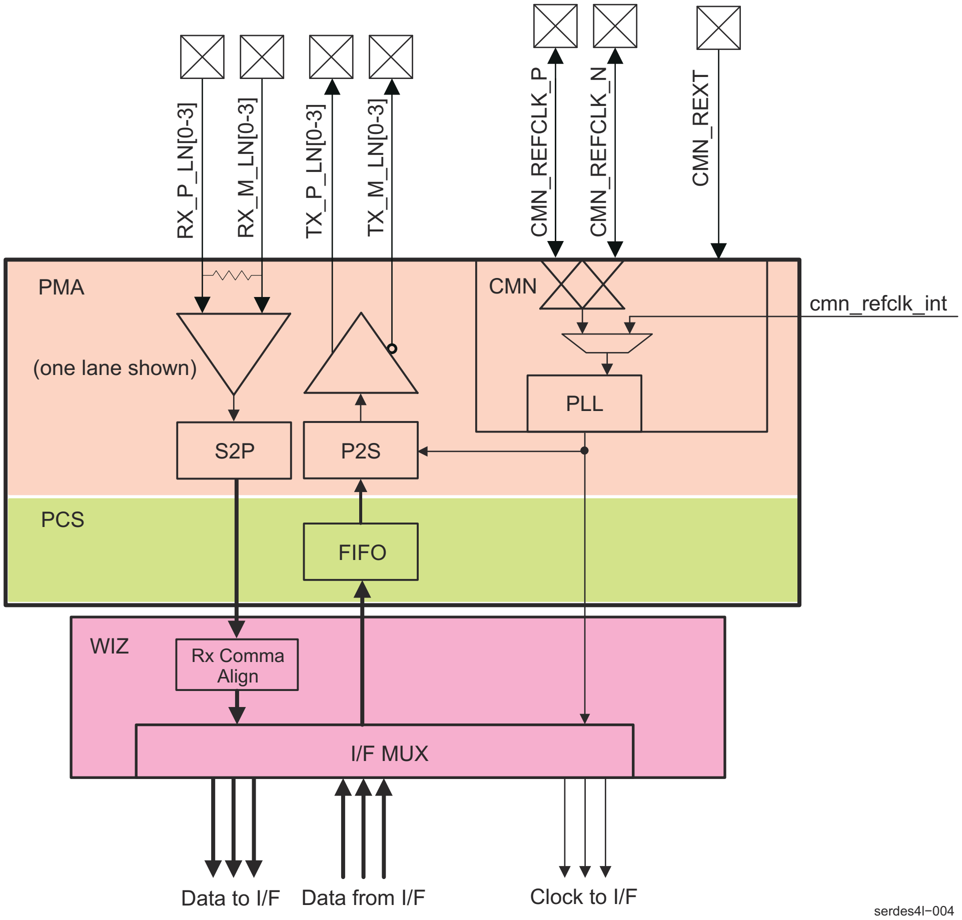

Figure 12-148. SerDes and WIZ Block Diagram

Building blocks of SerDes include:

- Lanes: The lanes handle all inputs and outputs from the serial interface, and contain the Tx/Rx I/Os, serializer/deserializer (P2S/S2P), and Clock and Data Recovery (CDR) unit. Each SerDes contains one Tx and Rx lane.
- Common module (CMN): The CMN handles peripheral and Tx clocking of the SerDes. It consists of internal PLLs and external reference clock input buffer, reset, and startup circuitry.
- Lanes and CMN are parts of the Physical Media Attachment (PMA) layer.
- Physical Coding Sub-block (PCS): The PCS is responsible for translating data from/to the parallel interface, as well as data encoding/decoding and symbol alignment.
- WIZ: The WIZ acts as a wrapper for the SerDes, and can both send control signals to and report status signals from the SerDes (register interface), and muxes SerDes to peripherals (USB, PCIe, and others).

12.2.4 Universal Serial Bus Subsystem (USBSS)

This section describes the Universal Serial Bus Subsystem (USBSS) in the device.

Note

This chapter serves to describe the integration of the third-party USB controller and should not be considered sufficient for those wishing to modify the existing Linux or RTOS USB driver(s) or create a new driver to support this controller implementation. For those who do wish to substantially modify the existing Linux or RTOS USB driver(s), or create new drivers, contact TI for more information on how to obtain the third-party documentation under NDA.

12.2.4.1 USB Overview

The USB 3.1 Gen1 Interface is a general-purpose cable bus, supporting data exchange between a host device and a wide range of simultaneously accessible peripherals, similar to previous versions of USB.

The device supports one USB subsystem integrated in the MAIN domain :

- USB3SS0 is SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with on-chip SS (USB3.0) PHY and HS/FS/LS [2](USB2.0) PHY

Table 12-228. USB Allocation Within Device Domains

Module Instance	Domain	
	MCU	MAIN
USB3SS0	-	✓

Figure 12-149 shows the USB subsystem highlights.

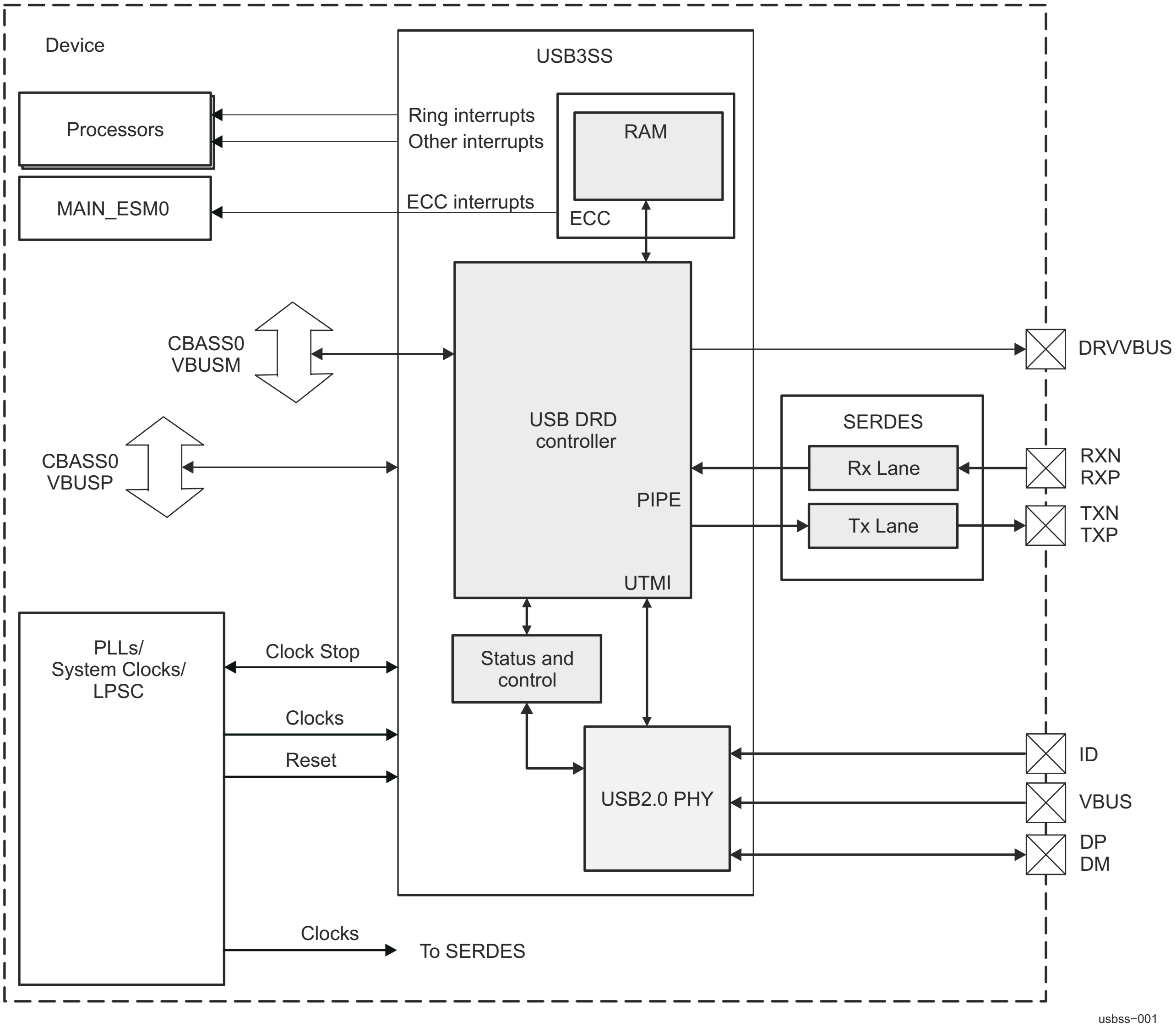

Figure 12-149. USB Subsystem Overview

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[2] LowSpeed (LS) is supported only in host mode.

12.2.4.1.1 USB Features

The USB subsystem supports the following USB Features:

- USB interface:
  - Compliant with USB 3.1 Gen1 specification
  - Compliant with xHCI 1.0 specification
  - Limited USB 2.0 on-the-go support
  - High speed (480 Mbps), and full speed (12Mbps) Device
  - SuperSpeed (5 Gbps), high speed (480 Mbps), full speed (12Mbps), and low speed (1.5 Mbps) Host
  - Single USB2.0 port
  - Single USB3.1 port
  - USB2 L1/L2 support
  - USB3 U1/U2/U3 support
- Dual mode operation:
  - Support for static host mode or static device mode based on software configuration.
  - Programmable runtime mode change
  - OTG 2.0 host negotiation protocol (HNP) support
- Host mode:
  - 64 slots supported
  - Up to 32 endpoints per slot
  - 256 primary streams supported
  - Root hub functionality
- USB2 PHY:
  - Fully compliant with UTMI+ Level 3 specification revision 1.0
  - Supports high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) data rates
  - Supports battery charging BC1.2v specification
  - Supports host, peripherals and OTG 2.0 (dual role device) applications
  - Supports D+/D- lane reversal for flexible board integration
  - Supports USB low-power states; namely, suspend and link power management (LPM)
  - Supports internal comparators for monitoring OTG voltage thresholds
  - Supports multiple PLL reference clocks
  - Supports internal PLL for high-speed (480 MHz) clock and data recovery (CDR) operation
  - Integrated termination resistors (45 Ω, 1.5 KΩ, and 15 KΩ)
  - Supports built-in self-test (BIST) for production testing
  - 3.3-V ESD support on VBUS

12.2.4.1.2 USB Not Supported Features

The following are USB features which are not supported by the hardware integration of the current device:

Table 12-229. USB3SS Unsupported Features

Feature	Reason
Virtualization (SRIOV or xHCI-IOV or ARM SMMU)	No Support
SuperSpeed (5 Gbps) Device Mode	No Support
Debug Trace for USB	No Support
Attach Detection Protocol (ADP)	This function is not possible because the USB2 PHY implements 3.3v ESD on the VBUS pin.
5 volt compatible VBUS pin	This function is not possible because the USB2 PHY implements 3.3v ESD on the VBUS pin. Note: The VBUS signal should be applied to a 20k/10k voltage divider which divides the potential by 3. This allows the VBUS signal to go up to 10.75 volts before exceeding the VBUS pin maximum of 3.63 volts.
NRDY Event TRB, when operating in host mode	NRDY Event TRB is not supported when operating in host mode.
Halt Endpoint Command TRB, when operating in host mode	Halt Endpoint Command TRB is not supported when operating in host mode.

Table 12-229. USB3SS Unsupported Features (continued)

Feature	Reason
OTG Protocol, for USB Type-C applications	OTG Protocol is not supported for USB Type-C applications.
Light HC Reset Capability (LHRC)	No Support
xHCI Debug Capability (Debug Port)	No Support
xHCI Save and Restore Operations	No Support
HIMD, when operating in host mode	No Support
Latency Tolerance Messaging	Set Latency Tolerance Value Command is not supported
Negotiate Bandwidth Command	No Support
Number of slots limited to 64	Total for USB2 and USB3
Number of active periodic endpoints limited to 96, when operating in host mode	No Support
Smart ISO	Deprecated in USB 3.2 specification
Secondary Streams	No Support
PTM, when operating in device mode	No Support

12.2.4.1.3 USB Terminology

The following acronyms and abbreviations are related to USB.

Term	Definition
ADP	Attach Detection Protocol: detects USB OTG attach/detach events.
DRD	Dual Role Device: USB Host and Peripheral capable.
DS	Down Stream (A USB port facing from a Host or Hub to a Device/Peripheral).
EP	Endpoint: USB communication channel between the USB link partners carrying a single transfer type (BULK, ISOCH, INT, or CONTROL) and bus sharing arbitration scheme.
FS	Full-Speed USB data rate (12 Mbps).
HNP	Host Negotiation Protocol, OTG extension to swap USB host and peripheral roles.
HS	High-Speed USB data rate (480 Mbps).
ITP	Isochronous Timestamp Packet: USB SS micro-frame boundary packets.
LMP	Link Management Packet.
LS	Low-Speed USB data rate (1.5 Mbps).
OTG	On-The-Go extension to USB protocol.
PHY	Physical Layer Device.
SS	Super-Speed USB data rate. 5 Gbps (USB3.0 or USB3.1 Gen1)
US	Upstream facing from a device (or hub) to the host (or a hub).
USB IF	USB Implementers Forum. The governing organization that develops and maintains the USB specifications and compliance standard. http://www.usb.org
xHC	Host Controller, designates the USB hardware that implements the xHCI specification.
xHCI	eXtensible Host Controller Interface. The specification that defines the register level interface for host controller.

12.2.4.2 USB Environment

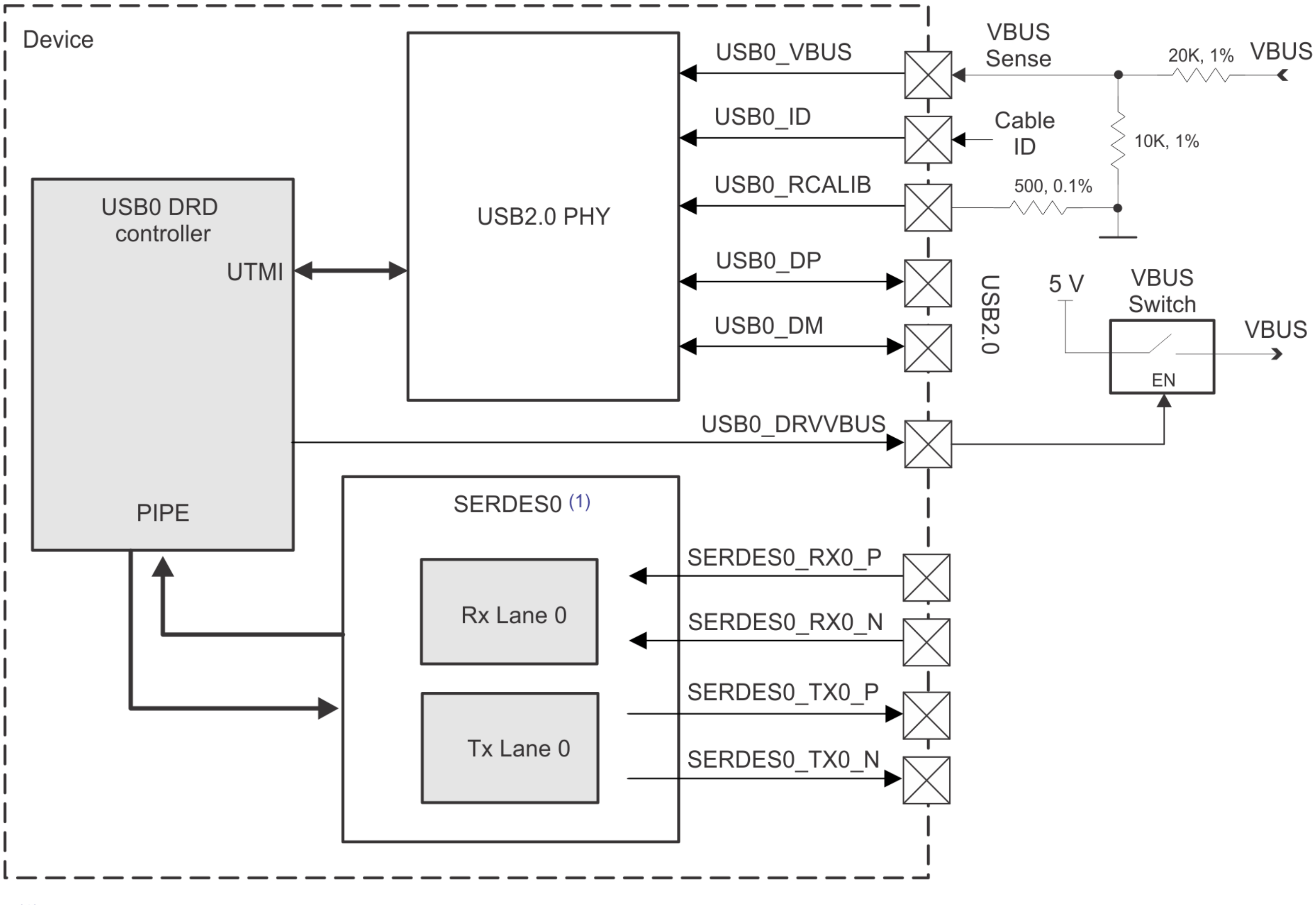

(1) See section *SerDes* for details

usbss−003

Figure 12-150. USB3SS0 Subsystem Environment

12.2.4.2.1 USB I/Os

Table describes the external signals of the USB3SS0 module.

Table 12-230. USB3SS0 Input/Output Description

Device Pin	Module Signal	I/O	Description	Value at Reset
USB0_DP	DP	I/O	DP to USB connector	HiZ
USB0_DM	DM	I/O	DM to USB connector	HiZ
USB0_ID	ID	A/I	ID to USB connector	HiZ
USB0_VBUS	VBUS	A/I	VBUS to USB connector	HiZ
USB0_RTRIM			USB2 PHYreference resistor	
USB0_DRVVBUS	DRVVBUS	O	3.3 Volt LVCMOS Output. Controls VBUS power switch	0
The following pins are implemented through SERDES				
USB0_SSRXN		I	N of differential receive data	HiZ
USB0_SSRXP		I	P of differential receive data	HiZ
USB0_SSTXN		O	N of differential transmit data	HiZ

Table 12-230. USB3SS0 Input/Output Description (continued)

Device Pin	Module Signal	I/O	Description	Value at Reset
USB0_SSTXP		O	P of differential transmit data	HiZ
USB0_REFCLKN		I	N of differential reference clock	HiZ
USB0_REFCLKP		I	P of differential reference clock	HiZ
USB0_REXT			SERDES reference resistor	

12.2.4.2.2 USB Subsystem Application

As the USB controller modules present in this device are DRD (Dual-Role Devices), they can support operation as either a USB Host or a USB Device. The operational mode determination is made based on the state of the USBn_ID pin; when this pin is grounded, the controller will operate as a USB Host, when this pin is left floating, the controller assumes the role of a USB Device. For implementations that do not require DRD functionality, the USBn_ID pin can either be left floating or can be grounded in the board design depending on the static role required. For implementations that do require DRD functionality, the USBn_ID pin should be connected directly to the corresponding ID pin on a USB Micro-AB socket. In doing so, the USBn_ID pin will be correctly terminated (open or grounded) depending on the cable attached and the controller will enter Host or Device mode accordingly.

12.2.4.2.3 VBUS Sense

The VBUS voltage needs to be monitored for detection of the various valid signals (AVALID, BVALID, and SESSEND).

The voltage of the VBUS signal is scaled down using an external resistor divider (as shown in Figure 12-1796), to limit the voltage applied to the VBUS pin. A zener diode is used to clamp the maximum intermediate voltage to 6.8 volts. The tolerance of resistors used must be less than 1%. The leakage current of the zener diode must be less than 100 nA at 5 V.

12.2.4.3 USB Integration

This section describes USB module integration in the device, including information about clocks, resets, and hardware requests.

12.2.4.3.1 Resets, Interrupts, and Clocks

Table 12-231. USB Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
USB0	MAIN	GP_CORE_CTL	LPSC_USB	6	OFF	YES	

Table 12-232. USB Resets

Module Instance	Source	Description
USB0	GP_CORE_CTL	USB0 Reset

Table 12-233. USB Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
USB0	USB0_a_ecc_aggr_corrected_err_level_0	ESM0_esm_lvl_event_IN_35	ESM0	USB0 interrupt request	level

Table 12-233. USB Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
	USB0_a_ecc_aggr_uncorrected_err_level_0	ESM0_esm_lvl_event_IN_111	ESM0	USB0 interrupt request	level
	USB0_asf_int_fatal_0	ESM0_esm_lvl_event_IN_142	ESM0	USB0 interrupt request	level
	USB0_asf_int_nonfatal_0	ESM0_esm_lvl_event_IN_143	ESM0	USB0 interrupt request	level
	USB0_host_system_error_0	GICSS0_spi_IN_219	GICSS0	USB0 interrupt request	level
		R5FSS0_CORE0_intr_IN_219	R5FSS0_CORE0	USB0 interrupt request	level
		R5FSS0_CORE1_intr_IN_219	R5FSS0_CORE1	USB0 interrupt request	level
		R5FSS1_CORE0_intr_IN_219	R5FSS1_CORE0	USB0 interrupt request	level
		R5FSS1_CORE1_intr_IN_219	R5FSS1_CORE1	USB0 interrupt request	level
	USB0_irq_[7:0]	GICSS0_spi_IN_[227:220]	GICSS0	USB0 interrupt request	level
		R5FSS0_CORE0_intr_IN_[227:220]	R5FSS0_CORE0	USB0 interrupt request	level
		R5FSS0_CORE1_intr_IN_[227:220]	R5FSS0_CORE1	USB0 interrupt request	level
		R5FSS1_CORE0_intr_IN_[227:220]	R5FSS1_CORE0	USB0 interrupt request	level
		R5FSS1_CORE1_intr_IN_[227:220]	R5FSS1_CORE1	USB0 interrupt request	level
	USB0_otgirq_0	GICSS0_spi_IN_228	GICSS0	USB0 interrupt request	level
		R5FSS0_CORE0_intr_IN_228	R5FSS0_CORE0	USB0 interrupt request	level
		R5FSS0_CORE1_intr_IN_228	R5FSS0_CORE1	USB0 interrupt request	level
		R5FSS1_CORE0_intr_IN_228	R5FSS1_CORE0	USB0 interrupt request	level
		R5FSS1_CORE1_intr_IN_228	R5FSS1_CORE1	USB0 interrupt request	level

Table 12-234. USB Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
USB0	ACLK_CLK	MAIN_SYSCLK0/2		
	CLK_LPM_CLK	MAIN_PLL1_HSDIV4_CLKOUT		

Table 12-234. USB Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
	PCLK_CLK	MAIN_SYSCLK0/4		
	USB2_APB_PCLK_CLK	MAIN_SYSCLK0/4		USB2PHY VBUSP interface clock
	USB2_REFCLOCK_CLK	HFOSC0_CLKOUT	USB0_CLKSEL[0:0]	USB2PHY reference clock.
		MAIN_PLL2_HSDIV4_CLKOUT		

12.2.4.4 USB Functional Description

Note

This chapter serves to describe the integration of the third-party USB controller and should not be considered sufficient for those wishing to modify the existing Linux or RTOS USB driver(s) or create a new driver to support this controller implementation. For those who do wish to substantially modify the existing Linux or RTOS USB driver(s), or create new drivers, contact TI for more information on how to obtain the third-party documentation under NDA.

The USB3SS subsystem contains the USB3.0 Dual Role Device (DRD) controller module and a USB2.0 PHY module. A wrapper module is controlling some top-level functions like Host and Device role switch and reset release.

The USB controller uses USB2PHY for USB2.0 operation and one of the device SERDESes for USB3.0 speeds.

12.2.4.4.1 USB Controller Reset

USB controller has three resets going in, called preset_n, pwrup_rst_n, and aresetn.

- preset_n comes from the mod_g_rst_n input coming from LPSC
- pwrup_rst_n is PWRUP_RST_N register bit in the USB wrapper module (USB3P0SS_W1). This reset has to be deasserted before accessing controller registers. The default value for pwrup_rst_n is 0 (reset asserted). This reset goes to the default asserted state when mod_g_rst_n reset is asserted.
- areset_n comes from PWRUP_RST_N register bit, but the deassertion is synchronized to ACLK.

12.2.4.4.2 Overcurrent Detection

The overcurrent detection circuit is external to the device. Software must specify an overcurrent condition to the controller whenever the overcurrent signal is received from the detection circuit. Software must set the OVERCURRENT_N bit to 0 in the USB3P0SS_W1 register when overcurrent was detected.

12.2.4.4.3 Top-Level Initialization Sequence

The following initialization sequence has to be followed before configuring the controller for USB operation:

1. Software must select and configure the SERDES for USB operation. Refer to *Serializer/Deserializer (SerDes)* for more details. USB2.0 PHY contains default configuration that normally does not need change
2. Software must configure the pseudo-static settings in USB3P0SS_W1 register
3. Software must set PWRUP_RST_N to 1 in order to deassert controller reset
4. Software must wait for controller to be ready in the respective mode selected by reading the respective status bits.

After the above sequence, software can access controller registers.

12.2.4.5 USB Registers

Note

Details on the USB controller registers are not provided in this TRM. The existing Linux or RTOS drivers should be used for proper USB operation. For those who do wish to substantially modify the existing Linux or RTOS USB driver(s), or create new drivers, contact TI for more information on how to obtain the third-party documentation under NDA.

12.3 Memory Interfaces

This section describes the memory interfaces in the device.

12.3.1 Flash Subsystem (FSS)

This section describes the Flash Subsystem (FSS) in the device.

12.3.1.1 FSS Overview

The Flash Subsystem (FSS) provides access to external Flash devices via Octal Serial Peripheral Interface (OSPI) .

The FSS includes one OSPI. For more information, see *Octal Serial Peripheral Interface (OSPI)*.

Table 12-223 shows FSS allocation across device domains.

Table 12-235. FSS Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
FSS0	-	✓

Figure 12-151 shows the FSS overview.

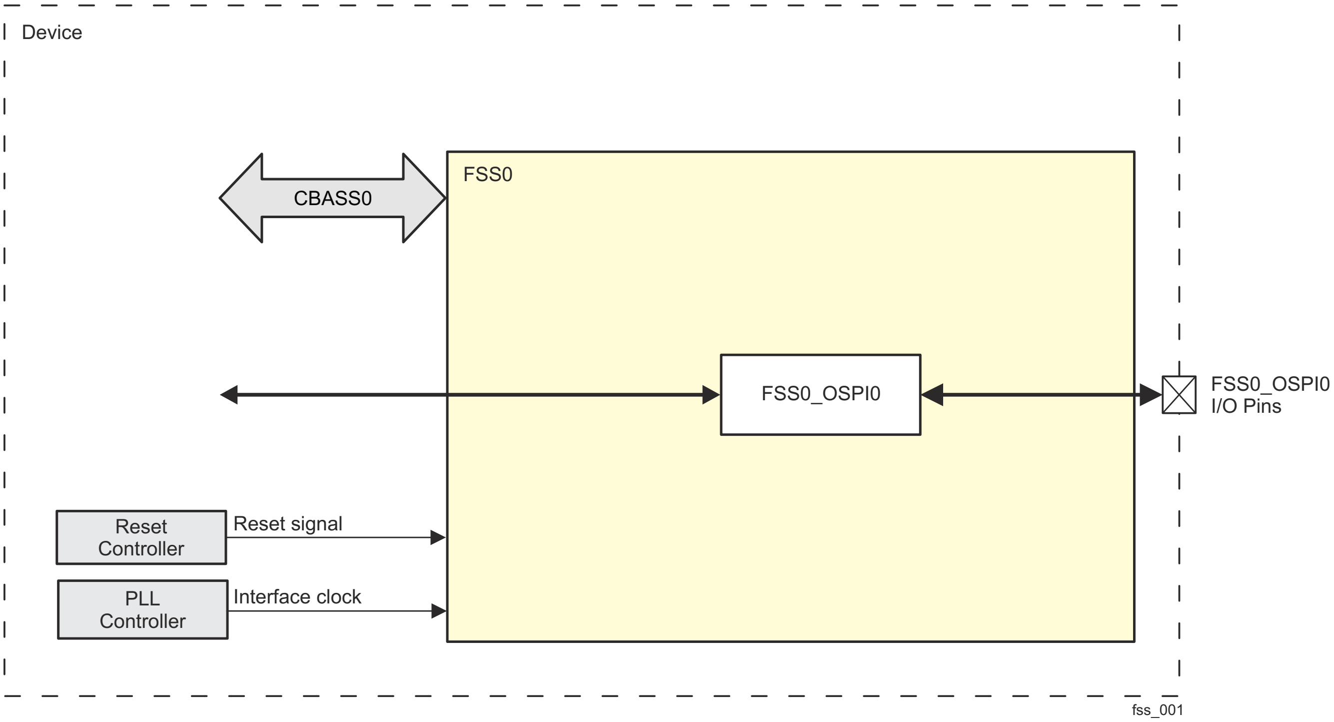

Figure 12-151. FSS Overview

12.3.1.1.1 FSS Features

12.3.1.1.2 FSS Not Supported Features

12.3.1.2 FSS Integration

This section describes the FSS integration in the device, including information about clocks, resets, and hardware requests.

12.3.1.2.1 FSS Integration

Figure 12-152 shows integration of FSS0.

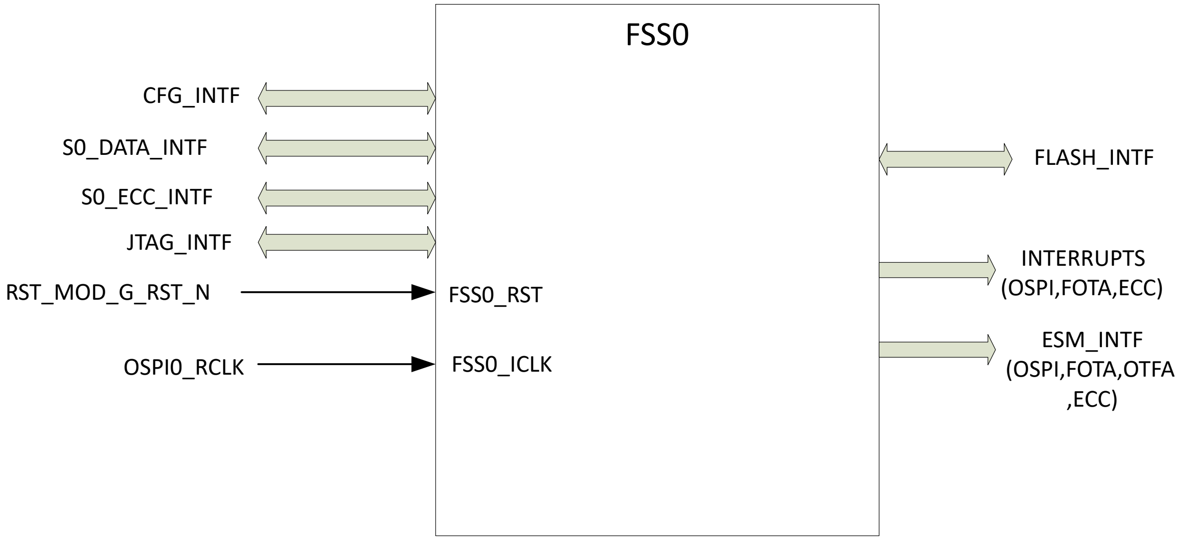

Figure 12-152. FSS0 Integration

Table 12-236. FSS0 Clocks

Module Instance	Module Clock Input	Source Clock Signal	Description
FSS0	FSS0_ICLK	OSPI0_RCLK_CLK	OSPI0 Clock
	FSS0_VBUS_CLK	VBUS_CLK	FSS CFG and DATA Clock

Table 12-237. FSS0 Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
FSS0	FSS0_RST	MOD_G_RST	SYS_RST	FSS0 system reset

FSS0 Hardware Requests

For more information, see

Note

For more information on the OSPI Integration, see .

Note

For more information on the interconnects, see the System Interconnect chapter.

For more information on power, reset, and clock management, see the corresponding sections within the Device Configuration chapter.

For more information on the device interrupt controllers, see the Interrupt Controllers chapter.

12.3.1.3 FSS Functional Description

12.3.1.3.1 FSS Detailed Block Diagram

12.3.1.3.2 FSS Block Diagram

12.3.1.3.3 FSS Regions

12.3.1.3.3.1 FSS Regions Boot Size Configuration

The boot size for FSS defaults to 64 MB but can be configured to be 128 MB. Selection of boot block which will be used is also configurable. For more information see CTRLMMR_FSS_CTRL register in *Control Module (CTRL_MMR*).

12.3.1.3.3.2 FSS Regions Boot Size Configuration

The boot size for FSS defaults to 64 MB but can be configured to be 128 MB. Selection of boot block which will be used is also configurable. For more information see CTRLMMR_FSS_CTRL register in *Control Module (CTRL_MMR*).

12.3.1.3.4 FSS Memory Regions

The FSS provides data transfer to OSPI through a single 64-bit S0 Data Interface, with data passing through ECCM/OTFA modules. The FSS memory space is divided into three distinct regions, each 128MB in size, for accessing flash memory. These regions are classified based on their functional features:

- Address translation support
- Boot capability
- On-the-fly Encryption and Authentication (OTFA)
- Error Correction Code (ECC) protection

Each region can be configured independently to enable or disable these features based on system requirements.

All these memory mapped regions map to the same physical location in the flash.

Table 12-238. FSS Memory Regions

FSS Regions	SoC Address Range	Size	Region Features	Description
Region 0	0x60000000 - 0x67FFFFFF	128 MB	Supports OTFA + ECC	External Memory Space
Region 1	0x80000000 - 0x87FFFFFF	128 MB	Supports OTFA + ECC	Boot Space
			Supports Address Remap-ability feature	
Region 3	0x88000000 - 0x8FFFFFFF	128 MB	NO OTFA + NO ECC	External Memory Space - Bypass Region

Note

There is no FSS Region 2.

1. **FSS Region 0 :** Region 0 supports the following operations:
   - Execute-In-Place (XIP)
   - DMA reads
   - DMA writes

   This region is designed to handle flash or RAM data that requires authentication and/or ECCM protection. It automatically performs address translation to accommodate the additional space needed for ECC and MAC data
2. **FSS Region 1 :** This region is similar to FSS Region 0, but can select 4KB to 128MB block, defined by the *_boot_segment_* and *_boot_mask_* registers. See section FSS Boot Region and Selection for details. Both FSS Region 0 and 1 have address translation to make room for the authentication and ECCM words. As mentioned above the main feature of FSS Region 1 that is not present in Region 0 and FSS Region 3 is Address Remapability using *_boot_segment_* and *_boot_mask_* registers.
3. **FSS Region 3 :**

Bypass Region Primary Functions:

a. Bypasses both ECC and OTFA processing
b. Enables direct flash programming with pre-authenticated and ECCM-protected data
c. Supports error correction (scrubbing) operations: Used to scrub ECCM errors in the event that the Flash takes a bit hit. That is to scrub a single bit error in flash, it may be necessary to re-write an entire block of flash. The FSS reports the untranslated block address; the system will translate the address based on MAC and ECCM modes to locate the real address in Flash or RAM for the scrubbing operation.

Additional Uses:

a. Used for validation of MAC and ECCM block programming
b. FOTA (Firmware Over The Air) operations: Used by FOTA HW ENGINE for flash writes in single interface RWW mode. It expects input data to be pre-encrypted and pre-authenticated with ECC and MAC.

Note

When using this region, data must be properly formatted with ECC and MAC before writing to flash.

It is important to note that FSS regions are logical partitions internal to the FSS module and are completely independent from the physical bank/region organization specified in the flash device data sheet. FSS regions just defines the dataflow path to/ from flash. All FSS Regions 0,1,3 map to the same physical location in the flash. The idea behind all 3 different FSS regions pointing to the same flash physical location is so that:

1. While writing to flash using Region 0 the data will go through the OTFA and ECC path and hence with be Encrypted and Authenticated (padded with MAC and ECC).
2. While writing to flash using Region 3 the data will go as it is without any Encryption / Authentication. (Bypasses OTFA and ECC)
3. FSS Region 1 is called boot space region as ROM uses FSS Region 1. If Address remap feature is enabled in MSS-CTRL and is R5F/any other controller throws access to that address range, then the access will be remapped to new location as explained in FSS Boot Region and Selection.

Note

128MBytes can be addressed using Address Bits[26:0] -> 27 Bits. Hence the upper 5 address Bits[31:27] are not relevant from perspective of flash/memory device.

12.3.1.3.4.1 FSS Boot Region and Selection

The boot placement in the flash is controlled by the below MMRs present in MSS_CTRL:

1. *MSS_OSPI_BOOT_CONFIG_SEG_BOOT_SEG[19:0]* - Interface S0 Boot segment selector
2. *MSS_OSPI_BOOT_CONFIG_MASK_BOOT_MASK[19:0]* - Interface S0 Boot mask

For documentation ease, the *MSS_OSPI_BOOT_CONFIG_SEG_BOOT_SEG[19:0]* will be referred to as *_boot_segment_.* and the *MSS_OSPI_BOOT_CONFIG_MASK_BOOT_SIZE [19:0]* will be referred to as *_boot_mask_.* The FSS boot region (Region 1) can be defined as a 4KB through 128MB block. Which 4KB through 128MB region of the 128M Byte is defined by the *_boot_segment_* register. These *_boot_segment_* bits replace the required number of bits of the 32-bit internal address based on segment size (determined by *_boot_mask)* when reading or writing region 1. The *_boot_mask_* determines which bits are replaced. Since minimum boot region granularity is 4KB, the FSS boot region 1 only specifies 20 bits of address, the upper 20 bits of a 32-bit internal address will be derived from the *_boot_segment_* and *_boot_mask_* registers. The *_boot_segment_* will replace the upper 20 bits of the internal address based on segment size derived from *_boot_mask_* which will determine the bits to be replaced.

This allows the boot sector to be placed anywhere within the translated flash space. In addition, this can be used to implement FOTA swap feature which requires CPU address map to remain the same while the firmware in flash is swapped to a different copy. Figure FSS Region 1 Remapping explains this concept in more detail. Typically, when the image binary is created, it is usually linked to load and run from a fixed address. For example, CPU could be executing from firmware A in flash while firmware B is being written (FOTA update). When swap to firmware B is required, SOC can reconfigure *_boot_segment_* and *_boot_mask_* to point to firmware B in flash while CPU still uses same address map as firmware A. This allows CPU address map to remain the same as previous firmware.

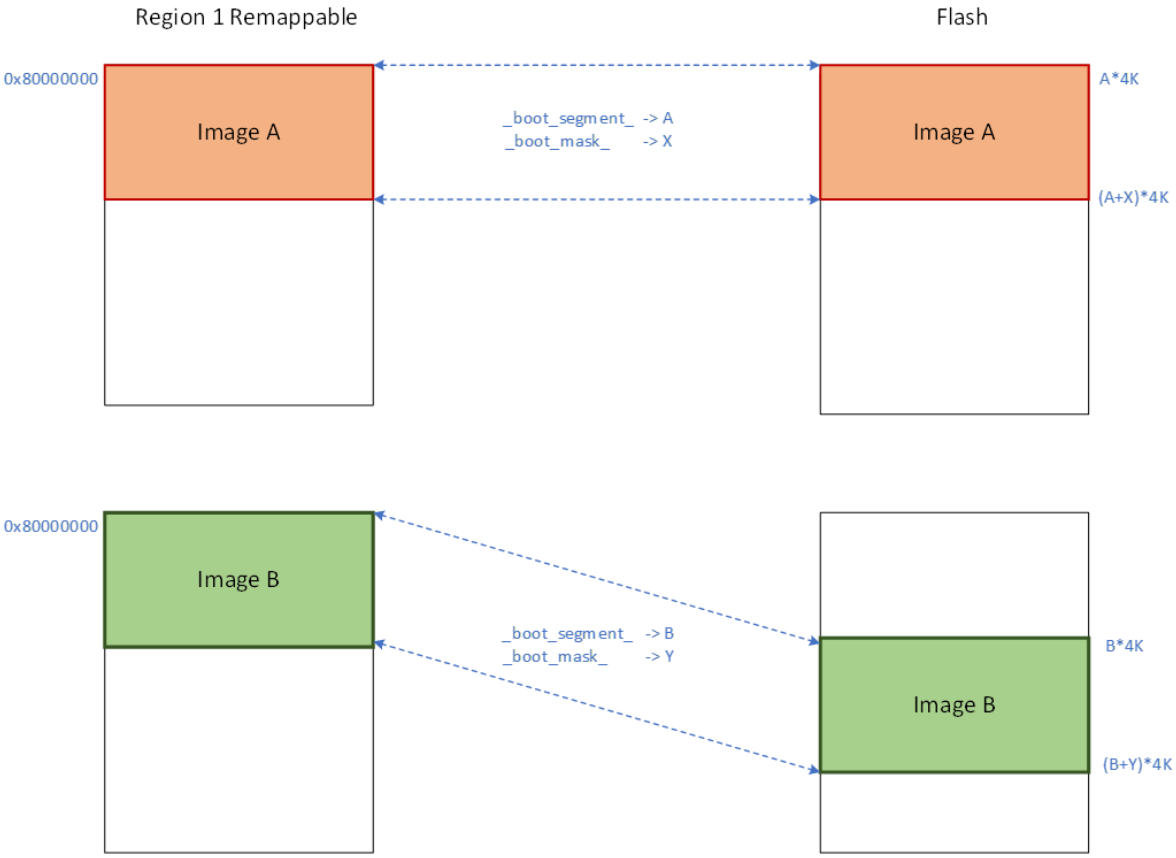

Figure 12-153. FSS Region 1 Remapping

The maximum memory region allocated for External memory Region in SoC is 128 MBytes. This 128 MBytes is addressable with lower 27 bits [26:0]. Hence the five upper address bits[31:27] are used by SoC to identify that it is FSS Data Region 1. Since the minimum granularity is 4KB the lower 12 address bits is taken as it is and not address translated. The Upper [31:12] address bits aligns to *_boot_segment_* and *_boot_mask_* bits [19:0].

Pseudo Code for address remapping

- if (boot_mask bit[i] ==1) : Then that address bit is replaced with the corresponding bit in*_boot_segment_*
- if (boot_mask bit[i] == 0) : Then the corresponding address bits are taken as it is (and not taken from *_boot_segment_* bits)

Example 1: Assume Image A is Primary Boot Image of size (<=16MB) located at 0x8000_0000 and Image B is located at offset of 16MB of flash (0x8100_0000). So in this case any access to 0x8**0**00_0000 should be mapped to 0x8**1**00_0000

Hence *_boot_segment_* value should be = 0x1000 and *_boot_mask_* = 0xFF000 as seen in Figure 12-154

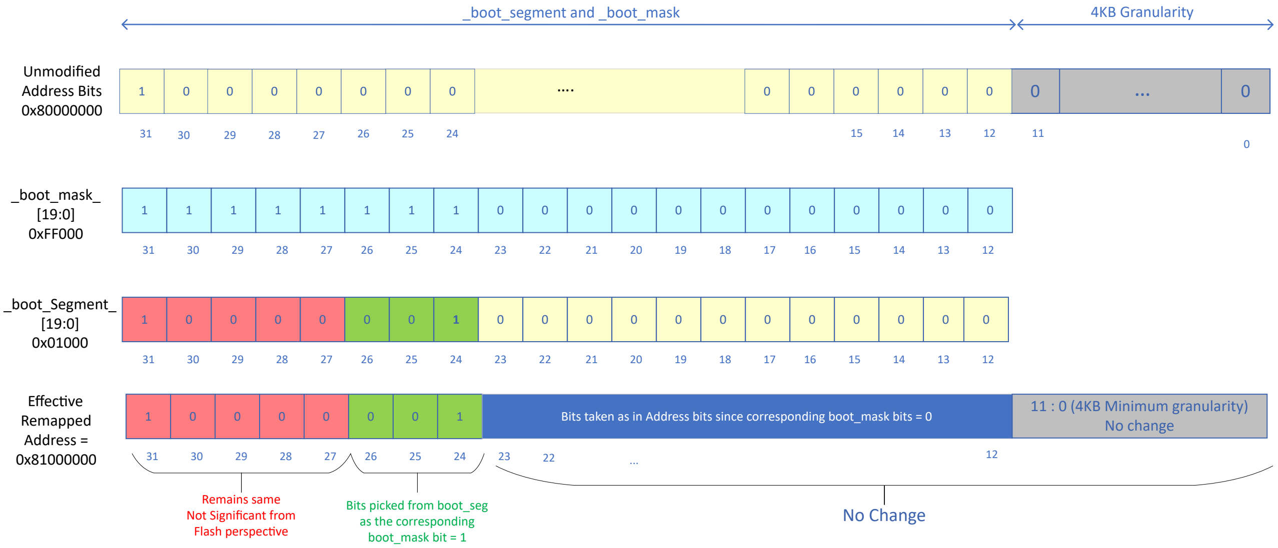

Figure 12-154. Boot_Segment and Boot_Mask Example Configuration

Hence any access to address 0x8000_0000 will be remapped to address 0x8100_0000. In other words the image at location 0x8100_0000 ' *before boot_segment & boot_mask configuration*' as seen in memory browser will be seen at location 0x8000_0000 (by ROM / memory browser) '*after boot_segment & boot_mask configuration*' .

Required offset in flash(before ECCMaddress translation	_boot_mask	_boot_segment	Effective offset(before ECCM address Translation)
4KB (minimum granularity)	0xFFFFF	0x00001	0x0000_1000
8KB	0xFFFFF	0x00002	0x0000_2000
128KB	0xFFFE0	0x00020	0x0002_0000
64MB	0xFC000	0x04000	0x0400_0000

Example 2: Consider the scenario where flash total size is 128KB, ECCM is enabled, 16-byte MAC is enabled, and boot segment size (determined by *_boot_segment_)* is 16KB. For this scenario, the highest address the *_boot_segment_* can be placed is address 0xFB12. Most time the boot sector will be set to zero, but this is not required.

Note

Care must be taken to account for the address translation as to not fall off or wrap the address of the flash

12.3.1.3.4.2 FSS Safety and Security

The FSS has Safety and Security which can be configured for Safety and/or Security enabled or disabled. These Safety and Security features manage additional in-band data (ECCM syndromes and MAC) that is added to the user data in the Flash device memory. For each 32 bytes of user data, Safety adds 4 bytes of ECCM and Security adds 4,8,12 or 16 bytes of MAC. If both Safety and Security are enabled, up to 20 bytes of overhead is going to be added to every 32 bytes of user data.

The FSS manages flash memory access in blocks, with block sizes varying based on enabled features:

Base Block Size: 32 bytes

Additional Overhead Requirements:

1. Safety (ECC) enabled: Adds 4 bytes per 32-byte block for ECCM syndrome data
2. Security (MAC) enabled: Adds 4, 8, 12, or 16 bytes per 32-byte block (based on programmed MAC size)
3. Both Safety and Security enabled: Total overhead is 8, 12, 16, or 20 bytes per 32-byte block. Combines ECCM syndrome (4 bytes) and MAC data (4-16 bytes)

Important Note: Once Safety or Security features are enabled, the corresponding space is reserved across all memory regions, regardless of whether individual regions are configured to use these features. The block size returns to 32 bytes only when both Safety and Security features are disabled.

The FSS HW is responsible for hiding this extra data from SOC. The FSS HW translates the accessed address, strips (on read) or adds (on writes) the necessary extra data

12.3.1.3.4.3 Read Optimizations

To distinguish between similar read optimization features implemented across different FSS modules, the following definitions are used:

1. **OSPI DAC Predicted Read feature :** This optimizes read performance by issuing a predicted read if the current reads are complete. Please refer to OSPI Controller section for more information.
2. **OSPI DAC Read PHY pipeline mode :** This feature is implemented by OSPI Controller to read extra bytes based on Controller configuration at the end of a read from flash. This ensures that chip select is not de-asserted during flash round-trip delay and sample delay associated with PHY DLL. Please refer to section Section 12.3.2.4.16.1 for more information.
3. **FSS XIP Prefetcher :**

   The prefetcher automatically loads the next 32-byte block from flash when specific conditions are met. This feature optimizes XIP performance in two ways:

   a. Addresses CPU request patterns: CPU XIP requests typically occur at random intervals. Requests are often non-consecutive
   b. Reduces latency: Proactively fetches the next cache line. Eliminates waiting time for CPU requests. Particularly effective for linear code execution

   For detailed implementation and conditions, refer to the FSS XIP Prefetcher
4. **ECCM Read Pipeline Mode :** This feature assists in maintaining address continuity to flash by reading MAC and ECCM words even if the request address is not in MAC or ECCM region. In this case, the unused MAC or ECCM words are discarded. This is implemented by the ECCM module since it is responsible for address translation and reserving space in flash for ECCM and MAC. The purpose for this is to ensure OSPI can receive continuous addresses such that it can skip sending command bytes to flash. This feature does not need continuous requests. It will predict that the next consecutive address will be requested and hence is optimizing the current request to maintain address continuity. Please refer to section *ECCM Read Pipelined mode* for more information.

12.3.1.3.4.4 FSS XIP Prefetcher

The FSS includes a prefetcher module optimized for XIP (Execute-In-Place) operations. When no pending requests exist, this module automatically fetches the next sequential block of data. This prefetching mechanism significantly improves performance during linear code execution

By default, the prefetcher block is enabled, and setting the *disxip* bit in the SYSCONFIG will disable this feature and any prefetched data will be discarded. Once the pre-fetch starts, it will continue as long as the following request occurs during the pre-fetch burst and the requested address is the same address as the pre-fetched burst address. If the read to the pre-fetch burst occurs after the bus has gone idle, the next burst will not be read. If a different block is read, then pre-fetching stops after current pre-fetch completes and the pre-fetch data is saved into a stack allowing up to 1 burst to be remembered. Any write to a pre-fetched burst address will cause that pre-fetched burst to be purged. If the *disxip* config bit is set pre-fetching is disabled and any prefetched data is discarded.

It is recommended to use *disxip* as a static configuration bit that is selected based on desired mode of operation and not toggled dynamically while reads are active. For example, pulsing *disxip* high by writing 1 and 0 in quick succession will not guarantee that prefetch buffer is purged. This is because this pulsing can occur while a prefetch read is in progress and *disxip* may end up being 0 while prefetch buffer is written. This race condition between software *disxip* pulsing and hardware prefetch buffer write can be avoided by ensuring that *disxip* is selected for next read phase based on whether prefetching is required for this phase.

Please note that this is referring to prefetching feature that is useful for linear accesses associated with XIP. This is NOT referring to XIP features implemented in flash Controller or memory device.

Although this feature has reference to XIP, it is not limited to XIP and is applicable to any reads from flash. However, XIP is used in the name since it is most likely to be used for XIP. Block copy requests are generally provided back-to-back and hence XIP prefetcher logic may not even be activated.

The prefetcher module also has the ability to turn all read request into 2-bytes aligned (even length) request due to OSPI limitation on DDR mode. In other words, the logic makes the OSPI address and length even and inclusive of the requested bytes. Setting the *ospi_ddr_disable_mode* bit will disable this feature and pass all read requests unchanged. To use this feature, the *ospi_32b_disable_mode* bit must be set.

This module also can take any read and make it a 32-bit read aligned to a 32-bit aligned address for OSPI pipeline modes. Setting the *ospi_32b_disable_mode* bit will disable this feature and pass all read requests unchanged. This feature has priority over the DDR feature so if both control bits are clear this feature is in operation.

12.3.1.3.4.5 Considerations for OSPI INDAC Read Mode with Address Translation

The OSPI Controller has an INDAC mode that involves configuration of start address and size for indirect operation. The FSS modules upstream of OSPI perform address translation in certain circumstances. It is important to understand the impact of this address translation on INDAC mode. Please refer section *Memory address translation for memory map calculation*. Also, please refer *Indirect Read Transfer Number Bytes Register* in OSPI Controller specification for more information on INDAC configuration.

12.3.1.4 FSS Programming Guide

12.3.1.4.1 FSS Initialization Sequence

12.3.1.4.2 Real-time operating requirements

The CPU or DMA can read any location in the memory map and ECCM, authentication or decryption will occur based on the region selection and size configuration.

In the event of an ECCM Single Error Detect error, the 32-byte block address and associated error bits are stored and an interrupt is generated if enabled.

The CPU can then service the interrupt and determine the error type. If a single error occurs, the CPU can scrub the flash block to determine if the error is permanent and requires reprogramming.

In the event of an ECCM Double Error Detect error, the 32-byte block address and associated error bits are stored and an interrupt is generated if enabled.

The CPU can then service the interrupt and determine the error type. If the Double error detect is within the flash, the region is corrupt and should not be used.

For both ECCM Double Error Detect and authentication error, the bus status will also be set. This prevents the CPU from executing the errant data.

12.3.1.4.3 FSS Power Up/Down Sequence

There are two PSC controls for the FSS: for FSS0 itself and for FSS0_OSPI0. The CPU enables the FSS0_OSPI0 before using the FSS. Software should ensure the FSS0_OSPI0 is enabled prior to FSS transactions.

Normal Power Down Sequence:

- Block any new transaction.
- Power down the FSS0_OSPI0.
- In the event when the FSS0_OSPI0 is powered down, the FSS can then be powered down.

12.3.2 Octal Serial Peripheral Interface (OSPI)

This section describes the Octal Serial Peripheral Interface (OSPI) module for the device.

Under-construction Notice

Note

This content is currently **under-construction** and subject to change prior to official device release.

12.3.2.1 OSPI Overview

The Octal Serial Peripheral Interface (OSPI) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad, or octal read and write access to external flash devices.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device controller at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM is accessed using user programmable configuration registers.

Table 12-227 shows the OSPI allocation across device domains.

Table 12-239. OSPI Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
FSS0_OSPI0	-	✓

Figure 12-155 shows the OSPI module overview.

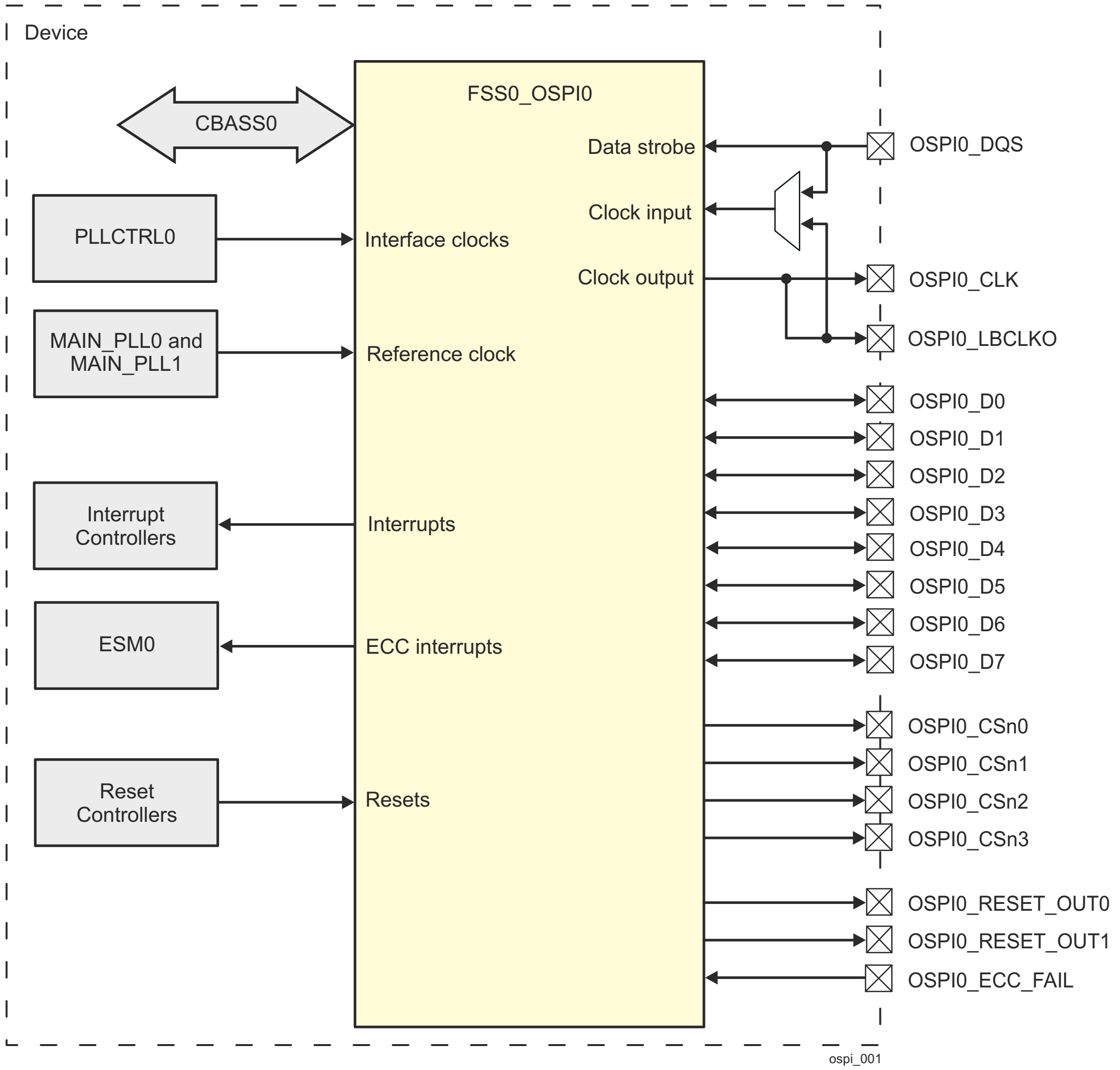

Figure 12-155. OSPI Overview

12.3.2.1.1 OSPI Features

The OSPI module has the following features:

- Support for single, dual, quad (QSPI mode) or octal I/O bus widths.
- Memory mapped ‘direct’ mode of operation for performing flash data transfers and executing code from flash memory.
- Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers.
- Local SRAM of configurable size to reduce advanced high-performance bus overhead and buffer flash data during indirect transfers.
- Set of software advanced peripheral bus accessible flash control registers to perform any flash command, including data transfers up to 8-bytes at a time.
- Additional addressable memory bank to accommodate more than 8-bytes at a time.
- Support for XIP, sometimes referred to as continuous mode.
- Support for DDR Mode and DTR protocol (including Octal DDR protocol with DQS for Octal-SPI devices)
- Programmable device sizes.
- Programmable write protected regions to block system writes from taking effect.

- Programmable delays between transactions.
- Legacy mode allowing software direct access to low level transmit and receive FIFOs, bypassing the higher layer processes.
- An independent reference clock to decouple bus clock from SPI clock – allows slow system clocks.
- Programmable baud rate generator to generate OSPI clocks.
- Features included to improve high speed read data capture mechanism.
- Option to use adapted clocks or DQS to further improve read data capturing.
- Programmable interrupt generation.
- Up to four external device selects - OSPI and QSPI devices can be mixed
- Programmable data decoder, enables continuous addressing mode for each of the connected devices and auto-detection of boundaries between devices.
- Supports BOOT mode.
- Bidirectional CRC on Multiple-SPI interface.
- Handling ECC errors for flash devices with embedded correction engine.
- Full integration with PHY module dedicated to more flexible and power efficient transfers.
- Supports RESET_OUT[1-0] and ECC_FAIL pins for external flash devices where ECC is checked on the flash.
- Automatic Flash device status polling for programming operation (Auto HW Polling)

12.3.2.1.2 OSPI Not Supported Features

The following features are not supported on this family of devices:

- DMA not supported.
- Pulse events not used.
- In Octal-SPI and Quad-SPI mode, Mode 1, 2, and 3 are not supported.

12.3.2.2 OSPI Environment

The FSS0_OSPI0 module is hereinafter referred to as OSPI module.

This section describes the OSPI external connections (environment).

The OSPI module is primarily intended for fast booting from Octal- and Quad-SPI flash memories. Figure 12-156 shows a typical connection of the OSPI module to an external Octal-SPI flash memory.

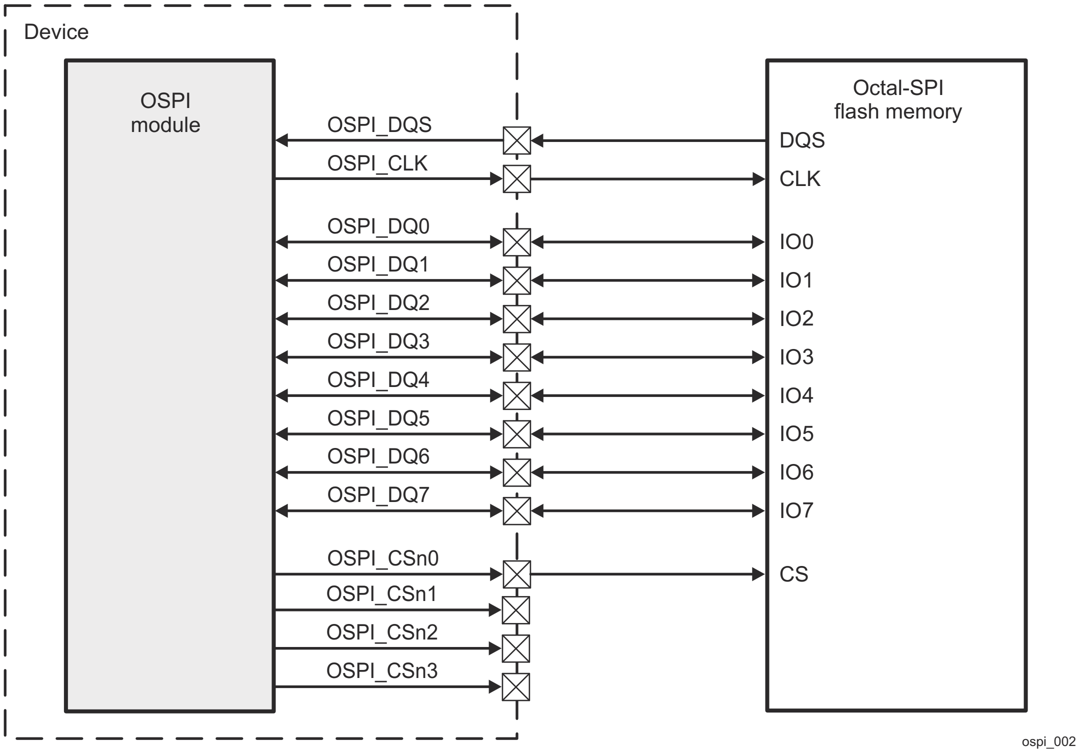

Figure 12-156. OSPI Connected to an External Octal-SPI Flash Memory

Table 12-228 lists and describes the FSS0_OSPI I/O signals.

Table 12-240. OSPI I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
			FSS0_OSPI0	
DQ0	OSPI0_D0	IO	FSS0_OSPI0 data input/output 0	HiZ
DQ1	OSPI0_D1	IO	FSS0_OSPI0 data input/output 1	HiZ
DQ2	OSPI0_D2	IO	FSS0_OSPI0 data input/output 2	HiZ
DQ3	OSPI0_D3	IO	FSS0_OSPI0 data input/output 3	HiZ
DQ4	OSPI0_D4	IO	FSS0_OSPI0 data input/output 4	HiZ
DQ5	OSPI0_D5	IO	FSS0_OSPI0 data input/output 5	HiZ
DQ6	OSPI0_D6	IO	FSS0_OSPI0 data input/output 6	HiZ
DQ7	OSPI0_D7	IO	FSS0_OSPI0 data input/output 7	HiZ
N_SS_OUT0	OSPI0_CSn0	O	FSS0_OSPI0 external flash device chip select 0	0x1
N_SS_OUT1	OSPI0_CSn1	O	FSS0_OSPI0 external flash device chip select 1	0x1
N_SS_OUT2	OSPI0_CSn2	O	FSS0_OSPI0 external flash device chip select 2	0x1
N_SS_OUT3	OSPI0_CSn3	O	FSS0_OSPI0 external flash device chip select 3	0x1
OCLK	OSPI0_CLK	O	FSS0_OSPI0 clock output for the external flash device	0x0
	OSPI0_LBCLKO	O	FSS0_OSPI0 external loopback output	0x0

Table 12-240. OSPI I/O Signals (continued)

Module Pin	Device Level Signal	I/O[(1)]	Description	Module Pin Reset Value[(2)]
DQS	OSPI0_DQS	I[(3)]	FSS0_OSPI0 data strobe / external loopback input	Don't care
RESET_OUT0	OSPI0_RESET_OUT0	O[(4)]	FSS0_OSPI0 reset output 0 for the external flash device. Pin is active low.	0x1
RESET_OUT1	OSPI0_RESET_OUT1	O[(4)]	FSS0_OSPI0 reset output 1 for the external flash device. Pin is active low.	0x1
ECC_FAIL	OSPI0_ECC_FAIL	I	FSS0_OSPI0 ECC status from the external flash device	0x1

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) When used as an external loopback input, the DQS signal can alternatively be referred to as LBCLKI. The LBCLKI clock input signal is a looped back version of the LBCLKO clock output signal and facilitates easier timing closure at higher speeds. The loopback has to be at board level in order to support higher OSPI speeds. The source of the loopback clock is defined by CTRLMMR_OSPI0_CLKSEL[4] LOOPCLK_SEL bit in *Control Module (CTRL_MMR)*.

(4) When OSPI flash memory is not used for Boot, the RESET_OUT[1:0] signals can be used to reset the OSPI flash. If OSPI flash is used for Boot, the flash needs to be reset in tandem with SoC PORz, thus the OSPI0_RESET_OUT[0:1] signal should not be used.

Table 12-229 describes the OSPI I/O connectivity to external SPI devices.

Table 12-241. OSPI I/O Connectivity to External SPI Devices

Module Pin	I/O[(1)]	Description			
		4-pin[(1)] SPI - Single Read/Write (SIO) (DATA_XFER_TYPE_EXT_MODE_FLD=0x0)	**4-pin[(1)] SPI - Dual Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x1)**	**6-pin[(1)] SPI - Quad Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x2)**	**11-pin[(1)] SPI - Octal Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x3)**
DQ0	IO	Used as SPI data output	Used as SPI data input 0 Used as SPI data output 0	Used as SPI data input 0 Used as SPI data output 0	Used as SPI data input 0 Used as SPI data output 0
DQ1	IO	Used as SPI data input	Used as SPI data input 1 Used as SPI data output 1	Used as SPI data input 1 Used as SPI data output 1	Used as SPI data input 1 Used as SPI data output 1
DQ2	IO	Not used	Not used	Used as SPI data input 2 Used as SPI data output 2	Used as SPI data input 2 Used as SPI data output 2
DQ3	IO	Not used	Not used	Used as SPI data input 3 Used as SPI data output 3	Used as SPI data input 3 Used as SPI data output 3
DQ4	IO	Not used	Not used	Not used	Used as SPI data input 4 Used as SPI data output 4
DQ5	IO	Not used	Not used	Not used	Used as SPI data input 5 Used as SPI data output 5
DQ6	IO	Not used	Not used	Not used	Used as SPI data input 6 Used as SPI data output 6
DQ7	IO	Not used	Not used	Not used	Used as SPI data input 7 Used as SPI data output 7
DQS	I[(2)]	Not used	Not used	Not used	Data strobe or loopback clock input
OCLK	O	Output clock or loopback clock output. For more information, see Table 12-228.			
N_SS_OUT0	O	External SPI device chip-select 0			
N_SS_OUT1	O	External SPI device chip-select 1			
N_SS_OUT2	O	External SPI device chip-select 2			
N_SS_OUT3	O	External SPI device chip-select 3			
RESET_OUT0	O	External SPI device reset 0. Pin is active low.			
RESET_OUT1	O	External SPI device reset 1. Pin is active low.			

Table 12-241. OSPI I/O Connectivity to External SPI Devices (continued)

Module Pin	I/O(1)	Description			
		4-pin(1) SPI - Single Read/Write (SIO) (DATA_XFER_TYPE_EXT_MODE_FLD=0x0)	4-pin(1) SPI - Dual Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x1)	6-pin(1) SPI - Quad Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x2)	11-pin(1) SPI - Octal Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x3)
ECC_FAIL	I	External SPI device ECC failure indication			

(1) This is the pin count at the external SPI flash memory side.

(2) When used as an external loopback input, the DQS signal can alternatively be referred to as LBCLKI. The LBCLKI clock input signal is a looped back version of the LBCLKO clock output signal and facilitates easier timing closure at higher speeds. The loopback has to be at board level in order to support higher OSPI speeds. The source of the oopback clock is defined by CTRLMMR_OSPI0_CLKSEL[4] LOOPCLK_SEL bit in *Control Module (CTRL_MMR)*.

Note

For OSPI0_CLK, OSPI0_LBCLKO, and OSPI0_DQS signals to work properly, the RXACTIVE bit of the appropriate CTRLMMR_PADCONFIGx registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.3.2.3 OSPI Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

12.3.2.3.1 OSPI Integration in MAIN Domain

There is one OSPI module integrated in the device MAIN domain - FSS0_OSPI0. Figure 12-157 shows its integration in the device.

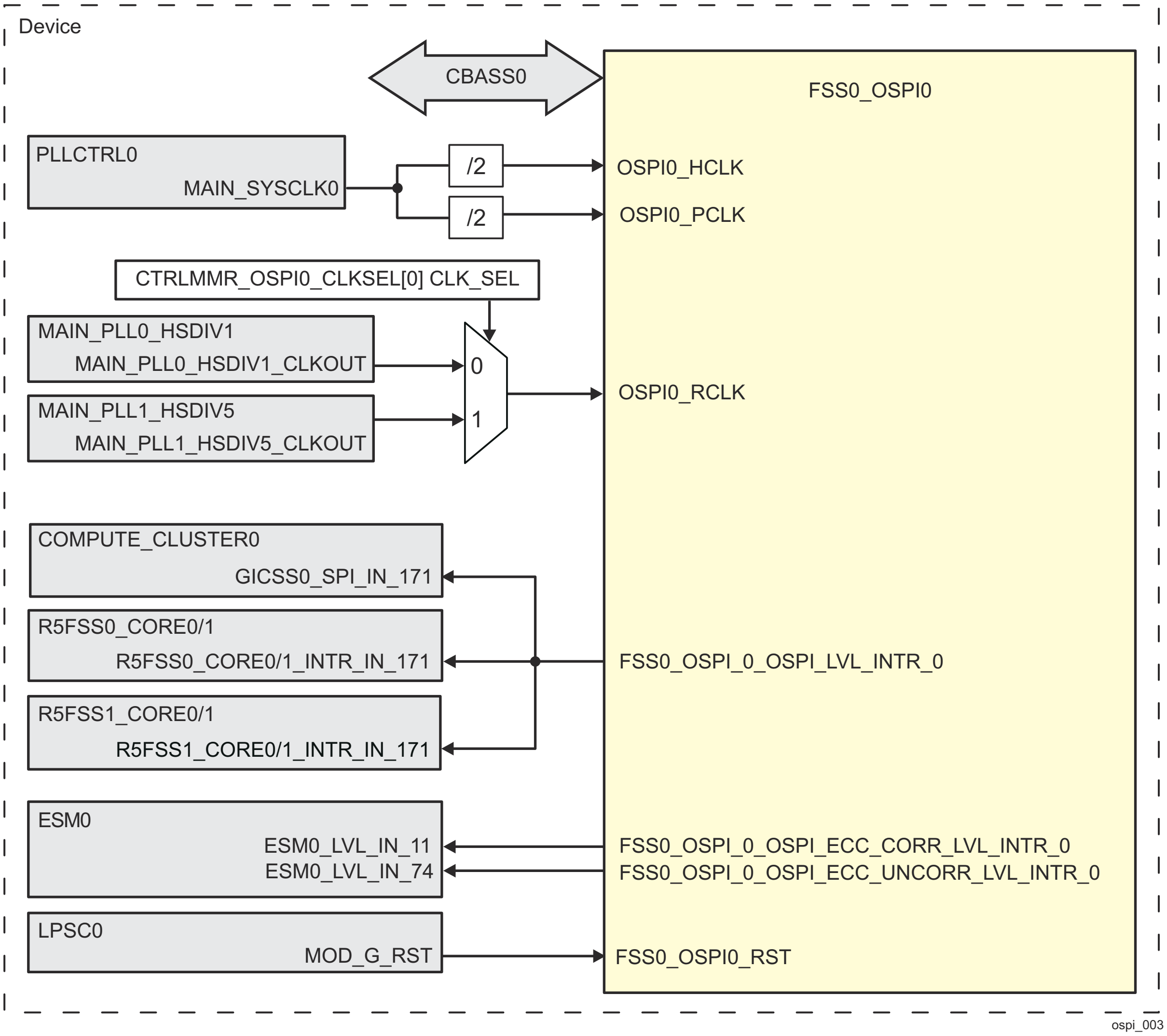

Figure 12-157. FSS0_OSPI Integration

Table 12-230 through Table 12-233 summarize the integration of FSS0_OSPI0 in device MAIN domain.

Table 12-242. FSS0_OSPI Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
FSS0_OSPI0	PSC0	PD0	LPSC0	CBASS0

Table 12-243. FSS0_OSPI Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
FSS0_OSPI0	OSPI0_HCLK	MAIN_SYSCLK0/2	PLLCTRL0	FSS0_OSPI0 data transfer clock
	OSPI0_PCLK	MAIN_SYSCLK0/2	PLLCTRL0	FSS0_OSPI0 configuration clock
	OSPI0_RCLK	MAIN_PLL0_HSDIV1_CLKOUT	MAIN_PLL0_HSDIV1	FSS0_OSPI0 Reference clock. Mux controlled by MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL

Table 12-243. FSS0_OSPI Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
		MAIN_PLL1_HSDIV5_CLKOUT	MAIN_PLL1_HSDIV5	[0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*

Table 12-244. FSS0_OSPI Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
FSS0_OSPI0	FSS0_OSPI0_RST	MOD_G_RST	LPSC0	FSS0_OSPI0 reset

Table 12-245. FSS0_OSPI Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
FSS0_OSPI0	FSS0_OSPI_0_OSPI_LVL_INTR_0	GICSS0_SPI_IN_171	COMPUTE_CLUSTER0	FSS0_OSPI0 interrupt	Level
		R5FSS0_CORE0_INTR_IN_171	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_171	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_171	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_171	R5FSS1_CORE1		
	FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_0	ESM0_LVL_IN_11	ESM0	FSS0_OSPI0 ECC Aggregator correctable error interrupt	Level
	FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_0	ESM0_LVL_IN_74	ESM0	FSS0_OSPI0 ECC Aggregator uncorrectable error interrupt	Level

Note

OSPI interrupts are further described in Section 12.3.2.4.7 , *OSPI Interrupt Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.3.2.4 OSPI Functional Description

12.3.2.4.1 OSPI Block Diagram

Figure 12-158 shows the OSPI module block diagram.

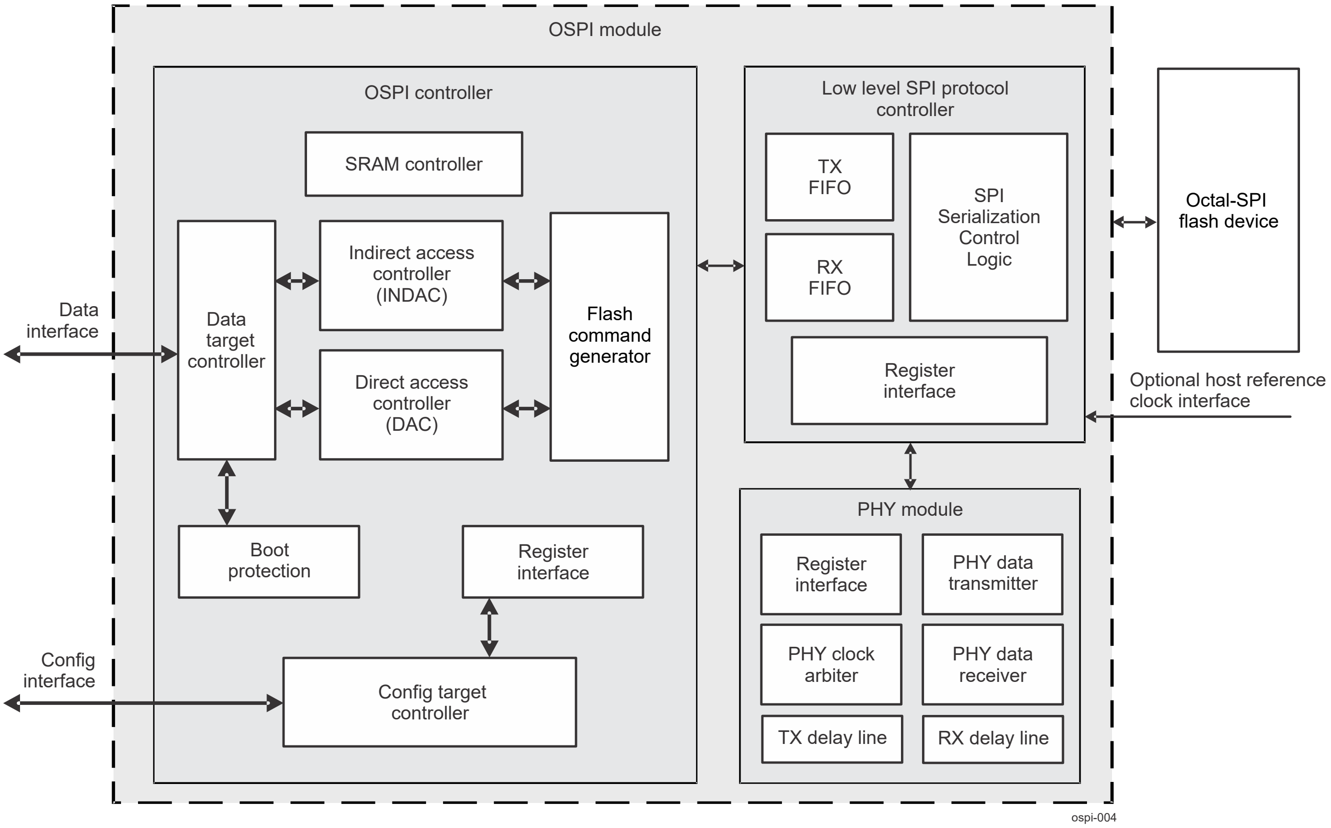

Figure 12-158. OSPI Block Diagram

The OSPI module is composed of three main blocks. The first one is the OSPI controller, the second one is the low level SPI protocol controller, and the third one is the integrated PHY.

The OSPI module has the following two target interfaces:

- Data target interface intended for data transfer.
- Configuration target interface intended for accessing the programmable set of registers.

12.3.2.4.1.1 Data Target Interface

The data interface is used for data transfer to external flash devices in direct and indirect mode of operation. The data target controller validates incoming data accesses, responds to invalid requests, performs any required byte and halfword reordering, blocks writes that violate the programmed write protection rules (only for direct access) and forwards the transfer request to either the direct access controller (DAC) or the indirect access controller (INDAC).

The data interface bus is 32-bits wide. Therefore only byte, halfword and word accesses are permitted. When the controller is configured to work in SPI Octal DDR Mode or Octal DDR Protocol (where 2 bytes are collected within single SPI clock cycle what exceeds the size of 1 byte transfer request), 8 bit transfer size is not allowed.

Note

Cache line wrap accesses over the data target port should be word aligned.

Data target port doesn't support cache line wrap bursts of 128 bytes.

12.3.2.4.1.2 Configuration Target Interface

The configuration interface is used to configure the OSPI module and perform software controlled flash accesses using the OSPI_FLASH_CMD_CTRL_REG register (for more information refer to Section 12.3.2.4.11 , *Software Triggered Instruction Generator (STIG)*). Depending on the address it routes the incoming interconnect transfer to the Low level SPI protocol controller or to the ECC aggregator. The configuration port is also used to interact with the OSPI configuration and SRAM ECC registers.

Note

The configuration interface supports only 32-bit accesses. For single byte or halfword manipulations software should perform read-modify-write operations.

12.3.2.4.1.3 OSPI Clock Domains

The OSPI module has two main clock sources for the Octal-SPI controller.

- For interface clocks
- For reference clock

The source for the interface clocks corresponds to the configuration and data buses. The data bus clock (OSPI_HCLK) is the main system clock used to transfer data over the data bus between a controller on the system interconnect and the OSPI module. The data bus clock also drives the internal OSPI SRAM. The configuration bus clock (OSPI_PCLK) is used to access the OSPI configuration register and perform basic configuration and for interrupt handling. The OSPI reference clock (OSPI_RCLK) drives the SPI transmit and receive logic in the OSPI module. It is also used to generate the output SPI protocol clock (OSPI_OCLK) and for oversampling of the input data. Using the reference clock (OSPI_RCLK) allows the OSPI module to decouple the frequency of the SPI flash device from the device system clocks, thereby providing more flexible clocking solution.

Note

There is no particular clock ratio requirement between configuration (OSPI_PCLK) and data bus (OSPI_HCLK) clocks.

12.3.2.4.2 OSPI Modes

Note

Some of the OSPI features described in this section may not be supported on this family of devices. For more information, see *OSPI Not Supported Features*.

The OSPI module supports four SPI modes. These modes are defined through the OSPI_CONFIG_REG[1] SEL_CLK_POL_FLD and OSPI_CONFIG_REG[2] SEL_CLK_PHASE_FLD bits. The SEL_CLK_POL_FLD bit defines the clock polarity and the SEL_CLK_PHASE_FLD bit defines the data launch and data capture relation to the OSPI clock edges. Table 12-234 gives a brief description of these modes.

Table 12-246. OSPI Modes

SPI Mode	SEL_CLK_POL_FLD	SEL_CLK_PHASE_FLD	Description
0	0	0	Clock inactive state: low
			Data launch edge: clock falling edge

Table 12-246. OSPI Modes (continued)

SPI Mode	SEL_CLK_POL_FLD	SEL_CLK_PHASE_FLD	Description
			Data capture edge: clock rising edge
1	0	1	Clock inactive state: low Data launch edge: clock rising edge Data capture edge: clock falling edge
2	1	0	Clock inactive state: high Data launch edge: clock rising edge Data capture edge: clock falling edge
3	1	1	Clock inactive state: high Data launch edge: clock falling edge Data capture edge: clock rising edge

Octal flash devices provide DQS signal which allows source synchronous capture, but for Quad flash devices the OSPI module has a loopback mode. In this loopback mode the clock, looped back at board level, is used for registering the input data, and the edge used is same as the launch edge, thus giving a full cycle path (for more information, see Section 12.3.2.4.2.1 , *Read Data Capture*).

12.3.2.4.2.1 Read Data Capture

Figure 12-159 shows the Read Data Capture Logic in the OSPI module.

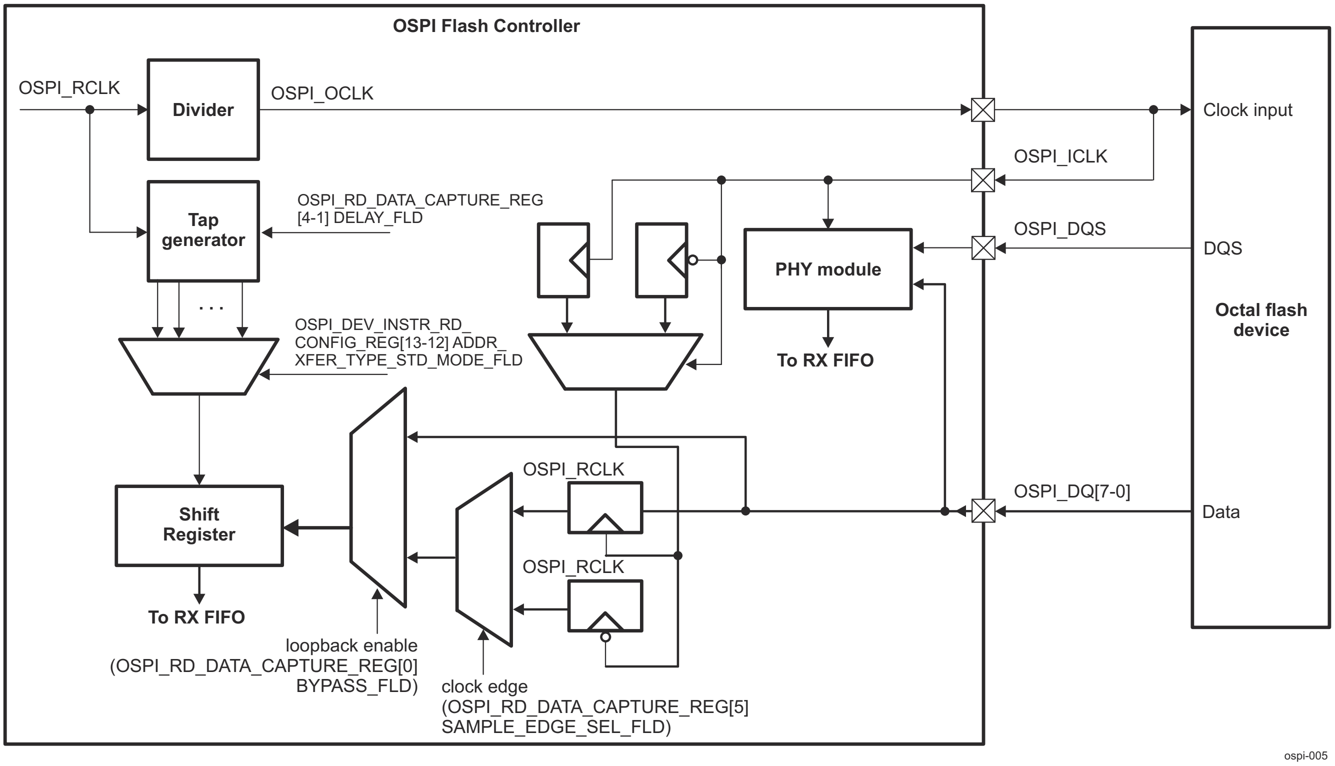

Figure 12-159. Read Data Capture Logic

The PHY module includes a DLL which allows adjustment of the sampling edge with respect to the incoming data to achieve maximum frequency. There are three sources for the sampling signal:

- The reference clock
- Output SPI clock external loopback
- The DQS (only available in Octal Flash devices)

The loopback mode (only for Quad flash devices) can work in two cases. The first one is when OSPI_CONFIG_REG[2] SEL_CLK_PHASE_FLD=0. When SEL_CLK_PHASE_FLD=1 there aren't enough clock falling edges for the register pipeline to catch the last data driven, thus causing a functional failure. Additionally, since the capture edge is falling edge, it gives a full cycle input path only in SPI mode 0, that is when SEL_CLK_POL_FLD=0 and SEL_CLK_PHASE_FLD=0. Thus SPI mode 0 is the first of two modes that support high MHz operation (greater than 50 MHz). The second mode is when SEL_CLK_PHASE_FLD=1 and SEL_CLK_PHASE_FLD=1 (SPI mode 3). In this case the missing clock falling edge is compensated inside the OSPI controller when using the incorporated PHY module by inverting the loopback clock.

The loopback mode is enabled by writing 0x0 to OSPI_RD_DATA_CAPTURE_REG[0] BYPASS_FLD. The taps are selected by programming OSPI_RD_DATA_CAPTURE_REG[4-1] DELAY_FLD field. The taps delay the read data capturing logic by the programmed number of OSPI_RCLK cycles.

12.3.2.4.2.1.1 Mechanisms of Data Capturing

There are two mechanisms of data capturing in the OSPI module. They can be combined in some parts to ensure reliable sampling solution independent on the system requirements and the controller configuration. The mechanisms are as follows:

- Data capturing mechanism using taps
- Data capturing mechanism using PHY module.

12.3.2.4.2.1.2 Data Capturing Mechanism Using Taps

This section describes the data capturing mechanism where sampling point is adjusted for one of the reference clock edges inside divided OSPI clock.

After POR, the adapted loopback clock circuit and the OSPI_RCLK delay register line both wake in a disabled state. The OSPI_RD_DATA_CAPTURE_REG register provides the control for the mechanism using taps.

OSPI_RD_DATA_CAPTURE_REG[5] SAMPLE_EDGE_SEL_FLD bit selects the edge of the reference clock, on which data outputs from flash memory are sampled.

OSPI_RD_DATA_CAPTURE_REG[4-1] DELAY_FLD bit field controls the additional number of read data capture cycles (this is the fast reference clock, running at least x4 of the device clock) that should be applied to the internal read data capture circuit. The large clock-to-out delay of the flash memory together with trace delays as well as other device delays may impose a maximum flash clock frequency which is less than the flash memory device itself can operate at. To compensate, software shall set this register to a value that guarantees robust data captures.

12.3.2.4.2.1.3 Data Capturing Mechanism Using PHY Module

PHY module is responsible for data capturing. More detailed description of all internal PHY sampling mechanisms is included in Section 12.3.2.4.16.2 , *Read Data Capturing by the PHY Module*.

12.3.2.4.2.1.4 External Pull Down on DQS

Per the OSPI protocol, the FLASH device drives DQS while CS is asserted. When CS is not asserted the FLASH device presents HiZ on DQS. When configured to use DQS, the controller uses the DQS as a clock, which samples the incoming data into a FIFO. Noise on the DQS when it is HiZ can cause spurious false triggering of the FIFO and filling it with invalid data. There is no way to clear this data except to reset the OSPI module.

To avoid this issue, it is recommended to add a pull down on the DQS line.

During device wakeup, before the IO ring is configured properly, the CS to the FLASH device is HiZ. Depending on the actual level of the CS line the FLASH device might drive the DQS High, Low or HiZ. A pull down on DQS forces the DQS input to Low, but the DQS might still be High or in the presence of noise there might be transitions between Low and High. This again can cause the same issue of capturing garbage data in the Controller FIFO.

To avoid this issue it is recommended to release the OSPI from reset only after the IO ring is configured properly.

12.3.2.4.3 OSPI Power Management

Note

The OSPI module does not provide any hardware signal for busy or idle status. Software need to ensure that the OSPI module is idle before clocks can be shut off by reading the OSPI_CONFIG_REG[31] IDLE_FLD bit.

OSPI_PCLK and OSPI_HCLK share the same clock stop request/acknowledge and clock enable/acknowledge interface.

12.3.2.4.4 Auto HW Polling

The OSPI controller is capable of automatically testing the Flash device busy bit to guarantee no reads or writes are ignored by the flash when it is busy burning in programmed data.

At the end of a programming transaction, the Flash device goes into a burn-in state and becomes busy.

When Auto HW Polling is enabled, the OSPI controller keeps track of programming transactions and will initiate a Flash status read polling transactions automatically, until Flash indicates it is not busy, before any additional data read or programming operations are sent to the flash device. See OSPI_WRITE_COMPLETION_CTRL_REG register and the associated registers.

The OSPI controller requires that the OSPI_WRITE_COMPLETION_CTRL_REG[23-16] POLL_COUNT_FLD field should always be set with values greater or equal to 3 (>=3).

12.3.2.4.5 Flash Reset

OSPI provides Flash reset out ports. These ports are active low and controlled thru OSPI_CONFIG_REG register.

12.3.2.4.6 OSPI Memory Regions

Table 12-235 shows the OSPI memory map in MAIN domain.

Table 12-247. OSPI Memory Map

Address Range	Size	Description
FSS0_OSPI0		
0x0 0FC4 0000 to 0x0 0FC4 00FF	256 B	Configuration registers space
0x0 0FC4 4000 to 0x0 0FC4 41FF	512 B	Global control registers space
0x0 0071 6000 to 0x0 0071 63FF	1 KB	OSPI_ECC_AGGR registers space

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Note

For more information about the memory space, see *FSS Memory Regions*.

12.3.2.4.7 OSPI Interrupt Requests

The OSPI module generates three interrupts. The ECC interrupts (FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_0 and FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_0) are generated by the OSPI ECC aggregator.

The other interrupt (FSS0_OSPI_0_OSPI_LVL_INTR_0) is generated by the OSPI module.

Table 12-236 lists the event flags and the corresponding mask bits of the sources which can cause interrupts.

Table 12-248. OSPI Events

Event Flag	Event Mask	Description
OSPI_IRQ_STATUS_REG[0] MODE_M_FAIL_FLD	OSPI_IRQ_MASK_REG[0] MODE_M_FAIL_MASK_FLD	Event Flag and Event Mask for the OSPI Interrupts.
OSPI_IRQ_STATUS_REG[1] UNDERFLOW_DET_FLD	OSPI_IRQ_MASK_REG[1] UNDERFLOW_DET_MASK_FLD	
OSPI_IRQ_STATUS_REG[2] INDIRECT_OP_DONE_FLD	OSPI_IRQ_MASK_REG[2] INDIRECT_OP_DONE_MASK_FLD	
OSPI_IRQ_STATUS_REG[3] INDIRECT_READ_REJECT_FLD	OSPI_IRQ_MASK_REG[3] INDIRECT_READ_REJECT_MASK_FLD	
OSPI_IRQ_STATUS_REG[4] PROT_WR_ATTEMPT_FLD	OSPI_IRQ_MASK_REG[4] PROT_WR_ATTEMPT_MASK_FLD	
OSPI_IRQ_STATUS_REG[5] ILLEGAL_ACCESS_DET_FLD	OSPI_IRQ_MASK_REG[5] ILLEGAL_ACCESS_DET_MASK_FLD	
OSPI_IRQ_STATUS_REG[6] INDIRECT_XFER_LEVEL_BREACH_FLD	OSPI_IRQ_MASK_REG[6] INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	
OSPI_IRQ_STATUS_REG[7] RECV_OVERFLOW_FLD	OSPI_IRQ_MASK_REG[7] RECV_OVERFLOW_MASK_FLD	
OSPI_IRQ_STATUS_REG[8] TX_FIFO_NOT_FULL_FLD	OSPI_IRQ_MASK_REG[8] TX_FIFO_NOT_FULL_MASK_FLD	
OSPI_IRQ_STATUS_REG[9] TX_FIFO_FULL_FLD	OSPI_IRQ_MASK_REG[9] TX_FIFO_FULL_MASK_FLD	
OSPI_IRQ_STATUS_REG[10] RX_FIFO_NOT_EMPTY_FLD	OSPI_IRQ_MASK_REG[10] RX_FIFO_NOT_EMPTY_MASK_FLD	
OSPI_IRQ_STATUS_REG[11] RX_FIFO_FULL_FLD	OSPI_IRQ_MASK_REG[11] RX_FIFO_FULL_MASK_FLD	
OSPI_IRQ_STATUS_REG[12] INDRD_SRAM_FULL_FLD	OSPI_IRQ_MASK_REG[12] INDRD_SRAM_FULL_MASK_FLD	
OSPI_IRQ_STATUS_REG[13] POLL_EXP_INT_FLD	OSPI_IRQ_MASK_REG[13] POLL_EXP_INT_MASK_FLD	
OSPI_IRQ_STATUS_REG[14] STIG_REQ_INT_FLD	OSPI_IRQ_MASK_REG[14] STIG_REQ_MASK_FLD	
OSPI_IRQ_STATUS_REG[16] RX_CRC_DATA_ERR_FLD	OSPI_IRQ_MASK_REG[16] RX_CRC_DATA_ERR_MASK_FLD	
OSPI_IRQ_STATUS_REG[17] RX_CRC_DATA_VAL_FLD	OSPI_IRQ_MASK_REG[17] RX_CRC_DATA_VAL_MASK_FLD	
OSPI_IRQ_STATUS_REG[18] TX_CRC_CHUNK_BRK_FLD	OSPI_IRQ_MASK_REG[18] TX_CRC_CHUNK_BRK_MASK_FLD	

Table 12-248. OSPI Events (continued)

Event Flag	Event Mask	Description
OSPI_IRQ_STATUS_REG[19] ECC_FAIL_FLD	OSPI_IRQ_MASK_REG[19] ECC_FAIL_MASK_FLD	
OSPI_ECC_DED_STATUS_REG0[0] SRAM_PEND	OSPI_ECC_DED_ENABLE_SET_REG0[0] SRAM_ENABLE_SET OSPI_ECC_SEC_ENABLE_CLR_REG0[0] SRAM_ENABLE_CLR	Event Flag and Event Mask for the ECC Interrupts.
OSPI_ECC_DED_STATUS_REG0[0] SRAM_PEND	OSPI_ECC_DED_ENABLE_SET_REG0[0] SRAM_ENABLE_SET OSPI_ECC_SEC_ENABLE_CLR_REG0[0] SRAM_ENABLE_CLR	
OSPI_ECC_AGGR_STATUS_SET[1-0] PARITY	OSPI_ECC_AGGR_ENABLE_SET[0] PARITY	
OSPI_ECC_AGGR_STATUS_SET[3-2] TIMEOUT	OSPI_ECC_AGGR_ENABLE_SET[1] TIMEOUT	
OSPI_ECC_AGGR_STATUS_CLR[1-0] PARITY	OSPI_ECC_AGGR_ENABLE_CLR[0] PARITY	
OSPI_ECC_AGGR_STATUS_CLR[3-2] TIMEOUT	OSPI_ECC_AGGR_ENABLE_CLR[1] TIMEOUT	

12.3.2.4.8 OSPI Data Interface

12.3.2.4.8.1 Data Interface Address Remapping

The incoming data interface address, by default, maps directly to the address sent serially to the FLASH device. If the FLASH device has a 24-bit address, then the 24 LSB's of the data address is forwarded. A remap feature is available to remap all incoming data addresses to ADDRESS + N, where N is the value stored in the OSPI_REMAP_ADDR_REG[31-0] VALUE_FLD bit field. It is enabled via the OSPI_CONFIG_REG[16] ENB_AHB_ADDR_REMAP_FLD bit. This feature could be used when software needs to move boot code to another FLASH region.

12.3.2.4.8.2 Write Protection

In order to protect the FLASH device, a software controlled write protection feature is supported. Any data write detected (by using DAC), pointing to an area of the FLASH that is protected, is not permitted.

A programmable region of the FLASH device, defined as a number of FLASH 'blocks' starting from a particular block number can be protected. Three programmable registers are provided. The first OSPI_LOWER_WR_PROT_REG register defines the FLASH block that is located at the bottom of the region to be protected. The second OSPI_UPPER_WR_PROT_REG register defines the FLASH block that is located at the top of the region to be protected. The third OSPI_WR_PROT_CTRL_REG register is a control register consisting of 2 bits. The OSPI_WR_PROT_CTRL_REG[0] INV_FLD bit allows software to invert the region that is being protected, causing the programmed region to become the only areas of FLASH memory that is not protected from writes. The OSPI_WR_PROT_CTRL_REG[1] ENB_FLD bit is the write protection enable bit. When this bit is set to 0, the FLASH device is unprotected.

For implementation, the data interface must map the incoming address into its associated FLASH block. A block can be between 1 and 65 KB, programmed via the OSPI_DEV_SIZE_CONFIG_REG register.

12.3.2.4.8.3 Access Forwarding

For legal accesses, the data interface will forward all accesses to one of two access controllers - the direct access and the indirect access controllers. Assuming DAC has been enabled via the OSPI_CONFIG_REG[7] ENB_DIR_ACC_CTRL_FLD bit, then by default all accesses will be forwarded to this controller. Before any accesses can be forwarded to INDAC, it must first be configured by software. This process is fully explained in Section 12.3.2.4.10 , *Indirect Controller (INDAC)*. If DAC is disabled, any incoming access that cannot be forwarded to INDAC will be completed immediately with an error. If DAC is enabled, the same access will be forwarded and serviced by DAC.

12.3.2.4.9 OSPI Direct Access Controller (DAC)

Direct access refers to the operation where data interface accesses directly trigger a read or write to FLASH memory. It is memory mapped and can be used to both access and directly execute code from external FLASH memory. Any incoming access that is not recognized as being within the programmable indirect trigger region is assumed to be a direct access and will be serviced by the DAC. Note that accesses that use DAC do not use the embedded SRAM. The data transfer stops when read or write burst is carried out. The amount of wait states applied will be dependent on the latency through the controller. Latency is kept to a minimum when the use of XIP read instructions are enabled (see OSPI_CONFIG_REG[18] ENTER_XIP_MODE_IMM_FLD and OSPI_CONFIG_REG[17] ENTER_XIP_MODE_FLD bits).

12.3.2.4.10 OSPI Indirect Access Controller (INDAC)

12.3.2.4.10.1 Indirect Read Controller

The aim of the indirect mode of operation is to read significant numbers of bytes from FLASH memory without requiring a data interface access to trigger it. Instead indirect operations are controlled and triggered by software via specific control/configuration Indirect Read Transfer registers (OSPI_INDIRECT_READ_XFER_CTRL_REG, OSPI_INDIRECT_READ_XFER_WATERMARK_REG, OSPI_INDIRECT_READ_XFER_START_REG, and OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG). This block will communicate with an embedded low level SPI protocol state machine module to perform an efficient and optimized FLASH read burst, placing the read data into the local SRAM module ready for fast and low latency delivery to any external controller.

By default, the Indirect Read controller is disabled. Before enabling it, software must configure how much data is required and the start address. The start address and total number of bytes to be fetched is defined in OSPI_INDIRECT_READ_XFER_START_REG and OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG registers, respectively. Up to two indirect operations can be programmed at any one time. The second operation can be triggered while the first is in progress. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. For more information refer to Section 12.3.2.4.10.3 , *Indirect Access Queuing*.

The total number of bytes to read in an indirect operation is not limited by the size of the SRAM. The size of SRAM will only limit the size of requests. In the case of SRAM overrun, the controller will back pressure FLASH reads until space becomes available in the SRAM. Back pressuring the reads on the SPI interface is handled by completing any current read burst, waiting until space in the SRAM becomes available and then issuing a new read burst at the address where the previous terminated burst ended.

An external controller will be able to fetch the data that the controller has read from external FLASH memory by issuing data interface reads to the OSPI module. The address of the incoming read access must be in the range of indirect trigger address programmed via the OSPI_IND_AHB_ADDR_TRIGGER_REG register to indirect trigger address + 2**(indirect trigger address range) - 1. Default value of the range is equal to 16 locations. This allows a 16-beat burst to be applied starting from the indirect trigger address. The smaller bursts are possible to handle effectively as well with this approach. Furthermore it is not strict requirement to push consecutive address sequence. Actual address just has to be in the indirect range to grant SRAM as source. Each valid Indirect Read will cause the internal SRAM to be popped, thereby decoupling the incoming read access address from the FLASH address – that is not direct mapped. Therefore the indirect trigger address does not have any relationship with the FLASH address. It is just to indicate that data should take the SRAM as source instead of the FLASH memory array after triggering of any valid Indirect Read. The FLASH address for Indirect Read is taken from the OSPI_INDIRECT_READ_XFER_START_REG register. Assuming the requested data is present in the SRAM at the point the data interface access is received by the OSPI module, then the data will be fetched from the SRAM and the response to the read burst will be achieved with minimum latency. Once the data has been read from the SRAM, the OSPI module will free up the associated resource in the SRAM.

If a read access is received whose address is not within the range described above then that access will not be completed using the indirect controller. It will instead be serviced by the direct access controller.

If a read access is received whose address is within the range described above but the requested data is not immediately present in the SRAM then wait states will be applied until the data has been read from FLASH and pushed to the SRAM.

If a read burst is received whose access elements traverse the Indirect trigger range, then the accesses within the Indirect trigger range will be processed by the indirect controller and the rest will be taken by the direct access controller. This is likely to be a software configuration error.

The external controller is only permitted to issue 32-bit data interface reads until the last word of an indirect transfer. This helps keep the SRAM control logic less complex. On the final read, the external controller may issue a 16-bit (Halfword) or byte access to complete the transfer. It is also permitted for the external controller to always issue a 32-bit Word read on the last indirect access. The controller will pad the upper bits of the response with zero. The current expectation is that the SRAM will be kept fairly full while the read operation is carried out. The fill level of the SRAM is directly readable by software reading the OSPI_SRAM_FILL_REG register.

An indirect operation may be cancelled at any time by setting 1 to OSPI_INDIRECT_READ_XFER_CTRL_REG[1] CANCEL_FLD bit.

Any bus controller should be allowed to initiate an indirect access. The OSPI module provide software access mechanism to the SRAM fill-level directly via configuration registers and then decide for itself when the data should be fetched from the local SRAM. The fill level watermark register (see OSPI_INDIRECT_READ_XFER_WATERMARK_REG register) is provided. When the SRAM fill level passes this watermark, an interrupt is generated. If the watermark value is > 0, the watermark interrupt is also generated when the final byte of data has been read by the OSPI module and placed in the SRAM, even if the actual SRAM fill level has not risen above the watermark. This last feature is useful to avoid software tracking how much data has been read and resetting the watermark value for the last few bytes of an indirect read transfer.

Two further interrupt sources are provided to help understand the status of an indirect operation. Firstly, an interrupt is generated when an indirect operation has completed. Secondly, an interrupt is generated if an Indirect Read operation was requested but could not be accepted due to the fact 2 indirect operations have already been buffered by the OSPI module.

Setting the OSPI_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit starts an indirect read operation. OSPI_INDIRECT_READ_XFER_CTRL_REG[2] RD_STATUS_FLD bit is available to check the status.

12.3.2.4.10.1.1 Indirect Read Transfer Process

The following sequence can be followed:

1. Setup OSPI_CONFIG_REG register.
2. Setup the indirect transfer's FLASH start address in the OSPI_INDIRECT_READ_XFER_START_REG register.
3. Setup the number of bytes to be transferred in the OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG register.
4. Setup the indirect transfer's trigger address in the OSPI_IND_AHB_ADDR_TRIGGER_REG register.
5. Setup the indirect transfer's trigger address range in the OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG register.
6. If the watermark interrupt feature is to be used, set the OSPI_INDIRECT_READ_XFER_WATERMARK_REG register which will cause an interrupt to be generated when the fill level increases beyond the watermark level. Setting the watermark can be useful indication to software when to read the next part of the indirect read transfer. Note that if the watermark is set to a value

other than zero, the watermark interrupt will always trigger once the final byte of indirect transfer has been fetched and placed in the embedded SRAM, even if the watermark value is higher than the actual completed fill level.

7. Trigger Indirect Read access by setting the OSPI_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit to 1.
8. If the watermark interrupt feature is to be used, wait for watermark interrupt. Else poll the SRAM fill level via the OSPI_SRAM_FILL_REG register to decide when sufficient data is in the SRAM to trigger data fetches.
9. Read the expected amount of data from SRAM. If there is still more data to fetch in order to complete the indirect read transfer, then loop back to step 8. Otherwise continue to step 10.
10. The completion status of the Indirect Read operation can be polled via the OSPI_INDIRECT_READ_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD bit.
11. An Indirect Complete interrupt will be generated when the Indirect read operation has completed.

12.3.2.4.10.2 Indirect Write Controller

The aim of the indirect mode of operation is to perform bulk transfer of data from the processor into a FLASH memory in the most efficient manner. The fewest possible write cycles inside the FLASH device will be carried out for the indirect transfer, thus maximizing the life of the device. Indirect write operation can be thought of from a software perspective as the inverse of the indirect read. It is controlled and triggered by software via specific control/configuration Indirect Write Transfer registers (for more information see the following registers: OSPI_INDIRECT_WRITE_XFER_CTRL_REG, OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG, OSPI_INDIRECT_WRITE_XFER_START_REG, and OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG). This block will await delivery of the write data via the external data interface controller, placing it in the local SRAM before communicating with the existing legacy SPI core to perform an efficient and optimized FLASH write burst.

By default, the indirect write controller is disabled. Before enabling it, the software must configure how much data is required and the start address. The start address and total number of bytes to be written is defined in OSPI_INDIRECT_WRITE_XFER_START_REG and OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG registers, respectively. Up to two indirect operations can be programmed at any one time. The second operation can be triggered while the first is in progress. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. The Indirect write queuing is very similar to indirect read queuing. For more information refer to Section 12.3.2.4.10.3 , *Indirect Access Queuing*.

The total number of bytes to write in an indirect operation is not limited by the size of the SRAM. The size of SRAM will only limit the amount of data that can be accepted from the external controller. In the case of an SRAM overrun, the controller will back pressure the data interface with wait states. Note the fill level of the SRAM is readable via programmable OSPI_SRAM_FILL_REG register and this can be used to avoid this situation.

An external controller will provide the write data and will transfer this to the OSPI module by issuing data interface writes. The address of the incoming write access must be in the range of Indirect trigger address programmed via the OSPI_IND_AHB_ADDR_TRIGGER_REG register to Indirect trigger address + 2**(Indirect trigger address range) - 1. Default value of the range is equal to 16 locations. This allows a 16-beat burst to be applied starting from the Indirect trigger address. The smaller bursts are possible to handle effectively as well with this approach. Furthermore it is not strict requirement to push consecutive address sequence. Actual address just has to be in the Indirect Range to grant SRAM as source. Each write will cause the internal SRAM to be pushed, thereby decoupling the incoming write access address from the FLASH address – that is not direct mapped. Therefore Indirect trigger address does not have any relationship with FLASH address. It is just to indicate that data should take SRAM as source instead of FLASH Memory array after triggering of any valid Indirect Write. The FLASH address for Indirect Write is taken from the OSPI_INDIRECT_WRITE_XFER_START_REG register. Assuming the SRAM is not full at the point the data interface access is received by the OSPI module, then the data will be pushed to the SRAM with minimum latency.

If a write access is received whose address is not within the range described above then that access will not be completed using the indirect controller. It will instead be serviced by the direct access controller.

If a write access is received whose address is within the range described above but the SRAM is full then wait states will be applied until some or all of the data has been pushed from the SRAM to the FLASH.

If a write burst is received whose access elements traverse the Indirect trigger range, then the accesses within the Indirect trigger range will be processed by the indirect controller, and the rest will be taken by the direct access controller. This is likely to be a software configuration error.

The external controller is only permitted to issue 32-bit data interface writes until the last word of an indirect transfer. This helps keep the SRAM control logic less complex. On the final write, the external controller may issue a 32-bit word, 16-bit (halfword) or a byte access to complete the transfer. If the number of bytes to write is less than 4 on the last transfer, the controller is still permitted to issue a 32-bit transfer. In these cases, the extra bytes are discarded by the controller.

When the SRAM holds a number of bytes equal to or greater than the size of a FLASH page (which itself is programmed into the OSPI module, with a default of 256 bytes) or when the SRAM holds all remaining bytes of the currently executing indirect transfer, the OSPI module will initiate a write burst to the flash command generator.

An indirect operation may be cancelled at any time by setting 1 to the OSPI_INDIRECT_WRITE_XFER_CTRL_REG[1] CANCEL_FLD bit.

Any bus controller should be allowed to initiate an indirect access. The OSPI module provide software access mechanism to the SRAM fill-level directly via the configuration registers and then decide for itself when the data should be written to the local SRAM. The fill level watermark register (see OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG register) is provided. When the SRAM fill level falls below this watermark, an interrupt is generated.

Two further interrupt sources are provided to help understand the status of an indirect operation. Firstly, an interrupt is generated when an indirect operation has completed. Secondly, an interrupt is generated if an indirect write operation was requested but could not be accepted due to the fact 2 indirect operations have already been buffered by the OSPI module.

Setting the OSPI_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit starts an indirect write operation. The OSPI_INDIRECT_WRITE_XFER_CTRL_REG[2] WR_STATUS_FLD bit is available to check the status.

12.3.2.4.10.2.1 Indirect Write Transfer Process

The following sequence can be followed:

1. Setup OSPI_CONFIG_REG register.
2. Setup the indirect transfer’s FLASH start address in the OSPI_INDIRECT_WRITE_XFER_START_REG register.
3. Setup the number of bytes to be transferred in the OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG register.
4. Setup the indirect transfer’s trigger address in the OSPI_IND_AHB_ADDR_TRIGGER_REG register.
5. Setup the indirect transfer's trigger address range in the OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG register.
6. It is functionally valid for software to simply write all the data to the SRAM in one block transfer. However, if the total number of bytes to write is greater than the size of the partitioned SRAM, then it is quite likely the SRAM will become full causing the OSPI to back-pressure the system data bus for a considerable time. This time is based on the FLASH data-rate and the page-write time of the device. To avoid sending all the write data in one block transfer, software can make use of the watermark interrupt to identify a convenient time to send data a page at a time to the SRAM module. Alternatively, software can poll the SRAM fill level register directly to identify how empty the SRAM is at any one time in order to make a judgment as to when the most practical time to send the next part of the transfer.

7. If the watermark interrupt feature is to be used, set the OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG register which will cause an interrupt to be generated when the fill level falls below the watermark. The watermark should be set to a number between zero and a page size. That is if the page size is 256 bytes, then setting the watermark to a value between 10 and 250 is reasonable and will cause the interrupt to trigger when the fill level drops below the programmed number. Setting the watermark can be useful to provide an indication to software when to write the next page of data to the SRAM.
8. Trigger Indirect Write access by setting OSPI_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit.
9. If the remaining number of bytes still to be transferred into the SRAM for the current indirect transfer is greater than a FLASH page, then write 1 FLASH page worth of data to the SRAM. Otherwise send the remaining data from the indirect transfer to SRAM.
10. If all the data in the indirect transfer has now been sent to the SRAM, then go to 12 and await indirect complete status. Otherwise if there is more data still to be transferred then either:
    - If the watermark interrupt feature is being used, then wait for watermark interrupt.
    - Alternatively the SRAM fill level can be interrogated to identify a convenient time to send more data.
11. Loop back to 9.
12. Optional: The completion status of the Indirect write operation can be polled via OSPI_INDIRECT_WRITE_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD.
13. An Indirect Complete interrupt will be generated when the Indirect write operation has completed.

12.3.2.4.10.3 Indirect Access Queuing

Software is permitted to queue up to two indirect transfers for both the indirect write controller and the indirect read controller. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. Any attempt to queue more than two operations will cause an interrupt to be generated. To take advantage of this feature, software should attempt to keep both indirect programming slots full at all times.

From the software perspective, indirect access queuing is achieved by triggering bit 0 of the indirect transfer control register (OSPI_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit or OSPI_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit) twice in short succession. The indirect number of bytes register (OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG or OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG register) and the indirect FLASH start address register (OSPI_INDIRECT_READ_XFER_START_REG or OSPI_INDIRECT_WRITE_XFER_START_REG register) must be setup with the relevant transfer data before START_FLD bit can be triggered for each transfer. Since these registers will change regularly, the hardware must keep sampled versions of these registers for the duration of the indirect transfer.

The internal register block will only issue an indirect start trigger to the key underlying datapath blocks one at a time. There are 2 independent datapath blocks in the indirect access controller that will receive and independently sample this information. The first is the datapath block on the data bus side of the SRAM. For indirect reads, this is a read interface, for indirect writes, it is a write interface. The second is the datapath block on the FLASH side of the SRAM. For indirect reads, this is a write interface, for indirect writes, it is a read interface. Both blocks will process the indirect transfers at different times. For example, for an indirect read operation, the datapath block on the FLASH side of the SRAM will be able to start processing the second queued transfer as soon as the last byte of the first transfer has been written to the SRAM. Before commencing the second transfer, this block must resample the OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG and OSPI_INDIRECT_READ_XFER_START_REG registers. Similarly, the datapath block on the bus side will resample the same registers locally when it has forwarded all the FLASH data associated with the first indirect transfer from the SRAM onto the data bus.

12.3.2.4.10.4 Consecutive Writes and Reads Using Indirect Transfers

It is permitted for software to trigger an indirect read operation while an indirect write operation is in progress. Similarly it is permitted to trigger an indirect write while an indirect read operation is in progress. Indirect write operations will take overall precedence.

12.3.2.4.10.5 Accessing the SRAM

The SRAM depth is separated in two segmets. The lower segment is reserved for indirect read use. The upper segment is for indirect write use only. The size of each segment is programmable via the OSPI_SRAM_PARTITION_CFG_REG register. This feature allows to allocate how many bits of the SRAM address bus are allocated to indirect read. By default, this is set so that exactly half of the SRAM is portioned for use by the indirect read controller. To ensure the read data bus is not directly fed by the SRAM read data through combinatorial logic, an extra bank of holding registers is included in the indirect read data path. These registers act as an extra location to be added to the allocated number of SRAM locations for indirect read.

To illustrate how the SRAM (and the extra bank of holding registers) can be allocated between indirect read and write, the following example is provided. The depth of the SRAM in this example is configured to be 8 bits. This is equal to 256 locations.

- If the OSPI_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x00, then 256 locations are allocated to indirect writes and 1 location to indirect reads.
- If the OSPI_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x01, then 255 locations are allocated to indirect writes and 2 locations to indirect reads.
- If the OSPI_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x02, then 254 locations are allocated to indirect writes and 3 locations to indirect reads.
- And so on until.
- If the OSPI_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFD, then 3 locations are allocated to indirect writes and 254 locations to indirect reads.
- If the OSPI_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFE, then 2 locations are allocated to indirect writes and 255 locations to indirect reads.
- If the OSPI_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFF, then 1 location is allocated to indirect writes and 256 locations to indirect reads.

Note

A value of 0xFF or 0x00 in the OSPI_SRAM_PARTITION_CFG_REG register should be avoided by software, as only the bottom 8 bits of the SRAM fill level are accessible through software (up to 255 limit) via the OSPI_SRAM_FILL_REG register. If the fill level reaches 256 on either the indirect read or write side, it will appear when reading the Fill Level to be 0.

There are four SRAM sources that are arbitrated and muxed onto the single SRAM port. Up to three sources can access this port at any one time. The sources are described as follows:

- Indirect Write, Write source. This is located on the data bus side of the SRAM.
- Indirect Write, Read source. This is located on the FLASH side of the SRAM.
- Indirect Read, Write source. This is located on the FLASH side of the SRAM.
- Indirect Read, Read source. This is located on the data bus side of the SRAM.

A fixed priority arbitration scheme is implemented. Table 12-237 shows priority allocated to these sources.

Table 12-249. SRAM Access Priority

SRAM Access Priority		
Indirect Write	Write to SRAM (from System Data Bus)	3rd (exclusive with Data Bus Read Request)
	Read from SRAM (from OSPI Module)	2nd
Indirect Read	Write to SRAM (from OSPI Module)	1st
	Read from SRAM (from System Data Bus)	3rd (exclusive with Data Bus Write Request)

Note

With the exception of the write port during an Indirect Read operation (on the FLASH side of the SRAM), the logic driving all four sources must not assume single cycle completion. Writes to the SRAM during an indirect read must be allowed to complete immediately to avoid data loss. Therefore this port is given maximum priority.

12.3.2.4.11 OSPI Software-Triggered Instruction Generator (STIG)

The DAC and INDAC are used to transfer data. In order to access the volatile and non-volatile configuration registers, the legacy SPI Status register, other status/protection registers as well as to perform ERASE functions, a separate software controller is required. The software triggered instruction generator (STIG) is controlled using the OSPI_FLASH_CMD_CTRL_REG register by setting up the command to issue to the FLASH device. This is a generic controller and can be used to perform any instruction that the FLASH device supports from the extended SPI protocol. Configuring of instructions which are not compliant with the specification of the FLASH devices could cause unpredicted behavior of the controller. OSPI_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD bits should be set different than OSPI_DEV_INSTR_RD_CONFIG_REG[7-0] RD_OPCODE_NON_XIP_FLD and OSPI_DEV_INSTR_WR_CONFIG_REG[7-0] WR_OPCODE_FLD. The OSPI_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD bit is used to trigger the command. The OSPI_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit is used by software to poll the status of the command execution. For reads, when the command has been serviced (OSPI_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit toggles from '1' to '0'), up to 8 bytes of read data will be placed in the OSPI_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_RD_DATA_UPPER_REG registers. For writes, the write data should be placed in the OSPI_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_WR_DATA_UPPER_REG registers.

The completion of the STIG request could be also checked by the corresponding interrupt. The occurrence of the interrupt indicates that the controller is ready for accepting a new STIG request. It is important to notice that completion of the STIG request is not equivalent to completion it on SPI side. For example, if STIG is configured to the command composed of data to transmit only, the data is taken from the corresponding STIG register fields and put into TX FIFO. Since all bytes to write are known, another STIG can be queued before serialization of the current one is completed.

There are some commands which require more data to read than 8 bytes (for example READ ID command). The additional STIG Memory Bank is implemented in order to accommodate these data if needed. The STIG Memory Bank (internal component of the controller) is controlled by the OSPI_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD bit. If enabled, the number of bytes to read in the STIG is extended to 16 as defined in OSPI_FLASH_COMMAND_CTRL_MEM_REG[18-16] NB_OF_STIG_READ_BYTES_FLD bit field. It should be noticed that there are very few commands (excluding Read Array ones which are not intended to handle effectively in STIG Mode but in Direct/Indirect Modes) which return more than 8 bytes to the controller. If the maximum number of bytes to Read using STIG in target application is less than 16, the depth of the STIG Memory Bank can be set smaller what will result in saving noticeable part of the area.

If number of bytes to Read in the STIG as defined in OSPI_FLASH_COMMAND_CTRL_MEM_REG[18-16] NB_OF_STIG_READ_BYTES_FLD bit field exceeds the Memory Bank Depth, remaining data will overwrite the STIG Memory Bank locations starting from its first address. OSPI_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_RD_DATA_UPPER_REG keep the last 8 bytes read from the Flash Device by STIG when Memory Bank is enabled. Therefore, for example if the user wants to get just a single byte from the last eight bytes from long continuous read SPI data chain, there is no need to access the STIG Memory Bank since data can be taken from suitable Flash Command Read Data register. In order to access more data, STIG Memory Bank data request should be triggered. It is controlled by the OSPI_FLASH_COMMAND_CTRL_MEM_REG and works analogously for triggering STIG from the functional standpoint.

OSPI_FLASH_COMMAND_CTRL_MEM_REG[0] TRIGGER_MEM_BANK_REQ_FLD bit is used to trigger the command, bit OSPI_FLASH_COMMAND_CTRL_MEM_REG[1] MEM_BANK_REQ_IN_PROGRESS_FLD is used by software to poll the status of the command execution. When

MEM_BANK_REQ_IN_PROGRESS_FLD bit toggles from "1" to "0", the byte of data (OSPI_FLASH_COMMAND_CTRL_MEM_REG[15-8] MEM_BANK_READ_DATA_FLD) from corresponding address (OSPI_FLASH_COMMAND_CTRL_MEM_REG[28-20] MEM_BANK_ADDR_FLD bit field) is valid. The address should be set before triggering the STIG Memory Bank access. Each consecutive STIG access overwrites the previous one so that the data in the Bank always fit into byte index fetched by the last STIG access configured to use the Memory Bank (first incoming byte equals first address of the Memory Bank, second one equals the second address and so on).

12.3.2.4.11.1 Servicing a STIG Request

A STIG request will cause the OSPI Flash controller to interrogate the OSPI_FLASH_CMD_CTRL_REG register to determine what and how many bytes it should send to the FLASH device. The OSPI_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD field of this register indicate the instruction to be sent and is always pushed first. If there is an address to send, then the address (the size of which is also programmed in the same register) is sent next. The address itself is stored in the OSPI_FLASH_CMD_ADDR_REG register. If Mode bits are enabled by OSPI_FLASH_CMD_CTRL_REG[18] ENB_MODE_BIT_FLD bit. OSPI_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field are being sent right after address. If OSPI_FLASH_CMD_CTRL_REG[18] ENB_MODE_BIT_FLD and OSPI_CONFIG_REG[29] CRC_ENABLE_FLD are both enabled, STIG will replace XIP Mode bits (not applicable for CRC aware SPI interface) for automatically calculated address CRC byte. Therefore, to execute CRC aware STIGs (meaning the commands requiring sending address CRC byte), ENB_MODE_BIT_FLD bit should always be set. If there are any dummy cycles to send (the size of which is also programmed in OSPI_FLASH_CMD_CTRL_REG register) then those are sent next. If there is data to write or read (the size of which is also programmed in OSPI_FLASH_CMD_CTRL_REG register) then for the case of writes, up to 8 bytes can be sent (as stored in the Flash Command Write Data registers, OSPI_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_WR_DATA_UPPER_REG registers) next. In the read case, when the read data has been collected from the FLASH device, the OSPI Flash Controller stores that in the Flash Command Read Data Registers (OSPI_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_RD_DATA_UPPER_REG registers). Up to 8 bytes can be get if OSPI_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD bit is disabled or up to 512 when enabled. When the OSPI Flash controller starts to service a STIG request, it sets the OSPI_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit to indicate a command execution is in progress. When the OSPI Flash controller is in the auto-polling state, servicing a STIG request is slightly different. Most of devices are largely inaccessible after a program operation until the device has completed that write. Some group of them has a possibility to suspend programming page. It can be controlled by the OSPI_POLLING_FLASH_STATUS_REG[8] DEVICE_STATUS_VALID_FLD bit, which indicate active auto-polling phase. After requesting a STIG, the OSPI Flash Controller immediately issues appropriate OPCODE to Memory. During servicing a STIG (in auto-polling phase) the status bit of command execution remains steady and other parts of transfer such as ADDRESS or DUMMY BITS, and so forth, are disabled (to issued Program Suspend Command is needed OPCODE only). There is a programmable option to add delay between every repetitive poll operation (delay is defined by OSPI_WRITE_COMPLETION_CTRL_REG[31-24] POLL_REP_DELAY_FLD bit field). This feature is implemented to free up SPI bandwidth if needed.

Note

The OSPI data is sent LSB first, while address is sent MSB first.

Note

The STIG complete status bit gets cleared before the actual flash access completes. Software should wait for about 700 ns if there is any dependency on actual access completion.

12.3.2.4.12 OSPI Arbitration Between Direct / Indirect Access Controller and STIG

When multiple controllers are active simultaneously, a simple fixed-priority arbitration scheme is used to arbitrate between each interface and access the external FLASH. The fixed priority is defined as follows, highest priority first.

- The Indirect Access Write
- The Direct Access Write
- The STIG
- The Direct Access Read
- The Indirect Access Read

12.3.2.4.13 OSPI Command Translation

Requests issued by the direct access controller, the indirect access controller or the STIG will be translated into a sequence of byte transfers to send downstream (before serialization to the FLASH device). These sequences depend on the requested transfer but an example of a typical 1-byte non sequential READ is shown below:

INSTRUCTION OPCODE -> ADDRESS -> Mode Byte -> Dummy Bytes -> 1 byte of don't care

For sequential accesses, an extra byte of data per read is pushed to the FLASH device on the back of the above sequence assuming it can be done so with no gap between each transferred byte.

When PHY mode is enabled and consequently no clock divider is configured, latency caused by multi domain synchronization may make an extra byte insufficient to avoid the transfer gap. To ensure the sequential access non-interrupted and keep the maximum performance of the controller, PHY Pipeline Mode is implemented. When enabled, number of don't care bytes is calculated based on the configuration.

The actual sequence sent to the FLASH device depends on the requested transfers, whether the transfer is non-sequential or sequential, whether the device has been configured in XIP mode and the state of the main Device Instruction Type programmable registers (OSPI_DEV_INSTR_RD_CONFIG_REG and OSPI_DEV_INSTR_WR_CONFIG_REG).

For writes, the write enable latch (or WEL) within the FLASH device itself must be high before a write sequence can be issued. The OSPI Flash Controller will automatically issue the write enable latch command before triggering a write command via the direct or indirect access controllers (DAC/INDAC) – that is the user does not need to perform this operation. For increasing flexibility and performance user can turn off this feature by setting the OSPI_DEV_INSTR_WR_CONFIG_REG[8] WEL_DIS_FLD bit. The opcode for WREN is typically 0x06 and is common between devices.

When write requests from the direct or indirect access controllers are no longer being received and all outstanding requests have been sent, the FLASH device will automatically start the page program write cycle. Any incoming request at this time will be held in wait states until the cycle has completed. The OSPI Flash Controller will automatically poll the FLASH device legacy SPI status register to identify when the write cycle has completed. This is achieved by sending the RDSR opcode to the FLASH device and waiting until the device itself has indicated the write cycle has completed (until the Write in Progress bit has cleared to zero and the write enable latch bit has also cleared to zero or device is ready bit has set to one). The WREN and the RDSR device instructions are the only ones that are sent by the controller under the hood. For any other specific instruction that the user determines should be sent to the device (for example if the device needs to be unprotected before a write command is issued), these should be handled separately by issuing FLASH commands via the STIG.

There is an option to trigger HOLD or RESET feature on I/Os of the Flash Device. The HOLD one is generally common across the devices and takes an alternative function of DQ3 pin (applicable when device operates neither in Quad SPI mode nor DDR). The transfer can be hold and then resumed by dedicated software trigger field (OSPI_CONFIG_REG[4] HOLD_PIN_FLD). The devices which have the HOLD feature on DQ3 usually need another dedicated pin for hardware reset and ones without HOLD feature usually have alternative reset on DQ3 what makes the additional reset pin being redundant. The controller supports both variants and reset selection register field (OSPI_CONFIG_REG[6] RESET_CFG_FLD) allows the user to configure which hardware reset solution is implemented in the device under usage.

After configuration is done, it is possible to trigger HOLD or RESET features using I/Os (OSPI_CONFIG_REG[4] HOLD_PIN_FLD or OSPI_CONFIG_REG[5] RESET_PIN_FLD bits). After HOLD activation the controller is introduced into waiting state and any other operations should not be requested before de-asserting of HOLD configuration bit. The HOLD feature is useful when any SPI transaction needs to be prolonged in order to adjust it into specific point in time. Note that any HOLD trigger issued during active SPI transaction may be synchronized into reference clock domain at the time the SPI transfer turns to be finished. In this case, there is nothing to hold so the low level SPI logic will not activate HOLD on DQ3. To check if HOLD request suspended the transfer OSPI_CONFIG_REG[31] IDLE_FLD bit can be polled for. If SPI is not in the IDLE state, the transfer was successfully suspended. It is important for the software to take care of resetting OSPI_CONFIG_REG[4] HOLD_PIN_FLD bit before newly triggered SPI transaction. In case HOLD request is set before the beginning of the transfer it will be HOLD right after it starts what may not always be a goal. The hardware RESET needs to be activated when CS is high (no valid transaction is present on SPI bus). It can be checked by polling of OSPI_CONFIG_REG[31]. If the controller is in the IDLE state and no other transfer requests are queued to perform, the hardware RESET can be triggered. The RESET feature is useful when any write, program or erase operation needs to be cancelled. No transfer request is permitted before driving the reset back to being inactive. Triggering HOLD or RESET on DQ3 at the time the device is configured to work in Quad SPI mode or DDR will overwrite transfer data on DQ3 with '0'. This behavior is considered as a software error so it is advisable for the system to make sure that the flash device was introduced to suitable SPI mode (that is by polling its configuration register) before triggering alternative DQ3 function. There are four independent reset outputs implemented to separate between multiple devices connected to the controller (up to 4 are supported). The decision which reset output is to be activated after triggering OSPI_CONFIG_REG[5] RESET_PIN_FLD bit is made based on OSPI_CONFIG_REG[9] PERIPH_SEL_DEC_FLD and OSPI_CONFIG_REG[13-10] PERIPH_CS_LINES_FLD bits. Reset output OSPI_ECC_VECTOR is to be directly driven into corresponding dedicated RESET pins of the devices with separated RESET pin and alternatively, Reset output OSPI_ECC_VECTOR is to be control OSPI_ECC_VECTOR of the DQ3 RESET devices enabling separating of DQ3 Controller Outputs on SoC integration level.

The controller supports all combinations of CPHA and CPOL for Serial Clock. It allows the controller to support any SPI target devices not limited to Flash Memories. Multiple-SPI flash devices use just a subset of these combinations depending on the Transfer Mode as defined in Table 12-238.

Table 12-250. Flash SPI Modes

(SEL_CLK_POL_FLD, SEL_CLK_PHASE_FLD)	Edge Mode	Support
0x00 (SPI MODE 0)	SDR	Yes
0x01 (SPI MODE 1)	SDR	No
0x10 (SPI MODE 2)	SDR	No
0x11 (SPI MODE 3)	SDR	No
0x00 (SPI MODE 0)	DDR	Yes
0x01 (SPI MODE 1)	DDR	No
0x10 (SPI MODE 2)	DDR	No
0x11 (SPI MODE 3)	DDR	No

12.3.2.4.14 Selecting the Flash Instruction Type

In order to send the correct READ and WRITE opcodes, software should initialize the OSPI_DEV_INSTR_RD_CONFIG_REG and the OSPI_DEV_INSTR_WR_CONFIG_REG registers. These registers include fields to setup the required instruction opcodes that is intended to be used to access the FLASH (default is basic READ and basic page program) as well as the instruction type, edge mode (DDR or SDR) and whether the instruction uses single, dual, quad or octal pins for address and data transfer. Providing this level of control to the user provides a future proofed generic solution. To ensure the controller can operate from a reset state, the registers will be reset to an opcode compatible with SIO devices what can be modified using BOOT feature.

Despite being applicable for both READs and WRITEs, the OSPI_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD field only appears once – it is not included in the OSPI_DEV_INSTR_WR_CONFIG_REG register. If software sets this to anything other than '0', then the address transfer type and the data transfer type bits of both OSPI_DEV_INSTR_RD_CONFIG_REG and OSPI_DEV_INSTR_WR_CONFIG_REG registers become don't care. It is made available to allow software to support the less common FLASH instructions where the opcode, address and data are sent on 2 or 4 lanes (the opcode from most instructions are sent serially to the FLASH device, even for dual/quad instructions).

There are devices capable to handling Read Operations in Dual Data Rate Mode (DDR) (it is also called Dual Transfer Rate Mode (DTR)). That means they can issue and capture the data on both rising and falling edges during working with dedicated command type. This enables the controller to maintain throughput at twice lower frequency of OSPI clock. The Device Read Instruction Register has DDR enable bit which informs Octal-SPI Flash Controller that opcode written into Read Opcode field is capable with DDR command type. The other field defined in OSPI_RD_DATA_CAPTURE_REG[19-16] DDR_READ_DELAY_FLD which enables the controller to shift the transmitted data in DDR mode. By default, data are shifted by 1 clock cycle to ensure hold timing greater than 0 during DDR transactions. It may not be sufficient for high reference clock frequency in accordance with the high dividers.

Table 12-239 shows how software should configure the OSPI module for selected specific READ and WRITE instruction supported by the abovementioned device.

Table 12-251. READ and WRITE Instruction Configuration

READ							
OPCODE	OPCODE sent over how many lanes / edge mode?	ADDRESS / DUMMY / MODE sent over how many lanes / edge mode?	DATA bytes sent over how many lanes / edge mode?	Instruction Type (OSPI_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD)	Address transfer type (OSPI_DEV_INSTR_RD_CONFIG_REG[13-12] ADDR_XFER_TYPE_STD_MODE_FLD)	Data transfer type (OSPI_DEV_INSTR_RD_CONFIG_REG[17-16] DATA_XFER_TYPE_EXT_MODE_FLD)	DDR bit enable (OSPI_DEV_INSTR_RD_CONFIG_REG[10] DDR_EN_FLD)
READ	1/SDR	1/SDR	1/SDR	0	0	0	0
FAST_READ	1/SDR	1/SDR	1/SDR	0	0	0	0
DTR_FAST_READ	1/SDR	1/DDR	1/DDR	0	0	0	1
DOFR (Dual O/p Fast Read)	1/SDR	1/SDR	2/SDR	0	0	1	0
DIOFR (Dual I/O Fast Read)	1/SDR	2/SDR	2/SDR	0	1	1	0
DDIOFR (DTR Dual I/ O Fast Read)	1/SDR	2/DDR	2/DDR	0	1	1	1
QOFR (Quad O/p Fast Read)	1/SDR	1/SDR	4/SDR	0	0	2	0
QIOFR (Quad I/O Fast Read)	1/SDR	4/SRD	4/SDR	0	2	2	0
DQIOFR (DTR Quad I/ O Fast Read)	1/SDR	4/DDR	4/DDR	0	2	2	1
OOFR (Octal O/p Fast Read)	1/SDR	1/SDR	8/SDR	0	0	3	0
OIOFR (Octal I/O Fast Read)	1/SDR	8/SDR	8/SDR	0	3	3	0
DOIOFR (DTR Octal O/p Fast Read)	1/SDR	1/DDR	8/DDR	0	0	3	1

Table 12-251. READ and WRITE Instruction Configuration (continued)

4DOIOFR (4-byte DTR Octal I/O Fast Read)	1/SDR	8/DDR	8/DDR	0	3	3	1
DCFR (Dual Command Fast Read)	2/SDR	2/SDR	2/SDR	1	Don't care	Don't care	0
DDCFR (DTR Dual Command Fast Read)	2/SDR	2/DDR	2/DDR	1	Don't care	Don't care	1
QCFR (Quad Command Fast Read)	4/SDR	4/SRD	4/SDR	2	Don't care	Don't care	0
DQCFR (DTR Quad Command Fast Read)	4/SDR	4/DDR	4/DDR	2	Don't care	Don't care	1
OCFR (Octal Command Fast Read)	8/SDR	8/SDR	8/SDR	3	Don't care	Don't care	0
4DOCFR (4-byte DTR Octal Command Fast Read)	8/SDR	8/DDR	8/DDR	3	Don't care	Don't care	1
WRITE							
OPCODE	OPCODE sent over how many lanes?	ADDRESS / DUMMY / MODE sent over how many lanes?	DATA bytes sent over how many lanes?	Instruction Type (OSPI_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD)	Address transfer type (OSPI_DEV_INSTR_WR_CONFIG_REG[13-12] ADDR_XFER_TYPE_STD_MODE_FLD)	Data transfer type (OSPI_DEV_INSTR_WR_CONFIG_REG[17-16] DATA_XFER_TYPE_EXT_MODE_FLD)	
PP	1	1	1	0	0	0	
DIFP (Dual Input Fast Program)	1	1	2	0	0	1	
DIEFP (Dual Input Extended Fast Program)	1	2	2	0	1	1	
QIFP (Quad Input Fast Program)	1	1	4	0	0	2	
QIEFP (Quad Input Extended Fast Program)	1	4	4	0	2	2	
OIFP (Octal Input Fast Program)	1	1	8	0	0	3	
OIEFP (Octal Input Extended Fast Program)	1	8	8	0	3	3	
DCPP (Dual Command Fast Program)	2	2	2	1	Don't care	Don't care	
QCPP (Quad Command Fast Program)	4	4	4	2	Don't care	Don't care	

Table 12-251. READ and WRITE Instruction Configuration (continued)

OCPP (Octal Command Fast Program)	8	8	8	3	Don't care	Don't care

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Note

This data are applicable for both 3-byte or 4-byte address variants of the commands if did not indicate otherwise.

Note

In DTR protocol all transfer phases (including opcode) take DDR edge mode independently on the command under execution. DTR protocol is to be enabled by OSPI_CONFIG_REG[24] ENABLE_DTR_PROTOCOL_FLD bit. It has higher priority than DDR Mode enable bit from OSPI_DEV_INSTR_RD_CONFIG_REG[10] DDR_EN_FLD.

12.3.2.4.15 OSPI Data Integrity

The CRC aware SPI transfer can be performed when both controller and device are configured to work in the Octal DDR Protocol.

For write transactions (the controller transmits data throughout all transfer), the controller is responsible for sending address CRC byte (XOR of all address bytes) following address bytes and TX data CRC byte (XOR of all data bytes to write) following data chunk with size as defined in OSPI_MODE_BIT_CONFIG_REG[10-8] CHUNK_SIZE_FLD bit field. All CRC data are being calculated and sent automatically by the controller and the external device is responsible for reacting accordingly on any possible interpolation on the Flash interface. For read transactions, the controller is also responsible for sending address CRC byte (like for write) and for getting and progressing RX data CRC byte returning by the Flash Device after each chunk with size as defined in OSPI_MODE_BIT_CONFIG_REG[10-8] CHUNK_SIZE_FLD bit field. At the time when the Flash Device is returning data back to the controller, the controller dynamically calculates checksum byte by byte. Once the chunk is completed, CRC returned from Flash Device should fit to dynamically calculated CRC by the controller. In case of any deviation, controller reports CRC error to the system by corresponding interrupt (CRC error interrupt). The controller also provides the last captured CRC data in RX data chunk (defined in OSPI_MODE_BIT_CONFIG_REG[31-24] RX_CRC_DATA_LOW_FLD and OSPI_MODE_BIT_CONFIG_REG[23-16] RX_CRC_DATA_UP_FLD bit fields) to give the software driver the opportunity to further detecting any data corruption on system interfaces. The CRC data valid interrupt informs the system about the accessibility of the new RX CRC data in the registers. Once the system gets the full data word, it can calculate CRC by itself. At the time it collects all data words in chunk and then gets the CRC data valid interrupt, it can compare these data and react accordingly.

Some devices also have embedded ECC mechanism allowing them to report data abnormal conditions on their ECC Correction Signal output. At the time this output turns low, the device expect the OSPI controller to read status register of the device in order to get more details about the source of detected abnormal situation. The OSPI controller investigates ECC status on its ECC_FAIL input and generates an interrupt when detecting this signal being low.

12.3.2.4.16 OSPI PHY Module

OSPI module fully integrates PHY module dedicated to more flexible and power efficient transfers.

The PHY module communicates with the OSPI Flash controller via the aforementioned PHY Interface and handles data transfer on low-level stage of design hierarchy. However, when the OSPI_RCLK is configured to be equal to the SPI clock instead of alternative approach using clock divider, there is just one OSPI_RCLK cycle (not 4 or more) within single SPI period or half period for DDR Mode (SPI Control Module works on reference clock). Given that OSPI_RCLK is the input clock for RX FIFO and the output one for TX FIFO, the PHY solution incurs more restrictive requirement for value of system clock in order to synchronize data without SPI transfer interruption. For example, when the controller operates in DDR 1× octal Mode, 2 bytes of data (equivalent to one RX FIFO location) is gathered within just single OSPI_RCLK cycle. The controller cannot predict next data access while operating in the Direct Mode (meaning its size or whether it is sequential to the previous one or not). As a result, if the OSPI_HCLK is not significantly greater than OSPI_RCLK, the SPI transfer has to be suspended until the Flash Command Generator forwards new data to TX FIFO.

An optional PHY Pipeline Mode is implemented to avoid the necessity of stable clocking of the system clock for the Direct Mode when the PHY mode is enabled and to keep maximum performance while ensuring correct operation of the OSPI controller with the PHY using low frequencies from all its domains. This mode is a trade-off between large software overhead when operating in the Indirect Mode and the described limitations present in the Direct Mode. For more information about PHY Pipeline Mode, see Section 12.3.2.4.16.1 , *PHY Pipeline Mode*.

When DDR 2× Mode is granted based on configuration – SPI transfer is automatically performed using the PHY module even if the OSPI_CONFIG_REG[3] PHY_MODE_ENABLE_FLD is de-asserted. SDR 2× commands are handled with PHY module paths being bypassed. Nevertheless, dividers of 2, 4 or 6 for DDR and divider of 2 for SDR should not be configured based on controller requirements and these configurations are perceived as a software error.

The following steps are an example of software algorithm of adapting the OSPI controller with the PHY module incorporated to work in octal 1× clock DDR Protocol. Note that all necessary configuration steps described in Section 12.3.2.5.2 , *Configuring the OSPI Controller for Optimal Use* shall be completed before the algorithm.

1. Set PHY mode enable (OSPI_CONFIG_REG[3] PHY_MODE_ENABLE_FLD bit) and DDR protocol (OSPI_CONFIG_REG[24] ENABLE_DTR_PROTOCOL_FLD bit). It is assumed that device is configured to work in DDR Protocol.
2. Before setting the DLL parameters, software calibration could be needed.
   OSPI_PHY_MASTER_CONTROL_REG[23] PHY_MASTER_BYPASS_MODE_FLD bit controls the bypass mode of the controller and target DLLs. If this bit is set, the DLL bypass mode is enabled. This mode is intended to be used only for debug. When set to 0, a Controller operational mode is selected, when set to 1 the Bypass mode is selected.
   DLL works in normal mode of operation where the target delay line settings are used as fractional delay of the controller delay line encoder reading of the number of delays in one cycle.
   Controller DLL is disabled with only 1 delay element in its delay line. The target delay lines decode delays in absolute delay elements rather than as fractional delays.
   - DLL Bypass Mode (follow only if operating in this mode):
     - Depending on frequency of reference clock, calculate how many delay elements should be used to shift this clock by 25% of its period (best case for DDR transfers from setup/hold timings standpoint). Note that delay could be slightly different in a real design. TX Delay is configured in OSPI_PHY_CONFIGURATION_REG[22-16] PHY_CONFIG_TX_DLL_DELAY_FLD bit field.
     - Re-synchronize DLLs by asserting OSPI_PHY_CONFIGURATION_REG[31] PHY_CONFIG_RESYNC_FLD bit (If this bit is already set by previous re-synchronization, toggle sequence from "0" to "1" must be generated in order to trigger re-synchronization DLL logic) and set PHY bypass mode enable through OSPI_PHY_MASTER_CONTROL_REG[23] PHY_MASTER_BYPASS_MODE_FLD bit.
   - DLL Controller Mode (follow only if operating in this mode):
     - Drive DLL reset bit OSPI_PHY_CONFIGURATION_REG[30] PHY_CONFIG_RESET_FLD into low.
     - Calculate initial delay value for the Controller DLL according to the OSPI_PHY_MASTER_CONTROL_REG[6-0] PHY_MASTER_INITIAL_DELAY_FLD bit field.
     - Depending on frequency of reference clock, calculate how many delay elements should be used to shift this clock by 25% of its period (best case for DDR transfers from setup/hold timings standpoint). Note that delay could be slightly different in a real design. TX Delay is configured in OSPI_PHY_CONFIGURATION_REG[22-16] PHY_CONFIG_TX_DLL_DELAY_FLD bit field.

  - Re-synchronize DLLs by asserting OSPI_PHY_CONFIGURATION_REG[31] PHY_CONFIG_RESYNC_FLD (If this bit is already set by previous re-synchronization, toggle sequence from "0" to "1" must be generated in order to trigger re-synchronization DLL logic) and set DLL reset bit back to high (since both bits are within the same register, it is acceptable to set both bits simultaneously).
  - Poll OSPI_DLL_OBSERVABLE_LOWER_REG[15] DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD bit. When set – lock is done.
  - Re-synchronize Target DLLs by asserting OSPI_PHY_CONFIGURATION_REG[31] PHY_CONFIG_RESYNC_FLD bit (If this bit is already set by previous re-synchronization, toggle sequence from "0" to "1" must be generated in order to trigger re-synchronization DLL logic) and set TX DLL Delay (OSPI_PHY_CONFIGURATION_REG[22-16] PHY_CONFIG_TX_DLL_DELAY_FLD) and RX DLL Delay (OSPI_PHY_CONFIGURATION_REG[6-0] PHY_CONFIG_RX_DLL_DELAY_FLD) fields which are equivalent to percentage clock offsets now. It is recommended to wait for the new configuration being propagated by 20 reference clock cycles before triggering the next SPI transfer.
- Consider Read Data from location where its value is predictable. This step can be performed in different ways, depending on the device. Parameter Page, ID, Status, Data from OTP region or Data from location of Flash Array the value of which is known can act as the pattern.
- Trigger Read request chosen from above options.
- Check correctness of data and store that information:
  - Increment value of RX clock delay – it is configurable in the OSPI_PHY_CONFIGURATION_REG[6-0] PHY_CONFIG_RX_DLL_DELAY_FLD bit field.
  - Re-synchronize DLLs.
  - Trigger valid Read request.
  - Check correctness of data and store information.
  - If range boundary of RX clock delay is achieved, go to step 3. Otherwise go back to step "Increment value of RX clock delay".

3. Set RX clock delay value for one from the middle of valid range based on information in storage.
4. Re-synchronize DLLs.
5. Set OSPI_DEV_INSTR_RD_CONFIG_REG for Octal Read DDR Configuration (each transfer phase should be configured to work in Octal mode, Number of Dummy cycles should be set as specified in the documentation of the device or more when because of additional read paths delays of actual systems data is predicted to be flopped by PHY module with delay excesses actual cycle of SPI clock generated by the controller).
6. Enable Pipeline mode in the OSPI_CONFIG_REG[25] PIPELINE_PHY_FLD bit.
7. Perform Sequential Read of Data consistent with conditions indicated within Section 12.3.2.4.16.1 , *PHY Pipeline Mode*.
8. After de-asserting the data target select signal by software – poll OSPI_CONFIG_REG[31] IDLE_FLD bit.
9. When it is asserted to high – next transfer request can be triggered.

12.3.2.4.16.1 PHY Pipeline Mode

This mode is used for Direct Read Mode of operation. If any other operations are intended to be executed, it is recommended to disable PHY Pipeline Mode and re-enable for subsequent Direct Reads in PHY mode. Since there is comprehensive software mechanism controlling Read data transfers in Indirect Mode, pipeline of data interface accesses is not effective for this mode. Enable PHY Pipeline feature when at least four 4-byte-sized data words are predicted to be read in sequentially. The Flash Command Generator pipelines and puts them into TX FIFO which causes CS to remain active because low level SPI protocol controller controls TX FIFO fill level. In order to correctly trigger Direct Read in Pipeline Mode TX FIFO must be empty. Therefore first polling of OSPI_CONFIG_REG[31] IDLE_FLD bit needs to be done. The sequential data transfer will be interrupted when the data target select signal of the data interface is asserted to low. This information is also detected by Data Target Module which informs the Flash Command Generator that the next access is invalid and a TX FIFO locations can be flushed transparently for the system.

In PHY Pipeline Mode it is recommended for Data Controller not to introduce wait states in between consecutive occurrences of the data interface signal that indicates transfer has finished. It will ensure regular transfer rate on data side. Introducing wait states gradually slows data transfer rate down and may finally cause SPI transfer interruption because of TX FIFO data starvation. The system, however, may need to introduce some number of wait states after completion of sequential transfer (composed of 4-byte sized data words) for progressing the data. The dedicated buffer is implemented in Data Target Controller which collects all incoming data during wait states injection. In order to keep SPI transfer uninterrupted, number of wait states should be as little as possible. The higher the OSPI_HCLK/ OSPI_RCLK ratio the more wait states can be introduced without SPI transfer interruption. In case the system is able to launch a new transfer before wait states overflow, buffered data transfer to the host will continue. It compensates slowed down transfer by introducing wait states. In case the system is not able to launch a new transfer before wait states overflow, next incoming transfer is considered non-sequential and is executed after all pipelined data is flushed.

This mode can be enabled when following conditions are met:
- OSPI_HCLK > OSPI_RCLK (Comparing the slow data clock with the fast reference one makes Pipeline Mode ineffective – Suspend of SPI Transfer would be possible. Consequently, this condition has to be met to operate in this mode.)
- Only 4-byte sized Data Words are permitted (This ensures more data clock cycles for synchronization of FIFOs between consecutive pulses of the signal indicating transfer has finished.)
- The transfer with introduced wait states or non-sequential transfers can only be triggered in between at least four 4-byte sized Data Bursts sequential accesses (16 Bytes) to be sure that Data Controller can trust buffered incoming data during wait states injection.
- Do not use Pipeline Mode along with Continuous Mode (XIP). Benefit of XIP is limited for bulk data transfers intended to execute in Pipeline Mode.

12.3.2.4.16.2 Read Data Capturing by the PHY Module

Read Data Capturing by the PHY module is useful, as the user is not responsible for the design dedicated DLL being compatible with the Octal-SPI Flash Controller. Another benefit is an option to adjust both SPI clock and sampling clock in a very wide range to fit them into individual requirements of any system. If loopback clock (OSPI_RD_DATA_CAPTURE_REG[0] BYPASS_FLD) and PHY mode (OSPI_CONFIG_REG[3] PHY_MODE_ENABLE_FLD) are both enabled, the loopback clock is driven into RX DLL instead of gated reference clock. Because of the architecture of DLL, loopback clock needs to be provided in SPI Mode 0. If DQS (OSPI_RD_DATA_CAPTURE_REG[8] DQS_ENABLE_FLD) and PHY mode (OSPI_CONFIG_REG[3] PHY_MODE_ENABLE_FLD) are both enabled, the DQS is driven into RX DLL instead of gated reference clock.

12.3.2.5 OSPI Programming Guide

12.3.2.5.1 Configuring the OSPI Controller for Use After Reset

The OSPI controller has been designed to wake up in a state that is suitable for performing basic reads and writes using the direct access controller. The BASIC read (opcode 0x03) and BASIC write (opcode 0x02) instructions are operations supported by all target devices. The controller also wakes up with a baud rate divider setting of divide-by-32. Assuming the reference clock is operating at 400 MHz after reset, then this means the effective SPI clock is just 12.5 MHz. This should be slow enough to meet all timing requirements of all target devices without any further device programming.

If the target device does not use 3 address bytes, the device size configuration register must be modified to the appropriate size.

If software plans to write to the device, and the number of bytes per device page is not equal to 256, then the device size configuration register must also be modified.

While not a requirement, it is prudent for software to enable the write protect feature prior to enabling the OSPI controller. This will block any data writes from taking effect. To do so, the protection registers (OSPI_LOWER_WR_PROT_REG, OSPI_UPPER_WR_PROT_REG and OSPI_WR_PROT_CTRL_REG) should be setup and the number of bytes per device block in the device size configuration register should also be setup.

After Power-on Reset (POR), software can read from and write to the FLASH device (albeit slowly). Enabling/Disabling the controller and DAC is achieved with just one write to corresponding fields of the OSPI_CONFIG_REG register. User shall take note to maintain the default values of the baud rate divisor and the default state of SEL_CLK_POL_FLD/ SEL_CLK_PHASE_FLD bits of this register. A write data value of 0x00780081 is recommended.

12.3.2.5.2 Configuring the OSPI Controller for Optimal Use

Note

When using the OSPI Controller, the opcodes in OSPI_DEV_INSTR_RD_CONFIG_REG[7-0] RD_OPCODE_NON_XIP_FLD, OSPI_DEV_INSTR_WR_CONFIG_REG[7-0] WR_OPCODE_FLD and OSPI_WRITE_COMPLETION_CTRL_REG[7-0] OPCODE_FLD bit fields shall not match the opcode in the OSPI_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD bit field.

For high speed transfers PHY mode can be enabled and for optimal configuration PHY Pipeline mode is recommended. For more information, see Section 12.3.2.4.16.1 , *PHY Pipeline Mode*.

To access the flash optimally, software must configure the controller accurately:

1. Wait until any pending STIG or INDAC operation has completed or poll OSPI_CONFIG_REG[31] IDLE_FLD bit.
2. Disable the DAC through OSPI_CONFIG_REG[7] ENB_DIR_ACC_CTLR_FLD bit. It is permitted, but not necessary to also disable the OSPI controller completely via OSPI_CONFIG_REG[0] ENB_SPI_FLD bit.
3. Update the OSPI_DEV_INSTR_RD_CONFIG_REG and OSPI_DEV_INSTR_WR_CONFIG_REG registers for the instruction type you wish to use for indirect and direct writes and reads.
4. Update the OSPI_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field if mode bits have been enabled in the OSPI_DEV_INSTR_RD_CONFIG_REG[20] MODE_BIT_ENABLE_FLD bit.
5. Update the OSPI_DEV_SIZE_CONFIG_REG if the contents are incorrect. Note parts or all of this register may have been updated after initialization. The number of address bytes is a key configuration setting required for performing reads and writes. The number of bytes per page is required for performing any write. The number of bytes per device block is only required if the write protect feature is used. If the default values are correct for the target device, or if some of the values (not including the number address bytes) were incorrect but device writes were not permitted.
6. Update the OSPI_DEV_DELAY_REG. This register allows the user to tweak how the chip select is driven after each FLASH access. This is required as each device may have different timing requirements. As

the serial clock frequency is increased, these timing requirements become more important. Note the numbers programmed in this register are based on the period of reference clock. Example: A device needs 50ns minimum time before CS can be re-asserted after it has been de-asserted. By default, the controller will only provide a minimum of 1 SCLK period. When the device is operating at 100 MHz, the SCLK period is only 10ns, so 40ns extra is required. Since the register defines the number of reference clock cycles to add, and reference clock is running at 400 MHz (2.5ns period), then the user should program a value of at least 16 to the OSPI_DEV_DELAY_REG[31-24] D_NSS_FLD. This delay can be extended during auto-polling phase. There is possibility to define the polling repetition delay in the OSPI_WRITE_COMPLETION_CTRL_REG[31-24] POLL_REP_DELAY_FLD bit field.

7. Update the OSPI_REMAP_ADDR_REG register, if required. Affects DAC path only.
8. Setup and enable write protection registers (OSPI_LOWER_WR_PROT_REG, OSPI_UPPER_WR_PROT_REG and OSPI_WR_PROT_CTRL_REG) if they are required and if they have not already been setup from post initialization.
9. Enable required interrupts via the OSPI_IRQ_MASK_REG register.
10. Setup the baud rate divisor in the OSPI_CONFIG_REG[22-19] MSTR_BAUD_DIV_FLD to define the required clock frequency of the target device.
11. Update the OSPI_RD_DATA_CAPTURE_REG register. This register will delay when the read data is captured and can help when the read data path from the device to the controller is long and the device clock frequency is high. An update to this register may not be necessary.
12. Enable the OSPI controller and the DAC via the OSPI_CONFIG_REG.

12.3.2.5.3 Using the Flash Command Control Register (STIG Operation)

The OSPI_FLASH_CMD_CTRL_REG register provides software means to access the FLASH device in a flexible and programmable manner. This is known as a STIG operation (Software Triggered Instruction Generator). The instruction opcode, number of address bytes (if any), the address itself, number of dummy cycles (if any), number of write data bytes (if any), the write data itself and the number of read data bytes (if any) can be programmed. Once these have been programmed, software can trigger the command via OSPI_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD bit and wait for its acceptance by polling OSPI_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit. When CMD_EXEC_STATUS_FLD bit turns de-asserted, another STIG can be triggered. This method of accessing the FLASH is the typical mechanism that software would use to access the FLASH device's registers, as well as for performing ERASE operations. It can also be used to access the FLASH array itself, although the maximum of 8 data bytes may be read or written at any one time, defined in the Flash Command Write and Read Data registers (OSPI_FLASH_RD_DATA_LOWER_REG, OSPI_FLASH_RD_DATA_UPPER_REG, OSPI_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_WR_DATA_UPPER_REG). This number of bytes can be extended for Read Data commands using additional STIG Memory Bank controlled by OSPI_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD and OSPI_FLASH_COMMAND_CTRL_MEM_REG.

Commands issued using this interface have a higher priority than all other READ accesses coming from data interface, and will therefore interrupt any READ commands being requested by the indirect or direct controllers.

12.3.2.5.4 Using SPI Legacy Mode

SPI legacy mode allows software to access the internal TX-FIFO and RX-FIFO directly, thus bypassing the direct, indirect and STIG controllers.

Legacy mode allows the user to issue any FLASH instruction to the device, but does place a heavy software overhead in order to manage the fill levels of the FIFO's effectively. This is because the legacy SPI core is bi-directional in nature, with data continuously being transferred in either direction while the chip select is enabled. Even if the driver only wishes to read data from the FLASH device, dummy data must be written out to ensure the chip select stays active, and vice versa for write transactions.

Since the TX-FIFO and RX-FIFO are of limited depth, software has a responsibility to maintain the FIFO levels to ensure the TX-FIFO does not become exhausted during the instruction execution and the RX-FIFO doesn't overflow. This can place a lot of overhead on software. Interrupts are provided to indicate when the fill levels pass programmable watermarks, which are themselves programmable registers OSPI_TX_THRESH_REG and OSPI_RX_THRESH_REG.

The limited depth may impose the limitation over execution of some specific SPI commands in legacy mode. Note that the controller interprets all transmitted bytes as valid. For example, if the Flash Device was configured to return valid data after many dummy cycles, the TX FIFO could become full before the controller sends all of dummy data.

12.3.2.5.5 Entering XIP Mode from POR

XIP is a mode that can be entered in a non-volatile way if the device has XIP enabled as a non-volatile configuration setting. Software will not be able to discover the state of XIP from POR via FLASH status register reads as the only operation a FLASH device will recognize when XIP mode is enabled is an XIP read operation.

If it is already known that the device will enter XIP from POR, then the OSPI_MODE_BIT_CONFIG_REG[7-0] MODE_FLD and OSPI_CONFIG_REG[18] ENTER_XIP_MODE_IMM_FLD bits should be set in initial boot.

If it is not already known that the device will enter XIP from POR, and XIP from POR may be supported by the attached FLASH device, then software can attempt to exit XIP mode by issuing an XIP exit command using a STIG command (via the OSPI_FLASH_CMD_CTRL_REG register). To do this, software must be aware of the mode bit requirements of that device, as XIP entry and exit changes per device.

12.3.2.5.6 Entering XIP Mode Otherwise

XIP mode is supported in most FLASH devices. Some of them use signature bits that are sent to the device immediately following the address bytes, other use signature bits and also require a FLASH device configuration register write to enable XIP. For the FLASH devices that must be compliant to the OSPI controller, the following steps can be taken by software to enter XIP mode:

1. Disable the DAC and INDAC (OSPI_CONFIG_REG[7] ENB_DIR_ACC_CTLR_FLD) to ensure no new data read accesses will be sent to the FLASH device.
2. (Optional) Configure the OSPI_FLASH_CMD_CTRL_REG to issue a VCR write to FLASH memory, because XIP mode must first be enabled for some devices.
3. Configure the XIP mode bits in the OSPI_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field.
4. Enable the local controllers XIP mode by setting OSPI_CONFIG_REG[17] ENTER_XIP_MODE_FLD bit.
5. Re-enable the DAC and, if required, the INDAC.

12.3.2.5.7 Exiting XIP Mode

To exit XIP mode, software should first disable the DAC and INDAC to ensure no new data read accesses will be sent to the FLASH device. It should then set mode bits to other than the established in the corresponding Flash Device specifications. These are dependent on the FLASH device and manufacturer. Software should then reset OSPI_CONFIG_REG[17] ENTER_XIP_MODE_FLD.

Note the FLASH device must see a READ instruction before it can disable its internal XIP mode state, so this means XIP mode will internally stay active until the next READ instruction is serviced. User must take care to ensure that XIP mode is disabled before the end of any READ sequence.

12.3.3 General-Purpose Memory Controller (GPMC)

This section describes the General-Purpose Memory Controller (GPMC) for the device.

12.3.3.1 GPMC Overview

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

Table 12-240 shows the GPMC module allocation within device domains.

Table 12-252. GPMC Module Allocation within Device Domains

Module Instance	Domain		
	WKUP	MCU	MAIN
GPMC0	-	-	✓

Figure 12-160 shows the GPMC0 module overview.

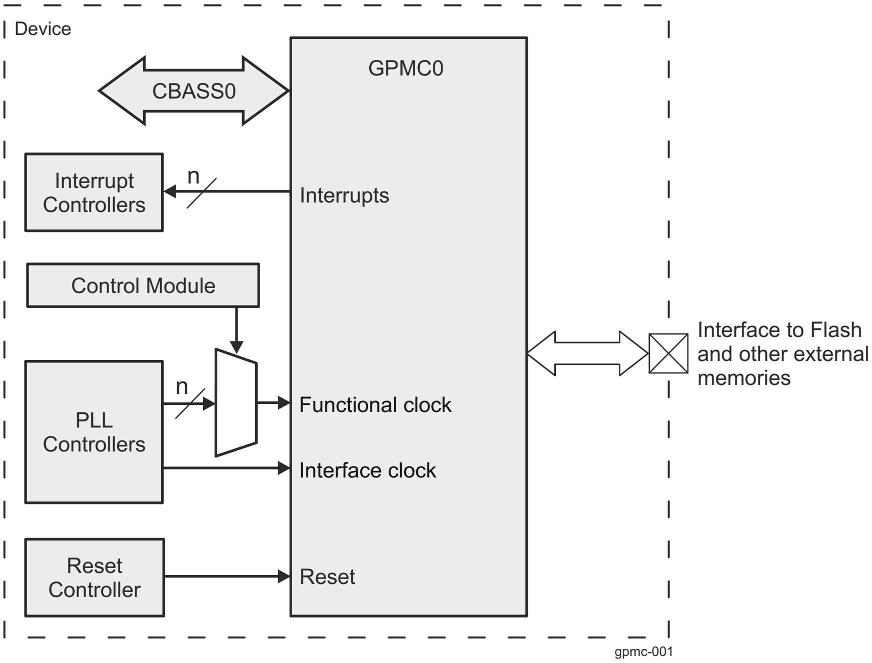

Figure 12-160. GPMC0 Overview

12.3.3.1.1 GPMC Features

The main features of the GPMC are:

- 8-, 16- or 32-bit-wide data path to external memory device
- Supports up to 4 chip select regions of programmable size and programmable base addresses in a total address space of 1GB
- Supports on-the-fly error code detection using the Bose-ChaudhurI-Hocquenghem (BCH) (t = 4, 8, or 16) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)
- Fully pipelined operation for optimal memory bandwidth usage
- The clock to the external memory is provided from GPMC_FCLK divided by 1, 2, 3, or 4
- Supports programmable autoclock gating when no access is detected

- Independent and programmable control signal timing parameters for setup and hold time on a per-chip basis. Parameters are set according to the memory device timing parameters with a timing granularity of one GPMC_FCLK clock cycle.
- Flexible internal access time control (wait state) and flexible handshake mode using external WAIT pin monitoring
- Support bus keeping
- Support bus turnaround
- Prefetch and write-posting engine associated with DMA controller at system level to achieve full performance from the NAND device with minimum effect on NOR/SRAM concurrent access
- 32-bit interconnect target interface which supports non-wrapping and wrapping burst of up to 16x32 bits.

The GPMC supports the following various access types:

- Asynchronous read/write access
- Asynchronous read page access (4-8-16-32 Word16, 4-8-16 Word32)
- Synchronous read/write access
- Synchronous read/write burst access without wrap capability (4-8-16-32 Word16, 4-8-16 Word32)
- Synchronous read/write burst access with wrap capability (4-8-16-32 Word16, 4-8-16 Word32)
- Address-data-multiplexed (AD) access
- Address-address-data (AAD) multiplexed access
- Little-endian access only

The GPMC can communicate with a wide range of external devices:

- External asynchronous or synchronous 8-bit wide memory or device (non burst device)
- External asynchronous or synchronous 16-bit wide memory or device
- External asynchronous or synchronous 32-bit wide memory or device
- External 16-bit non-multiplexed NOR flash device
- External 16- and 32-bit address and data multiplexed NOR Flash device
- External 8-bit and 16-bit NAND flash device
- External 16-bit and 32-bit pseudo-SRAM (pSRAM) device

Note

Page mode is available only in non-multiplexed mode.

Note

Above features of GPMC are generic GPMC IP features. GPMC features supported in particular SoC depends on the number of GPMC Address,data lines available in that SoC. For details regarding GPMC Address/Data lines, see device specific datasheet.

12.3.3.1.2 GPMC Not Supported Features

The following features are not supported on this family of devices:

- Asynchronous page write mode is not supported.
- Multiple write access in asynchronous mode is not supported.
- Multiple read access in asynchronous mode is not supported in address/data-multiplexed and AAD-multiplexed modes.

12.3.3.2 GPMC Environment

The GPMC0 module is hereinafter referred to as GPMC.

This section describes the GPMC0 external connections (environment).

12.3.3.2.1 GPMC Modes

This section shows four GPMC0 external connection options:

- Figure 12-161 shows a connection between the GPMC0 and a 32-bit synchronous address/data-multiplexed external memory device.
- Figure 12-162 shows a connection between the GPMC0 and a 16-bit synchronous address/data-multiplexed (or AAD-multiplexed but this protocol uses fewer address pins) external memory device.
- Figure 12-163 shows a connection between the GPMC0 and a 16-bit synchronous non-multiplexed external memory device.
- Figure 12-164 shows a connection between the GPMC0 and an 8-bit synchronous non-multiplexed external memory device.
- Figure 12-165 shows a connection between the GPMC0 and an 8-bit NAND device.

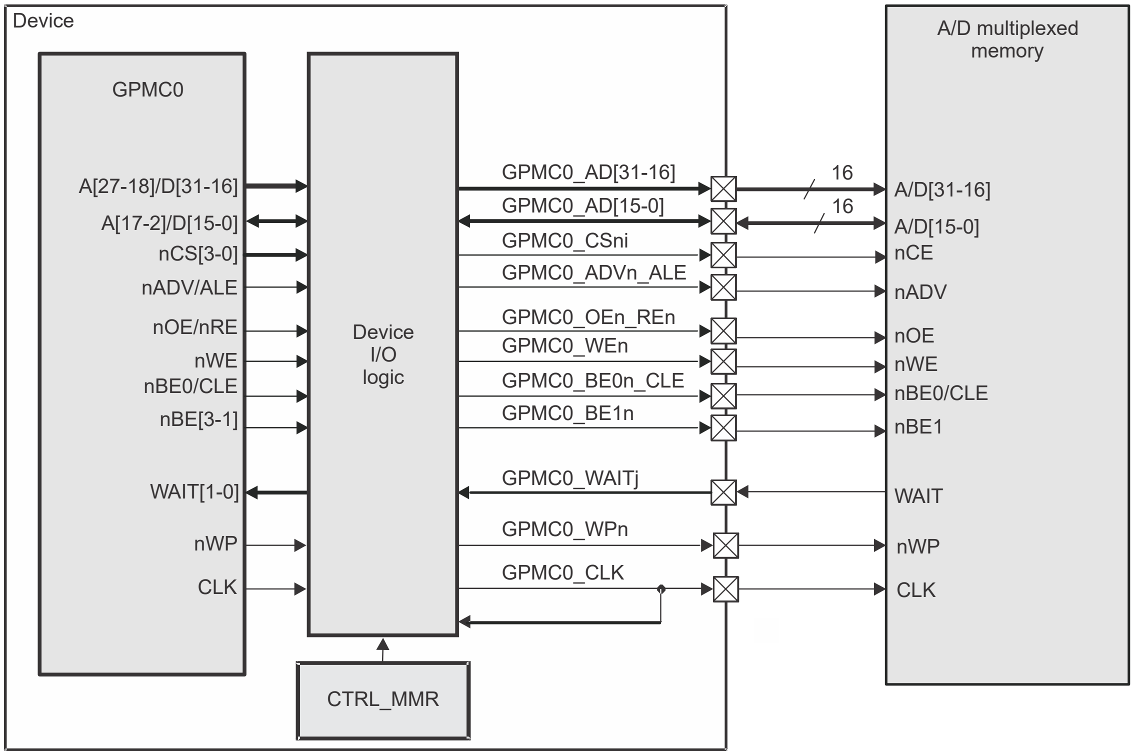

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-161. GPMC to 32-Bit Address/Data-Multiplexed Memory

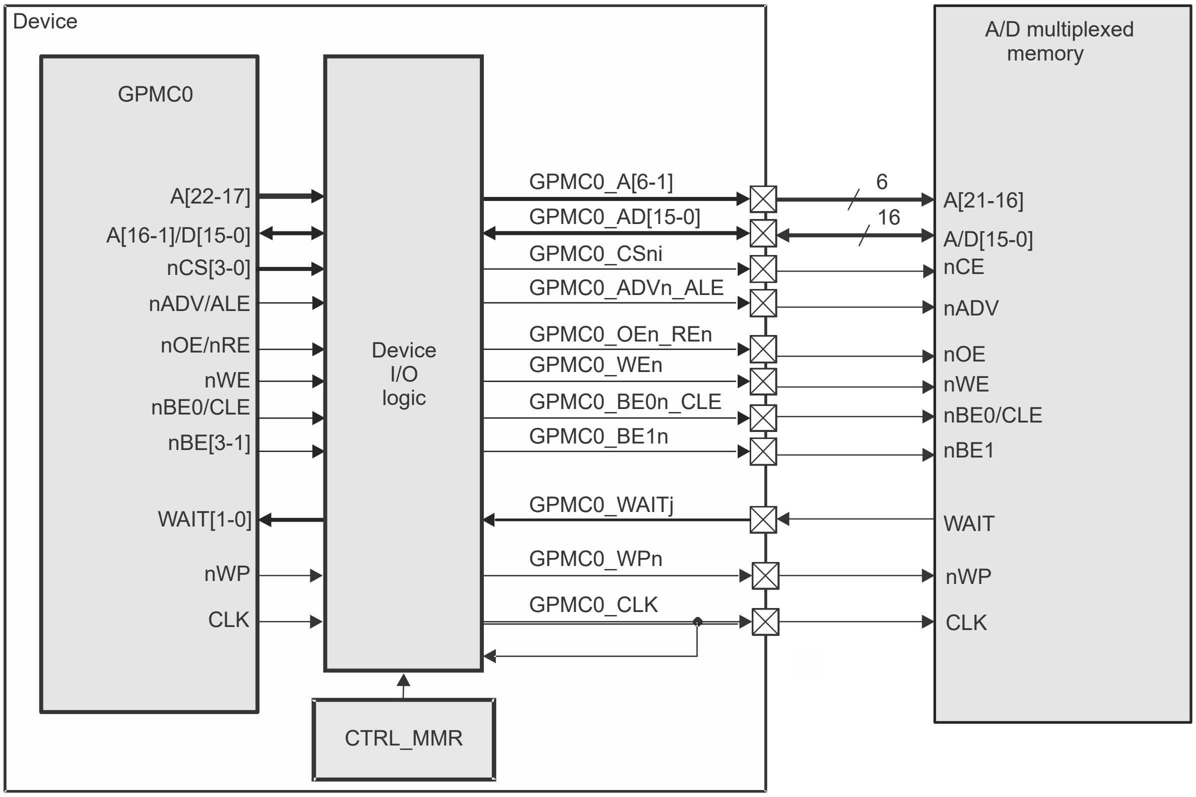

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-162. GPMC to 16-Bit Address/Data-Multiplexed Memory

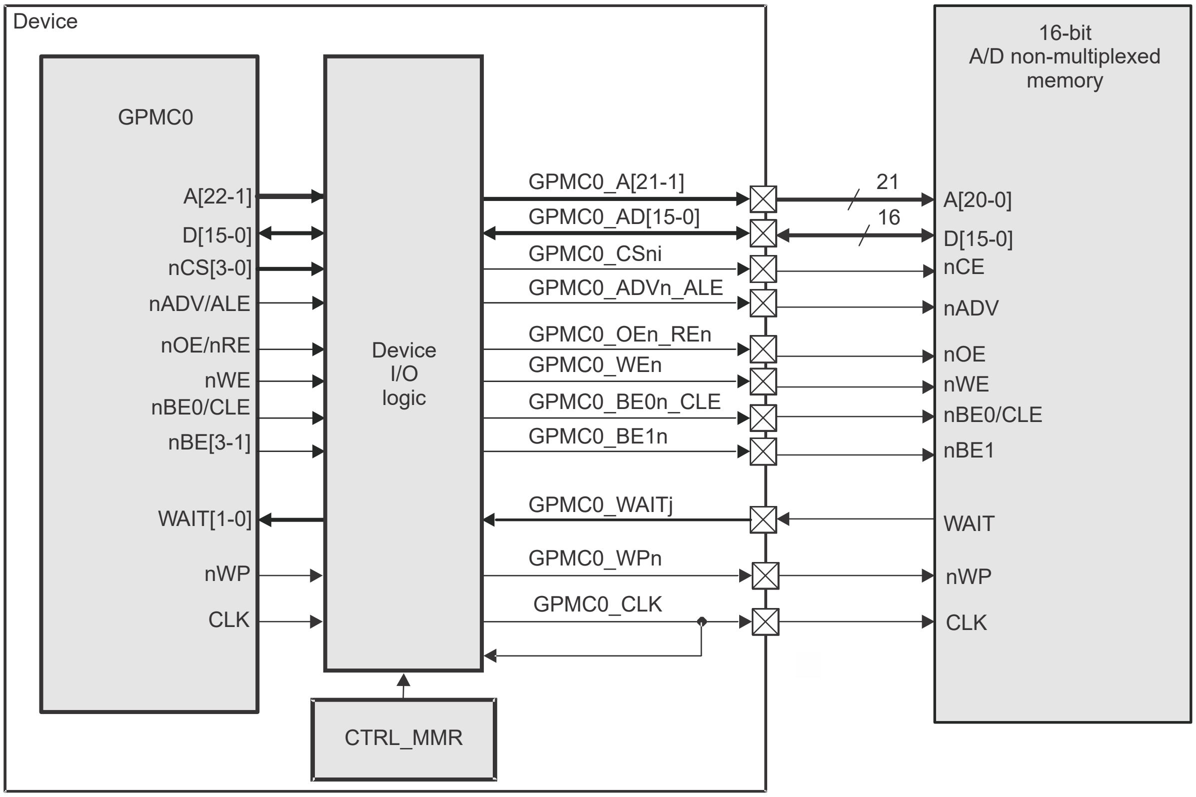

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-163. GPMC to 16-Bit Non-Multiplexed Memory

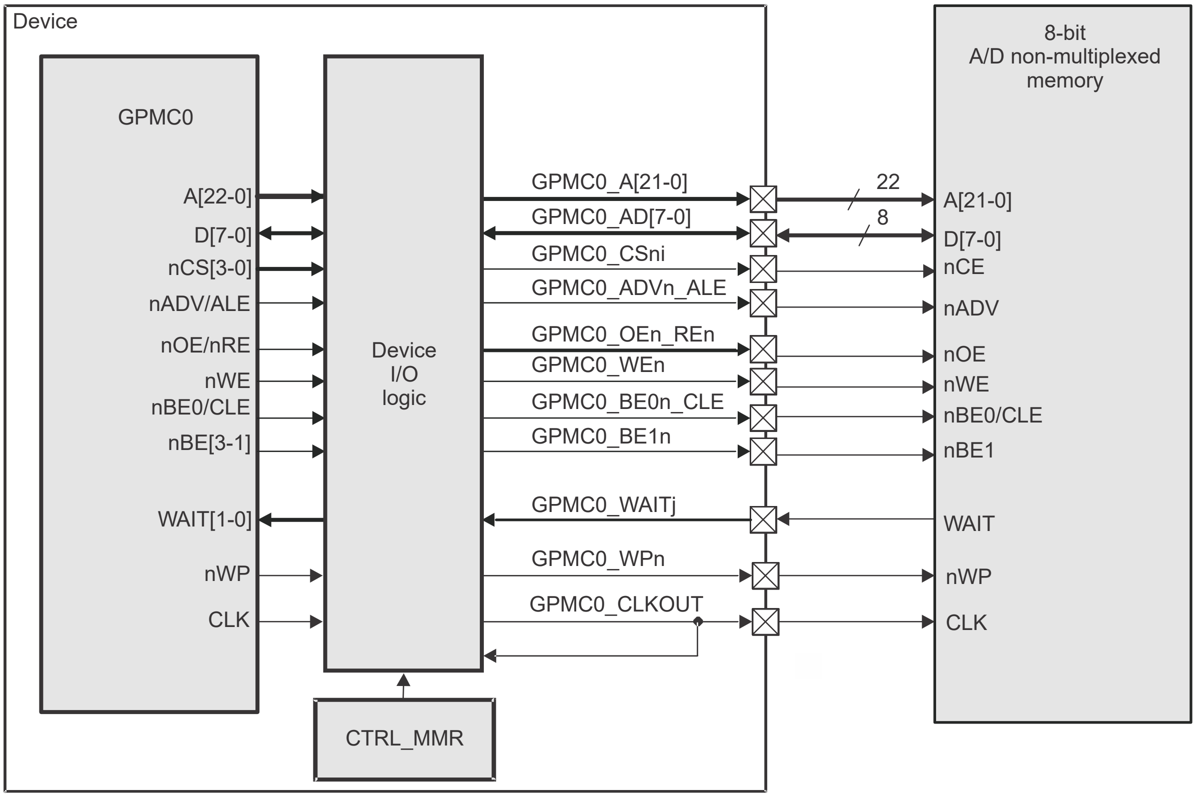

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-164. GPMC to 8-Bit Non-Multiplexed Memory

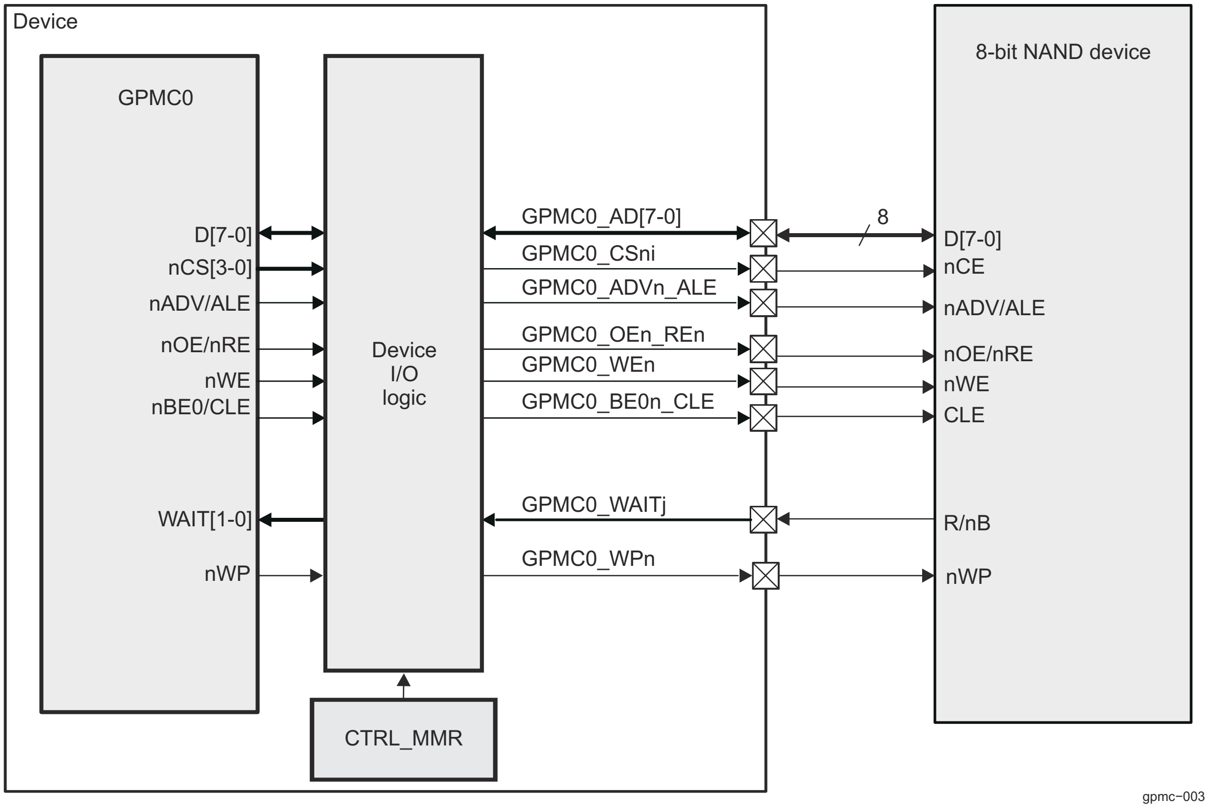

Note

i = 0 to 3

Note

j = 0 to 1

Figure 12-165. GPMC to 8-Bit NAND Device

12.3.3.2.2 GPMC I/O Signals

Table 12-241 lists the GPMC subsystem input/output (I/O) pins.

Table 12-253. GPMC I/O Signals (Controller Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
			GPMC0	
A[21-0]	GPMC0_A[21-0]	O	22-bit output address bus	-
A[27-2]/D[31-0]	GPMC0_AD[15-0]	I/O	Multiplexed address/data	-
nCS[3-0]	GPMC0_CSn[3-0]	O	Chip-selects (active low)	-
CLK CLKLB	GPMC0_CLK	O	Clock generated for the external memory or device. For more information, see *GPMC0 Integration*.	-
N/A	GPMC0_FCLK_MUX	O	Free running clock. GPMC functional clock (GPMC0_FCLK) propagated on a device pad. For more information on the GPMC0_FCLK_MUX integration, see *GPMC0 Integration*.	-
nADV/ALE	GPMC0_ADVn_ALE	O	Address valid (active low). Also used as address latch enable (active high) for NAND protocol memories.	-
nOE/nRE	GPMC0_OEn_REn	O	Output enable (active low). Also used as read enable (active low) for NAND protocol memories.	-

Table 12-253. GPMC I/O Signals (Controller Mode) (continued)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
nWE	GPMC0_WEn	O	Write enable (active low)	-
nBE0/CLE	GPMC0_BE0n_CLE	O	Lower-byte enable (active low). Also used as command latch enable for NAND protocol memories.	-
nBE1	GPMC0_BE1n	O	Upper-byte enable (active low)	-
WAIT[1-0]	GPMC0_WAIT[1-0]	I	External wait signal for NOR and NAND protocol memories. Can be mapped on any of the chip-selects.	-
nWP	GPMC0_WPn	O	Write protect (active low)	-
DIR	GPMC0_DIR	O	This signal can be used to control an external buffer direction. Also controls the signal direction of D[15-0]. Low during transmit (for write access: data OUT from GPMC0 to memory). High during receive (for read access: data IN from memory to GPMC0).	-

(1) I = Input; O = Output; I/O - Bidirectional

(2) HiZ = High Impedance

Note

For GPMC output clock signal (CLK) to work properly, the RXACTIVE bit of the appropriate CTRLMMR_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

Table 12-242 shows the use of address and data GPMC pins based on the type of external device.

Table 12-254. GPMC Pin Multiplexing Options

GPMC Pin	Multiplexed Address Data 32-Bit Device	Multiplexed Address Data 16-Bit Device	non-multiplexed Address Data 16-Bit Device (incomplete 28-bit address range)	non-multiplexed Address Data 8-Bit Device (incomplete 28-bit address range)	16-Bit NAND Device	8-Bit NAND Device
GPMC0_A[21]	Not used	Not used	A21	A21	Not used	Not used
GPMC0_A[20]	Not used	Not used	A20	A20	Not used	Not used
GPMC0_A[19]	Not used	Not used	A19	A19	Not used	Not used
GPMC0_A[18]	Not used	Not used	A18	A18	Not used	Not used
GPMC0_A[17]	Not used	Not used	A17	A17	Not used	Not used
GPMC0_A[16]	Not used	Not used	A16	A16	Not used	Not used
GPMC0_A[15]	Not used	Not used	A15	A15	Not used	Not used
GPMC0_A[14]	Not used	Not used	A14	A14	Not used	Not used
GPMC0_A[13]	Not used	Not used	A13	A13	Not used	Not used
GPMC0_A[12]	Not used	Not used	A12	A12	Not used	Not used
GPMC0_A[11]	Not used	Not used	A11	A11	Not used	Not used
GPMC0_A[10]	Not used	A26	A10	A10	Not used	Not used
GPMC0_A[9]	Not used	A25	A9	A9	Not used	Not used
GPMC0_A[8]	Not used	A24	A8	A8	Not used	Not used
GPMC0_A[7]	Not used	A23	A7	A7	Not used	Not used

Table 12-254. GPMC Pin Multiplexing Options (continued)

GPMC Pin	Multiplexed Address Data 32-Bit Device	Multiplexed Address Data 16-Bit Device	non-multiplexed Address Data 16-Bit Device (incomplete 28-bit address range)	non-multiplexed Address Data 8-Bit Device (incomplete 28-bit address range)	16-Bit NAND Device	8-Bit NAND Device
GPMC0_A[6]	Not used	A22	A6	A6	Not used	Not used
GPMC0_A[5]	Not used	A21	A5	A5	Not used	Not used
GPMC0_A[4]	Not used	A20	A4	A4	Not used	Not used
GPMC0_A[3]	Not used	A19	A3	A3	Not used	Not used
GPMC0_A[2]	Not used	A18	A2	A2	Not used	Not used
GPMC0_A[1] (2)	Not used	A17	A1 (2)	A1	Not used	Not used
GPMC0_A[0](1)	Not used	A0 - Not used	Not used	A0 (3)(4)	Not used	Not used
GPMC0_AD[31]	D31	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[30]	D30	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[29]	D29	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[28]	D28	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[27]	D27	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[26]	D26	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[25]	A27/D25	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[24]	A26/D24	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[23]	A25/D23	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[22]	A24/D22	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[21]	A23/D21	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[20]	A22/D20	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[19]	A21/D19	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[18]	A20/D18	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[17]	A19/D17	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[16]	A18/D16	Not used	Not used	Not used	Not used	Not used
GPMC0_AD[15]	A17/D15	A16/D15	D15	Not used	D15	Not used
GPMC0_AD[14]	A16/D14	A15/D14	D14	Not used	D14	Not used
GPMC0_AD[13]	A15/D13	A14/D13	D13	Not used	D13	Not used
GPMC0_AD[12]	A14/D12	A13/D12	D12	Not used	D12	Not used
GPMC0_AD[11]	A13/D11	A12/D11	D11	Not used	D11	Not used
GPMC0_AD[10]	A12/D10	A11/D10	D10	Not used	D10	Not used
GPMC0_AD[9]	A11/D9	A10/D9	D9	Not used	D9	Not used
GPMC0_AD[8]	A10/D8	A9/D8	D8	Not used	D8	Not used
GPMC0_AD[7]	A9/D7	A8/D7	D7	D7	D7	D7
GPMC0_AD[6]	A8/D6	A7/D6	D6	D6	D6	D6
GPMC0_AD[5]	A7/D5	A6/D5	D5	D5	D5	D5
GPMC0_AD[4]	A6/D4	A5/D4	D4	D4	D4	D4
GPMC0_AD[3]	A5/D3	A4/D3	D3	D3	D3	D3
GPMC0_AD[2]	A4/D2	A3/D2	D2	D2	D2	D2
GPMC0_AD[1]	A3/D1	A2/D1	D1	D1	D1	D1
GPMC0_AD[0]	A2/D0	A1/D0	D0	D0	D0	D0

(1) Used to effectively address 8-bit (only) non-multiplexed memories.

(2) GPMC0_A1 should be connected to the Least significant Address bit of the 16-bit non-multiplexed device. A1 in the 16-bit non multiplexed memory column refers to the LSB in the memory side (16-bit non multiplexed memory). Some flash vendors use A0 to represent the least significant bit of the memory.

(3) A0 here represents the LSB of 8-bit (only) non-multiplexed memories.

(4) For 16x/8x bit non-multiplexed memory device (both modes supported), some flash vendors use A(-1) to represent LSB of 8-bit mode and A0 to represent LSB in 16-bit mode. In this case GPMC0_A0 should be connected to A(-1) and GPMC_A1 should be connected to A0.

With all device types, the GPMC does not drive unnecessary address lines. They stay at their reset value of 0x0.

Address mapping supports address/data-multiplexed 16- or 32-bit-wide devices:

- The NOR flash memory controller still supports non-multiplexed address and data memory devices.
- Multiplexing mode can be selected through the GPMC_CONFIG1_i[9-8] MUXADDDATA bit field (where i = 0 to 3).

12.3.3.3 GPMC Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

12.3.3.3.1 GPMC Integration in MAIN Domain

A single GPMC module is integrated in the device MAIN domain - GPMC0. Figure 12-166 shows the GPMC0 integration.

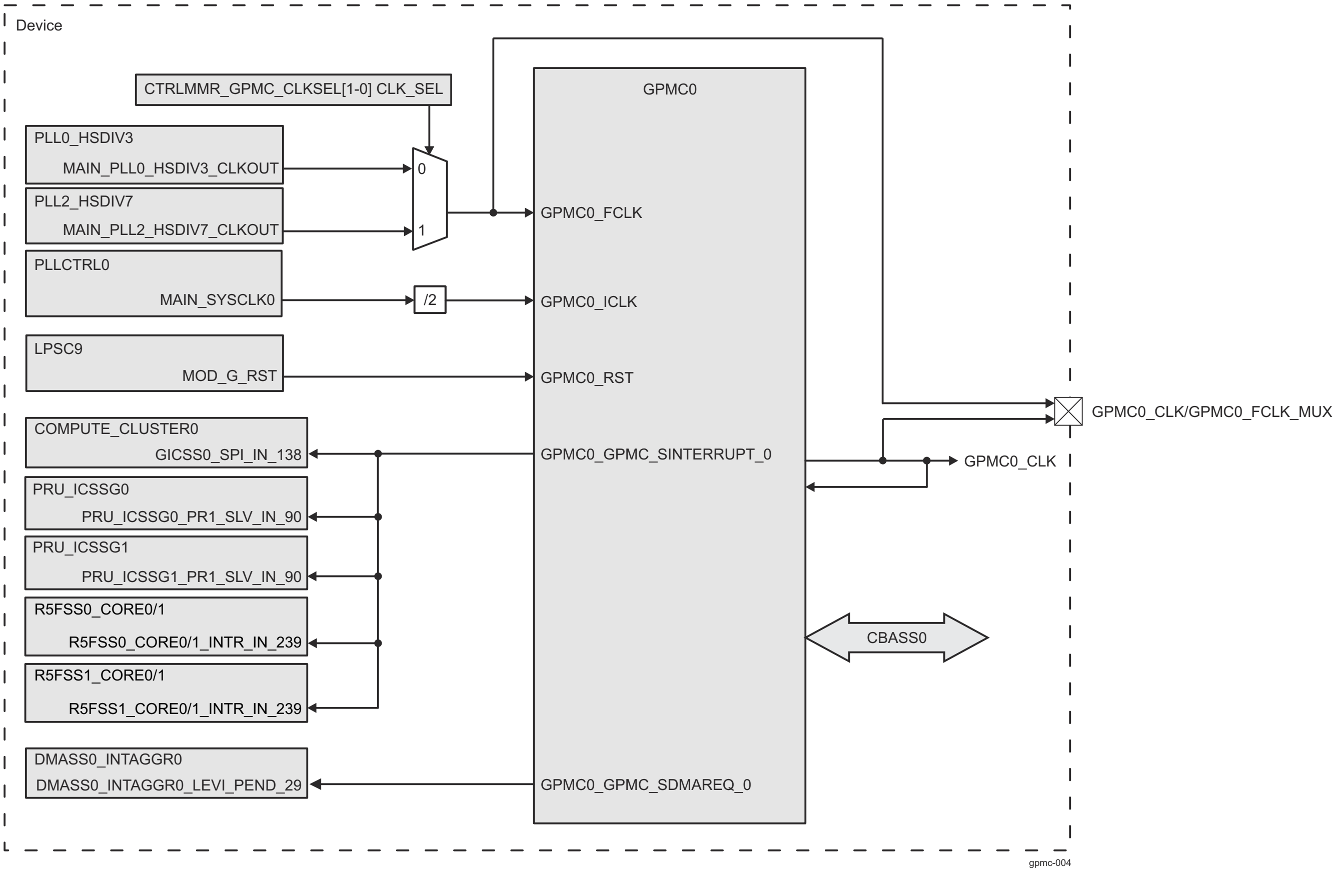

Figure 12-166. GPMC0 Integration

Table 12-243 through Table 12-246 summarize the integration of GPMC0 in device MAIN domain.

Table 12-255. GPMC0 Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
GPMC0	PSC0	PD0	LPSC9	CBASS0

Table 12-256. GPMC0 Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
GPMC0	GPMC0_FCLK	MAIN_PLL0_HSDIV3_CLKOUT	PLL0_HSDIV3	GPMC0 Functional Clock. For more information about clock multiplexing, see MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL[1-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MAIN_PLL2_HSDIV7_CLKOUT	PLL2_HSDIV7	
	GPMC0_ICLK	MAIN_SYSCLK0/2	PLLCTRL0	GPMC0 Interface Clock

Table 12-257. GPMC0 Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
GPMC0	GPMC0_RST	MOD_G_RST	LPSC9	GPMC0 Asynchronous Reset

Table 12-258. Interrupt Requests

Module Instance	Module Interrupt Input	Source Interrupt Signal	Destination	Description	Type
GPMC0	GPMC0_GPMC_SINTERRUPT_0	GICSS0_SPI_IN_138	COMPUTE_CLUSTER0	GPMC0 Interrupt Request	Level
		PRU_ICSSG0_PR1_SLV_IN_90	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_90	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_239	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_239	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_239	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_239	R5FSS1_CORE1		

Table 12-259. GPMC0 DMA Events

Module Instance	Module Interrupt Input	Source Interrupt Signal	Destination	Description	Type
GPMC0	GPMC0_GPMC_SDMAREQ_0	DMASS0_INTAGGR0_LEVI_PEND_29	DMASS0_INTAGGR0	DMA Event	Level

Note

GPMC0 interrupts are further described in Section 12.3.3.4.4 , *GPMC Interrupt Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.3.3.4 GPMC Functional Description

The GPMC basic programming model offers maximum flexibility to support various access protocols for each of the four configurable chip-selects. Use optimal chip-select settings, based on the characteristics of the external device:

- Different protocols can be selected to support generic asynchronous or synchronous random-access devices (NOR flash, SRAM) or to support specific NAND devices.
- The address and data bus can be multiplexed on the same external bus.
- Read and write access can be independently defined as asynchronous or synchronous.
- System requests (byte, 16-bit word, burst) are performed through single or multiple accesses. External access profiles (single, multiple with optimized burst length, native- or emulated-wrap) are based on external device characteristics (supported protocol, bus width, data buffer size, native-wrap support).
- System burst read or write requests are synchronous-burst (multiple-read or multiple-write). When neither burst nor page mode is supported by external memory or ASIC devices, system burst read or write requests are translated to successive single synchronous or asynchronous accesses (single reads or single writes). 8-bit wide devices are supported only in single synchronous or single asynchronous read or write mode.
- To simulate a programmable internal-wait-state, an external WAIT pin can be monitored to dynamically control external access at the beginning (initial access time) of and during a burst access.

Each control signal is controlled independently for each chip-select. The internal functional clock of the GPMC (GPMC_FCLK) is used as a time reference to specify the following:

- Read- and write-access duration
- Most GPMC external interface control-signal assertion and deassertion times
- Data-capture time during read access
- External wait-pin monitoring time
- Duration of idle time between accesses, when required

12.3.3.4.1 GPMC Block Diagram

Figure 12-167 shows the GPMC functional block diagram. The GPMC consists of six blocks:

- Interconnect port interface
- Address decoder, GPMC configuration, and chip-select configuration register file
- Access engine
- Prefetch and write-posting engine
- Error correction code engine (ECC)
- External device/memory port interface

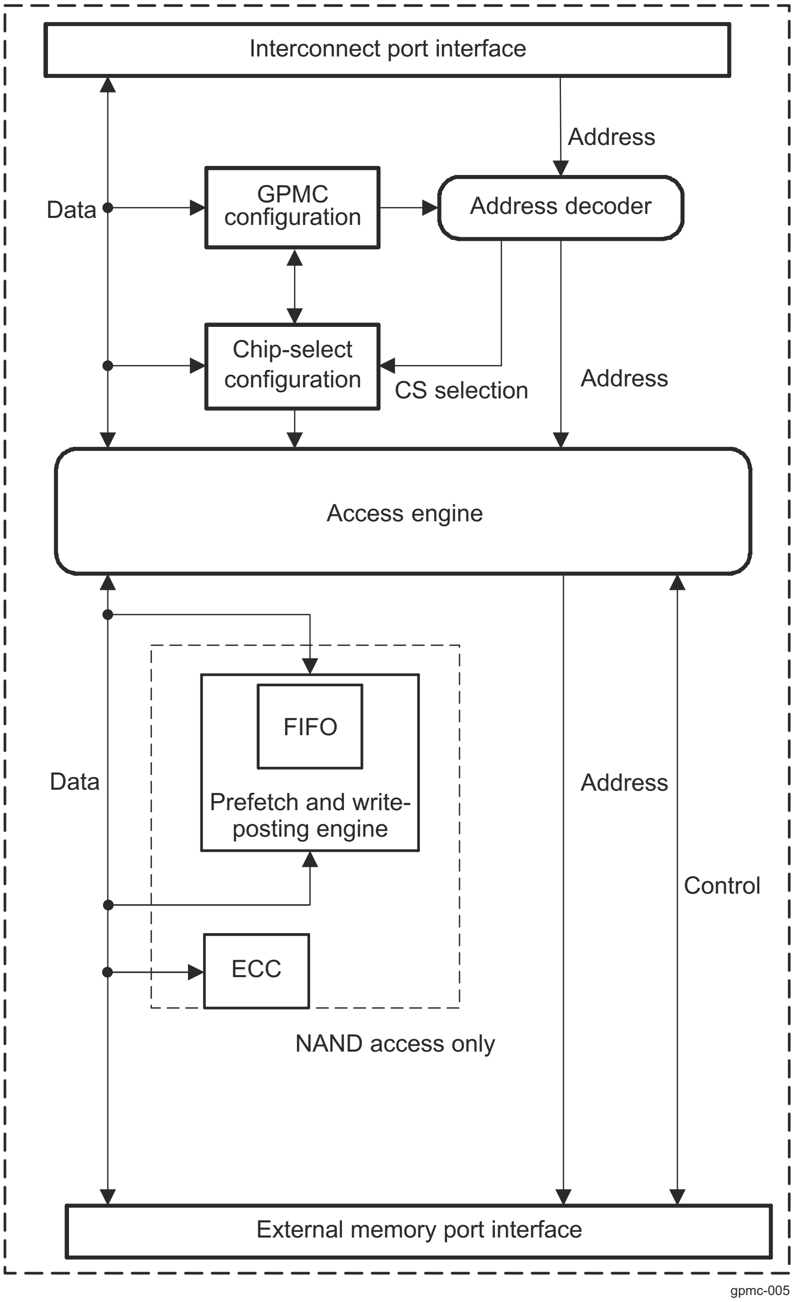

Figure 12-167. GPMC Block Diagram

The GPMC can access various external devices. The flexible programming model allows a wide range of attached device types and access schemes.

Based on the programmed configuration bit fields stored in the GPMC registers, the GPMC can generate the timing of all control signals depending on the attached device and access type.

Given the chip-select decoding and its associated configuration registers, the GPMC selects the appropriate control signal timing for the device type.

12.3.3.4.2 GPMC Clock Configuration

Table 12-248 describes the GPMC clocks.

Table 12-260. GPMC Clocks

Signal	I/O[1]	Description
GPMC_FCLK	I	Functional clock
GPMC_ICLK	I	Interface clock
CLK (GPMC_CLKOUT pin)	O	External clock provided to synchronous external memory devices and to DCC5 in the device.

(1) I = Input; O = Output; I/O - Bidirectional

The GPMC output clock (CLK) is generated by the GPMC from the internal GPMC_FCLK clock. The source of the GPMC_FCLK is described in *GPMC0 Clocks*. The GPMC output clock is configured using the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field (where i = 0 to 3), as shown in Table 12-249.

Table 12-261. GPMC Output Clock Configuration

Source Clock	GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER	GPMC Output Clock Provided to External Memory Device
GPMC_FCLK	00	GPMC_FCLK
	01	GPMC_FCLK/2
	10	GPMC_FCLK/3
	11	GPMC_FCLK/4

When using synchronous interface protocols, the GPMC output clock (CLK), toggles only during the read or write access cycle. In some applications, it may be desirable to have a continuous clock running at the GPMC interface clock frequency for clocking attached devices. This option is enabled by an optional clock path from GPMC functional clock input (GPMC_FCLK) to GPMC_FCLK_MUX. And output of this mux can be selected by CLKOUT_SEL bit field for GPMC_CONTROL Register present in MSS_CTRL. For more details, see MSS_CTRL chapter in GPMC Global Configuration.

Note that when using such synchronous interface protocols with the continuous clock option, user should ensure that the GPMC outputs are timed to the same frequency (GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0).

12.3.3.4.3 GPMC Power Management

Table 12-250 describes the local power-management features available for the GPMC module.

Table 12-262. GPMC Local Power-Management Features

Feature	Registers	Description
Clock autogating	GPMC_SYSCONFIG[0] AUTOIDLE	This bit allows a local power optimization inside the module, by gating the GPMC_ICLK clock upon the internal activity.
Target idle modes	GPMC_SYSCONFIG[4-3] IDLEMODE	Force-idle, no-idle and smart-idle modes are available.

12.3.3.4.4 GPMC Interrupt Requests

The GPMC generates one interrupt request (see *GPMC0 Hardware Requests*).

Table 12-251 lists the event flags, and their mask, that can cause module interrupts.

Table 12-263. GPMC Interrupt Events

Event Flag	Event Mask	Sensitivity	Description
GPMC_IRQSTATUS[9] WAIT1EDGE DETECTIONSTATUS	GPMC_IRQENABLE[9] WAIT1EDGE DETECTIONENABLE	Edge	Wait1 edge detection interrupt: Triggered if a rising or falling edge is detected on the GPMC_WAIT1 signal. The rising or falling edge detection of Wait1 is selected through the GPMC_CONFIG[9] WAIT1PINPOLARITY bit.

Table 12-263. GPMC Interrupt Events (continued)

Event Flag	Event Mask	Sensitivity	Description
GPMC_IRQSTATUS[8] WAIT0EDGE DETECTIONSTATUS	GPMC_IRQENABLE[8] WAIT0EDGE DETECTIONENABLE	Edge	Wait0 edge detection interrupt: Triggered if a rising or falling edge is detected on the GPMC_WAIT0 signal. The rising or falling edge detection of Wait0 is selected through the GPMC_CONFIG[8] WAIT0PINPOLARITY bit.
GPMC_IRQSTATUS[1] TERMINAL COUNTSTATUS	GPMC_IRQENABLE[1] TERMINAL COUNTENABLE	Level	Terminal count event: Triggered on prefetch process completion; that is, when the number of currently remaining data to be requested reaches 0.
GPMC_IRQSTATUS[0] FIFOEVENTSTATUS	GPMC_IRQENABLE[0] FIFOEVENTENABLE	Level	FIFO event interrupt: Indicates available FIFO levels for write-posting mode and prefetch mode. GPMC_PREFETCH_CONFIG1[2] DMAMODE must be set to 0.

12.3.3.4.5 GPMC Interconnect Port Interface

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

The GPMC interconnect interface is a pipelined interface including a 16 × 32-bit word write buffer.

Any system host can issue external access requests through the GPMC.

The device system can issue the following requests through this interface:

- One 8-, 16-, or 32-bit interconnect access (read/write)
- Two incrementing 32-bit interconnect accesses (read/write)
- Two wrapped 32-bit interconnect accesses (read/write)
- Four incrementing 32-bit interconnect accesses (read/write)
- Four wrapped 32-bit interconnect accesses (read/write)
- Eight incrementing 32-bit interconnect accesses (read/write)
- Eight wrapped 32-bit interconnect accesses (read/write)

Only linear burst transactions are supported; interleaved burst transactions are not supported. Only power-of-two-length precise bursts 2 × 32, 4 × 32, 8 × 32, and 16 × 32, with the burst base address aligned on the total burst size, are supported (this limitation applies to incrementing bursts only).

This interface also provides one interrupt and one DMA request line for specific event control.

It is recommended to program the GPMC_CONFIG1_i[24-23] ATTACHEDDEVICEPAGELENGTH bit field according to the page length of the effective attached device and to enable the GPMC_CONFIG1_i[31] WRAPBURST bit if the attached device supports wrapping burst.

It is possible, however, to emulate wrapping burst on a nonwrapping memory by providing relevant addresses within the page or by splitting transactions. Bursts larger than the memory page length are chopped into multiple burst transactions. Because of the alignment requirements, a page boundary is never crossed.

12.3.3.4.6 GPMC Address and Data Bus

The current application supports GPMC connection to NAND devices and to address/data-multiplexed memories or devices. Connection to address/data-non-multiplexed memories or devices is supported with an address range of 4MB.

Depending on the GPMC configuration of each chip-select, address and data bus lines that are not required for a particular access protocol are not updated (changed from current value) and are not sampled when input (input data bus).

- For address/data-multiplexed and AAD-multiplexed NOR devices, the address is multiplexed on the data bus.

- 8-bit-wide NOR devices do not use GPMC I/O: GPMC_AD[15-8] for data (they are used for address if needed).
- 16-bit-wide NAND devices do not use GPMC I/O: GPMC_A[22-0].
- 8-bit-wide NAND devices do not use GPMC I/O: GPMC_A[22-0] and GPMC I/O: GPMC_AD[15-8].

12.3.3.4.6.1 GPMC I/O Configuration Setting

Note

In this section and the following sections, the i in GPMC_CONFIGx_i stands for the GPMC chip-select i, where i = 0 to 3.

To select a NAND device, program the following register fields:

- GPMC_CONFIG1_i[11-10] DEVICETYPE = 0b10
- GPMC_CONFIG1_i[9-8] MUXADDDATA = 0b00

To select an address/data-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11-10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9-8] MUXADDDATA = 0b10

To select an address/address/data-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11-10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9-8] MUXADDDATA = 0b01

To select an address/data-non-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11-10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9-8] MUXADDDATA = 0b00

12.3.3.4.7 GPMC Address Decoder and Chip-Select Configuration

Addresses are decoded accordingly with the address request of the chip-select and the content of the chip-select base address register file, which includes a set of global GPMC configuration registers and four sets of chip-select configuration registers.

The GPMC configuration register file is memory-mapped and can be read or written with byte, 16-bit word, or 32-bit word accesses. The register file must be configured as a noncacheable, nonbufferable region to prevent any desynchronization between host execution (write request) and the completion of register configuration (write completed with register updated).

After the chip-select is configured, the access engine accesses the external device, drives the external interface control signals, and applies the interface protocol based on user-defined timing parameters and settings.

12.3.3.4.7.1 Chip-Select Base Address and Region Size

Any external memory or ASIC device attached to the GPMC external interface can be accessed by any device system host within the GPMC 128MB address space. For more information, see *Memory Map*.

Note

Even though GPMC supports total address space of 1GB, only 128MB are physically available in this device.

The GPMC 128MB address space can be divided into a maximum of four chip-select regions with programmable base address and programmable chip-select size. The chip-select size is programmable from 16MB to 256MB (must be a power-of-two) and is defined by the mask field. Attached memory smaller than the programmed chip-select region size is accessed through the entire chip-select region (aliasing).

Each chip-select has a 6-bit base address encoding and 4-bit decoding mask, which must be programmed according to the following rules:

- The programmed chip-select region base address must be aligned on the chip-select region size address boundary and is limited to a power-of-two address value. During access decoding, the value of the register base address is used to compare the address with the address bit line mapping, as shown in Figure 12-168 (with A0 as the device system byte-address line). The base address is programmed through the GPMC_CONFIG7_i[5-0] BASEADDRESS bit field.
- The register mask is used to exclude some address lines from the decoding. A register mask bit field set to 0 suppresses the associated address line from the address comparison (incoming address bit line is don't care). The value of the register mask must be limited to the subsequent value, based on the desired chip-select region size. Any other value has an undefined result. When multiple chip-select regions with overlapping addresses are enabled concurrently, access to these chip-select regions is cancelled and a GPMC access error is posted. The mask field is programmed through the GPMC_CONFIG7_i[11-8] MASKADDRESS bit field.

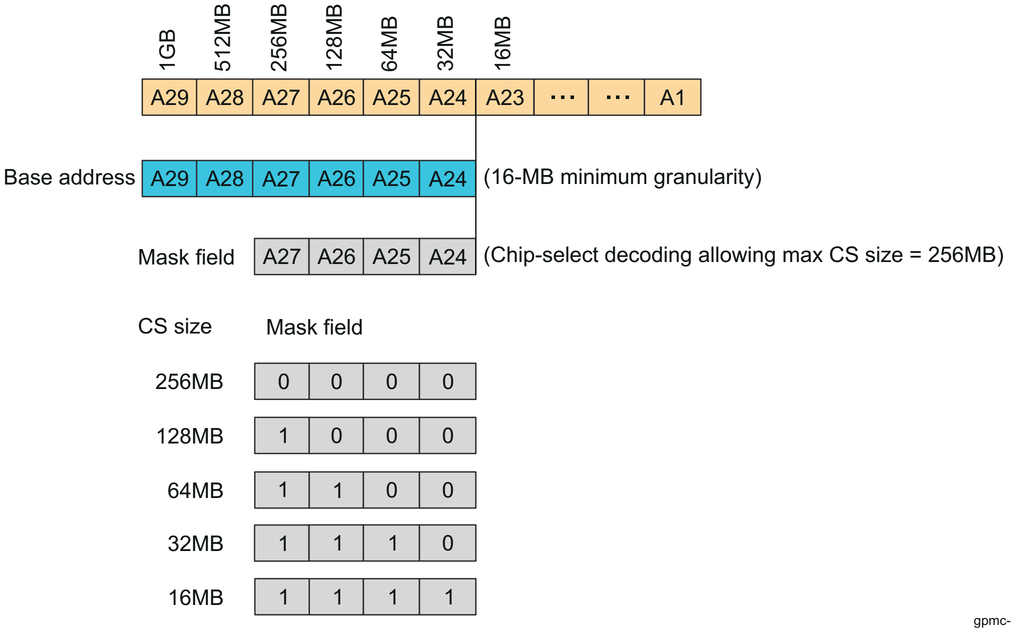

Figure 12-168. Chip-Select Address Mapping and Decoding Mask

For example, to map the 128MB address space (from 5000 0000h to 57FF FFFFh), the GPMC_CONFIG7_i[5-0] BASEADDRESS bit field should be set to 28h.

Eg : 68000000h = 01**10_1000**_0000_0000_0000_0000_0000_0000b

Base Address[29:24] = 10_1000 = 28h

Chip-select configuration (base and mask address or any protocol and timing settings) must be performed while the associated chip-select is disabled through the GPMC_CONFIG7_i[6] CSVALID bit (where i stands for the GPMC chip-select i, where i = 0 to 3). In addition, a chip-select configuration can be disabled only if there is no ongoing access to that chip-select. This requires monitoring the activity of the prefetch or write-posting engine if the engine is active on the chip-select. Also, the write buffer state must be monitored to wait for any posted write completion to the chip-select.

Any access attempted to a nonvalid GPMC address region (CSVALID disabled or address decoding outside a valid chip-select region) is not propagated to the external interface and a GPMC access error is posted. In case of overlapping chip-selects, an error is generated and no access occurs on either chip-select.

CS0 is the only chip-select region enabled after a power up or GPMC reset.

CAUTION

Although the GPMC interface can drive up to four chip-selects, the frequency specified for this interface is for a specific load. If this load is exceeded, the maximum frequency cannot be reached. One solution is to implement a board with buffers to allow the slowest device to maintain the total load on the lines at the value specified in the device-specific Datasheet.

12.3.3.4.7.2 Access Protocol

12.3.3.4.7.2.1 Supported Devices

The access protocol of each chip-select can be independently specified through the GPMC_CONFIG1_i[11-10] DEVICETYPE parameter (where i = 0 to 3) for:

- Random-access synchronous or asynchronous memory, such as NOR flash and SRAM
- NAND flash asynchronous devices

Note

For more information about the NAND flash GPMC basic programming model and NAND support, see Section 12.3.3.4.11 , *GPMC NAND Device Basic Programming Model*, and Section 12.3.3.4.11.1 , *NAND Memory Device in Byte or Word16 Stream Mode*.

12.3.3.4.7.2.2 Access Size Adaptation and Device Width

Each chip-select can be independently configured through the GPMC_CONFIG1_i[13-12] DEVICESIZE bit field (where i = 0 to 3) to interface with a 16- or 8-bit-wide device. System requests with data width greater than the external device data bus width are split into successive accesses according to the external device data-bus width and little-endian data organization.

12.3.3.4.7.2.3 Address/Data-Multiplexing Interface

For random synchronous or asynchronous memory interfacing (DEVICETYPE = 0b00), an address- and data-multiplexing protocol can be selected through the GPMC_CONFIG1_i[9-8] MUXADDDATA bit field (where i = 0 to 3). The nADV signal must be used as the external device address latch control signal. For the associated chip-select configuration, nADV assertion and deassertion time and nOE assertion time must be set to the appropriate value to meet the address latch setup/hold time requirements of the external device. See *GPMC Integration*.

Note

This address/data-multiplexing interface is not applicable to NAND device interfacing. NAND devices require a specific address, command, and data-multiplexing protocol. See Section 12.3.3.4.11 , *NAND Device Basic Programming Model*.

12.3.3.4.7.3 External Signals

12.3.3.4.7.3.1 WAIT Pin Monitoring Control

GPMC access time can be dynamically controlled using an external GPMC_WAIT pin when the external device access time is not deterministic and cannot be defined and controlled using only the GPMC internal RDACCESSTIME, WRACCESSTIME, and PAGEBURSTACCESSTIME wait-state generator.

The GPMC features two input WAIT pins: GPMC_WAIT1, and GPMC_WAIT0. These pins allow control of external devices with different WAIT pin polarity. They also allow the overlap of WAIT pin assertion from different devices without affecting access to devices for which the WAIT pin is not asserted.

- The GPMC_CONFIG1_i[17-16] WAITPINSELECT bit field (where i = 0 to 3) selects which input GPMC_WAIT pin is used for the device attached to the corresponding chip-select.

- The polarity of the WAIT pin is defined through the WAITxPINPOLARITY bit of the GPMC_CONFIG register. A WAIT pin configured to be active low means that low level on the WAIT signal indicates that the data is not ready and that the data bus is invalid. When a WAIT pin is inactive, data is valid.

The GPMC access engine can be configured per chip-select to monitor or not the WAIT pin of the external memory device, based on the access type: read or write.

- The GPMC_CONFIG1_i[22] WAITREADMONITORING bit defines whether or not the WAIT pin must be monitored during read accesses.
- The GPMC_CONFIG1_i[21] WAITWRITEMONITORING bit defines whether or not the WAIT pin must be monitored during write accesses.

The GPMC access engine can be configured to monitor the WAIT pin of the external memory device asynchronously or synchronously with the GPMC output clock, depending on the access type: synchronous or asynchronous (the GPMC_CONFIG1_i[29] READTYPE and GPMC_CONFIG1_i[27] WRITETYPE bits).

12.3.3.4.7.3.1.1 Wait Monitoring During Asynchronous Read Access

When WAIT pin monitoring is enabled for read accesses (WAITREADMONITORING), the effective access time is a logical AND combination of the RDACCESSTIME timing completion and the wait-deasserted state.

During asynchronous read accesses with WAIT pin monitoring enabled, the WAIT pin must be at a valid level (asserted or deasserted) for at least two GPMC clock cycles before RDACCESSTIME completes, to ensure correct dynamic access-time control through WAIT pin monitoring. The advance pipelining of the two GPMC clock cycles is the result of the internal synchronization requirements for the WAIT signal.

In this context, RDACCESSTIME is used as a wait invalid timing window and is set to such a value that the WAIT pin is at a valid state two GPMC clock cycles before RDACCESSTIME completes.

Similarly, during a multiple-access cycle (for example, asynchronous read page mode), the effective access time is a logical AND combination of PAGEBURSTACCESSTIME timing completion and the wait-deasserted state. Wait monitoring pipelining is also applicable to multiple accesses (access within a page).

- Wait monitored as active freezes the CYCLETIME counter. For an access within a page, when the CYCLETIME counter is by definition in a lock state, wait monitored as asserted extends the current access time in the page. Control signals are kept in their current state. The data bus is considered invalid, and no data are captured during this clock cycle.
- Wait monitored as inactive unfreezes the CYCLETIME counter. For an access within a page, when the CYCLETIME counter is by definition in a lock state, wait monitored as inactive completes the current access time and starts the next access phase in the page. The data bus is considered valid, and data are captured during this clock cycle. In case of a single access or if this was the last access in a multiple-access cycle, all signals are controlled according to their related control timing value and according to the CYCLETIME counter status.

When a delay larger than two GPMC clocks must be observed between wait-pin deactivation time and data valid time (including the required GPMC and the device data setup time), an extra delay can be added between wait-pin deassertion time detection and effective data-capture time and the effective unlock of the CYCLETIME counter. This extra delay can be programmed in the GPMC_CONFIG1_i[19-18] WAITMONITORINGTIME bit field (where i = 0 to 3).

Note

- The WAITMONITORINGTIME parameter does not delay the WAIT pin active or inactive detection, nor does it modify the two GPMC clocks pipelined detection delay.
- This extra delay is expressed as a number of GPMC output clock cycles, even though the access is defined as asynchronous, and no GPMC output clock is provided to the external device. Still, because GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER is used as a divider for the GPMC clock, it must be programmed to define the correct WAITMONITORINGTIME delay.

Figure 12-169 shows wait behavior during an asynchronous single read access.

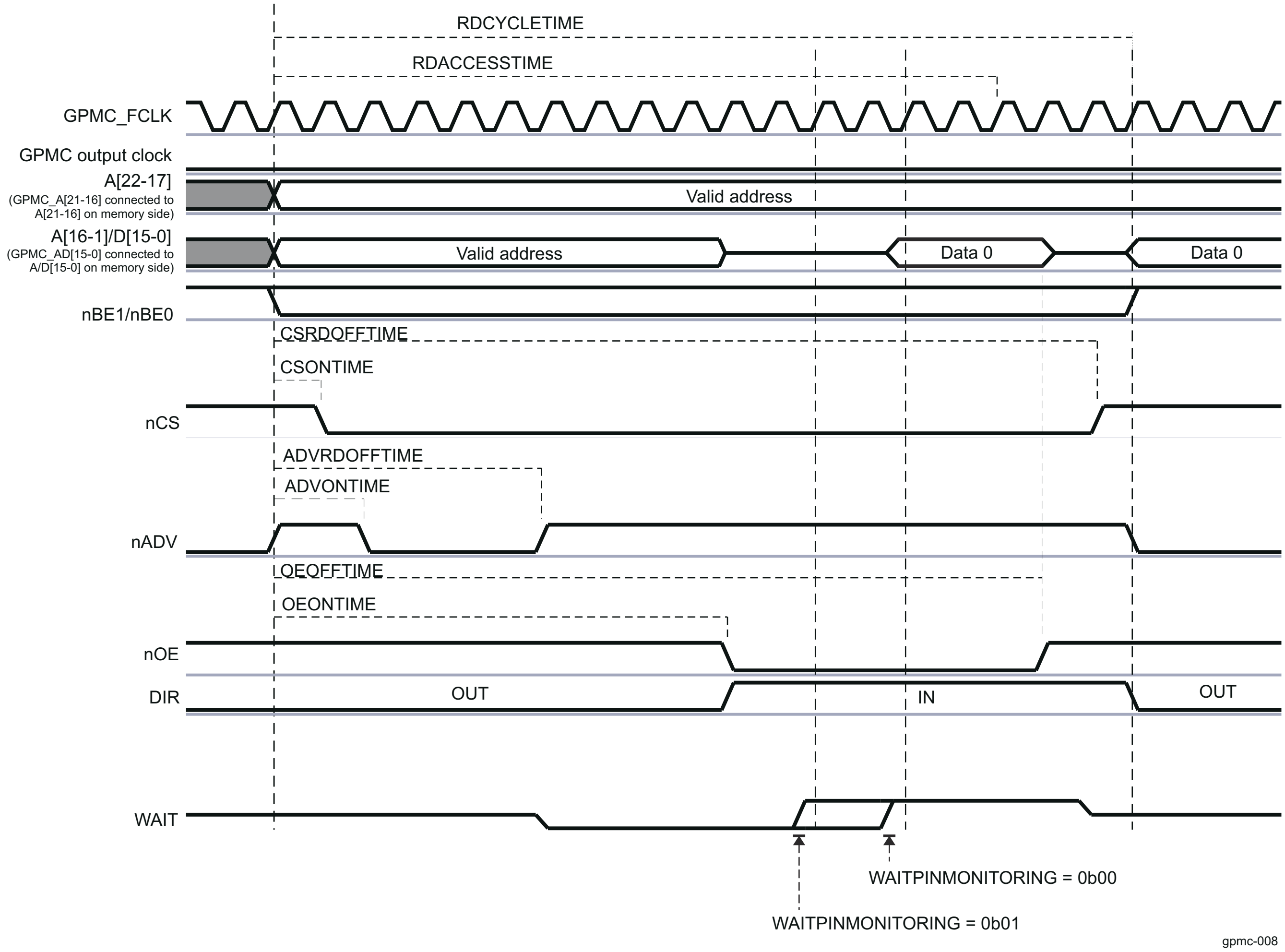

Figure 12-169. Wait Behavior During an Asynchronous Single Read Access (GPMCFCLKDivider = 1)

Note

The WAIT signal is active low. GPMC_CONFIG1_i[19-18] WAITMONITORINGTIME = 0b00, or 0b01.

12.3.3.4.7.3.1.2 Wait Monitoring During Asynchronous Write Access

When WAIT pin monitoring is enabled for write accesses (GPMC_CONFIG1_i[21] WAITWRITEMONITORING bit = 0x1), the wait invalid timing window is defined by the WRACCESSTIME field. WRACCESSTIME must be set so that the WAIT pin is at a valid state two GPMC clock cycles before WRACCESSTIME completes. The advance pipelining of the two GPMC clock cycles is the result of the internal synchronization requirements for the WAIT signal.

- Wait monitored as active freezes the CYCLETIME counter. This informs the GPMC that the data bus is not captured by the external device. The control signals are kept in their current state. The data bus still drives the data.
- Wait monitored as inactive unfreezes the CYCLETIME counter. This informs that the data bus is correctly captured by the external device. All signals, including the data bus, are controlled according to their related control timing value and to the CYCLETIME counter status.

When a delay larger than two GPMC clock cycles must be observed between wait-pin deassertion time and the effective data write into the external device (including the required GPMC data setup time and the device data setup time), an extra delay can be added between wait-pin deassertion time detection and effective data write time into the external device and the effective unfreezing of the CYCLETIME counter. This extra delay can be programmed in the GPMC_CONFIG1_i[19-18] WAITMONITORINGTIME bit field (where i = 0 to 3).

Note

- The WAITMONITORINGTIME parameter does not delay the WAIT pin assertion or deassertion detection, nor does it modify the two GPMC clock cycles pipelined detection delay.
- This extra delay is expressed as a number of GPMC output clock cycles, even though the access is defined as asynchronous, and even though no clock is provided to the external device. Still, because the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field is used as a divider for the GPMC clock, it must be programmed to define the correct WAITMONITORINGTIME delay.

12.3.3.4.7.3.1.3 Wait Monitoring During Synchronous Read Access

During synchronous accesses with WAIT pin monitoring enabled, the WAIT pin is captured synchronously with GPMC output clock, using the rising edge of this clock.

The WAIT signal can be programmed to apply to the same clock cycle in which it is captured. Alternatively, it can be sampled one or two GPMC output clock cycles ahead of the clock cycle to which it applies. This pipelining is applicable to the entire burst access and to all data phases in the burst access. This wait pipelining depth is programmed in the GPMC_CONFIG1_i[19-18] WAITMONITORINGTIME bit field (where i = 0 to 3), and is expressed as a number of GPMC output clock cycles.

In synchronous mode, when WAIT pin monitoring is enabled (the GPMC_CONFIG1_i[22] WAITREADMONITORING bit), the effective access time is a logical AND combination of the RDACCESSTIME timing completion and the wait-deasserted state detection.

Depending on the programmed value of WAITMONITORINGTIME, the WAIT pin must be at a valid level, either asserted or deasserted:

- In the same clock cycle the data is valid if WAITMONITORINGTIME = 0 (at RDACCESSTIME completion)
- In the WAITMONITORINGTIME x (GPMCFCLKDIVIDER + 1) GPMC_FCLK clock cycles before RDACCESSTIME completion if WAITMONITORINGTIME is not equal to 0

Similarly, during a multiple-access cycle (burst mode), the effective access time is a logical AND combination of PAGEBURSTACCESSTIME timing completion and the WAIT-INACTIVE state. The wait pipelining-depth programming applies to the whole burst access.

- Wait monitored as active freezes the CYCLETIME counter. For an access within a burst (when the CYCLETIME counter is by definition in a lock state), wait monitored as active extends the current access time in the burst. Control signals are kept in their current state. The data bus is considered invalid, and no data are captured during this clock cycle.
- Wait monitored as inactive unfreezes the CYCLETIME counter. For an access within a burst (when the CYCLETIME counter is by definition in lock state), wait monitored as inactive completes the current access time and starts the next access phase in the burst. The data bus is considered valid, and data are captured during this clock cycle. In a single access or if this was the last access in a multiple-access cycle, all signals are controlled according to their relative control timing value and the CYCLETIME counter status.

Figure 12-170 shows wait behavior during a synchronous read burst access.

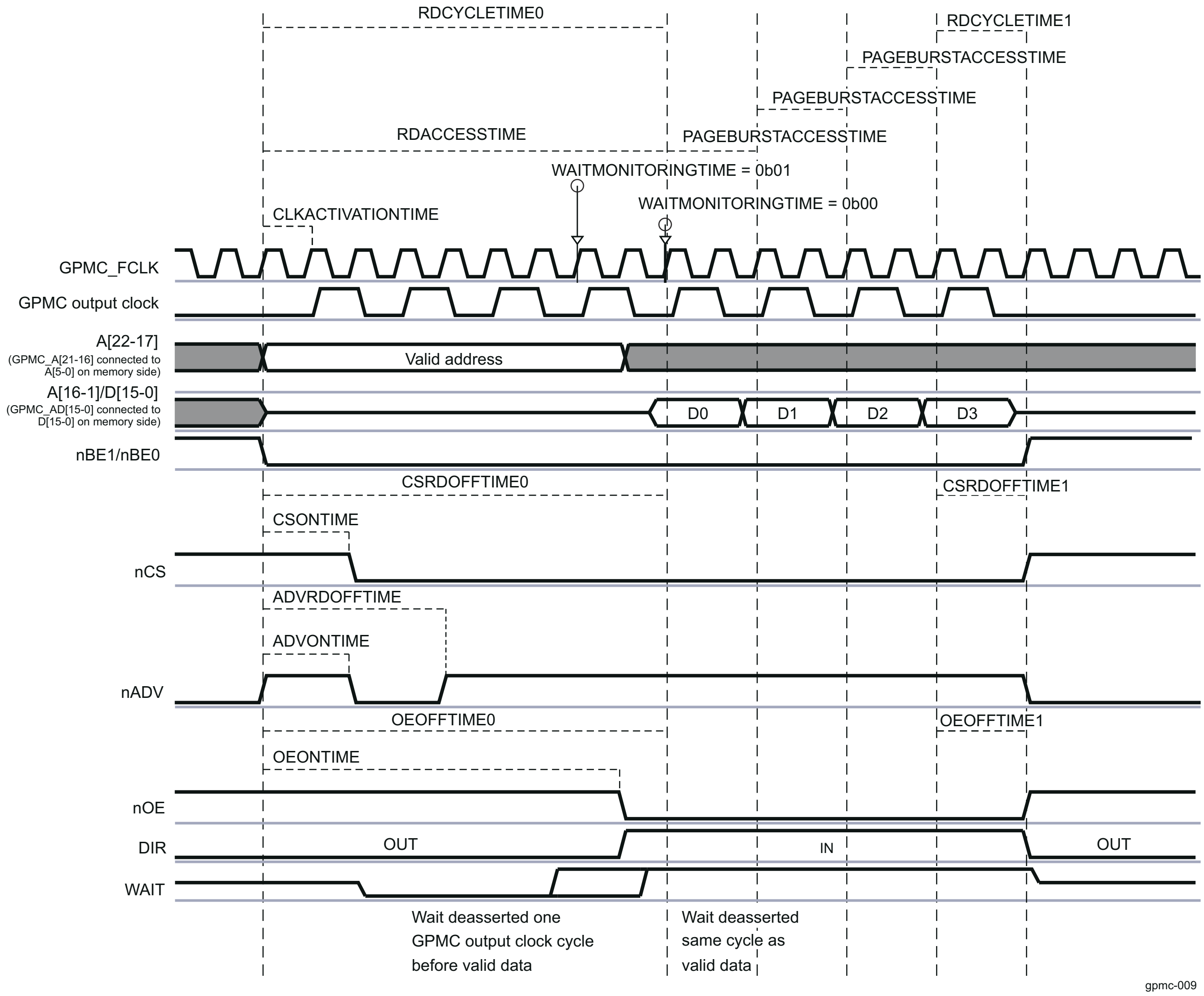

Figure 12-170. Wait Behavior During a Synchronous Read Burst Access

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Note

The WAIT signal is active low. WAITMONITORINGTIME = 0b00, 0b01.

12.3.3.4.7.3.1.4 Wait Monitoring During Synchronous Write Access

During synchronous accesses with WAIT pin monitoring enabled (the GPMC_CONFIG1_i[21] WAITWRITEMONITORING bit), the WAIT pin is captured synchronously with GPMC output clock, using the rising edge of this clock.

If enabled, external WAIT pin monitoring can be used in combination with WRACCESSTIME to delay the GPMC output clock capture edge of the effective memory device.

WAIT-monitoring pipelining depth is similar to synchronous read access:

- At WRACCESSTIME completion if WAITMONITORINGTIME = 0
- In the WAITMONITORINGTIME x (GPMCFCLKDIVIDER + 1) GPMC_FCLK cycles before WRACCESSTIME completion if WAITMONITORINGTIME is not equal to 0

Wait-monitoring pipelining definition applies to whole burst accesses:

- Wait monitored as active freezes the CYCLETIME counter. For accesses within a burst, when the CYCLETIME counter is by definition in a lock state, wait monitored as active indicates that the data bus is not being captured by the external device. Control signals are kept in their current state. The data bus is kept in its current state.
- Wait monitored as inactive unfreezes the CYCLETIME counter. For accesses within a burst, when the CYCLETIME counter is by definition in a lock state, wait monitored as inactive indicates the effective data capture of the bus by the external device and starts the next access of the burst. In case of a single access or if this was the last access in a multiple access cycle, all signals, including the data bus, are controlled according to their related control timing value and the CYCLETIME counter status.

Note

WAIT monitoring is supported for all configurations except GPMC_CONFIG1_i[19-18] WAITMONITORINGTIME = 0x0 (where i = 0 to 3) for write bursts with a clock divider of 1 or 2 (the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field is equal to 0x0 or 0x1, respectively).

12.3.3.4.7.3.1.5 Wait With NAND Device

For information about the use of the WAIT pin for communication with a NAND flash external device, see Section 12.3.3.4.11.2 , *NAND Device-Ready Pin*.

12.3.3.4.7.3.1.6 Idle Cycle Control Between Successive Accesses

12.3.3.4.7.3.1.6.1 Bus Turnaround (BUSTURNAROUND)

To prevent data-bus contention, an access that follows a read access to a slow memory/device must be delayed (in other words, control the nCS/nOE deassertion to data bus in high-impedance delay).

The bus turnaround is a time-out counter starting after nCS or nOE deassertion time, whichever occurs first, and delays the next access start-cycle time. The counter is programmed through the GPMC_CONFIG6_i[11-8] BUSTURNAROUND bit field (where i = 0 to 3).

After a read access to a chip-select with a nonzero BUSTURNAROUND, the next access is delayed until the BUSTURNAROUND delay completes, if the next access is one of the following:

- A write access to any chip-select (the same or different chip-select from which the data was read)
- A read access to a different chip-select than the chip-select from which the data was read access
- A read or write access to a chip-select associated with an address/data-multiplexed device

Note

Bus keeping starts after bus turnaround completion so that DIR changes from IN to OUT after bus turnaround. The bus does not have enough time to go into high-impedance even though it can be driven with the same value before bus turnaround timing.

BUSTURNAROUND delay runs in parallel with GPMC_CONFIG6_i[11:8] CYCLE2CYCLEDELAY bit field delays. BUSTURNAROUND is a timing parameter for the ending chip-select access, while CYCLE2CYCLEDELAY is a timing parameter for the following chip-select access. The effective minimum delay between successive accesses is driven by these delay timing parameters and by the access type of the following access (see Figure 12-171 through Figure 12-173).

Another way to prevent bus contention is to define an earlier nCS or nOE deassertion time for slow devices or to extend the value of RDCYCLETIME. Doing this prevents bus contention, but it also affects all accesses of this specific chip-select.

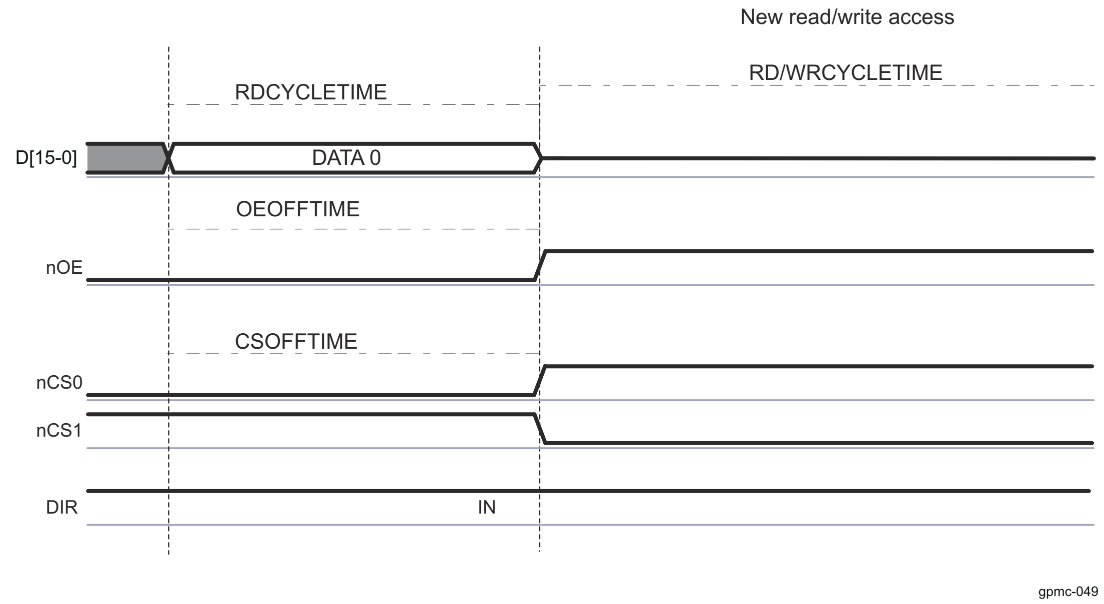

Figure 12-171. Read-to-Read for an Address-Data Multiplexed Device, on Different Chip-Select, Without Bus Turnaround (nCS Attached to a Fast Device)

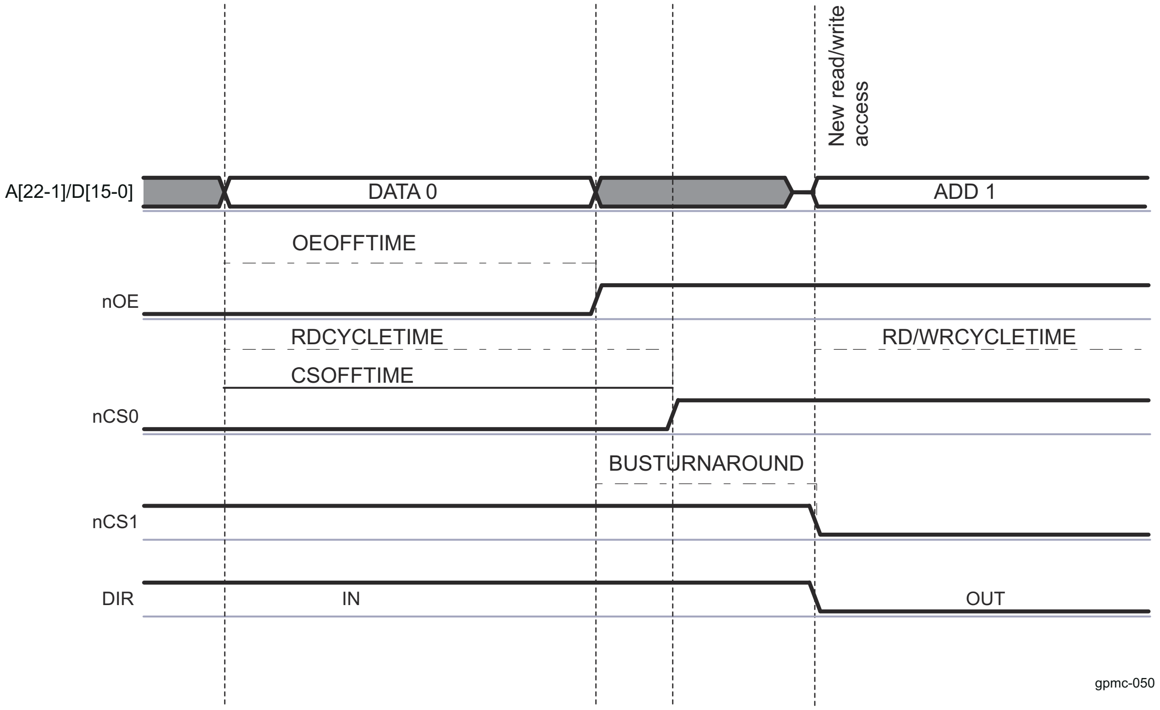

Figure 12-172. Read- to-Read/Write for an Address-Data Multiplexed Device, on Different Chip-Select, With Bus Turnaround

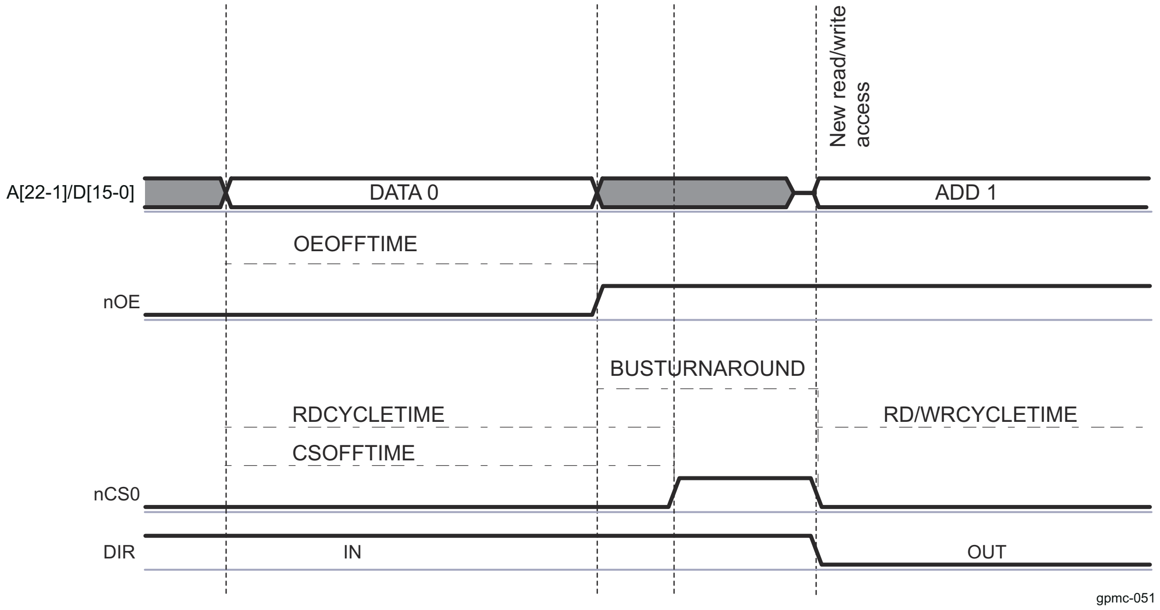

Figure 12-173. Read-to-Read/Write for a Address-Data or AAD-Multiplexed Device, on Same Chip-Select, With Bus Turnaround

12.3.3.4.7.3.1.6.2 Idle Cycles Between Accesses to Same Chip-Select (CYCLE2CYCLESAMECSEN, CYCLE2CYCLEDELAY)

Some devices require a minimum chip-select signal inactive time between accesses. The GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN bit (where i = 0 to 3) enables insertion of a minimum number of GPMC_FCLK cycles, defined by the GPMC_CONFIG6_i[11-8] CYCLE2CYCLEDELAY bit field, between successive accesses of any type (read or write) to the same chip-select.

If CYCLE2CYCLESAMECSEN is enabled, any subsequent access to the same chip-select is delayed until its CYCLE2CYCLEDELAY completes. The CYCLE2CYCLEDELAY counter starts when CSRDOFFTIME/CSWROFFTIME completes.

The same applies to successive accesses occurring during 32-bit word or burst accesses split into successive single accesses when the single-access mode is used (GPMC_CONFIG1_i[30] READMULTIPLE = 0 or GPMC_CONFIG1_i[28] WRITEMULTIPLE = 0).

All control signals (CS, ADV#/ALE, BE0#/CLE, WE#, and GPMC output clock (CLK)) are kept inactive (ADV#/ALE, BE0#/CLE, and GPMC output clock at low level; and CS, OE#/RE, and WE at high level) during the idle GPMC_FCLK cycles. This prevents back-to-back accesses to the same chip-select without idle cycles between accesses.

12.3.3.4.7.3.1.6.3 Idle Cycles Between Accesses to Different Chip-Select (CYCLE2CYCLEDIFFCSEN, CYCLE2CYCLEDELAY)

Because of the pipelined behavior of the system, successive accesses to different chip-selects can occur back-to-back with no idle cycles between accesses. Depending on the control signals (nCS, nADV/ALE, nBE0/CLE, nOE/RE, nWE) assertion and deassertion timing parameters and on the device timing parameters, the assertion times of some control signals may overlap between the successive accesses to a different chip-select. Similarly, some control signals (WE, OE/RE) may not respect required transition times.

To work around overlapping and to observe the required control-signal transitions, a minimum of CYCLE2CYCLEDELAY inactive cycles is inserted between the access being initiated to this chip-select and the previous access ending for a different chip-select. This applies to any type of access (read or write).

If the GPMC_CONFIG6_i[6] CYCLE2CYCLEDIFFCSEN bit is enabled, the chip-select access is delayed until CYCLE2CYCLEDELAY cycles have expired since the end of a previous access to a different chip-select.

CYCLE2CYCLEDELAY count starts at CSRDOFFTIME/CSWROFFTIME completion. All control signals are kept inactive during the idle GPMC_FCLK cycles.

Note

CYCLE2CYCLESAMECSEN and CYCLE2CYCLEDIFFCSEN must be set in the GPMC_CONFIG6_i registers to get idle cycles inserted between accesses on this chip-select and after accesses to a different chip-select, respectively.

The CYCLE2CYCLEDELAY delay runs in parallel with the BUSTURNAROUND delay. The BUSTURNAROUND is a timing parameter defined for the ending chip-select access, whereas CYCLE2CYCLEDELAY is a timing parameter defined for the starting chip-select access. The effective minimum delay between successive accesses is based on the larger delay timing parameter and on access type combination, because bus turnaround does not apply to all access types. For more information about bus turnaround, see Section 12.3.3.4.7.3.1.6.1 , *Bus Turnaround (BUSTURNAROUND)*.

Table 12-252 describes the configuration required for idle cycle insertion.

Table 12-264. Idle Cycle Insertion Configuration

1st Access Type	BUSTURNAROUND Timing Parameter	Second Access Type	Chip-Select	Add/Data Multiplexed	CYCLE2CYCLESAMECSEN Parameter	CYCLE2CYCLEDIFFCSEN Parameter	Idle Cycle Insertion Between the Two Accesses
R/W	= 0	R/W	Any	Any	0	x	No idle cycles are inserted if the two accesses are well pipelined.
R	> 0	R	Same	Nonmuxed	x	0	No idle cycles are inserted if the two accesses are well pipelined.
R	> 0	R	Different	Nonmuxed	0	0	BUSTURNAROUND cycles are inserted.
R	> 0	R/W	Any	Muxed	0	0	BUSTURNAROUND cycles are inserted.
R	> 0	W	Any	Any	0	0	BUSTURNAROUND cycles are inserted.
W	> 0	R/W	Any	Any	0	0	No idle cycles are inserted if the two accesses are well pipelined.
R/W	= 0	R/W	Same	Any	1	x	CYCLE2CYCLEDELAY cycles are inserted.
R/W	= 0	R/W	Different	Any	x	1	CYCLE2CYCLEDELAY cycles are inserted.
R/W	> 0	R/W	Same	Any	1	x	CYCLE2CYCLEDELAY cycles are inserted. If BTA idle cycles already apply on these two back-to-back accesses, the effective delay is max (BUSTURNAROUND, CYCLE2CYCLEDELAY).
R/W	> 0	R/W	Different	Any	x	1	CYCLE2CYCLEDELAY cycles are inserted. If BTA idle cycles already apply on these two back-to-back accesses, the effective delay is maximum (BUSTURNAROUND, CYCLE2CYCLEDELAY).

12.3.3.4.7.3.1.7 Slow Device Support (TIMEPARAGRANULARITY Parameter)

All access-timing parameters can be multiplied by 2 by setting the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit (where i stands for the GPMC chip-select i, where i = 0 to 3). Increasing all access timing parameters allows support of slow devices.

12.3.3.4.7.3.2 DIR Pin

The DIR pin is used to control I/O direction on the GPMC data bus GPMC_D[15-0]. Depending on pad multiplexing, this signal can be output and used externally to the device, if required. The DIR pin is low during transmit (OUT) and high during receive (IN).

For write accesses, the DIR pin stays OUT from start-cycle time to end-cycle time.

For read accesses, the DIR pin goes from OUT to IN at nOE assertion time and stays IN until:

- BUSTURNAROUND is enabled
  - The DIR pin goes from IN to OUT at end-cycle time plus programmable bus turnaround time.
- BUSTURNAROUND is disabled
  - After an asynchronous read access, the DIR pin goes from IN to OUT at RDACCESSTIME + 1 GPMC_FCLK cycle or when RDCYCLETIME completes, whichever occurs last.
  - After a synchronous read access, the DIR pin goes from IN to OUT at RDACCESSTIME + 2 GPMC_FCLK cycles or when RDCYCLETIME completes, whichever occurs last.

Because of the bus-keeping feature of the GPMC, after a read or write access and with no other accesses pending, the default value of the DIR pin is OUT (see Section 12.3.3.4.8.10 , *Bus Keeping Support*). In non-multiplexed devices, the DIR pin stays IN between two successive read accesses to prevent unnecessary toggling.

12.3.3.4.7.3.3 Reset

No reset signal is sent to the external memory device by the GPMC.

GPMC_RST is the reset signal for the GPMC module. It is connected and controlled by LPSC8 in VD_CORE. That reset signal initializes the internal state-machine and the internal configuration registers.

12.3.3.4.7.3.4 Write Protect Signal (nWP)

When connected to the attached memory device, the write protect signal can enable or disable the lockdown function of the attached memory. The nWP output pin value is controlled through the GPMC_CONFIG[4] WRITEPROTECT bit which is common for all chip selects.

12.3.3.4.7.3.5 Byte Enable (nBE1/nBE0)

Byte enable signals (nBE1/nBE0) are:

- Valid (asserted or nonasserted according to the incoming system request) from access start to access completion for asynchronous and synchronous single accesses
- Asserted low from access start to access completion for asynchronous and synchronous multiple read accesses
- Valid (asserted or nonasserted, according to the incoming system request) synchronously to each written data for synchronous multiple write accesses.

12.3.3.4.7.4 Error Handling

When an error occurs in the GPMC, the error information is stored in the GPMC_ERR_TYPE register and the address of the illegal access is stored in the GPMC_ERR_ADDRESS register. The GPMC keeps only the first error abort information until the GPMC_ERR_TYPE register is reset. Subsequent accesses that cause errors are not logged until the error is cleared by hardware with the GPMC_ERR_TYPE[0] ERRORVALID bit.

- ERRORNOTSUPPADD occurs when an incoming system request address decoding does not match any valid chip-select region, or if two chip-select regions are defined as overlapped, or if a register file access is tried outside the valid address range of 1KB.

- ERRORNOTSUPPMCMD occurs when an unsupported command request is decoded at the interconnect interface.
- ERRORTIMEOUT: A time-out mechanism prevents the system from hanging. The start value of the 9-bit time-out counter is defined in the GPMC_TIMEOUT_CONTROL register and enabled with the GPMC_TIMEOUT_CONTROL[0] TIMEOUTENABLE bit. When enabled, the counter starts at start-cycle time until it reaches 0 and data is not responded to from memory, and then a time-out error occurs. When data are sent from memory, this counter is reset to its start value. With multiple accesses (asynchronous page mode or synchronous burst mode), the counter is reset to its start value for each data access within the burst.

The GPMC does not generate interrupts on these errors. An interrupt generation is handled at interconnect level.

12.3.3.4.8 GPMC Timing Setting

The GPMC offers maximum flexibility to support various access protocols. Most of the timing parameters of the protocol access used by the GPMC to communicate with attached memories or devices are programmable on a chip-select basis. Assertion and deassertion times of control signals are defined to match the attached memory or device timing specifications and to get maximum performance during accesses. For more information about GPMC_CLKOUT and GPMC_FCLK, see Section 12.3.3.4.8.6 , *GPMC_CLKOUT*.

Note

In the following sections, the start access time refers to the time at which the access begins.

12.3.3.4.8.1 Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME)

The GPMC_CONFIG5_i[4-0] RDCYCLETIME and GPMC_CONFIG5_i[12-8] WRCYCLETIME bit fields (where i = 0 to 3) define the address bus and byte-enable valid time for read and write accesses. To ensure a correct duty cycle of GPMC output clock between accesses, RDCYCLETIME and WRCYCLETIME are expressed in GPMC_FCLK cycles and must be multiples of the GPMC output clock cycle. The RDCYCLETIME and WRCYCLETIME bit fields can be set with a granularity of 1 or 2 through the GPMC_CONFIG5_i[4] TIMEPARAGRANULARITY bit.

When RDCYCLETIME or WRCYCLETIME completes, if they are not already deasserted, all control signals (nCS, nADV/ALE, nOE/RE, nWE, and BE0/CLE) are deasserted to their reset values, regardless of their deassertion time parameters.

An exception to this forced deassertion occurs when a pipelined request to the same chip-select or to a different chip-select is pending. In such a case, it is not necessary to deassert a control signal with deassertion time parameters equal to the cycle-time parameter. This exception to forced deassertion prevents any unnecessary glitches. This requirement also applies to BE signals, thus avoiding an unnecessary BE glitch transition when pipelining requests.

Note

All control signals (CS, ADV#/ALE, BE0#/CLE, WE#, and GPMC output clock) are kept inactive (ADV#/ALE, BE0#/CLE, and GPMC output clock at low level; and CS, OE#/RE, and WE at high level) during the idle GPMC_FCLK cycles.

If no inactive cycles are required between successive accesses to the same chip-select or a different chip-select (GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN = 0 or GPMC_CONFIG6_i[6] CYCLE2CYCLEDIFFCSEN = 0, where i = 0 to 3), and if assertion-time parameters associated with the pipelined access are equal to 0, asserted control signals (nCS, nADV/ALE, nBE0/CLE, nWE, and nOE/RE) are kept asserted. This applies to any read/write to read/write access combination.

If inactive cycles are inserted between successive accesses (that is, CYCLE2CYCLESAMECSEN = 1 or CYCLE2CYCLEDIFFCSEN = 1), the control signals are forced to their respective default reset values for the number of GPMC_FCLK cycles defined in CYCLE2CYCLEDELAY.

12.3.3.4.8.2 nCS: Chip-Select Signal Control Assertion/Deassertion Time (CSONTIME / CSRDOFFTIME / CSWROFFTIME / CSEXTRADELAY)

The GPMC_CONFIG2_i[3-0] CSONTIME bit field (where i = 0 to 3) defines the nCS signal-assertion time relative to the start access time. It is common for read and write accesses.

The GPMC_CONFIG2_i[12-8] CSRDOFFTIME (read access) and GPMC_CONFIG2_i[20-16] CSWROFFTIME (write access) bit fields define the nCS signal deassertion time relative to start access time.

The CSONTIME, CSRDOFFTIME, and CSWROFFTIME parameters apply to synchronous and asynchronous modes. CSONTIME can be used to control an address and byte-enable setup time before chip-select assertion. CSRDOFFTIME and CSWROFFTIME can be used to control an address and byte-enable hold time after chip-select deassertion.

nCS signal transitions, as controlled through CSONTIME, CSRDOFFTIME, and CSWROFFTIME, can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG2_i[7] CSEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on the nCS assertion and deassertion time to ensure proper setup and hold time relative to GPMC output clock. CSEXTRADELAY is especially useful in configurations where GPMC output clock and GPMC_FCLK have the same frequency, but it can also be used for all GPMC configurations. If enabled, CSEXTRADELAY applies to all parameters that control nCS transitions.

The CSEXTRADELAY bit must be used carefully to avoid control signal overlap between successive accesses to different chip-selects. This implies the need to program the RDCYCLETIME and WRCYCLETIME bit fields to be greater than the nCS signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

12.3.3.4.8.3 nADV/ALE: Address Valid/Address Latch Enable Signal Control Assertion/Deassertion Time (ADVONTIME / ADVRDOFFTIME / ADVWROFFTIME / ADVEXTRADELAY/ADVAADMUXONTIME/ADVAADMUXRDOFFTIME/ADVAADMUXWROFFTIME)

The GPMC_CONFIG3_i[3-0] ADVONTIME field (where i = 0 to 3) defines the nADV/ALE signal-assertion time relative to start access time. It is common to read and write accesses.

The GPMC_CONFIG3_i[12-8] ADVRDOFFTIME (read access) and GPMC_CONFIG3_i[20-16] ADVWROFFTIME (write access) bit fields define the nADV/ALE signal-deassertion time relative to start access time.

ADVONTIME can be used to control an address and byte-enable valid setup time control before nADV/ALE assertion. ADVRDOFFTIME and ADVWROFFTIME can be used to control an address and byte-enable valid hold time control after nADV/ALE deassertion. ADVRDOFFTIME and ADVWROFFTIME apply to synchronous and asynchronous modes.

The nADV/ALE signal transitions as controlled through ADVONTIME, ADVRDOFFTIME, and ADVWROFFTIME can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG3_i[7] ADVEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on nADV/ALE assertion and deassertion time to ensure proper setup and hold time relative to GPMC output clock. The ADVEXTRADELAY configuration parameter is especially useful in configurations where GPMC output clock and GPMC_FCLK have the same frequency, but can be used for all GPMC configurations. If enabled, ADVEXTRADELAY applies to all parameters controlling nADV/ALE transitions.

ADVEXTRADELAY must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the RDCYCLETIME and WRCYCLETIME bit fields to be greater than nADV/ALE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

GPMC_CONFIG3_i[6-4] ADVAADMUXONTIME, GPMC_CONFIG3_i[26-24] ADVAADMUXRDOFFTIME, and GPMC_CONFIG3_i[30-28] ADVAADMUXWROFFTIME parameters have the same functions as ADVONTIME, ADVRDOFFTIME, and ADVWROFFTIME, but apply to the first address phase in the AAD-multiplexed protocol. The user must ensure that ADVAADMUXxxOFFTIME is programmed to a value less than or equal to ADVxxOFFTIME. Functionality in AAD-multiplexed mode is undefined if the settings do not comply with this requirement. ADVAADMUXxxOFFTIME can be programmed to the same value as ADVONTIME if no high nADV pulse is needed between the two AAD-multiplexed address phases, which is the typical case in synchronous mode. In this configuration, nADV is kept low until it reaches the correct ADVxxOFFTIME.

For more information about the use of ADVONTIME, ADVRDOFFTIME, ADVWROFFTIME, and ADVAADMUXRDOFFTIME and ADVAADMUXWROFFTIME for command latch enable (CLE) and address latch enable (ALE) use for a NAND flash interface, see Section 12.3.3.4.11 , *GPMC NAND Access Description*.

12.3.3.4.8.4 nOE/nRE: Output Enable/Read Enable Signal Control Assertion/Deassertion Time (OEONTIME / OEOFFTIME / OEEXTRADELAY / OEAADMUXONTIME / OEAADMUXOFFTIME)

The GPMC_CONFIG4_i[3-0] OEONTIME bit field (where i = 0 to 3) defines the nOE/nRE signal assertion time relative to start access time. It applies only to read accesses.

The GPMC_CONFIG4_i[12-8] OEOFFTIME bit field defines the nOE/nRE signal deassertion time relative to start access time. It applies only to read accesses. nOE/nRE is not asserted during a write cycle.

The OEONTIME, OEOFFTIME, OEAADMUXONTIME, and OEAADMUXOFFTIME parameters apply to synchronous and asynchronous modes. OEONTIME can be used to control an address and byte enable valid setup time control before nOE/nRE assertion. OEOFFTIME can be used to control an address and byte-enable valid hold time control after nOE/nRE assertion.

The OEAADMUXONTIME and OEAADMUXOFFTIME parameters have the same functions as OEONTIME and OEOFFTIME, but apply to the first OE assertion in the AAD-multiplexed protocol for a read phase, or to the only OE assertion for a write phase. The user must ensure that OEAADMUXOFFTIME is programmed to a value less than OEONTIME. Functionality in AAD-multiplexed mode is undefined if the settings do not comply with this requirement. OEAADMUXOFFTIME must never be equal to OEONTIME because the AAD-multiplexed protocol requires a second address phase with the nOE signal deasserted before nOE can be asserted again to define a read command.

The nOE/RE signal transitions as controlled through OEONTIME, OEOFFTIME, OEAADMUXONTIME, and OEAADMUXOFFTIME can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG4_i[7] OEEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on the nOE/RE assertion and deassertion time to ensure proper setup and hold time relative to GPMC output clock. If enabled, OEEXTRADELAY applies to all parameters controlling nOE/nRE transitions.

OEEXTRADELAY must be used carefully, to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program RDCYCLETIME and WRCYCLETIME to be greater than the nOE/RE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

Note

When the GPMC generates a read access to an address-/data-multiplexed device, it drives the address bus until nOE assertion time.

12.3.3.4.8.5 nWE: Write Enable Signal Control Assertion/Deassertion Time (WEONTIME / WEOFFTIME / WEEXTRADELAY)

The GPMC_CONFIG4_i[19-16] WEONTIME bit field (where i = 0 to 3) defines the nWE signal-assertion time relative to start access time. The GPMC_CONFIG4_i[28-24] WEOFFTIME bit field defines the nWE signal-deassertion time relative to start access time. These bit fields apply only to write accesses. nWE is not asserted during a read cycle.

WEONTIME can be used to control an address and byte-enable valid setup time control before nWE assertion. WEOFFTIME can be used to control an address and byte-enable valid hold time control after nWE assertion.

nWE signal transitions as controlled through WEONTIME, and WEOFFTIME can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG4_i[23] WEEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on nWE assertion and deassertion time to ensure proper setup and hold time relative to GPMC output clock. If enabled, WEEXTRADELAY applies to all parameters controlling nWE transitions.

The WEEXTRADELAY bit must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the WRCYCLETIME bit field to be greater than the nWE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

12.3.3.4.8.6 GPMC_CLKOUT

The GPMC output clock generated for external synchronous memory or device is GPMC_CLKOUT.

- The GPMC_CLKOUT clock frequency is the GPMC_FCLK functional clock frequency divided by 1, 2, 3, or 4, depending on the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field (where i = 0 to 3), with a guaranteed 50-percent duty cycle. For information about the duty cycle error, see the device-specific Datasheet.
- The GPMC_CLKOUT clock is activated only when the access in progress is defined as synchronous (read or write access).
- The GPMC_CONFIG1_i[26-25] CLKACTIVATIONTIME bit field (where i = 0 to 3) defines the number of GPMC_FCLK cycles from start access time to GPMC_CLKOUT activation.
- The GPMC_CLKOUT clock is stopped when cycle time completes and is asserted low between accesses.
- The GPMC_CLKOUT clock is kept low when access is defined as asynchronous.

CAUTION

When the cycle time completes, the GPMC_CLKOUT may be high because of the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field. To ensure correct stoppage of the GPMC_CLKOUT clock within the required 50-percent duty cycle, the user must extend the RDCYCLETIME or WRCYCLETIME value.

Note

To ensure a correct external clock cycle, the following rules must be applied:

- (RDCYCLETIME - CLKACTIVATIONTIME) must be a multiple of (GPMCFCLKDIVIDER + 1).
- The PAGEBURSTACCESSTIME value must be a multiple of (GPMCFCLKDIVIDER + 1).

12.3.3.4.8.7 GPMC Output Clock and Control Signals Setup and Hold

Control-signal transition (assertion and deassertion) setup and hold values with respect to the GPMC output clock edge can be controlled in the following ways:

- For the GPMC output clock signal, the GPMC_CONFIG1_i[26-25] CLKACTIVATIONTIME bit field (where i = 0 to 3) allows setup and hold control of control-signal assertion time.
- The use of a divided GPMC output clock allows setup and hold control of the control-signal assertion and deassertion times.
- When the GPMC output clock runs at the GPMC_FCLK frequency so that GPMC output clock edge and control-signal transitions refer to the same GPMC_FCLK edge, the control-signal transitions can be delayed by a half-GPMC_FCLK period to provide minimum setup and hold times. This half-GPMC_FCLK delay is enabled with the CSEXTRADELAY, ADVEXTRADELAY, OEEXTRADELAY, or WEEXTRADELAY parameter. This delay must be used carefully to prevent control-signal overlap between successive accesses to different chip-selects. This implies that the RDCYCLETIME and WRCYCLETIME are greater than the last control-signal deassertion time, including the extra half-GPMC_FCLK cycle.

12.3.3.4.8.8 Access Time (RDACCESSTIME / WRACCESSTIME)

The read/write access time durations can be programmed independently through the GPMC_CONFIG5_i[20-16] RDACCESSTIME and GPMC_CONFIG6_i[28-24] WRACCESSTIME bit fields (where i = 0 to 3). This allows nOE and GPMC data-capture timing parameters to be independent of nWE and memory device data capture timing parameters. The RDACCESSTIME and WRACCESSTIME bit fields can be set with a granularity of 1 or 2 through the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit.

12.3.3.4.8.8.1 Access Time on Read Access

In asynchronous read mode, for single and paged accesses, the GPMC_CONFIG5_i[20-16] RDACCESSTIME bit field (where i = 0 to 3) defines the number of GPMC_FCLK cycles from start access time to the GPMC_FCLK rising edge used for the first data capture. RDACCESSTIME must be programmed to the rounded greater value (in GPMC_FCLK cycles) of the read access time of the attached memory device.

In synchronous read mode, for single or burst accesses, RDACCESSTIME defines the number of GPMC_FCLK cycles from the start access time to the GPMC_FCLK rising edge corresponding to the GPMC output clock rising edge used for the first data capture.

GPMC output clock, which is sent to the memory device for synchronization with the GPMC controller, is internally retimed to correctly latch the returned data. The GPMC_CONFIG5_i[4-0] RDCYCLETIME bit field must be greater than RDACCESSTIME to let the GPMC latch the last return data using the internally retimed GPMC output clock.

The external WAIT signal can be used in conjunction with RDACCESSTIME to control the effective GPMC data-capture GPMC_FCLK edge on read access in asynchronous and synchronous modes. For more information about wait monitoring, see Section 12.3.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

12.3.3.4.8.8.2 Access Time on Write Access

In asynchronous write mode, the GPMC_CONFIG6_i[28-24] WRACCESSTIME timing parameter is not used to define the effective write access time. Instead, it is used as a wait invalid timing window and must be set to a correct value so that the GPMC_WAIT pin is at a valid state two GPMC output clock cycles before WRACCESSTIME completes. For more information about wait monitoring, see Section 12.3.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

In synchronous write mode, for single or burst accesses, WRACCESSTIME defines the number of GPMC_FCLK cycles from the start access time to the GPMC output clock rising edge used by the memory device for the first data capture.

The external WAIT signal can be used in conjunction with WRACCESSTIME to control the effective memory device data-capture GPMC output clock edge for a synchronous write access. For more information about wait monitoring, see Section 12.3.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

12.3.3.4.8.9 Page Burst Access Time (PAGEBURSTACCESSTIME)

The GPMC_CONFIG5_i[27-24] PAGEBURSTACCESSTIME bit field (where i = 0 to 3) can be set with a granularity of 1 or 2 through the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit.

12.3.3.4.8.9.1 Page Burst Access Time on Read Access

In asynchronous page read mode, the delay between successive word captures in a page is controlled through the PAGEBURSTACCESSTIME bit field. The PAGEBURSTACCESSTIME parameter must be programmed to the rounded greater value (in GPMC_FCLK cycles) of the read access time of the attached device.

In synchronous burst read mode, the delay between successive word captures in a burst is controlled through the PAGEBURSTACCESSTIME bit field.

The external WAIT signal can be used in conjunction with PAGEBURSTACCESSTIME to control the effective GPMC data-capture GPMC_FCLK edge on read access. For more information about wait monitoring, see Section 12.3.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

12.3.3.4.8.9.2 Page Burst Access Time on Write Access

Asynchronous page write mode is not supported. PAGEBURSTACCESSTIME is irrelevant in this case.

In synchronous burst write mode, PAGEBURSTACCESSTIME controls the delay between successive memory device word captures in a burst.

The external WAIT signal can be used in conjunction with PAGEBURSTACCESSTIME to control the effective memory device data capture GPMC output clock edge in synchronous write mode. For more information about wait monitoring, see Section 12.3.3.4.7.3.1 , *WAIT Pin Monitoring Control*.

12.3.3.4.8.10 Bus Keeping Support

At the end cycle time of a read access, if no other access is pending, the GPMC drives the bus with the last data read after RDCYCLETIME completes to prevent bus floating and reduce power consumption.

After a write access, if no other access is pending, the GPMC keeps driving the data bus after WRCYCLETIME completes with the same data to prevent bus floating and power consumption.

12.3.3.4.9 GPMC NOR Access Description

For each chip-select configuration, the read access can be specified as asynchronous or synchronous access through the GPMC_CONFIG1_i[29] READTYPE bit (where i = 0 to 3). For each chip-select configuration, the write access can be specified as synchronous or asynchronous access through the GPMC_CONFIG1_i[27] WRITETYPE bit where (i = 0 to 3).

Asynchronous and synchronous read and write access time and related control signals are controlled through timing parameters that refer to GPMC_FCLK. The primary difference of synchronous mode is the availability of a configurable clock interface to control the external device. Synchronous mode also affects data-capture and wait-pin monitoring schemes in read access.

For more information about asynchronous and synchronous access, see the descriptions of GPMC output clock (CLK), RdAccessTime, WrAccessTime, and WAIT pin monitoring.

For more information about timing-parameter settings, see the sample timing diagrams in this chapter.

Note

The address bus and nBE[1-0] are fixed for the duration of a synchronous burst read access, but they are updated for each byte of an asynchronous page-read access.

12.3.3.4.9.1 Asynchronous Access Description

This section describes:

- Asynchronous single-read operation on an address/data multiplexed device
- Asynchronous single write operation on an address/data-multiplexed device
- Asynchronous single read operation on an AAD-multiplexed device
- Asynchronous single write operation on an AAD-multiplexed device
- Asynchronous multiple (page) read operation on a non-multiplexed device

In asynchronous operations GPMC output clock is not provided outside the GPMC and is kept low.

12.3.3.4.9.1.1 Access on Address/Data Multiplexed Devices

12.3.3.4.9.1.1.1 Asynchronous Single-Read Operation on an Address/Data Multiplexed Device

Figure 12-174 shows an asynchronous single read operation on an address/data-multiplexed device.

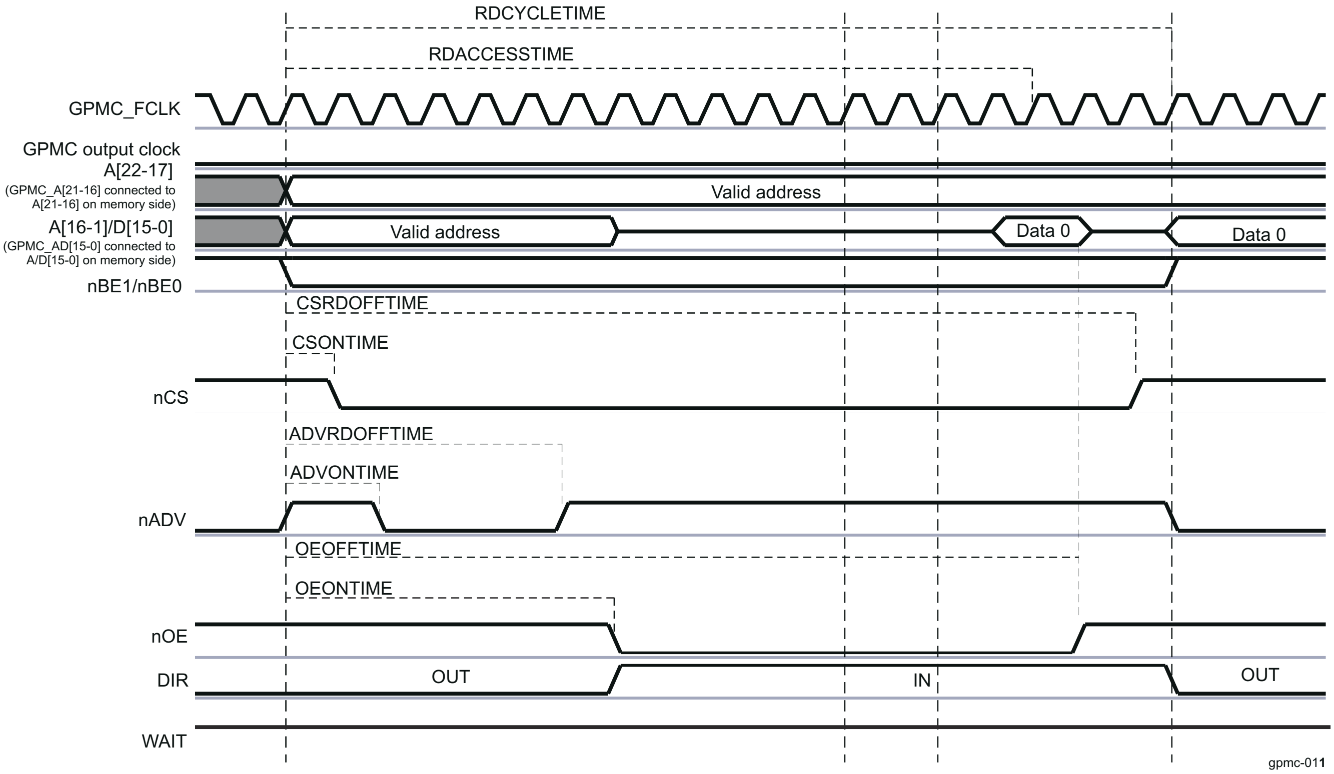

Figure 12-174. Asynchronous Single Read on an Address/Data-Multiplexed Device

For formulas to calculate timing parameters, see Section 12.3.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-293 lists the timing bit fields to set up to configure the GPMC in asynchronous single-read mode.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 12.3.3.4.7.2.3 , *Address/Data-Multiplexing Interface*.

Address bits (A[16-1] from a GPMC perspective, A[15-0] from an external device perspective) are placed on the address/data bus, and the remaining address bits GPMC_A[22-16] are placed on the address bus. The address phase ends at nOE assertion, when the DIR signal goes from OUT to IN.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3-0] CSONTIME bit field. It controls the address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12-8] CSRDOFFTIME bit field. It controls the address hold time from nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[12-8] ADVRDOFFTIME bit field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[3-0] OEONTIME bit field.
  - nOE deassertion time is controlled by the GPMC_CONFIG4_i[12-8] OEOFFTIME bit field.
- Read data is latched when RDACCESSTIME completes. Access time is defined in the GPMC_CONFIG5_i[20-16] RDACCESSTIME bit field.
- Direction signal DIR: DIR goes from OUT to IN at the same time that nOE is asserted.
- The end of the access is defined by the GPMC_CONFIG5_i[4-0] RDCYCLETIME parameter.

In the GPMC, when a 16-bit wide device is attached to the controller, a 32-bit word write access is split into two 16-bit word write accesses. For more information about GPMC access size and type adaptation, see Section 12.3.3.4.9.5 , *System Burst Versus External Device Burst Support*.

Between two successive accesses, if an nCS pulse is needed:

- The GPMC_CONFIG6_i[11-8] CYCLE2CYCLEDELAY bit field can be programmed with the GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN bit enabled.
- The CSWROFFTIME and CSONTIME parameters also allow a chip-select pulse, but this affects all other types of access.

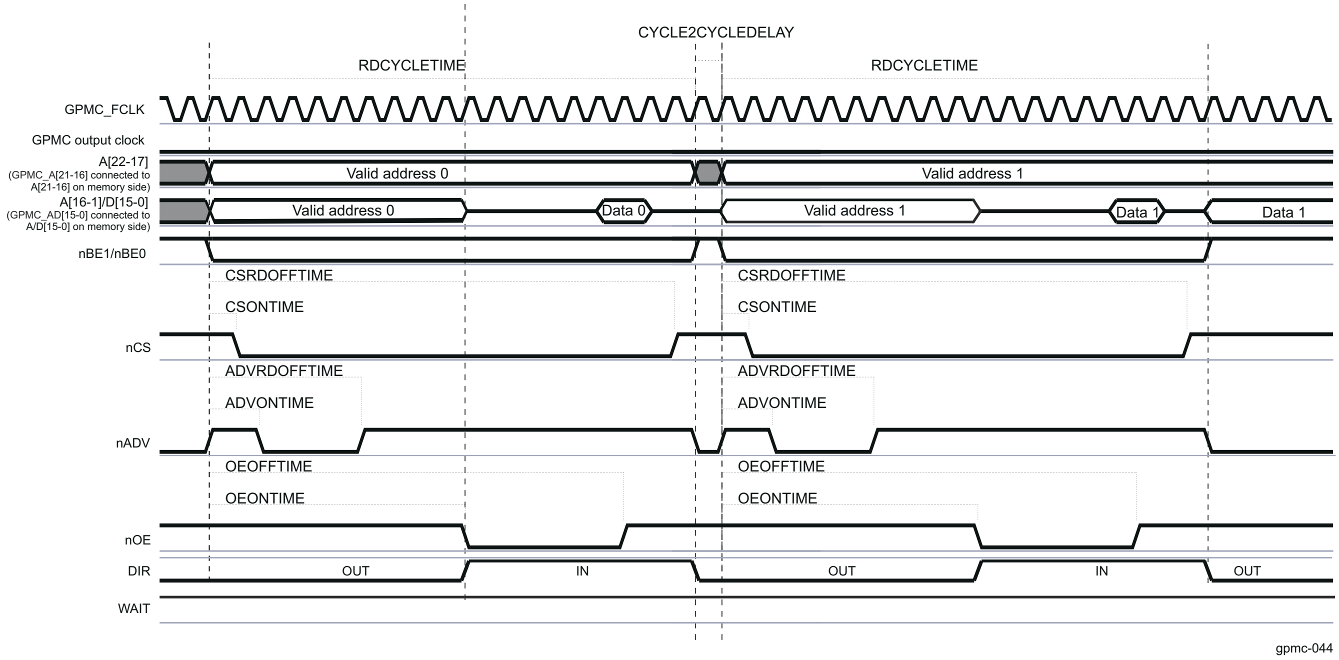

Figure 12-175. Two Asynchronous Single-Read Accesses on an Address/Data-Multiplexed Device (32-Bit Read Split Into 2 x 16-Bit Read)

12.3.3.4.9.1.1.2 Asynchronous Single-Write Operation on an Address/Data-Multiplexed Device

Figure 12-176 shows an asynchronous single-write operation on an address/data-multiplexed device.

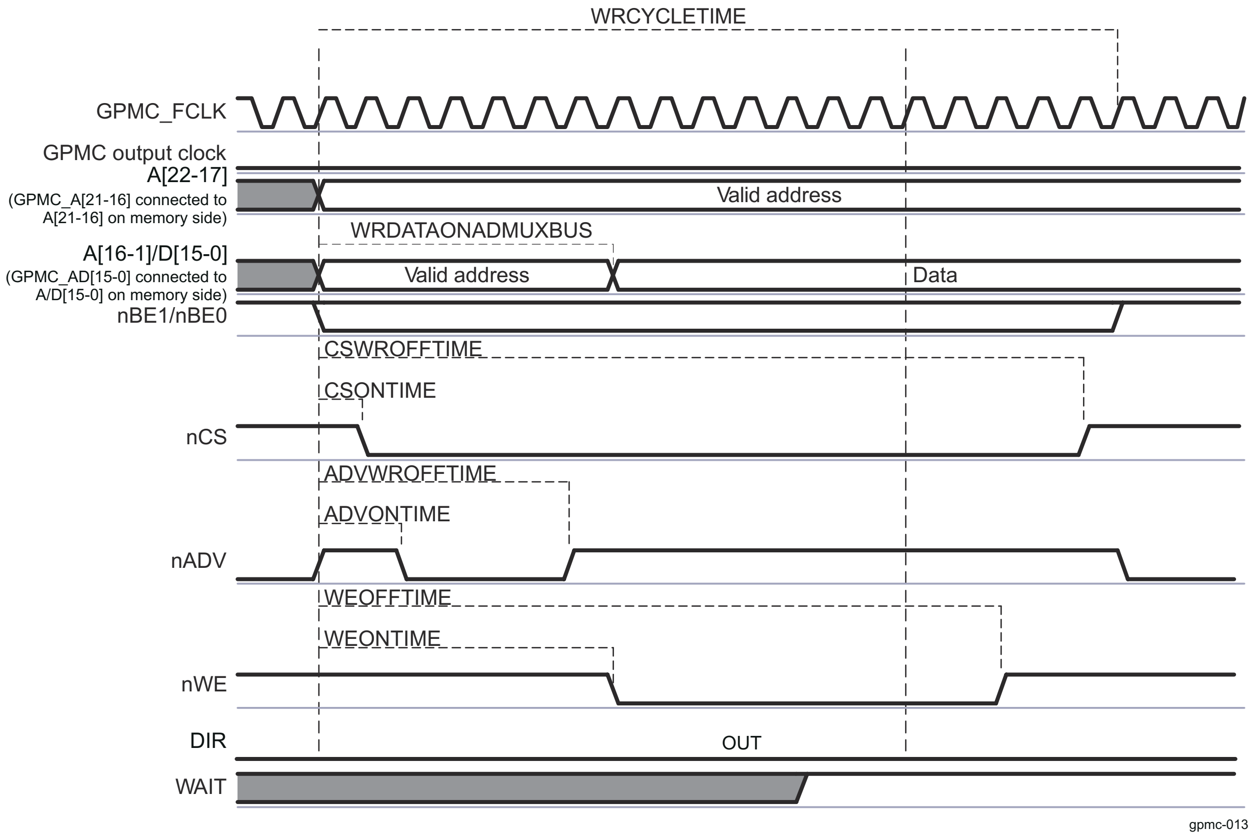

Figure 12-176. Asynchronous Single-Write on an Address/Data-Multiplexed Device

For formulas to calculate timing parameters, see Section 12.3.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-293 lists the timing bit fields to set up to configure the GPMC in asynchronous single-write mode.

When the GPMC generates a write access to an address/data-multiplexed device, it drives the address bus until nWE assertion time. For more information, see Section 12.3.3.4.7.2.3 , *Address/Data-Multiplexing Interface*.

The nCS and nADV signals are controlled in the same way as for a asynchronous single-read operation on an address/data-multiplexed device.

- Write enable signal nWE:
  - nWE assertion indicates a write cycle.
  - nWE assertion time is controlled by the GPMC_CONFIG4_i[19-16] WEONTIME bit field.
  - nWE deassertion time is controlled by the GPMC_CONFIG4_i[28-24] WEOFFTIME bit field.
- Direction signal DIR: DIR signal is OUT during the entire access.
- The end of the access is defined by the GPMC_CONFIG5_i[12-8] WRCYCLETIME parameter.

Address bits A[16-1] (GPMC point of view) are placed on the address/data bus at the start of cycle time, and the remaining address bits A[22-17] are placed on the address bus.

Data is driven on the address/data bus at a GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS time.

Note

Multiple write access in asynchronous mode is not supported. If WRITEMULTIPLE is enabled with WRITETYPE as asynchronous, the GPMC processes single asynchronous accesses.

After a write operation, if no other access (read or write) is pending, the data bus keeps its previous value. See Section 12.3.3.4.8.10 , *Bus Keeping Support*.

12.3.3.4.9.1.1.3 Asynchronous Multiple (Page) Write Operation on an Address/Data-Multiplexed Device

Write multiple (page) access in asynchronous mode is not supported for address/data-multiplexed devices.

If the GPMC_CONFIG1_i[28] WRITEMULTIPLE bit is enabled (0x1) with the GPMC_CONFIG1_i[27] WRITETYPE bit as asynchronous (0x0), the GPMC processes single asynchronous accesses.

For accesses on non-multiplexed devices, see Section 12.3.3.4.9.3 , *Asynchronous and Synchronous Accesses in non-multiplexed Mode*.

12.3.3.4.9.1.2 Access on Address/Address/Data-Multiplexed Devices

12.3.3.4.9.1.2.1 Asynchronous Single Read Operation on an AAD-Multiplexed Device

Figure 12-177 shows an asynchronous single-read operation on an AAD-multiplexed device.

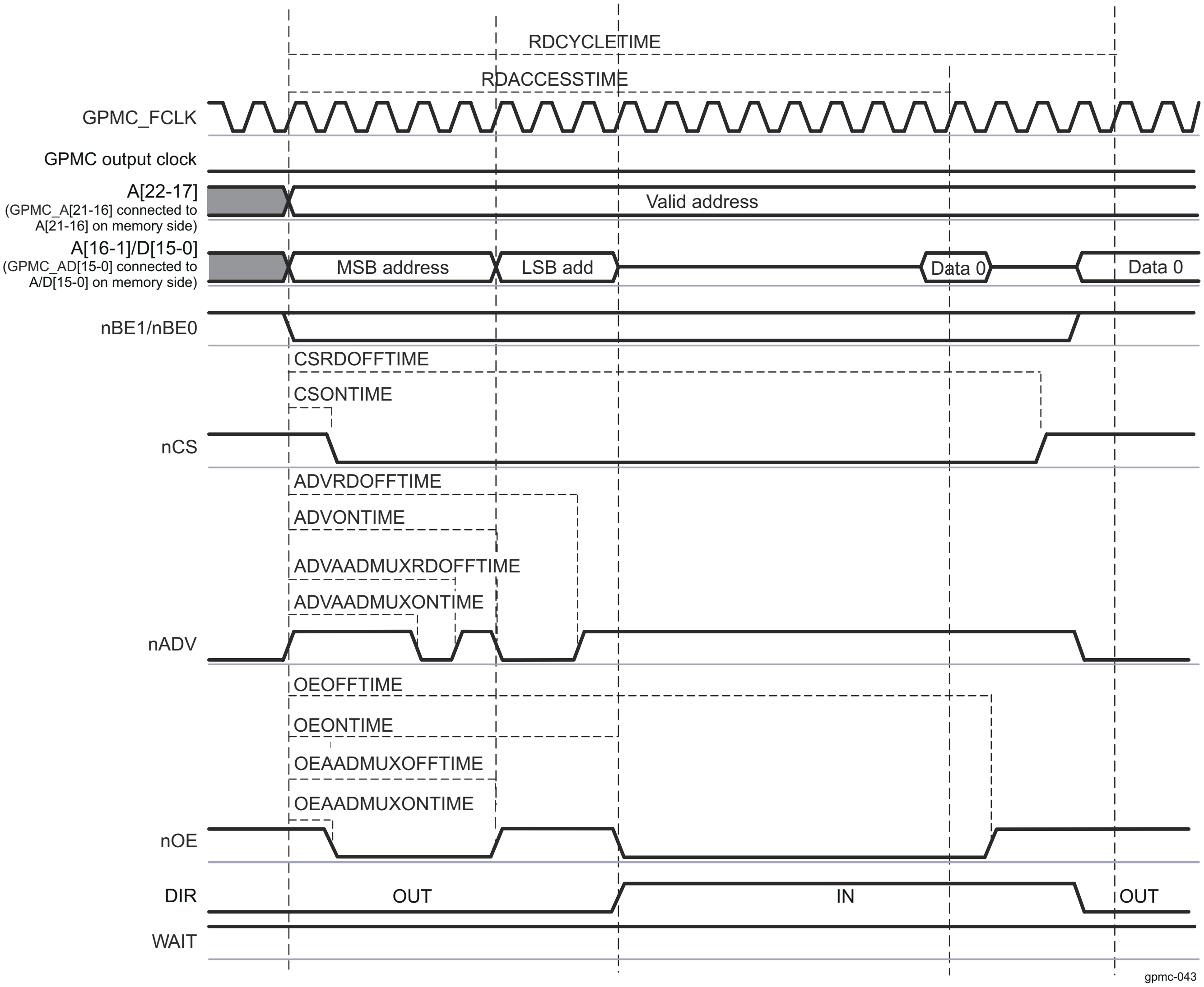

Figure 12-177. Asynchronous Single Read on an AAD-Multiplexed Device

For formulas to calculate timing parameters, see Section 12.3.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-293 lists the timing bit fields to set up to configure the GPMC in asynchronous single write mode.

When the GPMC generates a read access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The first address phase ends at the first nOE deassertion time. The second phase for LSB address is qualified with nOE driven high. The second address phase ends at the second nOE assertion time, when the DIR signal goes from OUT to IN.

The nCS and DIR signals are controlled in the same way as for an asynchronous single-read operation on an address/data-multiplexed device.

- Address valid signal nADV. nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6-4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26-24] ADVAADMUXRDOFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12-8] ADVRDOFFTIME bit field.
- Output Enable signal nOE. nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6-4] OEAADMUXONTIME bit field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG3_i[15-13] OEAADMUXOFFTIME bit field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3-0] OEONTIME bit field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12-8] OEOFFTIME bit field.

12.3.3.4.9.1.2.2 Asynchronous Single-Write Operation on an AAD-Multiplexed Device

Figure 12-178 shows an asynchronous single-write operation on an AAD-multiplexed device.

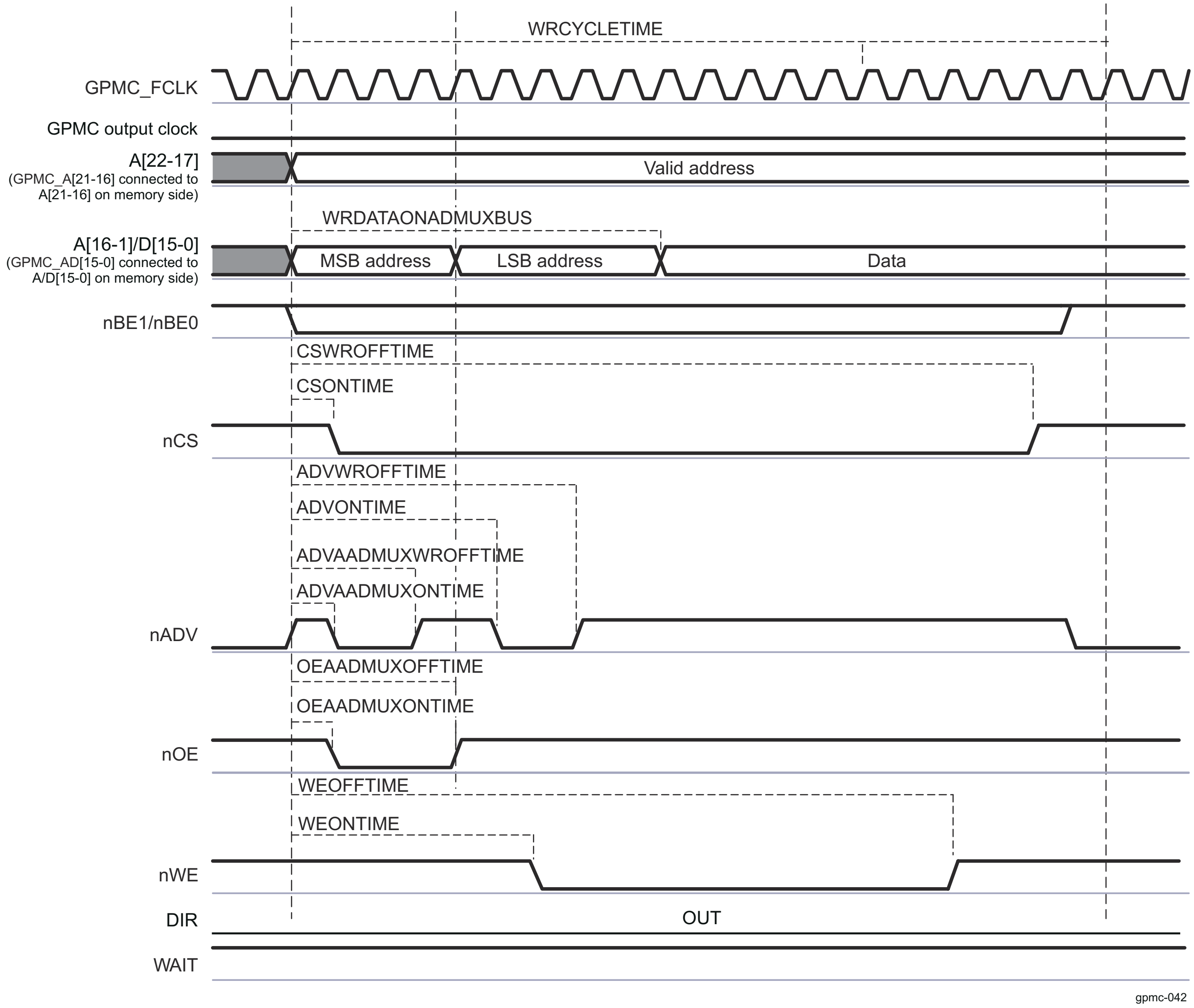

Figure 12-178. Asynchronous Single Write on an AAD-Multiplexed Device

For formulas to calculate timing parameters, see Section 12.3.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-293 lists the timing bit fields to set up to configure the GPMC in asynchronous single-write mode.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, nWE, and DIR signals are controlled in the same way as for an asynchronous single-write operation on an address/data-multiplexed device. See Table 12-284, *NAND Memory Type*.

- Address valid signal nADV is asserted and deasserted twice during a write transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6-4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[30-28] ADVAADMUXWROFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[20-16] ADVWROFFTIME bit field.
- Output enable signal nOE is asserted during the address phase of a write transaction:

  - nOE assertion time is controlled by the GPMC_CONFIG4_i[6-4] OEAADMUXONTIME bit field.
  - nOE deassertion time is controlled by the GPMC_CONFIG3_i[15-13] OEAADMUXOFFTIME bit field.

The address bits for the first address phase are driven onto the data bus until nOE deassertion. Data is driven onto the address/data bus at the clock edge defined by the GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS parameter.

12.3.3.4.9.1.2.3 Asynchronous Multiple (Page) Read Operation on an AAD-Multiplexed Device

Write multiple (page) access in asynchronous mode is not supported for AAD-multiplexed devices.

If the GPMC_CONFIG1_i[28] WRITEMULTIPLE bit is enabled (0x1) with the GPMC_CONFIG1_i[27] WRITETYPE bit as asynchronous (0x0), the GPMC processes single asynchronous accesses.

For accesses on non-multiplexed devices, see Section 12.3.3.4.9.3 , *Asynchronous and Synchronous Accessed in non-multiplexed Mode*.

12.3.3.4.9.2 Synchronous Access Description

This section describes read and write synchronous accesses on address/data-multiplexed devices. All information in this section can be applied to any type of memory (non-multiplexed, address and data-multiplexed, or AAD-multiplexed) with the difference limited to the address phase. For accesses on non-multiplexed devices, see Section 12.3.3.4.9.3 , *Asynchronous and Synchronous Accessed in non-multiplexed Mode*.

In synchronous operations:

- The GPMC_CLKOUT clock is provided outside the GPMC when accessing the memory device.
- The GPMC_CLKOUT clock is derived from the GPMC_FCLK clock using the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field. In the following section i stands for the chip-select number, i = 0 to 3.
- The GPMC_CONFIG1_i[26-25] CLKACTIVATIONTIME bit field specifies that the GPMC_CLKOUT is provided outside the GPMC for 0 to 2 GPMC_FCLK cycles after start access time until RDCYCLETIME or WRCYCLETIME completes.

12.3.3.4.9.2.1 Synchronous Single Read

Figure 12-179 and Figure 12-180 show a synchronous single-read operation with GPMCFCLKDIVIDER equal to 0 and 1, respectively.

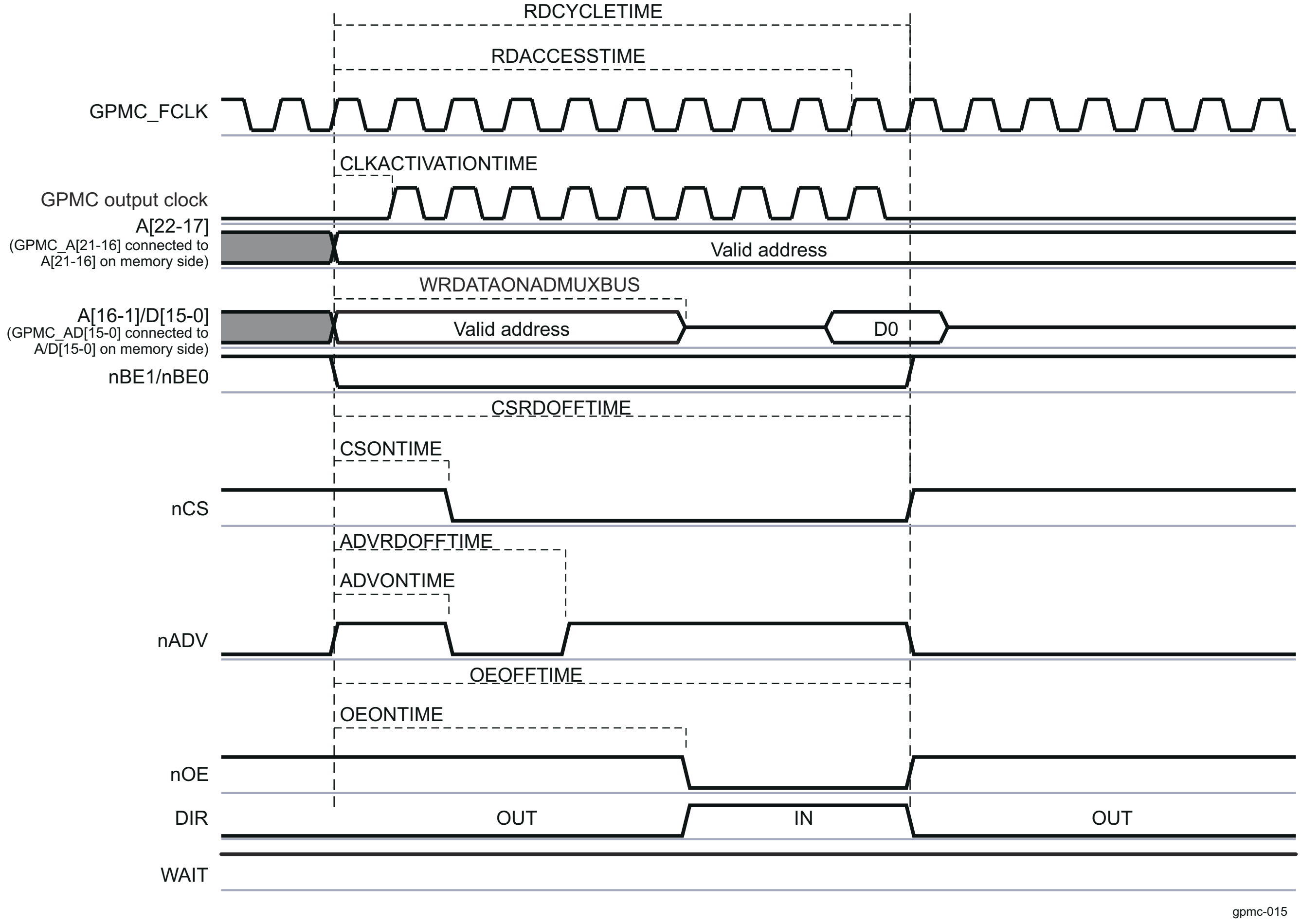

Figure 12-179. Synchronous Single Read (GPMCFCLKDIVIDER = 0)

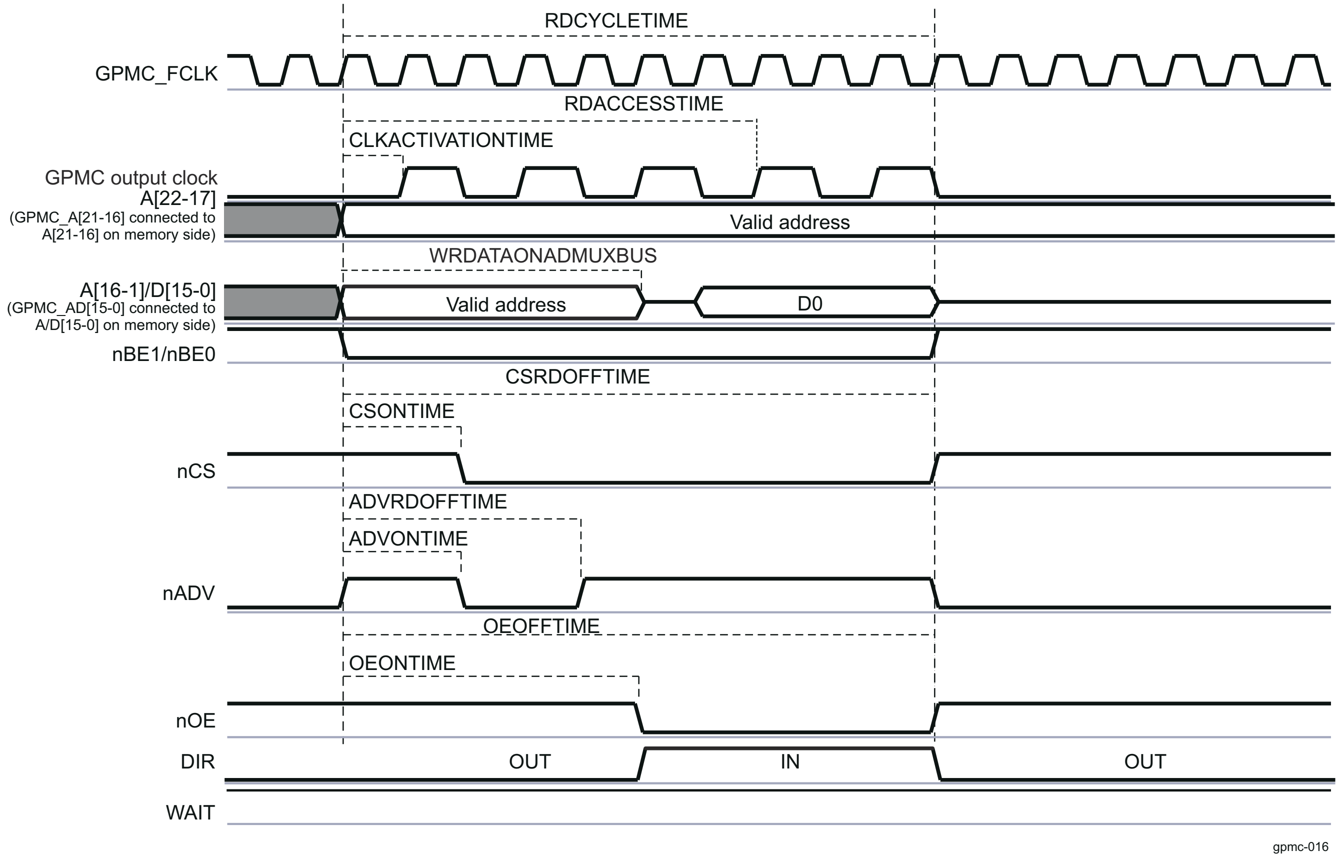

Figure 12-180. Synchronous Single Read (GPMCFCLKDIVIDER = 1)

For formulas to calculate timing parameters, see Section 12.3.3.5.6.1 , *GPMC Timing Parameters Formulas*.

Table 12-293 lists the timing bit fields to set up to configure the GPMC in asynchronous single-read mode.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 12.3.3.4.7.2.3 , *Address/Data-Multiplexing Interface*.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3-0] CSONTIME bit field and ensures address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12-8] CSRDOFFTIME bit field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[12-8] ADVRDOFFTIME bit field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[3-0] OEONTIME bit field.
  - nOE deassertion time is controlled by the GPMC_CONFIG4_i[12-8] OEOFFTIME bit field.
- Initial latency for the first read data is controlled by GPMC_CONFIG5_i[20-16] RDACCESSTIME bit field or by monitoring the WAIT signal.
- Total access time (the GPMC_CONFIG5_i[4-0] RDCYCLETIME bit field) corresponds to RDACCESSTIME plus the address hold time from nCS deassertion, plus time from RDACCESSTIME to CSRDOFFTIME.
- Direction signal DIR: DIR goes from OUT to IN at the same time as nOE assertion.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS and DIR signals are controlled in the same way as for a synchronous single-read operation on an address/data-multiplexed device.

- Address valid signal nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6-4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26-24] ADVAADMUXRDOFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12-8] ADVRDOFFTIME bit field.
- Output Enable signal nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6-4] OEAADMUXONTIME bit field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG3_i[15-13] OEAADMUXOFFTIME bit field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3-0] OEONTIME bit field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12-8] OEOFFTIME bit field.

After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value. See Section 12.3.3.4.8.10 , *Bus Keeping Support*.

12.3.3.4.9.2.2 Synchronous Multiple (Burst) Read (4-, 8-, 16-Word16 Burst With Wraparound Capability)

Figure 12-181 and Figure 12-182 show a synchronous multiple-read operation with GPMCFCLKDivider equal to 0 and 1, respectively.

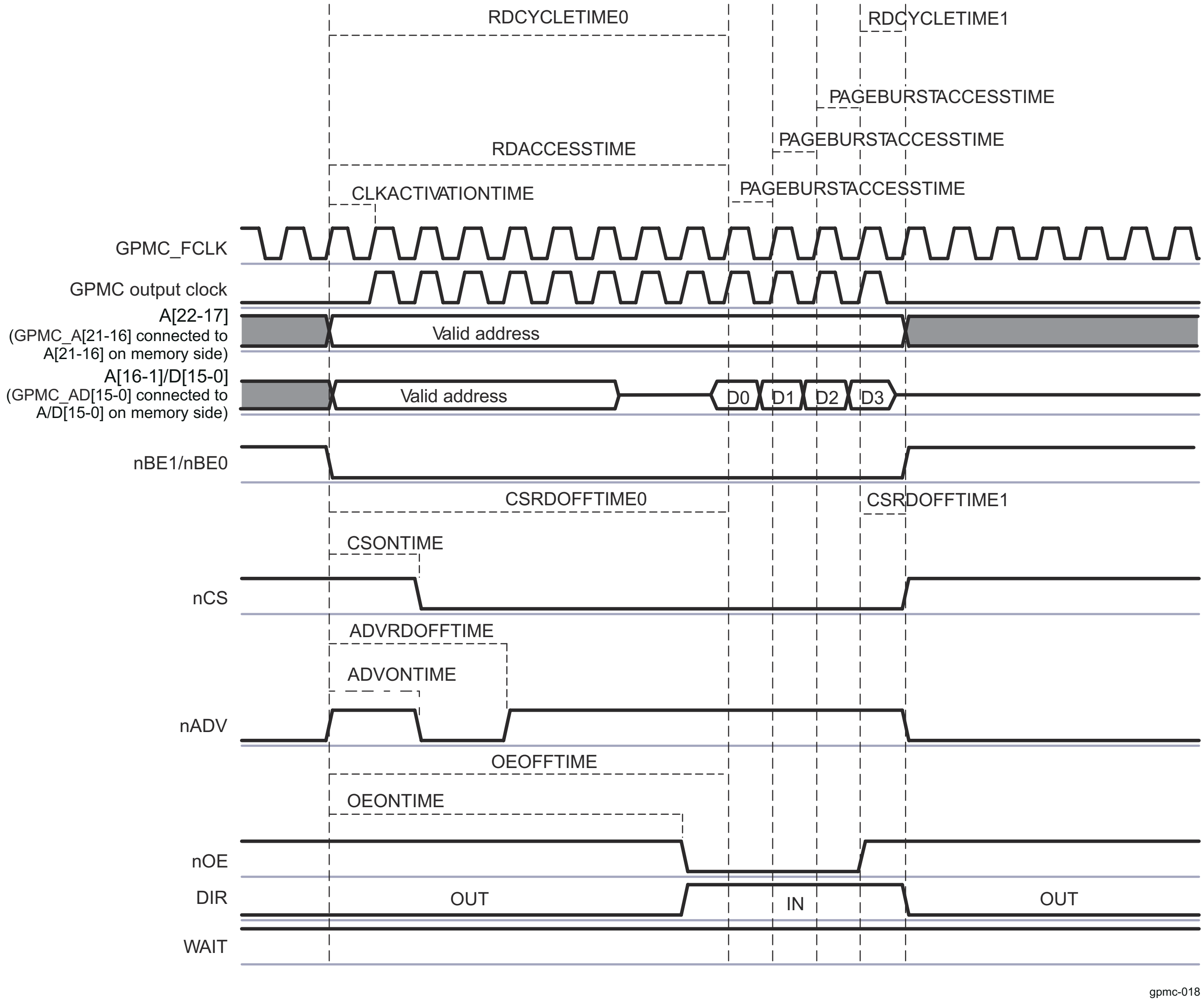

Figure 12-181. Synchronous Multiple (Burst) Read (GPMCFCLKDIVIDER = 0)

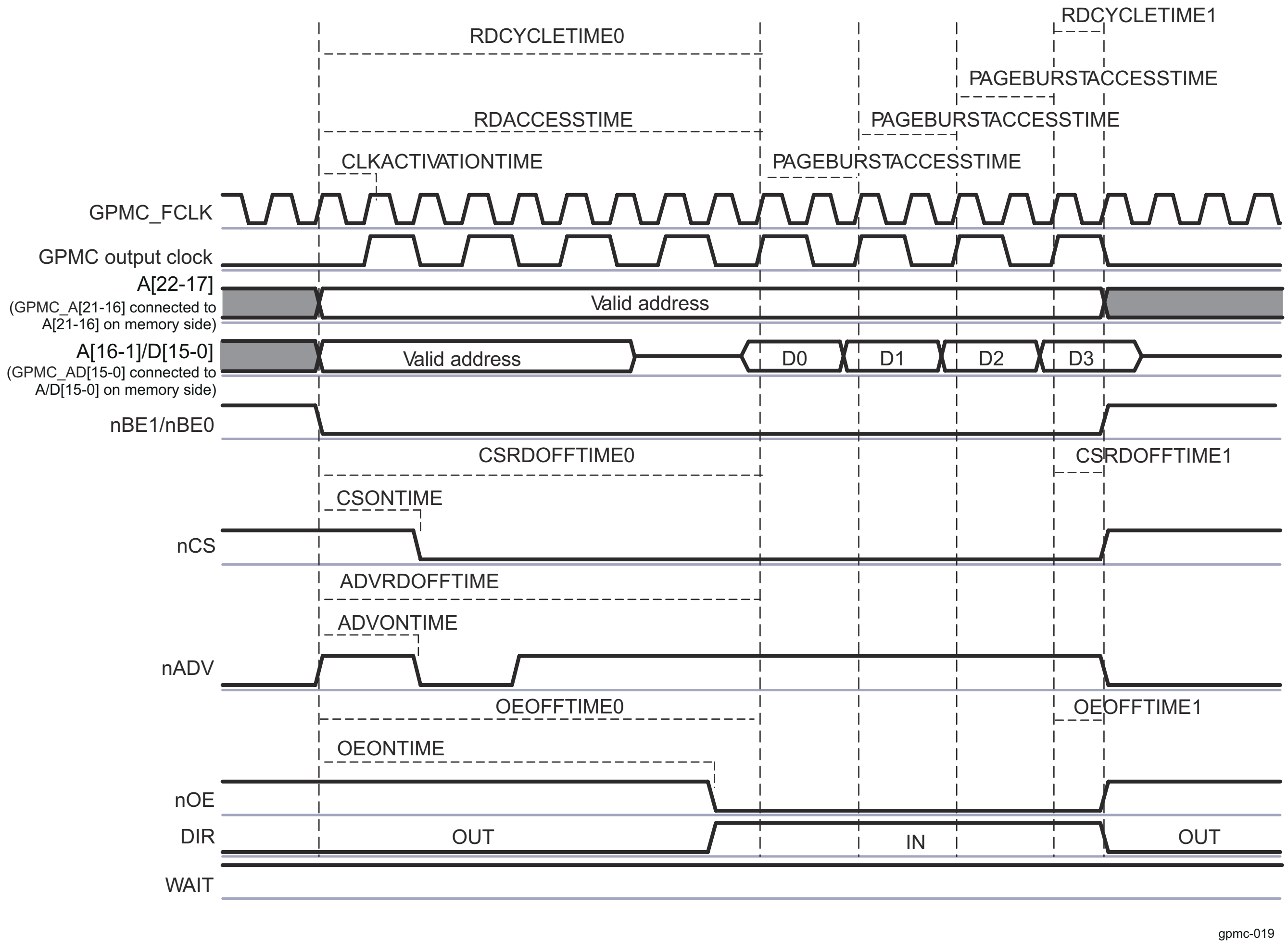

Figure 12-182. Synchronous Multiple (Burst) Read (GPMCFCLKDIVIDER = 1)

When the GPMC_CONFIG5_i[20-16] RDACCESSTIME bit field completes, control-signal timings are frozen during the multiple data transactions, corresponding to the GPMC_CONFIG5_i[27-24] PAGEBURSTACCESSTIME bit field multiplied by the number of remaining data transactions.

The nCS, nADV, nOE, and DIR signals are controlled in the same way as for a synchronous single-read operation. See Table 12-279, *NOR Memory Type*.

Initial latency for the first read data is controlled by RDACCESSTIME or by monitoring the WAIT signal. Successive read data are provided by the memory device every one or two GPMC_CLKOUT cycles. The PAGEBURSTACCESSTIME parameter must be set accordingly with the GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER bit field and the memory-device internal configuration. Depending on the device page length, the GPMC checks the device page crossing during a new burst request and purposely inserts initial latency (of RDACCESSTIME) when required.

Total access time GPMC_CONFIG5_i[4-0] RDCYCLETIME corresponds to RDACCESSTIME plus the address hold time from nCS deassertion. In Figure 12-182, the programmed value of RDCYCLETIME equals RDCYCLETIME0 + RDCYCLETIME1.

After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value. See Section 12.3.3.4.8.10 , *Bus Keeping Support*.

Burst wraparound is enabled through the GPMC_CONFIG1_i[31] WRAPBURST bit and allows a 4-, 8-, or 16-Word16 linear burst access to wrap within its burst-length boundary through the GPMC_CONFIG1_i[24-23] ATTACHEDDEVICEPAGELENGTH bit field.

12.3.3.4.9.2.3 Synchronous Single Write

Burst write mode is used for synchronous single or burst accesses.

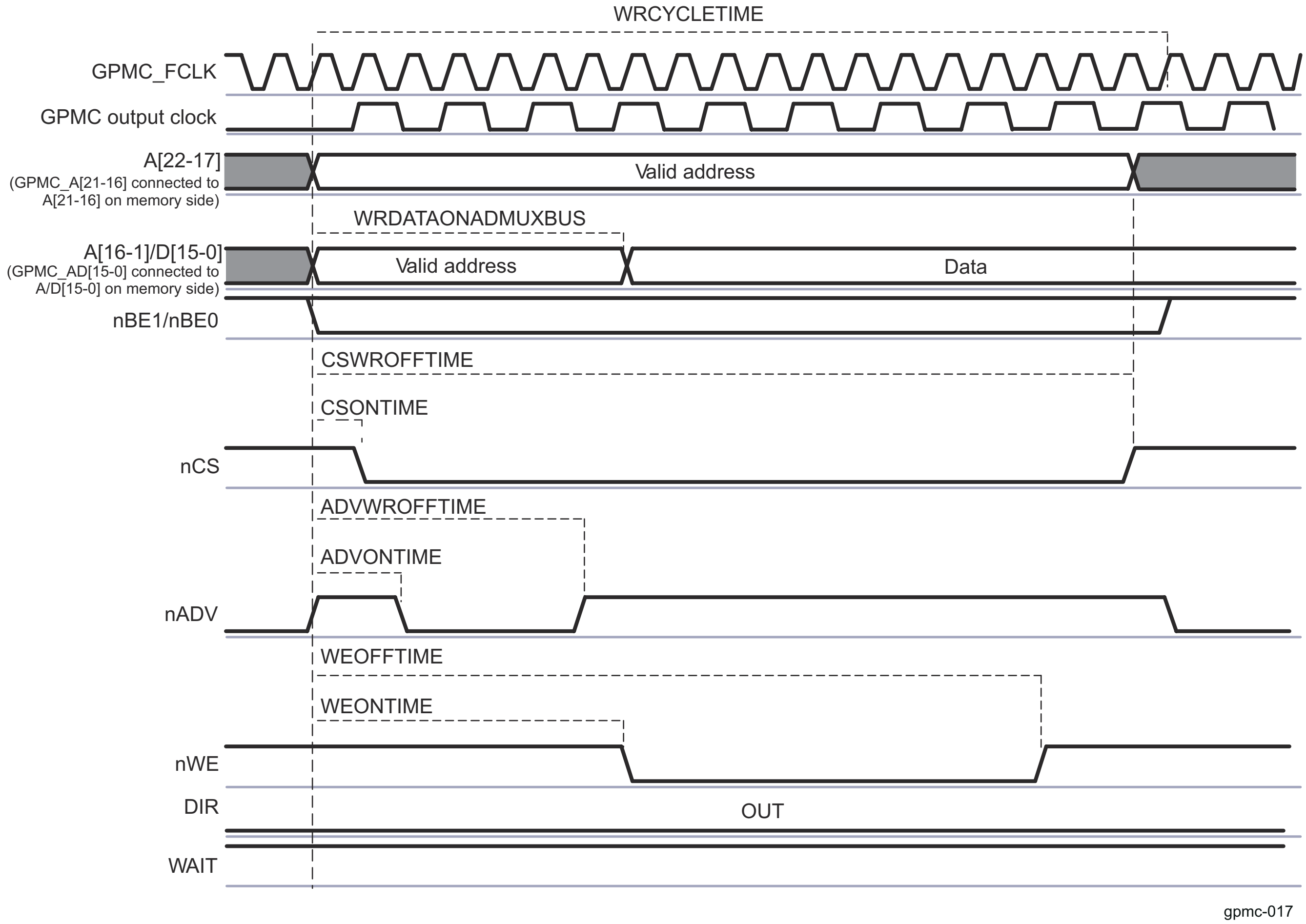

Figure 12-183. Synchronous Single Write on an Address/Data-Multiplexed Device

When the GPMC generates a write access to an address/data-multiplexed device, it drives the data bus (with address bits A[16-1]) until the GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS bit field time. The first data of the burst is driven on the address/data bus at WRDATAONADMUXBUS time.

12.3.3.4.9.2.4 Synchronous Multiple (Burst) Write

Synchronous burst write mode provides synchronous single or consecutive accesses.

Figure 12-184 shows a synchronous burst write access when the chip-select is configured in address/data-multiplexed mode.

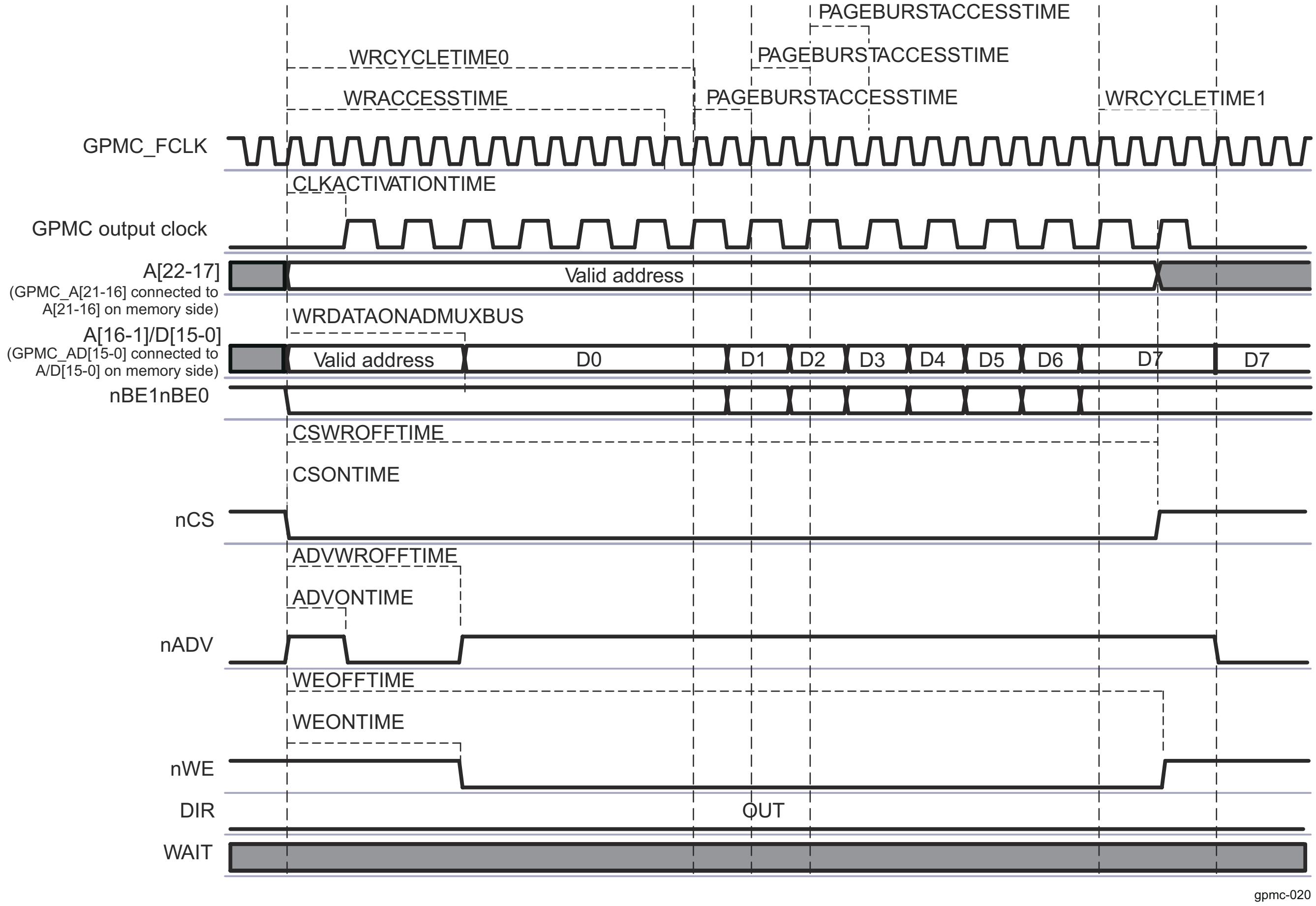

Figure 12-184. Synchronous Multiple Write (Burst Write) in Address/Data-Multiplexed Mode

Figure 12-185 shows the same synchronous burst write access when the chip-select is configured in address/address/data-multiplexed (AAD-multiplexed) mode.

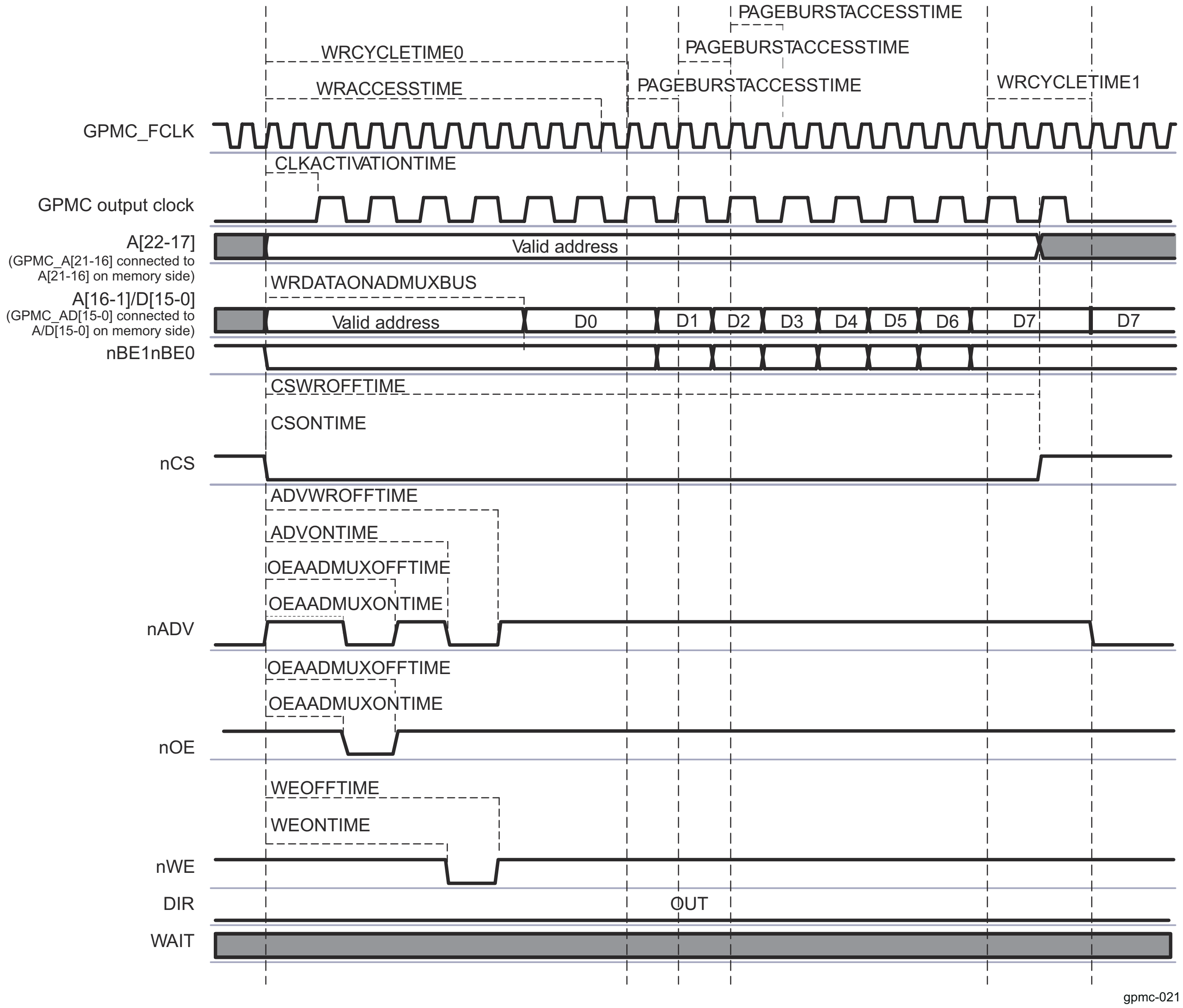

Figure 12-185. Synchronous Multiple Write (Burst Write) in Address/Address/Data-Multiplexed Mode

The first data of the burst is driven on the A/D bus at the GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS bit field.

When WRACCESSTIME completes, control-signal timings are frozen during the multiple data transactions, corresponding to the GPMC_CONFIG5_i[27-24] PAGEBURSTACCESSTIME bit field multiplied by the number of remaining data transactions.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 12.3.3.4.7.2.3 , *Address/Data-Multiplexing Interface*.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3-0] CSONTIME bit field (where i = 0 to 3) and ensures address setup time to nCS assertion.
  - nCS deassertion time controlled by the GPMC_CONFIG2_i[20-16] CSWROFFTIME bit field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[20-16] ADVWROFFTIME bit field.

- Write enable signal nWE:
  - nWE assertion indicates a read cycle.
  - nWE assertion time is controlled by the GPMC_CONFIG4_i[19-16] WEONTIME bit field.
  - nWE deassertion time is controlled by the GPMC_CONFIG4_i[28-24] WEOFFTIME bit field.

Note

The nWE falling edge must not be used to control the time when the burst first data is driven in the address/data bus, because some new devices require the nWE signal to be low during the address phase.

- Direction signal DIR is OUT during the entire access.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, and DIR signals are controlled as previously described.

- Address valid signal nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6-4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26-24] ADVAADMUXRDOFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3-0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12-8] ADVRDOFFTIME bit field.
- Output Enable signal nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6-4] OEAADMUXONTIME bit field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG4_i[15-13] OEAADMUXOFFTIME bit field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3-0] OEONTIME bit field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12-8] OEOFFTIME bit field.

First write data is driven by the GPMC at GPMC_CONFIG6_i[19-16] WRDATAONADMUXBUS, when in address/data-multiplexed configuration. The next write data of the burst is driven on the bus at WRACCESSTIME + 1 during GPMC_CONFIG5_i[27-24] PAGEBURSTACCESSTIME GPMC_FCLK cycles. The last data of the synchronous burst write is driven until GPMC_CONFIG5_i[12-8] WRCYCLETIME completes.

- WRACCESSTIME is defined in the GPMC_CONFIG6_i[28-24] bit field.
- The PAGEBURSTACCESSTIME parameter must be set accordingly with GPMCFCLKDIVIDER and the memory-device internal configuration.

Total access time GPMC_CONFIG5_i[12-8] WRCYCLETIME corresponds to WRACCESSTIME plus the address hold time from nCS deassertion. In Figure 12-184, the programmed value of WRCYCLETIME equals WRCYCLETIME0 + WRCYCLETIME1. WRCYCLETIME0 and WRCYCLETIME1 delays are not actual parameters and are only a graphical representation of the full WRCYCLETIME value.

After a write operation, if no other access (read or write) is pending, the data bus keeps the previous value. See Section 12.3.3.4.8.10 , *Bus Keeping Support*.

12.3.3.4.9.3 Asynchronous and Synchronous Accesses in non-multiplexed Mode

Page mode is available only in non-multiplexed mode.

- Asynchronous single-read operation on a non-multiplexed device
- Asynchronous single-write operation on a non-multiplexed device
- Asynchronous multiple- (page mode) read operation on a non-multiplexed device
- Synchronous operations on a non-multiplexed device

12.3.3.4.9.3.1 Asynchronous Single-Read Operation on non-multiplexed Device

Figure 12-186 shows an asynchronous single-read operation on a non-multiplexed device.

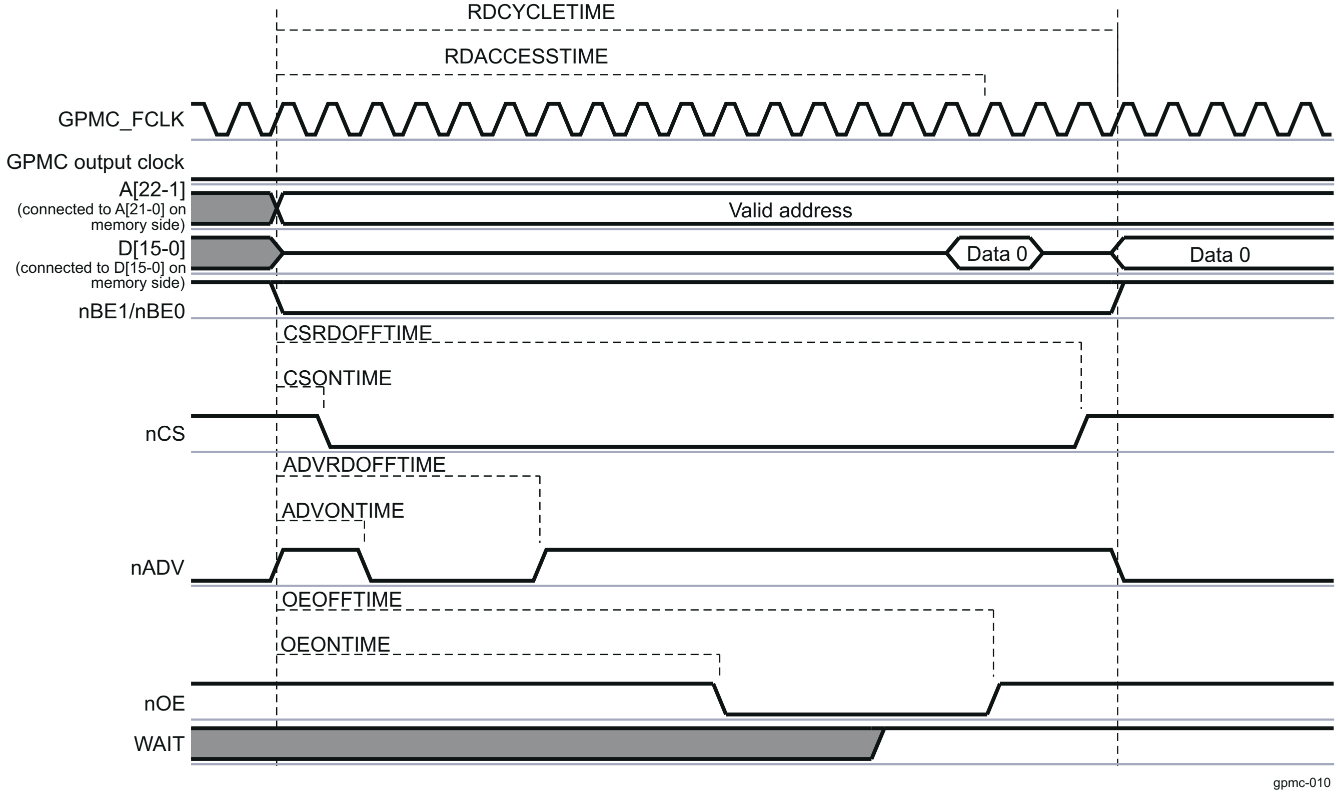

Figure 12-186. Asynchronous Single Read on an Address/Data-non-multiplexed Device

The 22-bit address (For a 16-bit data memory device, hence GPMC A[0] is not necessary to be output) is driven onto the address bus A[22-1] and the 16-bit data is driven onto the data bus D[15-0].

Read data is latched at GPMC_CONFIG1_5[20-16] RDACCESSTIME completion time. The end of the access is defined by the GPMC_CONFIG1_5[4-0] RDCYCLETIME parameter.

The nCS, nADV, nOE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 12-284, *NAND Memory Type*).

12.3.3.4.9.3.2 Asynchronous Single-Write Operation on non-multiplexed Device

Figure 12-187 shows an asynchronous single-write operation on a non-multiplexed device.

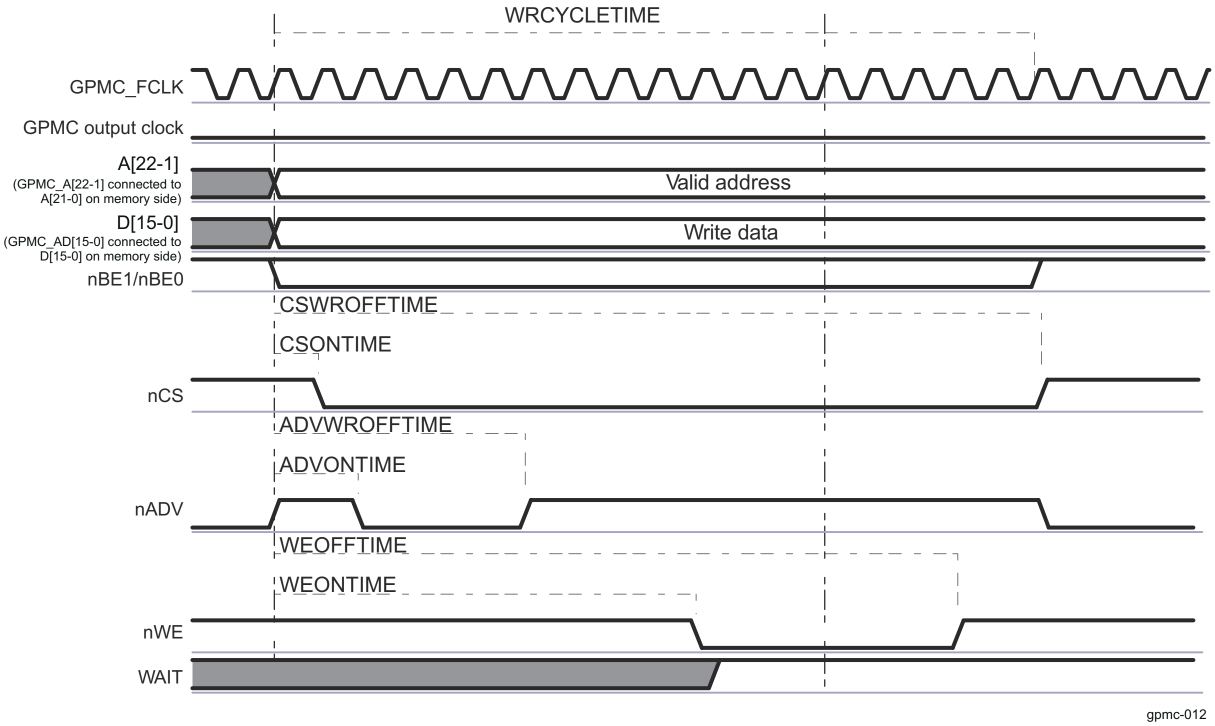

Figure 12-187. Asynchronous Single Write on an Address/Data-non-multiplexed Device

The nCS, nADV, nWE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 12-284).

12.3.3.4.9.3.3 Asynchronous Multiple (Page Mode) Read Operation on non-multiplexed Device

Figure 12-188 shows an asynchronous multiple-read operation on a non-multiplexed device in which two word32 host read accesses to the GPMC are split into one multiple- (page mode of 4 word16) read access to the attached device.

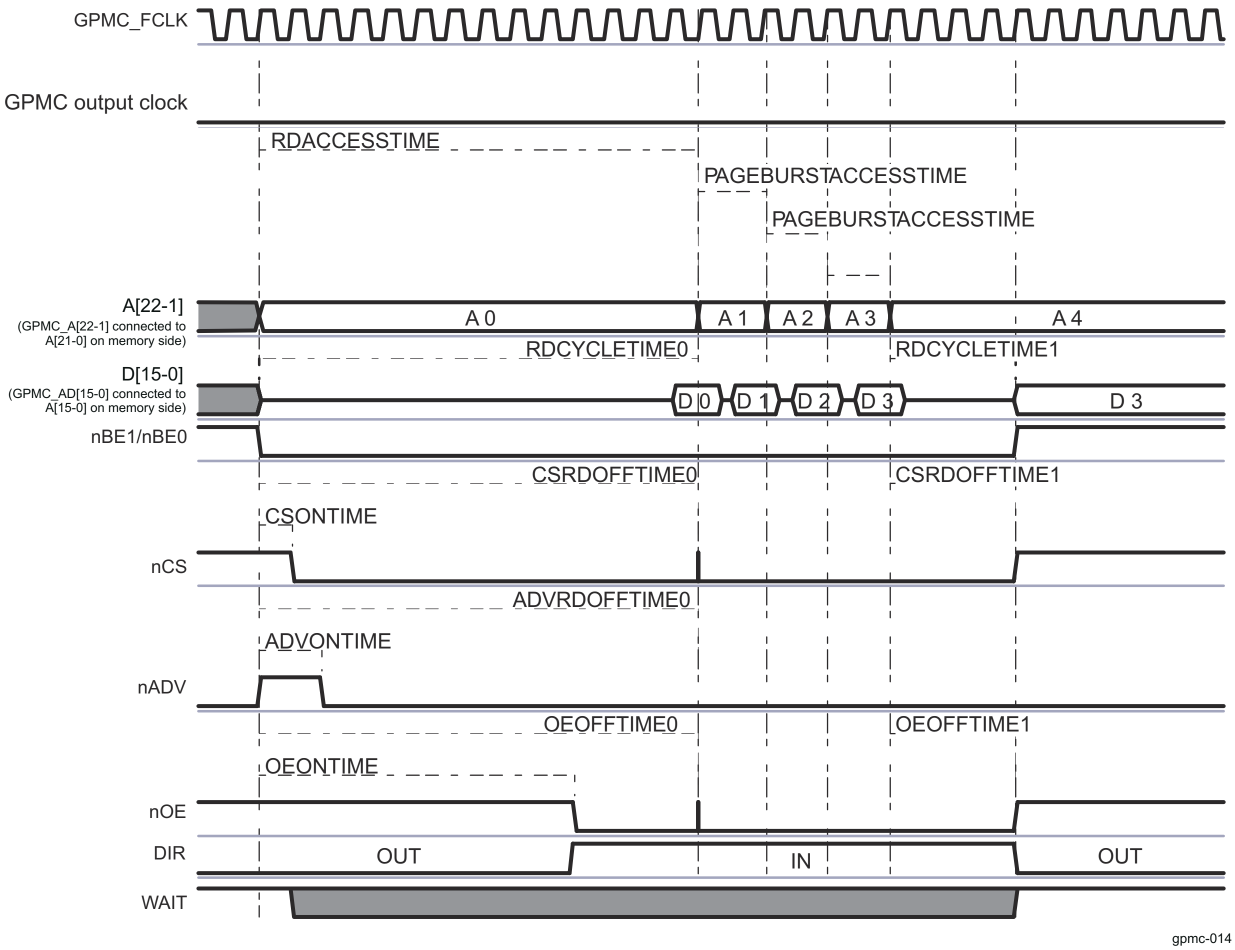

Figure 12-188. Asynchronous Multiple (Page Mode) Read

Note

The WAIT signal is active low.

The nCS, nADV, nOE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 12-284).

When RDACCESSTIME completes, control signal timings are frozen during the multiple data transactions, corresponding to PAGEBURSTACCESSTIME multiplied by the number of remaining data transactions.

Read data is latched at GPMC_CONFIG5_i[20-16] RDACCESSTIME completion time (where i = 0 to 3). The end of the access is defined by the GPMC_CONFIG5_i[4-0] RDCYCLETIME parameter.

During consecutive accesses, the GPMC increments the address after each data read completes.

Delay between successive read data in the page is controlled by the GPMC_CONFIG5_i[27-24] PAGEBURSTACCESSTIME parameter. Depending on the device page length, the GPMC can control device page crossing during a burst request and insert initial RDACCESSTIME latency. Page crossing is possible only with a new burst access, meaning a new initial access phase is initiated.

Total access time RDCYCLETIME corresponds to RDACCESSTIME, plus the address hold time, starting from the nCS deassertion.

- The read cycle time is defined in the GPMC_CONFIG5_i[4-0] RDCYCLETIME bit field.

- In Figure 12-188, the programmed value of RDCYCLETIME equals RDCYCLETIME0 (before paged accesses) + RDCYCLETIME1 (after paged accesses).

12.3.3.4.9.3.4 Synchronous Operations on a non-multiplexed Device

All information for this section is equivalent to similar operations for address/data-multiplexed or AAD-multiplexed accesses. The only difference resides in the address phase. See Section 12.3.3.5.3 , *GPMC Configuration in NOR Mode*.

12.3.3.4.9.4 Page and Burst Support

Each chip-select can be configured to process system single or burst requests into successive single accesses or asynchronous page/synchronous burst accesses, with appropriate access size adaptation.

Depending on the external device page or burst capability, read and write accesses can be independently configured through the GPMC. The GPMC_CONFIG1_i[30] READMULTIPLE and GPMC_CONFIG1_i[28] WRITMULTIPLE bits (where i = 0 to 3) are associated with the READTYPE and WRITETYPE parameters.

Note

- Asynchronous write page mode is not supported.
- 8-bit-wide device support is limited to nonburstable devices (READMULTIPLE and WRITEMULTIPLE are ignored).
- Not applicable to NAND device interfacing.

12.3.3.4.9.5 System Burst vs External Device Burst Support

The device system can issue the following requests to the GPMC:

- Byte, 16-bit word, 32-bit word requests (byte-enable-controlled). This is always a single request from the interconnect point of view.
- Incrementing fixed-length bursts of two, four, and eight words
- Wrapped (critical word access first) fixed-length burst of two, four, or eight words

To process a system request with the optimal protocol, the READMULTIPLE (and READTYPE) and WRITEMULTIPLE (and WRITETYPE) parameters must be set according to the burstable capability (synchronous or asynchronous) of the attached device.

The GPMC access engine issues only fixed-length bursts. The maximum length that can be issued is defined per chip-select by the GPMC_CONFIG1_i[24-23] ATTACHEDDEVICEPAGELENGTH bit field (where i = 0 to 3). When the value of ATTACHEDDEVICEPAGELENGTH is less than the length of the system burst request (including the appropriate access size adaptation according to the device width), the GPMC splits the system burst request into multiple bursts. Within the specified 4-, 8-, or 16-word value, the value of the ATTACHEDDEVICEPAGELENGTH bit field must correspond to the maximum length burst supported by the memory device configured in fixed-length burst mode (as opposed to continuous burst mode).

To get optimal performance from memory devices that natively support 16 Word16-length-wrapping burst capability (critical word access first), the ATTACHEDDEVICEPAGELENGTH parameter must be set to 16 words and the GPMC_CONFIG1_i[31] WRAPBURST bit (where i = 0 to 3) must be set to 1. Similarly DEVICEPAGELENGTH is set to 4 and 8 for memories supporting 4 and 8 Word16-length-wrapping burst, respectively.

When the memory device does not offer (or is not configured to offer) native 16 Word16-length-wrapping burst, the WRAPBURST parameter must be cleared, and the GPMC access engine emulates the wrapping burst by issuing the appropriate burst sequences according to the value of ATTACHEDDEVICEPAGELENGTH.

When the memory device does not support native-wrapping burst, there is usually no difference in behavior between a fixed-burst length mode and a continuous-burst mode configuration (except for a potential power increase from a memory-speculative data prefetch in a continuous burst read). However, even though continuous burst mode is compatible with GPMC behavior, because the GPMC access engine issues only fixed-length burst and does not benefit from continuous burst mode, it is best to configure the memory device in fixed-length burst mode.

The memory device maximum-length burst (configured in fixed-length burst wrap or nonwrap mode) usually corresponds to the memory device data buffer size. Memory devices with a minimum of 16 half-word buffers are the most appropriate (especially with wrap support), but memory devices with smaller buffer size (4 or 8) are also supported, assuming that the GPMC_CONFIG1_i[24-23] ATTACHEDDEVICEPAGELENGTH bit field is set accordingly to 4 or 8 words.

The device system issues only requests with addresses or starting addresses for nonwrapping burst requests; that is, the request size boundary is aligned. In case of an eight-word-wrapping burst, the wrapping address always occurs on the eight-word boundary. As a consequence, all words requested must be available from the memory data buffer when the buffer size is equal to or greater than the value of ATTACHEDDEVICEPAGELENGTH. This usually means that data can be read from or written to the buffer at a constant rate (number of cycles between data) without wait-states between data accesses. If the memory does not behave this way (nonzero wait-state burstable memory), WAIT pin monitoring must be enabled to dynamically control data access completion within the burst.

Note

When the system burst request length is less than the value of ATTACHEDDEVICEPAGELENGTH, the GPMC proceeds with the required accesses.

12.3.3.4.10 GPMC pSRAM Access Specificities

pSRAM devices are SRAM-pin-compatible low-power memories that contain a self-refreshed DRAM memory array. The GPMC_CONFIG1_i[11-10] DEVICETYPE bit field (where i = 0 to 3) must be set to 0b00.

The pSRAM device uses the NOR protocol. It supports the following operations:

- Asynchronous single read
- Asynchronous page read
- Asynchronous single write
- Synchronous single read and write
- Synchronous burst read
- Synchronous burst write (not supported by NOR flash memory)

pSRAM devices must be powered up and initialized in a predefined manner according to the specifications of the attached device.

pSRAM devices can be programmed to use either mode: fixed or variable latency. pSRAM devices can automatically schedule autorefresh operations, which force the GPMC to use its WAIT signal capability when read or write operations occur during an internal self-refresh operation, or they can automatically include the autorefresh operation in the access time. These devices do not require additional WAIT signal capability or a minimum nCS high pulse width between consecutive accesses to ensure that the correct internal refresh operation is scheduled.

12.3.3.4.11 GPMC NAND Access Description

NAND (8-bit and 16-bit) memory devices using a standard NAND asynchronous address/data-multiplexing scheme can be supported on any chip-select with the appropriate asynchronous configuration settings.

As for any other type of memory compatible with the GPMC interface, accesses to a chip-select allocated to a NAND device can be interleaved with accesses to chip-selects allocated to other external devices. This interleaved capability limits the system to *chip enable don't care* NAND devices, because the chip-select allocated to the NAND device must be deasserted if accesses to other chip-selects are requested.

12.3.3.4.11.1 NAND Memory Device in Byte or 16-bit Word Stream Mode

NAND devices require correct command and address programming before data array read or write accesses. The GPMC does not include specific hardware to translate a random address system request into a NAND-specific multiphase access. In that sense, GPMC NAND support, as opposed to random memory-map device support, is data stream-oriented (byte or 16-bit word).

The GPMC NAND programming model depends on a software driver for address and command formatting with the correct data address pointer value according to the block and page structure. Because of NAND structure and protocol interface diversity, the GPMC does not support automatic command and address phase programming, and software drivers must access the NAND device ID to ensure that correct command and address formatting are used for the identified device.

NAND device data read and write accesses are achieved through an asynchronous read or write access. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Any chip-select region can be qualified as a NAND region to constrain the nADV/ALE signal as ALE (ALE active high, default state value at low) during address program access, and the nBE0/CLE signal as CLE (CLE active high, default state value at low) during command program access. GPMC address lines are not used (the previous value is not changed) during NAND access.

12.3.3.4.11.1.1 Chip-Select Configuration for NAND Interfacing in Byte or Word Stream Mode

The GPMC_CONFIG7_i register (where i = 0 to 3) associated with a NAND device region interfaced in byte or word stream mode can be initialized with a minimum size of 16MB, because any address location in the chip-select memory region can be used to access a NAND data array. The NAND flash protocol specifies an address sequence where address bits are passed through the data bus in a series of write accesses with the ALE pin asserted. After this address phase, all operations are streamed and the system requests address is irrelevant.

CAUTION

To allow correct command, address, and data-access controls, the GPMC_CONFIG1_i register associated with a NAND device region must be initialized in asynchronous read and write modes with the parameters listed in Table 12-253. Failure to comply with these settings corrupts the NAND interface protocol.

Table 12-265. Chip-Select Configuration for NAND Interfacing

Bit Field	Register	Value	Comments
WRAPBURST	GPMC_CONFIG1_i[31] (1)	0	No wrap
READMULTIPLE	GPMC_CONFIG1_i[30]	0	Single access
READTYPE	GPMC_CONFIG1_i[29]	0	Asynchronous mode
WRITEMULTIPLE	GPMC_CONFIG1_i[28]	0	Single access
WRITETYPE	GPMC_CONFIG1_i[27]	0	Asynchronous mode
CLKACTIVATIONTIME	GPMC_CONFIG1_i[26-25]	0b00	
ATTACHEDDEVICEPAGELENGTH	GPMC_CONFIG1_i[24-23]	Don't care	Single-access mode
WAITREADMONITORING	GPMC_CONFIG1_i[22]	0	Wait not monitored by GPMC access engine
WAITWRITEMONITORING	GPMC_CONFIG1_i[21]	0	Wait not monitored by GPMC access engine
WAITMONITORINGTIME	GPMC_CONFIG1_i[19-18]	Don't care	Wait not monitored by GPMC access engine
WAITPINSELECT	GPMC_CONFIG1_i[17-16]		Select which wait is monitored by edge detectors
DEVICESIZE	GPMC_CONFIG1_i[13-12]	0b00 or 0b01	8- or 16-bit interface

Table 12-265. Chip-Select Configuration for NAND Interfacing (continued)

Bit Field	Register	Value	Comments
DEVICETYPE	GPMC_CONFIG1_i[11-10]	0b10	NAND device in stream mode
MUXADDDATA	GPMC_CONFIG1_i[9-8]	0b00	non-multiplexed mode
TIMEPARAGRANULARITY	GPMC_CONFIG1_i[4]	0	Timing achieved with best GPMC clock granularity
GPMCFCLKDIVIDER	GPMC_CONFIG1_i[1-0]	Don't care	Asynchronous mode

---

(1) i = 0 to 3

The GPMC_CONFIG1_i to GPMC_CONFIG4_i registers (where i = 0 to 3) associated with a NAND device region must be initialized with the correct control-signal timing value according to the NAND device timing parameters.

12.3.3.4.11.1.2 NAND Device Command and Address Phase Control

NAND devices require multiple address programming phases. The software driver must issue the correct number of command and address program accesses, according to the device command set and the device address-mapping scheme.

NAND device-command and address-phase programming is achieved through write requests to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i register locations (where i = 0 to 3) with the correct command and address values. These locations are mapped in the associated chip-select register region. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Command and address values are not latched during the access and cannot be read back at the register location.

- Only write accesses must be issued to these locations, but the GPMC does not discard any read access. Accessing a NAND device with nOE and CLE or ALE asserted (read access) can produce undefined results.
- Write accesses to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i register locations must be posted for faster operations (where i = 0 to 3). The GPMC_CONFIG[0] NANDFORCEPOSTEDWRITE bit enables write accesses to these locations as posted, even if they are defined as nonposted.

A write buffer is used to store write transaction information before the external device is accessed:

- Up to eight consecutive posted write accesses can be accepted and stored in the write buffer.
- For nonposted write, the pipeline is one deep.
- An GPMC_STATUS[0] EMPTYWRITEBUFFERSTATUS bit stores the empty status of the write buffer.

The GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i registers (where i = 0 to 3) are 32-bit word locations, which means any 32-or 16-bit word access is split into 4- or 2-byte accesses if an 8-bit-wide NAND device is attached. For multiple-command phase or multiple-address phase, the software driver can use 32- or 16-bit word access to these registers, but it must consider the splitting and little-endian ordering scheme. When only one byte command or address phase is required, only byte write access to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i registers can be used, and any of the four byte locations of the registers is valid.

The same applies to a GPMC_NAND_COMMAND_i and a GPMC_NAND_ADDRESS_i (where i = 0 to 3) 32-bit word write access to a 16-bit-wide NAND device (split into two 16-bit word accesses). In the case of a 16-bit word write access, the MSByte of the 16-bit word value must be set according to the NAND device requirement (usually 0). Either 16-bit word location or any one of the four byte locations of the registers is valid.

12.3.3.4.11.1.3 Command Latch Cycle

Writing data at the GPMC_NAND_COMMAND_i location (where i = 0 to 3) places the data as the NAND command value on the bus, using a regular asynchronous write access.

- nCE is controlled by the CSONTIME and CSWROFFTIME timing parameters.

- CLE is controlled by the ADVONTIME and ADVWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- ALE and nRE (nOE) are maintained inactive.

Figure 12-189 shows the NAND command latch cycle.

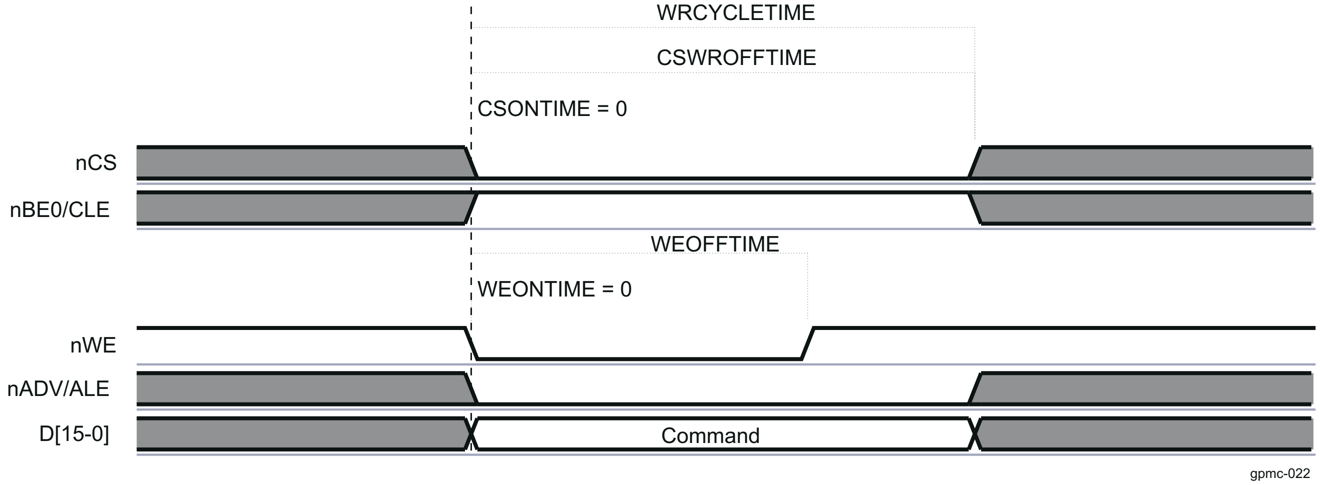

Figure 12-189. NAND Command Latch Cycle

Note

CLE is shared with the nBE0 output signal and has an inverted polarity from BE0. The NAND qualifier deals with this. During the asynchronous NAND data access cycle, nBE0 (also nBE1) must not toggle, because it is shared with CLE.

NAND flash memories do not use byte-enable signals.

12.3.3.4.11.1.4 Address Latch Cycle

Writing data at the GPMC_NAND_ADDRESS_i location (where i = 0 to 3) places the data as the NAND partial address value on the bus, using a regular asynchronous write access.

- nCS is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- ALE is controlled by the ADVONTIME and ADVWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- CLE and nRE (nOE) are maintained inactive.

Figure 12-190 shows the NAND address latch cycle.

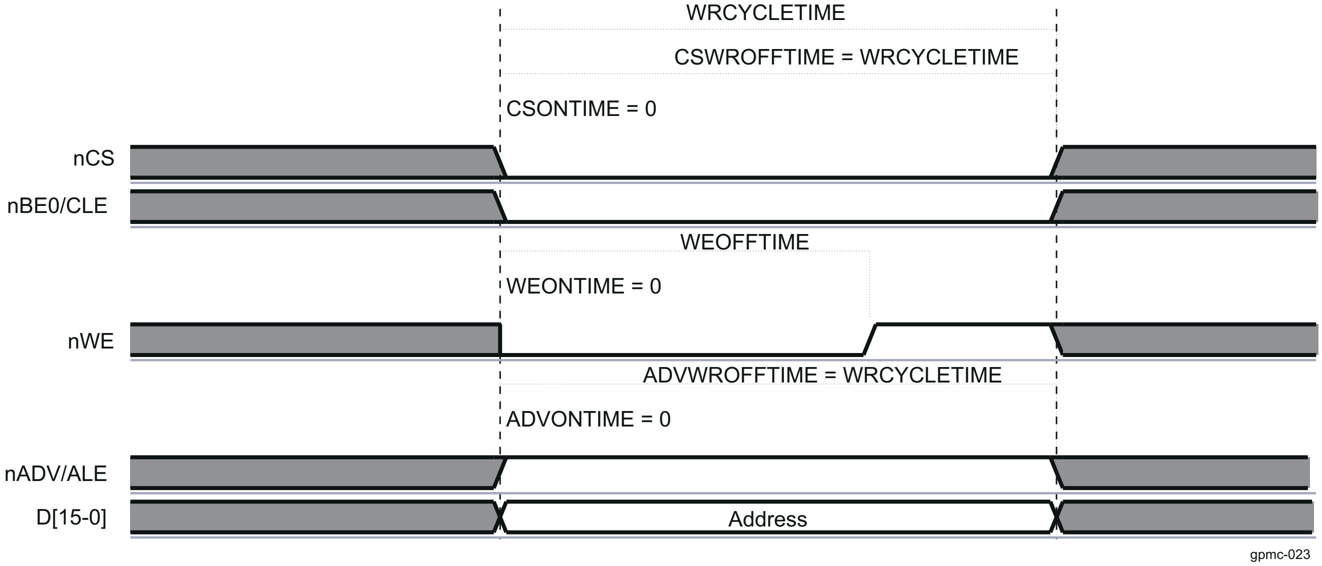

Figure 12-190. NAND Address Latch Cycle

Note

ALE is shared with the nADV output signal and has an inverted polarity from ADV. The NAND qualifier deals with this. During the asynchronous NAND data access cycle, ALE is kept stable.

12.3.3.4.11.1.5 NAND Device Data Read and Write Phase Control in Stream Mode

NAND device data read and write accesses are achieved through a read or write request to the chip-select-associated memory region at any address location in the region or through a read or write request to the GPMC_NAND_DATA_i location (where i = 0 to 3) mapped in the chip-select-associated control register region. GPMC_NAND_DATA_i is not a true register, but an address location to enable nRE or nWE signal control. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Reading data from the GPMC_NAND_DATA_i location or from any location in the associated chip-select memory region activates an asynchronous read access.

- nCS is controlled by the CSONTIME and CSRDOFFTIME timing parameters.
- nRE is controlled by the OEONTIME and OEOFFTIME timing parameters.
- To take advantage of nRE high-to-data invalid minimum timing value, RDACCESSTIME can be set so that data are effectively captured after nRE deassertion. This allows optimization of NAND read access cycle time completion. For optimal timing parameter settings, see the NAND device and the device timing parameters.

ALE, CLE, and nWE are maintained inactive.

Figure 12-191 shows the NAND data read cycle.

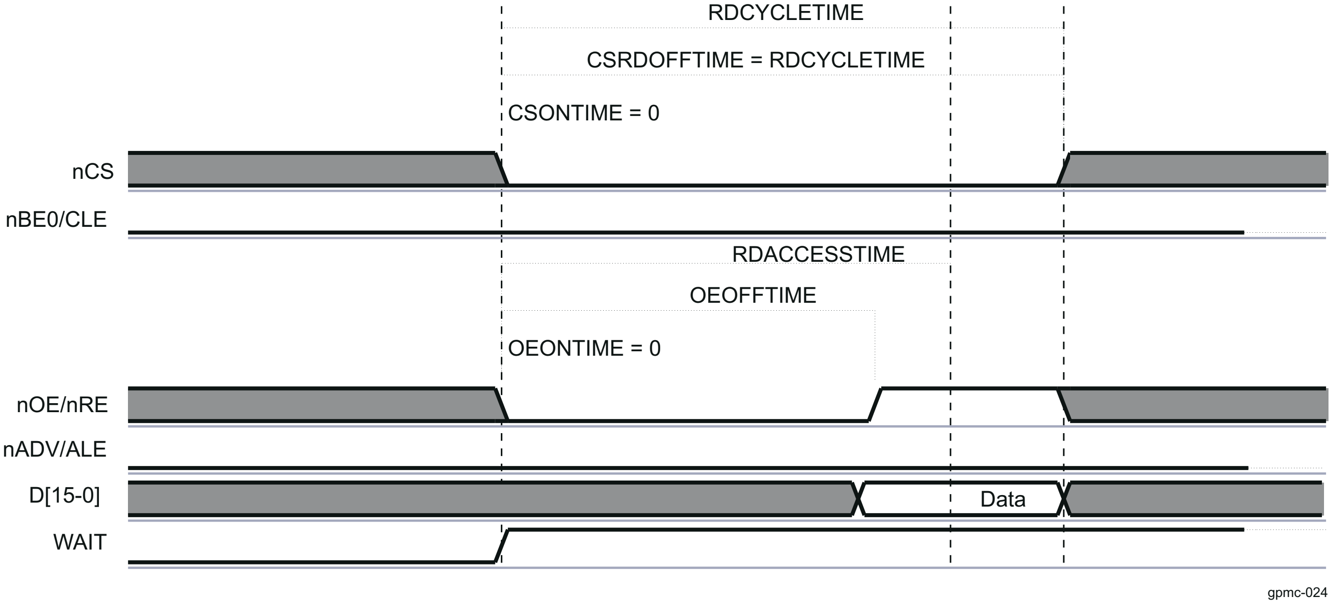

Figure 12-191. NAND Data Read Cycle

Writing data to the GPMC_NAND_DATA_i location or to any location in the associated chip-select memory region activates an asynchronous write access.

- nCS is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- ALE, CLE, and nRE (nOE) are maintained inactive.

Figure 12-192 shows the NAND data write cycle.

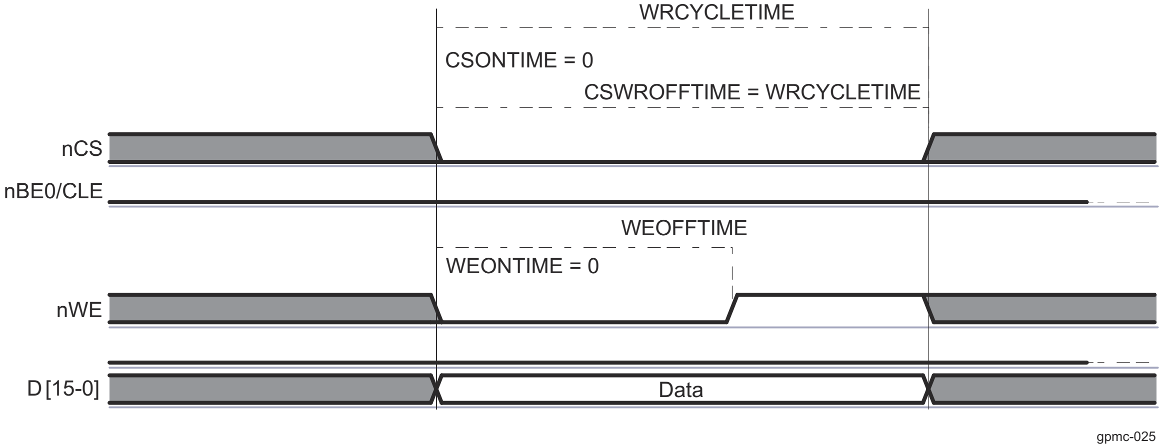

Figure 12-192. NAND Data Write Cycle

12.3.3.4.11.1.6 NAND Device General Chip-Select Timing Control Requirement

For most NAND devices, read data access time is dominated by nCS-to-data-valid timing and has faster nRE-to-data-valid timing. Successive accesses with nCS deassertions between accesses are affected by this timing constraint. Because accesses to a NAND device can be interleaved with other chip-select accesses, there is no certainty that nCS always stays low between two accesses to the same chip-select. Moreover, an nCS deassertion time between the same chip-select NAND accesses is likely to be required as follows: the nCS deassertion requires programming CYCLETIME and RDACCESSTIME according to the nCS-to-data-valid critical timing.

To get full performance from NAND read and write accesses, the prefetch engine can dynamically reduce the following on back-to-back NAND accesses (to the same memory) and suppress the minimum nCS high pulse width between accesses:

- RDCYCLETIME
- WRCYCLETIME
- RDACCESSTIME
- WRACCESSTIME
- CSRDOFFTIME
- CSWROFFTIME
- ADVRDOFFTIME
- ADVWROFFTIME
- OEOFFTIME
- WEOFFTIME

For more information about optimal prefetch engine access, see Section 12.3.3.4.11.4 , *Prefetch and Write-Posting Engine*.

Some NAND devices require minimum write-to-read idle time, especially for device-status read accesses following status-read command programming (write access). If such write-to-read transactions are used, a minimum nCS high pulse width must be set. For this, CYCLE2CYCLESAMECSEN and CYCLE2CYCLEDELAY must be set according to the appropriate timing requirement to prevent any timing violation.

NAND devices usually have an important nRE high-to-data bus in three-state mode. This requires a bus turnaround setting (BUSTURNAROUND = 1) so that the next access to a different chip-select is delayed until the BUSTURNAROUND delay completes. Back-to-back NAND read accesses to the same NAND flash are not affected by the programmed bus turnaround delay.

12.3.3.4.11.1.7 Read and Write Access Size Adaptation

12.3.3.4.11.1.7.1 8-Bit-Wide NAND Device

Host 16- and 32-bit word read and write access requests to a chip-select associated with an 8-bit-wide NAND device are split into successive read and write byte accesses to the NAND memory device. Byte access is ordered according to little-endian organization. A NAND 8-bit-wide device must be interfaced on the D0D7 interface bus lane. GPMC data accesses are justified on this bus lane when the cs is associated with an 8-bit-wide NAND device.

12.3.3.4.11.1.7.2 16-Bit-Wide NAND Device

Host 32-bit word read and write access requests to a chip-select associated with a 16-bit-wide NAND device are split into successive read and write 16-bit word accesses to the NAND memory device. 16-bit word access is ordered according to little-endian organization.

Host byte read and write access requests to a 16-bit-wide NAND device are completed as 16-bit accesses on the device itself, because there is no byte-addressing capability on 16-bit-wide NAND devices. This means that the NAND device address pointer is incremented on a 16-bit word basis and not on a byte basis. For a read access, only the requested byte is given back to the host, but the remaining byte is not stored or saved by the GPMC, and the next byte or 16-bit word read access gets the next 16-bit word NAND location. For a write access, the invalid byte part of the 16-bit word is driven to FF, and the next byte or 16-bit word write access programs the next 16-bit word NAND location.

Generally, byte access to a 16-bit-wide NAND device must be avoided, especially when ECC calculation is enabled. 8- or 16-bit ECC-based computations are corrupted by a byte read to a 16-bit-wide NAND device, because the nonrequested byte is considered invalid on a read access (not captured on the external data bus; FF is fed to the ECC engine) and is set to FF on a write access.

Host requests (read/write) issued in the chip-select memory region are translated in successive single or split accesses (read/write) to the attached device. Therefore, incrementing 32-bit burst requests are translated in multiple 32-bit sequential accesses following the access adaptation of the 32-bit to 8- or 16-bit device.

12.3.3.4.11.2 NAND Device-Ready Pin

The NAND memory device provides a ready pin to indicate data availability after a block/page opening and to indicate that data programming is complete. The ready pin can be connected to one of the wait GPMC input pins; data read accesses must not be tried when the ready pin is sampled inactive (device is not ready) even if the associated chip-select WAITREADMONITORING bit field is set. The duration of the NAND device busy state after the block/page opening is so long (up to 50 micro second) that accesses occurring when the ready pin is sampled inactive can stall GPMC access and eventually cause a system time-out.

Note

If a read access to a NAND flash is done using WAIT monitoring mode, the device is blocked during a page opening, and so is the GPMC. If the correct settings are used, other chip-selects can be used while the memory processes the page opening command.

To avoid a time-out caused by a block/page opening delay in NAND flash, disable the WAIT pin monitoring for read and write accesses (that is, set the GPMC_CONFIG1_i[21] WAITWRITEMONITORING and GPMC_CONFIG1_i[22] WAITREADMONITORING bits to 0, where i = 0 to 3), and use one of the following methods instead:

- Use software to poll the WAITxSTATUS bit (where x = 0 to 1) of the GPMC_STATUS.
- Configure an interrupt that is generated on the WAIT signal change (through the GPMC_IRQENABLE register bits[11-8]).

Even if the READWAITMONITORING bit is not set, the external memory nR/B pin status is captured in the programmed wait bit in the GPMC_STATUS register.

The READWAITMONITORING bit method must be used for other memories than NAND flash, if they require the use of a WAIT signal.

12.3.3.4.11.2.1 Ready Pin Monitored by Software Polling

The ready signal state can be monitored through the GPMC_STATUS[9-8] WAITxSTATUS bit (where x = 0 to 1). Software must monitor the ready pin only when the signal is declared valid. Refer to the NAND device timing parameters to set the correct software temporization to monitor ready only after the invalid window is complete from the last read command written to the NAND device.

12.3.3.4.11.2.2 Ready Pin Monitored by Hardware Interrupt

Each GPMC_WAIT input pin can generate an interrupt when a wait-to-no-wait transition is detected. Depending on whether the GPMC_CONFIG[9-8] WAITxPINPOLARITY bits (where x = 0 to 1) is active low or active high, the wait-to-no-wait transition is a low-to-high external WAIT signal transition or a high-to-low external WAIT signal transition, respectively.

The wait transition pin detector must be cleared before any transition detection. This is done by writing 1 to the WAITxEDGEDETECTIONSTATUS bit (where x = 0 to 1) of the GPMC_IRQSTATUS register according to the GPMC_WAIT pin used for the NAND device-ready signal monitoring. To detect a wait-to-no-wait transition, the transition detector requires a wait active time detection of a minimum of two GPMC_FCLK cycles. Software must incorporate precautions to clear the wait transition pin detector before wait (busy) time completes.

A wait-to-no-wait transition detection can issue a GPMC interrupt if the WAITxEDGEDETECTIONENABLE bit in the GPMC_IRQENABLE register is set and if the WAITxEDGEDETECTIONSTATUS bit field in the GPMC_IRQSTATUS register is set.

The WAITMONITORINGTIME bit field does not affect wait-to-no-wait transition time detection.

It is also possible to poll the WAITxEDGEDETECTIONSTATUS bit field in the GPMC_IRQSTATUS register according to the GPMC_WAIT pin used for NAND device ready signal monitoring.

12.3.3.4.11.3 ECC Calculator

The GPMC includes an error code correction (ECC) calculator circuitry that enables ECC calculation on the fly during data read or data program (that is, write) operations. The page size supported by the ECC calculator in one calculation/context is 512 bytes.

The user can choose from two different algorithms with different error correction capabilities through the GPMC_ECC_CONFIG[16] ECCALGORITHM bit:

1. Hamming code for 1-bit error code correction on 8- or 16-bit NAND flash organized with page size greater than 512 bytes
2. Bose-Chaudhurl-Hocquenghem (BCH) code for 4- to 16-bit error correction

The GPMC does not handle the error code correction directly. During writes, the GPMC computes parity bits. During reads, the GPMC provides enough information for the processor to correct errors without reading the data buffer all over again.

The Hamming code ECC is based on a 2-dimensional (2D) (row and column) bit parity accumulation. This parity accumulation is accomplished on the programmed number of bytes or 16-bit words read from the memory device, or is written to the memory device in stream mode.

Because the ECC engine includes only one accumulation context, it can be allocated to only one chip-select at a time through the GPMC_ECC_CONFIG[3-1] ECCCS bit field. Even if two chip-selects use different ECC algorithms, one the Hamming code and the other a BCH code, they must define separate ECC contexts because some of the ECC registers are common to all types of algorithms.

12.3.3.4.11.3.1 Hamming Code

All references to ECC in this subsection refer to the 1-bit error correction Hamming code.

The ECC is based on a 2D (row and column) bit parity accumulation known as the Hamming code. The parity accumulation is done for a programmed number of bytes or 16-bit word read from the memory device or written to the memory device in stream mode.

There is no automatic error detection or correction, and the software NAND driver must read the multiple ECC calculation results, compare them to the expected code value, and take the appropriate corrective actions according to the error handling strategy (ECC storage in spare byte, error correction on read, block invalidation).

The ECC engine includes a single accumulation context. It can be allocated to a single designated chip-select at a time, and parallel computations on different chip-selects are not possible. Because it is allocated to a single chip-select, the ECC computation is not affected by interleaved GPMC accesses to other chip-selects and devices. The ECC accumulation is sequentially processed in the order of data read from or written to the memory on the designated chip-select. The ECC engine does not differentiate read accesses from write accesses and does not differentiate data from command or status information. Software must ensure that only relevant data are passed to the NAND flash memory while the ECC computation engine is active.

The starting NAND page location must be programmed first, followed by an ECC accumulation context reset with an ECC enabling, if required. The NAND device accesses discussed in the following sections must be limited to data read or write until the specified number of ECC calculations is complete.

12.3.3.4.11.3.1.1 ECC Result Register and ECC Computation Accumulation Size

The GPMC includes up to nine ECC result registers (GPMC_ECCj_RESULT, where j = 1 to 9) to store ECC computation results when the specified number of bytes or 16-bit words has been computed.

The ECC result registers are used sequentially: one ECC result is stored in one ECC result register on the list, the next ECC result is stored in the next ECC result register on the list, and so forth, until the last ECC computation. The value of the GPMC_ECCj_RESULT register is valid only when the programmed number of bytes or 16-bit words has been accumulated, which means that the same number of bytes or 16-bit words has been read from or written to the NAND device in sequence.

The GPMC_ECC_CONTROL[3-0] ECCPOINTER bit field must be set to the correct value to select the ECC result register to be used first in the list for the incoming ECC computation process. The ECCPointer can be read to determine which ECC register is used in the next ECC result storage for the ongoing ECC computation. The value of the GPMC_ECCj_RESULT register (where j = 1 to 9) can be considered valid when ECCPOINTER equals j + 1. When the GPMC_ECCj_RESULT register (where j = 9) is updated, ECCPOINTER is frozen at 10, and ECC computing is stopped (ECCENABLE = 0).

The ECC accumulator must be reset before any ECC computation accumulation process. The GPMC_ECC_CONTROL[8] ECCCLEAR bit must be set to 1 (nonpersistent bit) to clear the accumulator and all ECC result registers.

For each ECC result (each GPMC_ECCj_RESULT register, where j = 1 to 9), the number of bytes or 16-bit words used for ECC computing accumulation can be selected from between two programmable values.

The ECCjRESULTSIZE bits (where j = 1 to 9) in the GPMC_ECC_SIZE_CONFIG register select which programmable size value (ECCSIZE0 or ECCSIZE1) must be used for this ECC result (stored in the GPMC_ECCj_RESULT register).

The ECCSIZE0 and ECCSIZE1 bit fields allow selection of the number of bytes or 16-bit words used for ECC computation accumulation. Any even values from 2 to 512 are allowed.

Flexibility in the number of ECCs computed and the number of bytes or 16-bit words used in the successive ECC computations enables different NAND page error-correction strategies. Usually based on 256 or 512 bytes and on 128 or 256 16-bit word, the number of ECC results required is a function of the NAND device page size. Specific ECC accumulation size can be used when computing the ECC on the NAND spare byte.

For example, with a 2-KB data page, 8-bit-wide NAND device, eight ECCs accumulated on 256 bytes can be computed and added to one extra ECC computed on the 24 spare bytes area where the eight ECC results used for comparison and correction with the computed data page ECC are stored. The GPMC then provides nine GPMC_ECCj_RESULT registers (j = 1 to 9) to store the results. In this case, ECCSIZE0 is set to 256, and ECCSIZE1 is set to 24; the ECC[1-8]RESULTSIZE bits are set to 0, and the ECC9RESULTSIZE bit is set to 1.

12.3.3.4.11.3.1.2 ECC Enabling

The GPMC_ECC_CONFIG[3-1] ECCCS bit field selects the allocated chip-select. The GPMC_ECC_CONFIG[0] ECCENABLE bit enables ECC computation on the next detected read or write access to the selected chip-select.

The following fields must not be changed or cleared while an ECC computation is in progress:

- ECCPOINTER
- ECCCLEAR
- ECCSIZE
- ECCjRESULTSIZE (where j = 1 to 9)
- ECC16B
- ECCCS

The ECC accumulator and ECC result register must not be changed or cleared while an ECC computation is in progress.

Table 12-254 describes the ECC enable settings.

Table 12-266. ECC Enable Settings

Bit Field	Register	Value	Comments
ECCCS	GPMC_ECC_CONFIG	0–3	Selects the chip-select where ECC is computed
ECC16B	GPMC_ECC_CONFIG	0/1	Selects column number for ECC calculation
ECCCLEAR	GPMC_ECC_CONTROL	0–7	Clears all ECC result registers
ECCPOINTER	GPMC_ECC_CONTROL	0–7	A write to this bit field selects the ECC result register where the first ECC computation is stored. Set to 1 by default.

Table 12-266. ECC Enable Settings (continued)

Bit Field	Register	Value	Comments
ECCSIZE1	GPMC_ECC_SIZE_CONFIG	0x00–0xFF	Defines ECCSIZE1
ECCSIZE0	GPMC_ECC_SIZE_CONFIG	0x00–0xFF	Defines ECCSIZE0
ECCjRESULTSIZE (j from 1 to 9)	GPMC_ECC_SIZE_CONFIG	0/1	Selects the size of ECCn result register
ECCENABLE	GPMC_ECC_CONFIG	1	Enables the ECC computation

12.3.3.4.11.3.1.3 ECC Computation

The ECC algorithm is a multiple parity bit accumulation computed on the odd and even bit streams extracted from the byte or Word16 streams. The parity accumulation is split into row and column accumulations, as shown in Figure 12-193 and Figure 12-194. The intermediate row and column parities are used to compute the upper level row and column parities. Only the final computation of each parity bit is used for ECC comparison and correction.

P1o = bit7 XOR bit5 XOR bit3 XOR bit1 on each byte of the data stream
P1e = bit6 XOR bit4 XOR bit2 XOR bit0 on each byte of the data stream

P2o = bit7 XOR bit6 XOR bit3 XOR bit2 on each byte of the data stream
P2e = bit5 XOR bit4 XOR bit1 XOR bit0 on each byte of the data stream

P4o = bit7 XOR bit6 XOR bit5 XOR bit4 on each byte of the data stream
P4e = bit3 XOR bit2 XOR bit1 XOR bit0 on each byte of the data stream

Each column parity bit is XORed with the previous accumulated value.

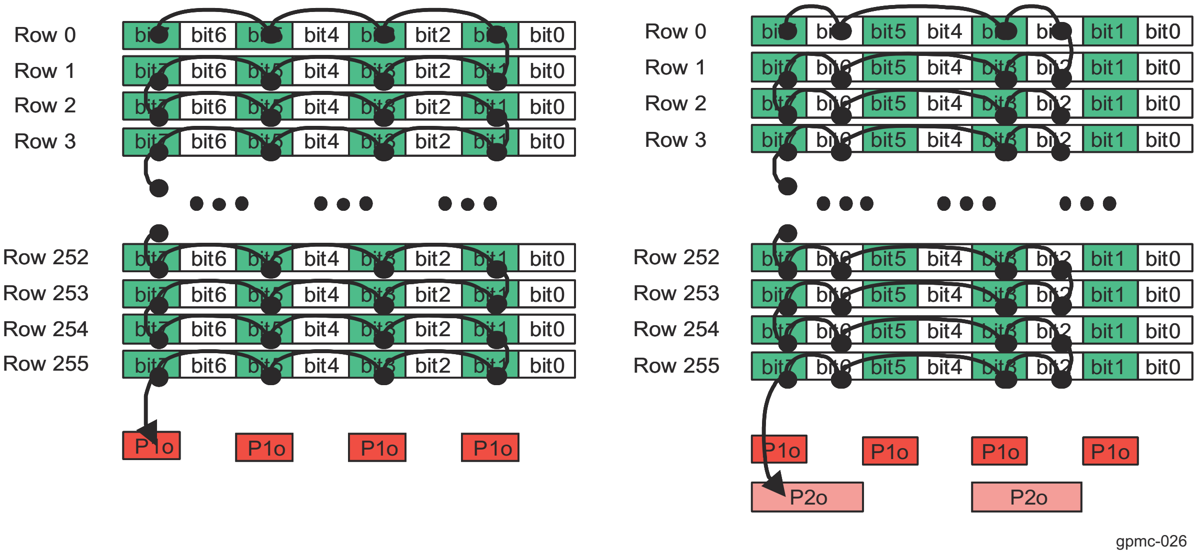

Figure 12-193. Hamming Code Accumulation Algorithm (1/2)

For line parities, the bits of each new data are XORed together, and line parity bits are computed as described below:

P8e = row0 XOR row2 XOR row4 XOR ... XOR row254
P8o = row1 XOR row3 XOR row5 XOR ... XOR row255

P16e = row0 XOR row1 XOR row4 XOR row5 XOR ... XOR row252 XOR row 253
P16o = row2 XOR row3 XOR row6 XOR row7 XOR ... XOR row254 XOR row 255

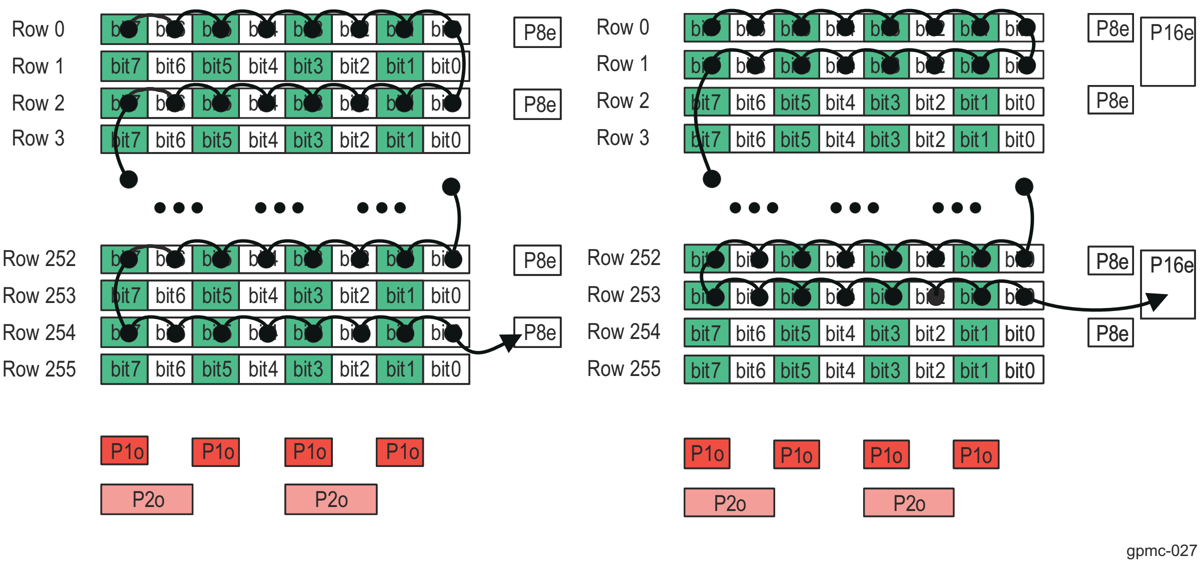

Figure 12-194. Hamming Code Accumulation Algorithm (2/2)

Unused parity bits in the result registers are set to 0.

Figure 12-195 shows ECC computation for a 256-byte data stream (read or write). The result includes six column parity bits (P1o-P2o-P4o for odd parities, and P1e-P2e-P4e for even parities) and sixteen row parity bits (P8o-P16o-P32o--P1024o for odd parities, and P8e-P16e-P32e--P1024e for even parities).

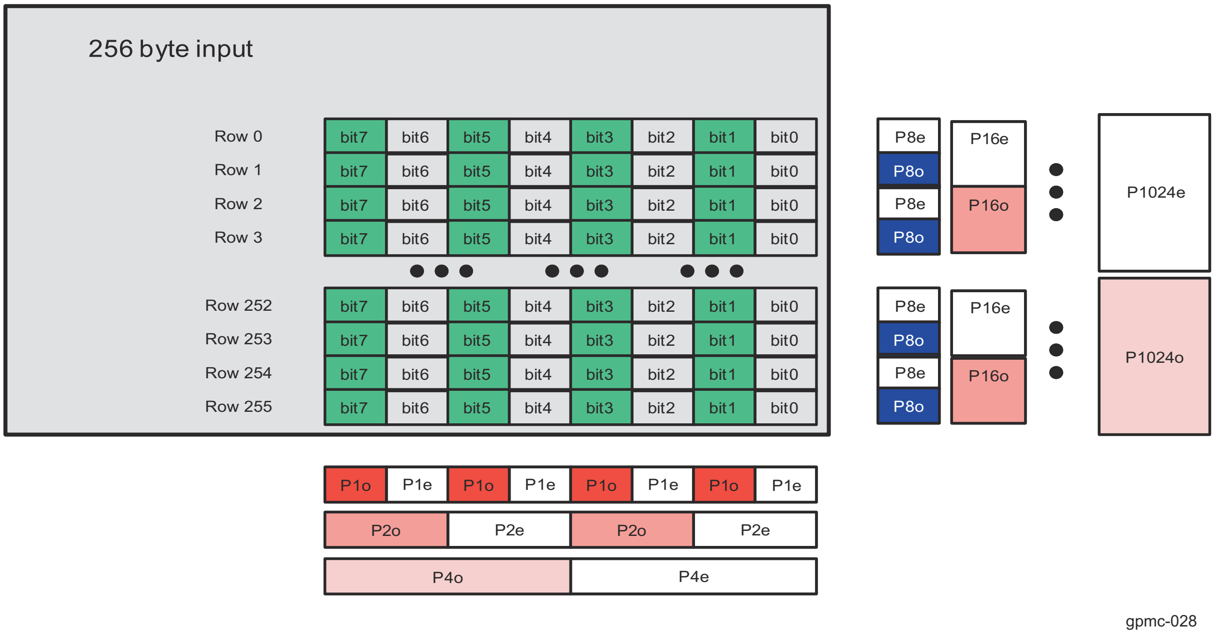

Figure 12-195. ECC Computation for a 256-Byte Data Stream (Read or Write)

Figure 12-196 shows ECC computation for a 512-byte data stream (read or write). The result includes six column parity bits (P1o-P2o-P4o for odd parities, and P1e-P2e-P4e for even parities) and eighteen row parity bits (P8o-P16o-P32o--P1024o- - P2048o for odd parities, and P8e-P16e-P32e--P1024e- P2048e for even parities).

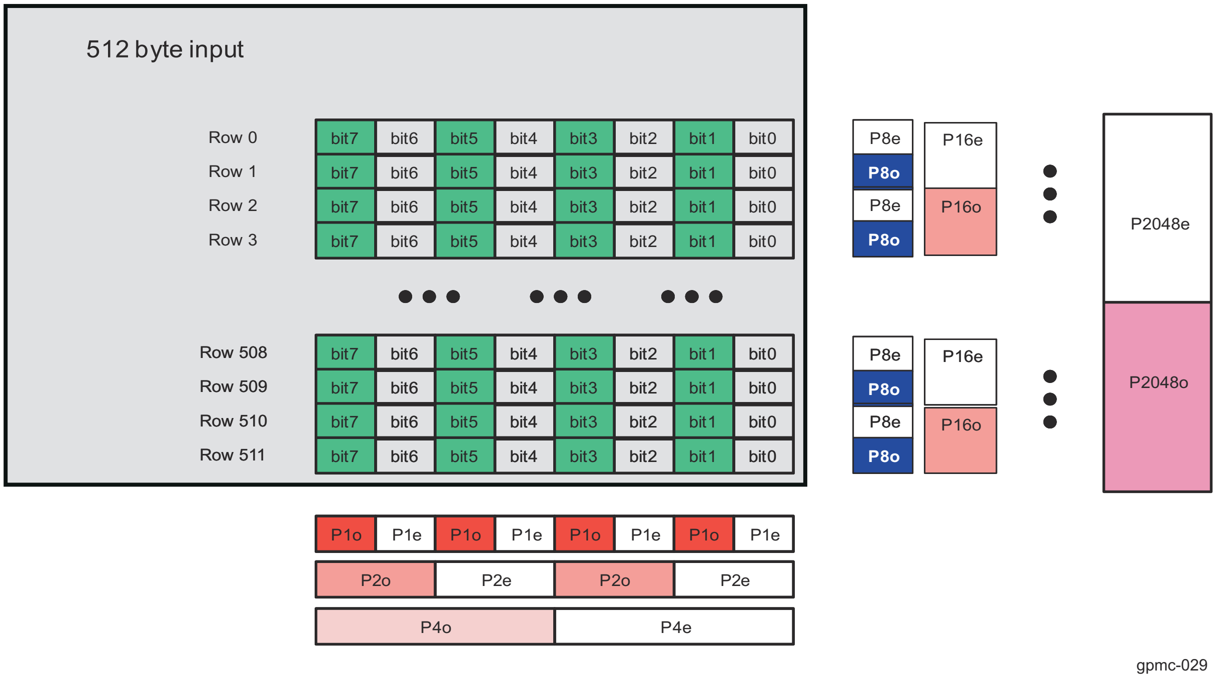

Figure 12-196. ECC Computation for a 512-Byte Data Stream (Read or Write)

For a 2-KB page, four 512 bytes ECC calculations plus 1 for the spare area are required. Results are stored in the GPMC_ECCj_RESULT registers (where j = 1 to 9).

12.3.3.4.11.3.1.4 ECC Comparison and Correction

To detect an error, the computed ECC result must be XORed with the parity value stored in the spare area of the accessed page.

- If the result of this logical XOR is all 0s, no error is detected and the read data is correct.
- If every second bit in the parity result is a 1, 1 bit is corrupted and is located at bit address (P2048o, P1024o, P512o, P256o, P128o, P64o, P32o, P16o, P8o, P4o, P2o, P1o). Software must correct the corresponding bit.
- If only 1 bit in the parity result is 1, it is an ECC error and the read data is correct.

12.3.3.4.11.3.1.5 ECC Calculation Based on 8-Bit Word

The 8-bit-based ECC computation is used for 8-bit-wide NAND device interfacing.

The 8-bit-based ECC computation can be used for 16-bit-wide NAND device interfacing to get backward compatibility on the error-handling strategy used with 8-bit-wide NAND devices. In this case, the 16-bit-wide data read from or written to the NAND device is fragmented into 2 bytes. According to little-endian access, the LSB of the 16-bit-wide data is ordered first in the byte stream used for 8-bit-based ECC computation.

12.3.3.4.11.3.1.6 ECC Calculation Based on 16-Bit Word

ECC computation based on an 16-bit word is used for 16-bit-wide NAND device interfacing. This ECC computation is not supported when interfacing an 8-bit-wide NAND device, and the GPMC_ECC_CONFIG[7] ECC16B bit must be set to 0 when interfacing an 8-bit-wide NAND device.

The parity computation based on 16-bit words affects the row and column parity mapping. The main difference is that the odd and even parity bits P8o and P8e are computed on rows for an 8-bit-based ECC and on columns for a 16-bit based ECC. Figure 12-197 and Figure 12-198 show a 128 Word16 ECC computation scheme and a 256 16-bit word ECC computation scheme.

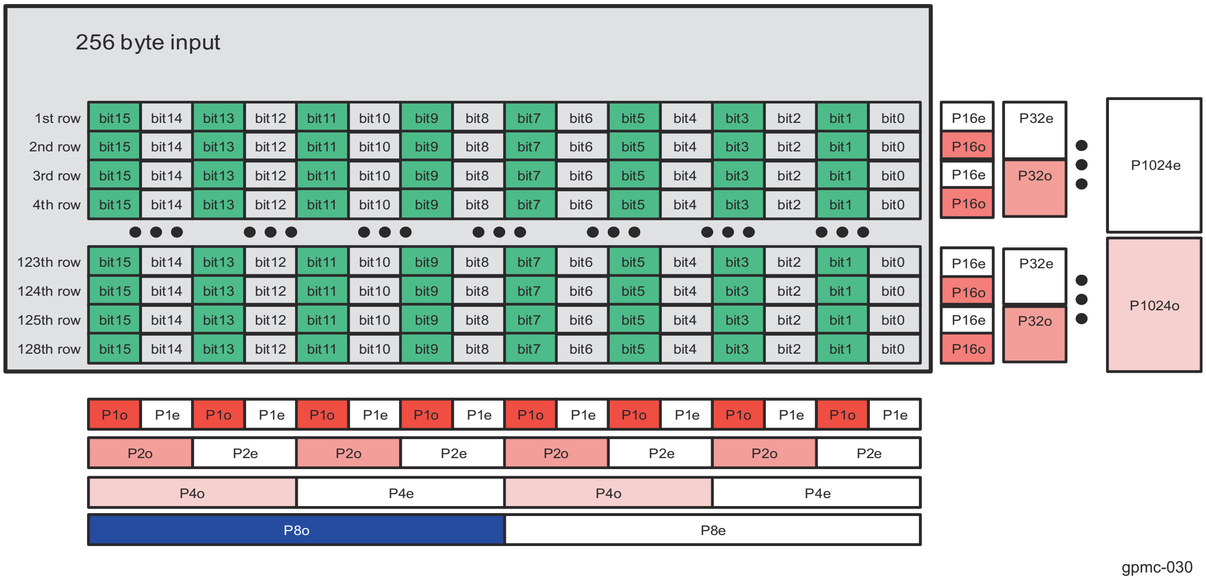

Figure 12-197. 128 Word16 ECC Computation

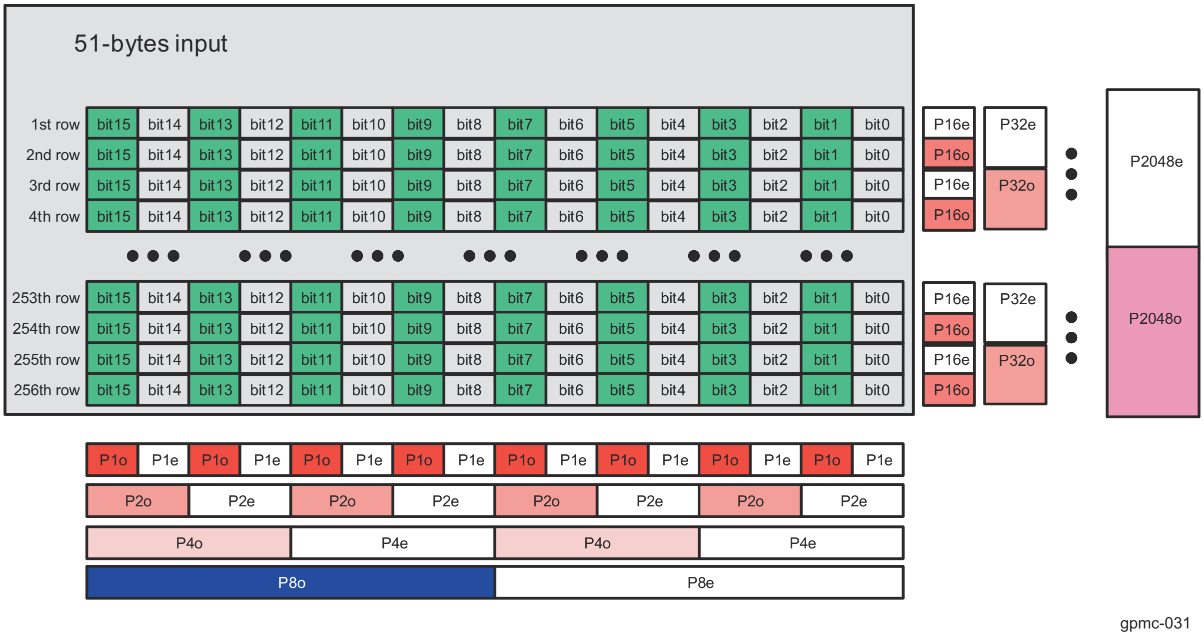

Figure 12-198. 256 Word16 ECC Computation

12.3.3.4.11.3.2 BCH Code

All references to ECC in this subsection refer to the 4- to 16-bit error correction BCH code.

12.3.3.4.11.3.2.1 Requirements

1. Read and write accesses to a NAND flash take place by whole pages, in a predetermined sequence: first the data byte page itself, and then some spare bytes, including the BCH ECC (and other information). The NAND device can cache a full page, including spares, for read and write accesses.
   - Typical page write sequence:
     - Sequential write to NAND cache of main data plus spare data, for a page. ECC is calculated on the fly. Calculated ECC can be inserted on the fly in the spares or replaced by dummy accesses.

  - When the calculated ECC is replaced by dummy accesses, it must be written to the cache in a second, separate phase. The ECC module is disabled during that time.
  - NAND writes its cache line (page) to the array.
- Typical page read sequence:
  - Sequential read of a page. ECC is calculated on the fly.
  - The status of the ECC module buffers determines the presence of errors.

2. Accesses to several memories can be interleaved by the GPMC, but only one of those memories at a time can be a NAND using the BCH engine; in other words, only one BCH calculation (for example, for a single page) can be ongoing at any time. The sequential nature of NAND accesses ensures that the data is always written or read out in the same order. BCH-relevant accesses are selected by the chip-selects of the GPMC.
3. Each page can hold up to 4KB of data, spare bytes not included. This means up to 8 × 512-byte BCH messages. Because all the data is written or read out first, followed by the BCH ECC, the BCH engine must be able to hold eight 104-bit remainders or syndromes (or smaller, 52-bit ones) at the same time.

   The BCH module can store all remainders internally. After the page start, an internal counter is used to detect the 512-byte sector boundaries. On those boundaries, the current remainder is stored and the divider reset for the next calculation. At the end of the page, the BCH module contains all remainders.
4. NAND access cycles hold 8 or 16 bits of data each (1 or 2 bytes); Each NAND cycle takes at least four cycles of the GPMC internal clock. This means the NAND flash timing parameters must define a RDCYCLETIME and a WRCYCLETIME of at least four clock cycles after optimization when using the BCH calculator.
5. The spare area is assumed to be large enough to hold the BCH ECC; that is, to have a message of at least 13 bytes available per 512-byte sector of data. The zone of unused spare area by the ECC may or may not be protected by the same ECC scheme, by extending the BCH message beyond 512 bytes (the maximum codeword is 1023 bytes long, ECC included, which leaves much space to cover spare bytes).

12.3.3.4.11.3.2.2 Memory Mapping of BCH Codeword

BCH encoding considers a block of data to protect as a polynomial message M(x). In a standard case, 512 bytes of data (that is, 2^{12} bits = 4096 bits) are seen as a polynomial of degree $2^{12} - 1 = 4095$, with parameters ranging from M0 to M4095. For 512 bytes of data, 52 bits are required for 4-bit error correction, 104 bits are required for 8-bit error correction, and 207 bits are required for 16-bit error correction. The ECC is a remainder polynomial R(x) of degree 103 (or 51, depending on the selected mode). The complete codeword C(x) is the concatenation of M(x) and R(x), as described in Table 12-255.

Table 12-267. Flattened BCH Codeword Mapping (512 Bytes + 104 Bits)

	Message M(x)			ECC R(x)		
Bit Number	M4095	...	M0	R103	...	R0

If the message is extended by the addition of spare bytes to be protected by the same ECC, the principle is still valid. For example, a 3-byte extension of the message gives a polynomial message M(x) of degree ((512 + 3) × 8) – 1 = 4119, for a total of 3 + 13 = 16 spare bytes of spare, all protected as part of the same codeword.

The message and the ECC bits are manipulated and mapped in the GPMC byte-oriented system. The ECC bits are stored in the following registers (where i = 0 to 3):

- GPMC_BCH_RESULT0_i
- GPMC_BCH_RESULT1_i
- GPMC_BCH_RESULT2_i
- GPMC_BCH_RESULT3_i

12.3.3.4.11.3.2.2.1 Memory Mapping of Data Message

The data message mapping must follow the following rules:

- Bit endianness within a byte is little-endian; that is, the bytes LSB is also the lowest-degree polynomial parameter: a byte b7-b0 (with b0 the LSB) represents a segment of polynomial $b7 * x^{(7+i)} + b6 * x^{(6+i)} + ... + b0 * x^i$

- The message is mapped in the NAND starting with the highest-order parameters, that is, in the lowest addresses of a NAND page.
- Byte endianness within the 16-bit words in the NAND is big-endian (that is, the same message mapped in 8- and 16-bit memories has the same content at the same byte address).

Note

The BCH module has no visibility over actual addresses. The most important point is the sequence of data words the BCH sees. However, the NAND page is always scanned incrementally in read and write accesses, which produces the mapping patterns described in the following.

Table 12-256 and Table 12-257 describe the mapping of the same 512-byte vector (typically, a BCH message) in the NAND memory space. The byte address is only an offset module 512 (0x200), because the same page may contain several contiguous 512-byte sectors (BCH blocks). The LSB and MSB are, respectively, the bits M0 and M(2^{12}–1) of the codeword mapping discussed previously. In both cases the data vectors are aligned; that is, their boundaries coincide with the RAM data word boundaries.

Table 12-268. Aligned Message Byte Mapping in 8-Bit NAND

Byte Offset	8-Bit Word
0x000	(MSB) Byte 511 (0x1FF)
0x001	Byte 510 (0x1FE)
...	...
0x1FF	Byte 0 (0x0) (LSB)

Table 12-269. Aligned Message Byte Mapping in 16-Bit NAND

Byte Offset	16-Bit Word MSB	16-Bit Word LSB
0x000	Byte 510 (0x1FE)	(MSB) Byte 511 (0x1FF)
0x002	Byte 508 (0x1FC)	Byte 509 (0x1FD)
...	...	...
0x1FE	Byte 0 (0x0)	(LSB) Byte 1 (0x1)

Table 12-258 through Table 12-263 list the mapping in memory of arbitrarily-sized messages, starting on access (byte or 16-bit word) boundaries for more clarity. Note that message may actually start and stop on arbitrary nibbles. A nibble is a 4-bit entity. The unused nibbles are not discarded, and they can still be used by the BCH module, but as part of the next message section (for example, on the ECC of another sector).

Table 12-270. Aligned Nibble Mapping of Message in 8-Bit NAND

Byte Offset	8-Bit Word	
	4-Bit Most Significant Nibble	4-Bit Least Significant Nibble
1	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-3	Nibble S-4
...	...	...
S/2 – 2	Nibble 3	Nibble 2
S/2 – 1	Nibble 1	Nibble 0 (LSB)

Table 12-271. Misaligned Nibble Mapping of Message in 8-Bit NAND

Byte Offset	8-Bit Word	
	4-Bit Most Significant Nibble	4-Bit Least Significant Nibble
1	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-3	Nibble S-4
...	...	...
(S + 1) / 2 – 2	Nibble 2	Nibble 1

Table 12-271. Misaligned Nibble Mapping of Message in 8-Bit NAND (continued)

Byte Offset	8-Bit Word	
(S + 1) / 2 – 1	Nibble 0 (LSB)	

Table 12-272. Aligned Nibble Mapping of Message in 16-Bit NAND

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		**4-Bit Least Significant Nibble**	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
S/2 – 4	Nibble 5	Nibble 4	Nibble 7	Nibble 6
S/2 – 2	Nibble 1	Nibble 0 (LSB)	Nibble 3	Nibble 2

Table 12-273. Misaligned Nibble Mapping of Message in 16-Bit NAND (1 Unused Nibble)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		**4-Bit Least Significant Nibble**	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 1) / 2 – 4	Nibble 4	Nibble 3	Nibble 6	Nibble 5
(S + 1) / 2 – 2	Nibble 0 (LSB)		Nibble 2	Nibble 1

Table 12-274. Misaligned Nibble Mapping of Message in 16-Bit NAND (2 Unused Nibbles)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		**4-Bit Least Significant Nibble**	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 2) / 2 – 4	Nibble 3	Nibble 2	Nibble 5	Nibble 4
(S + 2) / 2 – 2			Nibble 1	Nibble 0 (LSB)

Table 12-275. Misaligned Nibble Mapping of Message in 16-Bit NAND (3 Unused Nibbles)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		**4-Bit Least Significant Nibble**	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 3) / 2 – 4	Nibble 2	Nibble 1	Nibble 4	Nibble 3
(S + 3) / 2 – 2			Nibble 0 (LSB)	

Many other cases exist than those given in the previous tables; for example, where the message does not start on a word boundary.

12.3.3.4.11.3.2.2.2 Memory-Mapping of the ECC

The ECC (or remainder) is presented by the BCH module as a single 104-bit (or 52-bit), little-endian vector. Software must fetch those 13 bytes (or 6 bytes) from the module interface and then store them to the spare area (page write) in the NAND or to an intermediate buffer for comparison with the stored ECC (page read). There are no constraints on the ECC mapping inside the spare area: it is software-controlled.

It is advised, however, to maintain a coherence in the respective formats of the message or the ECC remainder once they have been read out of the NAND. The error correction algorithm works from the complete codeword (concatenated message and remainder) once an error is detected. The creation of this codeword must be made as straightforward as possible.

There are cases in which the same NAND access contains both data and the ECC protecting that data. This is the case when the data/ECC boundary (which can be on any nibble) does not coincide with an access boundary. The ECC is calculated on the fly following the write. In that case, the write must also contain part of the ECC because it is impossible to insert the ECC on the fly. Instead:

- During the initial page write (BCH encoding), the ECC is replaced by dummy bits. The BCH encoder is by definition turned OFF during the ECC section, so the BCH result is unmodified.
- During a second phase, the ECC is written to the correct location, next to the actual data.
- The completed line buffer is then written to the NAND array.

12.3.3.4.11.3.2.2.3 Wrapping Modes

For a given wrapping mode, the module automatically goes through a specific number of sections as data is being fed into the module. For each section, the BCH core can be enabled (in which case the data is fed to the BCH divider) or not (in which case the BCH simply counts to the end of the section). When enabled, the data is added to the ongoing calculation for a given sector number (for example, number 0).

Wrapping modes are described as follows. To better understand and see the real-life read and write sequences implemented with each mode, see Section 12.3.3.4.11.3.2.3 , *Supported NAND Page Mappings and ECC Schemes*.

For each mode:

- A sequence describes the mode in pseudo language, with, for each section, the size and the buffer used for ECC processing (if ON). The programmable lengths are size, size0, and size1.
- A checksum condition is given. If the checksum condition is not respected for a given mode, the module behavior is unpredictable. S is the number of sectors in the page; size0 and size1 are the section sizes programmed for the mode, in nibbles.

Wrapping modes 8 through 11 insert a 1-nibble padding where the BCH processing is OFF. This is intended for t = 4 ECC, where ECC is 6 bytes long and the ECC area is expected to include (at least) 1 unused nibble to remain byte-aligned.

12.3.3.4.11.3.2.2.3.1 Manual Mode (0x0)

This mode is intended for short sequences, added manually to a given buffer through the software data port input. A complete page may be built out of several such sequences.

To process an arbitrary sequence of 4-bit nibbles, accesses to the software data port, containing the appropriate data, must be made. If the sequence end does not coincide with an access boundary (for example, to process 5 nibbles = 20 bits in 16-bit access mode) and those nibbles must be skipped, a number of unused nibbles must be programmed in GPMC_ECC_SIZE_CONFIG[31-22] ECCSIZE1 In the same example, 5 nibbles to process + 3 to discard = 8 nibbles = 2 × 16-bit accesses. Software must set:

- GPMC_ECC_SIZE_CONFIG[21-12] ECCSIZE0 = 0x5
- GPMC_ECC_SIZE_CONFIG[31-22] ECCSIZE1 = 0x3

Note

In the following figures, size and size0 are the same parameter.

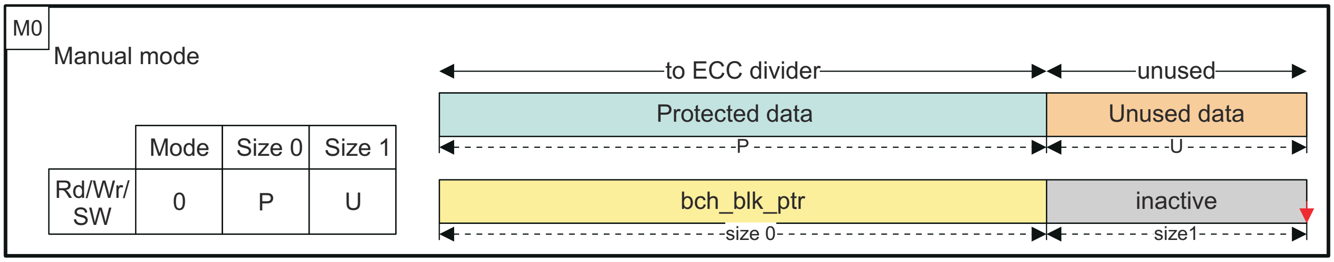

Figure 12-199. Manual Mode Sequence and Mapping

Section processing sequence:

- One time with buffer
  - size0 nibbles of data, processing ON
  - size1 nibbles of unused data, processing OFF

Checksum: size0 + size1 nibbles must fit in a whole number of accesses.

In the following sections, S is the number of sectors in the page.

12.3.3.4.11.3.2.2.3.2 Mode 0x1

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + size1)

12.3.3.4.11.3.2.2.3.3 Mode 0xA (10)

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
  - 1 nibble pad spare, processing OFF
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + 1 + size1)

12.3.3.4.11.3.2.2.3.4 Mode 0x2

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + size1)

12.3.3.4.11.3.2.2.3.5 Mode 0x3

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – size1)

12.3.3.4.11.3.2.2.3.6 Mode 0x7

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat S times (no buffer used)
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = size0 + (S – size1)

12.3.3.4.11.3.2.2.3.7 Mode 0x8

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – (1 + size1))

12.3.3.4.11.3.2.2.3.8 Mode 0x4

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time (no buffer used)
  - size0 nibbles spare, processing OFF
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – size1)

12.3.3.4.11.3.2.2.3.9 Mode 0x9

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time (no buffer used)
  - size0 nibbles spare, processing OFF
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – (1 + size1))

12.3.3.4.11.3.2.2.3.10 Mode 0x5

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + size1)

12.3.3.4.11.3.2.2.3.11 Mode 0xB (11)

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + 1 + size1)

12.3.3.4.11.3.2.2.3.12 Mode 0x6

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat S times (no buffer used)
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + size1)

12.3.3.4.11.3.2.3 Supported NAND Page Mappings and ECC Schemes

The following rules apply to the entire mapping description:

- Main data area (sectors) size is hardcoded to 512 bytes.
- Spare area size is programmable.
- All page sections (of main area data bytes, protected spare bytes, unprotected spare bytes, and ECC) are defined as explained in Section 12.3.3.4.11.3.2.2.1 , *Memory Mapping of Data Message*.

Each of the following sections gives a NAND page mapping example (per-sector spare mappings, pooled spare mapping, per-sector spare mapping, with ECC separated at the end of the page).

In the mapping diagrams, sections that belong to the same BCH codeword have the same color (blue or green); unprotected sections are not covered (orange) by the BCH scheme.

Below each mapping diagram, a write (encoding) and read (decoding: syndrome generation) sequence is given, with the number of the active buffers at each point in time (yellow). In the inactive zones (grey), no computing is taking place but the data counter is still active.

In Figure 12-200 through Figure 12-202, the tables on the left summarize the mode, size0, and size1 parameters to program for, respectively, write and read processing of a page, with the given mapping, where:

- P is the size of spare byte section Protected by the ECC (in nibbles)
- U is the size of spare byte section Unprotected by the ECC (in nibbles)
- E is the size of the ECC (in nibbles)
- S is the number of Sectors per page (two in the current diagrams)

Each time the processing of a BCH block is complete (ECC calculation for write/encoding, syndrome generation for read/decoding, indicated by red arrows), the update pointer is pulsed. The processing for block 0 can be the first or the last to complete, depending on the NAND page mapping and operation (read or write). All examples show a page size of 1 KB + spares; that is, S = 2 sectors of 512 bytes. The same principles can be extended to larger pages by adding more sectors.

The actual BCH codeword size is used during the error location work to restrict the search range: by definition, errors can happen only in the codeword that was actually written to the NAND, not in the mathematical codeword of $n = 2^{13} – 1 = 8191$ bits; that codeword (higher-order bits) is all-zero and implicit during computations.

The actual BCH codeword size depends on the mode, the programmed sizes, and the sector number (all sizes in nibbles):

- Spares mapped and protected per sector (below: see M1-M2-M3-M9-M10):
  - All sectors: (512) + P + E
- Spares pooled and protected by sector 0 (below: see M5-M6):
  - Sector 0 codeword: (512) + P + E
  - Other sectors: (512) + E
- Unprotected spares (below: see M4-M7-M8-M11-M12):
  - All codewords (512) + E

12.3.3.4.11.3.2.3.1 Per-Sector Spare Mappings

In these schemes, each 512-byte sector of the main area has its own dedicated section of the spare area. The spare area of each sector is composed of:

- ECC, which must be located after the data it protects
- Other data, which may or may not be protected by the ECC for its sector.

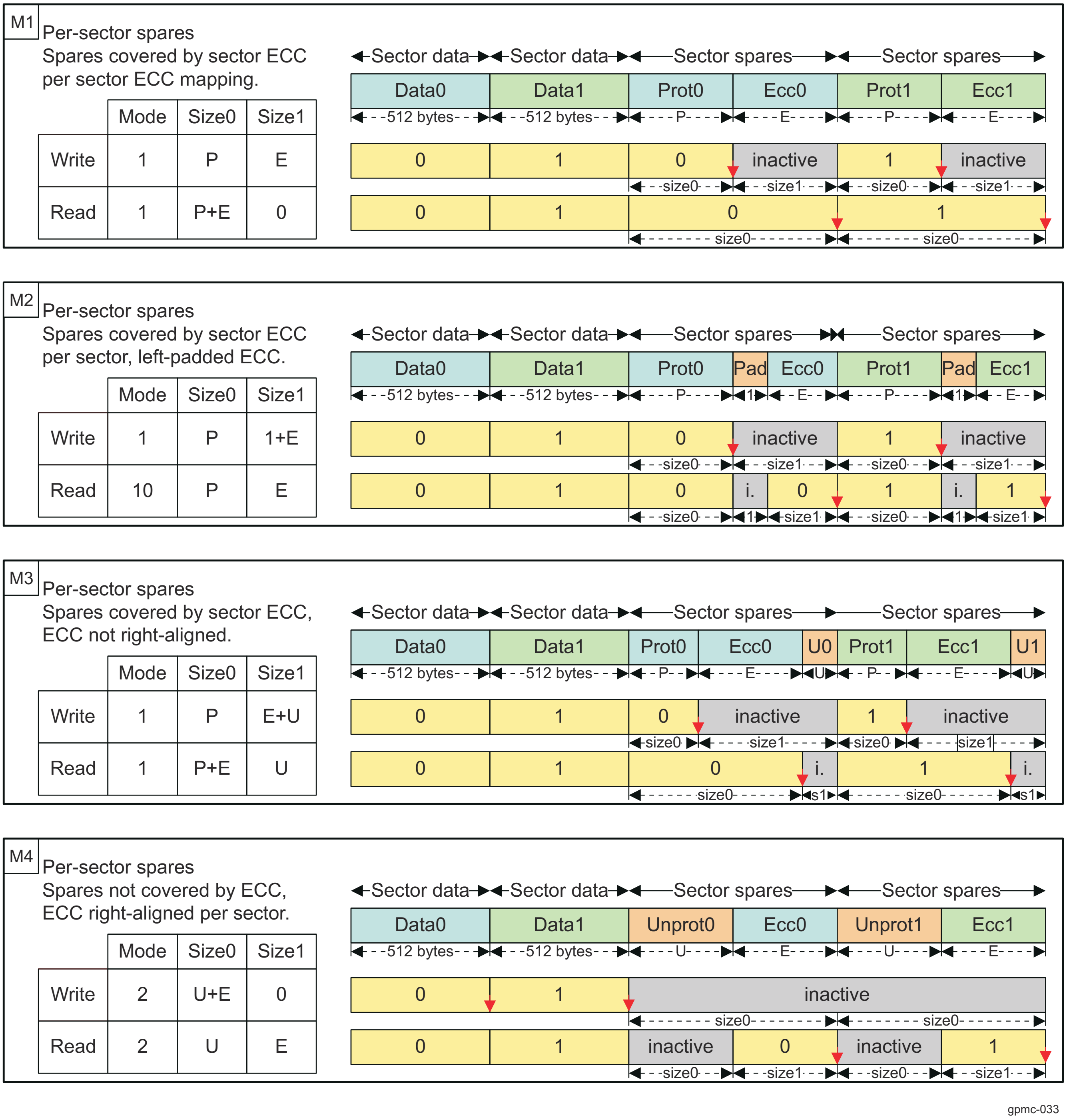

M1 Per-sector spares
Spares covered by sector ECC
per sector ECC mapping.

	Mode	Size0	Size1
Write	1	P	E
Read	1	P+E	0

M2 Per-sector spares
Spares covered by sector ECC
per sector, left-padded ECC.

	Mode	Size0	Size1
Write	1	P	1+E
Read	10	P	E

M3 Per-sector spares
Spares covered by sector ECC,
ECC not right-aligned.

	Mode	Size0	Size1
Write	1	P	E+U
Read	1	P+E	U

M4 Per-sector spares
Spares not covered by ECC,
ECC right-aligned per sector.

	Mode	Size0	Size1
Write	2	U+E	0
Read	2	U	E

Figure 12-200. NAND Page Mapping and ECC: Per-Sector Schemes

12.3.3.4.11.3.2.3.2 Pooled Spare Mapping

In the following schemes, the spare area is pooled for the page.

- The ECC of each sector is aligned at the end of the spare area.
- The non-ECC spare data may or may not be covered by the ECC of sector 0.

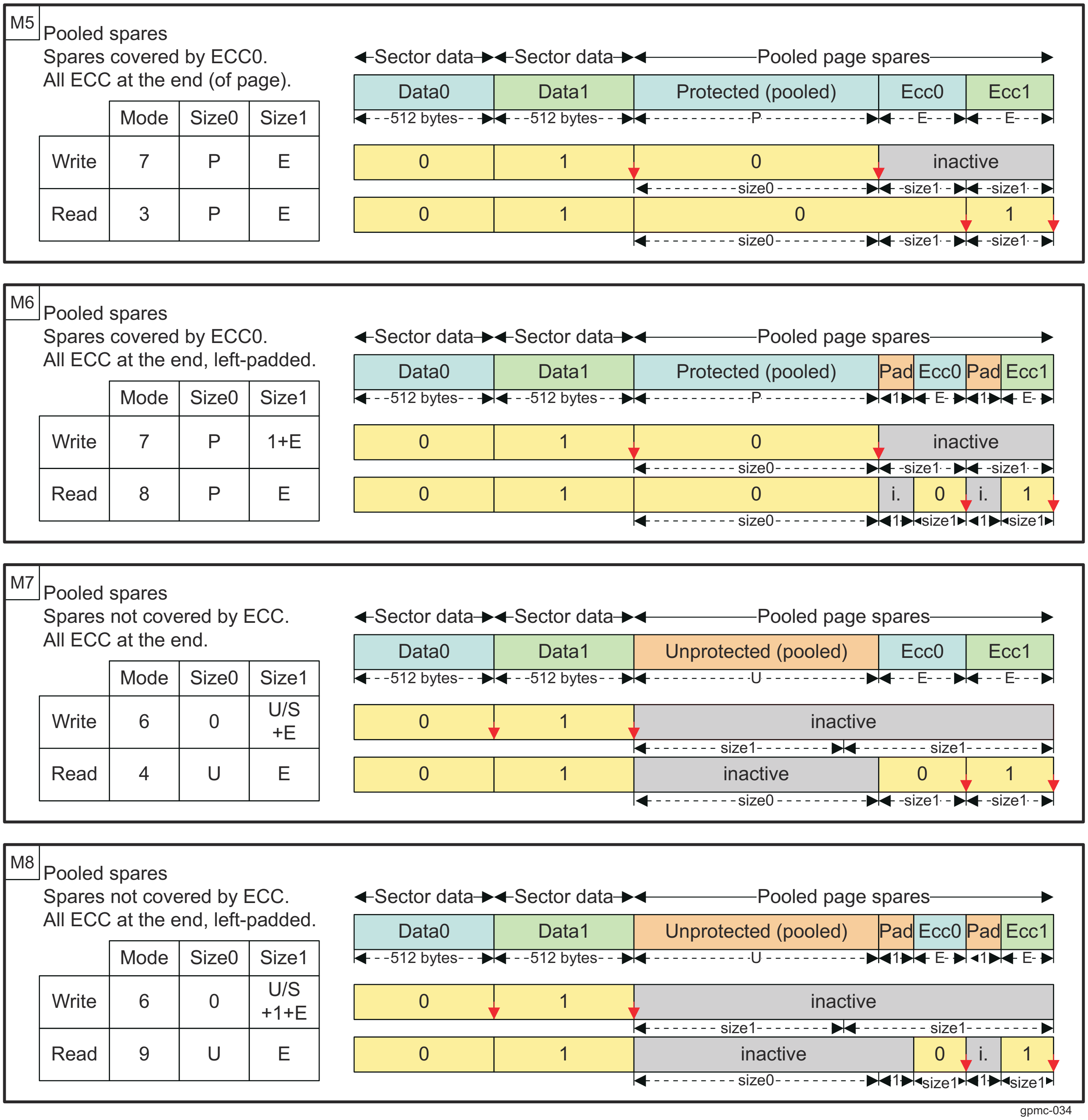

M5

	Mode	Size0	Size1
Write	7	P	E
Read	3	P	E

M6

	Mode	Size0	Size1
Write	7	P	1+E
Read	8	P	E

M7

	Mode	Size0	Size1
Write	6	0	U/S +E
Read	4	U	E

M8

	Mode	Size0	Size1
Write	6	0	U/S +1+E
Read	9	U	E

Figure 12-201. NAND Page Mapping and ECC: Pooled Spare Schemes

12.3.3.4.11.3.2.3.3 Per-Sector Spare Mapping, with ECC Separated at the End of the Page

In these schemes, each 512-byte sector of the main area is associated with two sections of the spare area.

- ECC section, all aligned at the end of the page
- Other data section, aligned before the ECCs, each of which may or may not be protected by the ECC for its sector.

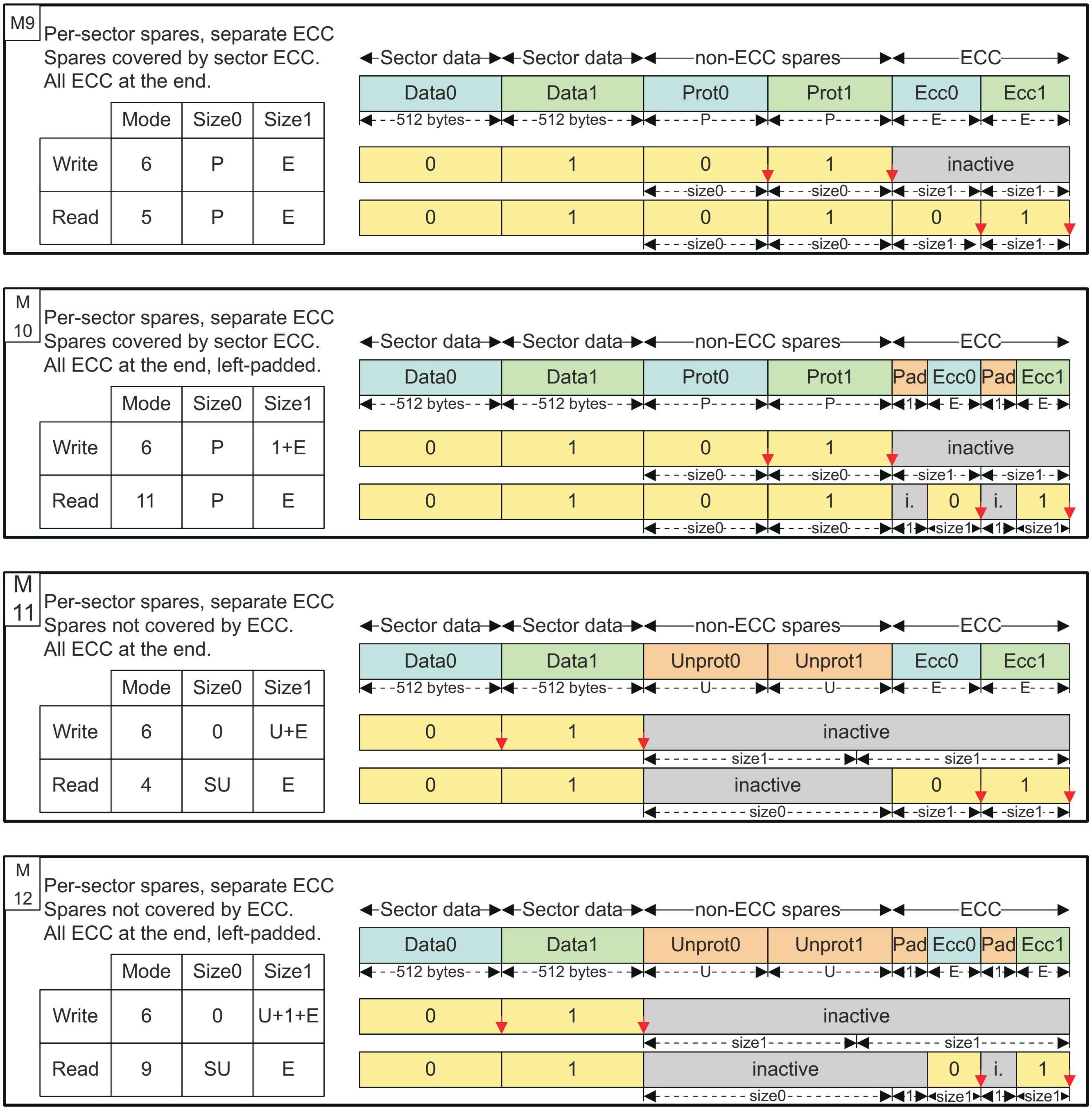

M9

	Mode	Size0	Size1
Write	6	P	E
Read	5	P	E

M10

	Mode	Size0	Size1
Write	6	P	1+E
Read	11	P	E

M11

	Mode	Size0	Size1
Write	6	0	U+E
Read	4	SU	E

M12

	Mode	Size0	Size1
Write	6	0	U+1+E
Read	9	SU	E

gpmc_035

Figure 12-202. NAND Page Mapping and ECC: Per-Sector Schemes, With Separate ECC

12.3.3.4.11.4 Prefetch and Write-Posting Engine

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

NAND device data access cycles are usually much slower than the CPU system frequency; such NAND read or write accesses issued by the processor affect the overall system performance, especially considering long read or write sequences required for NAND page loading or programming. To minimize this effect on system performance, the GPMC includes a prefetch and write-posting engine, which can be used to read from or write to any chip-select location in a buffered manner.

The prefetch and write-posting engine is a simplified embedded-access requester that presents requests to the access engine on a user-defined chip-select target. The access engine interleaves these requests with any request coming from the interconnect interface; as a default, the prefetch and write-posting engine has the lowest priority.

The prefetch and write-posting engine is dedicated to data-stream access (as opposed to random data access); thus, it is primarily dedicated to NAND support. The engine does not include an address generator; the request is limited to chip-select target identification. It includes a 64-byte FIFO associated with a DMA request synchronization line, for optimal DMA-based use.

The prefetch and write-posting engine uses an embedded 64-byte (32 16-bit word) FIFO to prefetch data from the NAND device in read mode (prefetch mode) or to store host data to be programmed into the NAND device in write mode (write-posting mode). The FIFO draining and filling (read and write) can be controlled by a device host processor through interrupt synchronization (an interrupt is triggered whenever a programmable threshold is reached) or by a device DMA module through DMA request synchronization, with a programmable request byte size in prefetch or posting mode.

The prefetch and write-posting engine includes a single memory pool. Therefore, only one mode, read or write, can be used at any given time. In other words, the prefetch and write-posting engine is a single-context engine that can be allocated to only one chip-select at a time for a read prefetch or a write-posting process.

The engine does not support atomic command and address phase programming and is limited to linear memory read or write access. As a consequence, it is limited to NAND data-stream access. The engine depends on the NAND software driver to control block and page opening with the correct data address pointer initialization, before the engine can read from or write to the NAND memory device.

Once started, engine data read and write sequencing is based solely on FIFO location availability and until the total programmed number of bytes is read or written.

Any host-concurrent accesses to a different chip-select are correctly interleaved with ongoing engine accesses. The engine has the lowest priority access so that host accesses to a different chip-select do not suffer a large latency.

A round-robin arbitration scheme can be enabled to ensure minimum bandwidth to the prefetch and write-posting engine in the case of back-to-back direct memory requests to a different chip-select. If the GPMC_PREFETCH_CONFIG1[23] PFPWENROUNDROBIN bit is enabled, the arbitration grants the prefetch and write-posting engine access to the GPMC bus for a number of requests programmed in the GPMC_PREFETCH_CONFIG1[19-16] PFPWWEIGHTEDPRIO bit field.

The prefetch/write-posting engine read or write request is routed to the access engine with the chip-select destination ID. After the required arbitration phase, the access engine processes the request as a single access with the data access size equal to the device size specified in the corresponding chip-select configuration.

Note

The destination chip-select configuration must be set to the NAND protocol-compatible configuration for which address lines are not used (the address bus is not changed from its current value). Selecting a different chip-select configuration can produce undefined behavior.

12.3.3.4.11.4.1 General Facts About the Engine Configuration

The engine can be configured only if the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit is deasserted.

The engine must be correctly configured in prefetch or write-posting mode and must be linked to a NAND chip-select before it can be started. The chip-select is linked using the GPMC_PREFETCH_CONFIG1[26-24] ENGINECSSELECTOR bit field.

In prefetch and write-posting modes, the engine uses byte or 16-bit word access requests, respectively, for an 8- or 16-bit-wide NAND device attached to the linked chip-select. The FIFOTHRESHOLD and TRANSFERCOUNT bit fields must be programmed accordingly as a number of bytes.

When the GPMC_PREFETCH_CONFIG1[7] ENABLEENGINE bit is set, the FIFO entry on the interconnect port side is accessible at any address in the associated chip-select memory region. When the ENABLEENGINE bit is set, any host access to this chip-select is rerouted to the FIFO input. Directly accessing the NAND device linked to this chip-select from the host is still possible through the following registers (where i = 0 to 3):

- GPMC_NAND_COMMAND_i
- GPMC_NAND_ADDRESS_i
- GPMC_NAND_DATA_i

The FIFO entry on the interconnect port can be accessed with byte, 16-bit word, or 32-bit word access size, according to little-endian format, even though the FIFO input is 32 bits wide.

The FIFO control is made easier through the use of interrupts or DMA requests associated with the FIFOTHRESHOLD bit field. The GPMC_PREFETCH_STATUS[30-24] FIFOPOINTER bit field monitors the number of available bytes to be read in prefetch mode or the number of free empty slots that can be written in write-posting mode. The GPMC_PREFETCH_STATUS[13-0] COUNTVALUE bit field monitors the number of remaining bytes to be read or written by the engine according to the value of the TRANSFERCOUNT bit field. The FIFOPOINTER and COUNTVALUE bit fields are always expressed as a number of bytes even if a 16-bit-wide NAND device is attached to the linked chip-select.

In prefetch mode, when the FIFOPOINTER equals 0 (that is, the FIFO is empty), a host read access receives the byte last read from the FIFO as its response. In case of 32-bit word or 16-bit word read accesses, the last byte read from the FIFO is copied the required number of times to fit the requested word size. In write-posting mode, when the FIFOPOINTER equals 0 (that is, the FIFO is full), a host write overwrites the last FIFO byte location. There is no underflow or overflow error reporting in the GPMC.

12.3.3.4.11.4.2 Prefetch Mode

The prefetch mode is selected when the GPMC_PREFETCH_CONFIG1[0] ACCESSMODE bit is cleared.

The NAND software driver must issue the block and page opening (READ) command with the correct data address pointer initialization before the engine can be started to read from the NAND memory device. The engine is started by asserting the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit. The STARTENGINE bit automatically clears when the prefetch process completes.

If required, the ECC calculator engine must be initialized (that is, reset, configured, and enabled) before the prefetch engine is started so that the ECC is computed correctly on all data read by the prefetch engine.

When the GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE bit is cleared, the prefetch engine starts requesting data as soon as the STARTENGINE bit is set. If using this configuration, the host must monitor the NAND device-ready pin so that it sets the STARTENGINE bit only when the NAND device is in a ready state (that is, data is valid for prefetching).

When the SYNCHROMODE bit is set, the prefetch engine starts requesting data when an active-to-inactive WAIT signal transition is detected. The transition detector must be cleared before any transition detection (see Section 12.3.3.4.11.2.2 , *Ready Pin Monitored by Hardware Interrupt*). The GPMC_PREFETCH_CONFIG1[5-4] WAITPINSELECTOR bit field selects which GPMC_WAIT pin edge detector triggers the prefetch engine in this synchronized mode.

If the STARTENGINE bit is set after the NAND address phase (page opening command), the engine is effectively started only after the actual NAND address phase completion. To prevent GPMC stall during this NAND address phase, set the STARTENGINE bit before NAND address phase completion when in synchronized mode. The prefetch engine starts when an active-to-inactive WAIT signal transition is detected. The STARTENGINE bit is automatically cleared on prefetch process completion.

The prefetch engine issues a read request to fill the FIFO with the amount of data specified by the GPMC_PREFETCH_CONFIG2[13-0] TRANSFERCOUNT bit field.

Table 12-264 describes the prefetch mode configuration.

Table 12-276. Prefetch Mode Configuration

Bit Field	Register	Value	Comments
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	0	Prefetch engine can be configured only if STARTENGINE is set to 0.
ENGINECSSELECTOR	GPMC_PREFETCH_CONFIG1[26-24]	0 to 3	Selects the chip-select associated with a NAND device where the prefetch engine is active.
ACCESSMODE	GPMC_PREFETCH_CONFIG1[0]	0	Selects prefetch mode
FIFOTHRESHOLD	GPMC_PREFETCH_CONFIG1[14-8]		Selects the maximum number of bytes read or written by the host on DMA or interrupt request
TRANSFERCOUNT	GPMC_PREFETCH_CONFIG2[13-0]		Selects the number of bytes to be read or written by the engine to the selected chip-select
SYNCHROMODE	GPMC_PREFETCH_CONFIG1[3]	0/1	Selects when the engine starts the access to the chip-select
WAITPINSELECT	GPMC_PREFETCH_CONFIG1[17-16]	0 to 1	Selects WAIT pin edge detector (if GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE = 0x1)
ENABLEOPTIMIZEDACCESS	GPMC_PREFETCH_CONFIG1[27]	0/1	See Section 12.3.3.4.11.4.6 , *Optimizing NAND Access Using the Prefetch and Write-Posting Engine*.
CYCLEOPTIMIZATION	GPMC_PREFETCH_CONFIG1[30-28]		Number of clock cycle removed to timing parameters
ENABLEENGINE	GPMC_PREFETCH_CONFIG1[7]	1	Engine enabled
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	1	Starts the prefetch engine

12.3.3.4.11.4.3 FIFO Control in Prefetch Mode

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

The FIFO can be drained directly by a device host processor or a DMA module channel.

In draining mode, the FIFO status can be monitored through the GPMC_PREFETCH_STATUS[30-24] FIFOPOINTER bit field or through the GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bit. The FIFOPOINTER indicates the current number of available data to be read; FIFOTHRESHOLDSTATUS set to 1 indicates that at least FIFOTHRESHOLD bytes are available from the FIFO.

An interrupt can be triggered by the GPMC if the GPMC_IRQENABLE[0] FIFOEVENTENABLE bit is set. The FIFO interrupt event is logged, and the GPMC_IRQSTATUS[0] FIFOEVENTSTATUS bit is set. To clear the interrupt, all the available bytes must be read, or at least enough bytes to get below the programmed FIFO threshold, and the FIFOEVENTSTATUS bit must be cleared to enable further interrupt events. The FIFOEVENTSTATUS bit must always be reset before asserting the FIFOEVENTENABLE bit to clear any out-of-date logged interrupt event. This interrupt generation must be enabled after enabling the STARTENGINE bit.

Prefetch completion can be monitored through the GPMC_PREFETCH_STATUS[13-0] COUNTVALUE bit field. COUNTVALUE indicates the number of currently remaining data to be requested according to the TRANSFERCOUNT value. An interrupt can be triggered by the GPMC when the prefetch process is complete (that is, COUNTVALUE equals 0) if the GPMC_IRQENABLE[1] TERMINALCOUNTEVENTENABLE bit is set.

At prefetch completion, the TERMINALCOUNT interrupt event is also logged, and the GPMC_IRQSTATUS[1] TERMINALCOUNTSTATUS bit is set. To clear the interrupt, the TERMINALCOUNTSTATUS bit must be cleared. The TERMINALCOUNTSTATUS bit must always be cleared prior to asserting the TERMINALCOUNTEVENTENABLE bit to clear any out-of-date logged interrupt event.

Note

The COUNTVALUE value is valid only when the prefetch engine is active (started), and an interrupt is only triggered when COUNTVALUE reaches 0, that is, when the prefetch engine automatically goes from an active to an inactive state.

The number of bytes to be prefetched (programmed in TRANSFERCOUNT) must be a multiple of the programmed FIFOTHRESHOLD to trigger the correct number of interrupts allowing a deterministic and transparent FIFO control. If this guideline is respected, the number of ISR accesses is always required and the FIFO is always empty after the last interrupt is triggered. In other cases, the TERMINALCOUNT interrupt must be used to read the remaining bytes in the FIFO (the number of remaining bytes being lower than the FIFOTHRESHOLD value).

In DMA draining mode, the GPMC_PREFETCH_CONFIG1[2] DMAMODE bit must be set so that the GPMC issues a DMA hardware request when at least FIFOTHRESHOLD bytes are ready to be read from the FIFO. The DMA channel that owns this DMA request must be programmed so that the number of bytes programmed in FIFOTHRESHOLD is read from the FIFO during the DMA request process. The DMA request is kept active until this number of bytes has effectively been read from the FIFO, and no other DMA request can be issued until the ongoing active request is complete.

In prefetch mode, the TERMINALCOUNT event is also a source of DMA requests if the number of bytes to be prefetched is not a multiple of FIFOTHRESHOLD, the remaining bytes in the FIFO can be read by the DMA channel using the last DMA request. This assumes that the number of remaining bytes to be read is known and controlled through the DMA channel programming model.

Any potentially active DMA request is cleared when the prefetch engine goes from inactive-to-active prefetch (the STARTENGINE bit is set to 1). The associated DMA channel must always be enabled after setting the STARTENGINE bit so that the out-of-date active DMA request does not trigger spurious DMA transfers.

12.3.3.4.11.4.4 Write-Posting Mode

The write-posting mode is selected when the GPMC_PREFETCH_CONFIG1[0] ACCESSMODE bit is set.

The NAND software driver must issue the correct address pointer initialization command (page program) before the engine can start writing data into the NAND memory device. The engine starts when the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit is set to 1. The STARTENGINE bit clears automatically when posting completes. When all data have been written to the NAND memory device, the NAND software driver must issue the second cycle program command and monitor the status for programming process completion (adding ECC handling, if required).

If used, the ECC calculator engine must be started (configured, reset, and enabled) before the posting engine is started so that the ECC parities are calculated properly on all data written by the prefetch engine to the associated chip-select.

In write-posting mode, the GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE bit must be cleared so that posting starts as soon as the STARTENGINE bit is set and the FIFO is not empty.

If the STARTENGINE bit is set after the NAND address phase (page program command), the STARTENGINE setting is effective only after the actual NAND command completion. To prevent GPMC stall during this NAND command phase, set the STARTENGINE bit field before the NAND address completion and ensure that the associated DMA channel is enabled after the NAND address phase.

The posting engine issues a write request when valid data are available from the FIFO and until the programmed GPMC_PREFETCH_CONFIG2[13-0] TRANSFERCOUNT accesses are complete.

The STARTENGINE bit clears automatically when posting completes. When all data have been written to the NAND memory device, the NAND software driver must issue the second cycle program command and monitor the status for programming process completion. The closing program command phase must be issued only when the full NAND page has been written into the NAND flash write buffer, including the spare area data and the ECC parities, if used.

Table 12-265 describes the write-posting configuration.

Table 12-277. Write-Posting Mode Configuration

Bit Field	Register	Value	Comments
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	0	Write-posting engine can be configured only if STARTENGINE is set to 0.
ENGINECSSELECTOR	GPMC_PREFETCH_CONFIG1[26-24]	0 to 3	Selects the chip-select associated with a NAND device where the prefetch engine is active
ACCESSMODE	GPMC_PREFETCH_CONFIG1[0]	1	Selects write-posting mode
FIFOTHRESHOLD	GPMC_PREFETCH_CONFIG1[14-8]		Selects the maximum number of bytes read or written by the host on DMA or interrupt request
TRANSFERCOUNT	GPMC_PREFETCH_CONFIG2[13-0]		Selects the number of bytes to be read or written by the engine from/to the selected chip-select
SYNCHROMODE	GPMC_PREFETCH_CONFIG1[3]	0	Engine starts the access to chip-select as soon as STARTENGINE is set.
ENABLEOPTIMIZEDACCESS	GPMC_PREFETCH_CONFIG1[27]	0/1	See Section 12.3.3.4.11.4.6 , *Optimizing NAND Access Using the Prefetch and Write-Posting Engine*.
CYCLEOPTIMIZATION	GPMC_PREFETCH_CONFIG1[30-28]		
ENABLEENGINE	GPMC_PREFETCH_CONFIG1[7]	1	Engine enabled
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	1	Starts the prefetch engine

12.3.3.4.11.4.5 FIFO Control in Write-Posting Mode

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

The FIFO can be filled directly by a device host processor or a DMA module channel.

In filling mode, the FIFO status can be monitored through the FIFOPOINTER or through the GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bit. FIFOPOINTER indicates the current number of available free byte places in the FIFO, and the FIFOTHRESHOLDSTATUS bit, when set, indicates that at least FIFOTHRESHOLD free byte places are available in the FIFO.

An interrupt can be issued by the GPMC if the GPMC_IRQENABLE[0] FIFOEVENTENABLE bit is set. When the interrupt is fired, the GPMC_IRQSTATUS[0] FIFOEVENTSTATUS bit is set. To clear the interrupt, enough bytes must be written to fill the FIFO or to get below the programmed threshold, and the FIFOEVENTSTATUS bit must be cleared to get further interrupt events. The FIFOEVENTSTATUS bit must always be cleared before asserting the FIFOEVENTENABLE bit to clear any out-of-date logged interrupt event. This interrupt must be enabled after enabling the STARTENGINE bit.

The posting completion can be monitored through the GPMC_PREFETCH_STATUS[13-0] COUNTVALUE bit field. COUNTVALUE indicates the current number of remaining data to be written based on the value of the TRANSFERCOUNT bit field. An interrupt is issued by the GPMC when the write-posting process completes (that is, COUNTVALUE equal to 0) if the GPMC_IRQENABLE[1] TERMINALCOUNTEVENTENABLE bit is set. When the interrupt is fired, the GPMC_IRQSTATUS[1] TERMINALCOUNTSTATUS bit is set. To clear the interrupt, the

TERMINALCOUNTSTATUS bit must be cleared. The TERMINALCOUNTSTATUS bit must always be cleared before asserting the TERMINALCOUNTEVENTENABLE bit to clear any out-of-date logged interrupt event.

Note

The value of the COUNTVALUE bit field is valid only if the write-posting engine is active and started, and an interrupt is issued only when COUNTVALUE reaches 0; that is, when the posting engine automatically goes from active to inactive.

In DMA filling mode, the DMAMode bit field in the GPMC_PREFETCH_CONFIG1[2] DMAMODE bit must be set so that the GPMC issues a DMA hardware request when at least FIFOTHRESHOLD bytes-free places are available in the FIFO. The DMA channel that owns this DMA request must be programmed so that a number of bytes equal to the value programmed in the FIFOTHRESHOLD bit field are written into the FIFO during the DMA access. The DMA request remains active until the associated number of bytes has effectively been written into the FIFO, and no other DMA request can be issued until the ongoing active request completes.

Any potentially active DMA request is cleared when the prefetch engine goes from inactive-to-active prefetch (STARTENGINE set to 1). The associated DMA channel must always be enabled after setting the STARTENGINE bit so that an out-of-date active DMA request does not trigger spurious DMA transfers.

In write-posting mode, DMA or CPU fills the FIFO with no consideration for the associated byte enables. Any byte stored in the FIFO is written into the memory device.

12.3.3.4.11.4.6 Optimizing NAND Access Using the Prefetch and Write-Posting Engine

Access time to a NAND memory device can be optimized for back-to-back accesses if the associated nCS signal is not deasserted between accesses. The GPMC access engine can track prefetch engine accesses to optimize the access timing parameter programmed for the allocated chip-select, if no accesses to other chip-selects (that is, interleaved accesses) occur. Similarly, the access engine also eliminates CYCLE2CYCLEDELAY even if CYCLE2CYCLESAMECSEN is set. This capability is limited to the prefetch and write-posting engine accesses, and accesses to a NAND memory device (through the defined chip-select memory region or through the GPMC_NAND_DATA_i location, where i = 0 to 3) are never optimized.

The GPMC_PREFETCH_CONFIG1[27] ENABLEOPTIMIZEDACCESS bit must be set to enable optimized accesses. To optimize access time, the GPMC_PREFETCH_CONFIG1[30-28] CYCLEOPTIMIZATION bit field defines the number of GPMC_FCLK cycles to be suppressed from the following timing parameters:

- RDCYCLETIME
- WRCYCLETIME
- RDACCESSTIME
- WRACCESSTIME
- CSOFFTIME
- ADVOFFTIME
- OEOFFTIME
- WEOFFTIME

Figure 12-203 shows that in the case of back-to-back accesses to the NAND flash through the prefetch engine, CYCLE2CYCLESAMECSEN is forced to 0 when using optimized accesses. The first access uses the regular timing settings for this chip-select. All accesses after this one use settings reduced by x clock cycles, x being defined by the GPMC_PREFETCH_CONFIG1[30-28] CYCLEOPTIMIZATION bit field.

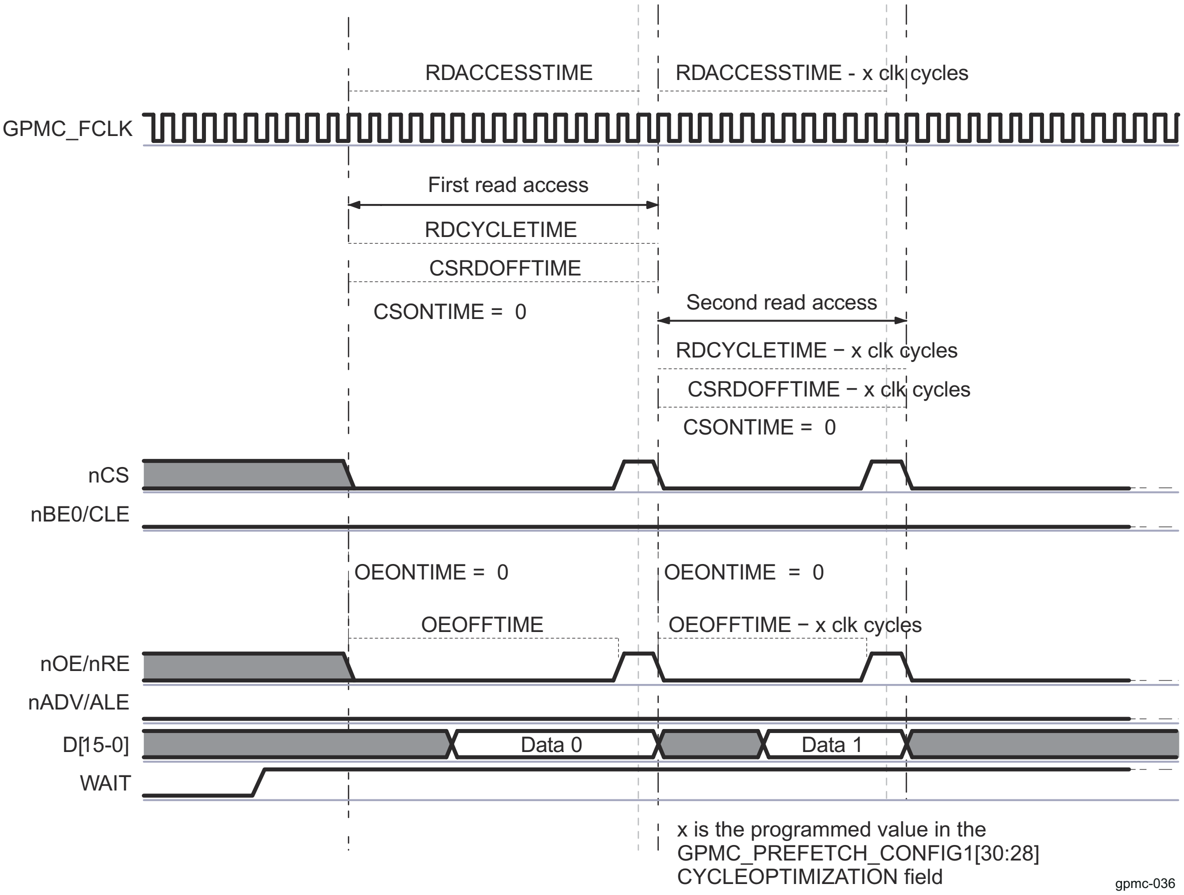

Figure 12-203. NAND Read Cycle Optimization Timing Description

12.3.3.4.11.4.7 Interleaved Accesses Between Prefetch and Write-Posting Engine and Other Chip-Selects

Any on-going read or write access from the prefetch and write-posting engine is completed before an access to any other chip-select can be initiated. As a default, the arbiter uses a fixed-priority algorithm, and the prefetch and write-posting engine has the lowest priority. The maximum latency added to access starting time in this case equals the RDCYCLETIME or WRCYCLETIME (optimized or not) plus the requested BUSTURNAROUND delay for bus turnaround completion programmed for the chip-select to which the NAND device is connected.

Alternatively, a round-robin arbitration can be used to prioritize accesses to the external bus. This arbitration scheme is enabled by setting the GPMC_PREFETCH_CONFIG1[23] PFPWENROUNDROBIN bit. When a request to another chip-select is received while the prefetch and write-posting engine is active, priority is given to the new request. The request processed thereafter is the prefetch and write-posting engine request, even if another interconnect request is passed in the mean time. The engine keeps control of the bus for an additional number of requests programmed in the GPMC_PREFETCH_CONFIG1[19-16] PFPWWEIGHTEDPRIO bit field. Control is then passed to the direct interconnect request.

As an example, the round-robin arbitration scheme is selected with PFPWWEIGHTEDPRIO set to 0x2. Considering that the prefetch and write-posting engine and the interconnect interface are always requesting access to the external interface, the GPMC grants priority to the direct interconnect access for one request. The GPMC then grants priority to the engine for three requests, and finally back to the direct interconnect access, until the arbiter is reset when one of the two initiators stops initiating requests.

12.3.3.4.12 GPMC Memory Regions

Table 12-266 shows the GPMC memory regions.

Table 12-278. GPMC Memory Map

Region Name	Address Range	Size	Description
	GPMC0		
GPMC0_CFG	0x4840 0000 to 0x4840 03FF	1 KB	Configuration registers space

12.3.3.4.13 GPMC Use Cases and Tips

12.3.3.4.13.1 How to Set GPMC Timing Parameters for Typical Accesses

12.3.3.4.13.1.1 External Memory Attached to the GPMC Module

As discussed in the introduction to this chapter, the GPMC module supports the following external memory types:

- Asynchronous or synchronous, 8- or 16-bit-wide memory or device
- 16-bit address/data-multiplexed or non-multiplexed NOR flash device
- 8- or 16-bit NAND flash device

The following examples describe how to calculate GPMC timing parameters by showing a typical parameter setup for the access to be performed.

The example is based on a 512-Mb multiplexed NOR flash memory with the following characteristics:

- Type: NOR flash (address/data-multiplexed mode)
- Size: 512M bits
- Data Bus: 16 bits wide
- Speed: 104-MHz clock frequency
- Read access time: 80 ns

12.3.3.4.13.1.2 Typical GPMC Setup

Table 12-267 lists some of the I/Os of the GPMC module.

Table 12-279. Typical GPMC Setup Signals

Module Pin	I/O(1)	Description
GPMC0_FCLK	Internal	Functional clock. Acts as the time reference.
GPMC0_ICLK	Internal	Interface clock. Acts as the time reference.
GPMC0_CLKOUT	O	External clock provided to the external device for synchronous operations
GPMC0_A[21-16]	O	Address
GPMC0_AD[15-0]	I/O	Data-multiplexed with addresses A[16-1] on memory side
GPMC0_CSn[3-0]	O	Chip-selects
GPMC0_ADVn_ALE	O	Address valid enable
GPMC0_OEn_REn	O	Output enable (read access only)
GPMC0_WEn	O	Write enable (write access only)
GPMC0_WAIT[1-0]	I	Ready signal from memory device. Indicates when valid burst data is ready to be read

(1) I = Input; O = Output

Figure 12-204 shows the typical connection between the GPMC module and an attached NOR Flash memory.

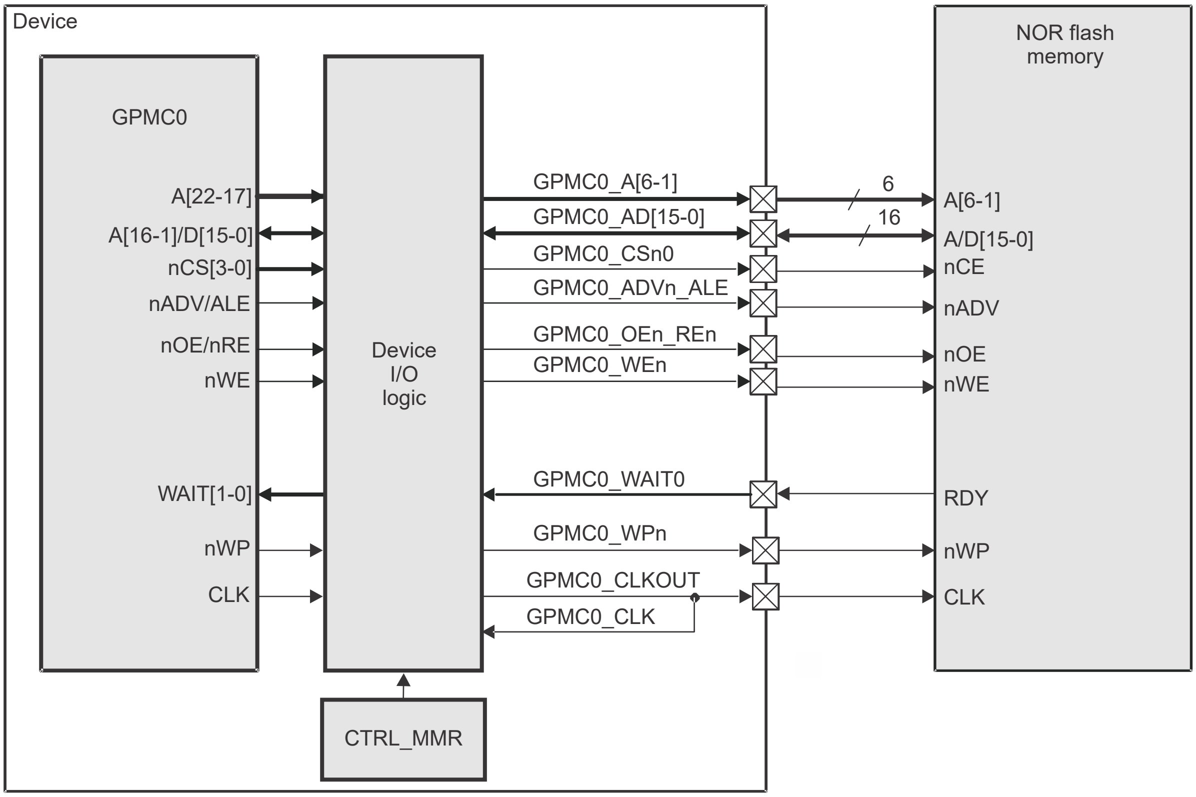

Figure 12-204. GPMC Connection to an External NOR Flash Memory

The following sections demonstrate how to calculate GPMC parameters for three access types:

- Synchronous burst read
- Asynchronous read
- Asynchronous single write

12.3.3.4.13.1.2.1 GPMC Configuration for Synchronous Burst Read Access

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Note

The examples in Section 12.3.3.4.13.1.2.1 through Section 12.3.3.4.13.1.2.3 are based on a clock rate of 104 MHz. See the device-specific Datasheet for the maximum frequency appropriate for this device and the memory datasheet for the maximum frequency for the particular memory device.

The clock runs at 104 MHz (f = 104 MHz; T = 9.615 ns).

Table 12-268 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Table 12-269 shows how to calculate timings for the GPMC using the memory parameters.

Figure 12-205 shows the synchronous burst read access.

Table 12-280. Useful Timing Parameters on the Memory Side

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCES	nCS setup time to clock	0

Table 12-280. Useful Timing Parameters on the Memory Side (continued)

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tACS	Address setup time to clock	3
tIACC	Synchronous access time	80
tBACC	Burst access time valid clock to output delay	5.2
tCEZ	Chip-select to High-Z	7
tOEZ	Output enable to High-Z	7
tAVC	nADV setup time	6
tAVD	nAVD pulse	6
tACH	Address hold time from clock	3

The following terms, which describe the timing interface between the controller and its attached device, are used to calculate the timing parameters on the GPMC side:

- Read access time (GPMC side): Time required to activate the clock + read access time requested on the memory side + data setup time required for optimal capture of a burst of data
- Data setup time (GPMC side): Ensures a good capture of a burst of data (as opposed to taking a burst of data out). One word of data is processed in one clock cycle (T = 9.615 ns). The read access time between two bursts of data is tBACC = 5.2 ns. Therefore, data setup time is a clock period – tBACC = 4.415 ns of data setup.
- Access completion (GPMC side): (Different from page burst access time) Time required between the last burst access and access completion: nCS/nOE hold time (nCS and nOE must be released at the end of an access. These signals are held to allow the access to complete).
- Read cycle time (GPMC side): Read access time + access completion
- Write cycle time for burst access: Not supported for NOR flash memory

Table 12-281. Calculating GPMC Timing Parameters

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Register Configurations
GPMC FCLK Divider	–	–	–	GPMCFCLKDIVIDER = 0x0
ClkActivation Time	min (tCES, tACS)	3	1	CLKACTIVATIONTIME = 0x1
RdAccessTime	roundmax (ClkActivationTime + tIACC + DataSetupTime)	94.03: (9.615 + 80 + 4.415)	10: roundmax (94.03 / 9.615)	RDACCESSTIME = 0xA
PageBurst RdAccessTime	roundmax (tBACC)	roundmax (5.2)	1	PAGEBURSTACCESSTIME = 0x1
RdCycleTime	RdAccess time + max (tCEZ, tOEZ)	101.03: (94.03 + 7)	11	RDCYCLETIME = 0xB
CsOnTime	tCES	0	0	CSONTIME = 0x0
CsReadOffTime	RdCycleTime	-	11	CSRDOFFTIME = 0xB
AdvOnTime	tAVC (1)	0	0	ADVONTIME = 0x0
AdvRdOffTime	tAVD + tAVC (2)	12	2	ADVRDOFFTIME = 0x2
OeOnTime (3)	(ClkActivationTime + tACH) < OeOnTime (ClkActivationTime + tIACC)	–	3, for instance	OEONTIME = 0x3
OeOffTime	RdCycleTime	–	11	OEOFFTIME = 0xB

(1) The external clock provided to the NOR flash is not yet available.

(2) AdvRdOffTime – AdvOnTime = tAVD; thus, AdvRdOffTime = tAVD + AdvOnTime = tAVD + tAVC.

(3) OeOnTime must ensure that addresses are available. It must not exceed the availability of the first burst of data.

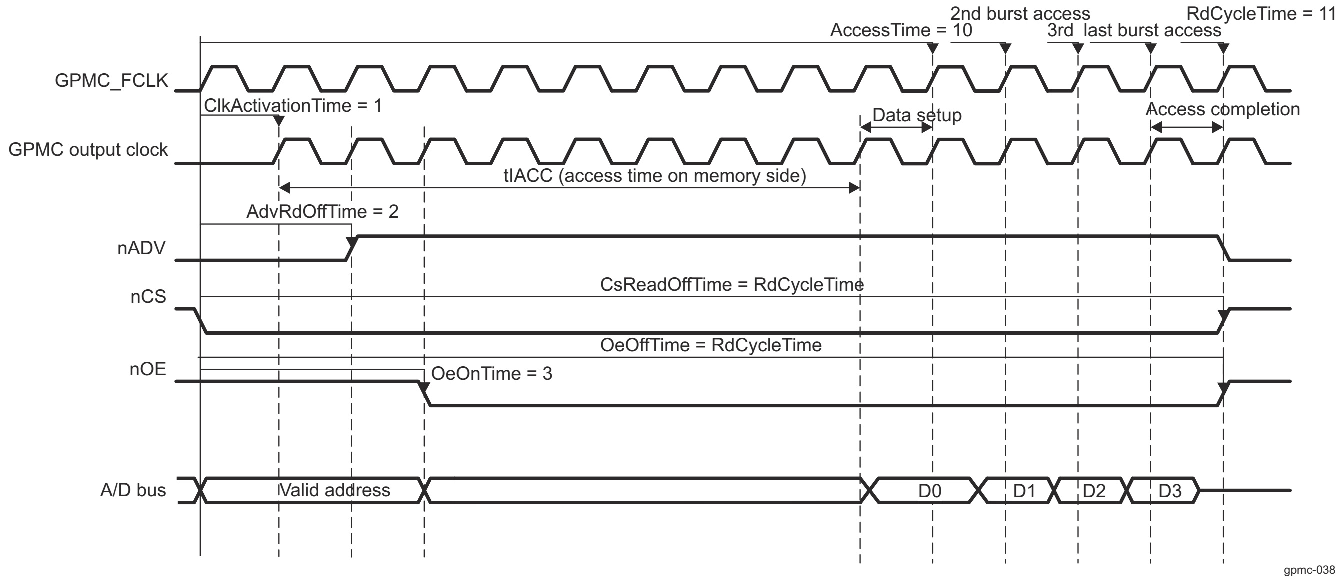

Figure 12-205. Synchronous Burst Read Access (Timing Parameters in Clock Cycles)

12.3.3.4.13.1.2.2 GPMC Configuration for Asynchronous Read Access

The clock runs at 104 MHz (f = 104 MHz; T = 9.615 ns).

Table 12-270 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Table 12-271 shows how to calculate timings for the GPMC using the memory parameters.

Figure 12-206 shows the asynchronous read access.

Table 12-282. AC Characteristics for Asynchronous Read Access

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCE	Read Access time from nCS low	80
tAAVDS	Address setup time to rising edge of nADV	3
tAVDP	nADV low time	6
tCAS	nCS setup time to nADV	0
tOE	Output enable to output valid	6
tOEZ	Output enable to High-Z	7

Use the following formula to calculate the RdCycleTime parameter for this typical access:

RdCycleTime = RdAccessTime + AccessCompletion = RdAccessTime + 1 clock cycle + tOEZ:

1. On the memory side, the external memory makes the data available to the output bus. This is the memory-side read access time defined in Table 12-270: the number of clock cycles between the address capture (nADV rising edge) and the data valid on the output bus.

   The GPMC requires some hold time to allow the data to be captured correctly and the access to be finished.
2. To read the data correctly, the GPMC must be configured to meet the data setup time requirement of the memory; the GPMC module captures the data on the next rising edge. This is access time on the GPMC side.
3. There must also be a data hold time for correctly reading the data (checking that there is no nOE/nCS deassertion while reading the data). This data hold time is one clock cycle (that is, RdAccessTime + 1).
4. To complete the access, nOE/nCS signals are driven to High-Z. RdAccessTime + 1 + tOEZ is the read cycle time.

5. Addresses can now be relatched and a new read cycle begun.

Table 12-283. GPMC Timing Parameters for Asynchronous Read Access

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Register Configurations
ClkActivationTime	n/a (asynchronous mode)			
RdAccessTime	round max (tCE)	80	10	RDACCESSTIME = 0xA
PageBurstAccessTime	N/A (single access)			
RdCycleTime	RdAccessTime + 1cycle + tOEZ	96.615	12	RDCYCLETIME = 0xC
CsOnTime	tCAS	0	0	CSONTIME = 0x0
CsReadOffTime	RdAccessTime + 1 cycle	89.615	11	CSRDOFFTIME = 0xB
AdvOnTime	tAAVDS	3	1	ADVONTIME = 0x1
AdvRdOffTime	tAAVDS + tAVDP	9	1	ADVRDOFFTIME = 0x1
OeOnTime	OeOnTime >= AdvRdOffTime (multiplexed mode)	-	3, for instance	OEONTIME = 0x3
OeOffTime	RdAccessTime + 1cycle	89.615	11	OEOFFTIME = 0xB

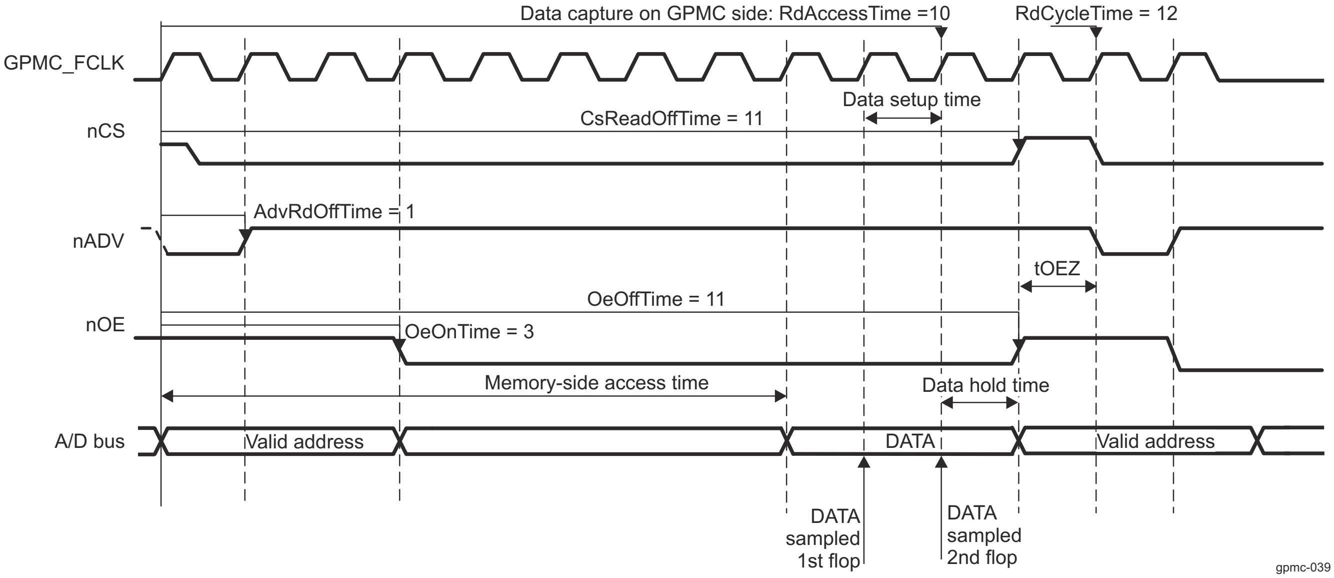

Figure 12-206. Asynchronous Single Read Access (Timing Parameters in Clock Cycles)

12.3.3.4.13.1.2.3 GPMC Configuration for Asynchronous Single Write Access

The clock runs at 104 MHz: (f = 104 MHz; T = 9.615 ns).

Table 12-273 shows how to calculate timings for the GPMC using the memory parameters.

Table 12-272 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Figure 12-207 shows the asynchronous single write access.

Table 12-284. AC Characteristics for Asynchronous Single Write (Memory Side)

AC Characteristics on the Memory Side	Description	Duration (ns)
tWC	Write cycle time	60
tAVDP	nADV low time	6
tWP	Write pulse width	25

Table 12-284. AC Characteristics for Asynchronous Single Write (Memory Side) (continued)

AC Characteristics on the Memory Side	Description	Duration (ns)
tWPH	Write pulse width high	20
tCS	nCS setup time to nWE	3
tCAS	nCS setup time to nADV	0
tAVSC	nADV setup time	3

For asynchronous single write access, write cycle time is WrCycleTime = WeOffTime + AccessCompletion = WeOffTime + 1. For the AccesCompletion, the GPMC requires one cycle of data hold time (nCS deassertion). For more information, see the device-specific Datasheet.

Table 12-285. GPMC Timing Parameters for Asynchronous Single Write

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Registers Configuration
ClkActivationTime	N/A (asynchronous mode)			
WdAccessTime	Applicable only to WAITMONITORING (the value is the same as for read access)			
PageBurstAccessTime	N/A (single access)			
WrCycleTime	WeOffTime + AccessCompletion	57.615	6	WRCYCLETIME = 0x6
CsOnTime	tCAS	0	0	CSONTIME = 0x0
CsWrOffTime	WeOffTime + 1	57.615	6	CSWROFFTIME = 0x6
AdvOnTime	tAVSC	3	1	ADVONTIME = 0x1
AdvWrOffTime	tAVSC + tAVDP	9	1	ADVWROFFTIME = 0x1
WeOnTime	tCS	3	1	WEONTIME = 0x1
WeOffTime	tCS + tWP + tWPH	48	5	WEOFFTIME = 0x5

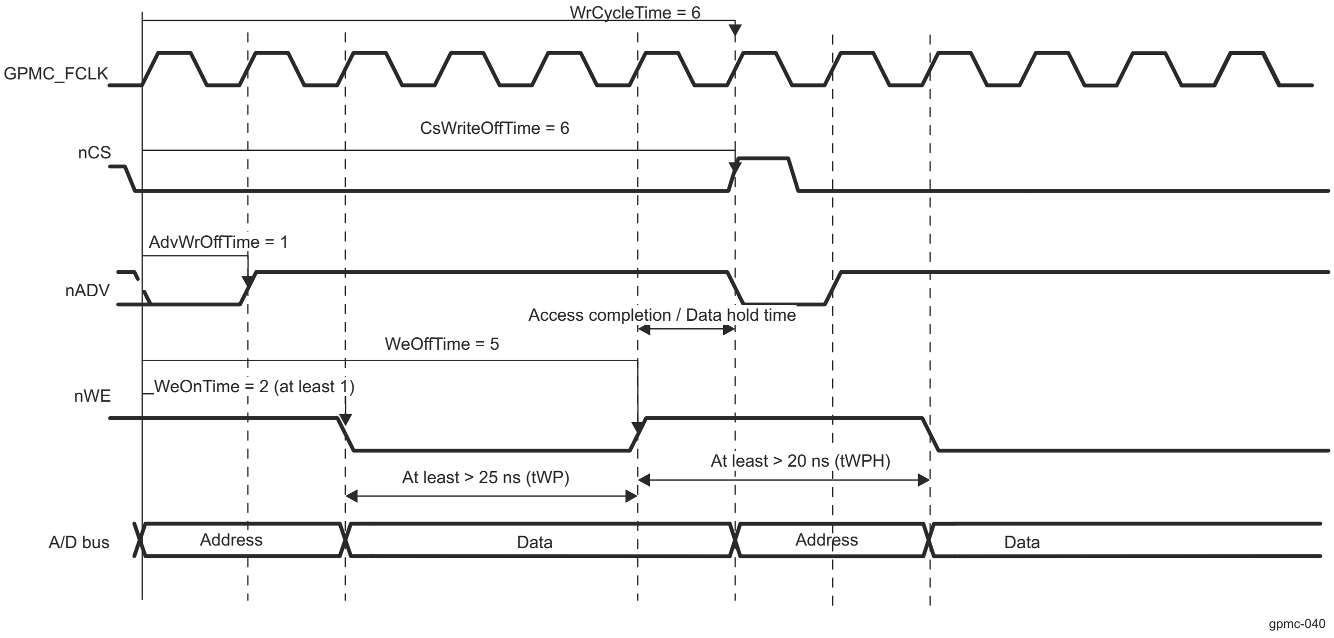

Figure 12-207. Asynchronous Single Write Access (Timing Parameters in Clock Cycles)

12.3.3.4.13.2 How to Choose a Suitable Memory to Use With the GPMC

This section is intended to help the user select a suitable memory device to interface with the GPMC controller.

12.3.3.4.13.2.1 Supported Memories or Devices

NAND flash and NOR flash architectures are the two flash technologies. The GPMC supports various types of external memory or devices, basically any one that supports NAND or NOR protocols:

- 8- and 16-bit-wide asynchronous or synchronous memory or device (only 8-bit: nonburst device)
- 16-bit address and data-multiplexed NOR flash devices (pSRAM, and so on)
- 8- and 16-bit NAND flash devices

12.3.3.4.13.2.1.1 Memory Pin Multiplexing

This section describes the interfacing differences of the GPMC supported memories.

Table 12-286. Supported Memory Interfaces

<table>
<tr><th>Function</th><th>16-Bit Address/ Data-Multiplexed pSRAM or NOR Flash [1]</th><th>16-Bit NAND</th><th>8-Bit NAND</th></tr>
<tr><td>GPMC_A[22]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[21]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[20]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[19]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[18]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[17]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[16]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[15]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[14]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[13]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[12]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[11]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_A[10]</td><td>A26</td><td></td><td></td></tr>
<tr><td>GPMC_A[9]</td><td>A25</td><td></td><td></td></tr>
<tr><td>GPMC_A[8]</td><td>A24</td><td></td><td></td></tr>
<tr><td>GPMC_A[7]</td><td>A23</td><td></td><td></td></tr>
<tr><td>GPMC_A[6]</td><td>A22</td><td></td><td></td></tr>
<tr><td>GPMC_A[5]</td><td>A21</td><td></td><td></td></tr>
<tr><td>GPMC_A[4]</td><td>A20</td><td></td><td></td></tr>
<tr><td>GPMC_A[3]</td><td>A19</td><td></td><td></td></tr>
<tr><td>GPMC_A[2]</td><td>A18</td><td></td><td></td></tr>
<tr><td>GPMC_A[1]</td><td>A17</td><td></td><td></td></tr>
<tr><td>GPMC_A[0]</td><td></td><td></td><td></td></tr>
<tr><td>GPMC_AD[15]</td><td>D15 or A16</td><td>IO15</td><td></td></tr>
<tr><td>GPMC_AD[14]</td><td>D14 or A15</td><td>IO14</td><td></td></tr>
<tr><td>GPMC_AD[13]</td><td>D13 or A14</td><td>IO13</td><td></td></tr>
<tr><td>GPMC_AD[12]</td><td>D12 or A13</td><td>IO12</td><td></td></tr>
<tr><td>GPMC_AD[11]</td><td>D11 or A12</td><td>IO11</td><td></td></tr>
<tr><td>GPMC_AD[10]</td><td>D10 or A11</td><td>IO10</td><td></td></tr>
<tr><td>GPMC_AD[9]</td><td>D9 or A10</td><td>IO9</td><td></td></tr>
<tr><td>GPMC_AD[8]</td><td>D8 or A9</td><td>IO8</td><td></td></tr>
<tr><td>GPMC_AD[7]</td><td>D7 or A8</td><td colspan="2">IO7</td></tr>
<tr><td>GPMC_AD[6]</td><td>D6 or A7</td><td colspan="2">IO6</td></tr>
<tr><td>GPMC_AD[5]</td><td>D5 or A6</td><td colspan="2">IO5</td></tr>
<tr><td>GPMC_AD[4]</td><td>D4 or A5</td><td colspan="2">IO4</td></tr>
</table>

Table 12-286. Supported Memory Interfaces (continued)

Function	16-Bit Address/ Data-Multiplexed pSRAM or NOR Flash (1)	16-Bit NAND	8-Bit NAND
GPMC_AD[3]	D3 or A4	IO3	
GPMC_AD[2]	D2 or A3	IO2	
GPMC_AD[1]	D1 or A2	IO1	
GPMC_AD[0]	D0 or A1	IO0	
GPMC_CLKOUT	CLK		
GPMC_CSn0	nCS0 (chip-select)	nCE0 (chip-enable)	
GPMC_CSn1	nCS1	nCE1	
GPMC_CSn2	nCS2	nCE2	
GPMC_CSn3	nCS3	nCE3	
GPMC_ADVn_ALE	nADV (address valid)	ALE (address latch enable)	
GPMC_OEn_REn	nOE (output enable)	nRE (read enable)	
GPMC_WEn	nWE (Write enable)	nWE (write enable)	
GPMC_BE0n_CLE	nBE0 (byte enable)	CLE (command latch enable)	
GPMC_BE1n	nBE1		
GPMC_WAIT0	WAIT0	R/nB0 (ready/busy)	
GPMC_WAIT1	WAIT1	R/nB1	
GPMC_WPn	nWP (Write Protect)	nWP (Write Protect)	

(1) Addresses seen from the device side. When interfacing to the external device, A1 is connected to the memory A0, A2 to the memory A1, and so on.

12.3.3.4.13.2.1.2 NAND Interface Protocol

NAND flash architecture, introduced in 1989, is a flash technology. NAND is a page-oriented memory device; that is, read and write accesses are done by pages. NAND achieves great density by sharing common areas of the storage transistor, which creates strings of serially connected transistors (in NOR devices, each transistor stands alone). Because of its high density NAND is best suited to devices that require high capacity data storage, such as pictures, music, and data files. NAND nonvolatility makes of it a good storage solution for many applications where mobility, low power, and speed are key factors. Low pin count and simple interface are other advantages of NAND.

Table 12-275 summarizes the NAND interface signals level applied to external device or memories.

Table 12-287. NAND Interface Bus Operations Summary

Bus Operation	CLE	ALE	nCE	nWE (1)	nRE (1)	nWP
Read (cmd input)	H	L	L	RE	H	x
Read (add input)	L	H	L	RE	H	x
Write (cmd input)	H	L	L	RE	H	H
Write (add input)	L	H	L	RE	H	H
Data input	L	L	L	RE	H	H
Data output	L	L	L	H	FE	x
Busy (during read)	x	x	H (2)	H (2)	H (2)	x
Busy (during program)	x	x	x	x	x	H
Busy (during erase)	x	x	x	x	x	H
Write protect	x	x	x	x	x	L

Table 12-287. NAND Interface Bus Operations Summary (continued)

Bus Operation	CLE	ALE	nCE	nWE (1)	nRE (1)	nWP
Standby	x	x	H	x	x	H/L

(1) RE stands for rising edge; FE stands for falling edge

(2) Can be nCE high, or WE and nRE high.

12.3.3.4.13.2.1.3 NOR Interface Protocol

NOR flash architecture, introduced in 1988, is a flash technology. Unlike NAND, which is a sequential access device, NOR is directly addressable; that is, it is designed to be a random access device. NOR is best suited to devices used to store and run code or firmware, usually in small capacities. While NOR has fast read capabilities, it also has slow write and erase functions when compared to the NAND architecture.

Table 12-276 summarizes the level of the NOR interface signals applied to external devices or memories.

Table 12-288. NOR Interface Bus Operations Summary

Bus Operation	CLK	nADV	nCS	nOE	nWE	WAIT	DQ[15-0]
Read (asynchronous)	x	L	L	L	H	Asserted	Output
Read (synchronous)	Running	L	L	L	H	Driven	Output
Read (burst suspend)	Halted	x	L	H	H	Active	Output
Write	x	L	L	H	L	Asserted	Input
Output disable	x	x	L	H	H	Asserted	High-Z
Standby	x	x	H	x	x	High-Z	High-Z

12.3.3.4.13.2.1.4 Other Technologies

Other supported device types interact with the GPMC through the NOR interface protocol.

FPGA (Field-Programmable Gate Array) is a low-power integrated circuit based on an array of programmable logic blocks.

pSRAM (pseudo-static random access memory) is a low-power memory device. pSRAM is based on the DRAM cell with internal refresh and address control features, and interfaces as a synchronous NOR flash. It has synchronous write capability.

12.3.3.5 GPMC Basic Programming Model

12.3.3.5.1 GPMC High-Level Programming Model Overview

The goal of the basic high-level programming model is to introduce a top-down approach to users that need to configure the GPMC module.

Figure 12-208 and Table 12-277 through Table 12-278 show a programming model top-level diagram for the GPMC, and a description of each step. Each block of the diagram is described in one of the following sections through a set of registers to configure.

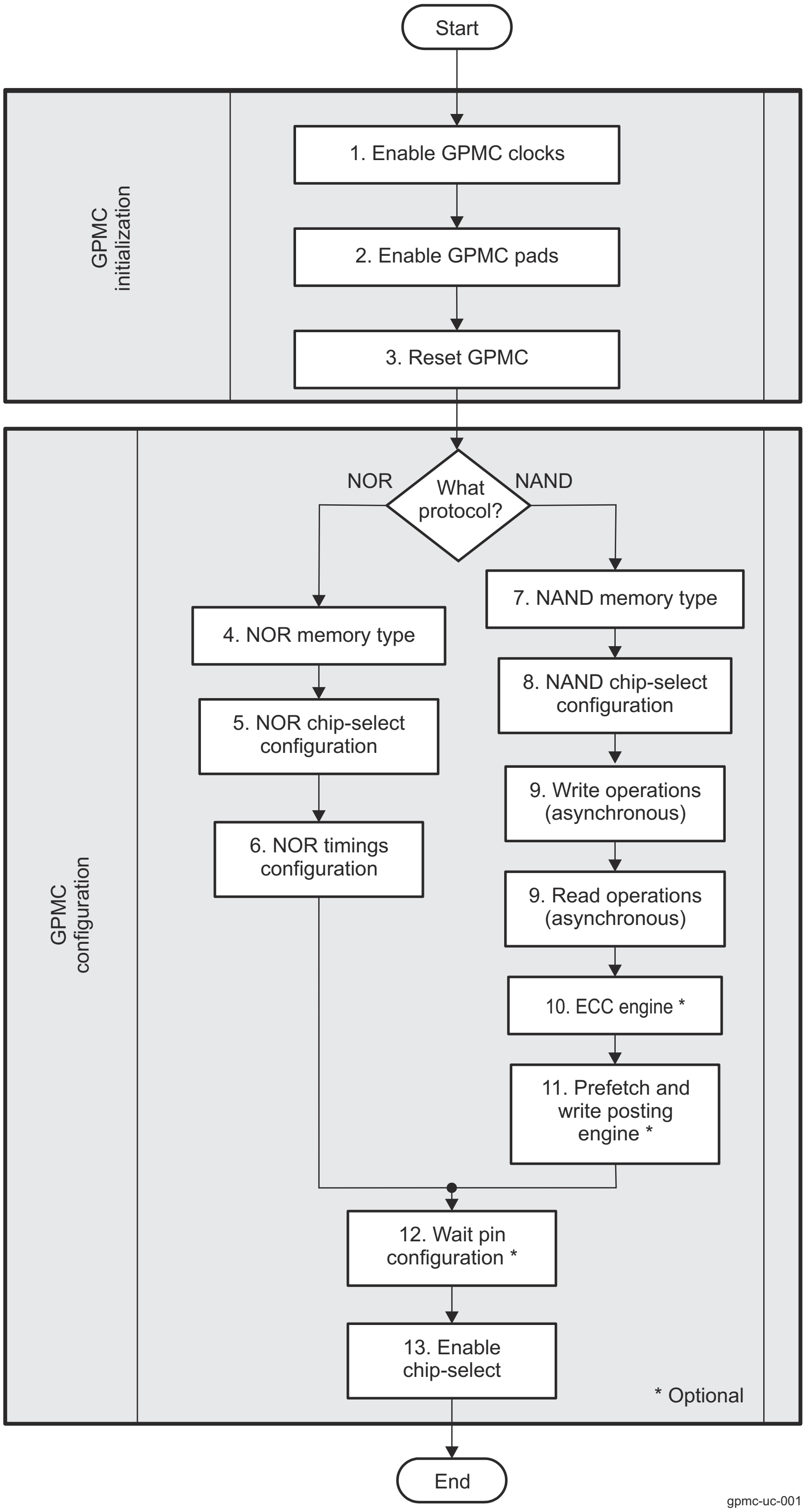

Figure 12-208. Programming Model Top-Level Diagram

Table 12-289. GPMC Configuration in NOR Mode

Step	Description
NOR Memory Type	See Table 12-279.

Table 12-289. GPMC Configuration in NOR Mode (continued)

Step	Description
NOR Chip-Select Configuration	See Table 12-280.
NOR Timings Configuration	See Table 12-281.
WAIT Pin Configuration	See Table 12-289.
Enable Chip-Select	See Table 12-290.

Table 12-290. GPMC Configuration in NAND Mode

Step	Description
NAND Memory Type	See Table 12-284.
NAND Chip-Select Configuration	See Table 12-285.
Write Operations (Asynchronous)	See Table 12-286.
Read Operations (Asynchronous)	See Table 12-286.
ECC Engine	See Table 12-287.
Prefetch and Write-Posting Engine	See Table 12-288.
WAIT Pin Configuration	See Table 12-289.
Enable Chip-Select	See Table 12-290.

12.3.3.5.2 GPMC Initialization

GPMC can be reset via software bit in LPSC. For more information, see *Reset*.

12.3.3.5.3 GPMC Configuration in NOR Mode

This section gives a generic configuration for parameters related to the NOR memory connected to the GPMC.

Table 12-291. NOR Memory Type

Subprocess Name	Register / Bit Field	Value
Set the NOR protocol.	GPMC_CONFIG1_i[11-10] DEVICETYPE	0x0
Set a device size.	GPMC_CONFIG1_i[13-12] DEVICESIZE	x
Select an address and data multiplexing protocol.	GPMC_CONFIG1_i[9-8] MUXADDDATA	x
Set the attached device page length.	GPMC_CONFIG1_i[24-23] ATTACHEDDEVICEPAGELENGTH	x
Set the wrapping burst capabilities.	GPMC_CONFIG1_i[31] WRAPBURST	x
Select a timing signals latencies factor.	GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY	x
Select an output clock frequency (1).	GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER	x
Choose an output clock activation time (1).	GPMC_CONFIG1_i[26-25] CLKACTIVATIONTIME	x
Set a single or multiple access for read operations (1).	GPMC_CONFIG1_i[30] READMULTIPLE	x
Set a synchronous or asynchronous mode for read operations.	GPMC_CONFIG1_i[29] READTYPE	x
Set a single or multiple access for write operations.	GPMC_CONFIG1_i[28] WRITEMULTIPLE	x
Set a synchronous or asynchronous mode for write operations.	GPMC_CONFIG1_i[27] WRITETYPE	x

(1) Applies only to synchronous configurations (or non-multiplexed asynchronous for multiple access one)

Table 12-292. NOR Chip-Select Configuration

Subprocess Name	Register/Bit Field	Value
Select the chip-select base address.	GPMC_CONFIG7_i[5-0] BASEADDRESS	x
Select the chip-select mask address.	GPMC_CONFIG7_i[11-8] MASKADDRESS	x

Table 12-293. NOR Timings Configuration

Subprocess Name	Register/Bit Field	Value
Configure adequate timing parameters in various memory modes.	See Section 12.3.3.5.6 , *GPMC Timing Parameters*	

Table 12-294. WAIT Pin Configuration

Subprocess Name	Register/Bit Field	Value
Enable or disable WAIT pin monitoring for read operations.	GPMC_CONFIG1_i[22] WAITREADMONITORING	x
Enable or disable WAIT pin monitoring for write operations.	GPMC_CONFIG1_i[21] WAITWRITEMONITORING	x
Select a WAIT pin monitoring time.	GPMC_CONFIG1_i[19-18] WAITMONITORINGTIME	x
Choose the input WAIT pin for the chip-select.	GPMC_CONFIG1_i[17-16] WAITPINSELECT	x

Table 12-295. Enable Chip-Select

Subprocess Name	Register/Bit Field	Value
When all parameters are configured, enable the chip-select.	GPMC_CONFIG7_i[6] CSVALID	x

12.3.3.5.4 GPMC Configuration in NAND Mode

This section gives a generic configuration for parameters related to the NAND memory connected to the GPMC.

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

Table 12-296. NAND Memory Type

Subprocess Name	Register/Bit Field	Value
Set the NAND protocol.	GPMC_CONFIG1_i[11-10] DEVICETYPE	0x2
Set a device size.	GPMC_CONFIG1_i[13-12] DEVICESIZE	x
Set the address and data multiplexing protocol to non-multiplexed attached device.	GPMC_CONFIG1_i[9-8] MUXADDDATA	0x0
Select a timing signals latencies factor.	GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY	x
Set a synchronous or asynchronous mode and a single or multiple access for read and write operations.	See Section 12.3.3.5.5 , *Set Memory Access*.	x

Table 12-297. NAND Chip-Select Configuration

Subprocess Name	Register/Bit Field	Value
Select the chip-select base address.	GPMC_CONFIG7_i[5-0] BASEADDRESS	x
Select the chip-select minimum granularity (16MB).	GPMC_CONFIG7_i[11-8] MASKADDRESS	x

Table 12-298. Asynchronous Read and Write Operations

Subprocess Name	Register/Bit Field	Value
Configure adequate timing parameters in asynchronous modes	See Section 12.3.3.5.6 , *GPMC Timing Parameters*.	

Table 12-299. ECC Engine

Subprocess Name	Register/Bit Field	Value
Select the ECC result register where the first ECC computation is stored (applies only to Hamming).	GPMC_ECC_CONTROL[3-0] ECCPOINTER	x (2)
Clear all ECC result registers.	GPMC_ECC_CONTROL[8] ECCCLEAR	Write 1 to clear.
Define ECCSIZE0 and ECCSIZE1.	GPMC_ECC_SIZE_CONFIG[21-12] ECCSIZE0 and [31-22] ECCSIZE1	x (1)

Table 12-299. ECC Engine (continued)

Subprocess Name	Register/Bit Field	Value
Select the size of each of the 9 result registers (size specified by ECCSIZE0 or ECCSIZE1).	GPMC_ECC_SIZE_CONFIG[j-1] ECCjRESULTSIZE where j = 1 to 9	x
Select the chip-select where ECC is computed.	GPMC_ECC_CONFIG[3-1] ECCCS	x
Select the Hamming code or BCH code ECC algorithm in use.	GPMC_ECC_CONFIG[16] ECCALGORITHM	x
Select word size for ECC calculation.	GPMC_ECC_CONFIG[7] ECC16B	x
If the BCH code is used, Set an error correction capability and Select a number of sectors to process.	GPMC_ECC_CONFIG[13-12] ECCBCHTSEL and GPMC_ECC_CONFIG[6-4] ECCTOPSECTOR	x
Enable the ECC computation.	GPMC_ECC_CONFIG[0] ECCENABLE	0x1

(1) Depends on the size of each sector in the NAND page

(2) This parameter depends on the numbers of sectors in a page.

Table 12-300. Prefetch and Write-Posting Engine

Subprocess Name	Register/Bit Field	Value
Disable the engine before configuration.	GPMC_PREFETCH_CONTROL[0] STARTENGINE	0x0
Select the chip-select associated with a NAND device where the prefetch engine is active.	GPMC_PREFETCH_CONFIG1[26-24] ENGINECSSELECTOR	x
Select access direction through prefetch engine, read or write.	GPMC_PREFETCH_CONFIG1[0] ACCESSMODE	x
Select the threshold used to issue an interrupt request.	GPMC_PREFETCH_CONFIG1[14-8] FIFOTHRESHOLD	x
Select interrupt synchronization mode.	GPMC_PREFETCH_CONFIG1[2] DMAMODE	x
Select if the engine immediately starts accessing the memory upon STARTENGINE assertion or if hardware synchronization based on a WAIT signal is used.	GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE	x
Select which WAIT pin edge detector should start the engine in synchronized mode.	GPMC_PREFETCH_CONFIG1[5-4] WAITPINSELECTOR	x
Enter a number of clock cycles removed to timing parameters (for all back-to-back accesses to the NAND flash except the first one).	GPMC_PREFETCH_CONFIG1[30-28] CYCLEOPTIMIZATION	x
Enable the prefetch postwrite engine.	GPMC_PREFETCH_CONFIG1[7] ENABLEENGINE	0x1
Select the number of bytes to be read or written by the engine to the selected chip-select.	GPMC_PREFETCH_CONFIG2[13-0] TRANSFERCOUNT	x
Start the prefetch engine.	GPMC_PREFETCH_CONTROL[0] STARTENGINE	0x1

Table 12-301. WAIT Pin Configuration

Subprocess Name	Register/Bit Field	Value
Selects when the engine starts the access to chip-select.	GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE	x
Select which WAIT pin edge detector should start the engine in synchronized mode.	GPMC_PREFETCH_CONFIG1[5-4] WAITPINSELECTOR	x

Table 12-302. Enable Chip-Select

Subprocess Name	Register/Bit Field	Value
When all parameters are configured, enable the chip-select.	GPMC_CONFIG7_i[6] CSVALID	x

12.3.3.5.5 Set Memory Access

Note

Some of the GMPC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

This section describes the bit field to configure to set the GPMC in various memory modes. Table 12-291 and Table 12-292 provide check lists for mode parameters and access type parameters, respectively.

Table 12-303. Mode Parameters Check List

Register	Bit	Name	Asynchronous				Synchronous			
			Single Read Access	Single Write Access	Multiple Read (Page) Access	Multiple Write (Page) Access	Single Read Access	Single Write Access	Multiple Read (Burst) Access	Multiple Write (Burst) Access
GPMC_CONFIG1_i	30	READMULTIPLE	0x0	Don't care	0x1 (1)	Not Supported	0x0	Don't care	0x1	Don't care
GPMC_CONFIG1_i	29	READTYPE	0x0	Don't care	0x0 (1)	Not Supported	0x1	Don't care	0x1	Don't care
GPMC_CONFIG1_i	28	WRITEMULTIPLE	Don't care	0x0	- (1)	Not Supported	Don't care	0x0	Don't care	0x1
GPMC_CONFIG1_i	27	WRITETYPE	Don't care	0x0	- (1)	Not Supported	Don't care	0x1	Don't care	0x1

(1) Multiple read is not supported in address/data-multiplexed and AAD-multiplexed modes. Multiple read is supported in non-multiplexed mode.

Table 12-304. Access Type Parameters Check List

Register	Bit	Name	Access Type		
			non-multiplexed	Address/ Data-Multiplexed	AAD-Multiplexed
GPMC_CONFIG1_i	9-8	MUXADDDATA	0x0	0x2	0x1

12.3.3.5.6 GPMC Timing Parameters

Figure 12-209 shows a programming model diagram for the NOR interfacing timing parameters.

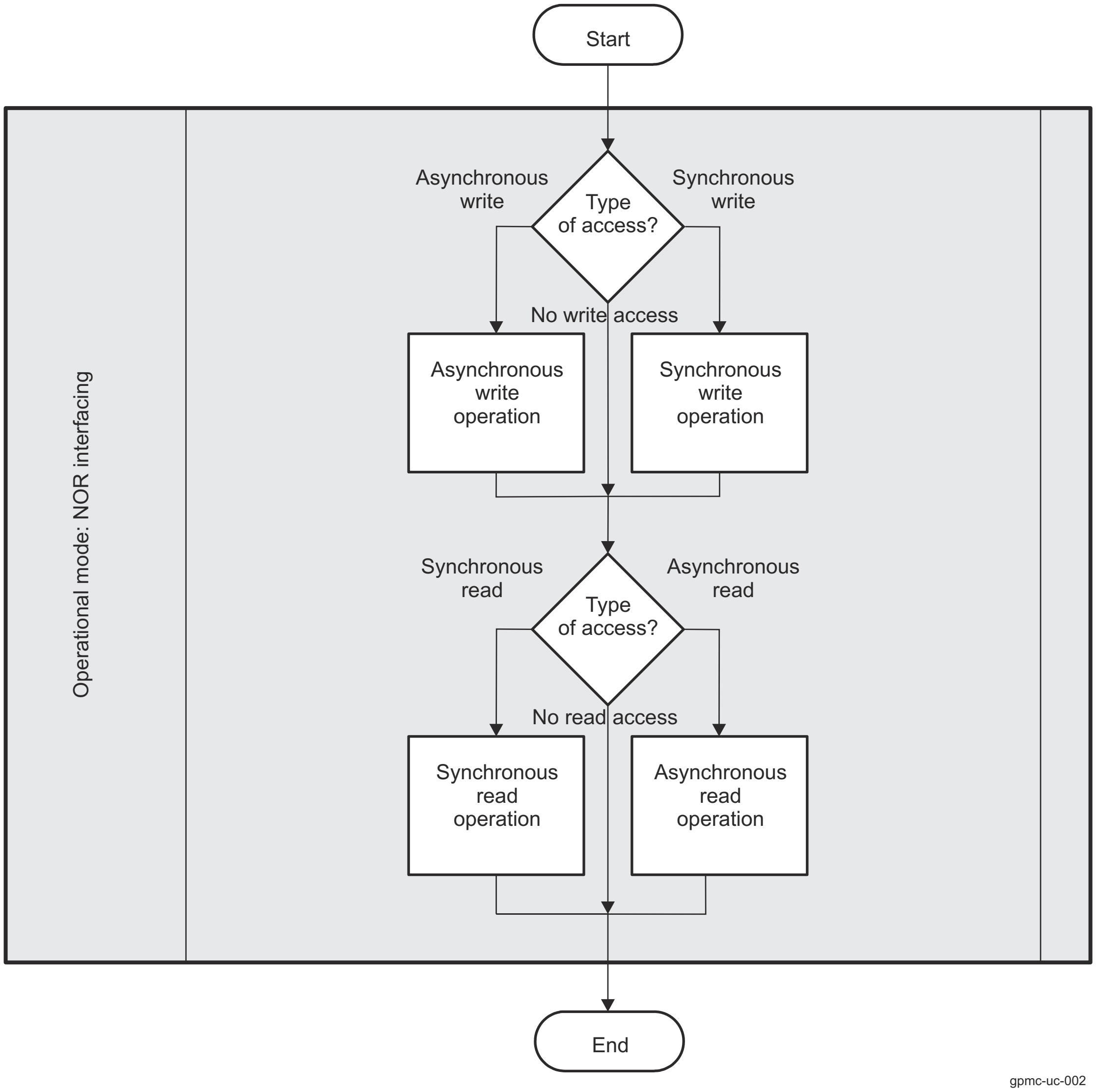

Figure 12-209. NOR Interfacing Timing Parameters Diagram

Table 12-293 lists the bit fields to configure adequate timing parameters in various memory modes.

Table 12-305. Timing Parameters

			Asynchronous			**Synchronous**				**Access Type**		
Register	**Bit**	**Name**	**Single Read Access**	**Single Write Access**	**Multiple Read (Page) access**	**Single Read Access**	**Single Write Access**	**Multiple Read (Burst) Access**	**Multiple Write (Burst) Access**	**Non-multiplexed**	**Address/ Data-Multiplexed**	**AAD Multiplexed**
GPMC_CONFIG1_i	9	MUXADDDATA	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG1_i	29	READTYPE	y		y	y		y		y	y	y
GPMC_CONFIG1_i	30	READMULTIPLE	y		y	y		y		y	y	y
GPMC_CONFIG1_i	27	WRITETYPE		y			y		y	y	y	y
GPMC_CONFIG1_i	28	WRITEMULTIPLE		y			y		y	y	y	y
GPMC_CONFIG1_i	31	WRAPBURST						y	y	y	y	y

Table 12-305. Timing Parameters (continued)

			Asynchronous			Synchronous				Access Type		
GPMC_CONFIG1_i	26-25	CLKACTIVATIONTIME				y	y	y	y	y	y	y
GPMC_CONFIG1_i	19-18	WAITMONITORINGTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG1_i	4	TIMEPARAGRANULARITY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG2_i	20-16	CSWROFFTIME		y			y		y	y	y	y
GPMC_CONFIG2_i	12-8	CSRDOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG2_i	7	CSEXTRADELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG2_i	3-0	CSONTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG3_i	30-28	ADVAADMUXWROFFTIME		y			y		y			y
GPMC_CONFIG3_i	30-29	ADVAADMUXRDOFFTIME	y		y	y		y				y
GPMC_CONFIG3_i	6-4	ADVAADMUXONTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG3_i	20-16	ADVWROFFTIME		y			y		y	y	y	y
GPMC_CONFIG3_i	12-8	ADVRDOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG3_i	7	ADVEXTRADELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG3_i	3-0	ADVONTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG4_i	15-13	OEAADMUXOFFTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG4_i	6-4	OEAADMUXONTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG4_i	28-24	WEOFFTIME		y			y		y	y	y	y
GPMC_CONFIG4_i	23	WEEXTRADELAY		y			y		y	y	y	y
GPMC_CONFIG4_i	19-16	WEONTIME		y			y		y	y	y	y
GPMC_CONFIG4_i	12-8	OEOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG4_i	7	OEEXTRADELAY	y		y	y		y		y	y	y
GPMC_CONFIG4_i	3-0	OEONTIME	y		y	y		y		y	y	y
GPMC_CONFIG5_i	27-24	PAGEBURSTACCESSTIME			y			y	y	y	y	y
GPMC_CONFIG5_i	20-16	RDACCESSTIME	y		y	y		y		y	y	y
GPMC_CONFIG5_i	12-8	WRCYCLETIME		y			y		y	y	y	y
GPMC_CONFIG5_i	4-0	RDCYCLETIME	y		y	y		y		y	y	y
GPMC_CONFIG6_i	28-24	WRACCESSTIME		y			y		y	y	y	y
GPMC_CONFIG6_i	19-16	WRDATAONADMUXBUS		y			y		y		y	y
GPMC_CONFIG6_i	11-8	CYCLE2CYCLEDELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	7	CYCLE2CYCLESAMECSEN	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	6	CYCLE2CYCLEDIFFCSEN	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	3-0	BUSTURNAROUND	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG7_i	6	CSVALID	y	y	y	y	y	y	y	y	y	y

12.3.3.5.6.1 GPMC Timing Parameters Formulas

This section is intended to help the user calculate the GPMC timing bit field values. Formulas are not listed exhaustively.

The section describes:

- NAND flash interface timing parameters formulas
- Synchronous NOR flash timing parameters formulas
- Asynchronous NOR flash timing parameters formulas

For complete information, such as OPP and board effects on timings, see the device-specific Datasheet.

12.3.3.5.6.1.1 NAND Flash Interface Timing Parameters Formulas

This section lists formulas to calculate NAND timing parameters. This is the case when GPMC_CONFIG1_i[11-10] DEVICETYPE = 0x2. Table 12-294 describes the NAND timing parameters.

Table 12-306. NAND Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – GPMC_WEn valid time
B	ns	Delay time – GPMC_CS valid to GPMC_WEn valid
C	ns	Delay time – GPMC_BE0n_CLE/GPMC_ADVn_ALE high to GPMC_WEn valid
D	ns	Delay time – GPMC_AD[15-0] valid to GPMC_WEn valid
E	ns	Delay time – GPMC_WEn invalid to GPMC_AD[15-0] invalid
F	ns	Delay time – GPMC_WEn invalid to GPMC_BE0n_CLE/GPMC_ADVn_ALE invalid
G	ns	Delay time – GPMC_WEn invalid to GPMC_CS invalid
H	ns	Cycle time – Write cycle time
I	ns	Delay time – GPMC_CS valid to GPMC_OEn_REn valid
J	ns	Setup time – GPMC_AD[15-0] valid to GPMC_OEn_REn invalid
K	ns	Pulse duration – GPMC_OEn_REn valid time
L	ns	Cycle time – Read cycle time
M	ns	Delay time – GPMC_OEn_REn invalid to GPMC_CS invalid

The configuration parameters are calculated through the following formulas. For more information, see the device-specific Datasheet.

A = (WEOffTime – WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period

B = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK period

C = ((WEOnTime – ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - ADVExtraDelay)) * GPMC_FCLK period

D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK period

E = (WrCycleTime – WEOffTime * (TimeParaGranularity + 1) – 0.5 * WEExtraDelay) * GPMC_FCLK period

F = (ADVWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – WEExtraDelay) * GPMC_FCLK period

G = (CSWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – WEExtraDelay) * GPMC_FCLK period

H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK period

I = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK period

J = ((RdAccessTime – OEOffTime) * (TimeParaGranularity + 1) – 0.5 * OEExtraDelay)) * GPMC_FCLK period

K = (OEOffTime – OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK period

L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK period

M = (CSRdOffTime – OEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - OEExtraDelay) * GPMC_FCLK period

Figure 12-210 shows a simplified example of command latch cycle timing where formulas are associated with signal waves.

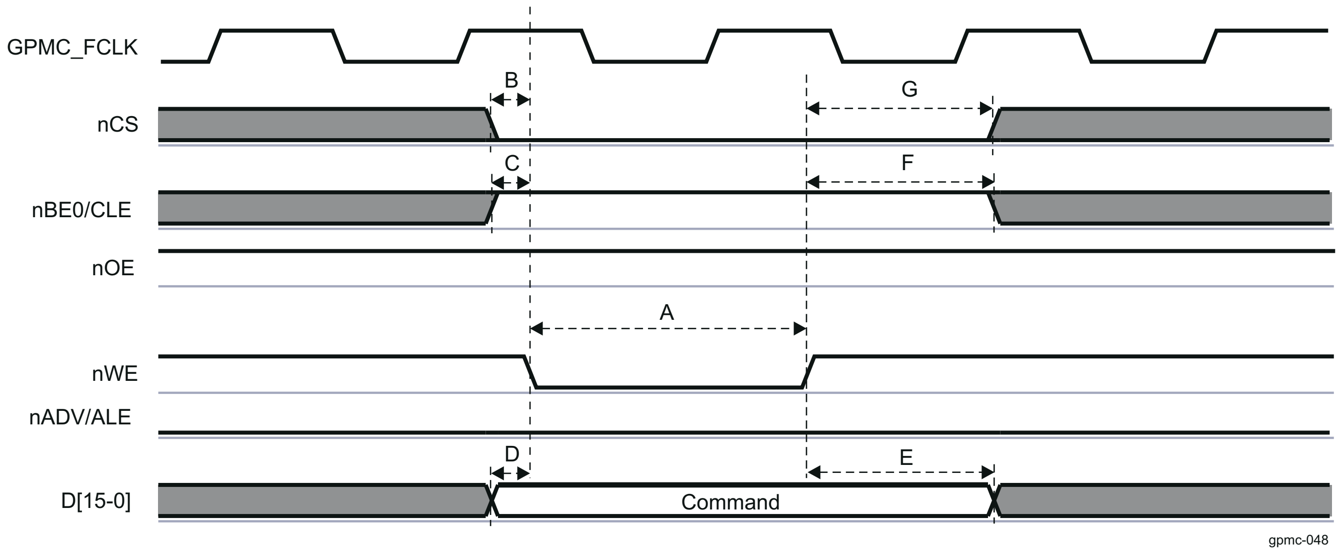

Figure 12-210. NAND Command Latch Cycle Timing Simplified Example

12.3.3.5.6.1.2 Synchronous NOR Flash Timing Parameters Formulas

This section lists all formulas to calculate synchronous NOR timing parameters. This is the case when GPMC_CONFIG1_i[11-10] DEVICETYPE = 0x0 and when READTYPE or WRITETYPE are set to synchronous mode. Table 12-295 describes the synchronous NOR formulas.

Table 12-307. Synchronous NOR Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – nCS low
B	ns	Delay time – address bus valid to CLK first edge
		Delay time – nBE0 / nBE1 valid to CLK first edge
C	ns	Pulse duration – nBE0 / nBE1 low
D	ns	Delay time – CLK rising edge to nBE0 / nBE1 invalid
		Delay time – CLK rising edge to nADV/ALE invalid
E	ns	Delay time – CLK rising edge to nCS invalid
		Delay time – CLK rising edge to nOE/nRE invalid
F	ns	Delay time – CLK rising edge to nCS transition
G	ns	Delay time – CLK rising edge to nADV/ALE transition
H	ns	Delay time – CLK rising edge to nOE/nRE transition
I	ns	Delay time – CLK rising edge to nWE transition
J	ns	Delay time – CLK rising edge to A[16-1/]D[15-0] data bus transition
		Delay time – CLK rising edge to nBE0 / nBE1 transition
K	ns	Pulse duration – nADV/ALE low
L	ns	Delay time – WAIT invalid to first data latching CLK edge

The configuration parameters are calculated through the following formulas. For more information, see the device-specific Datasheet.

1. For single read accesses:
   A = (CSRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = RDCYCLETIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (RDCYCLETIME – RDACCESSTIME) * GPMC_FCLK period
   E = (CSRDOFFTIME – RDACCESSTIME) * GPMC_FCLK period

2. For burst read accesses (where n is the page burst access number):
   A = (CSRDOFFTIME – CSONTIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = (RDCYCLETIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (RDCYCLETIME – (RDACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME)) * GPMC_FCLK period
   E = (CSRDOFFTIME – (RDACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME)) * GPMC_FCLK period
3. For burst write accesses (where n is the page burst access number):
   A = (CSWROFFTIME – CSONTIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = (WRCYCLETIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (WRCYCLETIME – (RDACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME)) * GPMC_FCLK period
   E = (CSWROFFTIME – (RDACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME)) * GPMC_FCLK period
4. For all accesses:
   For nCS falling edge (chip-select activated):
   - Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSONTIME are odd) or (CLKACTIVATIONTIME and CSONTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME) is a multiple of 3
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
     F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

   For nCS rising edge (chip-select deactivated) in reading mode:
   - Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSRDOFFTIME are odd) or (CLKACTIVATIONTIME and CSRDOFFTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
     F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

   For nCS rising edge (chip-select deactivated) in writing mode:
   - Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSWROFFTIME are odd) or (CLKACTIVATIONTIME and CSWROFFTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME) is a multiple of 3

  F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nADV falling edge (nADV activated):

- Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVONTIME are odd) or (CLKACTIVATIONTIME and ADVONTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nADV rising edge (nADV deactivated) in reading mode:

- Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVRDOFFTIME are odd) or (CLKACTIVATIONTIME and ADVRDOFFTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nADV rising edge (nADV deactivated) in writing mode:

- Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVWROFFTIME are odd) or (CLKACTIVATIONTIME and ADVWROFFTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nOE falling edge (nOE activated):

- Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and OEONTIME are odd) or (CLKACTIVATIONTIME and OEONTIME are even)

H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME) is a multiple of 3
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  H = (2 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nOE rising edge (nOE deactivated):
- Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and OEOFFTIME are odd) or (CLKACTIVATIONTIME and OEOFFTIME are even)
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  H = (2 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nWE falling edge (nWE activated):
- Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and WEONTIME are odd) or (CLKACTIVATIONTIME and WEONTIME are even)
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME) is a multiple of 3
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  I = (2 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nWE rising edge (nWE deactivated):
- Case where GPMC_CONFIG1_i[1-0] GPMCFCLKDIVIDER = 0x0:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and WEOFFTIME are odd) or (CLKACTIVATIONTIME and WEOFFTIME are even)
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  I = (2 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nADV low pulse duration:
- Read operation:

K = (ADVRDOFFTIME – ADVONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period

- Write operation:
  K = (ADVWROFFTIME – ADVONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period

For WAIT invalid to first data latching GPMC output clock edge:

- L = WAITMONITORINGTIME * (GPMCFCLKDIVIDER + 1) * GPMC_FCLK period + GPMC output clock period

Figure 12-211 shows a simplified example of a synchronous NOR single read where formulas are associated with signal waves.

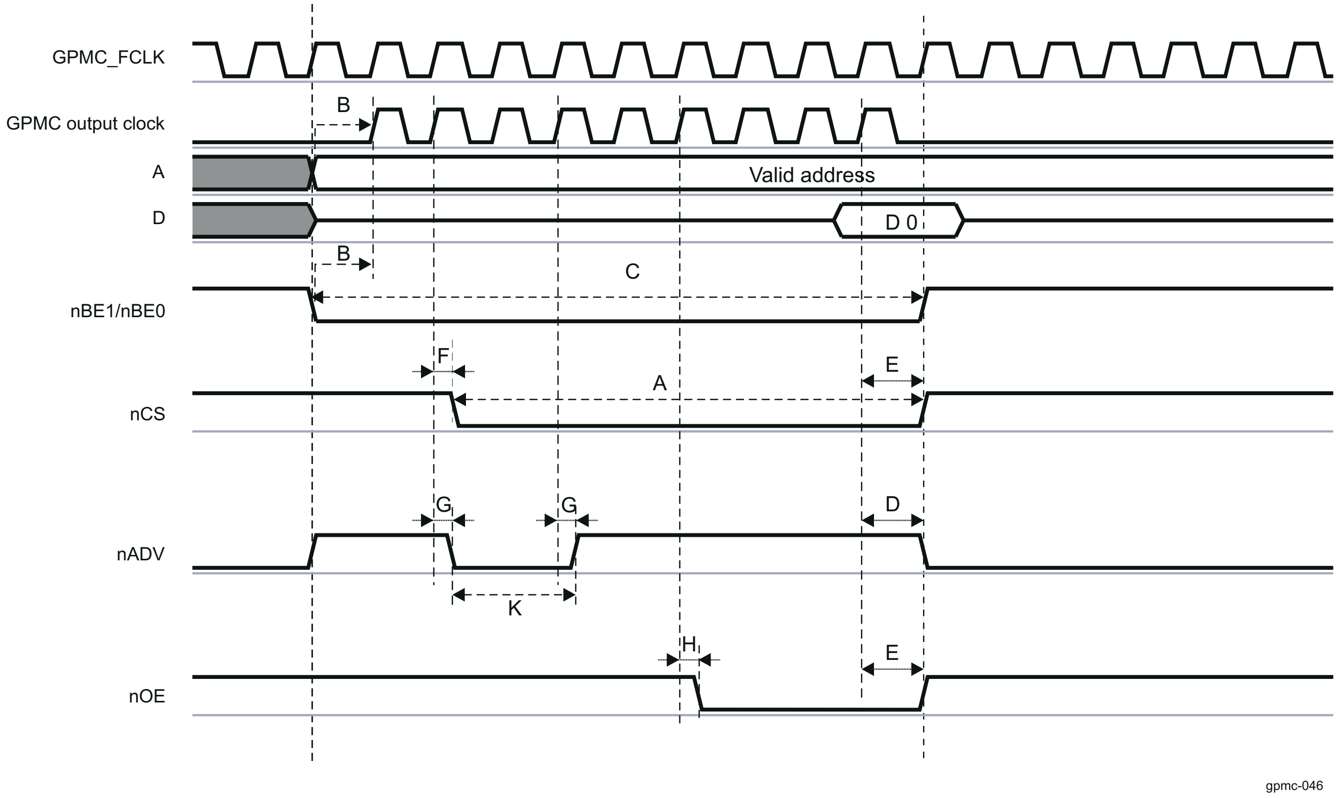

Figure 12-211. Synchronous NOR Single Read Simplified Example

12.3.3.5.6.1.3 Asynchronous NOR Flash Timing Parameters Formulas

This section lists all the formulas to calculate asynchronous NOR timing parameters. This is the case when GPMC_CONFIG1_i[11-10] DEVICETYPE = 0x0 and when READTYPE or WRITETYPE are set to asynchronous mode. Table 12-296 describes the asynchronous NOR formulas.

Table 12-308. Asynchronous NOR Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – nCS low
B	ns	Delay time – nCS valid to nADV/ALE invalid
C	ns	Delay time – nCS valid to nOE/nRE invalid (single read)
D	ns	Pulse duration – address bus valid - 2nd, 3rd and 4th accesses
E	ns	Delay time – nCS valid to nWE valid
F	ns	Delay time – nCS valid to nWE invalid
G	ns	Address invalid duration between two successive R/W accesses
H	ns	Setup time – read data valid before nOE/nRE high

Table 12-308. Asynchronous NOR Formulas Description (continued)

Configuration Parameter	Unit	Description
I	ns	Delay time – nCS valid to nOE/nRE invalid (burst read)
J	ns	Delay time – address bus valid to nCS valid
		Delay time – data bus valid to nCS valid
		Delay time – nBE0 / nBE1 valid to nCS valid
K	ns	Delay time – nCS valid to nADV/ALE valid
L	ns	Delay time – nCS valid to nOE/nRE valid
M	ns	Delay time – nCS valid to first data latching edge
N	ns	Pulse duration – nBE0 / nBE1 valid time
O	ns	Delay time – nCS valid to nADV/ALE valid

The configuration parameters are calculated through the following formulas. These formulas are not exhaustive. For more information, see the device-specific Datasheet.

- nCS low pulse:
  For single read: A = (CSRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst read: A = (CSRDOFFTIME – CSONTIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
  For single write: A = (CSWROFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst write: A = (CSWROFFTIME – CSONTIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
- nCS valid to nADV/ALE invalid delay:
  For reading: B = ((ADVRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
  For writing: B = ((ADVWROFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- C = ((OEOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- D = PAGEBURSTACCESSTIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
- E = ((WEONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (WEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- F = ((WEOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (WEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- G = CYCLE2CYCLEDELAY * GPMC_FCLK period
- H = ((OEOFFTIME – RDACCESSTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * OEEXTRADELAY) * GPMC_FCLK period
- I = ((OEOFFTIME + (N – 1) * PAGEBURSTACCESSTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period, where N = page burst access number
- J = (CSONTIME * (TIMEPARAGRANULARITY + 1) + 0.5 * CSEXTRADELAY) * GPMC_FCLK period
- K = ((ADVONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- L = ((OEONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- M = ((RDACCESSTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) – 0.5 * CSEXTRADELAY) * GPMC_FCLK period
- nBE0 /nBE1 pulse:
  For single read: N = RDCYCLETIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period

For burst read: N = (RDCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
For burst write: N = (WRCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number

- O = ((WRCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period

Figure 12-212 shows a simplified example of an asynchronous NOR single write where formulas are associated with signal waves.

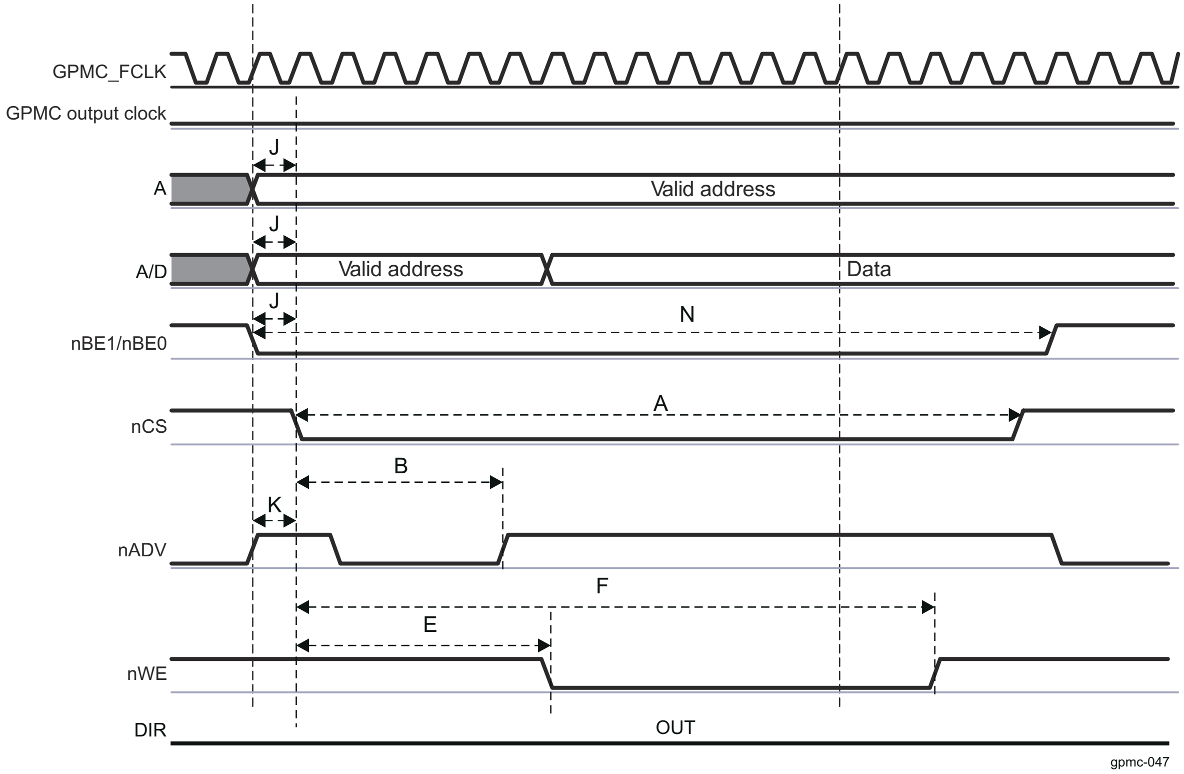

Figure 12-212. Asynchronous NOR Single Write Simplified Example

Note

Write multiple access is not supported in asynchronous mode. If WRITEMULTIPLE is enabled with WRITETYPE as asynchronous, the GPMC processes single asynchronous accesses.

12.3.4 Error Location Module (ELM)

This section describes the Error Location Module (ELM) for the device.

12.3.4.1 ELM Overview

The ELM extracts error addresses from generated syndrome polynomials.

The ELM is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

The General-Purpose Memory Controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-Chaudhuri-Hocquenghem (BCH) algorithm. The ELM extracts error addresses from these syndrome polynomials.

Based on the syndrome polynomial value, the ELM can detect errors, compute the number of errors, and give the location of each error bit. The actual data is not required to complete the error-correction algorithm. Errors can be reported anywhere in the NAND flash block, including in the parity bits.

The maximum acceptable number of errors that can be corrected depends on a programmable configuration parameter. 4-, 8-, and 16-bit error-correction levels are supported. The ELM depends on a static and fixed definition of the generator polynomial for each error-correction level that corresponds to the generator polynomials defined in the GPMC (there are three fixed polynomial for the three correction error levels). A larger number of errors than the programmed error-correction level may be detected, but the ELM cannot correct them all. The offending block is then tagged as *uncorrectable* in the associated computation exit status register. If the computation is successful, that is, if the number of errors detected does not exceed the maximum value authorized for the chosen correction capability, the exit status register contains the information on the number of detected errors.

When the error-location process completes, an interrupt is triggered to inform the software that its status can be checked. The number of detected errors and their locations in the NAND block can be retrieved from the module through register accesses.

Table 12-297 shows the ELM allocation across device domains.

Table 12-309. ELM Allocation Across Device Domains

Instance	Domain	
	MCU	**MAIN**
ELM0	-	✓

Figure 12-213 shows the ELM0 module overview.

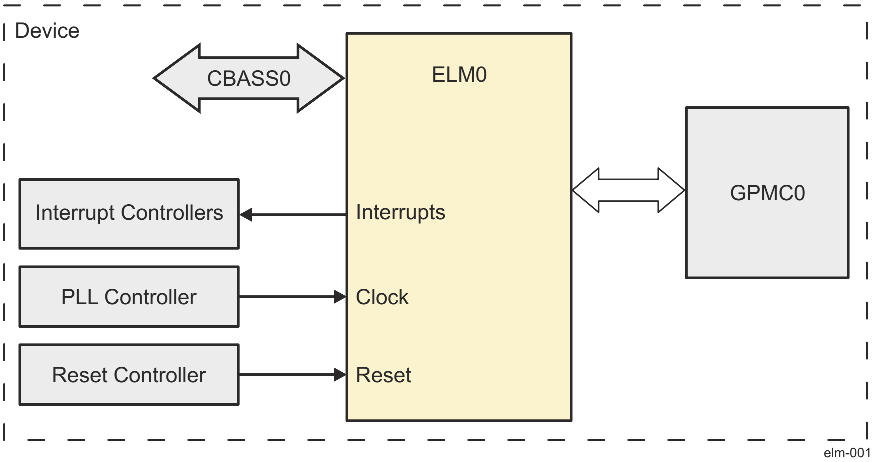

Figure 12-213. ELM0 Overview

12.3.4.1.1 ELM Features

The ELM has the following features:

- 4, 8, and 16 bits per 512-byte block error-location, based on BCH algorithms
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation on error-location process completion:
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode.

12.3.4.1.2 ELM Not Supported Features

The following features are not supported on this family of devices:

- Local power management of clock activity

12.3.4.2 ELM Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

12.3.4.2.1 ELM Integration in MAIN Domain

A single ELM module is integrated in the device MAIN domain - ELM0. Figure 12-214 shows the ELM0 integration.

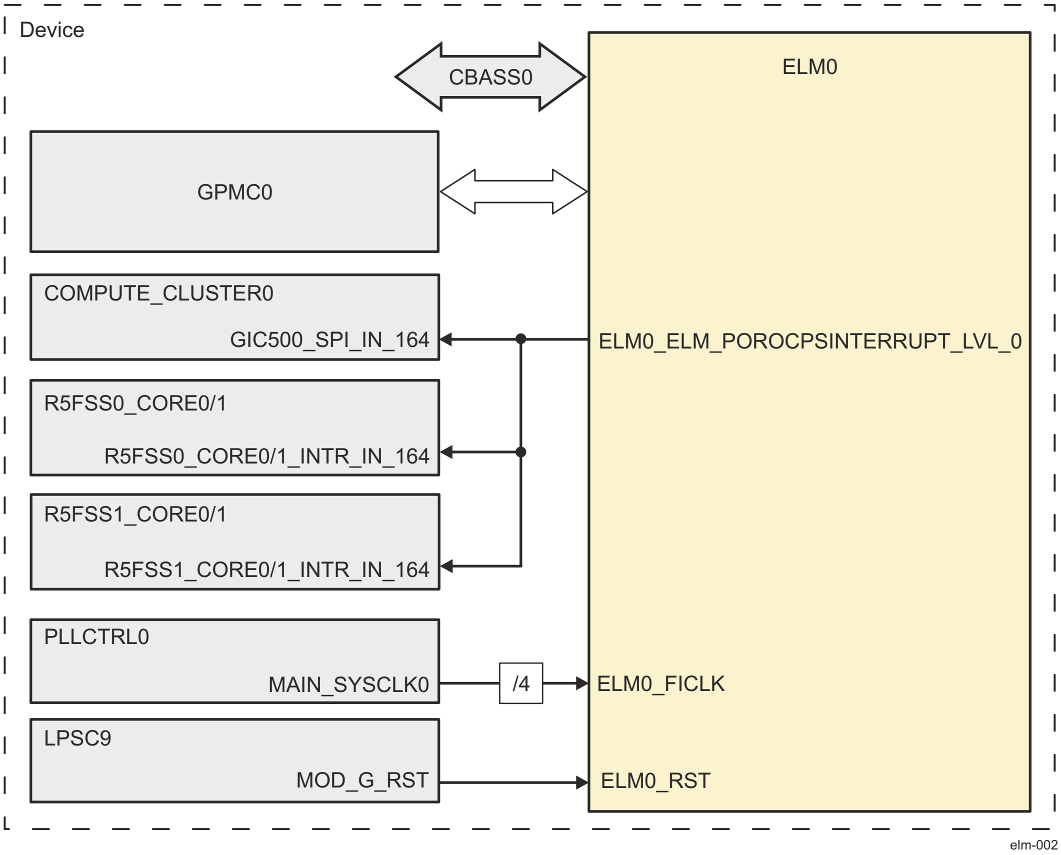

Figure 12-214. ELM0 Integration

Table 12-298 through Table 12-301 summarize the integration of ELM0 in device MAIN domain.

Table 12-310. ELM0 Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
ELM0	PSC0	PD0	LPSC9	CBASS0

Table 12-311. ELM0 Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
ELM0	ELM0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	ELM0 functional and interface clock
		Resets		
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
ELM0	ELM0_RST	MOD_G_RST	LPSC9	ELM0 hardware reset

Table 12-312. ELM0 Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
ELM0	ELM0_RST	MOD_G_RST	LPSC9	ELM0 hardware reset

Table 12-313. ELM0 Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ELM0	ELM0_ELM_POROCPSINTERRUPT_LVL_0	GIC500_SPI_IN_164	COMPUTE_CLUSTER0	Error-location process complete interrupt	Level
		R5FSS0_CORE0_INTR_IN_164	R5FSS0_CORE0	Error-location process complete interrupt	Level
		R5FSS0_CORE1_INTR_IN_164	R5FSS0_CORE1	Error-location process complete interrupt	Level
		R5FSS1_CORE0_INTR_IN_164	R5FSS1_CORE0	Error-location process complete interrupt	Level
		R5FSS1_CORE1_INTR_IN_164	R5FSS1_CORE1	Error-location process complete interrupt	Level

Note

ELM0 interrupts are further described in Section 12.3.4.3.3 , *ELM Interrupt Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.3.4.3 ELM Functional Description

The ELM0 module is hereinafter referred to as ELM.

The ELM is designed around the error-location engine, which handles the computation based on the input syndrome polynomials.

The ELM maps the error-location engine to a standard interconnect interface by using a set of registers to control inputs and outputs.

12.3.4.3.1 ELM Software Reset

To perform a software reset, set the ELM_SYSCONFIG[1] SOFTRESET bit to 1. The ELM_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the ELM_SYSCONFIG[1] SOFTRESET bit is automatically reset.

12.3.4.3.2 ELM Power Management

Note

Some of the ELM features described in this section may not be supported on this family of devices. For more information, see *ELM Not Supported Features*.

Table 12-302 describes the power-management features available to the ELM.

Table 12-314. Local Power-Management Features

Feature	Registers	Description
Clock autogating	ELM_SYSCONFIG[0] AUTOGATING	This bit allows a local power optimization inside the module by gating the ELM_FICLK clock upon the interface activity.
Idle modes	ELM_SYSCONFIG[4-3] SIDLEMODE	Force-idle, no-idle, and smart-idle modes are available.
Clock activity	ELM_SYSCONFIG[8] CLOCKACTIVITY	The clock can be switched off or maintained.

12.3.4.3.3 ELM Interrupt Requests

Table 12-303 lists the event flags, and their masks, that can cause module interrupts asserting the ELM0_ELM_POROCPSINTERRUPT_LVL_0 signal.

Table 12-315. ELM Events

Event Flag	Event Mask	Description
ELM_IRQSTATUS[8] PAGE_VALID	ELM_IRQENABLE[8] PAGE_MASK	Page interrupt
ELM_IRQSTATUS[7] LOC_VALID_7	ELM_IRQENABLE[7] LOCATION_MASK_7	Error-location interrupt for syndrome polynomial 7
ELM_IRQSTATUS[6] LOC_VALID_6	ELM_IRQENABLE[6] LOCATION_MASK_6	Error-location interrupt for syndrome polynomial 6
ELM_IRQSTATUS[5] LOC_VALID_5	ELM_IRQENABLE[5] LOCATION_MASK_5	Error-location interrupt for syndrome polynomial 5
ELM_IRQSTATUS[4] LOC_VALID_4	ELM_IRQENABLE[4] LOCATION_MASK_4	Error-location interrupt for syndrome polynomial 4
ELM_IRQSTATUS[3] LOC_VALID_3	ELM_IRQENABLE[3] LOCATION_MASK_3	Error-location interrupt for syndrome polynomial 3
ELM_IRQSTATUS[2] LOC_VALID_2	ELM_IRQENABLE[2] LOCATION_MASK_2	Error-location interrupt for syndrome polynomial 2
ELM_IRQSTATUS[1] LOC_VALID_1	ELM_IRQENABLE[1] LOCATION_MASK_1	Error-location interrupt for syndrome polynomial 1
ELM_IRQSTATUS[0] LOC_VALID_0	ELM_IRQENABLE[0] LOCATION_MASK_0	Error-location interrupt for syndrome polynomial 0

12.3.4.3.4 ELM Processing Initialization

ELM_LOCATION_CONFIG global setting parameters must be set before using the error-location engine. The ELM_LOCATION_CONFIG[1-0] ECC_BCH_LEVEL bit field defines the error-correction level used (4-, 8-, or 16-bit error correction). The ELM_LOCATION_CONFIG[26-16] ECC_SIZE bit field defines the maximum buffer length beyond which the engine processing no longer looks for errors.

Software can choose to use the ELM in continuous mode or page mode. If all ELM_PAGE_CTRL[i] SECTOR_i bits (i is the syndrome polynomial number, where i = 0 to 7) are reset, continuous mode is used. In any other case, page mode is implicitly selected.

- Continuous mode: Each syndrome polynomial is processed independently. Results for a syndrome can be retrieved and acknowledged at any time, regardless of the status of the other seven processing contexts.
- Page mode: Syndrome polynomials are grouped into atomic entities: only one page can be processed at any given time, even if all eight contexts are not used for this page. Unused contexts are lost and cannot be affected to any other processing. The full page must be acknowledged and cleared before moving to the next page.

For completion interrupts to be generated correctly, all ELM_IRQENABLE[i] LOCATION_MASK_i bits (where i = 0 to 7) must be forced to 0 when in page mode, and set to 1 in continuous mode. Additionally, the ELM_IRQENABLE[8] PAGE_MASK bit must be set to 1 when in page mode.

Software initiates error-location processing by writing a syndrome polynomial into one of the eight possible register sets. Each of these register sets includes seven registers: ELM_SYNDROME_FRAGMENT_0_i to ELM_SYNDROME_FRAGMENT_6_i. The first six registers can be written in any order, but ELM_SYNDROME_FRAGMENT_6_i must be written last because it includes the validity bit, which instructs the ELM that this syndrome polynomial must be processed (the ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit).

As soon as one validity bit is asserted (ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID = 0x1, where i = 0 to 7), error-location processing can start for the corresponding syndrome polynomial. The associated ELM_LOCATION_STATUS_i and ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i registers (where i = 0 to 7) are not reset. Software must not consider them until the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit is set.

12.3.4.3.5 ELM Processing Sequence

While the error-location engine is busy processing one syndrome polynomial, further syndrome polynomials can be written. They are processed when the current processing completes.

The engine completes early when:

- No error is detected; that is, when the ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE bit is set to 1 and the ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS bit field is set to 0x0.
- Too many errors are detected; that is, when the ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE bit is set to 0 while the ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS bit field is set with the value output by the error-location engine. The reported number of errors is not ensured if ECC_CORRECTABLE is 0.

If the engine completes early, the associated error-location registers ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i (where i = 0 to 7) are not updated.

In all other cases, the engine goes through the entire error-location process. Each time an error location is found, it is logged in the associated ECC_ERROR_LOCATION bit field. The first error detected is logged in the ELM_ERROR_LOCATION_0_i[12-0] ECC_ERROR_LOCATION bit field; the second is logged in the ELM_ERROR_LOCATION_1_i[12-0] ECC_ERROR_LOCATION bit field, and so on.

Table 12-304 describes the ELM_LOCATION_STATUS_i value decoding.

Table 12-316. ELM_LOCATION_STATUS_i Value Decoding

ECC_CORRECTABLE Value	ECC_NB_ERRORS Value	Status	Number of Errors Detected	Action Required

Table 12-316. ELM_LOCATION_STATUS_i Value Decoding (continued)

1	0	OK	0	None
1	≠ 0	OK	ECC_NB_ERRORS	Correct the data buffer read based on the ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i results.
0	Any	Failed	Unknown	Software-dependent

12.3.4.3.6 ELM Processing Completion

When the processing for a given syndrome polynomial completes, its ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit is reset. It must not be set again until the exit status registers, ELM_LOCATION_STATUS_i (where i = 0 to 7) for this processing are checked. Failure to comply with this rule leads to potential loss of the first polynomial process data output.

The error-location engine signals the process completion to the ELM. When this event is detected, the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit (where i = 0 to 7) is set. The processing exit status is available from the associated ELM_LOCATION_STATUS_i register, and error locations are stored in order in the ECC_ERROR_LOCATION bit fields. Software must read only valid error-location registers based on the number of errors detected and located.

Immediately after the error-location engine completes, a new syndrome polynomial can be processed, if any is available, as reported by the ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit, depending on the configured error-correction level. If several syndrome polynomials are available, a round-robin arbitration is used to select one for processing.

In continuous mode (that is, all bits in ELM_PAGE_CTRL are reset), an interrupt is triggered whenever a ELM_IRQSTATUS[i] LOC_VALID_i bit is asserted. Software must read the ELM_IRQSTATUS register to determine which polynomial is processed and retrieve the exit status and error locations (ELM_LOCATION_STATUS_i and ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i). When done, software must clear the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit by setting it to 1. Other status bits must be set to 0 so that other interrupts are not unintentionally cleared. When using this mode, the ELM_IRQSTATUS[8] PAGE_VALID interrupt is never triggered.

In page mode, the module does not trigger interrupts for the processing completion of each polynomial because the ELM_IRQENABLE[i] LOCATION_MASK_i bits are cleared. A page is defined using the ELM_PAGE_CTRL register. Each SECTOR_i bit set means the corresponding polynomial i is part of the page processing. A page is fully processed when all tagged polynomials have been processed, as logged in the ELM_IRQSTATUS[i] LOC_VALID_i bits. The module triggers an ELM_IRQSTATUS[8] PAGE_VALID interrupt whenever it detects that the full page has been processed. To make sure the next page can be correctly processed, all status bits in the ELM_IRQSTATUS register must be cleared by using a single atomic-write access.

Note

Do not modify page setting parameters in the ELM_PAGE_CTRL register unless the engine is idle, no polynomial input is valid, and all interrupts have been cleared.

Because no polynomial-level interrupt is triggered in page mode, polynomials cleared in the ELM_PAGE_CTRL[i] SECTOR_i bits (where i = 0 to 7) are processed as usual, but are essentially ignored. Software must manually poll the ELM_IRQSTATUS bits to check for their status.

12.3.4.4 ELM Basic Programming Model

12.3.4.4.1 ELM Low-Level Programming Model

12.3.4.4.1.1 Processing Initialization

Table 12-317. ELM Processing Initialization

Step	Register/Bit Field/Programming Model	Value
Resets the module.	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the target interface power management.	ELM_SYSCONFIG[4-3] SIDLEMODE	Set value
Defines the error-correction level used.	ELM_LOCATION_CONFIG[1-0] ECC_BCH_LEVEL	Set value
Defines the maximum buffer length.	ELM_LOCATION_CONFIG[26-16] ECC_SIZE	Set value
Sets the ELM in continuous mode or page mode.	ELM_PAGE_CTRL	Set value
IF continuous mode is used:	All ELM_PAGE_CTRL[i] SECTOR_i (where i = 0 to 7)	0x0
Enable interrupt for syndrome polynomial i.	ELM_IRQENABLE[i] LOCATION_MASK_i	0x1
ELSE (page mode is used):	One syndrome polynomial i is set ELM_PAGE_CTRL[i] SECTOR_i (where i = 0 to 7)	0x1
Disable all interrupts for syndrome polynomial and enable PAGE_MASK interrupt.	All ELM_IRQENABLE[i] LOCATION_MASK_i = 0x0 and ELM_IRQENABLE[8] PAGE_MASK = 0x1	Set value
ENDIF		Set value
Set the input syndrome polynomial i.	ELM_SYNDROME_FRAGMENT_0_i	Set value
	ELM_SYNDROME_FRAGMENT_1_i	Set value
	ELM_SYNDROME_FRAGMENT_5_i	Set value
	ELM_SYNDROME_FRAGMENT_6_i	Set value
Initiates the computation process.	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID	0x1

12.3.4.4.1.2 Read Results

The engine goes through the entire error-location process and results can be read. Table 12-306 and Table 12-307 describe the processing completion for continuous and page modes, respectively.

Table 12-318. ELM Processing Completion for Continuous Mode

Step	Register/Bit Field/Programming Model	Value
Wait until process is complete for syndrome polynomial i: Wait until the ELM0_ELM_POROCPSINTERRUPT_LVL_0 interrupt is generated, or poll the status register.		
Read for which i the error-location process is complete.	ELM_IRQSTATUS[i] LOC_VALID_i	0x1
IF the process fails (too many errors):	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x0
It is software dependant.		
ELSE (process successful, the engine completes):	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x1
Read the number of errors.	ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS	
Read the error-location bit addresses for syndrome polynomial i of the ECC_NB_ERRORS first registers. Software must correct errors in the data buffer.	ELM_ERROR_LOCATION_0_i[12-0] ECC_ERROR_LOCATION	
	ELM_ERROR_LOCATION_1_i[12-0] ECC_ERROR_LOCATION	
	...	
	ELM_ERROR_LOCATION_15_i[12-0] ECC_ERROR_LOCATION	
ENDIF		
Clear the corresponding i interrupt.	ELM_IRQSTATUS[i] LOC_VALID_i	0x1

A new syndrome polynomial can be processed after the end of processing (ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID = 0x0) and after the exit status register check (ELM_LOCATION_STATUS_i).

Table 12-319. ELM Processing Completion for Page Mode

Step	Register/Bit Field/Programming Model	Value
Wait until process is complete for syndrome polynomial i: Wait until the ELM0_ELM_POROCPSINTERRUPT_LVL_0 interrupt is generated, or poll the status register.		
Wait for page completed interrupt: All error locations are valid.	ELM_IRQSTATUS[8] PAGE_VALID	0x1
Repeat the following actions the necessary number of times. That is, once for each valid defined block in the page.		
Read the process exit status.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	
IF the process fails (too many errors):	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x0
It is software dependent.		
ELSE (process successful, the engine completes):	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x1
Read the number of errors.	ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS	
Read the error-location bit addresses for syndrome polynomial i of the ECC_NB_ERRORS first registers.	ELM_ERROR_LOCATION_0_i[12-0] ECC_ERROR_LOCATION	
	ELM_ERROR_LOCATION_1_i[12-0] ECC_ERROR_LOCATION	
	...	
	ELM_ERROR_LOCATION_15_i[12-0] ECC_ERROR_LOCATION	
ENDIF		
End Repeat		
Clear the ELM_IRQSTATUS register.	ELM_IRQSTATUS	0x1FF

Next page can be correctly processed after a page is fully processed, when all tagged polynomials have been processed (ELM_IRQSTATUS[i] LOC_VALID_i = 0x1 for all syndrome polynomials i used in the page).

12.3.4.4.1.3

Next page can be correctly processed after a page is fully processed, when all tagged polynomials have been processed (ELM_IRQSTATUS[i] LOC_VALID_i = 0x1 for all syndrome polynomials i used in the page).

12.3.4.4.2 Use Case: ELM Used in Continuous Mode

In this example, the ELM is programmed for an 8-bit error-correction capability in continuous mode (see Table 12-308). After reading a 528-byte NAND flash sector (512B data plus 16B spare area) with a 16-bit interface, a nonzero polynomial syndrome is reported from the GPMC (polynomial syndrome 0 is used in the ELM):

- P = 0x0A16ABE115E44F767BFB0D0980.

Table 12-320. Use Case: Continuous Mode

Step	Register/Bit Field/Programming Model	Value
Reset the module.	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the target interface power management: Smart idle is used.	ELM_SYSCONFIG[4-3] SIDLEMODE	0x2
Define the error-correction level used: 8 bits.	ELM_LOCATION_CONFIG[1-0] ECC_BCH_LEVEL	0x1
Define the maximum buffer length: 528 bytes (2 × 528 = 1056).	ELM_LOCATION_CONFIG[26-16] ECC_SIZE	0x420
Set the ELM in continuous mode.	ELM_PAGE_CTRL	0
Enable interrupt for syndrome polynomial 0.	ELM_IRQENABLE[0] LOCATION_MASK_0	0x1

Table 12-320. Use Case: Continuous Mode (continued)

Step	Register/Bit Field/Programming Model	Value
Set the input syndrome polynomial 0.	ELM_SYNDROME_FRAGMENT_0_i (where i = 0)	0xFB0D0980
	ELM_SYNDROME_FRAGMENT_1_i (where i = 0)	0xE44F767B
	ELM_SYNDROME_FRAGMENT_2_i (where i = 0)	0x16ABE115
	ELM_SYNDROME_FRAGMENT_3_i (where i = 0)	0x0000000A
Initiate the computation process.	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 0)	0x1
Wait until process is complete for syndrome polynomial 0: ELM0_ELM_POROCPSINTERRUPT_LVL_0 is generated or poll the status register.		
Read that error-location process is complete for syndrome polynomial 0.	ELM_IRQSTATUS[0] LOC_VALID_0	0x1
Read the process exit status: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 0)	0x1
Read the number of errors: Four errors detected.	ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS (where i = 0)	0x4
Read the error-location bit addresses for syndrome polynomial 0 of the first four registers: Errors are located in the data buffer at decimal addresses 431, 1062, 1909, 3452.	ELM_ERROR_LOCATION_0_i (where i = 0)	0x1AF
	ELM_ERROR_LOCATION_1_i (where i = 0)	0x426
	ELM_ERROR_LOCATION_2_i (where i = 0)	0x775
	ELM_ERROR_LOCATION_3_i (where i = 0)	0xD7C
Clear the corresponding interrupt for polynomial 0.	ELM_IRQSTATUS[0] LOC_VALID_0	0x1

The NAND flash data in the sector are seen as a polynomial of degree 4223 (number of bits in a 528 byte buffer minus 1), with each data bit being a coefficient in the polynomial. When reading from a NAND flash using the GPMC module, computation of the polynomial syndrome assumes that the first NAND word read at address 0x0 contains the highest-order coefficient in the message. Furthermore, in the 16-bit NAND word, bits are ordered from bit 7 to bit 0, and then from bit 15 to bit 8. Based on this convention, an address table of the data buffer can be built. NAND memory addresses in Table 12-309 are given in decimal format.

Table 12-321. 16-Bit NAND Sector Buffer Address Map

NAND Memory Address	Message Bit Addresses in Memory Word															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4215	4214	4213	4212	4211	4210	4209	4208	4223	4222	4221	4220	4219	4218	4217	4216
1	4175	4174	4173	4172	4171	4170	4169	4168	4183	4182	4181	4180	4179	4178	4177	4176
...																
47	3463	3462	3461	3460	3459	3458	3457	3456	3471	3470	3469	3468	3467	3466	3465	3464
48	3447	3446	3445	3444	3443	3442	3441	3440	3455	3454	3453	3452	3451	3450	3449	3448
49	3431	3430	3429	3428	3427	3426	3425	3424	3439	3438	3437	3436	3435	3434	3433	3432
50	3415	3414	3413	3412	3411	3410	3409	3408	3423	3422	3421	3420	3419	3418	3417	3416
...																
255	135	134	133	132	131	130	129	128	143	142	141	140	139	138	137	136
256	119	118	117	116	115	114	113	112	127	126	125	124	123	122	121	120
257	103	102	101	100	99	98	97	96	111	110	109	108	107	106	105	104
258	87	86	85	84	83	82	81	80	95	94	93	92	91	90	89	88
259	71	70	69	68	67	66	65	64	79	78	77	76	75	74	73	72
260	55	54	53	52	51	50	49	48	63	62	61	60	59	58	57	56
261	39	38	37	36	35	34	33	32	47	46	45	44	43	42	41	40
262	23	22	21	20	19	18	17	16	31	30	29	28	27	26	25	24

Table 12-321. 16-Bit NAND Sector Buffer Address Map (continued)

263	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

The table can now be used to determine which bits in the buffer were incorrect and must be flipped. In this example, the first bit to be flipped is bit 4 from the 49th byte read from memory. It is up to the processor to correctly map this word to the copied buffer and flip this bit. The same process must be repeated for all detected errors.

12.3.4.4.3 Use Case: ELM Used in Page Mode

In this example, the ELM module is programmed for a 16-bit error-correction capability in page mode (see Table 12-310). After reading a 528-byte NAND flash sector (512B data plus 16B spare area) with a 16-bit interface, four non-zero polynomial syndromes are reported from the GPMC (polynomial syndrome 0, 1, 2, and 3 are used in the ELM):

- P0 = 0xE8B0 12ADDB5A318E05BE B0693DB28330B5CC A329AA05E0B718EF
- P1 = 0xBAD0 49A0D932C22E6669 0948DF08BE093336 79C6BA10E5F935EB
- P2 = 0x69D9 B86ABCD5EC3697FA A6498FEE54556EA0 1579EF7D60BA3189
- P3 = 0x0

Table 12-322. Use Case: Page Mode

Step	Register/Bit Field/Programming Model	Value
Reset the module	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the target interface power management: Smart idle is used.	ELM_SYSCONFIG[4-3] SIDLEMODE	0x2
Define the error-correction level used: 16 bits	ELM_LOCATION_CONFIG[1-0] ECC_BCH_LEVEL	0x2
Define the maximum buffer length: 528 bytes	ELM_LOCATION_CONFIG[26-16] ECC_SIZE	0x420
Set the ELM in page mode (four blocks in a page)	ELM_PAGE_CTRL[0] SECTOR_0	0x1
	ELM_PAGE_CTRL[1] SECTOR_1	0x1
	ELM_PAGE_CTRL[2] SECTOR_2	0x1
	ELM_PAGE_CTRL[3] SECTOR_3	0x1
Disable all interrupts for syndrome polynomial and enable PAGE_MASK interrupt.	ELM_IRQENABLE	0x100
Set the input syndrome polynomial 0.	ELM_SYNDROME_FRAGMENT_0_i (where i = 0)	0xE0B718EF
	ELM_SYNDROME_FRAGMENT_1_i (where i = 0)	0xA329AA05
	ELM_SYNDROME_FRAGMENT_2_i (where i = 0)	0x8330B5CC
	ELM_SYNDROME_FRAGMENT_3_i (where i = 0)	0xB0693DB2
	ELM_SYNDROME_FRAGMENT_4_i (where i = 0)	0x318E05BE
	ELM_SYNDROME_FRAGMENT_5_i (where i = 0)	0x12ADDB5A
	ELM_SYNDROME_FRAGMENT_6_i (where i = 0)	0xE8B0
Set the input syndrome polynomial 1.	ELM_SYNDROME_FRAGMENT_0_i (where i = 1)	0xE5F935EB
	ELM_SYNDROME_FRAGMENT_1_i (where i = 1)	0x79C6BA10
	ELM_SYNDROME_FRAGMENT_2_i ((where i = 1)	0xBE093336
	ELM_SYNDROME_FRAGMENT_3_i (where i = 1)	0x0948DF08
	ELM_SYNDROME_FRAGMENT_4_i (where i = 1)	0xC22E6669
	ELM_SYNDROME_FRAGMENT_5_i (where i = 1)	0x49A0D932
	ELM_SYNDROME_FRAGMENT_6_i (where i = 1)	0xBAD0
Set the input syndrome polynomial 2.	ELM_SYNDROME_FRAGMENT_0_i (where i = 2)	0x60BA3189
	ELM_SYNDROME_FRAGMENT_1_i (where i = 2)	0x1579EF7D
	ELM_SYNDROME_FRAGMENT_2_i (where i = 2)	0x54556EA0
	ELM_SYNDROME_FRAGMENT_3_i (where i = 2)	0xA6498FEE

Table 12-322. Use Case: Page Mode (continued)

Step	Register/Bit Field/Programming Model	Value
	ELM_SYNDROME_FRAGMENT_4_i (where i = 2)	0xEC3697FA
	ELM_SYNDROME_FRAGMENT_5_i (where i = 2)	0xB86ABCD5
	ELM_SYNDROME_FRAGMENT_6_i (where i = 2)	0x69D9
Set the input syndrome polynomial 3.	ELM_SYNDROME_FRAGMENT_0_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_1_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_2_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_3_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_4_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_5_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_6_i (where i = 3)	0x0
Initiate the computation process for syndrome polynomial 0	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 0)	0x1
Initiate the computation process for syndrome polynomial 1	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 1)	0x1
Initiate the computation process for syndrome polynomial 2	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 2)	0x1
Initiate the computation process for syndrome polynomial 3	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 3)	0x1
Wait until process is complete for syndrome polynomial 0, 1, 2, and 3: Wait until the ELM0_ELM_POROCPSINTERRUPT_LVL_0 interrupt is generated or poll the status register.		
Wait for page completed interrupt: All error locations are valid.	ELM_IRQSTATUS[8] PAGE_VALID	0x1
Read the process exit status for syndrome polynomial 0: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 0)	0x1
Read the process exit status for syndrome polynomial 1: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 1)	0x1
Read the process exit status for syndrome polynomial 2: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 2)	0x1
Read the process exit status for syndrome polynomial 3: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 3)	0x1
Read the number of errors for syndrome polynomial 0: four errors detected.	ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS (where i = 0)	0x4
Read the number of errors for syndrome polynomial 1: two errors detected.	ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS (where i = 1)	0x2
Read the number of errors for syndrome polynomial 2: one error detected.	ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS (where i = 2)	0x1
Read the number of errors for syndrome polynomial 3: no errors detected.	ELM_LOCATION_STATUS_i[4-0] ECC_NB_ERRORS (where i = 3)	0x0
Read the error-location bit addresses for syndrome polynomial 0 of the first four registers:	ELM_ERROR_LOCATION_0_i (where i = 0)	0x1FE
	ELM_ERROR_LOCATION_1_i (where i = 0)	0x617
	ELM_ERROR_LOCATION_2_i (where i = 0)	0x650
	ELM_ERROR_LOCATION_3_i (where i = 0)	0xA83
Read the error-location bit addresses for syndrome polynomial 1 of the first two registers:	ELM_ERROR_LOCATION_0_i (where i = 1)	0x4
	ELM_ERROR_LOCATION_1_i (where i = 1)	0x1036

Table 12-322. Use Case: Page Mode (continued)

Step	Register/Bit Field/Programming Model	Value
Read the errors location bit addresses for syndrome polynomial 2 of the first registers:	ELM_ERROR_LOCATION_0_i (where i = 1)	0x3E8
Clear the ELM_IRQSTATUS register.	ELM_IRQSTATUS	0x1FF

12.3.5 Multi-Media Card Secure Digital (MMCSD) Interface

This section describes the MMCSD modules in the device.

12.3.5.1 MMCSD Overview

There are two MMCSD modules inside the device - MMCSD0 and MMCSD1. Each MMCSD module includes one MMCSD Host Controller.

Each controller has the following data bus width:

- MMCSD0 - 8-bit wide data bus
- MMCSD1 - 4-bit wide data bus

Table 12-311 shows MMCSD allocation across device domains.

Table 12-323. MMCSD Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
MMCSD0	-	✓
MMCSD1	-	✓

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded Multi-Media Card), SD 4.10 (Secure Digital), and SDIO 3.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

The MMCSD Host Controller provides accessibility to external MMC/SD/SDIO devices using a Programmed IO method or DMA data transfer method. In programmed IO method, the device CPU transfers data using the Buffer Data Port register (MMCSD0_DATA_PORT / MMCSD1_DATA_PORT). In DMA data transfer method, the MMCSD Host Controller can read or write memory without device CPU intervention.

Figure 12-215 shows the MMCSDi module overview (where i = 0 to 1).

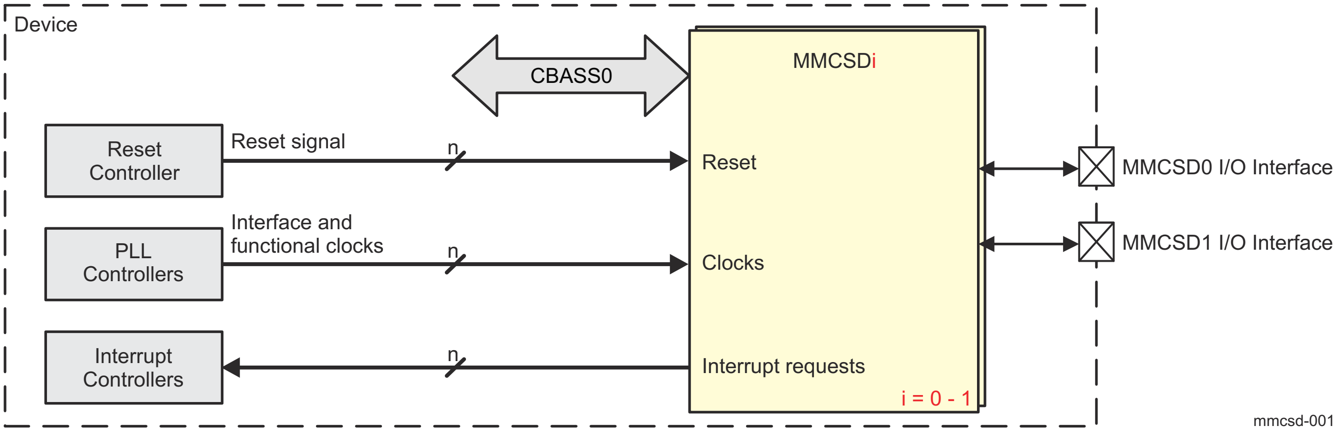

Figure 12-215. MMCSDi Module Overview

12.3.5.1.1 MMCSD Features

Each MMCSD Host Controller supports:

- Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3 (for more information about ADMA support, see Section 12.3.5.4.5 , *Advanced DMA*)
- System Bus Interface:
  - 64-bit data width (host interface)
  - 64-bit address
  - Clock asynchronous to MMCSD clock (MMCi_CLK)
  - Little endian only
- Configuration Bus Interface:
  - 32-bit data width (target interface)
  - Linear incrementing addressing mode
  - 32-bit aligned accesses only
  - Little endian only
- Muxing of other LVCMOS interfaces onto the MMCSD interface at the SoC level (MMCSD1 only)

MMCSD0 Host Controller (eMMC interface):

- Multi-Media Card Support:
  - eMMC Electrical Standard 5.1 (JESD84-B51)
  - Backward compatible with earlier eMMC standards
  - Legacy MMC SDR:
    - 1.8 V, 8-bit bus width, 0-25 MHz, 25 MBps
    - 1.8 V, 4-bit bus width, 0-25 MHz, 12.5 MBps
    - 1.8 V, 1-bit bus width, 0-25 MHz, 3.125 MBps
  - High Speed SDR:
    - 1.8 V, 8-bit bus width, 0-50 MHz, 50 MBps
    - 1.8 V, 4-bit bus width, 0-50 MHz, 25 MBps
    - 1.8 V, 1-bit bus width, 0-50 MHz, 6.25 MBps
  - High Speed DDR:
    - 1.8 V, 8-bit bus width, 0-50 MHz, 100 MBps
    - 1.8 V, 4-bit bus width, 0-50 MHz, 50 MBps
  - HS200 SDR:
    - 1.8 V, 0-200 MHz, 8-bit bus width, 200 MBps
    - 1.8 V, 0-200 MHz, 4-bit bus width, 100 MBps

MMCSD1 Host Controller (SD/SDIO interface):

-
- Secure Digital Card Support:
  - Backward compatible with earlier SD card specifications
  - SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01
  - SDIO Specification v3.00
  - Default Speed mode: 3.3 V signaling, frequency up to 25 MHz, up to 12.5 MBps
  - High Speed mode: 3.3 V signaling, frequency up to 50 MHz, up to 25 MBps
  - SDR12: UHS-I 1.8 V signaling, frequency up to 25 MHz, up to 12.5 MBps
  - SDR25: UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 25 MBps
  - SDR50: UHS-I 1.8 V signaling, frequency up to 100 MHz, up to 50 MBps
  - DDR50: UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 50 MBps
  - SDR104: UHS-I 1.8 V signaling, frequency up to 200 MHz, up to 100 MBps

12.3.5.1.2 MMCSD Not Supported Features

MMCSD0 Host Controller:

- Multi-Media Card:

  - 3.3 V, 3.0 V and 1.2 V
  - Secure Digital Card and SDIO
  - Muxing of other LVCMOS interfaces onto the MMCSD interface at the SoC level
  - HS400 DDR:
    - 1.8 V, 0-200 MHz, 8-bit bus width, 400 MBps

MMCSD1 Host Controller:

- Multi-Media Card
- Secure Digital Card:
  - UHS-II

12.3.5.2 MMCSD Environment

The MMCSD0 and MMCSD1 modules are hereinafter referred to as MMCSDi module.

This section describes the MMCSDi external connections (environment).

The MMCSD0 can be used for connection to 1, 4, or 8-bit devices (dedicated for connection to eMMC devices). The MMCSD1 can be used for connection to 1 or 4-bit devices (dedicated for connection to SD or SDIO devices). For each MMCSD an integrated UHS-I PHY provides interface to external device.

Figure 12-216 shows the MMCSDi (where i = 0 to 1) connected to MMC, SD, or SDIO device.

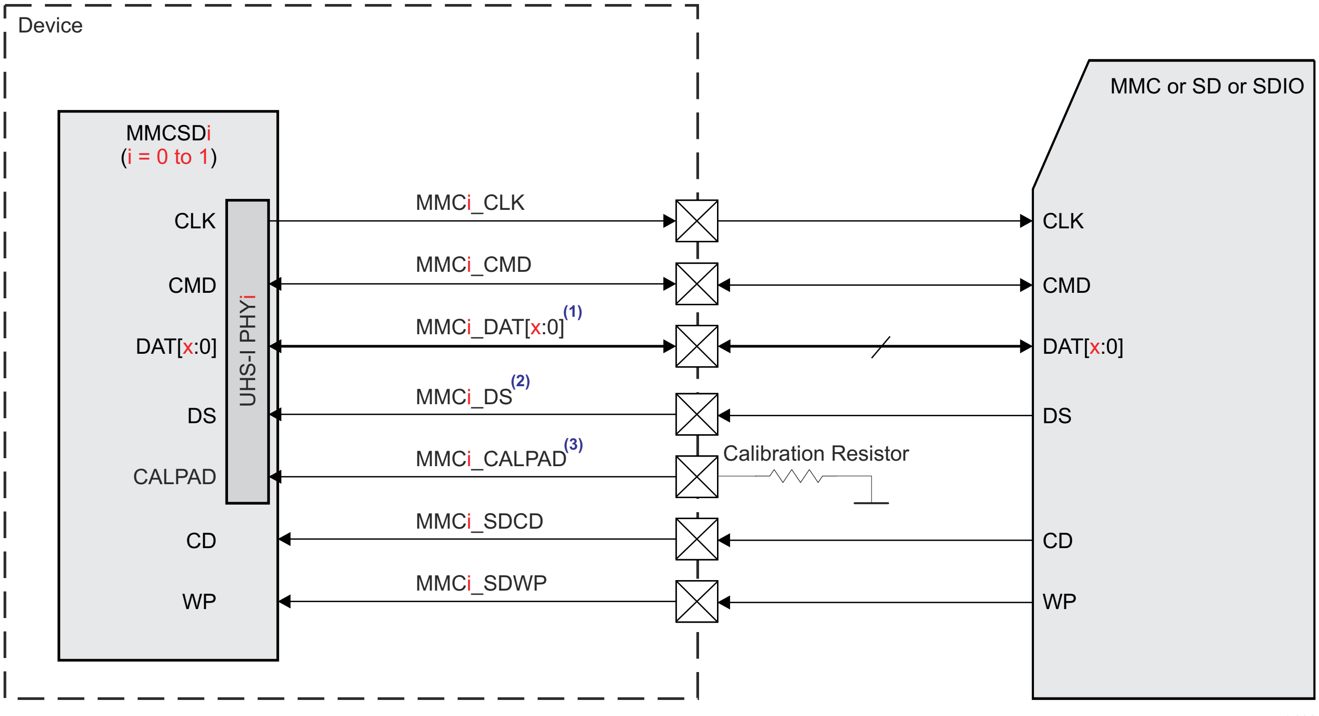

(1) x = 7 for MMCSD0 (8-bit wide data bus); x = 3 for MMCSD1 (4-bit wide data bus);
(2) Used for HS400 mode (MMCSD0 Only);
(3) Used for PHY Calibaration Resistor (MMCSD0 Only);

Figure 12-216. MMCSDi Connected to MMC, SD, or SDIO Device

Table 12-312 describes the MMCSDi I/O signals.

Table 12-324. MMCSDi I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value
		MMCSD0		
CLK	MMC0_CLK	O	External Clock	0x0
CMD	MMC0_CMD	I/O	Command Line	0x0
DAT[7:0]	MMC0_DAT[7:0]	I/O	Data Signals	0x0
DS	MMC0_DS	I	Data Strobe	0x0
CALPAD	MMC0_CALPAD[2]	A	PHY Calibration Resistor	HiZ
		MMCSD1		
CLK	MMC1_CLK	O	External Clock	0x0
CMD	MMC1_CMD	I/O	Command Line	0x0
DAT[3:0]	MMC1_DAT[3:0]	I/O	Data Signals	0x0
WP	MMC1_SDWP	I	SD Card Write Protect	0x1
CD	MMC1_SDCD	I	SD Card Detect	0x0

(1) I = Input; O = Output; HiZ = High Impedance; A = Analog

(2) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

Note

For MMC1_CLK signal to work properly, the RXACTIVE bit of the register should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), refer to the device-specific Datasheet.

12.3.5.2.1 MMCSD IO Mulitplexer

Figure 12-217 describes the IOMUX_ENABLE multilplexer, which is controlled by the MMC_SSCFG_PHY_CTRL_1_REG[31] IOMUX_ENABLE bit.

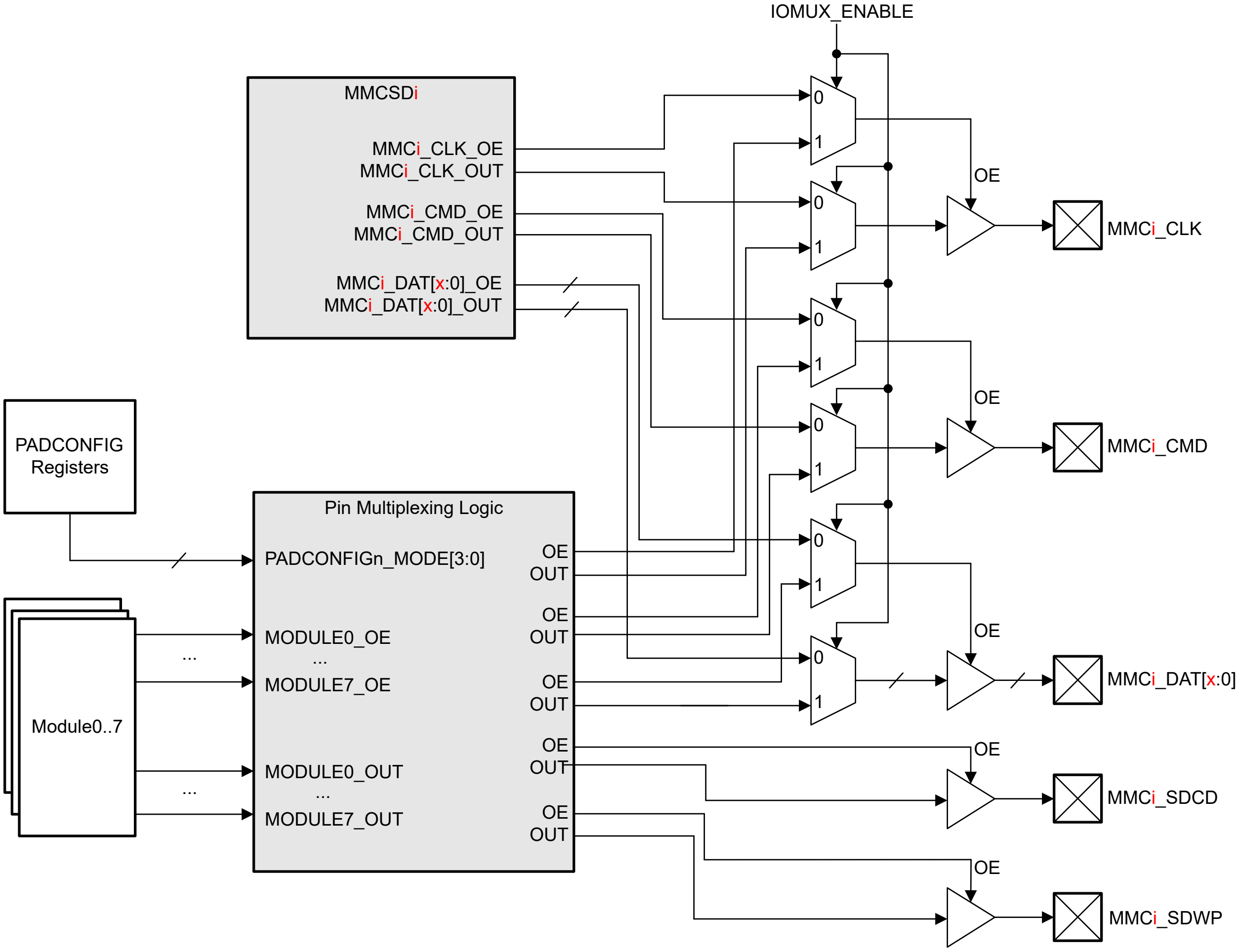

Note

i represents a valid instance of 4-bit MMCSD only. See the device data sheet for specifics.

Note

x=3 for MMCSD (4-bit wide data bus)

Note

Only MMCi_CLK, MMCi_CMD and MMCi_DAT[n:0] are routed through the IOMUX_ENABLE multiplexer. MMCi_SDCD and MMCi_SDWP are not routed through the IOMUX_ENABLE multiplexer.

Note

The IOMUX_ENABLE multiplexer does not affect the signal functions selected from the respective PADCONFIG register for the MMCi_SDCD or MMCi_SDWP pins.

Figure 12-217. MMCSD IOMUX_ENABLE Multiplexer

12.3.5.2.2 Protocol and Data Format

The bus protocol between the MMCSD Host Controller and the card is message-based. Each message is represented by one of the following parts:

- Command: A command starts an operation. The command is transferred serially from the MMCSD Host Controller to the card on the CMD line.
- Response: A response is an answer to a command. The response is sent from the card to the MMCSD Host Controller. It is transferred serially on the CMD line.
- Data: Data are transferred from the MMCSD Host Controller to the card or from the card to the MMCSD Host Controller using the data lines.
- Busy: The DAT[0] signal is maintained low by the card as far as it is programming the data received.
- CRC status: The CRC result is sent by the card through the DAT[0] line when executing a write transfer. In the case of transmission error, occurring on any of the active data lines, the card sends a negative CRC status on DAT[0]. In the case of successful transmission, over all active data lines, the card sends a positive CRC status on DAT[0] and starts the data programming procedure.

12.3.5.2.2.1 Protocol

There are two types of data transfer:

- Sequential operation
- Block-oriented operation

There are specific commands for each type of operation (sequential or block-oriented).

For information about commands and programming sequences supported by the MMC, SD, and SDIO devices, see the *Multi-Media Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification (Part E1)*.

Figure 12-218 and Figure 12-219 show how sequential operations are defined. Sequential operation is only for 1-bit transfer and initiates a continuous data stream. The transfer terminates when a stop command follows on the CMD line.

Note

Stream commands are supported only by MMCs.

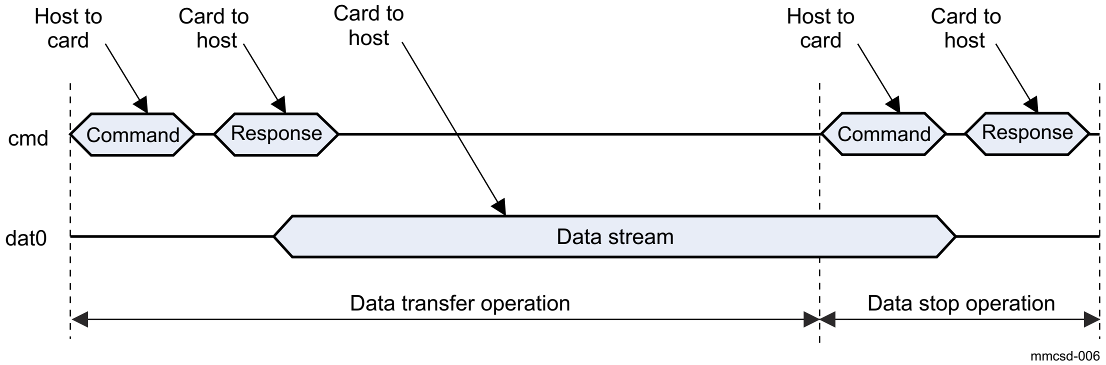

Figure 12-218. Sequential Read Operation (MMCs Only)

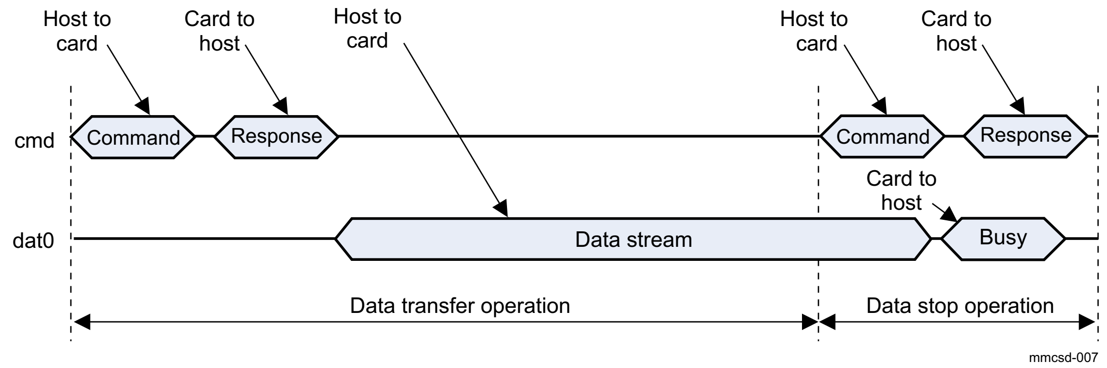

Figure 12-219. Sequential Write Operation (MMCs Only)

Figure 12-220 and Figure 12-221 show how multiple block-oriented operations are defined. A multiple block-oriented operation sends a data block plus CRC bits. The transfer terminates when a stop command follows on the CMD line. These operations are available for all kinds of devices (MMC, SD, SDIO).

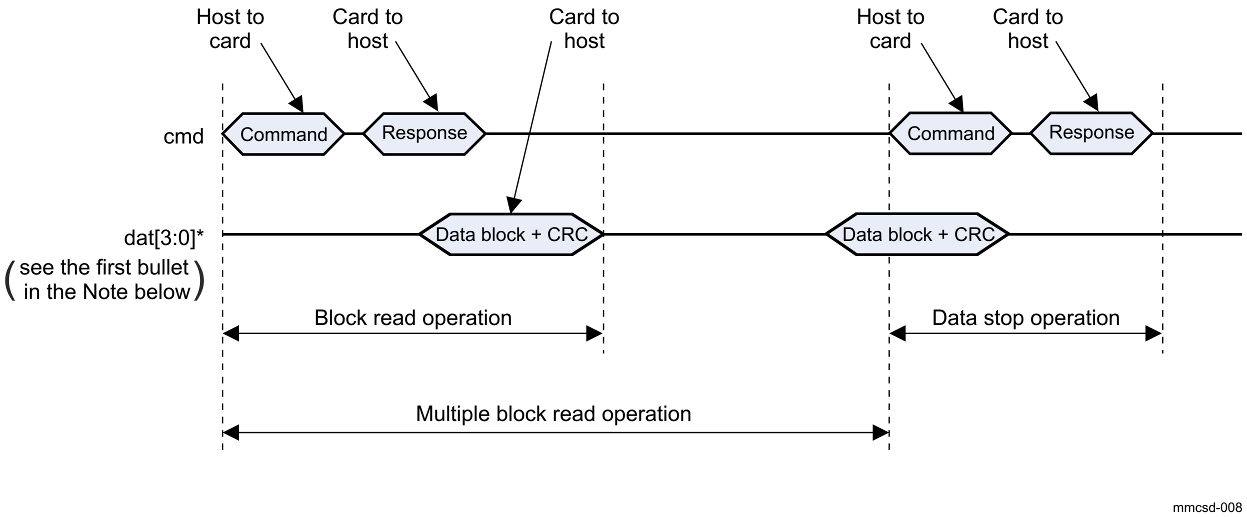

Figure 12-220. Multiple Block Read Operation

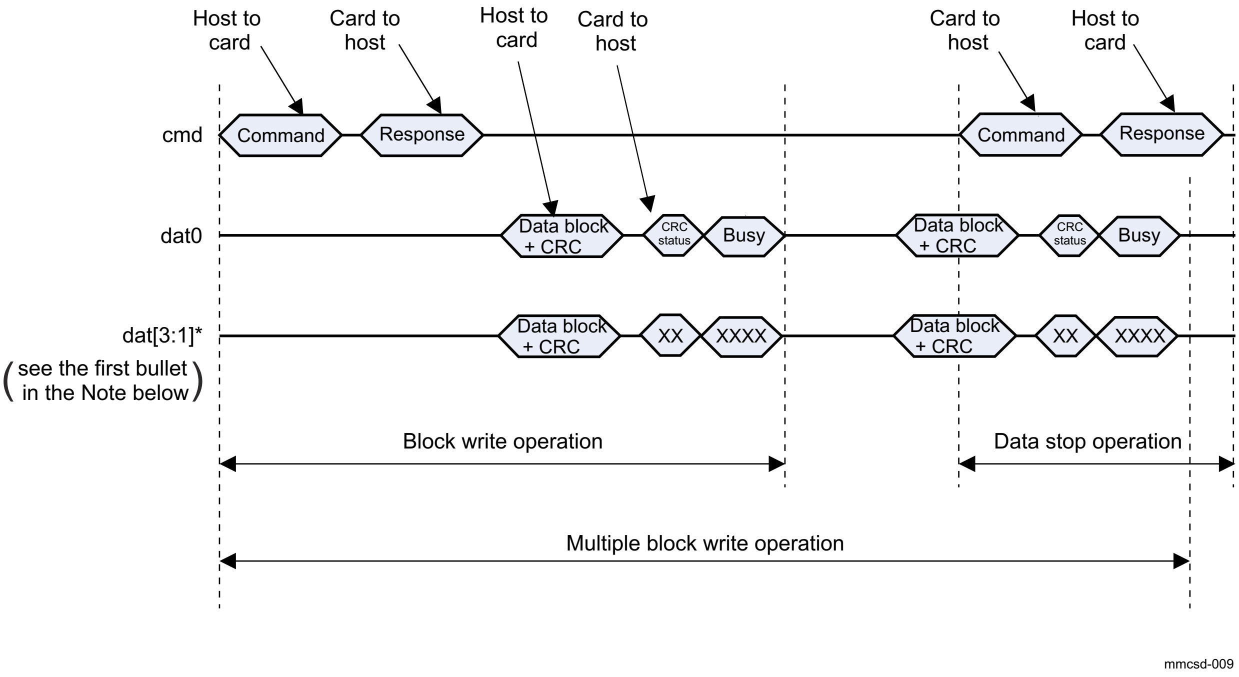

Figure 12-221. Multiple Block Write Operation With Card Busy Signal

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Note

- The card busy signal is not always generated by the card. Refer to Figure 12-220 and Figure 12-221, that show a particular case.
- Software must perform a software reset (see MMCSD0_SOFTWARE_RESET / MMCSD1_SOFTWARE_RESET register) after a data time-out to ensure that MMCi_CLK is stopped.
- For multiblock transfer, and especially for MMC devices, a transfer can be aborted without using a stop command. If a CMD23 is used before data transfer to define the number of blocks that will be transferred, then the transfer stops automatically after the last block (if the MMCs supports this feature).

12.3.5.2.2.2 Data Format

12.3.5.2.2.2.1 Coding Scheme for Command Token

Command tokens always start with 0 and end with 1. The second bit is a transmitter bit: 1 for a host command. The content is the command index (coded by 6 bits) and an argument (for example, an address), coded by 32 bits. The content is protected by 7-bit CRC checksum (see Figure 12-222).

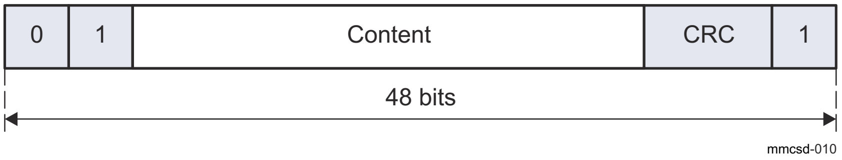

Figure 12-222. Command Token Format

12.3.5.2.2.2.2 Coding Scheme for Response Token

Response tokens always start with 0 and end with 1. The second bit is a transmitter bit: 0 for a card response. The content is different for each type of response (R1, R2, R3, R4, and R5, R6, R7 [for SD]) and the content is protected by 7-bit CRC checksum (see Figure 12-223 and Figure 12-224). Depending on the type of commands sent to the card, the MMCSD0_COMMAND / MMCSD1_COMMAND register must be configured differently to avoid false CRC or index errors to be flagged on command response (see Table 12-313). For more information about response types, see the *Multi-Media Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification (Part E1)*.

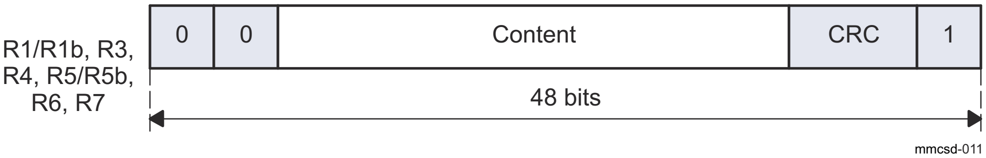

Figure 12-223. Response Token Format (R1/R1b, R3, R4, R5/R5b, R6, R7)

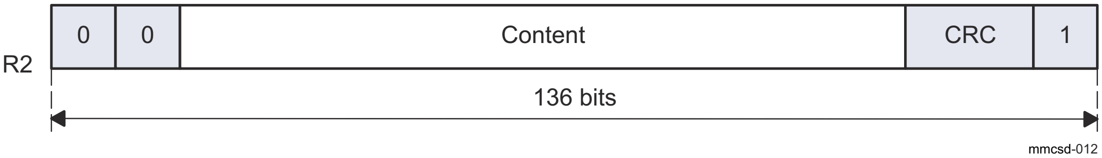

Figure 12-224. Response Token Format (R2)

Table 12-325. Relationship Between Configuration and Name of Response Type

Response Type MMCSD0_COMMAND[1-0] RESP_TYPE_SEL / MMCSD1_COMMAND[1-0] RESP_TYPE_SEL	Index Check Enable MMCSD0_COMMAND[4] CMD_INDEX_CHK_ENA / MMCSD1_COMMAND[4] CMD_INDEX_CHK_ENA	CRC Check Enable MMCSD0_COMMAND[3] CMD_CRC_CHK_ENA / MMCSD1_COMMAND[3] CMD_CRC_CHK_ENA	Name of Response Type
00	0	0	No response
01	0	1	R2
10	0	0	R3 (R4 for SD cards)
10	1	1	R1, R6, R5, (R7 for SD cards)
11	1	1	R1b, R5b

12.3.5.2.2.2.3 Coding Scheme for Data Token

Data tokens always start with 0 and end with 1 (see Figure 12-225 through Figure 12-227).

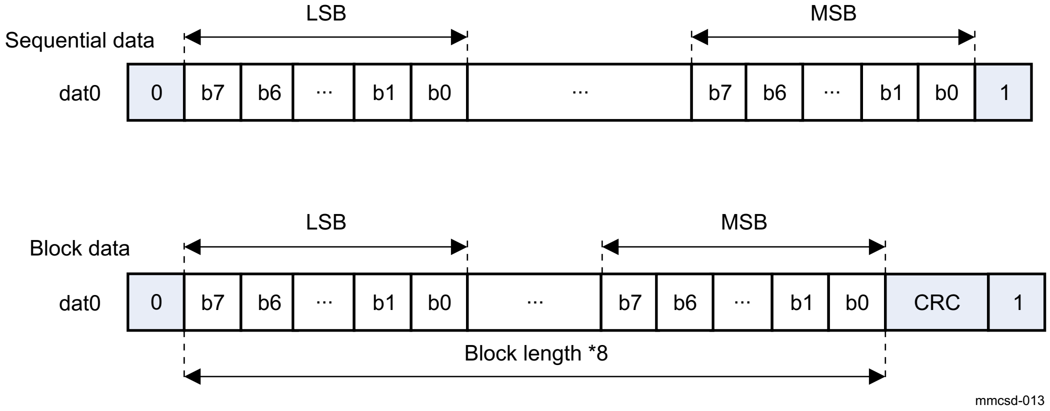

Figure 12-225. Data Token Format for 1-Bit Transfers

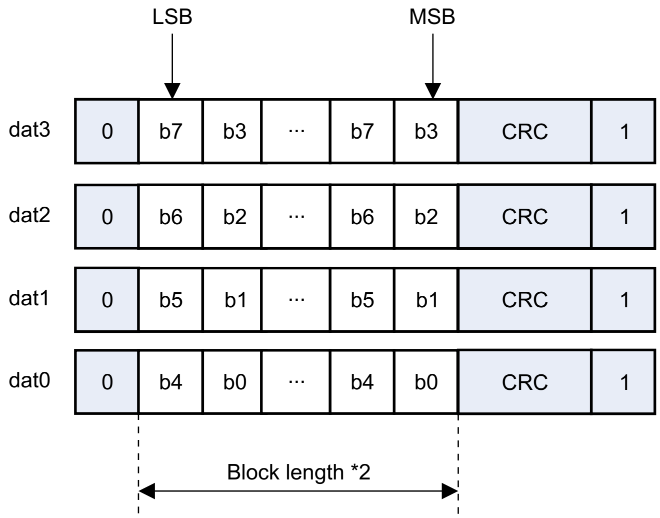

mmcsd-014

Figure 12-226. Data Token Format for 4-Bit Transfers

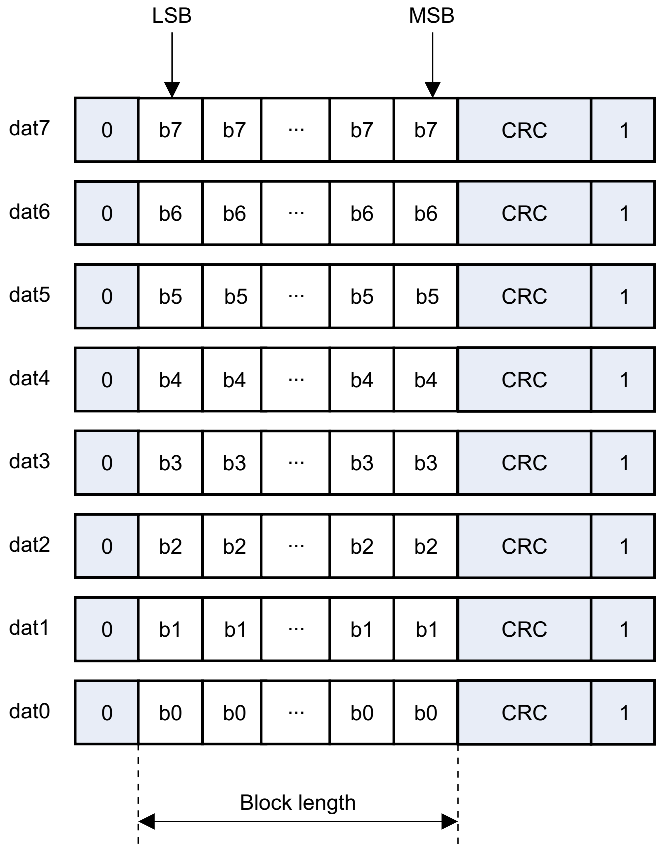

mmcsd-015

Figure 12-227. Data Token Format for 8-Bit Transfers

12.3.5.3 MMCSD Integration

This section describes the MMCSD integration in the device, including information about clocks, resets, and hardware requests.

12.3.5.3.1 MMCSD Integration in MAIN Domain

There are two MMCSD modules integrated in the device MAIN domain - MMCSD0 and MMCSD1. Figure 12-228 shows the integration of MMCSD0 and MMCSD1.

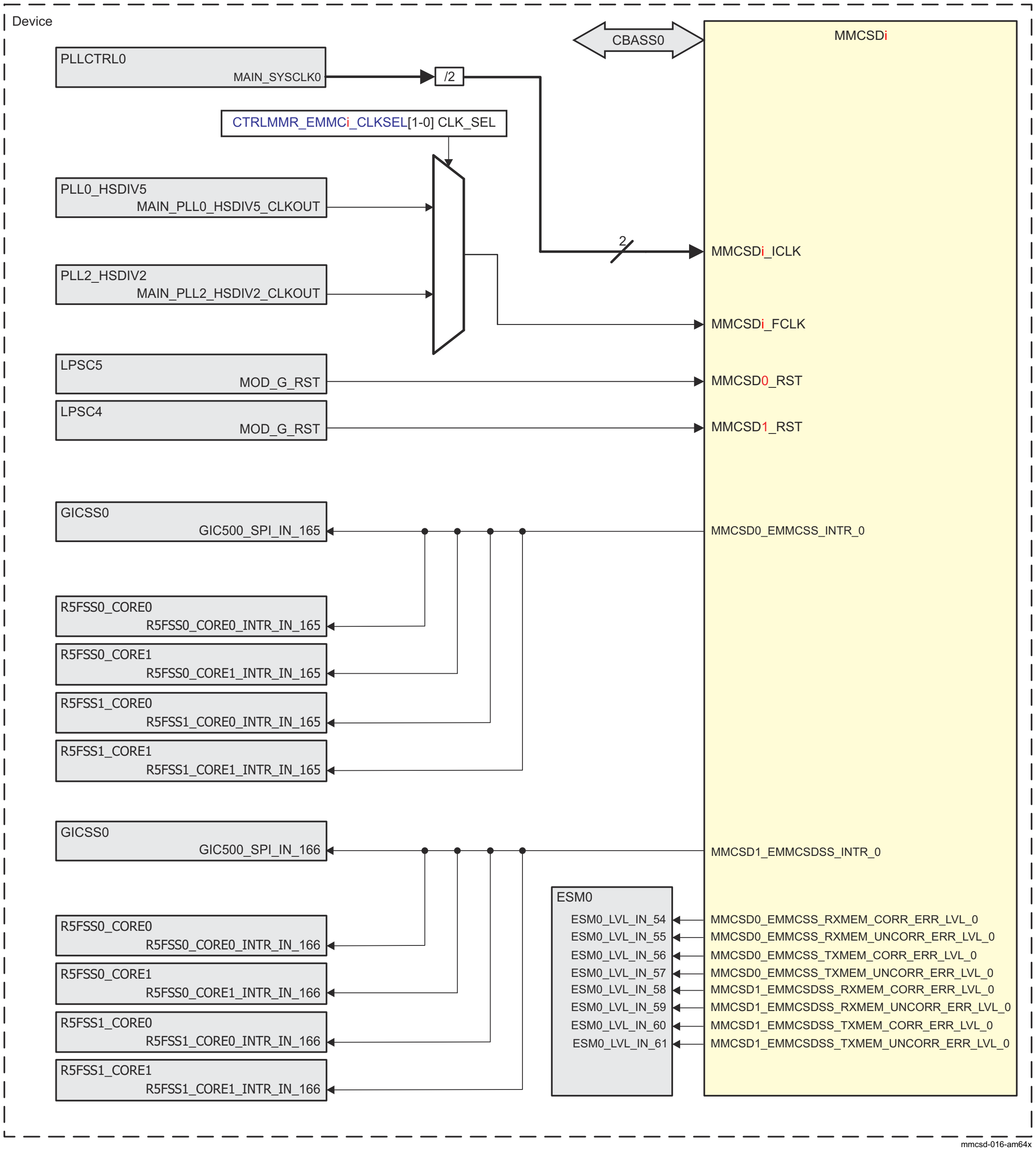
Device
PLLCTRL0
MAIN_SYSCLK0
/2
CBASS0
MMCSDi
CTRLMMR_EMMCi_CLKSEL[1-0] CLK_SEL
PLL0_HSDIV5
MAIN_PLL0_HSDIV5_CLKOUT
PLL2_HSDIV2
MAIN_PLL2_HSDIV2_CLKOUT
2
MMCSDi_ICLK
MMCSDi_FCLK
LPSC5
MOD_G_RST
MMCSD0_RST
LPSC4
MOD_G_RST
MMCSD1_RST
GICSS0
GIC500_SPI_IN_165
MMCSD0_EMMCSS_INTR_0
R5FSS0_CORE0
R5FSS0_CORE0_INTR_IN_165
R5FSS0_CORE1
R5FSS0_CORE1_INTR_IN_165
R5FSS1_CORE0
R5FSS1_CORE0_INTR_IN_165
R5FSS1_CORE1
R5FSS1_CORE1_INTR_IN_165
GICSS0
GIC500_SPI_IN_166
MMCSD1_EMMCSDSS_INTR_0
ESM0
ESM0_LVL_IN_54
ESM0_LVL_IN_55
ESM0_LVL_IN_56
ESM0_LVL_IN_57
ESM0_LVL_IN_58
ESM0_LVL_IN_59
ESM0_LVL_IN_60
ESM0_LVL_IN_61
MMCSD0_EMMCSS_RXMEM_CORR_ERR_LVL_0
MMCSD0_EMMCSS_RXMEM_UNCORR_ERR_LVL_0
MMCSD0_EMMCSS_TXMEM_CORR_ERR_LVL_0
MMCSD0_EMMCSS_TXMEM_UNCORR_ERR_LVL_0
MMCSD1_EMMCSDSS_RXMEM_CORR_ERR_LVL_0
MMCSD1_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_0
MMCSD1_EMMCSDSS_TXMEM_CORR_ERR_LVL_0
MMCSD1_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_0
R5FSS0_CORE0
R5FSS0_CORE0_INTR_IN_166
R5FSS0_CORE1
R5FSS0_CORE1_INTR_IN_166
R5FSS1_CORE0
R5FSS1_CORE0_INTR_IN_166
R5FSS1_CORE1
R5FSS1_CORE1_INTR_IN_166
mmcsd-016-am64x

Note

i = 0 to 1

Figure 12-228. MMCSD Integration

Table 12-314 through Table 12-317 summarize the integration of MMCSD0 and MMCSD1 in the device MAIN domain.

Table 12-326. MMCSD Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MMCSD0	PSC0	PD0	LPSC5	CBASS0
MMCSD1	PSC0	PD0	LPSC4	CBASS0

Table 12-327. MMCSD Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MMCSD0	MMCSD0_ICLK	MAIN_SYSCLK0/2	PLLCTRL0	MMCSD0 Interface Clock
	MMCSD0_FCLK	MAIN_PLL0_HSDIV5_CLKOUT (MMCSD0 default selection)	PLL0_HSDIV5	MMCSD0 Functional Clock (for more information about clock multiplexing, see CTRLMMR_EMMC0_CLKSEL[1-0] CLK_SEL bit field in Control Module (CTRL_MMR). Default: CTRLMMR_EMMC0_CLKSEL[1-0] CLK_SEL = 0, MAIN_PLL0_HSDIV5_CLKOUT is selected)
		MAIN_PLL2_HSDIV2_CLKOUT (MMCSD1 default selection)	PLL2_HSDIV2	
MMCSD1	MMCSD1_ICLK	MAIN_SYSCLK0/2	PLLCTRL0	MMCSD1 Interface Clock
	MMCSD1_FCLK	MAIN_PLL0_HSDIV5_CLKOUT (MMCSD0 default selection)	PLL0_HSDIV5	MMCSD1 Functional Clock (for more information about clock multiplexing, see CTRLMMR_EMMC1_CLKSEL[1-0] CLK_SEL bit field in Control Module (CTRL_MMR). Default: CTRLMMR_EMMC1_CLKSEL[1-0] CLK_SEL = 0, MAIN_PLL0_HSDIV5_CLKOUT is selected)
		MAIN_PLL2_HSDIV2_CLKOUT (MMCSD1 default selection)	PLL2_HSDIV2	

Table 12-328. MMCSD Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MMCSD0	MMCSD0_RST	MOD_G_RST	LPSC5	MMCSD0 Asynchronous Reset
MMCSD1	MMCSD1_RST	MOD_G_RST	LPSC4	MMCSD1 Asynchronous Reset

Table 12-329. MMCSD Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MMCSD0	MMCSD0_EMMCSS_INTR_0	GICSS0_SPI_IN_165	GICSS0	MMCSD0 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_165	R5FSS0_CORE0		

Table 12-329. MMCSD Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		R5FSS0_CORE1_INTR_IN_165	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_165	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_165	R5FSS1_CORE1		
	MMCSD0_EMMCSS_RXMEM_CORR_ERR_LVL_0	ESM0_LVL_IN_54	ESM0	MMCSD0 Receive ECC Correctable Error Interrupt Request	Level
	MMCSD0_EMMCSS_RXMEM_UNCORR_ERR_LVL_0	ESM0_LVL_IN_55	ESM0	MMCSD0 Receive ECC Uncorrectable Error Interrupt Request	Level
	MMCSD0_EMMCSS_TXMEM_CORR_ERR_LVL_0	ESM0_LVL_IN_56	ESM0	MMCSD0 Transmit ECC Correctable Error Interrupt Request	Level
	MMCSD0_EMMCSS_TXMEM_UNCORR_ERR_LVL_0	ESM0_LVL_IN_57	ESM0	MMCSD0 Transmit ECC Uncorrectable Error Interrupt Request	Level
MMCSD1	MMCSD1_EMMCSDSS_INTR_0	GICSS0_SPI_IN_166	GICSS0	MMCSD1 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_166	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_166	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_166	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_166	R5FSS1_CORE1		
	MMCSD1_EMMCSDSS_RXMEM_CORR_ERR_LVL_0	ESM0_LVL_IN_58	ESM0	MMCSD1 Receive ECC Correctable Error Interrupt Request	Level
	MMCSD1_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_0	ESM0_LVL_IN_59	ESM0	MMCSD1 Receive ECC Uncorrectable Error Interrupt Request	Level
	MMCSD1_EMMCSDSS_TXMEM_CORR_ERR_LVL_0	ESM0_LVL_IN_60	ESM0	MMCSD1 Transmit ECC Correctable Error Interrupt Request	Level

Table 12-329. MMCSD Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
	MMCSD1_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_0	ESM0_LVL_IN_61	ESM0	MMCSD1 Transmit ECC Uncorrectable Error Interrupt Request	Level

12.3.5.4 MMCSD Functional Description

12.3.5.4.1 Block Diagram

Figure 12-229 shows the MMCSDi module block diagram (where i = 0 to 1).

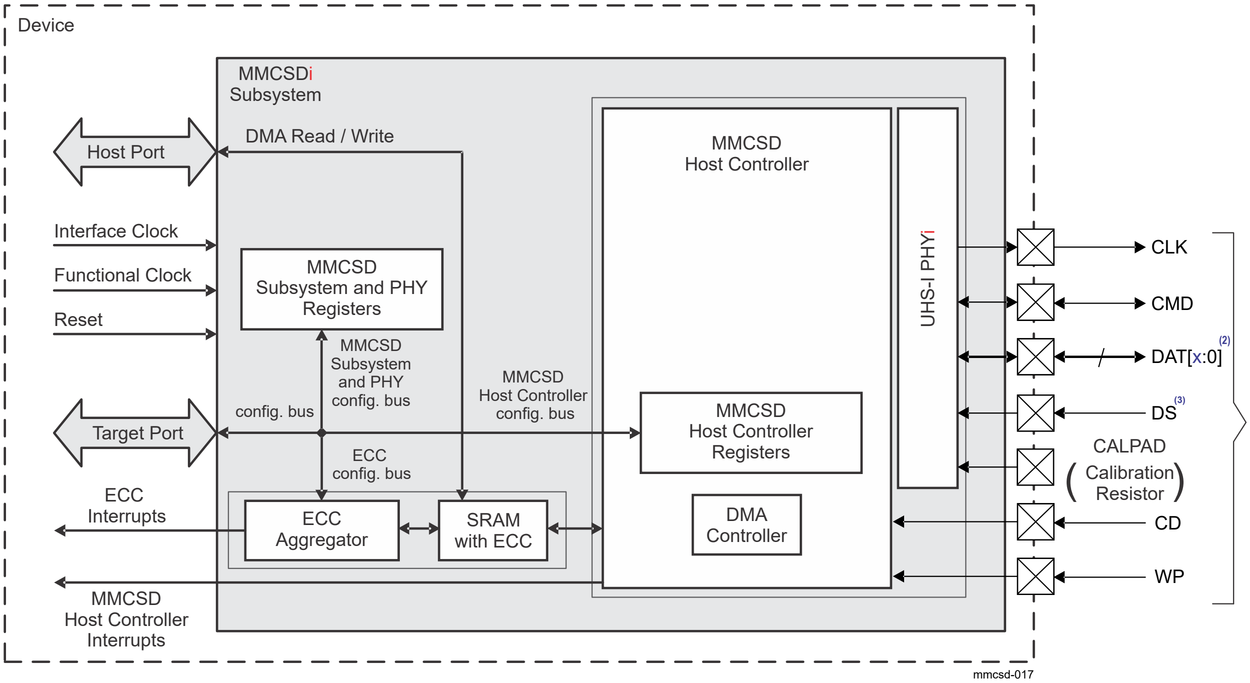

Figure 12-229. MMCSDi Module Block Diagram

Basic Blocks:

- MMCSD Host Controller: The MMCSD Host Controller is situated in the MMCSD Subsystem and provides accessibility to external MMC/SD/SDIO devices using a Programmed IO method or DMA data transfer method.
- UHS-I PHY: The integrated UHS-I PHY provides an interface between the MMCSD Host Controller and external MMC/SD/SDIO devices.
- MMCSDi Interface: The MMCSDi Interface includes all used interface pins (for more information, see *MMCSDi I/O Signals*).
- Host Port: Provides a 64-bit wide read/write interface between the device and the MMCSD Subsystem internal SRAM.
- Target Port: Provides a 32-bit wide interface between the device and the MMCSD Subsystem and MMCSD Host Controller parts.
- MMCSD Host Controller Registers: This block includes set of all MMCSD Host Controller registers.
- MMCSD Subsystem and PHY Registers: This block implements memory-mapped registers at the MMCSD Subsystem level and memory-mapped registers to control and program the MMCSD PHY.
- ECC Aggregator: The ECC Aggregator block facilitates aggregating and reporting internal SRAM ECC errors (for more information, see Section 12.3.5.4.4 , *ECC Support*).
- Internal SRAM with ECC: The internal SRAM block is used for data storage during read/write transactions.
- DMA Controller: Manages the data transfer between the device memory and the MMCSD Subsystem internal SRAM.
- System Clocks: There are asynchronous relationship between the interface (system) clock and functional clock (for more information, see *MMCSD Clocks*).
- System Reset: The reset to the MMCSD Subsystem provides reset to the all MMCSD Subsystem parts (for more information, see *MMCSD Clocks*).
- Interrupts: The MMCSD Subsystem sources one MMCSD Host Controller interrupt and four ECC Aggregator interrupts (for more information, see *MMCSD Hardware Requests* and *Interrupt Requests*).

For more information about all MMCSD registers, see *MMCSD Registers*.

The MMCSD Host Controller can use a Programmed IO method (PIO) or DMA data transfer method to access external MMC/SD/SDIO devices.

The target port is used for device CPU access to the MMCSD Host Controller register set. The MMCSD Host Controller register set provides the communication between the device CPU and the MMCSD Host Controller. In PIO method the device CPU transfers data using the MMCSD0_DATA_PORT / MMCSD1_DATA_PORT register. The data flow from the device memory to the external MMC/SD/SDIO device (and vice versa) is through the target port, the MMCSD0_DATA_PORT / MMCSD1_DATA_PORT register in the MMCSD Host Controller, and the PHY.

The host port is used for connection to the DMA controller (for more information about ADMA support, see Section 12.3.5.4.5 , *Advanced DMA* and MMCSD0_CAPABILITIES / MMCSD1_CAPABILITIES register). In DMA data transfer method the DMA controller uses the host port to transfer data between the device memory and the MMCSD Subsystem internal SRAM. The other side of the internal SRAM is connected to the MMCSD Host Controller. The data flow from the device memory to the external MMC/SD/SDIO device (and vice versa) is through the host port, internal SRAM, MMCSD Host Controller, and the PHY. The DMA controller manages the read/write operations from/to the internal SRAM without device CPU intervention.

12.3.5.4.2 Memory Regions

Table 12-318 shows MMCSDi module memory map.

Table 12-330. MMCSDi Module Memory Map

Address Range		Size	Description
MMCSD0	MMCSD1		
0x0FA10000 - 0x0FA10FFF	0x0FA00000 - 0x0FA00FFF	4 KB	MMCSD Host Controller registers region
0x0FA18000 - 0x0FA183FF	0x0FA08000 - 0x0FA083FF	1 KB	MMCSD Subsystem registers region
0x00706000 - 0x007063FF	0x00708000 - 0x007083FF	1 KB	ECC Aggregator Receive RAM registers region
0x00707000 - 0x007073FF	0x00709000 - 0x007093FF	1 KB	ECC Aggregator Transmit RAM registers region

12.3.5.4.3 Interrupt Requests

Each MMCSD instance sources one active high level MMCSD Host Controller interrupt and four active high level ECC Aggregator interrupts (see *MMCSD Hardware Requests*). The MMCSD Host Controller interrupt is generated based on the bit values in the MMCSD0_NORMAL_INTR_STS / MMCSD1_NORMAL_INTR_STS and MMCSD0_NORMAL_INTR_STS_ENA / MMCSD1_NORMAL_INTR_STS_ENA registers. The ECC Aggregator interrupts are generated based on the ECC errors - single and double bit errors (for more information about ECC Aggregator interrupts, see Section 12.3.5.4.4 , *ECC Support*).

12.3.5.4.4 ECC Support

The Error Correcting Code (ECC) is a mechanism for providing increased system reliability via reduction of memory software errors by allowing single bit errors to be detected and corrected (SEC) and double bit errors to be detected (DED).

There are two SRAM memories (transmit SRAM and receive SRAM) within each MMCSD instance. These two memories are ECC protected.

The SEC logic detects and corrects a single bit error (single bit error per ECC word or per ECC data segment). The DED logic only detects (does not correct) double errors (double bit errors per ECC word or per ECC data segment).

12.3.5.4.4.1 ECC Aggregator

There are two SRAMs (each with size 4 KB - 512 words × 64-bit) in each MMCSD Subsystem. One SRAM dedicated for transmit and one SRAM dedicated for receive operations.

Figure 12-230 shows the ECC Aggregator block diagram.

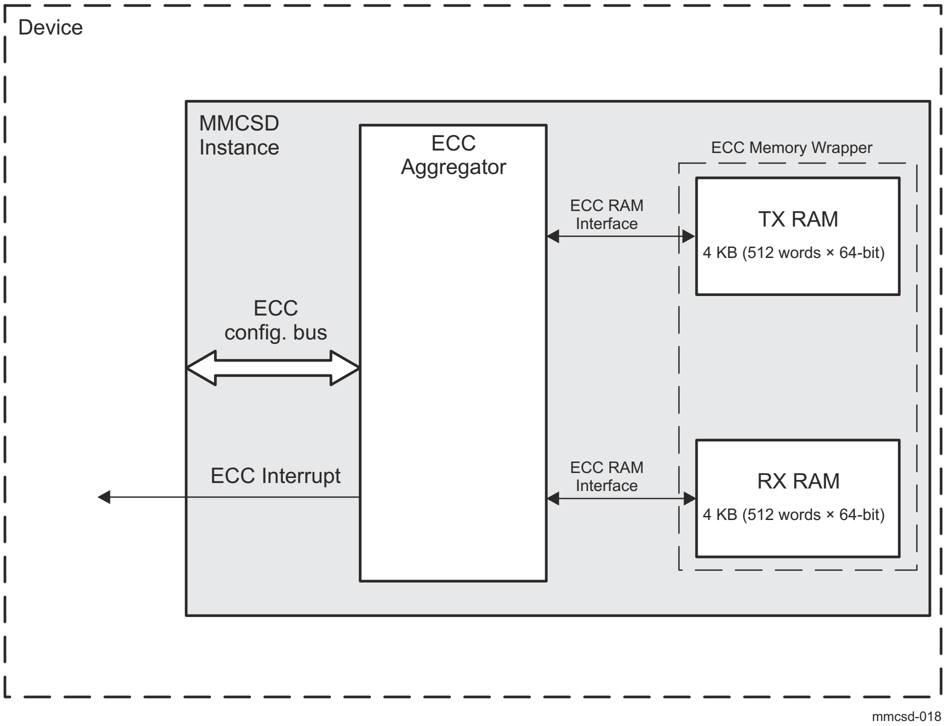

Figure 12-230. ECC Aggregator Block Diagram

Note

For more information about ECC Aggregator Registers, refer to *MMCSD Registers*.

12.3.5.4.5 Advanced DMA

The MMCSD modules support SD Advanced DMA – ADMA2 and ADMA3.

Note

For more information, refer to the SD Association specification titled *"SD Host Controller Simplified Specification, Part A2, Version 4.10"*.

12.3.5.5 MMCSD Programming Guide

12.3.5.5.1 Sequences

This section defines basic sequence flow chart divided into several sub sequences.

Note

This section is applicable for MMCSD0 and MMCSD1 but MMCSD0 registers are used in the content.

Note

UHSII is not supported. For more information, see *Not Supported Features*.

"Wait for interrupts" is used in the flow chart. This means the Host Driver waits until specified interrupts are asserted. If already asserted, then fall through that step in the flow chart. Timeout checking shall be always required to detect no interrupt generated but this is not described in the flow chart.

This specification uses the double box like Figure 12-231, (the step (1) in Figure 12-235), it means that the other flows, which already are shown, shall be performed. Therefore, the interrupt may be included in the other flows.

mmcsd-019

Figure 12-231. Double Box Notation

12.3.5.5.1.1 SD Card Detection

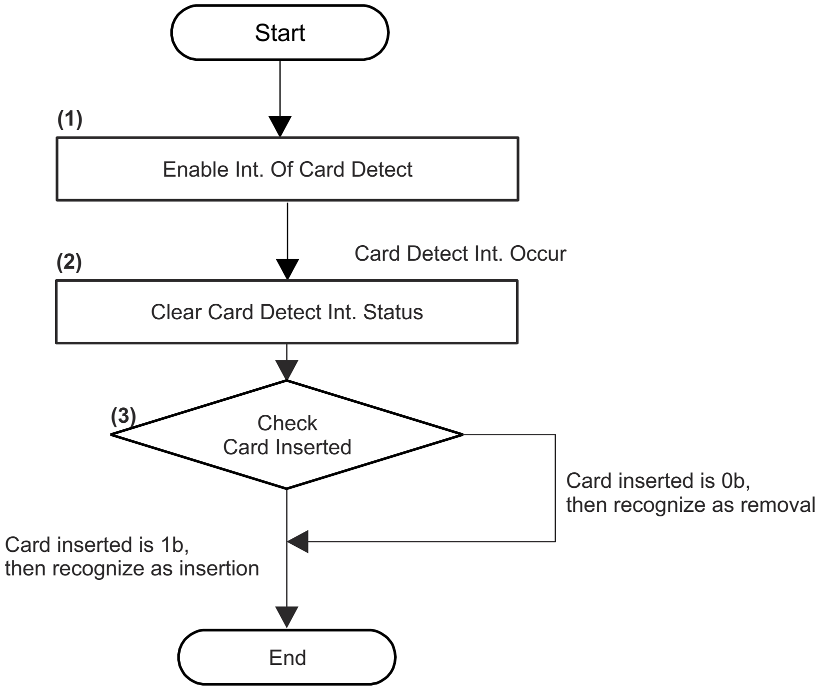

mmcsd-020

Figure 12-232. SD Card Detect Sequence

The flow chart for detecting a SD card is shown in Figure 12-232.

Each step is executed as follows:

To enable interrupt for card detection, write 1 to the following bits:

- MMCSD0_NORMAL_INTR_STS_ENA[6] CARD_INSERTION
- MMCSD0_NORMAL_INTR_SIG_ENA[6] CARD_INSERTION
- MMCSD0_NORMAL_INTR_STS_ENA[7] CARD_REMOVAL
- MMCSD0_NORMAL_INTR_SIG_ENA[7] CARD_REMOVAL

(1) When the Host Driver detects the card insertion or removal, clear its interrupt statuses. If Card Insertion interrupt is generated, write 1 to MMCSD0_NORMAL_INTR_STS_ENA[6] CARD_INSERTION bit. If Card Removal interrupt is generated, write 1 to MMCSD0_NORMAL_INTR_STS_ENA[7] CARD_REMOVAL bit.

(2) Check MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit. In the case where MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit is 1, the Host Driver can supply the power and the clock to the SD card. In the case where MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit is 0, the other executing processes of the Host Driver shall be immediately closed.

If miniSD adaptor is used for standard SD slot and miniSD card is inserted or extracted from the adaptor, card detect interrupt may not be generated. When host does not receive response to any commands, miniSD card is extracted or in idle state, the host should try to re-initialize the card. In this case, all card information shall be re-loaded.

12.3.5.5.1.2 SD Clock Control

12.3.5.5.1.2.1 Internal Clock Setup Sequence

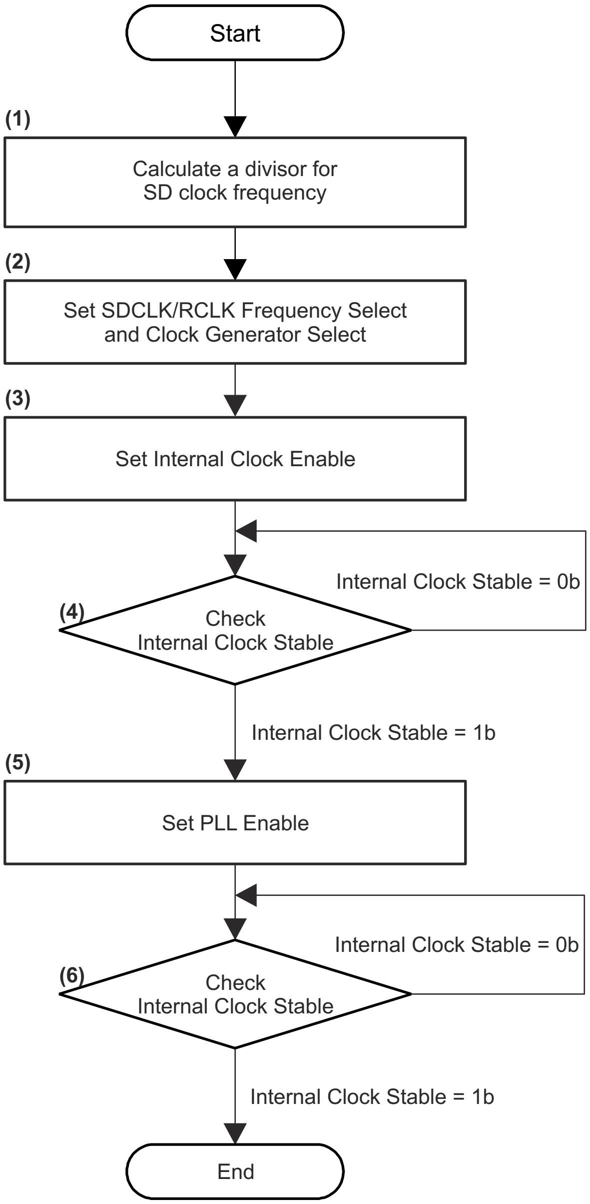

Figure 12-233. Internal Clock Setup Sequence

The sequence for supplying SD Clock to a SD card is described in Figure 12-233. From Version 4.10, MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is added. This sequence is also applicable to prior versions which do not support MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit.

(1) Calculate a divisor to determine SD Clock frequency for legacy IF or RCLK frequency for UHS-II IF by reading MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ and MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit fields. If non-zero value is set to MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field, Programmable Clock Mode can be used (for more information, see MMCSD0_CLOCK_CONTROL[5] CLKGEN_SEL bit). If MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ bit field is 00 0000b, the Host System shall provide this information to the Host Driver by another method.

(2) Set MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field and MMCSD0_CLOCK_CONTROL[5] CLKGEN_SEL bit in accordance with the calculated result of step (1).

If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set, these bits are set by Host Controller automatically as specified in the Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10).

(3) Set MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA bit.

(4) Check MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE bit. Repeat this step until this status is 1. Clock will be stable in shorter time but timeout of this loop is defined as 150 ms.

(5) Set MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit. This step does not affect Host Controllers which do not support MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit.

(6) If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is supported, PLL locked may be checked by this status (if MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this status is supposed to indicate 1 by step (3)). Clock will be stable in shorter time but timeout of this loop is defined as 150 ms.

12.3.5.5.1.2.2 SD Clock Supply and Stop Sequence

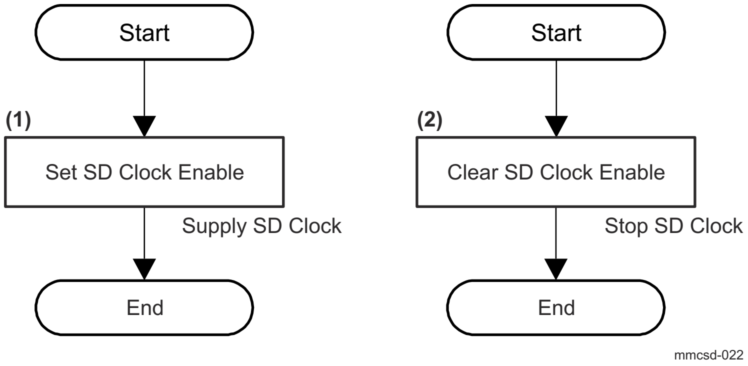

Figure 12-234. SD Clock Supply and Stop Sequence

The flow chart for stopping the SD Clock is shown in Figure 12-234. The Host Driver shall not stop the SD Clock when a SD transaction is occurring on the SD Bus -- namely, when either MMCSD0_PRESENTSTATE[1] INHIBIT_DAT or MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is set to 1.

(1) Setup Internal Clock (see Figure 12-233). Then set MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit to 1. Then, the Host Controller starts supplying the SD Clock.

(2) Set MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit to 0. Then, the Host Controller stops supplying the SD Clock. Internal Clock is still oscillating.

12.3.5.5.1.2.3 SD Clock Frequency Change Sequence

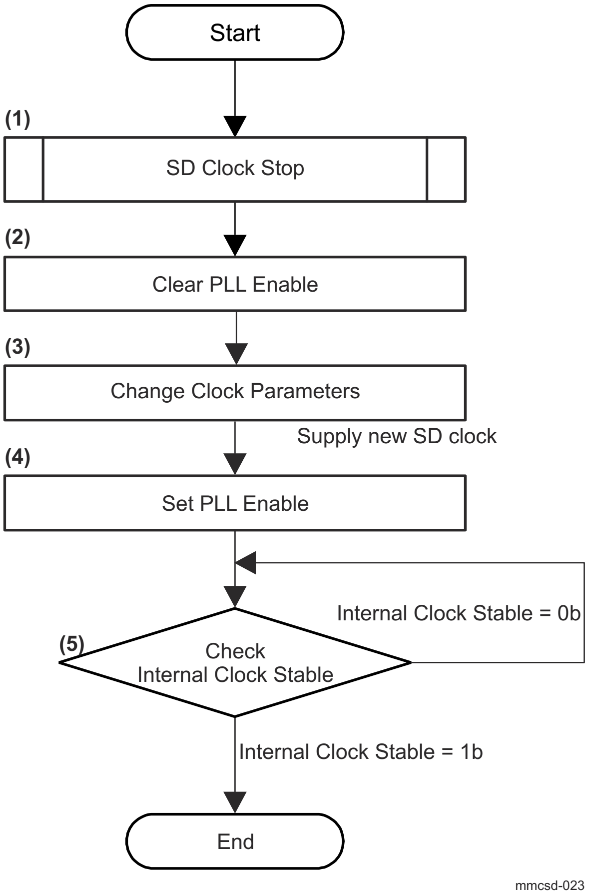

Figure 12-235. SD Clock Change Sequence

The sequence for changing SD Clock frequency is shown in Figure 12-235.

(1) Execute the SD Clock Stop Sequence (see Figure 12-234). If SD Clock supply to card is already stopped, skip this step.

(2) Clear MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit to 0. If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this step has no effect and may be skipped.

(3) When MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 0, change clock parameters in the MMCSD0_CLOCK_CONTROL register. When MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1, select Bus Speed Mode as described.

(4) Set MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit to 1. If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this step this step has no effect and may be skipped.

(5) Wait until MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE bit is set to 1. Clock will be stable in shorter time but timeout of this loop is defined as 150 ms. SD Clock Supply Sequence is required to provide clock to device (see Figure 12-234).

12.3.5.5.1.3 SD Bus Power Control

The sequence for controlling the SD Bus Power is described in Figure 12-236.

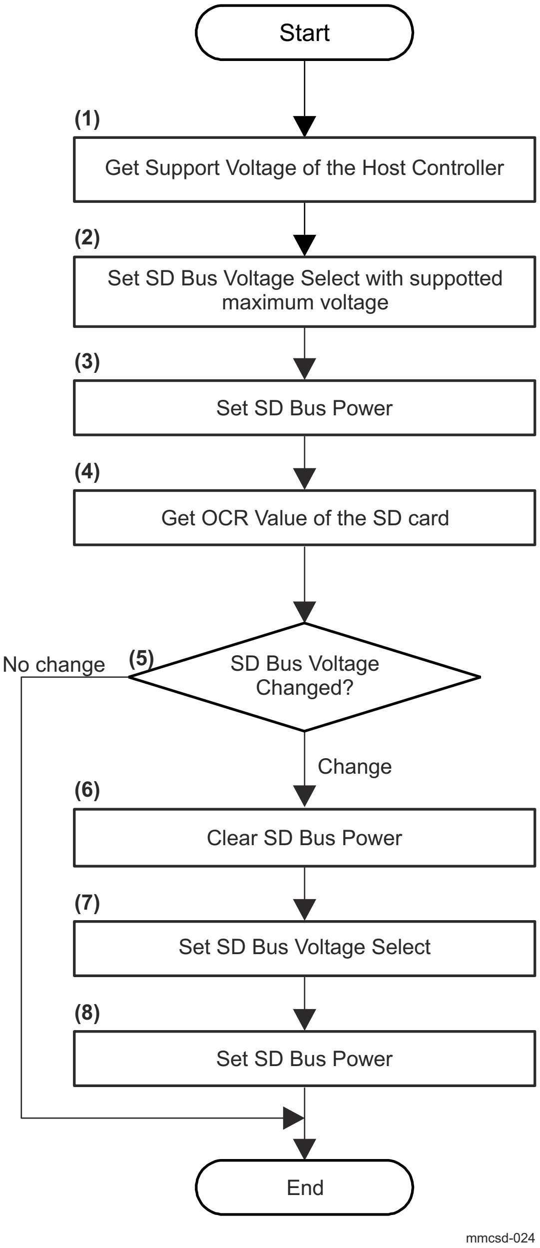

Figure 12-236. SD Bus Power Control Sequence

(1) By reading the MMCSD0_CAPABILITIES register, get the support voltage of the Host Controller.

(2) Set MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field with maximum voltage that the Host Controller supports.

(3) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit to 1.

(4) Get the OCR value of all function internal of SD card.

(5) Judge whether SD Bus voltage needs to be changed or not. In case where SD Bus voltage needs to be changed, go to step (6). In case where SD Bus voltage does not need to be changed, go to "End".

(6) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit to 0 for clearing this bit. The card requires voltage rising from 0 volt to detect it correctly. The Host Driver shall

clear MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit before changing voltage by setting MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field.

(7) Set MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field.

(8) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER to 1.

Note: Step (2) and step (3) can be executed at same time. And also, step (7) and step (8) can be executed at same time.

12.3.5.5.1.4 Changing Bus Width

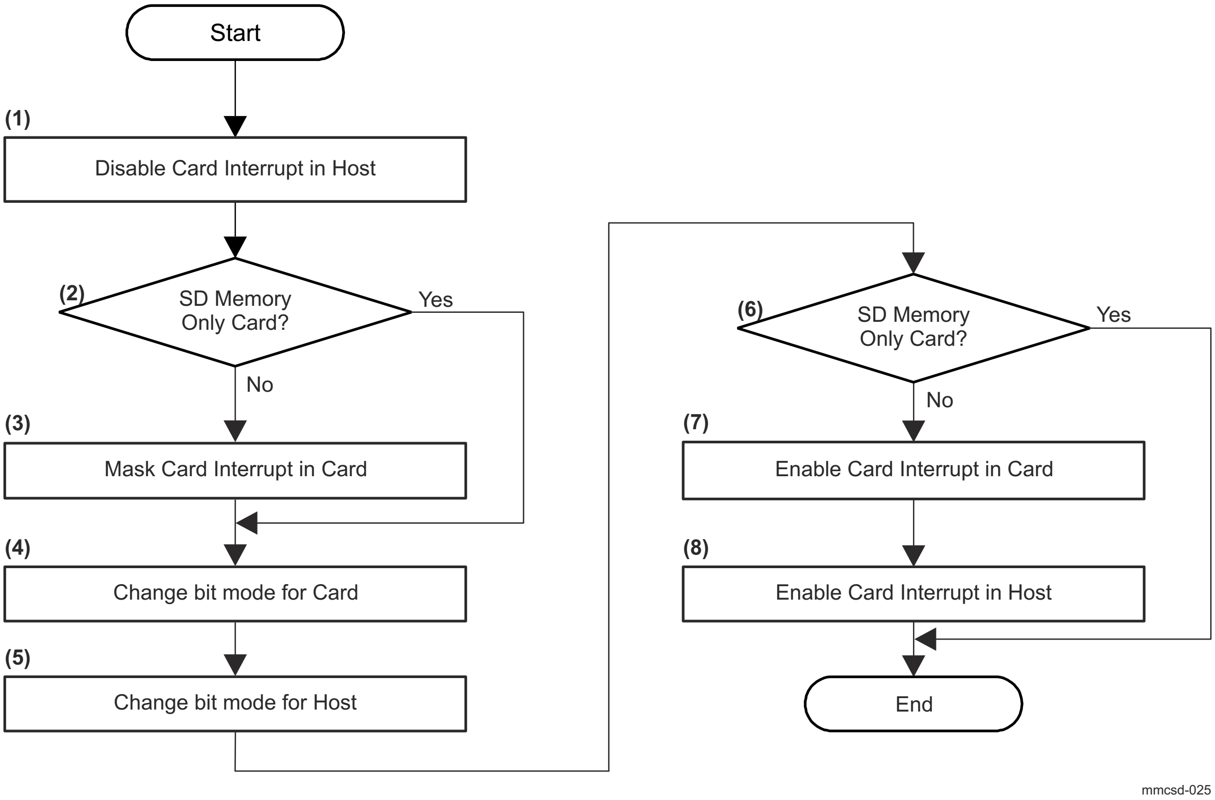

Figure 12-237. Change Bus Width Sequence

The sequence for changing bit mode on SD Bus is shown in Figure 12-237.

(1) Set MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 0 for masking incorrect interrupts that may occur while changing the bus width.

(2) In case of SD memory only card, go to step (4). In case of other card, go to step (3).

(3) Set "IENM" of the CCCR in a SDIO or SD combo card to 0 by CMD52.

(4) Change the bus width mode for a SD card. SD Memory Card bus width is changed by ACMD6 and SDIO card bus width is changed by setting Bus Width of Bus Interface Control register in CCCR.

(5) In case of changing to 4-bit mode, set MMCSD0_HOST_CONTROL1[1] DATA_WIDTH bit to 1. In another case (1-bit mode), set this bit to 0.

(6) In case of SD memory only card, go to the "End". In case of other card, go to step (7).

(7) Set "IENM" of the CCCR in a SDIO or SD combo card to 1 by CMD52.

(8) Set MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 1.

Note that if the card is locked, bus width cannot be changed. Unlock the card is required before changing bus width.

12.3.5.5.1.5 Timeout Setting on DAT Line

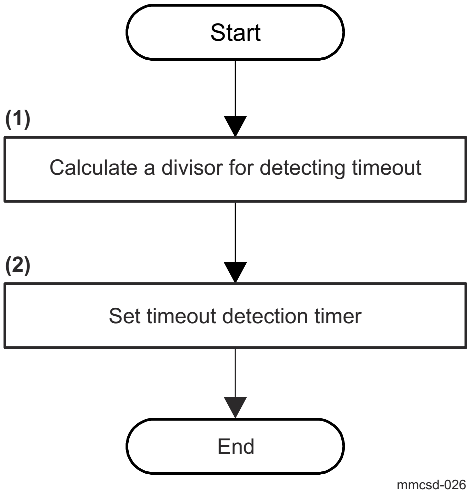

Figure 12-238. Timeout Setting Sequence

In order to detect timeout errors on DAT line, the Host Driver shall execute the following two steps before any SD transaction. For more information regarding SD transactions:

(1) Calculate a divisor to detect timeout errors by reading MMCSD0_CAPABILITIES[5-0] TIMEOUT_CLK_FREQ bit field and MMCSD0_CAPABILITIES[7] TIMEOUT_CLK_UNIT bit. If MMCSD0_CAPABILITIES[5-0] TIMEOUT_CLK_FREQ bit field is 00 0000b, the Host System shall provide this information to the Host Driver by another method.

(2) Set MMCSD0_TIMEOUT_CONTROL[3-0] COUNTER_VALUE bit field in accordance with the value from step (1) above.

12.3.5.5.1.6 Card Initialization and Identification (for SD I/F)

Figure 12-239 and Figure 12-240 shows initialization and card identification sequence for the Standard Capacity SD Memory Card (SDSC), the High Capacity SD Memory Card (SDHC) and the Extended Capacity SD Memory Card (SDXC) that was based on the Physical Layer Version 3.01. Refer to the latest sequence.

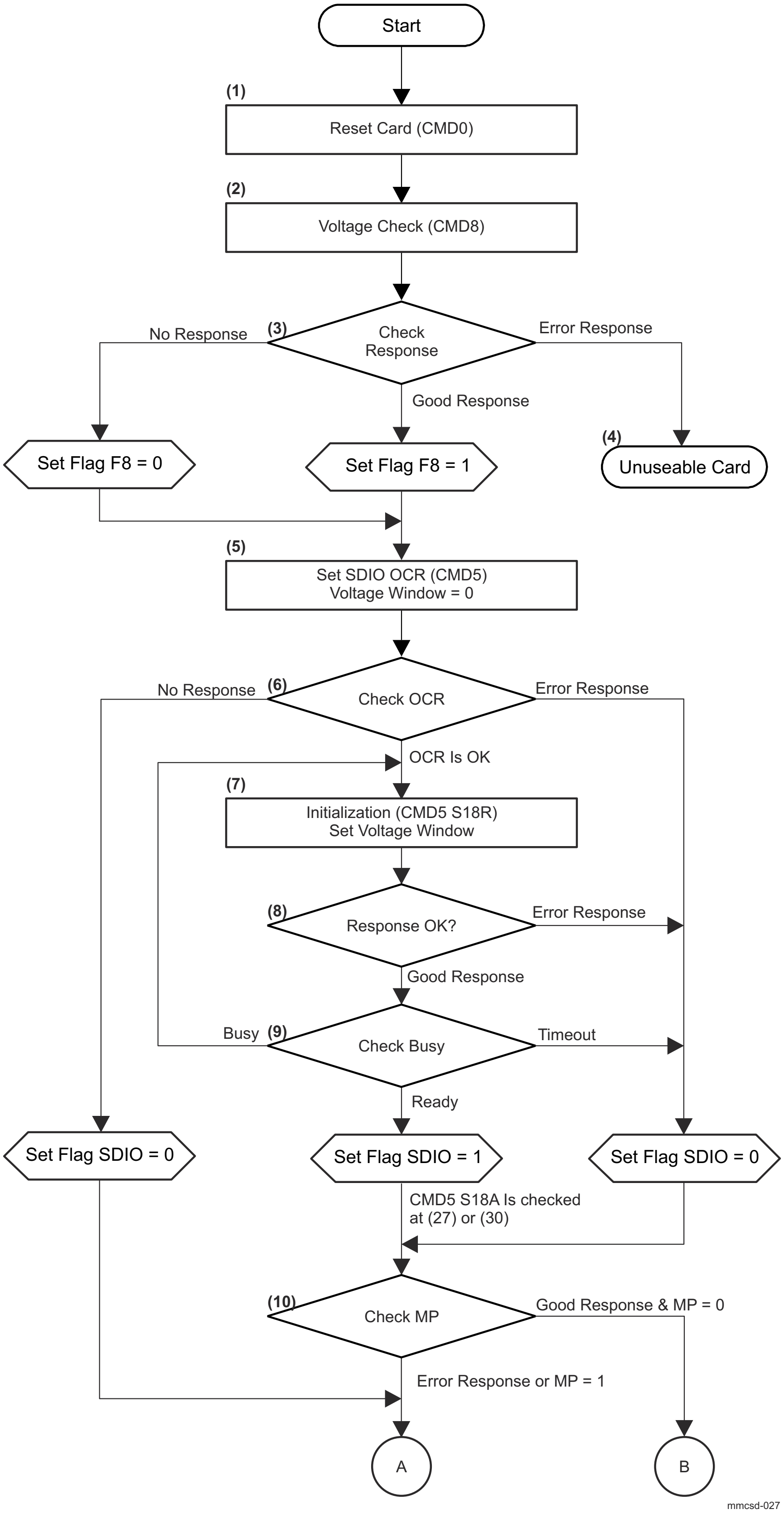

Figure 12-239. Card Initialization and Identification (1)

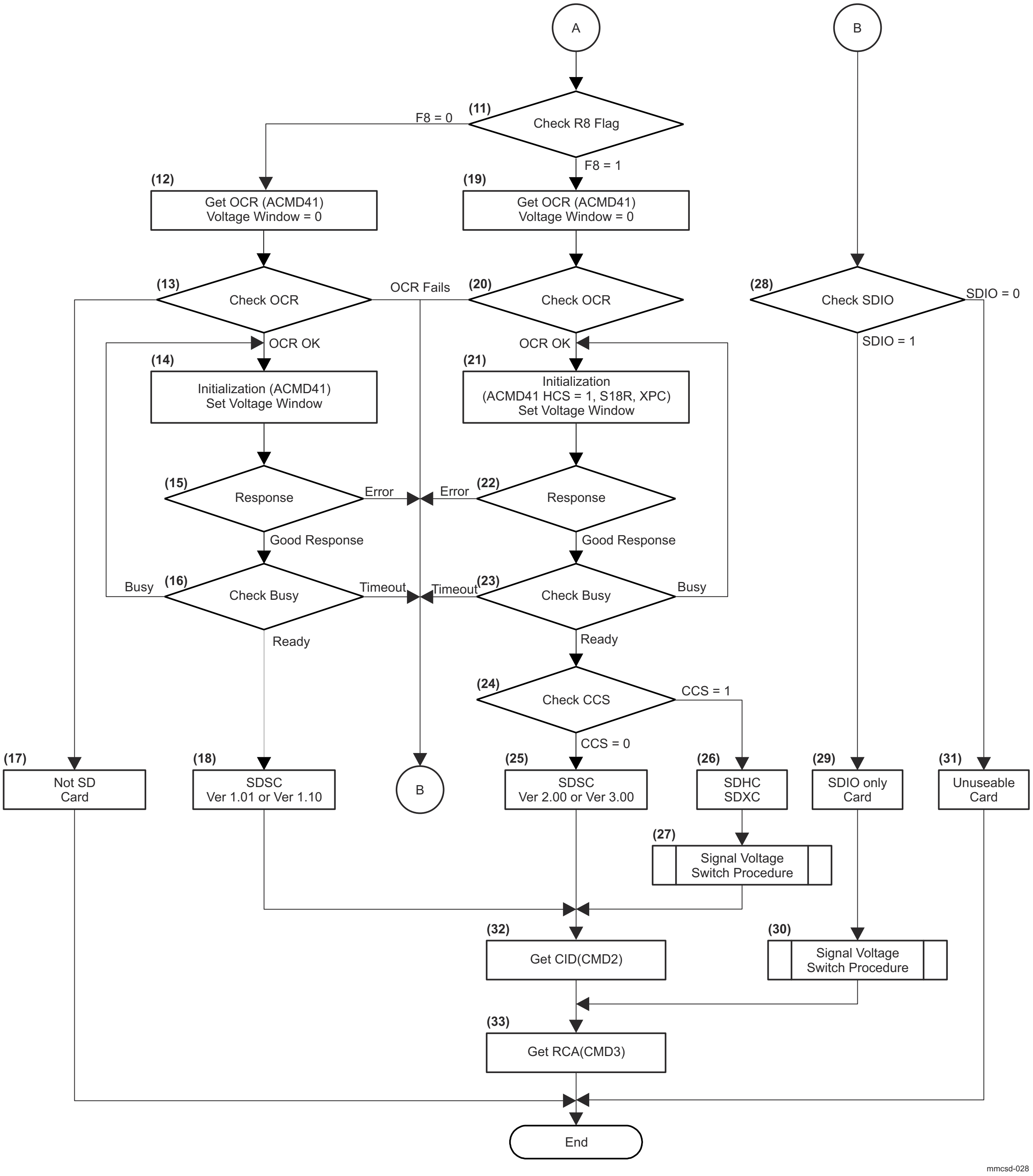

Figure 12-240. Card Initialization and Identification (2)

(1) SD Bus mode is selected by CMD0 (Keep Pin 1 to high during CMD0 execution).

(2) New CMD8 shall be issued after CMD0 to support High Capacity SD Memory Card.

(3) Voltage check command enables the Hosts to support future low voltage specification. However, at this time, only one voltage is defined. Legacy cards and Not SD cards do not respond to CMD8. In this case, set F8 to 0 (F8 is CMD8 valid flag used in step (11)) and go to Step (5). Only Version 2.00 or higher cards can respond to CMD8. The host needs to check whether CRC of the response is valid and whether VHS and check pattern in the argument are equal to VCA and check pattern in the response. Passing all these checks results in CMD8 response OK. In this case, set F8 to 1 and go to step (5). If one of the checks is failed, go to step (4).

(4) Initialization is stopped by CMD8 fails. The Host Driver should retry step (1) to (3) one more time (this is not described in the figure).

(5) SDIO OCR is available by issuing CMD5 with setting voltage window (bit 23 to 0) in the argument to 0. SDIO initialization is not started.

(6) No response means the card does not have SDIO function. Set SDIO flag to 0 and go to step (11). If the card responds to CMD5 and the response is OK, go to step (7). If the response is error, set SDIO flag to 0 and go to step (10). SDIO flag indicates whether SDIO functions are initialized or not.

(7) The SDIO portion starts initialization by CMD5 with setting the supply voltage to the voltage window. UHS-I supported host sets S18R to 1. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(8) If no response or error response is receive, set SDIO flag to 0 and go to step (10). If good response is received, go to step (9).

(9) Check busy status in the response. If busy is released, set SDIO flag to 1 and go to step (10). Repeat from step (7) while busy is indicated. Detecting timeout of 1 second exits the loop. In this case, set SDIO flag to 0 and go to step (10).

(10) Good response in this step means that all responses received at (6) and (8) are valid. When response is good, MP (memory present) flag in the response can be checked. If the response valid and MP = 0, go to step (28). Otherwise, go to step (11).

(11) Check F8 flag set in step (3). If CMD8 is executed correctly (F8 = 1), go to step (19). Otherwise, go to step (12).

(12) OCR is available by issuing ACMD41 with the voltage window (bit 23 to 0) in the argument is set to 0. Memory initialization is not started. The response of CMD55 (ACMD41) may indicate illegal command error due to some SD cards do not recognized CMD8. The Host Driver should ignore this error or issue CMD0 before ACMD41 to clear this error status.

(13) If response of CMD55 is not received, the card is not SD cards and goes to (17). If the card responds to CMD55, it may also respond to CMD41. If the responses of ACMD41 are OK, go to Step (14). Otherwise, go to step (28). Locked card can be detected by the card status in the response of CMD55.

(14) The memory portion starts initialization by Issuing ACMD41 with setting the supply voltage to the voltage window. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(15) If no response or error response is received, go to step (28). If good response is received, go to step (16).

(16) Check busy status in the response. If busy is released, go to step (18). Repeat from step (14) while busy is indicated. The interval of ACMD41 shall be less than 50 ms. Detecting timeout of 1 second exits the loop and go to step (28).

(17) The host recognizes that the card is not SD memory card and quits SD card initialization.

(18) The host recognizes that the card is Version 1.xx Standard Capacity SD Memory Card. Go to Step (30).

(19) OCR is available by issuing ACMD41 with setting the voltage window (bit 23 to 0) in the argument is set to 0. Memory initialization is not started. Setting of HCS does not affect this operation.

(20) If the card responds to CMD55, it may also respond to CMD41. If the responses of ACMD41 are OK, go to Step (21). Otherwise, go to step (28). Locked card can be detected by the card status in the response of CMD55.

(21) The memory portion starts initialization by Issuing ACMD41 with setting the supply voltage to the voltage window. UHS-I supported host sets S18R to1. If the host can supply more than 150mA, XPC is set to 1. HCS in the argument is set to 1, which indicates supporting High Capacity Memory Card. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(22) If no response or error response is received, go to step (28). If good response is received, go to step (23).

(23) Check busy status in the response. If busy is released, go to step (24). Repeat from step (21) while busy is indicated. The interval of ACMD41 shall be less than 50 ms. Detecting timeout of 1 second exits the loop and go to step (28).

(24) CCS in the response is valid after busy is released. If CCS = 0, it indicates the Standard Capacity SD Memory Card and go to step (25). If CCS = 1, it indicates the High Capacity SD Memory Card or Extended Capacity Memory Card and go to Step (26).

(25) The host recognizes that the card is Ver2.00 or Ver3.00 Standard Capacity SD Memory Card. Optimal functions defined in Version 2.00 or higher are available. Go to Step (32).

(26) The host recognizes that the card is the High Capacity SD Memory Card or Extended Capacity Memory Card.

(27) Perform the signal voltage switch procedure and go to step (32).

(28) Check SDIO flag. If SDIO = 1, go to step (28). Otherwise, go to step (31).

(29) The host recognizes that the card is SDIO only card and go to step (30).

(30) Perform the signal voltage switch procedure and go to step (33).

(31) The host recognizes that the card is unusable.

(32) In case of memory card, CMD2 is issued to get CID and Go to Step (31).

(33) CMD3 is issued to get RCA. If the RCA number is 0, the Host should issue CMD3 again.

12.3.5.5.1.6.1 Signal Voltage Switch Procedure (for UHS-I)

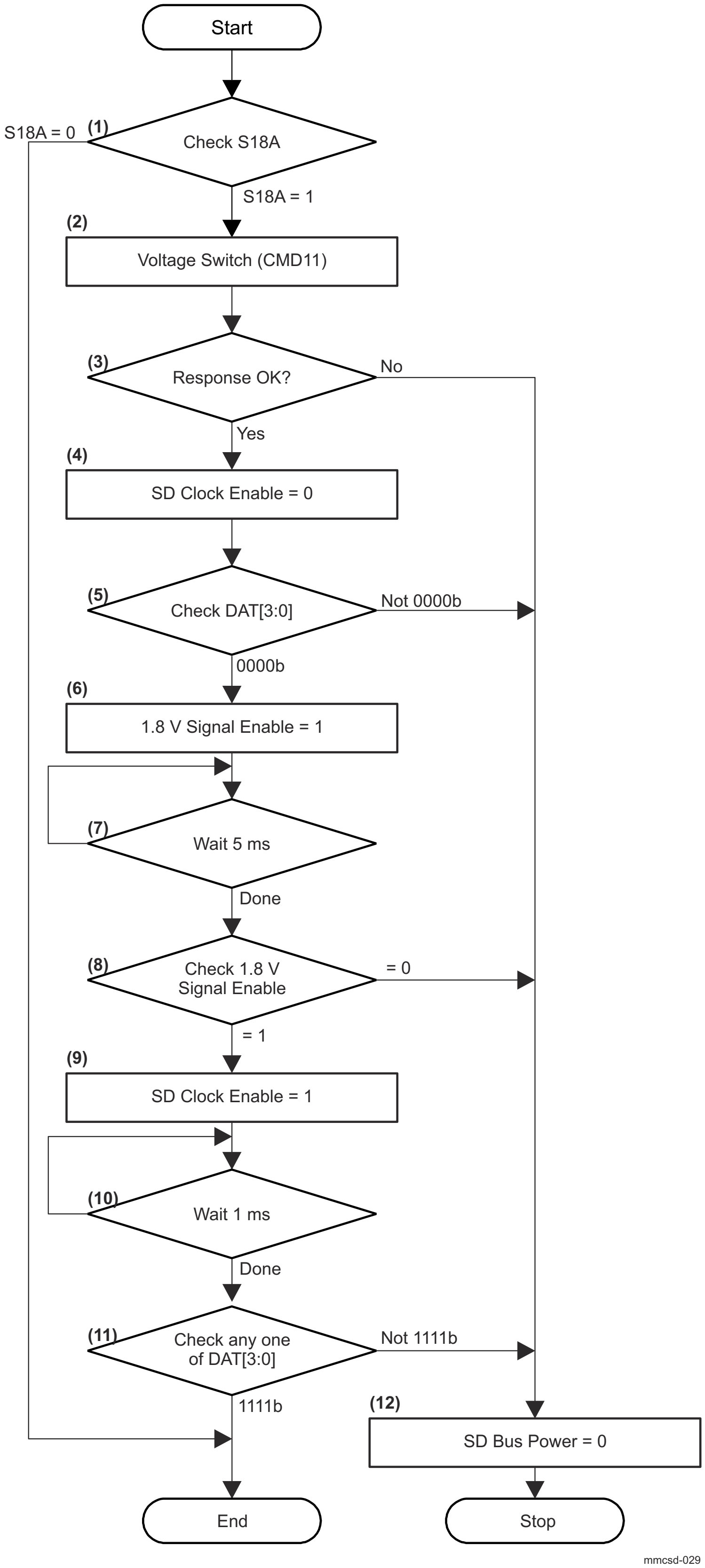

Figure 12-241. Signal Voltage Switch Procedure

(1) If S18A of CMD5 or S18A of ACMD41 is set to 1, signal voltage switch is performed according to the following steps. Otherwise, exits from this procedure.

(2) Issue CMD11.

(3) Check response and if an error is detected, go to step (12).

(4) Stop providing SD clock to the card.

(5) Check DAT[3:0] level. If the level is 0000b, the card is ready to start voltage switch sequence. Otherwise, go to (12) to quit the sequence.

(6) Set MMCSD0_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit.

(7) Wait 5 ms. 1.8 V voltage regulator shall be stable within this period.

(8) If MMCSD0_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit is cleared by Host Controller, go to step (12).

(9) Provide SD Clock to the card again.

(10) Wait 1 ms.

(11) Check DAT[3:0] level. If the level is 1111b, switch to 1.8 V signal level is completed successfully. Otherwise, go to (12).

(12) If an error occurs during voltage switch procedure, stop providing the power to the card. In this case, Host Driver should retry initialization procedure by setting S18R to 0 at step (7) and (21) in Figure 12-239 and Figure 12-240.

12.3.5.5.1.7 SD Transaction Generation

This section describes the sequences how to generate and control various kinds of SD transactions. SD transactions are classified into three cases:

(1) Transactions that do not use the DAT line.

(2) Transactions that use the DAT line only for the busy signal.

(3) Transactions that use the DAT line for transferring data.

In this specification the first and the second case's transactions are classified as "Transaction Control without Data Transfer using DAT Line", the third case's transaction is classified as "Transaction Control with Data Transfer using DAT Line". Refer to the latest SD Physical Layer Specification and SDIO Specification for more detail about SD commands specification.

12.3.5.5.1.7.1 Transaction Control without Data Transfer Using DAT Line

In this section, the sequence for how to issue SD Command and how to complete SD Command is explained. Figure 12-242 shows the sequence to issue a SD Command and Figure 12-243 shows the sequence to finalize a SD Command.

12.3.5.5.1.7.1.1 The Sequence to Issue a SD Command

The sequence to issue the SD Command is detailed in Figure 12-242.

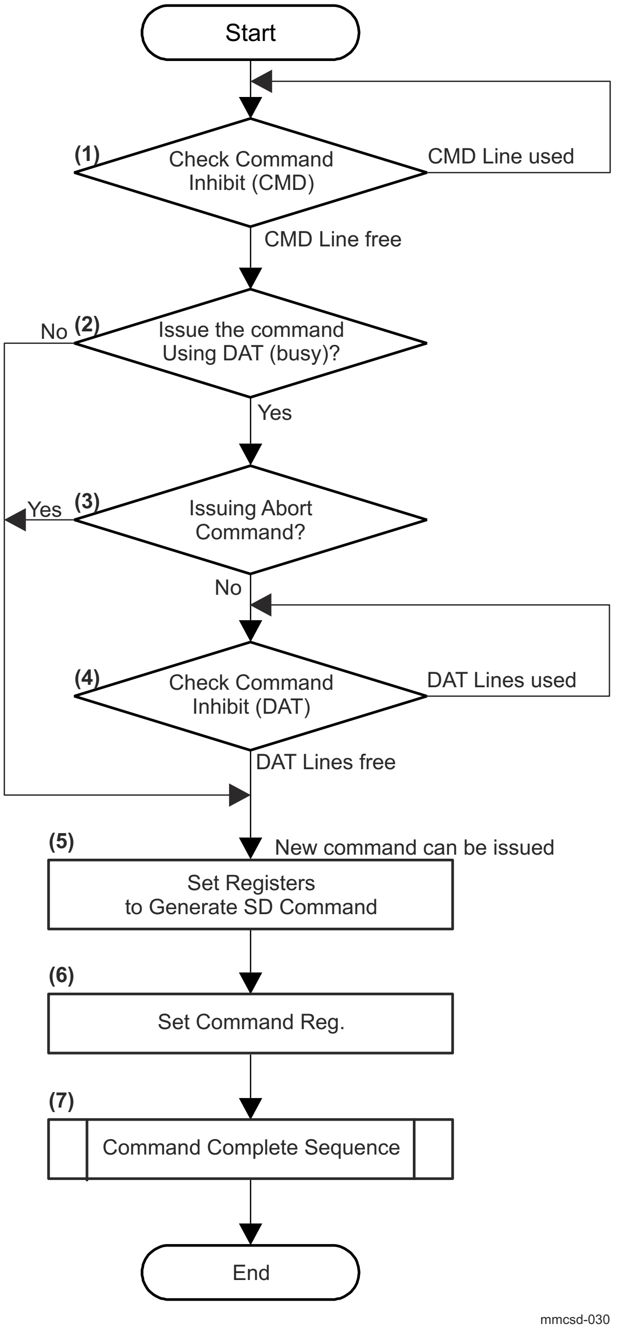

Figure 12-242. SD Command Issue Sequence

(1) Check MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit. Repeat this step until MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is 0. That is, when MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is 1, the Host Driver shall not issue a SD Command.

(2) If the Host Driver issues a SD Command using DAT lines including busy signal, go to step (3). If without using DAT lines including busy signal, go to step (5).

(3) If the Host Driver is issuing an abort command, go to step (5). In the case of nonabort command, go to step (4).

(4) Check MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit. Repeat this step until MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit is set to 0.

(5) Set registers except the MMCSD0_COMMAND register.

(6) Set the MMCSD0_COMMAND register.

Note: Writing the upper byte [3] in the MMCSD0_COMMAND register causes the Host Controller to issue a SD command to the SD card.

(7) Perform Command Completion Sequence in accordance.

12.3.5.5.1.7.1.2 The Sequence to Finalize a Command

Figure 12-243 shows the sequence to finalize a SD Command when response check is disabled. There is a possibility that some errors (Command Index/End bit/CRC/Timeout Error) occur during this sequence. If response check is enabled, error is indicated by Response Error Interrupt.

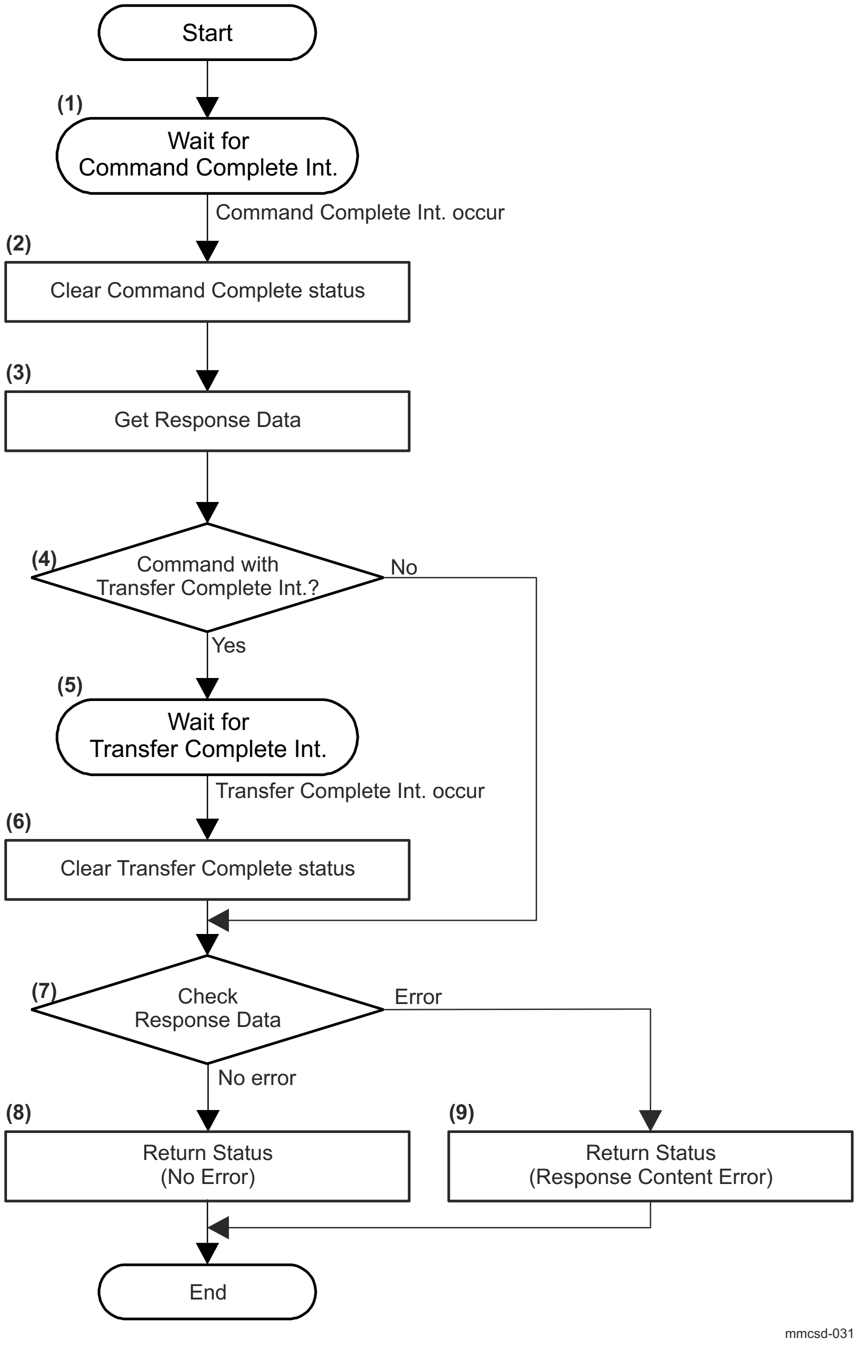

Figure 12-243. Command Complete Sequence

(1) If MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1 (response check is enabled), go to stop (4) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE). If the Command Complete Interrupt has occurred, go to step (2).

(2) Write 1 to MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(3) Read the Response register (see MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(4) Judge whether the command uses the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) or not. If it uses Transfer Complete, go to step (5). If not, go to step (7).

(5) Wait for the Transfer Complete Interrupt. If the Transfer Complete Interrupt has occurred, go to step (6).

(6) Write 1 to MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to clear this bit.

(7) Check for errors in Response Data (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7). If there is no error, go to step (8). If there is an error, go to step (9).

(8) Return Status of "No Error".

(9) Return Status of "Response Contents Error".

Note1: While waiting for the Transfer Complete interrupt, the Host Driver shall only issue commands that do not use the busy signal.

Note2: The Host Driver shall judge the Auto CMD12 complete by monitoring Transfer Complete.

Note3: When the last block of un-protected area is read using memory multiple block read command (CMD18), OUT_OF_RANGE error may occur even if the sequence is correct. The Host Driver should ignore it. This error will appear in the response of Auto CMD12 or in the response of the next memory command.

12.3.5.5.1.7.1.3

(1) If MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1 (response check is enabled), go to stop (4) else wait for the Command Complete Interrupt (MMCSD0_TRANSFER_MODE[0] CMD_COMPLETE). If the Command Complete Interrupt has occurred, go to step (2).

(2) Write 1 to MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(3) Read the Response register (see MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(4) Judge whether the command uses the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) or not. If it uses Transfer Complete, go to step (5). If not, go to step (7).

(5) Wait for the Transfer Complete Interrupt. If the Transfer Complete Interrupt has occurred, go to step (6).

(6) Write 1 to MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to clear this bit.

(7) Check for errors in Response Data (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7). If there is no error, go to step (8). If there is an error, go to step (9).

(8) Return Status of "No Error".

(9) Return Status of "Response Contents Error".

Note1: While waiting for the Transfer Complete interrupt, the Host Driver shall only issue commands that do not use the busy signal.

Note2: The Host Driver shall judge the Auto CMD12 complete by monitoring Transfer Complete.

Note3: When the last block of un-protected area is read using memory multiple block read command (CMD18), OUT_OF_RANGE error may occur even if the sequence is correct. The Host Driver should ignore it. This error will appear in the response of Auto CMD12 or in the response of the next memory command.

12.3.5.5.1.7.2 Transaction Control with Data Transfer Using DAT Line

Depending on whether DMA (optional) is used or not, there are two execution methods.

In addition, the sequences for SD transfers are classified into following three kinds according to how the number of blocks is specified:

(1) Single Block Transfer: The number of blocks is specified to the Host Controller before the transfer. The number of blocks specified is always one.

(2) Multiple Block Transfer: The number of blocks is specified to the Host Controller before the transfer. The number of blocks specified shall be one or more.

(3) Infinite Block Transfer: The number of blocks is not specified to the Host Controller before the transfer. This transfer is continued until an abort transaction is executed. This abort transaction is performed by CMD12 in the case of a SD memory card and by CMD52 in the case of a SDIO card.

12.3.5.5.1.7.2.1 Not using DMA

The sequence for not using DMA is shown in Figure 12-244.

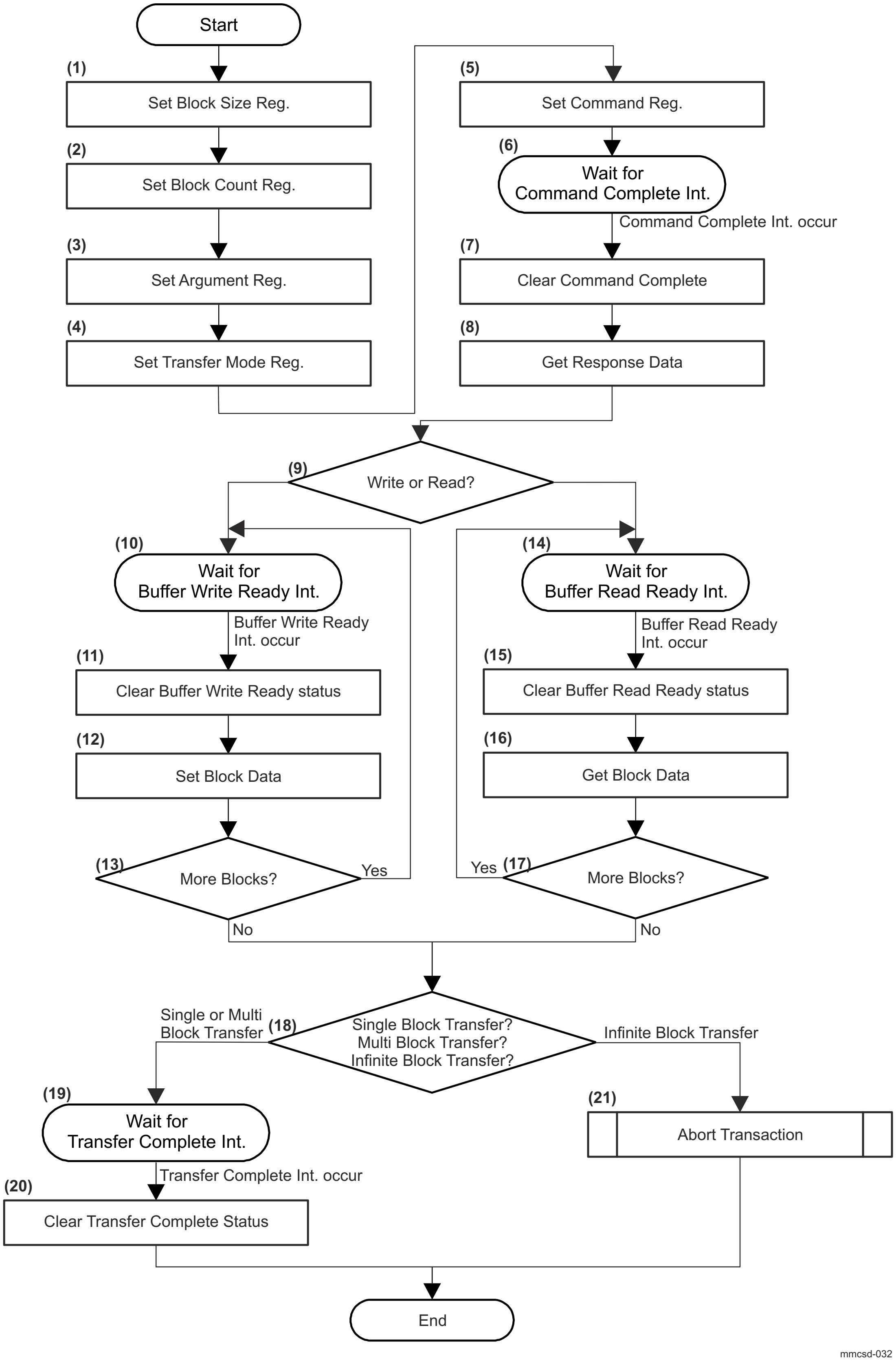

Figure 12-244. Transaction Control with Data Transfer Using DAT Line Sequence (Not using DMA)

(1) Set the value corresponding to the executed data byte length of one block to the MMCSD0_BLOCK_SIZE register.

(2) Set the value corresponding to the executed data block count to the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(3) Set the argument value to Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(4) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*.

If response check is enabled (MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5 (MMCSD0_TRANSFER_MODE[6] RESP_TYPE).

(5) Set the value to MMCSD0_COMMAND register.

Note: When writing the upper byte [3] of MMCSD0_COMMAND register, SD command is issued.

(6) If response check is enabled, go to stop (9) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(7) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit for clearing this bit.

(8) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(9) In the case where this sequence is for write to a card, go to step (10). In case of read from a card, go to step (14).

(10) Then wait for Buffer Write Ready Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[4] BUF_WR_READY).

(11) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[4] BUF_WR_READY bit for clearing this bit.

(12) Write block data (in according to the number of bytes specified at the step (1)) to MMCSD0_DATA_PORT register.

(13) Repeat until all blocks are sent and then go to step (18).

(14) Then wait for the Buffer Read Ready Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[5] BUF_RD_READY).

(15) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[5] BUF_RD_READY bit for clearing this bit.

(16) Read block data (in according to the number of bytes specified at the step (1)) from the MMCSD0_DATA_PORT register.

(17) Repeat until all blocks are received and then go to step (18).

(18) If this sequence is for Single or Multiple Block Transfer, go to step (19). In case of Infinite Block Transfer, go to step (21).

(19) Wait for Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(20) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit for clearing this bit.

(21) Perform the sequence for Abort Transaction in accordance with Section 12.3.5.5.1.8 , *Abort Transaction*.

Note: Step (1) and Step (2) can be executed at same time. Step (4) and Step (5) can be executed at same time.

12.3.5.5.1.7.2.2 Using SDMA

The sequence for using SDMA is shown in Figure 12-245.

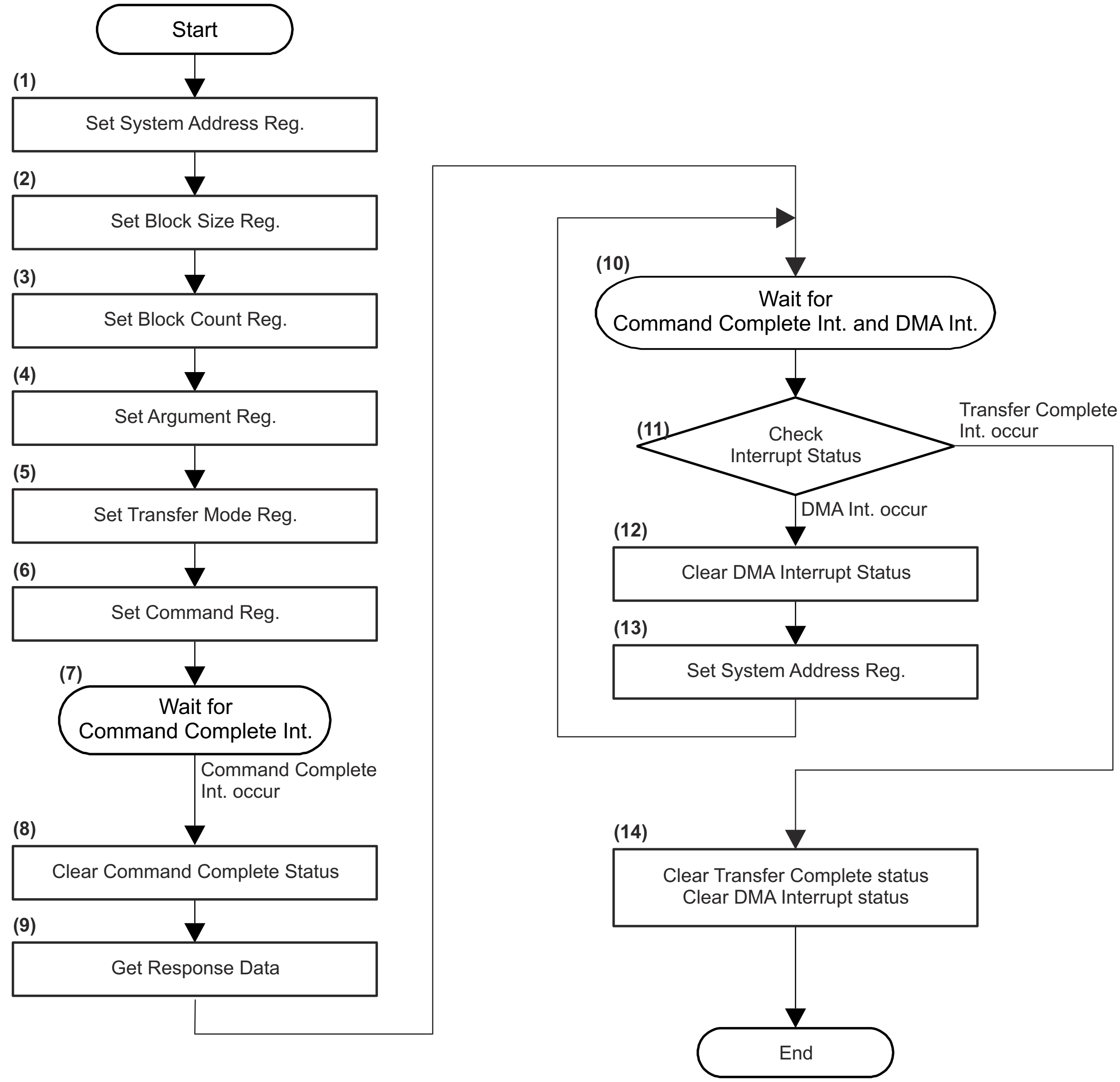

Figure 12-245. Transaction Control with Data Transfer Using DAT Line Sequence (Using SDMA)

(1) Data location of system memory is set to the SDMA System Address register if MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0 or set to the MMCSD0_ADMA_SYS_ADDRESS register if MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1.

(2) Set the value corresponding to the executed data byte length of one block in the MMCSD0_BLOCK_SIZE register.

(3) Set the value corresponding to the executed data block count in the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(4) Set the argument value to the Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(5) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the

MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*. If response check is enabled (MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5.

(6) Set the value to the MMCSD0_COMMAND register.

Note: When writing to the upper byte [3] of the MMCSD0_COMMAND register, the SD command is issued and SDMA is started.

(7) If response check is enabled, go to stop (10) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(8) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(9) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(10) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) and DMA Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT).

(11) If MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is set to 1, go to Step (14) else if MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit is set to 1, go to Step (12). The MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is higher priority than the MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit.

(12) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit to clear this bit.

(13) Set the next system address of the next data position to the System Address register (MMCSD0_ADMA_SYS_ADDRESS) and go to Step (10).

(14) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit and MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit to clear this bit.

Note: Step (2) and Step (3) can be executed simultaneously. Step (5) and Step (6) can also be executed simultaneously.

12.3.5.5.1.7.2.3 Using ADMA

The sequence for using ADMA is shown in Figure 12-246.

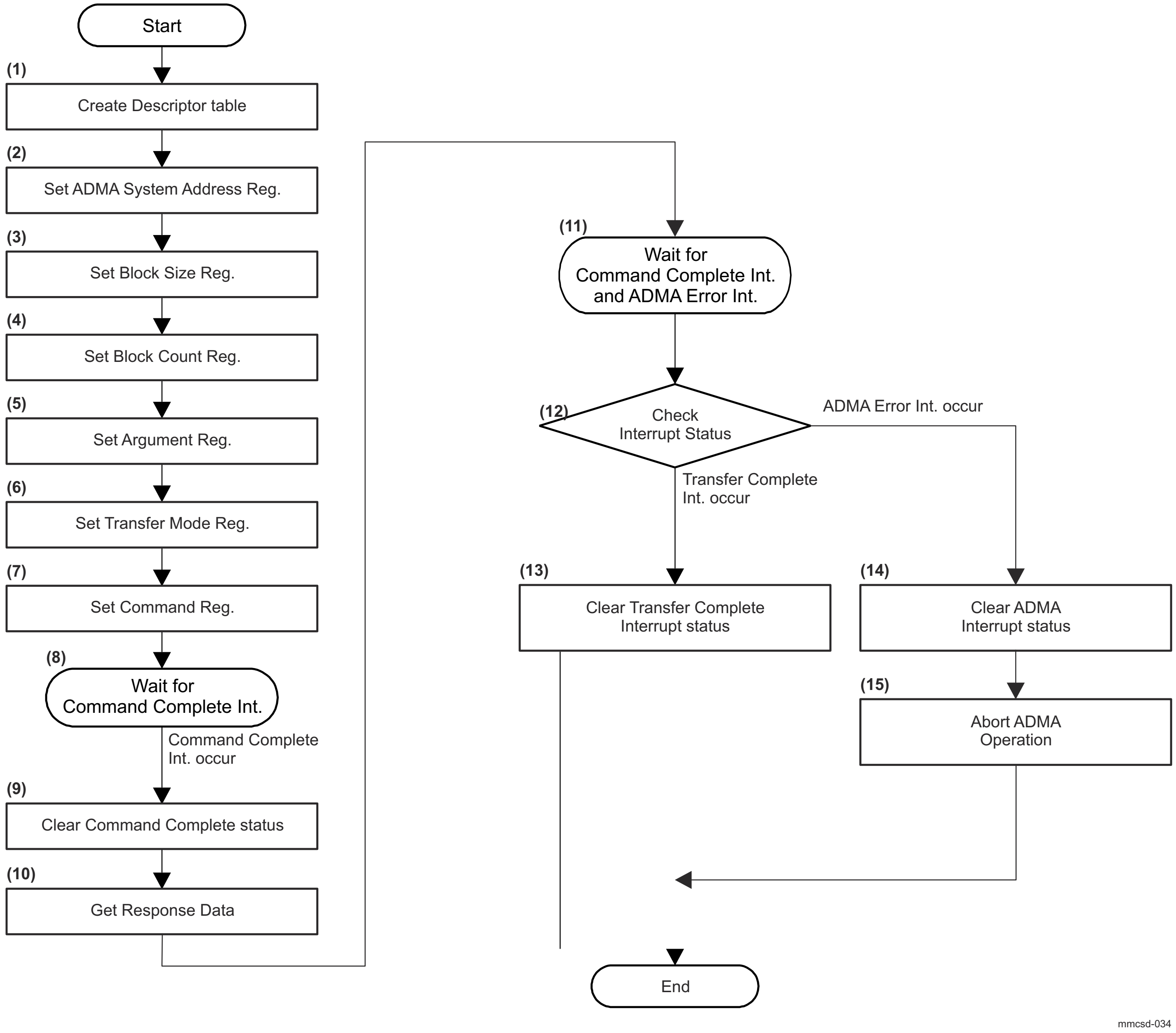

Figure 12-246. Transaction Control with Data Transfer Using DAT Line Sequence (Using ADMA)

(1) Create Descriptor table for ADMA in the system memory.

(2) Set the Descriptor address for ADMA in the MMCSD0_ADMA_SYS_ADDRESS register.

(3) Set the value corresponding to the executed data byte length of one block in the MMCSD0_BLOCK_SIZE register.

(4) Set the value corresponding to the executed data block count in the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(5) Set the argument value to the Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(6) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*. If response check is enabled (MMCSD0_TRANSFER_MODE[7]

RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5 (MMCSD0_TRANSFER_MODE[6] RESP_TYPE).

(7) Set the value to the MMCSD0_COMMAND register.

Note: When writing to the upper byte [3] of the MMCSD0_COMMAND register, the SD command is issued and DMA is started.

(8) If response check is enabled, go to stop (11) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(9) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(10) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(11) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) and ADMA Error Interrupt (MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE).

(12) If MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is set to 1, go to Step (13) else if MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE bit field is set to 1, go to Step (14).

(13) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to clear this bit.

(14) Write 1 to the MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE bit field to clear this bit.

(15) Abort ADMA operation. SD card operation should be stopped by issuing abort command. If necessary, the Host Driver checks MMCSD0_ADMA_ERR_STATUS register to detect why ADMA error is generated.

Note: Step (3) and Step (4) can be executed simultaneously. Step (6) and Step (7) can also be executed simultaneously.

12.3.5.5.1.8 Abort Transaction

An abort transaction is performed by issuing CMD12 for a SD memory card and by issuing CMD52 for a SDIO card. There are two cases where the Host Driver needs to do an Abort Transaction. The first case is when the Host Driver stops Infinite Block Transfers. The second case is when the Host Driver stops transfers while a Multiple Block Transfer is executing.

There are two ways to issue an Abort Command. The first is an asynchronous abort. The second is a synchronous abort. In an asynchronous abort sequence, the Host Driver can issue an Abort Command at any time unless MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is set to 1. In a synchronous abort, the Host Driver shall issue an Abort Command after the data transfer stopped by using MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

12.3.5.5.1.8.1 Asynchronous Abort

The sequence for Asynchronous Abort is shown in Figure 12-247.

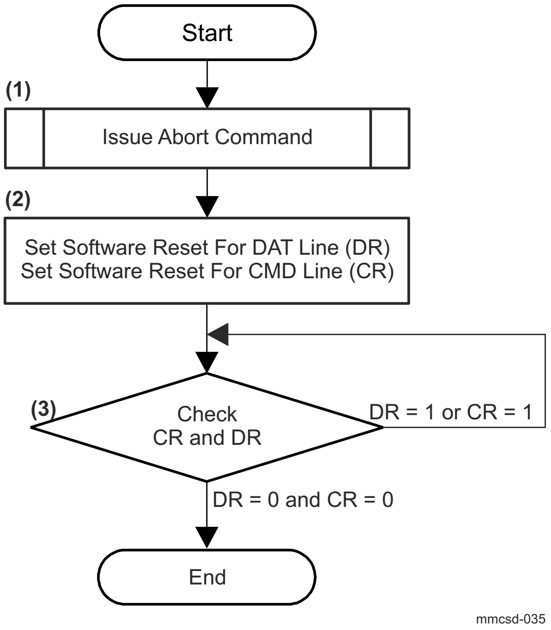

Figure 12-247. Asynchronous Abort Sequence

(1) Issue Abort Command in accordance.

(2) Set both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 to do software reset.

(3) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit are 0, go to "End". If either MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit or MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 1, go to step (3).

12.3.5.5.1.8.2 Synchronous Abort

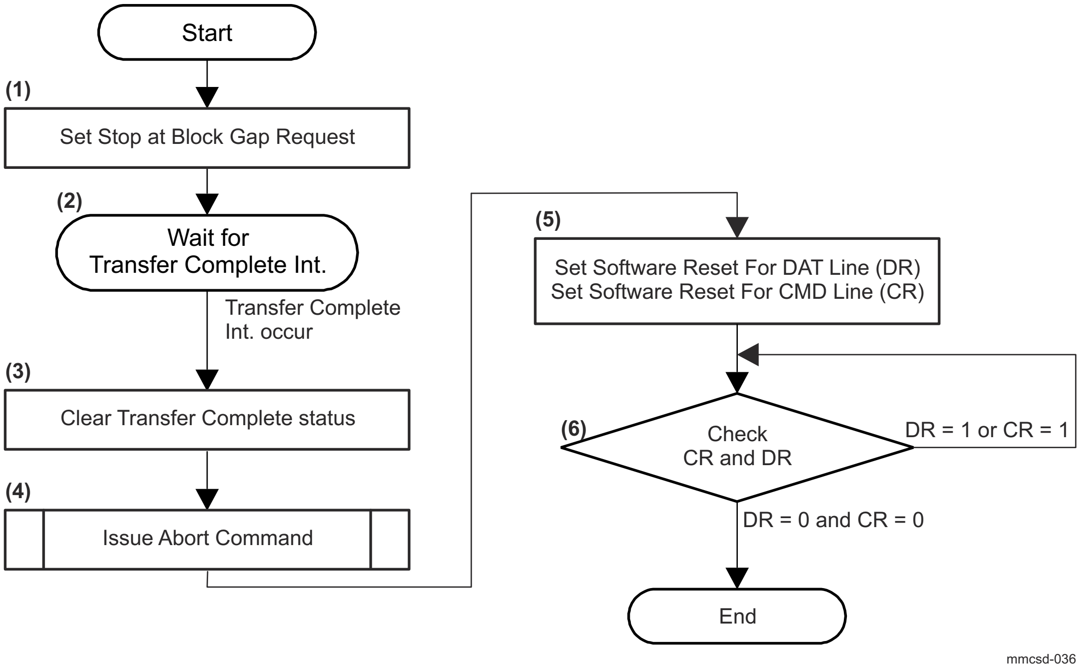

Figure 12-248. Synchronous Abort Sequence

(1) Set the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 1 to stop SD transactions.

(2) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(3) Set the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to 1 to clear this bit.

(4) Issue the Abort Command

(5) Set both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 to do software reset.

(6) Check both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit are 0, go to "End". If either MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit or MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 1, go to step (6).

12.3.5.5.1.9 Changing Bus Speed Mode

This section describes the sequence for switching the bus speed mode: Default Speed, High Speed mode and UHS-I mode. The switch command (CMD6) is used to change memory card bus speed mode. The EHS bit (SDIO Version 2.00) or BSS[2-0] bits (SDIO Version 3.00) in the CCCR register is used to change the bus speed mode for SDIO card. In case of Combo card, either of the switch method changes both memory and IO bus speed mode. This means the first switch is effective. Refer to the Physical Layer Specification Version 3.0x and the SDIO Specification Version 3.00 for more information about switching bus speed. Figure 12-249 shows the sequence for switching bus speed mode for Combo Card. Note that if the card is locked, bus width cannot be changed. Unlock the card is required before changing bus width.

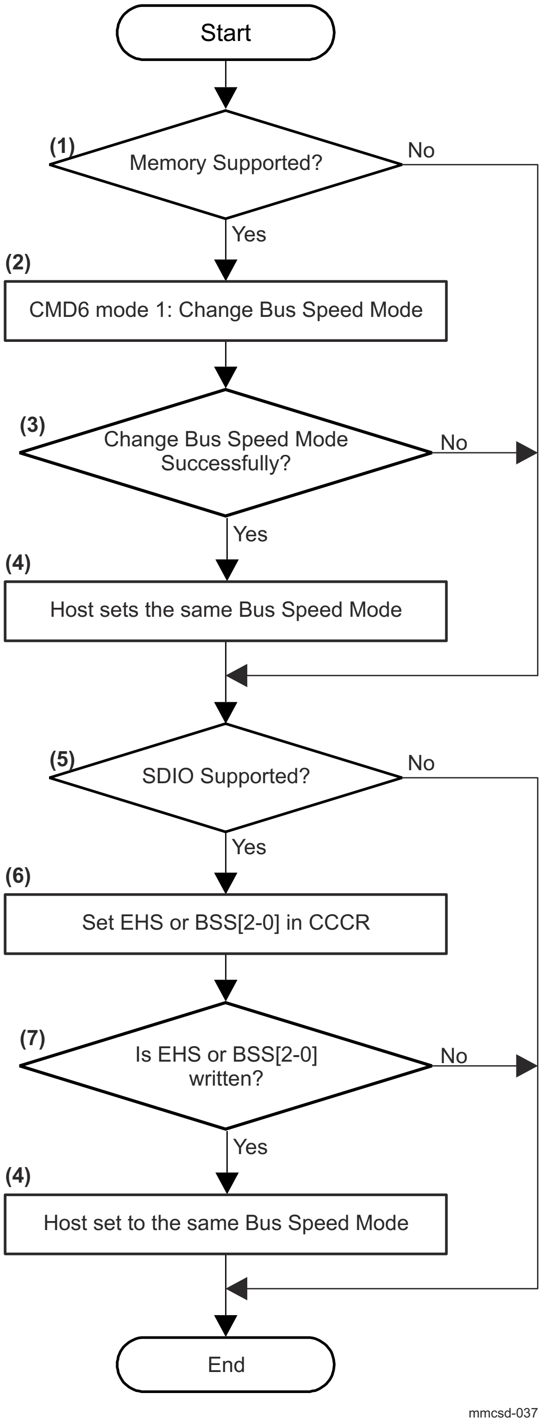

Figure 12-249. Changing Bus Speed Mode

(1) The Host Driver checks if the card supports memory. If not supported, go to (5).

(2) Issue CMD6 with mode 1 to change bus speed mode (Default, High Speed mode or UHS-I mode).

(3) Check the response of CMD6. If the card does not supports CMD6 (no response) or bus speed is not changed successfully, go to step (5). In this case, the card is in Default Speed mode.

(4) The Host Driver changes the Host Controller bus speed mode to the same mode.

(5) The Host Driver checks if the card supports SDIO. If not supported, go to the end.

(6) Issue CMD52 to write EHS bit or BSS[2-0] bits in CCCR to change bus speed mode (the same bus speed mode of (2) shall be set).

(7) If EHS or BSS[2-0] are not changed successfully, go to the end.

(8) The Host Driver changes the Host Controller bus speed to the same mode. In case of Combo card, bus speed is already changed at step (4) and this step does not affect changing bus speed.

12.3.5.5.1.10 Error Recovery

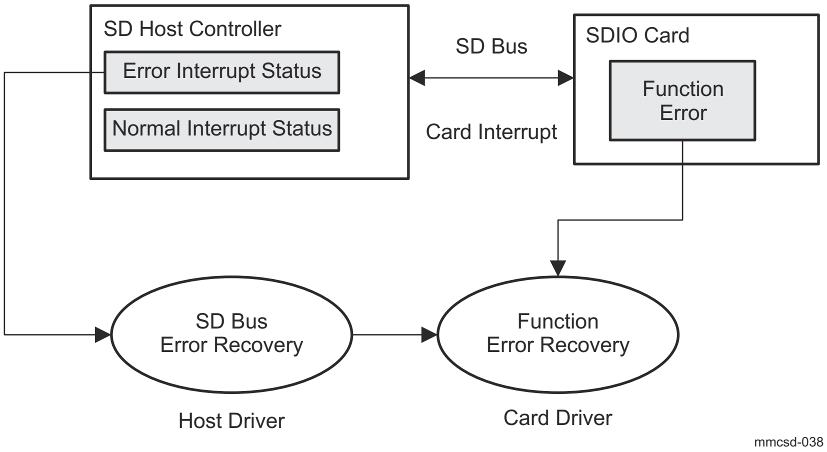

Figure 12-250. Error Report and Recovery

Figure 12-250 shows concept of error report and its recovery. The Host Controller has 2 interrupt status registers. If an error occurs in the SD Bus transaction, one of the bits is set in the MMCSD0_ERROR_INTR_STS register. If the function errors occur in the SDIO card, the card interrupt informs these function errors and the Card interrupt is set in the MMCSD0_NORMAL_INTR_STS_ENA register (the Card Interrupt is used to inform not only error statuses but also normal information. For example, to inform function ready). The Card Driver shall do function error recovery because the Host Driver does not know how to control the function. In the case that function error occurs due to SD Bus error, SD Bus error recovery is required before function error recovery. Abort command is used to recover SD Bus, and then the Host Driver should save error statuses related to SD Bus errors before issuing abort command and transfer these statuses to the Card Driver. These statuses may be used to recover function error. Following explanations are related to SD Bus error recovery. This specification does not specify the function error recovery.

When an error occurs during data transfer in 2L-HD UHS-II mode, there will be the case that Host Controller cannot drive D0 lane in input mode due to DIR LSS for retrieving lane direction is not detected. In this case, Host Driver cannot issue abort command for recovery. Then if DIR LSS is not detected, Host Controller sets MMCSD0_UHS2_ERR_INTR_STS[17] DEADLOCK_TIMEOUT bit. Host Driver should execute power cycle if MMCSD0_UHS2_ERR_INTR_STS[17] DEADLOCK_TIMEOUT bit is detected to recover from this error. Furthermore, if this type of error is detected several times in 2L-HD, Host Driver should use FD mode rather than using 2L-HD.

Implementation Note:

If the Card Driver cannot recover the function errors, the Host Driver should try following methods.

(9) Using IOEx for SDIO card

IOEx may be used as the reset per function basis. Sequence is as follows:

Clear IOEx = 0 and wait until IORx = 0 and then set IOEx = 1 again. SDIO may be recovered when IORx = 1.

(10) Using reset command for memory and SDIO card Re-initialization sequence is required.

(11) Off and on power supply for the SD Bus.

The card may be recovered by the power on reset. Re-initialization sequence is required.

The two cases where the Host Driver needs the "Error Recovery" sequence are classified as follows:

(1) Error Interrupt Recovery:

If error interrupt is indicated by the MMCSD0_ERROR_INTR_STS register, the Host Driver shall apply this sequence.

(2) Auto CMD12 Error Recovery:

If there are errors in Auto CMD12, the Host Driver shall apply this sequence. In terms of Return Status, Auto CMD12 Error Recovery is classified into 4 cases. It is shown in Figure 12-251. If error occurs during memory write transfer, strongly recommend using ACMD22 and then in the following recovery sequence, retry to send remaining blocks not written.

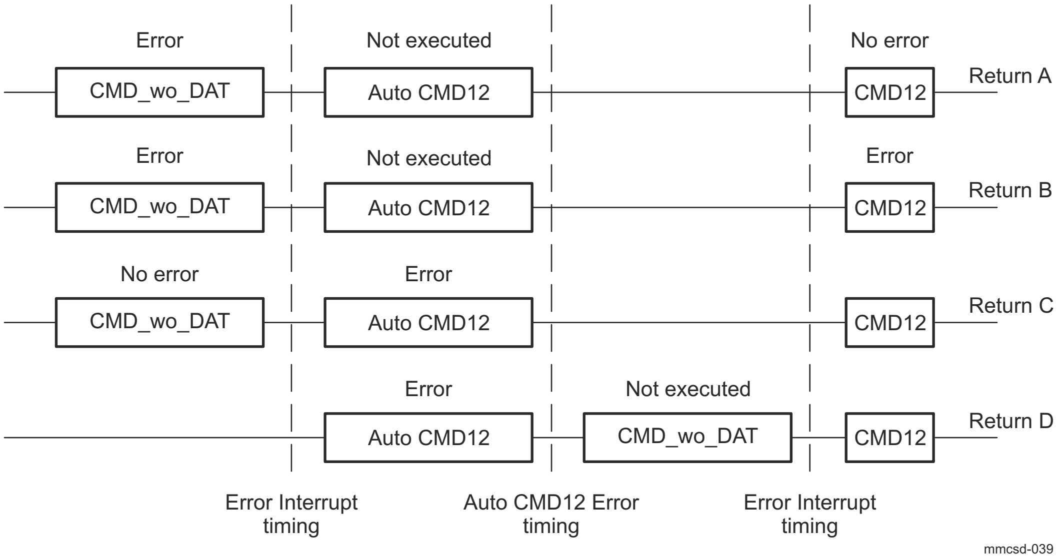

Figure 12-251. Return Status of Auto CMD12 Error Recovery

Implementation Note:

Abort command is used to recover from SD Bus error. SDIO transaction abort using CMD52 returns response but in the case of memory transaction abort using CMD12, response returns depending on the memory card state. If no response returns after issue CMD12, the Host Driver should check card state using CMD13. If the state is "tran" in the CURRENT_STATE, consider CMD12 is successful.

Implementation Note:

The following sequence is one possible error recovery flow. There may be another methods, sometimes using interrupts or polling. It can be possible to use another flows, based on Host System requirements.

In these error recovery sequences, return statuses for the next sequence. When the Host Controller cannot issue the next command due to SD Bus error, the error recovery sequences return "Non-recoverable" status. In this case, the Host System may cut off power to the SD Bus and then power on SD Bus and initialize both the Host Controller and the SD card again.

12.3.5.5.1.10.1 Error Interrupt Recovery

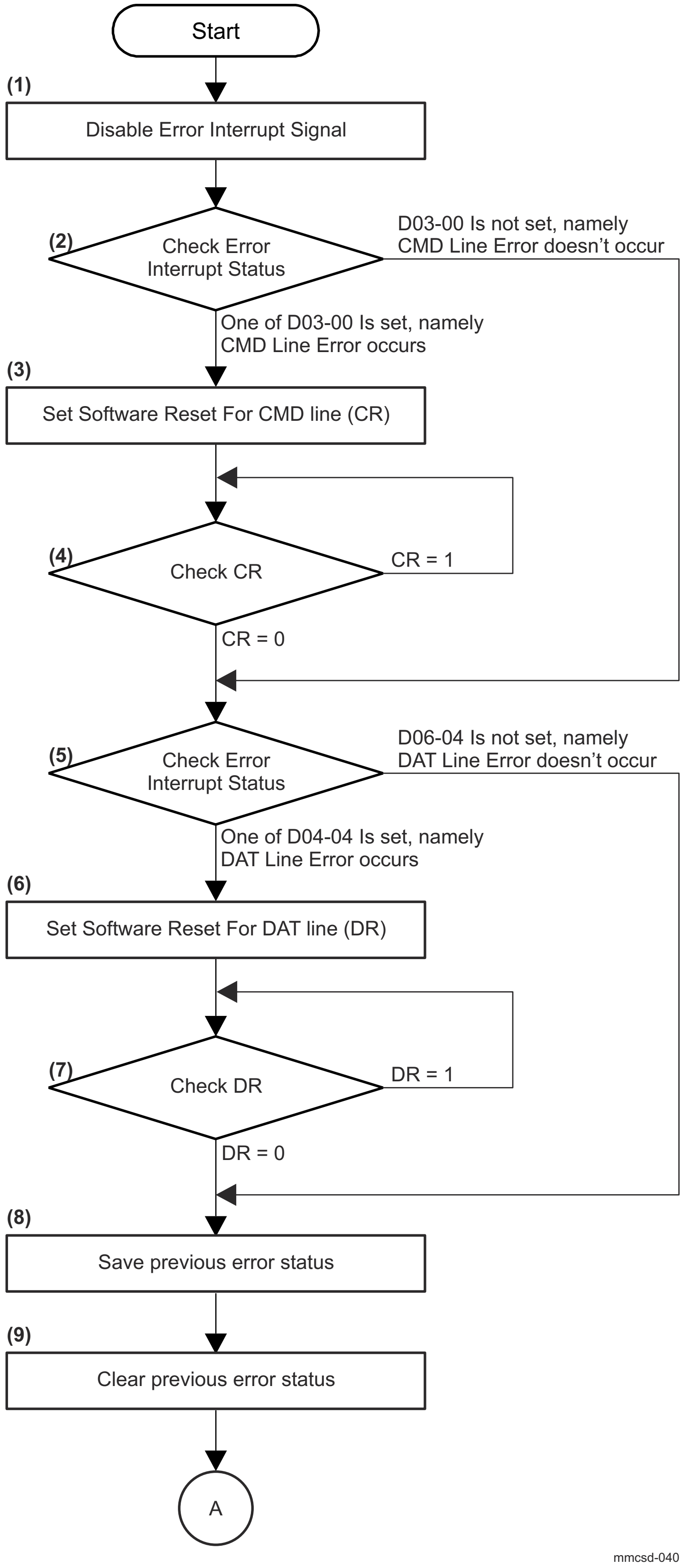

Figure 12-252. Error Interrupt Recovery Sequence (1)

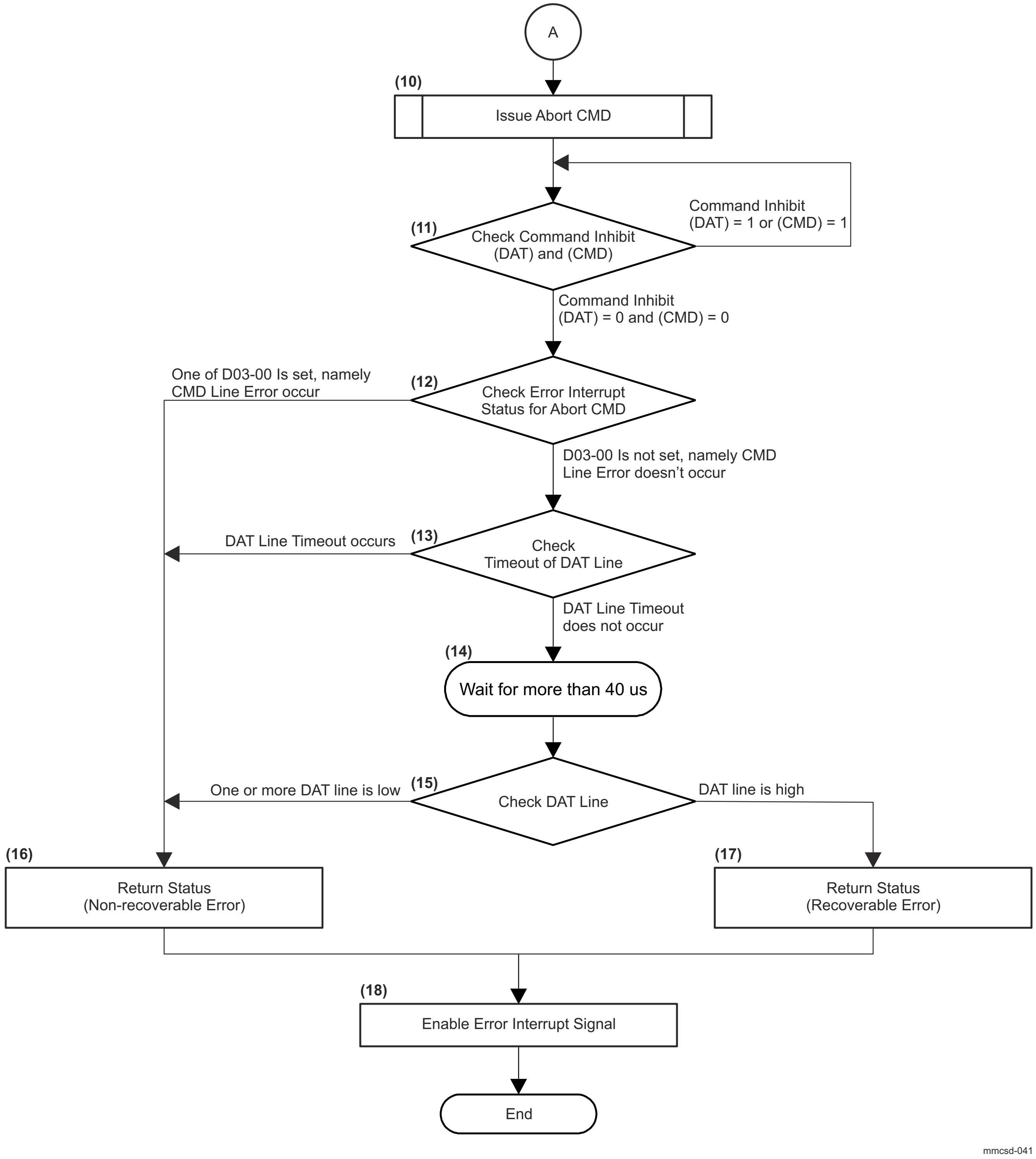

Figure 12-253. Error Interrupt Recovery Sequence (2)

(1) Disable the Error Interrupt Signal (MMCSD0_ERROR_INTR_SIG_ENA).

(2) Check bits D03-00 in the MMCSD0_ERROR_INTR_STS register. If one of these bits (D03-00) is set to 1, go to step (3). If none are set to 1 (all are 0), go to step (5).

(3) Set MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1.

(4) Check MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 0, go to step (5). If it is 1, go to step (4).

(5) Check bits D06-04 in the MMCSD0_ERROR_INTR_STS register. If one of these bits (D06-04) is set to 1, go to step (6). If none are set to 1 (all are 0), go to step (8).

(6) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(7) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (8). If it is 1, go to step (7).

(8) Save previous error status.

(9) Clear previous error status with setting them to 1.

(10) Issue Abort Command.

(11) MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit and MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit. Repeat this step until both MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit and MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit are set to 0.

(12) Check bits D03-00 in the MMCSD0_ERROR_INTR_STS register for Abort Command. If one of these bits is set to 1, go to step (16). If none of these bits are set to 1 (all are 0), go to step (13).

(13) Check MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If this bit is set to 1, go to step (16). If it is 0, go to step (14).

(14) Wait for more than 40 us.

(15) By monitoring the DAT [3:0] Line Signal Level in the MMCSD0_PRESENTSTATE register, judge whether the level of the DAT line is low or not. If one or more DAT lines are low, go to step (16). If the DAT lines are high, go to step (17).

(16) Return Status of "Non-recoverable Error".

(17) Return Status of "Recoverable Error".

(18) Enable the Error Interrupt Signal (MMCSD0_ERROR_INTR_SIG_ENA).

12.3.5.5.1.10.2 Auto CMD12 Error Recovery

Figure 12-254. Auto CMD12 Error Recovery

The sequence for Auto CMD12 Error Recovery is shown in Figure 12-254. Following four cases A-D shall be covered.

A: An error occurred in CMD_wo_DAT, but not in the SD memory transfer.

B: An error occurred in CMD_wo_DAT, and also occurred in the SD memory transfer.

C: An error did not occur in CMD_wo_DAT, but an error occurred in the SD memory transfer.

D: CMD_wo_DAT was not issued, and an error occurred in the SD memory transfer.

(1) Check MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit. If this bit is set to 1, go to step (2). If this bit is set to 0, go to step (6). In addition, the Host Driver shall define PCMD flag, which changes to 1 if MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit is set to 1.

(2) Wait for Error Interrupt Recovery for CMD_wo_DAT.

(3) Check "Return Status". In the case of "Non-recoverable Error", go to step (16). In the case of "Recoverable Error", go to step (4).

(4) Issue CMD12 .

(5) If the CMD line errors occur for the CMD12 (one of D03-00 is set in the MMCSD0_ERROR_INTR_STS register), "Return Status" is "Non-recoverable Error" and go to step (16). If not CMD line error and busy timeout error occur (D04 is set in the MMCSD0_ERROR_INTR_STS register), "Return Status" is "Recoverable Error" and go to step (11). Otherwise, "Return Status" is "No error" and go to step (17).

(6) Set MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 for software reset of the CMD line.

(7) Check MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 0, go to step (8). If it is 1, go to step (7).

(8) Issue CMD12 . Acceptance of CMD12 depends on the state of the card. CMD12 may make the card to return to tran state. If the card is already in tran state, the card does not response to CMD12.

(9) Check "Return Status" for CMD12. If "Return Status" returns "Non-recoverable Error", go to step (16). In the case of "Recoverable Error" or "No error", go to step (10).

(10) Check the MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit. If this bit is 0, go to step (11). If it is 1, go to step (14).

(11) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(12) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (13). If it is 1, go to step (12).

(13) Check the PCMD flag. If PCMD is 1, go to step (18). If it is 0, go to step (19).

(14) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(15) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (20). If it is 1, go to step (15).

(16) Return Status of "Non-recoverable Error".

(17) Return Status that an error has occurred in CMD_wo_DAT, but not in the SD memory transfer.

(18) Return Status that an error has occurred in both CMD_wo_DAT, and the SD memory transfer.

(19) Return Status that an error has not occurred in CMD_wo_DAT, but has occurred in the SD memory transfer.

(20) Return Status that CMD_wo_DAT has not been issued, and an error has occurred in the SD memory transfer.

12.3.5.5.1.11 Wakeup Control (Optional)

After the Host System goes into standby mode, the Host System can resume from standby via a wakeup event initiated by one of the following three events:

(1) Interrupt from a SD card: If an SD card interrupt occurs, the Host System can resume from standby mode. If the Host System uses this wakeup factor, SD Bus power shall be kept on.

(2) Insertion of SD card: If a SD card is inserted, the Host System can resume from standby mode.

(3) Removal of SD card: If a SD card is removed, the Host System can resume from standby mode.

The sequence for preparing wakeup before the Host System goes into standby mode is shown in Figure 12-255.

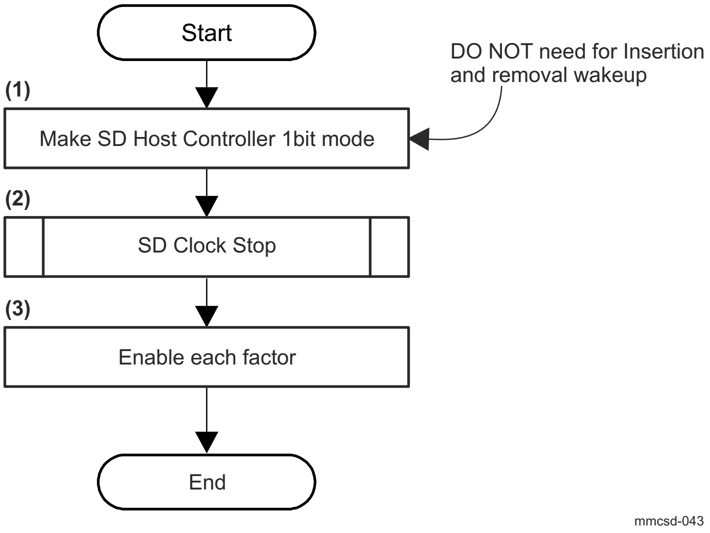

Figure 12-255. Wakeup Control before Standby Mode

(1) Set MMCSD0_HOST_CONTROL1[1] DATA_WIDTH bit to 0.

(2) Execute SD Clock Stop Sequence as described in Section 12.3.5.5.1.2.2 , *SD Clock Supply and Stop Sequence*.

(3) Clear the MMCSD0_NORMAL_INTR_STS register and the MMCSD0_NORMAL_INTR_SIG_ENA register, and then set the enable bits of each wakeup event factor to 1 in the MMCSD0_WAKEUP_CONTROL register and set the bits of MMCSD0_ERROR_INTR_STS_ENA register to use wakeup.

The sequence for wakeup once in standby mode is shown in Figure 12-256.

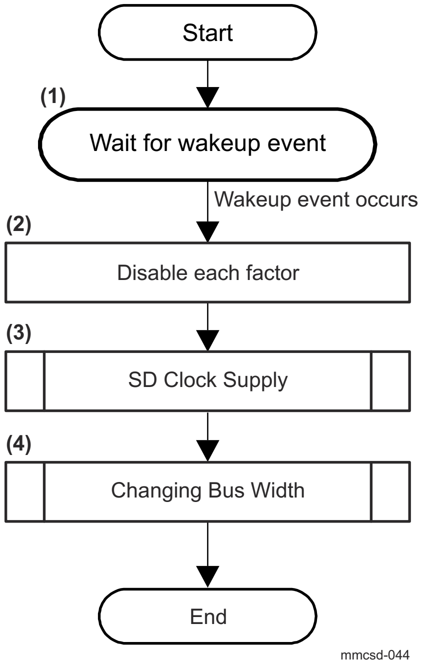

Figure 12-256. Wakeup from Standby

(1) Wait for wakeup event.

(2) Set the enable bits of each wakeup event factor to 0 in the MMCSD0_WAKEUP_CONTROL register and then clear event statuses in the MMCSD0_NORMAL_INTR_STS register. If necessary, set the MMCSD0_NORMAL_INTR_SIG_ENA register.

(3) Execute SD Clock Supply Sequence (see Section 12.3.5.5.1.2.2 , *SD Clock Supply and Stop Sequence*).

(4) Set the SD Bus width (see Section 12.3.5.5.1.4 , *Changing Bus Width*).

12.3.5.5.1.12 Suspend/Resume (Optional, Not Supported from Version 4.00)

If a SD card supports suspend and resume functionality, then the Host Controller can initiate suspend and resume. It is necessary for both the Host Controller and the SD card to support the function of "Read Wait". ADMA operation does not support this function.

12.3.5.5.1.12.1 Suspend Sequence

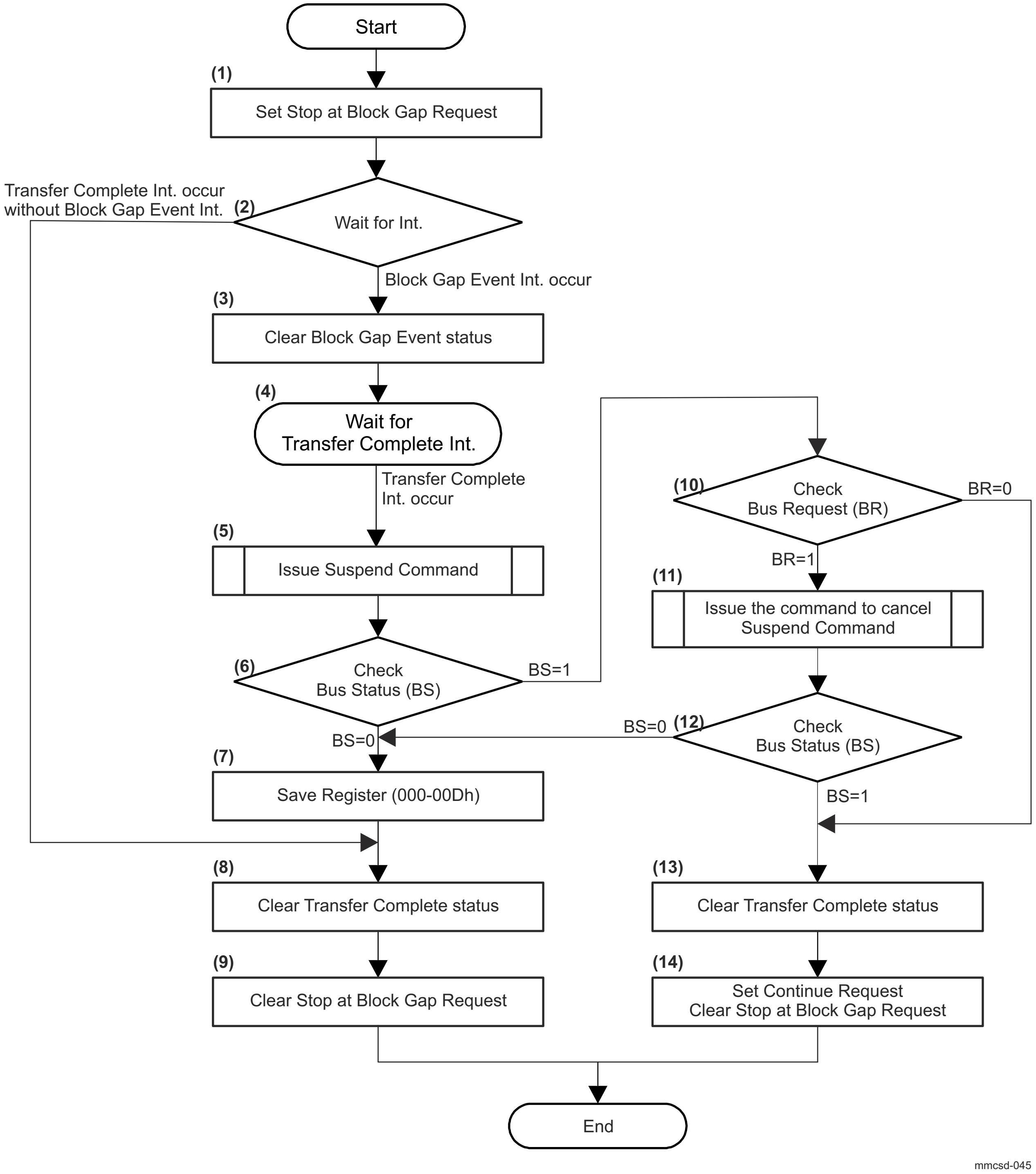

Figure 12-257. The Sequence for Suspend

(1) Set MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 1 to stop the SD transaction.

(2) Wait for an Interrupt. If MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit is set to 0 and MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is set to 1, go to step (8). If MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit is set to 1, go to step (3).

(3) Set MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit to 1 to clear this bit.

(4) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(5) Issue the Suspend Command in accordance with Section 12.3.5.5.1.7.1 , *Transaction Control without Data Transfer Using DAT Line*.

(6) Check the BS value of the response data. If BS is 0, go to step (7). If BS is 1, go to step (10).

(7) Save the register .

(8) Set MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit to 1 to clear this bit.

(9) Set MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 0 to clear this bit.

(10) Check the BR value of the response data. If BR is 1, go to step (11). If BR is 0, go to step (13).

(11) Issues the command to cancel the previous suspend command in accordance with Section 12.3.5.5.1.7.1 , *Transaction Control without Data Transfer Using DAT Line*.

(12) Check the BS value of the response data. If BS is 0, go to step (7). If BS is 1, go to step (13).

(13) Set MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit to 1 to clear this bit.

(14) Set MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 to continue the transaction. At the same time, write 0 to MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to clear this bit.

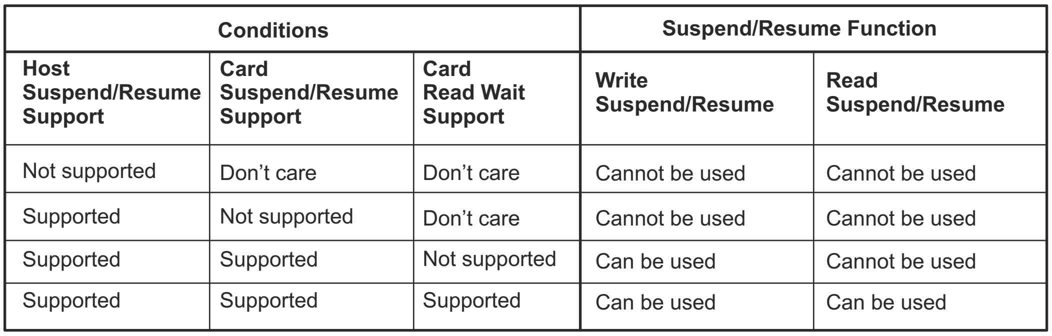

Conditions			Suspend/Resume Function	
Host Suspend/Resume Support	**Card Suspend/Resume Support**	**Card Read Wait Support**	**Write Suspend/Resume**	**Read Suspend/Resume**
Not supported	Don’t care	Don’t care	Cannot be used	Cannot be used
Supported	Not supported	Don’t care	Cannot be used	Cannot be used
Supported	Supported	Not supported	Can be used	Cannot be used
Supported	Supported	Supported	Can be used	Can be used

Figure 12-258. Suspend/Resume Condition

12.3.5.5.1.12.2 Resume Sequence

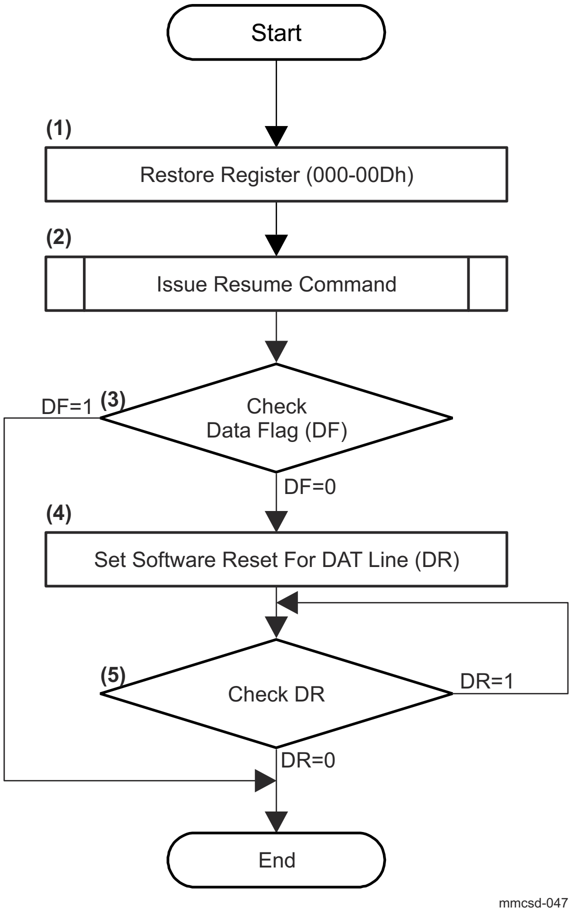

Figure 12-259. The Sequence for Resume

(1) Restore the register .

(2) Issue the Resume Command .

(3) Check the DF value of the response data. If DF is 0, go to step (4). If DF is 1, go to "End".

(4) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(5) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to "End". If it is 1, go to step (5).

12.3.5.5.1.12.3 Stop At Block Gap/Continue Timing for Read Transaction

The timing of Stop At Block Gap Request and Continue Request. The Transfer Complete interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is always generated by setting MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit where data transfer is stopped. However, generation of the Block Gap Event interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is dependent on whether the last data block is sent or not. Block Gap Event is not generated If all data blocks are transferred (the last block is transferred). It is not necessary to enable Block Gap Event interrupt. The status can be checked when transfer complete interrupt is detected. It is not necessary to use Continue Request (MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE) if Block Gap Event status is not set because there is no further data to be transferred. If Read Wait is not supported, Host Controller stops SD Clock at the block gap.

Implementation Note:

The MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL, MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE, MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bits shall be set and cleared by the Host Controller.

The MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set and cleared by the Host Driver. The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit shall be set by the Host Driver and be cleared by the Host Controller. The MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit and MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit shall be set by the Host Controller and be cleared by the Host Driver.

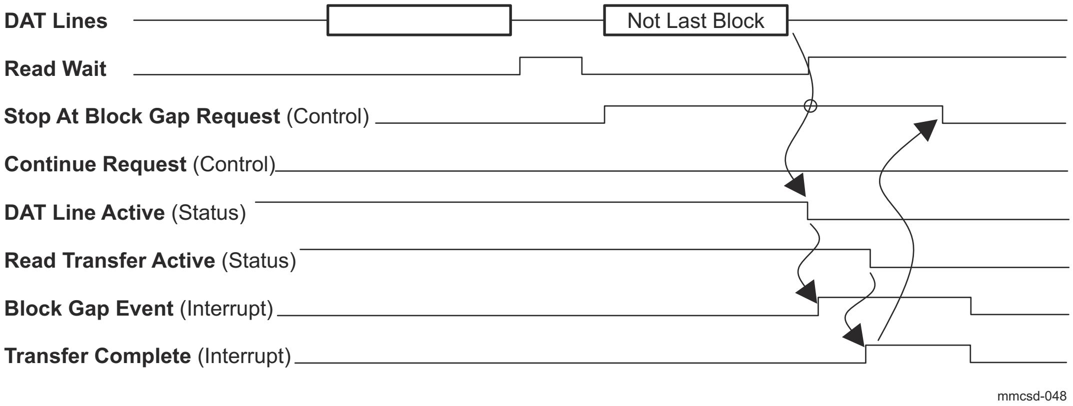

Figure 12-260. Wait Read Transfer by Stop At Block Gap Request

The Host Controller can accept a Stop At Block Gap Request (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP) when all the following conditions are met.

(1) It is at the block gap.

(2) The Host Controller can assert read wait or it is already asserted.

(3) The MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit is set to 1.

After accepting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit:

(1) Clear MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT).

(2) After all valid data has been read (No valid read data remains in the Host Controller), clear the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE).

(3) After accepting MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit, clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

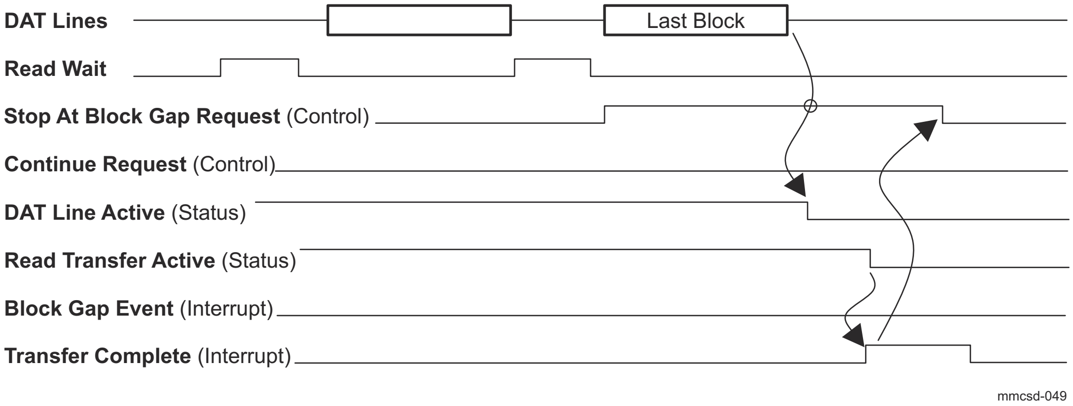

Figure 12-261. Stop At Block Gap Request is Not Accepted at the Last Block of the Read Transfer

If the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1 during the last block transfer, the Host Controller shall not accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and stops the transaction normally. The Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is not generated. When the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is generated, and if the MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit status is not set to 1, the driver shall clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

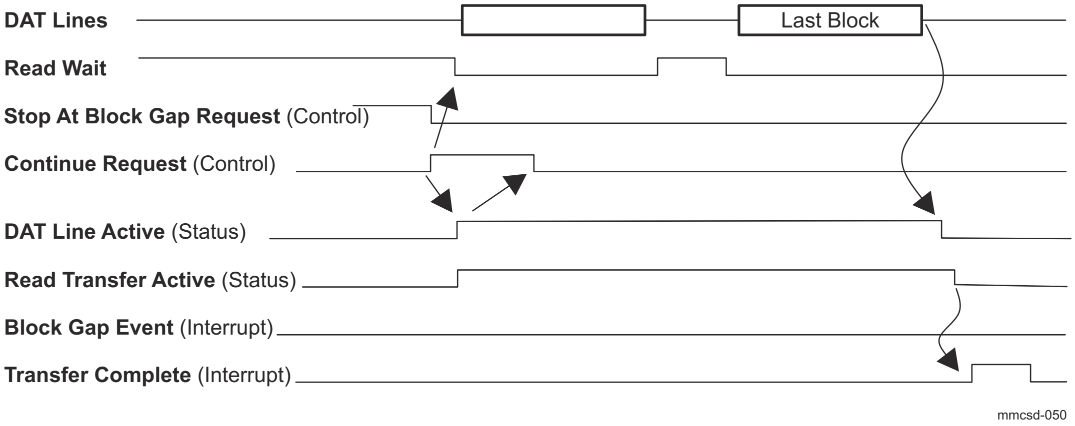

Figure 12-262. Continue Read Transfer by Continue Request

To restart a stopped data transfer, set the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 (the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set to 0).

After accepting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit:

(1) Release MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit (if the data block can accept the next data).

(2) Set the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit.

(3) The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit is automatically cleared by (2).

The end of the read transfer is specified by data length.

(1) Clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and do not generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit).

(2) After all valid data has been read (No valid read data remains in the Host Controller), clear the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

12.3.5.5.1.12.4 Stop At Block Gap/Continue Timing for Write Transaction

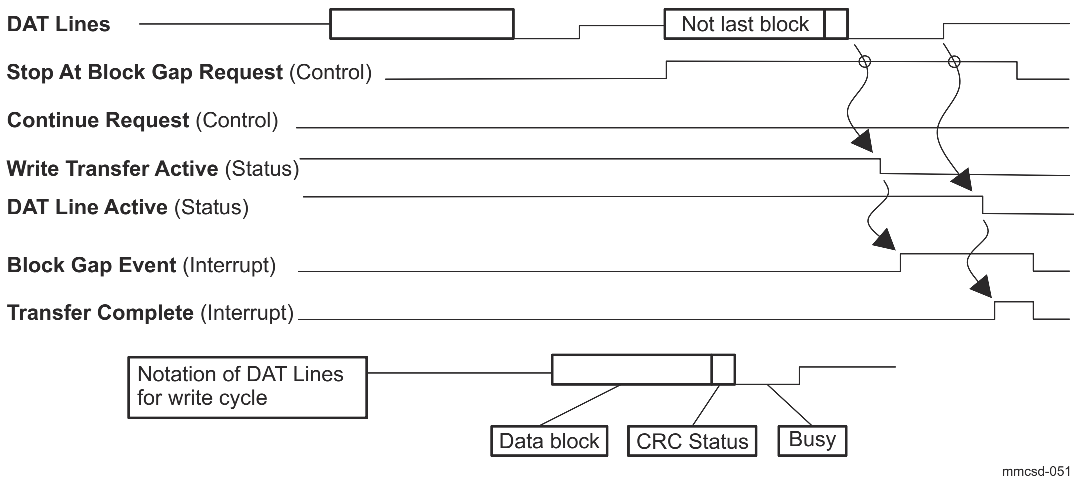

Figure 12-263. Wait Write Transfer by Stop At Block Gap Request

The Host Controller can accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit when matches all following conditions:

(1) It is at the block gap.

(2) No valid write data remains in the Host Controller.

After accepting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

(1) Clear the MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit and generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit).

(2) After the busy signal is released, clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

(3) After accepting the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit), clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

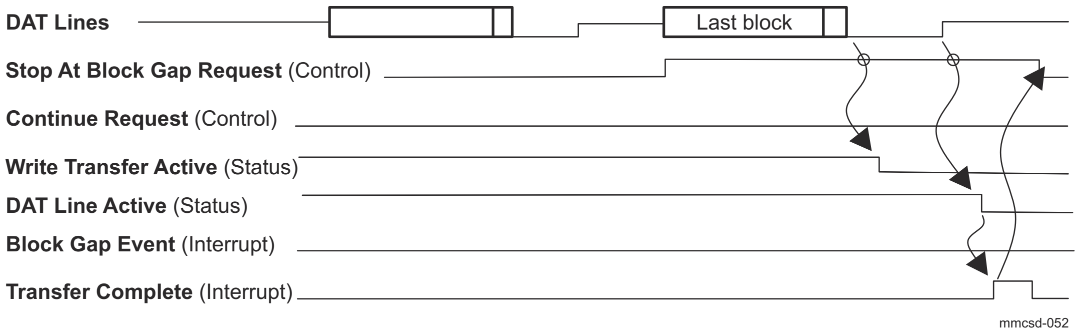

Figure 12-264. Stop At Block Gap Request is Not Accepted at the Last Block of the Write Transfer

If the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1 during the last block transfer, the Host Controller shall not accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and terminates the transaction normally. The Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is not generated. When the Transfer

Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is generated, and if the MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVEN bit is not set to 1, the driver shall clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

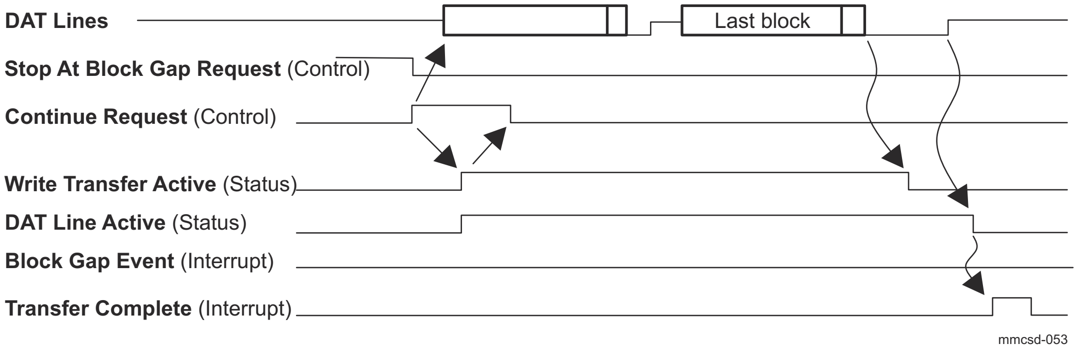

Figure 12-265. Continue Write Transfer by Continue Request

To restart a stopped data transfer, set the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 (the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set to 0).

After accepting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit:

(1) Set the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit.

(2) The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit is automatically cleared by (1).

The end of transfer is specified by data length.

(1) Clear the MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit, and do not generate the (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVEN).

(2) After the busy signal is released, clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generates the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

12.3.5.5.2 Driver Flow Sequence

Note

This section is applicable for MMCSD0 and MMCSD1 but MMCSD0 registers are used in the content.

Note

UHSII is not supported. For more information, see *MMCSD Not Supported Features*.

12.3.5.5.2.1 Host Controller Setup and Card Detection

12.3.5.5.2.1.1 Host Controller Setup Sequence

Figure 12-266 and Table 12-319 show a Host Controller setup sequence.

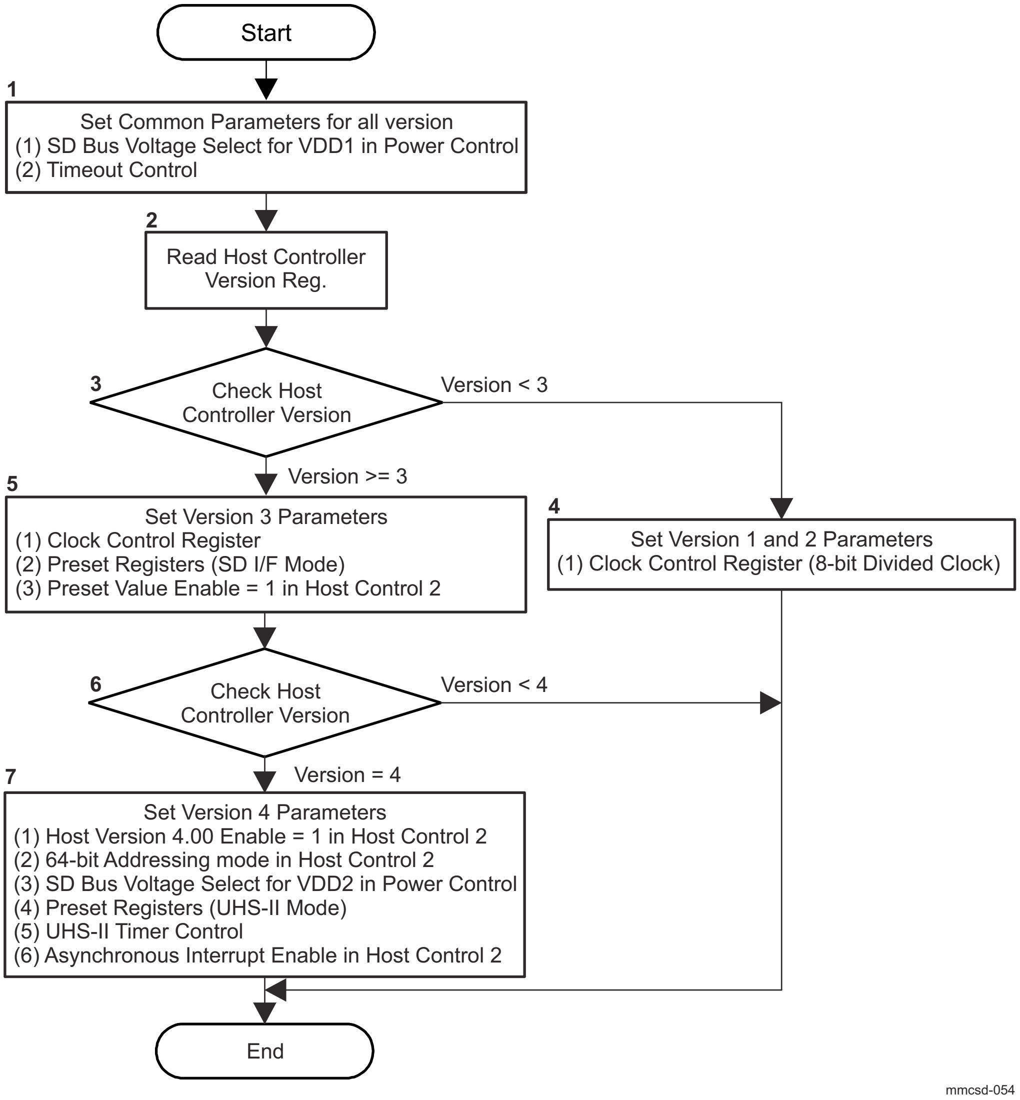

Figure 12-266. Host Controller Setup Sequence

Table 12-331. Host Controller Setup Sequence

Step	Description
1	Set parameters for all Host Controller version. Set the MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE and MMCSD0_TIMEOUT_CONTROL[3-0] COUNTER_VALUE bit fields.
2	Read the MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM bit field.
3	If Specification Version number (MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM) is less than version 3, go to step (4), if it is version 3 or later go to step (5).
4	Set the MMCSD0_CLOCK_CONTROL register using 8-bit Divided Clock mode.
5	Set Version 3 parameters. The MMCSD0_CLOCK_CONTROL register is sets in 10-bit Divided Clock Mode or Programmable Clock Mode. If Clock Multiplier in the MMCSD0_CAPABILITIES register is not zero, Programmable Clock Mode should be used. If Preset Value is used, set Preset Values of SD I/F Modes in the Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10) and set the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit to 1.
6	If Specification Version number (MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM) is version 4, go to step (7), if it is less than version 4, exits.
7	Set Version 4 parameters. Set the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit to 1. If the MMCSD0_CAPABILITIES[27] ADDR_64BIT_SUPPORT_V4 bit is set to 1, set the MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit to 1. If UHS-II Support is set to 1 and 1.8 V VDD2 Support is set to 1 in the MMCSD0_CAPABILITIES register, set SD Bus Voltage Select for VDD2 to 1.8 V mode in the MMCSD0_POWER_CONTROL register, set preset value for UHS-II Mode to Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10) and set Timeout Counter Value for CMD_RES and Timeout Counter Value for Deadlock in the MMCSD0_UHS2_TIMER_CONTROL register based on Timeout Clock Frequency and Timeout Clock Unit in the MMCSD0_CAPABILITIES register. If Asynchronous Interrupt Support in the MMCSD0_CAPABILITIES register is set to 1, set Asynchronous Interrupt Enable to 1 in the MMCSD0_HOST_CONTROL2 register.

12.3.5.5.2.1.2 Card Interface Detection Sequence

This procedure is invoked by the Card Insertion interrupt. Figure 12-267 and Table 12-320 show a card interface detection sequence.

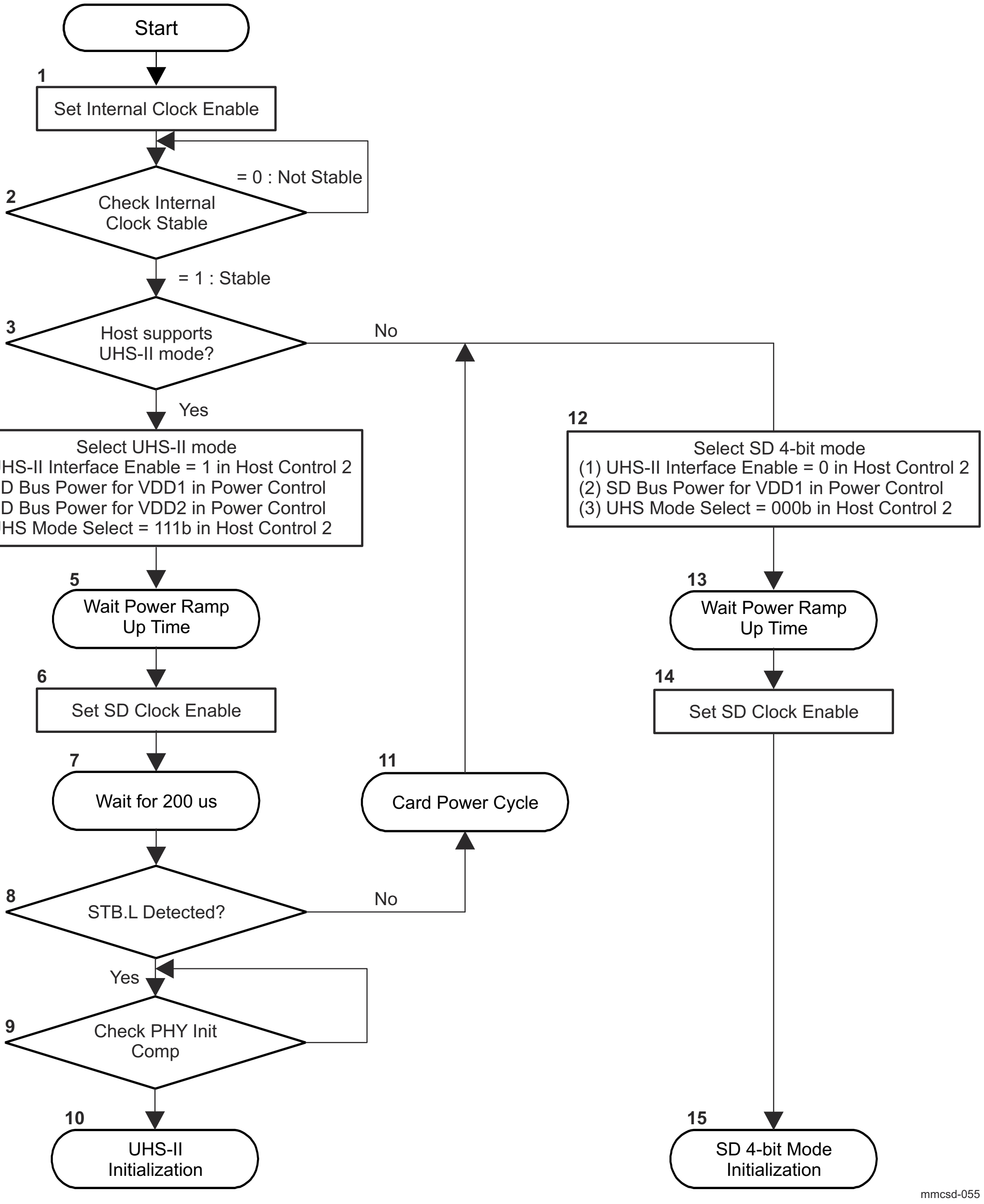

Figure 12-267. Card Interface Detection Sequence

Table 12-332. Card Interface Detection Sequence

Step	Description
1	Set Internal Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
2	Wait until Internal Clock Stable is set to 1 in the MMCSD0_CLOCK_CONTROL register.
3	If Host Supports UHS-II, go to step (4) else go to step (12).
4	Try to initialize a card to UHS-II mode. Set UHS-II Interface Enable to 1 in the MMCSD0_HOST_CONTROL2 register, set SD Bus Power for VDD1 and SD Bus Power for VDD2 to 1 in the MMCSD0_POWER_CONTROL register, and set UHS Mode Select to 111b in the MMCSD0_HOST_CONTROL2 register.

Table 12-332. Card Interface Detection Sequence (continued)

Step	Description
5	Wait power ramp up time. It is dependent on a Host System.
6	Set SD Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
7	Wait 200 μs to check a card supports UHS-II mode.
8	Check STB.L Detection in the MMCSD0_PRESENTSTATE register. If UHS-II IF is detected, go to step (9). If UHS-II IF is not detected, go to step (11).
9	Wait until Lane Synchronization in the MMCSD0_PRESENTSTATE register is set to 1 (PHY Initialization is completed).
10	Perform UHS-II initialization.
11	Perform card power cycle.
12	Try to initialize a card to SD 4-bit mode. Set UHS-II Interface Enable to 0 in the MMCSD0_HOST_CONTROL2 register, set SD Bus Power for VDD1 to 1 in the MMCSD0_POWER_CONTROL register, and set UHS Mode Select to 000b in the MMCSD0_HOST_CONTROL2 register.
13	Wait power ramp up time. It is dependent on a Host System.
14	Set SD Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
15	Perform SD 4-bit mode initialization. Refer to Section 12.3.5.5.1.6 , *Card Initialization and Identification (for SD I/F)*.

12.3.5.5.2.2 Boot Operation

The boot operation sequence is shown in Figure 12-268.

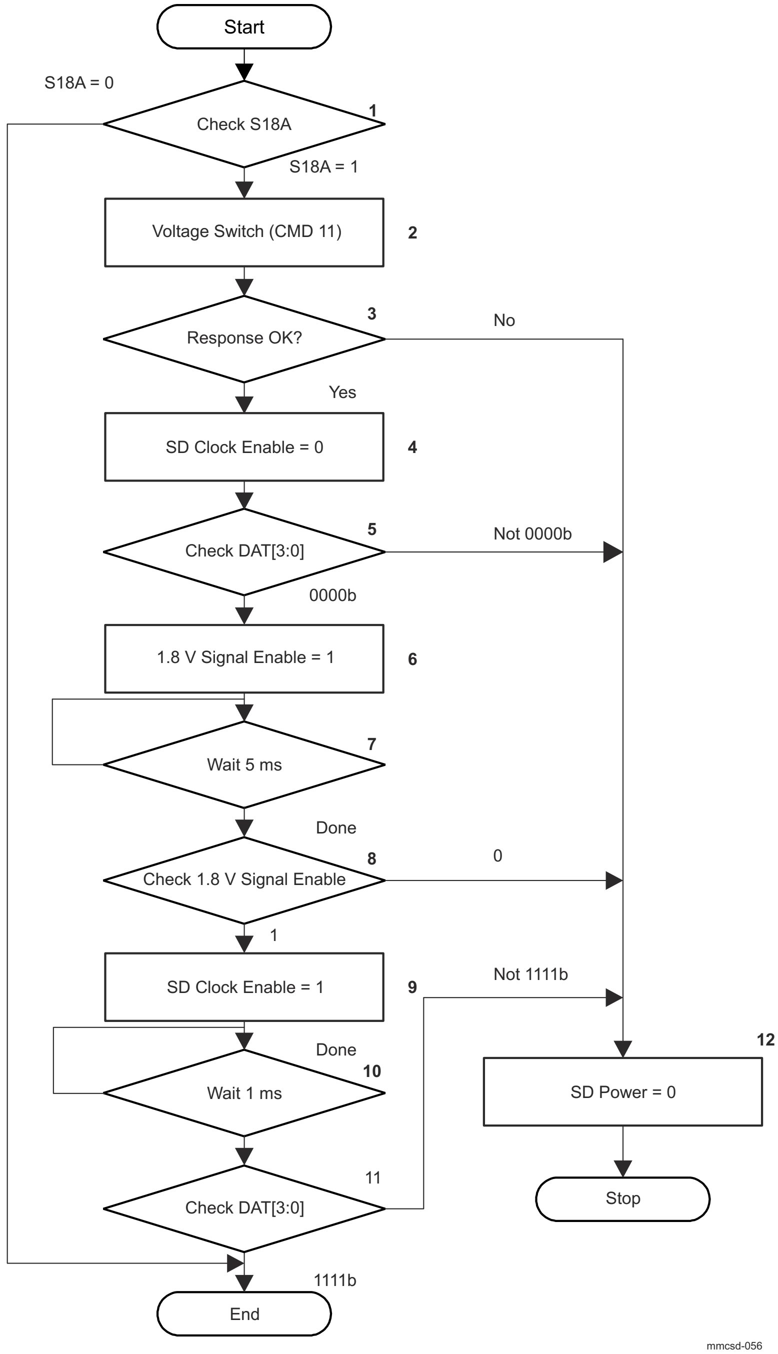

Figure 12-268. Boot Operation Sequence

12.3.5.5.2.2.1 Normal Boot Operation: (For Legacy eMMC 5.0)

The Host driver writes the boot timeout value into MMCSD0_BOOT_TIMEOUT_CONTROL register as per the eMMC4.3+ spec.

When the Host driver sets the "BOOT_ENABLE" to 1 in MMCSD0_BLOCK_GAP_CONTROL register and "DATA_XFER_DIR" bit to "1" in MMCSD0_TRANSFER_MODE register, the Host controller drives the CMD line to "0" for boot operation.

If the Host controller is configured to wait for boot acknowledgement from the eMMC4.3+ device, the controller receives the boot acknowledgement and asserts the "RCV_BOOT_ACK" interrupt to the driver

(MMCSD0_NORMAL_INTR_STS[13] RCV_BOOT_ACK). If the Host controller doesn't receive the boot acknowledgement from the device within the timeout value, the Host controller will assert the data timeout error interrupt (MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT).

After servicing the boot acknowledge interrupt or data timeout error interrupt, the driver programs the MMCSD0_BOOT_TIMEOUT_CONTROL register with boot data timeout value.

The eMMC4.3+ device starts sending the boot data on the data line and Host controller sends the same to system whenever a block of data is received from device. The Host controller terminates the boot operation when the programmed number of blocks is transferred to the System. The Driver can writes "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register.

The boot operation can also be terminated in between the boot transfer (the Driver can set the "BOOT_ENABLE" as "0" anytime to disable the boot operation). After the boot termination, the Host controller asserts soft reset for CMD line and DATA line internally once the driver clears the BOOT_COMPLETE interrupt (MMCSD0_NORMAL_INTR_STS[14] BOOT_COMPLETE), to reset all the state machines to idle state.

There is no need to perform error recovery sequence in case data timeout interrupt occurs during boot operation (ignore sending abort command, soft reset and just clear the timeout interrupt and proceed with the boot flow).

If the device sends wrong acknowledgement to the Host, the Host controller will assert Data CRC Error interrupt (MMCSD0_ERROR_INTR_STS[5] DATA_CRC) on the Driver. In this case, the Host driver has to stop the boot mode operation by setting "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

If the device sends end bit as "0" in acknowledgement to the Host, the Host controller will assert Data End Bit Error interrupt (MMCSD0_ERROR_INTR_STS[6] DATA_ENDBIT) on the Driver.

The Host driver stops the boot mode operation by setting "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

Note: Enable the MMCSD0_BLOCK_GAP_CONTROL[7] BOOT_ACK_ENA bit during boot operation. If failed, the controller will not wait for boot acknowledge from the card and send out data CRC error when the card sends boot acknowledgement first and followed by boot data.

12.3.5.5.2.2.2 Alternate Boot Operation (For Legacy eMMC 5.0):

The Host driver writes the boot timeout value as per the eMMC4.3+ spec into MMCSD0_BOOT_TIMEOUT_CONTROL register.

If the "ALT_BOOT_MODE" and "BOOT_ENABLE" is set to 1 in MMCSD0_BLOCK_GAP_CONTROL register and "DATA_XFER_DIR" bit is set to 1 in MMCSD0_TRANSFER_MODE register, the host controller drives the CMD0 (0xFFFFFFFA) on the CMD line.

The system shall wait for command complete interrupt before "RCV_BOOT_ACK" interrupt (MMCSD0_NORMAL_INTR_STS[13] RCV_BOOT_ACK).

If the Host controller is configured to wait for boot acknowledgement from the eMMC4.3+ device, the controller receives the boot acknowledgement and asserts the "RCV_BOOT_ACK" interrupt to the driver.

The eMMC4.3+ device starts sending the boot data on the data line and Host controller sends the same to system whenever a block of data is received from device. The System needs to send CMD0 to inform the device about the boot operation complete. The system shall program MMCSD0_COMMAND register with argument "00000000h" for the CMD0 and waits for command complete.

The Host controller terminates the boot operation when the programmed number of blocks are transferred to the System and the Driver shall send CMD0 to eMMC card and then program "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register.

The boot operation can be terminated at any time (the Driver can send CMD0 and set the "BOOT_ENABLE" as "0" anytime to disable the boot operation). After the boot termination, all state machines in the Host controller need to move to IDLE state. The Host controller asserts the soft reset for CMD and data line internally when the driver clears the BOOT_COMPLETE interrupt (MMCSD0_NORMAL_INTR_STS[14] BOOT_COMPLETE) and all the state machine goes to the idle state.

If the Host controller doesn't receive the acknowledgement from the device with in timeout value the Host controller will assert the data timeout error interrupt (MCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT).

The driver programs the MMCSD0_BOOT_TIMEOUT_CONTROL register with boot data timeout value.

There is no need to perform error recovery sequence in case of data timeout interrupt as mentioned above. If the device sends wrong acknowledgement to the Host, then Host controller will assert Data CRC Error interrupt to the Driver (MCSD0_ERROR_INTR_STS[5] DATA_CRC). The Host driver has to stop the boot mode operation by setting "ALT_BOOT_MODE" and "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

If the device sends end bit as "0" in acknowledgement to the Host, the Host controller asserts Data End Bit Error interrupt (MCSD0_ERROR_INTR_STS[6] DATA_ENDBIT) on the Driver. The Host driver stops the boot mode operation by setting "ALT_BOOT_MODE" and "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

Note: Enable the MMCSD0_BLOCK_GAP_CONTROL[7] BOOT_ACK_ENA bit during boot operation . If failed, the controller will not wait for boot acknowledge from the card and send out data CRC error when the card sends boot acknowledgement first and followed by boot data.

12.3.5.5.2.2.3 Boot Code Chunk Read Operation (For Legacy eMMC 5.0):

The following figure explains the boot code read done as chunks of data (the Driver can read the boot data as 2K, 4K, 1K and 8K etc. instead of 128K at a time

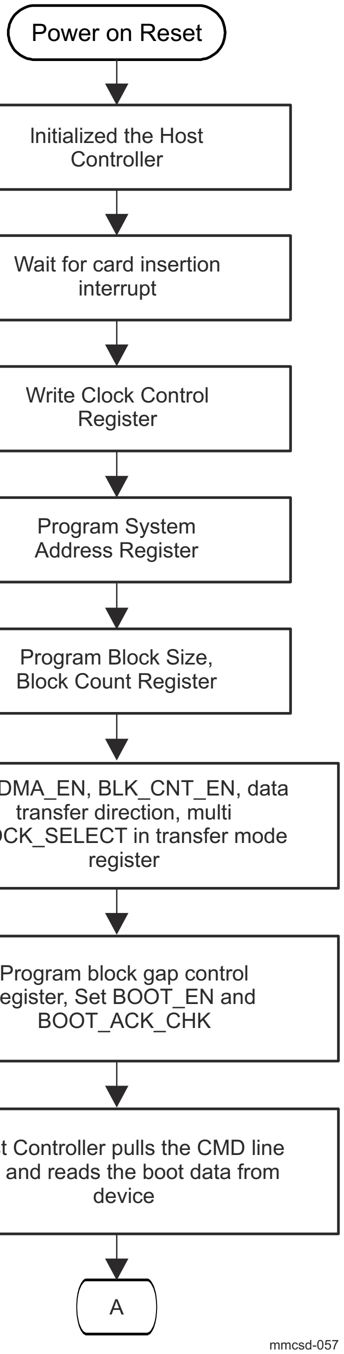

Figure 12-269. Boot Code Access Flow Diagram (1)

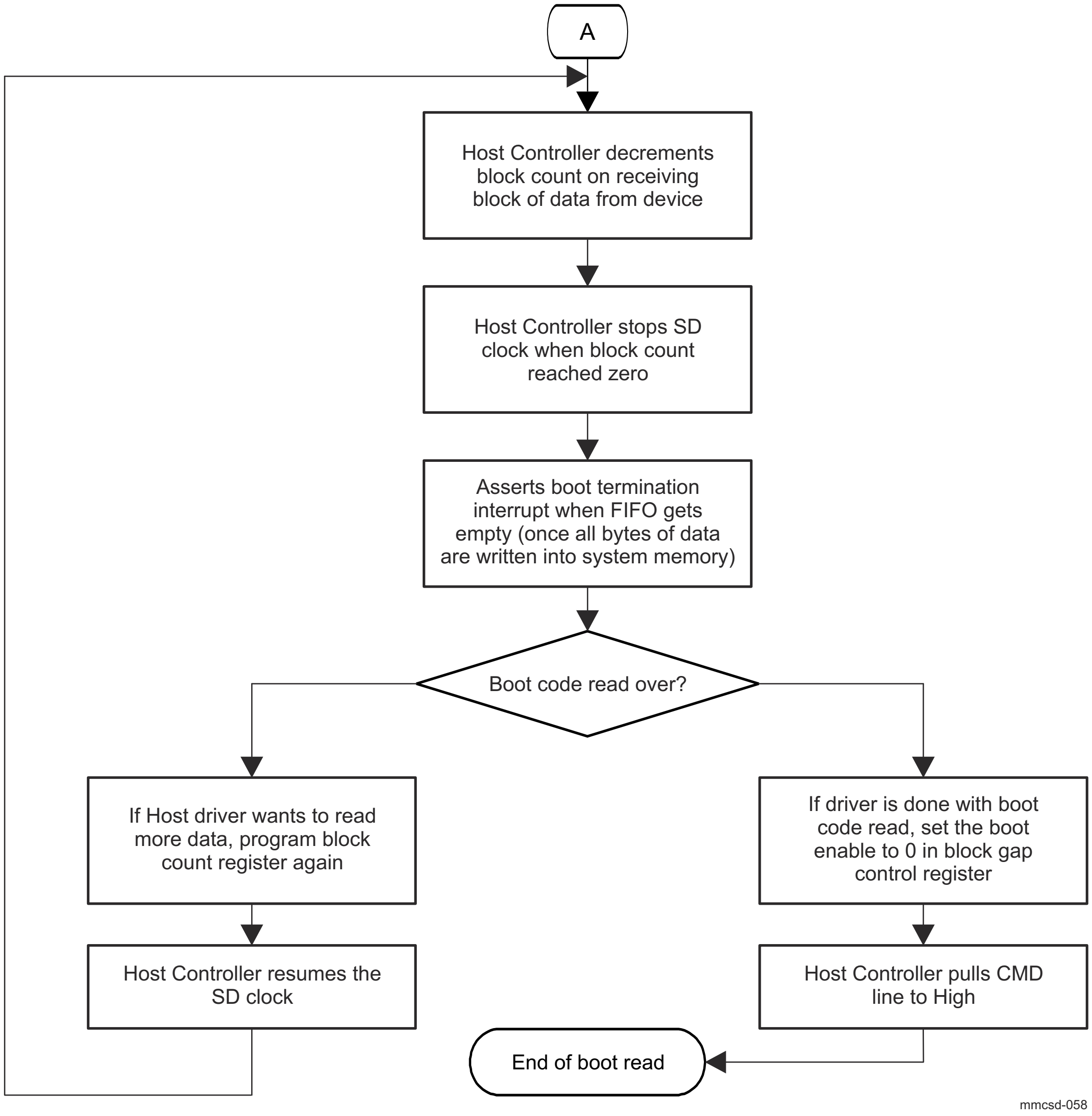

Figure 12-270. Boot Code Access Flow Diagram (2)

12.3.5.5.2.3 Retuning procedure (For Legacy Interface)

12.3.5.5.2.3.1 Sampling Clock Tuning

The SD bus can be operating in high clock frequency mode and then the data window from the card on CMD and DAT[3:0] lines gets smaller. The position of the data window will vary depending on the card and host system implementation. Therefore, the Host Controller shall support a tuning circuit when SDR104 or SDR50.

The Host Controller shall support a tuning circuit when SDR104 or SDR50 (if Use Tuning for SDR50 is set to 1 in the MMCSD0_CAPABILITIES register) is supported by executing the tuning procedure and adjusting the sampling clock. Execute Tuning and Sampling Clock Select in the MMCSD0_HOST_CONTROL2 register are used to control the tuning circuit.

12.3.5.5.2.3.2 Tuning Modes

The re-tuning timing is specified by two methods: Re-Tuning Request generated by Host Controller and expiration of a re-tuning timer prepared by Host Driver.

(1) Re-Tuning Mode 1 The host controller does not have any internal logic to detect when the re-tuning needs to be performed. In this case, the Host Driver should maintain all re-tuning timings by using a Re-Tuning Timer. To enable inserting the re-tuning procedure during data transfers, the data length per read/write command shall be limited up to 4 MB.

(2) Re-Tuning Mode 2 The host controller has the capability to indicate the re-tuning timing by Re-Tuning Request during data transfers. Then the data length per read/write command shall be limited up to 4 MB. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled.

12.3.5.5.2.3.3 Re-Tuning Mode 2

The Figure 12-271 defines sampling clock tuning procedure supported by Host Controller. In default, for lower frequency operation, fixed sampling clock is used to receive signals on CMD and DAT[3:0]. Before using SDR104, sampling clock tuning is required. Start of sampling clock tuning is requested by setting Execute Tuning to 1 and Sampling Clock Select to 0.

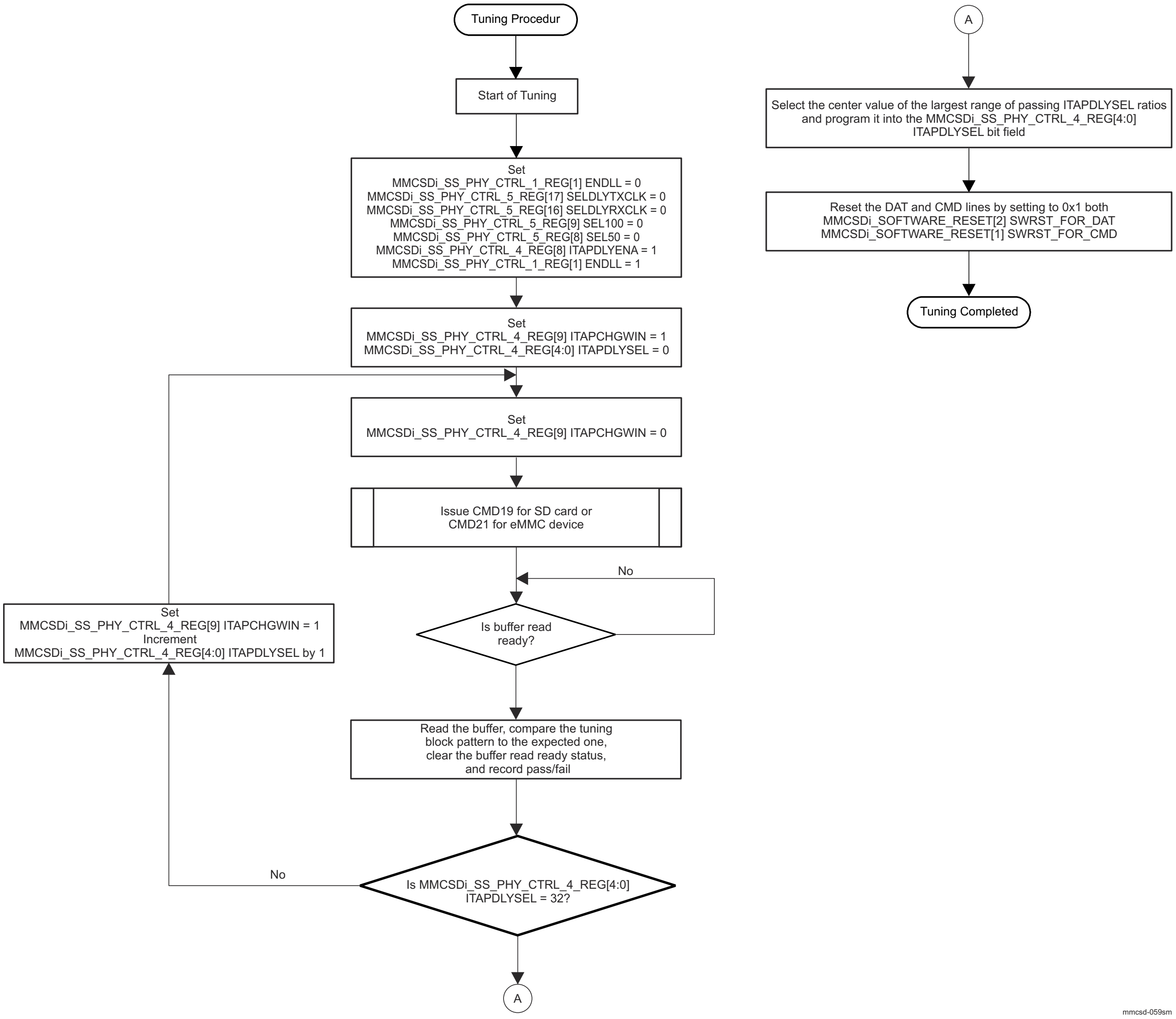

Figure 12-271. MMCSD Clock Tuning

Host driver issue CMD19 repeatedly until the host controller resets Execute Tuning to 0. Host Controller resets Execute Tuning to 0 when tuning is completed or tuning is not completed within 40 times. Host Driver can abort this loop by 40 times CMD19 issue or 150 ms time-out.

If tuning is completed successfully, Host Controller set Sampling Clock Select to 1 and this means the Host Controller start to use tuned sampling clock. If tuning is failed, Host Controller keeps Sampling Clock Select to 0. By writing Sampling Clock Select to 0, sampling clock is switched from tuned sampling clock to fixed sampling clock. Re-tuning time would be smaller than the first tuning time. CMD19 response errors are not indicated while tuning is performed.

The clock tuning tap delay values are selected using Variable sampling point detection. Fixed tap delay value is used for fixed tuning clock method.

12.3.5.5.2.4 Command Queuing Driver Flow Sequence

12.3.5.5.2.4.1 Command Queuing Initialization Sequence

Figure 12-272 and Table 12-321 show a Command Queuing initialization sequence.

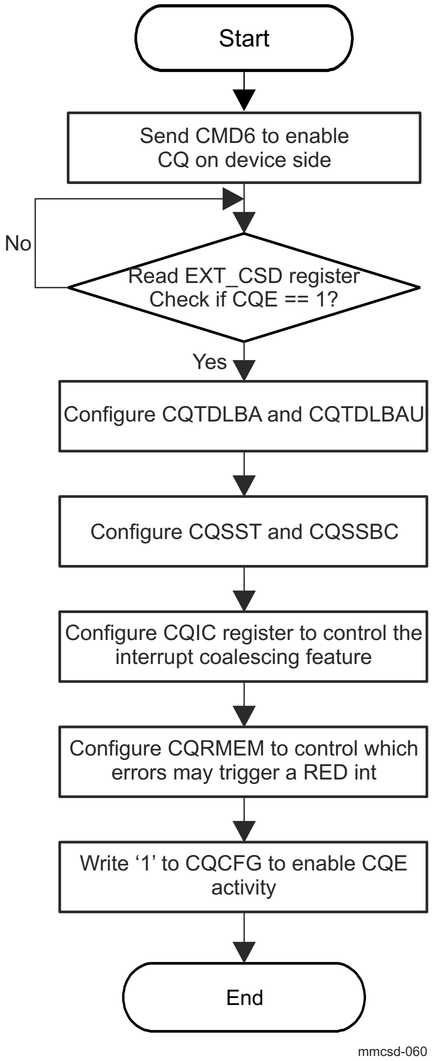

Figure 12-272. Command Queuing Initialization Sequence

Table 12-333. Command Queuing Initialization Sequence

Step	Description
1	Initialize and enable Command Queueing in the device.

Table 12-333. Command Queuing Initialization Sequence (continued)

Step	Description
2	Configure Task Descriptor size in MMCSD0_CQ_CONFIG register.
3	Configure MMCSD0_CQ_TDL_BASE_ADDR and MMCSD0_CQ_TDL_BASE_ADDR_UPBITS registers to point to the memory location allocated to the TDL in host memory.
4	Configure CQSST and CQSSBC to control when SEND_QUEUE_STATUS commands are sent to the device by CQE.
5	Configure MMCSD0_CQ_INTR_COALESCING register to control the interrupt coalescing feature: enable/disable, set interrupt count and timer protection.
6	Configure MMCSD0_CQ_RESP_ERR_MASK register to control which errors may trigger a RED interrupt (if different from reset values).
7	Write '1' to MMCSD0_CQ_CONFIG register to enable CQE activity.

12.3.5.5.2.4.2 Task Issuance Sequence

Figure 12-273 and Table 12-322 show a task issuance sequence.

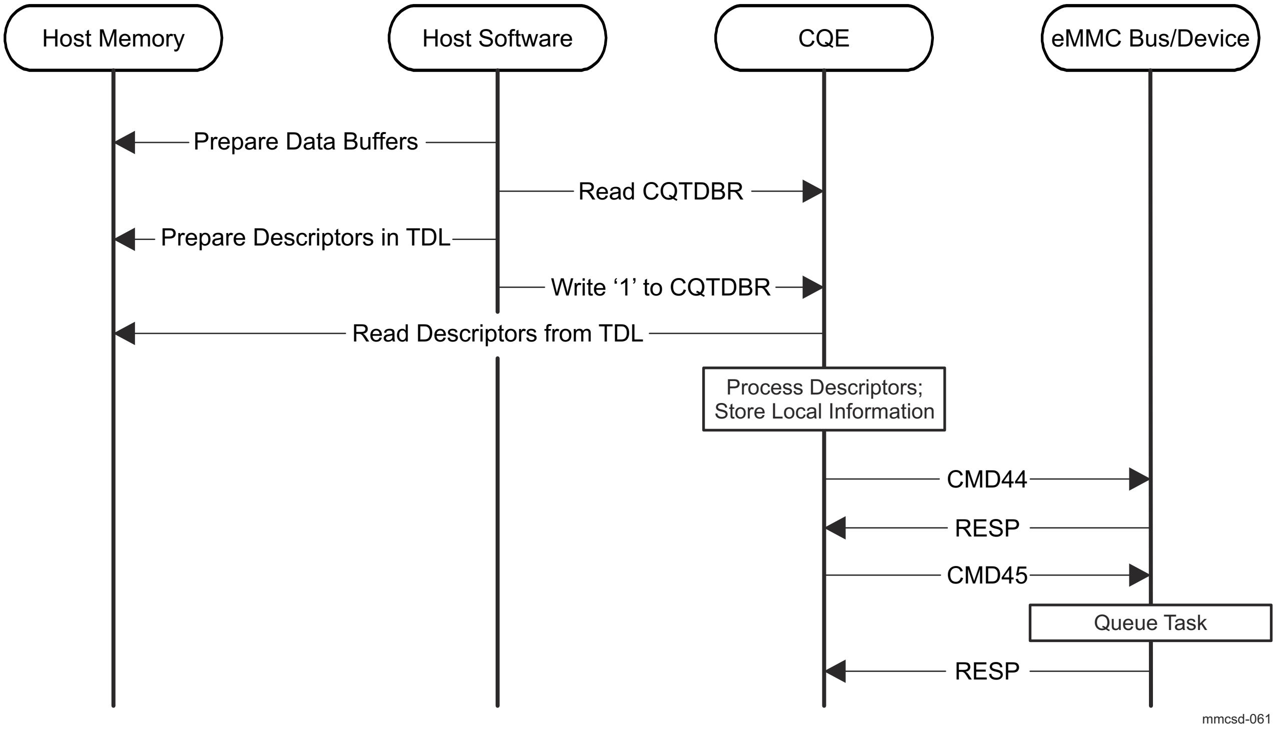

Figure 12-273. Task Issuance Sequence

Table 12-334. Task Issuance Sequence

Step	Description
1	Find an empty transfer request slot by reading the MMCSD0_CQ_TASK_DOOR_BELL register. An empty transfer request slot has its respective bit cleared to '0' in the MMCSD0_CQ_TASK_DOOR_BELL register.

Table 12-334. Task Issuance Sequence (continued)

Step	Description
2	Build a Task Descriptor at the 1st entry of the empty slot. Task Descriptor field values: • 1. Valid = 1, to indicate the descriptor is effective. • 2. End = 1, as required for Task Descriptors. • 3. Int = 1, if an interrupt on completion is required. Otherwise, Int = 0. • 4. Act = b101, to indicate a Task Descriptor . • 5. Data Direction = 1 for read commands, and 0 for write commands. • 6. Priority = 1 for high priority, and 0 for simple requests. • 7. QBR = 1 if Queue Barrier functionality is required. 0 otherwise. • 8. Forced Programming, Context ID, Tag Request, Reliable Write, Block Count, and Block Address programmed according to application requirements.
3	Build a Transfer Descriptor at the 2nd entry of the empty slot. Transfer Descriptor field values: • 1. Valid = 1, to indicate the descriptor is effective. • 2. End = 1, if a TRAN descriptor is used, to indicate the task only has one data buffer. End = 0 if LINK descriptor is used. • 3. Int = 0. Ignore in Command queueing. • 4. Act = b100, for TRAN descriptors, pointing directly to the task's single data buffer. Act = 401 b110, for LINK descriptors, point to a scatter/gather list (indirect). • 5. Address and Length programmed according to the data buffer supplied by the application.
4	If more than one transfer is requested, repeat step 1-3 for all needed transfers.
5	Set MMCSD0_CQ_TASK_DOOR_BELL register to indicate to the CQE that one or more transfer requests are ready to be sent to the attached device. Host software shall only write a '1' to the bit position that corresponds to new tasks; all other bit positions within MMCSD0_CQ_TASK_DOOR_BELL register should be written with a '0', which indicates no change to their current values.

12.3.5.5.2.4.3 Task Execution and Completion Sequence

The CQE is responsible for task execution, communication with the device and moving the data to the buffers in the host memory.

Figure 12-274 and Table 12-323 show a task execution and completion sequence.

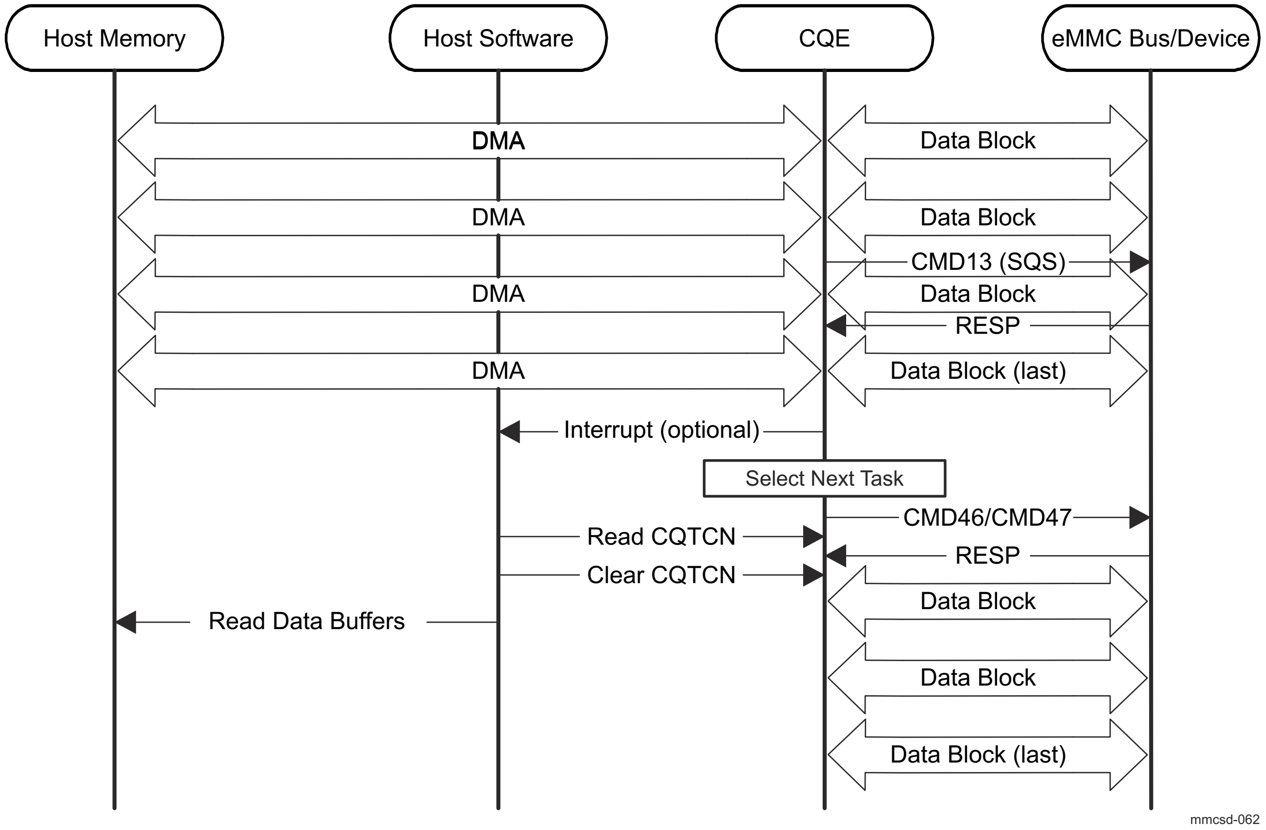

Figure 12-274. Task Execution and Completion Sequence

Table 12-335. Task Execution and Completion Sequence

Step	Description
1	Once the tasks are queued on the device side CQE sends CMD13 to determine the queue status. The queue status lets the CQE know which tasks are ready for execution.
2	The response to CMD13 may indicate no task is ready in which case the CQE is required to send CMD13 again at a later time as controlled CQSST register.
3	If a task is ready for execution then the host sends EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) to the device with the task id ordering it to execute a task.
4	When the task execution is completed, an interrupt may be generated, if requested, or as determined by Interrupt Coalescing mechanism.
5	The host software reads MMCSD0_CQ_TASK_COMP_NOTIF register to determine which task(s) has(have) been completed. Each bit set in MMCSD0_CQ_TASK_COMP_NOTIF register represents by index which task has completed but hasn't yet been served by software.
6	For every task completed clear the appropriate MMCSD0_CQ_TASK_COMP_NOTIF register bit.
7	Repeat steps 1-6 for the pending tasks.

12.3.5.5.2.4.4 Task Discard and Clear Sequence

Figure 12-275 and Table 12-324 show a task discard and clear sequence.

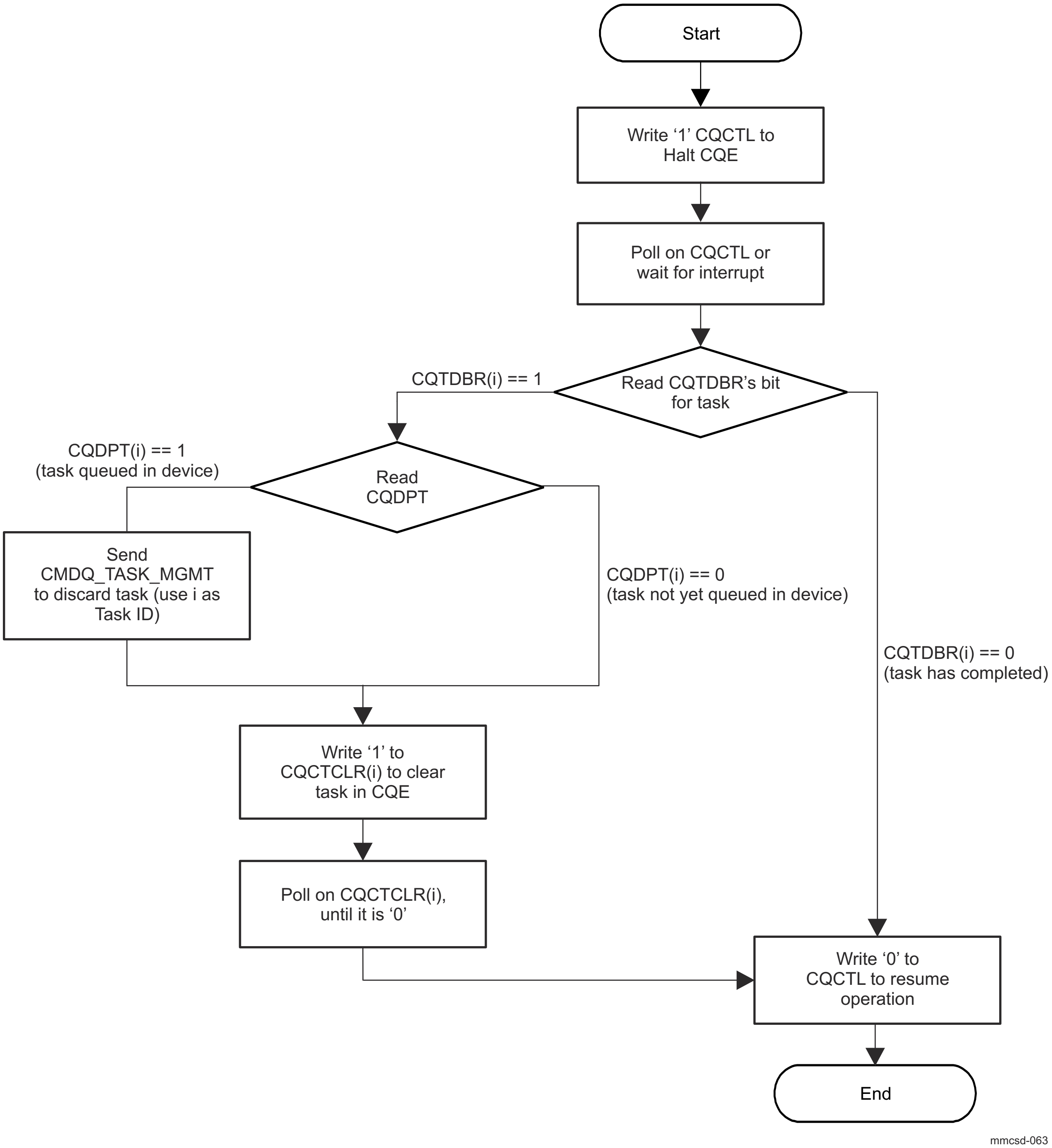

Figure 12-275. Task Discard and Clear Sequence

Table 12-336. Task Discard and Clear Sequence

Step	Description
1	While CQE is enabled write '1' to MMCSD0_CQ_CONTROL[0] HALT_BIT bit to halt CQE.
2	Poll on MMCSD0_CQ_INTR_STS[0] HALT_COMPLETE bit.
3	Read MMCSD0_CQ_TASK_DOOR_BELL register to determine if the task to be dicarded is set to 1.
4	Read MMCSD0_CQ_DEV_PENDING_TASKS register to check if the task is queued in the device.
5	Send CMDQ_TASK_MGMT(CMD48) to discard task using the task id as the argument.
6	Write '1' to CQCTCLR[i] to clear task in CQE.

Table 12-336. Task Discard and Clear Sequence (continued)

Step	Description
7	Poll on CQCTCLR[i] until it is '0'.
8	Write '0' to MMCSD0_CQ_CONTROL register to resume CQE.

12.3.5.5.2.4.5 Error Detect and Recovery when CQ is enabled

Figure 12-276 and Table 12-325 show an error detect and recovery sequence.

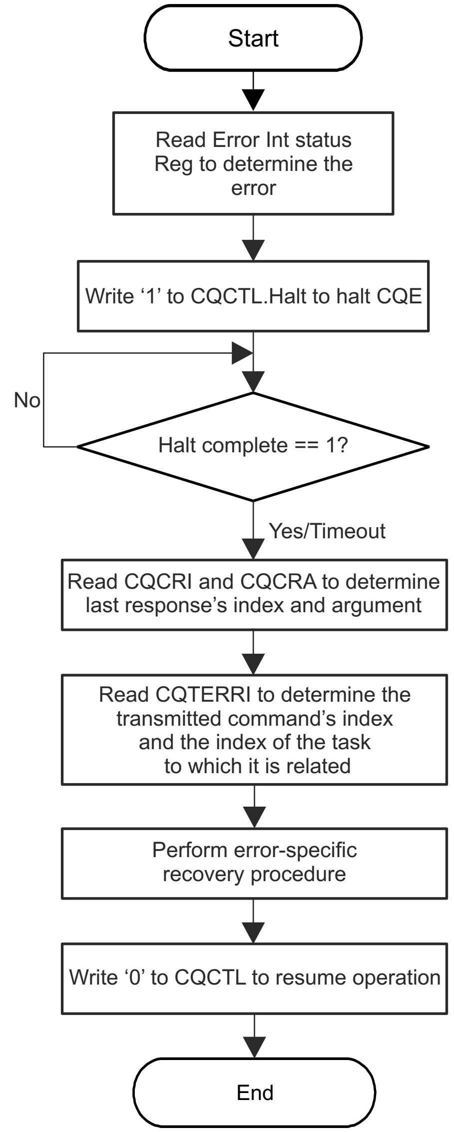

Figure 12-276. Error Detect and Recovery Sequence

Table 12-337. Error Detect and Recovery Sequence

Step	Description
1	Read eMMC host controller MMCSD0_ERROR_INTR_STS register and determine error is related to CQE.
2	Write '1' to MMCSD0_CQ_CONTROL[0] HALT_BIT bit to halt CQE.
3	Wait for MMCSD0_CQ_CONTROL[0] HALT_BIT bit to read '1'. In some error cases, this may not happen, so software should proceed to the next step after a sufficient time-out.

Table 12-337. Error Detect and Recovery Sequence (continued)

Step	Description
4	Read MMCSD0_CQ_CMD_RESP_INDEX and MMCSD0_CQ_CMD_RESP_ARG registers to determine last response's index and argument.
5	Read MMCSD0_CQ_TASK_ERR_INFO register to determine the transmitted command's index and the index of the task to which it is related.
6	Perform error-specific recovery procedure.
7	Write '0' to MMCSD0_CQ_CONTROL register to resume operation.

12.4 Industrial and Control Interfaces

This section describes the industrial and control interfaces in the device.

12.4.1 Modular Controller Area Network (MCAN)

This section describes the Modular Controller Area Network (MCAN) modules in the device.

12.4.1.1 MCAN Overview

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control. CAN has high immunity to electrical interference. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The device supports 2 MCAN modules:

- 2 in the device MAIN domain

They connect to the physical layer of the CAN network through external (for the device) transceivers. Each MCAN module supports flexible bit rates greater than 1 Mbps and is compliant to ISO 11898-1:2015.

Table 12-326 shows MCAN allocation across device domains.

Table 12-338. MCAN Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
MCAN0	-	✓
MCAN1	-	✓

Figure 12-277 shows the MCAN modules overview.

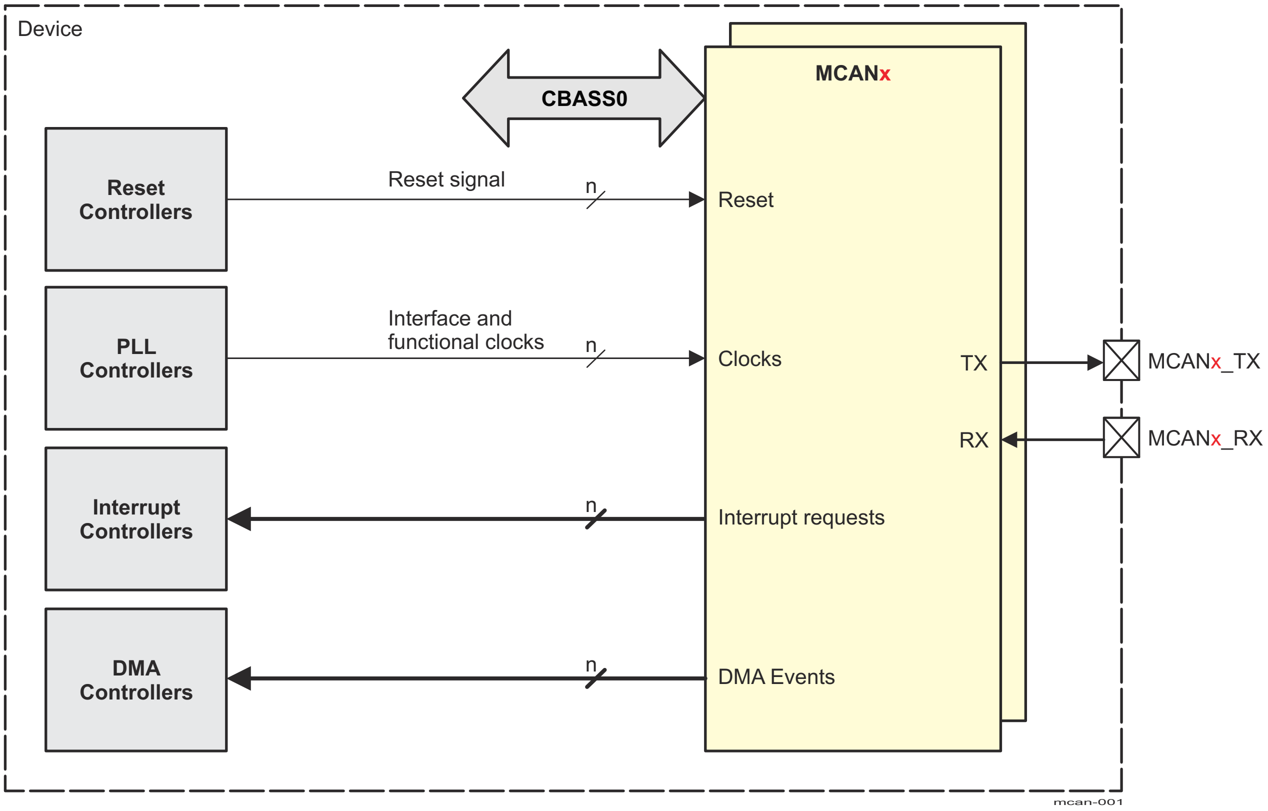

Note

x = 0 - 1

Figure 12-277. MCAN Modules Overview

12.4.1.1.1 MCAN Features

Each MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- SAE J1939 support
- AUTOSAR support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Internal Loopback mode for self-test
- Maskable interrupts, two interrupt lines
- Two clock domains (CAN clock/Host clock)
- Parity/ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Local power-down and wakeup support
- Timestamp Counter

12.4.1.1.2 MCAN Not Supported Features

- Host Bus Firewall
- GPIO Mode
- Clock Calibration
- External (IO) Loopback Mode
- Debug DMA (see Section 12.4.1.4.7.4)
- TX DMA Channels [31:3]

12.4.1.2 MCAN Environment

All module instances are hereinafter referred to as MCAN module.

This section describes the external MCAN connections (environment).

The CAN network physical layer consists of two-wire differential bus, usually twisted pair, and provides high level of interference immunity. An xternal CAN transceiver IC is needed to access a CAN bus by the MCAN.

Figure 12-278 shows the MCAN typical application.

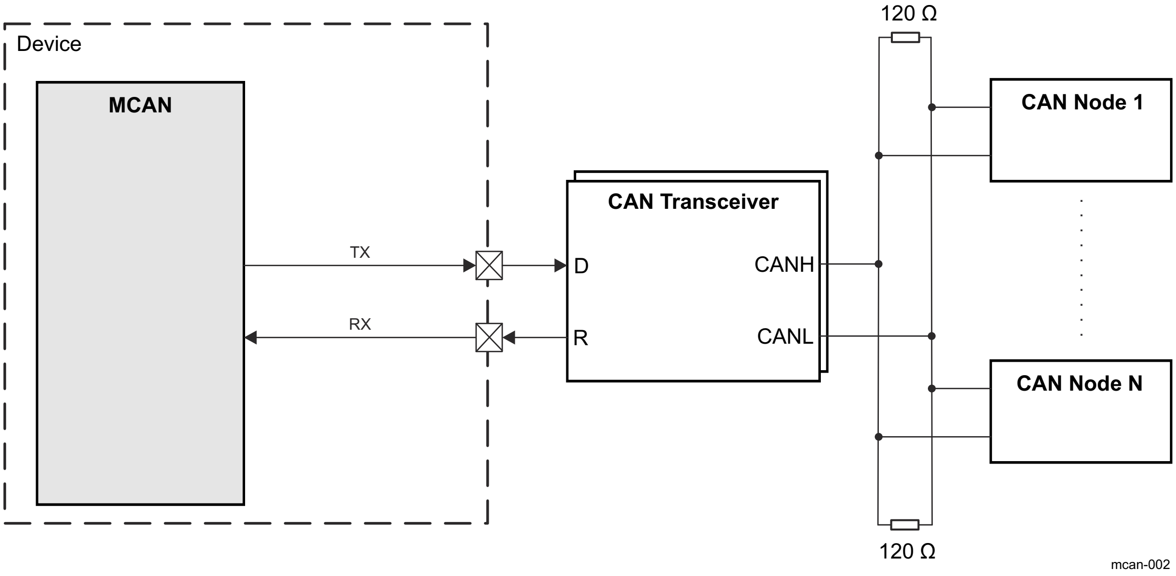

Figure 12-278. MCAN Typical Application

Table 12-327 describes the MCAN I/O signals.

Table 12-339. MCAN I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(1)
		MCAN[0-1]		
RX	MCAN0_RX	I	Serial data input from external CAN transceiver	HiZ
TX	MCAN0_TX	O	Serial data output to external CAN transceiver	1
RX	MCAN1_RX	I	Serial data input from external CAN transceiver	HiZ
TX	MCAN1_TX	O	Serial data output to external CAN transceiver	1

(1) I = Input; O = Output; HiZ = High Impedance

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Data sheet.

12.4.1.2.1 CAN Network Basics

- CAN bus is a 2-wire differential bus using Non-Return-to-Zero (NRZ) encoding and has two states:
  - Recessive state (logical 1)
  - Dominant state (logical 0)
- The network is multicontroller. When two or more nodes (ECUs) attempt to transmit at the same time, a non-destructive arbitration technique guarantees messages are sent in order of priority and no messages are lost.
- The message transmission is multicast. Data messages transmitted are identifier based, not address based.
- Content of message is labeled by the identifier that is unique throughout the network (for example: rpm, temperature, position, pressure, and so forth).
- All nodes on network receive the message and each performs an acceptance test on the identifier. If message is relevant, it is processed, otherwise it is ignored.
- The unique identifier also determines the priority of the message (the lower the numerical value of the identifier, the higher the priority is).
- Data is transmitted and received using message frames, consisting of the following basic fields:
  - Arbitration field
  - Control field
  - Data field (up to 8 bytes for Classical CAN and up to 64 bytes for CAN FD)
  - CRC field
  - ACK field

For more information, see *ISO 11898-1:2015: CAN data link layer and physical signaling*.

12.4.1.3 MCAN Integration

This section describes the MCAN integration in the device, including information about clocks, resets, and hardware requests.

12.4.1.3.1 MCAN Integration in MAIN Domain

There are two MCAN modules integrated in the device MAIN domain - MCAN[0-1].

Figure 12-279 shows the integration of MCAN[0-1].

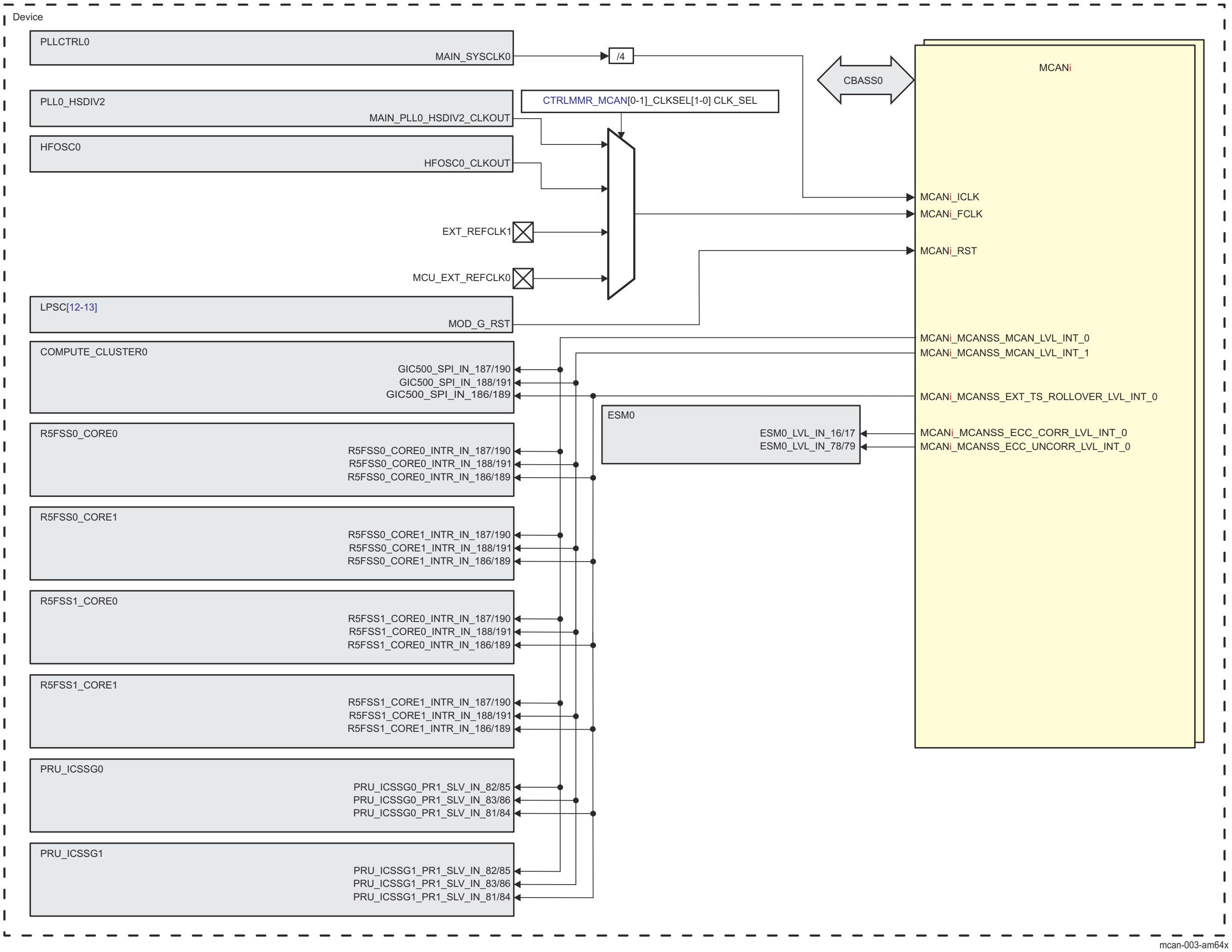

Note

i = 0 - 1

Figure 12-279. MCAN[0-1] Integration

Table 12-328 through Table 12-331 summarize the integration of MCAN[0-1] in the device MAIN domain.

Table 12-340. MCAN Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCAN0	PSC0	PD0	LPSC12	CBASS0
MCAN1	PSC0	PD0	LPSC13	CBASS0

Table 12-341. MCAN Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCAN0	MCAN0_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	Interface Clock

Table 12-341. MCAN Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
	MCAN0_FCLK	MAIN_PLL0_HSDIV2_CLKOUT (default)	PLL0_HSDIV2	Functional Clock (for more information about clock multiplexing, see MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL[1-0] CLK_SEL bit field in Section 5.1 , *Control Module (CTRL_MMR)*. Default: MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL[1-0] CLK_SEL = 0h, MAIN_PLL0_HSDIV2_CLKOUT is selected)
		EXT_REFCLK1	I/O pin	
		MCU_EXT_REFCLK0	I/O pin	
		HFOSC0_CLKOUT	HFOSC0	
MCAN1	MCAN1_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	Interface Clock
	MCAN1_FCLK	MAIN_PLL0_HSDIV2_CLKOUT (default)	PLL0_HSDIV2	Functional Clock (for more information about clock multiplexing, see MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL[1-0] CLK_SEL bit field in Section 5.1 , *Control Module (CTRL_MMR)*. Default: MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL[1-0] CLK_SEL = 0h, MAIN_PLL0_HSDIV2_CLKOUT is selected)
		EXT_REFCLK1	I/O pin	
		MCU_EXT_REFCLK0	I/O pin	
		HFOSC0_CLKOUT	HFOSC0	

Table 12-342. MCAN Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCAN0	MCAN0_RST	MOD_G_RST	LPSC12	Asynchronous Module Reset
MCAN1	MCAN1_RST	MOD_G_RST	LPSC13	Asynchronous Module Reset

Table 12-343. MCAN Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN0	MCAN0_MCANSS_MCAN_LVL_INT_0	GICSS0_SPI_IN_187	GICSS0	MCAN0 Line 0 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_187	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_187	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_187	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_187	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_82	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_82	PRU_ICSSG1		
	MCAN0_MCANSS_MCAN_LVL_INT_1	GICSS0_SPI_IN_188	GICSS0	MCAN0 Line 1 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_188	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_188	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_188	R5FSS1_CORE0		

Table 12-343. MCAN Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		R5FSS1_CORE1_INTR_IN_188	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_83	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_83	PRU_ICSSG1		
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_0	GICSS0_SPI_IN_186	GICSS0	MCAN0 External TimeStamp Counter Rollover Interrupt	Level
		R5FSS0_CORE0_INTR_IN_186	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_186	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_186	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_186	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_81	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_81	PRU_ICSSG1		
	MCAN0_MCANSS_ECC_CORR_LVL_INT_0	ESM0_LVL_IN_16	ESM0	MCAN0 ECC Correctable Error Interrupt Request	Level
	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_0	ESM0_LVL_IN_78	ESM0	MCAN0 ECC Uncorrectable Error Interrupt Request	Level
MCAN1	MCAN1_MCANSS_MCAN_LVL_INT_0	GICSS0_SPI_IN_190	GICSS0	MCAN1 Line 0 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_190	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_190	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_190	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_190	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_85	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_85	PRU_ICSSG1		
	MCAN1_MCANSS_MCAN_LVL_INT_1	GICSS0_SPI_IN_191	GICSS0	MCAN1 Line 1 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_191	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_191	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_191	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_191	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_86	PRU_ICSSG0		

Table 12-343. MCAN Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		PRU_ICSSG1_PR1_SLV_IN_86	PRU_ICSSG1		
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_0	GICSS0_SPI_IN_189	GICSS0	MCAN1 External TimeStamp Counter Rollover Interrupt	Level
		R5FSS0_CORE0_INTR_IN_189	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_189	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_189	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_189	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_84	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_84	PRU_ICSSG1		
	MCAN1_MCANSS_ECC_CORR_LVL_INT_0	ESM0_LVL_IN_17	ESM0	MCAN1 ECC Correctable Error Interrupt Request	Level
	MCAN1_MCANSS_ECC_UNCORR_LVL_INT_0	ESM0_LVL_IN_79	ESM0	MCAN1 ECC Uncorrectable Error Interrupt Request	Level

Note

For a description of the interrupt source, see Section 12.4.1.4.2 , *Interrupt and DMA Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

For more information on the device DMA controllers, see Section 11.1 , *Data Movement Architecture (DMA)*.

12.4.1.4 MCAN Functional Description

The MCAN module performs CAN protocol communication according to ISO 11898-1:2015. The bit rate can be programmed to values greater than 1 Mbps. Additional transceiver hardware is required for the connection to the physical layer (CAN bus).

For communication on a CAN network, individual message frames can be configured. The message frames and identifier masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the Message Handler.

The register set of the MCAN module can be accessed directly via the module interface. These registers are used to control and configure the CAN core and the Message Handler, and to access the Message RAM.

Figure 12-280 shows the MCAN module block diagram.

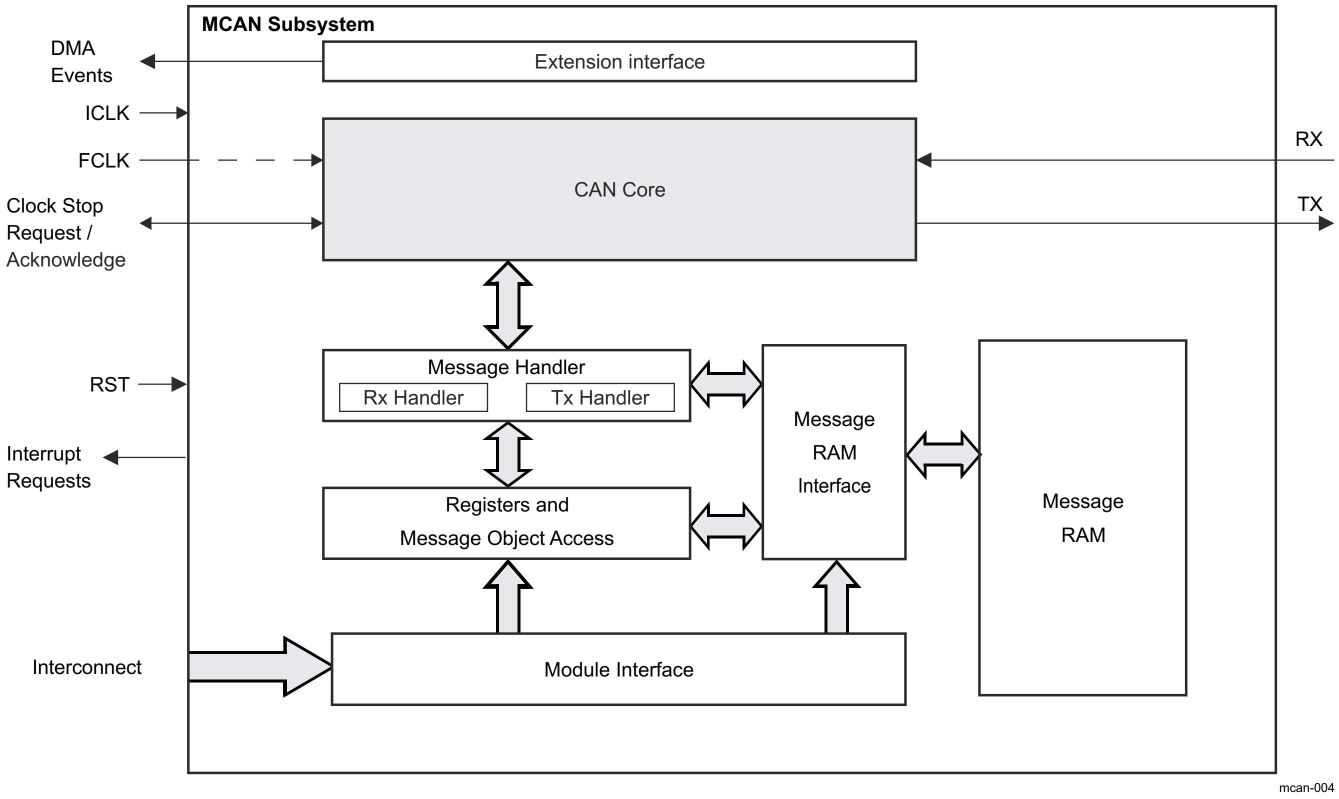

Figure 12-280. MCAN Block Diagram

The MCAN module blocks description:

- **CAN Core**: the CAN core consists of the CAN protocol controller and the Rx/Tx shift register. It handles all ISO 11898-1:2015 protocol functions and supports 11-bit and 29-bit identifiers.
- **Message Handler**: the Message Handler (Rx Handler and Tx Handler) is a state machine that controls the data transfer between the single-ported Message RAM and the CAN core's Rx/Tx shift register. It also handles the acceptance filtering and the Interrupt/DMA request generation as programmed in the control registers.
- **Message RAM**: the main purpose of the Message RAM is to store Rx/Tx messages, Tx Event elements, and Message ID Filter elements (for more information, see Section 12.4.1.4.10 , *Message RAM*).
- **Message RAM Interface**: enables connection between the Message RAM and the other blocks in the MCAN module.
- **Registers and Message Object Access**: data consistency is ensured by indirect accesses to the message objects. The interface registers have the same word-length as the Message RAM.

- **Module Interface**: provides connection to the Registers and Message Object Access block and Message RAM Interface block
- **Clocking**: two clocks are provided to the MCAN module: the peripheral synchronous clock (interface clock ICLK) and the peripheral asynchronous clock (functional clock - FCLK).
- **Extension Interface**: this interface is used for DMA requests signaling (see Section 12.4.1.4.2.2).

12.4.1.4.1 Module Clocking Requirements

Two clocks are provided to the MCAN module:

- the peripheral synchronous clock (ICLK) as the general module clock source
- and the peripheral asynchronous clock (FCLK) provided to the CAN core for generating the CAN bit timing.

Within the MCAN module there is a synchronization mechanism implemented to ensure safe data transfer between the two clock domains. There is synchronization between the signals from the Host clock domain to the CAN clock domain and vice versa and between the reset signal to the Host clock domain and to the CAN clock domain.

Note

ICLK must always be higher or equal to FCLK, in order to achieve a stable functionality of the MCAN module. Here, also the frequency shift of the modulated ICLK has to be considered:

$f_{0,\mathrm{ICLK}} \pm \Delta f_{\mathrm{FM,ICLK}} \geq f_{\mathrm{FCLK}}$

For more information on how to configure the relevant clock source registers, see Section 5.4 , *Clocking* and the device-specific Data sheet.

12.4.1.4.2 Interrupt and DMA Requests

The MCAN module provides interrupt and DMA requests. They are configured via the Host CPU. The Suspend Mode is requesting or forcing (based on MCANSS_CTRL[3] DBGSUSP_FREE bit) the MCAN module to go into initialization mode (see MCAN_CCCR[0] INIT bit) in which new interrupts and DMA requests will not be issued, that is to prevents the interrupt and DMA requests from propagating to the Host CPU (for more information, see Section 12.4.1.4.3.8.2 , *Suspend Mode*).

12.4.1.4.2.1 Interrupt Requests

The MCAN module has two interrupt lines. There are 30 internal interrupt sources. Each source can be configured to drive one of the two interrupt lines. The interrupts are 'level high' interrupts.

The MCAN core provides two interrupt requests (for Line 0 and Line 1).

For more information, see the following registers:

- Interrupt Register (MCAN_IR)
- Interrupt Enable (MCAN_IE)
- Interrupt Line Select (MCAN_ILS)
- Interrupt Line Enable (MCAN_ILE)

The MCAN module is capable of issuing ECC interrupts. After clearing the ECC interrupt source, the application software must also write 1 to EOI register (MCANSS_ECC_SEC_EOI_REG/MCANSS_ECC_DED_EOI_REG). For more information, see *ECC Aggregator*.

The MCAN module supports External Timestamp Counter. When the External Timestamp Counter rolls over it produces an interrupt (see *External Timestamp Counter*).

For more information, see the following registers:

- Interrupt Clear Shadow Register (MCANSS_ICS)
- Interrupt Raw Status Register (MCANSS_IRS)
- Interrupt Enable Clear Shadow Register (MCANSS_IECS)
- Interrupt Enable Register (MCANSS_IE)

- Interrupt Enable Status Register (MCANSS_IES)
- End Of Interrupt Register (MCANSS_EOI)
- External Timestamp Prescaler Register (MCANSS_EXT_TS_PRESCALER)
- External Timestamp Unserviced Interrupts Counter Register (MCANSS_EXT_TS_UNSERVICED_INTR_CNTR)

12.4.1.4.2.2 DMA Requests

Functional transmit and Filter DMA requests are generated by the MCAN module based on the signaling in the Extension Interface. The DMA signaling uses a simple DMA request active high pulse.

The active high pulse indicates a pending message is transmitted (see MCAN_TXBRP). This pulse can be used to transfer another message to the Tx Buffer, which would need to be followed by writing 1 to the corresponding MCAN_TXBAR[0] AR bit to mark a new Tx message pending transmission.

The Parity on Tx DMA Events is available using an EDC Controller which can be accessed through the ECC Aggregator.

Standard and Extended message filters can be set to issue a pulse when a filter match occurs. These 'Filter Events' can be used to DMA messages from the Rx FIFO. The events are high level single clock cycle pulses (ICLK).

12.4.1.4.3 Operating Modes

12.4.1.4.3.1 Software Initialization

Setting the MCAN_CCCR[0] INIT bit to 1 starts a software initialization. This is done either by software or by a hardware reset, when an uncorrected bit error was detected in the Message RAM, or by going Bus_Off state. While the MCAN_CCCR[0] INIT bit is set, the message transfer is stopped and the status of the output TX pin is recessive (high). The counters of the Error Management Logic (EML) are unchanged. Setting the MCAN_CCCR[0] INIT bit does not change any configuration register. Resetting the MCAN_CCCR[0] INIT bit finishes the software initialization. After waiting for the occurrence of a sequence of 11 consecutive recessive bits (indication for Bus_Idle state) the message transfer starts.

Access to the MCAN configuration registers is only enabled when both MCAN_CCCR[0] INIT and MCAN_CCCR[1] CCE bits are set (write protection).

The MCAN_CCCR[1] CCE bit can only be set/reset while the MCAN_CCCR[0] INIT = 1. The MCAN_CCCR[1] CCE bit is automatically reset when the MCAN_CCCR[0] INIT bit is reset.

The following registers are reset when the MCAN_CCCR[1] CCE bit is set:

- MCAN_HPMS - High Priority Message Status
- MCAN_RXF0S - Rx FIFO 0 Status
- MCAN_RXF1S - Rx FIFO 1 Status
- MCAN_TXFQS - Tx FIFO/Queue Status
- MCAN_TXBRP - Tx Buffer Request Pending
- MCAN_TXBTO - Tx Buffer Transmission Occurred
- MCAN_TXBCF - Tx Buffer Cancellation Finished
- MCAN_TXEFS - Tx Event FIFO Status

The Timeout Counter value MCAN_TOCV[15-0] TOC field is preset to the value configured by the MCAN_TOCC[31-16] TOP field when the MCAN_CCCR[1] CCE bit is set.

In addition the Tx Handler and Rx Handler are held in idle state while MCAN_CCCR[1] CCE = 1.

The following registers are only writeable while MCAN_CCCR[1] CCE = 0

- MCAN_TXBAR - Tx Buffer Add Request
- MCAN_TXBCR - Tx Buffer Cancellation Request

MCAN_CCCR[7] TEST and MCAN_CCCR[5] MON bits can only be set by the Host CPU while MCAN_CCCR[0] INIT = 1 and MCAN_CCCR[1] CCE = 1. Both bits may be reset at any time. The MCAN_CCCR[6] DAR bit can only be set/reset while MCAN_CCCR[0] INIT = 1
and MCAN_CCCR[1] CCE = 1.

Table 12-332 shows the steps to configure the MCAN module.

Table 12-344. Steps to Configure MCAN Module

Step	Operation	Description	Pseudo Code
1	Initialize MCAN_CCCR	Set MCAN_CCCR[0] INIT bit and check that it has been set	INIT = 1; If INIT ≠ 1, wait until it is
2	Unlock protected registers	Set MCAN_CCCR[1] CCE bit	CCE = 1;
3	Configure CAN mode	Set MCAN_CCCR[8] FDOE bit to CAN FD	FDOE = 1 for CAN FD FDOE = 0 for CAN
4	Configure Bit Rate Switching	Set MCAN_CCCR[9] BRSE bit	BRSE = 1 with bit rate switching BRSE = 0 without bit rate switching
5	Set bit timing	Set MCAN_NBTP register	
6	Lock protected registers	Clear MCAN_CCCR[1] CCE bit	CCE = 0;
7	Return MCAN module to normal operation	Clear MCAN_CCCR[0] INIT bit and check it has been cleared	INIT = 0; If INIT ≠ 0, wait until it is

12.4.1.4.3.2 Normal Operation

Once the MCAN module is initialized and the MCAN_CCCR[0] INIT bit is reset to zero, the MCAN module synchronizes itself to the CAN bus and is ready for communication. After passing the acceptance filtering, received messages including Message Identifier (ID) and Data Length Code (DLC) are stored into a dedicated Rx Buffer or into Rx FIFO 0/Rx FIFO 1.

For messages to be transmitted dedicated Tx Buffers and/or a Tx FIFO or a Tx Queue can be initialized or updated.

Note

Automated transmission on reception of remote frames is not supported.

12.4.1.4.3.3 CAN FD Operation

The CAN FD standard allows extended frames to be sent, up to 64 data bytes in a single frame at a higher bit rate for the data phase of a frame, up to 8 Mbps. The CAN FD standard introduces the ability to switch from one bit rate to another. Extended Data Length (EDL), as shown in Figure 12-281, sets a data length of up to 8 or up to 64 data bytes. Bit Rate Switching (BRS) indicates whether two bit rates (the data phase is transmitted at a different bit rate to the arbitration phase) are enabled.

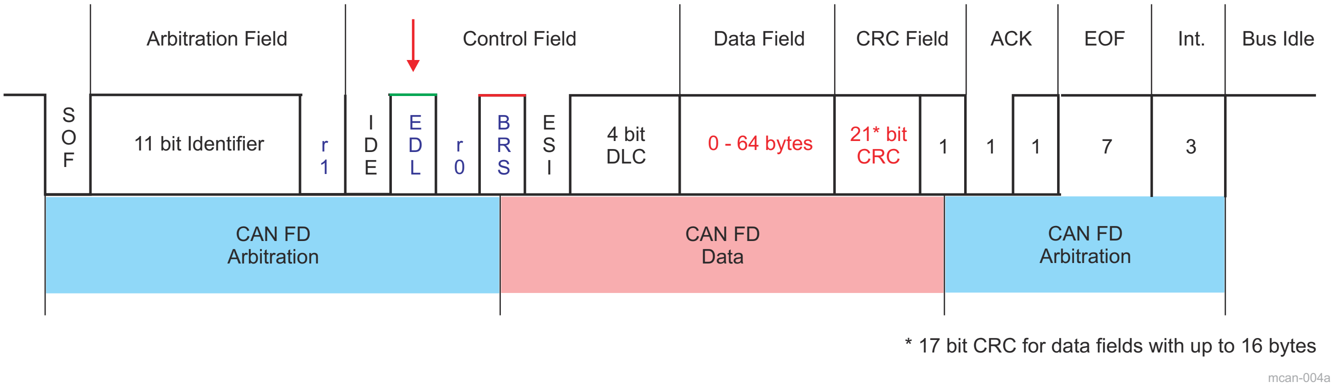

Figure 12-281. CAN FD Frame

Note

Figure 12-281 presents CAN FD frame according to the Non-ISO CAN FD (legacy) protocol. In the new ISO CAN FD protocol the CRC Field includes additional 5 bits (three stuff bit counter (SBC) bits and two parity bits). With these additional bits, a weakness identified in the error detection scheme chosen by the original protocol is removed. By setting MCAN_CCCR[15] NISO bit, the ISO or Non-ISO CAN FD format can be chosen. In CAN network ISO CAN FD and non-ISO CAN FD devices should never mix.

There are two variants of CAN FD frame transmission:

- CAN FD frame transmission without bit rate switching
- CAN FD frame transmission where control field, data field, and CRC field are transmitted with a higher bit rate than the beginning and the end of the frame

In the CAN frames FDF = recessive (logical 1) signifies a CAN FD frame, FDF = dominant (logical 0) signifies a Classic CAN frame. In a CAN FD frame, the two bits following FDF - res and BRS, decide whether the bit rate inside of this CAN FD frame is switched. A CAN FD bit rate switch is signified by res = dominant and BRS = recessive. Note that the coding of res = recessive is reserved for future expansion of the protocol. In case the MCAN module receives a frame with FDF = recessive and res = recessive, it will signal a Protocol Exception Event by setting the MCAN_PSR[14] EXE bit. When Protocol Exception Handling is enabled (MCAN_CCCR[12] PXHD = 0), this causes the operation state to change from Receiver (MCAN_PSR[4-3] ACT = 10) to Integrating (MCAN_PSR[4-3] ACT = 00) at the next sample point. In case Protocol Exception Handling is disabled (MCAN_CCCR[12] PXHD = 1), the MCAN will treat a recessive res bit as an form error and will respond with an error frame.

CAN FD operation is enabled by programming the MCAN_CCCR[8] FDOE bit. In case MCAN_CCCR[8] FDOE = 1, transmission and reception of CAN FD frames is enabled. Transmission and reception of Classic CAN frames is always possible. Whether a CAN FD frame or a Classic CAN frame is transmitted can be configured via the FDF bit in the respective Tx Buffer element.

With MCAN_CCCR[8] FDOE = 0, received frames are interpreted as Classic CAN frames, which leads to the transmission of an error frame when receiving a CAN FD frame. When CAN FD operation is disabled, no CAN FD frames are transmitted even if the FDF bit of a Tx Buffer element is set. The MCAN_CCCR[8] FDOE and MCAN_CCCR[9] BRSE bits can only be changed while the MCAN_CCCR[0] INIT and MCAN_CCCR[1] CCE bits are both set. With MCAN_CCCR[8] FDOE = 0, the setting of bits FDF and BRS is ignored and frames are transmitted in Classic CAN format.

With MCAN_CCCR[8] FDOE = 1 and MCAN_CCCR[9] BRSE = 0, only FDF bit of a Tx Buffer element is evaluated. With MCAN_CCCR[8] FDOE = 1 and MCAN_CCCR[9] BRSE = 1, transmission of CAN FD frames with bit rate switching is enabled. All Tx Buffer elements with bits FDF and BRS set are transmitted in CAN FD format with bit rate switching.

A mode change during CAN operation is only recommended under the following conditions:

- The failure rate in the CAN FD data phase is significant higher than in the CAN FD arbitration phase. In this case disable the CAN FD bit rate switching option for transmissions.
- During system startup all nodes are transmitting Classic CAN messages until it is verified that they are able to communicate in CAN FD format. If this is true, all nodes switch to CAN FD operation.
- Wakeup messages in CAN Partial Networking have to be transmitted in Classic CAN format.
- End-of-line programming in case not all nodes are CAN FD capable. Non CAN FD nodes are held in Silent mode until programming has completed. Then all nodes switch back to Classic CAN communication.

In the CAN FD format, the DLC coding differs from the standard CAN format (see Table 12-333).

Table 12-345. DLC Coding

DLC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Number of Data Bytes in Standard CAN	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8
Number of Data Bytes in CAN FD	0	1	2	3	4	5	6	7	8	12	16	20	24	32	48	64

For CAN FD frames, the bit timing will be switched inside the frame after the BRS (Bit Rate Switch) bit in case this bit is recessive. In the CAN FD arbitration phase, before the BRS bit, the nominal CAN bit timing (see Figure 12-282) is used as configured by the Nominal Bit Timing and Prescaler Register MCAN_NBTP. In the following CAN FD data phase, the data phase bit timing is used as configured by the Data Bit Timing and Prescaler Register MCAN_DBTP. The bit timing is switched back from the data phase timing at the CRC delimiter or when an error is detected, whichever occurs first.

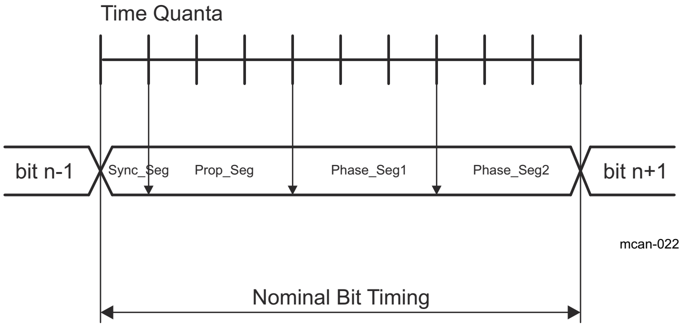

Figure 12-282. CAN Bit Timing

The maximum configurable data phase bit timing depends on the CAN clock frequency (FCLK). Example: with FCLK = 20 MHz and the shortest configurable bit time of 4 t_q (time quanta), the bit rate in the data phase is 5 Mbps.

In both data frame formats, CAN FD and CAN FD with bit rate switching, the value of the ESI (Error Status Indicator) bit depends on transmitter's error state (see MCAN_PSR[11] RESI bit) monitored at the start of the transmission. If the transmitter has error passive flag the ESI bit is transmitted recessive, else it is transmitted dominant.

The calculation of the parameters required for CAN bit timing configuration is dependent on a few fundamental equations. The bit rate (bits per second) calculation is based on the speed of the CAN clock, the bit rate pre-scalar value (BRP), and the time segments used to define the sampling point for the bit. The sampling point is the point of time at which the bus level is read and interpreted as the value at that respective time. The typical value of the sampling point is between 75-90%. Time segment 1 (TSEG1) is the time before the sampling point and is defined as the Prog_Seg time plus the Phase_Seg1 time per the CAN Bit Timing diagram. Time segment 2 (TSEG2) is the time after the sampling point which makes it equal to Phase_Seg2. When necessary, the Sync_Seg period of the nominal bit timing interval should be reflected in the equations by adding '1'.

$$TSEG1 = \mathrm{Prop\_Seg} + \mathrm{Phase\_Seg1} \tag{2}$$

$$TSEG2 = \mathrm{Phase\_Seg2} \tag{3}$$

$$Sampling\ Point\ (\%) = \frac{1 + \mathrm{TSEG1}}{1 + \mathrm{TSEG1} + \mathrm{TSEG2}} \tag{4}$$

$$Bit\ rate\left(bits\ per\ second\right) = \frac{\frac{\text{CAN clock speed in Hz}}{BRP}}{1 + \mathrm{TSEG1} + \mathrm{TSEG2}} \tag{5}$$

12.4.1.4.3.4 Transmitter Delay Compensation

12.4.1.4.3.4.1 Description

When only one CAN FD node is transmitting and all others are receivers the length of the bus line has no impact. When transmitting via the TX pin the MCAN module receives the transmitted data from its local CAN transceiver via the RX pin. The received data is delayed. If the transmitter delay is greater than TSEG1 (time segment before sample point), a bit error is detected.

The MCAN module provides a delay compensation mechanism to compensate the transmitter delay. The compensation mechanism enables transmission with higher bit rates during the CAN FD data phase independent of the delay of a specific CAN transceiver. Without transmitter delay compensation the bit rate in the data phase is limited by the transmitter delay.

The mechanism enables configurations where the data bit time is shorter than the transmitter delay (it is described in detail in ISO 11898-1:2015). The transmitter delay compensation is enabled by setting the MCAN_DBTP[23] TDC bit to 1.

The delayed transmit data is compared against the received data at the Secondary Sample Point (SSP) in order to check for bit errors during the data phase of transmitting nodes. If a bit error is detected, the transmitter will react on this bit error at the next following regular sample point. During arbitration phase the delay compensation is always disabled.

The received bit is compared against the transmitted bit at the SSP. The SSP position is defined as the sum of the measured delay from the MCAN's transmit output TX pin through the transceiver to the receive input RX pin plus the transmitter delay compensation offset configured by the MCAN_TDCR[14-8] TDCO field (see Figure 12-283). The transmitter delay compensation offset is used to adjust the position of the SSP inside the received bit (example: half of the bit time in the data phase). The position of the SSP is rounded down to the next integer number of mtq.

The actual transmitter delay compensation value can be checked by reading the MCAN_PSR[22-16] TDCV field. This field is cleared when the MCAN_CCCR[0] INIT bit is set and is updated at each transmission of CAN FD frame while the MCAN_DBTP[23] TDC bit is set.

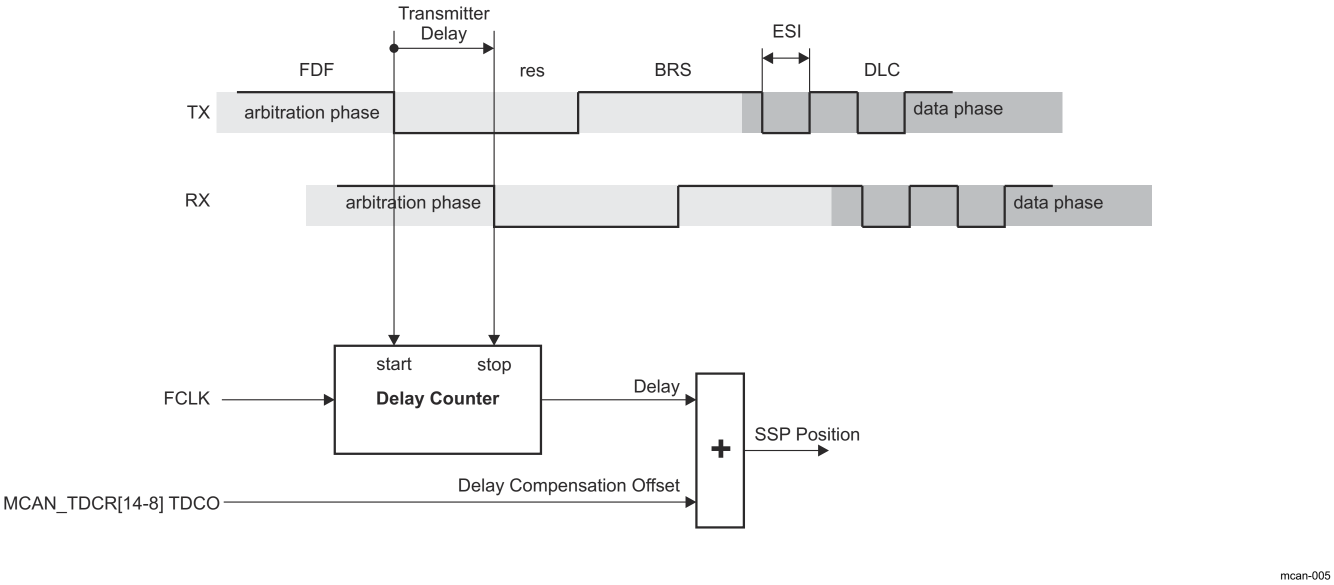

Figure 12-283. Transmitter Delay Measurement

12.4.1.4.3.4.2 Transmitter Delay Compensation Measurement

When transmitter delay compensation is enabled (by programming MCAN_DBTP[23] TDC = 1), the measurement is started within each transmitted CAN FD frame at the falling edge of FDF bit to bit res. The measurement is stopped when this edge is seen at the receive input RX pin of the transmitter. The resolution of this measurement is one mtq (see Figure 12-283). The mtq (minimum time quantum) dimension is equal to the CAN clock period (FCLK).

The use of a transmitter delay compensation filter window can be enabled by programming MCAN_TDCR[6-0] TDCF field. This filter feature defines a minimum value for the SSP position to avoid the case in which a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in an early taken SSP position. Dominant edges on the RX pin, that would result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least MCAN_TDCR[6-0] TDCF field and the RX pin is low.

The following boundary conditions have to be considered:

- The sum of the measured delay from the TX pin to the RX pin and the configured transmitter delay compensation offset (MCAN_TDCR[14-8] TDCO field) has to be less than 6 bit times in the data phase.
- The sum of the measured delay from the TX pin to the RX pin and the configured transmitter delay compensation offset (MCAN_TDCR[14-8] TDCO) field has to be less or equal 127 mtq. In case this sum exceeds 127 mtq, the maximum value of 127 mtq is used for transmitter delay compensation.
- The data phase ends at the sample point of the CRC delimiter, that stops checking of receive bits at the SSPs.

12.4.1.4.3.5 Restricted Operation Mode

In Restricted Operation Mode the CAN node is able to receive data and remote frames and acknowledge valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The receive and transmit error counters (MCAN_ECR[14-8] REC and MCAN_ECR[7-0] TEC) are frozen, while CAN error logging (MCAN_ECR[23-16] CEL) is active. The Host CPU can set the MCAN module into Restricted Operation Mode by setting MCAN_CCCR[2] ASM bit. The bit can only be set by the Host CPU at any time when both MCAN_CCCR[2] CCE and MCAN_CCCR[0] INIT bits are set to 1.

The Restricted Operation Mode is automatically entered when the Tx Handler does not read data from the Message RAM in time. To leave Restricted Operation Mode, the Host CPU has to reset MCAN_CCCR[2] ASM bit. This mode can be used in applications that adapt themselves to different CAN bit rates. In this case the application tests different bit rates and leaves the Restricted Operation Mode after it has received a valid frame.

Note

Restricted Operation Mode must not be combined with Internal Loopback Mode.

12.4.1.4.3.6 Bus Monitoring Mode

Entering Bus Monitoring Mode is done by setting the MCAN_CCCR[5] MON bit to 1. In this mode (see ISO 11898-1:2015, *Bus Monitoring* section), the MCAN module is able to receive valid data and remote frames, but cannot start a transmission. The MCAN module sends only recessive bits on the CAN bus. If the MCAN module is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the MCAN module monitors this dominant bit, although the CAN bus may remain in recessive state. In Bus Monitoring Mode the MCAN_TXBRP register is held in reset state. The Bus Monitoring Mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits. Figure 12-284 shows the connection of the TX and RX signals to the MCAN module in Bus Monitoring Mode.

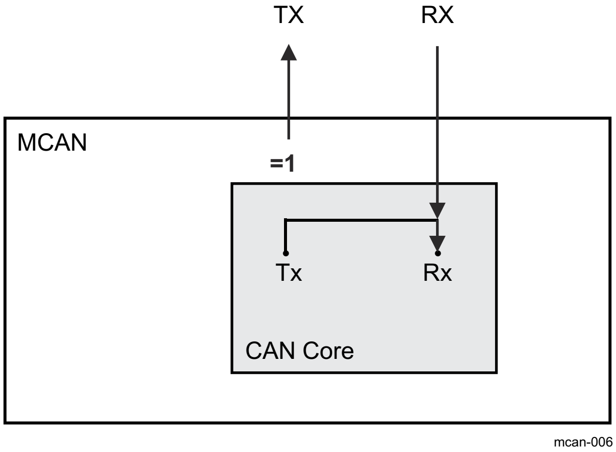

Figure 12-284. Connection of Signals in Bus Monitoring Mode

12.4.1.4.3.7 Disabled Automatic Retransmission (DAR) Mode

According to the CAN Specification (see ISO11898-1:2015, *Recovery Management* section), the MCAN module provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled (see the MCAN_CCCR[6] DAR bit).

12.4.1.4.3.7.1 Frame Transmission in DAR Mode

In DAR mode all transmissions are automatically cancelled after they started on the CAN bus. A Tx Buffer's Tx Request Pending MCAN_TXBRP[xx] TRPx bit is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

Successful transmission:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is set
- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is not set

Successful transmission in spite of cancellation:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is set
- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is set

Arbitration lost or frame transmission disturbed:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is not set
- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is set

In case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = 10 (transmission in spite of cancellation).

12.4.1.4.3.8 Power Down (Sleep Mode)

The entering in Power Down mode is controlled via two sources:

- PSC (via clock stop request signal)
- Software (by writing to the MCAN_CCCR[4] CSR bit)

As long as the clock stop request signal is active, the MCAN_CCCR[4] CSR bit is read as 1.

When all pending transmission requests have completed, the MCAN module waits until bus idle state is detected. Then the MCAN module sets the MCAN_CCCR[0] INIT bit to 1 to prevent any further CAN transfers.

The MCAN module acknowledges that it is ready for power down:

- By asserting clock stop acknowledge signal to the PSC (in case of PSC source).
- By setting the MCAN_CCCR[3] CSA flag bit to 1 (in case of Software source).

In this state, before the clocks are switched off, further register accesses can be made. Now the module clock inputs ICLK and FCLK may be switched off.

To leave power down mode, the application has to turn on the module clocks before resetting the input clock stop request signal respectively the MCAN_CCCR[4] CSR flag bit. The MCAN will acknowledge this by resetting the output clock stop acknowledge signal respectively the MCAN_CCCR[3] CSA flag bit. Afterwards, the application can restart CAN communication by resetting the MCAN_CCCR[0] INIT bit.

Restoring the clocks from clock stop mode, needs to be done according to how the clock stop was initiated:

- If Software asserts the MCAN_CCCR[3] CSA flag bit, once the MCAN module goes idle, the MCAN_CCCR[0] INIT bit is set. To get it started again, Software needs to write 0 to the MCAN_CCCR[0] INIT bit.
- If PSC is issuing a clock stop request, than there are two options for waking up:
    - After removing clock stop request signal, Software would need to write 0 to the MCAN_CCCR[0] INIT bit, or
    - If the MCANSS_CTRL[5] AUTOWAKEUP bit is set, than after removing clock stop request signal, an FSM inside the MCAN module will reset the MCAN_CCCR[0] INIT bit (without Software).

12.4.1.4.3.8.1 External Clock Stop Mode

The MCAN module supports two external clock stop modes:

- Immediate
- Graceful

In a graceful clock stop mode, when the clock stop request is asserted, the MCAN core will respond with clock stop acknowledge when all pending Tx messages have been processed and an Idle line had been detected. The MCAN_CCCR[0] INIT bit will be set, the MCAN core will go and stay Idle.

The automatic wakeup feature is enabled by setting the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits to 1 (for more information, see Section 12.4.1.4.3.8.3 , *Wakeup request*). When external clock stop request is removed and no suspend request is active, a read-modify-write to the MCAN_CCCR[0] INIT bit is performed to clear it.

12.4.1.4.3.8.2 Suspend Mode

The MCAN module supports two suspend modes:

- Immediate
- Graceful

In a graceful suspend mode (see the MCANSS_CTRL[3] DBGSUSP_FREE bit), when the suspend request is asserted, a clock stop request to the MCAN core is performed. The MCAN core will respond with clock stop acknowledge when all pending Tx messages have been processed and an Idle line had been detected. At that point the MCAN_CCCR[0] INIT bit will be set, the MCAN core will go and stay Idle. The suspend state can be verified by reading MCAN_CCCR[0] INIT bit.

The automatic wakeup feature is enabled by setting the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits to 1 (for more information, see Section 12.4.1.4.3.8.3 , *Wakeup request*). When suspend request is removed, if no external clock stop request is active, a read-modify-write to the MCAN_CCCR[0] INIT bit is performed to clear it.

During suspend mode the auto-clear feature is disabled. The following register fields have an auto-clear feature:

- MCAN_ECR[23-16] CEL
- MCAN_PSR[2-0] LEC
- MCAN_PSR[10-8] DLEC
- MCAN_PSR[11] RESI
- MCAN_PSR[12] RBRS
- MCAN_PSR[13] RFDF
- MCAN_PSR[14] PXE

12.4.1.4.3.8.3 Wakeup request

Issuing a clock stop request puts the MCAN module into Power Down mode (Sleep Mode). During transition from IDLE to ACTIVE, if the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits are enabled, after the MCAN Core respond to the removal of the clock stop request with removing the clock stop acknowledge, a read-modify-write will be issued to clear the MCAN_CCCR[0] INIT bit and the MCAN core will resume operation.

If the MCANSS_CTRL[4] WAKEUPREQEN bit is set, the MCAN module provides a wakeup request on the following wakeup event:

- The receive RX pin is dominant (logical 0)

The wakeup request is de-asserted when any of the following conditions occur:

- Clock stop request is removed and clock stop acknowledge is de-asserted
- A reset is applied to the MCAN module

12.4.1.4.3.9 Test Modes

The MCAN_TEST register write access is enabled by setting the test mode enable MCAN_CCCR[7] TEST bit to 1. The MCAN_TEST register allows the configuration of the test modes and test functions.

The CAN transmit TX pin has four output functions. One of those functions can be selected by programming the MCAN_TEST[6-5] TX field. Additionally to its default function (the serial data output) it can drive the CAN Sample Point signal to monitor the MCAN's bit timing and it can drive constant dominant or recessive values.

The actual value of the CAN receive RX pin can be monitored from MCAN_TEST[7] RX bit. Both functions can be used to check the CAN bus physical layer. Due to the synchronization mechanism between CAN clock (FCLK) and Host clock (ICLK) domain, there may be a delay of several Host clock periods between writing to the MCAN_TEST[6-5] TX field until the new configuration is visible at the output TX pin. This applies also when reading input RX pin via the MCAN_TEST[7] RX bit.

Note

Test modes should be used for self test only. The software control for TX pin interferes with all CAN protocol functions. It is not recommended to use test modes for application.

12.4.1.4.3.9.1 Internal Loopback Mode

The MCAN module can be set into Internal Loopback Mode by programming MCAN_TEST[4] LBCK and MCAN_CCCR[5] MON bits to 1. The Internal Loopback Mode is used for a 'Hot Selftest'. The 'Hot Selftest' allows the MCAN module to be tested without affecting a running CAN system connected to the TX and RX pins. In this mode RX pin is disconnected from the MCAN module and TX pin is held recessive. Figure 12-285 shows the connection of the TX and RX pins to the MCAN module in case of Internal Loopback Mode.

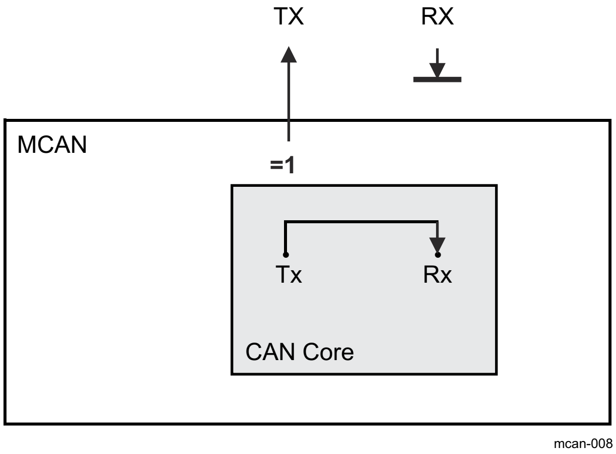

Figure 12-285. Internal Loopback Mode

12.4.1.4.4 Timestamp Generation

The MCAN module has integrated a 16-bit wrap-around counter for timestamp generation. The timestamp counter prescaler MCAN_TSCC[19-16] TCP field can be configured to clock the counter in multiples of CAN bit times (1-16). The counter is readable via the MCAN_TSCV[15-0] TSC field. A write access to the MCAN_TSCV register resets the counter to zero. When the timestamp counter wraps around the interrupt MCAN_IR[16] TSW flag is set. On start of a frame reception/transmission the counter value is captured and stored into the timestamp section of an Rx Buffer/Rx FIFO (RXTS[15-0]) or Tx Event FIFO (TXTS[15-0]) element. For more information, see Section 12.4.1.4.10 , *Message RAM*.

12.4.1.4.4.1 External Timestamp Counter

For CAN FD operation mode the MCAN core requires an External Timestamp Counter. An externally generated 16-bit vector may substitute the integrated 16-bit CAN bit time counter (internal timestamp counter) for receive and transmit timestamp generation. An external 16-bit timestamp counter can be used by programming the MCAN_TSCC[1-0] TSS field.

The External Timestamp Counter uses the interface clock (ICLK) as a reference clock. The MCAN Core accepts a 16-bit timestamp. A 24-bit prescaler provides a programmable resolution for the timestamp (see MCANSS_EXT_TS_PRESCALER[23-0] PRESCALER bit field). The External Timestamp Counter counter can be enabled or disabled through the MCANSS_CTRL[6] EXT_TS_CNTR_EN bit. When disabled the counter is reset back to zero. While enabled the counter keeps incrementing. When the timestamp rolls over the MCAN timestamp interrupt is generated.

When the timestamp rolls over the MCANSS_IRS register is set (see Figure 12-286). The MCANSS_IE register can be affected by writing to the MCANSS_IESS register to set or to the MCANSS_IECS register to clear. The MCANSS_IESS register is a shadow register mapped to the same address as the MCANSS_IE register. The level interrupt is a reflection of both MCANSS_IRS and MCANSS_IE being set. The MCANSS_IES register reflects the level interrupt. When an rollover event occurs the interrupt counter is incremented. Writing to the MCANSS_ICS register to clear the MCANSS_IRS register will also decrement the interrupt counter. Writing to the MCANSS_EOI register will issue another pulse if the interrupt counter is not zero.

The rollover event can be artificially simulated by software through writing to the Interrupt Set Shadow register (MCANSS_ISS). The MCANSS_ISS register is a shadow register mapped to the same address as the MCANSS_IRS register.

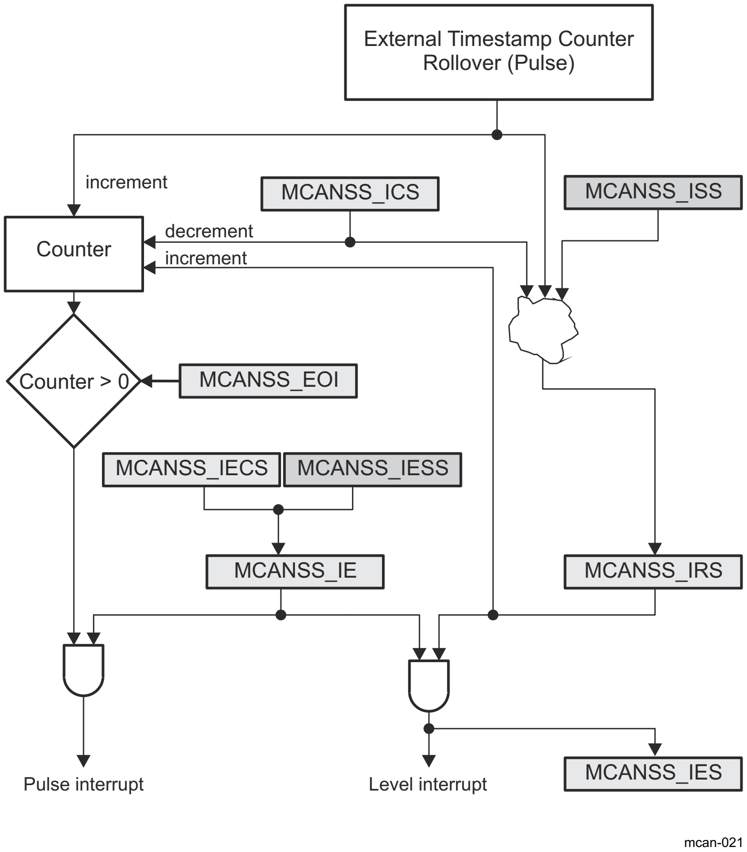

Figure 12-286. External Timestamp Counter Interrupt

12.4.1.4.5 Timeout Counter

The MCAN module has integrated a 16-bit Timeout Counter. It is used to signal timeout conditions for the Rx FIFO 0, Rx FIFO 1, and Tx Event FIFO Message RAM elements. The Timeout Counter is configured via the MCAN_TOCC register. It is enabled via the MCAN_TOCC[0] ETOC bit. The Timeout Counter operates as down-counter and uses the same prescaler programmed by the MCAN_TSCC[19-16] TCP field as the Timestamp Counter. The actual counter value can be monitored from the MCAN_TOCV[15-0] TOC field. The Timeout Counter can be started only when MCAN_CCCR[0] INIT = 0 and stopped when MCAN_CCCR[0] INIT = 1 (example: when the MCAN enters Bus_Off state). The operation mode is selected by the MCAN_TOCC[2-1] TOS field. When Continuous Mode is selected, the counter starts when MCAN_CCCR[0] INIT = 0, a write to the MCAN_TOCV register presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field and continues down-counting.

In case the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field. Down-counting is started when the first FIFO element is stored. Writing to the MCAN_TOCV register has no effect. When the counter reaches zero, the interrupt MCAN_IR[18] TOO flag is set.

In Continuous Mode, the counter is immediately restarted at the value configured by the MCAN_TOCC[31-16] TOP field.

12.4.1.4.6 ECC Support

The Message Memory is wrapped in an ECC wrapper providing SECDED parity functionality. The ECC wrapper is controlled by an ECC Aggregator.

12.4.1.4.6.1 ECC Wrapper

The ECC wrapper provides Single Error Correction (SEC) and Double Error Detection (DED) parity to the Message Memory content. It has side band signals for error notification. The ECC Wrapper implements an error injection test mode.

The error correction is done using a lazy write back. When an error is detected, it is noted in a FIFO Queue which waits for an access gap to write the data back and refresh the memory. If a transaction writes new data to the compromised entry before the lazy write back completes, the write back is discarded.

12.4.1.4.6.2 ECC Aggregator

Note

For more information about ECC Aggregator, refer to Section 12.6.4 , *ECC Aggregator*.

12.4.1.4.7 Rx Handling

The Rx Handler controls the following operations:

- Acceptance filtering
- The transfer of received messages to the Rx Buffers or to one of the two Rx FIFOs (Rx FIFO 0 or Rx FIFO 1)
- Rx FIFO Put and Get Index operations

12.4.1.4.7.1 Acceptance Filtering

The MCAN module is capable to configure two sets of acceptance filters - one set for standard and one set for extended identifiers. These filters can be assigned to an Rx Buffer or to one of the two Rx FIFOs.

The main features of the filter elements are:

- Each filter element can be configured as:
  - Range Filter (from - to)
  - Filter for specific IDs (for one or two dedicated IDs)
  - Classic Bit Mask Filter
- Each filter element can be enabled/disabled individually
- Each filter element can be configured for acceptance or rejection filtering
- Filters are checked sequentially and execution (acceptance filtering procedure) stops at the first matching filter element or when the end of the filter list is reached

Related configuration registers are:

- Global Filter Configuration (MCAN_GFC) register
- Standard ID Filter Configuration (MCAN_SIDFC) register
- Extended ID Filter Configuration (MCAN_XIDFC) register
- Extended ID AND Mask (MCAN_XIDAM) register

Depending on the configuration of the filter element (see SFEC/EFEC in Section 12.4.1.4.10 , *Message RAM*) if filter matches, one of the following actions is performed:

- Received frame is stored in FIFO 0 or FIFO 1
- Received frame is stored in Rx Buffer
- Received frame is stored in Rx Buffer and generation of pulse at filter event pin is performed. This is high level single ICLK pulse. For more information, see Section 12.4.1.4.2.1 , *DMA Requests*.
- Received frame is rejected
- Set High Priority Message interrupt flag MCAN_IR[8] HPM

- Set High Priority Message interrupt flag MCAN_IR[8] HPM and store received frame in FIFO 0 or FIFO 1

Acceptance filtering starts when complete Message ID is received. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If a filter element matches - the Rx Handler starts writing the received message data in portions of 32 bit to the matching Rx Buffer or Rx FIFO. If an error condition occurs (for example: CRC error), this message is rejected with the following impact on the affected Rx Buffer or Rx FIFO:

- Rx Buffer:
  New Data flag (MCAN_NDAT1/MCAN_NDAT2) of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data (for error type see MCAN_PSR[2-0] LEC respectively MCAN_PSR[10-8] DLEC fields).
- Rx FIFO:
  Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data (for error type see MCAN_PSR[2-0] LEC respectively MCAN_PSR[10-8] DLEC fields). If matching Rx FIFO is configured to operate in overwrite mode, the boundary conditions described in Section 12.4.1.4.7.2.2 have to be considered.

12.4.1.4.7.1.1 Range Filter

Each filter element can be configured to operate as Range Filter (Standard Filter Type SFT = 00/Extended Filter Type EFT = 00). The filter matches for all received message frames with IDs in the range from SFID1 to SFID2 (SFID2 ≥ SFID1) respectively in the range from EFID1 to EFID2 (EFID2 ≥ EFID1). For more information see Section 12.4.1.4.10.5 , *Standard Message ID Filter Element* and Section 12.4.1.4.10.6 , *Extended Message ID Filter Element*.

There are two options for range filtering of extended frames:

- Extended Filter Type EFT = 00: The Extended ID AND Mask (MCAN_XIDAM) is used for Range Filtering. The Message ID of received frames is ANDed with the Extended ID AND Mask (MCAN_XIDAM) before the range filter is applied.
- Extended Filter Type EFT = 11: The Extended ID AND Mask (MCAN_XIDAM) is not used for Range Filtering.

12.4.1.4.7.1.2 Filter for specific IDs

Each filter element can be configured to filter one or two dedicated Message IDs (Standard Filter Type SFT =01/ Extended Filter Type EFT =01). To filter only one specific Message ID, the filter element has to be configured with SFID1 = SFID2 respectively EFID1 = EFID2. For more information see Section 12.4.1.4.10.5 , *Standard Message ID Filter Element* and Section 12.4.1.4.10.6 , *Extended Message ID Filter Element*.

12.4.1.4.7.1.3 Classic Bit Mask Filter

Classic bit mask filtering can filter groups of Message IDs (Standard Filter Type SFT =10/Extended Filter Type EFT =10). This is done by masking single bits of a received Message ID. In this case SFID1/EFID1 element is used as Message ID filter, while SFID2/EFID2 element is used as filter mask.

A 0 bit at the filter mask (SFID2/EFID2) will mask out the corresponding bit position of the configured Message ID filter (SFID1/EFID1) and the value of the received Message ID at that bit position is not relevant for acceptance filtering. Only those bits of the received Message ID where the corresponding mask bits are 1 are relevant for acceptance filtering.

There are two interesting cases:

- All mask bits are 1: a match occurs only when the received Message ID and the configured Message ID filter are identical.
- All mask bits are 0: all Message IDs match.

12.4.1.4.7.1.4 Standard Message ID Filtering

The standard Message ID (11-bit ID) filtering flow is shown in Figure 12-287. Section 12.4.1.4.10.5 , *Standard Message ID Filter Element* describes the standard Message ID filter element.

The Remote Transmission Request (RTR) and Extended Identifier (XTD) bits of the received frames are compared against the list of configured filter elements. This is controlled by the following registers:

- Global Filter Configuration (MCAN_GFC) register
- Standard ID Filter Configuration (MCAN_SIDFC) register

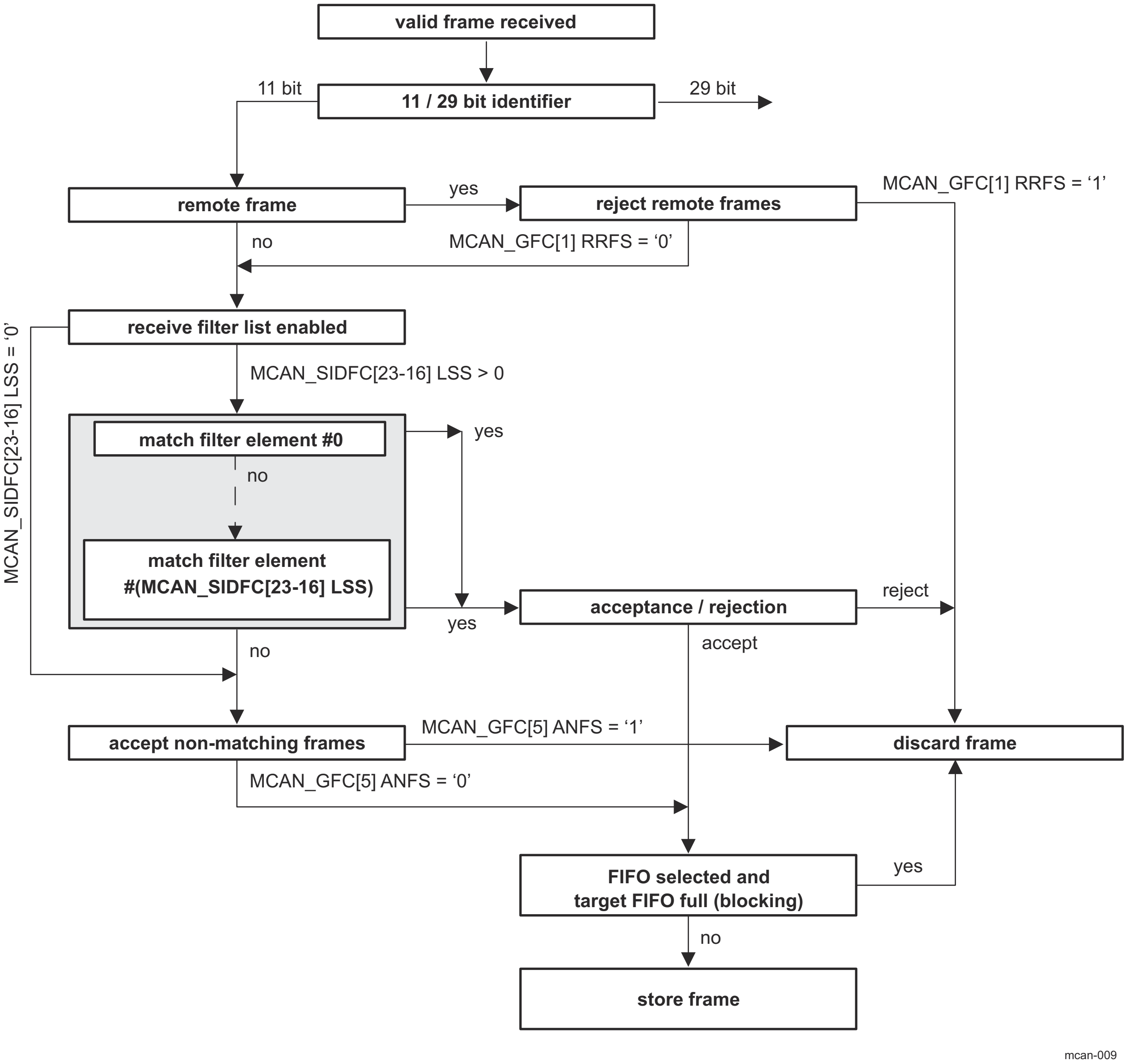

Figure 12-287. Standard Message ID Filter Path

12.4.1.4.7.1.5 Extended Message ID Filtering

The extended Message ID (29-bit ID) filtering flow is shown in Figure 12-288. Section 12.4.1.4.10.6 , *Extended Message ID Filter Element* describes the extended Message ID filter element.

The Remote Transmission Request (RTR) and Extended Identifier (XTD) bits of the received frames are compared against the list of configured filter elements. This is controlled by the following registers:

- Global Filter Configuration (MCAN_GFC) register
- Extended ID Filter Configuration (MCAN_XIDFC) register

Note that before the filter list is executed the received identifier is ANDed with the Extended ID AND Mask (MCAN_XIDAM).

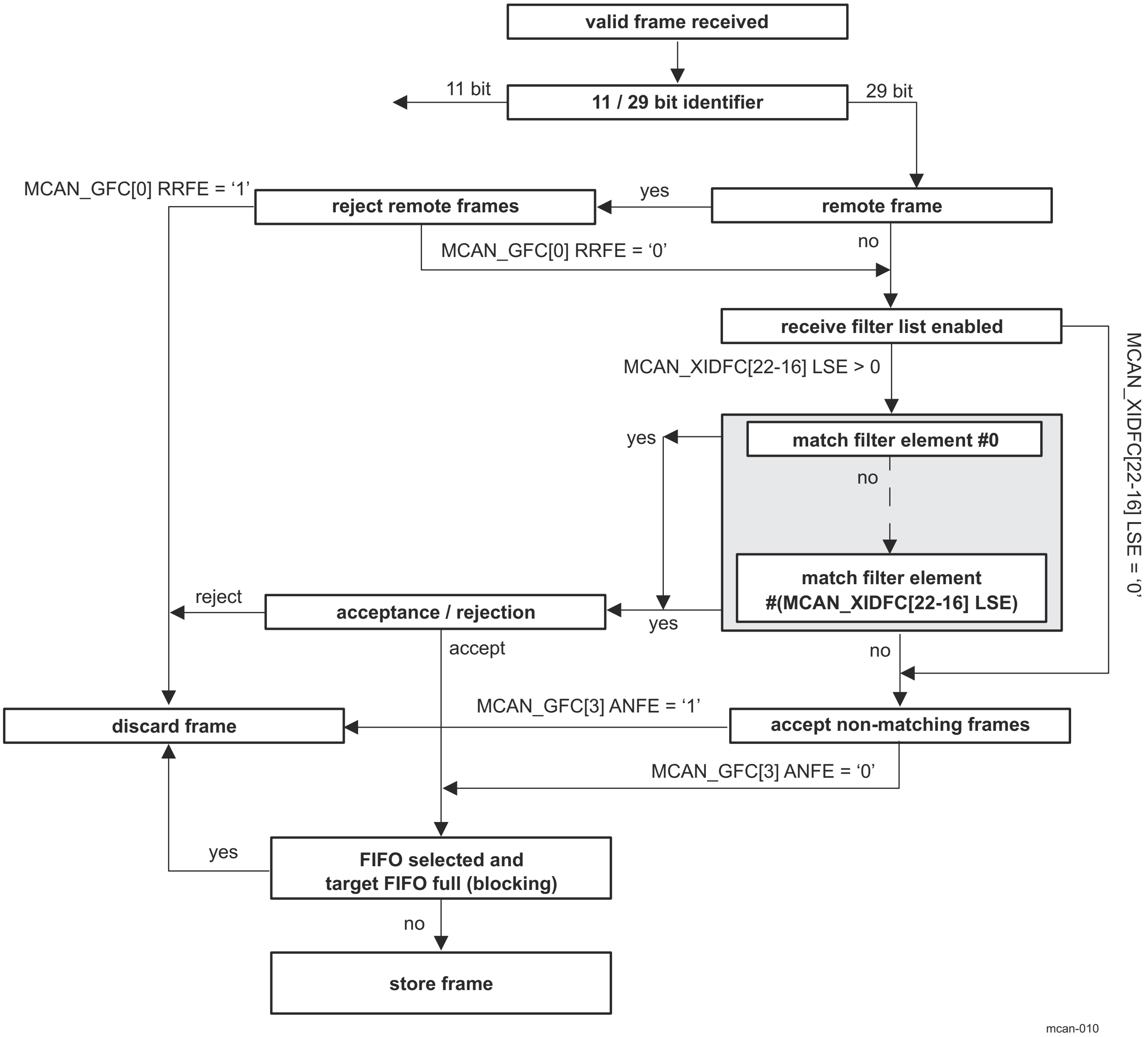

Figure 12-288. Extended Message ID Filter Path

12.4.1.4.7.2 Rx FIFOs

The configuration of the Rx FIFOs (Rx FIFO 0 and Rx FIFO 1) can be done via the MCAN_RXF0C and MCAN_RXF1C registers. Each Rx FIFO can be configured to store up to 64 received messages.

After acceptance filtering the received messages that passed are transferred to the Rx FIFO. The filter mechanisms available for the Rx FIFO 0 and Rx FIFO 1 is described in Section 12.4.1.4.7.1 , *Acceptance Filtering*. Section 12.4.1.4.10.2 , *Rx Buffer and FIFO Element* describes the Rx FIFO element.

The Rx FIFO watermark can be used to prevent an Rx FIFO overflow. If the Rx FIFO fill level reaches the Rx FIFO watermark configured by the MCAN_RXFnC[30-24] FnWM field (where: n = 0 or 1) an interrupt flag MCAN_IR[1] RF0W/MCAN_IR[5] RF1W is set.

When the Rx FIFO Put Index reaches the Rx FIFO Get Index (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI) an Rx FIFO Full condition is signalled by the MCAN_RXFnS[24] FnF status bit and interrupt flag MCAN_IR[2] RF0F/MCAN_IR[6] RF1F is set. Figure 12-289 shows Rx FIFO Status. The FIFOs fill level is presented in the MCAN_RXFnS[6-0] FnFL field (the number of elements stored in Rx FIFO).

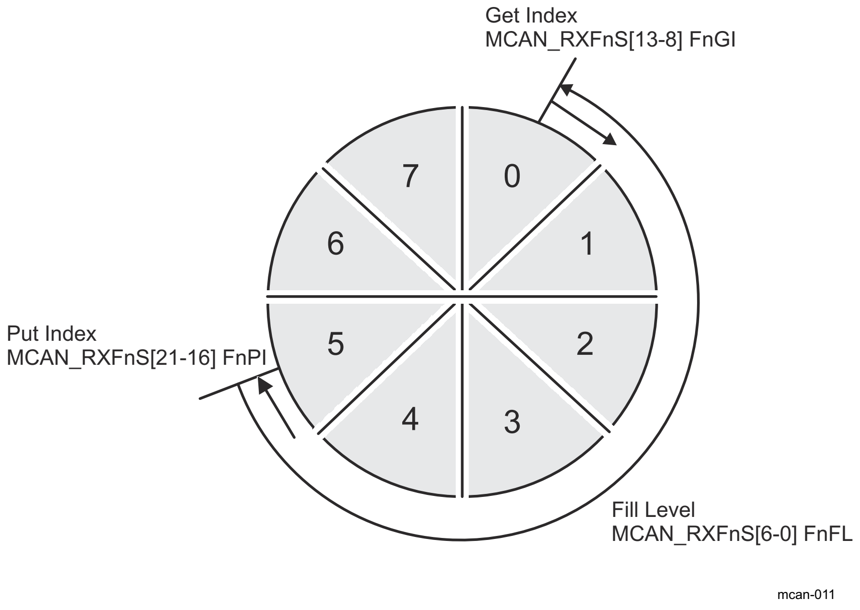

Figure 12-289. Rx FIFO Status

Rx FIFOs start address in the Message RAM (MCAN_RXFnC[15-2] FnSA field) have to be configured when reading from an Rx FIFO (Rx FIFO Get Index - MCAN_RXFnS[13-8] FnGI). Table 12-334 presents Rx Buffer/Rx FIFO Element Size for different Rx Buffer/Rx FIFO Data Field Size which is configured via the MCAN_RXESC register.

Table 12-346. Rx Buffer/Rx FIFO Element Size

MCAN_RXESC[10-8] RBDS MCAN_RXESC[2-0] F0DS/ MCAN_RXESC[6-4] F1DS	Data Field [bytes]	FIFO Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

12.4.1.4.7.2.1 Rx FIFO Blocking Mode

The Rx FIFO blocking mode is the default operation mode for the Rx FIFOs. It is configured by the MCAN_RXFnC[31] FnOM = 0.

If an Rx FIFO full condition is reached (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI), no further messages are written to the corresponding Rx FIFO until at least one message has been read out and the Rx FIFO Get Index has been incremented. An Rx FIFO full condition is signalled by the MCAN_RXFnS[24] FnF = 1 and interrupt flag MCAN_IR[2] RF0F/MCAN_IR[6] RF1F is set.

In case a message is received while the corresponding Rx FIFO is full, this message is rejected and the message lost condition is signalled by MCAN_RXFnS[25] RFnL = 1 and interrupt flag MCAN_IR[3] RFnL/ MCAN_IR[25] RFnL is set.

12.4.1.4.7.2.2 Rx FIFO Overwrite Mode

The Rx FIFO overwrite mode is configured by the MCAN_RXFnC[31] FnOM = 1. When an Rx FIFO full condition is reached (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI) signalled by MCAN_RXFnS[24] FnF = 1, the next accepted message for the FIFO will overwrite the oldest FIFO message. Put index/Get index are both incremented by one.

In overwrite mode if an Rx FIFO full condition is signalled, reading of the Rx FIFO elements should start at least at get index + 1. The reason for that is, that it might happen, that a received message is written to the Message RAM (Put index) while the Host CPU is reading from the Message RAM (Get index). In this case inconsistent data may be read from the respective Rx FIFO element. The problem is solved by adding an offset to the Get index when reading from the Rx FIFO. The offset depends on how fast the Host CPU accesses the Rx FIFO. Figure 12-290 shows an offset of two with respect to the Get index when reading the Rx FIFO. In this case the two messages stored in element 1 and 2 are lost.

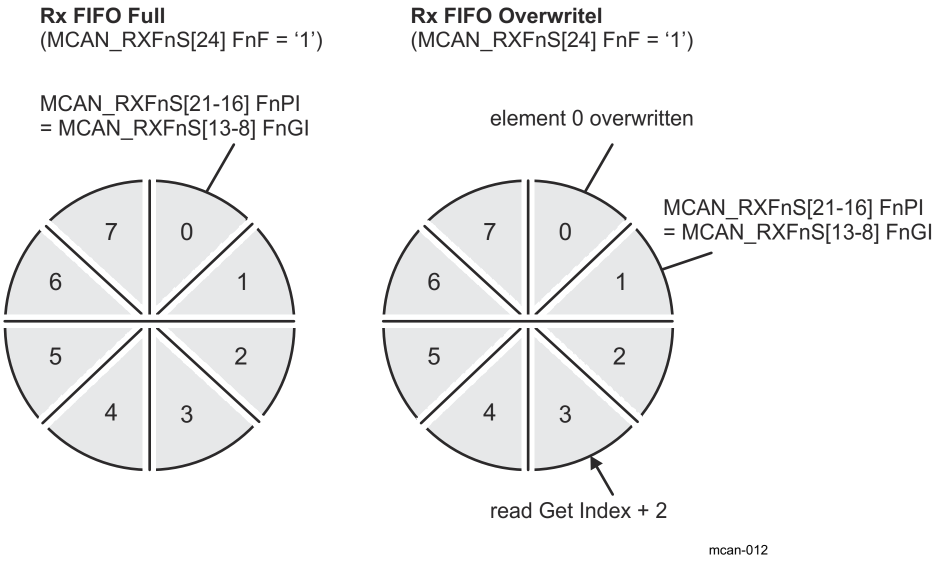

Figure 12-290. Rx FIFO Overflow Handling

After reading from the Rx FIFO, the number of the last element read has to be written to the Rx FIFO Acknowledge Index MCAN_RXFnA[5-0] FnAI. This increments the get index to that element number. In case the Put index has not been incremented to this Rx FIFO element, the Rx FIFO full condition is reset (MCAN_RXFnS[24] FnF = 0).

12.4.1.4.7.3 Dedicated Rx Buffers

The MCAN supports up to 64 dedicated Rx Buffers. The start address of the Rx Buffers section in the Message RAM is configured via MCAN_RXBC[15-2] RBSA field. To store in an Rx Buffer a Standard or Extended Message ID Filter Element with SFEC/EFEC = 111 and SFID2/EFID2[10-9] = 00 has to be configured (see Section 12.4.1.4.10.5 , *Standard Message ID Filter Element* and Section 12.4.1.4.10.6 , *Extended Message ID Filter Element*).

After a received message has been accepted by a filter element, the message is stored into the Rx Buffer in the Message RAM referenced by the filter element (the format is the same as for an Rx FIFO element). In addition the flag MCAN_IR[19] DRX (Message stored in Dedicated Rx Buffer) is set.

Table 12-335 shows Example Filter Configuration for Rx Buffers.

Table 12-347. Example Filter Configuration for Rx Buffers

Filter Element	SFID1[10-0] EFID1[28-0]	SFID2[10-9] EFID2[10-9]	SFID2[5-0] EFID2[5-0]
0	ID message 1	00	00 0000
1	ID message 2	00	00 0001
2	ID message 3	00	00 0010

After the last word of a matching received message has been written to the Message RAM, the respective New Data flag in register MCAN_NDAT1/MCAN_NDAT2 is set. As long as the New Data flag is set, the respective Rx Buffer is locked against updates from received matching frames. The New Data flags have to be reset by the Host CPU by writing a 1 to the respective bit position.

While an Rx Buffer's New Data flag is set, a Message ID Filter Element referencing this specific Rx Buffer will not match, causing the acceptance filtering to continue. Following Message ID Filter Elements may cause the received message to be stored into another Rx Buffer, or into an Rx FIFO, or the message may be rejected, depending on filter configuration.

12.4.1.4.7.3.1 Rx Buffer Handling

Rx Buffer Handling include the following steps:

- Reset interrupt flag MCAN_IR[19] DRX
- Read New Data registers
- Read messages from Message RAM
- Reset New Data flags of processed messages

12.4.1.4.7.4 Debug on CAN Support

Debug DMA is not supported feature. Debug messages can be traced through the RX FIFO (see Section 12.4.1.4.7.2).

12.4.1.4.8 Tx Handling

The Tx Handler is used to handle the Tx requests. It controls the transfer of transmit messages from the dedicated Tx Buffers, the Tx FIFO, and the Tx Queue to the CAN Core, the Tx Event FIFO, and the Put and Get Index operations. The MCAN module supports up to 32 Tx Buffers. These Tx Buffers can be configured as dedicated Tx Buffers, Tx FIFO, or Tx Queue and as combination of dedicated Tx Buffers/Tx FIFO or dedicated Tx Buffers/Tx Queue. For each Tx Buffer element Classical CAN or CAN FD transmission mode can be configured. Section 12.4.1.4.10.3 describes the Tx Buffer Element. Table 12-336 shows the possible configurations for message transmission.

Table 12-348. Possible Configurations for Message Transmission

MCAN_CCCR		Tx Buffer Element		Frame Transmission
MCAN_CCCR[9] BRSE	MCAN_CCCR[8] FDOE	FDF	BRS	
ignored	0	ignored	ignored	Classic CAN
0	1	0	ignored	Classic CAN
0	1	1	ignored	CAN FD without bit rate switching
1	1	0	ignored	Classic CAN
1	1	1	0	CAN FD without bit rate switching
1	1	1	1	CAN FD with bit rate switching

When the Tx Buffer Request Pending MCAN_TXBRP register is updated, or when a transmission has been started the Tx Handler starts scanning to check for the highest priority pending Tx request. The Tx Buffer with lowest Message ID has highest priority.

Note

AUTOSAR requires at least three Tx Queue Buffers and support of transmit cancellation.

12.4.1.4.8.1 Transmit Pause

The transmit pause feature is intended for use in CAN networks where the CAN Message IDs are specific and cannot easily be changed. These Message IDs may have a higher priority than other defined Message IDs, while in a specific application their relative priority should be inverse. This allows for a case where one ECU sends a burst of CAN messages that cause another ECU's CAN messages to be delayed (paused).

The transmit pause feature is enabled by the MCAN_CCCR[14] TXP bit. By default this bit is disabled (MCAN_CCCR[14] TXP = 0). Each time after successfully transmitted message, a pause for two CAN bit times occurs before the start of the next transmission. This allows the other CAN nodes in the network to transmit messages even if their Message IDs have lower priority.

12.4.1.4.8.2 Dedicated Tx Buffers

Dedicated Tx Buffers are intended for message transmission under complete control of the Host CPU.

There are two options:

- Each dedicated Tx Buffer is configured with a specific Message ID.
- Two or more dedicated Tx Buffers are configured with the same Message ID. In this case the Tx Buffer with the lowest buffer number is transmitted first.

After the data section has been updated, a transmission is requested by an Add Request. This is done via the MCAN_TXBAR[x]ARn bit (where x = 0 - 31). The requested messages arbitrate internally with messages from an optional Tx FIFO or Tx Queue and externally with messages on the CAN bus, and are sent out according to their Message ID.

Table 12-337 shows Tx Buffer/Tx FIFO/Tx Queue Element Size. A Dedicated Tx Buffer allocates Element Size 32-bit words in the Message RAM. The start address of a dedicated Tx Buffer in the Message RAM is calculated by adding transmit buffer index from 0 to 31 (MCAN_TXFQS[20-16] TFQPI) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

Table 12-349. Tx Buffer/Tx FIFO/Tx Queue Element Size

MCAN_TXESC[2-0] TBDS	Data Field [bytes]	Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

12.4.1.4.8.3 Tx FIFO

Tx FIFO mode is configured by setting bit MCAN_TXBC[30] TFQM = 0. The stored in the Tx FIFO messages are transmitted starting with the message referenced by the Get Index MCAN_TXFQS[12-8] TFGI field. After each transmission the Get Index is incremented until the Tx FIFO is empty. The Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field indicates the number of the available free Tx FIFO elements. The Tx FIFO allows transmission of messages with the same Message ID from different Tx Buffers in the order these messages have been written to the Tx FIFO.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index MCAN_TXFQS[20-16] TFQPI field. After each Add Request (MCAN_TXBAR[x] ARn = 1) the

Put Index is incemented to the next free Tx FIFO element. When the Put Index reaches the Get Index (MCAN_TXFQS[20-16] TFQPI = MCAN_TXFQS[12-8] TFGI), Tx FIFO Full condition is signalled by bit MCAN_TXFQS[21] TFQF = 1. In this case no further messages should be written to the Tx FIFO until the next message has been transmitted and the Get Index has been incremented.

The number of requested Tx buffers should not exceed the number of free Tx Buffers as indicated by the Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field.

In case a transmission request for the Tx Buffer referenced by the Get Index is cancelled, the Get Index is incremented to the next Tx Buffer with pending transmission request and the Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field is recalculated. In case transmission cancellation is applied to any other Tx Buffer - the Get Index and the FIFO Free Level remain unchanged.

A Tx FIFO element allocates Element Size 32-bit words in the Message RAM (see Table 12-337). The start address of the next available (free) Tx FIFO Buffer is calculated by adding Tx FIFO/Queue Put Index MCAN_TXFQS[20-16] TFQPI (from 0 to 31) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

12.4.1.4.8.4 Tx Queue

Tx Queue mode is configured by setting bit MCAN_TXBC[30] TFQM = 1. The stored in the Tx Queue messages are transmitted starting with the highest priority message (lowest Message ID). In case two or more Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index MCAN_TXFQS[20-16] TFQPI field. Each Add Request cyclically increments the Put Index to the next free Tx Buffer. In case of Tx Queue Full condition (MCAN_TXFQS[21] TFQF = 1), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been cancelled.

In Queue mode, only Full Index and Put Index are returned in read. The other fields - Get Index and Free Level are read as 0.

The application may use the MCAN_TXBRP register instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

A Tx Queue Buffer allocates Element Size 32-bit words in the Message RAM (see Table 12-337). The start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index MCAN_TXFQS[20-16] TFQPI (from 0 to 31) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

12.4.1.4.8.5 Mixed Dedicated Tx Buffers/Tx FIFO

For this combination the Tx Buffers section in the Message RAM is separated in two parts:

- Dedicated Tx Buffers: the number of Dedicated Tx Buffers is configured by the MCAN_TXBC[21-16] NDTB field
- Tx FIFO: the number of Tx Buffers assigned to the Tx FIFO is configured by the MCAN_TXBC[29-24] TFQS field

If the MCAN_TXBC[29-24] TFQS field is empty (zero) - only Dedicated Tx Buffers are used.

Tx prioritization:

- Scan Dedicated Tx Buffers and oldest pending Tx FIFO Buffer (referenced by the MCAN_TXFQS[12-8] TFGI field)
- Buffer with lowest Message ID gets highest priority and is transmitted next

Figure 12-291 shows Mixed Dedicated Tx Buffers/Tx FIFO example.

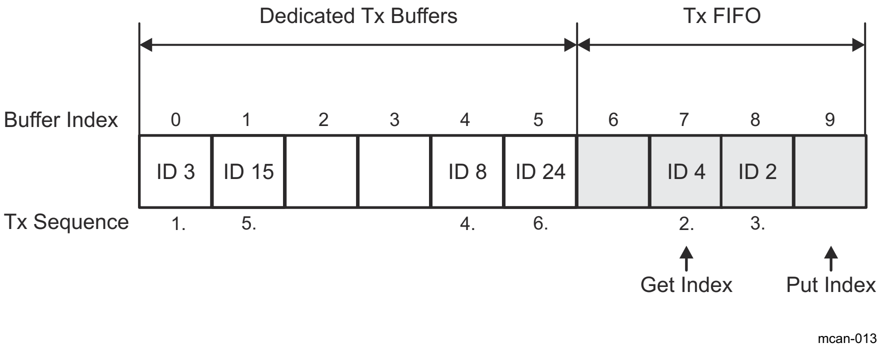

Figure 12-291. Mixed Dedicated Tx Buffers/Tx FIFO (example)

12.4.1.4.8.6 Mixed Dedicated Tx Buffers/Tx Queue

For this combination the Tx Buffers section in the Message RAM is separated in two parts:

- Dedicated Tx Buffers: the number of Dedicated Tx Buffers is configured by the MCAN_TXBC[21-16] NDTB field
- Tx Queue: the number of Tx Buffers assigned to the Tx Queue is configured by the MCAN_TXBC[29-24] TFQS field

If MCAN_TXBC[29-24] TFQS field is empty (zero) - only Dedicated Tx Buffers are used.

Tx prioritization:

- Scan all Tx Buffers with activated transmission request
- Tx Buffer with lowest Message ID gets highest priority and is transmitted next

Figure 12-292 shows Mixed Dedicated Tx Buffers/Tx Queue example.

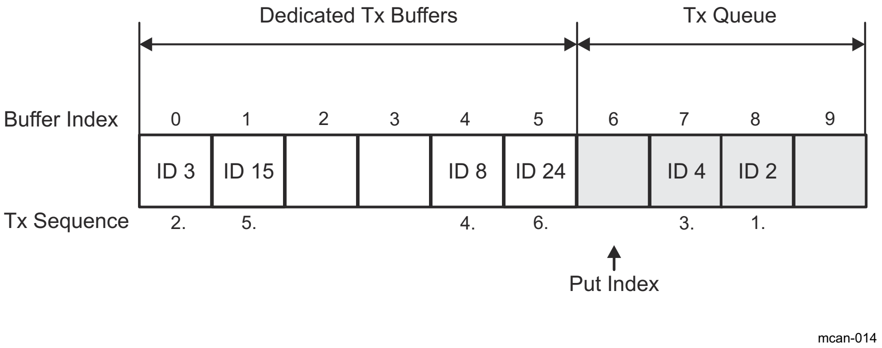

Figure 12-292. Mixed Dedicated Tx Buffers/Tx Queue (example)

12.4.1.4.8.7 Transmit Cancellation

This feature is especially intended for gateway and AUTOSAR based applications. The Host CPU can cancel a requested transmission from a dedicated Tx Buffer or a Tx Queue Buffer by setting bit MCAN_TXBCR[n] CRn = 1 (where n = 0 - 31). The corresponding bit position n is equivalent to the number of the Tx Buffer.

Transmit cancellation is not intended for Tx FIFO operation.

Successful cancellation is signalled by setting the corresponding bit of the MCAN_TXBCF register (MCAN_TXBCF[n] CFn = 1).

If transmission from a Tx Buffer is already ongoing and a transmit cancellation is requested, the corresponding MCAN_TXBRP[n] TRPn bit remains set as long as the transmission is in progress. If the transmission was successful, the corresponding MCAN_TXBTO[n] TOn and MCAN_TXBCF[n] CFn bits are set. If the transmission was not successful, only the corresponding bit MCAN_TXBCF[n] CFn = 1.

Note

If pending transmission is cancelled immediately before this transmission could have been started, a short time window occurs where no transmission is started even if another message is also pending in this node. This may enable another node to transmit a message which may have a lower priority than the second message in this node.

12.4.1.4.8.8 Tx Event Handling

To support Tx Event Handling the Message RAM has implemented a Tx Event FIFO section. Up to 32 Tx Event FIFO elements can be configured. Section 12.4.1.4.10.4 describes the Tx Event FIFO element. After message transmission on the CAN bus, Message ID and Timestamp are stored in a Tx Event FIFO element. To link a Tx Event to a Tx Event FIFO element, the Message Marker from the transmitted Tx Buffer is copied into the Tx Event FIFO element.

A Tx Event FIFO full condition is signalled by the MCAN_IR[14] TEFF bit. In this case no further elements are written to the Tx Event FIFO until at least one element has been read out and the Tx Event FIFO Get Index has been incremented (MCAN_TXEFS[12-8] EFGI). In case a Tx Event occurs while the Tx Event FIFO is full, this event is rejected and interrupt flag MCAN_IR[15] TEFL bit is set.

The Tx Event FIFO watermark can be configured to avoid a Tx Event FIFO overflow. When the Tx Event FIFO fill level reaches the Tx Event FIFO watermark configured by the MCAN_TXEFC[29-24] EFWM field, interrupt flag MCAN_IR[13] TEFW is set. When reading from the Tx Event FIFO, two times the Tx Event FIFO Get Index MCAN_TXEFS[12-8] EFGI field has to be added to the Tx Event FIFO start address MCAN_TXEFC[15-2] EFSA field.

12.4.1.4.9 FIFO Acknowledge Handling

The Get Indices of the two Rx FIFOs (Rx FIFO 0 or Rx FIFO 1) and the Tx Event FIFO are controlled by writing to the corresponding FIFO Acknowledge Index (see MCAN_RXF0A, MCAN_RXF1A, and MCAN_TXEFA). Writing to the FIFO Acknowledge Index will set the FIFO Get Index to the FIFO Acknowledge Index plus one and thereby updates the FIFO Fill Level.

There are two use cases:

- A single element has been read from the FIFO: the Get Index value is written to the FIFO Acknowledge Index.
- A sequence of elements has been read from the FIFO: the Get Index value (Index of the last element read) is written to the FIFO Acknowledge Index at the end of that read sequence.

The Host CPU has free access to the Message RAM. The special care has to be taken when reading FIFO elements in an arbitrary order (Get Index not considered). This can be useful when reading a High Priority Message from one of the two Rx FIFOs. In this case the FIFO's Acknowledge Index should not be written because this would set the Get Index to a wrong position and also changes the FIFO's Fill Level. In this case some of the older FIFO elements would be lost.

Note

The application has to ensure that a valid value is written to the FIFO Acknowledge Index. The MCAN module does not check for erroneous values.

12.4.1.4.10 Message RAM

The MCAN module has implemented Message RAM. The main purpose of the Message RAM is to store:

- Receive Messages
- Transmit Messages
- Tx Event Elements
- Message ID Filter Elements

12.4.1.4.10.1 Message RAM Configuration

The MCAN module is configured to allocate 4352 words in the Message RAM. The Message RAM has a width of 32 bits.

The following table presents the Message RAM Address Range for all device MCAN instances.

Table 12-350. Message RAM Address Range

Module Instance	Region Name	Address Range		Size
		Start	End	
MCAN0	MCAN0_MSGMEM_RAM	2070 8000h	2070 FFFFh	32 KB
MCAN1	MCAN1_MSGMEM_RAM	2071 8000h	2071 FFFFh	32 KB

The Message RAM is capable to include each of the sections listed in Figure 12-293. It is not necessary to configure each of the sections (a section in the Message RAM can be 0) and there is no restriction in regards to the sequence of the sections. For parity checking or ECC, the respective number of bits must to be added to each word.

The MCAN module addresses 32-bit words when addressing the Message RAM. The start addresses are configurable and are 32-bit word addresses.

The element size can be configured for:

- Rx FIFO 0 via the MCAN_RXESC[2-0] F0DS field
- Rx FIFO 1 via the MCAN_RXESC[6-4] F1DS field
- Rx Buffers via the MCAN_RXESC[10-8] RBDS field
- Tx Buffers via the MCAN_TXESC[2-0] TBDS field

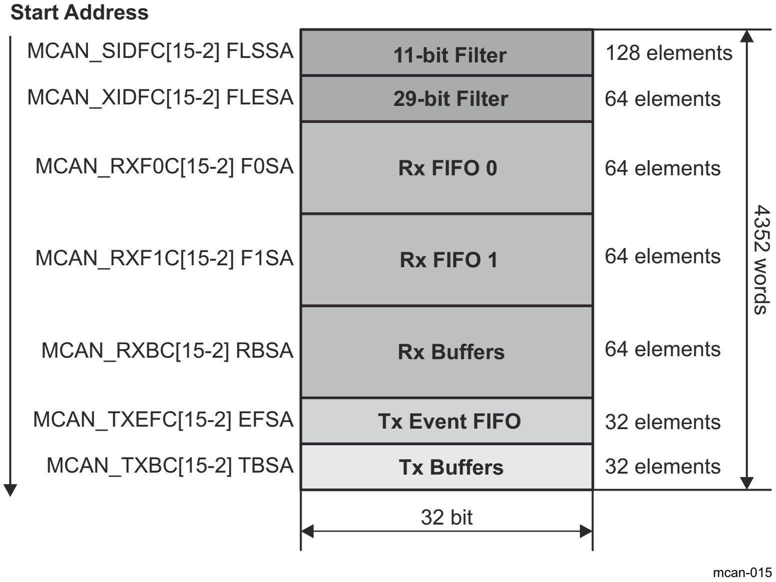

Figure 12-293. Message RAM Configuration

The Host CPU configures the following information in the Message RAM:

- Start addresses of the memory sections
- Number of elements in each section
- The size of the elements in some sections

Note

The MCAN module does not check for errors in the Message RAM configuration. The configuration of the start addresses of the different sections and the number of elements of each section has to be done carefully to prevent falsification or loss of data.

12.4.1.4.10.2 Rx Buffer and FIFO Element

Up to 64 Rx Buffers and two Rx FIFOs can be configured in the Message RAM. Each Rx FIFO section can be configured to store up to 64 received messages. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via the MCAN_RXESC register.

Figure 12-294 shows Rx Buffer/Rx FIFO element structure.

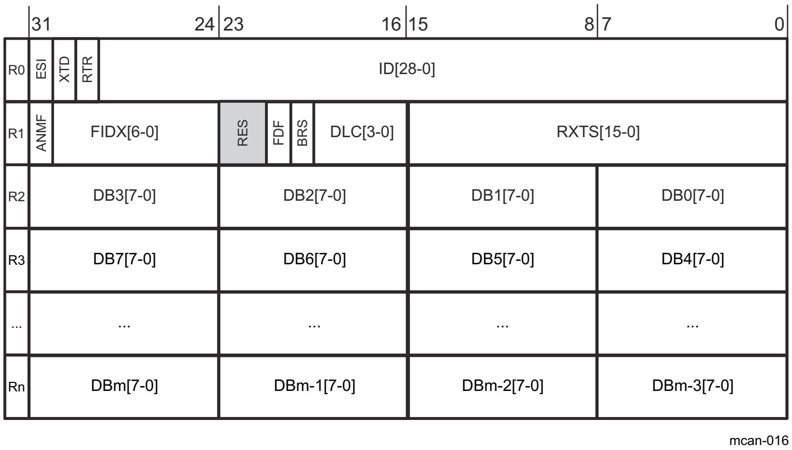

Figure 12-294. Rx Buffer/Rx FIFO Element Structure

Table 12-339 shows Rx Buffer/Rx FIFO element field descriptions.

Table 12-351. Rx Buffer/Rx FIFO Element Field Descriptions

Word	Bits	Field Name	Description
R0	31	ESI	Error State Indicator • 0h = Transmitting node is error active • 1h = Transmitting node is error passive
	30	XTD	Extended Identifier Signals to the Host CPU whether the received frame has a standard or extended identifier. • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier

Table 12-351. Rx Buffer/Rx FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	29	RTR	Remote Transmission Request Signals to the Host CPU whether the received frame is a data frame or a remote frame. • 0h = Received frame is a data frame • 1h = Received frame is a remote frame **Note:** There are no remote frames in CAN FD format. In case a CAN FD frame was received (FDF = 1), RTR bit reflects the state of the reserved r1 bit (RES[23]).
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier is stored into ID[28-18].
R1	31	ANMF	Accepted Non-matching Frame Acceptance of non-matching frames may be enabled via the MCAN_GFC[5-4] ANFS and MCAN_GFC[3-2] ANFE fields. • 0h = Received frame matching filter index FIDX field • 1h = Received frame did not match any Rx filter element
	30-24	FIDX[6-0]	Filter Index 0h-7Fh (0-127): Index of matching Rx acceptance filter element (invalid if ANMF = 1). Range is 0 to MCAN_SIDFC[23-16] LSS - 1 respectively MCAN_XIDFC[22-16] LSE - 1.
	23-22	RES	Reserved
	21	FDF	FD Format • 0h = Standard frame format • 1h = CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch • 0h = Frame received without bit rate switching • 1h = Frame received with bit rate switching
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: received frame has 0-8 data bytes • 9h-Fh (9-15) = CAN: received frame has 8 data bytes • 9h-Fh (9-15) = CAN FD: received frame has 12/16/20/24/32/48/64 data bytes
	15-0	RXTS[15-0]	Rx Timestamp Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC[19-16] TCP.
R2	31-24	DB3[7-0]	Data Byte 3

Table 12-351. Rx Buffer/Rx FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	23-16	DB2[7-0]	Data Byte 2
	15-8	DB1[7-0]	Data Byte 1
	7-0	DB0[7-0]	Data Byte 0
R3	31-24	DB7[7-0]	Data Byte 7
	23-16	DB6[7-0]	Data Byte 6
	15-8	DB5[7-0]	Data Byte 5
	7-0	DB4[7-0]	Data Byte 4
...	...	...	...
Rn	31-24	DBm[7-0]	Data Byte m
	23-16	DBm-1[7-0]	Data Byte m-1
	15-8	DBm-2[7-0]	Data Byte m-2
	7-0	DBm-3[7-0]	Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_RXESC), between two and sixteen 32-bit words (Rn = 3-17) are used for storage of a CAN message's data field.

12.4.1.4.10.3 Tx Buffer Element

The Tx Buffers section can be configured to hold dedicated Tx Buffers as well as a Tx FIFO/Tx Queue. In case that the Tx Buffers section is shared by dedicated Tx buffers and a Tx FIFO/Tx Queue, the dedicated Tx Buffers start at the beginning of the Tx Buffers section followed by the buffers assigned to the Tx FIFO or Tx Queue. The Tx Handler makes difference between dedicated Tx Buffers and Tx FIFO/Tx Queue via the MCAN_TXBC[29-24] TFQS and MCAN_TXBC[21-16] NDTB fields. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via the MCAN_TXESC register.

Figure 12-295 shows Tx Buffer element structure.

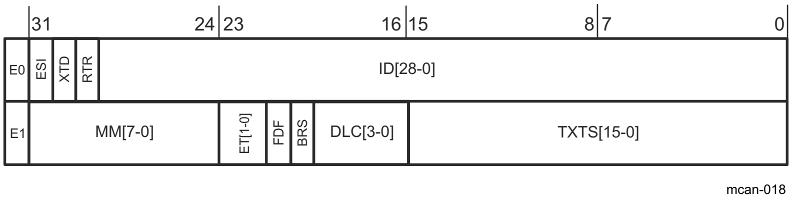

Figure 12-295. Tx Buffer Element Structure

Table 12-340 shows Tx Buffer element field descriptions.

Table 12-352. Tx Buffer Element Field Descriptions

Word	Bits	Field Name	Description
T0	31	ESI	Error State Indicator • 0h = ESI bit in CAN FD format depends only on error passive flag • 1h = ESI bit in CAN FD format transmitted recessive **Note:** The ESI bit of the transmit buffer is or'ed with the error passive flag to decide the value of the ESI bit in the transmitted CAN FD frame. As required by the CAN FD protocol specification, an error active node may optionally transmit the ESI bit recessive, but an error passive node will always transmit the ESI bit recessive.
	30	XTD	Extended Identifier • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier
	29	RTR	Remote Transmission Request • 0h = Transmit data frame • 1h = Transmit remote frame **Note:** When RTR = 1, the MCAN module transmits a remote frame according to ISO11898-1:2015, even if the MCAN_CCCR[8] FDOE bit enables the transmission in CAN FD format.
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier has to be written to ID[28-18].
T1	31-24	MM[7-0]	Message Marker Written by Host CPU during Tx Buffer configuration. Copied into Tx Event FIFO element for identification of Tx message status (see also MM[7-0] field in Table 12-341).
	23	EFC	Event FIFO Control • 0h = Don't store Tx events • 1h = Store Tx events
	22	RES	Reserved
	21	FDF	FD Format • 0h = Frame transmitted in Classic CAN format • 1h = Frame transmitted in CAN FD format

Table 12-352. Tx Buffer Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	20	BRS	Bit Rate Switch • 0h = CAN FD frames transmitted without bit rate switching • 1h = CAN FD frames transmitted with bit rate switching **Note:** ESI, FDF, and BRS bits are only evaluated when CAN FD operation is enabled vie the MCAN_CCCR[8] FDOE bit. BRS bit is only evaluated when in addition the MCAN_CCCR[9] BRSE = 1.
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: transmit frame has 0-8 data bytes • 9h-Fh (9-15) = CAN: transmit frame has 8 data bytes • 9h-Fh (9-15) = CAN FD: transmit frame has 12/16/20/24/32/48/64 data bytes
	15-0	RES	Reserved
T2	31-24	DB3[7-0]	Data Byte 3
	23-16	DB2[7-0]	Data Byte 2
	15-8	DB1[7-0]	Data Byte 1
	7-0	DB0[7-0]	Data Byte 0
T3	31-24	DB7[7-0]	Data Byte 7
	23-16	DB6[7-0]	Data Byte 6
	15-8	DB5[7-0]	Data Byte 5
	7-0	DB4[7-0]	Data Byte 4
...	...	...	...
Tn	31-24	DBm[7-0]	Data Byte m
	23-16	DBm-1[7-0]	Data Byte m-1
	15-8	DBm-2[7-0]	Data Byte m-2
	7-0	DBm-3[7-0]	Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_TXESC), between two and sixteen 32-bit words (Tn = 3-17) are used for storage of a CAN message's data field.

12.4.1.4.10.4 Tx Event FIFO Element

Each element stores information about transmitted messages. By reading the Tx Event FIFO the Host CPU gets this information in the order the messages were transmitted. Status information about the Tx Event FIFO can be obtained from the MCAN_TXEFS register.

Figure 12-296 shows Tx Event FIFO element structure.

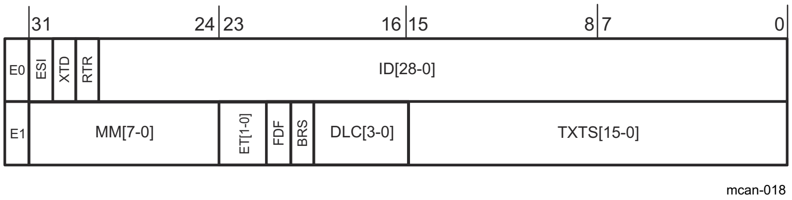

Figure 12-296. Tx Event FIFO Element Structure

Table 12-341 shows Tx Event FIFO element field descriptions.

Table 12-353. Tx Event FIFO Element Field Descriptions

Word	Bits	Field Name	Description
E0	31	ESI	Error State Indicator • 0h = Transmitting node is error active • 1h = Transmitting node is error passive
	30	XTD	Extended Identifier • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier
	29	RTR	Remote Transmission Request • 0h = Data frame transmitted • 1h = Remote frame transmitted
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier has to be written to ID[28-18].
E1	31-24	MM[7-0]	Message Marker Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status (see also MM[7-0] field in Table 12-340).
	23-22	ET[1-0]	Event Type • 0h = Reserved • 1h = Tx event • 2h = Transmission in spite of cancellation (always set for transmissions in DAR mode) • 3h = Reserved
	21	FDF	FD Format • 0h = Standard frame format • 1h = CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch • 0h = Frame transmitted without bit rate switching • 1h = Frame transmitted with bit rate switching

Table 12-353. Tx Event FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: frame with 0-8 data bytes transmitted • 9h-Fh (9-15) = CAN: frame with 8 data bytes transmitted • 9h-Fh (9-15) = CAN FD: frame with 12/16/20/24/32/48/64 data bytes transmitted
	15-0	TXTS[15-0]	Tx Timestamp Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC[19-16] TCP field.

12.4.1.4.10.5 Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, its address is the Filter List Standard Start Address MCAN_SIDFC[15-2] FLSSA field plus the index of the filter element (0-127).

Figure 12-297 shows Standard Message ID Filter element structure.

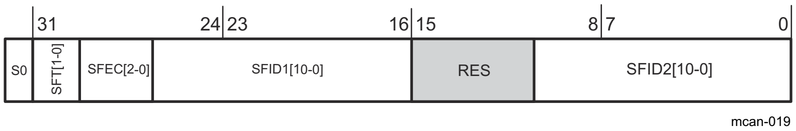

Figure 12-297. Standard Message ID Filter Element Structure

Table 12-342 shows Standard Message ID Filter element field descriptions.

Table 12-354. Standard Message ID Filter Element Field Descriptions

Word	Bits	Field Name	Description
S0	31-30	SFT[1-0]	Standard Filter Type • 0h = Range filter from SFID1 to SFID2 (SFID2 ≥ SFID1) • 1h = Dual ID filter for SFID1 or SFID2 • 2h = Classic filter: SFID1 = filter; SFID2 = mask • 3h = Filter element disabled **Note:** With SFT = 11 the filter element is disabled and the acceptance filtering continues (same behaviour as with SFEC = 000)

Table 12-354. Standard Message ID Filter Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	29-27	SFEC[2-0]	Standard Filter Element Configuration All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = 100, 101, or 110 a match sets interrupt flag MCAN_IR[8]HPM and, if enabled, an interrupt is generated. In this case the MCAN_HPMS register is updated with the status of the priority match. • 0h = Disable filter element • 1h = Store in Rx FIFO 0 if filter matches • 2h = Store in Rx FIFO 1 if filter matches • 3h = Reject ID if filter matches • 4h = Set priority if filter matches • 5h = Set priority and store in FIFO 0 if filter matches • 6h = Set priority and store in FIFO 1 if filter matches • 7h = Store into Rx Buffer , configuration of SFT[1-0] ignored
	26-16	SFID1[10-0]	Standard Filter ID 1 When filtering for Rx Buffers this field defines the ID of a standard message to be stored. The received identifiers must match exactly, no masking mechanism is used.
	15-11	RES	Reserved
	10-0	SFID2[10-0]	Standard Filter ID 2 This bit field has a different meaning depending on the configuration of SFEC: • 1) SFEC = 001 - 110 Second ID of standard ID filter element • 2) SFEC = 111 Filter for Rx Buffers
		SFID2[10-9]	This field is decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. • 0h = Store message into an Rx Buffer • 1h = Debug Message A • 2h = Debug Message B • 3h = Debug Message C **Note:** Debug feature is not supported.
		SFID2[8-6]	This field is used to control the filter event pins at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one MCAN_ICKL period in case the filter matches. **Note:** Only three filter event pins are supported.

Table 12-354. Standard Message ID Filter Element Field Descriptions (continued)

Word	Bits	Field Name	Description
		SFID2[5-0]	This field defines the offset to the Rx Buffer Start Address MCAN_RXBC[15-2] RBSA field for storage of a matching message.

12.4.1.4.10.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address MCAN_XIDFC[15-2] FLESA field plus two times the index of the filter element (0-63).

Figure 12-298 shows Extended Message ID Filter element structure.

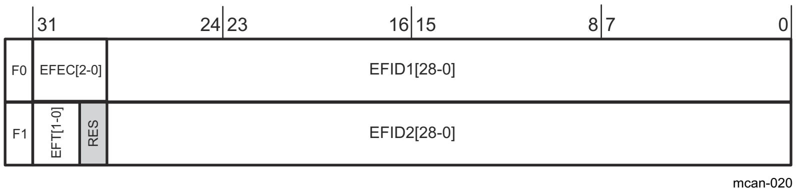

Figure 12-298. Extended Message ID Filter Element Structure

Table 12-343 shows Extended Message ID Filter element field descriptions.

Table 12-355. Extended Message ID Filter Element Field Descriptions

Word	Bits	Field Name	Description
F0	31-29	EFEC[2-0]	Extended Filter Element Configuration All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = 100, 101, or 110 a match sets interrupt flag MCAN_IR[8]HPM and, if enabled, an interrupt is generated. In this case the MCAN_HPMS register is updated with the status of the priority match. • 0h = Disable filter element • 1h = Store in Rx FIFO 0 if filter matches • 2h = Store in Rx FIFO 1 if filter matches • 3h = Reject ID if filter matches • 4h = Set priority if filter matches • 5h = Set priority and store in FIFO 0 if filter matches • 6h = Set priority and store in FIFO 1 if filter matches • 7h = Store into Rx Buffer or as debug message, configuration of EFT[1-0] ignored
	28-0	EFID1[28-0]	Extended Filter ID 1 First ID of extended ID filter element. When filtering for Rx Buffers this field defines the ID of an extended message to be stored. The received identifiers must match exactly, only XIDAM masking mechanism (see Section 12.4.1.4.7.1.5 , *Extended Message ID Filtering*) is used.

Table 12-355. Extended Message ID Filter Element Field Descriptions (continued)

Word	Bits	Field Name	Description
F1	31-30	EFT[1-0]	Extended Filter Type • 0h = Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1) • 1h = Dual ID filter for EFID1 or EFID2 • 2h = Classic filter: EFID1 = filter, EFID2 = mask • 3h = Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1), XIDAM mask not applied
	29	RES	Reserved
	28-0	EFID2[28-0]	Extended Filter ID 2 This bit field has a different meaning depending on the configuration of EFEC: • 1) EFEC = 001 - 110 Second ID of extended ID filter element • 2) EFEC = 111 Filter for Rx Buffers
		EFID2[10-9]	This field decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. • 0h = Store message into an Rx Buffer • 1h = Debug Message A • 2h = Debug Message B • 3h = Debug Message C **Note:** Debug feature is not supported.
		EFID2[8-6]	This field is used to control the filter event pins at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one MCAN_ICKL period in case the filter matches. **Note:** Only three filter event pins are supported.
		EFID2[5-0]	This field defines the offset to the Rx Buffer Start Address MCAN_RXBC[15-2] RBSA field for storage of a matching message.

12.4.2 Enhanced Capture (ECAP) Module

This section describes the Enhanced Capture (ECAP) module in the device.

12.4.2.1 ECAP Overview

The Enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The device has three instances of the ECAP module.

Table 12-344 shows the ECAP allocation across device domains.

Table 12-356. ECAP Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
ECAP0	-	✓
ECAP1	-	✓
ECAP2	-	✓

Figure 12-299 shows the ECAP modules overview.

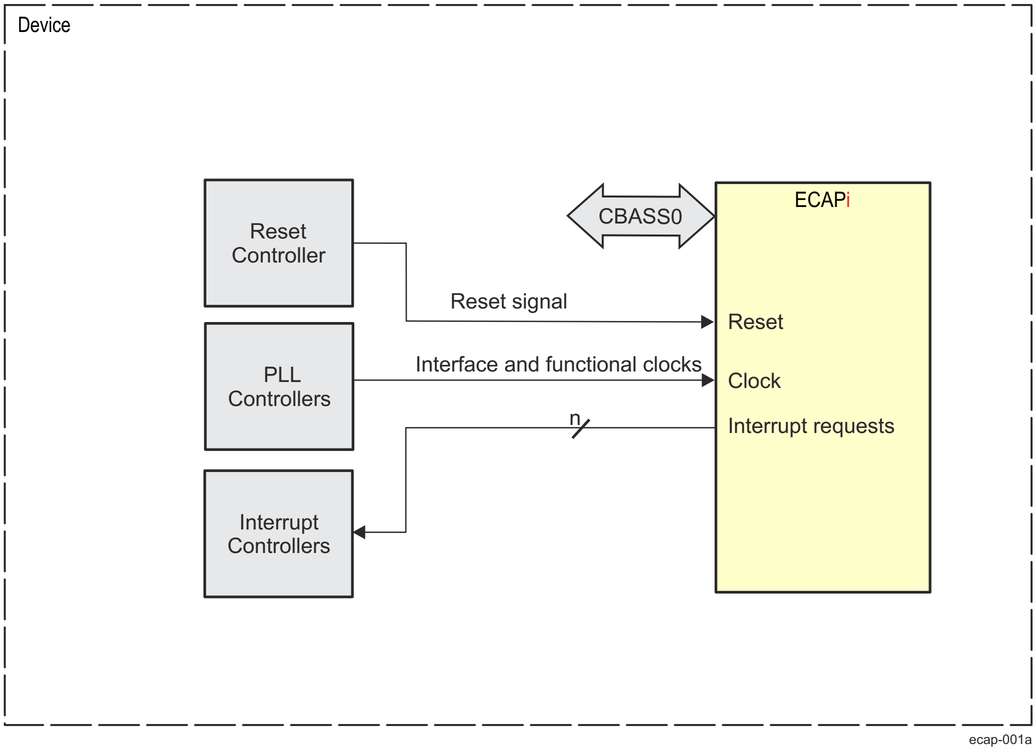

Note

i = 0 to 2

Figure 12-299. ECAP Overview

12.4.2.1.1 ECAP Features

The ECAP module includes the following features:

- 32-bit time base counter
- 4 × 32 bits event time-stamp capture registers (ECAP_CAP1 through ECAP_CAP4)
- 4-stage sequencer (Mod4 counter), synchronized to external events (ECAPx pin edges)
- Independent edge polarity (rising / falling edge) selection for all 4 sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Interrupt capabilities on any of the 4 capture events
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

12.4.2.2 ECAP Environment

12.4.2.2.1 ECAP I/O Interface

This section describes the ECAP external connections (environment).

Figure 12-300 shows the ECAP interface signals.

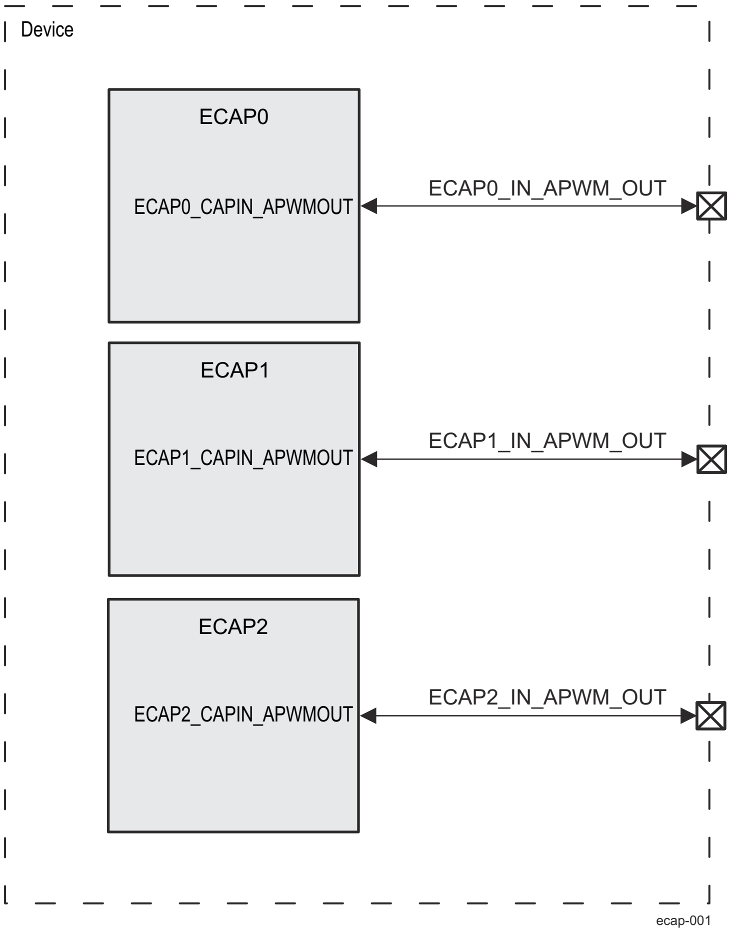

Figure 12-300. ECAP External Interface I/Os

Table 12-345 describes the ECAP I/O signals.

Table 12-357. ECAP I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
		ECAP0		
ECAP0_CAPIN_APWMOUT	ECAP0_IN_APWM_OUT	I/O	ECAP0 Capture input / PWM output	HiZ
		ECAP1		
ECAP1_CAPIN_APWMOUT	ECAP1_IN_APWM_OUT	I/O	ECAP1 Capture input / PWM output	HiZ
		ECAP2		
ECAP2_CAPIN_APWMOUT	ECAP2_IN_APWM_OUT	I/O	ECAP2 Capture input / PWM output	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.4.2.3 ECAP Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 12-301 shows the ECAP integration.

There are three instances of the Enhanced Capture (ECAP) module integrated in the device.

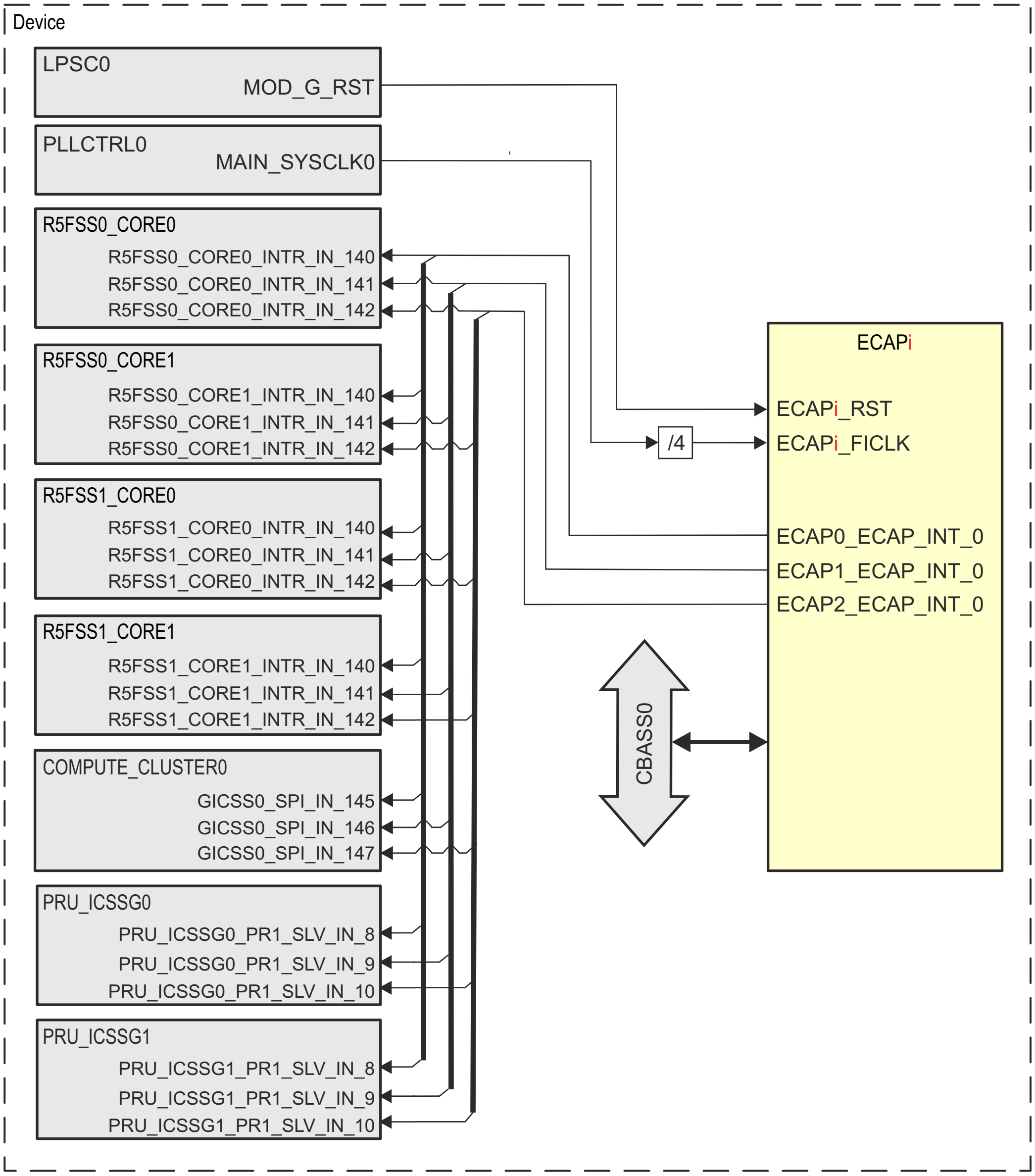

ecap-002-am64x

Note

i = 0 to 2

Figure 12-301. ECAP Integration

Table 12-346 through Table 12-349 summarize the integration of ECAP0, ECAP1 and ECAP2 modules in device MAIN domain.

Table 12-358. ECAP Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
ECAP0	PSC0	PD0	LPSC0	CBASS0
ECAP1	PSC0	PD0	LPSC0	CBASS0
ECAP2	PSC0	PD0	LPSC0	CBASS0

Table 12-359. ECAP Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
ECAP0	ECAP0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	ECAP0 functional and interface clock
ECAP1	ECAP1_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	ECAP1 functional and interface clock
ECAP2	ECAP2_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	ECAP2 functional and interface clock

Table 12-360. ECAP Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
ECAP0	ECAP0_RST	MOD_G_RST	LPSC0	Module Reset
ECAP1	ECAP1_RST	MOD_G_RST	LPSC0	Module Reset
ECAP2	ECAP2_RST	MOD_G_RST	LPSC0	Module Reset

Table 12-361. ECAP Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ECAP0	ECAP0_ECAP_INT_0	GICSS0_SPI_IN_145	COMPUTE_CLUSTER0	ECAP0 interrupt	Pulse
		PRU_ICSSG0_PR1_SLV_IN_8	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_8	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_140	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_140	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_140	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_140	R5FSS1_CORE1		
ECAP1	ECAP1_ECAP_INT_0	GICSS0_SPI_IN_146	COMPUTE_CLUSTER0	ECAP1 interrupt	Pulse
		PRU_ICSSG0_PR1_SLV_IN_9	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_9	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_141	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_141	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_141	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_141	R5FSS1_CORE1		
ECAP2	ECAP2_ECAP_INT_0	GICSS0_SPI_IN_147	COMPUTE_CLUSTER0	ECAP2 interrupt	Pulse
		PRU_ICSSG0_PR1_SLV_IN_10	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_10	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_142	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_142	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_142	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_142	R5FSS1_CORE1		

Note

For more information about interrupts, see Section 12.4.2.4.1.1.6 , *ECAP Interrupt Control*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.4.2.3.1 Daisy-Chain Connectivity between ECAP Modules

The ECAP modules provide input synchronisation signals to allow them to be synchronized to other modules or events. On the device, these signals are connected in a daisy-chain fashion for the ECAP0 to ECAP2 module as shown in Figure 12-302. The ECAP capture events come from external input pins.

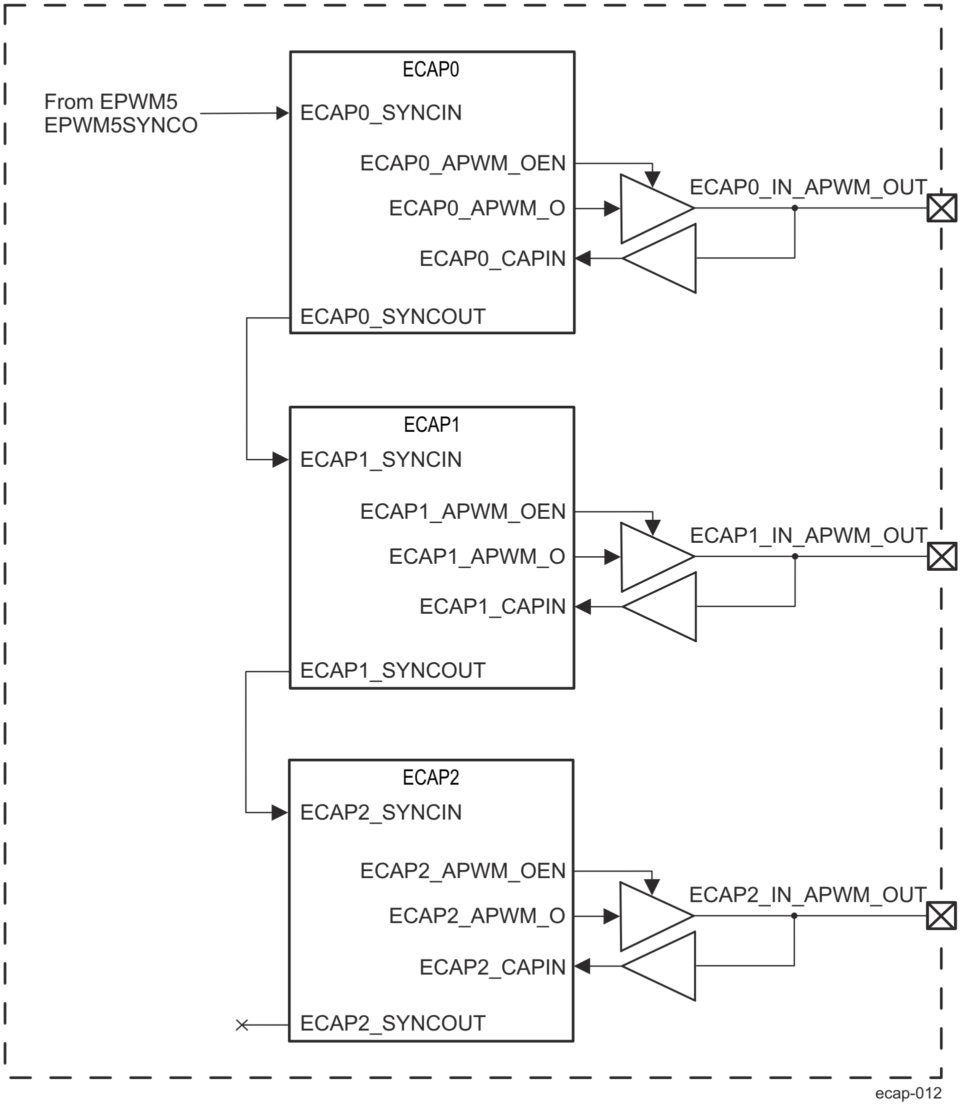

Figure 12-302. ECAP Daisy-Chain Connectivity

12.4.2.4 ECAP Functional Description

The ECAP module represents one complete capture channel, which has the following independent key resources:

- Dedicated input capture pin
- 32 events selection mapping capability to the input capture pin
- 32-bit time base counter
- 4 × 32-bit time-stamp capture registers (ECAP_CAP1 through ECAP_CAP4)
- 4-stage sequencer (Mod4 counter) that is synchronized to external events, ECAP pin rising/falling edges.
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Input capture signal prescaling (from 2-62)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Control for continuous time-stamp captures using a 4-deep circular buffer (ECAP_CAP1 through ECAP_CAP4) scheme
- Interrupt capabilities on any of the 4 capture events

Multiple identical ECAP modules can be contained in a system as shown in Figure 12-303. For actual number of the ECAP modules integrated in the device, refer to the *ECAP Integration*. The letter x within a signal or module name is used to indicate a generic ECAP instance on a device. For example, output interrupt request, ECAP1INT belongs to ECAP1, ECAP2INT belongs to ECAP2, and so forth.

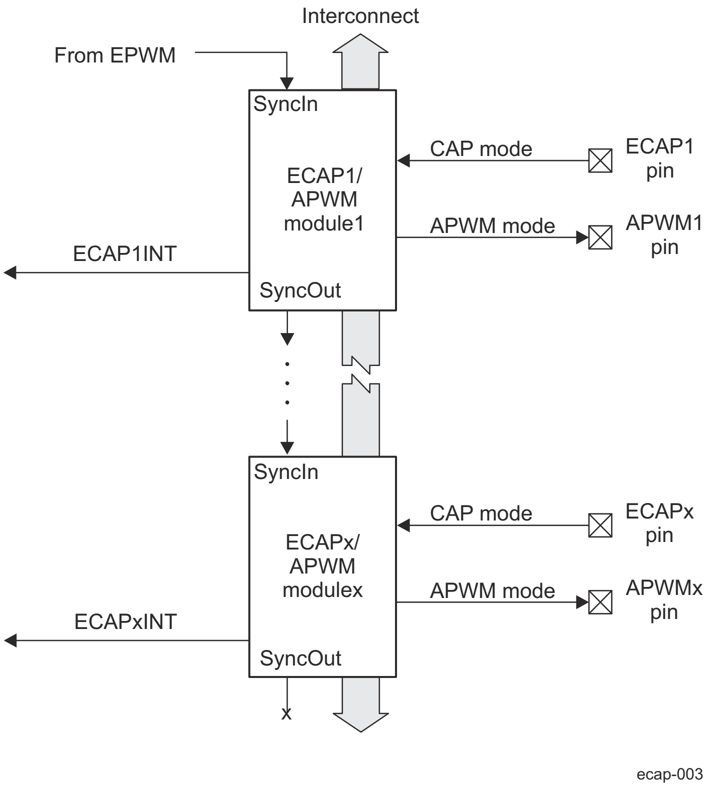

Figure 12-303. Multiple ECAP Modules

12.4.2.4.1 Capture and APWM Operating Modes

The ECAP module resources can be used to implement a single-channel PWM generator (with 32-bit capabilities) when it is not being used for input captures. The counter operates in count-up mode, providing a time-base for asymmetrical pulse width modulation (PWM) waveforms. The ECAP_CAP1 and ECAP_CAP2 registers become the active period and compare registers, respectively, while the ECAP_CAP3 and ECAP_CAP4 registers become the period and capture shadow registers, respectively. Figure 12-304 is a high-level view of both the capture and auxiliary pulse-width modulator (APWM) modes of operation.

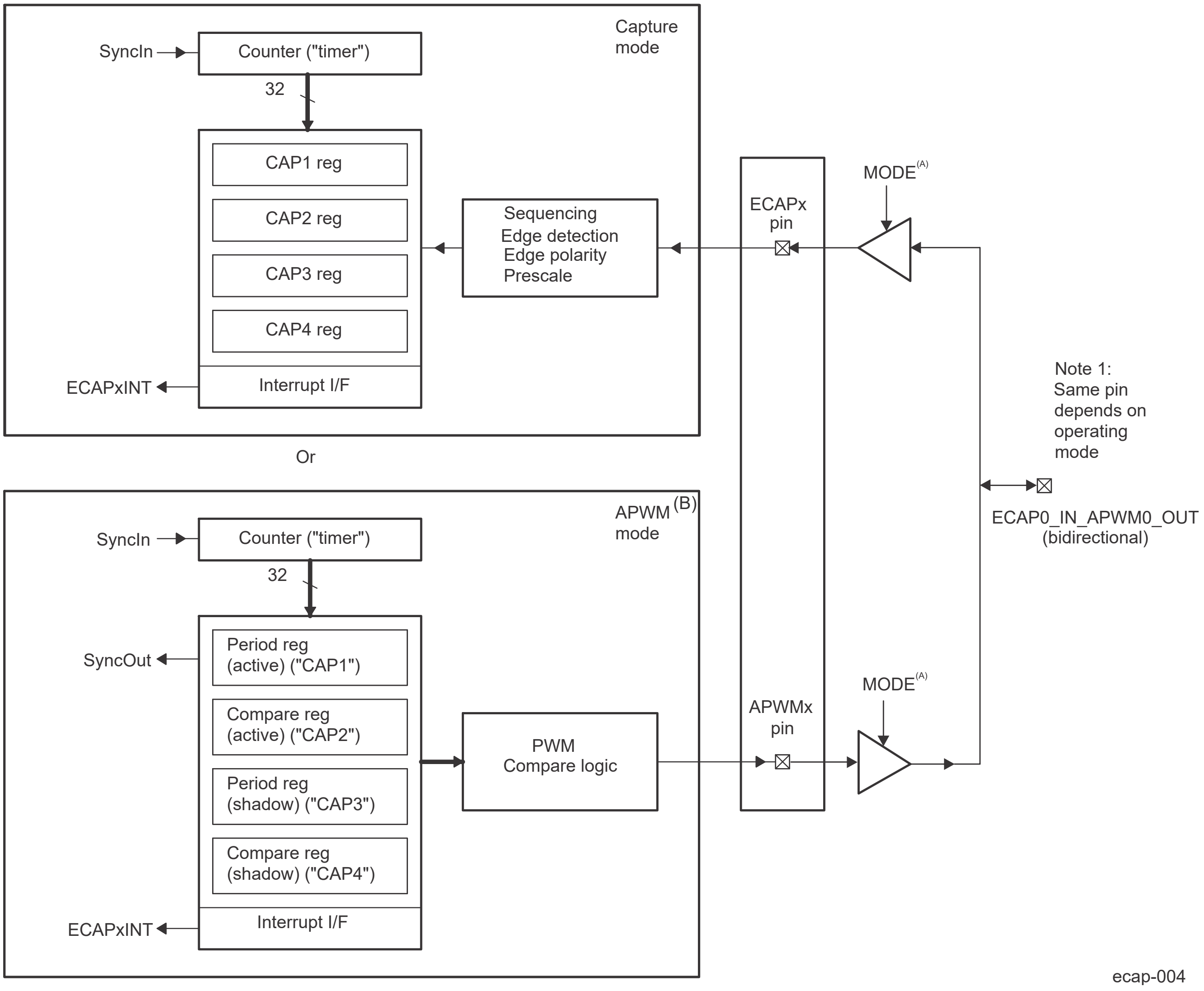

Note

A single pin is shared between CAP and APWM functions. In capture mode, it is an input. In APWM mode, it is an output.

Note

In APWM mode, writing any value to the ECAP_CAP1/ECAP_CAP2 active registers also writes the same value to the corresponding shadow registers (ECAP_CAP3/ECAP_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP_CAP3/ECAP_CAP4) invokes the shadow mode.

Figure 12-304. Capture and APWM Modes of Operation

12.4.2.4.1.1 ECAP Capture Mode Description

Figure 12-305 shows the various components that implement the capture function.

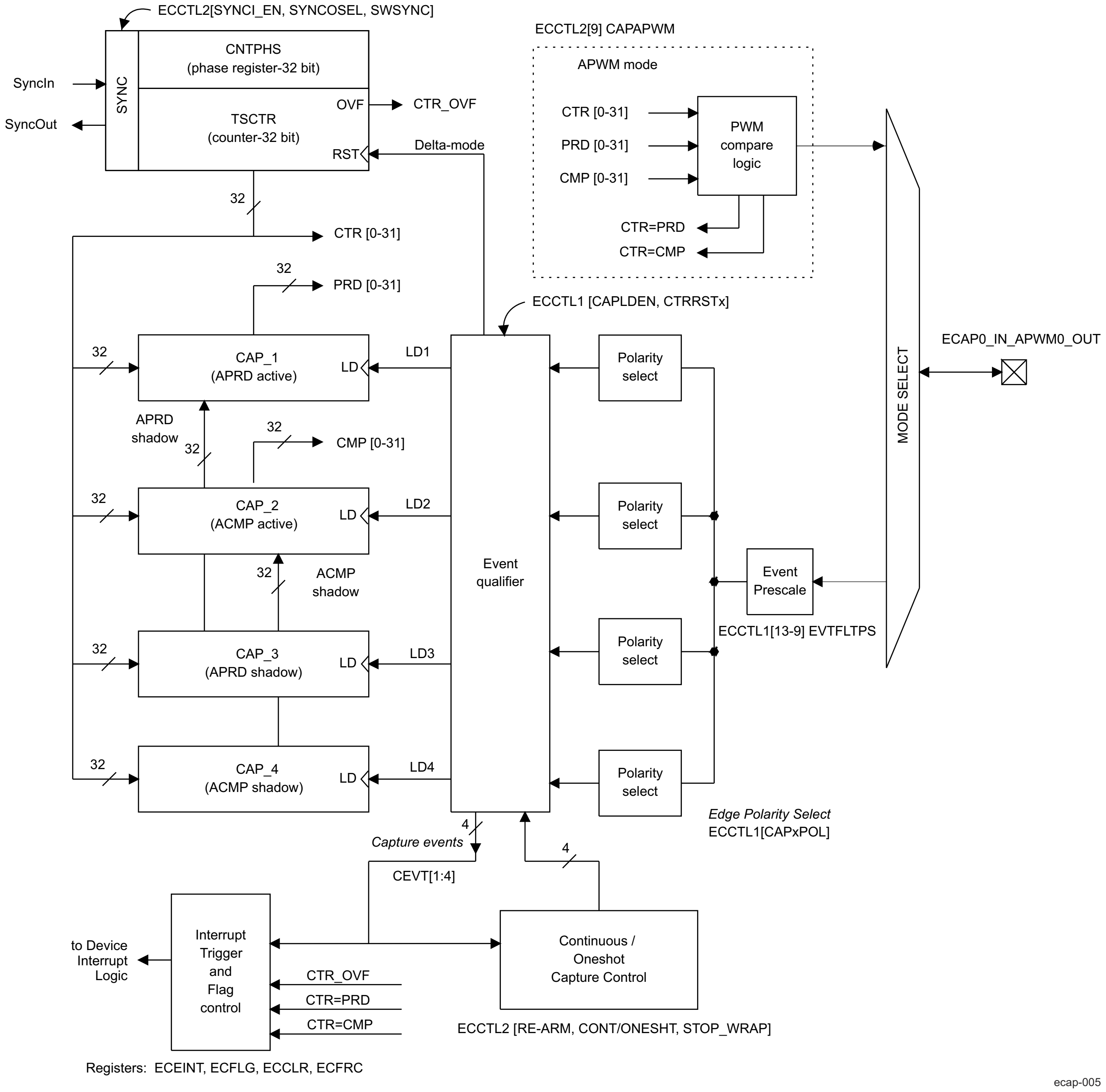

Figure 12-305. Capture Function Diagram

12.4.2.4.1.1.1 ECAP Event Prescaler

An input capture signal (pulse train) can be prescaled by N = 2-62 (in multiples of 2) or can bypass the prescaler. This is useful when very high frequency signals are used as inputs. Figure 12-306 shows a functional diagram and Figure 12-307 shows the operation of the prescale function.

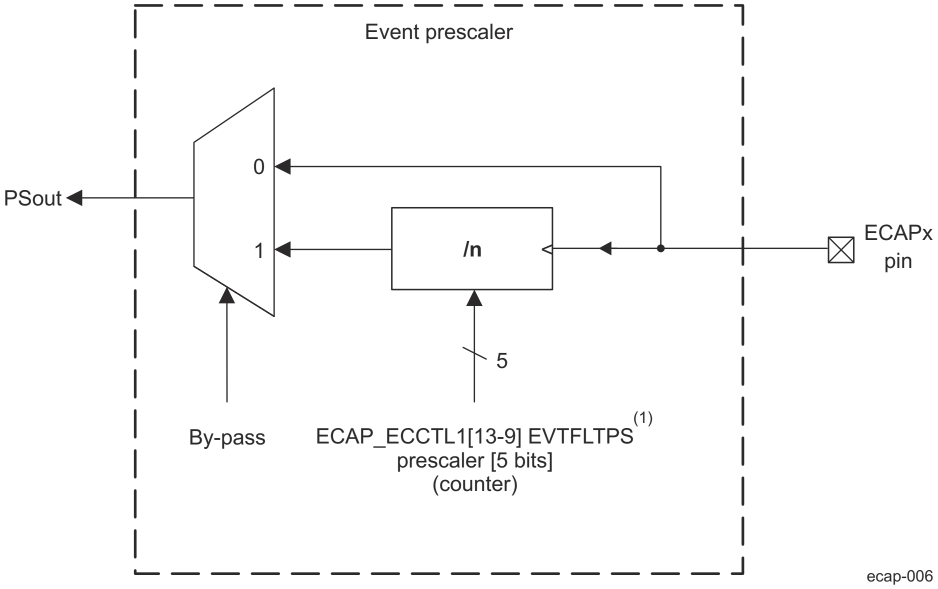

Note

When a prescale value of 1 is chosen (ECAP_ECCTL[13-9] EVTFLTPS = 0b0000) the input capture signal by-passes the prescale logic completely.

Figure 12-306. Event Prescale Control

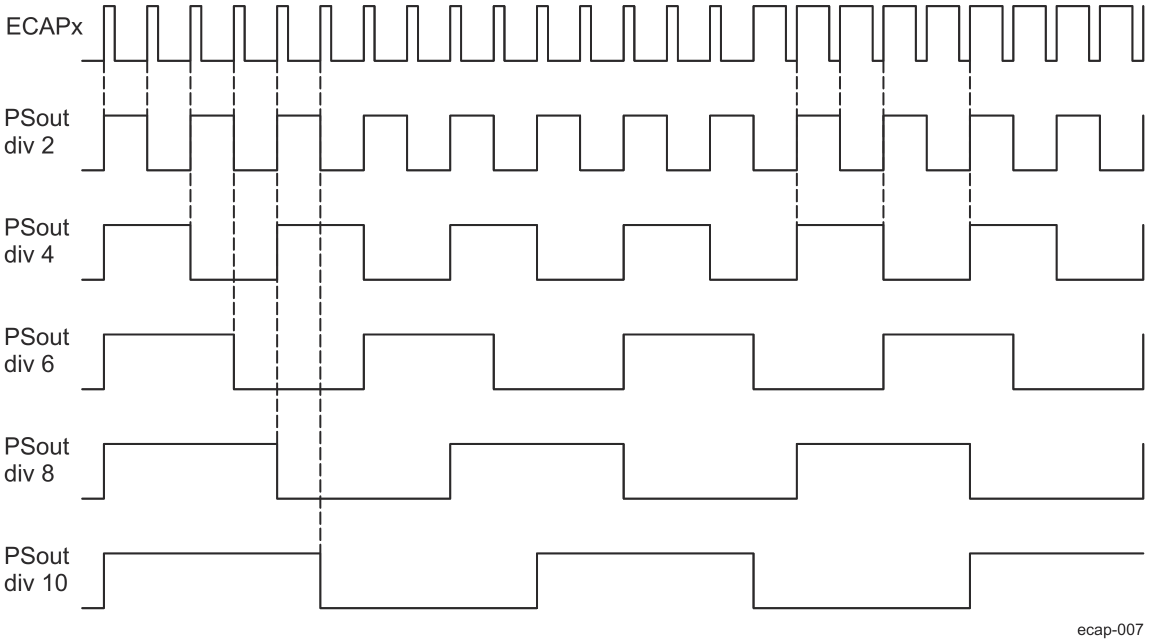

Figure 12-307. Prescale Function Waveforms

12.4.2.4.1.1.2 ECAP Edge Polarity Select and Qualifier

- Four independent edge polarity (rising edge/falling edge) selection multiplexers are used, one for each capture event.
- Each edge (up to 4) is event qualified by the Mod4 sequencer.
- The edge event is gated to its respective CAP*n* register by the Mod4 counter. The CAP*n* register is loaded on the falling edge.

12.4.2.4.1.1.3 ECAP Continuous/One-Shot Control

- The Mod4 (2-bit) counter is incremented via edge qualified events CEVT1 through CEVT4 (see the ECAP_ECINT_EN_FLG register).
- The Mod4 counter continues counting (0->1->2->3->0) and wraps around unless stopped.
- A 2-bit stop register is used to compare the Mod4 counter output; when equal the Mod4 counter stops and inhibits further loads of the ECAP_CAP1 through ECAP_CAP4 registers. This occurs during one-shot operation.

The continuous/one-shot block (Figure 12-308) controls the start/stop and reset (zero) functions of the Mod4 counter via a mono-shot type of action that can be triggered by the stop-value comparator and re-armed via software control.

Once armed, the ECAP module waits for 1-4 (defined by stop-value) capture events before freezing both the Mod4 counter and contents of the ECAP_CAP1 through ECAP_CAP4 registers (time-stamps).

Re-arming prepares the ECAP module for another capture sequence. Also re-arming clears (to zero) the Mod4 counter and permits loading of the ECAP_CAP1 through ECAP_CAP4 registers again, providing the ECAP_ECCTL[8] CAPLDEN bit is set.

In continuous mode, the Mod4 counter continues to run (0->1->2->3->0), the one-shot action is ignored, and capture values continue to be written to the ECAP_CAP1 through ECAP_CAP4 registers in a circular buffer sequence.

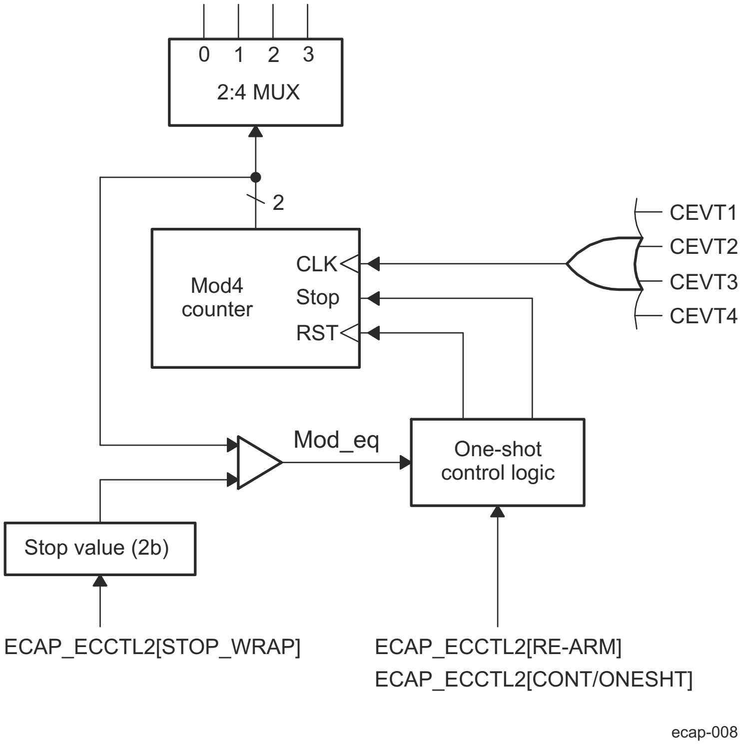

Figure 12-308. ECAP Continuous/One-shot Block Diagram

12.4.2.4.1.1.4 ECAP 32-Bit Counter and Phase Control

This counter (Figure 12-309) provides the time-base for event captures, and is clocked via the system clock.

A phase register is provided to achieve synchronization with other counters, via a hardware and software forced sync. This is useful in APWM mode when a phase offset between modules is needed.

On any of the four event loads, an option to reset the 32-bit counter is given. This is useful for time difference capture. The 32-bit counter value is captured first, then it is reset to 0 by any of the LD1 through LD4 signals.

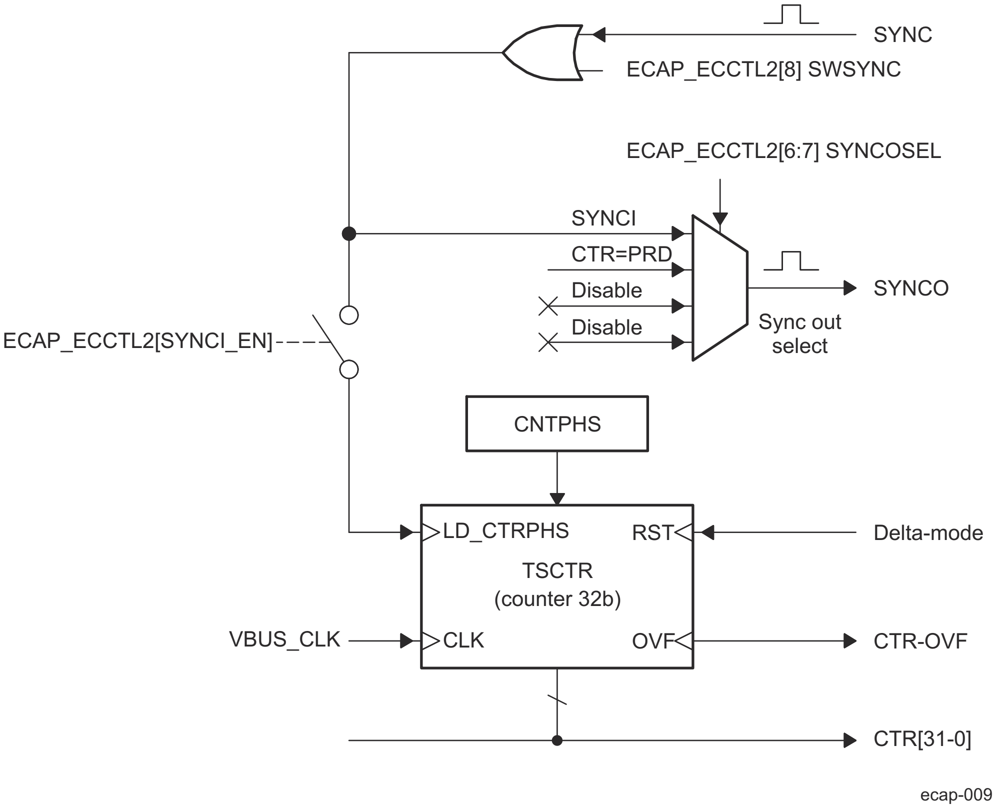

Figure 12-309. ECAP Counter and Synchronization Block Diagram

12.4.2.4.1.1.5 CAP1-CAP4 Registers

These 32-bit registers are fed by the 32-bit counter timer bus, CTR[0-31] and are loaded (capture a time-stamp) when their respective LD inputs are strobed.

Loading of the capture registers can be inhibited via the control ECAP_ECCTL[8] CAPLDEN bit. During one-shot operation, this bit is cleared (loading is inhibited) automatically when a stop condition occurs, StopValue = Mod4.

The ECAP_CAP1 and ECAP_CAP2 registers become the active period and compare registers, respectively, in APWM mode.

The ECAP_CAP3 and ECAP_CAP4 registers become the respective shadow registers (APRD and ACMP) for the ECAP_CAP1 and ECAP_CAP2 registers during APWM operation.

12.4.2.4.1.1.6 ECAP Interrupt Control

An interrupt can be generated on capture events CEVT1 through CEVT4, CNTOVF (see the ECAP_ECINT_EN_FLG[21] CNTOVF_FLG bit) or APWM events (TSCNT = PRD, TSCNT = CMP). See Figure 12-310.

A counter overflow event (FFFF FFFFh->0000 0000h) is also provided as an interrupt source (CNTOVF).

The capture events are edge and sequencer qualified (that is, ordered in time) by the polarity select and Mod4 gating, respectively.

One of these events can be selected as the interrupt source (from the ECAP*n* module) going to the interrupt controller.

Seven interrupt events (CEVT1, CEVT2, CEVT3, CEVT4, CNTOVF, TSCNT = PRD, TSCNT = CMP) can be generated. The interrupt enable register (ECAP_ECINT_EN_FLG) is used to enable/disable individual interrupt event sources. The interrupt flag register (ECAP_ECINT_EN_FLG) indicates if any interrupt event has been latched and contains the global interrupt flag ECAP_ECINT_EN_FLG[16] INT_FLG bit. An interrupt pulse is generated to the interrupt controller only if any of the interrupt events are enabled, the flag bit is 1h, and the INT_FLG flag bit is 0h. The interrupt service routine must clear the global interrupt flag bit and the serviced event via the interrupt clear register (ECAP_ECINT_CLR_FRC) before any other interrupt pulses are generated. The interrupt force register (ECAP_ECINT_CLR_FRC) can force an interrupt event. This is useful for test purposes.

12.4.2.4.1.1.7 ECAP Shadow Load and Lockout Control

In capture mode, this logic inhibits (locks out) any shadow loading of the ECAP_CAP1 or ECAP_CAP2 registers from APRD and ACMP registers, respectively.

In APWM mode, shadow loading is active and two choices are permitted:

- Immediate - APRD or ACMP are transferred to the ECAP_CAP1 or ECAP_CAP2 register immediately upon writing a new value.
- On period equal, CTR[31-0] = PRD[31-0]

Note

The CEVT1_FLG, CEVT2_FLG, CEVT3_FLG, CEVT4_FLG flags are only active in capture mode (ECAP_ECCTL[25] CAP_APWM == 0h). The TSCNT = PRD, TSCNT = CMP flags are only valid in APWM mode (ECAP_ECCTL[25] CAP_APWM == 1h). CNTOVF_FLG flag is valid in both modes.

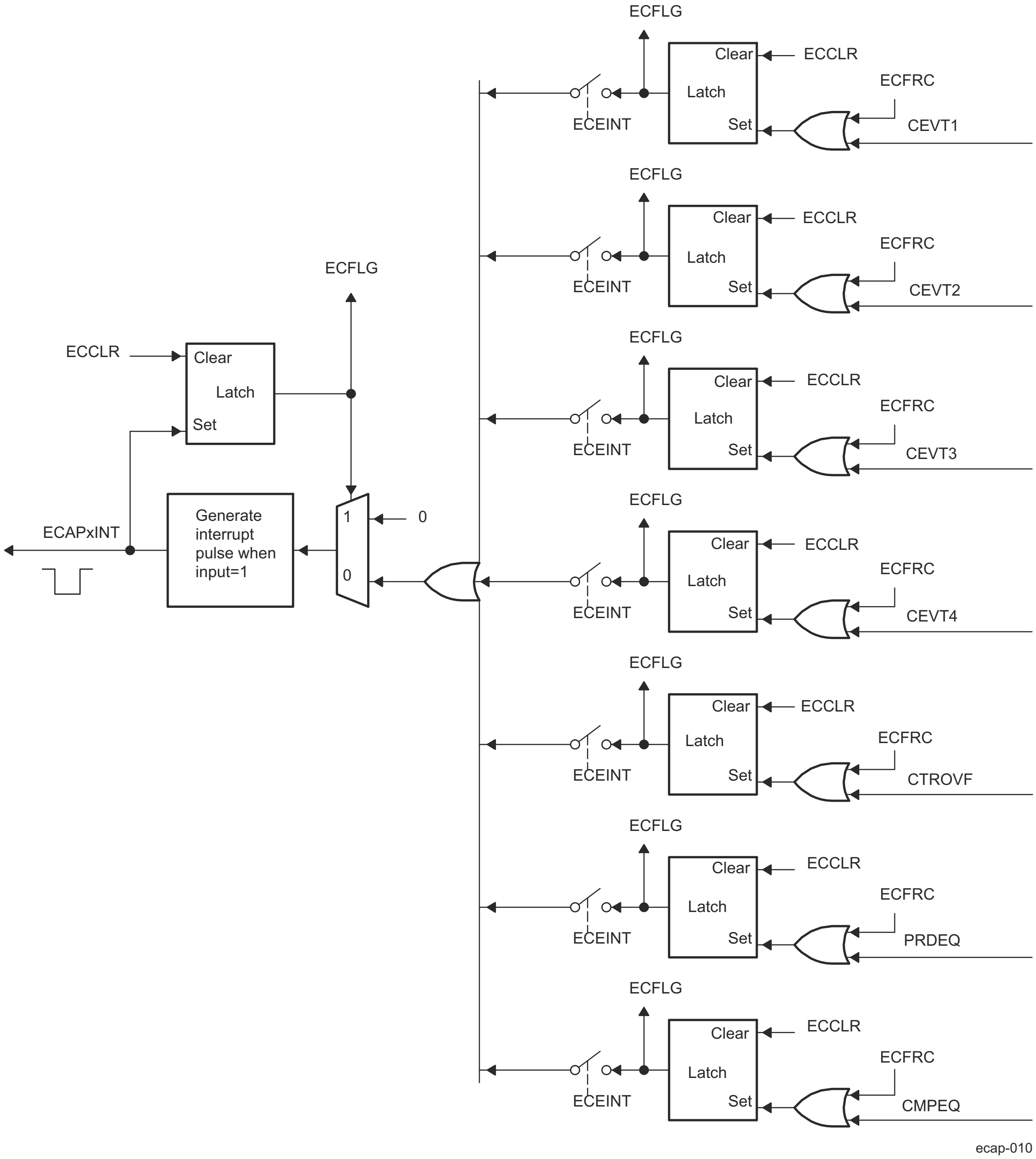

Figure 12-310. Interrupts in ECAP Module

12.4.2.4.1.2 ECAP APWM Mode Operation

Main operating highlights of the APWM section:

- The time-stamp counter bus is made available for comparison via 2 digital (32-bit) comparators.
- When the ECAP_CAP1/ECAP_CAP2 registers are not used in capture mode, their contents can be used as Period and Compare values in APWM mode.
- Double buffering is achieved via the shadow registers - APRD and ACMP (ECAP_CAP3/ECAP_CAP4). The shadow register contents are transferred over to ECAP_CAP1/ECAP_CAP2 registers either immediately upon a write, or on a TSCNT = PRD trigger.
- In APWM mode, writing to the ECAP_CAP1/ECAP_CAP2 active registers will also write the same value to the corresponding shadow registers (ECAP_CAP3/ECAP_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP_CAP3/ECAP_CAP4) will invoke the shadow mode.
- During initialization, software must write the PRD and CMP values to the active registers. This automatically copies the initial values into the shadow values. For subsequent compare updates, during run-time, software should use only shadow registers.

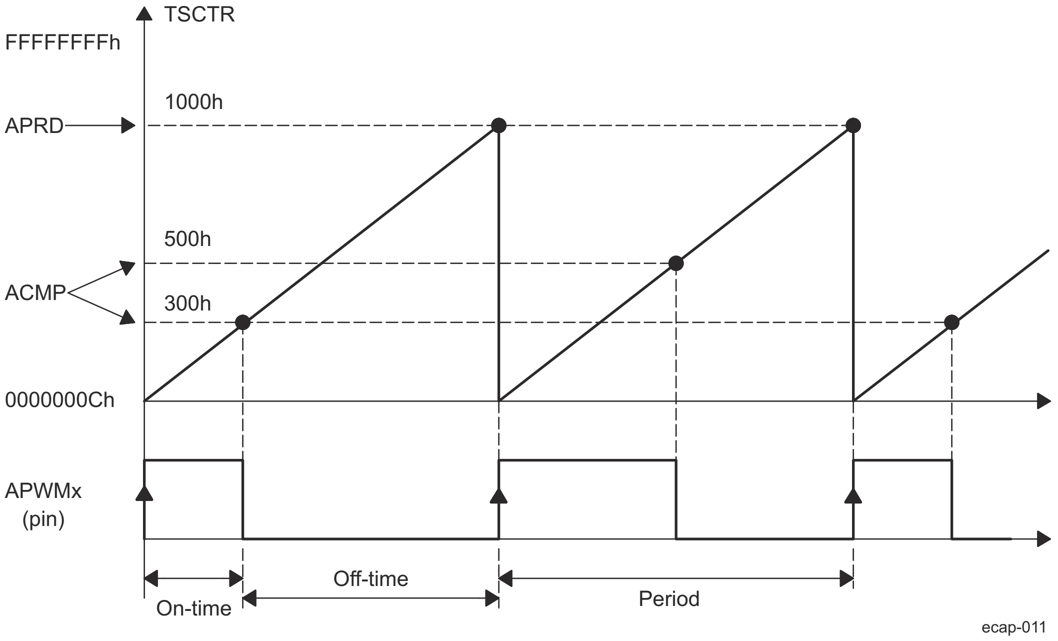

Figure 12-311. PWM Waveform Details of ECAP APWM Mode Operation

The behavior of APWM active-high mode (APWMPOL == 0) is:

```
CMP = 0x00000000, output low for duration of period (0% duty)
```

```
CMP = 0x00000001, output high 1 cycle
```

```
CMP = 0x00000002, output high 2 cycles
```

```
CMP = PERIOD, output high except for 1 cycle (<100% duty)
```

```
CMP = PERIOD+1, output high for complete period (100% duty)
```

```
CMP > PERIOD+1, output high for complete period
```

The behavior of APWM active-low mode (APWMPOL == 1) is:

```
CMP = 0x00000000, output high for duration of period (0% duty)
```

```
CMP = 0x00000001, output low 1 cycle
```

```
CMP = 0x00000002, output low 2 cycles
```

```
CMP = PERIOD, output low except for 1 cycle (<100% duty)
```

```
CMP = PERIOD+1, output low for complete period (100% duty)
```

```
CMP > PERIOD+1, output low for complete period
```

12.4.2.4.2 Summary of ECAP Functional Registers

Table 12-350 shows the ECAP module control and status register set. All 32-bit registers are aligned on even address boundaries and are organized in little-endian mode.

Note

In APWM mode, writing to the ECAP_CAP1/ECAP_CAP2 active registers also writes the same value to the corresponding shadow registers (ECAP_CAP3/ECAP_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP_CAP3/ECAP_CAP4) invokes the shadow mode.

Table 12-362. ECAP Control and Status Functional Registers

Offset	Register Name	Description	Size (×16)
0h	ECAP_TSCNT	Time-Stamp Counter Register	2
4h	ECAP_CNTPHS	Counter Phase Offset Value Register	2
8h	ECAP_CAP1	Capture 1 Register	2
Ch	ECAP_CAP2	Capture 2 Register	2
10h	ECAP_CAP3	Capture 3 Register	2
14h	ECAP_CAP4	Capture 4 Register	2
28h	ECAP_ECCTL	Capture Control Register	2
2Ch	ECAP_ECINT_EN_FLG	Capture Interrupt Enable and Flag Register	2
30h	ECAP_ECINT_CLR_FRC	Capture Interrupt Clear and Forcing Register	2
5Ch	ECAP_PID	Revision ID Register	2

Note

For more information on the ECAP registers, see *ECAP Registers.*

12.4.2.5 ECAP Use Cases

The following sections will provide applications examples and code snippets to show how to configure and operate the ECAP module. For clarity and ease of use, below are useful #defines which will help in the understanding of the examples.

```
// ECCTL1 ( ECAP Control Reg 1)
//==========================
// CAPxPOL bits
#defineEC_RISING      0x0
#defineEC_FALLING     0x1
// CTRRSTx bits
#defineEC_ABS_MODE    0x0
#defineEC_DELTA_MODE      0x1
// PRESCALE bits
#defineEC_BYPASS      0x0
#defineEC_DIV1        0x0
#defineEC_DIV2        0x1
#defineEC_DIV4        0x2
#defineEC_DIV6        0x3
#defineEC_DIV8        0x4
#defineEC_DIV10       0x5
// ECCTL2 ( ECAP Control Reg 2)
//==========================
// CONT/ONESHOT bit
#defineEC_CONTINUOUS      0x0
#defineEC_ONESHOT     0x1
// STOPVALUE bit
#defineEC_EVENT1      0x0
#defineEC_EVENT2      0x1
#defineEC_EVENT3      0x2
#defineEC_EVENT4      0x3
// RE-ARM bit
#defineEC_ARM         0x1
// TSCTRSTOP bit
#defineEC_FREEZE      0x0
#defineEC_RUN         0x1
// SYNCO_SEL bit
#defineEC_SYNCIN      0x0
#defineEC_CTR_PRD     0x1
#defineEC_SYNCO_DIS       0x2
// CAP/APWM mode bit
#defineEC_CAP_MODE    0x0
#defineEC_APWM_MODE       0x1
// APWMPOL bit
#defineEC_ACTV_HI     0x0
#defineEC_ACTV_LO     0x1
// Generic
#defineEC_DISABLE     0x0
#defineEC_ENABLE      0x1
#defineEC_FORCE       0x1
```

12.4.2.5.1 Absolute Time-Stamp Operation Rising Edge Trigger Example

Figure 12-312 shows an example of continuous capture operation (Mod4 counter wraps around). In this figure, TSCTR counts-up without resetting and capture events are qualified on the rising edge only, this gives period (and frequency) information.

On an event, the TSCTR contents (time-stamp) is first captured, then Mod4 counter is incremented to the next state. When the TSCTR reaches FFFF FFFFh (maximum value), it wraps around to 0000 0000h (not shown in Figure 12-312), if this occurs, the CNTOVF_FLG (counter overflow) flag is set, and an interrupt (if enabled) occurs. Captured time-stamps are valid at the point indicated by the diagram, after the 4-th event, hence event CEVT4 can conveniently be used to trigger an interrupt and the CPU can read data from the CAP*n* registers.

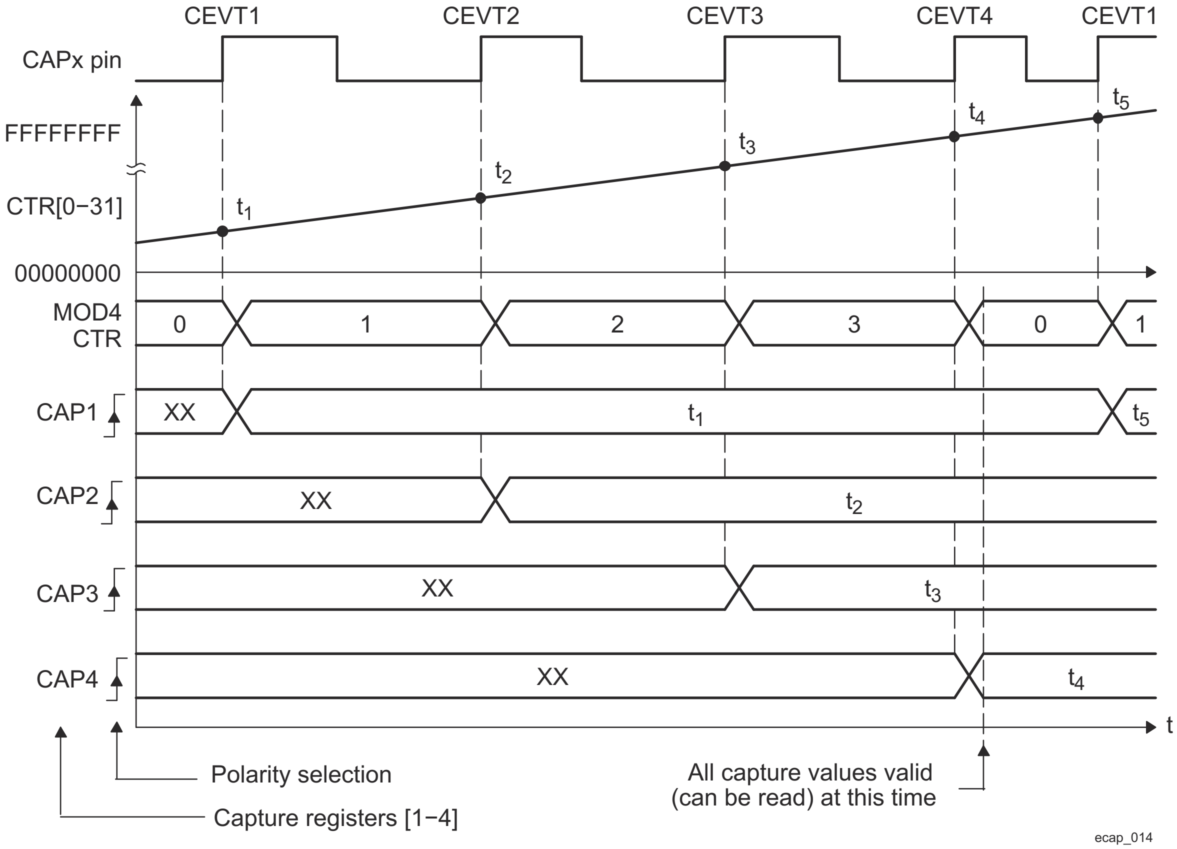

Figure 12-312. Capture Sequence for Absolute Time-Stamp, Rising Edge Detect

Table 12-363. ECAP Initialization for CAP Mode Absolute Time, Rising Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_RISING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_RISING
ECCTL1	CTRRST1	EC_ABS_MODE
ECCTL1	CTRRST2	EC_ABS_MODE
ECCTL1	CTRRST3	EC_ABS_MODE
ECCTL1	CTRRST4	EC_ABS_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for CAP Mode Absolute Time, Rising Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising edge trigger
// Run Time ( e.g. CEVT4 triggered ISR call)
//==========================================
TSt1 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at t1
TSt2 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at t2
TSt3 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at t3
TSt4 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at t4
Period1 = TSt2-TSt1;// Calculate 1st period
Period2 = TSt3-TSt2;// Calculate 2nd period
Period3 = TSt4-TSt3;// Calculate 3rd period
```

12.4.2.5.2 Absolute Time-Stamp Operation Rising and Falling Edge Trigger Example

In Figure 12-313 the ECAP operating mode is almost the same as in the previous section except capture events are qualified as either rising or falling edge, this now gives both period and duty cycle information: Period1 = $t_3 - t_1$, Period2 = $t_5 - t_3$, …etc. Duty Cycle1 (on-time %) = ($t_2 - t_1$) / Period1 x 100%, etc. Duty Cycle1 (off-time %) = ($t_3 - t_2$) / Period1 x 100%, etc.

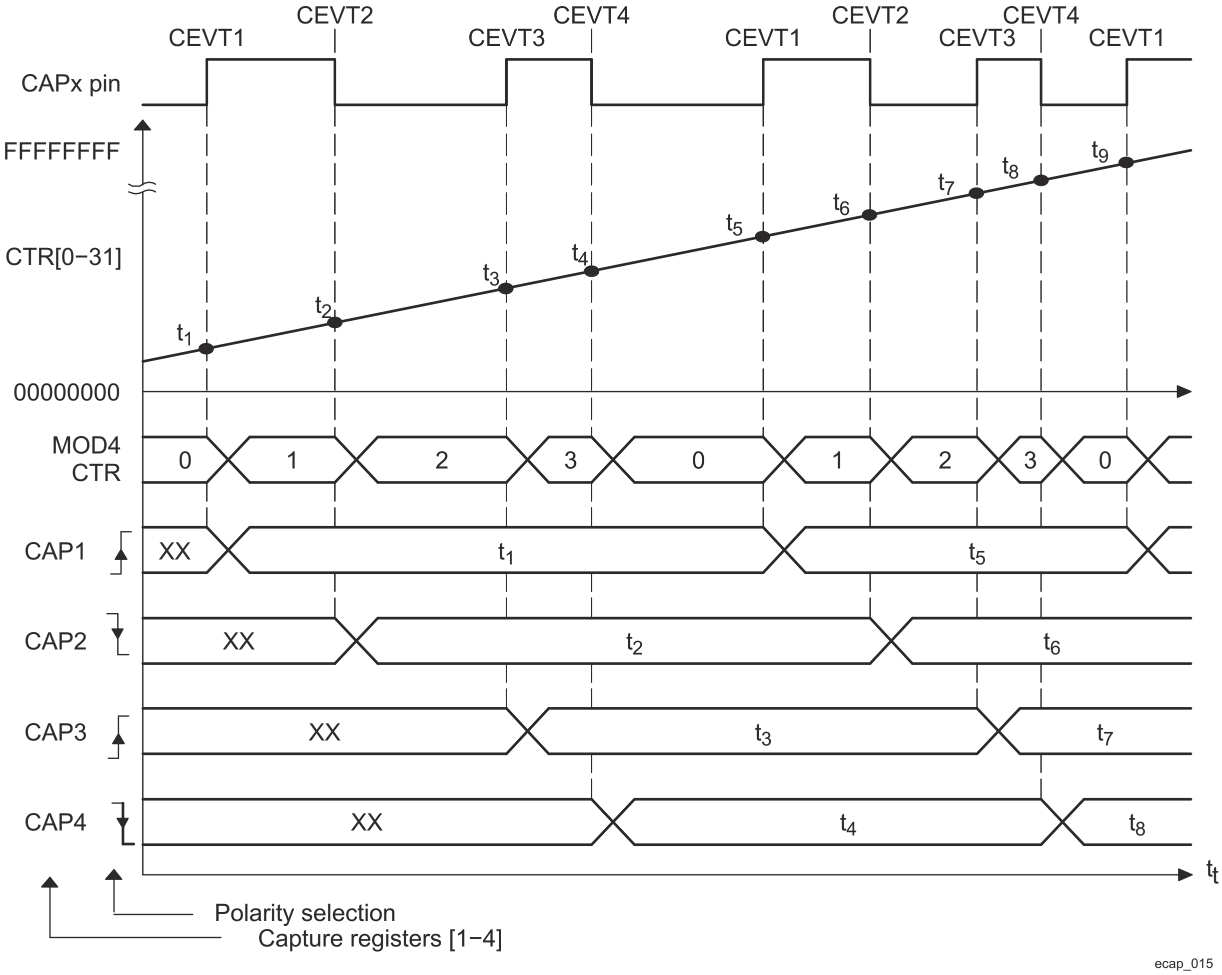

Figure 12-313. Capture Sequence for Absolute Time-Stamp, Rising and Falling Edge Detect

Table 12-364. ECAP Initialization for CAP Mode Absolute Time, Rising and Falling Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_FALLING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_FALLING
ECCTL1	CTRRST1	EC_ABS_MODE
ECCTL1	CTRRST2	EC_ABS_MODE
ECCTL1	CTRRST3	EC_ABS_MODE
ECCTL1	CTRRST4	EC_ABS_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for CAP Mode Absolute Time, Rising and Falling Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising & Falling edge triggers
// Run Time ( e.g. CEVT4 triggered ISR call)
//==========================================
TSt1 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at t1
TSt2 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at t2
TSt3 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at t3
TSt4 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at t4
Period1 = TSt3-TSt1;// Calculate 1st period
DutyOnTime1 = TSt2-TSt1;// Calculate On time
DutyOffTime1 = TSt3-TSt2;// Calculate Off time
```

12.4.2.5.3 Time Difference (Delta) Operation Rising Edge Trigger Example

Figure 12-314 shows how the ECAP module can be used to collect Delta timing data from pulse train waveforms. Here Continuous Capture mode (TSCTR counts-up without resetting, and Mod4 counter wraps around) is used. In Delta-time mode, TSCTR is Reset back to Zero on every valid event. Here Capture events are qualified as Rising edge only. On an event, TSCTR contents (time-stamp) is captured first, and then TSCTR is reset to Zero. The Mod4 counter then increments to the next state. If TSCTR reaches FFFF FFFFh (maximum value), before the next event, it wraps around to 0000 0000h and continues, a CNTOVF_FLG (counter overflow) Flag is set, and an Interrupt (if enabled) occurs. The advantage of Delta-time Mode is that the CAP*n* contents directly give timing data without the need for CPU calculations: Period1 = T_1, Period2 = T_2,…etc. As shown in Figure 12-314, the CEVT1 event is a good trigger point to read the timing data, T_1, T_2, T_3, T_4 are all valid here.

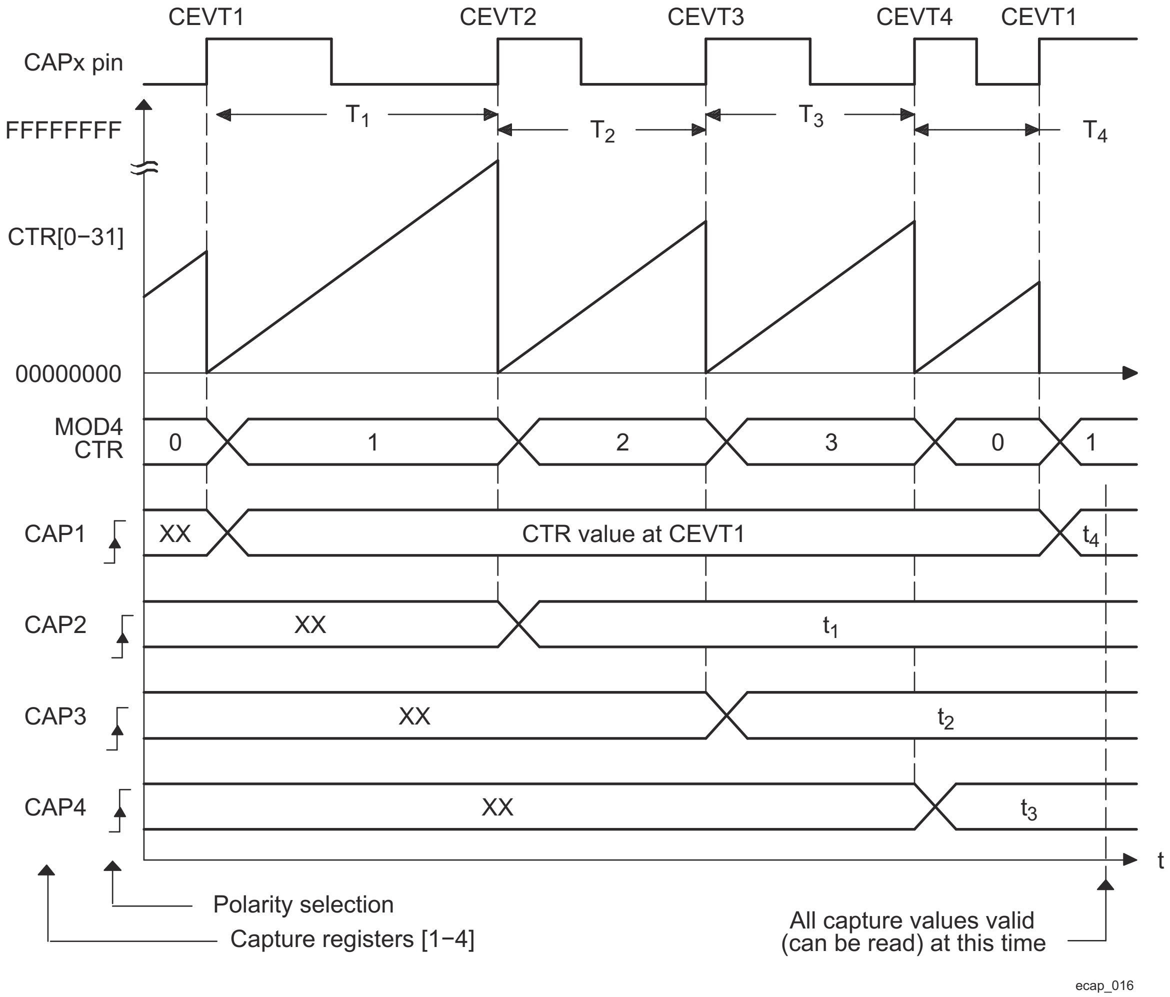

Figure 12-314. Capture Sequence for Delta Mode Time-Stamp, Rising Edge Detect

Table 12-365. ECAP Initialization for CAP Mode Delta Time, Rising Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_RISING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_RISING
ECCTL1	CTRRST1	EC_DELTA_MODE
ECCTL1	CTRRST2	EC_DELTA_MODE
ECCTL1	CTRRST3	EC_DELTA_MODE
ECCTL1	CTRRST4	EC_DELTA_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for CAP Mode Delta Time, Rising Edge Trigger

```
// Code snippet for CAP mode Delta Time, Rising edge trigger
// Run Time ( e.g. CEVT1 triggered ISR call)
//==========================================
// Note: here Time-stamp directly represents the Period value.
Period4 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at T1
Period1 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at T2
Period2 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at T3
Period3 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at T4
```

12.4.2.5.4 Time Difference (Delta) Operation Rising and Falling Edge Trigger Example

In Figure 12-315 the ECAP operating mode is almost the same as in previous section except Capture events are qualified as either Rising or Falling edge, this now gives both Period and Duty cycle information: Period1 = T_1 + T_2, Period2 = T_3 + T_4, …etc Duty Cycle1 (on-time %) = T_1 / Period1 × 100%, etc Duty Cycle1 (off-time %) = T_2 / Period1 × 100%, etc.

During initialization, you must write to the active registers for both period and compare. This will then automatically copy the init values into the shadow values. For subsequent compare updates, that is, during run-time, only the shadow registers must be used.

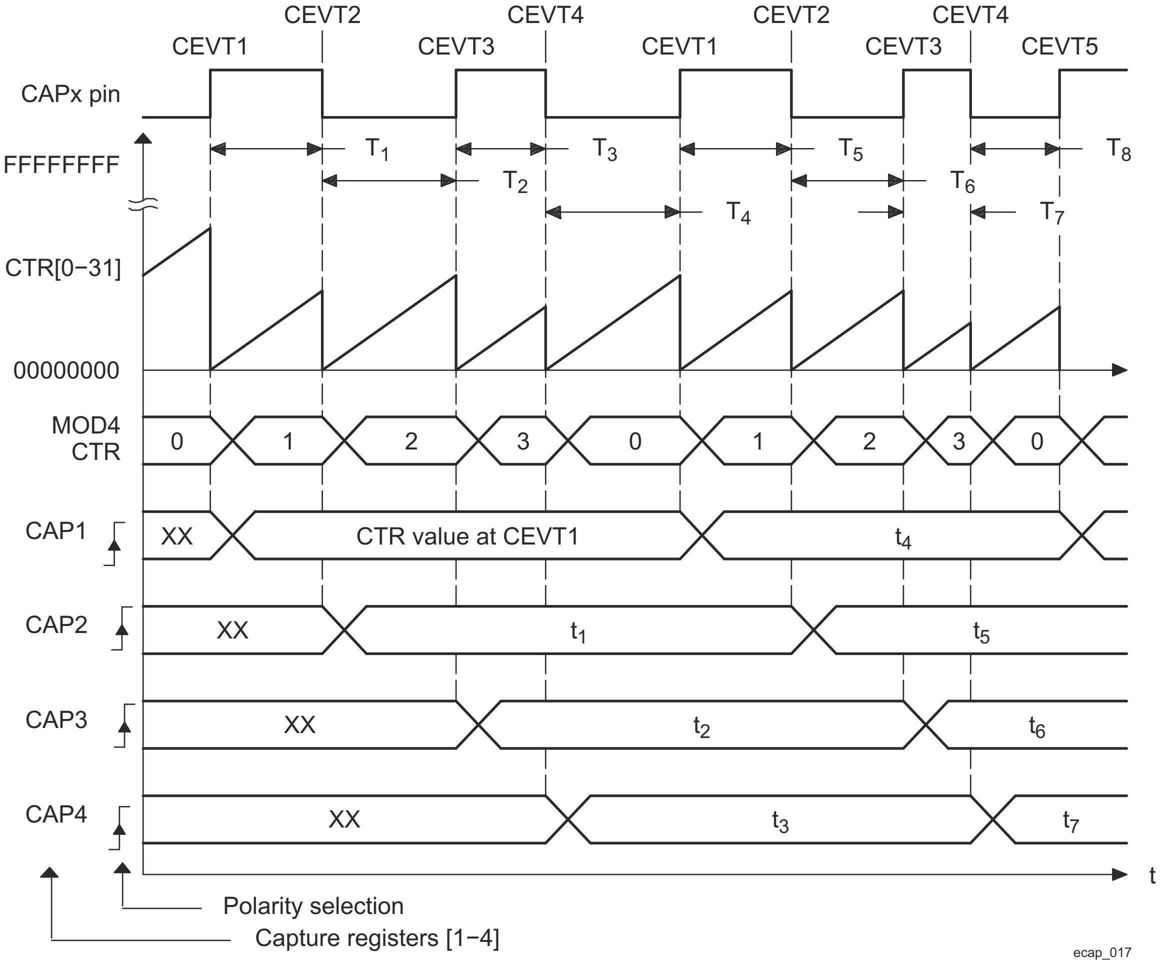

Figure 12-315. Capture Sequence for Delta Mode Time-Stamp, Rising and Falling Edge Detect

Table 12-366. ECAP Initialization for CAP Mode Delta Time, Rising and Falling Edge Triggers

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_FALLING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_FALLING
ECCTL1	CTRRST1	EC_DELTA_MODE
ECCTL1	CTRRST2	EC_DELTA_MODE
ECCTL1	CTRRST3	EC_DELTA_MODE
ECCTL1	CTRRST4	EC_DELTA_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for CAP Mode Delta Time, Rising and Falling Edge Triggers

```
// Code snippet for CAP mode Delta Time, Rising and Falling edge triggers
// Run Time ( e.g. CEVT1 triggered ISR call)
//==========================================
// Note: here Time-stamp directly represents the Duty cycle values.
DutyOnTime1 =  ECAPxRegs.CAP2;// Fetch Time-Stamp captured at T2
DutyOffTime1 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at T3
DutyOnTime2 =  ECAPxRegs.CAP4;// Fetch Time-Stamp captured at T4
DutyOffTime2 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at T1
Period1 = DutyOnTime1 + DutyOffTime1;
Period2 = DutyOnTime2 + DutyOffTime2;
```

12.4.2.5.5 Application of the APWM Mode

12.4.2.5.5.1 Simple PWM Generation (Independent Channel/s) Example

In this example, the ECAP module is configured to operate as a PWM generator. Here a very simple single channel PWM waveform is generated from output pin APWM*n*. The PWM polarity is active high, which means that the compare value (CAP2 reg is now a compare register) represents the on-time (high level) of the period. Alternatively, if the APWMPOL bit is configured for active low, then the compare value represents the off-time.

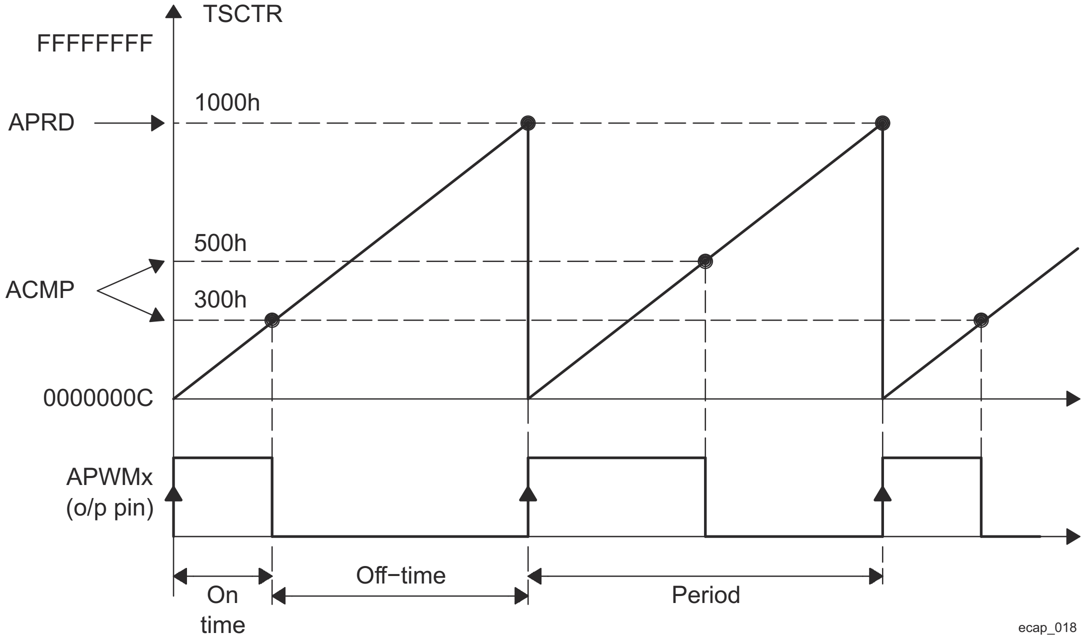

Figure 12-316. PWM Waveform Details of APWM Mode Operation

Table 12-367. ECAP Initialization for APWM Mode

Register	Bit	Value
CAP1	CAP1	0x1000
CTRPHS	CTRPHS	0x0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for APWM Mode

```
// Code snippet for APWM mode Example 1
// Run Time (Instant 1, e.g. ISR call)
//======================
   ECAPxRegs.CAP2 = 0x300;      // Set Duty cycle i.e. compare value
// Run Time (Instant 2, e.g. another ISR call)
//======================
   ECAPxRegs.CAP2 = 0x500;      // Set Duty cycle i.e. compare value
```

12.4.2.5.5.2 Multichannel PWM Generation with Synchronization Example

Figure 12-317 takes advantage of the synchronization feature between the ECAP modules. Here 4 independent PWM channels are required with different frequencies, but at integer multiples of each other to avoid "beat" frequencies. Hence one ECAP module is configured as the Controller and the remaining 3 are Targets all receiving their synch pulse (CTR = PRD) from the controller. Note the Controller is chosen to have the lower frequency (F1 = 1/20,000) requirement. Here Target2 Freq = 2 × F1, Target3 Freq = 4 × F1 and Target4 Freq = 5 × F1. Note here values are in decimal notation. Also, only the APWM1 output waveform is shown.

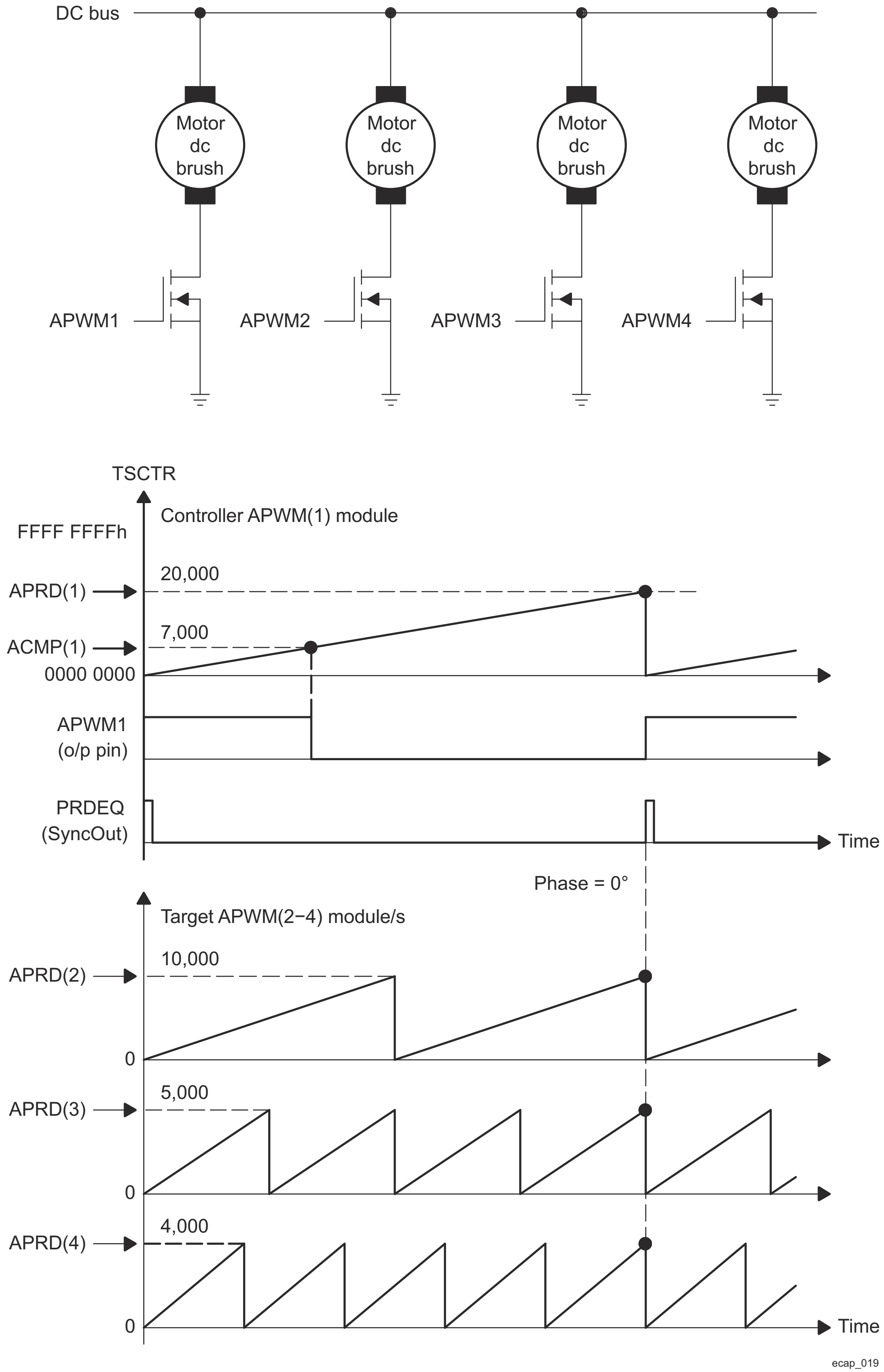

Figure 12-317. Multichannel PWM Example Using 4 ECAP Modules

Table 12-368. ECAP1 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	20000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_CTR_PRD
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-369. ECAP2 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	10000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-370. ECAP3 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	5000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-371. ECAP4 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	4000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for Multichannel PWM Generation with Synchronization

```
// Code snippet for APWM mode Example 2
// Run Time (Note: Example execution of one run-time instant)
//============================================================
   ECAP1Regs.CAP2 = 7000;    // Set Duty cycle i.e., compare value = 7000
   ECAP2Regs.CAP2 = 2000;    // Set Duty cycle i.e., compare value = 2000
   ECAP3Regs.CAP2 = 550;     // Set Duty cycle i.e., compare value = 550
   ECAP4Regs.CAP2 = 6500;    // Set Duty cycle i.e., compare value = 6500
```

12.4.2.5.5.3 Multichannel PWM Generation with Phase Control Example

In Figure 12-318, the Phase control feature of the APWM mode is used to control a 3 phase Interleaved DC/DC converter topology. This topology requires each phase to be off-set by 120° from each other. Hence if "Leg" 1 (controlled by APWM1) is the reference Leg (or phase), that is, 0°, then Leg 2 need 120° off-set and Leg 3 needs 240° off-set. The waveforms in Figure 12-318 show the timing relationship between each of the phases (Legs). Note ECAP1 module is the Controller and issues a SyncOut pulse to the targets (modules 2, 3) whenever TSCTR = Period value.

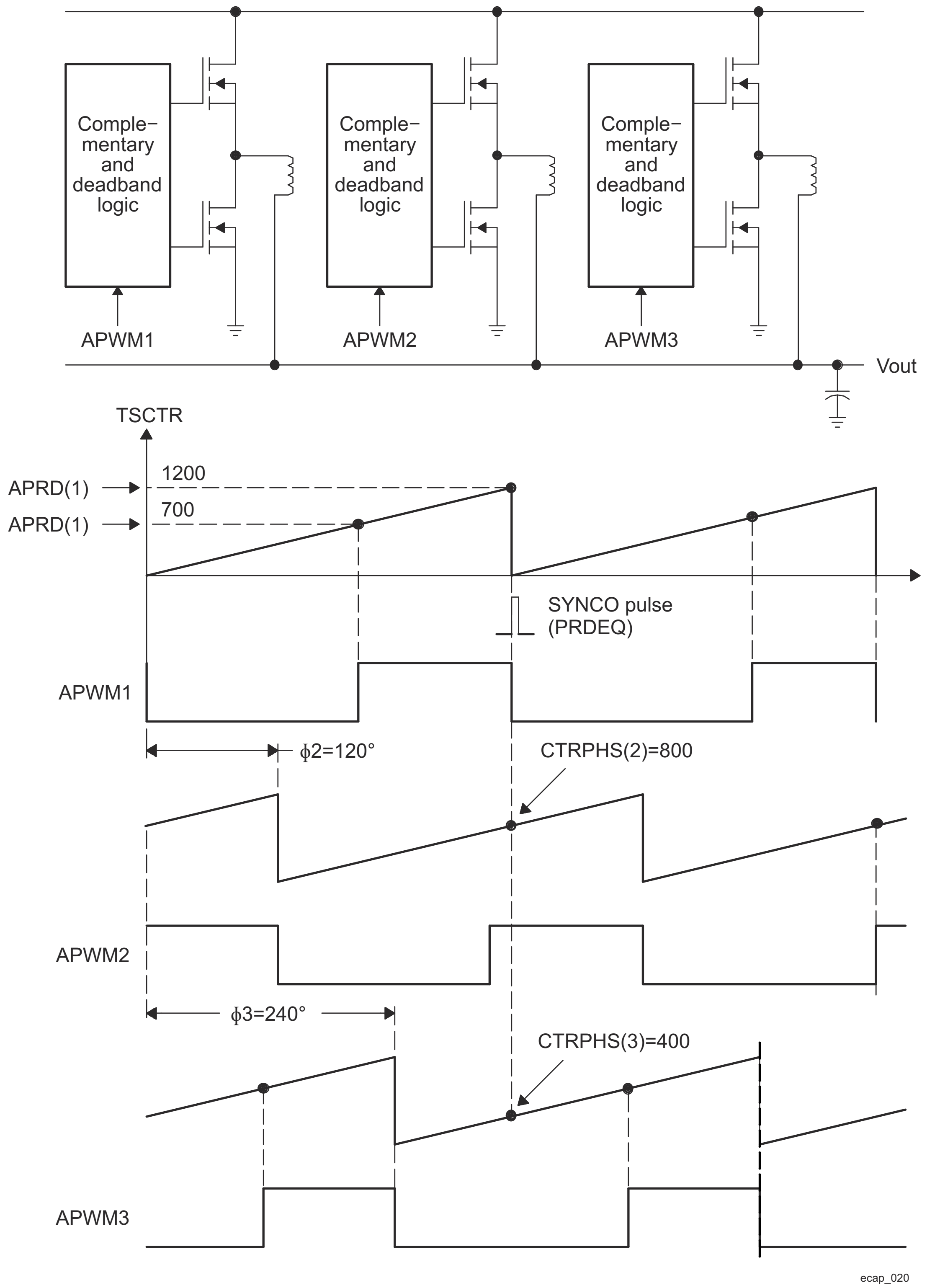

Figure 12-318. Multiphase (channel) Interleaved PWM Example Using 3 ECAP Modules

Table 12-372. ECAP1 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_CTR_PRD
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-373. ECAP2 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	800
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-374. ECAP3 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	400
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Code Snippet for Multichannel PWM Generation with Phase Control

```
// Code snippet for APWM mode Example 3
// Run Time (Note: Example execution of one run-time instant)
//============================================================
// All phases are set to the same duty cycle
  ECAP1Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
  ECAP2Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
  ECAP3Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
```

12.4.3 Enhanced Pulse Width Modulation (EPWM) Module

This chapter describes the Enhanced Pulse Width Modulation (EPWM) module in the device.

12.4.3.1 EPWM Overview

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross-coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single-channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description, the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWMx instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

The EPWM module represents one complete PWM channel composed of two PWM outputs: EPWMxA and EPWMxB.

As also described in Section 12.4.3.3.1.2 , *Daisy-Chain Connectivity between EPWM Modules*, the EPWM modules are chained together via a clock synchronization scheme that allows them to operate as a single system when required. Additionally, this synchronization scheme can be extended to the Enhanced Capture (ECAP) peripheral module. The EPWM modules can also operate stand-alone.

The device has nine instances of the EPWM modules.

Table 12-363 shows the EPWM allocation across device domains.

Table 12-375. EPWM Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
EPWM0	-	✓
EPWM1	-	✓
EPWM2	-	✓
EPWM3	-	✓
EPWM4	-	✓
EPWM5	-	✓
EPWM6	-	✓
EPWM7	-	✓
EPWM8	-	✓

Figure 12-319 shows the EPWM module overview.

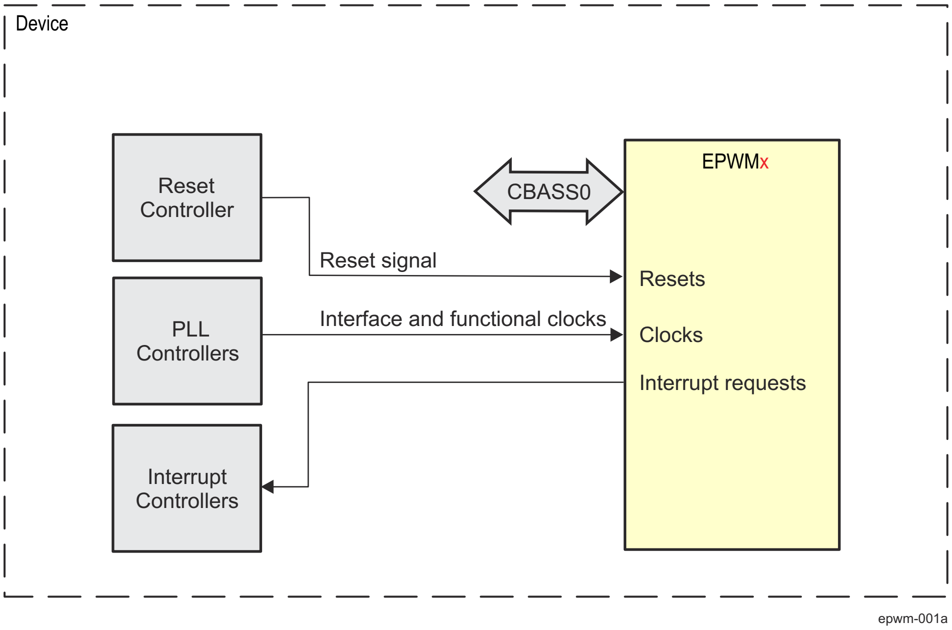

Note

x = 0 to 8

Figure 12-319. EPWM Overview

12.4.3.1.1 EPWM Features

Each EPWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Allows events to trigger both CPU interrupts and ADC start of conversions
- Programmable event prescaling minimizes CPU overhead on interrupts
- PWM chopping by a high-frequency carrier signal, useful for pulse transformer gate drives

12.4.3.1.2 EPWM Not Supported Features

- EPWM digital comparator modules
- EPWM High-resolution module

12.4.3.1.3 Multiple EPWM Module Details

Each EPWM module is connected to the input/output signals shown in Figure 12-320.

The order in which the EPWM modules are connected may differ from what is shown in Figure 12-320. See Section 12.4.3.3.1.2 , *Daisy-Chain Connectivity between EPWM Modules* for the actual synchronization scheme implemented in the device. Each EPWM module consists of seven submodules and is connected within a system via the signals shown in Figure 12-321.

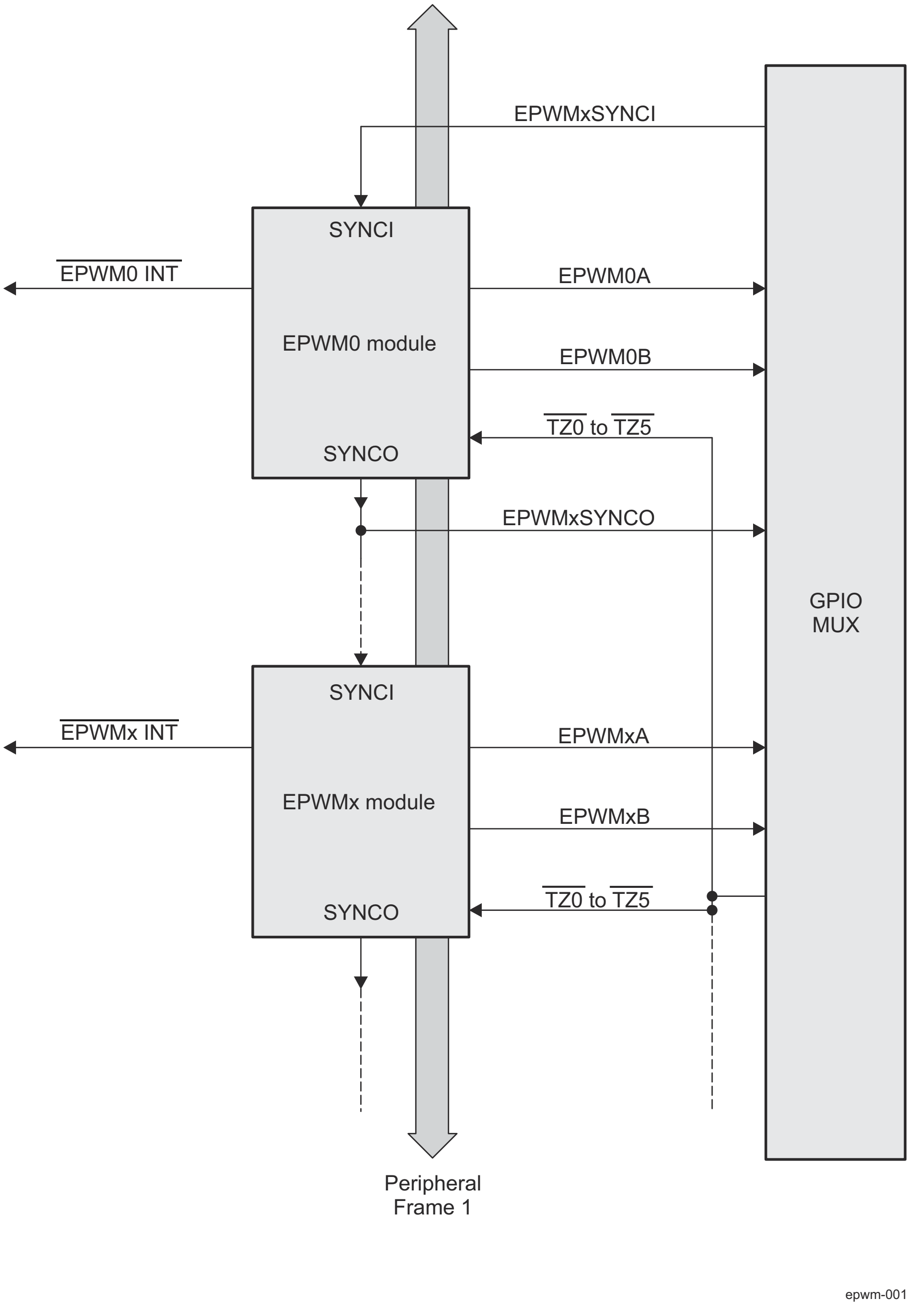

Note

x = 0 to 8

Figure 12-320. Multiple EPWM Modules

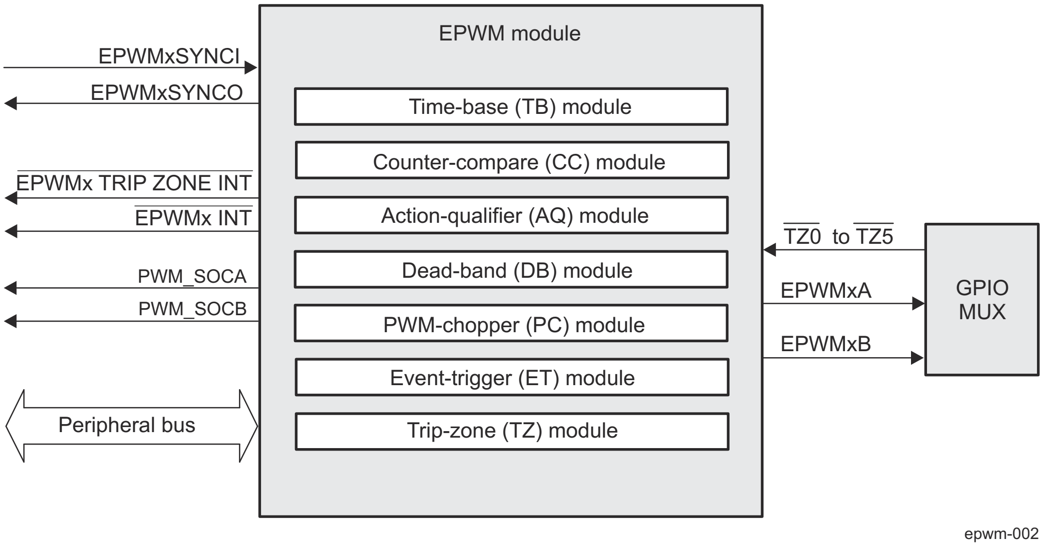

Note

x = 0 to 8

Figure 12-321. Submodules and Signal Connections for an EPWM Module

Figure 12-322 shows more internal details of a single EPWM module.

The main signals used by the EPWM module are:

- **PWM output signals (EPWMxA and EPWMxB)**
  The PWM output signals are available external to the device through the GPIO peripheral.
- **Trip-zone signals ($\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$)**
  These input signals alert the EPWM module of an external fault condition. Each module on a device can be configured to either use or ignore any of the trip-zone signals. The trip-zone signal can be configured as an asynchronous input through the GPIO peripheral.
- **Time-base synchronization input (EPWMxSYNCI) and output (EPWMxSYNCO) signals**
  The synchronization signals daisy chain the EPWM modules together. Each module can be configured to either use or ignore its synchronization input. For more information see Section 12.4.3.3.1.2 , *Daisy-Chain Connectivity between EPWM Modules*.
- **ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB)**
  Each EPWM module has two ADC start of conversion signals (one for each sequencer). Any EPWM module can trigger a start of conversion for either sequencer. Which event triggers the start of conversion is configured in the Event-Trigger submodule of the EPWM module.
- **Peripheral Bus**
  The peripheral bus is 32-bits wide and allows both 16-bit and 32-bit writes to the EPWM registers.

Figure 12-322 also shows the key internal submodule interconnect signals. Each submodule is described in Section 12.4.3.4 , *EPWM Functional Description*.

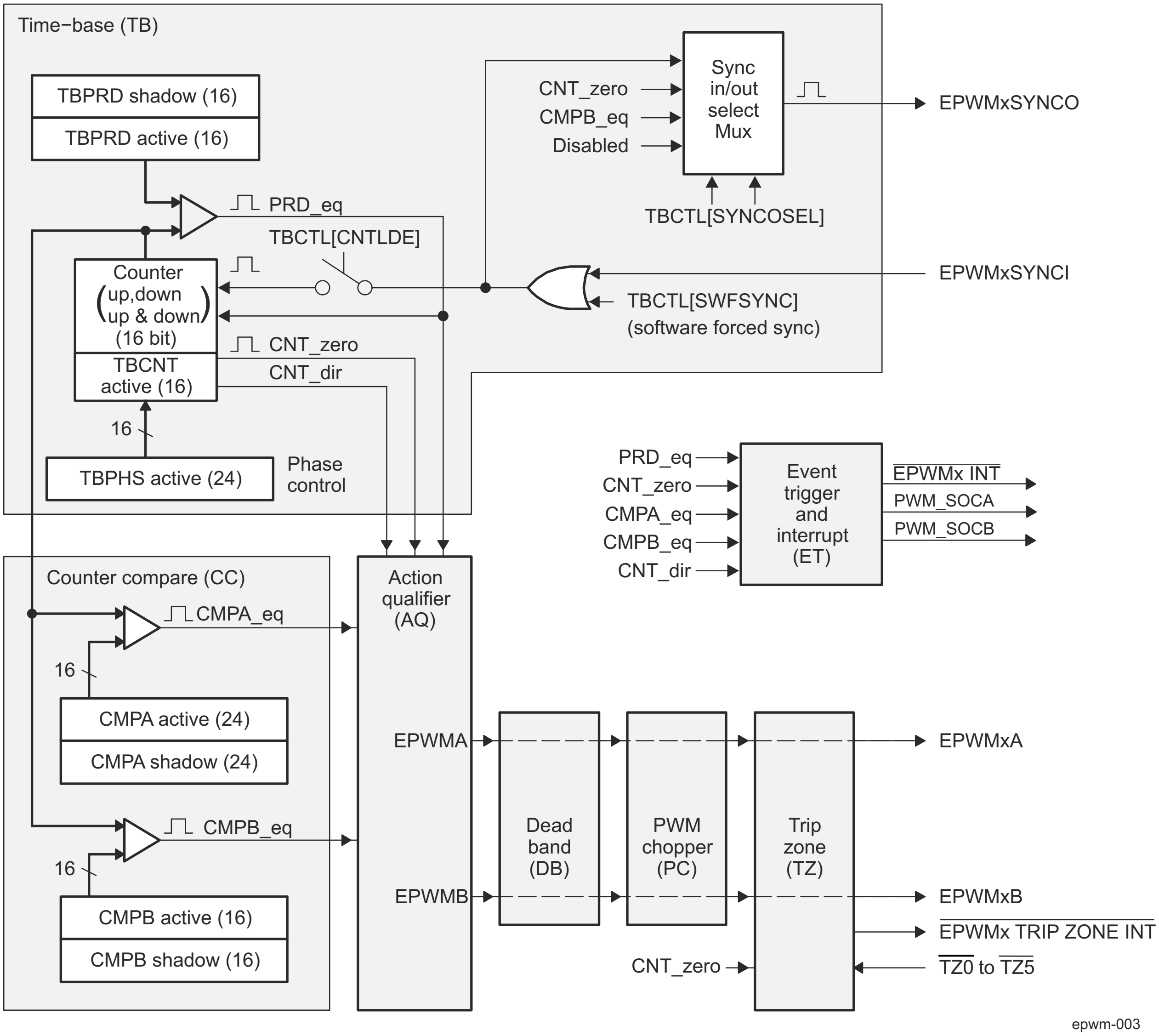

Figure 12-322. EPWM Submodule Interconnect Signals

12.4.3.2 EPWM Environment

The EPWMx (where x = 0 to 8) module is hereinafter referred to as EPWM module.

This section describes the EPWM external connections (environment).

Figure 12-323 shows the EPWM I/O interface signals.

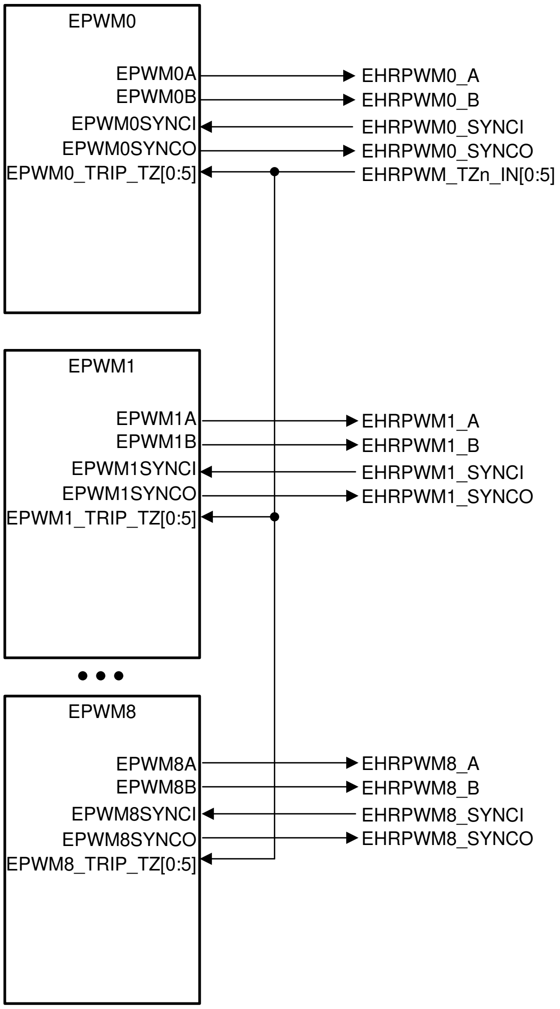

Figure 12-323. EPWM I/O Interface Signals

Table 12-364 describes the EPWM I/O signals.

Table 12-376. EPWM I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
		EPWM0		
EPWM0A	EHRPWM0_A	O	EPWM0 output A	0x0
EPWM0B	EHRPWM0_B	O	EPWM0 output B	0x0
EPWM0SYNCI	EHRPWM0_SYNCI	I	EPWM0 Sync input	HiZ
EPWM0SYNCO	EHRPWM0_SYNCO	O	EPWM0 Sync output	0x0
EPWM0_TRIP_TZ[0:5]	EHRPWM_TZn_IN[0:5]	I	EPWM0 TripZone input	HiZ
		EPWM1		
EPWM1A	EHRPWM1_A	O	EPWM1 output A	0x0
EPWM1B	EHRPWM1_B	O	EPWM1 output B	0x0

Table 12-376. EPWM I/O Signals (continued)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
EPWM1SYNCI(3)	EHRPWM1_SYNCI(3)	I	EPWM1 Sync input	HiZ
EPWM1SYNCO(3)	EHRPWM1_SYNCO(3)	O	EPWM1 Sync output	0x0
$\overline{\text{EPWM1\_TRIP\_TZ[0:5]}}$	EHRPWM_TZn_IN[0:5]	I	EPWM1 TripZone input	HiZ
EPWM2				
EPWM2A	EHRPWM2_A	O	EPWM2 output A	0x0
EPWM2B	EHRPWM2_B	O	EPWM2 output B	0x0
EPWM2SYNCI(3)	EHRPWM2_SYNCI(3)	I	EPWM2 Sync input	HiZ
EPWM2SYNCO(3)	EHRPWM2_SYNCO(3)	O	EPWM2 Sync output	0x0
$\overline{\text{EPWM2\_TRIP\_TZ[0:5]}}$	EHRPWM_TZn_IN[0:5]	I	EPWM2 TripZone input	HiZ
EPWM3				
EPWM3A	EHRPWM3_A	O	EPWM3 output A	0x0
EPWM3B	EHRPWM3_B	O	EPWM3 output B	0x0
EPWM3SYNCI	EHRPWM3_SYNCI	I	EPWM3 Sync input	HiZ
EPWM3SYNCO	EHRPWM3_SYNCO	O	EPWM3 Sync output	0x0
$\overline{\text{EPWM3\_TRIP\_TZ[0:5]}}$	EHRPWM_TZn_IN[0:5]	I	EPWM3 TripZone input	HiZ
EPWM4				
EPWM4A	EHRPWM4_A	O	EPWM4 output A	0x0
EPWM4B	EHRPWM4_B	O	EPWM4 output B	0x0
EPWM4SYNCI(3)	EHRPWM4_SYNCI(3)	I	EPWM4 Sync input	HiZ
EPWM4SYNCO(3)	EHRPWM4_SYNCO(3)	O	EPWM4 Sync output	0x0
$\overline{\text{EPWM4\_TRIP\_TZ[0:5]}}$	EHRPWM_TZn_IN[0:5]	I	EPWM4 TripZone input	HiZ
EPWM5				
EPWM5A	EHRPWM5_A	O	EPWM5 output A	0x0
EPWM5B	EHRPWM5_B	O	EPWM5 output B	0x0
EPWM5SYNCI(3)	EHRPWM5_SYNCI(3)	I	EPWM5 Sync input	HiZ
EPWM5SYNCO(3)	EHRPWM5_SYNCO(3)	O	EPWM5 Sync output	0x0
$\overline{\text{EPWM5\_TRIP\_TZ[0:5]}}$	EHRPWM_TZn_IN[0:5]	I	EPWM5 TripZone input	HiZ
EPWM6				
EPWM6A	EHRPWM6_A	O	EPWM6 output A	0x0
EPWM6B	EHRPWM6_B	O	EPWM6 output B	0x0
EPWM6SYNCI	EHRPWM6_SYNCI	I	EPWM6 Sync input	HiZ
EPWM6SYNCO	EHRPWM6_SYNCO	O	EPWM6 Sync output	0x0
$\overline{\text{EPWM6\_TRIP\_TZ[0:5]}}$	EHRPWM_TZn_IN[0:5]	I	EPWM6 TripZone input	HiZ
EPWM7				
EPWM7A	EHRPWM7_A	O	EPWM7 output A	0x0
EPWM7B	EHRPWM7_B	O	EPWM7 output B	0x0
EPWM7SYNCI(3)	EHRPWM7_SYNCI(3)	I	EPWM7 Sync input	HiZ
EPWM7SYNCO(3)	EHRPWM7_SYNCO(3)	O	EPWM7 Sync output	0x0
$\overline{\text{EPWM7\_TRIP\_TZ[0:5]}}$	EHRPWM_TZn_IN[0:5]	I	EPWM7 TripZone input	HiZ
EPWM8				
EPWM8A	EHRPWM8_A	O	EPWM8 output A	0x0
EPWM8B	EHRPWM8_B	O	EPWM8 output B	0x0
EPWM8SYNCI(3)	EHRPWM8_SYNCI(3)	I	EPWM8 Sync input	HiZ
EPWM8SYNCO(3)	EHRPWM8_SYNCO(3)	O	EPWM8 Sync output	0x0

Table 12-376. EPWM I/O Signals (continued)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
EPWM8_TRIP_TZ[0:5]	EHRPWM_TZn_IN[0:5]	I	EPWM8 TripZone input	HiZ
EPWM Start of Conversion				
PWM_SOCA	EHRPWM_SOCA	O	EPWM start of conversion output A	HiZ
PWM_SOCB	EHRPWM_SOCB	O	EPWM start of conversion output B	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) Not an external pin. See Daisy-Chain Connectivity between EPWM Modules

---

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.4.3.3 EPWM Integration

This section describes the EPWM module integration in the device, including information about clocks, resets, and hardware requests.

Figure 12-324 shows the EPWM integration.

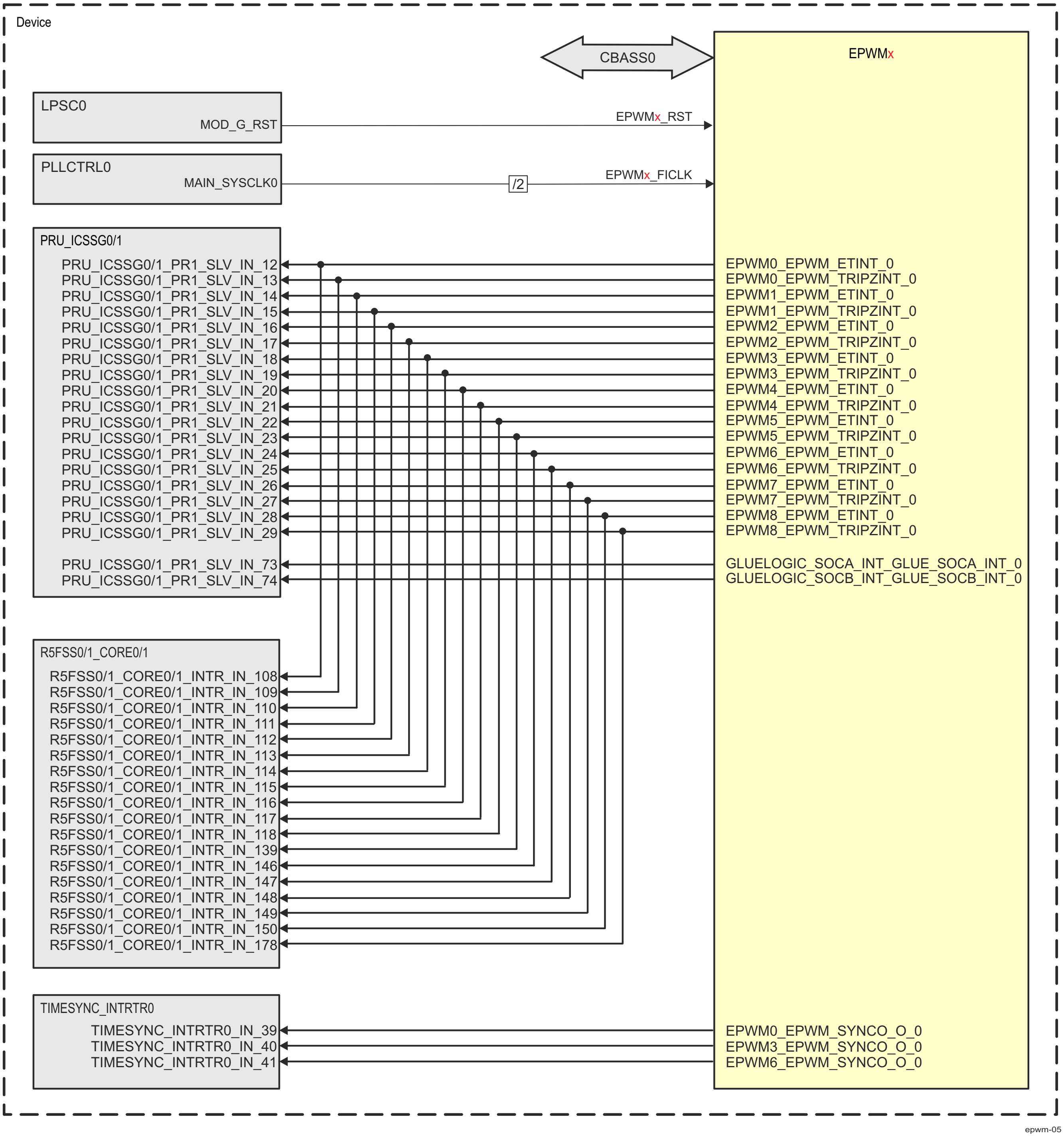

Note

x = 0 to 8

Figure 12-324. EPWM Integration

Table 12-365 through Table 12-368 summarize the integration of the EPWM module in the device.

Table 12-377. EPWM Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
EPWM0	PSC0	PD0	LPSC0	CBASS0
EPWM1	PSC0	PD0	LPSC0	CBASS0
EPWM2	PSC0	PD0	LPSC0	CBASS0
EPWM3	PSC0	PD0	LPSC0	CBASS0
EPWM4	PSC0	PD0	LPSC0	CBASS0
EPWM5	PSC0	PD0	LPSC0	CBASS0
EPWM6	PSC0	PD0	LPSC0	CBASS0
EPWM7	PSC0	PD0	LPSC0	CBASS0
EPWM8	PSC0	PD0	LPSC0	CBASS0

Table 12-378. EPWM Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
EPWM0	EPWM0_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM0 functional and interface clock
EPWM1	EPWM1_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM1 functional and interface clock
EPWM2	EPWM2_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM2 functional and interface clock
EPWM3	EPWM3_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM3 functional and interface clock
EPWM4	EPWM4_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM4 functional and interface clock
EPWM5	EPWM5_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM5 functional and interface clock
EPWM6	EPWM6_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM6 functional and interface clock
EPWM7	EPWM7_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM7 functional and interface clock
EPWM8	EPWM8_FICLK	MAIN_SYSCLK0/2	PLLCTRL0	EPWM8 functional and interface clock

Table 12-379. EPWM Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
EPWM0	EPWM0_RST	MOD_G_RST	LPSC0	Module Reset
EPWM1	EPWM1_RST	MOD_G_RST	LPSC0	Module Reset
EPWM2	EPWM2_RST	MOD_G_RST	LPSC0	Module Reset
EPWM3	EPWM3_RST	MOD_G_RST	LPSC0	Module Reset
EPWM4	EPWM4_RST	MOD_G_RST	LPSC0	Module Reset
EPWM5	EPWM5_RST	MOD_G_RST	LPSC0	Module Reset
EPWM6	EPWM6_RST	MOD_G_RST	LPSC0	Module Reset
EPWM7	EPWM7_RST	MOD_G_RST	LPSC0	Module Reset
EPWM8	EPWM8_RST	MOD_G_RST	LPSC0	Module Reset

Table 12-380. EPWM Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
EPWM0	EPWM0_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_12	PRU_ICSSG0	EPWM0 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_12	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_108	R5FSS0_CORE0		

Table 12-380. EPWM Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		R5FSS0_CORE1_INTR_IN_108	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_108	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_108	R5FSS1_CORE1		
	EPWM0_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_13	PRU_ICSSG0	EPWM0 Tripzone interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_13	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_109	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_109	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_109	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_109	R5FSS1_CORE1		
EPWM1	EPWM1_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_14	PRU_ICSSG0	EPWM1 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_14	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_110	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_110	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_110	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_110	R5FSS1_CORE1		
	EPWM1_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_15	PRU_ICSSG0	EPWM1 Tripzone interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_15	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_111	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_111	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_111	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_111	R5FSS1_CORE1		
EPWM2	EPWM2_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_16	PRU_ICSSG0	EPWM2 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_16	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_112	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_112	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_112	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_112	R5FSS1_CORE1		
	EPWM2_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_17	PRU_ICSSG0	EPWM2 Tripzone interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_17	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_113	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_113	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_113	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_113	R5FSS1_CORE1		
EPWM3	EPWM3_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_18	PRU_ICSSG0	EPWM3 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_18	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_114	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_114	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_114	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_114	R5FSS1_CORE1		
	EPWM3_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_19	PRU_ICSSG0	EPWM3 Tripzone interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_19	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_115	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_115	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_115	R5FSS1_CORE0		

Table 12-380. EPWM Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		R5FSS1_CORE1_INTR_IN_115	R5FSS1_CORE1		
EPWM4	EPWM4_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_20	PRU_ICSSG0	EPWM4 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_20	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_116	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_116	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_116	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_116	R5FSS1_CORE1		
	EPWM4_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_21	PRU_ICSSG0	EPWM4 Tripzone interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_21	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_117	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_117	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_117	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_117	R5FSS1_CORE1		
EPWM5	EPWM5_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_22	PRU_ICSSG0	EPWM5 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_22	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_118	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_118	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_118	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_118	R5FSS1_CORE1		
	EPWM5_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_23	PRU_ICSSG0	EPWM5 Tripzone interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_23	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_139	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_139	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_139	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_139	R5FSS1_CORE1		
EPWM6	EPWM6_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_24	PRU_ICSSG0	EPWM6 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_24	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_146	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_146	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_146	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_146	R5FSS1_CORE1		
	EPWM6_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_25	PRU_ICSSG0	EPWM6 Tripzone interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_25	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_147	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_147	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_147	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_147	R5FSS1_CORE1		
EPWM7	EPWM7_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_26	PRU_ICSSG0	EPWM7 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_26	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_148	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_148	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_148	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_148	R5FSS1_CORE1		
	EPWM7_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_27	PRU_ICSSG0	EPWM7 Tripzone interrupt	Pulse

Table 12-380. EPWM Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		PRU_ICSSG1_PR1_SLV_IN_27	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_149	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_149	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_149	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_149	R5FSS1_CORE1		
EPWM8	EPWM8_EPWM_ETINT_0	PRU_ICSSG0_PR1_SLV_IN_28	PRU_ICSSG0	EPWM8 interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_28	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_150	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_150	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_150	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_150	R5FSS1_CORE1		
	EPWM8_EPWM_TRIPZINT_0	PRU_ICSSG0_PR1_SLV_IN_29	PRU_ICSSG0	EPWM8 Tripzone interrupt	Pulse
		PRU_ICSSG1_PR1_SLV_IN_29	PRU_ICSSG1		
		R5FSS0_CORE0_INTR_IN_178	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_178	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_178	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_178	R5FSS1_CORE1		
EPWMx (x = 0 to 8)	GLUELOGIC_SOCA_INT_GLUE_SOCA_INT_0	PRU_ICSSG0_PR1_SLV_IN_73	PRU_ICSSG0	EPWM Start of Conversion A event	Pulse
		PRU_ICSSG1_PR1_SLV_IN_73	PRU_ICSSG1		
	GLUELOGIC_SOCB_INT_GLUE_SOCB_INT_0	PRU_ICSSG0_PR1_SLV_IN_74	PRU_ICSSG0	EPWM Start of Conversion B event	Pulse
		PRU_ICSSG1_PR1_SLV_IN_74	PRU_ICSSG1		

Table 12-381. EPWM Time Sync Events

Module Instance	Module Sync Output	Destination Sync Input	Destination	Description	Type
EPWM0	EPWM0_EPWM_SYNCO_O_0	TIMESYNC_INTRTR0_IN_39	TIMESYNC_INTRTR0	EPWM0 Sync event	Pulse
EPWM3	EPWM3_EPWM_SYNCO_O_0	TIMESYNC_INTRTR0_IN_40	TIMESYNC_INTRTR0	EPWM3 Sync event	Pulse
EPWM6	EPWM6_EPWM_SYNCO_O_0	TIMESYNC_INTRTR0_IN_41	TIMESYNC_INTRTR0	EPWM6 Sync event	Pulse

Note

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.4.3.3.1 EPWM Additional Integration Details

12.4.3.3.1.1 EPWM Tripzone Connectivity

Each EPWM supports 6 tripzone event inputs and each of those inputs from all the EPWMs are tied to a common tripzone input pin so that any EPWM can be triggered by any of the six tripzone inputs as shown in Figure 12-325.

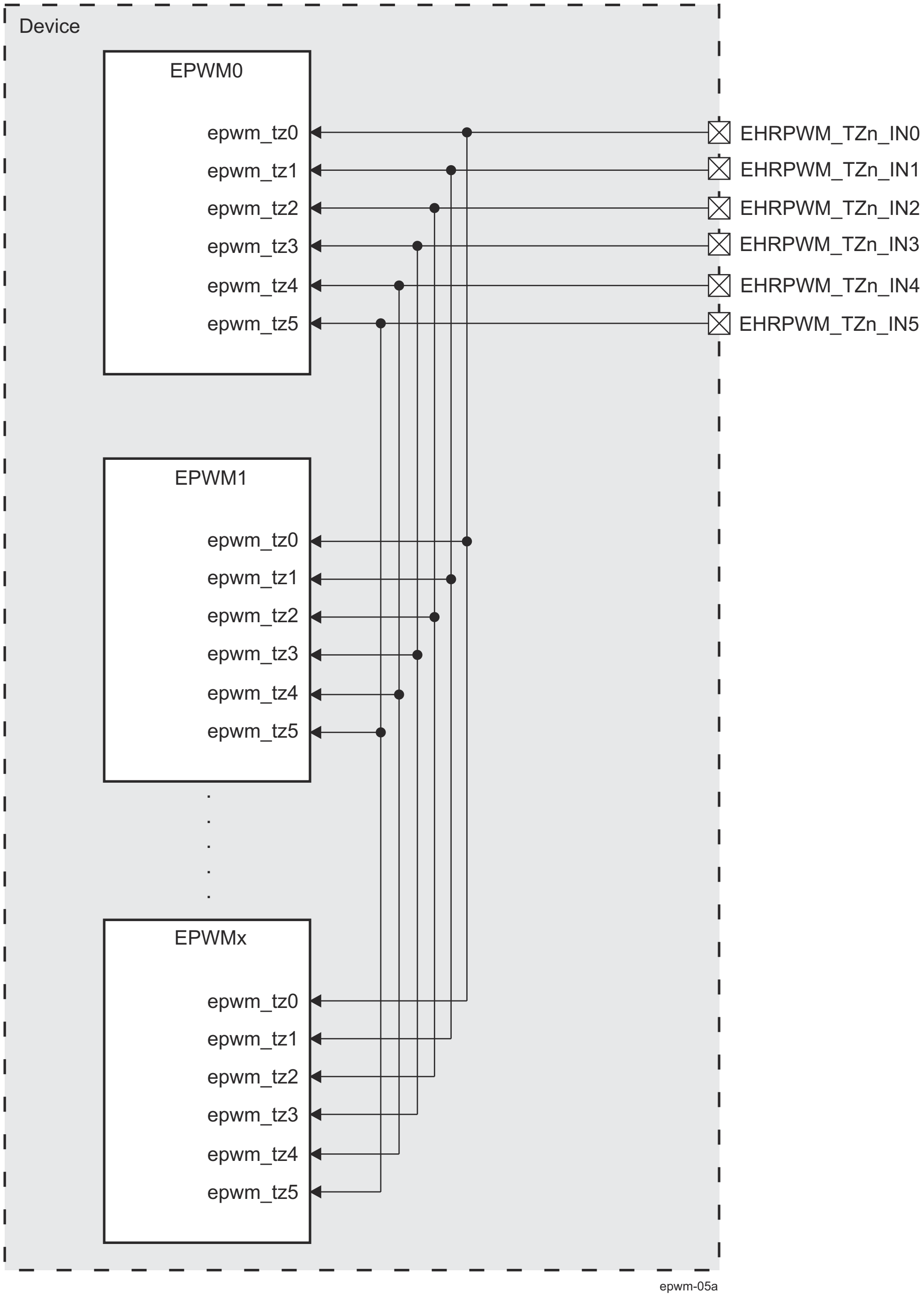

Note

x = 0 to 8

Figure 12-325. EPWM Tripzone Connectivity Detail

12.4.3.3.1.2 Daisy-Chain Connectivity between EPWM Modules

The EPWM modules provide synchronization signals to allow them to be synchronized to other modules or events. In this device, these signals are connected in a daisy-chain fashion for EPWM0-EPWM8 as shown in Figure 12-326. For EPWM3, EPWM4, EPWM5 and for EPWM6, EPWM7, EPWM8, the EPWM modules can be synchronized to a separate external event (routed through the SoC Sync mux3 and SoC Sync mux 6). Note that the EPWM0_SYNCIN, EPWM3_SYNCIN, and EPWM6_SYNCIN pins and the ICSSG interrupts that source the EPWMSYNCI inputs require synchronization. Also note that there can be no extra delay (synchronization or pipelining) between the EPWMSYNCOUT of one EPWM module and the EPWMSYNCI of the next, because this will induce a slight phase shift between the counters of the EPWM peripherals. The connections from the time sync and compare event routers are intended to reset the EPWM timebase counters for synchronization of the PWM output period to (some multiple of) an external synchronization pulse (for example: from a time synchronized network).

Note

The EPWM0 EPWM0SYNCI signal (device EHRPWM0_SYNCI input signal) triggers the event of the EPWM0 Phase Register being loaded into the Counter register (TBPHS -> TBCNT). This event is synchronous to the EPWM0 time-base clock (TBCLK).

The EPWM0 EPWM0SYNCO (device EHRPWM0_SYNCO output signal) is implicitly synchronous to the time-base clock, as this signal has a programmable source of event (in the EPWM_TBCTL[5-4] SYNCOSEL bit field) triggered synchronously to the EPWM0 TBCLK.

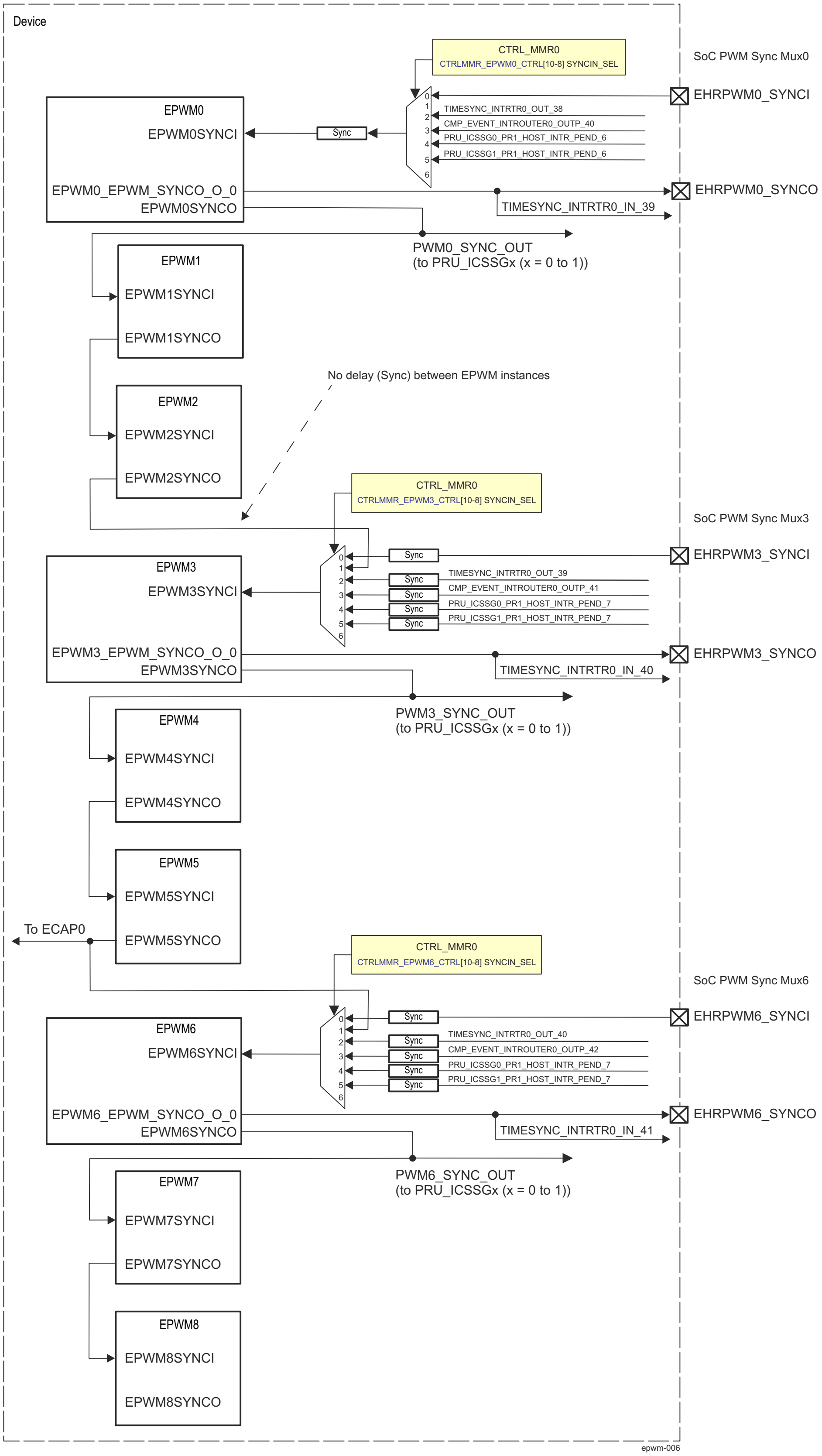

Figure 12-326. Daisy-Chain Connectivity between EPWM Modules

12.4.3.3.1.3 ADC start of conversion signals (PWM_SOCA and PWM_SOCB)

Each EPWM module provides start of conversion events (PWM_SOCA and PWM_SOCB), that can be used to start conversion of external ADC module. In this device all PWM_SOCA and all PWM_SOCB events are ORed together and hence any of the EPWMs can initiate an ADC start of conversion. These events are then multiplexed with an PRU_ICSSG[0-1] host interrupts (ICSSG_x_HOST_INTn, where x = 0 to 1 and n = 1 or 2), allowing either PRU_ICSSG[0-1] or EPWM0 through EPWM8 modules to trigger the PWM_SOCA/PWM_SOCB event pins (EHRPWM_SOCA and EHRPWM_SOCB). The PWM_SOCA and PWM_SOCB event output signals are also routed back to the PRU_ICSSGx (where x = 0 to 1) modules as interrupts as shown in Figure 12-327.

Note

ICSSG_x_HOST_INTn (where x = 0 to 1 and n = 1 or 2) interrupts are mapped to Host-3 and Host-4 of the PRU_ICSSG Interrupt Controller.

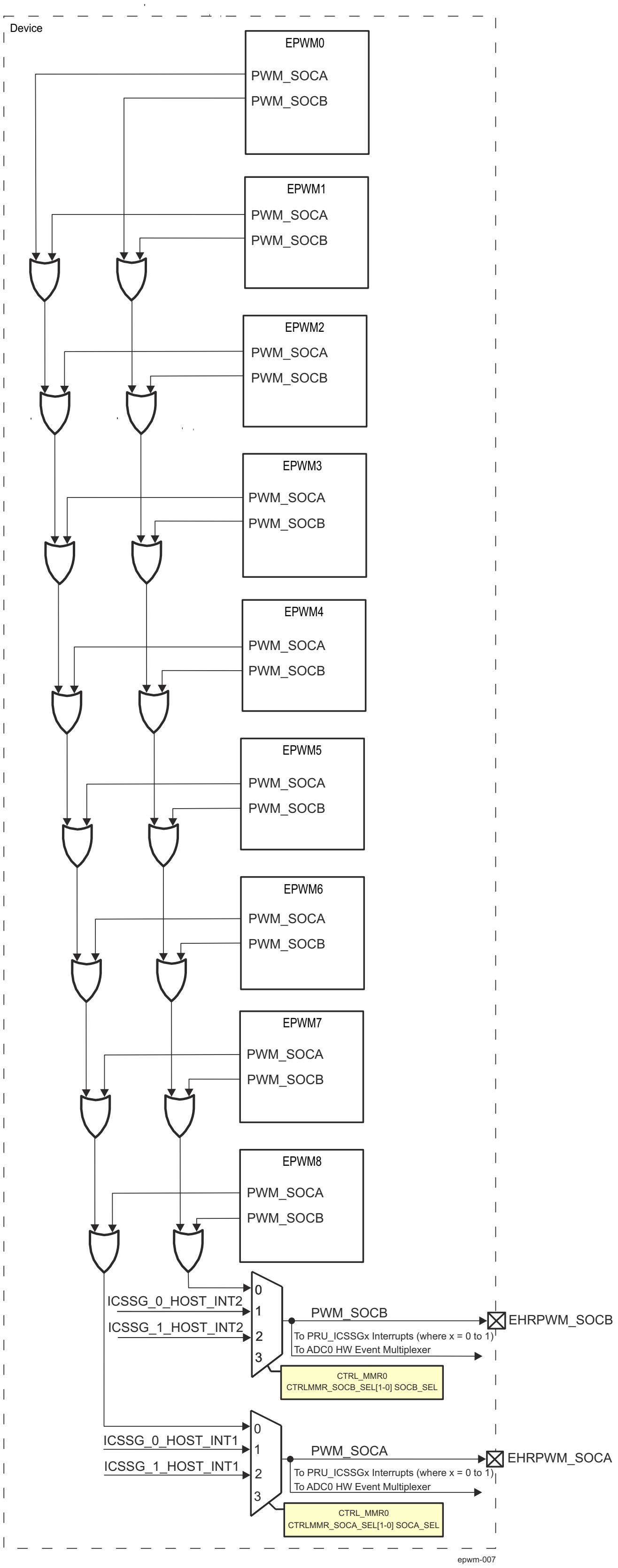

Figure 12-327. Interconnectivity of ADC Start of Conversion

12.4.3.3.1.4 EPWM Modules Time-Base Clock Gating

Each EPWM module has an EPWM TBCLKEN module input used to individually **enable / disable** its EPWM time-base clock. The EPWM time-base clock enable input comes from the MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN bits 0 to 8 in CTRL_MMR0 module, as seen in Table 12-370.

Table 12-382. EPWMn_TB_CLKEN bits

Instance	Bit	Register
EPWM0	0	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN
EPWM1	1	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN
EPWM2	2	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN
EPWM3	3	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN
EPWM4	4	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN
EPWM5	5	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN
EPWM6	6	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN
EPWM7	7	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN
EPWM8	8	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN

This individual TBCLKEN control can be used to align the EPWM time-base clock. The EPWMn_TB_CLKEN bit set to 0h, holds the TBCLK generation counter in its reset state. When EPWMn_TB_CLKEN is set to 1h, then the TBCLK generation counter is allowed to count.

12.4.3.4 EPWM Functional Description

8 submodules are included in each EPWM peripheral. Each of these submodules performs specific tasks that can be configured by software.

12.4.3.4.1 EPWM Submodule Features

Table 12-371 lists the seven key submodules together with a list of their main configuration parameters.

Table 12-383. Submodule Configuration Parameters

Submodule	Configuration Parameter or Option
Time-base (TB)	• Scale the time-base clock (TBCLK) relative to the system clock (FICLK). • Configure the PWM time-base counter (TBCNT) frequency or period. • Time-base counter mode selection: – count-up mode: used for asymmetric PWM – count-down mode: used for asymmetric PWM – count-up-and-down mode: used for symmetric PWM • Configure the time-base phase relative to another EPWM module. • Synchronize the time-base counter between modules through hardware or software. • Configure the direction (up or down) of the time-base counter after a synchronization event. • Configure how the time-base counter will behave when the device is halted by an emulator. • Specify the source for the synchronization output of the EPWM module: – Synchronization input signal – Time-base counter equal to zero – Time-base counter equal to counter-compare B (CMPB) – No output synchronization signal generated
Counter-compare (CC)	• Specify the PWM duty cycle for output EPWMxA and/or output EPWMxB • Specify the time at which switching events occur on the EPWMxA or EPWMxB output
Action-qualifier (AQ)	• Specify the type of action taken when a time-base or counter-compare submodule event occurs: – No action taken – Output EPWMxA and/or EPWMxB switched high – Output EPWMxA and/or EPWMxB switched low – Output EPWMxA and/or EPWMxB toggled • Force the PWM output state through software control • Configure and control the PWM dead-band through software
Dead-band (DB)	• Control of traditional complementary dead-band relationship between upper and lower switches • Specify the output rising-edge-delay value • Specify the output falling-edge delay value • Bypass the dead-band module entirely. In this case the PWM waveform is passed through without modification
PWM-chopper (PC)	• Create a chopping (carrier) frequency • Pulse width of the first pulse in the chopped pulse train • Duty cycle of the second and subsequent pulses • Bypass the PWM-chopper module entirely. In this case the PWM waveform is passed through without modification.

Table 12-383. Submodule Configuration Parameters (continued)

Submodule	Configuration Parameter or Option
Trip-zone (TZ)	• Configure the EPWM module to react to one, all, or none of the trip-zone pins • Specify the tripping action taken when a fault occurs: – Force EPWMxA and/or EPWMxB high – Force EPWMxA and/or EPWMxB low – Force EPWMxA and/or EPWMxB to a high-impedance state – Configure EPWMxA and/or EPWMxB to ignore any trip condition • Configure how often the EPWM will react to the trip-zone pin: – One-shot – Cycle-by-cycle • Enable the trip-zone to initiate an interrupt • Bypass the trip-zone module entirely
Event-trigger (ET)	• Enable the EPWM events that will trigger an interrupt. • Specify the rate at which events cause triggers (every occurrence or every second or third occurrence) • Poll, set, or clear event flags

Some examples on various EPWM module configurations are shown below. These examples use the constant definitions shown in Section 12.4.3.4.1.1 .

Constant Definitions Used in the EPWM Code Examples

```
// TBCTL (Time-Base Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// TBCNT MODE bits
#define         TB_COUNT_UP         0x0
#define         TB_COUNT_DOWN       0x1
#define         TB_COUNT_UPDOWN     0x2
#define         TB_FREEZE           0x3
// PHSEN bit
#define         TB_DISABLE          0x0
#define         TB_ENABLE           0x1
// PRDLD bit
#define         TB_SHADOW           0x0
#define         TB_IMMEDIATE        0x1
// SYNCOSEL bits
#define         TB_SYNC_IN          0x0
#define         TB_CTR_ZERO         0x1
#define         TB_CTR_CMPB         0x2
#define         TB_SYNC_DISABLE     0x3
// HSPCLKDIV and CLKDIV bits
#define         TB_DIV1             0x0
#define         TB_DIV2             0x1
#define         TB_DIV4             0x2
// PHSDIR bit
#define         TB_DOWN             0x0
#define         TB_UP               0x1
```

```
// CMPCTL (Compare Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// LOADAMODE and LOADBMODE bits
#define         CC_CTR_ZERO         0x0
#define         CC_CTR_PRD          0x1
#define         CC_CTR_ZERO_PRD     0x2
#define         CC_LD_DISABLE       0x3
// SHDWAMODE and SHDWBMODE bits
#define         CC_SHADOW           0x0
#define         CC_IMMEDIATE        0x1
// AQCTLA and AQCTLB (Action-qualifier Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// ZRO, PRD, CAU, CAD, CBU, CBD bits
#define         AQ_NO_ACTION        0x0
#define         AQ_CLEAR            0x1
#define         AQ_SET              0x2
```

```
#define         AQ_TOGGLE          0x3
// DBCTL (Dead-Band Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// MODE bits
#define         DB_DISABLE         0x0
#define         DBA_ENABLE         0x1
#define         DBB_ENABLE         0x2
#define DB_FULL_ENABLE 0x3
// POLSEL bits
#define         DB_ACTV_HI         0x0
#define         DB_ACTV_LOC        0x1
#define         DB_ACTV_HIC        0x2
#define         DB_ACTV_LO         0x3
// PCCTL (chopper control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// CHPEN bit
#define         CHP_ENABLE         0x0
#define CHP_DISABLE 0x1
// CHPFREQ bits
#define         CHP_DIV1           0x0
#define         CHP_DIV2           0x1
#define         CHP_DIV3           0x2
#define         CHP_DIV4           0x3
#define         CHP_DIV5           0x4
#define         CHP_DIV6           0x5
#define         CHP_DIV7           0x6
#define         CHP_DIV8           0x7
// CHPDUTY bits
#define         CHP1_8TH           0x0
#define         CHP2_8TH           0x1
#define         CHP3_8TH           0x2
#define         CHP4_8TH           0x3
#define         CHP5_8TH           0x4
#define         CHP6_8TH           0x5
#define         CHP7_8TH           0x6
// TZSEL (Trip-zone Select)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// CBCn and OSHTn bits
#define         TZ_ENABLE          0x0
#define         TZ_DISABLE         0x1
// TZCTL (Trip-zone Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// TZA and TZB bits
#define         TZ_HIZ             0x0
#define         TZ_FORCE_HI        0x1
#define         TZ_FORCE_LO        0x2
#define         TZ_DISABLE         0x3
// ETSEL (Event-trigger Select)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// INTSEL, SOCASEL, SOCBSEL bits
#define         ET_CTR_ZERO        0x1
#define         ET_CTR_PRD         0x2
#define         ET_CTRU_CMPA       0x4
#define         ET_CTRD_CMPA       0x5
#define         ET_CTRU_CMPB       0x6
#define         ET_CTRD_CMPB       0x7
// ETPS (Event-trigger Prescale)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// INTPRD, SOCAPRD, SOCBPRD bits
#define         ET_DISABLE         0x0
#define         ET_1ST             0x1
#define         ET_2ND             0x2
#define         ET_3RD             0x3
```

12.4.3.4.2 EPWM Time-Base (TB) Submodule

This section describes the Time-Base (TB) submodule in the PWM module.

12.4.3.4.2.1 Overview

Each EPWM module has its own time-base submodule that determines all of the timing events. Built-in synchronization logic allows the time-base of multiple EPWM modules (EPWMx) to work together as a single system. Figure 12-328 illustrates the time-base module's place within the EPWM.

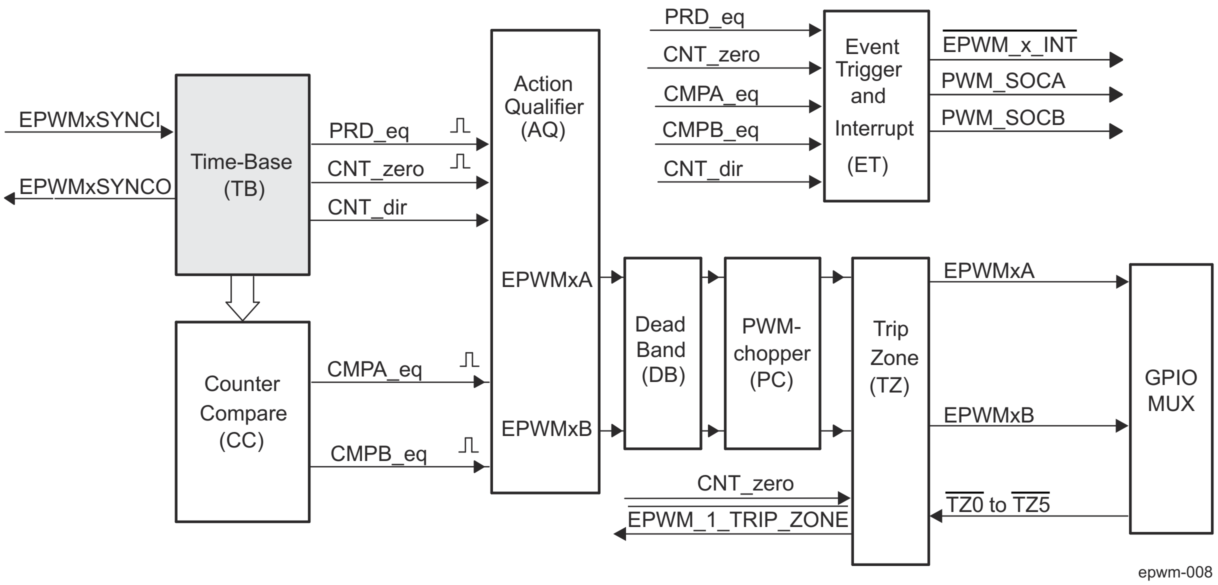

Figure 12-328. EPWM Time-Base Submodule

The TB module generates the period (or frequency) of the PWM output waveforms and consists of a 16-bit counter that can be configured for up, down or up and down counting. The time base for the counter is a pre-scaled version of the system clock (FICLK/n) which can be programmed for a pre-scale of 1, that is same as system clock.

TB module features:

- Specify the EPWMx time-base counter (TBCNT) frequency or period in the EPWM_TBCNT register to control how often events occur.
- Manage time-base synchronization with other EPWMx modules.
- Maintain a phase relationship with other EPWMx modules.
- Set the time-base counter to count-up, count-down, or count-up-and-down mode.
- Generate the following events:
  - PRD_eq (Time-base counter (EPWM_TBCNT register) equal to the specified period in EPWM_TBPRD register (that is TBCNT = TBPRD)).
  - CNT_zero (Time-base counter equal to zero (TBCNT = 0000h)).
- Configure the rate of the time-base clock; a prescaled version of the CPU m clock (FICLK). This allows the time-base counter to increment/decrement at a slower rate.

12.4.3.4.2.2 Controlling and Monitoring the EPWM Time-Base Submodule

Table 12-372 lists the registers used to control and monitor the time-base submodule.

Table 12-384. EPWM Time-Base Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_TBCTL	Time-Base Control Register	0h	No
EPWM_TBSTS	Time-Base Status Register	2h	No
HRPWM_TBPHSHR	HRPWM extension Phase Register (1)	4h	No
EPWM_TBPHS	Time-Base Phase Register	6h	No
EPWM_TBCNT	Time-Base Counter Register	8h	No
EPWM_TBPRD	Time-Base Period Register	Ah	Yes

(1) This register is available only on EPWM instances that include the high-resolution extension (HRPWM). On EPWM modules that do not include the HRPWM, this location is reserved. See *EPWM Integration* to determine which EPWM instances include this feature.

Figure 12-329 shows the critical signals and registers of the time-base submodule. Table 12-373 provides descriptions of the key signals associated with the time-base submodule.

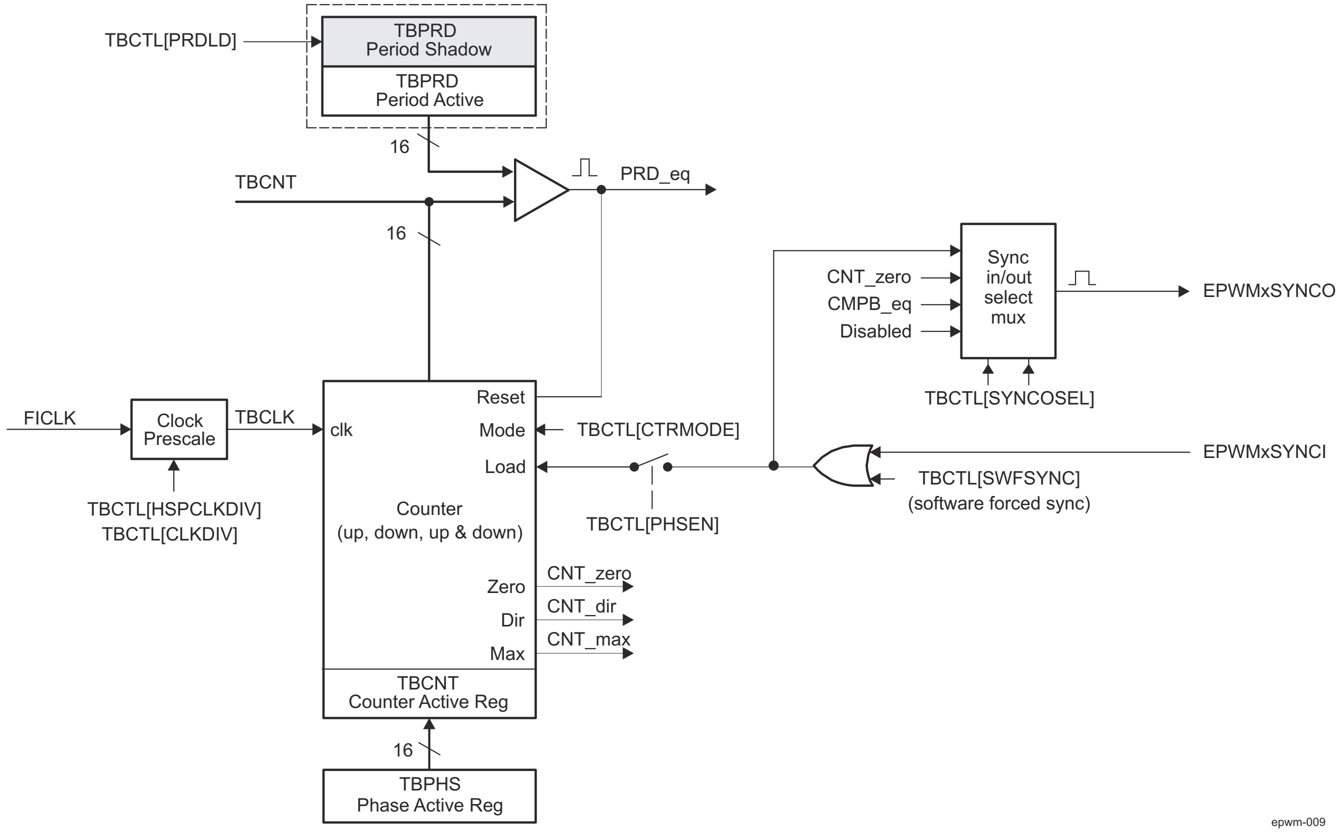

Figure 12-329. EPWM Time-Base Submodule Signals and Registers

Table 12-385. EPWM Time-Base Submodule Key Signals

Signal	Description
EPWMxSYNCI	Time-base synchronization input. Input pulse used to synchronize the time-base counter with the counter of another EPWM module earlier in the synchronization chain. An EPWM peripheral can be configured to use or ignore this signal. For the first EPWM module (EPWM0) this signal comes from a device pin. For subsequent EPWM modules this signal is passed from another EPWM peripheral. For example, EPWM2SYNCI is generated by the EPWM1 peripheral and the EPWM3SYNCI is generated (optional through internal multiplexer) by EPWM2 or from a device pin. See Section 12.4.3.4.2.3.2 for information on the synchronization order of a particular device.
EPWMxSYNCO	Time-base synchronization output. This output pulse is used to synchronize the counter of an EPWM module later in the synchronization chain. The EPWM module generates this signal from one of three event sources: 1. EPWMxSYNCI (Synchronization input pulse) 2. TBCNT = 0: The time-base counter (EPWM_TBCNT register) equal to zero (TBCNT = 0000h). 3. TBCNT = CMPB: The time-base counter (EPWM_TBCNT register) equal to the counter-compare B register — EPWM_CMPB (that is bitfield TBCNT = bitfield CMPB).
PRD_eq	Time-base counter equal to the specified period. This signal is generated whenever the counter value is equal to the active period register value. That is when TBCNT = TBPRD.
CNT_zero	Time-base counter equal to zero. This signal is generated whenever the counter value is zero. That is when TBCNT equals 0000h.
CMPB_eq	Time-base counter equal to active counter-compare B register (TBCNT = CMPB).

Table 12-385. EPWM Time-Base Submodule Key Signals (continued)

Signal	Description
	This event is generated by the counter-compare submodule and used by the synchronization out logic.
CNT_dir	Time-base counter direction. Indicates the current direction of the EPWM's time-base counter. This signal is high when the counter is increasing and low when it is decreasing.
CNT_max	Time-base counter equal max value (TBCNT = FFFFh). Generated event when the EPWM_TBCNT register value reaches its maximum value. This signal is only used only as a status bit.
TBCLK	Time-base clock. This is a prescaled version of the system clock — FICLK and is used by all submodules within the EPWMn. This clock determines the rate at which time-base counter increments or decrements.

12.4.3.4.2.3 Calculating PWM Period and Frequency

The frequency of PWM events is controlled by the time-base period register (EPWM_TBPRD) and the mode of the time-base counter. Figure 12-330 shows the period (T_{pwm}) and frequency (F_{pwm}) relationships for the up-count, down-count, and up-down-count time-base counter modes when the period is set to 4 (EPWM_TBPRD[15-0] TBPRD = 0x4). The time increment for each step is defined by the time-base clock (TBCLK) which is a prescaled version of the system clock (FICLK).

The time-base counter has three modes of operation selected by the time-base control register (EPWM_TBCTL):

- **Up-Down-Count Mode:** In up-down-count mode, the time-base counter starts from zero and increments until the period (TBPRD) value is reached. When the period value is reached, the time-base counter then decrements until it reaches zero. At this point the counter repeats the pattern and begins to increment.
- **Up-Count Mode:** In this mode, the time-base counter starts from zero and increments until it reaches the value in the period register (TBPRD). When the period value is reached, the time-base counter resets to zero and begins to increment once again.
- **Down-Count Mode:** In down-count mode, the time-base counter starts from the period (TBPRD) value and decrements until it reaches zero. When it reaches zero, the time-base counter is reset back to the period value and it repeats this pattern.

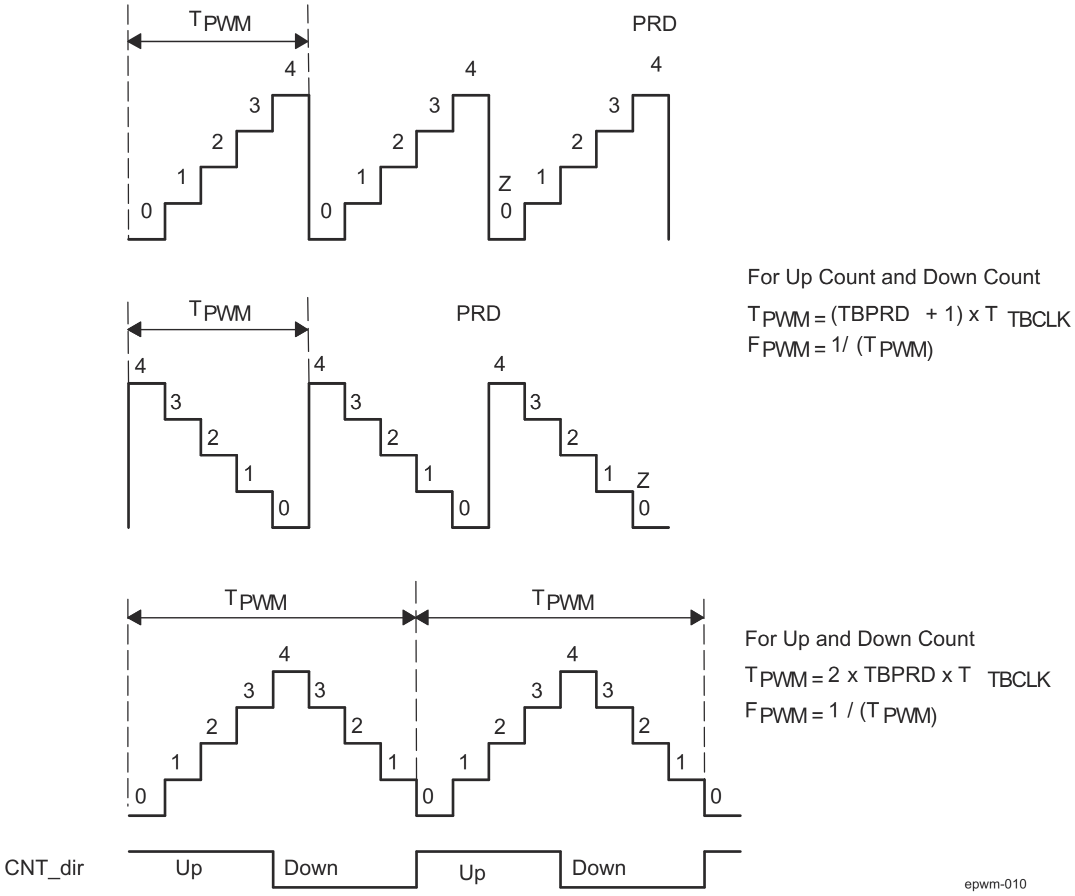

Figure 12-330. EPWM Time-Base Frequency and Period

12.4.3.4.2.3.1 EPWM Time-Base Period Shadow Register

The time-base period register (EPWM_TBPRD) has a shadow register. Shadowing allows the register update to be synchronized with the hardware. The following definitions are used to describe all shadow registers in the EPWM module:

- **Active Register:** The active register controls the hardware and is responsible for actions that the hardware causes or invokes.
- **Shadow Register:** The shadow register buffers or provides a temporary holding location for the active register. It has no direct effect on any control hardware. At a strategic point in time the shadow register's content is transferred to the active register. This prevents corruption or spurious operation due to the register being asynchronously modified by software.

The memory address of the shadow period register is the same as the active register. Which register is written to or read from is determined by the EPWM_TBCTL[3] PRDLD bit. This bit enables and disables the EPWM_TBPRD shadow register as follows:

- **Time-Base Period Shadow Mode:** The EPWM_TBPRD shadow register is enabled when EPWM_TBCTL[3] PRDLD = 0h. Reads from and writes to the EPWM_TBPRD register memory address go to the shadow register. The shadow register contents are transferred to the active register (EPWM_TBPRD (Active) ← EPWM_TBPRD (shadow)) when the time-base counter register (EPWM_TBCNT) equals zero (TBCNT = 0000h). By default the EPWM_TBPRD shadow register is enabled.
- **Time-Base Period Immediate Load Mode:** If immediate load mode is selected (EPWM_TBCTL[3] PRDLD = 1h), then a read from or a write to the TBPRD memory address goes directly to the active register.

12.4.3.4.2.3.2 EPWM Time-Base Counter Synchronization

A time-base synchronization scheme connects all of the EPWM modules on a device. Each EPWM module has a synchronization input (EPWMxSYNCI) and a synchronization output (EPWMxSYNCO). The input synchronization for the first instance (EPWM0) comes from an external pin. For the device EPWM environment sync pin details refer to *EPWM Environment*. The possible synchronization connections for the remaining EPWM modules is shown in Figure 12-331.

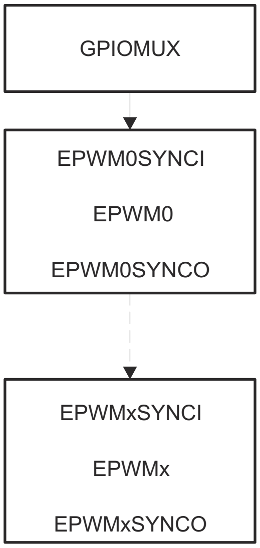

epwm-011

Figure 12-331. EPWM Time-Base Counter Synchronization Scheme 1

Each EPWM module can be configured to use or ignore the synchronization input. If the EPWM_TBCTL[2] PHSEN bit is set, then the time-base counter (TBCNT) of the EPWM module (EPWM_TBCNT register) will be automatically loaded with the phase register (EPWM_TBPHS) contents when one of the following conditions occur:

- **EPWMxSYNCI: Synchronization Input Pulse:** The value of the phase register is loaded into the counter register when an input synchronization pulse is detected (EPWM_TBPHS → EPWM_TBCNT). This operation occurs on the next valid time-base clock (TBCLK) edge.
- **Software Forced Synchronization Pulse:** Writing a 1h to the EPWM_TBCTL[6] SWFSYNC control bit invokes a software forced synchronization. This pulse is ORed with the synchronization input signal, and therefore has the same effect as a pulse on EPWMxSYNCI.

This feature enables the EPWM module to be automatically synchronized to the time base of another EPWM module. Lead or lag phase control can be added to the waveforms generated by different EPWM modules to synchronize them. In up-down-count mode, the EPWM_TBCTL[13] PHSDIR bit configures the direction of the time-base counter immediately after a synchronization event. The new direction is independent of the direction prior to the synchronization event. The TBPHS bit is ignored in count-up or count-down modes. See Figure 12-332 through Figure 12-335 for examples.

Clearing the EPWM_TBCTL[2] PHSEN bit configures the EPWM to ignore the synchronization input pulse. The synchronization pulse can still be allowed to flow-through to the EPWMxSYNCO and be used to synchronize other EPWM modules. In this way, a controller time-base (for example, EPWM1) and downstream modules (EPWM2–EPWMx) can be set and they may select to run in synchronization with the controller.

12.4.3.4.2.4 Phase Locking the Time-Base Clocks of Multiple EPWM Modules

As already described in *EPWM Modules Time-Base Clock Gating*, TB_CLKEN bit in the EPWMn_CTRL (where n = 0 to 5) register of the device CTRL_MMR0 can be used to individually control or globally synchronize the time-base clocks of all enabled EPWM modules on a device. When all TB_CLKEN bits are set to 0b0, the time-base clocks of all EPWMx (where x = 0 to 5) modules are stopped (default). When all TB_CLKEN bits are simultaneously set in software to 0b1, all EPWMx modules time-base clocks are started with the rising edge of TBCLK aligned. For perfectly synchronized TBCLKs, the prescaler bits in the EPWM_TBCTL register of each EPWM module must be set identically. The proper procedure for enabling the EPWM clocks is as follows:

1. Enable the EPWM module clocks.
2. Set TB_CLKEN = 0. This will stop the time-base clock within any enabled EPWMx module.
3. Configure the prescaler values and desired EPWM modes per each involved EPWMx.
4. Simultaneously set TB_CLKEN bits to 0b1.

12.4.3.4.2.5 EPWM Time-Base Counter Modes and Timing Waveforms

The time-base counter operates in one of four modes:

- Up-count mode which is asymmetrical.
- Down-count mode which is asymmetrical.
- Up-down-count which is symmetrical.
- Frozen where the time-base counter is held constant at the current value.

To illustrate the operation of the first three modes, Figure 12-332 to Figure 12-335 show when events are generated and how the time-base responds to an EPWMxSYNCI signal.

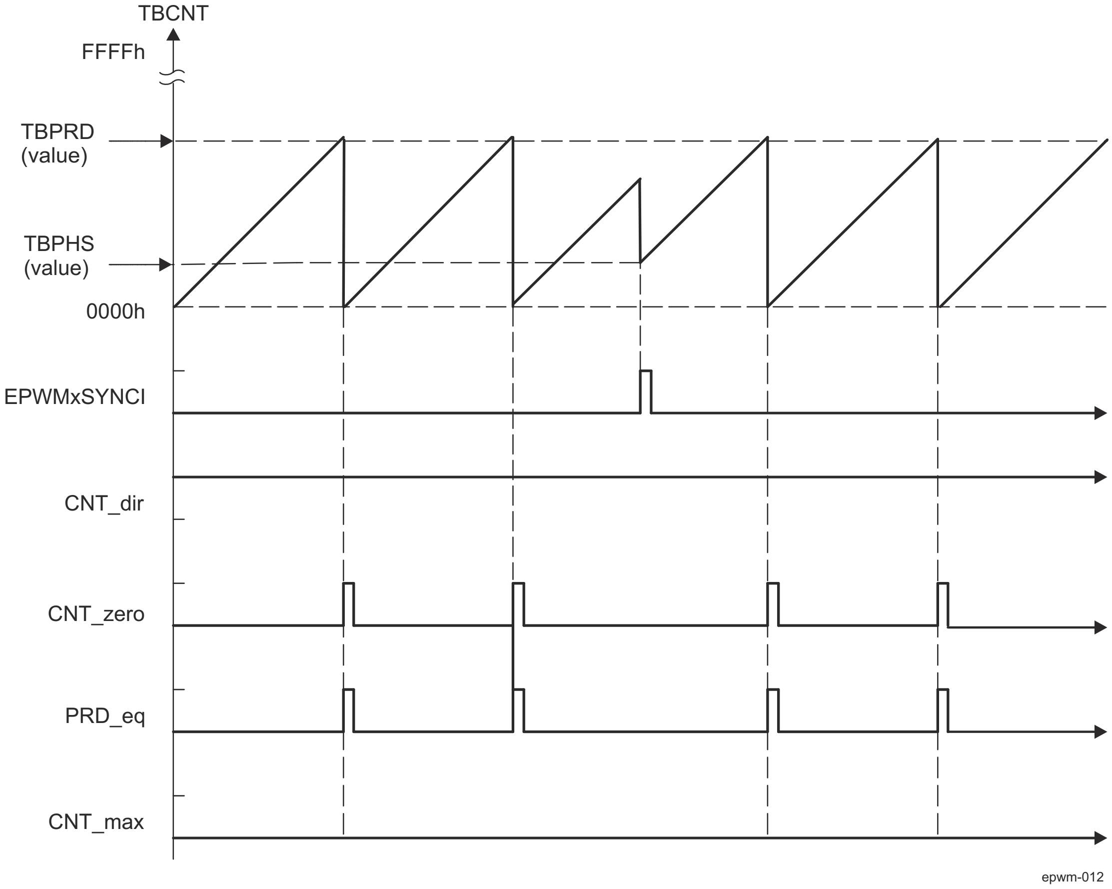

Figure 12-332. EPWM Time-Base Up-Count Mode Waveforms

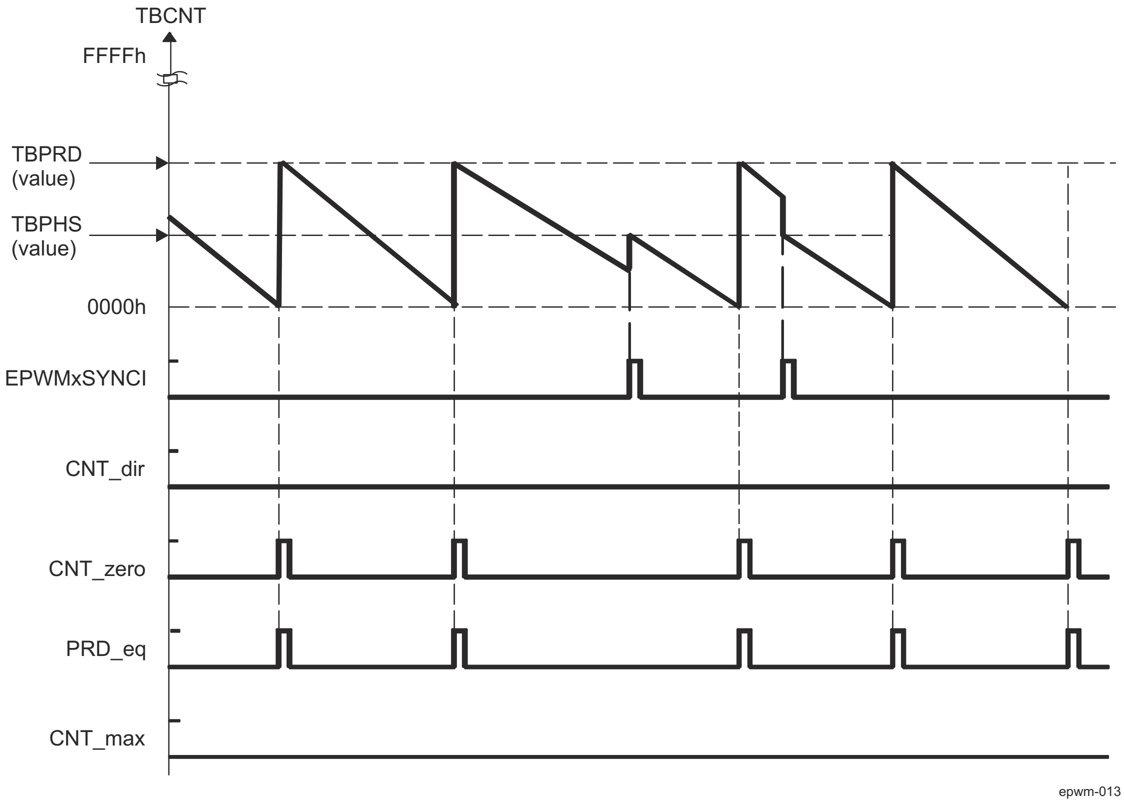

Figure 12-333. EPWM Time-Base Down-Count Mode Waveforms

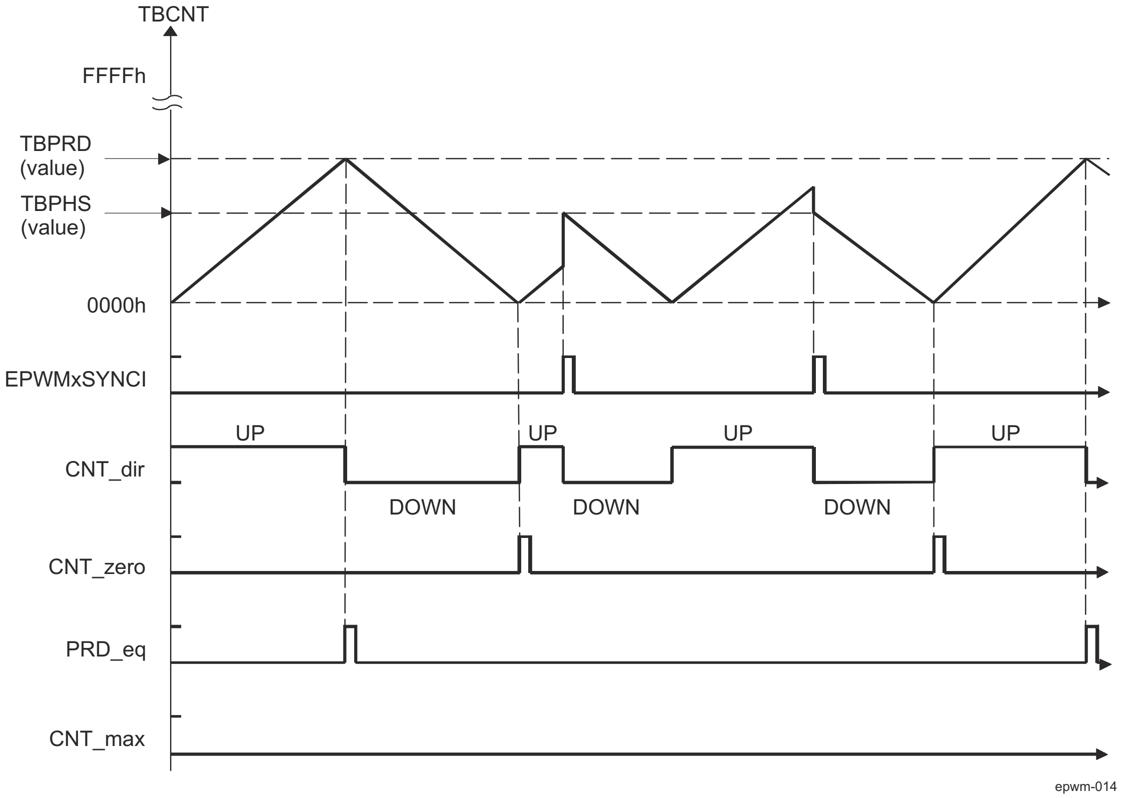

Figure 12-334. EPWM Time-Base Up-Down-Count Waveforms, EPWM_TBCTL[13] PHSDIR = 0 Count Down on Synchronization Event

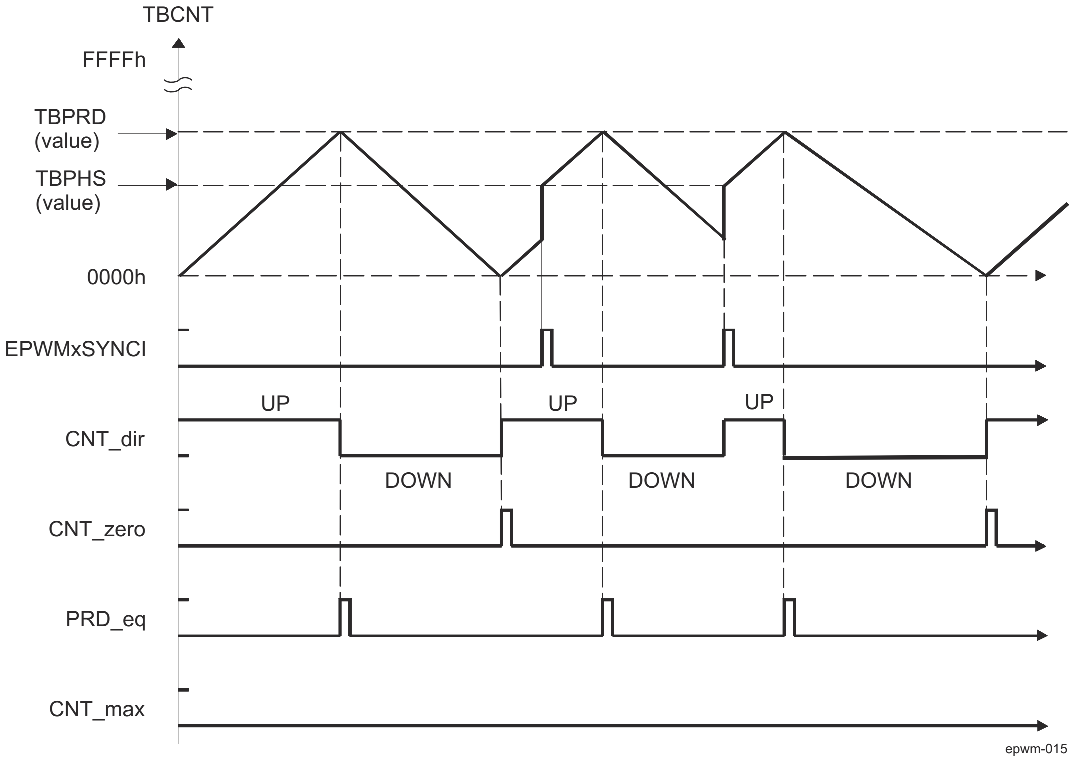

Figure 12-335. EPWM Time-Base Up-Down Count Waveforms, EPWM_TBCTL[13] PHSDIR = 1 Count Up on Synchronization Event

12.4.3.4.3 EPWM Counter-Compare (CC) Submodule

This section describes the Counter-Compare (CC) submodule in the PWM module.

12.4.3.4.3.1 Overview

Figure 12-336 illustrates the counter-compare submodule within the EPWM. Figure 12-337 shows the basic structure of the counter-compare submodule.

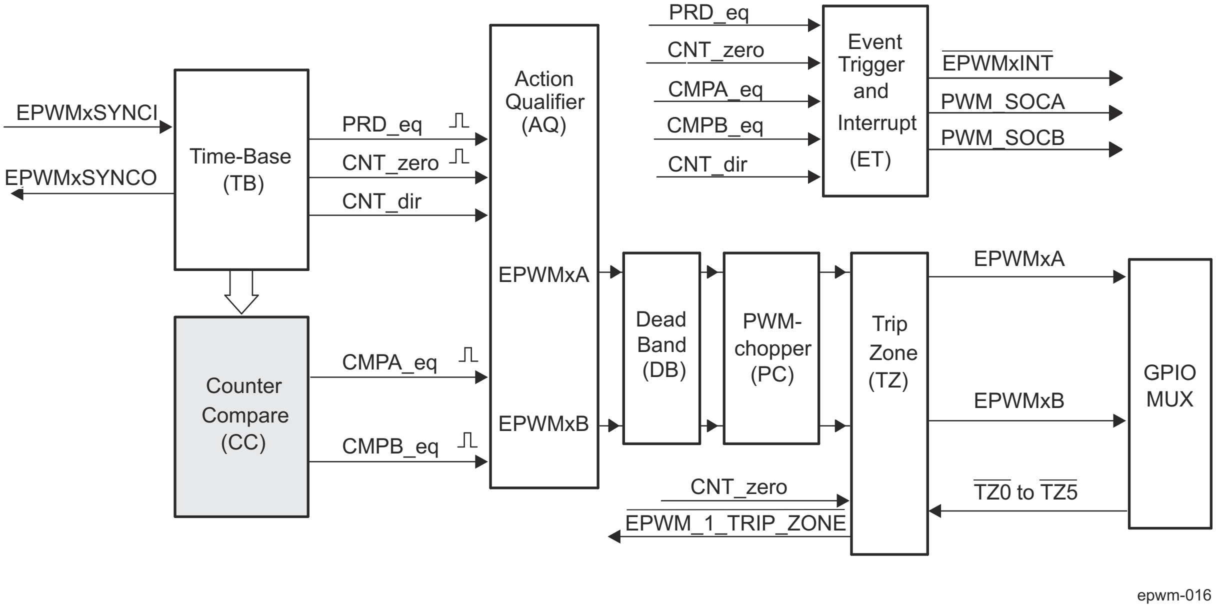

Figure 12-336. EPWM Counter-Compare Submodule

CC module features:

- Generates events based on programmable time stamps using the EPWM_CMPA and EPWM_CMPB registers
  - CMPA_eq (Time-base counter equals counter-compare A register (TBCNT = CMPA)).
  - CMPB_eq (Time-base counter equals counter-compare B register (TBCNT = CMPB)).
- Controls the PWM duty cycle if the action-qualifier submodule is configured appropriately
- Shadows new compare values to prevent corruption or glitches during the active PWM cycle.

The counter-compare submodule takes as input the time-base counter value. This value is continuously compared to the counter-compare A (EPWM_CMPA) and counter-compare B (EPWM_CMPB) registers. When the time-base counter is equal to one of the compare registers, the counter-compare unit generates an appropriate event.

12.4.3.4.3.2 Controlling and Monitoring the EPWM Counter-Compare Submodule

Table 12-374 lists the registers used to control and monitor the counter-compare submodule. Table 12-375 lists the key signals associated with the counter-compare submodule.

Table 12-386. EPWM Counter-Compare Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_CMPCTL	Counter-Compare Control Register.	Eh	No
HRPWM_CMPAHR	HRPWM Counter-Compare A Extension Register (1)	10h	Yes
EPWM_CMPA	Counter-Compare A Register	12h	Yes

Table 12-386. EPWM Counter-Compare Submodule Registers (continued)

Acronym	Register Description	Address Offset	Shadowed
EPWM_CMPB	Counter-Compare B Register	14h	Yes

(1) This register is available only on the EPWM modules with the high-resolution extension (HRPWM). On the EPWM modules that do not include the HRPWM, this location is reserved. See *EPWM Integration* to determine which EPWM instances include this feature.

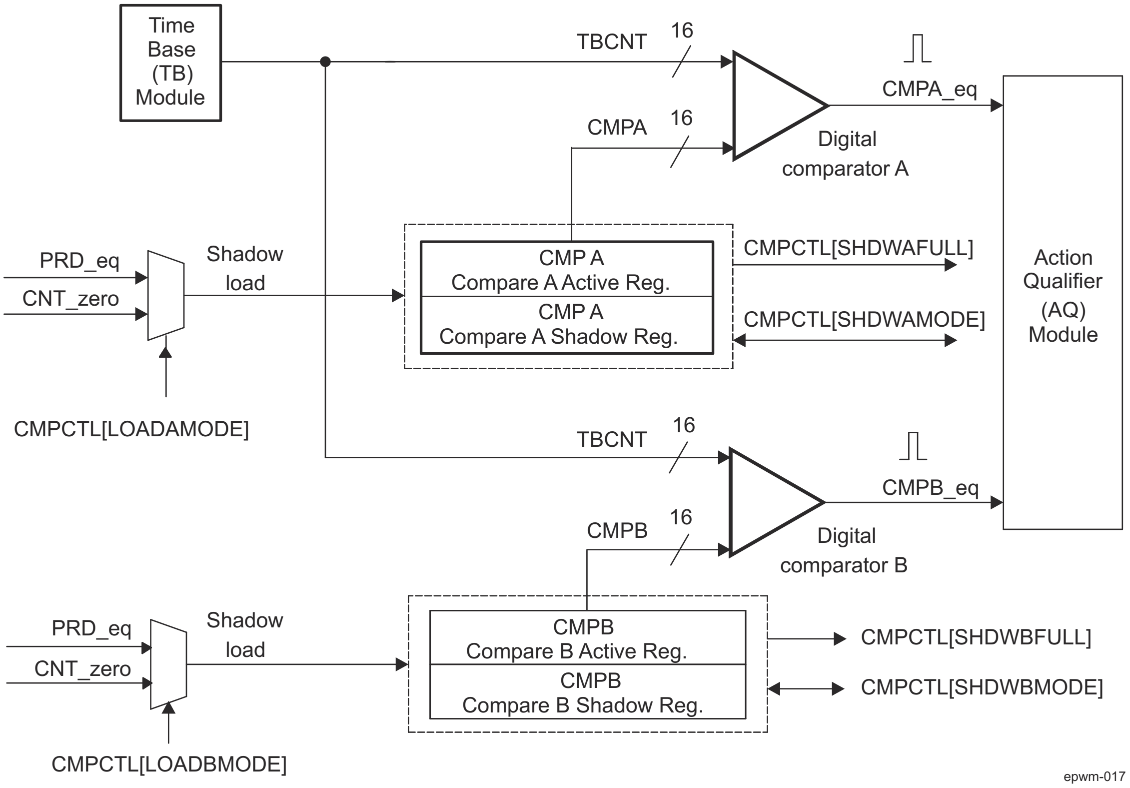

Figure 12-337. EPWM Counter-Compare Submodule Signals and Registers

Table 12-387. EPWM Counter-Compare Submodule Key Signals

Signal	Description of Event	Register Bitfields Compared
CMPA_eq	Time-base counter equal to the active counter-compare A value	TBCNT = CMPA
CMPB_eq	Time-base counter equal to the active counter-compare B value	TBCNT = CMPB
PRD_eq	Time-base counter equal to the active period. Used to load active counter-compare A and B registers from the shadow register	TBCNT = TBPRD
CNT_zero	Time-base counter equal to zero. Used to load active counter-compare A and B registers from the shadow register	TBCNT = 0000h

12.4.3.4.3.3 Operational Highlights for the EPWM Counter-Compare Submodule

The counter-compare submodule is responsible for generating two independent compare events based on two compare registers:

1. CMPA: Time-base counter equal to counter-compare A register (EPWM_TBCNT = EPWM_CMPA).
2. CMPB: Time-base counter equal to counter-compare B register (EPWM_TBCNT = EPWM_CMPB).

For up-count or down-count mode, each event occurs only once per cycle. For up-down-count mode each event occurs twice per cycle, if the compare value is between 0000h and TBPRD; and occurs once per cycle, if the compare value is equal to 0000h or equal to TBPRD. These events are fed into the action-qualifier submodule where they are qualified by the counter direction and converted into actions if enabled. Refer to Section 12.4.3.4.4 for more details.

The counter-compare EPWM_CMPA and EPWM_CMPB registers each have an associated shadow register. Shadowing provides a way to keep updates to the registers synchronized with the hardware. When shadowing is used, updates to the active registers only occurs at strategic points. This prevents corruption or spurious operation due to the register being asynchronously modified by software. The memory address of the active register and the shadow register is identical. Which register is written to or read from is determined by the EPWM_CMPCTL[4] SHDWAMODE and EPWM_CMPCTL[6] SHDWBMODE bits. These bits enable and disable the EPWM_CMPA shadow register and EPWM_CMPB shadow register respectively. The behavior of the two load modes is described below:

- **Shadow Load Mode:**
  The shadow mode for the EPWM_CMPA register is enabled by clearing the EPWM_CMPCTL[4] SHDWAMODE bit and the shadow register for EPWM_CMPB register is enabled by clearing the EPWM_CMPCTL[6] SHDWBMODE bit. Shadow mode is enabled by default for both EPWM_CMPA and EPWM_CMPB register.

  If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events:
  - PRD_eq: Time-base counter equal to the period (TBCNT = TBPRD).
  - CNT_zero: Time-base counter equal to zero (TBCNT = 0000h)
  - Both PRD_eq and CNT_zero events occurrence

  Which of these three events will drive the counter compare module is specified by the EPWM_CMPCTL[1-0] LOADAMODE and EPWM_CMPCTL[3-2] LOADBMODE register bit fields. Only the active register contents are used by the counter-compare submodule to generate events to be sent to the action-qualifier.
- **Immediate Load Mode:**
  If immediate load mode is selected (EPWM_CMPCTL[4] SHDWAMODE = 1h or EPWM_CMPCTL[6] SHDWBMODE = 1h), then a read from or a write to the register will go directly to the active register.

Figure 12-338 and Figure 12-339 show Compare A and B Dual Shadow registers.

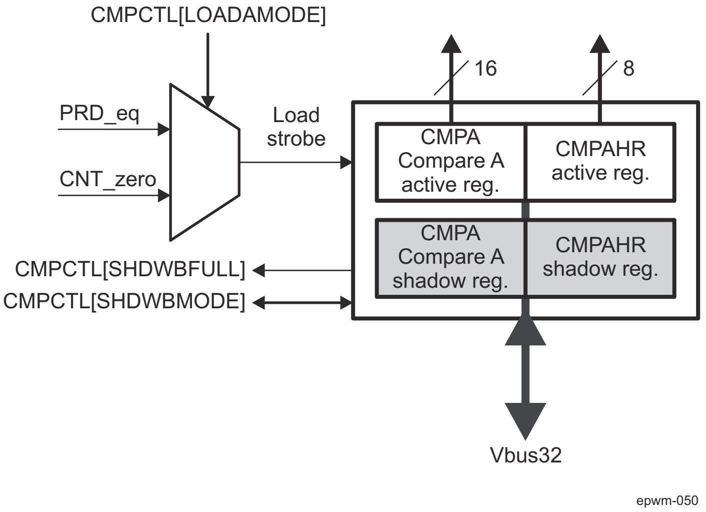

Figure 12-338. Compare A Dual Shadow register

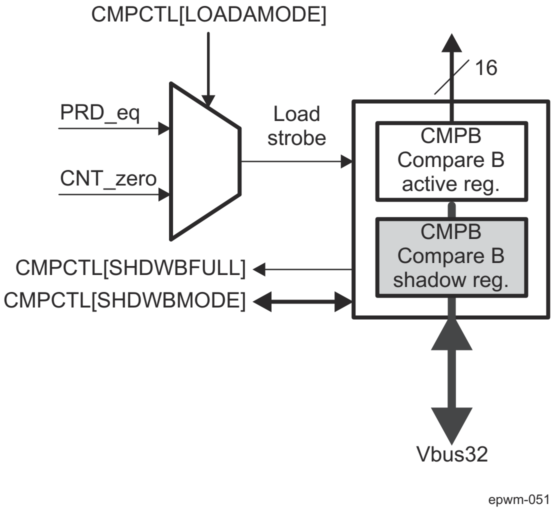

Figure 12-339. Compare B Dual Shadow register

Note

In HRPWM mode the user must perform a single 32-bit write access to both the HRPWM_CMPAHR and EPWM_CMPA registers. Two 16-bit accesses are not allowed.

12.4.3.4.3.4 EPWM Counter-Compare Submodule Timing Waveforms

As described in Section 12.4.3.4.2 , the Time Base (TB) module can be configured to operate in 3 distinct count modes:

- Up-count mode: used to generate an asymmetrical PWM waveform.
- Down-count mode: used to generate an asymmetrical PWM waveform.
- Up-down-count mode: used to generate a symmetrical PWM waveform.

The timing diagrams in Figure 12-340 to Figure 12-343 show how CMPA and CMPB events are generated in each of the 3 count modes and how the EPWMxSYNCI signal interacts.

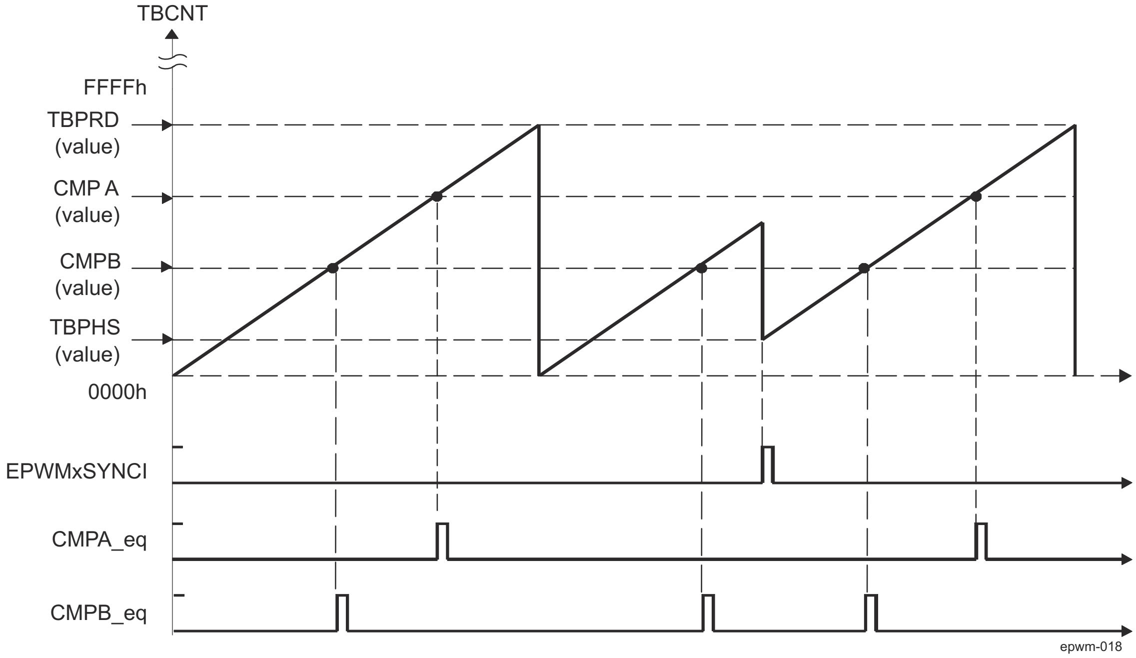

Note

An EPWMxSYNCI external synchronization event can cause a discontinuity in the TBCNT count sequence. This can lead to a compare event being skipped. This skipping is considered normal operation and must be taken into account.

Figure 12-340. EPWM Counter-Compare Event Waveforms in Up-Count Mode

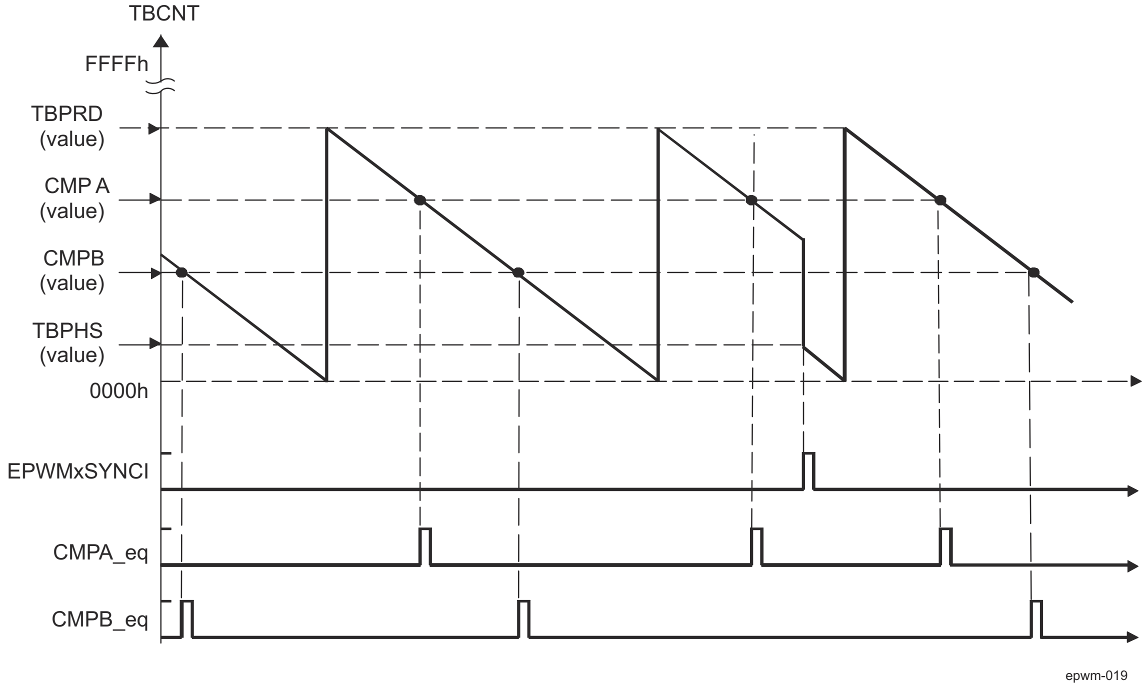

Figure 12-341. EPWM Counter-Compare Events in Down-Count Mode

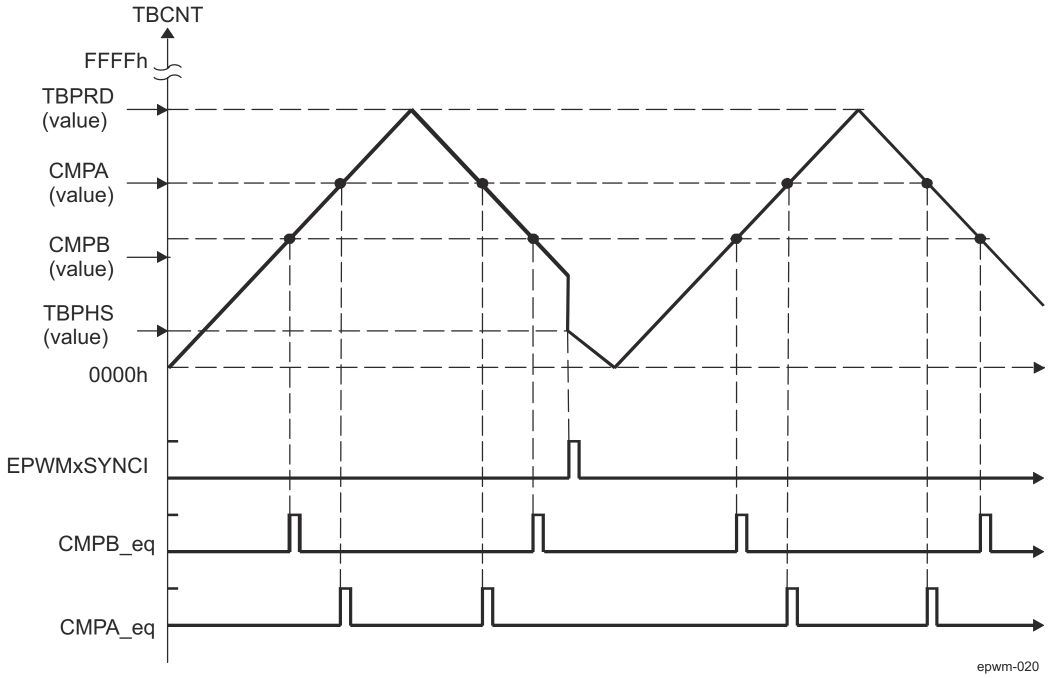

Figure 12-342. EPWM Counter-Compare Events in Up-Down-Count Mode, EPWM_TBCTL[13] PHSDIR = 0 Count Down on Synchronization Event

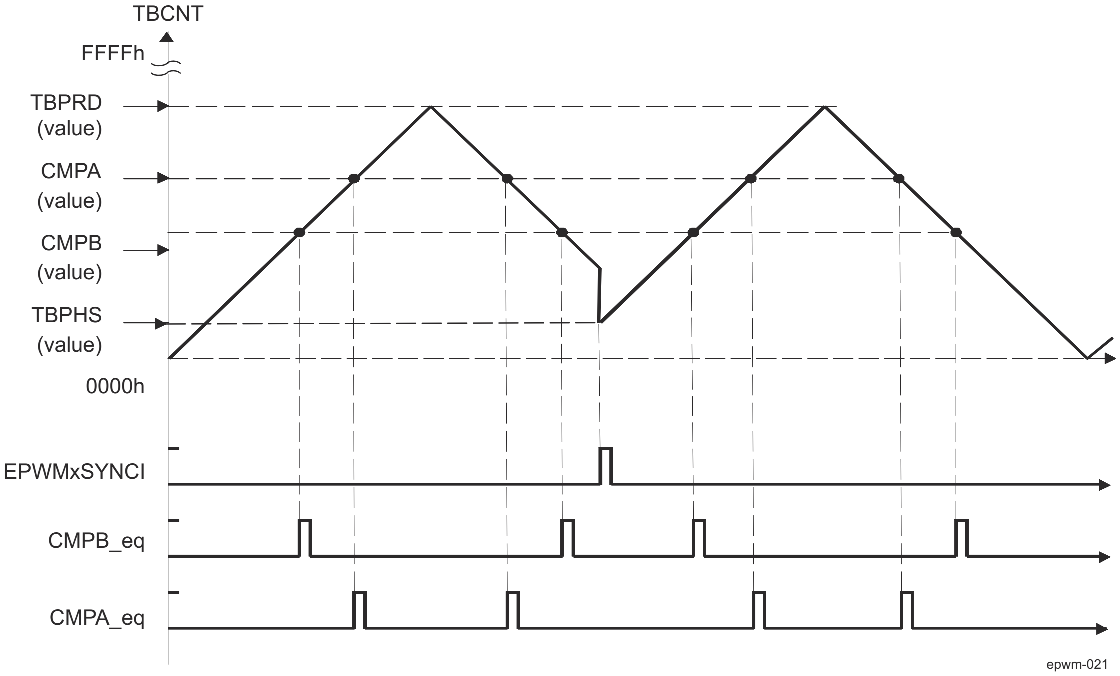

Figure 12-343. EPWM Counter-Compare Events in Up-Down-Count Mode, EPWM_TBCTL[13] PHSDIR = 1 Count Up on Synchronization Event

12.4.3.4.4 EPWM Action-Qualifier (AQ) Submodule

This section describes the Action-Qualifier (AQ) submodule in the PWM module.

12.4.3.4.4.1 Overview

Figure 12-344 shows the action-qualifier (AQ) submodule in the EPWM system. This submodule has the most important role in waveform construction and PWM generation. It decides which events are converted into various action types, thereby producing the required switched waveforms at the EPWMxA and EPWMxB outputs.

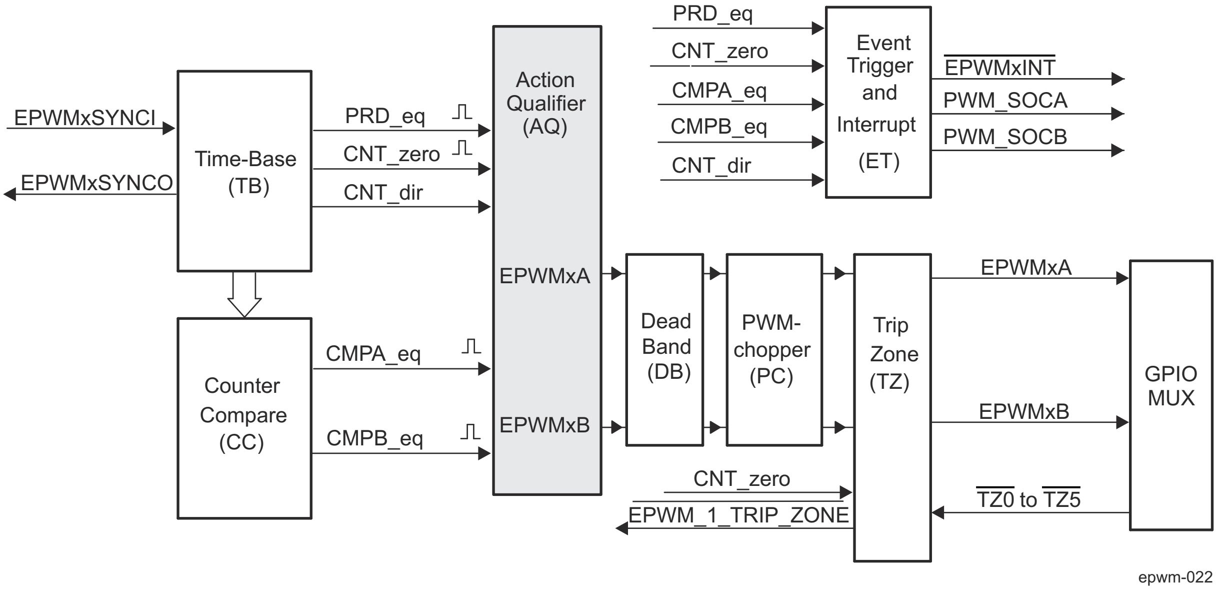

Figure 12-344. EPWM Action-Qualifier Submodule

AQ module features:

- Qualifying and generating actions (set, clear, toggle) based on the following events:
  - PRD_eq: Time-base counter equal to the period (TBCNT = TBPRD)
  - CNT_zero: Time-base counter equal to zero (TBCNT = 0000h)
  - CMPA_eq: Time-base counter equal to the counter-compare A register (TBCNT = CMPA)
  - CMPB_eq: Time-base counter equal to the counter-compare B register (TBCNT = CMPB)
- Managing priority when these events occur concurrently
- Providing independent control of events when the time-base counter is increasing and when it is decreasing

12.4.3.4.4.2 Controlling and Monitoring the EPWM Action-Qualifier Submodule

Table 12-376 lists the registers used to control and monitor the action-qualifier submodule.

Table 12-388. EPWM Action-Qualifier Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_AQCTLA	Action-Qualifier Control Register For Output A (EPWMxA)	16h	No
EPWM_AQCTLB	Action-Qualifier Control Register For Output B (EPWMxB)	18h	No
EPWM_AQSFRC	Action-Qualifier Software Force Register	1Ah	No
EPWM_AQCSFRC	Action-Qualifier Continuous Software Force	1Ch	Yes

The action-qualifier submodule is based on event-driven logic. It can be thought of as a programmable cross switch with events at the input and actions at the output, all of which are software controlled via the set of registers as shown in Figure 12-345. The possible input events are summarized again in Table 12-377.

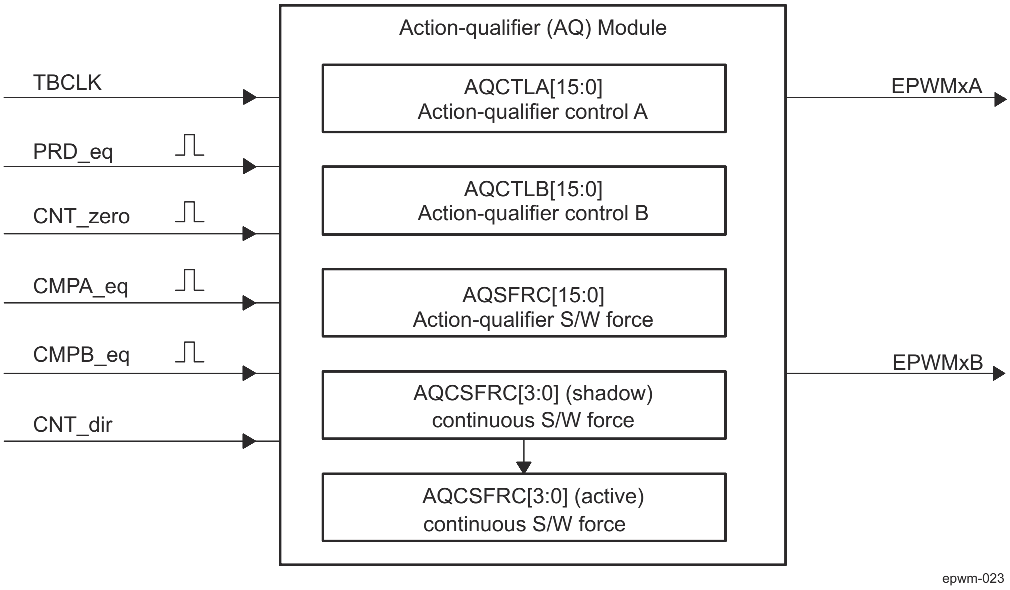

Figure 12-345. EPWM Action-Qualifier Submodule Inputs and Outputs

Table 12-389. EPWM Action-Qualifier Submodule Possible Input Events

Signal	Description	Register Bitfield Compared
PRD_eq	Time-base counter equal to the period value	TBCNT = TBPRD
CNT_zero	Time-base counter equal to zero	TBCNT = 0000h
CMPA_eq	Time-base counter equal to the counter-compare A	TBCNT = CMPA
CMPB_eq	Time-base counter equal to the counter-compare B	TBCNT = CMPB
Software forced event	Asynchronous event initiated by software	

The software forced action is a useful asynchronous event. This control is handled by EPWM_AQSFRC and EPWM_AQCSFRC registers.

The action-qualifier submodule controls how the two outputs EPWMxA and EPWMxB behave when a particular event occurs. The event inputs to the action-qualifier submodule are further qualified by the counter direction (up or down). This allows for independent action on outputs on both the count-up and count-down phases.

The possible actions imposed on outputs EPWMxA and EPWMxB are:

- **Set High:** Set output EPWMxA or EPWMxB to a high level.
- **Clear Low:** Set output EPWMxA or EPWMxB to a low level.
- **Toggle:** If EPWMxA or EPWMxB is currently pulled high, then pull the output low. If EPWMxA or EPWMxB is currently pulled low, then pull the output high.
- **Do Nothing:** Keep outputs EPWMxA and EPWMxB at same level as currently set. Although the "Do Nothing" option prevents an event from causing an action on the EPWMxA and EPWMxB outputs, this event can still trigger interrupts. See the Event_Trigger (ET) submodule description in Section 12.4.3.4.8 for details.

Actions are specified independently for either output (EPWMxA or EPWMxB). Any or all events can be configured to generate actions on a given output. All qualifier actions are configured via the control registers found at the end of this section.

For clarity, the drawings in this chapter use a set of symbolic actions. These symbols are summarized in Figure 12-346. Each symbol represents an action as a marker in time. Some actions are fixed in time (zero and period) while the CMPA and CMPB actions are moveable and their time positions are programmed via the counter-compare A and B registers, respectively. To turn off or disable an action, use the "Do Nothing option"; it is the default at reset.

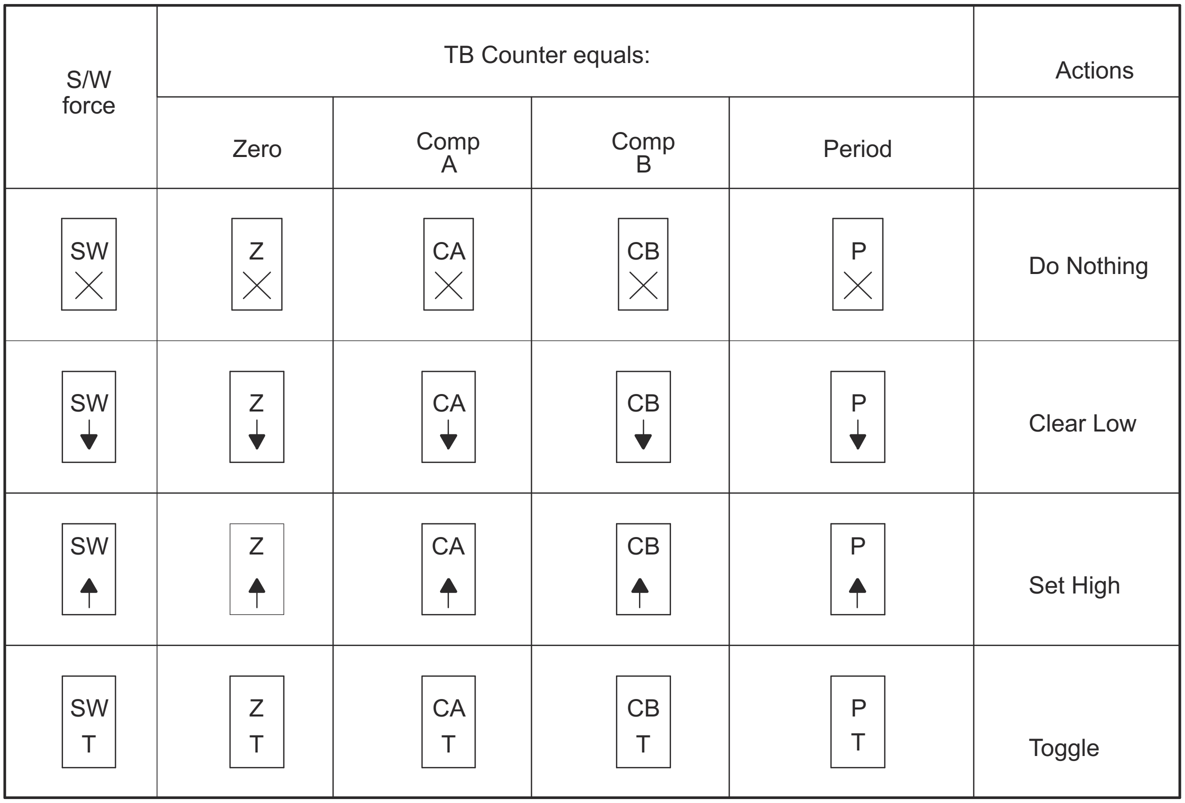

S/W force	TB Counter equals:				Actions
	Zero	Comp A	Comp B	Period	
SW ×	Z ×	CA ×	CB ×	P ×	Do Nothing
SW ↓	Z ↓	CA ↓	CB ↓	P ↓	Clear Low
SW ↑	Z ↑	CA ↑	CB ↑	P ↑	Set High
SW T	Z T	CA T	CB T	P T	Toggle

epwm-024

Figure 12-346. Possible Action-Qualifier Actions for EPWMxA and EPWMxB Outputs

12.4.3.4.4.3 EPWM Action-Qualifier Event Priority

It is possible for the EPWM action qualifier to receive more than one event at the same time. In this case events are assigned a priority by the hardware. The general rule is: events occurring later in time have a higher priority and software forced events always have the highest priority. The event priority levels for up-down-count mode are shown in Table 12-378. A priority level 1 is the highest priority and level 7 is the lowest. The priority changes slightly depending on the direction of TBCNT.

Table 12-390. EPWM Action-Qualifier Event Priority for Up-Down-Count Mode

Priority Level	Event if TBCNT is Incrementing TBCNT = 0 up to TBCNT = TBPRD	Event if TBCNT is Decrementing TBCNT = TBPRD down to TBCNT = 1
1 (Highest)	Software forced event	Software forced event
2	Counter equals CMPB on up-count (CBU)	Counter equals CMPB on down-count (CBD)
3	Counter equals CMPA on up-count (CAU)	Counter equals CMPA on down-count (CAD)
4	Counter equals zero	Counter equals period (TBPRD in EPWM_TBPRD active register)
5	Counter equals CMPB on down-count (CBD) (1)	Counter equals CMPB on up-count (CBU) (1)
6 (Lowest)	Counter equals CMPA on down-count (CAD) (1)	Counter equals CMPA on up-count (CBU) (1)

(1) To maintain symmetry for up-down-count mode, both up-events (CAU/CBU) and down-events (CAD/CBD) can be generated for TBPRD. Otherwise, up-events can occur only when the counter is incrementing and down-events can occur only when the counter is decrementing.

Table 12-379 shows the action-qualifier priority for up-count mode. In this case, the counter direction is always defined as up and thus down-count events will never be taken.

Table 12-391. EPWM Action-Qualifier Event Priority for Up-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to period (TBPRD)
3	Counter equal to CMPB on up-count (CBU)
4	Counter equal to CMPA on up-count (CAU)
5 (Lowest)	Counter equal to Zero

Table 12-380 shows the action-qualifier priority for down-count mode. In this case, the counter direction is always defined as down and thus up-count events will never be taken.

Table 12-392. EPWM Action-Qualifier Event Priority for Down-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to Zero
3	Counter equal to CMPB on down-count (CBD)
4	Counter equal to CMPA on down-count (CAD)
5 (Lowest)	Counter equal to period (TBPRD)

It is possible to set the compare value greater than the period. In this case the action will take place as shown in Table 12-381.

Table 12-393. Behavior if CMPA/CMPB is Greater than the Period

Counter Mode	Compare on Up-Count Event CAU/CBU	Compare on Down-Count Event CAU/CBU
Up-Count Mode	If CMPA/CMPB ≤ TBPRD period, then the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB > TBPRD, then the event will not occur.	Never occurs.
Down-Count Mode	Never occurs.	If CMPA/CMPB < TBPRD, the event will occur on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB ≥ TBPRD, the event will occur on a period match (TBCNT = TBPRD).
Up-Down-Count Mode	If CMPA/CMPB < TBPRD and the counter is incrementing, the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB is ≥ TBPRD, the event will occur on a period match (TBCNT = TBPRD).	If CMPA/CMPB < TBPRD and the counter is decrementing, the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB ≥ TBPRD, the event occurs on a period match (TBCNT = TBPRD).

12.4.3.4.4.4 Waveforms for Common EPWM Configurations

Note

The waveforms in this chapter show the EPWMs behavior for a static compare register value. In a running system, the active compare registers (EPWM_CMPA and EPWM_CMPB) are typically updated from their respective shadow registers once every period. The user specifies when the update will take place — either when the time-base counter reaches zero or when the time-base counter reaches period. There are some cases when the action based on the new value can be delayed by one period or the action based on the old value can take effect for an extra period. Some PWM configurations avoid this situation. These include, but are not limited to, the following:

Use up-down-count mode to generate a symmetric PWM:

- If EPWM_CMPA / EPWM_CMPB is loaded on zero, then use EPWM_CMPA / EPWM_CMPB values greater than or equal to 1.
- If EPWM_CMPA / EPWM_CMPB is loaded on period, then use EPWM_CMPA / EPWM_CMPB values less than or equal to TBPRD - 1.

  This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

Use up-down-count mode to generate an asymmetric PWM:

- To achieve 50-0% asymmetric PWM use the following configuration: Load EPWM_CMPA / EPWM_CMPB on period and use the period action to clear the PWM and a compare-up action to set the PWM. Modulate the compare value from 0 to TBPRD to achieve 50-0% PWM duty.

When using up-count mode to generate an asymmetric PWM:

- To achieve 0-100% asymmetric PWM use the following configuration: Load EPWM_CMPA / EPWM_CMPB on TBPRD. Use the Zero action to set the PWM and a compare-up action to clear the PWM. Modulate the compare value from 0 to TBPRD+1 to achieve 0-100% PWM duty.

Figure 12-347 shows how a symmetric PWM waveform can be generated using the up-down-count mode of the TBCNT. In this mode 0-100% DC modulation is achieved by using equal compare matches on the up count and down count portions of the waveform. In the example shown, CMPA is used to make the comparison. When the counter is incrementing the CMPA match will pull the PWM output high. Likewise, when the counter is decrementing the compare match will pull the PWM signal low. When EPWM_CMPA = EPWM_TBPRD, the PWM signal is low for the entire period giving the 0% duty waveform. When CMPA = 0, the PWM signal is high achieving 100% duty.

When using this configuration in practice, if CMPA/CMPB is loaded on zero, then use CMPA/CMPB values greater than or equal to 1. If CMPA/CMPB is loaded on period, then use CMPA/CMPB values less than or equal to TBPRD - 1. This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

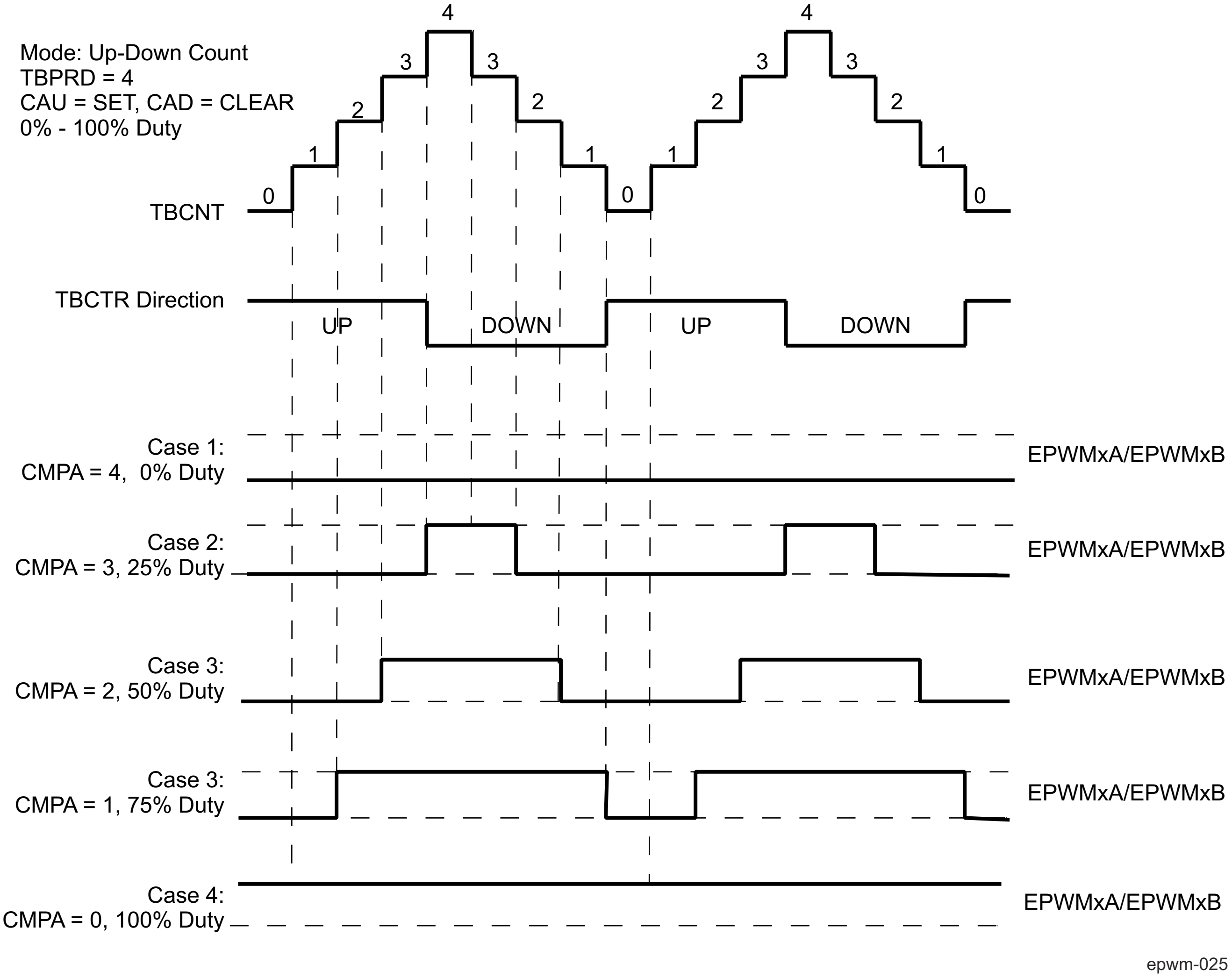

Figure 12-347. EPWM Up-Down-Count Mode Symmetrical Waveform

The PWM waveforms in Figure 12-348 through Figure 12-353 show some common action-qualifier configurations. Some conventions used in the figures are as follows:

- TBPRD, CMPA, and CMPB refer to the value written in their respective registers (EPWM_TBPRD, EPWM_CMPA, and EPWM_CMPB). The active register, not the shadow register, is used by the hardware.
- CMPx, refers to either CMPA or CMPB.
- EPWMxA and EPWMxB refer to the output signals from EPWMx
- Up-Down means Count-up-and-down mode, Up means up-count mode and Dwn means down-count mode
- Sym = Symmetric, Asym = Asymmetric

Table 12-382 and Table 12-383 contains initialization and runtime register configurations for the waveforms in Figure 12-348.

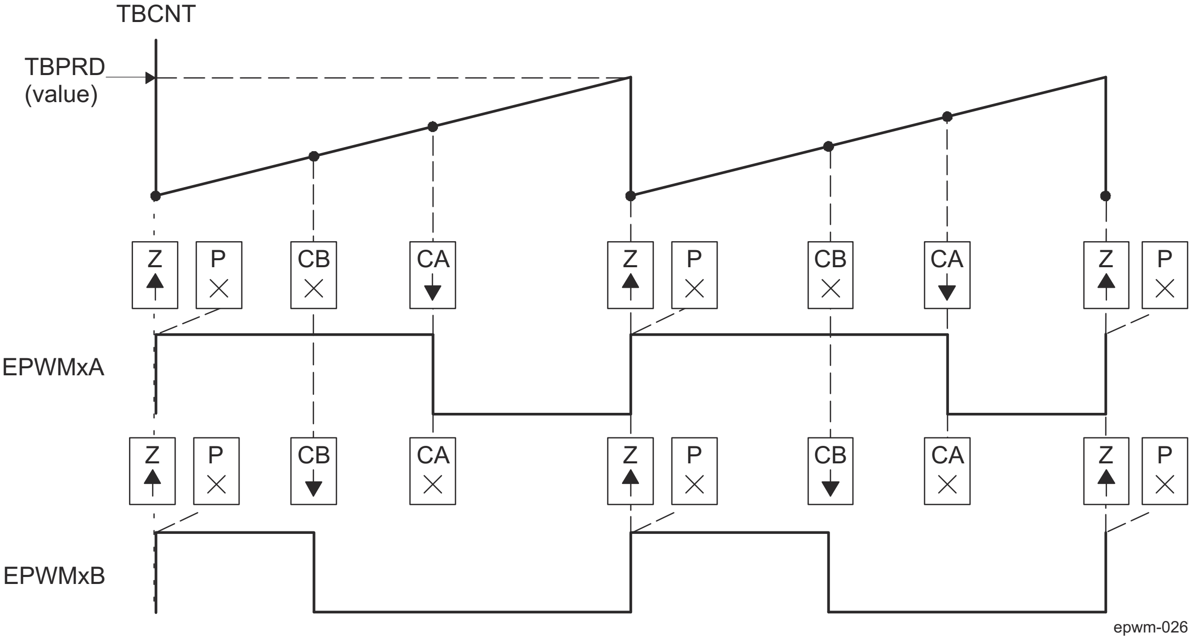

Note

PWM period = (TBPRD + 1) × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active high (that is, high time duty proportional to CMPA).

Note

Duty modulation for EPWMxB is set by CMPB and is active high (that is, high time duty proportional to CMPB).

Note

The "Do Nothing" actions (X) are shown for completeness, but will not be shown on subsequent diagrams.

Note

Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCNT wraps from period to 0000h.

Figure 12-348. Up, Single Edge Asymmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Active High

Table 12-394. EPWMx Initialization for Figure 12-348

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	200 (C8h)	Compare B = 200 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	ZRO	AQ_SET	
	CAU	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_SET	
	CBU	AQ_CLEAR	

Table 12-395. EPWMx Run Time Changes for Figure 12-348

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-384 and Table 12-385 contains initialization and runtime register configurations for the waveforms in Figure 12-349.

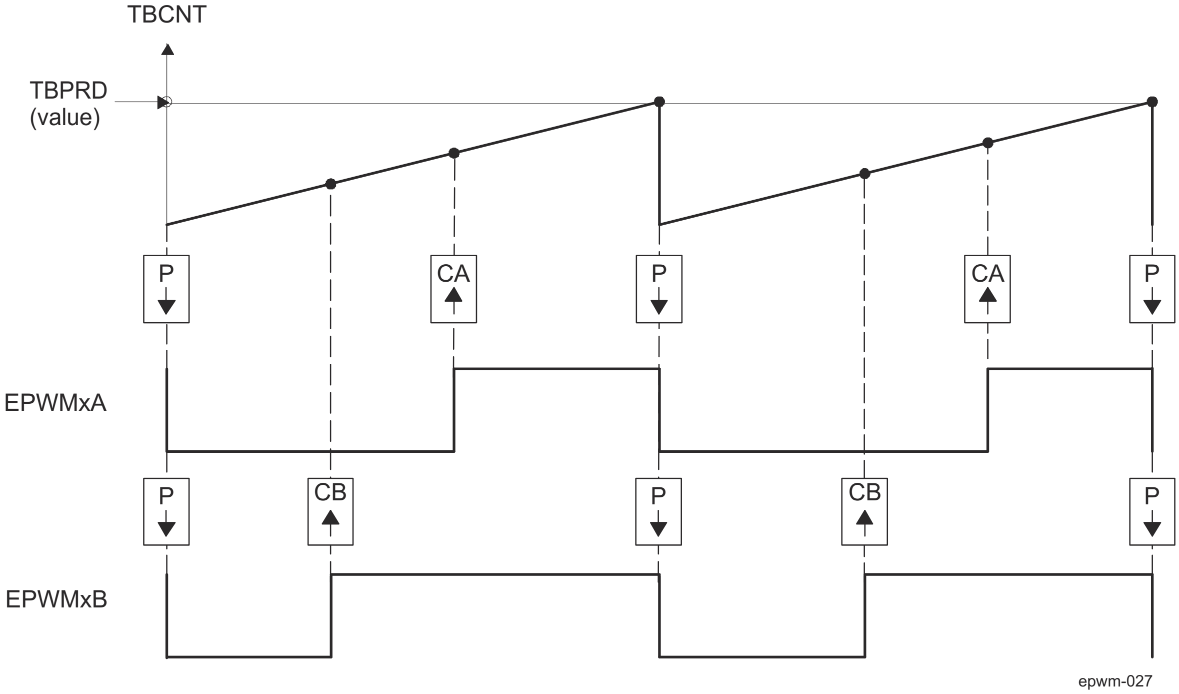

Note

PWM period = (TBPRD + 1) × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).

Note

Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

Note

The Do Nothing actions (X) are shown for completeness here, but will not be shown on subsequent diagrams.

Note

Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCNT wraps from period to 0000h.

Figure 12-349. Up, Single Edge Asymmetric Waveform With Independent Modulation on EPWMxA and EPWMxB — Active Low

Table 12-396. EPWMx Initialization for Figure 12-349

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	200 (C8h)	Compare B = 200 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	PRD	AQ_CLEAR	
	CAU	AQ_SET	
EPWM_AQCTLB	PRD	AQ_CLEAR	
	CBU	AQ_SET	

Table 12-397. EPWMx Run Time Changes for Figure 12-349

Register	Bit	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-386 and Table 12-387 contains initialization and runtime register configurations for the waveforms Figure 12-350. Use the code in *Constant Definitions Used in the EPWM Code Examples* to define the headers.

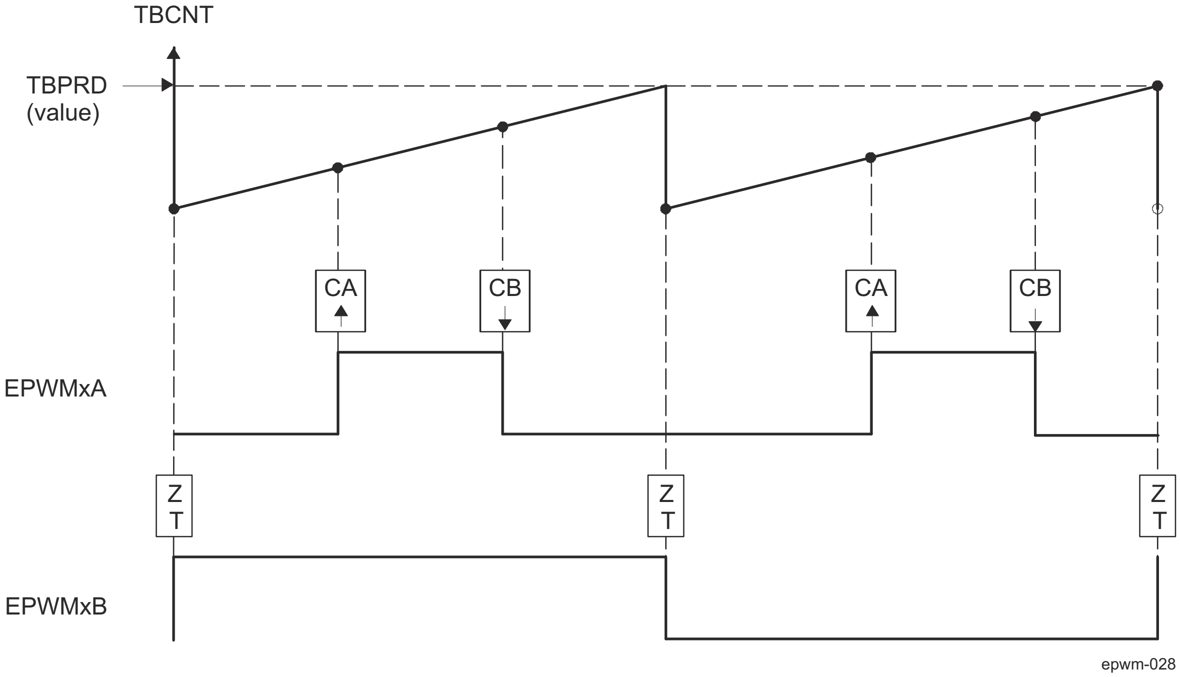

Note

PWM frequency = 1/((TBPRD + 1) × T_{TBCLK})

Note

Pulse can be placed anywhere within the PWM cycle (0000h - TBPRD)

Note

High time duty proportional to (CMPB - CMPA)

Note

EPWMxB can be used to generate a 50% duty square wave with frequency = 1/2 × ((TBPRD + 1) × TBCLK)

Figure 12-350. Up-Count, Pulse Placement Asymmetric Waveform With Independent Modulation on EPWMxA

Table 12-398. EPWMx Initialization for Figure 12-350

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	200 (C8h)	Compare A = 200 TBCLK counts
EPWM_CMPB	CMPB	400 (190h)	Compare B = 400 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CBU	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_TOGGLE	

Table 12-399. EPWMx Run Time Changes for Figure 12-350

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	EdgePosA	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	EdgePosB	

Table 12-388 and Table 12-389 contains initialization and runtime register configurations for the waveforms in Figure 12-351. Use the code in *Constant Definitions Used in the EPWM Code Examples* to define the headers.

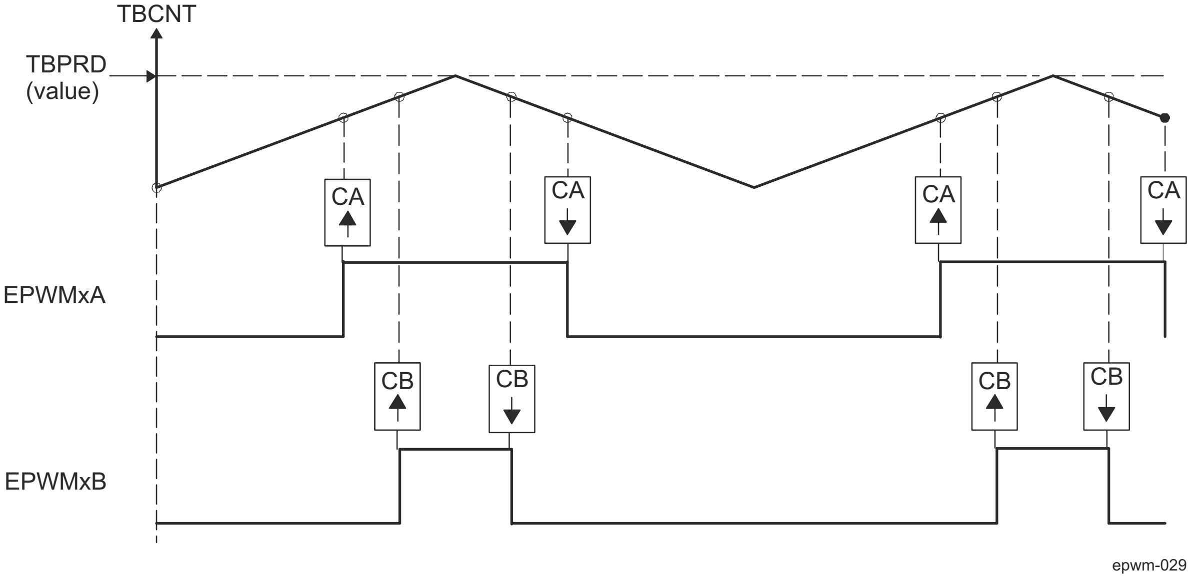

Note

PWM period = 2 x TBPRD × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).

Note

Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

Note

Outputs EPWMxA and EPWMxB can drive independent power switches.

Figure 12-351. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Active Low

Table 12-400. EPWMx Initialization for Figure 12-351

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	400 (190h)	Compare A = 400 TBCLK counts
EPWM_CMPB	CMPB	500 (1F4h)	Compare B = 500 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CAD	AQ_CLEAR	
EPWM_AQCTLB	CBU	AQ_SET	
	CBD	AQ_CLEAR	

Table 12-401. EPWMx Run Time Changes for Figure 12-351

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-390 and Table 12-391 contains initialization and runtime register configurations for the waveforms in Figure 12-352. Use the code in *Constant Definitions Used in the EPWM Code Examples* to define the headers.

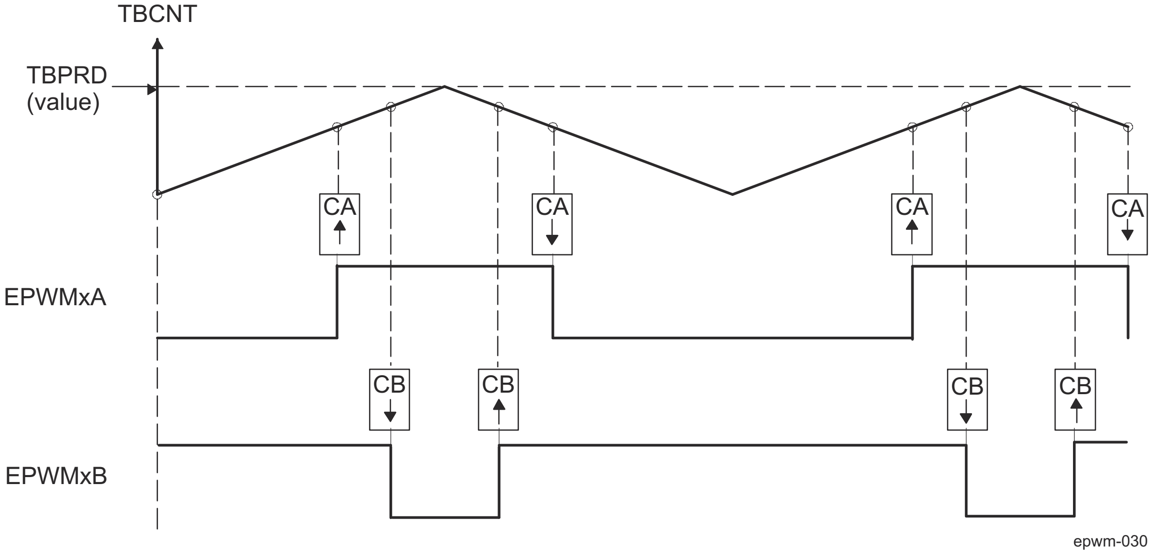

Note

PWM period = 2 × TBPRD × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low, that is, low time duty proportional to CMPA.

Note

Duty modulation for EPWMxB is set by CMPB and is active high, that is, high time duty proportional to CMPB.

Note

Outputs EPWMx can drive upper/lower (complementary) power switches.

Note

Dead-band = CMPB - CMPA (fully programmable edge placement by software). Note the dead-band module is also available if the more classical edge delay method is required.

Figure 12-352. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Complementary

Table 12-402. EPWMx Initialization for Figure 12-352

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	400 (190h)	Compare B = 400 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CAD	AQ_CLEAR	
EPWM_AQCTLB	CBU	AQ_CLEAR	
	CBD	AQ_SET	

Table 12-403. EPWMx Run Time Changes for Figure 12-352

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-392 and Table 12-393 contains initialization and runtime register configurations for the waveforms in Figure 12-353. Use the code in *Constant Definitions Used in the EPWM Code Examples* to define the headers.

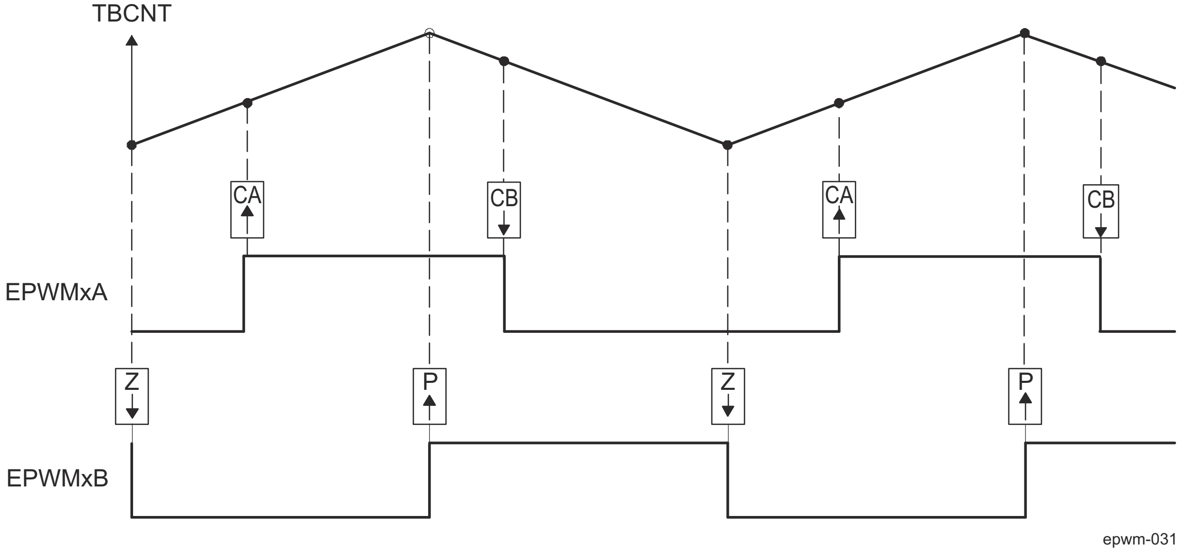

Note

PWM period = 2 × TBPRD × TBCLK

Note

Rising edge and falling edge can be asymmetrically positioned within a PWM cycle. This allows for pulse placement techniques.

Note

Duty modulation for EPWMxA is set by CMPA and CMPB.

Note

Low time duty for EPWMxA is proportional to (CMPA + CMPB).

Note

To change this example to active high, CMPA and CMPB actions need to be inverted (that is, Set ! Clear and Clear Set).

Note

Duty modulation for EPWMxB is fixed at 50% (utilizes spare action resources for EPWMxB).

Figure 12-353. Up-Down-Count, Dual Edge Asymmetric Waveform, With Independent Modulation on EPWMxA — Active Low

Table 12-404. EPWMx Initialization for Figure 12-353

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	250 (FAh)	Compare A = 250 TBCLK counts
EPWM_CMPB	CMPB	450 (1C2h)	Compare B = 450 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CBD	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_CLEAR	
	PRD	AQ_SET	

Table 12-405. EPWMx Run Time Changes for Figure 12-353

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	EdgePosA	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	EdgePosB	Adjust duty for output EPWM1B

12.4.3.4.5 EPWM Dead-Band Generator (DB) Submodule

This section describes the Dead-Band Generator (DB) submodule in the PWM module.

12.4.3.4.5.1 Overview

Figure 12-354 illustrates the dead-band generator submodule within the EPWM module.

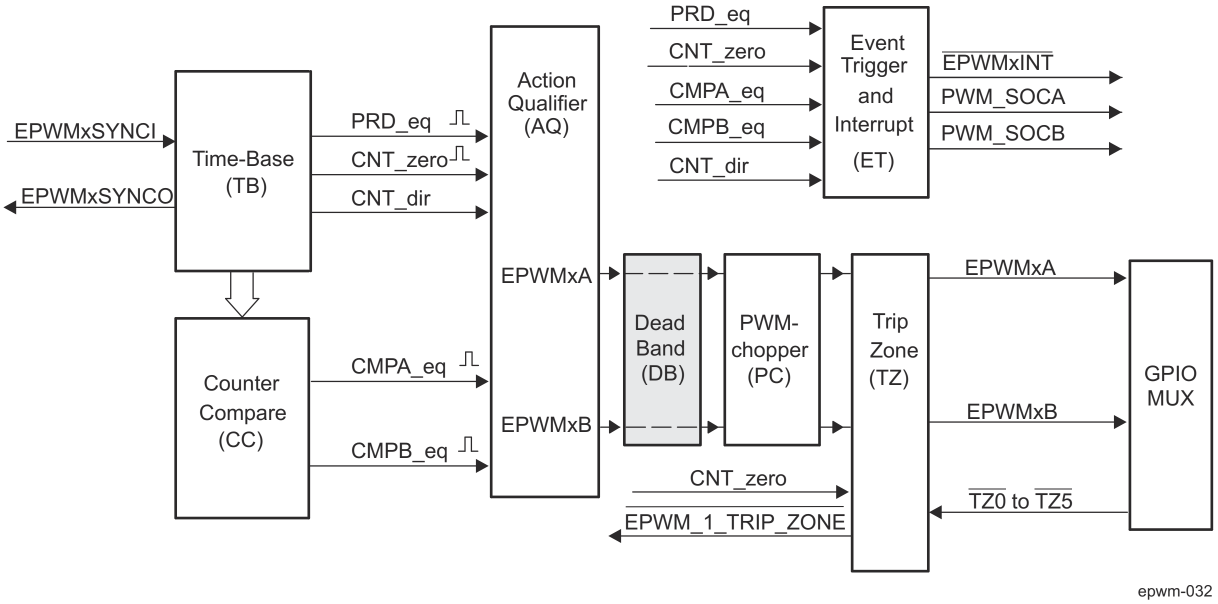

Figure 12-354. Dead-Band Generator Submodule

The "Action-qualifier (AQ) Module" section discussed how it is possible to generate the required dead-band by having full control over edge placement using both the CMPA and CMPB resources of the EPWM module. However, if the more classical edge delay-based dead-band with polarity control is required, then the dead-band generator submodule should be used.

The key functions of the dead-band generator submodule are:

- Generating appropriate signal pairs (EPWMxA and EPWMxB) with dead-band relationship from a single EPWMxA input
- Programming signal pairs for:
  - Active high (AH)
  - Active low (AL)
  - Active high complementary (AHC)
  - Active low complementary (ALC)
- Adding programmable delay to rising edges (RED)
- Adding programmable delay to falling edges (FED)
- Can be totally bypassed from the signal path (note dotted lines in Figure 12-354)

12.4.3.4.5.2 Controlling and Monitoring the EPWM Dead-Band Submodule

The dead-band generator submodule operation is controlled and monitored via the following registers:

Table 12-406. Dead-Band Generator Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_DBCTL	Dead-Band Control Register	1Eh	No
EPWM_DBRED	Dead-Band Rising Edge Delay Count Register	20h	No
EPWM_DBFED	Dead-Band Falling Edge Delay Count Register	22h	No

12.4.3.4.5.3 Operational Highlights for the EPWM Dead-Band Generator Submodule

The dead-band submodule has two groups of independent selection options as shown in Figure 12-355.

- **Input Source Selection:** The input signals to the dead-band module are the EPWMxA and EPWMxB output signals from the action-qualifier. In this section they will be referred to as EPWMxA In and EPWMxB In. Using the EPWM_DBCTL[5-4] IN_MODE control bits, the signal source for each delay, falling-edge or rising-edge, can be selected:
  - EPWMxA In is the source for both falling-edge and rising-edge delay. This is the default mode.
  - EPWMxA In is the source for falling-edge delay, EPWMxB In is the source for rising-edge delay.
  - EPWMxA In is the source for rising edge delay, EPWMxB In is the source for falling-edge delay.
  - EPWMxB In is the source for both falling-edge and rising-edge delay.
- **Output Mode Control:** The output mode is configured by way of the EPWM_DBCTL[1-0] OUT_MODE bit fields. These bits determine if the falling-edge delay, rising-edge delay, neither, or both are applied to the input signals.
- **Polarity Control:** The polarity control (EPWM_DBCTL[3-2] POLSEL) allows to be specified whether the rising-edge delayed signal and/or the falling-edge delayed signal is to be inverted before being sent out of the dead-band submodule.

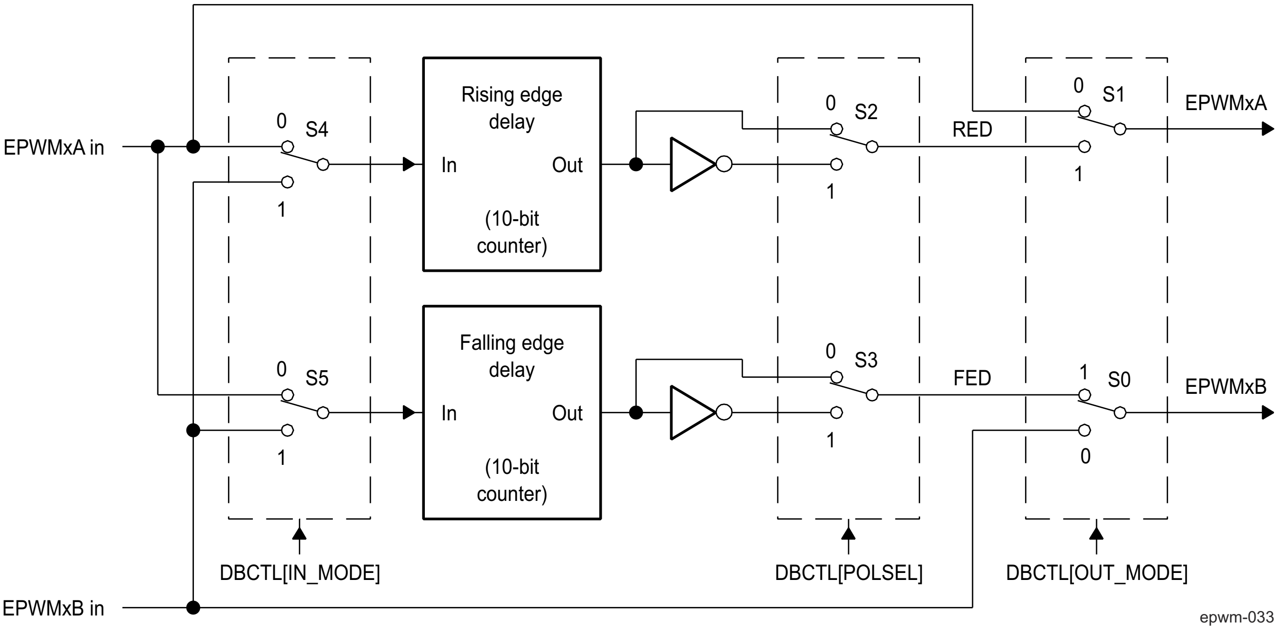

Figure 12-355. Configuration Options for the EPWM Dead-Band Generator Submodule

Although all combinations are supported, not all are typical usage modes. Table 12-395 lists some classical dead-band configurations. These modes assume that the EPWM_DBCTL[5-4] IN_MODE is configured such that EPWMxA In is the source for both falling-edge and rising-edge delay. Enhanced, or non-traditional modes can be achieved by changing the input signal source. The modes shown in Table 12-395 fall into the following categories:

- **Mode 1: Bypass both falling-edge delay (FED) and rising-edge delay (RED)** Allows to be fully disabled the dead-band submodule from the PWM signal path.
- **Mode 2-5: Classical Dead-Band Polarity Settings** These represent typical polarity configurations that should address all the active high/low modes required by available industry power switch gate drivers. The waveforms for these typical cases are shown in Figure 12-356. Note that to generate equivalent waveforms to Figure 12-356, configure the action-qualifier submodule to generate the signal as shown for EPWMxA.
- **Mode 6: Bypass rising-edge-delay and Mode 7: Bypass falling-edge-delay** Finally the last two entries in Table 12-395 show combinations where either the falling-edge-delay (FED) or rising-edge-delay (RED) blocks are bypassed.

Table 12-407. Classical Dead-Band Operating Modes

		EPWM_DBCTL[3-2] POLSEL		EPWM_DBCTL[1-0] OUT_MODE	
Mode	**Mode Description** (1)	**S3**	**S2**	**S1**	**S0**
1	EPWMxA and EPWMxB Passed Through (No Delay)	x	x	0	0
2	Active High Complementary (AHC)	1	0	1	1
3	Active Low Complementary (ALC)	0	1	1	1
4	Active High (AH)	0	0	1	1
5	Active Low (AL)	1	1	1	1
6	EPWMxA Out = EPWMxA In (No Delay) EPWMxB Out = EPWMxA In with Falling Edge Delay	0 or 1	0 or 1	0	1
7	EPWMxA Out = EPWMxA In with Rising Edge Delay EPWMxB Out = EPWMxB In with No Delay	0 or 1	0 or 1	1	0

(1) These are classical dead-band modes and assume that EPWM_DBCTL[5-4] IN_MODE = 0b00. That is, EPWMxA in is the source for both the falling-edge and rising-edge delays. Enhanced, non-traditional modes can be achieved by changing the IN_MODE configuration.

Figure 12-356 shows waveforms for typical cases where 0% < duty < 100%.

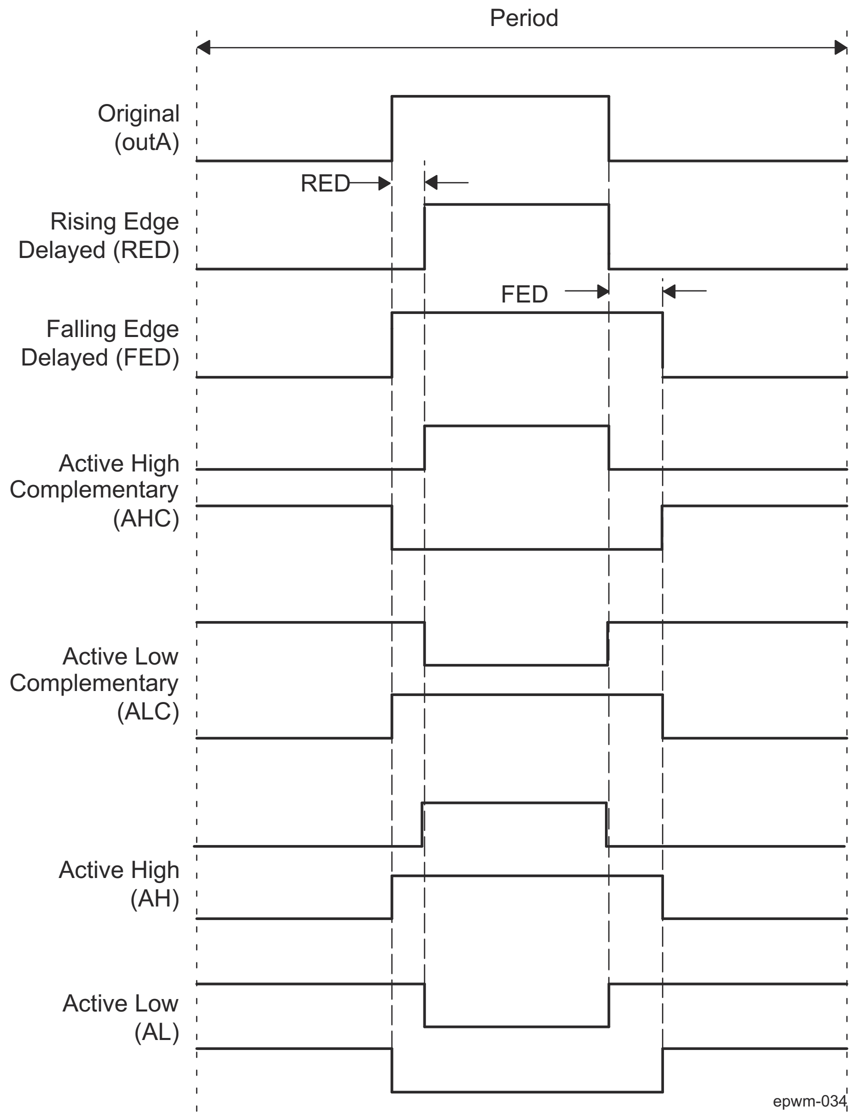

Figure 12-356. Dead-Band Waveforms for Typical Cases (0% < Duty < 100%)

The dead-band submodule supports independent values for rising-edge (RED) and falling-edge (FED) delays. The amount of delay is programmed using the EPWM_DBRED and EPWM_DBFED registers. These are 10-bit registers and their value represents the number of time-base clock, TBCLK, periods a signal edge is delayed by. For example, the formulas to calculate falling-edge-delay and rising-edge-delay are:

$FED = EPWM\_DBFED \times T_{TBCLK}$

$RED = EPWM\_DBRED \times T_{TBCLK}$

Where T_{TBCLK} is the period of TBCLK, the prescaled version of FICLK.

12.4.3.4.6 EPWM-Chopper (PC) Submodule

This section describes the PWM-Chopper (PC) submodule in the PWM module.

12.4.3.4.6.1 Overview

Figure 12-357 illustrates the PWM-chopper (PC) submodule within the EPWM module. The PWM-chopper submodule allows a high-frequency carrier signal to modulate the PWM waveform generated by the action-qualifier and dead-band submodules. This capability is important if a pulse transformer-based gate drivers to control the power switching elements is needed.

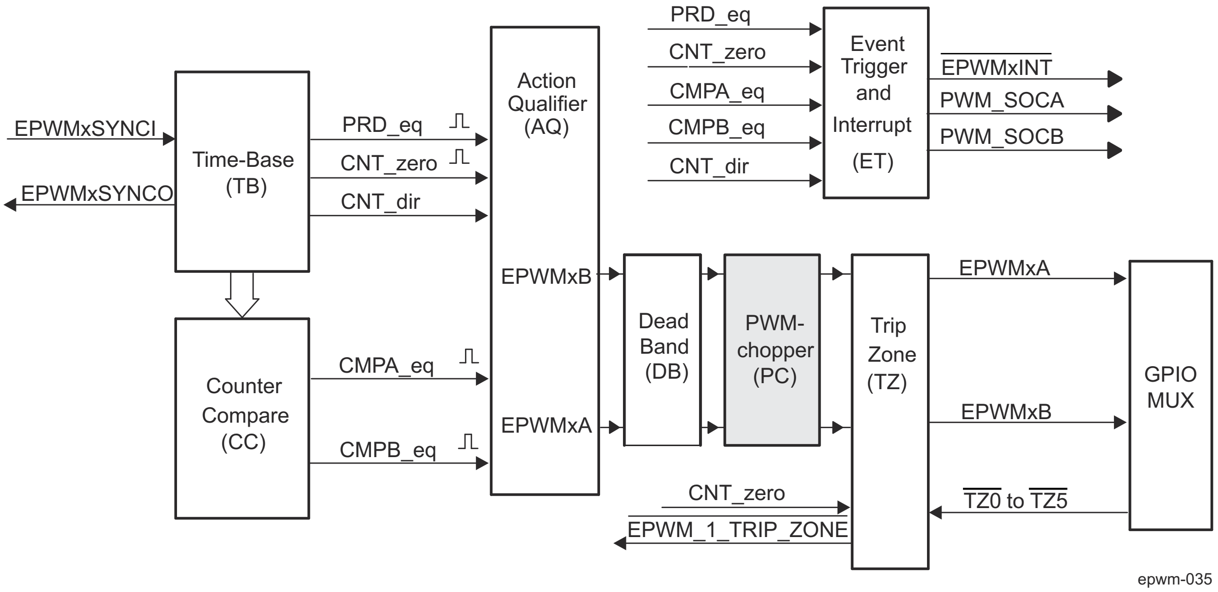

Figure 12-357. PWM-Chopper Submodule

PC module key features:

- Programmable chopping (carrier) frequency
- Programmable pulse width of first pulse
- Programmable duty cycle of second and subsequent pulses
- Can be fully bypassed if not required

12.4.3.4.6.2

PC module key features:

- Programmable chopping (carrier) frequency
- Programmable pulse width of first pulse
- Programmable duty cycle of second and subsequent pulses
- Can be fully bypassed if not required

12.4.3.4.6.3 Controlling the EPWM-Chopper Submodule

The EPWM-chopper submodule operation is controlled via the register in Table 12-396.

Table 12-408. EPWM-Chopper Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_PCCTL	PWM-chopper Control Register	3Ch	No

12.4.3.4.6.4 Operational Highlights for the EPWM-Chopper Submodule

Figure 12-358 shows the operational details of the EPWM-chopper submodule. The carrier clock is derived from FICLK. Its frequency and duty cycle are controlled via the CHPFREQ and CHPDUTY bits in the EPWM_PCCTL register. The one-shot block is a feature that provides a high energy first pulse to ensure hard and fast power switch turn on, while the subsequent pulses sustain pulses, ensuring the power switch remains on. The one-shot width is programmed via the OSHTWTH bits. The PWM-chopper submodule can be fully disabled (bypassed) via the CHPEN bit.

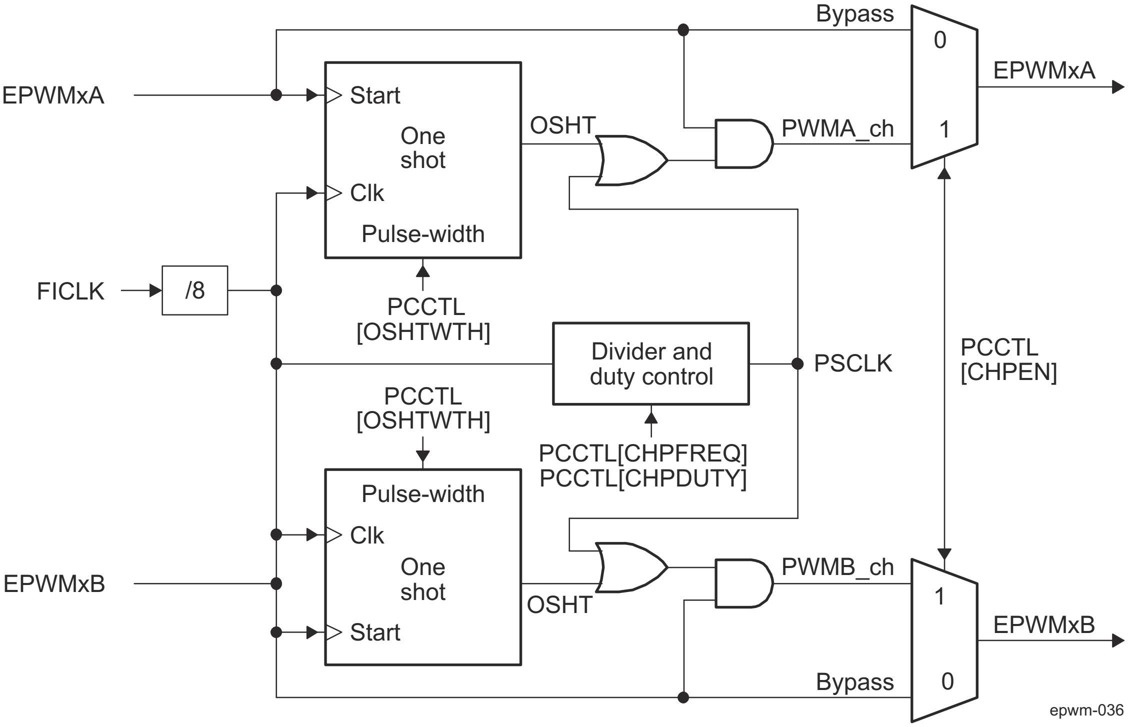

Figure 12-358. PWM-Chopper Submodule Signals and Registers

12.4.3.4.6.5 EPWM-Chopper Waveforms

Figure 12-359 shows simplified waveforms of the chopping action only; one-shot and duty-cycle control are not shown. Details of the one-shot and duty-cycle control are discussed in the following sections.

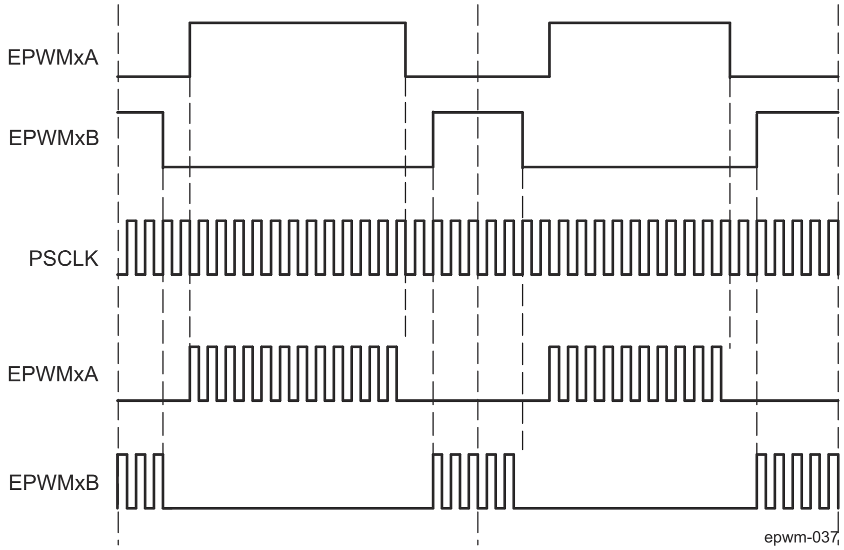

Figure 12-359. Simple EPWM-Chopper Submodule Waveforms Showing Chopping Action Only

12.4.3.4.6.5.1 EPWM-Chopper One-Shot Pulse

The width of the first pulse can be programmed to any of 16 possible pulse width values. The width or period of the first pulse is given by:

$T_{1stpulse} = T_{FICLK} \times 8 \times OSHTWTH$

Where T_{FICLK} is the period of the system clock (FICLK) and OSHTWTH is the four control bits (value from 1 to 16)

Figure 12-360 shows the first and subsequent sustaining pulses.

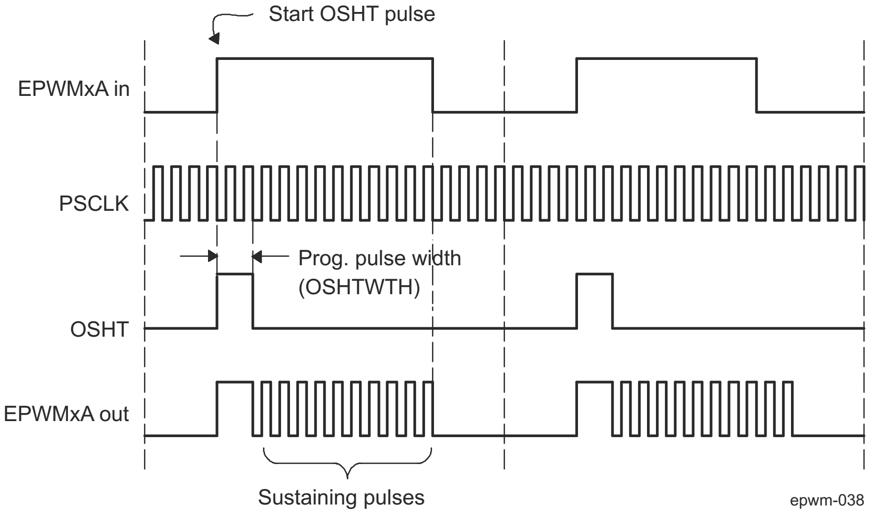

Figure 12-360. EPWM-Chopper Submodule Waveforms Showing the First Pulse and Subsequent Sustaining Pulses

12.4.3.4.6.5.2 EPWM-Chopper Duty Cycle Control

Pulse transformer-based gate drive designs need to comprehend the magnetic properties or characteristics of the transformer and associated circuitry. Saturation is one such consideration. To assist the gate drive designer, the duty cycles of the second and subsequent pulses have been made programmable. These sustaining pulses ensure the correct drive strength and polarity is maintained on the power switch gate during the on period, and hence a programmable duty cycle allows a design to be tuned or optimized via software control.

Figure 12-361 shows the duty cycle control that is possible by programming the CHPDUTY bits. One of seven possible duty ratios can be selected ranging from 12.5 to 87.5%.

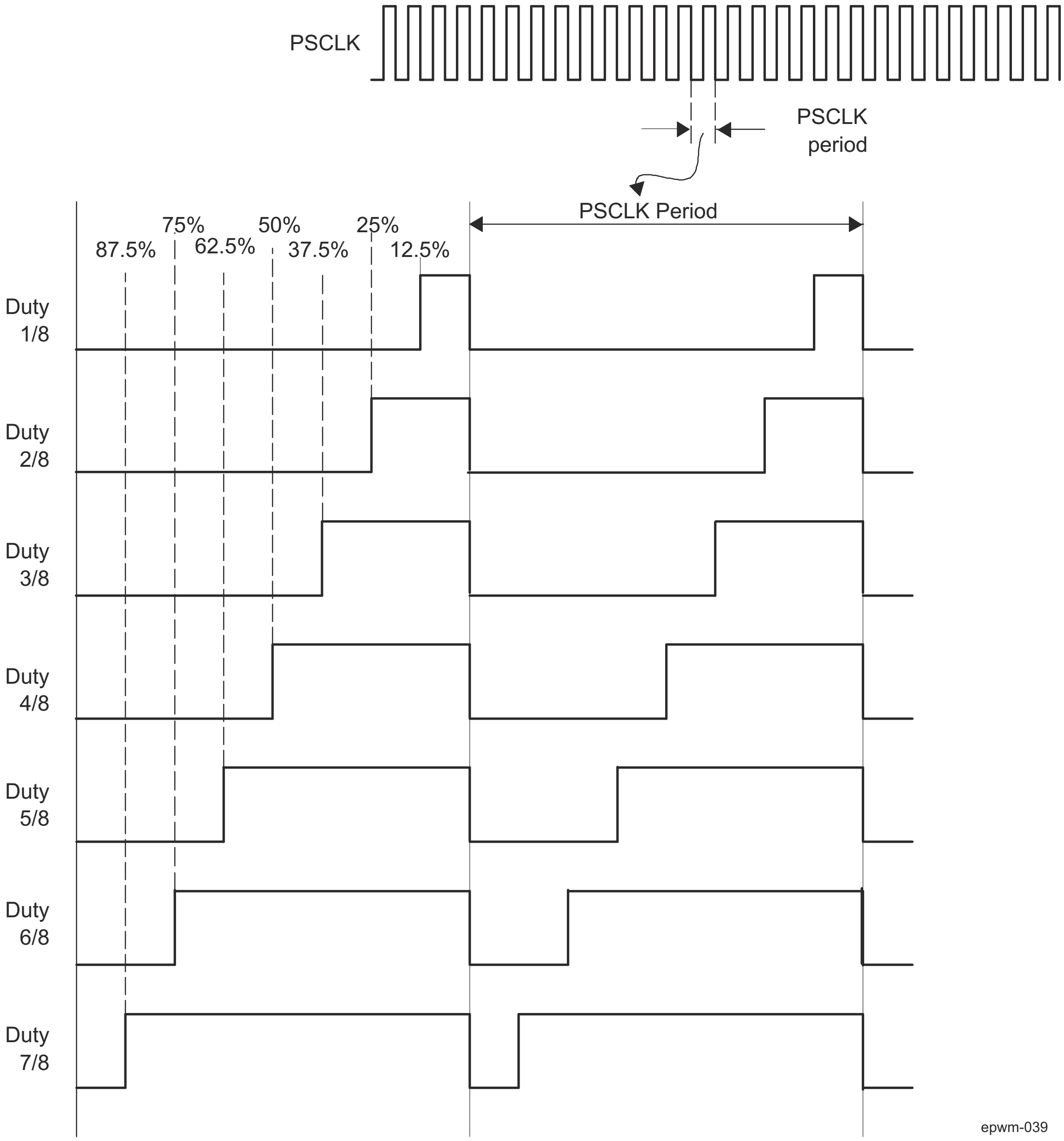

Figure 12-361. EPWM-Chopper Submodule Waveforms Showing the Pulse Width (Duty Cycle) Control of Sustaining Pulses

12.4.3.4.7 EPWM Trip-Zone (TZ) Submodule

This section describes the Trip-Zone (TZ) submodule in the PWM module.

12.4.3.4.7.1 Overview

Figure 12-362 shows how the trip-zone (TZ) submodule fits within the EPWM module. Each EPWM module is connected to six $\overline{\text{TZ}}$ signals ($\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$) that are sourced from the GPIO MUX. These signals indicates external fault or trip conditions, and the EPWM outputs can be programmed to respond accordingly when faults occur. See *EPWM Integration* to determine the number of trip-zone pins available for the device.

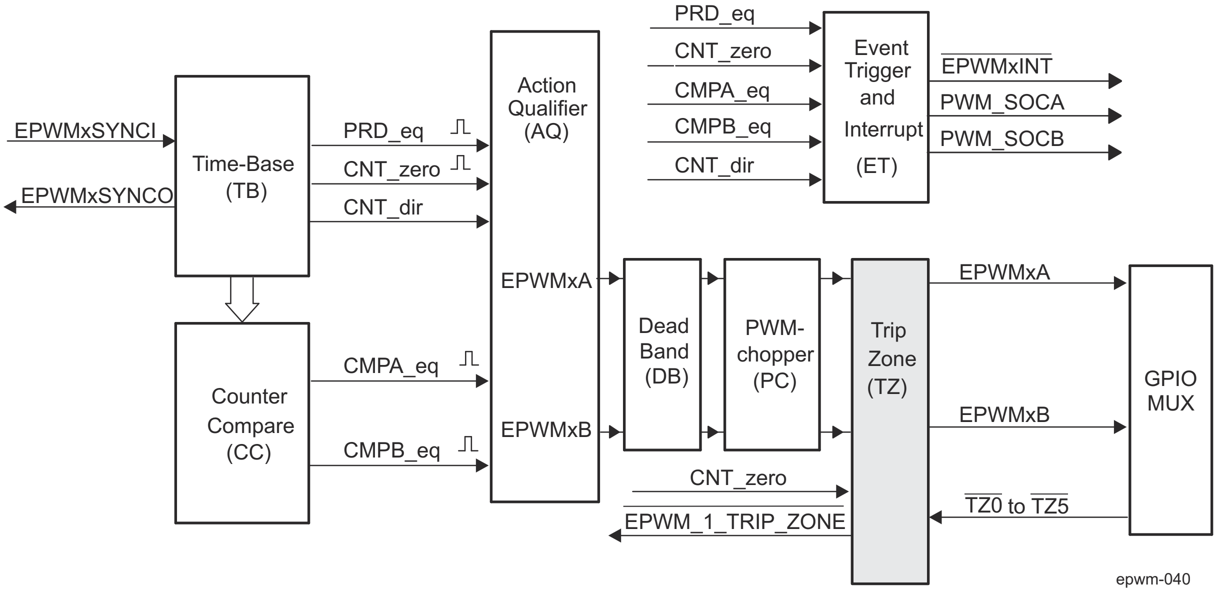

Figure 12-362. EPWM Trip-Zone Submodule

The key functions of the trip-zone submodule are:

- Trip inputs $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ can be flexibly mapped to any EPWM module.
- Upon a fault condition, outputs EPWMxA and EPWMxB can be forced to one of the following:
  - High
  - Low
  - High-impedance
  - No action taken
- Support for one-shot trip (OSHT) for major short circuits or over-current conditions.
- Support for cycle-by-cycle tripping (CBC) for current limiting operation.
- Each trip-zone input pin can be allocated to either one-shot or cycle-by-cycle operation.
- Interrupt generation is possible on any trip-zone pin.
- Software-forced tripping is also supported.
- The trip-zone submodule can be fully bypassed if it is not required.

Note

For each EPWMx module, 6 tripzone input events are supported ($\overline{\text{EPWMx\_TRIP\_TZ[5:0]}}$). Each tripzone input for all EPWMx modules (where x = 0 to 5) are tied to a common tripzone input pin, so that any EPWMx can be triggered by any of the six tripzone inputs.

12.4.3.4.7.2 Controlling and Monitoring the EPWM Trip-Zone Submodule

The trip-zone submodule operation is controlled and monitored through the following registers:

Table 12-409. EPWM Trip-Zone Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_TZSEL	Trip-Zone Select Register (1)	24h	No
EPWM_TZCTL	Trip-Zone Control Register (1)	28h	No
EPWM_TZEINT	Trip-Zone Enable Interrupt Register (1)	2Ah	No
EPWM_TZFLG	Trip-Zone Flag Register (1)	2Ch	No
EPWM_TZCLR	Trip-Zone Clear Register (1)	2Eh	No
EPWM_TZFRC	Trip-Zone Force Register (1)	30h	No

(1) All trip-zone registers are EALLOW protected and can be modified only after executing the EALLOW instruction.

12.4.3.4.7.3 Operational Highlights for the EPWM Trip-Zone Submodule

The trip-zone signals at pin $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ is an active-low input signal. When the pin goes low, it indicates that a trip event has occurred. Each EPWM module can be individually configured to ignore or use each of the trip-zone pins. Which trip-zone pins are used by a particular EPWM module is determined by the EPWM_TZSEL register for that specific EPWM module. The trip-zone signal may or may not be synchronized to the system clock (FICLK). A minimum of 1 FICLK low pulse on the $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs is sufficient to trigger a fault condition in the EPWM module. The asynchronous trip makes sure that if clocks are missing for any reason, the outputs can still be tripped by a valid event present on the $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs.

The $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs can be individually configured to provide either a cycle-by-cycle or one-shot trip event for a EPWM module. The configuration is determined by the EPWM_TZSEL[5-0] CBCk and EPWM_TZSEL[13-8] OSHTk bit field (where k = 0 to 5 corresponds to the trip pin), respectively.

- **Cycle-by-Cycle (CBC):** When a cycle-by-cycle trip event occurs, the action specified in the EPWM_TZCTL register is carried out immediately on the EPWMxA and/or EPWMxB output. Table 12-398 lists the possible actions. In addition, the cycle-by-cycle trip event flag (EPWM_TZFLG[1] CBC) is set and a EPWMxTZINT interrupt is generated if it is enabled in the EPWM_TZEINT register.

  The specified condition on the pins is automatically cleared when the EPWM time-base counter reaches zero (EPWM_TBCNT[15-0] TBCNT = 0000h) if the trip event is no longer present. Therefore, in this mode, the trip event is cleared or reset every PWM cycle. The EPWM_TZFLG[1] CBC flag bit will remain set until it is manually cleared by writing to the EPWM_TZCLR[1] CBC bit. If the cycle-by-cycle trip event is still present when the EPWM_TZFLG[1] CBC bit is cleared, then it will again be immediately set.
- **One-Shot (OSHT):** When a one-shot trip event occurs, the action specified in the EPWM_TZCTL register is carried out immediately on the EPWMxA and/or EPWMxB output. Table 12-398 lists the possible actions. In addition, the one-shot trip event flag (EPWM_TZFLG[2] OST) is set and a EPWMxTZINT interrupt is generated if it is enabled in the EPWM_TZEINT register. The one-shot trip condition must be cleared manually by writing to the EPWM_TZCLR[2] OST bit.

The action taken when a trip event occurs can be configured individually for each of the EPWM output pins by way of the EPWM_TZCTL[1-0] TZA and EPWM_TZCTL[3-2] TZB register bit field. One of four possible actions, shown in Table 12-398, can be taken on a trip event.

Table 12-410. Possible Actions On an EPWM Trip Event

EPWM_TZCTL[1-0] TZA and/or EPWM_TZCTL[3-2] TZB	EPWMxA and/or EPWMxB	Comment
0	High-Impedance	Tripped
1h	Force to High State	Tripped
2h	Force to Low State	Tripped
3h	No Change	Do Nothing. No change is made to the output.

Example of EPWM Trip-Zone Configurations

A one-shot trip event on $\overline{\text{TZ0}}$ pulls both EPWM1A, EPWM1B low and also forces EPWM2A and EPWM2B high.

- Configure the EPWM1 registers as follows:
  - EPWM_TZSEL[8] OSHT1 = 1: enables $\overline{\text{TZ}}$ as a one-shot event source for EPWM1
  - EPWM_TZCTL[1-0] TZA = 2: EPWM1A will be forced low on a trip event
  - EPWM_TZCTL[3-2] TZB = 2: EPWM1B will be forced low on a trip event
- Configure the EPWM2 registers as follows:
  - EPWM_TZSEL[8] OSHT1 = 1: enables $\overline{\text{TZ}}$ as a one-shot event source for EPWM2
  - EPWM_TZCTL[1-0] TZA = 1: EPWM2A will be forced high on a trip event
  - EPWM_TZCTL[3-2] TZB = 1: EPWM2B will be forced high on a trip event

12.4.3.4.7.4 Generating EPWM Trip-Event Interrupts

Figure 12-363 and Figure 12-364 illustrate the trip-zone submodule control and interrupt logic, respectively.

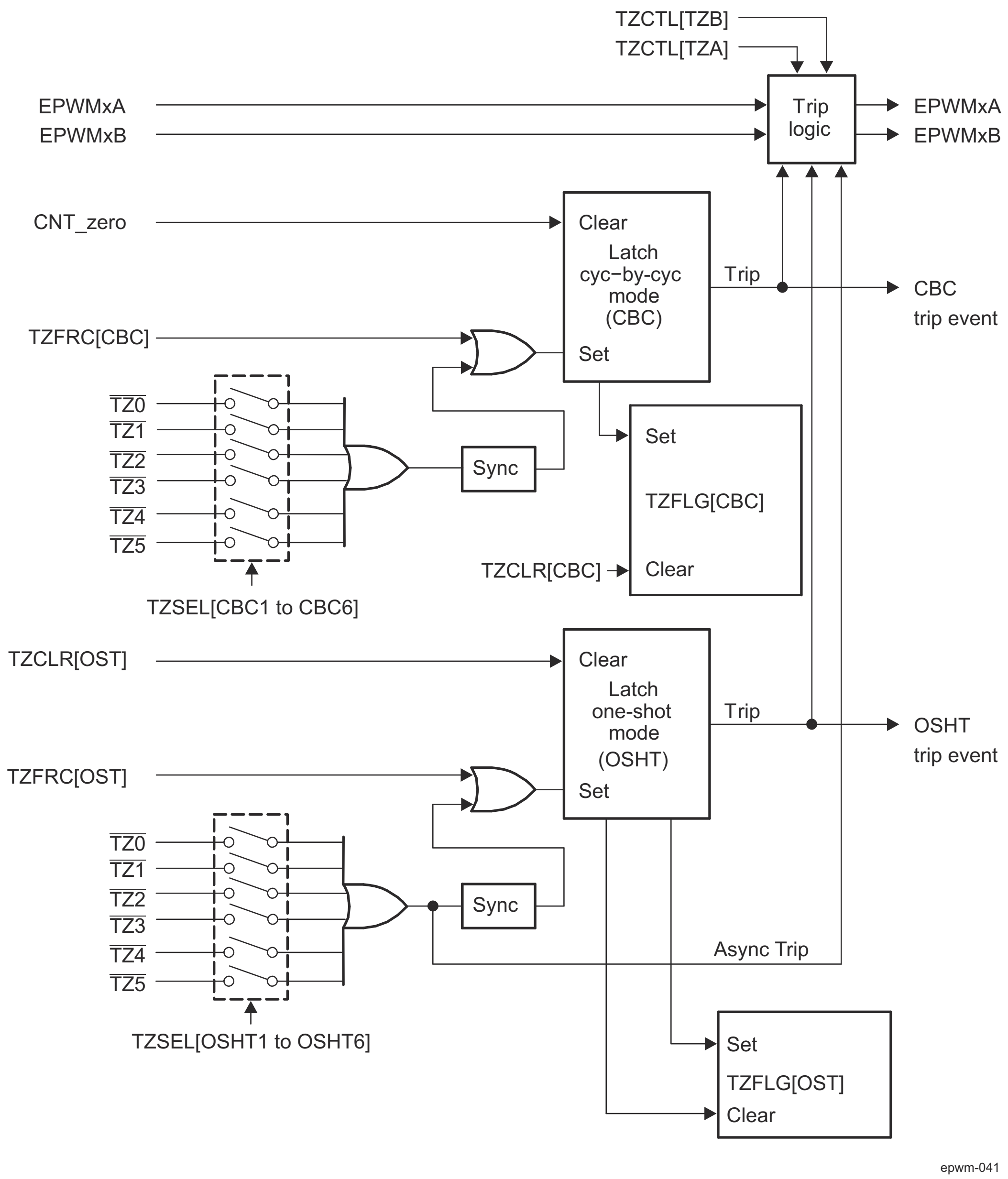

Figure 12-363. EPWM Trip-Zone Submodule Mode Control Logic

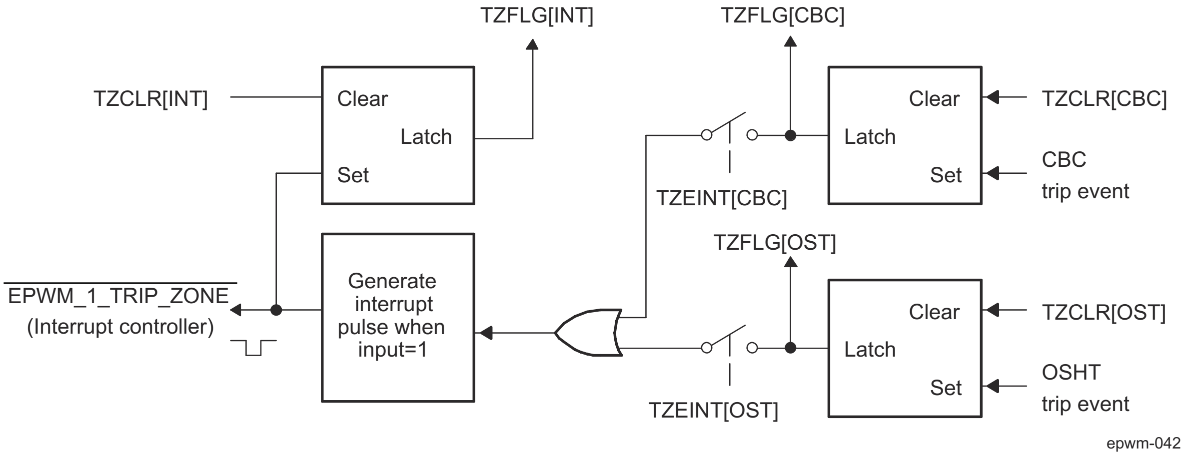

Figure 12-364. EPWM Trip-Zone Submodule Interrupt Logic

12.4.3.4.8 EPWM Event-Trigger (ET) Submodule

This section describes the Event-Trigger (ET) submodule in the PWM module.

12.4.3.4.8.1 Overview

Figure 12-365 shows the event-trigger (ET) submodule in the EPWM system. The event-trigger submodule manages the events generated by the time-base submodule and the counter-compare submodule to generate an aggregated interrupt request.

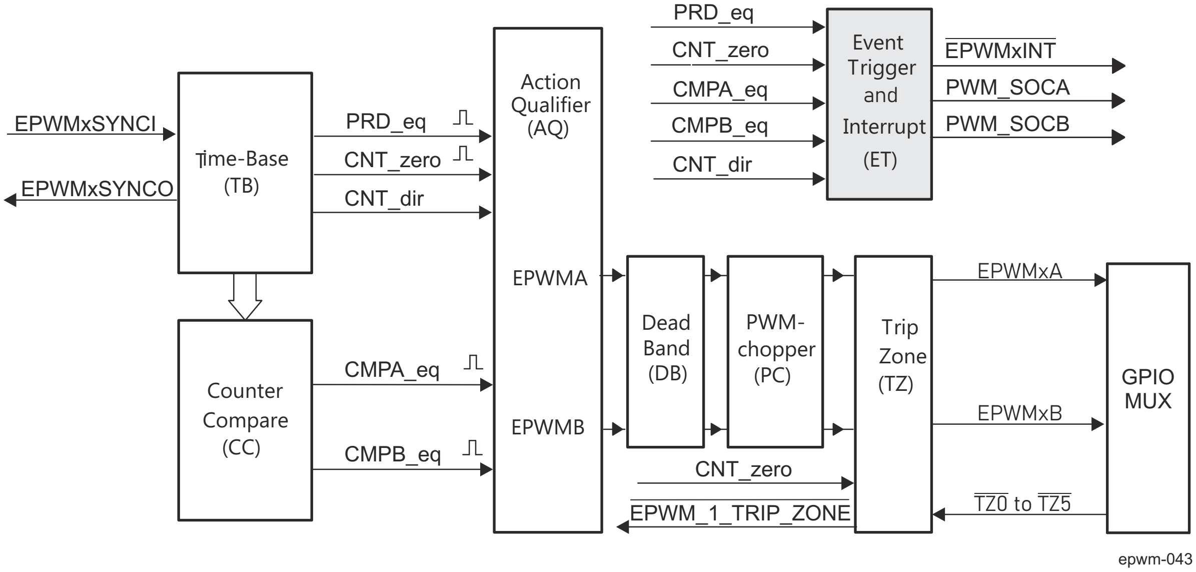

Figure 12-365. EPWM Event-Trigger Submodule

The key functions of the event-trigger submodule are:

- Receives event inputs generated by the time-base and counter-compare submodules
- Uses the time-base direction information for up/down event qualification
- Uses prescaling logic to issue interrupt requests at:
  - Every event
  - Every second event
  - Every third event
- Provides full visibility of event generation via event counters and flags

12.4.3.4.8.2 Controlling and Monitoring the EPWM Event-Trigger Submodule

The key registers used to configure the event-trigger submodule are shown in Table 12-399:

Table 12-411. EPWM Event-Trigger Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_ETSEL	Event-Trigger Selection Register	32h	No
EPWM_ETPS	Event-Trigger Prescale Register	34h	No
EPWM_ETFLG	Event-Trigger Flag Register	36h	No
EPWM_ETCLR	Event-Trigger Clear Register	38h	No
EPWM_ETFRC	Event-Trigger Force Register	3Ah	No

12.4.3.4.8.3 Operational Overview of the EPWM Event-Trigger Submodule

Each EPWM module has one interrupt request line as shown in Figure 12-366. Mapping interrupt lines to device host interrupt controllers is device specific and is covered in *EPWM Integration*.

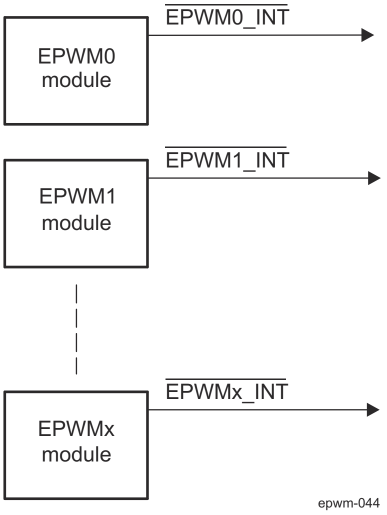

Figure 12-366. EPWM Event-Trigger Submodule Inter-Connectivity to Interrupt Controller

The event-trigger submodule monitors various event conditions (the left side inputs to event-trigger submodule shown in Figure 12-367) and can be configured to prescale these events before issuing an Interrupt request. The event-trigger prescaling logic can issue Interrupt requests at:

- Every event
- Every second event
- Every third event

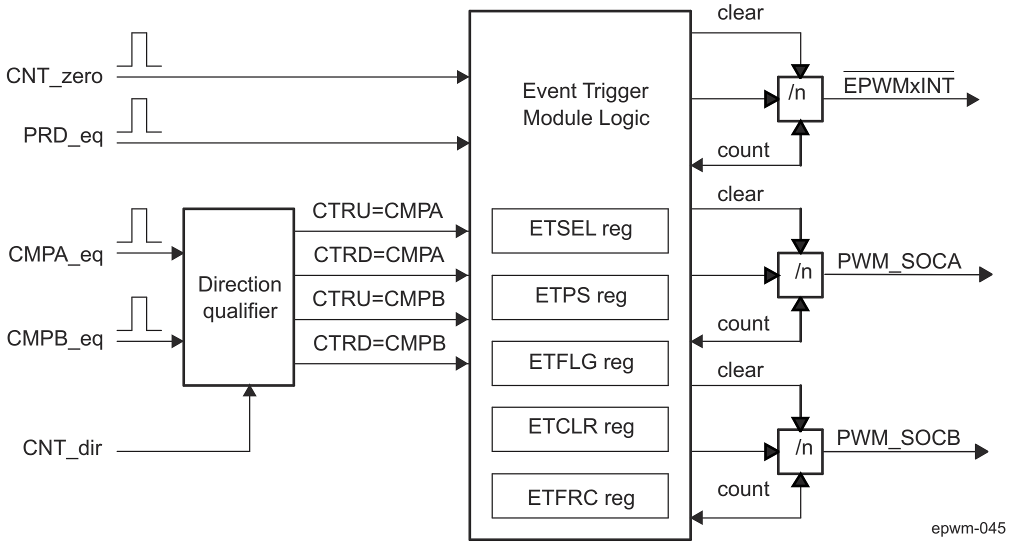

Figure 12-367. EPWM Event-Trigger Submodule Showing Event Inputs and Prescaled Outputs

- ETSEL — This selects which of the possible events will trigger an interrupt.
- ETPS — This programs the event prescaling options previously mentioned.
- ETFLG — These are flag bits indicating status of the selected and prescaled events.
- ETCLR — These bits allow to clear the flag bits in the EPWM_ETFLG register via software.
- ETFRC — These bits allow software forcing of an event. Useful for debugging or software intervention.

A more detailed look at how the various register bits interact with the Interrupt is shown in Figure 12-368.

Figure 12-368 shows the event-trigger's interrupt generation logic. The interrupt-period (EPWM_ETPS[1-0] INTPRD) bits specify the number of events required to cause an interrupt pulse to be generated. The choices available are:

- Do not generate an interrupt
- Generate an interrupt on every event
- Generate an interrupt on every second event
- Generate an interrupt on every third event

An interrupt cannot be generated on every fourth or more events.

Which event can cause an interrupt is configured by the interrupt selection (EPWM_ETSEL[2-0] INTSEL) bits. The event can be one of the following:

- Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h).
- Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD).
- Time-base counter equal to the compare A register (EPWM_CMPA) when the timer is incrementing.
- Time-base counter equal to the compare A register (EPWM_CMPA) when the timer is decrementing.
- Time-base counter equal to the compare B register (EPWM_CMPB) when the timer is incrementing.
- Time-base counter equal to the compare B register (EPWM_CMPB) when the timer is decrementing.

The number of events that have occurred can be read from the interrupt event counter (EPWM_ETPS[3-2] INTCNT) register bits. That is, when the specified event occurs the EPWM_ETPS[3-2] INTCNT bits are incremented until they reach the value specified by the EPWM_ETPS[1-0] INTPRD bit field. When EPWM_ETPS[3-2] INTCNT = EPWM_ETPS[1-0] INTPRD the counter stops counting and its output is set. The counter is only cleared when an interrupt is sent to the interrupt controller.

When EPWM_ETPS[3-2] INTCNT reaches EPWM_ETPS[1-0] INTPRD, one of the following behaviors will occur:

- If interrupts are enabled, EPWM_ETSEL[3] INTEN = 1h and the interrupt flag is clear, EPWM_ETFLG[0] INT = 0h, then an interrupt pulse is generated and the interrupt flag is set, EPWM_ETFLG[0] INT = 1h, and the event counter is cleared EPWM_ETPS[3-2] INTCNT = 0h. The counter will begin counting events again.
- If interrupts are disabled, EPWM_ETSEL[3] INTEN = 0, or the interrupt flag is set, EPWM_ETFLG[0] INT = 1h, the counter stops counting events when it reaches the period value EPWM_ETPS[3-2] INTCNT = EPWM_ETPS[1-0] INTPRD.
- If interrupts are enabled, but the interrupt flag is already set, then the counter will hold its output high until the ENTFLG[0] INT flag is cleared. This allows for one interrupt to be pending while one is serviced.

Writing to the INTPRD bits will automatically clear the counter INTCNT = 0 and the counter output will be reset (so no interrupts are generated). Writing a 1h to the EPWM_ETFRC[0] INT bit will increment the event counter INTCNT. The counter will behave as described above when INTCNT = INTPRD. When INTPRD = 0h, the counter is disabled and hence no events will be detected and the EPWM_ETFRC[0] INT bit is also ignored.

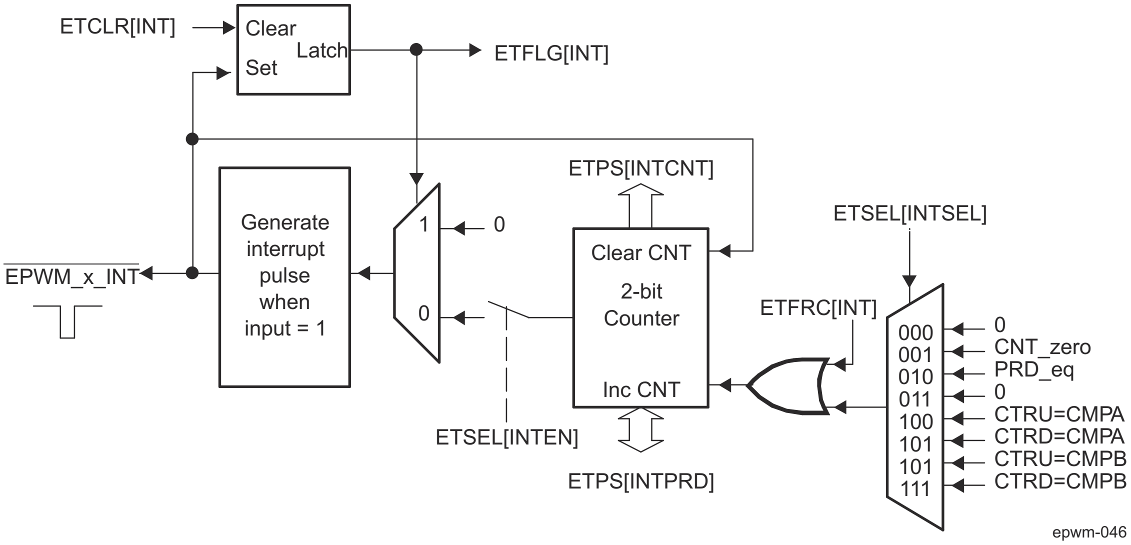

Figure 12-368. EPWM Event-Trigger Interrupt Generator

12.4.3.4.8.4 Operation Overview of the EPWM SOCx Pulse Generator

Figure 12-369 shows the operation of the event-trigger's start-of-conversion-A (SOCA) pulse generator. The EPWM_ETPS[11-10] SOCACNT counter and EPWM_ETPS[9-8] SOCAPRD period values behave similarly to the interrupt generator except that the pulses are continuously generated. That is, the pulse flag EPWM_ETFLG[2] SOCA is latched when a pulse is generated, but it does not stop further pulse generation. The enable/disable EPWM_ETSEL[11] SOCAEN bit stops pulse generation, but input events can still be counted until the period value is reached as with the interrupt generation logic. The event that will trigger an SOCA and SOCB pulse can be configured separately in the EPWM_ETSEL[10-8] SOCASEL and EPWM_ETSEL[14-12] SOCBSEL bit field. The possible events are the same events that can be specified for the interrupt generation logic.

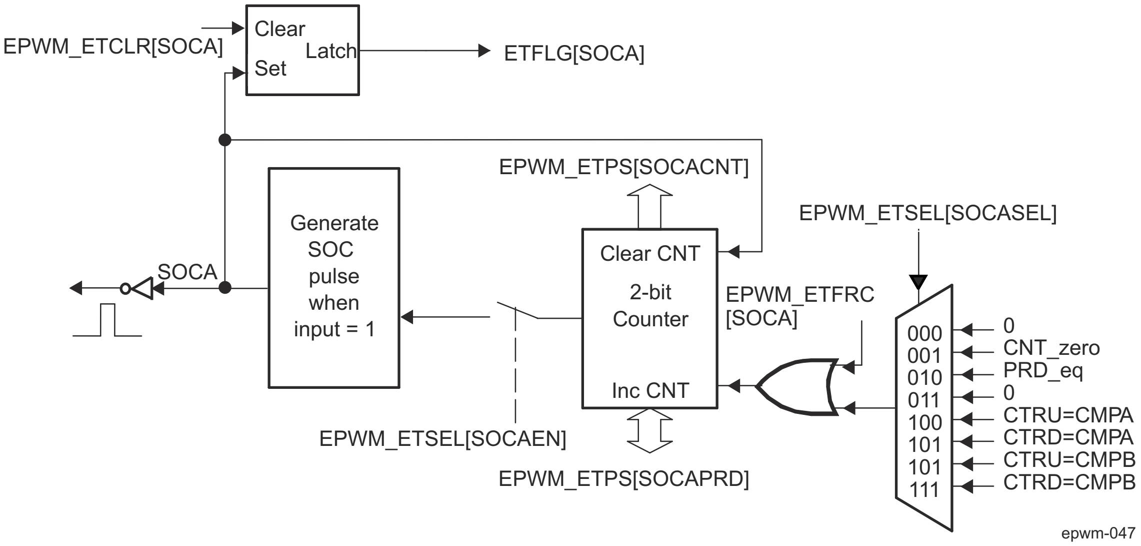

Figure 12-369. EPWM Event-Trigger SOCA Pulse Generator

Figure 12-370 shows the operation of the event-trigger's start-of-conversion-B (SOCB) pulse generator. The event-trigger's SOCB pulse generator operates the same way as the SOCA.

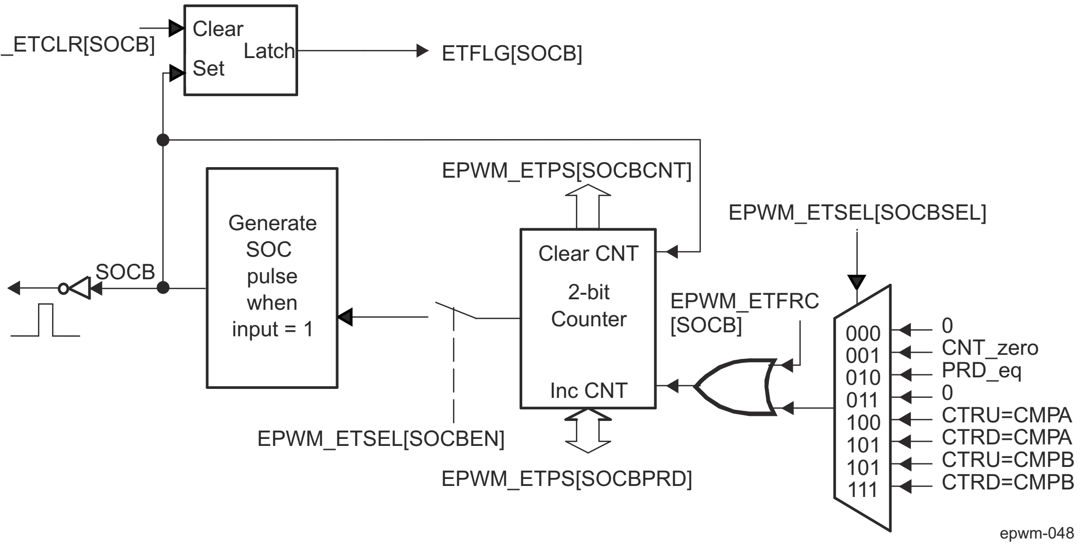

Figure 12-370. EPWM Event-Trigger SOCB Pulse Generator

12.4.3.4.9 EPWM Functional Register Groups

The Table 12-400 lists the groups of EPWM module registers according to their functionalities.

Table 12-412. EPWM Module Control and Status Registers Grouped by Submodule

Register Name	Offset	Size (×16)	Shadow	Register Description
Time-Base (TB) Submodule Registers				
EPWM_TBCTL	0h	1	No	Time-Base Control Register
EPWM_TBSTS	2h	1	No	Time-Base Status Register
EPWM_TBPHS	6h	1	No	Time-Base Phase Register
EPWM_TBCNT	8h	1	No	Time-Base Counter Register
EPWM_TBPRD	Ah	1	Yes	Time-Base Period Register
Counter-Compare (CC) Submodule Registers				
EPWM_CMPCTL	Eh	1	No	Counter-Compare Control Register
EPWM_CMPA	12h	1	Yes	Counter-Compare A Register
EPWM_CMPB	14h	1	Yes	Counter-Compare B Register
Action-Qualifier (AQ) Submodule Registers				
EPWM_AQCTLA	16h	1	No	Action-Qualifier Control Register for Output A (EPWMxA)
EPWM_AQCTLB	18h	1	No	Action-Qualifier Control Register for Output B (EPWMxB)
EPWM_AQSFRC	1Ah	1	No	Action-Qualifier Software Force Register
EPWM_AQCSFRC	1Ch	1	Yes	Action-Qualifier Continuous S/W Force Register Set
Dead-Band (DB) Generator Submodule Registers				
EPWM_DBCTL	1Eh	1	No	Dead-Band Generator Control Register
EPWM_DBRED	20h	1	No	Dead-Band Generator Rising Edge Delay Count Register
EPWM_DBFED	22h	1	No	Dead-Band Generator Falling Edge Delay Count Register
Trip-Zone (TZ) Submodule Registers				
EPWM_TZSEL	24h	1	No	Trip-Zone Select Register(1)
EPWM_TZCTL	28h	1	No	Trip-Zone Control Register (1)
EPWM_TZEINT	2Ah	1	No	Trip-Zone Enable Interrupt Register (1)

Table 12-412. EPWM Module Control and Status Registers Grouped by Submodule (continued)

Register Name	Offset	Size (×16)	Shadow	Register Description
EPWM_TZFLG	2Ch	1	No	Trip-Zone Flag Register (1)
EPWM_TZCLR	2Eh	1	No	Trip-Zone Clear Register (1)
EPWM_TZFRC	30h	1	No	Trip-Zone Force Register (1)
Event-Trigger (ET) Submodule Registers				
EPWM_ETSEL	32h	1	No	Event-Trigger Selection Register
EPWM_ETPS	34h	1	No	Event-Trigger Pre-Scale Register
EPWM_ETFLG	36h	1	No	Event-Trigger Flag Register
EPWM_ETCLR	38h	1	No	Event-Trigger Clear Register
EPWM_ETFRC	3Ah	1	No	Event-Trigger Force Register
PWM-Chopper Submodule Registers				
EPWM_PCCTL	3Ch	1	No	PWM-Chopper Control Register

(1) EALLOW protected registers.

12.4.3.4.10 Proper EPWM Interrupt Initialization Procedure

When the EPWM peripheral clock is enabled it is possible that interrupt flags may be set due to spurious events as the EPWM registers not being properly initialized. The proper procedure for initializing the EPWM peripheral is:

1. Disable global interrupts (CPU INTM flag)
2. Disable EPWM interrupts
3. Initialize peripheral registers
4. Clear any spurious EPWM flags
5. Enable EPWM interrupts
6. Enable global interrupts

12.4.4 Enhanced Quadrature Encoder Pulse (EQEP) Module

This section describes the Enhanced Quadrature Encoder Pulse (EQEP) module in the device.

12.4.4.1 EQEP Overview

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns, as shown in Figure 12-371. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

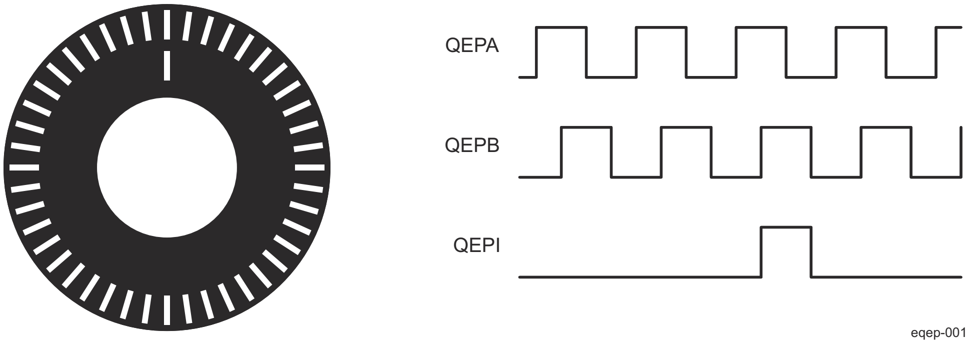

Figure 12-371. Optical Encoder Disk

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vise versa as shown in Figure 12-372.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 kHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

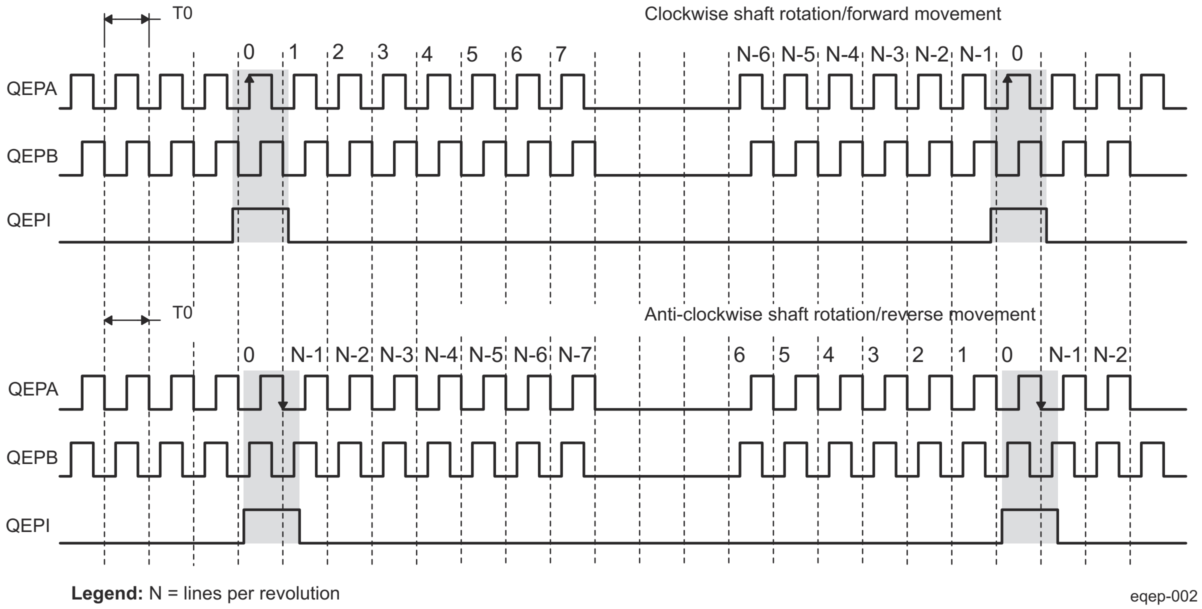

Figure 12-372. QEP Encoder Output Signal for Forward/Reverse Movement

Quadrature encoders from different manufacturers come with two forms of index pulse (gated index pulse or ungated index pulse) as shown in Figure 12-373. A nonstandard form of index pulse is ungated. In the ungated configuration, the index edges are not necessarily coincident with A and B signals. The gated index pulse is aligned to any of the four quadrature edges and width of the index pulse and can be equal to a quarter, half, or full period of the quadrature signal.

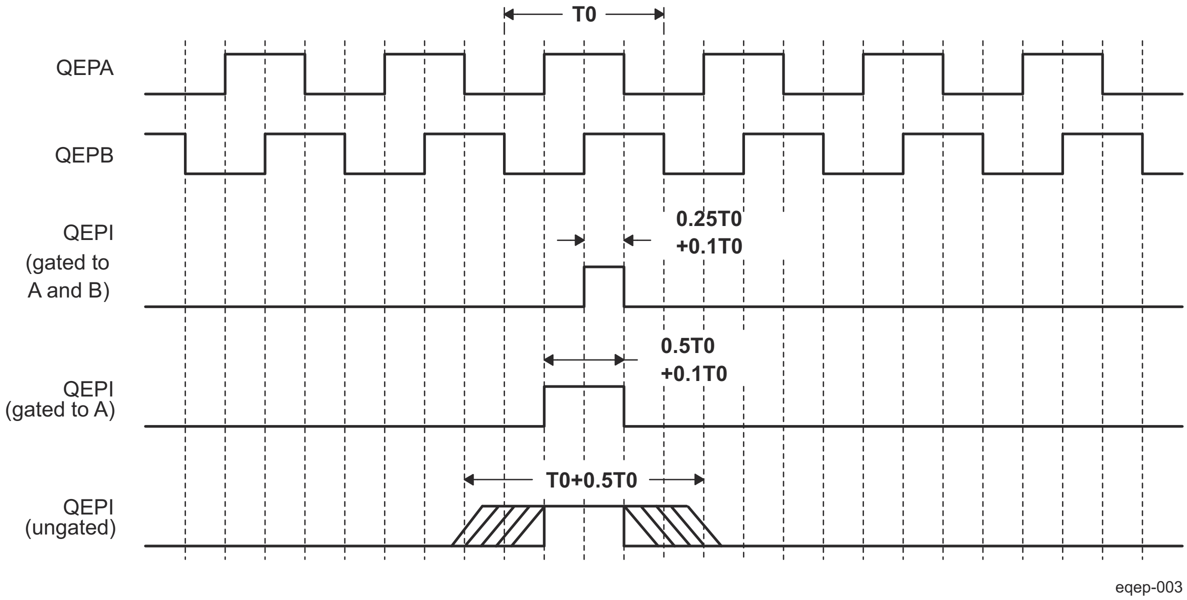

Figure 12-373. Index Pulse Example

Some typical applications for rotary encoders range from fax machines to motor controllers, and even robot localization. Rotary sensors are fundamental to the robotics and motion control systems found today. The optical shaft encoder can be used to improve a robot in various ways. The encoder can measure rotational distance traveled and speed, which can be used to monitor, for example, the angular position of a robot gripper arm or the speed of a robot.

General Issues: Estimating velocity from a digital position sensor is a cost-effective strategy in motor control. Two different first order approximations for velocity may be written as:

$$V(k) \approx \frac{x(k) - x(k\text{-}1)}{T} = \frac{\Delta X}{T} \tag{6}$$

eqep-004

$$V(k) \approx \frac{X}{t(k) - t(k\text{-}1)} = \frac{X}{\Delta T} \tag{7}$$

eqep-005

where

v(k): Velocity at time instant k

x(k): Position at time instant k

x(k-1): Position at time instant k - 1

T: Fixed unit time or inverse of velocity calculation rate

ΔX: Incremental position movement in unit time

t(k): Time instant "k"

t(k-1): Time instant "k - 1"

X: Fixed unit position

ΔT: Incremental time elapsed for unit position movement.

Equation 6 is the conventional approach to velocity estimation and it requires a time base to provide unit time event for velocity calculation. Unit time is the inverse of the velocity calculation rate.

The encoder count (position) is read once during each unit time event. The quantity [x(k) - x(k-1)] is formed by subtracting the previous reading from the current reading. Then the velocity estimate is computed by multiplying by the known constant 1/T (where T is the constant time between unit time events and is known in advance).

Estimation based on Equation 6 has an inherent accuracy limit directly related to the resolution of the position sensor and the unit time period T. For example, consider a 500-line per revolution quadrature encoder with a velocity calculation rate of 400 Hz. When used for position the quadrature encoder gives a four-fold increase in resolution, in this case, 2000 counts per revolution. The minimum rotation that can be detected is therefore 0.0005 revolutions, which gives a velocity resolution of 12 rpm when sampled at 400 Hz. While this resolution may be satisfactory at moderate or high speeds, for example, 1% error at 1200 rpm, it would clearly prove inadequate at low speeds. In fact, at speeds below 12 rpm, the speed estimate would erroneously be zero much of the time.

At low speed, Equation 7 provides a more accurate approach. It requires a position sensor that outputs a fixed interval pulse train, such as the aforementioned quadrature encoder. The width of each pulse is defined by motor speed for a given sensor resolution. Equation 7 can be used to calculate motor speed by measuring the elapsed time between successive quadrature pulse edges. However, this method suffers from the opposite limitation of Equation 6. A combination of relatively large motor speeds and high sensor resolution makes the time interval ΔT small, and thus more greatly influenced by the timer resolution. This can introduce considerable error into high-speed estimates.

For systems with a large speed range (that is, speed estimation is needed at both low and high speeds), one approach is to use Equation 7 at low speed and have the software switch over to Equation 6 when the motor speed rises above some specified threshold.

The device has three instances of the EQEP modules.

shows the EQEP allocation across device domains.

Figure 12-374 shows the EQEP module overview.

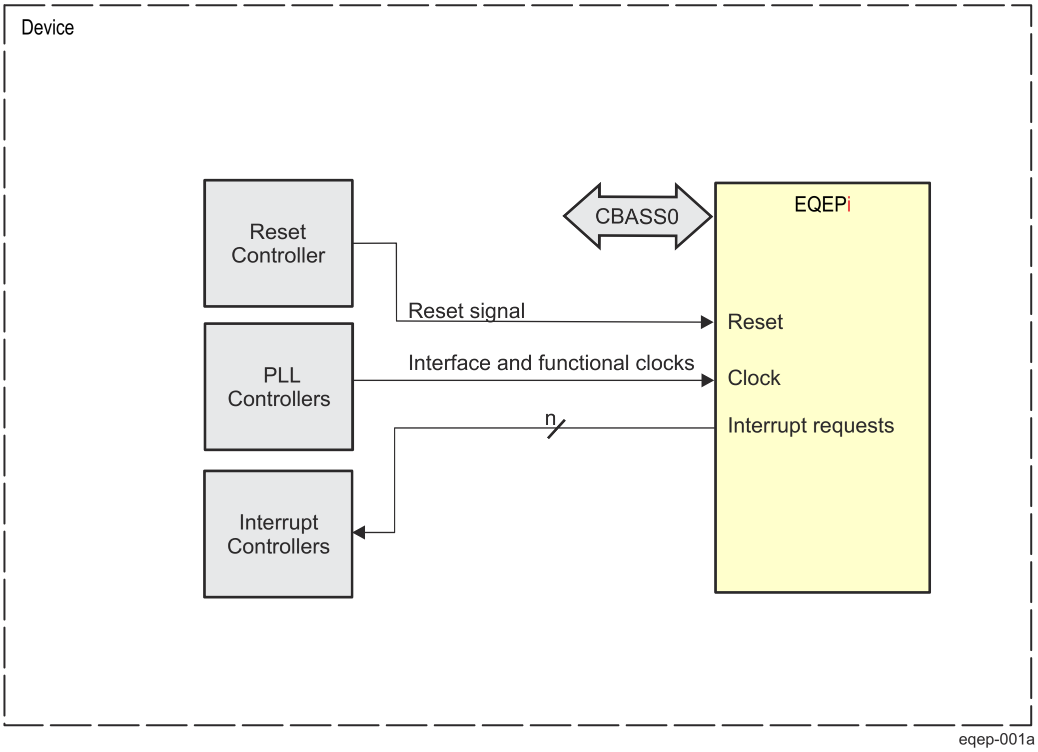

Note

i = 0 to 2

Figure 12-374. EQEP Overview

12.4.4.1.1 EQEP Features

The EQEP module includes the following features:

- Input synchronization
- Three stage/six stage digital noise filter
- Quadrature decoder unit
- Position counter and control unit for position measurement
- Quadrature edge capture unit for low-speed measurement
- Unit time base for speed and frequency measurement
- Watchdog timer for detecting stalls
- EQEP inputs (A/B/INDEX and STROBE) are available at chip level
- EQEP phase error output is also available. The status of the phase error can be observed by software through the CTRLMMR_EQEP_STAT register in the CTRL_MMR0 module.

12.4.4.1.2 EQEP Not Supported Features

The following EQEP features are not supported:

- EQEP quadrature outputs (A and B) are not pinned out

For more information about EQEP module restrictions in functionality, see *Device Specific EQEP Features*.

12.4.4.2 EQEP Environment

12.4.4.2.1 EQEP I/O Interface

The EQEPi (where i = 0 to 2) module is hereinafter referred to as EQEP module.

This section describes the EQEP external connections (environment).

Figure 12-375 shows the EQEP interface signals.

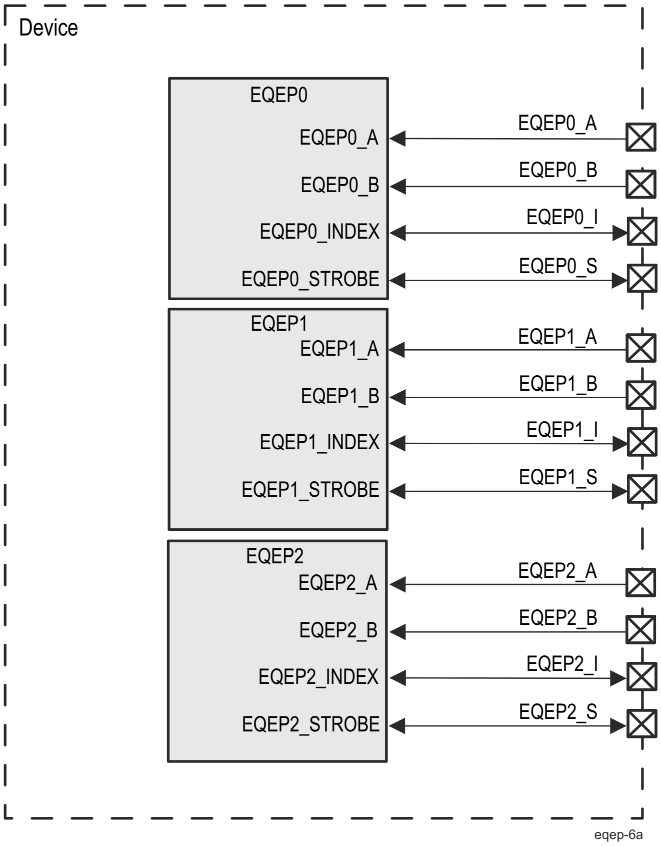

Figure 12-375. EQEP External Interface I/Os

Table 12-401 describes the EQEP I/O signals.

Table 12-413. EQEP I/O Signals

Module Pin	Device Level Signal Name	I/O Type[1]	Description	Module Pin Reset Value[2]
			EQEP0	
EQEP0_A	EQEP0_A	I	EQEP0 Quadrature input A	HiZ
EQEP0_B	EQEP0_B	I	EQEP0 Quadrature input B	HiZ
EQEP0_INDEX	EQEP0_I	I/O[3]	EQEP0 Index input/output	HiZ
EQEP0_STROBE	EQEP0_S	I/O[3]	EQEP0 Strobe input/output	HiZ
			EQEP1	
EQEP1_A	EQEP1_A	I	EQEP1 Quadrature input A	HiZ
EQEP1_B	EQEP1_B	I	EQEP1 Quadrature input B	HiZ
EQEP1_INDEX	EQEP1_I	I/O[3]	EQEP1 Index input/output	HiZ
EQEP1_STROBE	EQEP1_S	I/O[3]	EQEP1 Strobe input/output	HiZ
			EQEP2	
EQEP2_A	EQEP2_A	I	EQEP2 Quadrature input A	HiZ

Table 12-413. EQEP I/O Signals (continued)

Module Pin	Device Level Signal Name	I/O Type[1]	Description	Module Pin Reset Value[2]
EQEP2_B	EQEP2_B	I	EQEP2 Quadrature input B	HiZ
EQEP2_INDEX	EQEP2_I	I/O[3]	EQEP2 Index input/output	HiZ
EQEP2_STROBE	EQEP2_S	I/O[3]	EQEP2 Strobe input/output	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) Output functionality is not supported. Only inputs are pinned out. For more information see *Device Specific EQEP Features*.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.4.4.3 EQEP Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

There are three EQEP modules integrated in the device MAIN domain - EQEP0, EQEP1 and EQEP2.

Figure 12-376 shows the integration of EQEPi.

Note

i = 0 to 2

Figure 12-376. EQEP Integration

Table 12-402 through summarize the integration of EQEP0, EQEP1 and EQEP2 in the device MAIN domain.

Table 12-414. EQEP Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
EQEP0	PSC0	PD0	LPSC6	CBASS0
EQEP1	PSC0	PD0	LPSC6	CBASS0
EQEP2	PSC0	PD0	LPSC6	CBASS0

Table 12-415. EQEP Clocks and Resets

Clocks				
Module Instance	**Module Clock Input**	**Source Clock Signal**	**Source**	**Description**
EQEP0	EQEP0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	EQEP0 functional and interface clock
EQEP1	EQEP1_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	EQEP1 functional and interface clock
EQEP2	EQEP2_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	EQEP2 functional and interface clock
Resets				
Module Instance	**Module Reset Input**	**Source Reset Signal**	**Source**	**Description**
EQEP0	EQEP0_RST	MOD_G_RST	LPSC6	Module Reset
EQEP1	EQEP1_RST	MOD_G_RST	LPSC6	Module Reset
EQEP2	EQEP2_RST	MOD_G_RST	LPSC6	Module Reset

12.4.4.3.1 Device Specific EQEP Features

The EQEP module interface has some restrictions in functionality. The EQEP restrictions are, as follows:

- **Only EQEP inputs (A / B / INDEX and STROBE) are available to user at chip level**
- **EQEP phase error output (EQEP_ERR_PHASE_ERR) is also available**
  - The status of the phase error can be observed by software using the CTRLMMR_EQEP_STAT register in the CTRL_MMR0 module.

The EQEP functional interface signals which are NOT available to user are summarized in Table 12-404.

Table 12-416. Device Limitations for the EQEP Functional Interfaces

Module Interface	Signal	Description	Comment
EQEPi (where i = 0 to 2 for the device)	EQEP_EQEPA_O EQEP_EQEPB_O	EQEP quadrature A output EQEP quadrature B output	Not available at chip boundary (can not be used)
	EQEP_EQEPA_OEN EQEP_EQEPB_OEN	EQEP quadrature A output enable EQEP quadrature B output enable	

12.4.4.4 EQEP Functional Description

This section provides the EQEP functional description and corresponding functional details about EQEPx inputs.

Note

Multiple identical EQEP modules can be contained in a system. For actual number of EQEP modules integrated in the device, refer to *EQEP Integration*. The letter x within a signal or module name is used to indicate a generic EQEP instance on a device. For example, output interrupt request, EQEP0_EQEP_INT_0 belongs to EQEP0, EQEP1_EQEP_INT_0 belongs to EQEP1, and so forth.

The EQEP peripheral contains the following major functional units (as shown in Figure 12-377):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Three stage/six stage digital noise filter
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG).

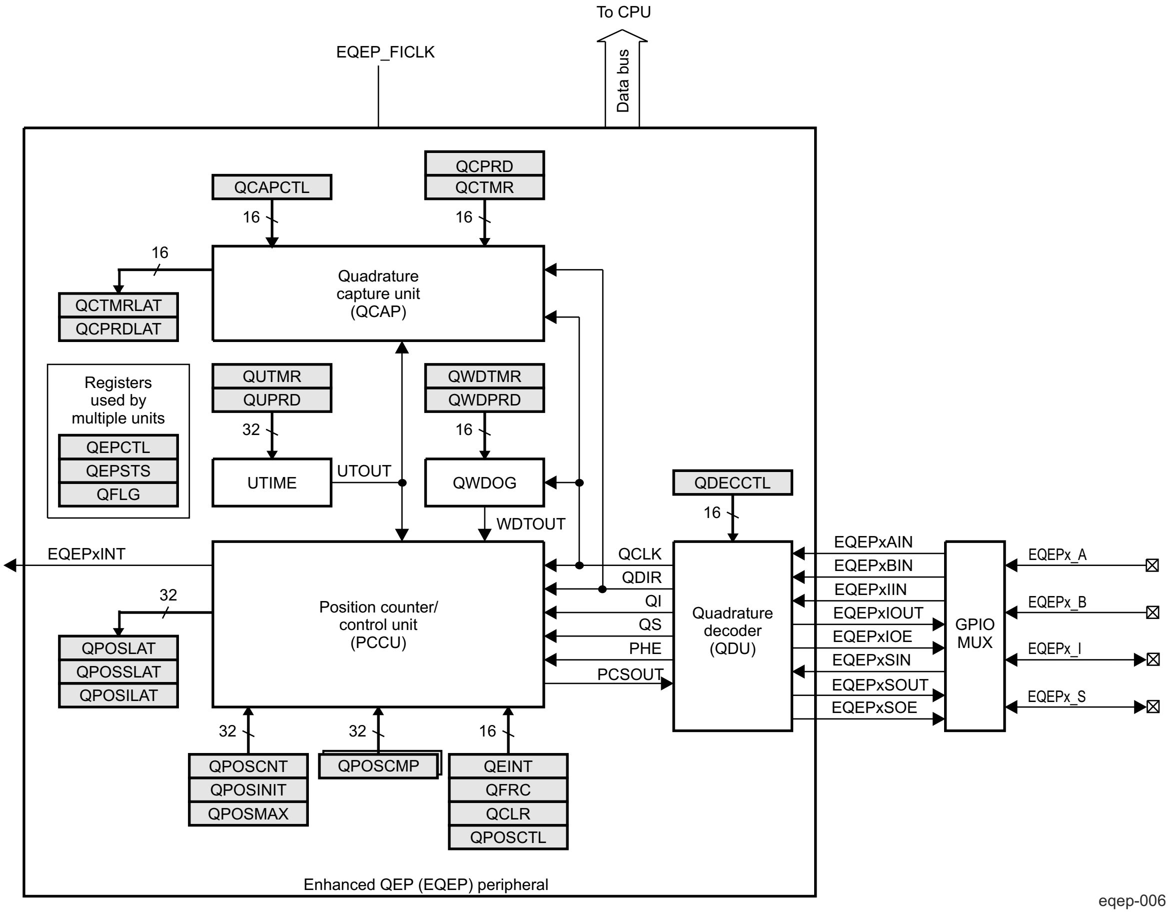

Figure 12-377. Functional Block Diagram of the EQEP Peripheral

12.4.4.4.1 EQEP Inputs

The EQEP inputs include two pins for quadrature-clock mode or direction-count mode, an index (or 0 marker), and a strobe input.

- EQEPx_A and EQEPx_B: These two pins can be used in quadrature-clock mode or direction-count mode.
  - Quadrature-clock mode: The EQEP encoders provide two square wave signals (A and B) 90 electrical degrees out of phase whose phase relationship is used to determine the direction of rotation of the input shaft and number of EQEP pulses from the index position to derive the relative position information. For forward or clockwise rotation, QEPA signal leads QEPB signal and vice versa. The quadrature decoder uses these two inputs to generate quadrature-clock and direction signals.
  - Direction-count mode: In direction-count mode, direction and clock signals are provided directly from the external source. Some position encoders have this type of output instead of quadrature output. The EQEPx_A pin provides the clock input and the EQEPx_B pin provides the direction input.
- EQEPx_I: Index or Zero Marker: The EQEP encoder uses an index signal to assign an absolute start position from which position information is incrementally encoded using quadrature pulses. This pin is connected to the index output of the EQEP encoder to optionally reset the position counter for each revolution. This signal can be used to initialize or latch the position counter on the occurrence of a desired event on the index pin.
- EQEPx_S: Strobe Input: This general-purpose strobe signal can initialize or latch the position counter on the occurrence of a desired event on the strobe pin. This signal is typically connected to a sensor or limit switch to notify that the motor has reached a defined position.

12.4.4.4.2 EQEP Quadrature Decoder Unit (QDU)

Figure 12-378 shows a functional block diagram of the QDU.

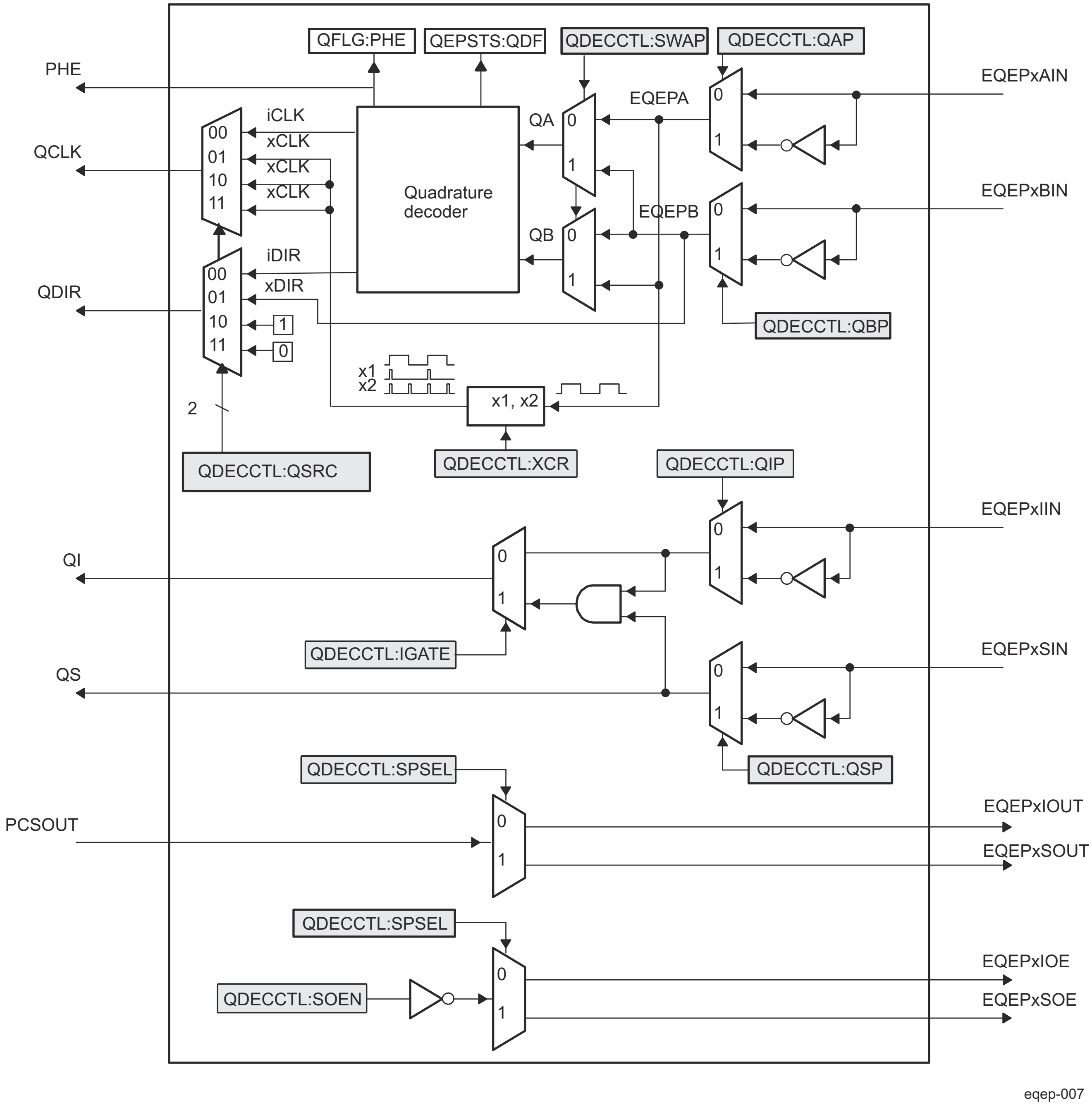

Figure 12-378. Functional Block Diagram of Decoder Unit

12.4.4.4.2.1 EQEP Position Counter Input Modes

Clock and direction input to position counter is selected using the QSRC bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL), based on interface input requirement as follows:

- Quadrature-count mode
- Direction-count mode
- UP-count mode
- DOWN-count mode.

12.4.4.4.2.1.1 Quadrature Count Mode

The quadrature decoder generates the direction and clock to the position counter in quadrature count mode.

Direction Decoding The direction decoding logic of the EQEP circuit determines which one of the sequences (EQEPA, EQEPB) is the leading sequence and accordingly updates the direction information in the QDF bit in the EQEP status register (EQEP_QEP_STS_CT). Table 12-405 and Figure 12-379 show the direction decoding logic in truth table and state machine form. Both edges of the EQEPA and EQEPB signals are sensed to generate count pulses for the position counter. Therefore, the frequency of the clock generated by the EQEP logic is four times that of each input sequence. Figure 12-380 shows the direction decoding and clock generation from the EQEP input signals.

Phase Error Flag In normal operating conditions, quadrature inputs EQEPA and EQEPB will be 90 degrees out of phase. The phase error flag (QPEI_FLG) is set in the EQEP_QINT_EN_FLG register when edge transition is detected simultaneously on the EQEPA and EQEPB signals to optionally generate interrupts. State transitions marked by dashed lines in Figure 12-379 are invalid transitions that generate a phase error.

Count Multiplication The EQEP position counter provides 4× times the resolution of an input clock by generating a quadrature-clock (QCLK) on the rising/falling edges of both EQEP input clocks (EQEPA and EQEPB) as shown in Figure 12-380.

Reverse Count In normal quadrature count operation, EQEPA input is fed to the QA input of the quadrature decoder and the EQEPB input is fed to the QB input of the quadrature decoder. Reverse counting is enabled by setting the SWAP bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL). This will swap the input to the quadrature decoder thereby reversing the counting direction.

Table 12-417. Quadrature Decoder Truth Table

Previous Edge	Present Edge	QDIR	QPOSCNT
QA↑	QB↑	UP	Increment (+1)
	QB↓	DOWN	Decrement (-1)
	QA↓	TOGGLE	Increment (+1) or Decrement (-1)
QA↓	QB↓	UP	Increment (+1)
	QB↑	DOWN	Decrement (-1)
	QA↑	TOGGLE	Increment (+1) or Decrement (-1)
QB↑	QA↑	DOWN	Decrement (-1)
	QA↓	UP	Increment (+1)
	QB↓	TOGGLE	Increment (+1) or Decrement (-1)
QB↓	QA↓	DOWN	Decrement (-1)
	QA↑	UP	Increment (+1)
	QB↑	TOGGLE	Increment (+1) or Decrement (-1)

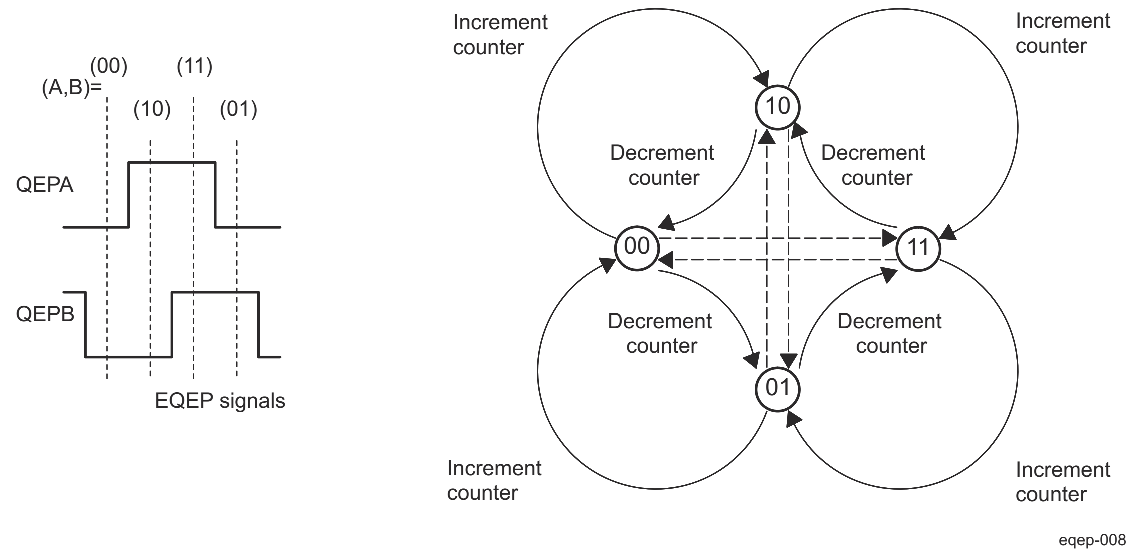

Figure 12-379. Quadrature Decoder State Machine

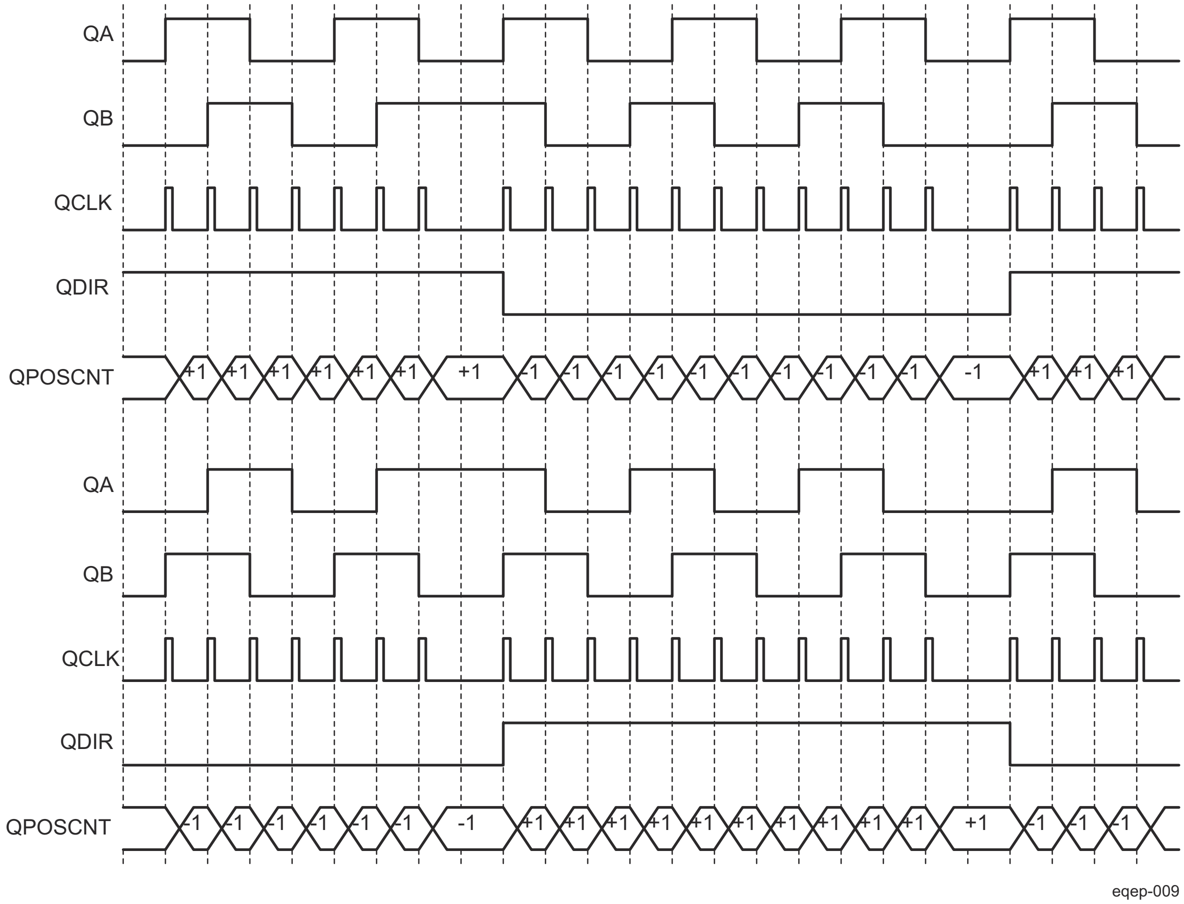

Figure 12-380. Quadrature-clock and Direction Decoding

12.4.4.4.2.1.2 EQEP Direction-count Mode

Some position encoders provide direction and clock outputs, instead of quadrature outputs. In such cases, direction-count mode can be used. EQEPA input will provide the clock for position counter and the EQEPB input will have the direction information. The position counter is incremented on every rising edge of a EQEPA input when the direction input is high and decremented when the direction input is low.

12.4.4.4.2.1.3 EQEP Up-Count Mode

The counter direction signal is hard-wired for up count and the position counter is used to measure the frequency of the EQEPA input. Setting of the XCR bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL) enables clock generation to the position counter on both edges of the QEPA input, thereby increasing the measurement resolution by 2× factor.

12.4.4.4.2.1.4 EQEP Down-Count Mode

The counter direction signal is hardwired for a down count and the position counter is used to measure the frequency of the EQEPA input. Setting of the XCR bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL) enables clock generation to the position counter on both edges of a EQEPA input, thereby increasing the measurement resolution by 2× factor.

12.4.4.4.2.2 EQEP Input Polarity Selection

Each EQEP input can be inverted using the in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL[8-5]) control bits. As an example, setting of the QIP bit in EQEP_QDEC_QEP_CTL inverts the index input.

12.4.4.4.2.3 EQEP Position-Compare Sync Output

The EQEP peripheral includes a position-compare unit that is used to generate the position-compare sync signal on compare match between the position counter register (EQEP_QPOSCNT) and the position-compare register (EQEP_QPOSCMP). This sync signal can be output using an index pin or strobe pin of the EQEP peripheral.

Setting the SOEN bit in the EQEP decoder and control register (EQEP_QDEC_QEP_CTL) enables the position-compare sync output and the SPSEL bit in EQEP_QDEC_QEP_CTL selects either an EQEP index pin or an EQEP strobe pin.

12.4.4.4.3 EQEP Position Counter and Control Unit (PCCU)

The position counter and control unit provides two configuration registers (EQEP_QDEC_QEP_CTL and EQEP_QCAP_QPOS_CTL) for setting up position counter operational modes, position counter initialization/latch modes and position-compare logic for sync signal generation.

12.4.4.4.3.1 EQEP Position Counter Operating Modes

Position counter data may be captured in different manners. In some systems, the position counter is accumulated continuously for multiple revolutions and the position counter value provides the position information with respect to the known reference. An example of this is the quadrature encoder mounted on the motor controlling the print head in the printer. Here the position counter is reset by moving the print head to the home position and then position counter provides absolute position information with respect to home position.

In other systems, the position counter is reset on every revolution using index pulse and position counter provides rotor angle with respect to index pulse position.

Position counter can be configured to operate in following four modes

- Position Counter Reset on Index Event
- Position Counter Reset on Maximum Position
- Position Counter Reset on the first Index Event
- Position Counter Reset on Unit Time Out Event (Frequency Measurement).

In all the above operating modes, position counter is reset to 0 on overflow and to QPOSMAX bifield value in EQEP_QPOSMAX register on underflow. Overflow occurs when the position counter counts up after QPOSMAX value. Underflow occurs when position counter counts down after "0". Interrupt flag is set to indicate overflow/ underflow in EQEP_QINT_EN_FLG register.

12.4.4.4.3.1.1 EQEP Position Counter Reset on Index Event (EQEP_QDEC_QEP_CTL[29-28] PCRM] = 0b00)

If the index event occurs during the forward movement, then position counter is reset to 0 on the next EQEP clock. If the index event occurs during the reverse movement, then the position counter is reset to the value in the EQEP_QPOSMAX register on the next EQEP clock.

First index marker is defined as the quadrature edge following the first index edge. The EQEP peripheral records the occurrence of the first index marker (EQEP_QEP_STS_CT[1] FIMF) and direction on the first index event marker (EQEP_QEP_STS_CT[6] FIDF) in EQEP_QEP_STS_CT registers, it also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for index event reset operation.

For example, if the first reset operation occurs on the falling edge of EQEPB during the forward direction, then all the subsequent reset must be aligned with the falling edge of EQEPB for the forward rotation and on the rising edge of EQEPB for the reverse rotation as shown in Figure 12-381.

The position-counter value is latched to the EQEP_QPOSILAT register and direction information is recorded in the EQEP_QEP_STS_CT[4] QDLF bit on every index event marker. The position-counter error flag (EQEP_QEP_STS_CT[0] PCEF) and error interrupt flag (EQEP_QINT_EN_FLG[17] PCEI_FLG) are set if the latched value is not equal to 0 or QPOSMAX. The position-counter error flag (EQEP_QEP_STS_CT[0] PCEF) is updated on every index event marker and an interrupt flag (EQEP_QINT_EN_FLG[17] PCEI_FLG) will be set on error that can be cleared only through software.

The index event latch configuration EQEP_QDEC_QEP_CTL[21-20] IEL bits are ignored in this mode and position counter error flag/interrupt flag are generated only in index event reset mode.

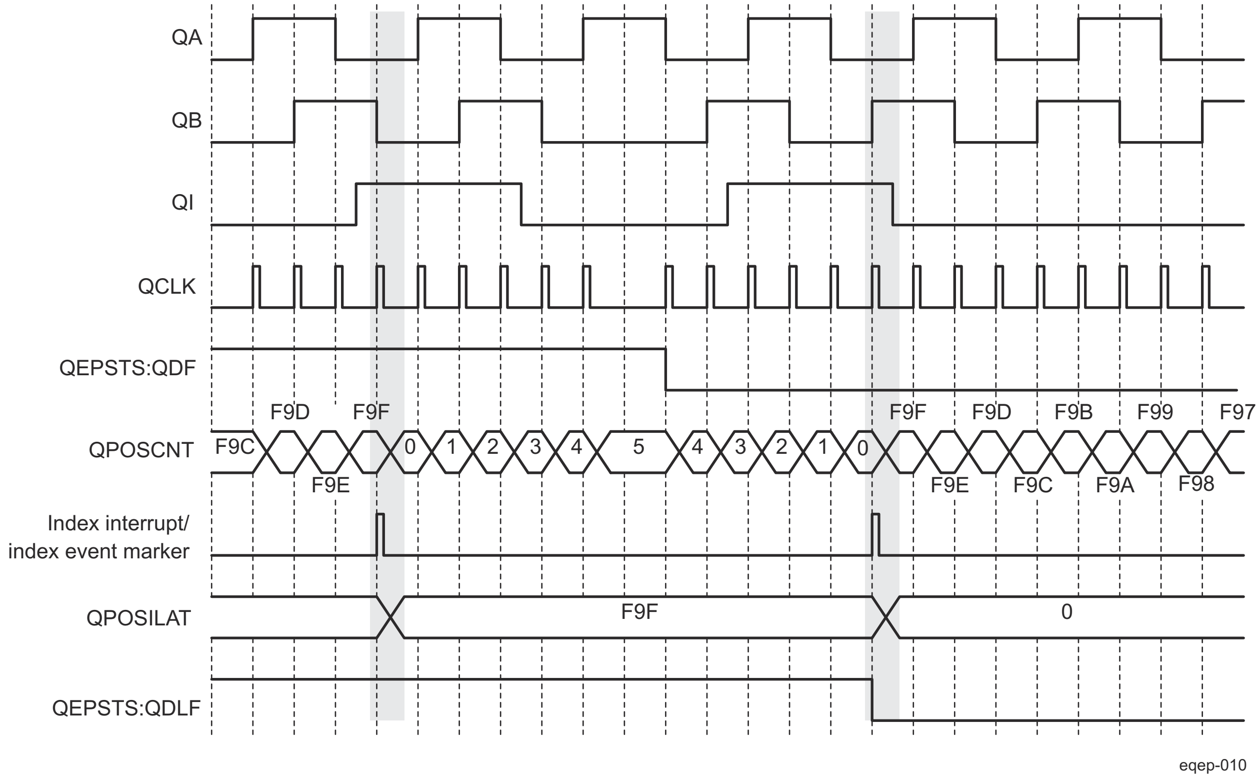

Figure 12-381. Position Counter Reset by Index Pulse for 1000 Line Encoder (QPOSMAX = 3999 or F9Fh)

12.4.4.4.3.1.2 EQEP Position Counter Reset on Maximum Position (EQEP_QDEC_QEP_CTL[29-28] PCRM=0b01)

If the position counter is equal to QPOSMAX (in EQEP_QPOSMAX register), then the position counter is reset to 0 on the next EQEP clock for forward movement and position counter overflow flag is set. If the position counter is equal to 0, then the position counter is reset to QPOSMAX on the next QEP clock for reverse movement and position counter underflow flag is set. Figure 12-382 shows the position counter reset operation in this mode.

First index marker is defined as the quadrature edge following the first index edge. The EQEP peripheral records the occurrence of the first index marker (EQEP_QEP_STS_CT[1] FIMF) and direction on the first index event marker (EQEP_QEP_STS_CT[6] FIDF); it also remembers the quadrature edge on the first index marker so that the same relative quadrature transition is used for the software index marker (EQEP_QDEC_QEP_CTL[21-20] IEL= 0b11).

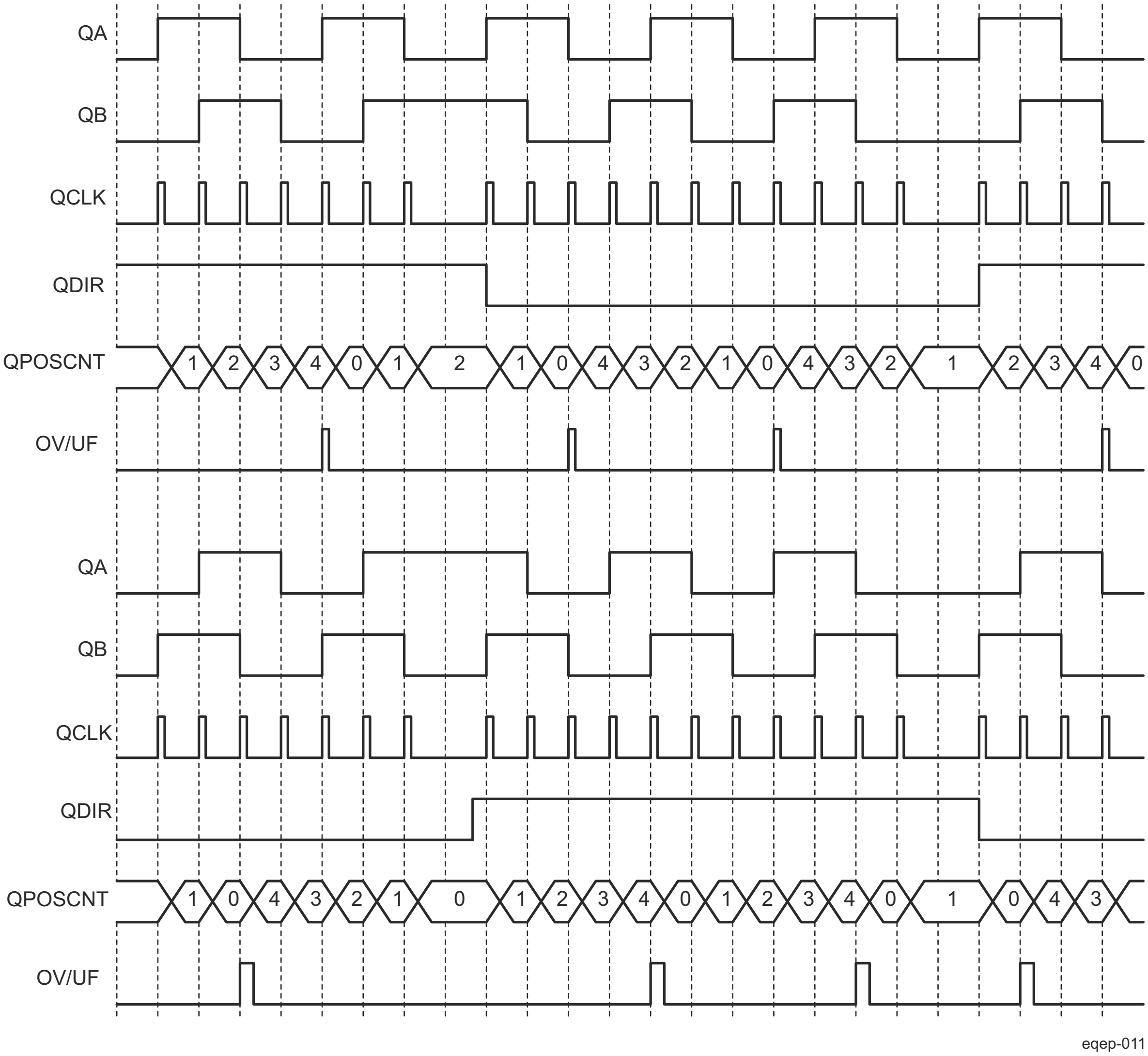

Figure 12-382. Position Counter Underflow/Overflow (QPOSMAX = 4)

12.4.4.4.3.1.3 Position Counter Reset on the First Index Event (EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b10)

If the index event occurs during forward movement, then the position counter is reset to 0 on the next EQEP clock. If the index event occurs during the reverse movement, then the position counter is reset to the value in the EQEP_QPOSMAX register on the next EQEP clock. Note that this is done only on the first occurrence and subsequently the position counter value is not reset on an index event; rather, it is reset based on maximum position as described in Section 12.4.4.4.3.1.2 .

First index marker is defined as the quadrature edge following the first index edge. The EQEP peripheral records the occurrence of the first index marker (EQEP_QEP_STS_CT[1] FIMF) and direction on the first index event marker (EQEP_QEP_STS_CT[6] FIDF) in EQEP_QEP_STS_CT registers. It also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for software index marker (EQEP_QDEC_QEP_CTL[21-20] IEL= 0b11).

12.4.4.4.3.1.4 Position Counter Reset on Unit Time out Event (EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b11)

In this mode, the QPOSCNT value is latched to the EQEP_QPOSLAT register and then the QPOSCNT field is reset (to 0 or the QPOSMAX value in the EQEP_QPOSMAX register, depending on the direction mode selected by EQEP_QDEC_QEP_CTL[15-14] QSRC bits on a unit time event). This is useful for frequency measurement.

12.4.4.4.3.2 EQEP Position Counter Latch

The EQEP index and strobe input can be configured to latch the position counter QPOSCNT (EQEP_QPOSCNT) into QPOSILAT (EQEP_QPOSILAT register) and QPOSSLAT (EQEP_QPOSSLAT register) bitfields, respectively, on occurrence of a definite event on these pins.

12.4.4.4.3.2.1 Index Event Latch

In some applications, it may not be desirable to reset the position counter on every index event and instead it may be required to operate the position counter in full 32-bit mode (EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b01 and EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b10 modes).

In such cases, the EQEP position counter can be configured to latch on the following events and direction information is recorded in the EQEP_QEP_STS_CT[4] QDLF bit on every index event marker.

- Latch on Rising edge (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b01)
- Latch on Falling edge (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b10)
- Latch on Index Event Marker (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b11)

This is particularly useful as an error checking mechanism to check if the position counter accumulated the correct number of counts between index events. As an example, the 1000-line encoder must count 4000 times when moving in the same direction between the index events.

The index event latch interrupt flag (EQEP_QINT_EN_FLG[26] IELI_FLG) is set when the position counter is latched to the EQEP_QPOSILAT register. The index event latch configuration bits are ignored when EQEP_QDEC_QEP_CTL[29-28] PCRM = 0b00.

When Position counter reset on an index event mode is selected through EQEP_QDEC_QEP_CTL[29-28] PCRM bit field (value: 0h), EQEP_QDEC_QEP_CTL[21-20] IEL bit field must be configured to 0h and position counter value is latched into the EQEP_QPOSILAT[31-0] QPOSILAT register for every index marker.

Latch on Rising Edge (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b01)	The position counter value (QPOSCNT) is latched to the EQEP_QPOSILAT register on every rising edge of an index input.
Latch on Falling Edge (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b10)	The position counter value (QPOSCNT) is latched to the EQEP_QPOSILAT register on every falling edge of index input.
Latch on Index Event Marker/Software Index Marker (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b11)	The first index marker is defined as the quadrature edge following the first index edge. The EQEP peripheral records the occurrence of the first index marker (EQEP_QEP_STS_CT[1] FIMF) and

direction on the first index event marker (EQEP_QEP_STS_CT[6] FIDF) in the EQEP_QEP_STS_CT registers. It also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for latching the position counter (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b11).

Figure 12-383 shows the position counter latch using an index event marker.

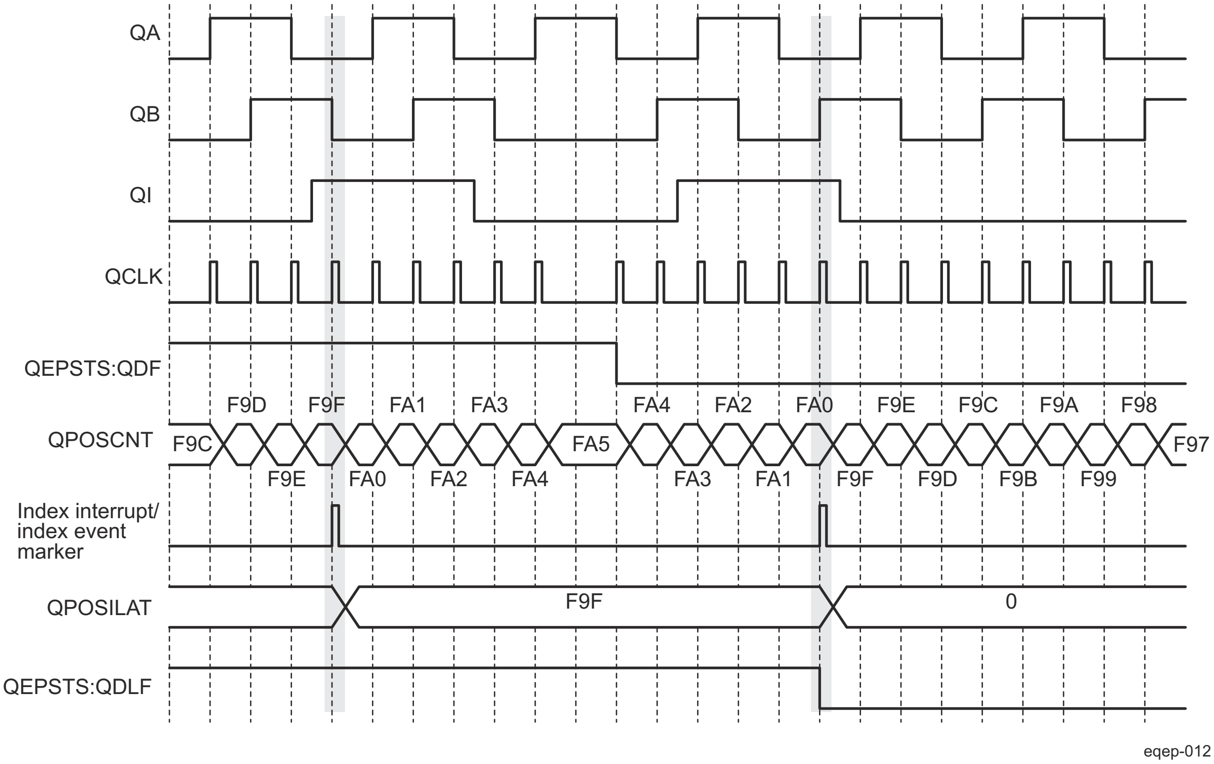

Figure 12-383. Software Index Marker for 1000-line Encoder (EQEP_QDEC_QEP_CTL[21-20] IEL = 0b01)

12.4.4.4.3.2.2 EQEP Strobe Event Latch

The position-counter value is latched to the EQEP_QPOSSLAT register on the rising edge of the strobe input (QCLK) by clearing the EQEP_QDEC_QEP_CTL[22] SEL bit. Latching on the falling edge of the strobe input (QCLK) can be done by inverting the strobe input using the EQEP_QDEC_QEP_CTL[5] QSP bit.

If the EQEP_QDEC_QEP_CTL[22] SEL bit is set, then the position counter value is latched to the EQEP_QPOSSLAT register on the rising edge of the strobe input for forward direction and on the falling edge of the strobe input for reverse direction as shown in Figure 12-384.

The strobe event latch interrupt flag (EQEP_QINT_EN_FLG[25] SELI_FLG) is set when the position counter is latched to the EQEP_QPOSSLAT register.

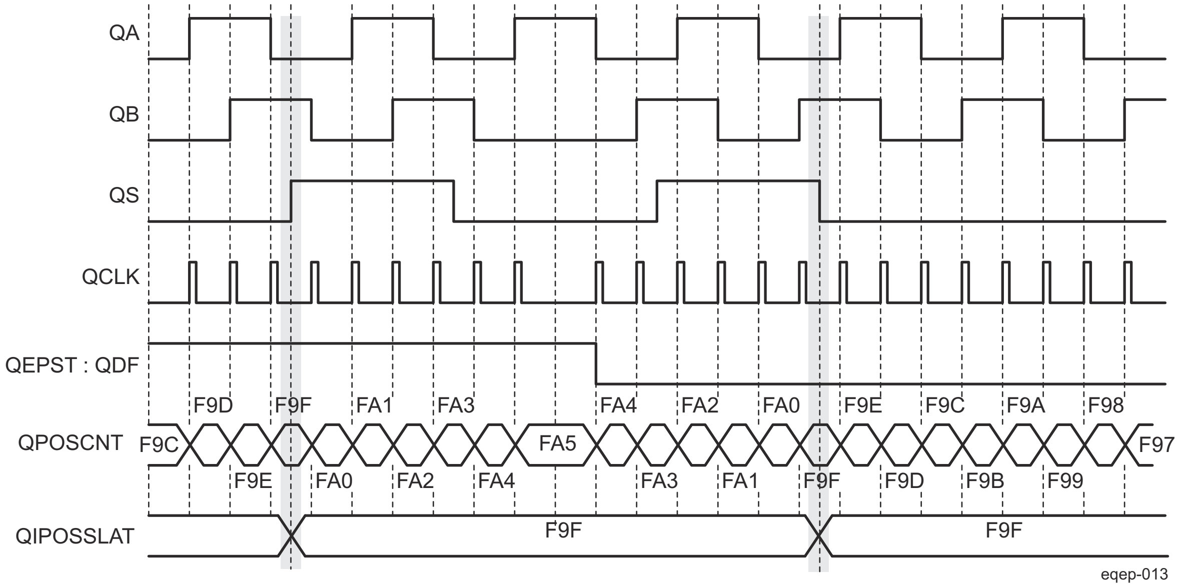

Figure 12-384. EQEP Strobe Event Latch (EQEP_QDEC_QEP_CTL[22] SEL = 0b1)

12.4.4.4.3.3 EQEP Position Counter Initialization

The position counter can be initialized using following events:

- Index event
- Strobe event
- Software initialization.

Note

When all of the above events occur simultaneously, the sequence of priority is as follows: 1) Software Initialization, 2) strobe event initialization, 3) Index Event Initialization.

Index Event Initialization (IEI)

The EQEPx_I index input can be used to trigger the initialization of the position counter at the rising or falling edge of the index input.

If the EQEP_QDEC_QEP_CTL[25-24] IEI bits are 2h, then the position counter (EQEP_QPOSCNT) is initialized with a value in the EQEP_QPOSINIT register on the rising edge of strobe input for forward direction and on the falling edge of strobe input for reverse direction.

The index event initialization interrupt flag (EQEP_QDEC_QEP_CTL[25-24] IEI) is set when the position counter is initialized with a value in the EQEP_QPOSINIT register.

If EQEP_QDEC_QEP_CTL[25-24] IEI bit field is configured with value 0h (default) or 1h, the index event initialization of position counter is disabled.

If EQEP_QDEC_QEP_CTL[25-24] IEI bit field is configured with value 3h, then the the position counter (EQEP_QPOSCNT) is initialized with a value in the EQEP_QPOSINIT register on the falling edge of strobe input signal.

Strobe Event Initialization (SEI)

If the EQEP_QDEC_QEP_CTL[27-26] SEI bits are 2h, then the position counter is initialized with a value in the EQEP_QPOSINIT register on the rising edge of strobe input.

If the EQEP_QDEC_QEP_CTL[27-26] SEI bits are 3h, then the position counter (EQEP_QPOSCNT) is initialized with a value in the EQEP_QPOSINIT register on the rising edge of strobe input for forward direction and on the falling edge of strobe input for reverse direction.

The strobe event initialization interrupt flag (EQEP_QDEC_QEP_CTL[27-26] SEI) is set when the position counter is initialized with a value in the EQEP_QPOSINIT register.

If EQEP_QDEC_QEP_CTL[27-26] SEI bit field is configured with value 0h (default) or 1h, the strobe event initialization of position counter is disabled.

Software Initialization (SWI)

The position counter can be initialized in software by writing a 1h to the EQEP_QDEC_QEP_CTL[23] SWI bit, which will automatically be cleared after initialization.

12.4.4.4.3.4 EQEP Position-Compare Unit

The EQEP peripheral includes a position-compare unit that is used to generate a sync output and/or interrupt on a position-compare match. Figure 12-385 shows a diagram. The position-compare (EQEP_QPOSCMP) register is shadowed and shadow mode can be enabled or disabled using the EQEP_QCAP_QPOS_CTL[31] PCSHDW bit. If the shadow mode is not enabled, the CPU writes directly to the active position compare register.

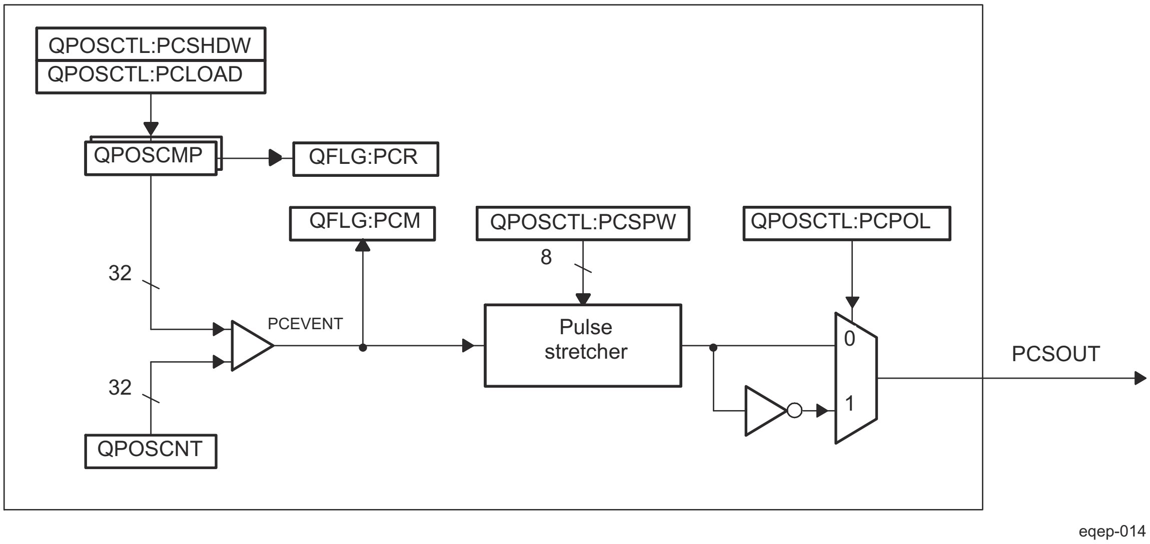

Figure 12-385. EQEP Position-compare Unit

In shadow mode, SW can configure the position-compare unit (EQEP_QCAP_QPOS_CTL[30] PCLOAD) to load the shadow register value into the active register on the following events and to generate the position-compare ready (EQEP_QINT_EN_FLG[23] PCRI_FLG) interrupt after loading.

- Load on compare match
- Load on position-counter zero event.

The position-compare match (EQEP_QINT_EN_FLG[24] PCMI_FLG) is set when the position-counter value (QPOSCNT) matches with the active position-compare register (EQEP_QPOSCMP) and the position-compare sync output of the programmable pulse width is generated on compare match to trigger an external device.

For example, if EQEP_QPOSCMP bitfield POSCMP = 0x2, the position-compare unit generates a position-compare event on the transition from 1 to 2 of the EQEP position counter for forward counting direction and on the transition from 3 to 2 of the EQEP position counter for reverse counting direction (see Figure 12-386).

Note

When EQEP_QCAP_QPOS_CTL[30] PCLOAD=0h, the shadow register is loaded into the active register as soon as POSCNT becomes zero, and it should not generate another shadow load if the POSCNT continues to stay at zero

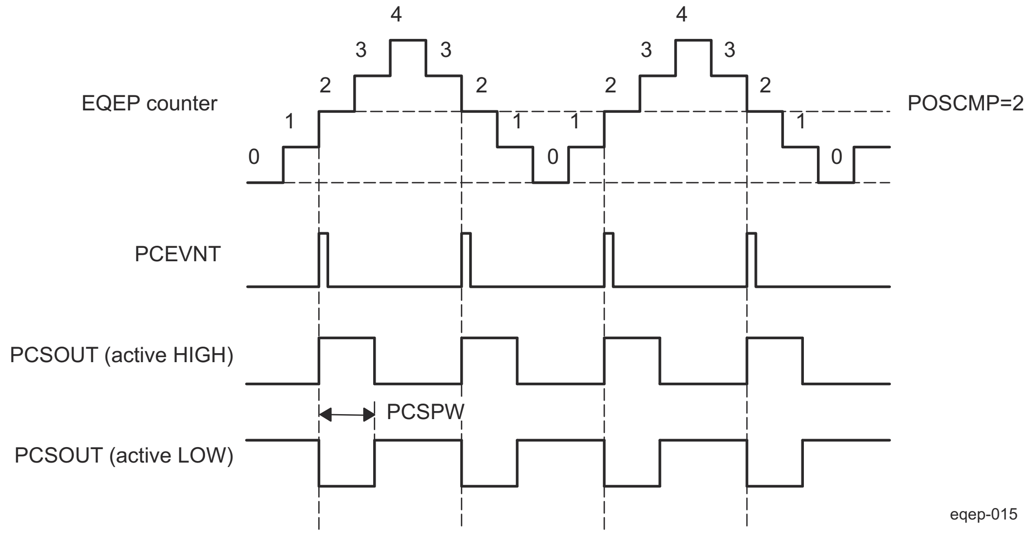

Figure 12-386. EQEP Position-compare Event Generation Points

The pulse stretcher logic in the position-compare unit generates a programmable position-compare sync pulse output on the position-compare match. In the event of a new position-compare match while a previous position-compare pulse is still active, then the pulse stretcher generates a pulse of specified duration from the new position-compare event as shown in Figure 12-387.

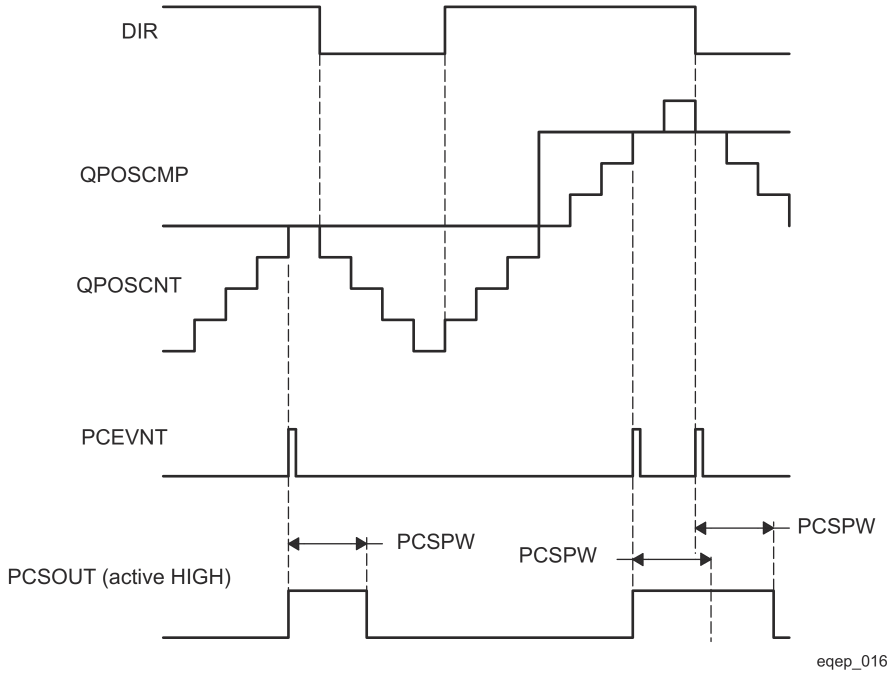

Figure 12-387. EQEP Position-compare Sync Output Pulse Stretcher

12.4.4.4.4 EQEP Edge Capture Unit

The EQEP peripheral includes an integrated edge capture unit to measure the elapsed time between the unit position events as shown in Figure 12-388. This feature is typically used for low speed measurement using the following equation:

$$V(k) = \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \quad (8)$$

eqep-017

where,

- X - Unit position is defined by integer multiple of quadrature edges (see Figure 12-389)
- ΔT - Elapsed time between unit position events
- v(k) - Velocity at time instant "k"

The EQEP capture timer (QCTMR bitfield in EQEP_QCTMR register) runs from prescaled SYSCLKOUT and the prescaler is programmed by the EQEP_QCAP_QPOS_CTL[6-4] CCPS bits. The capture timer QCTMR value is latched into the capture period register (EQEP_QC_PRD_TLAT) on every unit position event and then the capture timer is reset.

Time measurement (ΔT) between unit position events will be correct if the following conditions are met:

- No more than 65,535 counts have occurred between unit position events.
- No direction change between unit position events.

The capture unit sets the EQEP overflow error flag (EQEP_QEP_STS_CT[3] COEF) in the event of capture timer overflow between unit position events. If a direction change occurs between the unit position events, then an error flag is set in the status register (EQEP_QEP_STS_CT[2] CDEF).

Capture Timer (EQEP_QCTMR register) and Capture period register (EQEP_QC_PRD_TLAT) can be configured to latch on following events.

- CPU read of EQEP_QPOSCNT register
- Unit time-out event

If the EQEP_QDEC_QEP_CTL[18] QCLM bit is cleared, then the capture timer and capture period values are latched into the EQEP_QC_PRD_TLAT and EQEP_QCPRDLAT registers, respectively, when the CPU reads the position counter in EQEP_QPOSCNT.

Note

Capture timer and capture period values are not latched for an emulation read.

If the EQEP_QDEC_QEP_CTL[18] QCLM bit is set, then the position counter, capture timer, and capture period values are latched into the EQEP_QPOSLAT, EQEP_QC_PRD_TLAT and EQEP_QCPRDLAT registers, respectively, on unit time out.

Figure 12-390 shows the capture unit operation along with the position counter.

Note

The EQEP_QCAP_QPOS_CTL register should not be modified dynamically (such as switching CAPCLK prescaling mode from SYSCLKOUT/4 to SYSCLKOUT/8, where SYSCLKOUT is equivalent to EQEPx__FICLK). The capture unit must be disabled before changing the prescaler.

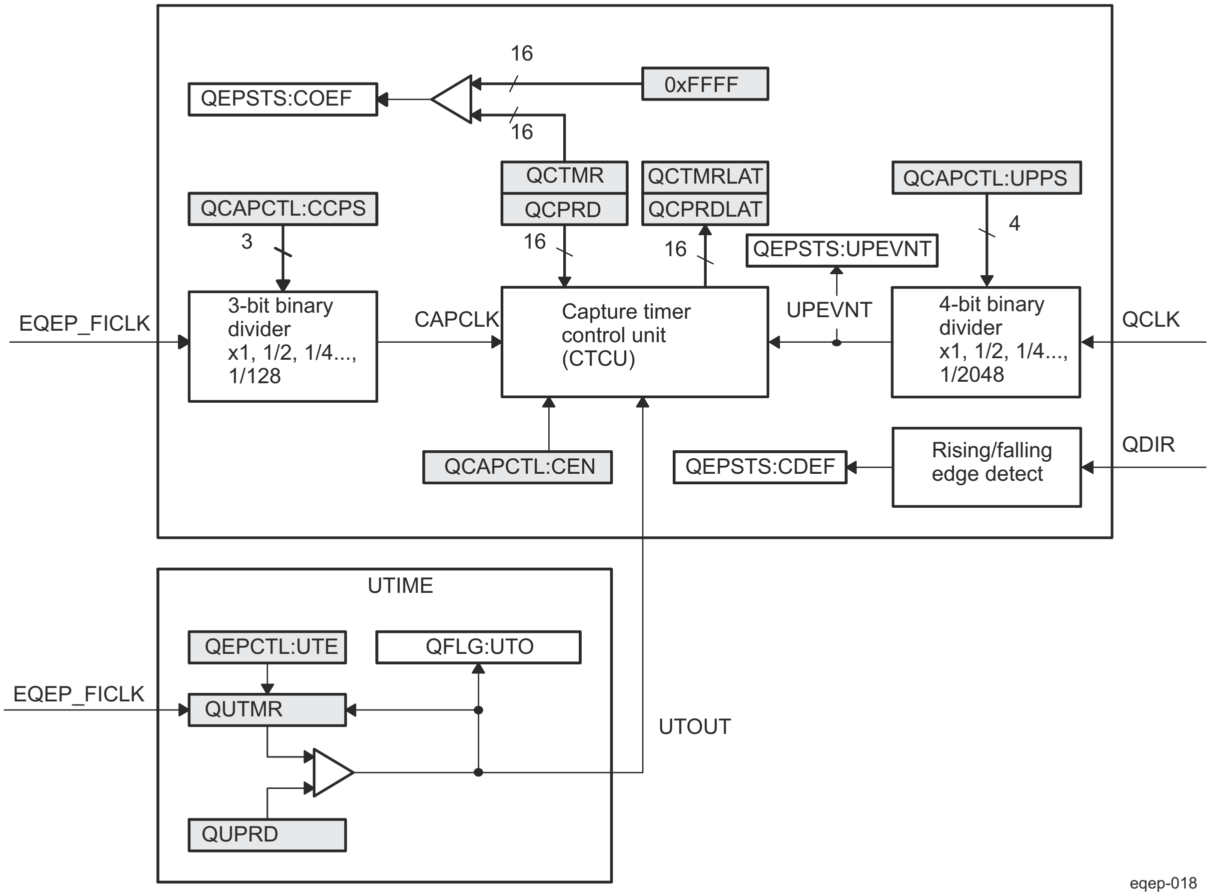

Figure 12-388. EQEP Edge Capture Unit

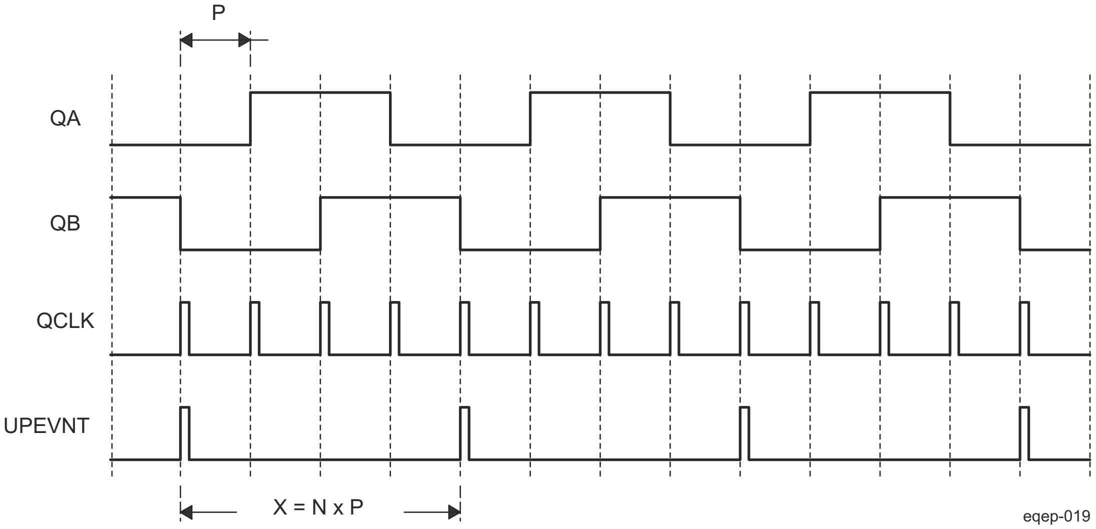

Note

N - Number of quadrature periods selected using EQEP_QCAP_QPOS_CTL[3-0] UPPS bits

Figure 12-389. Unit Position Event for Low Speed Measurement (EQEP_QCAP_QPOS_CTL[UPPS] = 0010)

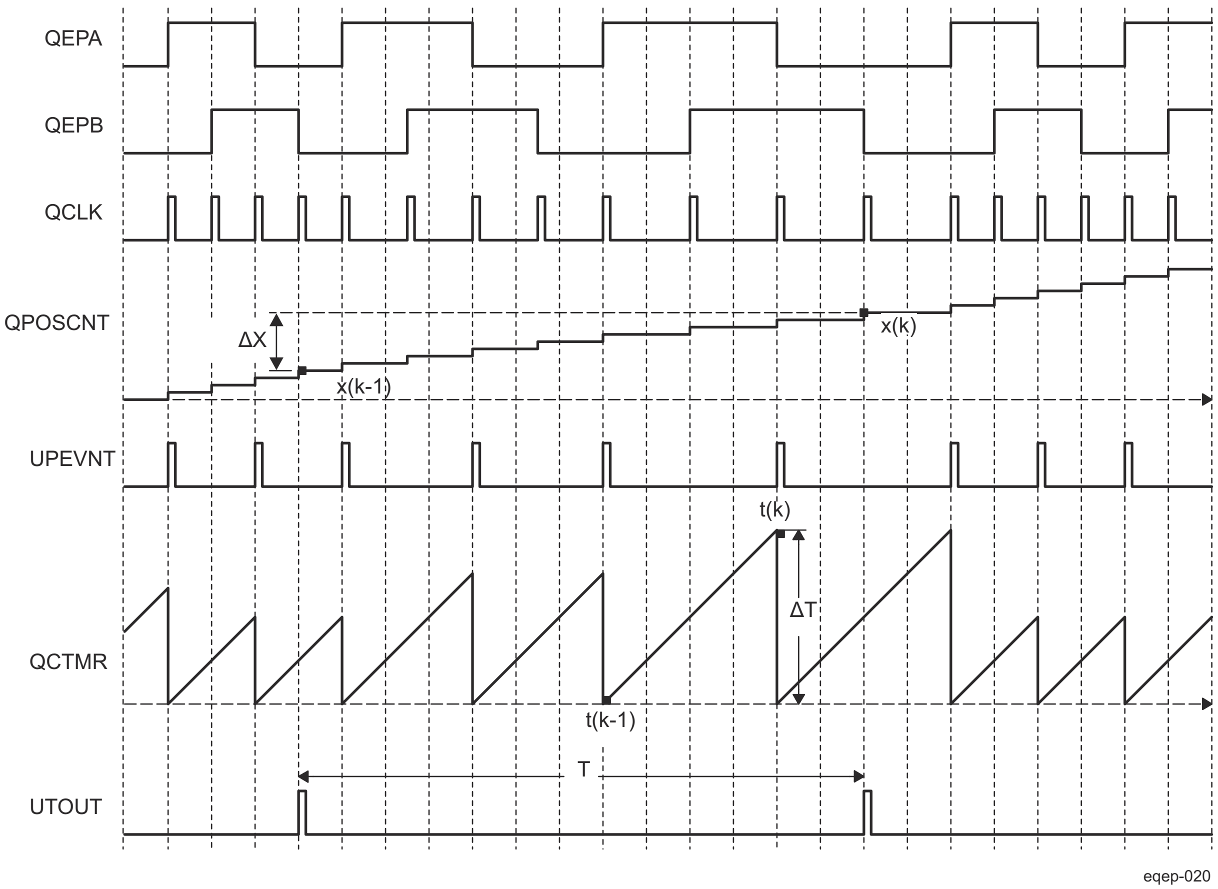

Figure 12-390. EQEP Edge Capture Unit - Timing Details

Velocity Calculation Equations:

$$V(k) = \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T} \quad \text{or}$$

$$V(k) = \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \qquad (9)$$

eqep_021

where

v(k): Velocity at time instant k

x(k): Position at time instant k

x(k-1): Position at time instant k - 1

T: Fixed unit time or inverse of velocity calculation rate

ΔX: Incremental position movement in unit time

X: Fixed unit position

ΔT: Incremental time elapsed for unit position movement

t(k): Time instant "k"

t(k-1): Time instant "k - 1"

Unit time (T) and unit period (X) are configured using the EQEP_QUPRD and EQEP_QCAP_QPOS_CTL[3-0] UPPS registers. Incremental position output and incremental time output is available in the EQEP_QPOSLAT and EQEP_QCPRDLAT registers.

Parameter	Relevant Register to Configure or Read the Information
T	Unit Period Register (EQEP_QUPRD)
ΔX	Incremental Position = QPOSLAT(k) - QPOSLAT(k - 1)
X	Fixed unit position defined by sensor resolution and QCAPCTL[3-0] UPPS bits
ΔT	Capture Period Latch (QCPRDLAT)

12.4.4.4.5 EQEP Watchdog

The EQEP peripheral contains a 16-bit watchdog timer that monitors the quadrature-clock to indicate proper operation of the motion-control system. The EQEP watchdog timer is clocked from SYSCLKOUT/64 and the quadrate clock event (pulse) resets the watchdog timer. If no quadrature-clock event is detected until a period match (QWDPRD = QWDTMR), then the watchdog timer will time out and the watchdog interrupt flag will be set (EQEP_QINT_EN_FLG[20] WTOI_FLG). The time-out value is programmable through the watchdog period bit field (EQEP_QWD_TMR_PRD[31-16] QWDPRD).

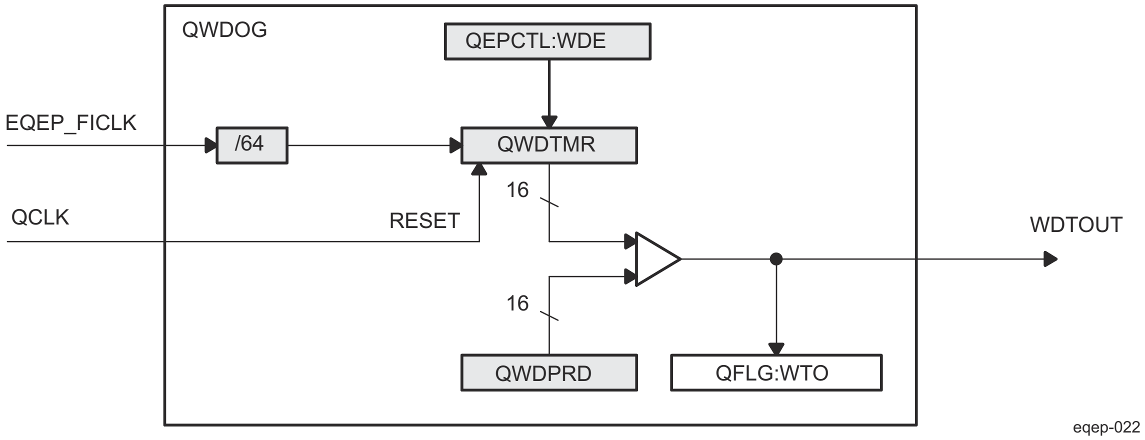

Figure 12-391. EQEP Watchdog Timer

12.4.4.4.6 Unit Timer Base

The EQEP peripheral includes a 32-bit timer (QUTMR) that is clocked by SYSCLKOUT to generate periodic interrupts for velocity calculations. The unit time out interrupt is set (EQEP_QINT_EN_FLG[27] UTOI_FLG) when the unit timer (QUTMR) matches the unit period register (EQEP_QUPRD).

The EQEP peripheral can be configured to latch the position counter, capture timer, and capture period values on a unit time out event. The latched values are used for velocity calculation as described in Section Section 12.4.4.4.4 .

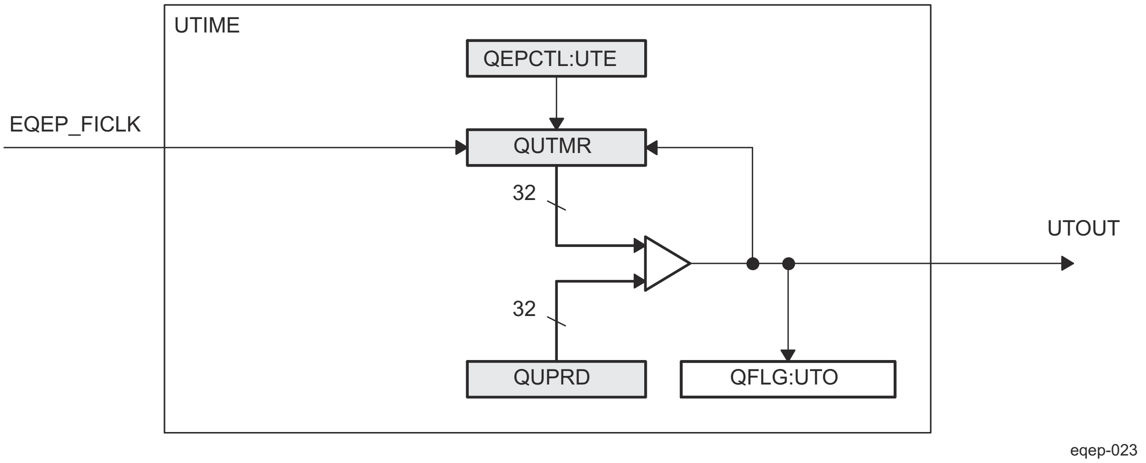

Figure 12-392. EQEP Unit Time Base

12.4.4.4.7 EQEP Interrupt Structure

Figure 12-393 shows how the interrupt mechanism works in the EQEP module.

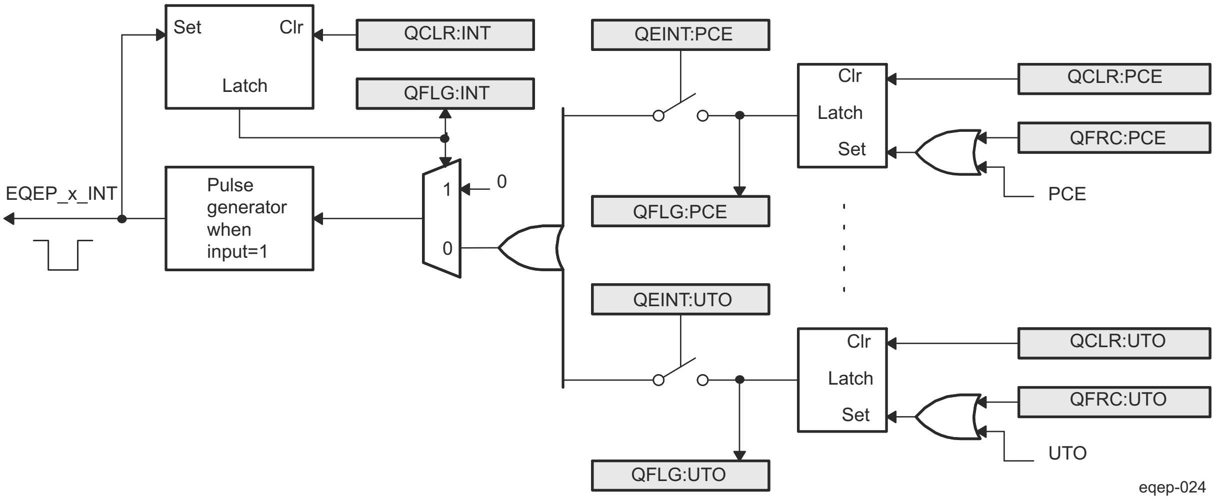

Figure 12-393. EQEP Interrupt Generation

Eleven interrupt events (PCE, PHE, QDC, WTO, PCU, PCO, PCR, PCM, SEL, IEL, and UTO) can be generated. The interrupt control register (EQEP_QINT_EN_FLG) is used to enable/disable individual interrupt event sources. The interrupt flag register (EQEP_QINT_EN_FLG) indicates if any interrupt event has been latched and contains the global interrupt flag bit (INT). An interrupt pulse is only generated to the interrupt controller if any of the interrupt events is enabled, the flag bit is 1 and the INT flag bit is 0. The interrupt service routine will need to clear the global interrupt flag bit and the serviced event, via the interrupt clear register (EQEP_QINT_CLR_FRC), before any other interrupt pulses are generated. SW can force an interrupt event by way of the interrupt force register (EQEP_QINT_CLR_FRC), which is useful for test purposes.

12.4.4.4.8 Summary of EQEP Functional Registers

Table 12-406 lists the registers with their memory locations, sizes, and reset values.

Table 12-418. EQEP Control and Status Functional Registers

Offset	Acronym	Register Description	Size (×16)/ #shadow
0h	EQEP_QPOSCNT	EQEP Position Counter Register	2/0
4h	EQEP_QPOSINIT	EQEP Position Counter Initialization Register	2/0
8h	EQEP_QPOSMAX	EQEP Maximum Position Count Register	2/0
Ch	EQEP_QPOSCMP	EQEP Position-Compare Register	2/1
10h	EQEP_QPOSILAT	EQEP Index Position Latch Register	2/0
14h	EQEP_QPOSSLAT	EQEP Strobe Position Latch Register	2/0
18h	EQEP_QPOSLAT	EQEP Position Counter Latch Register	2/0
1Ch	EQEP_QUTMR	EQEP Unit Timer Register	2/0
20h	EQEP_QUPRD	EQEP Unit Period Register	2/0
24h	EQEP_QWD_TMR_PRD	EQEP Watchdog Timer and Period Register	2/0
28h	EQEP_QDEC_QEP_CTL	EQEP Decoder and EQEP Control Register	2/0
2Ch	EQEP_QCAP_QPOS_CTL	EQEP Capture and Position Compare Control Register	2/0
30h	EQEP_QINT_EN_FLG	EQEP Interrupt Enable and Flag Register	2/0
34h	EQEP_QINT_CLR_FRC	EQEP Interrupt Clear and Forcing Register	2/0
38h	EQEP_QEP_STS_CT	EQEP Status and Capture Timer Register	2/0
3Ch	EQEP_QC_PRD_TLAT	EQEP Capture Period ant Timer Latch Register	2/0
40h	EQEP_QCPRDLAT	EQEP Capture Period Latch Register	1/0
5Ch	EQEP_PID	EQEP Revision ID Register	2/0

12.4.5 Fast Serial Interface (FSI)

This chapter contains a general description of the Fast Serial Interface (FSI) module. The FSI is a serial peripheral capable of reliable high-speed communication across isolation barriers.

12.4.5.1 FSI Overview

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable high-speed communication across isolation devices. Galvanic isolation devices are used in situations where two different electronic circuits, which do not have common power and ground connections, must exchange information. Though isolation devices facilitate these signal communications, they can also introduce a large delay on the signal lines and add skew between the signals. The FSI is designed specifically to ensure reliable high-speed communication for system scenarios that involve communication across isolation barriers without adding components.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently.

For additional information on the FSI module, refer to the *Fast Serial Interface (FSI) Skew Compensation Application Report*.

12.4.5.1.1 FSI Features

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Double Data Rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally-triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- FSI-SPI compatibility mode (limited features available)
- Tag match notifications

12.4.5.1.2 FSI Not Supported Featurs

- SPI Compatibility Mode as General Use SPI
- External DMA Transfers
- Multi-Peripheral Configuration/TDM Generation
- Does not support for clkstop_req/ack functionality. Software must ensure that the FSI IP's on both host and remote device are idle before triggering clkstop_req.

12.4.5.2 FSI Environment

This section describes the Fast Serial Interface (FSI) external connections (environment).

12.4.5.2.1 Signal Description

FSI is a point-to-point communication protocol. Hence, an FSI transmitter core communicates directly to a single FSI receiver core. Similarly, an FSI receiver core receives data from a single FSI transmitter core.

Each FSI core has three signals: one clock and two data signals. Data is always transmitted or received with the most-significant bit of each frame field being first. If multilane transmissions are not used, the TXD1 and RXD1 signals can be left unconnected and the GPIOs repurposed for other application needs. Table 12-407 and Table 12-408 describe the various signals that can be selected by the PADCONFIG register to be brought out to device pins.

> **CAUTION**
> The maximum RXCLK rate is SYSCLK/2 and must not exceed this limit.

Table 12-419. FSI Receiver Core Signals

Signal Name	Direction	Description	Inactive Level(1)
RXCLK	Input	This is the receive clock input signal for the FSI receive module. This must be connected to TXCLK of the transmitting FSI module.	Logic High
RXD0	Input	This is the primary data input line for reception. This must be connected to the TXD0 of the transmitting FSI module.	Logic High
RXD1	Input	This is an additional data input line for reception. This signal must be connected to the TXD1 of the transmitting FSI module to use multilane transmission.	Logic High

(1) Inactive level refers to the state of the pin while the module is not actively receiving data.

Table 12-420. FSI Transmitter Core Signals

Signal Name	Direction	Description	Inactive Level(1)
TXCLK	Output	This is the transmit clock and is driven by the FSI transmit module. During a transmission, four clock edges are transmitted before the start of frame phase (preamble) and four clock edges follow the last bit of the frame (postamble). Data is transmitted on both edges of the clock. In FSI-SPI compatibility mode, the preamble and the post frame clock edges are not transmitted. Data is transmitted only on one edge of the clock. Data transmits on rising edge and received on falling edge of the clock.	Logic High
TXD0	Output	This is the primary data output line for transmission and is driven by the FSI transmit module. When the FSI is configured for multilane transmission, TXD0 contains all the even numbered bits of the data and CRC bytes. Other frame fields such as frame type, start-of-frame, tag, and end-of-frame are transmitted in full.	Logic High
TXD1	Output	This is an additional data output line for transmission, if the FSI is configured for multilane transmission. This signal is driven by the FSI transmit module. During transmission, the data bits are split between TXD0 and TXD1. TXD1 contains all the odd numbered bits of the data and CRC bytes. This applies only to the data words and the CRC bytes. Other data frame related information like Frame Type, Start-of-Frame, Tag and End-of-frame, the state of this line are identical to TXD0.	Logic High

(1) Inactive level refers to the state of the pin while the module is not actively transmitting, or held in reset.

12.4.5.3 FSI Integration

This section describes FSI_TX and FSI_RX module integration in the device, including information about clocks, resets, and hardware requests.

FSI Allocation within Device Domain

Table 12-421. FSI_TX Allocation within Device

Module Instance	Domain	
	MCU	MAIN
FSI_TX0	-	✓
FSI_TX1	-	✓

Table 12-422. FSI_RX Allocation within Device

Module Instance	Domain	
	MCU	MAIN
FSI_RX0	-	✓
FSI_RX1	-	✓
FSI_RX2	-	✓
FSI_RX3	-	✓
FSI_RX4	-	✓
FSI_RX5	-	✓

FSI Device Integration

Table 12-423. FSI_TX Device Integration

Module Instance	Power Sleep Controller	Power Domain	Local Power Sleep Controller (Module Domain)	Device Interconnect
FSI_TX0	PSC0	PD0	LPSC0	CBASS0
FSI_TX1	PSC0	PD0	LPSC0	CBASS0

Table 12-424. FSI_RX Device Integration

Module Instance	Power Sleep Controller	Power Domain	Local Power Sleep Controller (Module Domain)	Device Interconnect
FSI_RX0	PSC0	PD0	LPSC0	CBASS0
FSI_RX1	PSC0	PD0	LPSC0	CBASS0
FSI_RX2	PSC0	PD0	LPSC0	CBASS0
FSI_RX3	PSC0	PD0	LPSC0	CBASS0
FSI_RX4	PSC0	PD0	LPSC0	CBASS0
FSI_RX5	PSC0	PD0	LPSC0	CBASS0

FSI Clocks

Table 12-425. FSI_TX Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
FSI_TX0	FSI_TX0_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	FSI Transmit Interface Clock
	FSI_TX0_PLL_CLK	MAIN_SYSCLK0	PLLCTRL0	FSI Transmit Functional Clock Input
	FSI_TX0_CLK	FSI_TX0_PLL_CLK	FSI_TX0	FSI Transmit Functional Clock Output
FSI_TX1	FSI_TX1_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	FSI Transmit Interface Clock
	FSI_TX1_PLL_CLK	MAIN_SYSCLK0	PLLCTRL0	FSI Transmit Functional Clock Input
	FSI_TX1_CLK	FSI_TX1_PLL_CLK	FSI_TX1	FSI Transmit Functional Clock Output

Table 12-426. FSI_RX Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
FSI_RX0	FSI_RX0_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	FSI Receive Interface Clock
	FSI_RX0_CLK	FSI_RX0_CLK Pin	I/O Pin	FSI Receive Functional Clock
	FSI_RX0_LPBK_CLK	FSI_TX0_CLK	FSI_TX0	FSI Receive Loopback Clock
FSI_RX1	FSI_RX1_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	FSI Receive Interface Clock
	FSI_RX1_CLK	FSI_RX1_CLK Pin	I/O Pin	FSI Receive Functional Clock
	FSI_RX1_LPBK_CLK	FSI_TX0_CLK	FSI_TX0	FSI Receive Loopback Clock
FSI_RX2	FSI_RX2_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	FSI Receive Interface Clock
	FSI_RX2_CLK	FSI_RX2_CLK Pin	I/O Pin	FSI Receive Functional Clock
	FSI_RX2_LBCLK	FSI_TX0_CLK	FSI_TX0	FSI Receive Loopback Clock
FSI_RX3	FSI_RX3_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	FSI Receive Interface Clock
	FSI_RX3_CLK	FSI_RX3_CLK Pin	I/O Pin	FSI Receive Functional Clock
	FSI_RX3_LPBK_CLK	FSI_TX1_CLK	FSI_TX1	FSI Receive Loopback Clock
FSI_RX4	FSI_RX4_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	FSI Receive Interface Clock
	FSI_RX4_CLK	FSI_RX4_CLK Pin	I/O Pin	FSI Receive Functional Clock
	FSI_RX4_LPBK_CLK	FSI_TX1_CLK	FSI_TX1	FSI Receive Loopback Clock
FSI_RX5	FSI_RX5_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	FSI Receive Interface Clock
	FSI_RX5_CLK	FSI_RX5_CLK Pin	I/O Pin	FSI Receive Functional Clock
	FSI_RX5_LPBK_CLK	FSI_TX1_CLK	FSI_TX1	FSI Receive Loopback Clock

FSI Resets

Table 12-427. FSI_TX Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
FSI_TX0	FSI_TX0_RST	MOD_G_RST	LPSC0	Asynchronous Module Reset
FSI_TX1	FSI_TX1_RST	MOD_G_RST	LPSC0	Asynchronous Module Reset

Table 12-428. FSI_RX Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
FSI_RX0	FSI_RX0_RST	MOD_G_RST	LPSC0	Asynchronous Module Reset
FSI_RX1	FSI_RX1_RST	MOD_G_RST	LPSC0	Asynchronous Module Reset
FSI_RX2	FSI_RX2_RST	MOD_G_RST	LPSC0	Asynchronous Module Reset
FSI_RX3	FSI_RX3_RST	MOD_G_RST	LPSC0	Asynchronous Module Reset
FSI_RX4	FSI_RX4_RST	MOD_G_RST	LPSC0	Asynchronous Module Reset
FSI_RX5	FSI_RX5_RST	MOD_G_RST	LPSC0	Asynchronous Module Reset

FSI Interrupt Requests

Table 12-429. FSI_TX Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
FSI_TX0	FSI_TX0_INT0	R5FSS0_CORE0_INTR_IN_28 R5FSS0_CORE1_INTR_IN_28 R5FSS1_CORE0_INTR_IN_28 R5FSS1_CORE1_INTR_IN_28 PRU_ICSSG0_PR1_SLV_IN_45 PRU_ICSSG1_PR1_SLV_IN_45	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Transmit Interrupt 0
	FSI_TX0_INT1	R5FSS0_CORE0_INTR_IN_29 R5FSS0_CORE1_INTR_IN_29 R5FSS1_CORE0_INTR_IN_29 R5FSS1_CORE1_INTR_IN_29 PRU_ICSSG0_PR1_SLV_IN_54 PRU_ICSSG1_PR1_SLV_IN_54	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Transmit Interrupt 1
FSI_TX1	FSI_TX1_INT0	R5FSS0_CORE0_INTR_IN_30 R5FSS0_CORE1_INTR_IN_30 R5FSS1_CORE0_INTR_IN_30 R5FSS1_CORE1_INTR_IN_30 PRU_ICSSG0_PR1_SLV_IN_55 PRU_ICSSG1_PR1_SLV_IN_55	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Transmit Interrupt 0
	FSI_TX1_INT1	R5FSS0_CORE0_INTR_IN_31 R5FSS0_CORE1_INTR_IN_31 R5FSS1_CORE0_INTR_IN_31 R5FSS1_CORE1_INTR_IN_31 PRU_ICSSG0_PR1_SLV_IN_56 PRU_ICSSG1_PR1_SLV_IN_56	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Transmit Interrupt 1

Table 12-430. FSI_RX Interrupt Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
FSI_RX0	FSI_RX0_INT0	R5FSS0_CORE0_INTR_IN_16 R5FSS0_CORE1_INTR_IN_16 R5FSS1_CORE0_INTR_IN_16 R5FSS1_CORE1_INTR_IN_16 PRU_ICSSG0_PR1_SLV_IN_33 PRU_ICSSG1_PR1_SLV_IN_33	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Receive Interrupt 0

Table 12-430. FSI_RX Interrupt Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
	FSI_RX0_INT1	R5FSS0_CORE0_INTR_IN_17	R5FSS0_CORE0	Pulse	FSI Receive Interrupt 1
		R5FSS0_CORE1_INTR_IN_17	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_17	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_17	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_34	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_34	PRU_ICSSG1		
FSI_RX1	FSI_RX1_INT0	R5FSS0_CORE0_INTR_IN_18	R5FSS0_CORE0	Pulse	FSI Receive Interrupt 0
		R5FSS0_CORE1_INTR_IN_18	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_18	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_18	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_35	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_35	PRU_ICSSG1		
	FSI_RX1_INT1	R5FSS0_CORE0_INTR_IN_19	R5FSS0_CORE0	Pulse	FSI Receive Interrupt 1
		R5FSS0_CORE1_INTR_IN_19	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_19	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_19	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_36	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_36	PRU_ICSSG1		
FSI_RX2	FSI_RX2_INT0	R5FSS0_CORE0_INTR_IN_20	R5FSS0_CORE0	Pulse	FSI Receive Interrupt 0
		R5FSS0_CORE1_INTR_IN_20	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_20	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_20	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_37	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_37	PRU_ICSSG1		
	FSI_RX2_INT1	R5FSS0_CORE0_INTR_IN_21	R5FSS0_CORE0	Pulse	FSI Receive Interrupt 1
		R5FSS0_CORE1_INTR_IN_21	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_21	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_21	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_38	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_38	PRU_ICSSG1		

Table 12-430. FSI_RX Interrupt Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
FSI_RX3	FSI_RX3_INT0	R5FSS0_CORE0_INTR_IN_22 R5FSS0_CORE1_INTR_IN_22 R5FSS1_CORE0_INTR_IN_22 R5FSS1_CORE1_INTR_IN_22 PRU_ICSSG0_PR1_SLV_IN_39 PRU_ICSSG1_PR1_SLV_IN_39	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Receive Interrupt 0
	FSI_RX3_INT1	R5FSS0_CORE0_INTR_IN_23 R5FSS0_CORE1_INTR_IN_23 R5FSS1_CORE0_INTR_IN_23 R5FSS1_CORE1_INTR_IN_23 PRU_ICSSG0_PR1_SLV_IN_40 PRU_ICSSG1_PR1_SLV_IN_40	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Receive Interrupt 1
FSI_RX4	FSI_RX4_INT0	R5FSS0_CORE0_INTR_IN_24 R5FSS0_CORE1_INTR_IN_24 R5FSS1_CORE0_INTR_IN_24 R5FSS1_CORE1_INTR_IN_24 PRU_ICSSG0_PR1_SLV_IN_41 PRU_ICSSG1_PR1_SLV_IN_41	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Receive Interrupt 0
	FSI_RX4_INT1	R5FSS0_CORE0_INTR_IN_25 R5FSS0_CORE1_INTR_IN_25 R5FSS1_CORE0_INTR_IN_25 R5FSS1_CORE1_INTR_IN_25 PRU_ICSSG0_PR1_SLV_IN_42 PRU_ICSSG1_PR1_SLV_IN_42	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Receive Interrupt 1
FSI_RX5	FSI_RX5_INT0	R5FSS0_CORE0_INTR_IN_26 R5FSS0_CORE1_INTR_IN_26 R5FSS1_CORE0_INTR_IN_26 R5FSS1_CORE1_INTR_IN_26 PRU_ICSSG0_PR1_SLV_IN_43 PRU_ICSSG1_PR1_SLV_IN_43	R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1 PRU_ICSSG0 PRU_ICSSG1	Pulse	FSI Receive Interrupt 0

Table 12-430. FSI_RX Interrupt Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Interrupt Type	Description
	FSI_RX5_INT1	R5FSS0_CORE0_INTR_IN_27	R5FSS0_CORE0	Pulse	FSI Receive Interrupt 1
		R5FSS0_CORE1_INTR_IN_27	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_27	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_27	R5FSS1_CORE1		
		PRU_ICSSG0_PR1_SLV_IN_44	PRU_ICSSG0		
		PRU_ICSSG1_PR1_SLV_IN_44	PRU_ICSSG1		

FSI DMA Events

Table 12-431. FSI_TX DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	DMA Event Type	Description
FSI_TX[0:1]	-	-	-	-	Module does not support device DMA Events.

Table 12-432. FSI_RX DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	DMA Event Type	Description
FSI_RX[0:5]	-	-	-	-	Module does not support device DMA Events.

12.4.5.3.1 FSI Interrupts

Each FSI module contains multiple interrupt sources that can be assigned to two different interrupt vectors: INT1 and INT2. Each interrupt source has an associated status flag, force, and clear bits in the EVT_STS, EVT_FRC, and the EVT_CLR registers, respectively.

Each interrupt can be assigned to either interrupt vector, INT1 and INT2, to allow for two priority levels. Alternately, the interrupt source can be prevented from generating any interrupt, though the status flag can still be set and monitored by software. The transmitter events are assigned to either interrupt vector in the TX_INT_CTRL register. The receiver events are assigned an interrupt vector using RX_INT1_CTRL and RX_INT2_CTRL registers. If an interrupt is not required, make sure the bit is not set in the respective INT_CTRL register.

12.4.5.3.1.1 Transmitter Interrupts

The transmitter can generate the following interrupts:

- **Frame Done (FRAME_DONE)**
  This event indicates that FSI has completed transmitting a frame.
- **Buffer Underrun (BUF_UNDERRUN)**
  This event indicates that the transmit buffer has experienced underrun. Buffer underrun occurs when the transmitter tries to read data from a location which has not yet be written to by the CPU, or DMA.
- **Buffer Overrun (BUF_OVERRUN)**
  The buffer overrun interrupt is generated when the buffer has experienced overrun. Buffer overrun may occur if a piece of data is overwritten before it has been transmitted.
- **Ping Frame Triggered (PING_TRIGGERED)**
  The ping frame triggered interrupt is generated when the ping frame has been triggered. This bit will be set when the ping counter has timed out or an external ping trigger event has occurred.

12.4.5.3.1.2 Receiver Interrupts

The receiver core is capable of generating interrupts from many different events:

- **Ping Watchdog Timeout (PING_WD_TO)**
  This event indicates that the ping watchdog timer has timed out. The receiver has not received a valid frame within the time period specified in the RX_PING_WD_REF register.
- **Frame Watchdog Timeout (FRAME_WD_TO)**
  This event indicates that the frame watchdog timer has timed out. The conditions of this timeout are set using the RX_FRAME_WD_CTRL register. As soon as the start of frame phase is detected, the frame watchdog counter will start counting from 0. The end of frame phase must complete by the time the watchdog counter reaches the reference value. If this does not happen, the watchdog will time out and this event will be generated. If this event occurs, the receiver must undergo a soft reset and subsequent resynchronization in order to guarantee proper operation.
- **CRC Error (CRC_ERR)**
  This error indicates that a CRC error has occurred. A CRC error will be generated when the received CRC and the computed CRC do not match.
- **Frame Type Error (TYPE_ERR)**
  This error indicates that an invalid frame type has been received. If this error occurs, the receiver must undergo a soft reset and subsequent resynchronization in order to guarantee proper operation.
- **End-of-Frame Error (EOF_ERR)**
  This error indicates that an invalid end-of-frame bit pattern has been received. If this error occurs, the receiver must undergo a soft reset and subsequent resynchronization in order to guarantee proper operation.
- **Receive Buffer Overrun (BUF_OVERRUN)**
  This event indicates that an overrun condition has occurred in the receive buffer.
- **Receive Buffer Underrun (BUF_UNDERRUN)**
  This event indicates that an underrun condition has occurred in the receive buffer. This condition occurs when software reads the buffer while it is empty.
- **Frame Done (FRAME_DONE)**
  This event indicates that a valid frame has been received without error.
- **Error Frame Received (ERR_FRAME)**
  This event indicates that an error frame has been received.
- **Ping Frame Received (PING_FRAME)**
  This event indicates that a ping frame has been received.
- **Frame Overrun (FRAME_OVERRUN)**
  This event indicates that a new frame has been received while the FRAME_DONE flag was still set.
- **Data Frame Received (DATA_FRAME)**
  This event indicates that a data frame has been received.
- **Ping Tag Matched (PING_TAG_MATCH)**
  This event indicates that a ping frame with a matching tag has been received.
- **Data Tag Matched (DATA_TAG_MATCH)**

This event indicates that a data frame with a matching tag has been received.

- **Error Tag Matched (ERROR_TAG_MATCH)**
  This event indicates that an error frame with a matching tag has been received.

12.4.5.3.1.3 Configuring Interrupts

To configure interrupts on the FSI, the application must select the interrupt vector for each desired event using the TX_INT_CTRL register for the transmitter, and RX_INT1_CTRL and RX_INT2_CTRL registers for the receiver. There is no module-level interrupt enable bit to configure.

Note

If an event is registered for both interrupt vectors, both interrupts fire. There are no hardware checks for overlapping interrupt vector assignments.

12.4.5.3.1.4 Handling Interrupts

Inside the interrupt service routine (ISR), the user must clear the event flag using the EVT_CLR register and then acknowledge the CPU interrupt.

If the one event occurs multiple times before the corresponding bit is cleared by software, no new interrupt is generated.

If multiple events occur simultaneously, or very close in time, it is possible to handle multiple conditions within a single interrupt. Each flag is independently set by hardware and must be cleared by application software. If multiple different events occur, the ISR can handle each in whatever order is deemed necessary by the application. It is not advisable to clear the full interrupt status register in every ISR. This can cause the application to miss events that can be detrimental to the application. A sample sequence for handling interrupts on the receiver follows; the transmitter routine is similar.

- On receiving an interrupt, copy the current state of the receive event and error status flag register (RX_EVT_STS) into a local snapshot variable.
- Read all of the bits from the snapshot to determine the events that require action.
- Perform the necessary actions for each of the events seen in the snapshot.
- Write to the receive event and error clear register (RX_EVT_CLR) with the snapshot to clear only those interrupts that were set at the beginning of the ISR.
- Repeat this sequence for every generated ISR.

There is a chance that another event occurred during the just-handled ISR since only the snapshot of events was handled and then cleared; an event flag can still be set at the end of the ISR. As soon as the ISR completes, a new interrupt is generated and this flag is still set and can be handled accordingly.

Software accesses tied to multiple events and handled within the same ISR can cause race conditions that cause the software to not function as desired. For example, it is recommended to use different interrupt lines if the user wants to enable events for both ping and data frames. If both events are handled within the same interrupt line, the software can only respond to one of the events if both events occur close in time.

12.4.5.4 FSI Functional Description

12.4.5.4.1 FSI Functional Description

The Fast Serial Interface Transmitter and Receiver modules (FSI_TX/FSI_RX) are two completely independent modules on the device. Each module has an independent set of control registers, clocking, and interrupts. The following sections describe the frame format and the various initialization and configuration procedures for both the transmitter and receiver.

12.4.5.4.2 FSI Transmitter Module (FSI_TX)

The FSI transmitter module handles the framing of data, CRC generation, and signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers allow the CPU to program, control, and monitor the operation of the FSI receiver. The transmit data buffer is accessible by the CPU.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Externally triggered data frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data

Figure 12-394 shows the high-level block diagram of the FSI transmitter. Figure 12-395 shows the block diagram of the transmitter core submodule.

The following sections describe the various aspects of the FSI transmitter in detail.

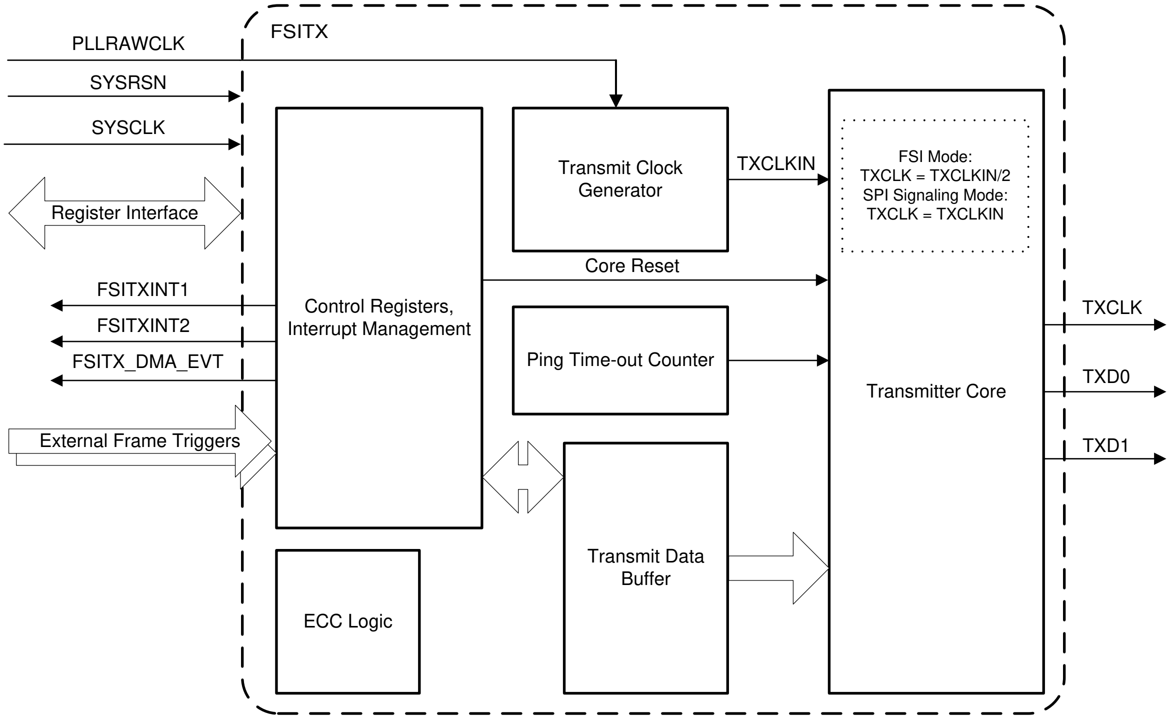

Figure 12-394. FSI Transmitter Block Diagram

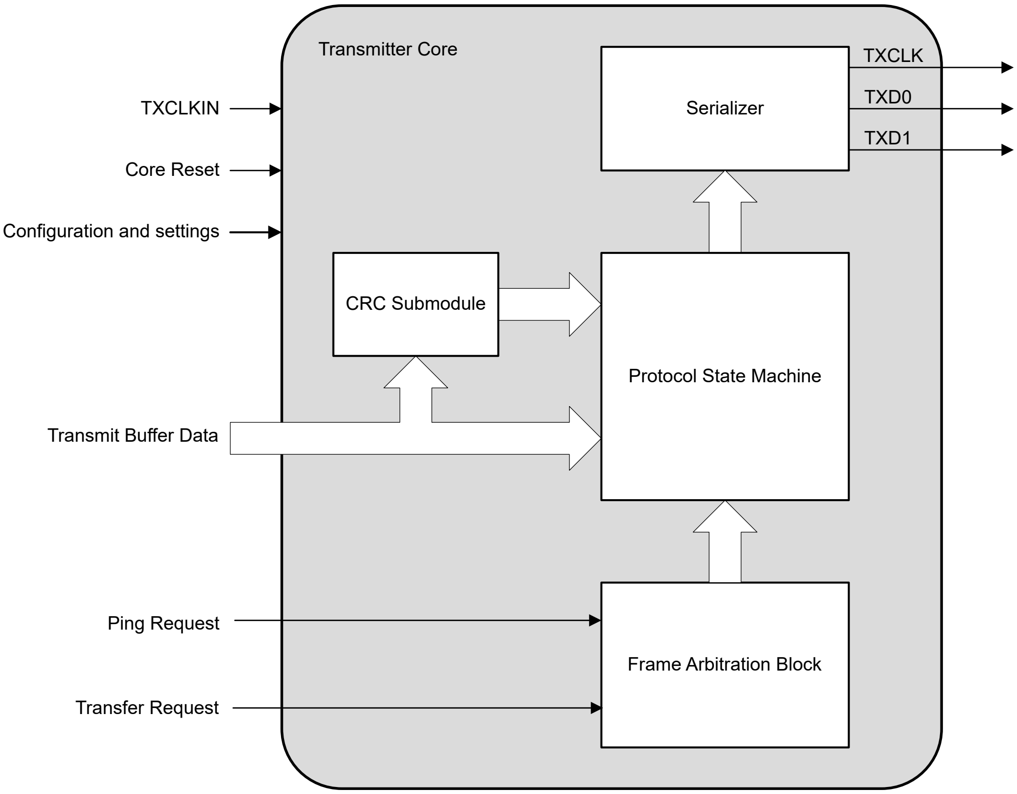

Figure 12-395. FSI Transmitter Core Block Diagram

12.4.5.4.2.1 Initialization

On the first initialization or after a module reset due to an underrun condition, the transmitter module executes the following initialization sequence to start or resume transmit operations.

1. Initialize the transmitter clock by setting TX_CLK_CTRL.CLK_RST to 1 and subsequently clearing the bit.
2. Set the clock to the transmitter core to PLLRAWCLK by setting TX_OPER_CTRL_LO.SEL_PLLCLK to 1.
3. Set the clock prescaler value to the desired rate by writing to TX_CLK_CTRL.PRESCALE_VAL.
4. Enable the transmitter clock divider by setting TX_CLK_CTRL.CLK_EN to 1.
5. Assert the transmitter module soft reset by writing 0xA501 to TX_MASTER_CTRLTX_MAIN_CTRL.
6. Wait four TXCLK cycles.
7. Release the transmitter core from reset by writing 0xA500 to TX_MASTER_CTRLTX_MAIN_CTRL.

After initialization and configuration, the transmitter module synchronizes with the receiver module before transmitting. The synchronization sequence is described in Section 12.4.5.5.1 .

CAUTION

Do not change TX_CLK_CTRL.PRESCALE_VAL while the clock is enabled (TX_CLK_CTRL.CLK_EN = 1). Doing so can cause undefined behavior.

12.4.5.4.2.2 FSI_TX Clocking

The transmitter core registers and control logic run off of the device system clock (SYSCLK).

The FSI Transmit Clock (TXCLK) is derived from PLLRAWCLK. PLLRAWCLK is divided down by configuring the clock prescaler value (TX_CLK_CTRL.PRESCALE_VAL) then setting the clock divider enable bit (TX_CLK_CTRL.CLK_EN). The clock prescaler value can be set to divide PLLRAWCLK by 1 (TX_CLK_CTRL.PRESCALE_VAL = 0x0 or 0x1) through 255(TX_CLK_CTRL.PRESCAL_VAL = 0xFF). Though TXCLK and SYSCLK are both derived from PLLRAWCLK, TXCLK is asynchronous with respect to SYSCLK.

CAUTION

TXCLK must never be configured to be faster than SYSCLK/2.

12.4.5.4.2.3 Transmitting Frames

On the transmitter, the ping frame is the only frame that can be set up and transmitted without any further software or DMA intervention. Ping frames can be transmitted by any (or all) of the three sources: automatic ping timer, software, or external triggers.

Each available frame type can be sent multiple ways. Generically, the following steps must be executed before the frame is sent. These steps can be executed in any order before the start condition is set.

1. Configure the frame type
2. Set the frame tag
3. If the frame to be sent is a data frame:
   - Set the user data
   - Write to the data buffer
   - Set the word length if the frame is a software defined frame length
4. Set the start condition

Note

Transmit Frame Start Restriction:

A new frame transmission can be initiated by one of the methods selected in the TX_OPER_CTRL_LO.START_MODE bits. If there is already a PING frame transmission taking place, due to a hardware initiated PING timer, the new frame transmission begins as soon as the on-going PING transmission is completed.

Once a START of frame has been initiated, the next START of frame is recognized when the first frame has started transmitting the End-of-Frame (EOF) field. If a new START trigger arrives before the current transmission has reached the EOF field, the trigger is lost without a notification.

Note

There is no hardware check implemented to check whether the type field written by software is valid or not. If an invalid type is used and a frame transmission is initiated, the behavior is:

- The transmitted frame structure is exactly like an NWORD data frame. The size of the data frame is determined by the value in the TX_FRAME_CTRL.N_WORDS register.
- The frame type field of the transmitted data frame is transmitted as programmed. If this is received by an FSI receiver, a Type error is generated.

This mechanism can be used for force a Type error in a received frame for testing purposes.

The following sections describe the specific configuration for each frame type and start condition.

12.4.5.4.2.3.1 Software Triggered Frames

The most basic way to transmit a data frame is through software. Each step must be handled by the application. To send a data frame using software, the following steps must be executed. Steps 1-6 can be executed in any order before setting TX_FRAME_CTRL.START. Some fields do not need to be reconfigured for every transmission. The frame tag, user data, and frame type are sticky and are retransmitted in the subsequent frame unless modified by software.

1. Write the data to be transmitted to the next location of the transmit data buffer.
2. Set TX_FRAME_CTRL.FRAME_TYPE to the appropriate value for the type of frame to be transmitted.
3. Set TX_FRAME_CTRL.N_WORDS to 1 less than the number of words to be transmitted if TX_FRAME_CTRL.FRAME_TYPE is set to 0011, the frame type of the software-defined length data frame. That is, if 16 words are transmitted, N = 16, set TX_FRAME_CTRL.N_WORDS to 15.
4. When the frame is assembled before transmitting, the FSITX hardware calculates the CRC to be transmitted. If TX_OPER_CTRL_LO.SW_CRC is 1, the application can calculate a custom CRC value and then set TX_USER_CRC to the result.
5. Set TX_FRAME_TAG_UDATA.FRAME_TAG to the desired tag.
6. Set TX_FRAME_TAG_UDATA.USER_DATA to the desired user data.
7. Set TX_FRAME_CTRL.START to 1 to initiate the transmission of the data frame.

Once the frame transmission has started, the TX_FRAME_CTRL.START is cleared by hardware. To monitor if the frame has completed, the software can poll TX_EVT_STS.FRAME_DONE.

12.4.5.4.2.3.2 Ping Frame Generation

Assuming the FSI transmitter has already been properly initialized, the following sequences can be used to configure and send ping frames.

12.4.5.4.2.3.2.1 Automatic Ping Frames

To generate periodic ping frames, the following steps must be followed:

1. Initialize the ping counter by writing 1 to TX_PING_CTRL.CNT_RST.
2. Set the desired ping tag to TX_PING_TAG.TAG.
3. Set the ping timer reference value to TX_PING_TO_REF.TO_REF.
4. Enable the ping timer by writing 1 to TX_PING_CTRL.TIMER_EN.

The ping timer is a free-running counter that counts up from 0. The current value of the ping timer counter is found in TX_PING_TO_CNT. When the current value of TX_PING_TO_CNT matches the reference value TX_PING_TO_REF.TO_REF, the TX_EVT_STS.PING_TRIGGERED is set. TX_PING_TO_CNT resets to 0 and resumes counting until the next match has occurred or the ping timer is halted by software (TX_PING_CTRL.TIMER_EN is set to 0).

12.4.5.4.2.3.2.2 Software Triggered Ping Frame

Software can also manually generate a ping frame. The process for sending a ping frame with software is very similar to sending the other types of frames. The following steps must be followed:

1. Set TX_FRAME_CTRL.FRAME_TYPE to 0000’b to denote that the frame being sent is a Ping Frame.
2. Set TX_FRAME_TAG_UDATA.FRAME_TAG to the desired value.
3. Write 1 to TX_FRAME_CTRL.START. This starts the transmission.

Once the frame transmission has started, the TX_FRAME_CTRL.START is cleared by hardware. To monitor if the frame has completed, the software can poll TX_EVT_STS.FRAME_DONE.

12.4.5.4.2.4 Transmit Buffer Management

The FSI transmitter has a 16-word buffer that the FSI transmitter pulls data to transmit. This buffer is implemented as a circular buffer, not a FIFO, so some care must be taken to properly interpret buffer overrun and underrun, as well as the TX_BUF_PTR_STS register. These flags and pointers work under the assumption that the software or DMA is using the buffer as a circular buffer. This mode of operation is the only way that the overrun, underrun, and pointer status are meaningful. If data is being sourced by the DMA and there is some other periodic trigger mechanism trying to initiate transfers, underrun becomes a critical error. If an underrun happens, a buffer went out of sync. This not only affects the current transfer, but can also affect all future transfers due to the ring buffer. Under such conditions, the underrun needs a soft reset to cleanly recover. Alternately, the software can manually stop the transmitting, reset the buffer pointers, clear the remaining error conditions, and then restart transmission. The software method involves a few steps, while the soft reset is a single action and makes sure of a full reset of the control registers.

Due to the flexibility of the transmit buffer, software can implement a simple ping-pong buffer or randomly load and send from any location of the buffer. If the buffer is used in this manner, error flags and status fields can be ignored without adversely affecting the transmitter capability. Additionally, the CURR_WORD_CNT is also invalid if used in this way. The application can set the buffer pointer manually by writing the 4-bit index to TX_BUF_PTR_LOAD. This forces the transmitter to start picking the data from the indicated location in the buffer.

12.4.5.4.2.5 CRC Submodule

The FSI transmitter can supply the CRC to the frame being transmitted through the embedded hardware CRC submodule or by supplying a user-defined value. This is controlled by setting TX_OPER_CTRL_LO.SW_CRC appropriately.

If hardware CRC generation is selected (TX_OPER_CTRL_LO.SW_CRC = 0, the default), the CRC is computed by hardware on the data and user data fields using the CRC polynomial 0x7 ($x^8 + x^2 + x + 1$). The transmitter module automatically computes the CRC on the data fields without user intervention when the frame is transmitted. For more information on how the CRC is generated by the CRC submodule, refer to Section 12.4.5.4.7 .

If software CRC generation is selected (TX_OPER_CTRL_LO.SW_CRC = 1), the CRC must be computed by software and placed in the TX_USER_CRC register. The next frame to be transmitted uses the value placed in the TX_USER_CRC register in place of the CRC value generated by the hardware.

As the TX_USER_CRC register is software-programmable, the application can use this field as an extra data field for application-specific purposes. If TX_USER_CRC is used in this manner, the CRC detection on the receiver is not valid and must be ignored.

12.4.5.4.2.6 Conditions in Which the Transmitter Must Undergo a Soft Reset

Unlike the receiver, there are no detectable errors that require a soft reset. A buffer overrun or underrun interrupt can or cannot require a soft reset to resume proper operation. This determination is up to the application software. Refer to Section 12.4.5.4.2.4 for more information on the transmit buffer.

12.4.5.4.2.7 Reset

The entire transmitter module and all transmitter registers are reset by SYSRSn. The transmitter core is reset by SYSRSn or by writing a 1 to TX_MAIN_CTRL.CORE_RST.

A module reset causes the registers to be reset to the default state.

12.4.5.4.3 FSI Receiver Module (FSI_RX)

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after they pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers allow the CPU to program, control, and monitor the operation of the FSI receiver. The receive data buffer is accessible by the CPU.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- FSI-SPI compatibility mode

Figure 12-396 provides a high-level overview of the internal modules present in the FSI receiver. Figure 12-397 shows a view of the FSI receiver core submodule. Not all data paths and internal connections are shown.

The following sections describe the various aspects of the FSI receiver module.

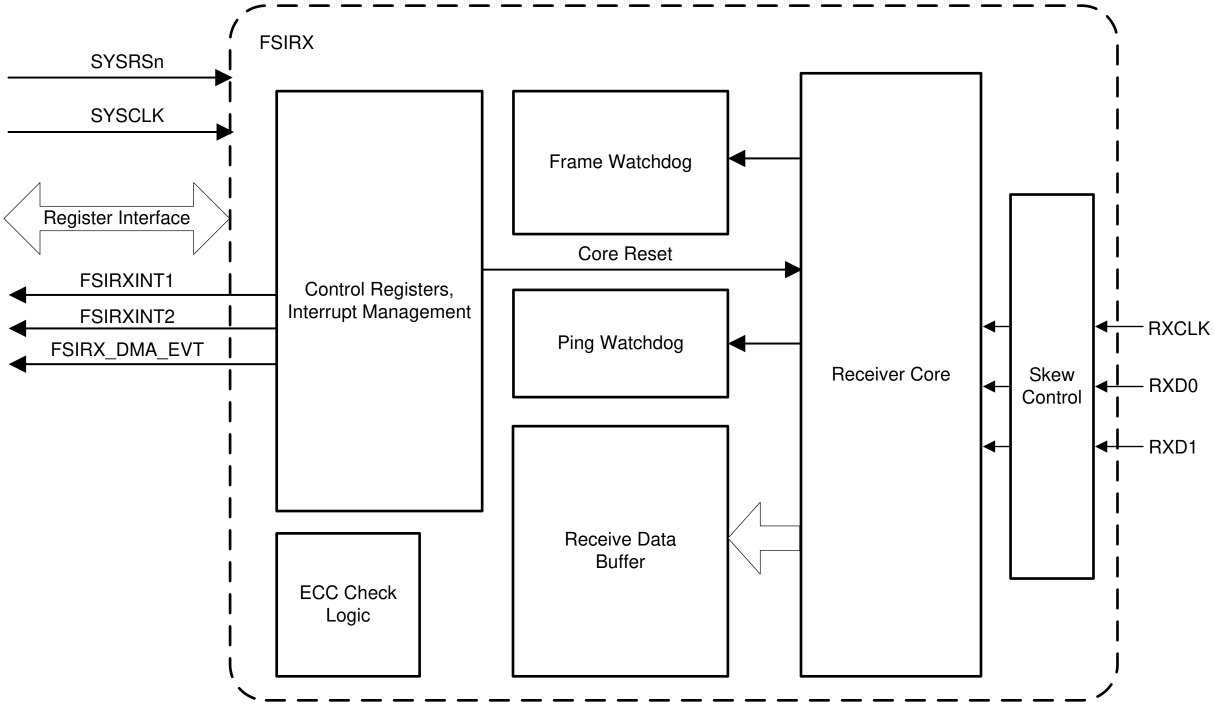

Figure 12-396. FSI Receiver Block Diagram

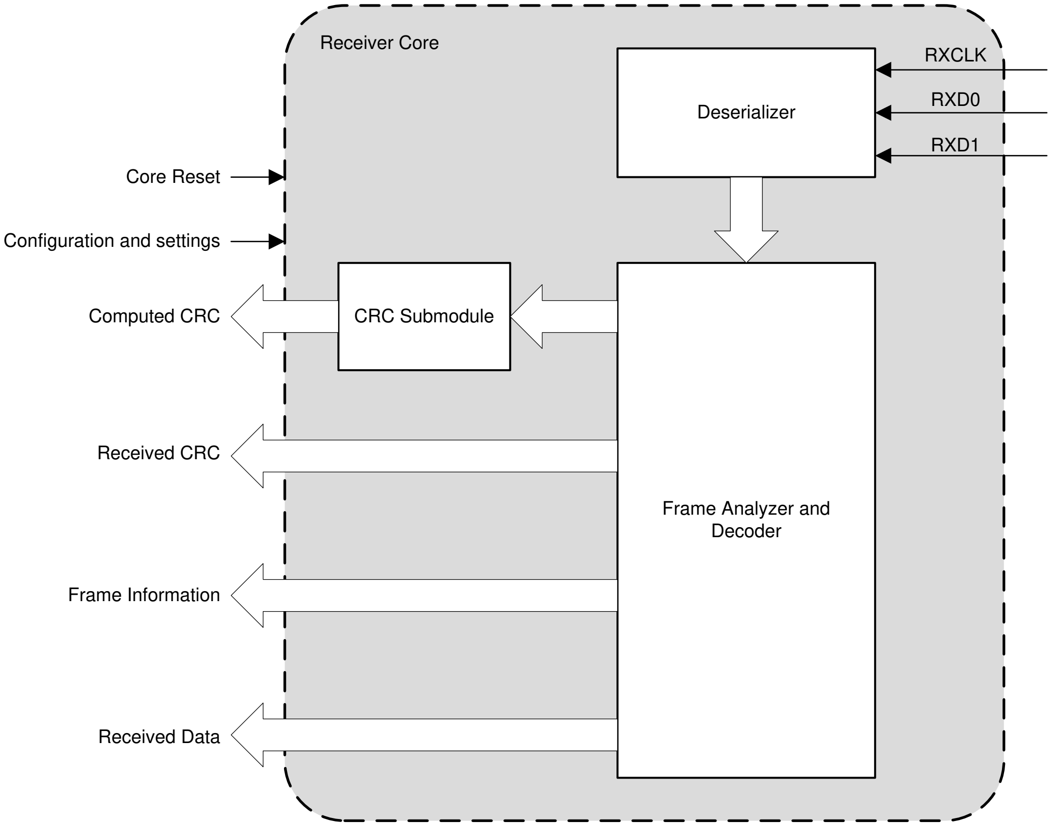

Figure 12-397. FSI Receiver Core Block Diagram

12.4.5.4.3.1 Initialization

On the first initialization or after a module reset following any frame error, the receiver module asserts and releases the receiver core reset bit (RX_MAIN_CTRL.CORE_RSTRX_MASTER_CTRL.CORE_RST) prior to any other initialization. Once the receiver module is initialized, the following steps are executed:

1. If required, assign interrupt sources to the necessary interrupt line.
2. If required, configure the ping watchdog to periodically check for an active link to the transmitter. See Section 12.4.5.4.3.4 for configuration details.
3. If required, configure the frame watchdog to make sure that each frame is received within a predetermined window. See Section 12.4.5.4.3.5 for configuration details.
4. Initialize the receive buffer pointer by writing to the RX_BUF_PTR_LOAD register. Received data is placed into the buffer starting with the address loaded in this register.
5. Make sure all errors and flags have been cleared from the RX_EVT_STS register.

At this point the receiver is ready to receive any incoming frames. Software can now either poll on the RX_EVT_STS register for various conditions. For example, when the RX_EVT_STS.FRAME_DONE and no other flags are set, the receiver has successfully received a frame without error.

Next, the application configures the various features such as the ping and frame watchdogs, DMA, external triggering, and so on. These features are described in subsequent sections. The receiver module is now ready to synchronize with the transmitter then begin reception. The synchronization sequence is described in Section 12.4.5.5.1 .

12.4.5.4.3.2 FSI_RX Clocking

The receiver module registers and control logic are clocked by the device system clock (SYSCLK). The receiver state machine is clocked by the receiver input clock pin (RXCLK).

> **CAUTION**
>
> RXCLK must never be faster than SYSCLK.

12.4.5.4.3.3 Receiving Frames

Once the receiver has been properly configured and synchronized, incoming messages are handled as described below. Note that there is no equivalent to a chip-select signal to gate incoming data. Every valid clock edge latches data into the receiver.

The header information of the received frame is placed in the respective register fields.

- RX_FRAME_INFO.FRAME_TYPE contains the received frame type.
- RX_FRAME_TAG_UDATA.FRAME_TAG contains the received frame tag.
- RX_FRAME_TAG_UDATA.USER_DATA contains the received user data.

If any error conditions occur during reception such as a CRC mismatch, frame error, frame timeout, buffer overrun, or ping watchdog timeout, the corresponding flag is set in the RX_EVT_STS register.

> **Note**
>
> If at any point during operation a frame error occurs, the receiver module must be reset and re-synchronized with the transmitter before the next frame can be successfully received. The follow errors are classified as frame errors:
>
> - Type error
> - CRC error
> - End of frame error

12.4.5.4.3.4 Ping Frame Watchdog

The ping frame watchdog is a hardware-enabled automatic error detection of the connection status to the transmitter. This watchdog monitors the time elapsed between ping frames. If the transmitter has been set up to periodically send out a ping frame, the receiver can be set up to monitor whether this frame has been received within a specified amount of time. If the time between ping frames has exceeded the programmed number of clock cycles, an event is triggered that can generate an interrupt or be monitored by software.

This watchdog has a dedicated counter that is reset and restarted upon the successful reception of a ping frame. The watchdog counter is incremented at the rate of SYSCLK. Optionally, the watchdog can be configured to be reset upon the successful reception of any frame. This option allows the receiver to monitor for any successful frame to indicate that the connection is still alive and the transmitter is still functioning as expected.

To configure the ping frame watchdog for operation:

1. Reset the ping watchdog counter by setting RX_PING_WD_CTRL.PING_WD_RST to 1 and then subsequently clearing the bit to 0.
2. Set RX_OPER_CTRL.PING_WD_RST_MODE to the desired watchdog reset event, set to 0 for ping frames only or set to 1 for any frame.
3. Set RX_PING_WD_REF to the maximum time between frames. Add 10 additional SYSCLK cycles to account for clock synchronization.
4. Enable the ping watchdog by setting RX_PING_WD_CTRL.PING_EN to 1.

The ping watchdog is now enabled and can now monitor for ping frames.

If the RX_PING_WD_CNT value reaches the value programmed in RX_PING_WD_REF, the RX_EVT_STS.PING_WD_TO flag is set. If configured, an interrupt can be generated on this event.

12.4.5.4.3.5 Frame Watchdog

The frame watchdog is an additional feature the receiver can use to monitor for any error conditions. This dedicated watchdog monitors the duration for a single frame to be received. The watchdog starts incrementing at the time the receiver detects a proper start of frame condition. If the end of frame condition is not detected within the expected number of SYSCLK cycles, the frame watchdog is triggered that can generate an interrupt or be monitored by software.

This watchdog is automatically started and stopped at the start-of-frame and end-of-frame conditions, respectively. The frame watchdog is connected to SYSCLK.

To configure the frame watchdog for operation:

1. Reset the frame watchdog counter by setting RX_FRAME_WD_CTRL. FRAME_WD_CNT_RST to 1 and then subsequently clearing the bit to 0.
2. Set RX_FRAME_WD_REF.FRAME_WD_REF to the maximum number of SYSCLK cycles expected to be in the longest frame that can be received. Add an additional 10 SYSCLK cycles to account for clock synchronization.
3. Enable the frame watchdog by setting RX_FRAME_WD_CTRL.FRAME_WD_CNT_EN to 1.

The frame watchdog is now enabled and can detect a failed frame.

If the RX_FRAME_WD_CNT reaches the value programmed in RX_FRAME_WD_REF, the RX_EVT_STS.FRAME_WD_TO flag is set. If enabled, an interrupt can be generated on this event.

If the frame watchdog interrupt ever occurs, the receiver core is in an invalid state to receive a new transmission. The only way to recover from a frame watchdog time out is to undergo a soft reset, and subsequently resynchronizing with the transmitter.

12.4.5.4.3.6 Delay Line Control

The receiver module has a programmable delay line on each of the external signal inputs: RXCLK, RXD0, and RXD1. The delay elements introduce delays on the respective lines. This is to facilitate adjustment for signal delays introduced by system level components such as signal buffers, ferrite beads, isolators, and so on, or board delays such as uneven trace lengths, long cable length, and so on. The length of the delay is controlled by setting the RX_DLY_LINE_CTRL register values for each line. By default, no delay is introduced by the delay line elements. The delay values must only be adjusted while the FSIRX is held in soft reset, making sure that there are no active transmissions during this process. Figure 12-398 shows a representation of the delay line circuitry for the input signals. The implementation for RXCLK, RXD0, and RXD1 are replicas of this diagram. All circuits behave similarly.

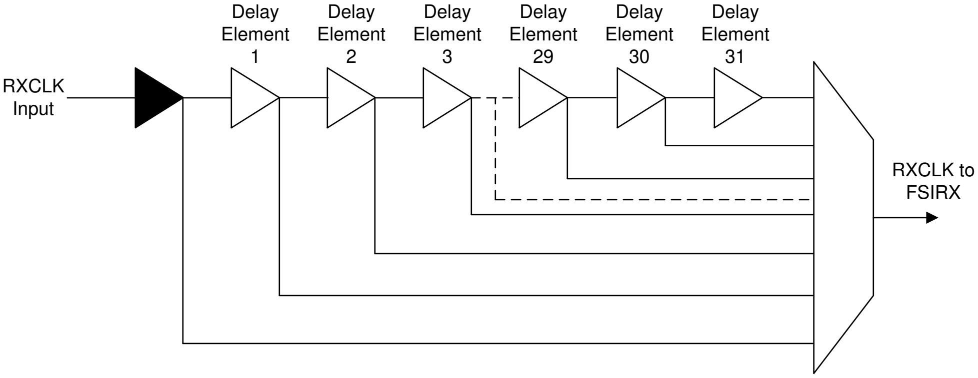

Figure 12-398. Delay Line Control Circuit

For more information on skew compensation, refer to *Fast Serial Interface (FSI) Skew Compensation*.

12.4.5.4.3.7 Buffer Management

The FSI receiver has a 16-word buffer that the data is copied to when the data has been received. This buffer is implemented as a circular buffer, not a FIFO, so some care must be taken to properly interpret buffer overrun and underrun as well as the RX_BUF_PTR_STS register. These flags and pointers work under the assumption that the software or DMA is using the buffer as a circular buffer. If the receiver state machine enters into an erroneous state, there is no way for software to cleanly handle this because there is no specified receive clock. For the receiver to detect a clean resynchronization, the state machine needs to be operational and not in the error state. The only way to recover from the error state is to reset the entire receiver module. For overrun and underrun, the receiver can no longer verify that values in the buffer are valid. As such, the best way to recover is to reset the FSI and resynchronize with the transmitter.

Due to the flexibility of the receive buffer, it is possible for software to implement a simple ping-pong buffer, or to randomly receive and read from any location of the buffer. If the buffer is used in this manner, these flags and status fields can be ignored without adversely affecting the receiver capability. Additionally, the CURR_WORD_CNT is also invalid if used in this way. The application can set the buffer pointer manually by writing the 4-bit index to RX_BUF_PTR_LOAD. This forces the receiver to start storing the received data starting at the indicated location in the buffer.

12.4.5.4.3.8 CRC Submodule

The receive module automatically calculates the CRC on the incoming data. The received CRC value is placed into RX_CRC_INFO.RX_CRC. The CRC value calculated by hardware on the received data is placed into RX_CRC_INFO.CALC_CRC. These values are compared by hardware and RX_EVT_STS.CRC_ERROR is set if there is a mismatch. The receiver can generate an interrupt based on RX_EVT_STS.CRC_ERROR if enabled.

Since the CRC is only used in data frames, the values found in RX_CRC_INFO.RX_CRC and RX_CRC_INFO.CALC_CRC are undefined during ping and error frames.

For more information on how the CRC is calculated, refer to Section 12.4.5.4.7 .

If the transmitting module is sending a software-defined CRC value (FSITX.TX_OPER_CTRL_LO.SW_CRC = 1), the receiver module triggers a CRC error event if the received value does not match the hardware-calculated value. As this is an application-level decision, the FSIRX can safely disregard the CRC error event. Application software needs to calculate and verify the incoming CRC using the same custom algorithm used on the transmitter and act appropriately.

The CRC field can also be used as an application-specific value, not a CRC. The application can use the RX_CRC_INFO.RX_CRC as required. All CRC errors and flags can be ignored in this situation.

12.4.5.4.3.9 Using the Zero Bits of the Receiver Tag Registers

The receiver tag registers (receiver frame tag and user data (RX_FRAME_TAG_UDATA) register and receiver ping tag (RX_PING_TAG) register)) have the least-significant bit set to 0. The actual received tag is in the bit positions 4:1. The reason for this is to facilitate user software to create a table of functions that can be called depending on the tag value. A function pointer needs a 32-bit storage space and, hence, each successive pointer is offset by 2. If the first pointer is at address x, then the second pointer is at address x + 2, the third at address x + 4, and so on. By keeping the LSB to 0, the five bits of the tag register (bits 4:0) can now be directly used as an index into a table of function pointers.

12.4.5.4.3.10 Conditions in Which the Receiver Must Undergo a Soft Reset

The receiver receives data on every clock edge. While there are specific patterns that determine the a start of a frame, and denote the end of a frame, these patterns are able to occur at any point during normal operation inside of the frame. If there ever is a point at which the receiver fails to detect a successful frame, the module must be reset to make sure that subsequent frames are received properly.

When any of the following errors occur in a received frame, the receiver can be required to be reset and resynchronized with the transmitter:
- Frame type error
- End of frame error
- Ping frame watchdog timeout
- Frame watchdog timeout
- Receiver in an invalid state due to noisy clock

The receiver core status (RX_VIS_1.RX_CORE_STS) can be monitored to determine if the receiver core has entered into an error state requiring a soft reset to resume communication. Incorrect frame type and end of frame errors always cause this bit to become set. A soft reset is required in these cases. A frame watchdog timeout always requires a reset due to the fact that the receiver state machine is still expecting more information when the watchdog timed out. RX_CORE_STS can be used to determine if a noise event was the cause of the failed frame. The ping frame watchdog also does not cause RX_CORE_STS to be set. Similar to the frame watchdog, a corrupt receiver can not be the reason for the ping frame to have timed out. The transmitter can have gone offline and never sent a ping frame. Alternately, during idle time, a noise event can have occurred, thereby putting the receiver into a corrupt state. As the receiver is able to detect this during the ping frame watchdog timeout interrupt handler, this type of event is not lost and the application can act appropriately.

As the receiver is clocked by RXCLK, not SYSCLK, a noisy clock or data line can cause some internal design constraints to be violated, putting the receiver core logic into undefined states. Make sure that the clock and data lines satisfy the Electrical Characteristics and timing requirements of the FSI module found in the device data sheet. Failure to do so can cause the receiver state machine to go into an unrecoverable error state. The receiver can only be recovered by undergoing a soft reset. To determine the state of the receiver core after an unexpected frame error, the application must check the receiver core status bit.

In addition to the above errors, buffer overrun or underrun can warrant a soft reset to resynchronize with the local application software. Refer to Section 12.4.5.4.3.8 for more information on the receive buffers. The requirement of resetting the receiver due to overrun or underrun is up to the application.

After the receiver has been placed into soft reset, the application must notify the other device's transmitter to begin a new synchronization phase. The simplest way to achieve this is through a ping or error frame sent with a designated tag. If the application is not using the FSITX on the device with the detected error, some other method must be established. The other device must stop transmitting and begin a new synchronization phase.

12.4.5.4.3.11 FSI_RX Reset

The receiver module and the registers are reset by SYSRSn. The receiver core is reset by SYSRSn or by writing a 1 to RX_MAIN_CTRL.CORE_RST.

A module reset causes the registers to be reset to the default state. After a module reset, the receiver module must be re-initialized and the data link re-established.

12.4.5.4.4 Frame Format

The FSI module transmits and receives information in frames. Each frame contains multiple phases where different information can be found. The number of phases as well as the total length of the frame varies depending on the frame type being transmitted. Frames can be as short as 16-bits long for a ping or error frame or 288-bits long for a 16-word data frame.

In normal transmission mode, there are four preamble clock edges before the start of the frame and four post-frame clock edges (postamble). Data is transmitted on both edges of the clock (double data rate). The basic frame structure is shown in Table 12-421. Each phase of the frame (such as start-of-frame, frame type, and so on) is transmitted with the most-significant bit first. Table 12-421 describes the basic frame structure used by the FSI and adapted according to which frame type is transmitted.

Table 12-433. Basic Frame Structure

Idle State	Preamble	Start of Frame	Frame Type	User Data	Data Words	CRC Byte	Frame Tag	End of Frame	Postamble	Idle State
	1111	1001	4 bits	8 bits	1-16 words	8 bits	4 bits	0110	1111	

The FSI also supports a FSI-SPI compatibility mode. The SPI compatible frame structure is similar to a standard FSI frame, but there are differences. Refer to Section 12.4.5.4.9 for more information on how to configure and use the FSI-SPI compatibility mode.

Note

One word of the FSI refers to 16 bits.

The terms “frame” and “packet” can be used interchangeably to describe the signaling format of the FSI.

12.4.5.4.4.1 FSI Frame Phases

The different phases of the frame structure are described in detail.

- **Idle State:** During the idle state, the clock and data lines are driven high, the inactive state.
- **Preamble:** The preamble phase contains four clock edges (or two complete clock pulses) with the data signals held in the high state. These clock edges serve to flush the receiver logic and prepare the receiver logic for receiving a new frame. This phase is not present in SPI compatibility mode.
- **Start of Frame:** The start of frame phase contains two clock pulses with four bits, 1001, transmitted on the data lines.
- **Frame Type:** The frame type phase contains two clock pulses with the 4-bit frame type code being transmitted on the data lines. The different frame types are described in detail in Section 12.4.5.4.4.2 . The transmitter must set the TX_FRAME_CTRL.FRAME_TYPE field before transmitting a frame. The received frame type is stored in the RX_FRAME_INFO.FRAME_TYPE.
- **User Data:** The user data phase contains a fully user-configurable data field. There are no restrictions on how this field is used. This phase is only available in data frames. The user data to be transmitted is set by writing to TX_FRAME_TAG_UDATA.USER_DATA. The received user data is stored in RX_FRAME_TAG_UDATA.USER_DATA.
- **Data:** The data phase contains the data that is being transmitted. The data is pulled from the transmit buffer of the transmitter and is placed in the receive buffer of the receiver. Word 0 is transmitted first. This phase is only present in data frames. Depending on the type of frame transmitted, this can contain anywhere between 1 and 16 words depending on the frame type selected. More information on data frames is found in Section 12.4.5.4.4.2.3 .
- **CRC Byte:** The CRC byte contains the CRC of the transmitted data. The value present in this phase can be sourced from either hardware or software based on the TX_OPER_CTRL_LO.SW_CRC bit. Refer to the module-specific section of the CRC Submodule for more information on the CRC is generated or used, for the transmitter and receiver modules respectively. The CRC byte is only present in data frames.
- **Frame Tag:** The frame tag contains the 4-bit user-defined frame tag. There are no restrictions on how this field is used in an application. The transmitter supplies this tag into the TX_FRAME_TAG_UDATA.FRAME_TAG bits for data frames. Ping frames use the tag defined in TX_PING_TAG.TAG. The receiver can access the received frame tag in RX_FRAME_TAG_UDATA.FRAME_TAG.
- **End of Frame:** The end of frame contains four clock edges with four bits, 0110, transmitted on the data lines.
- **Postamble:** The postamble contains four additional clock edges with the data lines held in the high state. After the postamble, the clock and data lines are driven high (inactive state). This phase is not present in FSI-SPI compatibility mode.

12.4.5.4.4.2 Frame Types

The FSI hardware can generate and handle many predefined frame types. The different frame types can be used by the application to signal different types of events or convey different information to the receiver. The different frame types influence which phases and data fields to include in the transmitted frames.

Table 12-422 provides a short overview of the different frame types used by the FSI. Each frame type is described in more detail in the following subsections.

Table 12-434. Frame Types and the 4-bit Codes

Frame Type	4-bit Frame Code	Description
PING	0000	Used typically for checking line integrity. A ping frame can be sent either by software or automatically by hardware.
ERROR	1111	Used typically during error conditions or any condition where one side wants to signal the other side for attention. However, the user software can use an error frame for any purpose.
DATA_1_WORD	0100	1 word data packet (16 bits of data)
DATA_2_WORD	0101	2 word data packet (32 bits of data)
DATA_4_WORD	0110	4 word data packet (64 bits of data)
DATA_6_WORD	0111	6 word data packet (96 bits of data)
DATA_N_WORD	0011	N(1-16) word data packet where software has programmed the number of the data words in a designated register. Both transmitter and receiver modules must have the same value programmed.
Reserved	0001, 0010, and 1000-1110	Reserved

12.4.5.4.4.2.1 Ping Frames

Ping frames are one of the most basic frames that can be generated by the FSI. Table 12-423 shows the structure of the ping frames.

Table 12-435. Ping Frame

Idle State	Preamble	SOF	Frame Type	Frame Tag	EOF	Postamble	Idle State
	1111	1001	0000	xxxx	0110	1111	

The ping frame type is always 0000. The frame tag is defined by the application. Separate frame tags exist for timer and software initiated ping frames. No data or CRC is transmitted in a ping frame.

The main purpose of the ping frame is to periodically send a notification to the receiver to make sure an active connection between the transmitter and receiver. The transmitter and receiver cores implement different features to allow the ping frame to operate as a line break detect feature.

On the transmitter, the ping frame is the only frame that can be set up and transmitted without any further software or DMA intervention. Ping frames can be transmitted by any (or all) of the three sources: automatic ping timer, software, or external triggers. See Section 12.4.5.4.2.3.2 for information on how the transmitter configures and sends the ping frames.

The receiver has a ping watchdog that can detect if a ping frame has not been received in a predetermined window. This allows the receiver to know if the connection between the receiver and the transmitter has been broken. See Section 12.4.5.4.3.4 for information on how the receiver handles ping frames.

12.4.5.4.4.2.2 Error Frames

Error frames are similar to ping frames in that there are no data fields transmitted. Despite the naming of this frame as an “error frame,” the usage of it is up to the application, as no restrictions are placed on how and when this type of frame is transmitted. Table 12-424 shows the structure of an error frame.

Table 12-436. Error Frame

Idle State	Preamble	SOF	Frame Type	Frame Tag	EOF	Postamble	Idle State
	1111	1001	1111	xxxx	0110	1111	

The structure of the error frame is the same as a ping frame. No data or CRC values are transmitted. The frame type is 1111 for all error frames, and the frame tag is defined by software in the TX_FRAME_TAG_UDATA register.

The receiver can detect if an error frame has been received based on the frame type field. Because of this, the receiver can read the incoming frame tag from the RX_FRAME_TAG_UDATA register and act on up to 16 different conditions.

12.4.5.4.4.2.3 Data Frames

Data frames are the most complex frames. As the name indicates, these frames are used to transfer data. Table 12-425 shows the general structure of data frames.

Table 12-437. Data Frame

Idle State	Preamble	SOF	Frame Type	User Data	Data Words	CRC Byte	Frame Tag	EOF	Postamble	Idle State
	1111	1001	0xxx	xxxx xxxx	1-16 words	xxxx xxxx	xxxx	0110	1111	

The frame type field reflects the 4-bit code of the frame type. A list of frame types can be seen in Table 12-422. The number of the data words transmitted is determined by the frame type chosen.

There are four fixed-length data frames supported by the frame type: 1 word, 2 words, 4 words, and 6 words.

Additionally, there is a user-defined data length frame type where the number of data words is fixed by software. Anywhere from 1 to 16 words can be transmitted in this frame type. This length must be configured in the N_WORDS field of the transmitter’s TX_FRAME_CTRL register and receiver’s RX_OPER_CTRL register.

12.4.5.4.4.3 Multi-Lane Transmission

The FSI is capable of transmitting and receiving data on two parallel data lines. When enabled, data bits are split between the data lines while the start of frame, frame type, frame tag, and end of frame fields are identical and complete on each line. The user data, data, and CRC fields are split between the data lines. Starting with the most-significant bit, the odd-numbered bits appear on D0 and even-numbered bits appear on D1.

In the following example, assume the following:

8-bit user data: u7u6u5u4u3u2u1u0

16-bit data: d15d14d13d12…d1d0

8-bit CRC: c7c6c5c4c3c2c1c0

Table 12-438. Multi-Lane Frame Format

Idle State	Preamble	SOF	Frame Type	User Data	Data Words	CRC Byte	Frame Tag	EOF	Postamble	Idle State
TXD0	1111	1001	0011	$u^7u^5u^3u^1$	$d^{15}d^{13}\ldots d^1$	$c^7c^5c^3c^1$	xxxx	0110	1111	
TXD1	1111	1001	0011	$u^6u^4u^2u^0$	$d^{14}d^{12}\ldots d^0$	$c^6c^4c^2c^0$	xxxx	0110	1111	

12.4.5.4.5 Flush Sequence

Every time there is a soft reset of the receiver, the receiver requires a flush sequence from the transmitter before the receiver can receive and decode frames. The receiver core has an asynchronous reset mechanism that allows the receive module to be reset even in the absence of the receive clocks. However, due to the design, this reset is released synchronous to the receive clock (RXCLK). Thus, the receiver requires five full clock pulses to be able to come out of reset. Sending the flush pattern makes sure that these clock edges are received and any subsequent frames sent to the receiver are correctly interpreted.

The flush sequence consists of a single toggle on both of the data lines as well as five consecutive pulses on the clock line.

If the FSI receiver is receiving data from a standard SPI, a data word of 0xFFFF from the SPI has the same effect as a flush sequence.

Figure 12-399 shows a sample plot of the flush sequence.

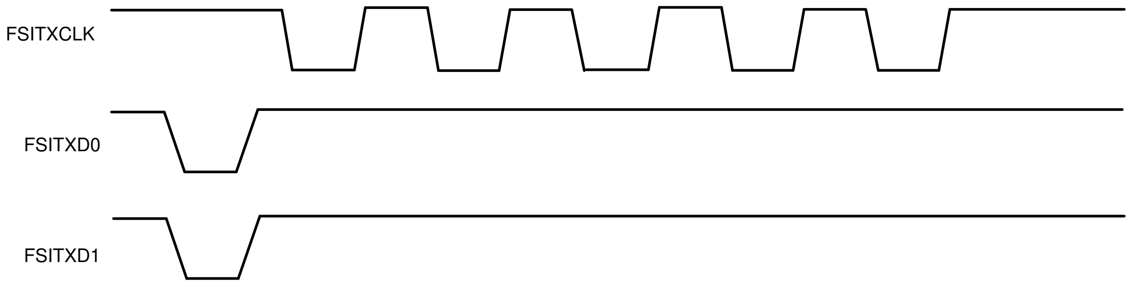

Figure 12-399. Flush Sequence Signals

12.4.5.4.6 Internal Loopback

The transmitter and receiver cores can be connected together internally to allow for development and debug. This is achieved by setting RX_MASTER_CTRL.INT_LOOPBACK to 1. Internal loopback will route the signals from the corresponding transmitter to the appropriate receiver pin. No configuration needs to be done in the transmitter.

Figure 12-400 shows the signal connections with internal loopback.

In this device, there are two FSI transmitter cores (FSI_TX0 and FSI_TX1), and six receiver cores (FSI_RX0, FSI_RX1, FSI_RX2, FSI_RX3, FSI_RX4, FSI_RX5, FSI_RX6). When using loopback mode, FSI_TX0 can be used in the loopback mode with FSI_RX0, FSI_RX1, and FSI_RX2 . At the same time, FSI_TX1 can be used in loopback mode with FSI_RX3, FSI_RX4, and FSI_RX5.

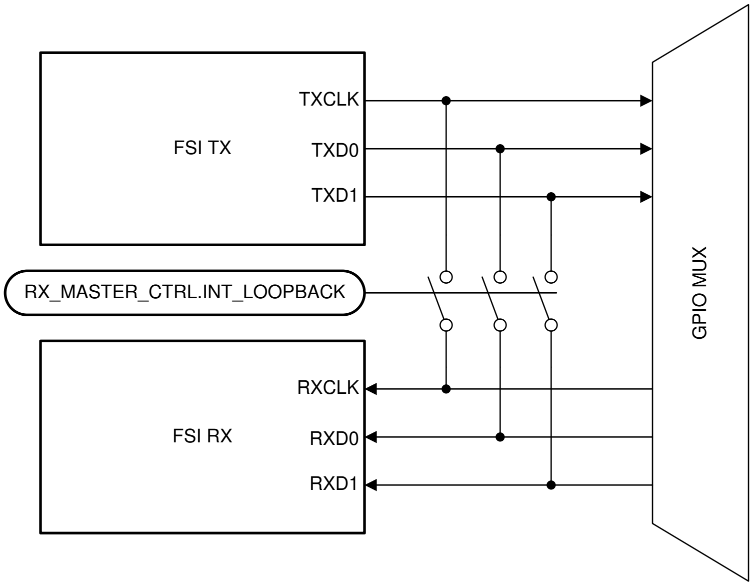

Figure 12-400. FSI with Internal Loopback

12.4.5.4.7 CRC Generation

The FSI uses CRC-8 with the polynomial 0x07 for the internal hardware CRC generation. This polynomial is also represented as x^8+x^2+x+1.

For example, for a 2-word data packet the following calculation occurs:

Data-1 = 0x4433

Data-0 = 0x2211

User Data = 0xAA

The CRC is computed with the bytes being taken in the following order (first to last):

0xAA – Byte 0, User Data

0x11 – Byte 1, Data-0, Least-significant byte

0x22 – Byte 2, Data-0, Most-significant byte

0x33 – Byte 3, Data-1, Least-significant byte

0x44 – Byte 4, Data-1, Most-significant byte

12.4.5.4.8 ECC Module

The FSI module comes with a 16-bit or 32-bit ECC computation module in both the transmitter and receiver. Use of this module is optional.

Note that the ECC is independent and unrelated to the hardware CRC computation module present in both the transmitter and receiver cores.

The following example shows a scenario in which the application requires ECC be calculated and transmitted on a 2-word data frame.

In the FSITX module:

1. Configure the ECC module for 32-bit data by setting TX_OPER_CTRL_HI.ECC_SEL to 1.
2. Write the data to the TX_ECC_DATA register as well as the transmit buffer.
3. Read TX_ECC_VAL Register. This register contains the 8-bit ECC value calculated on the data.
4. Copy the 8-bit data from TX_ECC_VAL to TX_FRAME_TAG_UDATA.USER_DATA.
5. Set the Start Condition to begin the transmission.

The reverse process is followed on the FSIRX module. Once the data frame is received, user software can do the following:

1. Copy the data from the receive buffer to the RX_ECC_DATA register.
2. Copy the received user data that contains the transmitted ECC value from RX_FRAME_TAG_UDATA.USER_DATA to the RX_ECC_VAL register.
3. Read the RX_ECC_LOG register. This contains the result of the ECC computation using the RX_ECC_DATA and RX_ECC_VAL registers.
    a. If no ECC errors were detected, RX_ECC_LOG is 0. The correct data is available in RX_ECC_SEC_DATA.
    b. If a single bit error was detected, RX_ECC_LOG.SBE is 1. The autocorrected data is available in RX_ECC_SEC_DATA.
    c. If multiple bit errors occurred, RX_ECC_LOG.MBE is 1. The data in RX_ECC_SEC_DATA is invalid and must not be used.

Using a 2-word data frame plus using the user data for the ECC is one possible implementation for ECC detection. Another option is to use a larger data frame a allocate one of the data words to be the ECC value.

12.4.5.4.9 FSI-SPI Compatibility Mode

The FSI supports a SPI compatibility mode. While the FSI can communicate with a standard SPI module, the FSI supports a limited configuration. The features of this compatibility mode are:

- Data transmits on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 is driven like an active-low, chip-select signal. The signal is low for the duration for the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks are transmitted. All signals return to the IDLE state after the frame phase is finished.
- It is not possible to transmit in the SPI peripheral configuration because the FSI TXCLK cannot take an external clock source.

Table 12-427 lists the frame structure of the FSI-SPI compatibility mode. Each frame phase is present in this mode. If the FSI is transmitting to a standard SPI module, the SPI must decode the frame structure. Similarly, if the FSI is configured as a SPI peripheral, the standard SPI must encode the transmission to be sent.

Table 12-439. FSI-SPI Compatibility Frame Structure

Idle State	Start of Frame	Frame Type	User Data	Data Words	CRC byte(1)	Frame Tag	End of Frame	Idle State
	1001	4 bits	8 bits	1-16 words	8 bits	4 bits	0110	

(1) The CRC byte is present only in data frames.

Because of the requirement that the standard SPI module encodes the various frame data, this limits the type of modules that can be connected to the FSI in SPI mode. The paired SPI module must have enough functionality to encode and decode the frames.

If the FSI is transmitted to a standard 16-bit SPI, the data is arranged in the following manner. The example provided in Table 12-428 assumes a DATA_2_WORD frame has been sent.

Table 12-440. Contents of Data Received by a Standard SPI

SPI Data	Data Contents
SPI word 0	1001, 0100, 8-bit User Data
SPI word 1	Data word 1
SPI word 2	Data word 2
SPI word 3	8-bit CRC, 4-bit Frame Tag, 0110

12.4.5.4.9.1 Available SPI Modes

There are a few wiring schemes available for the FSI to use when communicating with an SPI module.

12.4.5.4.9.1.1 FSITX as SPI Controller, Transmit Only

The FSITX can operate as an independent SPI controller module. In this condition, TXCLK is connected to SPICLK, TXD0 is connected to SPIPICO, and TXD1 is connected to $\overline{\text{SPIPTE}}$, the chip select.

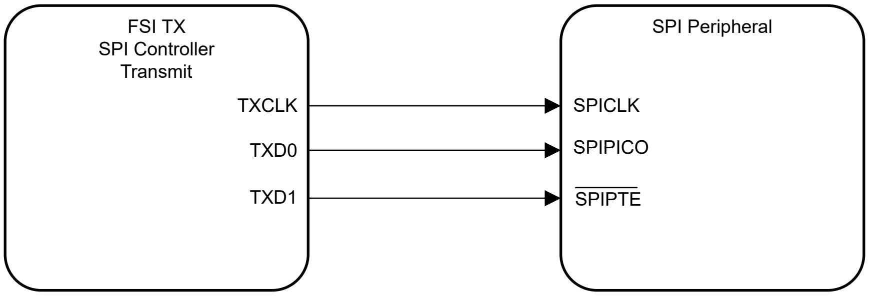

Figure 12-401. FSITX as SPI Controller, Transmit Only

When the FSI is an SPI transmitter, the application has the ability to check for frame errors, line breaks, CRC errors, and ECC checks on data. These are all encoded by hardware in every FSI frame. The SPI receiver requires some software to act upon this information.

Table 12-441. FSI as Controller Transmitter, SPI as Peripheral Receiver

Capability	Availability	Comment
Framing checks on the data frames	Yes	Can be implemented in software on the SPI receiver.
Ability to detect line breaks	Yes	Can be implemented in software on the SPI receiver but requires additional software overhead such as a timer or watchdog.
CRC check	Yes	Can be implemented in software on the SPI receiver. For devices that have MCRC, this is more efficient.
ECC on data	Yes	Can be implemented in software on the SPI receiver
Detection of abruptly terminated frames	No	
Double edge data rate	No	
Recovery from glitches on signal lines between frames	No	
Skew adjustment on signal lines	No	

12.4.5.4.9.1.1.1 Initialization

To configure the FSITX module to be an SPI controllercontroller for transmit only, proceed through the standard FSITX initialization procedure. Before releasing the FSITX from reset, set TX_OPER_CTRL_LO.SPI_MODE to 1. This enables the SPI clocking scheme and signaling structure.

12.4.5.4.9.1.1.2 Operation

The operation of the FSITX module in FSI-SPI Compatibility mode is the same as if the module is in standard FSI mode. The application can utilize the frame timer, ping frames, external frame triggers, and so on. Refer to Section 12.4.5.4.2 for more information on each of these features.

12.4.5.4.9.1.2 FSIRX as SPI Peripheral, Receive Only

The FSIRX can operate as an independent SPI peripheral module. In this usage, RXCLK is connected to SPICLK and RXD0 is connected to SPIPICO. RXD1 is unused. There is no requirement for a chip select signal to be used when connected to the FSIRX. This is because the FSIRX responds to any incoming clock edge. If there is any noise or unwanted clock transitions, a flush sequence is required to resynchronize the FSIRX module with the controller.

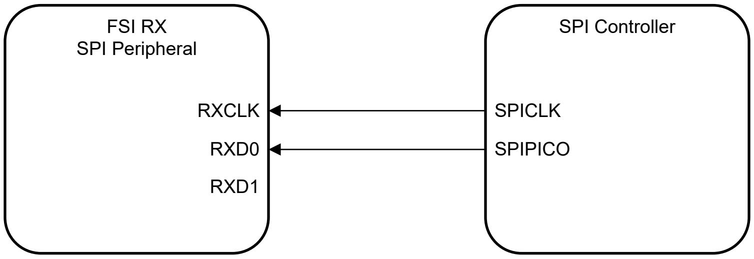

Figure 12-402. FSIRX as SPI Peripheral, Receive Only

When the FSI is an SPI receiver communicating with an SPI transmitter, the application has the ability to detect frame errors, line breaks, CRC errors, ECC checks on data, as well as abruptly terminated frames. Note that the FSI can handle all of this in hardware, but the SPI transmitter must encode the information into the data to be transmitted.

Table 12-442. SPI as Controller Transmitter, FSI as Peripheral Receiver

Capability	Availability	Comment
Framing checks on the data frames	Yes	Standard on FSI
Ability to detect line breaks	Yes	Can be implemented in software on the SPI transmitter but requires the use of a timer or watchdog in the transmitting SPI device.
CRC check	Yes	Can be implemented in software on the SPI transmitter.
ECC on data	Yes	Can be implemented in software on the SPI transmitter.
Detection of abruptly terminated frames	Yes	This is accomplished with the FSI setting up the frame watchdog counter.
Double edge data rate	No	
Recovery from glitches on signal lines between frames	Yes	Whenever glitches occur on either the clock or data lines in between transmissions, the initial flush pattern of a frame discards the effects of these glitches and causes the receiver to resynchronize when the real “start-of-frame” pattern is seen. So, the ability to reject glitches in between frames is very high.
Skew adjustment on signal lines	Yes	The FSI receiver has the ability to add delays to the incoming signal lines.

12.4.5.4.9.1.2.1 Initialization

To configure the FSIRX module to be an SPI peripheralperipheral for receiving only, proceed through the standard FSIRX initialization procedure. Before releasing the FSIRX from reset, set RX_OPER_CTRL.SPI_MODE to 1. This enables the SPI clocking scheme and signaling structure.

12.4.5.4.9.1.2.2 Operation

The operation of the FSIRX module in FSI-SPI compatibility mode is the same as if the module is in standard FSI mode. The application can utilize the Frame and Ping Watchdogs, CRC and ECC checks, and so on. Refer to Section 12.4.5.4.3 for more information on each of these features.

12.4.5.4.9.1.3 FSITX and FSIRX Emulating a Full Duplex SPI Controller

In this configuration, the FSITX is the controller clock. The FSITX module drives TXCLK (SPICLK), TXD0 (SPIPICO), and TXD1 (SPISTE/chip select) to the SPI peripheral. The SPIPOCI signal is connected back to the RXD0 signal. RXCLK can be applied either using the internal SPI pairing feature or externally wired, depending on the application requirements. Since the FSITX and RX modules are independent, the FSIRX can also be thought of as an additional SPI peripheral. Some software logic is required for the FSI to emulate an SPI controller fully.

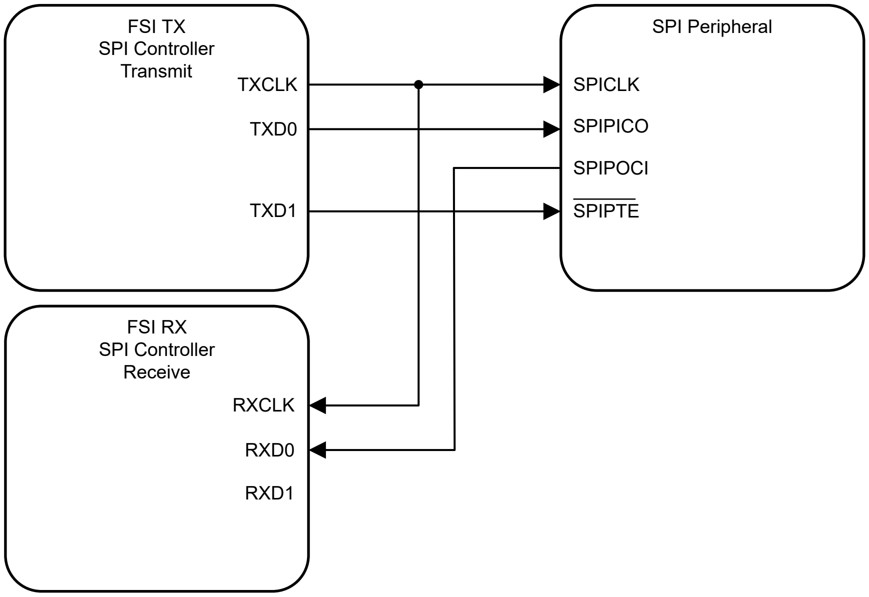

Figure 12-403. FSITX and FSIRX as SPI Controller, Full Duplex

12.4.5.4.9.1.3.1 Initialization

To configure both FSITX and RX modules for full duplex SPI controllercontroller operation, follow the initialization instructions for each module described in the preceding sections. Both FSITX and RX modules must set the respective SPI_MODE bits. This enables the SPI clocking scheme and signaling structures.

If internal clock loopback is desired, the FSIRX module must also set RX_MAIN_CTRL.SPI_PAIRINGRX_MASTER_CTRL.SPI_PAIRING to 1. This internally connects TXCLK to RXCLK. If using internal clock loopback, the GPIO used for RXCLK can be reallocated to other application requirements.

If the application requires an external clock loopback, make sure that TXCLK is connected to RXCLK. This is required if the SPI peripheralperipheral is across an isolation barrier and there is latency between TXCLK being launched and SPIPOCISPISOMI data being received on RXD0.

12.4.5.4.9.1.3.2 Operation

In this mode of operation, some higher level software must be written to emulate a full SPI controller module. There is no path for the transmit module to determine what the receive module received. Both the TX and RX modules are still able to utilize the various other features available, such as the ping frame timer, ping frame and frame watchdogs, CRC and ECC error checkers, and so on. The procedure for configuring these features is described elsewhere in this document.

12.4.5.5 FSI Programing Guide

This section describes various operational sequences and features for the FSI.

12.4.5.5.1 Establishing the Communication Link

Once the transmitter and receiver modules have been configured, some synchronization must occur before the modules exchange data. Since the receiver accepts data on any clock transition, the receiver core logic must be flushed to properly interpret the start of a new, valid frame. This is especially true when the FSI modules reside on separate devices and are possibly isolated.

The following example provides a suggested approach for establishing a clean communication link on two separate devices that power up in an arbitrary order. Note that this is only a sample synchronization. Depending on application requirements, a different approach can be followed. The single, most important aspect of synchronization is to make sure that the receiver is properly flushed and ready to receive a complete frame without error. How to achieve this is up to the application.

Figure 12-404 shows the connection of the devices in this example. While there is no true concept of a main device or a remote device node in the FSI protocol, the example uses this nomenclature as a simple way to describe the data flow.

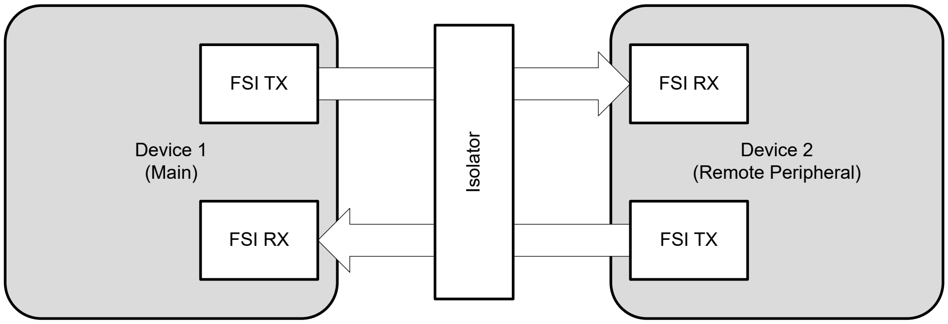

Figure 12-404. Point to Point Connection

Device 1 is the main node; it is the driver of the initialization sequence. Device 2 is the remote node; it responds to the main device commands. In this example, as well as in a real world use-case, neither the main device nor the remote device knows precisely when the other is ready to receive communication.

Sample sequences for both the main device and remote device are provided in the following subsections.

12.4.5.5.1.1 Establishing the Communication Link from the Main Device

The following sequence is an example of how the main device node establishes the communication link with the remote device without external signals outside of the standard communication link.

1. Assert the core reset to both the FSITX and FSIRX modules, and then deassert the resets.
2. Configure the transmitter and receiver for desired operation.
3. Set up the receiver interrupts to detect an incoming transmission.
4. Begin the ping loop:
    - Send the flush sequence.
    - Send a ping frame with the frame tag 0000.
    - Wait for some time. (determined by application)
    - If the FSIRX has received a valid ping frame, continue; else, iterate the loop again.
    - If the received ping frame tag was 0001, continue; else, iterate the loop again.
5. Send a ping frame with the frame tag 0001.

At this point, both the main transmit and receive channels have successfully received a frame from the remote counterparts. The link has been established and standard application communication can begin.

12.4.5.5.1.2 Establishing the Communication Link from the Remote Device

The following sequence is an example of how the remote device node establishes the communication link with the main device without external signals outside of the standard communication link.

1. Apply the core reset to both the FSITX and FSIRX modules, and then release the reset.
2. Configure the transmitter and receiver for desired operation.
3. Set up the receiver interrupts to detect an incoming transmission.
4. Wait for a receiver interrupt.
5. If the FSIRX has received a valid ping frame, continue; else, return to step 4.
6. If the received frame tag was 0000, continue; else, discard the transmission and return to step 4.
7. Send the flush sequence.
8. Send a ping frame with the frame tag 0001.
9. Wait for a receiver interrupt.
10. If the FSIRX has received a valid ping frame, continue; else, return to step 4.
11. If the received ping frame tag was 0001, continue; else, if the received frame tag was 0000, return to step 9. This can happen if a second ping frame was already in transit before receiving the remote device response in step 8.

At this point, both the transmit and receive modules have successfully received ping frames from the main counterparts. The link has been established and regular communication can now proceed. The application can configure periodic ping frames from the transmitter, initialize the receiver ping and frame watchdogs, and begin the communication required by the application.

12.4.5.5.2 Register Protection

Both the FSITX and FSIRX modules contain control registers that have embedded write protection. This is accomplished through register keys and a controller register lock. These protections ensure that no spurious writes or unintentional modifications to these registers are accepted. Refer to FSITX and FSIRX Registers for the register and bit descriptions to find the list of registers with write protections available.

Register Key Protection

In addition to EALLOW, some bits in the FSI registers are protected by a key. In order to write to these bits, the key must be written at the same time. For example, to put the transmitter core into reset, TX_controller_CTRL.CORE_RST must be set. To do this, write 0xA501 to TX_MASTER_CTRL, where 0xA500 is the KEY value, and 0x0001 is the CORE_RESET bit. Refer to the register descriptions for more information on which registers have write keys added.

Control Register Lock Protection

There also exists a controller lock to prevent any modifications to the control registers. There is an independent lock for each FSI module. For the list of registers that are protected by this control register lock, refer to the register descriptions section. The control register lock will prevent any writes to the control registers until the lock is released. To set the control register lock, write 0xA501 to RX_LOCK_CTRL and TX_LOCK_CTRL for the receiver and transmitter respectively.

The control register lock cannot be disabled by the application until a SYSRSn has been asserted. This can occur at the device level, or by writing to the appropriate peripheral soft reset register (DEV_CFG_REGS.SOFTPRESx) for the FSI module. Refer to Section 12.4.5.4.2.7 for more information on SYSRSn.

12.4.5.5.3 Emulation Mode

There is no specific emulation mode or configuration supported. The FSI cores are always in free running mode. CPU halts do not have any effect on the operation of the FSI. Reads of registers and data buffers by the debugger do not affect any flags or status of the data buffers.

If you want to stop the operation of either FSI module when the debugger halts, the following steps are required:

1. Set the debugger to real-time emulation mode.
2. Mark the FSI interrupt group as a time-critical interrupt. That is, enable the corresponding bit in the DBGIER register.
3. The ISR can check the DSTAT register and to determine if the ISR was called when the debugger was halted.
4. FSI operations can be disabled and the ISR can branch to a debug-specific halt location.

12.5 Timer Modules

This section describes the timer modules in the device.

12.5.1 Global Timebase Counter (GTC)

This section describes the global timebase counter (GTC) in the device.

12.5.1.1 Global Timebase Counter (GTC)

This section describes the Global Timebase Counter (GTC) in the device.

12.5.1.1.1 GTC Overview

The GTC module provides a continuous running counter that can be used for time synchronization and debug trace time stamping.

The device includes one GTC instance. Table 12-431 shows GTC allocation across device domains.

Table 12-443. GTC Allocation Across Device Domains

Module Instance	Domain	
	MCU	MAIN
GTC0	–	✓

12.5.1.1.1.1 GTC Features

The GTC supports the following features:

- 64-bit up counter
- No rollover during the lifetime of the device
- Compatible with ARMv8 system counter requirements:
  - Disabled at power-up
  - Register definition and memory map aligned to ARMv8 definition
  - Implements memory-mapped counter control and status frames
- Outputs reflected binary (Gray) encoded timer value for system timer bus distribution to other modules
- Selectable counter bit output as a push event that can be used by CPTS modules, timers or interface protocols

12.5.1.1.1.2 GTC Not Supported Features

The GTC module does *not* support:

- System counter frequency change for reduced power operation
- ARMv8 memory-mapped timer
- Register write locks (MMR kick protection)

12.5.1.1.2 GTC Integration

This section describes the GTC integration in the device, including information about clocks, resets, and hardware requests.

Figure 12-405 shows the GTC integration.

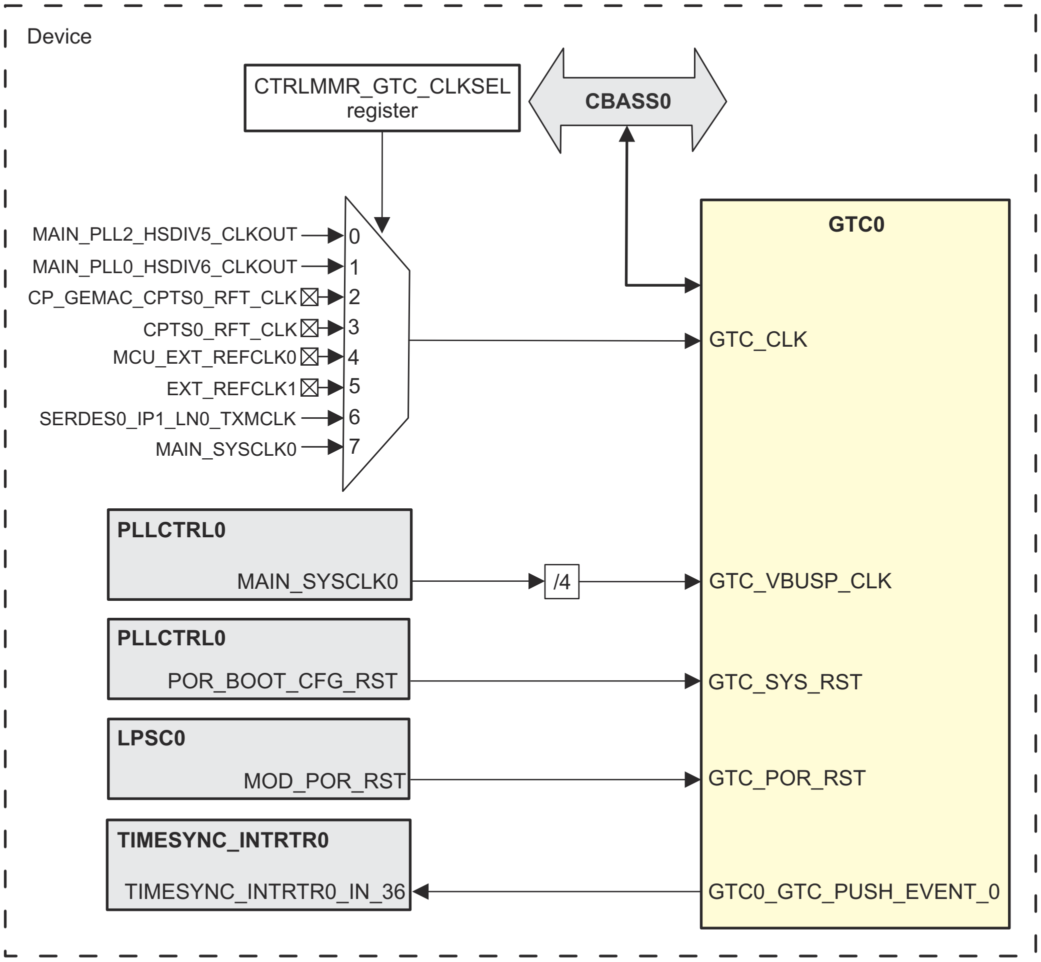

Figure 12-405. GTC Integration

Table 12-432 through Table 12-435 summarize the GTC integration.

Table 12-444. GTC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
GTC0	PSC0	PD0	LPSC0	CBASS0

Table 12-445. GTC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
GTC0	GTC_CLK	MAIN_PLL2_HSDIV5_CLKOUT[(1)]	PLL2	Module functional (counter) clock. Source clock selection is done through a mux which is controlled via CTRLMMR_GTC_CLKSEL[2-0] CLK_SEL register bit field.
		MAIN_PLL0_HSDIV6_CLKOUT	PLL0	
		CP_GEMAC_CPTS0_RFT_CLK	I/O pin	
		CPTS0_RFT_CLK	I/O pin	

Table 12-445. GTC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		SERDES0_IP1_LN0_TXMCLK	SERDES0, IP1, lane 0	
		MAIN_SYSCLK0	PLLCTRL0	
GTC0	GTC_VBUSP_CLK	MAIN_SYSCLK0/4	PLLCTRL0	Module interface clock.

(1) Default source.

Table 12-446. GTC Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
GTC0	GTC_POR_RST	MOD_POR_RST	LPSC0	Module reset. Affects counter and MMR logic.
	GTC_SYS_RST	POR_BOOT_CFG_RST	PLLCTRL0	POR that is unstretched and not delayed by any sequential logic. Used for boot config to sample device pins.

Table 12-447. GTC Hardware Time Sync Events

Module Instance	Module Sync Output	Destination Sync Input	Destination	Description	Type
GTC0	GTC0_GTC_PUSH_EVENT_0	TIMESYNC_INTRTR0_IN_36	TIMESYNC_INTRTR0	GTC hardware push event	Pulse

12.5.1.2 GTC Functional Description

12.5.1.2.1 GTC Block Diagram

The GTC is essentially comprised of a 64-bit up counter, a Gray encoder, a 64-bit multiplexer, and memory-mapped control registers. Figure 12-406 shows a high-level block diagram of the GTC.

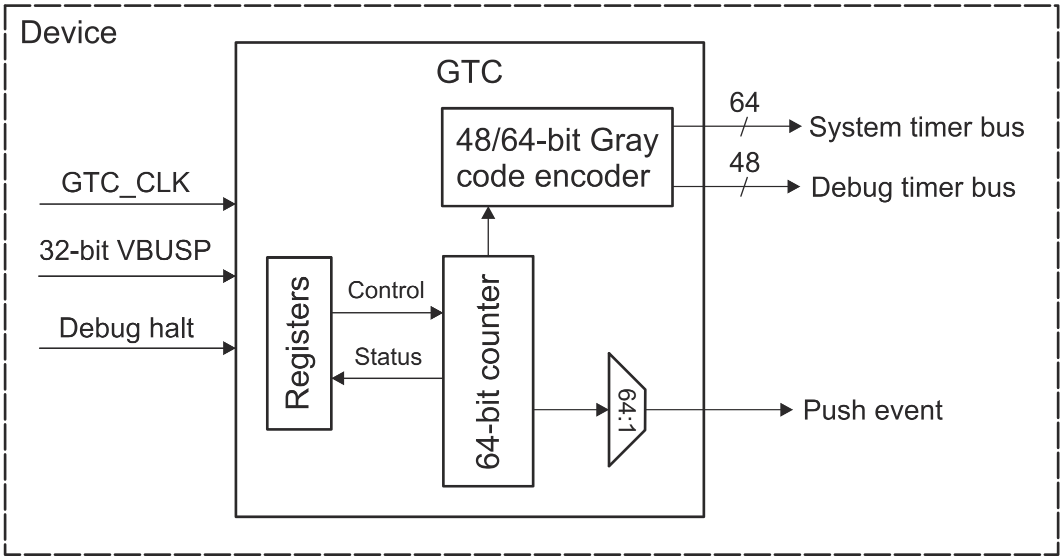

Figure 12-406. GTC Block Diagram

12.5.1.2.2 GTC Counter

The counter is a 64-bit binary up counter that increments on every GTC_CLK rising edge. The source for GTC_CLK is selected through a mux which is controlled via the CTRLMMR_GTC_CLKSEL[2-0] CLK_SEL register bit field.

The counter is disabled by default (at power-on-reset) and increments only when enabled by setting the GTC_CNTCR[0] EN bit to '1'. The current counter value is readable via the combined COUNTVALUE bit field of both GTC_CNTCV_HI (upper 32 bits) and GTC_CNTCV_LO (lower 32 bits) registers.

When counting is disabled, a new counter value can be loaded via a software write to the combined COUNTVALUE bit field. In this case, when the counter gets re-enabled, it will start counting from the last value written to this field.

The counter can be optionally configured to stop incrementing when a debug halt signal is issued, by writing a '1' to the GTC_CNTCR[1] HDBG bit. This condition is indicated through the GTC_CNTSR[1] DBGH status bit.

Steps to Clear the Counter Value to Zero

1. Disable the GTC
2. Clear GTC_CNTCV_LO (First)
3. Clear GTC_CNTCV_HI (Second)
4. Enable the GTC

Once the GTC is enabled, the GTC_CNTCV_HI bit will be cleared to zero.

12.5.1.2.3 GTC Register Partitioning

The ARMv8 architecture spec requires specific system-level components, each with one or two register frames. To accommodate this, the GTC memory-mapped registers (MMRs) are divided into four separate regions (4KB each):

- Peripheral MMRs (GTC0_GTC_CFG0): This region includes standard peripheral identification registers and any other control registers not associated with the ARMv8 system timer functions.

- Counter control MMRs (GTC0_GTC_CFG1): This region includes registers that provide control over the operation of the system timer.
- Counter status MMRs (GTC0_GTC_CFG2): This region includes registers that provide a mechanism for reading the status of the system timer.
- Timer control MMRs (GTC0_GTC_CFG3): This region includes registers that identify and provide a control mechanism for memory-mapped timer implementations. For this device, no memory-mapped timers are implemented and only the minimum registers required to indicate the presence of no timers are necessary.

12.5.2 RTI-Windowed Watchdog Timer (WWDT)

This section describes the Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module in the device.

CAUTION

The RTI module shall be used to serve only as a Digital Windowed Watchdog (DWWD).

The Real Time Interrupt module provides timer functionality for operating systems and for benchmarking code. The module incorporates several counters, which define the timebases needed for scheduling in the operating system.

This module is specifically designed to fulfill the requirements for OSEK (“Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug”; “Open Systems and the Corresponding Interfaces for Automotive Electronics”) as well as OSEK/Time compliant operating systems.

The timers also provide the ability to benchmark certain areas of code by reading the counter contents at the beginning and the end of the desired code range and calculating the difference between the values.

12.5.2.1 RTI Overview

There are seven RTI modules in the device. Table 12-436 shows the RTI allocation across device domains.

Table 12-448. RTI Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
MCU_RTI0	✓	-
RTI0	-	✓
RTI1	-	✓
RTI8	-	✓
RTI9	-	✓
RTI10	-	✓
RTI11	-	✓

Instances in the MCU domain:

- MCU_RTI0 is dedicated to the MCU cluster (MCU_M4FSS0) in lockstep and when unlocked serves as a Windowed Watchdog for the first M4F CPU core in the MCU domain (MCU_M4FSS0_CORE0).

Instances in the MAIN domain: They are intended to function as a Digital Windowed Watchdog for the CPU core that they are associated with, that is:

- RTI0 is dedicated to the first A53 CPU core in the A53 cluster (A53SS0_CORE0)
- RTI1 is dedicated to the second A53 CPU core in the A53 cluster (A53SS0_CORE1)
- RTI8 is dedicated to the first R5F CPU core in the Main domain (R5FSS0_CORE0)
- RTI9 is dedicated to the second R5F CPU core in the Main domain (R5FSS0_CORE1)
- RTI10 is dedicated to the third R5F CPU core in the Main domain (R5FSS1_CORE0)
- RTI11 is dedicated to the fourth R5F CPU core in the Main domain (R5FSS1_CORE1)

It is not intended to use an RTI that is provisioned for a particular CPU core with a different CPU core.

Figure 12-407 shows the RTI overview.

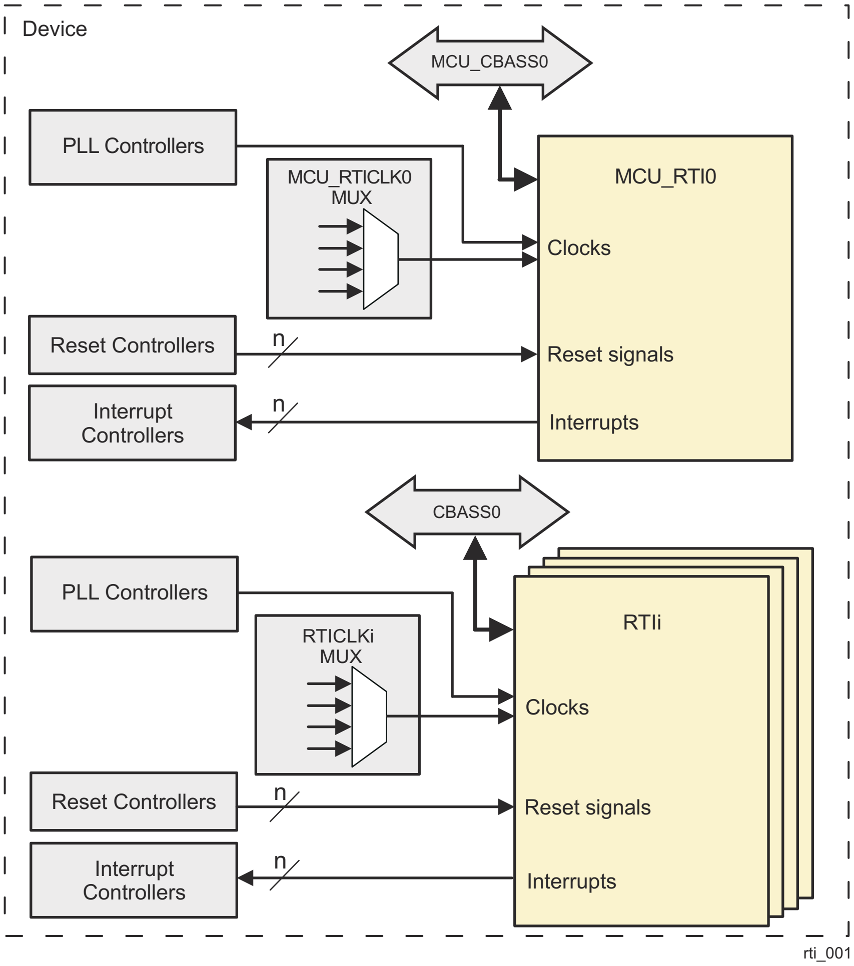

Note

i = 0, 1, 8, 9, 10, 11

Figure 12-407. RTI Overview

12.5.2.1.1 RTI Features

The RTI modules include the following main features:

- Windowed Watchdog Timer (WWDT) feature.
- Two independent 64 bit counter blocks (counter block0 or counter block1). Each block consists of
  - One 32 bit up counter
  - One 32 bit free running counter
  - Two capture registers for capturing the prescale and free running counter on a special event.
- Free running counter 0 can be incremented by either the internal prescale counter or by an external event.
- Four configurable compare registers for generating operating system ticks . Each event can be driven by either counter block0 or counter block1.
- Fast enabling/disabling of events.
- RTI clock input derived from any of the available clock sources, selectable in the System Module
- Optional capability to drive a pulse-width modulated signal out on an interrupt line.

12.5.2.1.2 RTI Not Supported Features

The following features are not supported on this family of devices:

- Real time interrupt functionality

- Analog and Digital Watchdog (DWD) Timers
- Periodic interrupt / DMA events
- Capture and compare events not used
- Counter operation is not supported and counter overflow interrupts are not used.

12.5.2.2 RTI Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

12.5.2.2.1 RTI Integration in MCU Domain

There is one RTI module integrated in the device MCU domain - MCU_RTI0. Figure 12-408 shows its integration in the device.

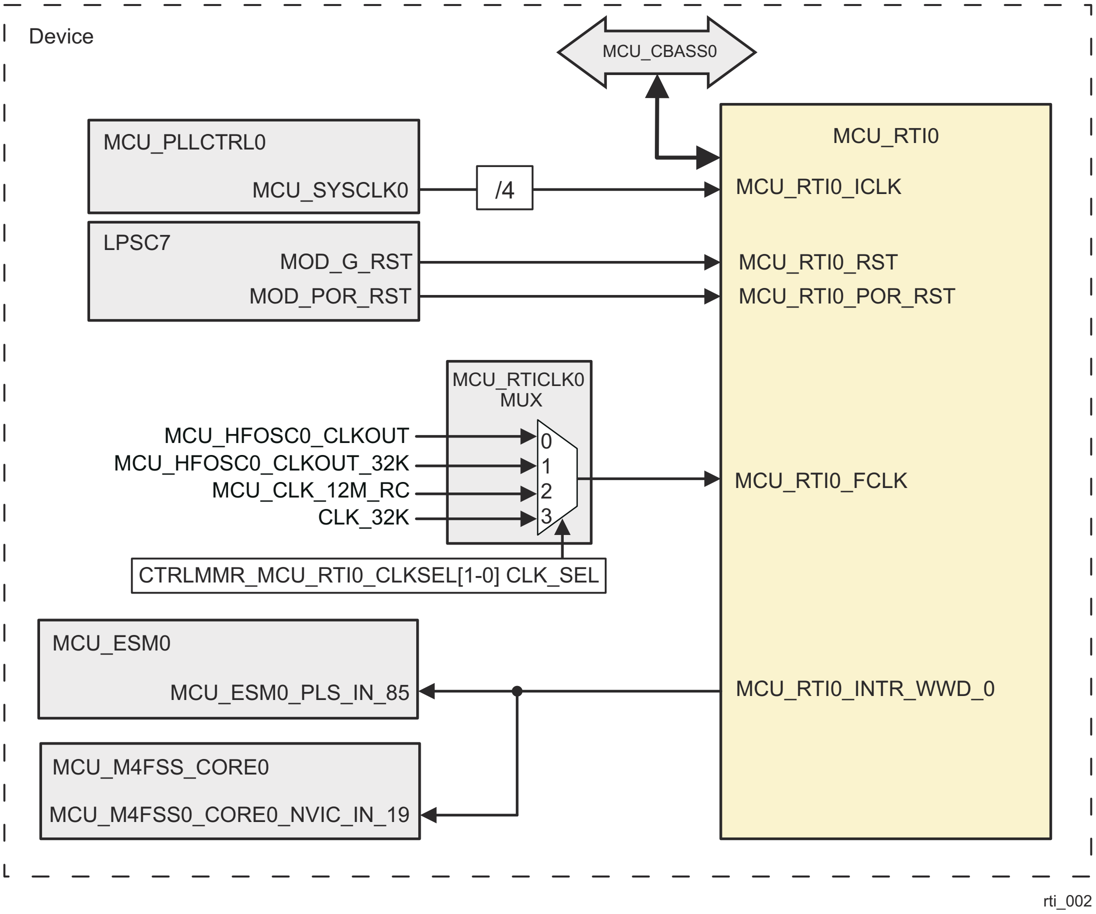

Figure 12-408. MCU_RTI Integration

Table 12-437 through Table 12-440 summarize the integration of MCU_RTI0 in device MCU domain.

The MCU_RTI0 instance is supplied by dedicated MCU_RTICLK0 clock mux.

Table 12-449. MCU_RTI Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_RTI0	MCU_PSC0	PD1	LPSC7	MCU_CBASS0

Table 12-450. MCU_RTI Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_RTI0	MCU_RTI0_ICLK	MCU_SYSCLK0/6	MCU_PLLCTRL0	MCU_RTI0 Interface Clock
	MCU_RTI0_FCLK	MCU_HFOSC0_CLKOUT MCU_HFOSC0_CLKOUT_32K	MCU_HFOSC0	MCU_RTI0 Functional Clock. For more information about clock multiplexing in MCU_RTICLK0 MUX, see CTRLMMR_MCU_WWD0_CLKSEL [1-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_CLK_12M_RC	MCU_RC_OSC_12M	
		CLK_32K		

Table 12-451. MCU_RTI Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
GTC0	GTC_POR_RST	MOD_POR_RST	LPSC0	Module reset. Affects counter and MMR logic.
	GTC_SYS_RST	POR_BOOT_CFG_RST	PLLCTRL0	POR that is unstretched and not delayed by any sequential logic. Used for boot config to sample device pins.

Table 12-452. MCU_RTI Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_RTI0	MCU_RTI0_INTR_WWD_0	MCU_M4FSS0_CORE0_NVIC_IN_19	MCU_M4FSS0_CORE0	MCU_RTI0 window watchdog violation interrupt	Pulse
		MCU_ESM0_PLS_IN_85	MCU_ESM0	MCU_RTI0 window watchdog violation interrupt	Pulse

---

Note

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.5.2.2.2 RTI Integration in MAIN Domain

There are six RTI modules integrated in the device MAIN domain. Figure 12-409 shows their integration in the device.

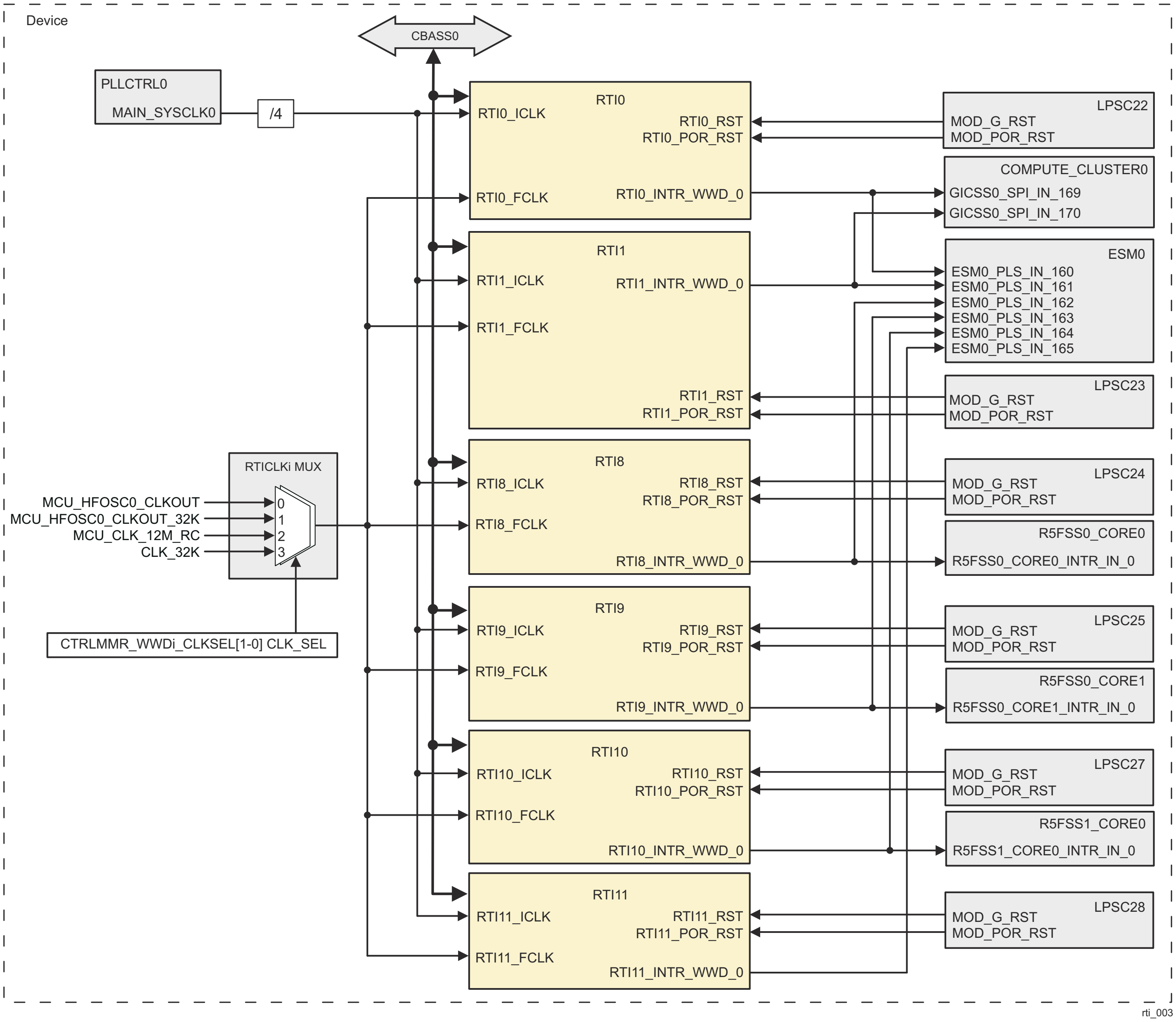

Note

i = 0, 1, 8, 9, 10, 11

Figure 12-409. RTI Integration

Table 12-441 through Table 12-444 summarize the integration of RTIi (where i = 0, 1, 8, 9, 10, 11) in device MAIN domain.

Each RTIi instance is supplied by dedicated RTICLKi mux.

Table 12-453. RTI Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
RTI0	PSC0	PD2	LPSC22	CBASS0
RTI1	PSC0	PD3	LPSC23	CBASS0
RTI8	PSC0	PD4	LPSC24	CBASS0
RTI9	PSC0	PD4	LPSC25	CBASS0
RTI10	PSC0	PD5	LPSC27	CBASS0
RTI11	PSC0	PD5	LPSC28	CBASS0

Table 12-454. RTI Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
RTI0	RTI0_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	RTI0 Interface Clock
	RTI0_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	RTI0 Functional Clock. For more information about clock multiplexing in RTICLK0 MUX, see MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL[1-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MCU_CLK_12M_RC	MCU_RC_OSC_12M	
		CLK_32K		
RTI1	RTI1_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	RTI1 Interface Clock
	RTI1_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	RTI1 Functional Clock. For more information about clock multiplexing in RTICLK1 MUX, see MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL[1-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MCU_CLK_12M_RC	MCU_RC_OSC_12M	
		CLK_32K		
RTI8	RTI8_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	RTI8 Interface Clock
	RTI8_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	RTI8 Functional Clock. For more information about clock multiplexing in RTICLK8 MUX, see MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL[1-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MCU_CLK_12M_RC	MCU_RC_OSC_12M	
		CLK_32K		
RTI9	RTI9_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	RTI9 Interface Clock
	RTI9_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	RTI9 Functional Clock. For more information about clock multiplexing in RTICLK9 MUX, see MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL[1-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MCU_CLK_12M_RC	MCU_RC_OSC_12M	
		CLK_32K		
RTI10	RTI10_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	RTI10 Interface Clock
	RTI10_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	RTI10 Functional Clock. For more information about clock multiplexing in RTICLK10 MUX, see MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL[1-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MCU_CLK_12M_RC	MCU_RC_OSC_12M	
		CLK_32K		
RTI11	RTI11_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	RTI11 Interface Clock
	RTI11_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	RTI11 Functional Clock. For more information about clock multiplexing in RTICLK11 MUX, see MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL[1-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MCU_CLK_12M_RC	MCU_RC_OSC_12M	
		CLK_32K		

Table 12-455. RTI Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
RTI0	RTI0_RST	MOD_G_RST	LPSC22	RTI0 Asynchronous Reset
	RTI0_POR_RST	MOD_POR_RST	LPSC22	RTI0 Power-On Reset
RTI1	RTI1_RST	MOD_G_RST	LPSC23	RTI1 Asynchronous Reset
	RTI1_POR_RST	MOD_POR_RST	LPSC23	RTI1 Power-On Reset
RTI8	RTI8_RST	MOD_G_RST	LPSC24	RTI8 Asynchronous Reset
	RTI8_POR_RST	MOD_POR_RST	LPSC24	RTI8 Power-On Reset
RTI9	RTI9_RST	MOD_G_RST	LPSC25	RTI9 Asynchronous Reset
	RTI9_POR_RST	MOD_POR_RST	LPSC25	RTI9 Power-On Reset
RTI10	RTI10_RST	MOD_G_RST	LPSC27	RTI10 Asynchronous Reset
	RTI10_POR_RST	MOD_POR_RST	LPSC27	RTI10 Power-On Reset
RTI11	RTI11_RST	MOD_G_RST	LPSC28	RTI11 Asynchronous Reset
	RTI11_POR_RST	MOD_POR_RST	LPSC28	RTI11 Power-On Reset

Table 12-456. RTI Hardware Requests

Interrupt Requests					
Module Instance	**Module Interrupt Signal**	**Destination Interrupt Input**	**Destination**	**Description**	**Type**
RTI0	RTI0_INTR_WWD_0	GICSS0_SPI_IN_169	COMPUTE_CLUSTER0	RTI0 window watchdog violation interrupt	Pulse
		ESM0_PLS_IN_160	ESM0		
RTI1	RTI1_INTR_WWD_0	GICSS0_SPI_IN_170	COMPUTE_CLUSTER0	RTI1 window watchdog violation interrupt	Pulse
		ESM0_PLS_IN_161	ESM0		
RTI8	RTI28_INTR_WWD_0	R5FSS0_CORE0_INTR_IN_0	R5FSS0_CORE0	RTI8 window watchdog violation interrupt	Pulse
		ESM0_PLS_IN_162	ESM0		
RTI9	RTI29_INTR_WWD_0	R5FSS0_CORE1_INTR_IN_0	R5FSS0_CORE1	RTI9 window watchdog violation interrupt	Pulse
		ESM0_PLS_IN_163	ESM0		
RTI10	RTI30_INTR_WWD_0	R5FSS1_CORE0_INTR_IN_0	R5FSS1_CORE0	RTI10 window watchdog violation interrupt	Pulse
		ESM0_PLS_IN_164	ESM0		
RTI11	RTI15_INTR_WWD_0	R5FSS1_CORE0_INTR_IN_0	R5FSS1_CORE1	RTI11 window watchdog violation interrupt	Pulse
		ESM0_PLS_IN_165	ESM0		

Note

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.5.2.3 RTI Functional Description

The MCU_RTI0 and RTIi (where i = 0, 1, 8, 9, 10, 11) modules are hereinafter referred to as RTI module.

12.5.2.3.1 RTI Digital Windowed Watchdog

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Note

Digital windowed watchdog (DWWD) timer is implemented using the digital windowed watchdog function of the RTI modules. Real time interrupt functionality is not supported. In this mode, the timer should default to disabled and user can adjust the period as desired before enabling the watchdog.

In addition to the time-out boundary configurable via the digital watchdog (DWD), some applications may also want to configure the start-time boundary of the watchdog. This is enabled by the digital windowed watchdog (DWWD) feature.

Functional Behavior

The DWWD opens a configurable time window in which the watchdog must be serviced. Any attempt to service the watchdog outside this time window, or a failure to service the watchdog in this time window, will cause the watchdog to generate either a reset or a non-maskable interrupt to the CPU. This is controlled by configuring the RTI_WWDRXNCTRL register. As stated earlier, when the watchdog needs to be enabled by software, the watchdog counter is disabled on a system reset. When the DWWD is configured to generate a non-maskable interrupt on a window violation, the watchdog counter continues to count down. The RTI_INTR_WWD interrupt handler needs to clear the watchdog violation status flag(s) and then service the watchdog by writing the correct sequence in the watchdog key RTI_WDKEY register. This service will cause the watchdog counter to get reloaded from the preload value and start counting down. If the RTI_INTR_WWD handler does not service the watchdog in time, it could count down all the way to zero and wrap around. No second exception for a time out is generated in this case.

Configuration of DWWD

The DWWD preload value (same as DWD preload) can only be configured when the DWWD counter is disabled. The window size and watchdog reaction to a violation can be configured even after the watchdog has been enabled. Any changes to the window size and watchdog reaction configurations will only take effect after the next servicing of the DWWD.

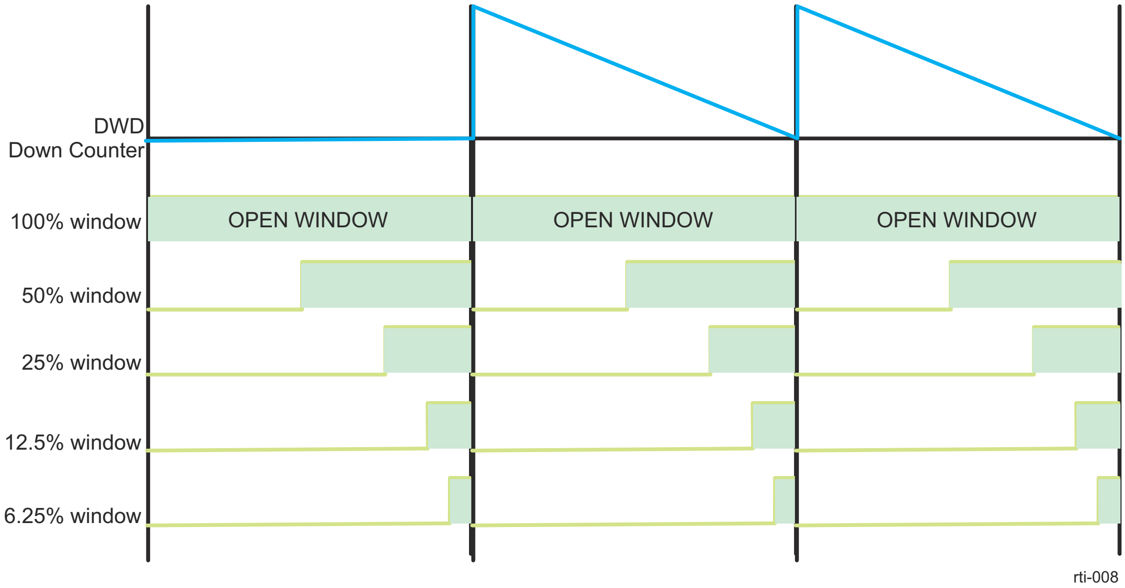

Figure 12-410. RTI Digital Windowed Watchdog Timing Example

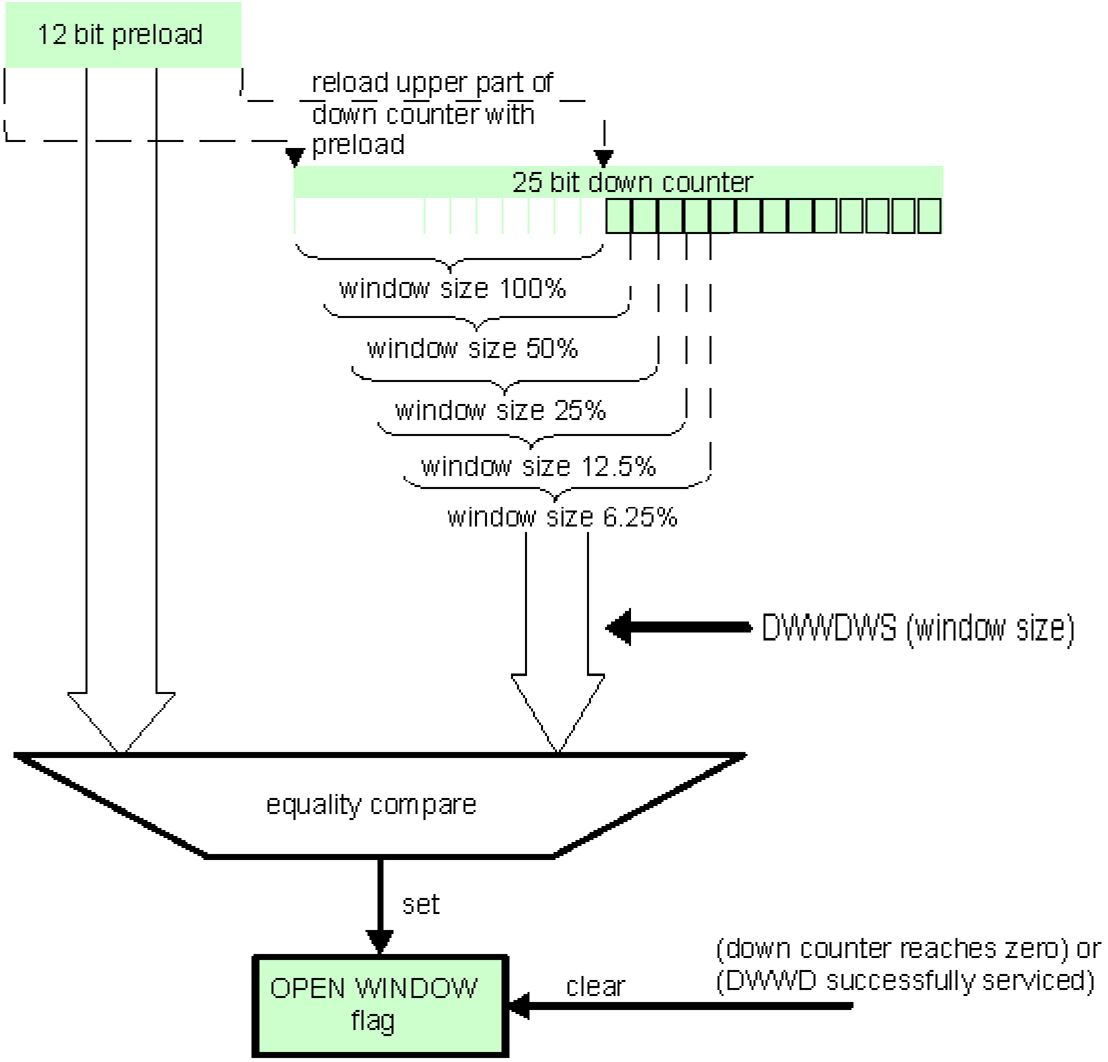

Figure 12-411. RTI Digital Windowed Watchdog Operation Block Diagram

12.5.2.3.1.1 RTI Debug Mode Behavior

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Once the system enters debug mode, the behavior of the RTI depends on the RTI_GCTRL[15] COS bit. If the bit is cleared and debug mode is active, all counters will stop operation. If the bit is set to one, all counters will be clocked normally and the RTI will work like in normal mode.

The DWD counter will not decrement in debug mode and will hold its current value, regardless of the RTI_GCTRL[15] COS bit.

Note

The user must not service the watchdog while in debug mode.

12.5.2.3.1.2 RTI Low Power Mode Operation

The operation of the RTI module is guaranteed in run, doze and snooze mode. In sleep or hibernate mode all clocks will be switched off and the RTI module will not work.

In doze and snooze modes all parts of the RTI are active, since it has to be able to wake up the device with compare and timebases interrupts. Capturing events generated by the interrupt module is also possible since in both modes the peripheral modules are able to generate interrupts, which can trigger capture events. The RTI module will generate compare and timebases interrupts. The compare interrupts will periodically wake up the device.

Note

In the special case of doze mode with DPLL off, RTI_FCLK might have a different period than with DPLL enabled, since RTI_FCLK will be derived from the oscillator output. It has to be ensured that the RTI_ICLK to RTI_FCLK ratio is at least 3:1.

The DWD/DWWD remains active when the device enters low power mode as long as the RTI_FCLK is kept active.

Whenever the LPSC that controls an RTI is in any state other than Enable (see *Module States*), the RTI cannot count or generate interrupts. For more information, see *Power Control Modules*.

During standard SoC warm reset the RTI and the rest of the SoC are reset. In this case, the RTI counters are stopped and interrupts are not issued. During reset-isolated warm reset, if an R5FSS is put in reset-isolation, then the associated RTI also becomes reset isolated. As such, the R5FSS and the RTI are not reset, but RTI stops counting and cannot generate interrupts until R5FSS is taken out of CLKSTOP (brought to Enable state).

12.5.2.3.2 RTI Digital Watchdog

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Some applications might use a digital watchdog (DWD) integrated in the RTI module. The digital watchdog generates resets after a programmable period, if no correct key sequence is written to the RTI_WDKEY register. Figure 12-412 shows the digital watchdog functional block.

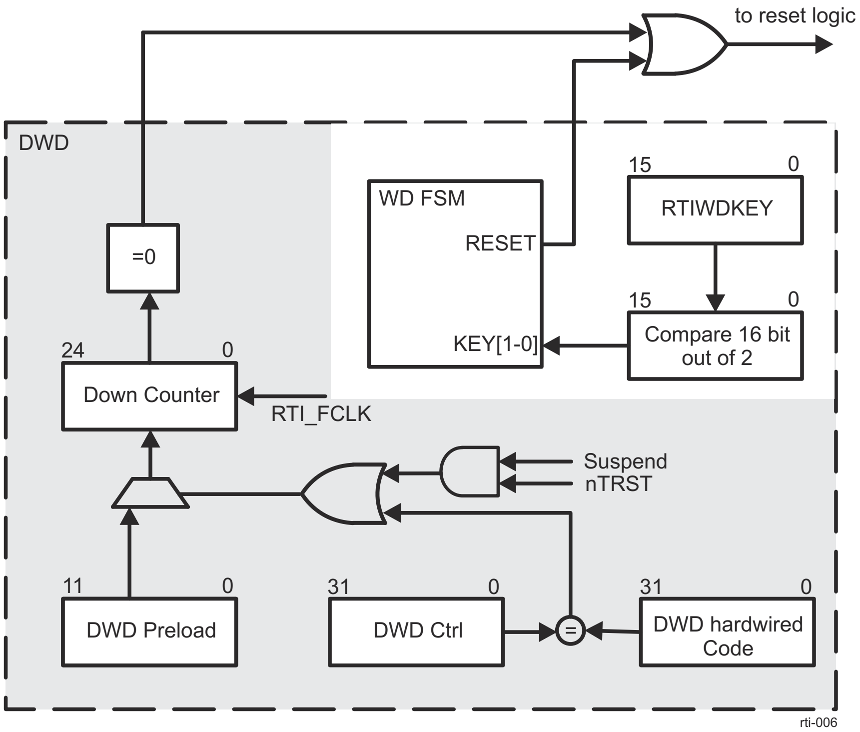

Figure 12-412. RTI Digital Watchdog Functional Block Diagram

The digital watchdog functionality is implemented such that it can be enabled by software.

The DWD starts counting down from the reset value of the RTI_DWDCNTR (DWD Counter Register). The DWD preload register can be configured at any time by the application according to the desired time-out period.

When enabled by software, the digital watchdog is disabled after system reset. If it should be used, it has to be enabled by writing A98559DAh to the RTI_DWDCTRL register. The DWD timeout period must be configured using the DWD preload register before the DWD is enabled. The DWD cannot be disabled by the application once it is enabled.

Note

When the DWD is enabled by software, any system reset will disable the DWD. This reset could have been generated by the watchdog itself.

If the correct key sequence is written to the RTI_WDKEY register (E51Ah followed by A35Ch), the 25-bit DWD Down Counter is reloaded with the 12-bit preload value stored in RTI_DWDPRLD register. If any incorrect value is written to the RTI_WDKEY register, a watchdog reset will occur immediately. A reset will also be generated, when the DWD Down Counter is decremented to 0.

The user has to take into account that the write to the RTI_WDKEY register takes 3 RTI_ICLK cycles. This needs to be considered for the DWD expiration calculation.

The DWD Down Counter will be decremented with RTI_FCLK frequency. If the RTI_FCLK is switched off via the disable registers of the Clock management, the DWD counter stops decrementing. The DWD module cannot generate a reset under this condition.

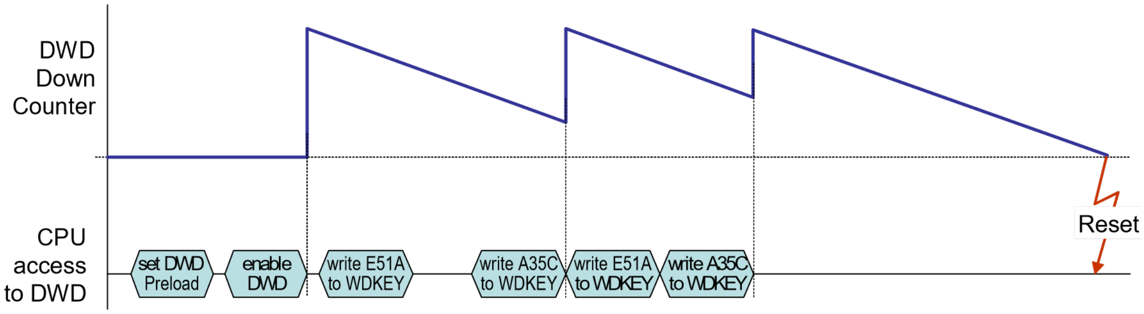

Figure 12-413. RTI Digital Watchdog Operation

The expiration time of the DWD Down Counter can be determined with following equation:

$$t_{exp} = (RTI\_DWDPRLD + 1) \times 2^{13} / RTI\_FCLK \quad (10)$$

where RTI_DWDPRLD = 0...4095

12.5.2.3.3 RTI Counter Operation

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Figure 12-414 shows the RTI module counter blocks. The RTI module supports two counter blocks.

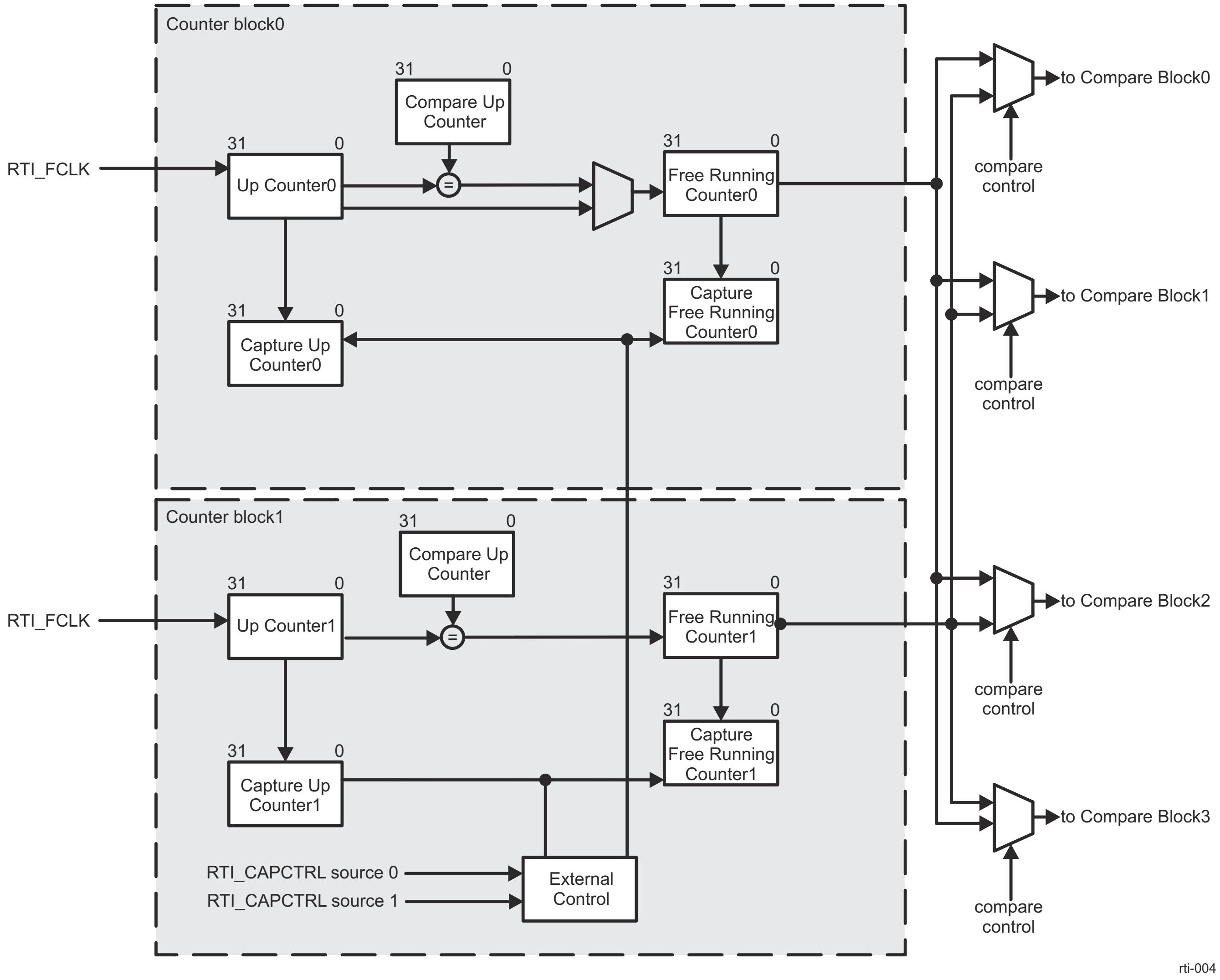

Figure 12-414. RTI Counters Block Diagram

Each block consists of two 32-bit up counters: Up Counter (UC), and Free Running Counter (FRC). The Up Counter (RTI_UC0 or RTI_UC1 register) is driven by the RTI_FCLK, and counts up until the compare value in the Compare Up Counter register (RTI_CPUC0 or RTI_CPUC1) is reached. When the compare matches, the second counter (RTI_FRC0 or RTI_FRC1 register), which is a free running counter, is incremented. At the same time UCx is reset to zero.

To ensure the consistency of the counters, when both counter values have to be determined, read the Free Running Counter first. This makes sure that at the time when the counter register is read, the Up Counter value has been stored into the counter register. The second read is then performed on the Up Counter register, which holds then the value of the counter cycle of the previous read on the Free Running Counter register.

Both blocks provide also a capture feature on external events. Two capture sources can trigger the capture event. Which event triggers block 0 or block 1 is configurable from the RTI_CAPCTRL register. The event sources come from the interrupt manager, enabling the device to generate a capture event when a peripheral module generates an interrupt. The peripheral which generates an RTI capture event is configured in the interrupt manager . When the event is detected, UCx and FRCx are stored in Capture Up Counter (RTI_CAUC0 or RTI_CAUC1) and Capture Free Running Counter (RTI_CAFRC0 or RTI_CAFRC1) registers. The read order of the captured values must be in the same order as the counter register reads. So, the CAFRCx must be read first, and then the CAUCx registers are read after the CAFRCx value has been determined. While CAFRCx is read, the CAUCx value is loaded into a shadow register to maintain data consistency, in case a capture event happens during the two reads. If the application fails to read the two registers before a second capture event happens, the previous data is overwritten.

Figure 12-415 shows the block diagram for one compare block. The RTI module supports four compare blocks.

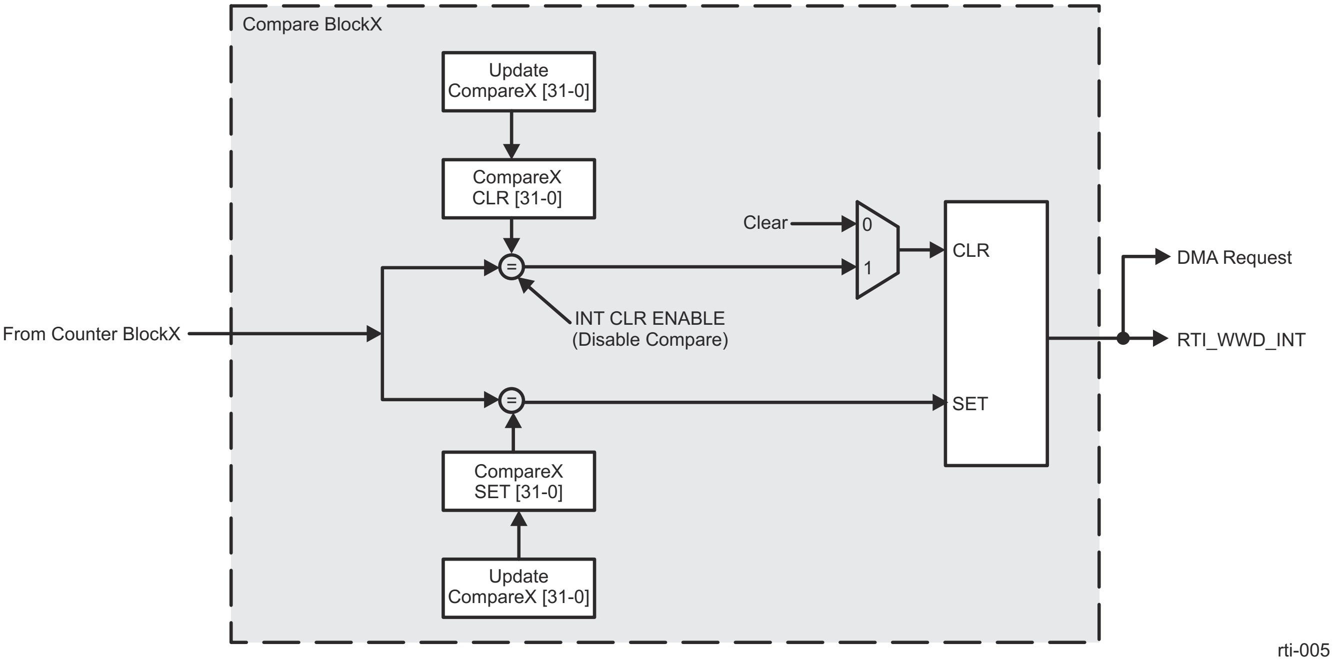

Figure 12-415. RTI Compare Block Diagram

In order to generate interrupt requests to the interrupt manager, there are four compare registers (RTI_COMP0, RTI_COMP1, RTI_COMP2, and RTI_COMP3). Each of the compare registers can be configured to work either on FRC0 (Counter block0) or FRC1 (Counter block1). When the counter value matches the compare value, an interrupt is generated. This sets an interrupt request line to the interrupt manager. The compare value gets updated automatically with the value stored in Update Compare (RTI_UDCP0, RTI_UDCP1, RTI_UDCP2, and RTI_UDCP3) registers when the compare matches. This gives the ability to generate periodic interrupts/DMA requests without having to update the compare value by software.

An optional feature allows an application to program another compare value which is then used to clear the interrupt request line. This feature is supported by four compare clear registers (RTI_COMP0CLR, RTI_COMP1CLR, RTI_COMP2CLR, and RTI_COMP3CLR). When the counter value matches the compare clear value, the interrupt line is cleared. This clears the interrupt request line to the interrupt manager. The compare clear value gets updated automatically with the value stored in Update Compare (RTI_UDCPx) registers when the compare matches.

12.5.3 Timers

This section describes the Timer modules for the device.

12.5.3.1 Timers Overview

There are sixteen timer modules in the device. Table 12-445 shows the timers allocation across device domains.

Table 12-457. Timers Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
MCU_TIMER0	✓	-
MCU_TIMER1	✓	-
MCU_TIMER2	✓	-
MCU_TIMER3	✓	-
TIMER0	-	✓
TIMER1	-	✓
TIMER2	-	✓
TIMER3	-	✓
TIMER4	-	✓
TIMER5	-	✓
TIMER6	-	✓
TIMER7	-	✓
TIMER8	-	✓
TIMER9	-	✓
TIMER10	-	✓
TIMER11	-	✓

All timers include specific functions to generate accurate tick interrupts to the operating system.

Each timer can be clocked from several different independent clocks. The selection of clock source is made from registers in the MCU_CTRL_MMR0/CTRL_MMR0.

In the MCU domain the device provides 4 timer pins, one for each instance, to be used as MCU Timer Capture inputs or as MCU Timer PWM outputs.

In the MAIN domain the device provides 11 timer pins, one for each instance, to be used as Timer Capture inputs or as Timer PWM outputs.

Each odd numbered timer instance from each of the domains may be optionally cascaded with the previous even numbered timer instance from the same domain to form up to a 64-bit timer. For example, TIMER1 may be cascaded to TIMER0, MCU_TIMER1 may be cascaded to MCU_TIMER0, etc.

When cascaded, TIMERi acts as a 32-bit prescaler to TIMERi+1, as well as MCU_TIMERn acts as a 32-bit prescaler to MCU_TIMERn+1. TIMERi / MCU_TIMERn must be configured to generate a PWM output edge at the desired rate to increment the TIMERi+1/ MCU_TIMERn+1 counter.

Figure 12-416 is an overview of the timers.

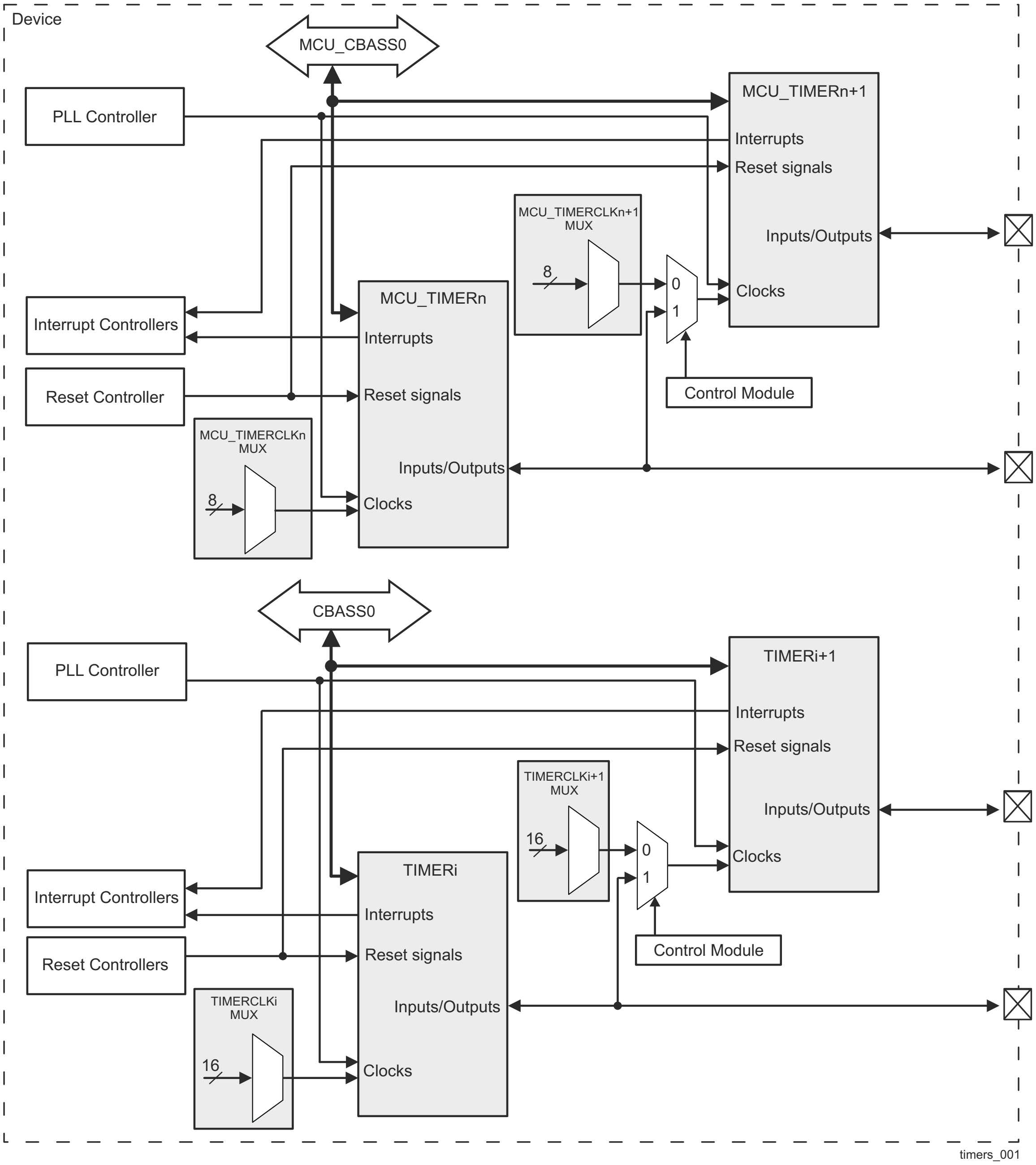

Note

i = 0, 2, 4, 6, 8, 10

Note

n = 0, 2

Figure 12-416. Timers Overview

12.5.3.1.1 Timers Features

The following are the main features of the timer controllers:

- Target interface supports:
  - 32-bit data bus width

  - 32-bit access supported
  - 10-bit address bus width
  - Write nonposted transaction mode supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start/stop mode
- Programmable divider clock source (2^n, where n = [0-8])
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- On-the-fly read/write register (while counting)
- Generates a 1-ms tick clock when functional clock is 32.768 kHz

12.5.3.1.2 Timers Not Supported Features

The following features are not supported on this family of devices:

- Atomic 64-bit timer value read of cascaded timers is not supported.
- Smart-idle with wake-up mode is not supported.

12.5.3.2 Timers Environment

The MCU_TIMER[3-0] and TIMER[11-0] modules are hereinafter referred to as timer module.

This section describes the timers external connections (environment).

12.5.3.2.1 Timer External System Interface

Each timer can send or receive stimulus to/from the external (off-chip) system. In the device all timers are configured to output a PWM pulse or receive an external event signal used as a trigger to capture the current timer count.

Figure 12-417 shows the external system interface for the timers, and Table 12-446 describes the timer inputs and outputs.

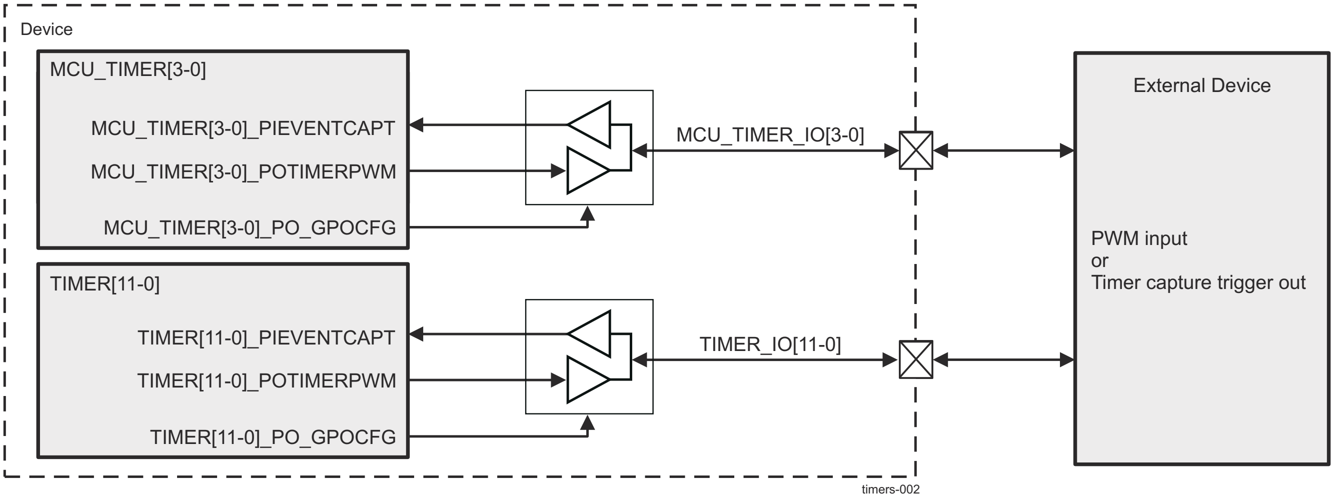

Figure 12-417. Timers External System Interface

Table 12-458. Timer I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
		MCU_TIMER[3-0]		
MCU_TIMER_IO0	MCU_TIMER0_PIEVENTCAPT MCU_TIMER0_POTIMERPWM	I/O	MCU_TIMER0 trigger input or MCU_TIMER0 output	0
MCU_TIMER_IO1	MCU_TIMER1_PIEVENTCAPT MCU_TIMER1_POTIMERPWM	I/O	MCU_TIMER1 trigger input or MCU_TIMER1 output	0
MCU_TIMER_IO2	MCU_TIMER2_PIEVENTCAPT MCU_TIMER2_POTIMERPWM	I/O	MCU_TIMER2 trigger input or MCU_TIMER2 output	0
MCU_TIMER_IO3	MCU_TIMER3_PIEVENTCAPT MCU_TIMER3_POTIMERPWM	I/O	MCU_TIMER3 trigger input or MCU_TIMER3 output	0
		TIMER[11-0]		
TIMER_IO0	TIMER0_PIEVENTCAPT TIMER0_POTIMERPWM	I/O	TIMER0 trigger input or TIMER0 PWM output	0
TIMER_IO1	TIMER1_PIEVENTCAPT TIMER1_POTIMERPWM	I/O	TIMER1 trigger input or TIMER1 output	0
TIMER_IO2	TIMER2_PIEVENTCAPT TIMER2_POTIMERPWM	I/O	TIMER2 trigger input or TIMER2 output	0
TIMER_IO3	TIMER3_PIEVENTCAPT TIMER3_POTIMERPWM	I/O	TIMER3 trigger input or TIMER3 output	0
TIMER_IO4	TIMER4_PIEVENTCAPT	I/O	TIMER4 trigger input or	0

Table 12-458. Timer I/O Signals (continued)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
	TIMER4_POTIMERPWM		TIMER4 PWM output	
TIMER_IO5	TIMER5_PIEVENTCAPT TIMER5_POTIMERPWM	I/O	TIMER5 trigger input or TIMER5 PWM output	0
TIMER_IO6	TIMER6_PIEVENTCAPT TIMER6_POTIMERPWM	I/O	TIMER6 trigger input or TIMER6 PWM output	0
TIMER_IO7	TIMER7_PIEVENTCAPT TIMER7_POTIMERPWM	I/O	TIMER7 trigger input or TIMER7 PWM output	0
TIMER_IO8	TIMER8_PIEVENTCAPT TIMER8_POTIMERPWM	I/O	TIMER8 trigger input or TIMER8 PWM output	0
TIMER_IO9	TIMER9_PIEVENTCAPT TIMER9_POTIMERPWM	I/O	TIMER9 trigger input or TIMER9 PWM output	0
TIMER_IO10	TIMER10_PIEVENTCAPT TIMER10_POTIMERPWM	I/O	TIMER10 trigger input or TIMER10 PWM output	0
TIMER_IO11	TIMER11_PIEVENTCAPT TIMER11_POTIMERPWM	I/O	TIMER11 trigger input or TIMER11 PWM output	0

(1) When configured for that function; I = Input, O = Output

Note

Each MCU_TIMER_PO_GPOCFG and TIMER_PO_GPOCFG signals are used as an output enable to control the function of the MCU_TIMER_IO[3-0], and respectively TIMER_IO[11-0], as the PWM output (PO_GPOCFG = 0) or capture input (PO_GPOCFG = 1).

Note

For more information about device level signals (pull-up/down resistors, buffer type, and others), see tables *Pin Attributes* in the device-specific Datasheet.

12.5.3.3 Timers Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

12.5.3.3.1 Timers Integration in MCU Domain

There are four timer modules integrated in the device MCU domain - MCU_TIMER0 through MCU_TIMER3. Figure 12-418 shows their integration in the device.

Each timer instance is supplied by dedicated TIMERCLKn clock mux. For MCU_TIMERn+1 the TIMERCLKn output is further muxed with the TIMERn_POTIMERPWM output.

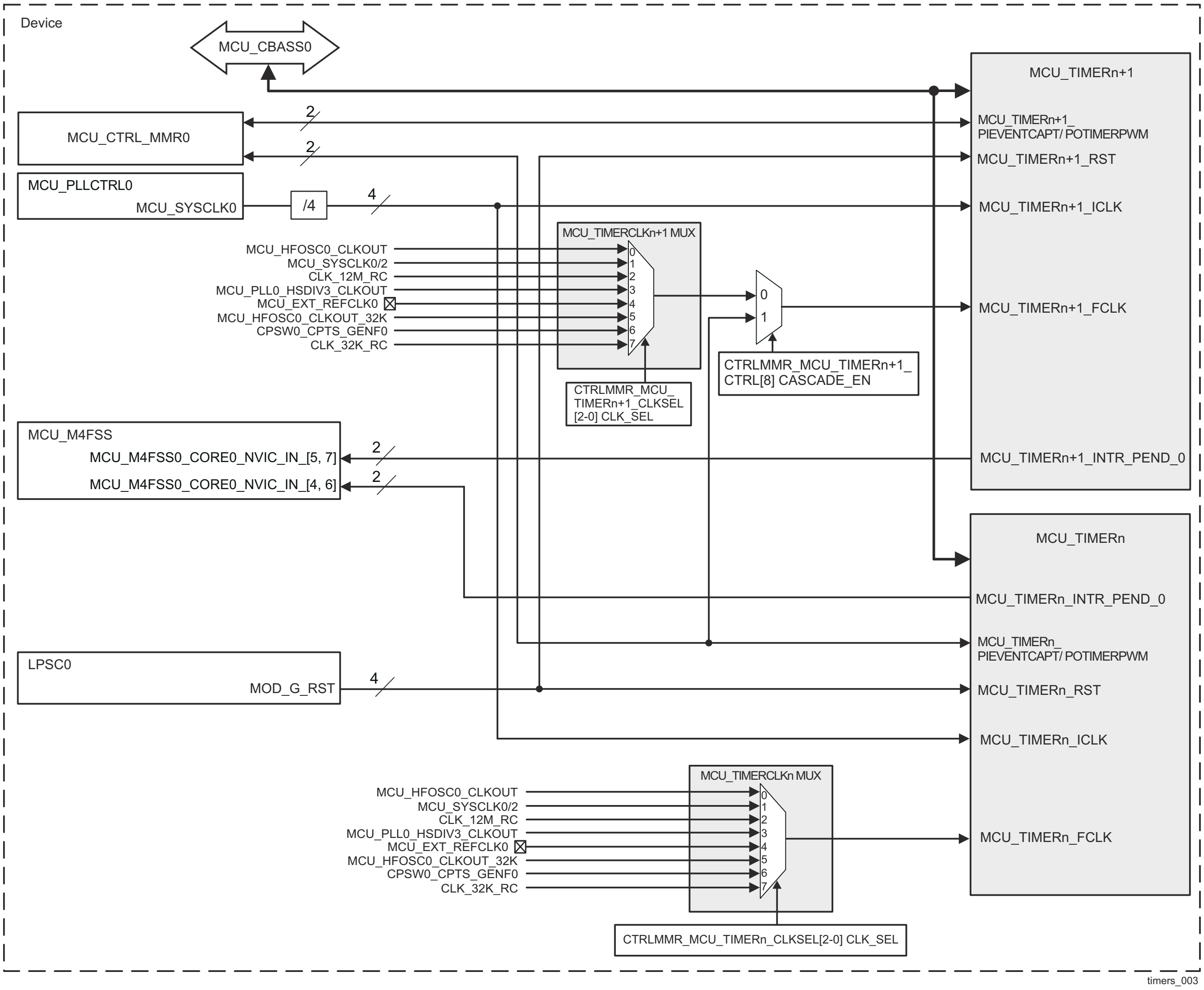

Note

n = 0, 2

Figure 12-418. MCU_TIMER Integration

Table 12-447 through Table 12-450 summarize the integration of MCU_TIMER0 through MCU_TIMER3 in device MCU domain.

Table 12-459. MCU_TIMER Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_TIMER0	MCU_PSC0	PD0	LPSC0	MCU_CBASS0
MCU_TIMER1	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-459. MCU_TIMER Integration Attributes (continued)

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_TIMER2	MCU_PSC0	PD0	LPSC0	MCU_CBASS0
MCU_TIMER3	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-460. MCU_TIMER Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_TIMER0	MCU_TIMER0_ICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_TIMER0 Interface Clock
	MCU_TIMER0_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	MCU_TIMER0 Functional Clock. Output of multiplexor MCU_TIMERCLK0 MUX controlled by CTRLMMR_MCU_TIMER0_CLKSEL[2-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*
		MCU_SYSCLK0/2	MCU_PLLCTRL0	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_PLL0_HSDIV3_CLKOUT	MCU_PLL0_HSDIV3	
		MCU_EXT_REFCLK0	I/O pin	
		MCU_HFOSC0_CLKOUT_32K	MCU_HFOSC0	
		CPSW0_CPTS_GENF0	CPSW0	
		CLK_32K_RC	MCU_RC_OSC_12M	
MCU_TIMER1	MCU_TIMER1_ICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_TIMER1 Interface Clock
	MCU_TIMER1_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	MCU_TIMER1 Functional Clock. Output of multiplexor MCU_TIMERCLK1 MUX controlled by CTRLMMR_MCU_TIMER1_CLKSEL[2-0] CLK_SEL or MCU_TIMER0_POTIMERPWM in Section 5.1 , *Control Module (CTRL_MMR)*
		MCU_SYSCLK0/2	MCU_PLLCTRL0	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_PLL0_HSDIV3_CLKOUT	MCU_PLL0_HSDIV3	
		MCU_EXT_REFCLK0	I/O pin	
		MCU_HFOSC0_CLKOUT_32K	MCU_HFOSC0	
		CPSW0_CPTS_GENF0	CPSW0	
		CLK_32K_RC	MCU_RC_OSC_12M	
MCU_TIMER2	MCU_TIMER2_ICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_TIMER2 Interface Clock
	MCU_TIMER2_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	MCU_TIMER2 Functional Clock. Output of multiplexor MCU_TIMERCLK2 MUX controlled by CTRLMMR_MCU_TIMER2_CLKSEL[2-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*
		MCU_SYSCLK0/2	MCU_PLLCTRL0	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_PLL0_HSDIV3_CLKOUT	MCU_PLL0_HSDIV3	
		MCU_EXT_REFCLK0	I/O pin	
		MCU_HFOSC0_CLKOUT_32K	MCU_HFOSC0	
		CPSW0_CPTS_GENF0	CPSW0	
		CLK_32K_RC	MCU_RC_OSC_12M	
MCU_TIMER3	MCU_TIMER3_ICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_TIMER3 Interface Clock
	MCU_TIMER3_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	MCU_TIMER3 Functional Clock. Output of multiplexor MCU_TIMERCLK3 MUX controlled by CTRLMMR_MCU_TIMER3_CLKSEL[2-0] CLK_SEL or MCU_TIMER2_POTIMERPWM in Section 5.1 , *Control Module (CTRL_MMR)*
		MCU_SYSCLK0/2	MCU_PLLCTRL0	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_PLL0_HSDIV3_CLKOUT	MCU_PLL0_HSDIV3	
		MCU_EXT_REFCLK0	I/O pin	
		MCU_HFOSC0_CLKOUT_32K	MCU_HFOSC0	

Table 12-460. MCU_TIMER Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
		CPSW0_CPTS_GENF0	CPSW0	
		CLK_32K_RC	MCU_RC_OSC_12M	

Table 12-461. MCU_TIMER Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_TIMER0	MCU_TIMER0_RST	MOD_G_RST	LPSC0	Asyncronous Reset to MCU_TIMER0
MCU_TIMER1	MCU_TIMER1_RST	MOD_G_RST	LPSC0	Asyncronous Reset to MCU_TIMER1
MCU_TIMER2	MCU_TIMER2_RST	MOD_G_RST	LPSC0	Asyncronous Reset to MCU_TIMER2
MCU_TIMER3	MCU_TIMER3_RST	MOD_G_RST	LPSC0	Asyncronous Reset to MCU_TIMER3

Table 12-462. MCU_TIMER Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_TIMER0	MCU_TIMER0_INTR_PEND_0	MCU_M4FSS0_CORE0_NVIC_IN_4	MCU_M4FSS0_CORE0	MCU_TIMER0 Interrupt Request	Level
MCU_TIMER1	MCU_TIMER1_INTR_PEND_0	MCU_M4FSS0_CORE0_NVIC_IN_5	MCU_M4FSS0_CORE0	MCU_TIMER1 Interrupt Request	Level
MCU_TIMER2	MCU_TIMER2_INTR_PEND_0	MCU_M4FSS0_CORE0_NVIC_IN_6	MCU_M4FSS0_CORE0	MCU_TIMER2 Interrupt Request	Level
MCU_TIMER3	MCU_TIMER3_INTR_PEND_0	MCU_M4FSS0_CORE0_NVIC_IN_7	MCU_M4FSS0_CORE0	MCU_TIMER3 Interrupt Request	Level

Note

Timer interrupts are further described in Section 12.5.3.4.4 , *Timer Interrupts*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.5.3.3.2 Timers Integration in MAIN Domain

There are twelve timer modules integrated in the device MAIN domain - TIMER0 through TIMER11. Figure 12-419 shows their integration in the device.

Each timer instance is supplied by dedicated TIMERCLKi clock mux. For TIMERi+1 the TIMERCLKi output is further muxed with the TIMERi_POTIMERPWM output.

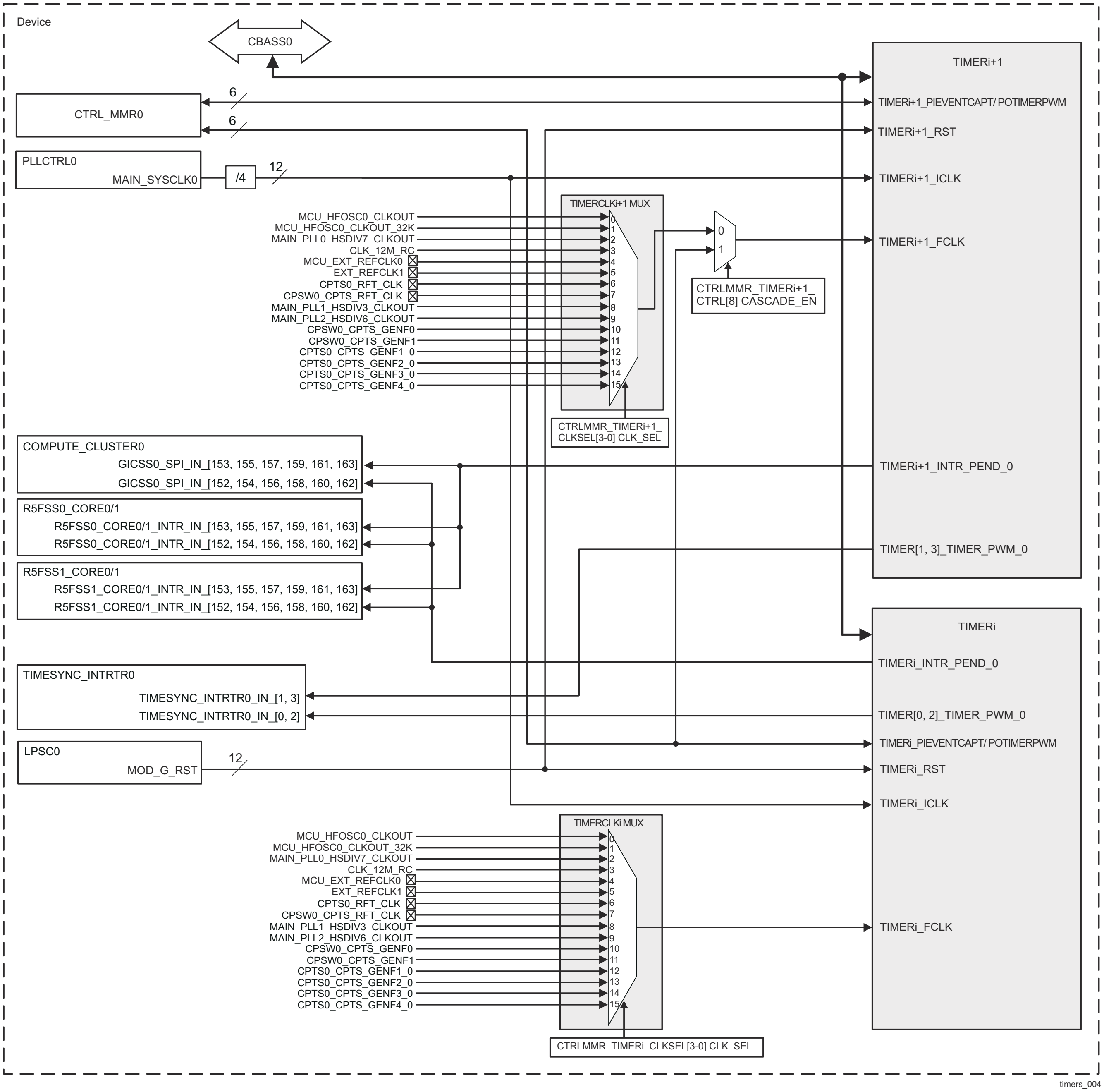

Note

i = 0, 2, 4, 6, 8, 10

Figure 12-419. TIMER Integration

Table 12-451 through Table 12-454 summarize the integration of TIMER0 through TIMER11 in device MAIN domain.

Table 12-463. TIMER Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
TIMER0	PSC0	PD0	LPSC0	CBASS0
TIMER1	PSC0	PD0	LPSC0	CBASS0
TIMER2	PSC0	PD0	LPSC0	CBASS0
TIMER3	PSC0	PD0	LPSC0	CBASS0
TIMER4	PSC0	PD0	LPSC0	CBASS0
TIMER5	PSC0	PD0	LPSC0	CBASS0
TIMER6	PSC0	PD0	LPSC0	CBASS0
TIMER7	PSC0	PD0	LPSC0	CBASS0
TIMER8	PSC0	PD0	LPSC0	CBASS0
TIMER9	PSC0	PD0	LPSC0	CBASS0
TIMER10	PSC0	PD0	LPSC0	CBASS0
TIMER11	PSC0	PD0	LPSC0	CBASS0

Table 12-464. TIMER Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
TIMER0	TIMER0_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER0 Interface Clock
	TIMER0_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER0 Functional Clock. Output of multiplexor TIMERCLK0 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL[3-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER1	TIMER1_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER1 Interface Clock
	TIMER1_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER1 Functional Clock. Output of multiplexor TIMERCLK1 MUX controlled by
		MCU_HFOSC0_CLKOUT_32K		

Table 12-464. TIMER Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL[3-0] CLK_SEL or TIMER0_POTIMERPWM in Section 5.1 , *Control Module (CTRL_MMR)*.
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER2	TIMER2_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER2 Interface Clock
	TIMER2_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER2 Functional Clock. Output of multiplexor TIMERCLK2 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL[3-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER3	TIMER3_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER3 Interface Clock
	TIMER3_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER3 Functional Clock. Output of multiplexor TIMERCLK3 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL[3-0] CLK_SEL or TIMER2_POTIMERPWM in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	

Table 12-464. TIMER Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER4	TIMER4_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER4 Interface Clock
	TIMER4_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER4 Functional Clock. Output of multiplexor TIMERCLK4 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL[3-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER5	TIMER5_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER5 Interface Clock
	TIMER5_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER5 Functional Clock. Output of multiplexor TIMERCLK5 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL[3-0] CLK_SEL or TIMER4_POTIMERPWM in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	

Table 12-464. TIMER Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER6	TIMER6_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER6 Interface Clock
	TIMER6_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER6 Functional Clock. Output of multiplexor TIMERCLK6 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL[3-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER7	TIMER7_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER7 Interface Clock
	TIMER7_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER7 Functional Clock. Output of multiplexor TIMERCLK7 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL[3-0] CLK_SEL or TIMER6_POTIMERPWM in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		

Table 12-464. TIMER Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
TIMER8	TIMER8_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER8 Interface Clock
	TIMER8_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER8 Functional Clock. Output of multiplexor TIMERCLK8 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL[3-0] CLK_SEL in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER9	TIMER9_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER9 Interface Clock
	TIMER9_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER9 Functional Clock. Output of multiplexor TIMERCLK9 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL[3-0] CLK_SEL or TIMER8_POTIMERPWM in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER10	TIMER10_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER10 Interface Clock
	TIMER10_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER10 Functional Clock. Output of multiplexor TIMERCLK10 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL[3-0] CLK_SEL in
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	

Table 12-464. TIMER Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
		CLK_12M_RC	MCU_RC_OSC_12M	Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		
TIMER11	TIMER11_ICLK	MAIN_SYSCLK0/4	PLLCTRL0	TIMER11 Interface Clock
	TIMER11_FCLK	MCU_HFOSC0_CLKOUT	MCU_HFOSC0	TIMER11 Functional Clock. Output of multiplexor TIMERCLK11 MUX controlled by MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL[3-0] CLK_SEL or TIMER10_POTIMERPWM in Section 5.1 , *Control Module (CTRL_MMR)*.
		MCU_HFOSC0_CLKOUT_32K		
		MAIN_PLL0_HSDIV7_CLKOUT	PLL0_HSDIV7	
		CLK_12M_RC	MCU_RC_OSC_12M	
		MCU_EXT_REFCLK0	I/O pin	
		EXT_REFCLK1	I/O pin	
		CPTS0_RFT_CLK	I/O pin	
		CPSW0_CPTS_RFT_CLK	I/O pin	
		MAIN_PLL1_HSDIV3_CLKOUT	PLL1_HSDIV3	
		MAIN_PLL2_HSDIV6_CLKOUT	PLL2_HSDIV6	
		CPSW0_CPTS_GENF0	CPSW0	
		CPSW0_CPTS_GENF1		
		CPTS0_CPTS_GENF1_0	CPTS0	
		CPTS0_CPTS_GENF2_0		
		CPTS0_CPTS_GENF3_0		
		CPTS0_CPTS_GENF4_0		

Table 12-465. TIMER Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
TIMER0	TIMER0_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER0
TIMER1	TIMER1_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER1
TIMER2	TIMER2_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER2
TIMER3	TIMER3_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER3
TIMER4	TIMER4_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER4

Table 12-465. TIMER Resets (continued)

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
TIMER5	TIMER5_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER5
TIMER6	TIMER6_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER6
TIMER7	TIMER7_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER7
TIMER8	TIMER8_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER8
TIMER9	TIMER9_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER9
TIMER10	TIMER10_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER10
TIMER11	TIMER11_RST	MOD_G_RST	LPSC0	Asyncronous Reset to TIMER11

Table 12-466. TIMER Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER0	TIMER0_INTR_PEND_0	GICSS0_SPI_IN_152	COMPUTE_CLUSTER0	TIMER0 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_152	R5FSS0_CORE0	TIMER0 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_152	R5FSS0_CORE1	TIMER0 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_152	R5FSS1_CORE0	TIMER0 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_152	R5FSS1_CORE1	TIMER0 Interrupt Request	Level
	TIMER0_TIMER_PWM_0	TIMESYNC_INTRTR0_IN_0	TIMESYNC_INTRTR0	TIMER0 Interrupt Request	Level
TIMER1	TIMER1_INTR_PEND_0	GICSS0_SPI_IN_153	COMPUTE_CLUSTER0	TIMER1 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_153	R5FSS0_CORE0	TIMER1 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_153	R5FSS0_CORE1	TIMER1 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_153	R5FSS1_CORE0	TIMER1 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_153	R5FSS1_CORE1	TIMER1 Interrupt Request	Level
	TIMER1_TIMER_PWM_0	TIMESYNC_INTRTR0_IN_1	TIMESYNC_INTRTR0	TIMER1 Interrupt Request	Level
TIMER2	TIMER2_INTR_PEND_0	GICSS0_SPI_IN_154	COMPUTE_CLUSTER0	TIMER2 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_154	R5FSS0_CORE0	TIMER2 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_154	R5FSS0_CORE1	TIMER2 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_154	R5FSS1_CORE0	TIMER2 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_154	R5FSS1_CORE1	TIMER2 Interrupt Request	Level
	TIMER2_TIMER_PWM_0	TIMESYNC_INTRTR0_IN_2	TIMESYNC_INTRTR0	TIMER2 Interrupt Request	Level
TIMER3	TIMER3_INTR_PEND_0	GICSS0_SPI_IN_155	COMPUTE_CLUSTER0	TIMER3 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_155	R5FSS0_CORE0	TIMER3 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_155	R5FSS0_CORE1	TIMER3 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_155	R5FSS1_CORE0	TIMER3 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_155	R5FSS1_CORE1	TIMER3 Interrupt Request	Level
	TIMER3_TIMER_PWM_0	TIMESYNC_INTRTR0_IN_3	TIMESYNC_INTRTR0	TIMER3 Interrupt Request	Level
TIMER4	TIMER4_INTR_PEND_0	GICSS0_SPI_IN_156	COMPUTE_CLUSTER0	TIMER4 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_156	R5FSS0_CORE0	TIMER4 Interrupt Request	Level

Table 12-466. TIMER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		R5FSS0_CORE1_INTR_IN_156	R5FSS0_CORE1	TIMER4 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_156	R5FSS1_CORE0	TIMER4 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_156	R5FSS1_CORE1	TIMER4 Interrupt Request	Level
TIMER5	TIMER5_INTR_PEND_0	GICSS0_SPI_IN_157	COMPUTE_CLUSTER0	TIMER5 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_157	R5FSS0_CORE0	TIMER5 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_157	R5FSS0_CORE1	TIMER5 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_157	R5FSS1_CORE0	TIMER5 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_157	R5FSS1_CORE1	TIMER5 Interrupt Request	Level
TIMER6	TIMER6_INTR_PEND_0	GICSS0_SPI_IN_158	COMPUTE_CLUSTER0	TIMER6 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_158	R5FSS0_CORE0	TIMER6 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_158	R5FSS0_CORE1	TIMER6 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_158	R5FSS1_CORE0	TIMER6 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_158	R5FSS1_CORE1	TIMER6 Interrupt Request	Level
TIMER7	TIMER7_INTR_PEND_0	GICSS0_SPI_IN_159	COMPUTE_CLUSTER0	TIMER7 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_159	R5FSS0_CORE0	TIMER7 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_159	R5FSS0_CORE1	TIMER7 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_159	R5FSS1_CORE0	TIMER7 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_159	R5FSS1_CORE1	TIMER7 Interrupt Request	Level
TIMER8	TIMER8_INTR_PEND_0	GICSS0_SPI_IN_160	COMPUTE_CLUSTER0	TIMER8 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_160	R5FSS0_CORE0	TIMER8 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_160	R5FSS0_CORE1	TIMER8 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_160	R5FSS1_CORE0	TIMER8 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_160	R5FSS1_CORE1	TIMER8 Interrupt Request	Level
TIMER9	TIMER9_INTR_PEND_0	GICSS0_SPI_IN_161	COMPUTE_CLUSTER0	TIMER9 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_161	R5FSS0_CORE0	TIMER9 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_161	R5FSS0_CORE1	TIMER9 Interrupt Request	Level

Table 12-466. TIMER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		R5FSS1_CORE0_INTR_IN_161	R5FSS1_CORE0	TIMER9 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_161	R5FSS1_CORE1	TIMER9 Interrupt Request	Level
TIMER10	TIMER10_INTR_PEND_0	GICSS0_SPI_IN_162	COMPUTE_CLUSTER0	TIMER10 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_162	R5FSS0_CORE0	TIMER10 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_162	R5FSS0_CORE1	TIMER10 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_162	R5FSS1_CORE0	TIMER10 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_162	R5FSS1_CORE1	TIMER10 Interrupt Request	Level
TIMER11	TIMER11_INTR_PEND_0	GICSS0_SPI_IN_163	COMPUTE_CLUSTER0	TIMER11 Interrupt Request	Level
		R5FSS0_CORE0_INTR_IN_163	R5FSS0_CORE0	TIMER11 Interrupt Request	Level
		R5FSS0_CORE1_INTR_IN_163	R5FSS0_CORE1	TIMER11 Interrupt Request	Level
		R5FSS1_CORE0_INTR_IN_163	R5FSS1_CORE0	TIMER11 Interrupt Request	Level
		R5FSS1_CORE1_INTR_IN_163	R5FSS1_CORE1	TIMER11 Interrupt Request	Level

Note

Timer interrupts are further described in Section 12.5.3.4.4 , *Timer Interrupts*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.5.3.4 Timers Functional Description

Each timer contains a free-running upward counter with autoreload capability on overflow. The timer counter can be read and written on-the-fly (while counting). Each timer includes compare logic to allow an interrupt event on a programmable counter matching value. A dedicated output signal can be pulsed or toggled on either an overflow or a match event. This offers time-stamp trigger signaling or PWM signal sources. A dedicated input signal can be used to trigger an automatic timer counter capture or an interrupt event on a programmable input signal transition. A programmable clock divider (prescaler) allows reduction of the timer input clock frequency. All internal timer interrupt sources are merged into one module interrupt line and one wake-up line.

Each internal interrupt source can be independently enabled and disabled by a dedicated bit in the DMTIMER1MS_IRQSTATUS_SET and DMTIMER1MS_IRQSTATUS_CLR register for the interrupt features, and a dedicated bit of the DMTIMER1MS_IRQWAKEEN register for a wake-up. In addition, timers have a mechanism implemented to generate an accurate tick interrupt.

For each timer implemented in the device, there are two possible clock sources:

- 32-kHz clock
- System clock

For more information of the selection of the input clock source, see Section 5.4 , *Clocking*.

Note

Application software must ensure that DMTIMER bus interface clock frequency be greater than input clock frequency before accessing DMTIMER registers. Failure to do so will result in bus hang condition.

Each timer supports three functional modes:

- Timer mode
- Capture mode
- Compare mode

The capture and compare modes are disabled by default after core reset.

12.5.3.4.1 Timer Block Diagram

Figure 12-420 is a block diagram of the timers.

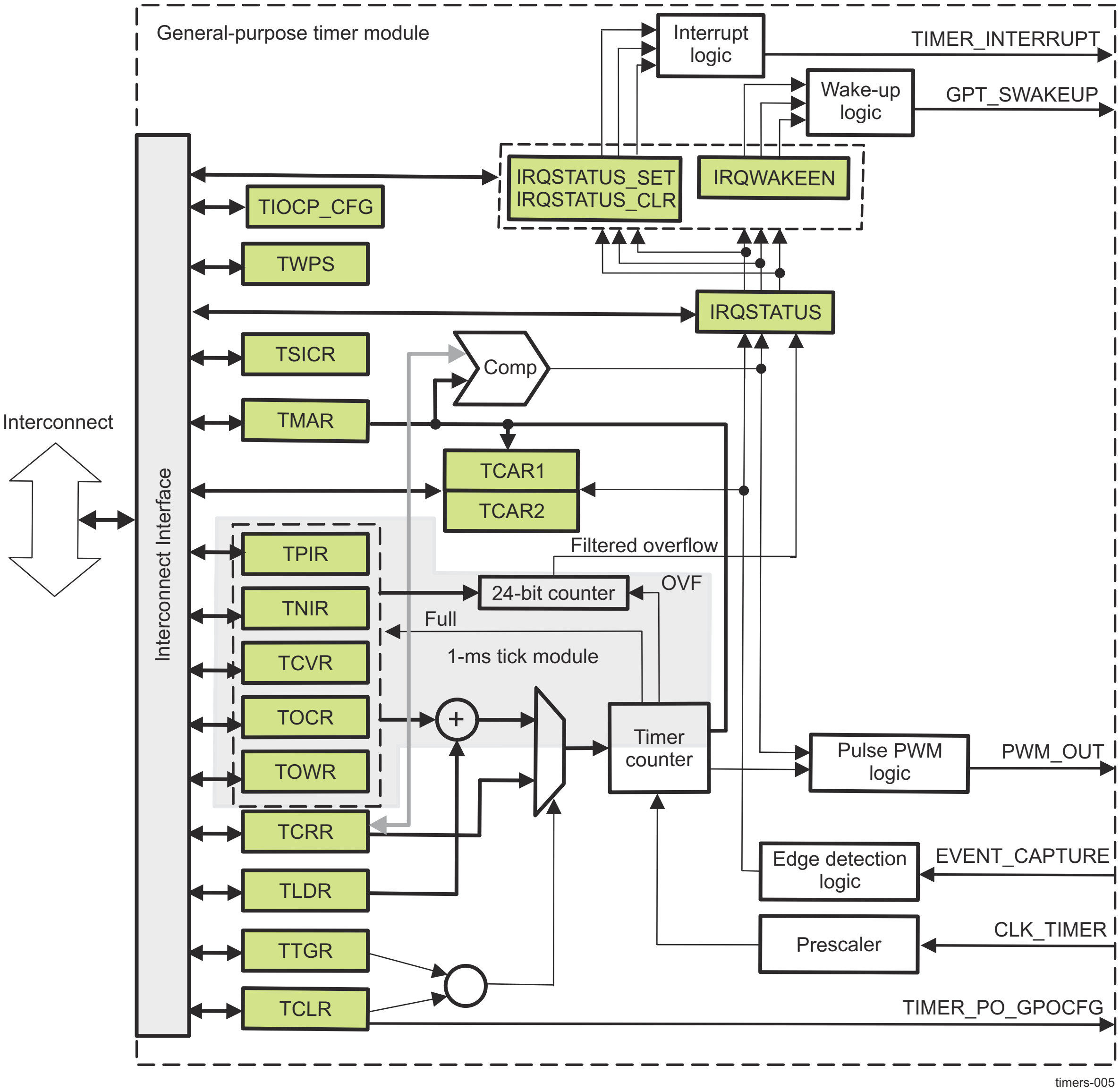

Figure 12-420. Timer Block Diagram

12.5.3.4.2 Timer Power Management

Note

Some of the timers features described in this section may not be supported on this family of devices. For more information, see Section 12.5.3.1.2 , *Timers Not Supported Features*.

The way the timer acknowledges the LPSC clock stop request is configurable through the DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE bit field.

Table 12-455 lists the IDLEMODE settings and the related acknowledgment modes.

Table 12-467. IDLEMODE Settings

IDLEMODE Value	Selected Mode	Description
00	Force-idle	The clock stop request is unconditionally acknowledged from the timer, regardless of its internal operations. This mode must be used carefully, because it does not prevent the loss of data when the clock is switched off.

Table 12-467. IDLEMODE Settings (continued)

IDLEMODE Value	Selected Mode	Description
01	No-idle	The clock stop request is never acknowledged from the timer. This mode is safe from a module point of view but is not efficient from a power-saving perspective because the clocks remain active.
10	Smart-idle	The timer acknowledges the clock stop request, basing its decision on its internal activity. The acknowledge signal is asserted only when all pending transactions and interrupt requests are treated. This is the best approach to efficient system power management.
11	Smart-idleWakeup	The module behaves like in Smart-idle mode, with the exception, that it can issue a wake-up request in sleep mode, if the functional clock is not cut off.

12.5.3.4.2.1 Wake-Up Capability

Note

Some of the timers features described in this section may not be supported on this family of devices. For more information, see Section 12.5.3.1.2 , *Timers Not Supported Features*.

If the DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE bit field sets the smart-idle mode or smart-idle with wake-up mode, the timer evaluates its internal capability to have the interface clock switched off. When there is no further internal activity (no pending interrupt sources: match, overflow, or timer capture events), the clock stop acknowledge signal is asserted and the timer enters sleep mode, ready to issue a wake-up request if configured in smart-idle with wake-up mode.

Figure 12-421 shows the wake-up request generation.

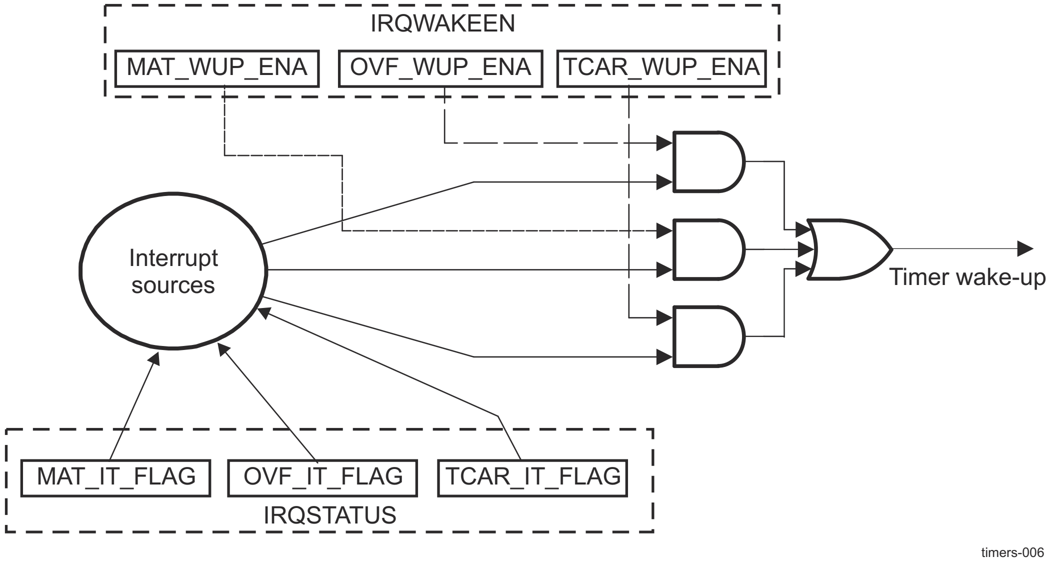

Figure 12-421. Wake-Up Request Generation

The timer wake-up-enable register allows masking of the expected source of the wake-up event that generates a wake-up request. The register is synchronously programmed with the interface clock before the Clock magagemet sends a clock stop request. The expected source of the wake-up event is an overflow (DMTIMER1MS_TCRR), a timer match (the compare result of DMTIMER1MS_TCRR and DMTIMER1MS_TMAR matches the counter value), and a timer capture (detection of an external pulse transition of the correct polarity on the TIMER_PIEVENTCAPT).

When the wake-up event is issued, the associated interrupt status bit is set in the timer status register (DMTIMER1MS_IRQSTATUS). The pending wake-up event is reset when the set status bit is overwritten with 1.

Note

The status bit must be reset to re-enter idle mode.

12.5.3.4.3 Timer Software Reset

DMTIMER1MS_TIOCP_CFG[0] SOFTRESET bit can initiate a software reset of the timer. This bit is autocleared to 0 when the reset is complete.

Before accessing or using the timer, the local host must ensure that internal reset is released by reading the DMTIMER1MS_TIOCP_CFG[0] SOFTRESET bit. This bit monitors the internal reset status.

12.5.3.4.4 Timer Interrupts

The timer can issue an overflow interrupt, a timer match interrupt, and a timer capture interrupt. Each internal interrupt source can be independently enabled and disabled in the interrupt-enable register (DMTIMER1MS_IRQSTATUS_SET) and disabled in the interrupt-disable register (DMTIMER1MS_IRQSTATUS_CLR). When the interrupt event is issued, the associated interrupt status bit is set in the timer status register (DMTIMER1MS_IRQSTATUS).

12.5.3.4.5 Timer Mode Functionality

The timer is an upward counter that can be started and stopped at any time through the timer control register (the DMTIMER1MS_TCLR[0] ST bit). The timer counter register (DMTIMER1MS_TCRR) can be loaded when stopped or on-the-fly (while counting). DMTIMER1MS_TCRR can be loaded directly by a DMTIMER1MS_TCRR write access with a new timer value. DMTIMER1MS_TCRR can also be loaded with the value held in the timer load register (DMTIMER1MS_TLDR) by a trigger register (DMTIMER1MS_TTGR) write access. The loading of DMTIMER1MS_TCRR is done regardless of the written value of DMTIMER1MS_TTGR. The value of DMTIMER1MS_TCRR can be read when stopped or captured on-the-fly by a DMTIMER1MS_TCRR read access. The timer is stopped and the counter value is set to 0 when the module reset is asserted. The timer is maintained at stop after the reset is released.

In one-shot mode (the DMTIMER1MS_TCLR[1] AR bit is set to 0), the counter is stopped after counting overflow occurs (the counter value remains at 0).

When the autoreload mode is enabled (the DMTIMER1MS_TCLR[1] AR bit is set to 1), DMTIMER1MS_TCRR is reloaded with the value of DMTIMER1MS_TLDR after a counting overflow occurs.

CAUTION

Do not put the overflow value (0xFFFF FFFF) in the DMTIMER1MS_TLDR register because it can lead to undesirable results.

An interrupt can be issued on overflow if the overflow interrupt-enable bit is set in the timer interrupt-enable register (the DMTIMER1MS_IRQSTATUS_SET[1] OVF_EN_FLAG bit is set to 1). A dedicated output pin (POTIMERPWM) can be programmed in the DMTIMER1MS_TCLR[12] PT bit through the DMTIMER1MS_TCLR[11-10] (PT and TRG bits) to generate one positive pulse (prescaler duration) or to invert the current value (toggle mode) when an overflow occurs. The DMTIMER1MS_TCLR[12] PT bit selects pulse/toggle modulation (the DMTIMER1MS_TCLR[11-10] TRG bit field selects trigger mode).

Figure 12-422 shows the DMTIMER1MS_TCRR timing value.

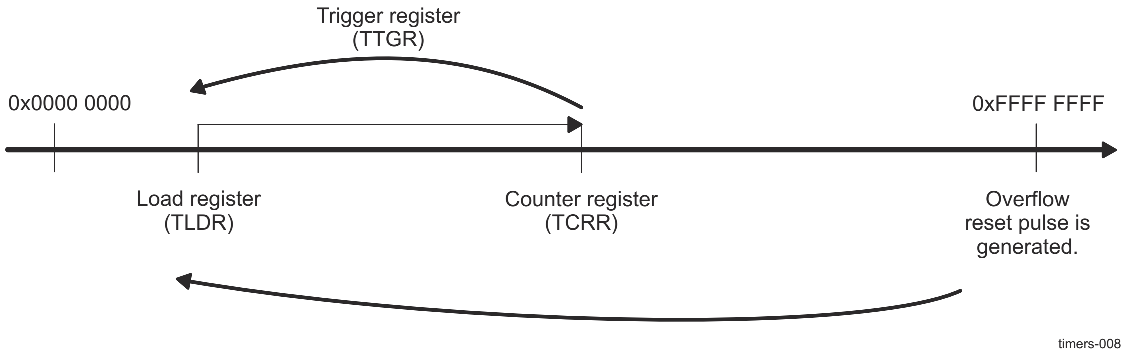

Figure 12-422. TIMER_TCRR Timing Value

12.5.3.4.5.1 1-ms Tick Generation

The interrupt period is not exactly 1 ms, because the timer input clock is 32.768 kHz. If the clock counts up to 32, it obtains a 0.977-ms period; if it counts up to 33, it obtains a 1.007-ms period. For large granularity, the error is cumulative and can generate important deviations from the standard value.

To minimize the error between a true 1-ms tick and the tick generated by the 32.768-kHz timer, the sequencing of periods less than 1 ms and periods greater than 1 ms must be shuffled. An additional 1-ms block is used to correct this error. See Figure 12-423.

In this implementation, the increment sequencing is automatically managed by the timer to minimize the error. The user must define only the value of the timer positive increment register (the DMTIMER1MS_TPIR[31-0] POSITIVE_INC_VALUE bit field) and the timer negative increment register (the DMTIMER1MS_TNIR[31-0] NEGATIVE_INC_VALUE bit field). An automatic adaptation mechanism is used to simplify the programming model.

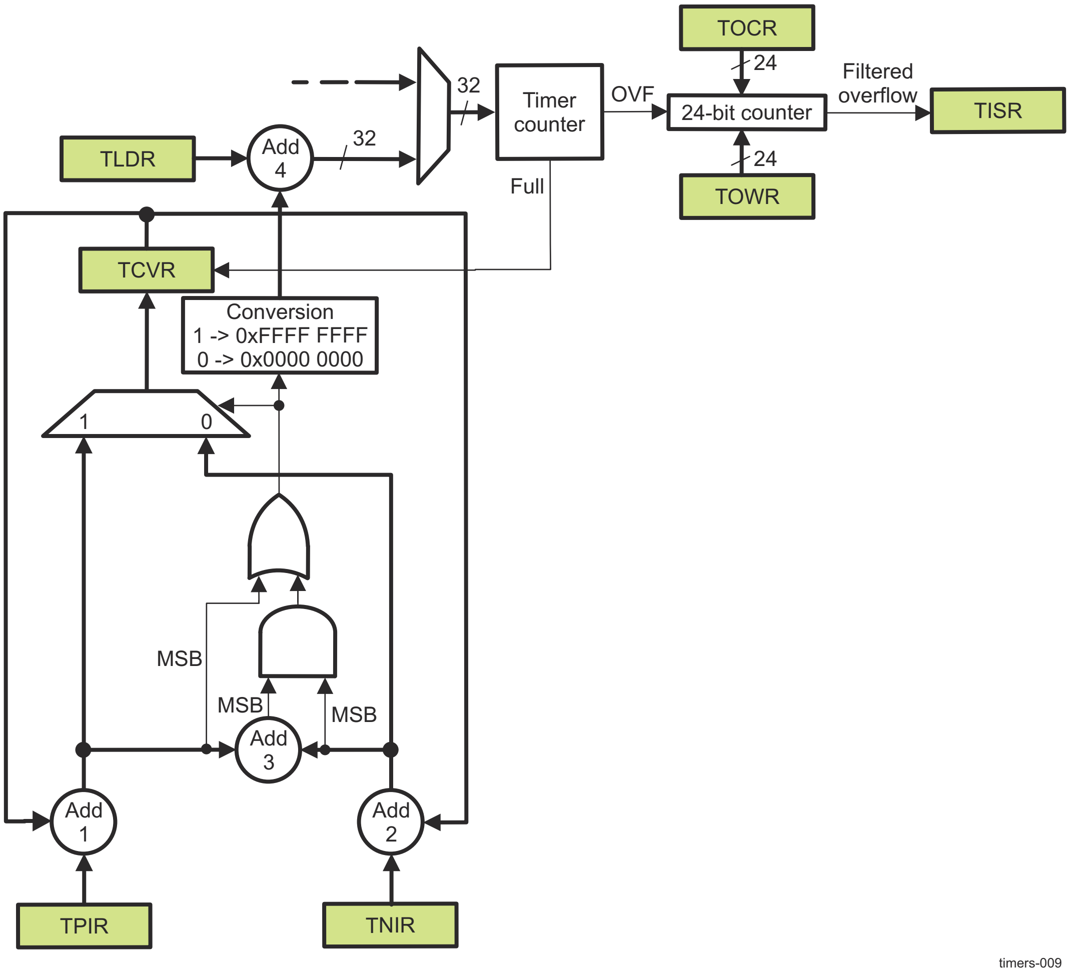

Figure 12-423. Block Diagram of the 1-ms Tick Module

The DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, and DMTIMER1MS_TCVR registers and adders Add1, Add2, and Add3 are used to define whether the next value loaded in the timer counter register (the DMTIMER1MS_TCRR[31-0] TIMER_COUNTER bit field) is the value of the DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field (period less than 1 ms) or the value of DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1 (period greater than 1 ms).

Table 12-456 lists the value loaded in the DMTIMER1MS_TCRR according to the sign of the result of Add1, Add2, and Add3.

MSB = 0: Positive value; MSB = 1: Negative value

Table 12-468. Value Loaded in TIMER_TCRR to Generate 1-ms Tick

Add1 MSB	Add2 MSB	Add3 MSB	Value of DMTIMER1MS_TCRR Register
0	0	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	0	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	1	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	1	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1
1	0	0	N/A
1	0	1	N/A
1	1	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1
1	1	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1

The values of the DMTIMER1MS_TPIR and DMTIMER1MS_TNIR registers are calculated using the following formulas:

- Positive increment value = (INTEGER[F_{clk} × T_{tick}] + 1) × 1e6) – (F_{clk} × T_{tick} × 1e6)
- Negative increment value = (INTEGER[F_{clk} × T_{tick}] × 1e6) – (F_{clk} × T_{tick} × 1e6)

Note

F_{clk} clock frequency (kHz)

T_{tick} tick period (ms)

The timer overflow counter register (DMTIMER1MS_TOCR) and the timer overflow wrapping register (DMTIMER1MS_TOWR) are used to filter interrupts. When the timer overflows, it increments the 24-bit DMTIMER1MS_TOCR. When the values in the 24-bit DMTIMER1MS_TOCR match the values in the 24-bit DMTIMER1MS_TOWR and the timer overflow is asserted, the DMTIMER1MS_TOCR is reset and an interrupt is generated to the DMTIMER1MS_IRQSTATUS register.

Note

DMTIMER1MS_TOWR has to be set to requested value. For example, if no interrupt needs to be masked DMTIMER1MS_TOWR must be set to 0, if one interrupt needs to be masked DMTIMER1MS_TOWR must be set to 1, if two interrupts need to be masked DMTIMER1MS_TOWR must be set to 2 and so on.

It is important to have in mind that the case when FFFFFF interrupts need to be masked is not possible.

With the conversion block in reset state (the positive increment register, negative increment register, and counter value register are zeroed), the programming model and the behavior of timers remain unchanged.

For 1-ms tick with a 32.768-kHz clock:

- DMTIMER1MS_TPIR[31-0] POSITIVE_INC_VALUE = 232,000
- DMTIMER1MS_TNIR[31-0] NEGATIVE_INC_VALUE = –768,000
- DMTIMER1MS_TLDR[31-0] LOAD_VALUE = 0xFFFF FFE0

Note

Any value of the tick period can be generated with the appropriate value of the DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, and DMTIMER1MS_TLDR.

By default, the DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR and the associated logic are in reset mode (all 0s) and have no effect on the programming model.

12.5.3.4.6 Timer Capture Mode Functionality

When a transition is detected on the module input pin (PIEVENTCAPT), the timer value in the DMTIMER1MS_TCRR can be captured and saved in the DMTIMER1MS_TCAR1 or DMTIMER1MS_TCAR2 register function of the mode selected in the DMTIMER1MS_TCLR[13] CAPT_MODE bit. The edge detection circuitry monitors transitions on the input pin (PIEVENTCAPT).

The rising edge, falling edge, or both, can be selected in the DMTIMER1MS_TCLR[9-8] TCM bit field to trigger the timer counter capture. The module sets the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit when an active edge is detected, and at the same time, the counter value DMTIMER1MS_TCRR is stored in timer capture register DMTIMER1MS_TCAR1 or DMTIMER1MS_TCAR2, as follows:

- If the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 0, on the first enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR1 register, and the next events are ignored (no update on the DMTIMER1MS_TCAR1 register and no interrupt triggering) until the detection logic is reset or the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG is cleared by writing 1 to it.
- If the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 1, on the first enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR1 register, and on the second enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR2 register. If a capture interrupt is enabled, the interrupt triggers on the second event capture. All other events are ignored (no update on DMTIMER1MS_TCAR1/DMTIMER1MS_TCAR2 and no interrupt triggering) until the detection logic is reset or the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit is cleared by writing 1 to it. This mechanism is useful for period calculation of a clock, if that clock is connected to the PIEVENTCAPT input pin.

The edge detection logic is reset (a new capture is enabled) when the active capture interrupt is served. The DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit is cleared by writing 1 to it or when the edge detection mode bits (the DMTIMER1MS_TCLR[9-8] TCM bit field) are changed from no-capture mode detection to any other mode. The timer functional clock (input to prescaler) is used to sample the input pin (PIEVENTCAPT). A negative or positive pulse input can be detected when the pulse time is greater than the functional clock period. An interrupt is issued on edge detection if the capture interrupt-enable bit is set in the DMTIMER1MS_IRQSTATUS_SET[2] TCAR_EN_FLAG bit. See the examples in Figure 12-424 and Figure 12-425.

In Figure 12-424, the value of the DMTIMER1MS_TCLR[9-8] TCM bit field is 1h, and the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 0. Only the rising edge of PIEVENTCAPT triggers a capture in the DMTIMER1MS_TCAR1 and DMTIMER1MS_TCAR2 registers, and only the DMTIMER1MS_TCAR1 register updates.

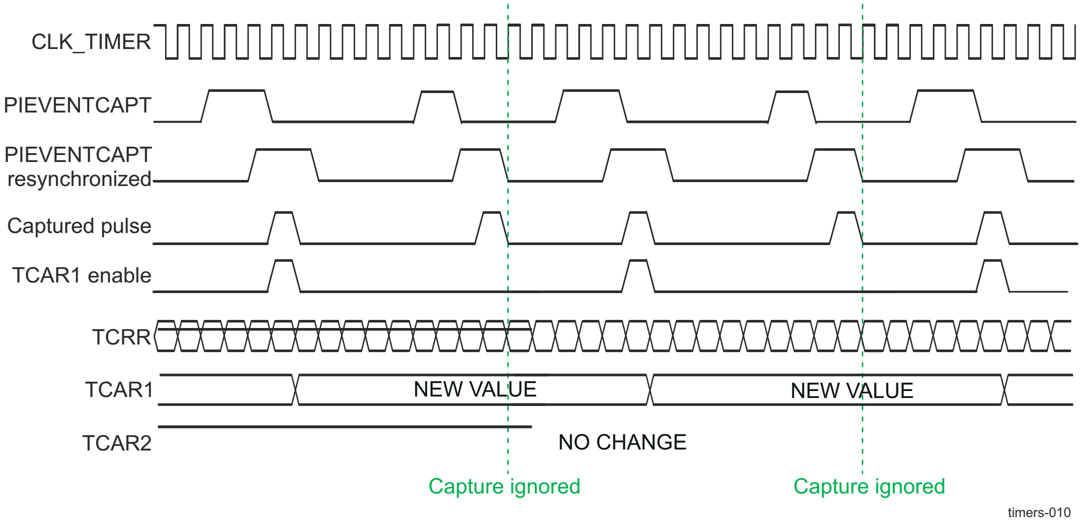

Figure 12-424. Capture Wave Example for TIMER_TCLR[13] CAPT_MODE = 0

In Figure 12-425, the value of the DMTIMER1MS_TCLR[9-8] TCM bit field is 1h, and the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 1. Only the rising edge of PIEVENTCAPT triggers a capture in the DMTIMER1MS_TCAR1 register on the first enabled event, and the DMTIMER1MS_TCAR2 register updates on the second enabled event.

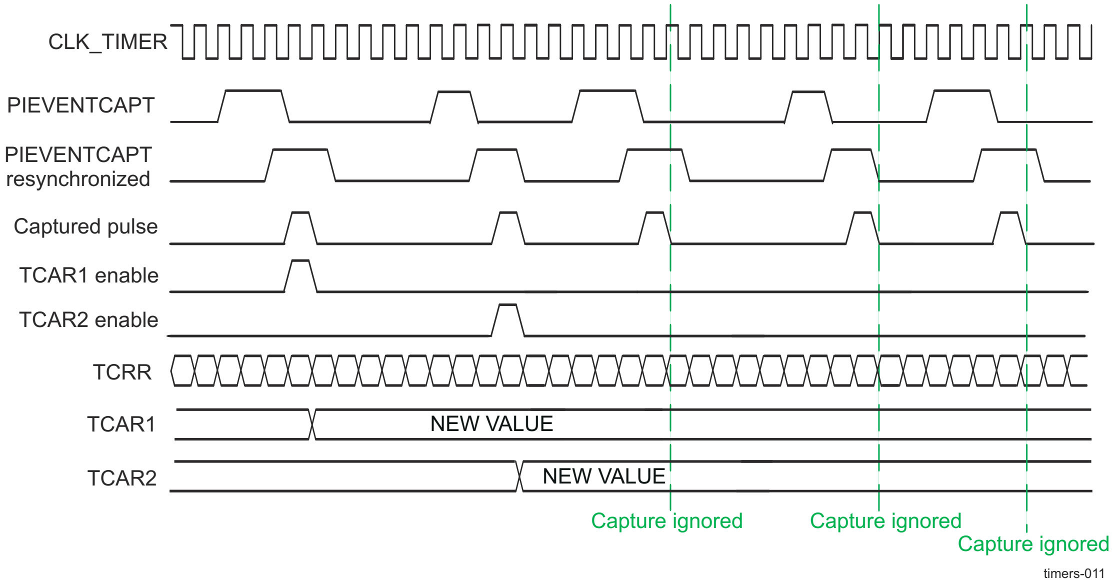

Figure 12-425. Capture Wave Example for TIMER_TCLR[13] CAPT_MODE = 1

12.5.3.4.7 Timer Compare Mode Functionality

When the compare-enable register DMTIMER1MS_TCLR[6] CE bit is set to 1, the timer value (the DMTIMER1MS_TCRR[31-0] TIMER_COUNTER bit field) is continuously compared to the value held in the timer match register (DMTIMER1MS_TMAR). The value of the DMTIMER1MS_TMAR[31-0] COMPARE_VALUE bit field can be loaded at any time (timer counting or stopped). When the DMTIMER1MS_TCRR and the DMTIMER1MS_TMAR values match, an interrupt is issued, if the DMTIMER1MS_IRQSTATUS_SET[0] MAT_EN_FLAG bit is set.

To prevent any unwanted interrupts due to reset value matching effect, write a compare value to the DMTIMER1MS_TMAR before setting the DMTIMER1MS_TCLR[6] CE bit.

The dedicated output pin (POTIMERPWM) can be programmed in the DMTIMER1MS_TCLR[12] PT bit through the DMTIMER1MS_TCLR[11-10] TRG bit field to generate one positive pulse (timer clock duration) or to invert the current value (toggle mode) when an overflow or a match occurs.

12.5.3.4.8 Timer Prescaler Functionality

A prescaler can be used to divide the timer counter input clock frequency. The prescaler is enabled when the DMTIMER1MS_TCLR[5] PRE bit is set. The DMTIMER1MS_TCLR[4-2] PTV bit field sets the 2^n division ratio (prescaler value is $2^{(PTV + 1)}$. The prescaler counter is reset when the timer counter is stopped or reloaded on-the-fly.

Table 12-457 lists the prescaler/timer reload values versus contexts.

Table 12-469. Prescaler/Timer Reload Values Versus Contexts

Context	Prescaler	Timer Counter
Overflow (when autoreload is on)	Reset	DMTIMER1MS_TLDR[31-0]
DMTIMER1MS_TCRR write	Reset	DMTIMER1MS_TCRR[31-0]
DMTIMER1MS_TTGR write	Reset	DMTIMER1MS_TLDR[31-0]
Stop	Reset	Frozen

12.5.3.4.9 Timer Pulse-Width Modulation

The timer can be configured to provide a programmable PWM output. The timer PWM (POTIMERPWM) output pin can be configured to toggle on an event. The DMTIMER1MS_TCLR[11-10] TRG bit field determines on which register value the PWM pin toggles. Either overflow or both overflow and match can be selected to toggle the timer PWM pin when a compare condition occurs.

Note

In toggle mode, when DMTIMER1MS_TCLR[11-10] TRG = 0x2 (overflow and match), the first event that toggles the PWM line is an overflow event.

The DMTIMER1MS_TCLR[7] SCPWM bit can be programmed to set or clear the timer PWM output signal only while the counter is stopped or the trigger is off. This allows setting the output pin to a known state before modulation starts. Modulation synchronously stops when the DMTIMER1MS_TCLR[11-10] TRG bit field is cleared and overflow occurs. This allows fixing a deterministic state of the output pin when modulation stops.

In Figure 12-426, the internal overflow pulse is set each time the (0xFFFF FFFF – DMTIMER1MS_TLDR[31-0] LOAD_VALUE + 1) value is reached, and the internal match pulse is set when the counter reaches the value of DMTIMER1MS_TMAR. Depending on the value of the DMTIMER1MS_TCLR[12] PT bit and DMTIMER1MS_TCLR[11-10] TRG bit field, the timer provides pulse or PWM event on the output pin (POTIMERPWM).

The DMTIMER1MS_TLDR and DMTIMER1MS_TMAR must keep values below the overflow value (0xFFFF FFFF) by at least two units. If the PWM trigger events are both overflow and match, the difference between the values kept in the DMTIMER1MS_TMAR and the value in the DMTIMER1MS_TLDR must be at least two units. When match event is used, the compare mode DMTIMER1MS_TCLR[6] CE bit must be set.

In Figure 12-426, the DMTIMER1MS_TCLR[7] SCPWM bit is set to 0. In Figure 12-427, the DMTIMER1MS_TCLR[7] SCPWM bit is set to 1. To obtain the desired wave form, start the counter at 0xFFFF FFFE value (to ensure an overflow first) or adjust the line polarity (DMTIMER1MS_TCLR[7] SCPWM bit).

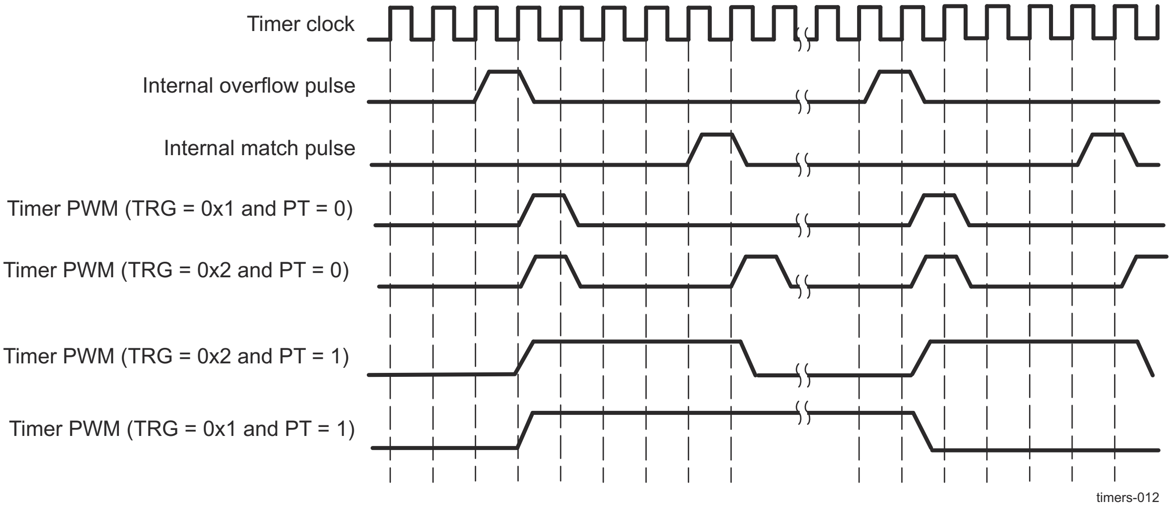

Figure 12-426. Timing Diagram of PWM With TIMER_TCLR[7] SCPWM Bit = 0

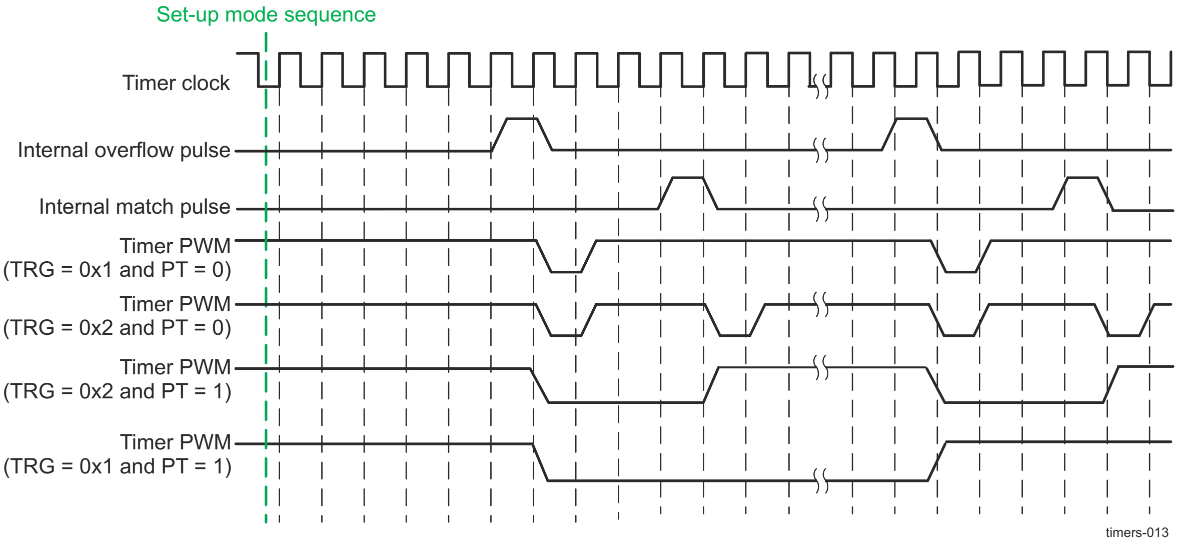

Figure 12-427. Timing Diagram of PWM With TIMER_TCLR[7] SCPWM Bit = 1

12.5.3.4.10 Timer Counting Rate

The timer rate is defined by the following values:

- Value of the prescaler fields (the DMTIMER1MS_TCLR[5] PRE bit and DMTIMER1MS_TCLR[4-2] PTV bit field)
- Value loaded into the DMTIMER1MS_TLDR

Table 12-458 lists the prescaler clock ratio values.

Table 12-470. Prescaler Clock Ratio Values

DMTIMER1MS_TCLR**[5] PRE**	DMTIMER1MS_TCLR**[4-2] PTV**	**Divisor (PS)**
0	X	1
1	0	2
1	1	4
1	2	8
1	3	16
1	4	32
1	5	64
1	6	128
1	7	256

Thus, the timer overflow rate is expressed as:

OVF_Rate = (0xFFFF FFFF – DMTIMER1MS_TLDR + 1) × (timer-functional clock period) × PS

With (timer-functional clock period) = 1/(timer-functional clock frequency) and PS = $2^{(PTV + 1)}$ if prescaler is enabled, or PS = 1 if prescaler is disabled.

CAUTION

Internal resynchronization causes any write to the DMTIMER1MS_TCLR[1] ST bit to have some latency before the register is updated:

2.5 × functional clock cycles write_TIMER_TCLR_latency 3.5 × functional clock cycles

Remember to consider this latency whenever the timer must be started or stopped by a software change to the DMTIMER1MS_TCLR[1] ST bit.

CAUTION

- In non-PWM mode, DMTIMER1MS_TLDR must be maintained at less than or equal to 0xFFFF FFFE.
- In PWM mode, DMTIMER1MS_TLDR must be maintained at less than or equal to 0xFFFF FFFD.

For example, with a timer clock input of 32 kHz and the DMTIMER1MS_TCLR[5] PRE bit set to 0, the timer output period is as listed in Table 12-459.

Table 12-471. Value and Corresponding Interrupt Period

DMTIMER1MS_TLDR[31-0] LOAD_VALUE	Interrupt Period
0x0000 0000	37 h
0xFFFF 0000	2 s
0xFFFF FFF0	500 µs
0xFFFF FFFE	62.5 µs

12.5.3.4.11 Timer Under Emulation

During emulation mode, the timer continues to run according to the value of the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit.

If the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit is set to 1, timer execution is not stopped in emulation mode and the interrupt is still generated when overflow or match is reached.

If the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit is set to 0, the prescaler and timer are frozen and both resume on exit from emulation mode. The asynchronous external input pin (MCU_TIMER_IO[9-0] or TIMER_IO[7-0]) is internally synchronized on two timer-clock rising edges.

12.5.3.4.12 Accessing Timer Registers

All accesses are posted mode, under the assumption that freq(timer clock) < freq(interface clock)/4, until software reconfiguration. In addition, it is not recommended to access the timer registers prior to the PLLs generating the timer and interface clocks have been configured and the clocks have stabilized. All registers are 32 bits wide, accessible through the configuration interface with 32-bit access (read/write).

Write operations to the following functional registers must be complete (the MSB must be written even if the MSB data is not used):

- DMTIMER1MS_TCLR
- DMTIMER1MS_TCRR
- DMTIMER1MS_TLDR
- DMTIMER1MS_TTGR
- DMTIMER1MS_TMAR
- DMTIMER1MS_TPIR
- DMTIMER1MS_TNIR
- DMTIMER1MS_TCVR
- DMTIMER1MS_TOCR
- DMTIMER1MS_TOWR

The following registers are not affected by the posted/nonposted mode selection; the write/read operation is effective and acknowledged (command accepted) after one interface clock cycle from command assertion:

- DMTIMER1MS_TIDR
- DMTIMER1MS_TIOCP_CFG
- DMTIMER1MS_IRQSTATUS
- DMTIMER1MS_IRQSTATUS_RAW
- DMTIMER1MS_IRQSTATUS_SET
- DMTIMER1MS_IRQSTATUS_CLR
- DMTIMER1MS_IRQWAKEEN
- DMTIMER1MS_TWPS
- DMTIMER1MS_TSICR

12.5.3.4.12.1 Writing to Timer Registers

The host uses the configuration interface to write to the following registers synchronously with the timer interface clock:

- DMTIMER1MS_TLDR
- DMTIMER1MS_TCRR
- DMTIMER1MS_TCLR
- DMTIMER1MS_TIOCP_CFG
- DMTIMER1MS_IRQSTATUS
- DMTIMER1MS_IRQSTATUS_SET
- DMTIMER1MS_IRQSTATUS_CLR
- DMTIMER1MS_IRQWAKEEN
- DMTIMER1MS_TTGR
- DMTIMER1MS_TSICR
- DMTIMER1MS_TMAR
- DMTIMER1MS_TPIR
- DMTIMER1MS_TNIR
- DMTIMER1MS_TCVR
- DMTIMER1MS_TOCR
- DMTIMER1MS_TOWR

12.5.3.4.12.1.1 Write Posting Synchronization Mode

This mode is used if the DMTIMER1MS_TSICR[2] POSTED bit is set to 1 (default value).

This mode uses a posted write scheme to update any internal register (DMTIMER1MS_TCLR, DMTIMER1MS_TCRR, DMTIMER1MS_TLDR, DMTIMER1MS_TTGR, DMTIMER1MS_TMAR, DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR). Therefore, the write transaction is immediately acknowledged on the configuration interface, although the effective write operation occurs later because of a resynchronization in the timer clock domain. The advantage is that neither the interconnect, nor the device that requested the write transaction is stalled.

For each register, a status bit is provided in the timer write-posted status (DMTIMER1MS_TWPS) register. In this mode, it is mandatory that software check this status bit before any write access. If a write is attempted to a register with a previous access pending, the previous access is discarded without notice.

The timer module updates the value of the timer counter register synchronously with the interface clock. Consequently, any read access to DMTIMER1MS_TCRR does not add any resynchronization latency; the current value is always available.

Note

Because the overflow IRQ is generated when the value of DMTIMER1MS_TCRR reaches 0xFFFF FFFF, and not when it changes its value to the value after overflow, it is necessary to wait a delay of (1 × PS × timer functional clock period) before any read access to DMTIMER1MS_TCRR to ensure a correct reading of its content.

Note

If DMTIMER1MS_TTGR register is written during a posted write to DMTIMER1MS_TCRR, the value to be written to DMTIMER1MS_TCRR will be discarded.

If a posted write to DMTIMER1MS_TCVR is started, the user must not write to DMTIMER1MS_TPIR or DMTIMER1MS_TNIR before the DMTIMER1MS_TCVR write is finished, because the value of DMTIMER1MS_TCVR is re-evaluated, so both the value to be written, and the recalculated value will be discarded.

If a write access is pending for a register, reading from this register does not yield a correct result. Software synchronization must be used to avoid incorrect results.

Functional frequency range: freq(timer clock) < freq(interface clock)/4.

12.5.3.4.12.1.2 Write Nonposting Synchronization Mode

This mode is used if the DMTIMER1MS_TSICR[2] POSTED bit is set to 0. It uses a nonposted write scheme to update any internal register. Therefore, the write transaction is not acknowledged on the configuration interface until the effective write operation occurs after the resynchronization in the timer functional clock domain. The drawback is that the interconnect and the device that requested the write transaction are stalled during this period.

The same full resynchronization scheme is used for a read transaction, and the same stall period applies. A register read following a write to the same register is always coherent.

This mode is functional regardless of the ratio between the configuration interface frequency and the timer clock frequency.

12.5.3.4.12.2 Reading From Timer Counter Registers

Note

LSB/MSB accesses cannot be interleaved (that is, the sequence LSB register 1, LSB register 2, MSB register 1, MSB register 2 is not supported).

The DMTIMER1MS_TCRR is a 32-bit “atomic datum” and its 16-bit capture is done on the 16-bit LSB first to allow atomic LSB16 + MSB16 capture. This capture scheme is also performed for the DMTIMER1MS_TCAR1 and DMTIMER1MS_TCAR2 registers as they can be changed due to internal processes too.

12.5.3.4.12.2.1 Read Posted

This mode is functional regardless of the ratio between the configuration interface frequency and the functional clock frequency. The recommended functional frequency range is freq(timer) < freq(interface clock)/4.

Read posted mode is used if DMTIMER1MS_TSICR[2] POSTED = 0x1 or DMTIMER1MS_TSICR[3] READ_MODE is set to 0. This mode uses a posted-read scheme for reading any internal timer register. The read transaction is immediately acknowledged on the configuration interface, prior to the value to be read has been resynchronized. With this method, neither the interconnect nor the device that requested the read transaction are stalled.

Read posted mode applies to DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR, which needs resynchronization from functional to interface clock domains.

Note that in Posted mode, if the DMTIMER1MS_TCRR is read immediately after wake-up and the interface clock is off during idle state, then it is possible to get an old value from just before going to idle state due to the fact the interface clock is needed for synchronization.

In order to avoid this situation, another synchronization mechanism is used for the first read operation after idle state. The DMTIMER1MS_TSICR[4] READ_AFTER_IDLE bit is used to enable/disable the mechanism.

When the synchronization mechanism is disabled (READ_AFTER_IDLE bit is set to 1), first read transaction takes only 2 interface clock cycles, but the read value of DMTIMER1MS_TCRR could be wrong.

When the synchronization mechanism is enabled (READ_AFTER_IDLE bit is set to 0), first read value of DMTIMER1MS_TCRR is correct, but the read transaction takes more than 2 interface clock cycles.

12.5.3.4.12.2.2 Read Non-Posted

This mode is functional regardless of the ratio between the configuration interface frequency and the functional clock frequency. Recommended functional frequency range is freq(timer) >= freq(interface clock)/4.

Read non-posted mode is used if DMTIMER1MS_TSICR[2] POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x1. This mode uses a non-posted read scheme for reading internal timer registers. The read transaction is not acknowledged on the configuration interface until the effective read operation occurs, after the resynchronization in the timer clock domain. The result is that both the interconnect and the device that requested the read transaction are stalled during this period.

This mode applies to DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR, which need resynchronization from functional to interface clock domains.

12.5.3.4.13 Timer Posted Mode Selection

A choice between two synchronization modes is made taking into account the frequency ratio and the stall periods that can be supported by the system, without impacting the global performance.

The posted mode selection applies only to registers that require synchronization on or from the timer clock domain. For write operation, the registers affected by posted and non-posted selection are DMTIMER1MS_TCLR, DMTIMER1MS_TLDR, DMTIMER1MS_TCRR, DMTIMER1MS_TTGR, DMTIMER1MS_TMAR, DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR. For read operation, the registers affected by this selection are: DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR.

The interface clock domain synchronous registers DMTIMER1MS_TIDR, DMTIMER1MS_TIOCP_CFG, DMTIMER1MS_IRQSTATUS, DMTIMER1MS_IRQSTATUS_SET, DMTIMER1MS_IRQWAKEEN, DMTIMER1MS_TWPS, and DMTIMER1MS_TSICR are not affected by posted and non-posted mode selection. The operation (read or write) is effective and acknowledged after one interface clock cycle from the command assertion.

The configuration of posted or non-posted mode can be changed (overwritten) by software by writing in DMTIMER1MS_TSICR[2] POSTED bit. The DMTIMER1MS_TSICR[3] READ_MODE defines how the read operation is performed when the module is configured in non-posted mode (see DMTIMER1MS_TSICR). The following cases are possible:

- DMTIMER1MS_TSICR[2] POSTED = 0x1 and DMTIMER1MS_TSICR[3] READ_MODE = x (don’t care): read and write operations are expected in posted mode.
- DMTIMER1MS_TSICR[2] POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x0: the write operation is executed in non-posted mode and read is executed in posted mode.

- DMTIMER1MS_TSICR[2]POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x1: write is executed in non-posted mode and read is executed in non-posted mode.

12.5.3.5 Timers Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

12.5.3.5.1 Timer Global Initialization

12.5.3.5.1.1 Main Sequence – Timer Module Global Initialization

Table 12-460 identifies the main steps for initializing the timer module when the module is to be used for the first time.

Table 12-472. Timer Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	DMTIMER1MS_TIOCP_CFG[0] SOFTRESET	0x1
Wait until reset release?	DMTIMER1MS_TIOCP_CFG[0] SOFTRESET	0x0
Configure idle mode.	DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE	0x-
Enable wake-up interrupt events.	DMTIMER1MS_IRQWAKEEN[2-0]	0x-
Select posted mode.	DMTIMER1MS_TSICR[2] POSTED	0x-

12.5.3.5.2 Timer Operational Mode Configuration

12.5.3.5.2.1 Timer Mode

12.5.3.5.2.1.1 Main Sequence – Timer Mode Configuration

Table 12-461 lists the steps in the timer mode configuration.

Table 12-473. Timer Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Enable overflow interrupt.	DMTIMER1MS_IRQSTATUS_SET[1] OVF_IT_FLAG	0x1
Load timer counter value.	DMTIMER1MS_TCRR	0x-
Load timer load value.	DMTIMER1MS_TLDR	0x-
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.5.3.5.2.2 Timer Compare Mode

12.5.3.5.2.2.1 Main Sequence – Timer Compare Mode Configuration

Table 12-462 lists the steps in the timer compare mode configuration.

Table 12-474. Timer Compare Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Enable match interrupt.	DMTIMER1MS_IRQSTATUS_SET[0] MAT_EN_FLAG	0x1
Load timer counter value.	DMTIMER1MS_TCRR	0x-
Load timer compare value.	DMTIMER1MS_TMAR	0x-
Enable compare mode.	DMTIMER1MS_TCLR[6] CE	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.5.3.5.2.3 Timer Capture Mode

12.5.3.5.2.3.1 Main Sequence – Timer Capture Mode Configuration

Table 12-463 lists the steps in the timer capture mode configuration.

Table 12-475. Timer Capture Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Initialize capture mode.	See Section 12.5.3.5.2.3.2 .	
Enable capture interrupt.	DMTIMER1MS_IRQSTATUS_SET[2] TCAR_EN_FLAG	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1
Detect event.	See Section 12.5.3.5.2.3.3 .	

12.5.3.5.2.3.2 Subsequence – Initialize Capture Mode

Table 12-464 lists the steps to initialize capture mode.

Table 12-476. Initialize Capture Mode

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Select TIMER[11-0] or MCU_TIMER[3-0] Capture input at device pins TIMER_IO[11-0] for TIMER[11-0] or at pins MCU_TIMER_IO[3-0] for MCU_TIMER[3-0].	DMTIMER1MS_TCLR[14] GPO_CFG	0x1
Select single or second event capture.	DMTIMER1MS_TCLR[13] CAPT_MODE	0x-
Select transition capture mode.	DMTIMER1MS_TCLR[9-8] TCM	0x-

12.5.3.5.2.3.3 Subsequence – Detect Event

Table 12-465 lists the steps in detecting an event.

Table 12-477. Detect Event

Step	Register/Bit Field/Programming Model	Value
Wait until event detected?	DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG	= 0x1
Read timer capture value.	DMTIMER1MS_TCAR1 and/or DMTIMER1MS_TCAR2	
Clear capture interrupt request.	DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG	0x1

12.5.3.5.2.4 Timer PWM Mode

12.5.3.5.2.4.1 Main Sequence – Timer PWM Mode Configuration

Table 12-466 lists the steps in the timer PWM mode configuration.

Table 12-478. Timer PWM Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Select trigger output mode.	DMTIMER1MS_TCLR[11-10] TRG	0x-
Select pulse or toggle modulation PWM mode.	DMTIMER1MS_TCLR[12] PT	0x-
Select TIMER[11-0] or MCU_TIMER[3-0] PWM output at device pins TIMER_IO[11-0] for TIMER[11-0] or at pins MCU_TIMER_IO[3-0] for MCU_TIMER[3-0].	DMTIMER1MS_TCLR[14] GPO_CFG	0x0
Configure PWM output pin default value.	DMTIMER1MS_TCLR[7] SCPWM	0x-

Table 12-478. Timer PWM Mode Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Load timer load value.	DMTIMER1MS_TCLR	0x-
Load timer compare value.	DMTIMER1MS_TCLR	0x-
Enable compare.	DMTIMER1MS_TCLR[6] CE	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.6 Internal Diagnostics Modules

This section describes the internal diagnostics modules in the device.

12.6.1 Dual Clock Comparator (DCC)

This section describes the Dual Clock Comparator (DCC) modules in the device.

12.6.1.1 DCC Overview

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

The device has seven instances of DCC modules. Table 12-467

Table 12-479. DCC Modules Allocation Across Device Domains

Module Instance	Domain	
	MCU	MAIN
MCU_DCC0	✓	-
DCC0	-	✓
DCC1	-	✓
DCC2	-	✓
DCC3	-	✓
DCC4	-	✓
DCC5	-	✓

12.6.1.1.1 DCC Features

The DCC uses two independent clock sources to detect when one is out of specification. Each DCC module implements the following features:

- Two independent counter blocks count clock pulses from each clock source
- Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
- Configurable timebase for error signal generation
- Error signal generation when one of the clocks is out of specification
- Clock frequency measurement
- Ability to continue the check in continuous mode despite the error. This is programmable capability.
- Ability to register up-to 4 readings of the error for all associated counts in FIFO.
- Synchronized handoffs between counting clock domains, processing clock domain or reporting clock domains (bus clock).

12.6.1.1.2 DCC Not Supported Features

The DCC does not support the following features:

- Debug suspend functionality depreciated . Software will have to disable DCCs if it starts messing with clocks during debug.

12.6.1.2 DCC Integration

This section describes the DCC integration in the device, including information about clocks, resets, and hardware requests.

12.6.1.2.1 DCC Integration in MCU Domain

There is one DCC module integrated in the device MCU domain - MCU_DCC0. Figure 12-428 shows the integration of MCU_DCC module.

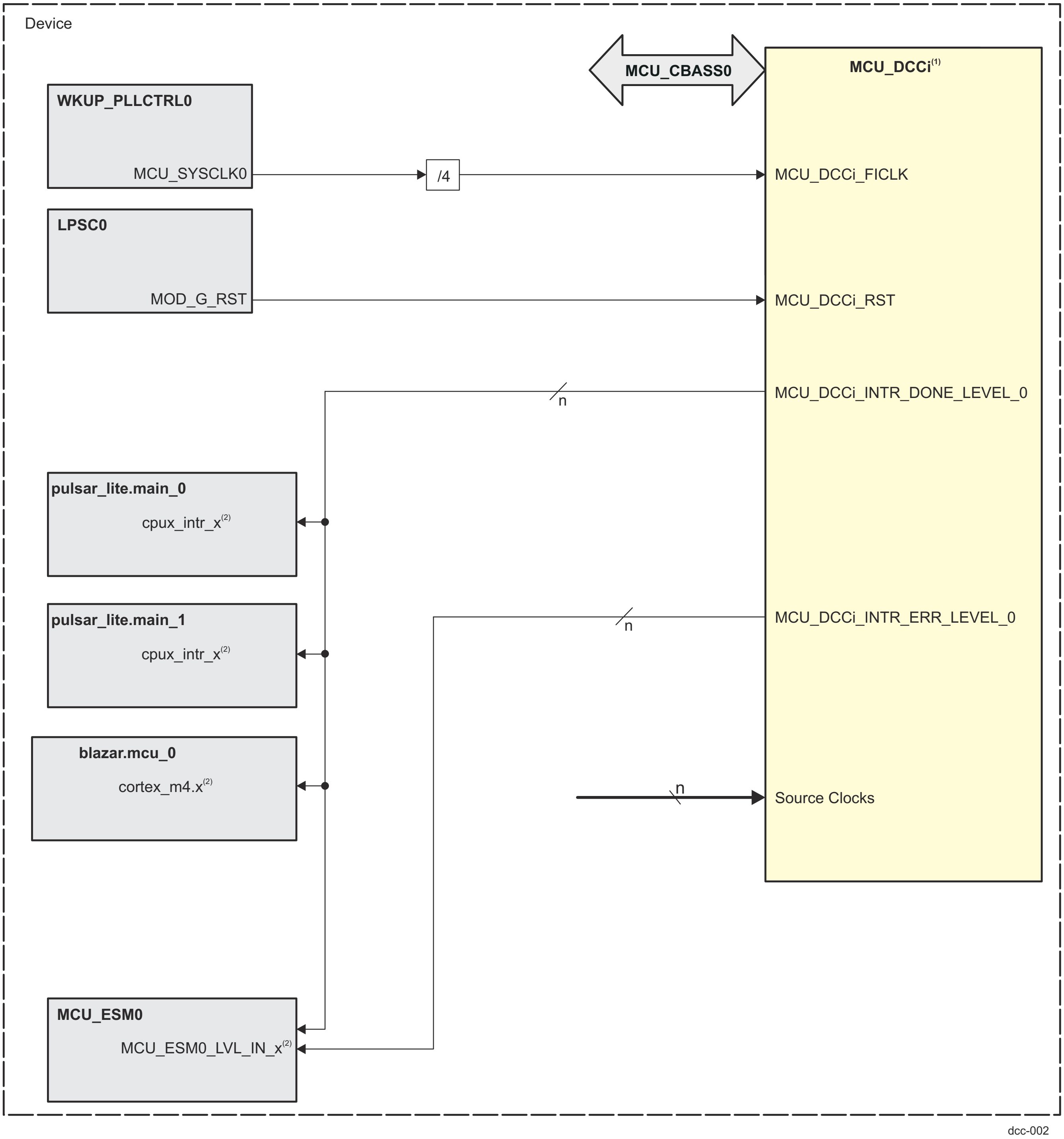

Note

i = 0

Note

x = Interrupt port index, see Table 12-471

Figure 12-428. MCU_DCC Integration

Table 12-468 through Table 12-471 summarize the integration of DCC in the device MCU domain.

Table 12-480. MCU_DCC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_DCC0	WKUP_PSC0	PD0	LPSC0	MCU_CBASS0
MCU_DCC1	WKUP_PSC0	PD0	LPSC0	MCU_CBASS0
MCU_DCC2	WKUP_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-481. MCU_DCC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_DCC0	MCU_DCC0_FICLK	MCU_SYSCLK0/4	WKUP_PLLCTRL0	MCU_DCC0 interface and functional clock

Table 12-482. MCU_DCC Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_DCC0	MCU_DCC0_RST	MOD_G_RST	LPSC0	MCU_DCC0 asynchronous module reset

Table 12-483. MCU_DCC Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_DCC0	MCU_DCC0_INTR_DONE_LEVEL_0			MCU_DCC0 one-shot mode complete interrupt	Level
				MCU_DCC0 one-shot mode complete interrupt	Level
				MCU_DCC0 one-shot mode complete interrupt	Level
				MCU_DCC0 one-shot mode complete interrupt	Level
				MCU_DCC0 one-shot mode complete interrupt	Level
	MCU_DCC0_INTR_ERR_LEVEL_0			MCU_DCC0 error interrupt	Level

Note

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

Section 12.6.1.2.1.1 summarizes the DCC input source clocks in the device MCU domain.

12.6.1.2.1.1 MCU DCC Input Source Clock Mapping

Table 12-484. MCU_DCC0 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
MCU_DCC0	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT
MCU_DCC0	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1
MCU_DCC0	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC
MCU_DCC0	dcc_input03_clk	0	3	MCU_PLLCTRL0	FICLK	main_SYSCLK0/4
MCU_DCC0	dcc_input10_clk	1	0	MCU_PLLCTRL0	chip_div1_clk_clk	MCU_SYSCLK0/2
MCU_DCC0	dcc_clksrc0_clk	1	1	hsdiv4_16fft_mcu_0	hsdivout0_clk	MCU_PLL0_HSDIV0_CLKOUT
MCU_DCC0	dcc_clksrc1_clk	1	2	hsdiv4_16fft_mcu_0	hsdivout1_clk	MCU_PLL0_HSDIV1_CLKOUT
MCU_DCC0	dcc_clksrc2_clk	1	3	hsdiv4_16fft_mcu_0	hsdivout2_clk	MCU_PLL0_HSDIV2_CLKOUT
MCU_DCC0	dcc_clksrc3_clk	1	4	hsdiv4_16fft_mcu_0	hsdivout3_clk	MCU_PLL0_HSDIV3_CLKOUT
MCU_DCC0	dcc_clksrc4_clk	1	5	hsdiv4_16fft_mcu_0	hsdivout4_clk	MCU_PLL0_HSDIV4_CLKOUT
MCU_DCC0	dcc_clksrc5_clk	1	6	RCOSC_32KHz_GEN_DIV3	out0	CLK_32K
MCU_DCC0	dcc_clksrc6_clk	1	7	HFOSC0_32KHz_GEN_DIV8	out0	HFOSC0_CLKOUT_32K
MCU_DCC0	dcc_clksrc7_clk	1	8	PINFUNCTION_MCU_EXT_REFCLK0in	MCU_EXT_REFCLK0	MCU_EXT_REFCLK0
MCU_DCC0	vbus_clk	1	9	MCU_PLLCTRL0	chip_div1_clk_clk	MCU_SYSCLK0/4

12.6.1.2.2 DCC Integration in MAIN Domain

There are six DCC modules integrated in the device MAIN domain - DCC0 through DCC5. Figure 12-429 shows the integration of DCC modules.

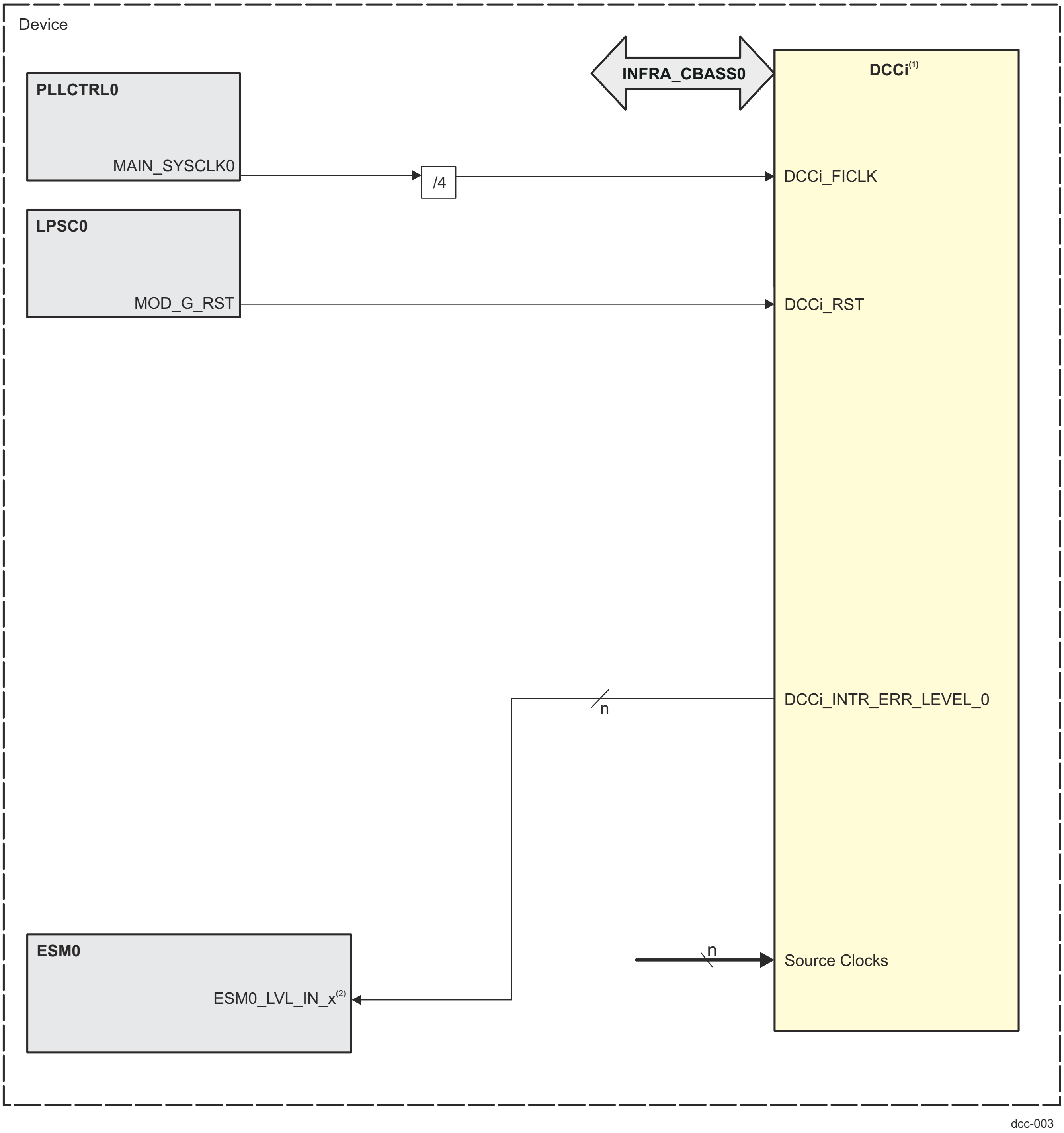

Note

i = 0 to 5

Note

x = Interrupt port index, see Table 12-476

Figure 12-429. DCC Integration

Table 12-473 through Table 12-476 summarize the integration of DCC in the device MAIN domain.

Table 12-485. DCC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
DCC0	PSC0	PD0	LPSC0	INFRA_CBASS0
DCC1	PSC0	PD0	LPSC0	INFRA_CBASS0
DCC2	PSC0	PD0	LPSC0	INFRA_CBASS0
DCC3	PSC0	PD0	LPSC0	INFRA_CBASS0
DCC4	PSC0	PD0	LPSC0	INFRA_CBASS0
DCC5	PSC0	PD0	LPSC0	INFRA_CBASS0

Table 12-486. DCC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
DCC0	DCC0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	DCC0 interface and functional clock
DCC1	DCC1_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	DCC1 interface and functional clock
DCC2	DCC2_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	DCC2 interface and functional clock
DCC3	DCC3_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	DCC3 interface and functional clock
DCC4	DCC4_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	DCC4 interface and functional clock
DCC5	DCC5_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	DCC5 interface and functional clock

Table 12-487. DCC Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
DCC0	DCC0_RST	MOD_G_RST	LPSC0	DCC0 asynchronous module reset
DCC1	DCC1_RST	MOD_G_RST	LPSC0	DCC1 asynchronous module reset
DCC2	DCC2_RST	MOD_G_RST	LPSC0	DCC2 asynchronous module reset
DCC3	DCC3_RST	MOD_G_RST	LPSC0	DCC3 asynchronous module reset
DCC4	DCC4_RST	MOD_G_RST	LPSC0	DCC4 asynchronous module reset
DCC5	DCC5_RST	MOD_G_RST	LPSC0	DCC5 asynchronous module reset

Table 12-488. DCC Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DCC0	DCC0_INTR_ERR_LEVEL_0	ESM0_LVL_IN_112	ESM0	DCC0 error interrupt	Level

Table 12-488. DCC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DCC1	DCC1_INTR_ERR_LEVEL_0	ESM0_LVL_IN_113	ESM0	DCC1 error interrupt	Level
DCC2	DCC2_INTR_ERR_LEVEL_0	ESM0_LVL_IN_114	ESM0	DCC2 error interrupt	Level
DCC3	DCC3_INTR_ERR_LEVEL_0	ESM0_LVL_IN_115	ESM0	DCC3 error interrupt	Level
DCC4	DCC4_INTR_ERR_LEVEL_0	ESM0_LVL_IN_116	ESM0	DCC4 error interrupt	Level
DCC5	DCC5_INTR_ERR_LEVEL_0	ESM0_LVL_IN_117	ESM0	DCC5 error interrupt	Level

Note

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

Section 12.6.1.2.2.1 summarizes the DCC input source clocks in the device MAIN domain.

12.6.1.2.2.1 DCC Input Source Clock Mapping

- DCC0 Input Source Clock Mapping
- DCC1 Input Source Clock Mapping
- DCC2 Input Source Clock Mapping
- DCC3 Input Source Clock Mapping
- DCC4 Input Source Clock Mapping
- DCC5 Input Source Clock Mapping

Table 12-489. DCC0 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC0	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT
DCC0	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1
DCC0	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC
DCC0	dcc_input03_clk	0	3	PLLCTRL0	FICLK	main_SYSCLK0/4
DCC0	dcc_input10_clk	1	0	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/2
DCC0	dcc_clksrc0_clk	1	1	hsdiv4_16fft_main_0	hsdivout1_clk	MAIN_PLL0_HSDIV1_CLKOUT
DCC0	dcc_clksrc1_clk	1	2	hsdiv4_16fft_main_0	hsdivout2_clk	MAIN_PLL0_HSDIV2_CLKOUT
DCC0	dcc_clksrc2_clk	1	3	hsdiv4_16fft_main_0	hsdivout3_clk	MAIN_PLL0_HSDIV3_CLKOUT
DCC0	dcc_clksrc3_clk	1	4	hsdiv4_16fft_main_0	hsdivout4_clk	MAIN_PLL0_HSDIV4_CLKOUT
DCC0	dcc_clksrc4_clk	1	5	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT
DCC0	dcc_clksrc5_clk	1	6	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1
DCC0	dcc_clksrc6_clk	1	7	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0
DCC0	dcc_clksrc7_clk	1	8	postdiv4_16ff_main_2	hsdivout8_clk	MAIN_PLL2_HSDIV8_CLKOUT
DCC0	vbus_clk	1	9	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4

Table 12-490. DCC1 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC1	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT
DCC1	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1
DCC1	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC
DCC1	dcc_input03_clk	0	3	PLLCTRL0	FICLK	main_SYSCLK0/4
DCC1	dcc_input10_clk	1	0	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4
DCC1	dcc_clksrc0_clk	1	1	postdiv4_16ff_main_0	hsdivout5_clk	MAIN_PLL0_HSDIV5_CLKOUT

Table 12-490. DCC1 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC1	dcc_clksrc1_clk	1	2	postdiv4_16ff_main_0	hsdivout6_clk	MAIN_PLL0_HSDIV6_CLKOUT
DCC1	dcc_clksrc2_clk	1	3	postdiv4_16ff_main_0	hsdivout7_clk	MAIN_PLL0_HSDIV7_CLKOUT
DCC1	dcc_clksrc3_clk	1	4	hsdiv4_16fft_main_1	hsdivout1_clk	MAIN_PLL1_HSDIV1_CLKOUT
DCC1	dcc_clksrc4_clk	1	5	postdiv4_16ff_main_0	hsdivout9_clk	MAIN_PLL0_HSDIV9_CLKOUT
DCC1	dcc_clksrc5_clk	1	6	hsdiv4_16fft_main_1	hsdivout0_clk	MAIN_PLL1_HSDIV0_CLKOUT
DCC1	dcc_clksrc6_clk	1	7	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC
DCC1	dcc_clksrc7_clk	1	8	hsdiv4_16fft_main_1	hsdivout2_clk	MAIN_PLL1_HSDIV2_CLKOUT
DCC1	vbus_clk	1	9	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4

Table 12-491. DCC2 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC2	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT
DCC2	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1
DCC2	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC
DCC2	dcc_input03_clk	0	3	PLLCTRL0	FICLK	main_SYSCLK0/4
DCC2	dcc_input10_clk	1	0	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4
DCC2	dcc_clksrc0_clk	1	1	hsdiv4_16fft_main_1	hsdivout3_clk	MAIN_PLL1_HSDIV3_CLKOUT
DCC2	dcc_clksrc1_clk	1	2	hsdiv1_16fft_main_14	hsdivout0_clk	MAIN_PLL14_HSDIV0_CLKOUT/2
DCC2	dcc_clksrc2_clk	1	3	postdiv1_16fft_main_1	hsdivout5_clk	MAIN_PLL1_HSDIV5_CLKOUT
DCC2	dcc_clksrc3_clk	1	4	postdiv1_16fft_main_1	hsdivout6_clk	MAIN_PLL1_HSDIV6_CLKOUT
DCC2	dcc_clksrc4_clk	1	5	hsdiv4_16fft_main_2	hsdivout0_clk	MAIN_PLL2_HSDIV0_CLKOUT
DCC2	dcc_clksrc5_clk	1	6	hsdiv1_16fft_main_14	hsdivout1_clk	MAIN_PLL14_HSDIV1_CLKOUT/2
DCC2	dcc_clksrc6_clk	1	7	hsdiv4_16fft_main_2	hsdivout2_clk	MAIN_PLL2_HSDIV2_CLKOUT
DCC2	dcc_clksrc7_clk	1	8	PINFUNCTION_PRG1_RGMII2_RXCin	PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
DCC2	vbus_clk	1	9	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4

Table 12-492. DCC3 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC3	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT

Table 12-492. DCC3 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC3	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1
DCC3	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC
DCC3	dcc_input03_clk	0	3	PLLCTRL0	FICLK	main_SYSCLK0/4
DCC3	dcc_input10_clk	1	0	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4
DCC3	dcc_clksrc0_clk	1	1	hsdiv4_16fft_main_1	hsdivout0_clk	MAIN_PLL1_HSDIV0_CLKOUT
DCC3	dcc_clksrc1_clk	1	2	postdiv4_16ff_main_2	hsdivout5_clk	MAIN_PLL2_HSDIV5_CLKOUT
DCC3	dcc_clksrc2_clk	1	3	PINFUNCTION_PRG1_RGMII1_RXCin	PRG1_RGMII1_RXC	PRG1_RGMII1_RXC/2
DCC3	dcc_clksrc3_clk	1	4	postdiv4_16ff_main_2	hsdivout7_clk	MAIN_PLL2_HSDIV7_CLKOUT
DCC3	dcc_clksrc4_clk	1	5	postdiv4_16ff_main_2	hsdivout6_clk	MAIN_PLL2_HSDIV6_CLKOUT
DCC3	dcc_clksrc5_clk	1	6	postdiv4_16ff_main_2	hsdivout9_clk	MAIN_PLL2_HSDIV9_CLKOUT
DCC3	dcc_clksrc6_clk	1	7	hsdiv0_16fft_main_8	hsdivout0_clk	MAIN_PLL8_HSDIV0_CLKOUT/4
DCC3	dcc_clksrc7_clk	1	8	hsdiv0_16fft_main_12	hsdivout0_clk	MAIN_PLL12_HSDIV0_CLKOUT
DCC3	vbus_clk	1	9	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4

Table 12-493. DCC4 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC4	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT
DCC4	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1
DCC4	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC
DCC4	dcc_input03_clk	0	3	PLLCTRL0	FICLK	main_SYSCLK0/4
DCC4	dcc_input10_clk	1	0	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/2
DCC4	dcc_clksrc0_clk	1	1	MAIN_GPMC_FCLK_SEL	out0	GPMC_fclk
DCC4	dcc_clksrc1_clk	1	2	PINFUNCTION_CPTS0_RFT_CLKin	CPTS0_RFT_CLK	CPTS_RFT_CLK
DCC4	dcc_clksrc2_clk	1	3	RCOSC_32KHz_GEN_DIV3	out0	CLK_32K
DCC4	dcc_clksrc3_clk	1	4	HFOSC0_32KHz_GEN_DIV8	out0	HFOSC0_CLKOUT_32K
DCC4	dcc_clksrc4_clk	1	5	PINFUNCTION_MCU_EXT_REFCLK0in	MCU_EXT_REFCLK0	MCU_EXT_REFCLK0
DCC4	dcc_clksrc5_clk	1	6	PINFUNCTION_RMII_REF_CLKin	RMII_REF_CLK	RMII_REF_CLK/4
DCC4	dcc_clksrc6_clk	1	7	PINFUNCTION_RGMII1_RXCin	RGMII1_RXC	RGMII1_RXC
DCC4	dcc_clksrc7_clk	1	8	PINFUNCTION_PRG0_RGMII1_RXCin	PRG0_RGMII1_RXC	PRG0_RGMII1_RXC/2

Table 12-493. DCC4 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC4	vbus_clk	1	9	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4

Table 12-494. DCC5 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source
DCC5	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT
DCC5	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1
DCC5	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC
DCC5	dcc_input03_clk	0	3	PLLCTRL0	FICLK	main_SYSCLK0/4
DCC5	dcc_input10_clk	1	0	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0
DCC5	dcc_clksrc0_clk	1	1	PINFUNCTION_PRG0_RGMII2_RXCin	PRG0_RGMII2_RXC	PRG0_RGMII2_RXC
DCC5	dcc_clksrc1_clk	1	2	PINFUNCTION_FSI_RX0_CLKin	FSI_RX0_CLK	FSI_RX0_CLK
DCC5	dcc_clksrc2_clk	1	3	PINFUNCTION_FSI_RX1_CLKin	FSI_RX1_CLK	FSI_RX1_CLK/2
DCC5	dcc_clksrc3_clk	1	4	PINFUNCTION_FSI_RX2_CLKin	FSI_RX2_CLK	FSI_RX2_CLK
DCC5	dcc_clksrc4_clk	1	5	PINFUNCTION_FSI_RX3_CLKin	FSI_RX3_CLK	FSI_RX3_CLK
DCC5	dcc_clksrc5_clk	1	6	PINFUNCTION_FSI_RX4_CLKin	FSI_RX4_CLK	FSI_RX4_CLK
DCC5	dcc_clksrc6_clk	1	7	PINFUNCTION_FSI_RX5_CLKin	FSI_RX5_CLK	FSI_RX5_CLK
DCC5	dcc_clksrc7_clk	1	8	PINFUNCTION_PRG1_RGMII2_RXCin	PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
DCC5	vbus_clk	1	9	PLLCTRL0	chip_div1_clk_clk	main_SYSCLK0/4

12.6.1.3 DCC Functional Description

The DCC module supports two selectable clock sources for Counter0 and Counter1. Counter0 receives CLOCK0[2] at reset. Counter1 receives CLOCK1 at reset. Figure 12-430 shows the DCC functional block diagram.

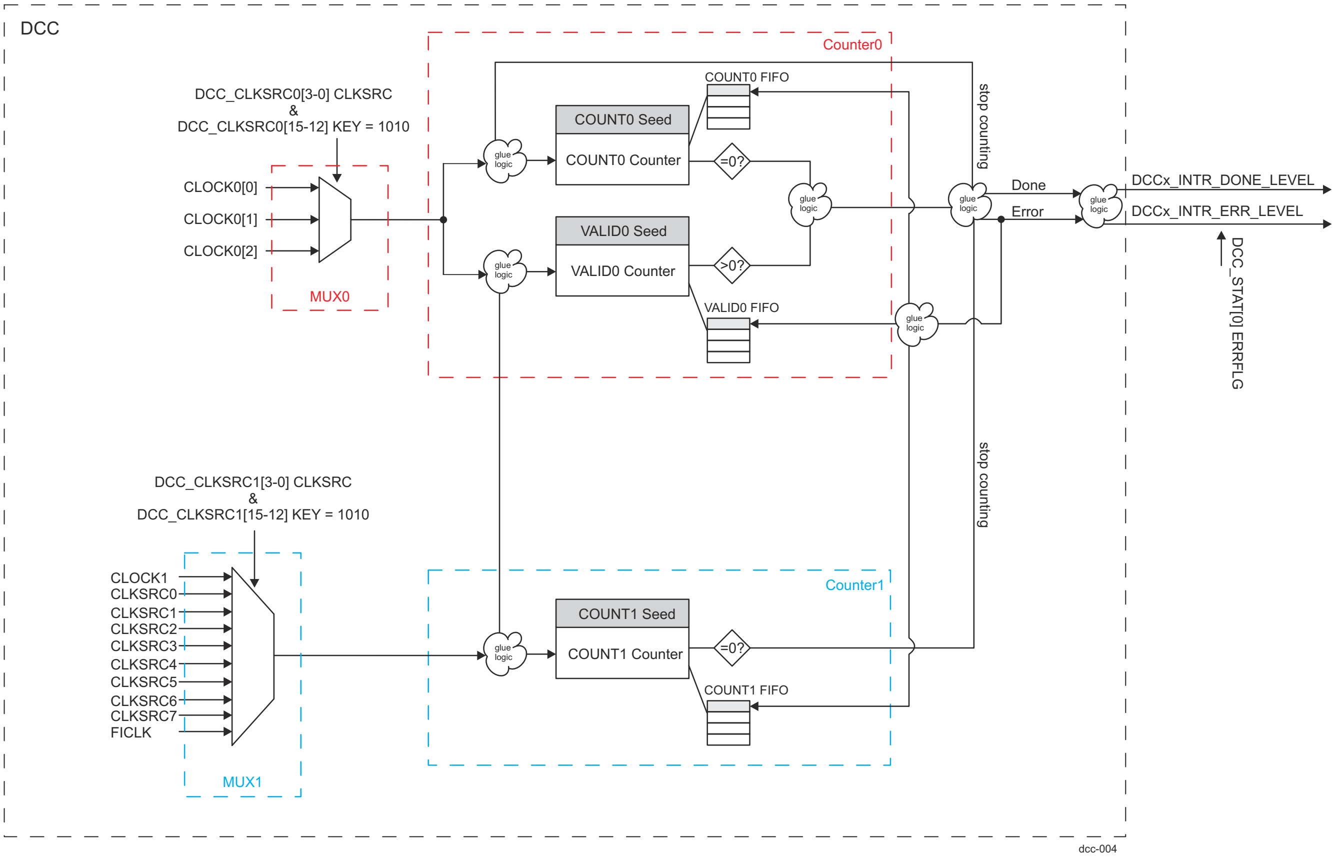

Figure 12-430. DCC Functional Block Diagram

12.6.1.3.1 DCC Counter Operation

DCC has two sets of counters with each set having programmable clock selection.

- The first set has two counters COUNT0 and VALID0. These operate from Clock0 (reference clock).
- The second set has one counter COUNT1 that is operated from Clock1 (measured clock). The selection of input clock from list of different counters increases the utility of DCC for debug and test across different clock sources available on the device.

COUNT0 and COUNT1 are configured based on the ratio between the frequencies of Clock0 and Clock1 (Clock1 frequency * COUNT0 = Clock0 frequency * COUNT1). Further, the tunable counter VALID0 on the Clock0 (reference clock) defines the window of margin for COUNT1 to end after COUNT0. This COUNT1 needs to complete within valid window for operation where clock relationship is as expected.

The error signal is generated by any one of the following conditions:

- Clock1 expires before the COUNT0 reaches 0.
- Clock1 expires after both COUNT0 and VALID0 reach 0.
- Clock1 not present.
- Clock0 not present.

Any of these errors causes the counters to stop counting by default. An application may then read out the counter values to help determine what caused the error. It would take multiple clocks (2-3 in each clock domain i.e. source and VBUSP_CLK) to stop the counters due to the cross-clock domain synchronizations. Counters can also be configured in a mode to reload and continue down-counting despite error so successive error event is not missed. Error is reported as exception and application is expected to read the counter values for determining quantum and direction of error.

Note

Reads of the counter value may not be exact since the read operation is synchronized to the VBUSP_CLK

Reloads or restarts occur under the following conditions:

- The module is reset or restarted through software (that is, software starts the module after reset, or software checks an error condition and decides to restart the module).
- In continuous mode without any error.
- In continuous mode with error, given CONT_ON_ERR is set, upon which counters restart counting as soon as the error is hit and the error counts are archived.

CAUTION

The DCC module does not check jitter for Clock0 or Clock1.

As the counter preset signal is synchronized to either of the source clock domains, the counters begin downcounting after two corresponding source clock cycles.

The error signal is to be captured to the VBUSP_CLK domain. There is 1 VBUSP_CLK period uncertainty on either side of the fixed width counting window (VALID0) in generating the error signal since the counters work in a different clock domain. This should be accounted for, when setting the count value for VALID0.

Operating the DCC with ‘0’ in the COUNTSEED1 or COUNTSEED0 or VALIDSEED0 register will result in undefined operation

Figure 12-431 through Figure 12-435 shows examples of counters relationship and error generation.

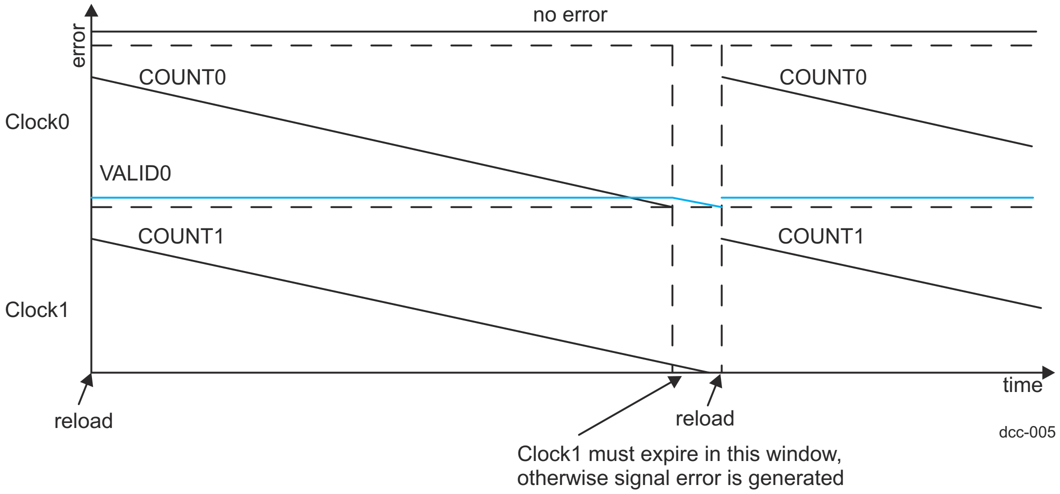

Figure 12-431. DCC Clock0 and Clock1 With no Error

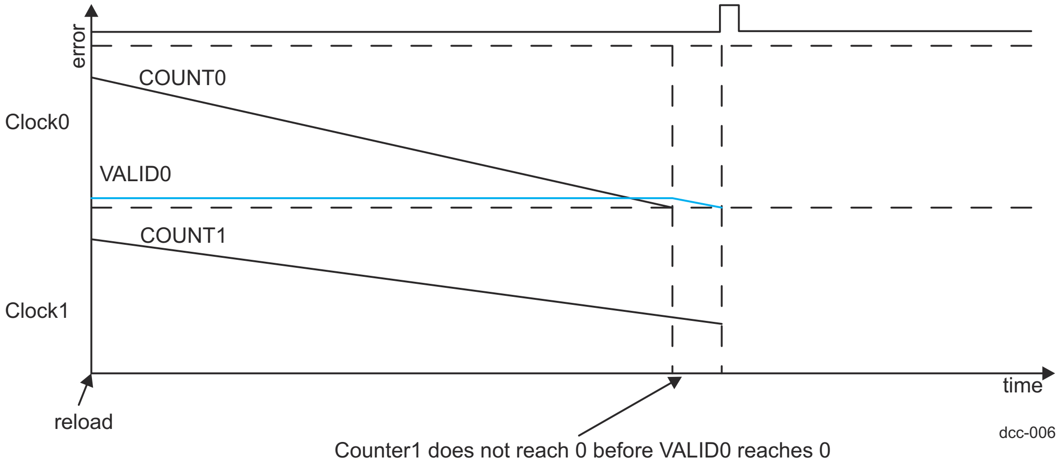

Figure 12-432. DCC Clock1 slower than Clock0 results in an error and stops counting

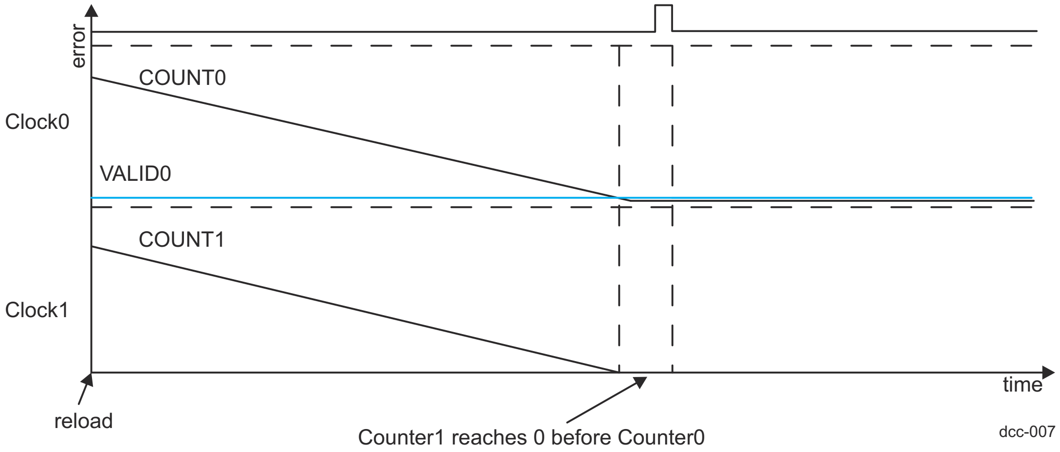

Figure 12-433. DCC Clock1 faster than Clock0 results in an error and stops counting

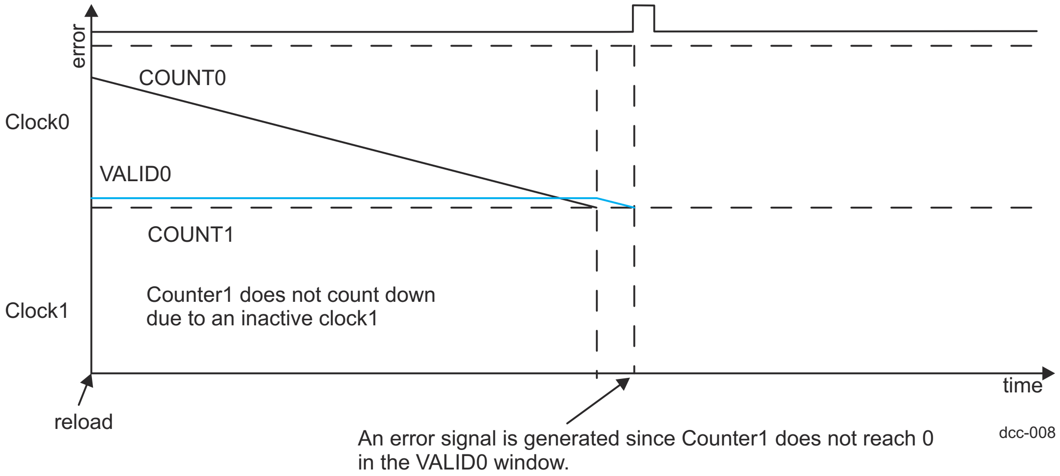

Figure 12-434. DCC Clock1 not present results in an error and stops counting

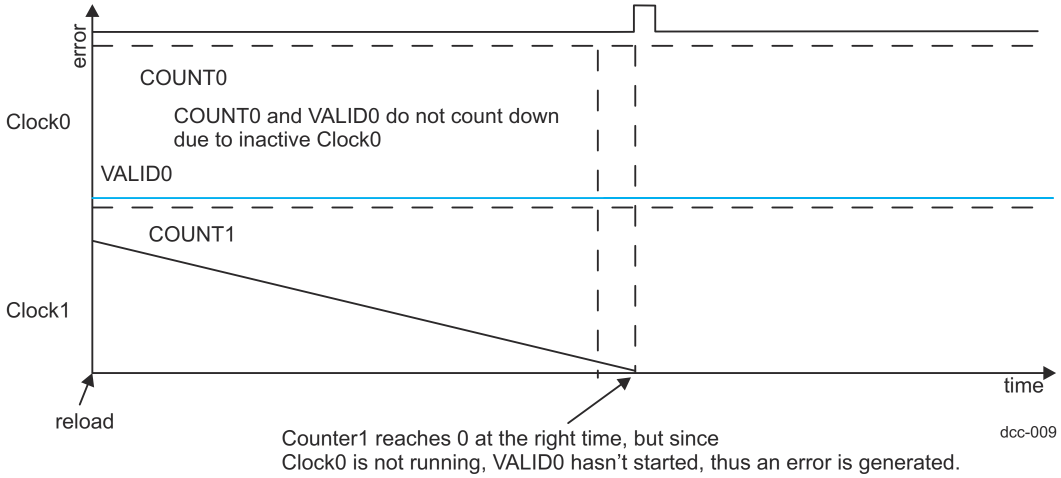

Figure 12-435. DCC Clock0 not present results in an error and stops counting

12.6.1.3.2 DCC Low Power Mode Operation

The DCC module does not function in Low Power Mode. It is the responsibility of software to stop the module before entering low power mode and to restart the module after exiting low power mode.

12.6.1.3.3 DCC Suspend Mode Behavior

The DCC module will continue running regardless of the state of emulation. All registers are readable via emulation reads.

12.6.1.3.4 DCC Single-Shot Mode

The DCC may be programmed to count down one time using single-shot mode. In this mode, the DCC stops operation when:

- Both COUNT0 and VALID0 reach 0
- COUNT1 reaches 0

At the end of one sequence in single-shot mode, the DCC will de-assert the enable value (DCCENA), disabling further counting. At the end of one sequence in single-shot mode, if it is no error that stops counting, then the done status bit is set and a done interrupt is driven. Application must clear the done bit before restarting counts. At the end of a sequence in single-shot mode, if there is an error, then the error status bit will be set. Application must clear the error status bit before starting the next sequence.

12.6.1.3.5 DCC Continuous Mode

When DCC runs in continuous mode both the counts shall get reloaded with seed value upon completion of counts without error. If the counts end in error DCC stops the operation and counts are not reloaded.

12.6.1.3.5.1 DCC Continue on Error

During debug, if there are events which are causing clocks to be anomalous over short period covering more than one evaluation window then it would be important to capture trajectory of error event and period around such event. To allow capturing the successive error events DCC can be programmed to continue after error. DCC_GCTRL2[3-0] CONT_ON_ERR shall be set to value other than "0101" to enable this mode. It is recommended to write "1010" to avoid single soft errors.

12.6.1.3.5.2 DCC Error Count

DCC also counts the number of error pulses generated since reset or since last time the error count is cleared. This is read/write register (DCCERRCNT) for CPU to clear when new trace of number of errors is required to be maintained.

12.6.1.3.6 DCC Control and count hand-off across clock domains

As the counters run in two different selectable clock domains and the register interface runs on the fixed bus clock domain, control signals and counter value hand-off have synchronizers implemented. These add to the margins of error while comparing the counts.

1. With all three counts synchronized to Functional Interface Clock (FICLK) domain for comparison error detection there is delay in terms of FICLK domain.
2. Based on the error signal, the enable for the counters is synchronized back to the respective clock domains of the counters, which adds latency in terms of clock periods which are different, this would create a skew between start of count. Depending upon frequency ratios of the clocks used, the difference between two could vary.

Application needs to consider the worst case delay differences while measuring the clocks.

12.6.1.3.7 DCC Error Trajectory Record

Once the clock errors out, the host can read the counter values to determine the extent of error to analyze type of failure. For short window comparisons this would become difficult, specially if there are back to back errors due to some transient event. Secondly, for random events which can cause an interrupt during the critical phase of application running, then event if not recorded may get overwritten and also not provide meaningful trace of error.

12.6.1.3.7.1 DCC FIFO Capturing for Errors

DCC provides the FIFO for capturing COUNT0, VALID0, and COUNT1 information which captures all three counts upon "Error" event. For "Done" event no results are captured by default.

12.6.1.3.7.2 DCC FIFO in Continuous Capture Mode

To track the VALID0 counter values regardless of "Error" or not, FIFOs can be configured to capture the count for each compare window. This is useful in validation and characterization exercise. DCC_GCTRL2 [11-7] FIFO_NONERR control when set to value other than "0101" this mode is set; it is recommended to write "1010" to avoid single soft errors. Note, this capture is applicable only in continuous mode and not in single shot mode.

12.6.1.3.7.3 DCC FIFO Details

The FIFO is 4 deep for each count and updates new count information for all the non-full FIFOs. Information is updated on every configured trigger of error or cycle completion. If full, the next values are not written till at-least one entry is read. Application owns responsibility to read the FIFOs uniformly to keep synchronisation between three entries of the FIFO. Both empty and full indications for individual FIFOs is provided through the DCCSTATUS2.

12.6.1.3.7.4 DCC FIFO Debug mode behavior

Upon debug access, the FIFO pointers should not advance hence not impacting the functional behavior. This requirement is same as other functional blocks in the device.

12.6.1.3.8 DCC Count Read Registers

DCC has provision to read the counts during operation. This is performed using DCCCNT0, DCCVALID0DCC2_DCCCNT0DCC2_DCCVALID0, and DCC2_DCCCNT1 DCCCNT1 registers. Read from these registers in default mode allows reading the present value of count. This is useful when in single shot mode or mode where DCC stops upon error.

These registers can be used to read the FIFO through the DCC2_DCCGCTRL2[7-4] FIFO_READ configuration. Reads on the empty FIFO shall provide the contents of last pointed location. Application shall track the empty/full conditions of the FIFOs to track the count records consistently.

Regardless of FIFO_READ configuration, the FIFO internally keeps updating records based on configured triggers until full.

Note

- Input0_clk and input1_clk are two asynchronous clock domains. In a system, VBUS clock may also be asynchronous relative to both Input0_clk and Input1_clk. The module must be able to generate an error when either Input0_clk or Input1_clk is not present. VBUS clock should not sample or affect the clock counting logic in any way.
- In general, the reference clock should be hooked up to Input0_clk and measured clock should be connected to Input1_clk. The default clock source i.e. ‘0’ should be assigned to connect with device native clock such as internal oscillator reference on both.
- The error interrupt signal is independent of the error flag bit. If the interrupt is masked, the error flag is still set when an error occurs. The error flag stays set until it is cleared, regardless of the status of the interrupt.
- The done flag in the DCCSTAT register would be set when the single shot mode completes without error and is independent of the DONEENA bits in the DCCGCTRL register. The done level interrupt would be set only if it is enabled by the DONEENA bits.
- Upon debug access, the FIFO pointers do not advance, hence not impacting the functional behavior.

12.6.2 Error Signaling Module (ESM)

This section describes the Error Signaling Module (ESM) in the device.

12.6.2.1 ESM Overview

The Error Signaling Module (ESM) aggregates events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with an event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in a safe, known state.

Table 12-483 shows ESM allocation across device domains.

Table 12-495. ESM Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
MCU_ESM0	✓	-
ESM0	-	✓

Figure 12-437 shows the ESM modules overview.

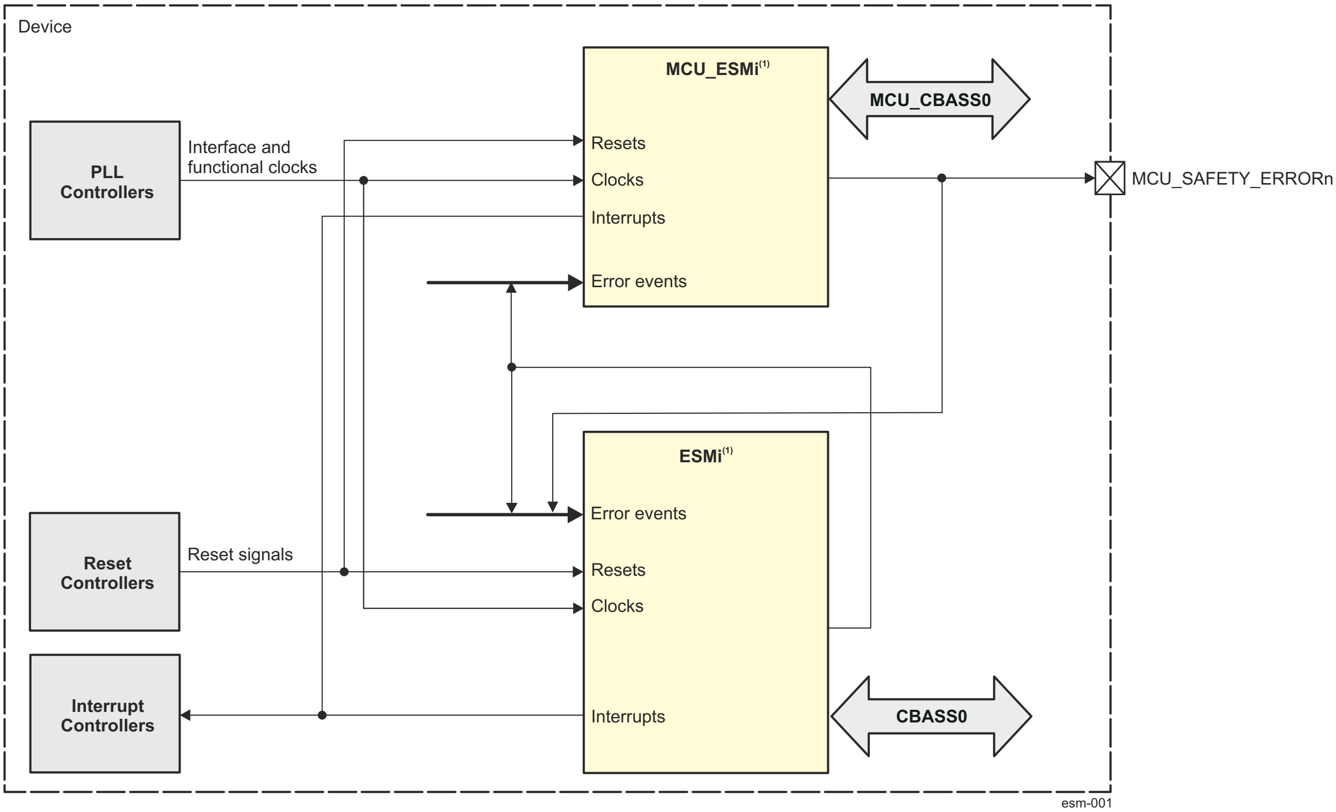

Note

i = 0

Figure 12-436. ESM Modules Overview

Figure 12-437. ESM Overview

12.6.2.1.1 ESM Features

Each ESM module implements the following features:

- Up to 1024 error event inputs
  - Implemented in groups of 32 events

  - Level or Pulse inputs (Pulse inputs are triple redundant)
- Selectable low and high priority interrupt error pin prioritization of each error event
- Error pin to signal severe device failure
  - Support of level or PWM modes
- Configurable timebase for error signal
- Error forcing capability
- Internal redundant flops on critical fields

12.6.2.2 ESM Environment

The MCU_ESM0 and ESM0 modules are hereinafter referred to as ESM module.

This section describes the ESM external connections (environment).

Figure 12-438 shows the ESM pins used for typical connections with external devices.

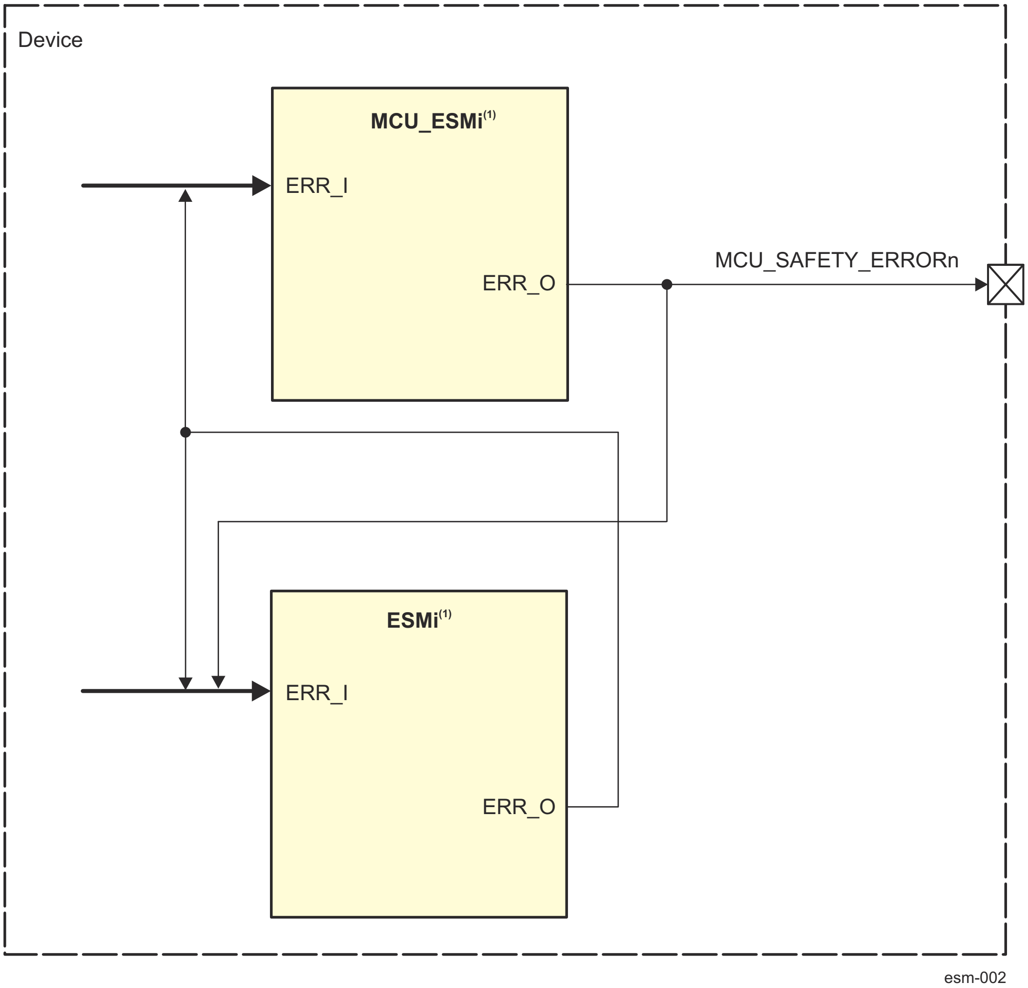

Note

i = 0

Figure 12-438. ESM Modules Environment

Table 12-484 describes the ESM I/O signals.

Table 12-496. ESM I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
			MCU_ESM0	
ERR_O[3]	MCU_SAFETY_ERRORn	O	Active low error output signal.	0[2]

(1) O = Output;

(2) During POR, the pin state is weak pull-down and the I/O is under the control of the device. Once PORz are de-asserted, SAFETY_ERRORn will be driven by the ESM module.

(3) The ERR_O output of MCU_ESM0 drives the MCU_SAFETY_ERRORn pin, but is also connected to the ERR_I of the ESM0. While ERR_O of ESM0 is connected to ERR_I of MCU_ESM0 and is also a loopback to its own ERR_I.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.6.2.3 ESM Integration

This section describes the ESM integration in the device, including information about clocks, resets, and hardware requests.

12.6.2.3.1 ESM Integration in MCU Domain

There is one ESM module integrated in the device MCU domain - MCU_ESM0. Figure 12-439 shows the integration of MCU_ESM0.

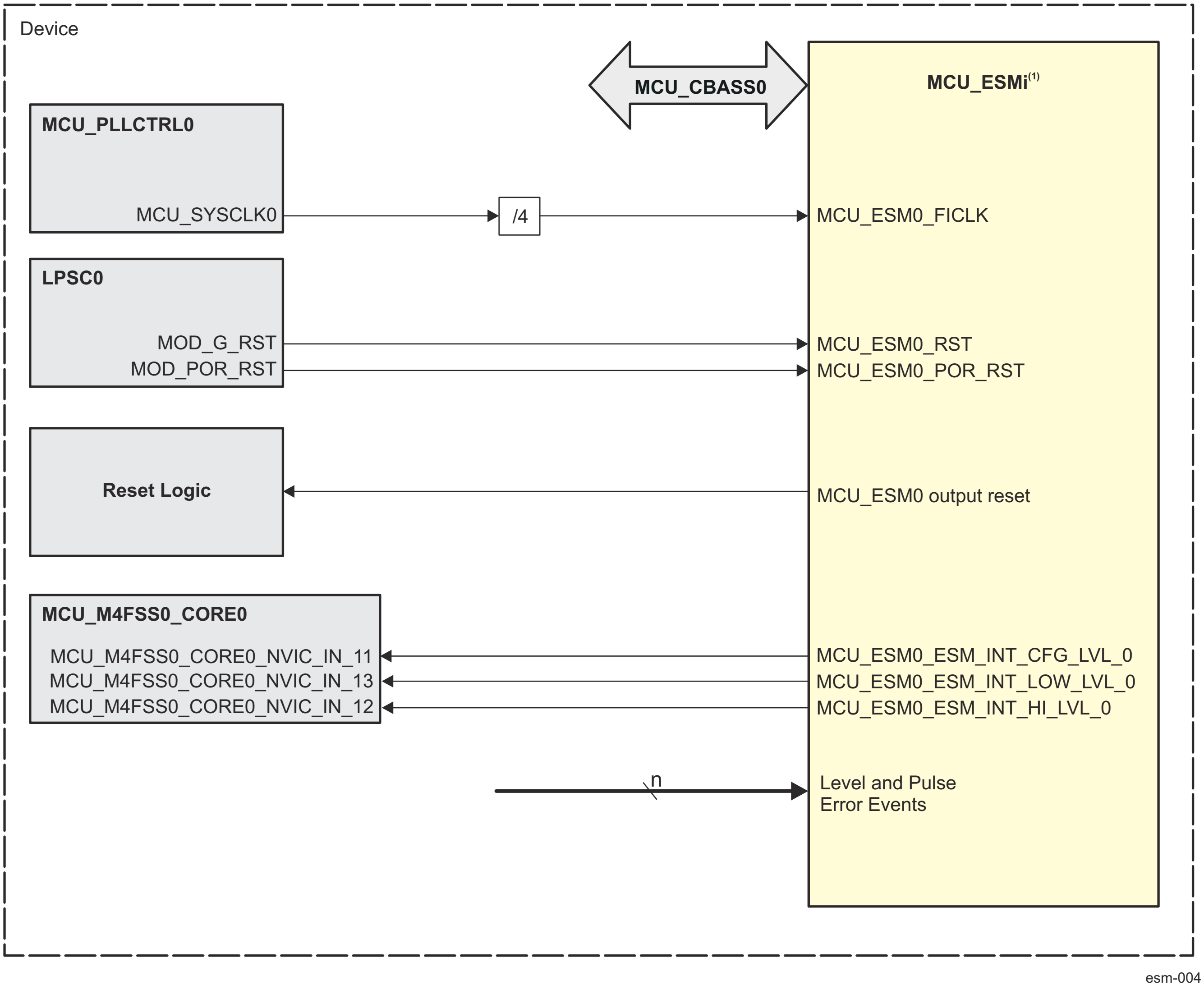

Note

i = 0

Figure 12-439. MCU_ESM Integration

Table 12-485 through Table 12-488 summarize the integration of ESM in the device MCU domain.

Table 12-497. MCU_ESM Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_ESM0	MCU_PSC0	PD0	LPSC0	MCU_CBASS0

Table 12-498. MCU_ESM Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_ESM0	MCU_ESM0_FICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_ESM0 Interface and Functional clock

Table 12-499. MCU_ESM Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_ESM0	MCU_ESM0_RST	MOD_G_RST	LPSC0	MCU_ESM0 Asynchronous module reset
	MCU_ESM0_POR_RST	MOD_POR_RST	LPSC0	MCU_ESM0 Power-on module reset

Table 12-500. MCU_ESM Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_ESM0	MCU_ESM0_ESM_INT_CFG_LVL_0	MCU_M4FSS0_CORE0_NVIC_IN_11	MCU_M4FSS0_CORE0	MCU_ESM0 configuration error interrupt	Level
	MCU_ESM0_ESM_INT_LOW_LVL_0	MCU_M4FSS0_CORE0_NVIC_IN_13	MCU_M4FSS0_CORE0	MCU_ESM0 low priority interrupt	Level
	MCU_ESM0_ESM_INT_HI_LVL_0	MCU_M4FSS0_CORE0_NVIC_IN_12	MCU_M4FSS0_CORE0	MCU_ESM0 high priority interrupt	Level

Note

Table 12-488 lists only the MCU_ESM0 interrupt outputs and input resets. For the mapping of system interrupt error events to MCU_ESM0 interrupt inputs, see Section 9.4 , *Interrupt Sources*. For more information of MCU_ESM0 output reset to device reset logic, see Section 5.3 , *Reset*.

Note

For a description of the interrupt requests, see Section 12.6.2.4.1 , *Interrupt Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.6.2.3.2 ESM Integration in MAIN Domain

There is one ESM module integrated in the device MAIN domain - ESM0. Figure 12-440 shows the integration of ESM0.

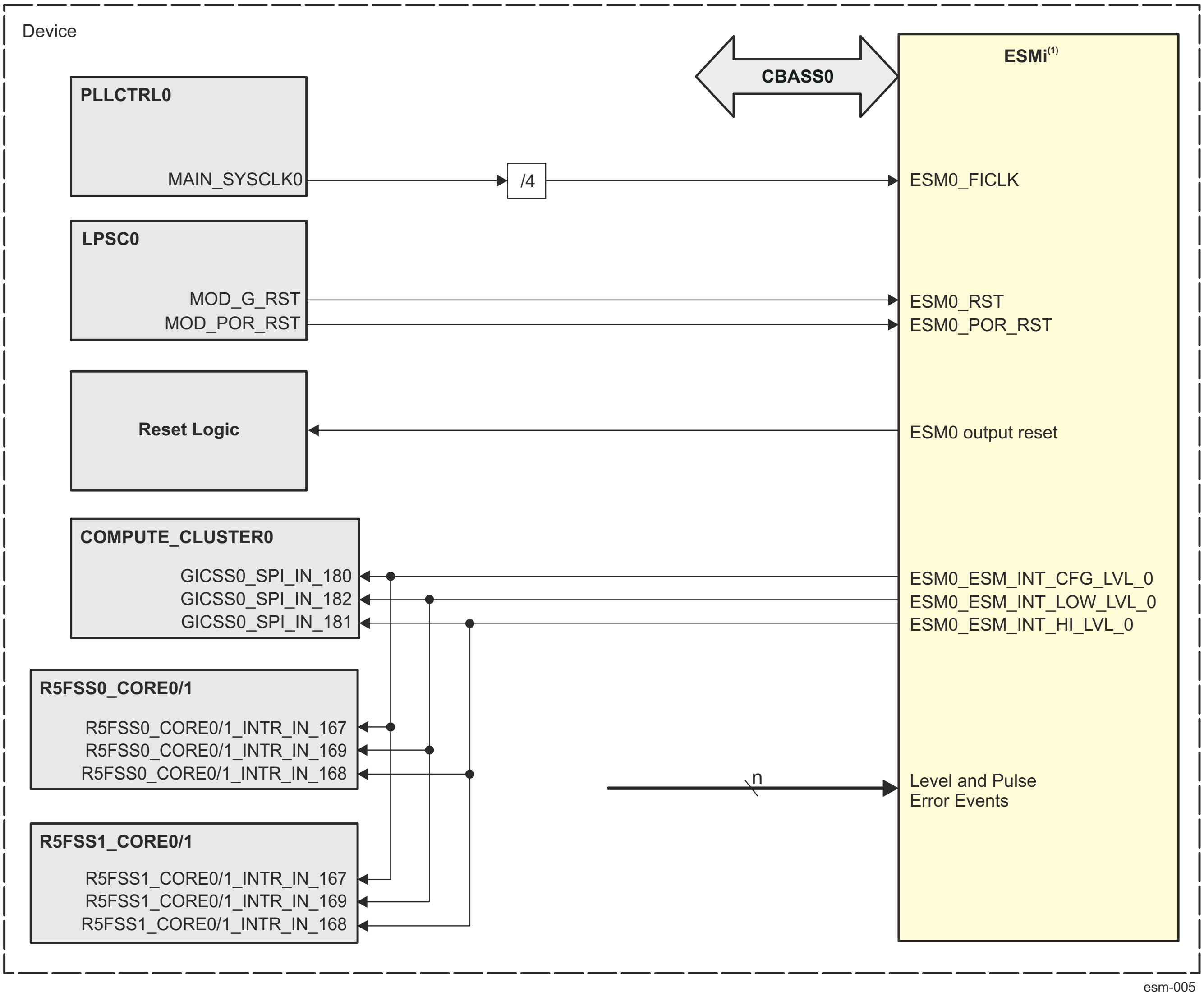

Note

i = 0

Figure 12-440. ESM Integration

Table 12-489 through Table 12-492 summarize the integration of ESM in the device MAIN domain.

Table 12-501. ESM Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
ESM0	PSC0	PD0	LPSC0	CBASS0

Table 12-502. ESM Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
ESM0	ESM0_FICLK	MAIN_SYSCLK0/4	PLLCTRL0	ESM0 Interface and Functional clock

Table 12-503. ESM Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
ESM0	ESM0_RST	MOD_G_RST	LPSC0	ESM0 Asynchronous module reset
	ESM0_POR_RST	MOD_POR_RST	LPSC0	ESM0 Power-on module reset

Table 12-504. ESM Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ESM0	ESM0_ESM_INT_CFG_LVL_0	GICSS0_SPI_IN_180	COMPUTE_CLUSTER0	ESM0 configuration error interrupt	Level
		R5FSS0_CORE0_INTR_IN_167	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_167	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_167	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_167	R5FSS1_CORE1		
	ESM0_ESM_INT_LOW_LVL_0	GICSS0_SPI_IN_182	COMPUTE_CLUSTER0	ESM0 low priority interrupt	Level
		R5FSS0_CORE0_INTR_IN_169	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_169	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_169	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_169	R5FSS1_CORE1		
	ESM0_ESM_INT_HI_LVL_0	GICSS0_SPI_IN_181	COMPUTE_CLUSTER0	ESM0 high priority interrupt	Level
		R5FSS0_CORE0_INTR_IN_168	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_168	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_168	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_168	R5FSS1_CORE1		

Note

Table 12-492 lists only the ESM0 interrupt outputs and input resets. For the mapping of system interrupt error events to ESM0 interrupt inputs, see Section 9.4 , *Interrupt Sources*. For more information of ESM0 output reset to device reset logic, see Section 5.3 , *Reset*.

Note

For a description of the interrupt requests, see Section 12.6.2.4.1 , *Interrupt Requests*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.6.2.4 ESM Functional Description

The Error Signaling Module (ESM) centralizes fault reports. The module provides mechanisms to classify errors by severity and to provide programmable error response. The error classification in the ESM is determined by programmed configuration for each individual error input. For each individual error input the configuration can be set to assert an output error pin, or generate an interrupt to a CPU, or both. When an individual error input is configured to generate an interrupt, the configuration also selects whether the interrupt that is generated is high priority or low priority.

By reporting the faults in a central location, the system can determine what caused the fault and what action can be taken. In general, the faults can be split into two categories:

- Corrected faults
- Non-corrected faults

The ESM reports errors in two ways:

- An interrupt to a processor in the device. This allows the device to analyze and try to recover from an error.
- An external ERROR pin. This allows the system outside of the SoC to monitor for potentially fatal errors(errors that the device cannot self-recover from). Moreover, the external I/O (ERROR pin) can operate in level or PWM modes. In level mode, the output remains asserted (active low) for a minimum period of time. After that period of time, if the error has been cleared by an internal processor, the pin goes inactive (high). If signal does not go inactive in that time, then an external agent must intervene, as an unrecoverable error can occur. In PWM mode, the error causes the output pin to maintain the value for a minimum period of time. After that period of time, if the error has been cleared by an internal processor, the pin continues the PWM pattern. If the signal does not go inactive in that time, then an external agent must intervene, as an unrecoverable error can occur.

Both mechanisms can be used at the same time for the same fault, signaling both an interrupt and the external ERROR pin. This allows the device to attempt to recover, but if recovery fails, then the external system is still alerted. If recovery succeeds, then the ERROR pin assertion can be removed so that the external system knows that a potentially unsafe condition was avoided.

Lastly, the ESM does not specify any methods of intervention, only the process of alerting internal CPUs and external monitors of an existing error event.

Figure 12-441 shows the ESM module block diagram. Not all instances may pinned out in the device. For more information, see *ESM Environment*.

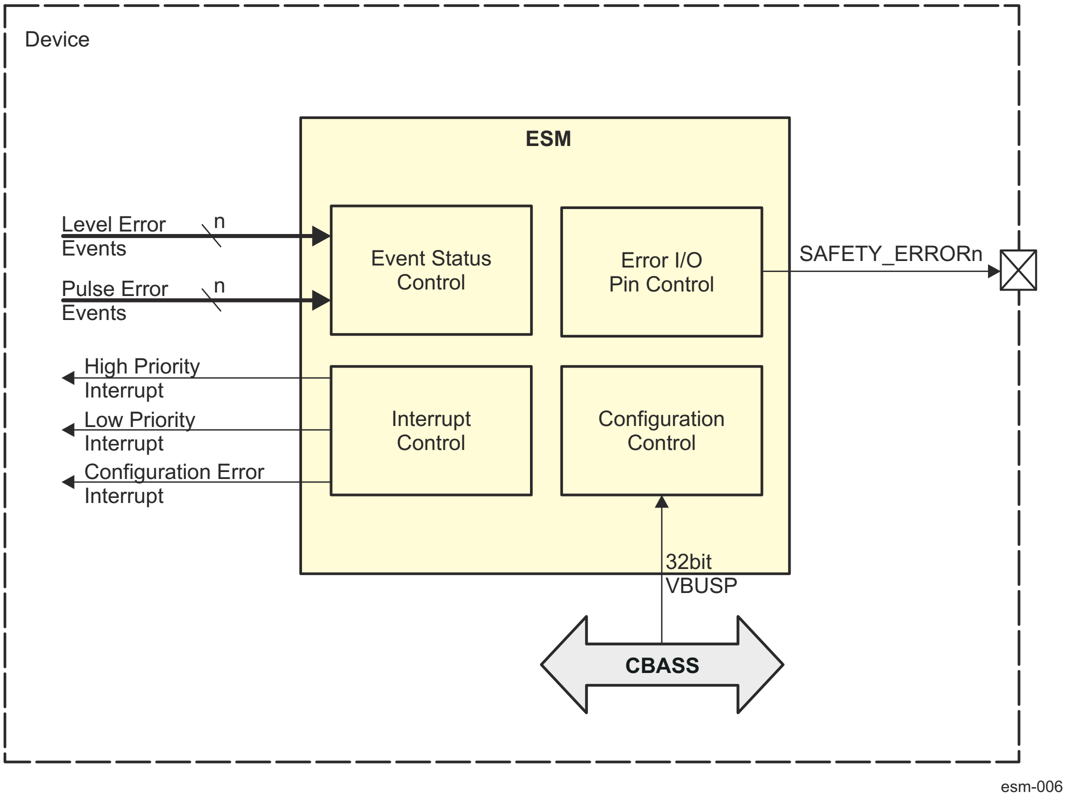

Figure 12-441. ESM Block Diagram

12.6.2.4.1 ESM Interrupt Requests

The ESM module generates three output interrupts to the device interrupt controllers:

- Configuration error interrupt (see Section 12.6.2.4.1.1)
- High priority error interrupt (see Section 12.6.2.4.1.2)
- Low priority error interrupt (see Section 12.6.2.4.1.3)

The error interrupt outputs are provided so that a processor in the device can be signaled to intervene when an error event occurs. Each error event input can be enabled, via software, to cause an error interrupt to occur (via the ESM_INTR_EN_SET_j register). Additionally, each error event input can be programmed to influence either the low priority (default) interrupt or the high priority interrupt (via the ESM_INT_PRIO_j). The low priority interrupt is intended for events that are of interest, but do not require immediate intervention. For example, an indication that there was a single bit error that was corrected may signal a low priority interrupt, so that information can be collected for statistical purposes. A high priority interrupt is intended for events that need immediate attention. For example, an indication that there was an uncorrected two-bit error may be signaled as a high priority interrupt.

12.6.2.4.1.1 ESM Configuration Error Interrupt

The configuration error interrupt (ESM_INT_CFG_LVL_0) indicates that there is an inconsistency in the configuration of one (or more) error group *j* registers (MMRs).

In such inconsistency in the internal copies of any of the MMRs caused by fault associated with error group *j*, the corresponding raw status will be set in the ESM_ERR_RAW register. If the corresponding bit is enabled in the ESM_ERR_EN_SET register, a configuration error interrupt will be triggered.

When a configuration error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_ERR_STS register to determine which group has a configuration error
2. Write the correct values to the following group registers:

Note

If there has been a configuration error, the values in the below registers cannot be guaranteed to be correct anymore. Therefore, software should maintain a copy of the correct values prior to an error to make sure that they can be re-programmed with the correct configuration.

---

  a. ESM_INTR_EN_SET_j
  b. ESM_INTR_EN_CLR_j
  c. ESM_INT_PRIO_j
  d. ESM_PIN_EN_SET_j
  e. ESM_PIN_EN_CLR_j

3. Service any pending interrupts in steps 3, 4, and 5 below

Note

The raw status of any pending interrupts may be inconsistent. Servicing the interrupt will return it to consistency via the error group ESM_RAW_j register. The raw interrupt status registers should also be cleared before enabling ESM or the ESM will generate an interrupt to CPU.

---

4. Write 0x1 to the appropriate bits in the ESM_ERR_STS register. This step will clear the raw status
   a. If the error event is still asserted (or re-asserted), the raw status will be set back to 0x1
   b. If there are no additional errors, the level interrupt will go low
5. Write the end of interrupt vector to the ESM_EOI register
   a. If there are additional configuration error interrupts pending, then a new pulse will be generated and the level interrupt will remain asserted
   b. If there are no additional low priority error interrupts pending, there will be no new pulse.

12.6.2.4.1.2 ESM Low Priority Error Interrupt

Events mapped to the low priority error interrupt (ESM_INT_LOW_LVL_0) are intended to be events of interest that should be addressed eventually, not events that require immediate attention. An example would be an event indicating a corrected error. The system may want to track this for statistical purposes, but it does not require immediate attention.

Any error event can be mapped to the low priority error interrupt. A low priority error interrupt will be generated when an event is enabled to cause an interrupt (via the ESM_INTR_EN_SET_j register) and mapped to the low priority error interrupt (via ESM_INT_PRIO_j register) and the raw status is set (via the ESM_RAW_j register).

When a low priority error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_LOW_PRI register
   a. If both [31-16]PLS and [15-0]LVL bit fields are equal to 0xFFFF, then interrupt is no longer asserted and the interrupt routine has ended.
   b. If either [31-16]PLS or [15-0]LVL bit fields are not equal to 0xFFFF, software has two options for determining what event to service:
      i. First option: Record the value in [31-16]PLS and [15-0]LVL bit fields. Determine which is higher priority. This is based on the global event map number of the highest priority low priority error event

---

Note

The global event map is neither defined by nor maintain in ESM. The global event map must be defined and maintained by software using software determined memory resources. It is conceivable that the global event map will be predefined and loaded during the execution of a secondary boot loader.

        - ii. Second option:
            1. Read the ESM_LOW register to determine which event group(s) have pending low priority error interrupts
            2. Read the desired error group *j* ESM_STS_j register
            3. Identify which low priority interrupt to service

2. Determine, based on the global event map for the device, where the error event came from
3. Service the error event based on the IP's specification:
    - a. The system may take several actions including (but not limited to):
        - i. Fixing the error
        - ii. Resetting the errored IP peripheral
        - iii. Resetting the device
        - iv. Communicating outside the device via the error pin for outside intervention

The rest of the steps assume that the error has been handled and the system wants to clear the error event. Clearing the error event depends on whether the event is a level (see Section 12.6.2.4.1.2.1) or pulse (see Section 12.6.2.4.1.2.2) event.

12.6.2.4.1.2.1 ESM Low Priority Error Level Event

When a low priority error level event has to be cleared, the acting processor must perform the following steps:

1. Clear the low priority error level event at the source
2. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This step will clear the raw status
    - a. If the error event is still asserted (or re-asserted) the raw status will be set back to 0x1
    - b. If there are no error events, the level will de-assert

Note

There is a possible software race condition if software manages to write to the Clear register before the de-asserted level from the source has been synchronized to the ESM clock. If this is an issue, software may perform a read-back at the source IP before writing the clear register to insure order.

3. Write the end of interrupt vector to the ESM_EOI interrupt register
    - a. If there are low priority error level events enabled and pending, then a new pulse will be generated
    - b. If there are no additional low priority error level events enabled and pending, there will be no new pulse
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j* ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.6.2.4.1.2.2 ESM Low Priority Error Pulse Event

When a low priority error pulse event has to be cleared, the acting processor must perform the following steps:

1. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This will clear the raw status and will de-assert the level interrupt.
2. Write the end of interrupt vector to the ESM_EOI interrupt register
    - a. If there are additional low priority error pulse events enabled and pending, then a new pulse will be generated and the level interrupt will remain asserted
    - b. If there are no additional low priority error pulse events enabled and pending, there will be no new pulse
3. Clear the error event at the source. The source may generate a new pulse which will show up as a new error event at the ESM

4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j* ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.6.2.4.1.3 ESM High Priority Error Interrupt

Events mapped to the high priority error interrupt are intended to be events that require immediate intervention from the system because a potentially dangerous error has occurred. An example would be an event indicating an uncorrected error. The system will want to diagnose the issue and intervene to ensure there are no violations.

Any error event can be mapped to the high priority error interrupt. A high priority error interrupt will be generated when an event is enabled to cause an interrupt (via the ESM_INTR_EN_SET_j) register and mapped to the high priority interrupt (via the ESM_INT_PRIO_j) register and the raw status is set (via the ESM_RAW_j).

When a high priority error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_HI_PRI register
   a. If both [31-16] PLS and [15-0] LVL bit fields are equal to 0xFFFF, then interrupt is no longer asserted and the interrupt routine has ended.
   b. If either [31-16] PLS or [15-0] LVL bit fields are not equal to 0xFFFF, software has two options for determining what event to service:
      i. First option: Record the value in [31-16] PLS and [15-0] LVL bit fields. Determine which is higher priority. This is based on the global event map number of the highest priority high priority error event.

Note

The global event map is neither defined by nor maintain in ESM. The global event map must be defined and maintained by software using software determined memory resources. It is conceivable that the global event map will be predefined and loaded during the execution of a secondary boot loader.

      ii. Second option:
         1. Read the ESM_HI register to determine which event group(s) have pending high priority error interrupts
         2. Read the desired error group *j* ESM_STS_j register
         3. Identify which high priority error interrupt to service

2. Determine, based on the global event map for the device, where the error event came from
3. Service the error event based on the IP's specification:
   a. The system may take several actions including (but not limited to):
      i. Fixing the error
      ii. Resetting the errored IP peripheral
      iii. Resetting the device
      iv. Communicating outside the device via the error pin for outside intervention

The rest of the steps assume that the error has been handled and the system wants to clear the error event. Clearing the error event depends on whether the event is a level (see Section 12.6.2.4.1.3.1) or pulse (see Section 12.6.2.4.1.3.2) event.

12.6.2.4.1.3.1 ESM High Priority Error Level Event

When a high priority error level event has to be cleared, the acting processor must perform the following steps:

1. Clear the error event at the source
2. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This step will clear the raw status

   a. If the error event is still asserted (or re-asserted) the raw status will be set back to 0x1
   b. If there are no error events, the level will de-assert

Note

There is a possible software race condition if software manages to write to the Clear register before the de-asserted level from the source has been synchronized to the ESM clock. If this is an issue, software may perform a read-back at the source IP before writing the clear register to insure order.

---

3. Write the end of interrupt vector to the ESM_EOI interrupt register
   a. If there are high priority error level events enabled and pending, then a new pulse will be generated
   b. If there are no additional high priority error level events enabled and pending, there will be no new pulse
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j* ESM_PIN_EN_SET_j register, but may be done regardless as an extra CLEAR is not harmful.

12.6.2.4.1.3.2 ESM High Priority Error Pulse Event

When a high priority error pulse event has to be cleared, the acting processor must perform the following steps:

1. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This will clear the raw status and will de-assert the level interrupt.
2. Write the end of interrupt vector to the ESM_EOI interrupt register
   a. If there are high priority error pulse events enabled and pending, then a new pulse will be generated and the level interrupt will remain asserted
   b. If there are no additional high priority error pulse events enabled and pending, there will be no new pulse
3. Clear the error event at the source. The source may generate a new pulse which will show up as a new error event at the ESM
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j* ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.6.2.4.2 ESM Error Event Inputs

The ESM can have up to 1024 error event inputs, configurable by groups of 32. For the mapping of system interrupt error events to ESM interrupt inputs, see *Interrupt Sources*.

Level error events (active high) are synchronized to the ESM clock. This synchronized value is captured in to a flop.

Pulse error events use rising edge detection. Each pulse error event has 3 redundant inputs. Each input has its own edge detection logic. Multiple transmission protects against Single Event Upsets (SEUs, transient errors) causing a pulse to be lost during transmission and against failure of the edge detection logic. Once an edge has been detected on any of the three inputs, the ESM_RAW_j status is set. Subsequent pulses are likely to come concurrently or quickly enough that software will not have reacted yet. This logic is intentionally biased against false negatives and towards false positives. An SEU that causes an event where none actually occurred will cause software to be called in to action. Software must observe that there is no real error and clear the false status.

12.6.2.4.3 ESM Error Pin Output

The error pin output (ERR_O) is used to signal an external agent that it needs to (or may need to) intervene because of an error. Each error event input can be programmed, via software, to influence the error pin output (via the ESM_PIN_EN_SET_j register). The error pin output is active low or PWM based on the ESM_EN[7-4] PWM_EN field. This bit field should only be modified when the ESM is disabled, based on the ESM_EN register.

During Power-On Reset (POR), the error pin is active (asserted low) and the device drives this via a weak internal pull-down. The I/O is under the control of the device. When POR is removed from the ESM, it will be driving the error pin so the device can hand over control to the ESM. The user may also add an external pull-down that is only active when the device is in reset.

During a warm reset the state of the error pin is unchanged, that is the error pin logic is only reset by a POR. The device leaves the I/O active during a warm reset.

The ESM has also a software error forcing capability on the error pin. That is, a force error can be set via the ESM_EN[3-0] KEY bit field.

CAUTION

The isolation value for the ERR_O output of ESM is active (0). This is intended and supposed to protect against an accidental transition to a low power state. If the actual low power mode transition is intended, the PMIC should be made aware by software to ignore the ESM error signal. Otherwise device resets will be asserted from companion chip.

Figure 12-442 describes the behavior of the error pin. Not shown is that a reset (Power-On-Reset only) will immediately transition the error pin to the ESM_RESET state and a Global Soft Reset will immediately transition the error pin to the ESM_IDLE state. A pending error interrupt event is any error event with the raw state set and the error pin Influence enabled. There are two types of "clear" events associated with servicing the error pin. The first is to clear the status of the pending event (see Section 12.6.2.4.1 for how to clear level and pulse pending events). The second is the CLEAR event meant to de-assert the error pin.

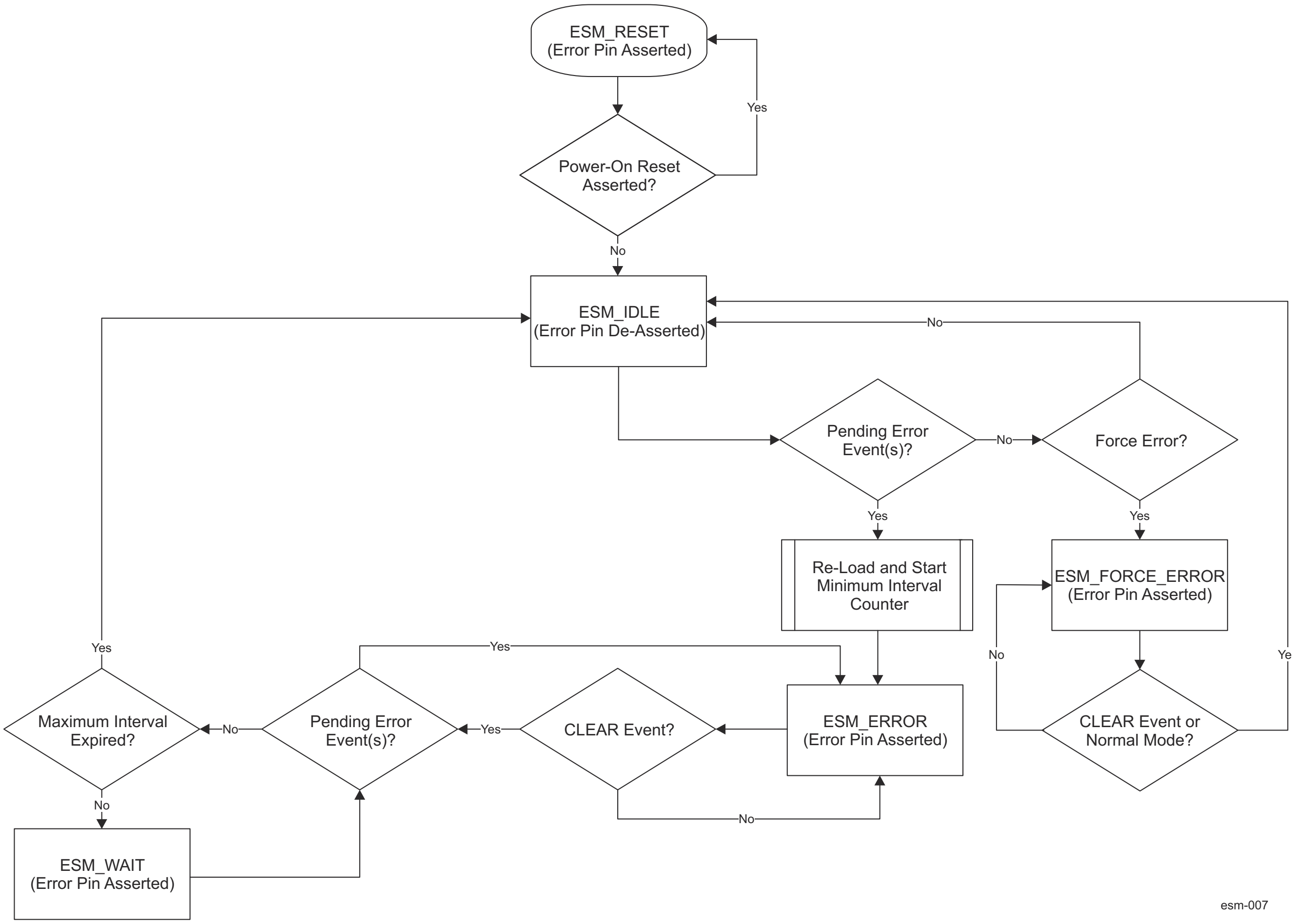

Figure 12-442. ESM Error Pin State Flowchart

If an error event happens that has been programmed to influence the error pin, the error pin will assert (active low) for a minimum time (as programmed by the ESM_PIN_CNTR_PRE register). In order for the error pin to de-assert, the following 3 things must happen:

1. The minimum time interval must expire
2. The event that caused the error pin to assert must be cleared (see Section 12.6.2.4.1)
3. A CLEAR (0x5) must be written to the ESM_PIN_CTRL register.

Note

Step 3 should happen after step 2, but either (or both) of these steps may happen before or after step 1.

Figure 12-443 shows a typical error pin assertion.

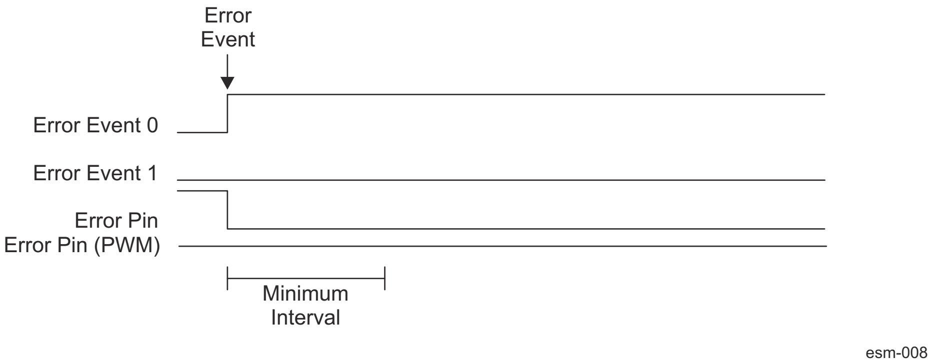

Figure 12-443. ESM Error Pin Assertion

If, during the minimum time, CLEAR is written to the error key, then the error pin will de-assert after the minimum time interval, as shown in Figure 12-444.

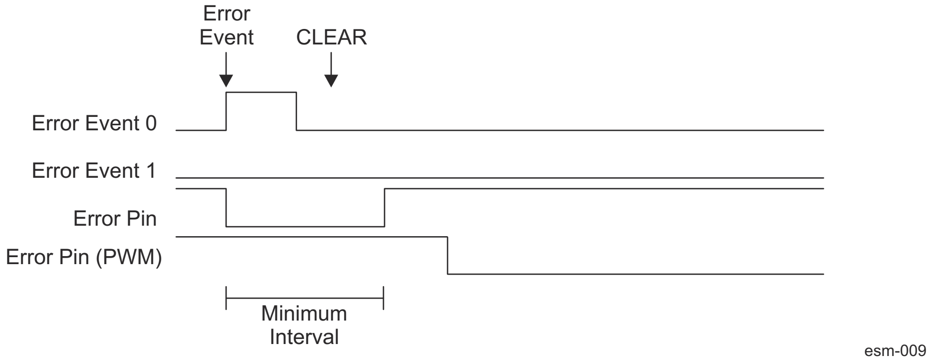

Figure 12-444. ESM Error Pin Assertion with CLEAR during Minimum Interval

If CLEAR is not written till after the minimum time interval, the error pin will de-assert when CLEAR is written. This is regardless of whether the error interrupt event itself is removed before or after the minimum time interval, as shown by the dotted line in Figure 12-445.

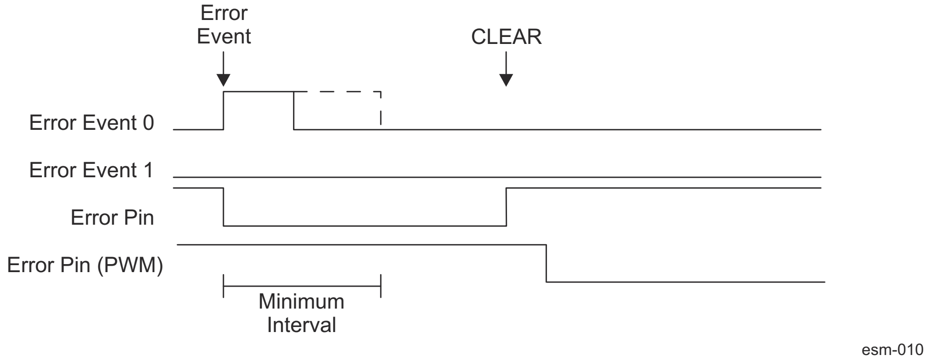

Figure 12-445. ESM Error Pin Asserting with CLEAR after Minimum Interval

When in the ESM_ERROR state and a CLEAR event happen, if there are still pending error events, the ESM stays in the ESM_ERROR state with the error pin asserted. Multiple error events when in the ESM_ERROR state do not reset the minimum time interval counter as shown in Figure 12-446.

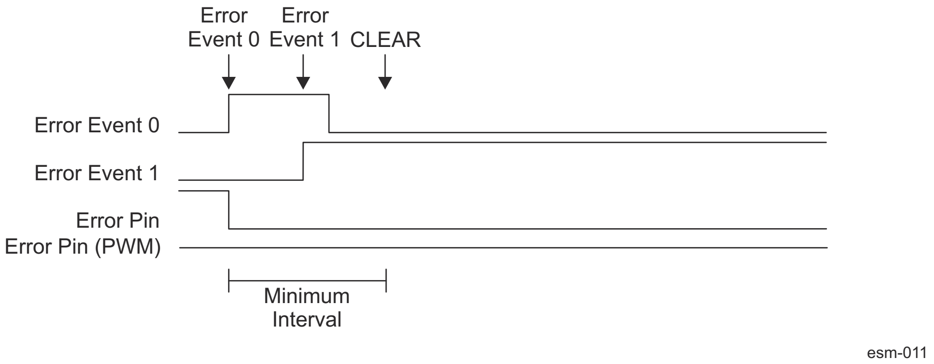

Figure 12-446. ESM Error Pin Asserting with Interval Reset by Additional Error Event(s)

A CLEAR event causes a re-evaluation of whether there are any pending error events. As such, a single CLEAR can be used to clear the error pin after multiple error events. Multiple CLEAR events can occur (such as the one with the dotted arrow shown in Figure 12-447), but are not necessary. No matter how many error events occur nor when (or how many) CLEAR events occur, the error pin will always be asserted for at least the minimum time interval

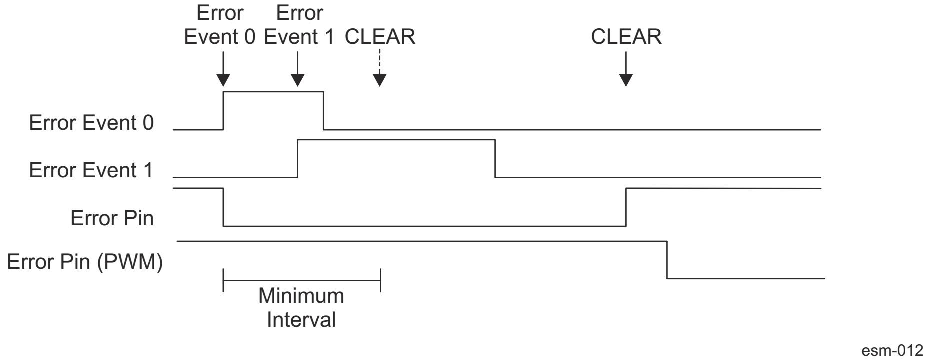

Figure 12-447. ESM Error Pin Asserting with Single CLEAR for Multiple Events

If all error events are cleared and the ESM is in the ESM_WAIT state, waiting for the minimum time interval to expire, and a new error interrupt event occurs, the ESM will go back to the ESM_ERROR state. The minimum time interval will not reset, but a new CLEAR event will be required as shown in Figure 12-448.

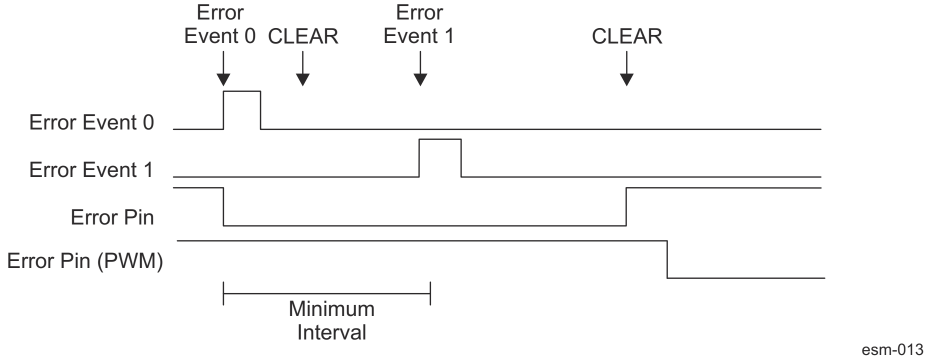

Figure 12-448. ESM Error Pin Asserting with New Error During Minimum Time Interval

Table 12-493 shows some common scenarios of how the error pin as well as the two associated registers (ESM_PIN_CTRL and ESM_PIN_STS) will be set.

Table 12-505. ESM Error Pin Scenarios

Scenario	Error Pin State Value	ESM_PIN_CTRL[3-0] KEY	ESM_PIN_STS[0] VAL status value	Additional Notes
POR Asserted	0	N/A	N/A	Registers are inaccessible. Device disables the I/O and pulls down internally.
After de-assertion of POR	1	0x0 (Normal Mode)	0x0	-
After de-assertion of Warm Reset (error was not asserted when reset asserted)	1	0x0 (Normal Mode)	0x0	-
After de-assertion of Warm Reset (error was asserted when reset asserted)	0	0x0 (Normal Mode)	0x1	-
Force error pin	0	0xA (Force Error Mode)	0x0	Forcing error on the pin via software.

12.6.2.4.4 PWM Mode

If the error output pin is in PWM mode then when no error is detected it will toggle according to programmable MMR widths for high and low periods. When an error occurs, the error pin stops toggling and remains constant until the error is cleared. An external PMIC that is detecting the PWM toggles can identify the error if the pin stops toggling. The periods should be programmed such that they fit within the expectation of the external PMIC.

12.6.2.4.5 ESM Minimum Time Interval

The minimum time interval is the minimum amount of time that the error pin will be asserted (active low) when an enabled error interrupt event happens. This value is system dependent, but should be enough time so that the external monitoring agent can always see the error pin asserted, but short enough so that if all of the error events are cleared, then the error pin can be de-asserted before the external agent decides to intervene. This is highly dependent on the application and the Fault Tolerant Time Interval.

The Minimum Time Interval counter is clock cycle based, therefore the time of the interval is a combination of the value in the ESM_PIN_CNTR_PRE register and the clock frequency of the ESM. Software must calculate the value accordingly. The Minimum Time Interval should be set according to the needs of the application.

12.6.2.4.6 ESM Protection for Registers

The configuration for each error group *j* of registers are backed up by 3 flops in order to protect against single or double-bit errors. When written, all 3 bits are set to the same value. When read (and for functioning of the internal state machines) the value is the OR of all 3 bits. Whenever any of the bits disagree, the Configuration Error interrupt is asserted (if enabled). The registers covered by this mechanism are:

- ESM_ERR_RAW
- ESM_ERR_STS
- ESM_ERR_EN_SET
- ESM_ERR_EN_CLR
- ESM_RAW_j
- ESM_STS_j
- ESM_INTR_EN_SET_j
- ESM_INTR_EN_CLR_j
- ESM_INT_PRIO_j
- ESM_PIN_EN_SET_j
- ESM_PIN_EN_CLR_j

The error pin control register ESM_PIN_CTRL contains a multi-bit field KEY. The key value ensures normal operation on the error pin and that an error even will be generated if one occurs. Software should periodically read check the KEY bit field value and make sure it is 0x0. If the value is not 0x0, software must re-write it to this key value (unless in test mode forcing an error on the pin) to ensure the normal operation. Table 12-494 lists the KEY values and their respective meaning.

Table 12-506. ESM Error Pin Control Values

ESM_PIN_CTRL[3-0] KEY	Description
N/A	Registers are inaccessible. Device disables the I/O and pulls down internally.
0x0 (Normal)	Normal operation mode - Error pin will activate when an enabled error event occurs.
0xA (Force Error)	Force error mode - Forces the error pin active. To clear the error pin (return to the ESM_IDLE state) write this field back to normal mode (writing a CLEAR event will also work). Force error mode must be set only while in IDLE. Attempting force error while in another state will have no effect.
0x5 (CLEAR)	CLEAR Event - generates a CLEAR event to the ESM state machine. KEY will return to normal mode (0x0) on the next cycle.
Other Values	All other values - Normal mode. Writing any of these values will have no effect. When reading any of these values indicates that one or more bits have experienced a single event upset, software should write the field back to 0x0. The ESM will continue to operate in normal mode.

The error pin counter pre-load register ESM_PIN_CNTR_PRE should also be read and checked periodically by software.

12.6.2.4.7 ESM Clock Stop

The ESM can only be put in to clock stop if all of the internal state machines are idle and the [3-0] KEY bit field for the global enable command is cleared in the ESM_EN register.

12.6.3 Memory Cyclic Redundancy Check (MCRC) Controller

This chapter describes the Memory Cyclic Redundancy Check (MCRC) controller in the device.

12.6.3.1 MCRC Overview

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system.

Table 12-507. MCRC Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
MCU_MCRC0	✓	-

12.6.3.1.1 MCRC Features

MCRC has the following features:

- Four channels to perform background signature verification on any memory subsystem
- Data compression on 8-, 16-, 32-, and 64-bit data size
- Maximum-length PSA (Parallel Signature Analysis) register constructed based on 64-bit primitive polynomial
- Each channel has a CRC Value Register which contains the pre-determined CRC value
- Use timed base event trigger from timer to initiate DMA data transfer
- Programmable 20-bit pattern counter per channel to count the number of data patterns for compression
- Three modes of operation:
  - Auto
  - Semi-CPU
  - Full-CPU
- For each channel, CRC can be performed either by MCRC Controller or by CPU
- Automatically performs signature verification without CPU intervention in AUTO mode
- Generates interrupt to CPU in Semi-CPU mode to allow CPU to perform signature verification itself
- Generates CRC fail interrupt in AUTO mode if signature verification fails
- Generates Timeout interrupt if CRC is not performed within the time limit
- Generates DMA request per channel to initiate CRC value transfer
- An 128-byte block burst address for the PSA register to DMA without constant mode bus attribute

12.6.3.1.2 MCRC Not Supported Features

The following features are not supported by the module:

- Data trace capability on VBUSM, ITCM and DTCM data buses.
- DMA support
- Auto Mode.

12.6.3.2 MCRC Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 12-449 shows the MCRC integration.

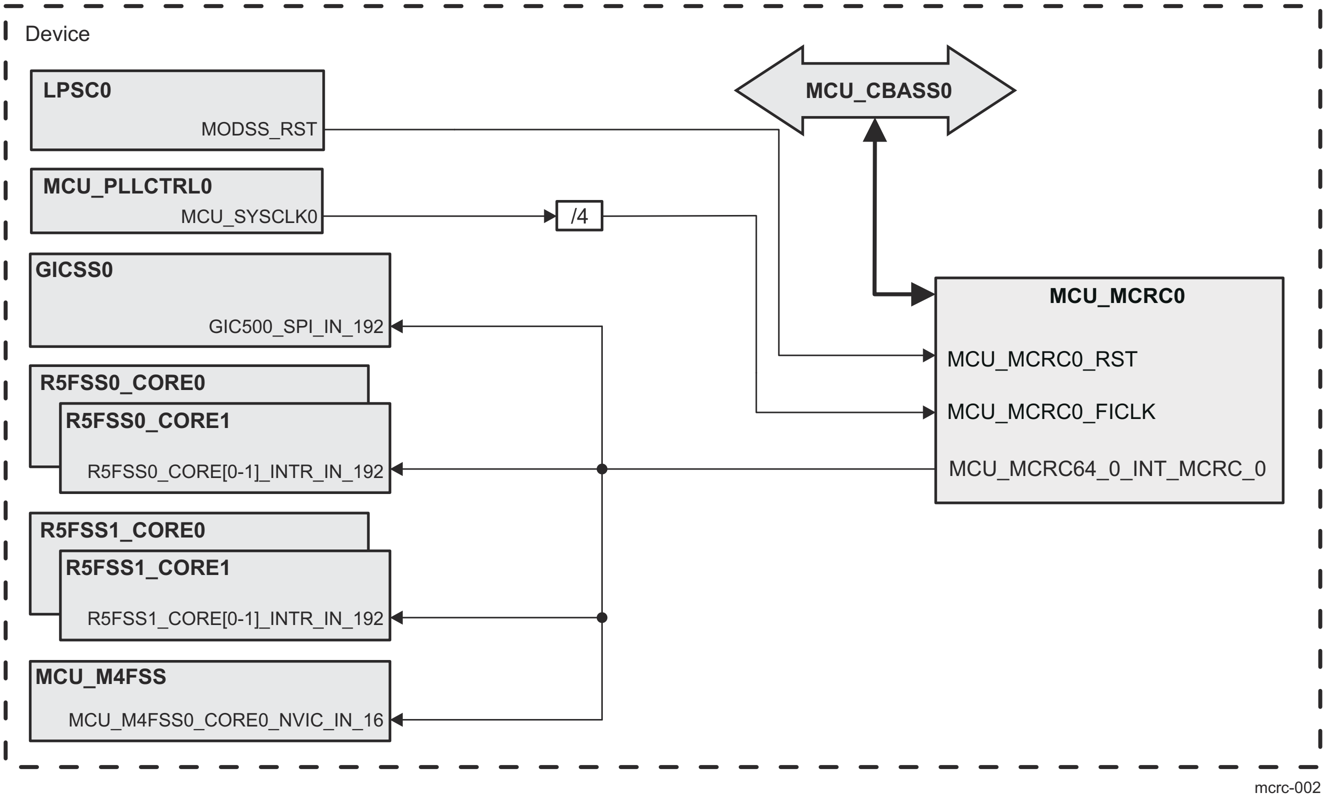

Figure 12-449. MCU_MCRC Integration

Table 12-496 and Table 12-497 summarize the integration of the module in the device.

Table 12-508. MCU_MCRC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
MCU_MCRC0	PSC0	GP	LPSC0	MCU_CBASS0

Table 12-509. MCU_MCRC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
MCU_MCRC0	MCRC0_FICLK	MCU_SYSCLK0/4	MCU_PLLCTRL0	MCU_MCRC0 clock. This clock is used for all interface and functional operations.

Table 12-510. MCU_MCRC Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
MCU_MCRC0	MCRC0_RST	MODSS_RST	LPSC0	MCU_MCRC0 hardware reset

Table 12-511. MCU_MCRC Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_MCRC0	MCU_MCRC64_0_INT_MCRC_0	GICSS0_SPI_IN_192	GICSS0	MCU_MCRC0 interrupt signal	Level

Table 12-511. MCU_MCRC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
		MCU_M4FSS0_CORE0_NVIC_IN_16	MCU_M4FSS		
		R5FSS0_CORE0_INTR_IN_192	R5FSS0_CORE0		
		R5FSS0_CORE1_INTR_IN_192	R5FSS0_CORE1		
		R5FSS1_CORE0_INTR_IN_192	R5FSS1_CORE0		
		R5FSS1_CORE1_INTR_IN_192	R5FSS1_CORE1		

Table 12-512. MCU_MCRC DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Description	Type
MCU_MCRC0	-	-	-	No PDMA channels to external DMA engines.	-

Note

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset, and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

12.6.3.3 MCRC Functional Description

12.6.3.3.1 MCRC Block Diagram

Figure 12-450 shows the MCRC internal blocks.

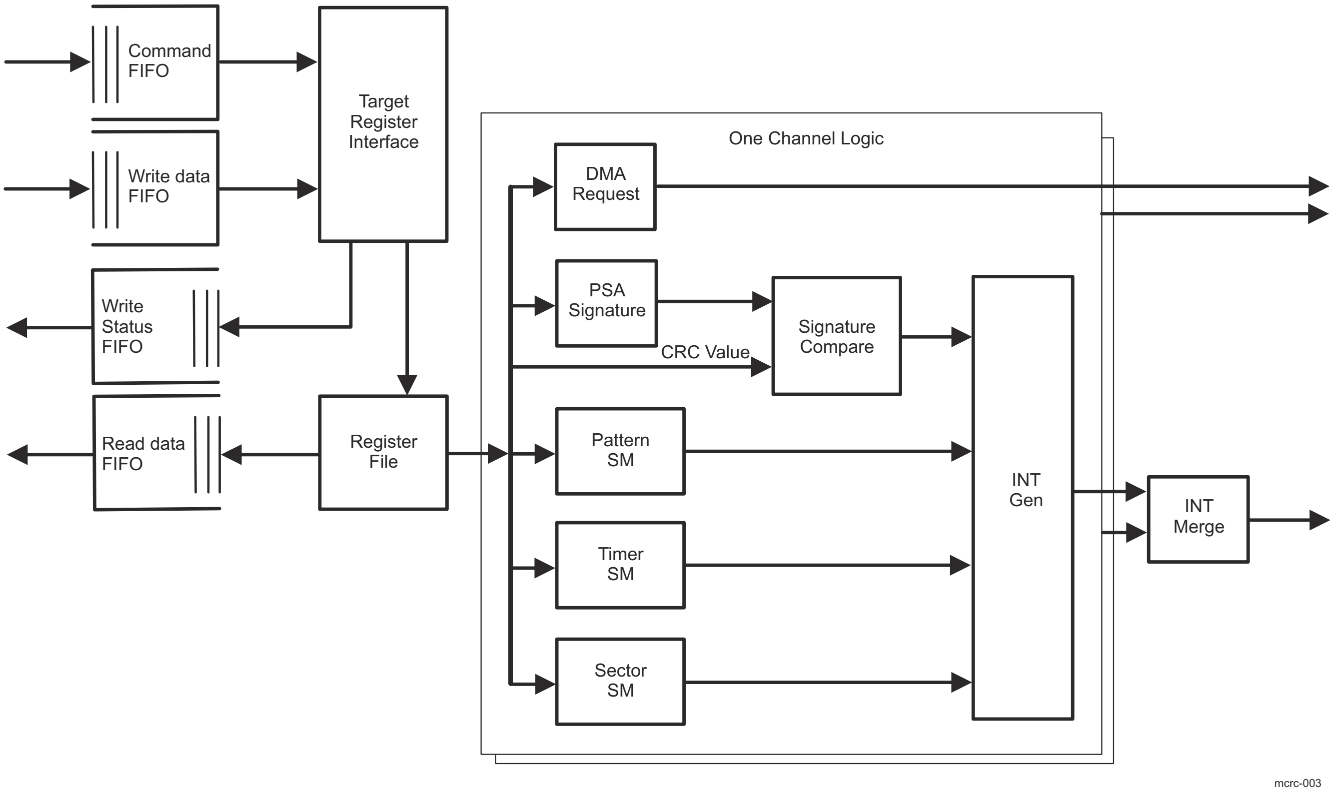

Figure 12-450. MCRC Block Diagram

- **Command FIFO**: The Command FIFO pipelines the commands to the target register interface. The Command and Write FIFOs allow the data to be coincident for processing. If there is no space for writes in the Write Status FIFO or no space in the Read Data FIFO for reads, the command processing will be halted until there is space in the appropriate FIFO. This FIFO is 4 elements deep.
- **Write FIFO**: The Write FIFO pipelines the write data to the target register interface. The Command and Write FIFOs allow the data to be coincident for processing. If there is no space for writes in the Write Status FIFO or no space in the Read Data FIFO for reads, the command processing will be halted until there is space in the appropriate FIFO. This FIFO is 2 elements deep.
- **Write Status FIFO**: The Write Status FIFO pipelines the write status back to the VBUSM. A write status will be issued on the final data phase of a write command. This FIFO is 2 elements deep.
- **Read Data FIFO**: The Read Data FIFO pipelines the read data back to the VBUSM. This FIFO is 3 elements deep.
- **Target Register Interface**: The Target Register Interface directs the written data to the register file.
- **PSA Signature**: The PSA Signature creates the signature of the data written. This data will then be compared to the CRC Value or read by software to determine goodness.
- **Pattern State Machine**: The Pattern State Machine determines when a block of data has been serviced.
- **Timer State Machine**: The Timer State Machine determines when overrun and under-run events are detected.
- **Sector State Machine**: The Sector State Machine determines when a sector error should be captured so the software can determine the errant block of data.
- **Signature Compare**: The Signature Compare block compares the current signature to the CRC Value register and sends the result to the Interrupt Generation block.

12.6.3.3.2 MCRC General Operation

There are four channels in MCRC controller and for each channel there is a PSA (Parallel Signature Analysis) Signature Register (MCRC_PSA_SIGREGL1-4) and a CRC (Cyclic Redundancy Check) Value Register (MCRC_CRC_REGL1-4).

A memory can be organized into multiple sectors with each sector consisting of multiple data patterns. A data pattern can be a 8-, 16-, 32-, or 64-bit data. MCRC module performs the signature calculation and compares the signature to a pre-determined value. The PSA Signature Register compresses an incoming data pattern into a signature when it is written. When one sector of data patterns are written into PSA Signature Register, a final signature corresponding to the sector is obtained. CRC Value Register stores the pre-determined signature corresponding to one sector of data patterns. The calculated signature and the pre-determined signature are then compared to each other for signature verification. To minimize CPU's involvement, data patterns transfer can be carried out at the background of CPU using DMA controller. DMA is setup to transfer data from memory of which the contents to be verified to the memory mapped PSA Signature Register. When DMA transfers data to the memory mapped PSA Signature Register, a signature is generated.

A programmable 20-bit data pattern counter is used for each channel to define the number of data patterns to calculate for each sector. Signature verification can be performed automatically by MCRC controller in AUTO mode or by CPU itself in Semi-CPU or Full-CPU mode. In AUTO mode, a self-sustained CRC signature calculation can be achieved without any CPU intervention.

12.6.3.3.3 MCRC Modes of Operation

MCRC Controller can operate in AUTO, Semi-CPU, and Full-CPU modes.

12.6.3.3.3.1 AUTO Mode

In AUTO mode, MCRC Controller in conjunction with DMA controller can perform CRC without CPU intervention. A sustained transfer of data to both the PSA Signature Register (MCRC_PSA_SIGREGL1-4) and a CRC (Cyclic Redundancy Check) Value Register (MCRC_CRC_REGL1-4) are performed in the background of CPU. When a mismatch is detected, an interrupt is generated to the CPU. A 16-bit, current sector ID register (MCRC_CRC_CURSEC_REG1-4) is provided to identify which sector causes a CRC failure.

12.6.3.3.3.2 Semi-CPU Mode

In Semi-CPU mode, DMA controller is also utilized to perform data patterns transfer to PSA Signature Register (MCRC_PSA_SIGREGL1-4). Instead of performing signature verification automatically, the CRC controller generates an compression complete interrupt to CPU after each sector is compressed. Upon responding to the interrupt the CPU performs the signature verification by reading the calculated signature stored at the PSA Sector Signature Register (MCRC_PSA_SECSIGREGL1-4) and compare it to a pre-determined CRC value.

12.6.3.3.3.3 Full-CPU Mode

In Full-CPU mode, the CPU does the data patterns transfer and signature verification all by itself. When CPU has enough throughput, it can perform data patterns transfer by reading data from the memory system to the PSA Signature Register (MCRC_PSA_SIGREGL1). After certain number of data patterns are compressed, the CPU can read from the PSA Signature Register and compare the calculated signature to the pre-determined CRC signature value. In Full-CPU mode, neither interrupt nor DMA request is generated. All counters are also disabled.

12.6.3.3.4 PSA Signature Register

The 64-bit PSA Signature Register (MCRC_PSA_SIGREGL1-4 and MCRC_PSA_SIGREGH1-4) is based on one of the selected CRC polynomials to produce the maximum length LFSR (Linear Feedback Shift Register).

$$\text{CRC64: } f(x) = x^{64} + x^4 + x^3 + x + 1 \tag{11}$$

Note

More details of the 64-bit primitive polynomial can be found at W. Stahnke, Primitive binary polynomials, Math. Comp. 27 (1973), 977--980.

There is one PSA Signature Register per CRC channel. PSA Signature Register can be both read and written. When it is written, it can either compress the data or just capture the data depending on the state of CHi_MODE bits (where i = 1 to 4). If CHi_MODE=0x0 (Data Capture), a seed value can be planted in the PSA Signature Register without compression. Other modes other than Data Capture will result with the data compressed by PSA Signature Register when it is written. Each channel can be planted with different seed value before compression starts. When PSA Signature Register is read, it gives the calculated signature.

MCRC Controller should be used in conjunction with the on-chip DMA controller to produce optimal system performance. The incoming data pattern to PSA Signature Register is typically initiated by the DMA controller. When DMA is properly setup, it would read data from the pre-determined memory system and write them to the memory mapped PSA Signature Register. Each time PSA Signature Register is written a signature is generated. CPU itself can also perform data transfer by reading from the memory system and perform write operation to PSA Signature Register if CPU has enough throughput to handle data patterns transfer.

After a system reset and when AUTO mode is enabled, MCRC Controller automatically generates a DMA request to request the pre-determined CRC value corresponding to the first sector of memory to be checked.

In AUTO mode, when one sector of data patterns is compressed, the signature stored at the PSA Signature Register is first copied to the PSA Sector Signature Register (MCRC_PSA_SECSIGREGL1-4) and PSA Signature Register is then cleared out to all zeros. An automatic signature verification is then performed by comparing the signature stored at the PSA Sector Signature Register to the CRC Value Register (MCRC_CRC_REGL1-4). After the comparison the MCRC Controller can generate a DMA request. Upon receiving the DMA request the DMA controller will update the CRC Value Register by transferring the next pre-determined signature value associated with the next sector of memory system. If the signature verification fails then MCRC Controller can generate a CRC fail interrupt.

In Full-CPU mode, no DMA request and interrupt are generated at all. The number of data patterns to be compressed is determined by CPU itself. Full-CPU mode is useful when DMA controller is not available to perform background data patterns transfer. Software can periodically generate a software interrupt to CPU and use CPU to accomplish data transfer and signature verification.

MCRC Controller supports double word, word, half word and byte access to the PSA Signature Register. During a non-doubleword write access, all unwritten byte lanes are padded with zeros before compression. Note that comparison between PSA Sector Signature Register and CRC Value Register is always in 64 bits because a compressed value is always expressed in 64 bits.

There is a software reset per channel for PSA Signature Register. When set, the PSA Signature Register is reset to all zeros.

PSA Signature Register is reset to zero under the following conditions:

- System reset
- PSA Software reset
- One sector of data patterns is compressed

12.6.3.3.5 PSA Sector Signature Register

After one sector of data is compressed, the final resulting signature calculated by PSA Signature Register is transferred to the 64-bit PSA Sector Signature Register (MCRC_PSA_SECSIGREGL1-4 and MCRC_PSA_SECSIGREGH1-4). PSA Signature Register is a read-only register. During Semi-CPU mode, the host CPU must read from the PSA Sector Signature Register instead of reading from PSA Signature Register for signature verification to avoid data coherency issue. The PSA Signature Register can be updated with new signature before the host CPU is able to retrieve it.

In Semi-CPU mode, no DMA request is generated. When one sector of data patterns is compressed, CRC controller first generates a compression complete interrupt. Responding to the interrupt, CPU will read the PSA Sector Signature Register and compare it to the known good signature or write the signature value to another memory location to build a signature file. In Semi-CPU mode, CPU must perform the signature verification in a manner to prevent any overrun condition. The overrun condition occurs when the compression complete interrupt is generated after one sector of data patterns is compressed and CPU has not read from the PSA Sector Signature Register to perform necessary signature verification before PSA Sector Signature Register is overridden with a new value. An overrun interrupt can be enabled to generate when overrun condition occurs.

12.6.3.3.6 CRC Value Register

Associated with each channel there is a 64-bit CRC Value Register (MCRC_CRC_REGL1-4 and MCRC_CRC_REGH1-4).

The CRC Value Register stores the pre-determined CRC value. After one sector of data patterns is compressed by PSA Signature Register, MCRC Controller can automatically compare the resulting signature stored at the PSA Sector Signature Register with the pre-determined value stored at the CRC Value Register if AUTO mode is enabled. If the signature verification fails, MCRC Controller can be enabled to generate an CRC fail interrupt. When the channel is set up for Semi-CPU mode, CRC controller first generates a compression complete interrupt to CPU. Upon servicing the interrupt, CPU will then read the PSA Sector Signature Register and then read the corresponding CRC value stored at another location and compare them. CPU must not read from the CRC Value Register during Semi-CPU or Full-CPU mode because the CRC Value Register is not updated during these two modes.

In AUTO mode, for first sector’s signature, DMA request is generated when mode is programmed to AUTO. For subsequent sectors, DMA request is generated after each sector is compressed. Responding to the DMA request, DMA controller reloads the CRC Value Register for the next sector of memory system to be checked. The user software needs to configure the DMA to ensure that the DMA first writes to the MCRC_CRC_REGL1 followed by the MCRC_CRC_REGH1 register in during the AUTO Mode.

When CRC Value Register is updated with a new CRC value, an internal flag is set to indicate that CRC Value Register contains the most current value. This flag is cleared when CRC comparison is performed. Each time at the end of the final data pattern compression of a sector, MCRC Controller first checks to see if the corresponding CRC Value Register has the most current CRC value stored in it by polling the flag. If the flag is set then the CRC comparison can be performed. If the flag is not set then it means the CRC Value Register contains stale information. A CRC underrun interrupt is generated. When an underrun condition is detected, signature verification is not performed.

MCRC Controller supports double word, word, half word and byte access to the CRC Value Register. As noted before comparison between PSA Sector Signature Register and CRC Value Register during AUTO mode is carried out in 64 bits.

12.6.3.3.7 Raw Data Register

The raw or un-compressed data written to the PSA Signature Register is also saved in the 64-bit Raw Data Register (MCRC_RAW_DATAREGL1-4 and MCRC_RAW_DATAREGH1-4). This register is read only.

12.6.3.3.8 Example DMA Controller Setup

DMA controller needs to be setup properly in either AUTO or Semi-CPU mode as DMA controller is used to transfer data patterns. Hardware or a combination of hardware and software DMA triggering are supported.

12.6.3.3.8.1 AUTO Mode Using Hardware Timer Trigger

There are two DMA channels associated with each CRC channel when in AUTO mode. One DMA channel is setup to transfer data patterns from the source memory to the PSA Signature Register (MCRC_PSA_SIGREGL1-4). The second DMA channel is setup to transfer the pre-determined signature to the CRC Value Register (MCRC_CRC_REGL1-4). The trigger source for the first DMA channel can be either by hardware or by software. As illustrated in Figure 12-451, a timer can be used to trigger a DMA request to initiate transfer from the source memory system to PSA Signature Register. In AUTO mode, MCRC Controller also generates DMA request after one sector of data patterns is compressed to initiate transfer of the next CRC value corresponding to the next sector of memory. Thus a new CRC value is always updated in the CRC Value Register (MCRC_CRC_REGL1-4)by DMA synchronized to each sector of memory.

A block of memory system is usually divided into many sectors. All sectors are the same size. The sector size is programmed in the MCRC_CRC_PCOUNT_REG1-4 and the number of sectors in one block is programmed in the MCRC_CRC_SCOUNT_REG1-4 of the respective channel. MCRC_CRC_PCOUNT_REG1-4 multiplies MCRC_CRC_SCOUNT_REG1-4 and multiplies transfer size of each data pattern should give the total block size in number of bytes.

The total size of the memory system to be examined is also programmed in the respective transfer count register inside DMA module. The DMA transfer count register is divided into two parts. They are element count and frame count. Note that a hardware DMA request can be programmed to trigger either one frame or one entire block transfer. In Figure 12-451, a hardware DMA request from a timer is used as a trigger source to initiate DMA transfer. If all four CRC channels are active in AUTO mode then a total of four DMA requests would be generated by MCRC Controller.

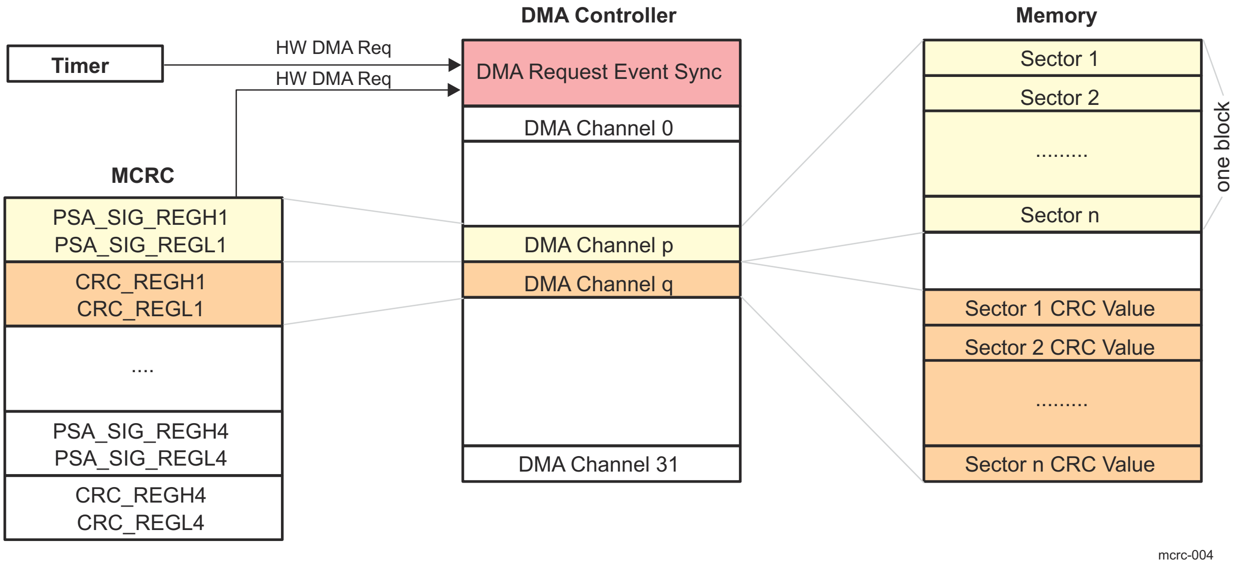

Figure 12-451. AUTO Mode Using Hardware Timer Trigger

12.6.3.3.8.2 AUTO Mode Using Software Trigger

The data patterns transfer can also be initiated by software. CPU can generate a software DMA request to activate the DMA channel to transfer data patterns from source memory system to the PSA Signature Register. To generate a software DMA request CPU needs to set the corresponding DMA channel in the DMA software trigger register. Note that just one software DMA request from CPU is enough to complete the entire data patterns transfer for all sectors. Please see AUTO Mode With Software CPU Trigger for illustration.

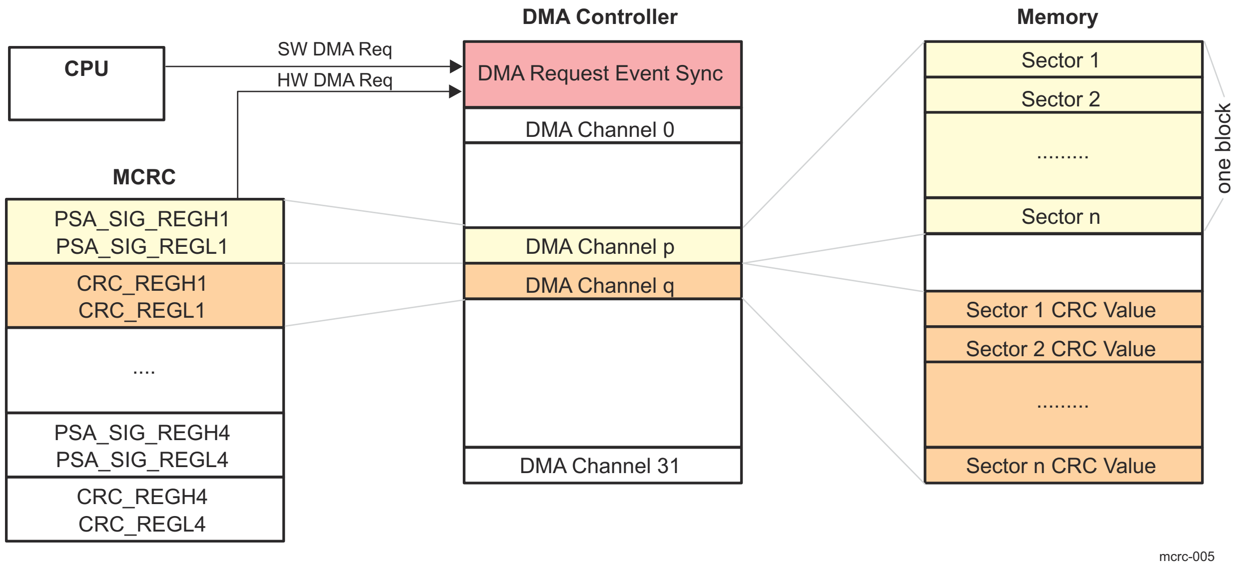

Figure 12-452. AUTO Mode With Software CPU Trigger

12.6.3.3.8.3 Semi-CPU Mode Using Hardware Timer Trigger

During Semi-CPU mode, no DMA request is generated by CRC controller. Therefore, no DMA channel is allocated to update CRC Value Register. CPU should not read from CRC Value Register in semi-CPU mode as it contains stale value. Note that no signature verification is performed at all during this mode. Similar to AUTO mode, either by hardware or by software DMA request can be used as a trigger for data patterns transfer. Figure 12-453 illustrates the DMA setup using semi-CPU mode with hardware timer trigger.

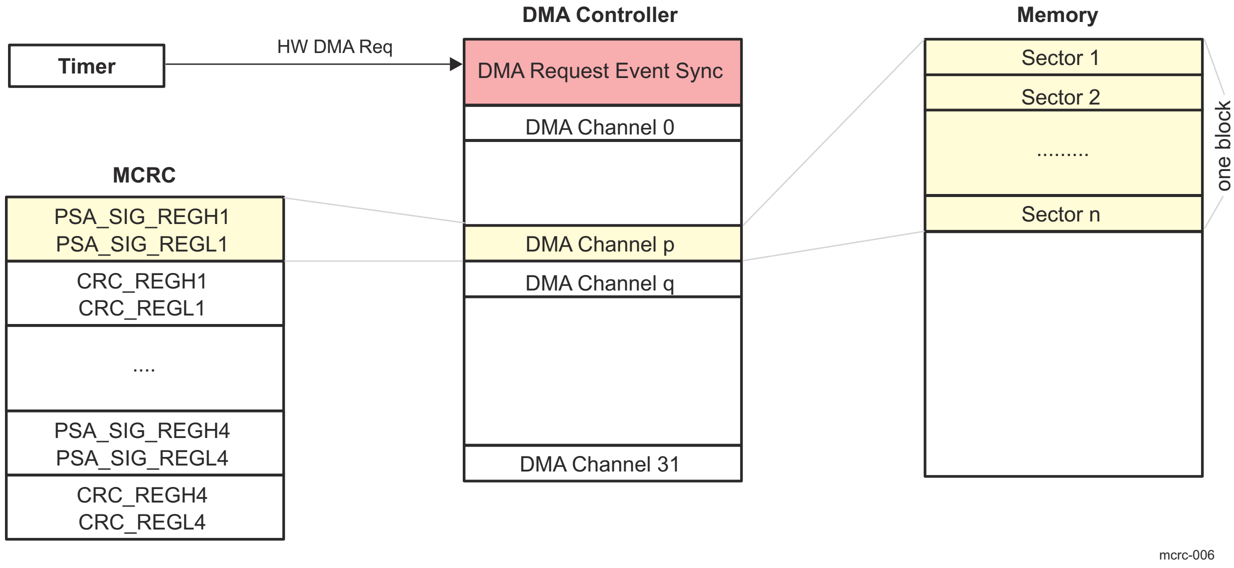

Figure 12-453. Semi-CPU Mode With Hardware Timer Trigger

Table 12-513. DMA Request and Counter Logic Operation According to CRC Mode

CRC Mode	DMA Request	Pattern Counter	Sector Counter	Timeout Counter
AUTO	Active	Active	Active	Active
Semi-CPU	Inactive	Active	Active	Active
Full CPU	Inactive	Inactive	Inactive	Inactive

12.6.3.3.9 Pattern Count Register

There is a 20-bit data pattern counter for every CRC channel. The data pattern counter is a down counter and can be pre-loaded with a programmable value stored in the Pattern Count Register (MCRC_CRC_PCOUNT_REG1-4). When the data pattern counter reaches zero, a compression complete interrupt is generated in Semi-CPU mode and an automatic signature verification is performed in AUTO mode. In AUTO only, DMA request is generated to trigger the DMA controller to update the CRC Value Register.

Note

The data pattern count must be divisible by the total transfer count as programmed in DMA controller. The total transfer count is the product of element count and frame count.

12.6.3.3.10 Sector Count Register/Current Sector Register

Each channel contains a 16-bit sector counter. The sector count register stores the number of sectors. Sector counter is a free running counter and is incremented by one each time when one sector of data patterns is compressed. When the signature verification fails, the current value stored in the sector counter is saved into current sector register (MCRC_CRC_CURSEC_REG1-4). If signature verification fails, CPU can read from the current sector register to identify the sector which causes the CRC mismatch. To aid and facilitate the CPU in determining the cause of a CRC failure it is advisable to use the following equation during CRC and DMA setup.

$$\text{CRC Pattern Count} \times \text{CRC Sector Count} = \text{DMA Element Count} \times \text{DMA Frame Count} \tag{12}$$

The current sector register is frozen from being updated until both the current sector register is read and CRC fail (CHi_CRC_FAIL) status bit is cleared by CPU. If CPU does not respond to the CRC failure in a timely manner before another sector produces a signature verification failure, the current sector register is not updated with the new sector number. An overrun interrupt is generate instead. If current sector register is already frozen with an erroneous sector and emulation is entered with SUSPEND signal goes to high then the register still remains frozen even it is read.

In Semi-CPU mode, the current sector register is used to indicate the sector for which the compression complete has last happened.

Current sector register is reset when the PSA software reset is enabled.

Note

Both data pattern count and sector count registers must be greater than or equal to one for the counters to count. After reset, pattern count and sector count registers default to zero and the associated counters are inactive.

12.6.3.3.11 Interrupts

CRC generate several types of interrupts per channel. Associated with each interrupt there is a interrupt enable bit (see MCRC_CRC_INTS). No interrupt is generated in Full-CPU mode.

- Compression complete interrupt
- CRC fail interrupt
- Overrun interrupt
- Underrun interrupt
- Timeout interrupt

Table 12-514. Interrupt Conditions Per CRC Mode

CRC Mode	Compression Complete	CRC Fail	Overrun	Underrun	Timeout
AUTO	No	Yes	Yes	Yes	Yes
Semi-CPU	Yes	No	Yes	No	Yes

Table 12-514. Interrupt Conditions Per CRC Mode (continued)

CRC Mode	Compression Complete	CRC Fail	Overrun	Underrun	Timeout
Full-CPU	No	No	No	No	No

12.6.3.3.11.1 Overrun Interrupt

Overrun Interrupt is generated in either AUTO or Semi-CPU mode. During AUTO mode, if a CRC fail is detected then the current sector number is recorded in the current sector register (MCRC_CRC_CURSEC_REG1-4). If CRC fail status bit is not cleared and current sector register is not read by the host CPU before another CRC fail is detected for another sector then an overrun interrupt is generated. During Semi-CPU mode, when the data pattern counter finishes counting, it generates a compression complete interrupt. At the same time the signature is copied into the PSA Sector Signature Register (MCRC_PSA_SECSIGREGL1-4). If the host CPU does not read the signature from PSA Sector Signature Register before it is updated again with a new signature value then an overrun interrupt is generated.

12.6.3.3.11.2 Timeout Interrupt

To ensure that the memory system is examined within a pre-defined time frame and no loss of incoming data there is a 24-bit timeout counter per CRC channel. The timeout counter can be pre-loaded with two different pre-load values, watchdog timeout pre-load value (MCRC_CRC_WDTOPLD1-4) and block complete timeout pre-load value (MCRC_CRC_BCTOPLD1-4). The timeout counter is clocked by a prescaler clock which is permanently running at division 64 of FICLK clock.

Watchdog timeout pre-load register (MCRC_CRC_WDTOPLD1-4) is used to check if DMA does supply a block of data responding to a request in a given time frame. Block complete timeout pre-load register (MCRC_CRC_BCTOPLD1-4) is used to check if one complete block of data patterns are compressed within a specific time frame. The timeout counter is first pre-loaded with MCRC_CRC_WDTOPLD1-4 after either AUTO or Semi-CPU mode is selected and starts to down count. If the timeout counter expires before DMA transfers any data pattern to PSA Signature Register then a timeout interrupt is generated. An incoming data pattern before the timeout counter expires will automatically pre-load the timeout counter with MCRC_CRC_BCTOPLD1-4 the block complete timeout pre-load value.

Block complete timeout pre-load value is used to check it one block of data patterns are compressed within a given time limit. If the timeout counter pre-loaded with MCRC_CRC_BCTOPLD1-4 value expires before one block of data patterns are compressed a timeout interrupt is generated. When one block (pattern count × sector count) of data patterns are compressed before the counter has expired, the counter is pre-loaded with MCRC_CRC_WDTOPLD1-4 value again. If the timeout counter is pre-loaded with zero then the counter is disable and no timeout interrupt is generated.

12.6.3.3.11.3 Underrun Interrupt

Underrun interrupt only occurs in AUTO mode. The interrupt is generated when the CRC Value Register is not updated with the corresponding signature when the data pattern counter finishes counting. During AUTO mode, MCRC Controller generates DMA request to update CRC Value Register in synchronization to the corresponding sector of the memory. Signature verification is also performed if underrun condition is detected. And CRC fail interrupt is generated at the same time as the underrun interrupt.

12.6.3.3.11.4 Compression Complete Interrupt

Compression complete interrupt is generated in Semi-CPU mode only. When the data pattern counter reaches zero, the compression complete flag is set and the interrupt is generated

12.6.3.3.11.5 Interrupt Offset Register

MCRC Controller only generates one interrupt request to interrupt manager. An interrupt offset register (MCRC_CRC_INT_OFFSET_REG) is provided to indicate the source of the pending interrupt with highest priority. Table 12-503 shows the offset interrupt vector address of each interrupt in an ascending order of priority.

Table 12-515. Interrupt Offset Mapping

Interrupt Condition	Offset Value
Phantom	0x0
Ch1 CRC Fail	0x1
Ch2 CRC Fail	0x2
Ch3 CRC Fail	0x3
Ch4 CRC Fail	0x4
reserved	0x5-0x8
Ch1 Compression Complete	0x9
Ch2 Compression Complete	0xA
Ch3 Compression Complete	0xB
Ch4 Compression Complete	0xC
reserved	0xD-0x10
Ch1 Overrun	0x11
Ch2 Overrun	0x12
Ch3 Overrun	0x13
Ch4 Overrun	0x14
reserved	0x15-0x18
Ch1 Underrun	0x19
Ch2 Underrun	0x1A
Ch3 Underrun	0x1B
Ch4 Underrun	0x1C
reserved	0x1D-0x20
Ch1 Timeout	0x21
Ch2 Timeout	0x22
Ch3 Timeout	0x23
Ch4 Timeout	0x24

12.6.3.3.11.6 Error Handling

When an interrupt is generated, host CPU must take appropriate actions to identify the source of error and restart the respective channel in DMA and MCRC module. To restart a CRC channel user must perform the following steps in the ISR:

1. Write to software reset bit in MCRC_CRC_CTRL0 register to reset the respective PSA Signature Register
2. Reset the CHi_MODE bits to 0 in MCRC_CRC_CTRL2 register as Data capture mode
3. Set the CHi_MODE bits in MCRC_CRC_CTRL2 register to desired new mode again
4. Release software reset

The host CPU must use byte write to restart each individual channel.

12.6.3.3.12 Power Down Mode

MCRC module can be put into power down mode when the power down control bit MCRC_CRC_CTRL1[0] PWDN is set. The module wakes up when the PWDN bit is cleared.

12.6.3.3.13 Emulation

A read access from a register in functional mode can sometimes trigger a certain internal event to follow. For example, reading interrupt offset register triggers an event to clear the corresponding interrupt status flag. During emulation when SUSPEND signal is high, a read access from any register should only return the register contents to the bus and should not trigger or mask any event as it would have in functional mode. This is to prevent debugger from reading the interrupt offset register, that is, during refreshing screen and cause the corresponding interrupt status flag to get cleared. Timeout counters are stopped to generate timeout interrupts in emulation mode. No VBUSM bus error will be generated if reading from the unimplemented locations. .

CEMUDBG is the VBUSM suspend signal which need not explicitly indicate that whether CPU is in suspend mode or not. In data trace mode, a separate suspend signal CPU_EMUSP, is used to indicate MCRC controller that the CPU is in suspend mode or not.

12.6.3.4 MCRC Programming Examples

12.6.3.4.1 Example: Auto Mode Using Time Based Event Triggering

A large memory area with 2 Mbyte (256 k × 32-bit [doubleword]) is to be checked in the background of CPU. CRC is to be performed every 1 Kbyte (128 doubleword). Therefore there will be 2048 pre-recorded CRC values. For illustration purpose, we map MCRC_CRC_REGL1 register to DMA channel 1 and MCRC_PSA_SIGREGL1 register to DMA channel 2. Let’s assume all DMA transfers are carried out in 64-bit transfer size.

12.6.3.4.1.1 DMA Setup

- Setup DMA channel 1 with the starting address from which the pre-determined CRC values are stored. Setup the destination address to the MCRC_CRC_REGL1. Put the source address at post increment addressing mode and put the destination address at constant addressing mode. Use hardware DMA request for channel 1 to trigger a frame transfer.
- Setup DMA channel 2 with the source address from which the contents of memory to be verified. Setup the destination address to the MCRC_PSA_SIGREGL1. Program the element transfer count to 128 and the frame transfer count to 2048. Program the read and write element size to 64 bits. Put the source address at post increment addressing mode and put the destination address at constant address mode. Use hardware DMA request for channel 2 to trigger an entire block transfer.

12.6.3.4.1.2 Timer Setup

The timer can be any general purpose timer which is capable of generating a time based DMA request.

- Setup Timer to generate DMA request associated with DMA channel 2. For example, software can setup the timer to generate a DMA request every 10 ms.

12.6.3.4.1.3 CRC Setup

- Program the pattern count MCRC_CRC_PCOUNT_REG1 to 128
- Program the sector count MCRC_CRC_SCOUNT_REG1 to 2048
- For example, we want the entire 2 Mbytes to be compressed within 5 ms. We can program the block complete timeout pre-load (MCRC_CRC_BCTOPLD1-4) value to 15625 (5 ms / (1 FICLK period × 64)) if CRC is operating at 200 MHz.
- Enable AUTO mode and all interrupts.

After AUTO mode is selected MCRC Controller automatically generates a DMA request on channel 1. Around the same time the timer module also generates a DMA request on DMA channel 2. When the first incoming data pattern arrives at the MCRC_PSA_SIGREGL1/H1, the MCRC Controller will compress it. After some time, the DMA controller would update the CMCRC_CRC_REGL1/H1 with a pre-determined value matching the calculated signature for the first sector of 128 64-bit data patterns. After one sector of data patterns are compressed, the MCRC Controller generate a CRC fail interrupt if signature stored at the MCRC_PSA_SECSIGREGL1/H1 does not match the MCRC_CRC_REGL1/H1 Register. MCRC Controller generates a DMA request on DMA channel 1 when one sector of data patterns are compressed. This routine will continue until the entire 2 Mbytes are consumed. If the timeout counter reached zero before the entire 2 Mbytes are compressed, a timeout interrupt is generated. After 2Mbytes are transferred, the DMA can generate an interrupt to CPU. The entire operation will continue again when DMA responds to the DMA request from both the timer and MCRC Controller. The CRC is performed totally without any CPU intervention.

12.6.3.4.2 Example: Auto Mode Without Using Time Based Triggering

A small but highly secured memory area with 1 Kbytes is to be checked in the background of CPU. CRC is to be performed every 1 Kbytes. Therefore, there is only one pre-recorded CRC value. For illustration purpose, we map channel 1 MCRC_CRC_REGL1/H1 to DMA channel 1 and channel 1 MCRC_PSA_SIGREGL1/H1 to DMA channel 2. Assume all transfers carried out by DMA are in 64-bit transfer size.

12.6.3.4.2.1 DMA Setup

- Setup DMA channel 1 with the source address from which the pre-determined CRC value is stored. Setup the destination address to the MCRC_CRC_REGL1 Register. Put the source address at constant addressing mode and put the destination address at constant addressing mode. Use hardware DMA request for channel 1.

- Setup DMA channel 2 with the source address from which the memory area to be verified. Setup the destination address to the MCRC_PSA_SIGREGL1/H1. Program the element transfer count to 128 and the frame transfer count to 1. Put the source address at post increment addressing mode and put the destination address at constant address mode. Generate a software DMA request on channel 2 after CRC has completed its setup. Enable autoinitiation for DMA channel 2.

12.6.3.4.2.2 CRC Setup

- Program the MCRC_CRC_PCOUNT_REG1 to 128
- Program the MCRC_CRC_SCOUNT_REG1 to 1
- Leaving the timeout count MCRC_CRC_BCTOPLD1 register with the reset value of zero means no timeout interrupt is generated
- Enable AUTO mode and all interrupts

After AUTO mode is selected the MCRC Controller automatically generates a DMA request on channel 1. At the same time the CPU generates a software DMA request on DMA channel 2. When the first incoming data pattern arrives at the MCRC_PSA_SIGREGL1/H1, the MCRC Controller will compress it. After some time, the DMA controller would update the MCRC_CRC_REGL1/H1 with a pre-determined value matching the calculated signature for the first sector of 128 64-bit data patterns. After one sector of data patterns are compressed, the MCRC Controller generate a CRC fail interrupt if signature stored at the MCRC_PSA_SECSIGREGL1/H1 does not match the MCRC_CRC_REGL1/H1. MCRC Controller generate a DMA request on DMA channel 1 again after one sector is compressed. After 1 Kbytes are transferred, the DMA can generate an interrupt to CPU. Responding to the DMA interrupt CPU can restart the CRC routine by generating a software DMA request onto channel 2 again.

12.6.3.4.3 Example: Semi-CPU Mode

If DMA controller is available in a system the CRC module can also operate in semi-CPU mode. This means that CPU can still make use of the DMA to perform data patterns transfer to CRC controller in the background. The difference between semi-CPU mode and AUTO mode is that CRC controller does not automatically perform the signature verification. CRC controllers generates a compression complete interrupt to CPU when the one sector of data patterns are compressed. CPU needs to perform the signature verification itself.

A memory area with 2 Mbytes is to be verified with the help of the CPU. CRC operation is to be performed every 1 Kbyte. Since there are 2 Mbytes (256 K doublewords) of memory to be check and we want to perform a CRC every 1 Kbytes (128 doublewords) and therefore there must be 2048 pre-recorded CRC values. In Semi-CPU mode, the MCRC_CRC_REGL1/H1 is not updated and contains indeterminate data.

12.6.3.4.3.1 DMA Setup

- Setup DMA channel 1 with the source address from which the memory area to be verified are mapped. Setup the destination address to the MCRC_PSA_SIGREGL1/H1. Put the starting address at post increment addressing mode and put the destination address at constant address mode. Use hardware DMA request to trigger an entire block transfer for channel 1. Disable autoinitiation for DMA channel 1.

12.6.3.4.3.2 Timer Setup

The timer can be any general purpose timer which is capable of generating a time-based DMA request.

- Setup Timer to generate DMA request associated with DMA channel 1. For example, software can setup the timer to generate a DMA request every 10 ms.

12.6.3.4.3.3 CRC Setup

- Program the MCRC_CRC_PCOUNT_REG1 to 128
- Program the MCRC_CRC_SCOUNT_REG1 to 2048
- For example, we want the entire 2 Mbytes to be compressed within 5 ms. We can program the block complete timeout pre-load value MCRC_CRC_BCTOPLD1 to 15625 (5 ms / (1 FICLK period × 64)) if CRC is operating at 200 MHz
- Enable AUTO mode and all interrupts.

The timer module first generates a DMA request on DMA channel 1 when it is enabled. When the first incoming data pattern arrives at the MCRC_PSA_SIGREGL1/H1, the CRC controller will compress it. After one sector of data patterns are compressed, the CRC controller generate a compression complete interrupt. Upon responding to the interrupt the CPU would read from the MCRC_PSA_SECSIGREGL1/H1. It is up to the CPU on how to deal with the PSA value just read. It can compare it to a known signature value or it can write it to another memory location to build a signature file or even transfer the signature out of the device via SCI or SPI. This routine will continue until the entire 2 Mbytes are consumed. The latency of the interrupt response from CPU can cause overrun condition. If CPU does not read from MCRC_PSA_SECSIGREGL1 before the PSA value is overridden with the signature of the next sector of memory, an overrun interrupt will be generated by CRC controller.

12.6.3.4.4 Example: Full-CPU Mode

In a system without the availability of DMA controller, the CRC routine can be operated by CPU provided the CPU has enough throughput. CPU needs to read from the memory area from which CRC is to be performed.

A memory area with 2 Mbytes is to be checked with the help of the CPU. CRC operation is to be performed every 1 Kbyte. In CPU mode, the MCRC_CRC_REGL1/H1 is not updated and contains indeterminate data.

12.6.3.4.4.1 CRC Setup

- All control registers can be left in their reset state. Only enable Full-CPU mode.

CPU itself reads from the memory and write the data to the MCRC_PSA_SIGREGL1/MCRC_PSA_SIGREGH1 inside MCRC Controller. When the first incoming data pattern arrives at the MCRC_PSA_SIGREGL1/MCRC_PSA_SIGREGH1, the MCRC Controller will compress it. After n data patterns are compressed, CPU can read from the MCRC_PSA_SIGREGL1/MCRC_PSA_SIGREGH1. It is up to the CPU on how to deal with the PSA signature value just read. It can compare it to a known signature value stored at another memory location.

12.6.4 ECC Aggregator

This section describes the common ECC aggregator functionality.

12.6.4.1 ECC Aggregator Overview

To increase functional and system reliability the memories (for example, FIFOs, queues, SRAMs and others) in many device modules and subsystems are protected by error correcting code (ECC). This is accomplished through an ECC aggregator and ECC wrapper. The ECC aggregator is connected to these memories (hereinafter ECC RAMs) and involved in the ECC process. Each memory is surrounded by an ECC wrapper which performs the ECC detection and correction. The wrapper communicates via serial interface with the aggregator which has memory mapped configuration interface.

The ECC aggregator is also connected to interconnect ECC components that protect the command, address and data buses of the system interconnect. ECC is calculated for the data bus and parity and redundancy for the command and address buses. Each interconnect ECC component has the same serial interface for communication with the aggregator as the ECC wrapper. An ECC aggregator may be connected to both endpoints - the ECC wrapper and interconnect ECC component.

The ECC aggregator, ECC wrapper and interconnect ECC component are considered as single entity and are hereinafter referred to as ECC aggregator unless otherwise explicitly specified.

Table 12-504 lists the device modules and subsystems which have ECC aggregator.

Table 12-516. Device Modules and Subsystems with ECC Aggregator

Module Instance	Domain	
	MCU	MAIN
PSRAMECC0	-	✓
CBASS0	-	✓
USB0	-	✓
MMCSD0	-	✓
MMCSD1	-	✓
FSS0_OSPI0	-	✓
GICSS0	-	✓
A53SS0	-	✓
PCIE0	-	✓
MCAN0	-	✓
MCAN1	-	✓
R5FSS0	-	✓
R5FSS1	-	✓
MSRAM_256K0 to MSRAM_256K7	-	✓
PRU_ICSSG0	-	✓
PRU_ICSSG1	-	✓
MCU_CBASS0	✓	-
MCU_M4FSS0	✓	-

12.6.4.1.1 ECC Aggregator Features

The ECC aggregator has the following features:

- Reduces memory software errors via single error correction (SEC) and double error detection (DED)
- Provides a mechanism to control and monitor the ECC protected memories in a module or subsystem
- Generates an interrupt for correctable error
- Generates an interrupt for non-correctable error
- Supports inject only mode for diagnostic purposes
- Supports software readable status for single and double-bit ECC errors and associated information such as row address where error has occurred and data bits that have been flipped
- Supports up to 256 ECC endpoints. An ECC endpoint is ECC RAM
- Detects single bit error via parity checking on:
  - Memory mapped configuration interface FIFO
  - Serial interface FIFO
  - Serial interface transaction
- Single bit error detection via parity checking results in a non-correctable error interrupt
- Supports timeout mechanism on transactions over the ECC serial interface. Timeout occurrence results in a non-correctable error interrupt.
- Certain control bits have redundancy and if a bit flips an interrupt is generated

12.6.4.2 ECC Aggregator Integration

This section describes an ECC aggregator integration in the device, including information about clocks, resets, and hardware requests.

Note

For a list of the device modules and subsystems which have ECC aggregator, see Table 12-504.

Table 12-505 shows the integration of an ECC aggregator module.

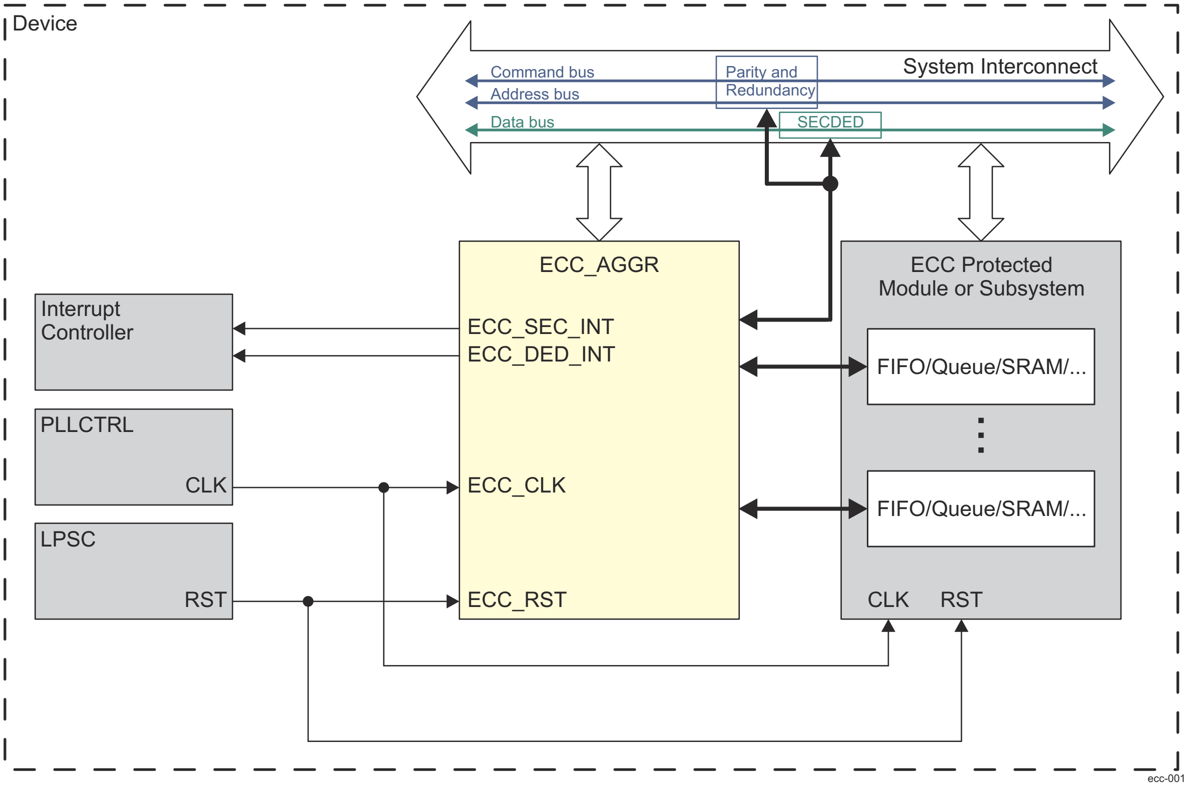

Figure 12-454. ECC Aggregator Integration

Table 12-505 through Table 12-508 summarize the integration of an ECC aggregator module.

Table 12-517. ECC Aggregator Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Interconnect
ECC_AGGR	Same PSC as the corresponding module or subsystem	Same PD as the corresponding module or subsystem	Same LPSC as the corresponding module or subsystem	Same CBASS as the corresponding module or subsystem

Table 12-518. ECC Aggregator Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
ECC_AGGR	ECC_CLK	Same as the corresponding module or subsystem(1)	Same as the corresponding module or subsystem(1)	ECC aggregator clock

(1) For information about clock and reset sources, see the respective *Clocks and Resets* table of the module or subsystem with ECC aggregator.

Table 12-519. ECC Aggregator Resets

Module Instance	Module Reset Input	Source Reset Signal	Source	Description
ECC_AGGR	ECC_RST	Same as the corresponding module or subsystem(1)	Same as the corresponding module or subsystem(1)	ECC aggregator reset

Table 12-520. ECC Aggregator Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ECC_AGGR	ECC_SEC_INT	See (1)	See (1)	Interrupt for correctable error (SEC)	Level
	ECC_DED_INT	See (1)	See (1)	Interrupt for non-correctable error (DED, parity, redundancy, timeout)	Level

(1) See the respective *Hardware Requests* table of the module or subsystem with ECC aggregator.

Table 12-521. ECC Aggregator DMA Events

Module Instance	Module DMA Event	Destination DMA Event Input	Destination	Description	Type
ECC_AGGR	-	-	-	-	-

Note

For more information on the interrupts, see Section 12.6.4.3.5 , *Interrupts*.

For more information on the interconnects, see Chapter 3 , *System Interconnect*.

For more information on the power, reset and clock management, see the corresponding sections within Chapter 5 , *Device Configuration*.

For more information on the device interrupt controllers, see Section 9.2 , *Interrupt Controllers*.

12.6.4.3 ECC Aggregator Functional Description

This section describes the architecture and functional details of the ECC aggregator.

12.6.4.3.1 ECC Aggregator Block Diagram

Figure 12-455 shows the ECC aggregator block diagram.

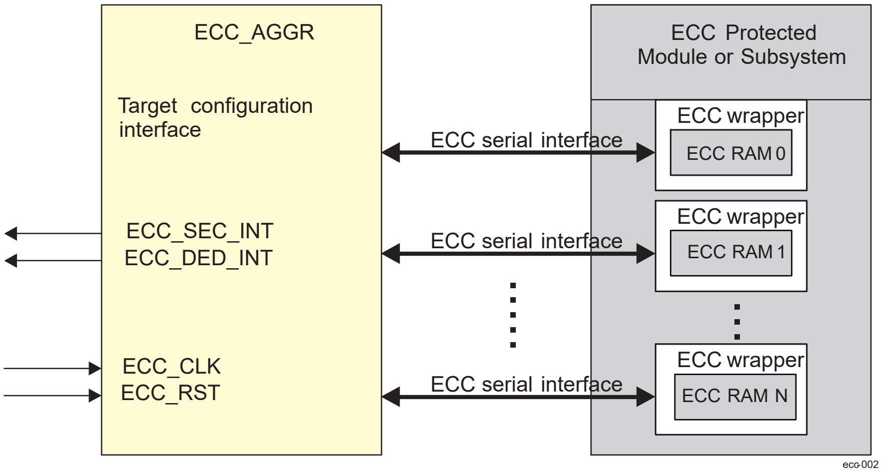

Figure 12-455. ECC Aggregator Block Diagram

The ECC aggregator is connected to one or more ECC endpoints each of which has assigned a unique ID used when the endpoint is accessed for status information or configuration. The ECC aggregator provides software access to all ECC related registers through its memory mapped target configuration interface while the serial interface is used to communicate with the ECC endpoints. Upon detection of single or double-bit error the corresponding interrupt line is asserted.

12.6.4.3.2 ECC Aggregator Register Groups

The ECC aggregator has ECC control, status and interrupt registers for each ECC endpoint in a module or subsystem. These registers are memory mapped and occupy 1 KB address space although part of it may contain reserved locations. The registers are split in the following types:

- **Global registers**. They are common to all ECC endpoints associated with the ECC aggregator and include the ECC_VECTOR and ECC_REV registers. Each ECC endpoint has assigned a unique ID. When this ID is written to the ECC_VECTOR[10-0] ECC_VECTOR field the corresponding endpoint is selected either for control or for status reading.
- **ECC control and status registers**. These registers are specific to each ECC endpoint and reside in the range from address offset 0x10 to 0x24 for the ECC RAM endpoint. They are memory mapped but are accessed through the ECC serial interface. They are also selected by the ECC endpoint ID written to the ECC_VECTOR[10-0] ECC_VECTOR field. Because of latency on the serial interface the ECC control and status registers are read by performing special sequence as described in Section 12.6.4.3.3 . These registers have also different functionality for types of ECC endpoints.
- **Interrupt registers**. They include interrupt status, interrupt enable, interrupt disable, and EOI registers. For more information, see Section 12.6.4.3.5 .

12.6.4.3.3 Read Access to the ECC Control and Status Registers

Read accesses to the ECC control and status registers for each ECC endpoint represent read operations over the ECC serial interface and are triggered by performing the following sequence:

1. Software writes the following in the ECC_VECTOR register:

  - The ECC endpoint ID in the ECC_VECTOR[10-0] ECC_VECTOR field to select particular ECC endpoint.
  - The register read address in the ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field to select which register has to be read through the ECC serial interface.
  - A value of 0x1 in the ECC_VECTOR[15] RD_SVBUS bit to trigger read operation through the ECC serial interface.
2. Software polls the ECC_VECTOR[24] RD_SVBUS_DONE bit to check if it is 0x1. This indicates that the read operation on the ECC serial interface has completed.
3. Software reads the data from the register previously selected by the ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field.

The following is an example for serial read operation:

1. Write 0x0010 8005 to the ECC_VECTOR register. This sends read request to the ECC_WRAP_REV register (address = 0x10) associated with ECC endpoint with ID = 5.
2. Poll the ECC_VECTOR[24] RD_SVBUS_DONE bit until value of 0x1 is read.
3. Read the ECC_WRAP_REV register to get its value.

12.6.4.3.4 Serial Write Operation

Write operations over the ECC serial interface are performed as follows:

1. Software specifies the ECC endpoint ID in the ECC_VECTOR[10-0] ECC_VECTOR field. The ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field is a don't care but the ECC_VECTOR[15] RD_SVBUS bit must be set to 0x0.
2. Software performs regular write operation to the desired address. If the ECC endpoint ID has already been specified, step 1 can be skipped. Unlike serial read operations it is not necessary to always specify the endpoint ID before performing serial write operation.

The following is an example for serial write operation:

1. Write 0x0000 0008 to the ECC_VECTOR register.
2. Write 0x0000 000F to the ECC_CTRL register. This sends write request with data 0x0000 000F to the ECC_CTRL register associated with ECC RAM with ID = 8.

12.6.4.3.5 Interrupts

The ECC aggregator generates the following interrupts:

- Correctable interrupt (ECC_SEC_INT) where hardware can correct the error but notifies the system in case of SEC.
- Non-correctable interrupt (ECC_DED_INT) where hardware cannot correct the error in cases of DED, parity check, redundancy check or timeout occurrence.

The following is the sequence for servicing interrupts:

- Software enables the interrupts for an ECC endpoint by writing 0x1 to the corresponding bit of the following interrupt enable register:
  - ECC_SEC_ENABLE_SET_REG0 for the correctable interrupt
  - ECC_DED_ENABLE_SET_REG0 for the non-correctable interrupt
- On receiving an interrupt, software checks which ECC endpoint has caused the error by reading the following interrupt status register:
  - ECC_SEC_STATUS_REG0 for the correctable interrupt
  - ECC_DED_STATUS_REG0 for the non-correctable interrupt
- Software performs serial read operations as described in Section 12.6.4.3.3 to read the following status registers that contain details about the error:
  - The endpoint is ECC RAM:
    - ECC_ERR_STAT1
    - ECC_ERR_STAT2

    - ECC_ERR_STAT3
- After the interrupt has been serviced, depending on the error type, software should clear the corresponding status bits in the ECC_ERR_STAT1 and ECC_ERR_STAT3 registers or in the ECC_CBASS_ERR_STAT1 register. Software has to poll these registers to guarantee that status bits are cleared as there is no other indication for write completion over the ECC serial interface.
  The value of the *_PEND_CLR fields in the ECC_CBASS_ERR_STAT1 register must be read and then written back to decrement the count of each field back to 0x0. A further error capture into the ECC_CBASS_ERR_STAT1 register does not occur unless all its fields are 0x0. The decrement value should not be larger than the read value. If a field in the ECC_CBASS_ERR_STAT1 register should not be modified, write a value of 0x0 to that field.
- Software writes 0x1 to the corresponding end of interrupt register to clear the interrupt:
  - ECC_SEC_EOI_REG for the correctable interrupt
  - ECC_DED_EOI_REG for the non-correctable interrupt

12.6.4.3.6 Inject Only Mode

There are modules that already perform the ECC generation and checking as part of their data path. In this case, the ECC wrapper may be configured in inject only mode, if needed. In this mode the ECC wrapper does not perform ECC detection and correction. The inject only mode allows users to inject single or double-bit errors so that the module logic can be tested for diagnostic purposes.

There is error injection logic for testing of the error checking logic (checkers). The injection logic can be configured to inject either single or double bit error. The ECC_ERR_CTRL1 and ECC_ERR_CTRL2 registers should be written first to setup the injection. Then, either the ECC_CTRL[3] FORCE_SEC or the ECC_CTRL[4] FORCE_DED bit must be set to 0x1 to start the injection. Both bits must not be set at the same time. If the injection should continue in incrementing mode, then the ECC_CTRL[5] FORCE_N_BIT bit should be set to 0x1. Once the FORCE_N_BIT is set, then each successive injection can simply write the ECC_CTRL register to set the FORCE_SEC or FORCE_DED again. Reading 0x0 from either the FORCE_SEC or the FORCE_DED bit indicates that the injection has completed, as these bits automatically clear when the checker indicates that it has performed the injection. The time for an injection to complete is not guaranteed, so some delay is needed between successive injections.

12.6.4.4 ECC Aggregators Interconnect

- Properties of ECC Aggregator Instance ADC0
- Properties of ECC Aggregator Instance COMPUTE_CLUSTER0
- Properties of ECC Aggregator Instance CPSW0
- Properties of ECC Aggregator Instance DMASS0
- Properties of ECC Aggregator Instance DMSC0
- Properties of ECC Aggregator Instance ECC_AGGR0
- Properties of ECC Aggregator Instance ECC_AGGR1
- EDC Checkers Information of ECC Aggregator Instance ECC_AGGR1
- Properties of ECC Aggregator Instance FSS0
- Properties of ECC Aggregator Instance GICSS0
- Properties of ECC Aggregator Instance MCAN0
- EDC Checkers Information of ECC Aggregator Instance MCAN0
- Properties of ECC Aggregator Instance MCAN1
- EDC Checkers Information of ECC Aggregator Instance MCAN1
- Properties of ECC Aggregator Instance MCU_ECC_AGGR0
- EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0
- Properties of ECC Aggregator Instance MCU_M4FSS0
- EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0
- Properties of ECC Aggregator Instance MMCSD0
- Properties of ECC Aggregator Instance MMCSD1
- Properties of ECC Aggregator Instance MSRAM_256K0
- Properties of ECC Aggregator Instance MSRAM_256K1
- Properties of ECC Aggregator Instance MSRAM_256K2

- Properties of ECC Aggregator Instance MSRAM_256K3
- Properties of ECC Aggregator Instance MSRAM_256K4
- Properties of ECC Aggregator Instance MSRAM_256K5
- Properties of ECC Aggregator Instance MSRAM_256K6
- Properties of ECC Aggregator Instance MSRAM_256K7
- Properties of ECC Aggregator Instance PCIE0
- Properties of ECC Aggregator Instance PDMA0
- Properties of ECC Aggregator Instance PDMA1
- Properties of ECC Aggregator Instance PRU_ICSSG0
- Properties of ECC Aggregator Instance PRU_ICSSG1
- Properties of ECC Aggregator Instance PSRAMECC0
- Properties of ECC Aggregator Instance R5FSS0
- Properties of ECC Aggregator Instance R5FSS1
- Properties of ECC Aggregator Instance SA2_UL0
- Properties of ECC Aggregator Instance USB0
- Properties of ECC Aggregator Instance VTM0
- EDC Checkers Information of ECC Aggregator Instance VTM0

Table 12-522. Properties of ECC Aggregator Instance ADC0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ADC12_CORE_FIFO_RAM0_TPRAM_ECC	0	ECC Wrapper	Inject with error capture	Yes	16	512 B
ADC12_CORE_FIFO_RAM1_TPRAM_ECC	1	ECC Wrapper	Inject with error capture	Yes	16	512 B

Table 12-523. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS	0	ECC Wrapper	Inject only	Yes	42	10 KB
CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS	1	ECC Wrapper	Inject only	Yes	42	10 KB
CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS	2	ECC Wrapper	Inject only	Yes	42	10 KB
CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS	3	ECC Wrapper	Inject only	Yes	42	10 KB
CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS	4	ECC Wrapper	Inject only	Yes	32	1 KB
CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS	5	ECC Wrapper	Inject only	Yes	32	1 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS	6	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS	7	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS	8	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS	9	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS	10	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS	11	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS	12	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS	13	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS	14	ECC Wrapper	Inject only	Yes	31	496 B

Table 12-523. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS	15	ECC Wrapper	Inject only	Yes	31	496 B
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS	16	ECC Wrapper	Inject only	Yes	31	496 B
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS	17	ECC Wrapper	Inject only	Yes	31	496 B
CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS	18	ECC Wrapper	Inject only	Yes	12	384 B
CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS	19	ECC Wrapper	Inject only	Yes	117	3 KB
CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS	20	ECC Wrapper	Inject only	Yes	117	3 KB
CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS	21	ECC Wrapper	Inject only	Yes	117	3 KB
CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS	22	ECC Wrapper	Inject only	Yes	117	3 KB
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS	23	ECC Wrapper	Inject only	Yes	38	608 B
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS	24	ECC Wrapper	Inject only	Yes	38	608 B
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS	25	ECC Wrapper	Inject only	Yes	38	608 B
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS	26	ECC Wrapper	Inject only	Yes	38	608 B
CPU0_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS	0	ECC Wrapper	Inject only	Yes	42	10 KB
CPU0_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS	1	ECC Wrapper	Inject only	Yes	42	10 KB
CPU0_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS	2	ECC Wrapper	Inject only	Yes	42	10 KB
CPU0_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS	3	ECC Wrapper	Inject only	Yes	42	10 KB
CPU0_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS	4	ECC Wrapper	Inject only	Yes	32	1 KB
CPU0_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS	5	ECC Wrapper	Inject only	Yes	32	1 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS	6	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS	7	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS	8	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS	9	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS	10	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS	11	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS	12	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS	13	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS	14	ECC Wrapper	Inject only	Yes	31	496 B
CPU0_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS	15	ECC Wrapper	Inject only	Yes	31	496 B
CPU0_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS	16	ECC Wrapper	Inject only	Yes	31	496 B

Table 12-523. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS	17	ECC Wrapper	Inject only	Yes	31	496 B
CPU0_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS	18	ECC Wrapper	Inject only	Yes	12	384 B
CPU0_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS	19	ECC Wrapper	Inject only	Yes	117	3 KB
CPU0_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS	20	ECC Wrapper	Inject only	Yes	117	3 KB
CPU0_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS	21	ECC Wrapper	Inject only	Yes	117	3 KB
CPU0_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS	22	ECC Wrapper	Inject only	Yes	117	3 KB
CPU0_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS	23	ECC Wrapper	Inject only	Yes	38	608 B
CPU0_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS	24	ECC Wrapper	Inject only	Yes	38	608 B
CPU0_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS	25	ECC Wrapper	Inject only	Yes	38	608 B
CPU0_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS	26	ECC Wrapper	Inject only	Yes	38	608 B
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY0_ECC_SVBUS	0	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY1_ECC_SVBUS	1	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY2_ECC_SVBUS	2	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY3_ECC_SVBUS	3	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY4_ECC_SVBUS	4	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY5_ECC_SVBUS	5	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY6_ECC_SVBUS	6	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY7_ECC_SVBUS	7	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY8_ECC_SVBUS	8	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY9_ECC_SVBUS	9	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY10_ECC_SVBUS	10	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY11_ECC_SVBUS	11	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY12_ECC_SVBUS	12	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY13_ECC_SVBUS	13	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY14_ECC_SVBUS	14	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_TAGRAM_SPRAM_WAY15_ECC_SVBUS	15	ECC Wrapper	Inject only	Yes	39	1 KB
A53_DUAL_U_L2_DATARAM_SPRAM_0_ECC_SVBUS	16	ECC Wrapper	Inject only	Yes	72	36 KB
A53_DUAL_U_L2_DATARAM_SPRAM_1_ECC_SVBUS	17	ECC Wrapper	Inject only	Yes	72	36 KB
A53_DUAL_U_L2_DATARAM_SPRAM_2_ECC_SVBUS	18	ECC Wrapper	Inject only	Yes	72	36 KB
A53_DUAL_U_L2_DATARAM_SPRAM_3_ECC_SVBUS	19	ECC Wrapper	Inject only	Yes	72	36 KB
A53_DUAL_U_L2_DATARAM_SPRAM_4_ECC_SVBUS	20	ECC Wrapper	Inject only	Yes	72	36 KB
A53_DUAL_U_L2_DATARAM_SPRAM_5_ECC_SVBUS	21	ECC Wrapper	Inject only	Yes	72	36 KB

Table 12-523. Properties of ECC Aggregator Instance COMPUTE_CLUSTER0 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
A53_DUAL_U_L2_DATARAM_SPRAM_6_ECC_SVBUS	22	ECC Wrapper	Inject only	Yes	72	36 KB
A53_DUAL_U_L2_DATARAM_SPRAM_7_ECC_SVBUS	23	ECC Wrapper	Inject only	Yes	72	36 KB

Table 12-524. Properties of ECC Aggregator Instance CPSW0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ALE_RAM	0	ECC Wrapper	Inject with error capture	Yes	568	4 KB
P0_RX_FIFO	1	ECC Wrapper	Inject with error capture	Yes	256	32 B
P0_TX_FIFO	2	ECC Wrapper	Inject with error capture	Yes	256	32 B
P1_RX_FIFO	3	ECC Wrapper	Inject with error capture	Yes	256	32 B
P1_TX_FIFO	4	ECC Wrapper	Inject with error capture	Yes	256	32 B
P2_RX_FIFO	5	ECC Wrapper	Inject with error capture	Yes	256	32 B
P2_TX_FIFO	6	ECC Wrapper	Inject with error capture	Yes	256	32 B
EST_RAM	19	ECC Wrapper	Inject with error capture	Yes	22	704 B

Table 12-525. Properties of ECC Aggregator Instance DMASS0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
DMSS_AM64_PKTDMA_CFG_CONFIG	0	ECC Wrapper	Inject with error capture	Yes	96	3 KB
DMSS_AM64_PKTDMA_CFG_STATE	1	ECC Wrapper	Inject with error capture	Yes	220	2 KB
DMSS_AM64_PKTDMA_TPCFIFO_F0	2	ECC Wrapper	Inject with error capture	Yes	141	4 KB
DMSS_AM64_PKTDMA_TPCFIFO_F1	3	ECC Wrapper	Inject with error capture	Yes	141	4 KB
DMSS_AM64_PKTDMA_RPCFIFO_F0	4	ECC Wrapper	Inject with error capture	Yes	128	3 KB
DMSS_AM64_PKTDMA_RPCFIFO_F1	5	ECC Wrapper	Inject with error capture	Yes	128	3 KB
DMSS_AM64_PKTDMA_RPCFIFO_WC	6	ECC Wrapper	Inject with error capture	Yes	22	957 B
DMSS_AM64_PKTDMA_STATS_STST0	7	ECC Wrapper	Inject with error capture	Yes	96	504 B
DMSS_AM64_PKTDMA_STATS_STSR0	8	ECC Wrapper	Inject with error capture	Yes	128	464 B
DMSS_AM64_PKTDMA_RINGOCC_CNTR	9	ECC Wrapper	Inject with error capture	Yes	18	1 KB
DMSS_AM64_BCDMA_CFG_CONFIG	10	ECC Wrapper	Inject with error capture	Yes	86	1 KB
DMSS_AM64_BCDMA_CFG_STATE	11	ECC Wrapper	Inject with error capture	Yes	400	5 KB
DMSS_AM64_BCDMA_PCFIFO_DFIFO_F0	12	ECC Wrapper	Inject with error capture	Yes	128	3 KB
DMSS_AM64_BCDMA_PCFIFO_DFIFO_F1	13	ECC Wrapper	Inject with error capture	Yes	128	3 KB
DMSS_AM64_BCDMA_TPCFIFO_F0	14	ECC Wrapper	Inject with error capture	Yes	141	2 KB
DMSS_AM64_BCDMA_TPCFIFO_F1	15	ECC Wrapper	Inject with error capture	Yes	141	2 KB
DMSS_AM64_BCDMA_RPCFIFO_F0	16	ECC Wrapper	Inject with error capture	Yes	128	2 KB
DMSS_AM64_BCDMA_RPCFIFO_F1	17	ECC Wrapper	Inject with error capture	Yes	128	2 KB
DMSS_AM64_BCDMA_RPCFIFO_WC	18	ECC Wrapper	Inject with error capture	Yes	19	570 B
DMSS_AM64_BCDMA_STATS_STST0	19	ECC Wrapper	Inject with error capture	Yes	96	672 B
DMSS_AM64_BCDMA_STATS_STSR0	20	ECC Wrapper	Inject with error capture	Yes	96	672 B
DMSS_AM64_BCDMA_RINGOCC_CNTR	21	ECC Wrapper	Inject with error capture	Yes	18	306 B
DMSS_AM64_INTAGGR_STATREG_SR_SPRAM_184X128_SWW_SR	22	ECC Wrapper	Inject with error capture	Yes	128	3 KB
DMSS_AM64_INTAGGR_COMMON_IM_TPRAM_2250X34_SWW_SR	23	ECC Wrapper	Inject with error capture	Yes	34	9 KB
DMSS_AM64_IPCSS_RINGACC_STRAM	24	ECC Wrapper	Inject with error capture	Yes	216	864 B
DMSS_AM64_IPCSS_SEC_PROXY_BUF_STRAM	25	ECC Wrapper	Inject with error capture	Yes	91	865 B
DMSS_AM64_IPCSS_SEC_PROXY_BUFRAM	26	ECC Wrapper	Inject with error capture	Yes	64	64 B

Table 12-526. Properties of ECC Aggregator Instance DMSC0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ISRAM1_RAMECC	0	ECC Wrapper	Inject with error capture	Yes	32	64 KB
ISRAM0_RAMECC	1	ECC Wrapper	Inject with error capture	Yes	32	64 KB
IM_RAMECC	2	ECC Wrapper	Inject with error capture	Yes	15	480 B
SR_RAMECC	3	ECC Wrapper	Inject with error capture	Yes	128	2 KB

Table 12-527. Properties of ECC Aggregator Instance ECC_AGGR0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ITIMER_MGR1024_MAIN_0_TIMER_FSM_RAMECC	0	ECC Wrapper	Inject with error capture	Yes	32	4 KB
ITIMER_MGR1024_MAIN_0_REPROG_FSM_RAMECC	1	ECC Wrapper	Inject with error capture	Yes	32	4 KB
ITIMER_MGR1024_MAIN_0_EFIFO_RAMECC	2	ECC Wrapper	Inject with error capture	Yes	11	1 KB

Table 12-528. Properties of ECC Aggregator Instance ECC_AGGR1

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
IMAILBOX8_MAIN_0_RAMECC	0	ECC Wrapper	Inject with error capture	Yes	32	2 KB
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	EDC Interconnect See Table 12-517	Inject with error capture	Yes		
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	EDC Interconnect See Table 12-517	Inject with error capture	Yes		
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	3	EDC Interconnect See Table 12-517	Inject with error capture	Yes		
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	EDC Interconnect See Table 12-517	Inject with error capture	Yes		
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	5	EDC Interconnect See Table 12-517	Inject with error capture	Yes		

Table 12-529. EDC Checkers Information of ECC Aggregator Instance ECC_AGGR1

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	0	1	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	1	32	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	2	1	Redundant
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	3	1	Redundant
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	4	1	Redundant
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	5	1	Redundant
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	6	1	Redundant
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	7	8	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	8	8	Parity

Table 12-529. EDC Checkers Information of ECC Aggregator Instance ECC_AGGR1 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	9	8	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	10	8	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	11	1	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC	1	12	1	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	0	1	Redundant
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	1	32	Error Detect and Correct
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	2	1	Redundant
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	3	3	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	4	1	Redundant
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	5	4	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	6	12	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	7	12	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	8	10	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	9	3	Parity
IAM64_MAIN_INFRA_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	2	10	1	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	3	0	1	Redundant
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	3	1	1	Redundant
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	3	2	10	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC	3	3	3	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	0	1	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	1	1	Redundant
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	2	10	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	3	3	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	4	3	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	5	1	Parity

Table 12-529. EDC Checkers Information of ECC Aggregator Instance ECC_AGGR1 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	6	1	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	7	2	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	8	3	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	9	1	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	10	10	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	11	5	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	12	3	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	13	4	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC	4	14	4	Parity
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	5	0	1	Redundant
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	5	1	32	Error Detect and Correct
IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC	5	2	1	Redundant

Table 12-530. Properties of ECC Aggregator Instance FSS0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
OSPI_OSPI_WRAP_SRAM	0	ECC Wrapper	Inject with error capture	Yes	32	1 KB

Table 12-531. Properties of ECC Aggregator Instance GICSS0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ICB_RAMECC	0	ECC Wrapper	Inject only	Yes	16	576 B
ITE_RAMECC	1	ECC Wrapper	Inject only	Yes	57	456 B
LPI_RAMECC	2	ECC Wrapper	Inject only	Yes	25	200 B

Table 12-532. Properties of ECC Aggregator Instance MCAN0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MCANSS_MSGMEM_WRAP_MSGMEM_ECC	0	ECC Wrapper	Inject with error capture	No	32	17 KB
CTRL_EDC_VBUSS	1	EDC Interconnect See Table 12-521	Inject with error capture	Yes		

Table 12-533. EDC Checkers Information of ECC Aggregator Instance MCAN0

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
CTRL_EDC_VBUSS	1	0	32	Parity

Table 12-534. Properties of ECC Aggregator Instance MCAN1

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MCANSS_MSGMEM_WRAP_MSGMEM_ECC	0	ECC Wrapper	Inject with error capture	No	32	17 KB
CTRL_EDC_VBUSS	1	EDC Interconnect See Table 12-523	Inject with error capture	Yes		

Table 12-535. EDC Checkers Information of ECC Aggregator Instance MCAN1

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
CTRL_EDC_VBUSS	1	0	32	Parity

Table 12-536. Properties of ECC Aggregator Instance MCU_ECC_AGGR0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_DST_BUSECC	6	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
ISAM64_MAIN2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL	9	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_RD_RAMECC	11	ECC Wrapper	Inject with error capture	Yes	76	38 B
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_WR_RAMECC	12	ECC Wrapper	Inject with error capture	Yes	76	38 B
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_DEFAULT_ERR_AM64_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	16	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	EDC Interconnect See Table 12-525	Inject with error capture	Yes		

Table 12-536. Properties of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
BLAZAR_VBUSP_M_P2P_DST_BUSECC	26	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
BLAZAR_VBUSP_S_P2P_DST_BUSECC	28	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	EDC Interconnect See Table 12-525	Inject with error capture	Yes		
SAM64_MCU_ECC_AGGR_EDC_CTRL	30	EDC Interconnect See Table 12-525	Inject with error capture	Yes		

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	0	32	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	1	32	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	2	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	3	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	4	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	5	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	6	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	7	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	8	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	9	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	10	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	11	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	12	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	13	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	14	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	15	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	16	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	17	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	18	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	19	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	20	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	21	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	22	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	23	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	24	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	25	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	26	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	27	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	28	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	29	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	30	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	31	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	32	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	33	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	34	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	35	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	36	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	37	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	38	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	39	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	40	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	41	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	42	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	43	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	44	2	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	45	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	46	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	47	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	48	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	49	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	50	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	51	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	52	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	53	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	54	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	55	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	56	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	57	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	58	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	59	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	60	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	61	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	62	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	63	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	64	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	65	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	66	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	67	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	68	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	69	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	70	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	71	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	72	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	73	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	74	4	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	75	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	76	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	77	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	78	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	79	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	80	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	81	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	82	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	83	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	84	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	85	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	86	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	87	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	88	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	89	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	90	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	91	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	92	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	93	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	94	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	95	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	96	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	97	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	98	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	99	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	100	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	101	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	102	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	103	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	104	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	105	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	106	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	107	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	108	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	109	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	110	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	111	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	112	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	113	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	114	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	115	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	116	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	117	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	118	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	119	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	120	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	121	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	122	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	123	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	124	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	125	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	126	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	127	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	128	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	129	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	130	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	131	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	132	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	133	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	134	2	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	135	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	136	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	137	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	138	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	139	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	140	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	141	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	142	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	143	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	144	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	145	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	146	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	147	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	148	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	149	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	150	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	151	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	152	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	153	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	154	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	155	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	156	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	157	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	158	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	159	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	160	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	161	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	162	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	163	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	164	4	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	165	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	166	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	167	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	168	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	169	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	170	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	171	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	172	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	173	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	174	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	175	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	176	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	177	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	178	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	179	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	180	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	181	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	182	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	183	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	184	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	185	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	186	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	187	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	188	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	189	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	190	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	191	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	192	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	193	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	194	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	195	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	196	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	197	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	198	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	199	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	200	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	201	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	202	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	203	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	204	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	205	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	206	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	207	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	208	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	209	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	210	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	211	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	212	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	213	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	214	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	215	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	216	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	217	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	218	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	219	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	220	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	221	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	222	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	223	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	224	2	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	225	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	226	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	227	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	228	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	229	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	230	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	231	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	232	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	233	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	234	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	235	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	236	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	237	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	238	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	239	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	240	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	241	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	242	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	243	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	244	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	245	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	246	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	247	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	248	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	249	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	250	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	251	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	252	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	253	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	254	4	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0	0	255	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	0	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	1	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	2	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	3	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	4	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	5	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	6	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	7	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	8	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	9	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	10	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	11	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	12	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	13	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	14	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	15	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	16	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	17	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	18	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	19	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	20	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	21	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	22	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	23	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	24	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	25	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	26	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	27	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	28	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	29	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	30	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	31	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	32	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	33	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	34	4	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	35	3	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	36	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	37	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	38	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	39	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	40	2	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	41	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	42	1	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	43	32	Parity
IAM64XX_MCU_PADCFG_CTRL_MMR_MCU_0_AM64XX_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1	1	44	32	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	0	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	1	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	2	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	3	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	4	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	5	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	6	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	7	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	8	12	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	9	24	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	10	6	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	11	3	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	12	3	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	13	12	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	14	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	15	3	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	16	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	17	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	18	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	19	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	20	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	21	8	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	22	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	23	5	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	24	4	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	25	7	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	26	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	27	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	28	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	29	7	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	30	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	31	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	32	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	33	7	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	34	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	35	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	36	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	37	7	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	38	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	39	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	40	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	41	7	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	42	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	43	1	Parity
IAM64_MCU_PLL_MMR_MCU_0_AM64_MCU_PLL_MMR_EDC_CTRL_BUSECC	2	44	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	0	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	1	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	2	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	3	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	4	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	5	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	6	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	7	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	8	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	9	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	10	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	11	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	12	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	13	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	14	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	15	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	16	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	17	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	18	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	19	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	20	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	21	8	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	22	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	23	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	24	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	25	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	26	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	27	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	28	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	29	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	30	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	31	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	32	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	33	2	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	34	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	35	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	36	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	37	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	38	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	39	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	40	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	41	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	42	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	43	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	44	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	45	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	46	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	47	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	48	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	49	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	50	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	51	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	52	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	53	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	54	2	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	55	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	56	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	57	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	58	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	59	5	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	60	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	61	2	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	62	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	63	5	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	64	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	65	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	66	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	67	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	68	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	69	14	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	70	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	71	21	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	72	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	73	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	74	30	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	75	32	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	76	8	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	77	2	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	78	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	79	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	80	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	81	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	82	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	83	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	84	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	85	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	86	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	87	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	88	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	89	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	90	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	91	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	92	31	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	93	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	94	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	95	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	96	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	97	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	98	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	99	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	100	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	101	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	102	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	103	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	104	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	105	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	106	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	107	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	108	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	109	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	110	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	111	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	112	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	113	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	114	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	115	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	116	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	117	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	118	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	119	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	120	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	121	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	122	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	123	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	124	12	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	125	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	126	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	127	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	128	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	129	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	130	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	131	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	132	12	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	133	2	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	134	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	135	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	136	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	137	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	138	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	139	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	140	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	141	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	142	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	143	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	144	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	145	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	146	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	147	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	148	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	149	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	150	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	151	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	152	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	153	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	154	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	155	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	156	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	157	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	158	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	159	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	160	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	161	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	162	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	163	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	164	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	165	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	166	8	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	167	8	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	168	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	169	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	170	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	171	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	172	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	173	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	174	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	175	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	176	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	177	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	178	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	179	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	180	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	181	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	182	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	183	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	184	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	185	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	186	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	187	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	188	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	189	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	190	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	191	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	192	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	193	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	194	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	195	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	196	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	197	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	198	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	199	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	200	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	201	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	202	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	203	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	204	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	205	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	206	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	207	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	208	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	209	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	210	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	211	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	212	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	213	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	214	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	215	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	216	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	217	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	218	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	219	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	220	7	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	221	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	222	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	223	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	224	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	225	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	226	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	227	4	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	228	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	229	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	230	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	231	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	232	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	233	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	234	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	235	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	236	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	237	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	238	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	239	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	240	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	241	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	242	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	243	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	244	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	245	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	246	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	247	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	248	6	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	249	3	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	250	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	251	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	252	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	253	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	254	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0	3	255	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	0	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	1	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	2	2	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	3	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	4	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	5	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	6	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	7	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	8	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	9	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	10	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	11	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	12	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	13	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	14	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	15	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	16	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	17	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	18	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	19	2	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	20	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	21	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	22	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	23	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	24	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	25	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	26	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	27	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	28	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	29	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	30	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	31	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	32	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	33	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	34	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	35	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	36	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	37	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	38	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	39	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	40	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	41	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	42	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	43	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	44	1	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	45	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	46	32	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	47	24	Parity
IAM64_MCU_CTRL_MMR_MCU_0_AM64_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1	4	48	1	Parity
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	0	1	Parity
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	1	32	Parity
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	2	1	Redundant
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	3	1	Redundant
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	4	1	Redundant
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	5	1	Redundant
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	6	1	Redundant
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	7	8	Parity
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	8	8	Parity
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	9	8	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	10	8	Parity
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	11	1	Parity
AM64_MCU_CBASS_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_MCU_0_CBASS_ERR_SLV_BRIDGE_BUSECC	5	12	1	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_DST_BUSECC	6	0	1	Redundant
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_DST_BUSECC	6	1	1	Redundant
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_DST_BUSECC	6	2	1	Redundant
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_DST_BUSECC	6	3	10	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_DST_BUSECC	6	4	3	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_DST_BUSECC	6	5	1	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_DST_BUSECC	6	6	1	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	0	1	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	1	32	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	2	1	Redundant
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	3	1	Redundant
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	4	10	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	5	3	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	6	3	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	7	1	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	8	1	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	9	2	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	10	3	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	11	1	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	12	10	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	13	5	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	14	3	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	15	4	Parity
AM64_MCU_CBASS_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_P2P_BRIDGE_ISAM64_MCU_ECC_AGGR_MCU_0_CFG_BRIDGE_SRC_BUSECC	7	16	4	Parity
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	0	1	Parity
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	1	32	Parity
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	2	1	Redundant

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	3	1	Redundant
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	4	1	Redundant
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	5	1	Redundant
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	6	1	Redundant
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	7	8	Parity
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	8	8	Parity
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	9	8	Parity
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	10	8	Parity
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	11	1	Parity
AM64_MCU_CBASS_IBLAZAR_MCU_0_VBUSP_S_P2P_BRIDGE_IBLAZAR_MCU_0_VBUSP_S_BRIDGE_BUSECC	8	12	1	Parity
ISAM64_MAIN2MCU_VBUSM_GASKET_MCU_0_EDC_CTRL	9	0	48	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	0	1	Redundant
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	1	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	2	4	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	3	10	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	4	32	Error Detect and Correct
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	5	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	6	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	7	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	8	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	9	30	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	10	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	11	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	12	10	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	13	12	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	14	4	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	15	3	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	16	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	17	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	18	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	19	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	20	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	21	10	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	22	10	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	23	12	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	24	4	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	25	3	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	26	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	27	10	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	28	3	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	29	3	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	30	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	31	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	32	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	33	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	34	3	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	35	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	36	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	37	1	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	38	30	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	39	6	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	40	6	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	41	6	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	42	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	43	10	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	44	3	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	45	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	46	4	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	47	5	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	48	4	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	49	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	50	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	51	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	52	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	53	22	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	54	22	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	55	10	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	56	3	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	57	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	58	4	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	59	5	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	60	4	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	61	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	62	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	63	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	64	2	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	65	55	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	66	55	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	67	8	Parity
ISAM64_MCU2MAIN_VBUSM_GASKET_MCU_0_EDC_CTRL	10	68	8	Parity
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	0	1	Parity
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	1	32	Parity
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	2	1	Redundant
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	3	1	Redundant
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	4	1	Redundant
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	5	1	Redundant
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	6	1	Redundant

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	7	8	Parity
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	8	8	Parity
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	9	8	Parity
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	10	8	Parity
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	11	1	Parity
AM64_MCU_CBASS_ISLAVE_SAFETY_GASKET_MCU_0_CFG_P2P_BRIDGE_ISLAVE_SAFETY_GASKET_MCU_0_CFG_BRIDGE_BUSECC	13	12	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	0	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	1	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	2	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	3	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	4	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	5	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	6	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	7	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	8	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	9	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	10	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	11	36	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	12	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	13	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	14	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	15	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	16	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	17	25	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	18	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	19	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	20	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	21	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	22	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	23	3	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	24	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	25	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	26	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	27	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	28	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	29	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	30	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	31	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	32	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	33	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	34	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	35	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	36	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	37	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	38	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	39	11	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	40	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	41	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	42	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	43	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	44	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	45	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	46	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	47	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	48	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	49	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	50	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	51	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	52	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	53	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	54	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	55	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	56	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	57	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	58	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	59	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	60	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	61	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	62	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	63	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	64	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	65	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	66	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	67	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	68	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	69	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	70	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	71	9	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	72	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	73	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	74	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	75	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	76	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	77	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	78	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	79	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	80	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	81	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	82	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	83	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	84	9	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	85	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	86	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	87	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	88	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	89	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	90	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	91	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	92	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	93	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	94	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	95	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	96	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	97	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	98	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	99	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	100	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	101	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	102	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	103	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	104	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	105	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	106	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	107	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	108	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	109	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	110	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	111	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	112	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	113	32	Error Detect and Correct

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	114	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	115	17	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	116	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	117	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	118	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	119	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	120	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	121	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	122	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	123	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	124	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	125	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	126	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	127	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	128	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	129	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	130	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	131	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	132	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	133	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	134	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	135	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	136	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	137	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	138	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	139	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	140	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	141	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	142	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	143	32	Error Detect and Correct

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	144	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	145	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	146	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	147	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	148	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	149	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	150	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	151	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	152	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	153	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	154	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	155	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	156	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	157	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	158	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	159	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	160	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	161	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	162	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	163	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	164	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	165	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	166	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	167	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	168	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	169	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	170	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	171	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	172	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	173	3	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	174	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	175	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	176	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	177	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	178	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	179	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	180	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	181	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	182	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	183	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	184	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	185	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	186	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	187	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	188	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	189	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	190	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	191	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	192	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	193	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	194	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	195	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	196	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	197	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	198	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	199	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	200	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	201	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	202	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	203	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	204	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	205	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	206	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	207	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	208	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	209	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	210	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	211	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	212	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	213	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	214	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	215	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	216	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	217	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	218	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	219	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	220	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	221	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	222	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	223	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	224	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	225	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	226	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	227	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	228	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	229	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	230	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	231	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	232	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	233	9	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	234	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	235	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	236	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	237	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	238	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	239	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	240	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	241	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	242	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	243	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	244	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	245	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	246	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	247	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	248	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	249	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	250	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	251	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	252	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	253	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	254	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_0	14	255	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	0	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	1	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	2	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	3	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	4	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	5	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	6	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	7	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	8	9	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	9	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	10	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	11	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	12	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	13	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	14	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	15	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	16	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	17	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	18	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	19	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	20	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	21	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	22	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	23	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	24	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	25	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	26	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	27	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	28	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	29	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	30	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	31	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	32	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	33	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	34	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	35	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	36	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	37	2	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	38	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	39	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	40	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	41	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	42	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	43	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	44	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	45	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	46	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	47	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	48	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	49	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	50	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	51	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	52	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	53	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	54	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	55	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	56	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	57	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	58	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	59	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	60	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	61	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	62	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	63	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	64	36	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	65	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	66	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	67	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	68	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	69	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	70	5	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	71	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	72	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	73	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	74	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	75	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	76	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	77	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	78	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	79	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	80	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	81	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	82	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	83	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	84	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	85	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	86	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	87	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	88	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	89	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	90	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	91	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	92	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	93	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	94	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	95	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	96	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	97	12	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	98	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	99	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	100	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	101	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	102	15	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	103	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	104	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	105	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	106	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	107	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	108	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	109	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	110	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	111	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	112	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	113	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	114	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	115	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	116	1	Redundant
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	117	32	Error Detect and Correct
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	118	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	119	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	120	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	121	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	122	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	123	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	124	10	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	125	5	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	126	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	127	4	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	128	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	129	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	130	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	131	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	132	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	133	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	134	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	135	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	136	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	137	8	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	138	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	139	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	140	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	141	3	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	142	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	143	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	144	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	145	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	146	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	147	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	148	4	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	149	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	150	2	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	151	1	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	152	12	Parity
AM64_MCU_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_1	15	153	1	Redundant
AM64_MCU_CBASS_DEFAULT_ERR_AM64_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	16	0	1	Redundant
AM64_MCU_CBASS_DEFAULT_ERR_AM64_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	16	1	1	Parity
AM64_MCU_CBASS_DEFAULT_ERR_AM64_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	16	2	4	Parity
AM64_MCU_CBASS_DEFAULT_ERR_AM64_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	16	3	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_DEFAULT_ERR_AM64_MCU_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC	16	4	32	Error Detect and Correct
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	0	32	Parity
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	1	32	Parity
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	2	1	Redundant
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	3	1	Parity
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	4	4	Parity
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	5	10	Parity
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	6	4	Parity
AM64_MCU_CBASS_DEFAULT_MMRS_AM64_MCU_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC	17	7	32	Error Detect and Correct
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	0	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	1	13	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	2	1	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	3	4	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	4	3	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	5	1	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	6	4	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	7	4	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	8	2	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	9	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	10	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	11	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	12	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	13	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	14	12	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	15	4	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	16	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	17	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	18	10	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	19	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	20	12	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	21	4	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	22	1	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	23	4	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	24	7	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	25	2	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	26	3	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	27	3	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	28	26	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	29	3	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	30	3	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	31	26	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	32	3	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	33	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	34	1	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	35	1	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	36	32	Error Detect and Correct
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	37	1	Redundant
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	38	1	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	39	10	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	40	10	Parity
AM64_MCU_CBASS_INT_DMSC_SCR_AM64_MCU_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC	18	41	1	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	0	1	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	1	1	Redundant
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	2	1	Redundant
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	3	1	Redundant
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	4	10	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	5	3	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	6	3	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	7	1	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	8	1	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	9	2	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	10	3	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	11	1	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	12	10	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	13	5	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	14	3	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	15	4	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	16	2	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	17	10	Parity
AM64_MCU_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_BUSECC	19	18	3	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	0	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	1	10	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	2	1	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	3	4	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	4	3	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	5	1	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	6	4	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	7	4	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	8	2	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	9	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	10	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	11	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	12	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	13	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	14	12	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	15	4	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	16	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	17	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	18	10	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	19	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	20	12	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	21	4	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	22	1	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	23	4	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	24	7	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	25	2	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	26	3	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	27	3	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	28	26	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	29	3	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	30	3	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	31	26	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	32	3	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	33	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	34	1	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	35	1	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	36	32	Error Detect and Correct
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	37	1	Redundant
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	38	1	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	39	10	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	40	10	Parity
AM64_MCU_CBASS_ERR_SCR_AM64_MCU_CBASS_ERR_SCR_EDC_CTRL_BUSECC	20	41	1	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	0	1	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	1	1	Redundant

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	2	1	Redundant
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	3	1	Redundant
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	4	10	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	5	3	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	6	3	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	7	1	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	8	1	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	9	2	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	10	3	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	11	1	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	12	10	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	13	5	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	14	3	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	15	4	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	16	2	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	17	10	Parity
AM64_MCU_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC	21	18	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	0	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	1	36	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	2	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	3	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	4	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	5	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	6	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	7	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	8	2	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	9	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	10	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	11	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	12	36	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	13	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	14	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	15	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	16	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	17	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	18	4	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	19	2	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	20	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	21	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	22	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	23	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	24	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	25	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	26	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	27	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	28	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	29	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	30	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	31	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	32	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	33	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	34	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	35	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	36	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	37	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	38	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	39	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	40	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	41	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	42	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	43	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	44	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	45	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	46	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	47	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	48	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	49	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	50	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	51	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	52	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	53	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	54	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	55	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	56	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	57	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	58	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	59	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	60	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	61	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	62	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	63	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	64	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	65	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	66	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	67	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	68	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	69	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	70	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	71	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	72	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	73	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	74	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	75	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	76	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	77	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	78	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	79	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	80	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	81	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	82	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	83	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	84	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	85	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	86	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	87	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	88	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	89	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	90	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	91	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	92	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	93	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	94	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	95	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	96	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	97	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	98	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	99	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	100	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	101	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	102	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	103	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	104	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	105	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	106	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	107	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	108	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	109	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	110	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	111	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	112	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	113	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	114	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	115	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	116	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	117	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	118	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	119	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	120	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	121	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	122	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	123	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	124	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	125	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	126	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	127	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	128	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	129	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	130	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	131	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	132	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	133	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	134	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	135	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	136	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	137	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	138	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	139	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	140	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	141	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	142	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	143	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	144	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	145	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	146	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	147	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	148	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	149	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	150	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	151	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	152	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	153	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	154	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	155	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	156	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	157	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	158	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	159	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	160	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	161	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	162	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	163	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	164	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	165	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	166	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	167	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	168	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	169	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	170	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	171	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	172	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	173	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	174	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	175	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	176	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	177	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	178	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	179	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	180	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	181	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	182	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	183	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	184	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	185	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	186	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	187	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	188	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	189	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	190	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	191	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	192	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	193	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	194	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	195	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	196	36	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	197	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	198	3	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	199	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	200	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	201	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	202	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	203	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	204	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	205	25	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	206	30	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	207	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	208	27	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	209	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	210	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	211	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	212	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	213	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	214	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	215	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	216	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	217	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	218	36	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	219	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	220	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	221	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	222	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	223	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	224	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	225	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	226	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	227	25	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	228	30	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	229	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	230	27	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	231	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	232	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	233	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	234	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	235	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	236	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	237	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	238	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	239	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	240	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	241	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	242	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	243	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	244	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	245	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	246	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	247	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	248	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	249	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	250	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	251	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	252	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	253	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	254	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_0	22	255	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	0	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	1	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	2	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	3	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	4	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	5	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	6	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	7	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	8	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	9	11	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	10	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	11	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	12	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	13	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	14	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	15	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	16	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	17	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	18	11	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	19	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	20	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	21	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	22	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	23	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	24	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	25	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	26	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	27	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	28	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	29	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	30	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	31	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	32	1	Redundant

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	33	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	34	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	35	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	36	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	37	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	38	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	39	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	40	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	41	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	42	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	43	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	44	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	45	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	46	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	47	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	48	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	49	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	50	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	51	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	52	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	53	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	54	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	55	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	56	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	57	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	58	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	59	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	60	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	61	9	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	62	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	63	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	64	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	65	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	66	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	67	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	68	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	69	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	70	9	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	71	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	72	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	73	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	74	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	75	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	76	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	77	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	78	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	79	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	80	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	81	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	82	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	83	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	84	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	85	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	86	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	87	9	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	88	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	89	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	90	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	91	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	92	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	93	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	94	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	95	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	96	9	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	97	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	98	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	99	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	100	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	101	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	102	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	103	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	104	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	105	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	106	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	107	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	108	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	109	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	110	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	111	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	112	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	113	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	114	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	115	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	116	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	117	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	118	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	119	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	120	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	121	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	122	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	123	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	124	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	125	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	126	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	127	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	128	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	129	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	130	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	131	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	132	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	133	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	134	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	135	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	136	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	137	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	138	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	139	17	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	140	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	141	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	142	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	143	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	144	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	145	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	146	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	147	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	148	17	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	149	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	150	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	151	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	152	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	153	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	154	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	155	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	156	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	157	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	158	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	159	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	160	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	161	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	162	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	163	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	164	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	165	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	166	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	167	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	168	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	169	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	170	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	171	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	172	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	173	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	174	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	175	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	176	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	177	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	178	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	179	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	180	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	181	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	182	8	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	183	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	184	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	185	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	186	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	187	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	188	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	189	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	190	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	191	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	192	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	193	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	194	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	195	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	196	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	197	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	198	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	199	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	200	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	201	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	202	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	203	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	204	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	205	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	206	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	207	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	208	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	209	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	210	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	211	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	212	26	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	213	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	214	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	215	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	216	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	217	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	218	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	219	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	220	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	221	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	222	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	223	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	224	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	225	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	226	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	227	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	228	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	229	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	230	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	231	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	232	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	233	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	234	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	235	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	236	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	237	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	238	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	239	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	240	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	241	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	242	12	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	243	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	244	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	245	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	246	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	247	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	248	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	249	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	250	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	251	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	252	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	253	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	254	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_1	23	255	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	0	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	1	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	2	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	3	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	4	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	5	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	6	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	7	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	8	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	9	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	10	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	11	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	12	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	13	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	14	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	15	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	16	3	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	17	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	18	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	19	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	20	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	21	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	22	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	23	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	24	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	25	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	26	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	27	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	28	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	29	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	30	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	31	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	32	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	33	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	34	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	35	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	36	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	37	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	38	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	39	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	40	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	41	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	42	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	43	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	44	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	45	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	46	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	47	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	48	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	49	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	50	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	51	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	52	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	53	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	54	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	55	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	56	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	57	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	58	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	59	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	60	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	61	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	62	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	63	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	64	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	65	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	66	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	67	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	68	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	69	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	70	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	71	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	72	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	73	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	74	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	75	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	76	3	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	77	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	78	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	79	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	80	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	81	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	82	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	83	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	84	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	85	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	86	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	87	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	88	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	89	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	90	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	91	9	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	92	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	93	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	94	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	95	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	96	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	97	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	98	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	99	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	100	9	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	101	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	102	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	103	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	104	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	105	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	106	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	107	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	108	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	109	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	110	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	111	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	112	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	113	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	114	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	115	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	116	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	117	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	118	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	119	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	120	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	121	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	122	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	123	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	124	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	125	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	126	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	127	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	128	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	129	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	130	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	131	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	132	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	133	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	134	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	135	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	136	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	137	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	138	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	139	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	140	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	141	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	142	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	143	9	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	144	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	145	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	146	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	147	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	148	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	149	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	150	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	151	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	152	9	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	153	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	154	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	155	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	156	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	157	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	158	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	159	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	160	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	161	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	162	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	163	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	164	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	165	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	166	1	Redundant

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	167	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	168	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	169	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	170	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	171	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	172	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	173	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	174	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	175	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	176	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	177	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	178	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	179	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	180	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	181	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	182	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	183	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	184	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	185	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	186	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	187	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	188	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	189	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	190	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	191	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	192	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	193	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	194	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	195	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	196	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	197	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	198	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	199	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	200	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	201	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	202	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	203	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	204	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	205	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	206	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	207	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	208	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	209	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	210	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	211	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	212	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	213	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	214	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	215	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	216	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	217	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	218	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	219	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	220	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	221	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	222	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	223	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	224	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	225	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	226	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	227	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	228	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	229	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	230	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	231	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	232	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	233	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	234	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	235	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	236	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	237	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	238	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	239	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	240	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	241	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	242	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	243	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	244	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	245	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	246	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	247	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	248	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	249	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	250	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	251	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	252	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	253	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	254	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_2	24	255	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	0	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	1	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	2	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	3	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	4	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	5	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	6	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	7	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	8	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	9	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	10	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	11	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	12	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	13	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	14	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	15	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	16	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	17	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	18	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	19	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	20	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	21	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	22	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	23	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	24	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	25	36	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	26	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	27	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	28	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	29	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	30	1	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	31	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	32	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	33	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	34	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	35	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	36	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	37	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	38	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	39	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	40	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	41	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	42	15	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	43	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	44	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	45	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	46	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	47	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	48	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	49	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	50	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	51	15	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	52	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	53	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	54	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	55	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	56	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	57	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	58	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	59	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	60	3	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	61	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	62	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	63	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	64	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	65	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	66	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	67	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	68	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	69	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	70	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	71	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	72	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	73	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	74	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	75	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	76	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	77	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	78	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	79	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	80	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	81	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	82	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	83	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	84	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	85	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	86	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	87	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	88	19	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	89	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	90	3	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	91	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	92	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	93	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	94	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	95	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	96	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	97	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	98	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	99	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	100	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	101	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	102	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	103	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	104	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	105	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	106	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	107	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	108	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	109	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	110	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	111	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	112	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	113	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	114	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	115	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	116	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	117	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	118	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	119	12	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	120	32	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	121	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	122	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	123	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	124	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	125	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	126	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	127	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	128	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	129	32	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	130	4	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	131	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	132	5	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	133	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	134	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	135	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	136	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	137	8	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	138	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	139	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	140	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	141	26	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	142	3	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	143	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	144	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	145	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	146	32	Error Detect and Correct
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	147	1	Redundant
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	148	1	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	149	10	Parity
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	150	10	Parity

Table 12-537. EDC Checkers Information of ECC Aggregator Instance MCU_ECC_AGGR0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_AM64_MCU_CBASS_SCRP_MCU_CLK4_SCR_EDC_CTRL_BUSECC_3	25	151	1	Parity
BLAZAR_VBUSP_M_P2P_DST_BUSECC	26	0	1	Redundant
BLAZAR_VBUSP_M_P2P_DST_BUSECC	26	1	1	Redundant
BLAZAR_VBUSP_M_P2P_DST_BUSECC	26	2	36	Parity
BLAZAR_VBUSP_M_P2P_DST_BUSECC	26	3	3	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	0	1	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	1	1	Redundant
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	2	36	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	3	3	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	4	3	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	5	1	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	6	1	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	7	2	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	8	3	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	9	1	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	10	10	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	11	5	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	12	3	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	13	4	Parity
BLAZAR_VBUSP_M_P2P_SRC_BUSECC	27	14	2	Parity
BLAZAR_VBUSP_S_P2P_DST_BUSECC	28	0	1	Redundant
BLAZAR_VBUSP_S_P2P_DST_BUSECC	28	1	1	Redundant
BLAZAR_VBUSP_S_P2P_DST_BUSECC	28	2	1	Redundant
BLAZAR_VBUSP_S_P2P_DST_BUSECC	28	3	32	Parity
BLAZAR_VBUSP_S_P2P_DST_BUSECC	28	4	3	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	0	1	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	1	32	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	2	1	Redundant
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	3	1	Redundant
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	4	32	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	5	3	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	6	3	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	7	1	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	8	1	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	9	2	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	10	3	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	11	1	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	12	10	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	13	5	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	14	3	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	15	4	Parity
BLAZAR_VBUSP_S_P2P_SRC_BUSECC	29	16	2	Parity
SAM64_MCU_ECC_AGGR_EDC_CTRL	30	0	1	Redundant
SAM64_MCU_ECC_AGGR_EDC_CTRL	30	1	32	Error Detect and Correct
SAM64_MCU_ECC_AGGR_EDC_CTRL	30	2	1	Parity
SAM64_MCU_ECC_AGGR_EDC_CTRL	30	3	10	Parity
SAM64_MCU_ECC_AGGR_EDC_CTRL	30	4	4	Parity
SAM64_MCU_ECC_AGGR_EDC_CTRL	30	5	3	Parity

Table 12-538. Properties of ECC Aggregator Instance MCU_M4FSS0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
BLAZAR_IIRAM_ECC	0	ECC Wrapper	Inject with error capture	No	32	192 KB
BLAZAR_IDRAM_ECC	1	ECC Wrapper	Inject with error capture	No	32	64 KB
BLAZAR_IIRAM_EDC_CTRL_0	2	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_IDRAM_EDC_CTRL_0	3	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_RAT_EDC_CTRL_0	4	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_IA2V_I_EDC_CTRL_0	10	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_IA2V_D_EDC_CTRL_0	11	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	EDC Interconnect See Table 12-527	Inject with error capture	Yes		
BLAZAR_ECC_EDC_CTRL	13	EDC Interconnect See Table 12-527	Inject with error capture	Yes		

Table 12-539. EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
BLAZAR_IIRAM_EDC_CTRL_0	2	0	1	Redundant
BLAZAR_IIRAM_EDC_CTRL_0	2	1	32	Error Detect and Correct
BLAZAR_IIRAM_EDC_CTRL_0	2	2	1	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	3	18	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	4	4	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	5	3	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	6	1	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	7	1	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	8	10	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	9	12	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	10	4	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	11	12	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	12	2	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	13	3	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	14	1	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	15	1	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	16	1	Redundant
BLAZAR_IIRAM_EDC_CTRL_0	2	17	64	Parity
BLAZAR_IIRAM_EDC_CTRL_0	2	18	28	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	0	1	Redundant
BLAZAR_IDRAM_EDC_CTRL_0	3	1	32	Error Detect and Correct
BLAZAR_IDRAM_EDC_CTRL_0	3	2	1	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	3	16	Parity

Table 12-539. EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
BLAZAR_IDRAM_EDC_CTRL_0	3	4	4	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	5	3	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	6	1	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	7	1	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	8	10	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	9	12	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	10	4	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	11	12	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	12	2	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	13	3	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	14	1	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	15	1	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	16	1	Redundant
BLAZAR_IDRAM_EDC_CTRL_0	3	17	64	Parity
BLAZAR_IDRAM_EDC_CTRL_0	3	18	28	Parity
BLAZAR_RAT_EDC_CTRL_0	4	0	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	1	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	2	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	3	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	4	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	5	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	6	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	7	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	8	6	Parity
BLAZAR_RAT_EDC_CTRL_0	4	9	6	Parity
BLAZAR_RAT_EDC_CTRL_0	4	10	6	Parity
BLAZAR_RAT_EDC_CTRL_0	4	11	6	Parity
BLAZAR_RAT_EDC_CTRL_0	4	12	6	Parity
BLAZAR_RAT_EDC_CTRL_0	4	13	6	Parity
BLAZAR_RAT_EDC_CTRL_0	4	14	6	Parity
BLAZAR_RAT_EDC_CTRL_0	4	15	6	Parity
BLAZAR_RAT_EDC_CTRL_0	4	16	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	17	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	18	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	19	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	20	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	21	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	22	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	23	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	24	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	25	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	26	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	27	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	28	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	29	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	30	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	31	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	32	4	Parity
BLAZAR_RAT_EDC_CTRL_0	4	33	4	Parity

Table 12-539. EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
BLAZAR_RAT_EDC_CTRL_0	4	34	4	Parity
BLAZAR_RAT_EDC_CTRL_0	4	35	4	Parity
BLAZAR_RAT_EDC_CTRL_0	4	36	4	Parity
BLAZAR_RAT_EDC_CTRL_0	4	37	4	Parity
BLAZAR_RAT_EDC_CTRL_0	4	38	4	Parity
BLAZAR_RAT_EDC_CTRL_0	4	39	4	Parity
BLAZAR_RAT_EDC_CTRL_0	4	40	32	Parity
BLAZAR_RAT_EDC_CTRL_0	4	41	1	Parity
BLAZAR_RAT_EDC_CTRL_0	4	42	1	Parity
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	0	1	Parity
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	1	32	Parity
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	2	1	Redundant
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	3	1	Redundant
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	4	1	Redundant
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	5	1	Redundant
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	6	1	Redundant
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	7	8	Parity
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	8	8	Parity
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	9	8	Parity
BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC	5	10	8	Parity
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	0	1	Parity
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	1	32	Parity
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	2	1	Redundant
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	3	1	Redundant
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	4	1	Redundant
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	5	1	Redundant
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	6	1	Redundant
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	7	8	Parity
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	8	8	Parity
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	9	8	Parity
BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC	6	10	8	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	0	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	1	22	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	2	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	3	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	4	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	5	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	6	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	7	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	8	2	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	9	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	10	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	11	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	12	22	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	13	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	14	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	15	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	16	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	17	4	Parity

Table 12-539. EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	18	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	19	2	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	20	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	21	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	22	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	23	22	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	24	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	25	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	26	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	27	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	28	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	29	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	30	2	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	31	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	32	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	33	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	34	22	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	35	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	36	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	37	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	38	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	39	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	40	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	41	2	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	42	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	43	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	44	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	45	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	46	10	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	47	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	48	12	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	49	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	50	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	51	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	52	10	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	53	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	54	12	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	55	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	56	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	57	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	58	10	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	59	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	60	12	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	61	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	62	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	63	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	64	10	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	65	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	66	12	Parity

Table 12-539. EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	67	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	68	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	69	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	70	10	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	71	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	72	12	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	73	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	74	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	75	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	76	7	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	77	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	78	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	79	7	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	80	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	81	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	82	7	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	83	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	84	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	85	9	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	86	5	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	87	6	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	88	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	89	26	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	90	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	91	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	92	26	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	93	4	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	94	35	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	95	26	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	96	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	97	35	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	98	26	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	99	3	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	100	5	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	101	26	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	102	5	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	103	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	104	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	105	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	106	32	Error Detect and Correct
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	107	1	Redundant
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	108	1	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	109	10	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	110	10	Parity
BLAZAR_CBASS_BLAZAR_SCR_BLAZAR_CBASS_BLAZAR_SCR_EDC_CTRL_BUSECC	7	111	1	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	0	32	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	1	32	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	2	32	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	3	32	Parity

Table 12-539. EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	4	48	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	5	1	Redundant
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	6	32	Error Detect and Correct
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	7	1	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	8	32	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	9	4	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	10	3	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	11	1	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	12	1	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	13	10	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	14	12	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	15	4	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	16	12	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	17	2	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	18	3	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	19	1	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	20	1	Parity
BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC	8	21	1	Redundant
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	0	1	Redundant
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	1	32	Error Detect and Correct
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	2	1	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	3	32	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	4	4	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	5	3	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	6	1	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	7	1	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	8	10	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	9	5	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	10	2	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	11	3	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	12	1	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	13	2	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	14	2	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	15	1	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	16	2	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	17	2	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	18	2	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	19	2	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	20	1	Redundant
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	21	32	Error Detect and Correct
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	22	1	Redundant
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	23	3	Parity
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	24	1	Redundant
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	25	32	Error Detect and Correct
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	26	1	Redundant
BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_0	9	27	3	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	0	1	Redundant
BLAZAR_IA2V_I_EDC_CTRL_0	10	1	1	Redundant
BLAZAR_IA2V_I_EDC_CTRL_0	10	2	3	Parity

Table 12-539. EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
BLAZAR_IA2V_I_EDC_CTRL_0	10	3	32	Error Detect and Correct
BLAZAR_IA2V_I_EDC_CTRL_0	10	4	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	5	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	6	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	7	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	8	38	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	9	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	10	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	11	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	12	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	13	64	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	14	1	Parity
BLAZAR_IA2V_I_EDC_CTRL_0	10	15	5	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	0	1	Redundant
BLAZAR_IA2V_D_EDC_CTRL_0	11	1	1	Redundant
BLAZAR_IA2V_D_EDC_CTRL_0	11	2	3	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	3	32	Error Detect and Correct
BLAZAR_IA2V_D_EDC_CTRL_0	11	4	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	5	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	6	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	7	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	8	38	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	9	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	10	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	11	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	12	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	13	64	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	14	1	Parity
BLAZAR_IA2V_D_EDC_CTRL_0	11	15	5	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	0	1	Redundant
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	1	1	Redundant
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	2	3	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	3	32	Error Detect and Correct
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	4	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	5	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	6	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	7	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	8	38	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	9	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	10	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	11	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	12	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	13	64	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	14	1	Parity
BLAZAR_SYS_GASKET_EDC_CTRL_0	12	15	5	Parity
BLAZAR_ECC_EDC_CTRL	13	0	1	Redundant
BLAZAR_ECC_EDC_CTRL	13	1	32	Error Detect and Correct
BLAZAR_ECC_EDC_CTRL	13	2	1	Parity
BLAZAR_ECC_EDC_CTRL	13	3	10	Parity

Table 12-539. EDC Checkers Information of ECC Aggregator Instance MCU_M4FSS0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
BLAZAR_ECC_EDC_CTRL	13	4	4	Parity
BLAZAR_ECC_EDC_CTRL	13	5	3	Parity

Table 12-540. Properties of ECC Aggregator Instance MMCSD0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EMMC8SS_16FFC_SDHC_WRAP_TXMEM	0	ECC Wrapper	Inject with error capture	Yes	64	4 KB
EMMC8SS_16FFC_SDHC_WRAP_RXMEM	0	ECC Wrapper	Inject with error capture	Yes	64	4 KB

Table 12-541. Properties of ECC Aggregator Instance MMCSD1

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
EMMCSD4SS_SDHC_WRAP_RXMEM	0	ECC Wrapper	Inject with error capture	Yes	64	4 KB
EMMCSD4SS_SDHC_WRAP_TXMEM	0	ECC Wrapper	Inject with error capture	Yes	64	4 KB

Table 12-542. Properties of ECC Aggregator Instance MSRAM_256K0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	No	64	256 KB

Table 12-543. Properties of ECC Aggregator Instance MSRAM_256K1

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	No	64	256 KB

Table 12-544. Properties of ECC Aggregator Instance MSRAM_256K2

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	No	64	256 KB

Table 12-545. Properties of ECC Aggregator Instance MSRAM_256K3

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	No	64	256 KB

Table 12-546. Properties of ECC Aggregator Instance MSRAM_256K4

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	No	64	256 KB

Table 12-547. Properties of ECC Aggregator Instance MSRAM_256K5

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	No	64	256 KB

Table 12-548. Properties of ECC Aggregator Instance MSRAM_256K6

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	No	64	256 KB

Table 12-549. Properties of ECC Aggregator Instance MSRAM_256K7

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
MSRAM32KX64E_MSRAM0_ECC0	0	ECC Wrapper	Inject with error capture	No	64	256 KB

Table 12-550. Properties of ECC Aggregator Instance PCIE0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PCIE_G2X1_64_CORE_DBN_WRAP_RAMS_AXIMFIFO	0	ECC Wrapper	Inject only	Yes	81	324 B
PCIE_G2X1_64_CORE_DBN_WRAP_RAMS_AXISFIFO	1	ECC Wrapper	Inject only	Yes	97	388 B
PCIE_G2X1_64_CORE_DBN_WRAP_RAMS_DIBRAM	2	ECC Wrapper	Inject only	Yes	81	1 KB
PCIE_G2X1_64_CORE_AXI2VBUSM_MST_KSBUS_AXI2VBUSM_RDATA_BUFFER	3	ECC Wrapper	Inject with error capture	Yes	66	8 KB
PCIE_G2X1_64_CORE_DBN_WRAP_RAMS_PNPFIFO	0	ECC Wrapper	Inject only	Yes	45	13 KB
PCIE_G2X1_64_CORE_DBN_WRAP_RAMS_RXCPLFIFO	1	ECC Wrapper	Inject only	Yes	45	2 KB
PCIE_G2X1_64_CORE_DBN_WRAP_RAMS_RPLYBUF	2	ECC Wrapper	Inject only	Yes	45	2 KB
PCIE_G2X1_64_CORE_DBN_WRAP_RAMS_AXISRODR	3	ECC Wrapper	Inject only	Yes	44	1 KB

Table 12-551. Properties of ECC Aggregator Instance PDMA0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PDMA_AM64_MAIN0_PDMA_CORE_TF0_F0_TPRAM_72X128_SBW_SR	0	ECC Wrapper	Inject with error capture	Yes	128	1 KB
PDMA_AM64_MAIN0_PDMA_CORE_TF0_F1_TPRAM_72X128_SBW_SR	1	ECC Wrapper	Inject with error capture	Yes	128	1 KB
PDMA_AM64_MAIN0_PDMA_CORE_RF0_F0_TPRAM_72X144_SBW_SR	2	ECC Wrapper	Inject with error capture	Yes	144	1 KB
PDMA_AM64_MAIN0_PDMA_CORE_RF0_F1_TPRAM_72X144_SBW_SR	3	ECC Wrapper	Inject with error capture	Yes	144	1 KB

Table 12-552. Properties of ECC Aggregator Instance PDMA1

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PDMA_AM64_MAIN1_PDMA_CORE_TF0_F0_TPRAM_60X128_SBW_SR	0	ECC Wrapper	Inject with error capture	Yes	128	960 B
PDMA_AM64_MAIN1_PDMA_CORE_TF0_F1_TPRAM_60X128_SBW_SR	1	ECC Wrapper	Inject with error capture	Yes	128	960 B
PDMA_AM64_MAIN1_PDMA_CORE_RF0_F0_TPRAM_68X144_SBW_SR	2	ECC Wrapper	Inject with error capture	Yes	144	1 KB
PDMA_AM64_MAIN1_PDMA_CORE_RF0_F1_TPRAM_68X144_SBW_SR	3	ECC Wrapper	Inject with error capture	Yes	144	1 KB

Table 12-553. Properties of ECC Aggregator Instance PRU_ICSSG0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ICSS_G_CORE_DRAM0_ECC	0	ECC Wrapper	Inject with error capture	Yes	32	8 KB
ICSS_G_CORE_DRAM1_ECC	1	ECC Wrapper	Inject with error capture	Yes	32	8 KB
ICSS_G_CORE_PR1_PDSP0_IRAM_ECC	2	ECC Wrapper	Inject with error capture	Yes	32	12 KB
ICSS_G_CORE_PR1_PDSP1_IRAM_ECC	3	ECC Wrapper	Inject with error capture	Yes	32	12 KB
ICSS_G_CORE_RAM_ECC	4	ECC Wrapper	Inject with error capture	Yes	32	64 KB
ICSS_G_CORE_PR1_RTU0_PDSP_IRAM_ECC	5	ECC Wrapper	Inject with error capture	Yes	32	8 KB
ICSS_G_CORE_PR1_RTU1_PDSP_IRAM_ECC	6	ECC Wrapper	Inject with error capture	Yes	32	8 KB
ICSS_G_CORE_PR1_PDSP_TX0_IRAM_ECC	7	ECC Wrapper	Inject with error capture	Yes	32	6 KB

Table 12-553. Properties of ECC Aggregator Instance PRU_ICSSG0 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ICSS_G_CORE_PR1_PDSP_TX1_IRAM_ECC	8	ECC Wrapper	Inject with error capture	Yes	32	6 KB

Table 12-554. Properties of ECC Aggregator Instance PRU_ICSSG1

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
ICSS_G_CORE_DRAM0_ECC	0	ECC Wrapper	Inject with error capture	Yes	32	8 KB
ICSS_G_CORE_DRAM1_ECC	1	ECC Wrapper	Inject with error capture	Yes	32	8 KB
ICSS_G_CORE_PR1_PDSP0_IRAM_ECC	2	ECC Wrapper	Inject with error capture	Yes	32	12 KB
ICSS_G_CORE_PR1_PDSP1_IRAM_ECC	3	ECC Wrapper	Inject with error capture	Yes	32	12 KB
ICSS_G_CORE_RAM_ECC	4	ECC Wrapper	Inject with error capture	Yes	32	64 KB
ICSS_G_CORE_PR1_RTU0_PDSP_IRAM_ECC	5	ECC Wrapper	Inject with error capture	Yes	32	8 KB
ICSS_G_CORE_PR1_RTU1_PDSP_IRAM_ECC	6	ECC Wrapper	Inject with error capture	Yes	32	8 KB
ICSS_G_CORE_PR1_PDSP_TX0_IRAM_ECC	7	ECC Wrapper	Inject with error capture	Yes	32	6 KB
ICSS_G_CORE_PR1_PDSP_TX1_IRAM_ECC	8	ECC Wrapper	Inject with error capture	Yes	32	6 KB

Table 12-555. Properties of ECC Aggregator Instance PSRAMECC0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PSRAM256X32E_PSRAM0_ECC	0	ECC Wrapper	Inject with error capture	No	32	1 KB

Table 12-556. Properties of ECC Aggregator Instance R5FSS0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_ITAG_RAM0	0	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_ITAG_RAM1	1	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_ITAG_RAM2	2	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_ITAG_RAM3	3	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_IDATA_BANK0	4	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK1	5	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK2	6	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK3	7	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_DTAG_RAM0	8	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DTAG_RAM1	9	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DTAG_RAM2	10	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DTAG_RAM3	11	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DDIRTY_RAM	12	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DDATA_RAM0	13	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM1	14	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM2	15	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM3	16	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM4	17	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM5	18	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM6	19	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM7	20	ECC Wrapper	Inject only	Yes	39	5 KB
PULSAR_LITE_ATCM0_BANK0	21	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_LITE_ATCM0_BANK1	22	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_LITE_B0TCM0_BANK0	23	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B0TCM0_BANK1	24	ECC Wrapper	Inject only	Yes	39	10 KB

Table 12-556. Properties of ECC Aggregator Instance R5FSS0 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
PULSAR_LITE_B1TCM0_BANK0	25	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B1TCM0_BANK1	26	ECC Wrapper	Inject only	Yes	39	10 KB
CPU0_KS_VIM_RAMECC	27	ECC Wrapper	Inject with error capture	Yes	30	960 B
CPU0_AXI2VBUSM_MEM_MST_RAMECC	28	ECC Wrapper	Inject with error capture	Yes	66	528 B
CPU1_ITAG_RAM0	0	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_ITAG_RAM1	1	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_ITAG_RAM2	2	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_ITAG_RAM3	3	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_IDATA_BANK0	4	ECC Wrapper	Inject only	Yes	72	9 KB
CPU1_IDATA_BANK1	5	ECC Wrapper	Inject only	Yes	72	9 KB
CPU1_IDATA_BANK2	6	ECC Wrapper	Inject only	Yes	72	9 KB
CPU1_IDATA_BANK3	7	ECC Wrapper	Inject only	Yes	72	9 KB
CPU1_DTAG_RAM0	8	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DTAG_RAM1	9	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DTAG_RAM2	10	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DTAG_RAM3	11	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DDIRTY_RAM	12	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DDATA_RAM0	13	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM1	14	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM2	15	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM3	16	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM4	17	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM5	18	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM6	19	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM7	20	ECC Wrapper	Inject only	Yes	39	5 KB
PULSAR_LITE_ATCM1_BANK0	21	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_LITE_ATCM1_BANK1	22	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_LITE_B0TCM1_BANK0	23	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B0TCM1_BANK1	24	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B1TCM1_BANK0	25	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B1TCM1_BANK1	26	ECC Wrapper	Inject only	Yes	39	10 KB
CPU1_KS_VIM_RAMECC	27	ECC Wrapper	Inject with error capture	Yes	30	960 B
CPU1_AXI2VBUSM_MEM_MST_RAMECC	28	ECC Wrapper	Inject with error capture	Yes	66	528 B

Table 12-557. Properties of ECC Aggregator Instance R5FSS1

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_ITAG_RAM0	0	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_ITAG_RAM1	1	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_ITAG_RAM2	2	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_ITAG_RAM3	3	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_IDATA_BANK0	4	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK1	5	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK2	6	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_IDATA_BANK3	7	ECC Wrapper	Inject only	Yes	72	9 KB
CPU0_DTAG_RAM0	8	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DTAG_RAM1	9	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DTAG_RAM2	10	ECC Wrapper	Inject only	Yes	28	896 B

Table 12-557. Properties of ECC Aggregator Instance R5FSS1 (continued)

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
CPU0_DTAG_RAM3	11	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DDIRTY_RAM	12	ECC Wrapper	Inject only	Yes	28	896 B
CPU0_DDATA_RAM0	13	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM1	14	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM2	15	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM3	16	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM4	17	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM5	18	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM6	19	ECC Wrapper	Inject only	Yes	39	5 KB
CPU0_DDATA_RAM7	20	ECC Wrapper	Inject only	Yes	39	5 KB
PULSAR_LITE_ATCM0_BANK0	21	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_LITE_ATCM0_BANK1	22	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_LITE_B0TCM0_BANK0	23	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B0TCM0_BANK1	24	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B1TCM0_BANK0	25	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B1TCM0_BANK1	26	ECC Wrapper	Inject only	Yes	39	10 KB
CPU0_KS_VIM_RAMECC	27	ECC Wrapper	Inject with error capture	Yes	30	960 B
CPU0_AXI2VBUSM_MEM_MST_RAMECC	28	ECC Wrapper	Inject with error capture	Yes	66	528 B
CPU1_ITAG_RAM0	0	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_ITAG_RAM1	1	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_ITAG_RAM2	2	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_ITAG_RAM3	3	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_IDATA_BANK0	4	ECC Wrapper	Inject only	Yes	72	9 KB
CPU1_IDATA_BANK1	5	ECC Wrapper	Inject only	Yes	72	9 KB
CPU1_IDATA_BANK2	6	ECC Wrapper	Inject only	Yes	72	9 KB
CPU1_IDATA_BANK3	7	ECC Wrapper	Inject only	Yes	72	9 KB
CPU1_DTAG_RAM0	8	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DTAG_RAM1	9	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DTAG_RAM2	10	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DTAG_RAM3	11	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DDIRTY_RAM	12	ECC Wrapper	Inject only	Yes	28	896 B
CPU1_DDATA_RAM0	13	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM1	14	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM2	15	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM3	16	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM4	17	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM5	18	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM6	19	ECC Wrapper	Inject only	Yes	39	5 KB
CPU1_DDATA_RAM7	20	ECC Wrapper	Inject only	Yes	39	5 KB
PULSAR_LITE_ATCM1_BANK0	21	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_LITE_ATCM1_BANK1	22	ECC Wrapper	Inject only	Yes	39	20 KB
PULSAR_LITE_B0TCM1_BANK0	23	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B0TCM1_BANK1	24	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B1TCM1_BANK0	25	ECC Wrapper	Inject only	Yes	39	10 KB
PULSAR_LITE_B1TCM1_BANK1	26	ECC Wrapper	Inject only	Yes	39	10 KB
CPU1_KS_VIM_RAMECC	27	ECC Wrapper	Inject with error capture	Yes	30	960 B
CPU1_AXI2VBUSM_MEM_MST_RAMECC	28	ECC Wrapper	Inject with error capture	Yes	66	528 B

Table 12-558. Properties of ECC Aggregator Instance SA2_UL0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
SA2_UL_PKTRAM0_ECC	0	ECC Wrapper	Inject with error capture	Yes	64	512 B
SA2_UL_PKTRAM1_ECC	1	ECC Wrapper	Inject with error capture	Yes	64	512 B
SA2_UL_PKA_PROG_RAM_ECC	2	ECC Wrapper	Inject with error capture	Yes	24	15 KB
SA2_UL_ENCR_CTXRAM_BANK01_ECC	3	ECC Wrapper	Inject with error capture	Yes	256	256 B
SA2_UL_ENCR_CTXRAM_BANK23_ECC	4	ECC Wrapper	Inject with error capture	Yes	256	256 B
SA2_UL_ENCR_CTXRAM_BANK4_ECC	5	ECC Wrapper	Inject with error capture	Yes	256	128 B
SA2_UL_AUTH_CTXRAM_BANK01_ECC	6	ECC Wrapper	Inject with error capture	Yes	256	256 B
SA2_UL_AUTH_CTXRAM_BANK23_ECC	7	ECC Wrapper	Inject with error capture	Yes	256	256 B
SA2_UL_AUTH_CTXRAM_BANK45_ECC	8	ECC Wrapper	Inject with error capture	Yes	256	256 B
SA2_UL_AUTH_CTXRAM_BANK67_ECC	9	ECC Wrapper	Inject with error capture	Yes	256	256 B
SA2_UL_AUTH_CTXRAM_BANK89_ECC	10	ECC Wrapper	Inject with error capture	Yes	256	256 B
SA2_UL_AUTH_CTXRAM_BANK10_ECC	11	ECC Wrapper	Inject with error capture	Yes	256	128 B

Table 12-559. Properties of ECC Aggregator Instance USB0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
USB3P0SS64_16FFC_USB3P0SS64_CORE_USB3P0_KSBUS_AXI2VBUSM_KSBUS_AXI2VBUSM_RDATA_BUFFER	0	ECC Wrapper	Inject with error capture	Yes	66	2 KB

Table 12-560. Properties of ECC Aggregator Instance VTM0

ECC Endpoint	RAM ID	ECC Type	Inject Type	Accessible Mem	Row Width	RAM Size
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	EDC Interconnect See Table 12-549	Inject with error capture	Yes		
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	EDC Interconnect See Table 12-549	Inject with error capture	Yes		
K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_EDC_CTRL_0	2	EDC Interconnect See Table 12-549	Inject with error capture	Yes		
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	EDC Interconnect See Table 12-549	Inject with error capture	Yes		

Table 12-561. EDC Checkers Information of ECC Aggregator Instance VTM0

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	0	1	Redundant
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	1	32	Error Detect and Correct
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	2	1	Parity
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	3	10	Parity
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	4	4	Parity
K3VTM_N16FFC_ECCAGGR_EDC_CTRL	0	5	3	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	0	1	Redundant
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	1	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	2	4	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	3	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	4	4	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	5	32	Error Detect and Correct
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	6	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	7	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	8	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	9	1	Parity

Table 12-561. EDC Checkers Information of ECC Aggregator Instance VTM0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	10	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	11	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	12	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	13	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	14	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	15	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	16	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	17	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	18	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	19	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	20	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	21	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	22	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	23	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	24	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	25	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	26	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	27	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	28	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	29	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	30	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	31	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	32	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	33	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	34	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	35	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	36	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	37	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	38	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	39	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	40	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	41	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	42	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	43	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	44	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	45	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	46	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	47	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	48	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	49	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	50	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	51	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	52	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	53	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	54	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	55	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	56	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	57	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	58	1	Parity

Table 12-561. EDC Checkers Information of ECC Aggregator Instance VTM0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	59	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	60	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	61	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	62	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	63	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	64	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	65	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	66	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	67	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	68	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	69	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	70	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	71	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	72	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	73	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	74	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	75	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	76	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	77	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	78	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	79	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	80	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	81	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	82	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	83	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	84	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	85	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	86	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	87	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	88	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	89	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	90	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	91	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	92	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	93	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	94	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	95	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	96	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	97	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	98	10	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	99	16	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	100	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	101	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	102	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	103	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	104	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	105	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	106	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	107	1	Parity

Table 12-561. EDC Checkers Information of ECC Aggregator Instance VTM0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	108	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	109	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	110	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	111	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	112	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	113	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	114	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	115	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	116	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	117	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	118	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	119	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	120	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	121	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	122	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	123	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	124	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	125	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	126	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	127	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	128	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	129	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	130	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	131	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	132	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	133	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	134	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	135	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	136	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	137	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	138	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	139	5	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	140	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	141	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	142	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	143	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	144	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	145	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	146	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	147	6	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	148	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	149	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	150	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	151	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	152	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	153	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	154	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	155	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	156	8	Parity

Table 12-561. EDC Checkers Information of ECC Aggregator Instance VTM0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	157	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	158	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	159	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	160	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	161	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	162	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	163	1	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	164	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	165	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	166	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	167	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	168	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	169	8	Parity
K3VTM_N16FFC_MMR_EDC_CTRL_0	1	170	8	Parity
K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_EDC_CTRL_0	2	0	1	Redundant
K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_EDC_CTRL_0	2	1	1	Redundant
K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_EDC_CTRL_0	2	2	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	0	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	1	10	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	2	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	3	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	4	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	5	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	6	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	7	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	8	2	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	9	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	10	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	11	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	12	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	13	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	14	12	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	15	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	16	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	17	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	18	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	19	12	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	20	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	21	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	22	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	23	10	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	24	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	25	12	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	26	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	27	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	28	4	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	29	7	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	30	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	31	4	Parity

Table 12-561. EDC Checkers Information of ECC Aggregator Instance VTM0 (continued)

Protected Interconnect	RAM ID	Group ID	Width	Checker Type
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	32	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	33	26	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	34	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	35	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	36	26	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	37	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	38	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	39	26	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	40	3	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	41	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	42	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	43	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	44	32	Error Detect and Correct
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	45	1	Redundant
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	46	1	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	47	10	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	48	10	Parity
K3VTM_N16FFC_CFG_CBASS_CFG_SCR_EDC_CTRL_0	3	49	1	Parity

Chapter 13

On-Chip Debug

This chapter describes the on-chip debug support including details on the various capabilities and features available through the SoC debug framework.

13.1 On-Chip Debug Overview

This chapter describes the properties and capabilities of the various features available through the On-Chip Debug framework deployed on this device.

The On-Chip Debug framework enables various Debug and Trace use-cases, including:

- **JTAG Tooling** – Access to on-chip debug resources is supported by an IEEE 1149.1 (JTAG) compliant interface that is supported by an Arm® CoreSight™ DAP JTAG-DP.
- **Self-Hosted Tooling** – code running on programmable cores within the device is able to use on-chip debug resources to enable embedded tooling solutions.
- **PCB-level interconnect testing** – IEEE 1149.1 and IEEE 1149.6 compliant Boundary Scan supports product level integration testing
- **Low Power Operation** – When on-chip JTAG and debug management logic is in a low power state, activity sensed on the JTAG interface will cause this logic to be placed in a functional state.
- **Stop Mode debugging** – Debug of embedded processors is supported using various mechanisms that can halt the pipeline of a CPU. Breakpoints (Software and Hardware), Watchpoints, Cross-Triggering, and On-demand (e.g. user requested) halt request mechanisms may be supported based on the capabilities of a given processor.
- **Debug-aware Peripherals** – Peripheral awareness of processor execution state allows safe suspension of peripheral operation. Supported by select peripherals.
- **Synchronized Debug** – Wide deployment of Cross-Triggering allows multiple processors and/or debug elements to be grouped together to process various actions based on a common event occurrence.
- **Processor Trace** – Support for the generation of a trace stream with the encoding of processor state that may include some combination of program flow, timing details (execution and stall), and memory references (address and/or data) with the goal of facilitating processor state reconstruction for debug purposes.
- **Software Messaging Trace** – Support for software messaging trace where embedded code running within the device can be instrumented to use memory writes to send important debug information to a trace stream.
- **System Traffic Trace** – Strategically selected points in the SoC topology are instrumented with trace-capable bus probes that support transaction trace, read-latency monitoring, and throughput computation.
- **Trace Correlation (through timestamping)** – Support for the correlation of different trace streams is enabled through the use of a common global timestamp that is distributed to supported trace sources.
- **Trace data movement** – Trace data movement on chip is supported using standard Arm ATB trace infrastructure components. Concurrent use of the trace bus by multiple trace sources is supported, with each trace source identifiable through a unique ID. An Arm® CoreSight™ Trace Router supports sending a trace stream off-chip (TPIU), to dedicated memory on-chip (TBR), or broadcasted to both (TPIU + TBR).
- **On-Chip trace collection via dedicated buffer** – An on-chip trace buffer is supported by logic that implements capturing trace data until either the memory fills (stop-on-full, system-bridge) or continuously until a request to stop is received (circular buffer). Interleaving of multiple trace streams is made possible through the use of a standardized encoding that embeds trace data along with the corresponding trace source ID.
- **Trace export over TPIU** – Trace data is exported over device LVCMOS pins using a standard protocol that embeds trace data along with the corresponding trace source ID.

> **CAUTION**
>
> Debug features that are intrusive in nature may affect the ability of the system to meet critical real-time deadlines and should be used with caution.

13.2 On-Chip Debug Features

The On-Chip Debug framework provides a comprehensive hardware platform for a rich debug and development experience. The On-Chip Debug framework supports these features:

- An IEEE 1149.1 (JTAG and Boundary Scan) compliant device interface
- Cross-triggering and Debug boot mode device interface
- Trace port device interface
- Advanced power, reset, and clock management to facilitate debug across complex low power modes

- Breakpoint-based debug
- Cross-triggering
- Program flow trace
- System traffic monitoring trace
- Software instrumentation trace
- Trace export via trace port device interface
- Trace capture on-chip via dedicated buffer with options to support stop-on-full, circular-buffer, or data hand-off to various peripherals
- Arm® CoreSight™ compliant debug components deployed to streamline 3rd party tooling support

See Module Integration

Note

Some features may not be available. See *Module Integration* for more information.

13.3 On-Chip Debug Functional Description

13.3.1 On-Chip Debug Block Diagram

A logical partitioning of the On-Chip Debug features deployed on this device is illustrated in Figure 13-1.

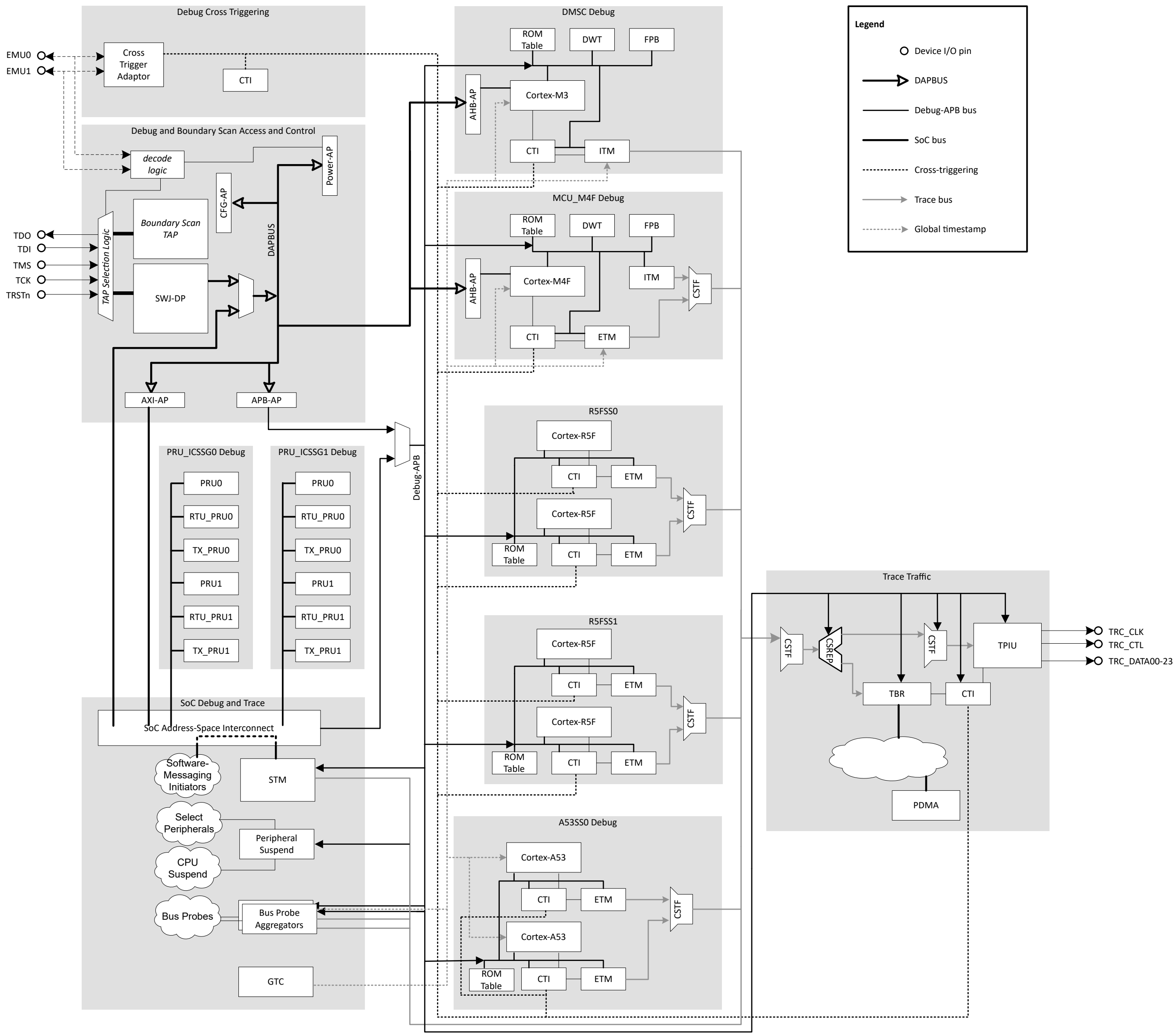

Figure 13-1. On-Chip Debug Block Diagram

13.3.2 Device Interfaces

On-Chip Debug features are supported through three device interfaces:

- **JTAG**: IEEE 1149.1 compliant interface that provides access to Boundary Scan and acts as the primary interface for off-chip access to On-Chip debug resources (See Section 13.3.2.1)
- **Trigger and Debug Boot Mode**: Multi-functional interface that supports product level cross-triggering and debug-related boot modes (See Section 13.3.7 , Section 13.3.4)
- **Trace Port**: Arm TPIU compliant Trace Port interface is used to facilitate export of trace (See Section 13.3.13)

Texas Instruments supports a variety of eXtended Development System (XDS™) JTAG controllers with various debug capabilities beyond only JTAG support. The following document is a good reference for guidelines: Emulation and Trace Headers. More information can also be found here:XDS Target Connection Guide .

The previous link connects to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.3.2.1 JTAG Interface

Table 13-1. JTAG Interface Signals

SignalName	I/OType[1]	Description
TRSTn	I	*Test Reset*. Initializes and disables the test interface.
TCK	I	*Test Clock*. Controls the timing of the test interface independently from any system clocks. TCK is pulsed by the equipment controlling the test and not by the tested device.
TMS	I	*Test Mode Select*. Controls the transitions of the test interface state machine.
TDI	I	*Test Data Input*. Supplies the data to the JTAG registers.
TDO	O/Z	*Test Data Output*. Used to serially output the data from the JTAG registers to the equipment controlling the test.

(1) I = Input; I/O = Input or output; O = Output; O/Z = Output or three-state

13.3.2.2 Trigger and Debug Boot Mode Interface

Table 13-2. Trigger and Debug Boot Mode Interface Signals

Signal Name	I/O Type[1]	Description
EMU0	I/O	Channel 0 trigger or boot mode select
EMU1	I/O	Channel 1 trigger or boot mode select

(1) I = Input; I/O = Input or output; O = Output; O/Z = Output or three-state

13.3.2.3 Trace Port Interface

Table 13-3. Trace Port Signals

Pin Name	TPIU Signal Name	I/O Type[1]	Description
TRC_CLK	TRACECLK	O	TraceClock
TRC_CTL	TRACECTL	O	TraceControl
TRC_DATA[*n*:0]	TRACEDATA[*n*:0]	O	TraceData [*n*:0]

(1) I = Input; I/O = Input or output; O = Output; O/Z = Output or three-state

Note

The Trace Port interface signals are associated with device pins that are multiplexed with other signal functions.

13.3.3 Debug and Boundary Scan Access and Control

On-Chip debug resources are made available through three mechanisms:

- JTAG access via DAP and related APs
- JTAG access via Boundary Scan TAP
- Embedded access to debug resources via SoC address space

DAP

Off-chip debug tools are able to access On-Chip debug resources via the JTAG interface when not in Boundary Scan mode (see below). A CoreSight™ Compliant DAP architecture provides access via a DP and a collection of APs:

- SWJ-DP: Arm® CoreSight™ compliant SWJ Debug Port provides support for a JTAG interface with a 4-bit IR

> **Note**
> Even though an SWJ-DP is implemented on-chip, only JTAG is supported. This device does not support SWD.

- APB-AP: Arm® CoreSight™ APB Access Port provides access to the Debug-APB address space which is the primary configuration space for On-Chip Debug resources.
- AXI-AP: Arm® CoreSight™ AXI Access Port provides access to the SoC address space, allowing visibility and control over system resources.
- Config-AP: TI Configuration AP supports access to SoC debug management registers
- Power-AP: TI Configuration AP supports advanced power, reset, and clock management. (See *Power, Reset, Clock Management*)

Table 13-4 describes the APSEL assignment for this device.

Table 13-4. DAP APSEL Assignment

APSEL	AP	Description
0	Config-AP	TI AP - Reserved
1	APB-AP	Provides access to Debug Config Plane
2	AXI-AP	Provides access to SoC Address Space
3	Power-AP	TI AP - Extended Power/Reset/Clock Control
4-5	Reserved	Reserved for future use
6	SEC-AP	TI AP - Authentication Interface
7	DMSC	
8	MCU_M4F	
10-31	Reserved	Reserved for future use

Boundary Scan

This device supports boundary scan using an IEEE 1149.1 compliant JTAG TAP that is made visible through the use of a compliance-enable mode (see *Debug Boot Modes and Boundary Scan Compliance*). IEEE 1149.1 and 1149.6 Boundary Scan support are defined in device-specific BSDL files that can be found in the respective device's product folder on ti.com.

SoC Address Space

The device architecture provides access to On-Chip debug resources through the SoC Address Space. This includes access to all DAP Access Ports (APs) as well as the Debug-APB address space.

13.3.4 Debug Boot Modes and Boundary Scan Compliance

The EMU1 and EMU0 device pins are used to convey debug boot mode behavior and can also be used as part of a boundary scan compliance sequence to enable boundary scan features.

Debug Boot Mode

EMU1 and EMU0 are sampled when MCU_PORz is de-asserted and the decoded value determines the debug boot mode behavior as detailed in Table 13-5.

Table 13-5. Debug Boot Modes

Sample Time	EMU1	EMU0	Boot Mode	Behavior
MCU_PORz deassertion	0	0	Reserved	Reserved for future use
	0	1	Reserved	Reserved for future use

Table 13-5. Debug Boot Modes (continued)

Sample Time	EMU1	EMU0	Boot Mode	Behavior
	1	0	Wait-In-Reset (WIR)	Device will remain quiescent until a debug connection is established and the debugger releases WIR. This mode is useful for debugging boot sequences.
	1	1	Normal	Device boots normally. Debug can connect at any time but the context will be post-boot.

Boundary Scan Compliance

EMU1 and EMU0 are sampled when TRSTz is de-asserted and the decoded value determines the debug boot mode behavior as detailed in Table 13-6.

Table 13-6. Boundary Scan Compliance

Sample Time	EMU1	EMU0	Boundary Scan Compliance	Behavior
TRSTn deassertion	0	1	Boundary Scan Enabled	The device's Boundary Scan TAP is connected to the device's JTAG interface.
	0	0		
	1	0	Boundary Scan Disabled	The device's SWJ-DP is connected to the device's JTAG interface.
	1	1		

13.3.5 Peripheral Suspend

Some peripherals on the device include support for a debug suspend capability that allows the peripheral's behavior to alter when an assigned CPU enters the debug suspend state. In order to use this feature, it must be enabled within the peripheral and a connection made between the desired suspend source (CPU) and the suspend destination (peripheral) of interest.

Details on the debug suspend feature for a specific peripheral, including how to enable it, is covered in the associated peripheral section.

On this device, there is a dedicated interrupt router (INTR) (DBGSUSPENDROUTER0 that supports the routing of a suspend source to a suspend destination. Details on the assignment of DBGSUSPENDROUTER0 inputs and outputs are provided Table 13-7 and Table 13-8.

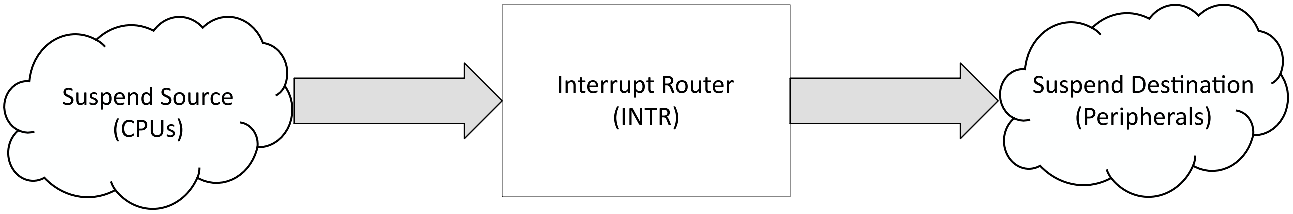

Figure 13-2. Peripheral Suspend Support

Table 13-7. Suspend Source Assignment

Index	Suspend Source	Description
1	A53SS0_0	A53SS0 Core 0
2	A53SS0_1	A53SS0 Core 1
19	R5FSS0_0	R5FSS0 Core 0
20	R5FSS0_1	R5FSS0 Core 1
21	R5FSS1_0	R5FSS1 Core 0
22	R5FSS1_1	R5FSS1 Core 1
24	MCU_M4FSS	MCU M4F

Table 13-8. Suspend Destination Assignment

Index	Suspend Destination	Description
0	GTC0	Global Time Counter
1	CPSW0	Ethernet Switch (SoC)
2	DMSS0	DMA SS (SoC)
5-3	Reserved	Reserved
6	ECAP0	Enhanced Capture Module
7	ECAP1	
8	ECAP2	
9	MCU_DCC0	Dual Clock Comparators
10	MCU_RTI0	Real-time Interrtupt (M4)
11	MCU_MCRC0	CRC64 (MCU)
12	DCC0	Dual Clock Comparators
13	DCC1	
14	DCC2	
15	DCC3	
16	DCC4	
17	DCC5	
18	Reserved	Reserved
19	PDMA0	Peripheral DMA
20	PDMA1	
21	PWM0	Enhanced Hi Resolution PWM (SoC)
22	PWM1	
23	PWM2	
24	PWM3	
25	PWM4	
26	PWM5	
27	EQEP0	Enhanced Quadrature Encoder Pulse (SoC)
28	EQEP1	
29	EQEP2	
30	MCAN0	MCAN
31	MCAN1	
32	MCU_I2C0	I2C (MCU)
33	MCU_I2C1	
34	Reserved	Reserved
35	I2C0	I2C (SoC)
36	I2C1	
37	I2C2	
38	I2C3	
39	PWM6	Enhanced Hi Resolution PWM (SoC)
40	PWM7	
41	PWM8	
42	RTI0	Real-time Interrupt (A53)
43	RTI1	
44	RTI10	Real-time Interrupt R5FSS1
45	RTI11	
46	MCU_TIMER0	Dual Mode Timer (MCU)

Table 13-8. Suspend Destination Assignment (continued)

Index	Suspend Destination	Description
47	MCU_TIMER1	
48	MCU_TIMER2	
49	MCU_TIMER3	
50	RTI8	Real-time Interrupt R5FSS0
51	RTI9	
52	TIMER6	Dual Mode Timer (SoC)
53	TIMER7	
54	TIMER8	
55	TIMER9	
56	TIMER10	
57	TIMER11	
58	TIMER0	
59	TIMER1	
60	TIMER2	
61	TIMER3	
62	TIMER4	
63	TIMER5	
127-64	Reserved	Reserved

13.3.6 Power, Reset, Clock Management

This device includes advanced power, reset, and clock management debug capabilities, including:

- **Wakeup support for debug logic**: logic within the device is able to sense JTAG activity and ensure that debug logic is on and able to service JTAG requests.
- **Reset isolation**: critical configuration and trace datapaths and logic are not sensitive to warm reset
- **Configuration independence**: debug configuration occurs over a debug-only interconnect, separate from SoC traffic to ensure debug logic remains available even during deadlock scenarios.
- **Power-AP**: a CoreSight™ compliant Access Port (AP) developed by TI that provides a standard interface for debug tooling to access status and control over power, reset, and clocking for the system and various LPSC-defined sub-domains.

13.3.7 Debug Cross Triggering

This device supports an Arm® CoreSight™ compliant four-channel programmable on-chip Cross Triggering network. In addition to the four-channel on-chip network, this device implements two channels of product level triggering via the EMU0 and EMU1 device pins.

Conceptually, each channel of Cross Triggering can be viewed as mapping of a user-defined set of events to a user-defined set of actions, where the occurrence of any event in the set-of-events results in the generation of the set-of-actions. Table 13-9 provides a domain-level summary of the supported events and actions.

Table 13-9. Domain-Level Summary of Triggering Capability

Domain	Events	Actions
Product-Level	Zero detected on EMU0 input pin	EMU0 output pin driven to Zero
	Zero detected on EMU1 input pin	EMU1 output pin driven to Zero
SoC Debug	TBR Acquisition Complete	TPIU insert trigger packet
	TBR Embedded buffer is full	TPIU start flush process
	System reset asserted	TBR insert trigger packet
	Bus Probe-n match	TBR start flush process
	STM write to a TRIG location	Bus Probe-n Start

Table 13-9. Domain-Level Summary of Triggering Capability (continued)

Domain	Events	Actions
	STM write to a trigger-enabled stimulus port	Bus Probe-n Stop
DMSC0	DMSC_M3 has halted	DMSC_M3 - halt request
		DMSC_M3 - resume request
MCU_M4F	MCU_M4F has halted	MCU_M4F – halt request
	ETM External Out (EXTOUT) trigger	MCU_M4F – resume request
	--	ETM External In (EXTIN) trigger
R5FFS0, R5FFS1	R5FFS# core-n has halted	R5FFS# core-n – halt request
	PMU generated interrupt	R5FFS# core-n – resume request
	ETM External Out (EXTOUT) trigger	ETM External In (EXTIN) trigger
A53SS0	A53SS0 core-n has halted	A53SS0 core-n – halt request
	PMU generated interrupt	A53SS0 core-n – resume request
	ETM External Out (EXTOUT) trigger	CTI interrupt
	--	ETM External In (EXTIN) trigger

13.3.8 R5FSS0/R5FSS1 Debug

This device includes two R5FSS sunsystems named R5FSS0 and R5FSS1. The R5FSS subsystem includes two Cortex-R5F corex and embedded debug capability, including:

- Independent debug configuration
- ROM Table
- Basic debug functionality (per core)
- Cross Triggering (per core)
- PMU: Performance Monitor Unit (per core)
- ETM: Embedded Trace Macrocell (per core)

A summary of the R5FSS0, R5FSS1 debug capabilities is detailed in Table 13-10.

Table 13-10. R5FSS0/R5FSS1 Debug Capabilities

Capability	Feature	Notes
Basic Debug	Independent debug configuration	Debug resource configuration is performed over a configuration interface that is isolated from functional traffic
	ROM table	Facilitates discovery of debug resources within debug configuration address space
	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state
	Software breakpoints	Software breakpoints are supported via opcode replacement
	Hardware breakpoints	Eight Debug Breakpoint resources support hardware breakpoints
	Hardware watchpoints	Eight Debug Watchpoint resources support data address breakpoints
	Core register access	Access to processor core registers
	System memory access	Access to memory from perspective of CPU
	Vector catch	Halting in response to an exception
	Arm® TrustZone® debug authentication	Provisioning for DBGEN and NIDEN
Cross Triggering	Debug state	Support for controlling execution state (run, halt) via triggers and creating triggers upon entry into debug state
	PMU	PMU interrupt trigger
	ETM	Five ETM external triggers (one ETM Trigger, two external out event triggers, two external in event triggers)
PMU	Profile Counters	Three counters can be used to count different events available for gathering statistics on the operation of the processor and memory system
	Cycle Counter	One dedicated counter available for counting CPU clock cycles

Table 13-10. R5FSS0/R5FSS1 Debug Capabilities (continued)

Capability	Feature	Notes
ETM	Triggering Infrastructure	Comprehensive triggering infrastructure supports use of comparators (address, data value, context ID), counters, sequencer state, an external inputs and outputs to control the enabling of trace.
	Instruction trace	Supports tracing of instruction flow
	Cycle-accurate tracing	Supports inclusion of a precise cycle count of executed instructions.
	Branch broadcast tracing	Support for tracing branch address details even in circumstances where that information might be discoverable from object code
	Data tracing	Support for data address and data value tracing

13.3.9 DMSC Debug

The DMSC0 includes an Arm Cortex M3 with embedded debug capability, including:

- Independent debug configuration via AHB-AP
- ROM Table
- Basic debug functionality
- Cross Triggering
- DWT : Data Watchpoint and Trace
- FPB : Flash Patch Breakpoint
- ITM : Instrumentation Trace Macrocell

A summary of the DMSC0 debug capabilities is detailed in Table 13-11.

Table 13-11. DMSC Debug Capabilities

Capability	Feature	Notes
Basic Debug	AHB-AP	AHB-AP provides access to resources
	ROM table	Facilitates discovery of debug resources within AHB-AP address space
	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state
	Core register access	Access to processor core registers
	Vector catch	Halting in response to an exception
	Software breakpoints	Software breakpoints are supported via opcode replacement
	System memory access	Access to M3 address space is supported via AHB-AP
Cross Triggering	Cross Triggering	Cross Triggering support via CoreSight™ CTI
DWT	Watchpoints	Four comparators implemented that can be configured to support watchpoints, data address trace, and PC sampling
	Data address trace	
	PC sampling trace	
	Cycle count matching	
	Performance counting	Profiling counter support provides visibility into instruction cycle count, exception overhead, sleep overhead, load-store overhead, and folded instruction count
FPB	Hardware breakpoints	Six instruction address comparators support hardware breakpoints
	Remapping of literal and instruction fetch accesses	Two comparators support address remapping of literal or instruction accesses to facilitate software patching
ITM	Software trace	Software writes to ITM stimulus registers provoke the generation of trace packets that convey the values written
	DWT hardware trace	Support for conveying DWT output using trace
	Timestamping	Support for attaching a local timestamp to trace traffic
	Global timestamping	Support for attaching a global timestamp to trace traffic

13.3.10 A53SS0 Debug

The A53SS0 is a multi-core Arm Cortex-A53 subsystem with embedded debug capability and features, including:

- Independent debug configuration
- ROM Table
- Basic debug functionality
- Cross Triggering
- PMU: Performance Monitor Unit
- ETM: Embedded Trace Macrocell

A summary of the A53SS0 debug capabilities and features is detailed in Table 13-12.

Table 13-12. A53SS0 Debug Capabilities

Capability	Feature	Notes
Basic Debug	Independent debug configuration	Debug resource configuration is performed over a configuration interface that is isolated from functional traffic
	ROM table	Facilitates discovery of debug resources within debug configuration address space
	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state
	Software breakpoints	Software breakpoints are supported via opcode replacement
	Hardware breakpoints	Six Debug Breakpoint resources support hardware breakpoints
	Hardware watchpoints	Four Debug Watchpoint resources support data address breakpoints
	Core register access	Access to processor core registers
	System memory access	Access to memory from perspective of CPU
	Vector catch	Halting in response to an exception
	Arm® TrustZone® debug authentication	Provisioning for DBGEN, NIDEN, SPIDEN, SPNIDEN, SUIDEN, and SUNIDEN
Cross Triggering	Debug state	Support for controlling execution state (run, halt) via triggers and creating triggers upon entry into debug state
	PMU	PMU interrupt trigger
	ETM	Four ETM external triggers
	CPU	CTI interrupt into CPU
PMU	Profile Counters	Six counters can be used to count different events available for gathering statistics on the operation of the processor and memory system
	Cycle Counter	One dedicated counter available for counting CPU clock cycles
ETM	Instruction trace with cycle counting	Support for tracing instruction execution with timing information
	Branch broadcast tracing	Support for tracing branch address details even in circumstances where that information might be discoverable from object code
	Return stack tracing	Support for tracing of the return stack
	Stall Control	Support for stalling the A53 processor to avoid ETM overflows
	Global timestamping	Support for attaching a global timestamp to trace traffic

13.3.11 PRU_ICSSG0/PRU_ICSSG1 Debug

This device includes two PRU_ICSSG instances named PRU_ICSSG0 and PRU_ICSSG1. The PRU_ICSSG includes six PRU RISC cores: PRU0, RTU_PRU0, TX_PRU0, PRU1, RTU_PRU1 and TX_PRU1. Each PRU supports basic debug functionality as detailed in Table 13-13.

Table 13-13. PRU_ICSS Debug Capabilities

Capability	Feature	Notes
Basic Debug	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state

Table 13-13. PRU_ICSS Debug Capabilities (continued)

Capability	Feature	Notes
	Software breakpoints	Software breakpoints are supported via opcode replacement
	Core register access	Access to processor core registers
	System memory access	Access to memory from perspective of CPU

13.3.12 SoC Debug and Trace

This device includes debug capabilities deployed at the system level, including:

- Software messaging trace
- Debug-aware peripherals
- Traffic monitoring with bus probes
- Global timestamping for trace

More details for each of these capability areas can be found in the corresponding sections below.

13.3.12.1 Software Messaging Trace

Software messaging trace is supported on this device by an MIPI STP-V2 compliant Arm® CoreSight™ STM with supporting logic that maps initiator IDs to specific STP Major Source IDs. The following device initiators support software messaging:

- A53SS0 cores
- DMSC0
- R5FSS0, R5FSS1
- MCU_M4F

13.3.12.2 Debug-Aware Peripherals

Select peripherals support a debug feature that allows them to react to the debug state of a controlling processor. For instance, a timer peripheral that is allocated to a particular processor could be configured to stop counting when the associated processor is in the halted state.

This device includes programmable support for shared peripherals that allows the developer to select the processor whose debug state a given peripheral should receive. Peripherals that are debug aware include programmable support to enable or disable sensitivity to debug.

A list of the processors and peripherals that support this debug model can be found in Table 13-14.

Table 13-14. Debug-Aware Peripheral Support

Supported Processors	Supported Peripherals
A53SS0 cores	GTC
R5FSS0, R5FSS1	CPSW3G
MCU_M4F	DMSS
--	TIMER instances
--	EPWM instances
--	MCAN instances
--	I2C instances
--	MCRC64 instances
--	ECAP instances
--	EQEP instances
--	PDMA0 (SPI0-2, UART0-1)
--	PDMA1 (SPI4, UART2-6, MCAN0-1, ADC0)
--	RTI/WWDT instances(1)

(1) RTI/WWDT suspend is associated with the processor that it is allocated to

13.3.12.3 Debug Suspend Router Connections

Debug Suspend Router Connections are shown in Table 13-15 and Table 13-16.

Table 13-15. Debug Suspend Router Connections (Inputs)

Index	Connection
0	Reserved
1	COMPUTE_CLUSTER0.CPU0
2	COMPUTE_CLUSTER0.CPU1
3-18	Reserved
19	R5FSS0
20	R5FSS0
21	R5FSS1
22	R5FSS1
23	Reserved
24	MCU_M4FSS0
25-31	Reserved

Table 13-16. Debug Suspend Router Connections (Outputs)

Index	Connection
0	GTC0
1	CPSW0
2	DMASS0
3-5	Reserved
6	ECAP0
7	ECAP1
8	ECAP2
9	Reserved
10	MCU_RTI0
11	MCU_MCRC64_0
12-18	Reserved
19	PDMA0
20	PDMA1
21	EPWM0
22	EPWM1
23	EPWM2
24	EPWM3
25	EPWM4
26	EPWM5
27	EQEP0
28	EQEP1
29	EQEP2
30	MCAN0
31	MCAN1
32	MCU_I2C0
33	MCU_I2C1
34	Reserved
35	I2C0
36	I2C1

Table 13-16. Debug Suspend Router Connections (Outputs) (continued)

Index	Connection
37	I2C2
38	I2C3
39	EPWM6
40	EPWM7
41	EPWM8
42	RTI0
43	RTI1
44	RTI10
45	RTI11
46	MCU_TIMER0
47	MCU_TIMER1
48	MCU_TIMER2
49	MCU_TIMER3
50	RTI8
51	RTI9
52	TIMER6
53	TIMER7
54	TIMER8
55	TIMER9
56	TIMER10
57	TIMER11
58	TIMER0
59	TIMER1
60	TIMER2
61	TIMER3
62	TIMER4

13.3.12.4 Traffic Monitoring With Bus Probes

Traffic monitoring bus probes are deployed at strategic points in the system interconnect and support the following capabilities:

- MIPI STP-V2 compliant trace messaging support with global timestamping support
- Latency Statistics Collection: Statistics on the timeliness of responses to read requests are collected during a sampling window and then read by a profiling entity (application thread or encoded into a trace message)
- Throughput Statistics Collection: Statistics on the amount of data moving across an interface are collected during a sampling window and then read by a profiling entity (application thread or encoded into a trace message)
- Transaction Trace: Information about specific transactions occurring at a probed location are captured and encoded into a trace message
- Complex filtering support allows discrimination of traffic being monitored
- Cross-Trigger support for enabling and disabling probe monitoring

Table 13-17 details the locations in the system interconnect that are probed:

Table 13-17. Bus Probe Points

Probe Point	Bus Monitoring Details
A53SS0 Write Initiator	Provides visibility to all write requests initiated by A53SS0
A53SS0 Read Initiator	Provides visibility to all read requests initiated by A53SS0
A53SS0 ACP Target	Monitors traffic to the A53SS0 ACP port

Table 13-17. Bus Probe Points (continued)

Probe Point	Bus Monitoring Details
DDR Target	Monitors traffic to DDR
GMPC Target	Monitors traffic to GPMC
FSS Target	Monitors traffic to FSS0
INFRA_CBASS0	Monitors traffic from CBASS0 to INFRA_CBASS0.
MCU_CBASS0	Monitors traffic from CBASS0 to MCU_CBASS0.
OCSRAM bank-n	Monitors traffic to the OCSRAM. Each bank of OCSRAM is supported by a dedicate probe.

13.3.12.5 Global Timestamping for Trace

Support for a global timestamp for use by debug is enabled by a 48-bit continuous timestamp managed by the device's GTC. This 48-bit global timestamp is readable by embedded software, via the GTC, and distributed across the device to various trace sources where it is used as a time reference when timestamping trace streams. Trace sources that support global timestamping, include:

- A53SS0 cores: ETM
- MCU_M4F: ITM and ETM
- STM
- Bus Probes

13.3.13 Trace Traffic

Trace traffic originates from a trace source, is distributed across the device using Arm® CoreSight™ compliant trace infrastructure components, and reaches one of two possible trace sinks.

13.3.13.1 Trace Sources

A summary of the trace sources present on this device is included in Table 13-18.

Table 13-18. Trace Sources

Domain	Trace Source
SoC Debug	Bus Probes
	STM
DMSC0	ITM
MCU_M4F	ITM
	ETM
R5FSS0, R5FSS1	ETM (each core)
A53SS0	ETM (each core)

13.3.13.2 Trace Infrastructure

Trace distribution is accomplished using standard Arm® CoreSight™ compliant trace infrastructure components:

- CoreSight™ Trace Funnels (CSTF): Non-programmable CSTFs are used at points of interleaving where multiple trace sources converge and form a single stream of trace traffic. This device includes one instance of a programmable CSTF that is deployed immediately before the TPIU.
- CoreSight™ Trace Replicator (CSREP): A programmable CSREP is used as a routing device, that can be used to forward trace traffic, based on its ID, to one, both, or none of the device trace sinks.

13.3.13.3 Trace Sinks

Two trace sinks are supported on this device:

- Arm® CoreSight™ TPIU: TPIU supports export of trace off-chip via LVCMOS device pins (See 1.3.3.3) for capture by an external receiver.
- TI Trace Buffer Router (TBR) with 64KB of storage: the TBR can function as a trace buffer or as a system bridge. As a trace buffer, the TBR can be setup to capture trace data until the internal buffer fills or it can operate as a circular buffer that will capture continuously. When configured as a system bridge the TBR's

storage becomes an elastic buffer that supports the concurrent queueing and dequeuing of trace traffic. The system bridge mode supports interrupt and event notification capabilities that support integration with device level CPUs and/or DMAs to support a variety of use cases, including, for e.g., relocation of trace data to DDR and off-chip export over USB.

13.3.14 Application Support

TI includes a set of system level debug facilities in the Debug Subsystem of devices known as Chip Tools (CTools). For easy integration of A53 processor trace and system trace into applications, a set of libraries commonly referred to as CToolsLib are provided. CToolsLib is a collection of embedded target APIs/libraries focused on enabling easy access to the CTools. CToolsLib encompasses the following libraries to assist in trace integration:

- STM Library
- CP Tracer Library
- TBR Library
- ETM Library

For more information about these libraries, downloadable files, and other useful links, please visit the CToolsLib Wiki site.

The previous link connects to TI community resources. Linked contents are provided “AS IS” by the respectivecontributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

Chapter 14

Registers

14.1 System Interconnect Registers

14.1.1 CBASS Registers

14.1.1.1 CBASS Summary Table

Table 14-1. CBASS0_ERR Registers, Base Address=3A00 0000h, Length=1024

Offset	Length	Register Name	CBASS Physical Address
0h	32	CBASS_ERR_PID	3A00 0000h
4h	32	CBASS_ERR_DESTINATION_ID	3A00 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	3A00 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	3A00 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	3A00 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	3A00 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	3A00 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	3A00 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	3A00 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	3A00 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	3A00 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	3A00 005Ch
60h	32	CBASS_ERR_EOI	3A00 0060h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768

Offset	Length	Register Name	CBASS Physical Address
400h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL	4500 0400h
404h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0	4500 0404h
408h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1	4500 0408h
40Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2	4500 040Ch
410h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L	4500 0410h
414h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H	4500 0414h
418h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L	4500 0418h
41Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H	4500 041Ch
420h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL	4500 0420h
424h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0	4500 0424h
428h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1	4500 0428h
42Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2	4500 042Ch
430h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L	4500 0430h
434h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H	4500 0434h
438h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L	4500 0438h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
43Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H	4500 043Ch
440h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL	4500 0440h
444h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0	4500 0444h
448h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1	4500 0448h
44Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2	4500 044Ch
450h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L	4500 0450h
454h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H	4500 0454h
458h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L	4500 0458h
45Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H	4500 045Ch
460h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL	4500 0460h
464h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0	4500 0464h
468h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1	4500 0468h
46Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2	4500 046Ch
470h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L	4500 0470h
474h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H	4500 0474h
478h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L	4500 0478h
47Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H	4500 047Ch
480h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL	4500 0480h
484h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0	4500 0484h
488h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1	4500 0488h
48Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2	4500 048Ch
490h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L	4500 0490h
494h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H	4500 0494h
498h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L	4500 0498h
49Ch	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H	4500 049Ch
4A0h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL	4500 04A0h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
4A4h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0	4500 04A4h
4A8h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1	4500 04A8h
4ACh	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2	4500 04ACh
4B0h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L	4500 04B0h
4B4h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H	4500 04B4h
4B8h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L	4500 04B8h
4BCh	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H	4500 04BCh
4C0h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL	4500 04C0h
4C4h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0	4500 04C4h
4C8h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1	4500 04C8h
4CCh	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2	4500 04CCh
4D0h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L	4500 04D0h
4D4h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H	4500 04D4h
4D8h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L	4500 04D8h
4DCh	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H	4500 04DCh
4E0h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL	4500 04E0h
4E4h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0	4500 04E4h
4E8h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1	4500 04E8h
4ECh	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2	4500 04ECh
4F0h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L	4500 04F0h
4F4h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H	4500 04F4h
4F8h	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L	4500 04F8h
4FCh	32	CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H	4500 04FCh
800h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL	4500 0800h
804h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0	4500 0804h
808h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1	4500 0808h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
80Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2	4500 080Ch
810h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L	4500 0810h
814h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H	4500 0814h
818h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L	4500 0818h
81Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H	4500 081Ch
820h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL	4500 0820h
824h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0	4500 0824h
828h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1	4500 0828h
82Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2	4500 082Ch
830h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L	4500 0830h
834h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H	4500 0834h
838h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L	4500 0838h
83Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H	4500 083Ch
840h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL	4500 0840h
844h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0	4500 0844h
848h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1	4500 0848h
84Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2	4500 084Ch
850h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L	4500 0850h
854h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H	4500 0854h
858h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L	4500 0858h
85Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H	4500 085Ch
860h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL	4500 0860h
864h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0	4500 0864h
868h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1	4500 0868h
86Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2	4500 086Ch
870h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L	4500 0870h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
874h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H	4500 0874h
878h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L	4500 0878h
87Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H	4500 087Ch
880h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL	4500 0880h
884h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0	4500 0884h
888h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1	4500 0888h
88Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2	4500 088Ch
890h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L	4500 0890h
894h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H	4500 0894h
898h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L	4500 0898h
89Ch	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H	4500 089Ch
8A0h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL	4500 08A0h
8A4h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0	4500 08A4h
8A8h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1	4500 08A8h
8ACh	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2	4500 08ACh
8B0h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L	4500 08B0h
8B4h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H	4500 08B4h
8B8h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L	4500 08B8h
8BCh	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H	4500 08BCh
8C0h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL	4500 08C0h
8C4h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0	4500 08C4h
8C8h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1	4500 08C8h
8CCh	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2	4500 08CCh
8D0h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L	4500 08D0h
8D4h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H	4500 08D4h
8D8h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L	4500 08D8h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
8DCh	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H	4500 08DCh
8E0h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL	4500 08E0h
8E4h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0	4500 08E4h
8E8h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1	4500 08E8h
8ECh	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2	4500 08ECh
8F0h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L	4500 08F0h
8F4h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H	4500 08F4h
8F8h	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L	4500 08F8h
8FCh	32	CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H	4500 08FCh
3800h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_CONTROL	4500 3800h
3804h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0	4500 3804h
3808h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1	4500 3808h
380Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2	4500 380Ch
3810h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L	4500 3810h
3814h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H	4500 3814h
3818h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L	4500 3818h
381Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H	4500 381Ch
3820h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_CONTROL	4500 3820h
3824h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0	4500 3824h
3828h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1	4500 3828h
382Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2	4500 382Ch
3830h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L	4500 3830h
3834h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H	4500 3834h
3838h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L	4500 3838h
383Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H	4500 383Ch
3840h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_CONTROL	4500 3840h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
3844h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0	4500 3844h
3848h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1	4500 3848h
384Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2	4500 384Ch
3850h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L	4500 3850h
3854h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H	4500 3854h
3858h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L	4500 3858h
385Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H	4500 385Ch
3860h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_CONTROL	4500 3860h
3864h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0	4500 3864h
3868h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1	4500 3868h
386Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2	4500 386Ch
3870h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L	4500 3870h
3874h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H	4500 3874h
3878h	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L	4500 3878h
387Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H	4500 387Ch
3C00h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_CONTROL	4500 3C00h
3C04h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0	4500 3C04h
3C08h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1	4500 3C08h
3C0Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2	4500 3C0Ch
3C10h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L	4500 3C10h
3C14h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H	4500 3C14h
3C18h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L	4500 3C18h
3C1Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H	4500 3C1Ch
3C20h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_CONTROL	4500 3C20h
3C24h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0	4500 3C24h
3C28h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1	4500 3C28h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
3C2Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2	4500 3C2Ch
3C30h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L	4500 3C30h
3C34h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H	4500 3C34h
3C38h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L	4500 3C38h
3C3Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H	4500 3C3Ch
3C40h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_CONTROL	4500 3C40h
3C44h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0	4500 3C44h
3C48h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1	4500 3C48h
3C4Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2	4500 3C4Ch
3C50h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L	4500 3C50h
3C54h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H	4500 3C54h
3C58h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L	4500 3C58h
3C5Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H	4500 3C5Ch
3C60h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_CONTROL	4500 3C60h
3C64h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0	4500 3C64h
3C68h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1	4500 3C68h
3C6Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2	4500 3C6Ch
3C70h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L	4500 3C70h
3C74h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H	4500 3C74h
3C78h	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L	4500 3C78h
3C7Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H	4500 3C7Ch
4000h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_CONTROL	4500 4000h
4004h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0	4500 4004h
4008h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1	4500 4008h
400Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2	4500 400Ch
4010h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L	4500 4010h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
4014h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H	4500 4014h
4018h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L	4500 4018h
401Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H	4500 401Ch
4020h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_CONTROL	4500 4020h
4024h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0	4500 4024h
4028h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1	4500 4028h
402Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2	4500 402Ch
4030h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L	4500 4030h
4034h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H	4500 4034h
4038h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L	4500 4038h
403Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H	4500 403Ch
4040h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_CONTROL	4500 4040h
4044h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0	4500 4044h
4048h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1	4500 4048h
404Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2	4500 404Ch
4050h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L	4500 4050h
4054h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H	4500 4054h
4058h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L	4500 4058h
405Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H	4500 405Ch
4060h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_CONTROL	4500 4060h
4064h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0	4500 4064h
4068h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1	4500 4068h
406Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2	4500 406Ch
4070h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L	4500 4070h
4074h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H	4500 4074h
4078h	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L	4500 4078h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
407Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H	4500 407Ch
4400h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_CONTROL	4500 4400h
4404h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0	4500 4404h
4408h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1	4500 4408h
440Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2	4500 440Ch
4410h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L	4500 4410h
4414h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H	4500 4414h
4418h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L	4500 4418h
441Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H	4500 441Ch
4420h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_CONTROL	4500 4420h
4424h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0	4500 4424h
4428h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1	4500 4428h
442Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2	4500 442Ch
4430h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L	4500 4430h
4434h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H	4500 4434h
4438h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L	4500 4438h
443Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H	4500 443Ch
4440h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_CONTROL	4500 4440h
4444h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0	4500 4444h
4448h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1	4500 4448h
444Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2	4500 444Ch
4450h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L	4500 4450h
4454h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H	4500 4454h
4458h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L	4500 4458h
445Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H	4500 445Ch
4460h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_CONTROL	4500 4460h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
4464h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0	4500 4464h
4468h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1	4500 4468h
446Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2	4500 446Ch
4470h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L	4500 4470h
4474h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H	4500 4474h
4478h	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L	4500 4478h
447Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H	4500 447Ch
4800h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_CONTROL	4500 4800h
4804h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0	4500 4804h
4808h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1	4500 4808h
480Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2	4500 480Ch
4810h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L	4500 4810h
4814h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H	4500 4814h
4818h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L	4500 4818h
481Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H	4500 481Ch
4820h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_CONTROL	4500 4820h
4824h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0	4500 4824h
4828h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1	4500 4828h
482Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2	4500 482Ch
4830h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L	4500 4830h
4834h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H	4500 4834h
4838h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L	4500 4838h
483Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H	4500 483Ch
4840h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_CONTROL	4500 4840h
4844h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0	4500 4844h
4848h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1	4500 4848h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
484Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2	4500 484Ch
4850h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L	4500 4850h
4854h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H	4500 4854h
4858h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L	4500 4858h
485Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H	4500 485Ch
4860h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_CONTROL	4500 4860h
4864h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0	4500 4864h
4868h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1	4500 4868h
486Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2	4500 486Ch
4870h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L	4500 4870h
4874h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H	4500 4874h
4878h	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L	4500 4878h
487Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H	4500 487Ch
4C00h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_CONTROL	4500 4C00h
4C04h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0	4500 4C04h
4C08h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1	4500 4C08h
4C0Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2	4500 4C0Ch
4C10h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L	4500 4C10h
4C14h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H	4500 4C14h
4C18h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L	4500 4C18h
4C1Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H	4500 4C1Ch
4C20h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_CONTROL	4500 4C20h
4C24h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0	4500 4C24h
4C28h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1	4500 4C28h
4C2Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2	4500 4C2Ch
4C30h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L	4500 4C30h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
4C34h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H	4500 4C34h
4C38h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L	4500 4C38h
4C3Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H	4500 4C3Ch
4C40h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_CONTROL	4500 4C40h
4C44h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0	4500 4C44h
4C48h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1	4500 4C48h
4C4Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2	4500 4C4Ch
4C50h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L	4500 4C50h
4C54h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H	4500 4C54h
4C58h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L	4500 4C58h
4C5Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H	4500 4C5Ch
4C60h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_CONTROL	4500 4C60h
4C64h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0	4500 4C64h
4C68h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1	4500 4C68h
4C6Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2	4500 4C6Ch
4C70h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L	4500 4C70h
4C74h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H	4500 4C74h
4C78h	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L	4500 4C78h
4C7Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H	4500 4C7Ch
5000h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL	4500 5000h
5004h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0	4500 5004h
5008h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1	4500 5008h
500Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2	4500 500Ch
5010h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L	4500 5010h
5014h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H	4500 5014h
5018h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L	4500 5018h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
501Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H	4500 501Ch
5020h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL	4500 5020h
5024h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0	4500 5024h
5028h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1	4500 5028h
502Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2	4500 502Ch
5030h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L	4500 5030h
5034h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H	4500 5034h
5038h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L	4500 5038h
503Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H	4500 503Ch
5040h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL	4500 5040h
5044h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0	4500 5044h
5048h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1	4500 5048h
504Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2	4500 504Ch
5050h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L	4500 5050h
5054h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H	4500 5054h
5058h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L	4500 5058h
505Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H	4500 505Ch
5060h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL	4500 5060h
5064h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0	4500 5064h
5068h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1	4500 5068h
506Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2	4500 506Ch
5070h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L	4500 5070h
5074h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H	4500 5074h
5078h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L	4500 5078h
507Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H	4500 507Ch
5080h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL	4500 5080h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
5084h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0	4500 5084h
5088h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1	4500 5088h
508Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2	4500 508Ch
5090h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L	4500 5090h
5094h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H	4500 5094h
5098h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L	4500 5098h
509Ch	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H	4500 509Ch
50A0h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL	4500 50A0h
50A4h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0	4500 50A4h
50A8h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1	4500 50A8h
50ACh	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2	4500 50ACh
50B0h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L	4500 50B0h
50B4h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H	4500 50B4h
50B8h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L	4500 50B8h
50BCh	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H	4500 50BCh
50C0h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL	4500 50C0h
50C4h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0	4500 50C4h
50C8h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1	4500 50C8h
50CCh	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2	4500 50CCh
50D0h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L	4500 50D0h
50D4h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H	4500 50D4h
50D8h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L	4500 50D8h
50DCh	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H	4500 50DCh
50E0h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL	4500 50E0h
50E4h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0	4500 50E4h
50E8h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1	4500 50E8h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
50ECh	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2	4500 50ECh
50F0h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L	4500 50F0h
50F4h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H	4500 50F4h
50F8h	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L	4500 50F8h
50FCh	32	CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H	4500 50FCh
5400h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_CONTROL	4500 5400h
5404h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_0	4500 5404h
5408h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_1	4500 5408h
540Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_2	4500 540Ch
5410h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_L	4500 5410h
5414h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_H	4500 5414h
5418h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_L	4500 5418h
541Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_H	4500 541Ch
5420h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_CONTROL	4500 5420h
5424h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_0	4500 5424h
5428h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_1	4500 5428h
542Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_2	4500 542Ch
5430h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_L	4500 5430h
5434h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_H	4500 5434h
5438h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_L	4500 5438h
543Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_H	4500 543Ch
5440h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_CONTROL	4500 5440h
5444h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_0	4500 5444h
5448h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_1	4500 5448h
544Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_2	4500 544Ch
5450h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_L	4500 5450h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
5454h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_H	4500 5454h
5458h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_L	4500 5458h
545Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_H	4500 545Ch
5460h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_CONTROL	4500 5460h
5464h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_0	4500 5464h
5468h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_1	4500 5468h
546Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_2	4500 546Ch
5470h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_L	4500 5470h
5474h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_H	4500 5474h
5478h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_L	4500 5478h
547Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_H	4500 547Ch
5480h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_CONTROL	4500 5480h
5484h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_0	4500 5484h
5488h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_1	4500 5488h
548Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_2	4500 548Ch
5490h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_L	4500 5490h
5494h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_H	4500 5494h
5498h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_L	4500 5498h
549Ch	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_H	4500 549Ch
54A0h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_CONTROL	4500 54A0h
54A4h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_0	4500 54A4h
54A8h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_1	4500 54A8h
54ACh	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_2	4500 54ACh
54B0h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_L	4500 54B0h
54B4h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_H	4500 54B4h
54B8h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_L	4500 54B8h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
54BCh	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_H	4500 54BCh
54C0h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_CONTROL	4500 54C0h
54C4h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_0	4500 54C4h
54C8h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_1	4500 54C8h
54CCh	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_2	4500 54CCh
54D0h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_L	4500 54D0h
54D4h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_H	4500 54D4h
54D8h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_L	4500 54D8h
54DCh	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_H	4500 54DCh
54E0h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_CONTROL	4500 54E0h
54E4h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_0	4500 54E4h
54E8h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_1	4500 54E8h
54ECh	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_2	4500 54ECh
54F0h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_L	4500 54F0h
54F4h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_H	4500 54F4h
54F8h	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_L	4500 54F8h
54FCh	32	CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_H	4500 54FCh
5800h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_CONTROL	4500 5800h
5804h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_0	4500 5804h
5808h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_1	4500 5808h
580Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_2	4500 580Ch
5810h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_L	4500 5810h
5814h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_H	4500 5814h
5818h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_L	4500 5818h
581Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_H	4500 581Ch
5820h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_CONTROL	4500 5820h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
5824h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_0	4500 5824h
5828h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_1	4500 5828h
582Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_2	4500 582Ch
5830h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_L	4500 5830h
5834h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_H	4500 5834h
5838h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_L	4500 5838h
583Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_H	4500 583Ch
5840h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_CONTROL	4500 5840h
5844h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_0	4500 5844h
5848h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_1	4500 5848h
584Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_2	4500 584Ch
5850h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_L	4500 5850h
5854h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_H	4500 5854h
5858h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_L	4500 5858h
585Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_H	4500 585Ch
5860h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_CONTROL	4500 5860h
5864h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_0	4500 5864h
5868h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_1	4500 5868h
586Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_2	4500 586Ch
5870h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_L	4500 5870h
5874h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_H	4500 5874h
5878h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_L	4500 5878h
587Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_H	4500 587Ch
5880h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_CONTROL	4500 5880h
5884h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_0	4500 5884h
5888h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_1	4500 5888h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
588Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_2	4500 588Ch
5890h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_L	4500 5890h
5894h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_H	4500 5894h
5898h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_L	4500 5898h
589Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_H	4500 589Ch
58A0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_CONTROL	4500 58A0h
58A4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_0	4500 58A4h
58A8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_1	4500 58A8h
58ACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_2	4500 58ACh
58B0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_L	4500 58B0h
58B4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_H	4500 58B4h
58B8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_L	4500 58B8h
58BCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_H	4500 58BCh
58C0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_CONTROL	4500 58C0h
58C4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_0	4500 58C4h
58C8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_1	4500 58C8h
58CCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_2	4500 58CCh
58D0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_L	4500 58D0h
58D4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_H	4500 58D4h
58D8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_L	4500 58D8h
58DCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_H	4500 58DCh
58E0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_CONTROL	4500 58E0h
58E4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_0	4500 58E4h
58E8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_1	4500 58E8h
58ECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_2	4500 58ECh
58F0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_L	4500 58F0h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
58F4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_H	4500 58F4h
58F8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_L	4500 58F8h
58FCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_H	4500 58FCh
5900h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_CONTROL	4500 5900h
5904h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_0	4500 5904h
5908h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_1	4500 5908h
590Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_2	4500 590Ch
5910h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_L	4500 5910h
5914h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_H	4500 5914h
5918h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_L	4500 5918h
591Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_H	4500 591Ch
5920h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_CONTROL	4500 5920h
5924h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_0	4500 5924h
5928h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_1	4500 5928h
592Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_2	4500 592Ch
5930h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_L	4500 5930h
5934h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_H	4500 5934h
5938h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_L	4500 5938h
593Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_H	4500 593Ch
5940h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_CONTROL	4500 5940h
5944h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_0	4500 5944h
5948h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_1	4500 5948h
594Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_2	4500 594Ch
5950h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_L	4500 5950h
5954h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_H	4500 5954h
5958h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_L	4500 5958h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
595Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_H	4500 595Ch
5960h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_CONTROL	4500 5960h
5964h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_0	4500 5964h
5968h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_1	4500 5968h
596Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_2	4500 596Ch
5970h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_L	4500 5970h
5974h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_H	4500 5974h
5978h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_L	4500 5978h
597Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_H	4500 597Ch
5980h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_CONTROL	4500 5980h
5984h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_0	4500 5984h
5988h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_1	4500 5988h
598Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_2	4500 598Ch
5990h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_L	4500 5990h
5994h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_H	4500 5994h
5998h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_L	4500 5998h
599Ch	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_H	4500 599Ch
59A0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_CONTROL	4500 59A0h
59A4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_0	4500 59A4h
59A8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_1	4500 59A8h
59ACh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_2	4500 59ACh
59B0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_L	4500 59B0h
59B4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_H	4500 59B4h
59B8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_L	4500 59B8h
59BCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_H	4500 59BCh
59C0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_CONTROL	4500 59C0h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
59C4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_0	4500 59C4h
59C8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_1	4500 59C8h
59CCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_2	4500 59CCh
59D0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_L	4500 59D0h
59D4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_H	4500 59D4h
59D8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_L	4500 59D8h
59DCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_H	4500 59DCh
59E0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_CONTROL	4500 59E0h
59E4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_0	4500 59E4h
59E8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_1	4500 59E8h
59ECh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_2	4500 59ECh
59F0h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_L	4500 59F0h
59F4h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_H	4500 59F4h
59F8h	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_L	4500 59F8h
59FCh	32	CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_H	4500 59FCh
5C00h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_CONTROL	4500 5C00h
5C04h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_0	4500 5C04h
5C08h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_1	4500 5C08h
5C0Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_2	4500 5C0Ch
5C10h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_L	4500 5C10h
5C14h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_H	4500 5C14h
5C18h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_L	4500 5C18h
5C1Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_H	4500 5C1Ch
5C20h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_CONTROL	4500 5C20h
5C24h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_0	4500 5C24h
5C28h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_1	4500 5C28h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
5C2Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_2	4500 5C2Ch
5C30h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_L	4500 5C30h
5C34h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_H	4500 5C34h
5C38h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_L	4500 5C38h
5C3Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_H	4500 5C3Ch
5C40h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_CONTROL	4500 5C40h
5C44h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_0	4500 5C44h
5C48h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_1	4500 5C48h
5C4Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_2	4500 5C4Ch
5C50h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_L	4500 5C50h
5C54h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_H	4500 5C54h
5C58h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_L	4500 5C58h
5C5Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_H	4500 5C5Ch
5C60h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_CONTROL	4500 5C60h
5C64h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_0	4500 5C64h
5C68h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_1	4500 5C68h
5C6Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_2	4500 5C6Ch
5C70h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_L	4500 5C70h
5C74h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_H	4500 5C74h
5C78h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_L	4500 5C78h
5C7Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_H	4500 5C7Ch
5C80h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_CONTROL	4500 5C80h
5C84h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_0	4500 5C84h
5C88h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_1	4500 5C88h
5C8Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_2	4500 5C8Ch
5C90h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_L	4500 5C90h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
5C94h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_H	4500 5C94h
5C98h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_L	4500 5C98h
5C9Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_H	4500 5C9Ch
5CA0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_CONTROL	4500 5CA0h
5CA4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_0	4500 5CA4h
5CA8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_1	4500 5CA8h
5CACh	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_2	4500 5CACh
5CB0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_L	4500 5CB0h
5CB4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_H	4500 5CB4h
5CB8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_L	4500 5CB8h
5CBCh	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_H	4500 5CBCh
5CC0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_CONTROL	4500 5CC0h
5CC4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_0	4500 5CC4h
5CC8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_1	4500 5CC8h
5CCCh	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_2	4500 5CCCh
5CD0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_L	4500 5CD0h
5CD4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_H	4500 5CD4h
5CD8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_L	4500 5CD8h
5CDCh	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_H	4500 5CDCh
5CE0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_CONTROL	4500 5CE0h
5CE4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_0	4500 5CE4h
5CE8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_1	4500 5CE8h
5CECh	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_2	4500 5CECh
5CF0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_L	4500 5CF0h
5CF4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_H	4500 5CF4h
5CF8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_L	4500 5CF8h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
5CFCh	32	CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_H	4500 5CFCh
6000h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_CONTROL	4500 6000h
6004h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_0	4500 6004h
6008h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_1	4500 6008h
600Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_2	4500 600Ch
6010h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_L	4500 6010h
6014h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_H	4500 6014h
6018h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_L	4500 6018h
601Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_H	4500 601Ch
6020h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_CONTROL	4500 6020h
6024h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_0	4500 6024h
6028h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_1	4500 6028h
602Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_2	4500 602Ch
6030h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_L	4500 6030h
6034h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_H	4500 6034h
6038h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_L	4500 6038h
603Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_H	4500 603Ch
6040h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_CONTROL	4500 6040h
6044h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_0	4500 6044h
6048h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_1	4500 6048h
604Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_2	4500 604Ch
6050h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_L	4500 6050h
6054h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_H	4500 6054h
6058h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_L	4500 6058h
605Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_H	4500 605Ch
6060h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_CONTROL	4500 6060h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
6064h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_0	4500 6064h
6068h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_1	4500 6068h
606Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_2	4500 606Ch
6070h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_L	4500 6070h
6074h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_H	4500 6074h
6078h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_L	4500 6078h
607Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_H	4500 607Ch
6080h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_CONTROL	4500 6080h
6084h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_0	4500 6084h
6088h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_1	4500 6088h
608Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_2	4500 608Ch
6090h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_L	4500 6090h
6094h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_H	4500 6094h
6098h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_L	4500 6098h
609Ch	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_H	4500 609Ch
60A0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_CONTROL	4500 60A0h
60A4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_0	4500 60A4h
60A8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_1	4500 60A8h
60ACh	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_2	4500 60ACh
60B0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_L	4500 60B0h
60B4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_H	4500 60B4h
60B8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_L	4500 60B8h
60BCh	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_H	4500 60BCh
60C0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_CONTROL	4500 60C0h
60C4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_0	4500 60C4h
60C8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_1	4500 60C8h

Table 14-2. CBASS0_FW Registers, Base Address=4500 0000h, Length=32768 (continued)

Offset	Length	Register Name	CBASS Physical Address
60CCh	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_2	4500 60CCh
60D0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_L	4500 60D0h
60D4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_H	4500 60D4h
60D8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_L	4500 60D8h
60DCh	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_H	4500 60DCh
60E0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_CONTROL	4500 60E0h
60E4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_0	4500 60E4h
60E8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_1	4500 60E8h
60ECh	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_2	4500 60ECh
60F0h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_L	4500 60F0h
60F4h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_H	4500 60F4h
60F8h	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_L	4500 60F8h
60FCh	32	CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_H	4500 60FCh

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536

Offset	Length	Register Name	CBASS Physical Address
400h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL	4588 0400h
410h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L	4588 0410h
414h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H	4588 0414h
418h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L	4588 0418h
41Ch	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H	4588 041Ch
420h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL	4588 0420h
800h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL	4588 0800h
810h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L	4588 0810h
814h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H	4588 0814h
818h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L	4588 0818h
81Ch	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H	4588 081Ch

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
820h	32	CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL	4588 0820h
1000h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_CONTROL	4588 1000h
1010h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_L	4588 1010h
1014h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_H	4588 1014h
1018h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_L	4588 1018h
101Ch	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_H	4588 101Ch
1020h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_DEF_CONTROL	4588 1020h
1400h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_CONTROL	4588 1400h
1410h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_L	4588 1410h
1414h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_H	4588 1414h
1418h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_L	4588 1418h
141Ch	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_H	4588 141Ch
1420h	32	CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_DEF_CONTROL	4588 1420h
2000h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL	4588 2000h
2010h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L	4588 2010h
2014h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H	4588 2014h
2018h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L	4588 2018h
201Ch	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H	4588 201Ch
2020h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL	4588 2020h
2400h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL	4588 2400h
2410h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L	4588 2410h
2414h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H	4588 2414h
2418h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L	4588 2418h
241Ch	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H	4588 241Ch
2420h	32	CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL	4588 2420h
2800h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_CONTROL	4588 2800h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
2810h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L	4588 2810h
2814h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H	4588 2814h
2818h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L	4588 2818h
281Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H	4588 281Ch
2820h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_DEF_CONTROL	4588 2820h
2C00h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_CONTROL	4588 2C00h
2C10h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L	4588 2C10h
2C14h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H	4588 2C14h
2C18h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L	4588 2C18h
2C1Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H	4588 2C1Ch
2C20h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_DEF_CONTROL	4588 2C20h
3C00h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_CONTROL	4588 3C00h
3C10h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L	4588 3C10h
3C14h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H	4588 3C14h
3C18h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L	4588 3C18h
3C1Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H	4588 3C1Ch
3C20h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_DEF_CONTROL	4588 3C20h
4000h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_CONTROL	4588 4000h
4010h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L	4588 4010h
4014h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H	4588 4014h
4018h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L	4588 4018h
401Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H	4588 401Ch
4020h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_DEF_CONTROL	4588 4020h
5000h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_CONTROL	4588 5000h
5010h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L	4588 5010h
5014h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H	4588 5014h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
5018h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L	4588 5018h
501Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H	4588 501Ch
5020h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_DEF_CONTROL	4588 5020h
5400h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_CONTROL	4588 5400h
5410h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L	4588 5410h
5414h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H	4588 5414h
5418h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L	4588 5418h
541Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H	4588 541Ch
5420h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_DEF_CONTROL	4588 5420h
6400h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_CONTROL	4588 6400h
6410h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L	4588 6410h
6414h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H	4588 6414h
6418h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L	4588 6418h
641Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H	4588 641Ch
6420h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_DEF_CONTROL	4588 6420h
6800h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_CONTROL	4588 6800h
6810h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L	4588 6810h
6814h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H	4588 6814h
6818h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L	4588 6818h
681Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H	4588 681Ch
6820h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_DEF_CONTROL	4588 6820h
7800h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL	4588 7800h
7810h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L	4588 7810h
7814h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H	4588 7814h
7818h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L	4588 7818h
781Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H	4588 781Ch

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
7820h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL	4588 7820h
7830h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L	4588 7830h
7834h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H	4588 7834h
7838h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L	4588 7838h
783Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H	4588 783Ch
7840h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL	4588 7840h
7850h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L	4588 7850h
7854h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H	4588 7854h
7858h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L	4588 7858h
785Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H	4588 785Ch
7860h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL	4588 7860h
7870h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L	4588 7870h
7874h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H	4588 7874h
7878h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L	4588 7878h
787Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H	4588 787Ch
7880h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL	4588 7880h
7890h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L	4588 7890h
7894h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H	4588 7894h
7898h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L	4588 7898h
789Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H	4588 789Ch
78A0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL	4588 78A0h
78B0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L	4588 78B0h
78B4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H	4588 78B4h
78B8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L	4588 78B8h
78BCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H	4588 78BCh
78C0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL	4588 78C0h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
78D0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L	4588 78D0h
78D4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H	4588 78D4h
78D8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L	4588 78D8h
78DCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H	4588 78DCh
78E0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL	4588 78E0h
78F0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L	4588 78F0h
78F4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H	4588 78F4h
78F8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L	4588 78F8h
78FCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H	4588 78FCh
7900h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL	4588 7900h
7910h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L	4588 7910h
7914h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H	4588 7914h
7918h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L	4588 7918h
791Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H	4588 791Ch
7920h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL	4588 7920h
7930h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L	4588 7930h
7934h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H	4588 7934h
7938h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L	4588 7938h
793Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H	4588 793Ch
7940h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL	4588 7940h
7950h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L	4588 7950h
7954h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H	4588 7954h
7958h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L	4588 7958h
795Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H	4588 795Ch
7960h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL	4588 7960h
7970h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L	4588 7970h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
7974h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H	4588 7974h
7978h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L	4588 7978h
797Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H	4588 797Ch
7980h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL	4588 7980h
7990h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L	4588 7990h
7994h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H	4588 7994h
7998h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L	4588 7998h
799Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H	4588 799Ch
79A0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL	4588 79A0h
79B0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L	4588 79B0h
79B4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H	4588 79B4h
79B8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L	4588 79B8h
79BCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H	4588 79BCh
79C0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL	4588 79C0h
79D0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L	4588 79D0h
79D4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H	4588 79D4h
79D8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L	4588 79D8h
79DCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H	4588 79DCh
79E0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL	4588 79E0h
79F0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L	4588 79F0h
79F4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H	4588 79F4h
79F8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L	4588 79F8h
79FCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H	4588 79FCh
7A00h	32	CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL	4588 7A00h
7C00h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL	4588 7C00h
7C10h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L	4588 7C10h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
7C14h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H	4588 7C14h
7C18h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L	4588 7C18h
7C1Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H	4588 7C1Ch
7C20h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL	4588 7C20h
7C30h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L	4588 7C30h
7C34h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H	4588 7C34h
7C38h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L	4588 7C38h
7C3Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H	4588 7C3Ch
7C40h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL	4588 7C40h
7C50h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L	4588 7C50h
7C54h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H	4588 7C54h
7C58h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L	4588 7C58h
7C5Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H	4588 7C5Ch
7C60h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL	4588 7C60h
7C70h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L	4588 7C70h
7C74h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H	4588 7C74h
7C78h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L	4588 7C78h
7C7Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H	4588 7C7Ch
7C80h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL	4588 7C80h
7C90h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L	4588 7C90h
7C94h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H	4588 7C94h
7C98h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L	4588 7C98h
7C9Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H	4588 7C9Ch
7CA0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL	4588 7CA0h
7CB0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L	4588 7CB0h
7CB4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H	4588 7CB4h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
7CB8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L	4588 7CB8h
7CBCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H	4588 7CBCh
7CC0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL	4588 7CC0h
7CD0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L	4588 7CD0h
7CD4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H	4588 7CD4h
7CD8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L	4588 7CD8h
7CDCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H	4588 7CDCh
7CE0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL	4588 7CE0h
7CF0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L	4588 7CF0h
7CF4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H	4588 7CF4h
7CF8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L	4588 7CF8h
7CFCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H	4588 7CFCh
7D00h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL	4588 7D00h
7D10h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L	4588 7D10h
7D14h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H	4588 7D14h
7D18h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L	4588 7D18h
7D1Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H	4588 7D1Ch
7D20h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL	4588 7D20h
7D30h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L	4588 7D30h
7D34h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H	4588 7D34h
7D38h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L	4588 7D38h
7D3Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H	4588 7D3Ch
7D40h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL	4588 7D40h
7D50h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L	4588 7D50h
7D54h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H	4588 7D54h
7D58h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L	4588 7D58h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
7D5Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H	4588 7D5Ch
7D60h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL	4588 7D60h
7D70h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L	4588 7D70h
7D74h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H	4588 7D74h
7D78h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L	4588 7D78h
7D7Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H	4588 7D7Ch
7D80h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL	4588 7D80h
7D90h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L	4588 7D90h
7D94h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H	4588 7D94h
7D98h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L	4588 7D98h
7D9Ch	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H	4588 7D9Ch
7DA0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL	4588 7DA0h
7DB0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L	4588 7DB0h
7DB4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H	4588 7DB4h
7DB8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L	4588 7DB8h
7DBCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H	4588 7DBCh
7DC0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL	4588 7DC0h
7DD0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L	4588 7DD0h
7DD4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H	4588 7DD4h
7DD8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L	4588 7DD8h
7DDCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H	4588 7DDCh
7DE0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL	4588 7DE0h
7DF0h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L	4588 7DF0h
7DF4h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H	4588 7DF4h
7DF8h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L	4588 7DF8h
7DFCh	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H	4588 7DFCh

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
7E00h	32	CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL	4588 7E00h
8000h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_CONTROL	4588 8000h
8010h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_L	4588 8010h
8014h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_H	4588 8014h
8018h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_L	4588 8018h
801Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_H	4588 801Ch
8020h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_CONTROL	4588 8020h
8030h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_L	4588 8030h
8034h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_H	4588 8034h
8038h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_L	4588 8038h
803Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_H	4588 803Ch
8040h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_CONTROL	4588 8040h
8050h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_L	4588 8050h
8054h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_H	4588 8054h
8058h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_L	4588 8058h
805Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_H	4588 805Ch
8060h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_CONTROL	4588 8060h
8070h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_L	4588 8070h
8074h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_H	4588 8074h
8078h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_L	4588 8078h
807Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_H	4588 807Ch
8080h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_CONTROL	4588 8080h
8090h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_L	4588 8090h
8094h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_H	4588 8094h
8098h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_L	4588 8098h
809Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_H	4588 809Ch

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
80A0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_CONTROL	4588 80A0h
80B0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_L	4588 80B0h
80B4h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_H	4588 80B4h
80B8h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_L	4588 80B8h
80BCh	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_H	4588 80BCh
80C0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_CONTROL	4588 80C0h
80D0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_L	4588 80D0h
80D4h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_H	4588 80D4h
80D8h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_L	4588 80D8h
80DCh	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_H	4588 80DCh
80E0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_CONTROL	4588 80E0h
80F0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_L	4588 80F0h
80F4h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_H	4588 80F4h
80F8h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_L	4588 80F8h
80FCh	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_H	4588 80FCh
8100h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_DEF_CONTROL	4588 8100h
8400h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_CONTROL	4588 8400h
8410h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_L	4588 8410h
8414h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_H	4588 8414h
8418h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_L	4588 8418h
841Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_H	4588 841Ch
8420h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_CONTROL	4588 8420h
8430h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_L	4588 8430h
8434h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_H	4588 8434h
8438h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_L	4588 8438h
843Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_H	4588 843Ch

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
8440h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_CONTROL	4588 8440h
8450h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_L	4588 8450h
8454h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_H	4588 8454h
8458h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_L	4588 8458h
845Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_H	4588 845Ch
8460h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_CONTROL	4588 8460h
8470h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_L	4588 8470h
8474h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_H	4588 8474h
8478h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_L	4588 8478h
847Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_H	4588 847Ch
8480h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_CONTROL	4588 8480h
8490h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_L	4588 8490h
8494h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_H	4588 8494h
8498h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_L	4588 8498h
849Ch	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_H	4588 849Ch
84A0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_CONTROL	4588 84A0h
84B0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_L	4588 84B0h
84B4h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_H	4588 84B4h
84B8h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_L	4588 84B8h
84BCh	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_H	4588 84BCh
84C0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_CONTROL	4588 84C0h
84D0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_L	4588 84D0h
84D4h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_H	4588 84D4h
84D8h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_L	4588 84D8h
84DCh	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_H	4588 84DCh
84E0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_CONTROL	4588 84E0h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
84F0h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_L	4588 84F0h
84F4h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_H	4588 84F4h
84F8h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_L	4588 84F8h
84FCh	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_H	4588 84FCh
8500h	32	CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_DEF_CONTROL	4588 8500h
8800h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL	4588 8800h
8810h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L	4588 8810h
8814h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H	4588 8814h
8818h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L	4588 8818h
881Ch	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H	4588 881Ch
8820h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL	4588 8820h
8C00h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL	4588 8C00h
8C10h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L	4588 8C10h
8C14h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H	4588 8C14h
8C18h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L	4588 8C18h
8C1Ch	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H	4588 8C1Ch
8C20h	32	CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL	4588 8C20h
9000h	32	CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL	4588 9000h
9010h	32	CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L	4588 9010h
9014h	32	CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H	4588 9014h
9018h	32	CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L	4588 9018h
901Ch	32	CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H	4588 901Ch
9020h	32	CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL	4588 9020h
9400h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL	4588 9400h
9410h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L	4588 9410h
9414h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H	4588 9414h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
9418h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L	4588 9418h
941Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H	4588 941Ch
9420h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_CONTROL	4588 9420h
9430h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_L	4588 9430h
9434h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_H	4588 9434h
9438h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_L	4588 9438h
943Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_H	4588 943Ch
9440h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_CONTROL	4588 9440h
9450h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_L	4588 9450h
9454h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_H	4588 9454h
9458h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_L	4588 9458h
945Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_H	4588 945Ch
9460h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_CONTROL	4588 9460h
9470h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_L	4588 9470h
9474h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_H	4588 9474h
9478h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_L	4588 9478h
947Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_H	4588 947Ch
9480h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_CONTROL	4588 9480h
9490h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_L	4588 9490h
9494h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_H	4588 9494h
9498h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_L	4588 9498h
949Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_H	4588 949Ch
94A0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_CONTROL	4588 94A0h
94B0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_L	4588 94B0h
94B4h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_H	4588 94B4h
94B8h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_L	4588 94B8h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
94BCh	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_H	4588 94BCh
94C0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_CONTROL	4588 94C0h
94D0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_L	4588 94D0h
94D4h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_H	4588 94D4h
94D8h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_L	4588 94D8h
94DCh	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_H	4588 94DCh
94E0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_CONTROL	4588 94E0h
94F0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_L	4588 94F0h
94F4h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_H	4588 94F4h
94F8h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_L	4588 94F8h
94FCh	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_H	4588 94FCh
9500h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL	4588 9500h
9800h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL	4588 9800h
9810h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L	4588 9810h
9814h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H	4588 9814h
9818h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L	4588 9818h
981Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H	4588 981Ch
9820h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_CONTROL	4588 9820h
9830h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_L	4588 9830h
9834h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_H	4588 9834h
9838h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_L	4588 9838h
983Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_H	4588 983Ch
9840h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_CONTROL	4588 9840h
9850h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_L	4588 9850h
9854h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_H	4588 9854h
9858h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_L	4588 9858h

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
985Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_H	4588 985Ch
9860h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_CONTROL	4588 9860h
9870h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_L	4588 9870h
9874h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_H	4588 9874h
9878h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_L	4588 9878h
987Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_H	4588 987Ch
9880h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_CONTROL	4588 9880h
9890h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_L	4588 9890h
9894h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_H	4588 9894h
9898h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_L	4588 9898h
989Ch	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_H	4588 989Ch
98A0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_CONTROL	4588 98A0h
98B0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_L	4588 98B0h
98B4h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_H	4588 98B4h
98B8h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_L	4588 98B8h
98BCh	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_H	4588 98BCh
98C0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_CONTROL	4588 98C0h
98D0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_L	4588 98D0h
98D4h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_H	4588 98D4h
98D8h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_L	4588 98D8h
98DCh	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_H	4588 98DCh
98E0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_CONTROL	4588 98E0h
98F0h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_L	4588 98F0h
98F4h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_H	4588 98F4h
98F8h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_L	4588 98F8h
98FCh	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_H	4588 98FCh

Table 14-3. CBASS0_ISC Registers, Base Address=4588 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
9900h	32	CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL	4588 9900h
9C00h	32	CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_CONTROL	4588 9C00h
9C10h	32	CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L	4588 9C10h
9C14h	32	CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H	4588 9C14h
9C18h	32	CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L	4588 9C18h
9C1Ch	32	CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H	4588 9C1Ch
9C20h	32	CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL	4588 9C20h
A000h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL	4588 A000h
A010h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L	4588 A010h
A014h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H	4588 A014h
A018h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L	4588 A018h
A01Ch	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H	4588 A01Ch
A020h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL	4588 A020h
A400h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL	4588 A400h
A410h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L	4588 A410h
A414h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H	4588 A414h
A418h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L	4588 A418h
A41Ch	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H	4588 A41Ch
A420h	32	CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL	4588 A420h

Table 14-4. CBASS0_GLB Registers, Base Address=45B0 8000h, Length=1024

Offset	Length	Register Name	CBASS Physical Address
0h	32	CBASS_GLB_PID	45B0 8000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 8004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 8020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 8024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 8028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 802Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 8030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 8034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 8038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 8040h

Table 14-4. CBASS0_GLB Registers, Base Address=45B0 8000h, Length=1024 (continued)

Offset	Length	Register Name	CBASS Physical Address
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 8044h

Table 14-5. CBASS0_QOS Registers, Base Address=45D8 0000h, Length=65536

Offset	Length	Register Name	CBASS Physical Address
500h	32	CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_MAP0	45D8 0500h
900h	32	CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_MAP0	45D8 0900h
1100h	32	CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_MAP0	45D8 1100h
1500h	32	CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_MAP0	45D8 1500h
2100h	32	CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_MAP0	45D8 2100h
2500h	32	CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_MAP0	45D8 2500h
2900h	32	CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_RMST_MAP0	45D8 2900h
2D00h	32	CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_WMST_MAP0	45D8 2D00h
3D00h	32	CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_RMST_MAP0	45D8 3D00h
4100h	32	CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_WMST_MAP0	45D8 4100h
5100h	32	CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_RMST_MAP0	45D8 5100h
5500h	32	CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_WMST_MAP0	45D8 5500h
6500h	32	CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_RMST_MAP0	45D8 6500h
6900h	32	CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_WMST_MAP0	45D8 6900h
7900h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP0	45D8 7900h
7904h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP1	45D8 7904h
7908h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP2	45D8 7908h
790Ch	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP3	45D8 790Ch
7910h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP4	45D8 7910h
7914h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP5	45D8 7914h
7918h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP6	45D8 7918h
791Ch	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP7	45D8 791Ch
7920h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP8	45D8 7920h
7924h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP9	45D8 7924h
7928h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP10	45D8 7928h
792Ch	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP11	45D8 792Ch
7930h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP12	45D8 7930h
7934h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP13	45D8 7934h
7938h	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP14	45D8 7938h
793Ch	32	CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP15	45D8 793Ch
7D00h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP0	45D8 7D00h
7D04h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP1	45D8 7D04h
7D08h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP2	45D8 7D08h
7D0Ch	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP3	45D8 7D0Ch
7D10h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP4	45D8 7D10h
7D14h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP5	45D8 7D14h
7D18h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP6	45D8 7D18h
7D1Ch	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP7	45D8 7D1Ch
7D20h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP8	45D8 7D20h

Table 14-5. CBASS0_QOS Registers, Base Address=45D8 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS Physical Address
7D24h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP9	45D8 7D24h
7D28h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP10	45D8 7D28h
7D2Ch	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP11	45D8 7D2Ch
7D30h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP12	45D8 7D30h
7D34h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP13	45D8 7D34h
7D38h	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP14	45D8 7D38h
7D3Ch	32	CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP15	45D8 7D3Ch
8100h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP0	45D8 8100h
8104h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP1	45D8 8104h
8108h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP2	45D8 8108h
810Ch	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP3	45D8 810Ch
8110h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP4	45D8 8110h
8114h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP5	45D8 8114h
8118h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP6	45D8 8118h
811Ch	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP7	45D8 811Ch
8500h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP0	45D8 8500h
8504h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP1	45D8 8504h
8508h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP2	45D8 8508h
850Ch	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP3	45D8 850Ch
8510h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP4	45D8 8510h
8514h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP5	45D8 8514h
8518h	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP6	45D8 8518h
851Ch	32	CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP7	45D8 851Ch
8900h	32	CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0	45D8 8900h
8D00h	32	CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0	45D8 8D00h
9100h	32	CBASS_QOS_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_MAP0	45D8 9100h
9500h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP0	45D8 9500h
9504h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP1	45D8 9504h
9508h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP2	45D8 9508h
950Ch	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP3	45D8 950Ch
9510h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP4	45D8 9510h
9514h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP5	45D8 9514h
9518h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP6	45D8 9518h
951Ch	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP7	45D8 951Ch
9900h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP0	45D8 9900h
9904h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP1	45D8 9904h
9908h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP2	45D8 9908h
990Ch	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP3	45D8 990Ch
9910h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP4	45D8 9910h
9914h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP5	45D8 9914h
9918h	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP6	45D8 9918h
991Ch	32	CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP7	45D8 991Ch
A100h	32	CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0	45D8 A100h
A500h	32	CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0	45D8 A500h

14.1.1.2 CBASS_ERR_PID Register

CBASS_ERR_PID Register (Offset = 0h) [reset = 6600A901h]

Register Description: The Revision Register contains the major and minor revisions for the module.

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Table 14-6. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0000h

Figure 14-1. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
15h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-8. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
15:11	RTL	R	15h	RTL revision. Will vary depending on release. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.3 CBASS_ERR_DESTINATION_ID Register

CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

Register Description: The Destination ID Register defines the destination ID value for error messages.

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Table 14-9. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0004h

Figure 14-2. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-11. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

Register Description: The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-12. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0024h

Figure 14-3. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-14. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.5 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

Register Description: The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-15. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0028h

Figure 14-4. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.1.6 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

Register Description: The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-18. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 002Ch

Figure 14-5. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-20. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.7 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

Register Description: The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-21. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0030h

Figure 14-6. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-23. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.8 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

Register Description: The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-24. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0034h

Figure 14-7. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-26. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

Table 14-26. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.9 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

Register Description: The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-27. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0038h

Figure 14-8. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.10 CBASS_ERR_ERR_INTR_RAW_STAT Register

CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

Register Description: Global Interrupt Raw Status Register

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Table 14-30. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0050h

Figure 14-9. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-32. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.11 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

Register Description: Global Interrupt Enabled Status Register

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Table 14-33. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0054h

Figure 14-10. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-35. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.12 CBASS_ERR_ERR_INTR_ENABLE_SET Register

CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Register Description: Interrupt Enable Set Register

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Table 14-36. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0058h

Figure 14-11. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-38. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.13 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Register Description: Interrupt Enable Clear Register

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Table 14-39. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 005Ch

Figure 14-12. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-41. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.14 CBASS_ERR_EOI Register

CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Register Description: EOI Register

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Table 14-42. Instance Table

Instance Name	Physical Address
CBASS0_ERR	3A00 0060h

Figure 14-13. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-44. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register Reset Source: SCRM_128b_clk2_rst_mod_g_rst_n

14.1.1.15 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL Register (Offset = 400h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Isam64_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-45. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0400h

Figure 14-14. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-47. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.16 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Register (Offset = 404h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-48. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0404h

Figure 14-15. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-50. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-50. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.17 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Register (Offset = 408h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-51. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0408h

Figure 14-16. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-53. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-53. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.18 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Register (Offset = 40Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-54. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 040Ch

Figure 14-17. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-56. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-56. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.19 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 80000000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-57. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0410h

Figure 14-18. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">80000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">80000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">80000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-59. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	80000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.20 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-60. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0414h

Figure 14-19. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-62. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.21 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = 7FFFFFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-63. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0418h

Figure 14-20. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7FFFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7FFFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7FFFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-65. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7FFFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.22 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 2h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 0 firewall.

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Table 14-66. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 041Ch

Figure 14-21. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
2h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
2h							

Table 14-68. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	2h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.23 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL Register (Offset = 420h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Isam64_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-69. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0420h

Figure 14-22. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-71. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.24 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Register (Offset = 424h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-72. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0424h

Figure 14-23. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-74. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-74. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.25 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Register (Offset = 428h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-75. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0428h

Figure 14-24. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-77. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-77. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.26 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Register (Offset = 42Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-78. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 042Ch

Figure 14-25. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-80. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-80. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.27 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-81. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0430h

Figure 14-26. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-83. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.28 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-84. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0434h

Figure 14-27. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-86. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.29 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-87. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0438h

Figure 14-28. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-89. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.30 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 1 firewall.

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Table 14-90. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 043Ch

Figure 14-29. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-92. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.31 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL Register (Offset = 440h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Isam64_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-93. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0440h

Figure 14-30. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-95. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.32 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Register (Offset = 444h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-96. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0444h

Figure 14-31. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-98. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-98. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.33 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Register (Offset = 448h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-99. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0448h

Figure 14-32. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-101. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-101. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.34 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Register (Offset = 44Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-102. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 044Ch

Figure 14-33. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-104. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-104. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.35 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-105. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0450h

Figure 14-34. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-107. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.36 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-108. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0454h

Figure 14-35. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-110. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.37 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-111. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0458h

Figure 14-36. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-113. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.38 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 2 firewall.

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Table 14-114. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 045Ch

Figure 14-37. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-116. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.39 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL Register (Offset = 460h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Isam64_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-117. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0460h

Figure 14-38. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-119. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.40 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Register (Offset = 464h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-120. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0464h

Figure 14-39. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-122. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-122. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.41 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Register (Offset = 468h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-123. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0468h

Figure 14-40. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-125. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-125. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.42 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Register (Offset = 46Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-126. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 046Ch

Figure 14-41. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-128. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-128. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.43 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-129. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0470h

Figure 14-42. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-131. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.44 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-132. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0474h

Figure 14-43. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-134. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.45 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-135. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0478h

Figure 14-44. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-137. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.46 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 3 firewall.

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Table 14-138. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 047Ch

Figure 14-45. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-140. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.47 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL Register (Offset = 480h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave Isam64_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-141. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0480h

Figure 14-46. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-143. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.48 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Register (Offset = 484h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-144. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0484h

Figure 14-47. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-146. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-146. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.49 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Register (Offset = 488h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-147. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0488h

Figure 14-48. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-149. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-149. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.50 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Register (Offset = 48Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-150. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 048Ch

Figure 14-49. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-152. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-152. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.51 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L Register (Offset = 490h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-153. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0490h

Figure 14-50. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-155. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.52 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H Register (Offset = 494h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-156. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0494h

Figure 14-51. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-158. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.53 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L Register (Offset = 498h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-159. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0498h

Figure 14-52. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-161. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.54 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H Register (Offset = 49Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 4 firewall.

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Table 14-162. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 049Ch

Figure 14-53. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-164. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.55 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL Register (Offset = 4A0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave Isam64_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-165. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04A0h

Figure 14-54. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-167. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.56 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Register (Offset = 4A4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-168. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04A4h

Figure 14-55. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-170. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-170. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.57 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Register (Offset = 4A8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-171. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04A8h

Figure 14-56. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-173. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-173. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.58 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Register (Offset = 4ACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-174. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04ACh

Figure 14-57. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-176. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-176. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.59 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L Register (Offset = 4B0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-177. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04B0h

Figure 14-58. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-179. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.60 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H Register (Offset = 4B4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-180. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04B4h

Figure 14-59. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-182. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.61 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L Register (Offset = 4B8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-183. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04B8h

Figure 14-60. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-185. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.62 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H Register (Offset = 4BCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 5 firewall.

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Table 14-186. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04BCh

Figure 14-61. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-188. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.63 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL Register (Offset = 4C0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave Isam64_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-189. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04C0h

Figure 14-62. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-191. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.64 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Register (Offset = 4C4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-192. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04C4h

Figure 14-63. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-194. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-194. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.65 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Register (Offset = 4C8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-195. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04C8h

Figure 14-64. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-197. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-197. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.66 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Register (Offset = 4CCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-198. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04CCh

Figure 14-65. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-200. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-200. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.67 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L Register (Offset = 4D0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-201. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04D0h

Figure 14-66. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-203. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.68 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H Register (Offset = 4D4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-204. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04D4h

Figure 14-67. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-206. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.69 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L Register (Offset = 4D8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-207. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04D8h

Figure 14-68. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-209. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.70 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H Register (Offset = 4DCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 6 firewall.

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Table 14-210. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04DCh

Figure 14-69. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-212. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.71 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL Register (Offset = 4E0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave Isam64_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-213. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04E0h

Figure 14-70. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-215. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.72 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Register (Offset = 4E4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-216. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04E4h

Figure 14-71. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-218. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-218. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.73 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Register (Offset = 4E8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-219. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04E8h

Figure 14-72. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-221. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-221. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.74 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Register (Offset = 4ECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave Isam64_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-222. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04ECh

Figure 14-73. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-224. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-224. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.75 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L Register (Offset = 4F0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-225. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04F0h

Figure 14-74. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-227. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.76 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H Register (Offset = 4F4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-228. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04F4h

Figure 14-75. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-230. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.77 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L Register (Offset = 4F8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-231. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04F8h

Figure 14-76. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-233. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.78 CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H Register (Offset = 4FCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_ddr_wrap_main_0.ddrss region 7 firewall.

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Table 14-234. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 04FCh

Figure 14-77. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-236. CBASS_FW_ISAM64_DDR_WRAP_MAIN_0_DDRSS_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.79 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Register (Offset = 800h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 0 firewall.

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Table 14-237. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0800h

Figure 14-78. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-239. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-239. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.80 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Register (Offset = 804h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 0 firewall.

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Table 14-240. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0804h

Figure 14-79. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-242. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-242. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.81 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Register (Offset = 808h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 0 firewall.

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Table 14-243. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0808h

Figure 14-80. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-245. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-245. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.82 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Register (Offset = 80Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 0 firewall.

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Table 14-246. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 080Ch

Figure 14-81. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-248. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-248. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.83 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 0 firewall.

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Table 14-249. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0810h

Figure 14-82. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-251. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.84 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 0 firewall.

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Table 14-252. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0814h

Figure 14-83. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-254. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.85 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFFFFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 0 firewall.

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Table 14-255. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0818h

Figure 14-84. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
FFFFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
FFFFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
FFFFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-257. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	FFFFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.86 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = Fh]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 0 firewall.

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Table 14-258. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 081Ch

Figure 14-85. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
Fh							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
Fh							

Table 14-260. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	Fh	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.87 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Register (Offset = 820h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 1 firewall.

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Table 14-261. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0820h

Figure 14-86. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-263. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-263. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.88 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Register (Offset = 824h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 1 firewall.

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Table 14-264. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0824h

Figure 14-87. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-266. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-266. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.89 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Register (Offset = 828h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 1 firewall.

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Table 14-267. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0828h

Figure 14-88. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-269. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-269. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.90 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Register (Offset = 82Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 1 firewall.

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Table 14-270. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 082Ch

Figure 14-89. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-272. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-272. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.91 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 1 firewall.

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Table 14-273. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0830h

Figure 14-90. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-275. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.92 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 1 firewall.

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Table 14-276. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0834h

Figure 14-91. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-278. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.93 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 1 firewall.

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Table 14-279. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0838h

Figure 14-92. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-281. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.94

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 1 firewall.

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Table 14-282. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 083Ch

Figure 14-93. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-284. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.95 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Register (Offset = 840h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 2 firewall.

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Table 14-285. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0840h

Figure 14-94. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-287. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-287. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.96 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Register (Offset = 844h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 2 firewall.

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Table 14-288. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0844h

Figure 14-95. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-290. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-290. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.97 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Register (Offset = 848h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 2 firewall.

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Table 14-291. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0848h

Figure 14-96. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-293. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-293. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.98 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Register (Offset = 84Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 2 firewall.

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Table 14-294. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 084Ch

Figure 14-97. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-296. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-296. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

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CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 2 firewall.

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Table 14-297. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0850h

Figure 14-98. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-299. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.100 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 2 firewall.

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Table 14-300. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0854h

Figure 14-99. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-302. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.101 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 2 firewall.

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Table 14-303. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0858h

Figure 14-100. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-305. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.102 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 2 firewall.

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Table 14-306. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 085Ch

Figure 14-101. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-308. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.103 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Register (Offset = 860h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 3 firewall.

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Table 14-309. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0860h

Figure 14-102. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-311. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-311. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.104 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Register (Offset = 864h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 3 firewall.

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Table 14-312. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0864h

Figure 14-103. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-314. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-314. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.105 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Register (Offset = 868h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 3 firewall.

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Table 14-315. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0868h

Figure 14-104. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-317. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-317. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.106 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Register (Offset = 86Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 3 firewall.

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Table 14-318. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 086Ch

Figure 14-105. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-320. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-320. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.107

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 3 firewall.

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Table 14-321. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0870h

Figure 14-106. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-323. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.108 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 3 firewall.

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Table 14-324. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0874h

Figure 14-107. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-326. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.109
CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 3 firewall.

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Table 14-327. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0878h

Figure 14-108. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-329. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.110 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 3 firewall.

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Table 14-330. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 087Ch

Figure 14-109. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-332. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.111 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Register (Offset = 880h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 4 firewall.

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Table 14-333. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0880h

Figure 14-110. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-335. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-335. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.112 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Register (Offset = 884h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 4 firewall.

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Table 14-336. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0884h

Figure 14-111. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-338. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-338. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.113 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Register (Offset = 888h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 4 firewall.

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Table 14-339. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0888h

Figure 14-112. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-341. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-341. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.114 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Register (Offset = 88Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 4 firewall.

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Table 14-342. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 088Ch

Figure 14-113. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-344. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-344. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.115 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L Register (Offset = 890h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 4 firewall.

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Table 14-345. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0890h

Figure 14-114. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-347. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.116 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H Register (Offset = 894h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 4 firewall.

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Table 14-348. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0894h

Figure 14-115. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-350. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.117 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L Register (Offset = 898h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 4 firewall.

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Table 14-351. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 0898h

Figure 14-116. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-353. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.118 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H Register (Offset = 89Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 4 firewall.

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Table 14-354. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 089Ch

Figure 14-117. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-356. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.119 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Register (Offset = 8A0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 5 firewall.

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Table 14-357. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08A0h

Figure 14-118. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-359. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-359. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.120 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Register (Offset = 8A4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 5 firewall.

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Table 14-360. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08A4h

Figure 14-119. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-362. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-362. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.121 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Register (Offset = 8A8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 5 firewall.

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Table 14-363. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08A8h

Figure 14-120. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-365. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-365. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.122
CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Register (Offset = 8ACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 5 firewall.

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Table 14-366. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08ACh

Figure 14-121. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-368. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-368. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.123 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L Register (Offset = 8B0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 5 firewall.

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Table 14-369. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08B0h

Figure 14-122. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-371. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.124 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H Register (Offset = 8B4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 5 firewall.

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Table 14-372. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08B4h

Figure 14-123. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-374. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.125 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L Register (Offset = 8B8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 5 firewall.

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Table 14-375. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08B8h

Figure 14-124. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-377. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.126 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H Register (Offset = 8BCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 5 firewall.

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Table 14-378. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08BCh

Figure 14-125. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-380. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.127 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Register (Offset = 8C0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 6 firewall.

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Table 14-381. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08C0h

Figure 14-126. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-383. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-383. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.128 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Register (Offset = 8C4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 6 firewall.

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Table 14-384. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08C4h

Figure 14-127. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-386. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-386. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.129 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Register (Offset = 8C8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 6 firewall.

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Table 14-387. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08C8h

Figure 14-128. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-389. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-389. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.130 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Register (Offset = 8CCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 6 firewall.

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Table 14-390. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08CCh

Figure 14-129. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-392. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-392. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.131 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L Register (Offset = 8D0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 6 firewall.

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Table 14-393. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08D0h

Figure 14-130. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-395. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.132 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H Register (Offset = 8D4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 6 firewall.

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Table 14-396. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08D4h

Figure 14-131. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-398. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.133 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L Register (Offset = 8D8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 6 firewall.

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Table 14-399. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08D8h

Figure 14-132. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-401. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.134 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H Register (Offset = 8DCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 6 firewall.

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Table 14-402. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08DCh

Figure 14-133. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-404. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.135 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Register (Offset = 8E0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 7 firewall.

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Table 14-405. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08E0h

Figure 14-134. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-407. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-407. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.136 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Register (Offset = 8E4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 7 firewall.

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Table 14-408. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08E4h

Figure 14-135. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-410. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-410. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.137 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Register (Offset = 8E8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 7 firewall.

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Table 14-411. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08E8h

Figure 14-136. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-413. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-413. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.138 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Register (Offset = 8ECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 7 firewall.

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Table 14-414. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08ECh

Figure 14-137. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-416. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-416. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.139 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L Register (Offset = 8F0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 7 firewall.

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Table 14-417. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08F0h

Figure 14-138. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-419. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.140 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H Register (Offset = 8F4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 7 firewall.

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Table 14-420. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08F4h

Figure 14-139. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-422. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.141 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L Register (Offset = 8F8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 7 firewall.

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Table 14-423. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08F8h

Figure 14-140. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-425. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.142 CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H Register (Offset = 8FCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_acp_w region 7 firewall.

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Table 14-426. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 08FCh

Figure 14-141. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-428. CBASS_FW_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_ACP_W_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.143 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_CONTROL Register (Offset = 3800h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Imsram32kx64e_main_0.slv region 0 firewall.

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Table 14-429. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3800h

Figure 14-142. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-431. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.144 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 3804h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 0 firewall.

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Table 14-432. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3804h

Figure 14-143. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-434. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-434. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.145 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 3808h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 0 firewall.

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Table 14-435. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3808h

Figure 14-144. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-437. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-437. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.146 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 380Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 0 firewall.

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Table 14-438. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 380Ch

Figure 14-145. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-440. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-440. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.147 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 3810h) [reset = 70000000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_0.slv region 0 firewall.

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Table 14-441. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3810h

Figure 14-146. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
70000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
70000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
70000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-443. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	70000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.148 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 3814h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_0.slv region 0 firewall.

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Table 14-444. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3814h

Figure 14-147. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-446. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.149 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 3818h) [reset = 7003FFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_0.slv region 0 firewall.

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Table 14-447. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3818h

Figure 14-148. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7003Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7003Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7003Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-449. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7003Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.150 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 381Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_0.slv region 0 firewall.

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Table 14-450. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 381Ch

Figure 14-149. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-452. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.151 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_CONTROL Register (Offset = 3820h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Imsram32kx64e_main_0.slv region 1 firewall.

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Table 14-453. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3820h

Figure 14-150. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-455. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.152 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 3824h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 1 firewall.

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Table 14-456. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3824h

Figure 14-151. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-458. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-458. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.153 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 3828h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 1 firewall.

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Table 14-459. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3828h

Figure 14-152. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-461. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-461. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.154 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 382Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 1 firewall.

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Table 14-462. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 382Ch

Figure 14-153. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-464. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-464. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.155 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 3830h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_0.slv region 1 firewall.

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Table 14-465. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3830h

Figure 14-154. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-467. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.156 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 3834h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_0.slv region 1 firewall.

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Table 14-468. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3834h

Figure 14-155. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-470. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.157 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 3838h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_0.slv region 1 firewall.

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Table 14-471. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3838h

Figure 14-156. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-473. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.158 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 383Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_0.slv region 1 firewall.

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Table 14-474. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 383Ch

Figure 14-157. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-476. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.159 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_CONTROL Register (Offset = 3840h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Imsram32kx64e_main_0.slv region 2 firewall.

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Table 14-477. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3840h

Figure 14-158. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-479. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.160 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 3844h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 2 firewall.

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Table 14-480. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3844h

Figure 14-159. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-482. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-482. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.161 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 3848h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 2 firewall.

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Table 14-483. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3848h

Figure 14-160. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-485. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-485. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.162 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 384Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 2 firewall.

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Table 14-486. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 384Ch

Figure 14-161. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-488. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-488. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.163 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 3850h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_0.slv region 2 firewall.

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Table 14-489. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3850h

Figure 14-162. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-491. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.164 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 3854h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_0.slv region 2 firewall.

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Table 14-492. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3854h

Figure 14-163. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-494. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.165 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 3858h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_0.slv region 2 firewall.

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Table 14-495. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3858h

Figure 14-164. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-497. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.166 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 385Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_0.slv region 2 firewall.

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Table 14-498. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 385Ch

Figure 14-165. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-500. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.167 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_CONTROL Register (Offset = 3860h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Imsram32kx64e_main_0.slv region 3 firewall.

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Table 14-501. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3860h

Figure 14-166. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-503. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.168 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 3864h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 3 firewall.

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Table 14-504. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3864h

Figure 14-167. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-506. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-506. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.169 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 3868h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 3 firewall.

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Table 14-507. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3868h

Figure 14-168. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-509. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-509. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.170 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 386Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_0.slv region 3 firewall.

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Table 14-510. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 386Ch

Figure 14-169. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-512. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-512. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.171 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 3870h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_0.slv region 3 firewall.

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Table 14-513. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3870h

Figure 14-170. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-515. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.172 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 3874h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_0.slv region 3 firewall.

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Table 14-516. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3874h

Figure 14-171. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-518. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.173 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 3878h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_0.slv region 3 firewall.

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Table 14-519. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3878h

Figure 14-172. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-521. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.174 CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 387Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_0.slv region 3 firewall.

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Table 14-522. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 387Ch

Figure 14-173. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-524. CBASS_FW_IMSRAM32KX64E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.175 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_CONTROL Register (Offset = 3C00h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Imsram32kx64e_main_1.slv region 0 firewall.

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Table 14-525. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C00h

Figure 14-174. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-527. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.176 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 3C04h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 0 firewall.

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Table 14-528. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C04h

Figure 14-175. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-530. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-530. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.177 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 3C08h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 0 firewall.

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Table 14-531. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C08h

Figure 14-176. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-533. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-533. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.178 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 3C0Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 0 firewall.

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Table 14-534. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C0Ch

Figure 14-177. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-536. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-536. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.179 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 3C10h) [reset = 70040000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_1.slv region 0 firewall.

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Table 14-537. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C10h

Figure 14-178. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
70040h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
70040h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
70040h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-539. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	70040h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.180 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 3C14h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_1.slv region 0 firewall.

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Table 14-540. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C14h

Figure 14-179. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-542. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.181 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 3C18h) [reset = 7007FFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_1.slv region 0 firewall.

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Table 14-543. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C18h

Figure 14-180. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7007Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7007Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7007Fh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-545. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7007Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.182 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 3C1Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_1.slv region 0 firewall.

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Table 14-546. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C1Ch

Figure 14-181. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-548. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.183 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_CONTROL Register (Offset = 3C20h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Imsram32kx64e_main_1.slv region 1 firewall.

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Table 14-549. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C20h

Figure 14-182. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-551. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.184 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 3C24h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 1 firewall.

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Table 14-552. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C24h

Figure 14-183. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-554. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-554. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.185 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 3C28h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 1 firewall.

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Table 14-555. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C28h

Figure 14-184. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-557. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-557. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.186 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 3C2Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 1 firewall.

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Table 14-558. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C2Ch

Figure 14-185. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-560. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-560. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.187 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 3C30h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_1.slv region 1 firewall.

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Table 14-561. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C30h

Figure 14-186. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-563. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.188 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 3C34h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_1.slv region 1 firewall.

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Table 14-564. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C34h

Figure 14-187. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-566. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.189 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 3C38h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_1.slv region 1 firewall.

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Table 14-567. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C38h

Figure 14-188. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-569. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.190 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 3C3Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_1.slv region 1 firewall.

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Table 14-570. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C3Ch

Figure 14-189. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-572. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.191 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_CONTROL Register (Offset = 3C40h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Imsram32kx64e_main_1.slv region 2 firewall.

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Table 14-573. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C40h

Figure 14-190. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-575. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.192 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 3C44h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 2 firewall.

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Table 14-576. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C44h

Figure 14-191. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-578. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-578. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.193 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 3C48h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 2 firewall.

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Table 14-579. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C48h

Figure 14-192. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-581. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-581. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.194 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 3C4Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 2 firewall.

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Table 14-582. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C4Ch

Figure 14-193. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-584. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-584. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.195 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 3C50h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_1.slv region 2 firewall.

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Table 14-585. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C50h

Figure 14-194. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-587. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.196 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 3C54h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_1.slv region 2 firewall.

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Table 14-588. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C54h

Figure 14-195. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-590. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.197 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 3C58h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_1.slv region 2 firewall.

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Table 14-591. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C58h

Figure 14-196. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-593. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.198 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 3C5Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_1.slv region 2 firewall.

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Table 14-594. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C5Ch

Figure 14-197. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-596. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.199 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_CONTROL Register (Offset = 3C60h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Imsram32kx64e_main_1.slv region 3 firewall.

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Table 14-597. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C60h

Figure 14-198. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-599. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.200 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 3C64h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 3 firewall.

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Table 14-600. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C64h

Figure 14-199. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-602. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-602. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.201 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 3C68h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 3 firewall.

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Table 14-603. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C68h

Figure 14-200. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-605. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-605. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.202 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 3C6Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_1.slv region 3 firewall.

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Table 14-606. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C6Ch

Figure 14-201. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-608. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-608. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.203 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 3C70h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_1.slv region 3 firewall.

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Table 14-609. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C70h

Figure 14-202. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-611. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.204 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 3C74h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_1.slv region 3 firewall.

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Table 14-612. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C74h

Figure 14-203. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-614. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.205 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 3C78h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_1.slv region 3 firewall.

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Table 14-615. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C78h

Figure 14-204. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-617. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.206 CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 3C7Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_1.slv region 3 firewall.

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Table 14-618. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 3C7Ch

Figure 14-205. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-620. CBASS_FW_IMSRAM32KX64E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.207 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_CONTROL Register (Offset = 4000h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Imsram32kx64e_main_2.slv region 0 firewall.

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Table 14-621. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4000h

Figure 14-206. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-623. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.208 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 4004h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 0 firewall.

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Table 14-624. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4004h

Figure 14-207. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-626. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-626. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.209 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 4008h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 0 firewall.

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Table 14-627. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4008h

Figure 14-208. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-629. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-629. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.210 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 400Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 0 firewall.

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Table 14-630. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 400Ch

Figure 14-209. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-632. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-632. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.211 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 4010h) [reset = 70080000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_2.slv region 0 firewall.

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Table 14-633. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4010h

Figure 14-210. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
70080h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
70080h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
70080h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-635. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	70080h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.212 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 4014h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_2.slv region 0 firewall.

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Table 14-636. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4014h

Figure 14-211. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-638. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.213 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 4018h) [reset = 700BFFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_2.slv region 0 firewall.

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Table 14-639. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4018h

Figure 14-212. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
700BFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
700BFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
700BFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-641. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	700BFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.214 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 401Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_2.slv region 0 firewall.

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Table 14-642. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 401Ch

Figure 14-213. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-644. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.215 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_CONTROL Register (Offset = 4020h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Imsram32kx64e_main_2.slv region 1 firewall.

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Table 14-645. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4020h

Figure 14-214. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-647. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.216 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 4024h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 1 firewall.

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Table 14-648. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4024h

Figure 14-215. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-650. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-650. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.217 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 4028h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 1 firewall.

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Table 14-651. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4028h

Figure 14-216. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-653. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-653. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.218 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 402Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 1 firewall.

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Table 14-654. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 402Ch

Figure 14-217. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-656. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-656. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.219 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 4030h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_2.slv region 1 firewall.

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Table 14-657. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4030h

Figure 14-218. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-659. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.220 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 4034h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_2.slv region 1 firewall.

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Table 14-660. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4034h

Figure 14-219. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-662. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.221 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 4038h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_2.slv region 1 firewall.

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Table 14-663. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4038h

Figure 14-220. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-665. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.222 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 403Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_2.slv region 1 firewall.

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Table 14-666. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 403Ch

Figure 14-221. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-668. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.223 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_CONTROL Register (Offset = 4040h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Imsram32kx64e_main_2.slv region 2 firewall.

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Table 14-669. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4040h

Figure 14-222. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-671. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.224 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 4044h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 2 firewall.

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Table 14-672. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4044h

Figure 14-223. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-674. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-674. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.225 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 4048h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 2 firewall.

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Table 14-675. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4048h

Figure 14-224. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-677. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-677. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.226 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 404Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 2 firewall.

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Table 14-678. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 404Ch

Figure 14-225. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-680. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-680. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.227 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 4050h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_2.slv region 2 firewall.

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Table 14-681. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4050h

Figure 14-226. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-683. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.228 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 4054h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_2.slv region 2 firewall.

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Table 14-684. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4054h

Figure 14-227. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-686. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.229 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 4058h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_2.slv region 2 firewall.

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Table 14-687. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4058h

Figure 14-228. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-689. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.230 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 405Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_2.slv region 2 firewall.

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Table 14-690. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 405Ch

Figure 14-229. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-692. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.231 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_CONTROL Register (Offset = 4060h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Imsram32kx64e_main_2.slv region 3 firewall.

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Table 14-693. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4060h

Figure 14-230. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-695. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.232 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 4064h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 3 firewall.

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Table 14-696. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4064h

Figure 14-231. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-698. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-698. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.233 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 4068h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 3 firewall.

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Table 14-699. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4068h

Figure 14-232. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-701. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-701. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.234 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 406Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_2.slv region 3 firewall.

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Table 14-702. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 406Ch

Figure 14-233. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-704. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-704. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.235 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 4070h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_2.slv region 3 firewall.

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Table 14-705. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4070h

Figure 14-234. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-707. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.236 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 4074h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_2.slv region 3 firewall.

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Table 14-708. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4074h

Figure 14-235. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-710. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.237 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 4078h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_2.slv region 3 firewall.

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Table 14-711. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4078h

Figure 14-236. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-713. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.238 CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 407Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_2.slv region 3 firewall.

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Table 14-714. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 407Ch

Figure 14-237. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-716. CBASS_FW_IMSRAM32KX64E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.239 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_CONTROL Register (Offset = 4400h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Imsram32kx64e_main_5.slv region 0 firewall.

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Table 14-717. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4400h

Figure 14-238. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-719. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.240 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 4404h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 0 firewall.

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Table 14-720. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4404h

Figure 14-239. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-722. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-722. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.241 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 4408h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 0 firewall.

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Table 14-723. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4408h

Figure 14-240. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-725. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-725. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.242 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 440Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 0 firewall.

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Table 14-726. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 440Ch

Figure 14-241. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-728. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-728. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.243 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 4410h) [reset = 70140000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_5.slv region 0 firewall.

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Table 14-729. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4410h

Figure 14-242. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">70140h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">70140h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">70140h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-731. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	70140h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.244 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 4414h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_5.slv region 0 firewall.

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Table 14-732. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4414h

Figure 14-243. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-734. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.245 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 4418h) [reset = 7017FFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_5.slv region 0 firewall.

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Table 14-735. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4418h

Figure 14-244. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7017Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7017Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7017Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-737. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7017Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.246 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 441Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_5.slv region 0 firewall.

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Table 14-738. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 441Ch

Figure 14-245. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-740. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.247 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_CONTROL Register (Offset = 4420h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Imsram32kx64e_main_5.slv region 1 firewall.

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Table 14-741. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4420h

Figure 14-246. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-743. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.248 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 4424h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 1 firewall.

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Table 14-744. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4424h

Figure 14-247. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-746. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-746. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.249 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 4428h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 1 firewall.

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Table 14-747. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4428h

Figure 14-248. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-749. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-749. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.250 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 442Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 1 firewall.

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Table 14-750. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 442Ch

Figure 14-249. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-752. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-752. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.251 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 4430h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_5.slv region 1 firewall.

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Table 14-753. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4430h

Figure 14-250. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-755. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.252 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 4434h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_5.slv region 1 firewall.

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Table 14-756. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4434h

Figure 14-251. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-758. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.253 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 4438h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_5.slv region 1 firewall.

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Table 14-759. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4438h

Figure 14-252. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-761. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.254 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 443Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_5.slv region 1 firewall.

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Table 14-762. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 443Ch

Figure 14-253. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-764. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.255 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_CONTROL Register (Offset = 4440h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Imsram32kx64e_main_5.slv region 2 firewall.

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Table 14-765. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4440h

Figure 14-254. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-767. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.256 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 4444h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 2 firewall.

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Table 14-768. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4444h

Figure 14-255. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-770. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-770. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.257 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 4448h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 2 firewall.

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Table 14-771. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4448h

Figure 14-256. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-773. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-773. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.258 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 444Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 2 firewall.

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Table 14-774. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 444Ch

Figure 14-257. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-776. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-776. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.259 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 4450h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_5.slv region 2 firewall.

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Table 14-777. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4450h

Figure 14-258. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-779. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.260 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 4454h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_5.slv region 2 firewall.

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Table 14-780. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4454h

Figure 14-259. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-782. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.261 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 4458h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_5.slv region 2 firewall.

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Table 14-783. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4458h

Figure 14-260. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-785. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.262 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 445Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_5.slv region 2 firewall.

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Table 14-786. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 445Ch

Figure 14-261. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-788. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.263 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_CONTROL Register (Offset = 4460h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Imsram32kx64e_main_5.slv region 3 firewall.

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Table 14-789. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4460h

Figure 14-262. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-791. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.264 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 4464h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 3 firewall.

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Table 14-792. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4464h

Figure 14-263. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-794. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-794. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.265 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 4468h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 3 firewall.

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Table 14-795. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4468h

Figure 14-264. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-797. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-797. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.266 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 446Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_5.slv region 3 firewall.

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Table 14-798. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 446Ch

Figure 14-265. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-800. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-800. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.267 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 4470h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_5.slv region 3 firewall.

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Table 14-801. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4470h

Figure 14-266. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-803. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.268 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 4474h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_5.slv region 3 firewall.

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Table 14-804. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4474h

Figure 14-267. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-806. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.269 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 4478h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_5.slv region 3 firewall.

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Table 14-807. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4478h

Figure 14-268. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-809. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.270 CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 447Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_5.slv region 3 firewall.

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Table 14-810. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 447Ch

Figure 14-269. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-812. CBASS_FW_IMSRAM32KX64E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.271 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_CONTROL Register (Offset = 4800h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Imsram32kx64e_main_4.slv region 0 firewall.

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Table 14-813. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4800h

Figure 14-270. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-815. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.272 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 4804h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 0 firewall.

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Table 14-816. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4804h

Figure 14-271. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-818. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-818. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.273 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 4808h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 0 firewall.

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Table 14-819. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4808h

Figure 14-272. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-821. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-821. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.274 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 480Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 0 firewall.

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Table 14-822. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 480Ch

Figure 14-273. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-824. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-824. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.275 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 4810h) [reset = 70100000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_4.slv region 0 firewall.

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Table 14-825. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4810h

Figure 14-274. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
70100h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
70100h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
70100h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-827. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	70100h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.276 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 4814h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_4.slv region 0 firewall.

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Table 14-828. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4814h

Figure 14-275. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-830. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.277 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 4818h) [reset = 7013FFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_4.slv region 0 firewall.

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Table 14-831. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4818h

Figure 14-276. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7013Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
7013Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7013Fh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-833. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7013Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.278 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 481Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_4.slv region 0 firewall.

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Table 14-834. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 481Ch

Figure 14-277. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-836. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.279 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_CONTROL Register (Offset = 4820h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Imsram32kx64e_main_4.slv region 1 firewall.

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Table 14-837. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4820h

Figure 14-278. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-839. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.280 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 4824h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 1 firewall.

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Table 14-840. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4824h

Figure 14-279. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-842. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-842. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.281 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 4828h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 1 firewall.

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Table 14-843. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4828h

Figure 14-280. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-845. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-845. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.282 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 482Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 1 firewall.

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Table 14-846. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 482Ch

Figure 14-281. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-848. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-848. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.283 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 4830h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_4.slv region 1 firewall.

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Table 14-849. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4830h

Figure 14-282. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-851. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.284 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 4834h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_4.slv region 1 firewall.

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Table 14-852. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4834h

Figure 14-283. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-854. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.285 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 4838h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_4.slv region 1 firewall.

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Table 14-855. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4838h

Figure 14-284. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-857. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.286 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 483Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_4.slv region 1 firewall.

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Table 14-858. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 483Ch

Figure 14-285. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-860. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.287 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_CONTROL Register (Offset = 4840h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Imsram32kx64e_main_4.slv region 2 firewall.

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Table 14-861. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4840h

Figure 14-286. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-863. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.288 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 4844h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 2 firewall.

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Table 14-864. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4844h

Figure 14-287. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-866. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-866. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.289 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 4848h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 2 firewall.

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Table 14-867. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4848h

Figure 14-288. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-869. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-869. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.290 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 484Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 2 firewall.

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Table 14-870. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 484Ch

Figure 14-289. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-872. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-872. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.291 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 4850h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_4.slv region 2 firewall.

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Table 14-873. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4850h

Figure 14-290. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-875. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.292 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 4854h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_4.slv region 2 firewall.

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Table 14-876. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4854h

Figure 14-291. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-878. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.293 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 4858h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_4.slv region 2 firewall.

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Table 14-879. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4858h

Figure 14-292. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-881. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.294 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 485Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_4.slv region 2 firewall.

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Table 14-882. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 485Ch

Figure 14-293. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-884. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.295 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_CONTROL Register (Offset = 4860h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Imsram32kx64e_main_4.slv region 3 firewall.

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Table 14-885. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4860h

Figure 14-294. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-887. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.296 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 4864h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 3 firewall.

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Table 14-888. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4864h

Figure 14-295. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-890. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-890. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.297 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 4868h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 3 firewall.

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Table 14-891. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4868h

Figure 14-296. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-893. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-893. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.298 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 486Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_4.slv region 3 firewall.

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Table 14-894. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 486Ch

Figure 14-297. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-896. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-896. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.299 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 4870h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_4.slv region 3 firewall.

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Table 14-897. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4870h

Figure 14-298. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-899. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.300 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 4874h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_4.slv region 3 firewall.

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Table 14-900. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4874h

Figure 14-299. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-902. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.301 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 4878h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_4.slv region 3 firewall.

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Table 14-903. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4878h

Figure 14-300. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-905. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.302 CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 487Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_4.slv region 3 firewall.

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Table 14-906. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 487Ch

Figure 14-301. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-908. CBASS_FW_IMSRAM32KX64E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.303 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_CONTROL Register (Offset = 4C00h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Imsram32kx64e_main_3.slv region 0 firewall.

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Table 14-909. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C00h

Figure 14-302. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-911. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.304 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 4C04h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 0 firewall.

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Table 14-912. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C04h

Figure 14-303. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-914. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-914. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.305 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 4C08h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 0 firewall.

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Table 14-915. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C08h

Figure 14-304. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-917. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-917. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.306 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 4C0Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 0 firewall.

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Table 14-918. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C0Ch

Figure 14-305. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-920. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-920. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.307 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 4C10h) [reset = 700C0000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_3.slv region 0 firewall.

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Table 14-921. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C10h

Figure 14-306. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">700C0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">700C0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">700C0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-923. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	700C0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.308 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 4C14h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_3.slv region 0 firewall.

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Table 14-924. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C14h

Figure 14-307. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-926. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.309 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 4C18h) [reset = 700FFFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_3.slv region 0 firewall.

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Table 14-927. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C18h

Figure 14-308. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">700FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">700FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">700FFh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-929. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	700FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.310 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 4C1Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_3.slv region 0 firewall.

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Table 14-930. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C1Ch

Figure 14-309. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-932. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.311 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_CONTROL Register (Offset = 4C20h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Imsram32kx64e_main_3.slv region 1 firewall.

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Table 14-933. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C20h

Figure 14-310. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-935. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.312 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 4C24h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 1 firewall.

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Table 14-936. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C24h

Figure 14-311. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-938. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-938. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.313 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 4C28h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 1 firewall.

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Table 14-939. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C28h

Figure 14-312. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-941. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-941. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.314 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 4C2Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 1 firewall.

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Table 14-942. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C2Ch

Figure 14-313. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-944. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-944. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.315 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 4C30h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_3.slv region 1 firewall.

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Table 14-945. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C30h

Figure 14-314. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-947. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.316 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 4C34h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_3.slv region 1 firewall.

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Table 14-948. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C34h

Figure 14-315. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-950. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.317 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 4C38h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_3.slv region 1 firewall.

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Table 14-951. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C38h

Figure 14-316. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-953. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.318 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 4C3Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_3.slv region 1 firewall.

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Table 14-954. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C3Ch

Figure 14-317. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-956. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.319 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_CONTROL Register (Offset = 4C40h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Imsram32kx64e_main_3.slv region 2 firewall.

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Table 14-957. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C40h

Figure 14-318. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-959. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.320 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 4C44h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 2 firewall.

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Table 14-960. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C44h

Figure 14-319. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-962. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-962. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.321 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 4C48h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 2 firewall.

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Table 14-963. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C48h

Figure 14-320. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-965. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-965. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.322 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 4C4Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 2 firewall.

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Table 14-966. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C4Ch

Figure 14-321. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-968. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-968. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.323 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 4C50h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_3.slv region 2 firewall.

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Table 14-969. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C50h

Figure 14-322. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-971. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.324 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 4C54h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_3.slv region 2 firewall.

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Table 14-972. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C54h

Figure 14-323. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-974. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.325 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 4C58h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_3.slv region 2 firewall.

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Table 14-975. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C58h

Figure 14-324. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-977. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.326 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 4C5Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_3.slv region 2 firewall.

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Table 14-978. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C5Ch

Figure 14-325. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-980. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.327 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_CONTROL Register (Offset = 4C60h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Imsram32kx64e_main_3.slv region 3 firewall.

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Table 14-981. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C60h

Figure 14-326. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-983. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.328 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 4C64h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 3 firewall.

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Table 14-984. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C64h

Figure 14-327. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-986. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-986. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.329 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 4C68h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 3 firewall.

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Table 14-987. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C68h

Figure 14-328. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-989. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-989. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.330 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 4C6Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_3.slv region 3 firewall.

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Table 14-990. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C6Ch

Figure 14-329. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-992. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-992. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.331 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 4C70h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_3.slv region 3 firewall.

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Table 14-993. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C70h

Figure 14-330. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-995. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.332 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 4C74h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_3.slv region 3 firewall.

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Table 14-996. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C74h

Figure 14-331. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-998. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.333 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 4C78h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_3.slv region 3 firewall.

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Table 14-999. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C78h

Figure 14-332. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1001. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.334 CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 4C7Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_3.slv region 3 firewall.

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Table 14-1002. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 4C7Ch

Figure 14-333. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1004. CBASS_FW_IMSRAM32KX64E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.335 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register (Offset = 5000h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Idmss_am64_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-1005. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5000h

Figure 14-334. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1007. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.336 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register (Offset = 5004h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-1008. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5004h

Figure 14-335. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1010. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1010. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.337 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register (Offset = 5008h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-1011. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5008h

Figure 14-336. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1013. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1013. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.338 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register (Offset = 500Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-1014. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 500Ch

Figure 14-337. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1016. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1016. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.339 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register (Offset = 5010h) [reset = 9B000000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-1017. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5010h

Figure 14-338. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">9B000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">9B000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">9B000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1019. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	9B000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.340 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register (Offset = 5014h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-1020. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5014h

Figure 14-339. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1022. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.341 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register (Offset = 5018h) [reset = 9B07FFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-1023. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5018h

Figure 14-340. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">9B07Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">9B07Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">9B07Fh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1025. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	9B07Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.342 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register (Offset = 501Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-1026. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 501Ch

Figure 14-341. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1028. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.343 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register (Offset = 5020h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Idmss_am64_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-1029. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5020h

Figure 14-342. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1031. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.344 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register (Offset = 5024h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-1032. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5024h

Figure 14-343. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1034. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1034. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.345 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register (Offset = 5028h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-1035. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5028h

Figure 14-344. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1037. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1037. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.346 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register (Offset = 502Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-1038. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 502Ch

Figure 14-345. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1040. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1040. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.347 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register (Offset = 5030h) [reset = 9C000000h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-1041. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5030h

Figure 14-346. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">9C000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">9C000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">9C000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1043. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	9C000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.348 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register (Offset = 5034h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-1044. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5034h

Figure 14-347. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1046. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.349 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register (Offset = 5038h) [reset = 9C3FFFFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-1047. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5038h

Figure 14-348. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
9C3FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
9C3FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
9C3FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1049. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	9C3FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.350 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register (Offset = 503Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-1050. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 503Ch

Figure 14-349. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1052. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.351 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register (Offset = 5040h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Idmss_am64_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-1053. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5040h

Figure 14-350. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1055. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.352 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register (Offset = 5044h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-1056. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5044h

Figure 14-351. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1058. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1058. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.353 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register (Offset = 5048h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-1059. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5048h

Figure 14-352. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1061. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1061. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.354 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register (Offset = 504Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-1062. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 504Ch

Figure 14-353. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1064. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1064. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.355 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register (Offset = 5050h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-1065. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5050h

Figure 14-354. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1067. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.356 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register (Offset = 5054h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-1068. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5054h

Figure 14-355. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1070. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.357 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register (Offset = 5058h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-1071. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5058h

Figure 14-356. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1073. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.358 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register (Offset = 505Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-1074. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 505Ch

Figure 14-357. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1076. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.359 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register (Offset = 5060h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Idmss_am64_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-1077. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5060h

Figure 14-358. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1079. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.360 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register (Offset = 5064h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-1080. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5064h

Figure 14-359. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1082. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1082. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.361 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register (Offset = 5068h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-1083. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5068h

Figure 14-360. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1085. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1085. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.362 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register (Offset = 506Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-1086. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 506Ch

Figure 14-361. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1088. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1088. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.363 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register (Offset = 5070h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-1089. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5070h

Figure 14-362. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1091. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.364 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register (Offset = 5074h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-1092. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5074h

Figure 14-363. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1094. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.365 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register (Offset = 5078h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-1095. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5078h

Figure 14-364. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1097. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.366 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register (Offset = 507Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-1098. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 507Ch

Figure 14-365. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1100. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.367 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register (Offset = 5080h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave Idmss_am64_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-1101. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5080h

Figure 14-366. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1103. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.368 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register (Offset = 5084h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-1104. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5084h

Figure 14-367. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1106. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1106. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.369 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register (Offset = 5088h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-1107. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5088h

Figure 14-368. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1109. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1109. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.370 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register (Offset = 508Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-1110. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 508Ch

Figure 14-369. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1112. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1112. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.371 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register (Offset = 5090h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-1113. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5090h

Figure 14-370. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1115. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.372 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register (Offset = 5094h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-1116. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5094h

Figure 14-371. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1118. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.373 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register (Offset = 5098h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-1119. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5098h

Figure 14-372. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1121. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.374 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register (Offset = 509Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-1122. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 509Ch

Figure 14-373. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1124. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.375 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register (Offset = 50A0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave Idmss_am64_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-1125. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50A0h

Figure 14-374. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1127. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.376 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register (Offset = 50A4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-1128. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50A4h

Figure 14-375. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1130. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1130. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.377 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register (Offset = 50A8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-1131. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50A8h

Figure 14-376. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1133. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1133. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.378 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register (Offset = 50ACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-1134. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50ACh

Figure 14-377. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1136. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1136. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.379 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register (Offset = 50B0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-1137. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50B0h

Figure 14-378. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1139. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.380 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register (Offset = 50B4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-1140. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50B4h

Figure 14-379. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1142. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.381 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register (Offset = 50B8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-1143. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50B8h

Figure 14-380. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1145. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.382 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register (Offset = 50BCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-1146. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50BCh

Figure 14-381. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1148. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.383 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register (Offset = 50C0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave Idmss_am64_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-1149. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50C0h

Figure 14-382. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1151. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.384 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register (Offset = 50C4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-1152. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50C4h

Figure 14-383. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1154. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1154. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.385 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register (Offset = 50C8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-1155. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50C8h

Figure 14-384. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1157. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1157. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.386 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register (Offset = 50CCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-1158. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50CCh

Figure 14-385. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1160. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1160. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.387 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register (Offset = 50D0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-1161. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50D0h

Figure 14-386. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1163. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.388 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register (Offset = 50D4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-1164. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50D4h

Figure 14-387. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1166. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.389 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register (Offset = 50D8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-1167. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50D8h

Figure 14-388. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1169. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.390 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register (Offset = 50DCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-1170. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50DCh

Figure 14-389. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1172. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.391 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register (Offset = 50E0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave Idmss_am64_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-1173. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50E0h

Figure 14-390. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1175. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.392 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register (Offset = 50E4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-1176. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50E4h

Figure 14-391. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1178. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1178. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.393 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register (Offset = 50E8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-1179. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50E8h

Figure 14-392. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1181. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1181. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.394 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register (Offset = 50ECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave Idmss_am64_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-1182. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50ECh

Figure 14-393. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1184. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1184. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.395 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register (Offset = 50F0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-1185. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50F0h

Figure 14-394. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1187. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.396 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register (Offset = 50F4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave Idmss_am64_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-1188. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50F4h

Figure 14-395. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1190. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.397 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register (Offset = 50F8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-1191. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50F8h

Figure 14-396. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1193. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.398 CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register (Offset = 50FCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave Idmss_am64_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-1194. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 50FCh

Figure 14-397. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1196. CBASS_FW_IDMSS_AM64_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.399 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_CONTROL Register (Offset = 5400h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 0 firewall.

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Table 14-1197. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5400h

Figure 14-398. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1199. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.400 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 5404h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 0 firewall.

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Table 14-1200. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5404h

Figure 14-399. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1202. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1202. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.401 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 5408h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 0 firewall.

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Table 14-1203. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5408h

Figure 14-400. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1205. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1205. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.402 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 540Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 0 firewall.

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Table 14-1206. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 540Ch

Figure 14-401. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1208. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1208. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.403 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 5410h) [reset = 4000000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 0 firewall.

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Table 14-1209. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5410h

Figure 14-402. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
4000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
4000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
4000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1211. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	4000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.404 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 5414h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 0 firewall.

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Table 14-1212. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5414h

Figure 14-403. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1214. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.405 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 5418h) [reset = 4000FFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 0 firewall.

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Table 14-1215. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5418h

Figure 14-404. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
4000h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
4000h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
4000h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1217. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	4000h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.406 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 541Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 0 firewall.

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Table 14-1218. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 541Ch

Figure 14-405. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1220. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.407 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_CONTROL Register (Offset = 5420h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 1 firewall.

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Table 14-1221. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5420h

Figure 14-406. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1223. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.408 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 5424h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 1 firewall.

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Table 14-1224. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5424h

Figure 14-407. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1226. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1226. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.409 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 5428h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 1 firewall.

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Table 14-1227. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5428h

Figure 14-408. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1229. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1229. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.410 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 542Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 1 firewall.

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Table 14-1230. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 542Ch

Figure 14-409. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1232. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1232. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.411 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 5430h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 1 firewall.

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Table 14-1233. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5430h

Figure 14-410. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1235. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.412 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 5434h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 1 firewall.

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Table 14-1236. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5434h

Figure 14-411. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1238. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.413 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 5438h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 1 firewall.

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Table 14-1239. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5438h

Figure 14-412. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1241. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.414 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 543Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 1 firewall.

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Table 14-1242. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 543Ch

Figure 14-413. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-1244. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.415 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_CONTROL Register (Offset = 5440h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 2 firewall.

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Table 14-1245. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5440h

Figure 14-414. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1247. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.416 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 5444h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 2 firewall.

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Table 14-1248. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5444h

Figure 14-415. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1250. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1250. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.417 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 5448h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 2 firewall.

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Table 14-1251. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5448h

Figure 14-416. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1253. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1253. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.418 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 544Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 2 firewall.

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Table 14-1254. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 544Ch

Figure 14-417. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1256. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1256. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.419 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 5450h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 2 firewall.

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Table 14-1257. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5450h

Figure 14-418. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1259. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.420 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 5454h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 2 firewall.

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Table 14-1260. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5454h

Figure 14-419. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1262. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.421 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 5458h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 2 firewall.

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Table 14-1263. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5458h

Figure 14-420. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1265. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.422 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 545Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 2 firewall.

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Table 14-1266. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 545Ch

Figure 14-421. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1268. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.423 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_CONTROL Register (Offset = 5460h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 3 firewall.

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Table 14-1269. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5460h

Figure 14-422. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1271. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.424 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 5464h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 3 firewall.

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Table 14-1272. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5464h

Figure 14-423. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1274. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1274. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.425 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 5468h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 3 firewall.

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Table 14-1275. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5468h

Figure 14-424. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1277. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1277. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.426 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 546Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 3 firewall.

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Table 14-1278. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 546Ch

Figure 14-425. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1280. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1280. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.427 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 5470h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 3 firewall.

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Table 14-1281. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5470h

Figure 14-426. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1283. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.428 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 5474h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 3 firewall.

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Table 14-1284. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5474h

Figure 14-427. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1286. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.429 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 5478h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 3 firewall.

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Table 14-1287. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5478h

Figure 14-428. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1289. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.430 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 547Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 3 firewall.

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Table 14-1290. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 547Ch

Figure 14-429. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1292. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.431 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_CONTROL Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_CONTROL Register (Offset = 5480h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 4 firewall.

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Table 14-1293. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5480h

Figure 14-430. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1295. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.432 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 5484h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 4 firewall.

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Table 14-1296. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5484h

Figure 14-431. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1298. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1298. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.433 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 5488h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 4 firewall.

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Table 14-1299. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5488h

Figure 14-432. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1301. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1301. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.434 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 548Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 4 firewall.

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Table 14-1302. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 548Ch

Figure 14-433. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1304. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1304. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.435 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 5490h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 4 firewall.

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Table 14-1305. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5490h

Figure 14-434. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1307. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.436 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 5494h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 4 firewall.

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Table 14-1308. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5494h

Figure 14-435. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1310. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.437 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 5498h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 4 firewall.

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Table 14-1311. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5498h

Figure 14-436. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1313. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.438 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 549Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 4 firewall.

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Table 14-1314. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 549Ch

Figure 14-437. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1316. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.439 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_CONTROL Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_CONTROL Register (Offset = 54A0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 5 firewall.

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Table 14-1317. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54A0h

Figure 14-438. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1319. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.440 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 54A4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 5 firewall.

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Table 14-1320. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54A4h

Figure 14-439. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1322. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1322. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.441 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 54A8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 5 firewall.

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Table 14-1323. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54A8h

Figure 14-440. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1325. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1325. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.442 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 54ACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 5 firewall.

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Table 14-1326. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54ACh

Figure 14-441. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1328. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1328. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.443 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 54B0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 5 firewall.

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Table 14-1329. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54B0h

Figure 14-442. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1331. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.444 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 54B4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 5 firewall.

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Table 14-1332. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54B4h

Figure 14-443. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1334. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.445 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 54B8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 5 firewall.

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Table 14-1335. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54B8h

Figure 14-444. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1337. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.446 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 54BCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 5 firewall.

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Table 14-1338. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54BCh

Figure 14-445. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1340. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.447 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_CONTROL Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_CONTROL Register (Offset = 54C0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 6 firewall.

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Table 14-1341. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54C0h

Figure 14-446. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1343. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.448 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 54C4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 6 firewall.

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Table 14-1344. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54C4h

Figure 14-447. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1346. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1346. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.449 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 54C8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 6 firewall.

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Table 14-1347. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54C8h

Figure 14-448. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1349. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1349. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.450 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 54CCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 6 firewall.

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Table 14-1350. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54CCh

Figure 14-449. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1352. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1352. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.451 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 54D0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 6 firewall.

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Table 14-1353. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54D0h

Figure 14-450. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1355. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.452 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 54D4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 6 firewall.

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Table 14-1356. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54D4h

Figure 14-451. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1358. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.453 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 54D8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 6 firewall.

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Table 14-1359. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54D8h

Figure 14-452. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1361. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.454 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 54DCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 6 firewall.

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Table 14-1362. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54DCh

Figure 14-453. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1364. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.455 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_CONTROL Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_CONTROL Register (Offset = 54E0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 7 firewall.

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Table 14-1365. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54E0h

Figure 14-454. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1367. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.456 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 54E4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 7 firewall.

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Table 14-1368. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54E4h

Figure 14-455. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1370. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1370. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.457 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 54E8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 7 firewall.

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Table 14-1371. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54E8h

Figure 14-456. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1373. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1373. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.458 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 54ECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 7 firewall.

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Table 14-1374. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54ECh

Figure 14-457. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1376. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1376. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.459 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 54F0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 7 firewall.

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Table 14-1377. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54F0h

Figure 14-458. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1379. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.460 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 54F4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 7 firewall.

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Table 14-1380. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54F4h

Figure 14-459. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1382. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.461 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 54F8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 7 firewall.

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Table 14-1383. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54F8h

Figure 14-460. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1385. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.462 CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 54FCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave Iexport_vbusm_32b_slv_main2mcu.slv region 7 firewall.

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Table 14-1386. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 54FCh

Figure 14-461. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1388. CBASS_FW_IEXPORT_VBUSM_32B_SLV_MAIN2MCU_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.463 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_CONTROL Register (Offset = 5800h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 0 firewall.

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Table 14-1389. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5800h

Figure 14-462. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1391. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.464 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 5804h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 0 firewall.

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Table 14-1392. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5804h

Figure 14-463. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1394. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1394. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.465 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 5808h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 0 firewall.

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Table 14-1395. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5808h

Figure 14-464. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1397. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1397. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.466 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 580Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 0 firewall.

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Table 14-1398. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 580Ch

Figure 14-465. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1400. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1400. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.467 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 5810h) [reset = 0h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 0 firewall.

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Table 14-1401. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5810h

Figure 14-466. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1403. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.468 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 5814h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 0 firewall.

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Table 14-1404. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5814h

Figure 14-467. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1406. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.469 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 5818h) [reset = FFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 0 firewall.

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Table 14-1407. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5818h

Figure 14-468. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1409. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.470 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 581Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 0 firewall.

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Table 14-1410. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 581Ch

Figure 14-469. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1412. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.471 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_CONTROL Register (Offset = 5820h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 1 firewall.

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Table 14-1413. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5820h

Figure 14-470. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1415. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.472 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 5824h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 1 firewall.

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Table 14-1416. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5824h

Figure 14-471. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1418. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1418. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.473 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 5828h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 1 firewall.

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Table 14-1419. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5828h

Figure 14-472. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1421. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1421. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.474 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 582Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 1 firewall.

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Table 14-1422. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 582Ch

Figure 14-473. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1424. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1424. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.475 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 5830h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 1 firewall.

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Table 14-1425. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5830h

Figure 14-474. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1427. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.476 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 5834h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 1 firewall.

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Table 14-1428. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5834h

Figure 14-475. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1430. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.477 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 5838h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 1 firewall.

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Table 14-1431. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5838h

Figure 14-476. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1433. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.478 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 583Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 1 firewall.

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Table 14-1434. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 583Ch

Figure 14-477. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1436. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.479 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_CONTROL Register (Offset = 5840h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 2 firewall.

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Table 14-1437. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5840h

Figure 14-478. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1439. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.480 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 5844h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 2 firewall.

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Table 14-1440. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5844h

Figure 14-479. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1442. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1442. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.481 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 5848h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 2 firewall.

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Table 14-1443. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5848h

Figure 14-480. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1445. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1445. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.482 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 584Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 2 firewall.

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Table 14-1446. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 584Ch

Figure 14-481. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1448. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1448. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.483 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 5850h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 2 firewall.

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Table 14-1449. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5850h

Figure 14-482. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1451. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.484 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 5854h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 2 firewall.

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Table 14-1452. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5854h

Figure 14-483. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1454. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.485 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 5858h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 2 firewall.

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Table 14-1455. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5858h

Figure 14-484. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1457. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.486 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 585Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 2 firewall.

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Table 14-1458. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 585Ch

Figure 14-485. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1460. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.487 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_CONTROL Register (Offset = 5860h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 3 firewall.

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Table 14-1461. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5860h

Figure 14-486. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1463. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.488 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 5864h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 3 firewall.

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Table 14-1464. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5864h

Figure 14-487. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1466. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1466. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.489 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 5868h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 3 firewall.

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Table 14-1467. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5868h

Figure 14-488. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1469. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1469. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.490 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 586Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 3 firewall.

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Table 14-1470. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 586Ch

Figure 14-489. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1472. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1472. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.491 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 5870h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 3 firewall.

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Table 14-1473. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5870h

Figure 14-490. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1475. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.492 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 5874h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 3 firewall.

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Table 14-1476. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5874h

Figure 14-491. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1478. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.493 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 5878h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 3 firewall.

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Table 14-1479. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5878h

Figure 14-492. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1481. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.494 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 587Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 3 firewall.

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Table 14-1482. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 587Ch

Figure 14-493. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1484. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.495 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_CONTROL Register (Offset = 5880h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 4 firewall.

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Table 14-1485. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5880h

Figure 14-494. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1487. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.496 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 5884h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 4 firewall.

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Table 14-1488. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5884h

Figure 14-495. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1490. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1490. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.497 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 5888h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 4 firewall.

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Table 14-1491. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5888h

Figure 14-496. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1493. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1493. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.498 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 588Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 4 firewall.

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Table 14-1494. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 588Ch

Figure 14-497. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1496. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1496. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.499 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 5890h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 4 firewall.

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Table 14-1497. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5890h

Figure 14-498. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1499. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.500 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 5894h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 4 firewall.

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Table 14-1500. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5894h

Figure 14-499. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1502. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.501 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 5898h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 4 firewall.

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Table 14-1503. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5898h

Figure 14-500. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1505. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.502 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 589Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 4 firewall.

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Table 14-1506. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 589Ch

Figure 14-501. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1508. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.503 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_CONTROL Register (Offset = 58A0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 5 firewall.

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Table 14-1509. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58A0h

Figure 14-502. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1511. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.504 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 58A4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 5 firewall.

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Table 14-1512. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58A4h

Figure 14-503. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1514. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1514. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.505 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 58A8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 5 firewall.

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Table 14-1515. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58A8h

Figure 14-504. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1517. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1517. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.506 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 58ACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 5 firewall.

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Table 14-1518. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58ACh

Figure 14-505. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1520. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1520. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.507 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 58B0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 5 firewall.

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Table 14-1521. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58B0h

Figure 14-506. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1523. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.508 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 58B4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 5 firewall.

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Table 14-1524. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58B4h

Figure 14-507. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1526. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.509 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 58B8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 5 firewall.

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Table 14-1527. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58B8h

Figure 14-508. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1529. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.510 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 58BCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 5 firewall.

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Table 14-1530. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58BCh

Figure 14-509. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1532. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.511 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_CONTROL Register (Offset = 58C0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 6 firewall.

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Table 14-1533. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58C0h

Figure 14-510. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1535. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.512 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 58C4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 6 firewall.

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Table 14-1536. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58C4h

Figure 14-511. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1538. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1538. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.513 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 58C8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 6 firewall.

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Table 14-1539. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58C8h

Figure 14-512. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1541. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1541. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.514 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 58CCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 6 firewall.

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Table 14-1542. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58CCh

Figure 14-513. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1544. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1544. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.515 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 58D0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 6 firewall.

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Table 14-1545. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58D0h

Figure 14-514. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1547. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.516 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 58D4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 6 firewall.

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Table 14-1548. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58D4h

Figure 14-515. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1550. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.517 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 58D8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 6 firewall.

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Table 14-1551. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58D8h

Figure 14-516. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1553. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.518 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 58DCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 6 firewall.

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Table 14-1554. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58DCh

Figure 14-517. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1556. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.519 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_CONTROL Register (Offset = 58E0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 7 firewall.

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Table 14-1557. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58E0h

Figure 14-518. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1559. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.520 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 58E4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 7 firewall.

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Table 14-1560. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58E4h

Figure 14-519. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1562. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1562. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.521 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 58E8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 7 firewall.

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Table 14-1563. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58E8h

Figure 14-520. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1565. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1565. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.522 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 58ECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 7 firewall.

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Table 14-1566. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58ECh

Figure 14-521. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1568. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1568. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.523 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 58F0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 7 firewall.

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Table 14-1569. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58F0h

Figure 14-522. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1571. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.524 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 58F4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 7 firewall.

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Table 14-1572. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58F4h

Figure 14-523. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1574. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.525 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 58F8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 7 firewall.

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Table 14-1575. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58F8h

Figure 14-524. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1577. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.526 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 58FCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 7 firewall.

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Table 14-1578. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 58FCh

Figure 14-525. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1580. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.527 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_CONTROL Register (Offset = 5900h) [reset = 0h]

Register Description: The FW Region 8 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 8 firewall.

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Table 14-1581. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5900h

Figure 14-526. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1583. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.528 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 5904h) [reset = 0h]

Register Description: The FW Region 8 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 8 firewall.

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Table 14-1584. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5904h

Figure 14-527. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1586. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1586. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.529 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 5908h) [reset = 0h]

Register Description: The FW Region 8 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 8 firewall.

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Table 14-1587. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5908h

Figure 14-528. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1589. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1589. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.530 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 590Ch) [reset = 0h]

Register Description: The FW Region 8 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 8 firewall.

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Table 14-1590. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 590Ch

Figure 14-529. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1592. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1592. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.531 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 5910h) [reset = 0h]

Register Description: The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 8 firewall.

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Table 14-1593. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5910h

Figure 14-530. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1595. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.532 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 5914h) [reset = 0h]

Register Description: The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 8 firewall.

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Table 14-1596. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5914h

Figure 14-531. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-1598. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.533 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 5918h) [reset = FFFh]

Register Description: The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 8 firewall.

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Table 14-1599. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5918h

Figure 14-532. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1601. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.534 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 591Ch) [reset = 0h]

Register Description: The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 8 firewall.

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Table 14-1602. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 591Ch

Figure 14-533. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1604. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.535 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_CONTROL Register (Offset = 5920h) [reset = 0h]

Register Description: The FW Region 9 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 9 firewall.

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Table 14-1605. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5920h

Figure 14-534. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1607. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.536 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 5924h) [reset = 0h]

Register Description: The FW Region 9 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 9 firewall.

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Table 14-1608. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5924h

Figure 14-535. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1610. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1610. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.537 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 5928h) [reset = 0h]

Register Description: The FW Region 9 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 9 firewall.

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Table 14-1611. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5928h

Figure 14-536. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1613. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1613. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.538 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 592Ch) [reset = 0h]

Register Description: The FW Region 9 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 9 firewall.

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Table 14-1614. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 592Ch

Figure 14-537. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1616. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1616. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.539 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 5930h) [reset = 0h]

Register Description: The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 9 firewall.

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Table 14-1617. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5930h

Figure 14-538. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1619. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.540 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 5934h) [reset = 0h]

Register Description: The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 9 firewall.

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Table 14-1620. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5934h

Figure 14-539. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1622. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.541 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 5938h) [reset = FFFh]

Register Description: The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 9 firewall.

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Table 14-1623. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5938h

Figure 14-540. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1625. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.542 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 593Ch) [reset = 0h]

Register Description: The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 9 firewall.

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Table 14-1626. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 593Ch

Figure 14-541. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1628. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.543 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_CONTROL Register (Offset = 5940h) [reset = 0h]

Register Description: The FW Region 10 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 10 firewall.

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Table 14-1629. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5940h

Figure 14-542. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1631. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.544 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 5944h) [reset = 0h]

Register Description: The FW Region 10 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 10 firewall.

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Table 14-1632. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5944h

Figure 14-543. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1634. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1634. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.545 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 5948h) [reset = 0h]

Register Description: The FW Region 10 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 10 firewall.

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Table 14-1635. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5948h

Figure 14-544. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1637. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1637. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.546 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 594Ch) [reset = 0h]

Register Description: The FW Region 10 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 10 firewall.

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Table 14-1638. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 594Ch

Figure 14-545. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1640. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1640. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.547 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 5950h) [reset = 0h]

Register Description: The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 10 firewall.

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Table 14-1641. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5950h

Figure 14-546. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1643. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.548 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 5954h) [reset = 0h]

Register Description: The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 10 firewall.

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Table 14-1644. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5954h

Figure 14-547. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1646. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.549 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 5958h) [reset = FFFh]

Register Description: The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 10 firewall.

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Table 14-1647. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5958h

Figure 14-548. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1649. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.550 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 595Ch) [reset = 0h]

Register Description: The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 10 firewall.

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Table 14-1650. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 595Ch

Figure 14-549. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1652. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.551 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_CONTROL Register (Offset = 5960h) [reset = 0h]

Register Description: The FW Region 11 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 11 firewall.

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Table 14-1653. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5960h

Figure 14-550. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1655. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.552 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 5964h) [reset = 0h]

Register Description: The FW Region 11 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 11 firewall.

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Table 14-1656. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5964h

Figure 14-551. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1658. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1658. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.553 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 5968h) [reset = 0h]

Register Description: The FW Region 11 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 11 firewall.

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Table 14-1659. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5968h

Figure 14-552. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1661. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1661. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.554 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 596Ch) [reset = 0h]

Register Description: The FW Region 11 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 11 firewall.

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Table 14-1662. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 596Ch

Figure 14-553. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1664. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1664. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.555 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 5970h) [reset = 0h]

Register Description: The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 11 firewall.

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Table 14-1665. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5970h

Figure 14-554. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1667. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.556 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 5974h) [reset = 0h]

Register Description: The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 11 firewall.

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Table 14-1668. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5974h

Figure 14-555. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1670. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.557 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 5978h) [reset = FFFh]

Register Description: The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 11 firewall.

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Table 14-1671. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5978h

Figure 14-556. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1673. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.558 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 597Ch) [reset = 0h]

Register Description: The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 11 firewall.

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Table 14-1674. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 597Ch

Figure 14-557. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1676. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.559 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_CONTROL Register (Offset = 5980h) [reset = 0h]

Register Description: The FW Region 12 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 12 firewall.

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Table 14-1677. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5980h

Figure 14-558. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1679. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.560 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 5984h) [reset = 0h]

Register Description: The FW Region 12 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 12 firewall.

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Table 14-1680. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5984h

Figure 14-559. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1682. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1682. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.561 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 5988h) [reset = 0h]

Register Description: The FW Region 12 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 12 firewall.

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Table 14-1683. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5988h

Figure 14-560. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1685. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1685. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.562 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 598Ch) [reset = 0h]

Register Description: The FW Region 12 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 12 firewall.

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Table 14-1686. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 598Ch

Figure 14-561. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1688. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1688. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.563 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 5990h) [reset = 0h]

Register Description: The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 12 firewall.

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Table 14-1689. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5990h

Figure 14-562. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1691. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.564 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 5994h) [reset = 0h]

Register Description: The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 12 firewall.

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Table 14-1692. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5994h

Figure 14-563. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1694. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.565 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 5998h) [reset = FFFh]

Register Description: The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 12 firewall.

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Table 14-1695. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5998h

Figure 14-564. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1697. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.566 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 599Ch) [reset = 0h]

Register Description: The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 12 firewall.

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Table 14-1698. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 599Ch

Figure 14-565. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1700. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.567 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_CONTROL Register (Offset = 59A0h) [reset = 0h]

Register Description: The FW Region 13 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 13 firewall.

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Table 14-1701. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59A0h

Figure 14-566. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1703. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.568 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 59A4h) [reset = 0h]

Register Description: The FW Region 13 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 13 firewall.

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Table 14-1704. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59A4h

Figure 14-567. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1706. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1706. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.569 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 59A8h) [reset = 0h]

Register Description: The FW Region 13 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 13 firewall.

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Table 14-1707. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59A8h

Figure 14-568. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1709. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1709. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.570 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 59ACh) [reset = 0h]

Register Description: The FW Region 13 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 13 firewall.

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Table 14-1710. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59ACh

Figure 14-569. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1712. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1712. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.571 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 59B0h) [reset = 0h]

Register Description: The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 13 firewall.

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Table 14-1713. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59B0h

Figure 14-570. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1715. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.572 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 59B4h) [reset = 0h]

Register Description: The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 13 firewall.

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Table 14-1716. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59B4h

Figure 14-571. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1718. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.573 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 59B8h) [reset = FFFh]

Register Description: The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 13 firewall.

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Table 14-1719. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59B8h

Figure 14-572. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1721. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.574 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 59BCh) [reset = 0h]

Register Description: The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 13 firewall.

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Table 14-1722. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59BCh

Figure 14-573. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1724. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.575 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_CONTROL Register (Offset = 59C0h) [reset = 0h]

Register Description: The FW Region 14 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 14 firewall.

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Table 14-1725. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59C0h

Figure 14-574. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1727. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.576 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 59C4h) [reset = 0h]

Register Description: The FW Region 14 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 14 firewall.

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Table 14-1728. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59C4h

Figure 14-575. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1730. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1730. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.577 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 59C8h) [reset = 0h]

Register Description: The FW Region 14 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 14 firewall.

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Table 14-1731. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59C8h

Figure 14-576. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1733. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1733. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.578 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 59CCh) [reset = 0h]

Register Description: The FW Region 14 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 14 firewall.

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Table 14-1734. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59CCh

Figure 14-577. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1736. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1736. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.579 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 59D0h) [reset = 0h]

Register Description: The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 14 firewall.

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Table 14-1737. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59D0h

Figure 14-578. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1739. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.580 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 59D4h) [reset = 0h]

Register Description: The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 14 firewall.

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Table 14-1740. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59D4h

Figure 14-579. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1742. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.581 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 59D8h) [reset = FFFh]

Register Description: The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 14 firewall.

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Table 14-1743. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59D8h

Figure 14-580. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1745. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.582 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 59DCh) [reset = 0h]

Register Description: The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 14 firewall.

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Table 14-1746. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59DCh

Figure 14-581. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1748. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.583 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_CONTROL Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_CONTROL Register (Offset = 59E0h) [reset = 0h]

Register Description: The FW Region 15 Control Register defines the control fields for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 15 firewall.

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Table 14-1749. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59E0h

Figure 14-582. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1751. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.584 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_0 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 59E4h) [reset = 0h]

Register Description: The FW Region 15 Permission 0 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 15 firewall.

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Table 14-1752. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59E4h

Figure 14-583. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1754. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1754. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.585 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_1 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 59E8h) [reset = 0h]

Register Description: The FW Region 15 Permission 1 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 15 firewall.

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Table 14-1755. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59E8h

Figure 14-584. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1757. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1757. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.586 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_2 Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 59ECh) [reset = 0h]

Register Description: The FW Region 15 Permission 2 Register defines the permissions for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 15 firewall.

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Table 14-1758. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59ECh

Figure 14-585. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1760. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1760. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.587 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 59F0h) [reset = 0h]

Register Description: The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 15 firewall.

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Table 14-1761. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59F0h

Figure 14-586. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1763. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.588 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 59F4h) [reset = 0h]

Register Description: The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 15 firewall.

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Table 14-1764. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59F4h

Figure 14-587. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1766. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.589 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_L Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 59F8h) [reset = FFFh]

Register Description: The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 15 firewall.

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Table 14-1767. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59F8h

Figure 14-588. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1769. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.590 CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_H Register

CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 59FCh) [reset = 0h]

Register Description: The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the slave br_scrm_64b_clk2_to_scrp_misc_clk2_l0 region 15 firewall.

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Table 14-1770. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 59FCh

Figure 14-589. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1772. CBASS_FW_BR_SCRM_64B_CLK2_TO_SCRP_MISC_CLK2_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.591 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_CONTROL Register (Offset = 5C00h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Imsram32kx64e_main_6.slv region 0 firewall.

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Table 14-1773. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C00h

Figure 14-590. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1775. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.592 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 5C04h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 0 firewall.

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Table 14-1776. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C04h

Figure 14-591. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1778. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1778. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.593 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 5C08h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 0 firewall.

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Table 14-1779. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C08h

Figure 14-592. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1781. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1781. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.594 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 5C0Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 0 firewall.

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Table 14-1782. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C0Ch

Figure 14-593. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1784. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1784. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.595 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 5C10h) [reset = 440A0000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_6.slv region 0 firewall.

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Table 14-1785. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C10h

Figure 14-594. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
440A0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
440A0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
440A0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1787. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	440A0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.596 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 5C14h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_6.slv region 0 firewall.

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Table 14-1788. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C14h

Figure 14-595. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1790. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.597 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 5C18h) [reset = 440DFFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_6.slv region 0 firewall.

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Table 14-1791. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C18h

Figure 14-596. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
440DFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
440DFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
440DFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1793. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	440DFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.598 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 5C1Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_6.slv region 0 firewall.

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Table 14-1794. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C1Ch

Figure 14-597. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1796. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.599 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_CONTROL Register (Offset = 5C20h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Imsram32kx64e_main_6.slv region 1 firewall.

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Table 14-1797. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C20h

Figure 14-598. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1799. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.600 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 5C24h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 1 firewall.

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Table 14-1800. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C24h

Figure 14-599. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1802. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1802. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.601 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 5C28h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 1 firewall.

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Table 14-1803. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C28h

Figure 14-600. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1805. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1805. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.602 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 5C2Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 1 firewall.

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Table 14-1806. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C2Ch

Figure 14-601. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1808. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1808. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.603 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 5C30h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_6.slv region 1 firewall.

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Table 14-1809. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C30h

Figure 14-602. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1811. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.604 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 5C34h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_6.slv region 1 firewall.

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Table 14-1812. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C34h

Figure 14-603. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1814. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.605 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 5C38h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_6.slv region 1 firewall.

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Table 14-1815. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C38h

Figure 14-604. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1817. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.606 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 5C3Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_6.slv region 1 firewall.

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Table 14-1818. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C3Ch

Figure 14-605. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1820. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.607 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_CONTROL Register (Offset = 5C40h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Imsram32kx64e_main_6.slv region 2 firewall.

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Table 14-1821. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C40h

Figure 14-606. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1823. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.608 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 5C44h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 2 firewall.

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Table 14-1824. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C44h

Figure 14-607. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1826. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1826. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.609 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 5C48h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 2 firewall.

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Table 14-1827. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C48h

Figure 14-608. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1829. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1829. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.610 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 5C4Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 2 firewall.

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Table 14-1830. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C4Ch

Figure 14-609. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1832. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1832. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.611 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 5C50h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_6.slv region 2 firewall.

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Table 14-1833. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C50h

Figure 14-610. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1835. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.612 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 5C54h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_6.slv region 2 firewall.

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Table 14-1836. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C54h

Figure 14-611. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1838. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.613 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 5C58h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_6.slv region 2 firewall.

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Table 14-1839. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C58h

Figure 14-612. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1841. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.614 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 5C5Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_6.slv region 2 firewall.

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Table 14-1842. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C5Ch

Figure 14-613. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1844. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.615 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_CONTROL Register (Offset = 5C60h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Imsram32kx64e_main_6.slv region 3 firewall.

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Table 14-1845. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C60h

Figure 14-614. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1847. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.616 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 5C64h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 3 firewall.

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Table 14-1848. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C64h

Figure 14-615. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1850. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1850. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.617 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 5C68h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 3 firewall.

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Table 14-1851. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C68h

Figure 14-616. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1853. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1853. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.618 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 5C6Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 3 firewall.

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Table 14-1854. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C6Ch

Figure 14-617. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1856. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1856. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.619 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 5C70h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_6.slv region 3 firewall.

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Table 14-1857. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C70h

Figure 14-618. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1859. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.620 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 5C74h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_6.slv region 3 firewall.

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Table 14-1860. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C74h

Figure 14-619. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1862. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.621 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 5C78h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_6.slv region 3 firewall.

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Table 14-1863. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C78h

Figure 14-620. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1865. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.622 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 5C7Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_6.slv region 3 firewall.

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Table 14-1866. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C7Ch

Figure 14-621. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1868. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.623 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_CONTROL Register (Offset = 5C80h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave Imsram32kx64e_main_6.slv region 4 firewall.

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Table 14-1869. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C80h

Figure 14-622. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1871. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.624 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 5C84h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 4 firewall.

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Table 14-1872. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C84h

Figure 14-623. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1874. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1874. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.625 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 5C88h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 4 firewall.

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Table 14-1875. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C88h

Figure 14-624. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1877. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1877. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.626 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 5C8Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 4 firewall.

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Table 14-1878. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C8Ch

Figure 14-625. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1880. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1880. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.627 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 5C90h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_6.slv region 4 firewall.

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Table 14-1881. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C90h

Figure 14-626. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1883. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.628 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 5C94h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_6.slv region 4 firewall.

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Table 14-1884. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C94h

Figure 14-627. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1886. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.629 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 5C98h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_6.slv region 4 firewall.

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Table 14-1887. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C98h

Figure 14-628. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1889. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.630 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 5C9Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_6.slv region 4 firewall.

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Table 14-1890. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5C9Ch

Figure 14-629. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1892. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.631 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_CONTROL Register (Offset = 5CA0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave Imsram32kx64e_main_6.slv region 5 firewall.

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Table 14-1893. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CA0h

Figure 14-630. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1895. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.632 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 5CA4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 5 firewall.

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Table 14-1896. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CA4h

Figure 14-631. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1898. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1898. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.633 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 5CA8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 5 firewall.

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Table 14-1899. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CA8h

Figure 14-632. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1901. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1901. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.634 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 5CACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 5 firewall.

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Table 14-1902. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CACh

Figure 14-633. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1904. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1904. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.635 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 5CB0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_6.slv region 5 firewall.

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Table 14-1905. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CB0h

Figure 14-634. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1907. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.636 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 5CB4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_6.slv region 5 firewall.

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Table 14-1908. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CB4h

Figure 14-635. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1910. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.637 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 5CB8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_6.slv region 5 firewall.

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Table 14-1911. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CB8h

Figure 14-636. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1913. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.638 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 5CBCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_6.slv region 5 firewall.

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Table 14-1914. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CBCh

Figure 14-637. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1916. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.639 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_CONTROL Register (Offset = 5CC0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave Imsram32kx64e_main_6.slv region 6 firewall.

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Table 14-1917. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CC0h

Figure 14-638. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1919. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.640 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 5CC4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 6 firewall.

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Table 14-1920. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CC4h

Figure 14-639. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1922. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1922. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.641 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 5CC8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 6 firewall.

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Table 14-1923. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CC8h

Figure 14-640. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1925. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1925. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.642 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 5CCCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 6 firewall.

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Table 14-1926. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CCCh

Figure 14-641. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1928. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1928. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.643 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 5CD0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_6.slv region 6 firewall.

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Table 14-1929. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CD0h

Figure 14-642. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1931. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.644 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 5CD4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_6.slv region 6 firewall.

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Table 14-1932. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CD4h

Figure 14-643. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1934. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.645 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 5CD8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_6.slv region 6 firewall.

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Table 14-1935. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CD8h

Figure 14-644. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1937. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.646 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 5CDCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_6.slv region 6 firewall.

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Table 14-1938. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CDCh

Figure 14-645. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1940. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.647 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_CONTROL Register (Offset = 5CE0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave Imsram32kx64e_main_6.slv region 7 firewall.

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Table 14-1941. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CE0h

Figure 14-646. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1943. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.648 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 5CE4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 7 firewall.

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Table 14-1944. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CE4h

Figure 14-647. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1946. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1946. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.649 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 5CE8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 7 firewall.

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Table 14-1947. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CE8h

Figure 14-648. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1949. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1949. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.650 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 5CECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_6.slv region 7 firewall.

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Table 14-1950. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CECh

Figure 14-649. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1952. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1952. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.651 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 5CF0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_6.slv region 7 firewall.

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Table 14-1953. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CF0h

Figure 14-650. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1955. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.652 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 5CF4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_6.slv region 7 firewall.

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Table 14-1956. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CF4h

Figure 14-651. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1958. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.653 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 5CF8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_6.slv region 7 firewall.

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Table 14-1959. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CF8h

Figure 14-652. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1961. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.654 CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 5CFCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_6.slv region 7 firewall.

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Table 14-1962. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 5CFCh

Figure 14-653. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1964. CBASS_FW_IMSRAM32KX64E_MAIN_6_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.655 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_CONTROL Register (Offset = 6000h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave Imsram32kx64e_main_7.slv region 0 firewall.

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Table 14-1965. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6000h

Figure 14-654. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1967. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.656 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 6004h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 0 firewall.

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Table 14-1968. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6004h

Figure 14-655. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1970. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1970. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.657 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 6008h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 0 firewall.

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Table 14-1971. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6008h

Figure 14-656. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1973. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1973. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.658 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 600Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 0 firewall.

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Table 14-1974. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 600Ch

Figure 14-657. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1976. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1976. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.659 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 6010h) [reset = 701C0000h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_7.slv region 0 firewall.

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Table 14-1977. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6010h

Figure 14-658. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">701C0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">701C0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">701C0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1979. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	701C0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.660 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 6014h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_7.slv region 0 firewall.

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Table 14-1980. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6014h

Figure 14-659. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1982. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.661 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 6018h) [reset = 701FFFFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_7.slv region 0 firewall.

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Table 14-1983. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6018h

Figure 14-660. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
701FFh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
701FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
701FFh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1985. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	701FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.662 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 601Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_7.slv region 0 firewall.

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Table 14-1986. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 601Ch

Figure 14-661. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1988. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.663 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_CONTROL Register (Offset = 6020h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave Imsram32kx64e_main_7.slv region 1 firewall.

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Table 14-1989. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6020h

Figure 14-662. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1991. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.664 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 6024h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 1 firewall.

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Table 14-1992. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6024h

Figure 14-663. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1994. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1994. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.665 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 6028h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 1 firewall.

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Table 14-1995. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6028h

Figure 14-664. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1997. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1997. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.666 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 602Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 1 firewall.

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Table 14-1998. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 602Ch

Figure 14-665. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2000. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2000. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.667 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 6030h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_7.slv region 1 firewall.

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Table 14-2001. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6030h

Figure 14-666. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2003. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.668 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 6034h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_7.slv region 1 firewall.

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Table 14-2004. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6034h

Figure 14-667. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2006. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.669 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 6038h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_7.slv region 1 firewall.

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Table 14-2007. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6038h

Figure 14-668. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2009. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.670 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 603Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_7.slv region 1 firewall.

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Table 14-2010. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 603Ch

Figure 14-669. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2012. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.671 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_CONTROL Register (Offset = 6040h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave Imsram32kx64e_main_7.slv region 2 firewall.

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Table 14-2013. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6040h

Figure 14-670. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2015. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.672 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 6044h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 2 firewall.

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Table 14-2016. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6044h

Figure 14-671. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2018. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2018. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.673 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 6048h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 2 firewall.

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Table 14-2019. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6048h

Figure 14-672. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2021. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2021. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.674 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 604Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 2 firewall.

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Table 14-2022. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 604Ch

Figure 14-673. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2024. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2024. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.675 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 6050h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_7.slv region 2 firewall.

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Table 14-2025. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6050h

Figure 14-674. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2027. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.676 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 6054h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_7.slv region 2 firewall.

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Table 14-2028. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6054h

Figure 14-675. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2030. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.677 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 6058h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_7.slv region 2 firewall.

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Table 14-2031. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6058h

Figure 14-676. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2033. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.678 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 605Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_7.slv region 2 firewall.

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Table 14-2034. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 605Ch

Figure 14-677. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2036. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.679 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_CONTROL Register (Offset = 6060h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave Imsram32kx64e_main_7.slv region 3 firewall.

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Table 14-2037. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6060h

Figure 14-678. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2039. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.680 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 6064h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 3 firewall.

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Table 14-2040. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6064h

Figure 14-679. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2042. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2042. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.681 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 6068h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 3 firewall.

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Table 14-2043. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6068h

Figure 14-680. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2045. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2045. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.682 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 606Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 3 firewall.

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Table 14-2046. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 606Ch

Figure 14-681. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2048. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2048. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.683 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 6070h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_7.slv region 3 firewall.

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Table 14-2049. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6070h

Figure 14-682. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2051. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.684 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 6074h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_7.slv region 3 firewall.

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Table 14-2052. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6074h

Figure 14-683. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2054. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.685 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 6078h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_7.slv region 3 firewall.

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Table 14-2055. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6078h

Figure 14-684. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2057. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.686 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 607Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_7.slv region 3 firewall.

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Table 14-2058. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 607Ch

Figure 14-685. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2060. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.687 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_CONTROL Register (Offset = 6080h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave Imsram32kx64e_main_7.slv region 4 firewall.

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Table 14-2061. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6080h

Figure 14-686. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2063. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.688 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 6084h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 4 firewall.

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Table 14-2064. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6084h

Figure 14-687. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2066. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2066. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.689 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 6088h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 4 firewall.

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Table 14-2067. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6088h

Figure 14-688. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2069. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2069. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.690 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 608Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 4 firewall.

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Table 14-2070. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 608Ch

Figure 14-689. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2072. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2072. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.691 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 6090h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_7.slv region 4 firewall.

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Table 14-2073. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6090h

Figure 14-690. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2075. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.692 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 6094h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_7.slv region 4 firewall.

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Table 14-2076. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6094h

Figure 14-691. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2078. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.693 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 6098h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_7.slv region 4 firewall.

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Table 14-2079. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 6098h

Figure 14-692. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2081. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.694 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 609Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_7.slv region 4 firewall.

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Table 14-2082. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 609Ch

Figure 14-693. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2084. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.695 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_CONTROL Register (Offset = 60A0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave Imsram32kx64e_main_7.slv region 5 firewall.

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Table 14-2085. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60A0h

Figure 14-694. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2087. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.696 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 60A4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 5 firewall.

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Table 14-2088. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60A4h

Figure 14-695. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2090. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2090. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.697 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 60A8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 5 firewall.

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Table 14-2091. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60A8h

Figure 14-696. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2093. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2093. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.698 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 60ACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 5 firewall.

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Table 14-2094. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60ACh

Figure 14-697. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2096. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2096. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.699 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 60B0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_7.slv region 5 firewall.

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Table 14-2097. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60B0h

Figure 14-698. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2099. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.700 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 60B4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_7.slv region 5 firewall.

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Table 14-2100. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60B4h

Figure 14-699. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2102. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.701 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 60B8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_7.slv region 5 firewall.

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Table 14-2103. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60B8h

Figure 14-700. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2105. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.702 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 60BCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_7.slv region 5 firewall.

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Table 14-2106. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60BCh

Figure 14-701. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2108. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.703 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_CONTROL Register (Offset = 60C0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave Imsram32kx64e_main_7.slv region 6 firewall.

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Table 14-2109. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60C0h

Figure 14-702. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2111. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.704 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 60C4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 6 firewall.

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Table 14-2112. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60C4h

Figure 14-703. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2114. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2114. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.705 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 60C8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 6 firewall.

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Table 14-2115. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60C8h

Figure 14-704. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2117. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2117. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.706 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 60CCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 6 firewall.

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Table 14-2118. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60CCh

Figure 14-705. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2120. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2120. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.707 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 60D0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_7.slv region 6 firewall.

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Table 14-2121. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60D0h

Figure 14-706. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2123. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.708 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 60D4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_7.slv region 6 firewall.

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Table 14-2124. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60D4h

Figure 14-707. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2126. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.709 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 60D8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_7.slv region 6 firewall.

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Table 14-2127. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60D8h

Figure 14-708. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2129. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.710 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 60DCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_7.slv region 6 firewall.

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Table 14-2130. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60DCh

Figure 14-709. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2132. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.711 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_CONTROL Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_CONTROL Register (Offset = 60E0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave Imsram32kx64e_main_7.slv region 7 firewall.

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Table 14-2133. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60E0h

Figure 14-710. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2135. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.712 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 60E4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 7 firewall.

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Table 14-2136. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60E4h

Figure 14-711. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2138. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2138. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.713 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 60E8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 7 firewall.

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Table 14-2139. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60E8h

Figure 14-712. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2141. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2141. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.714 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 60ECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave Imsram32kx64e_main_7.slv region 7 firewall.

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Table 14-2142. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60ECh

Figure 14-713. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2144. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2144. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.715 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 60F0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave Imsram32kx64e_main_7.slv region 7 firewall.

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Table 14-2145. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60F0h

Figure 14-714. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2147. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.716 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 60F4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave Imsram32kx64e_main_7.slv region 7 firewall.

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Table 14-2148. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60F4h

Figure 14-715. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2150. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.717 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 60F8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave Imsram32kx64e_main_7.slv region 7 firewall.

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Table 14-2151. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60F8h

Figure 14-716. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2153. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.718 CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 60FCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave Imsram32kx64e_main_7.slv region 7 firewall.

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Table 14-2154. Instance Table

Instance Name	Physical Address
CBASS0_FW	4500 60FCh

Figure 14-717. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2156. CBASS_FW_IMSRAM32KX64E_MAIN_7_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.719 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Register (Offset = 400h) [reset = 400h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_r region 0 ISC.

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Table 14-2157. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0400h

Figure 14-718. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2159. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2159. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.720 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_r region 0 ISC.

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Table 14-2160. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0410h

Figure 14-719. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2162. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.721 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_r region 0 ISC.

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Table 14-2163. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0414h

Figure 14-720. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2165. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.722 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_r region 0 ISC.

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Table 14-2166. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0418h

Figure 14-721. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2168. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.723 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_r region 0 ISC.

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Table 14-2169. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 041Ch

Figure 14-722. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2171. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.724 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Register (Offset = 420h) [reset = 44Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_r region 1 ISC.

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Table 14-2172. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0420h

Figure 14-723. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2174. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-2174. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.725 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Register (Offset = 800h) [reset = 400h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_w region 0 ISC.

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Table 14-2175. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0800h

Figure 14-724. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2177. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2177. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.726 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_w region 0 ISC.

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Table 14-2178. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0810h

Figure 14-725. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2180. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.727 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_w region 0 ISC.

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Table 14-2181. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0814h

Figure 14-726. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2183. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.728 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_w region 0 ISC.

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Table 14-2184. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0818h

Figure 14-727. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2186. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.729 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_w region 0 ISC.

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Table 14-2187. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 081Ch

Figure 14-728. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2189. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.730 CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Register (Offset = 820h) [reset = 44Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Isam64_a53_256kb_wrap_main_0.a53_dual_wrap_cba_axi_w region 1 ISC.

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Table 14-2190. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 0820h

Figure 14-729. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2192. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-2192. CBASS_ISC_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.731 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_CONTROL Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_CONTROL Register (Offset = 1000h) [reset = 8000h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iemmc8ss_16ffc_main_0.emmcss_wr region 0 ISC.

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Table 14-2193. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1000h

Figure 14-730. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
80h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2195. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2195. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	80h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.732 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1010h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iemmc8ss_16ffc_main_0.emmcss_wr region 0 ISC.

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Table 14-2196. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1010h

Figure 14-731. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2198. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.733 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1014h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iemmc8ss_16ffc_main_0.emmcss_wr region 0 ISC.

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Table 14-2199. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1014h

Figure 14-732. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2201. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.734 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1018h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iemmc8ss_16ffc_main_0.emmcss_wr region 0 ISC.

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Table 14-2202. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1018h

Figure 14-733. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2204. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.735 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 101Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iemmc8ss_16ffc_main_0.emmcss_wr region 0 ISC.

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Table 14-2205. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 101Ch

Figure 14-734. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2207. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.736 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_DEF_CONTROL Register (Offset = 1020h) [reset = 804Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iemmc8ss_16ffc_main_0.emmcss_wr region 1 ISC.

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Table 14-2208. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1020h

Figure 14-735. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
80h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2210. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2210. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	80h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.737 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_CONTROL Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_CONTROL Register (Offset = 1400h) [reset = 8000h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iemmc8ss_16ffc_main_0.emmcss_rd region 0 ISC.

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Table 14-2211. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1400h

Figure 14-736. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">80h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2213. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2213. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	80h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.738 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iemmc8ss_16ffc_main_0.emmcss_rd region 0 ISC.

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Table 14-2214. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1410h

Figure 14-737. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2216. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.739 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iemmc8ss_16ffc_main_0.emmcss_rd region 0 ISC.

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Table 14-2217. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1414h

Figure 14-738. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2219. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.740 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iemmc8ss_16ffc_main_0.emmcss_rd region 0 ISC.

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Table 14-2220. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1418h

Figure 14-739. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2222. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.741 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_H Register (Offset = 141Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iemmc8ss_16ffc_main_0.emmcss_rd region 0 ISC.

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Table 14-2223. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 141Ch

Figure 14-740. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2225. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.742 CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_DEF_CONTROL Register (Offset = 1420h) [reset = 804Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iemmc8ss_16ffc_main_0.emmcss_rd region 1 ISC.

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Table 14-2226. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 1420h

Figure 14-741. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
80h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2228. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2228. CBASS_ISC_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	80h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.743 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Register (Offset = 2000h) [reset = 9A00h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Igic500ss_1_2_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-2229. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2000h

Figure 14-742. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Ah							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2231. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2231. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Ah	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.744 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2010h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Igic500ss_1_2_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-2232. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2010h

Figure 14-743. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2234. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.745 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2014h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Igic500ss_1_2_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-2235. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2014h

Figure 14-744. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2237. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.746 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2018h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Igic500ss_1_2_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-2238. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2018h

Figure 14-745. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2240. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.747 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H Register (Offset = 201Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Igic500ss_1_2_main_0.mem_wr_vbusm region 0 ISC.

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Table 14-2241. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 201Ch

Figure 14-746. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2243. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.748 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Register (Offset = 2020h) [reset = 9A4Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Igic500ss_1_2_main_0.mem_wr_vbusm region 1 ISC.

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Table 14-2244. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2020h

Figure 14-747. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Ah							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2246. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2246. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Ah	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.749 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Register (Offset = 2400h) [reset = 9A00h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Igic500ss_1_2_main_0.mem_rd_vbusm_isc region 0 ISC.

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Table 14-2247. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2400h

Figure 14-748. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">9Ah</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2249. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2249. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Ah	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.750 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Igic500ss_1_2_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-2250. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2410h

Figure 14-749. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2252. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.751 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Igic500ss_1_2_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-2253. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2414h

Figure 14-750. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2255. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.752 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Igic500ss_1_2_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-2256. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2418h

Figure 14-751. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2258. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.753 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H Register (Offset = 241Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Igic500ss_1_2_main_0.mem_rd_vbusm region 0 ISC.

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Table 14-2259. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 241Ch

Figure 14-752. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2261. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.754 CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Register (Offset = 2420h) [reset = 9A4Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Igic500ss_1_2_main_0.mem_rd_vbusm region 1 ISC.

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Table 14-2262. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2420h

Figure 14-753. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">9Ah</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R</td><td>R/W1TS</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td colspan="4">Ah</td></tr>
</table>

Table 14-2264. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2264. CBASS_ISC_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Ah	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.755 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_CONTROL Register (Offset = 2800h) [reset = D400h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu0_rmst region 0 ISC.

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Table 14-2265. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2800h

Figure 14-754. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2267. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2267. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.756 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2810h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu0_rmst region 0 ISC.

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Table 14-2268. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2810h

Figure 14-755. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2270. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.757 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2814h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu0_rmst region 0 ISC.

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Table 14-2271. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2814h

Figure 14-756. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2273. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.758 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2818h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu0_rmst region 0 ISC.

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Table 14-2274. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2818h

Figure 14-757. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2276. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.759 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 281Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu0_rmst region 0 ISC.

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Table 14-2277. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 281Ch

Figure 14-758. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2279. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.760 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register (Offset = 2820h) [reset = D44Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu0_rmst region 1 ISC.

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Table 14-2280. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2820h

Figure 14-759. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2282. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2282. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.761 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_CONTROL Register (Offset = 2C00h) [reset = D400h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu0_wmst region 0 ISC.

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Table 14-2283. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2C00h

Figure 14-760. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2285. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2285. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.762 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2C10h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu0_wmst region 0 ISC.

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Table 14-2286. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2C10h

Figure 14-761. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2288. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.763 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2C14h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu0_wmst region 0 ISC.

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Table 14-2289. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2C14h

Figure 14-762. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2291. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.764 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2C18h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu0_wmst region 0 ISC.

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Table 14-2292. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2C18h

Figure 14-763. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2294. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.765 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 2C1Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu0_wmst region 0 ISC.

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Table 14-2295. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2C1Ch

Figure 14-764. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2297. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.766 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register (Offset = 2C20h) [reset = D44Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu0_wmst region 1 ISC.

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Table 14-2298. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 2C20h

Figure 14-765. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2300. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2300. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.767 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_CONTROL Register (Offset = 3C00h) [reset = D500h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu1_rmst region 0 ISC.

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Table 14-2301. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 3C00h

Figure 14-766. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D5h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2303. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2303. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D5h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.768 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 3C10h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu1_rmst region 0 ISC.

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Table 14-2304. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 3C10h

Figure 14-767. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2306. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.769 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 3C14h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu1_rmst region 0 ISC.

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Table 14-2307. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 3C14h

Figure 14-768. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2309. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.770 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 3C18h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu1_rmst region 0 ISC.

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Table 14-2310. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 3C18h

Figure 14-769. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2312. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.771 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 3C1Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu1_rmst region 0 ISC.

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Table 14-2313. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 3C1Ch

Figure 14-770. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2315. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.772 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_DEF_CONTROL Register (Offset = 3C20h) [reset = D54Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu1_rmst region 1 ISC.

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Table 14-2316. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 3C20h

Figure 14-771. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D5h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2318. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2318. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D5h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.773 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_CONTROL Register (Offset = 4000h) [reset = D500h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu1_wmst region 0 ISC.

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Table 14-2319. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 4000h

Figure 14-772. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D5h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2321. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2321. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D5h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.774 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 4010h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu1_wmst region 0 ISC.

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Table 14-2322. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 4010h

Figure 14-773. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2324. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.775 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 4014h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu1_wmst region 0 ISC.

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Table 14-2325. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 4014h

Figure 14-774. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2327. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.776 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 4018h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu1_wmst region 0 ISC.

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Table 14-2328. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 4018h

Figure 14-775. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2330. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.777 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 401Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu1_wmst region 0 ISC.

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Table 14-2331. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 401Ch

Figure 14-776. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2333. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.778 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_DEF_CONTROL Register (Offset = 4020h) [reset = D54Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu1_wmst region 1 ISC.

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Table 14-2334. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 4020h

Figure 14-777. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D5h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2336. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2336. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D5h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.779 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_CONTROL Register (Offset = 5000h) [reset = D600h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu0_rmst region 0 ISC.

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Table 14-2337. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5000h

Figure 14-778. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">D6h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2339. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2339. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D6h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.780 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 5010h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu0_rmst region 0 ISC.

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Table 14-2340. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5010h

Figure 14-779. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2342. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.781 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 5014h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu0_rmst region 0 ISC.

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Table 14-2343. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5014h

Figure 14-780. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2345. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.782 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 5018h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu0_rmst region 0 ISC.

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Table 14-2346. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5018h

Figure 14-781. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2348. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.783 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 501Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu0_rmst region 0 ISC.

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Table 14-2349. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 501Ch

Figure 14-782. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2351. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.784 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_DEF_CONTROL Register (Offset = 5020h) [reset = D64Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu0_rmst region 1 ISC.

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Table 14-2352. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5020h

Figure 14-783. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D6h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2354. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2354. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D6h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.785 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_CONTROL Register (Offset = 5400h) [reset = D600h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu0_wmst region 0 ISC.

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Table 14-2355. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5400h

Figure 14-784. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D6h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2357. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2357. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D6h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.786 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 5410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu0_wmst region 0 ISC.

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Table 14-2358. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5410h

Figure 14-785. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2360. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.787 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 5414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu0_wmst region 0 ISC.

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Table 14-2361. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5414h

Figure 14-786. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2363. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.788 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 5418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu0_wmst region 0 ISC.

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Table 14-2364. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5418h

Figure 14-787. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2366. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.789 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 541Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu0_wmst region 0 ISC.

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Table 14-2367. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 541Ch

Figure 14-788. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2369. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.790 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_DEF_CONTROL Register (Offset = 5420h) [reset = D64Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu0_wmst region 1 ISC.

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Table 14-2370. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 5420h

Figure 14-789. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D6h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2372. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2372. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D6h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.791 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_CONTROL Register (Offset = 6400h) [reset = D700h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu1_rmst region 0 ISC.

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Table 14-2373. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6400h

Figure 14-790. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D7h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2375. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2375. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D7h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.792 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 6410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu1_rmst region 0 ISC.

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Table 14-2376. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6410h

Figure 14-791. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2378. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.793 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 6414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu1_rmst region 0 ISC.

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Table 14-2379. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6414h

Figure 14-792. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2381. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.794 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 6418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu1_rmst region 0 ISC.

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Table 14-2382. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6418h

Figure 14-793. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2384. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.795 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 641Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu1_rmst region 0 ISC.

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Table 14-2385. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 641Ch

Figure 14-794. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2387. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.796 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_DEF_CONTROL Register (Offset = 6420h) [reset = D74Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu1_rmst region 1 ISC.

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Table 14-2388. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6420h

Figure 14-795. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_DEF_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">D7h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R</td><td>R/W1TS</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td colspan="4">Ah</td></tr>
</table>

Table 14-2390. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2390. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D7h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.797 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_CONTROL Register (Offset = 6800h) [reset = D700h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu1_wmst region 0 ISC.

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Table 14-2391. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6800h

Figure 14-796. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D7h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2393. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2393. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D7h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.798 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 6810h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu1_wmst region 0 ISC.

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Table 14-2394. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6810h

Figure 14-797. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2396. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.799 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 6814h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu1_wmst region 0 ISC.

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Table 14-2397. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6814h

Figure 14-798. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2399. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.800 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 6818h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu1_wmst region 0 ISC.

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Table 14-2400. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6818h

Figure 14-799. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2402. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.801 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 681Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu1_wmst region 0 ISC.

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Table 14-2403. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 681Ch

Figure 14-800. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2405. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.802 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_DEF_CONTROL Register (Offset = 6820h) [reset = D74Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu1_wmst region 1 ISC.

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Table 14-2406. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 6820h

Figure 14-801. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D7h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2408. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2408. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D7h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.803 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Register (Offset = 7800h) [reset = 8800h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 0 ISC.

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Table 14-2409. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7800h

Figure 14-802. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
88h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2411. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2411. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.804 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L Register (Offset = 7810h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 0 ISC.

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Table 14-2412. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7810h

Figure 14-803. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2414. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.805 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H Register (Offset = 7814h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 0 ISC.

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Table 14-2415. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7814h

Figure 14-804. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2417. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.806 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L Register (Offset = 7818h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 0 ISC.

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Table 14-2418. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7818h

Figure 14-805. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2420. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.807 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H Register (Offset = 781Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 0 ISC.

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Table 14-2421. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 781Ch

Figure 14-806. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2423. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.808 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Register (Offset = 7820h) [reset = 8800h]

Register Description: The ISC Region 1 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 1 ISC.

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Table 14-2424. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7820h

Figure 14-807. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">88h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2426. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2426. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.809 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L Register (Offset = 7830h) [reset = 0h]

Register Description: The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 1 ISC.

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Table 14-2427. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7830h

Figure 14-808. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2429. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.810 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H Register (Offset = 7834h) [reset = 0h]

Register Description: The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 1 ISC.

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Table 14-2430. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7834h

Figure 14-809. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2432. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.811 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L Register (Offset = 7838h) [reset = FFFh]

Register Description: The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 1 ISC.

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Table 14-2433. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7838h

Figure 14-810. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2435. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.812 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H Register (Offset = 783Ch) [reset = 0h]

Register Description: The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 1 ISC.

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Table 14-2436. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 783Ch

Figure 14-811. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2438. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.813 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Register (Offset = 7840h) [reset = 8800h]

Register Description: The ISC Region 2 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 2 ISC.

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Table 14-2439. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7840h

Figure 14-812. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
88h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2441. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2441. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.814 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L Register (Offset = 7850h) [reset = 0h]

Register Description: The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 2 ISC.

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Table 14-2442. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7850h

Figure 14-813. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2444. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.815 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H Register (Offset = 7854h) [reset = 0h]

Register Description: The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 2 ISC.

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Table 14-2445. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7854h

Figure 14-814. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2447. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.816 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L Register (Offset = 7858h) [reset = FFFh]

Register Description: The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 2 ISC.

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Table 14-2448. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7858h

Figure 14-815. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2450. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.817 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H Register (Offset = 785Ch) [reset = 0h]

Register Description: The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 2 ISC.

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Table 14-2451. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 785Ch

Figure 14-816. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2453. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.818 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Register (Offset = 7860h) [reset = 8800h]

Register Description: The ISC Region 3 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 3 ISC.

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Table 14-2454. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7860h

Figure 14-817. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2456. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2456. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.819 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L Register (Offset = 7870h) [reset = 0h]

Register Description: The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 3 ISC.

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Table 14-2457. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7870h

Figure 14-818. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2459. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.820 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H Register (Offset = 7874h) [reset = 0h]

Register Description: The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 3 ISC.

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Table 14-2460. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7874h

Figure 14-819. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2462. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.821 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L Register (Offset = 7878h) [reset = FFFh]

Register Description: The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 3 ISC.

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Table 14-2463. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7878h

Figure 14-820. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2465. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.822 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H Register (Offset = 787Ch) [reset = 0h]

Register Description: The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 3 ISC.

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Table 14-2466. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 787Ch

Figure 14-821. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2468. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.823 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Register (Offset = 7880h) [reset = 8800h]

Register Description: The ISC Region 4 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 4 ISC.

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Table 14-2469. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7880h

Figure 14-822. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2471. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2471. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.824 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L Register (Offset = 7890h) [reset = 0h]

Register Description: The ISC Region 4 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 4 ISC.

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Table 14-2472. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7890h

Figure 14-823. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2474. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.825 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H Register (Offset = 7894h) [reset = 0h]

Register Description: The ISC Region 4 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 4 ISC.

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Table 14-2475. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7894h

Figure 14-824. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2477. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.826 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L Register (Offset = 7898h) [reset = FFFh]

Register Description: The ISC Region 4 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 4 ISC.

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Table 14-2478. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7898h

Figure 14-825. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2480. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.827 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H Register (Offset = 789Ch) [reset = 0h]

Register Description: The ISC Region 4 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 4 ISC.

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Table 14-2481. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 789Ch

Figure 14-826. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2483. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.828 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Register (Offset = 78A0h) [reset = 8800h]

Register Description: The ISC Region 5 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 5 ISC.

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Table 14-2484. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78A0h

Figure 14-827. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
88h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2486. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2486. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.829 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L Register (Offset = 78B0h) [reset = 0h]

Register Description: The ISC Region 5 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 5 ISC.

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Table 14-2487. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78B0h

Figure 14-828. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2489. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.830 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H Register (Offset = 78B4h) [reset = 0h]

Register Description: The ISC Region 5 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 5 ISC.

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Table 14-2490. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78B4h

Figure 14-829. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2492. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.831 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L Register (Offset = 78B8h) [reset = FFFh]

Register Description: The ISC Region 5 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 5 ISC.

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Table 14-2493. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78B8h

Figure 14-830. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2495. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.832 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H Register (Offset = 78BCh) [reset = 0h]

Register Description: The ISC Region 5 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 5 ISC.

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Table 14-2496. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78BCh

Figure 14-831. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2498. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.833 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Register (Offset = 78C0h) [reset = 8800h]

Register Description: The ISC Region 6 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 6 ISC.

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Table 14-2499. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78C0h

Figure 14-832. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2501. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2501. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.834 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L Register (Offset = 78D0h) [reset = 0h]

Register Description: The ISC Region 6 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 6 ISC.

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Table 14-2502. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78D0h

Figure 14-833. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2504. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.835 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H Register (Offset = 78D4h) [reset = 0h]

Register Description: The ISC Region 6 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 6 ISC.

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Table 14-2505. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78D4h

Figure 14-834. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2507. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.836 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L Register (Offset = 78D8h) [reset = FFFh]

Register Description: The ISC Region 6 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 6 ISC.

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Table 14-2508. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78D8h

Figure 14-835. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2510. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.837 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H Register (Offset = 78DCh) [reset = 0h]

Register Description: The ISC Region 6 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 6 ISC.

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Table 14-2511. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78DCh

Figure 14-836. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2513. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.838 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Register (Offset = 78E0h) [reset = 8800h]

Register Description: The ISC Region 7 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 7 ISC.

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Table 14-2514. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78E0h

Figure 14-837. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
88h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2516. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2516. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.839 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L Register (Offset = 78F0h) [reset = 0h]

Register Description: The ISC Region 7 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 7 ISC.

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Table 14-2517. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78F0h

Figure 14-838. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2519. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.840 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H Register (Offset = 78F4h) [reset = 0h]

Register Description: The ISC Region 7 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 7 ISC.

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Table 14-2520. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78F4h

Figure 14-839. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2522. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.841 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L Register (Offset = 78F8h) [reset = FFFh]

Register Description: The ISC Region 7 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 7 ISC.

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Table 14-2523. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78F8h

Figure 14-840. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2525. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.842 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H Register (Offset = 78FCh) [reset = 0h]

Register Description: The ISC Region 7 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 7 ISC.

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Table 14-2526. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 78FCh

Figure 14-841. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2528. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.843 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Register (Offset = 7900h) [reset = 8800h]

Register Description: The ISC Region 8 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 8 ISC.

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Table 14-2529. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7900h

Figure 14-842. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2531. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2531. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.844 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L Register (Offset = 7910h) [reset = 0h]

Register Description: The ISC Region 8 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 8 ISC.

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Table 14-2532. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7910h

Figure 14-843. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2534. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.845 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H Register (Offset = 7914h) [reset = 0h]

Register Description: The ISC Region 8 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 8 ISC.

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Table 14-2535. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7914h

Figure 14-844. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2537. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.846 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L Register (Offset = 7918h) [reset = FFFh]

Register Description: The ISC Region 8 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 8 ISC.

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Table 14-2538. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7918h

Figure 14-845. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2540. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.847 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H Register (Offset = 791Ch) [reset = 0h]

Register Description: The ISC Region 8 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 8 ISC.

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Table 14-2541. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 791Ch

Figure 14-846. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2543. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.848 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Register (Offset = 7920h) [reset = 8800h]

Register Description: The ISC Region 9 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 9 ISC.

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Table 14-2544. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7920h

Figure 14-847. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
88h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2546. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2546. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.849 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L Register (Offset = 7930h) [reset = 0h]

Register Description: The ISC Region 9 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 9 ISC.

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Table 14-2547. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7930h

Figure 14-848. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2549. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.850 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H Register (Offset = 7934h) [reset = 0h]

Register Description: The ISC Region 9 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 9 ISC.

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Table 14-2550. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7934h

Figure 14-849. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2552. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.851 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L Register (Offset = 7938h) [reset = FFFh]

Register Description: The ISC Region 9 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 9 ISC.

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Table 14-2553. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7938h

Figure 14-850. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2555. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.852 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H Register (Offset = 793Ch) [reset = 0h]

Register Description: The ISC Region 9 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 9 ISC.

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Table 14-2556. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 793Ch

Figure 14-851. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2558. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.853 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Register (Offset = 7940h) [reset = 8800h]

Register Description: The ISC Region 10 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 10 ISC.

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Table 14-2559. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7940h

Figure 14-852. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
88h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2561. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2561. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.854 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L Register (Offset = 7950h) [reset = 0h]

Register Description: The ISC Region 10 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 10 ISC.

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Table 14-2562. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7950h

Figure 14-853. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2564. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.855 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H Register (Offset = 7954h) [reset = 0h]

Register Description: The ISC Region 10 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 10 ISC.

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Table 14-2565. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7954h

Figure 14-854. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2567. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.856 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L Register (Offset = 7958h) [reset = FFFh]

Register Description: The ISC Region 10 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 10 ISC.

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Table 14-2568. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7958h

Figure 14-855. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2570. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.857 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H Register (Offset = 795Ch) [reset = 0h]

Register Description: The ISC Region 10 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 10 ISC.

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Table 14-2571. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 795Ch

Figure 14-856. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2573. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.858 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Register (Offset = 7960h) [reset = 8800h]

Register Description: The ISC Region 11 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 11 ISC.

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Table 14-2574. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7960h

Figure 14-857. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2576. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2576. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.859 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L Register (Offset = 7970h) [reset = 0h]

Register Description: The ISC Region 11 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 11 ISC.

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Table 14-2577. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7970h

Figure 14-858. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2579. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.860 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H Register (Offset = 7974h) [reset = 0h]

Register Description: The ISC Region 11 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 11 ISC.

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Table 14-2580. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7974h

Figure 14-859. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2582. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.861 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L Register (Offset = 7978h) [reset = FFFh]

Register Description: The ISC Region 11 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 11 ISC.

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Table 14-2583. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7978h

Figure 14-860. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2585. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.862 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H Register (Offset = 797Ch) [reset = 0h]

Register Description: The ISC Region 11 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 11 ISC.

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Table 14-2586. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 797Ch

Figure 14-861. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2588. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.863 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Register (Offset = 7980h) [reset = 8800h]

Register Description: The ISC Region 12 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 12 ISC.

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Table 14-2589. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7980h

Figure 14-862. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">88h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2591. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2591. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.864 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L Register (Offset = 7990h) [reset = 0h]

Register Description: The ISC Region 12 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 12 ISC.

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Table 14-2592. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7990h

Figure 14-863. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2594. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.865 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H Register (Offset = 7994h) [reset = 0h]

Register Description: The ISC Region 12 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 12 ISC.

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Table 14-2595. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7994h

Figure 14-864. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2597. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.866 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L Register (Offset = 7998h) [reset = FFFh]

Register Description: The ISC Region 12 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 12 ISC.

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Table 14-2598. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7998h

Figure 14-865. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2600. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.867 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H Register (Offset = 799Ch) [reset = 0h]

Register Description: The ISC Region 12 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 12 ISC.

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Table 14-2601. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 799Ch

Figure 14-866. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2603. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.868 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Register (Offset = 79A0h) [reset = 8800h]

Register Description: The ISC Region 13 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 13 ISC.

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Table 14-2604. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79A0h

Figure 14-867. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2606. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2606. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.869 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L Register (Offset = 79B0h) [reset = 0h]

Register Description: The ISC Region 13 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 13 ISC.

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Table 14-2607. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79B0h

Figure 14-868. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2609. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.870 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H Register (Offset = 79B4h) [reset = 0h]

Register Description: The ISC Region 13 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 13 ISC.

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Table 14-2610. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79B4h

Figure 14-869. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2612. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.871 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L Register (Offset = 79B8h) [reset = FFFh]

Register Description: The ISC Region 13 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 13 ISC.

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Table 14-2613. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79B8h

Figure 14-870. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2615. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.872 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H Register (Offset = 79BCh) [reset = 0h]

Register Description: The ISC Region 13 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 13 ISC.

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Table 14-2616. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79BCh

Figure 14-871. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2618. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.873 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Register (Offset = 79C0h) [reset = 8800h]

Register Description: The ISC Region 14 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 14 ISC.

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Table 14-2619. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79C0h

Figure 14-872. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2621. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2621. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.874 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L Register (Offset = 79D0h) [reset = 0h]

Register Description: The ISC Region 14 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 14 ISC.

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Table 14-2622. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79D0h

Figure 14-873. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2624. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.875 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H Register (Offset = 79D4h) [reset = 0h]

Register Description: The ISC Region 14 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 14 ISC.

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Table 14-2625. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79D4h

Figure 14-874. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2627. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.876 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L Register (Offset = 79D8h) [reset = FFFh]

Register Description: The ISC Region 14 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 14 ISC.

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Table 14-2628. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79D8h

Figure 14-875. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2630. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.877 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H Register (Offset = 79DCh) [reset = 0h]

Register Description: The ISC Region 14 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 14 ISC.

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Table 14-2631. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79DCh

Figure 14-876. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2633. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.878 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Register (Offset = 79E0h) [reset = 8800h]

Register Description: The ISC Region 15 Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 15 ISC.

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Table 14-2634. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79E0h

Figure 14-877. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2636. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2636. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	88h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.879 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L Register (Offset = 79F0h) [reset = 0h]

Register Description: The ISC Region 15 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 15 ISC.

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Table 14-2637. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79F0h

Figure 14-878. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2639. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.880 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H Register (Offset = 79F4h) [reset = 0h]

Register Description: The ISC Region 15 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 15 ISC.

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Table 14-2640. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79F4h

Figure 14-879. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2642. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.881 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L Register (Offset = 79F8h) [reset = FFFh]

Register Description: The ISC Region 15 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 15 ISC.

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Table 14-2643. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79F8h

Figure 14-880. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2645. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.882 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H Register (Offset = 79FCh) [reset = 0h]

Register Description: The ISC Region 15 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 15 ISC.

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Table 14-2646. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 79FCh

Figure 14-881. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2648. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.883 CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Register (Offset = 7A00h) [reset = 884Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iicss_g_16ff_main_0.pr1_ext_vbusm region 16 ISC.

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Table 14-2649. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7A00h

Figure 14-882. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
88h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2651. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2651. CBASS_ISC_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	88h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.884 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Register (Offset = 7C00h) [reset = 8900h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 0 ISC.

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Table 14-2652. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C00h

Figure 14-883. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2654. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2654. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.885 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L Register (Offset = 7C10h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 0 ISC.

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Table 14-2655. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C10h

Figure 14-884. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2657. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.886 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H Register (Offset = 7C14h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 0 ISC.

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Table 14-2658. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C14h

Figure 14-885. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2660. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.887 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L Register (Offset = 7C18h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 0 ISC.

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Table 14-2661. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C18h

Figure 14-886. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2663. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.888 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H Register (Offset = 7C1Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 0 ISC.

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Table 14-2664. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C1Ch

Figure 14-887. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2666. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.889 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Register (Offset = 7C20h) [reset = 8900h]

Register Description: The ISC Region 1 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 1 ISC.

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Table 14-2667. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C20h

Figure 14-888. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2669. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2669. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.890 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L Register (Offset = 7C30h) [reset = 0h]

Register Description: The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 1 ISC.

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Table 14-2670. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C30h

Figure 14-889. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2672. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.891 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H Register (Offset = 7C34h) [reset = 0h]

Register Description: The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 1 ISC.

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Table 14-2673. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C34h

Figure 14-890. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2675. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.892 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L Register (Offset = 7C38h) [reset = FFFh]

Register Description: The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 1 ISC.

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Table 14-2676. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C38h

Figure 14-891. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2678. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.893 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H Register (Offset = 7C3Ch) [reset = 0h]

Register Description: The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 1 ISC.

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Table 14-2679. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C3Ch

Figure 14-892. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2681. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.894 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Register (Offset = 7C40h) [reset = 8900h]

Register Description: The ISC Region 2 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 2 ISC.

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Table 14-2682. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C40h

Figure 14-893. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2684. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2684. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.895 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L Register (Offset = 7C50h) [reset = 0h]

Register Description: The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 2 ISC.

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Table 14-2685. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C50h

Figure 14-894. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2687. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.896 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H Register (Offset = 7C54h) [reset = 0h]

Register Description: The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 2 ISC.

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Table 14-2688. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C54h

Figure 14-895. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2690. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.897 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L Register (Offset = 7C58h) [reset = FFFh]

Register Description: The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 2 ISC.

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Table 14-2691. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C58h

Figure 14-896. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2693. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.898 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H Register (Offset = 7C5Ch) [reset = 0h]

Register Description: The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 2 ISC.

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Table 14-2694. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C5Ch

Figure 14-897. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2696. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.899 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Register (Offset = 7C60h) [reset = 8900h]

Register Description: The ISC Region 3 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 3 ISC.

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Table 14-2697. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C60h

Figure 14-898. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2699. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2699. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.900 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L Register (Offset = 7C70h) [reset = 0h]

Register Description: The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 3 ISC.

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Table 14-2700. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C70h

Figure 14-899. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2702. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.901 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H Register (Offset = 7C74h) [reset = 0h]

Register Description: The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 3 ISC.

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Table 14-2703. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C74h

Figure 14-900. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2705. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.902 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L Register (Offset = 7C78h) [reset = FFFh]

Register Description: The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 3 ISC.

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Table 14-2706. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C78h

Figure 14-901. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2708. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.903 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H Register (Offset = 7C7Ch) [reset = 0h]

Register Description: The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 3 ISC.

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Table 14-2709. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C7Ch

Figure 14-902. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2711. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.904 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Register (Offset = 7C80h) [reset = 8900h]

Register Description: The ISC Region 4 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 4 ISC.

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Table 14-2712. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C80h

Figure 14-903. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
89h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2714. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2714. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.905 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L Register (Offset = 7C90h) [reset = 0h]

Register Description: The ISC Region 4 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 4 ISC.

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Table 14-2715. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C90h

Figure 14-904. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2717. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.906 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H Register (Offset = 7C94h) [reset = 0h]

Register Description: The ISC Region 4 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 4 ISC.

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Table 14-2718. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C94h

Figure 14-905. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2720. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.907 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L Register (Offset = 7C98h) [reset = FFFh]

Register Description: The ISC Region 4 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 4 ISC.

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Table 14-2721. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C98h

Figure 14-906. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2723. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.908 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H Register (Offset = 7C9Ch) [reset = 0h]

Register Description: The ISC Region 4 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 4 ISC.

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Table 14-2724. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7C9Ch

Figure 14-907. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2726. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.909 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Register (Offset = 7CA0h) [reset = 8900h]

Register Description: The ISC Region 5 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 5 ISC.

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Table 14-2727. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CA0h

Figure 14-908. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
89h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2729. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2729. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.910 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L Register (Offset = 7CB0h) [reset = 0h]

Register Description: The ISC Region 5 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 5 ISC.

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Table 14-2730. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CB0h

Figure 14-909. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2732. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.911 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H Register (Offset = 7CB4h) [reset = 0h]

Register Description: The ISC Region 5 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 5 ISC.

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Table 14-2733. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CB4h

Figure 14-910. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2735. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.912 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L Register (Offset = 7CB8h) [reset = FFFh]

Register Description: The ISC Region 5 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 5 ISC.

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Table 14-2736. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CB8h

Figure 14-911. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2738. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.913 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H Register (Offset = 7CBCh) [reset = 0h]

Register Description: The ISC Region 5 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 5 ISC.

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Table 14-2739. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CBCh

Figure 14-912. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2741. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.914 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Register (Offset = 7CC0h) [reset = 8900h]

Register Description: The ISC Region 6 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 6 ISC.

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Table 14-2742. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CC0h

Figure 14-913. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
89h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2744. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2744. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.915 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L Register (Offset = 7CD0h) [reset = 0h]

Register Description: The ISC Region 6 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 6 ISC.

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Table 14-2745. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CD0h

Figure 14-914. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2747. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.916 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H Register (Offset = 7CD4h) [reset = 0h]

Register Description: The ISC Region 6 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 6 ISC.

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Table 14-2748. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CD4h

Figure 14-915. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2750. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.917 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L Register (Offset = 7CD8h) [reset = FFFh]

Register Description: The ISC Region 6 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 6 ISC.

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Table 14-2751. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CD8h

Figure 14-916. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2753. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.918 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H Register (Offset = 7CDCh) [reset = 0h]

Register Description: The ISC Region 6 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 6 ISC.

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Table 14-2754. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CDCh

Figure 14-917. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2756. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.919 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Register (Offset = 7CE0h) [reset = 8900h]

Register Description: The ISC Region 7 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 7 ISC.

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Table 14-2757. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CE0h

Figure 14-918. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2759. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2759. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.920 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L Register (Offset = 7CF0h) [reset = 0h]

Register Description: The ISC Region 7 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 7 ISC.

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Table 14-2760. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CF0h

Figure 14-919. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2762. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.921 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H Register (Offset = 7CF4h) [reset = 0h]

Register Description: The ISC Region 7 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 7 ISC.

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Table 14-2763. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CF4h

Figure 14-920. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2765. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.922 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L Register (Offset = 7CF8h) [reset = FFFh]

Register Description: The ISC Region 7 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 7 ISC.

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Table 14-2766. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CF8h

Figure 14-921. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2768. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.923 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H Register (Offset = 7CFCh) [reset = 0h]

Register Description: The ISC Region 7 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 7 ISC.

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Table 14-2769. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7CFCh

Figure 14-922. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2771. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.924 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Register (Offset = 7D00h) [reset = 8900h]

Register Description: The ISC Region 8 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 8 ISC.

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Table 14-2772. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D00h

Figure 14-923. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2774. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2774. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.925 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L Register (Offset = 7D10h) [reset = 0h]

Register Description: The ISC Region 8 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 8 ISC.

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Table 14-2775. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D10h

Figure 14-924. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2777. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.926 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H Register (Offset = 7D14h) [reset = 0h]

Register Description: The ISC Region 8 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 8 ISC.

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Table 14-2778. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D14h

Figure 14-925. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2780. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.927 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L Register (Offset = 7D18h) [reset = FFFh]

Register Description: The ISC Region 8 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 8 ISC.

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Table 14-2781. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D18h

Figure 14-926. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2783. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.928 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H Register (Offset = 7D1Ch) [reset = 0h]

Register Description: The ISC Region 8 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 8 ISC.

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Table 14-2784. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D1Ch

Figure 14-927. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2786. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.929 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Register (Offset = 7D20h) [reset = 8900h]

Register Description: The ISC Region 9 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 9 ISC.

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Table 14-2787. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D20h

Figure 14-928. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2789. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2789. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.930 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L Register (Offset = 7D30h) [reset = 0h]

Register Description: The ISC Region 9 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 9 ISC.

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Table 14-2790. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D30h

Figure 14-929. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2792. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.931 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H Register (Offset = 7D34h) [reset = 0h]

Register Description: The ISC Region 9 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 9 ISC.

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Table 14-2793. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D34h

Figure 14-930. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2795. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.932 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L Register (Offset = 7D38h) [reset = FFFh]

Register Description: The ISC Region 9 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 9 ISC.

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Table 14-2796. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D38h

Figure 14-931. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2798. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.933 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H Register (Offset = 7D3Ch) [reset = 0h]

Register Description: The ISC Region 9 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 9 ISC.

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Table 14-2799. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D3Ch

Figure 14-932. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2801. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.934 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Register (Offset = 7D40h) [reset = 8900h]

Register Description: The ISC Region 10 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 10 ISC.

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Table 14-2802. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D40h

Figure 14-933. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2804. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2804. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.935 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L Register (Offset = 7D50h) [reset = 0h]

Register Description: The ISC Region 10 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 10 ISC.

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Table 14-2805. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D50h

Figure 14-934. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2807. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.936 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H Register (Offset = 7D54h) [reset = 0h]

Register Description: The ISC Region 10 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 10 ISC.

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Table 14-2808. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D54h

Figure 14-935. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2810. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.937 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L Register (Offset = 7D58h) [reset = FFFh]

Register Description: The ISC Region 10 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 10 ISC.

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Table 14-2811. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D58h

Figure 14-936. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2813. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.938 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H Register (Offset = 7D5Ch) [reset = 0h]

Register Description: The ISC Region 10 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 10 ISC.

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Table 14-2814. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D5Ch

Figure 14-937. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2816. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.939 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Register (Offset = 7D60h) [reset = 8900h]

Register Description: The ISC Region 11 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 11 ISC.

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Table 14-2817. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D60h

Figure 14-938. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
89h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2819. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2819. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.940 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L Register (Offset = 7D70h) [reset = 0h]

Register Description: The ISC Region 11 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 11 ISC.

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Table 14-2820. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D70h

Figure 14-939. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2822. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.941 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H Register (Offset = 7D74h) [reset = 0h]

Register Description: The ISC Region 11 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 11 ISC.

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Table 14-2823. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D74h

Figure 14-940. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2825. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.942 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L Register (Offset = 7D78h) [reset = FFFh]

Register Description: The ISC Region 11 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 11 ISC.

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Table 14-2826. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D78h

Figure 14-941. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2828. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.943 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H Register (Offset = 7D7Ch) [reset = 0h]

Register Description: The ISC Region 11 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 11 ISC.

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Table 14-2829. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D7Ch

Figure 14-942. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2831. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.944 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Register (Offset = 7D80h) [reset = 8900h]

Register Description: The ISC Region 12 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 12 ISC.

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Table 14-2832. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D80h

Figure 14-943. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">89h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2834. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2834. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.945 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L Register (Offset = 7D90h) [reset = 0h]

Register Description: The ISC Region 12 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 12 ISC.

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Table 14-2835. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D90h

Figure 14-944. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2837. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.946 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H Register (Offset = 7D94h) [reset = 0h]

Register Description: The ISC Region 12 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 12 ISC.

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Table 14-2838. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D94h

Figure 14-945. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2840. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.947 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L Register (Offset = 7D98h) [reset = FFFh]

Register Description: The ISC Region 12 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 12 ISC.

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Table 14-2841. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D98h

Figure 14-946. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2843. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.948 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H Register (Offset = 7D9Ch) [reset = 0h]

Register Description: The ISC Region 12 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 12 ISC.

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Table 14-2844. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7D9Ch

Figure 14-947. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2846. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.949 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Register (Offset = 7DA0h) [reset = 8900h]

Register Description: The ISC Region 13 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 13 ISC.

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Table 14-2847. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DA0h

Figure 14-948. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
89h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2849. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2849. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.950 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L Register (Offset = 7DB0h) [reset = 0h]

Register Description: The ISC Region 13 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 13 ISC.

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Table 14-2850. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DB0h

Figure 14-949. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2852. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.951 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H Register (Offset = 7DB4h) [reset = 0h]

Register Description: The ISC Region 13 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 13 ISC.

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Table 14-2853. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DB4h

Figure 14-950. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2855. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.952 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L Register (Offset = 7DB8h) [reset = FFFh]

Register Description: The ISC Region 13 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 13 ISC.

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Table 14-2856. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DB8h

Figure 14-951. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2858. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.953 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H Register (Offset = 7DBCh) [reset = 0h]

Register Description: The ISC Region 13 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 13 ISC.

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Table 14-2859. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DBCh

Figure 14-952. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2861. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.954 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Register (Offset = 7DC0h) [reset = 8900h]

Register Description: The ISC Region 14 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 14 ISC.

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Table 14-2862. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DC0h

Figure 14-953. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
89h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2864. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2864. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.955 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L Register (Offset = 7DD0h) [reset = 0h]

Register Description: The ISC Region 14 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 14 ISC.

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Table 14-2865. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DD0h

Figure 14-954. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2867. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.956 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H Register (Offset = 7DD4h) [reset = 0h]

Register Description: The ISC Region 14 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 14 ISC.

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Table 14-2868. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DD4h

Figure 14-955. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2870. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.957 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L Register (Offset = 7DD8h) [reset = FFFh]

Register Description: The ISC Region 14 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 14 ISC.

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Table 14-2871. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DD8h

Figure 14-956. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2873. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.958 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H Register (Offset = 7DDCh) [reset = 0h]

Register Description: The ISC Region 14 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 14 ISC.

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Table 14-2874. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DDCh

Figure 14-957. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2876. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.959 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Register (Offset = 7DE0h) [reset = 8900h]

Register Description: The ISC Region 15 Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 15 ISC.

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Table 14-2877. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DE0h

Figure 14-958. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
89h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2879. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2879. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	89h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.960 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L Register (Offset = 7DF0h) [reset = 0h]

Register Description: The ISC Region 15 Start Address Low Register defines the start address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 15 ISC.

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Table 14-2880. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DF0h

Figure 14-959. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2882. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.961 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H Register (Offset = 7DF4h) [reset = 0h]

Register Description: The ISC Region 15 Start Address High Register defines the start address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 15 ISC.

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Table 14-2883. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DF4h

Figure 14-960. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2885. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.962 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L Register (Offset = 7DF8h) [reset = FFFh]

Register Description: The ISC Region 15 End Address Low Register defines the end included address bits 31 to 0 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 15 ISC.

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Table 14-2886. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DF8h

Figure 14-961. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2888. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.963 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H Register (Offset = 7DFCh) [reset = 0h]

Register Description: The ISC Region 15 End Address High Register defines the end address bits 47 to 32 for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 15 ISC.

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Table 14-2889. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7DFCh

Figure 14-962. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2891. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.964 CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Register (Offset = 7E00h) [reset = 894Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iicss_g_16ff_main_1.pr1_ext_vbusm region 16 ISC.

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Table 14-2892. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 7E00h

Figure 14-963. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
89h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2894. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2894. CBASS_ISC_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	89h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.965 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_CONTROL Register (Offset = 8000h) [reset = B300h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 0 ISC.

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Table 14-2895. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8000h

Figure 14-964. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2897. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2897. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.966 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_L Register (Offset = 8010h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 0 ISC.

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Table 14-2898. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8010h

Figure 14-965. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2900. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.967 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_H Register (Offset = 8014h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 0 ISC.

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Table 14-2901. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8014h

Figure 14-966. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2903. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.968 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_L Register (Offset = 8018h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 0 ISC.

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Table 14-2904. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8018h

Figure 14-967. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2906. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.969 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_H Register (Offset = 801Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 0 ISC.

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Table 14-2907. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 801Ch

Figure 14-968. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2909. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.970 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_CONTROL Register (Offset = 8020h) [reset = B300h]

Register Description: The ISC Region 1 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 1 ISC.

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Table 14-2910. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8020h

Figure 14-969. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B3h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2912. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2912. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.971 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_L Register (Offset = 8030h) [reset = 0h]

Register Description: The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 1 ISC.

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Table 14-2913. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8030h

Figure 14-970. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2915. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.972 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_H Register (Offset = 8034h) [reset = 0h]

Register Description: The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 1 ISC.

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Table 14-2916. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8034h

Figure 14-971. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2918. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.973 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_L Register (Offset = 8038h) [reset = FFFh]

Register Description: The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 1 ISC.

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Table 14-2919. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8038h

Figure 14-972. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2921. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.974 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_H Register (Offset = 803Ch) [reset = 0h]

Register Description: The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 1 ISC.

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Table 14-2922. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 803Ch

Figure 14-973. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2924. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.975 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_CONTROL Register (Offset = 8040h) [reset = B300h]

Register Description: The ISC Region 2 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 2 ISC.

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Table 14-2925. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8040h

Figure 14-974. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2927. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2927. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.976 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_L Register (Offset = 8050h) [reset = 0h]

Register Description: The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 2 ISC.

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Table 14-2928. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8050h

Figure 14-975. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2930. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.977 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_H Register (Offset = 8054h) [reset = 0h]

Register Description: The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 2 ISC.

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Table 14-2931. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8054h

Figure 14-976. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2933. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.978 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_L Register (Offset = 8058h) [reset = FFFh]

Register Description: The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 2 ISC.

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Table 14-2934. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8058h

Figure 14-977. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2936. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.979 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_H Register (Offset = 805Ch) [reset = 0h]

Register Description: The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 2 ISC.

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Table 14-2937. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 805Ch

Figure 14-978. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2939. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.980 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_CONTROL Register (Offset = 8060h) [reset = B300h]

Register Description: The ISC Region 3 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 3 ISC.

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Table 14-2940. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8060h

Figure 14-979. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B3h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2942. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2942. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.981 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_L Register (Offset = 8070h) [reset = 0h]

Register Description: The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 3 ISC.

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Table 14-2943. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8070h

Figure 14-980. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2945. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.982 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_H Register (Offset = 8074h) [reset = 0h]

Register Description: The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 3 ISC.

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Table 14-2946. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8074h

Figure 14-981. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2948. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.983 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_L Register (Offset = 8078h) [reset = FFFh]

Register Description: The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 3 ISC.

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Table 14-2949. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8078h

Figure 14-982. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2951. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.984 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_H Register (Offset = 807Ch) [reset = 0h]

Register Description: The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 3 ISC.

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Table 14-2952. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 807Ch

Figure 14-983. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2954. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.985 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_CONTROL Register (Offset = 8080h) [reset = B300h]

Register Description: The ISC Region 4 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 4 ISC.

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Table 14-2955. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8080h

Figure 14-984. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2957. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2957. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.986 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_L Register (Offset = 8090h) [reset = 0h]

Register Description: The ISC Region 4 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 4 ISC.

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Table 14-2958. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8090h

Figure 14-985. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2960. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.987 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_H Register (Offset = 8094h) [reset = 0h]

Register Description: The ISC Region 4 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 4 ISC.

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Table 14-2961. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8094h

Figure 14-986. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2963. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.988 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_L Register (Offset = 8098h) [reset = FFFh]

Register Description: The ISC Region 4 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 4 ISC.

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Table 14-2964. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8098h

Figure 14-987. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2966. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.989 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_H Register (Offset = 809Ch) [reset = 0h]

Register Description: The ISC Region 4 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 4 ISC.

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Table 14-2967. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 809Ch

Figure 14-988. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2969. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.990 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_CONTROL Register (Offset = 80A0h) [reset = B300h]

Register Description: The ISC Region 5 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 5 ISC.

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Table 14-2970. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80A0h

Figure 14-989. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B3h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2972. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2972. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.991 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_L Register (Offset = 80B0h) [reset = 0h]

Register Description: The ISC Region 5 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 5 ISC.

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Table 14-2973. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80B0h

Figure 14-990. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2975. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.992 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_H Register (Offset = 80B4h) [reset = 0h]

Register Description: The ISC Region 5 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 5 ISC.

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Table 14-2976. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80B4h

Figure 14-991. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2978. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.993 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_L Register (Offset = 80B8h) [reset = FFFh]

Register Description: The ISC Region 5 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 5 ISC.

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Table 14-2979. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80B8h

Figure 14-992. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2981. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.994 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_H Register (Offset = 80BCh) [reset = 0h]

Register Description: The ISC Region 5 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 5 ISC.

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Table 14-2982. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80BCh

Figure 14-993. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2984. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.995 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_CONTROL Register (Offset = 80C0h) [reset = B300h]

Register Description: The ISC Region 6 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 6 ISC.

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Table 14-2985. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80C0h

Figure 14-994. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B3h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2987. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2987. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.996 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_L Register (Offset = 80D0h) [reset = 0h]

Register Description: The ISC Region 6 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 6 ISC.

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Table 14-2988. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80D0h

Figure 14-995. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2990. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.997 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_H Register (Offset = 80D4h) [reset = 0h]

Register Description: The ISC Region 6 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 6 ISC.

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Table 14-2991. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80D4h

Figure 14-996. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2993. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.998 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_L Register (Offset = 80D8h) [reset = FFFh]

Register Description: The ISC Region 6 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 6 ISC.

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Table 14-2994. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80D8h

Figure 14-997. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2996. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.999 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_H Register (Offset = 80DCh) [reset = 0h]

Register Description: The ISC Region 6 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 6 ISC.

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Table 14-2997. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80DCh

Figure 14-998. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2999. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1000 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_CONTROL Register (Offset = 80E0h) [reset = B300h]

Register Description: The ISC Region 7 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 7 ISC.

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Table 14-3000. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80E0h

Figure 14-999. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3002. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3002. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1001 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_L Register (Offset = 80F0h) [reset = 0h]

Register Description: The ISC Region 7 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 7 ISC.

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Table 14-3003. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80F0h

Figure 14-1000. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3005. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1002 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_H Register (Offset = 80F4h) [reset = 0h]

Register Description: The ISC Region 7 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 7 ISC.

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Table 14-3006. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80F4h

Figure 14-1001. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3008. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1003 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_L Register (Offset = 80F8h) [reset = FFFh]

Register Description: The ISC Region 7 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 7 ISC.

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Table 14-3009. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80F8h

Figure 14-1002. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3011. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1004 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_H Register (Offset = 80FCh) [reset = 0h]

Register Description: The ISC Region 7 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 7 ISC.

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Table 14-3012. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 80FCh

Figure 14-1003. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3014. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1005 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_DEF_CONTROL Register (Offset = 8100h) [reset = B34Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_rd region 8 ISC.

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Table 14-3015. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8100h

Figure 14-1004. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3017. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3017. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	B3h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1006 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_CONTROL Register (Offset = 8400h) [reset = B300h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 0 ISC.

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Table 14-3018. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8400h

Figure 14-1005. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B3h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3020. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3020. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1007 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 8410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 0 ISC.

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Table 14-3021. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8410h

Figure 14-1006. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3023. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1008 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 8414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 0 ISC.

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Table 14-3024. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8414h

Figure 14-1007. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3026. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1009 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 8418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 0 ISC.

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Table 14-3027. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8418h

Figure 14-1008. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3029. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1010 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 841Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 0 ISC.

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Table 14-3030. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 841Ch

Figure 14-1009. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3032. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1011 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_CONTROL Register (Offset = 8420h) [reset = B300h]

Register Description: The ISC Region 1 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 1 ISC.

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Table 14-3033. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8420h

Figure 14-1010. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3035. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3035. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1012 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_L Register (Offset = 8430h) [reset = 0h]

Register Description: The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 1 ISC.

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Table 14-3036. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8430h

Figure 14-1011. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3038. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1013 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_H Register (Offset = 8434h) [reset = 0h]

Register Description: The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 1 ISC.

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Table 14-3039. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8434h

Figure 14-1012. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3041. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1014 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_L Register (Offset = 8438h) [reset = FFFh]

Register Description: The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 1 ISC.

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Table 14-3042. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8438h

Figure 14-1013. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3044. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1015 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_H Register (Offset = 843Ch) [reset = 0h]

Register Description: The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 1 ISC.

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Table 14-3045. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 843Ch

Figure 14-1014. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3047. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1016 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_CONTROL Register (Offset = 8440h) [reset = B300h]

Register Description: The ISC Region 2 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 2 ISC.

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Table 14-3048. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8440h

Figure 14-1015. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3050. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3050. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1017 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_L Register (Offset = 8450h) [reset = 0h]

Register Description: The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 2 ISC.

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Table 14-3051. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8450h

Figure 14-1016. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3053. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1018 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_H Register (Offset = 8454h) [reset = 0h]

Register Description: The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 2 ISC.

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Table 14-3054. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8454h

Figure 14-1017. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3056. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1019 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_L Register (Offset = 8458h) [reset = FFFh]

Register Description: The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 2 ISC.

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Table 14-3057. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8458h

Figure 14-1018. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3059. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1020 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_H Register (Offset = 845Ch) [reset = 0h]

Register Description: The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 2 ISC.

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Table 14-3060. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 845Ch

Figure 14-1019. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3062. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1021 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_CONTROL Register (Offset = 8460h) [reset = B300h]

Register Description: The ISC Region 3 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 3 ISC.

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Table 14-3063. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8460h

Figure 14-1020. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3065. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3065. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1022 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_L Register (Offset = 8470h) [reset = 0h]

Register Description: The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 3 ISC.

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Table 14-3066. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8470h

Figure 14-1021. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3068. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1023 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_H Register (Offset = 8474h) [reset = 0h]

Register Description: The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 3 ISC.

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Table 14-3069. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8474h

Figure 14-1022. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3071. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1024 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_L Register (Offset = 8478h) [reset = FFFh]

Register Description: The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 3 ISC.

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Table 14-3072. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8478h

Figure 14-1023. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3074. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1025 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_H Register (Offset = 847Ch) [reset = 0h]

Register Description: The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 3 ISC.

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Table 14-3075. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 847Ch

Figure 14-1024. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3077. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1026 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_CONTROL Register (Offset = 8480h) [reset = B300h]

Register Description: The ISC Region 4 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 4 ISC.

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Table 14-3078. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8480h

Figure 14-1025. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B3h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3080. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3080. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1027 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_L Register (Offset = 8490h) [reset = 0h]

Register Description: The ISC Region 4 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 4 ISC.

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Table 14-3081. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8490h

Figure 14-1026. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3083. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1028 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_H Register (Offset = 8494h) [reset = 0h]

Register Description: The ISC Region 4 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 4 ISC.

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Table 14-3084. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8494h

Figure 14-1027. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3086. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1029 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_L Register (Offset = 8498h) [reset = FFFh]

Register Description: The ISC Region 4 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 4 ISC.

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Table 14-3087. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8498h

Figure 14-1028. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3089. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1030 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_H Register (Offset = 849Ch) [reset = 0h]

Register Description: The ISC Region 4 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 4 ISC.

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Table 14-3090. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 849Ch

Figure 14-1029. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3092. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1031 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_CONTROL Register (Offset = 84A0h) [reset = B300h]

Register Description: The ISC Region 5 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 5 ISC.

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Table 14-3093. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84A0h

Figure 14-1030. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3095. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3095. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1032 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_L Register (Offset = 84B0h) [reset = 0h]

Register Description: The ISC Region 5 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 5 ISC.

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Table 14-3096. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84B0h

Figure 14-1031. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3098. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1033 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_H Register (Offset = 84B4h) [reset = 0h]

Register Description: The ISC Region 5 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 5 ISC.

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Table 14-3099. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84B4h

Figure 14-1032. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3101. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1034 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_L Register (Offset = 84B8h) [reset = FFFh]

Register Description: The ISC Region 5 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 5 ISC.

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Table 14-3102. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84B8h

Figure 14-1033. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3104. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1035 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_H Register (Offset = 84BCh) [reset = 0h]

Register Description: The ISC Region 5 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 5 ISC.

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Table 14-3105. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84BCh

Figure 14-1034. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3107. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1036 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_CONTROL Register (Offset = 84C0h) [reset = B300h]

Register Description: The ISC Region 6 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 6 ISC.

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Table 14-3108. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84C0h

Figure 14-1035. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3110. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3110. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1037 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_L Register (Offset = 84D0h) [reset = 0h]

Register Description: The ISC Region 6 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 6 ISC.

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Table 14-3111. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84D0h

Figure 14-1036. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3113. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1038 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_H Register (Offset = 84D4h) [reset = 0h]

Register Description: The ISC Region 6 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 6 ISC.

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Table 14-3114. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84D4h

Figure 14-1037. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3116. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1039 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_L Register (Offset = 84D8h) [reset = FFFh]

Register Description: The ISC Region 6 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 6 ISC.

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Table 14-3117. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84D8h

Figure 14-1038. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3119. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1040 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_H Register (Offset = 84DCh) [reset = 0h]

Register Description: The ISC Region 6 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 6 ISC.

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Table 14-3120. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84DCh

Figure 14-1039. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3122. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1041 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_CONTROL Register (Offset = 84E0h) [reset = B300h]

Register Description: The ISC Region 7 Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 7 ISC.

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Table 14-3123. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84E0h

Figure 14-1040. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3125. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3125. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B3h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1042 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_L Register (Offset = 84F0h) [reset = 0h]

Register Description: The ISC Region 7 Start Address Low Register defines the start address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 7 ISC.

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Table 14-3126. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84F0h

Figure 14-1041. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3128. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1043 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_H Register (Offset = 84F4h) [reset = 0h]

Register Description: The ISC Region 7 Start Address High Register defines the start address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 7 ISC.

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Table 14-3129. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84F4h

Figure 14-1042. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3131. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1044 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_L Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_L Register (Offset = 84F8h) [reset = FFFh]

Register Description: The ISC Region 7 End Address Low Register defines the end included address bits 31 to 0 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 7 ISC.

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Table 14-3132. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84F8h

Figure 14-1043. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3134. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1045 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_H Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_H Register (Offset = 84FCh) [reset = 0h]

Register Description: The ISC Region 7 End Address High Register defines the end address bits 47 to 32 for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 7 ISC.

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Table 14-3135. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 84FCh

Figure 14-1044. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3137. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1046 CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_DEF_CONTROL Register (Offset = 8500h) [reset = B34Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipcie_g2x1_64_main_0.pcie_mst_wr region 8 ISC.

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Table 14-3138. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8500h

Figure 14-1045. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3140. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3140. CBASS_ISC_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	B3h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1047 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register (Offset = 8800h) [reset = 8100h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-3141. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8800h

Figure 14-1046. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
81h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3143. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3143. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	81h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1048 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 8810h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-3144. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8810h

Figure 14-1047. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3146. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1049 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 8814h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-3147. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8814h

Figure 14-1048. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3149. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1050 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 8818h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-3150. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8818h

Figure 14-1049. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3152. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1051 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 881Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iemmcsd4ss_main_0.emmcsdss_wr region 0 ISC.

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Table 14-3153. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 881Ch

Figure 14-1050. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3155. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1052 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register (Offset = 8820h) [reset = 814Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iemmcsd4ss_main_0.emmcsdss_wr region 1 ISC.

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Table 14-3156. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8820h

Figure 14-1051. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">81h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R</td><td>R/W1TS</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td colspan="4">Ah</td></tr>
</table>

Table 14-3158. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3158. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	81h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1053 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register (Offset = 8C00h) [reset = 8100h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-3159. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8C00h

Figure 14-1052. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
81h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3161. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3161. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	81h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1054 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register (Offset = 8C10h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-3162. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8C10h

Figure 14-1053. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3164. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1055 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register (Offset = 8C14h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-3165. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8C14h

Figure 14-1054. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3167. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1056 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register (Offset = 8C18h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-3168. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8C18h

Figure 14-1055. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3170. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1057 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register (Offset = 8C1Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iemmcsd4ss_main_0.emmcsdss_rd region 0 ISC.

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Table 14-3171. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8C1Ch

Figure 14-1056. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3173. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1058 CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register (Offset = 8C20h) [reset = 814Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iemmcsd4ss_main_0.emmcsdss_rd region 1 ISC.

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Table 14-3174. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 8C20h

Figure 14-1057. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
81h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3176. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3176. CBASS_ISC_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	81h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1059 CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Register

CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Register (Offset = 9000h) [reset = 9800h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Isa2_ul_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-3177. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9000h

Figure 14-1058. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
98h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3179. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3179. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	98h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1060 CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L Register (Offset = 9010h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Isa2_ul_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-3180. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9010h

Figure 14-1059. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3182. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1061 CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H Register (Offset = 9014h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Isa2_ul_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-3183. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9014h

Figure 14-1060. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3185. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1062 CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L Register (Offset = 9018h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Isa2_ul_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-3186. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9018h

Figure 14-1061. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3188. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1063 CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H Register (Offset = 901Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Isa2_ul_main_0.ctxcach_ext_dma region 0 ISC.

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Table 14-3189. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 901Ch

Figure 14-1062. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3191. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1064 CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Register (Offset = 9020h) [reset = 984Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Isa2_ul_main_0.ctxcach_ext_dma region 1 ISC.

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Table 14-3192. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9020h

Figure 14-1063. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
98h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3194. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3194. CBASS_ISC_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	98h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1065 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Register (Offset = 9400h) [reset = 9B00h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-3195. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9400h

Figure 14-1064. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3197. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3197. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1066 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L Register (Offset = 9410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-3198. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9410h

Figure 14-1065. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3200. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1067 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H Register (Offset = 9414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-3201. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9414h

Figure 14-1066. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3203. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1068 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L Register (Offset = 9418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-3204. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9418h

Figure 14-1067. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3206. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1069 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H Register (Offset = 941Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 0 ISC.

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Table 14-3207. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 941Ch

Figure 14-1068. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3209. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1070 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_CONTROL Register (Offset = 9420h) [reset = 9B00h]

Register Description: The ISC Region 1 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 1 ISC.

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Table 14-3210. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9420h

Figure 14-1069. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3212. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3212. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1071 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_L Register (Offset = 9430h) [reset = 0h]

Register Description: The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 1 ISC.

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Table 14-3213. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9430h

Figure 14-1070. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3215. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1072 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_H Register (Offset = 9434h) [reset = 0h]

Register Description: The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 1 ISC.

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Table 14-3216. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9434h

Figure 14-1071. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3218. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1073 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_L Register (Offset = 9438h) [reset = FFFh]

Register Description: The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 1 ISC.

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Table 14-3219. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9438h

Figure 14-1072. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3221. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1074 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_H Register (Offset = 943Ch) [reset = 0h]

Register Description: The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 1 ISC.

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Table 14-3222. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 943Ch

Figure 14-1073. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3224. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1075 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_CONTROL Register (Offset = 9440h) [reset = 9B00h]

Register Description: The ISC Region 2 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 2 ISC.

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Table 14-3225. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9440h

Figure 14-1074. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3227. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3227. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1076 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_L Register (Offset = 9450h) [reset = 0h]

Register Description: The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 2 ISC.

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Table 14-3228. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9450h

Figure 14-1075. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3230. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1077 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_H Register (Offset = 9454h) [reset = 0h]

Register Description: The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 2 ISC.

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Table 14-3231. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9454h

Figure 14-1076. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3233. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1078 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_L Register (Offset = 9458h) [reset = FFFh]

Register Description: The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 2 ISC.

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Table 14-3234. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9458h

Figure 14-1077. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3236. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1079 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_H Register (Offset = 945Ch) [reset = 0h]

Register Description: The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 2 ISC.

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Table 14-3237. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 945Ch

Figure 14-1078. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3239. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1080 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_CONTROL Register (Offset = 9460h) [reset = 9B00h]

Register Description: The ISC Region 3 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 3 ISC.

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Table 14-3240. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9460h

Figure 14-1079. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3242. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3242. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1081 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_L Register (Offset = 9470h) [reset = 0h]

Register Description: The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 3 ISC.

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Table 14-3243. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9470h

Figure 14-1080. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3245. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1082 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_H Register (Offset = 9474h) [reset = 0h]

Register Description: The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 3 ISC.

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Table 14-3246. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9474h

Figure 14-1081. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3248. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1083 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_L Register (Offset = 9478h) [reset = FFFh]

Register Description: The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 3 ISC.

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Table 14-3249. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9478h

Figure 14-1082. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3251. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1084 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_H Register (Offset = 947Ch) [reset = 0h]

Register Description: The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 3 ISC.

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Table 14-3252. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 947Ch

Figure 14-1083. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3254. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1085 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_CONTROL Register (Offset = 9480h) [reset = 9B00h]

Register Description: The ISC Region 4 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 4 ISC.

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Table 14-3255. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9480h

Figure 14-1084. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3257. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3257. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1086 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_L Register (Offset = 9490h) [reset = 0h]

Register Description: The ISC Region 4 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 4 ISC.

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Table 14-3258. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9490h

Figure 14-1085. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3260. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1087 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_H Register (Offset = 9494h) [reset = 0h]

Register Description: The ISC Region 4 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 4 ISC.

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Table 14-3261. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9494h

Figure 14-1086. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3263. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1088 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_L Register (Offset = 9498h) [reset = FFFh]

Register Description: The ISC Region 4 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 4 ISC.

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Table 14-3264. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9498h

Figure 14-1087. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3266. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1089 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_H Register (Offset = 949Ch) [reset = 0h]

Register Description: The ISC Region 4 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 4 ISC.

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Table 14-3267. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 949Ch

Figure 14-1088. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3269. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1090 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_CONTROL Register (Offset = 94A0h) [reset = 9B00h]

Register Description: The ISC Region 5 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 5 ISC.

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Table 14-3270. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94A0h

Figure 14-1089. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3272. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3272. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1091 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_L Register (Offset = 94B0h) [reset = 0h]

Register Description: The ISC Region 5 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 5 ISC.

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Table 14-3273. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94B0h

Figure 14-1090. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3275. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1092 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_H Register (Offset = 94B4h) [reset = 0h]

Register Description: The ISC Region 5 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 5 ISC.

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Table 14-3276. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94B4h

Figure 14-1091. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3278. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1093 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_L Register (Offset = 94B8h) [reset = FFFh]

Register Description: The ISC Region 5 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 5 ISC.

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Table 14-3279. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94B8h

Figure 14-1092. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3281. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1094 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_H Register (Offset = 94BCh) [reset = 0h]

Register Description: The ISC Region 5 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 5 ISC.

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Table 14-3282. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94BCh

Figure 14-1093. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3284. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1095 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_CONTROL Register (Offset = 94C0h) [reset = 9B00h]

Register Description: The ISC Region 6 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 6 ISC.

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Table 14-3285. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94C0h

Figure 14-1094. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3287. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3287. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1096 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_L Register (Offset = 94D0h) [reset = 0h]

Register Description: The ISC Region 6 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 6 ISC.

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Table 14-3288. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94D0h

Figure 14-1095. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3290. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1097 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_H Register (Offset = 94D4h) [reset = 0h]

Register Description: The ISC Region 6 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 6 ISC.

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Table 14-3291. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94D4h

Figure 14-1096. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3293. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1098 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_L Register (Offset = 94D8h) [reset = FFFh]

Register Description: The ISC Region 6 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 6 ISC.

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Table 14-3294. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94D8h

Figure 14-1097. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3296. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1099 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_H Register (Offset = 94DCh) [reset = 0h]

Register Description: The ISC Region 6 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 6 ISC.

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Table 14-3297. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94DCh

Figure 14-1098. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3299. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1100 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_CONTROL Register (Offset = 94E0h) [reset = 9B00h]

Register Description: The ISC Region 7 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 7 ISC.

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Table 14-3300. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94E0h

Figure 14-1099. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3302. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3302. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1101 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_L Register (Offset = 94F0h) [reset = 0h]

Register Description: The ISC Region 7 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 7 ISC.

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Table 14-3303. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94F0h

Figure 14-1100. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3305. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1102 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_H Register (Offset = 94F4h) [reset = 0h]

Register Description: The ISC Region 7 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 7 ISC.

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Table 14-3306. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94F4h

Figure 14-1101. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3308. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1103 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_L Register (Offset = 94F8h) [reset = FFFh]

Register Description: The ISC Region 7 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 7 ISC.

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Table 14-3309. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94F8h

Figure 14-1102. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3311. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1104 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_H Register (Offset = 94FCh) [reset = 0h]

Register Description: The ISC Region 7 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 7 ISC.

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Table 14-3312. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 94FCh

Figure 14-1103. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3314. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1105 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Register (Offset = 9500h) [reset = 9B4Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstr0 region 8 ISC.

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Table 14-3315. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9500h

Figure 14-1104. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3317. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3317. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Bh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1106 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Register (Offset = 9800h) [reset = 9B00h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-3318. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9800h

Figure 14-1105. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3320. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3320. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1107 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L Register (Offset = 9810h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-3321. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9810h

Figure 14-1106. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3323. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1108 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H Register (Offset = 9814h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-3324. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9814h

Figure 14-1107. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3326. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1109 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L Register (Offset = 9818h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-3327. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9818h

Figure 14-1108. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3329. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1110 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H Register (Offset = 981Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 0 ISC.

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Table 14-3330. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 981Ch

Figure 14-1109. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3332. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1111 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_CONTROL Register (Offset = 9820h) [reset = 9B00h]

Register Description: The ISC Region 1 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 1 ISC.

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Table 14-3333. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9820h

Figure 14-1110. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3335. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3335. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1112 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_L Register (Offset = 9830h) [reset = 0h]

Register Description: The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 1 ISC.

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Table 14-3336. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9830h

Figure 14-1111. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3338. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1113 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_H Register (Offset = 9834h) [reset = 0h]

Register Description: The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 1 ISC.

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Table 14-3339. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9834h

Figure 14-1112. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3341. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1114 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_L Register (Offset = 9838h) [reset = FFFh]

Register Description: The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 1 ISC.

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Table 14-3342. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9838h

Figure 14-1113. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3344. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1115 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_H Register (Offset = 983Ch) [reset = 0h]

Register Description: The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 1 ISC.

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Table 14-3345. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 983Ch

Figure 14-1114. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3347. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1116 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_CONTROL Register (Offset = 9840h) [reset = 9B00h]

Register Description: The ISC Region 2 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 2 ISC.

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Table 14-3348. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9840h

Figure 14-1115. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3350. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3350. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1117 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_L Register (Offset = 9850h) [reset = 0h]

Register Description: The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 2 ISC.

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Table 14-3351. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9850h

Figure 14-1116. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3353. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1118 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_H Register (Offset = 9854h) [reset = 0h]

Register Description: The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 2 ISC.

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Table 14-3354. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9854h

Figure 14-1117. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3356. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1119 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_L Register (Offset = 9858h) [reset = FFFh]

Register Description: The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 2 ISC.

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Table 14-3357. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9858h

Figure 14-1118. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3359. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1120 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_H Register (Offset = 985Ch) [reset = 0h]

Register Description: The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 2 ISC.

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Table 14-3360. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 985Ch

Figure 14-1119. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3362. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1121 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_CONTROL Register (Offset = 9860h) [reset = 9B00h]

Register Description: The ISC Region 3 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 3 ISC.

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Table 14-3363. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9860h

Figure 14-1120. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3365. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3365. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1122 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_L Register (Offset = 9870h) [reset = 0h]

Register Description: The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 3 ISC.

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Table 14-3366. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9870h

Figure 14-1121. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3368. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1123 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_H Register (Offset = 9874h) [reset = 0h]

Register Description: The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 3 ISC.

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Table 14-3369. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9874h

Figure 14-1122. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3371. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1124 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_L Register (Offset = 9878h) [reset = FFFh]

Register Description: The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 3 ISC.

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Table 14-3372. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9878h

Figure 14-1123. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3374. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1125 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_H Register (Offset = 987Ch) [reset = 0h]

Register Description: The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 3 ISC.

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Table 14-3375. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 987Ch

Figure 14-1124. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3377. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1126 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_CONTROL Register (Offset = 9880h) [reset = 9B00h]

Register Description: The ISC Region 4 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 4 ISC.

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Table 14-3378. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9880h

Figure 14-1125. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3380. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3380. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1127 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_L Register (Offset = 9890h) [reset = 0h]

Register Description: The ISC Region 4 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 4 ISC.

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Table 14-3381. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9890h

Figure 14-1126. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3383. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1128 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_H Register (Offset = 9894h) [reset = 0h]

Register Description: The ISC Region 4 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 4 ISC.

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Table 14-3384. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9894h

Figure 14-1127. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3386. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1129 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_L Register (Offset = 9898h) [reset = FFFh]

Register Description: The ISC Region 4 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 4 ISC.

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Table 14-3387. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9898h

Figure 14-1128. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3389. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1130 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_H Register (Offset = 989Ch) [reset = 0h]

Register Description: The ISC Region 4 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 4 ISC.

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Table 14-3390. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 989Ch

Figure 14-1129. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3392. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1131 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_CONTROL Register (Offset = 98A0h) [reset = 9B00h]

Register Description: The ISC Region 5 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 5 ISC.

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Table 14-3393. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98A0h

Figure 14-1130. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3395. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3395. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1132 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_L Register (Offset = 98B0h) [reset = 0h]

Register Description: The ISC Region 5 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 5 ISC.

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Table 14-3396. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98B0h

Figure 14-1131. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3398. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1133 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_H Register (Offset = 98B4h) [reset = 0h]

Register Description: The ISC Region 5 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 5 ISC.

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Table 14-3399. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98B4h

Figure 14-1132. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3401. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1134 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_L Register (Offset = 98B8h) [reset = FFFh]

Register Description: The ISC Region 5 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 5 ISC.

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Table 14-3402. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98B8h

Figure 14-1133. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3404. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1135 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_H Register (Offset = 98BCh) [reset = 0h]

Register Description: The ISC Region 5 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 5 ISC.

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Table 14-3405. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98BCh

Figure 14-1134. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3407. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1136 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_CONTROL Register (Offset = 98C0h) [reset = 9B00h]

Register Description: The ISC Region 6 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 6 ISC.

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Table 14-3408. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98C0h

Figure 14-1135. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
9Bh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3410. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3410. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1137 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_L Register (Offset = 98D0h) [reset = 0h]

Register Description: The ISC Region 6 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 6 ISC.

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Table 14-3411. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98D0h

Figure 14-1136. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3413. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1138 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_H Register (Offset = 98D4h) [reset = 0h]

Register Description: The ISC Region 6 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 6 ISC.

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Table 14-3414. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98D4h

Figure 14-1137. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3416. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1139 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_L Register (Offset = 98D8h) [reset = FFFh]

Register Description: The ISC Region 6 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 6 ISC.

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Table 14-3417. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98D8h

Figure 14-1138. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3419. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1140 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_H Register (Offset = 98DCh) [reset = 0h]

Register Description: The ISC Region 6 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 6 ISC.

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Table 14-3420. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98DCh

Figure 14-1139. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3422. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1141 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_CONTROL Register (Offset = 98E0h) [reset = 9B00h]

Register Description: The ISC Region 7 Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 7 ISC.

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Table 14-3423. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98E0h

Figure 14-1140. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3425. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3425. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	9Bh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1142 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_L Register (Offset = 98F0h) [reset = 0h]

Register Description: The ISC Region 7 Start Address Low Register defines the start address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 7 ISC.

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Table 14-3426. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98F0h

Figure 14-1141. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3428. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1143 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_H Register (Offset = 98F4h) [reset = 0h]

Register Description: The ISC Region 7 Start Address High Register defines the start address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 7 ISC.

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Table 14-3429. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98F4h

Figure 14-1142. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3431. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1144 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_L Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_L Register (Offset = 98F8h) [reset = FFFh]

Register Description: The ISC Region 7 End Address Low Register defines the end included address bits 31 to 0 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 7 ISC.

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Table 14-3432. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98F8h

Figure 14-1143. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3434. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1145 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_H Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_H Register (Offset = 98FCh) [reset = 0h]

Register Description: The ISC Region 7 End Address High Register defines the end address bits 47 to 32 for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 7 ISC.

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Table 14-3435. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 98FCh

Figure 14-1144. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3437. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1146 CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Register (Offset = 9900h) [reset = 9B4Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iusb3p0ss64_16ffc_main_0.mstw0 region 8 ISC.

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Table 14-3438. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9900h

Figure 14-1145. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
9Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3440. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3440. CBASS_ISC_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	9Bh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1147 CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Register

CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Register (Offset = 9C00h) [reset = B000h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ij7_led_main_0.vbusp region 0 ISC.

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Table 14-3441. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9C00h

Figure 14-1146. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
B0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3443. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3443. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1148 CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L Register (Offset = 9C10h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ij7_led_main_0.vbusp region 0 ISC.

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Table 14-3444. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9C10h

Figure 14-1147. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3446. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1149 CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H Register (Offset = 9C14h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ij7_led_main_0.vbusp region 0 ISC.

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Table 14-3447. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9C14h

Figure 14-1148. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3449. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1150 CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L Register (Offset = 9C18h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ij7_led_main_0.vbusp region 0 ISC.

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Table 14-3450. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9C18h

Figure 14-1149. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3452. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1151 CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H Register (Offset = 9C1Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ij7_led_main_0.vbusp region 0 ISC.

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Table 14-3453. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9C1Ch

Figure 14-1150. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3455. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1152 CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Register (Offset = 9C20h) [reset = B04Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ij7_led_main_0.vbusp region 1 ISC.

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Table 14-3456. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 9C20h

Figure 14-1151. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B0h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3458. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3458. CBASS_ISC_IJ7_LED_MAIN_0_VBUSP_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	B0h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1153 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Register (Offset = A000h) [reset = B100h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-3459. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A000h

Figure 14-1152. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B1h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3461. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3461. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B1h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1154 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L Register (Offset = A010h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-3462. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A010h

Figure 14-1153. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3464. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1155 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H Register (Offset = A014h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-3465. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A014h

Figure 14-1154. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3467. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1156 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L Register (Offset = A018h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-3468. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A018h

Figure 14-1155. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3470. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1157 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H Register (Offset = A01Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Idebugss_k3_wrap_cv0_main_0.vbusmr region 0 ISC.

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Table 14-3471. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A01Ch

Figure 14-1156. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3473. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1158 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Register (Offset = A020h) [reset = B14Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Idebugss_k3_wrap_cv0_main_0.vbusmr region 1 ISC.

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Table 14-3474. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A020h

Figure 14-1157. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
B1h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3476. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3476. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	B1h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1159 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Register (Offset = A400h) [reset = B100h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-3477. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A400h

Figure 14-1158. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3479. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3479. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	B1h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1160 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L Register (Offset = A410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-3480. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A410h

Figure 14-1159. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3482. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1161 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H Register (Offset = A414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-3483. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A414h

Figure 14-1160. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3485. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1162 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L Register (Offset = A418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-3486. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A418h

Figure 14-1161. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3488. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1163 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H Register (Offset = A41Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Idebugss_k3_wrap_cv0_main_0.vbusmw region 0 ISC.

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Table 14-3489. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A41Ch

Figure 14-1162. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3491. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1164 CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Register (Offset = A420h) [reset = B14Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Idebugss_k3_wrap_cv0_main_0.vbusmw region 1 ISC.

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Table 14-3492. Instance Table

Instance Name	Physical Address
CBASS0_ISC	4588 A420h

Figure 14-1163. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R</td><td>R/W1TS</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td colspan="4">Ah</td></tr>
</table>

Table 14-3494. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3494. CBASS_ISC_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	B1h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1165 CBASS_GLB_PID Register

CBASS_GLB_PID Register (Offset = 0h) [reset = 6600A901h]

Register Description: The Revision Register contains the major and minor revisions for the module.

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Table 14-3495. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8000h

Figure 14-1164. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
15h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-3497. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	15h	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1166 CBASS_GLB_DESTINATION_ID Register

CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

Register Description: The Destination ID Register defines the destination ID value for error messages.

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Table 14-3498. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8004h

Figure 14-1165. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-3500. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1167 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

Register Description: The Exception Logging Control Register controls the exception logging.

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Table 14-3501. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8020h

Figure 14-1166. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-3503. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1168 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

Register Description: The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-3504. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8024h

Figure 14-1167. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-3506. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1169 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

Register Description: The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-3507. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8028h

Figure 14-1168. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-3509. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.1.1170 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

Register Description: The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-3510. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 802Ch

Figure 14-1169. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-3512. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1171 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

Register Description: The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-3513. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8030h

Figure 14-1170. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-3515. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1172 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

Register Description: The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-3516. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8034h

Figure 14-1171. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-3518. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3518. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1173 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

Register Description: The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-3519. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8038h

Figure 14-1172. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BYTECNT							
R							
0h							

Table 14-3521. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1174 CBASS_GLB_EXCEPTION_PEND_SET Register

CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

Register Description: The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-3522. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8040h

Figure 14-1173. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-3524. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1175 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

Register Description: The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-3525. Instance Table

Instance Name	Physical Address
CBASS0_GLB	45B0 8044h

Figure 14-1174. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-3527. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.1176 CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_MAP0 Register

CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_MAP0 Register (Offset = 500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator A53SS0 Read Port per channel

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Table 14-3528. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 0500h

Figure 14-1175. CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3530. CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3530. CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_R_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1177 CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_MAP0 Register

CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_MAP0 Register (Offset = 900h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator A53SS0 Write Port per channel

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Table 14-3531. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 0900h

Figure 14-1176. CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-3533. CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3533. CBASS_QOS_ISAM64_A53_256KB_WRAP_MAIN_0_A53_DUAL_WRAP_CBA_AXI_W_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1178 CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_MAP0 Register

CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_MAP0 Register (Offset = 1100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator MMCSD0 Write Port per channel

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Table 14-3534. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 1100h

Figure 14-1177. CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3536. CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-3536. CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_WR_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1179 CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_MAP0 Register

CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_MAP0 Register (Offset = 1500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator MMCSD0 Read Port per channel

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Table 14-3537. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 1500h

Figure 14-1178. CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-3539. CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-3539. CBASS_QOS_IEMMC8SS_16FFC_MAIN_0_EMMCSS_RD_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1180 CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_MAP0 Register

CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_MAP0 Register (Offset = 2100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator GICSS0 Write Port per channel

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Table 14-3540. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 2100h

Figure 14-1179. CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3542. CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-3542. CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_WR_VBUSM_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1181 CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_MAP0 Register

CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_MAP0 Register (Offset = 2500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator GICSS0 Read Port per channel

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Table 14-3543. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 2500h

Figure 14-1180. CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3545. CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-3545. CBASS_QOS_IGIC500SS_1_2_MAIN_0_MEM_RD_VBUSM_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1182 CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_RMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_RMST_MAP0 Register (Offset = 2900h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator R5FSS0 CPU0 Read Port per channel

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Table 14-3546. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 2900h

Figure 14-1181. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_RMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3548. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_RMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1183 CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_WMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_WMST_MAP0 Register (Offset = 2D00h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator R5FSS0 CPU0 Write Port per channel

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Table 14-3549. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 2D00h

Figure 14-1182. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_WMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3551. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_WMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1184 CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_RMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_RMST_MAP0 Register (Offset = 3D00h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator R5FSS0 CPU1 Read Port per channel

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Table 14-3552. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 3D00h

Figure 14-1183. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_RMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3554. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_RMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1185 CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_WMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_WMST_MAP0 Register (Offset = 4100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator R5FSS0 CPU1 Write Port per channel

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Table 14-3555. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 4100h

Figure 14-1184. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_WMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3557. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_WMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1186 CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_RMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_RMST_MAP0 Register (Offset = 5100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator R5FSS1 CPU0 Read Port per channel

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Table 14-3558. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 5100h

Figure 14-1185. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_RMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3560. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_RMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1187 CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_WMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_WMST_MAP0 Register (Offset = 5500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator R5FSS1 CPU0 Write Port per channel

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Table 14-3561. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 5500h

Figure 14-1186. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_WMST_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-3563. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_WMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1188 CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_RMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_RMST_MAP0 Register (Offset = 6500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator R5FSS1 CPU1 Read Port per channel

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Table 14-3564. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 6500h

Figure 14-1187. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_RMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3566. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_RMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1189 CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_WMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_WMST_MAP0 Register (Offset = 6900h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator R5FSS1 CPU1 Write Port per channel

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Table 14-3567. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 6900h

Figure 14-1188. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_WMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3569. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_WMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1190 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP0 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP0 Register (Offset = 7900h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3570. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7900h

Figure 14-1189. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3572. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1191 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP1 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP1 Register (Offset = 7904h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3573. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7904h

Figure 14-1190. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3575. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1192 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP2 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP2 Register (Offset = 7908h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3576. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7908h

Figure 14-1191. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3578. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1193 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP3 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP3 Register (Offset = 790Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3579. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 790Ch

Figure 14-1192. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3581. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1194 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP4 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP4 Register (Offset = 7910h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3582. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7910h

Figure 14-1193. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3584. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1195 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP5 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP5 Register (Offset = 7914h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3585. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7914h

Figure 14-1194. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3587. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1196 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP6 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP6 Register (Offset = 7918h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3588. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7918h

Figure 14-1195. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3590. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1197 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP7 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP7 Register (Offset = 791Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3591. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 791Ch

Figure 14-1196. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3593. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1198 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP8 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP8 Register (Offset = 7920h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3594. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7920h

Figure 14-1197. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3596. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1199 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP9 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP9 Register (Offset = 7924h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3597. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7924h

Figure 14-1198. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3599. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1200 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP10 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP10 Register (Offset = 7928h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3600. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7928h

Figure 14-1199. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3602. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1201 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP11 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP11 Register (Offset = 792Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3603. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 792Ch

Figure 14-1200. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3605. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1202 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP12 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP12 Register (Offset = 7930h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3606. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7930h

Figure 14-1201. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3608. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1203 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP13 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP13 Register (Offset = 7934h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3609. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7934h

Figure 14-1202. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3611. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1204 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP14 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP14 Register (Offset = 7938h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3612. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7938h

Figure 14-1203. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3614. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1205 CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP15 Register

CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP15 Register (Offset = 793Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG0 Port per channel

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Table 14-3615. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 793Ch

Figure 14-1204. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3617. CBASS_QOS_IICSS_G_16FF_MAIN_0_PR1_EXT_VBUSM_MAP15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1206 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP0 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP0 Register (Offset = 7D00h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3618. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D00h

Figure 14-1205. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3620. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1207 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP1 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP1 Register (Offset = 7D04h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3621. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D04h

Figure 14-1206. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3623. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1208 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP2 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP2 Register (Offset = 7D08h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3624. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D08h

Figure 14-1207. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3626. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1209 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP3 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP3 Register (Offset = 7D0Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3627. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D0Ch

Figure 14-1208. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3629. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1210 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP4 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP4 Register (Offset = 7D10h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3630. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D10h

Figure 14-1209. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3632. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1211 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP5 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP5 Register (Offset = 7D14h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3633. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D14h

Figure 14-1210. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3635. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1212 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP6 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP6 Register (Offset = 7D18h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3636. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D18h

Figure 14-1211. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3638. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1213 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP7 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP7 Register (Offset = 7D1Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3639. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D1Ch

Figure 14-1212. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3641. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1214 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP8 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP8 Register (Offset = 7D20h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3642. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D20h

Figure 14-1213. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3644. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1215 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP9 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP9 Register (Offset = 7D24h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3645. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D24h

Figure 14-1214. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3647. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1216 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP10 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP10 Register (Offset = 7D28h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3648. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D28h

Figure 14-1215. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3650. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1217 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP11 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP11 Register (Offset = 7D2Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3651. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D2Ch

Figure 14-1216. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3653. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1218 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP12 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP12 Register (Offset = 7D30h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3654. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D30h

Figure 14-1217. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3656. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1219 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP13 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP13 Register (Offset = 7D34h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3657. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D34h

Figure 14-1218. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3659. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1220 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP14 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP14 Register (Offset = 7D38h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3660. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D38h

Figure 14-1219. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3662. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1221 CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP15 Register

CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP15 Register (Offset = 7D3Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PRU_ICSSG1 Port per channel

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Table 14-3663. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 7D3Ch

Figure 14-1220. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
NONE	R/W			NONE			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h			

Table 14-3665. CBASS_QOS_IICSS_G_16FF_MAIN_1_PR1_EXT_VBUSM_MAP15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.1.1.1222 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP0 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP0 Register (Offset = 8100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Read Port per channel

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Table 14-3666. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8100h

Figure 14-1221. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-3668. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1223 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP1 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP1 Register (Offset = 8104h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Read Port per channel

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Table 14-3669. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8104h

Figure 14-1222. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3671. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1224 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP2 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP2 Register (Offset = 8108h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Read Port per channel

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Table 14-3672. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8108h

Figure 14-1223. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			

7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3674. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1225 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP3 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP3 Register (Offset = 810Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Read Port per channel

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Table 14-3675. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 810Ch

Figure 14-1224. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3677. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1226 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP4 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP4 Register (Offset = 8110h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Read Port per channel

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Table 14-3678. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8110h

Figure 14-1225. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3680. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1227 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP5 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP5 Register (Offset = 8114h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Read Port per channel

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Table 14-3681. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8114h

Figure 14-1226. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3683. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1228 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP6 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP6 Register (Offset = 8118h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Read Port per channel

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Table 14-3684. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8118h

Figure 14-1227. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-3686. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1229 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP7 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP7 Register (Offset = 811Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Read Port per channel

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Table 14-3687. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 811Ch

Figure 14-1228. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3689. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_RD_MAP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1230 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP0 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP0 Register (Offset = 8500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Write Port per channel

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Table 14-3690. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8500h

Figure 14-1229. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-3692. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1231 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP1 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP1 Register (Offset = 8504h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Write Port per channel

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Table 14-3693. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8504h

Figure 14-1230. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3695. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1232 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP2 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP2 Register (Offset = 8508h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Write Port per channel

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Table 14-3696. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8508h

Figure 14-1231. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3698. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1233 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP3 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP3 Register (Offset = 850Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Write Port per channel

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Table 14-3699. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 850Ch

Figure 14-1232. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3701. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1234 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP4 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP4 Register (Offset = 8510h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Write Port per channel

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Table 14-3702. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8510h

Figure 14-1233. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-3704. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1235 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP5 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP5 Register (Offset = 8514h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Write Port per channel

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Table 14-3705. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8514h

Figure 14-1234. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3707. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1236 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP6 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP6 Register (Offset = 8518h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Write Port per channel

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Table 14-3708. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8518h

Figure 14-1235. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3710. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1237 CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP7 Register

CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP7 Register (Offset = 851Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator PCIE0 Write Port per channel

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Table 14-3711. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 851Ch

Figure 14-1236. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3713. CBASS_QOS_IPCIE_G2X1_64_MAIN_0_PCIE_MST_WR_MAP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1238 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0 Register

CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0 Register (Offset = 8900h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator MMCSD1 Write Port per channel

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Table 14-3714. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8900h

Figure 14-1237. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3716. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_WR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1239 CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0 Register

CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0 Register (Offset = 8D00h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator MMCSD1 Read Port per channel

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Table 14-3717. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 8D00h

Figure 14-1238. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3719. CBASS_QOS_IEMMCSD4SS_MAIN_0_EMMCSDSS_RD_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1240 CBASS_QOS_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_MAP0 Register

CBASS_QOS_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_MAP0 Register (Offset = 9100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator Isa2_ul_main_0.ctxcach_ext_dma per channel.

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Table 14-3720. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9100h

Figure 14-1239. CBASS_QOS_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3722. CBASS_QOS_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-3722. CBASS_QOS_ISA2_UL_MAIN_0_CTXCACH_EXT_DMA_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1241 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP0 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP0 Register (Offset = 9500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-3723. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9500h

Figure 14-1240. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3725. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1242 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP1 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP1 Register (Offset = 9504h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-3726. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9504h

Figure 14-1241. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3728. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1243 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP2 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP2 Register (Offset = 9508h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-3729. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9508h

Figure 14-1242. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3731. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1244 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP3 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP3 Register (Offset = 950Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-3732. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 950Ch

Figure 14-1243. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3734. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1245 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP4 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP4 Register (Offset = 9510h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-3735. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9510h

Figure 14-1244. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3737. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1246 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP5 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP5 Register (Offset = 9514h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-3738. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9514h

Figure 14-1245. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3740. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1247 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP6 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP6 Register (Offset = 9518h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-3741. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9518h

Figure 14-1246. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3743. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1248 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP7 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP7 Register (Offset = 951Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Read Port per channel

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Table 14-3744. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 951Ch

Figure 14-1247. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3746. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTR0_MAP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1249 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP0 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP0 Register (Offset = 9900h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-3747. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9900h

Figure 14-1248. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3749. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1250 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP1 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP1 Register (Offset = 9904h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-3750. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9904h

Figure 14-1249. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3752. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1251 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP2 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP2 Register (Offset = 9908h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-3753. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9908h

Figure 14-1250. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3755. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1252 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP3 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP3 Register (Offset = 990Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-3756. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 990Ch

Figure 14-1251. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3758. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1253 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP4 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP4 Register (Offset = 9910h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-3759. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9910h

Figure 14-1252. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3761. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1254 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP5 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP5 Register (Offset = 9914h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-3762. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9914h

Figure 14-1253. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3764. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1255 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP6 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP6 Register (Offset = 9918h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-3765. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 9918h

Figure 14-1254. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3767. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1256 CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP7 Register

CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP7 Register (Offset = 991Ch) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator USB0 Write Port per channel

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Table 14-3768. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 991Ch

Figure 14-1255. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3770. CBASS_QOS_IUSB3P0SS64_16FFC_MAIN_0_MSTW0_MAP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1257 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Register

CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Register (Offset = A100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator DEBUGSS0 Read Port per channel

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Table 14-3771. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 A100h

Figure 14-1256. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3773. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-3773. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMR_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.1.1258 CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Register

CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Register (Offset = A500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator DEBUGSS0 Write Port per channel

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Table 14-3774. Instance Table

Instance Name	Physical Address
CBASS0_QOS	45D8 A500h

Figure 14-1257. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-3776. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-3776. CBASS_QOS_IDEBUGSS_K3_WRAP_CV0_MAIN_0_VBUSMW_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.2 MCU_CBASS Registers

14.1.2.1 MCU_CBASS Summary Table

Table 14-3777. MCU_CBASS0_ERR Registers, Base Address=0472 0000h, Length=1024

Offset	Length	Register Name	MCU_CBASS Physical Address
0h	32	CBASS_ERR_PID	0472 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0472 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0472 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0472 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0472 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0472 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0472 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0472 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0472 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0472 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0472 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0472 005Ch
60h	32	CBASS_ERR_EOI	0472 0060h

Table 14-3778. MCU_CBASS0_ISC Registers, Base Address=4583 0000h, Length=1024

Offset	Length	Register Name	MCU_CBASS Physical Address
0h	32	CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_CONTROL	4583 0000h
10h	32	CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_L	4583 0010h
14h	32	CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_H	4583 0014h
18h	32	CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_L	4583 0018h
1Ch	32	CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_H	4583 001Ch
20h	32	CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_DEF_CONTROL	4583 0020h

Table 14-3779. MCU_CBASS0_GLB Registers, Base Address=45B0 2000h, Length=1024

Offset	Length	Register Name	MCU_CBASS Physical Address
0h	32	CBASS_GLB_PID	45B0 2000h

Table 14-3780. MCU_CBASS0_QOS Registers, Base Address=45D3 0000h, Length=1024

Offset	Length	Register Name	MCU_CBASS Physical Address
100h	32	CBASS_QOS_IBLAZAR_MCU_0_VBUSP_M_MAP0	45D3 0100h

14.1.2.2 CBASS_ERR_PID Register

CBASS_ERR_PID Register (Offset = 0h) [reset = 6600A101h]

Register Description: The Revision Register contains the major and minor revisions for the module.

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Table 14-3781. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0000h

Figure 14-1258. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
14h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-3783. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
15:11	RTL	R	14h	RTL revision. Will vary depending on release. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.3 CBASS_ERR_DESTINATION_ID Register

CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

Register Description: The Destination ID Register defines the destination ID value for error messages.

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Table 14-3784. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0004h

Figure 14-1259. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEST_ID							
R/W							
0h							

Table 14-3786. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

Register Description: The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-3787. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0024h

Figure 14-1260. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-3789. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.5 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

Register Description: The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-3790. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0028h

Figure 14-1261. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-3792. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

Register Description: The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-3793. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 002Ch

Figure 14-1262. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3795. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

Register Description: The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-3796. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0030h

Figure 14-1263. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-3798. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

Register Description: The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-3799. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0034h

Figure 14-1264. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-3801. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

Table 14-3801. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.9 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

Register Description: The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-3802. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0038h

Figure 14-1265. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-3804. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.10 CBASS_ERR_ERR_INTR_RAW_STAT Register

CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

Register Description: Global Interrupt Raw Status Register

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Table 14-3805. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0050h

Figure 14-1266. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-3807. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.11 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

Register Description: Global Interrupt Enabled Status Register

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Table 14-3808. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0054h

Figure 14-1267. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-3810. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.12 CBASS_ERR_ERR_INTR_ENABLE_SET Register

CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Register Description: Interrupt Enable Set Register

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Table 14-3811. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0058h

Figure 14-1268. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-3813. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.13 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Register Description: Interrupt Enable Clear Register

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Table 14-3814. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 005Ch

Figure 14-1269. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-3816. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.14 CBASS_ERR_EOI Register

CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Register Description: EOI Register

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Table 14-3817. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ERR	0472 0060h

Figure 14-1270. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-3819. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register Reset Source: scrp_mcu_clk4_rst_mod_g_rst_n

14.1.2.15 CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_CONTROL Register

CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_CONTROL Register (Offset = 0h) [reset = 6400h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Iblazar_mcu_0.vbusp_m region 0 ISC.

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Table 14-3820. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ISC	4583 0000h

Figure 14-1271. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
64h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3822. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3822. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	64h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.16 CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Iblazar_mcu_0.vbusp_m region 0 ISC.

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Table 14-3823. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ISC	4583 0010h

Figure 14-1272. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3825. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.17 CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Iblazar_mcu_0.vbusp_m region 0 ISC.

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Table 14-3826. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ISC	4583 0014h

Figure 14-1273. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3828. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.18 CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Iblazar_mcu_0.vbusp_m region 0 ISC.

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Table 14-3829. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ISC	4583 0018h

Figure 14-1274. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3831. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.19 CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Iblazar_mcu_0.vbusp_m region 0 ISC.

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Table 14-3832. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ISC	4583 001Ch

Figure 14-1275. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3834. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.20 CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_DEF_CONTROL Register (Offset = 20h) [reset = 644Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Iblazar_mcu_0.vbusp_m region 1 ISC.

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Table 14-3835. Instance Table

Instance Name	Physical Address
MCU_CBASS0_ISC	4583 0020h

Figure 14-1276. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
64h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3837. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3837. CBASS_ISC_IBLAZAR_MCU_0_VBUSP_M_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	64h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.21 CBASS_GLB_PID Register

CBASS_GLB_PID Register (Offset = 0h) [reset = 6600A101h]

Register Description: The Revision Register contains the major and minor revisions for the module.

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Table 14-3838. Instance Table

Instance Name	Physical Address
MCU_CBASS0_GLB	45B0 2000h

Figure 14-1277. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
14h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-3840. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	14h	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.2.22 CBASS_QOS_IBLAZAR_MCU_0_VBUSP_M_MAP0 Register

CBASS_QOS_IBLAZAR_MCU_0_VBUSP_M_MAP0 Register (Offset = 100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator Iblazar_mcu_0.vbusp_m per channel.

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Table 14-3841. Instance Table

Instance Name	Physical Address
MCU_CBASS0_QOS	45D3 0100h

Figure 14-1278. CBASS_QOS_IBLAZAR_MCU_0_VBUSP_M_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
RESERVED					RESERVED		
NONE					R/W		
0h					0h		

Table 14-3843. CBASS_QOS_IBLAZAR_MCU_0_VBUSP_M_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	RESERVED	NONE	0h	Reserved

14.1.3 cbass_fw

cbass_fw

14.1.3.1 cbass_fw Summaries

cbass_fw Summaries

Table 14-3844. CBASS_ERR Registers, Base Address=0022 0000h, Length=1024

Offset	Length	Register Name	CBASS_FW0 Physical Address
0h	32	CBASS_ERR_PID	0022 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0022 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0022 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0022 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0022 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0022 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0022 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0022 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0022 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0022 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0022 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0022 005Ch
60h	32	CBASS_ERR_EOI	0022 0060h

14.1.3.2 cbass_fw Registers

cbass_fw Registers

14.1.3.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 6600A901h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-3845. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0000h**

Figure 14-1279. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
15h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-3847. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
15:11	RTL	R	15h	RTL revision. Will vary depending on release. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-3848. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0004h**

Figure 14-1280. CBASS_ERR_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3850. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-3851. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0024h**

Figure 14-1281. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-3853. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-3854. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0028h**

Figure 14-1282. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-3856. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.3.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-3857. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 002Ch**

Figure 14-1283. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-3859. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-3860. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0030h**

Figure 14-1284. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-3862. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-3863. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0034h**

Figure 14-1285. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-3865. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

Table 14-3865. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-3866. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0038h**

Figure 14-1286. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-3868. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

Global Interrupt Raw Status Register

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Table 14-3869. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0050h**

Figure 14-1287. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-3871. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

Global Interrupt Enabled Status Register

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Table 14-3872. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0054h**

Figure 14-1288. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-3874. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Interrupt Enable Set Register

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Table 14-3875. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0058h**

Figure 14-1289. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-3877. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Interrupt Enable Clear Register

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Table 14-3878. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 005Ch**

Figure 14-1290. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-3880. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.3.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

EOI Register

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Table 14-3881. Instance Table

Instance Name	Physical Address
CBASS_FW0	**0022 0060h**

Figure 14-1291. CBASS_ERR_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3883. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register Reset Source: scrp_32b_clk4_rst_mod_g_rst_n

14.1.4 CBASS_INFRA Registers

14.1.4.1 CBASS_INFRA Summary Table

Table 14-3884. CBASS_INFRA1_ERR Registers, Base Address=0021 0000h, Length=1024

Offset	Length	Register Name	CBASS_INFRA Physical Address
0h	32	CBASS_ERR_PID	0021 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0021 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0021 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0021 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0021 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0021 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0021 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0021 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0021 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0021 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0021 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0021 005Ch
60h	32	CBASS_ERR_EOI	0021 0060h

Table 14-3885. CBASS_INFRA1_FW Registers, Base Address=4500 8000h, Length=4096

Offset	Length	Register Name	CBASS_INFRA Physical Address
800h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_CONTROL	4500 8800h
804h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_0	4500 8804h
808h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_1	4500 8808h
80Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_2	4500 880Ch
810h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_L	4500 8810h
814h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_H	4500 8814h
818h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_L	4500 8818h
81Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_H	4500 881Ch
820h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_CONTROL	4500 8820h
824h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_0	4500 8824h
828h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_1	4500 8828h
82Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_2	4500 882Ch
830h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_L	4500 8830h
834h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_H	4500 8834h
838h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_L	4500 8838h

Table 14-3885. CBASS_INFRA1_FW Registers, Base Address=4500 8000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_INFRA Physical Address
83Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_H	4500 883Ch
840h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_CONTROL	4500 8840h
844h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_0	4500 8844h
848h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_1	4500 8848h
84Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_2	4500 884Ch
850h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_L	4500 8850h
854h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_H	4500 8854h
858h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_L	4500 8858h
85Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_H	4500 885Ch
860h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_CONTROL	4500 8860h
864h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_0	4500 8864h
868h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_1	4500 8868h
86Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_2	4500 886Ch
870h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_L	4500 8870h
874h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_H	4500 8874h
878h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_L	4500 8878h
87Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_H	4500 887Ch
880h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_CONTROL	4500 8880h
884h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_0	4500 8884h
888h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_1	4500 8888h
88Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_2	4500 888Ch
890h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_L	4500 8890h
894h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_H	4500 8894h
898h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_L	4500 8898h
89Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_H	4500 889Ch
8A0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_CONTROL	4500 88A0h

Table 14-3885. CBASS_INFRA1_FW Registers, Base Address=4500 8000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_INFRA Physical Address
8A4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_0	4500 88A4h
8A8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_1	4500 88A8h
8ACh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_2	4500 88ACh
8B0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_L	4500 88B0h
8B4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_H	4500 88B4h
8B8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_L	4500 88B8h
8BCh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_H	4500 88BCh
8C0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_CONTROL	4500 88C0h
8C4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_0	4500 88C4h
8C8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_1	4500 88C8h
8CCh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_2	4500 88CCh
8D0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_L	4500 88D0h
8D4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_H	4500 88D4h
8D8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_L	4500 88D8h
8DCh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_H	4500 88DCh
8E0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_CONTROL	4500 88E0h
8E4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_0	4500 88E4h
8E8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_1	4500 88E8h
8ECh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_2	4500 88ECh
8F0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_L	4500 88F0h
8F4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_H	4500 88F4h
8F8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_L	4500 88F8h
8FCh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_H	4500 88FCh
C00h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_CONTROL	4500 8C00h
C04h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_0	4500 8C04h
C08h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_1	4500 8C08h

Table 14-3885. CBASS_INFRA1_FW Registers, Base Address=4500 8000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_INFRA Physical Address
C0Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_2	4500 8C0Ch
C10h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_L	4500 8C10h
C14h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_H	4500 8C14h
C18h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_L	4500 8C18h
C1Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_H	4500 8C1Ch
C20h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_CONTROL	4500 8C20h
C24h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_0	4500 8C24h
C28h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_1	4500 8C28h
C2Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_2	4500 8C2Ch
C30h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_L	4500 8C30h
C34h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_H	4500 8C34h
C38h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_L	4500 8C38h
C3Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_H	4500 8C3Ch
C40h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_CONTROL	4500 8C40h
C44h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_0	4500 8C44h
C48h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_1	4500 8C48h
C4Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_2	4500 8C4Ch
C50h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_L	4500 8C50h
C54h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_H	4500 8C54h
C58h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_L	4500 8C58h
C5Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_H	4500 8C5Ch
C60h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_CONTROL	4500 8C60h
C64h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_0	4500 8C64h
C68h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_1	4500 8C68h
C6Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_2	4500 8C6Ch
C70h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_L	4500 8C70h

Table 14-3885. CBASS_INFRA1_FW Registers, Base Address=4500 8000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_INFRA Physical Address
C74h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_H	4500 8C74h
C78h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_L	4500 8C78h
C7Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_H	4500 8C7Ch
C80h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_CONTROL	4500 8C80h
C84h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_0	4500 8C84h
C88h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_1	4500 8C88h
C8Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_2	4500 8C8Ch
C90h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_L	4500 8C90h
C94h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_H	4500 8C94h
C98h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_L	4500 8C98h
C9Ch	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_H	4500 8C9Ch
CA0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_CONTROL	4500 8CA0h
CA4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_0	4500 8CA4h
CA8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_1	4500 8CA8h
CACh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_2	4500 8CACh
CB0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_L	4500 8CB0h
CB4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_H	4500 8CB4h
CB8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_L	4500 8CB8h
CBCh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_H	4500 8CBCh
CC0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_CONTROL	4500 8CC0h
CC4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_0	4500 8CC4h
CC8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_1	4500 8CC8h
CCCh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_2	4500 8CCCh
CD0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_L	4500 8CD0h
CD4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_H	4500 8CD4h
CD8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_L	4500 8CD8h

Table 14-3885. CBASS_INFRA1_FW Registers, Base Address=4500 8000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_INFRA Physical Address
CDCh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_H	4500 8CDCh
CE0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_CONTROL	4500 8CE0h
CE4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_0	4500 8CE4h
CE8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_1	4500 8CE8h
CECh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_2	4500 8CECh
CF0h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_L	4500 8CF0h
CF4h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_H	4500 8CF4h
CF8h	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_L	4500 8CF8h
CFCh	32	CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_H	4500 8CFCh

Table 14-3886. CBASS_INFRA1_ISC Registers, Base Address=4582 0000h, Length=4096

Offset	Length	Register Name	CBASS_INFRA Physical Address
0h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL	4582 0000h
10h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L	4582 0010h
14h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H	4582 0014h
18h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L	4582 0018h
1Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H	4582 001Ch
20h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL	4582 0020h
400h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL	4582 0400h
410h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L	4582 0410h
414h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H	4582 0414h
418h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L	4582 0418h
41Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H	4582 041Ch
420h	32	CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL	4582 0420h
800h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL	4582 0800h
810h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L	4582 0810h
814h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H	4582 0814h

Table 14-3886. CBASS_INFRA1_ISC Registers, Base Address=4582 0000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_INFRA Physical Address
818h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L	4582 0818h
81Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H	4582 081Ch
820h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL	4582 0820h
C00h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL	4582 0C00h
C10h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L	4582 0C10h
C14h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H	4582 0C14h
C18h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L	4582 0C18h
C1Ch	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H	4582 0C1Ch
C20h	32	CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL	4582 0C20h

Table 14-3887. CBASS_INFRA1_GLB Registers, Base Address=45B0 1000h, Length=1024

Offset	Length	Register Name	CBASS_INFRA Physical Address
0h	32	CBASS_GLB_PID	45B0 1000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 1004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 1020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 1024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 1028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 102Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 1030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 1034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 1038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 1040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 1044h

Table 14-3888. CBASS_INFRA1_QOS Registers, Base Address=45D2 0000h, Length=4096

Offset	Length	Register Name	CBASS_INFRA Physical Address
100h	32	CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_PMST_MAP0	45D2 0100h
500h	32	CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_PMST_MAP0	45D2 0500h
900h	32	CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_PMST_MAP0	45D2 0900h
D00h	32	CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_PMST_MAP0	45D2 0D00h

14.1.4.2 CBASS_ERR_PID Register

CBASS_ERR_PID Register (Offset = 0h) [reset = 6600A901h]

Register Description: The Revision Register contains the major and minor revisions for the module.

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Table 14-3889. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0000h

Figure 14-1292. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
15h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-3891. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
15:11	RTL	R	15h	RTL revision. Will vary depending on release. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.3 CBASS_ERR_DESTINATION_ID Register

CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

Register Description: The Destination ID Register defines the destination ID value for error messages.

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Table 14-3892. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0004h

Figure 14-1293. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-3894. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

Register Description: The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-3895. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0024h

Figure 14-1294. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-3897. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.5 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

Register Description: The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-3898. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0028h

Figure 14-1295. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3900. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.4.6 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

Register Description: The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-3901. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 002Ch

Figure 14-1296. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-3903. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.7 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

Register Description: The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-3904. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0030h

Figure 14-1297. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-3906. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.8 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

Register Description: The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-3907. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0034h

Figure 14-1298. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-3909. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

Table 14-3909. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.9 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

Register Description: The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-3910. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0038h

Figure 14-1299. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3912. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.10 CBASS_ERR_ERR_INTR_RAW_STAT Register

CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

Register Description: Global Interrupt Raw Status Register

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Table 14-3913. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0050h

Figure 14-1300. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-3915. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.11 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

Register Description: Global Interrupt Enabled Status Register

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Table 14-3916. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0054h

Figure 14-1301. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-3918. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.12 CBASS_ERR_ERR_INTR_ENABLE_SET Register

CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Register Description: Interrupt Enable Set Register

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Table 14-3919. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0058h

Figure 14-1302. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-3921. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.13 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Register Description: Interrupt Enable Clear Register

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Table 14-3922. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 005Ch

Figure 14-1303. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-3924. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.14 CBASS_ERR_EOI Register

CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Register Description: EOI Register

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Table 14-3925. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ERR	0021 0060h

Figure 14-1304. CBASS_ERR_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3927. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register Reset Source: SCRP0_32b_clk4_rst_mod_g_rst_n

14.1.4.15 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_CONTROL Register (Offset = 800h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 0 firewall.

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Table 14-3928. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8800h

Figure 14-1305. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3930. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.16 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 804h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 0 firewall.

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Table 14-3931. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8804h

Figure 14-1306. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3933. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3933. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.17 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 808h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 0 firewall.

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Table 14-3934. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8808h

Figure 14-1307. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3936. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3936. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.18 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 80Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 0 firewall.

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Table 14-3937. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 880Ch

Figure 14-1308. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3939. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3939. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.19 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 0 firewall.

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Table 14-3940. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8810h

Figure 14-1309. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3942. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.20 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 0 firewall.

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Table 14-3943. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8814h

Figure 14-1310. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3945. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.21 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 0 firewall.

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Table 14-3946. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8818h

Figure 14-1311. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3948. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.22 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 0 firewall.

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Table 14-3949. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 881Ch

Figure 14-1312. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3951. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.23 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_CONTROL Register (Offset = 820h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 1 firewall.

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Table 14-3952. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8820h

Figure 14-1313. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3954. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.24 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 824h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 1 firewall.

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Table 14-3955. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8824h

Figure 14-1314. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3957. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3957. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.25 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 828h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 1 firewall.

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Table 14-3958. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8828h

Figure 14-1315. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3960. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3960. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.26 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 82Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 1 firewall.

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Table 14-3961. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 882Ch

Figure 14-1316. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3963. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3963. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.27 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 1 firewall.

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Table 14-3964. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8830h

Figure 14-1317. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3966. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.28 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 1 firewall.

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Table 14-3967. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8834h

Figure 14-1318. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3969. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.29 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 1 firewall.

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Table 14-3970. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8838h

Figure 14-1319. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3972. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.30 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 1 firewall.

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Table 14-3973. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 883Ch

Figure 14-1320. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3975. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.31 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_CONTROL Register (Offset = 840h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 2 firewall.

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Table 14-3976. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8840h

Figure 14-1321. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3978. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.32 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 844h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 2 firewall.

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Table 14-3979. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8844h

Figure 14-1322. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3981. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3981. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.33 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 848h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 2 firewall.

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Table 14-3982. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8848h

Figure 14-1323. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3984. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3984. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.34 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 84Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 2 firewall.

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Table 14-3985. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 884Ch

Figure 14-1324. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3987. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3987. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.35 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 2 firewall.

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Table 14-3988. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8850h

Figure 14-1325. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3990. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.36 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 2 firewall.

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Table 14-3991. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8854h

Figure 14-1326. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3993. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.37 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 2 firewall.

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Table 14-3994. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8858h

Figure 14-1327. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3996. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.38 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 2 firewall.

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Table 14-3997. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 885Ch

Figure 14-1328. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3999. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.39 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_CONTROL Register (Offset = 860h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 3 firewall.

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Table 14-4000. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8860h

Figure 14-1329. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4002. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.40 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 864h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 3 firewall.

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Table 14-4003. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8864h

Figure 14-1330. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4005. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4005. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.41 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 868h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 3 firewall.

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Table 14-4006. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8868h

Figure 14-1331. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4008. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4008. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.42 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 86Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 3 firewall.

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Table 14-4009. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 886Ch

Figure 14-1332. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4011. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4011. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.43 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 3 firewall.

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Table 14-4012. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8870h

Figure 14-1333. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4014. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.44 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 3 firewall.

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Table 14-4015. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8874h

Figure 14-1334. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4017. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.45 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 3 firewall.

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Table 14-4018. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8878h

Figure 14-1335. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4020. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.46 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 3 firewall.

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Table 14-4021. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 887Ch

Figure 14-1336. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4023. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.47 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_CONTROL Register (Offset = 880h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 4 firewall.

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Table 14-4024. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8880h

Figure 14-1337. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4026. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.48 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 884h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 4 firewall.

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Table 14-4027. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8884h

Figure 14-1338. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4029. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4029. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.49 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 888h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 4 firewall.

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Table 14-4030. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8888h

Figure 14-1339. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4032. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4032. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.50 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 88Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 4 firewall.

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Table 14-4033. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 888Ch

Figure 14-1340. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4035. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4035. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.51 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 890h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 4 firewall.

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Table 14-4036. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8890h

Figure 14-1341. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-4038. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.52 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 894h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 4 firewall.

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Table 14-4039. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8894h

Figure 14-1342. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4041. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.53 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 898h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 4 firewall.

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Table 14-4042. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8898h

Figure 14-1343. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4044. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.54 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 89Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 4 firewall.

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Table 14-4045. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 889Ch

Figure 14-1344. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4047. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.55 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_CONTROL Register (Offset = 8A0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 5 firewall.

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Table 14-4048. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88A0h

Figure 14-1345. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4050. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.56 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 8A4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 5 firewall.

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Table 14-4051. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88A4h

Figure 14-1346. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4053. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4053. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.57 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 8A8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 5 firewall.

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Table 14-4054. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88A8h

Figure 14-1347. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4056. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4056. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.58 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 8ACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 5 firewall.

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Table 14-4057. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88ACh

Figure 14-1348. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4059. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4059. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.59 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 8B0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 5 firewall.

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Table 14-4060. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88B0h

Figure 14-1349. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4062. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.60 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 8B4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 5 firewall.

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Table 14-4063. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88B4h

Figure 14-1350. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4065. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.61 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 8B8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 5 firewall.

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Table 14-4066. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88B8h

Figure 14-1351. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4068. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.62 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 8BCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 5 firewall.

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Table 14-4069. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88BCh

Figure 14-1352. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4071. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.63 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_CONTROL Register (Offset = 8C0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 6 firewall.

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Table 14-4072. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88C0h

Figure 14-1353. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4074. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.64 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 8C4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 6 firewall.

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Table 14-4075. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88C4h

Figure 14-1354. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4077. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4077. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.65 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 8C8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 6 firewall.

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Table 14-4078. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88C8h

Figure 14-1355. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4080. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4080. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.66 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 8CCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 6 firewall.

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Table 14-4081. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88CCh

Figure 14-1356. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4083. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4083. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.67 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 8D0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 6 firewall.

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Table 14-4084. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88D0h

Figure 14-1357. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4086. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.68 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 8D4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 6 firewall.

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Table 14-4087. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88D4h

Figure 14-1358. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4089. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.69 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 8D8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 6 firewall.

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Table 14-4090. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88D8h

Figure 14-1359. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4092. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.70 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 8DCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 6 firewall.

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Table 14-4093. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88DCh

Figure 14-1360. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4095. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.71 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_CONTROL Register (Offset = 8E0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 7 firewall.

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Table 14-4096. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88E0h

Figure 14-1361. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4098. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.72 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 8E4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 7 firewall.

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Table 14-4099. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88E4h

Figure 14-1362. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4101. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4101. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.73 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 8E8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 7 firewall.

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Table 14-4102. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88E8h

Figure 14-1363. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4104. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4104. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.74 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 8ECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 7 firewall.

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Table 14-4105. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88ECh

Figure 14-1364. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4107. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4107. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.75 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 8F0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 7 firewall.

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Table 14-4108. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88F0h

Figure 14-1365. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4110. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.76 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 8F4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 7 firewall.

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Table 14-4111. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88F4h

Figure 14-1366. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4113. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.77 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 8F8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 7 firewall.

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Table 14-4114. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88F8h

Figure 14-1367. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4116. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.78 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 8FCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP0_32b_clk4_l0 region 7 firewall.

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Table 14-4117. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 88FCh

Figure 14-1368. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4119. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP0_32B_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.79 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_CONTROL Register (Offset = C00h) [reset = 0h]

Register Description: The FW Region 0 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 0 firewall.

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Table 14-4120. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C00h

Figure 14-1369. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4122. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.80 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_0 Register (Offset = C04h) [reset = 0h]

Register Description: The FW Region 0 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 0 firewall.

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Table 14-4123. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C04h

Figure 14-1370. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4125. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4125. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.81 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_1 Register (Offset = C08h) [reset = 0h]

Register Description: The FW Region 0 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 0 firewall.

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Table 14-4126. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C08h

Figure 14-1371. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4128. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4128. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.82 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_2 Register (Offset = C0Ch) [reset = 0h]

Register Description: The FW Region 0 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 0 firewall.

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Table 14-4129. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C0Ch

Figure 14-1372. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4131. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4131. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.83 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 0h]

Register Description: The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 0 firewall.

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Table 14-4132. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C10h

Figure 14-1373. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4134. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.84 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 0h]

Register Description: The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 0 firewall.

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Table 14-4135. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C14h

Figure 14-1374. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4137. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.85 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = FFFh]

Register Description: The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 0 firewall.

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Table 14-4138. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C18h

Figure 14-1375. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4140. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.86 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 0h]

Register Description: The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 0 firewall.

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Table 14-4141. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C1Ch

Figure 14-1376. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4143. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.87 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_CONTROL Register (Offset = C20h) [reset = 0h]

Register Description: The FW Region 1 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 1 firewall.

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Table 14-4144. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C20h

Figure 14-1377. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4146. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.88 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_0 Register (Offset = C24h) [reset = 0h]

Register Description: The FW Region 1 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 1 firewall.

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Table 14-4147. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C24h

Figure 14-1378. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4149. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4149. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.89 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_1 Register (Offset = C28h) [reset = 0h]

Register Description: The FW Region 1 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 1 firewall.

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Table 14-4150. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C28h

Figure 14-1379. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4152. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4152. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.90 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_2 Register (Offset = C2Ch) [reset = 0h]

Register Description: The FW Region 1 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 1 firewall.

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Table 14-4153. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C2Ch

Figure 14-1380. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4155. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4155. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.91 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = C30h) [reset = 0h]

Register Description: The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 1 firewall.

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Table 14-4156. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C30h

Figure 14-1381. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4158. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.92 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = C34h) [reset = 0h]

Register Description: The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 1 firewall.

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Table 14-4159. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C34h

Figure 14-1382. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4161. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.93 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = C38h) [reset = FFFh]

Register Description: The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 1 firewall.

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Table 14-4162. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C38h

Figure 14-1383. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4164. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.94 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = C3Ch) [reset = 0h]

Register Description: The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 1 firewall.

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Table 14-4165. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C3Ch

Figure 14-1384. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4167. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.95 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_CONTROL Register (Offset = C40h) [reset = 0h]

Register Description: The FW Region 2 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 2 firewall.

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Table 14-4168. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C40h

Figure 14-1385. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4170. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.96 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_0 Register (Offset = C44h) [reset = 0h]

Register Description: The FW Region 2 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 2 firewall.

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Table 14-4171. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C44h

Figure 14-1386. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4173. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4173. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.97 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_1 Register (Offset = C48h) [reset = 0h]

Register Description: The FW Region 2 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 2 firewall.

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Table 14-4174. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C48h

Figure 14-1387. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4176. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4176. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.98 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_2 Register (Offset = C4Ch) [reset = 0h]

Register Description: The FW Region 2 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 2 firewall.

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Table 14-4177. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C4Ch

Figure 14-1388. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4179. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4179. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.99 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = C50h) [reset = 0h]

Register Description: The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 2 firewall.

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Table 14-4180. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C50h

Figure 14-1389. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4182. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.100 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = C54h) [reset = 0h]

Register Description: The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 2 firewall.

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Table 14-4183. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C54h

Figure 14-1390. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4185. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.101 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = C58h) [reset = FFFh]

Register Description: The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 2 firewall.

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Table 14-4186. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C58h

Figure 14-1391. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4188. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.102 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = C5Ch) [reset = 0h]

Register Description: The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 2 firewall.

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Table 14-4189. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C5Ch

Figure 14-1392. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4191. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.103 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_CONTROL Register (Offset = C60h) [reset = 0h]

Register Description: The FW Region 3 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 3 firewall.

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Table 14-4192. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C60h

Figure 14-1393. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4194. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.104 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_0 Register (Offset = C64h) [reset = 0h]

Register Description: The FW Region 3 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 3 firewall.

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Table 14-4195. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C64h

Figure 14-1394. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4197. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4197. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.105 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_1 Register (Offset = C68h) [reset = 0h]

Register Description: The FW Region 3 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 3 firewall.

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Table 14-4198. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C68h

Figure 14-1395. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4200. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4200. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.106 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_2 Register (Offset = C6Ch) [reset = 0h]

Register Description: The FW Region 3 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 3 firewall.

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Table 14-4201. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C6Ch

Figure 14-1396. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4203. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4203. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.107 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = C70h) [reset = 0h]

Register Description: The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 3 firewall.

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Table 14-4204. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C70h

Figure 14-1397. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4206. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.108 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = C74h) [reset = 0h]

Register Description: The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 3 firewall.

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Table 14-4207. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C74h

Figure 14-1398. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4209. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.109 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = C78h) [reset = FFFh]

Register Description: The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 3 firewall.

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Table 14-4210. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C78h

Figure 14-1399. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4212. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.110 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = C7Ch) [reset = 0h]

Register Description: The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 3 firewall.

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Table 14-4213. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C7Ch

Figure 14-1400. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4215. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.111 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_CONTROL Register (Offset = C80h) [reset = 0h]

Register Description: The FW Region 4 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 4 firewall.

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Table 14-4216. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C80h

Figure 14-1401. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4218. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.112 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_0 Register (Offset = C84h) [reset = 0h]

Register Description: The FW Region 4 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 4 firewall.

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Table 14-4219. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C84h

Figure 14-1402. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4221. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4221. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.113 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_1 Register (Offset = C88h) [reset = 0h]

Register Description: The FW Region 4 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 4 firewall.

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Table 14-4222. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C88h

Figure 14-1403. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4224. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4224. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.114 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_2 Register (Offset = C8Ch) [reset = 0h]

Register Description: The FW Region 4 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 4 firewall.

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Table 14-4225. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C8Ch

Figure 14-1404. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4227. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4227. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.115 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = C90h) [reset = 0h]

Register Description: The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 4 firewall.

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Table 14-4228. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C90h

Figure 14-1405. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4230. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.116 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = C94h) [reset = 0h]

Register Description: The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 4 firewall.

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Table 14-4231. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C94h

Figure 14-1406. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4233. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.117 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = C98h) [reset = FFFh]

Register Description: The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 4 firewall.

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Table 14-4234. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C98h

Figure 14-1407. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4236. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.118 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = C9Ch) [reset = 0h]

Register Description: The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 4 firewall.

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Table 14-4237. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8C9Ch

Figure 14-1408. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4239. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.119 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_CONTROL Register (Offset = CA0h) [reset = 0h]

Register Description: The FW Region 5 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 5 firewall.

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Table 14-4240. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CA0h

Figure 14-1409. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4242. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.120 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_0 Register (Offset = CA4h) [reset = 0h]

Register Description: The FW Region 5 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 5 firewall.

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Table 14-4243. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CA4h

Figure 14-1410. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4245. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4245. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.121 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_1 Register (Offset = CA8h) [reset = 0h]

Register Description: The FW Region 5 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 5 firewall.

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Table 14-4246. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CA8h

Figure 14-1411. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-4248. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4248. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.122 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_2 Register (Offset = CACh) [reset = 0h]

Register Description: The FW Region 5 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 5 firewall.

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Table 14-4249. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CACh

Figure 14-1412. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4251. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4251. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.123 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = CB0h) [reset = 0h]

Register Description: The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 5 firewall.

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Table 14-4252. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CB0h

Figure 14-1413. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4254. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.124 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = CB4h) [reset = 0h]

Register Description: The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 5 firewall.

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Table 14-4255. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CB4h

Figure 14-1414. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4257. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.125 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = CB8h) [reset = FFFh]

Register Description: The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 5 firewall.

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Table 14-4258. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CB8h

Figure 14-1415. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4260. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.126 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = CBCh) [reset = 0h]

Register Description: The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 5 firewall.

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Table 14-4261. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CBCh

Figure 14-1416. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4263. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.127 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_CONTROL Register (Offset = CC0h) [reset = 0h]

Register Description: The FW Region 6 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 6 firewall.

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Table 14-4264. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CC0h

Figure 14-1417. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4266. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.128 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_0 Register (Offset = CC4h) [reset = 0h]

Register Description: The FW Region 6 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 6 firewall.

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Table 14-4267. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CC4h

Figure 14-1418. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4269. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4269. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.129 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_1 Register (Offset = CC8h) [reset = 0h]

Register Description: The FW Region 6 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 6 firewall.

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Table 14-4270. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CC8h

Figure 14-1419. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4272. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4272. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.130 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_2 Register (Offset = CCCh) [reset = 0h]

Register Description: The FW Region 6 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 6 firewall.

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Table 14-4273. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CCCh

Figure 14-1420. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4275. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4275. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.131 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = CD0h) [reset = 0h]

Register Description: The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 6 firewall.

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Table 14-4276. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CD0h

Figure 14-1421. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4278. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.132 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = CD4h) [reset = 0h]

Register Description: The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 6 firewall.

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Table 14-4279. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CD4h

Figure 14-1422. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4281. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.133 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = CD8h) [reset = FFFh]

Register Description: The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 6 firewall.

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Table 14-4282. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CD8h

Figure 14-1423. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4284. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.134 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = CDCh) [reset = 0h]

Register Description: The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 6 firewall.

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Table 14-4285. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CDCh

Figure 14-1424. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4287. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.135 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_CONTROL Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_CONTROL Register (Offset = CE0h) [reset = 0h]

Register Description: The FW Region 7 Control Register defines the control fields for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 7 firewall.

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Table 14-4288. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CE0h

Figure 14-1425. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4290. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.136 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_0 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_0 Register (Offset = CE4h) [reset = 0h]

Register Description: The FW Region 7 Permission 0 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 7 firewall.

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Table 14-4291. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CE4h

Figure 14-1426. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4293. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4293. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.137 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_1 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_1 Register (Offset = CE8h) [reset = 0h]

Register Description: The FW Region 7 Permission 1 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 7 firewall.

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Table 14-4294. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CE8h

Figure 14-1427. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4296. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4296. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.138 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_2 Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_2 Register (Offset = CECh) [reset = 0h]

Register Description: The FW Region 7 Permission 2 Register defines the permissions for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 7 firewall.

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Table 14-4297. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CECh

Figure 14-1428. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4299. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4299. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.139 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = CF0h) [reset = 0h]

Register Description: The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 7 firewall.

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Table 14-4300. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CF0h

Figure 14-1429. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4302. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.140 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = CF4h) [reset = 0h]

Register Description: The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 7 firewall.

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Table 14-4303. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CF4h

Figure 14-1430. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4305. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.141 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_L Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = CF8h) [reset = FFFh]

Register Description: The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 7 firewall.

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Table 14-4306. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CF8h

Figure 14-1431. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4308. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.142 CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_H Register

CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = CFCh) [reset = 0h]

Register Description: The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave br_SCRP_32b_motor_to_SCRP_32b_miscIO_l0 region 7 firewall.

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Table 14-4309. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_FW	4500 8CFCh

Figure 14-1432. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4311. CBASS_FW_BR_SCRP_32B_MOTOR_TO_SCRP_32B_MISCIO_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.143 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Register (Offset = 0h) [reset = D400h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu0_pmst region 0 ISC.

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Table 14-4312. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0000h

Figure 14-1433. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4314. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4314. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.144 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu0_pmst region 0 ISC.

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Table 14-4315. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0010h

Figure 14-1434. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4317. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.145 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu0_pmst region 0 ISC.

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Table 14-4318. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0014h

Figure 14-1435. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4320. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.146 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu0_pmst region 0 ISC.

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Table 14-4321. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0018h

Figure 14-1436. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4323. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.147 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu0_pmst region 0 ISC.

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Table 14-4324. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 001Ch

Figure 14-1437. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4326. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.148 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 20h) [reset = D44Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu0_pmst region 1 ISC.

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Table 14-4327. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0020h

Figure 14-1438. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4329. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4329. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.149 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Register (Offset = 400h) [reset = D500h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu1_pmst region 0 ISC.

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Table 14-4330. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0400h

Figure 14-1439. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D5h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4332. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4332. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D5h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.150 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu1_pmst region 0 ISC.

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Table 14-4333. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0410h

Figure 14-1440. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4335. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.151 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu1_pmst region 0 ISC.

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Table 14-4336. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0414h

Figure 14-1441. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4338. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.152 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_0.cpu1_pmst region 0 ISC.

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Table 14-4339. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0418h

Figure 14-1442. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4341. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.153 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_0.cpu1_pmst region 0 ISC.

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Table 14-4342. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 041Ch

Figure 14-1443. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4344. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.154 CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 420h) [reset = D54Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_0.cpu1_pmst region 1 ISC.

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Table 14-4345. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0420h

Figure 14-1444. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D5h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4347. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4347. CBASS_ISC_IPULSAR_LITE_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D5h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.155 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Register (Offset = 800h) [reset = D600h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu0_pmst region 0 ISC.

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Table 14-4348. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0800h

Figure 14-1445. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D6h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4350. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4350. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D6h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.156 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu0_pmst region 0 ISC.

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Table 14-4351. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0810h

Figure 14-1446. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4353. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.157 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu0_pmst region 0 ISC.

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Table 14-4354. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0814h

Figure 14-1447. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4356. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.158 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu0_pmst region 0 ISC.

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Table 14-4357. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0818h

Figure 14-1448. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4359. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.159 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu0_pmst region 0 ISC.

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Table 14-4360. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 081Ch

Figure 14-1449. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4362. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.160 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 820h) [reset = D64Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu0_pmst region 1 ISC.

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Table 14-4363. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0820h

Figure 14-1450. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D6h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4365. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4365. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D6h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.161 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Register (Offset = C00h) [reset = D700h]

Register Description: The ISC Region 0 Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu1_pmst region 0 ISC.

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Table 14-4366. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0C00h

Figure 14-1451. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D7h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-4368. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4368. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	PRIV_ID	R/W	D7h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.162 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 0h]

Register Description: The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu1_pmst region 0 ISC.

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Table 14-4369. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0C10h

Figure 14-1452. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-4371. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.163 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 0h]

Register Description: The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu1_pmst region 0 ISC.

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Table 14-4372. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0C14h

Figure 14-1453. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4374. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.164 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = FFFh]

Register Description: The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the master Ipulsar_lite_main_1.cpu1_pmst region 0 ISC.

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Table 14-4375. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0C18h

Figure 14-1454. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4377. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.165 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 0h]

Register Description: The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the master Ipulsar_lite_main_1.cpu1_pmst region 0 ISC.

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Table 14-4378. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0C1Ch

Figure 14-1455. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4380. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.166 CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Register

CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Register (Offset = C20h) [reset = D74Ah]

Register Description: The ISC Default Region Control Register defines the control fields for the master Ipulsar_lite_main_1.cpu1_pmst region 1 ISC.

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Table 14-4381. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_ISC	4582 0C20h

Figure 14-1456. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D7h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-4383. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4383. CBASS_ISC_IPULSAR_LITE_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D7h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.167 CBASS_GLB_PID Register

CBASS_GLB_PID Register (Offset = 0h) [reset = 6600A901h]

Register Description: The Revision Register contains the major and minor revisions for the module.

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Table 14-4384. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1000h

Figure 14-1457. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
15h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-4386. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	15h	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.168 CBASS_GLB_DESTINATION_ID Register

CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

Register Description: The Destination ID Register defines the destination ID value for error messages.

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Table 14-4387. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1004h

Figure 14-1458. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-4389. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.169 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

Register Description: The Exception Logging Control Register controls the exception logging.

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Table 14-4390. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1020h

Figure 14-1459. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-4392. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.170 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

Register Description: The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-4393. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1024h

Figure 14-1460. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-4395. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.171 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

Register Description: The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-4396. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1028h

Figure 14-1461. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4398. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.4.172 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

Register Description: The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-4399. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 102Ch

Figure 14-1462. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-4401. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.173 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

Register Description: The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-4402. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1030h

Figure 14-1463. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-4404. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.174 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

Register Description: The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-4405. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1034h

Figure 14-1464. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-4407. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4407. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.175 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

Register Description: The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-4408. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1038h

Figure 14-1465. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-4410. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.176 CBASS_GLB_EXCEPTION_PEND_SET Register

CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

Register Description: The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-4411. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1040h

Figure 14-1466. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-4413. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.177 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

Register Description: The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-4414. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_GLB	45B0 1044h

Figure 14-1467. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-4416. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4.178 CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_PMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_PMST_MAP0 Register (Offset = 100h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator Ipulsar_lite_main_0.cpu0_pmst per channel.

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Table 14-4417. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_QOS	45D2 0100h

Figure 14-1468. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_PMST_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4419. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-4419. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU0_PMST_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.4.179 CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_PMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_PMST_MAP0 Register (Offset = 500h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator Ipulsar_lite_main_0.cpu1_pmst per channel.

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Table 14-4420. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_QOS	45D2 0500h

Figure 14-1469. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-4422. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-4422. CBASS_QOS_IPULSAR_LITE_MAIN_0_CPU1_PMST_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.4.180 CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_PMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_PMST_MAP0 Register (Offset = 900h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator Ipulsar_lite_main_1.cpu0_pmst per channel.

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Table 14-4423. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_QOS	45D2 0900h

Figure 14-1470. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-4425. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-4425. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU0_PMST_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.4.181 CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_PMST_MAP0 Register

CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_PMST_MAP0 Register (Offset = D00h) [reset = 7000h]

Register Description: The Map Register defines the fields for the initiator Ipulsar_lite_main_1.cpu1_pmst per channel.

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Table 14-4426. Instance Table

Instance Name	Physical Address
CBASS_INFRA1_QOS	45D2 0D00h

Figure 14-1471. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	RESERVED		
R/W				NONE	R/W		
0h				0h	0h		

Table 14-4428. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller.#brbr#ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-4428. CBASS_QOS_IPULSAR_LITE_MAIN_1_CPU1_PMST_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.1.5 cbass_dbg

cbass_dbg

14.1.5.1 cbass_dbg Summaries

cbass_dbg Summaries

Table 14-4429. CBASS_ERR Registers, Base Address=0020 0000h, Length=1024

Offset	Length	Register Name	CBASS_DBG0 Physical Address
0h	32	CBASS_ERR_PID	0020 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0020 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0020 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0020 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0020 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0020 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0020 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0020 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0020 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0020 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0020 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0020 005Ch
60h	32	CBASS_ERR_EOI	0020 0060h

14.1.5.2 cbass_dbg Registers

cbass_dbg Registers

14.1.5.2.1 CBASS_ERR_PID Register

1 CBASS_ERR_PID Register (Offset = 0h) [reset = 6600A101h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-4430. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0000h**

Figure 14-1472. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
14h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-4432. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
15:11	RTL	R	14h	RTL revision. Will vary depending on release. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.2 CBASS_ERR_DESTINATION_ID Register

1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-4433. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0004h**

Figure 14-1473. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-4435. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-4436. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0024h**

Figure 14-1474. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-4438. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-4439. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0028h**

Figure 14-1475. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4441. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.5.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-4442. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 002Ch**

Figure 14-1476. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-4444. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-4445. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0030h**

Figure 14-1477. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-4447. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-4448. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0034h**

Figure 14-1478. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-4450. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

Table 14-4450. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-4451. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0038h**

Figure 14-1479. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-4453. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

Global Interrupt Raw Status Register

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Table 14-4454. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0050h**

Figure 14-1480. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-4456. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

Global Interrupt Enabled Status Register

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Table 14-4457. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0054h**

Figure 14-1481. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-4459. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Interrupt Enable Set Register

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Table 14-4460. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0058h**

Figure 14-1482. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-4462. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Interrupt Enable Clear Register

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Table 14-4463. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 005Ch**

Figure 14-1483. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-4465. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.1.5.2.13 CBASS_ERR_EOI Register

1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

EOI Register

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Table 14-4466. Instance Table

Instance Name	Physical Address
CBASS_DBG0	**0020 0060h**

Figure 14-1484. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-4468. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register Reset Source: SCRP_maindbg_MCLK4_rst_mod_g_rst_n

14.2 Device Configuration Registers

14.2.1 CTRL_MMR Registers

14.2.1.1 General Purpose Control Registers

14.2.1.1.1 main_ctrl_mmr

main_ctrl_mmr

14.2.1.1.1.1 main_ctrl_mmr Summaries

main_ctrl_mmr Summaries

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072

Offset	Length	Register Name	CTRL_MMR0 Physical Address
0h	32	MAIN_CTRL_MMR_CFG0_PID	4300 0000h
8h	32	MAIN_CTRL_MMR_CFG0_MMR_CFG1	4300 0008h
14h	32	MAIN_CTRL_MMR_CFG0_JTAGID	4300 0014h
18h	32	MAIN_CTRL_MMR_CFG0_JTAG_USER_ID	4300 0018h
30h	32	MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT	4300 0030h
34h	32	MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG	4300 0034h
44h	32	MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS	4300 0044h
60h	32	MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0	4300 0060h
68h	32	MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2	4300 0068h
78h	32	MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6	4300 0078h
200h	32	MAIN_CTRL_MMR_CFG0_MAC_ID0	4300 0200h
204h	32	MAIN_CTRL_MMR_CFG0_MAC_ID1	4300 0204h
210h	32	MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0	4300 0210h
214h	32	MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1	4300 0214h
220h	32	MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0	4300 0220h
230h	32	MAIN_CTRL_MMR_CFG0_GP_SW0	4300 0230h
234h	32	MAIN_CTRL_MMR_CFG0_GP_SW1	4300 0234h
238h	32	MAIN_CTRL_MMR_CFG0_GP_SW2	4300 0238h
23Ch	32	MAIN_CTRL_MMR_CFG0_GP_SW3	4300 023Ch
270h	32	MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT	4300 0270h
1008h	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK0	4300 1008h
100Ch	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK1	4300 100Ch
1010h	32	MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS	4300 1010h
1014h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	4300 1014h
1018h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE	4300 1018h
101Ch	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	4300 101Ch
1020h	32	MAIN_CTRL_MMR_CFG0_EOI	4300 1020h
1024h	32	MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS	4300 1024h
1028h	32	MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	4300 1028h
102Ch	32	MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	4300 102Ch
1030h	32	MAIN_CTRL_MMR_CFG0_FAULT_CLEAR	4300 1030h
1100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	4300 1100h
1104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY	4300 1104h
1108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY	4300 1108h
110Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY	4300 110Ch

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
1110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY	4300 1110h
1114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY	4300 1114h
1118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY	4300 1118h
2000h	32	MAIN_CTRL_MMR_CFG0_PID_PROXY	4300 2000h
2008h	32	MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY	4300 2008h
2014h	32	MAIN_CTRL_MMR_CFG0_JTAGID_PROXY	4300 2014h
2018h	32	MAIN_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY	4300 2018h
2030h	32	MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY	4300 2030h
2034h	32	MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY	4300 2034h
2044h	32	MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY	4300 2044h
2060h	32	MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY	4300 2060h
2068h	32	MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY	4300 2068h
2078h	32	MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY	4300 2078h
2200h	32	MAIN_CTRL_MMR_CFG0_MAC_ID0_PROXY	4300 2200h
2204h	32	MAIN_CTRL_MMR_CFG0_MAC_ID1_PROXY	4300 2204h
2210h	32	MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0_PROXY	4300 2210h
2214h	32	MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1_PROXY	4300 2214h
2220h	32	MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY	4300 2220h
2230h	32	MAIN_CTRL_MMR_CFG0_GP_SW0_PROXY	4300 2230h
2234h	32	MAIN_CTRL_MMR_CFG0_GP_SW1_PROXY	4300 2234h
2238h	32	MAIN_CTRL_MMR_CFG0_GP_SW2_PROXY	4300 2238h
223Ch	32	MAIN_CTRL_MMR_CFG0_GP_SW3_PROXY	4300 223Ch
2270h	32	MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY	4300 2270h
3008h	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	4300 3008h
300Ch	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	4300 300Ch
3010h	32	MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	4300 3010h
3014h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	4300 3014h
3018h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	4300 3018h
301Ch	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	4300 301Ch
3020h	32	MAIN_CTRL_MMR_CFG0_EOI_PROXY	4300 3020h
3024h	32	MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	4300 3024h
3028h	32	MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	4300 3028h
302Ch	32	MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	4300 302Ch
3030h	32	MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	4300 3030h
3100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0	4300 3100h
3104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1	4300 3104h
3108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2	4300 3108h
310Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3	4300 310Ch
3110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4	4300 3110h

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
3114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5	4300 3114h
3118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6	4300 3118h
4008h	32	MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL	4300 4008h
4044h	32	MAIN_CTRL_MMR_CFG0_ENET1_CTRL	4300 4044h
4048h	32	MAIN_CTRL_MMR_CFG0_ENET2_CTRL	4300 4048h
4070h	32	MAIN_CTRL_MMR_CFG0_PCIE0_CTRL	4300 4070h
4080h	32	MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL	4300 4080h
40C0h	32	MAIN_CTRL_MMR_CFG0_ADC0_TRIM	4300 40C0h
40E0h	32	MAIN_CTRL_MMR_CFG0_SERDES0_CTRL	4300 40E0h
4100h	32	MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0	4300 4100h
4104h	32	MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1	4300 4104h
4110h	32	MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0	4300 4110h
4114h	32	MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1	4300 4114h
4130h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN	4300 4130h
4134h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET	4300 4134h
4138h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR	4300 4138h
4140h	32	MAIN_CTRL_MMR_CFG0_EPWM0_CTRL	4300 4140h
4144h	32	MAIN_CTRL_MMR_CFG0_EPWM1_CTRL	4300 4144h
4148h	32	MAIN_CTRL_MMR_CFG0_EPWM2_CTRL	4300 4148h
414Ch	32	MAIN_CTRL_MMR_CFG0_EPWM3_CTRL	4300 414Ch
4150h	32	MAIN_CTRL_MMR_CFG0_EPWM4_CTRL	4300 4150h
4154h	32	MAIN_CTRL_MMR_CFG0_EPWM5_CTRL	4300 4154h
4158h	32	MAIN_CTRL_MMR_CFG0_EPWM6_CTRL	4300 4158h
415Ch	32	MAIN_CTRL_MMR_CFG0_EPWM7_CTRL	4300 415Ch
4160h	32	MAIN_CTRL_MMR_CFG0_EPWM8_CTRL	4300 4160h
4170h	32	MAIN_CTRL_MMR_CFG0_SOCA_SEL	4300 4170h
4174h	32	MAIN_CTRL_MMR_CFG0_SOCB_SEL	4300 4174h
4180h	32	MAIN_CTRL_MMR_CFG0_EQEP0_CTRL	4300 4180h
4184h	32	MAIN_CTRL_MMR_CFG0_EQEP1_CTRL	4300 4184h
4188h	32	MAIN_CTRL_MMR_CFG0_EQEP2_CTRL	4300 4188h
41A0h	32	MAIN_CTRL_MMR_CFG0_EQEP_STAT	4300 41A0h
41B4h	32	MAIN_CTRL_MMR_CFG0_SDIO1_CTRL	4300 41B4h
4204h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL	4300 4204h
420Ch	32	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL	4300 420Ch
4214h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL	4300 4214h
421Ch	32	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL	4300 421Ch
4224h	32	MAIN_CTRL_MMR_CFG0_TIMER9_CTRL	4300 4224h
422Ch	32	MAIN_CTRL_MMR_CFG0_TIMER11_CTRL	4300 422Ch
42E0h	32	MAIN_CTRL_MMR_CFG0_I2C0_CTRL	4300 42E0h
4700h	32	MAIN_CTRL_MMR_CFG0_FSS_CTRL	4300 4700h
4710h	32	MAIN_CTRL_MMR_CFG0_ADC0_CTRL	4300 4710h
4750h	32	MAIN_CTRL_MMR_CFG0_DCC_STAT	4300 4750h
5008h	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK0	4300 5008h
500Ch	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK1	4300 500Ch

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
5100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	4300 5100h
5104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	4300 5104h
5108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY	4300 5108h
510Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	4300 510Ch
5110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	4300 5110h
5114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY	4300 5114h
5118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY	4300 5118h
511Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY	4300 511Ch
5120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY	4300 5120h
5124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY	4300 5124h
5128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY	4300 5128h
512Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY	4300 512Ch
5130h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY	4300 5130h
5134h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY	4300 5134h
5138h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY	4300 5138h
6008h	32	MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY	4300 6008h
6044h	32	MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY	4300 6044h
6048h	32	MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY	4300 6048h
6070h	32	MAIN_CTRL_MMR_CFG0_PCIE0_CTRL_PROXY	4300 6070h
6080h	32	MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL_PROXY	4300 6080h
60C0h	32	MAIN_CTRL_MMR_CFG0_ADC0_TRIM_PROXY	4300 60C0h
60E0h	32	MAIN_CTRL_MMR_CFG0_SERDES0_CTRL_PROXY	4300 60E0h
6100h	32	MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0_PROXY	4300 6100h
6104h	32	MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1_PROXY	4300 6104h
6110h	32	MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0_PROXY	4300 6110h
6114h	32	MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1_PROXY	4300 6114h
6130h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY	4300 6130h
6134h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET_PROXY	4300 6134h
6138h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR_PROXY	4300 6138h
6140h	32	MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY	4300 6140h
6144h	32	MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY	4300 6144h
6148h	32	MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY	4300 6148h

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
614Ch	32	MAIN_CTRL_MMR_CFG0_EPWM3_CTRL_PROXY	4300 614Ch
6150h	32	MAIN_CTRL_MMR_CFG0_EPWM4_CTRL_PROXY	4300 6150h
6154h	32	MAIN_CTRL_MMR_CFG0_EPWM5_CTRL_PROXY	4300 6154h
6158h	32	MAIN_CTRL_MMR_CFG0_EPWM6_CTRL_PROXY	4300 6158h
615Ch	32	MAIN_CTRL_MMR_CFG0_EPWM7_CTRL_PROXY	4300 615Ch
6160h	32	MAIN_CTRL_MMR_CFG0_EPWM8_CTRL_PROXY	4300 6160h
6170h	32	MAIN_CTRL_MMR_CFG0_SOCA_SEL_PROXY	4300 6170h
6174h	32	MAIN_CTRL_MMR_CFG0_SOCB_SEL_PROXY	4300 6174h
6180h	32	MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY	4300 6180h
6184h	32	MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY	4300 6184h
6188h	32	MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY	4300 6188h
61A0h	32	MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY	4300 61A0h
61B4h	32	MAIN_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY	4300 61B4h
6204h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY	4300 6204h
620Ch	32	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY	4300 620Ch
6214h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY	4300 6214h
621Ch	32	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY	4300 621Ch
6224h	32	MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY	4300 6224h
622Ch	32	MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY	4300 622Ch
62E0h	32	MAIN_CTRL_MMR_CFG0_I2C0_CTRL_PROXY	4300 62E0h
6700h	32	MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY	4300 6700h
6710h	32	MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY	4300 6710h
6750h	32	MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY	4300 6750h
7008h	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	4300 7008h
700Ch	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	4300 700Ch
7100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0	4300 7100h
7104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1	4300 7104h
7108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2	4300 7108h
710Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3	4300 710Ch
7110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4	4300 7110h
7114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5	4300 7114h
7118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6	4300 7118h
711Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7	4300 711Ch
7120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8	4300 7120h
7124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9	4300 7124h
7128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10	4300 7128h
712Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11	4300 712Ch
7130h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12	4300 7130h
7134h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13	4300 7134h
7138h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14	4300 7138h
8000h	32	MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL	4300 8000h
8010h	32	MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL	4300 8010h
8030h	32	MAIN_CTRL_MMR_CFG0_GTC_CLKSEL	4300 8030h
803Ch	32	MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL	4300 803Ch

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
8040h	32	MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL	4300 8040h
8044h	32	MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL	4300 8044h
8060h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL	4300 8060h
8064h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL	4300 8064h
8068h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL	4300 8068h
8080h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL	4300 8080h
8090h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL	4300 8090h
8098h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL	4300 8098h
8120h	32	MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL	4300 8120h
8140h	32	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL	4300 8140h
8150h	32	MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL	4300 8150h
8160h	32	MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL	4300 8160h
8168h	32	MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL	4300 8168h
8180h	32	MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL	4300 8180h
8190h	32	MAIN_CTRL_MMR_CFG0_USB0_CLKSEL	4300 8190h
81B0h	32	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL	4300 81B0h
81B4h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL	4300 81B4h
81B8h	32	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL	4300 81B8h
81BCh	32	MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL	4300 81BCh
81C0h	32	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL	4300 81C0h
81C4h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL	4300 81C4h
81C8h	32	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL	4300 81C8h
81CCh	32	MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL	4300 81CCh
81D0h	32	MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL	4300 81D0h
81D4h	32	MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL	4300 81D4h
81D8h	32	MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL	4300 81D8h
81DCh	32	MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL	4300 81DCh
8200h	32	MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL	4300 8200h
8204h	32	MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL	4300 8204h
8208h	32	MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL	4300 8208h
820Ch	32	MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL	4300 820Ch
8210h	32	MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL	4300 8210h
8240h	32	MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL	4300 8240h
8244h	32	MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL	4300 8244h
8248h	32	MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL	4300 8248h
824Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL	4300 824Ch
8250h	32	MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL	4300 8250h
8254h	32	MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL	4300 8254h
8258h	32	MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL	4300 8258h
8280h	32	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL	4300 8280h
8284h	32	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL	4300 8284h
8288h	32	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL	4300 8288h
828Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL	4300 828Ch
8290h	32	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL	4300 8290h

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
8294h	32	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL	4300 8294h
8298h	32	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL	4300 8298h
8380h	32	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL	4300 8380h
8384h	32	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL	4300 8384h
83A0h	32	MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL	4300 83A0h
83A4h	32	MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL	4300 83A4h
83A8h	32	MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL	4300 83A8h
83ACh	32	MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL	4300 83ACh
8400h	32	MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL	4300 8400h
8480h	32	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL	4300 8480h
8484h	32	MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL	4300 8484h
8500h	32	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL	4300 8500h
8510h	32	MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL	4300 8510h
9008h	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK0	4300 9008h
900Ch	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK1	4300 900Ch
9100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY	4300 9100h
9104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY	4300 9104h
9108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY	4300 9108h
910Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY	4300 910Ch
9110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY	4300 9110h
9114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY	4300 9114h
9118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY	4300 9118h
911Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY	4300 911Ch
9120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY	4300 9120h
9124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY	4300 9124h
9128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY	4300 9128h
A000h	32	MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY	4300 A000h
A010h	32	MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY	4300 A010h
A030h	32	MAIN_CTRL_MMR_CFG0_GTC_CLKSEL_PROXY	4300 A030h
A03Ch	32	MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY	4300 A03Ch
A040h	32	MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL_PROXY	4300 A040h
A044h	32	MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL_PROXY	4300 A044h
A060h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY	4300 A060h
A064h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY	4300 A064h
A068h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY	4300 A068h
A080h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY	4300 A080h

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
A090h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY	4300 A090h
A098h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY	4300 A098h
A120h	32	MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL_PROXY	4300 A120h
A140h	32	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY	4300 A140h
A150h	32	MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL_PROXY	4300 A150h
A160h	32	MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY	4300 A160h
A168h	32	MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY	4300 A168h
A180h	32	MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY	4300 A180h
A190h	32	MAIN_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY	4300 A190h
A1B0h	32	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY	4300 A1B0h
A1B4h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY	4300 A1B4h
A1B8h	32	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY	4300 A1B8h
A1BCh	32	MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY	4300 A1BCh
A1C0h	32	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY	4300 A1C0h
A1C4h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY	4300 A1C4h
A1C8h	32	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY	4300 A1C8h
A1CCh	32	MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY	4300 A1CCh
A1D0h	32	MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY	4300 A1D0h
A1D4h	32	MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY	4300 A1D4h
A1D8h	32	MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY	4300 A1D8h
A1DCh	32	MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY	4300 A1DCh
A200h	32	MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY	4300 A200h
A204h	32	MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY	4300 A204h
A208h	32	MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY	4300 A208h
A20Ch	32	MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY	4300 A20Ch
A210h	32	MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY	4300 A210h
A240h	32	MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY	4300 A240h
A244h	32	MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY	4300 A244h
A248h	32	MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY	4300 A248h
A24Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY	4300 A24Ch
A250h	32	MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY	4300 A250h
A254h	32	MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY	4300 A254h
A258h	32	MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY	4300 A258h
A280h	32	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY	4300 A280h
A284h	32	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY	4300 A284h
A288h	32	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY	4300 A288h
A28Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY	4300 A28Ch
A290h	32	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY	4300 A290h
A294h	32	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY	4300 A294h
A298h	32	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY	4300 A298h
A380h	32	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY	4300 A380h
A384h	32	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY	4300 A384h
A3A0h	32	MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL_PROXY	4300 A3A0h

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
A3A4h	32	MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL_PROXY	4300 A3A4h
A3A8h	32	MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL_PROXY	4300 A3A8h
A3ACh	32	MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL_PROXY	4300 A3ACh
A400h	32	MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL_PROXY	4300 A400h
A480h	32	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY	4300 A480h
A484h	32	MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY	4300 A484h
A500h	32	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY	4300 A500h
A510h	32	MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY	4300 A510h
B008h	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY	4300 B008h
B00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY	4300 B00Ch
B100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0	4300 B100h
B104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1	4300 B104h
B108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2	4300 B108h
B10Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3	4300 B10Ch
B110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4	4300 B110h
B114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5	4300 B114h
B118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6	4300 B118h
B11Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7	4300 B11Ch
B120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8	4300 B120h
B124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9	4300 B124h
B128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10	4300 B128h
C304h	32	MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE	4300 C304h
C310h	32	MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE	4300 C310h
C314h	32	MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE	4300 C314h
C318h	32	MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE	4300 C318h
C31Ch	32	MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE	4300 C31Ch
C320h	32	MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT	4300 C320h
C324h	32	MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC	4300 C324h
C330h	32	MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC	4300 C330h
C334h	32	MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC	4300 C334h
C338h	32	MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC	4300 C338h
C33Ch	32	MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC	4300 C33Ch
C400h	32	MAIN_CTRL_MMR_CFG0_PBIST_EN	4300 C400h
D008h	32	MAIN_CTRL_MMR_CFG0_LOCK3_KICK0	4300 D008h
D00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK3_KICK1	4300 D00Ch
D100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY	4300 D100h
D104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY	4300 D104h
D108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY	4300 D108h
D10Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY	4300 D10Ch
D110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY	4300 D110h

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
D114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY	4300 D114h
D118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY	4300 D118h
D11Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY	4300 D11Ch
D120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY	4300 D120h
E304h	32	MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE_PROXY	4300 E304h
E310h	32	MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE_PROXY	4300 E310h
E314h	32	MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE_PROXY	4300 E314h
E318h	32	MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE_PROXY	4300 E318h
E31Ch	32	MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE_PROXY	4300 E31Ch
E320h	32	MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY	4300 E320h
E324h	32	MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC_PROXY	4300 E324h
E330h	32	MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC_PROXY	4300 E330h
E334h	32	MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC_PROXY	4300 E334h
E338h	32	MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC_PROXY	4300 E338h
E33Ch	32	MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC_PROXY	4300 E33Ch
E400h	32	MAIN_CTRL_MMR_CFG0_PBIST_EN_PROXY	4300 E400h
F008h	32	MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY	4300 F008h
F00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY	4300 F00Ch
F100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0	4300 F100h
F104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1	4300 F104h
F108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2	4300 F108h
F10Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3	4300 F10Ch
F110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4	4300 F110h
F114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5	4300 F114h
F118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6	4300 F118h
F11Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7	4300 F11Ch
F120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8	4300 F120h
11008h	32	MAIN_CTRL_MMR_CFG0_LOCK4_KICK0	4301 1008h
1100Ch	32	MAIN_CTRL_MMR_CFG0_LOCK4_KICK1	4301 100Ch
11100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY	4301 1100h
11104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY	4301 1104h
11108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY	4301 1108h
1110Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY	4301 110Ch
11110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY	4301 1110h
11114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY	4301 1114h
11118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY	4301 1118h

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
1111Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY	4301 111Ch
11120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY	4301 1120h
11124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY	4301 1124h
11128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY	4301 1128h
1112Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY	4301 112Ch
11130h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY	4301 1130h
13008h	32	MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY	4301 3008h
1300Ch	32	MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY	4301 300Ch
13100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0	4301 3100h
13104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1	4301 3104h
13108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2	4301 3108h
1310Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3	4301 310Ch
13110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4	4301 3110h
13114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5	4301 3114h
13118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6	4301 3118h
1311Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7	4301 311Ch
13120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8	4301 3120h
13124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9	4301 3124h
13128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10	4301 3128h
1312Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11	4301 312Ch
13130h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12	4301 3130h
14000h	32	MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ	4301 4000h
14004h	32	MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK	4301 4004h
14080h	32	MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ	4301 4080h
140C0h	32	MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK	4301 40C0h
15008h	32	MAIN_CTRL_MMR_CFG0_LOCK5_KICK0	4301 5008h
1500Ch	32	MAIN_CTRL_MMR_CFG0_LOCK5_KICK1	4301 500Ch
15100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY	4301 5100h
15104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY	4301 5104h
16000h	32	MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY	4301 6000h
16004h	32	MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY	4301 6004h
16080h	32	MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY	4301 6080h
160C0h	32	MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY	4301 60C0h
17008h	32	MAIN_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY	4301 7008h
1700Ch	32	MAIN_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY	4301 700Ch
17100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0	4301 7100h

Table 14-4469. MAIN_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	CTRL_MMR0 Physical Address
17104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1	4301 7104h
18170h	32	MAIN_CTRL_MMR_CFG0_RST_CTRL	4301 8170h
18174h	32	MAIN_CTRL_MMR_CFG0_RST_STAT	4301 8174h
18178h	32	MAIN_CTRL_MMR_CFG0_RST_SRC	4301 8178h
1817Ch	32	MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD	4301 817Ch
19008h	32	MAIN_CTRL_MMR_CFG0_LOCK6_KICK0	4301 9008h
1900Ch	32	MAIN_CTRL_MMR_CFG0_LOCK6_KICK1	4301 900Ch
19100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY	4301 9100h
19104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY	4301 9104h
19108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY	4301 9108h
1A170h	32	MAIN_CTRL_MMR_CFG0_RST_CTRL_PROXY	4301 A170h
1A174h	32	MAIN_CTRL_MMR_CFG0_RST_STAT_PROXY	4301 A174h
1A178h	32	MAIN_CTRL_MMR_CFG0_RST_SRC_PROXY	4301 A178h
1A17Ch	32	MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY	4301 A17Ch
1B008h	32	MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY	4301 B008h
1B00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY	4301 B00Ch
1B100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0	4301 B100h
1B104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1	4301 B104h
1B108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2	4301 B108h

14.2.1.1.1.2 main_ctrl_mmr Registers

main_ctrl_mmr Registers

14.2.1.1.1.2.1 MAIN_CTRL_MMR_CFG0_PID Register

1 MAIN_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800213h]

PID register

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Table 14-4470. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0000h**

Figure 14-1485. MAIN_CTRL_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM		PID_MINOR					
R		R					
0h		13h					

Table 14-4472. MAIN_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	13h	Reset Source: mod_g_rst_n

14.2.1.1.1.2.2 MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register

1 MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000BFh]

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Table 14-4473. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0008h**

Figure 14-1486. MAIN_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
BFh							

Table 14-4475. MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing activated Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.1.2.3 MAIN_CTRL_MMR_CFG0_JTAGID Register

1 MAIN_CTRL_MMR_CFG0_JTAGID Register (Offset = 14h) [reset = 1BB3802Fh]

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Table 14-4476. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0014h**

Figure 14-1487. MAIN_CTRL_MMR_CFG0_JTAGID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">JTAGID_VARIANT</td><td colspan="4">JTAGID_PARTNO</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">BB38h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">JTAGID_PARTNO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">BB38h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">JTAGID_PARTNO</td><td colspan="4">JTAGID_MFG</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">BB38h</td><td colspan="4">17h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">JTAGID_MFG</td><td>JTAGID_LSB</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">17h</td><td>1h</td></tr>
</table>

Table 14-4478. MAIN_CTRL_MMR_CFG0_JTAGID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	JTAGID_VARIANT	R	1h	Used to indicate new PGs Reset Source: mod_por_rst_n
27:12	JTAGID_PARTNO	R	BB38h	Part number for boundary scan Reset Source: mod_por_rst_n
11:1	JTAGID_MFG	R	17h	Indicates manufacturer Reset Source: mod_por_rst_n
0	JTAGID_LSB	R	1h	Always 1 Reset Source: mod_por_rst_n

14.2.1.1.1.2.4 MAIN_CTRL_MMR_CFG0_JTAG_USER_ID Register

1 MAIN_CTRL_MMR_CFG0_JTAG_USER_ID Register (Offset = 18h) [reset = 0h]

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Table 14-4479. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0018h**

Figure 14-1488. MAIN_CTRL_MMR_CFG0_JTAG_USER_ID Name Register

31	30	29	28	27	26	25	24
JTAG_USER_ID_USERCODE							
R							
X							
23	22	21	20	19	18	17	16
JTAG_USER_ID_USERCODE							
R							
X							
15	14	13	12	11	10	9	8
JTAG_USER_ID_USERCODE							
R							
X							
7	6	5	4	3	2	1	0
JTAG_USER_ID_USERCODE							
R							
X							

Table 14-4481. MAIN_CTRL_MMR_CFG0_JTAG_USER_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_USER_ID_USERCODE	R	X	Device information Reset Source: mod_por_rst_n

14.2.1.1.1.2.5 MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT Register

1 MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT Register (Offset = 30h) [reset = 0h]

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Table 14-4482. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 0030h

Figure 14-1489. MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAIN_DEVSTAT_BOOTMODE							
R/W							
0h							
7	6	5	4	3	2	1	0
MAIN_DEVSTAT_BOOTMODE							
R/W							
0h							

Table 14-4484. MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAIN_DEVSTAT_BOOTMODE	R/W	0h	Specifies the device Primary and Backup boot media. Reset Source: mod_por_rst_n

14.2.1.1.1.2.6 MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG Register

1 MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG Register (Offset = 34h) [reset = 0h]

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Table 14-4485. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0034h**

Figure 14-1490. MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAIN_BOOTCFG_BOOTMODE							
R							
0h							
7	6	5	4	3	2	1	0
MAIN_BOOTCFG_BOOTMODE							
R							
0h							

Table 14-4487. MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAIN_BOOTCFG_BOOTMODE	R	0h	Specifies the device Primary and Backup boot media as latched at PORz Reset Source: mod_por_rst_n

14.2.1.1.1.2.7 MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS Register

1 MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS Register (Offset = 44h) [reset = 0h]

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Table 14-4488. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0044h**

Figure 14-1491. MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS Name Register

31	30	29	28	27	26	25	24
BOOT_PROGRESS_PROGRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
BOOT_PROGRESS_PROGRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
BOOT_PROGRESS_PROGRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
BOOT_PROGRESS_PROGRESS							
R/W							
0h							

Table 14-4490. MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BOOT_PROGRESS_PROGRESS	R/W	0h	Written by ROM to indicate boot progression. Values and their meaning are determined by the ROM. Reset Source: mod_por_rst_n

14.2.1.1.1.2.8 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register

1 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register (Offset = 60h) [reset = 0h]

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Table 14-4491. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0060h**

Figure 14-1492. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				DEVICE_FEATURE0_R5FSS1_CORE1	DEVICE_FEATURE0_R5FSS1_CORE0	DEVICE_FEATURE0_R5FSS0_CORE1	DEVICE_FEATURE0_R5FSS0_CORE0
NONE				R	R	R	R
0h				X	X	X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						DEVICE_FEATURE0_MPU_CLUSTER0_CORE1	DEVICE_FEATURE0_MPU_CLUSTER0_CORE0
NONE						R	R
0h						X	X

Table 14-4493. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	DEVICE_FEATURE0_R5FSS1_CORE1	R	X	R5FSS1 CPU1 activated when set. CPU0 must also be activated. Reset Source: mod_por_rst_n
18	DEVICE_FEATURE0_R5FSS1_CORE0	R	X	R5FSS1 CPU0 activated when set. Reset Source: mod_por_rst_n
17	DEVICE_FEATURE0_R5FSS0_CORE1	R	X	R5FSS0 CPU1 activated when set. CPU0 must also be activated. Reset Source: mod_por_rst_n
16	DEVICE_FEATURE0_R5FSS0_CORE0	R	X	R5FSS0 CPU0 activated when set. Reset Source: mod_por_rst_n
15:2	RESERVED	NONE	0h	Reserved
1	DEVICE_FEATURE0_MPU_CLUSTER0_CORE1	R	X	MPU Cluster0 Core 1 is activated when set Reset Source: mod_por_rst_n
0	DEVICE_FEATURE0_MPU_CLUSTER0_CORE0	R	X	MPU Cluster0 Core 0 is activated when set Reset Source: mod_por_rst_n

14.2.1.1.1.2.9 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register

1 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register (Offset = 68h) [reset = 0h]

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Table 14-4494. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 0068h

Figure 14-1493. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					DEVICE_FEATURE2_CRYPTO_PKA_EN	DEVICE_FEATURE2_CRYPTO_ENCR_EN	DEVICE_FEATURE2_CRYPTO_SHA_EN
NONE					R	R	R
0h					X	X	X
7	6	5	4	3	2	1	0
DEVICE_FEATURE2_AES_AUTH_EN	RESERVED						DEVICE_FEATURE2_MCAN_FD_MODE
R	NONE						R
X	0h						X

Table 14-4496. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	DEVICE_FEATURE2_CRYPTO_PKA_EN	R	X	SA2_UL Crypto Module PKA activated Reset Source: mod_por_rst_n
9	DEVICE_FEATURE2_CRYPTO_ENCR_EN	R	X	SA2_UL Crypto Module AES/3DES/DBRG activated Reset Source: mod_por_rst_n
8	DEVICE_FEATURE2_CRYPTO_SHA_EN	R	X	SA2_UL Crypto Module SHA/MD5 activated Reset Source: mod_por_rst_n
7	DEVICE_FEATURE2_AES_AUTH_EN	R	X	AES authentication is activated in FlashSS and DMSC when set Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE2_MCAN_FD_MODE	R	X	FD mode is supported on MCAN[1:0] when set Reset Source: mod_por_rst_n

14.2.1.1.1.2.10 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register

1 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register (Offset = 78h) [reset = 0h]

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Table 14-4497. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0078h**

Figure 14-1494. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td>DEVICE_FEATURE6_MAIN_RESERVED_2</td><td>DEVICE_FEATURE6_MAIN_RESERVED_1</td><td>DEVICE_FEATURE6_MAIN_RESERVED_0</td></tr>
<tr><td colspan="5">NONE</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>DEVICE_FEATURE6_SPARE1</td><td>DEVICE_FEATURE6_SPARE0</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>DEVICE_FEATURE6_SA2_UL</td><td colspan="5">RESERVED</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td colspan="5">NONE</td></tr>
<tr><td colspan="2">0h</td><td>X</td><td colspan="5">0h</td></tr>
</table>

Table 14-4499. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	DEVICE_FEATURE6_MAIN_RESERVED_2	R	X	Main Domain Reserved 2 LPSC is activated when set
25	DEVICE_FEATURE6_MAIN_RESERVED_1	R	X	Main Domain Reserved 1 LPSC is activated when set
24	DEVICE_FEATURE6_MAIN_RESERVED_0	R	X	Main Domain Reserved 0 LPSC is activated when set
23:18	RESERVED	NONE	0h	Reserved
17	DEVICE_FEATURE6_SPARE1	R	X	Spare1 LPSC is activated when set Reset Source: mod_por_rst_n
16	DEVICE_FEATURE6_SPARE0	R	X	Spare0 LPSC is activated when set Reset Source: mod_por_rst_n
15:6	RESERVED	NONE	0h	Reserved
5	DEVICE_FEATURE6_SA2_UL	R	X	MAIN domain security accelerator is activated when set Reset Source: mod_por_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.11 MAIN_CTRL_MMR_CFG0_MAC_ID0 Register

1 MAIN_CTRL_MMR_CFG0_MAC_ID0 Register (Offset = 200h) [reset = 0h]

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Table 14-4500. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0200h**

Figure 14-1495. MAIN_CTRL_MMR_CFG0_MAC_ID0 Name Register

31	30	29	28	27	26	25	24
MAC_ID0_MACID_LO							
R/W							
X							
23	22	21	20	19	18	17	16
MAC_ID0_MACID_LO							
R/W							
X							
15	14	13	12	11	10	9	8
MAC_ID0_MACID_LO							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID0_MACID_LO							
R/W							
X							

Table 14-4502. MAIN_CTRL_MMR_CFG0_MAC_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAC_ID0_MACID_LO	R/W	X	32 lsbs of MAC address This register can be updated optionally through ROM. Reset Source: mod_g_rst_n

14.2.1.1.1.2.12 MAIN_CTRL_MMR_CFG0_MAC_ID1 Register

1 MAIN_CTRL_MMR_CFG0_MAC_ID1 Register (Offset = 204h) [reset = 0h]

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Table 14-4503. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0204h**

Figure 14-1496. MAIN_CTRL_MMR_CFG0_MAC_ID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ID1_MACID_HI							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID1_MACID_HI							
R/W							
X							

Table 14-4505. MAIN_CTRL_MMR_CFG0_MAC_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAC_ID1_MACID_HI	R/W	X	16 msbs of MAC address This register can be updated optionally through ROM. Reset Source: mod_g_rst_n

14.2.1.1.1.2.13 MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0 Register

1 MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0 Register (Offset = 210h) [reset = B010104Ch]

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Table 14-4506. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0210h**

Figure 14-1497. MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0 Name Register

31	30	29	28	27	26	25	24
PCI_DEVICE_ID0_ID0							
R/W							
B010104Ch							
23	22	21	20	19	18	17	16
PCI_DEVICE_ID0_ID0							
R/W							
B010104Ch							
15	14	13	12	11	10	9	8
PCI_DEVICE_ID0_ID0							
R/W							
B010104Ch							
7	6	5	4	3	2	1	0
PCI_DEVICE_ID0_ID0							
R/W							
B010104Ch							

Table 14-4508. MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCI_DEVICE_ID0_ID0	R/W	B010104Ch	ROM can optionally update this register with a 32 bit value from Customer OTP. Reset Source: mod_g_rst_n

14.2.1.1.1.2.14 MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1 Register

1 MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1 Register (Offset = 214h) [reset = B010104Ch]

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Table 14-4509. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0214h**

Figure 14-1498. MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1 Name Register

31	30	29	28	27	26	25	24
PCI_DEVICE_ID1_ID1							
R/W							
B010104Ch							
23	22	21	20	19	18	17	16
PCI_DEVICE_ID1_ID1							
R/W							
B010104Ch							
15	14	13	12	11	10	9	8
PCI_DEVICE_ID1_ID1							
R/W							
B010104Ch							
7	6	5	4	3	2	1	0
PCI_DEVICE_ID1_ID1							
R/W							
B010104Ch							

Table 14-4511. MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCI_DEVICE_ID1_ID1	R/W	B010104Ch	ROM can optionally update this register with a 32 bit value from Customer OTP. Reset Source: mod_g_rst_n

14.2.1.1.1.2.15 MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register

1 MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register (Offset = 220h) [reset = 61650451h]

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Table 14-4512. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0220h**

Figure 14-1499. MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0 Name Register

31	30	29	28	27	26	25	24
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
23	22	21	20	19	18	17	16
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
15	14	13	12	11	10	9	8
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
7	6	5	4	3	2	1	0
USB_DEVICE_ID0_ID0							
R/W							
61650451h							

Table 14-4514. MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USB_DEVICE_ID0_ID0	R/W	61650451h	ROM can optionally update this register with a 32 bit value from Customer OTP. Reset Source: mod_g_rst_n

14.2.1.1.1.2.16 MAIN_CTRL_MMR_CFG0_GP_SW0 Register

1 MAIN_CTRL_MMR_CFG0_GP_SW0 Register (Offset = 230h) [reset = 0h]

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Table 14-4515. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 0230h

Figure 14-1500. MAIN_CTRL_MMR_CFG0_GP_SW0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-4517. MAIN_CTRL_MMR_CFG0_GP_SW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.1.2.17 MAIN_CTRL_MMR_CFG0_GP_SW1 Register

1 MAIN_CTRL_MMR_CFG0_GP_SW1 Register (Offset = 234h) [reset = 0h]

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Table 14-4518. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 0234h

Figure 14-1501. MAIN_CTRL_MMR_CFG0_GP_SW1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-4520. MAIN_CTRL_MMR_CFG0_GP_SW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.1.2.18 MAIN_CTRL_MMR_CFG0_GP_SW2 Register

1 MAIN_CTRL_MMR_CFG0_GP_SW2 Register (Offset = 238h) [reset = 0h]

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Table 14-4521. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 0238h

Figure 14-1502. MAIN_CTRL_MMR_CFG0_GP_SW2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-4523. MAIN_CTRL_MMR_CFG0_GP_SW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.1.2.19 MAIN_CTRL_MMR_CFG0_GP_SW3 Register

1 MAIN_CTRL_MMR_CFG0_GP_SW3 Register (Offset = 23Ch) [reset = 0h]

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Table 14-4524. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 023Ch

Figure 14-1503. MAIN_CTRL_MMR_CFG0_GP_SW3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
NONE				R			
0h				X			

Table 14-4526. MAIN_CTRL_MMR_CFG0_GP_SW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	RESERVED	R	X	Reserved

14.2.1.1.1.2.20 MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT Register

1 MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT Register (Offset = 270h) [reset = 0h]

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Table 14-4527. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 0270h**

Figure 14-1504. MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT Name Register

31	30	29	28	27	26	25	24
CBA_ERR_STAT_DBG_CBA_ERR	RESERVED						
R	NONE						
X	0h						

23	22	21	20	19	18	17	16
RESERVED							CBA_ERR_STAT_MCU_CBA_ERR
NONE							R
0h							X

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED						CBA_ERR_STAT_MAIN_INFRA_CBA_ERR	CBA_ERR_STAT_MAIN_CBA_ERR
NONE						R	R
0h						X	X

Table 14-4529. MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CBA_ERR_STAT_DBG_CBA_ERR	R	X	Reset Source: mod_g_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	CBA_ERR_STAT_MCU_CBA_ERR	R	X	Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1	CBA_ERR_STAT_MAIN_INFRA_CBA_ERR	R	X	Reset Source: mod_g_rst_n
0	CBA_ERR_STAT_MAIN_CBA_ERR	R	X	Reset Source: mod_g_rst_n

14.2.1.1.1.2.21 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-4530. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1008h**

Figure 14-1505. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-4532. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.22 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-4533. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 100Ch**

Figure 14-1506. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-4535. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.23 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-4536. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1010h**

Figure 14-1507. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-4538. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.24 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-4539. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 1014h

Figure 14-1508. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-4541. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.25 MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-4542. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 1018h

Figure 14-1509. MAIN_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-4544. MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.26 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-4545. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 101Ch**

Figure 14-1510. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-4547. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.27 MAIN_CTRL_MMR_CFG0_EOI Register

1 MAIN_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-4548. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1020h**

Figure 14-1511. MAIN_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-4550. MAIN_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.1.2.28 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-4551. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1024h**

Figure 14-1512. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-4553. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.1.2.29 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-4554. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 1028h

Figure 14-1513. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-4556. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.1.2.30 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-4557. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 102Ch**

Figure 14-1514. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 14-4559. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.1.2.31 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-4560. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1030h**

Figure 14-1515. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-4562. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.32 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4563. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1100h**

Figure 14-1516. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4565. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.33 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register (Offset = 1104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4566. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1104h**

Figure 14-1517. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1_READONLY							
R							
0h							

Table 14-4568. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.34 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register (Offset = 1108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4569. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1108h**

Figure 14-1518. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4571. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.35 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register (Offset = 110Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-4572. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 110Ch**

Figure 14-1519. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P0_R3_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P0_R3_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P0_R3_READONLY							
R							
0h							

Table 14-4574. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.36 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register (Offset = 1110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4575. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1110h**

Figure 14-1520. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4_READONLY							
R							
0h							

Table 14-4577. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.37 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register (Offset = 1114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4578. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1114h**

Figure 14-1521. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5_READONLY							
R							
0h							

Table 14-4580. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.38 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register (Offset = 1118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4581. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 1118h**

Figure 14-1522. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R6_READONLY							
R							
0h							

Table 14-4583. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.39 MAIN_CTRL_MMR_CFG0_PID_PROXY Register

1 MAIN_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800213h]

PID register

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Table 14-4584. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2000h**

Figure 14-1523. MAIN_CTRL_MMR_CFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16_PROXY							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		13h					

Table 14-4586. MAIN_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	13h	Reset Source: mod_g_rst_n

14.2.1.1.1.2.40 MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000BFh]

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Table 14-4587. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2008h**

Figure 14-1524. MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS_PROXY							
R							
BFh							

Table 14-4589. MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing activated Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.1.2.41 MAIN_CTRL_MMR_CFG0_JTAGID_PROXY Register

1 MAIN_CTRL_MMR_CFG0_JTAGID_PROXY Register (Offset = 2014h) [reset = 1BB3802Fh]

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Table 14-4590. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2014h**

Figure 14-1525. MAIN_CTRL_MMR_CFG0_JTAGID_PROXY Name Register

31	30	29	28	27	26	25	24
JTAGID_VARIANT_PROXY				JTAGID_PARTNO_PROXY			
R				R			
1h				BB38h			
23	22	21	20	19	18	17	16
JTAGID_PARTNO_PROXY							
R							
BB38h							
15	14	13	12	11	10	9	8
JTAGID_PARTNO_PROXY				JTAGID_MFG_PROXY			
R				R			
BB38h				17h			
7	6	5	4	3	2	1	0
JTAGID_MFG_PROXY							JTAGID_LSB_PROXY
R							R
17h							1h

Table 14-4592. MAIN_CTRL_MMR_CFG0_JTAGID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	JTAGID_VARIANT_PROXY	R	1h	Used to indicate new PGs Reset Source: mod_por_rst_n
27:12	JTAGID_PARTNO_PROXY	R	BB38h	Part number for boundary scan Reset Source: mod_por_rst_n
11:1	JTAGID_MFG_PROXY	R	17h	Indicates manufacturer Reset Source: mod_por_rst_n
0	JTAGID_LSB_PROXY	R	1h	Always 1 Reset Source: mod_por_rst_n

14.2.1.1.1.2.42 MAIN_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Register

1 MAIN_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Register (Offset = 2018h) [reset = 0h]

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Table 14-4593. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2018h

Figure 14-1526. MAIN_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Name Register

31	30	29	28	27	26	25	24
JTAG_USER_ID_USERCODE_PROXY							
R							
X							
23	22	21	20	19	18	17	16
JTAG_USER_ID_USERCODE_PROXY							
R							
X							
15	14	13	12	11	10	9	8
JTAG_USER_ID_USERCODE_PROXY							
R							
X							
7	6	5	4	3	2	1	0
JTAG_USER_ID_USERCODE_PROXY							
R							
X							

Table 14-4595. MAIN_CTRL_MMR_CFG0_JTAG_USER_ID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_USER_ID_USERCODE_PROXY	R	X	Device information Reset Source: mod_por_rst_n

14.2.1.1.1.2.43 MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY Register (Offset = 2030h) [reset = 0h]

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Table 14-4596. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2030h

Figure 14-1527. MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAIN_DEVSTAT_BOOTMODE_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
MAIN_DEVSTAT_BOOTMODE_PROXY							
R/W							
0h							

Table 14-4598. MAIN_CTRL_MMR_CFG0_MAIN_DEVSTAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAIN_DEVSTAT_BOOTMODE_PROXY	R/W	0h	Specifies the device Primary and Backup boot media. Reset Source: mod_por_rst_n

14.2.1.1.1.2.44 MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY Register (Offset = 2034h) [reset = 0h]

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Table 14-4599. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2034h**

Figure 14-1528. MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAIN_BOOTCFG_BOOTMODE_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
MAIN_BOOTCFG_BOOTMODE_PROXY							
R							
0h							

Table 14-4601. MAIN_CTRL_MMR_CFG0_MAIN_BOOTCFG_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAIN_BOOTCFG_BOOTMODE_PROXY	R	0h	Specifies the device Primary and Backup boot media as latched at PORz Reset Source: mod_por_rst_n

14.2.1.1.1.2.45 MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register (Offset = 2044h) [reset = 0h]

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Table 14-4602. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2044h

Figure 14-1529. MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Name Register

31	30	29	28	27	26	25	24
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							

Table 14-4604. MAIN_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BOOT_PROGRESS_PROGRESS_PROXY	R/W	0h	Written by ROM to indicate boot progression. Values and their meaning are determined by the ROM. Reset Source: mod_por_rst_n

14.2.1.1.1.2.46 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register (Offset = 2060h) [reset = 0h]

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Table 14-4605. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2060h

Figure 14-1530. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				DEVICE_FEATURE0_R5FSS1_CORE1_PROXY	DEVICE_FEATURE0_R5FSS1_CORE0_PROXY	DEVICE_FEATURE0_R5FSS0_CORE1_PROXY	DEVICE_FEATURE0_R5FSS0_CORE0_PROXY
NONE				R	R	R	R
0h				X	X	X	X
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DEVICE_FEATURE0_MPU_CLUSTER0_CORE1_PROXY	DEVICE_FEATURE0_MPU_CLUSTER0_CORE0_PROXY
NONE						R	R
0h						X	X

Table 14-4607. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	DEVICE_FEATURE0_R5FSS1_CORE1_PROXY	R	X	R5FSS1 CPU1 activated when set. CPU0 must also be activated. Reset Source: mod_por_rst_n
18	DEVICE_FEATURE0_R5FSS1_CORE0_PROXY	R	X	R5FSS1 CPU0 activated when set. Reset Source: mod_por_rst_n
17	DEVICE_FEATURE0_R5FSS0_CORE1_PROXY	R	X	R5FSS0 CPU1 activated when set. CPU0 must also be activated. Reset Source: mod_por_rst_n
16	DEVICE_FEATURE0_R5FSS0_CORE0_PROXY	R	X	R5FSS0 CPU0 activated when set. Reset Source: mod_por_rst_n
15:2	RESERVED	NONE	0h	Reserved
1	DEVICE_FEATURE0_MPU_CLUSTER0_CORE1_PROXY	R	X	MPU Cluster0 Core 1 is activated when set Reset Source: mod_por_rst_n

Table 14-4607. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DEVICE_FEATURE0_MPU_CLUSTER0_CORE0_PROXY	R	X	MPU Cluster0 Core 0 is activated when set Reset Source: mod_por_rst_n

14.2.1.1.1.2.47 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register (Offset = 2068h) [reset = 0h]

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Table 14-4608. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2068h**

Figure 14-1531. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					DEVICE_FEATURE2_CRYPTO_PKA_EN_PROXY	DEVICE_FEATURE2_CRYPTO_ENCR_EN_PROXY	DEVICE_FEATURE2_CRYPTO_SHA_EN_PROXY
NONE					R	R	R
0h					X	X	X
7	6	5	4	3	2	1	0
DEVICE_FEATURE2_AES_AUTH_EN_PROXY	RESERVED						DEVICE_FEATURE2_MCAN_FD_MODE_PROXY
R	NONE						R
X	0h						X

Table 14-4610. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	DEVICE_FEATURE2_CRYPTO_PKA_EN_PROXY	R	X	SA2_UL Crypto Module PKA activated Reset Source: mod_por_rst_n
9	DEVICE_FEATURE2_CRYPTO_ENCR_EN_PROXY	R	X	SA2_UL Crypto Module AES/3DES/DBRG activated Reset Source: mod_por_rst_n
8	DEVICE_FEATURE2_CRYPTO_SHA_EN_PROXY	R	X	SA2_UL Crypto Module SHA/MD5 activated Reset Source: mod_por_rst_n
7	DEVICE_FEATURE2_AES_AUTH_EN_PROXY	R	X	AES authentication is activated in FlashSS and DMSC when set Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE2_MCAN_FD_MODE_PROXY	R	X	FD mode is supported on MCAN[1:0] when set Reset Source: mod_por_rst_n

14.2.1.1.1.2.48 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register (Offset = 2078h) [reset = 0h]

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Table 14-4611. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2078h

Figure 14-1532. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED					DEVICE_FEATURE6_MAIN_RESERVED_2_PROXY	DEVICE_FEATURE6_MAIN_RESERVED_1_PROXY	DEVICE_FEATURE6_MAIN_RESERVED_0_PROXY
NONE					R	R	R
0h					X	X	X
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						DEVICE_FEATURE6_SPARE1_PROXY	DEVICE_FEATURE6_SPARE0_PROXY
NONE						R	R
0h						X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		DEVICE_FEATURE6_SA2_UL_PROXY	RESERVED				
NONE		R	NONE				
0h		X	0h				

Table 14-4613. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	DEVICE_FEATURE6_MAIN_RESERVED_2_PROXY	R	X	Main Domain Reserved 2 LPSC is activated when set
25	DEVICE_FEATURE6_MAIN_RESERVED_1_PROXY	R	X	Main Domain Reserved 1 LPSC is activated when set
24	DEVICE_FEATURE6_MAIN_RESERVED_0_PROXY	R	X	Main Domain Reserved 0 LPSC is activated when set
23:18	RESERVED	NONE	0h	Reserved
17	DEVICE_FEATURE6_SPARE1_PROXY	R	X	Spare1 LPSC is activated when set Reset Source: mod_por_rst_n
16	DEVICE_FEATURE6_SPARE0_PROXY	R	X	Spare0 LPSC is activated when set Reset Source: mod_por_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-4613. MAIN_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DEVICE_FEATURE6_SA2_UL_PROXY	R	X	MAIN domain security accelerator is activated when set Reset Source: mod_por_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.49 MAIN_CTRL_MMR_CFG0_MAC_ID0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAC_ID0_PROXY Register (Offset = 2200h) [reset = 0h]

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Table 14-4614. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2200h

Figure 14-1533. MAIN_CTRL_MMR_CFG0_MAC_ID0_PROXY Name Register

31	30	29	28	27	26	25	24
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
23	22	21	20	19	18	17	16
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
15	14	13	12	11	10	9	8
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID0_MACID_LO_PROXY							
R/W							
X							

Table 14-4616. MAIN_CTRL_MMR_CFG0_MAC_ID0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAC_ID0_MACID_LO_PROXY	R/W	X	32 lsbs of MAC address This register can be updated optionally through ROM. Reset Source: mod_g_rst_n

14.2.1.1.1.2.50 MAIN_CTRL_MMR_CFG0_MAC_ID1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAC_ID1_PROXY Register (Offset = 2204h) [reset = 0h]

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Table 14-4617. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2204h**

Figure 14-1534. MAIN_CTRL_MMR_CFG0_MAC_ID1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAC_ID1_MACID_HI_PROXY							
R/W							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAC_ID1_MACID_HI_PROXY							
R/W							
X							

Table 14-4619. MAIN_CTRL_MMR_CFG0_MAC_ID1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAC_ID1_MACID_HI_PROXY	R/W	X	16 msbs of MAC address This register can be updated optionally through ROM. Reset Source: mod_g_rst_n

14.2.1.1.1.2.51 MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0_PROXY Register (Offset = 2210h) [reset = B010104Ch]

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Table 14-4620. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2210h**

Figure 14-1535. MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0_PROXY Name Register

31	30	29	28	27	26	25	24
PCI_DEVICE_ID0_ID0_PROXY							
R/W							
B010104Ch							
23	22	21	20	19	18	17	16
PCI_DEVICE_ID0_ID0_PROXY							
R/W							
B010104Ch							
15	14	13	12	11	10	9	8
PCI_DEVICE_ID0_ID0_PROXY							
R/W							
B010104Ch							
7	6	5	4	3	2	1	0
PCI_DEVICE_ID0_ID0_PROXY							
R/W							
B010104Ch							

Table 14-4622. MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCI_DEVICE_ID0_ID0_PROXY	R/W	B010104Ch	ROM can optionally update this register with a 32 bit value from Customer OTP. Reset Source: mod_g_rst_n

14.2.1.1.1.2.52 MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1_PROXY Register (Offset = 2214h) [reset = B010104Ch]

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Table 14-4623. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2214h**

Figure 14-1536. MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1_PROXY Name Register

31	30	29	28	27	26	25	24
PCI_DEVICE_ID1_ID1_PROXY							
R/W							
B010104Ch							
23	22	21	20	19	18	17	16
PCI_DEVICE_ID1_ID1_PROXY							
R/W							
B010104Ch							
15	14	13	12	11	10	9	8
PCI_DEVICE_ID1_ID1_PROXY							
R/W							
B010104Ch							
7	6	5	4	3	2	1	0
PCI_DEVICE_ID1_ID1_PROXY							
R/W							
B010104Ch							

Table 14-4625. MAIN_CTRL_MMR_CFG0_PCI_DEVICE_ID1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCI_DEVICE_ID1_ID1_PROXY	R/W	B010104Ch	ROM can optionally update this register with a 32 bit value from Customer OTP. Reset Source: mod_g_rst_n

14.2.1.1.1.2.53 MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register (Offset = 2220h) [reset = 61650451h]

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Table 14-4626. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2220h**

Figure 14-1537. MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Name Register

31	30	29	28	27	26	25	24
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
23	22	21	20	19	18	17	16
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
15	14	13	12	11	10	9	8
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
7	6	5	4	3	2	1	0
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							

Table 14-4628. MAIN_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USB_DEVICE_ID0_ID0_PROXY	R/W	61650451h	ROM can optionally update this register with a 32 bit value from Customer OTP. Reset Source: mod_g_rst_n

14.2.1.1.1.2.54 MAIN_CTRL_MMR_CFG0_GP_SW0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_GP_SW0_PROXY Register (Offset = 2230h) [reset = 0h]

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Table 14-4629. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 2230h**

Figure 14-1538. MAIN_CTRL_MMR_CFG0_GP_SW0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
X							

Table 14-4631. MAIN_CTRL_MMR_CFG0_GP_SW0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.1.2.55 MAIN_CTRL_MMR_CFG0_GP_SW1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_GP_SW1_PROXY Register (Offset = 2234h) [reset = 0h]

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Table 14-4632. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2234h

Figure 14-1539. MAIN_CTRL_MMR_CFG0_GP_SW1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-4634. MAIN_CTRL_MMR_CFG0_GP_SW1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.1.2.56 MAIN_CTRL_MMR_CFG0_GP_SW2_PROXY Register

1 MAIN_CTRL_MMR_CFG0_GP_SW2_PROXY Register (Offset = 2238h) [reset = 0h]

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Table 14-4635. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2238h

Figure 14-1540. MAIN_CTRL_MMR_CFG0_GP_SW2_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
X							
23	22	21	20	19	18	17	16
RESERVED							
R							
X							
15	14	13	12	11	10	9	8
RESERVED							
R							
X							
7	6	5	4	3	2	1	0
RESERVED							
R							
X							

Table 14-4637. MAIN_CTRL_MMR_CFG0_GP_SW2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	X	Reserved

14.2.1.1.1.2.57 MAIN_CTRL_MMR_CFG0_GP_SW3_PROXY Register

1 MAIN_CTRL_MMR_CFG0_GP_SW3_PROXY Register (Offset = 223Ch) [reset = 0h]

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Table 14-4638. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 223Ch

Figure 14-1541. MAIN_CTRL_MMR_CFG0_GP_SW3_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
NONE				R			
0h				X			

Table 14-4640. MAIN_CTRL_MMR_CFG0_GP_SW3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	RESERVED	R	X	Reserved

14.2.1.1.1.2.58 MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register (Offset = 2270h) [reset = 0h]

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Table 14-4641. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 2270h

Figure 14-1542. MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CBA_ERR_STAT_DBG_CBA_ERR_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>X</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>CBA_ERR_STAT_MCU_CBA_ERR_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CBA_ERR_STAT_MAIN_INFRA_CBA_ERR_PROXY</td><td>CBA_ERR_STAT_MAIN_CBA_ERR_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>X</td></tr>
</table>

Table 14-4643. MAIN_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CBA_ERR_STAT_DBG_CBA_ERR_PROXY	R	X	Reset Source: mod_g_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	CBA_ERR_STAT_MCU_CBA_ERR_PROXY	R	X	Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1	CBA_ERR_STAT_MAIN_INFRA_CBA_ERR_PROXY	R	X	Reset Source: mod_g_rst_n
0	CBA_ERR_STAT_MAIN_CBA_ERR_PROXY	R	X	Reset Source: mod_g_rst_n

14.2.1.1.1.2.59 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-4644. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 3008h

Figure 14-1543. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-4646. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.60 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-4647. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 300Ch**

Figure 14-1544. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-4649. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.61 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-4650. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3010h**

Figure 14-1545. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-4652. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.62 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-4653. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3014h**

Figure 14-1546. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-4655. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.63 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-4656. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 3018h

Figure 14-1547. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-4658. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.64 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-4659. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 301Ch**

Figure 14-1548. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-4661. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.65 MAIN_CTRL_MMR_CFG0_EOI_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-4662. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3020h**

Figure 14-1549. MAIN_CTRL_MMR_CFG0_EOI_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_VECTOR_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4664. MAIN_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.1.2.66 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-4665. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3024h**

Figure 14-1550. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-4667. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.1.2.67 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-4668. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3028h**

Figure 14-1551. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-4670. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.1.2.68 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-4671. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 302Ch**

Figure 14-1552. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-4673. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.1.2.69 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-4674. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3030h**

Figure 14-1553. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>FAULT_CLR_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-4676. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.70 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4677. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3100h**

Figure 14-1554. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-4679. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.71 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register (Offset = 3104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4680. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3104h**

Figure 14-1555. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1							
R/W							
0h							

Table 14-4682. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.72 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register (Offset = 3108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4683. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3108h**

Figure 14-1556. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2							
R/W							
0h							

Table 14-4685. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.73 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register (Offset = 310Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-4686. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 310Ch**

Figure 14-1557. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4688. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.74 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register (Offset = 3110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4689. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3110h**

Figure 14-1558. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4691. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.75 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register (Offset = 3114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4692. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3114h**

Figure 14-1559. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5							
R/W							
0h							

Table 14-4694. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.76 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register (Offset = 3118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4695. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 3118h**

Figure 14-1560. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R6							
R/W							
0h							

Table 14-4697. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.77 MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL Register (Offset = 4008h) [reset = 80000004h]

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Table 14-4698. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 4008h

Figure 14-1561. MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL Name Register

31	30	29	28	27	26	25	24
RSVD	RESERVED						
	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED						USB0_PHY_CTRL_LOOPBACK_MODE	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
USB0_PHY_CTRL_PLL_STANDALONE	RESERVED			USB0_PHY_CTRL_PLL_CLKOUT_ON	RESERVED	USB0_PHY_CTRL_PLL_CLKOUT_SEL	
R/W	NONE			R/W	NONE	R/W	
0h	0h			0h	0h	0h	
7	6	5	4	3	2	1	0
RESERVED				USB0_PHY_CTRL_PLL_REF_SEL			
NONE				R/W			
0h				4h			

Table 14-4700. MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
30:18	RESERVED	NONE	0h	Reserved
17:16	USB0_PHY_CTRL_LOOPBACK_MODE	R/W	0h	Activates USB0 PHY loopback operation Reset Source: mod_g_rst_n
15	USB0_PHY_CTRL_PLL_STANDALONE	R/W	0h	Activates USB0 PHY as a standalone PLL Reset Source: mod_g_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	USB0_PHY_CTRL_PLL_CLKOUT_ON	R/W	0h	Controls USB0 PLL clock output Reset Source: mod_g_rst_n
10	RESERVED	NONE	0h	Reserved
9:8	USB0_PHY_CTRL_PLL_CLKOUT_SEL	R/W	0h	Selects the frequency of the USB0 PLL output clock Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	USB0_PHY_CTRL_PLL_REF_SEL	R/W	4h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should match the frequency value of either the HFOSC0 or HFOSC1 oscillator as selected by the USB0_CLKSEL register Reset Source: mod_g_rst_n

14.2.1.1.1.2.78 MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register (Offset = 4044h) [reset = 2h]

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Table 14-4701. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4044h**

Figure 14-1562. MAIN_CTRL_MMR_CFG0_ENET1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	ENET1_CTRL_PORT_MODE_SEL		
NONE			NONE	NONE	R/W		
0h			0h	0h	2h		

Table 14-4703. MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET1_CTRL_PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port1 interface Reset Source: sys_por_rst_n

14.2.1.1.1.2.79 MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register

1 MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register (Offset = 4048h) [reset = 2h]

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Table 14-4704. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4048h**

Figure 14-1563. MAIN_CTRL_MMR_CFG0_ENET2_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>RESERVED</td><td>RESERVED</td><td colspan="3">ENET2_CTRL_PORT_MODE_SEL</td></tr>
<tr><td colspan="3">NONE</td><td>NONE</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
</table>

Table 14-4706. MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET2_CTRL_PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port2 interface Reset Source: sys_por_rst_n

14.2.1.1.1.2.80 MAIN_CTRL_MMR_CFG0_PCIE0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_PCIE0_CTRL Register (Offset = 4070h) [reset = 1h]

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Table 14-4707. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 4070h

Figure 14-1564. MAIN_CTRL_MMR_CFG0_PCIE0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCIE0_CTRL_MODE_SEL	RESERVED					PCIE0_CTRL_GENERATION_SEL	
R/W	NONE					R/W	
0h	0h					1h	

Table 14-4709. MAIN_CTRL_MMR_CFG0_PCIE0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PCIE0_CTRL_MODE_SEL	R/W	0h	Selects the operating mode Reset Source: mod_g_rst_n
6:2	RESERVED	NONE	0h	Reserved
1:0	PCIE0_CTRL_GENERATION_SEL	R/W	1h	Configures the PCIe generation support in the PCIe capabilities linked-list Reset Source: mod_g_rst_n

14.2.1.1.1.2.81 MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL Register (Offset = 4080h) [reset = 0h]

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Table 14-4710. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4080h**

Figure 14-1565. MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SERDES0_LN0_CTRL_LANE_FUNC_SEL	
NONE						R/W	
0h						0h	

Table 14-4712. MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SERDES0_LN0_CTRL_LANE_FUNC_SEL	R/W	0h	Selects the SERDES0 lane0 function Reset Source: sys_por_rst_n

14.2.1.1.1.2.82 MAIN_CTRL_MMR_CFG0_ADC0_TRIM Register

1 MAIN_CTRL_MMR_CFG0_ADC0_TRIM Register (Offset = 40C0h) [reset = 0h]

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Table 14-4713. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 40C0h**

Figure 14-1566. MAIN_CTRL_MMR_CFG0_ADC0_TRIM Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">ADC0_TRIM_TRIM5</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ADC0_TRIM_TRIM4</td><td colspan="3">ADC0_TRIM_TRIM3</td><td colspan="2">ADC0_TRIM_TRIM2</td></tr>
<tr><td colspan="3">R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">X</td><td colspan="3">X</td><td colspan="2">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">ADC0_TRIM_TRIM2</td><td colspan="4">ADC0_TRIM_TRIM1</td><td colspan="2">ADC0_TRIM_ENABLE_CALB</td></tr>
<tr><td colspan="2">R/W</td><td colspan="4">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">X</td><td colspan="4">X</td><td colspan="2">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">ADC0_TRIM_ENABLE_CALB</td><td colspan="5">ADC0_TRIM_ENABLE_CAL</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">X</td><td colspan="5">X</td></tr>
</table>

Table 14-4715. MAIN_CTRL_MMR_CFG0_ADC0_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	ADC0_TRIM_TRIM5	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
23:21	ADC0_TRIM_TRIM4	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
20:18	ADC0_TRIM_TRIM3	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
17:14	ADC0_TRIM_TRIM2	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
13:10	ADC0_TRIM_TRIM1	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
9:5	ADC0_TRIM_ENABLE_CALB	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
4:0	ADC0_TRIM_ENABLE_CAL	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n

14.2.1.1.1.2.83 MAIN_CTRL_MMR_CFG0_SERDES0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_SERDES0_CTRL Register (Offset = 40E0h) [reset = 0h]

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Table 14-4716. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 40E0h

Figure 14-1567. MAIN_CTRL_MMR_CFG0_SERDES0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			SERDES0_CTRL_REF_SEL	RESERVED			SERDES0_CTRL_RET_EN
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4718. MAIN_CTRL_MMR_CFG0_SERDES0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	SERDES0_CTRL_REF_SEL	R/W	0h	REFCLK output select Reset Source: sys_por_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	SERDES0_CTRL_RET_EN	R/W	0h	Retention activate Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.84 MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0 Register

1 MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0 Register (Offset = 4100h) [reset = 0h]

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Table 14-4719. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4100h**

Figure 14-1568. MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							ICSSG0_CTRL0_RGMII0_ID_MODE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				ICSSG0_CTRL0_GPM_BIDI			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ICSSG0_CTRL0_GPM_BIDI							
R/W							
0h							
7	6	5	4	3	2	1	0
ICSSG0_CTRL0_GPM_BIDI							
R/W							
0h							

Table 14-4721. MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ICSSG0_CTRL0_RGMII0_ID_MODE	R/W	0h	Controls the ICSS_G0 RGMII0 port internal transmit delay Reset Source: sys_por_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	ICSSG0_CTRL0_GPM_BIDI	R/W	0h	Controls operation of the ICSS_G0 PRU0_GPO pins. Each bit n controls the corresponding PRG0_PRU0GPOn I/O Reset Source: sys_por_rst_n

14.2.1.1.1.2.85 MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1 Register

1 MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1 Register (Offset = 4104h) [reset = 0h]

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Table 14-4722. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4104h**

Figure 14-1569. MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							ICSSG0_CTRL1_RGMII1_ID_MODE
NONE							R/W
0h							0h

23	22	21	20	19	18	17	16
RESERVED				ICSSG0_CTRL1_GPM_BIDI			
NONE				R/W			
0h				0h			

15	14	13	12	11	10	9	8
ICSSG0_CTRL1_GPM_BIDI							
R/W							
0h							

7	6	5	4	3	2	1	0
ICSSG0_CTRL1_GPM_BIDI							
R/W							
0h							

Table 14-4724. MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ICSSG0_CTRL1_RGMII1_ID_MODE	R/W	0h	Controls the ICSS_G0 RGMII1 port internal transmit delay Reset Source: sys_por_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	ICSSG0_CTRL1_GPM_BIDI	R/W	0h	Controls operation of the ICSS_G0 PRU1_GPO pins. Each bit n controls the corresponding PRG0_PRU1GPOn I/O Reset Source: sys_por_rst_n

14.2.1.1.1.2.86 MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0 Register

1 MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0 Register (Offset = 4110h) [reset = 0h]

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Table 14-4725. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4110h**

Figure 14-1570. MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							ICSSG1_CTRL0_RGMII0_ID_MODE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				ICSSG1_CTRL0_GPM_BIDI			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ICSSG1_CTRL0_GPM_BIDI							
R/W							
0h							
7	6	5	4	3	2	1	0
ICSSG1_CTRL0_GPM_BIDI							
R/W							
0h							

Table 14-4727. MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ICSSG1_CTRL0_RGMII0_ID_MODE	R/W	0h	Controls the ICSS_G1 RGMII0 port internal transmit delay Reset Source: sys_por_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	ICSSG1_CTRL0_GPM_BIDI	R/W	0h	Controls operation of the ICSS_G1 PRU0_GPO pins. Each bit n controls the corresponding PRG1_PRU0GPOn I/O Reset Source: sys_por_rst_n

14.2.1.1.1.2.87 MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1 Register

1 MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1 Register (Offset = 4114h) [reset = 0h]

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Table 14-4728. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4114h**

Figure 14-1571. MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							ICSSG1_CTRL1_RGMII1_ID_MODE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				ICSSG1_CTRL1_GPM_BIDI			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ICSSG1_CTRL1_GPM_BIDI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ICSSG1_CTRL1_GPM_BIDI							
R/W							
0h							

Table 14-4730. MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ICSSG1_CTRL1_RGMII1_ID_MODE	R/W	0h	Controls the ICSS_G1 RGMII1 port internal transmit delay Reset Source: sys_por_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	ICSSG1_CTRL1_GPM_BIDI	R/W	0h	Controls operation of the ICSS_G1 PRU1_GPO pins. Each bit n controls the corresponding PRG1_PRU1GPOn I/O Reset Source: sys_por_rst_n

14.2.1.1.1.2.88 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register

1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register (Offset = 4130h) [reset = 0h]

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Table 14-4731. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**4300 4130h**

Figure 14-1572. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							EPWM_TB_CLKEN_EPWM8_TB_CLKEN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
EPWM_TB_CLKEN_EPWM7_TB_CLKEN	EPWM_TB_CLKEN_EPWM6_TB_CLKEN	EPWM_TB_CLKEN_EPWM5_TB_CLKEN	EPWM_TB_CLKEN_EPWM4_TB_CLKEN	EPWM_TB_CLKEN_EPWM3_TB_CLKEN	EPWM_TB_CLKEN_EPWM2_TB_CLKEN	EPWM_TB_CLKEN_EPWM1_TB_CLKEN	EPWM_TB_CLKEN_EPWM0_TB_CLKEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4733. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	EPWM_TB_CLKEN_EPWM8_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM8 When Set Reset Source: mod_g_rst_n
7	EPWM_TB_CLKEN_EPWM7_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM7 When Set Reset Source: mod_g_rst_n
6	EPWM_TB_CLKEN_EPWM6_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM6 When Set Reset Source: mod_g_rst_n
5	EPWM_TB_CLKEN_EPWM5_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM5 When Set Reset Source: mod_g_rst_n
4	EPWM_TB_CLKEN_EPWM4_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM4 When Set Reset Source: mod_g_rst_n
3	EPWM_TB_CLKEN_EPWM3_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM3 When Set Reset Source: mod_g_rst_n
2	EPWM_TB_CLKEN_EPWM2_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM2 When Set Reset Source: mod_g_rst_n

Table 14-4733. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EPWM_TB_CLKEN_EPWM1_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM1 When Set Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_EPWM0_TB_CLKEN	R/W	0h	Activates Timebase Clock of EPWM0 When Set Reset Source: mod_g_rst_n

14.2.1.1.1.2.89 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET Register

1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET Register (Offset = 4134h) [reset = 0h]

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Table 14-4734. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 4134h

Figure 14-1573. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							EPWM_TB_CLKEN_SET_EPWM8_TB_CLKEN
NONE							R/W1TS
0h							0h
7	6	5	4	3	2	1	0
EPWM_TB_CLKEN_SET_EPWM7_TB_CLKEN	EPWM_TB_CLKEN_SET_EPWM6_TB_CLKEN	EPWM_TB_CLKEN_SET_EPWM5_TB_CLKEN	EPWM_TB_CLKEN_SET_EPWM4_TB_CLKEN	EPWM_TB_CLKEN_SET_EPWM3_TB_CLKEN	EPWM_TB_CLKEN_SET_EPWM2_TB_CLKEN	EPWM_TB_CLKEN_SET_EPWM1_TB_CLKEN	EPWM_TB_CLKEN_SET_EPWM0_TB_CLKEN
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4736. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	EPWM_TB_CLKEN_SET_EPWM8_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM8 Reset Source: mod_g_rst_n
7	EPWM_TB_CLKEN_SET_EPWM7_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM7 Reset Source: mod_g_rst_n
6	EPWM_TB_CLKEN_SET_EPWM6_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM6 Reset Source: mod_g_rst_n
5	EPWM_TB_CLKEN_SET_EPWM5_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM5 Reset Source: mod_g_rst_n
4	EPWM_TB_CLKEN_SET_EPWM4_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM4 Reset Source: mod_g_rst_n
3	EPWM_TB_CLKEN_SET_EPWM3_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM3 Reset Source: mod_g_rst_n

Table 14-4736. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EPWM_TB_CLKEN_SET_EPWM2_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM2 Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_SET_EPWM1_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM1 Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_SET_EPWM0_TB_CLKEN	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.90 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR Register

1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR Register (Offset = 4138h) [reset = 0h]

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Table 14-4737. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4138h**

Figure 14-1574. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							EPWM_TB_CLKEN_CLR_EPWM8_TB_CLKEN
NONE							R/W1TC
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EPWM_TB_CLKEN_CLR_EPWM7_TB_CLKEN	EPWM_TB_CLKEN_CLR_EPWM6_TB_CLKEN	EPWM_TB_CLKEN_CLR_EPWM5_TB_CLKEN	EPWM_TB_CLKEN_CLR_EPWM4_TB_CLKEN	EPWM_TB_CLKEN_CLR_EPWM3_TB_CLKEN	EPWM_TB_CLKEN_CLR_EPWM2_TB_CLKEN	EPWM_TB_CLKEN_CLR_EPWM1_TB_CLKEN	EPWM_TB_CLKEN_CLR_EPWM0_TB_CLKEN
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4739. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	EPWM_TB_CLKEN_CLR_EPWM8_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM8 Reset Source: mod_g_rst_n
7	EPWM_TB_CLKEN_CLR_EPWM7_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM7 Reset Source: mod_g_rst_n
6	EPWM_TB_CLKEN_CLR_EPWM6_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM6 Reset Source: mod_g_rst_n
5	EPWM_TB_CLKEN_CLR_EPWM5_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM5 Reset Source: mod_g_rst_n
4	EPWM_TB_CLKEN_CLR_EPWM4_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM4 Reset Source: mod_g_rst_n
3	EPWM_TB_CLKEN_CLR_EPWM3_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM3 Reset Source: mod_g_rst_n

Table 14-4739. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EPWM_TB_CLKEN_CLR_EPWM2_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM2 Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_CLR_EPWM1_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM1 Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_CLR_EPWM0_TB_CLKEN	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.91 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register (Offset = 4140h) [reset = 0h]

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Table 14-4740. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 4140h

Figure 14-1575. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					EPWM0_CTRL_SYNCIN_SEL		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED			EPWM0_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4742. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM0_CTRL_SYNCIN_SEL	R/W	0h	Selects the source of the EPWM0 synchronization input Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM0_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.92 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register (Offset = 4144h) [reset = 0h]

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Table 14-4743. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4144h**

Figure 14-1576. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM1_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4745. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM1_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.93 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register (Offset = 4148h) [reset = 0h]

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Table 14-4746. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4148h**

Figure 14-1577. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED			EPWM2_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4748. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM2_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.94 MAIN_CTRL_MMR_CFG0_EPWM3_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM3_CTRL Register (Offset = 414Ch) [reset = 0h]

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Table 14-4749. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 414Ch**

Figure 14-1578. MAIN_CTRL_MMR_CFG0_EPWM3_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					EPWM3_CTRL_SYNCIN_SEL		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED			EPWM3_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4751. MAIN_CTRL_MMR_CFG0_EPWM3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM3_CTRL_SYNCIN_SEL	R/W	0h	Selects the source of the EPWM3 synchronization input Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM3_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.95 MAIN_CTRL_MMR_CFG0_EPWM4_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM4_CTRL Register (Offset = 4150h) [reset = 0h]

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Table 14-4752. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4150h**

Figure 14-1579. MAIN_CTRL_MMR_CFG0_EPWM4_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM4_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4754. MAIN_CTRL_MMR_CFG0_EPWM4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM4_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.96 MAIN_CTRL_MMR_CFG0_EPWM5_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM5_CTRL Register (Offset = 4154h) [reset = 0h]

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Table 14-4755. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 4154h

Figure 14-1580. MAIN_CTRL_MMR_CFG0_EPWM5_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM5_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4757. MAIN_CTRL_MMR_CFG0_EPWM5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM5_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.97 MAIN_CTRL_MMR_CFG0_EPWM6_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM6_CTRL Register (Offset = 4158h) [reset = 0h]

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Table 14-4758. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4158h**

Figure 14-1581. MAIN_CTRL_MMR_CFG0_EPWM6_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					EPWM6_CTRL_SYNCIN_SEL		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED			EPWM6_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4760. MAIN_CTRL_MMR_CFG0_EPWM6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM6_CTRL_SYNCIN_SEL	R/W	0h	Selects the source of the EPWM6 synchronization input Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM6_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.98 MAIN_CTRL_MMR_CFG0_EPWM7_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM7_CTRL Register (Offset = 415Ch) [reset = 0h]

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Table 14-4761. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 415Ch

Figure 14-1582. MAIN_CTRL_MMR_CFG0_EPWM7_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM7_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4763. MAIN_CTRL_MMR_CFG0_EPWM7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM7_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.99 MAIN_CTRL_MMR_CFG0_EPWM8_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EPWM8_CTRL Register (Offset = 4160h) [reset = 0h]

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Table 14-4764. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 4160h

Figure 14-1583. MAIN_CTRL_MMR_CFG0_EPWM8_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>EPWM8_CTRL_EALLOW</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4766. MAIN_CTRL_MMR_CFG0_EPWM8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM8_CTRL_EALLOW	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.100 MAIN_CTRL_MMR_CFG0_SOCA_SEL Register

1 MAIN_CTRL_MMR_CFG0_SOCA_SEL Register (Offset = 4170h) [reset = 0h]

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Table 14-4767. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 4170h

Figure 14-1584. MAIN_CTRL_MMR_CFG0_SOCA_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOCA_SEL_SOCA_SEL	
NONE						R/W	
0h						0h	

Table 14-4769. MAIN_CTRL_MMR_CFG0_SOCA_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SOCA_SEL_SOCA_SEL	R/W	0h	Selects the SOC A output source Reset Source: mod_g_rst_n

14.2.1.1.1.2.101 MAIN_CTRL_MMR_CFG0_SOCB_SEL Register

1 MAIN_CTRL_MMR_CFG0_SOCB_SEL Register (Offset = 4174h) [reset = 0h]

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Table 14-4770. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4174h**

Figure 14-1585. MAIN_CTRL_MMR_CFG0_SOCB_SEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">SOCB_SEL_SOCB_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-4772. MAIN_CTRL_MMR_CFG0_SOCB_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SOCB_SEL_SOCB_SEL	R/W	0h	Selects the SOC B output source Reset Source: mod_g_rst_n

14.2.1.1.1.2.102 MAIN_CTRL_MMR_CFG0_EQEP0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EQEP0_CTRL Register (Offset = 4180h) [reset = 0h]

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Table 14-4773. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4180h**

Figure 14-1586. MAIN_CTRL_MMR_CFG0_EQEP0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EQEP0_CTRL_SOCA_SEL				
NONE			R/W				
0h			0h				

Table 14-4775. MAIN_CTRL_MMR_CFG0_EQEP0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP0_CTRL_SOCA_SEL	R/W	0h	Selects the source of SOCA input for EQEP0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.103 MAIN_CTRL_MMR_CFG0_EQEP1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EQEP1_CTRL Register (Offset = 4184h) [reset = 0h]

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Table 14-4776. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4184h**

Figure 14-1587. MAIN_CTRL_MMR_CFG0_EQEP1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EQEP1_CTRL_SOCA_SEL				
NONE			R/W				
0h			0h				

Table 14-4778. MAIN_CTRL_MMR_CFG0_EQEP1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP1_CTRL_SOCA_SEL	R/W	0h	Selects the source of SOCA input for EQEP1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.104 MAIN_CTRL_MMR_CFG0_EQEP2_CTRL Register

1 MAIN_CTRL_MMR_CFG0_EQEP2_CTRL Register (Offset = 4188h) [reset = 0h]

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Table 14-4779. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4188h**

Figure 14-1588. MAIN_CTRL_MMR_CFG0_EQEP2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EQEP2_CTRL_SOCA_SEL				
NONE			R/W				
0h			0h				

Table 14-4781. MAIN_CTRL_MMR_CFG0_EQEP2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP2_CTRL_SOCA_SEL	R/W	0h	Selects the source of SOCA input for EQEP2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.105 MAIN_CTRL_MMR_CFG0_EQEP_STAT Register

1 MAIN_CTRL_MMR_CFG0_EQEP_STAT Register (Offset = 41A0h) [reset = 0h]

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Table 14-4782. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 41A0h**

Figure 14-1589. MAIN_CTRL_MMR_CFG0_EQEP_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EQEP_STAT_PHASE_ERR2	EQEP_STAT_PHASE_ERR1	EQEP_STAT_PHASE_ERR0
NONE					R	R	R
0h					X	X	X

Table 14-4784. MAIN_CTRL_MMR_CFG0_EQEP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	EQEP_STAT_PHASE_ERR2	R	X	EQEP2 Phase error status Reset Source: mod_g_rst_n
1	EQEP_STAT_PHASE_ERR1	R	X	EQEP1 Phase error status Reset Source: mod_g_rst_n
0	EQEP_STAT_PHASE_ERR0	R	X	EQEP0 Phase error status Reset Source: mod_g_rst_n

14.2.1.1.1.2.106 MAIN_CTRL_MMR_CFG0_SDIO1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_SDIO1_CTRL Register (Offset = 41B4h) [reset = 0h]

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Table 14-4785. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 41B4h**

Figure 14-1590. MAIN_CTRL_MMR_CFG0_SDIO1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO1_CTRL_DRV_STR				
NONE			R/W				
0h			X				

Table 14-4787. MAIN_CTRL_MMR_CFG0_SDIO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO1_CTRL_DRV_STR	R/W	X	Selects the SDIO drive strength Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.1.2.107 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register (Offset = 4204h) [reset = 0h]

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Table 14-4788. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4204h**

Figure 14-1591. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER1_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4790. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER1_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER1 to TIMER0 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.108 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register (Offset = 420Ch) [reset = 0h]

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Table 14-4791. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 420Ch**

Figure 14-1592. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							TIMER3_CTRL_CASCADE_EN
NONE							R/W
0h							0h

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4793. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER3_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER3 to TIMER2 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.109 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register (Offset = 4214h) [reset = 0h]

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Table 14-4794. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4214h**

Figure 14-1593. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER5_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4796. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER5_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER5 to TIMER4 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.110 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register (Offset = 421Ch) [reset = 0h]

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Table 14-4797. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 421Ch**

Figure 14-1594. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>TIMER7_CTRL_CASCADE_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4799. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER7_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER7 to TIMER6 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.111 MAIN_CTRL_MMR_CFG0_TIMER9_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER9_CTRL Register (Offset = 4224h) [reset = 0h]

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Table 14-4800. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4224h**

Figure 14-1595. MAIN_CTRL_MMR_CFG0_TIMER9_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER9_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4802. MAIN_CTRL_MMR_CFG0_TIMER9_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER9_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER9 to TIMER8 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.112 MAIN_CTRL_MMR_CFG0_TIMER11_CTRL Register

1 MAIN_CTRL_MMR_CFG0_TIMER11_CTRL Register (Offset = 422Ch) [reset = 0h]

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Table 14-4803. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 422Ch

Figure 14-1596. MAIN_CTRL_MMR_CFG0_TIMER11_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER11_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4805. MAIN_CTRL_MMR_CFG0_TIMER11_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER11_CTRL_CASCADE_EN	R/W	0h	Activates cascading of TIMER11 to TIMER10 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.113 MAIN_CTRL_MMR_CFG0_I2C0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_I2C0_CTRL Register (Offset = 42E0h) [reset = 0h]

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Table 14-4806. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 42E0h

Figure 14-1597. MAIN_CTRL_MMR_CFG0_I2C0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							I2C0_CTRL_HS_MCS_EN
NONE							R/W
0h							0h

Table 14-4808. MAIN_CTRL_MMR_CFG0_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	I2C0_CTRL_HS_MCS_EN	R/W	0h	HS Mode controller current source activate. Reset Source: mod_g_rst_n

14.2.1.1.1.2.114 MAIN_CTRL_MMR_CFG0_FSS_CTRL Register

1 MAIN_CTRL_MMR_CFG0_FSS_CTRL Register (Offset = 4700h) [reset = 0h]

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Table 14-4809. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4700h**

Figure 14-1598. MAIN_CTRL_MMR_CFG0_FSS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>FSS_CTRL_S0_BOOT_SIZE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">FSS_CTRL_S0_BOOT_SEG</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-4811. MAIN_CTRL_MMR_CFG0_FSS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	FSS_CTRL_S0_BOOT_SIZE	R/W	0h	Selects the size of the boot block to be used for the S0 (OSPI0) flash interface Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	FSS_CTRL_S0_BOOT_SEG	R/W	0h	Selects the boot block to be used for the S0 (OSPI0) flash interface. If the s0_boot_size is 128 MB then only bits [4:0] of this field are used. Care must be taken to account for the address translation as to not fall off or wrap the address of the flash. (e.g. if both ECC and authentication are activated for 64 MB boot, the highest valid block number is is 49, as sector 50 is only .2M Bytes in size.) Reset Source: mod_g_rst_n

14.2.1.1.1.2.115 MAIN_CTRL_MMR_CFG0_ADC0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_ADC0_CTRL Register (Offset = 4710h) [reset = 0h]

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Table 14-4812. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4710h**

Figure 14-1599. MAIN_CTRL_MMR_CFG0_ADC0_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>ADC0_CTRL_GPI_MODE_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ADC0_CTRL_TRIG_SEL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-4814. MAIN_CTRL_MMR_CFG0_ADC0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ADC0_CTRL_GPI_MODE_EN	R/W	0h	Activates ADC0 data pins to be used as general purpose inputs when set. This signal is tied to the en_dig_test input of MCU_ADC0 Reset Source: mod_g_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	ADC0_CTRL_TRIG_SEL	R/W	0h	Selects the source of the ADC hardware event trigger Reset Source: mod_g_rst_n

14.2.1.1.1.2.116 MAIN_CTRL_MMR_CFG0_DCC_STAT Register

1 MAIN_CTRL_MMR_CFG0_DCC_STAT Register (Offset = 4750h) [reset = 0h]

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Table 14-4815. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 4750h**

Figure 14-1600. MAIN_CTRL_MMR_CFG0_DCC_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>DCC_STAT_MCU_DCC0_INTR_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>DCC_STAT_DCC5_INTR_DONE</td><td>DCC_STAT_DCC4_INTR_DONE</td><td>DCC_STAT_DCC3_INTR_DONE</td><td>DCC_STAT_DCC2_INTR_DONE</td><td>DCC_STAT_DCC1_INTR_DONE</td><td>DCC_STAT_DCC0_INTR_DONE</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
</table>

Table 14-4817. MAIN_CTRL_MMR_CFG0_DCC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	DCC_STAT_MCU_DCC0_INTR_DONE	R	X	MCU_DCC0 Done Interrupt Status Reset Source: mod_g_rst_n
15:6	RESERVED	NONE	0h	Reserved
5	DCC_STAT_DCC5_INTR_DONE	R	X	DCC5 Done Interrupt Status Reset Source: mod_g_rst_n
4	DCC_STAT_DCC4_INTR_DONE	R	X	DCC4 Done Interrupt Status Reset Source: mod_g_rst_n
3	DCC_STAT_DCC3_INTR_DONE	R	X	DCC3 Done Interrupt Status Reset Source: mod_g_rst_n
2	DCC_STAT_DCC2_INTR_DONE	R	X	DCC2 Done Interrupt Status Reset Source: mod_g_rst_n
1	DCC_STAT_DCC1_INTR_DONE	R	X	DCC1 Done Interrupt Status Reset Source: mod_g_rst_n

Table 14-4817. MAIN_CTRL_MMR_CFG0_DCC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DCC_STAT_DCC0_INTR_DONE	R	X	DCC0 Done Interrupt Status Reset Source: mod_g_rst_n

14.2.1.1.1.2.117 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-4818. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5008h**

Figure 14-1601. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-4820. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.118 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-4821. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 500Ch**

Figure 14-1602. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-4823. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.119 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4824. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5100h**

Figure 14-1603. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-4826. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.120 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4827. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5104h**

Figure 14-1604. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-4829. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.121 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4830. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5108h**

Figure 14-1605. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-4832. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.122 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-4833. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 510Ch**

Figure 14-1606. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-4835. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.123 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4836. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5110h**

Figure 14-1607. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-4838. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.124 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register (Offset = 5114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4839. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5114h**

Figure 14-1608. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5_READONLY							
R							
0h							

Table 14-4841. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.125 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register (Offset = 5118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4842. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5118h**

Figure 14-1609. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6_READONLY							
R							
0h							

Table 14-4844. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.126 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register (Offset = 511Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-4845. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 511Ch**

Figure 14-1610. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7_READONLY							
R							
0h							

Table 14-4847. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.127 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register (Offset = 5120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4848. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5120h**

Figure 14-1611. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8_READONLY							
R							
0h							

Table 14-4850. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.128 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register (Offset = 5124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4851. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5124h**

Figure 14-1612. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9_READONLY							
R							
0h							

Table 14-4853. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.129 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register (Offset = 5128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4854. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5128h**

Figure 14-1613. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P1_R10_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P1_R10_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P1_R10_READONLY							
R							
0h							

Table 14-4856. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.130 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register (Offset = 512Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-4857. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 512Ch**

Figure 14-1614. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11_READONLY							
R							
0h							

Table 14-4859. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.131 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register (Offset = 5130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4860. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5130h**

Figure 14-1615. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P1_R12_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P1_R12_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P1_R12_READONLY							
R							
0h							

Table 14-4862. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.132 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY Register (Offset = 5134h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4863. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 5134h

Figure 14-1616. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R13_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R13_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R13_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R13_READONLY							
R							
0h							

Table 14-4865. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R13_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.133 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY Register (Offset = 5138h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4866. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 5138h**

Figure 14-1617. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R14_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R14_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R14_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R14_READONLY							
R							
0h							

Table 14-4868. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R14_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.134 MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register (Offset = 6008h) [reset = 80000004h]

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Table 14-4869. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6008h

Figure 14-1618. MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RSVD	RESERVED						
	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED						USB0_PHY_CTRL_LOOPBACK_MODE_PROXY	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
USB0_PHY_CTRL_PLL_STANDALONE_PROXY	RESERVED			USB0_PHY_CTRL_PLL_CLKOUT_ON_PROXY	RESERVED	USB0_PHY_CTRL_PLL_CLKOUT_SEL_PROXY	
R/W	NONE			R/W	NONE	R/W	
0h	0h			0h	0h	0h	
7	6	5	4	3	2	1	0
RESERVED				USB0_PHY_CTRL_PLL_REF_SEL_PROXY			
NONE				R/W			
0h				4h			

Table 14-4871. MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
30:18	RESERVED	NONE	0h	Reserved
17:16	USB0_PHY_CTRL_LOOPBACK_MODE_PROXY	R/W	0h	Activates USB0 PHY loopback operation Reset Source: mod_g_rst_n
15	USB0_PHY_CTRL_PLL_STANDALONE_PROXY	R/W	0h	Activates USB0 PHY as a standalone PLL Reset Source: mod_g_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	USB0_PHY_CTRL_PLL_CLKOUT_ON_PROXY	R/W	0h	Controls USB0 PLL clock output Reset Source: mod_g_rst_n
10	RESERVED	NONE	0h	Reserved
9:8	USB0_PHY_CTRL_PLL_CLKOUT_SEL_PROXY	R/W	0h	Selects the frequency of the USB0 PLL output clock Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4871. MAIN_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	USB0_PHY_CTRL_PLL_REF_SEL_PROXY	R/W	4h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should match the frequency value of either the HFOSC0 or HFOSC1 oscillator as selected by the USB0_CLKSEL register Reset Source: mod_g_rst_n

14.2.1.1.1.2.135 MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register (Offset = 6044h) [reset = 2h]

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Table 14-4872. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6044h

Figure 14-1619. MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	ENET1_CTRL_PORT_MODE_SEL_PROXY		
NONE			NONE	NONE	R/W		
0h			0h	0h	2h		

Table 14-4874. MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET1_CTRL_PORT_MODE_SEL_PROXY	R/W	2h	Selects Ethernet switch Port1 interface Reset Source: sys_por_rst_n

14.2.1.1.1.2.136 MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register (Offset = 6048h) [reset = 2h]

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Table 14-4875. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6048h**

Figure 14-1620. MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	ENET2_CTRL_PORT_MODE_SEL_PROXY		
NONE			NONE	NONE	R/W		
0h			0h	0h	2h		

Table 14-4877. MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET2_CTRL_PORT_MODE_SEL_PROXY	R/W	2h	Selects Ethernet switch Port2 interface Reset Source: sys_por_rst_n

14.2.1.1.1.2.137 MAIN_CTRL_MMR_CFG0_PCIE0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_PCIE0_CTRL_PROXY Register (Offset = 6070h) [reset = 1h]

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Table 14-4878. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6070h**

Figure 14-1621. MAIN_CTRL_MMR_CFG0_PCIE0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PCIE0_CTRL_MODE_SEL_PROXY	RESERVED					PCIE0_CTRL_GENERATION_SEL_PROXY	
R/W	NONE					R/W	
0h	0h					1h	

Table 14-4880. MAIN_CTRL_MMR_CFG0_PCIE0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PCIE0_CTRL_MODE_SEL_PROXY	R/W	0h	Selects the operating mode Reset Source: mod_g_rst_n
6:2	RESERVED	NONE	0h	Reserved
1:0	PCIE0_CTRL_GENERATION_SEL_PROXY	R/W	1h	Configures the PCIe generation support in the PCIe capabilities linked-list Reset Source: mod_g_rst_n

14.2.1.1.1.2.138 MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL_PROXY Register (Offset = 6080h) [reset = 0h]

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Table 14-4881. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6080h

Figure 14-1622. MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						SERDES0_LN0_CTRL_LANE_FUNC_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4883. MAIN_CTRL_MMR_CFG0_SERDES0_LN0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SERDES0_LN0_CTRL_LANE_FUNC_SEL_PROXY	R/W	0h	Selects the SERDES0 lane0 function Reset Source: sys_por_rst_n

14.2.1.1.1.2.139 MAIN_CTRL_MMR_CFG0_ADC0_TRIM_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ADC0_TRIM_PROXY Register (Offset = 60C0h) [reset = 0h]

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Table 14-4884. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 60C0h**

Figure 14-1623. MAIN_CTRL_MMR_CFG0_ADC0_TRIM_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">ADC0_TRIM_TRIM5_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ADC0_TRIM_TRIM4_PROXY</td><td colspan="3">ADC0_TRIM_TRIM3_PROXY</td><td colspan="2">ADC0_TRIM_TRIM2_PROXY</td></tr>
<tr><td colspan="3">R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">X</td><td colspan="3">X</td><td colspan="2">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">ADC0_TRIM_TRIM2_PROXY</td><td colspan="4">ADC0_TRIM_TRIM1_PROXY</td><td colspan="2">ADC0_TRIM_ENABLE_CALB_PROXY</td></tr>
<tr><td colspan="2">R/W</td><td colspan="4">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">X</td><td colspan="4">X</td><td colspan="2">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">ADC0_TRIM_ENABLE_CALB_PROXY</td><td colspan="5">ADC0_TRIM_ENABLE_CAL_PROXY</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">X</td><td colspan="5">X</td></tr>
</table>

Table 14-4886. MAIN_CTRL_MMR_CFG0_ADC0_TRIM_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	ADC0_TRIM_TRIM5_PROXY	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
23:21	ADC0_TRIM_TRIM4_PROXY	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
20:18	ADC0_TRIM_TRIM3_PROXY	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
17:14	ADC0_TRIM_TRIM2_PROXY	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
13:10	ADC0_TRIM_TRIM1_PROXY	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
9:5	ADC0_TRIM_ENABLE_CALB_PROXY	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n
4:0	ADC0_TRIM_ENABLE_CAL_PROXY	R/W	X	Trims Nonlinearities from ADC Reset Source: mod_por_rst_n

14.2.1.1.1.2.140 MAIN_CTRL_MMR_CFG0_SERDES0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SERDES0_CTRL_PROXY Register (Offset = 60E0h) [reset = 0h]

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Table 14-4887. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 60E0h

Figure 14-1624. MAIN_CTRL_MMR_CFG0_SERDES0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			SERDES0_CTRL_REF_SEL_PROXY	RESERVED			SERDES0_CTRL_RET_EN_PROXY
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-4889. MAIN_CTRL_MMR_CFG0_SERDES0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	SERDES0_CTRL_REF_SEL_PROXY	R/W	0h	REFCLK output select Reset Source: sys_por_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	SERDES0_CTRL_RET_EN_PROXY	R/W	0h	Retention activate Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.141 MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0_PROXY Register (Offset = 6100h) [reset = 0h]

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Table 14-4890. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6100h**

Figure 14-1625. MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							ICSSG0_CTRL0_RGMII0_ID_MODE_PROXY
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				ICSSG0_CTRL0_GPM_BIDI_PROXY			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ICSSG0_CTRL0_GPM_BIDI_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
ICSSG0_CTRL0_GPM_BIDI_PROXY							
R/W							
0h							

Table 14-4892. MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ICSSG0_CTRL0_RGMII0_ID_MODE_PROXY	R/W	0h	Controls the ICSS_G0 RGMII0 port internal transmit delay Reset Source: sys_por_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	ICSSG0_CTRL0_GPM_BIDI_PROXY	R/W	0h	Controls operation of the ICSS_G0 PRU0_GPO pins. Each bit n controls the corresponding PRG0_PRU0GPOn I/O Reset Source: sys_por_rst_n

14.2.1.1.1.2.142 MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1_PROXY Register (Offset = 6104h) [reset = 0h]

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Table 14-4893. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6104h**

Figure 14-1626. MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							ICSSG0_CTRL1_RGMII1_ID_MODE_PROXY
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				ICSSG0_CTRL1_GPM_BIDI_PROXY			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ICSSG0_CTRL1_GPM_BIDI_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
ICSSG0_CTRL1_GPM_BIDI_PROXY							
R/W							
0h							

Table 14-4895. MAIN_CTRL_MMR_CFG0_ICSSG0_CTRL1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ICSSG0_CTRL1_RGMII1_ID_MODE_PROXY	R/W	0h	Controls the ICSS_G0 RGMII1 port internal transmit delay Reset Source: sys_por_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	ICSSG0_CTRL1_GPM_BIDI_PROXY	R/W	0h	Controls operation of the ICSS_G0 PRU1_GPO pins. Each bit n controls the corresponding PRG0_PRU1GPOn I/O Reset Source: sys_por_rst_n

14.2.1.1.1.2.143 MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0_PROXY Register (Offset = 6110h) [reset = 0h]

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Table 14-4896. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6110h**

Figure 14-1627. MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							ICSSG1_CTRL0_RGMII0_ID_MODE_PROXY
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				ICSSG1_CTRL0_GPM_BIDI_PROXY			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ICSSG1_CTRL0_GPM_BIDI_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
ICSSG1_CTRL0_GPM_BIDI_PROXY							
R/W							
0h							

Table 14-4898. MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ICSSG1_CTRL0_RGMII0_ID_MODE_PROXY	R/W	0h	Controls the ICSS_G1 RGMII0 port internal transmit delay Reset Source: sys_por_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	ICSSG1_CTRL0_GPM_BIDI_PROXY	R/W	0h	Controls operation of the ICSS_G1 PRU0_GPO pins. Each bit n controls the corresponding PRG1_PRU0GPOn I/O Reset Source: sys_por_rst_n

14.2.1.1.1.2.144 MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1_PROXY Register (Offset = 6114h) [reset = 0h]

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Table 14-4899. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6114h**

Figure 14-1628. MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							ICSSG1_CTRL1_RGMII1_ID_MODE_PROXY
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				ICSSG1_CTRL1_GPM_BIDI_PROXY			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ICSSG1_CTRL1_GPM_BIDI_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
ICSSG1_CTRL1_GPM_BIDI_PROXY							
R/W							
0h							

Table 14-4901. MAIN_CTRL_MMR_CFG0_ICSSG1_CTRL1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ICSSG1_CTRL1_RGMII1_ID_MODE_PROXY	R/W	0h	Controls the ICSS_G1 RGMII1 port internal transmit delay Reset Source: sys_por_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	ICSSG1_CTRL1_GPM_BIDI_PROXY	R/W	0h	Controls operation of the ICSS_G1 PRU1_GPO pins. Each bit n controls the corresponding PRG1_PRU1GPOn I/O Reset Source: sys_por_rst_n

14.2.1.1.1.2.145 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register (Offset = 6130h) [reset = 0h]

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Table 14-4902. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6130h**

Figure 14-1629. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							EPWM_TB_CLKEN_EPWM8_TB_CLKEN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
EPWM_TB_CLKEN_EPWM7_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM6_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM5_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM4_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM3_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM2_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM1_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM0_TB_CLKEN_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4904. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	EPWM_TB_CLKEN_EPWM8_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM8 When Set Reset Source: mod_g_rst_n
7	EPWM_TB_CLKEN_EPWM7_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM7 When Set Reset Source: mod_g_rst_n
6	EPWM_TB_CLKEN_EPWM6_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM6 When Set Reset Source: mod_g_rst_n
5	EPWM_TB_CLKEN_EPWM5_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM5 When Set Reset Source: mod_g_rst_n
4	EPWM_TB_CLKEN_EPWM4_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM4 When Set Reset Source: mod_g_rst_n
3	EPWM_TB_CLKEN_EPWM3_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM3 When Set Reset Source: mod_g_rst_n

Table 14-4904. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EPWM_TB_CLKEN_EPWM2_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM2 When Set Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_EPWM1_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM1 When Set Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_EPWM0_TB_CLKEN_PROXY	R/W	0h	Activates Timebase Clock of EPWM0 When Set Reset Source: mod_g_rst_n

14.2.1.1.1.2.146 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET_PROXY Register (Offset = 6134h) [reset = 0h]

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Table 14-4905. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6134h

Figure 14-1630. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							EPWM_TB_CLKEN_SET_EPWM8_TB_CLKEN_PROXY
NONE							R/W1TS
0h							0h
7	6	5	4	3	2	1	0
EPWM_TB_CLKEN_SET_EPWM7_TB_CLKEN_PROXY	EPWM_TB_CLKEN_SET_EPWM6_TB_CLKEN_PROXY	EPWM_TB_CLKEN_SET_EPWM5_TB_CLKEN_PROXY	EPWM_TB_CLKEN_SET_EPWM4_TB_CLKEN_PROXY	EPWM_TB_CLKEN_SET_EPWM3_TB_CLKEN_PROXY	EPWM_TB_CLKEN_SET_EPWM2_TB_CLKEN_PROXY	EPWM_TB_CLKEN_SET_EPWM1_TB_CLKEN_PROXY	EPWM_TB_CLKEN_SET_EPWM0_TB_CLKEN_PROXY
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4907. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	EPWM_TB_CLKEN_SET_EPWM8_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM8 Reset Source: mod_g_rst_n
7	EPWM_TB_CLKEN_SET_EPWM7_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM7 Reset Source: mod_g_rst_n
6	EPWM_TB_CLKEN_SET_EPWM6_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM6 Reset Source: mod_g_rst_n
5	EPWM_TB_CLKEN_SET_EPWM5_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM5 Reset Source: mod_g_rst_n
4	EPWM_TB_CLKEN_SET_EPWM4_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM4 Reset Source: mod_g_rst_n

Table 14-4907. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_SET_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EPWM_TB_CLKEN_SET_EPWM3_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM3 Reset Source: mod_g_rst_n
2	EPWM_TB_CLKEN_SET_EPWM2_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM2 Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_SET_EPWM1_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM1 Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_SET_EPWM0_TB_CLKEN_PROXY	R/W1TS	0h	Writing One Activates Timebase Clock of EPWM0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.147 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR_PROXY Register (Offset = 6138h) [reset = 0h]

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Table 14-4908. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6138h**

Figure 14-1631. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							EPWM_TB_CLKEN_CLR_EPWM8_TB_CLKEN_PROXY
NONE							R/W1TC
0h							0h
7	6	5	4	3	2	1	0
EPWM_TB_CLKEN_CLR_EPWM7_TB_CLKEN_PROXY	EPWM_TB_CLKEN_CLR_EPWM6_TB_CLKEN_PROXY	EPWM_TB_CLKEN_CLR_EPWM5_TB_CLKEN_PROXY	EPWM_TB_CLKEN_CLR_EPWM4_TB_CLKEN_PROXY	EPWM_TB_CLKEN_CLR_EPWM3_TB_CLKEN_PROXY	EPWM_TB_CLKEN_CLR_EPWM2_TB_CLKEN_PROXY	EPWM_TB_CLKEN_CLR_EPWM1_TB_CLKEN_PROXY	EPWM_TB_CLKEN_CLR_EPWM0_TB_CLKEN_PROXY
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4910. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	EPWM_TB_CLKEN_CLR_EPWM8_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM8 Reset Source: mod_g_rst_n
7	EPWM_TB_CLKEN_CLR_EPWM7_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM7 Reset Source: mod_g_rst_n
6	EPWM_TB_CLKEN_CLR_EPWM6_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM6 Reset Source: mod_g_rst_n
5	EPWM_TB_CLKEN_CLR_EPWM5_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM5 Reset Source: mod_g_rst_n
4	EPWM_TB_CLKEN_CLR_EPWM4_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM4 Reset Source: mod_g_rst_n

Table 14-4910. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_CLR_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EPWM_TB_CLKEN_CLR_EPWM3_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM3 Reset Source: mod_g_rst_n
2	EPWM_TB_CLKEN_CLR_EPWM2_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM2 Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_CLR_EPWM1_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM1 Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_CLR_EPWM0_TB_CLKEN_PROXY	R/W1TC	0h	Writing One Deactivates Timebase Clock of EPWM0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.148 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register (Offset = 6140h) [reset = 0h]

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Table 14-4911. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6140h

Figure 14-1632. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">EPWM0_CTRL_SYNCIN_SEL_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>EPWM0_CTRL_EALLOW_PROXY</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4913. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM0_CTRL_SYNCIN_SEL_PROXY	R/W	0h	Selects the source of the EPWM0 synchronization input Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM0_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.149 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register (Offset = 6144h) [reset = 0h]

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Table 14-4914. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6144h**

Figure 14-1633. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM1_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4916. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM1_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.150 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register (Offset = 6148h) [reset = 0h]

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Table 14-4917. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6148h**

Figure 14-1634. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM2_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4919. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM2_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.151 MAIN_CTRL_MMR_CFG0_EPWM3_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM3_CTRL_PROXY Register (Offset = 614Ch) [reset = 0h]

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Table 14-4920. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 614Ch

Figure 14-1635. MAIN_CTRL_MMR_CFG0_EPWM3_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					EPWM3_CTRL_SYNCIN_SEL_PROXY		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED			EPWM3_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4922. MAIN_CTRL_MMR_CFG0_EPWM3_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM3_CTRL_SYNCIN_SEL_PROXY	R/W	0h	Selects the source of the EPWM3 synchronization input Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM3_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.152 MAIN_CTRL_MMR_CFG0_EPWM4_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM4_CTRL_PROXY Register (Offset = 6150h) [reset = 0h]

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Table 14-4923. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6150h**

Figure 14-1636. MAIN_CTRL_MMR_CFG0_EPWM4_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>EPWM4_CTRL_EALLOW_PROXY</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4925. MAIN_CTRL_MMR_CFG0_EPWM4_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM4_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.153 MAIN_CTRL_MMR_CFG0_EPWM5_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM5_CTRL_PROXY Register (Offset = 6154h) [reset = 0h]

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Table 14-4926. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6154h**

Figure 14-1637. MAIN_CTRL_MMR_CFG0_EPWM5_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM5_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4928. MAIN_CTRL_MMR_CFG0_EPWM5_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM5_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.154 MAIN_CTRL_MMR_CFG0_EPWM6_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM6_CTRL_PROXY Register (Offset = 6158h) [reset = 0h]

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Table 14-4929. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6158h

Figure 14-1638. MAIN_CTRL_MMR_CFG0_EPWM6_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					EPWM6_CTRL_SYNCIN_SEL_PROXY		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED			EPWM6_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4931. MAIN_CTRL_MMR_CFG0_EPWM6_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM6_CTRL_SYNCIN_SEL_PROXY	R/W	0h	Selects the source of the EPWM6 synchronization input Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM6_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.155 MAIN_CTRL_MMR_CFG0_EPWM7_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM7_CTRL_PROXY Register (Offset = 615Ch) [reset = 0h]

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Table 14-4932. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 615Ch

Figure 14-1639. MAIN_CTRL_MMR_CFG0_EPWM7_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM7_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4934. MAIN_CTRL_MMR_CFG0_EPWM7_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM7_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.156 MAIN_CTRL_MMR_CFG0_EPWM8_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EPWM8_CTRL_PROXY Register (Offset = 6160h) [reset = 0h]

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Table 14-4935. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6160h**

Figure 14-1640. MAIN_CTRL_MMR_CFG0_EPWM8_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM8_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4937. MAIN_CTRL_MMR_CFG0_EPWM8_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM8_CTRL_EALLOW_PROXY	R/W	0h	Activate write access to EPWM tripzone registers Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.157 MAIN_CTRL_MMR_CFG0_SOCA_SEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SOCA_SEL_PROXY Register (Offset = 6170h) [reset = 0h]

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Table 14-4938. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6170h

Figure 14-1641. MAIN_CTRL_MMR_CFG0_SOCA_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						SOCA_SEL_SOCA_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4940. MAIN_CTRL_MMR_CFG0_SOCA_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SOCA_SEL_SOCA_SEL_PROXY	R/W	0h	Selects the SOC A output source Reset Source: mod_g_rst_n

14.2.1.1.1.2.158 MAIN_CTRL_MMR_CFG0_SOCB_SEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SOCB_SEL_PROXY Register (Offset = 6174h) [reset = 0h]

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Table 14-4941. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6174h**

Figure 14-1642. MAIN_CTRL_MMR_CFG0_SOCB_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOCB_SEL_SOCB_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4943. MAIN_CTRL_MMR_CFG0_SOCB_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SOCB_SEL_SOCB_SEL_PROXY	R/W	0h	Selects the SOC B output source Reset Source: mod_g_rst_n

14.2.1.1.1.2.159 MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY Register (Offset = 6180h) [reset = 0h]

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Table 14-4944. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6180h**

Figure 14-1643. MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EQEP0_CTRL_SOCA_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4946. MAIN_CTRL_MMR_CFG0_EQEP0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP0_CTRL_SOCA_SEL_PROXY	R/W	0h	Selects the source of SOCA input for EQEP0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.160 MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY Register (Offset = 6184h) [reset = 0h]

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Table 14-4947. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6184h**

Figure 14-1644. MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			EQEP1_CTRL_SOCA_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4949. MAIN_CTRL_MMR_CFG0_EQEP1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP1_CTRL_SOCA_SEL_PROXY	R/W	0h	Selects the source of SOCA input for EQEP1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.161 MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY Register (Offset = 6188h) [reset = 0h]

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Table 14-4950. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6188h**

Figure 14-1645. MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EQEP2_CTRL_SOCA_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4952. MAIN_CTRL_MMR_CFG0_EQEP2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EQEP2_CTRL_SOCA_SEL_PROXY	R/W	0h	Selects the source of SOCA input for EQEP2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.162 MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY Register (Offset = 61A0h) [reset = 0h]

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Table 14-4953. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 61A0h**

Figure 14-1646. MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>EQEP_STAT_PHASE_ERR2_PROXY</td><td>EQEP_STAT_PHASE_ERR1_PROXY</td><td>EQEP_STAT_PHASE_ERR0_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>X</td><td>X</td><td>X</td></tr>
</table>

Table 14-4955. MAIN_CTRL_MMR_CFG0_EQEP_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	EQEP_STAT_PHASE_ERR2_PROXY	R	X	EQEP2 Phase error status Reset Source: mod_g_rst_n
1	EQEP_STAT_PHASE_ERR1_PROXY	R	X	EQEP1 Phase error status Reset Source: mod_g_rst_n
0	EQEP_STAT_PHASE_ERR0_PROXY	R	X	EQEP0 Phase error status Reset Source: mod_g_rst_n

14.2.1.1.1.2.163 MAIN_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY Register (Offset = 61B4h) [reset = 0h]

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Table 14-4956. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 61B4h

Figure 14-1647. MAIN_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO1_CTRL_DRV_STR_PROXY				
NONE			R/W				
0h			X				

Table 14-4958. MAIN_CTRL_MMR_CFG0_SDIO1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO1_CTRL_DRV_STR_PROXY	R/W	X	Selects the SDIO drive strength Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.1.2.164 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register (Offset = 6204h) [reset = 0h]

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Table 14-4959. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6204h**

Figure 14-1648. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER1_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4961. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER1_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER1 to TIMER0 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.165 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register (Offset = 620Ch) [reset = 0h]

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Table 14-4962. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 620Ch**

Figure 14-1649. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER3_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4964. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER3_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER3 to TIMER2 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.166 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register (Offset = 6214h) [reset = 0h]

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Table 14-4965. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6214h

Figure 14-1650. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER5_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4967. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER5_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER5 to TIMER4 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.167 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register (Offset = 621Ch) [reset = 0h]

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Table 14-4968. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 621Ch**

Figure 14-1651. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER7_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4970. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER7_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER7 to TIMER6 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.168 MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY Register (Offset = 6224h) [reset = 0h]

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Table 14-4971. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6224h

Figure 14-1652. MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER9_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4973. MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER9_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER9 to TIMER8 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.169 MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY Register (Offset = 622Ch) [reset = 0h]

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Table 14-4974. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 622Ch

Figure 14-1653. MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER11_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4976. MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER11_CTRL_CASCADE_EN_PROXY	R/W	0h	Activates cascading of TIMER11 to TIMER10 Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.170 MAIN_CTRL_MMR_CFG0_I2C0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_I2C0_CTRL_PROXY Register (Offset = 62E0h) [reset = 0h]

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Table 14-4977. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 62E0h

Figure 14-1654. MAIN_CTRL_MMR_CFG0_I2C0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							I2C0_CTRL_HS_MCS_EN_PROXY
NONE							R/W
0h							0h

Table 14-4979. MAIN_CTRL_MMR_CFG0_I2C0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	I2C0_CTRL_HS_MCS_EN_PROXY	R/W	0h	HS Mode controller current source activate. Reset Source: mod_g_rst_n

14.2.1.1.1.2.171 MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY Register (Offset = 6700h) [reset = 0h]

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Table 14-4980. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6700h**

Figure 14-1655. MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>FSS_CTRL_S0_BOOT_SIZE_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">FSS_CTRL_S0_BOOT_SEG_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-4982. MAIN_CTRL_MMR_CFG0_FSS_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	FSS_CTRL_S0_BOOT_SIZE_PROXY	R/W	0h	Selects the size of the boot block to be used for the S0 (OSPI0) flash interface Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	FSS_CTRL_S0_BOOT_SEG_PROXY	R/W	0h	Selects the boot block to be used for the S0 (OSPI0) flash interface. If the s0_boot_size is 128 MB then only bits [4:0] of this field are used. Care must be taken to account for the address translation as to not fall off or wrap the address of the flash. (e.g. if both ECC and authentication are activated for 64 MB boot, the highest valid block number is is 49, as sector 50 is only .2M Bytes in size.) Reset Source: mod_g_rst_n

14.2.1.1.1.2.172 MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Register (Offset = 6710h) [reset = 0h]

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Table 14-4983. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 6710h**

Figure 14-1656. MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ADC0_CTRL_GPI_MODE_EN_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ADC0_CTRL_TRIG_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4985. MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ADC0_CTRL_GPI_MODE_EN_PROXY	R/W	0h	Activates ADC0 data pins to be used as general purpose inputs when set. This signal is tied to the en_dig_test input of MCU_ADC0 Reset Source: mod_g_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	ADC0_CTRL_TRIG_SEL_PROXY	R/W	0h	Selects the source of the ADC hardware event trigger Reset Source: mod_g_rst_n

14.2.1.1.1.2.173 MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register (Offset = 6750h) [reset = 0h]

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Table 14-4986. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 6750h

Figure 14-1657. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							DCC_STAT_MCU_DCC0_INTR_DONE_PROXY
NONE							R
0h							X
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DCC_STAT_DCC5_INTR_DONE_PROXY	DCC_STAT_DCC4_INTR_DONE_PROXY	DCC_STAT_DCC3_INTR_DONE_PROXY	DCC_STAT_DCC2_INTR_DONE_PROXY	DCC_STAT_DCC1_INTR_DONE_PROXY	DCC_STAT_DCC0_INTR_DONE_PROXY
NONE		R	R	R	R	R	R
0h		X	X	X	X	X	X

Table 14-4988. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	DCC_STAT_MCU_DCC0_INTR_DONE_PROXY	R	X	MCU_DCC0 Done Interrupt Status Reset Source: mod_g_rst_n
15:6	RESERVED	NONE	0h	Reserved
5	DCC_STAT_DCC5_INTR_DONE_PROXY	R	X	DCC5 Done Interrupt Status Reset Source: mod_g_rst_n
4	DCC_STAT_DCC4_INTR_DONE_PROXY	R	X	DCC4 Done Interrupt Status Reset Source: mod_g_rst_n
3	DCC_STAT_DCC3_INTR_DONE_PROXY	R	X	DCC3 Done Interrupt Status Reset Source: mod_g_rst_n
2	DCC_STAT_DCC2_INTR_DONE_PROXY	R	X	DCC2 Done Interrupt Status Reset Source: mod_g_rst_n
1	DCC_STAT_DCC1_INTR_DONE_PROXY	R	X	DCC1 Done Interrupt Status Reset Source: mod_g_rst_n

Table 14-4988. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DCC_STAT_DCC0_INTR_DONE_PROXY	R	X	DCC0 Done Interrupt Status Reset Source: mod_g_rst_n

14.2.1.1.1.2.174 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-4989. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7008h**

Figure 14-1658. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-4991. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.175 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-4992. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 700Ch**

Figure 14-1659. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-4994. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.176 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4995. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7100h**

Figure 14-1660. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-4997. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.177 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4998. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7104h**

Figure 14-1661. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-5000. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.178 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5001. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7108h**

Figure 14-1662. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-5003. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.179 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5004. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 710Ch**

Figure 14-1663. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-5006. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.180 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5007. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7110h**

Figure 14-1664. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-5009. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.181 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5010. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7114h**

Figure 14-1665. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-5012. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.182 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register (Offset = 7118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5013. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7118h**

Figure 14-1666. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6							
R/W							
0h							

Table 14-5015. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.183 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register (Offset = 711Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5016. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 711Ch**

Figure 14-1667. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7							
R/W							
0h							

Table 14-5018. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.184 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register (Offset = 7120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5019. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7120h**

Figure 14-1668. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5021. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.185 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register (Offset = 7124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5022. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7124h**

Figure 14-1669. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9							
R/W							
0h							

Table 14-5024. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.186 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register (Offset = 7128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5025. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7128h**

Figure 14-1670. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10							
R/W							
0h							

Table 14-5027. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.187 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register (Offset = 712Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5028. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 712Ch

Figure 14-1671. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5030. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.188 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register (Offset = 7130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5031. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 7130h

Figure 14-1672. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12							
R/W							
0h							

Table 14-5033. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.189 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register (Offset = 7134h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5034. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7134h**

Figure 14-1673. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R13							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R13							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R13							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R13							
R/W							
0h							

Table 14-5036. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R13	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.190 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register (Offset = 7138h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5037. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 7138h**

Figure 14-1674. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R14							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R14							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R14							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R14							
R/W							
0h							

Table 14-5039. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R14	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.191 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register

1 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register (Offset = 8000h) [reset = 7h]

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Table 14-5040. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8000h**

Figure 14-1675. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>OBSCLK0_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OBSCLK0_CTRL_CLK_DIV</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">OBSCLK0_CTRL_CLK_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-5042. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	OBSCLK0_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_por_rst_n
15:8	OBSCLK0_CTRL_CLK_DIV	R/W	0h	OBSCLK0 output divider Reset Source: mod_por_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	OBSCLK0_CTRL_CLK_SEL	R/W	7h	OBSCLK0 clock source selection. Reset Source: mod_por_rst_n

14.2.1.1.1.2.192 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register

1 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register (Offset = 8010h) [reset = 0h]

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Table 14-5043. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8010h**

Figure 14-1676. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			CLKOUT_CTRL_CLK_EN	RESERVED			CLKOUT_CTRL_CLK_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-5045. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	CLKOUT_CTRL_CLK_EN	R/W	0h	When set, activates CLKOUT output Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	CLKOUT_CTRL_CLK_SEL	R/W	0h	Selects CLKOUT clock source Reset Source: mod_g_rst_n

14.2.1.1.1.2.193 MAIN_CTRL_MMR_CFG0_GTC_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_GTC_CLKSEL Register (Offset = 8030h) [reset = 0h]

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Table 14-5046. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8030h

Figure 14-1677. MAIN_CTRL_MMR_CFG0_GTC_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					GTC_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-5048. MAIN_CTRL_MMR_CFG0_GTC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	GTC_CLKSEL_CLK_SEL	R/W	0h	Selects the GTC timebase clock source Reset Source: mod_g_rst_n

14.2.1.1.1.2.194 MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL Register (Offset = 803Ch) [reset = 0h]

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Table 14-5049. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 803Ch

Figure 14-1678. MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EFUSE_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5051. MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EFUSE_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source Reset Source: mod_por_rst_n

14.2.1.1.1.2.195 MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL Register (Offset = 8040h) [reset = 0h]

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Table 14-5052. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8040h

Figure 14-1679. MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					ICSSG0_CLKSEL_IEP_CLKSEL		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ICSSG0_CLKSEL_CORE_CLKSEL
NONE							R/W
0h							0h

Table 14-5054. MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	ICSSG0_CLKSEL_IEP_CLKSEL	R/W	0h	Selects the ICSSG0 IEP clock source Reset Source: sys_por_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	ICSSG0_CLKSEL_CORE_CLKSEL	R/W	0h	Selects the ICSSG0 functional clock source Reset Source: sys_por_rst_n

14.2.1.1.1.2.196 MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL Register (Offset = 8044h) [reset = 0h]

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Table 14-5055. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8044h**

Figure 14-1680. MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					ICSSG1_CLKSEL_IEP_CLKSEL		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ICSSG1_CLKSEL_CORE_CLKSEL
NONE							R/W
0h							0h

Table 14-5057. MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	ICSSG1_CLKSEL_IEP_CLKSEL	R/W	0h	Selects the ICSSG1 IEP clock source Reset Source: sys_por_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	ICSSG1_CLKSEL_CORE_CLKSEL	R/W	0h	Selects the ICSSG1 functional clock source Reset Source: sys_por_rst_n

14.2.1.1.1.2.197 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register (Offset = 8060h) [reset = 0h]

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Table 14-5058. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8060h**

Figure 14-1681. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL0_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5060. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL0_CLKSEL_BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.198 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register (Offset = 8064h) [reset = 0h]

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Table 14-5061. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8064h**

Figure 14-1682. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL1_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5063. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL1_CLKSEL_BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.199 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register (Offset = 8068h) [reset = 0h]

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Table 14-5064. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8068h**

Figure 14-1683. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL2_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5066. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL2_CLKSEL_BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.200 MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL Register (Offset = 8080h) [reset = 800000h]

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Table 14-5067. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8080h**

Figure 14-1684. MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL8_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL8_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5069. MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL8_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL8_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.201 MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL Register (Offset = 8090h) [reset = 800000h]

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Table 14-5070. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8090h

Figure 14-1685. MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL12_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL12_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5072. MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL12_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL12_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.202 MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Register (Offset = 8098h) [reset = 800000h]

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Table 14-5073. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**4300 8098h**

Figure 14-1686. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL14_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL14_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5075. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL14_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL14_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.203 MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL Register (Offset = 8120h) [reset = 0h]

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Table 14-5076. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8120h

Figure 14-1687. MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PCIE0_CLKSEL_CPTS_CLKSEL		
NONE					R/W		
0h					0h		

Table 14-5078. MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PCIE0_CLKSEL_CPTS_CLKSEL	R/W	0h	Selects the clock source for the PCIE0 Common Platform Time Stamp module Reset Source: mod_por_rst_n

14.2.1.1.1.2.204 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register (Offset = 8140h) [reset = 0h]

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Table 14-5079. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8140h

Figure 14-1688. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPSW_CLKSEL_CPTS_CLKSEL			
NONE				R/W			
0h				0h			

Table 14-5081. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CPSW_CLKSEL_CPTS_CLKSEL	R/W	0h	Selects the clock source for the CPSW Ethernet switch Common Platform Time Stamp module Reset Source: mod_por_rst_n

14.2.1.1.1.2.205 MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL Register (Offset = 8150h) [reset = 0h]

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Table 14-5082. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8150h**

Figure 14-1689. MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">CPTS_CLKSEL_CPTS_CLKSEL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5084. MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPTS_CLKSEL_CPTS_CLKSEL	R/W	0h	Selects the clock source for the SoC Common Platform Time Stamp module Reset Source: mod_g_rst_n

14.2.1.1.1.2.206 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register (Offset = 8160h) [reset = 0h]

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Table 14-5085. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8160h

Figure 14-1690. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC0_CLKSEL_EMMCSD0_REFCLK_SEL
NONE							R/W
0h							0h

Table 14-5087. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC0_CLKSEL_EMMCSD0_REFCLK_SEL	R/W	0h	eMMC XIN_CLK selection Reset Source: mod_g_rst_n

14.2.1.1.1.2.207 MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL Register (Offset = 8168h) [reset = 1h]

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Table 14-5088. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8168h**

Figure 14-1691. MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							EMMC1_CLKSEL_EMMCSD1_IO_CLKLB_SEL
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							EMMC1_CLKSEL_EMMCSD1_REFCLK_SEL
NONE							R/W
0h							1h

Table 14-5090. MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC1_CLKSEL_EMMCSD1_IO_CLKLB_SEL	R/W	0h	eMMC IO Clock Selection: Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC1_CLKSEL_EMMCSD1_REFCLK_SEL	R/W	1h	eMMC XIN_CLK selection Reset Source: mod_g_rst_n

14.2.1.1.1.2.208 MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL Register (Offset = 8180h) [reset = 0h]

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Table 14-5091. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8180h

Figure 14-1692. MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GPMC_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5093. MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GPMC_CLKSEL_CLK_SEL	R/W	0h	Selects the GPMC clock source Reset Source: mod_g_rst_n

14.2.1.1.1.2.209 MAIN_CTRL_MMR_CFG0_USB0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USB0_CLKSEL Register (Offset = 8190h) [reset = 0h]

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Table 14-5094. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8190h**

Figure 14-1693. MAIN_CTRL_MMR_CFG0_USB0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							USB0_CLKSEL_REFCLK_SEL
NONE							R/W
0h							0h

Table 14-5096. MAIN_CTRL_MMR_CFG0_USB0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USB0_CLKSEL_REFCLK_SEL	R/W	0h	Selects the clock source for the USB0 ref_clk. Reset Source: mod_g_rst_n

14.2.1.1.1.2.210 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register (Offset = 81B0h) [reset = 0h]

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Table 14-5097. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81B0h**

Figure 14-1694. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER0_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5099. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER0_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.211 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register (Offset = 81B4h) [reset = 0h]

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Table 14-5100. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 81B4h

Figure 14-1695. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER1_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5102. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER1_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.212 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register (Offset = 81B8h) [reset = 0h]

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Table 14-5103. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81B8h**

Figure 14-1696. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMER2_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5105. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER2_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.213 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register (Offset = 81BCh) [reset = 0h]

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Table 14-5106. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81BCh**

Figure 14-1697. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER3_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5108. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER3_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.214 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register (Offset = 81C0h) [reset = 0h]

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Table 14-5109. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81C0h**

Figure 14-1698. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER4_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5111. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER4_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.215 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register (Offset = 81C4h) [reset = 0h]

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Table 14-5112. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81C4h**

Figure 14-1699. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER5_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5114. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER5_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.216 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register (Offset = 81C8h) [reset = 0h]

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Table 14-5115. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81C8h**

Figure 14-1700. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER6_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5117. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER6_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.217 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register (Offset = 81CCh) [reset = 0h]

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Table 14-5118. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81CCh**

Figure 14-1701. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER7_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5120. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER7_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.218 MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL Register (Offset = 81D0h) [reset = 0h]

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Table 14-5121. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81D0h**

Figure 14-1702. MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER8_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5123. MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER8_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.219 MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL Register (Offset = 81D4h) [reset = 0h]

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Table 14-5124. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 81D4h

Figure 14-1703. MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER9_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5126. MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER9_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.220 MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL Register (Offset = 81D8h) [reset = 0h]

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Table 14-5127. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 81D8h

Figure 14-1704. MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER10_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5129. MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER10_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.221 MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL Register (Offset = 81DCh) [reset = 0h]

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Table 14-5130. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 81DCh**

Figure 14-1705. MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER11_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5132. MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER11_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.222 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register (Offset = 8200h) [reset = 0h]

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Table 14-5133. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8200h**

Figure 14-1706. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI0_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5135. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI0_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.223 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register (Offset = 8204h) [reset = 0h]

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Table 14-5136. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8204h**

Figure 14-1707. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI1_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5138. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI1_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.224 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register (Offset = 8208h) [reset = 0h]

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Table 14-5139. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8208h**

Figure 14-1708. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI2_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5141. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI2_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.225 MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL Register (Offset = 820Ch) [reset = 0h]

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Table 14-5142. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 820Ch**

Figure 14-1709. MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI3_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5144. MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI3_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.226 MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL Register (Offset = 8210h) [reset = 0h]

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Table 14-5145. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8210h**

Figure 14-1710. MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI4_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5147. MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI4_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.227 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register (Offset = 8240h) [reset = 3h]

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Table 14-5148. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8240h**

Figure 14-1711. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART0_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART0_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-5150. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART0_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART0_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.228 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register (Offset = 8244h) [reset = 3h]

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Table 14-5151. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8244h**

Figure 14-1712. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART1_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART1_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-5153. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART1_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART1_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.229 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register (Offset = 8248h) [reset = 3h]

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Table 14-5154. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8248h

Figure 14-1713. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART2_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART2_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-5156. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART2_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART2_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.230 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register (Offset = 824Ch) [reset = 3h]

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Table 14-5157. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 824Ch

Figure 14-1714. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART3_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART3_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-5159. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART3_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART3_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.231 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register (Offset = 8250h) [reset = 3h]

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Table 14-5160. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8250h**

Figure 14-1715. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART4_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART4_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-5162. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART4_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART4_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.232 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register (Offset = 8254h) [reset = 3h]

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Table 14-5163. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8254h

Figure 14-1716. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART5_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART5_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-5165. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART5_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART5_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.233 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register

1 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register (Offset = 8258h) [reset = 3h]

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Table 14-5166. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8258h**

Figure 14-1717. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART6_CLK_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART6_CLK_CTRL_CLK_DIV</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-5168. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART6_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART6_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.234 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register (Offset = 8280h) [reset = 0h]

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Table 14-5169. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8280h

Figure 14-1718. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART0_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5171. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART0_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART0: Reset Source: mod_g_rst_n

14.2.1.1.1.2.235 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register (Offset = 8284h) [reset = 0h]

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Table 14-5172. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8284h**

Figure 14-1719. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART1_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5174. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART1_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART1: Reset Source: mod_g_rst_n

14.2.1.1.1.2.236 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register (Offset = 8288h) [reset = 0h]

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Table 14-5175. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8288h

Figure 14-1720. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART2_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5177. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART2_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART2: Reset Source: mod_g_rst_n

14.2.1.1.1.2.237 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register (Offset = 828Ch) [reset = 0h]

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Table 14-5178. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 828Ch

Figure 14-1721. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART3_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5180. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART3_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART3: Reset Source: mod_g_rst_n

14.2.1.1.1.2.238 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register (Offset = 8290h) [reset = 0h]

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Table 14-5181. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8290h

Figure 14-1722. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART4_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5183. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART4_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART4: Reset Source: mod_g_rst_n

14.2.1.1.1.2.239 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register (Offset = 8294h) [reset = 0h]

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Table 14-5184. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8294h**

Figure 14-1723. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART5_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5186. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART5_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART5: Reset Source: mod_g_rst_n

14.2.1.1.1.2.240 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register (Offset = 8298h) [reset = 0h]

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Table 14-5187. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8298h**

Figure 14-1724. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART6_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5189. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART6_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART6: Reset Source: mod_g_rst_n

14.2.1.1.1.2.241 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register (Offset = 8380h) [reset = 0h]

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Table 14-5190. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8380h

Figure 14-1725. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD0_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5192. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD0_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD0_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.242 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register (Offset = 8384h) [reset = 0h]

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Table 14-5193. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8384h**

Figure 14-1726. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD1_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD1_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5195. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD1_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD1_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD1_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.243 MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL Register (Offset = 83A0h) [reset = 0h]

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Table 14-5196. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 83A0h

Figure 14-1727. MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD8_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD8_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5198. MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD8_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD8_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD8_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.244 MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL Register (Offset = 83A4h) [reset = 0h]

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Table 14-5199. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 83A4h**

Figure 14-1728. MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD9_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD9_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5201. MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD9_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD9_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD9_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.245 MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL Register (Offset = 83A8h) [reset = 0h]

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Table 14-5202. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 83A8h**

Figure 14-1729. MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD10_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD10_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5204. MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD10_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD10_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD10_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.246 MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL Register (Offset = 83ACh) [reset = 0h]

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Table 14-5205. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 83ACh**

Figure 14-1730. MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD11_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD11_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5207. MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD11_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD11_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD11_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.247 MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL Register (Offset = 8400h) [reset = 0h]

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Table 14-5208. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8400h**

Figure 14-1731. MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SERDES0_CLKSEL_CORE_REFCLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5210. MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SERDES0_CLKSEL_CORE_REFCLK_SEL	R/W	0h	Selects the source for the core_refclk input Reset Source: mod_g_rst_n

14.2.1.1.1.2.248 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register (Offset = 8480h) [reset = 0h]

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Table 14-5211. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8480h

Figure 14-1732. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5213. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN0_CLKSEL_CLK_SEL	R/W	0h	MAIN MCAN_CLK selection Reset Source: sys_por_rst_n

14.2.1.1.1.2.249 MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL Register (Offset = 8484h) [reset = 0h]

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Table 14-5214. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8484h**

Figure 14-1733. MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN1_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5216. MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN1_CLKSEL_CLK_SEL	R/W	0h	MAIN MCAN_CLK selection Reset Source: sys_por_rst_n

14.2.1.1.1.2.250 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register (Offset = 8500h) [reset = 0h]

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Table 14-5217. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 8500h

Figure 14-1734. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			OSPI0_CLKSEL_LOOPCLK_SEL	RESERVED			OSPI0_CLKSEL_CLK_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-5219. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	OSPI0_CLKSEL_LOOPCLK_SEL	R/W	0h	OBSPI0 Loopback clock source Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	OSPI0_CLKSEL_CLK_SEL	R/W	0h	OSPI0 reference clock selection Reset Source: mod_g_rst_n

14.2.1.1.1.2.251 MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL Register

1 MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL Register (Offset = 8510h) [reset = 0h]

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Table 14-5220. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 8510h**

Figure 14-1735. MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ADC0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5222. MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ADC0_CLKSEL_CLK_SEL	R/W	0h	Selects the sampling clock source for ADC0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.252 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

- KICK0 component

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Table 14-5223. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9008h**

Figure 14-1736. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0							
R/W							
0h							

Table 14-5225. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.253 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

- KICK1 component

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Table 14-5226. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 900Ch**

Figure 14-1737. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1							
R/W							
0h							

Table 14-5228. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.254 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register (Offset = 9100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5229. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9100h**

Figure 14-1738. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5231. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.255 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register (Offset = 9104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5232. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9104h**

Figure 14-1739. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1_READONLY							
R							
0h							

Table 14-5234. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.256 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register (Offset = 9108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5235. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9108h**

Figure 14-1740. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P2_R2_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P2_R2_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P2_R2_READONLY							
R							
0h							

Table 14-5237. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.257 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register (Offset = 910Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5238. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 910Ch**

Figure 14-1741. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R3_READONLY							
R							
0h							

Table 14-5240. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.258 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register (Offset = 9110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5241. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9110h**

Figure 14-1742. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4_READONLY							
R							
0h							

Table 14-5243. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.259 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register (Offset = 9114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5244. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9114h**

Figure 14-1743. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5_READONLY							
R							
0h							

Table 14-5246. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.260 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register (Offset = 9118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5247. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9118h**

Figure 14-1744. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6_READONLY							
R							
0h							

Table 14-5249. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.261 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register (Offset = 911Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5250. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 911Ch**

Figure 14-1745. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7_READONLY							
R							
0h							

Table 14-5252. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.262 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register (Offset = 9120h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5253. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9120h**

Figure 14-1746. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R8_READONLY							
R							
0h							

Table 14-5255. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R8_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.263 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register (Offset = 9124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5256. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9124h**

Figure 14-1747. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R9_READONLY							
R							
0h							

Table 14-5258. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.264 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register (Offset = 9128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5259. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 9128h**

Figure 14-1748. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R10_READONLY							
R							
0h							

Table 14-5261. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.265 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register (Offset = A000h) [reset = 7h]

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Table 14-5262. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A000h

Figure 14-1749. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>OBSCLK0_CTRL_CLK_DIV_LD_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OBSCLK0_CTRL_CLK_DIV_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">OBSCLK0_CTRL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-5264. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	OBSCLK0_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_por_rst_n
15:8	OBSCLK0_CTRL_CLK_DIV_PROXY	R/W	0h	OBSCLK0 output divider Reset Source: mod_por_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	OBSCLK0_CTRL_CLK_SEL_PROXY	R/W	7h	OBSCLK0 clock source selection. Reset Source: mod_por_rst_n

14.2.1.1.1.2.266 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register (Offset = A010h) [reset = 0h]

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Table 14-5265. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A010h**

Figure 14-1750. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			CLKOUT_CTRL_CLK_EN_PROXY	RESERVED			CLKOUT_CTRL_CLK_SEL_PROXY
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-5267. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	CLKOUT_CTRL_CLK_EN_PROXY	R/W	0h	When set, activates CLKOUT output Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	CLKOUT_CTRL_CLK_SEL_PROXY	R/W	0h	Selects CLKOUT clock source Reset Source: mod_g_rst_n

14.2.1.1.1.2.267 MAIN_CTRL_MMR_CFG0_GTC_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_GTC_CLKSEL_PROXY Register (Offset = A030h) [reset = 0h]

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Table 14-5268. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A030h

Figure 14-1751. MAIN_CTRL_MMR_CFG0_GTC_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					GTC_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-5270. MAIN_CTRL_MMR_CFG0_GTC_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	GTC_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the GTC timebase clock source Reset Source: mod_g_rst_n

14.2.1.1.1.2.268 MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY Register (Offset = A03Ch) [reset = 0h]

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Table 14-5271. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A03Ch

Figure 14-1752. MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EFUSE_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5273. MAIN_CTRL_MMR_CFG0_EFUSE_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EFUSE_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source Reset Source: mod_por_rst_n

14.2.1.1.1.2.269 MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL_PROXY Register (Offset = A040h) [reset = 0h]

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Table 14-5274. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A040h

Figure 14-1753. MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					ICSSG0_CLKSEL_IEP_CLKSEL_PROXY		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ICSSG0_CLKSEL_CORE_CLKSEL_PROXY
NONE							R/W
0h							0h

Table 14-5276. MAIN_CTRL_MMR_CFG0_ICSSG0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	ICSSG0_CLKSEL_IEP_CLKSEL_PROXY	R/W	0h	Selects the ICSSG0 IEP clock source Reset Source: sys_por_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	ICSSG0_CLKSEL_CORE_CLKSEL_PROXY	R/W	0h	Selects the ICSSG0 functional clock source Reset Source: sys_por_rst_n

14.2.1.1.1.2.270 MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL_PROXY Register (Offset = A044h) [reset = 0h]

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Table 14-5277. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A044h**

Figure 14-1754. MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					ICSSG1_CLKSEL_IEP_CLKSEL_PROXY		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ICSSG1_CLKSEL_CORE_CLKSEL_PROXY
NONE							R/W
0h							0h

Table 14-5279. MAIN_CTRL_MMR_CFG0_ICSSG1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	ICSSG1_CLKSEL_IEP_CLKSEL_PROXY	R/W	0h	Selects the ICSSG1 IEP clock source Reset Source: sys_por_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	ICSSG1_CLKSEL_CORE_CLKSEL_PROXY	R/W	0h	Selects the ICSSG1 functional clock source Reset Source: sys_por_rst_n

14.2.1.1.1.2.271 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register (Offset = A060h) [reset = 0h]

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Table 14-5280. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A060h

Figure 14-1755. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL0_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5282. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL0_CLKSEL_BYP_WARM_RST_PROXY	R/W	0h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.272 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register (Offset = A064h) [reset = 0h]

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Table 14-5283. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A064h**

Figure 14-1756. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>MAIN_PLL1_CLKSEL_BYP_WARM_RST_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5285. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL1_CLKSEL_BYP_WARM_RST_PROXY	R/W	0h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.273 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register (Offset = A068h) [reset = 0h]

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Table 14-5286. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A068h**

Figure 14-1757. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL2_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5288. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL2_CLKSEL_BYP_WARM_RST_PROXY	R/W	0h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.274 MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY Register (Offset = A080h) [reset = 800000h]

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Table 14-5289. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A080h

Figure 14-1758. MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL8_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL8_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5291. MAIN_CTRL_MMR_CFG0_MAIN_PLL8_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL8_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL8_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.275 MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY Register (Offset = A090h) [reset = 800000h]

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Table 14-5292. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A090h**

Figure 14-1759. MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL12_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL12_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5294. MAIN_CTRL_MMR_CFG0_MAIN_PLL12_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL12_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL12_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.276 MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Register (Offset = A098h) [reset = 800000h]

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Table 14-5295. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A098h

Figure 14-1760. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL14_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL14_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5297. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL14_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL14_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.277 MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL_PROXY Register (Offset = A120h) [reset = 0h]

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Table 14-5298. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A120h**

Figure 14-1761. MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PCIE0_CLKSEL_CPTS_CLKSEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-5300. MAIN_CTRL_MMR_CFG0_PCIE0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PCIE0_CLKSEL_CPTS_CLKSEL_PROXY	R/W	0h	Selects the clock source for the PCIE0 Common Platform Time Stamp module Reset Source: mod_por_rst_n

14.2.1.1.1.2.278 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register (Offset = A140h) [reset = 0h]

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Table 14-5301. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A140h

Figure 14-1762. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPSW_CLKSEL_CPTS_CLKSEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5303. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CPSW_CLKSEL_CPTS_CLKSEL_PROXY	R/W	0h	Selects the clock source for the CPSW Ethernet switch Common Platform Time Stamp module Reset Source: mod_por_rst_n

14.2.1.1.1.2.279 MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL_PROXY Register (Offset = A150h) [reset = 0h]

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Table 14-5304. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A150h**

Figure 14-1763. MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CPTS_CLKSEL_CPTS_CLKSEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-5306. MAIN_CTRL_MMR_CFG0_CPTS_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPTS_CLKSEL_CPTS_CLKSEL_PROXY	R/W	0h	Selects the clock source for the SoC Common Platform Time Stamp module Reset Source: mod_g_rst_n

14.2.1.1.1.2.280 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register (Offset = A160h) [reset = 0h]

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Table 14-5307. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A160h**

Figure 14-1764. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC0_CLKSEL_EMMCSD0_REFCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5309. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC0_CLKSEL_EMMCSD0_REFCLK_SEL_PROXY	R/W	0h	eMMC XIN_CLK selection Reset Source: mod_g_rst_n

14.2.1.1.1.2.281 MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY Register (Offset = A168h) [reset = 1h]

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Table 14-5310. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A168h

Figure 14-1765. MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							EMMC1_CLKSEL_EMMCSD1_IO_CLKLB_SEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC1_CLKSEL_EMMCSD1_REFCLK_SEL_PROXY
NONE							R/W
0h							1h

Table 14-5312. MAIN_CTRL_MMR_CFG0_EMMC1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC1_CLKSEL_EMMCSD1_IO_CLKLB_SEL_PROXY	R/W	0h	eMMC IO Clock Selection: Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC1_CLKSEL_EMMCSD1_REFCLK_SEL_PROXY	R/W	1h	eMMC XIN_CLK selection Reset Source: mod_g_rst_n

14.2.1.1.1.2.282 MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY Register (Offset = A180h) [reset = 0h]

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Table 14-5313. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A180h**

Figure 14-1766. MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GPMC_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5315. MAIN_CTRL_MMR_CFG0_GPMC_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GPMC_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the GPMC clock source Reset Source: mod_g_rst_n

14.2.1.1.1.2.283 MAIN_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register (Offset = A190h) [reset = 0h]

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Table 14-5316. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A190h

Figure 14-1767. MAIN_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USB0_CLKSEL_REFCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5318. MAIN_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USB0_CLKSEL_REFCLK_SEL_PROXY	R/W	0h	Selects the clock source for the USB0 ref_clk. Reset Source: mod_g_rst_n

14.2.1.1.1.2.284 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register (Offset = A1B0h) [reset = 0h]

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Table 14-5319. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A1B0h

Figure 14-1768. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER0_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5321. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.285 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register (Offset = A1B4h) [reset = 0h]

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Table 14-5322. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A1B4h**

Figure 14-1769. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER1_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5324. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.286 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register (Offset = A1B8h) [reset = 0h]

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Table 14-5325. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A1B8h**

Figure 14-1770. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER2_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5327. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.287 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register (Offset = A1BCh) [reset = 0h]

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Table 14-5328. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A1BCh

Figure 14-1771. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMER3_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5330. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.288 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register (Offset = A1C0h) [reset = 0h]

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Table 14-5331. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A1C0h**

Figure 14-1772. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER4_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5333. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.289 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register (Offset = A1C4h) [reset = 0h]

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Table 14-5334. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A1C4h

Figure 14-1773. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER5_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5336. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER5_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.290 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register (Offset = A1C8h) [reset = 0h]

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Table 14-5337. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A1C8h

Figure 14-1774. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER6_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5339. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER6_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.291 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register (Offset = A1CCh) [reset = 0h]

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Table 14-5340. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A1CCh

Figure 14-1775. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER7_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5342. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER7_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.292 MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY Register (Offset = A1D0h) [reset = 0h]

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Table 14-5343. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A1D0h

Figure 14-1776. MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER8_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5345. MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER8_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.293 MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY Register (Offset = A1D4h) [reset = 0h]

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Table 14-5346. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A1D4h

Figure 14-1777. MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER9_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5348. MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER9_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.294 MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY Register (Offset = A1D8h) [reset = 0h]

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Table 14-5349. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A1D8h**

Figure 14-1778. MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER10_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5351. MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER10_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.295 MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY Register (Offset = A1DCh) [reset = 0h]

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Table 14-5352. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A1DCh

Figure 14-1779. MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER11_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5354. MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER11_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.1.2.296 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register (Offset = A200h) [reset = 0h]

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Table 14-5355. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A200h

Figure 14-1780. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5357. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.297 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register (Offset = A204h) [reset = 0h]

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Table 14-5358. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A204h

Figure 14-1781. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5360. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.298 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register (Offset = A208h) [reset = 0h]

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Table 14-5361. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A208h**

Figure 14-1782. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI2_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5363. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI2_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.299 MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY Register (Offset = A20Ch) [reset = 0h]

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Table 14-5364. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A20Ch

Figure 14-1783. MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI3_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5366. MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI3_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.300 MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY Register (Offset = A210h) [reset = 0h]

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Table 14-5367. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A210h

Figure 14-1784. MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI4_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5369. MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI4_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.301 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register (Offset = A240h) [reset = 3h]

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Table 14-5370. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A240h

Figure 14-1785. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART0_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART0_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-5372. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART0_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART0_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.302 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register (Offset = A244h) [reset = 3h]

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Table 14-5373. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A244h**

Figure 14-1786. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							USART1_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						USART1_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-5375. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART1_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART1_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.303 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register (Offset = A248h) [reset = 3h]

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Table 14-5376. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A248h

Figure 14-1787. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							USART2_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						USART2_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-5378. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART2_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART2_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.304 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register (Offset = A24Ch) [reset = 3h]

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Table 14-5379. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A24Ch

Figure 14-1788. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART3_CLK_CTRL_CLK_DIV_LD_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART3_CLK_CTRL_CLK_DIV_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-5381. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART3_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART3_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.305 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register (Offset = A250h) [reset = 3h]

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Table 14-5382. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A250h

Figure 14-1789. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							USART4_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						USART4_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-5384. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART4_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART4_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.306 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register (Offset = A254h) [reset = 3h]

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Table 14-5385. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**4300 A254h**

Figure 14-1790. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART5_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART5_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-5387. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART5_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART5_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.307 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register (Offset = A258h) [reset = 3h]

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Table 14-5388. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A258h**

Figure 14-1791. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART6_CLK_CTRL_CLK_DIV_LD_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART6_CLK_CTRL_CLK_DIV_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-5390. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART6_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART6_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.308 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register (Offset = A280h) [reset = 0h]

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Table 14-5391. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A280h**

Figure 14-1792. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART0_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5393. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART0: Reset Source: mod_g_rst_n

14.2.1.1.1.2.309 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register (Offset = A284h) [reset = 0h]

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Table 14-5394. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A284h**

Figure 14-1793. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART1_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5396. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART1: Reset Source: mod_g_rst_n

14.2.1.1.1.2.310 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register (Offset = A288h) [reset = 0h]

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Table 14-5397. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A288h**

Figure 14-1794. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART2_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5399. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART2: Reset Source: mod_g_rst_n

14.2.1.1.1.2.311 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register (Offset = A28Ch) [reset = 0h]

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Table 14-5400. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A28Ch

Figure 14-1795. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART3_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5402. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART3: Reset Source: mod_g_rst_n

14.2.1.1.1.2.312 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register (Offset = A290h) [reset = 0h]

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Table 14-5403. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A290h

Figure 14-1796. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART4_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5405. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART4: Reset Source: mod_g_rst_n

14.2.1.1.1.2.313 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register (Offset = A294h) [reset = 0h]

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Table 14-5406. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A294h

Figure 14-1797. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART5_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5408. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART5_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART5: Reset Source: mod_g_rst_n

14.2.1.1.1.2.314 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register (Offset = A298h) [reset = 0h]

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Table 14-5409. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A298h**

Figure 14-1798. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART6_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5411. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART6_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART6: Reset Source: mod_g_rst_n

14.2.1.1.1.2.315 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register (Offset = A380h) [reset = 0h]

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Table 14-5412. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A380h**

Figure 14-1799. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD0_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5414. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD0_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.316 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register (Offset = A384h) [reset = 0h]

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Table 14-5415. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A384h**

Figure 14-1800. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD1_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD1_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5417. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD1_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD1_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.317 MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL_PROXY Register (Offset = A3A0h) [reset = 0h]

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Table 14-5418. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A3A0h

Figure 14-1801. MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD8_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD8_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5420. MAIN_CTRL_MMR_CFG0_WWD8_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD8_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD8_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD8_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.318 MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL_PROXY Register (Offset = A3A4h) [reset = 0h]

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Table 14-5421. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A3A4h**

Figure 14-1802. MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>WWD9_CLKSEL_WRTLOCK_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">WWD9_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-5423. MAIN_CTRL_MMR_CFG0_WWD9_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD9_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD9_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD9_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.319 MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL_PROXY Register (Offset = A3A8h) [reset = 0h]

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Table 14-5424. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A3A8h**

Figure 14-1803. MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD10_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD10_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5426. MAIN_CTRL_MMR_CFG0_WWD10_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD10_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD10_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD10_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.320 MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL_PROXY Register (Offset = A3ACh) [reset = 0h]

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Table 14-5427. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A3ACh

Figure 14-1804. MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD11_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD11_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5429. MAIN_CTRL_MMR_CFG0_WWD11_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD11_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD11_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD11_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.1.2.321 MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL_PROXY Register (Offset = A400h) [reset = 0h]

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Table 14-5430. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A400h**

Figure 14-1805. MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SERDES0_CLKSEL_CORE_REFCLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5432. MAIN_CTRL_MMR_CFG0_SERDES0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SERDES0_CLKSEL_CORE_REFCLK_SEL_PROXY	R/W	0h	Selects the source for the core_refclk input Reset Source: mod_g_rst_n

14.2.1.1.1.2.322 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register (Offset = A480h) [reset = 0h]

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Table 14-5433. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 A480h

Figure 14-1806. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5435. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN0_CLKSEL_CLK_SEL_PROXY	R/W	0h	MAIN MCAN_CLK selection Reset Source: sys_por_rst_n

14.2.1.1.1.2.323 MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY Register (Offset = A484h) [reset = 0h]

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Table 14-5436. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A484h**

Figure 14-1807. MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN1_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5438. MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN1_CLKSEL_CLK_SEL_PROXY	R/W	0h	MAIN MCAN_CLK selection Reset Source: sys_por_rst_n

14.2.1.1.1.2.324 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register (Offset = A500h) [reset = 0h]

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Table 14-5439. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A500h**

Figure 14-1808. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			OSPI0_CLKSEL_LOOPCLK_SEL_PROXY	RESERVED			OSPI0_CLKSEL_CLK_SEL_PROXY
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-5441. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	OSPI0_CLKSEL_LOOPCLK_SEL_PROXY	R/W	0h	OBSPI0 Loopback clock source Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	OSPI0_CLKSEL_CLK_SEL_PROXY	R/W	0h	OSPI0 reference clock selection Reset Source: mod_g_rst_n

14.2.1.1.1.2.325 MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY Register (Offset = A510h) [reset = 0h]

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Table 14-5442. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 A510h**

Figure 14-1809. MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ADC0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5444. MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ADC0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the sampling clock source for ADC0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.326 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register (Offset = B008h) [reset = 0h]

- KICK0 component

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Table 14-5445. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B008h**

Figure 14-1810. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0_PROXY							
R/W							
0h							

Table 14-5447. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.327 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register (Offset = B00Ch) [reset = 0h]

- KICK1 component

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Table 14-5448. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 B00Ch

Figure 14-1811. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1_PROXY							
R/W							
0h							

Table 14-5450. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.328 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register (Offset = B100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5451. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B100h**

Figure 14-1812. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5453. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.329 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register (Offset = B104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5454. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B104h**

Figure 14-1813. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1							
R/W							
0h							

Table 14-5456. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.330 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register (Offset = B108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5457. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B108h**

Figure 14-1814. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R2							
R/W							
0h							

Table 14-5459. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.331 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register (Offset = B10Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5460. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B10Ch**

Figure 14-1815. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R3							
R/W							
0h							

Table 14-5462. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.332 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register (Offset = B110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5463. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B110h**

Figure 14-1816. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4							
R/W							
0h							

Table 14-5465. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.333 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register (Offset = B114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5466. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B114h**

Figure 14-1817. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5							
R/W							
0h							

Table 14-5468. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.334 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register (Offset = B118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5469. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B118h**

Figure 14-1818. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6							
R/W							
0h							

Table 14-5471. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.335 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register (Offset = B11Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5472. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B11Ch**

Figure 14-1819. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7							
R/W							
0h							

Table 14-5474. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.336 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register (Offset = B120h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5475. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B120h**

Figure 14-1820. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R8							
R/W							
0h							

Table 14-5477. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R8	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.337 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register (Offset = B124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5478. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B124h**

Figure 14-1821. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R9							
R/W							
0h							

Table 14-5480. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.338 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register (Offset = B128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5481. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 B128h**

Figure 14-1822. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R10							
R/W							
0h							

Table 14-5483. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.339 MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE Register

1 MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE Register (Offset = C304h) [reset = 0h]

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Table 14-5484. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 C304h

Figure 14-1823. MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE Name Register

31	30	29	28	27	26	25	24
CHAIN1_CRC_FUSE_CRC							
R							
X							
23	22	21	20	19	18	17	16
CHAIN1_CRC_FUSE_CRC							
R							
X							
15	14	13	12	11	10	9	8
CHAIN1_CRC_FUSE_CRC							
R							
X							
7	6	5	4	3	2	1	0
CHAIN1_CRC_FUSE_CRC							
R							
X							

Table 14-5486. MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN1_CRC_FUSE_CRC	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain1_CALC or Chain1_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.340 MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE Register

1 MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE Register (Offset = C310h) [reset = 0h]

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Table 14-5487. Instance Table

Instance Name	**Physical Address**
CTRL_MMR0	**4300 C310h**

Figure 14-1824. MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE Name Register

31	30	29	28	27	26	25	24
CHAIN4_CRC_FUSE_CRC							
R							
X							
23	22	21	20	19	18	17	16
CHAIN4_CRC_FUSE_CRC							
R							
X							
15	14	13	12	11	10	9	8
CHAIN4_CRC_FUSE_CRC							
R							
X							
7	6	5	4	3	2	1	0
CHAIN4_CRC_FUSE_CRC							
R							
X							

Table 14-5489. MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	CHAIN4_CRC_FUSE_CRC	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain4_CALC or Chain4_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.341 MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE Register

1 MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE Register (Offset = C314h) [reset = 0h]

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Table 14-5490. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 C314h

Figure 14-1825. MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE Name Register

31	30	29	28	27	26	25	24
CHAIN5_CRC_FUSE_CRC							
R							
X							
23	22	21	20	19	18	17	16
CHAIN5_CRC_FUSE_CRC							
R							
X							
15	14	13	12	11	10	9	8
CHAIN5_CRC_FUSE_CRC							
R							
X							
7	6	5	4	3	2	1	0
CHAIN5_CRC_FUSE_CRC							
R							
X							

Table 14-5492. MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN5_CRC_FUSE_CRC	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain5_CALC or Chain5_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.342 MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE Register

1 MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE Register (Offset = C318h) [reset = 0h]

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Table 14-5493. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 C318h**

Figure 14-1826. MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE Name Register

31	30	29	28	27	26	25	24
CHAIN6_CRC_FUSE_CRC							
R							
X							
23	22	21	20	19	18	17	16
CHAIN6_CRC_FUSE_CRC							
R							
X							
15	14	13	12	11	10	9	8
CHAIN6_CRC_FUSE_CRC							
R							
X							
7	6	5	4	3	2	1	0
CHAIN6_CRC_FUSE_CRC							
R							
X							

Table 14-5495. MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN6_CRC_FUSE_CRC	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain6_CALC or Chain6_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.343 MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE Register

1 MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE Register (Offset = C31Ch) [reset = 0h]

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Table 14-5496. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 C31Ch

Figure 14-1827. MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE Name Register

31	30	29	28	27	26	25	24
CHAIN7_CRC_FUSE_CRC							
R							
X							
23	22	21	20	19	18	17	16
CHAIN7_CRC_FUSE_CRC							
R							
X							
15	14	13	12	11	10	9	8
CHAIN7_CRC_FUSE_CRC							
R							
X							
7	6	5	4	3	2	1	0
CHAIN7_CRC_FUSE_CRC							
R							
X							

Table 14-5498. MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN7_CRC_FUSE_CRC	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain7_CALC or Chain7_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.344 MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT Register

1 MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT Register (Offset = C320h) [reset = 0h]

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Table 14-5499. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 C320h

Figure 14-1828. MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FUSE_CRC_STAT_CRC_ERR_7	FUSE_CRC_STAT_CRC_ERR_6	FUSE_CRC_STAT_CRC_ERR_5	FUSE_CRC_STAT_CRC_ERR_4	FUSE_CRC_STAT_CRC_ERR_3	FUSE_CRC_STAT_CRC_ERR_2	FUSE_CRC_STAT_CRC_ERR_1	RESERVED
R	R	R	R	R	R	R	NONE
X	X	X	X	X	X	X	0h

Table 14-5501. MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FUSE_CRC_STAT_CRC_ERR_7	R	X	Indicates eFuse CRC error on chain 7 Reset Source: mod_por_rst_n
6	FUSE_CRC_STAT_CRC_ERR_6	R	X	Indicates eFuse CRC error on chain 6 Reset Source: mod_por_rst_n
5	FUSE_CRC_STAT_CRC_ERR_5	R	X	Indicates eFuse CRC error on chain 5 Reset Source: mod_por_rst_n
4	FUSE_CRC_STAT_CRC_ERR_4	R	X	Indicates eFuse CRC error on chain 4 Reset Source: mod_por_rst_n
3	FUSE_CRC_STAT_CRC_ERR_3	R	X	Indicates eFuse CRC error on chain 3 Reset Source: mod_por_rst_n
2	FUSE_CRC_STAT_CRC_ERR_2	R	X	Indicates eFuse CRC error on chain 2 Reset Source: mod_por_rst_n
1	FUSE_CRC_STAT_CRC_ERR_1	R	X	Indicates eFuse CRC error on chain 1 Reset Source: mod_por_rst_n
0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.345 MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC Register

1 MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC Register (Offset = C324h) [reset = 0h]

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Table 14-5502. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 C324h**

Figure 14-1829. MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC Name Register

31	30	29	28	27	26	25	24
CHAIN1_CRC_CALC_CRC							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN1_CRC_CALC_CRC							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN1_CRC_CALC_CRC							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN1_CRC_CALC_CRC							
R/W							
X							

Table 14-5504. MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN1_CRC_CALC_CRC	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.346 MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC Register

1 MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC Register (Offset = C330h) [reset = 0h]

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Table 14-5505. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 C330h**

Figure 14-1830. MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC Name Register

31	30	29	28	27	26	25	24
CHAIN4_CRC_CALC_CRC							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN4_CRC_CALC_CRC							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN4_CRC_CALC_CRC							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN4_CRC_CALC_CRC							
R/W							
X							

Table 14-5507. MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN4_CRC_CALC_CRC	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.347 MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC Register

1 MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC Register (Offset = C334h) [reset = 0h]

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Table 14-5508. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 C334h**

Figure 14-1831. MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC Name Register

31	30	29	28	27	26	25	24
CHAIN5_CRC_CALC_CRC							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN5_CRC_CALC_CRC							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN5_CRC_CALC_CRC							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN5_CRC_CALC_CRC							
R/W							
X							

Table 14-5510. MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN5_CRC_CALC_CRC	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.348 MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC Register

1 MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC Register (Offset = C338h) [reset = 0h]

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Table 14-5511. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 C338h**

Figure 14-1832. MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC Name Register

31	30	29	28	27	26	25	24
CHAIN6_CRC_CALC_CRC							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN6_CRC_CALC_CRC							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN6_CRC_CALC_CRC							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN6_CRC_CALC_CRC							
R/W							
X							

Table 14-5513. MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN6_CRC_CALC_CRC	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.349 MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC Register

1 MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC Register (Offset = C33Ch) [reset = 0h]

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Table 14-5514. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 C33Ch**

Figure 14-1833. MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC Name Register

31	30	29	28	27	26	25	24
CHAIN7_CRC_CALC_CRC							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN7_CRC_CALC_CRC							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN7_CRC_CALC_CRC							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN7_CRC_CALC_CRC							
R/W							
X							

Table 14-5516. MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN7_CRC_CALC_CRC	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.350 MAIN_CTRL_MMR_CFG0_PBIST_EN Register

1 MAIN_CTRL_MMR_CFG0_PBIST_EN Register (Offset = C400h) [reset = 0h]

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Table 14-5517. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 C400h

Figure 14-1834. MAIN_CTRL_MMR_CFG0_PBIST_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PBIST_EN_PCIE0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED			PBIST_EN_USB0	RESERVED		PBIST_EN_EMMC1	PBIST_EN_EMMC0
NONE			R/W	NONE		R/W	R/W
0h			0h	0h		0h	0h

Table 14-5519. MAIN_CTRL_MMR_CFG0_PBIST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PBIST_EN_PCIE0	R/W	0h	Activates PBIST Access to PCIE0 Memories Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	PBIST_EN_USB0	R/W	0h	Activates PBIST Access to USB0 Memories Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PBIST_EN_EMMC1	R/W	0h	Activates PBIST Access to MMC1 Memories Reset Source: mod_g_rst_n
0	PBIST_EN_EMMC0	R/W	0h	Activates PBIST Access to MMC0 Memories Reset Source: mod_g_rst_n

14.2.1.1.1.2.351 MAIN_CTRL_MMR_CFG0_LOCK3_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK3_KICK0 Register (Offset = D008h) [reset = 0h]

- KICK0 component

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Table 14-5520. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D008h**

Figure 14-1835. MAIN_CTRL_MMR_CFG0_LOCK3_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0							
R/W							
0h							

Table 14-5522. MAIN_CTRL_MMR_CFG0_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.352 MAIN_CTRL_MMR_CFG0_LOCK3_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK3_KICK1 Register (Offset = D00Ch) [reset = 0h]

- KICK1 component

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Table 14-5523. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 D00Ch

Figure 14-1836. MAIN_CTRL_MMR_CFG0_LOCK3_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1							
R/W							
0h							

Table 14-5525. MAIN_CTRL_MMR_CFG0_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.353 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register (Offset = D100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5526. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D100h**

Figure 14-1837. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5528. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.354 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register (Offset = D104h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5529. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D104h**

Figure 14-1838. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R1_READONLY							
R							
0h							

Table 14-5531. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R1_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.355 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register (Offset = D108h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5532. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D108h**

Figure 14-1839. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R2_READONLY							
R							
0h							

Table 14-5534. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R2_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.356 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register (Offset = D10Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5535. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D10Ch**

Figure 14-1840. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R3_READONLY							
R							
0h							

Table 14-5537. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R3_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.357 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register (Offset = D110h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5538. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D110h**

Figure 14-1841. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R4_READONLY							
R							
0h							

Table 14-5540. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R4_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.358 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register (Offset = D114h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5541. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D114h**

Figure 14-1842. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R5_READONLY							
R							
0h							

Table 14-5543. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R5_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.359 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register (Offset = D118h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5544. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D118h**

Figure 14-1843. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R6_READONLY							
R							
0h							

Table 14-5546. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R6_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.360 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register (Offset = D11Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5547. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 D11Ch**

Figure 14-1844. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R7_READONLY							
R							
0h							

Table 14-5549. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R7_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.361 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register (Offset = D120h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5550. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 D120h

Figure 14-1845. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R8_READONLY							
R							
0h							

Table 14-5552. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R8_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.362 MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE_PROXY Register (Offset = E304h) [reset = 0h]

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Table 14-5553. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 E304h**

Figure 14-1846. MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN1_CRC_FUSE_CRC_PROXY							
R							
X							
23	22	21	20	19	18	17	16
CHAIN1_CRC_FUSE_CRC_PROXY							
R							
X							
15	14	13	12	11	10	9	8
CHAIN1_CRC_FUSE_CRC_PROXY							
R							
X							
7	6	5	4	3	2	1	0
CHAIN1_CRC_FUSE_CRC_PROXY							
R							
X							

Table 14-5555. MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_FUSE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN1_CRC_FUSE_CRC_PROXY	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain1_CALC or Chain1_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.363 MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE_PROXY Register (Offset = E310h) [reset = 0h]

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Table 14-5556. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 E310h

Figure 14-1847. MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN4_CRC_FUSE_CRC_PROXY							
R							
X							
23	22	21	20	19	18	17	16
CHAIN4_CRC_FUSE_CRC_PROXY							
R							
X							
15	14	13	12	11	10	9	8
CHAIN4_CRC_FUSE_CRC_PROXY							
R							
X							
7	6	5	4	3	2	1	0
CHAIN4_CRC_FUSE_CRC_PROXY							
R							
X							

Table 14-5558. MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_FUSE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN4_CRC_FUSE_CRC_PROXY	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain4_CALC or Chain4_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.364 MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE_PROXY Register (Offset = E314h) [reset = 0h]

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Table 14-5559. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 E314h**

Figure 14-1848. MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN5_CRC_FUSE_CRC_PROXY							
R							
X							
23	22	21	20	19	18	17	16
CHAIN5_CRC_FUSE_CRC_PROXY							
R							
X							
15	14	13	12	11	10	9	8
CHAIN5_CRC_FUSE_CRC_PROXY							
R							
X							
7	6	5	4	3	2	1	0
CHAIN5_CRC_FUSE_CRC_PROXY							
R							
X							

Table 14-5561. MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_FUSE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN5_CRC_FUSE_CRC_PROXY	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain5_CALC or Chain5_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.365 MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE_PROXY Register (Offset = E318h) [reset = 0h]

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Table 14-5562. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 E318h

Figure 14-1849. MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN6_CRC_FUSE_CRC_PROXY							
R							
X							
23	22	21	20	19	18	17	16
CHAIN6_CRC_FUSE_CRC_PROXY							
R							
X							
15	14	13	12	11	10	9	8
CHAIN6_CRC_FUSE_CRC_PROXY							
R							
X							
7	6	5	4	3	2	1	0
CHAIN6_CRC_FUSE_CRC_PROXY							
R							
X							

Table 14-5564. MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_FUSE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN6_CRC_FUSE_CRC_PROXY	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain6_CALC or Chain6_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.366 MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE_PROXY Register (Offset = E31Ch) [reset = 0h]

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Table 14-5565. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 E31Ch

Figure 14-1850. MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN7_CRC_FUSE_CRC_PROXY							
R							
X							
23	22	21	20	19	18	17	16
CHAIN7_CRC_FUSE_CRC_PROXY							
R							
X							
15	14	13	12	11	10	9	8
CHAIN7_CRC_FUSE_CRC_PROXY							
R							
X							
7	6	5	4	3	2	1	0
CHAIN7_CRC_FUSE_CRC_PROXY							
R							
X							

Table 14-5567. MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_FUSE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN7_CRC_FUSE_CRC_PROXY	R	X	This is the factory programmed CRC value to compare against the calculated value in either Chain7_CALC or Chain7_CALC_RO. Reset Source: mod_por_rst_n

14.2.1.1.1.2.367 MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY Register (Offset = E320h) [reset = 0h]

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Table 14-5568. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 E320h**

Figure 14-1851. MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FUSE_CRC_STAT_CRC_ERR_7_PROXY	FUSE_CRC_STAT_CRC_ERR_6_PROXY	FUSE_CRC_STAT_CRC_ERR_5_PROXY	FUSE_CRC_STAT_CRC_ERR_4_PROXY	FUSE_CRC_STAT_CRC_ERR_3_PROXY	FUSE_CRC_STAT_CRC_ERR_2_PROXY	FUSE_CRC_STAT_CRC_ERR_1_PROXY	RESERVED
R	R	R	R	R	R	R	NONE
X	X	X	X	X	X	X	0h

Table 14-5570. MAIN_CTRL_MMR_CFG0_FUSE_CRC_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FUSE_CRC_STAT_CRC_ERR_7_PROXY	R	X	Indicates eFuse CRC error on chain 7 Reset Source: mod_por_rst_n
6	FUSE_CRC_STAT_CRC_ERR_6_PROXY	R	X	Indicates eFuse CRC error on chain 6 Reset Source: mod_por_rst_n
5	FUSE_CRC_STAT_CRC_ERR_5_PROXY	R	X	Indicates eFuse CRC error on chain 5 Reset Source: mod_por_rst_n
4	FUSE_CRC_STAT_CRC_ERR_4_PROXY	R	X	Indicates eFuse CRC error on chain 4 Reset Source: mod_por_rst_n
3	FUSE_CRC_STAT_CRC_ERR_3_PROXY	R	X	Indicates eFuse CRC error on chain 3 Reset Source: mod_por_rst_n
2	FUSE_CRC_STAT_CRC_ERR_2_PROXY	R	X	Indicates eFuse CRC error on chain 2 Reset Source: mod_por_rst_n
1	FUSE_CRC_STAT_CRC_ERR_1_PROXY	R	X	Indicates eFuse CRC error on chain 1 Reset Source: mod_por_rst_n
0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.368 MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC_PROXY Register (Offset = E324h) [reset = 0h]

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Table 14-5571. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 E324h**

Figure 14-1852. MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN1_CRC_CALC_CRC_PROXY							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN1_CRC_CALC_CRC_PROXY							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN1_CRC_CALC_CRC_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN1_CRC_CALC_CRC_PROXY							
R/W							
X							

Table 14-5573. MAIN_CTRL_MMR_CFG0_CHAIN1_CRC_CALC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN1_CRC_CALC_CRC_PROXY	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.369 MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC_PROXY Register (Offset = E330h) [reset = 0h]

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Table 14-5574. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 E330h**

Figure 14-1853. MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN4_CRC_CALC_CRC_PROXY							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN4_CRC_CALC_CRC_PROXY							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN4_CRC_CALC_CRC_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN4_CRC_CALC_CRC_PROXY							
R/W							
X							

Table 14-5576. MAIN_CTRL_MMR_CFG0_CHAIN4_CRC_CALC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN4_CRC_CALC_CRC_PROXY	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.370 MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC_PROXY Register (Offset = E334h) [reset = 0h]

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Table 14-5577. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4300 E334h

Figure 14-1854. MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN5_CRC_CALC_CRC_PROXY							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN5_CRC_CALC_CRC_PROXY							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN5_CRC_CALC_CRC_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN5_CRC_CALC_CRC_PROXY							
R/W							
X							

Table 14-5579. MAIN_CTRL_MMR_CFG0_CHAIN5_CRC_CALC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN5_CRC_CALC_CRC_PROXY	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.371 MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC_PROXY Register (Offset = E338h) [reset = 0h]

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Table 14-5580. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 E338h**

Figure 14-1855. MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN6_CRC_CALC_CRC_PROXY							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN6_CRC_CALC_CRC_PROXY							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN6_CRC_CALC_CRC_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN6_CRC_CALC_CRC_PROXY							
R/W							
X							

Table 14-5582. MAIN_CTRL_MMR_CFG0_CHAIN6_CRC_CALC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN6_CRC_CALC_CRC_PROXY	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.372 MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC_PROXY Register (Offset = E33Ch) [reset = 0h]

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Table 14-5583. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 E33Ch**

Figure 14-1856. MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC_PROXY Name Register

31	30	29	28	27	26	25	24
CHAIN7_CRC_CALC_CRC_PROXY							
R/W							
X							
23	22	21	20	19	18	17	16
CHAIN7_CRC_CALC_CRC_PROXY							
R/W							
X							
15	14	13	12	11	10	9	8
CHAIN7_CRC_CALC_CRC_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
CHAIN7_CRC_CALC_CRC_PROXY							
R/W							
X							

Table 14-5585. MAIN_CTRL_MMR_CFG0_CHAIN7_CRC_CALC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHAIN7_CRC_CALC_CRC_PROXY	R/W	X	CRC calculated at device power up. Reset Source: mod_por_rst_n

14.2.1.1.1.2.373 MAIN_CTRL_MMR_CFG0_PBIST_EN_PROXY Register

1 MAIN_CTRL_MMR_CFG0_PBIST_EN_PROXY Register (Offset = E400h) [reset = 0h]

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Table 14-5586. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 E400h**

Figure 14-1857. MAIN_CTRL_MMR_CFG0_PBIST_EN_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PBIST_EN_PCIE0_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED			PBIST_EN_USB0_PROXY	RESERVED		PBIST_EN_EMMC1_PROXY	PBIST_EN_EMMC0_PROXY
NONE			R/W	NONE		R/W	R/W
0h			0h	0h		0h	0h

Table 14-5588. MAIN_CTRL_MMR_CFG0_PBIST_EN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PBIST_EN_PCIE0_PROXY	R/W	0h	Activates PBIST Access to PCIE0 Memories Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	PBIST_EN_USB0_PROXY	R/W	0h	Activates PBIST Access to USB0 Memories Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PBIST_EN_EMMC1_PROXY	R/W	0h	Activates PBIST Access to MMC1 Memories Reset Source: mod_g_rst_n
0	PBIST_EN_EMMC0_PROXY	R/W	0h	Activates PBIST Access to MMC0 Memories Reset Source: mod_g_rst_n

14.2.1.1.1.2.374 MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register (Offset = F008h) [reset = 0h]

- KICK0 component

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Table 14-5589. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F008h**

Figure 14-1858. MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0_PROXY							
R/W							
0h							

Table 14-5591. MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.375 MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register (Offset = F00Ch) [reset = 0h]

- KICK1 component

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Table 14-5592. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F00Ch**

Figure 14-1859. MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1_PROXY							
R/W							
0h							

Table 14-5594. MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.376 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register (Offset = F100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5595. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F100h**

Figure 14-1860. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0							
R/W							
0h							

Table 14-5597. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.377 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register (Offset = F104h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5598. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F104h**

Figure 14-1861. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R1							
R/W							
0h							

Table 14-5600. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R1	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.378 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register (Offset = F108h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5601. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F108h**

Figure 14-1862. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R2							
R/W							
0h							

Table 14-5603. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R2	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.379 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register (Offset = F10Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5604. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F10Ch**

Figure 14-1863. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R3							
R/W							
0h							

Table 14-5606. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R3	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.380 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register (Offset = F110h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5607. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F110h**

Figure 14-1864. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R4							
R/W							
0h							

Table 14-5609. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R4	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.381 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register (Offset = F114h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5610. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F114h**

Figure 14-1865. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R5							
R/W							
0h							

Table 14-5612. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R5	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.382 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register (Offset = F118h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5613. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F118h**

Figure 14-1866. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R6							
R/W							
0h							

Table 14-5615. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R6	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.383 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register (Offset = F11Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5616. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F11Ch**

Figure 14-1867. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R7							
R/W							
0h							

Table 14-5618. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R7	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.384 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register (Offset = F120h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5619. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4300 F120h**

Figure 14-1868. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R8							
R/W							
0h							

Table 14-5621. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R8	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.385 MAIN_CTRL_MMR_CFG0_LOCK4_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK4_KICK0 Register (Offset = 11008h) [reset = 0h]

- KICK0 component

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Table 14-5622. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1008h**

Figure 14-1869. MAIN_CTRL_MMR_CFG0_LOCK4_KICK0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK4_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK4_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK4_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK4_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5624. MAIN_CTRL_MMR_CFG0_LOCK4_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.386 MAIN_CTRL_MMR_CFG0_LOCK4_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK4_KICK1 Register (Offset = 1100Ch) [reset = 0h]

- KICK1 component

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Table 14-5625. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 100Ch**

Figure 14-1870. MAIN_CTRL_MMR_CFG0_LOCK4_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1							
R/W							
0h							

Table 14-5627. MAIN_CTRL_MMR_CFG0_LOCK4_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.387 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register (Offset = 11100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5628. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1100h**

Figure 14-1871. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0_READONLY							
R							
0h							

Table 14-5630. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.388 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register (Offset = 11104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5631. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1104h**

Figure 14-1872. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1_READONLY							
R							
0h							

Table 14-5633. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.389 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register (Offset = 11108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5634. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1108h**

Figure 14-1873. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5636. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.390 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register (Offset = 1110Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5637. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 110Ch**

Figure 14-1874. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3_READONLY							
R							
0h							

Table 14-5639. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.391 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register (Offset = 11110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5640. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1110h**

Figure 14-1875. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P4_R4_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P4_R4_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P4_R4_READONLY							
R							
0h							

Table 14-5642. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.392 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register (Offset = 11114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5643. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1114h**

Figure 14-1876. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5_READONLY							
R							
0h							

Table 14-5645. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.393 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register (Offset = 11118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5646. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1118h**

Figure 14-1877. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6_READONLY							
R							
0h							

Table 14-5648. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.394 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register (Offset = 1111Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5649. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 111Ch**

Figure 14-1878. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7_READONLY							
R							
0h							

Table 14-5651. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.395 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register (Offset = 11120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5652. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1120h**

Figure 14-1879. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8_READONLY							
R							
0h							

Table 14-5654. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.396 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register (Offset = 11124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5655. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1124h**

Figure 14-1880. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9_READONLY							
R							
0h							

Table 14-5657. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.397 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register (Offset = 11128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5658. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1128h**

Figure 14-1881. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10_READONLY							
R							
0h							

Table 14-5660. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.398 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register (Offset = 1112Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5661. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 112Ch**

Figure 14-1882. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R11_READONLY							
R							
0h							

Table 14-5663. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R11_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.399 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register (Offset = 11130h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5664. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 1130h**

Figure 14-1883. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R12_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P4_R12_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P4_R12_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P4_R12_READONLY							
R							
0h							

Table 14-5666. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R12_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.400 MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register (Offset = 13008h) [reset = 0h]

- KICK0 component

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Table 14-5667. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3008h**

Figure 14-1884. MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0_PROXY							
R/W							
0h							

Table 14-5669. MAIN_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.401 MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register (Offset = 1300Ch) [reset = 0h]

- KICK1 component

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Table 14-5670. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 300Ch**

Figure 14-1885. MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1_PROXY							
R/W							
0h							

Table 14-5672. MAIN_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.402 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register (Offset = 13100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5673. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3100h**

Figure 14-1886. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0							
R/W							
0h							

Table 14-5675. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.403 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register (Offset = 13104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5676. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3104h**

Figure 14-1887. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1							
R/W							
0h							

Table 14-5678. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.404 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register (Offset = 13108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5679. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3108h**

Figure 14-1888. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2							
R/W							
0h							

Table 14-5681. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.405 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register (Offset = 1310Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5682. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4301 310Ch

Figure 14-1889. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3							
R/W							
0h							

Table 14-5684. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.406 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register (Offset = 13110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5685. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3110h**

Figure 14-1890. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P4_R4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P4_R4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P4_R4							
R/W							
0h							

Table 14-5687. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.407 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register (Offset = 13114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5688. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3114h**

Figure 14-1891. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5							
R/W							
0h							

Table 14-5690. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.408 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register (Offset = 13118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5691. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3118h**

Figure 14-1892. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6							
R/W							
0h							

Table 14-5693. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.409 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register (Offset = 1311Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5694. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 311Ch**

Figure 14-1893. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5696. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.410 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register (Offset = 13120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5697. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3120h**

Figure 14-1894. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8							
R/W							
0h							

Table 14-5699. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.411 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register (Offset = 13124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5700. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3124h**

Figure 14-1895. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9							
R/W							
0h							

Table 14-5702. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.412 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register (Offset = 13128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5703. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3128h**

Figure 14-1896. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10							
R/W							
0h							

Table 14-5705. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.413 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register (Offset = 1312Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5706. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 312Ch**

Figure 14-1897. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5708. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R11	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.414 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register (Offset = 13130h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5709. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 3130h**

Figure 14-1898. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R12							
R/W							
0h							

Table 14-5711. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R12	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.415 MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ Register

1 MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ Register (Offset = 14000h) [reset = 0h]

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Table 14-5712. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 4000h**

Figure 14-1899. MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CHNG_DDR4_FSP_REQ_REQ
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						CHNG_DDR4_FSP_REQ_REQ_TYPE	
NONE						R/W	
0h						0h	

Table 14-5714. MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CHNG_DDR4_FSP_REQ_REQ	R/W	0h	Initiate FSP frequency change Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	CHNG_DDR4_FSP_REQ_REQ_TYPE	R/W	0h	Frequency request type Reset Source: mod_por_rst_n

14.2.1.1.1.2.416 MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK Register

1 MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK Register (Offset = 14004h) [reset = 0h]

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Table 14-5715. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 4004h**

Figure 14-1900. MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHNG_DDR4_FSP_ACK_ACK	RESERVED						CHNG_DDR4_FSP_ACK_ERROR
R	NONE						R
X	0h						X

Table 14-5717. MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CHNG_DDR4_FSP_ACK_ACK	R	X	Frequency change acknowledge. Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	CHNG_DDR4_FSP_ACK_ERROR	R	X	Frequency change error Reset Source: mod_por_rst_n

14.2.1.1.1.2.417 MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ Register

1 MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ Register (Offset = 14080h) [reset = 0h]

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Table 14-5718. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4301 4080h

Figure 14-1901. MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>DDR4_FSP_CLKCHNG_REQ_REQ</td><td colspan="5">RESERVED</td><td colspan="2">DDR4_FSP_CLKCHNG_REQ_REQ_TYPE</td></tr>
<tr><td>R</td><td colspan="5">NONE</td><td colspan="2">R</td></tr>
<tr><td>X</td><td colspan="5">0h</td><td colspan="2">X</td></tr>
</table>

Table 14-5720. MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DDR4_FSP_CLKCHNG_REQ_REQ	R	X	DDR Controller FSP clock change request Reset Source: mod_por_rst_n
6:2	RESERVED	NONE	0h	Reserved
1:0	DDR4_FSP_CLKCHNG_REQ_REQ_TYPE	R	X	Frequency request type Reset Source: mod_por_rst_n

14.2.1.1.1.2.418 MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK Register

1 MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK Register (Offset = 140C0h) [reset = 0h]

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Table 14-5721. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4301 40C0h

Figure 14-1902. MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							DDR4_FSP_CLKCHNG_ACK_ACK
NONE							R/W
0h							0h

Table 14-5723. MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DDR4_FSP_CLKCHNG_ACK_ACK	R/W	0h	DDR FSP clock change ackowledge Reset Source: mod_por_rst_n

14.2.1.1.1.2.419 MAIN_CTRL_MMR_CFG0_LOCK5_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK5_KICK0 Register (Offset = 15008h) [reset = 0h]

- KICK0 component

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Table 14-5724. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 5008h**

Figure 14-1903. MAIN_CTRL_MMR_CFG0_LOCK5_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK5_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK5_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK5_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK5_KICK0							
R/W							
0h							

Table 14-5726. MAIN_CTRL_MMR_CFG0_LOCK5_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK5_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.420 MAIN_CTRL_MMR_CFG0_LOCK5_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK5_KICK1 Register (Offset = 1500Ch) [reset = 0h]

- KICK1 component

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Table 14-5727. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 500Ch**

Figure 14-1904. MAIN_CTRL_MMR_CFG0_LOCK5_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK5_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK5_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK5_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK5_KICK1							
R/W							
0h							

Table 14-5729. MAIN_CTRL_MMR_CFG0_LOCK5_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK5_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.421 MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY Register (Offset = 15100h) [reset = 0h]

Claim bits for Partition 5

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Table 14-5730. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 5100h**

Figure 14-1905. MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P5_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P5_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P5_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P5_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5732. MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P5_R0_READONLY	R	0h	Claim bits for Partition 5 Reset Source: mod_g_rst_n

14.2.1.1.1.2.422 MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY Register (Offset = 15104h) [reset = 0h]

Claim bits for Partition 5

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Table 14-5733. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 5104h**

Figure 14-1906. MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P5_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P5_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P5_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P5_R1_READONLY							
R							
0h							

Table 14-5735. MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P5_R1_READONLY	R	0h	Claim bits for Partition 5 Reset Source: mod_g_rst_n

14.2.1.1.1.2.423 MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY Register (Offset = 16000h) [reset = 0h]

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Table 14-5736. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 6000h**

Figure 14-1907. MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CHNG_DDR4_FSP_REQ_REQ_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						CHNG_DDR4_FSP_REQ_REQ_TYPE_PROXY	
NONE						R/W	
0h						0h	

Table 14-5738. MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_REQ_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CHNG_DDR4_FSP_REQ_REQ_PROXY	R/W	0h	Initiate FSP frequency change Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	CHNG_DDR4_FSP_REQ_REQ_TYPE_PROXY	R/W	0h	Frequency request type Reset Source: mod_por_rst_n

14.2.1.1.1.2.424 MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY Register

1 MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY Register (Offset = 16004h) [reset = 0h]

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Table 14-5739. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 6004h**

Figure 14-1908. MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHNG_DDR4_FSP_ACK_ACK_PROXY	RESERVED						CHNG_DDR4_FSP_ACK_ERROR_PROXY
R	NONE						R
X	0h						X

Table 14-5741. MAIN_CTRL_MMR_CFG0_CHNG_DDR4_FSP_ACK_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CHNG_DDR4_FSP_ACK_ACK_PROXY	R	X	Frequency change acknowledge. Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	CHNG_DDR4_FSP_ACK_ERROR_PROXY	R	X	Frequency change error Reset Source: mod_por_rst_n

14.2.1.1.1.2.425 MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY Register (Offset = 16080h) [reset = 0h]

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Table 14-5742. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 6080h**

Figure 14-1909. MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DDR4_FSP_CLKCHNG_REQ_REQ_PROXY	RESERVED					DDR4_FSP_CLKCHNG_REQ_REQ_TYPE_PROXY	
R	NONE					R	
X	0h					X	

Table 14-5744. MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_REQ_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DDR4_FSP_CLKCHNG_REQ_REQ_PROXY	R	X	DDR Controller FSP clock change request Reset Source: mod_por_rst_n
6:2	RESERVED	NONE	0h	Reserved
1:0	DDR4_FSP_CLKCHNG_REQ_REQ_TYPE_PROXY	R	X	Frequency request type Reset Source: mod_por_rst_n

14.2.1.1.1.2.426 MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY Register

1 MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY Register (Offset = 160C0h) [reset = 0h]

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Table 14-5745. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 60C0h**

Figure 14-1910. MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DDR4_FSP_CLKCHNG_ACK_ACK_PROXY
NONE							R/W
0h							0h

Table 14-5747. MAIN_CTRL_MMR_CFG0_DDR4_FSP_CLKCHNG_ACK_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DDR4_FSP_CLKCHNG_ACK_ACK_PROXY	R/W	0h	DDR FSP clock change ackowledge Reset Source: mod_por_rst_n

14.2.1.1.1.2.427 MAIN_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY Register (Offset = 17008h) [reset = 0h]

- KICK0 component

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Table 14-5748. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 7008h**

Figure 14-1911. MAIN_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK5_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK5_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK5_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK5_KICK0_PROXY							
R/W							
0h							

Table 14-5750. MAIN_CTRL_MMR_CFG0_LOCK5_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK5_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.428 MAIN_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY Register (Offset = 1700Ch) [reset = 0h]

- KICK1 component

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Table 14-5751. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4301 700Ch

Figure 14-1912. MAIN_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK5_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK5_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK5_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK5_KICK1_PROXY							
R/W							
0h							

Table 14-5753. MAIN_CTRL_MMR_CFG0_LOCK5_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK5_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.429 MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0 Register (Offset = 17100h) [reset = 0h]

Claim bits for Partition 5

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Table 14-5754. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 7100h**

Figure 14-1913. MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P5_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P5_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P5_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P5_R0							
R/W							
0h							

Table 14-5756. MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P5_R0	R/W	0h	Claim bits for Partition 5 Reset Source: mod_g_rst_n

14.2.1.1.1.2.430 MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1 Register (Offset = 17104h) [reset = 0h]

Claim bits for Partition 5

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Table 14-5757. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 7104h**

Figure 14-1914. MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P5_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P5_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P5_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P5_R1							
R/W							
0h							

Table 14-5759. MAIN_CTRL_MMR_CFG0_CLAIMREG_P5_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P5_R1	R/W	0h	Claim bits for Partition 5 Reset Source: mod_g_rst_n

14.2.1.1.1.2.431 MAIN_CTRL_MMR_CFG0_RST_CTRL Register

1 MAIN_CTRL_MMR_CFG0_RST_CTRL Register (Offset = 18170h) [reset = 200FFh]

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Table 14-5760. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4301 8170h

Figure 14-1915. MAIN_CTRL_MMR_CFG0_RST_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td>RST_CTRL_MAIN_RESET_ISO_DONE_Z</td><td>RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z</td><td>RST_CTRL_DMSC_COLD_RESET_EN_Z</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RST_CTRL_SW_MAIN_POR</td><td colspan="4">RST_CTRL_SW_MAIN_WARMRST</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Fh</td><td colspan="4">Fh</td></tr>
</table>

Table 14-5762. MAIN_CTRL_MMR_CFG0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MAIN_RESET_ISO_DONE_Z	R/W	0h	Main Domain CPUs can set this bit to block warm reset in the main domain which is useful when the Main domain may be accessing Reset Source: main_chip1_rst_n
17	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z	R/W	1h	Deactivate Reset of Main by ESM Reset Source: main_chip1_rst_n
16	RST_CTRL_DMSC_COLD_RESET_EN_Z	R/W	0h	Deactivate Reset of Main by DMSC Reset Source: main_chip1_rst_n
15:8	RESERVED	NONE	0h	Reserved
7:4	RST_CTRL_SW_MAIN_POR	R/W	Fh	Causes Main Domain Power On Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n
3:0	RST_CTRL_SW_MAIN_WARMRST	R/W	Fh	Causes Main Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n

14.2.1.1.1.2.432 MAIN_CTRL_MMR_CFG0_RST_STAT Register

1 MAIN_CTRL_MMR_CFG0_RST_STAT Register (Offset = 18174h) [reset = 0h]

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Table 14-5763. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 8174h**

Figure 14-1916. MAIN_CTRL_MMR_CFG0_RST_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MCU_RESET_ISO_DONE_Z
NONE							R
0h							X

Table 14-5765. MAIN_CTRL_MMR_CFG0_RST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MCU_RESET_ISO_DONE_Z	R	X	is an outstanding warm reset request for the main domain. Once notified, MCU needs to finish any outstanding Reset Source: main_chip1_rst_n

14.2.1.1.1.2.433 MAIN_CTRL_MMR_CFG0_RST_SRC Register

1 MAIN_CTRL_MMR_CFG0_RST_SRC Register (Offset = 18178h) [reset = 0h]

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Table 14-5766. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4301 8178h

Figure 14-1917. MAIN_CTRL_MMR_CFG0_RST_SRC Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR	RST_SRC_MAIN_ESM_ERROR	RESERVED				RST_SRC_SW_MAIN_POR_FROM_MAIN	RST_SRC_SW_MAIN_POR_FROM_MCU
R	R	NONE				R	R
X	X	0h				X	X
23	22	21	20	19	18	17	16
RESERVED		RST_SRC_SW_MAIN_WARMRST_FROM_MAIN	RST_SRC_SW_MAIN_WARMRST_FROM_MCU	RESERVED			RST_SRC_SW_MCU_WARMRST
NONE		R	R	NONE			R
0h		X	X	0h			X
15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST	RST_SRC_COLD_OUT_RST	RESERVED			RST_SRC_DEBUG_RST
NONE		R	R	NONE			R
0h		X	X	0h			X
7	6	5	4	3	2	1	0
RESERVED			RST_SRC_THERMAL_RST	RESERVED	RST_SRC_MAIN_RESET_REQ	RESERVED	RST_SRC_MCU_RESET_PIN
NONE			R	NONE	R	NONE	R
0h			X	0h	X	0h	X

Table 14-5768. MAIN_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR	R	X	Reset Caused by MCU ESM Error Reset Source: main_chip1_rst_n
30	RST_SRC_MAIN_ESM_ERROR	R	X	Reset Caused by Main ESM Error Reset Source: main_chip1_rst_n
29:26	RESERVED	NONE	0h	Reserved
25	RST_SRC_SW_MAIN_POR_FROM_MAIN	R	X	Software Main Power On Reset From MAIN CTRL MMR Reset Source: main_chip1_rst_n
24	RST_SRC_SW_MAIN_POR_FROM_MCU	R	X	Software Main Power On Reset From MCU CTRL MMR Reset Source: main_chip1_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN	R	X	Software Main Warm Reset from MAIN CTRL MMR Reset Source: main_chip1_rst_n

Table 14-5768. MAIN_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	RST_SRC_SW_MAIN_WARMRST_FROM_MCU	R	X	Software Main Warm Reset From MCU CTRL MMR Reset Source: main_chip1_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST	R	X	Software Warm Reset Reset Source: main_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST	R	X	DMSC Warm Reset Reset Source: main_chip1_rst_n
12	RST_SRC_COLD_OUT_RST	R	X	DMSC Cold Reset Reset Source: main_chip1_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST	R	X	Debug Subsystem Initiated Reset Reset Source: main_chip1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST	R	X	Thermal Reset Reset Source: main_chip1_rst_n
3	RESERVED	NONE	0h	Reserved
2	RST_SRC_MAIN_RESET_REQ	R	X	Main Reset Pin Reset Source: main_chip1_rst_n
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN	R	X	Rest Caused by MCU Reset Pin Reset Source: main_chip1_rst_n

14.2.1.1.1.2.434 MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD Register

1 MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD Register (Offset = 1817Ch) [reset = 0h]

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Table 14-5769. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 817Ch**

Figure 14-1918. MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							

Table 14-5771. MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD	R	X	Magic Word Indicating Status of MCU Subsystem Boot Reset Source: main_chip1_rst_n

14.2.1.1.1.2.435 MAIN_CTRL_MMR_CFG0_LOCK6_KICK0 Register

1 MAIN_CTRL_MMR_CFG0_LOCK6_KICK0 Register (Offset = 19008h) [reset = 0h]

- KICK0 component

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Table 14-5772. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 9008h**

Figure 14-1919. MAIN_CTRL_MMR_CFG0_LOCK6_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0							
R/W							
0h							

Table 14-5774. MAIN_CTRL_MMR_CFG0_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.436 MAIN_CTRL_MMR_CFG0_LOCK6_KICK1 Register

1 MAIN_CTRL_MMR_CFG0_LOCK6_KICK1 Register (Offset = 1900Ch) [reset = 0h]

- KICK1 component

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Table 14-5775. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 900Ch**

Figure 14-1920. MAIN_CTRL_MMR_CFG0_LOCK6_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1							
R/W							
0h							

Table 14-5777. MAIN_CTRL_MMR_CFG0_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.437 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register (Offset = 19100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5778. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 9100h**

Figure 14-1921. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0_READONLY							
R							
0h							

Table 14-5780. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.438 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register (Offset = 19104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5781. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 9104h**

Figure 14-1922. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1_READONLY							
R							
0h							

Table 14-5783. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.439 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register (Offset = 19108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5784. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 9108h**

Figure 14-1923. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2_READONLY							
R							
0h							

Table 14-5786. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.440 MAIN_CTRL_MMR_CFG0_RST_CTRL_PROXY Register

1 MAIN_CTRL_MMR_CFG0_RST_CTRL_PROXY Register (Offset = 1A170h) [reset = 200FFh]

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Table 14-5787. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4301 A170h

Figure 14-1924. MAIN_CTRL_MMR_CFG0_RST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					RST_CTRL_MAIN_RESET_ISO_DONE_Z_PROXY	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z_PROXY	RST_CTRL_DMSC_COLD_RESET_EN_Z_PROXY
NONE					R/W	R/W	R/W
0h					0h	1h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RST_CTRL_SW_MAIN_POR_PROXY				RST_CTRL_SW_MAIN_WARMRST_PROXY			
R/W				R/W			
Fh				Fh			

Table 14-5789. MAIN_CTRL_MMR_CFG0_RST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MAIN_RESET_ISO_DONE_Z_PROXY	R/W	0h	Main Domain CPUs can set this bit to block warm reset in the main domain which is useful when the Main domain may be accessing Reset Source: main_chip1_rst_n
17	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z_PROXY	R/W	1h	Deactivate Reset of Main by ESM Reset Source: main_chip1_rst_n
16	RST_CTRL_DMSC_COLD_RESET_EN_Z_PROXY	R/W	0h	Deactivate Reset of Main by DMSC Reset Source: main_chip1_rst_n
15:8	RESERVED	NONE	0h	Reserved
7:4	RST_CTRL_SW_MAIN_POR_PROXY	R/W	Fh	Causes Main Domain Power On Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n
3:0	RST_CTRL_SW_MAIN_WARMRST_PROXY	R/W	Fh	Causes Main Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111 Reset Source: main_chip1_rst_n

14.2.1.1.1.2.441 MAIN_CTRL_MMR_CFG0_RST_STAT_PROXY Register

1 MAIN_CTRL_MMR_CFG0_RST_STAT_PROXY Register (Offset = 1A174h) [reset = 0h]

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Table 14-5790. Instance Table

Instance Name	Physical Address
CTRL_MMR0	4301 A174h

Figure 14-1925. MAIN_CTRL_MMR_CFG0_RST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RST_STAT_MCU_RESET_ISO_DONE_Z_PROXY
NONE							R
0h							X

Table 14-5792. MAIN_CTRL_MMR_CFG0_RST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MCU_RESET_ISO_DONE_Z_PROXY	R	X	is an outstanding warm reset request for the main domain. Once notified, MCU needs to finish any outstanding Reset Source: main_chip1_rst_n

14.2.1.1.1.2.442 MAIN_CTRL_MMR_CFG0_RST_SRC_PROXY Register

1 MAIN_CTRL_MMR_CFG0_RST_SRC_PROXY Register (Offset = 1A178h) [reset = 0h]

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Table 14-5793. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 A178h**

Figure 14-1926. MAIN_CTRL_MMR_CFG0_RST_SRC_PROXY Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR_PROXY	RST_SRC_MAIN_ESM_ERROR_PROXY	RESERVED				RST_SRC_SW_MAIN_POR_FROM_MAIN_PROXY	RST_SRC_SW_MAIN_POR_FROM_MCU_PROXY
R	R	NONE				R	R
X	X	0h				X	X
23	22	21	20	19	18	17	16
RESERVED		RST_SRC_SW_MAIN_WARMRST_FROM_MAIN_PROXY	RST_SRC_SW_MAIN_WARMRST_FROM_MCU_PROXY	RESERVED			RST_SRC_SW_MCU_WARMRST_PROXY
NONE		R	R	NONE			R
0h		X	X	0h			X
15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST_PROXY	RST_SRC_COLD_OUT_RST_PROXY	RESERVED			RST_SRC_DEBUG_RST_PROXY
NONE		R	R	NONE			R
0h		X	X	0h			X
7	6	5	4	3	2	1	0
RESERVED			RST_SRC_THERMAL_RST_PROXY	RESERVED	RST_SRC_MAIN_RESET_REQ_PROXY	RESERVED	RST_SRC_MCU_RESET_PIN_PROXY
NONE			R	NONE	R	NONE	R
0h			X	0h	X	0h	X

Table 14-5795. MAIN_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR_PROXY	R	X	Reset Caused by MCU ESM Error Reset Source: main_chip1_rst_n
30	RST_SRC_MAIN_ESM_ERROR_PROXY	R	X	Reset Caused by Main ESM Error Reset Source: main_chip1_rst_n
29:26	RESERVED	NONE	0h	Reserved
25	RST_SRC_SW_MAIN_POR_FROM_MAIN_PROXY	R	X	Software Main Power On Reset From MAIN CTRL MMR Reset Source: main_chip1_rst_n
24	RST_SRC_SW_MAIN_POR_FROM_MCU_PROXY	R	X	Software Main Power On Reset From MCU CTRL MMR Reset Source: main_chip1_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-5795. MAIN_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN_PROXY	R	X	Software Main Warm Reset from MAIN CTRL MMR Reset Source: main_chip1_rst_n
20	RST_SRC_SW_MAIN_WARMRST_FROM_MCU_PROXY	R	X	Software Main Warm Reset From MCU CTRL MMR Reset Source: main_chip1_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST_PROXY	R	X	Software Warm Reset Reset Source: main_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST_PROXY	R	X	DMSC Warm Reset Reset Source: main_chip1_rst_n
12	RST_SRC_COLD_OUT_RST_PROXY	R	X	DMSC Cold Reset Reset Source: main_chip1_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST_PROXY	R	X	Debug Subsystem Initiated Reset Reset Source: main_chip1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST_PROXY	R	X	Thermal Reset Reset Source: main_chip1_rst_n
3	RESERVED	NONE	0h	Reserved
2	RST_SRC_MAIN_RESET_REQ_PROXY	R	X	Main Reset Pin Reset Source: main_chip1_rst_n
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN_PROXY	R	X	Rest Caused by MCU Reset Pin Reset Source: main_chip1_rst_n

14.2.1.1.1.2.443 MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register

1 MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register (Offset = 1A17Ch) [reset = 0h]

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Table 14-5796. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 A17Ch**

Figure 14-1927. MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							

Table 14-5798. MAIN_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY	R	X	Magic Word Indicating Status of MCU Subsystem Boot Reset Source: main_chip1_rst_n

14.2.1.1.1.2.444 MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register (Offset = 1B008h) [reset = 0h]

- KICK0 component

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Table 14-5799. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 B008h**

Figure 14-1928. MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0_PROXY							
R/W							
0h							

Table 14-5801. MAIN_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.445 MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register

1 MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register (Offset = 1B00Ch) [reset = 0h]

- KICK1 component

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Table 14-5802. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 B00Ch**

Figure 14-1929. MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1_PROXY							
R/W							
0h							

Table 14-5804. MAIN_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.446 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register (Offset = 1B100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5805. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 B100h**

Figure 14-1930. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0							
R/W							
0h							

Table 14-5807. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.447 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register (Offset = 1B104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5808. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 B104h**

Figure 14-1931. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1							
R/W							
0h							

Table 14-5810. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.448 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register

1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register (Offset = 1B108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5811. Instance Table

Instance Name	Physical Address
CTRL_MMR0	**4301 B108h**

Figure 14-1932. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2							
R/W							
0h							

Table 14-5813. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2 mcu_ctrl_mmr

mcu_ctrl_mmr

14.2.1.1.2.1 mcu_ctrl_mmr Summaries

mcu_ctrl_mmr Summaries

Table 14-5814. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
0h	32	MCU_CTRL_MMR_CFG0_PID	0450 0000h
8h	32	MCU_CTRL_MMR_CFG0_MMR_CFG1	0450 0008h
1008h	32	MCU_CTRL_MMR_CFG0_LOCK0_KICK0	0450 1008h
100Ch	32	MCU_CTRL_MMR_CFG0_LOCK0_KICK1	0450 100Ch
1010h	32	MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS	0450 1010h
1014h	32	MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	0450 1014h
1018h	32	MCU_CTRL_MMR_CFG0_INTR_ENABLE	0450 1018h
101Ch	32	MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	0450 101Ch
1020h	32	MCU_CTRL_MMR_CFG0_EOI	0450 1020h
1024h	32	MCU_CTRL_MMR_CFG0_FAULT_ADDRESS	0450 1024h
1028h	32	MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	0450 1028h
102Ch	32	MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	0450 102Ch
1030h	32	MCU_CTRL_MMR_CFG0_FAULT_CLEAR	0450 1030h
1100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	0450 1100h
2000h	32	MCU_CTRL_MMR_CFG0_PID_PROXY	0450 2000h
2008h	32	MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY	0450 2008h
3008h	32	MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	0450 3008h
300Ch	32	MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	0450 300Ch
3010h	32	MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	0450 3010h
3014h	32	MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	0450 3014h
3018h	32	MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	0450 3018h
301Ch	32	MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	0450 301Ch
3020h	32	MCU_CTRL_MMR_CFG0_EOI_PROXY	0450 3020h
3024h	32	MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	0450 3024h
3028h	32	MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	0450 3028h
302Ch	32	MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	0450 302Ch
3030h	32	MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	0450 3030h
3100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0	0450 3100h
4084h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1	0450 4084h
4088h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2	0450 4088h
408Ch	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3	0450 408Ch
4090h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4	0450 4090h
4094h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5	0450 4094h
4098h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6	0450 4098h

Table 14-5814. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
40A0h	32	MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM	0450 40A0h
40B0h	32	MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT	0450 40B0h
4204h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL	0450 4204h
420Ch	32	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL	0450 420Ch
42E0h	32	MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL	0450 42E0h
4600h	32	MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL	0450 4600h
5008h	32	MCU_CTRL_MMR_CFG0_LOCK1_KICK0	0450 5008h
500Ch	32	MCU_CTRL_MMR_CFG0_LOCK1_KICK1	0450 500Ch
5100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	0450 5100h
5104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	0450 5104h
5108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY	0450 5108h
510Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	0450 510Ch
5110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	0450 5110h
5114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY	0450 5114h
5118h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY	0450 5118h
511Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY	0450 511Ch
5120h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY	0450 5120h
5124h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY	0450 5124h
5128h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY	0450 5128h
512Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY	0450 512Ch
5130h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY	0450 5130h
6084h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY	0450 6084h
6088h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY	0450 6088h
608Ch	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY	0450 608Ch
6090h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY	0450 6090h
6094h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY	0450 6094h
6098h	32	MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY	0450 6098h
60A0h	32	MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY	0450 60A0h
60B0h	32	MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY	0450 60B0h
6204h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY	0450 6204h
620Ch	32	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY	0450 620Ch
62E0h	32	MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY	0450 62E0h
6600h	32	MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL_PROXY	0450 6600h
7008h	32	MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	0450 7008h
700Ch	32	MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	0450 700Ch

Table 14-5814. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
7100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0	0450 7100h
7104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1	0450 7104h
7108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2	0450 7108h
710Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3	0450 710Ch
7110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4	0450 7110h
7114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5	0450 7114h
7118h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6	0450 7118h
711Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7	0450 711Ch
7120h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8	0450 7120h
7124h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9	0450 7124h
7128h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10	0450 7128h
712Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11	0450 712Ch
7130h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12	0450 7130h
8000h	32	MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL	0450 8000h
8010h	32	MCU_CTRL_MMR_CFG0_HFOSC0_CTRL	0450 8010h
8018h	32	MCU_CTRL_MMR_CFG0_HFOSC0_TRIM	0450 8018h
8024h	32	MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM	0450 8024h
8030h	32	MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL	0450 8030h
8040h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL	0450 8040h
8044h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK	0450 8044h
8050h	32	MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL	0450 8050h
8060h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL	0450 8060h
8064h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL	0450 8064h
8068h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL	0450 8068h
806Ch	32	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL	0450 806Ch
80A0h	32	MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL	0450 80A0h
80A4h	32	MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL	0450 80A4h
80B0h	32	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL	0450 80B0h
80D0h	32	MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL	0450 80D0h
9008h	32	MCU_CTRL_MMR_CFG0_LOCK2_KICK0	0450 9008h
900Ch	32	MCU_CTRL_MMR_CFG0_LOCK2_KICK1	0450 900Ch
9100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY	0450 9100h
9104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY	0450 9104h
A000h	32	MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY	0450 A000h
A010h	32	MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY	0450 A010h
A018h	32	MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY	0450 A018h
A024h	32	MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY	0450 A024h
A030h	32	MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY	0450 A030h
A040h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL_PROXY	0450 A040h
A044h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK_PROXY	0450 A044h
A050h	32	MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY	0450 A050h

Table 14-5814. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
A060h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY	0450 A060h
A064h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY	0450 A064h
A068h	32	MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY	0450 A068h
A06Ch	32	MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY	0450 A06Ch
A0A0h	32	MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY	0450 A0A0h
A0A4h	32	MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY	0450 A0A4h
A0B0h	32	MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY	0450 A0B0h
A0D0h	32	MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY	0450 A0D0h
B008h	32	MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY	0450 B008h
B00Ch	32	MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY	0450 B00Ch
B100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0	0450 B100h
B104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1	0450 B104h
C020h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL	0450 C020h
C024h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT	0450 C024h
C028h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0	0450 C028h
C02Ch	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1	0450 C02Ch
C030h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0	0450 C030h
C034h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1	0450 C034h
C038h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT	0450 C038h
C03Ch	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR	0450 C03Ch
D008h	32	MCU_CTRL_MMR_CFG0_LOCK3_KICK0	0450 D008h
D00Ch	32	MCU_CTRL_MMR_CFG0_LOCK3_KICK1	0450 D00Ch
D100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY	0450 D100h
E020h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL_PROXY	0450 E020h
E024h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT_PROXY	0450 E024h
E028h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0_PROXY	0450 E028h
E02Ch	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1_PROXY	0450 E02Ch
E030h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0_PROXY	0450 E030h
E034h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1_PROXY	0450 E034h
E038h	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT_PROXY	0450 E038h
E03Ch	32	MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR_PROXY	0450 E03Ch
F008h	32	MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY	0450 F008h

Table 14-5814. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
F00Ch	32	MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY	0450 F00Ch
F100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0	0450 F100h
11008h	32	MCU_CTRL_MMR_CFG0_LOCK4_KICK0	0451 1008h
1100Ch	32	MCU_CTRL_MMR_CFG0_LOCK4_KICK1	0451 100Ch
11100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY	0451 1100h
11104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY	0451 1104h
11108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY	0451 1108h
1110Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY	0451 110Ch
11110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY	0451 1110h
11114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY	0451 1114h
11118h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY	0451 1118h
1111Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY	0451 111Ch
11120h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY	0451 1120h
11124h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY	0451 1124h
11128h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY	0451 1128h
1112Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY	0451 112Ch
11130h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY	0451 1130h
11134h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY	0451 1134h
11138h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY	0451 1138h
13008h	32	MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY	0451 3008h
1300Ch	32	MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY	0451 300Ch
13100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0	0451 3100h
13104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1	0451 3104h
13108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2	0451 3108h
1310Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3	0451 310Ch
13110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4	0451 3110h
13114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5	0451 3114h
13118h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6	0451 3118h
1311Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7	0451 311Ch
13120h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8	0451 3120h
13124h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9	0451 3124h
13128h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10	0451 3128h
1312Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11	0451 312Ch
13130h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12	0451 3130h

Table 14-5814. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
13134h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13	0451 3134h
13138h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14	0451 3138h
18000h	32	MCU_CTRL_MMR_CFG0_POR_CTRL	0451 8000h
18004h	32	MCU_CTRL_MMR_CFG0_POR_STAT	0451 8004h
18100h	32	MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL	0451 8100h
18110h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL	0451 8110h
18114h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL	0451 8114h
18118h	32	MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL	0451 8118h
1811Ch	32	MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL	0451 811Ch
18120h	32	MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL	0451 8120h
18124h	32	MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL	0451 8124h
18128h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL	0451 8128h
1812Ch	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL	0451 812Ch
18130h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL	0451 8130h
18134h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL	0451 8134h
18138h	32	MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL	0451 8138h
1813Ch	32	MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL	0451 813Ch
18140h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL	0451 8140h
18144h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL	0451 8144h
18148h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL	0451 8148h
1814Ch	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL	0451 814Ch
18150h	32	MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL	0451 8150h
18154h	32	MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL	0451 8154h
18160h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL	0451 8160h
18170h	32	MCU_CTRL_MMR_CFG0_RST_CTRL	0451 8170h
18174h	32	MCU_CTRL_MMR_CFG0_RST_STAT	0451 8174h
18178h	32	MCU_CTRL_MMR_CFG0_RST_SRC	0451 8178h
1817Ch	32	MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD	0451 817Ch
18180h	32	MCU_CTRL_MMR_CFG0_ISO_CTRL	0451 8180h
18190h	32	MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL	0451 8190h
181B0h	32	MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT	0451 81B0h
18200h	32	MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL	0451 8200h
18208h	32	MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL	0451 8208h
18284h	32	MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL	0451 8284h
18288h	32	MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0	0451 8288h
19008h	32	MCU_CTRL_MMR_CFG0_LOCK6_KICK0	0451 9008h
1900Ch	32	MCU_CTRL_MMR_CFG0_LOCK6_KICK1	0451 900Ch

Table 14-5814. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
19100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY	0451 9100h
19104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY	0451 9104h
19108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY	0451 9108h
1910Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY	0451 910Ch
19110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY	0451 9110h
19114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY	0451 9114h
1A000h	32	MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY	0451 A000h
1A004h	32	MCU_CTRL_MMR_CFG0_POR_STAT_PROXY	0451 A004h
1A100h	32	MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY	0451 A100h
1A110h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY	0451 A110h
1A114h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY	0451 A114h
1A118h	32	MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY	0451 A118h
1A11Ch	32	MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY	0451 A11Ch
1A120h	32	MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY	0451 A120h
1A124h	32	MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY	0451 A124h
1A128h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL_PROXY	0451 A128h
1A12Ch	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL_PROXY	0451 A12Ch
1A130h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL_PROXY	0451 A130h
1A134h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL_PROXY	0451 A134h
1A138h	32	MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY	0451 A138h
1A13Ch	32	MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY	0451 A13Ch
1A140h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY	0451 A140h
1A144h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY	0451 A144h
1A148h	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY	0451 A148h
1A14Ch	32	MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY	0451 A14Ch
1A150h	32	MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY	0451 A150h
1A154h	32	MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY	0451 A154h

Table 14-5814. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
1A160h	32	MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY	0451 A160h
1A170h	32	MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY	0451 A170h
1A174h	32	MCU_CTRL_MMR_CFG0_RST_STAT_PROXY	0451 A174h
1A178h	32	MCU_CTRL_MMR_CFG0_RST_SRC_PROXY	0451 A178h
1A17Ch	32	MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY	0451 A17Ch
1A180h	32	MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY	0451 A180h
1A190h	32	MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY	0451 A190h
1A1B0h	32	MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY	0451 A1B0h
1A200h	32	MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY	0451 A200h
1A208h	32	MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY	0451 A208h
1A284h	32	MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL_PROXY	0451 A284h
1A288h	32	MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0_PROXY	0451 A288h
1B008h	32	MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY	0451 B008h
1B00Ch	32	MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY	0451 B00Ch
1B100h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0	0451 B100h
1B104h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1	0451 B104h
1B108h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2	0451 B108h
1B10Ch	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3	0451 B10Ch
1B110h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4	0451 B110h
1B114h	32	MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5	0451 B114h

14.2.1.1.2.2 mcu_ctrl_mmr Registers

mcu_ctrl_mmr Registers

14.2.1.1.2.2.1 MCU_CTRL_MMR_CFG0_PID Register

1 MCU_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800213h]

PID register

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Table 14-5815. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 0000h**

Figure 14-1933. MCU_CTRL_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM		PID_MINOR					
R		R					
0h		13h					

Table 14-5817. MCU_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	13h	Reset Source: mod_g_rst_n

14.2.1.1.2.2.2 MCU_CTRL_MMR_CFG0_MMR_CFG1 Register

1 MCU_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000DFh]

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Table 14-5818. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 0008h**

Figure 14-1934. MCU_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
DFh							

Table 14-5820. MCU_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing actived Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	DFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.2.2.3 MCU_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-5821. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1008h**

Figure 14-1935. MCU_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-5823. MCU_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.4 MCU_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-5824. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 100Ch**

Figure 14-1936. MCU_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-5826. MCU_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.5 MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-5827. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1010h**

Figure 14-1937. MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>PROXY_ERR</td><td>KICK_ERR</td><td>ADDR_ERR</td><td>PROT_ERR</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-5829. MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.6 MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-5830. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1014h

Figure 14-1938. MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5832. MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.7 MCU_CTRL_MMR_CFG0_INTR_ENABLE Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-5833. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1018h**

Figure 14-1939. MCU_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5835. MCU_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.8 MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-5836. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 101Ch**

Figure 14-1940. MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5838. MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.9 MCU_CTRL_MMR_CFG0_EOI Register

1 MCU_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-5839. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1020h**

Figure 14-1941. MCU_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-5841. MCU_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.2.2.10 MCU_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 MCU_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-5842. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1024h**

Figure 14-1942. MCU_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_ADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FAULT_ADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_ADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5844. MCU_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.2.2.11 MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-5845. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1028h**

Figure 14-1943. MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-5847. MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.2.2.12 MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-5848. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 102Ch**

Figure 14-1944. MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 14-5850. MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.2.2.13 MCU_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 MCU_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-5851. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1030h**

Figure 14-1945. MCU_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-5853. MCU_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.14 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5854. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 1100h**

Figure 14-1946. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-5856. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.15 MCU_CTRL_MMR_CFG0_PID_PROXY Register

1 MCU_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800213h]

PID register

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Table 14-5857. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 2000h**

Figure 14-1947. MCU_CTRL_MMR_CFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16_PROXY							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		13h					

Table 14-5859. MCU_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	13h	Reset Source: mod_g_rst_n

14.2.1.1.2.2.16 MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000DFh]

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Table 14-5860. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 2008h**

Figure 14-1948. MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS_PROXY							
R							
DFh							

Table 14-5862. MCU_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing actived Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	DFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.2.2.17 MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-5863. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3008h**

Figure 14-1949. MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-5865. MCU_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.18 MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-5866. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 300Ch**

Figure 14-1950. MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-5868. MCU_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.19 MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-5869. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3010h**

Figure 14-1951. MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5871. MCU_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.20 MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-5872. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3014h**

Figure 14-1952. MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5874. MCU_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.21 MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-5875. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3018h**

Figure 14-1953. MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5877. MCU_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.22 MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-5878. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 301Ch**

Figure 14-1954. MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5880. MCU_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.23 MCU_CTRL_MMR_CFG0_EOI_PROXY Register

1 MCU_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-5881. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3020h**

Figure 14-1955. MCU_CTRL_MMR_CFG0_EOI_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_VECTOR_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5883. MCU_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.2.2.24 MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-5884. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3024h**

Figure 14-1956. MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-5886. MCU_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.2.2.25 MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-5887. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3028h**

Figure 14-1957. MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-5889. MCU_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.2.2.26 MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-5890. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 302Ch**

Figure 14-1958. MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-5892. MCU_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.2.2.27 MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-5893. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3030h**

Figure 14-1959. MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-5895. MCU_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.28 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5896. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 3100h**

Figure 14-1960. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-5898. MCU_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.29 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 Register (Offset = 4084h) [reset = 0h]

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Table 14-5899. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4084h**

Figure 14-1961. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG1_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-5901. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG1_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel1 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.30 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 Register (Offset = 4088h) [reset = 0h]

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Table 14-5902. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4088h**

Figure 14-1962. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG2_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-5904. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG2_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel2 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.31 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 Register (Offset = 408Ch) [reset = 0h]

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Table 14-5905. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 408Ch**

Figure 14-1963. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG3_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-5907. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG3_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel3 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.32 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 Register (Offset = 4090h) [reset = 0h]

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Table 14-5908. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4090h**

Figure 14-1964. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG4_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-5910. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG4_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel4 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.33 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 Register (Offset = 4094h) [reset = 0h]

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Table 14-5911. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4094h**

Figure 14-1965. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG5_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-5913. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG5_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel5 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.34 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 Register (Offset = 4098h) [reset = 0h]

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Table 14-5914. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4098h**

Figure 14-1966. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG6_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-5916. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG6_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with debounce_sel6 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.35 MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM Register

1 MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM Register (Offset = 40A0h) [reset = 0h]

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Table 14-5917. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 40A0h**

Figure 14-1967. MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TEMP_DIODE_TRIM_TRIM					
NONE		R					
0h		X					
7	6	5	4	3	2	1	0
TEMP_DIODE_TRIM_TRIM							
R							
X							

Table 14-5919. MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TEMP_DIODE_TRIM_TRIM	R	X	Sets the diode non-ideality factor (n), starting from 100th place decimal and going down Reset Source: mod_por_rst_n

14.2.1.1.2.2.36 MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Register

1 MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Register (Offset = 40B0h) [reset = 0h]

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Table 14-5920. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 40B0h**

Figure 14-1968. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						MAIN_GPMC	RESERVED
NONE						R	NONE
0h						X	0h
15	14	13	12	11	10	9	8
RESERVED		MAIN_PRG1	MAIN_PRG0	RESERVED	MAIN_MMC1	RESERVED	MAIN_GEN
NONE		R	R	NONE	R	NONE	R
0h		X	X	0h	X	0h	X
7	6	5	4	3	2	1	0
RESERVED						MCU_FLASH	MCU_GEN
NONE						R	R
0h						X	X

Table 14-5922. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	MAIN_GPMC	R	X	Indicates the voltage for the GPMC I/O group (VDDSHV3) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
16:14	RESERVED	NONE	0h	Reserved
13	MAIN_PRG1	R	X	Indicates the voltage for the PRG1 I/O group (VDDSHV1) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
12	MAIN_PRG0	R	X	Indicates the voltage for the PRG0 I/O group (VDDSHV2) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
11	RESERVED	NONE	0h	Reserved

Table 14-5922. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MAIN_MMC1	R	X	Indicates the voltage for the MMC1 I/O group (VDDSHV5) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
9	RESERVED	NONE	0h	Reserved
8	MAIN_GEN	R	X	Indicates the voltage for the General I/O group (VDDSHV0) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
7:2	RESERVED	NONE	0h	Reserved
1	MCU_FLASH	R	X	Indicates the voltage for the Flash I/O group (VDDSHV4) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
0	MCU_GEN	R	X	Indicates the voltage for the MCU General I/O group (VDDSHV0_MCU) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED

14.2.1.1.2.2.37 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL Register (Offset = 4204h) [reset = 0h]

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Table 14-5923. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4204h**

Figure 14-1969. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCU_TIMER1_CTRL_CASCADE_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5925. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_TIMER1_CTRL_CASCADE_EN	R/W	0h	Actives cascading of TIMER1 to TIMER0 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.38 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL Register (Offset = 420Ch) [reset = 0h]

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Table 14-5926. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 420Ch**

Figure 14-1970. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MCU_TIMER3_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5928. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_TIMER3_CTRL_CASCADE_EN	R/W	0h	Actives cascading of TIMER3 to TIMER2 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.39 MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL Register (Offset = 42E0h) [reset = 0h]

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Table 14-5929. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 42E0h**

Figure 14-1971. MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCU_I2C0_CTRL_HS_MCS_EN
NONE							R/W
0h							0h

Table 14-5931. MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_I2C0_CTRL_HS_MCS_EN	R/W	0h	HS Mode controller current source active. Reset Source: mod_g_rst_n

14.2.1.1.2.2.40 MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL Register (Offset = 4600h) [reset = 0h]

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Table 14-5932. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 4600h**

Figure 14-1972. MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL Name Register

31	30	29	28	27	26	25	24
MCU_MTOG_CTRL_IDLE_STAT	RESERVED						
R	NONE						
X	0h						
23	22	21	20	19	18	17	16
MCU_MTOG_CTRL_FORCE_TIMEOUT							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_MTOG_CTRL_TIMEOUT_EN	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED					MCU_MTOG_CTRL_TIMEOUT_VAL		
NONE					R/W		
0h					0h		

Table 14-5934. MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_MTOG_CTRL_IDLE_STAT	R	X	Idle Status: Reset Source: mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	MCU_MTOG_CTRL_FORCE_TIMEOUT	R/W	0h	Force Timout Reset Source: mod_g_rst_n
15	MCU_MTOG_CTRL_TIMEOUT_EN	R/W	0h	Timeout Active Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved
2:0	MCU_MTOG_CTRL_TIMEOUT_VAL	R/W	0h	Gasket Timeout Value Reset Source: mod_g_rst_n

14.2.1.1.2.2.41 MCU_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-5935. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5008h**

Figure 14-1973. MCU_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-5937. MCU_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.42 MCU_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-5938. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 500Ch**

Figure 14-1974. MCU_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-5940. MCU_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.43 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5941. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5100h**

Figure 14-1975. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-5943. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.44 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5944. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5104h**

Figure 14-1976. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-5946. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.45 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5947. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5108h**

Figure 14-1977. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-5949. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.46 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5950. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 510Ch**

Figure 14-1978. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-5952. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.47 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5953. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5110h**

Figure 14-1979. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-5955. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.48 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register (Offset = 5114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5956. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5114h**

Figure 14-1980. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5_READONLY							
R							
0h							

Table 14-5958. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.49 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register (Offset = 5118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5959. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5118h**

Figure 14-1981. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6_READONLY							
R							
0h							

Table 14-5961. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.50 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register (Offset = 511Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5962. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 511Ch**

Figure 14-1982. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7_READONLY							
R							
0h							

Table 14-5964. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.51 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register (Offset = 5120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5965. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5120h**

Figure 14-1983. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8_READONLY							
R							
0h							

Table 14-5967. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.52 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register (Offset = 5124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5968. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5124h**

Figure 14-1984. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9_READONLY							
R							
0h							

Table 14-5970. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.53 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register (Offset = 5128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5971. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5128h**

Figure 14-1985. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10_READONLY							
R							
0h							

Table 14-5973. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.54 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register (Offset = 512Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5974. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 512Ch**

Figure 14-1986. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11_READONLY							
R							
0h							

Table 14-5976. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.55 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register (Offset = 5130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5977. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 5130h**

Figure 14-1987. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12_READONLY							
R							
0h							

Table 14-5979. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.56 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY Register (Offset = 6084h) [reset = 0h]

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Table 14-5980. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6084h**

Figure 14-1988. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG1_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5982. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG1_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel1 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.57 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY Register (Offset = 6088h) [reset = 0h]

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Table 14-5983. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6088h**

Figure 14-1989. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		DBOUNCE_CFG2_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5985. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG2_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel2 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.58 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY Register (Offset = 608Ch) [reset = 0h]

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Table 14-5986. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 608Ch**

Figure 14-1990. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG3_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5988. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG3_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel3 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.59 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY Register (Offset = 6090h) [reset = 0h]

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Table 14-5989. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6090h**

Figure 14-1991. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">DBOUNCE_CFG4_DB_CFG_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-5991. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG4_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel4 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.60 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY Register (Offset = 6094h) [reset = 0h]

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Table 14-5992. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6094h**

Figure 14-1992. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG5_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5994. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG5_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel5 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.61 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY Register

1 MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY Register (Offset = 6098h) [reset = 0h]

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Table 14-5995. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6098h**

Figure 14-1993. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG6_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5997. MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	DBOUNCE_CFG6_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with debounce_sel6 actived. Reset Source: mod_por_rst_n

14.2.1.1.2.2.62 MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY Register

1 MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY Register (Offset = 60A0h) [reset = 0h]

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Table 14-5998. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 60A0h**

Figure 14-1994. MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TEMP_DIODE_TRIM_TRIM_PROXY					
NONE		R					
0h		X					
7	6	5	4	3	2	1	0
TEMP_DIODE_TRIM_TRIM_PROXY							
R							
X							

Table 14-6000. MCU_CTRL_MMR_CFG0_TEMP_DIODE_TRIM_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TEMP_DIODE_TRIM_TRIM_PROXY	R	X	Sets the diode non-ideality factor (n), starting from 100th place decimal and going down Reset Source: mod_por_rst_n

14.2.1.1.2.2.63 MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Register (Offset = 60B0h) [reset = 0h]

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Table 14-6001. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 60B0h**

Figure 14-1995. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						MAIN_GPMC_PROXY	RESERVED
NONE						R	NONE
0h						X	0h
15	14	13	12	11	10	9	8
RESERVED		MAIN_PRG1_PROXY	MAIN_PRG0_PROXY	RESERVED	MAIN_MMC1_PROXY	RESERVED	MAIN_GEN_PROXY
NONE		R	R	NONE	R	NONE	R
0h		X	X	0h	X	0h	X
7	6	5	4	3	2	1	0
RESERVED						MCU_FLASH_PROXY	MCU_GEN_PROXY
NONE						R	R
0h						X	X

Table 14-6003. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	MAIN_GPMC_PROXY	R	X	Indicates the voltage for the GPMC I/O group (VDDSHV3) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
16:14	RESERVED	NONE	0h	Reserved
13	MAIN_PRG1_PROXY	R	X	Indicates the voltage for the PRG1 I/O group (VDDSHV1) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
12	MAIN_PRG0_PROXY	R	X	Indicates the voltage for the PRG0 I/O group (VDDSHV2) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED

Table 14-6003. MCU_CTRL_MMR_CFG0_IO_VOLTAGE_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RESERVED	NONE	0h	Reserved
10	MAIN_MMC1_PROXY	R	X	Indicates the voltage for the MMC1 I/O group (VDDSHV5) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
9	RESERVED	NONE	0h	Reserved
8	MAIN_GEN_PROXY	R	X	Indicates the voltage for the General I/O group (VDDSHV0) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
7:2	RESERVED	NONE	0h	Reserved
1	MCU_FLASH_PROXY	R	X	Indicates the voltage for the Flash I/O group (VDDSHV4) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED
0	MCU_GEN_PROXY	R	X	Indicates the voltage for the MCU General I/O group (VDDSHV0_MCU) Reset Source: mod_por_rst_n 0 IOGROUP_3P3V 1 IOGROUP_1P8V OTHER RESERVED

14.2.1.1.2.2.64 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY Register (Offset = 6204h) [reset = 0h]

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Table 14-6004. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6204h**

Figure 14-1996. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							MCU_TIMER1_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-6006. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_TIMER1_CTRL_CASCADE_EN_PROXY	R/W	0h	Actives cascading of TIMER1 to TIMER0 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.65 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY Register (Offset = 620Ch) [reset = 0h]

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Table 14-6007. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 620Ch**

Figure 14-1997. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCU_TIMER3_CTRL_CASCADE_EN_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6009. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_TIMER3_CTRL_CASCADE_EN_PROXY	R/W	0h	Actives cascading of TIMER3 to TIMER2 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.66 MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY Register (Offset = 62E0h) [reset = 0h]

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Table 14-6010. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 62E0h**

Figure 14-1998. MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCU_I2C0_CTRL_HS_MCS_EN_PROXY
NONE							R/W
0h							0h

Table 14-6012. MCU_CTRL_MMR_CFG0_MCU_I2C0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_I2C0_CTRL_HS_MCS_EN_PROXY	R/W	0h	HS Mode controller current source active. Reset Source: mod_g_rst_n

14.2.1.1.2.2.67 MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL_PROXY Register (Offset = 6600h) [reset = 0h]

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Table 14-6013. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 6600h**

Figure 14-1999. MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_MTOG_CTRL_IDLE_STAT_PROXY	RESERVED						
R	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MCU_MTOG_CTRL_FORCE_TIMEOUT_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_MTOG_CTRL_TIMEOUT_EN_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MCU_MTOG_CTRL_TIMEOUT_VAL_PROXY		
NONE					R/W		
0h					0h		

Table 14-6015. MCU_CTRL_MMR_CFG0_MCU_MTOG_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_MTOG_CTRL_IDLE_STAT_PROXY	R	X	Idle Status: Reset Source: mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	MCU_MTOG_CTRL_FORCE_TIMEOUT_PROXY	R/W	0h	Force Timout Reset Source: mod_g_rst_n
15	MCU_MTOG_CTRL_TIMEOUT_EN_PROXY	R/W	0h	Timeout Active Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved
2:0	MCU_MTOG_CTRL_TIMEOUT_VAL_PROXY	R/W	0h	Gasket Timeout Value Reset Source: mod_g_rst_n

14.2.1.1.2.2.68 MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-6016. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7008h**

Figure 14-2000. MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-6018. MCU_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.69 MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-6019. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 700Ch**

Figure 14-2001. MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-6021. MCU_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.70 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6022. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7100h**

Figure 14-2002. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6024. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.71 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6025. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7104h**

Figure 14-2003. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6027. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.72 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6028. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7108h**

Figure 14-2004. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-6030. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.73 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-6031. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 710Ch**

Figure 14-2005. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-6033. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.74 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6034. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7110h**

Figure 14-2006. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-6036. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.75 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6037. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7114h**

Figure 14-2007. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-6039. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.76 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register (Offset = 7118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6040. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7118h**

Figure 14-2008. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6							
R/W							
0h							

Table 14-6042. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.77 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register (Offset = 711Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-6043. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 711Ch**

Figure 14-2009. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7							
R/W							
0h							

Table 14-6045. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.78 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register (Offset = 7120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6046. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7120h**

Figure 14-2010. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8							
R/W							
0h							

Table 14-6048. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.79 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register (Offset = 7124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6049. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7124h**

Figure 14-2011. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9							
R/W							
0h							

Table 14-6051. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.80 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register (Offset = 7128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6052. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7128h**

Figure 14-2012. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10							
R/W							
0h							

Table 14-6054. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.81 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register (Offset = 712Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-6055. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 712Ch**

Figure 14-2013. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11							
R/W							
0h							

Table 14-6057. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.82 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register (Offset = 7130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6058. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 7130h**

Figure 14-2014. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12							
R/W							
0h							

Table 14-6060. MCU_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.83 MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Register (Offset = 8000h) [reset = 0h]

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Table 14-6061. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8000h**

Figure 14-2015. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							MCU_OBSCLK_CTRL_OUT_MUX_SEL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							MCU_OBSCLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				MCU_OBSCLK_CTRL_CLK_DIV			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED					MCU_OBSCLK_CTRL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-6063. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MCU_OBSCLK_CTRL_OUT_MUX_SEL	R/W	0h	MCU_OBSCLK pin output mux selection. Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MCU_OBSCLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Reset Source: mod_por_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MCU_OBSCLK_CTRL_CLK_DIV	R/W	0h	MCU_OBSCLK pin clock selection output divider Reset Source: mod_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCU_OBSCLK_CTRL_CLK_SEL	R/W	0h	MCU_OBSCLK pin clock selection Reset Source: mod_por_rst_n

14.2.1.1.2.2.84 MCU_CTRL_MMR_CFG0_HFOSC0_CTRL Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_CTRL Register (Offset = 8010h) [reset = 0h]

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Table 14-6064. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8010h**

Figure 14-2016. MCU_CTRL_MMR_CFG0_HFOSC0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			HFOSC0_CTRL_BP_C	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-6066. MCU_CTRL_MMR_CFG0_HFOSC0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	HFOSC0_CTRL_BP_C	R/W	0h	Oscillator bypass control. When set oscillator is in bypass mode Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.85 MCU_CTRL_MMR_CFG0_HFOSC0_TRIM Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_TRIM Register (Offset = 8018h) [reset = 131022h]

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Table 14-6067. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8018h**

Figure 14-2017. MCU_CTRL_MMR_CFG0_HFOSC0_TRIM Name Register

31	30	29	28	27	26	25	24
HFOSC0_TRIM_TRIM_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED		HFOSC0_TRIM_HYST		RESERVED	HFOSC0_TRIM_I_MULT		
NONE		R/W		NONE	R/W		
0h		1h		0h	3h		
15	14	13	12	11	10	9	8
RESERVED		HFOSC0_TRIM_R_REF					
NONE		R/W					
0h		10h					
7	6	5	4	3	2	1	0
HFOSC0_TRIM_I_IBIAS_COMP				HFOSC0_TRIM_R_IBIAS_REF			
R/W				R/W			
2h				2h			

Table 14-6069. MCU_CTRL_MMR_CFG0_HFOSC0_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_TRIM_TRIM_EN	R/W	0h	Apply MMR values to OSC trim inputs instead of tie-offs Reset Source: mod_por_rst_n
30:22	RESERVED	NONE	0h	Reserved
21:20	HFOSC0_TRIM_HYST	R/W	1h	Sets comparator hysterisis Reset Source: mod_por_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	HFOSC0_TRIM_I_MULT	R/W	3h	AGC AMP current multiplication gain Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	HFOSC0_TRIM_R_REF	R/W	10h	Sets the AMP AGC bias current Reset Source: mod_por_rst_n
7:4	HFOSC0_TRIM_I_IBIAS_COMP	R/W	2h	Sets the COMP bias current Reset Source: mod_por_rst_n
3:0	HFOSC0_TRIM_R_IBIAS_REF	R/W	2h	Sets the base IBIAS reference Reset Source: mod_por_rst_n

14.2.1.1.2.2.86 *MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM Register*

1 MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM Register (Offset = 8024h) [reset = 0h]

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Table 14-6070. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8024h**

Figure 14-2018. MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	RC12M_OSC_TRIM_TRIMOSC_COARSE_DIR	RC12M_OSC_TRIM_TRIMOSC_COARSE			RC12M_OSC_TRIM_TRIMOSC_FINE		
NONE	R/W	R/W			R/W		
0h	X	X			X		

Table 14-6072. MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	RC12M_OSC_TRIM_TRIMOSC_COARSE_DIR	R/W	X	Coarse adjustment direction. If output is greater than 12.5 Reset Source: mod_por_rst_n
5:3	RC12M_OSC_TRIM_TRIMOSC_COARSE	R/W	X	Coarse adjustment. Frequency is decreased or increased by 1.25 MHz per value based on the trimosc_coarse_dir value. Reset Source: mod_por_rst_n
2:0	RC12M_OSC_TRIM_TRIMOSC_FINE	R/W	X	Fine adjustment. Decreases the frequency by 250 KHz per value. Reset Source: mod_por_rst_n

14.2.1.1.2.2.87 MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Register (Offset = 8030h) [reset = 8068h]

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Table 14-6073. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8030h**

Figure 14-2019. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Name Register

31	30	29	28	27	26	25	24
HFOSC0_CLKOUT_32K_CTRL_RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN	RESERVED						HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS
R/W	NONE						R/W
1h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HFOSC0_CLKOUT_32K_CTRL_HSDIV						
NONE	R/W						
0h	68h						

Table 14-6075. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_CLKOUT_32K_CTRL_RESET	R/W	0h	Asynchronous Divider Reset Reset Source: sys_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN	R/W	1h	HFOSC0_CLKOUT_32K active: Reset Source: sys_por_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS	R/W	0h	HFOSC0_CLKOUT_32K Synchronize Deactivate Reset Source: sys_por_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HFOSC0_CLKOUT_32K_CTRL_HSDIV	R/W	68h	HFOSC0_CLKOUT_32K divider: Reset Source: sys_por_rst_n

14.2.1.1.2.2.88 MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL Register (Offset = 8040h) [reset = 0h]

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Table 14-6076. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8040h**

Figure 14-2020. MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCU_M4FSS_CLKSEL_M4FSS_CLKSEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-6078. MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_M4FSS_CLKSEL_M4FSS_CLKSEL	R/W	0h	Selects the Clock Divider for M4FSS Reset Source: mod_por_rst_n

14.2.1.1.2.2.89 MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK Register (Offset = 8044h) [reset = 23D08FFh]

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Table 14-6079. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8044h**

Figure 14-2021. MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK Name Register

31	30	29	28	27	26	25	24
RESERVED						MCU_M4FSS_SYSTICK_NOREF	MCU_M4FSS_SYSTICK_SKEW
NONE						R	R/W
0h						1h	0h
23	22	21	20	19	18	17	16
MCU_M4FSS_SYSTICK_TENMS							
R/W							
3D08FFh							
15	14	13	12	11	10	9	8
MCU_M4FSS_SYSTICK_TENMS							
R/W							
3D08FFh							
7	6	5	4	3	2	1	0
MCU_M4FSS_SYSTICK_TENMS							
R/W							
3D08FFh							

Table 14-6081. MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	MCU_M4FSS_SYSTICK_NOREF	R	1h	No External Reference Clock for SysTick is available Reset Source: mod_g_rst_n
24	MCU_M4FSS_SYSTICK_SKEW	R/W	0h	Indicates whether or not the M4FSS free running clock divided by TENMS produces a 100Hz tick exactly Reset Source: mod_g_rst_n
23:0	MCU_M4FSS_SYSTICK_TENMS	R/W	3D08FFh	Integer Divider Value that produces a 100Hz SysTick from the M4FSS Clock Frequency. Default is 3,999,999 (4M - 1) to produce a 100Hz clock from a 400 MHz M4FSS Clock. Reset Source: mod_g_rst_n

14.2.1.1.2.2.90 MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Register (Offset = 8050h) [reset = 800000h]

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Table 14-6082. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8050h**

Figure 14-2022. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Name Register

31	30	29	28	27	26	25	24
MCU_PLL_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MCU_PLL_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6084. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_PLL_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MCU_PLL_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. Reset Source: mcu_chip1_rst_n
22:9	RESERVED	NONE	0h	Reserved
8	MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN	R/W	0h	When set, actives automatic switching of MCU PLL[2:0] clock source to CLK_12M_RC if HFOSC0 clock loss is detected Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.91 MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL Register (Offset = 8060h) [reset = 0h]

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Table 14-6085. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8060h**

Figure 14-2023. MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER0_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-6087. MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER0_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.2.2.92 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL Register (Offset = 8064h) [reset = 0h]

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Table 14-6088. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8064h**

Figure 14-2024. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER1_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-6090. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER1_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.2.2.93 MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL Register (Offset = 8068h) [reset = 0h]

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Table 14-6091. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 8068h**

Figure 14-2025. MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER2_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-6093. MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER2_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.2.2.94 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL Register (Offset = 806Ch) [reset = 0h]

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Table 14-6094. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 806Ch**

Figure 14-2026. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER3_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-6096. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER3_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.2.2.95 MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL Register (Offset = 80A0h) [reset = 0h]

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Table 14-6097. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 80A0h**

Figure 14-2027. MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCU_SPI0_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6099. MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCU_SPI0_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.96 MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL Register (Offset = 80A4h) [reset = 0h]

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Table 14-6100. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 80A4h**

Figure 14-2028. MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCU_SPI1_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6102. MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCU_SPI1_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.97 MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL Register

1 MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL Register (Offset = 80B0h) [reset = 0h]

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Table 14-6103. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 80B0h**

Figure 14-2029. MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>MCU_WWD0_CLKSEL_WRTLOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MCU_WWD0_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-6105. MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_WWD0_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	MCU_WWD0_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.2.2.98 MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL Register

1 MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL Register (Offset = 80D0h) [reset = 0h]

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Table 14-6106. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 80D0h**

Figure 14-2030. MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DDR16SS_PMCTRL_DATA_RETENTION			
NONE				R/W			
0h				0h			

Table 14-6108. MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DDR16SS_PMCTRL_DATA_RETENTION	R/W	0h	DDR16SS Retention: Reset Source: mod_g_rst_n

14.2.1.1.2.2.99 MCU_CTRL_MMR_CFG0_LOCK2_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

- KICK0 component

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Table 14-6109. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 9008h**

Figure 14-2031. MCU_CTRL_MMR_CFG0_LOCK2_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0							
R/W							
0h							

Table 14-6111. MCU_CTRL_MMR_CFG0_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.100 MCU_CTRL_MMR_CFG0_LOCK2_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

- KICK1 component

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Table 14-6112. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 900Ch**

Figure 14-2032. MCU_CTRL_MMR_CFG0_LOCK2_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1							
R/W							
0h							

Table 14-6114. MCU_CTRL_MMR_CFG0_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.101 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register (Offset = 9100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-6115. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 9100h**

Figure 14-2033. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0_READONLY							
R							
0h							

Table 14-6117. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.102 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register (Offset = 9104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-6118. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 9104h**

Figure 14-2034. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1_READONLY							
R							
0h							

Table 14-6120. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.103 MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Register (Offset = A000h) [reset = 0h]

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Table 14-6121. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A000h**

Figure 14-2035. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							MCU_OBSCLK_CTRL_OUT_MUX_SEL_PROXY
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MCU_OBSCLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCU_OBSCLK_CTRL_CLK_DIV_PROXY			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MCU_OBSCLK_CTRL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-6123. MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MCU_OBSCLK_CTRL_OUT_MUX_SEL_PROXY	R/W	0h	MCU_OBSCLK pin output mux selection. Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MCU_OBSCLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Reset Source: mod_por_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MCU_OBSCLK_CTRL_CLK_DIV_PROXY	R/W	0h	MCU_OBSCLK pin clock selection output divider Reset Source: mod_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCU_OBSCLK_CTRL_CLK_SEL_PROXY	R/W	0h	MCU_OBSCLK pin clock selection Reset Source: mod_por_rst_n

14.2.1.1.2.2.104 MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY Register (Offset = A010h) [reset = 0h]

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Table 14-6124. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A010h**

Figure 14-2036. MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			HFOSC0_CTRL_BP_C_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-6126. MCU_CTRL_MMR_CFG0_HFOSC0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	HFOSC0_CTRL_BP_C_PROXY	R/W	0h	Oscillator bypass control. When set oscillator is in bypass mode Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.105 MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY Register (Offset = A018h) [reset = 131022h]

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Table 14-6127. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A018h**

Figure 14-2037. MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>HFOSC0_TRIM_TRIM_EN_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">HFOSC0_TRIM_HYST_PROXY</td><td>RESERVED</td><td colspan="3">HFOSC0_TRIM_I_MULT_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">1h</td><td>0h</td><td colspan="3">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">HFOSC0_TRIM_R_REF_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">HFOSC0_TRIM_I_IBIAS_COMP_PROXY</td><td colspan="4">HFOSC0_TRIM_R_IBIAS_REF_PROXY</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">2h</td><td colspan="4">2h</td></tr>
</table>

Table 14-6129. MCU_CTRL_MMR_CFG0_HFOSC0_TRIM_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_TRIM_TRIM_EN_PROXY	R/W	0h	Apply MMR values to OSC trim inputs instead of tie-offs Reset Source: mod_por_rst_n
30:22	RESERVED	NONE	0h	Reserved
21:20	HFOSC0_TRIM_HYST_PROXY	R/W	1h	Sets comparator hysterisis Reset Source: mod_por_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	HFOSC0_TRIM_I_MULT_PROXY	R/W	3h	AGC AMP current multiplication gain Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	HFOSC0_TRIM_R_REF_PROXY	R/W	10h	Sets the AMP AGC bias current Reset Source: mod_por_rst_n
7:4	HFOSC0_TRIM_I_IBIAS_COMP_PROXY	R/W	2h	Sets the COMP bias current Reset Source: mod_por_rst_n
3:0	HFOSC0_TRIM_R_IBIAS_REF_PROXY	R/W	2h	Sets the base IBIAS reference Reset Source: mod_por_rst_n

14.2.1.1.2.2.106 MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY Register

1 MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY Register (Offset = A024h) [reset = 0h]

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Table 14-6130. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A024h**

Figure 14-2038. MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	RC12M_OSC_TRIM_TRIMOSC_COARSE_DIR_PROXY	RC12M_OSC_TRIM_TRIMOSC_COARSE_PROXY			RC12M_OSC_TRIM_TRIMOSC_FINE_PROXY		
NONE	R/W	R/W			R/W		
0h	X	X			X		

Table 14-6132. MCU_CTRL_MMR_CFG0_RC12M_OSC_TRIM_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	RC12M_OSC_TRIM_TRIMOSC_COARSE_DIR_PROXY	R/W	X	Coarse adjustment direction. If output is greater than 12.5 Reset Source: mod_por_rst_n
5:3	RC12M_OSC_TRIM_TRIMOSC_COARSE_PROXY	R/W	X	Coarse adjustment. Frequency is decreased or increased by 1.25 MHz per value based on the trimosc_coarse_dir value. Reset Source: mod_por_rst_n
2:0	RC12M_OSC_TRIM_TRIMOSC_FINE_PROXY	R/W	X	Fine adjustment. Decreases the frequency by 250 KHz per value. Reset Source: mod_por_rst_n

14.2.1.1.2.2.107 MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register (Offset = A030h) [reset = 8068h]

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Table 14-6133. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A030h**

Figure 14-2039. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
HFOSC0_CLKOUT_32K_CTRL_RESET_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN_PROXY	RESERVED						HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS_PROXY
R/W	NONE						R/W
1h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HFOSC0_CLKOUT_32K_CTRL_HSDIV_PROXY						
NONE	R/W						
0h	68h						

Table 14-6135. MCU_CTRL_MMR_CFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_CLKOUT_32K_CTRL_RESET_PROXY	R/W	0h	Asynchronous Divider Reset Reset Source: sys_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN_PROXY	R/W	1h	HFOSC0_CLKOUT_32K active: Reset Source: sys_por_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS_PROXY	R/W	0h	HFOSC0_CLKOUT_32K Synchronize Deactivate Reset Source: sys_por_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HFOSC0_CLKOUT_32K_CTRL_HSDIV_PROXY	R/W	68h	HFOSC0_CLKOUT_32K divider: Reset Source: sys_por_rst_n

14.2.1.1.2.2.108 MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL_PROXY Register (Offset = A040h) [reset = 0h]

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Table 14-6136. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A040h**

Figure 14-2040. MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCU_M4FSS_CLKSEL_M4FSS_CLKSEL_PROXY
NONE							R/W
0h							0h

Table 14-6138. MCU_CTRL_MMR_CFG0_MCU_M4FSS_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_M4FSS_CLKSEL_M4FSS_CLKSEL_PROXY	R/W	0h	Selects the Clock Divider for M4FSS Reset Source: mod_por_rst_n

14.2.1.1.2.2.109 MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK_PROXY Register (Offset = A044h) [reset = 23D08FFh]

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Table 14-6139. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A044h**

Figure 14-2041. MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED						MCU_M4FSS_SYSTICK_NOREF_PROXY	MCU_M4FSS_SYSTICK_SKEW_PROXY
NONE						R	R/W
0h						1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MCU_M4FSS_SYSTICK_TENMS_PROXY							
R/W							
3D08FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_M4FSS_SYSTICK_TENMS_PROXY							
R/W							
3D08FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_M4FSS_SYSTICK_TENMS_PROXY							
R/W							
3D08FFh							

Table 14-6141. MCU_CTRL_MMR_CFG0_MCU_M4FSS_SYSTICK_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	MCU_M4FSS_SYSTICK_NOREF_PROXY	R	1h	No External Reference Clock for SysTick is available Reset Source: mod_g_rst_n
24	MCU_M4FSS_SYSTICK_SKEW_PROXY	R/W	0h	Indicates whether or not the M4FSS free running clock divided by TENMS produces a 100Hz tick exactly Reset Source: mod_g_rst_n
23:0	MCU_M4FSS_SYSTICK_TENMS_PROXY	R/W	3D08FFh	Integer Divider Value that produces a 100Hz SysTick from the M4FSS Clock Frequency. Default is 3,999,999 (4M - 1) to produce a 100Hz clock from a 400 MHz M4FSS Clock. Reset Source: mod_g_rst_n

14.2.1.1.2.2.110 MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Register (Offset = A050h) [reset = 800000h]

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Table 14-6142. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A050h**

Figure 14-2042. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_PLL_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MCU_PLL_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6144. MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_PLL_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MCU_PLL_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. Reset Source: mcu_chip1_rst_n
22:9	RESERVED	NONE	0h	Reserved
8	MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN_PROXY	R/W	0h	When set, actives automatic switching of MCU PLL[2:0] clock source to CLK_12M_RC if HFOSC0 clock loss is detected Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.111 MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY Register (Offset = A060h) [reset = 0h]

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Table 14-6145. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A060h**

Figure 14-2043. MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER0_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-6147. MCU_CTRL_MMR_CFG0_MCU_TIMER0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.2.2.112 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY Register (Offset = A064h) [reset = 0h]

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Table 14-6148. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A064h**

Figure 14-2044. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER1_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-6150. MCU_CTRL_MMR_CFG0_MCU_TIMER1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.2.2.113 MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY Register (Offset = A068h) [reset = 0h]

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Table 14-6151. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A068h**

Figure 14-2045. MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER2_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-6153. MCU_CTRL_MMR_CFG0_MCU_TIMER2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.2.2.114 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY Register (Offset = A06Ch) [reset = 0h]

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Table 14-6154. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A06Ch**

Figure 14-2046. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCU_TIMER3_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-6156. MCU_CTRL_MMR_CFG0_MCU_TIMER3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCU_TIMER3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control (Reserved values default to HFOSC0_CLK) Reset Source: sys_por_rst_n

14.2.1.1.2.2.115 MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY Register (Offset = A0A0h) [reset = 0h]

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Table 14-6157. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A0A0h**

Figure 14-2047. MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCU_SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6159. MCU_CTRL_MMR_CFG0_MCU_SPI0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCU_SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.116 MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY Register (Offset = A0A4h) [reset = 0h]

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Table 14-6160. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A0A4h**

Figure 14-2048. MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCU_SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6162. MCU_CTRL_MMR_CFG0_MCU_SPI1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCU_SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.117 MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY Register (Offset = A0B0h) [reset = 0h]

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Table 14-6163. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A0B0h**

Figure 14-2049. MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_WWD0_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCU_WWD0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-6165. MCU_CTRL_MMR_CFG0_MCU_WWD0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_WWD0_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	MCU_WWD0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Reset Source: mod_g_rst_n

14.2.1.1.2.2.118 MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY Register (Offset = A0D0h) [reset = 0h]

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Table 14-6166. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 A0D0h**

Figure 14-2050. MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DDR16SS_PMCTRL_DATA_RETENTION_PROXY			
NONE				R/W			
0h				0h			

Table 14-6168. MCU_CTRL_MMR_CFG0_DDR16SS_PMCTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DDR16SS_PMCTRL_DATA_RETENTION_PROXY	R/W	0h	DDR16SS Retention: Reset Source: mod_g_rst_n

14.2.1.1.2.2.119 MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register (Offset = B008h) [reset = 0h]

- KICK0 component

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Table 14-6169. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 B008h**

Figure 14-2051. MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0_PROXY							
R/W							
0h							

Table 14-6171. MCU_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.120 MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register (Offset = B00Ch) [reset = 0h]

- KICK1 component

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Table 14-6172. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 B00Ch**

Figure 14-2052. MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1_PROXY							
R/W							
0h							

Table 14-6174. MCU_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.121 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register (Offset = B100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-6175. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 B100h**

Figure 14-2053. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0							
R/W							
0h							

Table 14-6177. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.122 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register (Offset = B104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-6178. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 B104h**

Figure 14-2054. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1							
R/W							
0h							

Table 14-6180. MCU_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.123 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL Register (Offset = C020h) [reset = 0h]

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Table 14-6181. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C020h**

Figure 14-2055. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_CTRL_BIST_RESET	RESERVED			MCU_M4FSS0_LBIST_CTRL_BIST_RUN			
R/W	NONE			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			MCU_M4FSS0_LBIST_CTRL_SUBCHIP_ID				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_M4FSS0_LBIST_CTRL_RUNBIST_MODE				RESERVED		MCU_M4FSS0_LBIST_CTRL_DC_DEF	
R/W				NONE		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_M4FSS0_LBIST_CTRL_LOAD_DIV	RESERVED		MCU_M4FSS0_LBIST_CTRL_DIVIDE_RATIO				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-6183. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_M4FSS0_LBIST_CTRL_BIST_RESET	R/W	0h	This bitfield is not used. The bist_reset control for DMSC is generated by the POST state machine. The bitfield still reflects the efuse value. Reset Source: mod_g_rst_n
30:28	RESERVED	NONE	0h	Reserved
27:24	MCU_M4FSS0_LBIST_CTRL_BIST_RUN	R/W	0h	This bitfield is not used. The bist_run control for DMSC is generated by the POST state machine. The bitfield still reflects the efuse value. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	MCU_M4FSS0_LBIST_CTRL_SUBCHIP_ID	R/W	0h	Specifies which sub-chip is to be tested Reset Source: mod_g_rst_n
15:12	MCU_M4FSS0_LBIST_CTRL_RUNBIST_MODE	R/W	0h	Runbist mode active if all bits are 1 Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:8	MCU_M4FSS0_LBIST_CTRL_DC_DEF	R/W	0h	Clock delay after scan_active switching Reset Source: mod_g_rst_n

Table 14-6183. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	MCU_M4FSS0_LBIST_CTRL_LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1 Reset Source: mod_g_rst_n
6:5	RESERVED	NONE	0h	Reserved
4:0	MCU_M4FSS0_LBIST_CTRL_DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio Reset Source: mod_g_rst_n

14.2.1.1.2.2.124 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT Register (Offset = C024h) [reset = 0h]

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Table 14-6184. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C024h**

Figure 14-2056. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT Name Register

31	30	29	28	27	26	25	24
RESERVED		MCU_M4FSS0_LBIST_PATCOUNT_STATIC_PC_DEF					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
MCU_M4FSS0_LBIST_PATCOUNT_STATIC_PC_DEF							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCU_M4FSS0_LBIST_PATCOUNT_SET_PC_DEF			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_PATCOUNT_RESET_PC_DEF				MCU_M4FSS0_LBIST_PATCOUNT_SCAN_PC_DEF			
R/W				R/W			
0h				0h			

Table 14-6186. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	MCU_M4FSS0_LBIST_PATCOUNT_STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MCU_M4FSS0_LBIST_PATCOUNT_SET_PC_DEF	R/W	0h	Number of set patterns to run Reset Source: mod_g_rst_n
7:4	MCU_M4FSS0_LBIST_PATCOUNT_RESET_PC_DEF	R/W	0h	Number of reset patterns to run Reset Source: mod_g_rst_n
3:0	MCU_M4FSS0_LBIST_PATCOUNT_SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run Reset Source: mod_g_rst_n

14.2.1.1.2.2.125 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0 Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0 Register (Offset = C028h) [reset = 0h]

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Table 14-6187. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C028h**

Figure 14-2057. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0 Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_M4FSS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							

Table 14-6189. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_M4FSS0_LBIST_SEED0_PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0) Reset Source: mod_g_rst_n

14.2.1.1.2.2.126 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1 Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1 Register (Offset = C02Ch) [reset = 0h]

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Table 14-6190. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C02Ch**

Figure 14-2058. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			MCU_M4FSS0_LBIST_SEED1_PRPG_DEF				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_SEED1_PRPG_DEF							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_SEED1_PRPG_DEF							
R/W							
0h							

Table 14-6192. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	MCU_M4FSS0_LBIST_SEED1_PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32) Reset Source: mod_g_rst_n

14.2.1.1.2.2.127 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0 Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0 Register (Offset = C030h) [reset = 0h]

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Table 14-6193. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C030h**

Figure 14-2059. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0 Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_SPARE0_SPARE0							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_M4FSS0_LBIST_SPARE0_SPARE0							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_SPARE0_SPARE0							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_SPARE0_SPARE0						MCU_M4FSS0_LBIST_SPARE0_PBIST_SELFTEST_EN	MCU_M4FSS0_LBIST_SPARE0_LBIST_SELFTEST_EN
R/W						R/W	R/W
0h						0h	0h

Table 14-6195. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	MCU_M4FSS0_LBIST_SPARE0_SPARE0	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n
1	MCU_M4FSS0_LBIST_SPARE0_PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control Reset Source: mod_g_rst_n
0	MCU_M4FSS0_LBIST_SPARE0_LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control Reset Source: mod_g_rst_n

14.2.1.1.2.2.128 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1 Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1 Register (Offset = C034h) [reset = 0h]

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Table 14-6196. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C034h**

Figure 14-2060. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1 Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_M4FSS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_SPARE1_SPARE1							
R/W							
0h							

Table 14-6198. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_M4FSS0_LBIST_SPARE1_SPARE1	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n

14.2.1.1.2.2.129 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT Register (Offset = C038h) [reset = 0h]

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Table 14-6199. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C038h**

Figure 14-2061. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_STAT_BIST_DONE	RESERVED						
R	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_M4FSS0_LBIST_STAT_BIST_RUNNING	RESERVED					MCU_M4FSS0_LBIST_STAT_OUT_MUX_CTL	
R	NONE					R/W	
X	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_M4FSS0_LBIST_STAT_MISR_MUX_CTL							
R/W							
0h							

Table 14-6201. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_M4FSS0_LBIST_STAT_BIST_DONE	R	X	LBIST is done Reset Source: mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	MCU_M4FSS0_LBIST_STAT_BIST_RUNNING	R	X	LBIST is running Reset Source: mod_g_rst_n
14:10	RESERVED	NONE	0h	Reserved
9:8	MCU_M4FSS0_LBIST_STAT_OUT_MUX_CTL	R/W	0h	Selects source of LBIST output Reset Source: mod_g_rst_n
7:0	MCU_M4FSS0_LBIST_STAT_MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR. Reset Source: mod_g_rst_n

14.2.1.1.2.2.130 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR Register (Offset = C03Ch) [reset = 0h]

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Table 14-6202. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 C03Ch**

Figure 14-2062. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_MISR_MISR_RESULT							
R							
X							
23	22	21	20	19	18	17	16
MCU_M4FSS0_LBIST_MISR_MISR_RESULT							
R							
X							
15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_MISR_MISR_RESULT							
R							
X							
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_MISR_MISR_RESULT							
R							
X							

Table 14-6204. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_M4FSS0_LBIST_MISR_MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl Reset Source: mod_g_rst_n

14.2.1.1.2.2.131 MCU_CTRL_MMR_CFG0_LOCK3_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK3_KICK0 Register (Offset = D008h) [reset = 0h]

- KICK0 component

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Table 14-6205. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 D008h**

Figure 14-2063. MCU_CTRL_MMR_CFG0_LOCK3_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0							
R/W							
0h							

Table 14-6207. MCU_CTRL_MMR_CFG0_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.132 MCU_CTRL_MMR_CFG0_LOCK3_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK3_KICK1 Register (Offset = D00Ch) [reset = 0h]

- KICK1 component

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Table 14-6208. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 D00Ch**

Figure 14-2064. MCU_CTRL_MMR_CFG0_LOCK3_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1							
R/W							
0h							

Table 14-6210. MCU_CTRL_MMR_CFG0_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.133 MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register (Offset = D100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-6211. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 D100h**

Figure 14-2065. MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0_READONLY							
R							
0h							

Table 14-6213. MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.2.2.134 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL_PROXY Register (Offset = E020h) [reset = 0h]

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Table 14-6214. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E020h**

Figure 14-2066. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_CTRL_BIST_RESET_PROXY	RESERVED			MCU_M4FSS0_LBIST_CTRL_BIST_RUN_PROXY			
R/W	NONE			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			MCU_M4FSS0_LBIST_CTRL_SUBCHIP_ID_PROXY				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_M4FSS0_LBIST_CTRL_RUNBIST_MODE_PROXY				RESERVED		MCU_M4FSS0_LBIST_CTRL_DC_DEF_PROXY	
R/W				NONE		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_M4FSS0_LBIST_CTRL_LOAD_DIV_PROXY	RESERVED		MCU_M4FSS0_LBIST_CTRL_DIVIDE_RATIO_PROXY				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-6216. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_M4FSS0_LBIST_CTRL_BIST_RESET_PROXY	R/W	0h	This bitfield is not used. The bist_reset control for DMSC is generated by the POST state machine. The bitfield still reflects the efuse value. Reset Source: mod_g_rst_n
30:28	RESERVED	NONE	0h	Reserved
27:24	MCU_M4FSS0_LBIST_CTRL_BIST_RUN_PROXY	R/W	0h	This bitfield is not used. The bist_run control for DMSC is generated by the POST state machine. The bitfield still reflects the efuse value. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	MCU_M4FSS0_LBIST_CTRL_SUBCHIP_ID_PROXY	R/W	0h	Specifies which sub-chip is to be tested Reset Source: mod_g_rst_n
15:12	MCU_M4FSS0_LBIST_CTRL_RUNBIST_MODE_PROXY	R/W	0h	Runbist mode active if all bits are 1 Reset Source: mod_g_rst_n

Table 14-6216. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	RESERVED	NONE	0h	Reserved
9:8	MCU_M4FSS0_LBIST_CTRL_DC_DEF_PROXY	R/W	0h	Clock delay after scan_active switching Reset Source: mod_g_rst_n
7	MCU_M4FSS0_LBIST_CTRL_LOAD_DIV_PROXY	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1 Reset Source: mod_g_rst_n
6:5	RESERVED	NONE	0h	Reserved
4:0	MCU_M4FSS0_LBIST_CTRL_DIVIDE_RATIO_PROXY	R/W	0h	LBIST clock divide ratio Reset Source: mod_g_rst_n

14.2.1.1.2.2.135 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT_PROXY Register (Offset = E024h) [reset = 0h]

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Table 14-6217. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E024h**

Figure 14-2067. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED		MCU_M4FSS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
MCU_M4FSS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCU_M4FSS0_LBIST_PATCOUNT_SET_PC_DEF_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_PATCOUNT_RESET_PC_DEF_PROXY				MCU_M4FSS0_LBIST_PATCOUNT_SCAN_PC_DEF_PROXY			
R/W				R/W			
0h				0h			

Table 14-6219. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_PATCOUNT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	MCU_M4FSS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY	R/W	0h	Number of stuck-at patterns to run Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MCU_M4FSS0_LBIST_PATCOUNT_SET_PC_DEF_PROXY	R/W	0h	Number of set patterns to run Reset Source: mod_g_rst_n
7:4	MCU_M4FSS0_LBIST_PATCOUNT_RESET_PC_DEF_PROXY	R/W	0h	Number of reset patterns to run Reset Source: mod_g_rst_n
3:0	MCU_M4FSS0_LBIST_PATCOUNT_SCAN_PC_DEF_PROXY	R/W	0h	Number of chain test patterns to run Reset Source: mod_g_rst_n

14.2.1.1.2.2.136 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0_PROXY Register (Offset = E028h) [reset = 0h]

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Table 14-6220. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E028h**

Figure 14-2068. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MCU_M4FSS0_LBIST_SEED0_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MCU_M4FSS0_LBIST_SEED0_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MCU_M4FSS0_LBIST_SEED0_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MCU_M4FSS0_LBIST_SEED0_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6222. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_M4FSS0_LBIST_SEED0_PRPG_DEF_PROXY	R/W	0h	Initial seed for PRPG (bits 31:0) Reset Source: mod_g_rst_n

14.2.1.1.2.2.137 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1_PROXY Register (Offset = E02Ch) [reset = 0h]

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Table 14-6223. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E02Ch**

Figure 14-2069. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			MCU_M4FSS0_LBIST_SEED1_PRPG_DEF_PROXY				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_SEED1_PRPG_DEF_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_SEED1_PRPG_DEF_PROXY							
R/W							
0h							

Table 14-6225. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SEED1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	MCU_M4FSS0_LBIST_SEED1_PRPG_DEF_PROXY	R/W	0h	Initial seed for PRPG (bits 52:32) Reset Source: mod_g_rst_n

14.2.1.1.2.2.138 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0_PROXY Register (Offset = E030h) [reset = 0h]

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Table 14-6226. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E030h**

Figure 14-2070. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_M4FSS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_SPARE0_SPARE0_PROXY						MCU_M4FSS0_LBIST_SPARE0_PBIST_SELFTEST_EN_PROXY	MCU_M4FSS0_LBIST_SPARE0_LBIST_SELFTEST_EN_PROXY
R/W						R/W	R/W
0h						0h	0h

Table 14-6228. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	MCU_M4FSS0_LBIST_SPARE0_SPARE0_PROXY	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n
1	MCU_M4FSS0_LBIST_SPARE0_PBIST_SELFTEST_EN_PROXY	R/W	0h	PBIST isolation control Reset Source: mod_g_rst_n
0	MCU_M4FSS0_LBIST_SPARE0_LBIST_SELFTEST_EN_PROXY	R/W	0h	LBIST isolation control Reset Source: mod_g_rst_n

14.2.1.1.2.2.139 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1_PROXY Register (Offset = E034h) [reset = 0h]

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Table 14-6229. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E034h**

Figure 14-2071. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
MCU_M4FSS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							

Table 14-6231. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_SPARE1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_M4FSS0_LBIST_SPARE1_SPARE1_PROXY	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n

14.2.1.1.2.2.140 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT_PROXY Register (Offset = E038h) [reset = 0h]

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Table 14-6232. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E038h**

Figure 14-2072. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_STAT_BIST_DONE_PROXY	RESERVED						
R	NONE						
X	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
MCU_M4FSS0_LBIST_STAT_BIST_RUNNING_PROXY	RESERVED					MCU_M4FSS0_LBIST_STAT_OUT_MUX_CTL_PROXY	
R	NONE					R/W	
X	0h					0h	

7	6	5	4	3	2	1	0
MCU_M4FSS0_LBIST_STAT_MISR_MUX_CTL_PROXY							
R/W							
0h							

Table 14-6234. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_M4FSS0_LBIST_STAT_BIST_DONE_PROXY	R	X	LBIST is done Reset Source: mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	MCU_M4FSS0_LBIST_STAT_BIST_RUNNING_PROXY	R	X	LBIST is running Reset Source: mod_g_rst_n
14:10	RESERVED	NONE	0h	Reserved
9:8	MCU_M4FSS0_LBIST_STAT_OUT_MUX_CTL_PROXY	R/W	0h	Selects source of LBIST output Reset Source: mod_g_rst_n
7:0	MCU_M4FSS0_LBIST_STAT_MISR_MUX_CTL_PROXY	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR. Reset Source: mod_g_rst_n

14.2.1.1.2.2.141 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR_PROXY Register (Offset = E03Ch) [reset = 0h]

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Table 14-6235. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 E03Ch**

Figure 14-2073. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_M4FSS0_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MCU_M4FSS0_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_M4FSS0_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCU_M4FSS0_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							

Table 14-6237. MCU_CTRL_MMR_CFG0_MCU_M4FSS0_LBIST_MISR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCU_M4FSS0_LBIST_MISR_MISR_RESULT_PROXY	R	X	32-bits of MISR value selected by misr_mux_ctl Reset Source: mod_g_rst_n

14.2.1.1.2.2.142 MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register (Offset = F008h) [reset = 0h]

- KICK0 component

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Table 14-6238. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 F008h**

Figure 14-2074. MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0_PROXY							
R/W							
0h							

Table 14-6240. MCU_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.143 MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register (Offset = F00Ch) [reset = 0h]

- KICK1 component

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Table 14-6241. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 F00Ch**

Figure 14-2075. MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1_PROXY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCK3_KICK1_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK3_KICK1_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK3_KICK1_PROXY							
R/W							
0h							

Table 14-6243. MCU_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.144 MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register (Offset = F100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-6244. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0450 F100h**

Figure 14-2076. MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0							
R/W							
0h							

Table 14-6246. MCU_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.2.2.145 MCU_CTRL_MMR_CFG0_LOCK4_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK4_KICK0 Register (Offset = 11008h) [reset = 0h]

- KICK0 component

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Table 14-6247. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1008h**

Figure 14-2077. MCU_CTRL_MMR_CFG0_LOCK4_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0							
R/W							
0h							

Table 14-6249. MCU_CTRL_MMR_CFG0_LOCK4_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.146 MCU_CTRL_MMR_CFG0_LOCK4_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK4_KICK1 Register (Offset = 1100Ch) [reset = 0h]

- KICK1 component

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Table 14-6250. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 100Ch**

Figure 14-2078. MCU_CTRL_MMR_CFG0_LOCK4_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1							
R/W							
0h							

Table 14-6252. MCU_CTRL_MMR_CFG0_LOCK4_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.147 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register (Offset = 11100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6253. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1100h**

Figure 14-2079. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0_READONLY							
R							
0h							

Table 14-6255. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.148 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register (Offset = 11104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6256. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1104h**

Figure 14-2080. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1_READONLY							
R							
0h							

Table 14-6258. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.149 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register (Offset = 11108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6259. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1108h**

Figure 14-2081. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2_READONLY							
R							
0h							

Table 14-6261. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.150 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register (Offset = 1110Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-6262. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 110Ch**

Figure 14-2082. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3_READONLY							
R							
0h							

Table 14-6264. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.151 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register (Offset = 11110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6265. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1110h**

Figure 14-2083. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4_READONLY							
R							
0h							

Table 14-6267. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.152 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register (Offset = 11114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6268. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1114h**

Figure 14-2084. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5_READONLY							
R							
0h							

Table 14-6270. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.153 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register (Offset = 11118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6271. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1118h**

Figure 14-2085. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6_READONLY							
R							
0h							

Table 14-6273. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.154 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register (Offset = 1111Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-6274. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 111Ch**

Figure 14-2086. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7_READONLY							
R							
0h							

Table 14-6276. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.155 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register (Offset = 11120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6277. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1120h**

Figure 14-2087. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8_READONLY							
R							
0h							

Table 14-6279. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.156 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register (Offset = 11124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6280. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1124h**

Figure 14-2088. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9_READONLY							
R							
0h							

Table 14-6282. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.157 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register (Offset = 11128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6283. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1128h**

Figure 14-2089. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10_READONLY							
R							
0h							

Table 14-6285. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.158 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register (Offset = 1112Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-6286. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 112Ch**

Figure 14-2090. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R11_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R11_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R11_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R11_READONLY							
R							
0h							

Table 14-6288. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R11_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.159 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register (Offset = 11130h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6289. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1130h**

Figure 14-2091. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R12_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R12_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R12_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R12_READONLY							
R							
0h							

Table 14-6291. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R12_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.160 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY Register (Offset = 11134h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6292. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1134h**

Figure 14-2092. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R13_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R13_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R13_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R13_READONLY							
R							
0h							

Table 14-6294. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R13_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.161 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register (Offset = 11138h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6295. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 1138h**

Figure 14-2093. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R14_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R14_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R14_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R14_READONLY							
R							
0h							

Table 14-6297. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R14_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.162 MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register (Offset = 13008h) [reset = 0h]

- KICK0 component

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Table 14-6298. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3008h**

Figure 14-2094. MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0_PROXY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCK4_KICK0_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK4_KICK0_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK4_KICK0_PROXY							
R/W							
0h							

Table 14-6300. MCU_CTRL_MMR_CFG0_LOCK4_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.163 MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register (Offset = 1300Ch) [reset = 0h]

- KICK1 component

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Table 14-6301. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 300Ch**

Figure 14-2095. MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1_PROXY							
R/W							
0h							

Table 14-6303. MCU_CTRL_MMR_CFG0_LOCK4_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.164 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register (Offset = 13100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6304. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3100h**

Figure 14-2096. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0							
R/W							
0h							

Table 14-6306. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.165 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register (Offset = 13104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6307. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3104h**

Figure 14-2097. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1							
R/W							
0h							

Table 14-6309. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.166 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register (Offset = 13108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6310. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3108h**

Figure 14-2098. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2							
R/W							
0h							

Table 14-6312. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.167 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register (Offset = 1310Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-6313. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 310Ch**

Figure 14-2099. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3							
R/W							
0h							

Table 14-6315. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.168 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register (Offset = 13110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6316. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3110h**

Figure 14-2100. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4							
R/W							
0h							

Table 14-6318. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.169 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register (Offset = 13114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6319. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3114h**

Figure 14-2101. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5							
R/W							
0h							

Table 14-6321. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.170 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register (Offset = 13118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6322. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3118h**

Figure 14-2102. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6							
R/W							
0h							

Table 14-6324. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.171 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register (Offset = 1311Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-6325. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 311Ch**

Figure 14-2103. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7							
R/W							
0h							

Table 14-6327. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.172 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register (Offset = 13120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6328. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3120h**

Figure 14-2104. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8							
R/W							
0h							

Table 14-6330. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.173 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register (Offset = 13124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6331. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3124h**

Figure 14-2105. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9							
R/W							
0h							

Table 14-6333. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.174 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register (Offset = 13128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6334. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3128h**

Figure 14-2106. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10							
R/W							
0h							

Table 14-6336. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.175 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register (Offset = 1312Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-6337. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 312Ch**

Figure 14-2107. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R11							
R/W							
0h							

Table 14-6339. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R11	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.176 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register (Offset = 13130h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6340. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3130h**

Figure 14-2108. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R12							
R/W							
0h							

Table 14-6342. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R12	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.177 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register (Offset = 13134h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6343. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3134h**

Figure 14-2109. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R13							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R13							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R13							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R13							
R/W							
0h							

Table 14-6345. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R13	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.178 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register (Offset = 13138h) [reset = 0h]

Claim bits for Partition 4

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Table 14-6346. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 3138h**

Figure 14-2110. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R14							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R14							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R14							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R14							
R/W							
0h							

Table 14-6348. MCU_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R14	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.179 MCU_CTRL_MMR_CFG0_POR_CTRL Register

1 MCU_CTRL_MMR_CFG0_POR_CTRL Register (Offset = 18000h) [reset = 10h]

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Table 14-6349. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8000h**

Figure 14-2111. MCU_CTRL_MMR_CFG0_POR_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED		POR_CTRL_OVRD_SET5	POR_CTRL_OVRD_SET4	POR_CTRL_OVRD_SET3	POR_CTRL_OVRD_SET2	POR_CTRL_OVRD_SET1	POR_CTRL_OVRD_SET0
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED		POR_CTRL_OVRD5	POR_CTRL_OVRD4	POR_CTRL_OVRD3	POR_CTRL_OVRD2	POR_CTRL_OVRD1	POR_CTRL_OVRD0
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POR_CTRL_TRIM_SEL	RESERVED		POR_CTRL_MASK_HHV	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		1h	0h			

Table 14-6351. MCU_CTRL_MMR_CFG0_POR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	POR_CTRL_OVRD_SET5	R/W	0h	Reserved override set Reset Source: mod_por_rst_n
28	POR_CTRL_OVRD_SET4	R/W	0h	POKLVB override set Reset Source: mod_por_rst_n
27	POR_CTRL_OVRD_SET3	R/W	0h	POKLVA override set Reset Source: mod_por_rst_n
26	POR_CTRL_OVRD_SET2	R/W	0h	POKHV override set Reset Source: mod_por_rst_n
25	POR_CTRL_OVRD_SET1	R/W	0h	BGOK override set Reset Source: mod_por_rst_n
24	POR_CTRL_OVRD_SET0	R/W	0h	PORHV override set Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	POR_CTRL_OVRD5	R/W	0h	Reserved override active Reset Source: mod_por_rst_n

Table 14-6351. MCU_CTRL_MMR_CFG0_POR_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	POR_CTRL_OVRD4	R/W	0h	POKLVB override active Reset Source: mod_por_rst_n
19	POR_CTRL_OVRD3	R/W	0h	POKLVA override active Reset Source: mod_por_rst_n
18	POR_CTRL_OVRD2	R/W	0h	POKHV override active Reset Source: mod_por_rst_n
17	POR_CTRL_OVRD1	R/W	0h	BGOK override active Reset Source: mod_por_rst_n
16	POR_CTRL_OVRD0	R/W	0h	PORHV override active Reset Source: mod_por_rst_n
15:8	RESERVED	NONE	0h	Reserved
7	POR_CTRL_TRIM_SEL	R/W	0h	POR Trim Select Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	POR_CTRL_MASK_HHV	R/W	1h	Mask HHV/SOC_PORz outputs when applying new trim values Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.180 MCU_CTRL_MMR_CFG0_POR_STAT Register

1 MCU_CTRL_MMR_CFG0_POR_STAT Register (Offset = 18004h) [reset = 0h]

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Table 14-6352. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8004h**

Figure 14-2112. MCU_CTRL_MMR_CFG0_POR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							POR_STAT_BGOK
NONE							R
0h							X
7	6	5	4	3	2	1	0
RESERVED			POR_STAT_SOC_POR	RESERVED			
NONE			R	NONE			
0h			X	0h			

Table 14-6354. MCU_CTRL_MMR_CFG0_POR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	POR_STAT_BGOK	R	X	Bandgap OK status Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	POR_STAT_SOC_POR	R	X	POR module status Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.181 MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL Register

1 MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL Register (Offset = 18100h) [reset = 0h]

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Table 14-6355. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8100h**

Figure 14-2113. MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				POR_BANDGAP_CTRL_BGAPI			
NONE				R/W			
0h				X			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POR_BANDGAP_CTRL_BGAPV							
R/W							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POR_BANDGAP_CTRL_BGAPC							
R/W							
X							

Table 14-6357. MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	POR_BANDGAP_CTRL_BGAPI	R/W	X	Bandgap output current trim bits Reset Source: mod_por_rst_n
15:8	POR_BANDGAP_CTRL_BGAPV	R/W	X	Bandgap output voltage magnitude trim bits Reset Source: mod_por_rst_n
7:0	POR_BANDGAP_CTRL_BGAPC	R/W	X	Bandgap slope trim bits. Bit7 is used to calculate the offset Reset Source: mod_por_rst_n

14.2.1.1.2.2.182 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL Register (Offset = 18110h) [reset = 80000000h]

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Table 14-6358. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8110h**

Figure 14-2114. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET	POK_VDDA_MCU_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6360. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDA_MCU_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.183 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL Register (Offset = 18114h) [reset = 80000000h]

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Table 14-6361. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8114h**

Figure 14-2115. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET	POK_VDDA_MCU_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6363. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDA_MCU_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.184 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL Register (Offset = 18118h) [reset = 80000000h]

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Table 14-6364. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8118h**

Figure 14-2116. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET	POK_VDD_CORE_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6366. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDD_CORE_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.185 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL Register (Offset = 1811Ch) [reset = 80000000h]

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Table 14-6367. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 811Ch**

Figure 14-2117. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET	POK_VDD_CORE_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6369. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDD_CORE_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.186 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL Register (Offset = 18120h) [reset = 80000000h]

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Table 14-6370. Instance Table

Instance Name	**Physical Address**
MCU_CTRL_MMR0	**0451 8120h**

Figure 14-2118. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>POK_VDDR_CORE_UV_CTRL_HYST_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET</td><td colspan="7">POK_VDDR_CORE_UV_CTRL_POK_TRIM</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>X</td><td colspan="7">X</td></tr>
</table>

Table 14-6372. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDR_CORE_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.187 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL Register (Offset = 18124h) [reset = 80000000h]

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Table 14-6373. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8124h**

Figure 14-2119. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET	POK_VDDR_CORE_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6375. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDR_CORE_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.188 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL Register (Offset = 18128h) [reset = 80000000h]

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Table 14-6376. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8128h**

Figure 14-2120. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MCU_1P8_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MCU_1P8_UV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MCU_1P8_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6378. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MCU_1P8_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MCU_1P8_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MCU_1P8_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.189 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL Register (Offset = 1812Ch) [reset = 80000000h]

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Table 14-6379. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 812Ch**

Figure 14-2121. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MCU_1P8_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MCU_1P8_OV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MCU_1P8_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6381. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MCU_1P8_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MCU_1P8_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MCU_1P8_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.190 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL Register (Offset = 18130h) [reset = 80000000h]

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Table 14-6382. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8130h**

Figure 14-2122. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MCU_3P3_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MCU_3P3_UV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MCU_3P3_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6384. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MCU_3P3_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MCU_3P3_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MCU_3P3_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.191 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL Register (Offset = 18134h) [reset = 80000000h]

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Table 14-6385. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8134h**

Figure 14-2123. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MCU_3P3_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MCU_3P3_OV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MCU_3P3_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6387. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MCU_3P3_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MCU_3P3_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MCU_3P3_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.192 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register (Offset = 18138h) [reset = 80000000h]

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Table 14-6388. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8138h**

Figure 14-2124. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6390. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.193 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register (Offset = 1813Ch) [reset = 80000000h]

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Table 14-6391. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 813Ch**

Figure 14-2125. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6393. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.194 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register (Offset = 18140h) [reset = 80000000h]

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Table 14-6394. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8140h**

Figure 14-2126. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MAIN_1P8_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6396. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_1P8_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.195 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register (Offset = 18144h) [reset = 80000000h]

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Table 14-6397. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8144h**

Figure 14-2127. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MAIN_1P8_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6399. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_1P8_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.196 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register (Offset = 18148h) [reset = 80000000h]

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Table 14-6400. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8148h**

Figure 14-2128. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MAIN_3P3_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6402. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_3P3_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.197 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register (Offset = 1814Ch) [reset = 80000000h]

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Table 14-6403. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 814Ch**

Figure 14-2129. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET	POK_VDDSHV_MAIN_3P3_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6405. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_3P3_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.198 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL Register (Offset = 18150h) [reset = 80000000h]

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Table 14-6406. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8150h**

Figure 14-2130. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDS_DDRIO_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDS_DDRIO_UV_CTRL_OVER_VOLT_DET	POK_VDDS_DDRIO_UV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6408. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDS_DDRIO_UV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDS_DDRIO_UV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDS_DDRIO_UV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.199 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL Register (Offset = 18154h) [reset = 80000000h]

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Table 14-6409. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8154h**

Figure 14-2131. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDS_DDRIO_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDS_DDRIO_OV_CTRL_OVER_VOLT_DET	POK_VDDS_DDRIO_OV_CTRL_POK_TRIM						
R/W	R/W						
X	X						

Table 14-6411. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDS_DDRIO_OV_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDS_DDRIO_OV_CTRL_OVER_VOLT_DET	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDS_DDRIO_OV_CTRL_POK_TRIM	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.200 MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL Register (Offset = 18160h) [reset = 80000000h]

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Table 14-6412. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8160h**

Figure 14-2132. MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_PMIC_IN_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6414. MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_PMIC_IN_CTRL_HYST_EN	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Reset Source: mod_por_rst_n
14:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.201 MCU_CTRL_MMR_CFG0_RST_CTRL Register

1 MCU_CTRL_MMR_CFG0_RST_CTRL Register (Offset = 18170h) [reset = 20FFFh]

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Table 14-6415. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8170h**

Figure 14-2133. MCU_CTRL_MMR_CFG0_RST_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td>RST_CTRL_MCU_RESET_ISO_DONE_Z</td><td>RST_CTRL_MCU_ESM_ERROR_RST_EN_Z</td><td>RST_CTRL_DMSC_COLD_RESET_EN_Z</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">RST_CTRL_SW_MCU_WARMRST</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RST_CTRL_SW_MAIN_POR</td><td colspan="4">RST_CTRL_SW_MAIN_WARMRST</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Fh</td><td colspan="4">Fh</td></tr>
</table>

Table 14-6417. MCU_CTRL_MMR_CFG0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MCU_RESET_ISO_DONE_Z	R/W	0h	MCU can set this bit to block warm reset in the main domain which is useful when the MCU may be accessing Reset Source: mcu_chip1_rst_n
17	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z	R/W	1h	Deactivate Reset of MCU by ESM Reset Source: mcu_chip1_rst_n
16	RST_CTRL_DMSC_COLD_RESET_EN_Z	R/W	0h	Deactivate Reset of MCU by DMSC Reset Source: mcu_chip1_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	RST_CTRL_SW_MCU_WARMRST	R/W	Fh	This is a fault tolerant bitfield. Reset Source: mcu_chip1_rst_n
7:4	RST_CTRL_SW_MAIN_POR	R/W	Fh	This is a fault tolerant bitfield. Reset Source: main_chip1_rst_n
3:0	RST_CTRL_SW_MAIN_WARMRST	R/W	Fh	This is a fault tolerant bitfield. Reset Source: main_chip1_rst_n

14.2.1.1.2.2.202 MCU_CTRL_MMR_CFG0_RST_STAT Register

1 MCU_CTRL_MMR_CFG0_RST_STAT Register (Offset = 18174h) [reset = 0h]

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Table 14-6418. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8174h**

Figure 14-2134. MCU_CTRL_MMR_CFG0_RST_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MAIN_RESETSTATZ
NONE							R
0h							X

Table 14-6420. MCU_CTRL_MMR_CFG0_RST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MAIN_RESETSTATZ	R	X	Status of Main Domain Reset: Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.203 MCU_CTRL_MMR_CFG0_RST_SRC Register

1 MCU_CTRL_MMR_CFG0_RST_SRC Register (Offset = 18178h) [reset = 0h]

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Table 14-6421. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8178h**

Figure 14-2135. MCU_CTRL_MMR_CFG0_RST_SRC Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR	RST_SRC_MAIN_ESM_ERROR	RESERVED				RST_SRC_SW_MAIN_POR_FROM_MAIN	RST_SRC_SW_MAIN_POR_FROM_MCU
R/W	R/W	NONE				R/W	R/W
0h	0h	0h				0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		RST_SRC_SW_MAIN_WARMRST_FROM_MAIN	RST_SRC_SW_MAIN_WARMRST_FROM_MCU	RESERVED			RST_SRC_SW_MCU_WARMRST
NONE		R/W	R/W	NONE			R/W
0h		0h	0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		RST_SRC_WARM_OUT_RST	RST_SRC_COLD_OUT_RST	RESERVED			RST_SRC_DEBUG_RST
NONE		R/W	R/W	NONE			R/W
0h		0h	0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RST_SRC_THERMAL_RST	RESERVED	RST_SRC_MAIN_RESET_REQ	RESERVED	RST_SRC_MCU_RESET_PIN
NONE			R/W	NONE	R/W	NONE	R/W
0h			0h	0h	0h	0h	0h

Table 14-6423. MCU_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR	R/W	0h	Reset Caused by MCU ESM Error Reset Source: mod_por_rst_n
30	RST_SRC_MAIN_ESM_ERROR	R/W	0h	Reset Caused by Main ESM Error Reset Source: mod_por_rst_n
29:26	RESERVED	NONE	0h	Reserved
25	RST_SRC_SW_MAIN_POR_FROM_MAIN	R/W	0h	Software Main Power On Reset From MAIN CTRL MMR Reset Source: mod_por_rst_n
24	RST_SRC_SW_MAIN_POR_FROM_MCU	R/W	0h	Software Main Power On Reset From MCU CTRL MMR Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN	R/W	0h	Software Main Warm Reset from MAIN CTRL MMR Reset Source: mod_por_rst_n

Table 14-6423. MCU_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	RST_SRC_SW_MAIN_WARMRST_FROM_MCU	R/W	0h	Software Main Warm Reset From MCU CTRL MMR Reset Source: mod_por_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST	R/W	0h	Software Warm Reset Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST	R/W	0h	DMSC Warm Reset Reset Source: mod_por_rst_n
12	RST_SRC_COLD_OUT_RST	R/W	0h	DMSC Cold Reset Reset Source: mod_por_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST	R/W	0h	Debug Subsystem Initiated Reset Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST	R/W	0h	Thermal Reset Reset Source: mod_por_rst_n
3	RESERVED	NONE	0h	Reserved
2	RST_SRC_MAIN_RESET_REQ	R/W	0h	Main Reset Pin Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN	R/W	0h	Rest Caused by MCU Reset Pin Reset Source: mod_por_rst_n

14.2.1.1.2.2.204 MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD Register

1 MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD Register (Offset = 1817Ch) [reset = 0h]

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Table 14-6424. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 817Ch**

Figure 14-2136. MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R/W							
0h							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R/W							
0h							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R/W							
0h							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R/W							
0h							

Table 14-6426. MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD	R/W	0h	After a MCU_PORz reset this bit field resets to 0x00000000. Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.205 MCU_CTRL_MMR_CFG0_ISO_CTRL Register

1 MCU_CTRL_MMR_CFG0_ISO_CTRL Register (Offset = 18180h) [reset = 0h]

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Table 14-6427. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8180h**

Figure 14-2137. MCU_CTRL_MMR_CFG0_ISO_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ISO_CTRL_MCU_DBG_ISO_EN	ISO_CTRL_MCU_RST_ISO_EN
NONE						R/W	R/W
0h						0h	0h

Table 14-6429. MCU_CTRL_MMR_CFG0_ISO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	ISO_CTRL_MCU_DBG_ISO_EN	R/W	0h	Isolates the MCU domain from Debug Reset Source: mcu_chip1_rst_n
0	ISO_CTRL_MCU_RST_ISO_EN	R/W	0h	Isolates the MCU domain from Warm Reset initiated by Main Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.206 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register

1 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register (Offset = 18190h) [reset = 0h]

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Table 14-6430. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8190h**

Figure 14-2138. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Name Register

31	30	29	28	27	26	25	24
VDD_CORE_GLDTC_CTRL_PWDB	VDD_CORE_GLDTC_CTRL_RSTB	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED					VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL		
NONE					R/W		
0h					X		

15	14	13	12	11	10	9	8
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL					
NONE		R/W					
0h		X					

7	6	5	4	3	2	1	0
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL					
NONE		R/W					
0h		X					

Table 14-6432. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VDD_CORE_GLDTC_CTRL_PWDB	R/W	0h	Power down - active low. Reset Source: mcu_chip1_rst_n
30	VDD_CORE_GLDTC_CTRL_RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must be not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. Reset Source: mcu_chip1_rst_n
29:19	RESERVED	NONE	0h	Reserved
18:16	VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth Reset Source: mcu_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage Reset Source: mcu_chip1_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.207 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT Register

1 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT Register (Offset = 181B0h) [reset = 0h]

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Table 14-6433. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 81B0h**

Figure 14-2139. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG
NONE							R
0h							X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG
NONE							R
0h							X

Table 14-6435. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. Reset Source: mcu_chip1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.208 MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Register

1 MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Register (Offset = 18200h) [reset = 2001Fh]

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Table 14-6436. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8200h**

Figure 14-2140. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PRG_PP_0_CTRL_DEGLITCH_SEL	
NONE						R/W	
0h						2h	
15	14	13	12	11	10	9	8
PRG_PP_0_CTRL_POK_EN_SEL	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN
NONE			R/W	R/W	R/W	R/W	R/W
0h			1h	1h	1h	1h	1h

Table 14-6438. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_0_CTRL_DEGLITCH_SEL	R/W	2h	Deglitch period for PRG_PP0 POKs: Reset Source: mod_por_rst_n
15	PRG_PP_0_CTRL_POK_EN_SEL	R/W	0h	Select POK active source Reset Source: mod_por_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN	R/W	1h	Active VDDA_PMIC_IN undervoltage POK detection Reset Source: mod_por_rst_n
3	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN	R/W	1h	Active VDD_MCU overvoltage POK detection Reset Source: mod_por_rst_n
2	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN	R/W	1h	Active VDD_MCU undervoltage POK detection Reset Source: mod_por_rst_n
1	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN	R/W	1h	Active 1.8V VDDA_MCU overvoltage POK detection Reset Source: mod_por_rst_n

Table 14-6438. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PRG_PP_0_CTRL_POK_ VDDA_MCU_UV_EN	R/W	1h	Active 1.8V VDDA_MCU undervoltage POK detection Reset Source: mod_por_rst_n

14.2.1.1.2.2.209 MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register

1 MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register (Offset = 18208h) [reset = 2007Fh]

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Table 14-6439. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8208h

Figure 14-2141. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PRG_PP_1_CTRL_POK_PP_EN	RESERVED	PRG_PP_1_CTRL_DEGLITCH_SEL	
NONE				R/W	NONE	R/W	
0h				0h	0h	2h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRG_PP_1_CTRL_POK_EN_SEL	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL	PRG_PP_1_CTRL_POK_VDDSHV_MCU_3P3_OV_SEL	PRG_PP_1_CTRL_POK_VDDSHV_MCU_1P8_OV_SEL	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN	PRG_PP_1_CTRL_POK_VDDSHV_MCU_3P3_EN	PRG_PP_1_CTRL_POK_VDDSHV_MCU_1P8_EN	PRG_PP_1_CTRL_POK_VDDR_CORE_EN
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	1h	1h	1h	1h	1h	1h	1h

Table 14-6441. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	PRG_PP_1_CTRL_POK_PP_EN	R/W	0h	POK ping-pong active. When set, activesautomatic switching between undervoltage andovervoltage detection on PRG_PP1 (POK_VDDR_CORE, POK_VDDSHV_MCU_1P8, POK_VDDSHV_MCU_3P3, POK_VMON_CAP_MCU_GENERAL, POK_VDDSHV_MAIN_1P8, POK_VDDSHV_MAIN_3P3, and POK_VDDS_DDRIO) POKs. This bit has no effect if the POK's ov_sel bit = 1. Reset Source: mod_por_rst_n
18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_1_CTRL_DEGLITCH_SEL	R/W	2h	Deglitch period for PRG_PP1 POKs: Reset Source: mod_por_rst_n
15	PRG_PP_1_CTRL_POK_EN_SEL	R/W	0h	Select POK active source Reset Source: mod_por_rst_n

Table 14-6441. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL	R/W	0h	POK_VDDS_DDRIO mode: Reset Source: mod_por_rst_n
13	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL	R/W	0h	POK_VDDSHV_MAIN_3P3 mode: Reset Source: mod_por_rst_n
12	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL	R/W	0h	POK_VDDSHV_MAIN_1P8 mode: Reset Source: mod_por_rst_n
11	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL	R/W	0h	POK_VMON_CAP_MCU_GENERAL mode: Reset Source: mod_por_rst_n
10	PRG_PP_1_CTRL_POK_VDDSHV_MCU_3P3_OV_SEL	R/W	0h	POK_VDDSHV_MCU_3P3 mode: Reset Source: mod_por_rst_n
9	PRG_PP_1_CTRL_POK_VDDSHV_MCU_1P8_OV_SEL	R/W	0h	POK_VDDSHV_MCU_1P8 mode: Reset Source: mod_por_rst_n
8	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL	R/W	0h	POK_VDDR_CORE Mode: Reset Source: mod_por_rst_n
7	RESERVED	NONE	0h	Reserved
6	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN	R/W	1h	Active POK_VDDS_DDRIO (if pok_en_sel = 1): Reset Source: mod_por_rst_n
5	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN	R/W	1h	Active POK_VDDSHV_MAIN_3P3 (if pok_en_sel = 1): Reset Source: mod_por_rst_n
4	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN	R/W	1h	Active POK_VDDSHV_MAIN_1P8 (if pok_en_sel = 1): Reset Source: mod_por_rst_n
3	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN	R/W	1h	Active POK_VMON_CAP_MCU_GENERAL (if pok_en_sel = 1): Reset Source: mod_por_rst_n
2	PRG_PP_1_CTRL_POK_VDDSHV_MCU_3P3_EN	R/W	1h	Active POK_VDDSHV_MCU_3P3 (if pok_en_sel = 1): Reset Source: mod_por_rst_n
1	PRG_PP_1_CTRL_POK_VDDSHV_MCU_1P8_EN	R/W	1h	Active POK_VDDSHV_MCU_1P8 (if pok_en_sel = 1): Reset Source: mod_por_rst_n
0	PRG_PP_1_CTRL_POK_VDDR_CORE_EN	R/W	1h	Active POK_VDDR_CORE (if pok_en_sel = 1): Reset Source: mod_por_rst_n

14.2.1.1.2.2.210 MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL Register

1 MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL Register (Offset = 18284h) [reset = 0h]

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Table 14-6442. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8284h**

Figure 14-2142. MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCU_CLKGATE_CTRL_MCU_M4FSS_NOGATE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>MCU_CLKGATE_CTRL_MCU_CBA_ECC_AGGR_NOGATE</td><td>MCU_CLKGATE_CTRL_MCU_CBA_NOGATE</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>X</td></tr>
</table>

Table 14-6444. MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_CLKGATE_CTRL_MCU_M4FSS_NOGATE	R/W	X	MCU domain M4FSS0 clock gate deactivate. Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1	MCU_CLKGATE_CTRL_MCU_CBA_ECC_AGGR_NOGATE	R/W	X	MCU domain Pulsar clock gate deactivate. Reset Source: mod_por_rst_n
0	MCU_CLKGATE_CTRL_MCU_CBA_NOGATE	R/W	X	MCU domain Data bus (mcu_cbass) clock gate deactivate. Reset Source: mod_por_rst_n

14.2.1.1.2.2.211 MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0 Register

1 MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0 Register (Offset = 18288h) [reset = 0h]

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Table 14-6445. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 8288h**

Figure 14-2143. MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0 Name Register

31	30	29	28	27	26	25	24
MAIN_CLKGATE_CTRL0_MAIN_DMSC_NOGATE	RESERVED		MAIN_CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE	RESERVED	MAIN_CLKGATE_CTRL0_MAIN_R5FSS1_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_R5FSS0_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_TIMERMGR_NOGATE
R/W	NONE		R/W	NONE	R/W	R/W	R/W
X	0h		X	0h	X	X	X
23	22	21	20	19	18	17	16
RESERVED		MAIN_CLKGATE_CTRL0_MAIN_ICSSG1_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_ICSSG0_NOGATE	RESERVED	MAIN_CLKGATE_CTRL0_MAIN_PDMA1_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_PDMA0_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_DMSS_NOGATE
NONE		R/W	R/W	NONE	R/W	R/W	R/W
0h		X	X	0h	X	X	X
15	14	13	12	11	10	9	8
MAIN_CLKGATE_CTRL0_MAIN_GIC500_NOGATE	RESERVED				MAIN_CLKGATE_CTRL0_MAIN_A53_0_DBG_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_A53_0_CFG_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_A53_0_ACP_NOGATE
R/W	NONE				R/W	R/W	R/W
X	0h				X	X	X
7	6	5	4	3	2	1	0
MAIN_CLKGATE_CTRL0_MAIN_A53_0_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_CBA_ECC_AGG_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE	MAIN_CLKGATE_CTRL0_MAIN_CBA_NOGATE	RESERVED	MAIN_CLKGATE_CTRL0_MAIN_INFRA_ECC_AGG_NOGATE	RESERVED	MAIN_CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE
R/W	R/W	R/W	R/W	NONE	R/W	NONE	R/W
X	X	X	X	0h	X	0h	X

Table 14-6447. MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_CLKGATE_CTRL0_MAIN_DMSC_NOGATE	R/W	X	MAIN domain DMSC (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
30:29	RESERVED	NONE	0h	Reserved
28	MAIN_CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE	R/W	X	MAIN domain Debug bus clock gate deactivate. Reset Source: mod_por_rst_n
27	RESERVED	NONE	0h	Reserved
26	MAIN_CLKGATE_CTRL0_MAIN_R5FSS1_NOGATE	R/W	X	MAIN domain R5FSS1 clock gate deactivate. Reset Source: mod_por_rst_n

Table 14-6447. MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	MAIN_CLKGATE_CTRL0_MAIN_R5FSS0_NOGATE	R/W	X	MAIN domain R5FSS0 clock gate deactivate. Reset Source: mod_por_rst_n
24	MAIN_CLKGATE_CTRL0_MAIN_TIMERMGR_NOGATE	R/W	X	MAIN domain TIMERMGR (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	MAIN_CLKGATE_CTRL0_MAIN_ICSSG1_NOGATE	R/W	X	MAIN domain ICSSG1 clock gate deactivate. Reset Source: mod_por_rst_n
20	MAIN_CLKGATE_CTRL0_MAIN_ICSSG0_NOGATE	R/W	X	MAIN domain ICSSG0 clock gate deactivate. Reset Source: mod_por_rst_n
19	RESERVED	NONE	0h	Reserved
18	MAIN_CLKGATE_CTRL0_MAIN_PDMA1_NOGATE	R/W	X	MAIN domain PDMA1 (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
17	MAIN_CLKGATE_CTRL0_MAIN_PDMA0_NOGATE	R/W	X	MAIN domain PDMA0 (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
16	MAIN_CLKGATE_CTRL0_MAIN_DMSS_NOGATE	R/W	X	MAIN domain DMSS (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
15	MAIN_CLKGATE_CTRL0_MAIN_GIC500_NOGATE	R/W	X	MAIN A53SS0 (gic500_1_2) clock gate deactivate. Reset Source: mod_por_rst_n
14:11	RESERVED	NONE	0h	Reserved
10	MAIN_CLKGATE_CTRL0_MAIN_A53_0_DBG_NOGATE	R/W	X	MAIN A53SS0 Debug Port clock gate deactivate. Reset Source: mod_por_rst_n
9	MAIN_CLKGATE_CTRL0_MAIN_A53_0_CFG_NOGATE	R/W	X	MAIN A53SS0 Configuration Port clock gate deactivate. Reset Source: mod_por_rst_n
8	MAIN_CLKGATE_CTRL0_MAIN_A53_0_ACP_NOGATE	R/W	X	MAIN A53SS0 ACP clock gate deactivate. Reset Source: mod_por_rst_n
7	MAIN_CLKGATE_CTRL0_MAIN_A53_0_NOGATE	R/W	X	MAIN A53SS0 clock gate deactivate. Reset Source: mod_por_rst_n
6	MAIN_CLKGATE_CTRL0_MAIN_CBA_ECC_AGG_NOGATE	R/W	X	MAIN domain data bus ECC aggragator (main_cba_ecc_aggr_main_0) clock gate deactivate. Reset Source: mod_por_rst_n
5	MAIN_CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE	R/W	X	MAIN domain datal bus (main_fw_cbass) clock gate deactivate. Reset Source: mod_por_rst_n
4	MAIN_CLKGATE_CTRL0_MAIN_CBA_NOGATE	R/W	X	MAIN domain data bus (main_cbass) clock gate deactivate. Reset Source: mod_por_rst_n
3	RESERVED	NONE	0h	Reserved
2	MAIN_CLKGATE_CTRL0_MAIN_INFRA_ECC_AGG_NOGATE	R/W	X	MAIN domain Infrastructure ECC aggragator (main_infra_ecc_aggr) clock gate deactivate. Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	MAIN_CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE	R/W	X	MAIN domain Infrastructure bus (main_infra_cbass) clock gate deactivate. Reset Source: mod_por_rst_n

14.2.1.1.2.2.212 MCU_CTRL_MMR_CFG0_LOCK6_KICK0 Register

1 MCU_CTRL_MMR_CFG0_LOCK6_KICK0 Register (Offset = 19008h) [reset = 0h]

- KICK0 component

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Table 14-6448. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9008h**

Figure 14-2144. MCU_CTRL_MMR_CFG0_LOCK6_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0							
R/W							
0h							

Table 14-6450. MCU_CTRL_MMR_CFG0_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.213 MCU_CTRL_MMR_CFG0_LOCK6_KICK1 Register

1 MCU_CTRL_MMR_CFG0_LOCK6_KICK1 Register (Offset = 1900Ch) [reset = 0h]

- KICK1 component

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Table 14-6451. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 900Ch**

Figure 14-2145. MCU_CTRL_MMR_CFG0_LOCK6_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1							
R/W							
0h							

Table 14-6453. MCU_CTRL_MMR_CFG0_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.214 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register (Offset = 19100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6454. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9100h**

Figure 14-2146. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0_READONLY							
R							
0h							

Table 14-6456. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.215 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register (Offset = 19104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6457. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9104h**

Figure 14-2147. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P6_R1_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P6_R1_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P6_R1_READONLY							
R							
0h							

Table 14-6459. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.216 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register (Offset = 19108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6460. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9108h**

Figure 14-2148. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2_READONLY							
R							
0h							

Table 14-6462. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.217 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register (Offset = 1910Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-6463. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 910Ch**

Figure 14-2149. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3_READONLY							
R							
0h							

Table 14-6465. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.218 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register (Offset = 19110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6466. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9110h**

Figure 14-2150. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4_READONLY							
R							
0h							

Table 14-6468. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.219 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register (Offset = 19114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6469. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 9114h**

Figure 14-2151. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6471. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.220 MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Register (Offset = 1A000h) [reset = 10h]

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Table 14-6472. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A000h**

Figure 14-2152. MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED		POR_CTRL_OVRD_SET5_PROXY	POR_CTRL_OVRD_SET4_PROXY	POR_CTRL_OVRD_SET3_PROXY	POR_CTRL_OVRD_SET2_PROXY	POR_CTRL_OVRD_SET1_PROXY	POR_CTRL_OVRD_SET0_PROXY
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		POR_CTRL_OVRD5_PROXY	POR_CTRL_OVRD4_PROXY	POR_CTRL_OVRD3_PROXY	POR_CTRL_OVRD2_PROXY	POR_CTRL_OVRD1_PROXY	POR_CTRL_OVRD0_PROXY
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POR_CTRL_TRIM_SEL_PROXY	RESERVED		POR_CTRL_MASK_HHV_PROXY	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		1h	0h			

Table 14-6474. MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	POR_CTRL_OVRD_SET5_PROXY	R/W	0h	Reserved override set Reset Source: mod_por_rst_n
28	POR_CTRL_OVRD_SET4_PROXY	R/W	0h	POKLVB override set Reset Source: mod_por_rst_n
27	POR_CTRL_OVRD_SET3_PROXY	R/W	0h	POKLVA override set Reset Source: mod_por_rst_n
26	POR_CTRL_OVRD_SET2_PROXY	R/W	0h	POKHV override set Reset Source: mod_por_rst_n
25	POR_CTRL_OVRD_SET1_PROXY	R/W	0h	BGOK override set Reset Source: mod_por_rst_n
24	POR_CTRL_OVRD_SET0_PROXY	R/W	0h	PORHV override set Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-6474. MCU_CTRL_MMR_CFG0_POR_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	POR_CTRL_OVRD5_PROXY	R/W	0h	Reserved override active Reset Source: mod_por_rst_n
20	POR_CTRL_OVRD4_PROXY	R/W	0h	POKLVB override active Reset Source: mod_por_rst_n
19	POR_CTRL_OVRD3_PROXY	R/W	0h	POKLVA override active Reset Source: mod_por_rst_n
18	POR_CTRL_OVRD2_PROXY	R/W	0h	POKHV override active Reset Source: mod_por_rst_n
17	POR_CTRL_OVRD1_PROXY	R/W	0h	BGOK override active Reset Source: mod_por_rst_n
16	POR_CTRL_OVRD0_PROXY	R/W	0h	PORHV override active Reset Source: mod_por_rst_n
15:8	RESERVED	NONE	0h	Reserved
7	POR_CTRL_TRIM_SEL_PROXY	R/W	0h	POR Trim Select Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	POR_CTRL_MASK_HHV_PROXY	R/W	1h	Mask HHV/SOC_PORz outputs when applying new trim values Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.221 MCU_CTRL_MMR_CFG0_POR_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_POR_STAT_PROXY Register (Offset = 1A004h) [reset = 0h]

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Table 14-6475. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A004h**

Figure 14-2153. MCU_CTRL_MMR_CFG0_POR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							POR_STAT_BGOK_PROXY
NONE							R
0h							X
7	6	5	4	3	2	1	0
RESERVED			POR_STAT_SOC_POR_PROXY	RESERVED			
NONE			R	NONE			
0h			X	0h			

Table 14-6477. MCU_CTRL_MMR_CFG0_POR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	POR_STAT_BGOK_PROXY	R	X	Bandgap OK status Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	POR_STAT_SOC_POR_PROXY	R	X	POR module status Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.222 MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY Register (Offset = 1A100h) [reset = 0h]

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Table 14-6478. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A100h**

Figure 14-2154. MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				POR_BANDGAP_CTRL_BGAPI_PROXY			
NONE				R/W			
0h				X			
15	14	13	12	11	10	9	8
POR_BANDGAP_CTRL_BGAPV_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
POR_BANDGAP_CTRL_BGAPC_PROXY							
R/W							
X							

Table 14-6480. MCU_CTRL_MMR_CFG0_POR_BANDGAP_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	POR_BANDGAP_CTRL_BGAPI_PROXY	R/W	X	Bandgap output current trim bits Reset Source: mod_por_rst_n
15:8	POR_BANDGAP_CTRL_BGAPV_PROXY	R/W	X	Bandgap output voltage magnitude trim bits Reset Source: mod_por_rst_n
7:0	POR_BANDGAP_CTRL_BGAPC_PROXY	R/W	X	Bandgap slope trim bits. Bit7 is used to calculate the offset Reset Source: mod_por_rst_n

14.2.1.1.2.2.223 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register (Offset = 1A110h) [reset = 80000000h]

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Table 14-6481. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A110h**

Figure 14-2155. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDA_MCU_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6483. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDA_MCU_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.224 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register (Offset = 1A114h) [reset = 80000000h]

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Table 14-6484. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A114h**

Figure 14-2156. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDA_MCU_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6486. MCU_CTRL_MMR_CFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDA_MCU_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.225 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY Register (Offset = 1A118h) [reset = 80000000h]

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Table 14-6487. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A118h**

Figure 14-2157. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDD_CORE_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6489. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDD_CORE_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.226 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY Register (Offset = 1A11Ch) [reset = 80000000h]

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Table 14-6490. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A11Ch**

Figure 14-2158. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDD_CORE_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6492. MCU_CTRL_MMR_CFG0_POK_VDD_CORE_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDD_CORE_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.227 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register (Offset = 1A120h) [reset = 80000000h]

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Table 14-6493. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A120h**

Figure 14-2159. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDR_CORE_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6495. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDR_CORE_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.228 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register (Offset = 1A124h) [reset = 80000000h]

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Table 14-6496. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A124h**

Figure 14-2160. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDR_CORE_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6498. MCU_CTRL_MMR_CFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDR_CORE_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.229 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL_PROXY Register (Offset = 1A128h) [reset = 80000000h]

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Table 14-6499. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A128h**

Figure 14-2161. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MCU_1P8_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MCU_1P8_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MCU_1P8_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6501. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MCU_1P8_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MCU_1P8_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MCU_1P8_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.230 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL_PROXY Register (Offset = 1A12Ch) [reset = 80000000h]

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Table 14-6502. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A12Ch**

Figure 14-2162. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MCU_1P8_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MCU_1P8_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MCU_1P8_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6504. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_1P8_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MCU_1P8_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MCU_1P8_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MCU_1P8_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.231 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL_PROXY Register (Offset = 1A130h) [reset = 80000000h]

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Table 14-6505. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A130h**

Figure 14-2163. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MCU_3P3_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MCU_3P3_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MCU_3P3_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6507. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MCU_3P3_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MCU_3P3_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MCU_3P3_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.232 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL_PROXY Register (Offset = 1A134h) [reset = 80000000h]

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Table 14-6508. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A134h**

Figure 14-2164. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MCU_3P3_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MCU_3P3_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MCU_3P3_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6510. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MCU_3P3_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MCU_3P3_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MCU_3P3_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MCU_3P3_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.233 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register (Offset = 1A138h) [reset = 80000000h]

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Table 14-6511. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A138h**

Figure 14-2165. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6513. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.234 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register (Offset = 1A13Ch) [reset = 80000000h]

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Table 14-6514. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A13Ch**

Figure 14-2166. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6516. MCU_CTRL_MMR_CFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.235 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register (Offset = 1A140h) [reset = 80000000h]

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Table 14-6517. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A140h**

Figure 14-2167. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MAIN_1P8_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6519. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_1P8_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.236 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register (Offset = 1A144h) [reset = 80000000h]

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Table 14-6520. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A144h**

Figure 14-2168. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MAIN_1P8_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6522. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_1P8_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.237 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register (Offset = 1A148h) [reset = 80000000h]

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Table 14-6523. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A148h**

Figure 14-2169. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MAIN_3P3_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6525. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_3P3_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.238 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register (Offset = 1A14Ch) [reset = 80000000h]

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Table 14-6526. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A14Ch**

Figure 14-2170. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDSHV_MAIN_3P3_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6528. MCU_CTRL_MMR_CFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDSHV_MAIN_3P3_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.239 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY Register (Offset = 1A150h) [reset = 80000000h]

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Table 14-6529. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A150h**

Figure 14-2171. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDS_DDRIO_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDS_DDRIO_UV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDS_DDRIO_UV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6531. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDS_DDRIO_UV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDS_DDRIO_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDS_DDRIO_UV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.240 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY Register (Offset = 1A154h) [reset = 80000000h]

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Table 14-6532. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A154h**

Figure 14-2172. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDS_DDRIO_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDS_DDRIO_OV_CTRL_OVER_VOLT_DET_PROXY	POK_VDDS_DDRIO_OV_CTRL_POK_TRIM_PROXY						
R/W	R/W						
X	X						

Table 14-6534. MCU_CTRL_MMR_CFG0_POK_VDDS_DDRIO_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDS_DDRIO_OV_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDS_DDRIO_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	X	Over / under voltage detection mode Reset Source: mod_por_rst_n
6:0	POK_VDDS_DDRIO_OV_CTRL_POK_TRIM_PROXY	R/W	X	POK Trim Bits Reset Source: mod_por_rst_n

14.2.1.1.2.2.241 MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register (Offset = 1A160h) [reset = 80000000h]

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Table 14-6535. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A160h**

Figure 14-2173. MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_PMIC_IN_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-6537. MCU_CTRL_MMR_CFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_PMIC_IN_CTRL_HYST_EN_PROXY	R/W	1h	Active POK hysteresis Reset Source: mod_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Reset Source: mod_por_rst_n
14:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.242 MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Register (Offset = 1A170h) [reset = 20FFFh]

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Table 14-6538. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A170h**

Figure 14-2174. MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					RST_CTRL_MCU_RESET_ISO_DONE_Z_PROXY	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z_PROXY	RST_CTRL_DMSC_COLD_RESET_EN_Z_PROXY
NONE					R/W	R/W	R/W
0h					0h	1h	0h
15	14	13	12	11	10	9	8
RESERVED				RST_CTRL_SW_MCU_WARMRST_PROXY			
NONE				R/W			
0h				Fh			
7	6	5	4	3	2	1	0
RST_CTRL_SW_MAIN_POR_PROXY				RST_CTRL_SW_MAIN_WARMRST_PROXY			
R/W				R/W			
Fh				Fh			

Table 14-6540. MCU_CTRL_MMR_CFG0_RST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MCU_RESET_ISO_DONE_Z_PROXY	R/W	0h	MCU can set this bit to block warm reset in the main domain which is useful when the MCU may be accessing Reset Source: mcu_chip1_rst_n
17	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z_PROXY	R/W	1h	Deactivate Reset of MCU by ESM Reset Source: mcu_chip1_rst_n
16	RST_CTRL_DMSC_COLD_RESET_EN_Z_PROXY	R/W	0h	Deactivate Reset of MCU by DMSC Reset Source: mcu_chip1_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	RST_CTRL_SW_MCU_WARMRST_PROXY	R/W	Fh	This is a fault tolerant bitfield. Reset Source: mcu_chip1_rst_n
7:4	RST_CTRL_SW_MAIN_POR_PROXY	R/W	Fh	This is a fault tolerant bitfield. Reset Source: main_chip1_rst_n
3:0	RST_CTRL_SW_MAIN_WARMRST_PROXY	R/W	Fh	This is a fault tolerant bitfield. Reset Source: main_chip1_rst_n

14.2.1.1.2.2.243 *MCU_CTRL_MMR_CFG0_RST_STAT_PROXY Register*

1 MCU_CTRL_MMR_CFG0_RST_STAT_PROXY Register (Offset = 1A174h) [reset = 0h]

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Table 14-6541. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A174h**

Figure 14-2175. MCU_CTRL_MMR_CFG0_RST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MAIN_RESETSTATZ_PROXY
NONE							R
0h							X

Table 14-6543. MCU_CTRL_MMR_CFG0_RST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MAIN_RESETSTATZ_PROXY	R	X	Status of Main Domain Reset: Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.244 MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Register

1 MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Register (Offset = 1A178h) [reset = 0h]

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Table 14-6544. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A178h**

Figure 14-2176. MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR_PROXY	RST_SRC_MAIN_ESM_ERROR_PROXY	RESERVED				RST_SRC_SW_MAIN_POR_FROM_MAIN_PROXY	RST_SRC_SW_MAIN_POR_FROM_MCU_PROXY
R/W	R/W	NONE				R/W	R/W
0h	0h	0h				0h	0h
23	22	21	20	19	18	17	16
RESERVED		RST_SRC_SW_MAIN_WARMRST_FROM_MAIN_PROXY	RST_SRC_SW_MAIN_WARMRST_FROM_MCU_PROXY	RESERVED			RST_SRC_SW_MCU_WARMRST_PROXY
NONE		R/W	R/W	NONE			R/W
0h		0h	0h	0h			0h
15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST_PROXY	RST_SRC_COLD_OUT_RST_PROXY	RESERVED			RST_SRC_DEBUG_RST_PROXY
NONE		R/W	R/W	NONE			R/W
0h		0h	0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			RST_SRC_THERMAL_RST_PROXY	RESERVED	RST_SRC_MAIN_RESET_REQ_PROXY	RESERVED	RST_SRC_MCU_RESET_PIN_PROXY
NONE			R/W	NONE	R/W	NONE	R/W
0h			0h	0h	0h	0h	0h

Table 14-6546. MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR_PROXY	R/W	0h	Reset Caused by MCU ESM Error Reset Source: mod_por_rst_n
30	RST_SRC_MAIN_ESM_ERROR_PROXY	R/W	0h	Reset Caused by Main ESM Error Reset Source: mod_por_rst_n
29:26	RESERVED	NONE	0h	Reserved
25	RST_SRC_SW_MAIN_POR_FROM_MAIN_PROXY	R/W	0h	Software Main Power On Reset From MAIN CTRL MMR Reset Source: mod_por_rst_n
24	RST_SRC_SW_MAIN_POR_FROM_MCU_PROXY	R/W	0h	Software Main Power On Reset From MCU CTRL MMR Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-6546. MCU_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	RST_SRC_SW_MAIN_WARMRST_FROM_MAIN_PROXY	R/W	0h	Software Main Warm Reset from MAIN CTRL MMR Reset Source: mod_por_rst_n
20	RST_SRC_SW_MAIN_WARMRST_FROM_MCU_PROXY	R/W	0h	Software Main Warm Reset From MCU CTRL MMR Reset Source: mod_por_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST_PROXY	R/W	0h	Software Warm Reset Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST_PROXY	R/W	0h	DMSC Warm Reset Reset Source: mod_por_rst_n
12	RST_SRC_COLD_OUT_RST_PROXY	R/W	0h	DMSC Cold Reset Reset Source: mod_por_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST_PROXY	R/W	0h	Debug Subsystem Initiated Reset Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST_PROXY	R/W	0h	Thermal Reset Reset Source: mod_por_rst_n
3	RESERVED	NONE	0h	Reserved
2	RST_SRC_MAIN_RESET_REQ_PROXY	R/W	0h	Main Reset Pin Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN_PROXY	R/W	0h	Rest Caused by MCU Reset Pin Reset Source: mod_por_rst_n

14.2.1.1.2.2.245 MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register

1 MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register (Offset = 1A17Ch) [reset = 0h]

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Table 14-6547. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A17Ch**

Figure 14-2177. MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R/W							
0h							

Table 14-6549. MCU_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY	R/W	0h	After a MCU_PORz reset this bit field resets to 0x00000000. Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.246 MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY Register (Offset = 1A180h) [reset = 0h]

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Table 14-6550. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A180h**

Figure 14-2178. MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ISO_CTRL_MCU_DBG_ISO_EN_PROXY	ISO_CTRL_MCU_RST_ISO_EN_PROXY
NONE						R/W	R/W
0h						0h	0h

Table 14-6552. MCU_CTRL_MMR_CFG0_ISO_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	ISO_CTRL_MCU_DBG_ISO_EN_PROXY	R/W	0h	Isolates the MCU domain from Debug Reset Source: mcu_chip1_rst_n
0	ISO_CTRL_MCU_RST_ISO_EN_PROXY	R/W	0h	Isolates the MCU domain from Warm Reset initiated by Main Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.247 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register (Offset = 1A190h) [reset = 0h]

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Table 14-6553. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A190h**

Figure 14-2179. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
VDD_CORE_GLDTC_CTRL_PWDB_PROXY	VDD_CORE_GLDTC_CTRL_RSTB_PROXY	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED					VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL_PROXY		
NONE					R/W		
0h					X		
15	14	13	12	11	10	9	8
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL_PROXY					
NONE		R/W					
0h		X					
7	6	5	4	3	2	1	0
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL_PROXY					
NONE		R/W					
0h		X					

Table 14-6555. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VDD_CORE_GLDTC_CTRL_PWDB_PROXY	R/W	0h	Power down - active low. Reset Source: mcu_chip1_rst_n
30	VDD_CORE_GLDTC_CTRL_RSTB_PROXY	R/W	0h	Reset - active low. To ensure proper operation, rstb must be not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. Reset Source: mcu_chip1_rst_n
29:19	RESERVED	NONE	0h	Reserved
18:16	VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL_PROXY	R/W	X	Selects the glitch detect low-pass filter bandwidth Reset Source: mcu_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL_PROXY	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage Reset Source: mcu_chip1_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-6555. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL_PROXY	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.248 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY Register

1 MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY Register (Offset = 1A1B0h) [reset = 0h]

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Table 14-6556. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A1B0h**

Figure 14-2180. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_PROXY
NONE							R
0h							X
7	6	5	4	3	2	1	0
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_PROXY
NONE							R
0h							X

Table 14-6558. MCU_CTRL_MMR_CFG0_VDD_CORE_GLDTC_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_PROXY	R	X	High voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. Reset Source: mcu_chip1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_PROXY	R	X	Low voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.249 MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Register (Offset = 1A200h) [reset = 2001Fh]

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Table 14-6559. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A200h**

Figure 14-2181. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PRG_PP_0_CTRL_DEGLITCH_SEL_PROXY	
NONE						R/W	
0h						2h	
15	14	13	12	11	10	9	8
PRG_PP_0_CTRL_POK_EN_SEL_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN_PROXY	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN_PROXY	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN_PROXY	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN_PROXY	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN_PROXY
NONE			R/W	R/W	R/W	R/W	R/W
0h			1h	1h	1h	1h	1h

Table 14-6561. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_0_CTRL_DEGLITCH_SEL_PROXY	R/W	2h	Deglitch period for PRG_PP0 POKs: Reset Source: mod_por_rst_n
15	PRG_PP_0_CTRL_POK_EN_SEL_PROXY	R/W	0h	Select POK active source Reset Source: mod_por_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN_PROXY	R/W	1h	Active VDDA_PMIC_IN undervoltage POK detection Reset Source: mod_por_rst_n
3	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN_PROXY	R/W	1h	Active VDD_MCU overvoltage POK detection Reset Source: mod_por_rst_n
2	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN_PROXY	R/W	1h	Active VDD_MCU undervoltage POK detection Reset Source: mod_por_rst_n

Table 14-6561. MCU_CTRL_MMR_CFG0_PRG_PP_0_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN_PROXY	R/W	1h	Active 1.8V VDDA_MCU overvoltage POK detection Reset Source: mod_por_rst_n
0	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN_PROXY	R/W	1h	Active 1.8V VDDA_MCU undervoltage POK detection Reset Source: mod_por_rst_n

14.2.1.1.2.2.250 MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register (Offset = 1A208h) [reset = 2007Fh]

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Table 14-6562. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A208h**

Figure 14-2182. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PRG_PP_1_CTRL_POK_PP_EN_PROXY	RESERVED	PRG_PP_1_CTRL_DEGLITCH_SEL_PROXY	
NONE				R/W	NONE	R/W	
0h				0h	0h	2h	
15	14	13	12	11	10	9	8
PRG_PP_1_CTRL_POK_EN_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MCU_3P3_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MCU_1P8_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN_PROXY	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MCU_3P3_EN_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MCU_1P8_EN_PROXY	PRG_PP_1_CTRL_POK_VDDR_CORE_EN_PROXY
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	1h	1h	1h	1h	1h	1h	1h

Table 14-6564. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	PRG_PP_1_CTRL_POK_PP_EN_PROXY	R/W	0h	POK ping-pong active. When set, activesautomatic switching between undervoltage andovervoltage detection on PRG_PP1 (POK_VDDR_CORE, POK_VDDSHV_MCU_1P8, POK_VDDSHV_MCU_3P3, POK_VMON_CAP_MCU_GENERAL, POK_VDDSHV_MAIN_1P8, POK_VDDSHV_MAIN_3P3, and POK_VDDS_DDRIO) POKs. This bit has no effect if the POK's ov_sel bit = 1. Reset Source: mod_por_rst_n
18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_1_CTRL_DEGLITCH_SEL_PROXY	R/W	2h	Deglitch period for PRG_PP1 POKs: Reset Source: mod_por_rst_n
15	PRG_PP_1_CTRL_POK_EN_SEL_PROXY	R/W	0h	Select POK active source Reset Source: mod_por_rst_n

Table 14-6564. MCU_CTRL_MMR_CFG0_PRG_PP_1_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL_PROXY	R/W	0h	POK_VDDS_DDRIO mode: Reset Source: mod_por_rst_n
13	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL_PROXY	R/W	0h	POK_VDDSHV_MAIN_3P3 mode: Reset Source: mod_por_rst_n
12	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL_PROXY	R/W	0h	POK_VDDSHV_MAIN_1P8 mode: Reset Source: mod_por_rst_n
11	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL_PROXY	R/W	0h	POK_VMON_CAP_MCU_GENERAL mode: Reset Source: mod_por_rst_n
10	PRG_PP_1_CTRL_POK_VDDSHV_MCU_3P3_OV_SEL_PROXY	R/W	0h	POK_VDDSHV_MCU_3P3 mode: Reset Source: mod_por_rst_n
9	PRG_PP_1_CTRL_POK_VDDSHV_MCU_1P8_OV_SEL_PROXY	R/W	0h	POK_VDDSHV_MCU_1P8 mode: Reset Source: mod_por_rst_n
8	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL_PROXY	R/W	0h	POK_VDDR_CORE Mode: Reset Source: mod_por_rst_n
7	RESERVED	NONE	0h	Reserved
6	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN_PROXY	R/W	1h	Active POK_VDDS_DDRIO (if pok_en_sel = 1): Reset Source: mod_por_rst_n
5	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN_PROXY	R/W	1h	Active POK_VDDSHV_MAIN_3P3 (if pok_en_sel = 1): Reset Source: mod_por_rst_n
4	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN_PROXY	R/W	1h	Active POK_VDDSHV_MAIN_1P8 (if pok_en_sel = 1): Reset Source: mod_por_rst_n
3	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN_PROXY	R/W	1h	Active POK_VMON_CAP_MCU_GENERAL (if pok_en_sel = 1): Reset Source: mod_por_rst_n
2	PRG_PP_1_CTRL_POK_VDDSHV_MCU_3P3_EN_PROXY	R/W	1h	Active POK_VDDSHV_MCU_3P3 (if pok_en_sel = 1): Reset Source: mod_por_rst_n
1	PRG_PP_1_CTRL_POK_VDDSHV_MCU_1P8_EN_PROXY	R/W	1h	Active POK_VDDSHV_MCU_1P8 (if pok_en_sel = 1): Reset Source: mod_por_rst_n
0	PRG_PP_1_CTRL_POK_VDDR_CORE_EN_PROXY	R/W	1h	Active POK_VDDR_CORE (if pok_en_sel = 1): Reset Source: mod_por_rst_n

14.2.1.1.2.2.251 MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL_PROXY Register

1 MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL_PROXY Register (Offset = 1A284h) [reset = 0h]

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Table 14-6565. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A284h**

Figure 14-2183. MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							MCU_CLKGATE_CTRL_MCU_M4FSS_NOGATE_PROXY
NONE							R/W
0h							X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						MCU_CLKGATE_CTRL_MCU_CBA_ECC_AGGR_NOGATE_PROXY	MCU_CLKGATE_CTRL_MCU_CBA_NOGATE_PROXY
NONE						R/W	R/W
0h						X	X

Table 14-6567. MCU_CTRL_MMR_CFG0_MCU_CLKGATE_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MCU_CLKGATE_CTRL_MCU_M4FSS_NOGATE_PROXY	R/W	X	MCU domain M4FSS0 clock gate deactivate. Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1	MCU_CLKGATE_CTRL_MCU_CBA_ECC_AGGR_NOGATE_PROXY	R/W	X	MCU domain Pulsar clock gate deactivate. Reset Source: mod_por_rst_n
0	MCU_CLKGATE_CTRL_MCU_CBA_NOGATE_PROXY	R/W	X	MCU domain Data bus (mcu_cbass) clock gate deactivate. Reset Source: mod_por_rst_n

14.2.1.1.2.2.252 MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0_PROXY Register

1 MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0_PROXY Register (Offset = 1A288h) [reset = 0h]

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Table 14-6568. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 A288h**

Figure 14-2184. MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_CLKGATE_CTRL0_MAIN_DMSC_NOGATE_PROXY	RESERVED		MAIN_CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE_PROXY	RESERVED	MAIN_CLKGATE_CTRL0_MAIN_R5FSS1_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_R5FSS0_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_TIMERMGR_NOGATE_PROXY
R/W	NONE		R/W	NONE	R/W	R/W	R/W
X	0h		X	0h	X	X	X
23	22	21	20	19	18	17	16
RESERVED		MAIN_CLKGATE_CTRL0_MAIN_ICSSG1_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_ICSSG0_NOGATE_PROXY	RESERVED	MAIN_CLKGATE_CTRL0_MAIN_PDMA1_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_PDMA0_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_DMSS_NOGATE_PROXY
NONE		R/W	R/W	NONE	R/W	R/W	R/W
0h		X	X	0h	X	X	X
15	14	13	12	11	10	9	8
MAIN_CLKGATE_CTRL0_MAIN_GIC500_NOGATE_PROXY	RESERVED				MAIN_CLKGATE_CTRL0_MAIN_A53_0_DBG_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_A53_0_CFG_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_A53_0_ACP_NOGATE_PROXY
R/W	NONE				R/W	R/W	R/W
X	0h				X	X	X
7	6	5	4	3	2	1	0
MAIN_CLKGATE_CTRL0_MAIN_A53_0_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_CBA_ECC_AGG_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE_PROXY	MAIN_CLKGATE_CTRL0_MAIN_CBA_NOGATE_PROXY	RESERVED	MAIN_CLKGATE_CTRL0_MAIN_INFRA_ECC_AGG_NOGATE_PROXY	RESERVED	MAIN_CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE_PROXY
R/W	R/W	R/W	R/W	NONE	R/W	NONE	R/W
X	X	X	X	0h	X	0h	X

Table 14-6570. MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_CLKGATE_CTRL0_MAIN_DMSC_NOGATE_PROXY	R/W	X	MAIN domain DMSC (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
30:29	RESERVED	NONE	0h	Reserved
28	MAIN_CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE_PROXY	R/W	X	MAIN domain Debug bus clock gate deactivate. Reset Source: mod_por_rst_n
27	RESERVED	NONE	0h	Reserved

Table 14-6570. MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	MAIN_CLKGATE_CTRL0_MAIN_R5FSS1_NOGATE_PROXY	R/W	X	MAIN domain R5FSS1 clock gate deactivate. Reset Source: mod_por_rst_n
25	MAIN_CLKGATE_CTRL0_MAIN_R5FSS0_NOGATE_PROXY	R/W	X	MAIN domain R5FSS0 clock gate deactivate. Reset Source: mod_por_rst_n
24	MAIN_CLKGATE_CTRL0_MAIN_TIMERMGR_NOGATE_PROXY	R/W	X	MAIN domain TIMERMGR (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	MAIN_CLKGATE_CTRL0_MAIN_ICSSG1_NOGATE_PROXY	R/W	X	MAIN domain ICSSG1 clock gate deactivate. Reset Source: mod_por_rst_n
20	MAIN_CLKGATE_CTRL0_MAIN_ICSSG0_NOGATE_PROXY	R/W	X	MAIN domain ICSSG0 clock gate deactivate. Reset Source: mod_por_rst_n
19	RESERVED	NONE	0h	Reserved
18	MAIN_CLKGATE_CTRL0_MAIN_PDMA1_NOGATE_PROXY	R/W	X	MAIN domain PDMA1 (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
17	MAIN_CLKGATE_CTRL0_MAIN_PDMA0_NOGATE_PROXY	R/W	X	MAIN domain PDMA0 (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
16	MAIN_CLKGATE_CTRL0_MAIN_DMSS_NOGATE_PROXY	R/W	X	MAIN domain DMSS (pwr_dis_nogate) clock gate deactivate. Reset Source: mod_por_rst_n
15	MAIN_CLKGATE_CTRL0_MAIN_GIC500_NOGATE_PROXY	R/W	X	MAIN A53SS0 (gic500_1_2) clock gate deactivate. Reset Source: mod_por_rst_n
14:11	RESERVED	NONE	0h	Reserved
10	MAIN_CLKGATE_CTRL0_MAIN_A53_0_DBG_NOGATE_PROXY	R/W	X	MAIN A53SS0 Debug Port clock gate deactivate. Reset Source: mod_por_rst_n
9	MAIN_CLKGATE_CTRL0_MAIN_A53_0_CFG_NOGATE_PROXY	R/W	X	MAIN A53SS0 Configuration Port clock gate deactivate. Reset Source: mod_por_rst_n
8	MAIN_CLKGATE_CTRL0_MAIN_A53_0_ACP_NOGATE_PROXY	R/W	X	MAIN A53SS0 ACP clock gate deactivate. Reset Source: mod_por_rst_n
7	MAIN_CLKGATE_CTRL0_MAIN_A53_0_NOGATE_PROXY	R/W	X	MAIN A53SS0 clock gate deactivate. Reset Source: mod_por_rst_n
6	MAIN_CLKGATE_CTRL0_MAIN_CBA_ECC_AGG_NOGATE_PROXY	R/W	X	MAIN domain data bus ECC aggragator (main_cba_ecc_aggr_main_0) clock gate deactivate. Reset Source: mod_por_rst_n
5	MAIN_CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE_PROXY	R/W	X	MAIN domain datal bus (main_fw_cbass) clock gate deactivate. Reset Source: mod_por_rst_n
4	MAIN_CLKGATE_CTRL0_MAIN_CBA_NOGATE_PROXY	R/W	X	MAIN domain data bus (main_cbass) clock gate deactivate. Reset Source: mod_por_rst_n
3	RESERVED	NONE	0h	Reserved

Table 14-6570. MCU_CTRL_MMR_CFG0_MAIN_CLKGATE_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MAIN_CLKGATE_CTRL0_MAIN_INFRA_ECC_AGG_NOGATE_PROXY	R/W	X	MAIN domain Infrastructure ECC aggragator (main_infra_ecc_aggr) clock gate deactivate. Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	MAIN_CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE_PROXY	R/W	X	MAIN domain Infrastructure bus (main_infra_cbass) clock gate deactivate. Reset Source: mod_por_rst_n

14.2.1.1.2.2.253 MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register (Offset = 1B008h) [reset = 0h]

- KICK0 component

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Table 14-6571. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B008h**

Figure 14-2185. MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0_PROXY							
R/W							
0h							

Table 14-6573. MCU_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.254 MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register

1 MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register (Offset = 1B00Ch) [reset = 0h]

- KICK1 component

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Table 14-6574. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B00Ch**

Figure 14-2186. MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1_PROXY							
R/W							
0h							

Table 14-6576. MCU_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.255 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register (Offset = 1B100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6577. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B100h**

Figure 14-2187. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0							
R/W							
0h							

Table 14-6579. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.256 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register (Offset = 1B104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6580. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B104h**

Figure 14-2188. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1							
R/W							
0h							

Table 14-6582. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.257 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register (Offset = 1B108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6583. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B108h**

Figure 14-2189. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2							
R/W							
0h							

Table 14-6585. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.258 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register (Offset = 1B10Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-6586. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B10Ch**

Figure 14-2190. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3							
R/W							
0h							

Table 14-6588. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.259 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register (Offset = 1B110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6589. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B110h**

Figure 14-2191. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4							
R/W							
0h							

Table 14-6591. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.260 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register

1 MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register (Offset = 1B114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6592. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	**0451 B114h**

Figure 14-2192. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6594. MCU_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.2 Pad Configuration Registers

14.2.1.2.1 Pad Configuration Register Functional Description

The pad configuration registers are used to configure most of the device pads. Each pad configuration register is associated only with one pad and has bits as described in Table 14-4403.

Table 14-6595. Description Of The Pad Configuration Register Bits

Bit	Field	Type	Reset	Description

31	LOCK	R/W	(1)	Pad configuration register lock bit.
				`0h - The corresponding pad configuration register is unlocked. Its value can be modified. Further writes are allowed.`
				`1h - The corresponding pad configuration register is locked. Its value can not be modified. Further writes are not allowed.`
				Once the padconfig is locked a reset is the only allowed option to modify the padconfig.
				The lock bit can be reset only by PORz (MCU and Main Domain cold reset) event.

30-22	RESERVED	None	(1)	Reserved

Table 14-6595. Description Of The Pad Configuration Register Bits (continued)

Bit	Field	Type	Reset	Description

21	TX_DIS(3)	R/W	(1)	Driver Disable
				In normal operation, TX_DIS = 0, the buffer output enable is controlled by the peripheral selected via the MUXMODE bit field. TX_DIS can be used to override the peripheral control by forcing the output off. This can be used to prevent glitches when changing the MUXMODE value.
				`0h - Driver activation is under the control of the peripheral selected via the MUXMODE bit field.`
				`1h - Driver is disabled`

20 - 19	DRV_STR(4)	R/W	(1)	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
				`0h - Nominal`
				`1h - Reserved`
				`2h - Fast`
				`3h - Reserved`
				Note
				The nominal (default) DRV_STR settings should be used to ensure timings, unless specific instructions are given otherwise.

18	RXACTIVE(5)	R/W	(1)	Input enable for the Pad
				`0h - Receiver disabled`
				`1h - Receiver enabled`

17	PULLTYPESEL(2)	R/W	(1)	Pad Pullup / Pulldown type selection
				`0h - Pulldown selected`
				`1h - Pullup selected`

16	PULLUDEN(2)	R/W	(1)	Pad Pullup / Pulldown enable. This is an active low signal.
				`0h - Pullup / Pulldown enabled`
				`1h - Pullup / Pulldown disabled`

15	RESERVED	R/W	(1)	Reserved

14	ST_EN	R/W	(1)	Receiver Schmitt Trigger enable
				`0h - Schmitt trigger input disabled`
				`1h - Schmitt trigger input enabled`

13 - 11	DEBOUNCE_SEL	R/W	(1)	Selects the debounce period for select input signals. See I/O Debounce Control Registers for more information.
				`0h - Deactivated`
				`1h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1`
				`2h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2`
				`3h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3`
				`4h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4`
				`5h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5`
				`6h - Selects debounce value defined by MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6`
				`7h - Reserved`

10 - 4	RESERVED	R/W	(1)	Reserved

Table 14-6595. Description Of The Pad Configuration Register Bits (continued)

Bit	Field	Type	Reset	Description

3 - 0	MUXMODE	R/W	(1)	Pad functional signal mux selection Field values (others are reserved):
				`0h - Mux Mode 0`
				`1h - Mux Mode 1`
				`2h - Mux Mode 2`
				`3h - Mux Mode 3`
				`4h - Mux Mode 4`
				`5h - Mux Mode 5`
				`6h - Mux Mode 6`
				`7h - Mux Mode 7`
				`8h - Mux Mode 8`
				`9h - Mux Mode 9`
				`Ah - Mux Mode 10`
				`Bh - Mux Mode 11`
				`Ch - Mux Mode 12`
				`Dh - Mux Mode 13`
				`Eh - Mux Mode 14`
				`Fh - Mux Mode 15`

(1) See *Pad Configuration Registers* for reset values for Pad Configuration registers.

(2) These bits do not apply to "I2C OD FS" buffer types as these IOs do not have internal pull registers.

(3) To prevent unwanted glitches, software should disable the output driver by setting the TX_DIS bit before writing a new MUXMODE value. Once the new MUXMODE value is written, the TX_DIS bit can be reset in order to re-enable the pin driver.

(4) Use of settings other than the reset value could invalidate datasheet timings.

(5) The RXACTIVE bit must never be set without a valid logic state being sourced to the pin associated with the respective PADCONFIG register. This is very important since a floating input may damage the device.

Many of the device pads support pad multiplexing. This means that their function can be independently chosen from two or more options. The selection of functions available on each pad is enumerated in table “*Pin Multiplexing*” of the device-specific Datasheet. The desired function is selected via the MUXMODE field of the associated pad configuration register.

14.2.1.2.2 Pad Configuration PADCONFIG Registers

Table 14-6596. AM64X_PG2 PADCONFIG Registers

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values											
							LOCK[31]	RSVD[30:22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	RSVD[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG0	OSPI0_CLK		F4000h	F6000h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG1	OSPI0_LBCLKO		F4004h	F6004h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG2	OSPI0_DQS		F4008h	F6008h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG3	OSPI0_D0		F400Ch	F600Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG4	OSPI0_D1		F4010h	F6010h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG5	OSPI0_D2		F4014h	F6014h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG6	OSPI0_D3		F4018h	F6018h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG7	OSPI0_D4		F401Ch	F601Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG8	OSPI0_D5		F4020h	F6020h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG9	OSPI0_D6		F4024h	F6024h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG10	OSPI0_D7		F4028h	F6028h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG11	OSPI0_CSn0		F402Ch	F602Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG12	OSPI0_CSn1		F4030h	F6030h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG13	OSPI0_CSn2		F4034h	F6034h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG14	OSPI0_CSn3		F4038h	F6038h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG15	GPMC0_AD0		F403Ch	F603Ch	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG16	GPMC0_AD1		F4040h	F6040h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG17	GPMC0_AD2		F4044h	F6044h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG18	GPMC0_AD3		F4048h	F6048h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG19	GPMC0_AD4		F404Ch	F604Ch	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG20	GPMC0_AD5		F4050h	F6050h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG21	GPMC0_AD6		F4054h	F6054h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG22	GPMC0_AD7		F4058h	F6058h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG23	GPMC0_AD8		F405Ch	F605Ch	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG24	GPMC0_AD9		F4060h	F6060h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG25	GPMC0_AD10		F4064h	F6064h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG26	GPMC0_AD11	EQEP1_A	F4068h	F6068h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG27	GPMC0_AD12	EQEP1_B	F406Ch	F606Ch	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG28	GPMC0_AD13		F4070h	F6070h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG29	GPMC0_AD14		F4074h	F6074h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG30	GPMC0_AD15		F4078h	F6078h	LVCMOS	254007h	0	0	1	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG31	GPMC0_CLK		F407Ch	F607Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7

Table 14-6596. AM64X_PG2 PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values											
							LOCK[31]	RSVD[30:22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	RSVD[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG33	GPMC0_ADVn_ALE		F4084h	F6084h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG34	GPMC0_OEn_REn		F4088h	F6088h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG35	GPMC0_WEn		F408Ch	F608Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG36	GPMC0_BE0n_CLE		F4090h	F6090h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG37	GPMC0_BE1n		F4094h	F6094h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG38	GPMC0_WAIT0		F4098h	F6098h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG39	GPMC0_WAIT1		F409Ch	F609Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG40	GPMC0_WPn	EQEP0_A	F40A0h	F60A0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG41	GPMC0_DIR	EQEP0_B	F40A4h	F60A4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG42	GPMC0_CSn0	EQEP0_S	F40A8h	F60A8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG43	GPMC0_CSn1	EQEP0_I	F40ACh	F60ACh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG44	GPMC0_CSn2	EQEP1_S GPIO0_43	F40B0h	F60B0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG45	GPMC0_CSn3	EQEP1_I GPIO0_44	F40B4h	F60B4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG46	PRG1_PRU0_GPO0		F40B8h	F60B8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG47	PRG1_PRU0_GPO1		F40BCh	F60BCh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG48	PRG1_PRU0_GPO2		F40C0h	F60C0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG49	PRG1_PRU0_GPO3		F40C4h	F60C4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG50	PRG1_PRU0_GPO4		F40C8h	F60C8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG51	PRG1_PRU0_GPO5		F40CCh	F60CCh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG52	PRG1_PRU0_GPO6		F40D0h	F60D0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG53	PRG1_PRU0_GPO7		F40D4h	F60D4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG54	PRG1_PRU0_GPO8		F40D8h	F60D8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG55	PRG1_PRU0_GPO9		F40DCh	F60DCh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG56	PRG1_PRU0_GPO10		F40E0h	F60E0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG57	PRG1_PRU0_GPO11		F40E4h	F60E4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG58	PRG1_PRU0_GPO12		F40E8h	F60E8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG59	PRG1_PRU0_GPO13		F40ECh	F60ECh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG60	PRG1_PRU0_GPO14		F40F0h	F60F0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG61	PRG1_PRU0_GPO15		F40F4h	F60F4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG62	PRG1_PRU0_GPO16		F40F8h	F60F8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG63	PRG1_PRU0_GPO17		F40FCh	F60FCh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG64	PRG1_PRU0_GPO18		F4100h	F6100h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG65	PRG1_PRU0_GPO19		F4104h	F6104h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7

Table 14-6596. AM64X_PG2 PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values											
							LOCK[31]	RSVD[30:22]	TX_DIS[21](1)	DRV_STR[20:19](2)	RXACTIVE[18](3)	PULLTYPESEL[17](4)	PULLUDEN[16](4)	RSVD[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG66	PRG1_PRU1_GPO0		F4108h	F6108h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG67	PRG1_PRU1_GPO1		F410Ch	F610Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG68	PRG1_PRU1_GPO2		F4110h	F6110h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG69	PRG1_PRU1_GPO3		F4114h	F6114h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG70	PRG1_PRU1_GPO4		F4118h	F6118h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG71	PRG1_PRU1_GPO5		F411Ch	F611Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG72	PRG1_PRU1_GPO6		F4120h	F6120h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG73	PRG1_PRU1_GPO7		F4124h	F6124h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG74	PRG1_PRU1_GPO8		F4128h	F6128h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG75	PRG1_PRU1_GPO9		F412Ch	F612Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG76	PRG1_PRU1_GPO10		F4130h	F6130h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG77	PRG1_PRU1_GPO11		F4134h	F6134h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG78	PRG1_PRU1_GPO12		F4138h	F6138h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG79	PRG1_PRU1_GPO13		F413Ch	F613Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG80	PRG1_PRU1_GPO14		F4140h	F6140h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG81	PRG1_PRU1_GPO15		F4144h	F6144h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG82	PRG1_PRU1_GPO16		F4148h	F6148h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG83	PRG1_PRU1_GPO17		F414Ch	F614Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG84	PRG1_PRU1_GPO18		F4150h	F6150h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG85	PRG1_PRU1_GPO19		F4154h	F6154h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG86	PRG1_MDIO0_MDIO		F4158h	F6158h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG87	PRG1_MDIO0_MDC		F415Ch	F615Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG88	PRG0_PRU0_GPO0		F4160h	F6160h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG89	PRG0_PRU0_GPO1		F4164h	F6164h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG90	PRG0_PRU0_GPO2		F4168h	F6168h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG91	PRG0_PRU0_GPO3		F416Ch	F616Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG92	PRG0_PRU0_GPO4		F4170h	F6170h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG93	PRG0_PRU0_GPO5		F4174h	F6174h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG94	PRG0_PRU0_GPO6		F4178h	F6178h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG95	PRG0_PRU0_GPO7		F417Ch	F617Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG96	PRG0_PRU0_GPO8		F4180h	F6180h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG97	PRG0_PRU0_GPO9		F4184h	F6184h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG98	PRG0_PRU0_GPO10		F4188h	F6188h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG99	PRG0_PRU0_GPO11		F418Ch	F618Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7

Table 14-6596. AM64X_PG2 PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values											
							LOCK[31]	RSVD[30:22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	RSVD[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG100	PRG0_PRU0_GPO12		F4190h	F6190h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG101	PRG0_PRU0_GPO13		F4194h	F6194h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG102	PRG0_PRU0_GPO14		F4198h	F6198h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG103	PRG0_PRU0_GPO15		F419Ch	F619Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG104	PRG0_PRU0_GPO16		F41A0h	F61A0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG105	PRG0_PRU0_GPO17		F41A4h	F61A4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG106	PRG0_PRU0_GPO18		F41A8h	F61A8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG107	PRG0_PRU0_GPO19		F41ACh	F61ACh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG108	PRG0_PRU1_GPO0	EQEP0_A	F41B0h	F61B0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG109	PRG0_PRU1_GPO1	EQEP0_B	F41B4h	F61B4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG110	PRG0_PRU1_GPO2	EQEP0_S	F41B8h	F61B8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG111	PRG0_PRU1_GPO3	EQEP1_A	F41BCh	F61BCh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG112	PRG0_PRU1_GPO4	EQEP1_B	F41C0h	F61C0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG113	PRG0_PRU1_GPO5	EQEP1_S	F41C4h	F61C4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG114	PRG0_PRU1_GPO6	EQEP2_A	F41C8h	F61C8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG115	PRG0_PRU1_GPO7	EQEP2_B	F41CCh	F61CCh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG116	PRG0_PRU1_GPO8	EQEP2_S	F41D0h	F61D0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG117	PRG0_PRU1_GPO9	EQEP0_I	F41D4h	F61D4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG118	PRG0_PRU1_GPO10	EQEP1_I	F41D8h	F61D8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG119	PRG0_PRU1_GPO11	EQEP2_I	F41DCh	F61DCh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG120	PRG0_PRU1_GPO12	EQEP2_B	F41E0h	F61E0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG121	PRG0_PRU1_GPO13	EQEP0_I	F41E4h	F61E4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG122	PRG0_PRU1_GPO14	EQEP1_I	F41E8h	F61E8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG123	PRG0_PRU1_GPO15		F41ECh	F61ECh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG124	PRG0_PRU1_GPO16		F41F0h	F61F0h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG125	PRG0_PRU1_GPO17		F41F4h	F61F4h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG126	PRG0_PRU1_GPO18		F41F8h	F61F8h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG127	PRG0_PRU1_GPO19		F41FCh	F61FCh	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG128	PRG0_MDIO0_MDIO		F4200h	F6200h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG129	PRG0_MDIO0_MDC		F4204h	F6204h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG130	SPI0_CS0		F4208h	F6208h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG131	SPI0_CS1	ADC_EXT_TRIGGER0	F420Ch	F620Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG132	SPI0_CLK		F4210h	F6210h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG133	SPI0_D0		F4214h	F6214h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7

Table 14-6596. AM64X_PG2 PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values											
							LOCK[31]	RSVD[30:22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	RSVD[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG134	SPI0_D1		F4218h	F6218h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG135	SPI1_CS0		F421Ch	F621Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG136	SPI1_CS1	ADC_EXT_TRIGGER1	F4220h	F6220h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG137	SPI1_CLK		F4224h	F6224h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG138	SPI1_D0		F4228h	F6228h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG139	SPI1_D1		F422Ch	F622Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG140	UART0_RXD	EQEP0_A	F4230h	F6230h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG141	UART0_TXD	EQEP0_B	F4234h	F6234h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG142	UART0_CTSn	ADC_EXT_TRIGGER0 EQEP0_S	F4238h	F6238h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG143	UART0_RTSn	EQEP0_I	F423Ch	F623Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG144	UART1_RXD	EQEP1_A	F4240h	F6240h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG145	UART1_TXD	EQEP1_B	F4244h	F6244h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG146	UART1_CTSn	ADC_EXT_TRIGGER1 EQEP1_S	F4248h	F6248h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG147	UART1_RTSn	EQEP1_I	F424Ch	F624Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG148	MCAN0_TX	EQEP2_I	F4250h	F6250h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG149	MCAN0_RX	EQEP2_S	F4254h	F6254h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG150	MCAN1_TX	EQEP2_A	F4258h	F6258h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG151	MCAN1_RX	EQEP2_B	F425Ch	F625Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG152	I2C0_SCL		F4260h	F6260h	I2C OPEN DRAIN	54007h	0	0	0	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG153	I2C0_SDA		F4264h	F6264h	I2C OPEN DRAIN	54007h	0	0	0	0	1	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG154	I2C1_SCL		F4268h	F6268h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG155	I2C1_SDA		F426Ch	F626Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG156	ECAP0_IN_APWM_OUT	GPIO1_68	F4270h	F6270h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG157	EXT_REFCLK1		F4274h	F6274h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG158	EXTINTn	GPIO1_70	F4278h	F6278h	I2C OPEN DRAIN	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG159	MMC1_DAT3	GPIO1_71	F427Ch	F627Ch	SDIO	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG160	MMC1_DAT2	GPIO1_72	F4280h	F6280h	SDIO	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG161	MMC1_DAT1	GPIO1_73	F4284h	F6284h	SDIO	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG162	MMC1_DAT0	GPIO1_74	F4288h	F6288h	SDIO	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG163	MMC1_CLK[5]	GPIO1_75	F428Ch	F628Ch	SDIO	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG165	MMC1_CMD	GPIO1_76	F4294h	F6294h	SDIO	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG166	MMC1_SDCD	GPIO1_77	F4298h	F6298h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG167	MMC1_SDWP	GPIO1_78	F429Ch	F629Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7

Table 14-6596. AM64X_PG2 PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values											
							LOCK[31]	RSVD[30:22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	RSVD[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:4]	MUXMODE[3:0]
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG168	RESET_REQz		F42A0h	F62A0h	LVCMOS	264000h	0	0	1	0	1	1	0	1	1	0	0	0
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG169	RESETSTATz		F42A4h	F62A4h	LVCMOS	14000h	0	0	0	0	0	0	1	1	1	0	0	0
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG170	USB0_DRVVBUS		F42A8h	F62A8h	LVCMOS	204007h	0	0	1	0	0	0	0	1	1	0	0	7
MAIN_PADCFG_CTRL_MMR_CFG0_PADCONFIG171	PORz_OUT		F42ACh	F62ACh	LVCMOS	14000h	0	0	0	0	0	0	1	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG0	MCU_SPI0_CS0	MCU_GPIO0_13	4084000h	4086000h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG1	MCU_SPI0_CS1	MCU_GPIO0_12	4084004h	4086004h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG2	MCU_SPI0_CLK		4084008h	4086008h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG3	MCU_SPI0_D0		408400Ch	408600Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG4	MCU_SPI0_D1		4084010h	4086010h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG5	MCU_SPI1_CS0	MCU_GPIO0_5	4084014h	4086014h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG6	MCU_SPI1_CS1	MCU_GPIO0_6	4084018h	4086018h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG7	MCU_SPI1_CLK		408401Ch	408601Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG8	MCU_SPI1_D0		4084020h	4086020h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG9	MCU_SPI1_D1		4084024h	4086024h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG10	MCU_UART0_RXD		4084028h	4086028h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG11	MCU_UART0_TXD		408402Ch	408602Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG12	MCU_UART0_CTSn	MCU_GPIO0_1	4084030h	4086030h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG13	MCU_UART0_RTSn	MCU_GPIO0_0	4084034h	4086034h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG14	MCU_UART1_RXD		4084038h	4086038h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG15	MCU_UART1_TXD		408403Ch	408603Ch	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG16	MCU_UART1_CTSn	MCU_GPIO0_16	4084040h	4086040h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG17	MCU_UART1_RTSn	MCU_GPIO0_17	4084044h	4086044h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG18	MCU_I2C0_SCL		4084048h	4086048h	I2C OPEN DRAIN	54007h	0	0	0	0	1	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG19	MCU_I2C0_SDA		408404Ch	408604Ch	I2C OPEN DRAIN	54007h	0	0	0	0	1	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG20	MCU_I2C1_SCL	MCU_GPIO0_20	4084050h	4086050h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG21	MCU_I2C1_SDA	MCU_GPIO0_21	4084054h	4086054h	LVCMOS	214007h	0	0	1	0	0	0	1	1	1	0	0	7
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG22	MCU_RESETz		4084058h	4086058h	LVCMOS	264000h	0	0	1	0	1	1	0	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG23	MCU_PORz		408405Ch	408605Ch	LVCMOS	14000h	0	0	0	0	0	0	1	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG24	MCU_RESETSTATz		4084060h	4086060h	LVCMOS	14000h	0	0	0	0	0	0	1	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG25	MCU_SAFETY_ERRORn		4084064h	4086064h	LVCMOS	44000h	0	0	0	0	1	0	0	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG26	TCK		4084068h	4086068h	LVCMOS	264000h	0	0	1	0	1	1	0	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG27	TRSTn		408406Ch	408606Ch	LVCMOS	244000h	0	0	1	0	1	0	0	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG28	TDI		4084070h	4086070h	LVCMOS	264000h	0	0	1	0	1	1	0	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG29	TDO		4084074h	4086074h	LVCMOS	24000h	0	0	0	0	0	1	0	1	1	0	0	0

Table 14-6596. AM64X_PG2 PADCONFIG Registers (continued)

Register Name	Ball Name	Debounce Signal	Physical Address	Proxy Address	Buffer Type	Register Reset	Bit Field Reset Values											
							LOCK[31]	RSVD[30:22]	TX_DIS[21][1]	DRV_STR[20:19][2]	RXACTIVE[18][3]	PULLTYPESEL[17][4]	PULLUDEN[16][4]	RSVD[15]	ST_EN[14]	DEBOUNCE_SEL[13:11]	RSVD[10:4]	MUXMODE[3:0]
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG30	TMS		4084078h	4086078h	LVCMOS	264000h	0	0	1	0	1	1	0	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG31	EMU0		408407Ch	408607Ch	LVCMOS	264000h	0	0	1	0	1	1	0	1	1	0	0	0
MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIG32	EMU1		4084080h	4086080h	LVCMOS	264000h	0	0	1	0	1	1	0	1	1	0	0	0

(1) TX_DIS bit must be set before changing the MUXMODE value when the IO associated with a PADCONFIG register was previously configured to operate as an output. This is required to prevent a potential glitch propagating through the output buffer when the MUXMODE values is changed. A MUXMODE value change should be implemented with three PADCONFIG write operations, where the TX_DIS bit is set in the first write operation, the MUXMODE values is changed in the second write operation, and the TX_DIS bit is reset in the third write operation. This will disable the output buffer while the pin mux logic changes signal functions.

(2) Use of settings other than the reset value could invalidate datasheet timings.

(3) The RXACTIVE bit must never be set without a valid logic state being sourced to the pin associated with the respective PADCONFIG register. This is very important since a floating input may damage the device.

(4) These bits do not apply to "I2C OD FS" buffer types as these IOs do not have internal pull registers.

(5) For MMC1_CLK signal to work properly, the RXACTIVE bit should be set to 0x1 because of retiming purposes.

14.2.1.2.3 main_padcfg_ctrl_mmr

main_padcfg_ctrl_mmr

14.2.1.2.3.1 main_padcfg_ctrl_mmr Summaries

main_padcfg_ctrl_mmr Summaries

Table 14-6597. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
0h	32	MAIN_PADCFG_CTRL_MMR_CFG0_PID	000F 0000h
4h	32	MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0	000F 0004h
8h	32	MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1	000F 0008h
1008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	000F 1008h
100Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	000F 100Ch
1010h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS	000F 1010h
1014h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	000F 1014h
1018h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE	000F 1018h
101Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	000F 101Ch
1020h	32	MAIN_PADCFG_CTRL_MMR_CFG0_EOI	000F 1020h
1024h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS	000F 1024h
1028h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	000F 1028h
102Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	000F 102Ch
1030h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR	000F 1030h
1100h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	000F 1100h
2000h	32	MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY	000F 2000h
2004h	32	MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY	000F 2004h
2008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY	000F 2008h
3008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	000F 3008h
300Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	000F 300Ch
3010h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	000F 3010h
3014h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	000F 3014h
3018h	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	000F 3018h
301Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	000F 301Ch
3020h	32	MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY	000F 3020h
3024h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	000F 3024h
3028h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	000F 3028h

Table 14-6597. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
302Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	000F 302Ch
3030h	32	MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	000F 3030h
3100h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0	000F 3100h
5008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	000F 5008h
500Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	000F 500Ch
5100h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	000F 5100h
5104h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	000F 5104h
5108h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY	000F 5108h
510Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	000F 510Ch
5110h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	000F 5110h
5114h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY	000F 5114h
7008h	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	000F 7008h
700Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	000F 700Ch
7100h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0	000F 7100h
7104h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1	000F 7104h
7108h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2	000F 7108h
710Ch	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3	000F 710Ch
7110h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4	000F 7110h
7114h	32	MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5	000F 7114h

14.2.1.2.3.2 main_padcfg_ctrl_mmr Registers

main_padcfg_ctrl_mmr Registers

14.2.1.2.3.2.1 MAIN_PADCFG_CTRL_MMR_CFG0_PID Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800213h]

PID register

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Table 14-6598. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 0000h**

Figure 14-2193. MAIN_PADCFG_CTRL_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM		PID_MINOR					
R		R					
0h		13h					

Table 14-6600. MAIN_PADCFG_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	13h	Reset Source: mod_g_rst_n

14.2.1.2.3.2.2 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register (Offset = 4h) [reset = 10000001h]

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Table 14-6601. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 0004h**

Figure 14-2194. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV							
R							
1000h							
23	22	21	20	19	18	17	16
MMR_CFG0_CFG_REV							
R							
1000h							
15	14	13	12	11	10	9	8
MMR_CFG0_SPEC_REV							
R							
1h							
7	6	5	4	3	2	1	0
MMR_CFG0_SPEC_REV							
R							
1h							

Table 14-6603. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV	R	1h	Minor spec-only revision. Doesn't change RTL release Reset Source: mod_por_rst_n

14.2.1.2.3.2.3 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000BFh]

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Table 14-6604. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 0008h**

Figure 14-2195. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
BFh							

Table 14-6606. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.3.2.4 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-6607. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1008h**

Figure 14-2196. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-6609. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.5 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-6610. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 100Ch**

Figure 14-2197. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-6612. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.6 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-6613. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1010h**

Figure 14-2198. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6615. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.7 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-6616. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1014h**

Figure 14-2199. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6618. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.8 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-6619. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1018h**

Figure 14-2200. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6621. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.9 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-6622. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 101Ch**

Figure 14-2201. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6624. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.10 MAIN_PADCFG_CTRL_MMR_CFG0_EOI Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-6625. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1020h**

Figure 14-2202. MAIN_PADCFG_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-6627. MAIN_PADCFG_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.3.2.11 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-6628. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1024h**

Figure 14-2203. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-6630. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.3.2.12 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-6631. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1028h**

Figure 14-2204. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-6633. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.3.2.13 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-6634. Instance Table

Instance Name	**Physical Address**
PADCFG_CTRL0	**000F 102Ch**

Figure 14-2205. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							

23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			

15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							

7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 14-6636. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.3.2.14 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-6637. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1030h**

Figure 14-2206. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-6639. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.15 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-6640. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 1100h**

Figure 14-2207. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-6642. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.3.2.16 MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800213h]

PID register

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Table 14-6643. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 2000h**

Figure 14-2208. MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MSB16_PROXY							
R							
6180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		13h					

Table 14-6645. MAIN_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	13h	Reset Source: mod_g_rst_n

14.2.1.2.3.2.17 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register (Offset = 2004h) [reset = 10000001h]

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Table 14-6646. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 2004h**

Figure 14-2209. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MMR_CFG0_CFG_REV_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MMR_CFG0_CFG_REV_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MMR_CFG0_SPEC_REV_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MMR_CFG0_SPEC_REV_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-6648. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV_PROXY	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV_PROXY	R	1h	Minor spec-only revision. Doesn't change RTL release Reset Source: mod_por_rst_n

14.2.1.2.3.2.18 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000BFh]

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Table 14-6649. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 2008h**

Figure 14-2210. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS_PROXY							
R							
BFh							

Table 14-6651. MAIN_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.3.2.19 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-6652. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3008h**

Figure 14-2211. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-6654. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.20 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-6655. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 300Ch**

Figure 14-2212. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-6657. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.21 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-6658. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3010h**

Figure 14-2213. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6660. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.22 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-6661. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3014h**

Figure 14-2214. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6663. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.23 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-6664. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3018h**

Figure 14-2215. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6666. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.24 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-6667. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 301Ch**

Figure 14-2216. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6669. MAIN_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.25 MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-6670. Instance Table

Instance Name	**Physical Address**
PADCFG_CTRL0	**000F 3020h**

Figure 14-2217. MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_VECTOR_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6672. MAIN_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.3.2.26 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-6673. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3024h**

Figure 14-2218. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-6675. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.3.2.27 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-6676. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3028h**

Figure 14-2219. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-6678. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.3.2.28 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-6679. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 302Ch**

Figure 14-2220. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-6681. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.3.2.29 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-6682. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3030h**

Figure 14-2221. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-6684. MAIN_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.3.2.30 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-6685. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 3100h**

Figure 14-2222. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-6687. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.3.2.31 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-6688. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5008h**

Figure 14-2223. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-6690. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.32 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-6691. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 500Ch**

Figure 14-2224. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-6693. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.33 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6694. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5100h**

Figure 14-2225. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-6696. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.34 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6697. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5104h**

Figure 14-2226. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-6699. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.35 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6700. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5108h**

Figure 14-2227. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-6702. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.36 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-6703. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 510Ch**

Figure 14-2228. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-6705. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.37 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6706. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5110h**

Figure 14-2229. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-6708. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.38 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register (Offset = 5114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6709. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 5114h**

Figure 14-2230. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5_READONLY							
R							
0h							

Table 14-6711. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.39 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-6712. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7008h**

Figure 14-2231. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-6714. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.40 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-6715. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 700Ch**

Figure 14-2232. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCK1_KICK1_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK1_KICK1_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-6717. MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.3.2.41 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6718. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 7100h

Figure 14-2233. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-6720. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.42 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6721. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7104h**

Figure 14-2234. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-6723. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.43 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6724. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7108h**

Figure 14-2235. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-6726. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.44 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-6727. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 710Ch**

Figure 14-2236. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-6729. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.45 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6730. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7110h**

Figure 14-2237. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6732. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.3.2.46 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register

1 MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6733. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	**000F 7114h**

Figure 14-2238. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-6735. MAIN_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.4 mcu_padcfg_ctrl_mmr

mcu_padcfg_ctrl_mmr

14.2.1.2.4.1 mcu_padcfg_ctrl_mmr Summaries

mcu_padcfg_ctrl_mmr Summaries

Table 14-6736. MCU_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=0408 0000h, Length=32768

Offset	Length	Register Name	MCU_PADCFG_CTRL0 Physical Address
0h	32	MCU_PADCFG_CTRL_MMR_CFG0_PID	0408 0000h
4h	32	MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0	0408 0004h
8h	32	MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1	0408 0008h
1008h	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	0408 1008h
100Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	0408 100Ch
1010h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS	0408 1010h
1014h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	0408 1014h
1018h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE	0408 1018h
101Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	0408 101Ch
1020h	32	MCU_PADCFG_CTRL_MMR_CFG0_EOI	0408 1020h
1024h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS	0408 1024h
1028h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	0408 1028h
102Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	0408 102Ch
1030h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR	0408 1030h
1100h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	0408 1100h
2000h	32	MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY	0408 2000h
2004h	32	MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY	0408 2004h
2008h	32	MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY	0408 2008h
3008h	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	0408 3008h
300Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	0408 300Ch
3010h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	0408 3010h
3014h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	0408 3014h
3018h	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	0408 3018h
301Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	0408 301Ch
3020h	32	MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY	0408 3020h
3024h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	0408 3024h
3028h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	0408 3028h
302Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	0408 302Ch

Table 14-6736. MCU_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=0408 0000h, Length=32768 (continued)

Offset	Length	Register Name	MCU_PADCFG_CTRL0 Physical Address
3030h	32	MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	0408 3030h
3100h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0	0408 3100h
5008h	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	0408 5008h
500Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	0408 500Ch
5100h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	0408 5100h
5104h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY	0408 5104h
7008h	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	0408 7008h
700Ch	32	MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	0408 700Ch
7100h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0	0408 7100h
7104h	32	MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1	0408 7104h

14.2.1.2.4.2 mcu_padcfg_ctrl_mmr Registers

mcu_padcfg_ctrl_mmr Registers

14.2.1.2.4.2.1 MCU_PADCFG_CTRL_MMR_CFG0_PID Register

1 MCU_PADCFG_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800213h]

PID register

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Table 14-6737. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 0000h**

Figure 14-2239. MCU_PADCFG_CTRL_MMR_CFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">13h</td></tr>
</table>

Table 14-6739. MCU_PADCFG_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	13h	Reset Source: mod_g_rst_n

14.2.1.2.4.2.2 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register (Offset = 4h) [reset = 10000001h]

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Table 14-6740. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 0004h**

Figure 14-2240. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV							
R							
1000h							
23	22	21	20	19	18	17	16
MMR_CFG0_CFG_REV							
R							
1000h							
15	14	13	12	11	10	9	8
MMR_CFG0_SPEC_REV							
R							
1h							
7	6	5	4	3	2	1	0
MMR_CFG0_SPEC_REV							
R							
1h							

Table 14-6742. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV	R	1h	Minor spec-only revision. Doesn't change RTL release Reset Source: mod_por_rst_n

14.2.1.2.4.2.3 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000BFh]

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Table 14-6743. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 0008h**

Figure 14-2241. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS							
R							
BFh							

Table 14-6745. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.4.2.4 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-6746. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1008h**

Figure 14-2242. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-6748. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.5 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-6749. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 100Ch**

Figure 14-2243. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-6751. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.6 MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-6752. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1010h**

Figure 14-2244. MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6754. MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.7 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-6755. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1014h**

Figure 14-2245. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6757. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.8 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-6758. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1018h**

Figure 14-2246. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6760. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.9 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-6761. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 101Ch**

Figure 14-2247. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6763. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.10 MCU_PADCFG_CTRL_MMR_CFG0_EOI Register

1 MCU_PADCFG_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-6764. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1020h**

Figure 14-2248. MCU_PADCFG_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-6766. MCU_PADCFG_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.4.2.11 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-6767. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1024h**

Figure 14-2249. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-6769. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.4.2.12 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-6770. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1028h**

Figure 14-2250. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-6772. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.4.2.13 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-6773. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 102Ch**

Figure 14-2251. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 14-6775. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.4.2.14 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-6776. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1030h**

Figure 14-2252. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-6778. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.15 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-6779. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 1100h**

Figure 14-2253. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-6781. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.4.2.16 MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800213h]

PID register

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Table 14-6782. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 2000h**

Figure 14-2254. MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16_PROXY							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		13h					

Table 14-6784. MCU_PADCFG_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	13h	Reset Source: mod_g_rst_n

14.2.1.2.4.2.17 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register (Offset = 2004h) [reset = 10000001h]

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Table 14-6785. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 2004h**

Figure 14-2255. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
23	22	21	20	19	18	17	16
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
15	14	13	12	11	10	9	8
MMR_CFG0_SPEC_REV_PROXY							
R							
1h							
7	6	5	4	3	2	1	0
MMR_CFG0_SPEC_REV_PROXY							
R							
1h							

Table 14-6787. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV_PROXY	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV_PROXY	R	1h	Minor spec-only revision. Doesn't change RTL release Reset Source: mod_por_rst_n

14.2.1.2.4.2.18 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000BFh]

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Table 14-6788. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 2008h**

Figure 14-2256. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS_PROXY							
R							
BFh							

Table 14-6790. MCU_PADCFG_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	BFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.4.2.19 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-6791. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3008h**

Figure 14-2257. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-6793. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.20 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-6794. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 300Ch**

Figure 14-2258. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-6796. MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.21 MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-6797. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3010h**

Figure 14-2259. MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6799. MCU_PADCFG_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.22 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-6800. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3014h**

Figure 14-2260. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6802. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.23 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-6803. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3018h

Figure 14-2261. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6805. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.24 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-6806. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 301Ch**

Figure 14-2262. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6808. MCU_PADCFG_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.25 MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-6809. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3020h**

Figure 14-2263. MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR_PROXY							
R/W							
0h							

Table 14-6811. MCU_PADCFG_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.4.2.26 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-6812. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3024h**

Figure 14-2264. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-6814. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.4.2.27 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-6815. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3028h**

Figure 14-2265. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-6817. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.4.2.28 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-6818. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 302Ch**

Figure 14-2266. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-6820. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.4.2.29 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-6821. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3030h**

Figure 14-2267. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-6823. MCU_PADCFG_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.4.2.30 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-6824. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 3100h**

Figure 14-2268. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6826. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.4.2.31 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-6827. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 5008h**

Figure 14-2269. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK1_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK1_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK1_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK1_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6829. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.32 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-6830. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 500Ch**

Figure 14-2270. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-6832. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.33 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6833. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 5100h**

Figure 14-2271. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-6835. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.4.2.34 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6836. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 5104h**

Figure 14-2272. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-6838. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.4.2.35 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-6839. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 7008h**

Figure 14-2273. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-6841. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.36 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

1 MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-6842. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 700Ch**

Figure 14-2274. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-6844. MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.4.2.37 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6845. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 7100h**

Figure 14-2275. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-6847. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.4.2.38 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

1 MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6848. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	**0408 7104h**

Figure 14-2276. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-6850. MCU_PADCFG_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.3 Kick Protection Registers

14.2.1.3.1 Kick Protection Registers

- CTRL_MMR0 Partition Unlock Values
- MCU_CTRL_MMR0 Partition Unlock Values
- PADCFG_CTRL0 Partition Unlock Values
- MCU_PADCFG_CTRL0 Partition Unlock Values

Table 14-6851. CTRL_MMR0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MAIN_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x043001008	0x043003008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
MAIN_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x04300100C	0x04300300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
MAIN_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x043005008	0x043007008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
MAIN_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x04300500C	0x04300700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
MAIN_CTRL_MMR_CFG0_LOCK2_KICK0	Partition 2	0x68EF3490	0x043009008	0x04300B008	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
MAIN_CTRL_MMR_CFG0_LOCK2_KICK1	Partition 2	0xD172BC5A	0x04300900C	0x04300B00C	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
MAIN_CTRL_MMR_CFG0_LOCK3_KICK0	Partition 3	0x68EF3490	0x04300D008	0x04300F008	0xC000 to 0xDFFF	0xE000 to 0xFFFF	BIST control/status regs
MAIN_CTRL_MMR_CFG0_LOCK3_KICK1	Partition 3	0xD172BC5A	0x04300D00C	0x04300F00C	0xC000 to 0xDFFF	0xE000 to 0xFFFF	BIST control/status regs
MAIN_CTRL_MMR_CFG0_LOCK4_KICK0	Partition 4	0x68EF3490	0x043011008	0x043013008	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
MAIN_CTRL_MMR_CFG0_LOCK4_KICK1	Partition 4	0xD172BC5A	0x04301100C	0x04301300C	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
MAIN_CTRL_MMR_CFG0_LOCK5_KICK0	Partition 5	0x68EF3490	0x043015008	0x043017008	0x14000 to 0x15FFF	0x16000 to 0x17FFF	DDR Frequency Control
MAIN_CTRL_MMR_CFG0_LOCK5_KICK1	Partition 5	0xD172BC5A	0x04301500C	0x04301700C	0x14000 to 0x15FFF	0x16000 to 0x17FFF	DDR Frequency Control
MAIN_CTRL_MMR_CFG0_LOCK6_KICK0	Partition 6	0x68EF3490	0x043019008	0x04301B008	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status
MAIN_CTRL_MMR_CFG0_LOCK6_KICK1	Partition 6	0xD172BC5A	0x04301900C	0x04301B00C	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status

Table 14-6852. MCU_CTRL_MMR0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MCU_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x004501008	0x004503008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
MCU_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x00450100C	0x00450300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	General configuration and IPC regs
MCU_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x004505008	0x004507008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs

Table 14-6852. MCU_CTRL_MMR0 Partition Unlock Values (continued)

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MCU_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x00450500C	0x00450700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IP control/Status regs
MCU_CTRL_MMR_CFG0_LOCK2_KICK0	Partition 2	0x68EF3490	0x004509008	0x00450B008	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
MCU_CTRL_MMR_CFG0_LOCK2_KICK1	Partition 2	0xD172BC5A	0x00450900C	0x00450B00C	0x8000 to 0x9FFF	0xA000 to 0xBFFF	Clock control/status regs
MCU_CTRL_MMR_CFG0_LOCK3_KICK0	Partition 3	0x68EF3490	0x00450D008	0x00450F008	0xC000 to 0xDFFF	0xE000 to 0xFFFF	BIST control/status regs
MCU_CTRL_MMR_CFG0_LOCK3_KICK1	Partition 3	0xD172BC5A	0x00450D00C	0x00450F00C	0xC000 to 0xDFFF	0xE000 to 0xFFFF	BIST control/status regs
MCU_CTRL_MMR_CFG0_LOCK4_KICK0	Partition 4	0x68EF3490	0x004511008	0x004513008	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
MCU_CTRL_MMR_CFG0_LOCK4_KICK1	Partition 4	0xD172BC5A	0x00451100C	0x00451300C	0x10000 to 0x11FFF	0x12000 to 0x13FFF	Verification and test control/ status regs
MCU_CTRL_MMR_CFG0_LOCK6_KICK0	Partition 6	0x68EF3490	0x004519008	0x00451B008	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status
MCU_CTRL_MMR_CFG0_LOCK6_KICK1	Partition 6	0xD172BC5A	0x00451900C	0x00451B00C	0x18000 to 0x19FFF	0x1A000 to 0x1BFFF	Power and reset control and status

Table 14-6853. PADCFG_CTRL0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x0000F1008	0x0000F3008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	PID
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x0000F100C	0x0000F300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	PID
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x0000F5008	0x0000F7008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IO PAD Configuration Registers
MAIN_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x0000F500C	0x0000F700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IO PAD Configuration Registers

Table 14-6854. MCU_PADCFG_CTRL0 Partition Unlock Values

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK0	Partition 0	0x68EF3490	0x004081008	0x004083008	0x0000 to 0x1FFF	0x2000 to 0x3FFF	PID
MCU_PADCFG_CTRL_MMR_CFG0_LOCK0_KICK1	Partition 0	0xD172BC5A	0x00408100C	0x00408300C	0x0000 to 0x1FFF	0x2000 to 0x3FFF	PID
MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK0	Partition 1	0x68EF3490	0x004085008	0x004087008	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IO PAD Configuration Registers

Table 14-6854. MCU_PADCFG_CTRL0 Partition Unlock Values (continued)

Register	Partition	Unlock Value	Proxy0 Address	Proxy0 Address	Proxy0 Offset Range	Proxy1 Offset Range	Usage
MCU_PADCFG_CTRL_MMR_CFG0_LOCK1_KICK1	Partition 1	0xD172BC5A	0x00408500C	0x00408700C	0x4000 to 0x5FFF	0x6000 to 0x7FFF	IO PAD Configuration Registers

14.2.1.4 Security Control Registers

14.2.1.4.1 main_sec_mmr

main_sec_mmr

14.2.1.4.1.1 main_sec_mmr Summaries

main_sec_mmr Summaries

Table 14-6855. MAIN_SEC_MMR_CFG2 Registers, Base Address=4590 0000h, Length=131072

Offset	Length	Register Name	MAIN_SEC_MMR0 Physical Address
0h	32	MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG	4590 0000h
40h	32	MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG	4590 0040h
1000h	32	MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG	4590 1000h
1040h	32	MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG	4590 1040h
9000h	32	MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG	4590 9000h
9040h	32	MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG	4590 9040h
10000h	32	MAIN_SEC_MMR_CFG2_CLSTR16_CORE0_DBG_CFG	4591 0000h

Table 14-6856. MAIN_SEC_MMR_CFG0 Registers, Base Address=45A0 0000h, Length=131072

Offset	Length	Register Name	MAIN_SEC_MMR0 Physical Address
0h	32	MAIN_SEC_MMR_CFG0_PID	45A0 0000h
20h	32	MAIN_SEC_MMR_CFG0_CLSTR0_DEF	45A0 0020h
40h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CFG	45A0 0040h
80h	32	MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL	45A0 0080h
90h	32	MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT	45A0 0090h
100h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG	45A0 0100h
110h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO	45A0 0110h
114h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI	45A0 0114h
120h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL	45A0 0120h
130h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT	45A0 0130h
180h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG	45A0 0180h
190h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO	45A0 0190h
194h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI	45A0 0194h
1A0h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL	45A0 01A0h
1B0h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT	45A0 01B0h
1020h	32	MAIN_SEC_MMR_CFG0_CLSTR1_DEF	45A0 1020h
1040h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CFG	45A0 1040h
1080h	32	MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL	45A0 1080h
1090h	32	MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT	45A0 1090h
1100h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG	45A0 1100h
1110h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO	45A0 1110h
1114h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI	45A0 1114h
1120h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL	45A0 1120h

Table 14-6856. MAIN_SEC_MMR_CFG0 Registers, Base Address=45A0 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_SEC_MMR0 Physical Address
1130h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT	45A0 1130h
1180h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG	45A0 1180h
1190h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO	45A0 1190h
1194h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI	45A0 1194h
11A0h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL	45A0 11A0h
11B0h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT	45A0 11B0h
9020h	32	MAIN_SEC_MMR_CFG0_CLSTR9_DEF	45A0 9020h
9040h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CFG	45A0 9040h
9080h	32	MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL	45A0 9080h
9090h	32	MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT	45A0 9090h
9110h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO	45A0 9110h
9114h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI	45A0 9114h
9190h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO	45A0 9190h
9194h	32	MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI	45A0 9194h
10020h	32	MAIN_SEC_MMR_CFG0_CLSTR16_DEF	45A1 0020h
10130h	32	MAIN_SEC_MMR_CFG0_CLSTR16_CORE0_PMSTAT	45A1 0130h
18008h	32	MAIN_SEC_MMR_CFG0_GIC_CONFIG	45A1 8008h

14.2.1.4.1.2 main_sec_mmr Registers

main_sec_mmr Registers

14.2.1.4.1.2.1 MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register (Offset = 0h) [reset = AA00h]

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Table 14-6857. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 0000h**

Figure 14-2277. MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_DBG_CFG_DBGEN				CLSTR0_CORE0_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6859. MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR0_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug activate. Reset Source: sys_por_rst_n
11:8	CLSTR0_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug activate. Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.2 MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Register (Offset = 40h) [reset = AA00h]

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Table 14-6860. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 0040h**

Figure 14-2278. MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE1_DBG_CFG_DBGEN				CLSTR0_CORE1_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6862. MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR0_CORE1_DBG_CFG_DBGEN	R/W	Ah	Core1 Invasive debug activate. Reset Source: sys_por_rst_n
11:8	CLSTR0_CORE1_DBG_CFG_NIDEN	R/W	Ah	Core1 Non-invasive debug activate. Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.3 MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG Register (Offset = 1000h) [reset = AA00h]

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Table 14-6863. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 1000h**

Figure 14-2279. MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE0_DBG_CFG_DBGEN				CLSTR1_CORE0_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6865. MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR1_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug activate. Reset Source: sys_por_rst_n
11:8	CLSTR1_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug activate. Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.4 MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG Register (Offset = 1040h) [reset = AA00h]

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Table 14-6866. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 1040h**

Figure 14-2280. MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">CLSTR1_CORE1_DBG_CFG_DBGEN</td><td colspan="4">CLSTR1_CORE1_DBG_CFG_NIDEN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Ah</td><td colspan="4">Ah</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6868. MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR1_CORE1_DBG_CFG_DBGEN	R/W	Ah	Core1 Invasive debug activate. Reset Source: sys_por_rst_n
11:8	CLSTR1_CORE1_DBG_CFG_NIDEN	R/W	Ah	Core1 Non-invasive debug activate. Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.5 MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG Register (Offset = 9000h) [reset = AAAAh]

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Table 14-6869. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 9000h**

Figure 14-2281. MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR9_CORE0_DBG_CFG_SPNIDEN				CLSTR9_CORE0_DBG_CFG_SPIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
CLSTR9_CORE0_DBG_CFG_NIDEN				CLSTR9_CORE0_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-6871. MAIN_SEC_MMR_CFG2_CLSTR9_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR9_CORE0_DBG_CFG_SPNIDEN	R/W	Ah	Core0 Secure Non-Invasive debug activate. Reset Source: sys_por_rst_n
11:8	CLSTR9_CORE0_DBG_CFG_SPIDEN	R/W	Ah	Core0 Secure Invasive debug activate. Reset Source: sys_por_rst_n
7:4	CLSTR9_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-Invasive debug activate. Reset Source: sys_por_rst_n
3:0	CLSTR9_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug activate. Reset Source: sys_por_rst_n

14.2.1.4.1.2.6 MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG Register (Offset = 9040h) [reset = AAAAh]

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Table 14-6872. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4590 9040h**

Figure 14-2282. MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR9_CORE1_DBG_CFG_SPNIDEN				CLSTR9_CORE1_DBG_CFG_SPIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
CLSTR9_CORE1_DBG_CFG_NIDEN				CLSTR9_CORE1_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-6874. MAIN_SEC_MMR_CFG2_CLSTR9_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR9_CORE1_DBG_CFG_SPNIDEN	R/W	Ah	Core1 Secure Non-Invasive debug activate. Reset Source: sys_por_rst_n
11:8	CLSTR9_CORE1_DBG_CFG_SPIDEN	R/W	Ah	Core1 Secure Invasive debug activate. Reset Source: sys_por_rst_n
7:4	CLSTR9_CORE1_DBG_CFG_NIDEN	R/W	Ah	Core1 Non-Invasive debug activate. Reset Source: sys_por_rst_n
3:0	CLSTR9_CORE1_DBG_CFG_DBGEN	R/W	Ah	Core1 Invasive debug activate. Reset Source: sys_por_rst_n

14.2.1.4.1.2.7 MAIN_SEC_MMR_CFG2_CLSTR16_CORE0_DBG_CFG Register

1 MAIN_SEC_MMR_CFG2_CLSTR16_CORE0_DBG_CFG Register (Offset = 10000h) [reset = AA00h]

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Table 14-6875. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**4591 0000h**

Figure 14-2283. MAIN_SEC_MMR_CFG2_CLSTR16_CORE0_DBG_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">CLSTR16_CORE0_DBG_CFG_DBGEN</td><td colspan="4">CLSTR16_CORE0_DBG_CFG_NIDEN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Ah</td><td colspan="4">Ah</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6877. MAIN_SEC_MMR_CFG2_CLSTR16_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR16_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug activate. Reset Source: sys_por_rst_n
11:8	CLSTR16_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug activate. Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.8 MAIN_SEC_MMR_CFG0_PID Register

1 MAIN_SEC_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800213h]

PID register

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Table 14-6878. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0000h**

Figure 14-2284. MAIN_SEC_MMR_CFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">13h</td></tr>
</table>

Table 14-6880. MAIN_SEC_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	13h	Reset Source: mod_g_rst_n

14.2.1.4.1.2.9 MAIN_SEC_MMR_CFG0_CLSTR0_DEF Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_DEF Register (Offset = 20h) [reset = 2FF10h]

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Table 14-6881. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0020h**

Figure 14-2285. MAIN_SEC_MMR_CFG0_CLSTR0_DEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					CLSTR0_DEF_CORE_NUM		
NONE					R		
0h					2h		
15	14	13	12	11	10	9	8
CLSTR0_DEF_DSP_CORE_TYPE							
R							
FFh							
7	6	5	4	3	2	1	0
CLSTR0_DEF_ARM_CORE_TYPE							
R							
10h							

Table 14-6883. MAIN_SEC_MMR_CFG0_CLSTR0_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR0_DEF_CORE_NUM	R	2h	Number of cores in cluster Reset Source: mod_g_rst_n
15:8	CLSTR0_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Reset Source: mod_g_rst_n
7:0	CLSTR0_DEF_ARM_CORE_TYPE	R	10h	ARM core type configuration Reset Source: mod_g_rst_n

14.2.1.4.1.2.10 MAIN_SEC_MMR_CFG0_CLSTR0_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CFG Register (Offset = 40h) [reset = 0h]

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Table 14-6884. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0040h**

Figure 14-2286. MAIN_SEC_MMR_CFG0_CLSTR0_CFG Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD	CLSTR0_CFG_SINGLE_CORE_ONLY	CLSTR0_CFG_SINGLE_CORE	CLSTR0_CFG_MEM_INIT_DIS	RSVD	CLSTR0_CFG_DBG_NO_CLKSTOP	CLSTR0_CFG_TEINIT	RSVD
	R	R/W	R/W		R/W	R/W	
0h	X	X	0h	0h	0h	0h	0h

Table 14-6886. MAIN_SEC_MMR_CFG0_CLSTR0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
6	CLSTR0_CFG_SINGLE_CORE_ONLY	R	X	Single / Dual CPU Mode Supported: Reset Source: sys_por_rst_n
5	CLSTR0_CFG_SINGLE_CORE	R/W	X	Single / Dual CPU Mode: Reset Source: sys_por_rst_n
4	CLSTR0_CFG_MEM_INIT_DIS	R/W	0h	Deactivates SRAM initialization (TCM, Cache Tags, etc) at reset Reset Source: mod_g_rst_n
2	CLSTR0_CFG_DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior Reset Source: sys_por_rst_n
1	CLSTR0_CFG_TEINIT	R/W	0h	Exception handling state at reset: Reset Source: sys_por_rst_n

14.2.1.4.1.2.11 MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL Register (Offset = 80h) [reset = 0h]

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Table 14-6887. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0080h**

Figure 14-2287. MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD							
R							
0h							

Table 14-6889. MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved

14.2.1.4.1.2.12 MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT Register (Offset = 90h) [reset = 0h]

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Table 14-6890. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0090h**

Figure 14-2288. MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD							
R							
0h							

Table 14-6892. MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0H	Reserved

14.2.1.4.1.2.13 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register (Offset = 100h) [reset = 880h]

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Table 14-6893. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0100h**

Figure 14-2289. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_CFG_NMFI_EN	RESERVED			CLSTR0_CORE0_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	6	5	4	3	2	1	0
CLSTR0_CORE0_CFG_BTCM_EN	RESERVED			CLSTR0_CORE0_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-6895. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR0_CORE0_CFG_NMFI_EN	R/W	0h	Activate Core0 Non-Maskable Fast Interrupts Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR0_CORE0_CFG_TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR0_CORE0_CFG_BTCM_EN	R/W	1h	Activate Core0 BTCM RAM at reset Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE0_CFG_ATCM_EN	R/W	0h	Activate Core0 ATCM RAM at reset Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.14 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register (Offset = 110h) [reset = 200h]

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Table 14-6896. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0110h**

Figure 14-2290. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	22	21	20	19	18	17	16
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	6	5	4	3	2	1	0
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-6898. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.15 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register (Offset = 114h) [reset = 0h]

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Table 14-6899. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0114h**

Figure 14-2291. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-6901. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.4.1.2.16 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register (Offset = 120h) [reset = 0h]

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Table 14-6902. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0120h**

Figure 14-2292. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLSTR0_CORE0_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-6904. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR0_CORE0_PMCTRL_CORE_HALT	R/W	0h	Halt Core0 Reset Source: sys_por_rst_n

14.2.1.4.1.2.17 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register (Offset = 130h) [reset = 0h]

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Table 14-6905. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0130h**

Figure 14-2293. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLSTR0_CORE0_PMSTAT_CLK_GATE	RESERVED	CLSTR0_CORE0_PMSTAT_WFE	CLSTR0_CORE0_PMSTAT_WFI
NONE				R	NONE	R	R
0h				X	0h	X	X

Table 14-6907. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE0_PMSTAT_CLK_GATE	R	X	Core0 Clocked stopped due to WFI or WFE state Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR0_CORE0_PMSTAT_WFE	R	X	Core0 WFE Reset Source: mod_g_rst_n
0	CLSTR0_CORE0_PMSTAT_WFI	R	X	Core0 WFI Reset Source: mod_g_rst_n

14.2.1.4.1.2.18 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG Register (Offset = 180h) [reset = 880h]

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Table 14-6908. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0180h**

Figure 14-2294. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR0_CORE1_CFG_NMFI_EN	RESERVED			CLSTR0_CORE1_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR0_CORE1_CFG_BTCM_EN	RESERVED			CLSTR0_CORE1_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-6910. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR0_CORE1_CFG_NMFI_EN	R/W	0h	Activate Core1 Non-Maskable Fast Interrupts Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR0_CORE1_CFG_TCM_RSTBASE	R/W	1h	Core1 A/BTCM Reset Base Address Indicator Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR0_CORE1_CFG_BTCM_EN	R/W	1h	Activate Core1 BTCM RAM at reset Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE1_CFG_ATCM_EN	R/W	0h	Activate Core1 ATCM RAM at reset Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.19 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO Register (Offset = 190h) [reset = 200h]

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Table 14-6911. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0190h**

Figure 14-2295. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-6913. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.20 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI Register (Offset = 194h) [reset = 0h]

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Table 14-6914. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 0194h**

Figure 14-2296. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE1_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR0_CORE1_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-6916. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR0_CORE1_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.4.1.2.21 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL Register (Offset = 1A0h) [reset = 0h]

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Table 14-6917. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 01A0h**

Figure 14-2297. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLSTR0_CORE1_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-6919. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR0_CORE1_PMCTRL_CORE_HALT	R/W	0h	Halt Core1 Reset Source: sys_por_rst_n

14.2.1.4.1.2.22 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT Register (Offset = 1B0h) [reset = 0h]

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Table 14-6920. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 01B0h**

Figure 14-2298. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLSTR0_CORE1_PMSTAT_CLK_GATE	RESERVED	CLSTR0_CORE1_PMSTAT_WFE	CLSTR0_CORE1_PMSTAT_WFI
NONE				R	NONE	R	R
0h				X	0h	X	X

Table 14-6922. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE1_PMSTAT_CLK_GATE	R	X	Core1 Clocked stopped due to WFI or WFE state Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR0_CORE1_PMSTAT_WFE	R	X	Core1 WFE Reset Source: mod_g_rst_n
0	CLSTR0_CORE1_PMSTAT_WFI	R	X	Core1 WFI Reset Source: mod_g_rst_n

14.2.1.4.1.2.23 MAIN_SEC_MMR_CFG0_CLSTR1_DEF Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_DEF Register (Offset = 1020h) [reset = 2FF10h]

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Table 14-6923. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1020h**

Figure 14-2299. MAIN_SEC_MMR_CFG0_CLSTR1_DEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					CLSTR1_DEF_CORE_NUM		
NONE					R		
0h					2h		
15	14	13	12	11	10	9	8
CLSTR1_DEF_DSP_CORE_TYPE							
R							
FFh							
7	6	5	4	3	2	1	0
CLSTR1_DEF_ARM_CORE_TYPE							
R							
10h							

Table 14-6925. MAIN_SEC_MMR_CFG0_CLSTR1_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR1_DEF_CORE_NUM	R	2h	Number of cores in cluster Reset Source: mod_g_rst_n
15:8	CLSTR1_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Reset Source: mod_g_rst_n
7:0	CLSTR1_DEF_ARM_CORE_TYPE	R	10h	ARM core type configuration Reset Source: mod_g_rst_n

14.2.1.4.1.2.24 MAIN_SEC_MMR_CFG0_CLSTR1_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CFG Register (Offset = 1040h) [reset = 0h]

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Table 14-6926. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1040h**

Figure 14-2300. MAIN_SEC_MMR_CFG0_CLSTR1_CFG Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD	CLSTR1_CFG_SINGLE_CORE_ONLY	CLSTR1_CFG_SINGLE_CORE	CLSTR1_CFG_MEM_INIT_DIS	RSVD	CLSTR1_CFG_DBG_NO_CLKSTOP	CLSTR1_CFG_TEINIT	RSVD
	R	R/W	R/W		R/W	R/W	
0h	X	X	0h	0h	0h	0h	0h

Table 14-6928. MAIN_SEC_MMR_CFG0_CLSTR1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
6	CLSTR1_CFG_SINGLE_CORE_ONLY	R	X	Single / Dual CPU Mode Supported: Reset Source: sys_por_rst_n
5	CLSTR1_CFG_SINGLE_CORE	R/W	X	Single / Dual CPU Mode: Reset Source: sys_por_rst_n
4	CLSTR1_CFG_MEM_INIT_DIS	R/W	0h	Deactivates SRAM initialization (TCM, Cache Tags, etc) at reset Reset Source: mod_g_rst_n
2	CLSTR1_CFG_DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior Reset Source: sys_por_rst_n
1	CLSTR1_CFG_TEINIT	R/W	0h	Exception handling state at reset: Reset Source: sys_por_rst_n

14.2.1.4.1.2.25 MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL Register (Offset = 1080h) [reset = 0h]

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Table 14-6929. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1080h**

Figure 14-2301. MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6931. MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved

14.2.1.4.1.2.26 MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT Register (Offset = 1090h) [reset = 0h]

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Table 14-6932. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1090h**

Figure 14-2302. MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD							
R							
0h							

Table 14-6934. MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved

14.2.1.4.1.2.27 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG Register (Offset = 1100h) [reset = 880h]

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Table 14-6935. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1100h**

Figure 14-2303. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE0_CFG_NMFI_EN	RESERVED			CLSTR1_CORE0_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	6	5	4	3	2	1	0
CLSTR1_CORE0_CFG_BTCM_EN	RESERVED			CLSTR1_CORE0_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-6937. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR1_CORE0_CFG_NMFI_EN	R/W	0h	Activate Core0 Non-Maskable Fast Interrupts Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR1_CORE0_CFG_TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR1_CORE0_CFG_BTCM_EN	R/W	1h	Activate Core0 BTCM RAM at reset Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3	CLSTR1_CORE0_CFG_ATCM_EN	R/W	0h	Activate Core0 ATCM RAM at reset Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.28 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO Register (Offset = 1110h) [reset = 200h]

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Table 14-6938. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1110h**

Figure 14-2304. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	22	21	20	19	18	17	16
CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	14	13	12	11	10	9	8
CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	6	5	4	3	2	1	0
CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-6940. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.29 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI Register (Offset = 1114h) [reset = 0h]

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Table 14-6941. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1114h**

Figure 14-2305. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR1_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-6943. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR1_CORE0_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.4.1.2.30 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL Register (Offset = 1120h) [reset = 0h]

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Table 14-6944. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1120h

Figure 14-2306. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLSTR1_CORE0_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-6946. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR1_CORE0_PMCTRL_CORE_HALT	R/W	0h	Halt Core0 Reset Source: sys_por_rst_n

14.2.1.4.1.2.31 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT Register (Offset = 1130h) [reset = 0h]

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Table 14-6947. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1130h**

Figure 14-2307. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLSTR1_CORE0_PMSTAT_CLK_GATE	RESERVED	CLSTR1_CORE0_PMSTAT_WFE	CLSTR1_CORE0_PMSTAT_WFI
NONE				R	NONE	R	R
0h				X	0h	X	X

Table 14-6949. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR1_CORE0_PMSTAT_CLK_GATE	R	X	Core0 Clocked stopped due to WFI or WFE state Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR1_CORE0_PMSTAT_WFE	R	X	Core0 WFE Reset Source: mod_g_rst_n
0	CLSTR1_CORE0_PMSTAT_WFI	R	X	Core0 WFI Reset Source: mod_g_rst_n

14.2.1.4.1.2.32 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG Register (Offset = 1180h) [reset = 880h]

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Table 14-6950. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1180h**

Figure 14-2308. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE1_CFG_NMFI_EN	RESERVED			CLSTR1_CORE1_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	6	5	4	3	2	1	0
CLSTR1_CORE1_CFG_BTCM_EN	RESERVED			CLSTR1_CORE1_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-6952. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR1_CORE1_CFG_NMFI_EN	R/W	0h	Activate Core1 Non-Maskable Fast Interrupts Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR1_CORE1_CFG_TCM_RSTBASE	R/W	1h	Core1 A/BTCM Reset Base Address Indicator Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR1_CORE1_CFG_BTCM_EN	R/W	1h	Activate Core1 BTCM RAM at reset Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3	CLSTR1_CORE1_CFG_ATCM_EN	R/W	0h	Activate Core1 ATCM RAM at reset Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.33 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO Register (Offset = 1190h) [reset = 200h]

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Table 14-6953. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1190h**

Figure 14-2309. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-6955. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.4.1.2.34 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI Register (Offset = 1194h) [reset = 0h]

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Table 14-6956. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 1194h**

Figure 14-2310. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE1_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR1_CORE1_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-6958. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR1_CORE1_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.4.1.2.35 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL Register (Offset = 11A0h) [reset = 0h]

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Table 14-6959. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 11A0h**

Figure 14-2311. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLSTR1_CORE1_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-6961. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR1_CORE1_PMCTRL_CORE_HALT	R/W	0h	Halt Core1 Reset Source: sys_por_rst_n

14.2.1.4.1.2.36 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT Register (Offset = 11B0h) [reset = 0h]

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Table 14-6962. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 11B0h**

Figure 14-2312. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLSTR1_CORE1_PMSTAT_CLK_GATE	RESERVED	CLSTR1_CORE1_PMSTAT_WFE	CLSTR1_CORE1_PMSTAT_WFI
NONE				R	NONE	R	R
0h				X	0h	X	X

Table 14-6964. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR1_CORE1_PMSTAT_CLK_GATE	R	X	Core1 Clocked stopped due to WFI or WFE state Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR1_CORE1_PMSTAT_WFE	R	X	Core1 WFE Reset Source: mod_g_rst_n
0	CLSTR1_CORE1_PMSTAT_WFI	R	X	Core1 WFI Reset Source: mod_g_rst_n

14.2.1.4.1.2.37 MAIN_SEC_MMR_CFG0_CLSTR9_DEF Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_DEF Register (Offset = 9020h) [reset = 1FF00h]

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Table 14-6965. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9020h**

Figure 14-2313. MAIN_SEC_MMR_CFG0_CLSTR9_DEF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CLSTR9_DEF_CORE_NUM</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLSTR9_DEF_DSP_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLSTR9_DEF_ARM_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6967. MAIN_SEC_MMR_CFG0_CLSTR9_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	CLSTR9_DEF_CORE_NUM	R	1h	Number of cores in cluster Reset Source: mod_g_rst_n
15:8	CLSTR9_DEF_DSP_CORE_TYPE	R	FFh	Field values (others are reserved): Reset Source: mod_g_rst_n
7:0	CLSTR9_DEF_ARM_CORE_TYPE	R	0h	Field values (others are reserved): Reset Source: mod_g_rst_n

14.2.1.4.1.2.38 MAIN_SEC_MMR_CFG0_CLSTR9_CFG Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CFG Register (Offset = 9040h) [reset = 3h]

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Table 14-6968. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9040h**

Figure 14-2314. MAIN_SEC_MMR_CFG0_CLSTR9_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CLSTR9_CONFIG0_CP15_DISABLE1	CLSTR9_CONFIG0_CP15_DISABLE0
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED		CLSTR9_CONFIG0_CONFIG_TE1	CLSTR9_CONFIG0_CONFIG_TE0	RESERVED		CLSTR9_CONFIG0_AARCH1	CLSTR9_CONFIG0_AARCH0
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	0h	0h		1h	1h

Table 14-6970. MAIN_SEC_MMR_CFG0_CLSTR9_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CLSTR9_CONFIG0_CP15_DISABLE1	R/W	0h	Deactivate write access to secure CP15 registers for Core1 Reset Source: mod_g_rst_n
8	CLSTR9_CONFIG0_CP15_DISABLE0	R/W	0h	Deactivate write access to secure CP15 registers for Core0 Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLSTR9_CONFIG0_CONFIG_TE1	R/W	0h	Activate T32 exceptions for Core1 Reset Source: mod_g_rst_n
4	CLSTR9_CONFIG0_CONFIG_TE0	R/W	0h	Activate T32 exceptions for Core0 Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	CLSTR9_CONFIG0_AARCH1	R/W	1h	Core1 ARM Architecture configuration Reset Source: mod_g_rst_n
0	CLSTR9_CONFIG0_AARCH0	R/W	1h	Core0 ARM Architecture configuration Reset Source: mod_g_rst_n

14.2.1.4.1.2.39 MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Register (Offset = 9080h) [reset = 300h]

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Table 14-6971. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9080h**

Figure 14-2315. MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			CLSTR9_PM_CONFIG_L2RSTDISABLE	RESERVED		CLSTR9_PM_CONFIG_DBGPWRUP1	CLSTR9_PM_CONFIG_DBGPWRUP0
NONE			R/W	NONE		R/W	R/W
0h			0h	0h		1h	1h
7	6	5	4	3	2	1	0
CLSTR9_PM_CONFIG_DBGL1RSTDISABLE	CLSTR9_PM_CONFIG_CLEAR_MON	CLSTR9_PM_CONFIG_L2_FLUSHREQ	RESERVED			CLSTR9_PM_CONFIG_ACP_MASTER	CLSTR9_PM_CONFIG_SNOOP_IF
R/W	R/W	R/W	NONE			R/W	R/W
0h	0h	0h	0h			0h	0h

Table 14-6973. MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	CLSTR9_PM_CONFIG_L2RSTDISABLE	R/W	0h	Deactivate L2 cache automatic invalidate on reset functionality. Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9	CLSTR9_PM_CONFIG_DBGPWRUP1	R/W	1h	Core1 powered up Reset Source: mod_g_rst_n
8	CLSTR9_PM_CONFIG_DBGPWRUP0	R/W	1h	Core0 powered up Reset Source: mod_g_rst_n
7	CLSTR9_PM_CONFIG_DBGL1RSTDISABLE	R/W	0h	Deactivate L1 data cache automatic invalidate on reset functionality. Reset Source: mod_g_rst_n
6	CLSTR9_PM_CONFIG_CLEAR_MON	R/W	0h	Request to clear the external global exclusive monitor. Reset Source: mod_g_rst_n
5	CLSTR9_PM_CONFIG_L2_FLUSHREQ	R/W	0h	ARM L2 hardware flush request Reset Source: mod_g_rst_n
4:2	RESERVED	NONE	0h	Reserved

Table 14-6973. MAIN_SEC_MMR_CFG0_CLSTR9_PMCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLSTR9_PM_CONFIG_ACP_MASTER	R/W	0h	ACP Controller is inactive and is not participating in coherency. There must Reset Source: mod_g_rst_n
0	CLSTR9_PM_CONFIG_SNOOP_IF	R/W	0h	Snoop interface is inactive and not participating in coherency: Reset Source: mod_g_rst_n

14.2.1.4.1.2.40 MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Register (Offset = 9090h) [reset = 0h]

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Table 14-6974. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9090h**

Figure 14-2316. MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	CLSTR9_PM_STATUS_CLEAR_MONITOR_ACK	CLSTR9_PM_STATUS_STANDBY_WFI_L2	CLSTR9_PM_STATUS_L2_HW_FLUSH	RESERVED		CLSTR9_PM_STATUS_CORE1_SMPEN	CLSTR9_PM_STATUS_CORE0_SMPEN
NONE	R	R	R	NONE		R	R
0h	X	X	X	0h		X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLSTR9_PM_STATUS_CORE1_WFE	CLSTR9_PM_STATUS_CORE0_WFE	RESERVED		CLSTR9_PM_STATUS_CORE1_WFI	CLSTR9_PM_STATUS_CORE0_WFI
NONE		R	R	NONE		R	R
0h		X	X	0h		X	X

Table 14-6976. MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	CLSTR9_PM_STATUS_CLEAR_MONITOR_ACK	R	X	External global exclusive monitor clear acknowledge. Reset Source: mod_g_rst_n
13	CLSTR9_PM_STATUS_STANDBY_WFI_L2	R	X	Indicates L2 low power state Reset Source: mod_g_rst_n
12	CLSTR9_PM_STATUS_L2_HW_FLUSH	R	X	L2 hardware flush complete Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9	CLSTR9_PM_STATUS_CORE1_SMPEN	R	X	Core1 coherency indicator Reset Source: mod_g_rst_n
8	CLSTR9_PM_STATUS_CORE0_SMPEN	R	X	Core0 coherency indicator Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLSTR9_PM_STATUS_CORE1_WFE	R	X	Core1 WFE Reset Source: mod_g_rst_n

Table 14-6976. MAIN_SEC_MMR_CFG0_CLSTR9_PMSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CLSTR9_PM_STATUS_CORE0_WFE	R	X	Core0 WFE Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	CLSTR9_PM_STATUS_CORE1_WFI	R	X	Core1 WFI Reset Source: mod_g_rst_n
0	CLSTR9_PM_STATUS_CORE0_WFI	R	X	Core0 WFI Reset Source: mod_g_rst_n

14.2.1.4.1.2.41 MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO Register (Offset = 9110h) [reset = 0h]

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Table 14-6977. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9110h**

Figure 14-2317. MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-6979. MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR9_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO	R/W	0h	Core0 - Reset base vector (v8 Mode) Address[33:2] Reset Source: mod_g_rst_n

14.2.1.4.1.2.42 MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI Register (Offset = 9114h) [reset = 0h]

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Table 14-6980. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9114h**

Figure 14-2318. MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CLSTR9_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-6982. MAIN_SEC_MMR_CFG0_CLSTR9_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR9_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	R/W	0h	Core0 - Reset base vector (v8 Mode) Address[35:34] Reset Source: mod_g_rst_n

14.2.1.4.1.2.43 MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO Register (Offset = 9190h) [reset = 0h]

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Table 14-6983. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9190h**

Figure 14-2319. MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-6985. MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR9_RST_VEC_LO_CORE1_RESET_BASE_VECTOR_LO	R/W	0h	Core0 - Reset base vector (v8 Mode) Address[33:2] Reset Source: mod_g_rst_n

14.2.1.4.1.2.44 MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI Register

1 MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI Register (Offset = 9194h) [reset = 0h]

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Table 14-6986. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A0 9194h**

Figure 14-2320. MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CLSTR9_RST_VEC_HI_CORE1_RESET_BASE_VECTOR_HI	
NONE						R/W	
0h						0h	

Table 14-6988. MAIN_SEC_MMR_CFG0_CLSTR9_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR9_RST_VEC_HI_CORE1_RESET_BASE_VECTOR_HI	R/W	0h	Core0 - Reset base vector (v8 Mode) Address[35:34] Reset Source: mod_g_rst_n

14.2.1.4.1.2.45 MAIN_SEC_MMR_CFG0_CLSTR16_DEF Register

1 MAIN_SEC_MMR_CFG0_CLSTR16_DEF Register (Offset = 10020h) [reset = 1FF11h]

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Table 14-6989. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A1 0020h**

Figure 14-2321. MAIN_SEC_MMR_CFG0_CLSTR16_DEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					CLSTR16_DEF_CORE_NUM		
NONE					R		
0h					1h		
15	14	13	12	11	10	9	8
CLSTR16_DEF_DSP_CORE_TYPE							
R							
FFh							
7	6	5	4	3	2	1	0
CLSTR16_DEF_ARM_CORE_TYPE							
R							
11h							

Table 14-6991. MAIN_SEC_MMR_CFG0_CLSTR16_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR16_DEF_CORE_NUM	R	1h	Number of cores in cluster Reset Source: mod_g_rst_n
15:8	CLSTR16_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Reset Source: mod_g_rst_n
7:0	CLSTR16_DEF_ARM_CORE_TYPE	R	11h	ARM core type configuration Reset Source: mod_g_rst_n

14.2.1.4.1.2.46 MAIN_SEC_MMR_CFG0_CLSTR16_CORE0_PMSTAT Register

1 MAIN_SEC_MMR_CFG0_CLSTR16_CORE0_PMSTAT Register (Offset = 10130h) [reset = 0h]

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Table 14-6992. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A1 0130h**

Figure 14-2322. MAIN_SEC_MMR_CFG0_CLSTR16_CORE0_PMSTAT Name Register

31	30	29	28	27	26	25	24
RSVD							
0h							
23	22	21	20	19	18	17	16
RSVD							
0h							
15	14	13	12	11	10	9	8
RSVD							
0h							
7	6	5	4	3	2	1	0
RSVD							CLSTR16_CORE0_PMSTAT_WFI
							R
0h							X

Table 14-6994. MAIN_SEC_MMR_CFG0_CLSTR16_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	CLSTR16_CORE0_PMSTAT_WFI	R	X	M4FSS Sleeping Status Reset Source: mod_g_rst_n

14.2.1.4.1.2.47 MAIN_SEC_MMR_CFG0_GIC_CONFIG Register

1 MAIN_SEC_MMR_CFG0_GIC_CONFIG Register (Offset = 18008h) [reset = 300h]

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Table 14-6995. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	**45A1 8008h**

Figure 14-2323. MAIN_SEC_MMR_CFG0_GIC_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						GIC_CONFIG_A53SS0_CORE1_ACTIVE	GIC_CONFIG_A53SS0_CORE0_ACTIVE
NONE						R/W	R/W
0h						1h	1h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6997. MAIN_SEC_MMR_CFG0_GIC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	GIC_CONFIG_A53SS0_CORE1_ACTIVE	R/W	1h	Drives GIC cpu_active input for A53SS0 Core1. Reset Source: mod_g_rst_n
8	GIC_CONFIG_A53SS0_CORE0_ACTIVE	R/W	1h	Drives GIC cpu_active input for A53SS0 Core0. Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2 Power Registers

14.2.2.1 VTM

VTM

14.2.2.1.1 VTM Summaries

VTM Summaries

Table 14-6998. VTM_CFG1 Registers, Base Address=00B0 0000h, Length=1024

Offset	Length	Register Name	VTM0 Physical Address
0h	32	VTM_CFG1_PID	00B0 0000h
4h	32	VTM_CFG1_DEVINFO_PWR0	00B0 0004h
204h	32	VTM_CFG1_GT_TH1_INT_RAW_STAT_SET	00B0 0204h
208h	32	VTM_CFG1_GT_TH1_INT_EN_STAT_CLR	00B0 0208h
214h	32	VTM_CFG1_GT_TH1_INT_EN_SET	00B0 0214h
218h	32	VTM_CFG1_GT_TH1_INT_EN_CLR	00B0 0218h
224h	32	VTM_CFG1_GT_TH2_INT_RAW_STAT_SET	00B0 0224h
228h	32	VTM_CFG1_GT_TH2_INT_EN_STAT_CLR	00B0 0228h
234h	32	VTM_CFG1_GT_TH2_INT_EN_SET	00B0 0234h
238h	32	VTM_CFG1_GT_TH2_INT_EN_CLR	00B0 0238h
244h	32	VTM_CFG1_LT_TH0_INT_RAW_STAT_SET	00B0 0244h
248h	32	VTM_CFG1_LT_TH0_INT_EN_STAT_CLR	00B0 0248h
254h	32	VTM_CFG1_LT_TH0_INT_EN_SET	00B0 0254h
258h	32	VTM_CFG1_LT_TH0_INT_EN_CLR	00B0 0258h
0h	32	VTM_CFG1_VD_DEVINFO_J	00B0 0000h + formula
4h	32	VTM_CFG1_VD_OPPVID_J	00B0 0004h + formula
8h	32	VTM_CFG1_VD_EVT_STAT_J	00B0 0008h + formula
Ch	32	VTM_CFG1_VD_EVT_SET_J	00B0 000Ch + formula
10h	32	VTM_CFG1_VD_EVT_CLR_J	00B0 0010h + formula
0h	32	VTM_CFG1_TMPSENS_CTRL_J	00B0 0000h + formula
8h	32	VTM_CFG1_TMPSENS_STAT_J	00B0 0008h + formula
Ch	32	VTM_CFG1_TMPSENS_TH_J	00B0 000Ch + formula
10h	32	VTM_CFG1_TMPSENS_TH2_J	00B0 0010h + formula

Table 14-6999. VTM_CFG2 Registers, Base Address=00B0 1000h, Length=1024

Offset	Length	Register Name	VTM0 Physical Address
8h	32	VTM_CFG2_CLK_CTRL	00B0 1008h
Ch	32	VTM_CFG2_MISC_CTRL	00B0 100Ch
10h	32	VTM_CFG2_MISC_CTRL2	00B0 1010h
20h	32	VTM_CFG2_SAMPLE_CTRL	00B0 1020h
0h	32	VTM_CFG2_TMPSENS_CTRL_J	00B0 1000h + formula
4h	32	VTM_CFG2_TMPSENS_TRIM_J	00B0 1004h + formula

Table 14-7000. ECC_AGGR Registers, Base Address=00B0 2000h, Length=1024

Offset	Length	Register Name	VTM0 Physical Address
0h	32	ECC_AGGR_REV	00B0 2000h
8h	32	ECC_AGGR_VECTOR	00B0 2008h

Table 14-7000. ECC_AGGR Registers, Base Address=00B0 2000h, Length=1024 (continued)

Offset	Length	Register Name	VTM0 Physical Address
Ch	32	ECC_AGGR_STAT	00B0 200Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	00B0 2010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	00B0 203Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	00B0 2040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	00B0 2080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	00B0 20C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	00B0 213Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	00B0 2140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	00B0 2180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	00B0 21C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	00B0 2200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	00B0 2204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	00B0 2208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	00B0 220Ch

14.2.2.1.2 VTM Registers

VTM Registers

14.2.2.1.2.1 VTM_CFG1_PID Register

1 VTM_CFG1_PID Register (Offset = 0h) [reset = 661B8101h]

VTM Peripheral Identification Register

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Table 14-7001. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0000h**

Figure 14-2324. VTM_CFG1_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		61Bh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
61Bh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_RTL					X_MAJOR		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		Y_MINOR					
R		R					
0h		1h					

Table 14-7003. VTM_CFG1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: mod_g_rst_n
29:28	BU	R	2h	Business unit - Processors Reset Source: mod_g_rst_n
27:16	FUNC	R	61Bh	Module functional identifier - CTRL MMR Reset Source: mod_g_rst_n
15:11	R_RTL	R	10h	RTL revision number - actual value determined by RTL Reset Source: mod_g_rst_n
10:8	X_MAJOR	R	1h	Major revision number - actual value determined by RTL Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom revision number - actual value determined by RTL Reset Source: mod_g_rst_n
5:0	Y_MINOR	R	1h	Minor revision number - actual value determined by RTL Reset Source: mod_g_rst_n

14.2.2.1.2.2 VTM_CFG1_DEVINFO_PWR0 Register

1 VTM_CFG1_DEVINFO_PWR0 Register (Offset = 4h) [reset = 0h]

Device specific voltage domain and temp sensor information register.

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Table 14-7004. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0004h**

Figure 14-2325. VTM_CFG1_DEVINFO_PWR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">VTM_VD_MAP</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>VD_RTC</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>X</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">TMPSENS_CT</td><td colspan="4">CVD_CT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">X</td><td colspan="4">X</td></tr>
</table>

Table 14-7006. VTM_CFG1_DEVINFO_PWR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	VTM_VD_MAP	R	X	Core voltage domain, cVD, global mapping 4-bit code, in the context of this SOC. It shows in which cVD this VTM is instantiated/placed. This field indicates in which core voltage domain, cVD, has been physically placed this VTM. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff, d_vtm_vd_map. Reset Source: mod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12	VD_RTC	R	X	RTC voltage domain presence. 0: There is NO VD_RTC in this SOC. 1: There is a VD_RTC in this SOC. Reset value is a VTM tieoff, d_vd_rtc. Reset Source: mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	TMPSENS_CT	R	X	Number of temperature sensors associated with this VTM. Valid values are 4'h0 - 4'h8. 0x0: NO temp-sensor associated to this VTM. 0x8: 8 temp-sensors associated to this VTM. 0x9 to 0xF: invalid values. Reset value is a VTM tieoff, d_vtm_tmpsens_ct. Reset Source: mod_g_rst_n

Table 14-7006. VTM_CFG1_DEVINFO_PWR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CVD_CT	R	X	Number of core voltage domains in device. VD0 is always allocated to VD_RTC, if it exists, and VD1 always to VD_WKUP. The maximum number of cVDs in an SOC is 15, 0xF. Reset value is a VTM tieoff, d_device_cvd_ct. Reset Source: mod_g_rst_n

14.2.2.1.2.3 VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register

1 VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register (Offset = 204h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7007. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0204h**

Figure 14-2326. VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7009. VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the pending stats regardless of the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.1.2.4 VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register

1 VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register (Offset = 208h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt GT_TH1 per voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7010. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0208h**

Figure 14-2327. VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7012. VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt masked pending bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status that includes the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.1.2.5 VTM_CFG1_GT_TH1_INT_EN_SET Register

1 VTM_CFG1_GT_TH1_INT_EN_SET Register (Offset = 214h) [reset = 0h]

Enable set MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7013. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0214h**

Figure 14-2328. VTM_CFG1_GT_TH1_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7015. VTM_CFG1_GT_TH1_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.1.2.6 VTM_CFG1_GT_TH1_INT_EN_CLR Register

1 VTM_CFG1_GT_TH1_INT_EN_CLR Register (Offset = 218h) [reset = 0h]

Enable clear MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7016. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0218h**

Figure 14-2329. VTM_CFG1_GT_TH1_INT_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7018. VTM_CFG1_GT_TH1_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.1.2.7 VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register

1 VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register (Offset = 224h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7019. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0224h**

Figure 14-2330. VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7021. VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the pending status regardless of the enable setting. Reset Source: mod_g_rst_n

14.2.2.1.2.8 VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register

1 VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register (Offset = 228h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt GT_TH2 per voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7022. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0228h**

Figure 14-2331. VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7024. VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enabled pending bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status including the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.1.2.9 VTM_CFG1_GT_TH2_INT_EN_SET Register

1 VTM_CFG1_GT_TH2_INT_EN_SET Register (Offset = 234h) [reset = 0h]

Enable set MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7025. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0234h**

Figure 14-2332. VTM_CFG1_GT_TH2_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7027. VTM_CFG1_GT_TH2_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.1.2.10 VTM_CFG1_GT_TH2_INT_EN_CLR Register

1 VTM_CFG1_GT_TH2_INT_EN_CLR Register (Offset = 238h) [reset = 0h]

Enable clear MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7028. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0238h**

Figure 14-2333. VTM_CFG1_GT_TH2_INT_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7030. VTM_CFG1_GT_TH2_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.1.2.11 VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register

1 VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register (Offset = 244h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7031. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0244h**

Figure 14-2334. VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7033. VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the raw pending status regardless of the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.1.2.12 VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register

1 VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register (Offset = 248h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt LT_TH0 per voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7034. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0248h**

Figure 14-2335. VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7036. VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enabled pending status bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status that factors in the corresponding enable along with the pending status. Reset Source: mod_g_rst_n

14.2.2.1.2.13 VTM_CFG1_LT_TH0_INT_EN_SET Register

1 VTM_CFG1_LT_TH0_INT_EN_SET Register (Offset = 254h) [reset = 0h]

Enable set MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7037. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0254h**

Figure 14-2336. VTM_CFG1_LT_TH0_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7039. VTM_CFG1_LT_TH0_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.1.2.14 VTM_CFG1_LT_TH0_INT_EN_CLR Register

1 VTM_CFG1_LT_TH0_INT_EN_CLR Register (Offset = 258h) [reset = 0h]

Enable clear MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7040. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0258h**

Figure 14-2337. VTM_CFG1_LT_TH0_INT_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7042. VTM_CFG1_LT_TH0_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.1.2.15 VTM_CFG1_VD_DEVINFO_j Register

1 VTM_CFG1_VD_DEVINFO_j Register (Offset = 0h + formula) [reset = 0h]

Voltage domain a information register. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7043. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0000h + formula**

Figure 14-2338. VTM_CFG1_VD_DEVINFO_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			AVS0_SUP	VD_MAP			
NONE			R/W	R			
0h			X	X			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7045. VTM_CFG1_VD_DEVINFO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	AVS0_SUP	R/W	X	Indicates VD0 AVS class0 support. Indicates if the cVD associated with this VTM's VD MMR supports AVS-Class0: 0: No AVS-Class0. 1: Supports-AVS-Class0. Reset value is from e-fuse at module reset, efuse_vd[j]_avs_sup. Reset Source: mod_g_rst_n
11:8	VD_MAP	R	X	Indicates the core voltage domain mapping of VTM VD. Device specific field. This field indicates to which SOC cVD is this VD of this VTM map to. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff, d_vd[j]_vd_map_ipcfg. Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.1.2.16 VTM_CFG1_VD_OPPVID_j Register

1 VTM_CFG1_VD_OPPVID_j Register (Offset = 4h + formula) [reset = 0h]

Voltage domain a VID actual code used as reference by Firmware to set the various voltage domain supply voltages. Reset defaults are sourced from efuse for each OPP. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7046. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0004h + formula**

Figure 14-2339. VTM_CFG1_VD_OPPVID_j Name Register

31	30	29	28	27	26	25	24
OPP_3							
R/W							
X							
23	22	21	20	19	18	17	16
OPP_2							
R/W							
X							
15	14	13	12	11	10	9	8
OPP_1							
R/W							
X							
7	6	5	4	3	2	1	0
OPP_0							
R/W							
X							

Table 14-7048. VTM_CFG1_VD_OPPVID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	OPP_3	R/W	X	OPP 3 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_3. Reset Source: mod_por_rst_n
23:16	OPP_2	R/W	X	OPP 2 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_2. Reset Source: mod_por_rst_n
15:8	OPP_1	R/W	X	OPP 1 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_1. Reset Source: mod_por_rst_n

Table 14-7048. VTM_CFG1_VD_OPPVID_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	OPP_0	R/W	X	OPP 0 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_0. Reset Source: mod_por_rst_n

14.2.2.1.2.17 VTM_CFG1_VD_EVT_STAT_j Register

1 VTM_CFG1_VD_EVT_STAT_j Register (Offset = 8h + formula) [reset = 0h]

Voltage domain a event and control status register.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7049. Instance Table

Instance Name	Physical Address
VTM0	00B0 0008h + formula

Figure 14-2340. VTM_CFG1_VD_EVT_STAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LT_TH0_ALERT	GT_TH2_ALERT	GT_TH1_ALERT
NONE					R	R	R
0h					X	X	X

Table 14-7051. VTM_CFG1_VD_EVT_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LT_TH0_ALERT	R	X	This bit reflects the status of the TH0 undertemp alert resulting from the AND of all the similar alerts produced by the temp sensors selected by VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. Reset Source: mod_g_rst_n
1	GT_TH2_ALERT	R	X	This bit reflects the status of the merged temperature alert resulting from the combination of all the similar alerts produced by the temp-monitors selected as showed in field VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. This field shows the actual present level of the resulting OR function of the combined selected signals. Reset Source: mod_g_rst_n
0	GT_TH1_ALERT	R	X	This bit reflects the status of the merged temperature alert resulting from the OR of all the similar alerts produced by the temp-monitors selected as showed in field VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. This field shows the actual present value of the resulting OR function of the combined selected signals. Reset Source: mod_g_rst_n

14.2.2.1.2.18 VTM_CFG1_VD_EVT_SET_j Register

1 VTM_CFG1_VD_EVT_SET_j Register (Offset = Ch + formula) [reset = 0h]

Voltage domain a event select and control set register. NOTE: This MMR and the companion MMR VTM_VD[a]_EVT_SEL_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7052. Instance Table

Instance Name	Physical Address
VTM0	**00B0 000Ch + formula**

Figure 14-2341. VTM_CFG1_VD_EVT_SET_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TSENS_EVT_SEL							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7054. VTM_CFG1_VD_EVT_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TSENS_EVT_SEL	R/W1TS	0h	In this field we select which of the event contributions of the 8-maximum possible temp-monitors controlled by this VTM will contribute to generate the merged event/alerts of this VD. Any combination of them could be selected and varies between SOCs and VDs. Eg: 0x00 : No temp-monitor event contributes to generate the temperature events of this VD. 0x06: Temp-monitors[2,1] contribute to generate the temperature events of this VD. ... 0xFF: All 8 temp-monitors contribute to generate the temperature events of this VD. 0: Writing 0 to this field produces no effect. 1: Writing 1 to any of the bits in this field sets to 1 the corresponding bit in that field. Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.2.1.2.19 VTM_CFG1_VD_EVT_CLR_j Register

1 VTM_CFG1_VD_EVT_CLR_j Register (Offset = 10h + formula) [reset = 0h]

Voltage domain a event select and control clear register. NOTE: This MMR and the companion MMR VTM_VD[a]_EVT_SEL_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7055. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0010h + formula**

Figure 14-2342. VTM_CFG1_VD_EVT_CLR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TSENS_EVT_SEL							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7057. VTM_CFG1_VD_EVT_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TSENS_EVT_SEL	R/W1TC	0h	In this field we select which of the event contributions of the 8-maximum possible temp-monitors controlled by this VTM will contribute to generate the merged event/alerts of this VD. Any combination of them could be selected and varies between SOCs and VDs. Eg: 0x00 : No temp-monitor event contributes to generate the temperature events of this VD. 0x06: Temp-monitors[2,1] contribute to generate the temperature events of this VD. ... 0xFF: All 8 temp-monitors contribute to generate the temperature events of this VD. 0: Writing 0 to this field produces no effect. 1: Writing 1 to any of the bits in this field clears, = 0, the corresponding bit in that field. Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.2.1.2.20 VTM_CFG1_TMPSENS_CTRL_j Register

1 VTM_CFG1_TMPSENS_CTRL_j Register (Offset = 0h + formula) [reset = 0h]

Temperature Sensor Band-gap control register for sensor j.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7058. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0000h + formula**

Figure 14-2343. VTM_CFG1_TMPSENS_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					LT_TH0_EN	GT_TH2_EN	GT_TH1_EN
NONE					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7060. VTM_CFG1_TMPSENS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	LT_TH0_EN	R/W	0h	Enable under-threshold0 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is < value set for threshold point 0. Reset value is POR only. Reset Source: mod_por_rst_n
9	GT_TH2_EN	R/W	0h	Enable over-threshold2 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is > value set for threshold point 2. Reset value is POR only. Reset Source: mod_por_rst_n
8	GT_TH1_EN	R/W	0h	Enable over-threshold1 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is > value set for threshold point 1. Reset value is POR only. Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.1.2.21 VTM_CFG1_TMPSENS_STAT_j Register

1 VTM_CFG1_TMPSENS_STAT_j Register (Offset = 8h + formula) [reset = 0h]

Temperature Sensor Band-gap Status register for sensor j.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7061. Instance Table

Instance Name	Physical Address
VTM0	00B0 0008h + formula

Figure 14-2344. VTM_CFG1_TMPSENS_STAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				VD_MAP			
NONE				R			
0h				X			
15	14	13	12	11	10	9	8
MAXT_OUTRG_ALERT	LT_TH0_ALERT	GT_TH2_ALERT	GT_TH1_ALERT	EOC_FC_UPDATE	DATA_VALID	DATA_OUT	
R	R	R	R	R	R	R	
X	0h	0h	0h	0h	X	X	
7	6	5	4	3	2	1	0
DATA_OUT							
R							
X							

Table 14-7063. VTM_CFG1_TMPSENS_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	VD_MAP	R	X	Indicates the core voltage domain placement of the temp sensor. Device specific field. This field indicates in which core voltage domain, cVD, has been physically placed the temp-monitor. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff at POR, d_VTM_TMPSENS[j]_STAT_vd_map_ipcfg. Reset Source: mod_por_rst_n
15	MAXT_OUTRG_ALERT	R	X	This bit will be driven to a level 1 for a given temperature monitor if it has its corresponding bit maxt_outrg_en = 1, and the temperature reading is reporting to be outside the max temperature supported, temp > programmed value. The level of this signal is a reflection, with some clock delays, of the temperature code reading. This is NOT an sticky bit. Reset value is POR only. Reset Source: mod_por_rst_n

Table 14-7063. VTM_CFG1_TMPSENS_STAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	LT_TH0_ALERT	R	0h	This field reflects the status of the lt_th0_alert comparator result. The control MMR field lt_th0_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n
13	GT_TH2_ALERT	R	0h	This field reflects the status of the gt_th2_alert comparator result. The control MMR field gt_th2_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n
12	GT_TH1_ALERT	R	0h	This field reflects the status of the gt_th1_alert comparator result. The control MMR field gt_th1_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n
11	EOC_FC_UPDATE	R	0h	First time end of conversion. This field is reset to 0 every time VTM.por_rst_n or VTM_TMPSENS[j]_CTRL.clrz are active, or when continuous mode is deasserted. This bit will be set to 1 after the first time after reset release that data_valid transitions from 0 to 1, and remain at 1 until next time either of por_rst_n or VTM_TMPSENS[j]_CTRL.clrz are active, or when continuous mode is deasserted. Reset value is at POR or VTM_TMPSENS[j]_CTRL.clrz, or continuous mode deassertion. Reset Source: mod_por_rst_n
10	DATA_VALID	R	X	Data_valid signal value from sensor: ADC End of Conversion. End of conversion indicated by 0 to 1 transition. When high data_out(9:0) out of the temp-monitor is valid. This field doesn't reflect the instantaneous output from the temp-monitor. This field gets latched/updated in this VTM register when the data_valid value from temp-monitor toggles. Reset value is at POR or VTM_TMPSENS[j]_CTRL.clrz. Reset Source: mod_por_rst_n
9:0	DATA_OUT	R	X	Data_out signal value from sensor: Temperature data from the ADC in monitor. Valid after VTM_TMPSENS[j]_STAT.eoc_fc_update = 1. This value will be latched in this VTM register every time monitor output data_valid transitions from 0 to 1. Reset value is POR only. Reset Source: mod_por_rst_n

14.2.2.1.2.22 VTM_CFG1_TMPSENS_TH_j Register

1 VTM_CFG1_TMPSENS_TH_j Register (Offset = Ch + formula) [reset = 0h]

Temperature Sensor Band-gap Threshold register for sensor j.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7064. Instance Table

Instance Name	Physical Address
VTM0	**00B0 000Ch + formula**

Figure 14-2345. VTM_CFG1_TMPSENS_TH_j Name Register

31	30	29	28	27	26	25	24
RESERVED						TH1_VAL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
TH1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						TH0_VAL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TH0_VAL							
R/W							
0h							

Table 14-7066. VTM_CFG1_TMPSENS_TH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TH1_VAL	R/W	0h	Threshold point-1, thpt1, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is > th1_val[9:0] and gt_th1_en=1, that will cause the VTM to set the gt_th1_alert output. Once the current temp reading =< th1_val[9:0] then gt_th1_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TH0_VAL	R/W	0h	Threshold point-0, thpt0, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is < th0_val[9:0] and lt_th0_en=1, that will cause the VTM to set the lt_th0_alert output. Once the current temp reading => th0_val[9:0] then lt_th0_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n

14.2.2.1.2.23 VTM_CFG1_TMPSENS_TH2_j Register

1 VTM_CFG1_TMPSENS_TH2_j Register (Offset = 10h + formula) [reset = 0h]

Temperature Sensor Band-gap Threshold register 2 for sensor j.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7067. Instance Table

Instance Name	Physical Address
VTM0	**00B0 0010h + formula**

Figure 14-2346. VTM_CFG1_TMPSENS_TH2_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TH2_VAL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TH2_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7069. VTM_CFG1_TMPSENS_TH2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TH2_VAL	R/W	0h	Threshold point-2, thpt2, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is > th2_val[9:0] and gt_th2_en=1, that will cause the VTM to set the gt_th2_alert output. Once the current temp reading =< th2_val[9:0] then gt_th2_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n

14.2.2.1.2.24 VTM_CFG2_CLK_CTRL Register

1 VTM_CFG2_CLK_CTRL Register (Offset = 8h) [reset = 0h]

VTM clock related control MMR. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary. The e-fuse value is sampled from input port efuse_tsens_clk_src_div. The tsens_clks_src_div field is Device specific.

Return to Summary Table

Table 14-7070. Instance Table

Instance Name	Physical Address
VTM0	**00B0 1008h**

Figure 14-2347. VTM_CFG2_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>TSENS_CLK_SEL</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TSENS_CLK_DIV</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-7072. VTM_CFG2_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TSENS_CLK_SEL	R/W	0h	Temperature sensor clock source selector. Device specific. 0 = fix_ref_clk as source. 1 = fix_ref2_clk as source. Reset value is at POR only. Reset Source: mod_por_rst_n
30:5	RESERVED	NONE	0h	Reserved
4:0	TSENS_CLK_DIV	R/W	0h	Temperature sensor clock source divider selector. Device specific. Default set by e-fuse or tie-off. Divider uses select reference clock as source. 0 = 1x divide. 1 = 2x divide. ... 15 = 16x divide. ... 63 = 64x divide. Reset value is from e-fuse at POR, efuse_tsens_clk_src_div. Reset Source: mod_por_rst_n

14.2.2.1.2.25 VTM_CFG2_MISC_CTRL Register

1 VTM_CFG2_MISC_CTRL Register (Offset = Ch) [reset = 0h]

VTM miscellaneous control bits.

Return to Summary Table

Table 14-7073. Instance Table

Instance Name	Physical Address
VTM0	**00B0 100Ch**

Figure 14-2348. VTM_CFG2_MISC_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ANY_MAXT_OUTRG_ALERT_EN
NONE							R/W
0h							0h

Table 14-7075. VTM_CFG2_MISC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ANY_MAXT_OUTRG_ALERT_EN	R/W	0h	This bit when enabled will cause the VTM's output therm_maxtemp_outrange_alert to be driven high, if any of the sources for the maxt_outrg_alert, is set high. Whenever all the maxt_outrg_alert enabled sensor alerts, out of the 8 possible are back to 0 then the output, therm_maxtemp_outrange_alert, will also return to 0. Reset is at POR only. Reset Source: mod_por_rst_n

14.2.2.1.2.26 VTM_CFG2_MISC_CTRL2 Register

1 VTM_CFG2_MISC_CTRL2 Register (Offset = 10h) [reset = 0h]

VTM miscellaneous control bits.

Return to Summary Table

Table 14-7076. Instance Table

Instance Name	Physical Address
VTM0	**00B0 1010h**

Figure 14-2349. VTM_CFG2_MISC_CTRL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MAXT_OUTRG_ALERT_THR0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MAXT_OUTRG_ALERT_THR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MAXT_OUTRG_ALERT_THR</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MAXT_OUTRG_ALERT_THR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7078. VTM_CFG2_MISC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	MAXT_OUTRG_ALERT_THR0	R/W	0h	This defines the global max temperature out of range safe sample value. If the alert is enabled globally and for the sensor and the sensor reads a value <= this value then the alert is cleared after being triggered. This safe threshold defines at what temp the alert can be cleared. Reset is at POR only. Reset Source: mod_por_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	MAXT_OUTRG_ALERT_THR	R/W	0h	This defines the global max temperature out of range sample value. If the alert is enabled globally and for the sensor and the sensor reads a value >= this value then the alert is triggered. Reset is at POR only. Reset Source: mod_por_rst_n

14.2.2.1.2.27 VTM_CFG2_SAMPLE_CTRL Register

1 VTM_CFG2_SAMPLE_CTRL Register (Offset = 20h) [reset = 0h]

VTM sample related control MMR. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary. The e-fuse value is sampled from input port efuse_sample_clk_cnt. The sample_clk_cnt field is Device specific.

Return to Summary Table

Table 14-7079. Instance Table

Instance Name	Physical Address
VTM0	**00B0 1020h**

Figure 14-2350. VTM_CFG2_SAMPLE_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SAMPLE_PER_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
SAMPLE_PER_CNT							
R/W							
0h							

Table 14-7081. VTM_CFG2_SAMPLE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SAMPLE_PER_CNT	R/W	0h	Temperature sensor sample period count selector. Device specific. Default set by e-fuse or tie-off. This defines the sample period or number of sensor clocks between consecutive samples of the sensor allowed, from the start of the previous sample request to the start of the next sample request. After the sample is received the sensor status MMR fields will not be updated and the sensor will remain disabled. Reset value is from e-fuse at POR, efuse_sample_per_cnt. Reset Source: mod_por_rst_n

14.2.2.1.2.28 VTM_CFG2_TMPSENS_CTRL_j Register

1 VTM_CFG2_TMPSENS_CTRL_j Register (Offset = 0h + formula) [reset = 40h]

Temperature Sensor Band-gap control register for sensor j.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 7d

Table 14-7082. Instance Table

Instance Name	Physical Address
VTM0	**00B0 1000h + formula**

Figure 14-2351. VTM_CFG2_TMPSENS_CTRL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td>MAXT_OUTRG_EN</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="4">NONE</td><td>R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>CLRZ</td><td>SOC</td><td>CONT</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7084. VTM_CFG2_TMPSENS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	MAXT_OUTRG_EN	R/W	0h	Enable out-of-range event. This bit enables generation of the alert in case the given temperature sensors generates a temp code above a programmed max. 0 = Don't generate alert. 1 = Generate alert. Reset value is POR only. Reset Source: mod_por_rst_n
10:7	RESERVED	NONE	0h	Reserved
6	CLRZ	R/W	1h	Temp-Monitor control: 0 = Reset all Temp-monitor digital outputs. 1 = Allow operation of sensor. Reset value is POR only. Reset Source: mod_por_rst_n
5	SOC	R/W	0h	Temp-Monitor control: ADC Start of Conversion. A transition from 0 to 1 starts a new ADC conversion cycle. The bit with automatically clear when the conversion has completed. This mode is not valid when already in continuous mode. Reset value is POR only. Reset Source: mod_por_rst_n

Table 14-7084. VTM_CFG2_TMPSENS_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CONT	R/W	0h	Temp-Monitor control: ADC Continuous mode. Setting this mode enables the VTM to continuously monitor the sensor automatically. Each sample period the sensor will be accessed and the results captured. Reset value is POR only. Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.2.1.2.29 VTM_CFG2_TMPSENS_TRIM_j Register

1 VTM_CFG2_TMPSENS_TRIM_j Register (Offset = 4h + formula) [reset = 0h]

Temperature Sensor Band-gap trim values register for sensor j. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

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Offset = (j * 20h); where j = 0 to 7d

Table 14-7085. Instance Table

Instance Name	Physical Address
VTM0	**00B0 1004h + formula**

Figure 14-2352. VTM_CFG2_TMPSENS_TRIM_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TRIMO					
NONE		R/W					
0h		X					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TRIMG				
NONE			R/W				
0h			X				

Table 14-7087. VTM_CFG2_TMPSENS_TRIM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	TRIMO	R/W	X	Trim offset bits in the temp sensor. Reset value is from e-fuse at POR, efuse_tmpsens[j]_trimo. Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TRIMG	R/W	X	Trim gain bits in the temp sensor. Reset value is from e-fuse at POR, efuse_tmpsens[j]_trimg. Reset Source: mod_por_rst_n

14.2.2.1.2.30 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-7088. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2000h**

Figure 14-2353. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
5h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-7090. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.2.2.1.2.31 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-7091. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2008h**

Figure 14-2354. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-7093. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.2.2.1.2.32 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

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Table 14-7094. Instance Table

Instance Name	Physical Address
VTM0	**00B0 200Ch**

Figure 14-2355. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					4h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
4h							

Table 14-7096. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.2.2.1.2.33 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-7097. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2010h + formula**

Figure 14-2356. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-7099. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.2.2.1.2.34 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-7100. Instance Table

Instance Name	Physical Address
VTM0	**00B0 203Ch**

Figure 14-2357. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7102. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.2.2.1.2.35 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7103. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2040h**

Figure 14-2358. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	ECCAGG_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7105. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend

14.2.2.1.2.36 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7106. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2080h**

Figure 14-2359. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	ECCAGG_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7108. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend

Table 14-7108. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend

14.2.2.1.2.37 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7109. Instance Table

Instance Name	Physical Address
VTM0	**00B0 20C0h**

Figure 14-2360. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-7111. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend

Table 14-7111. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend

14.2.2.1.2.38 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-7112. Instance Table

Instance Name	Physical Address
VTM0	**00B0 213Ch**

Figure 14-2361. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7114. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.2.2.1.2.39 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7115. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2140h**

Figure 14-2362. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	ECCAGG_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7117. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend

14.2.2.1.2.40 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7118. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2180h**

Figure 14-2363. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	ECCAGG_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7120. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend

Table 14-7120. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend

14.2.2.1.2.41 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7121. Instance Table

Instance Name	Physical Address
VTM0	**00B0 21C0h**

Figure 14-2364. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-7123. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend

Table 14-7123. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend

14.2.2.1.2.42 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 14-7124. Instance Table

Instance Name	**Physical Address**
VTM0	**00B0 2200h**

Figure 14-2365. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7126. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.2.2.1.2.43 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-7127. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2204h**

Figure 14-2366. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7129. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.2.2.1.2.44 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-7130. Instance Table

Instance Name	Physical Address
VTM0	**00B0 2208h**

Figure 14-2367. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-7132. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.2.2.1.2.45 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-7133. Instance Table

Instance Name	Physical Address
VTM0	**00B0 220Ch**

Figure 14-2368. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-7135. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.2.2.2 PSC

PSC

14.2.2.2.1 PSC Summaries

PSC Summaries

Table 14-7136. PSC Registers, Base Address=0040 0000h, Length=4096

Offset	Length	Register Name	PSC0 Physical Address
0h	32	PSC_PID	0040 0000h
10h	32	PSC_GBLCTL	0040 0010h
14h	32	PSC_GBLSTAT	0040 0014h
18h	32	PSC_INTEVAL	0040 0018h
40h	32	PSC_MERRPR_J	0040 0040h + formula
50h	32	PSC_MERRCR_J	0040 0050h + formula
60h	32	PSC_PERRPR	0040 0060h
68h	32	PSC_PERRCR	0040 0068h
70h	32	PSC_EPCPR	0040 0070h
78h	32	PSC_EPCCR	0040 0078h
100h	32	PSC_RAILSTAT	0040 0100h
104h	32	PSC_RAILCTL	0040 0104h
108h	32	PSC_RAILSEL	0040 0108h
120h	32	PSC_PTCMD	0040 0120h
128h	32	PSC_PTSTAT	0040 0128h
200h	32	PSC_PDSTAT_J	0040 0200h + formula
300h	32	PSC_PDCTL_J	0040 0300h + formula
400h	32	PSC_PDCFG_J	0040 0400h + formula
600h	32	PSC_MDCFG_J	0040 0600h + formula
800h	32	PSC_MDSTAT_J	0040 0800h + formula
A00h	32	PSC_MDCTL_J	0040 0A00h + formula

14.2.2.2.2 PSC Registers

PSC Registers

14.2.2.2.2.1 PSC_PID Register

1 PSC_PID Register (Offset = 0h) [reset = 44820200h]

The peripheral identification register is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect) meaning that the values within this register should be hard-coded with the appropriate values and must not change from their hard-coded values.

Return to Summary Table

Table 14-7137. Instance Table

Instance Name	Physical Address
PSC0	**0040 0000h**

Figure 14-2369. PSC_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		0h		482h			
23	22	21	20	19	18	17	16
FUNC							
R							
482h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-7139. PSC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: chip_rst.chip_1_rst_n
29:28	BU	R	0h	Business Unit Reset Source: chip_rst.chip_1_rst_n
27:16	FUNC	R	482h	Module ID Reset Source: chip_rst.chip_1_rst_n
15:11	RTL	R	0h	RTL revision. Will vary depending on release Reset Source: chip_rst.chip_1_rst_n
10:8	MAJOR	R	2h	Major revision Reset Source: chip_rst.chip_1_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: chip_rst.chip_1_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.2 PSC_GBLCTL Register

1 PSC_GBLCTL Register (Offset = 10h) [reset = 0h]

This register contains global control to PSC.

Return to Summary Table

Table 14-7140. Instance Table

Instance Name	Physical Address
PSC0	**0040 0010h**

Figure 14-2370. PSC_GBLCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
IO_ANA_CTL							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7142. PSC_GBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	IO_ANA_CTL	R	0h	General purpose IO/Analog PowerDown control. Directly drives io_ana_pdctl_po[7:0] outputs. Reset Source: chip_rst.chip_1_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.2.2.3 PSC_GBLSTAT Register

1 PSC_GBLSTAT Register (Offset = 14h) [reset = 0h]

This register shows the PSC global status.

Return to Summary Table

Table 14-7143. Instance Table

Instance Name	Physical Address
PSC0	**0040 0014h**

Figure 14-2371. PSC_GBLSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED				EF_SMRFLEX			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
EF_SMRFLEX							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							OVRIDE
NONE							R
0h							0h

Table 14-7145. PSC_GBLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	EF_SMRFLEX	R	0h	Smart reflex class0 bits Reset Source: chip_rst.chip_1_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	OVRIDE	R	0h	PSC Override Status Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.4 PSC_INTEVAL Register

1 PSC_INTEVAL Register (Offset = 18h) [reset = 0h]

This register has no storage. Read from this register returns 0.

Return to Summary Table

Table 14-7146. Instance Table

Instance Name	Physical Address
PSC0	**0040 0018h**

Figure 14-2372. PSC_INTEVAL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td>GOSET</td><td>EPCSET</td><td>ERRSET</td><td>RESERVED</td></tr>
<tr><td colspan="4">NONE</td><td>W</td><td>W</td><td>W</td><td>NONE</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>EPCEV</td><td>ERREV</td><td>ALLEV</td></tr>
<tr><td colspan="5">NONE</td><td>W</td><td>W</td><td>W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7148. PSC_INTEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GOSET	W	0h	GOSTAT Interrupt Set Reset Source: chip_rst.chip_1_rst_n
18	EPCSET	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
17	ERRSET	W	0h	Combined Interrupt Set Reset Source: chip_rst.chip_1_rst_n
16:3	RESERVED	NONE	0h	Reserved
2	EPCEV	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
1	ERREV	W	0h	Re_evaluate Error Interrupt Reset Source: chip_rst.chip_1_rst_n
0	ALLEV	W	0h	Re_evaluate combined PSC interrupt Reset Source: chip_rst.chip_1_rst_n 0 Write of 0 has no effect 1 Re-evaluate the combined PSC interrupt PSC_ALLINT

14.2.2.2.2.5 PSC_MERRPR_j Register

1 PSC_MERRPR_j Register (Offset = 40h + formula) [reset = 0h]

This register records pending error conditions for all modules. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Offset = (j * 4h); where j = 0 to 1d

Table 14-7149. Instance Table

Instance Name	Physical Address
PSC0	**0040 0040h + formula**

Figure 14-2373. PSC_MERRPR_j Name Register

31	30	29	28	27	26	25	24
M							
R							
0h							
23	22	21	20	19	18	17	16
M							
R							
0h							
15	14	13	12	11	10	9	8
M							
R							
0h							
7	6	5	4	3	2	1	0
M							
R							
0h							

Table 14-7151. PSC_MERRPR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	R	0h	Records pending error conditions. Each bit n represents a module. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.6 PSC_MERRCR_j Register

1 PSC_MERRCR_j Register (Offset = 50h + formula) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Offset = (j * 4h); where j = 0 to 1d

Table 14-7152. Instance Table

Instance Name	Physical Address
PSC0	**0040 0050h + formula**

Figure 14-2374. PSC_MERRCR_j Name Register

31	30	29	28	27	26	25	24
M							
W1TC							
0h							
23	22	21	20	19	18	17	16
M							
W1TC							
0h							
15	14	13	12	11	10	9	8
M							
W1TC							
0h							
7	6	5	4	3	2	1	0
M							
W1TC							
0h							

Table 14-7154. PSC_MERRCR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	W1TC	0h	Write of 1 clears the corresponding MERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.7 PSC_PERRPR Register

1 PSC_PERRPR Register (Offset = 60h) [reset = 0h]

This register records pending error conditions for each power domain. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7155. Instance Table

Instance Name	Physical Address
PSC0	**0040 0060h**

Figure 14-2375. PSC_PERRPR Name Register

31	30	29	28	27	26	25	24
P							
R							
0h							
23	22	21	20	19	18	17	16
P							
R							
0h							
15	14	13	12	11	10	9	8
P							
R							
0h							
7	6	5	4	3	2	1	0
P							
R							
0h							

Table 14-7157. PSC_PERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R	0h	Power Domain n Error Condition. Each bit n represents a power domain. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.8 PSC_PERRCR Register

1 PSC_PERRCR Register (Offset = 68h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7158. Instance Table

Instance Name	Physical Address
PSC0	**0040 0068h**

Figure 14-2376. PSC_PERRCR Name Register

31	30	29	28	27	26	25	24
P							
W1TC							
0h							
23	22	21	20	19	18	17	16
P							
W1TC							
0h							
15	14	13	12	11	10	9	8
P							
W1TC							
0h							
7	6	5	4	3	2	1	0
P							
W1TC							
0h							

Table 14-7160. PSC_PERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	W1TC	0h	Write of 1 clears the corresponding PERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.9 PSC_EPCPR Register

1 PSC_EPCPR Register (Offset = 70h) [reset = 0h]

This register records pending external power control conditions. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7161. Instance Table

Instance Name	Physical Address
PSC0	**0040 0070h**

Figure 14-2377. PSC_EPCPR Name Register

31	30	29	28	27	26	25	24
EPC							
R							
0h							
23	22	21	20	19	18	17	16
EPC							
R							
0h							
15	14	13	12	11	10	9	8
EPC							
R							
0h							
7	6	5	4	3	2	1	0
EPC							
R							
0h							

Table 14-7163. PSC_EPCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	R	0h	External Power Control Intervention Request for Power Domain n Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.10 PSC_EPCCR Register

1 PSC_EPCCR Register (Offset = 78h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7164. Instance Table

Instance Name	Physical Address
PSC0	**0040 0078h**

Figure 14-2378. PSC_EPCCR Name Register

31	30	29	28	27	26	25	24
EPC							
W1TC							
0h							
23	22	21	20	19	18	17	16
EPC							
W1TC							
0h							
15	14	13	12	11	10	9	8
EPC							
W1TC							
0h							
7	6	5	4	3	2	1	0
EPC							
W1TC							
0h							

Table 14-7166. PSC_EPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	W1TC	0h	Write of 1 clears the corresponding EPCPR bit Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.11 PSC_RAILSTAT Register

1 PSC_RAILSTAT Register (Offset = 100h) [reset = 0h]

This register is a read-only and shows the current rail requestor whose request is being granted and the current value of the counter associated with this requestor.

Return to Summary Table

Table 14-7167. Instance Table

Instance Name	**Physical Address**
PSC0	**0040 0100h**

Figure 14-2379. PSC_RAILSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">RAILNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RAILCNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7169. PSC_RAILSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	RAILNUM	R	0h	Indicates Current Rail Requestor being processed by GPSC Reset Source: chip_rst.chip_1_rst_n
23:8	RESERVED	NONE	0h	Reserved
7:0	RAILCNT	R	0h	Indicates the current rail counter value Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.12 PSC_RAILCTL Register

1 PSC_RAILCTL Register (Offset = 104h) [reset = 0h]

This register is user programmable. It holds the counter values for rail counter. User can select one of the two counter values to be used for each power domain (see RAILSEL register).

Return to Summary Table

Table 14-7170. Instance Table

Instance Name	Physical Address
PSC0	**0040 0104h**

Figure 14-2380. PSC_RAILCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RAILCTR1							
R/W							
X							
7	6	5	4	3	2	1	0
RAILCTR0							
R/W							
X							

Table 14-7172. PSC_RAILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RAILCTR1	R/W	X	Rail Counter Value 1 Reset Source: chip_rst.chip_1_rst_n
7:0	RAILCTR0	R/W	X	Rail Counter Value 0 Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.13 PSC_RAILSEL Register

1 PSC_RAILSEL Register (Offset = 108h) [reset = 0h]

User can use this register to select the counter value (RAILCTL) for each power domain.

Return to Summary Table

Table 14-7173. Instance Table

Instance Name	Physical Address
PSC0	**0040 0108h**

Figure 14-2381. PSC_RAILSEL Name Register

31	30	29	28	27	26	25	24
P							
R/W							
X							
23	22	21	20	19	18	17	16
P							
R/W							
X							
15	14	13	12	11	10	9	8
P							
R/W							
X							
7	6	5	4	3	2	1	0
P							
R/W							
X							

Table 14-7175. PSC_RAILSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R/W	X	Rail Counter Select for Power Domain Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.14 PSC_PTCMD Register

1 PSC_PTCMD Register (Offset = 120h) [reset = 0h]

This is a pseudo-command register with no actual storage. Reads return 0. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7176. Instance Table

Instance Name	Physical Address
PSC0	**0040 0120h**

Figure 14-2382. PSC_PTCMD Name Register

31	30	29	28	27	26	25	24
GO							
W1TS							
0h							
23	22	21	20	19	18	17	16
GO							
W1TS							
0h							
15	14	13	12	11	10	9	8
GO							
W1TS							
0h							
7	6	5	4	3	2	1	0
GO							
W1TS							
0h							

Table 14-7178. PSC_PTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GO	W1TS	0h	Power Domain n GO Transition Reset Source: chip_rst.chip_1_rst_n 0 `Write of 0 has no effect` 1 `Sets corresponding PTSTAT.GOSTAT field which causes PSC hardware to evaluate PDCTL.NEXT and MDCTL.NEXT for this domain.`

14.2.2.2.2.15 PSC_PTSTAT Register

1 PSC_PTSTAT Register (Offset = 128h) [reset = 0h]

This is a status register. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7179. Instance Table

Instance Name	Physical Address
PSC0	**0040 0128h**

Figure 14-2383. PSC_PTSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GOSTAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GOSTAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GOSTAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GOSTAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7181. PSC_PTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description

31:0	GOSTAT	R	0h	Power Domain n Transition Command Status
				Reset Source: chip_rst.chip_1_rst_n
				`0` `No transitions in progress in Power Domain`
				`1` `Power Domain Transition in progress. Either the power domain is transitioning, or modules on this domain are transitioning.`

14.2.2.2.2.16 PSC_PDSTAT_j Register

1 PSC_PDSTAT_j Register (Offset = 200h + formula) [reset = 0h]

This is a status register. One register per power domain. Each register contains the status for the given power domain.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 11d

Table 14-7182. Instance Table

Instance Name	Physical Address
PSC0	**0040 0200h + formula**

Figure 14-2384. PSC_PDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				EMUIHB	PWRBAD	PORDONE	PORZ
NONE				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			STATE				
NONE			R				
0h			0h				

Table 14-7184. PSC_PDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	EMUIHB	R	0h	Emulation Alters Domain State Reset Source: chip_rst.chip_1_rst_n
10	PWRBAD	R	0h	Power Bad error Reset Source: chip_rst.chip_1_rst_n
9	PORDONE	R	0h	POR Done Input Status Reset Source: chip_rst.chip_1_rst_n
8	PORZ	R	0h	PORz output actual status Reset Source: chip_rst.chip_1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	STATE	R	0h	Current Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 Power domain is off 1 Power domain is on

14.2.2.2.2.17 PSC_PDCTL_j Register

1 PSC_PDCTL_j Register (Offset = 300h + formula) [reset = 0h]

This is a control register. One register per power domain.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 11d

Table 14-7185. Instance Table

Instance Name	Physical Address
PSC0	**0040 0300h + formula**

Figure 14-2385. PSC_PDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED	PWRSW	ISO	RESERVED			
R/W	NONE	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
WAKECNT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED	PDMODE			RESERVED		EMUIHBIE	EPCGOOD
NONE	R/W			NONE		R/W	R/W
0h	0h			0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED							NEXT
NONE							R/W
0h							0h

Table 14-7187. PSC_PDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit Reset Source: chip_rst.chip_1_rst_n
30	RESERVED	NONE	0h	Reserved
29	PWRSW	R/W	0h	Power shorting Switch Control Reset Source: chip_rst.chip_1_rst_n
28	ISO	R/W	0h	Isolation Cell control Reset Source: chip_rst.chip_1_rst_n
27:24	RESERVED	NONE	0h	Reserved
23:16	WAKECNT	R/W	0h	RAM wake count delay value Reset Source: chip_rst.chip_1_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-7187. PSC_PDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	PDMODE	R/W	0h	Power Down mode Reset Source: chip_rst.chip_1_rst_n 0 `Core Off, RAM Array Off, RAM Periphery Off` 8 `Core Retention, RAM Array Off, RAM Periphery Off` 9 `Core Retention, RAM Array Retention, RAM Periphery Off` 10 `Core On, RAM Array Retention, RAM Periphery Off` 11 `Core On, RAM Array Retention, RAM Periphery On` 15 `Core On, RAM Array On, RAM Periphery On`
11:10	RESERVED	NONE	0h	Reserved
9	EMUIHBIE	R/W	0h	Emulation alters domain state Reset Source: chip_rst.chip_1_rst_n 0 `Not enabled` 1 `Interrupt enabled`
8	EPCGOOD	R/W	0h	External Power Control Power Good Indication Reset Source: chip_rst.chip_1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	NEXT	R/W	0h	User_Desired Next Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 `Off` 1 `On`

14.2.2.2.2.18 PSC_PDCFG_j Register

1 PSC_PDCFG_j Register (Offset = 400h + formula) [reset = 0h]

This is a status register. It shows PSC settings for easy debug.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 11d

Table 14-7188. Instance Table

Instance Name	Physical Address
PSC0	**0040 0400h + formula**

Figure 14-2386. PSC_PDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ICEPICK	RESERVED	MEMSLPKWK	ALWAYSON
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-7190. PSC_PDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

3	ICEPICK	R	0h	Icepick support
				Reset Source: chip_rst.chip_1_rst_n
				`0 This domain does not have IcePick support`
				`1 This domain has IcePick support because one or more of its LPSCs have IcePick support`

2	RESERVED	NONE	0h	Reserved
1	MEMSLPKWK	R	0h	Memory sleep-wake domain Reset Source: chip_rst.chip_1_rst_n

0	ALWAYSON	R	0h	Always on power domain
				Reset Source: chip_rst.chip_1_rst_n
				`0 This domain is not an AlwaysON power domain`
				`1 This domain is an AlwaysON power domain`

14.2.2.2.2.19 PSC_MDCFG_j Register

1 PSC_MDCFG_j Register (Offset = 600h + formula) [reset = 0h]

This is a constant register showing some PSC settings for easy debug. This register is read only.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 35d

Table 14-7191. Instance Table

Instance Name	Physical Address
PSC0	**0040 0600h + formula**

Figure 14-2387. PSC_MDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PWRDOM				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
AUTOONLY	RESETISO	NEXTLOCK	ASYNC	ICEPICK	PERMDIS	PLLHANDSHAKE	NUMSCRDISBALE
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NUMSCRDISBALE		NUMCLKEN			NUMCLK		
R		R			R		
0h		0h			0h		

Table 14-7193. PSC_MDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PWRDOM	R	0h	Indicates which power domain this module belongs to Reset Source: chip_rst.chip_1_rst_n
15	AUTOONLY	R	0h	0: This LPSC supports all modes, 1: This LPSC supports Enable, AutoSleep or AutoWake only Reset Source: chip_rst.chip_1_rst_n
14	RESETISO	R	0h	0: This LPSC does not support Reset Isolation, 1: This LPSC supports Reset Isolation Reset Source: chip_rst.chip_1_rst_n
13	NEXTLOCK	R	0h	0: MDCTL.NEXT field is writable, 1: MDCTL.NEXT field is locked Reset Source: chip_rst.chip_1_rst_n
12	ASYNC	R	0h	Async Lpsc Reset Source: chip_rst.chip_1_rst_n
11	ICEPICK	R	0h	IcePick support Reset Source: chip_rst.chip_1_rst_n

Table 14-7193. PSC_MDCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PERMDIS	R	0h	Permanently disable Reset Source: chip_rst.chip_1_rst_n
9	PLLHANDSHAKE	R	0h	RTL parameter PLL_HANDSHAKE Reset Source: chip_rst.chip_1_rst_n
8:6	NUMSCRDISBALE	R	0h	Number of PWR_SCR_DISABLE interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
5:3	NUMCLKEN	R	0h	Number of PWR_CLK_EN interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
2:0	NUMCLK	R	0h	Number of PWR_CLKSTOP interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.20 PSC_MDSTAT_j Register

1 PSC_MDSTAT_j Register (Offset = 800h + formula) [reset = 0h]

This register shows the status of each module. Requires one register per module on the device.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 35d

Table 14-7194. Instance Table

Instance Name	Physical Address
PSC0	**0040 0800h + formula**

Figure 14-2388. PSC_MDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EMUIHB	EMURST
NONE						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED			MCKOUT	MRSTDONE	MRSTZ	LRSTDONE	LRSTZ
NONE			R	R	R	R	R
0h			0h	X	X	X	X
7	6	5	4	3	2	1	0
RESERVED		STATE					
NONE		R					
0h		X					

Table 14-7196. PSC_MDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EMUIHB	R	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. Reset Source: chip_rst.chip_1_rst_n 0 No emulation altering user-desired module state 1 Emulation alters user-desired module state
16	EMURST	R	0h	Emulation Alters Reset Reset Source: chip_rst.chip_1_rst_n 0 No emulation altering user-desired reset 1 Emulation has altered module reset to be different from what user desires
15:13	RESERVED	NONE	0h	Reserved
12	MCKOUT	R	0h	Actual modclk output to module Reset Source: chip_rst.chip_1_rst_n 0 modclk gated 1 modclk on

Table 14-7196. PSC_MDSTAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MRSTDONE	R	X	Module reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 module reset initialization not done 1 module reset initialization done
10	MRSTZ	R	X	Module reset actual status Reset Source: chip_rst.chip_1_rst_n 0 module reset modrst_po* asserted 1 module reset modrst_po* de-asserted
9	LRSTDONE	R	X	Module local reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 local reset initialization not done 1 local reset initialization done
8	LRSTZ	R	X	Module local reset actual status Reset Source: chip_rst.chip_1_rst_n 0 local reset mod_lrst_po* asserted 1 local reset mod_lrst_po* de-asserted
7:6	RESERVED	NONE	0h	Reserved
5:0	STATE	R	X	These bits indicate the current module state Values 0x0 - 0x5 = Key States Values 0x21 - 0x2B = Transitional States Other Values = Reserved Reset Source: chip_rst.chip_1_rst_n 0 SwRstDisable 1 SyncRst 2 Disable 3 Enable 4 AutoSleep 5 AutoWake 33 Disable Clk On 34 Disable In-Prog (waiting for clkstop_ack = 1) 35 Retry Disable (new vbus_req, retry--give clkstop_req = 1 again) 36 Enable In-Prog 37 Sleep In-Prog 38 ClockOn (from SwRstDisable to SyncRst) 39 ClockOff (from SyncRst to SwRstDisable) 40 ClockOn (from Disable to DisableClkOn) 41 ClockOff (from DisableClkOn to Disable) 42 ClockOn (from AutoSleep/Wake to Sleep In-Prog) 43 ClockOff (from DisableClkOn or Sleep In-Prog to AutoSleep/Wake) OTHER Reserved

14.2.2.2.2.21 PSC_MDCTL_j Register

1 PSC_MDCTL_j Register (Offset = A00h + formula) [reset = 0h]

This register provides specific control for the individual module. One register per module on the device.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 35d

Table 14-7197. Instance Table

Instance Name	Physical Address
PSC0	**0040 0A00h + formula**

Figure 14-2389. PSC_MDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED						
R/W	NONE						
X	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			RESETISO	BLKCHIP1RST	EMUIHBIE	EMURSTIE	LRSTZ
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			NEXT				
NONE			R/W				
0h			0h				

Table 14-7199. PSC_MDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	X	Force Bit Reset Source: chip_rst.chip_1_rst_n 0 `No force` 1 `Force`
30:13	RESERVED	NONE	0h	Reserved
12	RESETISO	R/W	0h	Reset Isolation Reset Source: chip_rst.chip_1_rst_n 0 `No reset isolation` 1 `Enable reset isolation`
11	BLKCHIP1RST	R/W	0h	Block Chip_1_Reset Reset Source: chip_rst.chip_1_rst_n
10	EMUIHBIE	R/W	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. Reset Source: chip_rst.chip_1_rst_n 0 `Not enabled` 1 `Interrupt enabled`

Table 14-7199. PSC_MDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EMURSTIE	R/W	0h	Emulation Alter Reset Interrupt Enable Reset Source: chip_rst.chip_1_rst_n 0 Not enabled 1 Interrupt enabled
8	LRSTZ	R/W	0h	Module local reset control Reset Source: chip_rst.chip_1_rst_n 0 assert local reset 1 de-assert local reset
7:5	RESERVED	NONE	0h	Reserved
4:0	NEXT	R/W	0h	Module Next State Only key states can be selected in this field. If a Reserved value is programmed into MDCTL.NEXT, hardware will internally force the state to SwRstDisable. If MDCFG.PERMDIS = 1, the module must remain in SwRstDisable after hardware places it in SwRstDisable state. The user is allowed to write this field but hardware ignores this field and always passes along MDCTL.NEXT = SwRstDisable. Reset Source: chip_rst.chip_1_rst_n 0 SwRstDisable 1 SyncRst 2 Disable 3 Enable 4 AutoSleep 5 AutoWake OTHER Reserved

14.2.2.3 PSC

PSC

14.2.2.3.1 PSC Summaries

PSC Summaries

Table 14-7200. PSC Registers, Base Address=0400 0000h, Length=4096

Offset	Length	Register Name	MCU_PSC0 Physical Address
0h	32	PSC_PID	0400 0000h
10h	32	PSC_GBLCTL	0400 0010h
14h	32	PSC_GBLSTAT	0400 0014h
18h	32	PSC_INTEVAL	0400 0018h
40h	32	PSC_MERRPR	0400 0040h
50h	32	PSC_MERRCR	0400 0050h
60h	32	PSC_PERRPR	0400 0060h
68h	32	PSC_PERRCR	0400 0068h
70h	32	PSC_EPCPR	0400 0070h
78h	32	PSC_EPCCR	0400 0078h
100h	32	PSC_RAILSTAT	0400 0100h
104h	32	PSC_RAILCTL	0400 0104h
108h	32	PSC_RAILSEL	0400 0108h
120h	32	PSC_PTCMD	0400 0120h
128h	32	PSC_PTSTAT	0400 0128h
200h	32	PSC_PDSTAT_J	0400 0200h + formula
300h	32	PSC_PDCTL_J	0400 0300h + formula
400h	32	PSC_PDCFG_J	0400 0400h + formula
600h	32	PSC_MDCFG_J	0400 0600h + formula
800h	32	PSC_MDSTAT_J	0400 0800h + formula
A00h	32	PSC_MDCTL_J	0400 0A00h + formula

14.2.2.3.2 PSC Registers

PSC Registers

14.2.2.3.2.1 PSC_PID Register

1 PSC_PID Register (Offset = 0h) [reset = 44820200h]

The peripheral identification register is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect) meaning that the values within this register should be hard-coded with the appropriate values and must not change from their hard-coded values.

Return to Summary Table

Table 14-7201. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0000h**

Figure 14-2390. PSC_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		0h		482h			
23	22	21	20	19	18	17	16
FUNC							
R							
482h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-7203. PSC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: chip_rst.chip_1_rst_n
29:28	BU	R	0h	Business Unit Reset Source: chip_rst.chip_1_rst_n
27:16	FUNC	R	482h	Module ID Reset Source: chip_rst.chip_1_rst_n
15:11	RTL	R	0h	RTL revision. Will vary depending on release Reset Source: chip_rst.chip_1_rst_n
10:8	MAJOR	R	2h	Major revision Reset Source: chip_rst.chip_1_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: chip_rst.chip_1_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.2 PSC_GBLCTL Register

1 PSC_GBLCTL Register (Offset = 10h) [reset = 0h]

This register contains global control to PSC.

Return to Summary Table

Table 14-7204. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0010h**

Figure 14-2391. PSC_GBLCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IO_ANA_CTL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7206. PSC_GBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	IO_ANA_CTL	R	0h	General purpose IO/Analog PowerDown control. Directly drives io_ana_pdctl_po[7:0] outputs. Reset Source: chip_rst.chip_1_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.3.2.3 PSC_GBLSTAT Register

1 PSC_GBLSTAT Register (Offset = 14h) [reset = 0h]

This register shows the PSC global status.

Return to Summary Table

Table 14-7207. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0014h**

Figure 14-2392. PSC_GBLSTAT Name Register

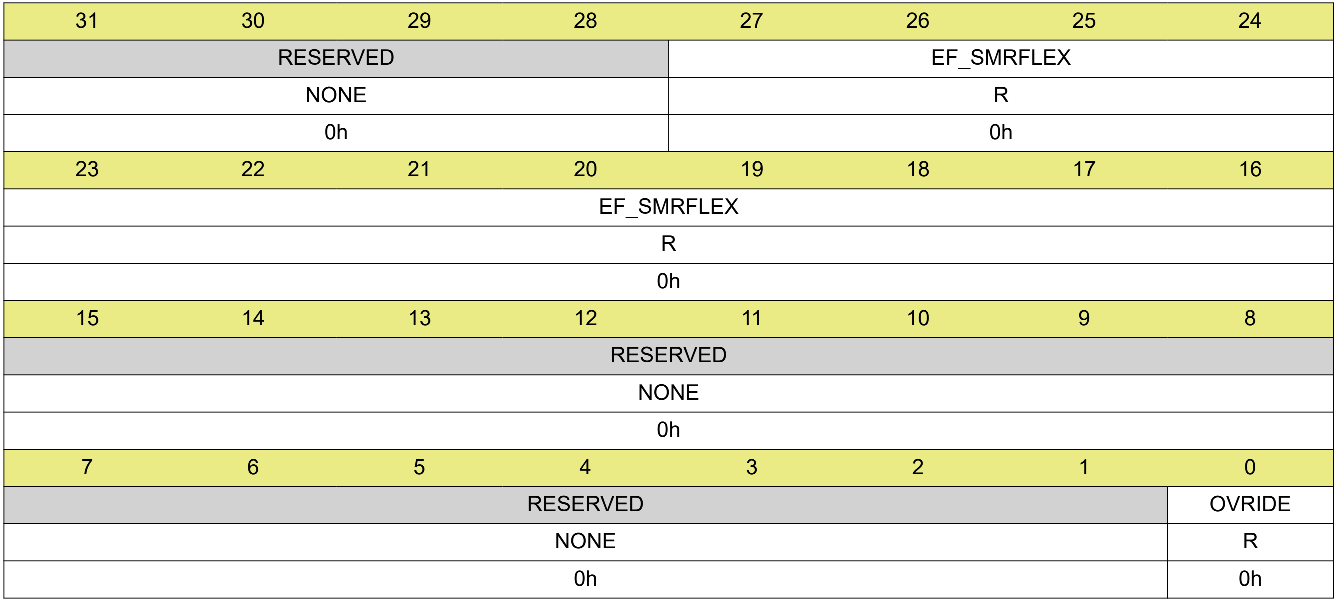

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">EF_SMRFLEX</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">EF_SMRFLEX</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>OVRIDE</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7209. PSC_GBLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	EF_SMRFLEX	R	0h	Smart reflex class0 bits Reset Source: chip_rst.chip_1_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	OVRIDE	R	0h	PSC Override Status Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.4 PSC_INTEVAL Register

1 PSC_INTEVAL Register (Offset = 18h) [reset = 0h]

This register has no storage. Read from this register returns 0.

Return to Summary Table

Table 14-7210. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0018h**

Figure 14-2393. PSC_INTEVAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				GOSET	EPCSET	ERRSET	RESERVED
NONE				W	W	W	NONE
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPCEV	ERREV	ALLEV
NONE					W	W	W
0h					0h	0h	0h

Table 14-7212. PSC_INTEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GOSET	W	0h	GOSTAT Interrupt Set Reset Source: chip_rst.chip_1_rst_n
18	EPCSET	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
17	ERRSET	W	0h	Combined Interrupt Set Reset Source: chip_rst.chip_1_rst_n
16:3	RESERVED	NONE	0h	Reserved
2	EPCEV	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
1	ERREV	W	0h	Re_evaluate Error Interrupt Reset Source: chip_rst.chip_1_rst_n
0	ALLEV	W	0h	Re_evaluate combined PSC interrupt Reset Source: chip_rst.chip_1_rst_n 0 Write of 0 has no effect 1 Re-evaluate the combined PSC interrupt PSC_ALLINT

14.2.2.3.2.5 PSC_MERRPR Register

1 PSC_MERRPR Register (Offset = 40h) [reset = 0h]

This register records pending error conditions for all modules. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Table 14-7213. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0040h**

Figure 14-2394. PSC_MERRPR Name Register

31	30	29	28	27	26	25	24
M							
R							
0h							
23	22	21	20	19	18	17	16
M							
R							
0h							
15	14	13	12	11	10	9	8
M							
R							
0h							
7	6	5	4	3	2	1	0
M							
R							
0h							

Table 14-7215. PSC_MERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	R	0h	Records pending error conditions. Each bit n represents a module. Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.6 PSC_MERRCR Register

1 PSC_MERRCR Register (Offset = 50h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Table 14-7216. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0050h**

Figure 14-2395. PSC_MERRCR Name Register

31	30	29	28	27	26	25	24
M							
W1TC							
0h							
23	22	21	20	19	18	17	16
M							
W1TC							
0h							
15	14	13	12	11	10	9	8
M							
W1TC							
0h							
7	6	5	4	3	2	1	0
M							
W1TC							
0h							

Table 14-7218. PSC_MERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	W1TC	0h	Write of 1 clears the corresponding MERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.7 PSC_PERRPR Register

1 PSC_PERRPR Register (Offset = 60h) [reset = 0h]

This register records pending error conditions for each power domain. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7219. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0060h**

Figure 14-2396. PSC_PERRPR Name Register

31	30	29	28	27	26	25	24
P							
R							
0h							
23	22	21	20	19	18	17	16
P							
R							
0h							
15	14	13	12	11	10	9	8
P							
R							
0h							
7	6	5	4	3	2	1	0
P							
R							
0h							

Table 14-7221. PSC_PERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R	0h	Power Domain n Error Condition. Each bit n represents a power domain. Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.8 PSC_PERRCR Register

1 PSC_PERRCR Register (Offset = 68h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7222. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0068h**

Figure 14-2397. PSC_PERRCR Name Register

31	30	29	28	27	26	25	24
P							
W1TC							
0h							
23	22	21	20	19	18	17	16
P							
W1TC							
0h							
15	14	13	12	11	10	9	8
P							
W1TC							
0h							
7	6	5	4	3	2	1	0
P							
W1TC							
0h							

Table 14-7224. PSC_PERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	W1TC	0h	Write of 1 clears the corresponding PERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.9 PSC_EPCPR Register

1 PSC_EPCPR Register (Offset = 70h) [reset = 0h]

This register records pending external power control conditions. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7225. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0070h**

Figure 14-2398. PSC_EPCPR Name Register

31	30	29	28	27	26	25	24
EPC							
R							
0h							
23	22	21	20	19	18	17	16
EPC							
R							
0h							
15	14	13	12	11	10	9	8
EPC							
R							
0h							
7	6	5	4	3	2	1	0
EPC							
R							
0h							

Table 14-7227. PSC_EPCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	R	0h	External Power Control Intervention Request for Power Domain n Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.10 PSC_EPCCR Register

1 PSC_EPCCR Register (Offset = 78h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7228. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0078h**

Figure 14-2399. PSC_EPCCR Name Register

31	30	29	28	27	26	25	24
EPC							
W1TC							
0h							
23	22	21	20	19	18	17	16
EPC							
W1TC							
0h							
15	14	13	12	11	10	9	8
EPC							
W1TC							
0h							
7	6	5	4	3	2	1	0
EPC							
W1TC							
0h							

Table 14-7230. PSC_EPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	W1TC	0h	Write of 1 clears the corresponding EPCPR bit Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.11 PSC_RAILSTAT Register

1 PSC_RAILSTAT Register (Offset = 100h) [reset = 0h]

This register is a read-only and shows the current rail requestor whose request is being granted and the current value of the counter associated with this requestor.

Return to Summary Table

Table 14-7231. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0100h**

Figure 14-2400. PSC_RAILSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED			RAILNUM				
NONE			R				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAILCNT							
R							
0h							

Table 14-7233. PSC_RAILSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	RAILNUM	R	0h	Indicates Current Rail Requestor being processed by GPSC Reset Source: chip_rst.chip_1_rst_n
23:8	RESERVED	NONE	0h	Reserved
7:0	RAILCNT	R	0h	Indicates the current rail counter value Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.12 PSC_RAILCTL Register

1 PSC_RAILCTL Register (Offset = 104h) [reset = 0h]

This register is user programmable. It holds the counter values for rail counter. User can select one of the two counter values to be used for each power domain (see RAILSEL register).

Return to Summary Table

Table 14-7234. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0104h**

Figure 14-2401. PSC_RAILCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RAILCTR1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RAILCTR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-7236. PSC_RAILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RAILCTR1	R/W	X	Rail Counter Value 1 Reset Source: chip_rst.chip_1_rst_n
7:0	RAILCTR0	R/W	X	Rail Counter Value 0 Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.13 PSC_RAILSEL Register

1 PSC_RAILSEL Register (Offset = 108h) [reset = 0h]

User can use this register to select the counter value (RAILCTL) for each power domain.

Return to Summary Table

Table 14-7237. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0108h**

Figure 14-2402. PSC_RAILSEL Name Register

31	30	29	28	27	26	25	24
P							
R/W							
X							
23	22	21	20	19	18	17	16
P							
R/W							
X							
15	14	13	12	11	10	9	8
P							
R/W							
X							
7	6	5	4	3	2	1	0
P							
R/W							
X							

Table 14-7239. PSC_RAILSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R/W	X	Rail Counter Select for Power Domain Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.14 PSC_PTCMD Register

1 PSC_PTCMD Register (Offset = 120h) [reset = 0h]

This is a pseudo-command register with no actual storage. Reads return 0. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7240. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0120h**

Figure 14-2403. PSC_PTCMD Name Register

31	30	29	28	27	26	25	24
GO							
W1TS							
0h							
23	22	21	20	19	18	17	16
GO							
W1TS							
0h							
15	14	13	12	11	10	9	8
GO							
W1TS							
0h							
7	6	5	4	3	2	1	0
GO							
W1TS							
0h							

Table 14-7242. PSC_PTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GO	W1TS	0h	Power Domain n GO Transition Reset Source: chip_rst.chip_1_rst_n 0 `Write of 0 has no effect` 1 `Sets corresponding PTSTAT.GOSTAT field which causes PSC hardware to evaluate PDCTL.NEXT and MDCTL.NEXT for this domain.`

14.2.2.3.2.15 PSC_PTSTAT Register

1 PSC_PTSTAT Register (Offset = 128h) [reset = 0h]

This is a status register. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7243. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0128h**

Figure 14-2404. PSC_PTSTAT Name Register

31	30	29	28	27	26	25	24
GOSTAT							
R							
0h							
23	22	21	20	19	18	17	16
GOSTAT							
R							
0h							
15	14	13	12	11	10	9	8
GOSTAT							
R							
0h							
7	6	5	4	3	2	1	0
GOSTAT							
R							
0h							

Table 14-7245. PSC_PTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GOSTAT	R	0h	Power Domain n Transition Command Status Reset Source: chip_rst.chip_1_rst_n 0 No transitions in progress in Power Domain 1 Power Domain Transition in progress. Either the power domain is transitioning, or modules on this domain are transitioning.

14.2.2.3.2.16 PSC_PDSTAT_j Register

1 PSC_PDSTAT_j Register (Offset = 200h + formula) [reset = 0h]

This is a status register. One register per power domain. Each register contains the status for the given power domain.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 1d

Table 14-7246. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0200h + formula**

Figure 14-2405. PSC_PDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				EMUIHB	PWRBAD	PORDONE	PORZ
NONE				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			STATE				
NONE			R				
0h			0h				

Table 14-7248. PSC_PDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	EMUIHB	R	0h	Emulation Alters Domain State Reset Source: chip_rst.chip_1_rst_n
10	PWRBAD	R	0h	Power Bad error Reset Source: chip_rst.chip_1_rst_n
9	PORDONE	R	0h	POR Done Input Status Reset Source: chip_rst.chip_1_rst_n
8	PORZ	R	0h	PORz output actual status Reset Source: chip_rst.chip_1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	STATE	R	0h	Current Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 Power domain is off 1 Power domain is on

14.2.2.3.2.17 PSC_PDCTL_j Register

1 PSC_PDCTL_j Register (Offset = 300h + formula) [reset = 0h]

This is a control register. One register per power domain.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 1d

Table 14-7249. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0300h + formula**

Figure 14-2406. PSC_PDCTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>FORCE</td><td>RESERVED</td><td>PWRSW</td><td>ISO</td><td colspan="4">RESERVED</td></tr>
<tr><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">WAKECNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">PDMODE</td><td colspan="2">RESERVED</td><td>EMUIHBIE</td><td>EPCGOOD</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>NEXT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7251. PSC_PDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit Reset Source: chip_rst.chip_1_rst_n
30	RESERVED	NONE	0h	Reserved
29	PWRSW	R/W	0h	Power shorting Switch Control Reset Source: chip_rst.chip_1_rst_n
28	ISO	R/W	0h	Isolation Cell control Reset Source: chip_rst.chip_1_rst_n
27:24	RESERVED	NONE	0h	Reserved
23:16	WAKECNT	R/W	0h	RAM wake count delay value Reset Source: chip_rst.chip_1_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-7251. PSC_PDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	PDMODE	R/W	0h	Power Down mode Reset Source: chip_rst.chip_1_rst_n 0 Core Off, RAM Array Off, RAM Periphery Off 8 Core Retention, RAM Array Off, RAM Periphery Off 9 Core Retention, RAM Array Retention, RAM Periphery Off 10 Core On, RAM Array Retention, RAM Periphery Off 11 Core On, RAM Array Retention, RAM Periphery On 15 Core On, RAM Array On, RAM Periphery On
11:10	RESERVED	NONE	0h	Reserved
9	EMUIHBIE	R/W	0h	Emulation alters domain state Reset Source: chip_rst.chip_1_rst_n 0 Not enabled 1 Interrupt enabled
8	EPCGOOD	R/W	0h	External Power Control Power Good Indication Reset Source: chip_rst.chip_1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	NEXT	R/W	0h	User_Desired Next Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 Off 1 On

14.2.2.3.2.18 PSC_PDCFG_j Register

1 PSC_PDCFG_j Register (Offset = 400h + formula) [reset = 0h]

This is a status register. It shows PSC settings for easy debug.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 1d

Table 14-7252. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0400h + formula**

Figure 14-2407. PSC_PDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ICEPICK	RESERVED	MEMSLPKWK	ALWAYSON
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-7254. PSC_PDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

3	ICEPICK	R	0h	Icepick support
				Reset Source: chip_rst.chip_1_rst_n
				`0 This domain does not have IcePick support`
				`1 This domain has IcePick support because one or more of its LPSCs have IcePick support`

2	RESERVED	NONE	0h	Reserved
1	MEMSLPKWK	R	0h	Memory sleep-wake domain Reset Source: chip_rst.chip_1_rst_n

0	ALWAYSON	R	0h	Always on power domain
				Reset Source: chip_rst.chip_1_rst_n
				`0 This domain is not an AlwaysON power domain`
				`1 This domain is an AlwaysON power domain`

14.2.2.3.2.19 PSC_MDCFG_j Register

1 PSC_MDCFG_j Register (Offset = 600h + formula) [reset = 0h]

This is a constant register showing some PSC settings for easy debug. This register is read only.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 7d

Table 14-7255. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0600h + formula**

Figure 14-2408. PSC_MDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PWRDOM				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
AUTOONLY	RESETISO	NEXTLOCK	ASYNC	ICEPICK	PERMDIS	PLLHANDSHAKE	NUMSCRDISBALE
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NUMSCRDISBALE		NUMCLKEN			NUMCLK		
R		R			R		
0h		0h			0h		

Table 14-7257. PSC_MDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PWRDOM	R	0h	Indicates which power domain this module belongs to Reset Source: chip_rst.chip_1_rst_n
15	AUTOONLY	R	0h	0: This LPSC supports all modes, 1: This LPSC supports Enable, AutoSleep or AutoWake only Reset Source: chip_rst.chip_1_rst_n
14	RESETISO	R	0h	0: This LPSC does not support Reset Isolation, 1: This LPSC supports Reset Isolation Reset Source: chip_rst.chip_1_rst_n
13	NEXTLOCK	R	0h	0: MDCTL.NEXT field is writable, 1: MDCTL.NEXT field is locked Reset Source: chip_rst.chip_1_rst_n
12	ASYNC	R	0h	Async Lpsc Reset Source: chip_rst.chip_1_rst_n
11	ICEPICK	R	0h	IcePick support Reset Source: chip_rst.chip_1_rst_n

Table 14-7257. PSC_MDCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PERMDIS	R	0h	Permanently disable Reset Source: chip_rst.chip_1_rst_n
9	PLLHANDSHAKE	R	0h	RTL parameter PLL_HANDSHAKE Reset Source: chip_rst.chip_1_rst_n
8:6	NUMSCRDISBALE	R	0h	Number of PWR_SCR_DISABLE interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
5:3	NUMCLKEN	R	0h	Number of PWR_CLK_EN interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
2:0	NUMCLK	R	0h	Number of PWR_CLKSTOP interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n

14.2.2.3.2.20 PSC_MDSTAT_j Register

1 PSC_MDSTAT_j Register (Offset = 800h + formula) [reset = 0h]

This register shows the status of each module. Requires one register per module on the device.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 7d

Table 14-7258. Instance Table

Instance Name	Physical Address
MCU_PSC0	**0400 0800h + formula**

Figure 14-2409. PSC_MDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED						EMUIHB	EMURST
NONE						R	R
0h						0h	0h

15	14	13	12	11	10	9	8
RESERVED			MCKOUT	MRSTDONE	MRSTZ	LRSTDONE	LRSTZ
NONE			R	R	R	R	R
0h			0h	X	X	X	X

7	6	5	4	3	2	1	0
RESERVED		STATE					
NONE		R					
0h		X					

Table 14-7260. PSC_MDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EMUIHB	R	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. Reset Source: chip_rst.chip_1_rst_n 0 `No emulation altering user-desired module state` 1 `Emulation alters user-desired module state`
16	EMURST	R	0h	Emulation Alters Reset Reset Source: chip_rst.chip_1_rst_n 0 `No emulation altering user-desired reset` 1 `Emulation has altered module reset to be different from what user desires`
15:13	RESERVED	NONE	0h	Reserved
12	MCKOUT	R	0h	Actual modclk output to module Reset Source: chip_rst.chip_1_rst_n 0 `modclk gated` 1 `modclk on`

Table 14-7260. PSC_MDSTAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MRSTDONE	R	X	Module reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 module reset initialization not done 1 module reset initialization done
10	MRSTZ	R	X	Module reset actual status Reset Source: chip_rst.chip_1_rst_n 0 module reset modrst_po* asserted 1 module reset modrst_po* de-asserted
9	LRSTDONE	R	X	Module local reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 local reset initialization not done 1 local reset initialization done
8	LRSTZ	R	X	Module local reset actual status Reset Source: chip_rst.chip_1_rst_n 0 local reset mod_lrst_po* asserted 1 local reset mod_lrst_po* de-asserted
7:6	RESERVED	NONE	0h	Reserved
5:0	STATE	R	X	These bits indicate the current module state Values 0x0 - 0x5 = Key States Values 0x21 - 0x2B = Transitional States Other Values = Reserved Reset Source: chip_rst.chip_1_rst_n 0 SwRstDisable 1 SyncRst 2 Disable 3 Enable 4 AutoSleep 5 AutoWake 33 Disable Clk On 34 Disable In-Prog (waiting for clkstop_ack = 1) 35 Retry Disable (new vbus_req, retry--give clkstop_req = 1 again) 36 Enable In-Prog 37 Sleep In-Prog 38 ClockOn (from SwRstDisable to SyncRst) 39 ClockOff (from SyncRst to SwRstDisable) 40 ClockOn (from Disable to DisableClkOn) 41 ClockOff (from DisableClkOn to Disable) 42 ClockOn (from AutoSleep/Wake to Sleep In-Prog) 43 ClockOff (from DisableClkOn or Sleep In-Prog to AutoSleep/Wake) OTHER Reserved

14.2.2.3.2.21 PSC_MDCTL_j Register

1 PSC_MDCTL_j Register (Offset = A00h + formula) [reset = 0h]

This register provides specific control for the individual module. One register per module on the device.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 7d

Table 14-7261. Instance Table

Instance Name	Physical Address
MCU_PSC0	0400 0A00h + formula

Figure 14-2410. PSC_MDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED						
R/W	NONE						
X	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			RESETISO	BLKCHIP1RST	EMUIHBIE	EMURSTIE	LRSTZ
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			NEXT				
NONE			R/W				
0h			0h				

Table 14-7263. PSC_MDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	X	Force Bit Reset Source: chip_rst.chip_1_rst_n 0 `No force` 1 `Force`
30:13	RESERVED	NONE	0h	Reserved
12	RESETISO	R/W	0h	Reset Isolation Reset Source: chip_rst.chip_1_rst_n 0 `No reset isolation` 1 `Enable reset isolation`
11	BLKCHIP1RST	R/W	0h	Block Chip_1_Reset Reset Source: chip_rst.chip_1_rst_n
10	EMUIHBIE	R/W	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. Reset Source: chip_rst.chip_1_rst_n 0 `Not enabled` 1 `Interrupt enabled`

Table 14-7263. PSC_MDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

9	EMURSTIE	R/W	0h	Emulation Alter Reset Interrupt Enable
				Reset Source: chip_rst.chip_1_rst_n
				`0 Not enabled`
				`1 Interrupt enabled`

8	LRSTZ	R/W	0h	Module local reset control
				Reset Source: chip_rst.chip_1_rst_n
				`0 assert local reset`
				`1 de-assert local reset`

7:5	RESERVED	NONE	0h	Reserved

4:0	NEXT	R/W	0h	Module Next State
				Only key states can be selected in this field.
				If a Reserved value is programmed into MDCTL.NEXT, hardware will internally force the state to SwRstDisable.
				If MDCFG.PERMDIS = 1, the module must remain in SwRstDisable after hardware places it in SwRstDisable state. The user is allowed to write this field but hardware ignores this field and always passes along MDCTL.NEXT = SwRstDisable.
				Reset Source: chip_rst.chip_1_rst_n
				`0 SwRstDisable`
				`1 SyncRst`
				`2 Disable`
				`3 Enable`
				`4 AutoSleep`
				`5 AutoWake`
				`OTHER Reserved`

14.2.3 Clocking Registers

14.2.3.1 MAIN_PLL_MMR_CFG Registers

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

14.2.3.1.1 MAIN_PLL_MMR Registers

14.2.3.1.1.1 MAIN_PLL_MMR Summary Table

Table 14-7264. PLL0_CFG Registers, Base Address=0068 0000h, Length=65536

Offset	Length	Register Name	MAIN_PLL_MMR Physical Address
0h	32	MAIN_PLL_MMR_CFG_PLL0_PID	0068 0000h
8h	32	MAIN_PLL_MMR_CFG_PLL0_CFG	0068 0008h
10h	32	MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0	0068 0010h
14h	32	MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1	0068 0014h
20h	32	MAIN_PLL_MMR_CFG_PLL0_CTRL	0068 0020h
24h	32	MAIN_PLL_MMR_CFG_PLL0_STAT	0068 0024h
30h	32	MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0	0068 0030h
34h	32	MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1	0068 0034h
38h	32	MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL	0068 0038h
40h	32	MAIN_PLL_MMR_CFG_PLL0_SS_CTRL	0068 0040h
44h	32	MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD	0068 0044h
60h	32	MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL	0068 0060h
64h	32	MAIN_PLL_MMR_CFG_PLL0_CAL_STAT	0068 0064h
80h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0	0068 0080h
84h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1	0068 0084h
88h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2	0068 0088h
8Ch	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3	0068 008Ch
90h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4	0068 0090h
94h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5	0068 0094h
98h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6	0068 0098h
9Ch	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7	0068 009Ch
A0h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8	0068 00A0h
A4h	32	MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9	0068 00A4h
1000h	32	MAIN_PLL_MMR_CFG_PLL1_PID	0068 1000h
1008h	32	MAIN_PLL_MMR_CFG_PLL1_CFG	0068 1008h
1010h	32	MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0	0068 1010h
1014h	32	MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1	0068 1014h
1020h	32	MAIN_PLL_MMR_CFG_PLL1_CTRL	0068 1020h
1024h	32	MAIN_PLL_MMR_CFG_PLL1_STAT	0068 1024h
1030h	32	MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0	0068 1030h
1034h	32	MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1	0068 1034h
1038h	32	MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL	0068 1038h
1040h	32	MAIN_PLL_MMR_CFG_PLL1_SS_CTRL	0068 1040h
1044h	32	MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD	0068 1044h
1060h	32	MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL	0068 1060h
1064h	32	MAIN_PLL_MMR_CFG_PLL1_CAL_STAT	0068 1064h
1080h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0	0068 1080h
1084h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1	0068 1084h
1088h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2	0068 1088h
108Ch	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3	0068 108Ch
1090h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4	0068 1090h

Table 14-7264. PLL0_CFG Registers, Base Address=0068 0000h, Length=65536 (continued)

Offset	Length	Register Name	MAIN_PLL_MMR Physical Address
1094h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5	0068 1094h
1098h	32	MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6	0068 1098h
2000h	32	MAIN_PLL_MMR_CFG_PLL2_PID	0068 2000h
2008h	32	MAIN_PLL_MMR_CFG_PLL2_CFG	0068 2008h
2010h	32	MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0	0068 2010h
2014h	32	MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1	0068 2014h
2020h	32	MAIN_PLL_MMR_CFG_PLL2_CTRL	0068 2020h
2024h	32	MAIN_PLL_MMR_CFG_PLL2_STAT	0068 2024h
2030h	32	MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0	0068 2030h
2034h	32	MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1	0068 2034h
2038h	32	MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL	0068 2038h
2040h	32	MAIN_PLL_MMR_CFG_PLL2_SS_CTRL	0068 2040h
2044h	32	MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD	0068 2044h
2060h	32	MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL	0068 2060h
2064h	32	MAIN_PLL_MMR_CFG_PLL2_CAL_STAT	0068 2064h
2080h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0	0068 2080h
2084h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1	0068 2084h
2088h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2	0068 2088h
208Ch	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3	0068 208Ch
2090h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4	0068 2090h
2094h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5	0068 2094h
2098h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6	0068 2098h
209Ch	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7	0068 209Ch
20A0h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8	0068 20A0h
20A4h	32	MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9	0068 20A4h
8000h	32	MAIN_PLL_MMR_CFG_PLL8_PID	0068 8000h
8008h	32	MAIN_PLL_MMR_CFG_PLL8_CFG	0068 8008h
8010h	32	MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0	0068 8010h
8014h	32	MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1	0068 8014h
8020h	32	MAIN_PLL_MMR_CFG_PLL8_CTRL	0068 8020h
8024h	32	MAIN_PLL_MMR_CFG_PLL8_STAT	0068 8024h
8030h	32	MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0	0068 8030h
8034h	32	MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1	0068 8034h
8038h	32	MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL	0068 8038h
8040h	32	MAIN_PLL_MMR_CFG_PLL8_SS_CTRL	0068 8040h
8044h	32	MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD	0068 8044h
8060h	32	MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL	0068 8060h
8064h	32	MAIN_PLL_MMR_CFG_PLL8_CAL_STAT	0068 8064h
8080h	32	MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0	0068 8080h
C000h	32	MAIN_PLL_MMR_CFG_PLL12_PID	0068 C000h
C008h	32	MAIN_PLL_MMR_CFG_PLL12_CFG	0068 C008h
C010h	32	MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0	0068 C010h
C014h	32	MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1	0068 C014h
C020h	32	MAIN_PLL_MMR_CFG_PLL12_CTRL	0068 C020h

Table 14-7264. PLL0_CFG Registers, Base Address=0068 0000h, Length=65536 (continued)

Offset	Length	Register Name	MAIN_PLL_MMR Physical Address
C024h	32	MAIN_PLL_MMR_CFG_PLL12_STAT	0068 C024h
C030h	32	MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0	0068 C030h
C034h	32	MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1	0068 C034h
C038h	32	MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL	0068 C038h
C040h	32	MAIN_PLL_MMR_CFG_PLL12_SS_CTRL	0068 C040h
C044h	32	MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD	0068 C044h
C060h	32	MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL	0068 C060h
C064h	32	MAIN_PLL_MMR_CFG_PLL12_CAL_STAT	0068 C064h
C080h	32	MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0	0068 C080h
E000h	32	MAIN_PLL_MMR_CFG_PLL14_PID	0068 E000h
E008h	32	MAIN_PLL_MMR_CFG_PLL14_CFG	0068 E008h
E010h	32	MAIN_PLL_MMR_CFG_PLL14_LOCKKEY0	0068 E010h
E014h	32	MAIN_PLL_MMR_CFG_PLL14_LOCKKEY1	0068 E014h
E020h	32	MAIN_PLL_MMR_CFG_PLL14_CTRL	0068 E020h
E024h	32	MAIN_PLL_MMR_CFG_PLL14_STAT	0068 E024h
E030h	32	MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL0	0068 E030h
E034h	32	MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL1	0068 E034h
E038h	32	MAIN_PLL_MMR_CFG_PLL14_DIV_CTRL	0068 E038h
E040h	32	MAIN_PLL_MMR_CFG_PLL14_SS_CTRL	0068 E040h
E044h	32	MAIN_PLL_MMR_CFG_PLL14_SS_SPREAD	0068 E044h
E060h	32	MAIN_PLL_MMR_CFG_PLL14_CAL_CTRL	0068 E060h
E064h	32	MAIN_PLL_MMR_CFG_PLL14_CAL_STAT	0068 E064h
E080h	32	MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL0	0068 E080h
E084h	32	MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL1	0068 E084h

14.2.3.1.1.2 MAIN_PLL_MMR_CFG_PLL0_PID Register

MAIN_PLL_MMR_CFG_PLL0_PID Register (Offset = 0h) [reset = 61801001h]

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Table 14-7265. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0000h

Figure 14-2411. MAIN_PLL_MMR_CFG_PLL0_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7267. MAIN_PLL_MMR_CFG_PLL0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.3 MAIN_PLL_MMR_CFG_PLL0_CFG Register

MAIN_PLL_MMR_CFG_PLL0_CFG Register (Offset = 8h) [reset = 3FF0801h]

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Table 14-7268. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0008h

Figure 14-2412. MAIN_PLL_MMR_CFG_PLL0_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-7270. MAIN_PLL_MMR_CFG_PLL0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-7270. MAIN_PLL_MMR_CFG_PLL0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.4 MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0 Register

MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0 Register (Offset = 10h) [reset = 0h]

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Table 14-7271. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0010h

Figure 14-2413. MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7273. MAIN_PLL_MMR_CFG_PLL0_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.5 MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1 Register

MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1 Register (Offset = 14h) [reset = 0h]

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Table 14-7274. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0014h

Figure 14-2414. MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7276. MAIN_PLL_MMR_CFG_PLL0_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n

14.2.3.1.1.6 MAIN_PLL_MMR_CFG_PLL0_CTRL Register

MAIN_PLL_MMR_CFG_PLL0_CTRL Register (Offset = 20h) [reset = 80010011h]

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Table 14-7277. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0020h

Figure 14-2415. MAIN_PLL_MMR_CFG_PLL0_CTRL Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td>BYPASS_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td colspan="7">RESERVED</td><td>BYP_ON_LOCKLOSS</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td>PLL_EN</td><td colspan="6">RESERVED</td><td>INTL_BYP_EN</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="2">RESERVED</td><td>CLK_4PH_EN</td><td>CLK_POSTDIV_EN</td><td colspan="2">RESERVED</td><td>DSM_EN</td><td>DAC_EN</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="2">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-7279. MAIN_PLL_MMR_CFG_PLL0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-7279. MAIN_PLL_MMR_CFG_PLL0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.7 MAIN_PLL_MMR_CFG_PLL0_STAT Register

MAIN_PLL_MMR_CFG_PLL0_STAT Register (Offset = 24h) [reset = 0h]

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Table 14-7280. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0024h

Figure 14-2416. MAIN_PLL_MMR_CFG_PLL0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7282. MAIN_PLL_MMR_CFG_PLL0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.8 MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register (Offset = 30h) [reset = 10h]

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Table 14-7283. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0030h

Figure 14-2417. MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FB_DIV_INT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_INT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-7285. MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.9 MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register (Offset = 34h) [reset = 0h]

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Table 14-7286. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0034h

Figure 14-2418. MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7288. MAIN_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.10 MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Register

MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Register (Offset = 38h) [reset = 1020001h]

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Table 14-7289. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0038h

Figure 14-2419. MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7291. MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-7291. MAIN_PLL_MMR_CFG_PLL0_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.11 MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Register

MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Register (Offset = 40h) [reset = 80000000h]

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Table 14-7292. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0040h

Figure 14-2420. MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="5">RESERVED</td><td colspan="2">WV_TBLE_MAXADDR</td></tr>
<tr><td>R/W</td><td colspan="5">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>1h</td><td colspan="5">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WV_TBLE_MAXADDR</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">NONE</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>DOWNSPREAD_EN</td><td colspan="3">RESERVED</td><td>WAVE_SEL</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-7294. MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7294. MAIN_PLL_MMR_CFG_PLL0_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.12 MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD Register

MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD Register (Offset = 44h) [reset = 10001h]

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Table 14-7295. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0044h

Figure 14-2421. MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7297. MAIN_PLL_MMR_CFG_PLL0_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.13 MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Register

MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Register (Offset = 60h) [reset = 20000h]

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Table 14-7298. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0060h

Figure 14-2422. MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7300. MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7300. MAIN_PLL_MMR_CFG_PLL0_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.14 MAIN_PLL_MMR_CFG_PLL0_CAL_STAT Register

MAIN_PLL_MMR_CFG_PLL0_CAL_STAT Register (Offset = 64h) [reset = 0h]

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Table 14-7301. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0064h

Figure 14-2423. MAIN_PLL_MMR_CFG_PLL0_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7303. MAIN_PLL_MMR_CFG_PLL0_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.15 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register (Offset = 80h) [reset = 0h]

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Table 14-7304. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0080h

Figure 14-2424. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7306. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.16 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register (Offset = 84h) [reset = 0h]

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Table 14-7307. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0084h

Figure 14-2425. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7309. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.17 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register (Offset = 88h) [reset = 0h]

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Table 14-7310. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0088h

Figure 14-2426. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7312. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.18 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register (Offset = 8Ch) [reset = 0h]

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Table 14-7313. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 008Ch

Figure 14-2427. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7315. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.19 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register (Offset = 90h) [reset = 0h]

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Table 14-7316. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0090h

Figure 14-2428. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7318. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.20 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register (Offset = 94h) [reset = 0h]

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Table 14-7319. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0094h

Figure 14-2429. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7321. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.21 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register (Offset = 98h) [reset = 0h]

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Table 14-7322. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 0098h

Figure 14-2430. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7324. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.22 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7 Register (Offset = 9Ch) [reset = 0h]

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Table 14-7325. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 009Ch

Figure 14-2431. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7327. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.23 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8 Register (Offset = A0h) [reset = 0h]

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Table 14-7328. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 00A0h

Figure 14-2432. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7330. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.24 MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9 Register

MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9 Register (Offset = A4h) [reset = 0h]

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Table 14-7331. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 00A4h

Figure 14-2433. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7333. MAIN_PLL_MMR_CFG_PLL0_HSDIV_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.25 MAIN_PLL_MMR_CFG_PLL1_PID Register

MAIN_PLL_MMR_CFG_PLL1_PID Register (Offset = 1000h) [reset = 61801001h]

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Table 14-7334. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1000h

Figure 14-2434. MAIN_PLL_MMR_CFG_PLL1_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7336. MAIN_PLL_MMR_CFG_PLL1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.26 MAIN_PLL_MMR_CFG_PLL1_CFG Register

MAIN_PLL_MMR_CFG_PLL1_CFG Register (Offset = 1008h) [reset = 7F0801h]

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Table 14-7337. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1008h

Figure 14-2435. MAIN_PLL_MMR_CFG_PLL1_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-7339. MAIN_PLL_MMR_CFG_PLL1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	7Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-7339. MAIN_PLL_MMR_CFG_PLL1_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.27 MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0 Register

MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0 Register (Offset = 1010h) [reset = 0h]

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Table 14-7340. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1010h

Figure 14-2436. MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">KEY</td><td>UNLOCKED</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7342. MAIN_PLL_MMR_CFG_PLL1_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.28 MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1 Register

MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1 Register (Offset = 1014h) [reset = 0h]

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Table 14-7343. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1014h

Figure 14-2437. MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7345. MAIN_PLL_MMR_CFG_PLL1_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers Reset Source: srst_n

14.2.3.1.1.29 MAIN_PLL_MMR_CFG_PLL1_CTRL Register

MAIN_PLL_MMR_CFG_PLL1_CTRL Register (Offset = 1020h) [reset = 80010011h]

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Table 14-7346. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1020h

Figure 14-2438. MAIN_PLL_MMR_CFG_PLL1_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>BYP_ON_LOCKLOSS</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>PLL_EN</td><td colspan="6">RESERVED</td><td>INTL_BYP_EN</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>CLK_4PH_EN</td><td>CLK_POSTDIV_EN</td><td colspan="2">RESERVED</td><td>DSM_EN</td><td>DAC_EN</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="2">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-7348. MAIN_PLL_MMR_CFG_PLL1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-7348. MAIN_PLL_MMR_CFG_PLL1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.30 MAIN_PLL_MMR_CFG_PLL1_STAT Register

MAIN_PLL_MMR_CFG_PLL1_STAT Register (Offset = 1024h) [reset = 0h]

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Table 14-7349. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1024h

Figure 14-2439. MAIN_PLL_MMR_CFG_PLL1_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7351. MAIN_PLL_MMR_CFG_PLL1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.31 MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0 Register (Offset = 1030h) [reset = 10h]

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Table 14-7352. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1030h

Figure 14-2440. MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7354. MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.32 MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1 Register (Offset = 1034h) [reset = 0h]

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Table 14-7355. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1034h

Figure 14-2441. MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7357. MAIN_PLL_MMR_CFG_PLL1_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.33 MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Register

MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Register (Offset = 1038h) [reset = 1020001h]

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Table 14-7358. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1038h

Figure 14-2442. MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7360. MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-7360. MAIN_PLL_MMR_CFG_PLL1_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.34 MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Register

MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Register (Offset = 1040h) [reset = 80000000h]

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Table 14-7361. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1040h

Figure 14-2443. MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7363. MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7363. MAIN_PLL_MMR_CFG_PLL1_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.35 MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD Register

MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD Register (Offset = 1044h) [reset = 10001h]

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Table 14-7364. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1044h

Figure 14-2444. MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MOD_DIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">SPREAD</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1h</td></tr>
</table>

Table 14-7366. MAIN_PLL_MMR_CFG_PLL1_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.36 MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Register

MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Register (Offset = 1060h) [reset = 20000h]

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Table 14-7367. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1060h

Figure 14-2445. MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7369. MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7369. MAIN_PLL_MMR_CFG_PLL1_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.37 MAIN_PLL_MMR_CFG_PLL1_CAL_STAT Register

MAIN_PLL_MMR_CFG_PLL1_CAL_STAT Register (Offset = 1064h) [reset = 0h]

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Table 14-7370. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1064h

Figure 14-2446. MAIN_PLL_MMR_CFG_PLL1_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7372. MAIN_PLL_MMR_CFG_PLL1_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.38 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0 Register (Offset = 1080h) [reset = 0h]

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Table 14-7373. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1080h

Figure 14-2447. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7375. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.39 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1 Register (Offset = 1084h) [reset = 0h]

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Table 14-7376. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1084h

Figure 14-2448. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7378. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.40 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2 Register

MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2 Register (Offset = 1088h) [reset = 0h]

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Table 14-7379. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1088h

Figure 14-2449. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-7381. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.41 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3 Register

MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3 Register (Offset = 108Ch) [reset = 0h]

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Table 14-7382. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 108Ch

Figure 14-2450. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7384. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.42 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4 Register

MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4 Register (Offset = 1090h) [reset = 0h]

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Table 14-7385. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1090h

Figure 14-2451. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7387. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.43 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5 Register

MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5 Register (Offset = 1094h) [reset = 0h]

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Table 14-7388. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1094h

Figure 14-2452. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7390. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.44 MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6 Register

MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6 Register (Offset = 1098h) [reset = 0h]

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Table 14-7391. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 1098h

Figure 14-2453. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7393. MAIN_PLL_MMR_CFG_PLL1_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.45 MAIN_PLL_MMR_CFG_PLL2_PID Register

MAIN_PLL_MMR_CFG_PLL2_PID Register (Offset = 2000h) [reset = 61801001h]

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Table 14-7394. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2000h

Figure 14-2454. MAIN_PLL_MMR_CFG_PLL2_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7396. MAIN_PLL_MMR_CFG_PLL2_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.46 MAIN_PLL_MMR_CFG_PLL2_CFG Register

MAIN_PLL_MMR_CFG_PLL2_CFG Register (Offset = 2008h) [reset = 3FF0801h]

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Table 14-7397. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2008h

Figure 14-2455. MAIN_PLL_MMR_CFG_PLL2_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
3FFh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
3FFh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-7399. MAIN_PLL_MMR_CFG_PLL2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-7399. MAIN_PLL_MMR_CFG_PLL2_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.47 MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0 Register

MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0 Register (Offset = 2010h) [reset = 0h]

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Table 14-7400. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2010h

Figure 14-2456. MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">KEY</td><td>UNLOCKED</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7402. MAIN_PLL_MMR_CFG_PLL2_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.48 MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1 Register

MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1 Register (Offset = 2014h) [reset = 0h]

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Table 14-7403. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2014h

Figure 14-2457. MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7405. MAIN_PLL_MMR_CFG_PLL2_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers Reset Source: srst_n

14.2.3.1.1.49 MAIN_PLL_MMR_CFG_PLL2_CTRL Register

MAIN_PLL_MMR_CFG_PLL2_CTRL Register (Offset = 2020h) [reset = 80010011h]

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Table 14-7406. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2020h

Figure 14-2458. MAIN_PLL_MMR_CFG_PLL2_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7408. MAIN_PLL_MMR_CFG_PLL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-7408. MAIN_PLL_MMR_CFG_PLL2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.50 MAIN_PLL_MMR_CFG_PLL2_STAT Register

MAIN_PLL_MMR_CFG_PLL2_STAT Register (Offset = 2024h) [reset = 0h]

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Table 14-7409. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2024h

Figure 14-2459. MAIN_PLL_MMR_CFG_PLL2_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LOCK</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7411. MAIN_PLL_MMR_CFG_PLL2_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.51 MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0 Register (Offset = 2030h) [reset = 10h]

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Table 14-7412. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2030h

Figure 14-2460. MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7414. MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.52 MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1 Register (Offset = 2034h) [reset = 0h]

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Table 14-7415. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2034h

Figure 14-2461. MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7417. MAIN_PLL_MMR_CFG_PLL2_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.53 MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Register

MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Register (Offset = 2038h) [reset = 1020001h]

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Table 14-7418. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2038h

Figure 14-2462. MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7420. MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-7420. MAIN_PLL_MMR_CFG_PLL2_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.54 MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Register

MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Register (Offset = 2040h) [reset = 80000000h]

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Table 14-7421. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2040h

Figure 14-2463. MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7423. MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7423. MAIN_PLL_MMR_CFG_PLL2_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.55 MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD Register

MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD Register (Offset = 2044h) [reset = 10001h]

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Table 14-7424. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2044h

Figure 14-2464. MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7426. MAIN_PLL_MMR_CFG_PLL2_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.56 MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Register

MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Register (Offset = 2060h) [reset = 20000h]

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Table 14-7427. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2060h

Figure 14-2465. MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_IN							
R/W							
0h							

Table 14-7429. MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7429. MAIN_PLL_MMR_CFG_PLL2_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.57 MAIN_PLL_MMR_CFG_PLL2_CAL_STAT Register

MAIN_PLL_MMR_CFG_PLL2_CAL_STAT Register (Offset = 2064h) [reset = 0h]

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Table 14-7430. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2064h

Figure 14-2466. MAIN_PLL_MMR_CFG_PLL2_CAL_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">LOCK_CNT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CAL_OUT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_OUT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7432. MAIN_PLL_MMR_CFG_PLL2_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.58 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0 Register (Offset = 2080h) [reset = 0h]

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Table 14-7433. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2080h

Figure 14-2467. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7435. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.59 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1 Register (Offset = 2084h) [reset = 0h]

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Table 14-7436. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2084h

Figure 14-2468. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7438. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.60 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2 Register (Offset = 2088h) [reset = 0h]

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Table 14-7439. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2088h

Figure 14-2469. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7441. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.61 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3 Register (Offset = 208Ch) [reset = 0h]

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Table 14-7442. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 208Ch

Figure 14-2470. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7444. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.62 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4 Register (Offset = 2090h) [reset = 0h]

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Table 14-7445. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2090h

Figure 14-2471. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7447. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.63 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5 Register (Offset = 2094h) [reset = 0h]

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Table 14-7448. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2094h

Figure 14-2472. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7450. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.64 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6 Register (Offset = 2098h) [reset = 0h]

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Table 14-7451. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 2098h

Figure 14-2473. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7453. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.65 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7 Register (Offset = 209Ch) [reset = 0h]

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Table 14-7454. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 209Ch

Figure 14-2474. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7456. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.66 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8 Register (Offset = 20A0h) [reset = 0h]

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Table 14-7457. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 20A0h

Figure 14-2475. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7459. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.67 MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9 Register

MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9 Register (Offset = 20A4h) [reset = 0h]

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Table 14-7460. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 20A4h

Figure 14-2476. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7462. MAIN_PLL_MMR_CFG_PLL2_HSDIV_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.68 MAIN_PLL_MMR_CFG_PLL8_PID Register

MAIN_PLL_MMR_CFG_PLL8_PID Register (Offset = 8000h) [reset = 61801001h]

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Table 14-7463. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8000h

Figure 14-2477. MAIN_PLL_MMR_CFG_PLL8_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7465. MAIN_PLL_MMR_CFG_PLL8_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.69 MAIN_PLL_MMR_CFG_PLL8_CFG Register

MAIN_PLL_MMR_CFG_PLL8_CFG Register (Offset = 8008h) [reset = 10801h]

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Table 14-7466. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8008h

Figure 14-2478. MAIN_PLL_MMR_CFG_PLL8_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-7468. MAIN_PLL_MMR_CFG_PLL8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-7468. MAIN_PLL_MMR_CFG_PLL8_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.70 MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0 Register

MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0 Register (Offset = 8010h) [reset = 0h]

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Table 14-7469. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8010h

Figure 14-2479. MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7471. MAIN_PLL_MMR_CFG_PLL8_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition8 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.71 MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1 Register

MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1 Register (Offset = 8014h) [reset = 0h]

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Table 14-7472. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8014h

Figure 14-2480. MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7474. MAIN_PLL_MMR_CFG_PLL8_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition8 registers Reset Source: srst_n

14.2.3.1.1.72 MAIN_PLL_MMR_CFG_PLL8_CTRL Register

MAIN_PLL_MMR_CFG_PLL8_CTRL Register (Offset = 8020h) [reset = 80010011h]

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Table 14-7475. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8020h

Figure 14-2481. MAIN_PLL_MMR_CFG_PLL8_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7477. MAIN_PLL_MMR_CFG_PLL8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-7477. MAIN_PLL_MMR_CFG_PLL8_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.73 MAIN_PLL_MMR_CFG_PLL8_STAT Register

MAIN_PLL_MMR_CFG_PLL8_STAT Register (Offset = 8024h) [reset = 0h]

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Table 14-7478. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8024h

Figure 14-2482. MAIN_PLL_MMR_CFG_PLL8_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7480. MAIN_PLL_MMR_CFG_PLL8_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.74 MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0 Register (Offset = 8030h) [reset = 10h]

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Table 14-7481. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8030h

Figure 14-2483. MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7483. MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.75 MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1 Register (Offset = 8034h) [reset = 0h]

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Table 14-7484. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8034h

Figure 14-2484. MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7486. MAIN_PLL_MMR_CFG_PLL8_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.76 MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Register

MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Register (Offset = 8038h) [reset = 1020001h]

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Table 14-7487. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8038h

Figure 14-2485. MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7489. MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-7489. MAIN_PLL_MMR_CFG_PLL8_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.77 MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Register

MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Register (Offset = 8040h) [reset = 80000001h]

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Table 14-7490. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8040h

Figure 14-2486. MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="5">RESERVED</td><td colspan="2">WV_TBLE_MAXADDR</td></tr>
<tr><td>R/W</td><td colspan="5">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>1h</td><td colspan="5">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WV_TBLE_MAXADDR</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">NONE</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>DOWNSPREAD_EN</td><td colspan="3">RESERVED</td><td>WAVE_SEL</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>1h</td></tr>
</table>

Table 14-7492. MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7492. MAIN_PLL_MMR_CFG_PLL8_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	1h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.78 MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD Register

MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD Register (Offset = 8044h) [reset = 10001h]

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Table 14-7493. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8044h

Figure 14-2487. MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7495. MAIN_PLL_MMR_CFG_PLL8_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.79 MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Register

MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Register (Offset = 8060h) [reset = 20000h]

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Table 14-7496. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8060h

Figure 14-2488. MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7498. MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7498. MAIN_PLL_MMR_CFG_PLL8_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.80 MAIN_PLL_MMR_CFG_PLL8_CAL_STAT Register

MAIN_PLL_MMR_CFG_PLL8_CAL_STAT Register (Offset = 8064h) [reset = 0h]

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Table 14-7499. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8064h

Figure 14-2489. MAIN_PLL_MMR_CFG_PLL8_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_OUT							
R							
0h							

Table 14-7501. MAIN_PLL_MMR_CFG_PLL8_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.81 MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0 Register (Offset = 8080h) [reset = 0h]

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Table 14-7502. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 8080h

Figure 14-2490. MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7504. MAIN_PLL_MMR_CFG_PLL8_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.82 MAIN_PLL_MMR_CFG_PLL12_PID Register

MAIN_PLL_MMR_CFG_PLL12_PID Register (Offset = C000h) [reset = 61801001h]

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Table 14-7505. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C000h

Figure 14-2491. MAIN_PLL_MMR_CFG_PLL12_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7507. MAIN_PLL_MMR_CFG_PLL12_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.83 MAIN_PLL_MMR_CFG_PLL12_CFG Register

MAIN_PLL_MMR_CFG_PLL12_CFG Register (Offset = C008h) [reset = 10801h]

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Table 14-7508. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C008h

Figure 14-2492. MAIN_PLL_MMR_CFG_PLL12_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
1h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HSDIV_PRSNT							
R							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-7510. MAIN_PLL_MMR_CFG_PLL12_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-7510. MAIN_PLL_MMR_CFG_PLL12_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.84 MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0 Register

MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0 Register (Offset = C010h) [reset = 0h]

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Table 14-7511. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C010h

Figure 14-2493. MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7513. MAIN_PLL_MMR_CFG_PLL12_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition12 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.85 MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1 Register

MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1 Register (Offset = C014h) [reset = 0h]

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Table 14-7514. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C014h

Figure 14-2494. MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7516. MAIN_PLL_MMR_CFG_PLL12_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition12 registers Reset Source: srst_n

14.2.3.1.1.86 MAIN_PLL_MMR_CFG_PLL12_CTRL Register

MAIN_PLL_MMR_CFG_PLL12_CTRL Register (Offset = C020h) [reset = 80010011h]

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Table 14-7517. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C020h

Figure 14-2495. MAIN_PLL_MMR_CFG_PLL12_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7519. MAIN_PLL_MMR_CFG_PLL12_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-7519. MAIN_PLL_MMR_CFG_PLL12_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.87 MAIN_PLL_MMR_CFG_PLL12_STAT Register

MAIN_PLL_MMR_CFG_PLL12_STAT Register (Offset = C024h) [reset = 0h]

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Table 14-7520. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C024h

Figure 14-2496. MAIN_PLL_MMR_CFG_PLL12_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LOCK</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7522. MAIN_PLL_MMR_CFG_PLL12_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.88 MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0 Register (Offset = C030h) [reset = 10h]

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Table 14-7523. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C030h

Figure 14-2497. MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7525. MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.89 MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1 Register (Offset = C034h) [reset = 0h]

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Table 14-7526. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C034h

Figure 14-2498. MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7528. MAIN_PLL_MMR_CFG_PLL12_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.90 MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Register

MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Register (Offset = C038h) [reset = 1020001h]

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Table 14-7529. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C038h

Figure 14-2499. MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7531. MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-7531. MAIN_PLL_MMR_CFG_PLL12_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.91 MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Register

MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Register (Offset = C040h) [reset = 80000000h]

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Table 14-7532. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C040h

Figure 14-2500. MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7534. MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7534. MAIN_PLL_MMR_CFG_PLL12_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.92 MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD Register

MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD Register (Offset = C044h) [reset = 10001h]

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Table 14-7535. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C044h

Figure 14-2501. MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7537. MAIN_PLL_MMR_CFG_PLL12_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.93 MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Register

MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Register (Offset = C060h) [reset = 20000h]

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Table 14-7538. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C060h

Figure 14-2502. MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7540. MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7540. MAIN_PLL_MMR_CFG_PLL12_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.94 MAIN_PLL_MMR_CFG_PLL12_CAL_STAT Register

MAIN_PLL_MMR_CFG_PLL12_CAL_STAT Register (Offset = C064h) [reset = 0h]

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Table 14-7541. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C064h

Figure 14-2503. MAIN_PLL_MMR_CFG_PLL12_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7543. MAIN_PLL_MMR_CFG_PLL12_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.95 MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0 Register (Offset = C080h) [reset = 0h]

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Table 14-7544. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 C080h

Figure 14-2504. MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7546. MAIN_PLL_MMR_CFG_PLL12_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.96 MAIN_PLL_MMR_CFG_PLL14_PID Register

MAIN_PLL_MMR_CFG_PLL14_PID Register (Offset = E000h) [reset = 61801001h]

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Table 14-7547. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E000h

Figure 14-2505. MAIN_PLL_MMR_CFG_PLL14_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7549. MAIN_PLL_MMR_CFG_PLL14_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.1.97 MAIN_PLL_MMR_CFG_PLL14_CFG Register

MAIN_PLL_MMR_CFG_PLL14_CFG Register (Offset = E008h) [reset = 30801h]

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Table 14-7550. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E008h

Figure 14-2506. MAIN_PLL_MMR_CFG_PLL14_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-7552. MAIN_PLL_MMR_CFG_PLL14_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-7552. MAIN_PLL_MMR_CFG_PLL14_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.1.98 MAIN_PLL_MMR_CFG_PLL14_LOCKKEY0 Register

MAIN_PLL_MMR_CFG_PLL14_LOCKKEY0 Register (Offset = E010h) [reset = 0h]

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Table 14-7553. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E010h

Figure 14-2507. MAIN_PLL_MMR_CFG_PLL14_LOCKKEY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">KEY</td><td>UNLOCKED</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7555. MAIN_PLL_MMR_CFG_PLL14_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition14 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.1.99 MAIN_PLL_MMR_CFG_PLL14_LOCKKEY1 Register

MAIN_PLL_MMR_CFG_PLL14_LOCKKEY1 Register (Offset = E014h) [reset = 0h]

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Table 14-7556. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E014h

Figure 14-2508. MAIN_PLL_MMR_CFG_PLL14_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7558. MAIN_PLL_MMR_CFG_PLL14_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition14 registers Reset Source: srst_n

14.2.3.1.1.100 MAIN_PLL_MMR_CFG_PLL14_CTRL Register

MAIN_PLL_MMR_CFG_PLL14_CTRL Register (Offset = E020h) [reset = 80010011h]

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Table 14-7559. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E020h

Figure 14-2509. MAIN_PLL_MMR_CFG_PLL14_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7561. MAIN_PLL_MMR_CFG_PLL14_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-7561. MAIN_PLL_MMR_CFG_PLL14_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.101 MAIN_PLL_MMR_CFG_PLL14_STAT Register

MAIN_PLL_MMR_CFG_PLL14_STAT Register (Offset = E024h) [reset = 0h]

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Table 14-7562. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E024h

Figure 14-2510. MAIN_PLL_MMR_CFG_PLL14_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7564. MAIN_PLL_MMR_CFG_PLL14_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.1.102 MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL0 Register (Offset = E030h) [reset = 10h]

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Table 14-7565. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E030h

Figure 14-2511. MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7567. MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.1.103 MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL1 Register (Offset = E034h) [reset = 0h]

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Table 14-7568. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E034h

Figure 14-2512. MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7570. MAIN_PLL_MMR_CFG_PLL14_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.1.104 MAIN_PLL_MMR_CFG_PLL14_DIV_CTRL Register

MAIN_PLL_MMR_CFG_PLL14_DIV_CTRL Register (Offset = E038h) [reset = 1020001h]

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Table 14-7571. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E038h

Figure 14-2513. MAIN_PLL_MMR_CFG_PLL14_DIV_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">POST_DIV2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">POST_DIV1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">REF_DIV</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-7573. MAIN_PLL_MMR_CFG_PLL14_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-7573. MAIN_PLL_MMR_CFG_PLL14_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.105 MAIN_PLL_MMR_CFG_PLL14_SS_CTRL Register

MAIN_PLL_MMR_CFG_PLL14_SS_CTRL Register (Offset = E040h) [reset = 80000000h]

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Table 14-7574. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E040h

Figure 14-2514. MAIN_PLL_MMR_CFG_PLL14_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7576. MAIN_PLL_MMR_CFG_PLL14_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7576. MAIN_PLL_MMR_CFG_PLL14_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.1.106 MAIN_PLL_MMR_CFG_PLL14_SS_SPREAD Register

MAIN_PLL_MMR_CFG_PLL14_SS_SPREAD Register (Offset = E044h) [reset = 10001h]

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Table 14-7577. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E044h

Figure 14-2515. MAIN_PLL_MMR_CFG_PLL14_SS_SPREAD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MOD_DIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">SPREAD</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1h</td></tr>
</table>

Table 14-7579. MAIN_PLL_MMR_CFG_PLL14_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.1.107 MAIN_PLL_MMR_CFG_PLL14_CAL_CTRL Register

MAIN_PLL_MMR_CFG_PLL14_CAL_CTRL Register (Offset = E060h) [reset = 20000h]

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Table 14-7580. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E060h

Figure 14-2516. MAIN_PLL_MMR_CFG_PLL14_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7582. MAIN_PLL_MMR_CFG_PLL14_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7582. MAIN_PLL_MMR_CFG_PLL14_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.1.108 MAIN_PLL_MMR_CFG_PLL14_CAL_STAT Register

MAIN_PLL_MMR_CFG_PLL14_CAL_STAT Register (Offset = E064h) [reset = 0h]

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Table 14-7583. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E064h

Figure 14-2517. MAIN_PLL_MMR_CFG_PLL14_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7585. MAIN_PLL_MMR_CFG_PLL14_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.1.109 MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL0 Register

MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL0 Register (Offset = E080h) [reset = 0h]

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Table 14-7586. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E080h

Figure 14-2518. MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7588. MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.1.110 MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL1 Register

MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL1 Register (Offset = E084h) [reset = 0h]

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Table 14-7589. Instance Table

Instance Name	Physical Address
PLL0_CFG	0068 E084h

Figure 14-2519. MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7591. MAIN_PLL_MMR_CFG_PLL14_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2 MCU_PLL_MMR_CFG Registers

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

14.2.3.2.1 MCU_PLL_MMR Registers

14.2.3.2.1.1 MCU_PLL_MMR Summary Table

Table 14-7592. MCU_PLL0_CFG Registers, Base Address=0404 0000h, Length=4096

Offset	Length	Register Name	MCU_PLL_MMR Physical Address
0h	32	MCU_PLL_MMR_CFG_PLL0_PID	0404 0000h
8h	32	MCU_PLL_MMR_CFG_PLL0_CFG	0404 0008h
10h	32	MCU_PLL_MMR_CFG_PLL0_LOCKKEY0	0404 0010h
14h	32	MCU_PLL_MMR_CFG_PLL0_LOCKKEY1	0404 0014h
20h	32	MCU_PLL_MMR_CFG_PLL0_CTRL	0404 0020h
24h	32	MCU_PLL_MMR_CFG_PLL0_STAT	0404 0024h
30h	32	MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0	0404 0030h
34h	32	MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1	0404 0034h
38h	32	MCU_PLL_MMR_CFG_PLL0_DIV_CTRL	0404 0038h
40h	32	MCU_PLL_MMR_CFG_PLL0_SS_CTRL	0404 0040h
44h	32	MCU_PLL_MMR_CFG_PLL0_SS_SPREAD	0404 0044h
60h	32	MCU_PLL_MMR_CFG_PLL0_CAL_CTRL	0404 0060h
64h	32	MCU_PLL_MMR_CFG_PLL0_CAL_STAT	0404 0064h
80h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0	0404 0080h
84h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1	0404 0084h
88h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2	0404 0088h
8Ch	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3	0404 008Ch
90h	32	MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4	0404 0090h

14.2.3.2.1.2 MCU_PLL_MMR_CFG_PLL0_PID Register

MCU_PLL_MMR_CFG_PLL0_PID Register (Offset = 0h) [reset = 61801001h]

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Table 14-7593. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0000h

Figure 14-2520. MCU_PLL_MMR_CFG_PLL0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">MISC</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">2h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-7595. MCU_PLL_MMR_CFG_PLL0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.2.1.3 MCU_PLL_MMR_CFG_PLL0_CFG Register

MCU_PLL_MMR_CFG_PLL0_CFG Register (Offset = 8h) [reset = 1F0801h]

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Table 14-7596. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0008h

Figure 14-2521. MCU_PLL_MMR_CFG_PLL0_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
1Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HSDIV_PRSNT							
R							
1Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-7598. MCU_PLL_MMR_CFG_PLL0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	1Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-7598. MCU_PLL_MMR_CFG_PLL0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.2.1.4 MCU_PLL_MMR_CFG_PLL0_LOCKKEY0 Register

MCU_PLL_MMR_CFG_PLL0_LOCKKEY0 Register (Offset = 10h) [reset = 0h]

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Table 14-7599. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0010h

Figure 14-2522. MCU_PLL_MMR_CFG_PLL0_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7601. MCU_PLL_MMR_CFG_PLL0_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.2.1.5 MCU_PLL_MMR_CFG_PLL0_LOCKKEY1 Register

MCU_PLL_MMR_CFG_PLL0_LOCKKEY1 Register (Offset = 14h) [reset = 0h]

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Table 14-7602. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0014h

Figure 14-2523. MCU_PLL_MMR_CFG_PLL0_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7604. MCU_PLL_MMR_CFG_PLL0_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n

14.2.3.2.1.6 MCU_PLL_MMR_CFG_PLL0_CTRL Register

MCU_PLL_MMR_CFG_PLL0_CTRL Register (Offset = 20h) [reset = 80010011h]

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Table 14-7605. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0020h

Figure 14-2524. MCU_PLL_MMR_CFG_PLL0_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7607. MCU_PLL_MMR_CFG_PLL0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved

Table 14-7607. MCU_PLL_MMR_CFG_PLL0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.2.1.7 MCU_PLL_MMR_CFG_PLL0_STAT Register

MCU_PLL_MMR_CFG_PLL0_STAT Register (Offset = 24h) [reset = 0h]

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Table 14-7608. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0024h

Figure 14-2525. MCU_PLL_MMR_CFG_PLL0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7610. MCU_PLL_MMR_CFG_PLL0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.2.1.8 MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register

MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register (Offset = 30h) [reset = 10h]

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Table 14-7611. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0030h

Figure 14-2526. MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7613. MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.2.1.9 MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register

MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register (Offset = 34h) [reset = 0h]

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Table 14-7614. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0034h

Figure 14-2527. MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7616. MCU_PLL_MMR_CFG_PLL0_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.2.1.10 MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Register

MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Register (Offset = 38h) [reset = 1020001h]

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Table 14-7617. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0038h

Figure 14-2528. MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7619. MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved

Table 14-7619. MCU_PLL_MMR_CFG_PLL0_DIV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.11 MCU_PLL_MMR_CFG_PLL0_SS_CTRL Register

MCU_PLL_MMR_CFG_PLL0_SS_CTRL Register (Offset = 40h) [reset = 80000000h]

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Table 14-7620. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0040h

Figure 14-2529. MCU_PLL_MMR_CFG_PLL0_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7622. MCU_PLL_MMR_CFG_PLL0_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7622. MCU_PLL_MMR_CFG_PLL0_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.2.1.12 MCU_PLL_MMR_CFG_PLL0_SS_SPREAD Register

MCU_PLL_MMR_CFG_PLL0_SS_SPREAD Register (Offset = 44h) [reset = 10001h]

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Table 14-7623. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0044h

Figure 14-2530. MCU_PLL_MMR_CFG_PLL0_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7625. MCU_PLL_MMR_CFG_PLL0_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.2.1.13 MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Register

MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Register (Offset = 60h) [reset = 20000h]

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Table 14-7626. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0060h

Figure 14-2531. MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>FAST_CAL</td><td>RESERVED</td><td colspan="3">CAL_CNT</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CAL_BYP</td><td colspan="3">RESERVED</td><td colspan="4">CAL_IN</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_IN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7628. MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7628. MCU_PLL_MMR_CFG_PLL0_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.2.1.14 MCU_PLL_MMR_CFG_PLL0_CAL_STAT Register

MCU_PLL_MMR_CFG_PLL0_CAL_STAT Register (Offset = 64h) [reset = 0h]

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Table 14-7629. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0064h

Figure 14-2532. MCU_PLL_MMR_CFG_PLL0_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7631. MCU_PLL_MMR_CFG_PLL0_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.2.1.15 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register

MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register (Offset = 80h) [reset = 0h]

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Table 14-7632. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0080h

Figure 14-2533. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7634. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.16 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register

MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register (Offset = 84h) [reset = 0h]

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Table 14-7635. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0084h

Figure 14-2534. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7637. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.17 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register

MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register (Offset = 88h) [reset = 0h]

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Table 14-7638. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0088h

Figure 14-2535. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-7640. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.18 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register

MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register (Offset = 8Ch) [reset = 0h]

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Table 14-7641. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 008Ch

Figure 14-2536. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7643. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.1.19 MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register

MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register (Offset = 90h) [reset = 0h]

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Table 14-7644. Instance Table

Instance Name	Physical Address
MCU_PLL0_CFG	0404 0090h

Figure 14-2537. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7646. MCU_PLL_MMR_CFG_PLL0_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.3 PLLCTRL Registers

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

14.2.3.3.1 PLLCTRL0 Registers

Table 14-5111 lists the PLLCTRL0 registers. All register offset addresses not listed in Table 14-5111 should be considered as reserved locations and the register contents should not be modified.

Table 14-7647. PLLCTRL0 Instances

Instance	Base Address
PLLCTRL0	0041 0000h
MCU_PLLCTRL0	4020 0000h

Table 14-7648. PLLCTRL0 Registers

Offset	Acronym	Register Name	PLLCTRL0 Physical Address	MCU_PLLCTRL0 Physical Address
0h	PID	Peripheral identification register	0041 0000h	4020 0000h
100h	PLLCTL	PLL control register	0041 0100h	4020 0100h
118h	PLLDIV1	PLL controller divider1 control register	0041 0118h	4020 0118h
11Ch	PLLDIV2	PLL controller divider2 control register	0041 011Ch	4020 011Ch
138h	PLLCMD	PLL Controller command register	0041 0138h	4020 0138h
13Ch	PLLSTAT	PLL Controller status register	0041 013Ch	4020 013Ch
140h	ALNCTL	PLL Controller clock align control register	0041 0140h	4020 0140h
144h	DCHANGE	PLLDIV ratio change register	0041 0144h	4020 0144h

1 PID Register (Offset = 0h) [reset = 44815C00h]

PID is shown in Figure 14-2538 and described in Table 14-5113.

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Peripheral identification register

Table 14-7649. PID Instances

Instance	Physical Address
PLLCTRL0	0041 0000h
MCU_PLLCTRL0	4020 0000h

Figure 14-2538. PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-0h		R-481h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-Bh					R-4h			R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-7651. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Peripheral identification register scheme
29-28	BU	R	0h	Business Unit
27-16	FUNC	R	481h	Module ID
15-11	RTL	R	Bh	RTL revision. Will vary depending on release
10-8	MAJOR	R	4h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

2 PLLCTL Register (Offset = 100h) [reset = X]

PLLCTL is shown in Figure 14-2539 and described in Table 14-5115.

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PLL control register

Table 14-7652. PLLCTL Instances

Instance	Physical Address
PLLCTRL0	0041 0100h
MCU_PLLCTRL0	4020 0100h

Figure 14-2539. PLLCTL Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD2</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD2</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RSVD2</td><td>EXCLKSRC</td><td>CLKMODE</td></tr>
<tr><td colspan="6">R/W-0h</td><td>R/W-0h</td><td>R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PLLSELB</td><td>RSVD1</td><td>PLLENSRC</td><td>PLLDIS</td><td>PLLRST</td><td>RSVD</td><td>PLLPWRDN</td><td>PLLEN</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-1h</td><td>R/W-X</td><td>R/W-X</td><td>R/W-0h</td><td>R/W-1h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-7654. PLLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RSVD2	R/W	0h	Reserved
9	EXCLKSRC	R/W	0h	Selects between using bypass clock or an external clock source. 0 = bypass clock 1 = external clock source
8	CLKMODE	R/W	X	Reference Clock Selection. 1 = clkin_pi is the reference clock 0 = oscin_pi is the reference clock This bit is only applicable when d_clkmodesrc_pi = 1. It is otherwise don't care.
7	PLLSELB	R/W	0h	Selects PLL A versus PLL B. 1 = PLL B is selected. PLL A is put in power down (pll_a_pwrdn_po = 1) 0 = PLL A is selected. PLL B is put in power down. (pll_b_pwrdn_po = 1)
6	RSVD1	R/W	0h	Reserved
5	PLLENSRC	R/W	1h	PLLEN Mux Control Source 1 = PLLEN Mux is controlled by input pllen_pi. PLLCTL.PLLEN is don't care 0 = PLLEN Mux is controlled by PLLCTL.PLLEN. pllen_pi is don't care

Table 14-7654. PLLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLLDIS	R/W	X	Asserts DISABLE to PLL if Supported 1 = PLL Controller output pll_disable_po = 1. 0 = PLL Controller output pll_disable_po = 0. Chip team must pay attention to the disable signal polarity of the PLL they use. Some PLLs may require PLLDIS = 1 to disable PLL, some PLLs require PLLDIS = 0 to disable PLL. Note that PLL Controller only supports one pll_disable_po output for both PLLA and PLLB. This is possible because the non-selected PLL is already placed in power down mode.
3	PLLRST	R/W	X	Asserts RESET to PLL if Supported. Controls output pll_reset_po. 1 = PLL Controller output pll_reset_po = 1. 0 = PLL Controller output pll_reset_po = 0. Chip team must pay attention to the reset signal polarity of the PLL they use. Some PLLs require PLLRST = 1 to reset the PLL. Some PLLs require PLLRST = 0 to reset the PLL. Note that PLL Controller only supports one pll_reset_po output for both PLLA and PLLB. This is possible because the non-selected PLL is already placed in power down mode.
2	RSVD	R/W	0h	Reserved
1	PLLPWRDN	R/W	1h	Selects PLL Power Down for the PLL selected by PLLSELB. The PLL not selected by PLLSELB is NOT controlled by PLLPWRDN bit. The not-selected PLL will stay in power down regardless of PLLPWRDN value. 0 = Selected PLL Operational. If PLLSELB = 0 (PLLA selected), PLL controller output pll_a_pwrdn_po is deasserted low. If PLLSELB = 1 (PLLB selected), PLL controller output pll_b_pwrdn_po is deasserted low. 1 = Selected PLL Placed In Power Down State. If PLLSELB = 0 (PLLA selected), PLL controller outputs pll_a_pwrdn_po is asserted high. If PLLSELB = 1 (PLLB selected), pll_b_pwrdn_po is asserted
0	PLLEN	R/W	0h	PLL Mode Enable This bit controls the multiplexer before the SYSCLK dividers D1 to Dn. 0 = Bypass Mode PreDiv, PLL, and PostDiv are bypassed. SYSCLK divided down directly from input reference clock refclk. 1 = PLL Mode PLL is used. SYSCLK divided down from PostDiv output

3 PLLDIV1 Register (Offset = 118h) [reset = X]

PLLDIV1 is shown in Figure 14-2540 and described in Table 14-5117.

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PLL controller divider1 control register

Table 14-7655. PLLDIV1 Instances

Instance	Physical Address
PLLCTRL0	0041 0118h
MCU_PLLCTRL0	4020 0118h

Figure 14-2540. PLLDIV1 Register

31	30	29	28	27	26	25	24
RSVD1							
R/W-0h							

23	22	21	20	19	18	17	16
RSVD1							
R/W-0h							

15	14	13	12	11	10	9	8
DN_EN	HALF_RATIO	RSVD					
R/W-X	R/W-0h	R/W-0h					

7	6	5	4	3	2	1	0
RATIO							
R/W-X							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-7657. PLLDIV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD1	R/W	0h	Reserved
15	DN_EN	R/W	X	Divider Dn Enable 0 = Divider n Disabled. SYSCLKn is also gated before and after divider Dn. 1 = Divider n Enabled
14	HALF_RATIO	R/W	0h	Ratio is in half steps. Example 1: if RATIO = 00000 and HALFRATIO = 1 the divider will be /1.5. Example 2: RATIO = 10111 and HALFRATIO = 1 divider will be /24.5. Example 3: if RATIO = 00011 and HALFRATIO = 0 divider will be /4. THE HALF RATIO DIVIDER IS NOT A 50% DUTY CYCLE. It is a single 1x high clock pulse followed by low time until ratio is met. Note: To enable half step ratio dividers user must also set the associated bit in the PLLHDIVEN register PRIOR to writing the PLLDIVn register. If PLLHDIVEN register is not enabled then HALF_RATIO will not be writable. Changing the PLLHDIVEN register, set or clear, will not set or clear the HALF_RATIO bit in PLLDIVn register. This is to protect and enable backward compatible software in the chance it accidentally wrote this bit field.
13-8	RSVD	R/W	0h	Reserved

Table 14-7657. PLLDIV1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RATIO	R/W	X	Divider Dn Ratio (SYSCLKn divider) 00000 = /1 00001 = /2 00010 = /3 00011 = /4 00100 = /5 00101 = /6 00110 = /7 00111 = /8 01000 = /9 01001 = /10 01010 = /11 01011 = /12 01100 = /13 01101 = /14 01110 = /15 01111 = /16 10000 = /17 10001 = /18 10010 = /19 10011 = /20 10100 = /21 10101 = /22 10110 = /23 10111 = /24 11000 = /25 11001 = /26 11010 = /27 11011 = /28 11100 = /29 11101 = /30 11110 = /31 11111 = /32 Note that the actual PLLDIVx divide ratio will not be modified when this field is written to. User must also set the GOSET bit so that the SYSCLKs selected in ALNCTL can change their RATIOs to the new values and remain phase-aligned. Note: see HALF_RATIO bit.

4 PLLDIV2 Register (Offset = 11Ch) [reset = X]

PLLDIV2 is shown in Figure 14-2541 and described in Table 14-5119.

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PLL controller divider2 control register

Table 14-7658. PLLDIV2 Instances

Instance	Physical Address
PLLCTRL0	0041 011Ch
MCU_PLLCTRL0	4020 011Ch

Figure 14-2541. PLLDIV2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD1</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD1</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>DN_EN</td><td>HALF_RATIO</td><td colspan="6">RSVD</td></tr>
<tr><td>R/W-X</td><td>R/W-0h</td><td colspan="6">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATIO</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-7660. PLLDIV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD1	R/W	0h	Reserved
15	DN_EN	R/W	X	Divider Dn Enable 0 = Divider n Disabled. SYSCLKn is also gated before and after divider Dn. 1 = Divider n Enabled
14	HALF_RATIO	R/W	0h	Ratio is in half steps. Example 1: if RATIO = 00000 and HALFRATIO = 1 the divider will be /1.5. Example 2: RATIO = 10111 and HALFRATIO = 1 divider will be /24.5. Example 3: if RATIO = 00011 and HALFRATIO = 0 divider will be /4. THE HALF RATIO DIVIDER IS NOT A 50% DUTY CYCLE. It is a single 1x high clock pulse followed by low time until ratio is met. Note: To enable half step ratio dividers user must also set the associated bit in the PLLHDIVEN register PRIOR to writing the PLLDIVn register. If PLLHDIVEN register is not enabled then HALF_RATIO will not be writable. Changing the PLLHDIVEN register, set or clear, will not set or clear the HALF_RATIO bit in PLLDIVn register. This is to protect and enable backward compatible software in the chance it accidentally wrote this bit field.
13-8	RSVD	R/W	0h	Reserved

Table 14-7660. PLLDIV2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RATIO	R/W	X	Divider Dn Ratio (SYSCLKn divider) 00000 = /1 00001 = /2 00010 = /3 00011 = /4 00100 = /5 00101 = 6 00110 = /7 00111 = /8 01000 = /9 01001 = /10 01010 = /11 01011 = /12 01100 = 13 01101 = /14 01110 = /15 01111 = /16 10000 = /17 10001 = /18 10010 = /19 10011 = /20 10100 = /21 10101 = /22 10110 = /23 10111 = /24 11000 = /25 11001 = /26 11010 = /27 11011 = /28 11100 = /29 11101 = /30 11110 = /31 11111 = /32 Note that the actual PLLDIVx divide ratio will not be modified when this field is written to. User must also set the GOSET bit so that the SYSCLKs selected in ALNCTL can change their RATIOs to the new values and remain phase-aligned. Note: see HALF_RATIO bit.

5 PLLCMD Register (Offset = 138h) [reset = 0h]

PLLCMD is shown in Figure 14-2542 and described in Table 14-5121.

Return to the Summary Table.

PLL Controller command register

Table 14-7661. PLLCMD Instances

Instance	Physical Address
PLLCTRL0	0041 0138h
MCU_PLLCTRL0	4020 0138h

Figure 14-2542. PLLCMD Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
RSVD							
R/W-0h							
7	6	5	4	3	2	1	0
RSVD						OSCPWRDN	GOSET
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-7663. PLLCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RSVD	R/W	0h	Reserved
1	OSCPWRDN	R/W	0h	Oscillator Power Down Command 1: A write of 1 (doesn't need to be a transition from 0 to 1) to this bit initiates oscillator power down command. 0: A write of 0 to this bit clears the bit to zero but causes no effect. Read from this field returns the value previously written. Once written a 1, the bit remains a 1 unless if user writes a 0 to it. Do not read this bit for status of oscillator power down. In the case when CLKMODE = 1 (CLKIN mode), write to OSCPWRDN bit still occurs, but no oscillator power down command is actually sent because osc is already in power down. Read from this bit returns the value written.

Table 14-7663. PLLCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GOSET	R/W	0h	GO bit for SYSCLKx phase alignment. GOSET = 1: A write of 1 to this bit signifies that the new divide ratios in PLLDIV [1:n] are taken into account at the nearest possible rising edge to phase align the clocks. The actual SYSCLKx to be aligned are selected in register ALNCTL. When divide-ratio change and clock alignment are completed, GOSET remains 1. Subsequent write of 1 to this register (even though the field was already a 1) causes the command for divide-ratio change and clock alignment. GOSET = 0: A write of 0 to this bit clears the bit to zero but causes no effect. Read from this field returns the value previously written. When writing consecutively to this field, the user must poll the GOSTAT between accesses to see if previous command for clock alignment and divide-ratio change has completed. Otherwise operation is undefined. Do not read GOSET in this command register for status.

6 PLLSTAT Register (Offset = 13Ch) [reset = X]

PLLSTAT is shown in Figure 14-2543 and described in Table 14-5123.

Return to the Summary Table.

PLL Controller status register

Table 14-7664. PLLSTAT Instances

Instance	Physical Address
PLLCTRL0	0041 013Ch
MCU_PLLCTRL0	4020 013Ch

Figure 14-2543. PLLSTAT Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
RSVD							
R/W-0h							
7	6	5	4	3	2	1	0
RSVD					STABLE	LOCK	GOSET
R/W-0h					R-X	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-7666. PLLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RSVD	R/W	0h	Reserved
2	STABLE	R	X	OSCIN Stable This bit shows the status of the rstclk_cnt_done_po signal. It indicates if the rstclk counter has finished counting, implying that the OSCIN/CLKIN is stable. The d_rstclk_cnt_pi must be set properly to allow rstclk counter to count sufficient amount of time for clock sources to become stable. 0 = rstclk counter not done counting, implying OSCIN/CLKIN input may not yet be stable. 1 = OSCIN/CLKIN is assumed to be stable. This bit is set to 1 if any one of the three cases is true: - rstclk counter has finished counting d_rstclk_cnt_pi number of rstclk cycles. - rstclk counter is parametrized out and does not exist, in which case OSCIN/CLKIN is assumed to be stable when por_pi_n is de-asserted.

Table 14-7666. PLLSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LOCK	R	0h	PLL Core STATUS This bit returns the lock status of the selected PLL core (if supported by PLL core). For example, if PLLSELB = 0 (PLLA selected), it reflects the status of pll_a_lock_i. If PLLSELB-1 (PLLB selected), it reflects the status of pll_b_lock_i. 0 = PLL core not locked. The corresponding PLL Controller output pll_[x]_lock_out = 0. (where [x] is a or b depending on PLLSELB). 1 = PLL core locked. The corresponding PLL Controller output pll_[x]_lock_out = 1. (where [x] is a or b depending on PLLSELB). Note that not all PLL Core supports the lock signal. Check the PLL used to see if it has a functional lock output. Therefore this bit may not need to be documented to users.
0	GOSET	R	0h	Reflects the status of GO transition. Read from this register returns the status of the GO operation. Writes to the register are ignored. GOSTAT = 1: This bit goes to 1 as soon as GOSET in PLLCMD is written to. It remains a 1 when GO operation (divide-ratio change and clock alignment) is in progress. This bit automatically clears to 0 when GO operation is completed. GOSTAT = 0: No GO operation in progress. Software note: Users must not initiate another GOSET operation in PLLCMD until GOSTAT is cleared to 0.

7 ALNCTL Register (Offset = 140h) [reset = 3h]

ALNCTL is shown in Figure 14-2544 and described in Table 14-5125.

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PLL Controller clock align control register

Table 14-7667. ALNCTL Instances

Instance	Physical Address
PLLCTRL0	0041 0140h
MCU_PLLCTRL0	4020 0140h

Figure 14-2544. ALNCTL Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ALN</td></tr>
<tr><td colspan="8">R/W-1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">ALN</td><td>ALN1</td></tr>
<tr><td colspan="7">R/W-1h</td><td>R/W-1h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-7669. ALNCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD	R/W	0h	Reserved
15-1	ALN	R/W	1h	SYSCLKx needs to be aligned with other clocks selected in this register. ALNx = 0: Do not need to align SYSCLKx to other clocks. SYSCLKx is left free-running. ALNx = 1: Align SYSCLKx to other clocks selected in this register Software note: This bit should only be modified when GOSTAT is 0. Software note: In the case when a divider is disabled (DxEN = 0) but the respective ALNx = 1, GO operation should ignore ALNx = 1. DxEN takes priority. Existence of ALN [8:3] are determined by RTL parameter SYSCLK. If the corresponding SYSCLK does not exist, the ALNx bit will be read-only and default to 0.
0	ALN1	R/W	1h	SYSCLK1 needs to be aligned with other clocks selected in this register. ALN1 = 0: Do not need to align SYSCLK1 to other clocks. SYSCLK1 is left free-running. ALN1 = 1: Align SYSCLK1 to other clocks selected in this register Software note: This bit should only be modified when GOSTAT is 0. Software note: in the case when a divider is disabled (D1EN = 0) but ALN1 = 1, GO operation should ignore ALN1 = 1. D1EN takes priority.

8 DCHANGE Register (Offset = 144h) [reset = 0h]

DCHANGE is shown in Figure 14-2545 and described in Table 14-5127.

Return to the Summary Table.

PLLDIV ratio change register

Table 14-7670. DCHANGE Instances

Instance	Physical Address
PLLCTRL0	0041 0144h
MCU_PLLCTRL0	4020 0144h

Figure 14-2545. DCHANGE Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
SYS							
R-0h							
7	6	5	4	3	2	1	0
SYS							SYS1
R-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-7672. DCHANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD	R/W	0h	Reserved
15-1	SYS	R	0h	SYSCLKx divide ratio has been modified. SYSCLKx ratio will be changed during GO operation. SYSx = 0: SYSCLKx ratio has not been modified. When GOSET is set, SYSCLKx will not be affected. SYSx = 1: SYSCLKx ratio has been modified. When GOSET is set, SYSCLKx will change to the new ratio.
0	SYS1	R	0h	SYSCLK1 divide ratio has been modified. SYSCLK1 ratio will be changed during GO operation. SYS1 = 0: SYSCLK1 ratio has not been modified. When GOSET is set, SYSCLK1 will not be affected. SYS1 = 1: SYSCLK1 ratio has been modified. When GOSET is set, SYSCLK1 will change to the new ratio.

14.3 Processors and Accelerators Registers

14.3.1 A53SS Registers

14.3.1.1 A53SS

A53SS

14.3.1.1.1 A53SS Summaries

A53SS Summaries

Table 14-7673. ECC_AGGR Registers, Base Address=0071 7000h, Length=1024

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	ECC_AGGR_REV	0071 7000h
8h	32	ECC_AGGR_VECTOR	0071 7008h
Ch	32	ECC_AGGR_STAT	0071 700Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 7010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 703Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 7040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 7080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 70C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 713Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 7140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 7180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 71C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 7200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 7204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 7208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 720Ch

Table 14-7674. ECC_AGGR Registers, Base Address=0071 7400h, Length=1024

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	ECC_AGGR_REV	0071 7400h
8h	32	ECC_AGGR_VECTOR	0071 7408h
Ch	32	ECC_AGGR_STAT	0071 740Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 7410h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 743Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 7440h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 7480h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 74C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 753Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 7540h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 7580h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 75C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 7600h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 7604h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 7608h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 760Ch

Table 14-7675. ECC_AGGR Registers, Base Address=0071 7800h, Length=1024

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	ECC_AGGR_REV	0071 7800h
8h	32	ECC_AGGR_VECTOR	0071 7808h
Ch	32	ECC_AGGR_STAT	0071 780Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 7810h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 783Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 7840h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 7880h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 78C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 793Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 7940h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 7980h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 79C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 7A00h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 7A04h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 7A08h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 7A0Ch

Table 14-7676. A53SS_APBADDR_ROMV8 Registers, Base Address=0007 3000 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_APBADDR_ROMV8_ROMENTRY0	0007 3000 0000h
4h	32	A53SS_APBADDR_ROMV8_ROMENTRY1	0007 3000 0004h
8h	32	A53SS_APBADDR_ROMV8_ROMENTRY2	0007 3000 0008h
Ch	32	A53SS_APBADDR_ROMV8_ROMENTRY3	0007 3000 000Ch
10h	32	A53SS_APBADDR_ROMV8_ROMENTRY4	0007 3000 0010h
14h	32	A53SS_APBADDR_ROMV8_ROMENTRY5	0007 3000 0014h
18h	32	A53SS_APBADDR_ROMV8_ROMENTRY6	0007 3000 0018h
1Ch	32	A53SS_APBADDR_ROMV8_ROMENTRY7	0007 3000 001Ch
FD0h	32	A53SS_APBADDR_ROMV8_ROM_PERIPHID4_VAL	0007 3000 0FD0h
FD4h	32	A53SS_APBADDR_ROMV8_ROM_PERIPHID5_VAL	0007 3000 0FD4h
FD8h	32	A53SS_APBADDR_ROMV8_ROM_PERIPHID6_VAL	0007 3000 0FD8h
FDCh	32	A53SS_APBADDR_ROMV8_ROM_PERIPHID7_VAL	0007 3000 0FDCh
FE0h	32	A53SS_APBADDR_ROMV8_ROM_PERIPHID0_VAL	0007 3000 0FE0h
FE4h	32	A53SS_APBADDR_ROMV8_ROM_PERIPHID1_VAL	0007 3000 0FE4h
FE8h	32	A53SS_APBADDR_ROMV8_ROM_PERIPHID2_VAL	0007 3000 0FE8h
FECh	32	A53SS_APBADDR_ROMV8_ROM_PERIPHID3_VAL	0007 3000 0FECh
FF0h	32	A53SS_APBADDR_ROMV8_ROM_COMPONID0_VAL	0007 3000 0FF0h
FF4h	32	A53SS_APBADDR_ROMV8_ROM_COMPONID1_VAL	0007 3000 0FF4h
FF8h	32	A53SS_APBADDR_ROMV8_ROM_COMPONID2_VAL	0007 3000 0FF8h
FFCh	32	A53SS_APBADDR_ROMV8_ROM_COMPONID3_VAL	0007 3000 0FFCh

Table 14-7677. A53SS_APBADDR_DBG_CPU0 Registers, Base Address=0007 3001 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
20h	32	A53SS_APBADDR_DBG_CPU0_EDESR	0007 3001 0020h
24h	32	A53SS_APBADDR_DBG_CPU0_EDECR	0007 3001 0024h

Table 14-7677. A53SS_APBADDR_DBG_CPU0 Registers, Base Address=0007 3001 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
30h	32	A53SS_APBADDR_DBG_CPU0_EDWAR_31_0	0007 3001 0030h
34h	32	A53SS_APBADDR_DBG_CPU0_EDWAR_63_32	0007 3001 0034h
80h	32	A53SS_APBADDR_DBG_CPU0_DBGDTRRX_EL0	0007 3001 0080h
84h	32	A53SS_APBADDR_DBG_CPU0_EDITR	0007 3001 0084h
88h	32	A53SS_APBADDR_DBG_CPU0_EDSCR	0007 3001 0088h
8Ch	32	A53SS_APBADDR_DBG_CPU0_DBGDTRTX_EL0	0007 3001 008Ch
90h	32	A53SS_APBADDR_DBG_CPU0_EDRCR	0007 3001 0090h
94h	32	A53SS_APBADDR_DBG_CPU0_EDACR	0007 3001 0094h
98h	32	A53SS_APBADDR_DBG_CPU0_EDECCR	0007 3001 0098h
A0h	32	A53SS_APBADDR_DBG_CPU0_EDPCSR_31_0	0007 3001 00A0h
A4h	32	A53SS_APBADDR_DBG_CPU0_EDCIDSR	0007 3001 00A4h
A8h	32	A53SS_APBADDR_DBG_CPU0_EDVIDSR	0007 3001 00A8h
ACh	32	A53SS_APBADDR_DBG_CPU0_EDPCSR_63_32	0007 3001 00ACh
300h	32	A53SS_APBADDR_DBG_CPU0_OSLAR_EL1	0007 3001 0300h
310h	32	A53SS_APBADDR_DBG_CPU0_EDPRCR	0007 3001 0310h
314h	32	A53SS_APBADDR_DBG_CPU0_EDPRSR	0007 3001 0314h
400h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_31_0	0007 3001 0400h
404h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_63_32	0007 3001 0404h
408h	32	A53SS_APBADDR_DBG_CPU0_DBGBCR0_EL1	0007 3001 0408h
410h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_31_0	0007 3001 0410h
414h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_63_32	0007 3001 0414h
418h	32	A53SS_APBADDR_DBG_CPU0_DBGBCR1_EL1	0007 3001 0418h
420h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_31_0	0007 3001 0420h
424h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_63_32	0007 3001 0424h
428h	32	A53SS_APBADDR_DBG_CPU0_DBGBCR2_EL1	0007 3001 0428h
430h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_31_0	0007 3001 0430h
434h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_63_32	0007 3001 0434h
438h	32	A53SS_APBADDR_DBG_CPU0_DBGBCR3_EL1	0007 3001 0438h
440h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_31_0	0007 3001 0440h
444h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_63_32	0007 3001 0444h
448h	32	A53SS_APBADDR_DBG_CPU0_DBGBCR4_EL1	0007 3001 0448h
450h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_31_0	0007 3001 0450h
454h	32	A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_63_32	0007 3001 0454h
458h	32	A53SS_APBADDR_DBG_CPU0_DBGBCR5_EL1	0007 3001 0458h
800h	32	A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_31_0	0007 3001 0800h
804h	32	A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_63_32	0007 3001 0804h
808h	32	A53SS_APBADDR_DBG_CPU0_DBGWCR0_EL1	0007 3001 0808h
810h	32	A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_31_0	0007 3001 0810h
814h	32	A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_63_32	0007 3001 0814h
818h	32	A53SS_APBADDR_DBG_CPU0_DBGWCR1_EL1	0007 3001 0818h
820h	32	A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_31_0	0007 3001 0820h
824h	32	A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_63_32	0007 3001 0824h
828h	32	A53SS_APBADDR_DBG_CPU0_DBGWCR2_EL1	0007 3001 0828h
830h	32	A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_31_0	0007 3001 0830h

Table 14-7677. A53SS_APBADDR_DBG_CPU0 Registers, Base Address=0007 3001 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
834h	32	A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_63_32	0007 3001 0834h
838h	32	A53SS_APBADDR_DBG_CPU0_DBGWCR3_EL1	0007 3001 0838h
D00h	32	A53SS_APBADDR_DBG_CPU0_MIDR_EL1	0007 3001 0D00h
D20h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_31_0	0007 3001 0D20h
D24h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_63_32	0007 3001 0D24h
D28h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_31_0	0007 3001 0D28h
D2Ch	32	A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_63_32	0007 3001 0D2Ch
D30h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_31_0	0007 3001 0D30h
D34h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_63_32	0007 3001 0D34h
D38h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_31_0	0007 3001 0D38h
D3Ch	32	A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_63_32	0007 3001 0D3Ch
D40h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_31_0	0007 3001 0D40h
D44h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_63_32	0007 3001 0D44h
D48h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_31_0	0007 3001 0D48h
D4Ch	32	A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_63_32	0007 3001 0D4Ch
D50h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_31_0	0007 3001 0D50h
D54h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_63_32	0007 3001 0D54h
D58h	32	A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_31_0	0007 3001 0D58h
D5Ch	32	A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_63_32	0007 3001 0D5Ch
F00h	32	A53SS_APBADDR_DBG_CPU0_EDITCTRL	0007 3001 0F00h
FA0h	32	A53SS_APBADDR_DBG_CPU0_DBGCLAIMSET_EL1	0007 3001 0FA0h
FA4h	32	A53SS_APBADDR_DBG_CPU0_DBGCLAIMCLR_EL1	0007 3001 0FA4h
FA8h	32	A53SS_APBADDR_DBG_CPU0_EDDEVAFF0	0007 3001 0FA8h
FACh	32	A53SS_APBADDR_DBG_CPU0_EDDEVAFF1	0007 3001 0FACh
FB0h	32	A53SS_APBADDR_DBG_CPU0_EDLAR	0007 3001 0FB0h
FB4h	32	A53SS_APBADDR_DBG_CPU0_EDLSR	0007 3001 0FB4h
FB8h	32	A53SS_APBADDR_DBG_CPU0_DBGAUTHSTATUS_EL1	0007 3001 0FB8h
FBCh	32	A53SS_APBADDR_DBG_CPU0_EDDEVARCH	0007 3001 0FBCh
FC0h	32	A53SS_APBADDR_DBG_CPU0_EDDEVID2	0007 3001 0FC0h
FC4h	32	A53SS_APBADDR_DBG_CPU0_EDDEVID1	0007 3001 0FC4h
FC8h	32	A53SS_APBADDR_DBG_CPU0_EDDEVID	0007 3001 0FC8h
FCCh	32	A53SS_APBADDR_DBG_CPU0_EDDEVTYPE	0007 3001 0FCCh
FD0h	32	A53SS_APBADDR_DBG_CPU0_EDPIDR4	0007 3001 0FD0h

Table 14-7677. A53SS_APBADDR_DBG_CPU0 Registers, Base Address=0007 3001 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FE0h	32	A53SS_APBADDR_DBG_CPU0_EDPIDR0	0007 3001 0FE0h
FE4h	32	A53SS_APBADDR_DBG_CPU0_EDPIDR1	0007 3001 0FE4h
FE8h	32	A53SS_APBADDR_DBG_CPU0_EDPIDR2	0007 3001 0FE8h
FECh	32	A53SS_APBADDR_DBG_CPU0_EDPIDR3	0007 3001 0FECh
FF0h	32	A53SS_APBADDR_DBG_CPU0_EDCIDR0	0007 3001 0FF0h
FF4h	32	A53SS_APBADDR_DBG_CPU0_EDCIDR1	0007 3001 0FF4h
FF8h	32	A53SS_APBADDR_DBG_CPU0_EDCIDR2	0007 3001 0FF8h
FFCh	32	A53SS_APBADDR_DBG_CPU0_EDCIDR3	0007 3001 0FFCh

Table 14-7678. A53SS_APBADDR_CTI_CPU0 Registers, Base Address=0007 3002 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_APBADDR_CTI_CPU0_CTICONTROL	0007 3002 0000h
10h	32	A53SS_APBADDR_CTI_CPU0_CTIINTACK	0007 3002 0010h
14h	32	A53SS_APBADDR_CTI_CPU0_CTIAPPSET	0007 3002 0014h
18h	32	A53SS_APBADDR_CTI_CPU0_CTIAPPCLEAR	0007 3002 0018h
1Ch	32	A53SS_APBADDR_CTI_CPU0_CTIAPPPULSE	0007 3002 001Ch
20h	32	A53SS_APBADDR_CTI_CPU0_CTIINEN0	0007 3002 0020h
24h	32	A53SS_APBADDR_CTI_CPU0_CTIINEN1	0007 3002 0024h
28h	32	A53SS_APBADDR_CTI_CPU0_CTIINEN2	0007 3002 0028h
2Ch	32	A53SS_APBADDR_CTI_CPU0_CTIINEN3	0007 3002 002Ch
30h	32	A53SS_APBADDR_CTI_CPU0_CTIINEN4	0007 3002 0030h
34h	32	A53SS_APBADDR_CTI_CPU0_CTIINEN5	0007 3002 0034h
38h	32	A53SS_APBADDR_CTI_CPU0_CTIINEN6	0007 3002 0038h
3Ch	32	A53SS_APBADDR_CTI_CPU0_CTIINEN7	0007 3002 003Ch
A0h	32	A53SS_APBADDR_CTI_CPU0_CTIOUTEN0	0007 3002 00A0h
A4h	32	A53SS_APBADDR_CTI_CPU0_CTIOUTEN1	0007 3002 00A4h
A8h	32	A53SS_APBADDR_CTI_CPU0_CTIOUTEN2	0007 3002 00A8h
ACh	32	A53SS_APBADDR_CTI_CPU0_CTIOUTEN3	0007 3002 00ACh
B0h	32	A53SS_APBADDR_CTI_CPU0_CTIOUTEN4	0007 3002 00B0h
B4h	32	A53SS_APBADDR_CTI_CPU0_CTIOUTEN5	0007 3002 00B4h
B8h	32	A53SS_APBADDR_CTI_CPU0_CTIOUTEN6	0007 3002 00B8h
BCh	32	A53SS_APBADDR_CTI_CPU0_CTIOUTEN7	0007 3002 00BCh
130h	32	A53SS_APBADDR_CTI_CPU0_CTITRIGINSTATUS	0007 3002 0130h
134h	32	A53SS_APBADDR_CTI_CPU0_CTITRIGOUTSTATUS	0007 3002 0134h
138h	32	A53SS_APBADDR_CTI_CPU0_CTICHINSTATUS	0007 3002 0138h
13Ch	32	A53SS_APBADDR_CTI_CPU0_CTICHOUTSTATUS	0007 3002 013Ch
140h	32	A53SS_APBADDR_CTI_CPU0_CTIGATE	0007 3002 0140h
144h	32	A53SS_APBADDR_CTI_CPU0_ASICCTL	0007 3002 0144h
F00h	32	A53SS_APBADDR_CTI_CPU0_CTIITCTRL	0007 3002 0F00h
FA0h	32	A53SS_APBADDR_CTI_CPU0_CTICLAIMSET	0007 3002 0FA0h
FA4h	32	A53SS_APBADDR_CTI_CPU0_CTICLAIMCLR	0007 3002 0FA4h
FA8h	32	A53SS_APBADDR_CTI_CPU0_CTIDEVAFF0	0007 3002 0FA8h
FACh	32	A53SS_APBADDR_CTI_CPU0_CTIDEVAFF1	0007 3002 0FACh
FB0h	32	A53SS_APBADDR_CTI_CPU0_CTILAR	0007 3002 0FB0h

Table 14-7678. A53SS_APBADDR_CTI_CPU0 Registers, Base Address=0007 3002 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FB4h	32	A53SS_APBADDR_CTI_CPU0_CTILSR	0007 3002 0FB4h
FB8h	32	A53SS_APBADDR_CTI_CPU0_CTIAUTHSTATUS	0007 3002 0FB8h
FBCh	32	A53SS_APBADDR_CTI_CPU0_CTIDEVARCH	0007 3002 0FBCh
FC0h	32	A53SS_APBADDR_CTI_CPU0_CTIDEVID2	0007 3002 0FC0h
FC4h	32	A53SS_APBADDR_CTI_CPU0_CTIDEVID1	0007 3002 0FC4h
FC8h	32	A53SS_APBADDR_CTI_CPU0_CTIDEVID	0007 3002 0FC8h
FCCh	32	A53SS_APBADDR_CTI_CPU0_CTIDEVTYPE	0007 3002 0FCCh
FD0h	32	A53SS_APBADDR_CTI_CPU0_CTIPIDR4	0007 3002 0FD0h
FD4h	32	A53SS_APBADDR_CTI_CPU0_CTIPIDR5	0007 3002 0FD4h
FD8h	32	A53SS_APBADDR_CTI_CPU0_CTIPIDR6	0007 3002 0FD8h
FDCh	32	A53SS_APBADDR_CTI_CPU0_CTIPIDR7	0007 3002 0FDCh
FE0h	32	A53SS_APBADDR_CTI_CPU0_CTIPIDR0	0007 3002 0FE0h
FE4h	32	A53SS_APBADDR_CTI_CPU0_CTIPIDR1	0007 3002 0FE4h
FE8h	32	A53SS_APBADDR_CTI_CPU0_CTIPIDR2	0007 3002 0FE8h
FECh	32	A53SS_APBADDR_CTI_CPU0_CTIPIDR3	0007 3002 0FECh
FF0h	32	A53SS_APBADDR_CTI_CPU0_CTICIDR0	0007 3002 0FF0h
FF4h	32	A53SS_APBADDR_CTI_CPU0_CTICIDR1	0007 3002 0FF4h
FF8h	32	A53SS_APBADDR_CTI_CPU0_CTICIDR2	0007 3002 0FF8h
FFCh	32	A53SS_APBADDR_CTI_CPU0_CTICIDR3	0007 3002 0FFCh

Table 14-7679. A53SS_APBADDR_PMU_CPU0 Registers, Base Address=0007 3003 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_APBADDR_PMU_CPU0_PMEVCNTR0_EL0	0007 3003 0000h
8h	32	A53SS_APBADDR_PMU_CPU0_PMEVCNTR1_EL0	0007 3003 0008h
10h	32	A53SS_APBADDR_PMU_CPU0_PMEVCNTR2_EL0	0007 3003 0010h
18h	32	A53SS_APBADDR_PMU_CPU0_PMEVCNTR3_EL0	0007 3003 0018h
20h	32	A53SS_APBADDR_PMU_CPU0_PMEVCNTR4_EL0	0007 3003 0020h
28h	32	A53SS_APBADDR_PMU_CPU0_PMEVCNTR5_EL0	0007 3003 0028h
F8h	32	A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_31_0	0007 3003 00F8h
FCh	32	A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_63_32	0007 3003 00FCh
400h	32	A53SS_APBADDR_PMU_CPU0_PMEVTYPER0_EL0	0007 3003 0400h
404h	32	A53SS_APBADDR_PMU_CPU0_PMEVTYPER1_EL0	0007 3003 0404h
408h	32	A53SS_APBADDR_PMU_CPU0_PMEVTYPER2_EL0	0007 3003 0408h
40Ch	32	A53SS_APBADDR_PMU_CPU0_PMEVTYPER3_EL0	0007 3003 040Ch
410h	32	A53SS_APBADDR_PMU_CPU0_PMEVTYPER4_EL0	0007 3003 0410h
414h	32	A53SS_APBADDR_PMU_CPU0_PMEVTYPER5_EL0	0007 3003 0414h
47Ch	32	A53SS_APBADDR_PMU_CPU0_PMCCFILTR_EL0	0007 3003 047Ch
C00h	32	A53SS_APBADDR_PMU_CPU0_PMCNTENSET_EL0	0007 3003 0C00h
C20h	32	A53SS_APBADDR_PMU_CPU0_PMCNTENCLR_EL0	0007 3003 0C20h
C40h	32	A53SS_APBADDR_PMU_CPU0_PMINTENSET_EL1	0007 3003 0C40h
C60h	32	A53SS_APBADDR_PMU_CPU0_PMINTENCLR_EL1	0007 3003 0C60h
C80h	32	A53SS_APBADDR_PMU_CPU0_PMOVSCLR_EL0	0007 3003 0C80h
CA0h	32	A53SS_APBADDR_PMU_CPU0_PMSWINC_EL0	0007 3003 0CA0h
CC0h	32	A53SS_APBADDR_PMU_CPU0_PMOVSSET_EL0	0007 3003 0CC0h

Table 14-7679. A53SS_APBADDR_PMU_CPU0 Registers, Base Address=0007 3003 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
E00h	32	A53SS_APBADDR_PMU_CPU0_PMCFGR	0007 3003 0E00h
E04h	32	A53SS_APBADDR_PMU_CPU0_PMCR_EL0	0007 3003 0E04h
E20h	32	A53SS_APBADDR_PMU_CPU0_PMCEID0_EL0	0007 3003 0E20h
E24h	32	A53SS_APBADDR_PMU_CPU0_PMCEID1_EL0	0007 3003 0E24h
F00h	32	A53SS_APBADDR_PMU_CPU0_PMITCTRL	0007 3003 0F00h
FA8h	32	A53SS_APBADDR_PMU_CPU0_PMDEVAFF0	0007 3003 0FA8h
FACh	32	A53SS_APBADDR_PMU_CPU0_PMDEVAFF1	0007 3003 0FACh
FB0h	32	A53SS_APBADDR_PMU_CPU0_PMLAR	0007 3003 0FB0h
FB4h	32	A53SS_APBADDR_PMU_CPU0_PMLSR	0007 3003 0FB4h
FB8h	32	A53SS_APBADDR_PMU_CPU0_PMAUTHSTATUS	0007 3003 0FB8h
FBCh	32	A53SS_APBADDR_PMU_CPU0_PMDEVARCH	0007 3003 0FBCh
FCCh	32	A53SS_APBADDR_PMU_CPU0_PMDEVTYPE	0007 3003 0FCCh
FD0h	32	A53SS_APBADDR_PMU_CPU0_PMPIDR4	0007 3003 0FD0h
FD4h	32	A53SS_APBADDR_PMU_CPU0_PMPIDR5	0007 3003 0FD4h
FD8h	32	A53SS_APBADDR_PMU_CPU0_PMPIDR6	0007 3003 0FD8h
FDCh	32	A53SS_APBADDR_PMU_CPU0_PMPIDR7	0007 3003 0FDCh
FE0h	32	A53SS_APBADDR_PMU_CPU0_PMPIDR0	0007 3003 0FE0h
FE4h	32	A53SS_APBADDR_PMU_CPU0_PMPIDR1	0007 3003 0FE4h
FE8h	32	A53SS_APBADDR_PMU_CPU0_PMPIDR2	0007 3003 0FE8h
FECh	32	A53SS_APBADDR_PMU_CPU0_PMPIDR3	0007 3003 0FECh
FF0h	32	A53SS_APBADDR_PMU_CPU0_PMCIDR0	0007 3003 0FF0h
FF4h	32	A53SS_APBADDR_PMU_CPU0_PMCIDR1	0007 3003 0FF4h
FF8h	32	A53SS_APBADDR_PMU_CPU0_PMCIDR2	0007 3003 0FF8h
FFCh	32	A53SS_APBADDR_PMU_CPU0_PMCIDR3	0007 3003 0FFCh

Table 14-7680. A53SS_APBADDR_ETM_CPU0 Registers, Base Address=0007 3004 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
4h	32	A53SS_APBADDR_ETM_CPU0_TRCPRGCTLR	0007 3004 0004h
Ch	32	A53SS_APBADDR_ETM_CPU0_TRCSTATR	0007 3004 000Ch
10h	32	A53SS_APBADDR_ETM_CPU0_TRCCONFIGR	0007 3004 0010h
18h	32	A53SS_APBADDR_ETM_CPU0_TRCAUXCTLR	0007 3004 0018h
20h	32	A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL0R	0007 3004 0020h
24h	32	A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL1R	0007 3004 0024h
2Ch	32	A53SS_APBADDR_ETM_CPU0_TRCSTALLCTLR	0007 3004 002Ch
30h	32	A53SS_APBADDR_ETM_CPU0_TRCTSCTLR	0007 3004 0030h
34h	32	A53SS_APBADDR_ETM_CPU0_TRCSYNCPR	0007 3004 0034h
38h	32	A53SS_APBADDR_ETM_CPU0_TRCCCCTLR	0007 3004 0038h
3Ch	32	A53SS_APBADDR_ETM_CPU0_TRCBBCTLR	0007 3004 003Ch
40h	32	A53SS_APBADDR_ETM_CPU0_TRCTRACEIDR	0007 3004 0040h
80h	32	A53SS_APBADDR_ETM_CPU0_TRCVICTLR	0007 3004 0080h
84h	32	A53SS_APBADDR_ETM_CPU0_TRCVIIECTLR	0007 3004 0084h
88h	32	A53SS_APBADDR_ETM_CPU0_TRCVISSCTLR	0007 3004 0088h
100h	32	A53SS_APBADDR_ETM_CPU0_TRCSEQEVR0	0007 3004 0100h
104h	32	A53SS_APBADDR_ETM_CPU0_TRCSEQEVR1	0007 3004 0104h

Table 14-7680. A53SS_APBADDR_ETM_CPU0 Registers, Base Address=0007 3004 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
108h	32	A53SS_APBADDR_ETM_CPU0_TRCSEQEVR2	0007 3004 0108h
118h	32	A53SS_APBADDR_ETM_CPU0_TRCSEQRSTEVR	0007 3004 0118h
11Ch	32	A53SS_APBADDR_ETM_CPU0_TRCSEQSTR	0007 3004 011Ch
120h	32	A53SS_APBADDR_ETM_CPU0_TRCEXTINSELR	0007 3004 0120h
140h	32	A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR0	0007 3004 0140h
144h	32	A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR1	0007 3004 0144h
150h	32	A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR0	0007 3004 0150h
154h	32	A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR1	0007 3004 0154h
160h	32	A53SS_APBADDR_ETM_CPU0_TRCCNTVR0	0007 3004 0160h
164h	32	A53SS_APBADDR_ETM_CPU0_TRCCNTVR1	0007 3004 0164h
180h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR8	0007 3004 0180h
184h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR9	0007 3004 0184h
188h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR10	0007 3004 0188h
18Ch	32	A53SS_APBADDR_ETM_CPU0_TRCIDR11	0007 3004 018Ch
190h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR12	0007 3004 0190h
194h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR13	0007 3004 0194h
1C0h	32	A53SS_APBADDR_ETM_CPU0_TRCIMSPEC0	0007 3004 01C0h
1E0h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR0	0007 3004 01E0h
1E4h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR1	0007 3004 01E4h
1E8h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR2	0007 3004 01E8h
1ECh	32	A53SS_APBADDR_ETM_CPU0_TRCIDR3	0007 3004 01ECh
1F0h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR4	0007 3004 01F0h
1F4h	32	A53SS_APBADDR_ETM_CPU0_TRCIDR5	0007 3004 01F4h
208h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR2	0007 3004 0208h
20Ch	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR3	0007 3004 020Ch
210h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR4	0007 3004 0210h
214h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR5	0007 3004 0214h
218h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR6	0007 3004 0218h
21Ch	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR7	0007 3004 021Ch
220h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR8	0007 3004 0220h
224h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR9	0007 3004 0224h
228h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR10	0007 3004 0228h
22Ch	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR11	0007 3004 022Ch
230h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR12	0007 3004 0230h
234h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR13	0007 3004 0234h
238h	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR14	0007 3004 0238h
23Ch	32	A53SS_APBADDR_ETM_CPU0_TRCRSCTLR15	0007 3004 023Ch
280h	32	A53SS_APBADDR_ETM_CPU0_TRCSSCCR0	0007 3004 0280h
2A0h	32	A53SS_APBADDR_ETM_CPU0_TRCSSCSR0	0007 3004 02A0h
300h	32	A53SS_APBADDR_ETM_CPU0_TRCOSLAR	0007 3004 0300h
304h	32	A53SS_APBADDR_ETM_CPU0_TRCOSLSR	0007 3004 0304h
310h	32	A53SS_APBADDR_ETM_CPU0_TRCPDCR	0007 3004 0310h
314h	32	A53SS_APBADDR_ETM_CPU0_TRCPDSR	0007 3004 0314h
400h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR0_31_0	0007 3004 0400h

Table 14-7680. A53SS_APBADDR_ETM_CPU0 Registers, Base Address=0007 3004 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
404h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR0_63_32	0007 3004 0404h
408h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR1_31_0	0007 3004 0408h
40Ch	32	A53SS_APBADDR_ETM_CPU0_TRCACVR1_63_32	0007 3004 040Ch
410h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR2_31_0	0007 3004 0410h
414h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR2_63_32	0007 3004 0414h
418h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR3_31_0	0007 3004 0418h
41Ch	32	A53SS_APBADDR_ETM_CPU0_TRCACVR3_63_32	0007 3004 041Ch
420h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR4_31_0	0007 3004 0420h
424h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR4_63_32	0007 3004 0424h
428h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR5_31_0	0007 3004 0428h
42Ch	32	A53SS_APBADDR_ETM_CPU0_TRCACVR5_63_32	0007 3004 042Ch
430h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR6_31_0	0007 3004 0430h
434h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR6_63_32	0007 3004 0434h
438h	32	A53SS_APBADDR_ETM_CPU0_TRCACVR7_31_0	0007 3004 0438h
43Ch	32	A53SS_APBADDR_ETM_CPU0_TRCACVR7_63_32	0007 3004 043Ch
480h	32	A53SS_APBADDR_ETM_CPU0_TRCACATR0	0007 3004 0480h
488h	32	A53SS_APBADDR_ETM_CPU0_TRCACATR1	0007 3004 0488h
490h	32	A53SS_APBADDR_ETM_CPU0_TRCACATR2	0007 3004 0490h
498h	32	A53SS_APBADDR_ETM_CPU0_TRCACATR3	0007 3004 0498h
4A0h	32	A53SS_APBADDR_ETM_CPU0_TRCACATR4	0007 3004 04A0h
4A8h	32	A53SS_APBADDR_ETM_CPU0_TRCACATR5	0007 3004 04A8h
4B0h	32	A53SS_APBADDR_ETM_CPU0_TRCACATR6	0007 3004 04B0h
4B8h	32	A53SS_APBADDR_ETM_CPU0_TRCACATR7	0007 3004 04B8h
600h	32	A53SS_APBADDR_ETM_CPU0_TRCCIDCVR0	0007 3004 0600h
640h	32	A53SS_APBADDR_ETM_CPU0_TRCVMIDCVR0	0007 3004 0640h
680h	32	A53SS_APBADDR_ETM_CPU0_TRCCIDCCTLR0	0007 3004 0680h
EE4h	32	A53SS_APBADDR_ETM_CPU0_TRCITATBIDR	0007 3004 0EE4h
EECh	32	A53SS_APBADDR_ETM_CPU0_TRCITIDATAR	0007 3004 0EECh
EF4h	32	A53SS_APBADDR_ETM_CPU0_TRCITIATBINR	0007 3004 0EF4h
EFCh	32	A53SS_APBADDR_ETM_CPU0_TRCITIATBOUTR	0007 3004 0EFCh
F00h	32	A53SS_APBADDR_ETM_CPU0_TRCITCTRL	0007 3004 0F00h
FA0h	32	A53SS_APBADDR_ETM_CPU0_TRCCLAIMSET	0007 3004 0FA0h
FA4h	32	A53SS_APBADDR_ETM_CPU0_TRCCLAIMCLR	0007 3004 0FA4h
FA8h	32	A53SS_APBADDR_ETM_CPU0_TRCDEVAFF0	0007 3004 0FA8h
FACh	32	A53SS_APBADDR_ETM_CPU0_TRCDEVAFF1	0007 3004 0FACh
FB0h	32	A53SS_APBADDR_ETM_CPU0_TRCLAR	0007 3004 0FB0h
FB4h	32	A53SS_APBADDR_ETM_CPU0_TRCLSR	0007 3004 0FB4h
FB8h	32	A53SS_APBADDR_ETM_CPU0_TRCAUTHSTATUS	0007 3004 0FB8h
FBCh	32	A53SS_APBADDR_ETM_CPU0_TRCDEVARCH	0007 3004 0FBCh
FC8h	32	A53SS_APBADDR_ETM_CPU0_TRCDEVID	0007 3004 0FC8h
FCCh	32	A53SS_APBADDR_ETM_CPU0_TRCDEVTYPE	0007 3004 0FCCh
FD0h	32	A53SS_APBADDR_ETM_CPU0_TRCPIDR4	0007 3004 0FD0h
FD4h	32	A53SS_APBADDR_ETM_CPU0_TRCPIDR5	0007 3004 0FD4h
FD8h	32	A53SS_APBADDR_ETM_CPU0_TRCPIDR6	0007 3004 0FD8h

Table 14-7680. A53SS_APBADDR_ETM_CPU0 Registers, Base Address=0007 3004 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FDCh	32	A53SS_APBADDR_ETM_CPU0_TRCPIDR7	0007 3004 0FDCh
FE0h	32	A53SS_APBADDR_ETM_CPU0_TRCPIDR0	0007 3004 0FE0h
FE4h	32	A53SS_APBADDR_ETM_CPU0_TRCPIDR1	0007 3004 0FE4h
FE8h	32	A53SS_APBADDR_ETM_CPU0_TRCPIDR2	0007 3004 0FE8h
FECh	32	A53SS_APBADDR_ETM_CPU0_TRCPIDR3	0007 3004 0FECh
FF0h	32	A53SS_APBADDR_ETM_CPU0_TRCCIDR0	0007 3004 0FF0h
FF4h	32	A53SS_APBADDR_ETM_CPU0_TRCCIDR1	0007 3004 0FF4h
FF8h	32	A53SS_APBADDR_ETM_CPU0_TRCCIDR2	0007 3004 0FF8h
FFCh	32	A53SS_APBADDR_ETM_CPU0_TRCCIDR3	0007 3004 0FFCh

Table 14-7681. A53SS_APBADDR_DBG_CPU1 Registers, Base Address=0007 3011 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
20h	32	A53SS_APBADDR_DBG_CPU1_EDESR	0007 3011 0020h
24h	32	A53SS_APBADDR_DBG_CPU1_EDECR	0007 3011 0024h
30h	32	A53SS_APBADDR_DBG_CPU1_EDWAR_31_0	0007 3011 0030h
34h	32	A53SS_APBADDR_DBG_CPU1_EDWAR_63_32	0007 3011 0034h
80h	32	A53SS_APBADDR_DBG_CPU1_DBGDTRRX_EL0	0007 3011 0080h
84h	32	A53SS_APBADDR_DBG_CPU1_EDITR	0007 3011 0084h
88h	32	A53SS_APBADDR_DBG_CPU1_EDSCR	0007 3011 0088h
8Ch	32	A53SS_APBADDR_DBG_CPU1_DBGDTRTX_EL0	0007 3011 008Ch
90h	32	A53SS_APBADDR_DBG_CPU1_EDRCR	0007 3011 0090h
94h	32	A53SS_APBADDR_DBG_CPU1_EDACR	0007 3011 0094h
98h	32	A53SS_APBADDR_DBG_CPU1_EDECCR	0007 3011 0098h
A0h	32	A53SS_APBADDR_DBG_CPU1_EDPCSR_31_0	0007 3011 00A0h
A4h	32	A53SS_APBADDR_DBG_CPU1_EDCIDSR	0007 3011 00A4h
A8h	32	A53SS_APBADDR_DBG_CPU1_EDVIDSR	0007 3011 00A8h
ACh	32	A53SS_APBADDR_DBG_CPU1_EDPCSR_63_32	0007 3011 00ACh
300h	32	A53SS_APBADDR_DBG_CPU1_OSLAR_EL1	0007 3011 0300h
310h	32	A53SS_APBADDR_DBG_CPU1_EDPRCR	0007 3011 0310h
314h	32	A53SS_APBADDR_DBG_CPU1_EDPRSR	0007 3011 0314h
400h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_31_0	0007 3011 0400h
404h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_63_32	0007 3011 0404h
408h	32	A53SS_APBADDR_DBG_CPU1_DBGBCR0_EL1	0007 3011 0408h
410h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_31_0	0007 3011 0410h
414h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_63_32	0007 3011 0414h
418h	32	A53SS_APBADDR_DBG_CPU1_DBGBCR1_EL1	0007 3011 0418h
420h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_31_0	0007 3011 0420h
424h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_63_32	0007 3011 0424h
428h	32	A53SS_APBADDR_DBG_CPU1_DBGBCR2_EL1	0007 3011 0428h
430h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_31_0	0007 3011 0430h
434h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_63_32	0007 3011 0434h
438h	32	A53SS_APBADDR_DBG_CPU1_DBGBCR3_EL1	0007 3011 0438h
440h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_31_0	0007 3011 0440h
444h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_63_32	0007 3011 0444h

Table 14-7681. A53SS_APBADDR_DBG_CPU1 Registers, Base Address=0007 3011 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
448h	32	A53SS_APBADDR_DBG_CPU1_DBGBCR4_EL1	0007 3011 0448h
450h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_31_0	0007 3011 0450h
454h	32	A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_63_32	0007 3011 0454h
458h	32	A53SS_APBADDR_DBG_CPU1_DBGBCR5_EL1	0007 3011 0458h
800h	32	A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_31_0	0007 3011 0800h
804h	32	A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_63_32	0007 3011 0804h
808h	32	A53SS_APBADDR_DBG_CPU1_DBGWCR0_EL1	0007 3011 0808h
810h	32	A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_31_0	0007 3011 0810h
814h	32	A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_63_32	0007 3011 0814h
818h	32	A53SS_APBADDR_DBG_CPU1_DBGWCR1_EL1	0007 3011 0818h
820h	32	A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_31_0	0007 3011 0820h
824h	32	A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_63_32	0007 3011 0824h
828h	32	A53SS_APBADDR_DBG_CPU1_DBGWCR2_EL1	0007 3011 0828h
830h	32	A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_31_0	0007 3011 0830h
834h	32	A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_63_32	0007 3011 0834h
838h	32	A53SS_APBADDR_DBG_CPU1_DBGWCR3_EL1	0007 3011 0838h
D00h	32	A53SS_APBADDR_DBG_CPU1_MIDR_EL1	0007 3011 0D00h
D20h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_31_0	0007 3011 0D20h
D24h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_63_32	0007 3011 0D24h
D28h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_31_0	0007 3011 0D28h
D2Ch	32	A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_63_32	0007 3011 0D2Ch
D30h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_31_0	0007 3011 0D30h
D34h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_63_32	0007 3011 0D34h
D38h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_31_0	0007 3011 0D38h
D3Ch	32	A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_63_32	0007 3011 0D3Ch
D40h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_31_0	0007 3011 0D40h
D44h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_63_32	0007 3011 0D44h
D48h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_31_0	0007 3011 0D48h
D4Ch	32	A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_63_32	0007 3011 0D4Ch
D50h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_31_0	0007 3011 0D50h
D54h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_63_32	0007 3011 0D54h
D58h	32	A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_31_0	0007 3011 0D58h
D5Ch	32	A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_63_32	0007 3011 0D5Ch

Table 14-7681. A53SS_APBADDR_DBG_CPU1 Registers, Base Address=0007 3011 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
F00h	32	A53SS_APBADDR_DBG_CPU1_EDITCTRL	0007 3011 0F00h
FA0h	32	A53SS_APBADDR_DBG_CPU1_DBGCLAIMSET_EL1	0007 3011 0FA0h
FA4h	32	A53SS_APBADDR_DBG_CPU1_DBGCLAIMCLR_EL1	0007 3011 0FA4h
FA8h	32	A53SS_APBADDR_DBG_CPU1_EDDEVAFF0	0007 3011 0FA8h
FACh	32	A53SS_APBADDR_DBG_CPU1_EDDEVAFF1	0007 3011 0FACh
FB0h	32	A53SS_APBADDR_DBG_CPU1_EDLAR	0007 3011 0FB0h
FB4h	32	A53SS_APBADDR_DBG_CPU1_EDLSR	0007 3011 0FB4h
FB8h	32	A53SS_APBADDR_DBG_CPU1_DBGAUTHSTATUS_EL1	0007 3011 0FB8h
FBCh	32	A53SS_APBADDR_DBG_CPU1_EDDEVARCH	0007 3011 0FBCh
FC0h	32	A53SS_APBADDR_DBG_CPU1_EDDEVID2	0007 3011 0FC0h
FC4h	32	A53SS_APBADDR_DBG_CPU1_EDDEVID1	0007 3011 0FC4h
FC8h	32	A53SS_APBADDR_DBG_CPU1_EDDEVID	0007 3011 0FC8h
FCCh	32	A53SS_APBADDR_DBG_CPU1_EDDEVTYPE	0007 3011 0FCCh
FD0h	32	A53SS_APBADDR_DBG_CPU1_EDPIDR4	0007 3011 0FD0h
FE0h	32	A53SS_APBADDR_DBG_CPU1_EDPIDR0	0007 3011 0FE0h
FE4h	32	A53SS_APBADDR_DBG_CPU1_EDPIDR1	0007 3011 0FE4h
FE8h	32	A53SS_APBADDR_DBG_CPU1_EDPIDR2	0007 3011 0FE8h
FECh	32	A53SS_APBADDR_DBG_CPU1_EDPIDR3	0007 3011 0FECh
FF0h	32	A53SS_APBADDR_DBG_CPU1_EDCIDR0	0007 3011 0FF0h
FF4h	32	A53SS_APBADDR_DBG_CPU1_EDCIDR1	0007 3011 0FF4h
FF8h	32	A53SS_APBADDR_DBG_CPU1_EDCIDR2	0007 3011 0FF8h
FFCh	32	A53SS_APBADDR_DBG_CPU1_EDCIDR3	0007 3011 0FFCh

Table 14-7682. A53SS_APBADDR_PMU_CPU1 Registers, Base Address=0007 3012 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_APBADDR_PMU_CPU1_PMEVCNTR0_EL0	0007 3012 0000h
8h	32	A53SS_APBADDR_PMU_CPU1_PMEVCNTR1_EL0	0007 3012 0008h
10h	32	A53SS_APBADDR_PMU_CPU1_PMEVCNTR2_EL0	0007 3012 0010h
18h	32	A53SS_APBADDR_PMU_CPU1_PMEVCNTR3_EL0	0007 3012 0018h
20h	32	A53SS_APBADDR_PMU_CPU1_PMEVCNTR4_EL0	0007 3012 0020h
28h	32	A53SS_APBADDR_PMU_CPU1_PMEVCNTR5_EL0	0007 3012 0028h
F8h	32	A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_31_0	0007 3012 00F8h
FCh	32	A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_63_32	0007 3012 00FCh
400h	32	A53SS_APBADDR_PMU_CPU1_PMEVTYPER0_EL0	0007 3012 0400h
404h	32	A53SS_APBADDR_PMU_CPU1_PMEVTYPER1_EL0	0007 3012 0404h
408h	32	A53SS_APBADDR_PMU_CPU1_PMEVTYPER2_EL0	0007 3012 0408h
40Ch	32	A53SS_APBADDR_PMU_CPU1_PMEVTYPER3_EL0	0007 3012 040Ch
410h	32	A53SS_APBADDR_PMU_CPU1_PMEVTYPER4_EL0	0007 3012 0410h
414h	32	A53SS_APBADDR_PMU_CPU1_PMEVTYPER5_EL0	0007 3012 0414h
47Ch	32	A53SS_APBADDR_PMU_CPU1_PMCCFILTR_EL0	0007 3012 047Ch
C00h	32	A53SS_APBADDR_PMU_CPU1_PMCNTENSET_EL0	0007 3012 0C00h
C20h	32	A53SS_APBADDR_PMU_CPU1_PMCNTENCLR_EL0	0007 3012 0C20h
C40h	32	A53SS_APBADDR_PMU_CPU1_PMINTENSET_EL1	0007 3012 0C40h
C60h	32	A53SS_APBADDR_PMU_CPU1_PMINTENCLR_EL1	0007 3012 0C60h

Table 14-7682. A53SS_APBADDR_PMU_CPU1 Registers, Base Address=0007 3012 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
C80h	32	A53SS_APBADDR_PMU_CPU1_PMOVSCLR_EL0	0007 3012 0C80h
CA0h	32	A53SS_APBADDR_PMU_CPU1_PMSWINC_EL0	0007 3012 0CA0h
CC0h	32	A53SS_APBADDR_PMU_CPU1_PMOVSSET_EL0	0007 3012 0CC0h
E00h	32	A53SS_APBADDR_PMU_CPU1_PMCFGR	0007 3012 0E00h
E04h	32	A53SS_APBADDR_PMU_CPU1_PMCR_EL0	0007 3012 0E04h
E20h	32	A53SS_APBADDR_PMU_CPU1_PMCEID0_EL0	0007 3012 0E20h
E24h	32	A53SS_APBADDR_PMU_CPU1_PMCEID1_EL0	0007 3012 0E24h
F00h	32	A53SS_APBADDR_PMU_CPU1_PMITCTRL	0007 3012 0F00h
FA8h	32	A53SS_APBADDR_PMU_CPU1_PMDEVAFF0	0007 3012 0FA8h
FACh	32	A53SS_APBADDR_PMU_CPU1_PMDEVAFF1	0007 3012 0FACh
FB0h	32	A53SS_APBADDR_PMU_CPU1_PMLAR	0007 3012 0FB0h
FB4h	32	A53SS_APBADDR_PMU_CPU1_PMLSR	0007 3012 0FB4h
FB8h	32	A53SS_APBADDR_PMU_CPU1_PMAUTHSTATUS	0007 3012 0FB8h
FBCh	32	A53SS_APBADDR_PMU_CPU1_PMDEVARCH	0007 3012 0FBCh
FCCh	32	A53SS_APBADDR_PMU_CPU1_PMDEVTYPE	0007 3012 0FCCh
FD0h	32	A53SS_APBADDR_PMU_CPU1_PMPIDR4	0007 3012 0FD0h
FD4h	32	A53SS_APBADDR_PMU_CPU1_PMPIDR5	0007 3012 0FD4h
FD8h	32	A53SS_APBADDR_PMU_CPU1_PMPIDR6	0007 3012 0FD8h
FDCh	32	A53SS_APBADDR_PMU_CPU1_PMPIDR7	0007 3012 0FDCh
FE0h	32	A53SS_APBADDR_PMU_CPU1_PMPIDR0	0007 3012 0FE0h
FE4h	32	A53SS_APBADDR_PMU_CPU1_PMPIDR1	0007 3012 0FE4h
FE8h	32	A53SS_APBADDR_PMU_CPU1_PMPIDR2	0007 3012 0FE8h
FECh	32	A53SS_APBADDR_PMU_CPU1_PMPIDR3	0007 3012 0FECh
FF0h	32	A53SS_APBADDR_PMU_CPU1_PMCIDR0	0007 3012 0FF0h
FF4h	32	A53SS_APBADDR_PMU_CPU1_PMCIDR1	0007 3012 0FF4h
FF8h	32	A53SS_APBADDR_PMU_CPU1_PMCIDR2	0007 3012 0FF8h
FFCh	32	A53SS_APBADDR_PMU_CPU1_PMCIDR3	0007 3012 0FFCh

Table 14-7683. A53SS_APBADDR_ETM_CPU1 Registers, Base Address=0007 3013 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
4h	32	A53SS_APBADDR_ETM_CPU1_TRCPRGCTLR	0007 3013 0004h
Ch	32	A53SS_APBADDR_ETM_CPU1_TRCSTATR	0007 3013 000Ch
10h	32	A53SS_APBADDR_ETM_CPU1_TRCCONFIGR	0007 3013 0010h
18h	32	A53SS_APBADDR_ETM_CPU1_TRCAUXCTLR	0007 3013 0018h
20h	32	A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL0R	0007 3013 0020h
24h	32	A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL1R	0007 3013 0024h
2Ch	32	A53SS_APBADDR_ETM_CPU1_TRCSTALLCTLR	0007 3013 002Ch
30h	32	A53SS_APBADDR_ETM_CPU1_TRCTSCTLR	0007 3013 0030h
34h	32	A53SS_APBADDR_ETM_CPU1_TRCSYNCPR	0007 3013 0034h
38h	32	A53SS_APBADDR_ETM_CPU1_TRCCCCTLR	0007 3013 0038h
3Ch	32	A53SS_APBADDR_ETM_CPU1_TRCBBCTLR	0007 3013 003Ch
40h	32	A53SS_APBADDR_ETM_CPU1_TRCTRACEIDR	0007 3013 0040h
80h	32	A53SS_APBADDR_ETM_CPU1_TRCVICTLR	0007 3013 0080h
84h	32	A53SS_APBADDR_ETM_CPU1_TRCVIIECTLR	0007 3013 0084h

Table 14-7683. A53SS_APBADDR_ETM_CPU1 Registers, Base Address=0007 3013 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
88h	32	A53SS_APBADDR_ETM_CPU1_TRCVISSCTLR	0007 3013 0088h
100h	32	A53SS_APBADDR_ETM_CPU1_TRCSEQEVR0	0007 3013 0100h
104h	32	A53SS_APBADDR_ETM_CPU1_TRCSEQEVR1	0007 3013 0104h
108h	32	A53SS_APBADDR_ETM_CPU1_TRCSEQEVR2	0007 3013 0108h
118h	32	A53SS_APBADDR_ETM_CPU1_TRCSEQRSTEVR	0007 3013 0118h
11Ch	32	A53SS_APBADDR_ETM_CPU1_TRCSEQSTR	0007 3013 011Ch
120h	32	A53SS_APBADDR_ETM_CPU1_TRCEXTINSELR	0007 3013 0120h
140h	32	A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR0	0007 3013 0140h
144h	32	A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR1	0007 3013 0144h
150h	32	A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR0	0007 3013 0150h
154h	32	A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR1	0007 3013 0154h
160h	32	A53SS_APBADDR_ETM_CPU1_TRCCNTVR0	0007 3013 0160h
164h	32	A53SS_APBADDR_ETM_CPU1_TRCCNTVR1	0007 3013 0164h
180h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR8	0007 3013 0180h
184h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR9	0007 3013 0184h
188h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR10	0007 3013 0188h
18Ch	32	A53SS_APBADDR_ETM_CPU1_TRCIDR11	0007 3013 018Ch
190h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR12	0007 3013 0190h
194h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR13	0007 3013 0194h
1C0h	32	A53SS_APBADDR_ETM_CPU1_TRCIMSPEC0	0007 3013 01C0h
1E0h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR0	0007 3013 01E0h
1E4h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR1	0007 3013 01E4h
1E8h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR2	0007 3013 01E8h
1ECh	32	A53SS_APBADDR_ETM_CPU1_TRCIDR3	0007 3013 01ECh
1F0h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR4	0007 3013 01F0h
1F4h	32	A53SS_APBADDR_ETM_CPU1_TRCIDR5	0007 3013 01F4h
208h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR2	0007 3013 0208h
20Ch	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR3	0007 3013 020Ch
210h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR4	0007 3013 0210h
214h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR5	0007 3013 0214h
218h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR6	0007 3013 0218h
21Ch	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR7	0007 3013 021Ch
220h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR8	0007 3013 0220h
224h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR9	0007 3013 0224h
228h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR10	0007 3013 0228h
22Ch	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR11	0007 3013 022Ch
230h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR12	0007 3013 0230h
234h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR13	0007 3013 0234h
238h	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR14	0007 3013 0238h
23Ch	32	A53SS_APBADDR_ETM_CPU1_TRCRSCTLR15	0007 3013 023Ch
280h	32	A53SS_APBADDR_ETM_CPU1_TRCSSCCR0	0007 3013 0280h
2A0h	32	A53SS_APBADDR_ETM_CPU1_TRCSSCSR0	0007 3013 02A0h
300h	32	A53SS_APBADDR_ETM_CPU1_TRCOSLAR	0007 3013 0300h
304h	32	A53SS_APBADDR_ETM_CPU1_TRCOSLSR	0007 3013 0304h

Table 14-7683. A53SS_APBADDR_ETM_CPU1 Registers, Base Address=0007 3013 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
310h	32	A53SS_APBADDR_ETM_CPU1_TRCPDCR	0007 3013 0310h
314h	32	A53SS_APBADDR_ETM_CPU1_TRCPDSR	0007 3013 0314h
400h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR0_31_0	0007 3013 0400h
404h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR0_63_32	0007 3013 0404h
408h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR1_31_0	0007 3013 0408h
40Ch	32	A53SS_APBADDR_ETM_CPU1_TRCACVR1_63_32	0007 3013 040Ch
410h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR2_31_0	0007 3013 0410h
414h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR2_63_32	0007 3013 0414h
418h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR3_31_0	0007 3013 0418h
41Ch	32	A53SS_APBADDR_ETM_CPU1_TRCACVR3_63_32	0007 3013 041Ch
420h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR4_31_0	0007 3013 0420h
424h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR4_63_32	0007 3013 0424h
428h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR5_31_0	0007 3013 0428h
42Ch	32	A53SS_APBADDR_ETM_CPU1_TRCACVR5_63_32	0007 3013 042Ch
430h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR6_31_0	0007 3013 0430h
434h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR6_63_32	0007 3013 0434h
438h	32	A53SS_APBADDR_ETM_CPU1_TRCACVR7_31_0	0007 3013 0438h
43Ch	32	A53SS_APBADDR_ETM_CPU1_TRCACVR7_63_32	0007 3013 043Ch
480h	32	A53SS_APBADDR_ETM_CPU1_TRCACATR0	0007 3013 0480h
488h	32	A53SS_APBADDR_ETM_CPU1_TRCACATR1	0007 3013 0488h
490h	32	A53SS_APBADDR_ETM_CPU1_TRCACATR2	0007 3013 0490h
498h	32	A53SS_APBADDR_ETM_CPU1_TRCACATR3	0007 3013 0498h
4A0h	32	A53SS_APBADDR_ETM_CPU1_TRCACATR4	0007 3013 04A0h
4A8h	32	A53SS_APBADDR_ETM_CPU1_TRCACATR5	0007 3013 04A8h
4B0h	32	A53SS_APBADDR_ETM_CPU1_TRCACATR6	0007 3013 04B0h
4B8h	32	A53SS_APBADDR_ETM_CPU1_TRCACATR7	0007 3013 04B8h
600h	32	A53SS_APBADDR_ETM_CPU1_TRCCIDCVR0	0007 3013 0600h
640h	32	A53SS_APBADDR_ETM_CPU1_TRCVMIDCVR0	0007 3013 0640h
680h	32	A53SS_APBADDR_ETM_CPU1_TRCCIDCCTLR0	0007 3013 0680h
EE4h	32	A53SS_APBADDR_ETM_CPU1_TRCITATBIDR	0007 3013 0EE4h
EECh	32	A53SS_APBADDR_ETM_CPU1_TRCITIDATAR	0007 3013 0EECh
EF4h	32	A53SS_APBADDR_ETM_CPU1_TRCITIATBINR	0007 3013 0EF4h
EFCh	32	A53SS_APBADDR_ETM_CPU1_TRCITIATBOUTR	0007 3013 0EFCh
F00h	32	A53SS_APBADDR_ETM_CPU1_TRCITCTRL	0007 3013 0F00h
FA0h	32	A53SS_APBADDR_ETM_CPU1_TRCCLAIMSET	0007 3013 0FA0h
FA4h	32	A53SS_APBADDR_ETM_CPU1_TRCCLAIMCLR	0007 3013 0FA4h
FA8h	32	A53SS_APBADDR_ETM_CPU1_TRCDEVAFF0	0007 3013 0FA8h
FACh	32	A53SS_APBADDR_ETM_CPU1_TRCDEVAFF1	0007 3013 0FACh
FB0h	32	A53SS_APBADDR_ETM_CPU1_TRCLAR	0007 3013 0FB0h
FB4h	32	A53SS_APBADDR_ETM_CPU1_TRCLSR	0007 3013 0FB4h
FB8h	32	A53SS_APBADDR_ETM_CPU1_TRCAUTHSTATUS	0007 3013 0FB8h
FBCh	32	A53SS_APBADDR_ETM_CPU1_TRCDEVARCH	0007 3013 0FBCh
FC8h	32	A53SS_APBADDR_ETM_CPU1_TRCDEVID	0007 3013 0FC8h
FCCh	32	A53SS_APBADDR_ETM_CPU1_TRCDEVTYPE	0007 3013 0FCCh

Table 14-7683. A53SS_APBADDR_ETM_CPU1 Registers, Base Address=0007 3013 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FD0h	32	A53SS_APBADDR_ETM_CPU1_TRCPIDR4	0007 3013 0FD0h
FD4h	32	A53SS_APBADDR_ETM_CPU1_TRCPIDR5	0007 3013 0FD4h
FD8h	32	A53SS_APBADDR_ETM_CPU1_TRCPIDR6	0007 3013 0FD8h
FDCh	32	A53SS_APBADDR_ETM_CPU1_TRCPIDR7	0007 3013 0FDCh
FE0h	32	A53SS_APBADDR_ETM_CPU1_TRCPIDR0	0007 3013 0FE0h
FE4h	32	A53SS_APBADDR_ETM_CPU1_TRCPIDR1	0007 3013 0FE4h
FE8h	32	A53SS_APBADDR_ETM_CPU1_TRCPIDR2	0007 3013 0FE8h
FECh	32	A53SS_APBADDR_ETM_CPU1_TRCPIDR3	0007 3013 0FECh
FF0h	32	A53SS_APBADDR_ETM_CPU1_TRCCIDR0	0007 3013 0FF0h
FF4h	32	A53SS_APBADDR_ETM_CPU1_TRCCIDR1	0007 3013 0FF4h
FF8h	32	A53SS_APBADDR_ETM_CPU1_TRCCIDR2	0007 3013 0FF8h
FFCh	32	A53SS_APBADDR_ETM_CPU1_TRCCIDR3	0007 3013 0FFCh

Table 14-7684. A53SS_APBADDR_CTI_CPU1 Registers, Base Address=0007 3014 0000h, Length=65536

Offset	Length	Register Name	A53SS0 Physical Address
0h	32	A53SS_APBADDR_CTI_CPU1_CTICONTROL	0007 3014 0000h
10h	32	A53SS_APBADDR_CTI_CPU1_CTIINTACK	0007 3014 0010h
14h	32	A53SS_APBADDR_CTI_CPU1_CTIAPPSET	0007 3014 0014h
18h	32	A53SS_APBADDR_CTI_CPU1_CTIAPPCLEAR	0007 3014 0018h
1Ch	32	A53SS_APBADDR_CTI_CPU1_CTIAPPPULSE	0007 3014 001Ch
20h	32	A53SS_APBADDR_CTI_CPU1_CTIINEN0	0007 3014 0020h
24h	32	A53SS_APBADDR_CTI_CPU1_CTIINEN1	0007 3014 0024h
28h	32	A53SS_APBADDR_CTI_CPU1_CTIINEN2	0007 3014 0028h
2Ch	32	A53SS_APBADDR_CTI_CPU1_CTIINEN3	0007 3014 002Ch
30h	32	A53SS_APBADDR_CTI_CPU1_CTIINEN4	0007 3014 0030h
34h	32	A53SS_APBADDR_CTI_CPU1_CTIINEN5	0007 3014 0034h
38h	32	A53SS_APBADDR_CTI_CPU1_CTIINEN6	0007 3014 0038h
3Ch	32	A53SS_APBADDR_CTI_CPU1_CTIINEN7	0007 3014 003Ch
A0h	32	A53SS_APBADDR_CTI_CPU1_CTIOUTEN0	0007 3014 00A0h
A4h	32	A53SS_APBADDR_CTI_CPU1_CTIOUTEN1	0007 3014 00A4h
A8h	32	A53SS_APBADDR_CTI_CPU1_CTIOUTEN2	0007 3014 00A8h
ACh	32	A53SS_APBADDR_CTI_CPU1_CTIOUTEN3	0007 3014 00ACh
B0h	32	A53SS_APBADDR_CTI_CPU1_CTIOUTEN4	0007 3014 00B0h
B4h	32	A53SS_APBADDR_CTI_CPU1_CTIOUTEN5	0007 3014 00B4h
B8h	32	A53SS_APBADDR_CTI_CPU1_CTIOUTEN6	0007 3014 00B8h
BCh	32	A53SS_APBADDR_CTI_CPU1_CTIOUTEN7	0007 3014 00BCh
130h	32	A53SS_APBADDR_CTI_CPU1_CTITRIGINSTATUS	0007 3014 0130h
134h	32	A53SS_APBADDR_CTI_CPU1_CTITRIGOUTSTATUS	0007 3014 0134h
138h	32	A53SS_APBADDR_CTI_CPU1_CTICHINSTATUS	0007 3014 0138h
13Ch	32	A53SS_APBADDR_CTI_CPU1_CTICHOUTSTATUS	0007 3014 013Ch
140h	32	A53SS_APBADDR_CTI_CPU1_CTIGATE	0007 3014 0140h
144h	32	A53SS_APBADDR_CTI_CPU1_ASICCTL	0007 3014 0144h
F00h	32	A53SS_APBADDR_CTI_CPU1_CTIITCTRL	0007 3014 0F00h
FA0h	32	A53SS_APBADDR_CTI_CPU1_CTICLAIMSET	0007 3014 0FA0h

Table 14-7684. A53SS_APBADDR_CTI_CPU1 Registers, Base Address=0007 3014 0000h, Length=65536 (continued)

Offset	Length	Register Name	A53SS0 Physical Address
FA4h	32	A53SS_APBADDR_CTI_CPU1_CTICLAIMCLR	0007 3014 0FA4h
FA8h	32	A53SS_APBADDR_CTI_CPU1_CTIDEVAFF0	0007 3014 0FA8h
FACh	32	A53SS_APBADDR_CTI_CPU1_CTIDEVAFF1	0007 3014 0FACh
FB0h	32	A53SS_APBADDR_CTI_CPU1_CTILAR	0007 3014 0FB0h
FB4h	32	A53SS_APBADDR_CTI_CPU1_CTILSR	0007 3014 0FB4h
FB8h	32	A53SS_APBADDR_CTI_CPU1_CTIAUTHSTATUS	0007 3014 0FB8h
FBCh	32	A53SS_APBADDR_CTI_CPU1_CTIDEVARCH	0007 3014 0FBCh
FC0h	32	A53SS_APBADDR_CTI_CPU1_CTIDEVID2	0007 3014 0FC0h
FC4h	32	A53SS_APBADDR_CTI_CPU1_CTIDEVID1	0007 3014 0FC4h
FC8h	32	A53SS_APBADDR_CTI_CPU1_CTIDEVID	0007 3014 0FC8h
FCCh	32	A53SS_APBADDR_CTI_CPU1_CTIDEVTYPE	0007 3014 0FCCh
FD0h	32	A53SS_APBADDR_CTI_CPU1_CTIPIDR4	0007 3014 0FD0h
FD4h	32	A53SS_APBADDR_CTI_CPU1_CTIPIDR5	0007 3014 0FD4h
FD8h	32	A53SS_APBADDR_CTI_CPU1_CTIPIDR6	0007 3014 0FD8h
FDCh	32	A53SS_APBADDR_CTI_CPU1_CTIPIDR7	0007 3014 0FDCh
FE0h	32	A53SS_APBADDR_CTI_CPU1_CTIPIDR0	0007 3014 0FE0h
FE4h	32	A53SS_APBADDR_CTI_CPU1_CTIPIDR1	0007 3014 0FE4h
FE8h	32	A53SS_APBADDR_CTI_CPU1_CTIPIDR2	0007 3014 0FE8h
FECh	32	A53SS_APBADDR_CTI_CPU1_CTIPIDR3	0007 3014 0FECh
FF0h	32	A53SS_APBADDR_CTI_CPU1_CTICIDR0	0007 3014 0FF0h
FF4h	32	A53SS_APBADDR_CTI_CPU1_CTICIDR1	0007 3014 0FF4h
FF8h	32	A53SS_APBADDR_CTI_CPU1_CTICIDR2	0007 3014 0FF8h
FFCh	32	A53SS_APBADDR_CTI_CPU1_CTICIDR3	0007 3014 0FFCh

14.3.1.1.2 A53SS Registers

A53SS Registers

14.3.1.1.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-7685. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7800h**

Figure 14-2546. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-7687. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-7688. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7808h**

Figure 14-2547. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h

23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							

15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		

7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-7690. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Bh]

Misc Status

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Table 14-7691. Instance Table

Instance Name	Physical Address
A53SS0	**0071 780Ch**

Figure 14-2548. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Bh							

Table 14-7693. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-7694. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7810h + formula**

Figure 14-2549. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-7696. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-7697. Instance Table

Instance Name	Physical Address
A53SS0	**0071 783Ch**

Figure 14-2550. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7699. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7700. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7840h**

Figure 14-2551. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7702. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-7702. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-7702. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7703. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7880h**

Figure 14-2552. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7705. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7705. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7705. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7706. Instance Table

Instance Name	Physical Address
A53SS0	**0071 78C0h**

Figure 14-2553. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7708. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7708. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7708. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-7709. Instance Table

Instance Name	Physical Address
A53SS0	**0071 793Ch**

Figure 14-2554. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7711. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7712. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7940h**

Figure 14-2555. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7714. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-7714. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-7714. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7715. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7980h**

Figure 14-2556. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7717. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7717. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7717. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7718. Instance Table

Instance Name	Physical Address
A53SS0	**0071 79C0h**

Figure 14-2557. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7720. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7720. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7720. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-7721. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A00h**

Figure 14-2558. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7723. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-7724. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A04h**

Figure 14-2559. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-7726. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-7727. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A08h**

Figure 14-2560. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-7729. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-7730. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A0Ch**

Figure 14-2561. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-7732. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.1.2.17 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

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Table 14-7733. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7800h**

Figure 14-2562. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-7735. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.18 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-7736. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7808h**

Figure 14-2563. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-7738. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.19 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Bh]

Misc Status

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Table 14-7739. Instance Table

Instance Name	Physical Address
A53SS0	**0071 780Ch**

Figure 14-2564. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Bh							

Table 14-7741. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.20 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-7742. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7810h + formula**

Figure 14-2565. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-7744. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.21 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-7745. Instance Table

Instance Name	**Physical Address**
A53SS0	**0071 783Ch**

Figure 14-2566. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7747. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.22 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7748. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7840h**

Figure 14-2567. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7750. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-7750. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-7750. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.23 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7751. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7880h**

Figure 14-2568. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7753. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7753. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7753. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.24 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7754. Instance Table

Instance Name	Physical Address
A53SS0	**0071 78C0h**

Figure 14-2569. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7756. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7756. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7756. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.25 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-7757. Instance Table

Instance Name	Physical Address
A53SS0	**0071 793Ch**

Figure 14-2570. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7759. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.26 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7760. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7940h**

Figure 14-2571. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7762. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-7762. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-7762. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.27 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7763. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7980h**

Figure 14-2572. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7765. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7765. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7765. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.28 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7766. Instance Table

Instance Name	Physical Address
A53SS0	**0071 79C0h**

Figure 14-2573. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7768. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7768. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7768. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.29 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-7769. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A00h**

Figure 14-2574. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-7771. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.30 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-7772. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A04h**

Figure 14-2575. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7774. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.31 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-7775. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A08h**

Figure 14-2576. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-7777. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.32 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-7778. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A0Ch**

Figure 14-2577. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-7780. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.1.2.33 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-7781. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7800h**

Figure 14-2578. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-7783. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.34 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-7784. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7808h**

Figure 14-2579. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7786. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.35 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Bh]

Misc Status

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Table 14-7787. Instance Table

Instance Name	Physical Address
A53SS0	**0071 780Ch**

Figure 14-2580. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Bh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Bh							

Table 14-7789. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Bh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.36 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-7790. Instance Table

Instance Name	Physical Address
A53SS0	0071 7810h + formula

Figure 14-2581. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-7792. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.37 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-7793. Instance Table

Instance Name	Physical Address
A53SS0	**0071 783Ch**

Figure 14-2582. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7795. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.38 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7796. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7840h**

Figure 14-2583. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7798. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-7798. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-7798. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.39 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7799. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7880h**

Figure 14-2584. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7801. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7801. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7801. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.40 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7802. Instance Table

Instance Name	Physical Address
A53SS0	**0071 78C0h**

Figure 14-2585. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7804. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7804. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7804. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.41 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-7805. Instance Table

Instance Name	Physical Address
A53SS0	**0071 793Ch**

Figure 14-2586. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7807. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.42 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7808. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7940h**

Figure 14-2587. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7810. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend

Table 14-7810. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend

Table 14-7810. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.43 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7811. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7980h**

Figure 14-2588. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7813. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7813. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7813. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.44 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7814. Instance Table

Instance Name	Physical Address
A53SS0	**0071 79C0h**

Figure 14-2589. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7816. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way3_ecc_svbus_pend

Table 14-7816. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way2_ecc_svbus_pend
24	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way1_ecc_svbus_pend
23	CPU1_A53_DUAL_U_L1D_TAGRAM_SPRAM_WAY0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_l1d_tagram_spram_way0_ecc_svbus_pend
22	CPU1_A53_DUAL_U_TLB_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank3_ecc_svbus_pend
21	CPU1_A53_DUAL_U_TLB_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank2_ecc_svbus_pend
20	CPU1_A53_DUAL_U_TLB_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank1_ecc_svbus_pend
19	CPU1_A53_DUAL_U_TLB_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_tlb_spram_bank0_ecc_svbus_pend
18	CPU1_A53_DUAL_U_DDIRTY_SPRAM_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddirty_spram_ecc_svbus_pend
17	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank3_ecc_svbus_pend
16	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank2_ecc_svbus_pend
15	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank1_ecc_svbus_pend
14	CPU1_A53_DUAL_U_DTAG_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_dtag_spram_bank0_ecc_svbus_pend
13	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK7_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank7_ecc_svbus_pend
12	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK6_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank6_ecc_svbus_pend
11	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK5_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank5_ecc_svbus_pend
10	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK4_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank4_ecc_svbus_pend
9	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK3_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank3_ecc_svbus_pend
8	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK2_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank2_ecc_svbus_pend

Table 14-7816. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank1_ecc_svbus_pend
6	CPU1_A53_DUAL_U_DDATA_SPRAM_BANK0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_ddata_spram_bank0_ecc_svbus_pend
5	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM1_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram1_ecc_svbus_pend
4	CPU1_A53_DUAL_U_ITAG_SPRAM_RAM0_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_itag_spram_ram0_ecc_svbus_pend
3	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_hi_ecc_svbus_pend
2	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK1_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank1_lo_ecc_svbus_pend
1	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_HI_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_hi_ecc_svbus_pend
0	CPU1_A53_DUAL_U_IDATA_SPRAM_BANK0_LO_ECC_SVBUS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_a53_dual_u_idata_spram_bank0_lo_ecc_svbus_pend

14.3.1.1.2.45 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-7817. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A00h**

Figure 14-2590. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7819. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.46 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-7820. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A04h**

Figure 14-2591. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-7822. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.47 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-7823. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A08h**

Figure 14-2592. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-7825. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.48 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-7826. Instance Table

Instance Name	Physical Address
A53SS0	**0071 7A0Ch**

Figure 14-2593. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-7828. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.1.2.49 A53SS_APBADDR_ROMV8_ROMENTRY0 Register

1 A53SS_APBADDR_ROMV8_ROMENTRY0 Register (Offset = 0h) [reset = 0h]

ROM Table Entry Register 0 (CPU 0 Debug Component)

Return to Summary Table

Table 14-7829. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0000h**

Figure 14-2594. A53SS_APBADDR_ROMV8_ROMENTRY0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7831. A53SS_APBADDR_ROMV8_ROMENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.50 A53SS_APBADDR_ROMV8_ROMENTRY1 Register

1 A53SS_APBADDR_ROMV8_ROMENTRY1 Register (Offset = 4h) [reset = 0h]

ROM Table Entry Register 1 (CPU 0 CTI Component)

Return to Summary Table

Table 14-7832. Instance Table

Instance Name	Physical Address
A53SS0	0007 3000 0004h

Figure 14-2595. A53SS_APBADDR_ROMV8_ROMENTRY1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7834. A53SS_APBADDR_ROMV8_ROMENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.51 A53SS_APBADDR_ROMV8_ROMENTRY2 Register

1 A53SS_APBADDR_ROMV8_ROMENTRY2 Register (Offset = 8h) [reset = 0h]

ROM Table Entry Register 2 (CPU 0 PMU Component)

Return to Summary Table

Table 14-7835. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0008h**

Figure 14-2596. A53SS_APBADDR_ROMV8_ROMENTRY2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7837. A53SS_APBADDR_ROMV8_ROMENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.52 A53SS_APBADDR_ROMV8_ROMENTRY3 Register

1 A53SS_APBADDR_ROMV8_ROMENTRY3 Register (Offset = Ch) [reset = 0h]

ROM Table Entry Register 3 (CPU 0 ETM Component)

Return to Summary Table

Table 14-7838. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 000Ch**

Figure 14-2597. A53SS_APBADDR_ROMV8_ROMENTRY3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7840. A53SS_APBADDR_ROMV8_ROMENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.53 A53SS_APBADDR_ROMV8_ROMENTRY4 Register

1 A53SS_APBADDR_ROMV8_ROMENTRY4 Register (Offset = 10h) [reset = 0h]

ROM Table Entry Register 4 (CPU 1 Debug Component)

Return to Summary Table

Table 14-7841. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0010h**

Figure 14-2598. A53SS_APBADDR_ROMV8_ROMENTRY4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7843. A53SS_APBADDR_ROMV8_ROMENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.54 A53SS_APBADDR_ROMV8_ROMENTRY5 Register

1 A53SS_APBADDR_ROMV8_ROMENTRY5 Register (Offset = 14h) [reset = 0h]

ROM Table Entry Register 5 (CPU 1 CTI Component)

Return to Summary Table

Table 14-7844. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0014h**

Figure 14-2599. A53SS_APBADDR_ROMV8_ROMENTRY5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7846. A53SS_APBADDR_ROMV8_ROMENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.55 A53SS_APBADDR_ROMV8_ROMENTRY6 Register

1 A53SS_APBADDR_ROMV8_ROMENTRY6 Register (Offset = 18h) [reset = 0h]

ROM Table Entry Register 6 (CPU 1 PMU Component)

Return to Summary Table

Table 14-7847. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0018h**

Figure 14-2600. A53SS_APBADDR_ROMV8_ROMENTRY6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7849. A53SS_APBADDR_ROMV8_ROMENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.56 A53SS_APBADDR_ROMV8_ROMENTRY7 Register

1 A53SS_APBADDR_ROMV8_ROMENTRY7 Register (Offset = 1Ch) [reset = 0h]

ROM Table Entry Register 7 (CPU 1 ETM Component)

Return to Summary Table

Table 14-7850. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 001Ch**

Figure 14-2601. A53SS_APBADDR_ROMV8_ROMENTRY7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7852. A53SS_APBADDR_ROMV8_ROMENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.57 A53SS_APBADDR_ROMV8_ROM_PERIPHID4_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_PERIPHID4_VAL Register (Offset = FD0h) [reset = 0h]

ROM Peripheral ID 4

Return to Summary Table

Table 14-7853. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FD0h**

Figure 14-2602. A53SS_APBADDR_ROMV8_ROM_PERIPHID4_VAL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7855. A53SS_APBADDR_ROMV8_ROM_PERIPHID4_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.58 A53SS_APBADDR_ROMV8_ROM_PERIPHID5_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_PERIPHID5_VAL Register (Offset = FD4h) [reset = 0h]

ROM Peripheral ID 5

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Table 14-7856. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FD4h**

Figure 14-2603. A53SS_APBADDR_ROMV8_ROM_PERIPHID5_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7858. A53SS_APBADDR_ROMV8_ROM_PERIPHID5_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.59 A53SS_APBADDR_ROMV8_ROM_PERIPHID6_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_PERIPHID6_VAL Register (Offset = FD8h) [reset = 0h]

ROM Peripheral ID 6

Return to Summary Table

Table 14-7859. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FD8h**

Figure 14-2604. A53SS_APBADDR_ROMV8_ROM_PERIPHID6_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7861. A53SS_APBADDR_ROMV8_ROM_PERIPHID6_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.60 A53SS_APBADDR_ROMV8_ROM_PERIPHID7_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_PERIPHID7_VAL Register (Offset = FDCh) [reset = 0h]

ROM Peripheral ID 7

Return to Summary Table

Table 14-7862. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FDCh**

Figure 14-2605. A53SS_APBADDR_ROMV8_ROM_PERIPHID7_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7864. A53SS_APBADDR_ROMV8_ROM_PERIPHID7_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.61 A53SS_APBADDR_ROMV8_ROM_PERIPHID0_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_PERIPHID0_VAL Register (Offset = FE0h) [reset = 0h]

ROM Peripheral ID 0

Return to Summary Table

Table 14-7865. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FE0h**

Figure 14-2606. A53SS_APBADDR_ROMV8_ROM_PERIPHID0_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7867. A53SS_APBADDR_ROMV8_ROM_PERIPHID0_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.62 A53SS_APBADDR_ROMV8_ROM_PERIPHID1_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_PERIPHID1_VAL Register (Offset = FE4h) [reset = 0h]

ROM Peripheral ID 1

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Table 14-7868. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FE4h**

Figure 14-2607. A53SS_APBADDR_ROMV8_ROM_PERIPHID1_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7870. A53SS_APBADDR_ROMV8_ROM_PERIPHID1_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.63 A53SS_APBADDR_ROMV8_ROM_PERIPHID2_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_PERIPHID2_VAL Register (Offset = FE8h) [reset = 0h]

ROM Peripheral ID 2

Return to Summary Table

Table 14-7871. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FE8h**

Figure 14-2608. A53SS_APBADDR_ROMV8_ROM_PERIPHID2_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7873. A53SS_APBADDR_ROMV8_ROM_PERIPHID2_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.64 A53SS_APBADDR_ROMV8_ROM_PERIPHID3_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_PERIPHID3_VAL Register (Offset = FECh) [reset = 0h]

ROM Peripheral ID 3

Return to Summary Table

Table 14-7874. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FECh**

Figure 14-2609. A53SS_APBADDR_ROMV8_ROM_PERIPHID3_VAL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7876. A53SS_APBADDR_ROMV8_ROM_PERIPHID3_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.65 A53SS_APBADDR_ROMV8_ROM_COMPONID0_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_COMPONID0_VAL Register (Offset = FF0h) [reset = 0h]

ROM Component ID 0

Return to Summary Table

Table 14-7877. Instance Table

Instance Name	Physical Address
A53SS0	0007 3000 0FF0h

Figure 14-2610. A53SS_APBADDR_ROMV8_ROM_COMPONID0_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7879. A53SS_APBADDR_ROMV8_ROM_COMPONID0_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.66 A53SS_APBADDR_ROMV8_ROM_COMPONID1_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_COMPONID1_VAL Register (Offset = FF4h) [reset = 0h]

ROM Component ID 1

Return to Summary Table

Table 14-7880. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FF4h**

Figure 14-2611. A53SS_APBADDR_ROMV8_ROM_COMPONID1_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7882. A53SS_APBADDR_ROMV8_ROM_COMPONID1_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.67 A53SS_APBADDR_ROMV8_ROM_COMPONID2_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_COMPONID2_VAL Register (Offset = FF8h) [reset = 0h]

ROM Component ID 2

Return to Summary Table

Table 14-7883. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FF8h**

Figure 14-2612. A53SS_APBADDR_ROMV8_ROM_COMPONID2_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7885. A53SS_APBADDR_ROMV8_ROM_COMPONID2_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.68 A53SS_APBADDR_ROMV8_ROM_COMPONID3_VAL Register

1 A53SS_APBADDR_ROMV8_ROM_COMPONID3_VAL Register (Offset = FFCh) [reset = 0h]

ROM Component ID 3

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Table 14-7886. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3000 0FFCh**

Figure 14-2613. A53SS_APBADDR_ROMV8_ROM_COMPONID3_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7888. A53SS_APBADDR_ROMV8_ROM_COMPONID3_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.3.1.1.2.69 A53SS_APBADDR_DBG_CPU0_EDESR Register

1 A53SS_APBADDR_DBG_CPU0_EDESR Register (Offset = 20h) [reset = 0h]

External Debug Event Status Register

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Table 14-7889. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0020h**

Figure 14-2614. A53SS_APBADDR_DBG_CPU0_EDESR Name Register

31	30	29	28	27	26	25	24
RES0_EDESR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDESR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDESR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDESR_31_3					SS	RC	OSUC
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-7891. A53SS_APBADDR_DBG_CPU0_EDESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDESR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step debug event pending. Possible values of this field are: 0 Reading this means that a Halting step debug event is not pending. Writing this means no action. 1 Reading this means that a Halting step debug event is pending. Writing this clears the pending Halting step debug event.
1	RC	R/W	0h	Reset catch debug event pending. Possible values of this field are: 0 Reading this means that a Reset catch debug event is not pending. Writing this means no action. 1 Reading this means that a Reset catch debug event is pending. Writing this clears the pending Reset catch debug event.
0	OSUC	R/W	0h	OS unlock debug event pending. Possible values of this field are: 0 Reading this means that an OS unlock catch debug event is not pending. Writing this means no action. 1 Reading this means that an OS unlock catch debug event is pending. Writing this clears the pending OS unlock catch debug event.

14.3.1.1.2.70 A53SS_APBADDR_DBG_CPU0_EDECR Register

1 A53SS_APBADDR_DBG_CPU0_EDECR Register (Offset = 24h) [reset = 0h]

External Debug Execution Control Register

Return to Summary Table

Table 14-7892. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0024h**

Figure 14-2615. A53SS_APBADDR_DBG_CPU0_EDECR Name Register

31	30	29	28	27	26	25	24
RES0_EDECR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDECR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDECR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDECR_31_3					SS	RCE	OSUCE
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-7894. A53SS_APBADDR_DBG_CPU0_EDECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDECR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step enable. Possible values of this field are: 0 Halting step debug event disabled. 1 Halting step debug event enabled. If the value of EDECR.SS is changed when the processor is in Non-debug state, the resulting value of EDECR.SS is UNKNOWN.
1	RCE	R/W	0h	Reset catch enable. Possible values of this field are: 0 Reset catch debug event disabled. 1 Reset catch debug event enabled.
0	OSUCE	R/W	0h	OS unlock catch enabled. Possible values of this field are: 0 OS unlock catch debug event disabled. 1 OS unlock catch debug event enabled.

14.3.1.1.2.71 A53SS_APBADDR_DBG_CPU0_EDWAR_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_EDWAR_31_0 Register (Offset = 30h) [reset = 0h]

External Debug Watchpoint Address Register (low word)

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Table 14-7895. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0030h**

Figure 14-2616. A53SS_APBADDR_DBG_CPU0_EDWAR_31_0 Name Register

31	30	29	28	27	26	25	24
EDWAR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_31_0							
R/W							
0h							

Table 14-7897. A53SS_APBADDR_DBG_CPU0_EDWAR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_31_0	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.72 A53SS_APBADDR_DBG_CPU0_EDWAR_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_EDWAR_63_32 Register (Offset = 34h) [reset = 0h]

External Debug Watchpoint Address Register (high word)

Return to Summary Table

Table 14-7898. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0034h**

Figure 14-2617. A53SS_APBADDR_DBG_CPU0_EDWAR_63_32 Name Register

31	30	29	28	27	26	25	24
EDWAR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_63_32							
R/W							
0h							

Table 14-7900. A53SS_APBADDR_DBG_CPU0_EDWAR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_63_32	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.73 A53SS_APBADDR_DBG_CPU0_DBGDTRRX_EL0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGDTRRX_EL0 Register (Offset = 80h) [reset = 0h]

Debug Data Transfer Register Receive

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Table 14-7901. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0080h**

Figure 14-2618. A53SS_APBADDR_DBG_CPU0_DBGDTRRX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRRX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRRX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRRX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRRX_EL0							
R/W							
0h							

Table 14-7903. A53SS_APBADDR_DBG_CPU0_DBGDTRRX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRRX_EL0	R/W	0h	Update DTRRX. Writes to this register update the value in DTRRX and set RXfull to 1.Reads of this register return the last value written to DTRRX and do not change RXfull.

14.3.1.1.2.74 A53SS_APBADDR_DBG_CPU0_EDITR Register

1 A53SS_APBADDR_DBG_CPU0_EDITR Register (Offset = 84h) [reset = 0h]

External Debug Instruction Transfer Register

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Table 14-7904. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0084h**

Figure 14-2619. A53SS_APBADDR_DBG_CPU0_EDITR Name Register

31	30	29	28	27	26	25	24
EDITR							
R/W							
0h							
23	22	21	20	19	18	17	16
EDITR							
R/W							
0h							
15	14	13	12	11	10	9	8
EDITR							
R/W							
0h							
7	6	5	4	3	2	1	0
EDITR							
R/W							
0h							

Table 14-7906. A53SS_APBADDR_DBG_CPU0_EDITR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDITR	R/W	0h	Used in Debug state for passing instructions to the processor for execution

14.3.1.1.2.75 A53SS_APBADDR_DBG_CPU0_EDSCR Register

1 A53SS_APBADDR_DBG_CPU0_EDSCR Register (Offset = 88h) [reset = 0h]

External Debug Status and Control Register

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Table 14-7907. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0088h**

Figure 14-2620. A53SS_APBADDR_DBG_CPU0_EDSCR Name Register

31	30	29	28	27	26	25	24
RES0_EDSCR_31_31	RXFULL	TXFULL	ITO	RXO	TXU	PIPEADV	ITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTDIS		TDA	MA	RES0_EDSCR_19_19	NS	RES0_EDSCR_17_17	SDD
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDSCR_15_15	HDE	RW				EL	
R/W	R/W	R/W				R/W	
0h	0h	0h				0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A	ERR	STATUS					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-7909. A53SS_APBADDR_DBG_CPU0_EDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES0_EDSCR_31_31	R/W	0h	Reserved, RES0.
30	RXFULL	R/W	0h	DTRRX full. This bit is RO.
29	TXFULL	R/W	0h	DTRTX full. This bit is RO.
28	ITO	R/W	0h	EDITR overrun. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. ITO is set to 0 on entry to Debug state.
27	RXO	R/W	0h	DTRRX overrun. This bit is RO.
26	TXU	R/W	0h	DTRTX underrun. This bit is RO.
25	PIPEADV	R/W	0h	Pipeline advance. Read-only. Set to 1 every time the processor pipeline retires one or more instructions. Cleared to 0 by a write to EDRCR.CSPA.The architecture does not define precisely when this bit is set to 1. It requires only that this happen periodically in Non-debug state to indicate that software execution is progressing.
24	ITE	R/W	0h	ITR empty. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. It is always valid in Debug state.

Table 14-7909. A53SS_APBADDR_DBG_CPU0_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	INTDIS	R/W	0h	Interrupt disable. Disables taking interrupts [including virtual interrupts and System Error interrupts] in Non-Debug state.If external invasive debug is disabled, the value of this field is ignored.If external invasive debug is enabled, the possible values of this field are: 00 Do not disable interrupts 01 Disable interrupts targeting Non-secure EL1. 10 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable interrupts targeting Secure EL1. 11 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable all other interrupts. The value of INTdis does not affect whether an interrupt is a WFI wake-up event, but can mask an interrupt as a WFE wake-up event.If EL3 and EL2 are not implemented, INTdis[0] is RO and reads the same value as INTdis[1], meaning only the values 0b00 and 0b11 can be selected.
21	TDA	R/W	0h	Trap debug registers accesses.
20	MA	R/W	0h	Memory access mode. Controls use of memory-access mode for accessing EDITR and the DCC. This bit is ignored if in Non-debug state and set to zero on entry to Debug state.Possible values of this field are: 0 Normal access mode 1 Memory access mode.
19	RES0_EDSCR_19_19	R/W	0h	Reserved, RES0.
18	NS	R/W	0h	Non-secure status. Read-only. When in Debug state, gives the current security state: 0 Secure state, IsSecure[] == TRUE 1 Non-secure state, IsSecure[] == FALSE. In Non-debug state, this bit is UNKNOWN.
17	RES0_EDSCR_17_17	R/W	0h	Reserved, RES0.
16	SDD	R/W	0h	Secure debug disabled. This bit is RO.On entry to Debug state:If entering in Secure state, SDD is set to 0.If entering in Non-secure state, SDD is set to the inverse of ExternalSecureInvasiveDebugEnabled[].In Debug state, the value of the SDD bit does not change, even if ExternalSecureInvasiveDebugEnabled[] changes.In Non-debug state:SDD returns the inverse of ExternalSecureInvasiveDebugEnabled[]. If the authentication signals that control ExternalSecureInvasiveDebugEnabled[] change, a context synchronization operation is required to guarantee their effect.This bit is unaffected by the Security state of the processor.If EL3 is not implemented and the implementation is Non-secure, this bit is RES1.
15	RES0_EDSCR_15_15	R/W	0h	Reserved, RES0.
14	HDE	R/W	0h	Halting debug mode enable. Possible values of this bit are: 0 Halting debug mode disabled. 1 Halting debug mode enabled.

Table 14-7909. A53SS_APBADDR_DBG_CPU0_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:10	RW	R/W	0h	Exception level register-width status. Read-only. In Debug state, each bit gives the current register width status of each EL: 1111 All exception levels are AArch64 state. 1110 EL0 is AArch32 state. All other exception levels are AArch64 state. 1100 EL0 and EL1 are AArch32 state. All other exception levels are AArch64 state. Never seen if EL2 is not implemented in the current security state. 1000 EL0, EL1, and, if implemented in the current security state, EL2 are AArch32 state. All other exception levels are AArch64 state. 0000 All exception levels are set to AArch32 state [32-bit configuration]. However:If not at EL0: RW[0] == RW[1].If EL2 is not implemented in the current security state: RW[2] == RW[1].If EL3 is not implemented: RW[3] == RW[2].In Non-debug state, this field is RAO.
9:8	EL	R/W	0h	Exception level. Read-only. In Debug state, this gives the current EL of the processor.In Non-debug state, this field is RAZ.
7	A	R/W	0h	System Error interrupt pending. Read-only. In Debug state, indicates whether a SError interrupt is pending:If HCR_EL2.{AMO, TGE} = {1, 0} and in Non-secure EL0 or EL1, a virtual SError interrupt.Otherwise, a physical SError interrupt. 0 No SError interrupt pending. 1 SError interrupt pending. A debugger can read EDSCR to check whether a SError interrupt is pending without having to execute further instructions. A pending SError might indicate data from target memory is corrupted.UNKNOWN in Non-debug state.
6	ERR	R/W	0h	Cumulative error flag. This field is RO. It is set to 1 following exceptions in Debug state and on any signaled overrun or underrun on the DTR or EDITR.

Table 14-7909. A53SS_APBADDR_DBG_CPU0_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	STATUS	R/W	0h	Debug status flags. This field is RO.The possible values of this field are: 000010 Processor is in Non-debug state. 000001 Processor is restarting [exiting Debug state]. 000111 Breakpoint. 010011 External debug request. 011011 Halting step, normal. 011111 Halting step, exclusive. 100011 OS unlock catch. 100111 Reset catch. 101011 Watchpoint. 101111 HLT instruction. 110011 Software access to debug register. 110111 Exception catch. 111011 Halting step, no syndrome. All other values of STATUS are reserved.

14.3.1.1.2.76 A53SS_APBADDR_DBG_CPU0_DBGDTRTX_EL0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGDTRTX_EL0 Register (Offset = 8Ch) [reset = 0h]

Debug Data Transfer Register Transmit

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Table 14-7910. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 008Ch**

Figure 14-2621. A53SS_APBADDR_DBG_CPU0_DBGDTRTX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRTX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRTX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRTX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRTX_EL0							
R/W							
0h							

Table 14-7912. A53SS_APBADDR_DBG_CPU0_DBGDTRTX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRTX_EL0	R/W	0h	Return DTRTX. Reads of this register return the value in DTRTX and clear TXfull to 0.Writes of this register update the value in DTRTX and do not change TXfull.

14.3.1.1.2.77 A53SS_APBADDR_DBG_CPU0_EDRCR Register

1 A53SS_APBADDR_DBG_CPU0_EDRCR Register (Offset = 90h) [reset = 0h]

External Debug Reserve Control Register

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Table 14-7913. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0090h**

Figure 14-2622. A53SS_APBADDR_DBG_CPU0_EDRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDRCR_31_5							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDRCR_31_5							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDRCR_31_5							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDRCR_31_5			CBRRQ	CSPA	CSE	RES0_EDRCR_1_0	
R/W			R/W	R/W	R/W	R/W	
0h			0h	0h	0h	0h	

Table 14-7915. A53SS_APBADDR_DBG_CPU0_EDRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_EDRCR_31_5	R/W	0h	Reserved, RES0.
4	CBRRQ	R/W	0h	Allow imprecise entry to Debug state. The actions on Writing to this bit are: 0 No action. 1 Allow imprecise entry to Debug state, for example by canceling pending bus accesses. Setting this bit to 1 allows a debugger to request imprecise entry to Debug state. An External Debug Request debug event must be pending before the debugger sets this bit to 1.This feature is optional. If this feature is not implemented, writes to this bit are ignored.
3	CSPA	R/W	0h	Clear Sticky Pipeline Advance. This bit is used to clear the EDSCR.PipeAdv bit to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.PipeAdv bit to 0.

Table 14-7915. A53SS_APBADDR_DBG_CPU0_EDRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CSE	R/W	0h	Clear Sticky Error. Used to clear the EDSCR cumulative error bits to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.{TXU, RXO, ERR} bits, and, if the processor is in Debug state, the EDSCR.ITO bit, to 0.
1:0	RES0_EDRCR_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.78 A53SS_APBADDR_DBG_CPU0_EDACR Register

1 A53SS_APBADDR_DBG_CPU0_EDACR Register (Offset = 94h) [reset = 0h]

External Debug Auxiliary Control Register

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Table 14-7916. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0094h**

Figure 14-2623. A53SS_APBADDR_DBG_CPU0_EDACR Name Register

31	30	29	28	27	26	25	24
RES0_EDACR_31_0							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_EDACR_31_0							
R/W							
0h							

15	14	13	12	11	10	9	8
RES0_EDACR_31_0							
R/W							
0h							

7	6	5	4	3	2	1	0
RES0_EDACR_31_0							
R/W							
0h							

Table 14-7918. A53SS_APBADDR_DBG_CPU0_EDACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDACR_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.79 A53SS_APBADDR_DBG_CPU0_EDECCR Register

1 A53SS_APBADDR_DBG_CPU0_EDECCR Register (Offset = 98h) [reset = 0h]

External Debug Exception Catch Control Register

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Table 14-7919. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0098h**

Figure 14-2624. A53SS_APBADDR_DBG_CPU0_EDECCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDECCR_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDECCR_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDECCR_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">NSE</td><td colspan="4">SE</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7921. A53SS_APBADDR_DBG_CPU0_EDECCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDECCR_31_8	R/W	0h	Reserved, RES0.
7:4	NSE	R/W	0h	Coarse-grained Non-secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Non-secure exception levels. 0010 Exception catch debug event enabled for Non-secure EL1. 0100 Exception catch debug event enabled for Non-secure EL2. 0110 Exception catch debug event enabled for Non-secure EL1 and EL2. All other values are reserved. Bits [7,4] are reserved, RES0.

Table 14-7921. A53SS_APBADDR_DBG_CPU0_EDECCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SE	R/W	0h	Coarse-grained Secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Secure exception levels. 0010 Exception catch debug event enabled for Secure EL1. 1000 Exception catch debug event enabled for Secure EL3. 1010 Exception catch debug event enabled for Secure EL1 and EL3. All other values are reserved. Bits [2,0] are reserved. RES0. Ignored if ExternalSecureInvasiveDebugEnabled[] == FALSE.

14.3.1.1.2.80 A53SS_APBADDR_DBG_CPU0_EDPCSR_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_EDPCSR_31_0 Register (Offset = A0h) [reset = 0h]

External Debug Program Counter Sample Register (low word)

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Table 14-7922. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 00A0h**

Figure 14-2625. A53SS_APBADDR_DBG_CPU0_EDPCSR_31_0 Name Register

31	30	29	28	27	26	25	24
EDPCSR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_31_0							
R/W							
0h							

Table 14-7924. A53SS_APBADDR_DBG_CPU0_EDPCSR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_31_0	R/W	0h	PC Sample low word, EDPCSRlo. Bits [31_0] of the sampled instruction address value. Reading EDPCSRlo has the side-effect of updating EDCIDSR, EDVIDSR, and EDPCSRhi. However:If the processor is in Debug state, or Sample-based profiling is prohibited, EDPCSRlo reads as 0xFFFFFFFF and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.If the processor is in Reset state, the sampled value is unknown and EDCIDSR, EDVIDSR and EDPCSRhi become UNKNOWN.If no instruction has been retired since the processor left Reset state, Debug state, or a state where Non-invasive debug is not permitted, the sampled value is UNKNOWN and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.For a read of EDPCSRlo from the memory-mapped interface, if EDLSR.SLK == 1, meaning the Software Lock is locked, then the access has no side-effects. That is, EDCIDSR, EDVIDSR, and EDPCSRhi are unchanged.

14.3.1.1.2.81 A53SS_APBADDR_DBG_CPU0_EDCIDSR Register

1 A53SS_APBADDR_DBG_CPU0_EDCIDSR Register (Offset = A4h) [reset = 0h]

External Debug Context ID Sample Register

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Table 14-7925. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 00A4h**

Figure 14-2626. A53SS_APBADDR_DBG_CPU0_EDCIDSR Name Register

31	30	29	28	27	26	25	24
CONTEXTIDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CONTEXTIDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CONTEXTIDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CONTEXTIDR							
R/W							
0h							

Table 14-7927. A53SS_APBADDR_DBG_CPU0_EDCIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXTIDR	R/W	0h	The sampled value of CONTEXTIDR_EL1, captured on Reading the low half of EDPCSR.If EL3 is implemented and using AArch32 then CONTEXTIDR is a Banked register, and EDCIDSR samples the current Banked copy of CONTEXTIDR.

14.3.1.1.2.82 A53SS_APBADDR_DBG_CPU0_EDVIDSR Register

1 A53SS_APBADDR_DBG_CPU0_EDVIDSR Register (Offset = A8h) [reset = 0h]

External Debug Virtual Context Sample Register

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Table 14-7928. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 00A8h**

Figure 14-2627. A53SS_APBADDR_DBG_CPU0_EDVIDSR Name Register

31	30	29	28	27	26	25	24
NS	E2	E3	HV	RES0_EDVIDSR_27_8			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RES0_EDVIDSR_27_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDVIDSR_27_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VMID							
R/W							
0h							

Table 14-7930. A53SS_APBADDR_DBG_CPU0_EDVIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NS	R/W	0h	Non-secure state sample. Indicates the security state associated with the most recent EDPCSR sample.
30	E2	R/W	0h	Exception level 2 status sample. Indicates whether the most recent EDPCSR sample was associated with EL2. If EDVIDSR.NS == 0, this bit is 0.
29	E3	R/W	0h	Exception level 3 status sample. Indicates whether the most recent EDPCSR sample was associated with AArch64 EL3. If EDVIDSR.NS == 1 or the processor was in AArch32 state when EDPCSR was read, this bit is 0.
28	HV	R/W	0h	EDPCSR high half valid. Indicates whether bits [63_32] of the most recent EDPCSR sample are valid. If EDVIDSR.HV == 0, the value of EDPCSR[63_32] is RAZ.
27:8	RES0_EDVIDSR_27_8	R/W	0h	Reserved, RES0.
7:0	VMID	R/W	0h	VMID sample. The value of VTTBR_EL2.VMID associated with the most recent EDPCSR sample. If EDVIDSR.NS == 0 or EDVIDSR.E2 == 1, this field is RAZ.

14.3.1.1.2.83 A53SS_APBADDR_DBG_CPU0_EDPCSR_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_EDPCSR_63_32 Register (Offset = ACh) [reset = 0h]

External Debug Program Counter Sample Register (high word)

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Table 14-7931. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 00ACh**

Figure 14-2628. A53SS_APBADDR_DBG_CPU0_EDPCSR_63_32 Name Register

31	30	29	28	27	26	25	24
EDPCSR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_63_32							
R/W							
0h							

Table 14-7933. A53SS_APBADDR_DBG_CPU0_EDPCSR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_63_32	R/W	0h	PC Sample high word, EDPCSRhi. If EDVIDSR.HV == 0 then this field is RAZ, otherwise bits [63_32] of the sampled PC.

14.3.1.1.2.84 A53SS_APBADDR_DBG_CPU0_OSLAR_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_OSLAR_EL1 Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-7934. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0300h**

Figure 14-2629. A53SS_APBADDR_DBG_CPU0_OSLAR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_OSLAR_EL1_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_OSLAR_EL1_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_OSLAR_EL1_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_OSLAR_EL1_31_1							OSLK
R/W							R/W
0h							0h

Table 14-7936. A53SS_APBADDR_DBG_CPU0_OSLAR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_OSLAR_EL1_31_1	R/W	0h	Reserved, RES0.
0	OSLK	R/W	0h	On writes to OSLAR_EL1, bit[0] is copied to the OS lock.Use EDPRSR.OSLK to check the current status of the lock.

14.3.1.1.2.85 A53SS_APBADDR_DBG_CPU0_EDPRCR Register

1 A53SS_APBADDR_DBG_CPU0_EDPRCR Register (Offset = 310h) [reset = 0h]

External Debug Power/Reset Control Register

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Table 14-7937. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0310h**

Figure 14-2630. A53SS_APBADDR_DBG_CPU0_EDPRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRCR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPRCR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPRCR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDPRCR_31_4				COREPURQ	RES0_EDPRCR_2_2	CWRR	CORENPDRQ
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-7939. A53SS_APBADDR_DBG_CPU0_EDPRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDPRCR_31_4	R/W	0h	Reserved, RES0.
3	COREPURQ	R/W	0h	Core powerup request. Allows a debugger to request that the power controller power up the core, enabling access to the debug register in the Core power domain. The actions on Writing to this bit are: 0 No effect. 1 Request the power controller to powerup the core. In an implementation that includes the recommended external debug interface, this bit drives the DBGPWRUPREQ signal.This bit can be read and written when the Core power domain is powered off.The power controller must not allow the Core power domain to switch off while this bit is one.
2	RES0_EDPRCR_2_2	R/W	0h	Reserved, RES0.

Table 14-7939. A53SS_APBADDR_DBG_CPU0_EDPRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CWRR	R/W	0h	Warm reset request. Write only bit that reads as zero. The actions on Writing to this bit are: 0 No action. 1 Request Warm reset. The processor ignores writes to this bit if any of the following are the case:ExternalInvasiveDebugEnabled[] == FALSE, EL3 is not implemented, and the processor is Non-secure.ExternalSecureInvasiveDebugEnabled[] == FALSE and one of the following is true:EL3 is implemented.The processor is Secure.The Core power domain is either completely off or in a low-power state where the Core power domain registers cannot be accessed.DoubleLockStatus[] == TRUE [OS Double Lock is set].OSLSR.OSLK == 1 [OS lock is locked].In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.
0	CORENPDRQ	R/W	0h	Core no powerdown request. Requests emulation of powerdown. Possible values of this bit are: 0 On a powerdown request, the system powers down the Core power domain. 1 On a powerdown request, the system emulates powerdown of the Core power domain. In this emulation mode the Core power domain is not actually powered down.

14.3.1.1.2.86 A53SS_APBADDR_DBG_CPU0_EDPRSR Register

1 A53SS_APBADDR_DBG_CPU0_EDPRSR Register (Offset = 314h) [reset = 3h]

External Debug Processor Status Register

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Table 14-7940. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0314h**

Figure 14-2631. A53SS_APBADDR_DBG_CPU0_EDPRSR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRSR_31_12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPRSR_31_12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPRSR_31_12				SDR	SPMAD	EPMAD	SDAD
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EDAD	DLK	OSLK	HALTED	SR	R	SPD	PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 14-7942. A53SS_APBADDR_DBG_CPU0_EDPRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_EDPRSR_31_12	R/W	0h	Reserved, RES0.
11	SDR	R/W	0h	Sticky debug restart. Set to 1 when the processor exits Debug state and cleared to 0 following reads of EDPRSR. 0 The processor has not restarted since EDPRSR was last read. 1 The processor has restarted since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.
10	SPMAD	R/W	0h	Sticky EPMAD error. Set to 1 if an access returns an error because AllowExternalPMUAccess[] == FALSE. 0 No accesses to the external performance monitors registers have failed since EDPRSR was last read. 1 At least one access to the external performance monitors registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.

Table 14-7942. A53SS_APBADDR_DBG_CPU0_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EPMAD	R/W	0h	External performance monitors access disable status. 0 External performance monitors access enabled. 1 External performance monitors access disabled. If external performance monitors access is not implemented, EPMAD is RAO. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
8	SDAD	R/W	0h	Sticky EDAD error. Set to 1 if an access returns an error because AllowExternalDebugAccess[] == FALSE. 0 No accesses to the external debug registers have failed since EDPRSR was last read. 1 At least one access to the external debug registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR.
7	EDAD	R/W	0h	External debug access disable status. 0 External debug access enabled. 1 External debug access disabled. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
6	DLK	R/W	0h	OS Double Lock status bit. 0 OSDLR_EL1.DLK == 0 or EDPRCR.CORENPDRQ == 1 or the processor is in Debug state. 1 OSDLR_EL1.DLK == 1 and EDPRCR.CORENPDRQ == 0 and the processor is in Non-debug state. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
5	OSLK	R/W	0h	OS lock status bit. A read of this bit returns the value of OSLSR_EL1.OSLK.This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1 or EDPRSR.PU is 0.
4	HALTED	R/W	0h	Halted status bit. Possible values are: 0 EDSCR.STATUS is 0b000010 [processor in Non-debug state]. 1 EDSCR.STATUS is not 0b000010. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
3	SR	R/W	0h	Sticky core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state and has not been reset since the last time EDPRSR was read. 1 The non-debug logic of the processor is in reset state or has been reset since the last time EDPRSR was read. This bit is UNKNOWN on reads if EDPRSR.DLK is 1 or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR if the non-debug logic of the processor is not in reset state.
2	R	R/W	0h	Core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state. 1 The non-debug logic of the processor is in reset state. This bit is UNKNOWN on reads if either EDPRSR.DLK is 1 or EDPRSR.PU is 0.

Table 14-7942. A53SS_APBADDR_DBG_CPU0_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SPD	R/W	1h	Sticky core power-down status bit.This bit is set to 1 on Cold reset to indicate the state of the debug registers has been lost. Since a Cold reset is required on powering up the processor, this usually indicates the Core power domain has been completely powered off.Possible values are: 0 If the Core power domain is off [EDPRSR.PU is 0], it is not known whether the state of the debug registers in the Core power domain is lost. Otherwise, the Core power domain is on, and the state of the debug registers in the Core power domain has not been lost. 1 The state of the debug registers in the Core power domain is lost. This bit is UNKNOWN on reads if both EDPRSR.DLK and EDPRSR.PU are 1.This bit clears to 0 following a read of EDPRSR if the processor is not in the powered down state. There are two logical power off states for the Core power domain:RetentionThe states of the debug registers, including EDPRSR.SPD, in the Core power domain is preserved, and restored on leaving retention state.Power-downThe states of the debug registers in the Core power domain is lost, and a Cold reset is asserted on leaving power-down state.In these states, it is IMPLEMENTATION DEFINED whether:EDPRSR.SPD shows whether the state of the debug registers in the Core power domain has been lost since the last time EDPRSR was read when the Core power domain was on.EDPRSR.SPD reads-as-zero.EDPRSR.SPD is not cleared following a read of EDPRSR in these states.This means it is IMPLEMENTATION DEFINED whether a processor implements EDPRSR.SPD as:Fixed RAZ when in one or both of the retention and power-down states.Retaining its previous value when in the retention state.Fixed RAO in the power-down state.Note that this definition does not allow EDPRSR.SPD to be fixed RAO in the low-power retention state, as the state of the debug registers in the Core power domain is not lost by entering this state. However, the bit can be read as 1 in this state if the state of the registers was lost before entering this state [i.e. EDPRSR has not been read since the last Cold reset].ARM recommends that an implementation make EDPRSR.SPD fixed RAO when in the power-down state, particularly if it does not support a low-power retention state.
0	PU	R/W	1h	Core power-up status bit. Indicates whether the Core power domain debug registers can be accessed: 0 Core is in a low-power or power-down state where the debug registers cannot be accessed. 1 Core is in a power-up state where the debug registers can be accessed.

14.3.1.1.2.87 A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_31_0 Register (Offset = 400h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7943. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0400h**

Figure 14-2632. A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_31_0							
R/W							
0h							

Table 14-7945. A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.88 A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_63_32 Register (Offset = 404h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7946. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0404h**

Figure 14-2633. A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_63_32							
R/W							
0h							

Table 14-7948. A53SS_APBADDR_DBG_CPU0_DBGBVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.89 A53SS_APBADDR_DBG_CPU0_DBGBCR0_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBCR0_EL1 Register (Offset = 408h) [reset = 0h]

Debug Breakpoint Control Register 0

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Table 14-7949. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0408h**

Figure 14-2634. A53SS_APBADDR_DBG_CPU0_DBGBCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR0_EL1_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BT				LBN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	RES0_DBGBCR0_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			RES0_DBGBCR0_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-7951. A53SS_APBADDR_DBG_CPU0_DBGBCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR0_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-7951. A53SS_APBADDR_DBG_CPU0_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR0_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-7951. A53SS_APBADDR_DBG_CPU0_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR0_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.90 A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_31_0 Register (Offset = 410h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7952. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0410h**

Figure 14-2635. A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_31_0							
R/W							
0h							

Table 14-7954. A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.91 A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_63_32 Register (Offset = 414h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7955. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0414h**

Figure 14-2636. A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_63_32							
R/W							
0h							

Table 14-7957. A53SS_APBADDR_DBG_CPU0_DBGBVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.92 A53SS_APBADDR_DBG_CPU0_DBGBCR1_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBCR1_EL1 Register (Offset = 418h) [reset = 0h]

Debug Breakpoint Control Register 1

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Table 14-7958. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0418h**

Figure 14-2637. A53SS_APBADDR_DBG_CPU0_DBGBCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR1_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR1_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR1_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-7960. A53SS_APBADDR_DBG_CPU0_DBGBCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR1_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-7960. A53SS_APBADDR_DBG_CPU0_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR1_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-7960. A53SS_APBADDR_DBG_CPU0_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR1_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.93 A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_31_0 Register (Offset = 420h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7961. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0420h**

Figure 14-2638. A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_31_0							
R/W							
0h							

Table 14-7963. A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.94 A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_63_32 Register (Offset = 424h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7964. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0424h**

Figure 14-2639. A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_63_32							
R/W							
0h							

Table 14-7966. A53SS_APBADDR_DBG_CPU0_DBGBVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.95 A53SS_APBADDR_DBG_CPU0_DBGBCR2_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBCR2_EL1 Register (Offset = 428h) [reset = 0h]

Debug Breakpoint Control Register 2

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Table 14-7967. Instance Table

Instance Name	Physical Address
A53SS0	0007 3001 0428h

Figure 14-2640. A53SS_APBADDR_DBG_CPU0_DBGBCR2_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR2_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR2_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR2_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-7969. A53SS_APBADDR_DBG_CPU0_DBGBCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR2_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-7969. A53SS_APBADDR_DBG_CPU0_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR2_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-7969. A53SS_APBADDR_DBG_CPU0_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR2_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.96 A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_31_0 Register (Offset = 430h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7970. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0430h**

Figure 14-2641. A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_31_0							
R/W							
0h							

Table 14-7972. A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.97 A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_63_32 Register (Offset = 434h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7973. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0434h**

Figure 14-2642. A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_63_32							
R/W							
0h							

Table 14-7975. A53SS_APBADDR_DBG_CPU0_DBGBVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.98 A53SS_APBADDR_DBG_CPU0_DBGBCR3_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBCR3_EL1 Register (Offset = 438h) [reset = 0h]

Debug Breakpoint Control Register 3

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Table 14-7976. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0438h**

Figure 14-2643. A53SS_APBADDR_DBG_CPU0_DBGBCR3_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR3_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR3_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR3_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-7978. A53SS_APBADDR_DBG_CPU0_DBGBCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR3_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-7978. A53SS_APBADDR_DBG_CPU0_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR3_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-7978. A53SS_APBADDR_DBG_CPU0_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR3_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.99 A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_31_0 Register (Offset = 440h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7979. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0440h**

Figure 14-2644. A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_31_0							
R/W							
0h							

Table 14-7981. A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.100 A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_63_32 Register (Offset = 444h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7982. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0444h**

Figure 14-2645. A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_63_32							
R/W							
0h							

Table 14-7984. A53SS_APBADDR_DBG_CPU0_DBGBVR4_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.101 A53SS_APBADDR_DBG_CPU0_DBGBCR4_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBCR4_EL1 Register (Offset = 448h) [reset = 0h]

Debug Breakpoint Control Register 4

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Table 14-7985. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0448h**

Figure 14-2646. A53SS_APBADDR_DBG_CPU0_DBGBCR4_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR4_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR4_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR4_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-7987. A53SS_APBADDR_DBG_CPU0_DBGBCR4_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR4_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-7987. A53SS_APBADDR_DBG_CPU0_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR4_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-7987. A53SS_APBADDR_DBG_CPU0_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR4_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.102 A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_31_0 Register (Offset = 450h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7988. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0450h**

Figure 14-2647. A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_31_0							
R/W							
0h							

Table 14-7990. A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.103 A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_63_32 Register (Offset = 454h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-7991. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0454h**

Figure 14-2648. A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_63_32							
R/W							
0h							

Table 14-7993. A53SS_APBADDR_DBG_CPU0_DBGBVR5_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.104 A53SS_APBADDR_DBG_CPU0_DBGBCR5_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGBCR5_EL1 Register (Offset = 458h) [reset = 0h]

Debug Breakpoint Control Register 5

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Table 14-7994. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0458h**

Figure 14-2649. A53SS_APBADDR_DBG_CPU0_DBGBCR5_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGBCR5_EL1_31_24</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BT</td><td colspan="4">LBN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">SSC</td><td>HMC</td><td colspan="4">RES0_DBGBCR5_EL1_12_9</td><td>BAS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">BAS</td><td colspan="2">RES0_DBGBCR5_EL1_4_3</td><td colspan="2">PMC</td><td>E</td></tr>
<tr><td colspan="3">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-7996. A53SS_APBADDR_DBG_CPU0_DBGBCR5_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR5_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-7996. A53SS_APBADDR_DBG_CPU0_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR5_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-7996. A53SS_APBADDR_DBG_CPU0_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR5_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.105 A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_31_0 Register (Offset = 800h) [reset = 0h]

Debug Watchpoint Value Register 0

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Table 14-7997. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0800h**

Figure 14-2650. A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR0_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-7999. A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR0_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.106 A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_63_32 Register (Offset = 804h) [reset = 0h]

Debug Watchpoint Extended Value Register 0

Return to Summary Table

Table 14-8000. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0804h**

Figure 14-2651. A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-8002. A53SS_APBADDR_DBG_CPU0_DBGWVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.107 A53SS_APBADDR_DBG_CPU0_DBGWCR0_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWCR0_EL1 Register (Offset = 808h) [reset = 0h]

Debug Watchpoint Control Register 0

Return to Summary Table

Table 14-8003. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0808h**

Figure 14-2652. A53SS_APBADDR_DBG_CPU0_DBGWCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR0_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR0_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8005. A53SS_APBADDR_DBG_CPU0_DBGWCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR0_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR0_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-8005. A53SS_APBADDR_DBG_CPU0_DBGWCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.108 A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_31_0 Register (Offset = 810h) [reset = 0h]

Debug Watchpoint Value Register 1

Return to Summary Table

Table 14-8006. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0810h**

Figure 14-2653. A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">VA</td><td colspan="2">RES0_DBGWVR1_EL1_31_0_1_0</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-8008. A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR1_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.109 A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_63_32 Register (Offset = 814h) [reset = 0h]

Debug Watchpoint Extended Value Register 1

Return to Summary Table

Table 14-8009. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0814h**

Figure 14-2654. A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESS							VA
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA							
R/W							
0h							

Table 14-8011. A53SS_APBADDR_DBG_CPU0_DBGWVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.110 A53SS_APBADDR_DBG_CPU0_DBGWCR1_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWCR1_EL1 Register (Offset = 818h) [reset = 0h]

Debug Watchpoint Control Register 1

Return to Summary Table

Table 14-8012. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0818h**

Figure 14-2655. A53SS_APBADDR_DBG_CPU0_DBGWCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR1_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR1_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8014. A53SS_APBADDR_DBG_CPU0_DBGWCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR1_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR1_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-8014. A53SS_APBADDR_DBG_CPU0_DBGWCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.111 A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_31_0 Register (Offset = 820h) [reset = 0h]

Debug Watchpoint Value Register 2

Return to Summary Table

Table 14-8015. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0820h**

Figure 14-2656. A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_31_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">VA</td><td colspan="2">RES0_DBGWVR2_EL1_31_0_1_0</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-8017. A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR2_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.112 A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_63_32 Register (Offset = 824h) [reset = 0h]

Debug Watchpoint Extended Value Register 2

Return to Summary Table

Table 14-8018. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0824h**

Figure 14-2657. A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESS</td><td>VA</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8020. A53SS_APBADDR_DBG_CPU0_DBGWVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.113 A53SS_APBADDR_DBG_CPU0_DBGWCR2_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWCR2_EL1 Register (Offset = 828h) [reset = 0h]

Debug Watchpoint Control Register 2

Return to Summary Table

Table 14-8021. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0828h**

Figure 14-2658. A53SS_APBADDR_DBG_CPU0_DBGWCR2_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR2_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR2_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8023. A53SS_APBADDR_DBG_CPU0_DBGWCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR2_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR2_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-8023. A53SS_APBADDR_DBG_CPU0_DBGWCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.114 A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_31_0 Register (Offset = 830h) [reset = 0h]

Debug Watchpoint Value Register 3

Return to Summary Table

Table 14-8024. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0830h**

Figure 14-2659. A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR3_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-8026. A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR3_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.115 A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_63_32 Register (Offset = 834h) [reset = 0h]

Debug Watchpoint Extended Value Register 3

Return to Summary Table

Table 14-8027. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0834h**

Figure 14-2660. A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-8029. A53SS_APBADDR_DBG_CPU0_DBGWVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.116 A53SS_APBADDR_DBG_CPU0_DBGWCR3_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGWCR3_EL1 Register (Offset = 838h) [reset = 0h]

Debug Watchpoint Control Register 3

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Table 14-8030. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0838h**

Figure 14-2661. A53SS_APBADDR_DBG_CPU0_DBGWCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR3_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR3_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8032. A53SS_APBADDR_DBG_CPU0_DBGWCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR3_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR3_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-8032. A53SS_APBADDR_DBG_CPU0_DBGWCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.117 A53SS_APBADDR_DBG_CPU0_MIDR_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_MIDR_EL1 Register (Offset = D00h) [reset = 410FD034h]

Main ID Register

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Table 14-8033. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D00h**

Figure 14-2662. A53SS_APBADDR_DBG_CPU0_MIDR_EL1 Name Register

31	30	29	28	27	26	25	24
IMPLEMENTER							
R/W							
41h							
23	22	21	20	19	18	17	16
VARIANT				ARCHITECTURE			
R/W				R/W			
0h				Fh			
15	14	13	12	11	10	9	8
PARTNUM							
R/W							
D03h							
7	6	5	4	3	2	1	0
PARTNUM				REVISION			
R/W				R/W			
D03h				4h			

Table 14-8035. A53SS_APBADDR_DBG_CPU0_MIDR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IMPLEMENTER	R/W	41h	The Implementer code. This field must hold an implementer code that has been assigned by ARM.
23:20	VARIANT	R/W	0h	An IMPLEMENTATION DEFINED variant number. Typically this field is used to distinguish between different product variants or major revisions of a product.
19:16	ARCHITECTURE	R/W	Fh	
15:4	PARTNUM	R/W	D03h	An IMPLEMENTATION DEFINED primary part number for the device. On processors implemented by ARM if the top four bits of the primary part number are 0x0 or 0x7 the variant and architecture are encoded differently
3:0	REVISION	R/W	4h	An IMPLEMENTATION DEFINED revision number for the device

14.3.1.1.2.118 A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_31_0 Register (Offset = D20h) [reset = 1002222h]

Processor Feature Register 0 (low word)

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Table 14-8036. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D20h**

Figure 14-2663. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_31_0_31_28				GIC			
R/W				R/W			
0h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADVSIMD				FP			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EL3				EL2			
R/W				R/W			
2h				2h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EL1				EL0			
R/W				R/W			
2h				2h			

Table 14-8038. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_ID_AA64PFR0_EL1_31_0_31_28	R/W	0h	Reserved, RES0.
27:24	GIC	R/W	1h	GIC system register interface. Permitted values are: 0000 No GIC system registers are supported. 0001 GICv3 system registers are supported. All other values are reserved.
23:20	ADVSIMD	R/W	0h	Advanced SIMD. Permitted values are: 0000 Advanced SIMD is implemented. 1111 Advanced SIMD is not implemented. All other values are reserved.
19:16	FP	R/W	0h	Floating-point. Permitted values are: 0000 Floating-point is implemented. 1111 Floating-point is not implemented. All other values are reserved.

Table 14-8038. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	EL3	R/W	2h	EL3 exception level handling. Permitted values are: 0000 EL3 is not implemented. 0001 EL3 can be executed in AArch64 state only. 0010 EL3 can be executed in either AArch64 or AArch32 state. All other values are reserved.
11:8	EL2	R/W	2h	EL2 exception level handling. Permitted values are: 0000 EL2 is not implemented. 0001 EL2 can be executed in AArch64 state only. 0010 EL2 can be executed in either AArch64 or AArch32 state. All other values are reserved.
7:4	EL1	R/W	2h	EL1 exception level handling. Permitted values are: 0000 EL1 is not implemented. 0001 EL1 can be executed in AArch64 state only. 0010 EL1 can be executed in either AArch64 or AArch32 state. All other values are reserved.
3:0	EL0	R/W	2h	EL0 exception level handling. Permitted values are: 0000 EL0 is not implemented. 0001 EL0 can be executed in AArch64 state only. 0010 EL0 can be executed in either AArch64 or AArch32 state. All other values are reserved.

14.3.1.1.2.119 A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_63_32 Register (Offset = D24h) [reset = 0h]

Processor Feature Register 0 (high word)

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Table 14-8039. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D24h**

Figure 14-2664. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-8041. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.120 A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_31_0 Register (Offset = D28h) [reset = 10305106h]

Debug Feature Register 0 (low word)

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Table 14-8042. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D28h**

Figure 14-2665. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
CTX_CMPS				RES0_ID_AA64DFR0_EL1_31_0_27_24			
R/W				R/W			
1h				0h			
23	22	21	20	19	18	17	16
WRPS				RES0_ID_AA64DFR0_EL1_31_0_19_16			
R/W				R/W			
3h				0h			
15	14	13	12	11	10	9	8
BRPS				PMUVER			
R/W				R/W			
5h				1h			
7	6	5	4	3	2	1	0
TRACEVER				DEBUGVER			
R/W				R/W			
0h				6h			

Table 14-8044. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CTX_CMPS	R/W	1h	Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.
27:24	RES0_ID_AA64DFR0_EL1_31_0_27_24	R/W	0h	Reserved, RES0.
23:20	WRPS	R/W	3h	Number of watchpoints, minus 1. The value of 0b0000 is reserved.
19:16	RES0_ID_AA64DFR0_EL1_31_0_19_16	R/W	0h	Reserved, RES0.
15:12	BRPS	R/W	5h	Number of breakpoints, minus 1. The value of 0b0000 is reserved.
11:8	PMUVER	R/W	1h	Performance Monitors extension version. Indicates whether system register interface to Performance Monitors extension is implemented. Permitted values are: 0000 Performance Monitors extension system registers not implemented. 0001 Performance Monitors extension system registers implemented, PMUv3. 1111 IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. All other values are reserved.

Table 14-8044. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRACEVER	R/W	0h	Trace extension. Indicates whether system register interface to Trace extension is implemented. Permitted values are: 0000 Trace extension system registers not implemented. 0001 Trace extension system registers implemented. All other values are reserved.A value of 0b0000 only indicates that no system register interface to the trace extension is implemented. A trace extension may nevertheless be implemented without a system register interface.
3:0	DEBUGVER	R/W	6h	Debug architecture version. Indicates presence of v8-A debug architecture. 0110 v8-A debug architecture. All other values are reserved.

14.3.1.1.2.121 A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_63_32 Register (Offset = D2Ch) [reset = 0h]

Debug Feature Register 0 (high word)

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Table 14-8045. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D2Ch**

Figure 14-2666. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-8047. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.122 A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_31_0 Register (Offset = D30h) [reset = 11120h]

Instruction Set Attribute Register 0 (low word)

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Table 14-8048. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D30h**

Figure 14-2667. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_31_0_31_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR0_EL1_31_0_31_20				CRC32			
R/W				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SHA2				SHA1			
R/W				R/W			
1h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AES				RES0_ID_AA64ISAR0_EL1_31_0_3_0			
R/W				R/W			
2h				0h			

Table 14-8050. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_ID_AA64ISAR0_EL1_31_0_31_20	R/W	0h	Reserved, RES0.
19:16	CRC32	R/W	1h	CRC32 instructions in AArch64. Possible values of this field are: 0000 No CRC32 instructions implemented. 0001 CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX instructions implemented. All other values are reserved.This field must have the same value as ID_ISAR5.CRC32. The architecture requires that if CRC32 is supported in one Execution state, it must be supported in both Execution states.
15:12	SHA2	R/W	1h	SHA2 instructions in AArch64. Possible values of this field are: 0000 No SHA2 instructions implemented. 0001 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions implemented. All other values are reserved.

Table 14-8050. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	SHA1	R/W	1h	SHA1 instructions in AArch64. Possible values of this field are: 0000 No SHA1 instructions implemented. 0001 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions implemented. All other values are reserved.
7:4	AES	R/W	2h	AES instructions in AArch64. Possible values of this field are: 0000 No AES instructions implemented. 0001 AESE, AESD, AESMC, and AESIMC instructions implemented. 0010 As for 0b0001, plus PMULL/PMULL2 instructions operating on 64-bit data quantities.
3:0	RES0_ID_AA64ISAR0_EL1_31_0_3_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.123 A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_63_32 Register (Offset = D34h) [reset = 0h]

Instruction Set Attribute Register 0 (high word)

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Table 14-8051. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D34h**

Figure 14-2668. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-8053. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.124 A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_31_0 Register (Offset = D38h) [reset = 1122h]

Memory Model Feature Register 0 (low word)

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Table 14-8054. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D38h**

Figure 14-2669. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
TGRAN4				TGRAN64			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
TGRAN16				BIGENDEL0			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SNSMEM				BIGEND			
R/W				R/W			
1h				1h			
7	6	5	4	3	2	1	0
ASIDBITS				PARANGE			
R/W				R/W			
2h				2h			

Table 14-8056. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TGRAN4	R/W	0h	Support for 4 Kbyte memory translation granule size. Permitted values are: 0000 4 KB granule supported. 1111 4 KB granule not supported. All other values are reserved.
27:24	TGRAN64	R/W	0h	Support for 64 Kbyte memory translation granule size. Permitted values are: 0000 64 KB granule supported. 1111 64 KB granule not supported. All other values are reserved.
23:20	TGRAN16	R/W	0h	Support for 16 Kbyte memory translation granule size. Permitted values are: 0000 16 KB granule not supported. 0001 16 KB granule supported. All other values are reserved.

Table 14-8056. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	BIGENDEL0	R/W	0h	Mixed-endian support at EL0 only. Permitted values are: 0000 No mixed-endian support at EL0. The SCTLR_EL1.E0E bit has a fixed value. 0001 Mixed-endian support at EL0. The SCTLR_EL1.E0E bit can be configured. All other values are reserved.This field is invalid and is RES0 if the BigEnd field, bits [11:8], is not 0b0000.
15:12	SNSMEM	R/W	1h	Secure versus Non-secure Memory distinction. Permitted values are: 0000 Does not support a distinction between Secure and Non-secure Memory. 0001 Does support a distinction between Secure and Non-secure Memory. All other values are reserved.
11:8	BIGEND	R/W	1h	Mixed-endian configuration support. Permitted values are: 0000 No mixed-endian support. The SCTLR_ELx.EE bits have a fixed value. See the BigEndEL0 field, bits[19:16], for whether EL0 supports mixed-endian. 0001 Mixed-endian support. The SCTLR_ELx.EE and SCTLR_EL1.E0E bits can be configured. All other values are reserved.
7:4	ASIDBITS	R/W	2h	Number of ASID bits. Permitted values are: 0000 8 bits. 0010 16 bits. All other values are reserved.
3:0	PARANGE	R/W	2h	Physical Address range supported. Permitted values are: 0000 32 bits, 4 GB. 0001 36 bits, 64 GB. 0010 40 bits, 1 TB. 0011 42 bits, 4 TB. 0100 44 bits, 16 TB. 0101 48 bits, 256 TB. All other values are reserved.

14.3.1.1.2.125 A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_63_32 Register (Offset = D3Ch) [reset = 0h]

Memory Model Feature Register 0 (high word)

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Table 14-8057. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D3Ch**

Figure 14-2670. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-8059. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.126 A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_31_0 Register (Offset = D40h) [reset = 0h]

Processor Feature Register 1 (low word)

Return to Summary Table

Table 14-8060. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D40h**

Figure 14-2671. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-8062. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.127 A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_63_32 Register (Offset = D44h) [reset = 0h]

Processor Feature Register 1 (high word)

Return to Summary Table

Table 14-8063. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D44h**

Figure 14-2672. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-8065. A53SS_APBADDR_DBG_CPU0_ID_AA64PFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.128 A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_31_0 Register (Offset = D48h) [reset = 0h]

Auxiliary Feature Register 1 (low word)

Return to Summary Table

Table 14-8066. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D48h**

Figure 14-2673. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-8068. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.129 A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_63_32 Register (Offset = D4Ch) [reset = 0h]

Auxiliary Feature Register 1 (high word)

Return to Summary Table

Table 14-8069. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D4Ch**

Figure 14-2674. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							

15	14	13	12	11	10	9	8
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							

7	6	5	4	3	2	1	0
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-8071. A53SS_APBADDR_DBG_CPU0_ID_AA64DFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.130 A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_31_0 Register (Offset = D50h) [reset = 0h]

Instruction Set Attribute Register 1 (low word)

Return to Summary Table

Table 14-8072. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D50h**

Figure 14-2675. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-8074. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.131 A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_63_32 Register (Offset = D54h) [reset = 0h]

Instruction Set Attribute Register 1 (high word)

Return to Summary Table

Table 14-8075. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D54h**

Figure 14-2676. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-8077. A53SS_APBADDR_DBG_CPU0_ID_AA64ISAR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.132 A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_31_0 Register (Offset = D58h) [reset = 0h]

Memory Model Feature Register 1 (low word)

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Table 14-8078. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D58h**

Figure 14-2677. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-8080. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.133 A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_63_32 Register (Offset = D5Ch) [reset = 0h]

Memory Model Feature Register 1 (high word)

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Table 14-8081. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0D5Ch**

Figure 14-2678. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-8083. A53SS_APBADDR_DBG_CPU0_ID_AA64MMFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.134 A53SS_APBADDR_DBG_CPU0_EDITCTRL Register

1 A53SS_APBADDR_DBG_CPU0_EDITCTRL Register (Offset = F00h) [reset = 0h]

External Debug Integration mode Control Register

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Table 14-8084. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0F00h**

Figure 14-2679. A53SS_APBADDR_DBG_CPU0_EDITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_EDITCTRL_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDITCTRL_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDITCTRL_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-8086. A53SS_APBADDR_DBG_CPU0_EDITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_EDITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.135 A53SS_APBADDR_DBG_CPU0_DBGCLAIMSET_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGCLAIMSET_EL1 Register (Offset = FA0h) [reset = FFh]

Debug Claim Tag Set Register

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Table 14-8087. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FA0h**

Figure 14-2680. A53SS_APBADDR_DBG_CPU0_DBGCLAIMSET_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGCLAIMSET_EL1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_DBGCLAIMSET_EL1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_DBGCLAIMSET_EL1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
</table>

Table 14-8089. A53SS_APBADDR_DBG_CPU0_DBGCLAIMSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMSET_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	FFh	Claim set bits. RAO.Writing a 1 to one of these bits sets the corresponding CLAIM bit to 1. This is an indirect write to the CLAIM bits.A single write operation can set multiple bits to 1. Writing 0 to one of these bits has no effect.

14.3.1.1.2.136 A53SS_APBADDR_DBG_CPU0_DBGCLAIMCLR_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGCLAIMCLR_EL1 Register (Offset = FA4h) [reset = 0h]

Debug Claim Tag Clear Register

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Table 14-8090. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FA4h**

Figure 14-2681. A53SS_APBADDR_DBG_CPU0_DBGCLAIMCLR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIM							
R/W							
0h							

Table 14-8092. A53SS_APBADDR_DBG_CPU0_DBGCLAIMCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMCLR_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	0h	Claim clear bits. Reading this field returns the current value of the CLAIM bits.Writing a 1 to one of these bits clears the corresponding CLAIM bit to 0. This is an indirect write to the CLAIM bits.A single write operation can clear multiple bits to 0. Writing 0 to one of these bits has no effect.

14.3.1.1.2.137 A53SS_APBADDR_DBG_CPU0_EDDEVAFF0 Register

1 A53SS_APBADDR_DBG_CPU0_EDDEVAFF0 Register (Offset = FA8h) [reset = 80000000h]

External Debug Device Affinity Register 0

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Table 14-8093. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FA8h**

Figure 14-2682. A53SS_APBADDR_DBG_CPU0_EDDEVAFF0 Name Register

31	30	29	28	27	26	25	24
EDDEVAFF0							
R/W							
80000000h							
23	22	21	20	19	18	17	16
EDDEVAFF0							
R/W							
80000000h							
15	14	13	12	11	10	9	8
EDDEVAFF0							
R/W							
80000000h							
7	6	5	4	3	2	1	0
EDDEVAFF0							
R/W							
80000000h							

Table 14-8095. A53SS_APBADDR_DBG_CPU0_EDDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF0	R/W	80000000h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.138 A53SS_APBADDR_DBG_CPU0_EDDEVAFF1 Register

1 A53SS_APBADDR_DBG_CPU0_EDDEVAFF1 Register (Offset = FACh) [reset = 0h]

External Debug Device Affinity Register 1

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Table 14-8096. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FACh**

Figure 14-2683. A53SS_APBADDR_DBG_CPU0_EDDEVAFF1 Name Register

31	30	29	28	27	26	25	24
EDDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
EDDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
EDDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
EDDEVAFF1							
R/W							
0h							

Table 14-8098. A53SS_APBADDR_DBG_CPU0_EDDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.139 A53SS_APBADDR_DBG_CPU0_EDLAR Register

1 A53SS_APBADDR_DBG_CPU0_EDLAR Register (Offset = FB0h) [reset = 0h]

External Debug Lock Access Register

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Table 14-8099. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FB0h**

Figure 14-2684. A53SS_APBADDR_DBG_CPU0_EDLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-8101. A53SS_APBADDR_DBG_CPU0_EDLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.140 A53SS_APBADDR_DBG_CPU0_EDLSR Register

1 A53SS_APBADDR_DBG_CPU0_EDLSR Register (Offset = FB4h) [reset = 0h]

External Debug Lock Status Register

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Table 14-8102. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FB4h**

Figure 14-2685. A53SS_APBADDR_DBG_CPU0_EDLSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDLSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDLSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDLSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RES0_EDLSR_31_3</td><td>NTT</td><td>SLK</td><td>SLI</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8104. A53SS_APBADDR_DBG_CPU0_EDLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.141 A53SS_APBADDR_DBG_CPU0_DBGAUTHSTATUS_EL1 Register

1 A53SS_APBADDR_DBG_CPU0_DBGAUTHSTATUS_EL1 Register (Offset = FB8h) [reset = AAh]

Debug Authentication Status register

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Table 14-8105. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FB8h**

Figure 14-2686. A53SS_APBADDR_DBG_CPU0_DBGAUTHSTATUS_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_DBGAUTHSTATUS_EL1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_DBGAUTHSTATUS_EL1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_DBGAUTHSTATUS_EL1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SNID</td><td colspan="2">SID</td><td colspan="2">NSNID</td><td colspan="2">NSID</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">2h</td><td colspan="2">2h</td><td colspan="2">2h</td><td colspan="2">2h</td></tr>
</table>

Table 14-8107. A53SS_APBADDR_DBG_CPU0_DBGAUTHSTATUS_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGAUTHSTATUS_EL1_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
5:4	SID	R/W	2h	Secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureInvasiveDebugEnabled[] == TRUE. Other values are reserved.

Table 14-8107. A53SS_APBADDR_DBG_CPU0_DBGAUTHSTATUS_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Non-secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
1:0	NSID	R/W	2h	Non-secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalInvasiveDebugEnabled[] == TRUE. Other values are reserved.

14.3.1.1.2.142 A53SS_APBADDR_DBG_CPU0_EDDEVARCH Register

1 A53SS_APBADDR_DBG_CPU0_EDDEVARCH Register (Offset = FBCh) [reset = 47706A15h]

External Debug Device Architecture Register

Return to Summary Table

Table 14-8108. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FBCh**

Figure 14-2687. A53SS_APBADDR_DBG_CPU0_EDDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6A15h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6A15h</td></tr>
</table>

Table 14-8110. A53SS_APBADDR_DBG_CPU0_EDDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For debug, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For debug, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	6A15h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For debug:Bits [15:12] are the architecture version, 0x6.Bits [11:0] are the architecture part number, 0xA15.This corresponds to debug architecture version v8-A.

14.3.1.1.2.143 A53SS_APBADDR_DBG_CPU0_EDDEVID2 Register

1 A53SS_APBADDR_DBG_CPU0_EDDEVID2 Register (Offset = FC0h) [reset = 0h]

External Debug Device ID Register 2

Return to Summary Table

Table 14-8111. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FC0h**

Figure 14-2688. A53SS_APBADDR_DBG_CPU0_EDDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID2_31_0							
R/W							
0h							

Table 14-8113. A53SS_APBADDR_DBG_CPU0_EDDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.144 A53SS_APBADDR_DBG_CPU0_EDDEVID1 Register

1 A53SS_APBADDR_DBG_CPU0_EDDEVID1 Register (Offset = FC4h) [reset = 2h]

External Debug Device ID Register 1

Return to Summary Table

Table 14-8114. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FC4h**

Figure 14-2689. A53SS_APBADDR_DBG_CPU0_EDDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID1_31_4				PCSROFFSET			
R/W				R/W			
0h				2h			

Table 14-8116. A53SS_APBADDR_DBG_CPU0_EDDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDDEVID1_31_4	R/W	0h	Reserved, RES0.
3:0	PCSROFFSET	R/W	2h	This field indicates the offset applied to PC samples returned by reads of EDPCSR. Permitted values of this field in v8-A are: 0000 EDPCSR not implemented. 0010 EDPCSR implemented, and samples have no offset applied and do not sample the instruction set state in AArch32 state.

14.3.1.1.2.145 A53SS_APBADDR_DBG_CPU0_EDDEVID Register

1 A53SS_APBADDR_DBG_CPU0_EDDEVID Register (Offset = FC8h) [reset = 3h]

External Debug Device ID Register 0

Return to Summary Table

Table 14-8117. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FC8h**

Figure 14-2690. A53SS_APBADDR_DBG_CPU0_EDDEVID Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID_31_28				AUXREGS			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RES0_EDDEVID_23_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID_23_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID_23_4				PCSAMPLE			
R/W				R/W			
0h				3h			

Table 14-8119. A53SS_APBADDR_DBG_CPU0_EDDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_EDDEVID_31_28	R/W	0h	Reserved, RES0.
27:24	AUXREGS	R/W	0h	Indicates support for Auxiliary registers. Permitted values for this field are: 0000 None supported. 0001 Support for External Debug Auxiliary Control Register, EDACR. All other values are reserved.
23:4	RES0_EDDEVID_23_4	R/W	0h	Reserved, RES0.
3:0	PCSAMPLE	R/W	3h	Indicates the level of Sample-based profiling support using external debug registers 40 through 43. Permitted values of this field in v8-A are: 0000 Architecture-defined form of Sample-based profiling not implemented. 0010 EDPCSR and EDCIDSR are implemented [only permitted if EL3 and EL2 are not implemented]. 0011 EDPCSR, EDCIDSR, and EDVIDSR are implemented. All other values are reserved.

14.3.1.1.2.146 A53SS_APBADDR_DBG_CPU0_EDDEVTYPE Register

1 A53SS_APBADDR_DBG_CPU0_EDDEVTYPE Register (Offset = FCCh) [reset = 15h]

External Debug Device Type Register

Return to Summary Table

Table 14-8120. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FCCh**

Figure 14-2691. A53SS_APBADDR_DBG_CPU0_EDDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				5h			

Table 14-8122. A53SS_APBADDR_DBG_CPU0_EDDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	5h	Major type. Must read as 0x5 to indicate this is a debug logic component.

14.3.1.1.2.147 A53SS_APBADDR_DBG_CPU0_EDPIDR4 Register

1 A53SS_APBADDR_DBG_CPU0_EDPIDR4 Register (Offset = FD0h) [reset = 4h]

External Debug Peripheral Identification Register 4

Return to Summary Table

Table 14-8123. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FD0h**

Figure 14-2692. A53SS_APBADDR_DBG_CPU0_EDPIDR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDPIDR4_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SIZE</td><td colspan="4">DES_2</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-8125. A53SS_APBADDR_DBG_CPU0_EDPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.148 A53SS_APBADDR_DBG_CPU0_EDPIDR0 Register

1 A53SS_APBADDR_DBG_CPU0_EDPIDR0 Register (Offset = FE0h) [reset = 3h]

External Debug Peripheral Identification Register 0

Return to Summary Table

Table 14-8126. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FE0h**

Figure 14-2693. A53SS_APBADDR_DBG_CPU0_EDPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
3h							

Table 14-8128. A53SS_APBADDR_DBG_CPU0_EDPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	3h	Part number, least significant byte.

14.3.1.1.2.149 A53SS_APBADDR_DBG_CPU0_EDPIDR1 Register

1 A53SS_APBADDR_DBG_CPU0_EDPIDR1 Register (Offset = FE4h) [reset = BDh]

External Debug Peripheral Identification Register 1

Return to Summary Table

Table 14-8129. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FE4h**

Figure 14-2694. A53SS_APBADDR_DBG_CPU0_EDPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				Dh			

Table 14-8131. A53SS_APBADDR_DBG_CPU0_EDPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	Dh	Part number, most significant nibble.

14.3.1.1.2.150 A53SS_APBADDR_DBG_CPU0_EDPIDR2 Register

1 A53SS_APBADDR_DBG_CPU0_EDPIDR2 Register (Offset = FE8h) [reset = 4Bh]

External Debug Peripheral Identification Register 2

Return to Summary Table

Table 14-8132. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FE8h**

Figure 14-2695. A53SS_APBADDR_DBG_CPU0_EDPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-8134. A53SS_APBADDR_DBG_CPU0_EDPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.151 A53SS_APBADDR_DBG_CPU0_EDPIDR3 Register

1 A53SS_APBADDR_DBG_CPU0_EDPIDR3 Register (Offset = FECh) [reset = 0h]

External Debug Peripheral Identification Register 3

Return to Summary Table

Table 14-8135. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FECh**

Figure 14-2696. A53SS_APBADDR_DBG_CPU0_EDPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-8137. A53SS_APBADDR_DBG_CPU0_EDPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using EDPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.152 A53SS_APBADDR_DBG_CPU0_EDCIDR0 Register

1 A53SS_APBADDR_DBG_CPU0_EDCIDR0 Register (Offset = FF0h) [reset = Dh]

External Debug Component Identification Register 0

Return to Summary Table

Table 14-8138. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FF0h**

Figure 14-2697. A53SS_APBADDR_DBG_CPU0_EDCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDCIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDCIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRMBL_0							
R/W							
Dh							

Table 14-8140. A53SS_APBADDR_DBG_CPU0_EDCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.153 A53SS_APBADDR_DBG_CPU0_EDCIDR1 Register

1 A53SS_APBADDR_DBG_CPU0_EDCIDR1 Register (Offset = FF4h) [reset = 90h]

External Debug Component Identification Register 1

Return to Summary Table

Table 14-8141. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FF4h**

Figure 14-2698. A53SS_APBADDR_DBG_CPU0_EDCIDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDCIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDCIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDCIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CLASS</td><td colspan="4">PRMBL_1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8143. A53SS_APBADDR_DBG_CPU0_EDCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.154 A53SS_APBADDR_DBG_CPU0_EDCIDR2 Register

1 A53SS_APBADDR_DBG_CPU0_EDCIDR2 Register (Offset = FF8h) [reset = 5h]

External Debug Component Identification Register 2

Return to Summary Table

Table 14-8144. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FF8h**

Figure 14-2699. A53SS_APBADDR_DBG_CPU0_EDCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-8146. A53SS_APBADDR_DBG_CPU0_EDCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.155 A53SS_APBADDR_DBG_CPU0_EDCIDR3 Register

1 A53SS_APBADDR_DBG_CPU0_EDCIDR3 Register (Offset = FFCh) [reset = B1h]

External Debug Component Identification Register 3

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Table 14-8147. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3001 0FFCh**

Figure 14-2700. A53SS_APBADDR_DBG_CPU0_EDCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-8149. A53SS_APBADDR_DBG_CPU0_EDCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.156 A53SS_APBADDR_CTI_CPU0_CTICONTROL Register

1 A53SS_APBADDR_CTI_CPU0_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register

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Table 14-8150. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0000h**

Figure 14-2701. A53SS_APBADDR_CTI_CPU0_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RES0_CTICONTROL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICONTROL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICONTROL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTICONTROL_31_1							GLBEN
R/W							R/W
0h							0h

Table 14-8152. A53SS_APBADDR_CTI_CPU0_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTICONTROL_31_1	R/W	0h	Reserved, RES0.
0	GLBEN	R/W	0h	Enables or disables the CTI mapping functions. Possible values of this field are: 0 CTI mapping functions disabled. 1 CTI mapping functions enabled. When the mapping functions are disabled, no new events are signaled on either output triggers or output channels. If a previously asserted output trigger has not been acknowledged, it remains asserted after the mapping functions are disabled. All output triggers are disabled by CTI reset.

14.3.1.1.2.157 A53SS_APBADDR_CTI_CPU0_CTIINTACK Register

1 A53SS_APBADDR_CTI_CPU0_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Output Trigger Acknowledge Register

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Table 14-8153. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0010h**

Figure 14-2702. A53SS_APBADDR_CTI_CPU0_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINTACK_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINTACK_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINTACK_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ACK_N							
R/W							
0h							

Table 14-8155. A53SS_APBADDR_CTI_CPU0_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTIINTACK_31_8	R/W	0h	Reserved RES0
7:0	ACK_N	R/W	0h	Can be used to create soft acknowledges for output triggers

14.3.1.1.2.158 A53SS_APBADDR_CTI_CPU0_CTIAPPSET Register

1 A53SS_APBADDR_CTI_CPU0_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register

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Table 14-8156. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0014h**

Figure 14-2703. A53SS_APBADDR_CTI_CPU0_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPSET_31_4				CTIAPPSETX			
R/W				R/W			
0h				0h			

Table 14-8158. A53SS_APBADDR_CTI_CPU0_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPSET_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPSETX	R/W	0h	Application trigger <x> enable

14.3.1.1.2.159 A53SS_APBADDR_CTI_CPU0_CTIAPPCLEAR Register

1 A53SS_APBADDR_CTI_CPU0_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register

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Table 14-8159. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0018h**

Figure 14-2704. A53SS_APBADDR_CTI_CPU0_CTIAPPCLEAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPCLEAR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPCLEAR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPCLEAR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIAPPCLEAR_31_4</td><td colspan="4">CTIAPPCLEARX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8161. A53SS_APBADDR_CTI_CPU0_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPCLEAR_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPCLEARX	R/W	0h	Application trigger <x> disable

14.3.1.1.2.160 A53SS_APBADDR_CTI_CPU0_CTIAPPPULSE Register

1 A53SS_APBADDR_CTI_CPU0_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Pulse Register

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Table 14-8162. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 001Ch**

Figure 14-2705. A53SS_APBADDR_CTI_CPU0_CTIAPPPULSE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPPULSE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPPULSE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPPULSE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIAPPPULSE_31_4</td><td colspan="4">CTIAPPPULSEX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8164. A53SS_APBADDR_CTI_CPU0_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPPULSE_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPPULSEX	R/W	0h	Generate event pulse on ECT channel <x>.

14.3.1.1.2.161 A53SS_APBADDR_CTI_CPU0_CTIINEN0 Register

1 A53SS_APBADDR_CTI_CPU0_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 0

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Table 14-8165. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0020h**

Figure 14-2706. A53SS_APBADDR_CTI_CPU0_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN0_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN0_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN0_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN0_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-8167. A53SS_APBADDR_CTI_CPU0_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN0_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 0 to output channel <x> enable

14.3.1.1.2.162 A53SS_APBADDR_CTI_CPU0_CTIINEN1 Register

1 A53SS_APBADDR_CTI_CPU0_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 1

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Table 14-8168. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0024h**

Figure 14-2707. A53SS_APBADDR_CTI_CPU0_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN1_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN1_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN1_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN1_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-8170. A53SS_APBADDR_CTI_CPU0_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN1_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 1 to output channel <x> enable

14.3.1.1.2.163 A53SS_APBADDR_CTI_CPU0_CTIINEN2 Register

1 A53SS_APBADDR_CTI_CPU0_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 2

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Table 14-8171. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0028h**

Figure 14-2708. A53SS_APBADDR_CTI_CPU0_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN2_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN2_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN2_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN2_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-8173. A53SS_APBADDR_CTI_CPU0_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN2_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 2 to output channel <x> enable

14.3.1.1.2.164 A53SS_APBADDR_CTI_CPU0_CTIINEN3 Register

1 A53SS_APBADDR_CTI_CPU0_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 3

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Table 14-8174. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 002Ch**

Figure 14-2709. A53SS_APBADDR_CTI_CPU0_CTIINEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN3_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN3_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN3_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIINEN3_31_4</td><td colspan="4">INENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8176. A53SS_APBADDR_CTI_CPU0_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN3_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 3 to output channel <x> enable

14.3.1.1.2.165 A53SS_APBADDR_CTI_CPU0_CTIINEN4 Register

1 A53SS_APBADDR_CTI_CPU0_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 4

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Table 14-8177. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0030h**

Figure 14-2710. A53SS_APBADDR_CTI_CPU0_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN4_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-8179. A53SS_APBADDR_CTI_CPU0_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN4_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 4 to output channel <x> enable

14.3.1.1.2.166 A53SS_APBADDR_CTI_CPU0_CTIINEN5 Register

1 A53SS_APBADDR_CTI_CPU0_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 5

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Table 14-8180. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0034h**

Figure 14-2711. A53SS_APBADDR_CTI_CPU0_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN5_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN5_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN5_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN5_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-8182. A53SS_APBADDR_CTI_CPU0_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN5_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 5 to output channel <x> enable

14.3.1.1.2.167 A53SS_APBADDR_CTI_CPU0_CTIINEN6 Register

1 A53SS_APBADDR_CTI_CPU0_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 6

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Table 14-8183. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0038h**

Figure 14-2712. A53SS_APBADDR_CTI_CPU0_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN6_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN6_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN6_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN6_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-8185. A53SS_APBADDR_CTI_CPU0_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN6_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 6 to output channel <x> enable

14.3.1.1.2.168 A53SS_APBADDR_CTI_CPU0_CTIINEN7 Register

1 A53SS_APBADDR_CTI_CPU0_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 7

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Table 14-8186. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 003Ch**

Figure 14-2713. A53SS_APBADDR_CTI_CPU0_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN7_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN7_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN7_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN7_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-8188. A53SS_APBADDR_CTI_CPU0_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN7_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 7 to output channel <x> enable

14.3.1.1.2.169 A53SS_APBADDR_CTI_CPU0_CTIOUTEN0 Register

1 A53SS_APBADDR_CTI_CPU0_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 0

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Table 14-8189. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00A0h**

Figure 14-2714. A53SS_APBADDR_CTI_CPU0_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN0_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-8191. A53SS_APBADDR_CTI_CPU0_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN0_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 0 enable

14.3.1.1.2.170 A53SS_APBADDR_CTI_CPU0_CTIOUTEN1 Register

1 A53SS_APBADDR_CTI_CPU0_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 1

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Table 14-8192. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00A4h**

Figure 14-2715. A53SS_APBADDR_CTI_CPU0_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN1_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-8194. A53SS_APBADDR_CTI_CPU0_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN1_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 1 enable

14.3.1.1.2.171 A53SS_APBADDR_CTI_CPU0_CTIOUTEN2 Register

1 A53SS_APBADDR_CTI_CPU0_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 2

Return to Summary Table

Table 14-8195. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00A8h**

Figure 14-2716. A53SS_APBADDR_CTI_CPU0_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN2_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN2_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-8197. A53SS_APBADDR_CTI_CPU0_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN2_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 2 enable

14.3.1.1.2.172 A53SS_APBADDR_CTI_CPU0_CTIOUTEN3 Register

1 A53SS_APBADDR_CTI_CPU0_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 3

Return to Summary Table

Table 14-8198. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00ACh**

Figure 14-2717. A53SS_APBADDR_CTI_CPU0_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN3_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-8200. A53SS_APBADDR_CTI_CPU0_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN3_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 3 enable

14.3.1.1.2.173 A53SS_APBADDR_CTI_CPU0_CTIOUTEN4 Register

1 A53SS_APBADDR_CTI_CPU0_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 4

Return to Summary Table

Table 14-8201. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00B0h**

Figure 14-2718. A53SS_APBADDR_CTI_CPU0_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN4_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-8203. A53SS_APBADDR_CTI_CPU0_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN4_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 4 enable

14.3.1.1.2.174 A53SS_APBADDR_CTI_CPU0_CTIOUTEN5 Register

1 A53SS_APBADDR_CTI_CPU0_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 5

Return to Summary Table

Table 14-8204. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00B4h**

Figure 14-2719. A53SS_APBADDR_CTI_CPU0_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN5_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-8206. A53SS_APBADDR_CTI_CPU0_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN5_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 5 enable

14.3.1.1.2.175 A53SS_APBADDR_CTI_CPU0_CTIOUTEN6 Register

1 A53SS_APBADDR_CTI_CPU0_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 6

Return to Summary Table

Table 14-8207. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00B8h**

Figure 14-2720. A53SS_APBADDR_CTI_CPU0_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN6_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-8209. A53SS_APBADDR_CTI_CPU0_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN6_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 6 enable

14.3.1.1.2.176 A53SS_APBADDR_CTI_CPU0_CTIOUTEN7 Register

1 A53SS_APBADDR_CTI_CPU0_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 7

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Table 14-8210. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 00BCh**

Figure 14-2721. A53SS_APBADDR_CTI_CPU0_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN7_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-8212. A53SS_APBADDR_CTI_CPU0_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN7_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 7 enable

14.3.1.1.2.177 A53SS_APBADDR_CTI_CPU0_CTITRIGINSTATUS Register

1 A53SS_APBADDR_CTI_CPU0_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

Return to Summary Table

Table 14-8213. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0130h**

Figure 14-2722. A53SS_APBADDR_CTI_CPU0_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
TRINN							
R/W							
0h							

Table 14-8215. A53SS_APBADDR_CTI_CPU0_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGINSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TRINN	R/W	0h	Provides the status of the trigger inputs

14.3.1.1.2.178 A53SS_APBADDR_CTI_CPU0_CTITRIGOUTSTATUS Register

1 A53SS_APBADDR_CTI_CPU0_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

Return to Summary Table

Table 14-8216. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0134h**

Figure 14-2723. A53SS_APBADDR_CTI_CPU0_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
TROUTN							
R/W							
0h							

Table 14-8218. A53SS_APBADDR_CTI_CPU0_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGOUTSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TROUTN	R/W	0h	Provides the status of the trigger outputs

14.3.1.1.2.179 A53SS_APBADDR_CTI_CPU0_CTICHINSTATUS Register

1 A53SS_APBADDR_CTI_CPU0_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

Return to Summary Table

Table 14-8219. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0138h**

Figure 14-2724. A53SS_APBADDR_CTI_CPU0_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICHINSTATUS_31_4				CHINN			
R/W				R/W			
0h				0h			

Table 14-8221. A53SS_APBADDR_CTI_CPU0_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHINSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHINN	R/W	0h	Provides the raw status of the ECT channel inputs to the CTI

14.3.1.1.2.180 A53SS_APBADDR_CTI_CPU0_CTICHOUTSTATUS Register

1 A53SS_APBADDR_CTI_CPU0_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

Return to Summary Table

Table 14-8222. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 013Ch**

Figure 14-2725. A53SS_APBADDR_CTI_CPU0_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTICHOUTSTATUS_31_4				CHOUTN			
R/W				R/W			
0h				0h			

Table 14-8224. A53SS_APBADDR_CTI_CPU0_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHOUTSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHOUTN	R/W	0h	Provides the status of the ECT channel outputs from the CTI

14.3.1.1.2.181 A53SS_APBADDR_CTI_CPU0_CTIGATE Register

1 A53SS_APBADDR_CTI_CPU0_CTIGATE Register (Offset = 140h) [reset = Fh]

CTI Channel Gate Enable Register

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Table 14-8225. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0140h**

Figure 14-2726. A53SS_APBADDR_CTI_CPU0_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIGATE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIGATE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIGATE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIGATE_31_4				GATEX			
R/W				R/W			
0h				Fh			

Table 14-8227. A53SS_APBADDR_CTI_CPU0_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIGATE_31_4	R/W	0h	Reserved RES0
3:0	GATEX	R/W	Fh	Determines whether events on channels propagate through the CTM to other ECT components or from the CTM into the CTI

14.3.1.1.2.182 A53SS_APBADDR_CTI_CPU0_ASICCTL Register

1 A53SS_APBADDR_CTI_CPU0_ASICCTL Register (Offset = 144h) [reset = 0h]

CTI External Multiplexor Control register

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Table 14-8228. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0144h**

Figure 14-2727. A53SS_APBADDR_CTI_CPU0_ASICCTL Name Register

31	30	29	28	27	26	25	24
RES0_ASICCTL_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ASICCTL_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ASICCTL_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-8230. A53SS_APBADDR_CTI_CPU0_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_ASICCTL_31_8	R/W	0h	Reserved, RES0.
7:0	ASICCTL	R/W	0h	IMPLEMENTATION DEFINED ASIC control. Provides a control for external multiplexing of additional triggers into the CTI.If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected in CTIDEVID.EXTMUXNUM.If CTIDEVID.EXTMUXNUM is zero, this field is RAZ.

14.3.1.1.2.183 A53SS_APBADDR_CTI_CPU0_CTIITCTRL Register

1 A53SS_APBADDR_CTI_CPU0_CTIITCTRL Register (Offset = F00h) [reset = 0h]

CTI Integration mode Control Register

Return to Summary Table

Table 14-8231. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0F00h**

Figure 14-2728. A53SS_APBADDR_CTI_CPU0_CTIITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_CTIITCTRL_31_1							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_CTIITCTRL_31_1							
R/W							
0h							

15	14	13	12	11	10	9	8
RES0_CTIITCTRL_31_1							
R/W							
0h							

7	6	5	4	3	2	1	0
RES0_CTIITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-8233. A53SS_APBADDR_CTI_CPU0_CTIITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTIITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.184 A53SS_APBADDR_CTI_CPU0_CTICLAIMSET Register

1 A53SS_APBADDR_CTI_CPU0_CTICLAIMSET Register (Offset = FA0h) [reset = Fh]

CTI Claim Set

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Table 14-8234. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FA0h**

Figure 14-2729. A53SS_APBADDR_CTI_CPU0_CTICLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICLAIMSET_31_4				CLAIMX			
R/W				R/W			
0h				Fh			

Table 14-8236. A53SS_APBADDR_CTI_CPU0_CTICLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	Fh	CLAIM tag set bit

14.3.1.1.2.185 A53SS_APBADDR_CTI_CPU0_CTICLAIMCLR Register

1 A53SS_APBADDR_CTI_CPU0_CTICLAIMCLR Register (Offset = FA4h) [reset = 0h]

CTI Claim Clear

Return to Summary Table

Table 14-8237. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FA4h**

Figure 14-2730. A53SS_APBADDR_CTI_CPU0_CTICLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTICLAIMCLR_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTICLAIMCLR_31_4</td><td colspan="4">CLAIMX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8239. A53SS_APBADDR_CTI_CPU0_CTICLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	0h	Clear CLAIM tag

14.3.1.1.2.186 A53SS_APBADDR_CTI_CPU0_CTIDEVAFF0 Register

1 A53SS_APBADDR_CTI_CPU0_CTIDEVAFF0 Register (Offset = FA8h) [reset = 80000000h]

CTI Device Affinity Register 0

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Table 14-8240. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FA8h**

Figure 14-2731. A53SS_APBADDR_CTI_CPU0_CTIDEVAFF0 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF0							
R/W							
80000000h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CTIDEVAFF0							
R/W							
80000000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CTIDEVAFF0							
R/W							
80000000h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTIDEVAFF0							
R/W							
80000000h							

Table 14-8242. A53SS_APBADDR_CTI_CPU0_CTIDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF0	R/W	80000000h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.187 A53SS_APBADDR_CTI_CPU0_CTIDEVAFF1 Register

1 A53SS_APBADDR_CTI_CPU0_CTIDEVAFF1 Register (Offset = FACh) [reset = 0h]

CTI Device Affinity Register 1

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Table 14-8243. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FACh**

Figure 14-2732. A53SS_APBADDR_CTI_CPU0_CTIDEVAFF1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CTIDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CTIDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CTIDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTIDEVAFF1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8245. A53SS_APBADDR_CTI_CPU0_CTIDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.188 A53SS_APBADDR_CTI_CPU0_CTILAR Register

1 A53SS_APBADDR_CTI_CPU0_CTILAR Register (Offset = FB0h) [reset = 0h]

CTI Lock Access Register

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Table 14-8246. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FB0h**

Figure 14-2733. A53SS_APBADDR_CTI_CPU0_CTILAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-8248. A53SS_APBADDR_CTI_CPU0_CTILAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.189 A53SS_APBADDR_CTI_CPU0_CTILSR Register

1 A53SS_APBADDR_CTI_CPU0_CTILSR Register (Offset = FB4h) [reset = 0h]

CTI Lock Status Register

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Table 14-8249. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FB4h**

Figure 14-2734. A53SS_APBADDR_CTI_CPU0_CTILSR Name Register

31	30	29	28	27	26	25	24
RES0_CTILSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTILSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTILSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTILSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-8251. A53SS_APBADDR_CTI_CPU0_CTILSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_CTILSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.190 A53SS_APBADDR_CTI_CPU0_CTIAUTHSTATUS Register

1 A53SS_APBADDR_CTI_CPU0_CTIAUTHSTATUS Register (Offset = FB8h) [reset = Ah]

CTI Authentication Status Register

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Table 14-8252. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FB8h**

Figure 14-2735. A53SS_APBADDR_CTI_CPU0_CTIAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTIAUTHSTATUS_31_4				NSNID		NSID	
R/W				R/W		R/W	
0h				2h		2h	

Table 14-8254. A53SS_APBADDR_CTI_CPU0_CTIAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_CTIAUTHSTATUS_31_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SNID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	NSID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSID.

14.3.1.1.2.191 A53SS_APBADDR_CTI_CPU0_CTIDEVARCH Register

1 A53SS_APBADDR_CTI_CPU0_CTIDEVARCH Register (Offset = FBCh) [reset = 47701A14h]

CTI Device Architecture Register

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Table 14-8255. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FBCh**

Figure 14-2736. A53SS_APBADDR_CTI_CPU0_CTIDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1A14h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1A14h</td></tr>
</table>

Table 14-8257. A53SS_APBADDR_CTI_CPU0_CTIDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For CTI, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For CTI, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	1A14h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For CTI:Bits [15:12] are the architecture version, 0x1.Bits [11:0] are the architecture part number, 0xA14.This corresponds to CTI architecture version CTIv2.

14.3.1.1.2.192 A53SS_APBADDR_CTI_CPU0_CTIDEVID2 Register

1 A53SS_APBADDR_CTI_CPU0_CTIDEVID2 Register (Offset = FC0h) [reset = 0h]

CTI Device ID Register 2

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Table 14-8258. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FC0h**

Figure 14-2737. A53SS_APBADDR_CTI_CPU0_CTIDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID2_31_0							
R/W							
0h							

Table 14-8260. A53SS_APBADDR_CTI_CPU0_CTIDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.193 A53SS_APBADDR_CTI_CPU0_CTIDEVID1 Register

1 A53SS_APBADDR_CTI_CPU0_CTIDEVID1 Register (Offset = FC4h) [reset = 0h]

CTI Device ID Register 1

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Table 14-8261. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FC4h**

Figure 14-2738. A53SS_APBADDR_CTI_CPU0_CTIDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID1_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIDEVID1_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIDEVID1_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTIDEVID1_31_0							
R/W							
0h							

Table 14-8263. A53SS_APBADDR_CTI_CPU0_CTIDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID1_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.194 A53SS_APBADDR_CTI_CPU0_CTIDEVID Register

1 A53SS_APBADDR_CTI_CPU0_CTIDEVID Register (Offset = FC8h) [reset = 1040800h]

CTI Device ID Register 0

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Table 14-8264. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FC8h**

Figure 14-2739. A53SS_APBADDR_CTI_CPU0_CTIDEVID Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID_31_26						INOUT	
R/W						R/W	
0h						1h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIDEVID_23_22		NUMCHAN					
R/W		R/W					
0h		4h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIDEVID_15_14		NUMTRIG					
R/W		R/W					
0h		8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTIDEVID_7_5			EXTMUXNUM				
R/W			R/W				
0h			0h				

Table 14-8266. A53SS_APBADDR_CTI_CPU0_CTIDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES0_CTIDEVID_31_26	R/W	0h	Reserved, RES0.
25:24	INOUT	R/W	1h	Input/output options. Indicates presence of the input gate. If the CTM is not implemented, this field is RAZ. 00 CTIGATE does not mask propagation of input events from external channels. 01 CTIGATE masks propagation of input events from external channels. All other values are reserved.
23:22	RES0_CTIDEVID_23_22	R/W	0h	Reserved, RES0.
21:16	NUMCHAN	R/W	4h	Number of ECT channels implemented. IMPLEMENTATION DEFINED. For v8-A, valid values are: 000011 3 channels [0..2] implemented. 000100 4 channels [0..3] implemented. 000101 5 channels [0..4] implemented. 000110 6 channels [0..5] implemented. and so on up to 0b100000, 32 channels [0..31] implemented.All other values are reserved.
15:14	RES0_CTIDEVID_15_14	R/W	0h	Reserved, RES0.

Table 14-8266. A53SS_APBADDR_CTI_CPU0_CTIDEVID Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	NUMTRIG	R/W	8h	Number of triggers implemented. IMPLEMENTATION DEFINED. This is one more than the index of the largest trigger, rather than the actual number of triggers.For v8-A, valid values are: 000011 Up to 3 triggers [0..2] implemented. 001000 Up to 8 triggers [0..7] implemented. 001001 Up to 9 triggers [0..8] implemented. 001010 Up to 10 triggers [0..9] implemented. and so on up to 0b100000, 32 triggers [0..31] implemented.All other values are reserved. If the Trace Extension is implemented, this field must be at least 001000. There is no guarantee that any of the implemented triggers, including the highest numbered, are connected to any components.
7:5	RES0_CTIDEVID_7_5	R/W	0h	Reserved, RES0.
4:0	EXTMUXNUM	R/W	0h	Maximum number of external triggers available for multiplexing into the CTI. This relates only to additional external triggers outside those defined for v8-A.

14.3.1.1.2.195 A53SS_APBADDR_CTI_CPU0_CTIDEVTYPE Register

1 A53SS_APBADDR_CTI_CPU0_CTIDEVTYPE Register (Offset = FCCh) [reset = 14h]

CTI Device Type Register

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Table 14-8267. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FCCh**

Figure 14-2740. A53SS_APBADDR_CTI_CPU0_CTIDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAJOR			
R/W				R/W			
1h				4h			

Table 14-8269. A53SS_APBADDR_CTI_CPU0_CTIDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	4h	Major type. Must read as 0x4 to indicate this is a cross-trigger component.

14.3.1.1.2.196 A53SS_APBADDR_CTI_CPU0_CTIPIDR4 Register

1 A53SS_APBADDR_CTI_CPU0_CTIPIDR4 Register (Offset = FD0h) [reset = 4h]

CTI Peripheral Identification Register 4

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Table 14-8270. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FD0h**

Figure 14-2741. A53SS_APBADDR_CTI_CPU0_CTIPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-8272. A53SS_APBADDR_CTI_CPU0_CTIPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.197 A53SS_APBADDR_CTI_CPU0_CTIPIDR5 Register

1 A53SS_APBADDR_CTI_CPU0_CTIPIDR5 Register (Offset = FD4h) [reset = 0h]

CTI Peripheral Identification Register 5

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Table 14-8273. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FD4h**

Figure 14-2742. A53SS_APBADDR_CTI_CPU0_CTIPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR5_31_0							
R/W							
0h							

Table 14-8275. A53SS_APBADDR_CTI_CPU0_CTIPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.198 A53SS_APBADDR_CTI_CPU0_CTIPIDR6 Register

1 A53SS_APBADDR_CTI_CPU0_CTIPIDR6 Register (Offset = FD8h) [reset = 0h]

CTI Peripheral Identification Register 6

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Table 14-8276. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FD8h**

Figure 14-2743. A53SS_APBADDR_CTI_CPU0_CTIPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIPIDR6_31_0							
R/W							
0h							

Table 14-8278. A53SS_APBADDR_CTI_CPU0_CTIPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.199 A53SS_APBADDR_CTI_CPU0_CTIPIDR7 Register

1 A53SS_APBADDR_CTI_CPU0_CTIPIDR7 Register (Offset = FDCh) [reset = 0h]

CTI Peripheral Identification Register 7

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Table 14-8279. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FDCh**

Figure 14-2744. A53SS_APBADDR_CTI_CPU0_CTIPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIPIDR7_31_0							
R/W							
0h							

Table 14-8281. A53SS_APBADDR_CTI_CPU0_CTIPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.200 A53SS_APBADDR_CTI_CPU0_CTIPIDR0 Register

1 A53SS_APBADDR_CTI_CPU0_CTIPIDR0 Register (Offset = FE0h) [reset = A8h]

CTI Peripheral Identification Register 0

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Table 14-8282. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FE0h**

Figure 14-2745. A53SS_APBADDR_CTI_CPU0_CTIPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
A8h							

Table 14-8284. A53SS_APBADDR_CTI_CPU0_CTIPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	A8h	Part number, least significant byte.

14.3.1.1.2.201 A53SS_APBADDR_CTI_CPU0_CTIPIDR1 Register

1 A53SS_APBADDR_CTI_CPU0_CTIPIDR1 Register (Offset = FE4h) [reset = B9h]

CTI Peripheral Identification Register 1

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Table 14-8285. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FE4h**

Figure 14-2746. A53SS_APBADDR_CTI_CPU0_CTIPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-8287. A53SS_APBADDR_CTI_CPU0_CTIPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.202 A53SS_APBADDR_CTI_CPU0_CTIPIDR2 Register

1 A53SS_APBADDR_CTI_CPU0_CTIPIDR2 Register (Offset = FE8h) [reset = 4Bh]

CTI Peripheral Identification Register 2

Return to Summary Table

Table 14-8288. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FE8h**

Figure 14-2747. A53SS_APBADDR_CTI_CPU0_CTIPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-8290. A53SS_APBADDR_CTI_CPU0_CTIPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.203 A53SS_APBADDR_CTI_CPU0_CTIPIDR3 Register

1 A53SS_APBADDR_CTI_CPU0_CTIPIDR3 Register (Offset = FECh) [reset = 0h]

CTI Peripheral Identification Register 3

Return to Summary Table

Table 14-8291. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FECh**

Figure 14-2748. A53SS_APBADDR_CTI_CPU0_CTIPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-8293. A53SS_APBADDR_CTI_CPU0_CTIPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using CTIPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.204 A53SS_APBADDR_CTI_CPU0_CTICIDR0 Register

1 A53SS_APBADDR_CTI_CPU0_CTICIDR0 Register (Offset = FF0h) [reset = Dh]

CTI Component Identification Register 0

Return to Summary Table

Table 14-8294. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FF0h**

Figure 14-2749. A53SS_APBADDR_CTI_CPU0_CTICIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-8296. A53SS_APBADDR_CTI_CPU0_CTICIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.205 A53SS_APBADDR_CTI_CPU0_CTICIDR1 Register

1 A53SS_APBADDR_CTI_CPU0_CTICIDR1 Register (Offset = FF4h) [reset = 90h]

CTI Component Identification Register 1

Return to Summary Table

Table 14-8297. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FF4h**

Figure 14-2750. A53SS_APBADDR_CTI_CPU0_CTICIDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTICIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTICIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTICIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CLASS</td><td colspan="4">PRMBL_1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8299. A53SS_APBADDR_CTI_CPU0_CTICIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.206 A53SS_APBADDR_CTI_CPU0_CTICIDR2 Register

1 A53SS_APBADDR_CTI_CPU0_CTICIDR2 Register (Offset = FF8h) [reset = 5h]

CTI Component Identification Register 2

Return to Summary Table

Table 14-8300. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FF8h**

Figure 14-2751. A53SS_APBADDR_CTI_CPU0_CTICIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-8302. A53SS_APBADDR_CTI_CPU0_CTICIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.207 A53SS_APBADDR_CTI_CPU0_CTICIDR3 Register

1 A53SS_APBADDR_CTI_CPU0_CTICIDR3 Register (Offset = FFCh) [reset = B1h]

CTI Component Identification Register 3

Return to Summary Table

Table 14-8303. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3002 0FFCh**

Figure 14-2752. A53SS_APBADDR_CTI_CPU0_CTICIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-8305. A53SS_APBADDR_CTI_CPU0_CTICIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.208 A53SS_APBADDR_PMU_CPU0_PMEVCNTR0_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVCNTR0_EL0 Register (Offset = 0h) [reset = 0h]

Performance Monitors Event Count Register 0

Return to Summary Table

Table 14-8306. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0000h**

Figure 14-2753. A53SS_APBADDR_PMU_CPU0_PMEVCNTR0_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR0_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR0_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR0_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR0_EL0							
R/W							
0h							

Table 14-8308. A53SS_APBADDR_PMU_CPU0_PMEVCNTR0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR0_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.209 A53SS_APBADDR_PMU_CPU0_PMEVCNTR1_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVCNTR1_EL0 Register (Offset = 8h) [reset = 0h]

Performance Monitors Event Count Register 1

Return to Summary Table

Table 14-8309. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0008h**

Figure 14-2754. A53SS_APBADDR_PMU_CPU0_PMEVCNTR1_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR1_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR1_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR1_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR1_EL0							
R/W							
0h							

Table 14-8311. A53SS_APBADDR_PMU_CPU0_PMEVCNTR1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR1_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.210 A53SS_APBADDR_PMU_CPU0_PMEVCNTR2_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVCNTR2_EL0 Register (Offset = 10h) [reset = 0h]

Performance Monitors Event Count Register 2

Return to Summary Table

Table 14-8312. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0010h**

Figure 14-2755. A53SS_APBADDR_PMU_CPU0_PMEVCNTR2_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR2_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR2_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR2_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR2_EL0							
R/W							
0h							

Table 14-8314. A53SS_APBADDR_PMU_CPU0_PMEVCNTR2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR2_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.211 A53SS_APBADDR_PMU_CPU0_PMEVCNTR3_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVCNTR3_EL0 Register (Offset = 18h) [reset = 0h]

Performance Monitors Event Count Register 3

Return to Summary Table

Table 14-8315. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0018h**

Figure 14-2756. A53SS_APBADDR_PMU_CPU0_PMEVCNTR3_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR3_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR3_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR3_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR3_EL0							
R/W							
0h							

Table 14-8317. A53SS_APBADDR_PMU_CPU0_PMEVCNTR3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR3_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.212 A53SS_APBADDR_PMU_CPU0_PMEVCNTR4_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVCNTR4_EL0 Register (Offset = 20h) [reset = 0h]

Performance Monitors Event Count Register 4

Return to Summary Table

Table 14-8318. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0020h**

Figure 14-2757. A53SS_APBADDR_PMU_CPU0_PMEVCNTR4_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR4_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR4_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR4_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR4_EL0							
R/W							
0h							

Table 14-8320. A53SS_APBADDR_PMU_CPU0_PMEVCNTR4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR4_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.213 A53SS_APBADDR_PMU_CPU0_PMEVCNTR5_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVCNTR5_EL0 Register (Offset = 28h) [reset = 0h]

Performance Monitors Event Count Register 5

Return to Summary Table

Table 14-8321. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0028h**

Figure 14-2758. A53SS_APBADDR_PMU_CPU0_PMEVCNTR5_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR5_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR5_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR5_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR5_EL0							
R/W							
0h							

Table 14-8323. A53SS_APBADDR_PMU_CPU0_PMEVCNTR5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR5_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.214 A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_31_0 Register

1 A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_31_0 Register (Offset = F8h) [reset = 0h]

Performance Monitors Cycle Counter (low word)

Return to Summary Table

Table 14-8324. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 00F8h**

Figure 14-2759. A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_31_0 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-8326. A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.215 A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_63_32 Register

1 A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_63_32 Register (Offset = FCh) [reset = 0h]

Performance Monitors Cycle Counter (high word)

Return to Summary Table

Table 14-8327. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 00FCh**

Figure 14-2760. A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_63_32 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-8329. A53SS_APBADDR_PMU_CPU0_PMCCNTR_EL0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.216 A53SS_APBADDR_PMU_CPU0_PMEVTYPER0_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVTYPER0_EL0 Register (Offset = 400h) [reset = 0h]

Performance Monitors Event Type Register 0

Return to Summary Table

Table 14-8330. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0400h**

Figure 14-2761. A53SS_APBADDR_PMU_CPU0_PMEVTYPER0_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER0_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER0_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER0_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-8332. A53SS_APBADDR_PMU_CPU0_PMEVTYPER0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-8332. A53SS_APBADDR_PMU_CPU0_PMEVTYPER0_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER0_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.217 A53SS_APBADDR_PMU_CPU0_PMEVTYPER1_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVTYPER1_EL0 Register (Offset = 404h) [reset = 0h]

Performance Monitors Event Type Register 1

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Table 14-8333. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0404h**

Figure 14-2762. A53SS_APBADDR_PMU_CPU0_PMEVTYPER1_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>P</td><td>U</td><td>NSK</td><td>NSU</td><td>NSH</td><td>M</td><td colspan="2">RES0_PMEVTYPER1_EL0_25_10</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMEVTYPER1_EL0_25_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RES0_PMEVTYPER1_EL0_25_10</td><td colspan="2">EVTCOUNT</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EVTCOUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8335. A53SS_APBADDR_PMU_CPU0_PMEVTYPER1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-8335. A53SS_APBADDR_PMU_CPU0_PMEVTYPER1_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER1_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.218 A53SS_APBADDR_PMU_CPU0_PMEVTYPER2_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVTYPER2_EL0 Register (Offset = 408h) [reset = 0h]

Performance Monitors Event Type Register 2

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Table 14-8336. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0408h**

Figure 14-2763. A53SS_APBADDR_PMU_CPU0_PMEVTYPER2_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER2_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER2_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER2_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-8338. A53SS_APBADDR_PMU_CPU0_PMEVTYPER2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-8338. A53SS_APBADDR_PMU_CPU0_PMEVTYPER2_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER2_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.219 A53SS_APBADDR_PMU_CPU0_PMEVTYPER3_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVTYPER3_EL0 Register (Offset = 40Ch) [reset = 0h]

Performance Monitors Event Type Register 3

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Table 14-8339. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 040Ch**

Figure 14-2764. A53SS_APBADDR_PMU_CPU0_PMEVTYPER3_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER3_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER3_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER3_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-8341. A53SS_APBADDR_PMU_CPU0_PMEVTYPER3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-8341. A53SS_APBADDR_PMU_CPU0_PMEVTYPER3_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER3_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.220 A53SS_APBADDR_PMU_CPU0_PMEVTYPER4_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVTYPER4_EL0 Register (Offset = 410h) [reset = 0h]

Performance Monitors Event Type Register 4

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Table 14-8342. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0410h**

Figure 14-2765. A53SS_APBADDR_PMU_CPU0_PMEVTYPER4_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER4_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER4_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER4_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-8344. A53SS_APBADDR_PMU_CPU0_PMEVTYPER4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-8344. A53SS_APBADDR_PMU_CPU0_PMEVTYPER4_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER4_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.221 A53SS_APBADDR_PMU_CPU0_PMEVTYPER5_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMEVTYPER5_EL0 Register (Offset = 414h) [reset = 0h]

Performance Monitors Event Type Register 5

Return to Summary Table

Table 14-8345. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0414h**

Figure 14-2766. A53SS_APBADDR_PMU_CPU0_PMEVTYPER5_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER5_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER5_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER5_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-8347. A53SS_APBADDR_PMU_CPU0_PMEVTYPER5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-8347. A53SS_APBADDR_PMU_CPU0_PMEVTYPER5_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER5_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.222 A53SS_APBADDR_PMU_CPU0_PMCCFILTR_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMCCFILTR_EL0 Register (Offset = 47Ch) [reset = 0h]

Performance Monitors Cycle Counter Filter Register

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Table 14-8348. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 047Ch**

Figure 14-2767. A53SS_APBADDR_PMU_CPU0_PMCCFILTR_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMCCFILTR_EL0_25_0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							

Table 14-8350. A53SS_APBADDR_PMU_CPU0_PMCCFILTR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count cycles in EL1. 1 Do not count cycles in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count cycles in EL0. 1 Do not count cycles in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Non-secure EL1 are counted.Otherwise, cycles in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, cycles in Non-secure EL0 are counted.Otherwise, cycles in Non-secure EL0 are not counted.

Table 14-8350. A53SS_APBADDR_PMU_CPU0_PMCCFILTR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count cycles in EL2. 1 Count cycles in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Secure EL3 are counted.Otherwise, cycles in Secure EL3 are not counted.
25:0	RES0_PMCCFILTR_EL0_25_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.223 A53SS_APBADDR_PMU_CPU0_PMCNTENSET_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMCNTENSET_EL0 Register (Offset = C00h) [reset = 0h]

Performance Monitors Count Enable Set Register

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Table 14-8351. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C00h**

Figure 14-2768. A53SS_APBADDR_PMU_CPU0_PMCNTENSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						

23	22	21	20	19	18	17	16
P_X							
R/W							
0h							

15	14	13	12	11	10	9	8
P_X							
R/W							
0h							

7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-8353. A53SS_APBADDR_PMU_CPU0_PMCNTENSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 enable bit. Enables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, enables the cycle counter.
30:0	P_X	R/W	0h	Event counter enable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> event counter is enabled. When written, enables PMEVCNTR<x>.

14.3.1.1.2.224 A53SS_APBADDR_PMU_CPU0_PMCNTENCLR_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMCNTENCLR_EL0 Register (Offset = C20h) [reset = 0h]

Performance Monitors Count Enable Clear Register

Return to Summary Table

Table 14-8354. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C20h**

Figure 14-2769. A53SS_APBADDR_PMU_CPU0_PMCNTENCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-8356. A53SS_APBADDR_PMU_CPU0_PMCNTENCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 disable bit. Disables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, disables the cycle counter.
30:0	P_X	R/W	0h	Event counter disable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> is enabled. When written, disables PMEVCNTR<x>.

14.3.1.1.2.225 A53SS_APBADDR_PMU_CPU0_PMINTENSET_EL1 Register

1 A53SS_APBADDR_PMU_CPU0_PMINTENSET_EL1 Register (Offset = C40h) [reset = 0h]

Performance Monitors Interrupt Enable Set Register

Return to Summary Table

Table 14-8357. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C40h**

Figure 14-2770. A53SS_APBADDR_PMU_CPU0_PMINTENSET_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-8359. A53SS_APBADDR_PMU_CPU0_PMINTENSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request enable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, enables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request enable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, enables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.226 A53SS_APBADDR_PMU_CPU0_PMINTENCLR_EL1 Register

1 A53SS_APBADDR_PMU_CPU0_PMINTENCLR_EL1 Register (Offset = C60h) [reset = 0h]

Performance Monitors Interrupt Enable Clear Register

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Table 14-8360. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C60h**

Figure 14-2771. A53SS_APBADDR_PMU_CPU0_PMINTENCLR_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-8362. A53SS_APBADDR_PMU_CPU0_PMINTENCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request disable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request disable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, disables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.227 A53SS_APBADDR_PMU_CPU0_PMOVSCLR_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMOVSCLR_EL0 Register (Offset = C80h) [reset = 0h]

Performance Monitors Overflow Flag Status Clear Register

Return to Summary Table

Table 14-8363. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0C80h**

Figure 14-2772. A53SS_APBADDR_PMU_CPU0_PMOVSCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-8365. A53SS_APBADDR_PMU_CPU0_PMOVSCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, clears the overflow bit to 0. PMCR_EL0.LC is used to control from which bit of PMCCNTR_EL0 [bit 31 or bit 63] an overflow is detected.
30:0	P_X	R/W	0h	Event counter overflow clear bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, clears the PMEVCNTR<x> overflow bit to 0.

14.3.1.1.2.228 A53SS_APBADDR_PMU_CPU0_PMSWINC_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMSWINC_EL0 Register (Offset = CA0h) [reset = 0h]

Performance Monitors Software Increment Register

Return to Summary Table

Table 14-8366. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0CA0h**

Figure 14-2773. A53SS_APBADDR_PMU_CPU0_PMSWINC_EL0 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMSWINC_EL0_31_6		P_X					
R/W		R/W					
0h		0h					

Table 14-8368. A53SS_APBADDR_PMU_CPU0_PMSWINC_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_PMSWINC_EL0_31_6	R/W	0h	Reserved RES0
5:0	P_X	R/W	0h	Event counter software increment bit for PMEVCNTR<x>

14.3.1.1.2.229 A53SS_APBADDR_PMU_CPU0_PMOVSSET_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMOVSSET_EL0 Register (Offset = CC0h) [reset = 0h]

Performance Monitors Overflow Flag Status Set Register

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Table 14-8369. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0CC0h**

Figure 14-2774. A53SS_APBADDR_PMU_CPU0_PMOVSSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-8371. A53SS_APBADDR_PMU_CPU0_PMOVSSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, sets the overflow bit to 1.
30:0	P_X	R/W	0h	Event counter overflow set bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, sets the PMEVCNTR<x> overflow bit to 1.

14.3.1.1.2.230 A53SS_APBADDR_PMU_CPU0_PMCFGR Register

1 A53SS_APBADDR_PMU_CPU0_PMCFGR Register (Offset = E00h) [reset = 1FF06h]

Performance Monitors Configuration Register

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Table 14-8372. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0E00h**

Figure 14-2775. A53SS_APBADDR_PMU_CPU0_PMCFGR Name Register

31	30	29	28	27	26	25	24
RES0_PMCFGR_31_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCFGR_31_20				UEN	WT	NA	EX
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CCD	CC	SIZE					
R/W	R/W	R/W					
1h	1h	3Fh					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
N							
R/W							
6h							

Table 14-8374. A53SS_APBADDR_PMU_CPU0_PMCFGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_PMCFGR_31_20	R/W	0h	Reserved, RES0.
19	UEN	R/W	0h	User-mode Enable Register supported. PMUSERENR_EL0 is not visible in the external debug interface, so this bit is RES0.
18	WT	R/W	0h	This feature is not supported, so this bit is RES0.
17	NA	R/W	0h	This feature is not supported, so this bit is RES0.
16	EX	R/W	1h	Export supported. Value is IMPLEMENTATION DEFINED. 0 PMCR_EL0.X is RES0. 1 PMCR_EL0.X is read/write.
15	CCD	R/W	1h	Cycle counter has prescale. This is RES1 if AArch32 is supported at any EL, and RES0 otherwise. 0 PMCR_EL0.D is RES0. 1 PMCR_EL0.D is read/write.
14	CC	R/W	1h	Dedicated cycle counter [counter 31] supported. This bit is RES1.
13:8	SIZE	R/W	3Fh	Size of counters. This field determines the spacing of counters in the memory-map.In v8-A the counters are at doubleword-aligned addresses, and the largest counter is 64-bits, so this field is 0b111111.

Table 14-8374. A53SS_APBADDR_PMU_CPU0_PMCFGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	N	R/W	6h	Number of counters implemented in addition to the cycle counter, PMCCNTR_EL0. The maximum number of event counters is 31, so bits[7:5] are always RES0. 00000000 Only PMCCNTR_EL0 implemented. 00000001 PMCCNTR_EL0 plus one event counter implemented. and so on up to 0b00011111, which indicates PMCCNTR_EL0 and 31 event counters implemented.

14.3.1.1.2.231 A53SS_APBADDR_PMU_CPU0_PMCR_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMCR_EL0 Register (Offset = E04h) [reset = 0h]

Performance Monitors Control Register

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Table 14-8375. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0E04h**

Figure 14-2776. A53SS_APBADDR_PMU_CPU0_PMCR_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMCR_EL0_31_11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMCR_EL0_31_11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RES0_PMCR_EL0_31_11</td><td colspan="3">RES0_PMCR_EL0_10_7</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RES0_PMCR_EL0_10_7</td><td>LC</td><td>DP</td><td>X</td><td>D</td><td>C</td><td>P</td><td>E</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8377. A53SS_APBADDR_PMU_CPU0_PMCR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RES0_PMCR_EL0_31_11	R/W	0h	Reserved, RAZ/WI.
10:7	RES0_PMCR_EL0_10_7	R/W	0h	Reserved, RES0.
6	LC	R/W	0h	Long cycle counter enable. Determines which PMCCNTR_EL0 bit generates an overflow recorded by PMOVSR[31]. 0 Cycle counter overflow on increment that changes PMCCNTR_EL0[31] from 1 to 0. 1 Cycle counter overflow on increment that changes PMCCNTR_EL0[63] from 1 to 0. ARM deprecates use of PMCR_EL0.LC = 0.
5	DP	R/W	0h	Disable cycle counter when event counting is prohibited. The possible values of this bit are: 0 PMCCNTR_EL0, if enabled, counts when event counting is prohibited. 1 PMCCNTR_EL0 does not count when event counting is prohibited. Event counting is prohibited when ProfilingProhibited[IsSecure[],PSTATE.EL] == TRUE.This bit is RW.

Table 14-8377. A53SS_APBADDR_PMU_CPU0_PMCR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	X	R/W	0h	Enable export of events in an IMPLEMENTATION DEFINED event stream. The possible values of this bit are: 0 Do not export events. 1 Export events where not prohibited. This bit is used to permit events to be exported to another debug device, such as an OPTIONAL trace extension, over an event bus. If the implementation does not include such an event bus, this bit is RAZ/WI.This bit does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface [CTI] that can be implemented as signals exported from the processor.If the implementation does not include an exported event stream, this bit is RAZ/WI. Otherwise this bit is RW.
3	D	R/W	0h	Clock divider. The possible values of this bit are: 0 When enabled, PMCCNTR_EL0 counts every clock cycle. 1 When enabled, PMCCNTR_EL0 counts once every 64 clock cycles. This bit is RW.If PMCR_EL0.LC == 1, this bit is ignored and the cycle counter counts every clock cycle.ARM deprecates use of PMCR.D = 1.
2	C	R/W	0h	Cycle counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset PMCCNTR_EL0 to zero. This bit is always RAZ.Resetting PMCCNTR_EL0 does not clear the PMCCNTR_EL0 overflow bit to 0.
1	P	R/W	0h	Event counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset all event counters, not including PMCCNTR_EL0, to zero. This bit is always RAZ.Resetting the event counters does not clear any overflow bits to 0.
0	E	R/W	0h	Enable. The possible values of this bit are: 0 All counters, including PMCCNTR_EL0, are disabled. 1 All counters are enabled by PMCNTENSET_EL0. This bit is RW.

14.3.1.1.2.232 A53SS_APBADDR_PMU_CPU0_PMCEID0_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMCEID0_EL0 Register (Offset = E20h) [reset = 67FFBFFFh]

Performance Monitors Common Event Identification Register 0

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Table 14-8378. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0E20h**

Figure 14-2777. A53SS_APBADDR_PMU_CPU0_PMCEID0_EL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CE_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">67FFBFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CE_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">67FFBFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CE_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">67FFBFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CE_31_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">67FFBFFFh</td></tr>
</table>

Table 14-8380. A53SS_APBADDR_PMU_CPU0_PMCEID0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CE_31_0	R/W	67FFBFFFh	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For each bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic310x01FL1D_CACHE_ALLOCATE300x01ECHAIN290x01DBUS_CYCLES280x01CTTBR_WRITE_RETIRED270x01BINST_SPEC260x01AMEMORY_ERROR250x019BUS_ACCESS240x018L2D_CACHE_WB230x017L2D_CACHE_REFILL220x016L2D_CACHE210x015L1D_CACHE_WB200x014L1I_CACHE190x013MEM_ACCESS180x012BR_PRED170x011CPU_CYCLES160x010BR_MIS_PRED150x00FUNALIGNED_LDST_RETIRED140x00EBR_RETURN_RETIRED130x00DBR_IMMED_RETIRED120x00CPC_WRITE_RETIRED110x00BCID_WRITE_RETIRED100x00AEXC_RETURN90x009EXC_TAKEN80x008INST_RETIRED70x007ST_RETIRED60x006LD_RETIRED50x005L1D_TLB_REFILL40x004L1D_CACHE30x003L1D_CACHE_REFILL20x002L1I_TLB_REFILL10x001L1I_CACHE_REFILL00x000SW_INCR

14.3.1.1.2.233 A53SS_APBADDR_PMU_CPU0_PMCEID1_EL0 Register

1 A53SS_APBADDR_PMU_CPU0_PMCEID1_EL0 Register (Offset = E24h) [reset = 0h]

Performance Monitors Common Event Identification Register 1

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Table 14-8381. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0E24h**

Figure 14-2778. A53SS_APBADDR_PMU_CPU0_PMCEID1_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_PMCEID1_EL0_31_1							CE_32
R/W							R/W
0h							0h

Table 14-8383. A53SS_APBADDR_PMU_CPU0_PMCEID1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMCEID1_EL0_31_1	R/W	0h	Reserved, RES0.
0	CE_32	R/W	0h	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For the bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic00x020L2D_CACHE_ALLOCATE

14.3.1.1.2.234 A53SS_APBADDR_PMU_CPU0_PMITCTRL Register

1 A53SS_APBADDR_PMU_CPU0_PMITCTRL Register (Offset = F00h) [reset = 0h]

Performance Monitors Integration mode Control Register

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Table 14-8384. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0F00h**

Figure 14-2779. A53SS_APBADDR_PMU_CPU0_PMITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_PMITCTRL_31_1</td><td>IME</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-8386. A53SS_APBADDR_PMU_CPU0_PMITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.235 A53SS_APBADDR_PMU_CPU0_PMDEVAFF0 Register

1 A53SS_APBADDR_PMU_CPU0_PMDEVAFF0 Register (Offset = FA8h) [reset = 80000000h]

Performance Monitors Device Affinity Register 0

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Table 14-8387. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FA8h**

Figure 14-2780. A53SS_APBADDR_PMU_CPU0_PMDEVAFF0 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF0							
R/W							
80000000h							
23	22	21	20	19	18	17	16
PMDEVAFF0							
R/W							
80000000h							
15	14	13	12	11	10	9	8
PMDEVAFF0							
R/W							
80000000h							
7	6	5	4	3	2	1	0
PMDEVAFF0							
R/W							
80000000h							

Table 14-8389. A53SS_APBADDR_PMU_CPU0_PMDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF0	R/W	80000000h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.236 A53SS_APBADDR_PMU_CPU0_PMDEVAFF1 Register

1 A53SS_APBADDR_PMU_CPU0_PMDEVAFF1 Register (Offset = FACh) [reset = 0h]

Performance Monitors Device Affinity Register 1

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Table 14-8390. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FACh**

Figure 14-2781. A53SS_APBADDR_PMU_CPU0_PMDEVAFF1 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
PMDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
PMDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
PMDEVAFF1							
R/W							
0h							

Table 14-8392. A53SS_APBADDR_PMU_CPU0_PMDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.237 A53SS_APBADDR_PMU_CPU0_PMLAR Register

1 A53SS_APBADDR_PMU_CPU0_PMLAR Register (Offset = FB0h) [reset = 0h]

Performance Monitors Lock Access Register

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Table 14-8393. Instance Table

Instance Name	Physical Address
A53SS0	0007 3003 0FB0h

Figure 14-2782. A53SS_APBADDR_PMU_CPU0_PMLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-8395. A53SS_APBADDR_PMU_CPU0_PMLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.238 A53SS_APBADDR_PMU_CPU0_PMLSR Register

1 A53SS_APBADDR_PMU_CPU0_PMLSR Register (Offset = FB4h) [reset = 3h]

Performance Monitors Lock Status Register

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Table 14-8396. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FB4h**

Figure 14-2783. A53SS_APBADDR_PMU_CPU0_PMLSR Name Register

31	30	29	28	27	26	25	24
RES0_PMLSR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMLSR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMLSR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_PMLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	1h	1h

Table 14-8398. A53SS_APBADDR_PMU_CPU0_PMLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_PMLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	1h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	1h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.239 A53SS_APBADDR_PMU_CPU0_PMAUTHSTATUS Register

1 A53SS_APBADDR_PMU_CPU0_PMAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Performance Monitors Authentication Status Register

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Table 14-8399. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FB8h**

Figure 14-2784. A53SS_APBADDR_PMU_CPU0_PMAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		RES0_PMAUTHSTATUS_5_4		NSNID		RES0_PMAUTHSTATUS_1_0	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-8401. A53SS_APBADDR_PMU_CPU0_PMAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.SNID.
5:4	RES0_PMAUTHSTATUS_5_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	RES0_PMAUTHSTATUS_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.240 A53SS_APBADDR_PMU_CPU0_PMDEVARCH Register

1 A53SS_APBADDR_PMU_CPU0_PMDEVARCH Register (Offset = FBCh) [reset = 47702A16h]

Performance Monitors Device Architecture Register

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Table 14-8402. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FBCh**

Figure 14-2785. A53SS_APBADDR_PMU_CPU0_PMDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	22	21	20	19	18	17	16
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	14	13	12	11	10	9	8
ARCHID							
R/W							
2A16h							
7	6	5	4	3	2	1	0
ARCHID							
R/W							
2A16h							

Table 14-8404. A53SS_APBADDR_PMU_CPU0_PMDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For Performance Monitors, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For Performance Monitors, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	2A16h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For Performance Monitors:Bits [15:12] are the architecture version, 0x2.Bits [11:0] are the architecture part number, 0xA16.This corresponds to Performance Monitors architecture version PMUv3.

14.3.1.1.2.241 A53SS_APBADDR_PMU_CPU0_PMDEVTYPE Register

1 A53SS_APBADDR_PMU_CPU0_PMDEVTYPE Register (Offset = FCCh) [reset = 16h]

Performance Monitors Device Type Register

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Table 14-8405. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FCCh**

Figure 14-2786. A53SS_APBADDR_PMU_CPU0_PMDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_PMDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R/W				R/W			
1h				6h			

Table 14-8407. A53SS_APBADDR_PMU_CPU0_PMDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	6h	Major type. Must read as 0x6 to indicate this is a performance monitor component.

14.3.1.1.2.242 A53SS_APBADDR_PMU_CPU0_PMPIDR4 Register

1 A53SS_APBADDR_PMU_CPU0_PMPIDR4 Register (Offset = FD0h) [reset = 4h]

Performance Monitors Peripheral Identification Register 4

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Table 14-8408. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FD0h**

Figure 14-2787. A53SS_APBADDR_PMU_CPU0_PMPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-8410. A53SS_APBADDR_PMU_CPU0_PMPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.243 A53SS_APBADDR_PMU_CPU0_PMPIDR5 Register

1 A53SS_APBADDR_PMU_CPU0_PMPIDR5 Register (Offset = FD4h) [reset = 0h]

Performance Monitors Peripheral Identification Register 5

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Table 14-8411. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FD4h**

Figure 14-2788. A53SS_APBADDR_PMU_CPU0_PMPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR5_31_0							
R/W							
0h							

Table 14-8413. A53SS_APBADDR_PMU_CPU0_PMPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.244 A53SS_APBADDR_PMU_CPU0_PMPIDR6 Register

1 A53SS_APBADDR_PMU_CPU0_PMPIDR6 Register (Offset = FD8h) [reset = 0h]

Performance Monitors Peripheral Identification Register 6

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Table 14-8414. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FD8h**

Figure 14-2789. A53SS_APBADDR_PMU_CPU0_PMPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR6_31_0							
R/W							
0h							

Table 14-8416. A53SS_APBADDR_PMU_CPU0_PMPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.245 A53SS_APBADDR_PMU_CPU0_PMPIDR7 Register

1 A53SS_APBADDR_PMU_CPU0_PMPIDR7 Register (Offset = FDCh) [reset = 0h]

Performance Monitors Peripheral Identification Register 7

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Table 14-8417. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FDCh**

Figure 14-2790. A53SS_APBADDR_PMU_CPU0_PMPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR7_31_0							
R/W							
0h							

Table 14-8419. A53SS_APBADDR_PMU_CPU0_PMPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.246 A53SS_APBADDR_PMU_CPU0_PMPIDR0 Register

1 A53SS_APBADDR_PMU_CPU0_PMPIDR0 Register (Offset = FE0h) [reset = D3h]

Performance Monitors Peripheral Identification Register 0

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Table 14-8420. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FE0h**

Figure 14-2791. A53SS_APBADDR_PMU_CPU0_PMPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
D3h							

Table 14-8422. A53SS_APBADDR_PMU_CPU0_PMPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	D3h	Part number, least significant byte.

14.3.1.1.2.247 A53SS_APBADDR_PMU_CPU0_PMPIDR1 Register

1 A53SS_APBADDR_PMU_CPU0_PMPIDR1 Register (Offset = FE4h) [reset = B9h]

Performance Monitors Peripheral Identification Register 1

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Table 14-8423. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FE4h**

Figure 14-2792. A53SS_APBADDR_PMU_CPU0_PMPIDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_PMPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_PMPIDR1_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">DES_0</td><td colspan="4">PART_1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Bh</td><td colspan="4">9h</td></tr>
</table>

Table 14-8425. A53SS_APBADDR_PMU_CPU0_PMPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.248 A53SS_APBADDR_PMU_CPU0_PMPIDR2 Register

1 A53SS_APBADDR_PMU_CPU0_PMPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Performance Monitors Peripheral Identification Register 2

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Table 14-8426. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FE8h**

Figure 14-2793. A53SS_APBADDR_PMU_CPU0_PMPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-8428. A53SS_APBADDR_PMU_CPU0_PMPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.249 A53SS_APBADDR_PMU_CPU0_PMPIDR3 Register

1 A53SS_APBADDR_PMU_CPU0_PMPIDR3 Register (Offset = FECh) [reset = 0h]

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Table 14-8429. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FECh**

Figure 14-2794. A53SS_APBADDR_PMU_CPU0_PMPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-8431. A53SS_APBADDR_PMU_CPU0_PMPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using PMPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.250 A53SS_APBADDR_PMU_CPU0_PMCIDR0 Register

1 A53SS_APBADDR_PMU_CPU0_PMCIDR0 Register (Offset = FF0h) [reset = Dh]

Performance Monitors Component Identification Register 0

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Table 14-8432. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FF0h**

Figure 14-2795. A53SS_APBADDR_PMU_CPU0_PMCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRMBL_0							
R/W							
Dh							

Table 14-8434. A53SS_APBADDR_PMU_CPU0_PMCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.251 A53SS_APBADDR_PMU_CPU0_PMCIDR1 Register

1 A53SS_APBADDR_PMU_CPU0_PMCIDR1 Register (Offset = FF4h) [reset = 90h]

Performance Monitors Component Identification Register 1

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Table 14-8435. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FF4h**

Figure 14-2796. A53SS_APBADDR_PMU_CPU0_PMCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-8437. A53SS_APBADDR_PMU_CPU0_PMCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.252 A53SS_APBADDR_PMU_CPU0_PMCIDR2 Register

1 A53SS_APBADDR_PMU_CPU0_PMCIDR2 Register (Offset = FF8h) [reset = 5h]

Performance Monitors Component Identification Register 2

Return to Summary Table

Table 14-8438. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FF8h**

Figure 14-2797. A53SS_APBADDR_PMU_CPU0_PMCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-8440. A53SS_APBADDR_PMU_CPU0_PMCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.253 A53SS_APBADDR_PMU_CPU0_PMCIDR3 Register

1 A53SS_APBADDR_PMU_CPU0_PMCIDR3 Register (Offset = FFCh) [reset = B1h]

Performance Monitors Component Identification Register 3

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Table 14-8441. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3003 0FFCh**

Figure 14-2798. A53SS_APBADDR_PMU_CPU0_PMCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-8443. A53SS_APBADDR_PMU_CPU0_PMCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.254 A53SS_APBADDR_ETM_CPU0_TRCPRGCTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCPRGCTLR Register (Offset = 4h) [reset = 0h]

Programming Control Register

Return to Summary Table

Table 14-8444. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0004h**

Figure 14-2799. A53SS_APBADDR_ETM_CPU0_TRCPRGCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPRGCTLR_31_1							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_TRCPRGCTLR_31_1							
R/W							
0h							

15	14	13	12	11	10	9	8
RES0_TRCPRGCTLR_31_1							
R/W							
0h							

7	6	5	4	3	2	1	0
RES0_TRCPRGCTLR_31_1							EN
R/W							R/W
0h							0h

Table 14-8446. A53SS_APBADDR_ETM_CPU0_TRCPRGCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCPRGCTLR_31_1	R/W	0h	Reserved, RES0.
0	EN	R/W	0h	Trace unit enable bit. Possible values are: 0 The trace unit is disabled. All trace resources are inactive and no trace is generated. 1 The trace unit is enabled.

14.3.1.1.2.255 A53SS_APBADDR_ETM_CPU0_TRCSTATR Register

1 A53SS_APBADDR_ETM_CPU0_TRCSTATR Register (Offset = Ch) [reset = 0h]

Status Register

Return to Summary Table

Table 14-8447. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 000Ch**

Figure 14-2800. A53SS_APBADDR_ETM_CPU0_TRCSTATR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSTATR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSTATR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSTATR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSTATR_31_2						PMSTABLE	IDLE
R/W						R/W	R/W
0h						0h	0h

Table 14-8449. A53SS_APBADDR_ETM_CPU0_TRCSTATR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSTATR_31_2	R/W	0h	Reserved, RES0.
1	PMSTABLE	R/W	0h	Programmer's model stable bit: 0 The programmer's model is not stable. 1 The programmer's model is stable. When polled, the trace unit trace registers return stable data. The programmer's model is stable when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.Reads from trace unit registers return stable data.
0	IDLE	R/W	0h	Idle status bit: 0 The trace unit is not idle. 1 The trace unit is idle. The trace unit is idle when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.The trace unit is drained of any trace.With the exception of the programming interfaces, all external interfaces on the trace unit are quiescent.

14.3.1.1.2.256 A53SS_APBADDR_ETM_CPU0_TRCCONFIGR Register

1 A53SS_APBADDR_ETM_CPU0_TRCCONFIGR Register (Offset = 10h) [reset = 1h]

Trace Configuration Register

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Table 14-8450. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0010h**

Figure 14-2801. A53SS_APBADDR_ETM_CPU0_TRCCONFIGR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCONFIGR_31_18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCONFIGR_31_18						DV	DA
R/W						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCONFIGR_15_15	QE		RS	TS	COND		
R/W	R/W		R/W	R/W	R/W		
0h	0h		0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VMID	CID	RES0_TRCCONFIGR_5_5	CCI	BB	INSTP0		RES1_TRCCONFIGR_0_0
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		1h

Table 14-8452. A53SS_APBADDR_ETM_CPU0_TRCCONFIGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCONFIGR_31_18	R/W	0h	Reserved, RES0.
17	DV	R/W	0h	Data value tracing bit: 0 Data value tracing is disabled. 1 Data value tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
16	DA	R/W	0h	Data address tracing bit: 0 Data address tracing is disabled. 1 Data address tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
15	RES0_TRCCONFIGR_15_15	R/W	0h	Reserved, RES0.

Table 14-8452. A53SS_APBADDR_ETM_CPU0_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	QE	R/W	0h	Q element enable field: 00 Q elements are disabled. 01 Q elements with instruction counts are enabled. Q elements without instruction counts are disabled. 11 Q elements with and without instruction counts are enabled. The value 0b10 is reserved.TRCIDR0.QSUPP indicates which values of this field are implemented.TRCCONFIGR.QE must be set to 0b00 if any of the following are true:TRCCONFIGR.INSTP0 is not 0b00.TRCCONFIGR.COND is not 0b000.TRCCONFIGR.BB is not 0.
12	RS	R/W	0h	Return stack enable bit. 0 Return stack is disabled. 1 Return stack is enabled. TRCIDR0.RETSTACK indicates whether this bit is supported. If it is not supported then this bit is RES0.
11	TS	R/W	0h	Global timestamp tracing bit: 0 Global timestamp tracing is disabled. 1 Global timestamp tracing is enabled. TRCTSCTLR controls the insertion of timestamps in the trace. TRCIDR0.TSSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
10:8	COND	R/W	0h	Conditional instruction tracing bit. The permitted values are: 000 Conditional instruction tracing is disabled. 001 Conditional load instructions are traced. 010 Conditional store instructions are traced. 011 Conditional load and store instructions are traced. 111 All conditional instructions are traced. All other values are reserved.TRCIDR0.TRCCOND indicates whether this field is supported. If it is not supported then this field is RES0.
7	VMID	R/W	0h	VMID tracing bit: 0 VMID tracing is disabled. 1 VMID tracing is enabled. TRCIDR2.VMIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
6	CID	R/W	0h	Context ID tracing bit: 0 Context ID tracing is disabled. 1 Context ID tracing is enabled. TRCIDR2.CIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
5	RES0_TRCCONFIGR_5_5	R/W	0h	Reserved, RES0.

Table 14-8452. A53SS_APBADDR_ETM_CPU0_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CCI	R/W	0h	Cycle counting instruction trace bit: 0 Cycle counting in the instruction trace is disabled. 1 Cycle counting in the instruction trace is enabled. TRCCCCTLR controls the threshold value for cycle counting. TRCIDR0.TRCCCI indicates whether this bit is supported. If it is not supported then this bit is RES0.
3	BB	R/W	0h	Branch broadcast mode bit: 0 Branch broadcast mode is disabled. 1 Branch broadcast mode is enabled. TRCBBCTLR controls which regions of memory are enabled to use branch broadcasting. TRCIDR0.TRCBB indicates whether this bit is supported. If it is not supported then this bit is RES0.
2:1	INSTP0	R/W	0h	Instruction P0 bit. This field controls whether load and store instructions are traced as P0 instructions: 00 Do not trace load and store instructions as P0 instructions. 01 Trace load instructions as P0 instructions. 10 Trace store instructions as P0 instructions. 11 Trace load and store instructions as P0 instructions. TRCIDR0.INSTP0 indicates whether this field is supported. If it is not supported then this field is RES0.
0	RES1_TRCCONFIGR_0_0	R/W	1h	Reserved, RES1.

14.3.1.1.2.257 A53SS_APBADDR_ETM_CPU0_TRCAUXCTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCAUXCTLR Register (Offset = 18h) [reset = 0h]

Auxiliary Control Register

Return to Summary Table

Table 14-8453. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0018h**

Figure 14-2802. A53SS_APBADDR_ETM_CPU0_TRCAUXCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
COREIFEN	RES0_TRCAUXCTLR_6_6	AUTHNOFLUSH	TSNODELAY	SYNCDELAY	OVFLW	IDLEACK	AFREADY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8455. A53SS_APBADDR_ETM_CPU0_TRCAUXCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUXCTLR_31_8	R/W	0h	Reserved RES0
7	COREIFEN	R/W	0h	Keep core interface enabled regardless of trace enable register state
6	RES0_TRCAUXCTLR_6_6	R/W	0h	Reserved RES0
5	AUTHNOFLUSH	R/W	0h	Do not flush trace on de-assertion of authentication inputs. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
4	TSNODELAY	R/W	0h	Do not delay timestamp insertion based on FIFO depth.
3	SYNCDELAY	R/W	0h	Delay periodic synchronization if FIFO is more than half-full.
2	OVFLW	R/W	0h	Force an overflow if synchronization is not completed when second synchronization becomes due. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
1	IDLEACK	R/W	0h	Force idle-drain acknowledge high CPU does not wait for trace to drain before entering WFX state. When this bit is set to 1 trace unit behavior deviates from architecturally-specified behavior.
0	AFREADY	R/W	0h	Always respond to AFREADY immediately. Does not have any interaction with FIFO draining even in WFI state.

14.3.1.1.2.258 A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL0R Register

1 A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL0R Register (Offset = 20h) [reset = 0h]

Event Control 0 Register

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Table 14-8456. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0020h**

Figure 14-2803. A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL0R Name Register

31	30	29	28	27	26	25	24
TYPE3	RESERVED_TRCEVENTCTL0R_30_28			SEL3			
R/W	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
TYPE2	RESERVED_TRCEVENTCTL0R_22_20			SEL2			
R/W	R/W			R/W			
0h	0h			0h			
15	14	13	12	11	10	9	8
TYPE1	RESERVED_TRCEVENTCTL0R_14_12			SEL1			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
TYPE0	RESERVED_TRCEVENTCTL0R_6_4			SEL0			
R/W	R/W			R/W			
0h	0h			0h			

Table 14-8458. A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL0R Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE3	R/W	0h	Selects the resource type for trace event 3
30:28	RESERVED_TRCEVENTCTL0R_30_28	R/W	0h	Reserved RES0
27:24	SEL3	R/W	0h	Selects the resource number based on the value of TYPE3
23	TYPE2	R/W	0h	Selects the resource type for trace event 2
22:20	RESERVED_TRCEVENTCTL0R_22_20	R/W	0h	Reserved RES0
19:16	SEL2	R/W	0h	Selects the resource number based on the value of TYPE2
15	TYPE1	R/W	0h	Selects the resource type for trace event 1
14:12	RESERVED_TRCEVENTCTL0R_14_12	R/W	0h	Reserved RES0
11:8	SEL1	R/W	0h	Selects the resource number based on the value of TYPE1
7	TYPE0	R/W	0h	Selects the resource type for trace event 0
6:4	RESERVED_TRCEVENTCTL0R_6_4	R/W	0h	Reserved RES0
3:0	SEL0	R/W	0h	Selects the resource number based on the value of TYPE0

14.3.1.1.2.259 A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL1R Register

1 A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL1R Register (Offset = 24h) [reset = 0h]

Event Control 1 Register

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Table 14-8459. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0024h**

Figure 14-2804. A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL1R Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCEVENTCTL1R_31_13			LPOVERRIDE	ATB	RESERVED_TRCEVENTCTL1R_10_4		
R/W			R/W	R/W	R/W		
0h			0h	0h	0h		
7	6	5	4	3	2	1	0
RESERVED_TRCEVENTCTL1R_10_4				EN			
R/W				R/W			
0h				0h			

Table 14-8461. A53SS_APBADDR_ETM_CPU0_TRCEVENTCTL1R Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_TRCEVENTCTL1R_31_13	R/W	0h	Reserved RES0
12	LPOVERRIDE	R/W	0h	Low power state behavior override
11	ATB	R/W	0h	ATB trigger enable
10:4	RESERVED_TRCEVENTCTL1R_10_4	R/W	0h	Reserved RES0
3:0	EN	R/W	0h	One bit per event to enable generation of an event element in the instruction trace stream when the selected event occurs

14.3.1.1.2.260 A53SS_APBADDR_ETM_CPU0_TRCSTALLCTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCSTALLCTLR Register (Offset = 2Ch) [reset = 0h]

Stall Control Register

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Table 14-8462. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 002Ch**

Figure 14-2805. A53SS_APBADDR_ETM_CPU0_TRCSTALLCTLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_TRCSTALLCTLR_31_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_TRCSTALLCTLR_31_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED_TRCSTALLCTLR_31_9</td><td>ISTALL</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_TRCSTALLCTLR_7_4</td><td colspan="2">LEVEL</td><td colspan="2">RESERVED_TRCSTALLCTLR_1_0</td></tr>
<tr><td colspan="4">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-8464. A53SS_APBADDR_ETM_CPU0_TRCSTALLCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_TRCSTALLCTLR_31_9	R/W	0h	Reserved RES0
8	ISTALL	R/W	0h	Controls if the trace unit can stall the processor when the instruction trace buffer space is less than LEVEL
7:4	RESERVED_TRCSTALLCTLR_7_4	R/W	0h	Reserved RES0
3:2	LEVEL	R/W	0h	The field can support 4 monotonic levels from 0b00 to 0b11
1:0	RESERVED_TRCSTALLCTLR_1_0	R/W	0h	Reserved RES0

14.3.1.1.2.261 A53SS_APBADDR_ETM_CPU0_TRCTSCTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCTSCTLR Register (Offset = 30h) [reset = 0h]

Global Timestamp Control Register

Return to Summary Table

Table 14-8465. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0030h**

Figure 14-2806. A53SS_APBADDR_ETM_CPU0_TRCTSCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCTSCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCTSCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCTSCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-8467. A53SS_APBADDR_ETM_CPU0_TRCTSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCTSCTLR_31_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams.

14.3.1.1.2.262 A53SS_APBADDR_ETM_CPU0_TRCSYNCPR Register

1 A53SS_APBADDR_ETM_CPU0_TRCSYNCPR Register (Offset = 34h) [reset = 0h]

Synchronization Period Register

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Table 14-8468. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0034h**

Figure 14-2807. A53SS_APBADDR_ETM_CPU0_TRCSYNCPR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RES0_TRCSYNCPR_31_5</td><td colspan="5">PERIOD</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-8470. A53SS_APBADDR_ETM_CPU0_TRCSYNCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCSYNCPR_31_5	R/W	0h	Reserved, RES0.
4:0	PERIOD	R/W	0h	Controls how many bytes of trace, the sum of instruction and data, that a trace unit can generate before a periodic trace synchronization request occurs. The number of bytes is always a power of two and the permitted values are: 00000 Periodic trace synchronization requests are disabled. This setting does not disable other types of trace synchronization request. 01000 Periodic trace synchronization request occurs after 2^8, or 256, bytes of trace. 01001 Periodic trace synchronization request occurs after 2^9, or 512, bytes of trace. 01010 Periodic trace synchronization request occurs after 2^10, or 1024, bytes of trace. and so on up to 0b10100, for which the request occurs after 2^20, or 1048576, bytes of trace.Values between 0b00001 and 0b001111 are reserved, as are values from 0b10101 onwards.

14.3.1.1.2.263 A53SS_APBADDR_ETM_CPU0_TRCCCCTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCCCCTLR Register (Offset = 38h) [reset = 0h]

Cycle Count Control Register

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Table 14-8471. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0038h**

Figure 14-2808. A53SS_APBADDR_ETM_CPU0_TRCCCCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCCCCTLR_31_12							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCCCTLR_31_12							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCCCTLR_31_12				THRESHOLD			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-8473. A53SS_APBADDR_ETM_CPU0_TRCCCCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_TRCCCCTLR_31_12	R/W	0h	Reserved, RES0.
11:0	THRESHOLD	R/W	0h	Sets the threshold value for instruction trace cycle counting.The minimum threshold value that can be programmed into THRESHOLD is given in TRCIDR3.CCITMIN.Writing a value of zero might cause UNPREDICTABLE behaviour.

14.3.1.1.2.264 A53SS_APBADDR_ETM_CPU0_TRCBBCTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCBBCTLR Register (Offset = 3Ch) [reset = 0h]

Branch Broadcast Control Register

Return to Summary Table

Table 14-8474. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 003Ch**

Figure 14-2809. A53SS_APBADDR_ETM_CPU0_TRCBBCTLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCBBCTLR_31_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCBBCTLR_31_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RES0_TRCBBCTLR_31_9</td><td>MODE</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RANGE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8476. A53SS_APBADDR_ETM_CPU0_TRCBBCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RES0_TRCBBCTLR_31_9	R/W	0h	Reserved, RES0.
8	MODE	R/W	0h	Mode bit: 0 Exclude mode. Branch broadcasting is not enabled in the address range that RANGE defines. If RANGE==0 then branch broadcasting is enabled for the entire memory map. 1 Include mode. Branch broadcasting is enabled in the address range that RANGE defines. If RANGE==0 then the branch broadcasting behavior is UNPREDICTABLE.
7:0	RANGE	R/W	0h	Address range field. Selects which address range comparator pairs are in use with branch broadcasting. Each bit represents an address range comparator pair, so bit[n] controls the selection of address range comparator pair n. If bit[n] is: 0 The address range that address range comparator pair n defines is not selected. 1 The address range that address range comparator pair n defines is selected.

14.3.1.1.2.265 A53SS_APBADDR_ETM_CPU0_TRCTRACEIDR Register

1 A53SS_APBADDR_ETM_CPU0_TRCTRACEIDR Register (Offset = 40h) [reset = 0h]

Trace ID Register

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Table 14-8477. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0040h**

Figure 14-2810. A53SS_APBADDR_ETM_CPU0_TRCTRACEIDR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCTRACEIDR_31_7							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCTRACEIDR_31_7	TRACEID						
R/W	R/W						
0h	0h						

Table 14-8479. A53SS_APBADDR_ETM_CPU0_TRCTRACEIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_TRCTRACEIDR_31_7	R/W	0h	Reserved RES0
6:0	TRACEID	R/W	0h	Trace ID value. When only instruction tracing is enabled this provides the trace ID.

14.3.1.1.2.266 A53SS_APBADDR_ETM_CPU0_TRCVICTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCVICTLR Register (Offset = 80h) [reset = 0h]

ViewInst Main Control Register

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Table 14-8480. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0080h**

Figure 14-2811. A53SS_APBADDR_ETM_CPU0_TRCVICTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVICTLR_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RES0_TRCVICTLR_15_12				TRCERR	TRCRESET	SSSTATUS	RES0_TRCVICTLR_8_8
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-8482. A53SS_APBADDR_ETM_CPU0_TRCVICTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVICTLR_31_24	R/W	0h	Reserved, RES0.
23:20	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Non-secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Non-secure state, for exception level n. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.

Table 14-8482. A53SS_APBADDR_ETM_CPU0_TRCVICTLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Secure state, for exception level n. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.
15:12	RES0_TRCVICTLR_15_12	R/W	0h	Reserved, RES0.
11	TRCERR	R/W	0h	If TRCIDR3.TRCERR==1, this bit controls whether a trace unit must trace a system error exception: 0 The trace unit does not trace a system error exception unless it traces the exception or instruction immediately prior to the system error exception. 1 The trace unit always traces a system error exception. If TRCIDR3.TRCERR==0, this bit is RES0.
10	TRCRESET	R/W	0h	Controls whether a trace unit must trace a Reset exception: 0 The trace unit does not trace a Reset exception unless it traces the exception or instruction immediately prior to the Reset exception. 1 The trace unit always traces a Reset exception.
9	SSSTATUS	R/W	0h	IF TRCIDR4.NUMACPAIRS>0 or TRCIDR.NUMPC>0, this bit returns the status of the start-stop logic: 0 The start-stop logic is in the stopped state. 1 The start-stop logic is in the started state. The bit only returns stable data when TRCSTATR.PMSTABLE==1.Before software enables the trace unit, TRCPRGCTLR.EN==1, it must write to this bit to set the initial state of the start-stop logic. If the start-stop logic is not used then set this bit to 1. ARM recommends that the value of this bit is set before each trace run begins.If TRCIDR4.NUMACPAIRS==0 and TRCIDR4.NUMPC==0, this bit is RES0, indicating that the start-stop logic is not implemented.
8	RES0_TRCVICTLR_8_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. [TODO: Add the bit assignments for EVENT fields into the descriptions directly?]

14.3.1.1.2.267 A53SS_APBADDR_ETM_CPU0_TRCVIIECTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCVIIECTLR Register (Offset = 84h) [reset = 0h]

ViewInst Include-Exclude Control Register

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Table 14-8483. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0084h**

Figure 14-2812. A53SS_APBADDR_ETM_CPU0_TRCVIIECTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVIIECTLR_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
EXCLUDE							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCVIIECTLR_15_8							
R/W							
0h							
7	6	5	4	3	2	1	0
INCLUDE							
R/W							
0h							

Table 14-8485. A53SS_APBADDR_ETM_CPU0_TRCVIIECTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVIIECTLR_31_24	R/W	0h	Reserved, RES0.
23:16	EXCLUDE	R/W	0h	0 1 The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:8	RES0_TRCVIIECTLR_15_8	R/W	0h	Reserved, RES0.
7:0	INCLUDE	R/W	0h	Include range field. Selects which address range comparator pairs are in use with ViewInst include control. Each bit represents an address range comparator pair, so bit[m] controls the selection of address range comparator pair m. If bit[m] is: 0 The address range that address range comparator pair m defines is not selected for ViewInst include control. 1 The address range that address range comparator pair m defines is selected for ViewInst include control. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.Selecting no include comparators indicates that all instructions are included by default. The exclude control then indicates which ranges are excluded.

14.3.1.1.2.268 A53SS_APBADDR_ETM_CPU0_TRCVISSCTLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCVISSCTLR Register (Offset = 88h) [reset = 0h]

ViewInst Start-Stop Control Register

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Table 14-8486. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0088h**

Figure 14-2813. A53SS_APBADDR_ETM_CPU0_TRCVISSCTLR Name Register

31	30	29	28	27	26	25	24
STOP							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STOP							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START							
R/W							
0h							

Table 14-8488. A53SS_APBADDR_ETM_CPU0_TRCVISSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STOP	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of stopping trace. Each bit represents a single address comparator, so bit[m] controls the selection of single address comparator m-16. If bit[m] is: 0 The single address comparator m-16 is not selected as a stop resource. 1 The single address comparator m-16 is selected as a stop resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:0	START	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of starting trace. Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n is not selected as a start resource. 1 The single address comparator n is selected as a start resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.269 A53SS_APBADDR_ETM_CPU0_TRCSEQEVR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCSEQEVR0 Register (Offset = 100h) [reset = 0h]

Sequencer State Transition Control Registers 0

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Table 14-8489. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0100h**

Figure 14-2814. A53SS_APBADDR_ETM_CPU0_TRCSEQEVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
B_N							
R/W							
0h							
7	6	5	4	3	2	1	0
F_N							
R/W							
0h							

Table 14-8491. A53SS_APBADDR_ETM_CPU0_TRCSEQEVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR0_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.270 A53SS_APBADDR_ETM_CPU0_TRCSEQEVR1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCSEQEVR1 Register (Offset = 104h) [reset = 0h]

Sequencer State Transition Control Registers 1

Return to Summary Table

Table 14-8492. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0104h**

Figure 14-2815. A53SS_APBADDR_ETM_CPU0_TRCSEQEVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
B_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F_N							
R/W							
0h							

Table 14-8494. A53SS_APBADDR_ETM_CPU0_TRCSEQEVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR1_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.271 A53SS_APBADDR_ETM_CPU0_TRCSEQEVR2 Register

1 A53SS_APBADDR_ETM_CPU0_TRCSEQEVR2 Register (Offset = 108h) [reset = 0h]

Sequencer State Transition Control Registers 2

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Table 14-8495. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0108h**

Figure 14-2816. A53SS_APBADDR_ETM_CPU0_TRCSEQEVR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
B_N							
R/W							
0h							
7	6	5	4	3	2	1	0
F_N							
R/W							
0h							

Table 14-8497. A53SS_APBADDR_ETM_CPU0_TRCSEQEVR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR2_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.272 A53SS_APBADDR_ETM_CPU0_TRCSEQRSTEVR Register

1 A53SS_APBADDR_ETM_CPU0_TRCSEQRSTEVR Register (Offset = 118h) [reset = 0h]

Sequencer Reset Control Register

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Table 14-8498. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0118h**

Figure 14-2817. A53SS_APBADDR_ETM_CPU0_TRCSEQRSTEVR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RST							
R/W							
0h							

Table 14-8500. A53SS_APBADDR_ETM_CPU0_TRCSEQRSTEVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCSEQRSTEVR_31_8	R/W	0h	Reserved, RES0.
7:0	RST	R/W	0h	Contains an event number. When the event occurs then the sequencer state moves to state 0.

14.3.1.1.2.273 A53SS_APBADDR_ETM_CPU0_TRCSEQSTR Register

1 A53SS_APBADDR_ETM_CPU0_TRCSEQSTR Register (Offset = 11Ch) [reset = 0h]

Sequencer State Register

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Table 14-8501. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 011Ch**

Figure 14-2818. A53SS_APBADDR_ETM_CPU0_TRCSEQSTR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQSTR_31_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQSTR_31_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCSEQSTR_31_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCSEQSTR_31_2						STATE	
R/W						R/W	
0h						0h	

Table 14-8503. A53SS_APBADDR_ETM_CPU0_TRCSEQSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSEQSTR_31_2	R/W	0h	Reserved, RES0.
1:0	STATE	R/W	0h	Sets or returns the state of the sequencer: 00 State 0. 01 State 1. 10 State 2. 11 State 3.

14.3.1.1.2.274 A53SS_APBADDR_ETM_CPU0_TRCEXTINSELR Register

1 A53SS_APBADDR_ETM_CPU0_TRCEXTINSELR Register (Offset = 120h) [reset = 0h]

External Input Select Register

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Table 14-8504. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0120h**

Figure 14-2819. A53SS_APBADDR_ETM_CPU0_TRCEXTINSELR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEXTINSELR_31_29			SEL3				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED_TRCEXTINSELR_23_21			SEL2				
R/W			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED_TRCEXTINSELR_15_13			SEL1				
R/W			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED_TRCEXTINSELR_7_5			SEL0				
R/W			R/W				
0h			0h				

Table 14-8506. A53SS_APBADDR_ETM_CPU0_TRCEXTINSELR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED_TRCEXTINSELR_31_29	R/W	0h	Reserved RES0
28:24	SEL3	R/W	0h	Selects an event from the external input bus for External Input Resource 3.
23:21	RESERVED_TRCEXTINSELR_23_21	R/W	0h	Reserved RES0
20:16	SEL2	R/W	0h	Selects an event from the external input bus for External Input Resource 2
15:13	RESERVED_TRCEXTINSELR_15_13	R/W	0h	Reserved RES0
12:8	SEL1	R/W	0h	Selects an event from the external input bus for External Input Resource 1
7:5	RESERVED_TRCEXTINSELR_7_5	R/W	0h	Reserved RES0
4:0	SEL0	R/W	0h	Selects an event from the external input bus for External Input Resource 0

14.3.1.1.2.275 A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR0 Register (Offset = 140h) [reset = 0h]

Counter Reload Value Registers 0

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Table 14-8507. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0140h**

Figure 14-2820. A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCNTRLDVR0_31_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCCNTRLDVR0_31_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VALUE_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VALUE_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8509. A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.276 A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR1 Register (Offset = 144h) [reset = 0h]

Counter Reload Value Registers 1

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Table 14-8510. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0144h**

Figure 14-2821. A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VALUE_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VALUE_N							
R/W							
0h							

Table 14-8512. A53SS_APBADDR_ETM_CPU0_TRCCNTRLDVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.277 A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR0 Register (Offset = 150h) [reset = 0h]

Counter Control Register 0

Return to Summary Table

Table 14-8513. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0150h**

Figure 14-2822. A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCNTCTLR0_31_18</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RES0_TRCCNTCTLR0_31_18</td><td>CNTCHAIN_N</td><td>RLDSELF_N</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RLDEVENT_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CNTEVENT_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8515. A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR0_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.278 A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR1 Register (Offset = 154h) [reset = 0h]

Counter Control Register 1

Return to Summary Table

Table 14-8516. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0154h**

Figure 14-2823. A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR1_31_18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTCTLR1_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RLDEVENT_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CNTEVENT_N							
R/W							
0h							

Table 14-8518. A53SS_APBADDR_ETM_CPU0_TRCCNTCTLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR1_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.279 A53SS_APBADDR_ETM_CPU0_TRCCNTVR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCNTVR0 Register (Offset = 160h) [reset = 0h]

Counter Value Registers 0

Return to Summary Table

Table 14-8519. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0160h**

Figure 14-2824. A53SS_APBADDR_ETM_CPU0_TRCCNTVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-8521. A53SS_APBADDR_ETM_CPU0_TRCCNTVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.280 A53SS_APBADDR_ETM_CPU0_TRCCNTVR1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCNTVR1 Register (Offset = 164h) [reset = 0h]

Counter Value Registers 1

Return to Summary Table

Table 14-8522. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0164h**

Figure 14-2825. A53SS_APBADDR_ETM_CPU0_TRCCNTVR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCNTVR1_31_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCCNTVR1_31_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VALUE_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VALUE_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8524. A53SS_APBADDR_ETM_CPU0_TRCCNTVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.281 A53SS_APBADDR_ETM_CPU0_TRCIDR8 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR8 Register (Offset = 180h) [reset = 0h]

ID Register 8

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Table 14-8525. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0180h**

Figure 14-2826. A53SS_APBADDR_ETM_CPU0_TRCIDR8 Name Register

31	30	29	28	27	26	25	24
MAXSPEC							
R/W							
0h							
23	22	21	20	19	18	17	16
MAXSPEC							
R/W							
0h							
15	14	13	12	11	10	9	8
MAXSPEC							
R/W							
0h							
7	6	5	4	3	2	1	0
MAXSPEC							
R/W							
0h							

Table 14-8527. A53SS_APBADDR_ETM_CPU0_TRCIDR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAXSPEC	R/W	0h	Indicates the maximum speculation depth of the instruction trace stream. This is the maximum number of P0 elements in the trace stream that can be speculative at any time.

14.3.1.1.2.282 A53SS_APBADDR_ETM_CPU0_TRCIDR9 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR9 Register (Offset = 184h) [reset = 0h]

ID Register 9

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Table 14-8528. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0184h**

Figure 14-2827. A53SS_APBADDR_ETM_CPU0_TRCIDR9 Name Register

31	30	29	28	27	26	25	24
NUMP0KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP0KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP0KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP0KEY							
R/W							
0h							

Table 14-8530. A53SS_APBADDR_ETM_CPU0_TRCIDR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP0KEY	R/W	0h	Indicates the number of P0 right-hand keys that the trace unit can use. A value of 0 or 1 indicates one P0 key.

14.3.1.1.2.283 A53SS_APBADDR_ETM_CPU0_TRCIDR10 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR10 Register (Offset = 188h) [reset = 0h]

ID Register 10

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Table 14-8531. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0188h**

Figure 14-2828. A53SS_APBADDR_ETM_CPU0_TRCIDR10 Name Register

31	30	29	28	27	26	25	24
NUMP1KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1KEY							
R/W							
0h							

Table 14-8533. A53SS_APBADDR_ETM_CPU0_TRCIDR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1KEY	R/W	0h	Indicates the number of P1 right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.284 A53SS_APBADDR_ETM_CPU0_TRCIDR11 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR11 Register (Offset = 18Ch) [reset = 0h]

ID Register 11

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Table 14-8534. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 018Ch**

Figure 14-2829. A53SS_APBADDR_ETM_CPU0_TRCIDR11 Name Register

31	30	29	28	27	26	25	24
NUMP1SPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1SPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1SPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1SPC							
R/W							
0h							

Table 14-8536. A53SS_APBADDR_ETM_CPU0_TRCIDR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1SPC	R/W	0h	Indicates the number of special P1 right-hand keys that the trace unit can use.

14.3.1.1.2.285 A53SS_APBADDR_ETM_CPU0_TRCIDR12 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR12 Register (Offset = 190h) [reset = 0h]

ID Register 12

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Table 14-8537. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0190h**

Figure 14-2830. A53SS_APBADDR_ETM_CPU0_TRCIDR12 Name Register

31	30	29	28	27	26	25	24
NUMCONDKEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDKEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDKEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDKEY							
R/W							
0h							

Table 14-8539. A53SS_APBADDR_ETM_CPU0_TRCIDR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDKEY	R/W	0h	Indicates the number of conditional instruction right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.286 A53SS_APBADDR_ETM_CPU0_TRCIDR13 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR13 Register (Offset = 194h) [reset = 0h]

ID Register 13

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Table 14-8540. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0194h**

Figure 14-2831. A53SS_APBADDR_ETM_CPU0_TRCIDR13 Name Register

31	30	29	28	27	26	25	24
NUMCONDSPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDSPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDSPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDSPC							
R/W							
0h							

Table 14-8542. A53SS_APBADDR_ETM_CPU0_TRCIDR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDSPC	R/W	0h	Indicates the number of special conditional instruction right-hand keys that the trace unit can use.

14.3.1.1.2.287 A53SS_APBADDR_ETM_CPU0_TRCIMSPEC0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIMSPEC0 Register (Offset = 1C0h) [reset = 0h]

Implementation Specific Register 0

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Table 14-8543. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01C0h**

Figure 14-2832. A53SS_APBADDR_ETM_CPU0_TRCIMSPEC0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EN				SUPPORT			
R/W				R/W			
0h				0h			

Table 14-8545. A53SS_APBADDR_ETM_CPU0_TRCIMSPEC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCIMSPEC0_31_8	R/W	0h	Reserved, RES0.
7:4	EN	R/W	0h	If SUPPORT is not 0b0000, controls whether the IMPLEMENTATION DEFINED features are enabled. The permitted values are: 0000 The IMPLEMENTATION DEFINED features are not enabled. The trace unit must behave as if the IMPLEMENTATION DEFINED features are not supported. and any other value, which indicates that the trace unit behavior is IMPLEMENTATION DEFINED.If SUPPORT is 0b0000, this field is RES0.
3:0	SUPPORT	R/W	0h	Indicates whether the implementation supports IMPLEMENTATION DEFINED features. The permitted values are: 0000 No IMPLEMENTATION DEFINED features are supported. The EN field is RES0. and any other value, which indicates that IMPLEMENTATION DEFINED features are supported. Use of these values requires written permission from ARM.

14.3.1.1.2.288 A53SS_APBADDR_ETM_CPU0_TRCIDR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR0 Register (Offset = 1E0h) [reset = 28000EA1h]

ID Register 0

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Table 14-8546. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01E0h**

Figure 14-2833. A53SS_APBADDR_ETM_CPU0_TRCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR0_31_30		COMMOPT	TSSIZE				
R/W		R/W	R/W				
0h		1h	8h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCIDR0_23_17							QSUPP
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
QSUPP	QFILT	CONDTYPE		NUMEVENT		RETSTACK	RES0_TRCIDR0_8_8
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		3h		1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRCCCI	TRCCOND	TRCBB	TRCDATA		INSTP0		RES0_TRCIDR0_0_0
R/W	R/W	R/W	R/W		R/W		R/W
1h	0h	1h	0h		0h		1h

Table 14-8548. A53SS_APBADDR_ETM_CPU0_TRCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RES0_TRCIDR0_31_30	R/W	0h	Reserved, RES0.
29	COMMOPT	R/W	1h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
28:24	TSSIZE	R/W	8h	Global timestamp size field. The permitted values are: 00000 Global timestamping is not implemented. 00110 Implementation supports a maximum global timestamp of 48bits. 01000 Implementation supports a maximum global timestamp of 64bits. All other values are reserved.When global timestamping is implemented then TRCCONFIGR.TS and TRCTSCTLR are supported.
23:17	RES0_TRCIDR0_23_17	R/W	0h	Reserved, RES0.

Table 14-8548. A53SS_APBADDR_ETM_CPU0_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:15	QSUPP	R/W	0h	Q element support field. The permitted values are: 00 Q element support is not implemented. TRCCONFIGR.QE is RES0. 01 Q element support is implemented, and only supports Q elements with instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b01. 10 Q element support is implemented, and only supports Q elements without instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b11. 11 Q element support is implemented, and supports both Q elements with instruction counts and Q elements without instruction counts. TRCCONFIGR.QE is fully implemented.
14	QFILT	R/W	0h	Q element filtering support field. The permitted values are: 0 Q element filtering is not implemented. 1 Q element filtering is implemented. TRCQCTLR is implemented. When QSUPP==0b00, this field is RES0.
13:12	CONDTYPE	R/W	0h	Conditional tracing field. The permitted values are: 00 The trace unit indicates only if a conditional instruction is a pass or fail. 01 The trace unit provides the Current Program Status Register [CPSR] status, for a conditional instruction. All other values are reserved.
11:10	NUMEVENT	R/W	3h	Number of events field. Indicates how many events the trace unit supports: 00 The trace unit supports 1 event. 01 The trace unit supports 2 events. 10 The trace unit supports 3 events. 11 The trace unit supports 4 events. This field controls how many fields are supported in TRCEVENTCTL0R, and indicates the size of TRCEVENTCTL1R.INSTEN.
9	RETSTACK	R/W	1h	Return stack bit. Indicates if the implementation supports a return stack: 0 Return stack is not implemented. 1 Return stack is implemented, so TRCCONFIGR.RS is supported.
8	RES0_TRCIDR0_8_8	R/W	0h	Reserved, RES0.
7	TRCCCI	R/W	1h	Cycle counting instruction bit. Indicates if the trace unit supports cycle counting for instructions: 0 Cycle counting in the instruction trace is not implemented. 1 Cycle counting in the instruction trace is implemented, so TRCCONFIGR.CCI and TRCCCCTLR are supported.

Table 14-8548. A53SS_APBADDR_ETM_CPU0_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRCCOND	R/W	0h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
5	TRCBB	R/W	1h	Branch broadcast tracing support bit. Indicates if the trace unit supports branch broadcast tracing: 0 Branch broadcast tracing is not supported. 1 Branch broadcast tracing is supported, so TRCCONFIGR.BB and TRCBBCTLR are supported.
4:3	TRCDATA	R/W	0h	Conditional tracing field. The permitted values are: 00 Data tracing is not supported. 11 Tracing of data addresses and data values is supported, so TRCCONFIGR.DA, TRCCONFIGR.DV, TRCSTALLCTLR.DATADISCARD, TRCSTALLCTLR.INSTPRIORITY, TRCSTALLCTLR.DSTALL, and TRCEVENTCTL1R.DATAEN are supported. All other values are reserved.
2:1	INSTP0	R/W	0h	P0 tracing support field. The permitted values are: 00 Tracing of load and store instructions as P0 elements is not supported. 11 Tracing of load and store instructions as P0 elements is supported, so TRCCONFIGR.INSTP0 is supported. All other values are reserved.
0	RES0_TRCIDR0_0_0	R/W	1h	Reserved, RES0.

14.3.1.1.2.289 A53SS_APBADDR_ETM_CPU0_TRCIDR1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR1 Register (Offset = 1E4h) [reset = 4100F404h]

ID Register 1

Return to Summary Table

Table 14-8549. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01E4h**

Figure 14-2834. A53SS_APBADDR_ETM_CPU0_TRCIDR1 Name Register

31	30	29	28	27	26	25	24
DESIGNER							
R/W							
41h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCIDR1_23_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES1_TRCIDR1_15_12				TRCARCHMAJ			
R/W				R/W			
Fh				4h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRCARCHMIN				REVISION			
R/W				R/W			
0h				4h			

Table 14-8551. A53SS_APBADDR_ETM_CPU0_TRCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DESIGNER	R/W	41h	Indicates which company designed the trace unit. The permitted values are: 01000001 ARM Limited. 01000100 Digital Equipment Corporation. 01001101 Motorola, Freescale Semiconductor Inc. 01010001 QUALCOMM Inc. 01010110 Marvell Semiconductor Inc. 01101001 Intel Corporation. All other values are reserved.
23:16	RES0_TRCIDR1_23_16	R/W	0h	Reserved, RES0.
15:12	RES1_TRCIDR1_15_12	R/W	Fh	Reserved, RES1.
11:8	TRCARCHMAJ	R/W	4h	Indicates the major version of the ETM architecture. The permitted value is: 100 ETMv4. All other values are reserved.

Table 14-8551. A53SS_APBADDR_ETM_CPU0_TRCIDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRCARCHMIN	R/W	0h	Indicates the minor version of the ETM architecture. The permitted value is: 0 ETMv4 minor version 0. All other values are reserved.
3:0	REVISION	R/W	4h	Returns an IMPLEMENTATION DEFINED value that identifies the revision of the trace registers and the OS Save and Restore registers.ARM recommends:That the initial implementation sets REVISION==0x0 and the field then increments for any subsequent implementations. However, it is acceptable to omit some values or use another scheme to identify the revision number.That TRCPIDR2.REVISION==TRCIDR1.REVISION. However, in situations where it is difficult to align these fields, such as with a metal layer fix, then it is acceptable to change the REVISION fields independently.

14.3.1.1.2.290 A53SS_APBADDR_ETM_CPU0_TRCIDR2 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR2 Register (Offset = 1E8h) [reset = 488h]

ID Register 2

Return to Summary Table

Table 14-8552. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01E8h**

Figure 14-2835. A53SS_APBADDR_ETM_CPU0_TRCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR2_31_29			CCSIZE				DVSIZE
R/W			R/W				R/W
0h			0h				0h

23	22	21	20	19	18	17	16
DVSIZE				DASIZE			
R/W				R/W			
0h				0h			

15	14	13	12	11	10	9	8
DASIZE	VMIDSIZE					CIDSIZE	
R/W	R/W					R/W	
0h	1h					4h	

7	6	5	4	3	2	1	0
CIDSIZE			IASIZE				
R/W			R/W				
4h			8h				

Table 14-8554. A53SS_APBADDR_ETM_CPU0_TRCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_TRCIDR2_31_29	R/W	0h	Reserved, RES0.
28:25	CCSIZE	R/W	0h	Indicates the size of the cycle counter in bits minus 12. 0000 The cycle counter is 12 bits in length. 0001 The cycle counter is 13 bits in length. and so on up to 0b1000, indicating the cycle counter is 20 bits in length.All other values are reserved.If cycle counting is not implemented, as indicated by TRCIDR0.TRCCCI, this field is 0b0000.
24:20	DVSIZE	R/W	0h	Indicates the data value size in bytes. The permitted values are: 00000 Data value tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data value size. 01000 Maximum of 64-bit data value size. All other values are reserved.

Table 14-8554. A53SS_APBADDR_ETM_CPU0_TRCIDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	DASIZE	R/W	0h	Indicates the data address size in bytes. The permitted values are: 00000 Data address tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data address size. 01000 Maximum of 64-bit data address size. All other values are reserved.
14:10	VMIDSIZE	R/W	1h	Indicates the VMID size. The permitted values are: 00000 VMID tracing is not supported. 00001 Maximum of 8-bit VMID size, so TRCCONFIGR.VMID is supported. All other values are reserved.
9:5	CIDSIZE	R/W	4h	Indicates the Context ID size. The permitted values are: 00000 Context ID tracing is not supported. 00100 Maximum of 32-bit Context ID size, so TRCCONFIGR.CID is supported. All other values are reserved.
4:0	IASIZE	R/W	8h	Indicates the instruction address size. The permitted values are: 00100 Maximum of 32-bit address size. 01000 Maximum of 64-bit address size. All other values are reserved.

14.3.1.1.2.291 A53SS_APBADDR_ETM_CPU0_TRCIDR3 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR3 Register (Offset = 1ECh) [reset = D7B0004h]

ID Register 3

Return to Summary Table

Table 14-8555. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01ECh**

Figure 14-2836. A53SS_APBADDR_ETM_CPU0_TRCIDR3 Name Register

31	30	29	28	27	26	25	24
NOOVERFLOW	NUMPROC			SYSSTALL	STALLCTL	SYNCPR	TRCERR
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			1h	1h	0h	1h
23	22	21	20	19	18	17	16
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
7h				Bh			
15	14	13	12	11	10	9	8
RES0_TRCIDR3_15_12				CCITMIN			
R/W				R/W			
0h				4h			
7	6	5	4	3	2	1	0
CCITMIN							
R/W							
4h							

Table 14-8557. A53SS_APBADDR_ETM_CPU0_TRCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOOVERFLOW	R/W	0h	Indicates if TRCSTALLCTLR.NOOVERFLOW is supported: 0 TRCSTALLCTLR.NOOVERFLOW is not supported, or STALLCTL==0. 1 TRCSTALLCTLR.NOOVERFLOW is supported.
30:28	NUMPROC	R/W	0h	Indicates the number of processors available for tracing. The possible values are: 000 The trace unit can trace one processor. 001 The trace unit can trace two processors. 010 The trace unit can trace three processors. and so on up to 0b111, which indicates the trace unit can trace eight processors.This field sets the maximum value of TRCPROCSELR.PROCSEL.
27	SYSSTALL	R/W	1h	Indicates if the implementation can support stall control: 0 The system does not support stall control of the processor. 1 The system can support stall control of the processor. The system supports stalling of the processor only when SYSSTALL==1 and STALLCTL==1.

Table 14-8557. A53SS_APBADDR_ETM_CPU0_TRCIDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	STALLCTL	R/W	1h	Indicates if TRCSTALLCTLR is supported: 0 TRCSTALLCTLR is not supported. 1 TRCSTALLCTLR is supported.
25	SYNCPR	R/W	0h	Indicates if an implementation has a fixed synchronization period: 0 TRCSYNCPR is read-write so software can change the synchronization period. 1 TRCSYNCPR is read-only so the synchronization period is fixed.
24	TRCERR	R/W	1h	Indicates if TRCVICTLR.TRCERR is supported: 0 TRCVICTLR.TRCERR is not supported 1 TRCVICTLR.TRCERR is supported.
23:20	EXLEVEL_NS	R/W	7h	In Non-secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Non-secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are not supported. 1 In Non-secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are supported. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]SBZ. EXLEVEL_NS[3] is never implemented.
19:16	EXLEVEL_S	R/W	Bh	In Secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are not supported. 1 In Secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are supported. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]SBZ. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.
15:12	RES0_TRCIDR3_15_12	R/W	0h	Reserved, RES0.
11:0	CCITMIN	R/W	4h	Indicates the minimum value that can be programmed in TRCCCCTLR.THRESHOLD.When cycle counting in the instruction trace is supported, that is TRCIDR0.TRCCCI==1, then the minimum value of this field is 0x001, otherwise it is 0x000.

14.3.1.1.2.292 A53SS_APBADDR_ETM_CPU0_TRCIDR4 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR4 Register (Offset = 1F0h) [reset = 11170004h]

ID Register 4

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Table 14-8558. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01F0h**

Figure 14-2837. A53SS_APBADDR_ETM_CPU0_TRCIDR4 Name Register

31	30	29	28	27	26	25	24
NUMVMIDC				NUMCIDC			
R/W				R/W			
1h				1h			
23	22	21	20	19	18	17	16
NUMSSCC				NUMRSPAIR			
R/W				R/W			
1h				7h			
15	14	13	12	11	10	9	8
NUMPC				RES0_TRCIDR4_11_9			SUPPDAC
R/W				R/W			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
NUMDVC				NUMACPAIRS			
R/W				R/W			
0h				4h			

Table 14-8560. A53SS_APBADDR_ETM_CPU0_TRCIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	NUMVMIDC	R/W	1h	Indicates the number of VMID comparators that are available for tracing. The permitted values are: 0000 No VMID comparators are available. 0001 The implementation has one VMID comparator. 0010 The implementation has two VMID comparators. and so on up to 0b1000, which indicates that the implementation has eight VMID comparators.All other values are reserved.
27:24	NUMCIDC	R/W	1h	Indicates the number of Context ID comparators that are available for tracing. The permitted values are: 0000 No Context ID comparators are available. 0001 The implementation has one Context ID comparator. 0010 The implementation has two Context ID comparators. and so on up to 0b1000, which indicates that the implementation has eight Context ID comparators.All other values are reserved.

Table 14-8560. A53SS_APBADDR_ETM_CPU0_TRCIDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	NUMSSCC	R/W	1h	Indicates the number of single-shot comparator controls that are available for tracing. The permitted values are: 0000 No single-shot comparator controls are available. 0001 The implementation has one single-shot comparator control. 0010 The implementation has two single-shot comparator controls. and so on up to 0b1000, which indicates that the implementation has eight single-shot comparator controls.All other values are reserved.
19:16	NUMRSPAIR	R/W	7h	Indicates the number of resource selection pairs that are available for tracing. The permitted values are: 0000 The implementation has one resource selection pair. 0001 The implementation has two resource selection pairs. 0010 The implementation has three resource selection pairs. and so on up to 0b1111, which indicates that the implementation has 16 resource selection pairs.Implementations always have at least one resource selection pair so that they can support the FALSE and TRUE resource selectors, 0 and 1.
15:12	NUMPC	R/W	0h	Indicates the number of processor comparator inputs that are available for tracing. The permitted values are: 0000 No processor comparator inputs are available. 0001 The implementation has one processor comparator input. 0010 The implementation has two processor comparator inputs. and so on up to 0b1000, which indicates that the implementation has eight processor comparator inputs.All other values are reserved.
11:9	RES0_TRCIDR4_11_9	R/W	0h	Reserved, RES0.
8	SUPPDAC	R/W	0h	Indicates if the implementation can support data address comparisons: 0 The implementation does not support data address comparisons. 1 The implementation can support data address comparisons
7:4	NUMDVC	R/W	0h	Indicates the number of data value comparators that are available for tracing. The permitted values are: 0000 No data value comparators are available. 0001 The implementation has one data value comparator. 0010 The implementation has two data value comparators. and so on up to 0b1000, which indicates that the implementation has eight data value comparators.All other values are reserved.
3:0	NUMACPAIRS	R/W	4h	Indicates the number of address comparator pairs that are available for tracing. The permitted values are: 0000 No address comparator pairs are available. 0001 The implementation has one address comparator pair. 0010 The implementation has two address comparator pairs. and so on up to 0b1000, which indicates that the implementation has eight address comparator pairs.All other values are reserved.

14.3.1.1.2.293 A53SS_APBADDR_ETM_CPU0_TRCIDR5 Register

1 A53SS_APBADDR_ETM_CPU0_TRCIDR5 Register (Offset = 1F4h) [reset = 28C7081Eh]

ID Register 5

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Table 14-8561. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 01F4h**

Figure 14-2838. A53SS_APBADDR_ETM_CPU0_TRCIDR5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>REDFUNCNTR</td><td colspan="3">NUMCNTR</td><td colspan="3">NUMSEQSTATE</td><td>RES0_TRCIDR5_24_24</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">2h</td><td colspan="3">4h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>LPOVERRIDE</td><td>ATBTRIG</td><td colspan="6">TRACEIDSIZE</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="6">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td colspan="6">7h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RES0_TRCIDR5_15_12</td><td colspan="3">NUMEXTINSEL</td><td>NUMEXTIN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="3">R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">4h</td><td>1Eh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUMEXTIN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1Eh</td></tr>
</table>

Table 14-8563. A53SS_APBADDR_ETM_CPU0_TRCIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDFUNCNTR	R/W	0h	Indicates if the reduced function counter is implemented: 0 The reduced function counter is not supported. 1 Counter 0 is implemented as a reduced function counter.
30:28	NUMCNTR	R/W	2h	Indicates the number of counters that are available for tracing. The permitted values are: 000 No counters are available. 001 The implementation has one counter. 010 The implementation has two counters. 011 The implementation has three counters. 100 The implementation has four counters. All other values are reserved.

Table 14-8563. A53SS_APBADDR_ETM_CPU0_TRCIDR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:25	NUMSEQSTATE	R/W	4h	Indicates the number of sequencer states that are implemented. The permitted values are: 000 No sequencer states are implemented. 100 The implementation has four sequencer states. All other values are reserved.
24	RES0_TRCIDR5_24_24	R/W	0h	Reserved, RES0.
23	LPOVERRIDE	R/W	1h	Indicates if the implementation can support low-power state override: 0 The implementation does not support low-power state override. 1 The implementation supports low-power state override, and the TRCEVENTCTL1R.LPOVERRIDE field is implemented. The trace unit must support low-power state override if it can enter a low-power mode where the resources and event trace generation are disabled.
22	ATBTRIG	R/W	1h	Indicates if the implementation can support ATB triggers: 0 The implementation does not support ATB triggers. 1 The implementation supports ATB triggers, and the TRCEVENTCTL1R.ATBTRIG field is implemented.
21:16	TRACEIDSIZE	R/W	7h	Indicates the trace ID width. The permitted value is: 111 The implementation supports a 7-bit trace ID. This sets the width of the TRCTRACEIDR.TRACEID field. All other values are reserved.The CoreSight ATB requires a 7-bit trace ID width.
15:12	RES0_TRCIDR5_15_12	R/W	0h	Reserved, RES0.
11:9	NUMEXTINSEL	R/W	4h	Indicates how many external input select resources are implemented. The permitted values are: 000 No external input select resources are available. If NUMEXTINSEL is zero, NUMEXTIN must also be zero. 001 The implementation has one external input select resource. 010 The implementation has two external input select resources. 011 The implementation has three external input select resources. 100 The implementation has four external input select resources. All other values are reserved.See TRCEXTINSELR for how to select an input select resource.
8:0	NUMEXTIN	R/W	1Eh	Indicates how many external inputs are implemented. The permitted values are: 000000000 No external inputs are available. If NUMEXTIN is zero, NUMEXTINSEL must also be zero. 000000001 The implementation has one external input. 000000010 The implementation has two external inputs. and so on up to 0b100000000, which indicates that the implementation has 256 external inputs.All other values >0b100000000 are reserved.See TRCEXTINSELR for how to select an external input.

14.3.1.1.2.294 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR2 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR2 Register (Offset = 208h) [reset = 0h]

Resource Selection Control Registers 2

Return to Summary Table

Table 14-8564. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0208h**

Figure 14-2839. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR2_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR2_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-8566. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR2_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8566. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.295 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR3 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR3 Register (Offset = 20Ch) [reset = 0h]

Resource Selection Control Registers 3

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Table 14-8567. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 020Ch**

Figure 14-2840. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR3_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR3_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-8569. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR3_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8569. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.296 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR4 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR4 Register (Offset = 210h) [reset = 0h]

Resource Selection Control Registers 4

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Table 14-8570. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0210h**

Figure 14-2841. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR4_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR4_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8572. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR4_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8572. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.297 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR5 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR5 Register (Offset = 214h) [reset = 0h]

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Table 14-8573. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0214h**

Figure 14-2842. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR5_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR5_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-8575. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR5_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8575. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.298 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR6 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR6 Register (Offset = 218h) [reset = 0h]

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Table 14-8576. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0218h**

Figure 14-2843. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR6_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR6_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-8578. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR6_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8578. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.299 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR7 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR7 Register (Offset = 21Ch) [reset = 0h]

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Table 14-8579. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 021Ch**

Figure 14-2844. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR7_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR7_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-8581. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR7_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8581. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.300 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR8 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR8 Register (Offset = 220h) [reset = 0h]

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Table 14-8582. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0220h**

Figure 14-2845. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR8 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR8_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR8_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-8584. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR8_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8584. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.301 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR9 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR9 Register (Offset = 224h) [reset = 0h]

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Table 14-8585. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0224h**

Figure 14-2846. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR9 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR9_31_22							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_TRCRSCTLR9_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							

7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-8587. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR9_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8587. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.302 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR10 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR10 Register (Offset = 228h) [reset = 0h]

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Table 14-8588. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0228h**

Figure 14-2847. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR10 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR10_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR10_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-8590. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR10_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8590. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.303 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR11 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR11 Register (Offset = 22Ch) [reset = 0h]

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Table 14-8591. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 022Ch**

Figure 14-2848. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR11_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR11_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8593. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR11_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8593. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.304 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR12 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR12 Register (Offset = 230h) [reset = 0h]

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Table 14-8594. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0230h**

Figure 14-2849. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR12_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR12_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8596. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR12_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8596. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.305 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR13 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR13 Register (Offset = 234h) [reset = 0h]

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Table 14-8597. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0234h**

Figure 14-2850. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR13 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR13_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR13_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-8599. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR13_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8599. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.306 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR14 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR14 Register (Offset = 238h) [reset = 0h]

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Table 14-8600. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0238h**

Figure 14-2851. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR14 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR14_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR14_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-8602. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR14_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8602. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.307 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR15 Register

1 A53SS_APBADDR_ETM_CPU0_TRCRSCTLR15 Register (Offset = 23Ch) [reset = 0h]

Resource Selection Control Registers 15

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Table 14-8603. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 023Ch**

Figure 14-2852. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR15 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR15_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR15_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-8605. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR15_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-8605. A53SS_APBADDR_ETM_CPU0_TRCRSCTLR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.308 A53SS_APBADDR_ETM_CPU0_TRCSSCCR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCSSCCR0 Register (Offset = 280h) [reset = 0h]

Single-Shot Comparator Control Register 0

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Table 14-8606. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0280h**

Figure 14-2853. A53SS_APBADDR_ETM_CPU0_TRCSSCCR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSSCCR0_31_25							RST
R/W							R/W
0h							0h
23	22	21	20	19	18	17	16
ARC							
R/W							
0h							
15	14	13	12	11	10	9	8
SAC							
R/W							
0h							
7	6	5	4	3	2	1	0
SAC							
R/W							
0h							

Table 14-8608. A53SS_APBADDR_ETM_CPU0_TRCSSCCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RES0_TRCSSCCR0_31_25	R/W	0h	Reserved, RES0.
24	RST	R/W	0h	Controls whether the single-shot comparator resource is reset when it fires. 0 When the single-shot comparator resource fires, it is not reset. 1 When the single-shot comparator resource fires, it is reset. This enables the single-shot comparator resource to fire multiple times.
23:16	ARC	R/W	0h	Selects one or more address range comparators for single-shot control.Each bit represents an address range comparator pair, so bit[n-16] controls the selection of address range comparator pair n-16. If bit[n-16] is: 0 The address range comparator pair n-16 is not selected for single-shot control. 1 The address range comparator pair n-16 is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

Table 14-8608. A53SS_APBADDR_ETM_CPU0_TRCSSCCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SAC	R/W	0h	Selects one or more single address comparators for single-shot control.Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n, is not selected for single-shot control. 1 The single address comparator n, is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.309 A53SS_APBADDR_ETM_CPU0_TRCSSCSR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCSSCSR0 Register (Offset = 2A0h) [reset = 1h]

Single-Shot Comparator Status Register 0

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Table 14-8609. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 02A0h**

Figure 14-2854. A53SS_APBADDR_ETM_CPU0_TRCSSCSR0 Name Register

31	30	29	28	27	26	25	24
STATUS	RES0_TRCSSCSR0_30_3						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RES0_TRCSSCSR0_30_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSSCSR0_30_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSSCSR0_30_3					DV	DA	INST
R/W					R/W	R/W	R/W
0h					0h	0h	1h

Table 14-8611. A53SS_APBADDR_ETM_CPU0_TRCSSCSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	STATUS	R/W	0h	Single-shot status bit. Indicates if any of the comparators that TRCSSCCRn.SAC or TRCSSCCRn.ARC selects have matched: 0 No match has occurred. 1 One or more matches has occurred. If TRCSSCCRn.RST==0 then there is only one match and no more matches are possible, and software must reset this bit to 0 to re-enable the single-shot control. STATUS must be written to set an initial state when configuring the trace unit, if the single-shot comparator is to be used.
30:3	RES0_TRCSSCSR0_30_3	R/W	0h	Reserved, RES0.
2	DV	R/W	0h	Data value comparator support bit. Indicates if the trace unit supports data address with data value comparisons: 0 Single-shot data address with data value comparisons are not supported. 1 Single-shot data address with data value comparisons are supported.

Table 14-8611. A53SS_APBADDR_ETM_CPU0_TRCSSCSR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DA	R/W	0h	Data address comparator support bit. Indicates if the trace unit supports data address comparisons: 0 Single-shot data address comparisons are not supported. 1 Single-shot data address comparisons are supported.
0	INST	R/W	1h	Instruction address comparator support bit. Indicates if the trace unit supports instruction address comparisons: 0 Single-shot instruction address comparisons are not supported. 1 Single-shot instruction address comparisons are supported.

14.3.1.1.2.310 A53SS_APBADDR_ETM_CPU0_TRCOSLAR Register

1 A53SS_APBADDR_ETM_CPU0_TRCOSLAR Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-8612. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0300h**

Figure 14-2855. A53SS_APBADDR_ETM_CPU0_TRCOSLAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLAR_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCOSLAR_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCOSLAR_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCOSLAR_31_1							LOCK
R/W							R/W
0h							0h

Table 14-8614. A53SS_APBADDR_ETM_CPU0_TRCOSLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCOSLAR_31_1	R/W	0h	Reserved, RES0.
0	LOCK	R/W	0h	OS Lock control bit: 0 Unlocks the OS Lock. 1 Locks the OS Lock. This setting disables the trace unit.

14.3.1.1.2.311 A53SS_APBADDR_ETM_CPU0_TRCOSLSR Register

1 A53SS_APBADDR_ETM_CPU0_TRCOSLSR Register (Offset = 304h) [reset = Ah]

OS Lock Status Register

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Table 14-8615. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3004 0304h**

Figure 14-2856. A53SS_APBADDR_ETM_CPU0_TRCOSLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLSR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCOSLSR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCOSLSR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCOSLSR_31_4				PRESENT	BIT32	LOCKED	RES0_TRCOSLSR_0_0
R/W				R/W	R/W	R/W	R/W
0h				1h	0h	1h	0h

Table 14-8617. A53SS_APBADDR_ETM_CPU0_TRCOSLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCOSLSR_31_4	R/W	0h	Reserved, RES0.
3	PRESENT	R/W	1h	Indicates whether the OS Lock is implemented.This bit is RES1, which indicates that the OS Lock is always implemented.
2	BIT32	R/W	0h	This bit is RES0, which indicates that software must perform a 32-bit write to update the TRCOSLAR.
1	LOCKED	R/W	1h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. When the trace unit core power domain is powered down the value is UNKNOWN. The TRCPDSR indicates if the trace unit core power domain is powered down.
0	RES0_TRCOSLSR_0_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.312 A53SS_APBADDR_ETM_CPU0_TRCPDCR Register

1 A53SS_APBADDR_ETM_CPU0_TRCPDCR Register (Offset = 310h) [reset = 0h]

Power Down Control Register

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Table 14-8618. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0310h**

Figure 14-2857. A53SS_APBADDR_ETM_CPU0_TRCPDCR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDCR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPDCR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPDCR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCPDCR_31_4				PU	RES0_TRCPDCR_2_0		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-8620. A53SS_APBADDR_ETM_CPU0_TRCPDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCPDCR_31_4	R/W	0h	Reserved, RES0.
3	PU	R/W	0h	Powerup request bit: 0 The system can remove power from the trace unit. The TRCPDSR indicates if the trace unit is powered down. 1 The system must provide power to the trace unit. Typically, a trace unit drives a signal representing the value of this bit to a power controller to request that the trace unit core power domain is powered up. However, if the trace unit and the processor are in the same power domain then the implementation might combine the PU status with a signal from the processor.
2:0	RES0_TRCPDCR_2_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.313 A53SS_APBADDR_ETM_CPU0_TRCPDSR Register

1 A53SS_APBADDR_ETM_CPU0_TRCPDSR Register (Offset = 314h) [reset = 0h]

Power Down Status Register

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Table 14-8621. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0314h**

Figure 14-2858. A53SS_APBADDR_ETM_CPU0_TRCPDSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDSR_31_6							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPDSR_31_6							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPDSR_31_6							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPDSR_31_6		LOCKED	RES0_TRCPDSR_4_2			STICKYPD	POWER
R/W		R/W	R/W			R/W	R/W
0h		0h	0h			0h	0h

Table 14-8623. A53SS_APBADDR_ETM_CPU0_TRCPDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RES0_TRCPDSR_31_6	R/W	0h	Reserved, RES0.
5	LOCKED	R/W	0h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. The value is UNKNOWN when the trace unit core power domain is powered down, that is, when POWER==0.
4:2	RES0_TRCPDSR_4_2	R/W	0h	Reserved, RES0.
1	STICKYPD	R/W	0h	Sticky powerdown status bit. Indicates whether the trace register state is valid: 0 If POWER==1 then the state of TRCOSLSR and the trace registers are valid. If POWER==0 then it is UNKNOWN whether the state of TRCOSLSR and the trace registers are valid. 1 The state of TRCOSLSR and the trace registers might not be valid. The trace unit sets this bit to 1 if either the trace unit is reset, or the power to the trace unit core power domain is removed and the trace register state is not valid. After this register is read, if the Software Lock is unlocked and the trace unit core power domain is powered up, then the trace unit sets this bit to 0. The TRCLAR controls whether the Software Lock is locked.

Table 14-8623. A53SS_APBADDR_ETM_CPU0_TRCPDSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POWER	R/W	0h	Power status bit: 0 The trace unit core power domain is not powered. The trace registers are not accessible and they all return an error response. 1 The trace unit core power domain is powered. The trace registers are accessible.

14.3.1.1.2.314 A53SS_APBADDR_ETM_CPU0_TRCACVR0_31_0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR0_31_0 Register (Offset = 400h) [reset = 0h]

Address Comparator Value Registers 0 (low word)

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Table 14-8624. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0400h**

Figure 14-2859. A53SS_APBADDR_ETM_CPU0_TRCACVR0_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8626. A53SS_APBADDR_ETM_CPU0_TRCACVR0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.315 A53SS_APBADDR_ETM_CPU0_TRCACVR0_63_32 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR0_63_32 Register (Offset = 404h) [reset = 0h]

Address Comparator Value Registers 0 (high word)

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Table 14-8627. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0404h**

Figure 14-2860. A53SS_APBADDR_ETM_CPU0_TRCACVR0_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8629. A53SS_APBADDR_ETM_CPU0_TRCACVR0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.316 A53SS_APBADDR_ETM_CPU0_TRCACVR1_31_0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR1_31_0 Register (Offset = 408h) [reset = 0h]

Address Comparator Value Registers 1 (low word)

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Table 14-8630. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0408h**

Figure 14-2861. A53SS_APBADDR_ETM_CPU0_TRCACVR1_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8632. A53SS_APBADDR_ETM_CPU0_TRCACVR1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.317 A53SS_APBADDR_ETM_CPU0_TRCACVR1_63_32 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR1_63_32 Register (Offset = 40Ch) [reset = 0h]

Address Comparator Value Registers 1 (high word)

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Table 14-8633. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 040Ch**

Figure 14-2862. A53SS_APBADDR_ETM_CPU0_TRCACVR1_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8635. A53SS_APBADDR_ETM_CPU0_TRCACVR1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.318 A53SS_APBADDR_ETM_CPU0_TRCACVR2_31_0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR2_31_0 Register (Offset = 410h) [reset = 0h]

Address Comparator Value Registers 2 (low word)

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Table 14-8636. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0410h**

Figure 14-2863. A53SS_APBADDR_ETM_CPU0_TRCACVR2_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8638. A53SS_APBADDR_ETM_CPU0_TRCACVR2_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.319 A53SS_APBADDR_ETM_CPU0_TRCACVR2_63_32 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR2_63_32 Register (Offset = 414h) [reset = 0h]

Address Comparator Value Registers 2 (high word)

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Table 14-8639. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0414h**

Figure 14-2864. A53SS_APBADDR_ETM_CPU0_TRCACVR2_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8641. A53SS_APBADDR_ETM_CPU0_TRCACVR2_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.320 A53SS_APBADDR_ETM_CPU0_TRCACVR3_31_0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR3_31_0 Register (Offset = 418h) [reset = 0h]

Address Comparator Value Registers 3 (low word)

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Table 14-8642. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0418h**

Figure 14-2865. A53SS_APBADDR_ETM_CPU0_TRCACVR3_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8644. A53SS_APBADDR_ETM_CPU0_TRCACVR3_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.321 A53SS_APBADDR_ETM_CPU0_TRCACVR3_63_32 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR3_63_32 Register (Offset = 41Ch) [reset = 0h]

Address Comparator Value Registers 3 (high word)

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Table 14-8645. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 041Ch**

Figure 14-2866. A53SS_APBADDR_ETM_CPU0_TRCACVR3_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8647. A53SS_APBADDR_ETM_CPU0_TRCACVR3_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.322 A53SS_APBADDR_ETM_CPU0_TRCACVR4_31_0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR4_31_0 Register (Offset = 420h) [reset = 0h]

Address Comparator Value Registers 4 (low word)

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Table 14-8648. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0420h**

Figure 14-2867. A53SS_APBADDR_ETM_CPU0_TRCACVR4_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8650. A53SS_APBADDR_ETM_CPU0_TRCACVR4_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.323 A53SS_APBADDR_ETM_CPU0_TRCACVR4_63_32 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR4_63_32 Register (Offset = 424h) [reset = 0h]

Address Comparator Value Registers 4 (high word)

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Table 14-8651. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0424h**

Figure 14-2868. A53SS_APBADDR_ETM_CPU0_TRCACVR4_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8653. A53SS_APBADDR_ETM_CPU0_TRCACVR4_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.324 A53SS_APBADDR_ETM_CPU0_TRCACVR5_31_0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR5_31_0 Register (Offset = 428h) [reset = 0h]

Address Comparator Value Registers 5 (low word)

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Table 14-8654. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0428h**

Figure 14-2869. A53SS_APBADDR_ETM_CPU0_TRCACVR5_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8656. A53SS_APBADDR_ETM_CPU0_TRCACVR5_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.325 A53SS_APBADDR_ETM_CPU0_TRCACVR5_63_32 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR5_63_32 Register (Offset = 42Ch) [reset = 0h]

Address Comparator Value Registers 5 (high word)

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Table 14-8657. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 042Ch**

Figure 14-2870. A53SS_APBADDR_ETM_CPU0_TRCACVR5_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8659. A53SS_APBADDR_ETM_CPU0_TRCACVR5_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.326 A53SS_APBADDR_ETM_CPU0_TRCACVR6_31_0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR6_31_0 Register (Offset = 430h) [reset = 0h]

Address Comparator Value Registers 6 (low word)

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Table 14-8660. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0430h**

Figure 14-2871. A53SS_APBADDR_ETM_CPU0_TRCACVR6_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8662. A53SS_APBADDR_ETM_CPU0_TRCACVR6_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.327 A53SS_APBADDR_ETM_CPU0_TRCACVR6_63_32 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR6_63_32 Register (Offset = 434h) [reset = 0h]

Address Comparator Value Registers 6 (high word)

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Table 14-8663. Instance Table

Instance Name	Physical Address
A53SS0	0007 3004 0434h

Figure 14-2872. A53SS_APBADDR_ETM_CPU0_TRCACVR6_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8665. A53SS_APBADDR_ETM_CPU0_TRCACVR6_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.328 A53SS_APBADDR_ETM_CPU0_TRCACVR7_31_0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR7_31_0 Register (Offset = 438h) [reset = 0h]

Address Comparator Value Registers 7 (low word)

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Table 14-8666. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0438h**

Figure 14-2873. A53SS_APBADDR_ETM_CPU0_TRCACVR7_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8668. A53SS_APBADDR_ETM_CPU0_TRCACVR7_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.329 A53SS_APBADDR_ETM_CPU0_TRCACVR7_63_32 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACVR7_63_32 Register (Offset = 43Ch) [reset = 0h]

Address Comparator Value Registers 7 (high word)

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Table 14-8669. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 043Ch**

Figure 14-2874. A53SS_APBADDR_ETM_CPU0_TRCACVR7_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-8671. A53SS_APBADDR_ETM_CPU0_TRCACVR7_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.330 A53SS_APBADDR_ETM_CPU0_TRCACATR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACATR0 Register (Offset = 480h) [reset = 0h]

Address Comparator Access Type Registers 0

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Table 14-8672. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0480h**

Figure 14-2875. A53SS_APBADDR_ETM_CPU0_TRCACATR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR0_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR0_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR0_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-8674. A53SS_APBADDR_ETM_CPU0_TRCACATR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR0_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-8674. A53SS_APBADDR_ETM_CPU0_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-8674. A53SS_APBADDR_ETM_CPU0_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR0_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-8674. A53SS_APBADDR_ETM_CPU0_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.331 A53SS_APBADDR_ETM_CPU0_TRCACATR1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACATR1 Register (Offset = 488h) [reset = 0h]

Address Comparator Access Type Registers 1

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Table 14-8675. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0488h**

Figure 14-2876. A53SS_APBADDR_ETM_CPU0_TRCACATR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR1_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR1_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR1_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-8677. A53SS_APBADDR_ETM_CPU0_TRCACATR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR1_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-8677. A53SS_APBADDR_ETM_CPU0_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-8677. A53SS_APBADDR_ETM_CPU0_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR1_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-8677. A53SS_APBADDR_ETM_CPU0_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.332 A53SS_APBADDR_ETM_CPU0_TRCACATR2 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACATR2 Register (Offset = 490h) [reset = 0h]

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Table 14-8678. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0490h**

Figure 14-2877. A53SS_APBADDR_ETM_CPU0_TRCACATR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR2_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR2_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR2_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-8680. A53SS_APBADDR_ETM_CPU0_TRCACATR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR2_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-8680. A53SS_APBADDR_ETM_CPU0_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-8680. A53SS_APBADDR_ETM_CPU0_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR2_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-8680. A53SS_APBADDR_ETM_CPU0_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.333 A53SS_APBADDR_ETM_CPU0_TRCACATR3 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACATR3 Register (Offset = 498h) [reset = 0h]

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Table 14-8681. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0498h**

Figure 14-2878. A53SS_APBADDR_ETM_CPU0_TRCACATR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR3_31_22							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_TRCACATR3_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	

15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			

7	6	5	4	3	2	1	0
RES0_TRCACATR3_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-8683. A53SS_APBADDR_ETM_CPU0_TRCACATR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR3_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-8683. A53SS_APBADDR_ETM_CPU0_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-8683. A53SS_APBADDR_ETM_CPU0_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR3_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-8683. A53SS_APBADDR_ETM_CPU0_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.334 A53SS_APBADDR_ETM_CPU0_TRCACATR4 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACATR4 Register (Offset = 4A0h) [reset = 0h]

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Table 14-8684. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 04A0h**

Figure 14-2879. A53SS_APBADDR_ETM_CPU0_TRCACATR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR4_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR4_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR4_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-8686. A53SS_APBADDR_ETM_CPU0_TRCACATR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR4_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-8686. A53SS_APBADDR_ETM_CPU0_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-8686. A53SS_APBADDR_ETM_CPU0_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR4_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-8686. A53SS_APBADDR_ETM_CPU0_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.335 A53SS_APBADDR_ETM_CPU0_TRCACATR5 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACATR5 Register (Offset = 4A8h) [reset = 0h]

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Table 14-8687. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 04A8h**

Figure 14-2880. A53SS_APBADDR_ETM_CPU0_TRCACATR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR5_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR5_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR5_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-8689. A53SS_APBADDR_ETM_CPU0_TRCACATR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR5_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-8689. A53SS_APBADDR_ETM_CPU0_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-8689. A53SS_APBADDR_ETM_CPU0_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR5_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-8689. A53SS_APBADDR_ETM_CPU0_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.336 A53SS_APBADDR_ETM_CPU0_TRCACATR6 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACATR6 Register (Offset = 4B0h) [reset = 0h]

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Table 14-8690. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 04B0h**

Figure 14-2881. A53SS_APBADDR_ETM_CPU0_TRCACATR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR6_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR6_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR6_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-8692. A53SS_APBADDR_ETM_CPU0_TRCACATR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR6_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-8692. A53SS_APBADDR_ETM_CPU0_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-8692. A53SS_APBADDR_ETM_CPU0_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR6_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-8692. A53SS_APBADDR_ETM_CPU0_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.337 A53SS_APBADDR_ETM_CPU0_TRCACATR7 Register

1 A53SS_APBADDR_ETM_CPU0_TRCACATR7 Register (Offset = 4B8h) [reset = 0h]

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Table 14-8693. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 04B8h**

Figure 14-2882. A53SS_APBADDR_ETM_CPU0_TRCACATR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR7_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR7_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR7_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-8695. A53SS_APBADDR_ETM_CPU0_TRCACATR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR7_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-8695. A53SS_APBADDR_ETM_CPU0_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-8695. A53SS_APBADDR_ETM_CPU0_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR7_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-8695. A53SS_APBADDR_ETM_CPU0_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.338 A53SS_APBADDR_ETM_CPU0_TRCCIDCVR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCIDCVR0 Register (Offset = 600h) [reset = 0h]

Context ID Comparator Value Register 0

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Table 14-8696. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0600h**

Figure 14-2883. A53SS_APBADDR_ETM_CPU0_TRCCIDCVR0 Name Register

31	30	29	28	27	26	25	24
VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-8698. A53SS_APBADDR_ETM_CPU0_TRCCIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE	R/W	0h	Context ID value. The implemented width of this field is IMPLEMENTATION DEFINED and is set by TRCIDR2.CIDSIZE. Unimplemented bits are RAZ/WI.After a processor reset, the ETM architecture assumes that the Context ID is zero until the processor updates the Context ID.

14.3.1.1.2.339 A53SS_APBADDR_ETM_CPU0_TRCVMIDCVR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCVMIDCVR0 Register (Offset = 640h) [reset = 0h]

VMID Comparator Value Register 0

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Table 14-8699. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0640h**

Figure 14-2884. A53SS_APBADDR_ETM_CPU0_TRCVMIDCVR0 Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-8701. A53SS_APBADDR_ETM_CPU0_TRCVMIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_TRCVMIDCVR0_31_8	R/W	0h	Reserved RES0
7:0	VALUE	R/W	0h	Contains a VMID value.

14.3.1.1.2.340 A53SS_APBADDR_ETM_CPU0_TRCCIDCCTLR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCIDCCTLR0 Register (Offset = 680h) [reset = 0h]

Context ID Comparator Control Register 0

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Table 14-8702. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0680h**

Figure 14-2885. A53SS_APBADDR_ETM_CPU0_TRCCIDCCTLR0 Name Register

31	30	29	28	27	26	25	24
COMP_N							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_N							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_N							
R/W							
0h							

Table 14-8704. A53SS_APBADDR_ETM_CPU0_TRCCIDCCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_N	R/W	0h	Controls the mask value that the trace unit applies to TRCCIDCVRn. Each bit in this field corresponds to a byte in TRCCIDCVRn. When a bit is: 0 The trace unit includes the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. 1 The trace unit ignores the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. Supported only if TRCIDR4.NUMCIDC > n, otherwise the field is RES0.

14.3.1.1.2.341 A53SS_APBADDR_ETM_CPU0_TRCITATBIDR Register

1 A53SS_APBADDR_ETM_CPU0_TRCITATBIDR Register (Offset = EE4h) [reset = 0h]

Integration ATB Identification Register

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Table 14-8705. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0EE4h**

Figure 14-2886. A53SS_APBADDR_ETM_CPU0_TRCITATBIDR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITATBIDR_31_7							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCITATBIDR_31_7							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCITATBIDR_31_7							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCITATBIDR_31_7	ID						
R/W	R/W						
0h	0h						

Table 14-8707. A53SS_APBADDR_ETM_CPU0_TRCITATBIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES0_TRCITATBIDR_31_7	R/W	0h	Reserved RES0
6:0	ID	R/W	0h	Drives the ATIDMn[6:0] output pins

14.3.1.1.2.342 A53SS_APBADDR_ETM_CPU0_TRCITIDATAR Register

1 A53SS_APBADDR_ETM_CPU0_TRCITIDATAR Register (Offset = EECh) [reset = 0h]

Integration Instruction ATB Data Register

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Table 14-8708. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0EECh**

Figure 14-2887. A53SS_APBADDR_ETM_CPU0_TRCITIDATAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITIDATAR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITIDATAR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITIDATAR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITIDATAR_31_5			ATDATAM_31	ATDATAM_23	ATDATAM_15	ATDATAM_7	ATDATAM_0
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-8710. A53SS_APBADDR_ETM_CPU0_TRCITIDATAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCITIDATAR_31_5	R/W	0h	Reserved RES0
4	ATDATAM_31	R/W	0h	Drives the ATDATAM[31] output
3	ATDATAM_23	R/W	0h	Drives the ATDATAM[23] output
2	ATDATAM_15	R/W	0h	Drives the ATDATAM[15] output
1	ATDATAM_7	R/W	0h	Drives the ATDATAM[7] output
0	ATDATAM_0	R/W	0h	Drives the ATDATAM[0] output

14.3.1.1.2.343 A53SS_APBADDR_ETM_CPU0_TRCITIATBINR Register

1 A53SS_APBADDR_ETM_CPU0_TRCITIATBINR Register (Offset = EF4h) [reset = 0h]

Integration Instruction ATB In Register

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Table 14-8711. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0EF4h**

Figure 14-2888. A53SS_APBADDR_ETM_CPU0_TRCITIATBINR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCITIATBINR_31_2						AFVALIDM	ATREADYM
R/W						R/W	R/W
0h						0h	0h

Table 14-8713. A53SS_APBADDR_ETM_CPU0_TRCITIATBINR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_TRCITIATBINR_31_2	R/W	0h	Reserved. Read undefined.
1	AFVALIDM	R/W	0h	Returns the value of the AFVALIDMn input pin
0	ATREADYM	R/W	0h	Returns the value of the ATREADYMn input pin

14.3.1.1.2.344 A53SS_APBADDR_ETM_CPU0_TRCITIATBOUTR Register

1 A53SS_APBADDR_ETM_CPU0_TRCITIATBOUTR Register (Offset = EFCh) [reset = 0h]

Integration Instruction ATB Out Register

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Table 14-8714. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0EFCh**

Figure 14-2889. A53SS_APBADDR_ETM_CPU0_TRCITIATBOUTR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBOUTR_31_10							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCITIATBOUTR_31_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCITIATBOUTR_31_10						BYTES	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED_TRCITIATBOUTR_7_2						AFREADY	ATVALID
R/W						R/W	R/W
0h						0h	0h

Table 14-8716. A53SS_APBADDR_ETM_CPU0_TRCITIATBOUTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_TRCITIATBOUTR_31_10	R/W	0h	Reserved. Read undefined.
9:8	BYTES	R/W	0h	Drives the ATBYTESMn[1:0] output pins
7:2	RESERVED_TRCITIATBOUTR_7_2	R/W	0h	Reserved. Read undefined.
1	AFREADY	R/W	0h	Drives the AFREADYMn output pin
0	ATVALID	R/W	0h	Drives the ATVALIDMn output pin

14.3.1.1.2.345 A53SS_APBADDR_ETM_CPU0_TRCITCTRL Register

1 A53SS_APBADDR_ETM_CPU0_TRCITCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Control Register

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Table 14-8717. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0F00h**

Figure 14-2890. A53SS_APBADDR_ETM_CPU0_TRCITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_TRCITCTRL_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCITCTRL_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCITCTRL_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCITCTRL_31_1							ITEN
R/W							R/W
0h							0h

Table 14-8719. A53SS_APBADDR_ETM_CPU0_TRCITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCITCTRL_31_1	R/W	0h	Reserved, RES0.
0	ITEN	R/W	0h	Integration mode enable bit: 0 The trace unit is not in integration mode. 1 The trace unit is in integration mode. This mode enables a debug agent to perform topology detection, and System-on-Chip [SoC] test software to perform integration testing.

14.3.1.1.2.346 A53SS_APBADDR_ETM_CPU0_TRCCLAIMSET Register

1 A53SS_APBADDR_ETM_CPU0_TRCCLAIMSET Register (Offset = FA0h) [reset = Fh]

Claim Tag Set Register

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Table 14-8720. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FA0h**

Figure 14-2891. A53SS_APBADDR_ETM_CPU0_TRCCLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCCLAIMSET_31_4				SET			
R/W				R/W			
0h				Fh			

Table 14-8722. A53SS_APBADDR_ETM_CPU0_TRCCLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	SET	R/W	Fh	Sets bits in the claim tag and determines the number of claim tag bits implemented.

14.3.1.1.2.347 A53SS_APBADDR_ETM_CPU0_TRCCLAIMCLR Register

1 A53SS_APBADDR_ETM_CPU0_TRCCLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-8723. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FA4h**

Figure 14-2892. A53SS_APBADDR_ETM_CPU0_TRCCLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCCLAIMCLR_31_4				CLR			
R/W				R/W			
0h				0h			

Table 14-8725. A53SS_APBADDR_ETM_CPU0_TRCCLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLR	R/W	0h	Clears bits in the claim tag and determines the current value of the claim tag.

14.3.1.1.2.348 A53SS_APBADDR_ETM_CPU0_TRCDEVAFF0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCDEVAFF0 Register (Offset = FA8h) [reset = 80000000h]

Device Affinity Register 0

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Table 14-8726. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FA8h**

Figure 14-2893. A53SS_APBADDR_ETM_CPU0_TRCDEVAFF0 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_31_0							
R/W							
80000000h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MPIDR_EL1_31_0							
R/W							
80000000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPIDR_EL1_31_0							
R/W							
80000000h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPIDR_EL1_31_0							
R/W							
80000000h							

Table 14-8728. A53SS_APBADDR_ETM_CPU0_TRCDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_31_0	R/W	80000000h	Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.349 A53SS_APBADDR_ETM_CPU0_TRCDEVAFF1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCDEVAFF1 Register (Offset = FACh) [reset = 0h]

Device Affinity Register 1

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Table 14-8729. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FACh**

Figure 14-2894. A53SS_APBADDR_ETM_CPU0_TRCDEVAFF1 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
MPIDR_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
MPIDR_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MPIDR_EL1_63_32							
R/W							
0h							

Table 14-8731. A53SS_APBADDR_ETM_CPU0_TRCDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_63_32	R/W	0h	Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.350 A53SS_APBADDR_ETM_CPU0_TRCLAR Register

1 A53SS_APBADDR_ETM_CPU0_TRCLAR Register (Offset = FB0h) [reset = 0h]

Software Lock Access Register

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Table 14-8732. Instance Table

Instance Name	Physical Address
A53SS0	0007 3004 0FB0h

Figure 14-2895. A53SS_APBADDR_ETM_CPU0_TRCLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-8734. A53SS_APBADDR_ETM_CPU0_TRCLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Writing the key value 0xC5ACCE55 to this field clears the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register sets the lock, disabling write accesses to this component's registers through a memory mapped interface.Software can use the Software Lock to prevent accidental modification of the trace unit registers by software being debugged. For example, software that accidentally initializes an incorrect region of memory might disable the trace unit and make it impossible to trace the software.

14.3.1.1.2.351 A53SS_APBADDR_ETM_CPU0_TRCLSR Register

1 A53SS_APBADDR_ETM_CPU0_TRCLSR Register (Offset = FB4h) [reset = 0h]

Software Lock Status Register

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Table 14-8735. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FB4h**

Figure 14-2896. A53SS_APBADDR_ETM_CPU0_TRCLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-8737. A53SS_APBADDR_ETM_CPU0_TRCLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_TRCLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. Possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. RAO.

14.3.1.1.2.352 A53SS_APBADDR_ETM_CPU0_TRCAUTHSTATUS Register

1 A53SS_APBADDR_ETM_CPU0_TRCAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Authentication Status Register

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Table 14-8738. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FB8h**

Figure 14-2897. A53SS_APBADDR_ETM_CPU0_TRCAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCAUTHSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		SID		NSNID		NSID	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-8740. A53SS_APBADDR_ETM_CPU0_TRCAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Indicates whether the system enables the trace unit to support Secure non-invasive debug: 00 The trace unit does not implement support for Secure non-invasive debug. 01 Reserved. 10 Secure non-invasive debug is disabled. 11 Secure non-invasive debug is enabled.
5:4	SID	R/W	0h	Indicates whether the trace unit supports Secure invasive debug: 00 The trace unit does not support Secure invasive debug. All other values are reserved.

Table 14-8740. A53SS_APBADDR_ETM_CPU0_TRCAUTHSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Indicates whether the system enables the trace unit to support Non-secure non-invasive debug: 00 The trace unit does not implement support for Non-secure non-invasive debug. 01 Reserved. 10 Non-secure non-invasive debug is disabled. 11 Non-secure non-invasive debug is enabled.
1:0	NSID	R/W	0h	Indicates whether the trace unit supports Non-secure invasive debug: 00 The trace unit does not support Non-secure invasive debug. All other values are reserved.

14.3.1.1.2.353 A53SS_APBADDR_ETM_CPU0_TRCDEVARCH Register

1 A53SS_APBADDR_ETM_CPU0_TRCDEVARCH Register (Offset = FBCh) [reset = 47704A13h]

Device Architecture Register

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Table 14-8741. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FBCh**

Figure 14-2898. A53SS_APBADDR_ETM_CPU0_TRCDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4A13h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4A13h</td></tr>
</table>

Table 14-8743. A53SS_APBADDR_ETM_CPU0_TRCDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For trace, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is RAO.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For trace, the revision defined by ETMv4 is 0x0.All other values are reserved.
15:0	ARCHID	R/W	4A13h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For trace, bits [15:12] are the architecture version, 0x4; bits [11:0] are the architecture part number, 0xA13.This corresponds to trace architecture version ETMv4.

14.3.1.1.2.354 A53SS_APBADDR_ETM_CPU0_TRCDEVID Register

1 A53SS_APBADDR_ETM_CPU0_TRCDEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-8744. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FC8h**

Figure 14-2899. A53SS_APBADDR_ETM_CPU0_TRCDEVID Name Register

31	30	29	28	27	26	25	24
DEVID							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVID							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVID							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVID							
R/W							
0h							

Table 14-8746. A53SS_APBADDR_ETM_CPU0_TRCDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVID	R/W	0h	Indicates the capabilities of the trace unit. The implemented width of this field and its bit assignments are IMPLEMENTATION DEFINED. Unimplemented bits are RAZ/WI.If a component is configurable then ARM recommends that this field can also indicate which configuration options are implemented that differ from the standard configuration.

14.3.1.1.2.355 A53SS_APBADDR_ETM_CPU0_TRCDEVTYPE Register

1 A53SS_APBADDR_ETM_CPU0_TRCDEVTYPE Register (Offset = FCCh) [reset = 13h]

Device Type Register

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Table 14-8747. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FCCh**

Figure 14-2900. A53SS_APBADDR_ETM_CPU0_TRCDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAIN			
R/W				R/W			
1h				3h			

Table 14-8749. A53SS_APBADDR_ETM_CPU0_TRCDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Returns 0x1, to indicate that the ETM generates processor trace.All other values are reserved.
3:0	MAIN	R/W	3h	Returns 0x3, to indicate that the ETM is a trace source.All other values are reserved.

14.3.1.1.2.356 A53SS_APBADDR_ETM_CPU0_TRCPIDR4 Register

1 A53SS_APBADDR_ETM_CPU0_TRCPIDR4 Register (Offset = FD0h) [reset = 4h]

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Table 14-8750. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FD0h**

Figure 14-2901. A53SS_APBADDR_ETM_CPU0_TRCPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-8752. A53SS_APBADDR_ETM_CPU0_TRCPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RES0. This indicates that the ETM memory map occupies 4KB.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code. For ARM Limited, this field is 0b0100.

14.3.1.1.2.357 A53SS_APBADDR_ETM_CPU0_TRCPIDR5 Register

1 A53SS_APBADDR_ETM_CPU0_TRCPIDR5 Register (Offset = FD4h) [reset = 0h]

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Table 14-8753. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FD4h**

Figure 14-2902. A53SS_APBADDR_ETM_CPU0_TRCPIDR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR5_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR5_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR5_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR5_7_0							
R/W							
0h							

Table 14-8755. A53SS_APBADDR_ETM_CPU0_TRCPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR5_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR5_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.358 A53SS_APBADDR_ETM_CPU0_TRCPIDR6 Register

1 A53SS_APBADDR_ETM_CPU0_TRCPIDR6 Register (Offset = FD8h) [reset = 0h]

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Table 14-8756. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FD8h**

Figure 14-2903. A53SS_APBADDR_ETM_CPU0_TRCPIDR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR6_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR6_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR6_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR6_7_0							
R/W							
0h							

Table 14-8758. A53SS_APBADDR_ETM_CPU0_TRCPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR6_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR6_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.359 A53SS_APBADDR_ETM_CPU0_TRCPIDR7 Register

1 A53SS_APBADDR_ETM_CPU0_TRCPIDR7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register 7

Return to Summary Table

Table 14-8759. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FDCh**

Figure 14-2904. A53SS_APBADDR_ETM_CPU0_TRCPIDR7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCPIDR7_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_TRCPIDR7_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8761. A53SS_APBADDR_ETM_CPU0_TRCPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR7_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR7_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.360 A53SS_APBADDR_ETM_CPU0_TRCPIDR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCPIDR0 Register (Offset = FE0h) [reset = 5Dh]

Peripheral Identification Register 0

Return to Summary Table

Table 14-8762. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FE0h**

Figure 14-2905. A53SS_APBADDR_ETM_CPU0_TRCPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R/W							
5Dh							

Table 14-8764. A53SS_APBADDR_ETM_CPU0_TRCPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	5Dh	Part number, bits[7:0].

14.3.1.1.2.361 A53SS_APBADDR_ETM_CPU0_TRCPIDR1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCPIDR1 Register (Offset = FE4h) [reset = B9h]

Peripheral Identification Register 1

Return to Summary Table

Table 14-8765. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FE4h**

Figure 14-2906. A53SS_APBADDR_ETM_CPU0_TRCPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-8767. A53SS_APBADDR_ETM_CPU0_TRCPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, bits[3:0] of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, bits[11:8].

14.3.1.1.2.362 A53SS_APBADDR_ETM_CPU0_TRCPIDR2 Register

1 A53SS_APBADDR_ETM_CPU0_TRCPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Peripheral Identification Register 2

Return to Summary Table

Table 14-8768. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FE8h**

Figure 14-2907. A53SS_APBADDR_ETM_CPU0_TRCPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-8770. A53SS_APBADDR_ETM_CPU0_TRCPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	The IMPLEMENTATION DEFINED revision number for the ETM implementation. See also TRCIDR1.REVISION.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.363 A53SS_APBADDR_ETM_CPU0_TRCPIDR3 Register

1 A53SS_APBADDR_ETM_CPU0_TRCPIDR3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register 3

Return to Summary Table

Table 14-8771. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FECh**

Figure 14-2908. A53SS_APBADDR_ETM_CPU0_TRCPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-8773. A53SS_APBADDR_ETM_CPU0_TRCPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	The IMPLEMENTATION DEFINED manufacturing revision number for the implementation. After silicon is available, if metal fixes are necessary, the manufacturer can alter the top metal layer so that this field can indicate any post-fab silicon changes.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.364 A53SS_APBADDR_ETM_CPU0_TRCCIDR0 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCIDR0 Register (Offset = FF0h) [reset = Dh]

Component Identification Register 0

Return to Summary Table

Table 14-8774. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FF0h**

Figure 14-2909. A53SS_APBADDR_ETM_CPU0_TRCCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-8776. A53SS_APBADDR_ETM_CPU0_TRCCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.365 A53SS_APBADDR_ETM_CPU0_TRCCIDR1 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCIDR1 Register (Offset = FF4h) [reset = 90h]

Component Identification Register 1

Return to Summary Table

Table 14-8777. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FF4h**

Figure 14-2910. A53SS_APBADDR_ETM_CPU0_TRCCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-8779. A53SS_APBADDR_ETM_CPU0_TRCCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, to indicate that the ETM is a debug component, with CoreSight architecture compliant management registers.
3:0	PRMBL_1	R/W	0h	Preamble. Must read as 0x0.

14.3.1.1.2.366 A53SS_APBADDR_ETM_CPU0_TRCCIDR2 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCIDR2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register 2

Return to Summary Table

Table 14-8780. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FF8h**

Figure 14-2911. A53SS_APBADDR_ETM_CPU0_TRCCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-8782. A53SS_APBADDR_ETM_CPU0_TRCCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.367 A53SS_APBADDR_ETM_CPU0_TRCCIDR3 Register

1 A53SS_APBADDR_ETM_CPU0_TRCCIDR3 Register (Offset = FFCh) [reset = B1h]

Component Identification Register 3

Return to Summary Table

Table 14-8783. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3004 0FFCh**

Figure 14-2912. A53SS_APBADDR_ETM_CPU0_TRCCIDR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCCIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">B1h</td></tr>
</table>

Table 14-8785. A53SS_APBADDR_ETM_CPU0_TRCCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.368 A53SS_APBADDR_DBG_CPU1_EDESR Register

1 A53SS_APBADDR_DBG_CPU1_EDESR Register (Offset = 20h) [reset = 0h]

External Debug Event Status Register

Return to Summary Table

Table 14-8786. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0020h**

Figure 14-2913. A53SS_APBADDR_DBG_CPU1_EDESR Name Register

31	30	29	28	27	26	25	24
RES0_EDESR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDESR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDESR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDESR_31_3					SS	RC	OSUC
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-8788. A53SS_APBADDR_DBG_CPU1_EDESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDESR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step debug event pending. Possible values of this field are: 0 Reading this means that a Halting step debug event is not pending. Writing this means no action. 1 Reading this means that a Halting step debug event is pending. Writing this clears the pending Halting step debug event.
1	RC	R/W	0h	Reset catch debug event pending. Possible values of this field are: 0 Reading this means that a Reset catch debug event is not pending. Writing this means no action. 1 Reading this means that a Reset catch debug event is pending. Writing this clears the pending Reset catch debug event.
0	OSUC	R/W	0h	OS unlock debug event pending. Possible values of this field are: 0 Reading this means that an OS unlock catch debug event is not pending. Writing this means no action. 1 Reading this means that an OS unlock catch debug event is pending. Writing this clears the pending OS unlock catch debug event.

14.3.1.1.2.369 A53SS_APBADDR_DBG_CPU1_EDECR Register

1 A53SS_APBADDR_DBG_CPU1_EDECR Register (Offset = 24h) [reset = 0h]

External Debug Execution Control Register

Return to Summary Table

Table 14-8789. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0024h**

Figure 14-2914. A53SS_APBADDR_DBG_CPU1_EDECR Name Register

31	30	29	28	27	26	25	24
RES0_EDECR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDECR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDECR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDECR_31_3					SS	RCE	OSUCE
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-8791. A53SS_APBADDR_DBG_CPU1_EDECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDECR_31_3	R/W	0h	Reserved, RES0.
2	SS	R/W	0h	Halting step enable. Possible values of this field are: 0 Halting step debug event disabled. 1 Halting step debug event enabled. If the value of EDECR.SS is changed when the processor is in Non-debug state, the resulting value of EDECR.SS is UNKNOWN.
1	RCE	R/W	0h	Reset catch enable. Possible values of this field are: 0 Reset catch debug event disabled. 1 Reset catch debug event enabled.
0	OSUCE	R/W	0h	OS unlock catch enabled. Possible values of this field are: 0 OS unlock catch debug event disabled. 1 OS unlock catch debug event enabled.

14.3.1.1.2.370 A53SS_APBADDR_DBG_CPU1_EDWAR_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_EDWAR_31_0 Register (Offset = 30h) [reset = 0h]

External Debug Watchpoint Address Register (low word)

Return to Summary Table

Table 14-8792. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0030h**

Figure 14-2915. A53SS_APBADDR_DBG_CPU1_EDWAR_31_0 Name Register

31	30	29	28	27	26	25	24
EDWAR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_31_0							
R/W							
0h							

Table 14-8794. A53SS_APBADDR_DBG_CPU1_EDWAR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_31_0	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.371 A53SS_APBADDR_DBG_CPU1_EDWAR_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_EDWAR_63_32 Register (Offset = 34h) [reset = 0h]

External Debug Watchpoint Address Register (high word)

Return to Summary Table

Table 14-8795. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0034h**

Figure 14-2916. A53SS_APBADDR_DBG_CPU1_EDWAR_63_32 Name Register

31	30	29	28	27	26	25	24
EDWAR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDWAR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDWAR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDWAR_63_32							
R/W							
0h							

Table 14-8797. A53SS_APBADDR_DBG_CPU1_EDWAR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDWAR_63_32	R/W	0h	Watchpoint address. The virtual data address being accessed when a watchpoint debug event was triggered and caused entry to Debug state.UNKNOWN if the processor is not in Debug state, or if Debug state was entered other than for a watchpoint debug event.The address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

14.3.1.1.2.372 A53SS_APBADDR_DBG_CPU1_DBGDTRRX_EL0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGDTRRX_EL0 Register (Offset = 80h) [reset = 0h]

Debug Data Transfer Register Receive

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Table 14-8798. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0080h**

Figure 14-2917. A53SS_APBADDR_DBG_CPU1_DBGDTRRX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRRX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRRX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRRX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRRX_EL0							
R/W							
0h							

Table 14-8800. A53SS_APBADDR_DBG_CPU1_DBGDTRRX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRRX_EL0	R/W	0h	Update DTRRX. Writes to this register update the value in DTRRX and set RXfull to 1.Reads of this register return the last value written to DTRRX and do not change RXfull.

14.3.1.1.2.373 A53SS_APBADDR_DBG_CPU1_EDITR Register

1 A53SS_APBADDR_DBG_CPU1_EDITR Register (Offset = 84h) [reset = 0h]

External Debug Instruction Transfer Register

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Table 14-8801. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0084h**

Figure 14-2918. A53SS_APBADDR_DBG_CPU1_EDITR Name Register

31	30	29	28	27	26	25	24
EDITR							
R/W							
0h							
23	22	21	20	19	18	17	16
EDITR							
R/W							
0h							
15	14	13	12	11	10	9	8
EDITR							
R/W							
0h							
7	6	5	4	3	2	1	0
EDITR							
R/W							
0h							

Table 14-8803. A53SS_APBADDR_DBG_CPU1_EDITR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDITR	R/W	0h	Used in Debug state for passing instructions to the processor for execution

14.3.1.1.2.374 A53SS_APBADDR_DBG_CPU1_EDSCR Register

1 A53SS_APBADDR_DBG_CPU1_EDSCR Register (Offset = 88h) [reset = 0h]

External Debug Status and Control Register

Return to Summary Table

Table 14-8804. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0088h**

Figure 14-2919. A53SS_APBADDR_DBG_CPU1_EDSCR Name Register

31	30	29	28	27	26	25	24
RES0_EDSCR_31_31	RXFULL	TXFULL	ITO	RXO	TXU	PIPEADV	ITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTDIS		TDA	MA	RES0_EDSCR_19_19	NS	RES0_EDSCR_17_17	SDD
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDSCR_15_15	HDE	RW				EL	
R/W	R/W	R/W				R/W	
0h	0h	0h				0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A	ERR	STATUS					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-8806. A53SS_APBADDR_DBG_CPU1_EDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES0_EDSCR_31_31	R/W	0h	Reserved, RES0.
30	RXFULL	R/W	0h	DTRRX full. This bit is RO.
29	TXFULL	R/W	0h	DTRTX full. This bit is RO.
28	ITO	R/W	0h	EDITR overrun. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. ITO is set to 0 on entry to Debug state.
27	RXO	R/W	0h	DTRRX overrun. This bit is RO.
26	TXU	R/W	0h	DTRTX underrun. This bit is RO.
25	PIPEADV	R/W	0h	Pipeline advance. Read-only. Set to 1 every time the processor pipeline retires one or more instructions. Cleared to 0 by a write to EDRCR.CSPA.The architecture does not define precisely when this bit is set to 1. It requires only that this happen periodically in Non-debug state to indicate that software execution is progressing.
24	ITE	R/W	0h	ITR empty. This bit is RO.If the processor is not in Debug state, this bit is UNKNOWN. It is always valid in Debug state.

Table 14-8806. A53SS_APBADDR_DBG_CPU1_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	INTDIS	R/W	0h	Interrupt disable. Disables taking interrupts [including virtual interrupts and System Error interrupts] in Non-Debug state.If external invasive debug is disabled, the value of this field is ignored.If external invasive debug is enabled, the possible values of this field are: 00 Do not disable interrupts 01 Disable interrupts targeting Non-secure EL1. 10 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable interrupts targeting Secure EL1. 11 Disable interrupts targeting only Non-secure EL1 and Non-secure EL2. If external secure invasive debug is enabled, also disable all other interrupts. The value of INTdis does not affect whether an interrupt is a WFI wake-up event, but can mask an interrupt as a WFE wake-up event.If EL3 and EL2 are not implemented, INTdis[0] is RO and reads the same value as INTdis[1], meaning only the values 0b00 and 0b11 can be selected.
21	TDA	R/W	0h	Trap debug registers accesses.
20	MA	R/W	0h	Memory access mode. Controls use of memory-access mode for accessing EDITR and the DCC. This bit is ignored if in Non-debug state and set to zero on entry to Debug state.Possible values of this field are: 0 Normal access mode 1 Memory access mode.
19	RES0_EDSCR_19_19	R/W	0h	Reserved, RES0.
18	NS	R/W	0h	Non-secure status. Read-only. When in Debug state, gives the current security state: 0 Secure state, IsSecure[] == TRUE 1 Non-secure state, IsSecure[] == FALSE. In Non-debug state, this bit is UNKNOWN.
17	RES0_EDSCR_17_17	R/W	0h	Reserved, RES0.
16	SDD	R/W	0h	Secure debug disabled. This bit is RO.On entry to Debug state:If entering in Secure state, SDD is set to 0.If entering in Non-secure state, SDD is set to the inverse of ExternalSecureInvasiveDebugEnabled[].In Debug state, the value of the SDD bit does not change, even if ExternalSecureInvasiveDebugEnabled[] changes.In Non-debug state:SDD returns the inverse of ExternalSecureInvasiveDebugEnabled[]. If the authentication signals that control ExternalSecureInvasiveDebugEnabled[] change, a context synchronization operation is required to guarantee their effect.This bit is unaffected by the Security state of the processor.If EL3 is not implemented and the implementation is Non-secure, this bit is RES1.
15	RES0_EDSCR_15_15	R/W	0h	Reserved, RES0.
14	HDE	R/W	0h	Halting debug mode enable. Possible values of this bit are: 0 Halting debug mode disabled. 1 Halting debug mode enabled.

Table 14-8806. A53SS_APBADDR_DBG_CPU1_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:10	RW	R/W	0h	Exception level register-width status. Read-only. In Debug state, each bit gives the current register width status of each EL: 1111 All exception levels are AArch64 state. 1110 EL0 is AArch32 state. All other exception levels are AArch64 state. 1100 EL0 and EL1 are AArch32 state. All other exception levels are AArch64 state. Never seen if EL2 is not implemented in the current security state. 1000 EL0, EL1, and, if implemented in the current security state, EL2 are AArch32 state. All other exception levels are AArch64 state. 0000 All exception levels are set to AArch32 state [32-bit configuration]. However:If not at EL0: RW[0] == RW[1].If EL2 is not implemented in the current security state: RW[2] == RW[1].If EL3 is not implemented: RW[3] == RW[2].In Non-debug state, this field is RAO.
9:8	EL	R/W	0h	Exception level. Read-only. In Debug state, this gives the current EL of the processor.In Non-debug state, this field is RAZ.
7	A	R/W	0h	System Error interrupt pending. Read-only. In Debug state, indicates whether a SError interrupt is pending:If HCR_EL2.{AMO, TGE} = {1, 0} and in Non-secure EL0 or EL1, a virtual SError interrupt.Otherwise, a physical SError interrupt. 0 No SError interrupt pending. 1 SError interrupt pending. A debugger can read EDSCR to check whether a SError interrupt is pending without having to execute further instructions. A pending SError might indicate data from target memory is corrupted.UNKNOWN in Non-debug state.
6	ERR	R/W	0h	Cumulative error flag. This field is RO. It is set to 1 following exceptions in Debug state and on any signaled overrun or underrun on the DTR or EDITR.

Table 14-8806. A53SS_APBADDR_DBG_CPU1_EDSCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	STATUS	R/W	0h	Debug status flags. This field is RO.The possible values of this field are: 000010 Processor is in Non-debug state. 000001 Processor is restarting [exiting Debug state]. 000111 Breakpoint. 010011 External debug request. 011011 Halting step, normal. 011111 Halting step, exclusive. 100011 OS unlock catch. 100111 Reset catch. 101011 Watchpoint. 101111 HLT instruction. 110011 Software access to debug register. 110111 Exception catch. 111011 Halting step, no syndrome. All other values of STATUS are reserved.

14.3.1.1.2.375 A53SS_APBADDR_DBG_CPU1_DBGDTRTX_EL0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGDTRTX_EL0 Register (Offset = 8Ch) [reset = 0h]

Debug Data Transfer Register Transmit

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Table 14-8807. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 008Ch**

Figure 14-2920. A53SS_APBADDR_DBG_CPU1_DBGDTRTX_EL0 Name Register

31	30	29	28	27	26	25	24
DBGDTRTX_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGDTRTX_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGDTRTX_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGDTRTX_EL0							
R/W							
0h							

Table 14-8809. A53SS_APBADDR_DBG_CPU1_DBGDTRTX_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGDTRTX_EL0	R/W	0h	Return DTRTX. Reads of this register return the value in DTRTX and clear TXfull to 0.Writes of this register update the value in DTRTX and do not change TXfull.

14.3.1.1.2.376 A53SS_APBADDR_DBG_CPU1_EDRCR Register

1 A53SS_APBADDR_DBG_CPU1_EDRCR Register (Offset = 90h) [reset = 0h]

External Debug Reserve Control Register

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Table 14-8810. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0090h**

Figure 14-2921. A53SS_APBADDR_DBG_CPU1_EDRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDRCR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDRCR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDRCR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDRCR_31_5			CBRRQ	CSPA	CSE	RES0_EDRCR_1_0	
R/W			R/W	R/W	R/W	R/W	
0h			0h	0h	0h	0h	

Table 14-8812. A53SS_APBADDR_DBG_CPU1_EDRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_EDRCR_31_5	R/W	0h	Reserved, RES0.
4	CBRRQ	R/W	0h	Allow imprecise entry to Debug state. The actions on Writing to this bit are: 0 No action. 1 Allow imprecise entry to Debug state, for example by canceling pending bus accesses. Setting this bit to 1 allows a debugger to request imprecise entry to Debug state. An External Debug Request debug event must be pending before the debugger sets this bit to 1.This feature is optional. If this feature is not implemented, writes to this bit are ignored.
3	CSPA	R/W	0h	Clear Sticky Pipeline Advance. This bit is used to clear the EDSCR.PipeAdv bit to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.PipeAdv bit to 0.

Table 14-8812. A53SS_APBADDR_DBG_CPU1_EDRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CSE	R/W	0h	Clear Sticky Error. Used to clear the EDSCR cumulative error bits to 0. The actions on Writing to this bit are: 0 No action. 1 Clear the EDSCR.{TXU, RXO, ERR} bits, and, if the processor is in Debug state, the EDSCR.ITO bit, to 0.
1:0	RES0_EDRCR_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.377 A53SS_APBADDR_DBG_CPU1_EDACR Register

1 A53SS_APBADDR_DBG_CPU1_EDACR Register (Offset = 94h) [reset = 0h]

External Debug Auxiliary Control Register

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Table 14-8813. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3011 0094h**

Figure 14-2922. A53SS_APBADDR_DBG_CPU1_EDACR Name Register

31	30	29	28	27	26	25	24
RES0_EDACR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDACR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDACR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDACR_31_0							
R/W							
0h							

Table 14-8815. A53SS_APBADDR_DBG_CPU1_EDACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDACR_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.378 A53SS_APBADDR_DBG_CPU1_EDECCR Register

1 A53SS_APBADDR_DBG_CPU1_EDECCR Register (Offset = 98h) [reset = 0h]

External Debug Exception Catch Control Register

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Table 14-8816. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0098h**

Figure 14-2923. A53SS_APBADDR_DBG_CPU1_EDECCR Name Register

31	30	29	28	27	26	25	24
RES0_EDECCR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDECCR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDECCR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
NSE				SE			
R/W				R/W			
0h				0h			

Table 14-8818. A53SS_APBADDR_DBG_CPU1_EDECCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDECCR_31_8	R/W	0h	Reserved, RES0.
7:4	NSE	R/W	0h	Coarse-grained Non-secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Non-secure exception levels. 0010 Exception catch debug event enabled for Non-secure EL1. 0100 Exception catch debug event enabled for Non-secure EL2. 0110 Exception catch debug event enabled for Non-secure EL1 and EL2. All other values are reserved. Bits [7,4] are reserved, RES0.

Table 14-8818. A53SS_APBADDR_DBG_CPU1_EDECCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SE	R/W	0h	Coarse-grained Secure exception catch. Possible values of this field are: 0000 Exception catch debug event disabled for Secure exception levels. 0010 Exception catch debug event enabled for Secure EL1. 1000 Exception catch debug event enabled for Secure EL3. 1010 Exception catch debug event enabled for Secure EL1 and EL3. All other values are reserved. Bits [2,0] are reserved. RES0. Ignored if ExternalSecureInvasiveDebugEnabled[] == FALSE.

14.3.1.1.2.379 A53SS_APBADDR_DBG_CPU1_EDPCSR_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_EDPCSR_31_0 Register (Offset = A0h) [reset = 0h]

External Debug Program Counter Sample Register (low word)

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Table 14-8819. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 00A0h**

Figure 14-2924. A53SS_APBADDR_DBG_CPU1_EDPCSR_31_0 Name Register

31	30	29	28	27	26	25	24
EDPCSR_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_31_0							
R/W							
0h							

Table 14-8821. A53SS_APBADDR_DBG_CPU1_EDPCSR_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_31_0	R/W	0h	PC Sample low word, EDPCSRlo. Bits [31_0] of the sampled instruction address value. Reading EDPCSRlo has the side-effect of updating EDCIDSR, EDVIDSR, and EDPCSRhi. However:If the processor is in Debug state, or Sample-based profiling is prohibited, EDPCSRlo reads as 0xFFFFFFFF and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.If the processor is in Reset state, the sampled value is unknown and EDCIDSR, EDVIDSR and EDPCSRhi become UNKNOWN.If no instruction has been retired since the processor left Reset state, Debug state, or a state where Non-invasive debug is not permitted, the sampled value is UNKNOWN and EDCIDSR, EDVIDSR, and EDPCSRhi become UNKNOWN.For a read of EDPCSRlo from the memory-mapped interface, if EDLSR.SLK == 1, meaning the Software Lock is locked, then the access has no side-effects. That is, EDCIDSR, EDVIDSR, and EDPCSRhi are unchanged.

14.3.1.1.2.380 A53SS_APBADDR_DBG_CPU1_EDCIDSR Register

1 A53SS_APBADDR_DBG_CPU1_EDCIDSR Register (Offset = A4h) [reset = 0h]

External Debug Context ID Sample Register

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Table 14-8822. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 00A4h**

Figure 14-2925. A53SS_APBADDR_DBG_CPU1_EDCIDSR Name Register

31	30	29	28	27	26	25	24
CONTEXTIDR							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXTIDR							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXTIDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXTIDR							
R/W							
0h							

Table 14-8824. A53SS_APBADDR_DBG_CPU1_EDCIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXTIDR	R/W	0h	The sampled value of CONTEXTIDR_EL1, captured on Reading the low half of EDPCSR.If EL3 is implemented and using AArch32 then CONTEXTIDR is a Banked register, and EDCIDSR samples the current Banked copy of CONTEXTIDR.

14.3.1.1.2.381 A53SS_APBADDR_DBG_CPU1_EDVIDSR Register

1 A53SS_APBADDR_DBG_CPU1_EDVIDSR Register (Offset = A8h) [reset = 0h]

External Debug Virtual Context Sample Register

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Table 14-8825. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 00A8h**

Figure 14-2926. A53SS_APBADDR_DBG_CPU1_EDVIDSR Name Register

31	30	29	28	27	26	25	24
NS	E2	E3	HV	RES0_EDVIDSR_27_8			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RES0_EDVIDSR_27_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDVIDSR_27_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VMID							
R/W							
0h							

Table 14-8827. A53SS_APBADDR_DBG_CPU1_EDVIDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NS	R/W	0h	Non-secure state sample. Indicates the security state associated with the most recent EDPCSR sample.
30	E2	R/W	0h	Exception level 2 status sample. Indicates whether the most recent EDPCSR sample was associated with EL2. If EDVIDSR.NS == 0, this bit is 0.
29	E3	R/W	0h	Exception level 3 status sample. Indicates whether the most recent EDPCSR sample was associated with AArch64 EL3. If EDVIDSR.NS == 1 or the processor was in AArch32 state when EDPCSR was read, this bit is 0.
28	HV	R/W	0h	EDPCSR high half valid. Indicates whether bits [63_32] of the most recent EDPCSR sample are valid. If EDVIDSR.HV == 0, the value of EDPCSR[63_32] is RAZ.
27:8	RES0_EDVIDSR_27_8	R/W	0h	Reserved, RES0.
7:0	VMID	R/W	0h	VMID sample. The value of VTTBR_EL2.VMID associated with the most recent EDPCSR sample. If EDVIDSR.NS == 0 or EDVIDSR.E2 == 1, this field is RAZ.

14.3.1.1.2.382 A53SS_APBADDR_DBG_CPU1_EDPCSR_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_EDPCSR_63_32 Register (Offset = ACh) [reset = 0h]

External Debug Program Counter Sample Register (high word)

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Table 14-8828. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 00ACh**

Figure 14-2927. A53SS_APBADDR_DBG_CPU1_EDPCSR_63_32 Name Register

31	30	29	28	27	26	25	24
EDPCSR_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
EDPCSR_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
EDPCSR_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
EDPCSR_63_32							
R/W							
0h							

Table 14-8830. A53SS_APBADDR_DBG_CPU1_EDPCSR_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDPCSR_63_32	R/W	0h	PC Sample high word, EDPCSRhi. If EDVIDSR.HV == 0 then this field is RAZ, otherwise bits [63_32] of the sampled PC.

14.3.1.1.2.383 A53SS_APBADDR_DBG_CPU1_OSLAR_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_OSLAR_EL1 Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-8831. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0300h**

Figure 14-2928. A53SS_APBADDR_DBG_CPU1_OSLAR_EL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_OSLAR_EL1_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_OSLAR_EL1_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_OSLAR_EL1_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_OSLAR_EL1_31_1</td><td>OSLK</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-8833. A53SS_APBADDR_DBG_CPU1_OSLAR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_OSLAR_EL1_31_1	R/W	0h	Reserved, RES0.
0	OSLK	R/W	0h	On writes to OSLAR_EL1, bit[0] is copied to the OS lock.Use EDPRSR.OSLK to check the current status of the lock.

14.3.1.1.2.384 A53SS_APBADDR_DBG_CPU1_EDPRCR Register

1 A53SS_APBADDR_DBG_CPU1_EDPRCR Register (Offset = 310h) [reset = 0h]

External Debug Power/Reset Control Register

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Table 14-8834. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0310h**

Figure 14-2929. A53SS_APBADDR_DBG_CPU1_EDPRCR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRCR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPRCR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPRCR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_EDPRCR_31_4				COREPURQ	RES0_EDPRCR_2_2	CWRR	CORENPDRQ
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-8836. A53SS_APBADDR_DBG_CPU1_EDPRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDPRCR_31_4	R/W	0h	Reserved, RES0.
3	COREPURQ	R/W	0h	Core powerup request. Allows a debugger to request that the power controller power up the core, enabling access to the debug register in the Core power domain. The actions on Writing to this bit are: 0 No effect. 1 Request the power controller to powerup the core. In an implementation that includes the recommended external debug interface, this bit drives the DBGPWRUPREQ signal.This bit can be read and written when the Core power domain is powered off.The power controller must not allow the Core power domain to switch off while this bit is one.
2	RES0_EDPRCR_2_2	R/W	0h	Reserved, RES0.

Table 14-8836. A53SS_APBADDR_DBG_CPU1_EDPRCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CWRR	R/W	0h	Warm reset request. Write only bit that reads as zero. The actions on Writing to this bit are: 0 No action. 1 Request Warm reset. The processor ignores writes to this bit if any of the following are the case:ExternalInvasiveDebugEnabled[] == FALSE, EL3 is not implemented, and the processor is Non-secure.ExternalSecureInvasiveDebugEnabled[] == FALSE and one of the following is true:EL3 is implemented.The processor is Secure.The Core power domain is either completely off or in a low-power state where the Core power domain registers cannot be accessed.DoubleLockStatus[] == TRUE [OS Double Lock is set].OSLSR.OSLK == 1 [OS lock is locked].In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.
0	CORENPDRQ	R/W	0h	Core no powerdown request. Requests emulation of powerdown. Possible values of this bit are: 0 On a powerdown request, the system powers down the Core power domain. 1 On a powerdown request, the system emulates powerdown of the Core power domain. In this emulation mode the Core power domain is not actually powered down.

14.3.1.1.2.385 A53SS_APBADDR_DBG_CPU1_EDPRSR Register

1 A53SS_APBADDR_DBG_CPU1_EDPRSR Register (Offset = 314h) [reset = 3h]

External Debug Processor Status Register

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Table 14-8837. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0314h**

Figure 14-2930. A53SS_APBADDR_DBG_CPU1_EDPRSR Name Register

31	30	29	28	27	26	25	24
RES0_EDPRSR_31_12							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPRSR_31_12							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPRSR_31_12				SDR	SPMAD	EPMAD	SDAD
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EDAD	DLK	OSLK	HALTED	SR	R	SPD	PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 14-8839. A53SS_APBADDR_DBG_CPU1_EDPRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_EDPRSR_31_12	R/W	0h	Reserved, RES0.
11	SDR	R/W	0h	Sticky debug restart. Set to 1 when the processor exits Debug state and cleared to 0 following reads of EDPRSR. 0 The processor has not restarted since EDPRSR was last read. 1 The processor has restarted since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.
10	SPMAD	R/W	0h	Sticky EPMAD error. Set to 1 if an access returns an error because AllowExternalPMUAccess[] == FALSE. 0 No accesses to the external performance monitors registers have failed since EDPRSR was last read. 1 At least one access to the external performance monitors registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 when following a read of EDPRSR.

Table 14-8839. A53SS_APBADDR_DBG_CPU1_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EPMAD	R/W	0h	External performance monitors access disable status. 0 External performance monitors access enabled. 1 External performance monitors access disabled. If external performance monitors access is not implemented, EPMAD is RAO. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
8	SDAD	R/W	0h	Sticky EDAD error. Set to 1 if an access returns an error because AllowExternalDebugAccess[] == FALSE. 0 No accesses to the external debug registers have failed since EDPRSR was last read. 1 At least one access to the external debug registers has failed since EDPRSR was last read. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR.
7	EDAD	R/W	0h	External debug access disable status. 0 External debug access enabled. 1 External debug access disabled. This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1, or EDPRSR.PU is 0.
6	DLK	R/W	0h	OS Double Lock status bit. 0 OSDLR_EL1.DLK == 0 or EDPRCR.CORENPDRQ == 1 or the processor is in Debug state. 1 OSDLR_EL1.DLK == 1 and EDPRCR.CORENPDRQ == 0 and the processor is in Non-debug state. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
5	OSLK	R/W	0h	OS lock status bit. A read of this bit returns the value of OSLSR_EL1.OSLK.This bit is UNKNOWN on reads if either of EDPRSR.{DLK, R} is 1 or EDPRSR.PU is 0.
4	HALTED	R/W	0h	Halted status bit. Possible values are: 0 EDSCR.STATUS is 0b000010 [processor in Non-debug state]. 1 EDSCR.STATUS is not 0b000010. This bit is UNKNOWN on reads if EDPRSR.PU is 0.
3	SR	R/W	0h	Sticky core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state and has not been reset since the last time EDPRSR was read. 1 The non-debug logic of the processor is in reset state or has been reset since the last time EDPRSR was read. This bit is UNKNOWN on reads if EDPRSR.DLK is 1 or EDPRSR.PU is 0.This bit clears to 0 following a read of EDPRSR if the non-debug logic of the processor is not in reset state.
2	R	R/W	0h	Core reset status bit. Possible values are: 0 The non-debug logic of the processor is not in reset state. 1 The non-debug logic of the processor is in reset state. This bit is UNKNOWN on reads if either EDPRSR.DLK is 1 or EDPRSR.PU is 0.

Table 14-8839. A53SS_APBADDR_DBG_CPU1_EDPRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SPD	R/W	1h	Sticky core power-down status bit.This bit is set to 1 on Cold reset to indicate the state of the debug registers has been lost. Since a Cold reset is required on powering up the processor, this usually indicates the Core power domain has been completely powered off.Possible values are: 0 If the Core power domain is off [EDPRSR.PU is 0], it is not known whether the state of the debug registers in the Core power domain is lost. Otherwise, the Core power domain is on, and the state of the debug registers in the Core power domain has not been lost. 1 The state of the debug registers in the Core power domain is lost. This bit is UNKNOWN on reads if both EDPRSR.DLK and EDPRSR.PU are 1.This bit clears to 0 following a read of EDPRSR if the processor is not in the powered down state. There are two logical power off states for the Core power domain:RetentionThe states of the debug registers, including EDPRSR.SPD, in the Core power domain is preserved, and restored on leaving retention state.Power-downThe states of the debug registers in the Core power domain is lost, and a Cold reset is asserted on leaving power-down state.In these states, it is IMPLEMENTATION DEFINED whether:EDPRSR.SPD shows whether the state of the debug registers in the Core power domain has been lost since the last time EDPRSR was read when the Core power domain was on.EDPRSR.SPD reads-as-zero.EDPRSR.SPD is not cleared following a read of EDPRSR in these states.This means it is IMPLEMENTATION DEFINED whether a processor implements EDPRSR.SPD as:Fixed RAZ when in one or both of the retention and power-down states.Retaining its previous value when in the retention state.Fixed RAO in the power-down state.Note that this definition does not allow EDPRSR.SPD to be fixed RAO in the low-power retention state, as the state of the debug registers in the Core power domain is not lost by entering this state. However, the bit can be read as 1 in this state if the state of the registers was lost before entering this state [i.e. EDPRSR has not been read since the last Cold reset].ARM recommends that an implementation make EDPRSR.SPD fixed RAO when in the power-down state, particularly if it does not support a low-power retention state.
0	PU	R/W	1h	Core power-up status bit. Indicates whether the Core power domain debug registers can be accessed: 0 Core is in a low-power or power-down state where the debug registers cannot be accessed. 1 Core is in a power-up state where the debug registers can be accessed.

14.3.1.1.2.386 A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_31_0 Register (Offset = 400h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8840. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0400h**

Figure 14-2931. A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_31_0							
R/W							
0h							

Table 14-8842. A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.387 A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_63_32 Register (Offset = 404h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR0_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8843. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0404h**

Figure 14-2932. A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR0_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR0_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR0_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR0_EL1_63_32							
R/W							
0h							

Table 14-8845. A53SS_APBADDR_DBG_CPU1_DBGBVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR0_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.388 A53SS_APBADDR_DBG_CPU1_DBGBCR0_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBCR0_EL1 Register (Offset = 408h) [reset = 0h]

Debug Breakpoint Control Register 0

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Table 14-8846. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0408h**

Figure 14-2933. A53SS_APBADDR_DBG_CPU1_DBGBCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR0_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR0_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR0_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8848. A53SS_APBADDR_DBG_CPU1_DBGBCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR0_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-8848. A53SS_APBADDR_DBG_CPU1_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR0_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-8848. A53SS_APBADDR_DBG_CPU1_DBGBCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR0_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.389 A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_31_0 Register (Offset = 410h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8849. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0410h**

Figure 14-2934. A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_31_0							
R/W							
0h							

Table 14-8851. A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.390 A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_63_32 Register (Offset = 414h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR1_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8852. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0414h**

Figure 14-2935. A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR1_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR1_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR1_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR1_EL1_63_32							
R/W							
0h							

Table 14-8854. A53SS_APBADDR_DBG_CPU1_DBGBVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR1_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.391 A53SS_APBADDR_DBG_CPU1_DBGBCR1_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBCR1_EL1 Register (Offset = 418h) [reset = 0h]

Debug Breakpoint Control Register 1

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Table 14-8855. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0418h**

Figure 14-2936. A53SS_APBADDR_DBG_CPU1_DBGBCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR1_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR1_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR1_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8857. A53SS_APBADDR_DBG_CPU1_DBGBCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR1_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-8857. A53SS_APBADDR_DBG_CPU1_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR1_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-8857. A53SS_APBADDR_DBG_CPU1_DBGBCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR1_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.392 A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_31_0 Register (Offset = 420h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8858. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0420h**

Figure 14-2937. A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR2_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR2_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR2_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR2_EL1_31_0							
R/W							
0h							

Table 14-8860. A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.393 A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_63_32 Register (Offset = 424h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR2_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8861. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0424h**

Figure 14-2938. A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DBGBVR2_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DBGBVR2_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DBGBVR2_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DBGBVR2_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8863. A53SS_APBADDR_DBG_CPU1_DBGBVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR2_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.394 A53SS_APBADDR_DBG_CPU1_DBGBCR2_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBCR2_EL1 Register (Offset = 428h) [reset = 0h]

Debug Breakpoint Control Register 2

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Table 14-8864. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0428h**

Figure 14-2939. A53SS_APBADDR_DBG_CPU1_DBGBCR2_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR2_EL1_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BT				LBN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	RES0_DBGBCR2_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			RES0_DBGBCR2_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8866. A53SS_APBADDR_DBG_CPU1_DBGBCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR2_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-8866. A53SS_APBADDR_DBG_CPU1_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR2_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-8866. A53SS_APBADDR_DBG_CPU1_DBGBCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR2_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.395 A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_31_0 Register (Offset = 430h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8867. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0430h**

Figure 14-2940. A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR3_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR3_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR3_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR3_EL1_31_0							
R/W							
0h							

Table 14-8869. A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.396 A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_63_32 Register (Offset = 434h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR3_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8870. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0434h**

Figure 14-2941. A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DBGBVR3_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DBGBVR3_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DBGBVR3_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DBGBVR3_EL1_63_32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8872. A53SS_APBADDR_DBG_CPU1_DBGBVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR3_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.397 A53SS_APBADDR_DBG_CPU1_DBGBCR3_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBCR3_EL1 Register (Offset = 438h) [reset = 0h]

Debug Breakpoint Control Register 3

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Table 14-8873. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0438h**

Figure 14-2942. A53SS_APBADDR_DBG_CPU1_DBGBCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR3_EL1_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BT				LBN			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	RES0_DBGBCR3_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			RES0_DBGBCR3_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8875. A53SS_APBADDR_DBG_CPU1_DBGBCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR3_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-8875. A53SS_APBADDR_DBG_CPU1_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR3_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-8875. A53SS_APBADDR_DBG_CPU1_DBGBCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR3_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.398 A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_31_0 Register (Offset = 440h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8876. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0440h**

Figure 14-2943. A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_31_0							
R/W							
0h							

Table 14-8878. A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.399 A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_63_32 Register (Offset = 444h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR4_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8879. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0444h**

Figure 14-2944. A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR4_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR4_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR4_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR4_EL1_63_32							
R/W							
0h							

Table 14-8881. A53SS_APBADDR_DBG_CPU1_DBGBVR4_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR4_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.400 A53SS_APBADDR_DBG_CPU1_DBGBCR4_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBCR4_EL1 Register (Offset = 448h) [reset = 0h]

Debug Breakpoint Control Register 4

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Table 14-8882. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0448h**

Figure 14-2945. A53SS_APBADDR_DBG_CPU1_DBGBCR4_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR4_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR4_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR4_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8884. A53SS_APBADDR_DBG_CPU1_DBGBCR4_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR4_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-8884. A53SS_APBADDR_DBG_CPU1_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR4_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-8884. A53SS_APBADDR_DBG_CPU1_DBGBCR4_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR4_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.401 A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_31_0 Register (Offset = 450h) [reset = 0h]

Debug Breakpoint Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8885. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0450h**

Figure 14-2946. A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_31_0							
R/W							
0h							

Table 14-8887. A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_31_0	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.402 A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_63_32 Register (Offset = 454h) [reset = 0h]

Debug Breakpoint Extended Value Registers. Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR5_EL1. Multiple uses of this register refer to ARMv8

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Table 14-8888. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0454h**

Figure 14-2947. A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
DBGBVR5_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGBVR5_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGBVR5_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGBVR5_EL1_63_32							
R/W							
0h							

Table 14-8890. A53SS_APBADDR_DBG_CPU1_DBGBVR5_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGBVR5_EL1_63_32	R/W	0h	Holds a virtual address or a VMID and/or a context ID for use in breakpoint matching

14.3.1.1.2.403 A53SS_APBADDR_DBG_CPU1_DBGBCR5_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGBCR5_EL1 Register (Offset = 458h) [reset = 0h]

Debug Breakpoint Control Register 5

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Table 14-8891. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0458h**

Figure 14-2948. A53SS_APBADDR_DBG_CPU1_DBGBCR5_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGBCR5_EL1_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
BT				LBN			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SSC		HMC	RES0_DBGBCR5_EL1_12_9				BAS
R/W		R/W	R/W				R/W
0h		0h	0h				0h
7	6	5	4	3	2	1	0
BAS			RES0_DBGBCR5_EL1_4_3		PMC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8893. A53SS_APBADDR_DBG_CPU1_DBGBCR5_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_DBGBCR5_EL1_31_24	R/W	0h	Reserved, RES0.

Table 14-8893. A53SS_APBADDR_DBG_CPU1_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	BT	R/W	0h	Breakpoint Type. Possible values are: 0000 Unlinked instruction address match. 0001 Linked instruction address match. 0010 Unlinked context ID match. 0011 Linked context ID match 0100 Unlinked instruction address mismatch. 0101 Linked instruction address mismatch. 1000 Unlinked VMID match. 1001 Linked VMID match. 1010 Unlinked VMID and context ID match. 1011 Linked VMID and context ID match. The field breaks down as follows:BT[3:1]: Base type.000Match address. DBGBVR<n>_EL1 is the address of an instruction.010Mismatch address. Behaves as type 0b000 if in an AArch64 translation, or if halting debug-mode is enabled and halting is allowed. Otherwise, DBGBVR<n>_EL1 is the address of an instruction to be stepped.001Match context ID. DBGBVR<n>_EL1[31_0] is a context ID.100Match VMID. DBGBVR<n>_EL1[39:32] is a VMID.101Match VMID and context ID. DBGBVR<n>_EL1[31_0] is a context ID, and DBGBVR<n>_EL1[39:32] is a VMID.BT[0]: Enable linking.If the breakpoint is not context-aware, BT[3] and BT[1] are RES0. If EL2 is not implemented, BT[3] is RES0. If EL1 using AArch32 is not implemented, BT[2] is RES0.The values 011x and 11xx are reserved, but must behave as if the breakpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields.
12:9	RES0_DBGBCR5_EL1_12_9	R/W	0h	Reserved, RES0.

Table 14-8893. A53SS_APBADDR_DBG_CPU1_DBGBCR5_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	BAS	R/W	0h	Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and execution state. In an AArch64-only implementation, this field is reserved, RES1. Otherwise:BAS[2] and BAS[0] are read/write.BAS[3] and BAS[1] are read-only copies of BAS[2] and BAS[0] respectively.The values 0b0011 and 0b1100 are only supported if AArch32 is supported at any exception level.The permitted values depend on the breakpoint type.For Address match breakpoints in either AArch32 or AArch64 state:BASMatch instruction atConstraint for debuggers0b0011DBGBVR<n>_EL1Use for T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for A64 and A32 instructions.0b0000 is reserved and must behave as if the breakpoint is disabled or map to a permitted value.For Address mismatch breakpoints in an AArch32 stage 1 translation regime:BASStep instruction atConstraint for debuggers0b0000-Use for a match anywhere breakpoint.0b0011DBGBVR<n>_EL1Use for stepping T32 and T32EE instructions.0b1100DBGBVR<n>_EL1+2Use for stepping T32 and T32EE instructions.0b1111DBGBVR<n>_EL1Use for stepping A64 and A32 instructions.For Context matching breakpoints, this field is RES1 and ignored.
4:3	RES0_DBGBCR5_EL1_4_3	R/W	0h	Reserved, RES0.
2:1	PMC	R/W	0h	Privilege mode control. Determines the exception level or levels at which a breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable breakpoint DBGBVR<n>_EL1. Possible values are: 0 Breakpoint disabled. 1 Breakpoint enabled.

14.3.1.1.2.404 A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_31_0 Register (Offset = 800h) [reset = 0h]

Debug Watchpoint Value Register 0

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Table 14-8894. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0800h**

Figure 14-2949. A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR0_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-8896. A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR0_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.405 A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_63_32 Register (Offset = 804h) [reset = 0h]

Debug Watchpoint Extended Value Register 0

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Table 14-8897. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0804h**

Figure 14-2950. A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_63_32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESS</td><td>VA</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8899. A53SS_APBADDR_DBG_CPU1_DBGWVR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.406 A53SS_APBADDR_DBG_CPU1_DBGWCR0_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWCR0_EL1 Register (Offset = 808h) [reset = 0h]

Debug Watchpoint Control Register 0

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Table 14-8900. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0808h**

Figure 14-2951. A53SS_APBADDR_DBG_CPU1_DBGWCR0_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR0_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR0_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8902. A53SS_APBADDR_DBG_CPU1_DBGWCR0_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR0_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR0_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-8902. A53SS_APBADDR_DBG_CPU1_DBGWCR0_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.407 A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_31_0 Register (Offset = 810h) [reset = 0h]

Debug Watchpoint Value Register 1

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Table 14-8903. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0810h**

Figure 14-2952. A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR1_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-8905. A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR1_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.408 A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_63_32 Register (Offset = 814h) [reset = 0h]

Debug Watchpoint Extended Value Register 1

Return to Summary Table

Table 14-8906. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0814h**

Figure 14-2953. A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-8908. A53SS_APBADDR_DBG_CPU1_DBGWVR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.409 A53SS_APBADDR_DBG_CPU1_DBGWCR1_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWCR1_EL1 Register (Offset = 818h) [reset = 0h]

Debug Watchpoint Control Register 1

Return to Summary Table

Table 14-8909. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0818h**

Figure 14-2954. A53SS_APBADDR_DBG_CPU1_DBGWCR1_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR1_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR1_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8911. A53SS_APBADDR_DBG_CPU1_DBGWCR1_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR1_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR1_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-8911. A53SS_APBADDR_DBG_CPU1_DBGWCR1_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.410 A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_31_0 Register (Offset = 820h) [reset = 0h]

Debug Watchpoint Value Register 2

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Table 14-8912. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0820h**

Figure 14-2955. A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	22	21	20	19	18	17	16
VA							
R/W							
0h							
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA						RES0_DBGWVR2_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-8914. A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR2_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.411 A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_63_32 Register (Offset = 824h) [reset = 0h]

Debug Watchpoint Extended Value Register 2

Return to Summary Table

Table 14-8915. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0824h**

Figure 14-2956. A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-8917. A53SS_APBADDR_DBG_CPU1_DBGWVR2_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.412 A53SS_APBADDR_DBG_CPU1_DBGWCR2_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWCR2_EL1 Register (Offset = 828h) [reset = 0h]

Debug Watchpoint Control Register 2

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Table 14-8918. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0828h**

Figure 14-2957. A53SS_APBADDR_DBG_CPU1_DBGWCR2_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR2_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_DBGWCR2_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8920. A53SS_APBADDR_DBG_CPU1_DBGWCR2_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR2_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR2_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-8920. A53SS_APBADDR_DBG_CPU1_DBGWCR2_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.413 A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_31_0 Register (Offset = 830h) [reset = 0h]

Debug Watchpoint Value Register 3

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Table 14-8921. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0830h**

Figure 14-2958. A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
VA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA						RES0_DBGWVR3_EL1_31_0_1_0	
R/W						R/W	
0h						0h	

Table 14-8923. A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.
1:0	RES0_DBGWVR3_EL1_31_0_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.414 A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_63_32 Register (Offset = 834h) [reset = 0h]

Debug Watchpoint Extended Value Register 3

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Table 14-8924. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0834h**

Figure 14-2959. A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RESS							
R/W							
0h							
23	22	21	20	19	18	17	16
RESS							VA
R/W							R/W
0h							0h
15	14	13	12	11	10	9	8
VA							
R/W							
0h							
7	6	5	4	3	2	1	0
VA							
R/W							
0h							

Table 14-8926. A53SS_APBADDR_DBG_CPU1_DBGWVR3_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESS	R/W	0h	Reserved, Sign extended. Hardwired to the value of the sign bit, bit [48]. Hardware and software must treat this field as RES0 if bit[48] is 0, and as RES1 if bit[48] is 1.
16:0	VA	R/W	0h	Bits[48:2] of the address value for comparison.ARM deprecates setting DBGWVR<n>_EL1[2] == 1.

14.3.1.1.2.415 A53SS_APBADDR_DBG_CPU1_DBGWCR3_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGWCR3_EL1 Register (Offset = 838h) [reset = 0h]

Debug Watchpoint Control Register 3

Return to Summary Table

Table 14-8927. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0838h**

Figure 14-2960. A53SS_APBADDR_DBG_CPU1_DBGWCR3_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGWCR3_EL1_31_29			MASK				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RES0_DBGWCR3_EL1_23_21			WT	LBN			
R/W			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
SSC		HMC	BAS				
R/W		R/W	R/W				
0h		0h	0h				
7	6	5	4	3	2	1	0
BAS			LSC		PAC		E
R/W			R/W		R/W		R/W
0h			0h		0h		0h

Table 14-8929. A53SS_APBADDR_DBG_CPU1_DBGWCR3_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_DBGWCR3_EL1_31_29	R/W	0h	Reserved, RES0.
28:24	MASK	R/W	0h	Address mask. Only objects up to 2GB can be watched using a single mask. 00000 No mask. 00001 Reserved. 00010 Reserved. Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits [0x00000007 mask for address] to 0b11111 masking 31 address bits [0x7FFFFFFF mask for address].
23:21	RES0_DBGWCR3_EL1_23_21	R/W	0h	Reserved, RES0.
20	WT	R/W	0h	Watchpoint type. Possible values are: 0 Unlinked data address match. 1 Linked data address match.
19:16	LBN	R/W	0h	Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

Table 14-8929. A53SS_APBADDR_DBG_CPU1_DBGWCR3_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SSC	R/W	0h	Security state control. Determines the security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.
13	HMC	R/W	0h	Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.
12:5	BAS	R/W	0h	Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.BASDescriptionxxxxxxx1Match byte at DBGWVR<n>_EL1xxxxxx1xMatch byte at DBGWVR<n>_EL1+1xxxxx1xxMatch byte at DBGWVR<n>_EL1+2xxxx1xxxMatch byte at DBGWVR<n>_EL1+3In cases where DBGWVR<n>_EL1 addresses a double-word:BASDescription, if DBGWVR<n>_EL1[2] == 0xxx1xxxxMatch byte at DBGWVR<n>_EL1+4xx1xxxxxMatch byte at DBGWVR<n>_EL1+5x1xxxxxxMatch byte at DBGWVR<n>_EL1+61xxxxxxxMatch byte at DBGWVR<n>_EL1+7If DBGWVR<n>_EL1[2] == 1, only BAS[3:0] is used. ARM deprecates setting DBGWVR<n>_EL1 == 1.The valid values for BAS are 0b0000000, or a binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software.If BAS is zero, no bytes are watched by this watchpoint.Ignored if E is 0.
4:3	LSC	R/W	0h	Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are: 01 Match instructions that load from a watchpointed address. 10 Match instructions that store to a watchpointed address. 11 Match instructions that load from or store to a watchpointed address. All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.Ignored if E is 0.
2:1	PAC	R/W	0h	Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.
0	E	R/W	0h	Enable watchpoint n. Possible values are: 0 Watchpoint disabled. 1 Watchpoint enabled.

14.3.1.1.2.416 A53SS_APBADDR_DBG_CPU1_MIDR_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_MIDR_EL1 Register (Offset = D00h) [reset = 410FD034h]

Main ID Register

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Table 14-8930. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D00h**

Figure 14-2961. A53SS_APBADDR_DBG_CPU1_MIDR_EL1 Name Register

31	30	29	28	27	26	25	24
IMPLEMENTER							
R/W							
41h							
23	22	21	20	19	18	17	16
VARIANT				ARCHITECTURE			
R/W				R/W			
0h				Fh			
15	14	13	12	11	10	9	8
PARTNUM							
R/W							
D03h							
7	6	5	4	3	2	1	0
PARTNUM				REVISION			
R/W				R/W			
D03h				4h			

Table 14-8932. A53SS_APBADDR_DBG_CPU1_MIDR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IMPLEMENTER	R/W	41h	The Implementer code. This field must hold an implementer code that has been assigned by ARM.
23:20	VARIANT	R/W	0h	An IMPLEMENTATION DEFINED variant number. Typically this field is used to distinguish between different product variants or major revisions of a product.
19:16	ARCHITECTURE	R/W	Fh	
15:4	PARTNUM	R/W	D03h	An IMPLEMENTATION DEFINED primary part number for the device. On processors implemented by ARM if the top four bits of the primary part number are 0x0 or 0x7 the variant and architecture are encoded differently
3:0	REVISION	R/W	4h	An IMPLEMENTATION DEFINED revision number for the device

14.3.1.1.2.417 A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_31_0 Register (Offset = D20h) [reset = 1002222h]

Processor Feature Register 0 (low word)

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Table 14-8933. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D20h**

Figure 14-2962. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_31_0_31_28				GIC			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
ADVSIMD				FP			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
EL3				EL2			
R/W				R/W			
2h				2h			
7	6	5	4	3	2	1	0
EL1				EL0			
R/W				R/W			
2h				2h			

Table 14-8935. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_ID_AA64PFR0_EL1_31_0_31_28	R/W	0h	Reserved, RES0.
27:24	GIC	R/W	1h	GIC system register interface. Permitted values are: 0000 No GIC system registers are supported. 0001 GICv3 system registers are supported. All other values are reserved.
23:20	ADVSIMD	R/W	0h	Advanced SIMD. Permitted values are: 0000 Advanced SIMD is implemented. 1111 Advanced SIMD is not implemented. All other values are reserved.
19:16	FP	R/W	0h	Floating-point. Permitted values are: 0000 Floating-point is implemented. 1111 Floating-point is not implemented. All other values are reserved.

Table 14-8935. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	EL3	R/W	2h	EL3 exception level handling. Permitted values are: 0000 EL3 is not implemented. 0001 EL3 can be executed in AArch64 state only. 0010 EL3 can be executed in either AArch64 or AArch32 state. All other values are reserved.
11:8	EL2	R/W	2h	EL2 exception level handling. Permitted values are: 0000 EL2 is not implemented. 0001 EL2 can be executed in AArch64 state only. 0010 EL2 can be executed in either AArch64 or AArch32 state. All other values are reserved.
7:4	EL1	R/W	2h	EL1 exception level handling. Permitted values are: 0000 EL1 is not implemented. 0001 EL1 can be executed in AArch64 state only. 0010 EL1 can be executed in either AArch64 or AArch32 state. All other values are reserved.
3:0	EL0	R/W	2h	EL0 exception level handling. Permitted values are: 0000 EL0 is not implemented. 0001 EL0 can be executed in AArch64 state only. 0010 EL0 can be executed in either AArch64 or AArch32 state. All other values are reserved.

14.3.1.1.2.418 A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_63_32 Register (Offset = D24h) [reset = 0h]

Processor Feature Register 0 (high word)

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Table 14-8936. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D24h**

Figure 14-2963. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-8938. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.419 A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_31_0 Register (Offset = D28h) [reset = 10305106h]

Debug Feature Register 0 (low word)

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Table 14-8939. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D28h**

Figure 14-2964. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
CTX_CMPS				RES0_ID_AA64DFR0_EL1_31_0_27_24			
R/W				R/W			
1h				0h			
23	22	21	20	19	18	17	16
WRPS				RES0_ID_AA64DFR0_EL1_31_0_19_16			
R/W				R/W			
3h				0h			
15	14	13	12	11	10	9	8
BRPS				PMUVER			
R/W				R/W			
5h				1h			
7	6	5	4	3	2	1	0
TRACEVER				DEBUGVER			
R/W				R/W			
0h				6h			

Table 14-8941. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CTX_CMPS	R/W	1h	Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.
27:24	RES0_ID_AA64DFR0_EL1_31_0_27_24	R/W	0h	Reserved, RES0.
23:20	WRPS	R/W	3h	Number of watchpoints, minus 1. The value of 0b0000 is reserved.
19:16	RES0_ID_AA64DFR0_EL1_31_0_19_16	R/W	0h	Reserved, RES0.
15:12	BRPS	R/W	5h	Number of breakpoints, minus 1. The value of 0b0000 is reserved.
11:8	PMUVER	R/W	1h	Performance Monitors extension version. Indicates whether system register interface to Performance Monitors extension is implemented. Permitted values are: 0000 Performance Monitors extension system registers not implemented. 0001 Performance Monitors extension system registers implemented, PMUv3. 1111 IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. All other values are reserved.

Table 14-8941. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRACEVER	R/W	0h	Trace extension. Indicates whether system register interface to Trace extension is implemented. Permitted values are: 0000 Trace extension system registers not implemented. 0001 Trace extension system registers implemented. All other values are reserved.A value of 0b0000 only indicates that no system register interface to the trace extension is implemented. A trace extension may nevertheless be implemented without a system register interface.
3:0	DEBUGVER	R/W	6h	Debug architecture version. Indicates presence of v8-A debug architecture. 0110 v8-A debug architecture. All other values are reserved.

14.3.1.1.2.420 A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_63_32 Register (Offset = D2Ch) [reset = 0h]

Debug Feature Register 0 (high word)

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Table 14-8942. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D2Ch**

Figure 14-2965. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-8944. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.421 A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_31_0 Register (Offset = D30h) [reset = 11120h]

Instruction Set Attribute Register 0 (low word)

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Table 14-8945. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D30h**

Figure 14-2966. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_31_0_31_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_ID_AA64ISAR0_EL1_31_0_31_20				CRC32			
R/W				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SHA2				SHA1			
R/W				R/W			
1h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AES				RES0_ID_AA64ISAR0_EL1_31_0_3_0			
R/W				R/W			
2h				0h			

Table 14-8947. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_ID_AA64ISAR0_EL1_31_0_31_20	R/W	0h	Reserved, RES0.
19:16	CRC32	R/W	1h	CRC32 instructions in AArch64. Possible values of this field are: 0000 No CRC32 instructions implemented. 0001 CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX instructions implemented. All other values are reserved.This field must have the same value as ID_ISAR5.CRC32. The architecture requires that if CRC32 is supported in one Execution state, it must be supported in both Execution states.
15:12	SHA2	R/W	1h	SHA2 instructions in AArch64. Possible values of this field are: 0000 No SHA2 instructions implemented. 0001 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions implemented. All other values are reserved.

Table 14-8947. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	SHA1	R/W	1h	SHA1 instructions in AArch64. Possible values of this field are: 0000 No SHA1 instructions implemented. 0001 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions implemented. All other values are reserved.
7:4	AES	R/W	2h	AES instructions in AArch64. Possible values of this field are: 0000 No AES instructions implemented. 0001 AESE, AESD, AESMC, and AESIMC instructions implemented. 0010 As for 0b0001, plus PMULL/PMULL2 instructions operating on 64-bit data quantities.
3:0	RES0_ID_AA64ISAR0_EL1_31_0_3_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.422 A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_63_32 Register (Offset = D34h) [reset = 0h]

Instruction Set Attribute Register 0 (high word)

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Table 14-8948. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D34h**

Figure 14-2967. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-8950. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.423 A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_31_0 Register (Offset = D38h) [reset = 1122h]

Memory Model Feature Register 0 (low word)

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Table 14-8951. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D38h**

Figure 14-2968. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
TGRAN4				TGRAN64			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
TGRAN16				BIGENDEL0			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SNSMEM				BIGEND			
R/W				R/W			
1h				1h			
7	6	5	4	3	2	1	0
ASIDBITS				PARANGE			
R/W				R/W			
2h				2h			

Table 14-8953. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TGRAN4	R/W	0h	Support for 4 Kbyte memory translation granule size. Permitted values are: 0000 4 KB granule supported. 1111 4 KB granule not supported. All other values are reserved.
27:24	TGRAN64	R/W	0h	Support for 64 Kbyte memory translation granule size. Permitted values are: 0000 64 KB granule supported. 1111 64 KB granule not supported. All other values are reserved.
23:20	TGRAN16	R/W	0h	Support for 16 Kbyte memory translation granule size. Permitted values are: 0000 16 KB granule not supported. 0001 16 KB granule supported. All other values are reserved.

Table 14-8953. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	BIGENDEL0	R/W	0h	Mixed-endian support at EL0 only. Permitted values are: 0000 No mixed-endian support at EL0. The SCTLR_EL1.E0E bit has a fixed value. 0001 Mixed-endian support at EL0. The SCTLR_EL1.E0E bit can be configured. All other values are reserved.This field is invalid and is RES0 if the BigEnd field, bits [11:8], is not 0b0000.
15:12	SNSMEM	R/W	1h	Secure versus Non-secure Memory distinction. Permitted values are: 0000 Does not support a distinction between Secure and Non-secure Memory. 0001 Does support a distinction between Secure and Non-secure Memory. All other values are reserved.
11:8	BIGEND	R/W	1h	Mixed-endian configuration support. Permitted values are: 0000 No mixed-endian support. The SCTLR_ELx.EE bits have a fixed value. See the BigEndEL0 field, bits[19:16], for whether EL0 supports mixed-endian. 0001 Mixed-endian support. The SCTLR_ELx.EE and SCTLR_EL1.E0E bits can be configured. All other values are reserved.
7:4	ASIDBITS	R/W	2h	Number of ASID bits. Permitted values are: 0000 8 bits. 0010 16 bits. All other values are reserved.
3:0	PARANGE	R/W	2h	Physical Address range supported. Permitted values are: 0000 32 bits, 4 GB. 0001 36 bits, 64 GB. 0010 40 bits, 1 TB. 0011 42 bits, 4 TB. 0100 44 bits, 16 TB. 0101 48 bits, 256 TB. All other values are reserved.

14.3.1.1.2.424 A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_63_32 Register (Offset = D3Ch) [reset = 0h]

Memory Model Feature Register 0 (high word)

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Table 14-8954. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D3Ch**

Figure 14-2969. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR0_EL1_63_32_31_0							
R/W							
0h							

Table 14-8956. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR0_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR0_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.425 A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_31_0 Register (Offset = D40h) [reset = 0h]

Processor Feature Register 1 (low word)

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Table 14-8957. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D40h**

Figure 14-2970. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-8959. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.426 A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_63_32 Register (Offset = D44h) [reset = 0h]

Processor Feature Register 1 (high word)

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Table 14-8960. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D44h**

Figure 14-2971. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64PFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-8962. A53SS_APBADDR_DBG_CPU1_ID_AA64PFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64PFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.427 A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_31_0 Register (Offset = D48h) [reset = 0h]

Auxiliary Feature Register 1 (low word)

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Table 14-8963. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D48h**

Figure 14-2972. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-8965. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.428 A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_63_32 Register (Offset = D4Ch) [reset = 0h]

Auxiliary Feature Register 1 (high word)

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Table 14-8966. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D4Ch**

Figure 14-2973. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64DFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-8968. A53SS_APBADDR_DBG_CPU1_ID_AA64DFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64DFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.429 A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_31_0 Register (Offset = D50h) [reset = 0h]

Instruction Set Attribute Register 1 (low word)

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Table 14-8969. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D50h**

Figure 14-2974. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-8971. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.430 A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_63_32 Register (Offset = D54h) [reset = 0h]

Instruction Set Attribute Register 1 (high word)

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Table 14-8972. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D54h**

Figure 14-2975. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64ISAR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-8974. A53SS_APBADDR_DBG_CPU1_ID_AA64ISAR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64ISAR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.431 A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_31_0 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_31_0 Register (Offset = D58h) [reset = 0h]

Memory Model Feature Register 1 (low word)

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Table 14-8975. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D58h**

Figure 14-2976. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_31_0 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR1_EL1_31_0_31_0							
R/W							
0h							

Table 14-8977. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_31_0_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.432 A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_63_32 Register

1 A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_63_32 Register (Offset = D5Ch) [reset = 0h]

Memory Model Feature Register 1 (high word)

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Table 14-8978. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0D5Ch**

Figure 14-2977. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_63_32 Name Register

31	30	29	28	27	26	25	24
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_ID_AA64MMFR1_EL1_63_32_31_0							
R/W							
0h							

Table 14-8980. A53SS_APBADDR_DBG_CPU1_ID_AA64MMFR1_EL1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_ID_AA64MMFR1_EL1_63_32_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.433 A53SS_APBADDR_DBG_CPU1_EDITCTRL Register

1 A53SS_APBADDR_DBG_CPU1_EDITCTRL Register (Offset = F00h) [reset = 0h]

External Debug Integration mode Control Register

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Table 14-8981. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0F00h**

Figure 14-2978. A53SS_APBADDR_DBG_CPU1_EDITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_EDITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-8983. A53SS_APBADDR_DBG_CPU1_EDITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_EDITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.434 A53SS_APBADDR_DBG_CPU1_DBGCLAIMSET_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGCLAIMSET_EL1 Register (Offset = FA0h) [reset = FFh]

Debug Claim Tag Set Register

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Table 14-8984. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FA0h**

Figure 14-2979. A53SS_APBADDR_DBG_CPU1_DBGCLAIMSET_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMSET_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
FFh							

Table 14-8986. A53SS_APBADDR_DBG_CPU1_DBGCLAIMSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMSET_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	FFh	Claim set bits. RAO.Writing a 1 to one of these bits sets the corresponding CLAIM bit to 1. This is an indirect write to the CLAIM bits.A single write operation can set multiple bits to 1. Writing 0 to one of these bits has no effect.

14.3.1.1.2.435 A53SS_APBADDR_DBG_CPU1_DBGCLAIMCLR_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGCLAIMCLR_EL1 Register (Offset = FA4h) [reset = 0h]

Debug Claim Tag Clear Register

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Table 14-8987. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FA4h**

Figure 14-2980. A53SS_APBADDR_DBG_CPU1_DBGCLAIMCLR_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGCLAIMCLR_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIM							
R/W							
0h							

Table 14-8989. A53SS_APBADDR_DBG_CPU1_DBGCLAIMCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGCLAIMCLR_EL1_31_8	R/W	0h	Reserved, RAZ/SBZ. Software can rely on these bits Reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.
7:0	CLAIM	R/W	0h	Claim clear bits. Reading this field returns the current value of the CLAIM bits.Writing a 1 to one of these bits clears the corresponding CLAIM bit to 0. This is an indirect write to the CLAIM bits.A single write operation can clear multiple bits to 0. Writing 0 to one of these bits has no effect.

14.3.1.1.2.436 A53SS_APBADDR_DBG_CPU1_EDDEVAFF0 Register

1 A53SS_APBADDR_DBG_CPU1_EDDEVAFF0 Register (Offset = FA8h) [reset = 80000001h]

External Debug Device Affinity Register 0

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Table 14-8990. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FA8h**

Figure 14-2981. A53SS_APBADDR_DBG_CPU1_EDDEVAFF0 Name Register

31	30	29	28	27	26	25	24
EDDEVAFF0							
R/W							
80000001h							
23	22	21	20	19	18	17	16
EDDEVAFF0							
R/W							
80000001h							
15	14	13	12	11	10	9	8
EDDEVAFF0							
R/W							
80000001h							
7	6	5	4	3	2	1	0
EDDEVAFF0							
R/W							
80000001h							

Table 14-8992. A53SS_APBADDR_DBG_CPU1_EDDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF0	R/W	80000001h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.437 A53SS_APBADDR_DBG_CPU1_EDDEVAFF1 Register

1 A53SS_APBADDR_DBG_CPU1_EDDEVAFF1 Register (Offset = FACh) [reset = 0h]

External Debug Device Affinity Register 1

Return to Summary Table

Table 14-8993. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FACh**

Figure 14-2982. A53SS_APBADDR_DBG_CPU1_EDDEVAFF1 Name Register

31	30	29	28	27	26	25	24
EDDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
EDDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
EDDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
EDDEVAFF1							
R/W							
0h							

Table 14-8995. A53SS_APBADDR_DBG_CPU1_EDDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EDDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.438 A53SS_APBADDR_DBG_CPU1_EDLAR Register

1 A53SS_APBADDR_DBG_CPU1_EDLAR Register (Offset = FB0h) [reset = 0h]

External Debug Lock Access Register

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Table 14-8996. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FB0h**

Figure 14-2983. A53SS_APBADDR_DBG_CPU1_EDLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-8998. A53SS_APBADDR_DBG_CPU1_EDLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.439 A53SS_APBADDR_DBG_CPU1_EDLSR Register

1 A53SS_APBADDR_DBG_CPU1_EDLSR Register (Offset = FB4h) [reset = 0h]

External Debug Lock Status Register

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Table 14-8999. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FB4h**

Figure 14-2984. A53SS_APBADDR_DBG_CPU1_EDLSR Name Register

31	30	29	28	27	26	25	24
RES0_EDLSR_31_3							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDLSR_31_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDLSR_31_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-9001. A53SS_APBADDR_DBG_CPU1_EDLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_EDLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.440 A53SS_APBADDR_DBG_CPU1_DBGAUTHSTATUS_EL1 Register

1 A53SS_APBADDR_DBG_CPU1_DBGAUTHSTATUS_EL1 Register (Offset = FB8h) [reset = AAh]

Debug Authentication Status register

Return to Summary Table

Table 14-9002. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FB8h**

Figure 14-2985. A53SS_APBADDR_DBG_CPU1_DBGAUTHSTATUS_EL1 Name Register

31	30	29	28	27	26	25	24
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_DBGAUTHSTATUS_EL1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R/W		R/W		R/W		R/W	
2h		2h		2h		2h	

Table 14-9004. A53SS_APBADDR_DBG_CPU1_DBGAUTHSTATUS_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_DBGAUTHSTATUS_EL1_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
5:4	SID	R/W	2h	Secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Non-secure. 10 Implemented and disabled. ExternalSecureInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalSecureInvasiveDebugEnabled[] == TRUE. Other values are reserved.

Table 14-9004. A53SS_APBADDR_DBG_CPU1_DBGAUTHSTATUS_EL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Non-secure non-invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalNoninvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalNoninvasiveDebugEnabled[] == TRUE. Other values are reserved.
1:0	NSID	R/W	2h	Non-secure invasive debug. Possible values of this field are: 00 Not implemented. EL3 is not implemented and the processor is Secure. 10 Implemented and disabled. ExternalInvasiveDebugEnabled[] == FALSE. 11 Implemented and enabled. ExternalInvasiveDebugEnabled[] == TRUE. Other values are reserved.

14.3.1.1.2.441 A53SS_APBADDR_DBG_CPU1_EDDEVARCH Register

1 A53SS_APBADDR_DBG_CPU1_EDDEVARCH Register (Offset = FBCh) [reset = 47706A15h]

External Debug Device Architecture Register

Return to Summary Table

Table 14-9005. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FBCh**

Figure 14-2986. A53SS_APBADDR_DBG_CPU1_EDDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6A15h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6A15h</td></tr>
</table>

Table 14-9007. A53SS_APBADDR_DBG_CPU1_EDDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For debug, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For debug, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	6A15h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For debug:Bits [15:12] are the architecture version, 0x6.Bits [11:0] are the architecture part number, 0xA15.This corresponds to debug architecture version v8-A.

14.3.1.1.2.442 A53SS_APBADDR_DBG_CPU1_EDDEVID2 Register

1 A53SS_APBADDR_DBG_CPU1_EDDEVID2 Register (Offset = FC0h) [reset = 0h]

External Debug Device ID Register 2

Return to Summary Table

Table 14-9008. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FC0h**

Figure 14-2987. A53SS_APBADDR_DBG_CPU1_EDDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID2_31_0							
R/W							
0h							

Table 14-9010. A53SS_APBADDR_DBG_CPU1_EDDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_EDDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.443 A53SS_APBADDR_DBG_CPU1_EDDEVID1 Register

1 A53SS_APBADDR_DBG_CPU1_EDDEVID1 Register (Offset = FC4h) [reset = 2h]

External Debug Device ID Register 1

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Table 14-9011. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FC4h**

Figure 14-2988. A53SS_APBADDR_DBG_CPU1_EDDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDDEVID1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID1_31_4				PCSROFFSET			
R/W				R/W			
0h				2h			

Table 14-9013. A53SS_APBADDR_DBG_CPU1_EDDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_EDDEVID1_31_4	R/W	0h	Reserved, RES0.
3:0	PCSROFFSET	R/W	2h	This field indicates the offset applied to PC samples returned by reads of EDPCSR. Permitted values of this field in v8-A are: 0000 EDPCSR not implemented. 0010 EDPCSR implemented, and samples have no offset applied and do not sample the instruction set state in AArch32 state.

14.3.1.1.2.444 A53SS_APBADDR_DBG_CPU1_EDDEVID Register

1 A53SS_APBADDR_DBG_CPU1_EDDEVID Register (Offset = FC8h) [reset = 3h]

External Debug Device ID Register 0

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Table 14-9014. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FC8h**

Figure 14-2989. A53SS_APBADDR_DBG_CPU1_EDDEVID Name Register

31	30	29	28	27	26	25	24
RES0_EDDEVID_31_28				AUXREGS			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RES0_EDDEVID_23_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDDEVID_23_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_EDDEVID_23_4				PCSAMPLE			
R/W				R/W			
0h				3h			

Table 14-9016. A53SS_APBADDR_DBG_CPU1_EDDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RES0_EDDEVID_31_28	R/W	0h	Reserved, RES0.
27:24	AUXREGS	R/W	0h	Indicates support for Auxiliary registers. Permitted values for this field are: 0000 None supported. 0001 Support for External Debug Auxiliary Control Register, EDACR. All other values are reserved.
23:4	RES0_EDDEVID_23_4	R/W	0h	Reserved, RES0.
3:0	PCSAMPLE	R/W	3h	Indicates the level of Sample-based profiling support using external debug registers 40 through 43. Permitted values of this field in v8-A are: 0000 Architecture-defined form of Sample-based profiling not implemented. 0010 EDPCSR and EDCIDSR are implemented [only permitted if EL3 and EL2 are not implemented]. 0011 EDPCSR, EDCIDSR, and EDVIDSR are implemented. All other values are reserved.

14.3.1.1.2.445 A53SS_APBADDR_DBG_CPU1_EDDEVTYPE Register

1 A53SS_APBADDR_DBG_CPU1_EDDEVTYPE Register (Offset = FCCh) [reset = 15h]

External Debug Device Type Register

Return to Summary Table

Table 14-9017. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FCCh**

Figure 14-2990. A53SS_APBADDR_DBG_CPU1_EDDEVTYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDDEVTYPE_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDDEVTYPE_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDDEVTYPE_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SUB</td><td colspan="4">MAJOR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">5h</td></tr>
</table>

Table 14-9019. A53SS_APBADDR_DBG_CPU1_EDDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	5h	Major type. Must read as 0x5 to indicate this is a debug logic component.

14.3.1.1.2.446 A53SS_APBADDR_DBG_CPU1_EDPIDR4 Register

1 A53SS_APBADDR_DBG_CPU1_EDPIDR4 Register (Offset = FD0h) [reset = 4h]

External Debug Peripheral Identification Register 4

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Table 14-9020. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FD0h**

Figure 14-2991. A53SS_APBADDR_DBG_CPU1_EDPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-9022. A53SS_APBADDR_DBG_CPU1_EDPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.447 A53SS_APBADDR_DBG_CPU1_EDPIDR0 Register

1 A53SS_APBADDR_DBG_CPU1_EDPIDR0 Register (Offset = FE0h) [reset = 3h]

External Debug Peripheral Identification Register 0

Return to Summary Table

Table 14-9023. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FE0h**

Figure 14-2992. A53SS_APBADDR_DBG_CPU1_EDPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R/W							
3h							

Table 14-9025. A53SS_APBADDR_DBG_CPU1_EDPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	3h	Part number, least significant byte.

14.3.1.1.2.448 A53SS_APBADDR_DBG_CPU1_EDPIDR1 Register

1 A53SS_APBADDR_DBG_CPU1_EDPIDR1 Register (Offset = FE4h) [reset = BDh]

External Debug Peripheral Identification Register 1

Return to Summary Table

Table 14-9026. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FE4h**

Figure 14-2993. A53SS_APBADDR_DBG_CPU1_EDPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				Dh			

Table 14-9028. A53SS_APBADDR_DBG_CPU1_EDPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	Dh	Part number, most significant nibble.

14.3.1.1.2.449 A53SS_APBADDR_DBG_CPU1_EDPIDR2 Register

1 A53SS_APBADDR_DBG_CPU1_EDPIDR2 Register (Offset = FE8h) [reset = 4Bh]

External Debug Peripheral Identification Register 2

Return to Summary Table

Table 14-9029. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FE8h**

Figure 14-2994. A53SS_APBADDR_DBG_CPU1_EDPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_EDPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_EDPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-9031. A53SS_APBADDR_DBG_CPU1_EDPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.450 A53SS_APBADDR_DBG_CPU1_EDPIDR3 Register

1 A53SS_APBADDR_DBG_CPU1_EDPIDR3 Register (Offset = FECh) [reset = 0h]

External Debug Peripheral Identification Register 3

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Table 14-9032. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FECh**

Figure 14-2995. A53SS_APBADDR_DBG_CPU1_EDPIDR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_EDPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_EDPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_EDPIDR3_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9034. A53SS_APBADDR_DBG_CPU1_EDPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using EDPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.451 A53SS_APBADDR_DBG_CPU1_EDCIDR0 Register

1 A53SS_APBADDR_DBG_CPU1_EDCIDR0 Register (Offset = FF0h) [reset = Dh]

External Debug Component Identification Register 0

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Table 14-9035. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FF0h**

Figure 14-2996. A53SS_APBADDR_DBG_CPU1_EDCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-9037. A53SS_APBADDR_DBG_CPU1_EDCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.452 A53SS_APBADDR_DBG_CPU1_EDCIDR1 Register

1 A53SS_APBADDR_DBG_CPU1_EDCIDR1 Register (Offset = FF4h) [reset = 90h]

External Debug Component Identification Register 1

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Table 14-9038. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FF4h**

Figure 14-2997. A53SS_APBADDR_DBG_CPU1_EDCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-9040. A53SS_APBADDR_DBG_CPU1_EDCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.453 A53SS_APBADDR_DBG_CPU1_EDCIDR2 Register

1 A53SS_APBADDR_DBG_CPU1_EDCIDR2 Register (Offset = FF8h) [reset = 5h]

External Debug Component Identification Register 2

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Table 14-9041. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FF8h**

Figure 14-2998. A53SS_APBADDR_DBG_CPU1_EDCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-9043. A53SS_APBADDR_DBG_CPU1_EDCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.454 A53SS_APBADDR_DBG_CPU1_EDCIDR3 Register

1 A53SS_APBADDR_DBG_CPU1_EDCIDR3 Register (Offset = FFCh) [reset = B1h]

External Debug Component Identification Register 3

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Table 14-9044. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3011 0FFCh**

Figure 14-2999. A53SS_APBADDR_DBG_CPU1_EDCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_EDCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_EDCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_EDCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-9046. A53SS_APBADDR_DBG_CPU1_EDCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_EDCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.455 A53SS_APBADDR_PMU_CPU1_PMEVCNTR0_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVCNTR0_EL0 Register (Offset = 0h) [reset = 0h]

Performance Monitors Event Count Register 0

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Table 14-9047. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0000h**

Figure 14-3000. A53SS_APBADDR_PMU_CPU1_PMEVCNTR0_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR0_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR0_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR0_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR0_EL0							
R/W							
0h							

Table 14-9049. A53SS_APBADDR_PMU_CPU1_PMEVCNTR0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR0_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.456 A53SS_APBADDR_PMU_CPU1_PMEVCNTR1_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVCNTR1_EL0 Register (Offset = 8h) [reset = 0h]

Performance Monitors Event Count Register 1

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Table 14-9050. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0008h**

Figure 14-3001. A53SS_APBADDR_PMU_CPU1_PMEVCNTR1_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR1_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR1_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR1_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR1_EL0							
R/W							
0h							

Table 14-9052. A53SS_APBADDR_PMU_CPU1_PMEVCNTR1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR1_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.457 A53SS_APBADDR_PMU_CPU1_PMEVCNTR2_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVCNTR2_EL0 Register (Offset = 10h) [reset = 0h]

Performance Monitors Event Count Register 2

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Table 14-9053. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0010h**

Figure 14-3002. A53SS_APBADDR_PMU_CPU1_PMEVCNTR2_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR2_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR2_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR2_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR2_EL0							
R/W							
0h							

Table 14-9055. A53SS_APBADDR_PMU_CPU1_PMEVCNTR2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR2_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.458 A53SS_APBADDR_PMU_CPU1_PMEVCNTR3_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVCNTR3_EL0 Register (Offset = 18h) [reset = 0h]

Performance Monitors Event Count Register 3

Return to Summary Table

Table 14-9056. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0018h**

Figure 14-3003. A53SS_APBADDR_PMU_CPU1_PMEVCNTR3_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR3_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR3_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR3_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR3_EL0							
R/W							
0h							

Table 14-9058. A53SS_APBADDR_PMU_CPU1_PMEVCNTR3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR3_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.459 A53SS_APBADDR_PMU_CPU1_PMEVCNTR4_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVCNTR4_EL0 Register (Offset = 20h) [reset = 0h]

Performance Monitors Event Count Register 4

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Table 14-9059. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0020h**

Figure 14-3004. A53SS_APBADDR_PMU_CPU1_PMEVCNTR4_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR4_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR4_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR4_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR4_EL0							
R/W							
0h							

Table 14-9061. A53SS_APBADDR_PMU_CPU1_PMEVCNTR4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR4_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.460 A53SS_APBADDR_PMU_CPU1_PMEVCNTR5_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVCNTR5_EL0 Register (Offset = 28h) [reset = 0h]

Performance Monitors Event Count Register 5

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Table 14-9062. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0028h**

Figure 14-3005. A53SS_APBADDR_PMU_CPU1_PMEVCNTR5_EL0 Name Register

31	30	29	28	27	26	25	24
PMEVCNTR5_EL0							
R/W							
0h							
23	22	21	20	19	18	17	16
PMEVCNTR5_EL0							
R/W							
0h							
15	14	13	12	11	10	9	8
PMEVCNTR5_EL0							
R/W							
0h							
7	6	5	4	3	2	1	0
PMEVCNTR5_EL0							
R/W							
0h							

Table 14-9064. A53SS_APBADDR_PMU_CPU1_PMEVCNTR5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMEVCNTR5_EL0	R/W	0h	Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

14.3.1.1.2.461 A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_31_0 Register

1 A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_31_0 Register (Offset = F8h) [reset = 0h]

Performance Monitors Cycle Counter (low word)

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Table 14-9065. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 00F8h**

Figure 14-3006. A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_31_0 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-9067. A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.462 A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_63_32 Register

1 A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_63_32 Register (Offset = FCh) [reset = 0h]

Performance Monitors Cycle Counter (high word)

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Table 14-9068. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 00FCh**

Figure 14-3007. A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_63_32 Name Register

31	30	29	28	27	26	25	24
CCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 14-9070. A53SS_APBADDR_PMU_CPU1_PMCCNTR_EL0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CCNT	R/W	0h	Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:Every processor clock cycle.Every 64th processor clock cycle.The cycle count can be reset to zero by Writing 1 to PMCR_EL0.C.

14.3.1.1.2.463 A53SS_APBADDR_PMU_CPU1_PMEVTYPER0_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVTYPER0_EL0 Register (Offset = 400h) [reset = 0h]

Performance Monitors Event Type Register 0

Return to Summary Table

Table 14-9071. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0400h**

Figure 14-3008. A53SS_APBADDR_PMU_CPU1_PMEVTYPER0_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER0_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER0_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER0_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-9073. A53SS_APBADDR_PMU_CPU1_PMEVTYPER0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-9073. A53SS_APBADDR_PMU_CPU1_PMEVTYPER0_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER0_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.464 A53SS_APBADDR_PMU_CPU1_PMEVTYPER1_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVTYPER1_EL0 Register (Offset = 404h) [reset = 0h]

Performance Monitors Event Type Register 1

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Table 14-9074. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0404h**

Figure 14-3009. A53SS_APBADDR_PMU_CPU1_PMEVTYPER1_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER1_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER1_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER1_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-9076. A53SS_APBADDR_PMU_CPU1_PMEVTYPER1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-9076. A53SS_APBADDR_PMU_CPU1_PMEVTYPER1_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER1_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.465 A53SS_APBADDR_PMU_CPU1_PMEVTYPER2_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVTYPER2_EL0 Register (Offset = 408h) [reset = 0h]

Performance Monitors Event Type Register 2

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Table 14-9077. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0408h**

Figure 14-3010. A53SS_APBADDR_PMU_CPU1_PMEVTYPER2_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER2_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER2_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER2_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-9079. A53SS_APBADDR_PMU_CPU1_PMEVTYPER2_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-9079. A53SS_APBADDR_PMU_CPU1_PMEVTYPER2_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER2_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.466 A53SS_APBADDR_PMU_CPU1_PMEVTYPER3_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVTYPER3_EL0 Register (Offset = 40Ch) [reset = 0h]

Performance Monitors Event Type Register 3

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Table 14-9080. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 040Ch**

Figure 14-3011. A53SS_APBADDR_PMU_CPU1_PMEVTYPER3_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER3_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER3_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER3_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-9082. A53SS_APBADDR_PMU_CPU1_PMEVTYPER3_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-9082. A53SS_APBADDR_PMU_CPU1_PMEVTYPER3_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER3_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.467 A53SS_APBADDR_PMU_CPU1_PMEVTYPER4_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVTYPER4_EL0 Register (Offset = 410h) [reset = 0h]

Performance Monitors Event Type Register 4

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Table 14-9083. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0410h**

Figure 14-3012. A53SS_APBADDR_PMU_CPU1_PMEVTYPER4_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER4_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMEVTYPER4_EL0_25_10							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMEVTYPER4_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
EVTCOUNT							
R/W							
0h							

Table 14-9085. A53SS_APBADDR_PMU_CPU1_PMEVTYPER4_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-9085. A53SS_APBADDR_PMU_CPU1_PMEVTYPER4_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER4_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.468 A53SS_APBADDR_PMU_CPU1_PMEVTYPER5_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMEVTYPER5_EL0 Register (Offset = 414h) [reset = 0h]

Performance Monitors Event Type Register 5

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Table 14-9086. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0414h**

Figure 14-3013. A53SS_APBADDR_PMU_CPU1_PMEVTYPER5_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMEVTYPER5_EL0_25_10	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMEVTYPER5_EL0_25_10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMEVTYPER5_EL0_25_10						EVTCOUNT	
R/W						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVTCOUNT							
R/W							
0h							

Table 14-9088. A53SS_APBADDR_PMU_CPU1_PMEVTYPER5_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count events in EL1. 1 Do not count events in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count events in EL0. 1 Do not count events in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Non-secure EL1 are counted.Otherwise, events in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, events in Non-secure EL0 are counted.Otherwise, events in Non-secure EL0 are not counted.

Table 14-9088. A53SS_APBADDR_PMU_CPU1_PMEVTYPER5_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count events in EL2. 1 Count events in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, events in Secure EL3 are counted.Otherwise, events in Secure EL3 are not counted.
25:10	RES0_PMEVTYPER5_EL0_25_10	R/W	0h	Reserved, RES0.
9:0	EVTCOUNT	R/W	0h	Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.Software must program this field with an event defined by the processor or a common event defined by the architecture.If evtCount is programmed to an event that is reserved or not implemented, the behavior depends on the event type.For common architectural and microarchitectural events:No events are counted.The value read back on evtCount is the value written.For IMPLEMENTATION DEFINED events:It is UNPREDICTABLE what event, if any, is counted. UNPREDICTABLE in this case means the event must not expose privileged information.The value read back on evtCount is an UNKNOWN value with the same effect.ARM recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

14.3.1.1.2.469 A53SS_APBADDR_PMU_CPU1_PMCCFILTR_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMCCFILTR_EL0 Register (Offset = 47Ch) [reset = 0h]

Performance Monitors Cycle Counter Filter Register

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Table 14-9089. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 047Ch**

Figure 14-3014. A53SS_APBADDR_PMU_CPU1_PMCCFILTR_EL0 Name Register

31	30	29	28	27	26	25	24
P	U	NSK	NSU	NSH	M	RES0_PMCCFILTR_EL0_25_0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMCCFILTR_EL0_25_0							
R/W							
0h							

Table 14-9091. A53SS_APBADDR_PMU_CPU1_PMCCFILTR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P	R/W	0h	EL1 modes filtering bit. Controls counting in EL1. If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the NSK bit. The possible values of this bit are: 0 Count cycles in EL1. 1 Do not count cycles in EL1.
30	U	R/W	0h	EL0 filtering bit. Controls counting in EL0. If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the NSU bit. The possible values of this bit are: 0 Count cycles in EL0. 1 Do not count cycles in EL0.
29	NSK	R/W	0h	Non-secure kernel modes filtering bit. Controls counting in Non-secure EL1. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Non-secure EL1 are counted.Otherwise, cycles in Non-secure EL1 are not counted.
28	NSU	R/W	0h	Non-secure user modes filtering bit. Controls counting in Non-secure EL0. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of U, cycles in Non-secure EL0 are counted.Otherwise, cycles in Non-secure EL0 are not counted.

Table 14-9091. A53SS_APBADDR_PMU_CPU1_PMCCFILTR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NSH	R/W	0h	Non-secure Hyp modes filtering bit. Controls counting in Non-secure EL2. If EL2 is not implemented, this bit is RES0. 0 Do not count cycles in EL2. 1 Count cycles in EL2.
26	M	R/W	0h	Secure EL3 filtering bit. Most applications can ignore this bit and set the value to zero. If EL3 is not implemented, this bit is RES0.If the value of this bit is equal to the value of P, cycles in Secure EL3 are counted.Otherwise, cycles in Secure EL3 are not counted.
25:0	RES0_PMCCFILTR_EL0_25_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.470 A53SS_APBADDR_PMU_CPU1_PMCNTENSET_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMCNTENSET_EL0 Register (Offset = C00h) [reset = 0h]

Performance Monitors Count Enable Set Register

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Table 14-9092. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C00h**

Figure 14-3015. A53SS_APBADDR_PMU_CPU1_PMCNTENSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-9094. A53SS_APBADDR_PMU_CPU1_PMCNTENSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 enable bit. Enables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, enables the cycle counter.
30:0	P_X	R/W	0h	Event counter enable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> event counter is enabled. When written, enables PMEVCNTR<x>.

14.3.1.1.2.471 A53SS_APBADDR_PMU_CPU1_PMCNTENCLR_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMCNTENCLR_EL0 Register (Offset = C20h) [reset = 0h]

Performance Monitors Count Enable Clear Register

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Table 14-9095. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C20h**

Figure 14-3016. A53SS_APBADDR_PMU_CPU1_PMCNTENCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-9097. A53SS_APBADDR_PMU_CPU1_PMCNTENCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 disable bit. Disables the cycle counter register. Possible values are: 0 When read, means the cycle counter is disabled. When written, has no effect. 1 When read, means the cycle counter is enabled. When written, disables the cycle counter.
30:0	P_X	R/W	0h	Event counter disable bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> is disabled. When written, has no effect. 1 When read, means that PMEVCNTR<x> is enabled. When written, disables PMEVCNTR<x>.

14.3.1.1.2.472 A53SS_APBADDR_PMU_CPU1_PMINTENSET_EL1 Register

1 A53SS_APBADDR_PMU_CPU1_PMINTENSET_EL1 Register (Offset = C40h) [reset = 0h]

Performance Monitors Interrupt Enable Set Register

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Table 14-9098. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C40h**

Figure 14-3017. A53SS_APBADDR_PMU_CPU1_PMINTENSET_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
P_X							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P_X							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P_X							
R/W							
0h							

Table 14-9100. A53SS_APBADDR_PMU_CPU1_PMINTENSET_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request enable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, enables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request enable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, enables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.473 A53SS_APBADDR_PMU_CPU1_PMINTENCLR_EL1 Register

1 A53SS_APBADDR_PMU_CPU1_PMINTENCLR_EL1 Register (Offset = C60h) [reset = 0h]

Performance Monitors Interrupt Enable Clear Register

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Table 14-9101. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C60h**

Figure 14-3018. A53SS_APBADDR_PMU_CPU1_PMINTENCLR_EL1 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-9103. A53SS_APBADDR_PMU_CPU1_PMINTENCLR_EL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow interrupt request disable bit. Possible values are: 0 When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect. 1 When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.
30:0	P_X	R/W	0h	Event counter overflow interrupt request disable bit for PMEVCNTR<x>_EL0.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is disabled. When written, has no effect. 1 When read, means that the PMEVCNTR<x>_EL0 event counter interrupt request is enabled. When written, disables the PMEVCNTR<x>_EL0 interrupt request.

14.3.1.1.2.474 A53SS_APBADDR_PMU_CPU1_PMOVSCLR_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMOVSCLR_EL0 Register (Offset = C80h) [reset = 0h]

Performance Monitors Overflow Flag Status Clear Register

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Table 14-9104. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0C80h**

Figure 14-3019. A53SS_APBADDR_PMU_CPU1_PMOVSCLR_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-9106. A53SS_APBADDR_PMU_CPU1_PMOVSCLR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, clears the overflow bit to 0. PMCR_EL0.LC is used to control from which bit of PMCCNTR_EL0 [bit 31 or bit 63] an overflow is detected.
30:0	P_X	R/W	0h	Event counter overflow clear bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values of each bit are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, clears the PMEVCNTR<x> overflow bit to 0.

14.3.1.1.2.475 A53SS_APBADDR_PMU_CPU1_PMSWINC_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMSWINC_EL0 Register (Offset = CA0h) [reset = 0h]

Performance Monitors Software Increment Register

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Table 14-9107. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0CA0h**

Figure 14-3020. A53SS_APBADDR_PMU_CPU1_PMSWINC_EL0 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMSWINC_EL0_31_6							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMSWINC_EL0_31_6		P_X					
R/W		R/W					
0h		0h					

Table 14-9109. A53SS_APBADDR_PMU_CPU1_PMSWINC_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_PMSWINC_EL0_31_6	R/W	0h	Reserved RES0
5:0	P_X	R/W	0h	Event counter software increment bit for PMEVCNTR<x>

14.3.1.1.2.476 A53SS_APBADDR_PMU_CPU1_PMOVSSET_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMOVSSET_EL0 Register (Offset = CC0h) [reset = 0h]

Performance Monitors Overflow Flag Status Set Register

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Table 14-9110. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0CC0h**

Figure 14-3021. A53SS_APBADDR_PMU_CPU1_PMOVSSET_EL0 Name Register

31	30	29	28	27	26	25	24
C	P_X						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
P_X							
R/W							
0h							
15	14	13	12	11	10	9	8
P_X							
R/W							
0h							
7	6	5	4	3	2	1	0
P_X							
R/W							
0h							

Table 14-9112. A53SS_APBADDR_PMU_CPU1_PMOVSSET_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	C	R/W	0h	PMCCNTR_EL0 overflow bit. Possible values are: 0 When read, means the cycle counter has not overflowed. When written, has no effect. 1 When read, means the cycle counter has overflowed. When written, sets the overflow bit to 1.
30:0	P_X	R/W	0h	Event counter overflow set bit for PMEVCNTR<x>.N is the value in PMCR_EL0.N. Bits [30:N] are RAZ/WI.Possible values are: 0 When read, means that PMEVCNTR<x> has not overflowed. When written, has no effect. 1 When read, means that PMEVCNTR<x> has overflowed. When written, sets the PMEVCNTR<x> overflow bit to 1.

14.3.1.1.2.477 A53SS_APBADDR_PMU_CPU1_PMCFGR Register

1 A53SS_APBADDR_PMU_CPU1_PMCFGR Register (Offset = E00h) [reset = 1FF06h]

Performance Monitors Configuration Register

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Table 14-9113. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0E00h**

Figure 14-3022. A53SS_APBADDR_PMU_CPU1_PMCFGR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_PMCFGR_31_20</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RES0_PMCFGR_31_20</td><td>UEN</td><td>WT</td><td>NA</td><td>EX</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CCD</td><td>CC</td><td colspan="6">SIZE</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="6">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td colspan="6">3Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">6h</td></tr>
</table>

Table 14-9115. A53SS_APBADDR_PMU_CPU1_PMCFGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES0_PMCFGR_31_20	R/W	0h	Reserved, RES0.
19	UEN	R/W	0h	User-mode Enable Register supported. PMUSERENR_EL0 is not visible in the external debug interface, so this bit is RES0.
18	WT	R/W	0h	This feature is not supported, so this bit is RES0.
17	NA	R/W	0h	This feature is not supported, so this bit is RES0.
16	EX	R/W	1h	Export supported. Value is IMPLEMENTATION DEFINED. 0 PMCR_EL0.X is RES0. 1 PMCR_EL0.X is read/write.
15	CCD	R/W	1h	Cycle counter has prescale. This is RES1 if AArch32 is supported at any EL, and RES0 otherwise. 0 PMCR_EL0.D is RES0. 1 PMCR_EL0.D is read/write.
14	CC	R/W	1h	Dedicated cycle counter [counter 31] supported. This bit is RES1.
13:8	SIZE	R/W	3Fh	Size of counters. This field determines the spacing of counters in the memory-map.In v8-A the counters are at doubleword-aligned addresses, and the largest counter is 64-bits, so this field is 0b111111.

Table 14-9115. A53SS_APBADDR_PMU_CPU1_PMCFGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	N	R/W	6h	Number of counters implemented in addition to the cycle counter, PMCCNTR_EL0. The maximum number of event counters is 31, so bits[7:5] are always RES0. 00000000 Only PMCCNTR_EL0 implemented. 00000001 PMCCNTR_EL0 plus one event counter implemented. and so on up to 0b00011111, which indicates PMCCNTR_EL0 and 31 event counters implemented.

14.3.1.1.2.478 A53SS_APBADDR_PMU_CPU1_PMCR_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMCR_EL0 Register (Offset = E04h) [reset = 0h]

Performance Monitors Control Register

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Table 14-9116. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0E04h**

Figure 14-3023. A53SS_APBADDR_PMU_CPU1_PMCR_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCR_EL0_31_11							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCR_EL0_31_11							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCR_EL0_31_11					RES0_PMCR_EL0_10_7		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_PMCR_EL0_10_7	LC	DP	X	D	C	P	E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9118. A53SS_APBADDR_PMU_CPU1_PMCR_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RES0_PMCR_EL0_31_11	R/W	0h	Reserved, RAZ/WI.
10:7	RES0_PMCR_EL0_10_7	R/W	0h	Reserved, RES0.
6	LC	R/W	0h	Long cycle counter enable. Determines which PMCCNTR_EL0 bit generates an overflow recorded by PMOVSR[31]. 0 Cycle counter overflow on increment that changes PMCCNTR_EL0[31] from 1 to 0. 1 Cycle counter overflow on increment that changes PMCCNTR_EL0[63] from 1 to 0. ARM deprecates use of PMCR_EL0.LC = 0.
5	DP	R/W	0h	Disable cycle counter when event counting is prohibited. The possible values of this bit are: 0 PMCCNTR_EL0, if enabled, counts when event counting is prohibited. 1 PMCCNTR_EL0 does not count when event counting is prohibited. Event counting is prohibited when ProfilingProhibited[IsSecure[],PSTATE.EL] == TRUE.This bit is RW.

Table 14-9118. A53SS_APBADDR_PMU_CPU1_PMCR_EL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	X	R/W	0h	Enable export of events in an IMPLEMENTATION DEFINED event stream. The possible values of this bit are: 0 Do not export events. 1 Export events where not prohibited. This bit is used to permit events to be exported to another debug device, such as an OPTIONAL trace extension, over an event bus. If the implementation does not include such an event bus, this bit is RAZ/WI.This bit does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface [CTI] that can be implemented as signals exported from the processor.If the implementation does not include an exported event stream, this bit is RAZ/WI. Otherwise this bit is RW.
3	D	R/W	0h	Clock divider. The possible values of this bit are: 0 When enabled, PMCCNTR_EL0 counts every clock cycle. 1 When enabled, PMCCNTR_EL0 counts once every 64 clock cycles. This bit is RW.If PMCR_EL0.LC == 1, this bit is ignored and the cycle counter counts every clock cycle.ARM deprecates use of PMCR.D = 1.
2	C	R/W	0h	Cycle counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset PMCCNTR_EL0 to zero. This bit is always RAZ.Resetting PMCCNTR_EL0 does not clear the PMCCNTR_EL0 overflow bit to 0.
1	P	R/W	0h	Event counter reset. This bit is WO. The effects of Writing to this bit are: 0 No action. 1 Reset all event counters, not including PMCCNTR_EL0, to zero. This bit is always RAZ.Resetting the event counters does not clear any overflow bits to 0.
0	E	R/W	0h	Enable. The possible values of this bit are: 0 All counters, including PMCCNTR_EL0, are disabled. 1 All counters are enabled by PMCNTENSET_EL0. This bit is RW.

14.3.1.1.2.479 A53SS_APBADDR_PMU_CPU1_PMCEID0_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMCEID0_EL0 Register (Offset = E20h) [reset = 67FFBFFFh]

Performance Monitors Common Event Identification Register 0

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Table 14-9119. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0E20h**

Figure 14-3024. A53SS_APBADDR_PMU_CPU1_PMCEID0_EL0 Name Register

31	30	29	28	27	26	25	24
CE_31_0							
R/W							
67FFBFFFh							
23	22	21	20	19	18	17	16
CE_31_0							
R/W							
67FFBFFFh							
15	14	13	12	11	10	9	8
CE_31_0							
R/W							
67FFBFFFh							
7	6	5	4	3	2	1	0
CE_31_0							
R/W							
67FFBFFFh							

Table 14-9121. A53SS_APBADDR_PMU_CPU1_PMCEID0_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CE_31_0	R/W	67FFBFFFh	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For each bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic310x01FL1D_CACHE_ALLOCATE300x01ECHAIN290x01DBUS_CYCLES280x01CTTBR_WRITE_RETIRED270x01BINST_SPEC260x01AMEMORY_ERROR250x019BUS_ACCESS240x018L2D_CACHE_WB230x017L2D_CACHE_REFILL220x016L2D_CACHE210x015L1D_CACHE_WB200x014L1I_CACHE190x013MEM_ACCESS180x012BR_PRED170x011CPU_CYCLES160x010BR_MIS_PRED150x00FUNALIGNED_LDST_RETIRED140x00EBR_RETURN_RETIRED130x00DBR_IMMED_RETIRED120x00CPC_WRITE_RETIRED110x00BCID_WRITE_RETIRED100x00AEXC_RETURN90x009EXC_TAKEN80x008INST_RETIRED70x007ST_RETIRED60x006LD_RETIRED50x005L1D_TLB_REFILL40x004L1D_CACHE30x003L1D_CACHE_REFILL20x002L1I_TLB_REFILL10x001L1I_CACHE_REFILL00x000SW_INCR

14.3.1.1.2.480 A53SS_APBADDR_PMU_CPU1_PMCEID1_EL0 Register

1 A53SS_APBADDR_PMU_CPU1_PMCEID1_EL0 Register (Offset = E24h) [reset = 0h]

Performance Monitors Common Event Identification Register 1

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Table 14-9122. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0E24h**

Figure 14-3025. A53SS_APBADDR_PMU_CPU1_PMCEID1_EL0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCEID1_EL0_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMCEID1_EL0_31_1							CE_32
R/W							R/W
0h							0h

Table 14-9124. A53SS_APBADDR_PMU_CPU1_PMCEID1_EL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMCEID1_EL0_31_1	R/W	0h	Reserved, RES0.
0	CE_32	R/W	0h	Common architectural and microarchitectural feature events that can be counted by the PMU event counters.For the bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.BitEvent numberEvent mnemonic00x020L2D_CACHE_ALLOCATE

14.3.1.1.2.481 A53SS_APBADDR_PMU_CPU1_PMITCTRL Register

1 A53SS_APBADDR_PMU_CPU1_PMITCTRL Register (Offset = F00h) [reset = 0h]

Performance Monitors Integration mode Control Register

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Table 14-9125. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0F00h**

Figure 14-3026. A53SS_APBADDR_PMU_CPU1_PMITCTRL Name Register

31	30	29	28	27	26	25	24
RES0_PMITCTRL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMITCTRL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMITCTRL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_PMITCTRL_31_1							IME
R/W							R/W
0h							0h

Table 14-9127. A53SS_APBADDR_PMU_CPU1_PMITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_PMITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.482 A53SS_APBADDR_PMU_CPU1_PMDEVAFF0 Register

1 A53SS_APBADDR_PMU_CPU1_PMDEVAFF0 Register (Offset = FA8h) [reset = 80000001h]

Performance Monitors Device Affinity Register 0

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Table 14-9128. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FA8h**

Figure 14-3027. A53SS_APBADDR_PMU_CPU1_PMDEVAFF0 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF0							
R/W							
80000001h							
23	22	21	20	19	18	17	16
PMDEVAFF0							
R/W							
80000001h							
15	14	13	12	11	10	9	8
PMDEVAFF0							
R/W							
80000001h							
7	6	5	4	3	2	1	0
PMDEVAFF0							
R/W							
80000001h							

Table 14-9130. A53SS_APBADDR_PMU_CPU1_PMDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF0	R/W	80000001h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.483 A53SS_APBADDR_PMU_CPU1_PMDEVAFF1 Register

1 A53SS_APBADDR_PMU_CPU1_PMDEVAFF1 Register (Offset = FACh) [reset = 0h]

Performance Monitors Device Affinity Register 1

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Table 14-9131. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FACh**

Figure 14-3028. A53SS_APBADDR_PMU_CPU1_PMDEVAFF1 Name Register

31	30	29	28	27	26	25	24
PMDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
PMDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
PMDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
PMDEVAFF1							
R/W							
0h							

Table 14-9133. A53SS_APBADDR_PMU_CPU1_PMDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PMDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.484 A53SS_APBADDR_PMU_CPU1_PMLAR Register

1 A53SS_APBADDR_PMU_CPU1_PMLAR Register (Offset = FB0h) [reset = 0h]

Performance Monitors Lock Access Register

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Table 14-9134. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FB0h**

Figure 14-3029. A53SS_APBADDR_PMU_CPU1_PMLAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-9136. A53SS_APBADDR_PMU_CPU1_PMLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.485 A53SS_APBADDR_PMU_CPU1_PMLSR Register

1 A53SS_APBADDR_PMU_CPU1_PMLSR Register (Offset = FB4h) [reset = 3h]

Performance Monitors Lock Status Register

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Table 14-9137. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FB4h**

Figure 14-3030. A53SS_APBADDR_PMU_CPU1_PMLSR Name Register

31	30	29	28	27	26	25	24
RES0_PMLSR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMLSR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMLSR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_PMLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	1h	1h

Table 14-9139. A53SS_APBADDR_PMU_CPU1_PMLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_PMLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	1h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	1h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.486 A53SS_APBADDR_PMU_CPU1_PMAUTHSTATUS Register

1 A53SS_APBADDR_PMU_CPU1_PMAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Performance Monitors Authentication Status Register

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Table 14-9140. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FB8h**

Figure 14-3031. A53SS_APBADDR_PMU_CPU1_PMAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMAUTHSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SNID		RES0_PMAUTHSTATUS_5_4		NSNID		RES0_PMAUTHSTATUS_1_0	
R/W		R/W		R/W		R/W	
2h		0h		2h		0h	

Table 14-9142. A53SS_APBADDR_PMU_CPU1_PMAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.SNID.
5:4	RES0_PMAUTHSTATUS_5_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	Holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	RES0_PMAUTHSTATUS_1_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.487 A53SS_APBADDR_PMU_CPU1_PMDEVARCH Register

1 A53SS_APBADDR_PMU_CPU1_PMDEVARCH Register (Offset = FBCh) [reset = 47702A16h]

Performance Monitors Device Architecture Register

Return to Summary Table

Table 14-9143. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FBCh**

Figure 14-3032. A53SS_APBADDR_PMU_CPU1_PMDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	22	21	20	19	18	17	16
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	14	13	12	11	10	9	8
ARCHID							
R/W							
2A16h							
7	6	5	4	3	2	1	0
ARCHID							
R/W							
2A16h							

Table 14-9145. A53SS_APBADDR_PMU_CPU1_PMDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For Performance Monitors, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For Performance Monitors, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	2A16h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For Performance Monitors:Bits [15:12] are the architecture version, 0x2.Bits [11:0] are the architecture part number, 0xA16.This corresponds to Performance Monitors architecture version PMUv3.

14.3.1.1.2.488 A53SS_APBADDR_PMU_CPU1_PMDEVTYPE Register

1 A53SS_APBADDR_PMU_CPU1_PMDEVTYPE Register (Offset = FCCh) [reset = 16h]

Performance Monitors Device Type Register

Return to Summary Table

Table 14-9146. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FCCh**

Figure 14-3033. A53SS_APBADDR_PMU_CPU1_PMDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_PMDEVTYPE_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMDEVTYPE_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMDEVTYPE_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAJOR			
R/W				R/W			
1h				6h			

Table 14-9148. A53SS_APBADDR_PMU_CPU1_PMDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	6h	Major type. Must read as 0x6 to indicate this is a performance monitor component.

14.3.1.1.2.489 A53SS_APBADDR_PMU_CPU1_PMPIDR4 Register

1 A53SS_APBADDR_PMU_CPU1_PMPIDR4 Register (Offset = FD0h) [reset = 4h]

Performance Monitors Peripheral Identification Register 4

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Table 14-9149. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FD0h**

Figure 14-3034. A53SS_APBADDR_PMU_CPU1_PMPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-9151. A53SS_APBADDR_PMU_CPU1_PMPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.490 A53SS_APBADDR_PMU_CPU1_PMPIDR5 Register

1 A53SS_APBADDR_PMU_CPU1_PMPIDR5 Register (Offset = FD4h) [reset = 0h]

Performance Monitors Peripheral Identification Register 5

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Table 14-9152. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FD4h**

Figure 14-3035. A53SS_APBADDR_PMU_CPU1_PMPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR5_31_0							
R/W							
0h							

Table 14-9154. A53SS_APBADDR_PMU_CPU1_PMPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.491 A53SS_APBADDR_PMU_CPU1_PMPIDR6 Register

1 A53SS_APBADDR_PMU_CPU1_PMPIDR6 Register (Offset = FD8h) [reset = 0h]

Performance Monitors Peripheral Identification Register 6

Return to Summary Table

Table 14-9155. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FD8h**

Figure 14-3036. A53SS_APBADDR_PMU_CPU1_PMPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR6_31_0							
R/W							
0h							

Table 14-9157. A53SS_APBADDR_PMU_CPU1_PMPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.492 A53SS_APBADDR_PMU_CPU1_PMPIDR7 Register

1 A53SS_APBADDR_PMU_CPU1_PMPIDR7 Register (Offset = FDCh) [reset = 0h]

Performance Monitors Peripheral Identification Register 7

Return to Summary Table

Table 14-9158. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FDCh**

Figure 14-3037. A53SS_APBADDR_PMU_CPU1_PMPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_PMPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_PMPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_PMPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_PMPIDR7_31_0							
R/W							
0h							

Table 14-9160. A53SS_APBADDR_PMU_CPU1_PMPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_PMPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.493 A53SS_APBADDR_PMU_CPU1_PMPIDR0 Register

1 A53SS_APBADDR_PMU_CPU1_PMPIDR0 Register (Offset = FE0h) [reset = D3h]

Performance Monitors Peripheral Identification Register 0

Return to Summary Table

Table 14-9161. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FE0h**

Figure 14-3038. A53SS_APBADDR_PMU_CPU1_PMPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR0_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR0_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR0_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R/W							
D3h							

Table 14-9163. A53SS_APBADDR_PMU_CPU1_PMPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	D3h	Part number, least significant byte.

14.3.1.1.2.494 A53SS_APBADDR_PMU_CPU1_PMPIDR1 Register

1 A53SS_APBADDR_PMU_CPU1_PMPIDR1 Register (Offset = FE4h) [reset = B9h]

Performance Monitors Peripheral Identification Register 1

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Table 14-9164. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FE4h**

Figure 14-3039. A53SS_APBADDR_PMU_CPU1_PMPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR1_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMPIDR1_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMPIDR1_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-9166. A53SS_APBADDR_PMU_CPU1_PMPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.495 A53SS_APBADDR_PMU_CPU1_PMPIDR2 Register

1 A53SS_APBADDR_PMU_CPU1_PMPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Performance Monitors Peripheral Identification Register 2

Return to Summary Table

Table 14-9167. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FE8h**

Figure 14-3040. A53SS_APBADDR_PMU_CPU1_PMPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-9169. A53SS_APBADDR_PMU_CPU1_PMPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.496 A53SS_APBADDR_PMU_CPU1_PMPIDR3 Register

1 A53SS_APBADDR_PMU_CPU1_PMPIDR3 Register (Offset = FECh) [reset = 0h]

Performance Monitors Peripheral Identification Register 3

Return to Summary Table

Table 14-9170. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FECh**

Figure 14-3041. A53SS_APBADDR_PMU_CPU1_PMPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMPIDR3_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMPIDR3_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMPIDR3_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-9172. A53SS_APBADDR_PMU_CPU1_PMPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using PMPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.497 A53SS_APBADDR_PMU_CPU1_PMCIDR0 Register

1 A53SS_APBADDR_PMU_CPU1_PMCIDR0 Register (Offset = FF0h) [reset = Dh]

Performance Monitors Component Identification Register 0

Return to Summary Table

Table 14-9173. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FF0h**

Figure 14-3042. A53SS_APBADDR_PMU_CPU1_PMCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-9175. A53SS_APBADDR_PMU_CPU1_PMCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.498 A53SS_APBADDR_PMU_CPU1_PMCIDR1 Register

1 A53SS_APBADDR_PMU_CPU1_PMCIDR1 Register (Offset = FF4h) [reset = 90h]

Performance Monitors Component Identification Register 1

Return to Summary Table

Table 14-9176. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FF4h**

Figure 14-3043. A53SS_APBADDR_PMU_CPU1_PMCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_PMCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_PMCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-9178. A53SS_APBADDR_PMU_CPU1_PMCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.499 A53SS_APBADDR_PMU_CPU1_PMCIDR2 Register

1 A53SS_APBADDR_PMU_CPU1_PMCIDR2 Register (Offset = FF8h) [reset = 5h]

Performance Monitors Component Identification Register 2

Return to Summary Table

Table 14-9179. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FF8h**

Figure 14-3044. A53SS_APBADDR_PMU_CPU1_PMCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-9181. A53SS_APBADDR_PMU_CPU1_PMCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.500 A53SS_APBADDR_PMU_CPU1_PMCIDR3 Register

1 A53SS_APBADDR_PMU_CPU1_PMCIDR3 Register (Offset = FFCh) [reset = B1h]

Performance Monitors Component Identification Register 3

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Table 14-9182. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3012 0FFCh**

Figure 14-3045. A53SS_APBADDR_PMU_CPU1_PMCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_PMCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_PMCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_PMCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-9184. A53SS_APBADDR_PMU_CPU1_PMCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_PMCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.501 A53SS_APBADDR_ETM_CPU1_TRCPRGCTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCPRGCTLR Register (Offset = 4h) [reset = 0h]

Programming Control Register

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Table 14-9185. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0004h**

Figure 14-3046. A53SS_APBADDR_ETM_CPU1_TRCPRGCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPRGCTLR_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPRGCTLR_31_1							EN
R/W							R/W
0h							0h

Table 14-9187. A53SS_APBADDR_ETM_CPU1_TRCPRGCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCPRGCTLR_31_1	R/W	0h	Reserved, RES0.
0	EN	R/W	0h	Trace unit enable bit. Possible values are: 0 The trace unit is disabled. All trace resources are inactive and no trace is generated. 1 The trace unit is enabled.

14.3.1.1.2.502 A53SS_APBADDR_ETM_CPU1_TRCSTATR Register

1 A53SS_APBADDR_ETM_CPU1_TRCSTATR Register (Offset = Ch) [reset = 0h]

Status Register

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Table 14-9188. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 000Ch**

Figure 14-3047. A53SS_APBADDR_ETM_CPU1_TRCSTATR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSTATR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSTATR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSTATR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSTATR_31_2						PMSTABLE	IDLE
R/W						R/W	R/W
0h						0h	0h

Table 14-9190. A53SS_APBADDR_ETM_CPU1_TRCSTATR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSTATR_31_2	R/W	0h	Reserved, RES0.
1	PMSTABLE	R/W	0h	Programmer's model stable bit: 0 The programmer's model is not stable. 1 The programmer's model is stable. When polled, the trace unit trace registers return stable data. The programmer's model is stable when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.Reads from trace unit registers return stable data.
0	IDLE	R/W	0h	Idle status bit: 0 The trace unit is not idle. 1 The trace unit is idle. The trace unit is idle when all of the following are true:TRCPRGCTLR.EN==0 or the OS Lock is locked.The trace unit is drained of any trace.With the exception of the programming interfaces, all external interfaces on the trace unit are quiescent.

14.3.1.1.2.503 A53SS_APBADDR_ETM_CPU1_TRCCONFIGR Register

1 A53SS_APBADDR_ETM_CPU1_TRCCONFIGR Register (Offset = 10h) [reset = 1h]

Trace Configuration Register

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Table 14-9191. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0010h**

Figure 14-3048. A53SS_APBADDR_ETM_CPU1_TRCCONFIGR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCONFIGR_31_18</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RES0_TRCCONFIGR_31_18</td><td>DV</td><td>DA</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RES0_TRCCONFIGR_15_15</td><td colspan="2">QE</td><td>RS</td><td>TS</td><td colspan="3">COND</td></tr>
<tr><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>VMID</td><td>CID</td><td>RES0_TRCCONFIGR_5_5</td><td>CCI</td><td>BB</td><td colspan="2">INSTP0</td><td>RES1_TRCCONFIGR_0_0</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>1h</td></tr>
</table>

Table 14-9193. A53SS_APBADDR_ETM_CPU1_TRCCONFIGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCONFIGR_31_18	R/W	0h	Reserved, RES0.
17	DV	R/W	0h	Data value tracing bit: 0 Data value tracing is disabled. 1 Data value tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
16	DA	R/W	0h	Data address tracing bit: 0 Data address tracing is disabled. 1 Data address tracing is enabled when INSTP0 is not 0b00. TRCIDR0.TRCDATA indicates whether this bit is supported. If it is not supported then this bit is RES0.
15	RES0_TRCCONFIGR_15_15	R/W	0h	Reserved, RES0.

Table 14-9193. A53SS_APBADDR_ETM_CPU1_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	QE	R/W	0h	Q element enable field: 00 Q elements are disabled. 01 Q elements with instruction counts are enabled. Q elements without instruction counts are disabled. 11 Q elements with and without instruction counts are enabled. The value 0b10 is reserved.TRCIDR0.QSUPP indicates which values of this field are implemented.TRCCONFIGR.QE must be set to 0b00 if any of the following are true:TRCCONFIGR.INSTP0 is not 0b00.TRCCONFIGR.COND is not 0b000.TRCCONFIGR.BB is not 0.
12	RS	R/W	0h	Return stack enable bit. 0 Return stack is disabled. 1 Return stack is enabled. TRCIDR0.RETSTACK indicates whether this bit is supported. If it is not supported then this bit is RES0.
11	TS	R/W	0h	Global timestamp tracing bit: 0 Global timestamp tracing is disabled. 1 Global timestamp tracing is enabled. TRCTSCTLR controls the insertion of timestamps in the trace. TRCIDR0.TSSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
10:8	COND	R/W	0h	Conditional instruction tracing bit. The permitted values are: 000 Conditional instruction tracing is disabled. 001 Conditional load instructions are traced. 010 Conditional store instructions are traced. 011 Conditional load and store instructions are traced. 111 All conditional instructions are traced. All other values are reserved.TRCIDR0.TRCCOND indicates whether this field is supported. If it is not supported then this field is RES0.
7	VMID	R/W	0h	VMID tracing bit: 0 VMID tracing is disabled. 1 VMID tracing is enabled. TRCIDR2.VMIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
6	CID	R/W	0h	Context ID tracing bit: 0 Context ID tracing is disabled. 1 Context ID tracing is enabled. TRCIDR2.CIDSIZE indicates whether this bit is supported. If it is not supported then this bit is RES0.
5	RES0_TRCCONFIGR_5_5	R/W	0h	Reserved, RES0.

Table 14-9193. A53SS_APBADDR_ETM_CPU1_TRCCONFIGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CCI	R/W	0h	Cycle counting instruction trace bit: 0 Cycle counting in the instruction trace is disabled. 1 Cycle counting in the instruction trace is enabled. TRCCCCTLR controls the threshold value for cycle counting. TRCIDR0.TRCCCI indicates whether this bit is supported. If it is not supported then this bit is RES0.
3	BB	R/W	0h	Branch broadcast mode bit: 0 Branch broadcast mode is disabled. 1 Branch broadcast mode is enabled. TRCBBCTLR controls which regions of memory are enabled to use branch broadcasting. TRCIDR0.TRCBB indicates whether this bit is supported. If it is not supported then this bit is RES0.
2:1	INSTP0	R/W	0h	Instruction P0 bit. This field controls whether load and store instructions are traced as P0 instructions: 00 Do not trace load and store instructions as P0 instructions. 01 Trace load instructions as P0 instructions. 10 Trace store instructions as P0 instructions. 11 Trace load and store instructions as P0 instructions. TRCIDR0.INSTP0 indicates whether this field is supported. If it is not supported then this field is RES0.
0	RES1_TRCCONFIGR_0_0	R/W	1h	Reserved, RES1.

14.3.1.1.2.504 A53SS_APBADDR_ETM_CPU1_TRCAUXCTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCAUXCTLR Register (Offset = 18h) [reset = 0h]

Auxiliary Control Register

Return to Summary Table

Table 14-9194. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0018h**

Figure 14-3049. A53SS_APBADDR_ETM_CPU1_TRCAUXCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCAUXCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
COREIFEN	RES0_TRCAUXCTLR_6_6	AUTHNOFLUSH	TSNODELAY	SYNCDELAY	OVFLW	IDLEACK	AFREADY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9196. A53SS_APBADDR_ETM_CPU1_TRCAUXCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUXCTLR_31_8	R/W	0h	Reserved RES0
7	COREIFEN	R/W	0h	Keep core interface enabled regardless of trace enable register state
6	RES0_TRCAUXCTLR_6_6	R/W	0h	Reserved RES0
5	AUTHNOFLUSH	R/W	0h	Do not flush trace on de-assertion of authentication inputs. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
4	TSNODELAY	R/W	0h	Do not delay timestamp insertion based on FIFO depth.
3	SYNCDELAY	R/W	0h	Delay periodic synchronization if FIFO is more than half-full.
2	OVFLW	R/W	0h	Force an overflow if synchronization is not completed when second synchronization becomes due. When this bit is set to 1 the trace unit behavior deviates from architecturally-specified behavior.
1	IDLEACK	R/W	0h	Force idle-drain acknowledge high CPU does not wait for trace to drain before entering WFX state. When this bit is set to 1 trace unit behavior deviates from architecturally-specified behavior.
0	AFREADY	R/W	0h	Always respond to AFREADY immediately. Does not have any interaction with FIFO draining even in WFI state.

14.3.1.1.2.505 A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL0R Register

1 A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL0R Register (Offset = 20h) [reset = 0h]

Event Control 0 Register

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Table 14-9197. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0020h**

Figure 14-3050. A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL0R Name Register

31	30	29	28	27	26	25	24
TYPE3	RESERVED_TRCEVENTCTL0R_30_28			SEL3			
R/W	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
TYPE2	RESERVED_TRCEVENTCTL0R_22_20			SEL2			
R/W	R/W			R/W			
0h	0h			0h			
15	14	13	12	11	10	9	8
TYPE1	RESERVED_TRCEVENTCTL0R_14_12			SEL1			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
TYPE0	RESERVED_TRCEVENTCTL0R_6_4			SEL0			
R/W	R/W			R/W			
0h	0h			0h			

Table 14-9199. A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL0R Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE3	R/W	0h	Selects the resource type for trace event 3
30:28	RESERVED_TRCEVENTCTL0R_30_28	R/W	0h	Reserved RES0
27:24	SEL3	R/W	0h	Selects the resource number based on the value of TYPE3
23	TYPE2	R/W	0h	Selects the resource type for trace event 2
22:20	RESERVED_TRCEVENTCTL0R_22_20	R/W	0h	Reserved RES0
19:16	SEL2	R/W	0h	Selects the resource number based on the value of TYPE2
15	TYPE1	R/W	0h	Selects the resource type for trace event 1
14:12	RESERVED_TRCEVENTCTL0R_14_12	R/W	0h	Reserved RES0
11:8	SEL1	R/W	0h	Selects the resource number based on the value of TYPE1
7	TYPE0	R/W	0h	Selects the resource type for trace event 0
6:4	RESERVED_TRCEVENTCTL0R_6_4	R/W	0h	Reserved RES0
3:0	SEL0	R/W	0h	Selects the resource number based on the value of TYPE0

14.3.1.1.2.506 A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL1R Register

1 A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL1R Register (Offset = 24h) [reset = 0h]

Event Control 1 Register

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Table 14-9200. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0024h**

Figure 14-3051. A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL1R Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCEVENTCTL1R_31_13							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCEVENTCTL1R_31_13			LPOVERRIDE	ATB	RESERVED_TRCEVENTCTL1R_10_4		
R/W			R/W	R/W	R/W		
0h			0h	0h	0h		
7	6	5	4	3	2	1	0
RESERVED_TRCEVENTCTL1R_10_4				EN			
R/W				R/W			
0h				0h			

Table 14-9202. A53SS_APBADDR_ETM_CPU1_TRCEVENTCTL1R Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_TRCEVENTCTL1R_31_13	R/W	0h	Reserved RES0
12	LPOVERRIDE	R/W	0h	Low power state behavior override
11	ATB	R/W	0h	ATB trigger enable
10:4	RESERVED_TRCEVENTCTL1R_10_4	R/W	0h	Reserved RES0
3:0	EN	R/W	0h	One bit per event to enable generation of an event element in the instruction trace stream when the selected event occurs

14.3.1.1.2.507 A53SS_APBADDR_ETM_CPU1_TRCSTALLCTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCSTALLCTLR Register (Offset = 2Ch) [reset = 0h]

Stall Control Register

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Table 14-9203. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 002Ch**

Figure 14-3052. A53SS_APBADDR_ETM_CPU1_TRCSTALLCTLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCSTALLCTLR_31_9							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCSTALLCTLR_31_9							ISTALL
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED_TRCSTALLCTLR_7_4				LEVEL		RESERVED_TRCSTALLCTLR_1_0	
R/W				R/W		R/W	
0h				0h		0h	

Table 14-9205. A53SS_APBADDR_ETM_CPU1_TRCSTALLCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_TRCSTALLCTLR_31_9	R/W	0h	Reserved RES0
8	ISTALL	R/W	0h	Controls if the trace unit can stall the processor when the instruction trace buffer space is less than LEVEL
7:4	RESERVED_TRCSTALLCTLR_7_4	R/W	0h	Reserved RES0
3:2	LEVEL	R/W	0h	The field can support 4 monotonic levels from 0b00 to 0b11
1:0	RESERVED_TRCSTALLCTLR_1_0	R/W	0h	Reserved RES0

14.3.1.1.2.508 A53SS_APBADDR_ETM_CPU1_TRCTSCTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCTSCTLR Register (Offset = 30h) [reset = 0h]

Global Timestamp Control Register

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Table 14-9206. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0030h**

Figure 14-3053. A53SS_APBADDR_ETM_CPU1_TRCTSCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCTSCTLR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCTSCTLR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCTSCTLR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EVENT							
R/W							
0h							

Table 14-9208. A53SS_APBADDR_ETM_CPU1_TRCTSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCTSCTLR_31_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams.

14.3.1.1.2.509 A53SS_APBADDR_ETM_CPU1_TRCSYNCPR Register

1 A53SS_APBADDR_ETM_CPU1_TRCSYNCPR Register (Offset = 34h) [reset = 0h]

Synchronization Period Register

Return to Summary Table

Table 14-9209. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0034h**

Figure 14-3054. A53SS_APBADDR_ETM_CPU1_TRCSYNCPR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCSYNCPR_31_5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RES0_TRCSYNCPR_31_5</td><td colspan="5">PERIOD</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-9211. A53SS_APBADDR_ETM_CPU1_TRCSYNCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCSYNCPR_31_5	R/W	0h	Reserved, RES0.
4:0	PERIOD	R/W	0h	Controls how many bytes of trace, the sum of instruction and data, that a trace unit can generate before a periodic trace synchronization request occurs. The number of bytes is always a power of two and the permitted values are: 00000 Periodic trace synchronization requests are disabled. This setting does not disable other types of trace synchronization request. 01000 Periodic trace synchronization request occurs after 2^8, or 256, bytes of trace. 01001 Periodic trace synchronization request occurs after 2^9, or 512, bytes of trace. 01010 Periodic trace synchronization request occurs after 2^10, or 1024, bytes of trace. and so on up to 0b10100, for which the request occurs after 2^20, or 1048576, bytes of trace.Values between 0b00001 and 0b001111 are reserved, as are values from 0b10101 onwards.

14.3.1.1.2.510 A53SS_APBADDR_ETM_CPU1_TRCCCCTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCCCCTLR Register (Offset = 38h) [reset = 0h]

Cycle Count Control Register

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Table 14-9212. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0038h**

Figure 14-3055. A53SS_APBADDR_ETM_CPU1_TRCCCCTLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCCCCTLR_31_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCCCCTLR_31_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RES0_TRCCCCTLR_31_12</td><td colspan="4">THRESHOLD</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">THRESHOLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9214. A53SS_APBADDR_ETM_CPU1_TRCCCCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RES0_TRCCCCTLR_31_12	R/W	0h	Reserved, RES0.
11:0	THRESHOLD	R/W	0h	Sets the threshold value for instruction trace cycle counting.The minimum threshold value that can be programmed into THRESHOLD is given in TRCIDR3.CCITMIN.Writing a value of zero might cause UNPREDICTABLE behaviour.

14.3.1.1.2.511 A53SS_APBADDR_ETM_CPU1_TRCBBCTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCBBCTLR Register (Offset = 3Ch) [reset = 0h]

Branch Broadcast Control Register

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Table 14-9215. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 003Ch**

Figure 14-3056. A53SS_APBADDR_ETM_CPU1_TRCBBCTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCBBCTLR_31_9							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCBBCTLR_31_9							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCBBCTLR_31_9							MODE
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
RANGE							
R/W							
0h							

Table 14-9217. A53SS_APBADDR_ETM_CPU1_TRCBBCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RES0_TRCBBCTLR_31_9	R/W	0h	Reserved, RES0.
8	MODE	R/W	0h	Mode bit: 0 Exclude mode. Branch broadcasting is not enabled in the address range that RANGE defines. If RANGE==0 then branch broadcasting is enabled for the entire memory map. 1 Include mode. Branch broadcasting is enabled in the address range that RANGE defines. If RANGE==0 then the branch broadcasting behavior is UNPREDICTABLE.
7:0	RANGE	R/W	0h	Address range field. Selects which address range comparator pairs are in use with branch broadcasting. Each bit represents an address range comparator pair, so bit[n] controls the selection of address range comparator pair n. If bit[n] is: 0 The address range that address range comparator pair n defines is not selected. 1 The address range that address range comparator pair n defines is selected.

14.3.1.1.2.512 A53SS_APBADDR_ETM_CPU1_TRCTRACEIDR Register

1 A53SS_APBADDR_ETM_CPU1_TRCTRACEIDR Register (Offset = 40h) [reset = 0h]

Trace ID Register

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Table 14-9218. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0040h**

Figure 14-3057. A53SS_APBADDR_ETM_CPU1_TRCTRACEIDR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_TRCTRACEIDR_31_7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_TRCTRACEIDR_31_7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_TRCTRACEIDR_31_7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED_TRCTRACEIDR_31_7</td><td colspan="7">TRACEID</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-9220. A53SS_APBADDR_ETM_CPU1_TRCTRACEIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_TRCTRACEIDR_31_7	R/W	0h	Reserved RES0
6:0	TRACEID	R/W	0h	Trace ID value. When only instruction tracing is enabled this provides the trace ID.

14.3.1.1.2.513 A53SS_APBADDR_ETM_CPU1_TRCVICTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCVICTLR Register (Offset = 80h) [reset = 0h]

ViewInst Main Control Register

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Table 14-9221. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0080h**

Figure 14-3058. A53SS_APBADDR_ETM_CPU1_TRCVICTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVICTLR_31_24							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCVICTLR_15_12				TRCERR	TRCRESET	SSSTATUS	RES0_TRCVICTLR_8_8
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVENT							
R/W							
0h							

Table 14-9223. A53SS_APBADDR_ETM_CPU1_TRCVICTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVICTLR_31_24	R/W	0h	Reserved, RES0.
23:20	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Non-secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Non-secure state, for exception level n. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.

Table 14-9223. A53SS_APBADDR_ETM_CPU1_TRCVICTLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level: 0 The trace unit generates instruction trace, in Secure state, for exception level n. 1 The trace unit does not generate instruction trace, in Secure state, for exception level n. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. If instruction tracing is not implemented for a given exception level, the corresponding bit in this field is not implemented. Unimplemented bits are RAZ/WI.
15:12	RES0_TRCVICTLR_15_12	R/W	0h	Reserved, RES0.
11	TRCERR	R/W	0h	If TRCIDR3.TRCERR==1, this bit controls whether a trace unit must trace a system error exception: 0 The trace unit does not trace a system error exception unless it traces the exception or instruction immediately prior to the system error exception. 1 The trace unit always traces a system error exception. If TRCIDR3.TRCERR==0, this bit is RES0.
10	TRCRESET	R/W	0h	Controls whether a trace unit must trace a Reset exception: 0 The trace unit does not trace a Reset exception unless it traces the exception or instruction immediately prior to the Reset exception. 1 The trace unit always traces a Reset exception.
9	SSSTATUS	R/W	0h	IF TRCIDR4.NUMACPAIRS>0 or TRCIDR.NUMPC>0, this bit returns the status of the start-stop logic: 0 The start-stop logic is in the stopped state. 1 The start-stop logic is in the started state. The bit only returns stable data when TRCSTATR.PMSTABLE==1.Before software enables the trace unit, TRCPRGCTLR.EN==1, it must write to this bit to set the initial state of the start-stop logic. If the start-stop logic is not used then set this bit to 1. ARM recommends that the value of this bit is set before each trace run begins.If TRCIDR4.NUMACPAIRS==0 and TRCIDR4.NUMPC==0, this bit is RES0, indicating that the start-stop logic is not implemented.
8	RES0_TRCVICTLR_8_8	R/W	0h	Reserved, RES0.
7:0	EVENT	R/W	0h	An event selector. [TODO: Add the bit assignments for EVENT fields into the descriptions directly?]

14.3.1.1.2.514 A53SS_APBADDR_ETM_CPU1_TRCVIIECTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCVIIECTLR Register (Offset = 84h) [reset = 0h]

ViewInst Include-Exclude Control Register

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Table 14-9224. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0084h**

Figure 14-3059. A53SS_APBADDR_ETM_CPU1_TRCVIIECTLR Name Register

31	30	29	28	27	26	25	24
RES0_TRCVIIECTLR_31_24							
R/W							
0h							
23	22	21	20	19	18	17	16
EXCLUDE							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCVIIECTLR_15_8							
R/W							
0h							
7	6	5	4	3	2	1	0
INCLUDE							
R/W							
0h							

Table 14-9226. A53SS_APBADDR_ETM_CPU1_TRCVIIECTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES0_TRCVIIECTLR_31_24	R/W	0h	Reserved, RES0.
23:16	EXCLUDE	R/W	0h	0 1 The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:8	RES0_TRCVIIECTLR_15_8	R/W	0h	Reserved, RES0.
7:0	INCLUDE	R/W	0h	Include range field. Selects which address range comparator pairs are in use with ViewInst include control. Each bit represents an address range comparator pair, so bit[m] controls the selection of address range comparator pair m. If bit[m] is: 0 The address range that address range comparator pair m defines is not selected for ViewInst include control. 1 The address range that address range comparator pair m defines is selected for ViewInst include control. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.Selecting no include comparators indicates that all instructions are included by default. The exclude control then indicates which ranges are excluded.

14.3.1.1.2.515 A53SS_APBADDR_ETM_CPU1_TRCVISSCTLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCVISSCTLR Register (Offset = 88h) [reset = 0h]

ViewInst Start-Stop Control Register

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Table 14-9227. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0088h**

Figure 14-3060. A53SS_APBADDR_ETM_CPU1_TRCVISSCTLR Name Register

31	30	29	28	27	26	25	24
STOP							
R/W							
0h							
23	22	21	20	19	18	17	16
STOP							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 14-9229. A53SS_APBADDR_ETM_CPU1_TRCVISSCTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STOP	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of stopping trace. Each bit represents a single address comparator, so bit[m] controls the selection of single address comparator m-16. If bit[m] is: 0 The single address comparator m-16 is not selected as a stop resource. 1 The single address comparator m-16 is selected as a stop resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.
15:0	START	R/W	0h	Selects which single address comparators are in use with ViewInst start-stop control, for the purpose of starting trace. Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n is not selected as a start resource. 1 The single address comparator n is selected as a start resource. The implemented width of the field, n, is IMPLEMENTATION DEFINED and is set by the value of 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.516 A53SS_APBADDR_ETM_CPU1_TRCSEQEVR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCSEQEVR0 Register (Offset = 100h) [reset = 0h]

Sequencer State Transition Control Registers 0

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Table 14-9230. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0100h**

Figure 14-3061. A53SS_APBADDR_ETM_CPU1_TRCSEQEVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQEVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
B_N							
R/W							
0h							
7	6	5	4	3	2	1	0
F_N							
R/W							
0h							

Table 14-9232. A53SS_APBADDR_ETM_CPU1_TRCSEQEVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR0_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.517 A53SS_APBADDR_ETM_CPU1_TRCSEQEVR1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCSEQEVR1 Register (Offset = 104h) [reset = 0h]

Sequencer State Transition Control Registers 1

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Table 14-9233. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0104h**

Figure 14-3062. A53SS_APBADDR_ETM_CPU1_TRCSEQEVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQEVR1_31_16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
B_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F_N							
R/W							
0h							

Table 14-9235. A53SS_APBADDR_ETM_CPU1_TRCSEQEVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR1_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.518 A53SS_APBADDR_ETM_CPU1_TRCSEQEVR2 Register

1 A53SS_APBADDR_ETM_CPU1_TRCSEQEVR2 Register (Offset = 108h) [reset = 0h]

Sequencer State Transition Control Registers 2

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Table 14-9236. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0108h**

Figure 14-3063. A53SS_APBADDR_ETM_CPU1_TRCSEQEVR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQEVR2_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
B_N							
R/W							
0h							
7	6	5	4	3	2	1	0
F_N							
R/W							
0h							

Table 14-9238. A53SS_APBADDR_ETM_CPU1_TRCSEQEVR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCSEQEVR2_31_16	R/W	0h	Reserved, RES0.
15:8	B_N	R/W	0h	Backward field. Contains an event number. When the event occurs then the sequencer state moves from state n+1 to state n.For example, for TRCSEQEVR2, if B2==0x14 then when event 0x14 occurs, the sequencer moves from state 3 to state 2.
7:0	F_N	R/W	0h	Forward field. Contains an event number. When the event occurs then the sequencer state moves from state n to state n+1.For example, for TRCSEQEVR1, if F1==0x12 then when event 0x12 occurs, the sequencer moves from state 1 to state 2.

14.3.1.1.2.519 A53SS_APBADDR_ETM_CPU1_TRCSEQRSTEVR Register

1 A53SS_APBADDR_ETM_CPU1_TRCSEQRSTEVR Register (Offset = 118h) [reset = 0h]

Sequencer Reset Control Register

Return to Summary Table

Table 14-9239. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0118h**

Figure 14-3064. A53SS_APBADDR_ETM_CPU1_TRCSEQRSTEVR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSEQRSTEVR_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RST							
R/W							
0h							

Table 14-9241. A53SS_APBADDR_ETM_CPU1_TRCSEQRSTEVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCSEQRSTEVR_31_8	R/W	0h	Reserved, RES0.
7:0	RST	R/W	0h	Contains an event number. When the event occurs then the sequencer state moves to state 0.

14.3.1.1.2.520 A53SS_APBADDR_ETM_CPU1_TRCSEQSTR Register

1 A53SS_APBADDR_ETM_CPU1_TRCSEQSTR Register (Offset = 11Ch) [reset = 0h]

Sequencer State Register

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Table 14-9242. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 011Ch**

Figure 14-3065. A53SS_APBADDR_ETM_CPU1_TRCSEQSTR Name Register

31	30	29	28	27	26	25	24
RES0_TRCSEQSTR_31_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCSEQSTR_31_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCSEQSTR_31_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCSEQSTR_31_2						STATE	
R/W						R/W	
0h						0h	

Table 14-9244. A53SS_APBADDR_ETM_CPU1_TRCSEQSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES0_TRCSEQSTR_31_2	R/W	0h	Reserved, RES0.
1:0	STATE	R/W	0h	Sets or returns the state of the sequencer: 00 State 0. 01 State 1. 10 State 2. 11 State 3.

14.3.1.1.2.521 A53SS_APBADDR_ETM_CPU1_TRCEXTINSELR Register

1 A53SS_APBADDR_ETM_CPU1_TRCEXTINSELR Register (Offset = 120h) [reset = 0h]

External Input Select Register

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Table 14-9245. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0120h**

Figure 14-3066. A53SS_APBADDR_ETM_CPU1_TRCEXTINSELR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCEXTINSELR_31_29			SEL3				
R/W			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED_TRCEXTINSELR_23_21			SEL2				
R/W			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED_TRCEXTINSELR_15_13			SEL1				
R/W			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED_TRCEXTINSELR_7_5			SEL0				
R/W			R/W				
0h			0h				

Table 14-9247. A53SS_APBADDR_ETM_CPU1_TRCEXTINSELR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED_TRCEXTINSELR_31_29	R/W	0h	Reserved RES0
28:24	SEL3	R/W	0h	Selects an event from the external input bus for External Input Resource 3.
23:21	RESERVED_TRCEXTINSELR_23_21	R/W	0h	Reserved RES0
20:16	SEL2	R/W	0h	Selects an event from the external input bus for External Input Resource 2
15:13	RESERVED_TRCEXTINSELR_15_13	R/W	0h	Reserved RES0
12:8	SEL1	R/W	0h	Selects an event from the external input bus for External Input Resource 1
7:5	RESERVED_TRCEXTINSELR_7_5	R/W	0h	Reserved RES0
4:0	SEL0	R/W	0h	Selects an event from the external input bus for External Input Resource 0

14.3.1.1.2.522 A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR0 Register (Offset = 140h) [reset = 0h]

Counter Reload Value Registers 0

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Table 14-9248. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0140h**

Figure 14-3067. A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTRLDVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-9250. A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.523 A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR1 Register (Offset = 144h) [reset = 0h]

Counter Reload Value Registers 1

Return to Summary Table

Table 14-9251. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0144h**

Figure 14-3068. A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTRLDVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-9253. A53SS_APBADDR_ETM_CPU1_TRCCNTRLDVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTRLDVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the reload value for counter <n>. When a reload event occurs for counter <n> then the trace unit copies the VALUE<n> field into counter <n>.

14.3.1.1.2.524 A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR0 Register (Offset = 150h) [reset = 0h]

Counter Control Register 0

Return to Summary Table

Table 14-9254. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0150h**

Figure 14-3069. A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR0_31_18							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTCTLR0_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RLDEVENT_N							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTEVENT_N							
R/W							
0h							

Table 14-9256. A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR0_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.525 A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR1 Register (Offset = 154h) [reset = 0h]

Counter Control Register 1

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Table 14-9257. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0154h**

Figure 14-3070. A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTCTLR1_31_18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCNTCTLR1_31_18						CNTCHAIN_N	RLDSELF_N
R/W						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RLDEVENT_N							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CNTEVENT_N							
R/W							
0h							

Table 14-9259. A53SS_APBADDR_ETM_CPU1_TRCCNTCTLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RES0_TRCCNTCTLR1_31_18	R/W	0h	Reserved, RES0.
17	CNTCHAIN_N	R/W	0h	For TRCCNTCTLR3 and TRCCNTCTLR1, controls whether counter <n> decrements when a reload event occurs for counter <n-1>: 0 1 For TRCCNTCTLR2 and TRCCNTCTLR0, this bit is RES0.
16	RLDSELF_N	R/W	0h	Controls whether a reload event occurs for counter <n>, when counter <n> reaches zero: 0 The trace unit does not generate a reload event. 1 The trace unit generates a reload event for counter <n>, provided that the event resource that CNTEVENT<n> specifies is active.
15:8	RLDEVENT_N	R/W	0h	Selects an event, that when it occurs causes a reload event for counter <n>.
7:0	CNTEVENT_N	R/W	0h	Selects an event, that when it occurs causes counter <n> to decrement.

14.3.1.1.2.526 A53SS_APBADDR_ETM_CPU1_TRCCNTVR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCNTVR0 Register (Offset = 160h) [reset = 0h]

Counter Value Registers 0

Return to Summary Table

Table 14-9260. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0160h**

Figure 14-3071. A53SS_APBADDR_ETM_CPU1_TRCCNTVR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR0_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR0_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-9262. A53SS_APBADDR_ETM_CPU1_TRCCNTVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR0_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.527 A53SS_APBADDR_ETM_CPU1_TRCCNTVR1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCNTVR1 Register (Offset = 164h) [reset = 0h]

Counter Value Registers 1

Return to Summary Table

Table 14-9263. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0164h**

Figure 14-3072. A53SS_APBADDR_ETM_CPU1_TRCCNTVR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCNTVR1_31_16							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCNTVR1_31_16							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_N							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_N							
R/W							
0h							

Table 14-9265. A53SS_APBADDR_ETM_CPU1_TRCCNTVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES0_TRCCNTVR1_31_16	R/W	0h	Reserved, RES0.
15:0	VALUE_N	R/W	0h	Contains the count value of counter <n>.

14.3.1.1.2.528 A53SS_APBADDR_ETM_CPU1_TRCIDR8 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR8 Register (Offset = 180h) [reset = 0h]

ID Register 8

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Table 14-9266. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0180h**

Figure 14-3073. A53SS_APBADDR_ETM_CPU1_TRCIDR8 Name Register

31	30	29	28	27	26	25	24
MAXSPEC							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAXSPEC							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAXSPEC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAXSPEC							
R/W							
0h							

Table 14-9268. A53SS_APBADDR_ETM_CPU1_TRCIDR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAXSPEC	R/W	0h	Indicates the maximum speculation depth of the instruction trace stream. This is the maximum number of P0 elements in the trace stream that can be speculative at any time.

14.3.1.1.2.529 A53SS_APBADDR_ETM_CPU1_TRCIDR9 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR9 Register (Offset = 184h) [reset = 0h]

ID Register 9

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Table 14-9269. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0184h**

Figure 14-3074. A53SS_APBADDR_ETM_CPU1_TRCIDR9 Name Register

31	30	29	28	27	26	25	24
NUMP0KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP0KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP0KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP0KEY							
R/W							
0h							

Table 14-9271. A53SS_APBADDR_ETM_CPU1_TRCIDR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP0KEY	R/W	0h	Indicates the number of P0 right-hand keys that the trace unit can use. A value of 0 or 1 indicates one P0 key.

14.3.1.1.2.530 A53SS_APBADDR_ETM_CPU1_TRCIDR10 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR10 Register (Offset = 188h) [reset = 0h]

ID Register 10

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Table 14-9272. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0188h**

Figure 14-3075. A53SS_APBADDR_ETM_CPU1_TRCIDR10 Name Register

31	30	29	28	27	26	25	24
NUMP1KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1KEY							
R/W							
0h							

Table 14-9274. A53SS_APBADDR_ETM_CPU1_TRCIDR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1KEY	R/W	0h	Indicates the number of P1 right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.531 A53SS_APBADDR_ETM_CPU1_TRCIDR11 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR11 Register (Offset = 18Ch) [reset = 0h]

ID Register 11

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Table 14-9275. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 018Ch**

Figure 14-3076. A53SS_APBADDR_ETM_CPU1_TRCIDR11 Name Register

31	30	29	28	27	26	25	24
NUMP1SPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMP1SPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMP1SPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMP1SPC							
R/W							
0h							

Table 14-9277. A53SS_APBADDR_ETM_CPU1_TRCIDR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMP1SPC	R/W	0h	Indicates the number of special P1 right-hand keys that the trace unit can use.

14.3.1.1.2.532 A53SS_APBADDR_ETM_CPU1_TRCIDR12 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR12 Register (Offset = 190h) [reset = 0h]

ID Register 12

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Table 14-9278. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0190h**

Figure 14-3077. A53SS_APBADDR_ETM_CPU1_TRCIDR12 Name Register

31	30	29	28	27	26	25	24
NUMCONDKEY							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDKEY							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDKEY							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDKEY							
R/W							
0h							

Table 14-9280. A53SS_APBADDR_ETM_CPU1_TRCIDR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDKEY	R/W	0h	Indicates the number of conditional instruction right-hand keys that the trace unit can use. The number includes normal and special keys.

14.3.1.1.2.533 A53SS_APBADDR_ETM_CPU1_TRCIDR13 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR13 Register (Offset = 194h) [reset = 0h]

ID Register 13

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Table 14-9281. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0194h**

Figure 14-3078. A53SS_APBADDR_ETM_CPU1_TRCIDR13 Name Register

31	30	29	28	27	26	25	24
NUMCONDSPC							
R/W							
0h							
23	22	21	20	19	18	17	16
NUMCONDSPC							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMCONDSPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NUMCONDSPC							
R/W							
0h							

Table 14-9283. A53SS_APBADDR_ETM_CPU1_TRCIDR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NUMCONDSPC	R/W	0h	Indicates the number of special conditional instruction right-hand keys that the trace unit can use.

14.3.1.1.2.534 A53SS_APBADDR_ETM_CPU1_TRCIMSPEC0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIMSPEC0 Register (Offset = 1C0h) [reset = 0h]

Implementation Specific Register 0

Return to Summary Table

Table 14-9284. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01C0h**

Figure 14-3079. A53SS_APBADDR_ETM_CPU1_TRCIMSPEC0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCIMSPEC0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
EN				SUPPORT			
R/W				R/W			
0h				0h			

Table 14-9286. A53SS_APBADDR_ETM_CPU1_TRCIMSPEC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCIMSPEC0_31_8	R/W	0h	Reserved, RES0.
7:4	EN	R/W	0h	If SUPPORT is not 0b0000, controls whether the IMPLEMENTATION DEFINED features are enabled. The permitted values are: 0000 The IMPLEMENTATION DEFINED features are not enabled. The trace unit must behave as if the IMPLEMENTATION DEFINED features are not supported. and any other value, which indicates that the trace unit behavior is IMPLEMENTATION DEFINED.If SUPPORT is 0b0000, this field is RES0.
3:0	SUPPORT	R/W	0h	Indicates whether the implementation supports IMPLEMENTATION DEFINED features. The permitted values are: 0000 No IMPLEMENTATION DEFINED features are supported. The EN field is RES0. and any other value, which indicates that IMPLEMENTATION DEFINED features are supported. Use of these values requires written permission from ARM.

14.3.1.1.2.535 A53SS_APBADDR_ETM_CPU1_TRCIDR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR0 Register (Offset = 1E0h) [reset = 28000EA1h]

ID Register 0

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Table 14-9287. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01E0h**

Figure 14-3080. A53SS_APBADDR_ETM_CPU1_TRCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR0_31_30		COMMOPT	TSSIZE				
R/W		R/W	R/W				
0h		1h	8h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCIDR0_23_17							QSUPP
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
QSUPP	QFILT	CONDTYPE		NUMEVENT		RETSTACK	RES0_TRCIDR0_8_8
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		3h		1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRCCCI	TRCCOND	TRCBB	TRCDATA		INSTP0		RES0_TRCIDR0_0_0
R/W	R/W	R/W	R/W		R/W		R/W
1h	0h	1h	0h		0h		1h

Table 14-9289. A53SS_APBADDR_ETM_CPU1_TRCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RES0_TRCIDR0_31_30	R/W	0h	Reserved, RES0.
29	COMMOPT	R/W	1h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
28:24	TSSIZE	R/W	8h	Global timestamp size field. The permitted values are: 00000 Global timestamping is not implemented. 00110 Implementation supports a maximum global timestamp of 48bits. 01000 Implementation supports a maximum global timestamp of 64bits. All other values are reserved.When global timestamping is implemented then TRCCONFIGR.TS and TRCTSCTLR are supported.
23:17	RES0_TRCIDR0_23_17	R/W	0h	Reserved, RES0.

Table 14-9289. A53SS_APBADDR_ETM_CPU1_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:15	QSUPP	R/W	0h	Q element support field. The permitted values are: 00 Q element support is not implemented. TRCCONFIGR.QE is RES0. 01 Q element support is implemented, and only supports Q elements with instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b01. 10 Q element support is implemented, and only supports Q elements without instruction counts. TRCCONFIGR.QE can only take the values 0b00 or 0b11. 11 Q element support is implemented, and supports both Q elements with instruction counts and Q elements without instruction counts. TRCCONFIGR.QE is fully implemented.
14	QFILT	R/W	0h	Q element filtering support field. The permitted values are: 0 Q element filtering is not implemented. 1 Q element filtering is implemented. TRCQCTLR is implemented. When QSUPP==0b00, this field is RES0.
13:12	CONDTYPE	R/W	0h	Conditional tracing field. The permitted values are: 00 The trace unit indicates only if a conditional instruction is a pass or fail. 01 The trace unit provides the Current Program Status Register [CPSR] status, for a conditional instruction. All other values are reserved.
11:10	NUMEVENT	R/W	3h	Number of events field. Indicates how many events the trace unit supports: 00 The trace unit supports 1 event. 01 The trace unit supports 2 events. 10 The trace unit supports 3 events. 11 The trace unit supports 4 events. This field controls how many fields are supported in TRCEVENTCTL0R, and indicates the size of TRCEVENTCTL1R.INSTEN.
9	RETSTACK	R/W	1h	Return stack bit. Indicates if the implementation supports a return stack: 0 Return stack is not implemented. 1 Return stack is implemented, so TRCCONFIGR.RS is supported.
8	RES0_TRCIDR0_8_8	R/W	0h	Reserved, RES0.
7	TRCCCI	R/W	1h	Cycle counting instruction bit. Indicates if the trace unit supports cycle counting for instructions: 0 Cycle counting in the instruction trace is not implemented. 1 Cycle counting in the instruction trace is implemented, so TRCCONFIGR.CCI and TRCCCCTLR are supported.

Table 14-9289. A53SS_APBADDR_ETM_CPU1_TRCIDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRCCOND	R/W	0h	Conditional instruction tracing support bit. Indicates if the trace unit supports conditional instruction tracing: 0 Conditional instruction tracing is not supported. 1 Conditional instruction tracing is supported, so TRCCONFIGR.COND is supported.
5	TRCBB	R/W	1h	Branch broadcast tracing support bit. Indicates if the trace unit supports branch broadcast tracing: 0 Branch broadcast tracing is not supported. 1 Branch broadcast tracing is supported, so TRCCONFIGR.BB and TRCBBCTLR are supported.
4:3	TRCDATA	R/W	0h	Conditional tracing field. The permitted values are: 00 Data tracing is not supported. 11 Tracing of data addresses and data values is supported, so TRCCONFIGR.DA, TRCCONFIGR.DV, TRCSTALLCTLR.DATADISCARD, TRCSTALLCTLR.INSTPRIORITY, TRCSTALLCTLR.DSTALL, and TRCEVENTCTL1R.DATAEN are supported. All other values are reserved.
2:1	INSTP0	R/W	0h	P0 tracing support field. The permitted values are: 00 Tracing of load and store instructions as P0 elements is not supported. 11 Tracing of load and store instructions as P0 elements is supported, so TRCCONFIGR.INSTP0 is supported. All other values are reserved.
0	RES0_TRCIDR0_0_0	R/W	1h	Reserved, RES0.

14.3.1.1.2.536 A53SS_APBADDR_ETM_CPU1_TRCIDR1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR1 Register (Offset = 1E4h) [reset = 4100F404h]

ID Register 1

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Table 14-9290. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01E4h**

Figure 14-3081. A53SS_APBADDR_ETM_CPU1_TRCIDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DESIGNER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">41h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCIDR1_23_16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RES1_TRCIDR1_15_12</td><td colspan="4">TRCARCHMAJ</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Fh</td><td colspan="4">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">TRCARCHMIN</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-9292. A53SS_APBADDR_ETM_CPU1_TRCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DESIGNER	R/W	41h	Indicates which company designed the trace unit. The permitted values are: 01000001 ARM Limited. 01000100 Digital Equipment Corporation. 01001101 Motorola, Freescale Semiconductor Inc. 01010001 QUALCOMM Inc. 01010110 Marvell Semiconductor Inc. 01101001 Intel Corporation. All other values are reserved.
23:16	RES0_TRCIDR1_23_16	R/W	0h	Reserved, RES0.
15:12	RES1_TRCIDR1_15_12	R/W	Fh	Reserved, RES1.
11:8	TRCARCHMAJ	R/W	4h	Indicates the major version of the ETM architecture. The permitted value is: 100 ETMv4. All other values are reserved.

Table 14-9292. A53SS_APBADDR_ETM_CPU1_TRCIDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	TRCARCHMIN	R/W	0h	Indicates the minor version of the ETM architecture. The permitted value is: 0 ETMv4 minor version 0. All other values are reserved.
3:0	REVISION	R/W	4h	Returns an IMPLEMENTATION DEFINED value that identifies the revision of the trace registers and the OS Save and Restore registers.ARM recommends:That the initial implementation sets REVISION==0x0 and the field then increments for any subsequent implementations. However, it is acceptable to omit some values or use another scheme to identify the revision number.That TRCPIDR2.REVISION==TRCIDR1.REVISION. However, in situations where it is difficult to align these fields, such as with a metal layer fix, then it is acceptable to change the REVISION fields independently.

14.3.1.1.2.537 A53SS_APBADDR_ETM_CPU1_TRCIDR2 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR2 Register (Offset = 1E8h) [reset = 488h]

ID Register 2

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Table 14-9293. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01E8h**

Figure 14-3082. A53SS_APBADDR_ETM_CPU1_TRCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCIDR2_31_29			CCSIZE				DVSIZE
R/W			R/W				R/W
0h			0h				0h
23	22	21	20	19	18	17	16
DVSIZE				DASIZE			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
DASIZE	VMIDSIZE					CIDSIZE	
R/W	R/W					R/W	
0h	1h					4h	
7	6	5	4	3	2	1	0
CIDSIZE			IASIZE				
R/W			R/W				
4h			8h				

Table 14-9295. A53SS_APBADDR_ETM_CPU1_TRCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES0_TRCIDR2_31_29	R/W	0h	Reserved, RES0.
28:25	CCSIZE	R/W	0h	Indicates the size of the cycle counter in bits minus 12. 0000 The cycle counter is 12 bits in length. 0001 The cycle counter is 13 bits in length. and so on up to 0b1000, indicating the cycle counter is 20 bits in length.All other values are reserved.If cycle counting is not implemented, as indicated by TRCIDR0.TRCCCI, this field is 0b0000.
24:20	DVSIZE	R/W	0h	Indicates the data value size in bytes. The permitted values are: 00000 Data value tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data value size. 01000 Maximum of 64-bit data value size. All other values are reserved.

Table 14-9295. A53SS_APBADDR_ETM_CPU1_TRCIDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	DASIZE	R/W	0h	Indicates the data address size in bytes. The permitted values are: 00000 Data address tracing is not supported. Therefore, an implementation must also set TRCIDR0.TRCDATA==0b00. 00100 Maximum of 32-bit data address size. 01000 Maximum of 64-bit data address size. All other values are reserved.
14:10	VMIDSIZE	R/W	1h	Indicates the VMID size. The permitted values are: 00000 VMID tracing is not supported. 00001 Maximum of 8-bit VMID size, so TRCCONFIGR.VMID is supported. All other values are reserved.
9:5	CIDSIZE	R/W	4h	Indicates the Context ID size. The permitted values are: 00000 Context ID tracing is not supported. 00100 Maximum of 32-bit Context ID size, so TRCCONFIGR.CID is supported. All other values are reserved.
4:0	IASIZE	R/W	8h	Indicates the instruction address size. The permitted values are: 00100 Maximum of 32-bit address size. 01000 Maximum of 64-bit address size. All other values are reserved.

14.3.1.1.2.538 A53SS_APBADDR_ETM_CPU1_TRCIDR3 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR3 Register (Offset = 1ECh) [reset = D7B0004h]

ID Register 3

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Table 14-9296. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01ECh**

Figure 14-3083. A53SS_APBADDR_ETM_CPU1_TRCIDR3 Name Register

31	30	29	28	27	26	25	24
NOOVERFLOW	NUMPROC			SYSSTALL	STALLCTL	SYNCPR	TRCERR
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			1h	1h	0h	1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
7h				Bh			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCIDR3_15_12				CCITMIN			
R/W				R/W			
0h				4h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CCITMIN							
R/W							
4h							

Table 14-9298. A53SS_APBADDR_ETM_CPU1_TRCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOOVERFLOW	R/W	0h	Indicates if TRCSTALLCTLR.NOOVERFLOW is supported: 0 TRCSTALLCTLR.NOOVERFLOW is not supported, or STALLCTL==0. 1 TRCSTALLCTLR.NOOVERFLOW is supported.
30:28	NUMPROC	R/W	0h	Indicates the number of processors available for tracing. The possible values are: 000 The trace unit can trace one processor. 001 The trace unit can trace two processors. 010 The trace unit can trace three processors. and so on up to 0b111, which indicates the trace unit can trace eight processors.This field sets the maximum value of TRCPROCSELR.PROCSEL.
27	SYSSTALL	R/W	1h	Indicates if the implementation can support stall control: 0 The system does not support stall control of the processor. 1 The system can support stall control of the processor. The system supports stalling of the processor only when SYSSTALL==1 and STALLCTL==1.

Table 14-9298. A53SS_APBADDR_ETM_CPU1_TRCIDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	STALLCTL	R/W	1h	Indicates if TRCSTALLCTLR is supported: 0 TRCSTALLCTLR is not supported. 1 TRCSTALLCTLR is supported.
25	SYNCPR	R/W	0h	Indicates if an implementation has a fixed synchronization period: 0 TRCSYNCPR is read-write so software can change the synchronization period. 1 TRCSYNCPR is read-only so the synchronization period is fixed.
24	TRCERR	R/W	1h	Indicates if TRCVICTLR.TRCERR is supported: 0 TRCVICTLR.TRCERR is not supported 1 TRCVICTLR.TRCERR is supported.
23:20	EXLEVEL_NS	R/W	7h	In Non-secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Non-secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are not supported. 1 In Non-secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_NS and TRCVICTLR.EXLEVEL_NS are supported. The exception levels are:Bit[20]Exception level 0.Bit[21]Exception level 1.Bit[22]Exception level 2.Bit[23]SBZ. EXLEVEL_NS[3] is never implemented.
19:16	EXLEVEL_S	R/W	Bh	In Secure state, each bit indicates whether instruction tracing is supported for the corresponding exception level: 0 In Secure state, exception level n is not supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are not supported. 1 In Secure state, exception level n is supported so the corresponding bits in TRCACATRn.EXLEVEL_S and TRCVICTLR.EXLEVEL_S are supported. The exception levels are:Bit[16]Exception level 0.Bit[17]Exception level 1.Bit[18]SBZ. EXLEVEL_S[2] is never implemented.Bit[19]Exception level 3.
15:12	RES0_TRCIDR3_15_12	R/W	0h	Reserved, RES0.
11:0	CCITMIN	R/W	4h	Indicates the minimum value that can be programmed in TRCCCCTLR.THRESHOLD.When cycle counting in the instruction trace is supported, that is TRCIDR0.TRCCCI==1, then the minimum value of this field is 0x001, otherwise it is 0x000.

14.3.1.1.2.539 A53SS_APBADDR_ETM_CPU1_TRCIDR4 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR4 Register (Offset = 1F0h) [reset = 11170004h]

ID Register 4

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Table 14-9299. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01F0h**

Figure 14-3084. A53SS_APBADDR_ETM_CPU1_TRCIDR4 Name Register

31	30	29	28	27	26	25	24
NUMVMIDC				NUMCIDC			
R/W				R/W			
1h				1h			
23	22	21	20	19	18	17	16
NUMSSCC				NUMRSPAIR			
R/W				R/W			
1h				7h			
15	14	13	12	11	10	9	8
NUMPC				RES0_TRCIDR4_11_9			SUPPDAC
R/W				R/W			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
NUMDVC				NUMACPAIRS			
R/W				R/W			
0h				4h			

Table 14-9301. A53SS_APBADDR_ETM_CPU1_TRCIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	NUMVMIDC	R/W	1h	Indicates the number of VMID comparators that are available for tracing. The permitted values are: 0000 No VMID comparators are available. 0001 The implementation has one VMID comparator. 0010 The implementation has two VMID comparators. and so on up to 0b1000, which indicates that the implementation has eight VMID comparators.All other values are reserved.
27:24	NUMCIDC	R/W	1h	Indicates the number of Context ID comparators that are available for tracing. The permitted values are: 0000 No Context ID comparators are available. 0001 The implementation has one Context ID comparator. 0010 The implementation has two Context ID comparators. and so on up to 0b1000, which indicates that the implementation has eight Context ID comparators.All other values are reserved.

Table 14-9301. A53SS_APBADDR_ETM_CPU1_TRCIDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:20	NUMSSCC	R/W	1h	Indicates the number of single-shot comparator controls that are available for tracing. The permitted values are: 0000 No single-shot comparator controls are available. 0001 The implementation has one single-shot comparator control. 0010 The implementation has two single-shot comparator controls. and so on up to 0b1000, which indicates that the implementation has eight single-shot comparator controls.All other values are reserved.
19:16	NUMRSPAIR	R/W	7h	Indicates the number of resource selection pairs that are available for tracing. The permitted values are: 0000 The implementation has one resource selection pair. 0001 The implementation has two resource selection pairs. 0010 The implementation has three resource selection pairs. and so on up to 0b1111, which indicates that the implementation has 16 resource selection pairs.Implementations always have at least one resource selection pair so that they can support the FALSE and TRUE resource selectors, 0 and 1.
15:12	NUMPC	R/W	0h	Indicates the number of processor comparator inputs that are available for tracing. The permitted values are: 0000 No processor comparator inputs are available. 0001 The implementation has one processor comparator input. 0010 The implementation has two processor comparator inputs. and so on up to 0b1000, which indicates that the implementation has eight processor comparator inputs.All other values are reserved.
11:9	RES0_TRCIDR4_11_9	R/W	0h	Reserved, RES0.
8	SUPPDAC	R/W	0h	Indicates if the implementation can support data address comparisons: 0 The implementation does not support data address comparisons. 1 The implementation can support data address comparisons
7:4	NUMDVC	R/W	0h	Indicates the number of data value comparators that are available for tracing. The permitted values are: 0000 No data value comparators are available. 0001 The implementation has one data value comparator. 0010 The implementation has two data value comparators. and so on up to 0b1000, which indicates that the implementation has eight data value comparators.All other values are reserved.
3:0	NUMACPAIRS	R/W	4h	Indicates the number of address comparator pairs that are available for tracing. The permitted values are: 0000 No address comparator pairs are available. 0001 The implementation has one address comparator pair. 0010 The implementation has two address comparator pairs. and so on up to 0b1000, which indicates that the implementation has eight address comparator pairs.All other values are reserved.

14.3.1.1.2.540 A53SS_APBADDR_ETM_CPU1_TRCIDR5 Register

1 A53SS_APBADDR_ETM_CPU1_TRCIDR5 Register (Offset = 1F4h) [reset = 28C7081Eh]

ID Register 5

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Table 14-9302. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 01F4h**

Figure 14-3085. A53SS_APBADDR_ETM_CPU1_TRCIDR5 Name Register

31	30	29	28	27	26	25	24
REDFUNCNTR	NUMCNTR			NUMSEQSTATE			RES0_TRCIDR5_24_24
R/W	R/W			R/W			R/W
0h	2h			4h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPOVERRIDE	ATBTRIG	TRACEIDSIZE					
R/W	R/W	R/W					
1h	1h	7h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCIDR5_15_12				NUMEXTINSEL			NUMEXTIN
R/W				R/W			R/W
0h				4h			1Eh
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUMEXTIN							
R/W							
1Eh							

Table 14-9304. A53SS_APBADDR_ETM_CPU1_TRCIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REDFUNCNTR	R/W	0h	Indicates if the reduced function counter is implemented: 0 The reduced function counter is not supported. 1 Counter 0 is implemented as a reduced function counter.
30:28	NUMCNTR	R/W	2h	Indicates the number of counters that are available for tracing. The permitted values are: 000 No counters are available. 001 The implementation has one counter. 010 The implementation has two counters. 011 The implementation has three counters. 100 The implementation has four counters. All other values are reserved.

Table 14-9304. A53SS_APBADDR_ETM_CPU1_TRCIDR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:25	NUMSEQSTATE	R/W	4h	Indicates the number of sequencer states that are implemented. The permitted values are: 000 No sequencer states are implemented. 100 The implementation has four sequencer states. All other values are reserved.
24	RES0_TRCIDR5_24_24	R/W	0h	Reserved, RES0.
23	LPOVERRIDE	R/W	1h	Indicates if the implementation can support low-power state override: 0 The implementation does not support low-power state override. 1 The implementation supports low-power state override, and the TRCEVENTCTL1R.LPOVERRIDE field is implemented. The trace unit must support low-power state override if it can enter a low-power mode where the resources and event trace generation are disabled.
22	ATBTRIG	R/W	1h	Indicates if the implementation can support ATB triggers: 0 The implementation does not support ATB triggers. 1 The implementation supports ATB triggers, and the TRCEVENTCTL1R.ATBTRIG field is implemented.
21:16	TRACEIDSIZE	R/W	7h	Indicates the trace ID width. The permitted value is: 111 The implementation supports a 7-bit trace ID. This sets the width of the TRCTRACEIDR.TRACEID field. All other values are reserved.The CoreSight ATB requires a 7-bit trace ID width.
15:12	RES0_TRCIDR5_15_12	R/W	0h	Reserved, RES0.
11:9	NUMEXTINSEL	R/W	4h	Indicates how many external input select resources are implemented. The permitted values are: 000 No external input select resources are available. If NUMEXTINSEL is zero, NUMEXTIN must also be zero. 001 The implementation has one external input select resource. 010 The implementation has two external input select resources. 011 The implementation has three external input select resources. 100 The implementation has four external input select resources. All other values are reserved.See TRCEXTINSELR for how to select an input select resource.
8:0	NUMEXTIN	R/W	1Eh	Indicates how many external inputs are implemented. The permitted values are: 000000000 No external inputs are available. If NUMEXTIN is zero, NUMEXTINSEL must also be zero. 000000001 The implementation has one external input. 000000010 The implementation has two external inputs. and so on up to 0b100000000, which indicates that the implementation has 256 external inputs.All other values >0b100000000 are reserved.See TRCEXTINSELR for how to select an external input.

14.3.1.1.2.541 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR2 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR2 Register (Offset = 208h) [reset = 0h]

Resource Selection Control Registers 2

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Table 14-9305. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0208h**

Figure 14-3086. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR2_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR2_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9307. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR2_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9307. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.542 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR3 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR3 Register (Offset = 20Ch) [reset = 0h]

Resource Selection Control Registers 3

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Table 14-9308. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 020Ch**

Figure 14-3087. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR3_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR3_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9310. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR3_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9310. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.543 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR4 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR4 Register (Offset = 210h) [reset = 0h]

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Table 14-9311. Instance Table

Instance Name	**Physical Address**
A53SS0	**0007 3013 0210h**

Figure 14-3088. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR4_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR4_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-9313. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR4_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9313. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.544 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR5 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR5 Register (Offset = 214h) [reset = 0h]

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Table 14-9314. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0214h**

Figure 14-3089. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR5_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR5_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-9316. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR5_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9316. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.545 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR6 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR6 Register (Offset = 218h) [reset = 0h]

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Table 14-9317. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0218h**

Figure 14-3090. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR6_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR6_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-9319. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR6_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9319. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.546 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR7 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR7 Register (Offset = 21Ch) [reset = 0h]

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Table 14-9320. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 021Ch**

Figure 14-3091. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR7_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR7_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-9322. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR7_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9322. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.547 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR8 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR8 Register (Offset = 220h) [reset = 0h]

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Table 14-9323. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0220h**

Figure 14-3092. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR8 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR8_31_22							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_TRCRSCTLR8_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							

7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-9325. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR8_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9325. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.548 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR9 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR9 Register (Offset = 224h) [reset = 0h]

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Table 14-9326. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0224h**

Figure 14-3093. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR9 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR9_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR9_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-9328. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR9_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9328. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.549 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR10 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR10 Register (Offset = 228h) [reset = 0h]

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Table 14-9329. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0228h**

Figure 14-3094. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR10 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR10_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR10_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-9331. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR10_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9331. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.550 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR11 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR11 Register (Offset = 22Ch) [reset = 0h]

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Table 14-9332. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 022Ch**

Figure 14-3095. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR11 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR11_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR11_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-9334. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR11_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9334. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.551 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR12 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR12 Register (Offset = 230h) [reset = 0h]

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Table 14-9335. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0230h**

Figure 14-3096. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR12 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR12_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCRSCTLR12_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							
7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-9337. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR12_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9337. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.552 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR13 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR13 Register (Offset = 234h) [reset = 0h]

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Table 14-9338. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0234h**

Figure 14-3097. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCRSCTLR13_31_22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RES0_TRCRSCTLR13_31_22</td><td>PAIRINV</td><td>INV</td><td colspan="4">GROUP</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SELECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9340. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR13_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9340. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.553 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR14 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR14 Register (Offset = 238h) [reset = 0h]

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Table 14-9341. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0238h**

Figure 14-3098. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR14 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR14_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCRSCTLR14_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT							
R/W							
0h							

Table 14-9343. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR14_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9343. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.554 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR15 Register

1 A53SS_APBADDR_ETM_CPU1_TRCRSCTLR15 Register (Offset = 23Ch) [reset = 0h]

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Table 14-9344. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 023Ch**

Figure 14-3099. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR15 Name Register

31	30	29	28	27	26	25	24
RES0_TRCRSCTLR15_31_22							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_TRCRSCTLR15_31_22		PAIRINV	INV	GROUP			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			

15	14	13	12	11	10	9	8
SELECT							
R/W							
0h							

7	6	5	4	3	2	1	0
SELECT							
R/W							
0h							

Table 14-9346. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCRSCTLR15_31_22	R/W	0h	Reserved, RES0.
21	PAIRINV	R/W	0h	If n is an even number, controls whether the combined result from a resource pair is inverted: 0 The combined result is not inverted. 1 The combined result is inverted. If n is an odd number, this field is RES0.
20	INV	R/W	0h	Controls whether the resource that GROUP and SELECT selects is inverted: 0 The selected resource is not inverted. 1 The selected resource is inverted.

Table 14-9346. A53SS_APBADDR_ETM_CPU1_TRCRSCTLR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	GROUP	R/W	0h	Selects a group of resources. Possible values are: 0000 For SELECT bits 0 to 3, selects external input selector 0 to 3; other bits are reserved. 0001 For SELECT bits 0 to 7, selects processor comparator inputs 0 to 7; other bits are reserved. 0010 For SELECT bits 0 to 3, selects counter at zero 0 to 3; for SELECT bits 4 to 7, selects sequencer states 0 to 3; other bits are reserved. 0011 For SELECT bits 0 to 7, selects single-shot comparator control 0 to 7; other bits are reserved. 0100 For SELECT bits 0 to 15, selects single address comparator 0 to 15. 0101 For SELECT bits 0 to 7, selects address range comparator 0 to 7; other bits are reserved. 0110 For SELECT bits 0 to 7, selects Context ID comparator 0 to 7; other bits are reserved. 0111 For SELECT bits 0 to 7, selects VMID comparator 0 to 7; other bits are reserved. All other values are reserved.
15:0	SELECT	R/W	0h	Selects one or more resources from the group that the GROUP field selects. Each bit represents a resource from the selected group.See the GROUP field description for details.

14.3.1.1.2.555 A53SS_APBADDR_ETM_CPU1_TRCSSCCR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCSSCCR0 Register (Offset = 280h) [reset = 0h]

Single-Shot Comparator Control Register 0

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Table 14-9347. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0280h**

Figure 14-3100. A53SS_APBADDR_ETM_CPU1_TRCSSCCR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RES0_TRCSSCCR0_31_25</td><td>RST</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ARC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9349. A53SS_APBADDR_ETM_CPU1_TRCSSCCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RES0_TRCSSCCR0_31_25	R/W	0h	Reserved, RES0.
24	RST	R/W	0h	Controls whether the single-shot comparator resource is reset when it fires. 0 When the single-shot comparator resource fires, it is not reset. 1 When the single-shot comparator resource fires, it is reset. This enables the single-shot comparator resource to fire multiple times.
23:16	ARC	R/W	0h	Selects one or more address range comparators for single-shot control.Each bit represents an address range comparator pair, so bit[n-16] controls the selection of address range comparator pair n-16. If bit[n-16] is: 0 The address range comparator pair n-16 is not selected for single-shot control. 1 The address range comparator pair n-16 is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

Table 14-9349. A53SS_APBADDR_ETM_CPU1_TRCSSCCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SAC	R/W	0h	Selects one or more single address comparators for single-shot control.Each bit represents a single address comparator, so bit[n] controls the selection of single address comparator n. If bit[n] is: 0 The single address comparator n, is not selected for single-shot control. 1 The single address comparator n, is selected for single-shot control. The width of this field is IMPLEMENTATION DEFINED. The field contains a number of implemented bits equal to 2 x TRCIDR4.NUMACPAIRS. Unimplemented bits are RAZ/WI.

14.3.1.1.2.556 A53SS_APBADDR_ETM_CPU1_TRCSSCSR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCSSCSR0 Register (Offset = 2A0h) [reset = 1h]

Single-Shot Comparator Status Register 0

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Table 14-9350. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 02A0h**

Figure 14-3101. A53SS_APBADDR_ETM_CPU1_TRCSSCSR0 Name Register

31	30	29	28	27	26	25	24
STATUS	RES0_TRCSSCSR0_30_3						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RES0_TRCSSCSR0_30_3							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCSSCSR0_30_3							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCSSCSR0_30_3					DV	DA	INST
R/W					R/W	R/W	R/W
0h					0h	0h	1h

Table 14-9352. A53SS_APBADDR_ETM_CPU1_TRCSSCSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	STATUS	R/W	0h	Single-shot status bit. Indicates if any of the comparators that TRCSSCCRn.SAC or TRCSSCCRn.ARC selects have matched: 0 No match has occurred. 1 One or more matches has occurred. If TRCSSCCRn.RST==0 then there is only one match and no more matches are possible, and software must reset this bit to 0 to re-enable the single-shot control. STATUS must be written to set an initial state when configuring the trace unit, if the single-shot comparator is to be used.
30:3	RES0_TRCSSCSR0_30_3	R/W	0h	Reserved, RES0.
2	DV	R/W	0h	Data value comparator support bit. Indicates if the trace unit supports data address with data value comparisons: 0 Single-shot data address with data value comparisons are not supported. 1 Single-shot data address with data value comparisons are supported.

Table 14-9352. A53SS_APBADDR_ETM_CPU1_TRCSSCSR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DA	R/W	0h	Data address comparator support bit. Indicates if the trace unit supports data address comparisons: 0 Single-shot data address comparisons are not supported. 1 Single-shot data address comparisons are supported.
0	INST	R/W	1h	Instruction address comparator support bit. Indicates if the trace unit supports instruction address comparisons: 0 Single-shot instruction address comparisons are not supported. 1 Single-shot instruction address comparisons are supported.

14.3.1.1.2.557 A53SS_APBADDR_ETM_CPU1_TRCOSLAR Register

1 A53SS_APBADDR_ETM_CPU1_TRCOSLAR Register (Offset = 300h) [reset = 0h]

OS Lock Access Register

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Table 14-9353. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0300h**

Figure 14-3102. A53SS_APBADDR_ETM_CPU1_TRCOSLAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLAR_31_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCOSLAR_31_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCOSLAR_31_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCOSLAR_31_1							LOCK
R/W							R/W
0h							0h

Table 14-9355. A53SS_APBADDR_ETM_CPU1_TRCOSLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCOSLAR_31_1	R/W	0h	Reserved, RES0.
0	LOCK	R/W	0h	OS Lock control bit: 0 Unlocks the OS Lock. 1 Locks the OS Lock. This setting disables the trace unit.

14.3.1.1.2.558 A53SS_APBADDR_ETM_CPU1_TRCOSLSR Register

1 A53SS_APBADDR_ETM_CPU1_TRCOSLSR Register (Offset = 304h) [reset = Ah]

OS Lock Status Register

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Table 14-9356. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0304h**

Figure 14-3103. A53SS_APBADDR_ETM_CPU1_TRCOSLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCOSLSR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCOSLSR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCOSLSR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCOSLSR_31_4				PRESENT	BIT32	LOCKED	RES0_TRCOSLSR_0_0
R/W				R/W	R/W	R/W	R/W
0h				1h	0h	1h	0h

Table 14-9358. A53SS_APBADDR_ETM_CPU1_TRCOSLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCOSLSR_31_4	R/W	0h	Reserved, RES0.
3	PRESENT	R/W	1h	Indicates whether the OS Lock is implemented.This bit is RES1, which indicates that the OS Lock is always implemented.
2	BIT32	R/W	0h	This bit is RES0, which indicates that software must perform a 32-bit write to update the TRCOSLAR.
1	LOCKED	R/W	1h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. When the trace unit core power domain is powered down the value is UNKNOWN. The TRCPDSR indicates if the trace unit core power domain is powered down.
0	RES0_TRCOSLSR_0_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.559 A53SS_APBADDR_ETM_CPU1_TRCPDCR Register

1 A53SS_APBADDR_ETM_CPU1_TRCPDCR Register (Offset = 310h) [reset = 0h]

Power Down Control Register

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Table 14-9359. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0310h**

Figure 14-3104. A53SS_APBADDR_ETM_CPU1_TRCPDCR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDCR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPDCR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPDCR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPDCR_31_4				PU	RES0_TRCPDCR_2_0		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-9361. A53SS_APBADDR_ETM_CPU1_TRCPDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_TRCPDCR_31_4	R/W	0h	Reserved, RES0.
3	PU	R/W	0h	Powerup request bit: 0 The system can remove power from the trace unit. The TRCPDSR indicates if the trace unit is powered down. 1 The system must provide power to the trace unit. Typically, a trace unit drives a signal representing the value of this bit to a power controller to request that the trace unit core power domain is powered up. However, if the trace unit and the processor are in the same power domain then the implementation might combine the PU status with a signal from the processor.
2:0	RES0_TRCPDCR_2_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.560 A53SS_APBADDR_ETM_CPU1_TRCPDSR Register

1 A53SS_APBADDR_ETM_CPU1_TRCPDSR Register (Offset = 314h) [reset = 0h]

Power Down Status Register

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Table 14-9362. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0314h**

Figure 14-3105. A53SS_APBADDR_ETM_CPU1_TRCPDSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCPDSR_31_6							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPDSR_31_6							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPDSR_31_6							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCPDSR_31_6		LOCKED	RES0_TRCPDSR_4_2			STICKYPD	POWER
R/W		R/W	R/W			R/W	R/W
0h		0h	0h			0h	0h

Table 14-9364. A53SS_APBADDR_ETM_CPU1_TRCPDSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RES0_TRCPDSR_31_6	R/W	0h	Reserved, RES0.
5	LOCKED	R/W	0h	OS Lock status bit: 0 The OS Lock is unlocked. 1 The OS Lock is locked. The value is UNKNOWN when the trace unit core power domain is powered down, that is, when POWER==0.
4:2	RES0_TRCPDSR_4_2	R/W	0h	Reserved, RES0.
1	STICKYPD	R/W	0h	Sticky powerdown status bit. Indicates whether the trace register state is valid: 0 If POWER==1 then the state of TRCOSLSR and the trace registers are valid. If POWER==0 then it is UNKNOWN whether the state of TRCOSLSR and the trace registers are valid. 1 The state of TRCOSLSR and the trace registers might not be valid. The trace unit sets this bit to 1 if either the trace unit is reset, or the power to the trace unit core power domain is removed and the trace register state is not valid. After this register is read, if the Software Lock is unlocked and the trace unit core power domain is powered up, then the trace unit sets this bit to 0. The TRCLAR controls whether the Software Lock is locked.

Table 14-9364. A53SS_APBADDR_ETM_CPU1_TRCPDSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POWER	R/W	0h	Power status bit: 0 The trace unit core power domain is not powered. The trace registers are not accessible and they all return an error response. 1 The trace unit core power domain is powered. The trace registers are accessible.

14.3.1.1.2.561 A53SS_APBADDR_ETM_CPU1_TRCACVR0_31_0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR0_31_0 Register (Offset = 400h) [reset = 0h]

Address Comparator Value Registers 0 (low word)

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Table 14-9365. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0400h**

Figure 14-3106. A53SS_APBADDR_ETM_CPU1_TRCACVR0_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9367. A53SS_APBADDR_ETM_CPU1_TRCACVR0_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.562 A53SS_APBADDR_ETM_CPU1_TRCACVR0_63_32 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR0_63_32 Register (Offset = 404h) [reset = 0h]

Address Comparator Value Registers 0 (high word)

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Table 14-9368. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0404h**

Figure 14-3107. A53SS_APBADDR_ETM_CPU1_TRCACVR0_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9370. A53SS_APBADDR_ETM_CPU1_TRCACVR0_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.563 A53SS_APBADDR_ETM_CPU1_TRCACVR1_31_0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR1_31_0 Register (Offset = 408h) [reset = 0h]

Address Comparator Value Registers 1 (low word)

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Table 14-9371. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0408h**

Figure 14-3108. A53SS_APBADDR_ETM_CPU1_TRCACVR1_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9373. A53SS_APBADDR_ETM_CPU1_TRCACVR1_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.564 A53SS_APBADDR_ETM_CPU1_TRCACVR1_63_32 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR1_63_32 Register (Offset = 40Ch) [reset = 0h]

Address Comparator Value Registers 1 (high word)

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Table 14-9374. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 040Ch**

Figure 14-3109. A53SS_APBADDR_ETM_CPU1_TRCACVR1_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9376. A53SS_APBADDR_ETM_CPU1_TRCACVR1_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.565 A53SS_APBADDR_ETM_CPU1_TRCACVR2_31_0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR2_31_0 Register (Offset = 410h) [reset = 0h]

Address Comparator Value Registers 2 (low word)

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Table 14-9377. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0410h**

Figure 14-3110. A53SS_APBADDR_ETM_CPU1_TRCACVR2_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9379. A53SS_APBADDR_ETM_CPU1_TRCACVR2_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.566 A53SS_APBADDR_ETM_CPU1_TRCACVR2_63_32 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR2_63_32 Register (Offset = 414h) [reset = 0h]

Address Comparator Value Registers 2 (high word)

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Table 14-9380. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0414h**

Figure 14-3111. A53SS_APBADDR_ETM_CPU1_TRCACVR2_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9382. A53SS_APBADDR_ETM_CPU1_TRCACVR2_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.567 A53SS_APBADDR_ETM_CPU1_TRCACVR3_31_0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR3_31_0 Register (Offset = 418h) [reset = 0h]

Address Comparator Value Registers 3 (low word)

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Table 14-9383. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0418h**

Figure 14-3112. A53SS_APBADDR_ETM_CPU1_TRCACVR3_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9385. A53SS_APBADDR_ETM_CPU1_TRCACVR3_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.568 A53SS_APBADDR_ETM_CPU1_TRCACVR3_63_32 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR3_63_32 Register (Offset = 41Ch) [reset = 0h]

Address Comparator Value Registers 3 (high word)

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Table 14-9386. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 041Ch**

Figure 14-3113. A53SS_APBADDR_ETM_CPU1_TRCACVR3_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9388. A53SS_APBADDR_ETM_CPU1_TRCACVR3_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.569 A53SS_APBADDR_ETM_CPU1_TRCACVR4_31_0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR4_31_0 Register (Offset = 420h) [reset = 0h]

Address Comparator Value Registers 4 (low word)

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Table 14-9389. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0420h**

Figure 14-3114. A53SS_APBADDR_ETM_CPU1_TRCACVR4_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9391. A53SS_APBADDR_ETM_CPU1_TRCACVR4_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.570 A53SS_APBADDR_ETM_CPU1_TRCACVR4_63_32 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR4_63_32 Register (Offset = 424h) [reset = 0h]

Address Comparator Value Registers 4 (high word)

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Table 14-9392. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0424h**

Figure 14-3115. A53SS_APBADDR_ETM_CPU1_TRCACVR4_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9394. A53SS_APBADDR_ETM_CPU1_TRCACVR4_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.571 A53SS_APBADDR_ETM_CPU1_TRCACVR5_31_0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR5_31_0 Register (Offset = 428h) [reset = 0h]

Address Comparator Value Registers 5 (low word)

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Table 14-9395. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0428h**

Figure 14-3116. A53SS_APBADDR_ETM_CPU1_TRCACVR5_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9397. A53SS_APBADDR_ETM_CPU1_TRCACVR5_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.572 A53SS_APBADDR_ETM_CPU1_TRCACVR5_63_32 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR5_63_32 Register (Offset = 42Ch) [reset = 0h]

Address Comparator Value Registers 5 (high word)

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Table 14-9398. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 042Ch**

Figure 14-3117. A53SS_APBADDR_ETM_CPU1_TRCACVR5_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9400. A53SS_APBADDR_ETM_CPU1_TRCACVR5_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.573 A53SS_APBADDR_ETM_CPU1_TRCACVR6_31_0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR6_31_0 Register (Offset = 430h) [reset = 0h]

Address Comparator Value Registers 6 (low word)

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Table 14-9401. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0430h**

Figure 14-3118. A53SS_APBADDR_ETM_CPU1_TRCACVR6_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9403. A53SS_APBADDR_ETM_CPU1_TRCACVR6_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.574 A53SS_APBADDR_ETM_CPU1_TRCACVR6_63_32 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR6_63_32 Register (Offset = 434h) [reset = 0h]

Address Comparator Value Registers 6 (high word)

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Table 14-9404. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0434h**

Figure 14-3119. A53SS_APBADDR_ETM_CPU1_TRCACVR6_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9406. A53SS_APBADDR_ETM_CPU1_TRCACVR6_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.575 A53SS_APBADDR_ETM_CPU1_TRCACVR7_31_0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR7_31_0 Register (Offset = 438h) [reset = 0h]

Address Comparator Value Registers 7 (low word)

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Table 14-9407. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0438h**

Figure 14-3120. A53SS_APBADDR_ETM_CPU1_TRCACVR7_31_0 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9409. A53SS_APBADDR_ETM_CPU1_TRCACVR7_31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.576 A53SS_APBADDR_ETM_CPU1_TRCACVR7_63_32 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACVR7_63_32 Register (Offset = 43Ch) [reset = 0h]

Address Comparator Value Registers 7 (high word)

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Table 14-9410. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 043Ch**

Figure 14-3121. A53SS_APBADDR_ETM_CPU1_TRCACVR7_63_32 Name Register

31	30	29	28	27	26	25	24
ADDRESS							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-9412. A53SS_APBADDR_ETM_CPU1_TRCACVR7_63_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDRESS	R/W	0h	Address value.The address comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then it must ignore those upper bits in the comparison. For example, in a system that supports both 32-bit and 64-bit addresses, when the processor is in 32-bit state the comparator must ignore the ADDRESS[63_32] bits.

14.3.1.1.2.577 A53SS_APBADDR_ETM_CPU1_TRCACATR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACATR0 Register (Offset = 480h) [reset = 0h]

Address Comparator Access Type Registers 0

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Table 14-9413. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0480h**

Figure 14-3122. A53SS_APBADDR_ETM_CPU1_TRCACATR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR0_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR0_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR0_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-9415. A53SS_APBADDR_ETM_CPU1_TRCACATR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR0_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-9415. A53SS_APBADDR_ETM_CPU1_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-9415. A53SS_APBADDR_ETM_CPU1_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR0_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-9415. A53SS_APBADDR_ETM_CPU1_TRCACATR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.578 A53SS_APBADDR_ETM_CPU1_TRCACATR1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACATR1 Register (Offset = 488h) [reset = 0h]

Address Comparator Access Type Registers 1

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Table 14-9416. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0488h**

Figure 14-3123. A53SS_APBADDR_ETM_CPU1_TRCACATR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR1_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR1_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR1_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-9418. A53SS_APBADDR_ETM_CPU1_TRCACATR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR1_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-9418. A53SS_APBADDR_ETM_CPU1_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-9418. A53SS_APBADDR_ETM_CPU1_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR1_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-9418. A53SS_APBADDR_ETM_CPU1_TRCACATR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.579 A53SS_APBADDR_ETM_CPU1_TRCACATR2 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACATR2 Register (Offset = 490h) [reset = 0h]

Address Comparator Access Type Registers 2

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Table 14-9419. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0490h**

Figure 14-3124. A53SS_APBADDR_ETM_CPU1_TRCACATR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR2_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR2_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR2_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-9421. A53SS_APBADDR_ETM_CPU1_TRCACATR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR2_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-9421. A53SS_APBADDR_ETM_CPU1_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-9421. A53SS_APBADDR_ETM_CPU1_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR2_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-9421. A53SS_APBADDR_ETM_CPU1_TRCACATR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.580 A53SS_APBADDR_ETM_CPU1_TRCACATR3 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACATR3 Register (Offset = 498h) [reset = 0h]

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Table 14-9422. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0498h**

Figure 14-3125. A53SS_APBADDR_ETM_CPU1_TRCACATR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR3_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR3_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR3_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-9424. A53SS_APBADDR_ETM_CPU1_TRCACATR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR3_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-9424. A53SS_APBADDR_ETM_CPU1_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-9424. A53SS_APBADDR_ETM_CPU1_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR3_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-9424. A53SS_APBADDR_ETM_CPU1_TRCACATR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.581 A53SS_APBADDR_ETM_CPU1_TRCACATR4 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACATR4 Register (Offset = 4A0h) [reset = 0h]

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Table 14-9425. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 04A0h**

Figure 14-3126. A53SS_APBADDR_ETM_CPU1_TRCACATR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR4_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR4_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR4_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-9427. A53SS_APBADDR_ETM_CPU1_TRCACATR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR4_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-9427. A53SS_APBADDR_ETM_CPU1_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-9427. A53SS_APBADDR_ETM_CPU1_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR4_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-9427. A53SS_APBADDR_ETM_CPU1_TRCACATR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.582 A53SS_APBADDR_ETM_CPU1_TRCACATR5 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACATR5 Register (Offset = 4A8h) [reset = 0h]

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Table 14-9428. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 04A8h**

Figure 14-3127. A53SS_APBADDR_ETM_CPU1_TRCACATR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR5_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR5_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR5_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-9430. A53SS_APBADDR_ETM_CPU1_TRCACATR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR5_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-9430. A53SS_APBADDR_ETM_CPU1_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-9430. A53SS_APBADDR_ETM_CPU1_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR5_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-9430. A53SS_APBADDR_ETM_CPU1_TRCACATR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.583 A53SS_APBADDR_ETM_CPU1_TRCACATR6 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACATR6 Register (Offset = 4B0h) [reset = 0h]

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Table 14-9431. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 04B0h**

Figure 14-3128. A53SS_APBADDR_ETM_CPU1_TRCACATR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR6_31_22							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCACATR6_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	14	13	12	11	10	9	8
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RES0_TRCACATR6_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-9433. A53SS_APBADDR_ETM_CPU1_TRCACATR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR6_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-9433. A53SS_APBADDR_ETM_CPU1_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-9433. A53SS_APBADDR_ETM_CPU1_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR6_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-9433. A53SS_APBADDR_ETM_CPU1_TRCACATR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.584 A53SS_APBADDR_ETM_CPU1_TRCACATR7 Register

1 A53SS_APBADDR_ETM_CPU1_TRCACATR7 Register (Offset = 4B8h) [reset = 0h]

Address Comparator Access Type Registers 7

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Table 14-9434. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 04B8h**

Figure 14-3129. A53SS_APBADDR_ETM_CPU1_TRCACATR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCACATR7_31_22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCACATR7_31_22		DTBM	DATARANGE	DATASIZE		DATAMATCH	
R/W		R/W	R/W	R/W		R/W	
0h		0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXLEVEL_NS				EXLEVEL_S			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCACATR7_7_7	CONTEXT			CONTEXTTYPE		TYPE	
R/W	R/W			R/W		R/W	
0h	0h			0h		0h	

Table 14-9436. A53SS_APBADDR_ETM_CPU1_TRCACATR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RES0_TRCACATR7_31_22	R/W	0h	Reserved, RES0.
21	DTBM	R/W	0h	Controls whether data address comparisons use the data address [63:56] bits: 0 The trace unit ignores the data address [63:56] bits for data address comparisons. 1 The trace unit uses the data address [63:56] bits for data address comparisons. Supported only if TRCIDR2.DASIZE indicates that the data address size is 64 bits, otherwise this bit is RES0.

Table 14-9436. A53SS_APBADDR_ETM_CPU1_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DATARANGE	R/W	0h	Controls whether a data value comparison uses the single address comparator or the address range comparator: 0 The trace unit uses the single address comparator for data value comparisons. The behavior of the address range comparator is UNPREDICTABLE. 1 The trace unit uses the address range comparator for data value comparisons. The behavior of the single address comparators in this pair is UNPREDICTABLE. The trace unit ignores this field when DATAMATCH==0b00.Supported only if the corresponding data value comparator is supported, otherwise this bit is RES0.
19:18	DATASIZE	R/W	0h	Controls the width of the data value comparison: 00 Byte. 01 Halfword. 10 Word. 11 Doubleword. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.The doubleword width is supported only if TRCIDR2.DVSIZE indicates that 64-bit values are supported. If 64-bit values are not supported, 0b11 is reserved.
17:16	DATAMATCH	R/W	0h	Controls how the trace unit performs a data value comparison: 00 The trace unit does not perform a data value comparison. 01 The trace unit performs a data value comparison and signals a match if both values are identical. 10 Reserved. 11 The trace unit performs a data value comparison and signals a match if both values are different. Supported only if the corresponding data value comparator is supported, otherwise this field is RES0.
15:12	EXLEVEL_NS	R/W	0h	In Non-secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Non-secure state, for exception level n. 1 The trace unit does not perform a comparison, in Non-secure state, for exception level n. The exception levels are:Bit[12]Exception level 0.Bit[13]Exception level 1.Bit[14]Exception level 2.Bit[15]RAZ/WI. EXLEVEL_NS[3] is never implemented.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_NS. Unimplemented bits are RAZ/WI.

Table 14-9436. A53SS_APBADDR_ETM_CPU1_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	EXLEVEL_S	R/W	0h	In Secure state, each bit controls whether a comparison can occur for the corresponding exception level: 0 The trace unit can perform a comparison, in Secure state, for exception level n. 1 The trace unit does not perform a comparison, in Secure state, for exception level n. The exception levels are:Bit[8]Exception level 0.Bit[9]Exception level 1.Bit[10]RAZ/WI. EXLEVEL_S[2] is never implemented.Bit[11]Exception level 3.The content of the field is IMPLEMENTATION DEFINED and is set by the value of TRCIDR3.EXLEVEL_S. Unimplemented bits are RAZ/WI.
7	RES0_TRCACATR7_7_7	R/W	0h	Reserved, RES0.
6:4	CONTEXT	R/W	0h	If TRCIDR4.NUMCIDFC > 0 or TRCIDR4.NUMVMIDC > 0, selects a Context ID comparator or VMID comparator: 000 Comparator 0. 001 Comparator 1. 010 Comparator 2. and so on up to 0b111, which indicates comparator 7.The implemented width of this field is determined by the size of whichever of TRCIDR4.NUMVMIDC and TRCIDR4.NUMCIDC is larger. If the largest field is one bit long, then this field implements one bit, bit[4]. If the largest field is four bits long, then this field implements two bits, bits[5:4]. Unimplemented bits within the field are RAZ/WI.If TRCIDR4.NUMCIDFC==0 and TRCIDR4.NUMVMIDC==0, this field is RES0.
3:2	CONTEXTTYPE	R/W	0h	If TRCIDR4.NUMVMIDC>0 and TRCIDR4.NUMCIDC>0, this field controls whether the trace unit performs a Context ID comparison, a virtual machine identifier [VMID] comparison, or both comparisons: 00 The trace unit does not perform a Context ID or VMID comparison. 01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match. 10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match. 11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches. If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC>0, bit [3] is RES0 and bit[2] controls whether the trace unit performs a Context ID comparison, as with cases 0b00 and 0b01 above.If TRCIDR4.NUMVMIDC==0 and TRCIDR4.NUMCIDC==0, both bits are RES0.

Table 14-9436. A53SS_APBADDR_ETM_CPU1_TRCACATR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TYPE	R/W	0h	Controls what type of comparison the trace unit performs: 00 Instruction address. 01 Data load address. 10 Data store address. 11 Data load address or data store address. If TRCIDR4.SUPPDAC does not indicate that data address comparisons are implemented, then this field is RES0. This means that any comparison performed by this address comparator is an instruction address comparison.

14.3.1.1.2.585 A53SS_APBADDR_ETM_CPU1_TRCCIDCVR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCIDCVR0 Register (Offset = 600h) [reset = 0h]

Context ID Comparator Value Register 0

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Table 14-9437. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0600h**

Figure 14-3130. A53SS_APBADDR_ETM_CPU1_TRCCIDCVR0 Name Register

31	30	29	28	27	26	25	24
VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-9439. A53SS_APBADDR_ETM_CPU1_TRCCIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE	R/W	0h	Context ID value. The implemented width of this field is IMPLEMENTATION DEFINED and is set by TRCIDR2.CIDSIZE. Unimplemented bits are RAZ/WI.After a processor reset, the ETM architecture assumes that the Context ID is zero until the processor updates the Context ID.

14.3.1.1.2.586 A53SS_APBADDR_ETM_CPU1_TRCVMIDCVR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCVMIDCVR0 Register (Offset = 640h) [reset = 0h]

VMID Comparator Value Register 0

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Table 14-9440. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0640h**

Figure 14-3131. A53SS_APBADDR_ETM_CPU1_TRCVMIDCVR0 Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCVMIDCVR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-9442. A53SS_APBADDR_ETM_CPU1_TRCVMIDCVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_TRCVMIDCVR0_31_8	R/W	0h	Reserved RES0
7:0	VALUE	R/W	0h	Contains a VMID value.

14.3.1.1.2.587 A53SS_APBADDR_ETM_CPU1_TRCCIDCCTLR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCIDCCTLR0 Register (Offset = 680h) [reset = 0h]

Context ID Comparator Control Register 0

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Table 14-9443. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0680h**

Figure 14-3132. A53SS_APBADDR_ETM_CPU1_TRCCIDCCTLR0 Name Register

31	30	29	28	27	26	25	24
COMP_N							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_N							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_N							
R/W							
0h							

Table 14-9445. A53SS_APBADDR_ETM_CPU1_TRCCIDCCTLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_N	R/W	0h	Controls the mask value that the trace unit applies to TRCCIDCVRn. Each bit in this field corresponds to a byte in TRCCIDCVRn. When a bit is: 0 The trace unit includes the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. 1 The trace unit ignores the relevant byte in TRCCIDCVRn when it performs the Context ID comparison. Supported only if TRCIDR4.NUMCIDC > n, otherwise the field is RES0.

14.3.1.1.2.588 A53SS_APBADDR_ETM_CPU1_TRCITATBIDR Register

1 A53SS_APBADDR_ETM_CPU1_TRCITATBIDR Register (Offset = EE4h) [reset = 0h]

Integration ATB Identification Register

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Table 14-9446. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0EE4h**

Figure 14-3133. A53SS_APBADDR_ETM_CPU1_TRCITATBIDR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITATBIDR_31_7							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITATBIDR_31_7							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITATBIDR_31_7							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITATBIDR_31_7	ID						
R/W	R/W						
0h	0h						

Table 14-9448. A53SS_APBADDR_ETM_CPU1_TRCITATBIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES0_TRCITATBIDR_31_7	R/W	0h	Reserved RES0
6:0	ID	R/W	0h	Drives the ATIDMn[6:0] output pins

14.3.1.1.2.589 A53SS_APBADDR_ETM_CPU1_TRCITIDATAR Register

1 A53SS_APBADDR_ETM_CPU1_TRCITIDATAR Register (Offset = EECh) [reset = 0h]

Integration Instruction ATB Data Register

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Table 14-9449. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0EECh**

Figure 14-3134. A53SS_APBADDR_ETM_CPU1_TRCITIDATAR Name Register

31	30	29	28	27	26	25	24
RES0_TRCITIDATAR_31_5							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCITIDATAR_31_5							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCITIDATAR_31_5							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_TRCITIDATAR_31_5			ATDATAM_31	ATDATAM_23	ATDATAM_15	ATDATAM_7	ATDATAM_0
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-9451. A53SS_APBADDR_ETM_CPU1_TRCITIDATAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RES0_TRCITIDATAR_31_5	R/W	0h	Reserved RES0
4	ATDATAM_31	R/W	0h	Drives the ATDATAM[31] output
3	ATDATAM_23	R/W	0h	Drives the ATDATAM[23] output
2	ATDATAM_15	R/W	0h	Drives the ATDATAM[15] output
1	ATDATAM_7	R/W	0h	Drives the ATDATAM[7] output
0	ATDATAM_0	R/W	0h	Drives the ATDATAM[0] output

14.3.1.1.2.590 A53SS_APBADDR_ETM_CPU1_TRCITIATBINR Register

1 A53SS_APBADDR_ETM_CPU1_TRCITIATBINR Register (Offset = EF4h) [reset = 0h]

Integration Instruction ATB In Register

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Table 14-9452. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0EF4h**

Figure 14-3135. A53SS_APBADDR_ETM_CPU1_TRCITIATBINR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCITIATBINR_31_2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCITIATBINR_31_2						AFVALIDM	ATREADYM
R/W						R/W	R/W
0h						0h	0h

Table 14-9454. A53SS_APBADDR_ETM_CPU1_TRCITIATBINR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_TRCITIATBINR_31_2	R/W	0h	Reserved. Read undefined.
1	AFVALIDM	R/W	0h	Returns the value of the AFVALIDMn input pin
0	ATREADYM	R/W	0h	Returns the value of the ATREADYMn input pin

14.3.1.1.2.591 A53SS_APBADDR_ETM_CPU1_TRCITIATBOUTR Register

1 A53SS_APBADDR_ETM_CPU1_TRCITIATBOUTR Register (Offset = EFCh) [reset = 0h]

Integration Instruction ATB Out Register

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Table 14-9455. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0EFCh**

Figure 14-3136. A53SS_APBADDR_ETM_CPU1_TRCITIATBOUTR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_TRCITIATBOUTR_31_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_TRCITIATBOUTR_31_10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_TRCITIATBOUTR_31_10</td><td colspan="2">BYTES</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED_TRCITIATBOUTR_7_2</td><td>AFREADY</td><td>ATVALID</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9457. A53SS_APBADDR_ETM_CPU1_TRCITIATBOUTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_TRCITIATBOUTR_31_10	R/W	0h	Reserved. Read undefined.
9:8	BYTES	R/W	0h	Drives the ATBYTESMn[1:0] output pins
7:2	RESERVED_TRCITIATBOUTR_7_2	R/W	0h	Reserved. Read undefined.
1	AFREADY	R/W	0h	Drives the AFREADYMn output pin
0	ATVALID	R/W	0h	Drives the ATVALIDMn output pin

14.3.1.1.2.592 A53SS_APBADDR_ETM_CPU1_TRCITCTRL Register

1 A53SS_APBADDR_ETM_CPU1_TRCITCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Control Register

Return to Summary Table

Table 14-9458. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0F00h**

Figure 14-3137. A53SS_APBADDR_ETM_CPU1_TRCITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_TRCITCTRL_31_1</td><td>ITEN</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9460. A53SS_APBADDR_ETM_CPU1_TRCITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_TRCITCTRL_31_1	R/W	0h	Reserved, RES0.
0	ITEN	R/W	0h	Integration mode enable bit: 0 The trace unit is not in integration mode. 1 The trace unit is in integration mode. This mode enables a debug agent to perform topology detection, and System-on-Chip [SoC] test software to perform integration testing.

14.3.1.1.2.593 A53SS_APBADDR_ETM_CPU1_TRCCLAIMSET Register

1 A53SS_APBADDR_ETM_CPU1_TRCCLAIMSET Register (Offset = FA0h) [reset = Fh]

Claim Tag Set Register

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Table 14-9461. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FA0h**

Figure 14-3138. A53SS_APBADDR_ETM_CPU1_TRCCLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_TRCCLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCCLAIMSET_31_4				SET			
R/W				R/W			
0h				Fh			

Table 14-9463. A53SS_APBADDR_ETM_CPU1_TRCCLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	SET	R/W	Fh	Sets bits in the claim tag and determines the number of claim tag bits implemented.

14.3.1.1.2.594 A53SS_APBADDR_ETM_CPU1_TRCCLAIMCLR Register

1 A53SS_APBADDR_ETM_CPU1_TRCCLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

Return to Summary Table

Table 14-9464. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FA4h**

Figure 14-3139. A53SS_APBADDR_ETM_CPU1_TRCCLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_TRCCLAIMCLR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCCLAIMCLR_31_4				CLR			
R/W				R/W			
0h				0h			

Table 14-9466. A53SS_APBADDR_ETM_CPU1_TRCCLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_TRCCLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLR	R/W	0h	Clears bits in the claim tag and determines the current value of the claim tag.

14.3.1.1.2.595 A53SS_APBADDR_ETM_CPU1_TRCDEVAFF0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCDEVAFF0 Register (Offset = FA8h) [reset = 80000001h]

Device Affinity Register 0

Return to Summary Table

Table 14-9467. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FA8h**

Figure 14-3140. A53SS_APBADDR_ETM_CPU1_TRCDEVAFF0 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_31_0							
R/W							
80000001h							
23	22	21	20	19	18	17	16
MPIDR_EL1_31_0							
R/W							
80000001h							
15	14	13	12	11	10	9	8
MPIDR_EL1_31_0							
R/W							
80000001h							
7	6	5	4	3	2	1	0
MPIDR_EL1_31_0							
R/W							
80000001h							

Table 14-9469. A53SS_APBADDR_ETM_CPU1_TRCDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_31_0	R/W	80000001h	Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.596 A53SS_APBADDR_ETM_CPU1_TRCDEVAFF1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCDEVAFF1 Register (Offset = FACh) [reset = 0h]

Device Affinity Register 1

Return to Summary Table

Table 14-9470. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FACh**

Figure 14-3141. A53SS_APBADDR_ETM_CPU1_TRCDEVAFF1 Name Register

31	30	29	28	27	26	25	24
MPIDR_EL1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
MPIDR_EL1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
MPIDR_EL1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MPIDR_EL1_63_32							
R/W							
0h							

Table 14-9472. A53SS_APBADDR_ETM_CPU1_TRCDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MPIDR_EL1_63_32	R/W	0h	Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.597 A53SS_APBADDR_ETM_CPU1_TRCLAR Register

1 A53SS_APBADDR_ETM_CPU1_TRCLAR Register (Offset = FB0h) [reset = 0h]

Software Lock Access Register

Return to Summary Table

Table 14-9473. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FB0h**

Figure 14-3142. A53SS_APBADDR_ETM_CPU1_TRCLAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9475. A53SS_APBADDR_ETM_CPU1_TRCLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Writing the key value 0xC5ACCE55 to this field clears the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register sets the lock, disabling write accesses to this component's registers through a memory mapped interface.Software can use the Software Lock to prevent accidental modification of the trace unit registers by software being debugged. For example, software that accidentally initializes an incorrect region of memory might disable the trace unit and make it impossible to trace the software.

14.3.1.1.2.598 A53SS_APBADDR_ETM_CPU1_TRCLSR Register

1 A53SS_APBADDR_ETM_CPU1_TRCLSR Register (Offset = FB4h) [reset = 0h]

Software Lock Status Register

Return to Summary Table

Table 14-9476. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FB4h**

Figure 14-3143. A53SS_APBADDR_ETM_CPU1_TRCLSR Name Register

31	30	29	28	27	26	25	24
RES0_TRCLSR_31_3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCLSR_31_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCLSR_31_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_TRCLSR_31_3					NTT	SLK	SLI
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-9478. A53SS_APBADDR_ETM_CPU1_TRCLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_TRCLSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. Possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. RAO.

14.3.1.1.2.599 A53SS_APBADDR_ETM_CPU1_TRCAUTHSTATUS Register

1 A53SS_APBADDR_ETM_CPU1_TRCAUTHSTATUS Register (Offset = FB8h) [reset = 88h]

Authentication Status Register

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Table 14-9479. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FB8h**

Figure 14-3144. A53SS_APBADDR_ETM_CPU1_TRCAUTHSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_TRCAUTHSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_TRCAUTHSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_TRCAUTHSTATUS_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SNID</td><td colspan="2">SID</td><td colspan="2">NSNID</td><td colspan="2">NSID</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">2h</td><td colspan="2">0h</td><td colspan="2">2h</td><td colspan="2">0h</td></tr>
</table>

Table 14-9481. A53SS_APBADDR_ETM_CPU1_TRCAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCAUTHSTATUS_31_8	R/W	0h	Reserved, RES0.
7:6	SNID	R/W	2h	Indicates whether the system enables the trace unit to support Secure non-invasive debug: 00 The trace unit does not implement support for Secure non-invasive debug. 01 Reserved. 10 Secure non-invasive debug is disabled. 11 Secure non-invasive debug is enabled.
5:4	SID	R/W	0h	Indicates whether the trace unit supports Secure invasive debug: 00 The trace unit does not support Secure invasive debug. All other values are reserved.

Table 14-9481. A53SS_APBADDR_ETM_CPU1_TRCAUTHSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	NSNID	R/W	2h	Indicates whether the system enables the trace unit to support Non-secure non-invasive debug: 00 The trace unit does not implement support for Non-secure non-invasive debug. 01 Reserved. 10 Non-secure non-invasive debug is disabled. 11 Non-secure non-invasive debug is enabled.
1:0	NSID	R/W	0h	Indicates whether the trace unit supports Non-secure invasive debug: 00 The trace unit does not support Non-secure invasive debug. All other values are reserved.

14.3.1.1.2.600 A53SS_APBADDR_ETM_CPU1_TRCDEVARCH Register

1 A53SS_APBADDR_ETM_CPU1_TRCDEVARCH Register (Offset = FBCh) [reset = 47704A13h]

Device Architecture Register

Return to Summary Table

Table 14-9482. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FBCh**

Figure 14-3145. A53SS_APBADDR_ETM_CPU1_TRCDEVARCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ARCHITECT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">ARCHITECT</td><td>PRESENT</td><td colspan="4">REVISION</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">23Bh</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4A13h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ARCHID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4A13h</td></tr>
</table>

Table 14-9484. A53SS_APBADDR_ETM_CPU1_TRCDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For trace, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is RAO.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For trace, the revision defined by ETMv4 is 0x0.All other values are reserved.
15:0	ARCHID	R/W	4A13h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For trace, bits [15:12] are the architecture version, 0x4; bits [11:0] are the architecture part number, 0xA13.This corresponds to trace architecture version ETMv4.

14.3.1.1.2.601 A53SS_APBADDR_ETM_CPU1_TRCDEVID Register

1 A53SS_APBADDR_ETM_CPU1_TRCDEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-9485. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FC8h**

Figure 14-3146. A53SS_APBADDR_ETM_CPU1_TRCDEVID Name Register

31	30	29	28	27	26	25	24
DEVID							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVID							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVID							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVID							
R/W							
0h							

Table 14-9487. A53SS_APBADDR_ETM_CPU1_TRCDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVID	R/W	0h	Indicates the capabilities of the trace unit. The implemented width of this field and its bit assignments are IMPLEMENTATION DEFINED. Unimplemented bits are RAZ/WI.If a component is configurable then ARM recommends that this field can also indicate which configuration options are implemented that differ from the standard configuration.

14.3.1.1.2.602 A53SS_APBADDR_ETM_CPU1_TRCDEVTYPE Register

1 A53SS_APBADDR_ETM_CPU1_TRCDEVTYPE Register (Offset = FCCh) [reset = 13h]

Device Type Register

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Table 14-9488. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FCCh**

Figure 14-3147. A53SS_APBADDR_ETM_CPU1_TRCDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCDEVTYPE_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUB				MAIN			
R/W				R/W			
1h				3h			

Table 14-9490. A53SS_APBADDR_ETM_CPU1_TRCDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Returns 0x1, to indicate that the ETM generates processor trace.All other values are reserved.
3:0	MAIN	R/W	3h	Returns 0x3, to indicate that the ETM is a trace source.All other values are reserved.

14.3.1.1.2.603 A53SS_APBADDR_ETM_CPU1_TRCPIDR4 Register

1 A53SS_APBADDR_ETM_CPU1_TRCPIDR4 Register (Offset = FD0h) [reset = 4h]

Peripheral Identification Register 4

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Table 14-9491. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FD0h**

Figure 14-3148. A53SS_APBADDR_ETM_CPU1_TRCPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR4_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR4_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR4_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-9493. A53SS_APBADDR_ETM_CPU1_TRCPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RES0. This indicates that the ETM memory map occupies 4KB.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code. For ARM Limited, this field is 0b0100.

14.3.1.1.2.604 A53SS_APBADDR_ETM_CPU1_TRCPIDR5 Register

1 A53SS_APBADDR_ETM_CPU1_TRCPIDR5 Register (Offset = FD4h) [reset = 0h]

Peripheral Identification Register 5

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Table 14-9494. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FD4h**

Figure 14-3149. A53SS_APBADDR_ETM_CPU1_TRCPIDR5 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR5_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR5_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR5_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR5_7_0							
R/W							
0h							

Table 14-9496. A53SS_APBADDR_ETM_CPU1_TRCPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR5_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR5_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.605 A53SS_APBADDR_ETM_CPU1_TRCPIDR6 Register

1 A53SS_APBADDR_ETM_CPU1_TRCPIDR6 Register (Offset = FD8h) [reset = 0h]

Peripheral Identification Register 6

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Table 14-9497. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FD8h**

Figure 14-3150. A53SS_APBADDR_ETM_CPU1_TRCPIDR6 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR6_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR6_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR6_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_TRCPIDR6_7_0							
R/W							
0h							

Table 14-9499. A53SS_APBADDR_ETM_CPU1_TRCPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR6_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR6_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.606 A53SS_APBADDR_ETM_CPU1_TRCPIDR7 Register

1 A53SS_APBADDR_ETM_CPU1_TRCPIDR7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register 7

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Table 14-9500. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FDCh**

Figure 14-3151. A53SS_APBADDR_ETM_CPU1_TRCPIDR7 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR7_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR7_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR7_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_TRCPIDR7_7_0							
R/W							
0h							

Table 14-9502. A53SS_APBADDR_ETM_CPU1_TRCPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR7_31_8	R/W	0h	Reserved, RES0.
7:0	RESERVED_TRCPIDR7_7_0	R/W	0h	RES0, reserved for future use.

14.3.1.1.2.607 A53SS_APBADDR_ETM_CPU1_TRCPIDR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCPIDR0 Register (Offset = FE0h) [reset = 5Dh]

Peripheral Identification Register 0

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Table 14-9503. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FE0h**

Figure 14-3152. A53SS_APBADDR_ETM_CPU1_TRCPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
5Dh							

Table 14-9505. A53SS_APBADDR_ETM_CPU1_TRCPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	5Dh	Part number, bits[7:0].

14.3.1.1.2.608 A53SS_APBADDR_ETM_CPU1_TRCPIDR1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCPIDR1 Register (Offset = FE4h) [reset = B9h]

Peripheral Identification Register 1

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Table 14-9506. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FE4h**

Figure 14-3153. A53SS_APBADDR_ETM_CPU1_TRCPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-9508. A53SS_APBADDR_ETM_CPU1_TRCPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, bits[3:0] of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, bits[11:8].

14.3.1.1.2.609 A53SS_APBADDR_ETM_CPU1_TRCPIDR2 Register

1 A53SS_APBADDR_ETM_CPU1_TRCPIDR2 Register (Offset = FE8h) [reset = 4Bh]

Peripheral Identification Register 2

Return to Summary Table

Table 14-9509. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FE8h**

Figure 14-3154. A53SS_APBADDR_ETM_CPU1_TRCPIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCPIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCPIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R/W				R/W	R/W		
4h				1h	3h		

Table 14-9511. A53SS_APBADDR_ETM_CPU1_TRCPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	The IMPLEMENTATION DEFINED revision number for the ETM implementation. See also TRCIDR1.REVISION.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.610 A53SS_APBADDR_ETM_CPU1_TRCPIDR3 Register

1 A53SS_APBADDR_ETM_CPU1_TRCPIDR3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register 3

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Table 14-9512. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FECh**

Figure 14-3155. A53SS_APBADDR_ETM_CPU1_TRCPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCPIDR3_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCPIDR3_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCPIDR3_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-9514. A53SS_APBADDR_ETM_CPU1_TRCPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	The IMPLEMENTATION DEFINED manufacturing revision number for the implementation. After silicon is available, if metal fixes are necessary, the manufacturer can alter the top metal layer so that this field can indicate any post-fab silicon changes.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.611 A53SS_APBADDR_ETM_CPU1_TRCCIDR0 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCIDR0 Register (Offset = FF0h) [reset = Dh]

Component Identification Register 0

Return to Summary Table

Table 14-9515. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FF0h**

Figure 14-3156. A53SS_APBADDR_ETM_CPU1_TRCCIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-9517. A53SS_APBADDR_ETM_CPU1_TRCCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.612 A53SS_APBADDR_ETM_CPU1_TRCCIDR1 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCIDR1 Register (Offset = FF4h) [reset = 90h]

Component Identification Register 1

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Table 14-9518. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FF4h**

Figure 14-3157. A53SS_APBADDR_ETM_CPU1_TRCCIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_TRCCIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_TRCCIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-9520. A53SS_APBADDR_ETM_CPU1_TRCCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, to indicate that the ETM is a debug component, with CoreSight architecture compliant management registers.
3:0	PRMBL_1	R/W	0h	Preamble. Must read as 0x0.

14.3.1.1.2.613 A53SS_APBADDR_ETM_CPU1_TRCCIDR2 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCIDR2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register 2

Return to Summary Table

Table 14-9521. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FF8h**

Figure 14-3158. A53SS_APBADDR_ETM_CPU1_TRCCIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR2_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR2_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR2_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R/W							
5h							

Table 14-9523. A53SS_APBADDR_ETM_CPU1_TRCCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.614 A53SS_APBADDR_ETM_CPU1_TRCCIDR3 Register

1 A53SS_APBADDR_ETM_CPU1_TRCCIDR3 Register (Offset = FFCh) [reset = B1h]

Component Identification Register 3

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Table 14-9524. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3013 0FFCh**

Figure 14-3159. A53SS_APBADDR_ETM_CPU1_TRCCIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_TRCCIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_TRCCIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_TRCCIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-9526. A53SS_APBADDR_ETM_CPU1_TRCCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_TRCCIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.1.1.2.615 A53SS_APBADDR_CTI_CPU1_CTICONTROL Register

1 A53SS_APBADDR_CTI_CPU1_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register

Return to Summary Table

Table 14-9527. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0000h**

Figure 14-3160. A53SS_APBADDR_CTI_CPU1_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RES0_CTICONTROL_31_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICONTROL_31_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICONTROL_31_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTICONTROL_31_1							GLBEN
R/W							R/W
0h							0h

Table 14-9529. A53SS_APBADDR_CTI_CPU1_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTICONTROL_31_1	R/W	0h	Reserved, RES0.
0	GLBEN	R/W	0h	Enables or disables the CTI mapping functions. Possible values of this field are: 0 CTI mapping functions disabled. 1 CTI mapping functions enabled. When the mapping functions are disabled, no new events are signaled on either output triggers or output channels. If a previously asserted output trigger has not been acknowledged, it remains asserted after the mapping functions are disabled. All output triggers are disabled by CTI reset.

14.3.1.1.2.616 A53SS_APBADDR_CTI_CPU1_CTIINTACK Register

1 A53SS_APBADDR_CTI_CPU1_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Output Trigger Acknowledge Register

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Table 14-9530. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0010h**

Figure 14-3161. A53SS_APBADDR_CTI_CPU1_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINTACK_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINTACK_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINTACK_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACK_N							
R/W							
0h							

Table 14-9532. A53SS_APBADDR_CTI_CPU1_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTIINTACK_31_8	R/W	0h	Reserved RES0
7:0	ACK_N	R/W	0h	Can be used to create soft acknowledges for output triggers

14.3.1.1.2.617 A53SS_APBADDR_CTI_CPU1_CTIAPPSET Register

1 A53SS_APBADDR_CTI_CPU1_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register

Return to Summary Table

Table 14-9533. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0014h**

Figure 14-3162. A53SS_APBADDR_CTI_CPU1_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIAPPSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIAPPSET_31_4				CTIAPPSETX			
R/W				R/W			
0h				0h			

Table 14-9535. A53SS_APBADDR_CTI_CPU1_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPSET_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPSETX	R/W	0h	Application trigger <x> enable

14.3.1.1.2.618 A53SS_APBADDR_CTI_CPU1_CTIAPPCLEAR Register

1 A53SS_APBADDR_CTI_CPU1_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register

Return to Summary Table

Table 14-9536. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0018h**

Figure 14-3163. A53SS_APBADDR_CTI_CPU1_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIAPPCLEAR_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIAPPCLEAR_31_4				CTIAPPCLEARX			
R/W				R/W			
0h				0h			

Table 14-9538. A53SS_APBADDR_CTI_CPU1_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPCLEAR_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPCLEARX	R/W	0h	Application trigger <x> disable

14.3.1.1.2.619 A53SS_APBADDR_CTI_CPU1_CTIAPPPULSE Register

1 A53SS_APBADDR_CTI_CPU1_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Pulse Register

Return to Summary Table

Table 14-9539. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 001Ch**

Figure 14-3164. A53SS_APBADDR_CTI_CPU1_CTIAPPPULSE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPPULSE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPPULSE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIAPPPULSE_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIAPPPULSE_31_4</td><td colspan="4">CTIAPPPULSEX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9541. A53SS_APBADDR_CTI_CPU1_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIAPPPULSE_31_4	R/W	0h	Reserved RES0
3:0	CTIAPPPULSEX	R/W	0h	Generate event pulse on ECT channel <x>.

14.3.1.1.2.620 A53SS_APBADDR_CTI_CPU1_CTIINEN0 Register

1 A53SS_APBADDR_CTI_CPU1_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 0

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Table 14-9542. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0020h**

Figure 14-3165. A53SS_APBADDR_CTI_CPU1_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN0_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN0_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN0_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN0_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-9544. A53SS_APBADDR_CTI_CPU1_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN0_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 0 to output channel <x> enable

14.3.1.1.2.621 A53SS_APBADDR_CTI_CPU1_CTIINEN1 Register

1 A53SS_APBADDR_CTI_CPU1_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 1

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Table 14-9545. Instance Table

Instance Name	Physical Address
A53SS0	0007 3014 0024h

Figure 14-3166. A53SS_APBADDR_CTI_CPU1_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN1_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN1_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN1_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN1_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-9547. A53SS_APBADDR_CTI_CPU1_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN1_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 1 to output channel <x> enable

14.3.1.1.2.622 A53SS_APBADDR_CTI_CPU1_CTIINEN2 Register

1 A53SS_APBADDR_CTI_CPU1_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 2

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Table 14-9548. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0028h**

Figure 14-3167. A53SS_APBADDR_CTI_CPU1_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIINEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIINEN2_31_4</td><td colspan="4">INENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9550. A53SS_APBADDR_CTI_CPU1_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN2_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 2 to output channel <x> enable

14.3.1.1.2.623 A53SS_APBADDR_CTI_CPU1_CTIINEN3 Register

1 A53SS_APBADDR_CTI_CPU1_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 3

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Table 14-9551. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 002Ch**

Figure 14-3168. A53SS_APBADDR_CTI_CPU1_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN3_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN3_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN3_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN3_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-9553. A53SS_APBADDR_CTI_CPU1_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN3_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 3 to output channel <x> enable

14.3.1.1.2.624 A53SS_APBADDR_CTI_CPU1_CTIINEN4 Register

1 A53SS_APBADDR_CTI_CPU1_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 4

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Table 14-9554. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0030h**

Figure 14-3169. A53SS_APBADDR_CTI_CPU1_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN4_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN4_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN4_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN4_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-9556. A53SS_APBADDR_CTI_CPU1_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN4_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 4 to output channel <x> enable

14.3.1.1.2.625 A53SS_APBADDR_CTI_CPU1_CTIINEN5 Register

1 A53SS_APBADDR_CTI_CPU1_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 5

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Table 14-9557. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0034h**

Figure 14-3170. A53SS_APBADDR_CTI_CPU1_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN5_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN5_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN5_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN5_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-9559. A53SS_APBADDR_CTI_CPU1_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN5_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 5 to output channel <x> enable

14.3.1.1.2.626 A53SS_APBADDR_CTI_CPU1_CTIINEN6 Register

1 A53SS_APBADDR_CTI_CPU1_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 6

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Table 14-9560. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0038h**

Figure 14-3171. A53SS_APBADDR_CTI_CPU1_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIINEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIINEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIINEN6_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-9562. A53SS_APBADDR_CTI_CPU1_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN6_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 6 to output channel <x> enable

14.3.1.1.2.627 A53SS_APBADDR_CTI_CPU1_CTIINEN7 Register

1 A53SS_APBADDR_CTI_CPU1_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Input Trigger to Output Channel Enable Register 7

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Table 14-9563. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 003Ch**

Figure 14-3172. A53SS_APBADDR_CTI_CPU1_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIINEN7_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIINEN7_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIINEN7_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIINEN7_31_4				INENX			
R/W				R/W			
0h				0h			

Table 14-9565. A53SS_APBADDR_CTI_CPU1_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIINEN7_31_4	R/W	0h	Reserved RES0
3:0	INENX	R/W	0h	Input trigger 7 to output channel <x> enable

14.3.1.1.2.628 A53SS_APBADDR_CTI_CPU1_CTIOUTEN0 Register

1 A53SS_APBADDR_CTI_CPU1_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 0

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Table 14-9566. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00A0h**

Figure 14-3173. A53SS_APBADDR_CTI_CPU1_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN0_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN0_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-9568. A53SS_APBADDR_CTI_CPU1_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN0_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 0 enable

14.3.1.1.2.629 A53SS_APBADDR_CTI_CPU1_CTIOUTEN1 Register

1 A53SS_APBADDR_CTI_CPU1_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 1

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Table 14-9569. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00A4h**

Figure 14-3174. A53SS_APBADDR_CTI_CPU1_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN1_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN1_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-9571. A53SS_APBADDR_CTI_CPU1_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN1_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 1 enable

14.3.1.1.2.630 A53SS_APBADDR_CTI_CPU1_CTIOUTEN2 Register

1 A53SS_APBADDR_CTI_CPU1_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 2

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Table 14-9572. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00A8h**

Figure 14-3175. A53SS_APBADDR_CTI_CPU1_CTIOUTEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_CTIOUTEN2_31_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_CTIOUTEN2_31_4</td><td colspan="4">OUTENX</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9574. A53SS_APBADDR_CTI_CPU1_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN2_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 2 enable

14.3.1.1.2.631 A53SS_APBADDR_CTI_CPU1_CTIOUTEN3 Register

1 A53SS_APBADDR_CTI_CPU1_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 3

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Table 14-9575. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00ACh**

Figure 14-3176. A53SS_APBADDR_CTI_CPU1_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTIOUTEN3_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTIOUTEN3_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-9577. A53SS_APBADDR_CTI_CPU1_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN3_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 3 enable

14.3.1.1.2.632 A53SS_APBADDR_CTI_CPU1_CTIOUTEN4 Register

1 A53SS_APBADDR_CTI_CPU1_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 4

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Table 14-9578. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00B0h**

Figure 14-3177. A53SS_APBADDR_CTI_CPU1_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN4_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN4_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-9580. A53SS_APBADDR_CTI_CPU1_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN4_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 4 enable

14.3.1.1.2.633 A53SS_APBADDR_CTI_CPU1_CTIOUTEN5 Register

1 A53SS_APBADDR_CTI_CPU1_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 5

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Table 14-9581. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00B4h**

Figure 14-3178. A53SS_APBADDR_CTI_CPU1_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN5_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN5_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-9583. A53SS_APBADDR_CTI_CPU1_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN5_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 5 enable

14.3.1.1.2.634 A53SS_APBADDR_CTI_CPU1_CTIOUTEN6 Register

1 A53SS_APBADDR_CTI_CPU1_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 6

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Table 14-9584. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00B8h**

Figure 14-3179. A53SS_APBADDR_CTI_CPU1_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN6_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN6_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-9586. A53SS_APBADDR_CTI_CPU1_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN6_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 6 enable

14.3.1.1.2.635 A53SS_APBADDR_CTI_CPU1_CTIOUTEN7 Register

1 A53SS_APBADDR_CTI_CPU1_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Input Channel to Output Trigger Enable Register 7

Return to Summary Table

Table 14-9587. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 00BCh**

Figure 14-3180. A53SS_APBADDR_CTI_CPU1_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIOUTEN7_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIOUTEN7_31_4				OUTENX			
R/W				R/W			
0h				0h			

Table 14-9589. A53SS_APBADDR_CTI_CPU1_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIOUTEN7_31_4	R/W	0h	Reserved RES0
3:0	OUTENX	R/W	0h	Input channel <x> to output trigger 7 enable

14.3.1.1.2.636 A53SS_APBADDR_CTI_CPU1_CTITRIGINSTATUS Register

1 A53SS_APBADDR_CTI_CPU1_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

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Table 14-9590. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0130h**

Figure 14-3181. A53SS_APBADDR_CTI_CPU1_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTITRIGINSTATUS_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRINN							
R/W							
0h							

Table 14-9592. A53SS_APBADDR_CTI_CPU1_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGINSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TRINN	R/W	0h	Provides the status of the trigger inputs

14.3.1.1.2.637 A53SS_APBADDR_CTI_CPU1_CTITRIGOUTSTATUS Register

1 A53SS_APBADDR_CTI_CPU1_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

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Table 14-9593. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0134h**

Figure 14-3182. A53SS_APBADDR_CTI_CPU1_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTITRIGOUTSTATUS_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
TROUTN							
R/W							
0h							

Table 14-9595. A53SS_APBADDR_CTI_CPU1_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_CTITRIGOUTSTATUS_31_8	R/W	0h	Reserved RES0
7:0	TROUTN	R/W	0h	Provides the status of the trigger outputs

14.3.1.1.2.638 A53SS_APBADDR_CTI_CPU1_CTICHINSTATUS Register

1 A53SS_APBADDR_CTI_CPU1_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

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Table 14-9596. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0138h**

Figure 14-3183. A53SS_APBADDR_CTI_CPU1_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICHINSTATUS_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICHINSTATUS_31_4				CHINN			
R/W				R/W			
0h				0h			

Table 14-9598. A53SS_APBADDR_CTI_CPU1_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHINSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHINN	R/W	0h	Provides the raw status of the ECT channel inputs to the CTI

14.3.1.1.2.639 A53SS_APBADDR_CTI_CPU1_CTICHOUTSTATUS Register

1 A53SS_APBADDR_CTI_CPU1_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

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Table 14-9599. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 013Ch**

Figure 14-3184. A53SS_APBADDR_CTI_CPU1_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTICHOUTSTATUS_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTICHOUTSTATUS_31_4				CHOUTN			
R/W				R/W			
0h				0h			

Table 14-9601. A53SS_APBADDR_CTI_CPU1_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICHOUTSTATUS_31_4	R/W	0h	Reserved RES0
3:0	CHOUTN	R/W	0h	Provides the status of the ECT channel outputs from the CTI

14.3.1.1.2.640 A53SS_APBADDR_CTI_CPU1_CTIGATE Register

1 A53SS_APBADDR_CTI_CPU1_CTIGATE Register (Offset = 140h) [reset = Fh]

CTI Channel Gate Enable Register

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Table 14-9602. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0140h**

Figure 14-3185. A53SS_APBADDR_CTI_CPU1_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIGATE_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIGATE_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIGATE_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIGATE_31_4				GATEX			
R/W				R/W			
0h				Fh			

Table 14-9604. A53SS_APBADDR_CTI_CPU1_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTIGATE_31_4	R/W	0h	Reserved RES0
3:0	GATEX	R/W	Fh	Determines whether events on channels propagate through the CTM to other ECT components or from the CTM into the CTI

14.3.1.1.2.641 A53SS_APBADDR_CTI_CPU1_ASICCTL Register

1 A53SS_APBADDR_CTI_CPU1_ASICCTL Register (Offset = 144h) [reset = 0h]

CTI External Multiplexor Control register

Return to Summary Table

Table 14-9605. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0144h**

Figure 14-3186. A53SS_APBADDR_CTI_CPU1_ASICCTL Name Register

31	30	29	28	27	26	25	24
RES0_ASICCTL_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_ASICCTL_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_ASICCTL_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-9607. A53SS_APBADDR_CTI_CPU1_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_ASICCTL_31_8	R/W	0h	Reserved, RES0.
7:0	ASICCTL	R/W	0h	IMPLEMENTATION DEFINED ASIC control. Provides a control for external multiplexing of additional triggers into the CTI.If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected in CTIDEVID.EXTMUXNUM.If CTIDEVID.EXTMUXNUM is zero, this field is RAZ.

14.3.1.1.2.642 A53SS_APBADDR_CTI_CPU1_CTIITCTRL Register

1 A53SS_APBADDR_CTI_CPU1_CTIITCTRL Register (Offset = F00h) [reset = 0h]

CTI Integration mode Control Register

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Table 14-9608. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0F00h**

Figure 14-3187. A53SS_APBADDR_CTI_CPU1_CTIITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIITCTRL_31_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RES0_CTIITCTRL_31_1</td><td>IME</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9610. A53SS_APBADDR_CTI_CPU1_CTIITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES0_CTIITCTRL_31_1	R/W	0h	Reserved, RES0.
0	IME	R/W	0h	Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED. 0 Normal operation. 1 Integration mode enabled.

14.3.1.1.2.643 A53SS_APBADDR_CTI_CPU1_CTICLAIMSET Register

1 A53SS_APBADDR_CTI_CPU1_CTICLAIMSET Register (Offset = FA0h) [reset = Fh]

CTI Claim Set

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Table 14-9611. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FA0h**

Figure 14-3188. A53SS_APBADDR_CTI_CPU1_CTICLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICLAIMSET_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICLAIMSET_31_4				CLAIMX			
R/W				R/W			
0h				Fh			

Table 14-9613. A53SS_APBADDR_CTI_CPU1_CTICLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMSET_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	Fh	CLAIM tag set bit

14.3.1.1.2.644 A53SS_APBADDR_CTI_CPU1_CTICLAIMCLR Register

1 A53SS_APBADDR_CTI_CPU1_CTICLAIMCLR Register (Offset = FA4h) [reset = 0h]

CTI Claim Clear

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Table 14-9614. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FA4h**

Figure 14-3189. A53SS_APBADDR_CTI_CPU1_CTICLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_CTICLAIMCLR_31_4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_CTICLAIMCLR_31_4				CLAIMX			
R/W				R/W			
0h				0h			

Table 14-9616. A53SS_APBADDR_CTI_CPU1_CTICLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_CTICLAIMCLR_31_4	R/W	0h	Reserved RES0
3:0	CLAIMX	R/W	0h	Clear CLAIM tag

14.3.1.1.2.645 A53SS_APBADDR_CTI_CPU1_CTIDEVAFF0 Register

1 A53SS_APBADDR_CTI_CPU1_CTIDEVAFF0 Register (Offset = FA8h) [reset = 80000001h]

CTI Device Affinity Register 0

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Table 14-9617. Instance Table

Instance Name	Physical Address
A53SS0	0007 3014 0FA8h

Figure 14-3190. A53SS_APBADDR_CTI_CPU1_CTIDEVAFF0 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF0							
R/W							
80000001h							
23	22	21	20	19	18	17	16
CTIDEVAFF0							
R/W							
80000001h							
15	14	13	12	11	10	9	8
CTIDEVAFF0							
R/W							
80000001h							
7	6	5	4	3	2	1	0
CTIDEVAFF0							
R/W							
80000001h							

Table 14-9619. A53SS_APBADDR_CTI_CPU1_CTIDEVAFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF0	R/W	80000001h	MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.646 A53SS_APBADDR_CTI_CPU1_CTIDEVAFF1 Register

1 A53SS_APBADDR_CTI_CPU1_CTIDEVAFF1 Register (Offset = FACh) [reset = 0h]

CTI Device Affinity Register 1

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Table 14-9620. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FACh**

Figure 14-3191. A53SS_APBADDR_CTI_CPU1_CTIDEVAFF1 Name Register

31	30	29	28	27	26	25	24
CTIDEVAFF1							
R/W							
0h							
23	22	21	20	19	18	17	16
CTIDEVAFF1							
R/W							
0h							
15	14	13	12	11	10	9	8
CTIDEVAFF1							
R/W							
0h							
7	6	5	4	3	2	1	0
CTIDEVAFF1							
R/W							
0h							

Table 14-9622. A53SS_APBADDR_CTI_CPU1_CTIDEVAFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTIDEVAFF1	R/W	0h	MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented exception level.

14.3.1.1.2.647 A53SS_APBADDR_CTI_CPU1_CTILAR Register

1 A53SS_APBADDR_CTI_CPU1_CTILAR Register (Offset = FB0h) [reset = 0h]

CTI Lock Access Register

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Table 14-9623. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FB0h**

Figure 14-3192. A53SS_APBADDR_CTI_CPU1_CTILAR Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							
R/W							
0h							

Table 14-9625. A53SS_APBADDR_CTI_CPU1_CTILAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEY	R/W	0h	Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory mapped interface.

14.3.1.1.2.648 A53SS_APBADDR_CTI_CPU1_CTILSR Register

1 A53SS_APBADDR_CTI_CPU1_CTILSR Register (Offset = FB4h) [reset = 0h]

CTI Lock Status Register

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Table 14-9626. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FB4h**

Figure 14-3193. A53SS_APBADDR_CTI_CPU1_CTILSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTILSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTILSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTILSR_31_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RES0_CTILSR_31_3</td><td>NTT</td><td>SLK</td><td>SLI</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9628. A53SS_APBADDR_CTI_CPU1_CTILSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RES0_CTILSR_31_3	R/W	0h	Reserved, RES0.
2	NTT	R/W	0h	Not thirty-two bit access required. RAZ.
1	SLK	R/W	0h	Software lock status for this component. For an access to LSR that is not a memory-mapped access, or when the software lock is not implemented, this field is RES0.For memory-mapped accesses when the software lock is implemented, possible values of this field are: 0 Lock clear. Writes are permitted to this component's registers. 1 Lock set. Writes to this component's registers are ignored, and reads have no side effects.
0	SLI	R/W	0h	Software lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are: 0 Software lock not implemented or not memory-mapped access. 1 Software lock implemented and memory-mapped access.

14.3.1.1.2.649 A53SS_APBADDR_CTI_CPU1_CTIAUTHSTATUS Register

1 A53SS_APBADDR_CTI_CPU1_CTIAUTHSTATUS Register (Offset = FB8h) [reset = Ah]

CTI Authentication Status Register

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Table 14-9629. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FB8h**

Figure 14-3194. A53SS_APBADDR_CTI_CPU1_CTIAUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIAUTHSTATUS_31_4							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIAUTHSTATUS_31_4				NSNID		NSID	
R/W				R/W		R/W	
0h				2h		2h	

Table 14-9631. A53SS_APBADDR_CTI_CPU1_CTIAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES0_CTIAUTHSTATUS_31_4	R/W	0h	Reserved, RES0.
3:2	NSNID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SNID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSNID.
1:0	NSID	R/W	2h	If EL3 is not implemented and the processor is Secure, holds the same value as DBGAUTHSTATUS_EL1.SID.Otherwise, holds the same value as DBGAUTHSTATUS_EL1.NSID.

14.3.1.1.2.650 A53SS_APBADDR_CTI_CPU1_CTIDEVARCH Register

1 A53SS_APBADDR_CTI_CPU1_CTIDEVARCH Register (Offset = FBCh) [reset = 47701A14h]

CTI Device Architecture Register

Return to Summary Table

Table 14-9632. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FBCh**

Figure 14-3195. A53SS_APBADDR_CTI_CPU1_CTIDEVARCH Name Register

31	30	29	28	27	26	25	24
ARCHITECT							
R/W							
23Bh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ARCHITECT			PRESENT	REVISION			
R/W			R/W	R/W			
23Bh			1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ARCHID							
R/W							
1A14h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ARCHID							
R/W							
1A14h							

Table 14-9634. A53SS_APBADDR_CTI_CPU1_CTIDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	ARCHITECT	R/W	23Bh	Defines the architecture of the component. For CTI, this is ARM Limited.Bits [31:28] are the JEP 106 continuation code, 0x4.Bits [27:21] are the JEP 106 ID code, 0x3B.
20	PRESENT	R/W	1h	When set to 1, indicates that the DEVARCH is present.This field is 1 in v8-A.
19:16	REVISION	R/W	0h	Defines the architecture revision. For architectures defined by ARM this is the minor revision.For CTI, the revision defined by v8-A is 0x0.All other values are reserved.
15:0	ARCHID	R/W	1A14h	Defines this part to be a v8-A debug component. For architectures defined by ARM this is further subdivided.For CTI:Bits [15:12] are the architecture version, 0x1.Bits [11:0] are the architecture part number, 0xA14.This corresponds to CTI architecture version CTIv2.

14.3.1.1.2.651 A53SS_APBADDR_CTI_CPU1_CTIDEVID2 Register

1 A53SS_APBADDR_CTI_CPU1_CTIDEVID2 Register (Offset = FC0h) [reset = 0h]

CTI Device ID Register 2

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Table 14-9635. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FC0h**

Figure 14-3196. A53SS_APBADDR_CTI_CPU1_CTIDEVID2 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID2_31_0							
R/W							
0h							

Table 14-9637. A53SS_APBADDR_CTI_CPU1_CTIDEVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID2_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.652 A53SS_APBADDR_CTI_CPU1_CTIDEVID1 Register

1 A53SS_APBADDR_CTI_CPU1_CTIDEVID1 Register (Offset = FC4h) [reset = 0h]

CTI Device ID Register 1

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Table 14-9638. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FC4h**

Figure 14-3197. A53SS_APBADDR_CTI_CPU1_CTIDEVID1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIDEVID1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIDEVID1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RES0_CTIDEVID1_31_0							
R/W							
0h							

Table 14-9640. A53SS_APBADDR_CTI_CPU1_CTIDEVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES0_CTIDEVID1_31_0	R/W	0h	Reserved, RES0.

14.3.1.1.2.653 A53SS_APBADDR_CTI_CPU1_CTIDEVID Register

1 A53SS_APBADDR_CTI_CPU1_CTIDEVID Register (Offset = FC8h) [reset = 1040800h]

CTI Device ID Register 0

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Table 14-9641. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FC8h**

Figure 14-3198. A53SS_APBADDR_CTI_CPU1_CTIDEVID Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVID_31_26						INOUT	
R/W						R/W	
0h						1h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIDEVID_23_22		NUMCHAN					
R/W		R/W					
0h		4h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIDEVID_15_14		NUMTRIG					
R/W		R/W					
0h		8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES0_CTIDEVID_7_5			EXTMUXNUM				
R/W			R/W				
0h			0h				

Table 14-9643. A53SS_APBADDR_CTI_CPU1_CTIDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES0_CTIDEVID_31_26	R/W	0h	Reserved, RES0.
25:24	INOUT	R/W	1h	Input/output options. Indicates presence of the input gate. If the CTM is not implemented, this field is RAZ. 00 CTIGATE does not mask propagation of input events from external channels. 01 CTIGATE masks propagation of input events from external channels. All other values are reserved.
23:22	RES0_CTIDEVID_23_22	R/W	0h	Reserved, RES0.
21:16	NUMCHAN	R/W	4h	Number of ECT channels implemented. IMPLEMENTATION DEFINED. For v8-A, valid values are: 000011 3 channels [0..2] implemented. 000100 4 channels [0..3] implemented. 000101 5 channels [0..4] implemented. 000110 6 channels [0..5] implemented. and so on up to 0b100000, 32 channels [0..31] implemented.All other values are reserved.
15:14	RES0_CTIDEVID_15_14	R/W	0h	Reserved, RES0.

Table 14-9643. A53SS_APBADDR_CTI_CPU1_CTIDEVID Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	NUMTRIG	R/W	8h	Number of triggers implemented. IMPLEMENTATION DEFINED. This is one more than the index of the largest trigger, rather than the actual number of triggers.For v8-A, valid values are: 000011 Up to 3 triggers [0..2] implemented. 001000 Up to 8 triggers [0..7] implemented. 001001 Up to 9 triggers [0..8] implemented. 001010 Up to 10 triggers [0..9] implemented. and so on up to 0b100000, 32 triggers [0..31] implemented.All other values are reserved. If the Trace Extension is implemented, this field must be at least 001000. There is no guarantee that any of the implemented triggers, including the highest numbered, are connected to any components.
7:5	RES0_CTIDEVID_7_5	R/W	0h	Reserved, RES0.
4:0	EXTMUXNUM	R/W	0h	Maximum number of external triggers available for multiplexing into the CTI. This relates only to additional external triggers outside those defined for v8-A.

14.3.1.1.2.654 A53SS_APBADDR_CTI_CPU1_CTIDEVTYPE Register

1 A53SS_APBADDR_CTI_CPU1_CTIDEVTYPE Register (Offset = FCCh) [reset = 14h]

CTI Device Type Register

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Table 14-9644. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FCCh**

Figure 14-3199. A53SS_APBADDR_CTI_CPU1_CTIDEVTYPE Name Register

31	30	29	28	27	26	25	24
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIDEVTYPE_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAJOR			
R/W				R/W			
1h				4h			

Table 14-9646. A53SS_APBADDR_CTI_CPU1_CTIDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIDEVTYPE_31_8	R/W	0h	Reserved, RES0.
7:4	SUB	R/W	1h	Subtype. Must read as 0x1 to indicate this is a processor component.
3:0	MAJOR	R/W	4h	Major type. Must read as 0x4 to indicate this is a cross-trigger component.

14.3.1.1.2.655 A53SS_APBADDR_CTI_CPU1_CTIPIDR4 Register

1 A53SS_APBADDR_CTI_CPU1_CTIPIDR4 Register (Offset = FD0h) [reset = 4h]

CTI Peripheral Identification Register 4

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Table 14-9647. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FD0h**

Figure 14-3200. A53SS_APBADDR_CTI_CPU1_CTIPIDR4 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR4_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR4_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR4_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R/W				R/W			
0h				4h			

Table 14-9649. A53SS_APBADDR_CTI_CPU1_CTIPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR4_31_8	R/W	0h	Reserved, RES0.
7:4	SIZE	R/W	0h	Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.
3:0	DES_2	R/W	4h	Designer, JEP106 continuation code, least significant nibble. For ARM Limited, this field is 0b0100.

14.3.1.1.2.656 A53SS_APBADDR_CTI_CPU1_CTIPIDR5 Register

1 A53SS_APBADDR_CTI_CPU1_CTIPIDR5 Register (Offset = FD4h) [reset = 0h]

CTI Peripheral Identification Register 5

Return to Summary Table

Table 14-9650. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FD4h**

Figure 14-3201. A53SS_APBADDR_CTI_CPU1_CTIPIDR5 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR5_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR5_31_0							
R/W							
0h							

Table 14-9652. A53SS_APBADDR_CTI_CPU1_CTIPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR5_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.657 A53SS_APBADDR_CTI_CPU1_CTIPIDR6 Register

1 A53SS_APBADDR_CTI_CPU1_CTIPIDR6 Register (Offset = FD8h) [reset = 0h]

CTI Peripheral Identification Register 6

Return to Summary Table

Table 14-9653. Instance Table

Instance Name	Physical Address
A53SS0	0007 3014 0FD8h

Figure 14-3202. A53SS_APBADDR_CTI_CPU1_CTIPIDR6 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR6_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR6_31_0							
R/W							
0h							

Table 14-9655. A53SS_APBADDR_CTI_CPU1_CTIPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR6_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.658 A53SS_APBADDR_CTI_CPU1_CTIPIDR7 Register

1 A53SS_APBADDR_CTI_CPU1_CTIPIDR7 Register (Offset = FDCh) [reset = 0h]

CTI Peripheral Identification Register 7

Return to Summary Table

Table 14-9656. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FDCh**

Figure 14-3203. A53SS_APBADDR_CTI_CPU1_CTIPIDR7 Name Register

31	30	29	28	27	26	25	24
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_CTIPIDR7_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_CTIPIDR7_31_0							
R/W							
0h							

Table 14-9658. A53SS_APBADDR_CTI_CPU1_CTIPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_CTIPIDR7_31_0	R/W	0h	Reserved RES0

14.3.1.1.2.659 A53SS_APBADDR_CTI_CPU1_CTIPIDR0 Register

1 A53SS_APBADDR_CTI_CPU1_CTIPIDR0 Register (Offset = FE0h) [reset = A8h]

CTI Peripheral Identification Register 0

Return to Summary Table

Table 14-9659. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FE0h**

Figure 14-3204. A53SS_APBADDR_CTI_CPU1_CTIPIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTIPIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTIPIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PART_0							
R/W							
A8h							

Table 14-9661. A53SS_APBADDR_CTI_CPU1_CTIPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PART_0	R/W	A8h	Part number, least significant byte.

14.3.1.1.2.660 A53SS_APBADDR_CTI_CPU1_CTIPIDR1 Register

1 A53SS_APBADDR_CTI_CPU1_CTIPIDR1 Register (Offset = FE4h) [reset = B9h]

CTI Peripheral Identification Register 1

Return to Summary Table

Table 14-9662. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FE4h**

Figure 14-3205. A53SS_APBADDR_CTI_CPU1_CTIPIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR1_31_8							
R/W							
0h							

23	22	21	20	19	18	17	16
RES0_CTIPIDR1_31_8							
R/W							
0h							

15	14	13	12	11	10	9	8
RES0_CTIPIDR1_31_8							
R/W							
0h							

7	6	5	4	3	2	1	0
DES_0				PART_1			
R/W				R/W			
Bh				9h			

Table 14-9664. A53SS_APBADDR_CTI_CPU1_CTIPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	DES_0	R/W	Bh	Designer, least significant nibble of JEP106 ID code. For ARM Limited, this field is 0b1011.
3:0	PART_1	R/W	9h	Part number, most significant nibble.

14.3.1.1.2.661 A53SS_APBADDR_CTI_CPU1_CTIPIDR2 Register

1 A53SS_APBADDR_CTI_CPU1_CTIPIDR2 Register (Offset = FE8h) [reset = 4Bh]

CTI Peripheral Identification Register 2

Return to Summary Table

Table 14-9665. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FE8h**

Figure 14-3206. A53SS_APBADDR_CTI_CPU1_CTIPIDR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES0_CTIPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RES0_CTIPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RES0_CTIPIDR2_31_8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVISION</td><td>JEDEC</td><td colspan="3">DES_1</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">4h</td><td>1h</td><td colspan="3">3h</td></tr>
</table>

Table 14-9667. A53SS_APBADDR_CTI_CPU1_CTIPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR2_31_8	R/W	0h	Reserved, RES0.
7:4	REVISION	R/W	4h	Part major revision. Parts can also use this field to extend Part number to 16-bits.
3	JEDEC	R/W	1h	RAO. Indicates a JEP106 identity code is used.
2:0	DES_1	R/W	3h	Designer, most significant bits of JEP106 ID code. For ARM Limited, this field is 0b011.

14.3.1.1.2.662 A53SS_APBADDR_CTI_CPU1_CTIPIDR3 Register

1 A53SS_APBADDR_CTI_CPU1_CTIPIDR3 Register (Offset = FECh) [reset = 0h]

CTI Peripheral Identification Register 3

Return to Summary Table

Table 14-9668. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FECh**

Figure 14-3207. A53SS_APBADDR_CTI_CPU1_CTIPIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTIPIDR3_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTIPIDR3_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTIPIDR3_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R/W				R/W			
0h				0h			

Table 14-9670. A53SS_APBADDR_CTI_CPU1_CTIPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTIPIDR3_31_8	R/W	0h	Reserved, RES0.
7:4	REVAND	R/W	0h	Part minor revision. Parts using CTIPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.
3:0	CMOD	R/W	0h	Customer modified. Indicates someone other than the Designer has modified the component.

14.3.1.1.2.663 A53SS_APBADDR_CTI_CPU1_CTICIDR0 Register

1 A53SS_APBADDR_CTI_CPU1_CTICIDR0 Register (Offset = FF0h) [reset = Dh]

CTI Component Identification Register 0

Return to Summary Table

Table 14-9671. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FF0h**

Figure 14-3208. A53SS_APBADDR_CTI_CPU1_CTICIDR0 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR0_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR0_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR0_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R/W							
Dh							

Table 14-9673. A53SS_APBADDR_CTI_CPU1_CTICIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR0_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_0	R/W	Dh	Preamble. Must read as 0x0D.

14.3.1.1.2.664 A53SS_APBADDR_CTI_CPU1_CTICIDR1 Register

1 A53SS_APBADDR_CTI_CPU1_CTICIDR1 Register (Offset = FF4h) [reset = 90h]

CTI Component Identification Register 1

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Table 14-9674. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FF4h**

Figure 14-3209. A53SS_APBADDR_CTI_CPU1_CTICIDR1 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR1_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTICIDR1_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTICIDR1_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R/W				R/W			
9h				0h			

Table 14-9676. A53SS_APBADDR_CTI_CPU1_CTICIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR1_31_8	R/W	0h	Reserved, RES0.
7:4	CLASS	R/W	9h	Component class. Reads as 0x9, debug component.
3:0	PRMBL_1	R/W	0h	Preamble. RAZ.

14.3.1.1.2.665 A53SS_APBADDR_CTI_CPU1_CTICIDR2 Register

1 A53SS_APBADDR_CTI_CPU1_CTICIDR2 Register (Offset = FF8h) [reset = 5h]

CTI Component Identification Register 2

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Table 14-9677. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FF8h**

Figure 14-3210. A53SS_APBADDR_CTI_CPU1_CTICIDR2 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR2_31_8							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES0_CTICIDR2_31_8							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES0_CTICIDR2_31_8							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRMBL_2							
R/W							
5h							

Table 14-9679. A53SS_APBADDR_CTI_CPU1_CTICIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR2_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_2	R/W	5h	Preamble. Must read as 0x05.

14.3.1.1.2.666 A53SS_APBADDR_CTI_CPU1_CTICIDR3 Register

1 A53SS_APBADDR_CTI_CPU1_CTICIDR3 Register (Offset = FFCh) [reset = B1h]

CTI Component Identification Register 3

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Table 14-9680. Instance Table

Instance Name	Physical Address
A53SS0	**0007 3014 0FFCh**

Figure 14-3211. A53SS_APBADDR_CTI_CPU1_CTICIDR3 Name Register

31	30	29	28	27	26	25	24
RES0_CTICIDR3_31_8							
R/W							
0h							
23	22	21	20	19	18	17	16
RES0_CTICIDR3_31_8							
R/W							
0h							
15	14	13	12	11	10	9	8
RES0_CTICIDR3_31_8							
R/W							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R/W							
B1h							

Table 14-9682. A53SS_APBADDR_CTI_CPU1_CTICIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES0_CTICIDR3_31_8	R/W	0h	Reserved, RES0.
7:0	PRMBL_3	R/W	B1h	Preamble. Must read as 0xB1.

14.3.2 M4FSS Registers

14.3.2.1 M4FSS_RAT_0 Registers

14.3.2.1.1 M4FSS_RAT_0 Summary Table

Table 14-9683. MCU_M4FSS0_RAT Registers, Base Address=05FF 0000h, Length=4096

Offset	Length	Register Name	M4FSS_RAT_0 Physical Address
0h	32	RAT_PID	05FF 0000h
4h	32	RAT_CONFIG	05FF 0004h
20h + formula	32	RAT_REGION_CTRL_j	05FF 0020h
24h + formula	32	RAT_REGION_BASE_j	05FF 0024h
28h + formula	32	RAT_REGION_TRANS_L_j	05FF 0028h
2Ch + formula	32	RAT_REGION_TRANS_U_j	05FF 002Ch
804h	32	RAT_DESTINATION_ID	05FF 0804h
820h	32	RAT_EXCEPTION_LOGGING_CONTROL	05FF 0820h
824h	32	RAT_EXCEPTION_LOGGING_HEADER0	05FF 0824h
828h	32	RAT_EXCEPTION_LOGGING_HEADER1	05FF 0828h
82Ch	32	RAT_EXCEPTION_LOGGING_DATA0	05FF 082Ch
830h	32	RAT_EXCEPTION_LOGGING_DATA1	05FF 0830h
834h	32	RAT_EXCEPTION_LOGGING_DATA2	05FF 0834h
838h	32	RAT_EXCEPTION_LOGGING_DATA3	05FF 0838h
840h	32	RAT_EXCEPTION_PEND_SET	05FF 0840h
844h	32	RAT_EXCEPTION_PEND_CLEAR	05FF 0844h
848h	32	RAT_EXCEPTION_ENABLE_SET	05FF 0848h
84Ch	32	RAT_EXCEPTION_ENABLE_CLEAR	05FF 084Ch
850h	32	RAT_EOI_REG	05FF 0850h

14.3.2.1.2 RAT_PID Register

RAT_PID Register (Offset = 0h) [reset = 66804100h]

Register Description: The Revision Register contains the major and minor revisions for the module.

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Table 14-9684. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0000h

Figure 14-3212. RAT_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		680h			
23	22	21	20	19	18	17	16
FUNC							
R							
680h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
8h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-9686. RAT_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: mod_g_rst_n
27:16	FUNC	R	680h	Module ID Reset Source: mod_g_rst_n
15:11	RTL	R	8h	RTL revision. Will vary depending on release. Reset Source: mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: mod_g_rst_n

14.3.2.1.3 RAT_CONFIG Register

RAT_CONFIG Register (Offset = 4h) [reset = 240108h]

Register Description: The Config Register contains the configuration values for the module.

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Table 14-9687. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0004h

Figure 14-3213. RAT_CONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_WIDTH</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">24h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDRS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">REGIONS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
</table>

Table 14-9689. RAT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	ADDR_WIDTH	R	24h	Number of address bits Reset Source: mod_g_rst_n
15:8	ADDRS	R	1h	Number of addresses Reset Source: mod_g_rst_n
7:0	REGIONS	R	8h	Number of regions Reset Source: mod_g_rst_n

14.3.2.1.4 RAT_REGION_CTRL_j Register

RAT_REGION_CTRL_j Register (Offset = 20h + formula) [reset = 0h]

Register Description: The Control for Region a

Formula = (j * 10h); where j = 0 to 7d

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Table 14-9690. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0020h + formula

Figure 14-3214. RAT_REGION_CTRL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">SIZE</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-9692. RAT_REGION_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the Region Reset Source: mod_g_rst_n
30:6	RESERVED	NONE	0h	Reserved
5:0	SIZE	R/W	0h	Size of the Region in Address Bits. 0 = 1 byte, 1 = 2B, 2 = 4B, 3 = 8B, etc. up to 32 = 4GB. Reset Source: mod_g_rst_n

14.3.2.1.5 RAT_REGION_BASE_j Register

RAT_REGION_BASE_j Register (Offset = 24h + formula) [reset = 0h]

Register Description: The Base Address for Region a. This is the source address for matching to a region.

Formula = (j * 10h); where j = 0 to 7d

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Table 14-9693. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0024h + formula

Figure 14-3215. RAT_REGION_BASE_j Name Register

31	30	29	28	27	26	25	24
BASE							
R/W							
0h							
23	22	21	20	19	18	17	16
BASE							
R/W							
0h							
15	14	13	12	11	10	9	8
BASE							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE							
R/W							
0h							

Table 14-9695. RAT_REGION_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size. Reset Source: mod_g_rst_n

14.3.2.1.6 RAT_REGION_TRANS_L_j Register

RAT_REGION_TRANS_L_j Register (Offset = 28h + formula) [reset = 0h]

Register Description: The Translated Lower Address Bits for Region a

Formula = (j * 10h); where j = 0 to 7d

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Table 14-9696. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0028h + formula

Figure 14-3216. RAT_REGION_TRANS_L_j Name Register

31	30	29	28	27	26	25	24
LOWER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOWER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOWER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOWER							
R/W							
0h							

Table 14-9698. RAT_REGION_TRANS_L_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOWER	R/W	0h	Translated Lower Address Bits for the Region. It must be aligned to the programmed size. Reset Source: mod_g_rst_n

14.3.2.1.7 RAT_REGION_TRANS_U_j Register

RAT_REGION_TRANS_U_j Register (Offset = 2Ch + formula) [reset = 0h]

Register Description: The Translated Upper Address Bits for Region a

Formula = (j * 10h); where j = 0 to 7d

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Table 14-9699. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 002Ch + formula

Figure 14-3217. RAT_REGION_TRANS_U_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				UPPER			
NONE				R/W			
0h				0h			

Table 14-9701. RAT_REGION_TRANS_U_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	UPPER	R/W	0h	Translated Upper Address Bits for the Region Reset Source: mod_g_rst_n

14.3.2.1.8 RAT_DESTINATION_ID Register

RAT_DESTINATION_ID Register (Offset = 804h) [reset = 0h]

Register Description: The Destination ID Register defines the destination ID value for error messages.

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Table 14-9702. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0804h

Figure 14-3218. RAT_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9704. RAT_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: mod_g_rst_n

14.3.2.1.9 RAT_EXCEPTION_LOGGING_CONTROL Register

RAT_EXCEPTION_LOGGING_CONTROL Register (Offset = 820h) [reset = 0h]

Register Description: The Exception Logging Control Register controls the exception logging.

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Table 14-9705. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0820h

Figure 14-3219. RAT_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-9707. RAT_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set. Reset Source: mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: mod_g_rst_n

14.3.2.1.10 RAT_EXCEPTION_LOGGING_HEADER0 Register

RAT_EXCEPTION_LOGGING_HEADER0 Register (Offset = 824h) [reset = 0h]

Register Description: The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-9708. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0824h

Figure 14-3220. RAT_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-9710. RAT_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 4 = RAT. Reset Source: mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: mod_g_rst_n

14.3.2.1.11 RAT_EXCEPTION_LOGGING_HEADER1 Register

RAT_EXCEPTION_LOGGING_HEADER1 Register (Offset = 828h) [reset = 0h]

Register Description: The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-9711. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0828h

Figure 14-3221. RAT_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9713. RAT_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: mod_g_rst_n
23:16	CODE	R	0h	Code. 1 = Boundary crossing error. Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.3.2.1.12 RAT_EXCEPTION_LOGGING_DATA0 Register

RAT_EXCEPTION_LOGGING_DATA0 Register (Offset = 82Ch) [reset = 0h]

Register Description: The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-9714. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 082Ch

Figure 14-3222. RAT_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-9716. RAT_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: mod_g_rst_n

14.3.2.1.13 RAT_EXCEPTION_LOGGING_DATA1 Register

RAT_EXCEPTION_LOGGING_DATA1 Register (Offset = 830h) [reset = 0h]

Register Description: The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-9717. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0830h

Figure 14-3223. RAT_EXCEPTION_LOGGING_DATA1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_H</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_H</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9719. RAT_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 12 bits. Reset Source: mod_g_rst_n

14.3.2.1.14 RAT_EXCEPTION_LOGGING_DATA2 Register

RAT_EXCEPTION_LOGGING_DATA2 Register (Offset = 834h) [reset = 0h]

Register Description: The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-9720. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0834h

Figure 14-3224. RAT_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-9722. RAT_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: mod_g_rst_n
12	READ	R	0h	Read. Reset Source: mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: mod_g_rst_n

Table 14-9722. RAT_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: mod_g_rst_n

14.3.2.1.15 RAT_EXCEPTION_LOGGING_DATA3 Register

RAT_EXCEPTION_LOGGING_DATA3 Register (Offset = 838h) [reset = 0h]

Register Description: The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

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Table 14-9723. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0838h

Figure 14-3225. RAT_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-9725. RAT_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: mod_g_rst_n

14.3.2.1.16 RAT_EXCEPTION_PEND_SET Register

RAT_EXCEPTION_PEND_SET Register (Offset = 840h) [reset = 0h]

Register Description: The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

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Table 14-9726. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0840h

Figure 14-3226. RAT_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-9728. RAT_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: mod_g_rst_n

14.3.2.1.17 RAT_EXCEPTION_PEND_CLEAR Register

RAT_EXCEPTION_PEND_CLEAR Register (Offset = 844h) [reset = 0h]

Register Description: The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

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Table 14-9729. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0844h

Figure 14-3227. RAT_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-9731. RAT_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: mod_g_rst_n

14.3.2.1.18 RAT_EXCEPTION_ENABLE_SET Register

RAT_EXCEPTION_ENABLE_SET Register (Offset = 848h) [reset = 0h]

Register Description: The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

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Table 14-9732. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0848h

Figure 14-3228. RAT_EXCEPTION_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-9734. RAT_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SET	R/W1TS	0h	Write a 1 to set the exception interrupt enable signal. Reset Source: mod_g_rst_n

14.3.2.1.19 RAT_EXCEPTION_ENABLE_CLEAR Register

RAT_EXCEPTION_ENABLE_CLEAR Register (Offset = 84Ch) [reset = 0h]

Register Description: The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

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Table 14-9735. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 084Ch

Figure 14-3229. RAT_EXCEPTION_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-9737. RAT_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_CLR	R/W1TC	0h	Write a 1 to clear the exception interrupt enable signal. Reset Source: mod_g_rst_n

14.3.2.1.20 RAT_EOI_REG Register

RAT_EOI_REG Register (Offset = 850h) [reset = 0h]

Register Description: EOI Register

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Table 14-9738. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_RAT	05FF 0850h

Figure 14-3230. RAT_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-9740. RAT_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register Reset Source: mod_g_rst_n

14.3.2.2 M4FSS_IRAM_0 Registers

14.3.2.2.1 M4FSS_IRAM_0 Summary Table

Table 14-9741. MCU_M4FSS0_blazar_iram Registers, Base Address=0500 0000h, Length=262144

Offset	Length	Register Name	M4FSS_IRAM_0 Physical Address
0h + formula	32	M4FSS_IRAM_0_BLAZAR_IRAM_RAM_REG_j	0500 0000h

14.3.2.2.2 M4FSS_IRAM_0_BLAZAR_IRAM_RAM_REG_j Register

M4FSS_IRAM_0_BLAZAR_IRAM_RAM_REG_j Register (Offset = 0h + formula) [reset = 0h]

Register Description: The RAM memory words provide memory mapped random access data storage.

Formula = (j * 4h); where j = 0 to 49151d

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Table 14-9742. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_blazar_iram	0500 0000h + formula

Figure 14-3231. M4FSS_IRAM_0_BLAZAR_IRAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-9744. M4FSS_IRAM_0_BLAZAR_IRAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: mod_g_rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: mod_g_rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: mod_g_rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: mod_g_rst_n

14.3.2.3 M4FSS_DRAM_0

M4FSS_DRAM_0

14.3.2.3.1 M4FSS_DRAM_0 Summaries

M4FSS_DRAM_0 Summaries

Table 14-9745. M4FSS_DRAM_0_IDRAM_SLV_RAM Registers, Base Address=0504 0000h, Length=65536

Offset	Length	Register Name	MCU_M4FSS0_DRAM_0 Physical Address
0h	32	M4FSS_DRAM_0_IDRAM_SLV_RAM_RAM_REG_J	0504 0000h + formula

14.3.2.3.2 M4FSS_DRAM_0 Registers

M4FSS_DRAM_0 Registers

14.3.2.3.2.1 M4FSS_DRAM_0_IDRAM_SLV_RAM_RAM_REG_j Register

1 M4FSS_DRAM_0_IDRAM_SLV_RAM_RAM_REG_j Register (Offset = 0h + formula) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

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Offset = (j * 4h); where j = 0 to 16383d

Table 14-9746. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_DRAM_0	0504 0000h + formula

Figure 14-3232. M4FSS_DRAM_0_IDRAM_SLV_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-9748. M4FSS_DRAM_0_IDRAM_SLV_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_mod_g_rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_mod_g_rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_mod_g_rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_mod_g_rst_n

14.3.2.4 M4FSS_ECC_AGGR_0

M4FSS_ECC_AGGR_0

14.3.2.4.1 M4FSS_ECC_AGGR_0 Summaries

M4FSS_ECC_AGGR_0 Summaries

Table 14-9749. ECC_AGGR Registers, Base Address=05FF 1000h, Length=1024

Offset	Length	Register Name	MCU_M4FSS0_ECC_AGGR_0 Physical Address
0h	32	ECC_AGGR_REV	05FF 1000h
8h	32	ECC_AGGR_VECTOR	05FF 1008h
Ch	32	ECC_AGGR_STAT	05FF 100Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	05FF 1010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	05FF 103Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	05FF 1040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	05FF 1080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	05FF 10C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	05FF 113Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	05FF 1140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	05FF 1180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	05FF 11C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	05FF 1200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	05FF 1204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	05FF 1208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	05FF 120Ch

14.3.2.4.2 M4FSS_ECC_AGGR_0 Registers

M4FSS_ECC_AGGR_0 Registers

14.3.2.4.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-9750. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1000h**

Figure 14-3233. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
5h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-9752. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.2.4.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-9753. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1008h**

Figure 14-3234. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-9755. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.2.4.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = Eh]

Misc Status

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Table 14-9756. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 100Ch**

Figure 14-3235. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">Eh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Eh</td></tr>
</table>

Table 14-9758. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	Eh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.2.4.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-9759. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1010h + formula**

Figure 14-3236. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-9761. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.2.4.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-9762. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 103Ch**

Figure 14-3237. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-9764. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.2.4.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9765. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1040h**

Figure 14-3238. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		ECCAGG_PEND	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_PEND	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_PEND	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_PEND	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_PEND	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_PEND
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_PEND	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_PEND	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_PEND	BLAZAR_RAT_EDC_CTRL_BUSECC_PEND	DRAM_BUSECC_PEND	IRAM_BUSECC_PEND	DRAM_RAMECC_PEND	IRAM_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9767. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
12	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_Ia2v_s_edc_ctrl_busecc_pend
11	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_Ia2v_d_edc_ctrl_busecc_pend
10	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_Ia2v_i_edc_ctrl_busecc_pend
9	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_sys_scr_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend

Table 14-9767. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_cbass_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
7	BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_cbass_blazar_scr_scr_blazar_cbass_blazar_scr_scr_edc_ctrl_busecc_pend
6	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_cbass_Iecc_s_p2p_bridge_Iecc_s_bridge_busecc_pend
5	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_cbass_vbusp_s_p2p_bridge_vbusp_s_bridge_busecc_pend
4	BLAZAR_RAT_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_rat_edc_ctrl_busecc_pend
3	DRAM_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for dram_busecc_pend
2	IRAM_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for iram_busecc_pend
1	DRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for dram_ramecc_pend
0	IRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for iram_ramecc_pend

14.3.2.4.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9768. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1080h**

Figure 14-3239. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED		ECCAGG_ENABLE_SET	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_ENABLE_SET	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_ENABLE_SET	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_ENABLE_SET	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_SET	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_SET
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_ENABLE_SET	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	BLAZAR_RAT_EDC_CTRL_BUSECC_ENABLE_SET	DRAM_BUSECC_ENABLE_SET	IRAM_BUSECC_ENABLE_SET	DRAM_RAMECC_ENABLE_SET	IRAM_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9770. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
12	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_Ia2v_s_edc_ctrl_busecc_pend
11	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_Ia2v_d_edc_ctrl_busecc_pend
10	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_Ia2v_i_edc_ctrl_busecc_pend

Table 14-9770. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_sys_scr_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
8	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_cbass_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
7	BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_cbass_blazar_scr_scr_blazar_cbass_blazar_scr_scr_edc_ctrl_busecc_pend
6	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_cbass_Iecc_s_p2p_bridge_Iecc_s_bridge_busecc_pend
5	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_cbass_vbusp_s_p2p_bridge_vbusp_s_bridge_busecc_pend
4	BLAZAR_RAT_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_rat_edc_ctrl_busecc_pend
3	DRAM_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dram_busecc_pend
2	IRAM_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for iram_busecc_pend
1	DRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dram_ramecc_pend
0	IRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for iram_ramecc_pend

14.3.2.4.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9771. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 10C0h**

Figure 14-3240. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		ECCAGG_ENABLE_CLR	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_ENABLE_CLR	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_ENABLE_CLR	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_ENABLE_CLR	BLAZAR_SYSSCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_CLR	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_CLR
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_ENABLE_CLR	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	BLAZAR_RAT_EDC_CTRL_BUSECC_ENABLE_CLR	DRAM_BUSECC_ENABLE_CLR	IRAM_BUSECC_ENABLE_CLR	DRAM_RAMECC_ENABLE_CLR	IRAM_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9773. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
12	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_Ia2v_s_edc_ctrl_busecc_pend
11	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_Ia2v_d_edc_ctrl_busecc_pend
10	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_Ia2v_i_edc_ctrl_busecc_pend

Table 14-9773. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_sys_scr_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
8	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_cbass_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
7	BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_cbass_blazar_scr_scr_blazar_cbass_blazar_scr_scr_edc_ctrl_busecc_pend
6	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_cbass_Iecc_s_p2p_bridge_Iecc_s_bridge_busecc_pend
5	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_cbass_vbusp_s_p2p_bridge_vbusp_s_bridge_busecc_pend
4	BLAZAR_RAT_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_rat_edc_ctrl_busecc_pend
3	DRAM_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dram_busecc_pend
2	IRAM_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for iram_busecc_pend
1	DRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dram_ramecc_pend
0	IRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for iram_ramecc_pend

14.3.2.4.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-9774. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 113Ch**

Figure 14-3241. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-9776. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.2.4.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9777. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1140h**

Figure 14-3242. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		ECCAGG_PEND	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_PEND	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_PEND	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_PEND	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_PEND	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_PEND
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_PEND	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_PEND	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_PEND	BLAZAR_RAT_EDC_CTRL_BUSECC_PEND	DRAM_BUSECC_PEND	IRAM_BUSECC_PEND	DRAM_RAMECC_PEND	IRAM_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9779. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
12	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_Ia2v_s_edc_ctrl_busecc_pend
11	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_Ia2v_d_edc_ctrl_busecc_pend
10	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_Ia2v_i_edc_ctrl_busecc_pend
9	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_sys_scr_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend

Table 14-9779. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_cbass_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
7	BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_cbass_blazar_scr_scr_blazar_cbass_blazar_scr_scr_edc_ctrl_busecc_pend
6	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_cbass_Iecc_s_p2p_bridge_Iecc_s_bridge_busecc_pend
5	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_cbass_vbusp_s_p2p_bridge_vbusp_s_bridge_busecc_pend
4	BLAZAR_RAT_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for blazar_rat_edc_ctrl_busecc_pend
3	DRAM_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for dram_busecc_pend
2	IRAM_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for iram_busecc_pend
1	DRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for dram_ramecc_pend
0	IRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for iram_ramecc_pend

14.3.2.4.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9780. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1180h**

Figure 14-3243. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		ECCAGG_ENABLE_SET	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_ENABLE_SET	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_ENABLE_SET	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_ENABLE_SET	BLAZAR_SYSSCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_SET	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_SET
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_ENABLE_SET	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	BLAZAR_RAT_EDC_CTRL_BUSECC_ENABLE_SET	DRAM_BUSECC_ENABLE_SET	IRAM_BUSECC_ENABLE_SET	DRAM_RAMECC_ENABLE_SET	IRAM_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9782. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
12	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_Ia2v_s_edc_ctrl_busecc_pend
11	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_Ia2v_d_edc_ctrl_busecc_pend
10	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_Ia2v_i_edc_ctrl_busecc_pend

Table 14-9782. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_sys_scr_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
8	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_cbass_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
7	BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_cbass_blazar_scr_scr_blazar_cbass_blazar_scr_scr_edc_ctrl_busecc_pend
6	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_cbass_Iecc_s_p2p_bridge_Iecc_s_bridge_busecc_pend
5	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_cbass_vbusp_s_p2p_bridge_vbusp_s_bridge_busecc_pend
4	BLAZAR_RAT_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for blazar_rat_edc_ctrl_busecc_pend
3	DRAM_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dram_busecc_pend
2	IRAM_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for iram_busecc_pend
1	DRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dram_ramecc_pend
0	IRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for iram_ramecc_pend

14.3.2.4.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9783. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 11C0h**

Figure 14-3244. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED		ECCAGG_ENABLE_CLR	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_ENABLE_CLR	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_ENABLE_CLR	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_ENABLE_CLR	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_CLR	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_CLR
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_ENABLE_CLR	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	BLAZAR_RAT_EDC_CTRL_BUSECC_ENABLE_CLR	DRAM_BUSECC_ENABLE_CLR	IRAM_BUSECC_ENABLE_CLR	DRAM_RAMECC_ENABLE_CLR	IRAM_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9785. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
12	BLAZAR_IA2V_S_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_Ia2v_s_edc_ctrl_busecc_pend
11	BLAZAR_IA2V_D_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_Ia2v_d_edc_ctrl_busecc_pend
10	BLAZAR_IA2V_I_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_Ia2v_i_edc_ctrl_busecc_pend

Table 14-9785. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	BLAZAR_SYS_SCR_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_sys_scr_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
8	BLAZAR_CBASS_VBUS_CLK_EDC_CTRL_CBASS_INT_VBUS_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_cbass_vbus_clk_edc_ctrl_cbass_int_vbus_busecc_pend
7	BLAZAR_CBASS_BLAZAR_SCR_SCR_BLAZAR_CBASS_BLAZAR_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_cbass_blazar_scr_scr_blazar_cbass_blazar_scr_scr_edc_ctrl_busecc_pend
6	BLAZAR_CBASS_IECC_S_P2P_BRIDGE_IECC_S_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_cbass_Iecc_s_p2p_bridge_Iecc_s_bridge_busecc_pend
5	BLAZAR_CBASS_VBUSP_S_P2P_BRIDGE_VBUSP_S_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_cbass_vbusp_s_p2p_bridge_vbusp_s_bridge_busecc_pend
4	BLAZAR_RAT_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for blazar_rat_edc_ctrl_busecc_pend
3	DRAM_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dram_busecc_pend
2	IRAM_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for iram_busecc_pend
1	DRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dram_ramecc_pend
0	IRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for iram_ramecc_pend

14.3.2.4.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-9786. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1200h**

Figure 14-3245. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-9788. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.2.4.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-9789. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1204h**

Figure 14-3246. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9791. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.2.4.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-9792. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 1208h**

Figure 14-3247. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-9794. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.2.4.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-9795. Instance Table

Instance Name	Physical Address
MCU_M4FSS0_ECC_AGGR_0	**05FF 120Ch**

Figure 14-3248. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-9797. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.3 R5FSS Registers

14.3.3.1 R5FSS_COMMON0

R5FSS_COMMON0

14.3.3.1.1 R5FSS_COMMON0 Summaries

R5FSS_COMMON0 Summaries

Table 14-9798. ECC_AGGR Registers, Base Address=3C01 0000h, Length=1024

Offset	Length	Register Name	R5FSS0_COMMON0 Physical Address	R5FSS1_COMMON0 Physical Address
0h	32	ECC_AGGR_REV	3C01 0000h	3C03 0000h
8h	32	ECC_AGGR_VECTOR	3C01 0008h	3C03 0008h
Ch	32	ECC_AGGR_STAT	3C01 000Ch	3C03 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3C01 0010h + formula	3C03 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3C01 003Ch	3C03 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3C01 0040h	3C03 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3C01 0080h	3C03 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3C01 00C0h	3C03 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3C01 013Ch	3C03 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3C01 0140h	3C03 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3C01 0180h	3C03 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3C01 01C0h	3C03 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3C01 0200h	3C03 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3C01 0204h	3C03 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	3C01 0208h	3C03 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3C01 020Ch	3C03 020Ch

Table 14-9799. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS Registers, Base Address=3C01 8000h, Length=256

Offset	Length	Register Name	R5FSS0_COMMON0 Physical Address	R5FSS1_COMMON0 Physical Address
0h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR	3C01 8000h	3C03 8000h
4h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS	3C01 8004h	3C03 8004h
8h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS	3C01 8008h	3C03 8008h
Ch	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS	3C01 800Ch	3C03 800Ch
10h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS	3C01 8010h	3C03 8010h
14h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS	3C01 8014h	3C03 8014h
18h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET	3C01 8018h	3C03 8018h

Table 14-9799. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS Registers, Base Address=3C01 8000h, Length=256 (continued)

Offset	Length	Register Name	R5FSS0_COMMON0 Physical Address	R5FSS1_COMMON0 Physical Address
1Ch	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR	3C01 801Ch	3C03 801Ch
20h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET	3C01 8020h	3C03 8020h
24h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR	3C01 8024h	3C03 8024h
40h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID	3C01 8040h	3C03 8040h

Table 14-9800. ECC_AGGR Registers, Base Address=3F00 D000h, Length=1024

Offset	Length	Register Name	R5FSS0_COMMON0 Physical Address	R5FSS1_COMMON0 Physical Address
0h	32	ECC_AGGR_REV	3F00 D000h	3F00 E000h
8h	32	ECC_AGGR_VECTOR	3F00 D008h	3F00 E008h
Ch	32	ECC_AGGR_STAT	3F00 D00Ch	3F00 E00Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3F00 D010h + formula	3F00 E010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3F00 D03Ch	3F00 E03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3F00 D040h	3F00 E040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3F00 D080h	3F00 E080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3F00 D0C0h	3F00 E0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3F00 D13Ch	3F00 E13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3F00 D140h	3F00 E140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3F00 D180h	3F00 E180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3F00 D1C0h	3F00 E1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3F00 D200h	3F00 E200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3F00 D204h	3F00 E204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	3F00 D208h	3F00 E208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3F00 D20Ch	3F00 E20Ch

14.3.3.1.2 R5FSS_COMMON0 Registers

R5FSS_COMMON0 Registers

14.3.3.1.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-9801. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D000h**
R5FSS1_COMMON0	**3F00 E000h**

Figure 14-3249. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-9803. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.3.1.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-9804. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D008h**
R5FSS1_COMMON0	**3F00 E008h**

Figure 14-3250. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9806. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.3.1.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Dh]

Misc Status

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Table 14-9807. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D00Ch**
R5FSS1_COMMON0	**3F00 E00Ch**

Figure 14-3251. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Dh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Dh							

Table 14-9809. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Dh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.3.1.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-9810. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D010h + formula**
R5FSS1_COMMON0	**3F00 E010h + formula**

Figure 14-3252. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-9812. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.3.1.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-9813. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D03Ch**
R5FSS1_COMMON0	**3F00 E03Ch**

Figure 14-3253. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-9815. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.3.1.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9816. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D040h**
R5FSS1_COMMON0	**3F00 E040h**

Figure 14-3254. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9818. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend

Table 14-9818. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.3.1.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9819. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D080h**
R5FSS1_COMMON0	**3F00 E080h**

Figure 14-3255. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9821. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend

Table 14-9821. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.3.1.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9822. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	3F00 D0C0h
R5FSS1_COMMON0	3F00 E0C0h

Figure 14-3256. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9824. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend

Table 14-9824. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.3.1.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-9825. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D13Ch**
R5FSS1_COMMON0	**3F00 E13Ch**

Figure 14-3257. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9827. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.3.1.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9828. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D140h**
R5FSS1_COMMON0	**3F00 E140h**

Figure 14-3258. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9830. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend

Table 14-9830. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.3.1.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9831. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D180h**
R5FSS1_COMMON0	**3F00 E180h**

Figure 14-3259. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9833. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend

Table 14-9833. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.3.1.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9834. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D1C0h**
R5FSS1_COMMON0	**3F00 E1C0h**

Figure 14-3260. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9836. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend

Table 14-9836. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.3.1.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-9837. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D200h**
R5FSS1_COMMON0	**3F00 E200h**

Figure 14-3261. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-9839. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.3.1.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-9840. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D204h**
R5FSS1_COMMON0	**3F00 E204h**

Figure 14-3262. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-9842. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.3.1.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-9843. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D208h**
R5FSS1_COMMON0	**3F00 E208h**

Figure 14-3263. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-9845. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.3.1.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-9846. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D20Ch**
R5FSS1_COMMON0	**3F00 E20Ch**

Figure 14-3264. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-9848. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.3.1.2.17 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register (Offset = 0h) [reset = 0h]

This register contains config bits to enable or disable change requests added to the IP

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Table 14-9849. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 8000h**
R5FSS1_COMMON0	**3C03 8000h**

Figure 14-3265. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							COMBINE_TCM_LOCKSTEP_MODE
NONE							R/W
0h							0h

Table 14-9851. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	COMBINE_TCM_LOCKSTEP_MODE	R/W	0h	this bit disables the CR logic to combine TCM in lockstep mode Reset Source: mod_g_rst_n

14.3.3.1.2.18 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register (Offset = 4h) [reset = 0h]

Status bits showing the PULSAR CPU0 EVNT_BUS single bit error counters

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Table 14-9852. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 8004h**
R5FSS1_COMMON0	**3C03 8004h**

Figure 14-3266. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EVNT_BUS8	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
EVNT_BUS7		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-9854. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	EVNT_BUS8	R	0h	Status bits showing the PULSAR CPU0 EVNT 8 single bit error counter. Reset Source: mod_g_rst_n
15:14	EVNT_BUS7	R	0h	Status bits showing the PULSAR CPU0 EVNT 7 single bit error counter. Reset Source: mod_g_rst_n
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU0 EVNT 6 single bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU0 EVNT 5 single bit error counter. Reset Source: mod_g_rst_n

Table 14-9854. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU0 EVNT 4 single bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU0 EVNT 3 single bit error counter. Reset Source: mod_g_rst_n
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU0 EVNT 2 single bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU0 EVNT 1 single bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU0 EVNT 0 single bit error counter. Reset Source: mod_g_rst_n

14.3.3.1.2.19 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register (Offset = 8h) [reset = 0h]

Status bits showing the PULSAR CPU1 EVNT_BUS single bit error counters

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Table 14-9855. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 8008h**
R5FSS1_COMMON0	**3C03 8008h**

Figure 14-3267. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EVNT_BUS8	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
EVNT_BUS7		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-9857. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	EVNT_BUS8	R	0h	Status bits showing the PULSAR CPU1 EVNT 8 single bit error counter. Reset Source: mod_g_rst_n
15:14	EVNT_BUS7	R	0h	Status bits showing the PULSAR CPU1 EVNT 7 single bit error counter. Reset Source: mod_g_rst_n
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU1 EVNT 6 single bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU1 EVNT 5 single bit error counter. Reset Source: mod_g_rst_n

Table 14-9857. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU1 EVNT 4 single bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU1 EVNT 3 single bit error counter. Reset Source: mod_g_rst_n
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU1 EVNT 2 single bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU1 EVNT 1 single bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU1 EVNT 0 single bit error counter. Reset Source: mod_g_rst_n

14.3.3.1.2.20 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register (Offset = Ch) [reset = 0h]

Status bits showing the PULSAR CPU0 EVNT_BUS multi bit error counters

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Table 14-9858. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 800Ch**
R5FSS1_COMMON0	**3C03 800Ch**

Figure 14-3268. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
NONE		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-9860. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU0 EVNT 6 multi bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU0 EVNT 5 multi bit error counter. Reset Source: mod_g_rst_n
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU0 EVNT 4 multi bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU0 EVNT 3 multi bit error counter. Reset Source: mod_g_rst_n

Table 14-9860. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU0 EVNT 2 multi bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU0 EVNT 1 multi bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU0 EVNT 0 multi bit error counter. Reset Source: mod_g_rst_n

14.3.3.1.2.21 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register (Offset = 10h) [reset = 0h]

Status bits showing the PULSAR CPU1 EVNT_BUS multi bit error counters

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Table 14-9861. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 8010h**
R5FSS1_COMMON0	**3C03 8010h**

Figure 14-3269. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
NONE		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-9863. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU1 EVNT 6 multi bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU1 EVNT 5 multi bit error counter. Reset Source: mod_g_rst_n
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU1 EVNT 4 multi bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU1 EVNT 3 multi bit error counter. Reset Source: mod_g_rst_n

Table 14-9863. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU1 EVNT 2 multi bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU1 EVNT 1 multi bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU1 EVNT 0 multi bit error counter. Reset Source: mod_g_rst_n

14.3.3.1.2.22 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register (Offset = 14h) [reset = 0h]

ESM status bits for the PULSAR EVNT BUS

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Table 14-9864. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 8014h**
R5FSS1_COMMON0	**3C03 8014h**

Figure 14-3270. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-9866. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R	0h	ESM status of CPU1 multiple bit errors on EVNT BUS Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R	0h	ESM status of CPU1 single bit errors on EVNT BUS Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R	0h	ESM status of CPU0 multiple bit errors on EVNT BUS Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R	0h	ESM status of CPU0 single bit errors on EVNT BUS Reset Source: mod_g_rst_n

14.3.3.1.2.23 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register (Offset = 18h) [reset = 0h]

SET the PULSAR EVNT BUS ESM events

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Table 14-9867. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	3C01 8018h
R5FSS1_COMMON0	3C03 8018h

Figure 14-3271. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9869. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TS	0h	SET CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TS	0h	SET CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TS	0h	SET CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TS	0h	SET CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.3.1.2.24 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register (Offset = 1Ch) [reset = 0h]

RESET the PULSAR EVNT BUS ESM events

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Table 14-9870. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 801Ch**
R5FSS1_COMMON0	**3C03 801Ch**

Figure 14-3272. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Name Register

31	30	29	28	27	26	25	24
CPU1_EB6_MULTIPLE_BIT_ERROR	CPU1_EB5_MULTIPLE_BIT_ERROR	CPU1_EB4_MULTIPLE_BIT_ERROR	CPU1_EB3_MULTIPLE_BIT_ERROR	CPU1_EB2_MULTIPLE_BIT_ERROR	CPU1_EB1_MULTIPLE_BIT_ERROR	CPU1_EB0_MULTIPLE_BIT_ERROR	CPU1_EB8_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_EB7_SINGLE_BIT_ERROR	CPU1_EB6_SINGLE_BIT_ERROR	CPU1_EB5_SINGLE_BIT_ERROR	CPU1_EB4_SINGLE_BIT_ERROR	CPU1_EB3_SINGLE_BIT_ERROR	CPU1_EB2_SINGLE_BIT_ERROR	CPU1_EB1_SINGLE_BIT_ERROR	CPU1_EB0_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_EB6_MULTIPLE_BIT_ERROR	CPU0_EB5_MULTIPLE_BIT_ERROR	CPU0_EB4_MULTIPLE_BIT_ERROR	CPU0_EB3_MULTIPLE_BIT_ERROR	CPU0_EB2_MULTIPLE_BIT_ERROR	CPU0_EB1_MULTIPLE_BIT_ERROR	CPU0_EB0_MULTIPLE_BIT_ERROR	CPU0_EB8_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_EB7_SINGLE_BIT_ERROR	CPU0_EB6_SINGLE_BIT_ERROR	CPU0_EB5_SINGLE_BIT_ERROR	CPU0_EB4_SINGLE_BIT_ERROR	CPU0_EB3_SINGLE_BIT_ERROR	CPU0_EB2_SINGLE_BIT_ERROR	CPU0_EB1_SINGLE_BIT_ERROR	CPU0_EB0_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9872. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU1_EB6_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 31 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
30	CPU1_EB5_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 30 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
29	CPU1_EB4_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 29 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
28	CPU1_EB3_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 28 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n

Table 14-9872. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CPU1_EB2_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 27 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
26	CPU1_EB1_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 26 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
25	CPU1_EB0_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 25 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
24	CPU1_EB8_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 24 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
23	CPU1_EB7_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 23 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
22	CPU1_EB6_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 22 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
21	CPU1_EB5_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 21 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
20	CPU1_EB4_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 20 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
19	CPU1_EB3_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 19 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
18	CPU1_EB2_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 18 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
17	CPU1_EB1_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 17 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
16	CPU1_EB0_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 16 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
15	CPU0_EB6_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 15 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
14	CPU0_EB5_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 14 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
13	CPU0_EB4_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 13 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
12	CPU0_EB3_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 12 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
11	CPU0_EB2_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 11 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
10	CPU0_EB1_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 10 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
9	CPU0_EB0_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 9 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
8	CPU0_EB8_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 8 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
7	CPU0_EB7_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 7 SINGLE BIT Error Counter Reset Source: mod_g_rst_n

Table 14-9872. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CPU0_EB6_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 6 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
5	CPU0_EB5_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 5 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
4	CPU0_EB4_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 4 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
3	CPU0_EB3_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 3 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
2	CPU0_EB2_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 2 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
1	CPU0_EB1_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 1 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
0	CPU0_EB0_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 0 SINGLE BIT Error Counter Reset Source: mod_g_rst_n

14.3.3.1.2.25 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register (Offset = 20h) [reset = 0h]

MASK the PULSAR EVNT BUS ESM events

Return to Summary Table

Table 14-9873. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 8020h**
R5FSS1_COMMON0	**3C03 8020h**

Figure 14-3273. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>CPU1_MULTIPLE_BIT_ERROR</td><td>CPU1_SINGLE_BIT_ERROR</td><td>CPU0_MULTIPLE_BIT_ERROR</td><td>CPU0_SINGLE_BIT_ERROR</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9875. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TS	0h	MASK CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TS	0h	MASK CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TS	0h	MASK CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TS	0h	MASK CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.3.1.2.26 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register (Offset = 24h) [reset = 0h]

UNMASK the PULSAR EVNT BUS ESM events

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Table 14-9876. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 8024h**
R5FSS1_COMMON0	**3C03 8024h**

Figure 14-3274. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>CPU1_MULTIPLE_BIT_ERROR</td><td>CPU1_SINGLE_BIT_ERROR</td><td>CPU0_MULTIPLE_BIT_ERROR</td><td>CPU0_SINGLE_BIT_ERROR</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9878. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.3.1.2.27 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register

1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register (Offset = 40h) [reset = 60801904h]

Module ID register

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Table 14-9879. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3C01 8040h**
R5FSS1_COMMON0	**3C03 8040h**

Figure 14-3275. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6080h							
23	22	21	20	19	18	17	16
MODID							
R							
6080h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
3h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		4h					

Table 14-9881. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6080h	Module ID field Reset Source: mod_g_rst_n
15:11	REVRTL	R	3h	RTL revision. Will vary depending on release Reset Source: mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	REVMIN	R	4h	Minor revision Reset Source: mod_g_rst_n

14.3.3.1.2.28 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-9882. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D000h**
R5FSS1_COMMON0	**3F00 E000h**

Figure 14-3276. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">5h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-9884. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.3.1.2.29 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-9885. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D008h**
R5FSS1_COMMON0	**3F00 E008h**

Figure 14-3277. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9887. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.3.1.2.30 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Dh]

Misc Status

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Table 14-9888. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D00Ch**
R5FSS1_COMMON0	**3F00 E00Ch**

Figure 14-3278. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Dh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Dh							

Table 14-9890. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Dh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.3.1.2.31 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-9891. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D010h + formula**
R5FSS1_COMMON0	**3F00 E010h + formula**

Figure 14-3279. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-9893. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.3.1.2.32 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-9894. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D03Ch**
R5FSS1_COMMON0	**3F00 E03Ch**

Figure 14-3280. ECC_AGGR_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9896. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.3.1.2.33 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9897. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D040h**
R5FSS1_COMMON0	**3F00 E040h**

Figure 14-3281. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9899. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend

Table 14-9899. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.3.1.2.34 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9900. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D080h**
R5FSS1_COMMON0	**3F00 E080h**

Figure 14-3282. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9902. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend

Table 14-9902. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.3.1.2.35 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9903. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D0C0h**
R5FSS1_COMMON0	**3F00 E0C0h**

Figure 14-3283. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9905. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend

Table 14-9905. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.3.1.2.36 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-9906. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D13Ch**
R5FSS1_COMMON0	**3F00 E13Ch**

Figure 14-3284. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-9908. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.3.1.2.37 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9909. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D140h**
R5FSS1_COMMON0	**3F00 E140h**

Figure 14-3285. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9911. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend

Table 14-9911. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.3.1.2.38 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9912. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D180h**
R5FSS1_COMMON0	**3F00 E180h**

Figure 14-3286. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9914. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend

Table 14-9914. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.3.1.2.39 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9915. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D1C0h**
R5FSS1_COMMON0	**3F00 E1C0h**

Figure 14-3287. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9917. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend

Table 14-9917. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.3.1.2.40 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-9918. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D200h**
R5FSS1_COMMON0	**3F00 E200h**

Figure 14-3288. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-9920. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.3.1.2.41 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-9921. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D204h**
R5FSS1_COMMON0	**3F00 E204h**

Figure 14-3289. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-9923. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.3.1.2.42 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-9924. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D208h**
R5FSS1_COMMON0	**3F00 E208h**

Figure 14-3290. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-9926. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.3.1.2.43 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-9927. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	**3F00 D20Ch**
R5FSS1_COMMON0	**3F00 E20Ch**

Figure 14-3291. ECC_AGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-9929. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.4 R5FSS_VIM Registers

14.3.4.1 R5FSS_VIM Registers

Table 14-6640 lists the memory-mapped registers for the R5FSS_VIM module. All register offset addresses not listed in Table 14-6640 should be considered as reserved locations and the register contents should not be modified.

Table 14-9930. R5FSS_VIM Instances

Instance	Base Address
R5FSS_VIC_CFG	2FFF 0000h(1)

(1) R5FSS0/1 private memory-mapped register space. This region is only accessible by its associated R5F core; it is not accessible by any other SoC initiator. The base address is the same for each CPU view inside R5FSS0/1.

Table 14-9931. R5FSS_VIM Registers

Offset	Acronym	Register Name	R5FSS_VIC_CFG Physical Address
0h	R5FSS_VIM_PID	Revision register	2FFF 0000h
4h	R5FSS_VIM_INFO	Info register	2FFF 0004h
8h	R5FSS_VIM_PRIIRQ	Prioritized IRQ register	2FFF 0008h
Ch	R5FSS_VIM_PRIFIQ	Prioritized FIQ register	2FFF 000Ch
10h	R5FSS_VIM_IRQGSTS	IRQ group status register	2FFF 0010h
14h	R5FSS_VIM_FIQGSTS	FIQ group status register	2FFF 0014h
18h	R5FSS_VIM_IRQVEC	IRQ vector address register	2FFF 0018h
1Ch	R5FSS_VIM_FIQVEC	FIQ vector address register	2FFF 001Ch
20h	R5FSS_VIM_ACTIRQ	Active IRQ register	2FFF 0020h
24h	R5FSS_VIM_ACTFIQ	Active FIQ register	2FFF 0024h
30h	R5FSS_VIM_DEDVEC	DED vector address register	2FFF 0030h
400h + formula	R5FSS_VIM_RAW_j	Raw status/set register	2FFF 0400h + formula
404h + formula	R5FSS_VIM_STS_j	Interrupt enable status/clear register	2FFF 0404h + formula
408h + formula	R5FSS_VIM_INTR_EN_SET_j	Interrupt enable set register	2FFF 0408h + formula
40Ch + formula	R5FSS_VIM_INTR_EN_CLR_j	Interrupt enabled clear register	2FFF 040Ch + formula
410h + formula	R5FSS_VIM_IRQSTS_j	IRQ interrupt enable status/clear register	2FFF 0410h + formula
414h + formula	R5FSS_VIM_FIQSTS_j	FIQ interrupt enable status/clear register	2FFF 0414h + formula
418h + formula	R5FSS_VIM_INTMAP_j	Interrupt map register	2FFF 0418h + formula
41Ch + formula	R5FSS_VIM_INTTYPE_j	Interrupt type register	2FFF 041Ch + formula
1000h + formula	R5FSS_VIM_PRI_INT_j	Interrupt priority register	2FFF 1000h + formula
2000h + formula	R5FSS_VIM_VEC_INT_j	Interrupt vector register	2FFF 2000h + formula

1 R5FSS_VIM_PID Register (Offset = 0h) [reset = 60900001h]

R5FSS_VIM_PID is shown in Figure 14-3292 and described in Table 14-6642.

Return to Summary Table.

This register contains the major and minor revisions for the module.

Table 14-9932. R5FSS_VIM_PID Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0000h

Figure 14-3292. R5FSS_VIM_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-60900001h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9934. R5FSS_VIM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	60900001h	TI internal data. Identifies revision of peripheral.

2 R5FSS_VIM_INFO Register (Offset = 4h) [reset = 200h]

R5FSS_VIM_INFO is shown in Figure 14-3293 and described in Table 14-6644.

Return to Summary Table.

This contains information about the configuration of the R5FSS_VIM.

Table 14-9935. R5FSS_VIM_INFO Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0004h

Figure 14-3293. R5FSS_VIM_INFO Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="21">RESERVED</td><td colspan="11">INTERRUPTS</td></tr>
<tr><td colspan="21">R-0h</td><td colspan="11">R-200h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9937. R5FSS_VIM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
10-0	INTERRUPTS	R	200h	Indicates the number of interrupts supported by the VIM.

3 R5FSS_VIM_PRIIRQ Register (Offset = 8h) [reset = 0h]

R5FSS_VIM_PRIIRQ is shown in Figure 14-3294 and described in Table 14-6646.

Return to Summary Table.

This register contains the number of the highest priority pending IRQ.

Table 14-9938. R5FSS_VIM_PRIIRQ Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0008h

Figure 14-3294. R5FSS_VIM_PRIIRQ Register

31	30	29	28	27	26	25	24
VALID	RESERVED						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED				PRI			
R-0h				R-0h			
15	14	13	12	11	10	9	8
RESERVED						NUM	
R-0h						R-0h	
7	6	5	4	3	2	1	0
NUM							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9940. R5FSS_VIM_PRIIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	This field indicates if the NUM field of this register is valid. 0h = NUM field is invalid (no pending IRQ interrupts) 1h = NUM field is valid (pending IRQ interrupt)
30-20	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
19-16	PRI	R	0h	This field indicates the priority of the pending IRQ interrupt. 0h = Highest priority ... Fh = Lowest priority This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.
15-10	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.

Table 14-9940. R5FSS_VIM_PRIIRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NUM	R	0h	This field indicates the interrupt number of the pending IRQ interrupt with the highest priority. 0h = Interrupt 0 1h = Interrupt 1 ... 3FFh = Interrupt 1023 (Note: The highest supported value is device-specific.) This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.

4 R5FSS_VIM_PRIFIQ Register (Offset = Ch) [reset = 0h]

R5FSS_VIM_PRIFIQ is shown in Figure 14-3295 and described in Table 14-6648.

Return to Summary Table.

This register contains the number of the highest priority pending FIQ.

Table 14-9941. R5FSS_VIM_PRIFIQ Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 000Ch

Figure 14-3295. R5FSS_VIM_PRIFIQ Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>VALID</td><td colspan="7">RESERVED</td></tr>
<tr><td>R-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PRI</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">NUM</td></tr>
<tr><td colspan="6">R-0h</td><td colspan="2">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9943. R5FSS_VIM_PRIFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	This field indicates if the NUM field of this register is valid. 0h = NUM field is invalid (no pending FIQ interrupts) 1h = NUM field is valid (pending FIQ interrupt)
30-20	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
19-16	PRI	R	0h	This field indicates the priority of the pending FIQ interrupt. 0h = Highest priority ... Fh = Lowest priority This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.
15-10	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.

Table 14-9943. R5FSS_VIM_PRIFIQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NUM	R	0h	This field indicates the interrupt number of the pending FIQ interrupt with the highest priority. 0h = Interrupt 0 1h = Interrupt 1 ... 3FFh = Interrupt 1023 (Note: The highest supported value is device-specific.) This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.

5 R5FSS_VIM_IRQGSTS Register (Offset = 10h) [reset = 0h]

R5FSS_VIM_IRQGSTS is shown in Figure 14-3296 and described in Table 14-6650.

Return to Summary Table.

This register indicates which groups of interrupts have pending, unmasked IRQ interrupts.

Table 14-9944. R5FSS_VIM_IRQGSTS Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0010h

Figure 14-3296. R5FSS_VIM_IRQGSTS Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">STS</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9946. R5FSS_VIM_IRQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R	0h	This field indicates that one or more interrupts in group M are mapped to IRQ, unmasked, and pending. Bit 0 corresponds to group 0, bit 1 corresponds to group 1, etc. The interrupts associated with each group are [(M*32)+31:M*32]

6 R5FSS_VIM_FIQGSTS Register (Offset = 14h) [reset = 0h]

R5FSS_VIM_FIQGSTS is shown in Figure 14-3297 and described in Table 14-6652.

Return to Summary Table.

This register indicates which groups of interrupts have pending, unmasked FIQ interrupts.

Table 14-9947. R5FSS_VIM_FIQGSTS Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0014h

Figure 14-3297. R5FSS_VIM_FIQGSTS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9949. R5FSS_VIM_FIQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R	0h	This field indicates that one or more interrupts in group M are mapped to FIQ, unmasked, and pending. Bit 0 corresponds to group 0, bit 1 corresponds to group 1, etc. The interrupts associated with each group are [(M*32)+31:M*32]

7 R5FSS_VIM_IRQVEC Register (Offset = 18h) [reset = 0h]

R5FSS_VIM_IRQVEC is shown in Figure 14-3298 and described in Table 14-6654.

Return to Summary Table.

This register contains the 32-bit interrupt vector address of the currently pending IRQ.

Table 14-9950. R5FSS_VIM_IRQVEC Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0018h

Figure 14-3298. R5FSS_VIM_IRQVEC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														RESERVED	
R-0h																														R-0h	

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9952. R5FSS_VIM_IRQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R	0h	This field contains the upper 30 bits of the 32-bit interrupt vector address (addresses must be 32-bit aligned) of the currently pending highest priority IRQ (as indicated by the R5FSS_VIM_PRIIRQ[9-0] NUM field). Reading this register returns the interrupt vector address of the pending IRQ with the highest priority. It also has the following effects: - Mask all IRQ interrupts of an equivalent or lower priority - De-asserts the IRQn signal - De-asserts the coreN_IRQADDRV signal (if set) - Loads R5FSS_VIM_ACTIRQ Writing any value to this register will not alter its contents, but will have the following effect: - Remove the mask on all IRQ priorities This field is only valid if the R5FSS_VIM_PRIIRQ[31] VALID flag is set.
1-0	RESERVED	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. (Vector addresses must be 32-bit aligned.)

8 R5FSS_VIM_FIQVEC Register (Offset = 1Ch) [reset = 0h]

R5FSS_VIM_FIQVEC is shown in Figure 14-3299 and described in Table 14-6656.

Return to Summary Table.

This register contains the 32-bit interrupt vector address of the currently pending FIQ.

Table 14-9953. R5FSS_VIM_FIQVEC Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 001Ch

Figure 14-3299. R5FSS_VIM_FIQVEC Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="30">ADDR</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="30">R-0h</td><td colspan="2">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9955. R5FSS_VIM_FIQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R	0h	This field contains the upper 30 bits of the 32-bit interrupt vector address (addresses must be 32-bit aligned) of the currently pending highest priority FIQ (as indicated by the R5FSS_VIM_PRIFIQ[9-0] NUM field). Reading this register returns the interrupt vector address of the pending FIQ with the highest priority. It also has the following effects: - Mask all FIQ interrupts of an equivalent or lower priority - De-asserts the FIQn signal - Loads R5FSS_VIM_ACTFIQ Writing any value to this register will not alter its contents, but will have the following effect: - Remove the mask on all FIQ priorities This field is only valid if the R5FSS_VIM_PRIFIQ[31] VALID flag is set.
1-0	RESERVED	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. (Vector addresses must be 32-bit aligned.)

9 R5FSS_VIM_ACTIRQ Register (Offset = 20h) [reset = 0h]

R5FSS_VIM_ACTIRQ is shown in Figure 14-3300 and described in Table 14-6658.

Return to Summary Table.

This register contains the number of the active IRQ.

Table 14-9956. R5FSS_VIM_ACTIRQ Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0020h

Figure 14-3300. R5FSS_VIM_ACTIRQ Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>VALID</td><td colspan="7">RESERVED</td></tr>
<tr><td>R-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PRI</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">NUM</td></tr>
<tr><td colspan="6">R-0h</td><td colspan="2">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9958. R5FSS_VIM_ACTIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	This field indicates if the NUM field of this register is valid. This field is set whenever the R5FSS_VIM_IRQVEC is read. It is cleared whenever the R5FSS_VIM_IRQVEC is written. 0h = NUM field is invalid (no active IRQ interrupts) 1h = NUM field is valid (active IRQ interrupt)
30-20	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
19-16	PRI	R	0h	This field indicates the priority of the active IRQ interrupt. 0h = Highest priority ... Fh = Lowest priority This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.
15-10	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.

Table 14-9958. R5FSS_VIM_ACTIRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NUM	R	0h	This field indicates the interrupt number of the active IRQ interrupt. This field is loaded with the value from the R5FSS_VIM_PRIIRQ whenever the R5FSS_VIM_IRQVEC is read. 0h = Interrupt 0 1h = Interrupt 1 … 3FFh = Interrupt 1023 (Note: The highest supported value is device-specific.) This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.

10 R5FSS_VIM_ACTFIQ Register (Offset = 24h) [reset = 0h]

R5FSS_VIM_ACTFIQ is shown in Figure 14-3301 and described in Table 14-6660.

Return to Summary Table.

This register contains the number of the active FIQ.

Table 14-9959. R5FSS_VIM_ACTFIQ Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0024h

Figure 14-3301. R5FSS_VIM_ACTFIQ Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>VALID</td><td colspan="7">RESERVED</td></tr>
<tr><td>R-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PRI</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">NUM</td></tr>
<tr><td colspan="6">R-0h</td><td colspan="2">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-9961. R5FSS_VIM_ACTFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	This field indicates if the NUM field of this register is valid. This field is set whenever the R5FSS_VIM_PRIFIQ is read. It is cleared whenever the R5FSS_VIM_FIQVEC is written. 0h = NUM field is invalid (no active FIQ interrupts) 1h = NUM field is valid (active FIQ interrupt)
30-20	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
19-16	PRI	R	0h	This field indicates the priority of the active FIQ interrupt. 0h = Highest priority ... Fh = Lowest priority This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.
15-10	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.

Table 14-9961. R5FSS_VIM_ACTFIQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NUM	R	0h	This field indicates the interrupt number of the active FIQ interrupt. This field is loaded with the value from the R5FSS_VIM_PRIFIQ whenever the R5FSS_VIM_FIQVEC is read. 0h = Interrupt 0 1h = Interrupt 1 … 3FFh = Interrupt 1023 (Note: The highest supported value is device-specific.) This field is only valid if the VALID flag of this register is set. Otherwise the value is unpredictable.

11 R5FSS_VIM_DEDVEC Register (Offset = 30h) [reset = 0h]

R5FSS_VIM_DEDVEC is shown in Figure 14-3302 and described in Table 14-6662.

Return to Summary Table.

This register contains the 32-bit interrupt vector address to be used as a default in case of a DED error in any of the vectors.

Table 14-9962. R5FSS_VIM_DEDVEC Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0030h

Figure 14-3302. R5FSS_VIM_DEDVEC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														RESERVED	
R/W-0h																														R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-9964. R5FSS_VIM_DEDVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R/W	0h	This field contains the upper 30 bits of the 32-bit interrupt vector address (the address must be 32-bit aligned) of an interrupt to be used if an uncorrectable double-bit error (DED) is detected in any of the interrupt vector addresses. If there is a DED, both the R5FSS_VIM_IRQVEC and R5FSS_VIM_FIQVEC registers (along with the VECADDR output) will be populated with the value in this field instead of their normal vector. - ECC Aggregator will indicate where there was a DED. Software may go correct that one location. - Software may keep an ISR at the DED vector which corrects the vectors or otherwise deals with the scenario. - This mechanism is provided because there is no way to indicate on the coreN_IRQADDR to the CPU that the vector is invalid, and it is undesirable to have the CPU jump to a random address.
1-0	RESERVED	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. (Vector addresses must be 32-bit aligned.)

12 R5FSS_VIM_RAW_j Register (Offset = 400h + formula) [reset = 0h]

R5FSS_VIM_RAW_j is shown in Figure 14-3303 and described in Table 14-6664.

Return to Summary Table.

This register indicates the raw status of the events in group M.

Offset = 400h + (j * 20h); where j = 0h to Fh.

Table 14-9965. R5FSS_VIM_RAW_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0400h + formula

Figure 14-3303. R5FSS_VIM_RAW_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS																															
R/W1S-0h																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-9967. R5FSS_VIM_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R/W1S	0h	This is the raw status of the events in group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Inactive Read 1h = Active/pending Write 0h = No effect Write 1h = Set to interrupt raw status

13 R5FSS_VIM_STS_j Register (Offset = 404h + formula) [reset = 0h]

R5FSS_VIM_STS_j is shown in Figure 14-3304 and described in Table 14-6666.

Return to Summary Table.

This register indicates the masked status of the events in group M.

Offset = 404h + (j * 20h); where j = 0h to Fh.

Table 14-9968. R5FSS_VIM_STS_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0404h + formula

Figure 14-3304. R5FSS_VIM_STS_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-9970. R5FSS_VIM_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This is the masked status of the events in group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Inactive or disabled Read 1h = Active/pending and enabled Write 0h = No effect Write 1h = Clear interrupt raw status

14 R5FSS_VIM_INTR_EN_SET_j Register (Offset = 408h + formula) [reset = 0h]

R5FSS_VIM_INTR_EN_SET_j is shown in Figure 14-3305 and described in Table 14-6668.

Return to Summary Table.

This register is used to enable the mask for the events in group M.

Offset = 408h + (j * 20h); where j = 0h to Fh.

Table 14-9971. R5FSS_VIM_INTR_EN_SET_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0408h + formula

Figure 14-3305. R5FSS_VIM_INTR_EN_SET_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1S-0h																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-9973. R5FSS_VIM_INTR_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1S	0h	This field is used to enable the mask of events in group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Disabled Read 1h = Enabled Write 0h = No effect Write 1h = Set enable

15 R5FSS_VIM_INTR_EN_CLR_j Register (Offset = 40Ch + formula) [reset = 0h]

R5FSS_VIM_INTR_EN_CLR_j is shown in Figure 14-3306 and described in Table 14-6670.

Return to Summary Table.

This register is used to disable the mask for the events in group M.

Offset = 40Ch + (j * 20h); where j = 0h to Fh.

Table 14-9974. R5FSS_VIM_INTR_EN_CLR_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 040Ch + formula

Figure 14-3306. R5FSS_VIM_INTR_EN_CLR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-9976. R5FSS_VIM_INTR_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This field is used to disable the mask of events in group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Disabled Read 1h = Enabled Read 0h = No effect Read 1h = Clear enable

16 R5FSS_VIM_IRQSTS_j Register (Offset = 410h + formula) [reset = 0h]

R5FSS_VIM_IRQSTS_j is shown in Figure 14-3307 and described in Table 14-6672.

Return to Summary Table.

This register indicates the masked status of the events in Group M that are also mapped as IRQs.

Offset = 410h + (j * 20h); where j = 0h to Fh.

Table 14-9977. R5FSS_VIM_IRQSTS_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0410h + formula

Figure 14-3307. R5FSS_VIM_IRQSTS_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-9979. R5FSS_VIM_IRQSTS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This is the masked status of the events in group M that are mapped to IRQ. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Inactive, disabled, or not an IRQ Read 1h = Active/pending, enabled, and IRQ Write 0h = No effect Write 1h = Clear interrupt raw status (if IRQ)

17 R5FSS_VIM_FIQSTS_j Register (Offset = 414h + formula) [reset = 0h]

R5FSS_VIM_FIQSTS_j is shown in Figure 14-3308 and described in Table 14-6674.

Return to Summary Table.

This register indicates the masked status of the events in group M that are also mapped as FIQs.

Offset = 414h + (j * 20h); where j = 0h to Fh.

Table 14-9980. R5FSS_VIM_FIQSTS_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0414h + formula

Figure 14-3308. R5FSS_VIM_FIQSTS_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">MSK</td></tr>
<tr><td colspan="32">R/W1C-0h</td></tr>
</table>

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-9982. R5FSS_VIM_FIQSTS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This is the masked status of the events in group M that are mapped to FIQ. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). Read 0h = Inactive, disabled, or not an FIQ Read 1h = Active/pending, enabled, and FIQ Write 0h = No effect Write 1h = Clear interrupt raw status (if FIQ)

18 R5FSS_VIM_INTMAP_j Register (Offset = 418h + formula) [reset = 0h]

R5FSS_VIM_INTMAP_j is shown in Figure 14-3309 and described in Table 14-6676.

Return to Summary Table.

This register is used to map interrupts as IRQ or FIQ.

Offset = 418h + (j * 20h); where j = 0h to Fh.

Table 14-9983. R5FSS_VIM_INTMAP_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 0418h + formula

Figure 14-3309. R5FSS_VIM_INTMAP_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-9985. R5FSS_VIM_INTMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). 0h = IRQ interrupt (default) 1h = FIQ interrupt

19 R5FSS_VIM_INTTYPE_j Register (Offset = 41Ch + formula) [reset = 0h]

R5FSS_VIM_INTTYPE_j is shown in Figure 14-3310 and described in Table 14-6678.

Return to Summary Table.

This register indicates whether an interrupt is a pulse or level source.

Offset = 41Ch + (j * 20h); where j = 0h to Fh.

Table 14-9986. R5FSS_VIM_INTTYPE_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 041Ch + formula

Figure 14-3310. R5FSS_VIM_INTTYPE_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">MSK</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-9988. R5FSS_VIM_INTTYPE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. Each bit corresponds to event Q, where Q = M*32+bit (example: bit 0 is event M*32+0, bit 1 is M*32+1, etc). 0h = Level (default) 1h = Pulse Note: This is only informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event. The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level.

20 R5FSS_VIM_PRI_INT_j Register (Offset = 1000h + formula) [reset = 0h]

R5FSS_VIM_PRI_INT_j is shown in Figure 14-3311 and described in Table 14-6680.

Return to Summary Table.

This register is used to set the priority of interrupt Q.

Offset = 1000h + (j * 4h); where j = 0h to FFh.

Table 14-9989. R5FSS_VIM_PRI_INT_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 1000h + formula

Figure 14-3311. R5FSS_VIM_PRI_INT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												VAL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-9991. R5FSS_VIM_PRI_INT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved. Reads return 0. Writes have no effect.
3-0	VAL	R/W	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration. 0h = Highest priority … Fh = Lowest priority (default)

21 R5FSS_VIM_VEC_INT_j Register (Offset = 2000h + formula) [reset = 0h]

R5FSS_VIM_VEC_INT_j is shown in Figure 14-3312 and described in Table 14-6682.

Return to Summary Table.

This register contains the vector address associated with interrupt Q.

Offset = 2000h + (j * 4h); where j = 0h to FFh.

Table 14-9992. R5FSS_VIM_VEC_INT_j Instances

Instance	Physical Address
R5FSS_VIC_CFG	2FFF 2000h + formula

Figure 14-3312. R5FSS_VIM_VEC_INT_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="30">VAL</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="30">R/W-0h</td><td colspan="2">R-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-9994. R5FSS_VIM_VEC_INT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	VAL	R/W	0h	These are the upper 30 bits of the 32-bit vector address associated with interrupt Q. It is the address that will be reflected in the R5FSS_VIM_IRQVEC or R5FSS_VIM_FIQVEC and the VECADDR output when interrupt Q is the active interrupt. Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new vector address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed. Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1-0	RESERVED	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. (Vector addresses must be 32-bit aligned.)

14.3.5 R5FSS_RAT

14.3.5.1 R5FSS_RAT Registers

Table 14-6684 lists the memory-mapped registers for the R5FSS_RAT. All register offset addresses not listed in Table 14-6684 should be considered as reserved locations and the register contents should not be modified.

Table 14-9995. R5FSS_RAT Instances

Instance	Base Address
R5FSS_RAT_CFG	2FFE 0000h(1)

(1) R5FSS0/1 private memory-mapped register space. This region is only accessible by its associated R5F core; it is not accessible by any other SoC initiator. The base address is the same for each CPU view inside R5FSS0/1.

Table 14-9996. R5FSS_RAT Registers

Offset	Acronym	Register Name	R5FSS_RAT_CFG Physical Address
0h	R5FSS_RAT_PID	Revision register	2FFE 0000h
4h	R5FSS_RAT_CONFIG	Config register	2FFE 0004h
20h + formula	R5FSS_RAT_CTRL_j	Region control register	2FFE 0020h + formula
24h + formula	R5FSS_RAT_BASE_j	Region base register	2FFE 0024h + formula
28h + formula	R5FSS_RAT_TRANS_L_j	Region translated lower address register	2FFE 0028h + formula
2Ch + formula	R5FSS_RAT_TRANS_U_j	Region translated upper address register	2FFE 002Ch + formula
804h	R5FSS_RAT_DESTINATION_ID	Destination ID register	2FFE 0804h
820h	R5FSS_RAT_EXCEPTION_LOGGING_CONTROL	Exception logging control register	2FFE 0820h
824h	R5FSS_RAT_EXCEPTION_LOGGING_HEADER0	Exception logging header 0 register	2FFE 0824h
828h	R5FSS_RAT_EXCEPTION_LOGGING_HEADER1	Exception logging header 1 register	2FFE 0828h
82Ch	R5FSS_RAT_EXCEPTION_LOGGING_DATA0	Exception logging data 0 register	2FFE 082Ch
830h	R5FSS_RAT_EXCEPTION_LOGGING_DATA1	Exception logging data 1 register	2FFE 0830h
834h	R5FSS_RAT_EXCEPTION_LOGGING_DATA2	Exception logging data 2 register	2FFE 0834h
838h	R5FSS_RAT_EXCEPTION_LOGGING_DATA3	Exception logging data 3 register	2FFE 0838h
840h	R5FSS_RAT_EXCEPTION_PEND_SET	Exception logging interrupt pending set register	2FFE 0840h
844h	R5FSS_RAT_EXCEPTION_PEND_CLEAR	Exception logging interrupt pending clear register	2FFE 0844h
848h	R5FSS_RAT_EXCEPTION_ENABLE_SET	Exception logging interrupt enable set register	2FFE 0848h
84Ch	R5FSS_RAT_EXCEPTION_ENABLE_CLEAR	Exception logging interrupt enable clear register	2FFE 084Ch
850h	R5FSS_RAT_EOI_REG	EOI register	2FFE 0850h

1 R5FSS_RAT_PID Register (Offset = 0h) [reset = 66801100h]

R5FSS_RAT_PID is shown in Figure 14-3313 and described in Table 14-6686.

Return to Summary Table.

This register contains the major and minor revisions for the module.

Table 14-9997. R5FSS_RAT_PID Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0000h

Figure 14-3313. R5FSS_RAT_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66801100h																															

Table 14-9999. R5FSS_RAT_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66801100h	TI internal data. Identifies revision of peripheral.

2 R5FSS_RAT_CONFIG Register (Offset = 4h) [reset = 240204h]

R5FSS_RAT_CONFIG is shown in Figure 14-3314 and described in Table 14-6688.

Return to Summary Table.

This register contains the configuration values for the module.

Table 14-10000. R5FSS_RAT_CONFIG Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0004h

Figure 14-3314. R5FSS_RAT_CONFIG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">ADDR_WIDTH</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R-24h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDRS</td><td colspan="8">REGIONS</td></tr>
<tr><td colspan="8">R-2h</td><td colspan="8">R-4h</td></tr>
</table>

Table 14-10002. R5FSS_RAT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved.
23-16	ADDR_WIDTH	R	24h	Number of address bits.
15-8	ADDRS	R	2h	Number of addresses.
7-0	REGIONS	R	4h	Number of regions.

3 R5FSS_RAT_CTRL_j Register (Offset = 20h + formula) [reset = 0h]

R5FSS_RAT_CTRL_j is shown in Figure 14-3315 and described in Table 14-6690.

Return to Summary Table.

This region controls the size and the enable for a region.

Offset = 20h + (j * 10h); where j = 0h to Fh.

Table 14-10003. R5FSS_RAT_CTRL_j Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0020h + formula

Figure 14-3315. R5FSS_RAT_CTRL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	RESERVED														
R/W-0h	R-0h														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SIZE					
R-0h										R/W-0h					

Table 14-10005. R5FSS_RAT_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the region.
30-6	RESERVED	R	0h	Reserved.
5-0	SIZE	R/W	0h	Size of the region in address bits. 0h = 1B 1h = 2B 2h = 4B ... 20h = 4GB

4 R5FSS_RAT_BASE_j Register (Offset = 24h + formula) [reset = 0h]

R5FSS_RAT_BASE_j is shown in Figure 14-3316 and described in Table 14-6692.

Return to Summary Table.

This register is used for the base address for a region. This is the source address for matching to a region.

Offset = 24h + (j * 10h); where j = 0h to Fh.

Table 14-10006. R5FSS_RAT_BASE_j Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0024h + formula

Figure 14-3316. R5FSS_RAT_BASE_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">BASE</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

Table 14-10008. R5FSS_RAT_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASE	R/W	0h	Base address for the region. It must be aligned to the programmed size.

5 R5FSS_RAT_TRANS_L_j Register (Offset = 28h + formula) [reset = 0h]

R5FSS_RAT_TRANS_L_j is shown in Figure 14-3317 and described in Table 14-6694.

Return to Summary Table.

This register contains the translated lower address bits for a region.

Offset = 28h + (j * 10h); where j = 0h to Fh.

Table 14-10009. R5FSS_RAT_TRANS_L_j Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0028h + formula

Figure 14-3317. R5FSS_RAT_TRANS_L_j Register

31-0
LOWER
R/W-0h

Table 14-10011. R5FSS_RAT_TRANS_L_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOWER	R/W	0h	Translated lower address bits for the region. It must be aligned to the programmed size.

6 R5FSS_RAT_TRANS_U_j Register (Offset = 2Ch + formula) [reset = 0h]

R5FSS_RAT_TRANS_U_j is shown in Figure 14-3318 and described in Table 14-6696.

Return to Summary Table.

This register contains the translated upper address bits for a region.

Offset = 2Ch + (j * 10h); where j = 0h to Fh

Table 14-10012. R5FSS_RAT_TRANS_U_j Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 002Ch + formula

Figure 14-3318. R5FSS_RAT_TRANS_U_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																UPPER															
R-0h																R/W-0h															

Table 14-10014. R5FSS_RAT_TRANS_U_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved.
15-0	UPPER	R/W	0h	Translated upper address bits for the region.

7 R5FSS_RAT_DESTINATION_ID Register (Offset = 804h) [reset = 0h]

R5FSS_RAT_DESTINATION_ID is shown in Figure 14-3319 and described in Table 14-6698.

Return to Summary Table.

This register defines the destination ID value for error messages.

Table 14-10015. R5FSS_RAT_DESTINATION_ID Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0804h

Figure 14-3319. R5FSS_RAT_DESTINATION_ID Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="24">R-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

Table 14-10017. R5FSS_RAT_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved.
7-0	DEST_ID	R/W	0h	Destination ID.

8 R5FSS_RAT_EXCEPTION_LOGGING_CONTROL Register (Offset = 820h) [reset = 0h]

R5FSS_RAT_EXCEPTION_LOGGING_CONTROL is shown in Figure 14-3320 and described in Table 14-6700.

Return to Summary Table.

This register controls the exception logging.

Table 14-10018. R5FSS_RAT_EXCEPTION_LOGGING_CONTROL Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0820h

Figure 14-3320. R5FSS_RAT_EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
R-0h						R/W-0h	R/W-0h

Table 14-10020. R5FSS_RAT_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved.
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

9 R5FSS_RAT_EXCEPTION_LOGGING_HEADER0 Register (Offset = 824h) [reset = 0h]

R5FSS_RAT_EXCEPTION_LOGGING_HEADER0 is shown in Figure 14-3321 and described in Table 14-6702.

Return to Summary Table.

This register contains the first word of the header.

Table 14-10021. R5FSS_RAT_EXCEPTION_LOGGING_HEADER0 Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0824h

Figure 14-3321. R5FSS_RAT_EXCEPTION_LOGGING_HEADER0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TYPE_F</td><td colspan="16">SRC_ID</td><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="16">R-0h</td><td colspan="8">R-0h</td></tr>
</table>

Table 14-10023. R5FSS_RAT_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type. 4h = RAT.
23-8	SRC_ID	R	0h	Source ID.
7-0	DEST_ID	R	0h	Destination ID.

10 R5FSS_RAT_EXCEPTION_LOGGING_HEADER1 Register (Offset = 828h) [reset = 0h]

R5FSS_RAT_EXCEPTION_LOGGING_HEADER1 is shown in Figure 14-3322 and described in Table 14-6704.

Return to Summary Table.

This register contains the second word of the header.

Table 14-10024. R5FSS_RAT_EXCEPTION_LOGGING_HEADER1 Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0828h

Figure 14-3322. R5FSS_RAT_EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP								CODE								RESERVED															
R-0h								R-0h								R-0h															

Table 14-10026. R5FSS_RAT_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code. 1h = Boundary crossing error.
15-0	RESERVED	R	0h	Reserved.

11 R5FSS_RAT_EXCEPTION_LOGGING_DATA0 Register (Offset = 82Ch) [reset = 0h]

R5FSS_RAT_EXCEPTION_LOGGING_DATA0 is shown in Figure 14-3323 and described in Table 14-6706.

Return to Summary Table.

This register contains the first word of the data.

Table 14-10027. R5FSS_RAT_EXCEPTION_LOGGING_DATA0 Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 082Ch

Figure 14-3323. R5FSS_RAT_EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

Table 14-10029. R5FSS_RAT_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Address lower 32 bits.

12 R5FSS_RAT_EXCEPTION_LOGGING_DATA1 Register (Offset = 830h) [reset = 0h]

R5FSS_RAT_EXCEPTION_LOGGING_DATA1 is shown in Figure 14-3324 and described in Table 14-6708.

Return to Summary Table.

This register contains the second word of the data.

Table 14-10030. R5FSS_RAT_EXCEPTION_LOGGING_DATA1 Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0830h

Figure 14-3324. R5FSS_RAT_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-0h																R-0h															

Table 14-10032. R5FSS_RAT_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved.
15-0	ADDR_H	R	0h	Address upper 12 bits.

13 R5FSS_RAT_EXCEPTION_LOGGING_DATA2 Register (Offset = 834h) [reset = 0h]

R5FSS_RAT_EXCEPTION_LOGGING_DATA2 is shown in Figure 14-3325 and described in Table 14-6710.

Return to Summary Table.

This register contains the third word of the data.

Table 14-10033. R5FSS_RAT_EXCEPTION_LOGGING_DATA2 Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0834h

Figure 14-3325. R5FSS_RAT_EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-0h				R-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R-0h							

Table 14-10035. R5FSS_RAT_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved.
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	0h	Reserved.
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

14 R5FSS_RAT_EXCEPTION_LOGGING_DATA3 Register (Offset = 838h) [reset = 0h]

R5FSS_RAT_EXCEPTION_LOGGING_DATA3 is shown in Figure 14-3326 and described in Table 14-6712.

Return to Summary Table.

This register contains the fourth word of the data. Reading this register will clear the error pending bit.

Table 14-10036. R5FSS_RAT_EXCEPTION_LOGGING_DATA3 Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0838h

Figure 14-3326. R5FSS_RAT_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						BYTECNT									
R-0h																						R-0h									

Table 14-10038. R5FSS_RAT_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved.
9-0	BYTECNT	R	0h	Byte count.

15 R5FSS_RAT_EXCEPTION_PEND_SET Register (Offset = 840h) [reset = 0h]

R5FSS_RAT_EXCEPTION_PEND_SET is shown in Figure 14-3327 and described in Table 14-6714.

Return to Summary Table.

This register allows to set the exception pending signal.

Table 14-10039. R5FSS_RAT_EXCEPTION_PEND_SET Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0840h

Figure 14-3327. R5FSS_RAT_EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R-0h							R/W1S-0h

Table 14-10041. R5FSS_RAT_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved.
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pending signal.

16 R5FSS_RAT_EXCEPTION_PEND_CLEAR Register (Offset = 844h) [reset = 0h]

R5FSS_RAT_EXCEPTION_PEND_CLEAR is shown in Figure 14-3328 and described in Table 14-6716.

Return to Summary Table.

This register allows to clear the pend signal.

Table 14-10042. R5FSS_RAT_EXCEPTION_PEND_CLEAR Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0844h

Figure 14-3328. R5FSS_RAT_EXCEPTION_PEND_CLEAR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PEND_CLR</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W1C-0h</td></tr>
</table>

Table 14-10044. R5FSS_RAT_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved.
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pending signal.

17 R5FSS_RAT_EXCEPTION_ENABLE_SET Register (Offset = 848h) [reset = 0h]

R5FSS_RAT_EXCEPTION_ENABLE_SET is shown in Figure 14-3329 and described in Table 14-6718.

Return to Summary Table.

This register allows to set the interrupt enable signal.

Table 14-10045. R5FSS_RAT_EXCEPTION_ENABLE_SET Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0848h

Figure 14-3329. R5FSS_RAT_EXCEPTION_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
R-0h							R/W1S-0h

Table 14-10047. R5FSS_RAT_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved.
0	ENABLE_SET	R/W1S	0h	Write a 1 to set the exception interrupt enable signal.

18 R5FSS_RAT_EXCEPTION_ENABLE_CLEAR Register (Offset = 84Ch) [reset = 0h]

R5FSS_RAT_EXCEPTION_ENABLE_CLEAR is shown in Figure 14-3330 and described in Table 14-6720.

Return to Summary Table.

This register allows to clear the interrupt enable signal.

Table 14-10048. R5FSS_RAT_EXCEPTION_ENABLE_CLEAR Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 084Ch

Figure 14-3330. R5FSS_RAT_EXCEPTION_ENABLE_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
R-0h							R/W1C-0h

Table 14-10050. R5FSS_RAT_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved.
0	ENABLE_CLR	R/W1C	0h	Write a 1 to clear the exception interrupt enable signal.

19 R5FSS_RAT_EOI_REG Register (Offset = 850h) [reset = 0h]

R5FSS_RAT_EOI_REG is shown in Figure 14-3331 and described in Table 14-6722.

Return to Summary Table.

EOI Register.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-10051. R5FSS_RAT_EOI_REG Instances

Instance	Physical Address
R5FSS_RAT_CFG	2FFE 0850h

Figure 14-3331. R5FSS_RAT_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EOI_WR															
R-0h																R/W-0h															

Table 14-10053. R5FSS_RAT_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved.
15-0	EOI_WR	R/W	0h	EOI value.

14.3.6 PRUSS Registers

14.3.6.1 PRU_ICSSG Registers

14.3.6.1.1 PRU_ICSSG PRU_CTRL, RTU_PRU_CTRL, and TX_PRU_CTRL Registers

Table 14-6724 through Table 14-6726 lists the memory-mapped control registers for the PRU_ICSSG PRU0/PRU1, RTU_PRU0/RTU_PRU1 and TX_PRU0/TX_PRU1 cores. All register offset addresses not listed in Table 14-6724 through Table 14-6726 should be considered as reserved locations and the register contents should not be modified.

Note

PDSP in instance names is equivalent to the PRU processor.

Table 14-10054. PRU_CTRL Instances

Instance	Base Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 2000h
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 4000h
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 2000h
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 4000h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 3000h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 3800h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 3000h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 3800h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 5000h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 5800h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 5000h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 5800h

Table 14-10055. PRU_CTRL Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_PDSP0_IRAM Physical Address	PRU_ICSSG0_PR1_PDSP1_IRAM Physical Address	PRU_ICSSG1_PR1_PDSP0_IRAM Physical Address	PRU_ICSSG1_PR1_PDSP1_IRAM Physical Address
0h	ICSSG_PRU_CONTROL	Control Register	3002 2000h	3002 4000h	300A 2000h	300A 4000h
4h	ICSSG_PRU_STATUS	Status Register	3002 2004h	3002 4004h	300A 2004h	300A 4004h
8h	ICSSG_PRU_WAKEUP_EN	Wakeup Enable Register	3002 2008h	3002 4008h	300A 2008h	300A 4008h
Ch	ICSSG_PRU_CYCLE	Cycle Count	3002 200Ch	3002 400Ch	300A 200Ch	300A 400Ch
10h	ICSSG_PRU_STALL	Stall Count	3002 2010h	3002 4010h	300A 2010h	300A 4010h
20h	ICSSG_PRU_CTBIR0	Constant Table Block Index Register 0	3002 2020h	3002 4020h	300A 2020h	300A 4020h
24h	ICSSG_PRU_CTBIR1	Constant Table Block Index Register 1	3002 2024h	3002 4024h	300A 2024h	300A 4024h
28h	ICSSG_PRU_CTPPR0	Constant Table Programmable Pointer Register 0	3002 2028h	3002 4028h	300A 2028h	300A 4028h
2Ch	ICSSG_PRU_CTPPR1	Constant Table Programmable Pointer Register 1	3002 202Ch	3002 402Ch	300A 202Ch	300A 402Ch

Table 14-10056. PRU_CTRL Registers 2

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM Physical Address	PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM Physical Address	PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM Physical Address	PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM Physical Address
0h	ICSSG_PRU_CONTROL	Control Register	3002 3000h	3002 3800h	300A 3000h	300A 3800h
4h	ICSSG_PRU_STATUS	Status Register	3002 3004h	3002 3804h	300A 3004h	300A 3804h

Table 14-10056. PRU_CTRL Registers 2 (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM Physical Address	PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM Physical Address	PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM Physical Address	PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM Physical Address
8h	ICSSG_PRU_WAKEUP_EN	Wakeup Enable Register	3002 3008h	3002 3808h	300A 3008h	300A 3808h
Ch	ICSSG_PRU_CYCLE	Cycle Count	3002 300Ch	3002 380Ch	300A 300Ch	300A 380Ch
10h	ICSSG_PRU_STALL	Stall Count	3002 3010h	3002 3810h	300A 3010h	300A 3810h
20h	ICSSG_PRU_CTBIR0	Constant Table Block Index Register 0	3002 3020h	3002 3820h	300A 3020h	300A 3820h
24h	ICSSG_PRU_CTBIR1	Constant Table Block Index Register 1	3002 3024h	3002 3824h	300A 3024h	300A 3824h
28h	ICSSG_PRU_CTPPR0	Constant Table Programmable Pointer Register 0	3002 3028h	3002 3828h	300A 3028h	300A 3828h
2Ch	ICSSG_PRU_CTPPR1	Constant Table Programmable Pointer Register 1	3002 302Ch	3002 382Ch	300A 302Ch	300A 382Ch

Table 14-10057. PRU_CTRL Registers 4

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TX_PDSP0_IRAM Physical Address	PRU_ICSSG0_PR1_TX_PDSP1_IRAM Physical Address	PRU_ICSSG1_PR1_TX_PDSP0_IRAM Physical Address	PRU_ICSSG1_PR1_TX_PDSP1_IRAM Physical Address
0h	ICSSG_PRU_CONTROL	Control Register	3002 5000h	3002 5800h	300A 5000h	300A 5800h
4h	ICSSG_PRU_STATUS	Status Register	3002 5004h	3002 5804h	300A 5004h	300A 5804h
8h	ICSSG_PRU_WAKEUP_EN	Wakeup Enable Register	3002 5008h	3002 5808h	300A 5008h	300A 5808h
Ch	ICSSG_PRU_CYCLE	Cycle Count	3002 500Ch	3002 580Ch	300A 500Ch	300A 580Ch
10h	ICSSG_PRU_STALL	Stall Count	3002 5010h	3002 5810h	300A 5010h	300A 5810h
20h	ICSSG_PRU_CTBIR0	Constant Table Block Index Register 0	3002 5020h	3002 5820h	300A 5020h	300A 5820h
24h	ICSSG_PRU_CTBIR1	Constant Table Block Index Register 1	3002 5024h	3002 5824h	300A 5024h	300A 5824h
28h	ICSSG_PRU_CTPPR0	Constant Table Programmable Pointer Register 0	3002 5028h	3002 5828h	300A 5028h	300A 5828h
2Ch	ICSSG_PRU_CTPPR1	Constant Table Programmable Pointer Register 1	3002 502Ch	3002 582Ch	300A 502Ch	300A 582Ch

1 ICSSG_PRU_CONTROL Register (Offset = 0h) [reset = 1h]

PRU_CONTROL is shown in Figure 14-3332 and described in Table 14-6728.

PRU Control Register.

Table 14-10058. ICSSG_PRU_CONTROL Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 2000h
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 4000h
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 2000h
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 4000h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 3000h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 3800h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 3000h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 3800h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 5000h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 5800h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 5000h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 5800h

Figure 14-3332. ICSSG_PRU_CONTROL Register

31	30	29	28	27	26	25	24
PCOUNTER_RST_VAL							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PCOUNTER_RST_VAL							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RUNSTATE	RESERVED	TS_ENABLE	RESERVED				SINGLE_STEP
R-0h	R-0h	R-0h					R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RESERVED	COUNTER_ENABLE	SLEEPING	ENABLE	SOFT_RST_N
R-0h				R/W-0h	R/W-0h	R/W-0h	R-1h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10060. ICSSG_PRU_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PCOUNTER_RST_VAL	R/W	0h	Program Counter Reset Value: This field controls the address where the PRU will start executing code from after it is taken out of reset.

Table 14-10060. ICSSG_PRU_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RUNSTATE	R	0h	Run State: This bit indicates whether the PRU is currently executing an instruction or is halted. 0h = PRU is halted and host has access to the instruction RAM and debug registers regions. 1h = PRU is currently running and the host is locked out of the instruction RAM and debug registers regions. This bit is used by an external debug agent to know when the PRU has actually halted when waiting for a HALT instruction to execute, a single step to finish, or any other time when the [1]ENABLE has been cleared.
14	RESERVED			Reserved
13	TS_ENABLE	R	0h	Task Swapping Enable: This bit indicates the current state of the internal task swapping enable flag. When this bit is clear, the PRU will ignore requests which are presented on the Task Swap Request interface. When this bit is set, the PRU will gracefully complete any multi-cycle instruction and will then issue an XCHG instruction using the 22 LSBs as provided on the task swap request interface.
12-9	RESERVED	R	0h	Reserved
8	SINGLE_STEP	R/W	0h	Single Step Enable: This bit controls whether or not the PRU will only execute a single instruction when enabled. 0h = PRU will free run when enabled. 1h = PRU will execute a single instruction and then the [1]ENABLE bit will be cleared. Note that this bit does not actually enable the PRU, it only sets the policy for how much code will be run after the PRU is enabled. The [1]ENABLE bit must be explicitly asserted. It is expressly legal to initialize both the [8]SINGLE_STEP and [1]ENABLE bits simultaneously. (Two independent writes are not required to cause the stated functionality).
7-5	RESERVED	R	0h	Reserved
4	RESERVED			Reserved
3	COUNTER_ENABLE	R/W	0h	PRU Cycle Counter Enable: Enables PRU cycle counters. 0h = Counters not enabled. 1h = Counters enabled.
2	SLEEPING	R/W	0h	PRU Sleep Indicator: This bit indicates whether or not the PRU is currently asleep. 0h = PRU is not asleep. 1h = PRU is asleep. If this bit is written to a 0h, the PRU will be forced to power up from sleep mode.

Table 14-10060. ICSSG_PRU_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ENABLE	R/W	0h	Processor Enable: This bit controls whether or not the PRU is allowed to fetch new instructions. 0h = PRU is disabled. 1h = PRU is enabled. If this bit is de-asserted while the PRU is currently running and has completed the initial cycle of a multi-cycle instruction (LBxO,SBxO,SCAN, etc.), the current instruction will be allowed to complete before the PRU pauses execution. Otherwise, the PRU will halt immediately. Because of the unpredictability timing sensitivity of the instruction execution loop, this bit is not a reliable indication of whether or not the PRU is currently running. The [15]RUNSTATE bit should be consulted for an absolute indication of the run state of the core. When the PRU is halted, its internal state remains coherent therefore this bit can be reasserted without issuing a software reset and the PRU will resume processing exactly where it left off in the instruction stream.
0	SOFT_RST_N	R/W	1h	Soft Reset: When this bit is cleared, the PRU will be reset. This bit is set back to 1h on the next cycle after it has been cleared.

2 ICSSG_PRU_STATUS Register (Offset = 4h) [reset = 0h]

PRU_STATUS is shown in Figure 14-3333 and described in Table 14-6730.

PRU Status Register.

Table 14-10061. ICSSG_PRU_STATUS Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 2004h
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 4004h
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 2004h
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 4004h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 3004h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 3804h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 3004h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 3804h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 5004h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 5804h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 5004h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 5804h

Figure 14-3333. ICSSG_PRU_STATUS Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">PCOUNTER</td></tr>
<tr><td colspan="16">R-0h</td><td colspan="16">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10063. ICSSG_PRU_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PCOUNTER	R	0h	Program Counter: This field is a registered (1 cycle delayed) reflection of the PRU program counter. Note that the PC is an instruction address where each instruction is a 32 bit word. This is not a byte address and to compute the byte address, multiply the PC by 4 (For example: PC of 2 = byte address of 8h, or PC of 8 = byte address of 20h).

3 ICSSG_PRU_WAKEUP_EN Register (Offset = 8h) [reset = 0h]

PRU_WAKEUP_EN is shown in Figure 14-3334 and described in Table 14-6732.

PRU Wakeup Enable Register.

Table 14-10064. ICSSG_PRU_WAKEUP_EN Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 2008h
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 4008h
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 2008h
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 4008h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 3008h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 3808h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 3008h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 3808h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 5008h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 5808h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 5008h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 5808h

Figure 14-3334. ICSSG_PRU_WAKEUP_EN Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">BITWISE_ENABLES</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10066. ICSSG_PRU_WAKEUP_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BITWISE_ENABLES	R/W	0h	Wakeup Enables: This field is ANDed with the incoming R31 status inputs (whose bit positions were specified in the stmap parameter) to produce a vector which is unary ORed to produce the status_wakeup source for the core. Setting any bit in this vector will allow the corresponding status input to wake up the core when it is asserted high. The PRU should set this enable vector prior to executing a SLP (sleep) instruction to ensure that the desired sources can wake up the core.

4 ICSSG_PRU_CYCLE Register (Offset = Ch) [reset = 0h]

PRU_CYCLE is shown in Figure 14-3335 and described in Table 14-6734.

PRU Cycle Count. This register counts the number of cycles for which the PRU has been enabled.

Table 14-10067. ICSSG_PRU_CYCLE Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 200Ch
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 400Ch
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 200Ch
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 400Ch
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 300Ch
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 380Ch
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 300Ch
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 380Ch
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 500Ch
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 580Ch
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 500Ch
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 580Ch

Figure 14-3335. ICSSG_PRU_CYCLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYCLECOUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10069. ICSSG_PRU_CYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CYCLECOUNT	R/W	0h	This value is incremented by 1 for every cycle during which the PRU is enabled and the counter is enabled (both bits [1]ENABLE and [3]COUNTER_ENABLE set in the ICSSG_PRU_CONTROL register). Counting halts while the PRU is disabled or counter is disabled, and resumes when re-eneabled. Counter clears the [3]COUNTER_ENABLE bit in the ICSSG_PRU_CONTROL register when the count reaches FFFFFFFFh. (Count does not wrap). The register can be read at any time. The register can be cleared when the counter or PRU is disabled. Clearing this register also clears the PRU Stall Count Register (ICSSG_PRU_STALL).

5 ICSSG_PRU_STALL Register (Offset = 10h) [reset = 0h]

PRU_STALL is shown in Figure 14-3336 and described in Table 14-6736.

PRU Stall Count Register. This register counts the number of cycles for which the PRU has been enabled, but unable to fetch a new instruction. It is linked to the Cycle Count Register (ICSSG_PRU_CYCLE, offset: 0Ch) such that this register reflects the stall cycles measured over the same cycles as counted by the cycle count register. Thus the value of this register is always less than or equal to cycle count.

Table 14-10070. ICSSG_PRU_STALL Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 2010h
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 4010h
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 2010h
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 4010h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 3010h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 3810h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 3010h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 3810h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 5010h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 5810h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 5010h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 5810h

Figure 14-3336. ICSSG_PRU_STALL Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">STALLCOUNT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10072. ICSSG_PRU_STALL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STALLCOUNT	R	0h	This value is incremented by 1 for every cycle during which the PRU is enabled and the counter is enabled (both bits [1]ENABLE and [3]COUNTER_ENABLE set in the ICSSG_PRU_CONTROL register), and the PRU was unable to fetch a new instruction for any reason. Counting halts while the PRU is disabled or the counter is disabled, and resumes when re-enabled. The register can be read at any time. The register is cleared when PRU Cycle Count Register (ICSSG_PRU_CYCLE) is cleared.

6 ICSSG_PRU_CTBIR0 Register (Offset = 20h) [reset = 0h]

PRU_CTBIR0 is shown in Figure 14-3337 and described in Table 14-6738.

Constant Table Block Index Register 0. This register is used to set the block indices which are used to modify entries 24 and 25 in the PRU Constant Table. This register can be written by the PRU whenever it needs to change to a new base pointer for a block in the State Scratchpad RAM. This function is useful since the PRU is often processing multiple processing threads which require it to change contexts. The PRU can use this register to avoid requiring excessive amounts of code for repetitive context switching.

Table 14-10073. ICSSG_PRU_CTBIR0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 2020h
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 4020h
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 2020h
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 4020h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 3020h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 3820h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 3020h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 3820h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 5020h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 5820h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 5020h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 5820h

Figure 14-3337. ICSSG_PRU_CTBIR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								C25_BLK_INDEX							
R-0h								R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED								C24_BLK_INDEX							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10075. ICSSG_PRU_CTBIR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	C25_BLK_INDEX	R/W	0h	PRU Constant Entry 25 Block Index: This field sets the value that will appear in bits 15:8 of entry 25 in the PRU Constant Table. This field while always present is only used if the ctreg_cnt configuration value is less than 26.
15-8	RESERVED	R	0h	Reserved
7-0	C24_BLK_INDEX	R/W	0h	PRU Constant Entry 24 Block Index: This field sets the value that will appear in bits 15:8 of entry 24 in the PRU Constant Table. This field while always present is only used if the ctreg_cnt configuration value is less than 25.

7 ICSSG_PRU_CTBIR1 Register (Offset = 24h) [reset = 0h]

PRU_CTBIR1 is shown in Figure 14-3338 and described in Table 14-6740.

Constant Table Block Index Register 1. This register is used to set the block indices which are used to modify entries 26 and 27 in the PRU Constant Table. This register can be written by the PRU whenever it needs to change to a new base pointer for a block in the State Scratchpad RAM. This function is useful since the PRU is often processing multiple processing threads which require it to change contexts. The PRU can use this register to avoid requiring excessive amounts of code for repetitive context switching.

Table 14-10076. ICSSG_PRU_CTBIR1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 2024h
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 4024h
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 2024h
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 4024h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 3024h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 3824h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 3024h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 3824h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 5024h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 5824h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 5024h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 5824h

Figure 14-3338. ICSSG_PRU_CTBIR1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">C27_BLK_INDEX</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">C26_BLK_INDEX</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10078. ICSSG_PRU_CTBIR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	C27_BLK_INDEX	R/W	0h	PRU Constant Entry 27 Block Index: This field sets the value that will appear in bits 15:8 of entry 27 in the PRU Constant Table. This field while always present is only used if the ctreg_cnt configuration value is less than 28.
15-8	RESERVED	R	0h	Reserved
7-0	C26_BLK_INDEX	R/W	0h	PRU Constant Entry 26 Block Index: This field sets the value that will appear in bits 15:8 of entry 26 in the PRU Constant Table. This field while always present is only used if the ctreg_cnt configuration value is less than 27.

8 ICSSG_PRU_CTPPR0 Register (Offset = 28h) [reset = 0h]

PRU_CTPPR0 is shown in Figure 14-3339 and described in Table 14-6742.

Constant Table Programmable Pointer Register 0. This register allows the PRU to set up the 256-byte page index for entries 28 and 29 in the PRU Constant Table which serve as general purpose pointers which can be configured to point to any locations inside the session router address map. This register is useful when the PRU needs to frequently access certain structures inside the session router address space whose locations are not hard coded such as tables in scratchpad memory.

Table 14-10079. ICSSG_PRU_CTPPR0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 2028h
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 4028h
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 2028h
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 4028h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 3028h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 3828h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 3028h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 3828h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 5028h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 5828h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 5028h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 5828h

Figure 14-3339. ICSSG_PRU_CTPPR0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">C29_POINTER</td><td colspan="16">C28_POINTER</td></tr>
<tr><td colspan="16">R/W-0h</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10081. ICSSG_PRU_CTPPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	C29_POINTER	R/W	0h	PRU Constant Entry 29 Pointer: This field sets the value that will appear in bits [23-8] of entry 29 in the PRU Constant Table. This field while always present is only used if the ctreg_cnt configuration value is less than 30.
15-0	C28_POINTER	R/W	0h	PRU Constant Entry 28 Pointer: This field sets the value that will appear in bits [23-8] of entry 28 in the PRU Constant Table. This field while always present is only used if the ctreg_cnt configuration value is less than 29.

9 ICSSG_PRU_CTPPR1 Register (Offset = 2Ch) [reset = 0h]

PRU_CTPPR1 is shown in Figure 14-3340 and described in Table 14-6744.

Constant Table Programmable Pointer Register 1. This register functions the same as the PRU Constant Table Programmable Pointer Register 0 but allows the PRU to control entries 30 and 31 in the PRU Constant Table.

Table 14-10082. ICSSG_PRU_CTPPR1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	3002 202Ch
PRU_ICSSG0_PR1_PDSP1_IRAM	3002 402Ch
PRU_ICSSG1_PR1_PDSP0_IRAM	300A 202Ch
PRU_ICSSG1_PR1_PDSP1_IRAM	300A 402Ch
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	3002 302Ch
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	3002 382Ch
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	300A 302Ch
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	300A 382Ch
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	3002 502Ch
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	3002 582Ch
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	300A 502Ch
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	300A 582Ch

Figure 14-3340. ICSSG_PRU_CTPPR1 Register

31-16	15-0
C31_POINTER	C30_POINTER
R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10084. ICSSG_PRU_CTPPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	C31_POINTER	R/W	0h	PRU Constant Entry 31 Pointer: This field sets the value that will appear in bits [23-8] of entry 31 in the PRU Constant Table. This field while always present is only used if the ctreg_cnt configuration value is less than 32.
15-0	C30_POINTER	R/W	0h	PRU Constant Entry 30 Pointer: This field sets the value that will appear in bits [23-8] of entry 30 in the PRU Constant Table. This field while always present is only used if the ctreg_cnt configuration value is less than 31.

14.3.6.1.2 PRU_ICSSG PRU_DEBUG, RTU_PRU_DEBUG, and TX_PRU_DEBUG Registers

Table 14-6746 through Table 14-6748 lists the memory-mapped registers for the PRU_ICSSG PRU_DEBUG, RTU_PRU_DEBUG and TX_PRU_DEBUG. All register offset addresses not listed in Table 14-6746 through Table 14-6748 should be considered as reserved locations and the register contents should not be modified.

Note

PDSP in instance names is equivalent to the PRU processor names.

Table 14-10085. PRU_DEBUG Instances

Instance	Base Address
PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG	3002 2400h
PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG	3002 4400h
PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG	300A 2400h
PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG	300A 4400h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	3002 3400h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	3002 3C00h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	300A 3400h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	300A 3C00h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM_DEBUG	3002 5400h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM_DEBUG	3002 5C00h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM_DEBUG	300A 5400h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM_DEBUG	300A 5C00h

Table 14-10086. PRU_DEBUG Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG Physical Address	PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG Physical Address
0h + formula	ICSSG_DBG_GPREG_y	DEBUG PRU General Purpose Registers 0 to 31	3002 2400h + formula	3002 4400h + formula	300A 2400h + formula	300A 4400h + formula
80h + formula	ICSSG_DBG_CT_REG_y	DEBUG PRU Constant Table Entry Registers 0 to 31	3002 2480h + formula	3002 4480h + formula	300A 2480h + formula	300A 4480h + formula

Table 14-10087. PRU_DEBUG Registers 2

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG Physical Address	PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG Physical Address
0h + formula	ICSSG_DBG_GPREG_y	DEBUG PRU General Purpose Registers 0 to 31	3002 3400h + formula	3002 3C00h + formula	300A 3400h + formula	300A 3C00h + formula
80h + formula	ICSSG_DBG_CT_REG_y	DEBUG PRU Constant Table Entry Registers 0 to 31	3002 3480h + formula	3002 3C80h + formula	300A 3480h + formula	300A 3C80h + formula

Table 14-10088. PRU_DEBUG Registers 3

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TX_PDSP0_IRAM_DEBUG Physical Address	PRU_ICSSG0_PR1_TX_PDSP1_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_TX_PDSP0_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_TX_PDSP1_IRAM_DEBUG Physical Address
0h + formula	ICSSG_DBG_GPREG_y	DEBUG PRU General Purpose Registers 0 to 31	3002 5400h + formula	3002 5C00h + formula	300A 5400h + formula	300A 5C00h + formula
80h + formula	ICSSG_DBG_CT_REG_y	DEBUG PRU Constant Table Entry Registers 0 to 31	3002 5480h + formula	3002 5C80h + formula	300A 5480h + formula	300A 5C80h + formula

1 ICSSG_DBG_GPREG_y Register (Offset = 0h + formula) [reset = 0h]

ICSSG_DBG_GPREG_y is shown in Figure 14-3341 and described in Table 14-6750.

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DEBUG PRU General Purpose Registers 0 to 31. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Offset = 0h + (y * 4); where y = 0 to 31

Table 14-10089. ICSSG_DBG_GPREG_y Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG	3002 2400h + formula
PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG	3002 4400h + formula
PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG	300A 2400h + formula
PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG	300A 4400h + formula
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	3002 3400h + formula
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	3002 3C00h + formula
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	300A 3400h + formula
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	300A 3C00h + formula
PRU_ICSSG0_PR1_TX_PDSP0_IRAM_DEBUG	3002 5400h + formula
PRU_ICSSG0_PR1_TX_PDSP1_IRAM_DEBUG	3002 5C00h + formula
PRU_ICSSG1_PR1_TX_PDSP0_IRAM_DEBUG	300A 5400h + formula
PRU_ICSSG1_PR1_TX_PDSP1_IRAM_DEBUG	300A 5C00h + formula

Figure 14-3341. ICSSG_DBG_GPREG_y Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">GP_REGy</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 14-10091. ICSSG_DBG_GPREG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REGy	R/W	0h	PRU Internal GP Register y: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal register file.

2 ICSSG_DBG_CT_REG_y Register (Offset = 80h + formula) [reset = 0h]

ICSSG_DBG_CT_REG_y is shown in Figure 14-3342 and described in Table 14-6752.

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DEBUG PRU Constant Table Entry Registers 0 to 31. This register allows an external agent to debug/or configure the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Offset = 80h + (y * 4); where y = 0 to 31

Table 14-10092. ICSSG_DBG_CT_REG_y Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG	3002 2480h + formula
PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG	3002 4480h + formula
PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG	300A 2480h + formula
PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG	300A 4480h + formula
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	3002 3480h + formula
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	3002 3C80h + formula
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	300A 3480h + formula
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	300A 3C80h + formula
PRU_ICSSG0_PR1_TX_PDSP0_IRAM_DEBUG	3002 5480h + formula
PRU_ICSSG0_PR1_TX_PDSP1_IRAM_DEBUG	3002 5C80h + formula
PRU_ICSSG1_PR1_TX_PDSP0_IRAM_DEBUG	300A 5480h + formula
PRU_ICSSG1_PR1_TX_PDSP1_IRAM_DEBUG	300A 5C80h + formula

Figure 14-3342. ICSSG_DBG_CT_REG_y Register

31-0
CT_REGy
R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 14-10094. ICSSG_DBG_CT_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REGy	R/W	0h	PRU Internal Constants Table Entry y (where y = 0 to 31): Reading this field directly inspects the corresponding entry in the PRU internal constants table. Note: For each register y where y is less than the ctreg_cnt configuration parameter, the PRU internal Constants Table Entry Register will be writable and these registers are to be used to set the value for these constants. As for reads, the PRU must be disabled in order to access these registers.

14.3.6.1.3 PRU_ICSSG_ECC_AGGR Registers

Table 14-6754 lists the memory-mapped registers for the PRU_ICSSG_ECC_AGGR registers. All register offset addresses not listed in Table 14-6754 should be considered as reserved locations and the register contents should not be modified.

Table 14-10095. PRU_ICSSG_ECC_AGGR Instances

Instance	Base Address
PRU_ICSSG0_ECC_AGGR	3F00 A000h
PRU_ICSSG1_ECC_AGGR	3F00 B000h

Table 14-10096. PRU_ICSSG_ECC_AGGR Registers

Offset	Acronym	Register Name	PRU_ICSSG0_ECC_AGGR Physical Address	PRU_ICSSG1_ECC_AGGRPhysical Address
0h	ICSSG_REV	Aggregator Revision Register	3F00 A000h	3F00 B000h
8h	ICSSG_VECTOR	ECC Vector Register	3F00 A008h	3F00 B008h
Ch	ICSSG_STAT	Misc Status	3F00 A00Ch	3F00 B00Ch
3Ch	ICSSG_SEC_EOI_REG	EOI Register	3F00 A03Ch	3F00 B03Ch
40h	ICSSG_SEC_STATUS_REG0	Interrupt Status Register 0	3F00 A040h	3F00 B040h
80h	ICSSG_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	3F00 A080h	3F00 B080h
C0h	ICSSG_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	3F00 A0C0h	3F00 B0C0h
13Ch	ICSSG_DED_EOI_REG	EOI Register	3F00 A13Ch	3F00 B13Ch
140h	ICSSG_DED_STATUS_REG0	Interrupt Status Register 0	3F00 A140h	3F00 B140h
180h	ICSSG_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	3F00 A180h	3F00 B180h
1C0h	ICSSG_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	3F00 A1C0h	3F00 B1C0h
200h	ICSSG_AGGR_ENABLE_SET	AGGR Interrupt Enable Set Register	3F00 A200h	0BF0 1200h
204h	ICSSG_AGGR_ENABLE_CLR	AGGR Interrupt Enable Clear Register	3F00 A204h	0BF0 1204h
208h	ICSSG_AGGR_STATUS_SET	AGGR Interrupt Status Set Register	3F00 A208h	0BF0 1208h
20Ch	ICSSG_AGGR_STATUS_CLR	AGGR Interrupt Status Clear Register	3F00 A20Ch	0BF0 120Ch

1 ICSSG_REV Register (Offset = 0h) [reset = 66A0E200h]

ICSSG_REV is shown in Figure 14-3343 and described in Table 14-6756.

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Table 14-10097. ICSSG_REV Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A000h
PRU_ICSSG1_ECC_AGGR	3F00 B000h

Figure 14-3343. ICSSG_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Ch					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10099. ICSSG_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Ch	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

2 ICSSG_VECTOR Register (Offset = 8h) [reset = X]

ICSSG_VECTOR is shown in Figure 14-3344 and described in Table 14-6758.

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ECC Vector Register

Table 14-10100. ICSSG_VECTOR Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A008h
PRU_ICSSG1_ECC_AGGR	3F00 B008h

Figure 14-3344. ICSSG_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-10102. ICSSG_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

3 ICSSG_STAT Register (Offset = Ch) [reset = X]

ICSSG_STAT is shown in Figure 14-3345 and described in Table 14-6760.

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Table 14-10103. ICSSG_STAT Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A00Ch
PRU_ICSSG1_ECC_AGGR	3F00 B00Ch

Figure 14-3345. ICSSG_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-X																					R-9h										

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10105. ICSSG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMS	R	9h	Indicates the number of RAMS serviced by the ECC aggregator

4 ICSSG_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

ICSSG_SEC_EOI_REG is shown in Figure 14-3346 and described in Table 14-6762.

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EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-10106. ICSSG_SEC_EOI_REG Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A03Ch
PRU_ICSSG1_ECC_AGGR	3F00 B03Ch

Figure 14-3346. ICSSG_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-10108. ICSSG_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

5 ICSSG_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

ICSSG_SEC_STATUS_REG0 is shown in Figure 14-3347 and described in Table 14-6764.

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Interrupt Status Register 0

Table 14-10109. ICSSG_SEC_STATUS_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A040h
PRU_ICSSG1_ECC_AGGR	3F00 B040h

Figure 14-3347. ICSSG_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PR1_PDSP_TX1_IRAM_PEND
R/W-X							R/W1S-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PR1_PDSP_TX0_IRAM_PEND	PR1_RTU1_IRAM_ECC_PEND	PR1_RTU0_IRAM_ECC_PEND	PR1_RAM_PEND	PR1_PDSP1_IRAM_PEND	PR1_PDSP0_IRAM_PEND	PR1_DRAM1_PEND	PR1_DRAM0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-10111. ICSSG_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_ram_pend
3	PR1_PDSP1_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp0_iram_pend
1	PR1_DRAM1_PEND	R/W1S	0h	Interrupt Pending Status for pr1_dram1_pend
0	PR1_DRAM0_PEND	R/W1S	0h	Interrupt Pending Status for pr1_dram0_pend

6 ICSSG_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

ICSSG_SEC_ENABLE_SET_REG0 is shown in Figure 14-3348 and described in Table 14-6766.

Return to Summary Table.

Interrupt Enable Set Register 0

Table 14-10112. ICSSG_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A080h
PRU_ICSSG1_ECC_AGGR	3F00 B080h

Figure 14-3348. ICSSG_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PR1_PDSP_TX1_IRAM_ENABLE_SET
R/W-X							R/W1S-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PR1_PDSP_TX0_IRAM_ENABLE_SET	PR1_RTU1_IRAM_ECC_ENABLE_SET	PR1_RTU0_IRAM_ECC_ENABLE_SET	PR1_RAM_ENABLE_SET	PR1_PDSP1_IRAM_ENABLE_SET	PR1_PDSP0_IRAM_ENABLE_SET	PR1_DRAM1_ENABLE_SET	PR1_DRAM0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-10114. ICSSG_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_dram1_pend

Table 14-10114. ICSSG_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PR1_DRAM0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_dram0_pend

7 ICSSG_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

ICSSG_SEC_ENABLE_CLR_REG0 is shown in Figure 14-3349 and described in Table 14-6768.

Return to Summary Table.

Interrupt Enable Clear Register 0

Table 14-10115. ICSSG_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A0C0h
PRU_ICSSG1_ECC_AGGR	3F00 B0C0h

Figure 14-3349. ICSSG_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX1_IRAM_ENABLE_CLR
R/W-X							R/W1C-0h

7	6	5	4	3	2	1	0
PR1_PDSP_TX0_IRAM_ENABLE_CLR	PR1_RTU1_IRAM_ECC_ENABLE_CLR	PR1_RTU0_IRAM_ECC_ENABLE_CLR	PR1_RAM_ENABLE_CLR	PR1_PDSP1_IRAM_ENABLE_CLR	PR1_PDSP0_IRAM_ENABLE_CLR	PR1_DRAM1_ENABLE_CLR	PR1_DRAM0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-10117. ICSSG_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_dram1_pend

Table 14-10117. ICSSG_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PR1_DRAM0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_dram0_pend

8 ICSSG_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

ICSSG_DED_EOI_REG is shown in Figure 14-3350 and described in Table 14-6770.

Return to Summary Table.

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-10118. ICSSG_DED_EOI_REG Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A13Ch
PRU_ICSSG1_ECC_AGGR	3F00 B13Ch

Figure 14-3350. ICSSG_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-10120. ICSSG_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

9 ICSSG_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

ICSSG_DED_STATUS_REG0 is shown in Figure 14-3351 and described in Table 14-6772.

Return to Summary Table.

Interrupt Status Register 0

Table 14-10121. ICSSG_DED_STATUS_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A140h
PRU_ICSSG1_ECC_AGGR	3F00 B140h

Figure 14-3351. ICSSG_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX1_IRAM_PEND
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX0_IRAM_PEND	PR1_RTU1_IRAM_ECC_PEND	PR1_RTU0_IRAM_ECC_PEND	PR1_RAM_PEND	PR1_PDSP1_IRAM_PEND	PR1_PDSP0_IRAM_PEND	PR1_DRAM1_PEND	PR1_DRAM0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-10123. ICSSG_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_ram_pend
3	PR1_PDSP1_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp0_iram_pend
1	PR1_DRAM1_PEND	R/W1S	0h	Interrupt Pending Status for pr1_dram1_pend
0	PR1_DRAM0_PEND	R/W1S	0h	Interrupt Pending Status for pr1_dram0_pend

10 ICSSG_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

ICSSG_DED_ENABLE_SET_REG0 is shown in Figure 14-3352 and described in Table 14-6774.

Return to Summary Table.

Interrupt Enable Set Register 0

Table 14-10124. ICSSG_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A180h
PRU_ICSSG1_ECC_AGGR	3F00 B180h

Figure 14-3352. ICSSG_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX1_IRAM_ENABLE_SET
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX0_IRAM_ENABLE_SET	PR1_RTU1_IRAM_ECC_ENABLE_SET	PR1_RTU0_IRAM_ECC_ENABLE_SET	PR1_RAM_ENABLE_SET	PR1_PDSP1_IRAM_ENABLE_SET	PR1_PDSP0_IRAM_ENABLE_SET	PR1_DRAM1_ENABLE_SET	PR1_DRAM0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-10126. ICSSG_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_dram1_pend

Table 14-10126. ICSSG_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PR1_DRAM0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_dram0_pend

11 ICSSG_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

ICSSG_DED_ENABLE_CLR_REG0 is shown in Figure 14-3353 and described in Table 14-6776.

Return to Summary Table.

Interrupt Enable Clear Register 0

Table 14-10127. ICSSG_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A1C0h
PRU_ICSSG1_ECC_AGGR	3F00 B1C0h

Figure 14-3353. ICSSG_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX1_IRAM_ENABLE_CLR
R/W-X							R/W1C-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX0_IRAM_ENABLE_CLR	PR1_RTU1_IRAM_ECC_ENABLE_CLR	PR1_RTU0_IRAM_ECC_ENABLE_CLR	PR1_RAM_ENABLE_CLR	PR1_PDSP1_IRAM_ENABLE_CLR	PR1_PDSP0_IRAM_ENABLE_CLR	PR1_DRAM1_ENABLE_CLR	PR1_DRAM0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-10129. ICSSG_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_dram1_pend

Table 14-10129. ICSSG_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PR1_DRAM0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_dram0_pend

12 ICSSG_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

ICSSG_AGGR_ENABLE_SET is shown in Figure 14-3354 and described in Table 14-6778.

Return to Summary Table.

AGGR interrupt enable set Register

Table 14-10130. ICSSG_AGGR_ENABLE_SET Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A200h
PRU_ICSSG1_ECC_AGGR	3F00 B200h

Figure 14-3354. ICSSG_AGGR_ENABLE_SET Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">R/W-X</td><td>R/W1S-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-10132. ICSSG_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for SVBUS timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

13 ICSSG_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

ICSSG_AGGR_ENABLE_CLR is shown in Figure 14-3355 and described in Table 14-6780.

Return to Summary Table.

AGGR interrupt enable clear Register

Table 14-10133. ICSSG_AGGR_ENABLE_CLR Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A204h
PRU_ICSSG1_ECC_AGGR	3F00 B204h

Figure 14-3355. ICSSG_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-10135. ICSSG_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for SVBUS timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

14 ICSSG_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

ICSSG_AGGR_STATUS_SET is shown in Figure 14-3356 and described in Table 14-6782.

Return to Summary Table.

AGGR interrupt status set Register

Table 14-10136. ICSSG_AGGR_STATUS_SET Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A208h
PRU_ICSSG1_ECC_AGGR	3F00 B208h

Figure 14-3356. ICSSG_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10138. ICSSG_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/W	0h	interrupt status set for SVBUS timeout errors
1-0	PARITY	R/W	0h	interrupt status set for parity errors

15 ICSSG_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

ICSSG_AGGR_STATUS_CLR is shown in Figure 14-3357 and described in Table 14-6784.

Return to Summary Table.

AGGR interrupt status clear Register

Table 14-10139. ICSSG_AGGR_STATUS_CLR Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	3F00 A20Ch
PRU_ICSSG1_ECC_AGGR	3F00 B20Ch

Figure 14-3357. ICSSG_AGGR_STATUS_CLR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">R/W-X</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10141. ICSSG_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/W	0h	interrupt status clear for SVBUS timeout errors
1-0	PARITY	R/W	0h	interrupt status clear for parity errors

14.3.6.1.4 PRU_ICSSG_DDRAM Registers

Table 14-6786 lists the memory-mapped registers for the PRU_ICSSG_DDRAM0 registers. All register offset addresses not listed in Table 14-6786 should be considered as reserved locations and the register contents should not be modified.

Table 14-10142. PRU_ICSSG_DDRAM Instances

Instance	Base Address
PRU_ICSSG0_DRAM0_SLV_RAM	3000 0000h
PRU_ICSSG1_DRAM0_SLV_RAM	3008 0000h
PRU_ICSSG0_DRAM1_SLV_RAM	3000 2000h
PRU_ICSSG1_DRAM1_SLV_RAM	3008 2000h

Table 14-10143. PRU_ICSSG_DDRAM Registers

Offset	Acronym	Register Name	PRU_ICSSG0_DRAM0_SLV_RAM Physical Address	PRU_ICSSG1_DRAM0_SLV_RAM Physical Address
0h + formula	ICSSG_DRAM_REG_y	RAM memory word	3000 0000h + formula	3008 0000h + formula

Table 14-10144. PRU_ICSSG_DDRAM Registers 2

Offset	Acronym	Register Name	PRU_ICSSG0_DRAM1_SLV_RAM Physical Address	PRU_ICSSG1_DRAM1_SLV_RAM Physical Address
0h + formula	ICSSG_DRAM_REG_y	RAM memory word	3000 2000h + formula	3008 2000h + formula

1 ICSSG_DRAM_REG_y Register (Offset = 0h + formula) [reset = 0h]

ICSSG_DRAM_REG_y is shown in Figure 14-3358 and described in Table 14-6789.

Return to Summary Table.

The RAM memory words provide memory mapped random access data storage.

Offset = 0h + (y * 4h); where y = 0h to 7FFh

Table 14-10145. ICSSG_DRAM_REG_y Instances

Instance	Physical Address
PRU_ICSSG0_DRAM0_SLV_RAM	3000 0000h + formula
PRU_ICSSG0_DRAM1_SLV_RAM	3000 2000h + formula
PRU_ICSSG1_DRAM0_SLV_RAM	3008 0000h + formula
PRU_ICSSG1_DRAM1_SLV_RAM	3008 2000h + formula

Figure 14-3358. ICSSG_DRAM_REG_y Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTE3</td><td colspan="8">BYTE2</td><td colspan="8">BYTE1</td><td colspan="8">BYTE0</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10147. ICSSG_DRAM_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BYTE3	R/W	0h	This is the MSB (Most Significant Byte)
23-16	BYTE2	R/W	0h	This is the UMB (Upper Middle Byte)
15-8	BYTE1	R/W	0h	This is the LMB (Lower Middle Byte)
7-0	BYTE0	R/W	0h	This is the LSB (Least Significant Byte)

14.3.6.1.5 PRU_ICSSG_CFG Registers

Table 14-6791 lists the memory-mapped registers for the PRU_ICSSG_CFG registers. All register offset addresses not listed in Table 14-6791 should be considered as reserved locations and the register contents should not be modified.

Table 14-10148. PRU_ICSSG_CFG Instances

Instance	Base Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6000h
PRU_ICSSG1_PR1_CFG_SLV	300A 6000h

Table 14-10149. PRU_ICSSG_CFG Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_CFG_SLV Physical Address	PRU_ICSSG1_PR1_CFG_SLV Physical Address
0h	ICSSG_PID_REG	PID Register	3002 6000h	300A 6000h
4h	ICSSG_HWDIS_REG	HW Disable Register	3002 6004h	300A 6004h
8h	ICSSG_GPCFG0_REG	GP Configuration 0 Register	3002 6008h	300A 6008h
Ch	ICSSG_GPCFG1_REG	GP Configuration 1 Register	3002 600Ch	300A 600Ch
10h	ICSSG_CGR_REG	Clock Gating Register	3002 6010h	300A 6010h
14h	ICSSG_GPECFG0_REG	GP Enc Configuration 0 Register	3002 6014h	300A 6014h
18h	ICSSG_GPECFG1_REG	GP Enc Configuration 1 Register	3002 6018h	300A 6018h
1Ch	ICSSG_RSTISO_REG	Reset Isolation Register	3002 601Ch	300A 601Ch
2Ch	ICSSG_MII_RT_REG	MII_RT Event Enable Register	3002 602Ch	300A 602Ch
30h	ICSSG_IEPCLK_REG	IEP Configuration Register	3002 6030h	300A 6030h
34h	ICSSG_SPP_REG	Scratchpad Priority and Shift Register	3002 6034h	300A 6034h
3Ch	ICSSG_CORE_SYNC_REG	CoreSync Configuration Register	3002 603Ch	300A 603Ch
40h	ICSSG_SA_MX_REG	SA Mux Selection Register	3002 6040h	300A 6040h
44h	ICSSG_PRU0_SD_CFG_REG	SD Config Register	3002 6044h	300A 6044h
48h	ICSSG_PRU0_SD_CLK_SEL_REG0	PRU0 FD, ACC and Clock Selection Register 0	3002 6048h	300A 6048h
4Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG0	PRU0 FD and Over Sample Size Register 0	3002 604Ch	300A 604Ch
50h	ICSSG_PRU0_SD_CLK_SEL_REG1	PRU0 FD, ACC and Clock Selection Register 1	3002 6050h	300A 6050h
54h	ICSSG_PRU0_SD_SAMPLE_SIZE_REG1	PRU0 FD and Over Sample Size Register 1	3002 6054h	300A 6054h
58h	ICSSG_PRU0_SD_CLK_SEL_REG2	PRU0 FD, ACC and Clock Selection Register 2	3002 6058h	300A 6058h
5Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG2	PRU0 FD and Over Sample Size Register 2	3002 605Ch	300A 605Ch
60h	ICSSG_PRU0_SD_CLK_SEL_REG3	PRU0 FD, ACC and Clock Selection Register 3	3002 6060h	300A 6060h
64h	ICSSG_PRU0_SD_SAMPLE_SIZE_REG3	PRU0 FD and Over Sample Size Register 3	3002 6064h	300A 6064h
68h	ICSSG_PRU0_SD_CLK_SEL_REG4	PRU0 FD, ACC and Clock Selection Register 4	3002 6068h	300A 6068h
6Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG4	PRU0 FD and Over Sample Size Register 4	3002 606Ch	300A 606Ch
70h	ICSSG_PRU0_SD_CLK_SEL_REG5	PRU0 FD, ACC and Clock Selection Register 5	3002 6070h	300A 6070h

Table 14-10149. PRU_ICSSG_CFG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_CFG_SLV Physical Address	PRU_ICSSG1_PR1_CFG_SLV Physical Address
74h	ICSSG_PRU0_SD_SAMPLE_SIZE_REG5	PRU0 FD and Over Sample Size Register 5	3002 6074h	300A 6074h
78h	ICSSG_PRU0_SD_CLK_SEL_REG6	PRU0 FD, ACC and Clock Selection Register 6	3002 6078h	300A 6078h
7Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG6	PRU0 FD and Over Sample Size Register 6	3002 607Ch	300A 607Ch
80h	ICSSG_PRU0_SD_CLK_SEL_REG7	PRU0 FD, ACC and Clock Selection Register 7	3002 6080h	300A 6080h
84h	ICSSG_PRU0_SD_SAMPLE_SIZE_REG7	PRU0 FD and Over Sample Size Register 7	3002 6084h	300A 6084h
88h	ICSSG_PRU0_SD_CLK_SEL_REG8	PRU0 FD, ACC and Clock Selection Register 8	3002 6088h	300A 6088h
8Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG8	PRU0 FD and Over Sample Size Register 8	3002 608Ch	300A 608Ch
90h	ICSSG_PRU1_SD_CFG_REG	SD Config Register	3002 6090h	300A 6090h
94h	ICSSG_PRU1_SD_CLK_SEL_REG0	PRU1 FD, ACC and Clock Selection Register 0	3002 6094h	300A 6094h
98h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG0	PRU1 FD and Over Sample Size Register 0	3002 6098h	300A 6098h
9Ch	ICSSG_PRU1_SD_CLK_SEL_REG1	PRU1 FD, ACC and Clock Selection Register 1	3002 609Ch	300A 609Ch
A0h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG1	PRU1 FD and Over Sample Size Register 1	3002 60A0h	300A 60A0h
A4h	ICSSG_PRU1_SD_CLK_SEL_REG2	PRU1 FD, ACC and Clock Selection Register 2	3002 60A4h	300A 60A4h
A8h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG2	PRU1 FD and Over Sample Size Register 2	3002 60A8h	300A 60A8h
ACh	ICSSG_PRU1_SD_CLK_SEL_REG3	PRU1 FD, ACC and Clock Selection Register 3	3002 60ACh	300A 60ACh
B0h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG3	PRU1 FD and Over Sample Size Register 3	3002 60B0h	300A 60B0h
B4h	ICSSG_PRU1_SD_CLK_SEL_REG4	PRU1 FD, ACC and Clock Selection Register 4	3002 60B4h	300A 60B4h
B8h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG4	PRU1 FD and Over Sample Size Register 4	3002 60B8h	300A 60B8h
BCh	ICSSG_PRU1_SD_CLK_SEL_REG5	PRU1 FD, ACC and Clock Selection Register 5	3002 60BCh	300A 60BCh
C0h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG5	PRU1 FD and Over Sample Size Register 5	3002 60C0h	300A 60C0h
C4h	ICSSG_PRU1_SD_CLK_SEL_REG6	PRU1 FD, ACC and Clock Selection Register 6	3002 60C4h	300A 60C4h
C8h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG6	PRU1 FD and Over Sample Size Register 6	3002 60C8h	300A 60C8h
CCh	ICSSG_PRU1_SD_CLK_SEL_REG7	PRU1 FD, ACC and Clock Selection Register 7	3002 60CCh	300A 60CCh
D0h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG7	PRU1 FD and Over Sample Size Register 7	3002 60D0h	300A 60D0h
D4h	ICSSG_PRU1_SD_CLK_SEL_REG8	PRU1 FD, ACC and Clock Selection Register 8	3002 60D4h	300A 60D4h
D8h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG8	PRU1 FD and Over Sample Size Register 8	3002 60D8h	300A 60D8h

Table 14-10149. PRU_ICSSG_CFG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_CFG_SLV Physical Address	PRU_ICSSG1_PR1_CFG_SLV Physical Address
E0h	ICSSG_PRU0_ED_RX_CFG_REG	PRU0 ED Receive Global Configuration Register	3002 60E0h	300A 60E0h
E4h	ICSSG_PRU0_ED_TX_CFG_REG	PRU0 ED Transmit Global Configuration Register	3002 60E4h	300A 60E4h
E8h	ICSSG_PRU0_ED_CH0_CFG0_REG	PRU0 ED Channel 0 Configuration 0 Register	3002 60E8h	300A 60E8h
ECh	ICSSG_PRU0_ED_CH0_CFG1_REG	PRU0 ED Channel 0 Configuration 1 Register	3002 60ECh	300A 60ECh
F0h	ICSSG_PRU0_ED_CH1_CFG0_REG	PRU0 ED Channel 1 Configuration 0 Register	3002 60F0h	300A 60F0h
F4h	ICSSG_PRU0_ED_CH1_CFG1_REG	PRU0 ED Channel 1 Configuration 1 Register	3002 60F4h	300A 60F4h
F8h	ICSSG_PRU0_ED_CH2_CFG0_REG	PRU0 ED Channel 2 Configuration 0 Register	3002 60F8h	300A 60F8h
FCh	ICSSG_PRU0_ED_CH2_CFG1_REG	PRU0 ED Channel 2 Configuration 1 Register	3002 60FCh	300A 60FCh
100h	ICSSG_PRU1_ED_RX_CFG_REG	PRU1 ED Receive Global Configuration Register	3002 6100h	300A 6100h
104h	ICSSG_PRU1_ED_TX_CFG_REG	PRU1 ED Transmit Global Configuration Register	3002 6104h	300A 6104h
108h	ICSSG_PRU1_ED_CH0_CFG0_REG	PRU1 ED Channel 0 Configuration 0 Register	3002 6108h	300A 6108h
10Ch	ICSSG_PRU1_ED_CH0_CFG1_REG	PRU1 ED Channel 0 Configuration 1 Register	3002 610Ch	300A 610Ch
110h	ICSSG_PRU1_ED_CH1_CFG0_REG	PRU1 ED Channel 1 Configuration 0 Register	3002 6110h	300A 6110h
114h	ICSSG_PRU1_ED_CH1_CFG1_REG	PRU1 ED Channel 1 Configuration 1 Register	3002 6114h	300A 6114h
118h	ICSSG_PRU1_ED_CH2_CFG0_REG	PRU1 ED Channel 2 Configuration 0 Register	3002 6118h	300A 6118h
11Ch	ICSSG_PRU1_ED_CH2_CFG1_REG	PRU1 ED Channel 2 Configuration 1 Register	3002 611Ch	300A 611Ch
124h	ICSSG_RTU0_POKE_EN0_REG	RTU0 Poke Enable 0 Register	3002 6124h	300A 6124h
12Ch	ICSSG_RTU1_POKE_EN0_REG	RTU1 Poke Enable 0 Register	3002 612Ch	300A 612Ch
130h	ICSSG_PWM0	PWM0 Trip Configuration Register	3002 6130h	300A 6130h
134h	ICSSG_PWM1	PWM1 Trip Configuration Register	3002 6134h	300A 6134h
138h	ICSSG_PWM2	PWM2 Trip Configuration Register	3002 6138h	300A 6138h
13Ch	ICSSG_PWM3	PWM3 Trip Configuration Register	3002 613Ch	300A 613Ch
140h	ICSSG_PWM0_0	PWM0 State Configuration 0 Register	3002 6140h	300A 6140h
144h	ICSSG_PWM0_1	PWM0 State Configuration 1 Register	3002 6144h	300A 6144h
148h	ICSSG_PWM0_2	PWM0 State Configuration 2 Register	3002 6148h	300A 6148h
14Ch	ICSSG_PWM1_0	PWM1 State Configuration 0 Register	3002 614Ch	300A 614Ch
150h	ICSSG_PWM1_1	PWM1 State Configuration 1 Register	3002 6150h	300A 6150h
154h	ICSSG_PWM1_2	PWM1 State Configuration 2 Register	3002 6154h	300A 6154h

Table 14-10149. PRU_ICSSG_CFG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_CFG_SLV Physical Address	PRU_ICSSG1_PR1_CFG_SLV Physical Address
158h	ICSSG_PWM2_0	PWM2 State Configuration 0 Register	3002 6158h	300A 6158h
15Ch	ICSSG_PWM2_1	PWM2 State Configuration 1 Register	3002 615Ch	300A 615Ch
160h	ICSSG_PWM2_2	PWM2 State Configuration 2 Register	3002 6160h	300A 6160h
164h	ICSSG_PWM3_0	PWM3 State Configuration 0 Register	3002 6164h	300A 6164h
168h	ICSSG_PWM3_1	PWM3 State Configuration 1 Register	3002 6168h	300A 6168h
16Ch	ICSSG_PWM3_2	PWM3 State Configuration 2 Register	3002 616Ch	300A 616Ch
170h	ICSSG_SPIN_LOCK0	Spin Lock 0 Register	3002 6170h	300A 6170h
174h	ICSSG_SPIN_LOCK1	Spin Lock 1 Register	3002 6174h	300A 6174h
178h	ICSSG_PA_STAT_PDSP_CFG0	PA STATS PDSP0 Vector 0 Register	3002 6178h	300A 6178h
17Ch	ICSSG_PA_STAT_PDSP_STAT0	PA STATS PDSP0 Status 0 Register	3002 617Ch	300A 617Ch
180h	ICSSG_PA_STAT_PDSP_CFG1	PA STATS PDSP0 Vector 1 Register	3002 6180h	300A 6180h
184h	ICSSG_PA_STAT_PDSP_STAT1	PA STATS PDSP0 Status 1 Register	3002 6184h	300A 6184h
188h	ICSSG_PA_STAT_PDSP_CFG2	PA STATS PDSP0 Vector 2 Register	3002 6188h	300A 6188h
18Ch	ICSSG_PA_STAT_PDSP_STAT2	PA STATS PDSP0 Status 2 Register	3002 618Ch	300A 618Ch
190h	ICSSG_PA_STAT_PDSP_CFG3	PA STATS PDSP0 Vector 3 Register	3002 6190h	300A 6190h
194h	ICSSG_PA_STAT_PDSP_STAT3	PA STATS PDSP0 Status 3 Register	3002 6194h	300A 6194h

1 ICSSG_PID_REG Register (Offset = 0h) [reset = Xh]

ICSSG_PID_REG is shown in Figure 14-3359 and described in Table 14-6793.

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PID Register.

Table 14-10150. ICSSG_PID_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6000h
PRU_ICSSG1_PR1_CFG_SLV	300A 6000h

Figure 14-3359. ICSSG_PID_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">MODID</td></tr>
<tr><td colspan="16">6B00h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="5">R-X</td><td colspan="3">R-1h</td><td colspan="2">R-0h</td><td colspan="6">R-X</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10152. ICSSG_PID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6B00h	Module ID field. ICSS_G.
15-11	REVRTL	R	0h	RTL revision. 190H in this device.
10-8	REVMAJ	R	1h	Major
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	3h	Minor. 03H in this device.

2 ICSSG_HWDIS_REG Register (Offset = 4h) [reset = X]

ICSSG_HWDIS_REG is shown in Figure 14-3360 and described in Table 14-6795.

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HW Disable Register

Table 14-10153. ICSSG_HWDIS_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6004h
PRU_ICSSG1_PR1_CFG_SLV	300A 6004h

Figure 14-3360. ICSSG_HWDIS_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">HWDIS</td></tr>
<tr><td colspan="24">R-X</td><td colspan="8">R-X</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10155. ICSSG_HWDIS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	HWDIS	R	X	Read the state of the efuse bits which drive pr1_hw_disable[7:0]

3 ICSSG_GPCFG0_REG Register (Offset = 8h) [reset = X]

ICSSG_GPCFG0_REG is shown in Figure 14-3361 and described in Table 14-6797.

Return to Summary Table.

GP Configuration 0 Register

Table 14-10156. ICSSG_GPCFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6008h
PRU_ICSSG1_PR1_CFG_SLV	300A 6008h

Figure 14-3361. ICSSG_GPCFG0_REG Register

31	30	29	28	27	26	25	24
RESERVED		PR1_PRU0_GP_MUX_SEL				PRU0_GPO_SH1_SEL	PRU0_GPO_DIV1
R/W-X		R/W-0h				R-0h	R/W-0h
23	22	21	20	19	18	17	16
PRU0_GPO_DIV1				PRU0_GPO_DIV0			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
PRU0_GPO_DIV0	PRU0_GPO_MODE	PRU0_GPI_SB	PRU0_GPI_DIV1				
R/W-0h	R/W-0h	R/W1C-0h	R/W-0h				
7	6	5	4	3	2	1	0
PRU0_GPI_DIV0					PRU0_GPI_CLK_MODE	PRU0_GPI_MODE	
R/W-0h					R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to clear Bit; *-n* = value after reset

Table 14-10158. ICSSG_GPCFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-26	PR1_PRU0_GP_MUX_SEL	R/W	0h	Controls the icss_wrap mux sel 0h = GP selected 1h = EnDAT mode 2h = MII mode 3h = SD mode
25	PRU0_GPO_SH1_SEL	R	0h	This defines which shadow register is currently getting used for GPO shifting. 0h = gpo_sh0 is selected 1h = gpo_sh1 is selected
24-20	PRU0_GPO_DIV1	R/W	0h	Divisor value , divide by PRU0_GPO_DIV1 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved

Table 14-10158. ICSSG_GPCFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-15	PRU0_GPO_DIV0	R/W	0h	Divisor value , divide by PRU0_GPO_DIV0 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
14	PRU0_GPO_MODE	R/W	0h	0h = Parallel output mode 1h = Serial output mode, pru<n>_r30[31] enables shift pru<n>r30[0] is shift data out pru<n>r30[1] is shift clock
13	PRU0_GPI_SB	R/W1C	0h	PRU0_GPI_SB set when first capture on 1 on r31_status[0] r31_status[29] == PRU0_GPI_SB Read 1 Start Bit event occurred Read 0 Start Bit event has not occurred Write 1 Will clear PRU0_GPI_SB, 28 bit shift register, and shift counter Write 0 No Effect
12-8	PRU0_GPI_DIV1	R/W	0h	Divisor value , divide by PRU0_GPI_DIV1 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
7-3	PRU0_GPI_DIV0	R/W	0h	Divisor value , divide by PRU0_GPI_DIV0 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
2	PRU0_GPI_CLK_MODE	R/W	0h	Parallel 16-bit capture mode clock edge 0h = Use the positive edge of pru<n>_r31_status[16] 1h = Use the negative edge of pru<n>_r31_status[16]
1-0	PRU0_GPI_MODE	R/W	0h	0h = Direct connect of pru<n>_r31_status[29:0] 1h = Parallel 16-bit capture mode. pru<n>_r31_status [15:0] is captured using pru<n>_r31_status [16] 2h = 29-bit shift. pru<n>_r31_status[0] -> r31_status[0] -> r31_status[1] -> r_status[28] -> bit bucket 3h = mii_rt mode. Selects mii_rt pru0 bus

4 ICSSG_GPCFG1_REG Register (Offset = Ch) [reset = X]

ICSSG_GPCFG1_REG is shown in Figure 14-3362 and described in Table 14-6799.

Return to Summary Table.

GP Configuration 1 Register

Table 14-10159. ICSSG_GPCFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 600Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 600Ch

Figure 14-3362. ICSSG_GPCFG1_REG Register

31	30	29	28	27	26	25	24
RESERVED		PR1_PRU1_GP_MUX_SEL				PRU1_GPO_SH1_SEL	PRU1_GPO_DIV1
R/W-X		R/W-0h				R-0h	R/W-0h

23	22	21	20	19	18	17	16
PRU1_GPO_DIV1				PRU1_GPO_DIV0			
R/W-0h				R/W-0h			

15	14	13	12	11	10	9	8
PRU1_GPO_DIV0	PRU1_GPO_MODE	PRU1_GPI_SB	PRU1_GPI_DIV1				
R/W-0h	R/W-0h	R/W1C-0h	R/W-0h				

7	6	5	4	3	2	1	0
PRU1_GPI_DIV0					PRU1_GPI_CLK_MODE	PRU1_GPI_MODE	
R/W-0h					R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to clear Bit; *-n* = value after reset

Table 14-10161. ICSSG_GPCFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-26	PR1_PRU1_GP_MUX_SEL	R/W	0h	Controls the icss_wrap mux sel 0h = GP selected 1h = EnDAT mode 2h = MII mode 3h = SD mode
25	PRU1_GPO_SH1_SEL	R	0h	This defines which shadow register is currently getting used for GPO shifting. 0h = gpo_sh0 is selected 1h = gpo_sh1 is selected
24-20	PRU1_GPO_DIV1	R/W	0h	Divisor value , divide by PRU1_GPO_DIV1 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved

Table 14-10161. ICSSG_GPCFG1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-15	PRU1_GPO_DIV0	R/W	0h	Divisor value , divide by PRU1_GPO_DIV0 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
14	PRU1_GPO_MODE	R/W	0h	0hh = Parallel output mode 0x1h = Serial output mode, pru<n>_r30[31] enables shift pru<n>r30[0] is shift data out pru<n>r30[1] is shift clock
13	PRU1_GPI_SB	R/W1C	0h	PRU1_GPI_SB set when first capture on 1 on r31_status[0] r31_status[29] == PRU1_GPI_SB Read 1 Start Bit event occurred Read 0 Start Bit event has not occurred Write 1 Will clear PRU1_GPI_SB, 28 bit shift register, and shift counter Write 0 No Effect
12-8	PRU1_GPI_DIV1	R/W	0h	Divisor value , divide by PRU1_GPI_DIV1 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
7-3	PRU1_GPI_DIV0	R/W	0h	Divisor value , divide by PRU1_GPI_DIV0 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
2	PRU1_GPI_CLK_MODE	R/W	0h	Parallel 16-bit capture mode clock edge 0h = Use the positive edge of pru<n>_r31_status[16] 0x1h = Use the negative edge of pru<n>_r31_status[16]
1-0	PRU1_GPI_MODE	R/W	0h	0h = Direct connect of pru<n>_r31_status[29:0] 1h = Parallel 16-bit capture mode. pru<n>_r31_status [15:0] is captured using pru<n>_r31_status [16] 2h = 29-bit shift. pru<n>_r31_status[0] -> r31_status[0]->r31_status[1]..-> r_status[28] -> bit bucket 3h = mii_rt mode. Selects mii_rt pru1 bus

5 ICSSG_CGR_REG Register (Offset = 10h) [reset = X]

ICSSG_CGR_REG is shown in Figure 14-3363 and described in Table 14-6801.

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Clock Gating Register

Table 14-10162. ICSSG_CGR_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6010h
PRU_ICSSG1_PR1_CFG_SLV	300A 6010h

Figure 14-3363. ICSSG_CGR_REG Register

31	30	29	28	27	26	25	24
ICSS_STOP_ACK	ICSS_STOP_REQ	ICSS_PWR_IDLE	RESERVED				
R/W-1h	R-0h	R/W-1h	R/W-X				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		BOTTTOM_HALF_CLK_GATE_EN	TOP_HALF_CLK_GATE_EN	AUTO_SLICE1_CLK_GATE_EN	AUTO_SLICE0_CLK_GATE_EN	IEP_CLK_EN	IEP_CLK_STOP_ACK
R/W-X		R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IEP_CLK_STOP_REQ	ECAP_CLK_EN	ECAP_CLK_STOP_ACK	ECAP_CLK_STOP_REQ	UART_CLK_EN	UART_CLK_STOP_ACK	UART_CLK_STOP_REQ	INTC_CLK_EN
R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTC_CLK_STOP_ACK	INTC_CLK_STOP_REQ	RESERVED					
R-0h	R/W-0h	R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10164. ICSSG_CGR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ICSS_STOP_ACK	R/W	1h	ICSS 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
30	ICSS_STOP_REQ	R	0h	ICSS 0h = No Gate Clock Request 1h = Gate Clock Request
29	ICSS_PWR_IDLE	R/W	1h	ICSS 0h = Not Idle 1h = Idle
28-22	RESERVED	R/W	X	
21	BOTTTOM_HALF_CLK_GATE_EN	R/W	1h	Bottom Clock Gate for slice 0 and 1 0 = Disable Clock 1 = Enable Clock
20	TOP_HALF_CLK_GATE_EN	R/W	1h	Top Clock Gate for slice 0 and 1 0 = Disable Clock 1 = Enable Clock

Table 14-10164. ICSSG_CGR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	AUTO_SLICE1_CLK_GATE_EN	R/W	0h	Auto Clock Gate for slice 1 Ethernet 0 = Disable Clock 1 = Enable Auto Clock
18	AUTO_SLICE0_CLK_GATE_EN	R/W	0h	Auto Clock Gate for slice 0 Ethernet 0 = Disable Clock 1 = Enable Clock
17	IEP_CLK_EN	R/W	1h	IEP 0h = Disable Clock 1h = Enable Clock
16	IEP_CLK_STOP_ACK	R	0h	IEP 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
15	IEP_CLK_STOP_REQ	R/W	0h	IEP 0h = do not request to stop clock 1h = request to stop clock
14	ECAP_CLK_EN	R/W	1h	ECAP 0h = Disable Clock 1h = Enable Clock
13	ECAP_CLK_STOP_ACK	R	0h	ECAP 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
12	ECAP_CLK_STOP_REQ	R/W	0h	ECAP 0h = do not request to stop clock 1h = request to stop clock
11	UART_CLK_EN	R/W	1h	UART 0h = Disable Clock 1h = Enable Clock
10	UART_CLK_STOP_ACK	R	0h	UART 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
9	UART_CLK_STOP_REQ	R/W	0h	UART 0h = do not request to stop clock 1h = request to stop clock
8	INTC_CLK_EN	R/W	1h	INTC 0h = Disable Clock 1h = Enable Clock
7	INTC_CLK_STOP_ACK	R	0h	INTC 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
6	INTC_CLK_STOP_REQ	R/W	0h	INTC 0h = do not request to stop clock 1h = request to stop clock

Table 14-10164. ICSSG_CGR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	RESERVED	R/W	X	

6 ICSSG_GPECFG0_REG Register (Offset = 14h) [reset = X]

ICSSG_GPECFG0_REG is shown in Figure 14-3364 and described in Table 14-6803.

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GP Enc Configuration 0 Register

Table 14-10165. ICSSG_GPECFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6014h
PRU_ICSSG1_PR1_CFG_SLV	300A 6014h

Figure 14-3364. ICSSG_GPECFG0_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>PRU0_GPO_SHIFT_CLK_DONE</td><td>PRU0_GPO_SHIFT_CLK_HIGH</td></tr>
<tr><td colspan="6">R/W-X</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRU0_GPO_SHIFT_CNT</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>PRU0_GPO_SHIFT_GP_EN</td><td>PRU0_GPO_SHIFT_CLK_FREE</td><td>PRU0_GPO_SHIFT_SWAP</td><td colspan="2">RESERVED</td><td>PRU0_GPI_SHIFT_EN</td><td>PRU0_GPI_SB_P</td></tr>
<tr><td>R/W-X</td><td>R/W-0h</td><td>R/W-1h</td><td>R/W-0h</td><td colspan="2">R/W-X</td><td>R/W-1h</td><td>R/W-1h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10167. ICSSG_GPECFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	PRU0_GPO_SHIFT_CLK_DONE	R/W	0h	Shift Clock Done is active when PRU0_GPO_SHIFT_CNT is none zero 0h = Shift Bit Count has not expired 1h = Set when Shift Bit Count has expired Write 1 to clear. This is only valid when PRU0/1_GPO_SHIFT_CLK_FREE is not set
16	PRU0_GPO_SHIFT_CLK_HIGH	R/W	0h	Shift Clock Stop High 0h = Stop Low, if Stop is enabled 1h = Stop High,if Stop is enabled This is only active when PRU0/1_GPO_SHIFT_CLK_FREE is not set Also, you must define PRU0/1_GPO_SHIFT_CNT Note: Software can only update once during initial configuration

Table 14-10167. ICSSG_GPECFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	PRU0_GPO_SHIFT_CNT	R/W	0h	Shift Bit Count 0h – 0x3h = Reserved PRU0_GPO_SHIFT_CNT determine how many bits to shift out. After the count is reached it will stop shifting , the last bit will remain persistent. 0x4h = shift 4 bits 0x5h = shift 5 bits 0xff = shift 255 bits This is only active when PRU0/1_GPO_SHIFT_CLK_FREE is not set Note: first new shift data is before the first clock edge. Due to this fact, the number of shift_clk is one minus PRU0/1_GPO_SHIFT_CNT
7	RESERVED	R/W	X	
6	PRU0_GPO_SHIFT_GP_EN	R/W	0h	Enable pru<n>r30[15:2] control during shift out mode 0h = direction connection pru<n>r30[15:2] is controlled by r30[15:2] 1h = shadow connection pru<n>r30[15:2] is controlled by r30_shadow[15:2] Note: r30_shadow[15:2] is updated by r30[15:2] when r30[28] is high
5	PRU0_GPO_SHIFT_CLK_FREE	R/W	1h	Free Running Clock Mode This controls the behavior of the Shift Clock Out 0h = Shift Clock Out only active when bits are shifted out Default state of Shift Clock Out is low before and after shift (Shift is enabled only when shift_enable is TRUE and PRU0_GPO_SHIFT_CNT has not expired 1h = Shift Clock Out Free running The clock will start and remain active independent of shifting out new data When shift_enable is de-asserted and shift data out is completed, data out will go low
4	PRU0_GPO_SHIFT_SWAP	R/W	0h	0h = No Swap The shadow copy gets loaded with R30[15:0] 1h = Swap The shadow copy gets loaded with R30[0:15]
3-2	RESERVED	R/W	X	
1	PRU0_GPI_SHIFT_EN	R/W	1h	GPI Shift In Enable 0h = disable This will freeze the current shift in process This will also disable the looking for a SB if SB event has not occurred 1h = enable
0	PRU0_GPI_SB_P	R/W	1h	GPI Shift In Start Bit Polarity 0h = Active Low SB is set on the first “0” seen 1h = Active High SB is set on the first “1” seen

7 ICSSG_GPECFG1_REG Register (Offset = 18h) [reset = X]

ICSSG_GPECFG1_REG is shown in Figure 14-3365 and described in Table 14-6805.

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GP Enc Configuration 1 Register

Table 14-10168. ICSSG_GPECFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6018h
PRU_ICSSG1_PR1_CFG_SLV	300A 6018h

Figure 14-3365. ICSSG_GPECFG1_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PRU1_GPO_SHIFT_CLK_DONE	PRU1_GPO_SHIFT_CLK_HIGH
R/W-X						R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_GPO_SHIFT_CNT							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRU1_GPO_SHIFT_GP_EN	PRU1_GPO_SHIFT_CLK_FREE	PRU1_GPO_SHIFT_SWAP	RESERVED		PRU1_GPI_SHIFT_EN	PRU1_GPI_SB_P
R/W-X	R/W-0h	R/W-1h	R/W-0h	R/W-X		R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10170. ICSSG_GPECFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	PRU1_GPO_SHIFT_CLK_DONE	R/W	0h	Shift Clock Done is active when PRU1_GPO_SHIFT_CNT is none zero 0h = Shift Bit Count has not expired 1h = Set when Shift Bit Count has expired Write 1 to clear This is only valid when PRU0/1_GPO_SHIFT_CLK_FREE is not set
16	PRU1_GPO_SHIFT_CLK_HIGH	R/W	0h	Shift Clock Stop High 0h = Stop Low, if Stop is enabled 1h = Stop High,if Stop is enabled This is only valid when PRU0/1_GPO_SHIFT_CLK_FREE is not set Also, you must define PRU0/1_GPO_SHIFT_CNT Note: Software can only update once during intial configuration

Table 14-10170. ICSSG_GPECFG1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	PRU1_GPO_SHIFT_CNT	R/W	0h	Shift Bit Count 0h – 3h = Reserved PRU1_GPO_SHIFT_CNT determine how many bits to shift out. After the count is reached it will stop shifting , the last bit will remain presistant. 4h = shift 4 bits 5h = shift 5 bits ffh = shift 255 bits This is only active when PRU0/1_GPO_SHIFT_CLK_FREE is not set Note: first new shift data is before the first clock edge Do to this fact, the number of shift_clk is one minus PRU0/1_GPO_SHIFT_CNT
7	RESERVED	R/W	X	
6	PRU1_GPO_SHIFT_GP_EN	R/W	0h	Enable pru<n>r30[15:2] control during shift out mode 0h = direction connection pru<n>r30[15:2] is controlled by r30[15:2] 1h = shadow connection pru<n>r30[15:2] is controlled by r30_shadow[15:2] Note: r30_shadow[15:2] is updated by r30[15:2] when r30[28] is high
5	PRU1_GPO_SHIFT_CLK_FREE	R/W	1h	Free Running Clock Mode This controls the behavior of the Shift Clock Out 0h = Shift Clock Out only active when bits are shifted out Default state of Shift Clock Out is low before and after shift 1h = Shift Clock Out Free running The clock will start and remain active independent of shifting out new data
4	PRU1_GPO_SHIFT_SWAP	R/W	0h	0h = No Swap The shadow copy gets loaded with R30[15:0] 1h = Swap The shadow copy gets loaded with R30[0:15]
3-2	RESERVED	R/W	X	
1	PRU1_GPI_SHIFT_EN	R/W	1h	GPI Shift In Enable 0h = disable This will freeze the current shift in process This will also disable the looking for a SB if SB event has not occurred 1h = enable
0	PRU1_GPI_SB_P	R/W	1h	GPI Shift In Start Bit Polarity 0h = Active Low SB is set on the first “0” seen 1h = Active High SB is set on the first “1” seen

8 ICSSG_RSTISO_REG Register (Offset = 1Ch) [reset = X]

ICSSG_RSTISO_REG is shown in Figure 14-3366 and described in Table 14-6807.

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Reset Isolation Register

Table 14-10171. ICSSG_RSTISO_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 601Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 601Ch

Figure 14-3366. ICSSG_RSTISO_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					RESET_EDGE	RESET_ISO_ACK	RESET_ISO_REQ
R/W-X					W-0h	W-0h	R/W1C-1h

LEGEND: R/W = Read/Write; W = Write Only; R/W1C = Read/Write 1 to Clear-*n* = value after reset

Table 14-10173. ICSSG_RSTISO_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	RESET_EDGE	W	0h	Reset Edge Assertion Write 1 will reset ALL xfr2vbux_rx/tx, xfr2psi, scr_ext_cbass, and icss_g_core_ksdma_psil_endpt widgets
1	RESET_ISO_ACK	W	0h	Reset ISO Ack Write 1 will cause to acknowledge the Reset ISO Request
0	RESET_ISO_REQ	R/W1C	0h	Reset ISO Request Read 0 = No Active Requested Read 1 = Active Requested Write 1 to clear This bit gets set and held when pr1_rst_reset_iso_req input is asserted. Note, this will also cause system_event[3] to assert to INTC

9 ICSSG_MII_RT_REG Register (Offset = 2Ch) [reset = X]

ICSSG_MII_RT_REG is shown in Figure 14-3367 and described in Table 14-6809.

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MII_RT Event Enable Register

Table 14-10174. ICSSG_MII_RT_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 602Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 602Ch

Figure 14-3367. ICSSG_MII_RT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							MII_RT_EVENT_EN
R/W-X							R/W-1h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10176. ICSSG_MII_RT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	MII_RT_EVENT_EN	R/W	1h	Enables the MII_RT Events to the INTC 0h = disabled Use external events 1h = enabled Use MII_RT events

10 ICSSG_IEPCLK_REG Register (Offset = 30h) [reset = X]

ICSSG_IEPCLK_REG is shown in Figure 14-3368 and described in Table 14-6811.

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IEP Configuration Register

Table 14-10177. ICSSG_IEPCLK_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6030h
PRU_ICSSG1_PR1_CFG_SLV	300A 6030h

Figure 14-3368. ICSSG_IEPCLK_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						IEP1_SLV_EN	IEP_OCP_CLK_EN
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10179. ICSSG_IEPCLK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	IEP1_SLV_EN	R/W	0h	IEP1 Controller Counter Target enable 0h = disabled 1h = enabled When Enabled IEP1 counter[63:0] is from IEP0 during 64-bit mode IEP1 counter[31:0] is from IEP0 during 32-bit mode
0	IEP_OCP_CLK_EN	R/W	0h	Defines the source of the IEP CLK 0h = iep_clk is the source Async Mode 1h = ICSSGn_CORE_CLK is the source Sync Mode When this is selected the async IEP bridge is bypassed No transaction active when this bit get SET It can only get CLR by a HW reset Note: This means all PRU-ICSSG IOs which use internal IEP clock can use ether internal core clock or external IEP clock.

11 ICSSG_SPP_REG Register (Offset = 34h) [reset = X]

ICSSG_SPP_REG is shown in Figure 14-3369 and described in Table 14-6813.

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Scratchpad Priority and Shift Register

Table 14-10180. ICSSG_SPP_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6034h
PRU_ICSSG1_PR1_CFG_SLV	300A 6034h

Figure 14-3369. ICSSG_SPP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RTU_XFR_SHIFT_EN	XFR_BYTE_SHIFT_EN	XFR_SHIFT_EN	PRU1_PAD_HP_EN
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10182. ICSSG_SPP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	RTU_XFR_SHIFT_EN	R/W	0h	Shift enable using R0[4:0] to define the number of 32-bit offset for XIN and XOUT operations. 0h = disabled 1h = enabled When enabled, R0[4:0] (internal to RTU) defines the number of 32-bits the XIN and XOUT operation to the scratch pad bank. R0[4:0] = 2 XIN/XOUT of R4 will read/write bank<n>.R6 Wrap is supported R0[4:0] = 4 XIN/XOUT of R18:29 will read/write bank<n>.R22:R3
2	XFR_BYTE_SHIFT_EN	R/W	0h	Shift enable using R0[6:0] to define the number of 8-bit offset for XIN and XOUT operations. 0h = disabled 1h = enabled When enabled, R0[6:0] (internal to PRU/RTU) defines the number of 8-bits the XIN and XOUT operation to the scratch pad bank.

Table 14-10182. ICSSG_SPP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XFR_SHIFT_EN	R/W	0h	Shift enable using R0[4:0] to define the number of 32-bit offset for XIN and XOUT operations. 0h = disabled 1h = enabled When enabled, R0[4:0] (internal to PRU) defines the number of 32-bits the XIN and XOUT operation to the scratch pad bank. R0[4:0] = 2 XIN/XOUT of R4 will read/write bank<n>.R6 Wrap is supported R0[4:0] = 4 XIN/XOUT of R18:29 will read/write bank<n>.R22:R3
0	PRU1_PAD_HP_EN	R/W	0h	Reserved

12 ICSSG_CORE_SYNC_REG Register (Offset = 3Ch) [reset = X]

ICSSG_CORE_SYNC_REG is shown in Figure 14-3370 and described in Table 14-6815.

Return to Summary Table.

CoreSync Configuration Register.

Table 14-10183. ICSSG_CORE_SYNC_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 603Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 603Ch

Figure 14-3370. ICSSG_CORE_SYNC_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							CORE_VBUSP_SYNC_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10185. ICSSG_CORE_SYNC_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	CORE_VBUSP_SYNC_EN	R/W	0h	Defines the source of the internal CORE CLK 0h = ICSSGn_CORE_CLK is the source Async Mode 1h = ICSSGn_ICLK is the source (Sync Mode) When this is selected the async vbusp controller bridge is bypassed No transaction active when this bit get SET It can only get CLR by a HW reset The user should enable to get the lowest latency and high speed, since ICSSGn_ICLK should be at 250 MHz Note: This means all PRU_ICSSG IOs which use internal core clock (CORE_CLK) can use ether external core clock or external ICSSGn_ICLK.

13 ICSSG_SA_MX_REG Register (Offset = 40h) [reset = X]

ICSSG_SA_MX_REG is shown in Figure 14-3371 and described in Table 14-6817.

Return to Summary Table.

SA Mux Selection Register.

Table 14-10186. ICSSG_SA_MX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6040h
PRU_ICSSG1_PR1_CFG_SLV	300A 6040h

Figure 14-3371. ICSSG_SA_MX_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PWM_EFC_EN</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">PWM3_REMAP_EN</td><td colspan="2">PWM0_REMAP_EN</td></tr>
<tr><td colspan="4">R-X</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>G_MUX_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W-0h</td><td colspan="7">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10188. ICSSG_SA_MX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16	PWM_EFC_EN	R/W	0h	PWM efficiency mode 0 Legacy mode 1 Efficiency mode In this mode PWM SM will go from IDLE to ACTIVE and the same time PWM output will get updated during this SM state transition And IEP CMP flags will get auto HW cleared
15-12	RESERVED	R	X	
16-12	RESERVED	R	X	
11-10	PWM3_REMAP_EN	R/W	0h	If enabled, ICSSG Host interrupt 7 (PRU_ICSSGn_PR1_HOST_INTR_REQ_7) now controls pwm3_sync_in Only PRU_ICSSG0 controls the remap 0h = pwm_in_pwm3_sync_in_intc_h7 = pwm3_sync_in(no remap) 1h = pwm_in_pwm3_sync_in_intc_h7 = pr0_host_intr7_intr_pend (PRU_ICSSG0) 2h = pwm_in_pwm3_sync_in_intc_h7 = pr1_host_intr7_intr_pend (PRU_ICSSG1) 3h = Reserved

Table 14-10188. ICSSG_SA_MX_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	PWM0_REMAP_EN	R/W	0h	If enabled, ICSSG Host interrupt 6 (PRU_ICSSGn_PR1_HOST_INTR_REQ_6) now controls pwm0_sync_in Only PRU_ICSSG0 controls the remap 0h = pwm_in_pwm0_sync_in_intc_h6 = pwm_in_pwm0_sync_in (no remap) 1h = pwm_in_pwm0_sync_in_intc_h6 = pr0_host_intr6_intr_pend (PRU_ICSSG0) 2h = pwm_in_pwm0_sync_in_intc_h6 = pr1_host_intr6_intr_pend (PRU_ICSSG1) 3h = Reserved
7	G_MUX_EN	R/W	0h	See *PRU_ICSSG<k > I/O Signals* for details. 0 Default/Legacy 1 Few SD and EnDAT pins get remapped to enable different usecase
7	RESERVED	R/W	0h	Reserved
6-0	RESERVED	R/W	0h	Reserved

14 ICSSG_PRU0_SD_CFG_REG Register (Offset = 44h) [reset = X]

ICSSG_PRU0_SD_CFG_REG is shown in Figure 14-3372 and described in Table 14-6819.

Return to Summary Table.

SD Config Register.

Table 14-10189. ICSSG_PRU0_SD_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6044h
PRU_ICSSG1_PR1_CFG_SLV	300A 6044h

Figure 14-3372. ICSSG_PRU0_SD_CFG_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MAN_CLK_PERIOD</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MAN_CLK_CAL_DONE</td></tr>
<tr><td colspan="7">R-X</td><td>R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>MAN_STATUS</td><td colspan="4">CH_SEL</td><td>MAN_DATA_NV_EN</td><td>MAN_SD_EN</td><td>SHARE_EN</td></tr>
<tr><td>R-0h</td><td colspan="4">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read Only-*n* = value after reset

Table 14-10191. ICSSG_PRU0_SD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MAN_CLK_PERIOD	R	0h	Estimated Manchester clock period for SDx
23-17	RESERVED	R	X	
16	MAN_CLK_CAL_DONE	R	0h	Manchester clock calibration status for SDx. Manchester logic internal signal that indicates first completion of clock decoding phase (calibration stage 2 in Manchester decoding flowchart); status is sticky and cleared by reset
15	MAN_STATUS	R	0h	Manchester status for SDx.
14-11	CH_SEL	R/W	0h	Manchester SD channel select for the 3 status fields above 0 = SD0 .. 8 = SD8
10	MAN_DATA_NV_EN	R/W	0h	Manchester Decode Mode Data Inversion 0 = rising edge is 1 1 = falling edge is 1
9	MAN_SD_EN	R/W	0h	Manchester Decode Mode 0 = disable 1 = enable If enabled, then you need to enable one clock per data channel
8	SHARE_EN	R/W	0h	Load Share Enable 0 = PRUx owns SD0 - SD8 1 = RTUx owns SD0 - SD2, PRUx owns SD3 - SD5, TX_PRUx owns SD6 - SD8

Table 14-10191. ICSSG_PRU0_SD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	X	

15 ICSSG_PRU0_SD_CLK_SEL_REG0 Register (Offset = 48h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG0 is shown in Figure 14-3373 and described in Table 14-6821.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 0.

Table 14-10192. ICSSG_PRU0_SD_CLK_SEL_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6048h
PRU_ICSSG1_PR1_CFG_SLV	300A 6048h

Figure 14-3373. ICSSG_PRU0_SD_CLK_SEL_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRU0_FD_ZERO_MAX_0	PRU0_FD_ZERO_MAX_LIMIT_0					PRU0_FD_ZERO_MIN_0
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ZERO_MIN_LIMIT_0					RESERVED		
R/W-0h					R/W-X		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PRU0_SD_ACC_SEL0		RESERVED	PRU0_SD_CLK_INV0	PRU0_SD_CLK_SEL0	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10194. ICSSG_PRU0_SD_CLK_SEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_0	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_0	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_0	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10194. ICSSG_PRU0_SD_CLK_SEL_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_0	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL0	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV0	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL0	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

16 ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register (Offset = 4Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 is shown in Figure 14-3374 and described in Table 14-6823.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 0.

Table 14-10195. ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 604Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 604Ch

Figure 14-3374. ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_FD_EN_0	PRU0_FD_ONE_MAX_0	PRU0_FD_ONE_MAX_LIMIT_0					PRU0_FD_ONE_MIN_0
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ONE_MIN_LIMIT_0					PRU0_FD_WINDOW_SIZE_0		
R/W-0h					R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_SD_SAMPLE_SIZE0							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10197. ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_0	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_0	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_0	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10197. ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_0	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_0	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_0	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE0	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) Note: the 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 .. Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3hh, then the third clock after first 1 is detected, the VAL will get set.

17 ICSSG_PRU0_SD_CLK_SEL_REG1 Register (Offset = 50h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG1 is shown in Figure 14-3375 and described in Table 14-6825.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 1.

Table 14-10198. ICSSG_PRU0_SD_CLK_SEL_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6050h
PRU_ICSSG1_PR1_CFG_SLV	300A 6050h

Figure 14-3375. ICSSG_PRU0_SD_CLK_SEL_REG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_1	PRU0_FD_ZERO_MAX_LIMIT_1					PRU0_FD_ZERO_MIN_1
R/W-X	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_1					RESERVED		
R/W-0h					R/W-X		

7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL1		RESERVED	PRU0_SD_CLK_INV1	PRU0_SD_CLK_SEL1	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10200. ICSSG_PRU0_SD_CLK_SEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_1	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_1	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_1	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10200. ICSSG_PRU0_SD_CLK_SEL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_1	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL1	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV1	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL1	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

18 ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register (Offset = 54h) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 is shown in Figure 14-3376 and described in Table 14-6827.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 1.

Table 14-10201. ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6054h
PRU_ICSSG1_PR1_CFG_SLV	300A 6054h

Figure 14-3376. ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_1	PRU0_FD_ONE_MAX_1	PRU0_FD_ONE_MAX_LIMIT_1					PRU0_FD_ONE_MIN_1
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_1					PRU0_FD_WINDOW_SIZE_1		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE1							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10203. ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_1	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_1	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_1	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10203. ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_1	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_1	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_1	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE1	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) Note: the 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

19 ICSSG_PRU0_SD_CLK_SEL_REG2 Register (Offset = 58h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG2 is shown in Figure 14-3377 and described in Table 14-6829.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 2

Table 14-10204. ICSSG_PRU0_SD_CLK_SEL_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6058h
PRU_ICSSG1_PR1_CFG_SLV	300A 6058h

Figure 14-3377. ICSSG_PRU0_SD_CLK_SEL_REG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_2	PRU0_FD_ZERO_MAX_LIMIT_2					PRU0_FD_ZERO_MIN_2
R/W-X	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_2					RESERVED		
R/W-0h					R/W-X		

7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL2		RESERVED	PRU0_SD_CLK_INV2	PRU0_SD_CLK_SEL2	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10206. ICSSG_PRU0_SD_CLK_SEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_2	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_2	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_2	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10206. ICSSG_PRU0_SD_CLK_SEL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_2	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL2	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV2	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL2	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1= pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

20 ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register (Offset = 5Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 is shown in Figure 14-3378 and described in Table 14-6831.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 2.

Table 14-10207. ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 605Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 605Ch

Figure 14-3378. ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_2	PRU0_FD_ONE_MAX_2	PRU0_FD_ONE_MAX_LIMIT_2					PRU0_FD_ONE_MIN_2
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_2					PRU0_FD_WINDOW_SIZE_2		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE2							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10209. ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_2	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_2	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_2	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10209. ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_2	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_2	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_2	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE2	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) Note: the 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

21 ICSSG_PRU0_SD_CLK_SEL_REG3 Register (Offset = 60h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG3 is shown in Figure 14-3379 and described in Table 14-6833.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 3.

Table 14-10210. ICSSG_PRU0_SD_CLK_SEL_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6060h
PRU_ICSSG1_PR1_CFG_SLV	300A 6060h

Figure 14-3379. ICSSG_PRU0_SD_CLK_SEL_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_3	PRU0_FD_ZERO_MAX_LIMIT_3					PRU0_FD_ZERO_MIN_3
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_3					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL3		RESERVED	PRU0_SD_CLK_INV3	PRU0_SD_CLK_SEL3	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10212. ICSSG_PRU0_SD_CLK_SEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_3	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_3	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_3	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10212. ICSSG_PRU0_SD_CLK_SEL_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_3	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL3	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV3	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL3	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

22 ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register (Offset = 64h) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 is shown in Figure 14-3380 and described in Table 14-6835.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 3.

Table 14-10213. ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6064h
PRU_ICSSG1_PR1_CFG_SLV	300A 6064h

Figure 14-3380. ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_FD_EN_3	PRU0_FD_ONE_MAX_3	PRU0_FD_ONE_MAX_LIMIT_3					PRU0_FD_ONE_MIN_3
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ONE_MIN_LIMIT_3					PRU0_FD_WINDOW_SIZE_3		
R/W-0h					R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_SD_SAMPLE_SIZE3							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10215. ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_3	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_3	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_3	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10215. ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_3	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_3	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_3	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE3	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) Note: the 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

23 ICSSG_PRU0_SD_CLK_SEL_REG4 Register (Offset = 68h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG4 is shown in Figure 14-3381 and described in Table 14-6837.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 4.

Table 14-10216. ICSSG_PRU0_SD_CLK_SEL_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6068h
PRU_ICSSG1_PR1_CFG_SLV	300A 6068h

Figure 14-3381. ICSSG_PRU0_SD_CLK_SEL_REG4 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_4	PRU0_FD_ZERO_MAX_LIMIT_4					PRU0_FD_ZERO_MIN_4
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_4					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL4		RESERVED	PRU0_SD_CLK_INV4	PRU0_SD_CLK_SEL4	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10218. ICSSG_PRU0_SD_CLK_SEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_4	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_4	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_4	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10218. ICSSG_PRU0_SD_CLK_SEL_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_4	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL4	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV4	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL4	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

24 ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register (Offset = 6Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 is shown in Figure 14-3382 and described in Table 14-6839.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 4.

Table 14-10219. ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 606Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 606Ch

Figure 14-3382. ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PRU0_FD_EN_4</td><td>PRU0_FD_ONE_MAX_4</td><td colspan="5">PRU0_FD_ONE_MAX_LIMIT_4</td><td>PRU0_FD_ONE_MIN_4</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td colspan="5">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU0_FD_ONE_MIN_LIMIT_4</td><td colspan="3">PRU0_FD_WINDOW_SIZE_4</td></tr>
<tr><td colspan="5">R/W-0h</td><td colspan="3">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRU0_SD_SAMPLE_SIZE4</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10221. ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_4	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_4	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_4	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10221. ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_4	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_4	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_4	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE4	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

25 ICSSG_PRU0_SD_CLK_SEL_REG5 Register (Offset = 70h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG5 is shown in Figure 14-3383 and described in Table 14-6841.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 5.

Table 14-10222. ICSSG_PRU0_SD_CLK_SEL_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6070h
PRU_ICSSG1_PR1_CFG_SLV	300A 6070h

Figure 14-3383. ICSSG_PRU0_SD_CLK_SEL_REG5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_5	PRU0_FD_ZERO_MAX_LIMIT_5					PRU0_FD_ZERO_MIN_5
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_5					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL5		RESERVED	PRU0_SD_CLK_INV5	PRU0_SD_CLK_SEL5	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10224. ICSSG_PRU0_SD_CLK_SEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_5	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_5	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_5	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10224. ICSSG_PRU0_SD_CLK_SEL_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_5	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL5	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV5	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL5	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

26 ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register (Offset = 74h) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 is shown in Figure 14-3384 and described in Table 14-6843.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 5.

Table 14-10225.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6074h
PRU_ICSSG1_PR1_CFG_SLV	300A 6074h

Figure 14-3384. ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_5	PRU0_FD_ONE_MAX_5	PRU0_FD_ONE_MAX_LIMIT_5					PRU0_FD_ONE_MIN_5
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_5					PRU0_FD_WINDOW_SIZE_5		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE5							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10227. ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_5	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_5	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_5	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10227. ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_5	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_5	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_5	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE5	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

27 ICSSG_PRU0_SD_CLK_SEL_REG6 Register (Offset = 78h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG6 is shown in Figure 14-3385 and described in Table 14-6845.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 6.

Table 14-10228. ICSSG_PRU0_SD_CLK_SEL_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6078h
PRU_ICSSG1_PR1_CFG_SLV	300A 6078h

Figure 14-3385. ICSSG_PRU0_SD_CLK_SEL_REG6 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_6	PRU0_FD_ZERO_MAX_LIMIT_6					PRU0_FD_ZERO_MIN_6
R/W-X	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_6					RESERVED		
R/W-0h					R/W-X		

7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL6		RESERVED	PRU0_SD_CLK_INV6	PRU0_SD_CLK_SEL6	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10230. ICSSG_PRU0_SD_CLK_SEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_6	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_6	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_6	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10230. ICSSG_PRU0_SD_CLK_SEL_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_6	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL6	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV6	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL6	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

28 ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register (Offset = 7Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 is shown in Figure 14-3386 and described in Table 14-6847.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 6.

Table 14-10231. ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 607Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 607Ch

Figure 14-3386. ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
PRU0_FD_EN_6	PRU0_FD_ONE_MAX_6	PRU0_FD_ONE_MAX_LIMIT_6					PRU0_FD_ONE_MIN_6
R/W-0h	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_6					PRU0_FD_WINDOW_SIZE_6		
R/W-0h					R/W-0h		

7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE6							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10233. ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_6	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_6	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_6	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10233. ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_6	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_6	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_6	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE6	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

29 ICSSG_PRU0_SD_CLK_SEL_REG7 Register (Offset = 80h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG7 is shown in Figure 14-3387 and described in Table 14-6849.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 7.

Table 14-10234. ICSSG_PRU0_SD_CLK_SEL_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6080h
PRU_ICSSG1_PR1_CFG_SLV	300A 6080h

Figure 14-3387. ICSSG_PRU0_SD_CLK_SEL_REG7 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_7	PRU0_FD_ZERO_MAX_LIMIT_7					PRU0_FD_ZERO_MIN_7
R/W-X	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_7					RESERVED		
R/W-0h					R/W-X		

7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL7		RESERVED	PRU0_SD_CLK_INV7	PRU0_SD_CLK_SEL7	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10236. ICSSG_PRU0_SD_CLK_SEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_7	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_7	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_7	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10236. ICSSG_PRU0_SD_CLK_SEL_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_7	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL7	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV7	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL7	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

30 ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register (Offset = 84h) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 is shown in Figure 14-3388 and described in Table 14-6851.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 7.

Table 14-10237. ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6084h
PRU_ICSSG1_PR1_CFG_SLV	300A 6084h

Figure 14-3388. ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_7	PRU0_FD_ONE_MAX_7	PRU0_FD_ONE_MAX_LIMIT_7					PRU0_FD_ONE_MIN_7
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_7					PRU0_FD_WINDOW_SIZE_7		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE7							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10239. ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_7	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_7	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_7	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10239. ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_7	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_7	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_7	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE7	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

31 ICSSG_PRU0_SD_CLK_SEL_REG8 Register (Offset = 88h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG8 is shown in Figure 14-3389 and described in Table 14-6853.

Return to Summary Table.

PRU0 FD, ACC and Clock Selection Register 8.

Table 14-10240. ICSSG_PRU0_SD_CLK_SEL_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6088h
PRU_ICSSG1_PR1_CFG_SLV	300A 6088h

Figure 14-3389. ICSSG_PRU0_SD_CLK_SEL_REG8 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>PRU0_FD_ZERO_MAX_8</td><td colspan="5">PRU0_FD_ZERO_MAX_LIMIT_8</td><td>PRU0_FD_ZERO_MIN_8</td></tr>
<tr><td>R/W-X</td><td>R/W-0h</td><td colspan="5">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU0_FD_ZERO_MIN_LIMIT_8</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">PRU0_SD_ACC_SEL8</td><td>RESERVED</td><td>PRU0_SD_CLK_INV8</td><td colspan="2">PRU0_SD_CLK_SEL8</td></tr>
<tr><td colspan="2">R/W-X</td><td colspan="2">R/W-0h</td><td>R/W-X</td><td>R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10242. ICSSG_PRU0_SD_CLK_SEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_8	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_8	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_8	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10242. ICSSG_PRU0_SD_CLK_SEL_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LIMIT_8	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL8	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV8	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL8	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

32 ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register (Offset = 8Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 is shown in Figure 14-3390 and described in Table 14-6855.

Return to Summary Table.

PRU0 FD and Over Sample Size Register 8.

Table 14-10243. ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 608Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 608Ch

Figure 14-3390. ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PRU0_FD_EN_8</td><td>PRU0_FD_ONE_MAX_8</td><td colspan="5">PRU0_FD_ONE_MAX_LIMIT_8</td><td>PRU0_FD_ONE_MIN_8</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td colspan="5">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU0_FD_ONE_MIN_LIMIT_8</td><td colspan="3">PRU0_FD_WINDOW_SIZE_8</td></tr>
<tr><td colspan="5">R/W-0h</td><td colspan="3">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRU0_SD_SAMPLE_SIZE8</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10245. ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_8	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_8	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_8	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10245. ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU0_FD_ONE_MIN_8	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU0_FD_ONE_MIN_LIMIT_8	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_8	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE8	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

33 ICSSG_PRU1_SD_CFG_REG Register (Offset = 90h) [reset = X]

ICSSG_PRU1_SD_CFG_REG is shown in Figure 14-3391 and described in Table 14-6857.

Return to Summary Table.

SD Register.

Table 14-10246. ICSSG_PRU1_SD_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6090h
PRU_ICSSG1_PR1_CFG_SLV	300A 6090h

Figure 14-3391. ICSSG_PRU1_SD_CFG_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MAN_CLK_PERIOD</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MAN_CLK_CAL_DONE</td></tr>
<tr><td colspan="7">R-X</td><td>R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>MAN_STATUS</td><td colspan="4">SH_SEL</td><td>MAN_DATA_NV_EN</td><td>MAN_SD_EN</td><td>SHARE_EN</td></tr>
<tr><td>R-0h</td><td colspan="4">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read Only-*n* = value after reset

Table 14-10248. ICSSG_PRU1_SD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MAN_CLK_PERIOD	R	0h	Manchester clock period status for SDx
23-17	RESERVED	R	X	
16	MAN_CLK_CAL_DONE	R	0h	Manchester clock calibration status for SDx
15	MAN_STATUS	R	0h	Manchester status for SDx
14-11	SH_SEL	R/W	0h	Manchester SD Ch select for the 3 status fields 0 = SD0 .. 8 = SD8
10	MAN_DATA_NV_EN	R/W	0h	Manchester Decode Mode Data Inversion 0 = rising edge is 1 1 = falling edge is 1
9	MAN_SD_EN	R/W	0h	Manchester Decode Mode 0 = disable 1 = enable If enabled, then you need to enable one clock per data channel
8	SHARE_EN	R/W	0h	Load Share Enable 0 = PRUx owns SD0 -> SD8 1 = RTUx owns SD0 -> SD2, PRUx owns SD3 ->SD5, TX_PRUx owns SD6->SD8
7-0	RESERVED	R	X	

34 ICSSG_PRU1_SD_CLK_SEL_REG0 Register (Offset = 94h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG0 is shown in Figure 14-3392 and described in Table 14-6859.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 0

Table 14-10249. ICSSG_PRU1_SD_CLK_SEL_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6094h
PRU_ICSSG1_PR1_CFG_SLV	300A 6094h

Figure 14-3392. ICSSG_PRU1_SD_CLK_SEL_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_0	PRU1_FD_ZERO_MAX_LIMIT_0					PRU1_FD_ZERO_MIN_0
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_0					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL0		RESERVED	PRU1_SD_CLK_INV0	PRU1_SD_CLK_SEL0	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10251. ICSSG_PRU1_SD_CLK_SEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_0	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_0	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_0	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10251. ICSSG_PRU1_SD_CLK_SEL_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_0	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL0	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV0	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL0	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

35 ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register (Offset = 98h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 is shown in Figure 14-3393 and described in Table 14-6861.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 0.

Table 14-10252. ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6098h
PRU_ICSSG1_PR1_CFG_SLV	300A 6098h

Figure 14-3393. ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_0	PRU1_FD_ONE_MAX_0	PRU1_FD_ONE_MAX_LIMIT_0					PRU1_FD_ONE_MIN_0
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_0					PRU1_FD_WINDOW_SIZE_0		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE0							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10254. ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_0	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_0	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_0	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10254. ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_0	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_0	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_0	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE0	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

36 ICSSG_PRU1_SD_CLK_SEL_REG1 Register (Offset = 9Ch) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG1 is shown in Figure 14-3394 and described in Table 14-6863.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 1.

Table 14-10255. ICSSG_PRU1_SD_CLK_SEL_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 609Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 609Ch

Figure 14-3394. ICSSG_PRU1_SD_CLK_SEL_REG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_1	PRU1_FD_ZERO_MAX_LIMIT_1					PRU1_FD_ZERO_MIN_1
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_1					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL1		RESERVED	PRU1_SD_CLK_INV1	PRU1_SD_CLK_SEL1	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10257. ICSSG_PRU1_SD_CLK_SEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_1	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_1	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1 = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_1	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10257. ICSSG_PRU1_SD_CLK_SEL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_1	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL1	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV1	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL1	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

37 ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register (Offset = A0h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 is shown in Figure 14-3395 and described in Table 14-6865.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 1.

Table 14-10258. ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60A0h
PRU_ICSSG1_PR1_CFG_SLV	300A 60A0h

Figure 14-3395. ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PRU1_FD_EN_1</td><td>PRU1_FD_ONE_MAX_1</td><td colspan="5">PRU1_FD_ONE_MAX_LIMIT_1</td><td>PRU1_FD_ONE_MIN_1</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td colspan="5">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU1_FD_ONE_MIN_LIMIT_1</td><td colspan="3">PRU1_FD_WINDOW_SIZE_1</td></tr>
<tr><td colspan="5">R/W-0h</td><td colspan="3">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRU1_SD_SAMPLE_SIZE1</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10260. ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_1	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_1	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_1	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10260. ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_1	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_1	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_1	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE1	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

38 ICSSG_PRU1_SD_CLK_SEL_REG2 Register (Offset = A4h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG2 is shown in Figure 14-3396 and described in Table 14-6867.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 2.

Table 14-10261. ICSSG_PRU1_SD_CLK_SEL_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60A4h
PRU_ICSSG1_PR1_CFG_SLV	300A 60A4h

Figure 14-3396. ICSSG_PRU1_SD_CLK_SEL_REG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_2	PRU1_FD_ZERO_MAX_LIMIT_2					PRU1_FD_ZERO_MIN_2
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_2					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL2		RESERVED	PRU1_SD_CLK_INV2	PRU1_SD_CLK_SEL2	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10263. ICSSG_PRU1_SD_CLK_SEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_2	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_2	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_2	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10263. ICSSG_PRU1_SD_CLK_SEL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_2	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL2	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV2	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL2	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

39 ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register (Offset = A8h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 is shown in Figure 14-3397 and described in Table 14-6869.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 2.

Table 14-10264. ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60A8h
PRU_ICSSG1_PR1_CFG_SLV	300A 60A8h

Figure 14-3397. ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
PRU1_FD_EN_2	PRU1_FD_ONE_MAX_2	PRU1_FD_ONE_MAX_LIMIT_2					PRU1_FD_ONE_MIN_2
R/W-0h	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_2					PRU1_FD_WINDOW_SIZE_2		
R/W-0h					R/W-0h		

7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE2							
R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10266. ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_2	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_2	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_2	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10266. ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_2	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_2	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_2	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE2	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

40 ICSSG_PRU1_SD_CLK_SEL_REG3 Register (Offset = ACh) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG3 is shown in Figure 14-3398 and described in Table 14-6871.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 3.

Table 14-10267. ICSSG_PRU1_SD_CLK_SEL_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60ACh
PRU_ICSSG1_PR1_CFG_SLV	300A 60ACh

Figure 14-3398. ICSSG_PRU1_SD_CLK_SEL_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_3	PRU1_FD_ZERO_MAX_LIMIT_3					PRU1_FD_ZERO_MIN_3
R/W-X	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_3					RESERVED		
R/W-0h					R/W-X		

7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL3		RESERVED	PRU1_SD_CLK_INV3	PRU1_SD_CLK_SEL3	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10269. ICSSG_PRU1_SD_CLK_SEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_3	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_3	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_3	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10269. ICSSG_PRU1_SD_CLK_SEL_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_3	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL3	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV3	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL3	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

41 ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register (Offset = B0h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 is shown in Figure 14-3399 and described in Table 14-6873.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 3.

Table 14-10270. ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60B0h
PRU_ICSSG1_PR1_CFG_SLV	300A 60B0h

Figure 14-3399. ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_3	PRU1_FD_ONE_MAX_3	PRU1_FD_ONE_MAX_LIMIT_3					PRU1_FD_ONE_MIN_3
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_3					PRU1_FD_WINDOW_SIZE_3		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE3							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10272. ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_3	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_3	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_3	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10272. ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_3	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_3	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_3	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE3	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

42 ICSSG_PRU1_SD_CLK_SEL_REG4 Register (Offset = B4h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG4 is shown in Figure 14-3400 and described in Table 14-6875.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 4.

Table 14-10273. ICSSG_PRU1_SD_CLK_SEL_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60B4h
PRU_ICSSG1_PR1_CFG_SLV	300A 60B4h

Figure 14-3400. ICSSG_PRU1_SD_CLK_SEL_REG4 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_4	PRU1_FD_ZERO_MAX_LIMIT_4					PRU1_FD_ZERO_MIN_4
R/W-X	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_4					RESERVED		
R/W-0h					R/W-X		

7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL4		RESERVED	PRU1_SD_CLK_INV4	PRU1_SD_CLK_SEL4	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10275. ICSSG_PRU1_SD_CLK_SEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_4	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_4	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_4	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10275. ICSSG_PRU1_SD_CLK_SEL_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_4	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL4	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV4	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL4	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

43 ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register (Offset = B8h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 is shown in Figure 14-3401 and described in Table 14-6877.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 4.

Table 14-10276. ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60B8h
PRU_ICSSG1_PR1_CFG_SLV	300A 60B8h

Figure 14-3401. ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_FD_EN_4	PRU1_FD_ONE_MAX_4	PRU1_FD_ONE_MAX_LIMIT_4					PRU1_FD_ONE_MIN_4
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ONE_MIN_LIMIT_4					PRU1_FD_WINDOW_SIZE_4		
R/W-0h					R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_SD_SAMPLE_SIZE4							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10278. ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_4	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_4	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_4	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10278. ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_4	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_4	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_4	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE4	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

44 ICSSG_PRU1_SD_CLK_SEL_REG5 Register (Offset = BCh) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG5 is shown in Figure 14-3402 and described in Table 14-6879.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 5

Table 14-10279. ICSSG_PRU1_SD_CLK_SEL_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60BCh
PRU_ICSSG1_PR1_CFG_SLV	300A 60BCh

Figure 14-3402. ICSSG_PRU1_SD_CLK_SEL_REG5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_5	PRU1_FD_ZERO_MAX_LIMIT_5					PRU1_FD_ZERO_MIN_5
R/W-X	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_5					RESERVED		
R/W-0h					R/W-X		

7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL5		RESERVED	PRU1_SD_CLK_INV5	PRU1_SD_CLK_SEL5	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10281. ICSSG_PRU1_SD_CLK_SEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_5	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_5	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_5	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10281. ICSSG_PRU1_SD_CLK_SEL_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_5	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL5	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV5	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL5	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

45 ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register (Offset = C0h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 is shown in Figure 14-3403 and described in Table 14-6881.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 5

Table 14-10282. ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60C0h
PRU_ICSSG1_PR1_CFG_SLV	300A 60C0h

Figure 14-3403. ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_5	PRU1_FD_ONE_MAX_5	PRU1_FD_ONE_MAX_LIMIT_5					PRU1_FD_ONE_MIN_5
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_5					PRU1_FD_WINDOW_SIZE_5		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE5							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10284. ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_5	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_5	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_5	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10284. ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_5	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_5	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_5	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE5	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

46 ICSSG_PRU1_SD_CLK_SEL_REG6 Register (Offset = C4h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG6 is shown in Figure 14-3404 and described in Table 14-6883.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 6

Table 14-10285. ICSSG_PRU1_SD_CLK_SEL_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60C4h
PRU_ICSSG1_PR1_CFG_SLV	300A 60C4h

Figure 14-3404. ICSSG_PRU1_SD_CLK_SEL_REG6 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_6	PRU1_FD_ZERO_MAX_LIMIT_6					PRU1_FD_ZERO_MIN_6
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_6					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL6		RESERVED	PRU1_SD_CLK_INV6	PRU1_SD_CLK_SEL6	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10287. ICSSG_PRU1_SD_CLK_SEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_6	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_6	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_6	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10287. ICSSG_PRU1_SD_CLK_SEL_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_6	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL6	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV6	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL6	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

47 ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register (Offset = C8h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 is shown in Figure 14-3405 and described in Table 14-6885.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 6

Table 14-10288. ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60C8h
PRU_ICSSG1_PR1_CFG_SLV	300A 60C8h

Figure 14-3405. ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
PRU1_FD_EN_6	PRU1_FD_ONE_MAX_6	PRU1_FD_ONE_MAX_LIMIT_6					PRU1_FD_ONE_MIN_6
R/W-0h	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_6					PRU1_FD_WINDOW_SIZE_6		
R/W-0h					R/W-0h		

7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE6							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10290. ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_6	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_6	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_6	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10290. ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_6	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_6	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_6	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE6	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

48 ICSSG_PRU1_SD_CLK_SEL_REG7 Register (Offset = CCh) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG7 is shown in Figure 14-3406 and described in Table 14-6887.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 7

Table 14-10291. ICSSG_PRU1_SD_CLK_SEL_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60CCh
PRU_ICSSG1_PR1_CFG_SLV	300A 60CCh

Figure 14-3406. ICSSG_PRU1_SD_CLK_SEL_REG7 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>PRU1_FD_ZERO_MAX_7</td><td colspan="5">PRU1_FD_ZERO_MAX_LIMIT_7</td><td>PRU1_FD_ZERO_MIN_7</td></tr>
<tr><td>R/W-X</td><td>R/W-0h</td><td colspan="5">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU1_FD_ZERO_MIN_LIMIT_7</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">PRU1_SD_ACC_SEL7</td><td>RESERVED</td><td>PRU1_SD_CLK_INV7</td><td colspan="2">PRU1_SD_CLK_SEL7</td></tr>
<tr><td colspan="2">R/W-X</td><td colspan="2">R/W-0h</td><td>R/W-X</td><td>R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10293. ICSSG_PRU1_SD_CLK_SEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_7	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_7	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_7	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10293. ICSSG_PRU1_SD_CLK_SEL_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_7	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL7	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV7	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL7	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

49 ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register (Offset = D0h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 is shown in Figure 14-3407 and described in Table 14-6889.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 7

Table 14-10294. ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60D0h
PRU_ICSSG1_PR1_CFG_SLV	300A 60D0h

Figure 14-3407. ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_7	PRU1_FD_ONE_MAX_7	PRU1_FD_ONE_MAX_LIMIT_7					PRU1_FD_ONE_MIN_7
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_7					PRU1_FD_WINDOW_SIZE_7		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE7							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10296. ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_7	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_7	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_7	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10296. ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_7	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_7	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_7	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE7	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

50 ICSSG_PRU1_SD_CLK_SEL_REG8 Register (Offset = D4h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG8 is shown in Figure 14-3408 and described in Table 14-6891.

Return to Summary Table.

PRU1 FD, ACC and Clock Selection Register 8

Table 14-10297. ICSSG_PRU1_SD_CLK_SEL_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60D4h
PRU_ICSSG1_PR1_CFG_SLV	300A 60D4h

Figure 14-3408. ICSSG_PRU1_SD_CLK_SEL_REG8 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_8	PRU1_FD_ZERO_MAX_LIMIT_8					PRU1_FD_ZERO_MIN_8
R/W-X	R/W-0h	R/W-0h					R/W-0h

15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_8					RESERVED		
R/W-0h					R/W-X		

7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL8		RESERVED	PRU1_SD_CLK_INV8	PRU1_SD_CLK_SEL8	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10299. ICSSG_PRU1_SD_CLK_SEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_8	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_8	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_8	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 14-10299. ICSSG_PRU1_SD_CLK_SEL_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LIMIT_8	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL8	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV8	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL8	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

51 ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register (Offset = D8h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 is shown in Figure 14-3409 and described in Table 14-6893.

Return to Summary Table.

PRU1 FD and Over Sample Size Register 8

Table 14-10300. ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60D8h
PRU_ICSSG1_PR1_CFG_SLV	300A 60D8h

Figure 14-3409. ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_FD_EN_8	PRU1_FD_ONE_MAX_8	PRU1_FD_ONE_MAX_LIMIT_8					PRU1_FD_ONE_MIN_8
R/W-0h	R/W-0h	R/W-0h					R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ONE_MIN_LIMIT_8					PRU1_FD_WINDOW_SIZE_8		
R/W-0h					R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_SD_SAMPLE_SIZE8							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10302. ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_8	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_8	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_8	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32

Table 14-10302. ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU1_FD_ONE_MIN_8	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear
15-11	PRU1_FD_ONE_MIN_LIMIT_8	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_8	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE8	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

52 ICSSG_PRU0_ED_RX_CFG_REG Register (Offset = E0h) [reset = X]

ICSSG_PRU0_ED_RX_CFG_REG is shown in Figure 14-3410 and described in Table 14-6895.

Return to Summary Table.

PRU0 ED Receive Global Configuration Register

Table 14-10303. ICSSG_PRU0_ED_RX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60E0h
PRU_ICSSG1_PR1_CFG_SLV	300A 60E0h

Figure 14-3410. ICSSG_PRU0_ED_RX_CFG_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_RX_DIV_FACTOR							
R/W-0h							

23	22	21	20	19	18	17	16
PRU0_ED_RX_DIV_FACTOR							
R/W-0h							

15	14	13	12	11	10	9	8
PRU0_ED_RX_DIV_FACTOR_FRAC	RESERVED						
R/W-0h	R/W-X						

7	6	5	4	3	2	1	0
RESERVED			PRU0_ED_RX_CLK_SEL	PRU0_ED_RX_SB_POL	PRU0_ED_RX_SAMPLE_SIZE		
R/W-X			R/W-0h	R/W-1h	R/W-7h		

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10305. ICSSG_PRU0_ED_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_RX_DIV_FACTOR	R/W	0h	Div factor for divh16 0h = div 1 1h = div 2 Nh = div (N+1) This divh16 is post divfrac, the effective rate will be Effective rate is 1.5 X main div if frac enabled Effective rate is 1.0 X main div if frac disabled For example , divh16 set to 3h Div by 6 if frac enabled Div by 4 if frac enabled For example , divh16 set to 4 Div by 7.5 if frac enabled Div by 5 if frac enabled
15	PRU0_ED_RX_DIV_FACTOR_FRAC	R/W	0h	Enable Fractional division before the divh16 0h = div 1 1h = div 1.5
14-5	RESERVED	R/W	X	

Table 14-10305. ICSSG_PRU0_ED_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PRU0_ED_RX_CLK_SEL	R/W	0h	Selects the clock source for the divh16fr 0 =192 MHz, the uart_clk 1h = 200 MHz, the ICSSGn_CORE_CLK
3	PRU0_ED_RX_SB_POL	R/W	1h	Defines the polarity of the RX Start Bit 0h = 0 1h = 1 Reset/default state
2-0	PRU0_ED_RX_SAMPLE_SIZE	R/W	7h	Over Sample size This defines the number of samples before the shadow copy gets updated and the VAL flag gets set The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 6 = Over Sample of 7 7 = Over Sample of 8 Note: the Over Sample Clock rate divided by the 1x Clock rate must equal the Over Sample size.

53 ICSSG_PRU0_ED_TX_CFG_REG Register (Offset = E4h) [reset = X]

ICSSG_PRU0_ED_TX_CFG_REG is shown in Figure 14-3411 and described in Table 14-6897.

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PRU0 ED Transmit Global Configuration Register

Table 14-10306. ICSSG_PRU0_ED_TX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60E4h
PRU_ICSSG1_PR1_CFG_SLV	300A 60E4h

Figure 14-3411. ICSSG_PRU0_ED_TX_CFG_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_DIV_FACTOR							
R/W-0h							
23	22	21	20	19	18	17	16
PRU0_ED_TX_DIV_FACTOR							
R/W-0h							
15	14	13	12	11	10	9	8
PRU0_ED_TX_DIV_FACTOR_FRAC	RESERVED			SHARE_EN	PRU0_ENDAT2_CLK_SYNC	PRU0_ENDAT1_CLK_SYNC	PRU0_ENDAT0_CLK_SYNC
R/W-0h	R/W-X			R/W-0h	R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
PRU0_ED_BUSY_2	PRU0_ED_BUSY_1	PRU0_ED_BUSY_0	PRU0_ED_TX_CLK_SEL	RESERVED			
R-0h	R-0h	R-0h	R/W-0h	R/W-X			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10308. ICSSG_PRU0_ED_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_TX_DIV_FACTOR	R/W	0h	Div factor for divh16 0h = div 1 1h = div 2 Nh = div (N+1) This divh16 is post divfrac, the effective rate will be Effective rate is 1.5 X main div if frac enabled Effective rate is 1.0 X main div if frac disabled For example , divh16 set to 3h Div by 6 if frac enabled Div by 4 if frac enabled For example , divh16 set to 4 Div by 7.5 if frac enabled Div by 5 if frac enabled
15	PRU0_ED_TX_DIV_FACTOR_FRAC	R/W	0h	Enable Fractional division before the divh16 0h = div 1 1h = div 1.5
14-11	RESERVED	R/W	X	

Table 14-10308. ICSSG_PRU0_ED_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	RESERVED	R/W	X	
11	SHARE_EN	R/W	0h	Load Share Enable 0 PRU owns ED0/ED1/ED2 1 RTU owns ED0, PRU owns ED1, and TS_PRU owns ED2
10	PRU0_ENDAT2_CLK_SYNC	R	1h	Observation of pru<n>_endat2_clk pin state
9	PRU0_ENDAT1_CLK_SYNC	R	1h	Observation of pru<n>_endat1_clk pin state
8	PRU0_ENDAT0_CLK_SYNC	R	1h	Observation of pru<n>_endat0_clk pin state
7	PRU0_ED_BUSY_2	R	0h	Determines when you can assert tx go for channel 2 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
6	PRU0_ED_BUSY_1	R	0h	Determines when you can assert tx go for channel 1 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
5	PRU0_ED_BUSY_0	R	0h	Determines when you can assert tx go for channel 0 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
4	PRU0_ED_TX_CLK_SEL	R/W	0h	Selects the clock source for the divh16fr 0h = 192 MHz, the uart_clk 1h = 200 MHz, the ICSSGn_CORE_CLK
3-0	RESERVED	R/W	X	

54 ICSSG_PRU0_ED_CH0_CFG0_REG Register (Offset = E8h) [reset = 0h]

ICSSG_PRU0_ED_CH0_CFG0_REG is shown in Figure 14-3412 and described in Table 14-6899.

Return to Summary Table.

PRU0 ED Channel 0 Configuration 0 Register

Table 14-10309. ICSSG_PRU0_ED_CH0_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60E8h
PRU_ICSSG1_PR1_CFG_SLV	300A 60E8h

Figure 14-3412. ICSSG_PRU0_ED_CH0_CFG0_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PRU0_ED_TX_FIFO_SWAP_BITS0</td><td>PRU0_ED_SW_CLK_OUT0</td><td>PRU0_ED_CLK_OUT_OVR_EN0</td><td>PRU0_ED_RX_SNOOP0</td><td colspan="4">PRU0_ED_RX_FRAME_SIZE0</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R-0h</td><td colspan="4">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRU0_ED_RX_FRAME_SIZE0</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU0_ED_TX_FRAME_SIZE0</td><td colspan="3">PRU0_ED_TX_WDLY0</td></tr>
<tr><td colspan="5">R/W-0h</td><td colspan="3">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRU0_ED_TX_WDLY0</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10311. ICSSG_PRU0_ED_CH0_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS0	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU0_ED_SW_CLK_OUT0	R/W	0h	This controls the state of pru<n>_ endat<m>_clk when endat_clk_out_override_en is set
29	PRU0_ED_CLK_OUT_OVR_EN0	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_ endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU0_ED_RX_SNOOP0	R	0h	Direct Read of pru<n>_ endat<m>_in state

Table 14-10311. ICSSG_PRU0_ED_CH0_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU0_ED_RX_FRAME_SIZE0	R/W	0h	RX frame size, after SB is detected 0h = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1h = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU0_ED_TX_FRAME_SIZE0	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8 = TX FIFO will transmit 8 bits then stop 9 = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU0_ED_TX_WDLY0	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

55 ICSSG_PRU0_ED_CH0_CFG1_REG Register (Offset = ECh) [reset = 0h]

ICSSG_PRU0_ED_CH0_CFG1_REG is shown in Figure 14-3413 and described in Table 14-6901.

Return to Summary Table.

PRU0 ED Channel 0 Configuration 1 Register

Table 14-10312. ICSSG_PRU0_ED_CH0_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60ECh
PRU_ICSSG1_PR1_CFG_SLV	300A 60ECh

Figure 14-3413. ICSSG_PRU0_ED_CH0_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU0_ED_RX_EN_COUNTER0															
R/W-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_ED_TST_DELAY_COUNTER0															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10314. ICSSG_PRU0_ED_CH0_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_RX_EN_COUNTER0	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5 s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must be use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU0_ED_TST_DELAY_COUNTER0	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

56 ICSSG_PRU0_ED_CH1_CFG0_REG Register (Offset = F0h) [reset = 0h]

ICSSG_PRU0_ED_CH1_CFG0_REG is shown in Figure 14-3414 and described in Table 14-6903.

Return to Summary Table.

PRU0 ED Channel 1 Configuration 0 Register

Table 14-10315. ICSSG_PRU0_ED_CH1_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60F0h
PRU_ICSSG1_PR1_CFG_SLV	300A 60F0h

Figure 14-3414. ICSSG_PRU0_ED_CH1_CFG0_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PRU0_ED_TX_FIFO_SWAP_BITS1</td><td>PRU0_ED_SW_CLK_OUT1</td><td>PRU0_ED_CLK_OUT_OVR_EN1</td><td>PRU0_ED_RX_SNOOP1</td><td colspan="4">PRU0_ED_RX_FRAME_SIZE1</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R-0h</td><td colspan="4">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRU0_ED_RX_FRAME_SIZE1</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU0_ED_TX_FRAME_SIZE1</td><td colspan="3">PRU0_ED_TX_WDLY1</td></tr>
<tr><td colspan="5">R/W-0h</td><td colspan="3">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRU0_ED_TX_WDLY1</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10317. ICSSG_PRU0_ED_CH1_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS1	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU0_ED_SW_CLK_OUT1	R/W	0h	This controls the state of pru<n>_ endat<m>_clk when endat_clk_out_override_en is set
29	PRU0_ED_CLK_OUT_OVR_EN1	R/W	0h	When set, this gives the software the abilty to have direct control of pru<n>_ endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU0_ED_RX_SNOOP1	R	0h	Direct Read of pru<n>_ endat<m>_in state

Table 14-10317. ICSSG_PRU0_ED_CH1_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU0_ED_RX_FRAME_SIZE1	R/W	0h	RX frame size, after SB is detected 0 = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1 = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU0_ED_TX_FRAME_SIZE1	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8h = TX FIFO will transmit 8 bits then stop 9h = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU0_ED_TX_WDLY1	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

57 ICSSG_PRU0_ED_CH1_CFG1_REG Register (Offset = F4h) [reset = 0h]

ICSSG_PRU0_ED_CH1_CFG1_REG is shown in Figure 14-3415 and described in Table 14-6905.

Return to Summary Table.

PRU0 ED Channel 1 Configuration 1 Register

Table 14-10318. ICSSG_PRU0_ED_CH1_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60F4h
PRU_ICSSG1_PR1_CFG_SLV	300A 60F4h

Figure 14-3415. ICSSG_PRU0_ED_CH1_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU0_ED_RX_EN_COUNTER1															
R/W-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU0_ED_TST_DELAY_COUNTER1															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10320. ICSSG_PRU0_ED_CH1_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_RX_EN_COUNTER1	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5 s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must be use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU0_ED_TST_DELAY_COUNTER1	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

58 ICSSG_PRU0_ED_CH2_CFG0_REG Register (Offset = F8h) [reset = 0h]

ICSSG_PRU0_ED_CH2_CFG0_REG is shown in Figure 14-3416 and described in Table 14-6907.

Return to Summary Table.

PRU0 ED Channel 2 Configuration 0 Register

Table 14-10321. ICSSG_PRU0_ED_CH2_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60F8h
PRU_ICSSG1_PR1_CFG_SLV	300A 60F8h

Figure 14-3416. ICSSG_PRU0_ED_CH2_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_FIFO_SWAP_BITS2	PRU0_ED_SW_CLK_OUT2	PRU0_ED_CLK_OUT_OVR_EN2	PRU0_ED_RX_SNOOP2	PRU0_ED_RX_FRAME_SIZE2			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			

23	22	21	20	19	18	17	16
PRU0_ED_RX_FRAME_SIZE2							
R/W-0h							

15	14	13	12	11	10	9	8
PRU0_ED_TX_FRAME_SIZE2					PRU0_ED_TX_WDLY2		
R/W-0h					R/W-0h		

7	6	5	4	3	2	1	0
PRU0_ED_TX_WDLY2							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10323. ICSSG_PRU0_ED_CH2_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS2	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU0_ED_SW_CLK_OUT2	R/W	0h	This controls the state of pru<n>_ endat<m>_clk when endat_clk_out_override_en is set
29	PRU0_ED_CLK_OUT_OVR_EN2	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_ endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU0_ED_RX_SNOOP2	R	0h	Direct Read of pru<n>_ endat<m>_in state

Table 14-10323. ICSSG_PRU0_ED_CH2_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU0_ED_RX_FRAME_SIZE2	R/W	0h	RX frame size, after SB is detected 0 = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1 = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU0_ED_TX_FRAME_SIZE2	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8h = TX FIFO will transmit 8 bits then stop 9h = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU0_ED_TX_WDLY2	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

59 ICSSG_PRU0_ED_CH2_CFG1_REG Register (Offset = FCh) [reset = 0h]

ICSSG_PRU0_ED_CH2_CFG1_REG is shown in Figure 14-3417 and described in Table 14-6909.

Return to Summary Table.

PRU0 ED Channel 2 Configuration 1 Register

Table 14-10324. ICSSG_PRU0_ED_CH2_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 60FCh
PRU_ICSSG1_PR1_CFG_SLV	300A 60FCh

Figure 14-3417. ICSSG_PRU0_ED_CH2_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU0_ED_RX_EN_COUNTER2															
R/W-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU0_ED_TST_DELAY_COUNTER2															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10326. ICSSG_PRU0_ED_CH2_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_RX_EN_COUNTER2	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must be use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU0_ED_TST_DELAY_COUNTER2	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

60 ICSSG_PRU1_ED_RX_CFG_REG Register (Offset = 100h) [reset = X]

ICSSG_PRU1_ED_RX_CFG_REG is shown in Figure 14-3418 and described in Table 14-6911.

Return to Summary Table.

PRU1 ED Receive Global Configuration Register.

Table 14-10327. ICSSG_PRU1_ED_RX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6100h
PRU_ICSSG1_PR1_CFG_SLV	300A 6100h

Figure 14-3418. ICSSG_PRU1_ED_RX_CFG_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PRU1_ED_RX_DIV_FACTOR</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRU1_ED_RX_DIV_FACTOR</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>PRU1_ED_RX_DIV_FACTOR_FRAC</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W-0h</td><td colspan="7">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>PRU1_ED_RX_CLK_SEL</td><td>PRU1_ED_RX_SB_POL</td><td colspan="3">PRU1_ED_RX_SAMPLE_SIZE</td></tr>
<tr><td colspan="3">R/W-X</td><td>R/W-0h</td><td>R/W-1h</td><td colspan="3">R/W-7h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10329. ICSSG_PRU1_ED_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_RX_DIV_FACTOR	R/W	0h	div factor for divh16 0h = div 1 1h = div 2 Nh = div (N+1) This divh16 is post divfrac, the effective rate will be Effective rate is 1.5 X main div if frac enabled Effective rate is 1.0 X main div if frac disabled For example , divh16 set to 3h Div by 6 if frac enabled Div by 4 if frac enabled For example , divh16 set to 4 Div by 7.5 if frac enabled Div by 5 if frac enabled
15	PRU1_ED_RX_DIV_FACTOR_FRAC	R/W	0h	Enable Fractional division before the divh16 0h = div 1 1h = div 1.5
14-5	RESERVED	R/W	X	

Table 14-10329. ICSSG_PRU1_ED_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PRU1_ED_RX_CLK_SEL	R/W	0h	Selects the clock source for the divh16fr 0h = 192 MHz, the uart_clk 1h = 200 MHz, the ICSSGn_CORE_CLK
3	PRU1_ED_RX_SB_POL	R/W	1h	Defines the polarity of the RX Start Bit 0h = 0 1h = 1 Reset/default state
2-0	PRU1_ED_RX_SAMPLE_SIZE	R/W	7h	Over Sample size This defines the number of samples before the shadow copy gets updated and the VAL flag gets set The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 6h = Over Sample of 7 7h = Over Sample of 8 Note: the Over Sample Clock rate divided by the 1x Clock rate must equal the Over Sample size.

61 ICSSG_PRU1_ED_TX_CFG_REG Register (Offset = 104h) [reset = X]

ICSSG_PRU1_ED_TX_CFG_REG is shown in Figure 14-3419 and described in Table 14-6913.

Return to Summary Table.

PRU1 ED Transmit Global Configuration Register.

Table 14-10330. ICSSG_PRU1_ED_TX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6104h
PRU_ICSSG1_PR1_CFG_SLV	300A 6104h

Figure 14-3419. ICSSG_PRU1_ED_TX_CFG_REG Register

31	30	29	28	27	26	25	24
PRU01_ED_TX_DIV_FACTOR							
R/W-0h							
23	22	21	20	19	18	17	16
PRU01_ED_TX_DIV_FACTOR							
R/W-0h							
15	14	13	12	11	10	9	8
PRU1_ED_TX_DIV_FACTOR_FRAC	RESERVED			SHARE_EN	PRU1_ENDAT2_CLK_SYNC	PRU1_ENDAT1_CLK_SYNC	PRU1_ENDAT0_CLK_SYNC
R/W-0h	R/W-X			R/W-0h	R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
PRU1_ED_BUSY_2	PRU1_ED_BUSY_1	PRU1_ED_BUSY_0	PRU1_ED_TX_CLK_SEL	RESERVED			
R-0h	R-0h	R-0h	R/W-0h	R/W-X			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10332. ICSSG_PRU1_ED_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_TX_DIV_FACTOR	R/W	0h	Div factor for divh16 0h = div 1 1h = div 2 Nh = div (N+1) This divh16 is post divfrac, the effective rate will be Effective rate is 1.5 X main div if frac enabled Effective rate is 1.0 X main div if frac disabled For example , divh16 set to 3h Div by 6 if frac enabled Div by 4 if frac enabled For example , divh16 set to 4 Div by 7.5 if frac enabled Div by 5 if frac enabled
15	PRU1_ED_TX_DIV_FACTOR_FRAC	R/W	0h	Enable Fractional division before the divh16 0h = div 1 1h = div 1.5
14-11	RESERVED	R/W	X	

Table 14-10332. ICSSG_PRU1_ED_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	RESERVED	R/W	X	
11	SHARE_EN	R/W	0h	Load Share Enable 0 PRU owns ED0/ED1/ED2 1 RTU owns ED0, PRU owns ED1, and TS_PRU owns ED2
10	PRU1_ENDAT2_CLK_SYNC	R	1h	Observation of pru<n>_endat2_clk pin state
9	PRU1_ENDAT1_CLK_SYNC	R	1h	Observation of pru<n>_endat1_clk pin state
8	PRU1_ENDAT0_CLK_SYNC	R	1h	Observation of pru<n>_endat0_clk pin state
7	PRU1_ED_BUSY_2	R	0h	Determines when you can assert tx go for channel 2 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
6	PRU1_ED_BUSY_1	R	0h	Determines when you can assert tx go for channel 1 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
5	PRU1_ED_BUSY_0	R	0h	Determines when you can assert tx go for channel 0 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
4	PRU1_ED_TX_CLK_SEL	R/W	0h	Selects the clock source for the divh16fr 0h = 192 MHz, the uart_clk 1h = 200 MHz, the ICSSGn_CORE_CLK
3-0	RESERVED	R/W	X	

62 ICSSG_PRU1_ED_CH0_CFG0_REG Register (Offset = 108h) [reset = 0h]

ICSSG_PRU1_ED_CH0_CFG0_REG is shown in Figure 14-3420 and described in Table 14-6915.

Return to Summary Table.

PRU1 ED Channel 0 Configuration 0 Register.

Table 14-10333. ICSSG_PRU1_ED_CH0_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6108h
PRU_ICSSG1_PR1_CFG_SLV	300A 6108h

Figure 14-3420. ICSSG_PRU1_ED_CH0_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS0	PRU1_ED_SW_CLK_OUT0	PRU1_ED_CLK_OUT_OVR_EN0	PRU1_ED_RX_SNOOP0	PRU1_ED_RX_FRAME_SIZE0			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	22	21	20	19	18	17	16
PRU1_ED_RX_FRAME_SIZE0							
R/W-0h							
15	14	13	12	11	10	9	8
PRU1_ED_TX_FRAME_SIZE0					PRU1_ED_TX_WDLY0		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_ED_TX_WDLY0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10335. ICSSG_PRU1_ED_CH0_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS0	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU1_ED_SW_CLK_OUT0	R/W	0h	This controls the state of pru<n>_ endat<m>_clk when endat_clk_out_override_en is set
29	PRU1_ED_CLK_OUT_OVR_EN0	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_ endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU1_ED_RX_SNOOP0	R	0h	Direct Read of pru<n>_ endat<m>_in state

Table 14-10335. ICSSG_PRU1_ED_CH0_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU1_ED_RX_FRAME_SIZE0	R/W	0h	RX frame size, after SB is detected 0h = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1h = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 4095 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU1_ED_TX_FRAME_SIZE0	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8 = TX FIFO will transmit 8 bits then stop 9 = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU1_ED_TX_WDLY0	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

63 ICSSG_PRU1_ED_CH0_CFG1_REG Register (Offset = 10Ch) [reset = 0h]

ICSSG_PRU1_ED_CH0_CFG1_REG is shown in Figure 14-3421 and described in Table 14-6917.

Return to Summary Table.

PRU1 ED Channel 0 Configuration 1 Register.

Table 14-10336. ICSSG_PRU1_ED_CH0_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 610Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 610Ch

Figure 14-3421. ICSSG_PRU1_ED_CH0_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU1_ED_RX_EN_COUNTER0															
R/W-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_ED_TST_DELAY_COUNTER0															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10338. ICSSG_PRU1_ED_CH0_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_RX_EN_COUNTER0	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0h if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5 s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU1_ED_TST_DELAY_COUNTER0	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

64 ICSSG_PRU1_ED_CH1_CFG0_REG Register (Offset = 110h) [reset = 0h]

ICSSG_PRU1_ED_CH1_CFG0_REG is shown in Figure 14-3422 and described in Table 14-6919.

Return to Summary Table.

PRU1 ED Channel 1 Configuration 0 Register.

Table 14-10339. ICSSG_PRU1_ED_CH1_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6110h
PRU_ICSSG1_PR1_CFG_SLV	300A 6110h

Figure 14-3422. ICSSG_PRU1_ED_CH1_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS1	PRU1_ED_SW_CLK_OUT1	PRU1_ED_CLK_OUT_OVR_EN1	PRU1_ED_RX_SNOOP1	PRU1_ED_RX_FRAME_SIZE1			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	22	21	20	19	18	17	16
PRU1_ED_RX_FRAME_SIZE1							
R/W-0h							
15	14	13	12	11	10	9	8
PRU1_ED_TX_FRAME_SIZE1					PRU1_ED_TX_WDLY1		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_ED_TX_WDLY1							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10341. ICSSG_PRU1_ED_CH1_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS1	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU1_ED_SW_CLK_OUT1	R/W	0h	This controls the state of pru<n>_ endat<m>_clk when endat_clk_out_override_en is set
29	PRU1_ED_CLK_OUT_OVR_EN1	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_ endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU1_ED_RX_SNOOP1	R	0h	Direct Read of pru<n>_ endat<m>_in state

Table 14-10341. ICSSG_PRU1_ED_CH1_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU1_ED_RX_FRAME_SIZE1	R/W	0h	RX frame size, after SB is detected 0h = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1 = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU1_ED_TX_FRAME_SIZE1	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8h = TX FIFO will transmit 8 bits then stop 9h = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU1_ED_TX_WDLY1	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

65 ICSSG_PRU1_ED_CH1_CFG1_REG Register (Offset = 114h) [reset = 0h]

ICSSG_PRU1_ED_CH1_CFG1_REG is shown in Figure 14-3423 and described in Table 14-6921.

Return to Summary Table.

PRU1 ED Channel 1 Configuration 1 Register.

Table 14-10342. ICSSG_PRU1_ED_CH1_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6114h
PRU_ICSSG1_PR1_CFG_SLV	300A 6114h

Figure 14-3423. ICSSG_PRU1_ED_CH1_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU1_ED_RX_EN_COUNTER1															
R/W-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU1_ED_TST_DELAY_COUNTER1															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10344. ICSSG_PRU1_ED_CH1_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_RX_EN_COUNTER1	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU1_ED_TST_DELAY_COUNTER1	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

66 ICSSG_PRU1_ED_CH2_CFG0_REG Register (Offset = 118h) [reset = 0h]

ICSSG_PRU1_ED_CH2_CFG0_REG is shown in Figure 14-3424 and described in Table 14-6923.

Return to Summary Table.

PRU1 ED Channel 2 Configuration 0 Register.

Table 14-10345. ICSSG_PRU1_ED_CH2_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6118h
PRU_ICSSG1_PR1_CFG_SLV	300A 6118h

Figure 14-3424. ICSSG_PRU1_ED_CH2_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS2	PRU1_ED_SW_CLK_OUT2	PRU1_ED_CLK_OUT_OVR_EN2	PRU1_ED_RX_SNOOP2	PRU1_ED_RX_FRAME_SIZE2			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_ED_RX_FRAME_SIZE2							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_ED_TX_FRAME_SIZE2					PRU1_ED_TX_WDLY2		
R/W-0h					R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_ED_TX_WDLY2							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10347. ICSSG_PRU1_ED_CH2_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS2	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU1_ED_SW_CLK_OUT2	R/W	0h	This controls the state of pru<n>_ endat<m>_clk when endat_clk_out_override_en is set
29	PRU1_ED_CLK_OUT_OVR_EN2	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_ endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU1_ED_RX_SNOOP2	R	0h	Direct Read of pru<n>_ endat<m>_in state

Table 14-10347. ICSSG_PRU1_ED_CH2_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU1_ED_RX_FRAME_SIZE2	R/W	0h	RX frame size, after SB is detected 0h = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1 = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU1_ED_TX_FRAME_SIZE2	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8h = TX FIFO will transmit 8 bits then stop 9h = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU1_ED_TX_WDLY2	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

67 ICSSG_PRU1_ED_CH2_CFG1_REG Register (Offset = 11Ch) [reset = 0h]

ICSSG_PRU1_ED_CH2_CFG1_REG is shown in Figure 14-3425 and described in Table 14-6925.

Return to Summary Table.

PRU1 ED Channel 2 Configuration 1 Register.

Table 14-10348. ICSSG_PRU1_ED_CH2_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 611Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 611Ch

Figure 14-3425. ICSSG_PRU1_ED_CH2_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU1_ED_RX_EN_COUNTER2															
R/W-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_ED_TST_DELAY_COUNTER2															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10350. ICSSG_PRU1_ED_CH2_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_RX_EN_COUNTER2	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is no required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5 s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU1_ED_TST_DELAY_COUNTER2	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

68 ICSSG_RTU0_POKE_EN0_REG Register (Offset = 124h) [reset = 0h]

ICSSG_RTU0_POKE_EN0_REG is shown in Figure 14-3426 and described in Table 14-6927.

Return to Summary Table.

RTU0 Poke Enable 0 Register.

Table 14-10351. ICSSG_RTU0_POKE_EN0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6124h
PRU_ICSSG1_PR1_CFG_SLV	300A 6124h

Figure 14-3426. ICSSG_RTU0_POKE_EN0_REG Register

31	30	29	28	27	26	25	24
RTU0_POKE_R27_EN				RTU0_POKE_R26_EN			
R/W-0h				R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RTU0_POKE_R25_EN				RTU0_POKE_R24_EN			
R/W-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTU0_POKE_R23_EN				RTU0_POKE_R22_EN			
R/W-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RTU0_POKE_R21_EN				RTU0_POKE_R20_EN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10353. ICSSG_RTU0_POKE_EN0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RTU0_POKE_R27_EN	R/W	0h	This enables the external values to get poked into PRU’s internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
27-24	RTU0_POKE_R26_EN	R/W	0h	This enables the external values to get poked into PRU’s internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
23-20	RTU0_POKE_R25_EN	R/W	0h	This enables the external values to get poked into PRU’s internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
19-16	RTU0_POKE_R24_EN	R/W	0h	This enables the external values to get poked into PRU’s internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte

Table 14-10353. ICSSG_RTU0_POKE_EN0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RTU0_POKE_R23_EN	R/W	0h	This enables the external values to get poked into PRU’s internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
11-8	RTU0_POKE_R22_EN	R/W	0h	This enables the external values to get poked into PRU’s internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
7-4	RTU0_POKE_R21_EN	R/W	0h	This enables the external values to get poked into PRU’s internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
3-0	RTU0_POKE_R20_EN	R/W	0h	This enables the external values to get poked into PRU’s internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte

69 ICSSG_RTU1_POKE_EN0_REG Register (Offset = 12Ch) [reset = 0h]

ICSSG_RTU1_POKE_EN0_REG is shown in Figure 14-3427 and described in Table 14-6929.

Return to Summary Table.

RTU1 Poke Enable 0 Register.

Table 14-10354. ICSSG_RTU1_POKE_EN0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 612Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 612Ch

Figure 14-3427. ICSSG_RTU1_POKE_EN0_REG Register

31	30	29	28	27	26	25	24
RTU1_POKE_R27_EN				RTU1_POKE_R26_EN			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
RTU1_POKE_R25_EN				RTU1_POKE_R24_EN			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RTU1_POKE_R23_EN				RTU1_POKE_R22_EN			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RTU1_POKE_R21_EN				RTU1_POKE_R20_EN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10356. ICSSG_RTU1_POKE_EN0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RTU1_POKE_R27_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
27-24	RTU1_POKE_R26_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
23-20	RTU1_POKE_R25_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
19-16	RTU1_POKE_R24_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte

Table 14-10356. ICSSG_RTU1_POKE_EN0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RTU1_POKE_R23_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
11-8	RTU1_POKE_R22_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
7-4	RTU1_POKE_R21_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
3-0	RTU1_POKE_R20_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte

70 ICSSG_PWM0 Register (Offset = 130h) [reset = X]

ICSSG_PWM0 is shown in Figure 14-3428 and described in Table 14-6931.

Return to Summary Table.

PWM0 Trip Configuration Register.

Table 14-10357. ICSSG_PWM0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6130h
PRU_ICSSG1_PR1_CFG_SLV	300A 6130h

Figure 14-3428. ICSSG_PWM0 Register

31	30	29	28	27	26	25	24
RESERVED	PWM0_TRIP_S	PWM0_TRIP_VEC					
R/W-X	R/W-0h	R-0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWM0_TRIP_VEC			PWM0_POS_ERR_TRIP	PWM0_OVER_ERR_TRIP	PWM0_TRIP_RESET	PWM0_TRIP_CMP0_EN	PWM0_TRIP_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWM0_TRIP_MASK							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM0_DEBOUNCE_VALUE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10359. ICSSG_PWM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	PWM0_TRIP_S	R/W	0h	Trip status. Cleared by trip reset.
29-21	PWM0_TRIP_VEC	R	0h	Trip trigger cause vector. Cleared by trip reset. 0h: PWM0_POS_ERR_TRIP (trip_e5) 1h: PWM0_OVER_ERR_TRIP (trip_e4) 2h: PWM0_0_SD_SHORT_ERR_TRIP (trip_e3_0) 3h: PWM0_1_SD_SHORT_ERR_TRIP (trip_e3_1) 4h: PWM0_2_SD_SHORT_ERR_TRIP (trip_e3_2) 5h: PWM0_DEBOUNCE_TRIP_IN (trip_e2) 6h: PWM0_0_DEBOUNCE_TRIP (trip_e1_0) 7h: PWM0_1_DEBOUNCE_TRIP (trip_e1_1) 8h: PWM0_2_DEBOUNCE_TRIP (trip_e1_2)
20	PWM0_POS_ERR_TRIP	R/W	0h	Software position feedback error trip
19	PWM0_OVER_ERR_TRIP	R/W	0h	Software overcurrent error trip
18	PWM0_TRIP_RESET	R/W	0h	Software trip reset

Table 14-10359. ICSSG_PWM0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	PWM0_TRIP_CMP0_EN	R/W	0h	CMP0 reset trip clear enable
16-8	PWM0_TRIP_MASK	R/W	0h	Software mask for trip, one hot
7-0	PWM0_DEBOUNCE_VALUE	R/W	0h	Debounce counter , defines the number of core_clk required for the pulse not to get rejected

71 ICSSG_PWM1 Register (Offset = 134h) [reset = X]

ICSSG_PWM1 is shown in Figure 14-3429 and described in Table 14-6933.

Return to Summary Table.

PWM1 Trip Configuration Register.

Table 14-10360. ICSSG_PWM1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6134h
PRU_ICSSG1_PR1_CFG_SLV	300A 6134h

Figure 14-3429. ICSSG_PWM1 Register

31	30	29	28	27	26	25	24
RESERVED	PWM1_TRIP_S	PWM1_TRIP_VEC					
R/W-X	R/W-0h	R-0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWM1_TRIP_VEC			PWM1_POS_ERR_TRIP	PWM1_OVER_ERR_TRIP	PWM1_TRIP_RESET	PWM1_TRIP_CMP0_EN	PWM1_TRIP_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWM1_TRIP_MASK							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM1_DEBOUNCE_VALUE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10362. ICSSG_PWM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	PWM1_TRIP_S	R/W	0h	Trip status. Cleared by trip reset.
29-21	PWM1_TRIP_VEC	R	0h	Trip trigger cause vector. Cleared by trip reset. 0h: PWM1_POS_ERR_TRIP (trip_e5) 1h: PWM1_OVER_ERR_TRIP (trip_e4) 2h: PWM1_0_SD_SHORT_ERR_TRIP (trip_e3_0) 3h: PWM1_1_SD_SHORT_ERR_TRIP (trip_e3_1) 4h: PWM1_2_SD_SHORT_ERR_TRIP (trip_e3_2) 5h: PWM1_DEBOUNCE_TRIP_IN (trip_e2) 6h: PWM1_0_DEBOUNCE_TRIP (trip_e1_0) 7h: PWM1_1_DEBOUNCE_TRIP (trip_e1_1) 8h: PWM1_2_DEBOUNCE_TRIP (trip_e1_2)
20	PWM1_POS_ERR_TRIP	R/W	0h	Software position feedback error trip
19	PWM1_OVER_ERR_TRIP	R/W	0h	Software overcurrent error trip
18	PWM1_TRIP_RESET	R/W	0h	Software trip reset

Table 14-10362. ICSSG_PWM1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	PWM1_TRIP_CMP0_EN	R/W	0h	CMP0 reset trip clear enable
16-8	PWM1_TRIP_MASK	R/W	0h	Software mask for trip, one hot
7-0	PWM1_DEBOUNCE_VALUE	R/W	0h	Debounce counter, defines the number of core_clk required for the pulse not to get rejected

72 ICSSG_PWM2 Register (Offset = 138h) [reset = X]

ICSSG_PWM2 is shown in Figure 14-3430 and described in Table 14-6935.

Return to Summary Table.

PWM2 Trip Configuration Register.

Table 14-10363. ICSSG_PWM2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6138h
PRU_ICSSG1_PR1_CFG_SLV	300A 6138h

Figure 14-3430. ICSSG_PWM2 Register

31	30	29	28	27	26	25	24
RESERVED	PWM2_TRIP_S	PWM2_TRIP_VEC					
R/W-X	R/W-0h	R-0h					

23	22	21	20	19	18	17	16
PWM2_TRIP_VEC			PWM2_POS_ERR_TRIP	PWM2_OVER_ERR_TRIP	PWM2_TRIP_RESET	PWM2_TRIP_CMP0_EN	PWM2_TRIP_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
PWM2_TRIP_MASK							
R/W-0h							

7	6	5	4	3	2	1	0
PWM2_DEBOUNCE_VALUE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10365. ICSSG_PWM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	PWM2_TRIP_S	R/W	0h	Trip status. Cleared by trip reset.
29-21	PWM2_TRIP_VEC	R	0h	Trip trigger cause vector. Cleared by trip reset. 0h: PWM2_POS_ERR_TRIP (trip_e5) 1h: PWM2_OVER_ERR_TRIP (trip_e4) 2h: PWM2_0_SD_SHORT_ERR_TRIP (trip_e3_0) 3h: PWM2_1_SD_SHORT_ERR_TRIP (trip_e3_1) 4h: PWM2_2_SD_SHORT_ERR_TRIP (trip_e3_2) 5h: PWM2_DEBOUNCE_TRIP_IN (trip_e2) 6h: PWM2_0_DEBOUNCE_TRIP (trip_e1_0) 7h: PWM2_1_DEBOUNCE_TRIP (trip_e1_1) 8h: PWM2_2_DEBOUNCE_TRIP (trip_e1_2)
20	PWM2_POS_ERR_TRIP	R/W	0h	Software position feedback error trip
19	PWM2_OVER_ERR_TRIP	R/W	0h	Software overcurrent error trip
18	PWM2_TRIP_RESET	R/W	0h	Software trip reset

Table 14-10365. ICSSG_PWM2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	PWM2_TRIP_CMP0_EN	R/W	0h	CMP0 reset trip clear enable
16-8	PWM2_TRIP_MASK	R/W	0h	Software mask for trip, one hot
7-0	PWM2_DEBOUNCE_VALUE	R/W	0h	Debounce counter, defines the number of core_clk required for the pulse not to get rejected

73 ICSSG_PWM3 Register (Offset = 13Ch) [reset = X]

ICSSG_PWM3 is shown in Figure 14-3431 and described in Table 14-6937.

Return to Summary Table.

PWM3 Trip Configuration Register

Table 14-10366. ICSSG_PWM3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 613Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 613Ch

Figure 14-3431. ICSSG_PWM3 Register

31	30	29	28	27	26	25	24
RESERVED	PWM3_TRIP_S	PWM3_TRIP_VEC					
R/W-X	R/W-0h	R-0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWM3_TRIP_VEC			PWM3_POS_ERR_TRIP	PWM3_OVER_ERR_TRIP	PWM3_TRIP_RESET	PWM3_TRIP_CMP0_EN	PWM3_TRIP_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWM3_TRIP_MASK							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM3_DEBOUNCE_VALUE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10368. ICSSG_PWM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	PWM3_TRIP_S	R/W	0h	Trip status.
29-21	PWM3_TRIP_VEC	R	0h	Trip trigger cause vector. Cleared by trip reset. 0h: PWM3_POS_ERR_TRIP (trip_e5) 1h: PWM3_OVER_ERR_TRIP (trip_e4) 2h: PWM3_0_SD_SHORT_ERR_TRIP (trip_e3_0) 3h: PWM3_1_SD_SHORT_ERR_TRIP (trip_e3_1) 4h: PWM3_2_SD_SHORT_ERR_TRIP (trip_e3_2) 5h: PWM3_DEBOUNCE_TRIP_IN (trip_e2) 6h: PWM3_0_DEBOUNCE_TRIP (trip_e1_0) 7h: PWM3_1_DEBOUNCE_TRIP (trip_e1_1) 8h: PWM3_2_DEBOUNCE_TRIP (trip_e1_2)
20	PWM3_POS_ERR_TRIP	R/W	0h	Software position feedback error trip
19	PWM3_OVER_ERR_TRIP	R/W	0h	Software overcurrent error trip
18	PWM3_TRIP_RESET	R/W	0h	Software trip reset

Table 14-10368. ICSSG_PWM3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	PWM3_TRIP_CMP0_EN	R/W	0h	CMP0 reset trip clear enable
16-8	PWM3_TRIP_MASK	R/W	0h	Software mask for trip, one hot
7-0	PWM3_DEBOUNCE_VALUE	R/W	0h	Debounce counter, defines the number of core_clk required for the pulse not to get rejected

74 ICSSG_PWM0_0 Register (Offset = 140h) [reset = X]

ICSSG_PWM0_0 is shown in Figure 14-3432 and described in Table 14-6939.

Return to Summary Table.

PWM0 State Configuration 0 Register.

Table 14-10369. ICSSG_PWM0_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6140h
PRU_ICSSG1_PR1_CFG_SLV	300A 6140h

Figure 14-3432. ICSSG_PWM0_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM0_0_NEG_ACT		PWM0_0_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM0_0_NEG_TRIP		PWM0_0_POS_TRIP		PWM0_0_NEG_INIT		PWM0_0_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10371. ICSSG_PWM0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM0_0_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM0_0_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM0_0_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM0_0_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10371. ICSSG_PWM0_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM0_0_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM0_0_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

75 ICSSG_PWM0_1 Register (Offset = 144h) [reset = X]

ICSSG_PWM0_1 is shown in Figure 14-3433 and described in Table 14-6941.

Return to Summary Table.

PWM0 State Configuration 1 Register.

Table 14-10372. ICSSG_PWM0_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6144h
PRU_ICSSG1_PR1_CFG_SLV	300A 6144h

Figure 14-3433. ICSSG_PWM0_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PWM0_1_NEG_ACT		PWM0_1_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM0_1_NEG_TRIP		PWM0_1_POS_TRIP		PWM0_1_NEG_INIT		PWM0_1_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10374. ICSSG_PWM0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM0_1_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM0_1_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM0_1_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM0_1_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10374. ICSSG_PWM0_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM0_1_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM0_1_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

76 ICSSG_PWM0_2 Register (Offset = 148h) [reset = X]

ICSSG_PWM0_2 is shown in Figure 14-3434 and described in Table 14-6943.

Return to Summary Table.

PWM0 State Configuration 2 Register.

Table 14-10375. ICSSG_PWM0_2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6148h
PRU_ICSSG1_PR1_CFG_SLV	300A 6148h

Figure 14-3434. ICSSG_PWM0_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PWM0_2_NEG_ACT		PWM0_2_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM0_2_NEG_TRIP		PWM0_2_POS_TRIP		PWM0_2_NEG_INIT		PWM0_2_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10377. ICSSG_PWM0_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM0_2_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM0_2_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM0_2_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM0_2_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10377. ICSSG_PWM0_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM0_2_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM0_2_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

77 ICSSG_PWM1_0 Register (Offset = 14Ch) [reset = X]

ICSSG_PWM1_0 is shown in Figure 14-3435 and described in Table 14-6945.

Return to Summary Table.

PWM1 State Configuration 0 Register.

Table 14-10378. ICSSG_PWM1_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 614Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 614Ch

Figure 14-3435. ICSSG_PWM1_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PWM1_0_NEG_ACT		PWM1_0_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM1_0_NEG_TRIP		PWM1_0_POS_TRIP		PWM1_0_NEG_INIT		PWM1_0_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10380. ICSSG_PWM1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM1_0_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM1_0_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM1_0_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM1_0_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10380. ICSSG_PWM1_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM1_0_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM1_0_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

78 ICSSG_PWM1_1 Register (Offset = 150h) [reset = X]

ICSSG_PWM1_1 is shown in Figure 14-3436 and described in Table 14-6947.

Return to Summary Table.

PWM1 State Configuration 1 Register.

Table 14-10381. ICSSG_PWM1_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6150h
PRU_ICSSG1_PR1_CFG_SLV	300A 6150h

Figure 14-3436. ICSSG_PWM1_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM1_1_NEG_ACT		PWM1_1_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM1_1_NEG_TRIP		PWM1_1_POS_TRIP		PWM1_1_NEG_INIT		PWM1_1_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10383. ICSSG_PWM1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM1_1_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM1_1_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM1_1_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM1_1_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10383. ICSSG_PWM1_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM1_1_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM1_1_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

79 ICSSG_PWM1_2 Register (Offset = 154h) [reset = X]

ICSSG_PWM1_2 is shown in Figure 14-3437 and described in Table 14-6949.

Return to Summary Table.

PWM1 State Configuration 2 Register.

Table 14-10384. ICSSG_PWM1_2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6154h
PRU_ICSSG1_PR1_CFG_SLV	300A 6154h

Figure 14-3437. ICSSG_PWM1_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PWM1_2_NEG_ACT		PWM1_2_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM1_2_NEG_TRIP		PWM1_2_POS_TRIP		PWM1_2_NEG_INIT		PWM1_2_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10386. ICSSG_PWM1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM1_2_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM1_2_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM1_2_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM1_2_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10386. ICSSG_PWM1_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM1_2_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM1_2_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

80 ICSSG_PWM2_0 Register (Offset = 158h) [reset = X]

ICSSG_PWM2_0 is shown in Figure 14-3438 and described in Table 14-6951.

Return to Summary Table.

PWM2 State Configuration 0 Register.

Table 14-10387. ICSSG_PWM2_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6158h
PRU_ICSSG1_PR1_CFG_SLV	300A 6158h

Figure 14-3438. ICSSG_PWM2_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM2_0_NEG_ACT		PWM2_0_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM2_0_NEG_TRIP		PWM2_0_POS_TRIP		PWM2_0_NEG_INIT		PWM2_0_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10389. ICSSG_PWM2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM2_0_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM2_0_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM2_0_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM2_0_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10389. ICSSG_PWM2_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM2_0_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM2_0_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

81 ICSSG_PWM2_1 Register (Offset = 15Ch) [reset = X]

ICSSG_PWM2_1 is shown in Figure 14-3439 and described in Table 14-6953.

Return to Summary Table.

PWM2 State Configuration 1 Register.

Table 14-10390. ICSSG_PWM2_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 615Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 615Ch

Figure 14-3439. ICSSG_PWM2_1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">PWM2_1_NEG_ACT</td><td colspan="2">PWM2_1_POS_ACT</td></tr>
<tr><td colspan="4">R/W-X</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PWM2_1_NEG_TRIP</td><td colspan="2">PWM2_1_POS_TRIP</td><td colspan="2">PWM2_1_NEG_INIT</td><td colspan="2">PWM2_1_POS_INIT</td></tr>
<tr><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10392. ICSSG_PWM2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM2_1_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM2_1_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM2_1_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM2_1_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10392. ICSSG_PWM2_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM2_1_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM2_1_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

82 ICSSG_PWM2_2 Register (Offset = 160h) [reset = X]

ICSSG_PWM2_2 is shown in Figure 14-3440 and described in Table 14-6955.

Return to Summary Table.

PWM2 State Configuration 2 Register.

Table 14-10393. ICSSG_PWM2_2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6160h
PRU_ICSSG1_PR1_CFG_SLV	300A 6160h

Figure 14-3440. ICSSG_PWM2_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM2_2_NEG_ACT		PWM2_2_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM2_2_NEG_TRIP		PWM2_2_POS_TRIP		PWM2_2_NEG_INIT		PWM2_2_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10395. ICSSG_PWM2_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM2_2_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM2_2_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM2_2_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM2_2_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10395. ICSSG_PWM2_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM2_2_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM2_2_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

83 ICSSG_PWM3_0 Register (Offset = 164h) [reset = X]

ICSSG_PWM3_0 is shown in Figure 14-3441 and described in Table 14-6957.

Return to Summary Table.

PWM3 State Configuration 0 Register.

Table 14-10396. ICSSG_PWM3_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6164h
PRU_ICSSG1_PR1_CFG_SLV	300A 6164h

Figure 14-3441. ICSSG_PWM3_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PWM3_0_NEG_ACT		PWM3_0_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM3_0_NEG_TRIP		PWM3_0_POS_TRIP		PWM3_0_NEG_INIT		PWM3_0_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10398. ICSSG_PWM3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM3_0_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM3_0_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM3_0_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM3_0_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10398. ICSSG_PWM3_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM3_0_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM3_0_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

84 ICSSG_PWM3_1 Register (Offset = 168h) [reset = X]

ICSSG_PWM3_1 is shown in Figure 14-3442 and described in Table 14-6959.

Return to Summary Table.

PWM3 State Configuration 1 Register.

Table 14-10399. ICSSG_PWM3_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6168h
PRU_ICSSG1_PR1_CFG_SLV	300A 6168h

Figure 14-3442. ICSSG_PWM3_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PWM3_1_NEG_ACT		PWM3_1_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM3_1_NEG_TRIP		PWM3_1_POS_TRIP		PWM3_1_NEG_INIT		PWM3_1_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10401. ICSSG_PWM3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM3_1_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM3_1_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM3_1_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM3_1_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10401. ICSSG_PWM3_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM3_1_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM3_1_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

85 ICSSG_PWM3_2 Register (Offset = 16Ch) [reset = X]

ICSSG_PWM3_2 is shown in Figure 14-3443 and described in Table 14-6961.

Return to Summary Table.

PWM3 State Configuration 2 Register.

Table 14-10402. ICSSG_PWM3_2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 616Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 616Ch

Figure 14-3443. ICSSG_PWM3_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM3_2_NEG_ACT		PWM3_2_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM3_2_NEG_TRIP		PWM3_2_POS_TRIP		PWM3_2_NEG_INIT		PWM3_2_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10404. ICSSG_PWM3_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM3_2_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM3_2_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM3_2_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM3_2_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H

Table 14-10404. ICSSG_PWM3_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PWM3_2_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H
1-0	PWM3_2_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

86 ICSSG_SPIN_LOCK0 Register (Offset = 170h) [reset = X]

ICSSG_SPIN_LOCK0 is shown in Figure 14-3444 and described in Table 14-6963.

Return to Summary Table.

Spin Lock 0 Register.

Table 14-10405. ICSSG_SPIN_LOCK0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6170h
PRU_ICSSG1_PR1_CFG_SLV	300A 6170h

Figure 14-3444. ICSSG_SPIN_LOCK0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		MMR_OWN_REQ_VECTOR_0					
R/W-X		R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						MMR_OWN_REQ_CLR_0	MMR_OWN_REQ_STATUS_0
R/W-X						W-0h	R-X

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10407. ICSSG_SPIN_LOCK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-8	MMR_OWN_REQ_VECTOR_0	R/W	0h	Spin Lock flag Vector
7-2	RESERVED	R/W	X	
1	MMR_OWN_REQ_CLR_0	W	0h	Spin Lock Status Clear
0	MMR_OWN_REQ_STATUS_0	R	X	Spin Lock Status

87 ICSSG_SPIN_LOCK1 Register (Offset = 174h) [reset = X]

ICSSG_SPIN_LOCK1 is shown in Figure 14-3445 and described in Table 14-6965.

Return to Summary Table.

Spin Lock 1 Register.

Table 14-10408. ICSSG_SPIN_LOCK1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6174h
PRU_ICSSG1_PR1_CFG_SLV	300A 6174h

Figure 14-3445. ICSSG_SPIN_LOCK1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED		MMR_OWN_REQ_VECTOR_1					
R/W-X		R/W-0h					

7	6	5	4	3	2	1	0
RESERVED						MMR_OWN_REQ_CLR_1	MMR_OWN_REQ_STATUS_1
R/W-X						W-0h	R-X

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10410. ICSSG_SPIN_LOCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-8	MMR_OWN_REQ_VECTOR_1	R/W	0h	Spin Lock flag Vector
7-2	RESERVED	R/W	X	
1	MMR_OWN_REQ_CLR_1	W	0h	Spin Lock Status Clear
0	MMR_OWN_REQ_STATUS_1	R	X	Spin Lock Status

88 ICSSG_PA_STAT_PDSP_CFG0 Register (Offset = 178h) [reset = 0h]

ICSSG_PA_STAT_PDSP_CFG0 is shown in Figure 14-3446 and described in Table 14-6967.

Return to Summary Table.

PA STATS PRU Vector 0 Register.

Table 14-10411. ICSSG_PA_STAT_PDSP_CFG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6178h
PRU_ICSSG1_PR1_CFG_SLV	300A 6178h

Figure 14-3446. ICSSG_PA_STAT_PDSP_CFG0 Register

31	30	29	28	27	26	25	24
PA_PDSP0_INC_TYPE	PA_PDSP0_INC_VAL						
R/W-0h	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PA_PDSP0_INC_VAL							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_PDSP0_INC_VAL		PA_PDSP0_INDEX					
R/W-0h		R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_PDSP0_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10413. ICSSG_PA_STAT_PDSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PA_PDSP0_INC_TYPE	R/W	0h	pa_pdsp0_inc_type
30-14	PA_PDSP0_INC_VAL	R/W	0h	pa_pdsp0_inc_val
13-0	PA_PDSP0_INDEX	R/W	0h	pa_pdsp0_index

89 ICSSG_PA_STAT_PDSP_STAT0 Register (Offset = 17Ch) [reset = X]

ICSSG_PA_STAT_PDSP_STAT0 is shown in Figure 14-3447 and described in Table 14-6969.

Return to Summary Table.

PA STATS PRU Status 0 Register.

Table 14-10414. ICSSG_PA_STAT_PDSP_STAT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 617Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 617Ch

Figure 14-3447. ICSSG_PA_STAT_PDSP_STAT0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				PA_PDSP0_STATUS			PA_PDSP0_READY
R-X				R-0h			R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10416. ICSSG_PA_STAT_PDSP_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-1	PA_PDSP0_STATUS	R	0h	pa_pdsp0_status
0	PA_PDSP0_READY	R	0h	pa_pdsp0_ready

90 ICSSG_PA_STAT_PDSP_CFG1 Register (Offset = 180h) [reset = 0h]

ICSSG_PA_STAT_PDSP_CFG1 is shown in Figure 14-3448 and described in Table 14-6971.

Return to Summary Table.

PA STATS PRU Vector 1 Register.

Table 14-10417. ICSSG_PA_STAT_PDSP_CFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6180h
PRU_ICSSG1_PR1_CFG_SLV	300A 6180h

Figure 14-3448. ICSSG_PA_STAT_PDSP_CFG1 Register

31	30	29	28	27	26	25	24
PA_PDSP1_INC_TYPE	PA_PDSP1_INC_VAL						
R/W-0h	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PA_PDSP1_INC_VAL							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_PDSP1_INC_VAL		PA_PDSP1_INDEX					
R/W-0h		R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_PDSP1_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10419. ICSSG_PA_STAT_PDSP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PA_PDSP1_INC_TYPE	R/W	0h	pa_pdsp1_inc_type
30-14	PA_PDSP1_INC_VAL	R/W	0h	pa_pdsp1_inc_val
13-0	PA_PDSP1_INDEX	R/W	0h	pa_pdsp1_index

91 ICSSG_PA_STAT_PDSP_STAT1 Register (Offset = 184h) [reset = X]

ICSSG_PA_STAT_PDSP_STAT1 is shown in Figure 14-3449 and described in Table 14-6973.

Return to Summary Table.

PA STATS PRU Status 1 Register.

Table 14-10420. ICSSG_PA_STAT_PDSP_STAT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6184h
PRU_ICSSG1_PR1_CFG_SLV	300A 6184h

Figure 14-3449. ICSSG_PA_STAT_PDSP_STAT1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				PA_PDSP1_STATUS			PA_PDSP1_READY
R-X				R-0h			R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10422. ICSSG_PA_STAT_PDSP_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-1	PA_PDSP1_STATUS	R	0h	pa_pdsp1_status
0	PA_PDSP1_READY	R	0h	pa_pdsp1_ready

92 ICSSG_PA_STAT_PDSP_CFG2 Register (Offset = 188h) [reset = 0h]

ICSSG_PA_STAT_PDSP_CFG2 is shown in Figure 14-3450 and described in Table 14-6975.

Return to Summary Table.

PA STATS PRU Vector 2 Register.

Table 14-10423. ICSSG_PA_STAT_PDSP_CFG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6188h
PRU_ICSSG1_PR1_CFG_SLV	300A 6188h

Figure 14-3450. ICSSG_PA_STAT_PDSP_CFG2 Register

31	30	29	28	27	26	25	24
PA_PDSP2_INC_TYPE	PA_PDSP2_INC_VAL						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
PA_PDSP2_INC_VAL							
R/W-0h							
15	14	13	12	11	10	9	8
PA_PDSP2_INC_VAL		PA_PDSP2_INDEX					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
PA_PDSP2_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10425. ICSSG_PA_STAT_PDSP_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PA_PDSP2_INC_TYPE	R/W	0h	pa_pdsp2_inc_type
30-14	PA_PDSP2_INC_VAL	R/W	0h	pa_pdsp2_inc_val
13-0	PA_PDSP2_INDEX	R/W	0h	pa_pdsp2_index

93 ICSSG_PA_STAT_PDSP_STAT2 Register (Offset = 18Ch) [reset = X]

ICSSG_PA_STAT_PDSP_STAT2 is shown in Figure 14-3451 and described in Table 14-6977.

Return to Summary Table.

PA STATS PRU Status 2 Register.

Table 14-10426. ICSSG_PA_STAT_PDSP_STAT2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 618Ch
PRU_ICSSG1_PR1_CFG_SLV	300A 618Ch

Figure 14-3451. ICSSG_PA_STAT_PDSP_STAT2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="3">PA_PDSP2_STATUS</td><td>PA_PDSP2_READY</td></tr>
<tr><td colspan="4">R-X</td><td colspan="3">R-0h</td><td>R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10428. ICSSG_PA_STAT_PDSP_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-1	PA_PDSP2_STATUS	R	0h	pa_pdsp2_status
0	PA_PDSP2_READY	R	0h	pa_pdsp2_ready

94 ICSSG_PA_STAT_PDSP_CFG3 Register (Offset = 190h) [reset = 0h]

ICSSG_PA_STAT_PDSP_CFG3 is shown in Figure 14-3452 and described in Table 14-6979.

Return to Summary Table.

PA STATS PRU Vector 3 Register.

Table 14-10429. ICSSG_PA_STAT_PDSP_CFG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6190h
PRU_ICSSG1_PR1_CFG_SLV	300A 6190h

Figure 14-3452. ICSSG_PA_STAT_PDSP_CFG3 Register

31	30	29	28	27	26	25	24
PA_PDSP3_INC_TYPE	PA_PDSP3_INC_VAL						
R/W-0h	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PA_PDSP3_INC_VAL							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_PDSP3_INC_VAL		PA_PDSP3_INDEX					
R/W-0h		R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_PDSP3_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10431. ICSSG_PA_STAT_PDSP_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PA_PDSP3_INC_TYPE	R/W	0h	pa_pdsp3_inc_type
30-14	PA_PDSP3_INC_VAL	R/W	0h	pa_pdsp3_inc_val
13-0	PA_PDSP3_INDEX	R/W	0h	pa_pdsp3_index

95 ICSSG_PA_STAT_PDSP_STAT3 Register (Offset = 194h) [reset = X]

ICSSG_PA_STAT_PDSP_STAT3 is shown in Figure 14-3453 and described in Table 14-6981.

Return to Summary Table.

PA STATS PRU Status 3 Register.

Table 14-10432. ICSSG_PA_STAT_PDSP_STAT3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	3002 6194h
PRU_ICSSG1_PR1_CFG_SLV	300A 6194h

Figure 14-3453. ICSSG_PA_STAT_PDSP_STAT3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PA_PDSP3_STATUS			PA_PDSP3_READY
R-X				R-0h			R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10434. ICSSG_PA_STAT_PDSP_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-1	PA_PDSP3_STATUS	R	0h	pa_pdsp3_status
0	PA_PDSP3_READY	R	0h	pa_pdsp3_ready

14.3.6.1.6 PRU_ECAP_ECAP0 Registers

Table 14-6983 lists the memory-mapped registers for the PRU_ECAP_ECAP0 registers. All register offset addresses not listed in Table 14-6983 should be considered as reserved locations and the register contents should not be modified.

Table 14-10435. PRU_ECAP_ECAP0 Instances

Instance	Base Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0000h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0000h

Table 14-10436. PRU_ECAP_ECAP0 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV Physical Address	PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV Physical Address
0h	ECAP_TSCNT	Time Stamp Counter Register	3003 0000h	300B 0000h
4h	ECAP_CNTPHS	Counter Phase Control Register	3003 0004h	300B 0004h
8h	ECAP_CAP1	Capture-1 Register	3003 0008h	300B 0008h
Ch	ECAP_CAP2	Capture-2 Register	3003 000Ch	300B 000Ch
10h	ECAP_CAP3	Capture-3 Register	3003 0010h	300B 0010h
14h	ECAP_CAP4	Capture-4 Register	3003 0014h	300B 0014h
28h	ECAP_ECCTL2_ECCTL1	ECAP Control Register 1	3003 0028h	300B 0028h
2Ch	ECAP_ECFLG_ECEINT	ECAP Interrupt Enable Register	3003 002Ch	300B 002Ch
30h	ECAP_ECCLR	ECAP Interrupt Clear Register	3003 0030h	300B 0030h
34h	ECAP_ECFRC	ECAP Interrupt Forcing Register	3003 0034h	300B 0034h
5Ch	ECAP_PID	ECAP Peripheral Id Register	3003 005Ch	300B 005Ch

1 ECAP_TSCNT Register (Offset = 0h) [reset = 0h]

ECAP_TSCNT is shown in Figure 14-3454 and described in Table 14-6985.

Return to Summary Table.

Time Stamp Counter Register.

Table 14-10437. ECAP_TSCNT Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0000h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0000h

Figure 14-3454. ECAP_TSCNT Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TSCNT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10439. ECAP_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TSCNT	R/W	0h	Active 32-bit counter register which is used as the capture time-base.

2 ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]

ECAP_CNTPHS is shown in Figure 14-3455 and described in Table 14-6987.

Return to Summary Table.

Counter Phase Control Register.

Table 14-10440. ECAP_CNTPHS Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0004h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0004h

Figure 14-3455. ECAP_CNTPHS Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CNTPHS</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10442. ECAP_CNTPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CNTPHS	R/W	0h	Counter phase value register that can be programmed for phase lag/lead. This register shadows ECAP_TSCNT and is loaded into ECAP_TSCNT upon either a SYNCI event or software force via a control bit. Used to achieve phase control synchronization with respect to other ECAP and EPWM time-bases.

3 ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

ECAP_CAP1 is shown in Figure 14-3456 and described in Table 14-6989.

Return to Summary Table.

Capture-1 Register.

Table 14-10443. ECAP_CAP1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0008h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0008h

Figure 14-3456. ECAP_CAP1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10445. ECAP_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP1	R/W	0h	This register can be loaded (written) by the following: a) Time-stamp (that is, counter value) during a capture event. b) Software may be useful for test purposes/initialization. c) APRD shadow register (that is, ECAP_CAP3) when used in APWM mode.

4 ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

ECAP_CAP2 is shown in Figure 14-3457 and described in Table 14-6991.

Return to Summary Table.

Capture-2 Register.

Table 14-10446. ECAP_CAP2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 000Ch
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 000Ch

Figure 14-3457. ECAP_CAP2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP2																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10448. ECAP_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP2	R/W	0h	This register can be loaded (written) by the following: a) Time-stamp (that is, counter value) during a capture event. b) Software may be useful for test purposes. c) ACMP shadow register (that is, ECAP_CAP4) when used in APWM mode.

5 ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

ECAP_CAP3 is shown in Figure 14-3458 and described in Table 14-6993.

Return to Summary Table.

Capture-3 Register.

Table 14-10449. ECAP_CAP3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0010h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0010h

Figure 14-3458. ECAP_CAP3 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAP3</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10451. ECAP_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP3	R/W	0h	In CMP mode this is a time-stamp capture register. In APWM mode this is the period shadow (APER) register. User updates the PWM period value via this register. In this mode ECAP_CAP3 (APRD) shadows ECAP_CAP1.

6 ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

ECAP_CAP4 is shown in Figure 14-3459 and described in Table 14-6995.

Return to Summary Table.

Capture-4 Register.

Table 14-10452. ECAP_CAP4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0014h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0014h

Figure 14-3459. ECAP_CAP4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP4																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10454. ECAP_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP4	R/W	0h	In CMP mode this is a time-stamp capture register. In APWM mode this is the compare shadow (ACMP) register. User updates the PWM compare value via this register. In this mode ECAP_CAP4 (ACMP) shadows ECAP_CAP2.

7 ECAP_ECCTL2_ECCTL1 Register (Offset = 28h) [reset = 00060000h]

ECAP_ECCTL2_ECCTL1 is shown in Figure 14-3460 and described in Table 14-6997.

Return to Summary Table.

ECAP Control Register 1.

Table 14-10455. ECAP_ECCTL2_ECCTL1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0028h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0028h

Figure 14-3460. ECAP_ECCTL2_ECCTL1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">FILTER</td><td>APWMPOL</td><td>CAP_APWM</td><td>SWSYNC</td></tr>
<tr><td colspan="5">R-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">SYNCO_SEL</td><td>SYNCI_EN</td><td>TSCNTSTP</td><td>REARM_RESET</td><td colspan="2">STOPVALUE</td><td>CONT_ONESHT</td></tr>
<tr><td colspan="2">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td colspan="2">R/W-3h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>FREE</td><td>SOFT</td><td colspan="5">EVTFLTPS</td><td>CAPLDEN</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td colspan="5">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CTRRST4</td><td>CAP4POL</td><td>CTRRST3</td><td>CAP3POL</td><td>CTRRST2</td><td>CAP2POL</td><td>CTRRST1</td><td>CAP1POL</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10457. ECAP_ECCTL2_ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	FILTER	R	0h	
26	APWMPOL	R/W	0h	APWM output polarity select: 0h = Output is active high (that is, compare value defines high time) 1h = Output is active low (that is, compare value defines low time) Note: This is applicable only in APWM operating mode.

Table 14-10457. ECAP_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CAP_APWM	R/W	0h	CAP/APWM operating mode select: 0h = ECAP module operates in capture mode. This mode forces the following configuration: a) Inhibits ECAP_TSCNT resets via CTR = PRD event b) Inhibits shadow loads on ECAP_CAP1 and ECAP_CAP2 registers. c) Permits user to enable ECAP_CAP1 to ECAP_CAP4 register load. d) ECAP input/APWM output pin operates as a capture input. 1h = ECAP module operates in APWM mode. This mode forces the following configuration: a) Resets TSCNT on CTR = PRD event (period boundary). b) Permits shadow loading on ECAP_CAP1 and ECAP_CAP2 registers. c) Disables loading of time-stamps into ECAP_CAP1 to ECAP_CAP4 registers. d) ECAP input/APWM output pin operates as a APWM output.
24	SWSYNC	R/W	0h	Software forced counter (ECAP_TSCNT) synchronizing: 0h = Writing a zero has no effect will always return a zero 1h = Writing a one will force a ECAP_TSCNT shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0b00. After writing a one this bit returns to a zero. Note: This provides a convenient software method to synchronize some or all ECAP timebases. In APWM mode, the synchronizing can also be done via the CTR = PRD event.
23-22	SYNCO_SEL	R/W	0h	Sync-out select: 0h = Select sync-in event to be the sync-out signal (pass through) 1h = Select CTR = PRD event to be the sync-out signal 2h = Disable sync out signal 3h = Disable sync out signal Note: Selection CTR = PRD is meaningful only in APWM mode, however can still be chosen in CAP mode, if user believes it to be useful.
21	SYNCI_EN	R/W	0h	Counter (ECAP_TSCNT) sync-in select mode: 0h = Disable sync-in option 1h = Enable counter (ECAP_TSCNT) to be loaded from ECAP_CNTPHS register upon either a SYNCI signal or a software force event

Table 14-10457. ECAP_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TSCNTSTP	R/W	0h	Counter stop (freeze) control: 0h = Counter stopped 1h = Counter free running
19	REARM_RESET	R/W	0h	One-shot re-arming, that is, wait for stop trigger: 0h = Writing a zero has no effect (reading always returns a 0) 1h = Writing a one arms the one-shot sequence as follows: 1) resets the mod4 counter to zero 2) un-freezes the mod4 counter 3) enables capture register loads Note: The re-arm function is valid in oneshot or continuous mode.
18-17	STOPVALUE	R/W	3h	Stop value for one-shot mode. This is the number (between 1-4) of captures allowed to occur before the CAP(1-4) registers are frozen, that is, capture sequence is stopped. 0h = Stop after capture event 1 1h = Stop after capture event 2 2h = Stop after capture event 3 3h = Stop after capture event 4 Note: STOPVALUE is compared to mod4 counter, and when equal, the following two actions occur: (1) Mod4 counter is stopped (frozen). (2) Capture register loads are inhibited. Note: In one shot mode, further interrupt events are blocked until re-armed, once the number of events captured has been reached .
16	CONT_ONESHT	R/W	0h	Continuous or one-shot mode control (applicable only in capture mode): 0h = Operate in continuous mode 1h = Operate in one-shot mode
15	FREE	R/W	0h	Emulation control. 0h = ECAP_TSCNT counter stops immediately on emulation suspend 1h = ECAP_TSCNT counter runs until = 0 0b1x = ECAP_TSCNT counter is unaffected by emulation suspend (run free)
14	SOFT	R/W	0h	Emulation control. 0h = ECAP_TSCNT counter stops immediately on emulation suspend 1h = ECAP_TSCNT counter runs until = 0 0b1x = ECAP_TSCNT counter is unaffected by emulation suspend (run free)

Table 14-10457. ECAP_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-9	EVTFLTPS	R/W	0h	Event filter prescale select: 0h = Divide by 1 (that is, no prescale, by-pass the prescaler) 1h = Divide by 2 2h = Divide by 4 3h = Divide by 6 4h = Divide by 8 5h = Divide by 10 1Eh = Divide by 60 1Fh = Divide by 62
8	CAPLDEN	R/W	0h	Enable loading of CAP(1-4) registers on a capture event: 0h = Disable CAP (1-4) register loads at capture event time 1h = Enable CAP(1-4) register loads at capture event time
7	CTRRST4	R/W	0h	Counter reset on capture event 4: 0h = Do not reset counter on capture event 4 (absolute time stamp) 1h = Reset counter after event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	R/W	0h	Capture event 4 polarity select: 0h = Capture event 4 triggered on a rising edge (RE) 1h = Capture event 4 triggered on a falling edge (FE)
5	CTRRST3	R/W	0h	Counter reset on capture event 3: 0h = Do not reset counter on capture event 3 (absolute time stamp) 1h = Reset counter after event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture event 3 polarity select: 0h = Capture event 3 triggered on a rising edge (RE) 1h = Capture event 3 triggered on a falling edge (FE)
3	CTRRST2	R/W	0h	Counter reset on capture event 2: 0h = Do not reset counter on capture event 2 (absolute time stamp) 1h = Reset counter after event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture event 2 polarity select: 0h = Capture event 2 triggered on a rising edge (RE) 1h = Capture event 2 triggered on a falling edge (FE)

Table 14-10457. ECAP_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CTRRST1	R/W	0h	Counter reset on capture event 1: 0h = Do not reset counter on capture event 1 (absolute time stamp) 1h = Reset counter after event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture event 1 polarity select: 0h = Capture event 1 triggered on a rising edge (RE) 1h = Capture event 1 triggered on a falling edge (FE)

8 ECAP_ECFLG_ECEINT Register (Offset = 2Ch) [reset = 0h]

ECAP_ECFLG_ECEINT is shown in Figure 14-3461 and described in Table 14-6999.

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ECAP Interrupt Enable Register.

Table 14-10458. ECAP_ECFLG_ECEINT Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 002Ch
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 002Ch

Figure 14-3461. ECAP_ECFLG_ECEINT Register

31	30	29	28	27	26	25	24
FLAG_RESV0							
R-0h							
23	22	21	20	19	18	17	16
FLAG_CMPEQ	FLAG_PRDEQ	FLAG_CNTOVF	FLAG_CEVT4	FLAG_CEVT3	FLAG_CEVT2	FLAG_CEVT1	FLAG_INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
EN__RESV1							
R-0h							
7	6	5	4	3	2	1	0
EN_CMPEQ	EN_PRDEQ	EN_CNTOVF	EN_CEVT4	EN_CEVT3	EN_CEVT2	EN_CEVT1	EN_RESV0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10460. ECAP_ECFLG_ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	FLAG_RESV0	R	0h	
23	FLAG_CMPEQ	R	0h	Compare equal status flag: 0h = Indicates no event occurred 1h = Indicates the counter (ECAP_TSCNT) reached the compare register value (ACMP) Note: This flag is only active in APWM mode.
22	FLAG_PRDEQ	R	0h	Period equal status flag: 0h = Indicates no event occurred 1h = Indicates the counter (ECAP_TSCNT) reached the period register value (APER) and was reset Note: This flag is only active in APWM mode.

Table 14-10460. ECAP_ECFLG_ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	FLAG_CNTOVF	R	0h	Counter overflow status flag: 0h = Indicates no event occurred 1h = Indicates the counter (ECAP_TSCNT) has made the transition from FFFFFFFFh to 00000000h Note: This flag is active in CAP and APWM mode.
20	FLAG_CEVT4	R	0h	Capture event 4 status flag: 0h = Indicates no event occurred 1h = Indicates the fourth event occurred at ECAPx pin Note: This flag is only active in CAP mode.
19	FLAG_CEVT3	R	0h	Capture event 3 status flag: 0h = Indicates no event occurred 1h = Indicates the third event occurred at ECAPx pin Note: This flag is only active in CAP mode.
18	FLAG_CEVT2	R	0h	Capture event 2 status flag: 0h = Indicates no event occurred 1h = Indicates the second event occurred at ECAPx pin Note: This flag is only active in CAP mode.
17	FLAG_CEVT1	R	0h	Capture event 1 status flag: 0h = Indicates no event occurred 1h = Indicates the first event occurred at ECAPx pin Note: This flag is only active in CAP mode.
16	FLAG_INT	R	0h	Global interrupt status flag: 0h = Indicates no interrupt generated 1h = Indicates that an interrupt was generated from one of the following events
15-8	EN__RESV1	R	0h	
7	EN_CMPEQ	R/W	0h	Compare equal interrupt enable: 0h = Disable compare equal as an interrupt source 1h = Enable compare equal as an interrupt source
6	EN_PRDEQ	R/W	0h	Period equal interrupt enable: 0h = Disable period equal as an interrupt source 1h = Enable period equal as an interrupt source
5	EN_CNTOVF	R/W	0h	Counter overflow interrupt enable: 0h = Disable counter overflow as an interrupt source 1h = Enable counter overflow as an interrupt source

Table 14-10460. ECAP_ECFLG_ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EN_CEVT4	R/W	0h	Capture event 4 interrupt enable: 0h = Disable capture event 1 as an interrupt source 1h = Enable capture event 1 as an interrupt source
3	EN_CEVT3	R/W	0h	Capture event 3 interrupt enable: 0h = Disable capture event 1 as an interrupt source 1h = Enable capture event 1 as an interrupt source
2	EN_CEVT2	R/W	0h	Capture event 2 interrupt enable: 0h = Disable capture event 1 as an interrupt source 1h = Enable capture event 1 as an interrupt source
1	EN_CEVT1	R/W	0h	Capture event 1 interrupt enable: 0h = Disable capture event 1 as an interrupt source 1h = Enable capture event 1 as an interrupt source
0	EN_RESV0	R	0h	

9 ECAP_ECCLR Register (Offset = 30h) [reset = X]

ECAP_ECCLR is shown in Figure 14-3462 and described in Table 14-7001.

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ECAP Interrupt Clear Register.

Table 14-10461. ECAP_ECCLR Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0030h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0030h

Figure 14-3462. ECAP_ECCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
_RESV0							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10463. ECAP_ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	_RESV0	R	0h	
7	CMPEQ	R/W	0h	Compare equal status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
6	PRDEQ	R/W	0h	Period equal status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
5	CNTOVF	R/W	0h	Counter overflow status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
4	CEVT4	R/W	0h	Capture event 4 status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition

Table 14-10463. ECAP_ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CEVT3	R/W	0h	Capture event 3 status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
2	CEVT2	R/W	0h	Capture event 2 status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
1	CEVT1	R/W	0h	Capture event 1 status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
0	INT	R/W	0h	Global interrupt clear flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the clear flag and enable further interrupts to be generated if any of the clear flags are set to 1

10 ECAP_ECFRC Register (Offset = 34h) [reset = X]

ECAP_ECFRC is shown in Figure 14-3463 and described in Table 14-7003.

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ECAP Interrupt Forcing Register.

Table 14-10464. ECAP_ECFRC Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 0034h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 0034h

Figure 14-3463. ECAP_ECFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
_RESV1							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	_RESV0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-10466. ECAP_ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	_RESV1	R	0h	
7	CMPEQ	R/W	0h	Force compare equal: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the the CMPEQ flag bit
6	PRDEQ	R/W	0h	Force period equal: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the PRDEQ flag bit
5	CNTOVF	R/W	0h	Force counter overflow: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CNTOVF flag bit
4	CEVT4	R/W	0h	Force capture event 4: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CEVT4 flag bit

Table 14-10466. ECAP_ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CEVT3	R/W	0h	Force capture event 3: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CEVT3 flag bit
2	CEVT2	R/W	0h	Force capture event 2: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CEVT2 flag bit
1	CEVT1	R/W	0h	Force capture event 1: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CEVT1 flag bit
0	_RESV0	R	0h	

11 ECAP_PID Register (Offset = 5Ch) [reset = 44D22100h]

ECAP_PID is shown in Figure 14-3464 and described in Table 14-7005.

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ECAP Peripheral Id Register.

Table 14-10467. ECAP_PID Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	3003 005Ch
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	300B 005Ch

Figure 14-3464. ECAP_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVID																															
R-44D22100h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10469. ECAP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVID	R	44D22100h	TI internal data.

14.3.6.1.7 PRU_ICSS_INTC_INTC Registers

Table 14-7007 lists the memory-mapped registers for the PRU_ICSS_INTC_INTC registers. All register offset addresses not listed in Table 14-7007 should be considered as reserved locations and the register contents should not be modified.

Table 14-10470. PRU_ICSS_INTC_INTC Instances

Instance	Base Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0000h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0000h

Table 14-10471. PRU_ICSS_INTC_INTC Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV Physical Address	PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV Physical Address
0h	ICSS_INTC_REVISION_REG	Revision Register	3002 0000h	300A 0000h
4h	ICSS_INTC_CONTROL_REG	Control Register	3002 0004h	300A 0004h
10h	ICSS_INTC_GLOBAL_ENABLE_HINT_REG	Global Host Int Enable Register	3002 0010h	300A 0010h
1Ch	ICSS_INTC_GLB_NEST_LEVEL_REG	Global Nesting Level Register	3002 001Ch	300A 001Ch
20h	ICSS_INTC_STATUS_SET_INDEX_REG	Status Set Index Register	3002 0020h	300A 0020h
24h	ICSS_INTC_STATUS_CLR_INDEX_REG	Status Clear Index Register	3002 0024h	300A 0024h
28h	ICSS_INTC_ENABLE_SET_INDEX_REG	Enable Set Index Register	3002 0028h	300A 0028h
2Ch	ICSS_INTC_ENABLE_CLR_INDEX_REG	Enable Clear Index Register	3002 002Ch	300A 002Ch
34h	ICSS_INTC_HINT_ENABLE_SET_INDEX_REG	Host Int Enable Set Index Register	3002 0034h	300A 0034h
38h	ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG	Host Int Enable Clear Index Register	3002 0038h	300A 0038h
80h	ICSS_INTC_GLB_PRI_INTR_REG	Global Prioritized Interrupt Register	3002 0080h	300A 0080h
200h	ICSS_INTC_RAW_STATUS_REG0	Raw Status Register 0	3002 0200h	300A 0200h
204h	ICSS_INTC_RAW_STATUS_REG1	Raw Status Register 1	3002 0204h	300A 0204h
208h	ICSS_INTC_RAW_STATUS_REG2	Raw Status Register 2	3002 0208h	300A 0208h
20Ch	ICSS_INTC_RAW_STATUS_REG3	Raw Status Register 3	3002 020Ch	300A 020Ch
210h	ICSS_INTC_RAW_STATUS_REG4	Raw Status Register 4	3002 0210h	300A 0210h
280h	ICSS_INTC_ENA_STATUS_REG0	Enabled Status Register 0	3002 0280h	300A 0280h
284h	ICSS_INTC_ENA_STATUS_REG1	Enabled Status Register 1	3002 0284h	300A 0284h
288h	ICSS_INTC_ENA_STATUS_REG2	Enabled Status Register 2	3002 0288h	300A 0288h
28Ch	ICSS_INTC_ENA_STATUS_REG3	Enabled Status Register 3	3002 028Ch	300A 028Ch
290h	ICSS_INTC_ENA_STATUS_REG4	Enabled Status Register 4	3002 0290h	300A 0290h
300h	ICSS_INTC_ENABLE_REG0	Enable Register 0	3002 0300h	300A 0300h
304h	ICSS_INTC_ENABLE_REG1	Enable Register 1	3002 0304h	300A 0304h
308h	ICSS_INTC_ENABLE_REG2	Enable Register 2	3002 0308h	300A 0308h
30Ch	ICSS_INTC_ENABLE_REG3	Enable Register 3	3002 030Ch	300A 030Ch
310h	ICSS_INTC_ENABLE_REG4	Enable Register 4	3002 0310h	300A 0310h
380h	ICSS_INTC_ENABLE_CLR_REG0	Enable Clear Register 0	3002 0380h	300A 0380h
384h	ICSS_INTC_ENABLE_CLR_REG1	Enable Clear Register 1	3002 0384h	300A 0384h
388h	ICSS_INTC_ENABLE_CLR_REG2	Enable Clear Register 2	3002 0388h	300A 0388h
38Ch	ICSS_INTC_ENABLE_CLR_REG3	Enable Clear Register 3	3002 038Ch	300A 038Ch
390h	ICSS_INTC_ENABLE_CLR_REG4	Enable Clear Register 4	3002 0390h	300A 0390h

Table 14-10471. PRU_ICSS_INTC_INTC Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV Physical Address	PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV Physical Address
400h	ICSS_INTC_CH_MAP_REG0	Interrupt Channel Map Register for 0 to 0+3	3002 0400h	300A 0400h
404h	ICSS_INTC_CH_MAP_REG1	Interrupt Channel Map Register for 4 to 4+3	3002 0404h	300A 0404h
408h	ICSS_INTC_CH_MAP_REG2	Interrupt Channel Map Register for 8 to 8+3	3002 0408h	300A 0408h
40Ch	ICSS_INTC_CH_MAP_REG3	Interrupt Channel Map Register for 12 to 12+3	3002 040Ch	300A 040Ch
410h	ICSS_INTC_CH_MAP_REG4	Interrupt Channel Map Register for 16 to 16+3	3002 0410h	300A 0410h
414h	ICSS_INTC_CH_MAP_REG5	Interrupt Channel Map Register for 20 to 20+3	3002 0414h	300A 0414h
418h	ICSS_INTC_CH_MAP_REG6	Interrupt Channel Map Register for 24 to 24+3	3002 0418h	300A 0418h
41Ch	ICSS_INTC_CH_MAP_REG7	Interrupt Channel Map Register for 28 to 28+3	3002 041Ch	300A 041Ch
420h	ICSS_INTC_CH_MAP_REG8	Interrupt Channel Map Register for 32 to 32+3	3002 0420h	300A 0420h
424h	ICSS_INTC_CH_MAP_REG9	Interrupt Channel Map Register for 36 to 36+3	3002 0424h	300A 0424h
428h	ICSS_INTC_CH_MAP_REG10	Interrupt Channel Map Register for 40 to 40+3	3002 0428h	300A 0428h
42Ch	ICSS_INTC_CH_MAP_REG11	Interrupt Channel Map Register for 44 to 44+3	3002 042Ch	300A 042Ch
430h	ICSS_INTC_CH_MAP_REG12	Interrupt Channel Map Register for 48 to 48+3	3002 0430h	300A 0430h
434h	ICSS_INTC_CH_MAP_REG13	Interrupt Channel Map Register for 52 to 52+3	3002 0434h	300A 0434h
438h	ICSS_INTC_CH_MAP_REG14	Interrupt Channel Map Register for 56 to 56+3	3002 0438h	300A 0438h
43Ch	ICSS_INTC_CH_MAP_REG15	Interrupt Channel Map Register for 60 to 60+3	3002 043Ch	300A 043Ch
440h	ICSS_INTC_CH_MAP_REG16	Interrupt Channel Map Register for 64 to 64+3	3002 0440h	300A 0440h
444h	ICSS_INTC_CH_MAP_REG17	Interrupt Channel Map Register for 68 to 68+3	3002 0444h	300A 0444h
448h	ICSS_INTC_CH_MAP_REG18	Interrupt Channel Map Register for 72 to 72+3	3002 0448h	300A 0448h
44Ch	ICSS_INTC_CH_MAP_REG19	Interrupt Channel Map Register for 76 to 76+3	3002 044Ch	300A 044Ch
450h	ICSS_INTC_CH_MAP_REG20	Interrupt Channel Map Register for 80 to 80+3	3002 0450h	300A 0450h
454h	ICSS_INTC_CH_MAP_REG21	Interrupt Channel Map Register for 84 to 84+3	3002 0454h	300A 0454h
458h	ICSS_INTC_CH_MAP_REG22	Interrupt Channel Map Register for 88 to 88+3	3002 0458h	300A 0458h
45Ch	ICSS_INTC_CH_MAP_REG23	Interrupt Channel Map Register for 92 to 92+3	3002 045Ch	300A 045Ch
460h	ICSS_INTC_CH_MAP_REG24	Interrupt Channel Map Register for 96 to 96+3	3002 0460h	300A 0460h

Table 14-10471. PRU_ICSS_INTC_INTC Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV Physical Address	PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV Physical Address
464h	ICSS_INTC_CH_MAP_REG25	Interrupt Channel Map Register for 100 to 100+3	3002 0464h	300A 0464h
468h	ICSS_INTC_CH_MAP_REG26	Interrupt Channel Map Register for 104 to 104+3	3002 0468h	300A 0468h
46Ch	ICSS_INTC_CH_MAP_REG27	Interrupt Channel Map Register for 108 to 108+3	3002 046Ch	300A 046Ch
470h	ICSS_INTC_CH_MAP_REG28	Interrupt Channel Map Register for 112 to 112+3	3002 0470h	300A 0470h
474h	ICSS_INTC_CH_MAP_REG29	Interrupt Channel Map Register for 116 to 116+3	3002 0474h	300A 0474h
478h	ICSS_INTC_CH_MAP_REG30	Interrupt Channel Map Register for 120 to 120+3	3002 0478h	300A 0478h
47Ch	ICSS_INTC_CH_MAP_REG31	Interrupt Channel Map Register for 124 to 124+3	3002 047Ch	300A 047Ch
480h	ICSS_INTC_CH_MAP_REG32	Interrupt Channel Map Register for 128 to 128+3	3002 0480h	300A 0480h
484h	ICSS_INTC_CH_MAP_REG33	Interrupt Channel Map Register for 132 to 132+3	3002 0484h	300A 0484h
488h	ICSS_INTC_CH_MAP_REG34	Interrupt Channel Map Register for 136 to 136+3	3002 0488h	300A 0488h
48Ch	ICSS_INTC_CH_MAP_REG35	Interrupt Channel Map Register for 140 to 140+3	3002 048Ch	300A 048Ch
490h	ICSS_INTC_CH_MAP_REG36	Interrupt Channel Map Register for 144 to 144+3	3002 0490h	300A 0490h
494h	ICSS_INTC_CH_MAP_REG37	Interrupt Channel Map Register for 148 to 148+3	3002 0494h	300A 0494h
498h	ICSS_INTC_CH_MAP_REG38	Interrupt Channel Map Register for 152 to 152+3	3002 0498h	300A 0498h
49Ch	ICSS_INTC_CH_MAP_REG39	Interrupt Channel Map Register for 156 to 156+3	3002 049Ch	300A 049Ch
800h	ICSS_INTC_HINT_MAP_REG0	Host Interrupt Map Register for 0 to 0+3	3002 0800h	300A 0800h
804h	ICSS_INTC_HINT_MAP_REG1	Host Interrupt Map Register for 4 to 4+3	3002 0804h	300A 0804h
808h	ICSS_INTC_HINT_MAP_REG2	Host Interrupt Map Register for 8 to 8+3	3002 0808h	300A 0808h
80Ch	ICSS_INTC_HINT_MAP_REG3	Host Interrupt Map Register for 12 to 12+3	3002 080Ch	300A 080Ch
810h	ICSS_INTC_HINT_MAP_REG4	Host Interrupt Map Register for 16 to 16+4	3002 0810h	300A 0810h
900h	ICSS_INTC_PRI_HINT_REG0	Host Int 0 Prioritized Interrupt Register	3002 0900h	300A 0900h
904h	ICSS_INTC_PRI_HINT_REG1	Host Int 1 Prioritized Interrupt Register	3002 0904h	300A 0904h
908h	ICSS_INTC_PRI_HINT_REG2	Host Int 2 Prioritized Interrupt Register	3002 0908h	300A 0908h
90Ch	ICSS_INTC_PRI_HINT_REG3	Host Int 3 Prioritized Interrupt Register	3002 090Ch	300A 090Ch
910h	ICSS_INTC_PRI_HINT_REG4	Host Int 4 Prioritized Interrupt Register	3002 0910h	300A 0910h
914h	ICSS_INTC_PRI_HINT_REG5	Host Int 5 Prioritized Interrupt Register	3002 0914h	300A 0914h
918h	ICSS_INTC_PRI_HINT_REG6	Host Int 6 Prioritized Interrupt Register	3002 0918h	300A 0918h
91Ch	ICSS_INTC_PRI_HINT_REG7	Host Int 7 Prioritized Interrupt Register	3002 091Ch	300A 091Ch
920h	ICSS_INTC_PRI_HINT_REG8	Host Int 8 Prioritized Interrupt Register	3002 0920h	300A 0920h
924h	ICSS_INTC_PRI_HINT_REG9	Host Int 9 Prioritized Interrupt Register	3002 0924h	300A 0924h
928h	ICSS_INTC_PRI_HINT_REG10	Host Int 10 Prioritized Interrupt Register	3002 0928h	300A 0928h

Table 14-10471. PRU_ICSS_INTC_INTC Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV Physical Address	PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV Physical Address
92Ch	ICSS_INTC_PRI_HINT_REG11	Host Int 11 Prioritized Interrupt Register	3002 092Ch	300A 092Ch
930h	ICSS_INTC_PRI_HINT_REG12	Host Int 12 Prioritized Interrupt Register	3002 0930h	300A 0930h
934h	ICSS_INTC_PRI_HINT_REG13	Host Int 13 Prioritized Interrupt Register	3002 0934h	300A 0934h
938h	ICSS_INTC_PRI_HINT_REG14	Host Int 14 Prioritized Interrupt Register	3002 0938h	300A 0938h
93Ch	ICSS_INTC_PRI_HINT_REG15	Host Int 15 Prioritized Interrupt Register	3002 093Ch	300A 093Ch
940h	ICSS_INTC_PRI_HINT_REG16	Host Int 16 Prioritized Interrupt Register	3002 0940h	300A 0940h
944h	ICSS_INTC_PRI_HINT_REG17	Host Int 17 Prioritized Interrupt Register	3002 0944h	300A 0944h
948h	ICSS_INTC_PRI_HINT_REG18	Host Int 18 Prioritized Interrupt Register	3002 0948h	300A 0948h
94Ch	ICSS_INTC_PRI_HINT_REG19	Host Int 19 Prioritized Interrupt Register	3002 094Ch	300A 094Ch
D00h	ICSS_INTC_POLARITY_REG0	Polarity Register 0	3002 0D00h	300A 0D00h
D04h	ICSS_INTC_POLARITY_REG1	Polarity Register 1	3002 0D04h	300A 0D04h
D08h	ICSS_INTC_POLARITY_REG2	Polarity Register 2	3002 0D08h	300A 0D08h
D0Ch	ICSS_INTC_POLARITY_REG3	Polarity Register 3	3002 0D0Ch	300A 0D0Ch
D10h	ICSS_INTC_POLARITY_REG4	Polarity Register 4	3002 0D10h	300A 0D10h
D80h	ICSS_INTC_TYPE_REG0	Type Register 0	3002 0D80h	300A 0D80h
D84h	ICSS_INTC_TYPE_REG1	Type Register 1	3002 0D84h	300A 0D84h
D88h	ICSS_INTC_TYPE_REG2	Type Register 2	3002 0D88h	300A 0D88h
D8Ch	ICSS_INTC_TYPE_REG3	Type Register 3	3002 0D8Ch	300A 0D8Ch
D90h	ICSS_INTC_TYPE_REG4	Type Register 4	3002 0D90h	300A 0D90h
1100h	ICSS_INTC_NEST_LEVEL_REG0	Host Int 0 Nesting Level Register	3002 1100h	300A 1100h
1104h	ICSS_INTC_NEST_LEVEL_REG1	Host Int 1 Nesting Level Register	3002 1104h	300A 1104h
1108h	ICSS_INTC_NEST_LEVEL_REG2	Host Int 2 Nesting Level Register	3002 1108h	300A 1108h
110Ch	ICSS_INTC_NEST_LEVEL_REG3	Host Int 3 Nesting Level Register	3002 110Ch	300A 110Ch
1110h	ICSS_INTC_NEST_LEVEL_REG4	Host Int 4 Nesting Level Register	3002 1110h	300A 1110h
1114h	ICSS_INTC_NEST_LEVEL_REG5	Host Int 5 Nesting Level Register	3002 1114h	300A 1114h
1118h	ICSS_INTC_NEST_LEVEL_REG6	Host Int 6 Nesting Level Register	3002 1118h	300A 1118h
111Ch	ICSS_INTC_NEST_LEVEL_REG7	Host Int 7 Nesting Level Register	3002 111Ch	300A 111Ch
1120h	ICSS_INTC_NEST_LEVEL_REG8	Host Int 8 Nesting Level Register	3002 1120h	300A 1120h
1124h	ICSS_INTC_NEST_LEVEL_REG9	Host Int 9 Nesting Level Register	3002 1124h	300A 1124h
1128h	ICSS_INTC_NEST_LEVEL_REG10	Host Int 10 Nesting Level Register	3002 1128h	300A 1128h
112Ch	ICSS_INTC_NEST_LEVEL_REG11	Host Int 11 Nesting Level Register	3002 112Ch	300A 112Ch
1130h	ICSS_INTC_NEST_LEVEL_REG12	Host Int 12 Nesting Level Register	3002 1130h	300A 1130h
1134h	ICSS_INTC_NEST_LEVEL_REG13	Host Int 13 Nesting Level Register	3002 1134h	300A 1134h
1138h	ICSS_INTC_NEST_LEVEL_REG14	Host Int 14 Nesting Level Register	3002 1138h	300A 1138h
113Ch	ICSS_INTC_NEST_LEVEL_REG15	Host Int 15 Nesting Level Register	3002 113Ch	300A 113Ch
1140h	ICSS_INTC_NEST_LEVEL_REG16	Host Int 16 Nesting Level Register	3002 1140h	300A 1140h
1144h	ICSS_INTC_NEST_LEVEL_REG17	Host Int 17 Nesting Level Register	3002 1144h	300A 1144h
1148h	ICSS_INTC_NEST_LEVEL_REG18	Host Int 18 Nesting Level Register	3002 1148h	300A 1148h
114Ch	ICSS_INTC_NEST_LEVEL_REG19	Host Int 19 Nesting Level Register	3002 114Ch	300A 114Ch
1500h	ICSS_INTC_ENABLE_HINT_REG0	Host Int Enable Register 0	3002 1500h	300A 1500h

1 ICSS_INTC_REVISION_REG Register (Offset = 0h) [reset = X]

ICSS_INTC_REVISION_REG is shown in Figure 14-3465 and described in Table 14-7009.

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Revision Register

Table 14-10472. ICSS_INTC_REVISION_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0000h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0000h

Figure 14-3465. ICSS_INTC_REVISION_REG Register

31	30	29	28	27	26	25	24
REV_SCHEME		RESERVED		REV_MODULE			
R-1h		R-X		R-E82h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REV_MODULE							
R-E82h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REV_RTL					REV_MAJOR		
R-15h					R-1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REV_CUSTOM		REV_MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10474. ICSS_INTC_REVISION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	REV_SCHEME	R	1h	Scheme
29-28	RESERVED	R	X	
27-16	REV_MODULE	R	E82h	Module ID
15-11	REV_RTL	R	15h	RTL revisions
10-8	REV_MAJOR	R	1h	Major revision
7-6	REV_CUSTOM	R	0h	Custom revision
5-0	REV_MINOR	R	0h	Minor revision

2 ICSS_INTC_CONTROL_REG Register (Offset = 4h) [reset = X]

ICSS_INTC_CONTROL_REG is shown in Figure 14-3466 and described in Table 14-7011.

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Control Register

Table 14-10475. ICSS_INTC_CONTROL_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0004h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0004h

Figure 14-3466. ICSS_INTC_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRIORITY_HOLD_MODE	NEST_MODE		WAKEUP_MODE	RESERVED
R/W-X			R/W-0h	R/W-0h		R/W-0h	R/W-X

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10477. ICSS_INTC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	PRIORITY_HOLD_MODE	R/W	0h	Priority Holding Mode
3-2	NEST_MODE	R/W	0h	Nesting Mode
1	WAKEUP_MODE	R/W	0h	Wakeup mode enable
0	RESERVED	R/W	X	

3 ICSS_INTC_GLOBAL_ENABLE_HINT_REG Register (Offset = 10h) [reset = X]

ICSS_INTC_GLOBAL_ENABLE_HINT_REG is shown in Figure 14-3467 and described in Table 14-7013.

Return to Summary Table.

Global Host Int Enable Register

Table 14-10478. ICSS_INTC_GLOBAL_ENABLE_HINT_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0010h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0010h

Figure 14-3467. ICSS_INTC_GLOBAL_ENABLE_HINT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_HINT_ANY
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10480. ICSS_INTC_GLOBAL_ENABLE_HINT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_HINT_ANY	R/W	0h	Global Enable for all Host Interrupts

4 ICSS_INTC_GLB_NEST_LEVEL_REG Register (Offset = 1Ch) [reset = X]

ICSS_INTC_GLB_NEST_LEVEL_REG is shown in Figure 14-3468 and described in Table 14-7015.

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Global Nesting Level Register

Table 14-10481. ICSS_INTC_GLB_NEST_LEVEL_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 001Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 001Ch

Figure 14-3468. ICSS_INTC_GLB_NEST_LEVEL_REG Register

31	30	29	28	27	26	25	24
GLB_NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							GLB_NEST_LEVEL
R/W-X							R/W-100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GLB_NEST_LEVEL							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10483. ICSS_INTC_GLB_NEST_LEVEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GLB_NEST_AUTO_OVR	W	X	Global Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	GLB_NEST_LEVEL	R/W	100h	Global Nesting Level

5 ICSS_INTC_STATUS_SET_INDEX_REG Register (Offset = 20h) [reset = X]

ICSS_INTC_STATUS_SET_INDEX_REG is shown in Figure 14-3469 and described in Table 14-7017.

Return to Summary Table.

Status Set Index Register

Table 14-10484. ICSS_INTC_STATUS_SET_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0020h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0020h

Figure 14-3469. ICSS_INTC_STATUS_SET_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						STATUS_SET_INDEX									
W-X						W-0h									

LEGEND: W = Write Only; -*n* = value after reset

Table 14-10486. ICSS_INTC_STATUS_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	STATUS_SET_INDEX	W	0h	Status Set Index Register (write index to set status)

6 ICSS_INTC_STATUS_CLR_INDEX_REG Register (Offset = 24h) [reset = X]

ICSS_INTC_STATUS_CLR_INDEX_REG is shown in Figure 14-3470 and described in Table 14-7019.

Return to Summary Table.

Status Clear Index Register

Table 14-10487. ICSS_INTC_STATUS_CLR_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0024h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0024h

Figure 14-3470. ICSS_INTC_STATUS_CLR_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						STATUS_CLR_INDEX									
W-X						W-0h									

LEGEND: W = Write Only; -*n* = value after reset

Table 14-10489. ICSS_INTC_STATUS_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	STATUS_CLR_INDEX	W	0h	Status Clear Index Register (write index to clear status of)

7 ICSS_INTC_ENABLE_SET_INDEX_REG Register (Offset = 28h) [reset = X]

ICSS_INTC_ENABLE_SET_INDEX_REG is shown in Figure 14-3471 and described in Table 14-7021.

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Enable Set Index Register

Table 14-10490. ICSS_INTC_ENABLE_SET_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0028h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0028h

Figure 14-3471. ICSS_INTC_ENABLE_SET_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ENABLE_SET_INDEX									
W-X						W1S-0h									

LEGEND: W = Write Only; W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-10492. ICSS_INTC_ENABLE_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	ENABLE_SET_INDEX	W1S	0h	Enable Set Index Register (write index to set enable of)

8 ICSS_INTC_ENABLE_CLR_INDEX_REG Register (Offset = 2Ch) [reset = X]

ICSS_INTC_ENABLE_CLR_INDEX_REG is shown in Figure 14-3472 and described in Table 14-7023.

Return to Summary Table.

Enable Clear Index Register

Table 14-10493. ICSS_INTC_ENABLE_CLR_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 002Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 002Ch

Figure 14-3472. ICSS_INTC_ENABLE_CLR_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ENABLE_CLR_INDEX									
W-X						W1C-0h									

LEGEND: W = Write Only; W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 14-10495. ICSS_INTC_ENABLE_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	ENABLE_CLR_INDEX	W1C	0h	Enable Clear Index Register (write index to clear enable of)

9 ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Register (Offset = 34h) [reset = X]

ICSS_INTC_HINT_ENABLE_SET_INDEX_REG is shown in Figure 14-3473 and described in Table 14-7025.

Return to Summary Table.

Host Int Enable Set Index Register

Table 14-10496. ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0034h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0034h

Figure 14-3473. ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						HINT_ENABLE_SET_INDEX									
W-X						W1S-0h									

LEGEND: W = Write Only; W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-10498. ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	HINT_ENABLE_SET_INDEX	W1S	0h	Enable SET for Host Interrupts

10 ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Register (Offset = 38h) [reset = X]

ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG is shown in Figure 14-3474 and described in Table 14-7027.

Return to Summary Table.

Host Int Enable Clear Index Register

Table 14-10499. ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0038h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0038h

Figure 14-3474. ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						HINT_ENABLE_CLR_INDEX									
W-X						W1C-0h									

LEGEND: W = Write Only; W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 14-10501. ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	HINT_ENABLE_CLR_INDEX	W1C	0h	Enable CLEAR for Host Interrupts

11 ICSS_INTC_GLB_PRI_INTR_REG Register (Offset = 80h) [reset = X]

ICSS_INTC_GLB_PRI_INTR_REG is shown in Figure 14-3475 and described in Table 14-7029.

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Global Prioritized Interrupt Register

Table 14-10502. ICSS_INTC_GLB_PRI_INTR_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0080h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0080h

Figure 14-3475. ICSS_INTC_GLB_PRI_INTR_REG Register

31	30	29	28	27	26	25	24
GLB_NONE	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						GLB_PRI_INTR	
R-X						R-0h	
7	6	5	4	3	2	1	0
GLB_PRI_INTR							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10504. ICSS_INTC_GLB_PRI_INTR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GLB_NONE	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	GLB_PRI_INTR	R	0h	Prioritized Interrupt

12 ICSS_INTC_RAW_STATUS_REG0 Register (Offset = 200h) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG0 is shown in Figure 14-3476 and described in Table 14-7031.

Return to Summary Table.

Raw Status Register 0

Table 14-10505. ICSS_INTC_RAW_STATUS_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0200h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0200h

Figure 14-3476. ICSS_INTC_RAW_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RAW_STATUS_31	RAW_STATUS_30	RAW_STATUS_29	RAW_STATUS_28	RAW_STATUS_27	RAW_STATUS_26	RAW_STATUS_25	RAW_STATUS_24
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_23	RAW_STATUS_22	RAW_STATUS_21	RAW_STATUS_20	RAW_STATUS_19	RAW_STATUS_18	RAW_STATUS_17	RAW_STATUS_16
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_15	RAW_STATUS_14	RAW_STATUS_13	RAW_STATUS_12	RAW_STATUS_11	RAW_STATUS_10	RAW_STATUS_9	RAW_STATUS_8
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_7	RAW_STATUS_6	RAW_STATUS_5	RAW_STATUS_4	RAW_STATUS_3	RAW_STATUS_2	RAW_STATUS_1	RAW_STATUS_0
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; *-n* = value after reset

Table 14-10507. ICSS_INTC_RAW_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_31	W1S	0h	Raw Status (write 1 to set) for intr_in[31]
30	RAW_STATUS_30	W1S	0h	Raw Status (write 1 to set) for intr_in[30]
29	RAW_STATUS_29	W1S	0h	Raw Status (write 1 to set) for intr_in[29]
28	RAW_STATUS_28	W1S	0h	Raw Status (write 1 to set) for intr_in[28]
27	RAW_STATUS_27	W1S	0h	Raw Status (write 1 to set) for intr_in[27]
26	RAW_STATUS_26	W1S	0h	Raw Status (write 1 to set) for intr_in[26]
25	RAW_STATUS_25	W1S	0h	Raw Status (write 1 to set) for intr_in[25]
24	RAW_STATUS_24	W1S	0h	Raw Status (write 1 to set) for intr_in[24]
23	RAW_STATUS_23	W1S	0h	Raw Status (write 1 to set) for intr_in[23]
22	RAW_STATUS_22	W1S	0h	Raw Status (write 1 to set) for intr_in[22]
21	RAW_STATUS_21	W1S	0h	Raw Status (write 1 to set) for intr_in[21]
20	RAW_STATUS_20	W1S	0h	Raw Status (write 1 to set) for intr_in[20]
19	RAW_STATUS_19	W1S	0h	Raw Status (write 1 to set) for intr_in[19]
18	RAW_STATUS_18	W1S	0h	Raw Status (write 1 to set) for intr_in[18]
17	RAW_STATUS_17	W1S	0h	Raw Status (write 1 to set) for intr_in[17]
16	RAW_STATUS_16	W1S	0h	Raw Status (write 1 to set) for intr_in[16]

Table 14-10507. ICSS_INTC_RAW_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RAW_STATUS_15	W1S	0h	Raw Status (write 1 to set) for intr_in[15]
14	RAW_STATUS_14	W1S	0h	Raw Status (write 1 to set) for intr_in[14]
13	RAW_STATUS_13	W1S	0h	Raw Status (write 1 to set) for intr_in[13]
12	RAW_STATUS_12	W1S	0h	Raw Status (write 1 to set) for intr_in[12]
11	RAW_STATUS_11	W1S	0h	Raw Status (write 1 to set) for intr_in[11]
10	RAW_STATUS_10	W1S	0h	Raw Status (write 1 to set) for intr_in[10]
9	RAW_STATUS_9	W1S	0h	Raw Status (write 1 to set) for intr_in[9]
8	RAW_STATUS_8	W1S	0h	Raw Status (write 1 to set) for intr_in[8]
7	RAW_STATUS_7	W1S	0h	Raw Status (write 1 to set) for intr_in[7]
6	RAW_STATUS_6	W1S	0h	Raw Status (write 1 to set) for intr_in[6]
5	RAW_STATUS_5	W1S	0h	Raw Status (write 1 to set) for intr_in[5]
4	RAW_STATUS_4	W1S	0h	Raw Status (write 1 to set) for intr_in[4]
3	RAW_STATUS_3	W1S	0h	Raw Status (write 1 to set) for intr_in[3]
2	RAW_STATUS_2	W1S	0h	Raw Status (write 1 to set) for intr_in[2]
1	RAW_STATUS_1	W1S	0h	Raw Status (write 1 to set) for intr_in[1]
0	RAW_STATUS_0	W1S	0h	Raw Status (write 1 to set) for intr_in[0]

13 ICSS_INTC_RAW_STATUS_REG1 Register (Offset = 204h) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG1 is shown in Figure 14-3477 and described in Table 14-7033.

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Raw Status Register 1

Table 14-10508. ICSS_INTC_RAW_STATUS_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0204h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0204h

Figure 14-3477. ICSS_INTC_RAW_STATUS_REG1 Register

31	30	29	28	27	26	25	24
RAW_STATUS_63	RAW_STATUS_62	RAW_STATUS_61	RAW_STATUS_60	RAW_STATUS_59	RAW_STATUS_58	RAW_STATUS_57	RAW_STATUS_56
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_55	RAW_STATUS_54	RAW_STATUS_53	RAW_STATUS_52	RAW_STATUS_51	RAW_STATUS_50	RAW_STATUS_49	RAW_STATUS_48
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_47	RAW_STATUS_46	RAW_STATUS_45	RAW_STATUS_44	RAW_STATUS_43	RAW_STATUS_42	RAW_STATUS_41	RAW_STATUS_40
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_39	RAW_STATUS_38	RAW_STATUS_37	RAW_STATUS_36	RAW_STATUS_35	RAW_STATUS_34	RAW_STATUS_33	RAW_STATUS_32
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; *-n* = value after reset

Table 14-10510. ICSS_INTC_RAW_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_63	W1S	0h	Raw Status (write 1 to set) for intr_in[63]
30	RAW_STATUS_62	W1S	0h	Raw Status (write 1 to set) for intr_in[62]
29	RAW_STATUS_61	W1S	0h	Raw Status (write 1 to set) for intr_in[61]
28	RAW_STATUS_60	W1S	0h	Raw Status (write 1 to set) for intr_in[60]
27	RAW_STATUS_59	W1S	0h	Raw Status (write 1 to set) for intr_in[59]
26	RAW_STATUS_58	W1S	0h	Raw Status (write 1 to set) for intr_in[58]
25	RAW_STATUS_57	W1S	0h	Raw Status (write 1 to set) for intr_in[57]
24	RAW_STATUS_56	W1S	0h	Raw Status (write 1 to set) for intr_in[56]
23	RAW_STATUS_55	W1S	0h	Raw Status (write 1 to set) for intr_in[55]
22	RAW_STATUS_54	W1S	0h	Raw Status (write 1 to set) for intr_in[54]
21	RAW_STATUS_53	W1S	0h	Raw Status (write 1 to set) for intr_in[53]
20	RAW_STATUS_52	W1S	0h	Raw Status (write 1 to set) for intr_in[52]
19	RAW_STATUS_51	W1S	0h	Raw Status (write 1 to set) for intr_in[51]
18	RAW_STATUS_50	W1S	0h	Raw Status (write 1 to set) for intr_in[50]
17	RAW_STATUS_49	W1S	0h	Raw Status (write 1 to set) for intr_in[49]
16	RAW_STATUS_48	W1S	0h	Raw Status (write 1 to set) for intr_in[48]

Table 14-10510. ICSS_INTC_RAW_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RAW_STATUS_47	W1S	0h	Raw Status (write 1 to set) for intr_in[47]
14	RAW_STATUS_46	W1S	0h	Raw Status (write 1 to set) for intr_in[46]
13	RAW_STATUS_45	W1S	0h	Raw Status (write 1 to set) for intr_in[45]
12	RAW_STATUS_44	W1S	0h	Raw Status (write 1 to set) for intr_in[44]
11	RAW_STATUS_43	W1S	0h	Raw Status (write 1 to set) for intr_in[43]
10	RAW_STATUS_42	W1S	0h	Raw Status (write 1 to set) for intr_in[42]
9	RAW_STATUS_41	W1S	0h	Raw Status (write 1 to set) for intr_in[41]
8	RAW_STATUS_40	W1S	0h	Raw Status (write 1 to set) for intr_in[40]
7	RAW_STATUS_39	W1S	0h	Raw Status (write 1 to set) for intr_in[39]
6	RAW_STATUS_38	W1S	0h	Raw Status (write 1 to set) for intr_in[38]
5	RAW_STATUS_37	W1S	0h	Raw Status (write 1 to set) for intr_in[37]
4	RAW_STATUS_36	W1S	0h	Raw Status (write 1 to set) for intr_in[36]
3	RAW_STATUS_35	W1S	0h	Raw Status (write 1 to set) for intr_in[35]
2	RAW_STATUS_34	W1S	0h	Raw Status (write 1 to set) for intr_in[34]
1	RAW_STATUS_33	W1S	0h	Raw Status (write 1 to set) for intr_in[33]
0	RAW_STATUS_32	W1S	0h	Raw Status (write 1 to set) for intr_in[32]

14 ICSS_INTC_RAW_STATUS_REG2 Register (Offset = 208h) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG2 is shown in Figure 14-3478 and described in Table 14-7035.

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Raw Status Register 2

Table 14-10511. ICSS_INTC_RAW_STATUS_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0208h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0208h

Figure 14-3478. ICSS_INTC_RAW_STATUS_REG2 Register

31	30	29	28	27	26	25	24
RAW_STATUS_95	RAW_STATUS_94	RAW_STATUS_93	RAW_STATUS_92	RAW_STATUS_91	RAW_STATUS_90	RAW_STATUS_89	RAW_STATUS_88
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_87	RAW_STATUS_86	RAW_STATUS_85	RAW_STATUS_84	RAW_STATUS_83	RAW_STATUS_82	RAW_STATUS_81	RAW_STATUS_80
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_79	RAW_STATUS_78	RAW_STATUS_77	RAW_STATUS_76	RAW_STATUS_75	RAW_STATUS_74	RAW_STATUS_73	RAW_STATUS_72
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_71	RAW_STATUS_70	RAW_STATUS_69	RAW_STATUS_68	RAW_STATUS_67	RAW_STATUS_66	RAW_STATUS_65	RAW_STATUS_64
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; *-n* = value after reset

Table 14-10513. ICSS_INTC_RAW_STATUS_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_95	W1S	0h	Raw Status (write 1 to set) for slv_events_in[31]
30	RAW_STATUS_94	W1S	0h	Raw Status (write 1 to set) for slv_events_in[30]
29	RAW_STATUS_93	W1S	0h	Raw Status (write 1 to set) for slv_events_in[29]
28	RAW_STATUS_92	W1S	0h	Raw Status (write 1 to set) for slv_events_in[28]
27	RAW_STATUS_91	W1S	0h	Raw Status (write 1 to set) for slv_events_in[27]
26	RAW_STATUS_90	W1S	0h	Raw Status (write 1 to set) for slv_events_in[26]
25	RAW_STATUS_89	W1S	0h	Raw Status (write 1 to set) for slv_events_in[25]
24	RAW_STATUS_88	W1S	0h	Raw Status (write 1 to set) for slv_events_in[24]
23	RAW_STATUS_87	W1S	0h	Raw Status (write 1 to set) for slv_events_in[23]
22	RAW_STATUS_86	W1S	0h	Raw Status (write 1 to set) for slv_events_in[22]
21	RAW_STATUS_85	W1S	0h	Raw Status (write 1 to set) for slv_events_in[21]
20	RAW_STATUS_84	W1S	0h	Raw Status (write 1 to set) for slv_events_in[20]
19	RAW_STATUS_83	W1S	0h	Raw Status (write 1 to set) for slv_events_in[19]
18	RAW_STATUS_82	W1S	0h	Raw Status (write 1 to set) for slv_events_in[18]
17	RAW_STATUS_81	W1S	0h	Raw Status (write 1 to set) for slv_events_in[17]
16	RAW_STATUS_80	W1S	0h	Raw Status (write 1 to set) for slv_events_in[16]

Table 14-10513. ICSS_INTC_RAW_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RAW_STATUS_79	W1S	0h	Raw Status (write 1 to set) for slv_events_in[15]
14	RAW_STATUS_78	W1S	0h	Raw Status (write 1 to set) for slv_events_in[14]
13	RAW_STATUS_77	W1S	0h	Raw Status (write 1 to set) for slv_events_in[13]
12	RAW_STATUS_76	W1S	0h	Raw Status (write 1 to set) for slv_events_in[12]
11	RAW_STATUS_75	W1S	0h	Raw Status (write 1 to set) for slv_events_in[11]
10	RAW_STATUS_74	W1S	0h	Raw Status (write 1 to set) for slv_events_in[10]
9	RAW_STATUS_73	W1S	0h	Raw Status (write 1 to set) for slv_events_in[9]
8	RAW_STATUS_72	W1S	0h	Raw Status (write 1 to set) for slv_events_in[8]
7	RAW_STATUS_71	W1S	0h	Raw Status (write 1 to set) for slv_events_in[7]
6	RAW_STATUS_70	W1S	0h	Raw Status (write 1 to set) for slv_events_in[6]
5	RAW_STATUS_69	W1S	0h	Raw Status (write 1 to set) for slv_events_in[5]
4	RAW_STATUS_68	W1S	0h	Raw Status (write 1 to set) for slv_events_in[4]
3	RAW_STATUS_67	W1S	0h	Raw Status (write 1 to set) for slv_events_in[3]
2	RAW_STATUS_66	W1S	0h	Raw Status (write 1 to set) for slv_events_in[2]
1	RAW_STATUS_65	W1S	0h	Raw Status (write 1 to set) for slv_events_in[1]
0	RAW_STATUS_64	W1S	0h	Raw Status (write 1 to set) for slv_events_in[0]

15 ICSS_INTC_RAW_STATUS_REG3 Register (Offset = 20Ch) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG3 is shown in Figure 14-3479 and described in Table 14-7037.

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Raw Status Register 3

Table 14-10514. ICSS_INTC_RAW_STATUS_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 020Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 020Ch

Figure 14-3479. ICSS_INTC_RAW_STATUS_REG3 Register

31	30	29	28	27	26	25	24
RAW_STATUS_127	RAW_STATUS_126	RAW_STATUS_125	RAW_STATUS_124	RAW_STATUS_123	RAW_STATUS_122	RAW_STATUS_121	RAW_STATUS_120
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_119	RAW_STATUS_118	RAW_STATUS_117	RAW_STATUS_116	RAW_STATUS_115	RAW_STATUS_114	RAW_STATUS_113	RAW_STATUS_112
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_111	RAW_STATUS_110	RAW_STATUS_109	RAW_STATUS_108	RAW_STATUS_107	RAW_STATUS_106	RAW_STATUS_105	RAW_STATUS_104
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_103	RAW_STATUS_102	RAW_STATUS_101	RAW_STATUS_100	RAW_STATUS_99	RAW_STATUS_98	RAW_STATUS_97	RAW_STATUS_96
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; *-n* = value after reset

Table 14-10516. ICSS_INTC_RAW_STATUS_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_127	W1S	0h	Raw Status (write 1 to set) for slv_events_in[63]
30	RAW_STATUS_126	W1S	0h	Raw Status (write 1 to set) for slv_events_in[62]
29	RAW_STATUS_125	W1S	0h	Raw Status (write 1 to set) for slv_events_in[61]
28	RAW_STATUS_124	W1S	0h	Raw Status (write 1 to set) for slv_events_in[60]
27	RAW_STATUS_123	W1S	0h	Raw Status (write 1 to set) for slv_events_in[59]
26	RAW_STATUS_122	W1S	0h	Raw Status (write 1 to set) for slv_events_in[58]
25	RAW_STATUS_121	W1S	0h	Raw Status (write 1 to set) for slv_events_in[57]
24	RAW_STATUS_120	W1S	0h	Raw Status (write 1 to set) for slv_events_in[56]
23	RAW_STATUS_119	W1S	0h	Raw Status (write 1 to set) for slv_events_in[55]
22	RAW_STATUS_118	W1S	0h	Raw Status (write 1 to set) for slv_events_in[54]
21	RAW_STATUS_117	W1S	0h	Raw Status (write 1 to set) for slv_events_in[53]
20	RAW_STATUS_116	W1S	0h	Raw Status (write 1 to set) for slv_events_in[52]
19	RAW_STATUS_115	W1S	0h	Raw Status (write 1 to set) for slv_events_in[51]
18	RAW_STATUS_114	W1S	0h	Raw Status (write 1 to set) for slv_events_in[50]
17	RAW_STATUS_113	W1S	0h	Raw Status (write 1 to set) for slv_events_in[49]
16	RAW_STATUS_112	W1S	0h	Raw Status (write 1 to set) for slv_events_in[48]

Table 14-10516. ICSS_INTC_RAW_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RAW_STATUS_111	W1S	0h	Raw Status (write 1 to set) for slv_events_in[47]
14	RAW_STATUS_110	W1S	0h	Raw Status (write 1 to set) for slv_events_in[46]
13	RAW_STATUS_109	W1S	0h	Raw Status (write 1 to set) for slv_events_in[45]
12	RAW_STATUS_108	W1S	0h	Raw Status (write 1 to set) for slv_events_in[44]
11	RAW_STATUS_107	W1S	0h	Raw Status (write 1 to set) for slv_events_in[43]
10	RAW_STATUS_106	W1S	0h	Raw Status (write 1 to set) for slv_events_in[42]
9	RAW_STATUS_105	W1S	0h	Raw Status (write 1 to set) for slv_events_in[41]
8	RAW_STATUS_104	W1S	0h	Raw Status (write 1 to set) for slv_events_in[40]
7	RAW_STATUS_103	W1S	0h	Raw Status (write 1 to set) for slv_events_in[39]
6	RAW_STATUS_102	W1S	0h	Raw Status (write 1 to set) for slv_events_in[38]
5	RAW_STATUS_101	W1S	0h	Raw Status (write 1 to set) for slv_events_in[37]
4	RAW_STATUS_100	W1S	0h	Raw Status (write 1 to set) for slv_events_in[36]
3	RAW_STATUS_99	W1S	0h	Raw Status (write 1 to set) for slv_events_in[35]
2	RAW_STATUS_98	W1S	0h	Raw Status (write 1 to set) for slv_events_in[34]
1	RAW_STATUS_97	W1S	0h	Raw Status (write 1 to set) for slv_events_in[33]
0	RAW_STATUS_96	W1S	0h	Raw Status (write 1 to set) for slv_events_in[32]

16 ICSS_INTC_RAW_STATUS_REG4 Register (Offset = 210h) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG4 is shown in Figure 14-3480 and described in Table 14-7039.

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Raw Status Register 4

Table 14-10517. ICSS_INTC_RAW_STATUS_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0210h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0210h

Figure 14-3480. ICSS_INTC_RAW_STATUS_REG4 Register

31	30	29	28	27	26	25	24
RAW_STATUS_159	RAW_STATUS_158	RAW_STATUS_157	RAW_STATUS_156	RAW_STATUS_155	RAW_STATUS_154	RAW_STATUS_153	RAW_STATUS_152
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_151	RAW_STATUS_150	RAW_STATUS_149	RAW_STATUS_148	RAW_STATUS_147	RAW_STATUS_146	RAW_STATUS_145	RAW_STATUS_144
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_143	RAW_STATUS_142	RAW_STATUS_141	RAW_STATUS_140	RAW_STATUS_139	RAW_STATUS_138	RAW_STATUS_137	RAW_STATUS_136
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_135	RAW_STATUS_134	RAW_STATUS_133	RAW_STATUS_132	RAW_STATUS_131	RAW_STATUS_130	RAW_STATUS_129	RAW_STATUS_128
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; *-n* = value after reset

Table 14-10519. ICSS_INTC_RAW_STATUS_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_159	W1S	0h	Raw Status (write 1 to set) for slv_events_in[95]
30	RAW_STATUS_158	W1S	0h	Raw Status (write 1 to set) for slv_events_in[94]
29	RAW_STATUS_157	W1S	0h	Raw Status (write 1 to set) for slv_events_in[93]
28	RAW_STATUS_156	W1S	0h	Raw Status (write 1 to set) for slv_events_in[92]
27	RAW_STATUS_155	W1S	0h	Raw Status (write 1 to set) for slv_events_in[91]
26	RAW_STATUS_154	W1S	0h	Raw Status (write 1 to set) for slv_events_in[90]
25	RAW_STATUS_153	W1S	0h	Raw Status (write 1 to set) for slv_events_in[89]
24	RAW_STATUS_152	W1S	0h	Raw Status (write 1 to set) for slv_events_in[88]
23	RAW_STATUS_151	W1S	0h	Raw Status (write 1 to set) for slv_events_in[87]
22	RAW_STATUS_150	W1S	0h	Raw Status (write 1 to set) for slv_events_in[86]
21	RAW_STATUS_149	W1S	0h	Raw Status (write 1 to set) for slv_events_in[85]
20	RAW_STATUS_148	W1S	0h	Raw Status (write 1 to set) for slv_events_in[84]
19	RAW_STATUS_147	W1S	0h	Raw Status (write 1 to set) for slv_events_in[83]
18	RAW_STATUS_146	W1S	0h	Raw Status (write 1 to set) for slv_events_in[82]
17	RAW_STATUS_145	W1S	0h	Raw Status (write 1 to set) for slv_events_in[81]
16	RAW_STATUS_144	W1S	0h	Raw Status (write 1 to set) for slv_events_in[80]

Table 14-10519. ICSS_INTC_RAW_STATUS_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RAW_STATUS_143	W1S	0h	Raw Status (write 1 to set) for slv_events_in[79]
14	RAW_STATUS_142	W1S	0h	Raw Status (write 1 to set) for slv_events_in[78]
13	RAW_STATUS_141	W1S	0h	Raw Status (write 1 to set) for slv_events_in[77]
12	RAW_STATUS_140	W1S	0h	Raw Status (write 1 to set) for slv_events_in[76]
11	RAW_STATUS_139	W1S	0h	Raw Status (write 1 to set) for slv_events_in[75]
10	RAW_STATUS_138	W1S	0h	Raw Status (write 1 to set) for slv_events_in[74]
9	RAW_STATUS_137	W1S	0h	Raw Status (write 1 to set) for slv_events_in[73]
8	RAW_STATUS_136	W1S	0h	Raw Status (write 1 to set) for slv_events_in[72]
7	RAW_STATUS_135	W1S	0h	Raw Status (write 1 to set) for slv_events_in[71]
6	RAW_STATUS_134	W1S	0h	Raw Status (write 1 to set) for slv_events_in[70]
5	RAW_STATUS_133	W1S	0h	Raw Status (write 1 to set) for slv_events_in[69]
4	RAW_STATUS_132	W1S	0h	Raw Status (write 1 to set) for slv_events_in[68]
3	RAW_STATUS_131	W1S	0h	Raw Status (write 1 to set) for slv_events_in[67]
2	RAW_STATUS_130	W1S	0h	Raw Status (write 1 to set) for slv_events_in[66]
1	RAW_STATUS_129	W1S	0h	Raw Status (write 1 to set) for slv_events_in[65]
0	RAW_STATUS_128	W1S	0h	Raw Status (write 1 to set) for slv_events_in[64]

17 ICSS_INTC_ENA_STATUS_REG0 Register (Offset = 280h) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG0 is shown in Figure 14-3481 and described in Table 14-7041.

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Enabled Status Register 0

Table 14-10520. ICSS_INTC_ENA_STATUS_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0280h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0280h

Figure 14-3481. ICSS_INTC_ENA_STATUS_REG0 Register

31	30	29	28	27	26	25	24
ENA_STATUS_31	ENA_STATUS_30	ENA_STATUS_29	ENA_STATUS_28	ENA_STATUS_27	ENA_STATUS_26	ENA_STATUS_25	ENA_STATUS_24
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_23	ENA_STATUS_22	ENA_STATUS_21	ENA_STATUS_20	ENA_STATUS_19	ENA_STATUS_18	ENA_STATUS_17	ENA_STATUS_16
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_15	ENA_STATUS_14	ENA_STATUS_13	ENA_STATUS_12	ENA_STATUS_11	ENA_STATUS_10	ENA_STATUS_9	ENA_STATUS_8
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_7	ENA_STATUS_6	ENA_STATUS_5	ENA_STATUS_4	ENA_STATUS_3	ENA_STATUS_2	ENA_STATUS_1	ENA_STATUS_0
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 14-10522. ICSS_INTC_ENA_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_31	W1C	0h	Enabled Status for intr_in[31]
30	ENA_STATUS_30	W1C	0h	Enabled Status for intr_in[30]
29	ENA_STATUS_29	W1C	0h	Enabled Status for intr_in[29]
28	ENA_STATUS_28	W1C	0h	Enabled Status for intr_in[28]
27	ENA_STATUS_27	W1C	0h	Enabled Status for intr_in[27]
26	ENA_STATUS_26	W1C	0h	Enabled Status for intr_in[26]
25	ENA_STATUS_25	W1C	0h	Enabled Status for intr_in[25]
24	ENA_STATUS_24	W1C	0h	Enabled Status for intr_in[24]
23	ENA_STATUS_23	W1C	0h	Enabled Status for intr_in[23]
22	ENA_STATUS_22	W1C	0h	Enabled Status for intr_in[22]
21	ENA_STATUS_21	W1C	0h	Enabled Status for intr_in[21]
20	ENA_STATUS_20	W1C	0h	Enabled Status for intr_in[20]
19	ENA_STATUS_19	W1C	0h	Enabled Status for intr_in[19]
18	ENA_STATUS_18	W1C	0h	Enabled Status for intr_in[18]
17	ENA_STATUS_17	W1C	0h	Enabled Status for intr_in[17]
16	ENA_STATUS_16	W1C	0h	Enabled Status for intr_in[16]

Table 14-10522. ICSS_INTC_ENA_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENA_STATUS_15	W1C	0h	Enabled Status for intr_in[15]
14	ENA_STATUS_14	W1C	0h	Enabled Status for intr_in[14]
13	ENA_STATUS_13	W1C	0h	Enabled Status for intr_in[13]
12	ENA_STATUS_12	W1C	0h	Enabled Status for intr_in[12]
11	ENA_STATUS_11	W1C	0h	Enabled Status for intr_in[11]
10	ENA_STATUS_10	W1C	0h	Enabled Status for intr_in[10]
9	ENA_STATUS_9	W1C	0h	Enabled Status for intr_in[9]
8	ENA_STATUS_8	W1C	0h	Enabled Status for intr_in[8]
7	ENA_STATUS_7	W1C	0h	Enabled Status for intr_in[7]
6	ENA_STATUS_6	W1C	0h	Enabled Status for intr_in[6]
5	ENA_STATUS_5	W1C	0h	Enabled Status for intr_in[5]
4	ENA_STATUS_4	W1C	0h	Enabled Status for intr_in[4]
3	ENA_STATUS_3	W1C	0h	Enabled Status for intr_in[3]
2	ENA_STATUS_2	W1C	0h	Enabled Status for intr_in[2]
1	ENA_STATUS_1	W1C	0h	Enabled Status for intr_in[1]
0	ENA_STATUS_0	W1C	0h	Enabled Status for intr_in[0]

18 ICSS_INTC_ENA_STATUS_REG1 Register (Offset = 284h) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG1 is shown in Figure 14-3482 and described in Table 14-7043.

Return to Summary Table.

Enabled Status Register 1

Table 14-10523. ICSS_INTC_ENA_STATUS_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0284h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0284h

Figure 14-3482. ICSS_INTC_ENA_STATUS_REG1 Register

31	30	29	28	27	26	25	24
ENA_STATUS_63	ENA_STATUS_62	ENA_STATUS_61	ENA_STATUS_60	ENA_STATUS_59	ENA_STATUS_58	ENA_STATUS_57	ENA_STATUS_56
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_55	ENA_STATUS_54	ENA_STATUS_53	ENA_STATUS_52	ENA_STATUS_51	ENA_STATUS_50	ENA_STATUS_49	ENA_STATUS_48
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_47	ENA_STATUS_46	ENA_STATUS_45	ENA_STATUS_44	ENA_STATUS_43	ENA_STATUS_42	ENA_STATUS_41	ENA_STATUS_40
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_39	ENA_STATUS_38	ENA_STATUS_37	ENA_STATUS_36	ENA_STATUS_35	ENA_STATUS_34	ENA_STATUS_33	ENA_STATUS_32
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; *-n* = value after reset

Table 14-10525. ICSS_INTC_ENA_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_63	W1C	0h	Enabled Status for intr_in[63]
30	ENA_STATUS_62	W1C	0h	Enabled Status for intr_in[62]
29	ENA_STATUS_61	W1C	0h	Enabled Status for intr_in[61]
28	ENA_STATUS_60	W1C	0h	Enabled Status for intr_in[60]
27	ENA_STATUS_59	W1C	0h	Enabled Status for intr_in[59]
26	ENA_STATUS_58	W1C	0h	Enabled Status for intr_in[58]
25	ENA_STATUS_57	W1C	0h	Enabled Status for intr_in[57]
24	ENA_STATUS_56	W1C	0h	Enabled Status for intr_in[56]
23	ENA_STATUS_55	W1C	0h	Enabled Status for intr_in[55]
22	ENA_STATUS_54	W1C	0h	Enabled Status for intr_in[54]
21	ENA_STATUS_53	W1C	0h	Enabled Status for intr_in[53]
20	ENA_STATUS_52	W1C	0h	Enabled Status for intr_in[52]
19	ENA_STATUS_51	W1C	0h	Enabled Status for intr_in[51]
18	ENA_STATUS_50	W1C	0h	Enabled Status for intr_in[50]
17	ENA_STATUS_49	W1C	0h	Enabled Status for intr_in[49]
16	ENA_STATUS_48	W1C	0h	Enabled Status for intr_in[48]

Table 14-10525. ICSS_INTC_ENA_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENA_STATUS_47	W1C	0h	Enabled Status for intr_in[47]
14	ENA_STATUS_46	W1C	0h	Enabled Status for intr_in[46]
13	ENA_STATUS_45	W1C	0h	Enabled Status for intr_in[45]
12	ENA_STATUS_44	W1C	0h	Enabled Status for intr_in[44]
11	ENA_STATUS_43	W1C	0h	Enabled Status for intr_in[43]
10	ENA_STATUS_42	W1C	0h	Enabled Status for intr_in[42]
9	ENA_STATUS_41	W1C	0h	Enabled Status for intr_in[41]
8	ENA_STATUS_40	W1C	0h	Enabled Status for intr_in[40]
7	ENA_STATUS_39	W1C	0h	Enabled Status for intr_in[39]
6	ENA_STATUS_38	W1C	0h	Enabled Status for intr_in[38]
5	ENA_STATUS_37	W1C	0h	Enabled Status for intr_in[37]
4	ENA_STATUS_36	W1C	0h	Enabled Status for intr_in[36]
3	ENA_STATUS_35	W1C	0h	Enabled Status for intr_in[35]
2	ENA_STATUS_34	W1C	0h	Enabled Status for intr_in[34]
1	ENA_STATUS_33	W1C	0h	Enabled Status for intr_in[33]
0	ENA_STATUS_32	W1C	0h	Enabled Status for intr_in[32]

19 ICSS_INTC_ENA_STATUS_REG2 Register (Offset = 288h) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG2 is shown in Figure 14-3483 and described in Table 14-7045.

Return to Summary Table.

Enabled Status Register 2

Table 14-10526. ICSS_INTC_ENA_STATUS_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0288h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0288h

Figure 14-3483. ICSS_INTC_ENA_STATUS_REG2 Register

31	30	29	28	27	26	25	24
ENA_STATUS_95	ENA_STATUS_94	ENA_STATUS_93	ENA_STATUS_92	ENA_STATUS_91	ENA_STATUS_90	ENA_STATUS_89	ENA_STATUS_88
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_87	ENA_STATUS_86	ENA_STATUS_85	ENA_STATUS_84	ENA_STATUS_83	ENA_STATUS_82	ENA_STATUS_81	ENA_STATUS_80
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_79	ENA_STATUS_78	ENA_STATUS_77	ENA_STATUS_76	ENA_STATUS_75	ENA_STATUS_74	ENA_STATUS_73	ENA_STATUS_72
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_71	ENA_STATUS_70	ENA_STATUS_69	ENA_STATUS_68	ENA_STATUS_67	ENA_STATUS_66	ENA_STATUS_65	ENA_STATUS_64
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 14-10528. ICSS_INTC_ENA_STATUS_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_95	W1C	0h	Enabled Status for slv_events_in[31]
30	ENA_STATUS_94	W1C	0h	Enabled Status for slv_events_in[30]
29	ENA_STATUS_93	W1C	0h	Enabled Status for slv_events_in[29]
28	ENA_STATUS_92	W1C	0h	Enabled Status for slv_events_in[28]
27	ENA_STATUS_91	W1C	0h	Enabled Status for slv_events_in[27]
26	ENA_STATUS_90	W1C	0h	Enabled Status for slv_events_in[26]
25	ENA_STATUS_89	W1C	0h	Enabled Status for slv_events_in[25]
24	ENA_STATUS_88	W1C	0h	Enabled Status for slv_events_in[24]
23	ENA_STATUS_87	W1C	0h	Enabled Status for slv_events_in[23]
22	ENA_STATUS_86	W1C	0h	Enabled Status for slv_events_in[22]
21	ENA_STATUS_85	W1C	0h	Enabled Status for slv_events_in[21]
20	ENA_STATUS_84	W1C	0h	Enabled Status for slv_events_in[20]
19	ENA_STATUS_83	W1C	0h	Enabled Status for slv_events_in[19]
18	ENA_STATUS_82	W1C	0h	Enabled Status for slv_events_in[18]
17	ENA_STATUS_81	W1C	0h	Enabled Status for slv_events_in[17]
16	ENA_STATUS_80	W1C	0h	Enabled Status for slv_events_in[16]

Table 14-10528. ICSS_INTC_ENA_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENA_STATUS_79	W1C	0h	Enabled Status for slv_events_in[15]
14	ENA_STATUS_78	W1C	0h	Enabled Status for slv_events_in[14]
13	ENA_STATUS_77	W1C	0h	Enabled Status for slv_events_in[13]
12	ENA_STATUS_76	W1C	0h	Enabled Status for slv_events_in[12]
11	ENA_STATUS_75	W1C	0h	Enabled Status for slv_events_in[11]
10	ENA_STATUS_74	W1C	0h	Enabled Status for slv_events_in[10]
9	ENA_STATUS_73	W1C	0h	Enabled Status for slv_events_in[9]
8	ENA_STATUS_72	W1C	0h	Enabled Status for slv_events_in[8]
7	ENA_STATUS_71	W1C	0h	Enabled Status for slv_events_in[7]
6	ENA_STATUS_70	W1C	0h	Enabled Status for slv_events_in[6]
5	ENA_STATUS_69	W1C	0h	Enabled Status for slv_events_in[5]
4	ENA_STATUS_68	W1C	0h	Enabled Status for slv_events_in[4]
3	ENA_STATUS_67	W1C	0h	Enabled Status for slv_events_in[3]
2	ENA_STATUS_66	W1C	0h	Enabled Status for slv_events_in[2]
1	ENA_STATUS_65	W1C	0h	Enabled Status for slv_events_in[1]
0	ENA_STATUS_64	W1C	0h	Enabled Status for slv_events_in[0]

20 ICSS_INTC_ENA_STATUS_REG3 Register (Offset = 28Ch) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG3 is shown in Figure 14-3484 and described in Table 14-7047.

Return to Summary Table.

Enabled Status Register 3

Table 14-10529. ICSS_INTC_ENA_STATUS_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 028Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 028Ch

Figure 14-3484. ICSS_INTC_ENA_STATUS_REG3 Register

31	30	29	28	27	26	25	24
ENA_STATUS_127	ENA_STATUS_126	ENA_STATUS_125	ENA_STATUS_124	ENA_STATUS_123	ENA_STATUS_122	ENA_STATUS_121	ENA_STATUS_120
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_119	ENA_STATUS_118	ENA_STATUS_117	ENA_STATUS_116	ENA_STATUS_115	ENA_STATUS_114	ENA_STATUS_113	ENA_STATUS_112
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_111	ENA_STATUS_110	ENA_STATUS_109	ENA_STATUS_108	ENA_STATUS_107	ENA_STATUS_106	ENA_STATUS_105	ENA_STATUS_104
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_103	ENA_STATUS_102	ENA_STATUS_101	ENA_STATUS_100	ENA_STATUS_99	ENA_STATUS_98	ENA_STATUS_97	ENA_STATUS_96
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; *-n* = value after reset

Table 14-10531. ICSS_INTC_ENA_STATUS_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_127	W1C	0h	Enabled Status for slv_events_in[63]
30	ENA_STATUS_126	W1C	0h	Enabled Status for slv_events_in[62]
29	ENA_STATUS_125	W1C	0h	Enabled Status for slv_events_in[61]
28	ENA_STATUS_124	W1C	0h	Enabled Status for slv_events_in[60]
27	ENA_STATUS_123	W1C	0h	Enabled Status for slv_events_in[59]
26	ENA_STATUS_122	W1C	0h	Enabled Status for slv_events_in[58]
25	ENA_STATUS_121	W1C	0h	Enabled Status for slv_events_in[57]
24	ENA_STATUS_120	W1C	0h	Enabled Status for slv_events_in[56]
23	ENA_STATUS_119	W1C	0h	Enabled Status for slv_events_in[55]
22	ENA_STATUS_118	W1C	0h	Enabled Status for slv_events_in[54]
21	ENA_STATUS_117	W1C	0h	Enabled Status for slv_events_in[53]
20	ENA_STATUS_116	W1C	0h	Enabled Status for slv_events_in[52]
19	ENA_STATUS_115	W1C	0h	Enabled Status for slv_events_in[51]
18	ENA_STATUS_114	W1C	0h	Enabled Status for slv_events_in[50]
17	ENA_STATUS_113	W1C	0h	Enabled Status for slv_events_in[49]
16	ENA_STATUS_112	W1C	0h	Enabled Status for slv_events_in[48]

Table 14-10531. ICSS_INTC_ENA_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENA_STATUS_111	W1C	0h	Enabled Status for slv_events_in[47]
14	ENA_STATUS_110	W1C	0h	Enabled Status for slv_events_in[46]
13	ENA_STATUS_109	W1C	0h	Enabled Status for slv_events_in[45]
12	ENA_STATUS_108	W1C	0h	Enabled Status for slv_events_in[44]
11	ENA_STATUS_107	W1C	0h	Enabled Status for slv_events_in[43]
10	ENA_STATUS_106	W1C	0h	Enabled Status for slv_events_in[42]
9	ENA_STATUS_105	W1C	0h	Enabled Status for slv_events_in[41]
8	ENA_STATUS_104	W1C	0h	Enabled Status for slv_events_in[40]
7	ENA_STATUS_103	W1C	0h	Enabled Status for slv_events_in[39]
6	ENA_STATUS_102	W1C	0h	Enabled Status for slv_events_in[38]
5	ENA_STATUS_101	W1C	0h	Enabled Status for slv_events_in[37]
4	ENA_STATUS_100	W1C	0h	Enabled Status for slv_events_in[36]
3	ENA_STATUS_99	W1C	0h	Enabled Status for slv_events_in[35]
2	ENA_STATUS_98	W1C	0h	Enabled Status for slv_events_in[34]
1	ENA_STATUS_97	W1C	0h	Enabled Status for slv_events_in[33]
0	ENA_STATUS_96	W1C	0h	Enabled Status for slv_events_in[32]

21 ICSS_INTC_ENA_STATUS_REG4 Register (Offset = 290h) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG4 is shown in Figure 14-3485 and described in Table 14-7049.

Return to Summary Table.

Enabled Status Register 4

Table 14-10532. ICSS_INTC_ENA_STATUS_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0290h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0290h

Figure 14-3485. ICSS_INTC_ENA_STATUS_REG4 Register

31	30	29	28	27	26	25	24
ENA_STATUS_159	ENA_STATUS_158	ENA_STATUS_157	ENA_STATUS_156	ENA_STATUS_155	ENA_STATUS_154	ENA_STATUS_153	ENA_STATUS_152
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_151	ENA_STATUS_150	ENA_STATUS_149	ENA_STATUS_148	ENA_STATUS_147	ENA_STATUS_146	ENA_STATUS_145	ENA_STATUS_144
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_143	ENA_STATUS_142	ENA_STATUS_141	ENA_STATUS_140	ENA_STATUS_139	ENA_STATUS_138	ENA_STATUS_137	ENA_STATUS_136
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_135	ENA_STATUS_134	ENA_STATUS_133	ENA_STATUS_132	ENA_STATUS_131	ENA_STATUS_130	ENA_STATUS_129	ENA_STATUS_128
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 14-10534. ICSS_INTC_ENA_STATUS_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_159	W1C	0h	Enabled Status for slv_events_in[95]
30	ENA_STATUS_158	W1C	0h	Enabled Status for slv_events_in[94]
29	ENA_STATUS_157	W1C	0h	Enabled Status for slv_events_in[93]
28	ENA_STATUS_156	W1C	0h	Enabled Status for slv_events_in[92]
27	ENA_STATUS_155	W1C	0h	Enabled Status for slv_events_in[91]
26	ENA_STATUS_154	W1C	0h	Enabled Status for slv_events_in[90]
25	ENA_STATUS_153	W1C	0h	Enabled Status for slv_events_in[89]
24	ENA_STATUS_152	W1C	0h	Enabled Status for slv_events_in[88]
23	ENA_STATUS_151	W1C	0h	Enabled Status for slv_events_in[87]
22	ENA_STATUS_150	W1C	0h	Enabled Status for slv_events_in[86]
21	ENA_STATUS_149	W1C	0h	Enabled Status for slv_events_in[85]
20	ENA_STATUS_148	W1C	0h	Enabled Status for slv_events_in[84]
19	ENA_STATUS_147	W1C	0h	Enabled Status for slv_events_in[83]
18	ENA_STATUS_146	W1C	0h	Enabled Status for slv_events_in[82]
17	ENA_STATUS_145	W1C	0h	Enabled Status for slv_events_in[81]
16	ENA_STATUS_144	W1C	0h	Enabled Status for slv_events_in[80]

Table 14-10534. ICSS_INTC_ENA_STATUS_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENA_STATUS_143	W1C	0h	Enabled Status for slv_events_in[79]
14	ENA_STATUS_142	W1C	0h	Enabled Status for slv_events_in[78]
13	ENA_STATUS_141	W1C	0h	Enabled Status for slv_events_in[77]
12	ENA_STATUS_140	W1C	0h	Enabled Status for slv_events_in[76]
11	ENA_STATUS_139	W1C	0h	Enabled Status for slv_events_in[75]
10	ENA_STATUS_138	W1C	0h	Enabled Status for slv_events_in[74]
9	ENA_STATUS_137	W1C	0h	Enabled Status for slv_events_in[73]
8	ENA_STATUS_136	W1C	0h	Enabled Status for slv_events_in[72]
7	ENA_STATUS_135	W1C	0h	Enabled Status for slv_events_in[71]
6	ENA_STATUS_134	W1C	0h	Enabled Status for slv_events_in[70]
5	ENA_STATUS_133	W1C	0h	Enabled Status for slv_events_in[69]
4	ENA_STATUS_132	W1C	0h	Enabled Status for slv_events_in[68]
3	ENA_STATUS_131	W1C	0h	Enabled Status for slv_events_in[67]
2	ENA_STATUS_130	W1C	0h	Enabled Status for slv_events_in[66]
1	ENA_STATUS_129	W1C	0h	Enabled Status for slv_events_in[65]
0	ENA_STATUS_128	W1C	0h	Enabled Status for slv_events_in[64]

22 ICSS_INTC_ENABLE_REG0 Register (Offset = 300h) [reset = 0h]

ICSS_INTC_ENABLE_REG0 is shown in Figure 14-3486 and described in Table 14-7051.

Return to Summary Table.

Enable Register 0

Table 14-10535. ICSS_INTC_ENABLE_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0300h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0300h

Figure 14-3486. ICSS_INTC_ENABLE_REG0 Register

31	30	29	28	27	26	25	24
ENABLE_31	ENABLE_30	ENABLE_29	ENABLE_28	ENABLE_27	ENABLE_26	ENABLE_25	ENABLE_24
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_23	ENABLE_22	ENABLE_21	ENABLE_20	ENABLE_19	ENABLE_18	ENABLE_17	ENABLE_16
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_15	ENABLE_14	ENABLE_13	ENABLE_12	ENABLE_11	ENABLE_10	ENABLE_9	ENABLE_8
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_7	ENABLE_6	ENABLE_5	ENABLE_4	ENABLE_3	ENABLE_2	ENABLE_1	ENABLE_0
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-10537. ICSS_INTC_ENABLE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_31	W1S	0h	Enable (set) for intr_in[31]
30	ENABLE_30	W1S	0h	Enable (set) for intr_in[30]
29	ENABLE_29	W1S	0h	Enable (set) for intr_in[29]
28	ENABLE_28	W1S	0h	Enable (set) for intr_in[28]
27	ENABLE_27	W1S	0h	Enable (set) for intr_in[27]
26	ENABLE_26	W1S	0h	Enable (set) for intr_in[26]
25	ENABLE_25	W1S	0h	Enable (set) for intr_in[25]
24	ENABLE_24	W1S	0h	Enable (set) for intr_in[24]
23	ENABLE_23	W1S	0h	Enable (set) for intr_in[23]
22	ENABLE_22	W1S	0h	Enable (set) for intr_in[22]
21	ENABLE_21	W1S	0h	Enable (set) for intr_in[21]
20	ENABLE_20	W1S	0h	Enable (set) for intr_in[20]
19	ENABLE_19	W1S	0h	Enable (set) for intr_in[19]
18	ENABLE_18	W1S	0h	Enable (set) for intr_in[18]
17	ENABLE_17	W1S	0h	Enable (set) for intr_in[17]
16	ENABLE_16	W1S	0h	Enable (set) for intr_in[16]
15	ENABLE_15	W1S	0h	Enable (set) for intr_in[15]
14	ENABLE_14	W1S	0h	Enable (set) for intr_in[14]
13	ENABLE_13	W1S	0h	Enable (set) for intr_in[13]

Table 14-10537. ICSS_INTC_ENABLE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ENABLE_12	W1S	0h	Enable (set) for intr_in[12]
11	ENABLE_11	W1S	0h	Enable (set) for intr_in[11]
10	ENABLE_10	W1S	0h	Enable (set) for intr_in[10]
9	ENABLE_9	W1S	0h	Enable (set) for intr_in[9]
8	ENABLE_8	W1S	0h	Enable (set) for intr_in[8]
7	ENABLE_7	W1S	0h	Enable (set) for intr_in[7]
6	ENABLE_6	W1S	0h	Enable (set) for intr_in[6]
5	ENABLE_5	W1S	0h	Enable (set) for intr_in[5]
4	ENABLE_4	W1S	0h	Enable (set) for intr_in[4]
3	ENABLE_3	W1S	0h	Enable (set) for intr_in[3]
2	ENABLE_2	W1S	0h	Enable (set) for intr_in[2]
1	ENABLE_1	W1S	0h	Enable (set) for intr_in[1]
0	ENABLE_0	W1S	0h	Enable (set) for intr_in[0]

23 ICSS_INTC_ENABLE_REG1 Register (Offset = 304h) [reset = 0h]

ICSS_INTC_ENABLE_REG1 is shown in Figure 14-3487 and described in Table 14-7053.

Return to Summary Table.

Enable Register 1

Table 14-10538. ICSS_INTC_ENABLE_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0304h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0304h

Figure 14-3487. ICSS_INTC_ENABLE_REG1 Register

31	30	29	28	27	26	25	24
ENABLE_63	ENABLE_62	ENABLE_61	ENABLE_60	ENABLE_59	ENABLE_58	ENABLE_57	ENABLE_56
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_55	ENABLE_54	ENABLE_53	ENABLE_52	ENABLE_51	ENABLE_50	ENABLE_49	ENABLE_48
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_47	ENABLE_46	ENABLE_45	ENABLE_44	ENABLE_43	ENABLE_42	ENABLE_41	ENABLE_40
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_39	ENABLE_38	ENABLE_37	ENABLE_36	ENABLE_35	ENABLE_34	ENABLE_33	ENABLE_32
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-10540. ICSS_INTC_ENABLE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_63	W1S	0h	Enable (set) for intr_in[63]
30	ENABLE_62	W1S	0h	Enable (set) for intr_in[62]
29	ENABLE_61	W1S	0h	Enable (set) for intr_in[61]
28	ENABLE_60	W1S	0h	Enable (set) for intr_in[60]
27	ENABLE_59	W1S	0h	Enable (set) for intr_in[59]
26	ENABLE_58	W1S	0h	Enable (set) for intr_in[58]
25	ENABLE_57	W1S	0h	Enable (set) for intr_in[57]
24	ENABLE_56	W1S	0h	Enable (set) for intr_in[56]
23	ENABLE_55	W1S	0h	Enable (set) for intr_in[55]
22	ENABLE_54	W1S	0h	Enable (set) for intr_in[54]
21	ENABLE_53	W1S	0h	Enable (set) for intr_in[53]
20	ENABLE_52	W1S	0h	Enable (set) for intr_in[52]
19	ENABLE_51	W1S	0h	Enable (set) for intr_in[51]
18	ENABLE_50	W1S	0h	Enable (set) for intr_in[50]
17	ENABLE_49	W1S	0h	Enable (set) for intr_in[49]
16	ENABLE_48	W1S	0h	Enable (set) for intr_in[48]
15	ENABLE_47	W1S	0h	Enable (set) for intr_in[47]
14	ENABLE_46	W1S	0h	Enable (set) for intr_in[46]
13	ENABLE_45	W1S	0h	Enable (set) for intr_in[45]

Table 14-10540. ICSS_INTC_ENABLE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ENABLE_44	W1S	0h	Enable (set) for intr_in[44]
11	ENABLE_43	W1S	0h	Enable (set) for intr_in[43]
10	ENABLE_42	W1S	0h	Enable (set) for intr_in[42]
9	ENABLE_41	W1S	0h	Enable (set) for intr_in[41]
8	ENABLE_40	W1S	0h	Enable (set) for intr_in[40]
7	ENABLE_39	W1S	0h	Enable (set) for intr_in[39]
6	ENABLE_38	W1S	0h	Enable (set) for intr_in[38]
5	ENABLE_37	W1S	0h	Enable (set) for intr_in[37]
4	ENABLE_36	W1S	0h	Enable (set) for intr_in[36]
3	ENABLE_35	W1S	0h	Enable (set) for intr_in[35]
2	ENABLE_34	W1S	0h	Enable (set) for intr_in[34]
1	ENABLE_33	W1S	0h	Enable (set) for intr_in[33]
0	ENABLE_32	W1S	0h	Enable (set) for intr_in[32]

24 ICSS_INTC_ENABLE_REG2 Register (Offset = 308h) [reset = 0h]

ICSS_INTC_ENABLE_REG2 is shown in Figure 14-3488 and described in Table 14-7055.

Return to Summary Table.

Enable Register 2

Table 14-10541. ICSS_INTC_ENABLE_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0308h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0308h

Figure 14-3488. ICSS_INTC_ENABLE_REG2 Register

31	30	29	28	27	26	25	24
ENABLE_95	ENABLE_94	ENABLE_93	ENABLE_92	ENABLE_91	ENABLE_90	ENABLE_89	ENABLE_88
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_87	ENABLE_86	ENABLE_85	ENABLE_84	ENABLE_83	ENABLE_82	ENABLE_81	ENABLE_80
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_79	ENABLE_78	ENABLE_77	ENABLE_76	ENABLE_75	ENABLE_74	ENABLE_73	ENABLE_72
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_71	ENABLE_70	ENABLE_69	ENABLE_68	ENABLE_67	ENABLE_66	ENABLE_65	ENABLE_64
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-10543. ICSS_INTC_ENABLE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_95	W1S	0h	Enable (set) for slv_events_in[31]
30	ENABLE_94	W1S	0h	Enable (set) for slv_events_in[30]
29	ENABLE_93	W1S	0h	Enable (set) for slv_events_in[29]
28	ENABLE_92	W1S	0h	Enable (set) for slv_events_in[28]
27	ENABLE_91	W1S	0h	Enable (set) for slv_events_in[27]
26	ENABLE_90	W1S	0h	Enable (set) for slv_events_in[26]
25	ENABLE_89	W1S	0h	Enable (set) for slv_events_in[25]
24	ENABLE_88	W1S	0h	Enable (set) for slv_events_in[24]
23	ENABLE_87	W1S	0h	Enable (set) for slv_events_in[23]
22	ENABLE_86	W1S	0h	Enable (set) for slv_events_in[22]
21	ENABLE_85	W1S	0h	Enable (set) for slv_events_in[21]
20	ENABLE_84	W1S	0h	Enable (set) for slv_events_in[20]
19	ENABLE_83	W1S	0h	Enable (set) for slv_events_in[19]
18	ENABLE_82	W1S	0h	Enable (set) for slv_events_in[18]
17	ENABLE_81	W1S	0h	Enable (set) for slv_events_in[17]
16	ENABLE_80	W1S	0h	Enable (set) for slv_events_in[16]
15	ENABLE_79	W1S	0h	Enable (set) for slv_events_in[15]
14	ENABLE_78	W1S	0h	Enable (set) for slv_events_in[14]
13	ENABLE_77	W1S	0h	Enable (set) for slv_events_in[13]

Table 14-10543. ICSS_INTC_ENABLE_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ENABLE_76	W1S	0h	Enable (set) for slv_events_in[12]
11	ENABLE_75	W1S	0h	Enable (set) for slv_events_in[11]
10	ENABLE_74	W1S	0h	Enable (set) for slv_events_in[10]
9	ENABLE_73	W1S	0h	Enable (set) for slv_events_in[9]
8	ENABLE_72	W1S	0h	Enable (set) for slv_events_in[8]
7	ENABLE_71	W1S	0h	Enable (set) for slv_events_in[7]
6	ENABLE_70	W1S	0h	Enable (set) for slv_events_in[6]
5	ENABLE_69	W1S	0h	Enable (set) for slv_events_in[5]
4	ENABLE_68	W1S	0h	Enable (set) for slv_events_in[4]
3	ENABLE_67	W1S	0h	Enable (set) for slv_events_in[3]
2	ENABLE_66	W1S	0h	Enable (set) for slv_events_in[2]
1	ENABLE_65	W1S	0h	Enable (set) for slv_events_in[1]
0	ENABLE_64	W1S	0h	Enable (set) for slv_events_in[0]

25 ICSS_INTC_ENABLE_REG3 Register (Offset = 30Ch) [reset = 0h]

ICSS_INTC_ENABLE_REG3 is shown in Figure 14-3489 and described in Table 14-7057.

Return to Summary Table.

Enable Register 3

Table 14-10544. ICSS_INTC_ENABLE_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 030Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 030Ch

Figure 14-3489. ICSS_INTC_ENABLE_REG3 Register

31	30	29	28	27	26	25	24
ENABLE_127	ENABLE_126	ENABLE_125	ENABLE_124	ENABLE_123	ENABLE_122	ENABLE_121	ENABLE_120
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_119	ENABLE_118	ENABLE_117	ENABLE_116	ENABLE_115	ENABLE_114	ENABLE_113	ENABLE_112
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_111	ENABLE_110	ENABLE_109	ENABLE_108	ENABLE_107	ENABLE_106	ENABLE_105	ENABLE_104
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_103	ENABLE_102	ENABLE_101	ENABLE_100	ENABLE_99	ENABLE_98	ENABLE_97	ENABLE_96
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-10546. ICSS_INTC_ENABLE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_127	W1S	0h	Enable (set) for slv_events_in[63]
30	ENABLE_126	W1S	0h	Enable (set) for slv_events_in[62]
29	ENABLE_125	W1S	0h	Enable (set) for slv_events_in[61]
28	ENABLE_124	W1S	0h	Enable (set) for slv_events_in[60]
27	ENABLE_123	W1S	0h	Enable (set) for slv_events_in[59]
26	ENABLE_122	W1S	0h	Enable (set) for slv_events_in[58]
25	ENABLE_121	W1S	0h	Enable (set) for slv_events_in[57]
24	ENABLE_120	W1S	0h	Enable (set) for slv_events_in[56]
23	ENABLE_119	W1S	0h	Enable (set) for slv_events_in[55]
22	ENABLE_118	W1S	0h	Enable (set) for slv_events_in[54]
21	ENABLE_117	W1S	0h	Enable (set) for slv_events_in[53]
20	ENABLE_116	W1S	0h	Enable (set) for slv_events_in[52]
19	ENABLE_115	W1S	0h	Enable (set) for slv_events_in[51]
18	ENABLE_114	W1S	0h	Enable (set) for slv_events_in[50]
17	ENABLE_113	W1S	0h	Enable (set) for slv_events_in[49]
16	ENABLE_112	W1S	0h	Enable (set) for slv_events_in[48]
15	ENABLE_111	W1S	0h	Enable (set) for slv_events_in[47]
14	ENABLE_110	W1S	0h	Enable (set) for slv_events_in[46]
13	ENABLE_109	W1S	0h	Enable (set) for slv_events_in[45]

Table 14-10546. ICSS_INTC_ENABLE_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ENABLE_108	W1S	0h	Enable (set) for slv_events_in[44]
11	ENABLE_107	W1S	0h	Enable (set) for slv_events_in[43]
10	ENABLE_106	W1S	0h	Enable (set) for slv_events_in[42]
9	ENABLE_105	W1S	0h	Enable (set) for slv_events_in[41]
8	ENABLE_104	W1S	0h	Enable (set) for slv_events_in[40]
7	ENABLE_103	W1S	0h	Enable (set) for slv_events_in[39]
6	ENABLE_102	W1S	0h	Enable (set) for slv_events_in[38]
5	ENABLE_101	W1S	0h	Enable (set) for slv_events_in[37]
4	ENABLE_100	W1S	0h	Enable (set) for slv_events_in[36]
3	ENABLE_99	W1S	0h	Enable (set) for slv_events_in[35]
2	ENABLE_98	W1S	0h	Enable (set) for slv_events_in[34]
1	ENABLE_97	W1S	0h	Enable (set) for slv_events_in[33]
0	ENABLE_96	W1S	0h	Enable (set) for slv_events_in[32]

26 ICSS_INTC_ENABLE_REG4 Register (Offset = 310h) [reset = 0h]

ICSS_INTC_ENABLE_REG4 is shown in Figure 14-3490 and described in Table 14-7059.

Return to Summary Table.

Enable Register 4

Table 14-10547. ICSS_INTC_ENABLE_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0310h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0310h

Figure 14-3490. ICSS_INTC_ENABLE_REG4 Register

31	30	29	28	27	26	25	24
ENABLE_159	ENABLE_158	ENABLE_157	ENABLE_156	ENABLE_155	ENABLE_154	ENABLE_153	ENABLE_152
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_151	ENABLE_150	ENABLE_149	ENABLE_148	ENABLE_147	ENABLE_146	ENABLE_145	ENABLE_144
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_143	ENABLE_142	ENABLE_141	ENABLE_140	ENABLE_139	ENABLE_138	ENABLE_137	ENABLE_136
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_135	ENABLE_134	ENABLE_133	ENABLE_132	ENABLE_131	ENABLE_130	ENABLE_129	ENABLE_128
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-10549. ICSS_INTC_ENABLE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_159	W1S	0h	Enable (set) for slv_events_in[95]
30	ENABLE_158	W1S	0h	Enable (set) for slv_events_in[94]
29	ENABLE_157	W1S	0h	Enable (set) for slv_events_in[93]
28	ENABLE_156	W1S	0h	Enable (set) for slv_events_in[92]
27	ENABLE_155	W1S	0h	Enable (set) for slv_events_in[91]
26	ENABLE_154	W1S	0h	Enable (set) for slv_events_in[90]
25	ENABLE_153	W1S	0h	Enable (set) for slv_events_in[89]
24	ENABLE_152	W1S	0h	Enable (set) for slv_events_in[88]
23	ENABLE_151	W1S	0h	Enable (set) for slv_events_in[87]
22	ENABLE_150	W1S	0h	Enable (set) for slv_events_in[86]
21	ENABLE_149	W1S	0h	Enable (set) for slv_events_in[85]
20	ENABLE_148	W1S	0h	Enable (set) for slv_events_in[84]
19	ENABLE_147	W1S	0h	Enable (set) for slv_events_in[83]
18	ENABLE_146	W1S	0h	Enable (set) for slv_events_in[82]
17	ENABLE_145	W1S	0h	Enable (set) for slv_events_in[81]
16	ENABLE_144	W1S	0h	Enable (set) for slv_events_in[80]
15	ENABLE_143	W1S	0h	Enable (set) for slv_events_in[79]
14	ENABLE_142	W1S	0h	Enable (set) for slv_events_in[78]
13	ENABLE_141	W1S	0h	Enable (set) for slv_events_in[77]

Table 14-10549. ICSS_INTC_ENABLE_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ENABLE_140	W1S	0h	Enable (set) for slv_events_in[76]
11	ENABLE_139	W1S	0h	Enable (set) for slv_events_in[75]
10	ENABLE_138	W1S	0h	Enable (set) for slv_events_in[74]
9	ENABLE_137	W1S	0h	Enable (set) for slv_events_in[73]
8	ENABLE_136	W1S	0h	Enable (set) for slv_events_in[72]
7	ENABLE_135	W1S	0h	Enable (set) for slv_events_in[71]
6	ENABLE_134	W1S	0h	Enable (set) for slv_events_in[70]
5	ENABLE_133	W1S	0h	Enable (set) for slv_events_in[69]
4	ENABLE_132	W1S	0h	Enable (set) for slv_events_in[68]
3	ENABLE_131	W1S	0h	Enable (set) for slv_events_in[67]
2	ENABLE_130	W1S	0h	Enable (set) for slv_events_in[66]
1	ENABLE_129	W1S	0h	Enable (set) for slv_events_in[65]
0	ENABLE_128	W1S	0h	Enable (set) for slv_events_in[64]

27 ICSS_INTC_ENABLE_CLR_REG0 Register (Offset = 380h) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG0 is shown in Figure 14-3491 and described in Table 14-7061.

Return to Summary Table.

Enable Clear Register 0

Table 14-10550. ICSS_INTC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0380h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0380h

Figure 14-3491. ICSS_INTC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
ENABLE_31_CLR	ENABLE_30_CLR	ENABLE_29_CLR	ENABLE_28_CLR	ENABLE_27_CLR	ENABLE_26_CLR	ENABLE_25_CLR	ENABLE_24_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_23_CLR	ENABLE_22_CLR	ENABLE_21_CLR	ENABLE_20_CLR	ENABLE_19_CLR	ENABLE_18_CLR	ENABLE_17_CLR	ENABLE_16_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_15_CLR	ENABLE_14_CLR	ENABLE_13_CLR	ENABLE_12_CLR	ENABLE_11_CLR	ENABLE_10_CLR	ENABLE_9_CLR	ENABLE_8_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_7_CLR	ENABLE_6_CLR	ENABLE_5_CLR	ENABLE_4_CLR	ENABLE_3_CLR	ENABLE_2_CLR	ENABLE_1_CLR	ENABLE_0_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; *-n* = value after reset

Table 14-10552. ICSS_INTC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_31_CLR	W1C	0h	Enable clear for intr_in[31]
30	ENABLE_30_CLR	W1C	0h	Enable clear for intr_in[30]
29	ENABLE_29_CLR	W1C	0h	Enable clear for intr_in[29]
28	ENABLE_28_CLR	W1C	0h	Enable clear for intr_in[28]
27	ENABLE_27_CLR	W1C	0h	Enable clear for intr_in[27]
26	ENABLE_26_CLR	W1C	0h	Enable clear for intr_in[26]
25	ENABLE_25_CLR	W1C	0h	Enable clear for intr_in[25]
24	ENABLE_24_CLR	W1C	0h	Enable clear for intr_in[24]
23	ENABLE_23_CLR	W1C	0h	Enable clear for intr_in[23]
22	ENABLE_22_CLR	W1C	0h	Enable clear for intr_in[22]
21	ENABLE_21_CLR	W1C	0h	Enable clear for intr_in[21]
20	ENABLE_20_CLR	W1C	0h	Enable clear for intr_in[20]
19	ENABLE_19_CLR	W1C	0h	Enable clear for intr_in[19]
18	ENABLE_18_CLR	W1C	0h	Enable clear for intr_in[18]
17	ENABLE_17_CLR	W1C	0h	Enable clear for intr_in[17]
16	ENABLE_16_CLR	W1C	0h	Enable clear for intr_in[16]

Table 14-10552. ICSS_INTC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENABLE_15_CLR	W1C	0h	Enable clear for intr_in[15]
14	ENABLE_14_CLR	W1C	0h	Enable clear for intr_in[14]
13	ENABLE_13_CLR	W1C	0h	Enable clear for intr_in[13]
12	ENABLE_12_CLR	W1C	0h	Enable clear for intr_in[12]
11	ENABLE_11_CLR	W1C	0h	Enable clear for intr_in[11]
10	ENABLE_10_CLR	W1C	0h	Enable clear for intr_in[10]
9	ENABLE_9_CLR	W1C	0h	Enable clear for intr_in[9]
8	ENABLE_8_CLR	W1C	0h	Enable clear for intr_in[8]
7	ENABLE_7_CLR	W1C	0h	Enable clear for intr_in[7]
6	ENABLE_6_CLR	W1C	0h	Enable clear for intr_in[6]
5	ENABLE_5_CLR	W1C	0h	Enable clear for intr_in[5]
4	ENABLE_4_CLR	W1C	0h	Enable clear for intr_in[4]
3	ENABLE_3_CLR	W1C	0h	Enable clear for intr_in[3]
2	ENABLE_2_CLR	W1C	0h	Enable clear for intr_in[2]
1	ENABLE_1_CLR	W1C	0h	Enable clear for intr_in[1]
0	ENABLE_0_CLR	W1C	0h	Enable clear for intr_in[0]

28 ICSS_INTC_ENABLE_CLR_REG1 Register (Offset = 384h) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG1 is shown in Figure 14-3492 and described in Table 14-7063.

Return to Summary Table.

Enable Clear Register 1

Table 14-10553. ICSS_INTC_ENABLE_CLR_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0384h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0384h

Figure 14-3492. ICSS_INTC_ENABLE_CLR_REG1 Register

31	30	29	28	27	26	25	24
ENABLE_63_CLR	ENABLE_62_CLR	ENABLE_61_CLR	ENABLE_60_CLR	ENABLE_59_CLR	ENABLE_58_CLR	ENABLE_57_CLR	ENABLE_56_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_55_CLR	ENABLE_54_CLR	ENABLE_53_CLR	ENABLE_52_CLR	ENABLE_51_CLR	ENABLE_50_CLR	ENABLE_49_CLR	ENABLE_48_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_47_CLR	ENABLE_46_CLR	ENABLE_45_CLR	ENABLE_44_CLR	ENABLE_43_CLR	ENABLE_42_CLR	ENABLE_41_CLR	ENABLE_40_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_39_CLR	ENABLE_38_CLR	ENABLE_37_CLR	ENABLE_36_CLR	ENABLE_35_CLR	ENABLE_34_CLR	ENABLE_33_CLR	ENABLE_32_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; *-n* = value after reset

Table 14-10555. ICSS_INTC_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_63_CLR	W1C	0h	Enable clear for intr_in[63]
30	ENABLE_62_CLR	W1C	0h	Enable clear for intr_in[62]
29	ENABLE_61_CLR	W1C	0h	Enable clear for intr_in[61]
28	ENABLE_60_CLR	W1C	0h	Enable clear for intr_in[60]
27	ENABLE_59_CLR	W1C	0h	Enable clear for intr_in[59]
26	ENABLE_58_CLR	W1C	0h	Enable clear for intr_in[58]
25	ENABLE_57_CLR	W1C	0h	Enable clear for intr_in[57]
24	ENABLE_56_CLR	W1C	0h	Enable clear for intr_in[56]
23	ENABLE_55_CLR	W1C	0h	Enable clear for intr_in[55]
22	ENABLE_54_CLR	W1C	0h	Enable clear for intr_in[54]
21	ENABLE_53_CLR	W1C	0h	Enable clear for intr_in[53]
20	ENABLE_52_CLR	W1C	0h	Enable clear for intr_in[52]
19	ENABLE_51_CLR	W1C	0h	Enable clear for intr_in[51]
18	ENABLE_50_CLR	W1C	0h	Enable clear for intr_in[50]
17	ENABLE_49_CLR	W1C	0h	Enable clear for intr_in[49]
16	ENABLE_48_CLR	W1C	0h	Enable clear for intr_in[48]

Table 14-10555. ICSS_INTC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENABLE_47_CLR	W1C	0h	Enable clear for intr_in[47]
14	ENABLE_46_CLR	W1C	0h	Enable clear for intr_in[46]
13	ENABLE_45_CLR	W1C	0h	Enable clear for intr_in[45]
12	ENABLE_44_CLR	W1C	0h	Enable clear for intr_in[44]
11	ENABLE_43_CLR	W1C	0h	Enable clear for intr_in[43]
10	ENABLE_42_CLR	W1C	0h	Enable clear for intr_in[42]
9	ENABLE_41_CLR	W1C	0h	Enable clear for intr_in[41]
8	ENABLE_40_CLR	W1C	0h	Enable clear for intr_in[40]
7	ENABLE_39_CLR	W1C	0h	Enable clear for intr_in[39]
6	ENABLE_38_CLR	W1C	0h	Enable clear for intr_in[38]
5	ENABLE_37_CLR	W1C	0h	Enable clear for intr_in[37]
4	ENABLE_36_CLR	W1C	0h	Enable clear for intr_in[36]
3	ENABLE_35_CLR	W1C	0h	Enable clear for intr_in[35]
2	ENABLE_34_CLR	W1C	0h	Enable clear for intr_in[34]
1	ENABLE_33_CLR	W1C	0h	Enable clear for intr_in[33]
0	ENABLE_32_CLR	W1C	0h	Enable clear for intr_in[32]

29 ICSS_INTC_ENABLE_CLR_REG2 Register (Offset = 388h) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG2 is shown in Figure 14-3493 and described in Table 14-7065.

Return to Summary Table.

Enable Clear Register 2

Table 14-10556. ICSS_INTC_ENABLE_CLR_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0388h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0388h

Figure 14-3493. ICSS_INTC_ENABLE_CLR_REG2 Register

31	30	29	28	27	26	25	24
ENABLE_95_CLR	ENABLE_94_CLR	ENABLE_93_CLR	ENABLE_92_CLR	ENABLE_91_CLR	ENABLE_90_CLR	ENABLE_89_CLR	ENABLE_88_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_87_CLR	ENABLE_86_CLR	ENABLE_85_CLR	ENABLE_84_CLR	ENABLE_83_CLR	ENABLE_82_CLR	ENABLE_81_CLR	ENABLE_80_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_79_CLR	ENABLE_78_CLR	ENABLE_77_CLR	ENABLE_76_CLR	ENABLE_75_CLR	ENABLE_74_CLR	ENABLE_73_CLR	ENABLE_72_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_71_CLR	ENABLE_70_CLR	ENABLE_69_CLR	ENABLE_68_CLR	ENABLE_67_CLR	ENABLE_66_CLR	ENABLE_65_CLR	ENABLE_64_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 14-10558. ICSS_INTC_ENABLE_CLR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_95_CLR	W1C	0h	Enable clear for slv_events_in[31]
30	ENABLE_94_CLR	W1C	0h	Enable clear for slv_events_in[30]
29	ENABLE_93_CLR	W1C	0h	Enable clear for slv_events_in[29]
28	ENABLE_92_CLR	W1C	0h	Enable clear for slv_events_in[28]
27	ENABLE_91_CLR	W1C	0h	Enable clear for slv_events_in[27]
26	ENABLE_90_CLR	W1C	0h	Enable clear for slv_events_in[26]
25	ENABLE_89_CLR	W1C	0h	Enable clear for slv_events_in[25]
24	ENABLE_88_CLR	W1C	0h	Enable clear for slv_events_in[24]
23	ENABLE_87_CLR	W1C	0h	Enable clear for slv_events_in[23]
22	ENABLE_86_CLR	W1C	0h	Enable clear for slv_events_in[22]
21	ENABLE_85_CLR	W1C	0h	Enable clear for slv_events_in[21]
20	ENABLE_84_CLR	W1C	0h	Enable clear for slv_events_in[20]
19	ENABLE_83_CLR	W1C	0h	Enable clear for slv_events_in[19]
18	ENABLE_82_CLR	W1C	0h	Enable clear for slv_events_in[18]
17	ENABLE_81_CLR	W1C	0h	Enable clear for slv_events_in[17]
16	ENABLE_80_CLR	W1C	0h	Enable clear for slv_events_in[16]

Table 14-10558. ICSS_INTC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENABLE_79_CLR	W1C	0h	Enable clear for slv_events_in[15]
14	ENABLE_78_CLR	W1C	0h	Enable clear for slv_events_in[14]
13	ENABLE_77_CLR	W1C	0h	Enable clear for slv_events_in[13]
12	ENABLE_76_CLR	W1C	0h	Enable clear for slv_events_in[12]
11	ENABLE_75_CLR	W1C	0h	Enable clear for slv_events_in[11]
10	ENABLE_74_CLR	W1C	0h	Enable clear for slv_events_in[10]
9	ENABLE_73_CLR	W1C	0h	Enable clear for slv_events_in[9]
8	ENABLE_72_CLR	W1C	0h	Enable clear for slv_events_in[8]
7	ENABLE_71_CLR	W1C	0h	Enable clear for slv_events_in[7]
6	ENABLE_70_CLR	W1C	0h	Enable clear for slv_events_in[6]
5	ENABLE_69_CLR	W1C	0h	Enable clear for slv_events_in[5]
4	ENABLE_68_CLR	W1C	0h	Enable clear for slv_events_in[4]
3	ENABLE_67_CLR	W1C	0h	Enable clear for slv_events_in[3]
2	ENABLE_66_CLR	W1C	0h	Enable clear for slv_events_in[2]
1	ENABLE_65_CLR	W1C	0h	Enable clear for slv_events_in[1]
0	ENABLE_64_CLR	W1C	0h	Enable clear for slv_events_in[0]

30 ICSS_INTC_ENABLE_CLR_REG3 Register (Offset = 38Ch) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG3 is shown in Figure 14-3494 and described in Table 14-7067.

Return to Summary Table.

Enable Clear Register 3

Table 14-10559. ICSS_INTC_ENABLE_CLR_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 038Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 038Ch

Figure 14-3494. ICSS_INTC_ENABLE_CLR_REG3 Register

31	30	29	28	27	26	25	24
ENABLE_127_CLR	ENABLE_126_CLR	ENABLE_125_CLR	ENABLE_124_CLR	ENABLE_123_CLR	ENABLE_122_CLR	ENABLE_121_CLR	ENABLE_120_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_119_CLR	ENABLE_118_CLR	ENABLE_117_CLR	ENABLE_116_CLR	ENABLE_115_CLR	ENABLE_114_CLR	ENABLE_113_CLR	ENABLE_112_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_111_CLR	ENABLE_110_CLR	ENABLE_109_CLR	ENABLE_108_CLR	ENABLE_107_CLR	ENABLE_106_CLR	ENABLE_105_CLR	ENABLE_104_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_103_CLR	ENABLE_102_CLR	ENABLE_101_CLR	ENABLE_100_CLR	ENABLE_99_CLR	ENABLE_98_CLR	ENABLE_97_CLR	ENABLE_96_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 14-10561. ICSS_INTC_ENABLE_CLR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_127_CLR	W1C	0h	Enable clear for slv_events_in[63]
30	ENABLE_126_CLR	W1C	0h	Enable clear for slv_events_in[62]
29	ENABLE_125_CLR	W1C	0h	Enable clear for slv_events_in[61]
28	ENABLE_124_CLR	W1C	0h	Enable clear for slv_events_in[60]
27	ENABLE_123_CLR	W1C	0h	Enable clear for slv_events_in[59]
26	ENABLE_122_CLR	W1C	0h	Enable clear for slv_events_in[58]
25	ENABLE_121_CLR	W1C	0h	Enable clear for slv_events_in[57]
24	ENABLE_120_CLR	W1C	0h	Enable clear for slv_events_in[56]
23	ENABLE_119_CLR	W1C	0h	Enable clear for slv_events_in[55]
22	ENABLE_118_CLR	W1C	0h	Enable clear for slv_events_in[54]
21	ENABLE_117_CLR	W1C	0h	Enable clear for slv_events_in[53]
20	ENABLE_116_CLR	W1C	0h	Enable clear for slv_events_in[52]
19	ENABLE_115_CLR	W1C	0h	Enable clear for slv_events_in[51]
18	ENABLE_114_CLR	W1C	0h	Enable clear for slv_events_in[50]
17	ENABLE_113_CLR	W1C	0h	Enable clear for slv_events_in[49]
16	ENABLE_112_CLR	W1C	0h	Enable clear for slv_events_in[48]

Table 14-10561. ICSS_INTC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENABLE_111_CLR	W1C	0h	Enable clear for slv_events_in[47]
14	ENABLE_110_CLR	W1C	0h	Enable clear for slv_events_in[46]
13	ENABLE_109_CLR	W1C	0h	Enable clear for slv_events_in[45]
12	ENABLE_108_CLR	W1C	0h	Enable clear for slv_events_in[44]
11	ENABLE_107_CLR	W1C	0h	Enable clear for slv_events_in[43]
10	ENABLE_106_CLR	W1C	0h	Enable clear for slv_events_in[42]
9	ENABLE_105_CLR	W1C	0h	Enable clear for slv_events_in[41]
8	ENABLE_104_CLR	W1C	0h	Enable clear for slv_events_in[40]
7	ENABLE_103_CLR	W1C	0h	Enable clear for slv_events_in[39]
6	ENABLE_102_CLR	W1C	0h	Enable clear for slv_events_in[38]
5	ENABLE_101_CLR	W1C	0h	Enable clear for slv_events_in[37]
4	ENABLE_100_CLR	W1C	0h	Enable clear for slv_events_in[36]
3	ENABLE_99_CLR	W1C	0h	Enable clear for slv_events_in[35]
2	ENABLE_98_CLR	W1C	0h	Enable clear for slv_events_in[34]
1	ENABLE_97_CLR	W1C	0h	Enable clear for slv_events_in[33]
0	ENABLE_96_CLR	W1C	0h	Enable clear for slv_events_in[32]

31 ICSS_INTC_ENABLE_CLR_REG4 Register (Offset = 390h) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG4 is shown in Figure 14-3495 and described in Table 14-7069.

Return to Summary Table.

Enable Clear Register 4

Table 14-10562. ICSS_INTC_ENABLE_CLR_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0390h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0390h

Figure 14-3495. ICSS_INTC_ENABLE_CLR_REG4 Register

31	30	29	28	27	26	25	24
ENABLE_159_CLR	ENABLE_158_CLR	ENABLE_157_CLR	ENABLE_156_CLR	ENABLE_155_CLR	ENABLE_154_CLR	ENABLE_153_CLR	ENABLE_152_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_151_CLR	ENABLE_150_CLR	ENABLE_149_CLR	ENABLE_148_CLR	ENABLE_147_CLR	ENABLE_146_CLR	ENABLE_145_CLR	ENABLE_144_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_143_CLR	ENABLE_142_CLR	ENABLE_141_CLR	ENABLE_140_CLR	ENABLE_139_CLR	ENABLE_138_CLR	ENABLE_137_CLR	ENABLE_136_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_135_CLR	ENABLE_134_CLR	ENABLE_133_CLR	ENABLE_132_CLR	ENABLE_131_CLR	ENABLE_130_CLR	ENABLE_129_CLR	ENABLE_128_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; *-n* = value after reset

Table 14-10564. ICSS_INTC_ENABLE_CLR_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_159_CLR	W1C	0h	Enable clear for slv_events_in[95]
30	ENABLE_158_CLR	W1C	0h	Enable clear for slv_events_in[94]
29	ENABLE_157_CLR	W1C	0h	Enable clear for slv_events_in[93]
28	ENABLE_156_CLR	W1C	0h	Enable clear for slv_events_in[92]
27	ENABLE_155_CLR	W1C	0h	Enable clear for slv_events_in[91]
26	ENABLE_154_CLR	W1C	0h	Enable clear for slv_events_in[90]
25	ENABLE_153_CLR	W1C	0h	Enable clear for slv_events_in[89]
24	ENABLE_152_CLR	W1C	0h	Enable clear for slv_events_in[88]
23	ENABLE_151_CLR	W1C	0h	Enable clear for slv_events_in[87]
22	ENABLE_150_CLR	W1C	0h	Enable clear for slv_events_in[86]
21	ENABLE_149_CLR	W1C	0h	Enable clear for slv_events_in[85]
20	ENABLE_148_CLR	W1C	0h	Enable clear for slv_events_in[84]
19	ENABLE_147_CLR	W1C	0h	Enable clear for slv_events_in[83]
18	ENABLE_146_CLR	W1C	0h	Enable clear for slv_events_in[82]
17	ENABLE_145_CLR	W1C	0h	Enable clear for slv_events_in[81]
16	ENABLE_144_CLR	W1C	0h	Enable clear for slv_events_in[80]

Table 14-10564. ICSS_INTC_ENABLE_CLR_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ENABLE_143_CLR	W1C	0h	Enable clear for slv_events_in[79]
14	ENABLE_142_CLR	W1C	0h	Enable clear for slv_events_in[78]
13	ENABLE_141_CLR	W1C	0h	Enable clear for slv_events_in[77]
12	ENABLE_140_CLR	W1C	0h	Enable clear for slv_events_in[76]
11	ENABLE_139_CLR	W1C	0h	Enable clear for slv_events_in[75]
10	ENABLE_138_CLR	W1C	0h	Enable clear for slv_events_in[74]
9	ENABLE_137_CLR	W1C	0h	Enable clear for slv_events_in[73]
8	ENABLE_136_CLR	W1C	0h	Enable clear for slv_events_in[72]
7	ENABLE_135_CLR	W1C	0h	Enable clear for slv_events_in[71]
6	ENABLE_134_CLR	W1C	0h	Enable clear for slv_events_in[70]
5	ENABLE_133_CLR	W1C	0h	Enable clear for slv_events_in[69]
4	ENABLE_132_CLR	W1C	0h	Enable clear for slv_events_in[68]
3	ENABLE_131_CLR	W1C	0h	Enable clear for slv_events_in[67]
2	ENABLE_130_CLR	W1C	0h	Enable clear for slv_events_in[66]
1	ENABLE_129_CLR	W1C	0h	Enable clear for slv_events_in[65]
0	ENABLE_128_CLR	W1C	0h	Enable clear for slv_events_in[64]

32 ICSS_INTC_CH_MAP_REG0 Register (Offset = 400h) [reset = X]

ICSS_INTC_CH_MAP_REG0 is shown in Figure 14-3496 and described in Table 14-7071.

Return to Summary Table.

Interrupt Channel Map Register for 0 to 0+3

Table 14-10565. ICSS_INTC_CH_MAP_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0400h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0400h

Figure 14-3496. ICSS_INTC_CH_MAP_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_3					RESERVED			CH_MAP_2				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_1					RESERVED			CH_MAP_0				
R/W-X			R/W-0h					R/W-X			W-0h				

LEGEND: R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10567. ICSS_INTC_CH_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_3	R/W	0h	Interrupt Channel Map for intr_in[3]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_2	R/W	0h	Interrupt Channel Map for intr_in[2]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_1	R/W	0h	Interrupt Channel Map for intr_in[1]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_0	W	0h	Interrupt Channel Map for intr_in[0]

33 ICSS_INTC_CH_MAP_REG1 Register (Offset = 404h) [reset = X]

ICSS_INTC_CH_MAP_REG1 is shown in Figure 14-3497 and described in Table 14-7073.

Return to Summary Table.

Interrupt Channel Map Register for 4 to 4+3

Table 14-10568. ICSS_INTC_CH_MAP_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0404h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0404h

Figure 14-3497. ICSS_INTC_CH_MAP_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_7					RESERVED			CH_MAP_6				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_5					RESERVED			CH_MAP_4				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10570. ICSS_INTC_CH_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_7	R/W	0h	Interrupt Channel Map for intr_in[7]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_6	R/W	0h	Interrupt Channel Map for intr_in[6]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_5	R/W	0h	Interrupt Channel Map for intr_in[5]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_4	R/W	0h	Interrupt Channel Map for intr_in[4]

34 ICSS_INTC_CH_MAP_REG2 Register (Offset = 408h) [reset = X]

ICSS_INTC_CH_MAP_REG2 is shown in Figure 14-3498 and described in Table 14-7075.

Return to Summary Table.

Interrupt Channel Map Register for 8 to 8+3

Table 14-10571. ICSS_INTC_CH_MAP_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0408h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0408h

Figure 14-3498. ICSS_INTC_CH_MAP_REG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_11					RESERVED			CH_MAP_10				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_9					RESERVED			CH_MAP_8				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10573. ICSS_INTC_CH_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_11	R/W	0h	Interrupt Channel Map for intr_in[11]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_10	R/W	0h	Interrupt Channel Map for intr_in[10]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_9	R/W	0h	Interrupt Channel Map for intr_in[9]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_8	R/W	0h	Interrupt Channel Map for intr_in[8]

35 ICSS_INTC_CH_MAP_REG3 Register (Offset = 40Ch) [reset = X]

ICSS_INTC_CH_MAP_REG3 is shown in Figure 14-3499 and described in Table 14-7077.

Return to Summary Table.

Interrupt Channel Map Register for 12 to 12+3

Table 14-10574. ICSS_INTC_CH_MAP_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 040Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 040Ch

Figure 14-3499. ICSS_INTC_CH_MAP_REG3 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_15</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_14</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_13</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_12</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10576. ICSS_INTC_CH_MAP_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_15	R/W	0h	Interrupt Channel Map for intr_in[15]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_14	R/W	0h	Interrupt Channel Map for intr_in[14]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_13	R/W	0h	Interrupt Channel Map for intr_in[13]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_12	R/W	0h	Interrupt Channel Map for intr_in[12]

36 ICSS_INTC_CH_MAP_REG4 Register (Offset = 410h) [reset = X]

ICSS_INTC_CH_MAP_REG4 is shown in Figure 14-3500 and described in Table 14-7079.

Return to Summary Table.

Interrupt Channel Map Register for 16 to 16+3

Table 14-10577. ICSS_INTC_CH_MAP_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0410h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0410h

Figure 14-3500. ICSS_INTC_CH_MAP_REG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_19					RESERVED			CH_MAP_18				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_17					RESERVED			CH_MAP_16				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10579. ICSS_INTC_CH_MAP_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_19	R/W	0h	Interrupt Channel Map for intr_in[19]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_18	R/W	0h	Interrupt Channel Map for intr_in[18]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_17	R/W	0h	Interrupt Channel Map for intr_in[17]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_16	R/W	0h	Interrupt Channel Map for intr_in[16]

37 ICSS_INTC_CH_MAP_REG5 Register (Offset = 414h) [reset = X]

ICSS_INTC_CH_MAP_REG5 is shown in Figure 14-3501 and described in Table 14-7081.

Return to Summary Table.

Interrupt Channel Map Register for 20 to 20+3

Table 14-10580. ICSS_INTC_CH_MAP_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0414h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0414h

Figure 14-3501. ICSS_INTC_CH_MAP_REG5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_23					RESERVED			CH_MAP_22				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_21					RESERVED			CH_MAP_20				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10582. ICSS_INTC_CH_MAP_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_23	R/W	0h	Interrupt Channel Map for intr_in[23]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_22	R/W	0h	Interrupt Channel Map for intr_in[22]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_21	R/W	0h	Interrupt Channel Map for intr_in[21]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_20	R/W	0h	Interrupt Channel Map for intr_in[20]

38 ICSS_INTC_CH_MAP_REG6 Register (Offset = 418h) [reset = X]

ICSS_INTC_CH_MAP_REG6 is shown in Figure 14-3502 and described in Table 14-7083.

Return to Summary Table.

Interrupt Channel Map Register for 24 to 24+3

Table 14-10583. ICSS_INTC_CH_MAP_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0418h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0418h

Figure 14-3502. ICSS_INTC_CH_MAP_REG6 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_27</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_26</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_25</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_24</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10585. ICSS_INTC_CH_MAP_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_27	R/W	0h	Interrupt Channel Map for intr_in[27]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_26	R/W	0h	Interrupt Channel Map for intr_in[26]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_25	R/W	0h	Interrupt Channel Map for intr_in[25]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_24	R/W	0h	Interrupt Channel Map for intr_in[24]

39 ICSS_INTC_CH_MAP_REG7 Register (Offset = 41Ch) [reset = X]

ICSS_INTC_CH_MAP_REG7 is shown in Figure 14-3503 and described in Table 14-7085.

Return to Summary Table.

Interrupt Channel Map Register for 28 to 28+3

Table 14-10586. ICSS_INTC_CH_MAP_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 041Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 041Ch

Figure 14-3503. ICSS_INTC_CH_MAP_REG7 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_31</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_30</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_29</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_28</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10588. ICSS_INTC_CH_MAP_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_31	R/W	0h	Interrupt Channel Map for intr_in[31]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_30	R/W	0h	Interrupt Channel Map for intr_in[30]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_29	R/W	0h	Interrupt Channel Map for intr_in[29]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_28	R/W	0h	Interrupt Channel Map for intr_in[28]

40 ICSS_INTC_CH_MAP_REG8 Register (Offset = 420h) [reset = X]

ICSS_INTC_CH_MAP_REG8 is shown in Figure 14-3504 and described in Table 14-7087.

Return to Summary Table.

Interrupt Channel Map Register for 32 to 32+3

Table 14-10589. ICSS_INTC_CH_MAP_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0420h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0420h

Figure 14-3504. ICSS_INTC_CH_MAP_REG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_35					RESERVED			CH_MAP_34				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_33					RESERVED			CH_MAP_32				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10591. ICSS_INTC_CH_MAP_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_35	R/W	0h	Interrupt Channel Map for intr_in[35]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_34	R/W	0h	Interrupt Channel Map for intr_in[34]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_33	R/W	0h	Interrupt Channel Map for intr_in[33]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_32	R/W	0h	Interrupt Channel Map for intr_in[32]

41 ICSS_INTC_CH_MAP_REG9 Register (Offset = 424h) [reset = X]

ICSS_INTC_CH_MAP_REG9 is shown in Figure 14-3505 and described in Table 14-7089.

Return to Summary Table.

Interrupt Channel Map Register for 36 to 36+3

Table 14-10592. ICSS_INTC_CH_MAP_REG9 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0424h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0424h

Figure 14-3505. ICSS_INTC_CH_MAP_REG9 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_39</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_38</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_37</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_36</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10594. ICSS_INTC_CH_MAP_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_39	R/W	0h	Interrupt Channel Map for intr_in[39]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_38	R/W	0h	Interrupt Channel Map for intr_in[38]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_37	R/W	0h	Interrupt Channel Map for intr_in[37]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_36	R/W	0h	Interrupt Channel Map for intr_in[36]

42 ICSS_INTC_CH_MAP_REG10 Register (Offset = 428h) [reset = X]

ICSS_INTC_CH_MAP_REG10 is shown in Figure 14-3506 and described in Table 14-7091.

Return to Summary Table.

Interrupt Channel Map Register for 40 to 40+3

Table 14-10595. ICSS_INTC_CH_MAP_REG10 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0428h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0428h

Figure 14-3506. ICSS_INTC_CH_MAP_REG10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_43					RESERVED			CH_MAP_42				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_41					RESERVED			CH_MAP_40				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10597. ICSS_INTC_CH_MAP_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_43	R/W	0h	Interrupt Channel Map for intr_in[43]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_42	R/W	0h	Interrupt Channel Map for intr_in[42]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_41	R/W	0h	Interrupt Channel Map for intr_in[41]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_40	R/W	0h	Interrupt Channel Map for intr_in[40]

43 ICSS_INTC_CH_MAP_REG11 Register (Offset = 42Ch) [reset = X]

ICSS_INTC_CH_MAP_REG11 is shown in Figure 14-3507 and described in Table 14-7093.

Return to Summary Table.

Interrupt Channel Map Register for 44 to 44+3

Table 14-10598. ICSS_INTC_CH_MAP_REG11 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 042Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 042Ch

Figure 14-3507. ICSS_INTC_CH_MAP_REG11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_47					RESERVED			CH_MAP_46				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_45					RESERVED			CH_MAP_44				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10600. ICSS_INTC_CH_MAP_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_47	R/W	0h	Interrupt Channel Map for intr_in[47]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_46	R/W	0h	Interrupt Channel Map for intr_in[46]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_45	R/W	0h	Interrupt Channel Map for intr_in[45]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_44	R/W	0h	Interrupt Channel Map for intr_in[44]

44 ICSS_INTC_CH_MAP_REG12 Register (Offset = 430h) [reset = X]

ICSS_INTC_CH_MAP_REG12 is shown in Figure 14-3508 and described in Table 14-7095.

Return to Summary Table.

Interrupt Channel Map Register for 48 to 48+3

Table 14-10601. ICSS_INTC_CH_MAP_REG12 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0430h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0430h

Figure 14-3508. ICSS_INTC_CH_MAP_REG12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_51					RESERVED			CH_MAP_50				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_49					RESERVED			CH_MAP_48				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10603. ICSS_INTC_CH_MAP_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_51	R/W	0h	Interrupt Channel Map for intr_in[51]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_50	R/W	0h	Interrupt Channel Map for intr_in[50]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_49	R/W	0h	Interrupt Channel Map for intr_in[49]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_48	R/W	0h	Interrupt Channel Map for intr_in[48]

45 ICSS_INTC_CH_MAP_REG13 Register (Offset = 434h) [reset = X]

ICSS_INTC_CH_MAP_REG13 is shown in Figure 14-3509 and described in Table 14-7097.

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Interrupt Channel Map Register for 52 to 52+3

Table 14-10604. ICSS_INTC_CH_MAP_REG13 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0434h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0434h

Figure 14-3509. ICSS_INTC_CH_MAP_REG13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_55					RESERVED			CH_MAP_54				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_53					RESERVED			CH_MAP_52				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10606. ICSS_INTC_CH_MAP_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_55	R/W	0h	Interrupt Channel Map for intr_in[55]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_54	R/W	0h	Interrupt Channel Map for intr_in[54]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_53	R/W	0h	Interrupt Channel Map for intr_in[53]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_52	R/W	0h	Interrupt Channel Map for intr_in[52]

46 ICSS_INTC_CH_MAP_REG14 Register (Offset = 438h) [reset = X]

ICSS_INTC_CH_MAP_REG14 is shown in Figure 14-3510 and described in Table 14-7099.

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Interrupt Channel Map Register for 56 to 56+3

Table 14-10607. ICSS_INTC_CH_MAP_REG14 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0438h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0438h

Figure 14-3510. ICSS_INTC_CH_MAP_REG14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_59					RESERVED			CH_MAP_58				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_57					RESERVED			CH_MAP_56				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10609. ICSS_INTC_CH_MAP_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_59	R/W	0h	Interrupt Channel Map for intr_in[59]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_58	R/W	0h	Interrupt Channel Map for intr_in[58]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_57	R/W	0h	Interrupt Channel Map for intr_in[57]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_56	R/W	0h	Interrupt Channel Map for intr_in[56]

47 ICSS_INTC_CH_MAP_REG15 Register (Offset = 43Ch) [reset = X]

ICSS_INTC_CH_MAP_REG15 is shown in Figure 14-3511 and described in Table 14-7101.

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Interrupt Channel Map Register for 60 to 60+3

Table 14-10610. ICSS_INTC_CH_MAP_REG15 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 043Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 043Ch

Figure 14-3511. ICSS_INTC_CH_MAP_REG15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_63					RESERVED			CH_MAP_62				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_61					RESERVED			CH_MAP_60				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10612. ICSS_INTC_CH_MAP_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_63	R/W	0h	Interrupt Channel Map for intr_in[63]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_62	R/W	0h	Interrupt Channel Map for intr_in[62]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_61	R/W	0h	Interrupt Channel Map for intr_in[61]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_60	R/W	0h	Interrupt Channel Map for intr_in[60]

48 ICSS_INTC_CH_MAP_REG16 Register (Offset = 440h) [reset = X]

ICSS_INTC_CH_MAP_REG16 is shown in Figure 14-3512 and described in Table 14-7103.

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Interrupt Channel Map Register for 64 to 64+3

Table 14-10613. ICSS_INTC_CH_MAP_REG16 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0440h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0440h

Figure 14-3512. ICSS_INTC_CH_MAP_REG16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_67					RESERVED			CH_MAP_66				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_65					RESERVED			CH_MAP_64				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10615. ICSS_INTC_CH_MAP_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_67	R/W	0h	Interrupt Channel Map for slv_events_in[3]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_66	R/W	0h	Interrupt Channel Map for slv_events_in[2]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_65	R/W	0h	Interrupt Channel Map for slv_events_in[1]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_64	R/W	0h	Interrupt Channel Map for slv_events_in[0]

49 ICSS_INTC_CH_MAP_REG17 Register (Offset = 444h) [reset = X]

ICSS_INTC_CH_MAP_REG17 is shown in Figure 14-3513 and described in Table 14-7105.

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Interrupt Channel Map Register for 68 to 68+3

Table 14-10616. ICSS_INTC_CH_MAP_REG17 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0444h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0444h

Figure 14-3513. ICSS_INTC_CH_MAP_REG17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_71					RESERVED			CH_MAP_70				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_69					RESERVED			CH_MAP_68				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10618. ICSS_INTC_CH_MAP_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_71	R/W	0h	Interrupt Channel Map for slv_events_in[7]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_70	R/W	0h	Interrupt Channel Map for slv_events_in[6]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_69	R/W	0h	Interrupt Channel Map for slv_events_in[5]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_68	R/W	0h	Interrupt Channel Map for slv_events_in[4]

50 ICSS_INTC_CH_MAP_REG18 Register (Offset = 448h) [reset = X]

ICSS_INTC_CH_MAP_REG18 is shown in Figure 14-3514 and described in Table 14-7107.

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Interrupt Channel Map Register for 72 to 72+3

Table 14-10619. ICSS_INTC_CH_MAP_REG18 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0448h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0448h

Figure 14-3514. ICSS_INTC_CH_MAP_REG18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_75					RESERVED			CH_MAP_74				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_73					RESERVED			CH_MAP_72				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10621. ICSS_INTC_CH_MAP_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_75	R/W	0h	Interrupt Channel Map for slv_events_in[11]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_74	R/W	0h	Interrupt Channel Map for slv_events_in[10]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_73	R/W	0h	Interrupt Channel Map for slv_events_in[9]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_72	R/W	0h	Interrupt Channel Map for slv_events_in[8]

51 ICSS_INTC_CH_MAP_REG19 Register (Offset = 44Ch) [reset = X]

ICSS_INTC_CH_MAP_REG19 is shown in Figure 14-3515 and described in Table 14-7109.

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Interrupt Channel Map Register for 76 to 76+3

Table 14-10622. ICSS_INTC_CH_MAP_REG19 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 044Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 044Ch

Figure 14-3515. ICSS_INTC_CH_MAP_REG19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_79					RESERVED			CH_MAP_78				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_77					RESERVED			CH_MAP_76				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10624. ICSS_INTC_CH_MAP_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_79	R/W	0h	Interrupt Channel Map for slv_events_in[15]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_78	R/W	0h	Interrupt Channel Map for slv_events_in[14]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_77	R/W	0h	Interrupt Channel Map for slv_events_in[13]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_76	R/W	0h	Interrupt Channel Map for slv_events_in[12]

52 ICSS_INTC_CH_MAP_REG20 Register (Offset = 450h) [reset = X]

ICSS_INTC_CH_MAP_REG20 is shown in Figure 14-3516 and described in Table 14-7111.

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Interrupt Channel Map Register for 80 to 80+3

Table 14-10625. ICSS_INTC_CH_MAP_REG20 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0450h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0450h

Figure 14-3516. ICSS_INTC_CH_MAP_REG20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_83					RESERVED			CH_MAP_82				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_81					RESERVED			CH_MAP_80				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10627. ICSS_INTC_CH_MAP_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_83	R/W	0h	Interrupt Channel Map for slv_events_in[19]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_82	R/W	0h	Interrupt Channel Map for slv_events_in[18]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_81	R/W	0h	Interrupt Channel Map for slv_events_in[17]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_80	R/W	0h	Interrupt Channel Map for slv_events_in[16]

53 ICSS_INTC_CH_MAP_REG21 Register (Offset = 454h) [reset = X]

ICSS_INTC_CH_MAP_REG21 is shown in Figure 14-3517 and described in Table 14-7113.

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Interrupt Channel Map Register for 84 to 84+3

Table 14-10628. ICSS_INTC_CH_MAP_REG21 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0454h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0454h

Figure 14-3517. ICSS_INTC_CH_MAP_REG21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_87					RESERVED			CH_MAP_86				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_85					RESERVED			CH_MAP_84				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10630. ICSS_INTC_CH_MAP_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_87	R/W	0h	Interrupt Channel Map for slv_events_in[23]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_86	R/W	0h	Interrupt Channel Map for slv_events_in[22]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_85	R/W	0h	Interrupt Channel Map for slv_events_in[21]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_84	R/W	0h	Interrupt Channel Map for slv_events_in[20]

54 ICSS_INTC_CH_MAP_REG22 Register (Offset = 458h) [reset = X]

ICSS_INTC_CH_MAP_REG22 is shown in Figure 14-3518 and described in Table 14-7115.

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Interrupt Channel Map Register for 88 to 88+3

Table 14-10631. ICSS_INTC_CH_MAP_REG22 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0458h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0458h

Figure 14-3518. ICSS_INTC_CH_MAP_REG22 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_91					RESERVED			CH_MAP_90				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_89					RESERVED			CH_MAP_88				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10633. ICSS_INTC_CH_MAP_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_91	R/W	0h	Interrupt Channel Map for slv_events_in[27]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_90	R/W	0h	Interrupt Channel Map for slv_events_in[26]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_89	R/W	0h	Interrupt Channel Map for slv_events_in[25]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_88	R/W	0h	Interrupt Channel Map for slv_events_in[24]

55 ICSS_INTC_CH_MAP_REG23 Register (Offset = 45Ch) [reset = X]

ICSS_INTC_CH_MAP_REG23 is shown in Figure 14-3519 and described in Table 14-7117.

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Interrupt Channel Map Register for 92 to 92+3

Table 14-10634. ICSS_INTC_CH_MAP_REG23 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 045Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 045Ch

Figure 14-3519. ICSS_INTC_CH_MAP_REG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_95					RESERVED			CH_MAP_94				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_93					RESERVED			CH_MAP_92				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10636. ICSS_INTC_CH_MAP_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_95	R/W	0h	Interrupt Channel Map for slv_events_in[31]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_94	R/W	0h	Interrupt Channel Map for slv_events_in[30]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_93	R/W	0h	Interrupt Channel Map for slv_events_in[29]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_92	R/W	0h	Interrupt Channel Map for slv_events_in[28]

56 ICSS_INTC_CH_MAP_REG24 Register (Offset = 460h) [reset = X]

ICSS_INTC_CH_MAP_REG24 is shown in Figure 14-3520 and described in Table 14-7119.

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Interrupt Channel Map Register for 96 to 96+3

Table 14-10637. ICSS_INTC_CH_MAP_REG24 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0460h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0460h

Figure 14-3520. ICSS_INTC_CH_MAP_REG24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_99					RESERVED			CH_MAP_98				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_97					RESERVED			CH_MAP_96				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10639. ICSS_INTC_CH_MAP_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_99	R/W	0h	Interrupt Channel Map for slv_events_in[35]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_98	R/W	0h	Interrupt Channel Map for slv_events_in[34]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_97	R/W	0h	Interrupt Channel Map for slv_events_in[33]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_96	R/W	0h	Interrupt Channel Map for slv_events_in[32]

57 ICSS_INTC_CH_MAP_REG25 Register (Offset = 464h) [reset = X]

ICSS_INTC_CH_MAP_REG25 is shown in Figure 14-3521 and described in Table 14-7121.

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Interrupt Channel Map Register for 100 to 100+3

Table 14-10640. ICSS_INTC_CH_MAP_REG25 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0464h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0464h

Figure 14-3521. ICSS_INTC_CH_MAP_REG25 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_103					RESERVED			CH_MAP_102				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_101					RESERVED			CH_MAP_100				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10642. ICSS_INTC_CH_MAP_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_103	R/W	0h	Interrupt Channel Map for slv_events_in[39]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_102	R/W	0h	Interrupt Channel Map for slv_events_in[38]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_101	R/W	0h	Interrupt Channel Map for slv_events_in[37]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_100	R/W	0h	Interrupt Channel Map for slv_events_in[36]

58 ICSS_INTC_CH_MAP_REG26 Register (Offset = 468h) [reset = X]

ICSS_INTC_CH_MAP_REG26 is shown in Figure 14-3522 and described in Table 14-7123.

Return to Summary Table.

Interrupt Channel Map Register for 104 to 104+3

Table 14-10643. ICSS_INTC_CH_MAP_REG26 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0468h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0468h

Figure 14-3522. ICSS_INTC_CH_MAP_REG26 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_107					RESERVED			CH_MAP_106				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_105					RESERVED			CH_MAP_104				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10645. ICSS_INTC_CH_MAP_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_107	R/W	0h	Interrupt Channel Map for slv_events_in[43]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_106	R/W	0h	Interrupt Channel Map for slv_events_in[42]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_105	R/W	0h	Interrupt Channel Map for slv_events_in[41]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_104	R/W	0h	Interrupt Channel Map for slv_events_in[40]

59 ICSS_INTC_CH_MAP_REG27 Register (Offset = 46Ch) [reset = X]

ICSS_INTC_CH_MAP_REG27 is shown in Figure 14-3523 and described in Table 14-7125.

Return to Summary Table.

Interrupt Channel Map Register for 108 to 108+3

Table 14-10646. ICSS_INTC_CH_MAP_REG27 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 046Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 046Ch

Figure 14-3523. ICSS_INTC_CH_MAP_REG27 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_111					RESERVED			CH_MAP_110				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_109					RESERVED			CH_MAP_108				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10648. ICSS_INTC_CH_MAP_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_111	R/W	0h	Interrupt Channel Map for slv_events_in[47]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_110	R/W	0h	Interrupt Channel Map for slv_events_in[46]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_109	R/W	0h	Interrupt Channel Map for slv_events_in[45]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_108	R/W	0h	Interrupt Channel Map for slv_events_in[44]

60 ICSS_INTC_CH_MAP_REG28 Register (Offset = 470h) [reset = X]

ICSS_INTC_CH_MAP_REG28 is shown in Figure 14-3524 and described in Table 14-7127.

Return to Summary Table.

Interrupt Channel Map Register for 112 to 112+3

Table 14-10649. ICSS_INTC_CH_MAP_REG28 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0470h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0470h

Figure 14-3524. ICSS_INTC_CH_MAP_REG28 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_115					RESERVED			CH_MAP_114				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_113					RESERVED			CH_MAP_112				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10651. ICSS_INTC_CH_MAP_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_115	R/W	0h	Interrupt Channel Map for slv_events_in[51]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_114	R/W	0h	Interrupt Channel Map for slv_events_in[50]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_113	R/W	0h	Interrupt Channel Map for slv_events_in[49]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_112	R/W	0h	Interrupt Channel Map for slv_events_in[48]

61 ICSS_INTC_CH_MAP_REG29 Register (Offset = 474h) [reset = X]

ICSS_INTC_CH_MAP_REG29 is shown in Figure 14-3525 and described in Table 14-7129.

Return to Summary Table.

Interrupt Channel Map Register for 116 to 116+3

Table 14-10652. ICSS_INTC_CH_MAP_REG29 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0474h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0474h

Figure 14-3525. ICSS_INTC_CH_MAP_REG29 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_119					RESERVED			CH_MAP_118				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_117					RESERVED			CH_MAP_116				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10654. ICSS_INTC_CH_MAP_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_119	R/W	0h	Interrupt Channel Map for slv_events_in[55]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_118	R/W	0h	Interrupt Channel Map for slv_events_in[54]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_117	R/W	0h	Interrupt Channel Map for slv_events_in[53]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_116	R/W	0h	Interrupt Channel Map for slv_events_in[52]

62 ICSS_INTC_CH_MAP_REG30 Register (Offset = 478h) [reset = X]

ICSS_INTC_CH_MAP_REG30 is shown in Figure 14-3526 and described in Table 14-7131.

Return to Summary Table.

Interrupt Channel Map Register for 120 to 120+3

Table 14-10655. ICSS_INTC_CH_MAP_REG30 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0478h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0478h

Figure 14-3526. ICSS_INTC_CH_MAP_REG30 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_123					RESERVED			CH_MAP_122				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_121					RESERVED			CH_MAP_120				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10657. ICSS_INTC_CH_MAP_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_123	R/W	0h	Interrupt Channel Map for slv_events_in[59]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_122	R/W	0h	Interrupt Channel Map for slv_events_in[58]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_121	R/W	0h	Interrupt Channel Map for slv_events_in[57]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_120	R/W	0h	Interrupt Channel Map for slv_events_in[56]

63 ICSS_INTC_CH_MAP_REG31 Register (Offset = 47Ch) [reset = X]

ICSS_INTC_CH_MAP_REG31 is shown in Figure 14-3527 and described in Table 14-7133.

Return to Summary Table.

Interrupt Channel Map Register for 124 to 124+3

Table 14-10658. ICSS_INTC_CH_MAP_REG31 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 047Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 047Ch

Figure 14-3527. ICSS_INTC_CH_MAP_REG31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_127					RESERVED			CH_MAP_126				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_125					RESERVED			CH_MAP_124				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10660. ICSS_INTC_CH_MAP_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_127	R/W	0h	Interrupt Channel Map for slv_events_in[63]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_126	R/W	0h	Interrupt Channel Map for slv_events_in[62]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_125	R/W	0h	Interrupt Channel Map for slv_events_in[61]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_124	R/W	0h	Interrupt Channel Map for slv_events_in[60]

64 ICSS_INTC_CH_MAP_REG32 Register (Offset = 480h) [reset = X]

ICSS_INTC_CH_MAP_REG32 is shown in Figure 14-3528 and described in Table 14-7135.

Return to Summary Table.

Interrupt Channel Map Register for 128 to 128+3

Table 14-10661. ICSS_INTC_CH_MAP_REG32 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0480h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0480h

Figure 14-3528. ICSS_INTC_CH_MAP_REG32 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_131					RESERVED			CH_MAP_130				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH_MAP_129					RESERVED			CH_MAP_128				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10663. ICSS_INTC_CH_MAP_REG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_131	R/W	0h	Interrupt Channel Map for slv_events_in[67]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_130	R/W	0h	Interrupt Channel Map for slv_events_in[66]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_129	R/W	0h	Interrupt Channel Map for slv_events_in[65]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_128	R/W	0h	Interrupt Channel Map for slv_events_in[64]

65 ICSS_INTC_CH_MAP_REG33 Register (Offset = 484h) [reset = X]

ICSS_INTC_CH_MAP_REG33 is shown in Figure 14-3529 and described in Table 14-7137.

Return to Summary Table.

Interrupt Channel Map Register for 132 to 132+3

Table 14-10664. ICSS_INTC_CH_MAP_REG33 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0484h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0484h

Figure 14-3529. ICSS_INTC_CH_MAP_REG33 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_135					RESERVED			CH_MAP_134				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_133					RESERVED			CH_MAP_132				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10666. ICSS_INTC_CH_MAP_REG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_135	R/W	0h	Interrupt Channel Map for slv_events_in[71]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_134	R/W	0h	Interrupt Channel Map for slv_events_in[70]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_133	R/W	0h	Interrupt Channel Map for slv_events_in[69]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_132	R/W	0h	Interrupt Channel Map for slv_events_in[68]

66 ICSS_INTC_CH_MAP_REG34 Register (Offset = 488h) [reset = X]

ICSS_INTC_CH_MAP_REG34 is shown in Figure 14-3530 and described in Table 14-7139.

Return to Summary Table.

Interrupt Channel Map Register for 136 to 136+3

Table 14-10667. ICSS_INTC_CH_MAP_REG34 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0488h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0488h

Figure 14-3530. ICSS_INTC_CH_MAP_REG34 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_139					RESERVED			CH_MAP_138				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_137					RESERVED			CH_MAP_136				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10669. ICSS_INTC_CH_MAP_REG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_139	R/W	0h	Interrupt Channel Map for slv_events_in[75]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_138	R/W	0h	Interrupt Channel Map for slv_events_in[74]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_137	R/W	0h	Interrupt Channel Map for slv_events_in[73]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_136	R/W	0h	Interrupt Channel Map for slv_events_in[72]

67 ICSS_INTC_CH_MAP_REG35 Register (Offset = 48Ch) [reset = X]

ICSS_INTC_CH_MAP_REG35 is shown in Figure 14-3531 and described in Table 14-7141.

Return to Summary Table.

Interrupt Channel Map Register for 140 to 140+3

Table 14-10670. ICSS_INTC_CH_MAP_REG35 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 048Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 048Ch

Figure 14-3531. ICSS_INTC_CH_MAP_REG35 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_143					RESERVED			CH_MAP_142				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_141					RESERVED			CH_MAP_140				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10672. ICSS_INTC_CH_MAP_REG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_143	R/W	0h	Interrupt Channel Map for slv_events_in[79]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_142	R/W	0h	Interrupt Channel Map for slv_events_in[78]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_141	R/W	0h	Interrupt Channel Map for slv_events_in[77]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_140	R/W	0h	Interrupt Channel Map for slv_events_in[76]

68 ICSS_INTC_CH_MAP_REG36 Register (Offset = 490h) [reset = X]

ICSS_INTC_CH_MAP_REG36 is shown in Figure 14-3532 and described in Table 14-7143.

Return to Summary Table.

Interrupt Channel Map Register for 144 to 144+3

Table 14-10673. ICSS_INTC_CH_MAP_REG36 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0490h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0490h

Figure 14-3532. ICSS_INTC_CH_MAP_REG36 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_147					RESERVED			CH_MAP_146				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_145					RESERVED			CH_MAP_144				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10675. ICSS_INTC_CH_MAP_REG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_147	R/W	0h	Interrupt Channel Map for slv_events_in[83]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_146	R/W	0h	Interrupt Channel Map for slv_events_in[82]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_145	R/W	0h	Interrupt Channel Map for slv_events_in[81]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_144	R/W	0h	Interrupt Channel Map for slv_events_in[80]

69 ICSS_INTC_CH_MAP_REG37 Register (Offset = 494h) [reset = X]

ICSS_INTC_CH_MAP_REG37 is shown in Figure 14-3533 and described in Table 14-7145.

Return to Summary Table.

Interrupt Channel Map Register for 148 to 148+3

Table 14-10676. ICSS_INTC_CH_MAP_REG37 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0494h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0494h

Figure 14-3533. ICSS_INTC_CH_MAP_REG37 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_151					RESERVED			CH_MAP_150				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_149					RESERVED			CH_MAP_148				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10678. ICSS_INTC_CH_MAP_REG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_151	R/W	0h	Interrupt Channel Map for slv_events_in[87]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_150	R/W	0h	Interrupt Channel Map for slv_events_in[86]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_149	R/W	0h	Interrupt Channel Map for slv_events_in[85]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_148	R/W	0h	Interrupt Channel Map for slv_events_in[84]

70 ICSS_INTC_CH_MAP_REG38 Register (Offset = 498h) [reset = X]

ICSS_INTC_CH_MAP_REG38 is shown in Figure 14-3534 and described in Table 14-7147.

Return to Summary Table.

Interrupt Channel Map Register for 152 to 152+3

Table 14-10679. ICSS_INTC_CH_MAP_REG38 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0498h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0498h

Figure 14-3534. ICSS_INTC_CH_MAP_REG38 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_155</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_154</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_153</td><td colspan="3">RESERVED</td><td colspan="5">CH_MAP_152</td></tr>
<tr><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td><td colspan="3">R/W-X</td><td colspan="5">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10681. ICSS_INTC_CH_MAP_REG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_155	R/W	0h	Interrupt Channel Map for slv_events_in[91]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_154	R/W	0h	Interrupt Channel Map for slv_events_in[90]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_153	R/W	0h	Interrupt Channel Map for slv_events_in[89]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_152	R/W	0h	Interrupt Channel Map for slv_events_in[88]

71 ICSS_INTC_CH_MAP_REG39 Register (Offset = 49Ch) [reset = X]

ICSS_INTC_CH_MAP_REG39 is shown in Figure 14-3535 and described in Table 14-7149.

Return to Summary Table.

Interrupt Channel Map Register for 156 to 156+3

Table 14-10682. ICSS_INTC_CH_MAP_REG39 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 049Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 049Ch

Figure 14-3535. ICSS_INTC_CH_MAP_REG39 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			CH_MAP_159					RESERVED			CH_MAP_158				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CH_MAP_157					RESERVED			CH_MAP_156				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10684. ICSS_INTC_CH_MAP_REG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_159	R/W	0h	Interrupt Channel Map for slv_events_in[95]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_158	R/W	0h	Interrupt Channel Map for slv_events_in[94]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_157	R/W	0h	Interrupt Channel Map for slv_events_in[93]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_156	R/W	0h	Interrupt Channel Map for slv_events_in[92]

72 ICSS_INTC_HINT_MAP_REG0 Register (Offset = 800h) [reset = X]

ICSS_INTC_HINT_MAP_REG0 is shown in Figure 14-3536 and described in Table 14-7151.

Return to Summary Table.

Host Interrupt Map Register for 0 to 0+3

Table 14-10685. ICSS_INTC_HINT_MAP_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0800h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0800h

Figure 14-3536. ICSS_INTC_HINT_MAP_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			HINT_MAP_3					RESERVED			HINT_MAP_2				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			HINT_MAP_1					RESERVED			HINT_MAP_0				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10687. ICSS_INTC_HINT_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_3	R/W	0h	Host Interrupt Map for Channel 3
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_2	R/W	0h	Host Interrupt Map for Channel 2
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_1	R/W	0h	Host Interrupt Map for Channel 1
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_0	R/W	0h	Host Interrupt Map for Channel 0

73 ICSS_INTC_HINT_MAP_REG1 Register (Offset = 804h) [reset = X]

ICSS_INTC_HINT_MAP_REG1 is shown in Figure 14-3537 and described in Table 14-7153.

Return to Summary Table.

Host Interrupt Map Register for 4 to 4+3

Table 14-10688. ICSS_INTC_HINT_MAP_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0804h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0804h

Figure 14-3537. ICSS_INTC_HINT_MAP_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			HINT_MAP_7					RESERVED			HINT_MAP_6				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			HINT_MAP_5					RESERVED			HINT_MAP_4				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10690. ICSS_INTC_HINT_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_7	R/W	0h	Host Interrupt Map for Channel 7
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_6	R/W	0h	Host Interrupt Map for Channel 6
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_5	R/W	0h	Host Interrupt Map for Channel 5
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_4	R/W	0h	Host Interrupt Map for Channel 4

74 ICSS_INTC_HINT_MAP_REG2 Register (Offset = 808h) [reset = X]

ICSS_INTC_HINT_MAP_REG2 is shown in Figure 14-3538 and described in Table 14-7155.

Return to Summary Table.

Host Interrupt Map Register for 8 to 8+3

Table 14-10691. ICSS_INTC_HINT_MAP_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0808h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0808h

Figure 14-3538. ICSS_INTC_HINT_MAP_REG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			HINT_MAP_11					RESERVED			HINT_MAP_10				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			HINT_MAP_9					RESERVED			HINT_MAP_8				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10693. ICSS_INTC_HINT_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_11	R/W	0h	Host Interrupt Map for Channel 11
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_10	R/W	0h	Host Interrupt Map for Channel 10
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_9	R/W	0h	Host Interrupt Map for Channel 9
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_8	R/W	0h	Host Interrupt Map for Channel 8

75 ICSS_INTC_HINT_MAP_REG3 Register (Offset = 80Ch) [reset = X]

ICSS_INTC_HINT_MAP_REG3 is shown in Figure 14-3539 and described in Table 14-7157.

Return to Summary Table.

Host Interrupt Map Register for 12 to 12+3

Table 14-10694. ICSS_INTC_HINT_MAP_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 080Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 080Ch

Figure 14-3539. ICSS_INTC_HINT_MAP_REG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			HINT_MAP_15					RESERVED			HINT_MAP_14				
R/W-X			R/W-0h					R/W-X			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			HINT_MAP_13					RESERVED			HINT_MAP_12				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10696. ICSS_INTC_HINT_MAP_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_15	R/W	0h	Host Interrupt Map for Channel 15
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_14	R/W	0h	Host Interrupt Map for Channel 14
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_13	R/W	0h	Host Interrupt Map for Channel 13
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_12	R/W	0h	Host Interrupt Map for Channel 12

76 ICSS_INTC_HINT_MAP_REG4 Register (Offset = 810h) [reset = X]

ICSS_INTC_HINT_MAP_REG4 is shown in Figure 14-3540 and described in Table 14-7159.

Return to Summary Table.

Host Interrupt Map Register for 16 to 16+4

Table 14-10697. ICSS_INTC_HINT_MAP_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0810h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0810h

Figure 14-3540. ICSS_INTC_HINT_MAP_REG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			HINT_MAP_19					RESERVED			HINT_MAP_18				
R/W-X			R/W-0h					R/W-X			R/W-0h				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			HINT_MAP_17					RESERVED			HINT_MAP_16				
R/W-X			R/W-0h					R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10699. ICSS_INTC_HINT_MAP_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_19	R/W	0h	Host Interrupt Map for Channel 19
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_18	R/W	0h	Host Interrupt Map for Channel 18
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_17	R/W	0h	Host Interrupt Map for Channel 17
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_16	R/W	0h	Host Interrupt Map for Channel 16

77 ICSS_INTC_PRI_HINT_REG0 Register (Offset = 900h) [reset = X]

ICSS_INTC_PRI_HINT_REG0 is shown in Figure 14-3541 and described in Table 14-7161.

Return to Summary Table.

Host Int 0 Prioritized Interrupt Register

Table 14-10700. ICSS_INTC_PRI_HINT_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0900h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0900h

Figure 14-3541. ICSS_INTC_PRI_HINT_REG0 Register

31	30	29	28	27	26	25	24
NONE_HINT_0	RESERVED						
R-1h	R-X						

23	22	21	20	19	18	17	16
RESERVED							
R-X							

15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_0	
R-X						R-0h	

7	6	5	4	3	2	1	0
PRI_HINT_0							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10702. ICSS_INTC_PRI_HINT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_0	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_0	R	0h	Host Int 0 Prioritized Interrupt

78 ICSS_INTC_PRI_HINT_REG1 Register (Offset = 904h) [reset = X]

ICSS_INTC_PRI_HINT_REG1 is shown in Figure 14-3542 and described in Table 14-7163.

Return to Summary Table.

Host Int 1 Prioritized Interrupt Register

Table 14-10703. ICSS_INTC_PRI_HINT_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0904h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0904h

Figure 14-3542. ICSS_INTC_PRI_HINT_REG1 Register

31	30	29	28	27	26	25	24
NONE_HINT_1	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_1	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_1							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10705. ICSS_INTC_PRI_HINT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_1	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_1	R	0h	Host Int 1 Prioritized Interrupt

79 ICSS_INTC_PRI_HINT_REG2 Register (Offset = 908h) [reset = X]

ICSS_INTC_PRI_HINT_REG2 is shown in Figure 14-3543 and described in Table 14-7165.

Return to Summary Table.

Host Int 2 Prioritized Interrupt Register

Table 14-10706. ICSS_INTC_PRI_HINT_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0908h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0908h

Figure 14-3543. ICSS_INTC_PRI_HINT_REG2 Register

31	30	29	28	27	26	25	24
NONE_HINT_2	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_2	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_2							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10708. ICSS_INTC_PRI_HINT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_2	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_2	R	0h	Host Int 2 Prioritized Interrupt

80 ICSS_INTC_PRI_HINT_REG3 Register (Offset = 90Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG3 is shown in Figure 14-3544 and described in Table 14-7167.

Return to Summary Table.

Host Int 3 Prioritized Interrupt Register

Table 14-10709. ICSS_INTC_PRI_HINT_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 090Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 090Ch

Figure 14-3544. ICSS_INTC_PRI_HINT_REG3 Register

31	30	29	28	27	26	25	24
NONE_HINT_3	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_3	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_3							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10711. ICSS_INTC_PRI_HINT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_3	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_3	R	0h	Host Int 3 Prioritized Interrupt

81 ICSS_INTC_PRI_HINT_REG4 Register (Offset = 910h) [reset = X]

ICSS_INTC_PRI_HINT_REG4 is shown in Figure 14-3545 and described in Table 14-7169.

Return to Summary Table.

Host Int 4 Prioritized Interrupt Register

Table 14-10712. ICSS_INTC_PRI_HINT_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0910h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0910h

Figure 14-3545. ICSS_INTC_PRI_HINT_REG4 Register

31	30	29	28	27	26	25	24
NONE_HINT_4	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_4	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_4							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10714. ICSS_INTC_PRI_HINT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_4	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_4	R	0h	Host Int 4 Prioritized Interrupt

82 ICSS_INTC_PRI_HINT_REG5 Register (Offset = 914h) [reset = X]

ICSS_INTC_PRI_HINT_REG5 is shown in Figure 14-3546 and described in Table 14-7171.

Return to Summary Table.

Host Int 5 Prioritized Interrupt Register

Table 14-10715. ICSS_INTC_PRI_HINT_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0914h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0914h

Figure 14-3546. ICSS_INTC_PRI_HINT_REG5 Register

31	30	29	28	27	26	25	24
NONE_HINT_5	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_5	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_5							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10717. ICSS_INTC_PRI_HINT_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_5	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_5	R	0h	Host Int 5 Prioritized Interrupt

83 ICSS_INTC_PRI_HINT_REG6 Register (Offset = 918h) [reset = X]

ICSS_INTC_PRI_HINT_REG6 is shown in Figure 14-3547 and described in Table 14-7173.

Return to Summary Table.

Host Int 6 Prioritized Interrupt Register

Table 14-10718. ICSS_INTC_PRI_HINT_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0918h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0918h

Figure 14-3547. ICSS_INTC_PRI_HINT_REG6 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>NONE_HINT_6</td><td colspan="7">RESERVED</td></tr>
<tr><td>R-1h</td><td colspan="7">R-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PRI_HINT_6</td></tr>
<tr><td colspan="6">R-X</td><td colspan="2">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRI_HINT_6</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10720. ICSS_INTC_PRI_HINT_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_6	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_6	R	0h	Host Int 6 Prioritized Interrupt

84 ICSS_INTC_PRI_HINT_REG7 Register (Offset = 91Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG7 is shown in Figure 14-3548 and described in Table 14-7175.

Return to Summary Table.

Host Int 7 Prioritized Interrupt Register

Table 14-10721. ICSS_INTC_PRI_HINT_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 091Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 091Ch

Figure 14-3548. ICSS_INTC_PRI_HINT_REG7 Register

31	30	29	28	27	26	25	24
NONE_HINT_7	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_7	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_7							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10723. ICSS_INTC_PRI_HINT_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_7	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_7	R	0h	Host Int 7 Prioritized Interrupt

85 ICSS_INTC_PRI_HINT_REG8 Register (Offset = 920h) [reset = X]

ICSS_INTC_PRI_HINT_REG8 is shown in Figure 14-3549 and described in Table 14-7177.

Return to Summary Table.

Host Int 8 Prioritized Interrupt Register

Table 14-10724. ICSS_INTC_PRI_HINT_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0920h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0920h

Figure 14-3549. ICSS_INTC_PRI_HINT_REG8 Register

31	30	29	28	27	26	25	24
NONE_HINT_8	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_8	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_8							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10726. ICSS_INTC_PRI_HINT_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_8	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_8	R	0h	Host Int 8 Prioritized Interrupt

86 ICSS_INTC_PRI_HINT_REG9 Register (Offset = 924h) [reset = X]

ICSS_INTC_PRI_HINT_REG9 is shown in Figure 14-3550 and described in Table 14-7179.

Return to Summary Table.

Host Int 9 Prioritized Interrupt Register

Table 14-10727. ICSS_INTC_PRI_HINT_REG9 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0924h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0924h

Figure 14-3550. ICSS_INTC_PRI_HINT_REG9 Register

31	30	29	28	27	26	25	24
NONE_HINT_9	RESERVED						
R-1h	R-X						

23	22	21	20	19	18	17	16
RESERVED							
R-X							

15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_9	
R-X						R-0h	

7	6	5	4	3	2	1	0
PRI_HINT_9							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10729. ICSS_INTC_PRI_HINT_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_9	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_9	R	0h	Host Int 9 Prioritized Interrupt

87 ICSS_INTC_PRI_HINT_REG10 Register (Offset = 928h) [reset = X]

ICSS_INTC_PRI_HINT_REG10 is shown in Figure 14-3551 and described in Table 14-7181.

Return to Summary Table.

Host Int 10 Prioritized Interrupt Register

Table 14-10730. ICSS_INTC_PRI_HINT_REG10 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0928h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0928h

Figure 14-3551. ICSS_INTC_PRI_HINT_REG10 Register

31	30	29	28	27	26	25	24
NONE_HINT_10	RESERVED						
R-1h	R-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_10	
R-X						R-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_10							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10732. ICSS_INTC_PRI_HINT_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_10	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_10	R	0h	Host Int 10 Prioritized Interrupt

88 ICSS_INTC_PRI_HINT_REG11 Register (Offset = 92Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG11 is shown in Figure 14-3552 and described in Table 14-7183.

Return to Summary Table.

Host Int 11 Prioritized Interrupt Register

Table 14-10733. ICSS_INTC_PRI_HINT_REG11 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 092Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 092Ch

Figure 14-3552. ICSS_INTC_PRI_HINT_REG11 Register

31	30	29	28	27	26	25	24
NONE_HINT_11	RESERVED						
R-1h	R-X						

23	22	21	20	19	18	17	16
RESERVED							
R-X							

15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_11	
R-X						R-0h	

7	6	5	4	3	2	1	0
PRI_HINT_11							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10735. ICSS_INTC_PRI_HINT_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_11	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_11	R	0h	Host Int 11 Prioritized Interrupt

89 ICSS_INTC_PRI_HINT_REG12 Register (Offset = 930h) [reset = X]

ICSS_INTC_PRI_HINT_REG12 is shown in Figure 14-3553 and described in Table 14-7185.

Return to Summary Table.

Host Int 12 Prioritized Interrupt Register

Table 14-10736. ICSS_INTC_PRI_HINT_REG12 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0930h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0930h

Figure 14-3553. ICSS_INTC_PRI_HINT_REG12 Register

31	30	29	28	27	26	25	24
NONE_HINT_12	RESERVED						
R-1h	R-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_12	
R-X						R-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_12							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10738. ICSS_INTC_PRI_HINT_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_12	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_12	R	0h	Host Int 12 Prioritized Interrupt

90 ICSS_INTC_PRI_HINT_REG13 Register (Offset = 934h) [reset = X]

ICSS_INTC_PRI_HINT_REG13 is shown in Figure 14-3554 and described in Table 14-7187.

Return to Summary Table.

Host Int 13 Prioritized Interrupt Register

Table 14-10739. ICSS_INTC_PRI_HINT_REG13 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0934h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0934h

Figure 14-3554. ICSS_INTC_PRI_HINT_REG13 Register

31	30	29	28	27	26	25	24
NONE_HINT_13	RESERVED						
R-1h	R-X						

23	22	21	20	19	18	17	16
RESERVED							
R-X							

15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_13	
R-X						R-0h	

7	6	5	4	3	2	1	0
PRI_HINT_13							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10741. ICSS_INTC_PRI_HINT_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_13	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_13	R	0h	Host Int 13 Prioritized Interrupt

91 ICSS_INTC_PRI_HINT_REG14 Register (Offset = 938h) [reset = X]

ICSS_INTC_PRI_HINT_REG14 is shown in Figure 14-3555 and described in Table 14-7189.

Return to Summary Table.

Host Int 14 Prioritized Interrupt Register

Table 14-10742. ICSS_INTC_PRI_HINT_REG14 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0938h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0938h

Figure 14-3555. ICSS_INTC_PRI_HINT_REG14 Register

31	30	29	28	27	26	25	24
NONE_HINT_14	RESERVED						
R-1h	R-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_14	
R-X						R-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_14							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10744. ICSS_INTC_PRI_HINT_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_14	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_14	R	0h	Host Int 14 Prioritized Interrupt

92 ICSS_INTC_PRI_HINT_REG15 Register (Offset = 93Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG15 is shown in Figure 14-3556 and described in Table 14-7191.

Return to Summary Table.

Host Int 15 Prioritized Interrupt Register

Table 14-10745. ICSS_INTC_PRI_HINT_REG15 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 093Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 093Ch

Figure 14-3556. ICSS_INTC_PRI_HINT_REG15 Register

31	30	29	28	27	26	25	24
NONE_HINT_15	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_15	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_15							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 14-10747. ICSS_INTC_PRI_HINT_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_15	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_15	R	0h	Host Int 15 Prioritized Interrupt

93 ICSS_INTC_PRI_HINT_REG16 Register (Offset = 940h) [reset = X]

ICSS_INTC_PRI_HINT_REG16 is shown in Figure 14-3557 and described in Table 14-7193.

Return to Summary Table.

Host Int 16 Prioritized Interrupt Register

Table 14-10748. ICSS_INTC_PRI_HINT_REG16 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0940h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0940h

Figure 14-3557. ICSS_INTC_PRI_HINT_REG16 Register

31	30	29	28	27	26	25	24
NONE_HINT_16	RESERVED						
R-1h	R-X						

23	22	21	20	19	18	17	16
RESERVED							
R-X							

15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_16	
R-X						R-0h	

7	6	5	4	3	2	1	0
PRI_HINT_16							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10750. ICSS_INTC_PRI_HINT_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_16	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_16	R	0h	Host Int 16 Prioritized Interrupt

94 ICSS_INTC_PRI_HINT_REG17 Register (Offset = 944h) [reset = X]

ICSS_INTC_PRI_HINT_REG17 is shown in Figure 14-3558 and described in Table 14-7195.

Return to Summary Table.

Host Int 17 Prioritized Interrupt Register

Table 14-10751. ICSS_INTC_PRI_HINT_REG17 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0944h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0944h

Figure 14-3558. ICSS_INTC_PRI_HINT_REG17 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>NONE_HINT_17</td><td colspan="7">RESERVED</td></tr>
<tr><td>R-1h</td><td colspan="7">R-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PRI_HINT_17</td></tr>
<tr><td colspan="6">R-X</td><td colspan="2">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRI_HINT_17</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10753. ICSS_INTC_PRI_HINT_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_17	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_17	R	0h	Host Int 17 Prioritized Interrupt

95 ICSS_INTC_PRI_HINT_REG18 Register (Offset = 948h) [reset = X]

ICSS_INTC_PRI_HINT_REG18 is shown in Figure 14-3559 and described in Table 14-7197.

Return to Summary Table.

Host Int 18 Prioritized Interrupt Register

Table 14-10754. ICSS_INTC_PRI_HINT_REG18 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0948h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0948h

Figure 14-3559. ICSS_INTC_PRI_HINT_REG18 Register

31	30	29	28	27	26	25	24
NONE_HINT_18	RESERVED						
R-1h	R-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_18	
R-X						R-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_18							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10756. ICSS_INTC_PRI_HINT_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_18	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_18	R	0h	Host Int 18 Prioritized Interrupt

96 ICSS_INTC_PRI_HINT_REG19 Register (Offset = 94Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG19 is shown in Figure 14-3560 and described in Table 14-7199.

Return to Summary Table.

Host Int 19 Prioritized Interrupt Register

Table 14-10757. ICSS_INTC_PRI_HINT_REG19 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 094Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 094Ch

Figure 14-3560. ICSS_INTC_PRI_HINT_REG19 Register

31	30	29	28	27	26	25	24
NONE_HINT_19	RESERVED						
R-1h	R-X						

23	22	21	20	19	18	17	16
RESERVED							
R-X							

15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_19	
R-X						R-0h	

7	6	5	4	3	2	1	0
PRI_HINT_19							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10759. ICSS_INTC_PRI_HINT_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_19	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_19	R	0h	Host Int 19 Prioritized Interrupt

97 ICSS_INTC_POLARITY_REG0 Register (Offset = D00h) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG0 is shown in Figure 14-3561 and described in Table 14-7201.

Return to Summary Table.

Polarity Register 0

Table 14-10760. ICSS_INTC_POLARITY_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D00h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D00h

Figure 14-3561. ICSS_INTC_POLARITY_REG0 Register

31	30	29	28	27	26	25	24
POLARITY_31	POLARITY_30	POLARITY_29	POLARITY_28	POLARITY_27	POLARITY_26	POLARITY_25	POLARITY_24
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_23	POLARITY_22	POLARITY_21	POLARITY_20	POLARITY_19	POLARITY_18	POLARITY_17	POLARITY_16
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_15	POLARITY_14	POLARITY_13	POLARITY_12	POLARITY_11	POLARITY_10	POLARITY_9	POLARITY_8
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_7	POLARITY_6	POLARITY_5	POLARITY_4	POLARITY_3	POLARITY_2	POLARITY_1	POLARITY_0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10762. ICSS_INTC_POLARITY_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_31	R/W	1h	Polarity for intr_in[31] 0=low
30	POLARITY_30	R/W	1h	Polarity for intr_in[30] 0=low
29	POLARITY_29	R/W	1h	Polarity for intr_in[29] 0=low
28	POLARITY_28	R/W	1h	Polarity for intr_in[28] 0=low
27	POLARITY_27	R/W	1h	Polarity for intr_in[27] 0=low
26	POLARITY_26	R/W	1h	Polarity for intr_in[26] 0=low
25	POLARITY_25	R/W	1h	Polarity for intr_in[25] 0=low
24	POLARITY_24	R/W	1h	Polarity for intr_in[24] 0=low
23	POLARITY_23	R/W	1h	Polarity for intr_in[23] 0=low
22	POLARITY_22	R/W	1h	Polarity for intr_in[22] 0=low
21	POLARITY_21	R/W	1h	Polarity for intr_in[21] 0=low

Table 14-10762. ICSS_INTC_POLARITY_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	POLARITY_20	R/W	1h	Polarity for intr_in[20] 0=low
19	POLARITY_19	R/W	1h	Polarity for intr_in[19] 0=low
18	POLARITY_18	R/W	1h	Polarity for intr_in[18] 0=low
17	POLARITY_17	R/W	1h	Polarity for intr_in[17] 0=low
16	POLARITY_16	R/W	1h	Polarity for intr_in[16] 0=low
15	POLARITY_15	R/W	1h	Polarity for intr_in[15] 0=low
14	POLARITY_14	R/W	1h	Polarity for intr_in[14] 0=low
13	POLARITY_13	R/W	1h	Polarity for intr_in[13] 0=low
12	POLARITY_12	R/W	1h	Polarity for intr_in[12] 0=low
11	POLARITY_11	R/W	1h	Polarity for intr_in[11] 0=low
10	POLARITY_10	R/W	1h	Polarity for intr_in[10] 0=low
9	POLARITY_9	R/W	1h	Polarity for intr_in[9] 0=low
8	POLARITY_8	R/W	1h	Polarity for intr_in[8] 0=low
7	POLARITY_7	R/W	1h	Polarity for intr_in[7] 0=low
6	POLARITY_6	R/W	1h	Polarity for intr_in[6] 0=low
5	POLARITY_5	R/W	1h	Polarity for intr_in[5] 0=low
4	POLARITY_4	R/W	1h	Polarity for intr_in[4] 0=low
3	POLARITY_3	R/W	1h	Polarity for intr_in[3] 0=low
2	POLARITY_2	R/W	1h	Polarity for intr_in[2] 0=low
1	POLARITY_1	R/W	1h	Polarity for intr_in[1] 0=low
0	POLARITY_0	R/W	1h	Polarity for intr_in[0] 0=low

98 ICSS_INTC_POLARITY_REG1 Register (Offset = D04h) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG1 is shown in Figure 14-3562 and described in Table 14-7203.

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Polarity Register 1

Table 14-10763. ICSS_INTC_POLARITY_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D04h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D04h

Figure 14-3562. ICSS_INTC_POLARITY_REG1 Register

31	30	29	28	27	26	25	24
POLARITY_63	POLARITY_62	POLARITY_61	POLARITY_60	POLARITY_59	POLARITY_58	POLARITY_57	POLARITY_56
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_55	POLARITY_54	POLARITY_53	POLARITY_52	POLARITY_51	POLARITY_50	POLARITY_49	POLARITY_48
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_47	POLARITY_46	POLARITY_45	POLARITY_44	POLARITY_43	POLARITY_42	POLARITY_41	POLARITY_40
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_39	POLARITY_38	POLARITY_37	POLARITY_36	POLARITY_35	POLARITY_34	POLARITY_33	POLARITY_32
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10765. ICSS_INTC_POLARITY_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_63	R/W	1h	Polarity for intr_in[63] 0=low
30	POLARITY_62	R/W	1h	Polarity for intr_in[62] 0=low
29	POLARITY_61	R/W	1h	Polarity for intr_in[61] 0=low
28	POLARITY_60	R/W	1h	Polarity for intr_in[60] 0=low
27	POLARITY_59	R/W	1h	Polarity for intr_in[59] 0=low
26	POLARITY_58	R/W	1h	Polarity for intr_in[58] 0=low
25	POLARITY_57	R/W	1h	Polarity for intr_in[57] 0=low
24	POLARITY_56	R/W	1h	Polarity for intr_in[56] 0=low
23	POLARITY_55	R/W	1h	Polarity for intr_in[55] 0=low
22	POLARITY_54	R/W	1h	Polarity for intr_in[54] 0=low
21	POLARITY_53	R/W	1h	Polarity for intr_in[53] 0=low

Table 14-10765. ICSS_INTC_POLARITY_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	POLARITY_52	R/W	1h	Polarity for intr_in[52] 0=low
19	POLARITY_51	R/W	1h	Polarity for intr_in[51] 0=low
18	POLARITY_50	R/W	1h	Polarity for intr_in[50] 0=low
17	POLARITY_49	R/W	1h	Polarity for intr_in[49] 0=low
16	POLARITY_48	R/W	1h	Polarity for intr_in[48] 0=low
15	POLARITY_47	R/W	1h	Polarity for intr_in[47] 0=low
14	POLARITY_46	R/W	1h	Polarity for intr_in[46] 0=low
13	POLARITY_45	R/W	1h	Polarity for intr_in[45] 0=low
12	POLARITY_44	R/W	1h	Polarity for intr_in[44] 0=low
11	POLARITY_43	R/W	1h	Polarity for intr_in[43] 0=low
10	POLARITY_42	R/W	1h	Polarity for intr_in[42] 0=low
9	POLARITY_41	R/W	1h	Polarity for intr_in[41] 0=low
8	POLARITY_40	R/W	1h	Polarity for intr_in[40] 0=low
7	POLARITY_39	R/W	1h	Polarity for intr_in[39] 0=low
6	POLARITY_38	R/W	1h	Polarity for intr_in[38] 0=low
5	POLARITY_37	R/W	1h	Polarity for intr_in[37] 0=low
4	POLARITY_36	R/W	1h	Polarity for intr_in[36] 0=low
3	POLARITY_35	R/W	1h	Polarity for intr_in[35] 0=low
2	POLARITY_34	R/W	1h	Polarity for intr_in[34] 0=low
1	POLARITY_33	R/W	1h	Polarity for intr_in[33] 0=low
0	POLARITY_32	R/W	1h	Polarity for intr_in[32] 0=low

99 ICSS_INTC_POLARITY_REG2 Register (Offset = D08h) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG2 is shown in Figure 14-3563 and described in Table 14-7205.

Return to Summary Table.

Polarity Register 2

Table 14-10766. ICSS_INTC_POLARITY_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D08h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D08h

Figure 14-3563. ICSS_INTC_POLARITY_REG2 Register

31	30	29	28	27	26	25	24
POLARITY_95	POLARITY_94	POLARITY_93	POLARITY_92	POLARITY_91	POLARITY_90	POLARITY_89	POLARITY_88
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_87	POLARITY_86	POLARITY_85	POLARITY_84	POLARITY_83	POLARITY_82	POLARITY_81	POLARITY_80
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_79	POLARITY_78	POLARITY_77	POLARITY_76	POLARITY_75	POLARITY_74	POLARITY_73	POLARITY_72
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_71	POLARITY_70	POLARITY_69	POLARITY_68	POLARITY_67	POLARITY_66	POLARITY_65	POLARITY_64
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10768. ICSS_INTC_POLARITY_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_95	R/W	1h	Polarity for slv_events_in[31] 0=low
30	POLARITY_94	R/W	1h	Polarity for slv_events_in[30] 0=low
29	POLARITY_93	R/W	1h	Polarity for slv_events_in[29] 0=low
28	POLARITY_92	R/W	1h	Polarity for slv_events_in[28] 0=low
27	POLARITY_91	R/W	1h	Polarity for slv_events_in[27] 0=low
26	POLARITY_90	R/W	1h	Polarity for slv_events_in[26] 0=low
25	POLARITY_89	R/W	1h	Polarity for slv_events_in[25] 0=low
24	POLARITY_88	R/W	1h	Polarity for slv_events_in[24] 0=low
23	POLARITY_87	R/W	1h	Polarity for slv_events_in[23] 0=low
22	POLARITY_86	R/W	1h	Polarity for slv_events_in[22] 0=low
21	POLARITY_85	R/W	1h	Polarity for slv_events_in[21] 0=low

Table 14-10768. ICSS_INTC_POLARITY_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	POLARITY_84	R/W	1h	Polarity for slv_events_in[20] 0=low
19	POLARITY_83	R/W	1h	Polarity for slv_events_in[19] 0=low
18	POLARITY_82	R/W	1h	Polarity for slv_events_in[18] 0=low
17	POLARITY_81	R/W	1h	Polarity for slv_events_in[17] 0=low
16	POLARITY_80	R/W	1h	Polarity for slv_events_in[16] 0=low
15	POLARITY_79	R/W	1h	Polarity for slv_events_in[15] 0=low
14	POLARITY_78	R/W	1h	Polarity for slv_events_in[14] 0=low
13	POLARITY_77	R/W	1h	Polarity for slv_events_in[13] 0=low
12	POLARITY_76	R/W	1h	Polarity for slv_events_in[12] 0=low
11	POLARITY_75	R/W	1h	Polarity for slv_events_in[11] 0=low
10	POLARITY_74	R/W	1h	Polarity for slv_events_in[10] 0=low
9	POLARITY_73	R/W	1h	Polarity for slv_events_in[9] 0=low
8	POLARITY_72	R/W	1h	Polarity for slv_events_in[8] 0=low
7	POLARITY_71	R/W	1h	Polarity for slv_events_in[7] 0=low
6	POLARITY_70	R/W	1h	Polarity for slv_events_in[6] 0=low
5	POLARITY_69	R/W	1h	Polarity for slv_events_in[5] 0=low
4	POLARITY_68	R/W	1h	Polarity for slv_events_in[4] 0=low
3	POLARITY_67	R/W	1h	Polarity for slv_events_in[3] 0=low
2	POLARITY_66	R/W	1h	Polarity for slv_events_in[2] 0=low
1	POLARITY_65	R/W	1h	Polarity for slv_events_in[1] 0=low
0	POLARITY_64	R/W	1h	Polarity for slv_events_in[0] 0=low

100 ICSS_INTC_POLARITY_REG3 Register (Offset = D0Ch) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG3 is shown in Figure 14-3564 and described in Table 14-7207.

Return to Summary Table.

Polarity Register 3

Table 14-10769. ICSS_INTC_POLARITY_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D0Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D0Ch

Figure 14-3564. ICSS_INTC_POLARITY_REG3 Register

31	30	29	28	27	26	25	24
POLARITY_127	POLARITY_126	POLARITY_125	POLARITY_124	POLARITY_123	POLARITY_122	POLARITY_121	POLARITY_120
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_119	POLARITY_118	POLARITY_117	POLARITY_116	POLARITY_115	POLARITY_114	POLARITY_113	POLARITY_112
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_111	POLARITY_110	POLARITY_109	POLARITY_108	POLARITY_107	POLARITY_106	POLARITY_105	POLARITY_104
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_103	POLARITY_102	POLARITY_101	POLARITY_100	POLARITY_99	POLARITY_98	POLARITY_97	POLARITY_96
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10771. ICSS_INTC_POLARITY_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_127	R/W	1h	Polarity for slv_events_in[63] 0=low
30	POLARITY_126	R/W	1h	Polarity for slv_events_in[62] 0=low
29	POLARITY_125	R/W	1h	Polarity for slv_events_in[61] 0=low
28	POLARITY_124	R/W	1h	Polarity for slv_events_in[60] 0=low
27	POLARITY_123	R/W	1h	Polarity for slv_events_in[59] 0=low
26	POLARITY_122	R/W	1h	Polarity for slv_events_in[58] 0=low
25	POLARITY_121	R/W	1h	Polarity for slv_events_in[57] 0=low
24	POLARITY_120	R/W	1h	Polarity for slv_events_in[56] 0=low
23	POLARITY_119	R/W	1h	Polarity for slv_events_in[55] 0=low
22	POLARITY_118	R/W	1h	Polarity for slv_events_in[54] 0=low
21	POLARITY_117	R/W	1h	Polarity for slv_events_in[53] 0=low

Table 14-10771. ICSS_INTC_POLARITY_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	POLARITY_116	R/W	1h	Polarity for slv_events_in[52] 0=low
19	POLARITY_115	R/W	1h	Polarity for slv_events_in[51] 0=low
18	POLARITY_114	R/W	1h	Polarity for slv_events_in[50] 0=low
17	POLARITY_113	R/W	1h	Polarity for slv_events_in[49] 0=low
16	POLARITY_112	R/W	1h	Polarity for slv_events_in[48] 0=low
15	POLARITY_111	R/W	1h	Polarity for slv_events_in[47] 0=low
14	POLARITY_110	R/W	1h	Polarity for slv_events_in[46] 0=low
13	POLARITY_109	R/W	1h	Polarity for slv_events_in[45] 0=low
12	POLARITY_108	R/W	1h	Polarity for slv_events_in[44] 0=low
11	POLARITY_107	R/W	1h	Polarity for slv_events_in[43] 0=low
10	POLARITY_106	R/W	1h	Polarity for slv_events_in[42] 0=low
9	POLARITY_105	R/W	1h	Polarity for slv_events_in[41] 0=low
8	POLARITY_104	R/W	1h	Polarity for slv_events_in[40] 0=low
7	POLARITY_103	R/W	1h	Polarity for slv_events_in[39] 0=low
6	POLARITY_102	R/W	1h	Polarity for slv_events_in[38] 0=low
5	POLARITY_101	R/W	1h	Polarity for slv_events_in[37] 0=low
4	POLARITY_100	R/W	1h	Polarity for slv_events_in[36] 0=low
3	POLARITY_99	R/W	1h	Polarity for slv_events_in[35] 0=low
2	POLARITY_98	R/W	1h	Polarity for slv_events_in[34] 0=low
1	POLARITY_97	R/W	1h	Polarity for slv_events_in[33] 0=low
0	POLARITY_96	R/W	1h	Polarity for slv_events_in[32] 0=low

101 ICSS_INTC_POLARITY_REG4 Register (Offset = D10h) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG4 is shown in Figure 14-3565 and described in Table 14-7209.

Return to Summary Table.

Polarity Register 4

Table 14-10772. ICSS_INTC_POLARITY_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D10h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D10h

Figure 14-3565. ICSS_INTC_POLARITY_REG4 Register

31	30	29	28	27	26	25	24
POLARITY_159	POLARITY_158	POLARITY_157	POLARITY_156	POLARITY_155	POLARITY_154	POLARITY_153	POLARITY_152
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_151	POLARITY_150	POLARITY_149	POLARITY_148	POLARITY_147	POLARITY_146	POLARITY_145	POLARITY_144
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_143	POLARITY_142	POLARITY_141	POLARITY_140	POLARITY_139	POLARITY_138	POLARITY_137	POLARITY_136
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_135	POLARITY_134	POLARITY_133	POLARITY_132	POLARITY_131	POLARITY_130	POLARITY_129	POLARITY_128
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10774. ICSS_INTC_POLARITY_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_159	R/W	1h	Polarity for slv_events_in[95] 0=low
30	POLARITY_158	R/W	1h	Polarity for slv_events_in[94] 0=low
29	POLARITY_157	R/W	1h	Polarity for slv_events_in[93] 0=low
28	POLARITY_156	R/W	1h	Polarity for slv_events_in[92] 0=low
27	POLARITY_155	R/W	1h	Polarity for slv_events_in[91] 0=low
26	POLARITY_154	R/W	1h	Polarity for slv_events_in[90] 0=low
25	POLARITY_153	R/W	1h	Polarity for slv_events_in[89] 0=low
24	POLARITY_152	R/W	1h	Polarity for slv_events_in[88] 0=low
23	POLARITY_151	R/W	1h	Polarity for slv_events_in[87] 0=low
22	POLARITY_150	R/W	1h	Polarity for slv_events_in[86] 0=low
21	POLARITY_149	R/W	1h	Polarity for slv_events_in[85] 0=low

Table 14-10774. ICSS_INTC_POLARITY_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	POLARITY_148	R/W	1h	Polarity for slv_events_in[84] 0=low
19	POLARITY_147	R/W	1h	Polarity for slv_events_in[83] 0=low
18	POLARITY_146	R/W	1h	Polarity for slv_events_in[82] 0=low
17	POLARITY_145	R/W	1h	Polarity for slv_events_in[81] 0=low
16	POLARITY_144	R/W	1h	Polarity for slv_events_in[80] 0=low
15	POLARITY_143	R/W	1h	Polarity for slv_events_in[79] 0=low
14	POLARITY_142	R/W	1h	Polarity for slv_events_in[78] 0=low
13	POLARITY_141	R/W	1h	Polarity for slv_events_in[77] 0=low
12	POLARITY_140	R/W	1h	Polarity for slv_events_in[76] 0=low
11	POLARITY_139	R/W	1h	Polarity for slv_events_in[75] 0=low
10	POLARITY_138	R/W	1h	Polarity for slv_events_in[74] 0=low
9	POLARITY_137	R/W	1h	Polarity for slv_events_in[73] 0=low
8	POLARITY_136	R/W	1h	Polarity for slv_events_in[72] 0=low
7	POLARITY_135	R/W	1h	Polarity for slv_events_in[71] 0=low
6	POLARITY_134	R/W	1h	Polarity for slv_events_in[70] 0=low
5	POLARITY_133	R/W	1h	Polarity for slv_events_in[69] 0=low
4	POLARITY_132	R/W	1h	Polarity for slv_events_in[68] 0=low
3	POLARITY_131	R/W	1h	Polarity for slv_events_in[67] 0=low
2	POLARITY_130	R/W	1h	Polarity for slv_events_in[66] 0=low
1	POLARITY_129	R/W	1h	Polarity for slv_events_in[65] 0=low
0	POLARITY_128	R/W	1h	Polarity for slv_events_in[64] 0=low

102 ICSS_INTC_TYPE_REG0 Register (Offset = D80h) [reset = 0h]

ICSS_INTC_TYPE_REG0 is shown in Figure 14-3566 and described in Table 14-7211.

Return to Summary Table.

Type Register 0

Table 14-10775. ICSS_INTC_TYPE_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D80h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D80h

Figure 14-3566. ICSS_INTC_TYPE_REG0 Register

31	30	29	28	27	26	25	24
TYPE_31	TYPE_30	TYPE_29	TYPE_28	TYPE_27	TYPE_26	TYPE_25	TYPE_24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_23	TYPE_22	TYPE_21	TYPE_20	TYPE_19	TYPE_18	TYPE_17	TYPE_16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_15	TYPE_14	TYPE_13	TYPE_12	TYPE_11	TYPE_10	TYPE_9	TYPE_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_7	TYPE_6	TYPE_5	TYPE_4	TYPE_3	TYPE_2	TYPE_1	TYPE_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10777. ICSS_INTC_TYPE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_31	R/W	0h	Type for intr_in[31] 0=level
30	TYPE_30	R/W	0h	Type for intr_in[30] 0=level
29	TYPE_29	R/W	0h	Type for intr_in[29] 0=level
28	TYPE_28	R/W	0h	Type for intr_in[28] 0=level
27	TYPE_27	R/W	0h	Type for intr_in[27] 0=level
26	TYPE_26	R/W	0h	Type for intr_in[26] 0=level
25	TYPE_25	R/W	0h	Type for intr_in[25] 0=level
24	TYPE_24	R/W	0h	Type for intr_in[24] 0=level
23	TYPE_23	R/W	0h	Type for intr_in[23] 0=level
22	TYPE_22	R/W	0h	Type for intr_in[22] 0=level
21	TYPE_21	R/W	0h	Type for intr_in[21] 0=level

Table 14-10777. ICSS_INTC_TYPE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TYPE_20	R/W	0h	Type for intr_in[20] 0=level
19	TYPE_19	R/W	0h	Type for intr_in[19] 0=level
18	TYPE_18	R/W	0h	Type for intr_in[18] 0=level
17	TYPE_17	R/W	0h	Type for intr_in[17] 0=level
16	TYPE_16	R/W	0h	Type for intr_in[16] 0=level
15	TYPE_15	R/W	0h	Type for intr_in[15] 0=level
14	TYPE_14	R/W	0h	Type for intr_in[14] 0=level
13	TYPE_13	R/W	0h	Type for intr_in[13] 0=level
12	TYPE_12	R/W	0h	Type for intr_in[12] 0=level
11	TYPE_11	R/W	0h	Type for intr_in[11] 0=level
10	TYPE_10	R/W	0h	Type for intr_in[10] 0=level
9	TYPE_9	R/W	0h	Type for intr_in[9] 0=level
8	TYPE_8	R/W	0h	Type for intr_in[8] 0=level
7	TYPE_7	R/W	0h	Type for intr_in[7] 0=level
6	TYPE_6	R/W	0h	Type for intr_in[6] 0=level
5	TYPE_5	R/W	0h	Type for intr_in[5] 0=level
4	TYPE_4	R/W	0h	Type for intr_in[4] 0=level
3	TYPE_3	R/W	0h	Type for intr_in[3] 0=level
2	TYPE_2	R/W	0h	Type for intr_in[2] 0=level
1	TYPE_1	R/W	0h	Type for intr_in[1] 0=level
0	TYPE_0	R/W	0h	Type for intr_in[0] 0=level

103 ICSS_INTC_TYPE_REG1 Register (Offset = D84h) [reset = 0h]

ICSS_INTC_TYPE_REG1 is shown in Figure 14-3567 and described in Table 14-7213.

Return to Summary Table.

Type Register 1

Table 14-10778. ICSS_INTC_TYPE_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D84h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D84h

Figure 14-3567. ICSS_INTC_TYPE_REG1 Register

31	30	29	28	27	26	25	24
TYPE_63	TYPE_62	TYPE_61	TYPE_60	TYPE_59	TYPE_58	TYPE_57	TYPE_56
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_55	TYPE_54	TYPE_53	TYPE_52	TYPE_51	TYPE_50	TYPE_49	TYPE_48
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_47	TYPE_46	TYPE_45	TYPE_44	TYPE_43	TYPE_42	TYPE_41	TYPE_40
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_39	TYPE_38	TYPE_37	TYPE_36	TYPE_35	TYPE_34	TYPE_33	TYPE_32
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10780. ICSS_INTC_TYPE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_63	R/W	0h	Type for intr_in[63] 0=level
30	TYPE_62	R/W	0h	Type for intr_in[62] 0=level
29	TYPE_61	R/W	0h	Type for intr_in[61] 0=level
28	TYPE_60	R/W	0h	Type for intr_in[60] 0=level
27	TYPE_59	R/W	0h	Type for intr_in[59] 0=level
26	TYPE_58	R/W	0h	Type for intr_in[58] 0=level
25	TYPE_57	R/W	0h	Type for intr_in[57] 0=level
24	TYPE_56	R/W	0h	Type for intr_in[56] 0=level
23	TYPE_55	R/W	0h	Type for intr_in[55] 0=level
22	TYPE_54	R/W	0h	Type for intr_in[54] 0=level
21	TYPE_53	R/W	0h	Type for intr_in[53] 0=level

Table 14-10780. ICSS_INTC_TYPE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TYPE_52	R/W	0h	Type for intr_in[52] 0=level
19	TYPE_51	R/W	0h	Type for intr_in[51] 0=level
18	TYPE_50	R/W	0h	Type for intr_in[50] 0=level
17	TYPE_49	R/W	0h	Type for intr_in[49] 0=level
16	TYPE_48	R/W	0h	Type for intr_in[48] 0=level
15	TYPE_47	R/W	0h	Type for intr_in[47] 0=level
14	TYPE_46	R/W	0h	Type for intr_in[46] 0=level
13	TYPE_45	R/W	0h	Type for intr_in[45] 0=level
12	TYPE_44	R/W	0h	Type for intr_in[44] 0=level
11	TYPE_43	R/W	0h	Type for intr_in[43] 0=level
10	TYPE_42	R/W	0h	Type for intr_in[42] 0=level
9	TYPE_41	R/W	0h	Type for intr_in[41] 0=level
8	TYPE_40	R/W	0h	Type for intr_in[40] 0=level
7	TYPE_39	R/W	0h	Type for intr_in[39] 0=level
6	TYPE_38	R/W	0h	Type for intr_in[38] 0=level
5	TYPE_37	R/W	0h	Type for intr_in[37] 0=level
4	TYPE_36	R/W	0h	Type for intr_in[36] 0=level
3	TYPE_35	R/W	0h	Type for intr_in[35] 0=level
2	TYPE_34	R/W	0h	Type for intr_in[34] 0=level
1	TYPE_33	R/W	0h	Type for intr_in[33] 0=level
0	TYPE_32	R/W	0h	Type for intr_in[32] 0=level

104 ICSS_INTC_TYPE_REG2 Register (Offset = D88h) [reset = 0h]

ICSS_INTC_TYPE_REG2 is shown in Figure 14-3568 and described in Table 14-7215.

Return to Summary Table.

Type Register 2

Table 14-10781. ICSS_INTC_TYPE_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D88h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D88h

Figure 14-3568. ICSS_INTC_TYPE_REG2 Register

31	30	29	28	27	26	25	24
TYPE_95	TYPE_94	TYPE_93	TYPE_92	TYPE_91	TYPE_90	TYPE_89	TYPE_88
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_87	TYPE_86	TYPE_85	TYPE_84	TYPE_83	TYPE_82	TYPE_81	TYPE_80
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_79	TYPE_78	TYPE_77	TYPE_76	TYPE_75	TYPE_74	TYPE_73	TYPE_72
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_71	TYPE_70	TYPE_69	TYPE_68	TYPE_67	TYPE_66	TYPE_65	TYPE_64
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10783. ICSS_INTC_TYPE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_95	R/W	0h	Type for slv_events_in[31] 0=level
30	TYPE_94	R/W	0h	Type for slv_events_in[30] 0=level
29	TYPE_93	R/W	0h	Type for slv_events_in[29] 0=level
28	TYPE_92	R/W	0h	Type for slv_events_in[28] 0=level
27	TYPE_91	R/W	0h	Type for slv_events_in[27] 0=level
26	TYPE_90	R/W	0h	Type for slv_events_in[26] 0=level
25	TYPE_89	R/W	0h	Type for slv_events_in[25] 0=level
24	TYPE_88	R/W	0h	Type for slv_events_in[24] 0=level
23	TYPE_87	R/W	0h	Type for slv_events_in[23] 0=level
22	TYPE_86	R/W	0h	Type for slv_events_in[22] 0=level
21	TYPE_85	R/W	0h	Type for slv_events_in[21] 0=level

Table 14-10783. ICSS_INTC_TYPE_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TYPE_84	R/W	0h	Type for slv_events_in[20] 0=level
19	TYPE_83	R/W	0h	Type for slv_events_in[19] 0=level
18	TYPE_82	R/W	0h	Type for slv_events_in[18] 0=level
17	TYPE_81	R/W	0h	Type for slv_events_in[17] 0=level
16	TYPE_80	R/W	0h	Type for slv_events_in[16] 0=level
15	TYPE_79	R/W	0h	Type for slv_events_in[15] 0=level
14	TYPE_78	R/W	0h	Type for slv_events_in[14] 0=level
13	TYPE_77	R/W	0h	Type for slv_events_in[13] 0=level
12	TYPE_76	R/W	0h	Type for slv_events_in[12] 0=level
11	TYPE_75	R/W	0h	Type for slv_events_in[11] 0=level
10	TYPE_74	R/W	0h	Type for slv_events_in[10] 0=level
9	TYPE_73	R/W	0h	Type for slv_events_in[9] 0=level
8	TYPE_72	R/W	0h	Type for slv_events_in[8] 0=level
7	TYPE_71	R/W	0h	Type for slv_events_in[7] 0=level
6	TYPE_70	R/W	0h	Type for slv_events_in[6] 0=level
5	TYPE_69	R/W	0h	Type for slv_events_in[5] 0=level
4	TYPE_68	R/W	0h	Type for slv_events_in[4] 0=level
3	TYPE_67	R/W	0h	Type for slv_events_in[3] 0=level
2	TYPE_66	R/W	0h	Type for slv_events_in[2] 0=level
1	TYPE_65	R/W	0h	Type for slv_events_in[1] 0=level
0	TYPE_64	R/W	0h	Type for slv_events_in[0] 0=level

105 ICSS_INTC_TYPE_REG3 Register (Offset = D8Ch) [reset = 0h]

ICSS_INTC_TYPE_REG3 is shown in Figure 14-3569 and described in Table 14-7217.

Return to Summary Table.

Type Register 3

Table 14-10784. ICSS_INTC_TYPE_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D8Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D8Ch

Figure 14-3569. ICSS_INTC_TYPE_REG3 Register

31	30	29	28	27	26	25	24
TYPE_127	TYPE_126	TYPE_125	TYPE_124	TYPE_123	TYPE_122	TYPE_121	TYPE_120
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_119	TYPE_118	TYPE_117	TYPE_116	TYPE_115	TYPE_114	TYPE_113	TYPE_112
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_111	TYPE_110	TYPE_109	TYPE_108	TYPE_107	TYPE_106	TYPE_105	TYPE_104
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_103	TYPE_102	TYPE_101	TYPE_100	TYPE_99	TYPE_98	TYPE_97	TYPE_96
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10786. ICSS_INTC_TYPE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_127	R/W	0h	Type for slv_events_in[63] 0=level
30	TYPE_126	R/W	0h	Type for slv_events_in[62] 0=level
29	TYPE_125	R/W	0h	Type for slv_events_in[61] 0=level
28	TYPE_124	R/W	0h	Type for slv_events_in[60] 0=level
27	TYPE_123	R/W	0h	Type for slv_events_in[59] 0=level
26	TYPE_122	R/W	0h	Type for slv_events_in[58] 0=level
25	TYPE_121	R/W	0h	Type for slv_events_in[57] 0=level
24	TYPE_120	R/W	0h	Type for slv_events_in[56] 0=level
23	TYPE_119	R/W	0h	Type for slv_events_in[55] 0=level
22	TYPE_118	R/W	0h	Type for slv_events_in[54] 0=level
21	TYPE_117	R/W	0h	Type for slv_events_in[53] 0=level

Table 14-10786. ICSS_INTC_TYPE_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TYPE_116	R/W	0h	Type for slv_events_in[52] 0=level
19	TYPE_115	R/W	0h	Type for slv_events_in[51] 0=level
18	TYPE_114	R/W	0h	Type for slv_events_in[50] 0=level
17	TYPE_113	R/W	0h	Type for slv_events_in[49] 0=level
16	TYPE_112	R/W	0h	Type for slv_events_in[48] 0=level
15	TYPE_111	R/W	0h	Type for slv_events_in[47] 0=level
14	TYPE_110	R/W	0h	Type for slv_events_in[46] 0=level
13	TYPE_109	R/W	0h	Type for slv_events_in[45] 0=level
12	TYPE_108	R/W	0h	Type for slv_events_in[44] 0=level
11	TYPE_107	R/W	0h	Type for slv_events_in[43] 0=level
10	TYPE_106	R/W	0h	Type for slv_events_in[42] 0=level
9	TYPE_105	R/W	0h	Type for slv_events_in[41] 0=level
8	TYPE_104	R/W	0h	Type for slv_events_in[40] 0=level
7	TYPE_103	R/W	0h	Type for slv_events_in[39] 0=level
6	TYPE_102	R/W	0h	Type for slv_events_in[38] 0=level
5	TYPE_101	R/W	0h	Type for slv_events_in[37] 0=level
4	TYPE_100	R/W	0h	Type for slv_events_in[36] 0=level
3	TYPE_99	R/W	0h	Type for slv_events_in[35] 0=level
2	TYPE_98	R/W	0h	Type for slv_events_in[34] 0=level
1	TYPE_97	R/W	0h	Type for slv_events_in[33] 0=level
0	TYPE_96	R/W	0h	Type for slv_events_in[32] 0=level

106 ICSS_INTC_TYPE_REG4 Register (Offset = D90h) [reset = 0h]

ICSS_INTC_TYPE_REG4 is shown in Figure 14-3570 and described in Table 14-7219.

Return to Summary Table.

Type Register 4

Table 14-10787. ICSS_INTC_TYPE_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 0D90h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 0D90h

Figure 14-3570. ICSS_INTC_TYPE_REG4 Register

31	30	29	28	27	26	25	24
TYPE_159	TYPE_158	TYPE_157	TYPE_156	TYPE_155	TYPE_154	TYPE_153	TYPE_152
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_151	TYPE_150	TYPE_149	TYPE_148	TYPE_147	TYPE_146	TYPE_145	TYPE_144
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_143	TYPE_142	TYPE_141	TYPE_140	TYPE_139	TYPE_138	TYPE_137	TYPE_136
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_135	TYPE_134	TYPE_133	TYPE_132	TYPE_131	TYPE_130	TYPE_129	TYPE_128
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10789. ICSS_INTC_TYPE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_159	R/W	0h	Type for slv_events_in[95] 0=level
30	TYPE_158	R/W	0h	Type for slv_events_in[94] 0=level
29	TYPE_157	R/W	0h	Type for slv_events_in[93] 0=level
28	TYPE_156	R/W	0h	Type for slv_events_in[92] 0=level
27	TYPE_155	R/W	0h	Type for slv_events_in[91] 0=level
26	TYPE_154	R/W	0h	Type for slv_events_in[90] 0=level
25	TYPE_153	R/W	0h	Type for slv_events_in[89] 0=level
24	TYPE_152	R/W	0h	Type for slv_events_in[88] 0=level
23	TYPE_151	R/W	0h	Type for slv_events_in[87] 0=level
22	TYPE_150	R/W	0h	Type for slv_events_in[86] 0=level
21	TYPE_149	R/W	0h	Type for slv_events_in[85] 0=level

Table 14-10789. ICSS_INTC_TYPE_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TYPE_148	R/W	0h	Type for slv_events_in[84] 0=level
19	TYPE_147	R/W	0h	Type for slv_events_in[83] 0=level
18	TYPE_146	R/W	0h	Type for slv_events_in[82] 0=level
17	TYPE_145	R/W	0h	Type for slv_events_in[81] 0=level
16	TYPE_144	R/W	0h	Type for slv_events_in[80] 0=level
15	TYPE_143	R/W	0h	Type for slv_events_in[79] 0=level
14	TYPE_142	R/W	0h	Type for slv_events_in[78] 0=level
13	TYPE_141	R/W	0h	Type for slv_events_in[77] 0=level
12	TYPE_140	R/W	0h	Type for slv_events_in[76] 0=level
11	TYPE_139	R/W	0h	Type for slv_events_in[75] 0=level
10	TYPE_138	R/W	0h	Type for slv_events_in[74] 0=level
9	TYPE_137	R/W	0h	Type for slv_events_in[73] 0=level
8	TYPE_136	R/W	0h	Type for slv_events_in[72] 0=level
7	TYPE_135	R/W	0h	Type for slv_events_in[71] 0=level
6	TYPE_134	R/W	0h	Type for slv_events_in[70] 0=level
5	TYPE_133	R/W	0h	Type for slv_events_in[69] 0=level
4	TYPE_132	R/W	0h	Type for slv_events_in[68] 0=level
3	TYPE_131	R/W	0h	Type for slv_events_in[67] 0=level
2	TYPE_130	R/W	0h	Type for slv_events_in[66] 0=level
1	TYPE_129	R/W	0h	Type for slv_events_in[65] 0=level
0	TYPE_128	R/W	0h	Type for slv_events_in[64] 0=level

107 ICSS_INTC_NEST_LEVEL_REG0 Register (Offset = 1100h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG0 is shown in Figure 14-3571 and described in Table 14-7221.

Return to Summary Table.

Host Int 0 Nesting Level Register

Table 14-10790. ICSS_INTC_NEST_LEVEL_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1100h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1100h

Figure 14-3571. ICSS_INTC_NEST_LEVEL_REG0 Register

31	30	29	28	27	26	25	24
NEST_AUTO_ OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_0
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_0							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10792. ICSS_INTC_NEST_LEVEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_0	R/W	100h	Host Int 0 Nesting Level

108 ICSS_INTC_NEST_LEVEL_REG1 Register (Offset = 1104h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG1 is shown in Figure 14-3572 and described in Table 14-7223.

Return to Summary Table.

Host Int 1 Nesting Level Register

Table 14-10793. ICSS_INTC_NEST_LEVEL_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1104h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1104h

Figure 14-3572. ICSS_INTC_NEST_LEVEL_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>NEST_AUTO_OVR</td><td colspan="7">RESERVED</td></tr>
<tr><td>W-X</td><td colspan="7">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>NEST_HINT_1</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W-100h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NEST_HINT_1</td></tr>
<tr><td colspan="8">R/W-100h</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10795. ICSS_INTC_NEST_LEVEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_1	R/W	100h	Host Int 1 Nesting Level

109 ICSS_INTC_NEST_LEVEL_REG2 Register (Offset = 1108h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG2 is shown in Figure 14-3573 and described in Table 14-7225.

Return to Summary Table.

Host Int 2 Nesting Level Register

Table 14-10796. ICSS_INTC_NEST_LEVEL_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1108h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1108h

Figure 14-3573. ICSS_INTC_NEST_LEVEL_REG2 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_2
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_2							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10798. ICSS_INTC_NEST_LEVEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_2	R/W	100h	Host Int 2 Nesting Level

110 ICSS_INTC_NEST_LEVEL_REG3 Register (Offset = 110Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG3 is shown in Figure 14-3574 and described in Table 14-7227.

Return to Summary Table.

Host Int 3 Nesting Level Register

Table 14-10799. ICSS_INTC_NEST_LEVEL_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 110Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 110Ch

Figure 14-3574. ICSS_INTC_NEST_LEVEL_REG3 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_3
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_3							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10801. ICSS_INTC_NEST_LEVEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_3	R/W	100h	Host Int 3 Nesting Level

111 ICSS_INTC_NEST_LEVEL_REG4 Register (Offset = 1110h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG4 is shown in Figure 14-3575 and described in Table 14-7229.

Return to Summary Table.

Host Int 4 Nesting Level Register

Table 14-10802. ICSS_INTC_NEST_LEVEL_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1110h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1110h

Figure 14-3575. ICSS_INTC_NEST_LEVEL_REG4 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_4
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_4							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10804. ICSS_INTC_NEST_LEVEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_4	R/W	100h	Host Int 4 Nesting Level

112 ICSS_INTC_NEST_LEVEL_REG5 Register (Offset = 1114h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG5 is shown in Figure 14-3576 and described in Table 14-7231.

Return to Summary Table.

Host Int 5 Nesting Level Register

Table 14-10805. ICSS_INTC_NEST_LEVEL_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1114h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1114h

Figure 14-3576. ICSS_INTC_NEST_LEVEL_REG5 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_5
R/W-X							R/W-100h

7	6	5	4	3	2	1	0
NEST_HINT_5							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10807. ICSS_INTC_NEST_LEVEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_5	R/W	100h	Host Int 5 Nesting Level

113 ICSS_INTC_NEST_LEVEL_REG6 Register (Offset = 1118h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG6 is shown in Figure 14-3577 and described in Table 14-7233.

Return to Summary Table.

Host Int 6 Nesting Level Register

Table 14-10808. ICSS_INTC_NEST_LEVEL_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1118h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1118h

Figure 14-3577. ICSS_INTC_NEST_LEVEL_REG6 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>NEST_AUTO_OVR</td><td colspan="7">RESERVED</td></tr>
<tr><td>W-X</td><td colspan="7">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>NEST_HINT_6</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W-100h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NEST_HINT_6</td></tr>
<tr><td colspan="8">R/W-100h</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10810. ICSS_INTC_NEST_LEVEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_6	R/W	100h	Host Int 6 Nesting Level

114 ICSS_INTC_NEST_LEVEL_REG7 Register (Offset = 111Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG7 is shown in Figure 14-3578 and described in Table 14-7235.

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Host Int 7 Nesting Level Register

Table 14-10811. ICSS_INTC_NEST_LEVEL_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 111Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 111Ch

Figure 14-3578. ICSS_INTC_NEST_LEVEL_REG7 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_7
R/W-X							R/W-100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_7							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10813. ICSS_INTC_NEST_LEVEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_7	R/W	100h	Host Int 7 Nesting Level

115 ICSS_INTC_NEST_LEVEL_REG8 Register (Offset = 1120h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG8 is shown in Figure 14-3579 and described in Table 14-7237.

Return to Summary Table.

Host Int 8 Nesting Level Register

Table 14-10814. ICSS_INTC_NEST_LEVEL_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1120h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1120h

Figure 14-3579. ICSS_INTC_NEST_LEVEL_REG8 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_8
R/W-X							R/W-100h

7	6	5	4	3	2	1	0
NEST_HINT_8							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10816. ICSS_INTC_NEST_LEVEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_8	R/W	100h	Host Int 8 Nesting Level

116 ICSS_INTC_NEST_LEVEL_REG9 Register (Offset = 1124h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG9 is shown in Figure 14-3580 and described in Table 14-7239.

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Host Int 9 Nesting Level Register

Table 14-10817. ICSS_INTC_NEST_LEVEL_REG9 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1124h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1124h

Figure 14-3580. ICSS_INTC_NEST_LEVEL_REG9 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_9
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_9							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10819. ICSS_INTC_NEST_LEVEL_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_9	R/W	100h	Host Int 9 Nesting Level

117 ICSS_INTC_NEST_LEVEL_REG10 Register (Offset = 1128h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG10 is shown in Figure 14-3581 and described in Table 14-7241.

Return to Summary Table.

Host Int 10 Nesting Level Register

Table 14-10820. ICSS_INTC_NEST_LEVEL_REG10 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1128h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1128h

Figure 14-3581. ICSS_INTC_NEST_LEVEL_REG10 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_10
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_10							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10822. ICSS_INTC_NEST_LEVEL_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_10	R/W	100h	Host Int 10 Nesting Level

118 ICSS_INTC_NEST_LEVEL_REG11 Register (Offset = 112Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG11 is shown in Figure 14-3582 and described in Table 14-7243.

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Host Int 11 Nesting Level Register

Table 14-10823. ICSS_INTC_NEST_LEVEL_REG11 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 112Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 112Ch

Figure 14-3582. ICSS_INTC_NEST_LEVEL_REG11 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_11
R/W-X							R/W-100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_11							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10825. ICSS_INTC_NEST_LEVEL_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_11	R/W	100h	Host Int 11 Nesting Level

119 ICSS_INTC_NEST_LEVEL_REG12 Register (Offset = 1130h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG12 is shown in Figure 14-3583 and described in Table 14-7245.

Return to Summary Table.

Host Int 11 Nesting Level Register

Table 14-10826. ICSS_INTC_NEST_LEVEL_REG12 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1130h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1130h

Figure 14-3583. ICSS_INTC_NEST_LEVEL_REG12 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_12
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_12							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10828. ICSS_INTC_NEST_LEVEL_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_12	R/W	100h	Host Int 12 Nesting Level

120 ICSS_INTC_NEST_LEVEL_REG13 Register (Offset = 1134h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG13 is shown in Figure 14-3584 and described in Table 14-7247.

Return to Summary Table.

Host Int 11 Nesting Level Register

Table 14-10829. ICSS_INTC_NEST_LEVEL_REG13 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1134h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1134h

Figure 14-3584. ICSS_INTC_NEST_LEVEL_REG13 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_13
R/W-X							R/W-100h

7	6	5	4	3	2	1	0
NEST_HINT_13							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10831. ICSS_INTC_NEST_LEVEL_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_13	R/W	100h	Host Int 13 Nesting Level

121 ICSS_INTC_NEST_LEVEL_REG14 Register (Offset = 1138h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG14 is shown in Figure 14-3585 and described in Table 14-7249.

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Host Int 11 Nesting Level Register

Table 14-10832. ICSS_INTC_NEST_LEVEL_REG14 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1138h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1138h

Figure 14-3585. ICSS_INTC_NEST_LEVEL_REG14 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_14
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_14							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10834. ICSS_INTC_NEST_LEVEL_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_14	R/W	100h	Host Int 14 Nesting Level

122 ICSS_INTC_NEST_LEVEL_REG15 Register (Offset = 113Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG15 is shown in Figure 14-3586 and described in Table 14-7251.

Return to Summary Table.

Host Int 11 Nesting Level Register

Table 14-10835. ICSS_INTC_NEST_LEVEL_REG15 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 113Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 113Ch

Figure 14-3586. ICSS_INTC_NEST_LEVEL_REG15 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_15
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_15							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10837. ICSS_INTC_NEST_LEVEL_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_15	R/W	100h	Host Int 15 Nesting Level

123 ICSS_INTC_NEST_LEVEL_REG16 Register (Offset = 1140h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG16 is shown in Figure 14-3587 and described in Table 14-7253.

Return to Summary Table.

Host Int 11 Nesting Level Register

Table 14-10838. ICSS_INTC_NEST_LEVEL_REG16 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1140h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1140h

Figure 14-3587. ICSS_INTC_NEST_LEVEL_REG16 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_16
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_16							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10840. ICSS_INTC_NEST_LEVEL_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_16	R/W	100h	Host Int 16 Nesting Level

124 ICSS_INTC_NEST_LEVEL_REG17 Register (Offset = 1144h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG17 is shown in Figure 14-3588 and described in Table 14-7255.

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Host Int 11 Nesting Level Register

Table 14-10841. ICSS_INTC_NEST_LEVEL_REG17 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1144h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1144h

Figure 14-3588. ICSS_INTC_NEST_LEVEL_REG17 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>NEST_AUTO_OVR</td><td colspan="7">RESERVED</td></tr>
<tr><td>W-X</td><td colspan="7">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>NEST_HINT_17</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W-100h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NEST_HINT_17</td></tr>
<tr><td colspan="8">R/W-100h</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10843. ICSS_INTC_NEST_LEVEL_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_17	R/W	100h	Host Int 17 Nesting Level

125 ICSS_INTC_NEST_LEVEL_REG18 Register (Offset = 1148h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG18 is shown in Figure 14-3589 and described in Table 14-7257.

Return to Summary Table.

Host Int 11 Nesting Level Register

Table 14-10844. ICSS_INTC_NEST_LEVEL_REG18 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1148h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1148h

Figure 14-3589. ICSS_INTC_NEST_LEVEL_REG18 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_18
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_18							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-10846. ICSS_INTC_NEST_LEVEL_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_18	R/W	100h	Host Int 18 Nesting Level

126 ICSS_INTC_NEST_LEVEL_REG19 Register (Offset = 114Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG19 is shown in Figure 14-3590 and described in Table 14-7259.

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Host Int 11 Nesting Level Register

Table 14-10847. ICSS_INTC_NEST_LEVEL_REG19 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 114Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 114Ch

Figure 14-3590. ICSS_INTC_NEST_LEVEL_REG19 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_19
R/W-X							R/W-100h

7	6	5	4	3	2	1	0
NEST_HINT_19							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 14-10849. ICSS_INTC_NEST_LEVEL_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_19	R/W	100h	Host Int 19 Nesting Level

127 ICSS_INTC_ENABLE_HINT_REG0 Register (Offset = 1500h) [reset = X]

ICSS_INTC_ENABLE_HINT_REG0 is shown in Figure 14-3591 and described in Table 14-7261.

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Host Int Enable Register 0

Table 14-10850. ICSS_INTC_ENABLE_HINT_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	3002 1500h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	300A 1500h

Figure 14-3591. ICSS_INTC_ENABLE_HINT_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				ENABLE_HINT_19	ENABLE_HINT_18	ENABLE_HINT_17	ENABLE_HINT_16
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ENABLE_HINT_15	ENABLE_HINT_14	ENABLE_HINT_13	ENABLE_HINT_12	ENABLE_HINT_11	ENABLE_HINT_10	ENABLE_HINT_9	ENABLE_HINT_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ENABLE_HINT_7	ENABLE_HINT_6	ENABLE_HINT_5	ENABLE_HINT_4	ENABLE_HINT_3	ENABLE_HINT_2	ENABLE_HINT_1	ENABLE_HINT_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10852. ICSS_INTC_ENABLE_HINT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	ENABLE_HINT_19	R/W	0h	Enable for Host Int 19
18	ENABLE_HINT_18	R/W	0h	Enable for Host Int 18
17	ENABLE_HINT_17	R/W	0h	Enable for Host Int 17
16	ENABLE_HINT_16	R/W	0h	Enable for Host Int 16
15	ENABLE_HINT_15	R/W	0h	Enable for Host Int 15
14	ENABLE_HINT_14	R/W	0h	Enable for Host Int 14
13	ENABLE_HINT_13	R/W	0h	Enable for Host Int 13
12	ENABLE_HINT_12	R/W	0h	Enable for Host Int 12
11	ENABLE_HINT_11	R/W	0h	Enable for Host Int 11
10	ENABLE_HINT_10	R/W	0h	Enable for Host Int 10
9	ENABLE_HINT_9	R/W	0h	Enable for Host Int 9
8	ENABLE_HINT_8	R/W	0h	Enable for Host Int 8
7	ENABLE_HINT_7	R/W	0h	Enable for Host Int 7
6	ENABLE_HINT_6	R/W	0h	Enable for Host Int 6
5	ENABLE_HINT_5	R/W	0h	Enable for Host Int 5
4	ENABLE_HINT_4	R/W	0h	Enable for Host Int 4

Table 14-10852. ICSS_INTC_ENABLE_HINT_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ENABLE_HINT_3	R/W	0h	Enable for Host Int 3
2	ENABLE_HINT_2	R/W	0h	Enable for Host Int 2
1	ENABLE_HINT_1	R/W	0h	Enable for Host Int 1
0	ENABLE_HINT_0	R/W	0h	Enable for Host Int 0

14.3.6.1.8 PRU_UART Registers

Table 14-10853. ICSS_G_PR1_ICSS_UART_UART_SLV Registers, Base Address=3002 8000h, Length=64

Offset	Length	Register Name	PRU_ICSSG0 Physical Address	PRU_ICSSG1 Physical Address
0h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_RBR	3002 8000h	300A 8000h
0h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_THR	3002 8000h	300A 8000h
4h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_IER	3002 8004h	300A 8004h
8h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_IIR	3002 8008h	300A 8008h
8h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_FCR	3002 8008h	300A 8008h
Ch	32	ICSS_G_PR1_ICSS_UART_UART_SLV_LCR	3002 800Ch	300A 800Ch
10h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_MCR	3002 8010h	300A 8010h
14h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_LSR	3002 8014h	300A 8014h
18h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_MSR	3002 8018h	300A 8018h
1Ch	32	ICSS_G_PR1_ICSS_UART_UART_SLV_SCR	3002 801Ch	300A 801Ch
20h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_DLL	3002 8020h	300A 8020h
24h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_DLH	3002 8024h	300A 8024h
28h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_REVID1	3002 8028h	300A 8028h
2Ch	32	ICSS_G_PR1_ICSS_UART_UART_SLV_REVID2	3002 802Ch	300A 802Ch
30h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT	3002 8030h	300A 8030h
34h	32	ICSS_G_PR1_ICSS_UART_UART_SLV_MDR	3002 8034h	300A 8034h

14.3.6.1.9 ICSS_G_PR1_ICSS_UART_UART_SLV_RBR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_RBR Register (Offset = 0h) [reset = 0h]

Receiver Buffer Register (read only) The UART receiver section consists of a receiver shift register (RSR) and a receiver buffer register (RBR). When the UART is in the FIFO mode, RBR is a 16-byte FIFO. Timing is supplied by the 16x receiver clock or 13x receiver clock by programming OSM_SEL bit field of MDR register. Receiver section control is a function of the line control register (LCR). RSR receives serial data from the UARTn_RXD pin. Then RSR concatenates the data and moves it into RBR (or the receiver FIFO). In the non-FIFO mode, when a character is placed in RBR and the receiver data-ready interrupt is enabled (DR = 1 in IER), an interrupt is generated. This interrupt is cleared when the character is read from RBR. In the FIFO mode, the interrupt is generated when the FIFO is filled to the trigger level selected in the FIFO control register (FCR), and it is cleared when the FIFO contents drop below the trigger level.

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Table 14-10854. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8000h**
PRU_ICSSG1	**300A 8000h**

Figure 14-3592. ICSS_G_PR1_ICSS_UART_UART_SLV_RBR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-10856. ICSS_G_PR1_ICSS_UART_UART_SLV_RBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATA	R	0h	Received Data

14.3.6.1.10 ICSS_G_PR1_ICSS_UART_UART_SLV_THR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_THR Register (Offset = 0h) [reset = 0h]

The transmitter holding register (THR) (write only) The UART transmitter section consists of a transmitter hold register (THR) and a transmitter shift register (TSR). When the UART is in the FIFO mode, THR is a 16-byte FIFO. Transmitter section control is a function of the line control register (LCR). THR receives data from the internal data bus and when TSR is idle, the UART moves the data from THR to TSR. The UART serializes the data in TSR and transmits the data on the TX pin. In the non-FIFO mode, if THR is empty and the THR empty (THRE) interrupt is enabled (ETBEI = 1 in IER), an interrupt is generated. This interrupt is cleared when a character is loaded into THR or the interrupt identification register (IIR) is read. In the FIFO mode, the interrupt is generated when the transmitter FIFO is empty, and it is cleared when at least one byte is loaded into the FIFO or IIR is read.

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Table 14-10857. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8000h**
PRU_ICSSG1	**300A 8000h**

Figure 14-3593. ICSS_G_PR1_ICSS_UART_UART_SLV_THR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATA							
W							
0h							

Table 14-10859. ICSS_G_PR1_ICSS_UART_UART_SLV_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATA	W	0h	Data to transmit

14.3.6.1.11 ICSS_G_PR1_ICSS_UART_UART_SLV_IER Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_IER Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) is used to individually enable or disable each type of interrupt request that can be generated by the UART. Each interrupt request that is enabled in IER is forwarded to the CPU.

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Table 14-10860. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	3002 8004h
PRU_ICSSG1	300A 8004h

Figure 14-3594. ICSS_G_PR1_ICSS_UART_UART_SLV_IER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EDSSI	ELSI	ETBEI	ERBI
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-10862. ICSS_G_PR1_ICSS_UART_UART_SLV_IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EDSSI	R/W	0h	Enable for Modem Status Interrupt
2	ELSI	R/W	0h	Enable for Receiver Line Status Interrupt 0h Receiver line status interrupt is disabled. 1h Received line status is enabled
1	ETBEI	R/W	0h	Enable for Transmitter Holding Register Empty Interrupt 0h Transmitter holding register empty interrupt is disabled. 1h Transmitter holding register empty interrupt is enabled.
0	ERBI	R/W	0h	Enable for Receiver Data Available Interrupt 0h Receiver data available interrupt and character timeout indication interrupt is disabled. 1h Receiver data available interrupt and character timeout indication interrupt is enabled.

14.3.6.1.12 ICSS_G_PR1_ICSS_UART_UART_SLV_IIR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_IIR Register (Offset = 8h) [reset = 1h]

The interrupt identification register (IIR) is a read-only register at the same address as the FIFO control register (FCR), which is a write-only register. When an interrupt is generated and enabled in the interrupt enable register (IER), IIR indicates that an interrupt is pending in the IPEND bit and encodes the type of interrupt in the INTID bits. Reading IIR clears any THR empty (THRE) interrupts that are pending.

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Table 14-10863. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8008h**
PRU_ICSSG1	**300A 8008h**

Figure 14-3595. ICSS_G_PR1_ICSS_UART_UART_SLV_IIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FIFOEN		RESERVED		INTID			IPEND
R		NONE		R			R
0h		0h		0h			1h

Table 14-10865. ICSS_G_PR1_ICSS_UART_UART_SLV_IIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved

7:6	FIFOEN	R	0h	FIFOs enabled
				`0h Non-FIFO mode`
				`1h-2h Reserved`
				`3h FIFOs are enabled. FIFOEN bit in the FIFO control register (FCR) is set to 1.`

5:4	RESERVED	NONE	0h	Reserved

3:1	INTID	R	0h	Interrupt Type
				`0h Reserved`
				`1h Transmitter holding register empty (priority 3)`
				`2h Receiver data available (priority 2)`
				`3h Receiver line status (priority 1, highest)`
				`4h-5h Reserved`
				`6h Character timeout indication (priority 2)`
				`7h Reserved`

Table 14-10865. ICSS_G_PR1_ICSS_UART_UART_SLV_IIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

0	IPEND	R	1h	Interrupt pending.
				When any UART interrupt is generated and is enabled in IER, IPEND is forced to 0. IPEND remains 0 until all pending interrupts are cleared or until a hardware reset occurs. If no interrupts are enabled, IPEND is never forced to 0.
				`0h Interrupts pending`
				`1h No interrupts pending`

14.3.6.1.13 ICSS_G_PR1_ICSS_UART_UART_SLV_FCR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_FCR Register (Offset = 8h) [reset = 0h]

FIFO Control Register (write only) The FIFO control register (FCR) is a write-only register at the same address as the interrupt identification register (IIR), which is a read-only register.

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Table 14-10866. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	3002 8008h
PRU_ICSSG1	300A 8008h

Figure 14-3596. ICSS_G_PR1_ICSS_UART_UART_SLV_FCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RXFITL		RESERVED		DMAMODE1	TXCLR	RXCLR	FIFOEN
W		NONE		W	W	W	W
0h		0h		1h	0h	0h	0h

Table 14-10868. ICSS_G_PR1_ICSS_UART_UART_SLV_FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved

7:6	RXFITL	W	0h	Receiver FIFO trigger level.
				RXFIFTL sets the trigger level for the receiver FIFO.
				When the trigger level is reached, a receiver data-ready interrupt is generated (if the interrupt request is enabled).
				Once the FIFO drops below the trigger level, the interrupt is cleared.
				`0h 1 byte`
				`1h 4 bytes`
				`2h 8 bytes`
				`3h 14 bytes`

5:4	RESERVED	NONE	0h	Reserved

3	DMAMODE1	W	1h	DMA MODE1 enable if FIFOs are enabled.
				Always write 1 to DMAMODE1.
				After a hardware reset, change DMAMODE1 from 0 to 1.
				DMAMODE1 = 1 is a requirement for proper communication between the UART and the EDMA controller.
				`0h DMA MODE 1 is disabled`
				`1h DMA MODE 1 is enabled`

Table 14-10868. ICSS_G_PR1_ICSS_UART_UART_SLV_FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TXCLR	W	0h	Transmitter FIFO clear. Write a 1 to TXCLR to clear the bit. 0h No effect 1h Clears transmitter FIFO and resets the transmitter FIFO counter. The shift register is not cleared.
1	RXCLR	W	0h	Receiver FIFO clear. Write a 1 to RXCLR to clear the bit. 0h No effect 1h Clears receiver FIFO and resets the receiver FIFO counter. The shift register is not cleared.
0	FIFOEN	W	0h	Transmitter and receiver FIFOs mode enable. FIFOEN must be set before other FCR bits are written to or the FCR bits are not programmed. Clearing this bit clears the FIFO counters. 0h Non-FIFO mode. The transmitter and receiver FIFOs are disabled, and the FIFO pointers are cleared. 1h FIFO mode. The transmitter and receiver FIFOs are enabled.

14.3.6.1.14 ICSS_G_PR1_ICSS_UART_UART_SLV_LCR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_LCR Register (Offset = Ch) [reset = 0h]

Line Control Register (LCR) The system programmer controls the format of the asynchronous data communication exchange by using LCR. In addition, the programmer can retrieve, inspect, and modify the content of LCR; this eliminates the need for separate storage of the line characteristics in system memory.

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Table 14-10869. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 800Ch**
PRU_ICSSG1	**300A 800Ch**

Figure 14-3597. ICSS_G_PR1_ICSS_UART_UART_SLV_LCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DLAB	BC	SP	EPS	PEN	STB	WLS1	WLS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10871. ICSS_G_PR1_ICSS_UART_UART_SLV_LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DLAB	R/W	0h	Divisor latch access bit. The divisor latch registers (DLL and DLH) can be accessed at dedicated addresses or at addresses shared by RBR, THR, and IER. Using the shared addresses requires toggling DLAB to change which registers are selected. If you use the dedicated addresses, you can keep DLAB = 0. 0 `Allows access to the receiver buffer register (RBR), the transmitter holding register (THR), and the interrupt enable register (IER) selected. At the address shared by RBR, THR, and DLL, the CPU can read from RBR and write to THR. At the address shared by IER and DLH, the CPU can read from and write to IER.` 1 `Allows access to the divisor latches of the baud generator during a read or write operation (DLL and DLH). At the address shared by RBR, THR, and DLL, the CPU can read from and write to DLL. At the address shared by IER and DLH, the CPU can read from and write to DLH.`

Table 14-10871. ICSS_G_PR1_ICSS_UART_UART_SLV_LCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BC	R/W	0h	Break Control 0 Break condition is disabled 1 Break condition is transmitted to the receiving UART. A break condition is a condition where the UARTn_TXD signal is forced to the spacing (cleared) state.
5	SP	R/W	0h	Stick parity. The SP bit works in conjunction with the EPS and PEN bits. 0 Stick parity is disabled 1 Stick parity is enabled -When odd parity is selected (EPS = 0), the PARITY bit is transmitted and checked as set. -When even parity is selected (EPS = 1), the PARITY bit is transmitted and checked as cleared.
4	EPS	R/W	0h	Even parity select. Selects the parity when parity is enabled (PEN = 1). The EPS bit works in conjunction with the SP and PEN bits. 0 Odd parity is selected (an odd number of logic 1s is transmitted or checked in the data and PARITY bits). 1 Even parity is selected (an even number of logic 1s is transmitted or checked in the data and PARITY bits).
3	PEN	R/W	0h	Parity enable. The PEN bit works in conjunction with the SP and EPS bits. 0 No PARITY bit is transmitted or checked. 1 Parity bit is generated in transmitted data and is checked in received data between the last data word bit and the first STOP bit.
2	STB	R/W	0h	Number of STOP bits generated. STB specifies 1, 1.5, or 2 STOP bits in each transmitted character. When STB = 1, the WLS bit determines the number of STOP bits. The receiver clocks only the first STOP bit, regardless of the number of STOP bits selected. 0 1 STOP bit is generated. 1 WLS bit determines the number of STOP bits: -When WLS = 0, 1.5 STOP bits are generated. -When WLS = 1h, 2h, or 3h, 2 STOP bits are generated.
1	WLS1	R/W	0h	Word Length Select Bit 1
0	WLS	R/W	0h	Word length select. Number of bits in each transmitted or received serial character. When STB = 1, the WLS bit determines the number of STOP bits. 0 5 bits 1 6 bits 2 7 bits 3 8 bits

14.3.6.1.15 ICSS_G_PR1_ICSS_UART_UART_SLV_MCR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_MCR Register (Offset = 10h) [reset = 0h]

Modem Control Register (MCR) The modem control register provides the ability to enable/disable the autoflow functions, and enable/disable the loopback function for diagnostic purposes.

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Table 14-10872. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8010h**
PRU_ICSSG1	**300A 8010h**

Figure 14-3598. ICSS_G_PR1_ICSS_UART_UART_SLV_MCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		AFE	LOOP	OUT2	OUT1	RTS	RESERVED
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-10874. ICSS_G_PR1_ICSS_UART_UART_SLV_MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	AFE	R/W	0h	Autoflow control enable. Autoflow control allows the UARTn_RTS and UARTn_CTS signals to provide handshaking between UARTs during data transfer. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved and should be cleared to 0. 0 `Autoflow control is disabled.` 1 `Autoflow control is enabled: -When RTS = 0, UARTnCTS is only enabled -When RTS = 1, UARTn_RTS and UARTn_CTS are enabled`
4	LOOP	R/W	0h	Loop back mode enable. LOOP is used for the diagnostic testing using the loop back feature. 0 `Loop back mode is disabled.` 1 `Loop back mode is enabled. When LOOP is set, the following occur: -The UARTn_TXD signal is set high. -The UARTn_RXD pin is disconnected -The output of the transmitter shift register (TSR) is lopped back in to the receiver shift register (RSR) input.`
3	OUT2	R/W	0h	Out2 Bit

Table 14-10874. ICSS_G_PR1_ICSS_UART_UART_SLV_MCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OUT1	R/W	0h	Out1 Bit
1	RTS	R/W	0h	RTS control. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved and should be cleared to 0. 0 `UARTn_RTS is disabled, UARTn_CTS is only enabled.` 1 `UARTn_RTS and UARTn_CTS are enabled.`
0	RESERVED	R/W	0h	Reserved

14.3.6.1.16 ICSS_G_PR1_ICSS_UART_UART_SLV_LSR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_LSR Register (Offset = 14h) [reset = 60h]

Line Status Register (LSR) LSR provides information to the CPU concerning the status of data transfers. LSR is intended for read operations only; do not write to this register. Bits 1 through 4 record the error conditions that produce a receiver line status interrupt.

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Table 14-10875. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8014h**
PRU_ICSSG1	**300A 8014h**

Figure 14-3599. ICSS_G_PR1_ICSS_UART_UART_SLV_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RXFIFOE	TEMT	THRE	BI	FE	PE	OE	DR
R	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-10877. ICSS_G_PR1_ICSS_UART_UART_SLV_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RXFIFOE	R	0h	Receiver FIFO error. *In non-FIFO mode:* 0 = There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver buffer register (RBR). 1 = There is a parity error, framing error, or break indicator in the receiver buffer register (RBR). *In FIFO mode:* 0 = There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver FIFO and there are no more errors in the receiver FIFO. 1 = At least one parity error, framing error, or break indicator in the receiver FIFO.

Table 14-10877. ICSS_G_PR1_ICSS_UART_UART_SLV_LSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TEMT	R	1h	Transmitter empty (TEMT) indicator. *In non-FIFO mode:* 0 = Either the transmitter holding register (THR) or the transmitter shift register (TSR) contains a data character. 1 = Both the transmitter holding register (THR) and the transmitter shift register (TSR) are empty. *In FIFO mode:* 0 = Either the transmitter FIFO or the transmitter shift register (TSR) contains a data character. 1 = Both the transmitter FIFO and the transmitter shift register (TSR) are empty.
5	THRE	R	1h	Transmitter holding register empty (THRE) indicator. If the THRE bit is set and the corresponding interrupt enable bit is set (ETBEI = 1 in IER), an interrupt request is generated. *In non-FIFO mode:* 0 = Transmitter holding register (THR) is not empty. THR has been loaded by the CPU. 1 = Transmitter holding register (THR) is empty (ready to accept a new character). The content of THR has been transferred to the transmitter shift register (TSR). *In FIFO mode:* 0 = Transmitter FIFO is not empty. At least one character has been written to the transmitter FIFO. You can write to the transmitter FIFO if it is not full. 1 = Transmitter FIFO is empty. The last character in the FIFO has been transferred to the transmitter shift register (TSR).
4	BI	R	0h	Break indicator. The BI bit is set whenever the receive data input (UARTn_RXD) was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the START, data, PARITY, and STOP bits. If the BI bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. *In non-FIFO mode:* 0 = No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver buffer register (RBR). 1 = A break has been detected with the character in the receiver buffer register (RBR). *In FIFO mode:* 0 = No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver FIFO and the next character to be read from the FIFO has no break indicator. 1 = A break has been detected with the character at the top of the receiver FIFO.

Table 14-10877. ICSS_G_PR1_ICSS_UART_UART_SLV_LSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	FE	R	0h	Framing error (FE) indicator. A framing error occurs when the received character does not have a valid STOP bit. In response to a framing error, the UART sets the FE bit and waits until the signal on the RX pin goes high. Once the RX signal goes high, the receiver is ready to detect a new START bit and receive new data. If the FE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. *In non-FIFO mode:* 0 = No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR). 1 = A framing error has been detected with the character in the receiver buffer register (RBR). *In FIFO mode:* 0 = No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no framing error. 1 = A framing error has been detected with the character at the top of the receiver FIFO.
2	PE	R	0h	Parity error (PE) indicator. A parity error occurs when the parity of the received character does not match the parity selected with the EPS bit in the line control register (LCR). If the PE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. *In non-FIFO mode:* 0 = No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR). 1 = A parity error has been detected with the character in the receiver buffer register (RBR). *In FIFO mode:* 0 = No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no parity error. 1 = A parity error has been detected with the character at the top of the receiver FIFO.
1	OE	R	0h	Overrun error (OE) indicator. An overrun error in the non-FIFO mode is different from an overrun error in the FIFO mode. If the OE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. *In non-FIFO mode:* 0 = No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR). 1 = Overrun error has been detected. Before the character in the receiver buffer register (RBR) could be read, it was overwritten by the next character arriving in RBR. *In FIFO mode:* 0 = No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR). 1 = Overrun error has been detected. If data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The new character overwrites the character in the shift register, but it is not transferred to the FIFO.

Table 14-10877. ICSS_G_PR1_ICSS_UART_UART_SLV_LSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DR	R	0h	Data-ready (DR) indicator for the receiver. If the DR bit is set and the corresponding interrupt enable bit is set (ERBI = 1 in IER), an interrupt request is generated. *In non-FIFO mode:* 0 = Data is not ready, or the DR bit was cleared because the character was read from the receiver buffer register (RBR). 1 = Data is ready. A complete incoming character has been received and transferred into the receiver buffer register (RBR). *In FIFO mode:* 0 = Data is not ready, or the DR bit was cleared because all of the characters in the receiver FIFO have been read. 1 = Data is ready. There is at least one unread character in the receiver FIFO. If the FIFO is empty, the DR bit is set as soon as a complete incoming character has been received and transferred into the FIFO. The DR bit remains set until the FIFO is empty again.

14.3.6.1.17 ICSS_G_PR1_ICSS_UART_UART_SLV_MSR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_MSR Register (Offset = 18h) [reset = 0h]

Modem Status Register (MSR) MSR provides information to the CPU concerning the status of modem control signals. MSR is intended for read operations only; do not write to this register.

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Table 14-10878. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8018h**
PRU_ICSSG1	**300A 8018h**

Figure 14-3600. ICSS_G_PR1_ICSS_UART_UART_SLV_MSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CD	RI	DSR	CTS	DCD	TERI	DDSR	DCTS
R	R	R	R	R	R	R	R
X	X	X	X	0h	0h	0h	0h

Table 14-10880. ICSS_G_PR1_ICSS_UART_UART_SLV_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CD	R	X	Complement of the Carrier Detect input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 3 (OUT2).
6	RI	R	X	Complement of the Ring Indicator input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 2 (OUT1).
5	DSR	R	X	Complement of the Data Set Ready input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 0 (DTR).
4	CTS	R	X	Complement of the Clear To Send input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 1 (RTS).
3	DCD	R	0h	Change in DCD indicator bit. DCD indicates that the DCD input has changed state since the last time it was read by the CPU. When DCD is set and the modem status interrupt is enabled, a modem status interrupt is generated.

Table 14-10880. ICSS_G_PR1_ICSS_UART_UART_SLV_MSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TERI	R	0h	Trailing edge of RI (TERI) indicator bit. TERI indicates that the RI input has changed from a low to a high. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.
1	DDSR	R	0h	Change in DSR indicator bit. DDSR indicates that the DSR input has changed state since the last time it was read by the CPU. When DDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated.
0	DCTS	R	0h	Change in CTS indicator bit. DCTS indicates that the CTS input has changed state since the last time it was read by the CPU. When DCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled, no interrupt is generated.

14.3.6.1.18 ICSS_G_PR1_ICSS_UART_UART_SLV_SCR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_SCR Register (Offset = 1Ch) [reset = 0h]

Scratch Pad Register (SCR) SCR is intended for programmer's use as a scratch pad. It temporarily holds the programmer's data without affecting UART operation.

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Table 14-10881. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 801Ch**
PRU_ICSSG1	**300A 801Ch**

Figure 14-3601. ICSS_G_PR1_ICSS_UART_UART_SLV_SCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-10883. ICSS_G_PR1_ICSS_UART_UART_SLV_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATA	R/W	0h	Scratch Register Bits These bits are intended for the programmer's use as a scratch pad in the sense that it temporarily holds the programmer's data without affecting any other UART operation.

14.3.6.1.19 ICSS_G_PR1_ICSS_UART_UART_SLV_DLL Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_DLL Register (Offset = 20h) [reset = 0h]

Divisor LSB Latch

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Table 14-10884. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8020h**
PRU_ICSSG1	**300A 8020h**

Figure 14-3602. ICSS_G_PR1_ICSS_UART_UART_SLV_DLL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DLL							
R/W							
0h							

Table 14-10886. ICSS_G_PR1_ICSS_UART_UART_SLV_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DLL	R/W	0h	The 8 least-significant bits (LSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator.

14.3.6.1.20 ICSS_G_PR1_ICSS_UART_UART_SLV_DLH Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_DLH Register (Offset = 24h) [reset = 0h]

Divisor MSB Latch

Return to Summary Table

Table 14-10887. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	3002 8024h
PRU_ICSSG1	300A 8024h

Figure 14-3603. ICSS_G_PR1_ICSS_UART_UART_SLV_DLH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DLH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10889. ICSS_G_PR1_ICSS_UART_UART_SLV_DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DLH	R/W	0h	The 8 most-significant bits (MSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator.

14.3.6.1.21 ICSS_G_PR1_ICSS_UART_UART_SLV_REVID1 Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_REVID1 Register (Offset = 28h) [reset = 44141102h]

Revision Identification Register 1

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Table 14-10890. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8028h**
PRU_ICSSG1	**300A 8028h**

Figure 14-3604. ICSS_G_PR1_ICSS_UART_UART_SLV_REVID1 Name Register

31	30	29	28	27	26	25	24
REVID1							
R							
11020002h							
23	22	21	20	19	18	17	16
REVID1							
R							
11020002h							
15	14	13	12	11	10	9	8
REVID1							
R							
11020002h							
7	6	5	4	3	2	1	0
REVID1							
R							
11020002h							

Table 14-10892. ICSS_G_PR1_ICSS_UART_UART_SLV_REVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REVID1	R	11020002h	Peripheral Identification Number

14.3.6.1.22 ICSS_G_PR1_ICSS_UART_UART_SLV_REVID2 Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_REVID2 Register (Offset = 2Ch) [reset = 0h]

Revision Identification Register 2

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Table 14-10893. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 802Ch**
PRU_ICSSG1	**300A 802Ch**

Figure 14-3605. ICSS_G_PR1_ICSS_UART_UART_SLV_REVID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVID2							
R							
0h							

Table 14-10895. ICSS_G_PR1_ICSS_UART_UART_SLV_REVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	REVID2	R	0h	Peripheral Identification Number

14.3.6.1.23 ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT Register (Offset = 30h) [reset = 2h]

UART PowerManagement and Emulation Register

Return to Summary Table

Table 14-10896. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8030h**
PRU_ICSSG1	**300A 8030h**

Figure 14-3606. ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>UTRST</td><td>URRST</td><td colspan="5">RESERVED</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="5">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>RESERVED</td><td>FREE</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-10898. ICSS_G_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	UTRST	R/W	0h	UART transmitter reset. Resets and enables the transmitter. 0 Transmitter is disabled and in reset state. 1 Transmitter is enabled.
13	URRST	R/W	0h	UART receiver reset. Resets and enables the receiver. 0 Receiver is disabled and in reset state. 1 Receiver is enabled.
12:2	RESERVED	NONE	0h	Reserved
1	RESERVED	R	1h	Reserved
0	FREE	R/W	0h	Free-running enable mode bit. This bit determines the emulation mode functionality of the UART. When halted, the UART can handle register read/write requests, but does not generate any transmission/ reception, interrupts or events. 0 If a transmission is not in progress, the UART halts immediately. If a transmission is in progress, the UART halts after completion of the one-word transmission. 1 Free-running mode is enabled; UART continues to run normally.

14.3.6.1.24 ICSS_G_PR1_ICSS_UART_UART_SLV_MDR Register

1 ICSS_G_PR1_ICSS_UART_UART_SLV_MDR Register (Offset = 34h) [reset = 0h]

UART Mode Definition Register

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Table 14-10899. Instance Table

Instance Name	Physical Address
PRU_ICSSG0	**3002 8034h**
PRU_ICSSG1	**300A 8034h**

Figure 14-3607. ICSS_G_PR1_ICSS_UART_UART_SLV_MDR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							OSM_SEL
NONE							R/W
0h							0h

Table 14-10901. ICSS_G_PR1_ICSS_UART_UART_SLV_MDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved

0	OSM_SEL	R/W	0h	Over-Sampling Mode Select
				`0 16x over-sampling`
				`1 13x over-sampling`

14.3.6.1.25 PRU_IEP_IEP Registers

Table 14-7296 lists the memory-mapped registers for the PRU_IEP_IEP registers. All register offset addresses not listed in Table 14-7296 should be considered as reserved locations and the register contents should not be modified.

Table 14-10902. PRU_IEP_IEP Instances

Instance	Base Address
PRU_ICSSG0_IEP0	3002 E000h
PRU_ICSSG0_IEP1	3002 F000h
PRU_ICSSG1_IEP0	300A E000h
PRU_ICSSG1_IEP1	300A F000h

Table 14-10903. PRU_ICSSG0_IEP Registers

Offset	Acronym	Register Name	PRU_ICSSG0_IEP0 Physical Address	PRU_ICSSG0_IEP1 Physical Address
0h	IEP_GLOBAL_CFG_REG	Global Configuration Register	3002 E000h	3002 F000h
4h	IEP_GLOBAL_STATUS_REG	Status Register	3002 E004h	3002 F004h
8h	IEP_COMPEN_REG	Compensation Register	3002 E008h	3002 F008h
Ch	IEP_SLOW_COMPEN_REG	Slow Compensation Register	3002 E00Ch	3002 F00Ch
10h	IEP_COUNT_REG0	64-bit Count Value Low Register	3002 E010h	3002 F010h
14h	IEP_COUNT_REG1	64-bit Count Value High Register	3002 E014h	3002 F014h
18h	IEP_CAP_CFG_REG	Capture Configuration Register	3002 E018h	3002 F018h
1Ch	IEP_CAP_STATUS_REG	Capture Status Register	3002 E01Ch	3002 F01Ch
20h	IEP_CAPR0_REG0	Capture Rise 0 Low Register	3002 E020h	3002 F020h
24h	IEP_CAPR0_REG1	Capture Rise 0 High Register	3002 E024h	3002 F024h
28h	IEP_CAPR1_REG0	Capture Rise 1 Low Register	3002 E028h	3002 F028h
2Ch	IEP_CAPR1_REG1	Capture Rise 1 High Register	3002 E02Ch	3002 F02Ch
30h	IEP_CAPR2_REG0	Capture Rise 2 Low Register	3002 E030h	3002 F030h
34h	IEP_CAPR2_REG1	Capture Rise 2 High Register	3002 E034h	3002 F034h
38h	IEP_CAPR3_REG0	Capture Rise 3 Low Register	3002 E038h	3002 F038h
3Ch	IEP_CAPR3_REG1	Capture Rise 3 High Register	3002 E03Ch	3002 F03Ch
40h	IEP_CAPR4_REG0	Capture Rise 4 Low Register	3002 E040h	3002 F040h
44h	IEP_CAPR4_REG1	Capture Rise 4 High Register	3002 E044h	3002 F044h
48h	IEP_CAPR5_REG0	Capture Rise 5 Low Register	3002 E048h	3002 F048h
4Ch	IEP_CAPR5_REG1	Capture Rise 5 High Register	3002 E04Ch	3002 F04Ch
50h	IEP_CAPR6_REG0	Capture Rise 6 Low Register	3002 E050h	3002 F050h
54h	IEP_CAPR6_REG1	Capture Rise 6 High Register	3002 E054h	3002 F054h
58h	IEP_CAPF6_REG0	Capture Fall 6 Low Register	3002 E058h	3002 F058h
5Ch	IEP_CAPF6_REG1	Capture Fall 6 High Register	3002 E05Ch	3002 F05Ch
60h	IEP_CAPR7_REG0	Capture Rise 7 Low Register	3002 E060h	3002 F060h
64h	IEP_CAPR7_REG1	Capture Rise 7 High Register	3002 E064h	3002 F064h
68h	IEP_CAPF7_REG0	Capture Fall 7 Low Register	3002 E068h	3002 F068h
6Ch	IEP_CAPF7_REG1	Capture Fall 7 High Register	3002 E06Ch	3002 F06Ch
70h	IEP_CMP_CFG_REG	Compare Configuration Register	3002 E070h	3002 F070h
74h	IEP_CMP_STATUS_REG	Compare Status Register	3002 E074h	3002 F074h
78h	IEP_CMP0_REG0	Compare 0 Low Register	3002 E078h	3002 F078h
7Ch	IEP_CMP0_REG1	Compare 0 High Register	3002 E07Ch	3002 F07Ch
80h	IEP_CMP1_REG0	Compare 1 Low Register	3002 E080h	3002 F080h

Table 14-10903. PRU_ICSSG0_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_IEP0 Physical Address	PRU_ICSSG0_IEP1 Physical Address
84h	IEP_CMP1_REG1	Compare 1 High Register	3002 E084h	3002 F084h
88h	IEP_CMP2_REG0	Compare 2 Low Register	3002 E088h	3002 F088h
8Ch	IEP_CMP2_REG1	Compare 2 High Register	3002 E08Ch	3002 F08Ch
90h	IEP_CMP3_REG0	Compare 3 Low Register	3002 E090h	3002 F090h
94h	IEP_CMP3_REG1	Compare 3 High Register	3002 E094h	3002 F094h
98h	IEP_CMP4_REG0	Compare 4 Low Register	3002 E098h	3002 F098h
9Ch	IEP_CMP4_REG1	Compare 4 High Register	3002 E09Ch	3002 F09Ch
A0h	IEP_CMP5_REG0	Compare 5 Low Register	3002 E0A0h	3002 F0A0h
A4h	IEP_CMP5_REG1	Compare 5 High Register	3002 E0A4h	3002 F0A4h
A8h	IEP_CMP6_REG0	Compare 6 Low Register	3002 E0A8h	3002 F0A8h
ACh	IEP_CMP6_REG1	Compare 6 High Register	3002 E0ACh	3002 F0ACh
B0h	IEP_CMP7_REG0	Compare 7 Low Register	3002 E0B0h	3002 F0B0h
B4h	IEP_CMP7_REG1	Compare 7 High Register	3002 E0B4h	3002 F0B4h
B8h	IEP_RXIPG0_REG	Status for the RX port which is attached to PRU0 Register	3002 E0B8h	3002 F0B8h
BCh	IEP_RXIPG1_REG	Status for the RX port which is attached to PRU1 Register	3002 E0BCh	3002 F0BCh
C0h	IEP_CMP8_REG0	Compare 8 Low Register	3002 E0C0h	3002 F0C0h
C4h	IEP_CMP8_REG1	Compare 8 High Register	3002 E0C4h	3002 F0C4h
C8h	IEP_CMP9_REG0	Compare 9 Low Register	3002 E0C8h	3002 F0C8h
CCh	IEP_CMP9_REG1	Compare 9 High Register	3002 E0CCh	3002 F0CCh
D0h	IEP_CMP10_REG0	Compare 10 Low Register	3002 E0D0h	3002 F0D0h
D4h	IEP_CMP10_REG1	Compare 10 High Register	3002 E0D4h	3002 F0D4h
D8h	IEP_CMP11_REG0	Compare 11 Low Register	3002 E0D8h	3002 F0D8h
DCh	IEP_CMP11_REG1	Compare 11 High Register	3002 E0DCh	3002 F0DCh
E0h	IEP_CMP12_REG0	Compare 12 Low Register	3002 E0E0h	3002 F0E0h
E4h	IEP_CMP12_REG1	Compare 12 High Register	3002 E0E4h	3002 F0E4h
E8h	IEP_CMP13_REG0	Compare 13 Low Register	3002 E0E8h	3002 F0E8h
ECh	IEP_CMP13_REG1	Compare 13 High Register	3002 E0ECh	3002 F0ECh
F0h	IEP_CMP14_REG0	Compare 14 Low Register	3002 E0F0h	3002 F0F0h
F4h	IEP_CMP14_REG1	Compare 14 High Register	3002 E0F4h	3002 F0F4h
F8h	IEP_CMP15_REG0	Compare 15 Low Register	3002 E0F8h	3002 F0F8h
FCh	IEP_CMP15_REG1	Compare 15 High Register	3002 E0FCh	3002 F0FCh
100h	IEP_COUNT_RESET_VAL_REG0	Reset value of the Controller Counter (lower 32-bits) Register	3002 E100h	3002 F100h
104h	IEP_COUNT_RESET_VAL_REG1	Reset value of the Controller Counter (upper 32-bits) Register	3002 E104h	3002 F104h
108h	IEP_PWM_REG	PWM Sync Out Register	3002 E108h	3002 F108h
10Ch	IEP_CAPR0_BI_REG0	Capture Big Endian Rise00 Register	3002 E10Ch	3002 F10Ch
110h	IEP_CAPR0_BI_REG1	Capture Big Endian Rise10 Register	3002 E110h	3002 F110h
114h	IEP_CAPR1_BI_REG0	Capture Big Endian Rise01 Register	3002 E114h	3002 F114h
118h	IEP_CAPR1_BI_REG1	Capture Big Endian Rise11 Register	3002 E118h	3002 F118h
11Ch	IEP_CAPR2_BI_REG0	Capture Big Endian Rise02 Register	3002 E11Ch	3002 F11Ch
120h	IEP_CAPR2_BI_REG1	Capture Big Endian Rise12 Register	3002 E120h	3002 F120h
124h	IEP_CAPR3_BI_REG0	Capture Big Endian Rise03 Register	3002 E124h	3002 F124h

Table 14-10903. PRU_ICSSG0_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_IEP0 Physical Address	PRU_ICSSG0_IEP1 Physical Address
128h	IEP_CAPR3_BI_REG1	Capture Big Endian Rise13 Register	3002 E128h	3002 F128h
12Ch	IEP_CAPR4_BI_REG0	Capture Big Endian Rise04 Register	3002 E12Ch	3002 F12Ch
130h	IEP_CAPR4_BI_REG1	Capture Big Endian Rise14 Register	3002 E130h	3002 F130h
134h	IEP_CAPR5_BI_REG0	Capture Big Endian Rise05 Register	3002 E134h	3002 F134h
138h	IEP_CAPR5_BI_REG1	Capture Big Endian Rise15 Register	3002 E138h	3002 F138h
13Ch	IEP_CAPR6_BI_REG0	Capture Big Endian Rise06 Register	3002 E13Ch	3002 F13Ch
140h	IEP_CAPR6_BI_REG1	Capture Big Endian Rise16 Register	3002 E140h	3002 F140h
144h	IEP_CAPF6_BI_REG0	Capture Big Endian Fall06 Register	3002 E144h	3002 F144h
148h	IEP_CAPF6_BI_REG1	Capture Big Endian Fall16 Register	3002 E148h	3002 F148h
14Ch	IEP_CAPR7_BI_REG0	Capture Big Endian Rise07 Register	3002 E14Ch	3002 F14Ch
150h	IEP_CAPR7_BI_REG1	Capture Big Endian Rise17 Register	3002 E150h	3002 F150h
154h	IEP_CAPF7_BI_REG0	Capture Big Endian Fall07 Register	3002 E154h	3002 F154h
158h	IEP_CAPF7_BI_REG1	Capture Big Endian Fall17 Register	3002 E158h	3002 F158h
180h	IEP_SYNC_CTRL_REG	Sync Generation Control Register	3002 E180h	3002 F180h
184h	IEP_SYNC_FIRST_STAT_REG	Sync Generation First Event Status Register	3002 E184h	3002 F184h
188h	IEP_SYNC0_STAT_REG	Sync 0 Status Register	3002 E188h	3002 F188h
18Ch	IEP_SYNC1_STAT_REG	Sync 1 Status Register	3002 E18Ch	3002 F18Ch
190h	IEP_SYNC_PWIDTH_REG	Sync Pulse Width Configure Register	3002 E190h	3002 F190h
194h	IEP_SYNC0_PERIOD_REG	Sync 0 Period Configure Register	3002 E194h	3002 F194h
198h	IEP_SYNC1_DELAY_REG	Sync 1 Delay Register	3002 E198h	3002 F198h
19Ch	IEP_SYNC_START_REG	Sync Start Configure Register	3002 E19Ch	3002 F19Ch
200h	IEP_WD_PREDIV_REG	Watchdog Pre-Divider Register	3002 E200h	3002 F200h
204h	IEP_PDI_WD_TIM_REG	PDI Watchdog Timer Configure Register	3002 E204h	3002 F204h
208h	IEP_PD_WD_TIM_REG	PD Watchdog Timer Configure Register	3002 E208h	3002 F208h
20Ch	IEP_WD_STATUS_REG	Watchdog Status Register	3002 E20Ch	3002 F20Ch
210h	IEP_WD_EXP_CNT_REG	Watchdog Timer Expiration Counter Register	3002 E210h	3002 F210h
214h	IEP_WD_CTRL_REG	Watchdog Control Register	3002 E214h	3002 F214h
300h	IEP_DIGIO_CTRL_REG	DIGIO Control Register	3002 E300h	3002 F300h
304h	IEP_DIGIO_STATUS_REG	DIGIO Status Register	3002 E304h	3002 F304h
308h	IEP_DIGIO_DATA_IN_REG	DIGIO Data Input Register	3002 E308h	3002 F308h
30Ch	IEP_DIGIO_DATA_IN_RAW_REG	DIGIO Data Input Direct Sample Register	3002 E30Ch	3002 F30Ch
310h	IEP_DIGIO_DATA_OUT_REG	DIGIO Data Output Register	3002 E310h	3002 F310h
314h	IEP_DIGIO_DATA_OUT_EN_REG	DIGIO Data Input which controls tri-state of pr<k>_edio_data_out_en[3:0] Register	3002 E314h	3002 F314h
318h	IEP_DIGIO_EXP_REG	DIGIO, Defines which RX_EOF is used Register	3002 E318h	3002 F318h

Table 14-10904. PRU_ICSSG1_IEP Registers

Offset	Acronym	Register Name	PRU_ICSSG1_IEP0 Physical Address	PRU_ICSSG1_IEP1 Physical Address
0h	IEP_GLOBAL_CFG_REG	Global Configuration Register	300A E000h	300A F000h
4h	IEP_GLOBAL_STATUS_REG	Status Register	300A E004h	300A F004h
8h	IEP_COMPEN_REG	Compensation Register	300A E008h	300A F008h
Ch	IEP_SLOW_COMPEN_REG	Slow Compensation Register	300A E00Ch	300A F00Ch

Table 14-10904. PRU_ICSSG1_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG1 _IEP0 Physical Address	PRU_ICSSG1 _IEP1 Physical Address
10h	IEP_COUNT_REG0	64-bit Count Value Low Register	300A E010h	300A F010h
14h	IEP_COUNT_REG1	64-bit Count Value High Register	300A E014h	300A F014h
18h	IEP_CAP_CFG_REG	Capture Configuration Register	300A E018h	300A F018h
1Ch	IEP_CAP_STATUS_REG	Capture Status Register	300A E01Ch	300A F01Ch
20h	IEP_CAPR0_REG0	Capture Rise 0 Low Register	300A E020h	300A F020h
24h	IEP_CAPR0_REG1	Capture Rise 0 High Register	300A E024h	300A F024h
28h	IEP_CAPR1_REG0	Capture Rise 1 Low Register	300A E028h	300A F028h
2Ch	IEP_CAPR1_REG1	Capture Rise 1 High Register	300A E02Ch	300A F02Ch
30h	IEP_CAPR2_REG0	Capture Rise 2 Low Register	300A E030h	300A F030h
34h	IEP_CAPR2_REG1	Capture Rise 2 High Register	300A E034h	300A F034h
38h	IEP_CAPR3_REG0	Capture Rise 3 Low Register	300A E038h	300A F038h
3Ch	IEP_CAPR3_REG1	Capture Rise 3 High Register	300A E03Ch	300A F03Ch
40h	IEP_CAPR4_REG0	Capture Rise 4 Low Register	300A E040h	300A F040h
44h	IEP_CAPR4_REG1	Capture Rise 4 High Register	300A E044h	300A F044h
48h	IEP_CAPR5_REG0	Capture Rise 5 Low Register	300A E048h	300A F048h
4Ch	IEP_CAPR5_REG1	Capture Rise 5 High Register	300A E04Ch	300A F04Ch
50h	IEP_CAPR6_REG0	Capture Rise 6 Low Register	300A E050h	300A F050h
54h	IEP_CAPR6_REG1	Capture Rise 6 High Register	300A E054h	300A F054h
58h	IEP_CAPF6_REG0	Capture Fall 6 Low Register	300A E058h	300A F058h
5Ch	IEP_CAPF6_REG1	Capture Fall 6 High Register	300A E05Ch	300A F05Ch
60h	IEP_CAPR7_REG0	Capture Rise 7 Low Register	300A E060h	300A F060h
64h	IEP_CAPR7_REG1	Capture Rise 7 High Register	300A E064h	300A F064h
68h	IEP_CAPF7_REG0	Capture Fall 7 Low Register	300A E068h	300A F068h
6Ch	IEP_CAPF7_REG1	Capture Fall 7 High Register	300A E06Ch	300A F06Ch
70h	IEP_CMP_CFG_REG	Compare Configuration Register	300A E070h	300A F070h
74h	IEP_CMP_STATUS_REG	Compare Status Register	300A E074h	300A F074h
78h	IEP_CMP0_REG0	Compare 0 Low Register	300A E078h	300A F078h
7Ch	IEP_CMP0_REG1	Compare 0 High Register	300A E07Ch	300A F07Ch
80h	IEP_CMP1_REG0	Compare 1 Low Register	300A E080h	300A F080h
84h	IEP_CMP1_REG1	Compare 1 High Register	300A E084h	300A F084h
88h	IEP_CMP2_REG0	Compare 2 Low Register	300A E088h	300A F088h
8Ch	IEP_CMP2_REG1	Compare 2 High Register	300A E08Ch	300A F08Ch
90h	IEP_CMP3_REG0	Compare 3 Low Register	300A E090h	300A F090h
94h	IEP_CMP3_REG1	Compare 3 High Register	300A E094h	300A F094h
98h	IEP_CMP4_REG0	Compare 4 Low Register	300A E098h	300A F098h
9Ch	IEP_CMP4_REG1	Compare 4 High Register	300A E09Ch	300A F09Ch
A0h	IEP_CMP5_REG0	Compare 5 Low Register	300A E0A0h	300A F0A0h
A4h	IEP_CMP5_REG1	Compare 5 High Register	300A E0A4h	300A F0A4h
A8h	IEP_CMP6_REG0	Compare 6 Low Register	300A E0A8h	300A F0A8h
ACh	IEP_CMP6_REG1	Compare 6 High Register	300A E0ACh	300A F0ACh
B0h	IEP_CMP7_REG0	Compare 7 Low Register	300A E0B0h	300A F0B0h
B4h	IEP_CMP7_REG1	Compare 7 High Register	300A E0B4h	300A F0B4h

Table 14-10904. PRU_ICSSG1_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG1_IEP0 Physical Address	PRU_ICSSG1_IEP1 Physical Address
B8h	IEP_RXIPG0_REG	Status for the RX port which is attached to PRU0 Register	300A E0B8h	300A F0B8h
BCh	IEP_RXIPG1_REG	Status for the RX port which is attached to PRU1 Register	300A E0BCh	300A F0BCh
C0h	IEP_CMP8_REG0	Compare 8 Low Register	300A E0C0h	300A F0C0h
C4h	IEP_CMP8_REG1	Compare 8 High Register	300A E0C4h	300A F0C4h
C8h	IEP_CMP9_REG0	Compare 9 Low Register	300A E0C8h	300A F0C8h
CCh	IEP_CMP9_REG1	Compare 9 High Register	300A E0CCh	300A F0CCh
D0h	IEP_CMP10_REG0	Compare 10 Low Register	300A E0D0h	300A F0D0h
D4h	IEP_CMP10_REG1	Compare 10 High Register	300A E0D4h	300A F0D4h
D8h	IEP_CMP11_REG0	Compare 11 Low Register	300A E0D8h	300A F0D8h
DCh	IEP_CMP11_REG1	Compare 11 High Register	300A E0DCh	300A F0DCh
E0h	IEP_CMP12_REG0	Compare 12 Low Register	300A E0E0h	300A F0E0h
E4h	IEP_CMP12_REG1	Compare 12 High Register	300A E0E4h	300A F0E4h
E8h	IEP_CMP13_REG0	Compare 13 Low Register	300A E0E8h	300A F0E8h
ECh	IEP_CMP13_REG1	Compare 13 High Register	300A E0ECh	300A F0ECh
F0h	IEP_CMP14_REG0	Compare 14 Low Register	300A E0F0h	300A F0F0h
F4h	IEP_CMP14_REG1	Compare 14 High Register	300A E0F4h	300A F0F4h
F8h	IEP_CMP15_REG0	Compare 15 Low Register	300A E0F8h	300A F0F8h
FCh	IEP_CMP15_REG1	Compare 15 High Register	300A E0FCh	300A F0FCh
100h	IEP_COUNT_RESET_VAL_REG0	Reset value of the Controller Counter (lower 32-bits) Register	300A E100h	300A F100h
104h	IEP_COUNT_RESET_VAL_REG1	Reset value of the Controller Counter (upper 32-bits) Register	300A E104h	300A F104h
108h	IEP_PWM_REG	PWM Sync Out Register	300A E108h	300A F108h
10Ch	IEP_CAPR0_BI_REG0	Capture Big Endian Rise00 Register	300A E10Ch	300A F10Ch
110h	IEP_CAPR0_BI_REG1	Capture Big Endian Rise10 Register	300A E110h	300A F110h
114h	IEP_CAPR1_BI_REG0	Capture Big Endian Rise01 Register	300A E114h	300A F114h
118h	IEP_CAPR1_BI_REG1	Capture Big Endian Rise11 Register	300A E118h	300A F118h
11Ch	IEP_CAPR2_BI_REG0	Capture Big Endian Rise02 Register	300A E11Ch	300A F11Ch
120h	IEP_CAPR2_BI_REG1	Capture Big Endian Rise12 Register	300A E120h	300A F120h
124h	IEP_CAPR3_BI_REG0	Capture Big Endian Rise03 Register	300A E124h	300A F124h
128h	IEP_CAPR3_BI_REG1	Capture Big Endian Rise13 Register	300A E128h	300A F128h
12Ch	IEP_CAPR4_BI_REG0	Capture Big Endian Rise04 Register	300A E12Ch	300A F12Ch
130h	IEP_CAPR4_BI_REG1	Capture Big Endian Rise14 Register	300A E130h	300A F130h
134h	IEP_CAPR5_BI_REG0	Capture Big Endian Rise05 Register	300A E134h	300A F134h
138h	IEP_CAPR5_BI_REG1	Capture Big Endian Rise15 Register	300A E138h	300A F138h
13Ch	IEP_CAPR6_BI_REG0	Capture Big Endian Rise06 Register	300A E13Ch	300A F13Ch
140h	IEP_CAPR6_BI_REG1	Capture Big Endian Rise16 Register	300A E140h	300A F140h
144h	IEP_CAPF6_BI_REG0	Capture Big Endian Fall06 Register	300A E144h	300A F144h
148h	IEP_CAPF6_BI_REG1	Capture Big Endian Fall16 Register	300A E148h	300A F148h
14Ch	IEP_CAPR7_BI_REG0	Capture Big Endian Rise07 Register	300A E14Ch	300A F14Ch
150h	IEP_CAPR7_BI_REG1	Capture Big Endian Rise17 Register	300A E150h	300A F150h
154h	IEP_CAPF7_BI_REG0	Capture Big Endian Fall07 Register	300A E154h	300A F154h

Table 14-10904. PRU_ICSSG1_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG1 _IEP0 Physical Address	PRU_ICSSG1 _IEP1 Physical Address
158h	IEP_CAPF7_BI_REG1	Capture Big Endian Fall17 Register	300A E158h	300A F158h
180h	IEP_SYNC_CTRL_REG	Sync Generation Control Register	300A E180h	300A F180h
184h	IEP_SYNC_FIRST_STAT_REG	Sync Generation First Event Status Register	300A E184h	300A F184h
188h	IEP_SYNC0_STAT_REG	Sync 0 Status Register	300A E188h	300A F188h
18Ch	IEP_SYNC1_STAT_REG	Sync 1 Status Register	300A E18Ch	300A F18Ch
190h	IEP_SYNC_PWIDTH_REG	Sync Pulse Width Configure Register	300A E190h	300A F190h
194h	IEP_SYNC0_PERIOD_REG	Sync 0 Period Configure Register	300A E194h	300A F194h
198h	IEP_SYNC1_DELAY_REG	Sync 1 Delay Register	300A E198h	300A F198h
19Ch	IEP_SYNC_START_REG	Sync Start Configure Register	300A E19Ch	300A F19Ch
200h	IEP_WD_PREDIV_REG	Watchdog Pre-Divider Register	300A E200h	300A F200h
204h	IEP_PDI_WD_TIM_REG	PDI Watchdog Timer Configure Register	300A E204h	300A F204h
208h	IEP_PD_WD_TIM_REG	PD Watchdog Timer Configure Register	300A E208h	300A F208h
20Ch	IEP_WD_STATUS_REG	Watchdog Status Register	300A E20Ch	300A F20Ch
210h	IEP_WD_EXP_CNT_REG	Watchdog Timer Expiration Counter Register	300A E210h	300A F210h
214h	IEP_WD_CTRL_REG	Watchdog Control Register	300A E214h	300A F214h
300h	IEP_DIGIO_CTRL_REG	DIGIO Control Register	300A E300h	300A F300h
304h	IEP_DIGIO_STATUS_REG	DIGIO Status Register	300A E304h	300A F304h
308h	IEP_DIGIO_DATA_IN_REG	DIGIO Data Input Register	300A E308h	300A F308h
30Ch	IEP_DIGIO_DATA_IN_RAW_REG	DIGIO Data Input Direct Sample Register	300A E30Ch	300A F30Ch
310h	IEP_DIGIO_DATA_OUT_REG	DIGIO Data Output Register	300A E310h	300A F310h
314h	IEP_DIGIO_DATA_OUT_EN_REG	DIGIO Data Input which controls tri-state of pr<k>_edio_data_out_en[3:0] Register	300A E314h	300A F314h
318h	IEP_DIGIO_EXP_REG	DIGIO, Defines which RX_EOF is used Register	300A E318h	300A F318h

1 IEP_GLOBAL_CFG_REG Register (Offset = 0h) [reset = X]

IEP_GLOBAL_CFG_REG is shown in Figure 14-3608 and described in Table 14-7299.

Return to Summary Table.

Global Configuration Register.

Table 14-10905. IEP_GLOBAL_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E000h
PRU_ICSSG0_IEP1	3002 F000h
PRU_ICSSG1_IEP0	300A E000h
PRU_ICSSG1_IEP1	300A F000h

Figure 14-3608. IEP_GLOBAL_CFG_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CMP_INC</td></tr>
<tr><td colspan="4">R/W-X</td><td colspan="4">R/W-5h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CMP_INC</td></tr>
<tr><td colspan="8">R/W-5h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">DEFAULT_INC</td><td colspan="3">RESERVED</td><td>CNT_ENABLE</td></tr>
<tr><td colspan="4">R/W-5h</td><td colspan="3">R/W-X</td><td>R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10907. IEP_GLOBAL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	CMP_INC	R/W	5h	Defines the increment value when compensation is active
7-4	DEFAULT_INC	R/W	5h	Defines the default increment value
3-1	RESERVED	R/W	X	
0	CNT_ENABLE	R/W	0h	Counter enable. 0h = Disables the counter. The counter maintains the current count. 1h = Enables the counter.

2 IEP_GLOBAL_STATUS_REG Register (Offset = 4h) [reset = X]

IEP_GLOBAL_STATUS_REG is shown in Figure 14-3609 and described in Table 14-7301.

Return to Summary Table.

Status Register.

Table 14-10908. IEP_GLOBAL_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E004h
PRU_ICSSG0_IEP1	3002 F004h
PRU_ICSSG1_IEP0	300A E004h
PRU_ICSSG1_IEP1	300A F004h

Figure 14-3609. IEP_GLOBAL_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							CNT_OVF
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-10910. IEP_GLOBAL_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	CNT_OVF	R/W1C	0h	Counter overflow status. 0h = No overflow 1h = Overflow occurred

3 IEP_COMPEN_REG Register (Offset = 8h) [reset = X]

IEP_COMPEN_REG is shown in Figure 14-3610 and described in Table 14-7303.

Return to Summary Table.

Compensation Register.

Table 14-10911. IEP_COMPEN_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E008h
PRU_ICSSG0_IEP1	3002 F008h
PRU_ICSSG1_IEP0	300A E008h
PRU_ICSSG1_IEP1	300A F008h

Figure 14-3610. IEP_COMPEN_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="9">RESERVED</td><td colspan="23">COMPEN_CNT</td></tr>
<tr><td colspan="9">R/W-X</td><td colspan="23">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10913. IEP_COMPEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-0	COMPEN_CNT	R/W	0h	0h = Compensation is disabled counter inc by default_inc <value> compensation is enabled until compen_cnt decrements to 0 rd see the current compen_cnt decremented on every iep_clk when the value in [22-0]COMPEN_CNT is not equal to 0h, then count increments by cmp_inc. Note: that slow_compen_cnt must be set to zero if compen_cnt is not zero.

4 IEP_SLOW_COMPEN_REG Register (Offset = Ch) [reset = 0h]

IEP_SLOW_COMPEN_REG is shown in Figure 14-3611 and described in Table 14-7305.

Return to Summary Table.

Slow Compensation Register.

Table 14-10914. IEP_SLOW_COMPEN_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E00Ch
PRU_ICSSG0_IEP1	3002 F00Ch
PRU_ICSSG1_IEP0	300A E00Ch
PRU_ICSSG1_IEP1	300A F00Ch

Figure 14-3611. IEP_SLOW_COMPEN_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">SLOW_COMPEN_CNT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10916. IEP_SLOW_COMPEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SLOW_COMPEN_CNT	R/W	0h	Slow compensation counter. Write 0h = Slow compensation is disabled and counter will increment by DEFAULT_INC. Write Nh = Compensation is enabled for 1 count for every SLOW_COMPEN_CNT cycle, this is free running and continuous until software clears the MMR. For example, SLOW_COMPEN_CNT = 16, every 16 clock cycles the compensation value is used for 1 count. Note: COMPEN_CNT MUST be set to zero IF SLOW_COMPEN_CNT is not zero. Software can read the number of cycles left until the compensation event. For example, software writes SLOW_COMPEN_CNT = 100h and reads SLOW_COMPEN_CNT = 7h = This means in 6 more IEP_CLK cycles before the counter reaches 1h for the compensation event. If software writes SLOW_COMPEN_CNT = 8000h before compensation event, then the counter will reset to 8000h.

5 IEP_COUNT_REG0 Register (Offset = 10h) [reset = 0h]

IEP_COUNT_REG0 is shown in Figure 14-3612 and described in Table 14-7307.

Return to Summary Table.

64-bit Count Value Low Register.

Table 14-10917. IEP_COUNT_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E010h
PRU_ICSSG0_IEP1	3002 F010h
PRU_ICSSG1_IEP0	300A E010h
PRU_ICSSG1_IEP1	300A F010h

Figure 14-3612. IEP_COUNT_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT_LO																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10919. IEP_COUNT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT_LO	R/W	0h	When Shadow Mode is disabled, this is the 64-bit count value (lower 32-bits). The count is incremented (DEFAULT_INC or CMP_INC) on every positive edge of ICSSGn_IEP_CLK (200MHz) or ICSSGn_ICLK. In 64-bit mode, reading this value locks the IEP_COUNT_REG1[31-0] COUNT_HI value. When Shadow Mode is enabled, the counter will be in 32-bit mode.

6 IEP_COUNT_REG1 Register (Offset = 14h) [reset = 0h]

IEP_COUNT_REG1 is shown in Figure 14-3613 and described in Table 14-7309.

Return to Summary Table.

64-bit Count Value High Register.

Table 14-10920. IEP_COUNT_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E014h
PRU_ICSSG0_IEP1	3002 F014h
PRU_ICSSG1_IEP0	300A E014h
PRU_ICSSG1_IEP1	300A F014h

Figure 14-3613. IEP_COUNT_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">COUNT_HI</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10922. IEP_COUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT_HI	R/W	0h	When Shadow Mode is disabled: The controller upper 32-bits of the 64-bit count value. The count is incremented (DEFAULT_INC or CMP_INC) on every positive edge of ICSSGn_IEP_CLK (200MHz) or ICSSGn_ICLK. This value only updates when software reads IEP_COUNT_REG0[31-0] COUNT_LO. When Shadow Mode is enabled: This counts the counter reset events caused by CMP0. But, limited to 24-bit counter, so software must clear before this threshold is met. Any writes to COUNT_LO or COUNT_HI will reset COUNT_HI to 0. Max COUNT_HI is 0xFF_FFFF and will stop at this value

7 IEP_CAP_CFG_REG Register (Offset = 18h) [reset = X]

IEP_CAP_CFG_REG is shown in Figure 14-3614 and described in Table 14-7311.

Return to Summary Table.

Capture Configuration Register.

Table 14-10923. IEP_CAP_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E018h
PRU_ICSSG0_IEP1	3002 F018h
PRU_ICSSG1_IEP0	300A E018h
PRU_ICSSG1_IEP1	300A F018h

Figure 14-3614. IEP_CAP_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								EXT_CAP_EN						CAP_ASYNC_EN	
R/W-X								R/W-0h						R/W-7Fh	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP_ASYNC_EN						CAP_EN									
R/W-7Fh						R/W-0h									

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10925. IEP_CAP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-18	EXT_CAP_EN	R/W	0h	
17-10	CAP_ASYNC_EN	R/W	7Fh	Synchronization of the capture inputs to the ICSS_IEP_CLK/ ICSS_VCLK_CLK enable. Note if input capture signal is asynchronous to ICSS_IEP_CLK, enabling synchronization will cause the capture contents to be invalid. CAP_ASYNC_EN[n] maps to CAPR[n]. 0h = Disable synchronization 1h = Enable synchronization
9-0	CAP_EN	R/W	0h	

8 IEP_CAP_STATUS_REG Register (Offset = 1Ch) [reset = X]

IEP_CAP_STATUS_REG is shown in Figure 14-3615 and described in Table 14-7313.

Return to Summary Table.

Capture Status Register.

Table 14-10926. IEP_CAP_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E01Ch
PRU_ICSSG0_IEP1	3002 F01Ch
PRU_ICSSG1_IEP0	300A E01Ch
PRU_ICSSG1_IEP1	300A F01Ch

Figure 14-3615. IEP_CAP_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								CAP_RAW							
R-X								R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CAP_VALID										
R-X					R-0h										

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10928. IEP_CAP_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	CAP_RAW	R	0h	Raw/Current status bit for each of the capture registers, where CAP_RAW[n] maps to CAPR[n]. 0h = Current state is low. 1h = Current state is high.
15-11	RESERVED	R	X	
10-0	CAP_VALID	R	0h	A Capture Valid Status , OR tree 0h = No Hit for any cap event 1h = Hit for 1 or more cap event is pending

9 IEP_CAPR0_REG0 Register (Offset = 20h) [reset = 0h]

IEP_CAPR0_REG0 is shown in Figure 14-3616 and described in Table 14-7315.

Return to Summary Table.

Capture Rise 0 Low Register.

Table 14-10929. IEP_CAPR0_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E020h
PRU_ICSSG0_IEP1	3002 F020h
PRU_ICSSG1_IEP0	300A E020h
PRU_ICSSG1_IEP1	300A F020h

Figure 14-3616. IEP_CAPR0_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR0_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10931. IEP_CAPR0_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR0_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

10 IEP_CAPR0_REG1 Register (Offset = 24h) [reset = 0h]

IEP_CAPR0_REG1 is shown in Figure 14-3617 and described in Table 14-7317.

Return to Summary Table.

Capture Rise 0 High Register.

Table 14-10932. IEP_CAPR0_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E024h
PRU_ICSSG0_IEP1	3002 F024h
PRU_ICSSG1_IEP0	300A E024h
PRU_ICSSG1_IEP1	300A F024h

Figure 14-3617. IEP_CAPR0_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR0_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10934. IEP_CAPR0_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR0_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

11 IEP_CAPR1_REG0 Register (Offset = 28h) [reset = 0h]

IEP_CAPR1_REG0 is shown in Figure 14-3618 and described in Table 14-7319.

Return to Summary Table.

Capture Rise 1 Low Register.

Table 14-10935. IEP_CAPR1_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E028h
PRU_ICSSG0_IEP1	3002 F028h
PRU_ICSSG1_IEP0	300A E028h
PRU_ICSSG1_IEP1	300A F028h

Figure 14-3618. IEP_CAPR1_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR1_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10937. IEP_CAPR1_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR1_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

12 IEP_CAPR1_REG1 Register (Offset = 2Ch) [reset = 0h]

IEP_CAPR1_REG1 is shown in Figure 14-3619 and described in Table 14-7321.

Return to Summary Table.

Capture Rise 1 High Register.

Table 14-10938. IEP_CAPR1_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E02Ch
PRU_ICSSG0_IEP1	3002 F02Ch
PRU_ICSSG1_IEP0	300A E02Ch
PRU_ICSSG1_IEP1	300A F02Ch

Figure 14-3619. IEP_CAPR1_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR1_1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-10940. IEP_CAPR1_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR1_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

13 IEP_CAPR2_REG0 Register (Offset = 30h) [reset = 0h]

IEP_CAPR2_REG0 is shown in Figure 14-3620 and described in Table 14-7323.

Return to Summary Table.

Capture Rise 2 Low Register

Table 14-10941. IEP_CAPR2_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E030h
PRU_ICSSG0_IEP1	3002 F030h
PRU_ICSSG1_IEP0	300A E030h
PRU_ICSSG1_IEP1	300A F030h

Figure 14-3620. IEP_CAPR2_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR2_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10943. IEP_CAPR2_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR2_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

14 IEP_CAPR2_REG1 Register (Offset = 34h) [reset = 0h]

IEP_CAPR2_REG1 is shown in Figure 14-3621 and described in Table 14-7325.

Return to Summary Table.

Capture Rise 2 High Register.

Table 14-10944. IEP_CAPR2_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E034h
PRU_ICSSG0_IEP1	3002 F034h
PRU_ICSSG1_IEP0	300A E034h
PRU_ICSSG1_IEP1	300A F034h

Figure 14-3621. IEP_CAPR2_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR2_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10946. IEP_CAPR2_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR2_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

15 IEP_CAPR3_REG0 Register (Offset = 38h) [reset = 0h]

IEP_CAPR3_REG0 is shown in Figure 14-3622 and described in Table 14-7327.

Return to Summary Table.

Capture Rise 3 Low Register.

Table 14-10947. IEP_CAPR3_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E038h
PRU_ICSSG0_IEP1	3002 F038h
PRU_ICSSG1_IEP0	300A E038h
PRU_ICSSG1_IEP1	300A F038h

Figure 14-3622. IEP_CAPR3_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR3_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10949. IEP_CAPR3_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR3_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

16 IEP_CAPR3_REG1 Register (Offset = 3Ch) [reset = 0h]

IEP_CAPR3_REG1 is shown in Figure 14-3623 and described in Table 14-7329.

Return to Summary Table.

Capture Rise 3 High Register.

Table 14-10950. IEP_CAPR3_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E03Ch
PRU_ICSSG0_IEP1	3002 F03Ch
PRU_ICSSG1_IEP0	300A E03Ch
PRU_ICSSG1_IEP1	300A F03Ch

Figure 14-3623. IEP_CAPR3_REG1 Register

31-0
CAPR3_1
R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10952. IEP_CAPR3_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR3_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

17 IEP_CAPR4_REG0 Register (Offset = 40h) [reset = 0h]

IEP_CAPR4_REG0 is shown in Figure 14-3624 and described in Table 14-7331.

Return to Summary Table.

Capture Rise 4 Low Register.

Table 14-10953. IEP_CAPR4_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E040h
PRU_ICSSG0_IEP1	3002 F040h
PRU_ICSSG1_IEP0	300A E040h
PRU_ICSSG1_IEP1	300A F040h

Figure 14-3624. IEP_CAPR4_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR4_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10955. IEP_CAPR4_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR4_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

18 IEP_CAPR4_REG1 Register (Offset = 44h) [reset = 0h]

IEP_CAPR4_REG1 is shown in Figure 14-3625 and described in Table 14-7333.

Return to Summary Table.

Capture Rise 4 High Register.

Table 14-10956. IEP_CAPR4_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E044h
PRU_ICSSG0_IEP1	3002 F044h
PRU_ICSSG1_IEP0	300A E044h
PRU_ICSSG1_IEP1	300A F044h

Figure 14-3625. IEP_CAPR4_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR4_1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10958. IEP_CAPR4_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR4_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

19 IEP_CAPR5_REG0 Register (Offset = 48h) [reset = 0h]

IEP_CAPR5_REG0 is shown in Figure 14-3626 and described in Table 14-7335.

Return to Summary Table.

Capture Rise 5 Low Register.

Table 14-10959. IEP_CAPR5_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E048h
PRU_ICSSG0_IEP1	3002 F048h
PRU_ICSSG1_IEP0	300A E048h
PRU_ICSSG1_IEP1	300A F048h

Figure 14-3626. IEP_CAPR5_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR5_0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10961. IEP_CAPR5_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR5_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

20 IEP_CAPR5_REG1 Register (Offset = 4Ch) [reset = 0h]

IEP_CAPR5_REG1 is shown in Figure 14-3627 and described in Table 14-7337.

Return to Summary Table.

Capture Rise 5 High Register.

Table 14-10962. IEP_CAPR5_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E04Ch
PRU_ICSSG0_IEP1	3002 F04Ch
PRU_ICSSG1_IEP0	300A E04Ch
PRU_ICSSG1_IEP1	300A F04Ch

Figure 14-3627. IEP_CAPR5_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR5_1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10964. IEP_CAPR5_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR5_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

21 IEP_CAPR6_REG0 Register (Offset = 50h) [reset = 0h]

IEP_CAPR6_REG0 is shown in Figure 14-3628 and described in Table 14-7339.

Return to Summary Table.

Capture Rise 6 Low Register.

Table 14-10965. IEP_CAPR6_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E050h
PRU_ICSSG0_IEP1	3002 F050h
PRU_ICSSG1_IEP0	300A E050h
PRU_ICSSG1_IEP1	300A F050h

Figure 14-3628. IEP_CAPR6_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR6_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10967. IEP_CAPR6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR6_0	R	0h	Value captured for CAPR6 event. Lower 32-bits.

22 IEP_CAPR6_REG1 Register (Offset = 54h) [reset = 0h]

IEP_CAPR6_REG1 is shown in Figure 14-3629 and described in Table 14-7341.

Return to Summary Table.

Capture Rise 6 High Register.

Table 14-10968. IEP_CAPR6_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E054h
PRU_ICSSG0_IEP1	3002 F054h
PRU_ICSSG1_IEP0	300A E054h
PRU_ICSSG1_IEP1	300A F054h

Figure 14-3629. IEP_CAPR6_REG1 Register

31-0
CAPR6_1
R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10970. IEP_CAPR6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR6_1	R	0h	Value captured for CAPR6 event. Upper 32-bits.

23 IEP_CAPF6_REG0 Register (Offset = 58h) [reset = 0h]

IEP_CAPF6_REG0 is shown in Figure 14-3630 and described in Table 14-7343.

Return to Summary Table.

Capture Fall 6 Low Register.

Table 14-10971. IEP_CAPF6_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E058h
PRU_ICSSG0_IEP1	3002 F058h
PRU_ICSSG1_IEP0	300A E058h
PRU_ICSSG1_IEP1	300A F058h

Figure 14-3630. IEP_CAPF6_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPF6_0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-10973. IEP_CAPF6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF6_0	R	0h	Value captured for CAPF6 (fall) event. Lower 32-bits.

24 IEP_CAPF6_REG1 Register (Offset = 5Ch) [reset = 0h]

IEP_CAPF6_REG1 is shown in Figure 14-3631 and described in Table 14-7345.

Return to Summary Table.

Capture Fall 6 High Register.

Table 14-10974. IEP_CAPF6_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E05Ch
PRU_ICSSG0_IEP1	3002 F05Ch
PRU_ICSSG1_IEP0	300A E05Ch
PRU_ICSSG1_IEP1	300A F05Ch

Figure 14-3631. IEP_CAPF6_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPF6_1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10976. IEP_CAPF6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF6_1	R	0h	Value captured for CAPF6 (fall) event. Lower 32-bits.

25 IEP_CAPR7_REG0 Register (Offset = 60h) [reset = 0h]

IEP_CAPR7_REG0 is shown in Figure 14-3632 and described in Table 14-7347.

Return to Summary Table.

Capture Rise 7 Low Register.

Table 14-10977. IEP_CAPR7_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E060h
PRU_ICSSG0_IEP1	3002 F060h
PRU_ICSSG1_IEP0	300A E060h
PRU_ICSSG1_IEP1	300A F060h

Figure 14-3632. IEP_CAPR7_REG0 Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">CAPR7_0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10979. IEP_CAPR7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR7_0	R	0h	Value captured for CAPR7 (rise) event. Lower 32-bits.

26 IEP_CAPR7_REG1 Register (Offset = 64h) [reset = 0h]

IEP_CAPR7_REG1 is shown in Figure 14-3633 and described in Table 14-7349.

Return to Summary Table.

Capture Rise 7 High Register.

Table 14-10980. IEP_CAPR7_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E064h
PRU_ICSSG0_IEP1	3002 F064h
PRU_ICSSG1_IEP0	300A E064h
PRU_ICSSG1_IEP1	300A F064h

Figure 14-3633. IEP_CAPR7_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR7_1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-10982. IEP_CAPR7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR7_1	R	0h	Value captured for CAPR7 (rise) event. Upper 32-bits.

27 IEP_CAPF7_REG0 Register (Offset = 68h) [reset = 0h]

IEP_CAPF7_REG0 is shown in Figure 14-3634 and described in Table 14-7351.

Return to Summary Table.

Capture Fall 7 Low Register.

Table 14-10983. IEP_CAPF7_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E068h
PRU_ICSSG0_IEP1	3002 F068h
PRU_ICSSG1_IEP0	300A E068h
PRU_ICSSG1_IEP1	300A F068h

Figure 14-3634. IEP_CAPF7_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPF7_0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10985. IEP_CAPF7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF7_0	R	0h	Value captured for CAPF7 (fall) event. Lower 32-bits.

28 IEP_CAPF7_REG1 Register (Offset = 6Ch) [reset = 0h]

IEP_CAPF7_REG1 is shown in Figure 14-3635 and described in Table 14-7353.

Return to Summary Table.

Capture Fall 7 High Register.

Table 14-10986. IEP_CAPF7_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E06Ch
PRU_ICSSG0_IEP1	3002 F06Ch
PRU_ICSSG1_IEP0	300A E06Ch
PRU_ICSSG1_IEP1	300A F06Ch

Figure 14-3635. IEP_CAPF7_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF7_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-10988. IEP_CAPF7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF7_1	R	0h	Value captured for CAPF7 (fall) event. Upper 32-bits.

29 IEP_CMP_CFG_REG Register (Offset = 70h) [reset = X]

IEP_CMP_CFG_REG is shown in Figure 14-3636 and described in Table 14-7355.

Return to Summary Table.

Compare Configuration Register.

Table 14-10989. IEP_CMP_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E070h
PRU_ICSSG0_IEP1	3002 F070h
PRU_ICSSG1_IEP0	300A E070h
PRU_ICSSG1_IEP1	300A F070h

Figure 14-3636. IEP_CMP_CFG_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						SHADOW_EN	CMP_EN
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CMP_EN							
R/W-0h							
7	6	5	4	3	2	1	0
CMP_EN							CMP0_RST_CNT_EN
R/W-0h							R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-10991. IEP_CMP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	SHADOW_EN	R/W	0h	
16-1	CMP_EN	R/W	0h	Enable bits for each of the compare registers 0h = Disables CMPj/k Event 1h = Enables CMPj/k Event CMP_EN[0] (bit 1 of register) maps to CMP0 event
0	CMP0_RST_CNT_EN	R/W	0h	Enable the reset of the counter 0h = Disable 1h = Enable the reset of the counter if a CMP0 event occurs

30 IEP_CMP_STATUS_REG Register (Offset = 74h) [reset = X]

IEP_CMP_STATUS_REG is shown in Figure 14-3637 and described in Table 14-7357.

Return to Summary Table.

Compare Status Register.

Table 14-10992. IEP_CMP_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E074h
PRU_ICSSG0_IEP1	3002 F074h
PRU_ICSSG1_IEP0	300A E074h
PRU_ICSSG1_IEP1	300A F074h

Figure 14-3637. IEP_CMP_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMP_STATUS															
R/W-X																R/W1C-0h															

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-10994. IEP_CMP_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	CMP_STATUS	R/W1C	0h	Status bit for each of the compare registers. "Match" indicates the current counter is greater than or equal to the compare value. Note: it is the firmware's responsibility to handle the IEP overflow. 0h = No match has occurred 1h = A match occurred. The associated hardware event signal will assert and remain high until the status is cleared. Shadow Mode Disabled: Any write to a CMP register will cause the corresponding CMP_STATUS bit to get cleared Shadow Mode Enabled: Any write to the active CMP<n>_0 will cause the corresponding CMP_STATUS to get cleared. Any write to the shadow CMP<n>_1 will have no effect on pending state If PWM_EFC_EN is set, hardware will auto clear the bit on next clock cycle.

31 IEP_CMP0_REG0 Register (Offset = 78h) [reset = 0h]

IEP_CMP0_REG0 is shown in Figure 14-3638 and described in Table 14-7359.

Return to Summary Table.

Compare 0 Low Register.

Table 14-10995. IEP_CMP0_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E078h
PRU_ICSSG0_IEP1	3002 F078h
PRU_ICSSG1_IEP0	300A E078h
PRU_ICSSG1_IEP1	300A F078h

Figure 14-3638. IEP_CMP0_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP0_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-10997. IEP_CMP0_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP0_0	R/W	0h	Compare 0 low value

32 IEP_CMP0_REG1 Register (Offset = 7Ch) [reset = 0h]

IEP_CMP0_REG1 is shown in Figure 14-3639 and described in Table 14-7361.

Return to Summary Table.

Compare 0 High Register.

Table 14-10998. IEP_CMP0_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E07Ch
PRU_ICSSG0_IEP1	3002 F07Ch
PRU_ICSSG1_IEP0	300A E07Ch
PRU_ICSSG1_IEP1	300A F07Ch

Figure 14-3639. IEP_CMP0_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP0_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11000. IEP_CMP0_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP0_1	R/W	0h	Compare 0 high value

33 IEP_CMP1_REG0 Register (Offset = 80h) [reset = 0h]

IEP_CMP1_REG0 is shown in Figure 14-3640 and described in Table 14-7363.

Return to Summary Table.

Compare 1 Low Register.

Table 14-11001. IEP_CMP1_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E080h
PRU_ICSSG0_IEP1	3002 F080h
PRU_ICSSG1_IEP0	300A E080h
PRU_ICSSG1_IEP1	300A F080h

Figure 14-3640. IEP_CMP1_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP1_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11003. IEP_CMP1_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP1_0	R/W	0h	Compare 1 low value

34 IEP_CMP1_REG1 Register (Offset = 84h) [reset = 0h]

IEP_CMP1_REG1 is shown in Figure 14-3641 and described in Table 14-7365.

Return to Summary Table.

Compare 1 High Register.

Table 14-11004. IEP_CMP1_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E084h
PRU_ICSSG0_IEP1	3002 F084h
PRU_ICSSG1_IEP0	300A E084h
PRU_ICSSG1_IEP1	300A F084h

Figure 14-3641. IEP_CMP1_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP1_1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11006. IEP_CMP1_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP1_1	R/W	0h	Compare 1 high value

35 IEP_CMP2_REG0 Register (Offset = 88h) [reset = 0h]

IEP_CMP2_REG0 is shown in Figure 14-3642 and described in Table 14-7367.

Return to Summary Table.

Compare 2 Low Register.

Table 14-11007. IEP_CMP2_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E088h
PRU_ICSSG0_IEP1	3002 F088h
PRU_ICSSG1_IEP0	300A E088h
PRU_ICSSG1_IEP1	300A F088h

Figure 14-3642. IEP_CMP2_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP2_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11009. IEP_CMP2_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP2_0	R/W	0h	Compare 2 low value

36 IEP_CMP2_REG1 Register (Offset = 8Ch) [reset = 0h]

IEP_CMP2_REG1 is shown in Figure 14-3643 and described in Table 14-7369.

Return to Summary Table.

Compare 2 High Register.

Table 14-11010. IEP_CMP2_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E08Ch
PRU_ICSSG0_IEP1	3002 F08Ch
PRU_ICSSG1_IEP0	300A E08Ch
PRU_ICSSG1_IEP1	300A F08Ch

Figure 14-3643. IEP_CMP2_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP2_1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11012. IEP_CMP2_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP2_1	R/W	0h	Compare 2 high value

37 IEP_CMP3_REG0 Register (Offset = 90h) [reset = 0h]

IEP_CMP3_REG0 is shown in Figure 14-3644 and described in Table 14-7371.

Return to Summary Table.

Compare 3 Low Register.

Table 14-11013. IEP_CMP3_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E090h
PRU_ICSSG0_IEP1	3002 F090h
PRU_ICSSG1_IEP0	300A E090h
PRU_ICSSG1_IEP1	300A F090h

Figure 14-3644. IEP_CMP3_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP3_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11015. IEP_CMP3_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP3_0	R/W	0h	Compare 3 low value

38 IEP_CMP3_REG1 Register (Offset = 94h) [reset = 0h]

IEP_CMP3_REG1 is shown in Figure 14-3645 and described in Table 14-7373.

Return to Summary Table.

Compare 3 High Register.

Table 14-11016. IEP_CMP3_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E094h
PRU_ICSSG0_IEP1	3002 F094h
PRU_ICSSG1_IEP0	300A E094h
PRU_ICSSG1_IEP1	300A F094h

Figure 14-3645. IEP_CMP3_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP3_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11018. IEP_CMP3_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP3_1	R/W	0h	Compare 3 high value

39 IEP_CMP4_REG0 Register (Offset = 98h) [reset = 0h]

IEP_CMP4_REG0 is shown in Figure 14-3646 and described in Table 14-7375.

Return to Summary Table.

Compare 4 Low Register.

Table 14-11019. IEP_CMP4_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E098h
PRU_ICSSG0_IEP1	3002 F098h
PRU_ICSSG1_IEP0	300A E098h
PRU_ICSSG1_IEP1	300A F098h

Figure 14-3646. IEP_CMP4_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP4_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11021. IEP_CMP4_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP4_0	R/W	0h	Compare 4 low value

40 IEP_CMP4_REG1 Register (Offset = 9Ch) [reset = 0h]

IEP_CMP4_REG1 is shown in Figure 14-3647 and described in Table 14-7377.

Return to Summary Table.

Compare 4 High Register.

Table 14-11022. IEP_CMP4_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E09Ch
PRU_ICSSG0_IEP1	3002 F09Ch
PRU_ICSSG1_IEP0	300A E09Ch
PRU_ICSSG1_IEP1	300A F09Ch

Figure 14-3647. IEP_CMP4_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP4_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11024. IEP_CMP4_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP4_1	R/W	0h	Compare 4 high value

41 IEP_CMP5_REG0 Register (Offset = A0h) [reset = 0h]

IEP_CMP5_REG0 is shown in Figure 14-3648 and described in Table 14-7379.

Return to Summary Table.

Compare 5 Low Register.

Table 14-11025. IEP_CMP5_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0A0h
PRU_ICSSG0_IEP1	3002 F0A0h
PRU_ICSSG1_IEP0	300A E0A0h
PRU_ICSSG1_IEP1	300A F0A0h

Figure 14-3648. IEP_CMP5_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP5_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11027. IEP_CMP5_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP5_0	R/W	0h	Compare 5 low value

42 IEP_CMP5_REG1 Register (Offset = A4h) [reset = 0h]

IEP_CMP5_REG1 is shown in Figure 14-3649 and described in Table 14-7381.

Return to Summary Table.

Compare 5 High Register.

Table 14-11028. IEP_CMP5_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0A4h
PRU_ICSSG0_IEP1	3002 F0A4h
PRU_ICSSG1_IEP0	300A E0A4h
PRU_ICSSG1_IEP1	300A F0A4h

Figure 14-3649. IEP_CMP5_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP5_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11030. IEP_CMP5_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP5_1	R/W	0h	Compare 5 high value

43 IEP_CMP6_REG0 Register (Offset = A8h) [reset = 0h]

IEP_CMP6_REG0 is shown in Figure 14-3650 and described in Table 14-7383.

Return to Summary Table.

Compare 6 Low Register.

Table 14-11031. IEP_CMP6_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0A8h
PRU_ICSSG0_IEP1	3002 F0A8h
PRU_ICSSG1_IEP0	300A E0A8h
PRU_ICSSG1_IEP1	300A F0A8h

Figure 14-3650. IEP_CMP6_REG0 Register

31-0
CMP6_0
R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11033. IEP_CMP6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP6_0	R/W	0h	Compare 6 low value

44 IEP_CMP6_REG1 Register (Offset = ACh) [reset = 0h]

IEP_CMP6_REG1 is shown in Figure 14-3651 and described in Table 14-7385.

Return to Summary Table.

Compare 6 High Register.

Table 14-11034. IEP_CMP6_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0ACh
PRU_ICSSG0_IEP1	3002 F0ACh
PRU_ICSSG1_IEP0	300A E0ACh
PRU_ICSSG1_IEP1	300A F0ACh

Figure 14-3651. IEP_CMP6_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP6_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11036. IEP_CMP6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP6_1	R/W	0h	Compare 6 high value

45 IEP_CMP7_REG0 Register (Offset = B0h) [reset = 0h]

IEP_CMP7_REG0 is shown in Figure 14-3652 and described in Table 14-7387.

Return to Summary Table.

Compare 7 Low Register.

Table 14-11037. IEP_CMP7_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0B0h
PRU_ICSSG0_IEP1	3002 F0B0h
PRU_ICSSG1_IEP0	300A E0B0h
PRU_ICSSG1_IEP1	300A F0B0h

Figure 14-3652. IEP_CMP7_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP7_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11039. IEP_CMP7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP7_0	R/W	0h	Compare 7 low value

46 IEP_CMP7_REG1 Register (Offset = B4h) [reset = 0h]

IEP_CMP7_REG1 is shown in Figure 14-3653 and described in Table 14-7389.

Return to Summary Table.

Compare 7 High Register.

Table 14-11040. IEP_CMP7_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0B4h
PRU_ICSSG0_IEP1	3002 F0B4h
PRU_ICSSG1_IEP0	300A E0B4h
PRU_ICSSG1_IEP1	300A F0B4h

Figure 14-3653. IEP_CMP7_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP7_1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11042. IEP_CMP7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP7_1	R/W	0h	Compare 7 high value

47 IEP_RXIPG0_REG Register (Offset = B8h) [reset = FFFF0000h]

IEP_RXIPG0_REG is shown in Figure 14-3654 and described in Table 14-7391.

Return to Summary Table.

Status for the RX port which is attached to PRU0 Register.

Table 14-11043. IEP_RXIPG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0B8h
PRU_ICSSG0_IEP1	3002 F0B8h
PRU_ICSSG1_IEP0	300A E0B8h
PRU_ICSSG1_IEP1	300A F0B8h

Figure 14-3654. IEP_RXIPG0_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RX_MIN_IPG0</td><td colspan="16">RX_IPG0</td></tr>
<tr><td colspan="16">R/W-FFFFh</td><td colspan="16">R-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11045. IEP_RXIPG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MIN_IPG0	R/W	FFFFh	Defines the minimum number of ICSS_IEP_CLK/ICCS_VCLK_CLK cycles that is RX_DV is sampled low. It stores the smallest RX_IPG duration. It can be read at any time and gets updated after RX_IPG is updated, if RX_MIN_IPG is greater than RX_IPG.
15-0	RX_IPG0	R	0h	Records the current number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles RX_DV is sampled low. Value is updated after RX_DV transitions from low to high. It will saturate at FFFFh.

48 IEP_RXIPG1_REG Register (Offset = BCh) [reset = FFFF0000h]

IEP_RXIPG1_REG is shown in Figure 14-3655 and described in Table 14-7393.

Return to Summary Table.

Status for the RX port which is attached to PRU1 Register.

Table 14-11046. IEP_RXIPG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0BCh
PRU_ICSSG0_IEP1	3002 F0BCh
PRU_ICSSG1_IEP0	300A E0BCh
PRU_ICSSG1_IEP1	300A F0BCh

Figure 14-3655. IEP_RXIPG1_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RX_MIN_IPG1</td><td colspan="16">RX_IPG1</td></tr>
<tr><td colspan="16">R/W-FFFFh</td><td colspan="16">R-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11048. IEP_RXIPG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MIN_IPG1	R/W	FFFFh	Defines the minimum number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles that is RX_DV is sampled low. It stores the smallest RX_IPG duration. It can be read at any time and gets updated after RX_IPG is updated, if RX_MIN_IPG is greater than RX_IPG.
15-0	RX_IPG1	R	0h	Records the current number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles RX_DV is sampled low. Value is updated after RX_DV transitions from low to high. It will saturate at FFFFh.

49 IEP_CMP8_REG0 Register (Offset = C0h) [reset = 0h]

IEP_CMP8_REG0 is shown in Figure 14-3656 and described in Table 14-7395.

Return to Summary Table.

Compare 8 Low Register.

Table 14-11049. IEP_CMP8_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0C0h
PRU_ICSSG0_IEP1	3002 F0C0h
PRU_ICSSG1_IEP0	300A E0C0h
PRU_ICSSG1_IEP1	300A F0C0h

Figure 14-3656. IEP_CMP8_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP8_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11051. IEP_CMP8_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP8_0	R/W	0h	Compare 8 low value

50 IEP_CMP8_REG1 Register (Offset = C4h) [reset = 0h]

IEP_CMP8_REG1 is shown in Figure 14-3657 and described in Table 14-7397.

Return to Summary Table.

Compare 8 High Register.

Table 14-11052. IEP_CMP8_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0C4h
PRU_ICSSG0_IEP1	3002 F0C4h
PRU_ICSSG1_IEP0	300A E0C4h
PRU_ICSSG1_IEP1	300A F0C4h

Figure 14-3657. IEP_CMP8_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP8_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11054. IEP_CMP8_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP8_1	R/W	0h	Compare 8 high value

51 IEP_CMP9_REG0 Register (Offset = C8h) [reset = 0h]

IEP_CMP9_REG0 is shown in Figure 14-3658 and described in Table 14-7399.

Return to Summary Table.

Compare 9 Low Register.

Table 14-11055. IEP_CMP9_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0C8h
PRU_ICSSG0_IEP1	3002 F0C8h
PRU_ICSSG1_IEP0	300A E0C8h
PRU_ICSSG1_IEP1	300A F0C8h

Figure 14-3658. IEP_CMP9_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP9_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11057. IEP_CMP9_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP9_0	R/W	0h	Compare 9 low value

52 IEP_CMP9_REG1 Register (Offset = CCh) [reset = 0h]

IEP_CMP9_REG1 is shown in Figure 14-3659 and described in Table 14-7401.

Return to Summary Table.

Compare 9 High Register.

Table 14-11058. IEP_CMP9_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0CCh
PRU_ICSSG0_IEP1	3002 F0CCh
PRU_ICSSG1_IEP0	300A E0CCh
PRU_ICSSG1_IEP1	300A F0CCh

Figure 14-3659. IEP_CMP9_REG1 Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">CMP9_1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11060. IEP_CMP9_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP9_1	R/W	0h	Compare 9 high value

53 IEP_CMP10_REG0 Register (Offset = D0h) [reset = 0h]

IEP_CMP10_REG0 is shown in Figure 14-3660 and described in Table 14-7403.

Return to Summary Table.

Compare 10 Low Register.

Table 14-11061. IEP_CMP10_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0D0h
PRU_ICSSG0_IEP1	3002 F0D0h
PRU_ICSSG1_IEP0	300A E0D0h
PRU_ICSSG1_IEP1	300A F0D0h

Figure 14-3660. IEP_CMP10_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP10_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11063. IEP_CMP10_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP10_0	R/W	0h	Compare 10 low value

54 IEP_CMP10_REG1 Register (Offset = D4h) [reset = 0h]

IEP_CMP10_REG1 is shown in Figure 14-3661 and described in Table 14-7405.

Return to Summary Table.

Compare 10 High Register.

Table 14-11064. IEP_CMP10_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0D4h
PRU_ICSSG0_IEP1	3002 F0D4h
PRU_ICSSG1_IEP0	300A E0D4h
PRU_ICSSG1_IEP1	300A F0D4h

Figure 14-3661. IEP_CMP10_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP10_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11066. IEP_CMP10_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP10_1	R/W	0h	Compare 10 high value

55 IEP_CMP11_REG0 Register (Offset = D8h) [reset = 0h]

IEP_CMP11_REG0 is shown in Figure 14-3662 and described in Table 14-7407.

Return to Summary Table.

Compare 11 Low Register.

Table 14-11067. IEP_CMP11_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0D8h
PRU_ICSSG0_IEP1	3002 F0D8h
PRU_ICSSG1_IEP0	300A E0D8h
PRU_ICSSG1_IEP1	300A F0D8h

Figure 14-3662. IEP_CMP11_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP11_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11069. IEP_CMP11_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP11_0	R/W	0h	Compare 11 low value

56 IEP_CMP11_REG1 Register (Offset = DCh) [reset = 0h]

IEP_CMP11_REG1 is shown in Figure 14-3663 and described in Table 14-7409.

Return to Summary Table.

Compare 11 High Register.

Table 14-11070. IEP_CMP11_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0DCh
PRU_ICSSG0_IEP1	3002 F0DCh
PRU_ICSSG1_IEP0	300A E0DCh
PRU_ICSSG1_IEP1	300A F0DCh

Figure 14-3663. IEP_CMP11_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP11_1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11072. IEP_CMP11_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP11_1	R/W	0h	Compare 11 high value

57 IEP_CMP12_REG0 Register (Offset = E0h) [reset = 0h]

IEP_CMP12_REG0 is shown in Figure 14-3664 and described in Table 14-7411.

Return to Summary Table.

Compare 12 Low Register.

Table 14-11073. IEP_CMP12_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0E0h
PRU_ICSSG0_IEP1	3002 F0E0h
PRU_ICSSG1_IEP0	300A E0E0h
PRU_ICSSG1_IEP1	300A F0E0h

Figure 14-3664. IEP_CMP12_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP12_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11075. IEP_CMP12_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP12_0	R/W	0h	Compare 12 low value

58 IEP_CMP12_REG1 Register (Offset = E4h) [reset = 0h]

IEP_CMP12_REG1 is shown in Figure 14-3665 and described in Table 14-7413.

Return to Summary Table.

Compare 12 High Register.

Table 14-11076. IEP_CMP12_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0E4h
PRU_ICSSG0_IEP1	3002 F0E4h
PRU_ICSSG1_IEP0	300A E0E4h
PRU_ICSSG1_IEP1	300A F0E4h

Figure 14-3665. IEP_CMP12_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP12_1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11078. IEP_CMP12_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP12_1	R/W	0h	Compare 12 high value

59 IEP_CMP13_REG0 Register (Offset = E8h) [reset = 0h]

IEP_CMP13_REG0 is shown in Figure 14-3666 and described in Table 14-7415.

Return to Summary Table.

Compare 13 Low Register.

Table 14-11079. IEP_CMP13_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0E8h
PRU_ICSSG0_IEP1	3002 F0E8h
PRU_ICSSG1_IEP0	300A E0E8h
PRU_ICSSG1_IEP1	300A F0E8h

Figure 14-3666. IEP_CMP13_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP13_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11081. IEP_CMP13_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP13_0	R/W	0h	Compare 13 low value

60 IEP_CMP13_REG1 Register (Offset = ECh) [reset = 0h]

IEP_CMP13_REG1 is shown in Figure 14-3667 and described in Table 14-7417.

Return to Summary Table.

Compare 13 High Register.

Table 14-11082. IEP_CMP13_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0ECh
PRU_ICSSG0_IEP1	3002 F0ECh
PRU_ICSSG1_IEP0	300A E0ECh
PRU_ICSSG1_IEP1	300A F0ECh

Figure 14-3667. IEP_CMP13_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP13_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11084. IEP_CMP13_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP13_1	R/W	0h	Compare 13 high value

61 IEP_CMP14_REG0 Register (Offset = F0h) [reset = 0h]

IEP_CMP14_REG0 is shown in Figure 14-3668 and described in Table 14-7419.

Return to Summary Table.

Compare 14 Low Register.

Table 14-11085. IEP_CMP14_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0F0h
PRU_ICSSG0_IEP1	3002 F0F0h
PRU_ICSSG1_IEP0	300A E0F0h
PRU_ICSSG1_IEP1	300A F0F0h

Figure 14-3668. IEP_CMP14_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP14_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11087. IEP_CMP14_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP14_0	R/W	0h	Compare 14 low value

62 IEP_CMP14_REG1 Register (Offset = F4h) [reset = 0h]

IEP_CMP14_REG1 is shown in Figure 14-3669 and described in Table 14-7421.

Return to Summary Table.

Compare 14 High Register.

Table 14-11088. IEP_CMP14_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0F4h
PRU_ICSSG0_IEP1	3002 F0F4h
PRU_ICSSG1_IEP0	300A E0F4h
PRU_ICSSG1_IEP1	300A F0F4h

Figure 14-3669. IEP_CMP14_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP14_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11090. IEP_CMP14_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP14_1	R/W	0h	Compare 14 high value

63 IEP_CMP15_REG0 Register (Offset = F8h) [reset = 0h]

IEP_CMP15_REG0 is shown in Figure 14-3670 and described in Table 14-7423.

Return to Summary Table.

Compare 15 Low Register.

Table 14-11091. IEP_CMP15_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0F8h
PRU_ICSSG0_IEP1	3002 F0F8h
PRU_ICSSG1_IEP0	300A E0F8h
PRU_ICSSG1_IEP1	300A F0F8h

Figure 14-3670. IEP_CMP15_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP15_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11093. IEP_CMP15_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP15_0	R/W	0h	Compare 15 low value

64 IEP_CMP15_REG1 Register (Offset = FCh) [reset = 0h]

IEP_CMP15_REG1 is shown in Figure 14-3671 and described in Table 14-7425.

Return to Summary Table.

Compare 15 High Register.

Table 14-11094. IEP_CMP15_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E0FCh
PRU_ICSSG0_IEP1	3002 F0FCh
PRU_ICSSG1_IEP0	300A E0FCh
PRU_ICSSG1_IEP1	300A F0FCh

Figure 14-3671. IEP_CMP15_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CMP15_1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11096. IEP_CMP15_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP15_1	R/W	0h	Compare 15 high value

65 IEP_COUNT_RESET_VAL_REG0 Register (Offset = 100h) [reset = 0h]

IEP_COUNT_RESET_VAL_REG0 is shown in Figure 14-3672 and described in Table 14-7427.

Return to Summary Table.

Reset value of the Controller Counter (lower 32-bits) Register.

Table 14-11097. IEP_COUNT_RESET_VAL_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E100h
PRU_ICSSG0_IEP1	3002 F100h
PRU_ICSSG1_IEP0	300A E100h
PRU_ICSSG1_IEP1	300A F100h

Figure 14-3672. IEP_COUNT_RESET_VAL_REG0 Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">RESET_VAL_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11099. IEP_COUNT_RESET_VAL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESET_VAL_0	R/W	0h	Reset value (lower 32-bits). This register enables SW to define the reset state of the Controller Counter, which can be reset by the following events (if enabled): CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. The RESET_VAL should be in increments of the DEFAULT_INC (default state is 5). For example, 0000_000Ah.

66 IEP_COUNT_RESET_VAL_REG1 Register (Offset = 104h) [reset = 0h]

IEP_COUNT_RESET_VAL_REG1 is shown in Figure 14-3673 and described in Table 14-7429.

Return to Summary Table.

Reset value of the Controller Counter (upper 32-bits) Register.

Table 14-11100. IEP_COUNT_RESET_VAL_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E104h
PRU_ICSSG0_IEP1	3002 F104h
PRU_ICSSG1_IEP0	300A E104h
PRU_ICSSG1_IEP1	300A F104h

Figure 14-3673. IEP_COUNT_RESET_VAL_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">RESET_VAL_1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11102. IEP_COUNT_RESET_VAL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESET_VAL_1	R/W	0h	This enables SW to define the reset state of the Controller counter when it gets reset do to the following 3 possible events if enabled: CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. It should be in increments of the DEFAULT_INC, default state is 5 For example, 0000_000Ah

67 IEP_PWM_REG Register (Offset = 108h) [reset = X]

IEP_PWM_REG is shown in Figure 14-3674 and described in Table 14-7431.

Return to Summary Table.

PWM Sync Out Register.

Table 14-11103. IEP_PWM_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E108h
PRU_ICSSG0_IEP1	3002 F108h
PRU_ICSSG1_IEP0	300A E108h
PRU_ICSSG1_IEP1	300A F108h

Figure 14-3674. IEP_PWM_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PWM3_HIT	PWM3_RST_CNT_EN	PWM0_HIT	PWM0_RST_CNT_EN
R/W-X				R/W1C-0h	R/W-0h	R/W1C-0h	R/W-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-11105. IEP_PWM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	PWM3_HIT	R/W1C	0h	The raw status bit of eHRPWM3_SYNCO event. 0h = No eHRPWM3_SYNCO event 1h = eHRPWM3_SYNCO event occurred Write 1 to Clear.
2	PWM3_RST_CNT_EN	R/W	0h	Enable the reset of the counter by a eHRPWM3_SYNCO event. 0h = Disable 1h = Enable the reset of the counter if a eHRPWM3_SYNCO event occurs
1	PWM0_HIT	R/W1C	0h	The raw status bit of eHRPWM0_SYNCO event. 0h = No eHRPWM0_SYNCO event 1h = eHRPWM0_SYNCO event occurred Write 1 to Clear.

Table 14-11105. IEP_PWM_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PWM0_RST_CNT_EN	R/W	0h	Enable the reset of the counter by a eHRPWM0_SYNCO event. 0h = Disable 1h = Enable the reset of the counter if a eHRPWM0_SYNCO event occurs

68 IEP_CAPR0_BI_REG0 Register (Offset = 10Ch) [reset = 0h]

IEP_CAPR0_BI_REG0 is shown in Figure 14-3675 and described in Table 14-7433.

Return to Summary Table.

Capture Big Endian Rise00 Register.

Table 14-11106. IEP_CAPR0_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E10Ch
PRU_ICSSG0_IEP1	3002 F10Ch
PRU_ICSSG1_IEP0	300A E10Ch
PRU_ICSSG1_IEP1	300A F10Ch

Figure 14-3675. IEP_CAPR0_BI_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR0_0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11108. IEP_CAPR0_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR0_0	R	0h	Capture Value for CAPR0 event. Big Endian Format The bytes are the same order. Within the byte, the bits are flipped.

69 IEP_CAPR0_BI_REG1 Register (Offset = 110h) [reset = 0h]

IEP_CAPR0_BI_REG1 is shown in Figure 14-3676 and described in Table 14-7435.

Return to Summary Table.

Capture Big Endian Rise10 Register.

Table 14-11109. IEP_CAPR0_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E110h
PRU_ICSSG0_IEP1	3002 F110h
PRU_ICSSG1_IEP0	300A E110h
PRU_ICSSG1_IEP1	300A F110h

Figure 14-3676. IEP_CAPR0_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR0_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11111. IEP_CAPR0_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR0_1	R	0h	Capture Value for CAPR0 event. Big Endian Format The bytes are the same order. Within the byte, the bits are flipped.

70 IEP_CAPR1_BI_REG0 Register (Offset = 114h) [reset = 0h]

IEP_CAPR1_BI_REG0 is shown in Figure 14-3677 and described in Table 14-7437.

Return to Summary Table.

Capture Big Endian Rise01 Register.

Table 14-11112. IEP_CAPR1_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E114h
PRU_ICSSG0_IEP1	3002 F114h
PRU_ICSSG1_IEP0	300A E114h
PRU_ICSSG1_IEP1	300A F114h

Figure 14-3677. IEP_CAPR1_BI_REG0 Register

31–0
CAPR1_0
R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11114. IEP_CAPR1_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR1_0	R	0h	Capture Value for CAPR1 event. The bytes are the same order. Within the byte, the bits are flipped.

71 IEP_CAPR1_BI_REG1 Register (Offset = 118h) [reset = 0h]

IEP_CAPR1_BI_REG1 is shown in Figure 14-3678 and described in Table 14-7439.

Return to Summary Table.

Capture Big Endian Rise11 Register

Table 14-11115. IEP_CAPR1_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E118h
PRU_ICSSG0_IEP1	3002 F118h
PRU_ICSSG1_IEP0	300A E118h
PRU_ICSSG1_IEP1	300A F118h

Figure 14-3678. IEP_CAPR1_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR1_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11117. IEP_CAPR1_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR1_1	R	0h	Capture Value for CAPR1 event. The bytes are the same order. Within the byte, the bits are flipped.

72 IEP_CAPR2_BI_REG0 Register (Offset = 11Ch) [reset = 0h]

IEP_CAPR2_BI_REG0 is shown in Figure 14-3679 and described in Table 14-7441.

Return to Summary Table.

Capture Big Endian Rise02 Register.

Table 14-11118. IEP_CAPR2_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E11Ch
PRU_ICSSG0_IEP1	3002 F11Ch
PRU_ICSSG1_IEP0	300A E11Ch
PRU_ICSSG1_IEP1	300A F11Ch

Figure 14-3679. IEP_CAPR2_BI_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR2_0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11120. IEP_CAPR2_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR2_0	R	0h	Capture Value for CAPR2 event. The bytes are the same order. Within the byte, the bits are flipped.

73 IEP_CAPR2_BI_REG1 Register (Offset = 120h) [reset = 0h]

IEP_CAPR2_BI_REG1 is shown in Figure 14-3680 and described in Table 14-7443.

Return to Summary Table.

Capture Big Endian Rise12 Register.

Table 14-11121. IEP_CAPR2_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E120h
PRU_ICSSG0_IEP1	3002 F120h
PRU_ICSSG1_IEP0	300A E120h
PRU_ICSSG1_IEP1	300A F120h

Figure 14-3680. IEP_CAPR2_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR2_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11123. IEP_CAPR2_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR2_1	R	0h	Capture Value for CAPR2 event. The bytes are the same order. Within the byte, the bits are flipped.

74 IEP_CAPR3_BI_REG0 Register (Offset = 124h) [reset = 0h]

IEP_CAPR3_BI_REG0 is shown in Figure 14-3681 and described in Table 14-7445.

Return to Summary Table.

Capture Big Endian Rise03 Register.

Table 14-11124. IEP_CAPR3_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E124h
PRU_ICSSG0_IEP1	3002 F124h
PRU_ICSSG1_IEP0	300A E124h
PRU_ICSSG1_IEP1	300A F124h

Figure 14-3681. IEP_CAPR3_BI_REG0 Register

31 … 0
CAPR3_0
R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11126. IEP_CAPR3_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR3_0	R	0h	Capture Value for CAPR3 event. The bytes are the same order. Within the byte, the bits are flipped.

75 IEP_CAPR3_BI_REG1 Register (Offset = 128h) [reset = 0h]

IEP_CAPR3_BI_REG1 is shown in Figure 14-3682 and described in Table 14-7447.

Return to Summary Table.

Capture Big Endian Rise13 Register.

Table 14-11127. IEP_CAPR3_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E128h
PRU_ICSSG0_IEP1	3002 F128h
PRU_ICSSG1_IEP0	300A E128h
PRU_ICSSG1_IEP1	300A F128h

Figure 14-3682. IEP_CAPR3_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR3_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11129. IEP_CAPR3_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR3_1	R	0h	Capture Value for CAPR3 event. The bytes are the same order. Within the byte, the bits are flipped.

76 IEP_CAPR4_BI_REG0 Register (Offset = 12Ch) [reset = 0h]

IEP_CAPR4_BI_REG0 is shown in Figure 14-3683 and described in Table 14-7449.

Return to Summary Table.

Capture Big Endian Rise04 Register.

Table 14-11130. IEP_CAPR4_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E12ch
PRU_ICSSG0_IEP1	3002 F12ch
PRU_ICSSG1_IEP0	300A E12ch
PRU_ICSSG1_IEP1	300A F12ch

Figure 14-3683. IEP_CAPR4_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR4_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11132. IEP_CAPR4_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR4_0	R	0h	Capture Value for CAPR4 event. The bytes are the same order. Within the byte, the bits are flipped.

77 IEP_CAPR4_BI_REG1 Register (Offset = 130h) [reset = 0h]

IEP_CAPR4_BI_REG1 is shown in Figure 14-3684 and described in Table 14-7451.

Return to Summary Table.

Capture Big Endian Rise14 Register.

Table 14-11133. IEP_CAPR4_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E130h
PRU_ICSSG0_IEP1	3002 F130h
PRU_ICSSG1_IEP0	300A E130h
PRU_ICSSG1_IEP1	300A F130h

Figure 14-3684. IEP_CAPR4_BI_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR4_1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11135. IEP_CAPR4_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR4_1	R	0h	Capture Value for CAPR4 event. The bytes are the same order. Within the byte, the bits are flipped.

78 IEP_CAPR5_BI_REG0 Register (Offset = 134h) [reset = 0h]

IEP_CAPR5_BI_REG0 is shown in Figure 14-3685 and described in Table 14-7453.

Return to Summary Table.

Capture Big Endian Rise05 Register.

Table 14-11136. IEP_CAPR5_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E134h
PRU_ICSSG0_IEP1	3002 F134h
PRU_ICSSG1_IEP0	300A E134h
PRU_ICSSG1_IEP1	300A F134h

Figure 14-3685. IEP_CAPR5_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR5_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11138. IEP_CAPR5_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR5_0	R	0h	Capture Value for CAPR5 event. The bytes are the same order. Within the byte, the bits are flipped.

79 IEP_CAPR5_BI_REG1 Register (Offset = 138h) [reset = 0h]

IEP_CAPR5_BI_REG1 is shown in Figure 14-3686 and described in Table 14-7455.

Return to Summary Table.

Capture Big Endian Rise15 Register.

Table 14-11139. IEP_CAPR5_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E138h
PRU_ICSSG0_IEP1	3002 F138h
PRU_ICSSG1_IEP0	300A E138h
PRU_ICSSG1_IEP1	300A F138h

Figure 14-3686. IEP_CAPR5_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR5_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11141. IEP_CAPR5_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR5_1	R	0h	Capture Value for CAPR5 event. The bytes are the same order. Within the byte, the bits are flipped.

80 IEP_CAPR6_BI_REG0 Register (Offset = 13Ch) [reset = 0h]

IEP_CAPR6_BI_REG0 is shown in Figure 14-3687 and described in Table 14-7457.

Return to Summary Table.

Capture Big Endian Rise06 Register.

Table 14-11142. IEP_CAPR6_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E13Ch
PRU_ICSSG0_IEP1	3002 F13Ch
PRU_ICSSG1_IEP0	300A E13Ch
PRU_ICSSG1_IEP1	300A F13Ch

Figure 14-3687. IEP_CAPR6_BI_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPR6_0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11144. IEP_CAPR6_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR6_0	R	0h	Capture Value for CAPR6 event. The bytes are the same order. Within the byte, the bits are flipped.

81 IEP_CAPR6_BI_REG1 Register (Offset = 140h) [reset = 0h]

IEP_CAPR6_BI_REG1 is shown in Figure 14-3688 and described in Table 14-7459.

Return to Summary Table.

Capture Big Endian Rise16 Register.

Table 14-11145. IEP_CAPR6_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E140h
PRU_ICSSG0_IEP1	3002 F140h
PRU_ICSSG1_IEP0	300A E140h
PRU_ICSSG1_IEP1	300A F140h

Figure 14-3688. IEP_CAPR6_BI_REG1 Register

31–0
CAPR6_1
R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11147. IEP_CAPR6_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR6_1	R	0h	Capture Value for CAPR6 event. The bytes are the same order. Within the byte, the bits are flipped.

82 IEP_CAPF6_BI_REG0 Register (Offset = 144h) [reset = 0h]

IEP_CAPF6_BI_REG0 is shown in Figure 14-3689 and described in Table 14-7461.

Return to Summary Table.

Capture Big Endian Fall06 Register.

Table 14-11148. IEP_CAPF6_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E144h
PRU_ICSSG0_IEP1	3002 F144h
PRU_ICSSG1_IEP0	300A E144h
PRU_ICSSG1_IEP1	300A F144h

Figure 14-3689. IEP_CAPF6_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF6_0																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11150. IEP_CAPF6_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF6_0	R	0h	Capture Value for CAPF6 event. The bytes are the same order. Within the byte, the bits are flipped.

83 IEP_CAPF6_BI_REG1 Register (Offset = 148h) [reset = 0h]

IEP_CAPF6_BI_REG1 is shown in Figure 14-3690 and described in Table 14-7463.

Return to Summary Table.

Capture Big Endian Fall16 Register.

Table 14-11151. IEP_CAPF6_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E148h
PRU_ICSSG0_IEP1	3002 F148h
PRU_ICSSG1_IEP0	300A E148h
PRU_ICSSG1_IEP1	300A F148h

Figure 14-3690. IEP_CAPF6_BI_REG1 Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">CAPF6_1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11153. IEP_CAPF6_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF6_1	R	0h	Capture Value for CAPF6 event.

84 IEP_CAPR7_BI_REG0 Register (Offset = 14Ch) [reset = 0h]

IEP_CAPR7_BI_REG0 is shown in Figure 14-3691 and described in Table 14-7465.

Return to Summary Table.

Capture Big Endian Rise07 Register.

Table 14-11154. IEP_CAPR7_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E14Ch
PRU_ICSSG0_IEP1	3002 F14Ch
PRU_ICSSG1_IEP0	300A E14Ch
PRU_ICSSG1_IEP1	300A F14Ch

Figure 14-3691. IEP_CAPR7_BI_REG0 Register

31-0
CAPR7_0
R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11156. IEP_CAPR7_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR7_0	R	0h	Capture Value for CAPR7 event. The bytes are the same order. Within the byte, the bits are flipped.

85 IEP_CAPR7_BI_REG1 Register (Offset = 150h) [reset = 0h]

IEP_CAPR7_BI_REG1 is shown in Figure 14-3692 and described in Table 14-7467.

Return to Summary Table.

Capture Big Endian Rise17 Register.

Table 14-11157. IEP_CAPR7_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E150h
PRU_ICSSG0_IEP1	3002 F150h
PRU_ICSSG1_IEP0	300A E150h
PRU_ICSSG1_IEP1	300A F150h

Figure 14-3692. IEP_CAPR7_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR7_1																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11159. IEP_CAPR7_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR7_1	R	0h	Capture Value for CAPR7 event. The bytes are the same order. Within the byte, the bits are flipped.

86 IEP_CAPF7_BI_REG0 Register (Offset = 154h) [reset = 0h]

IEP_CAPF7_BI_REG0 is shown in Figure 14-3693 and described in Table 14-7469.

Return to Summary Table.

Capture Big Endian Fall07 Register.

Table 14-11160. IEP_CAPF7_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E154h
PRU_ICSSG0_IEP1	3002 F154h
PRU_ICSSG1_IEP0	300A E154h
PRU_ICSSG1_IEP1	300A F154h

Figure 14-3693. IEP_CAPF7_BI_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPF7_0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11162. IEP_CAPF7_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF7_0	R	0h	Capture Value for CAPF7 event. The bytes are the same order. Within the byte, the bits are flipped.

87 IEP_CAPF7_BI_REG1 Register (Offset = 158h) [reset = 0h]

IEP_CAPF7_BI_REG1 is shown in Figure 14-3694 and described in Table 14-7471.

Return to Summary Table.

Capture Big Endian Fall17 Register.

Table 14-11163. IEP_CAPF7_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E158h
PRU_ICSSG0_IEP1	3002 F158h
PRU_ICSSG1_IEP0	300A E158h
PRU_ICSSG1_IEP1	300A F158h

Figure 14-3694. IEP_CAPF7_BI_REG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPF7_1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11165. IEP_CAPF7_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF7_1	R	0h	Capture Value for CAPF7 event. The bytes are the same order. Within the byte, the bits are flipped.

88 IEP_SYNC_CTRL_REG Register (Offset = 180h) [reset = X]

IEP_SYNC_CTRL_REG is shown in Figure 14-3695 and described in Table 14-7473.

Return to Summary Table.

Sync Generation Control Register.

Table 14-11166. IEP_SYNC_CTRL_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E180h
PRU_ICSSG0_IEP1	3002 F180h
PRU_ICSSG1_IEP0	300A E180h
PRU_ICSSG1_IEP1	300A F180h

Figure 14-3695. IEP_SYNC_CTRL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED					SYNC1_OUT_NV_EN	SYNC0_OUT_NV_EN	SYNC1_IND_EN
R/W-X					R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
SYNC1_CYCLIC_EN	SYNC1_ACK_EN	SYNC0_CYCLIC_EN	SYNC0_ACK_EN	RESERVED	SYNC1_EN	SYNC0_EN	SYNC_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11168. IEP_SYNC_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10	SYNC1_OUT_NV_EN	R/W	0h	0 = sync1_out is not inverted 1 = sync1_out is inverted Only effects the output
9	SYNC0_OUT_NV_EN	R/W	0h	0 = sync0_out is not inverted 1 = sync0_out is inverted Only effects the output
8	SYNC1_IND_EN	R/W	0h	SYNC1 independent mode enable. Independent mode means the SYNC1 signal can be different from SYNC0. 0h = Dependent mode. SYNC1 is dependent on SYNC0 1h = Independent mode
7	SYNC1_CYCLIC_EN	R/W	0h	SYNC1 single shot or cyclic/auto generation mode enable 0h = Disable, single shot mode 1h = Enable, cyclic generation mode

Table 14-11168. IEP_SYNC_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SYNC1_ACK_EN	R/W	0h	SYNC1 acknowledgement mode enable 0h = Disable, SYNC1 will go low after pulse width is met. 1h = Enable, SYNC1 will remain asserted until receiving software acknowledges by writing"1" IEP_SYNC1_STAT_REG which clears on write.
5	SYNC0_CYCLIC_EN	R/W	0h	SYNC0 single shot or cyclic/auto generation mode enable 0h = Disable, single shot mode 1h = Enable, cyclic generation mode
4	SYNC0_ACK_EN	R/W	0h	SYNC0 acknowledgement mode enable 0h = Disable, SYNC0 will go low after pulse width is met. 1h = Enable, SYNC0 will remain asserted until receiving software acknowledges by writing "1" IEP_SYNC0_STAT_REG which clears on write.
3	RESERVED	R/W	X	
2	SYNC1_EN	R/W	0h	SYNC1 generation enable 0h = Disable SYNC1 generation. If SYNC1 is low, it will stop immediately. If SYNC1 is high, it will stop after SYNC1 goes low 1h = Enable SYNC1 generation
1	SYNC0_EN	R/W	0h	SYNC0 generation enable 0h = Disable SYNC0 generation. If SYNC0 is low, it will stop immediately If SYNC0 is high, it will stop after SYNC0 goes low 1h = Enable SYNC0 generation
0	SYNC_EN	R/W	0h	SYNC generation enable 0h = Disable the generation and clocking of SYNC0 and SYNC1 logic. If SYNC0 AND SYNC1 is low, it will stop immediately. If SYNC0 OR SYNC1 is high, it will stop after SYCN0 AND SYNC1 goes low. Note: that you might get 1 extra high pulse if this is disabled during a high pulse of one and the 2nd pulse goes high before the last pulse low if you do not de-assert sync0_en and sync1_en at the same time. SW should always de-assert both sync1_en and sync0_en at the same time as sync_en is de-asserted 1h = Enables SYNC0 and SYNC1 generation

89 IEP_SYNC_FIRST_STAT_REG Register (Offset = 184h) [reset = X]

IEP_SYNC_FIRST_STAT_REG is shown in Figure 14-3696 and described in Table 14-7475.

Return to Summary Table.

Sync Generation First Event Status Register.

Table 14-11169. IEP_SYNC_FIRST_STAT_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E184h
PRU_ICSSG0_IEP1	3002 F184h
PRU_ICSSG1_IEP0	300A E184h
PRU_ICSSG1_IEP1	300A F184h

Figure 14-3696. IEP_SYNC_FIRST_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						FIRST_SYNC1	FIRST_SYNC0
R-X						R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11171. IEP_SYNC_FIRST_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	FIRST_SYNC1	R	0h	SYNC1 First Event status 0h = SYNC1 first event has NOT occurred 1h = SYNC1 first event has occurred. This bits is cleared when sync1_en = 0
0	FIRST_SYNC0	R	0h	SYNC0 First Event status 0h = SYNC0 first event has not occurred 1h = SYNC0 first event has occurred. This bits is cleared when sync0_en = 0

90 IEP_SYNC0_STAT_REG Register (Offset = 188h) [reset = X]

IEP_SYNC0_STAT_REG is shown in Figure 14-3697 and described in Table 14-7477.

Return to Summary Table.

Sync 0 Status Register.

Table 14-11172. IEP_SYNC0_STAT_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E188h
PRU_ICSSG0_IEP1	3002 F188h
PRU_ICSSG1_IEP0	300A E188h
PRU_ICSSG1_IEP1	300A F188h

Figure 14-3697. IEP_SYNC0_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SYNC0_PEND
R-X							R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11174. IEP_SYNC0_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	SYNC0_PEND	R	0h	SYNC0 pending state 0h = SYNC0 is not pending 1h = SYNC0 is pending or has occurred when SYNC0_ACK_EN = 0 (Disable). Write "1" to clear

91 IEP_SYNC1_STAT_REG Register (Offset = 18Ch) [reset = X]

IEP_SYNC1_STAT_REG is shown in Figure 14-3698 and described in Table 14-7479.

Return to Summary Table.

Sync 1 Status Register.

Table 14-11175. IEP_SYNC1_STAT_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E18Ch
PRU_ICSSG0_IEP1	3002 F18Ch
PRU_ICSSG1_IEP0	300A E18Ch
PRU_ICSSG1_IEP1	300A F18Ch

Figure 14-3698. IEP_SYNC1_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							SYNC1_PEND
R-X							R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11177. IEP_SYNC1_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	SYNC1_PEND	R	0h	SYNC1 pending state 0h = SYNC1 is not pending 1h = SYNC1 is pending or has occurred when SYNC1_ACK_EN = 0 (Disable). Write "1" to Clear

92 IEP_SYNC_PWIDTH_REG Register (Offset = 190h) [reset = 0h]

IEP_SYNC_PWIDTH_REG is shown in Figure 14-3699 and described in Table 14-7481.

Return to Summary Table.

Sync Pulse Width Configure Register.

Table 14-11178. IEP_SYNC_PWIDTH_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E190h
PRU_ICSSG0_IEP1	3002 F190h
PRU_ICSSG1_IEP0	300A E190h
PRU_ICSSG1_IEP1	300A F190h

Figure 14-3699. IEP_SYNC_PWIDTH_REG Register

31–0
SYNC_HPW
R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11180. IEP_SYNC_PWIDTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC_HPW	R/W	0h	Defines the number of clock cycles SYNC0/1 will be high. Note if SYNC0/1 is disabled during pulse width time (that is, SYNC_CTRL[SYNC0_EN | SYNC1_EN | SYNC_EN] = 0), the ongoing pulse will be terminated. 0h = 1 clock cycle. 1h = 2 clock cycles. Nh: N+1 clock cycles.

93 IEP_SYNC0_PERIOD_REG Register (Offset = 194h) [reset = 1h]

IEP_SYNC0_PERIOD_REG is shown in Figure 14-3700 and described in Table 14-7483.

Return to Summary Table.

Sync 0 Period Configure Register.

Table 14-11181. IEP_SYNC0_PERIOD_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E194h
PRU_ICSSG0_IEP1	3002 F194h
PRU_ICSSG1_IEP0	300A E194h
PRU_ICSSG1_IEP1	300A F194h

Figure 14-3700. IEP_SYNC0_PERIOD_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC0_PERIOD																															
R/W-1h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11183. IEP_SYNC0_PERIOD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC0_PERIOD	R/W	1h	Defines the period between the rising edges of SYNC0. 0h = Reserved 1h = 2 clk cycles period N: N+1 clk cycles period

94 IEP_SYNC1_DELAY_REG Register (Offset = 198h) [reset = 0h]

IEP_SYNC1_DELAY_REG is shown in Figure 14-3701 and described in Table 14-7485.

Return to Summary Table.

Sync 1 Delay Register.

Table 14-11184. IEP_SYNC1_DELAY_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E198h
PRU_ICSSG0_IEP1	3002 F198h
PRU_ICSSG1_IEP0	300A E198h
PRU_ICSSG1_IEP1	300A F198h

Figure 14-3701. IEP_SYNC1_DELAY_REG Register

31–0
SYNC1_DELAY
R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11186. IEP_SYNC1_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC1_DELAY	R/W	0h	When SYNC1_IND_EN = 0, defines number of clock cycles from the start of SYNC0 to the start of SYNC1. Note: this is the delay before the start of SYNC1. 0h = No delay. 1h = 1 clock cycle delay. Nh: N clock cycles delay. When SYNC1_IND_EN = 1, defines the period between the rising edges of SYNC1. 0h = Reserved. 1h = 2 clock cycles period. Nh: N+1 clock cycles period.

95 IEP_SYNC_START_REG Register (Offset = 19Ch) [reset = 0h]

IEP_SYNC_START_REG is shown in Figure 14-3702 and described in Table 14-7487.

Return to Summary Table.

Sync Start Configure Register.

Table 14-11187. IEP_SYNC_START_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E19Ch
PRU_ICSSG0_IEP1	3002 F19Ch
PRU_ICSSG1_IEP0	300A E19Ch
PRU_ICSSG1_IEP1	300A F19Ch

Figure 14-3702. IEP_SYNC_START_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">SYNC_START</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11189. IEP_SYNC_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC_START	R/W	0h	Defines the start time after the activation event. 0h = 1 clock cycle delay. Nh: N+1 clock cycles delay.

96 IEP_WD_PREDIV_REG Register (Offset = 200h) [reset = X]

IEP_WD_PREDIV_REG is shown in Figure 14-3703 and described in Table 14-7489.

Return to Summary Table.

Watchdog Pre-Divider Register

Table 14-11190. IEP_WD_PREDIV_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E200h
PRU_ICSSG0_IEP1	3002 F200h
PRU_ICSSG1_IEP0	300A E200h
PRU_ICSSG1_IEP1	300A F200h

Figure 14-3703. IEP_WD_PREDIV_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">PRE_DIV</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-4E20h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11192. IEP_WD_PREDIV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PRE_DIV	R/W	4E20h	Defines the number of ICSS_IEP_CLK cycles per WD clock event. Note that the WD clock is a free-running clock. The value 0x4e20 (or 20000) generates a rate of 100 us if ICSS_IEP_CLK is 200 MHz. seconds/(WD event) = (clock cycles per WD event)/(clock cycles per second) = 20000/(200 x [10]^6) = 100us

97 IEP_PDI_WD_TIM_REG Register (Offset = 204h) [reset = X]

IEP_PDI_WD_TIM_REG is shown in Figure 14-3704 and described in Table 14-7491.

Return to Summary Table.

PDI Watchdog Timer Configure Register.

Table 14-11193. IEP_PDI_WD_TIM_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E204h
PRU_ICSSG0_IEP1	3002 F204h
PRU_ICSSG1_IEP0	300A E204h
PRU_ICSSG1_IEP1	300A F204h

Figure 14-3704. IEP_PDI_WD_TIM_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PDI_WD_TIME															
R/W-X																R/W-3E8h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11195. IEP_PDI_WD_TIM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PDI_WD_TIME	R/W	3E8h	Defines the number of WD ticks (or increments) for PDI WD, that is, the number of WD increments. If PRUSS_IEP_WD_PREDIV[15-0] PRE_DIV is set to 100us, then the value 0x03e8 (or 1000) provides a rate of 100ms. Read returns the current count. Counter is reset by software write to register or when Digital Data In capture occurs. WD is disabled if WD time is set to 0x0. Note: when an expiration event occurs, the expiration counter (PDI_EXP_CNT) increments and status (PDI_WD_STAT) clears.

98 IEP_PD_WD_TIM_REG Register (Offset = 208h) [reset = X]

IEP_PD_WD_TIM_REG is shown in Figure 14-3705 and described in Table 14-7493.

Return to Summary Table.

PD Watchdog Timer Configure Register.

Table 14-11196. IEP_PD_WD_TIM_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E208h
PRU_ICSSG0_IEP1	3002 F208h
PRU_ICSSG1_IEP0	300A E208h
PRU_ICSSG1_IEP1	300A F208h

Figure 14-3705. IEP_PD_WD_TIM_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PD_WD_TIME															
R/W-X																R/W-3E8h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11198. IEP_PD_WD_TIM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PD_WD_TIME	R/W	3E8h	Defines the number of WD ticks (or increments) for PD WD, that is, the number of WD increments. If PRUSS_IEP_WD_PREDIV[15-0] PRE_DIV is set to 100us, then 0x03e8 (or 1000) provides a rate of 100ms. Read returns the current count. Counter is reset by software write to register or every write access to Sync Managers with WD trigger enable bit set. WD is disabled if WD time is set to 0x0. Expiration actions: Increment expiration counter, clear status. Digital Data out forced to zero if pr[k]_edio_oe_ext = 1 and PRUSS_IEP_DIGIO_EXP[0] SW_DATA_OUT_UPDATE = 0.

99 IEP_WD_STATUS_REG Register (Offset = 20Ch) [reset = X]

IEP_WD_STATUS_REG is shown in Figure 14-3706 and described in Table 14-7495.

Return to Summary Table.

Watchdog Status Register.

Table 14-11199. IEP_WD_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E20Ch
PRU_ICSSG0_IEP1	3002 F20Ch
PRU_ICSSG1_IEP0	300A E20Ch
PRU_ICSSG1_IEP1	300A F20Ch

Figure 14-3706. IEP_WD_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_STAT
R-X							R-1h
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_STAT
R-X							R-1h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11201. IEP_WD_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16	PDI_WD_STAT	R	1h	WD PDI status. 0h = Expired (PDI_WD_EXP event generated) 1h = Active or disabled
15-1	RESERVED	R	X	
0	PD_WD_STAT	R	1h	WD PD status (triggered by Sync Mangers status). 0h = Expired (PD_WD_EXP event generated) 1h = Active or disabled

100 IEP_WD_EXP_CNT_REG Register (Offset = 210h) [reset = X]

IEP_WD_EXP_CNT_REG is shown in Figure 14-3707 and described in Table 14-7497.

Return to Summary Table.

Watchdog Timer Expiration Counter Register.

Table 14-11202. IEP_WD_EXP_CNT_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E210h
PRU_ICSSG0_IEP1	3002 F210h
PRU_ICSSG1_IEP0	300A E210h
PRU_ICSSG1_IEP1	300A F210h

Figure 14-3707. IEP_WD_EXP_CNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PD_EXP_CNT								PDI_EXP_CNT							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11204. IEP_WD_EXP_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PD_EXP_CNT	R/W	0h	WD PD expiration counter. Counter increments on every PD time out and stops at FFh.
7-0	PDI_EXP_CNT	R/W	0h	WD PDI expiration counter. Counter increments on every PDI time out and stops at FFh.

101 IEP_WD_CTRL_REG Register (Offset = 214h) [reset = X]

IEP_WD_CTRL_REG is shown in Figure 14-3708 and described in Table 14-7499.

Return to Summary Table.

Watchdog Control Register.

Table 14-11205. IEP_WD_CTRL_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E214h
PRU_ICSSG0_IEP1	3002 F214h
PRU_ICSSG1_IEP0	300A E214h
PRU_ICSSG1_IEP1	300A F214h

Figure 14-3708. IEP_WD_CTRL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11207. IEP_WD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PDI_WD_EN	R/W	0h	Watchdog PDI 0h = Disable 1h = Enable
15-1	RESERVED	R/W	X	
0	PD_WD_EN	R/W	0h	Watchdog PD 0h = Disable 1h = Enable

102 IEP_DIGIO_CTRL_REG Register (Offset = 300h) [reset = X]

IEP_DIGIO_CTRL_REG is shown in Figure 14-3709 and described in Table 14-7501.

Return to Summary Table.

DIGIO Control Register.

Table 14-11208. IEP_DIGIO_CTRL_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E300h
PRU_ICSSG0_IEP1	3002 F300h
PRU_ICSSG1_IEP0	300A E300h
PRU_ICSSG1_IEP1	300A F300h

Figure 14-3709. IEP_DIGIO_CTRL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUT_MODE		IN_MODE		WD_MODE	BIDI_MODE	OUTVALID_MODE	OUTVALID_POL
R/W-0h		R/W-0h		R/W-0h	R-1h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11210. IEP_DIGIO_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	OUT_MODE	R/W	0h	Defines events that triggers data out to be updated. Note if OUTVALID_MODE is set, then data out is forced to zero if a WD PD expiration occurs (PD_WD_EXP) from the WD block and pr<k>_edio_oe_ext = 1. 0h = PRU0/1_RX_EOF 1h = Reserved 2h: DC SYNC0 event 3h = DC SYNC1 event After ML release keep Reserved in filter2 and delete Reserved without filter

Table 14-11210. IEP_DIGIO_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	IN_MODE	R/W	0h	Defines event that triggers data in to be sampled 0h = PRU0/1_RX_SOF After ML release put PRU0/1_RX_SOF to filter1; delete Reserved without filter 1h = Rising edge of external PR<k>_EDC_LATCH0_IN signal 2h: DC rising edge of SYNC0 event After ML release put DC rising edge of SYNC0 event to filter1; delete Reserved without filter 3h = DC rising edge of SYNC1 event After ML release put DC rising edge of SYNC1 event to filter1; delete Reserved without filter
3	WD_MODE	R/W	0h	Defines Watchdog behavior 0h = Outputs are reset immediately after watchdog expires 1h = Outputs are reset with next output event that follows watchdog expiration After ML release keep Reserved in filter2 and delete Reserved without filter
2	BIDI_MODE	R	1h	Defines the digital input/output direction. NOTE THAT DUE TO INTEGRATION, ACTUAL MODE IS UNIDIRECTIONAL IN THIS DEVICE. 0h = Unidirectional mode: digital input/output direction of pins configured individually 1h = Bidirectional mode: all I/O pins are bidirectional and direction configuration is ignored After ML release keep Reserved in filter2 and delete Reserved without filter
1	OUTVALID_MODE	R/W	0h	Defines the outvalid mode behavior. 0h = Output event signaling 1h = Output data is updated if watchdog is triggered. Output data is forced to zero if PD_WD_EXP from the WD block and pr1_edio_oe_ext = 1 After ML release keep Reserved in filter2 and delete Reserved without filter
0	OUTVALID_POL	R	0h	Defines OUTVALID polarity 0h = Active High 1h = Active Low After ML release keep Reserved in filter2 and delete Reserved without filter

103 IEP_DIGIO_STATUS_REG Register (Offset = 304h) [reset = 0h]

IEP_DIGIO_STATUS_REG is shown in Figure 14-3710 and described in Table 14-7503.

Return to Summary Table.

DIGIO Status Register.

Table 14-11211. IEP_DIGIO_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E304h
PRU_ICSSG0_IEP1	3002 F304h
PRU_ICSSG1_IEP0	300A E304h
PRU_ICSSG1_IEP1	300A F304h

Figure 14-3710. IEP_DIGIO_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIGIO_STAT																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11213. IEP_DIGIO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIGIO_STAT	R	0h	Reserved

104 IEP_DIGIO_DATA_IN_REG Register (Offset = 308h) [reset = 0h]

IEP_DIGIO_DATA_IN_REG is shown in Figure 14-3711 and described in Table 14-7505.

Return to Summary Table.

DIGIO Data Input Register.

Table 14-11214. IEP_DIGIO_DATA_IN_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E308h
PRU_ICSSG0_IEP1	3002 F308h
PRU_ICSSG1_IEP0	300A E308h
PRU_ICSSG1_IEP1	300A F308h

Figure 14-3711. IEP_DIGIO_DATA_IN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_IN																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11216. IEP_DIGIO_DATA_IN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_IN	R	0h	Data input. Digital inputs can be configured to be sampled in four ways. 1h = Digital inputs are sampled at the start of each frame. The SOF signal can be used externally to update the input data, because the SOF is signaled before input data is sampled. 2h: The sample time can be controlled externally by using the PR<k>_EDC_LATCH0_IN signal. 3h = Digital inputs are sampled at SYNC0 events. 4h = Digital inputs are sampled at SYNC1 events. These can be configured by [5-4] IN_MODE bit field in the PRUSS_IEP_DIGIO_CTRL register.

105 IEP_DIGIO_DATA_IN_RAW_REG Register (Offset = 30Ch) [reset = 0h]

IEP_DIGIO_DATA_IN_RAW_REG is shown in Figure 14-3712 and described in Table 14-7507.

Return to Summary Table.

DIGIO Data Input Direct Sample Register.

Table 14-11217. IEP_DIGIO_DATA_IN_RAW_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E30Ch
PRU_ICSSG0_IEP1	3002 F30Ch
PRU_ICSSG1_IEP0	300A E30Ch
PRU_ICSSG1_IEP1	300A F30Ch

Figure 14-3712. IEP_DIGIO_DATA_IN_RAW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_IN_RAW																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11219. IEP_DIGIO_DATA_IN_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_IN_RAW	R	0h	Data input which direct sample of PR<k>_EDIO_DATA[0:31]. Only PR<k>_EDIO_DATA[0:3] are exported to device pins in this device.

106 IEP_DIGIO_DATA_OUT_REG Register (Offset = 310h) [reset = 0h]

IEP_DIGIO_DATA_OUT_REG is shown in Figure 14-3713 and described in Table 14-7509.

Return to Summary Table.

DIGIO Data Output Register.

Table 14-11220. IEP_DIGIO_DATA_OUT_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E310h
PRU_ICSSG0_IEP1	3002 F310h
PRU_ICSSG1_IEP0	300A E310h
PRU_ICSSG1_IEP1	300A F310h

Figure 14-3713. IEP_DIGIO_DATA_OUT_REG Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">DATA_OUT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11222. IEP_DIGIO_DATA_OUT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_OUT	R/W	0h	Data output. Digital outputs can be configured to be updated in four ways. 1h = Digital outputs are updated at the end of each frame (EOF mode). 2h: Digital outputs are updated with SYNC0 events 3h = Digital outputs are updated SYNC1 events. 4h = Digital outputs are updated at the end of a frame which triggered the Process Data Watchdog. Digital Outputs are only updated if the frame was correct (WD_TRIG mode). These can be configured by [7-6] OUT_MODE bit field in the PRUSS_IEP_DIGIO_CTRL.

107 IEP_DIGIO_DATA_OUT_EN_REG Register (Offset = 314h) [reset = 0h]

IEP_DIGIO_DATA_OUT_EN_REG is shown in Figure 14-3714 and described in Table 14-7511.

Return to Summary Table.

DIGIO Data Input which controls tri-state of pr<k>_edio_data_out_en[3:0] Register.

Table 14-11223. IEP_DIGIO_DATA_OUT_EN_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E314h
PRU_ICSSG0_IEP1	3002 F314h
PRU_ICSSG1_IEP0	300A E314h
PRU_ICSSG1_IEP1	300A F314h

Figure 14-3714. IEP_DIGIO_DATA_OUT_EN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_OUT_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11225. IEP_DIGIO_DATA_OUT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_OUT_EN	R/W	0h	Data input which controls tri-state of PR<k>_EDIO_DATA[0:3] 0h = Driver enabled. 1h = Sets outputs to HiZ.

108 IEP_DIGIO_EXP_REG Register (Offset = 318h) [reset = X]

IEP_DIGIO_EXP_REG is shown in Figure 14-3715 and described in Table 14-7513.

Return to Summary Table.

DIGIO, Defines which RX_EOF is used Register.

Table 14-11226. IEP_DIGIO_EXP_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	3002 E318h
PRU_ICSSG0_IEP1	3002 F318h
PRU_ICSSG1_IEP0	300A E318h
PRU_ICSSG1_IEP1	300A F318h

Figure 14-3715. IEP_DIGIO_EXP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED		EOF_SEL	SOF_SEL	SOF_DLY			
R/W-X		R/W-0h	R/W-0h	R/W-0h			

7	6	5	4	3	2	1	0
OUTVALID_DLY				RESERVED	SW_OUTVALID	OUTVALID_OVR_EN	SW_DATA_OUT_UP
R/W-2h				R/W-X	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11228. IEP_DIGIO_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13	EOF_SEL	R/W	0h	Defines which RX_EOF is used for PR<k>_EDIO_DATA_IN[0:3] capture 0h = PRU0_RX_EOF 1h = PRU1_RX_EOF After ML release keep Reserved in filter2 and delete Reserved without filter
12	SOF_SEL	R/W	0h	Defines which RX_SOF is used for PR<k>_EDIO_DATA_IN[0:3] capture 0h = PRU0_RX_SOF 1h = PRU1_RX_SOF After ML release keep Reserved in filter2 and delete Reserved without filter

Table 14-11228. IEP_DIGIO_EXP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	SOF_DLY	R/W	0h	Define the number of iep_clk (ICSS_IEP_CLK) cycle delay of SOF PR<k>_EDIO_DATA_IN[0:3] capture After ML release keep Reserved in filter2 and delete Reserved without filter
7-4	OUTVALID_DLY	R/W	2h	Define the number of iep_clk (ICSS_IEP_CLK) cycle delay on assertion of PR<k>_EDIO_OUTVALID. Min is 2 clock cycles. Max is 16 clock cycles After ML release keep Reserved in filter2 and delete Reserved without filter
3	RESERVED	R/W	X	
2	SW_OUTVALID	R/W	0h	PR<k>_EDIO_OUTVALID = SW_OUTVALID, only if OUTVALID_OVR_EN is set. After ML release keep Reserved in filter2 and delete Reserved without filter
1	OUTVALID_OVR_EN	R/W	0h	Software override enable 0h = Disable override 1h = Enable override
0	SW_DATA_OUT_UP	R/W	0h	Defines the value of pr<k>_edio_data_out when OUTVALID_OVR_EN = 1. Read 0h = Start bit event has not occurred Read 1h = Start bit event occurred Write 0h = No effect Write 1h = Causes an update of pr<k>_edio_data_out by software data out

14.3.6.1.26 PRU_MDIO_MDIO Registers

Table 14-7515 lists the memory-mapped registers for the PRU_MDIO_MDIO registers. All register offset addresses not listed in Table 14-7515 should be considered as reserved locations and the register contents should not be modified.

Table 14-11229. PRU_MDIO_MDIO Instances

Instance	Base Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2400h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2400h

Table 14-11230. PRU_MDIO_MDIO Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MDIO_V1P7_MDIO Physical Address	PRU_ICSSG1_PR1_MDIO_V1P7_MDIO Physical Address
0h	MDIO_VERSION_REG	MDIO Version Register	3003 2400h	300B 2400h
4h	MDIO_CONTROL_REG	MDIO Control Register	3003 2404h	300B 2404h
8h	MDIO_ALIVE_REG	MDIO Alive Register	3003 2408h	300B 2408h
Ch	MDIO_LINK_REG	MDIO Link Register	3003 240Ch	300B 240Ch
10h	MDIO_LINK_INT_RAW_REG	MDIO Link Interrupt Raw Register	3003 2410h	300B 2410h
14h	MDIO_LINK_INT_MASKED_REG	MDIO Link Interrupt Masked Register	3003 2414h	300B 2414h
18h	MDIO_LINK_INT_MASK_SET_REG	MDIO Link Interrupt Mask Set Register	3003 2418h	300B 2418h
1Ch	MDIO_LINK_INT_MASK_CLEAR_REG	MDIO Link Interrupt Mask Clear Register	3003 241Ch	300B 241Ch
20h	MDIO_USER_INT_RAW_REG	MDIO User Interrupt Raw Register	3003 2420h	300B 2420h
24h	MDIO_USER_INT_MASKED_REG	MDIO User Interrupt Masked Register	3003 2424h	300B 2424h
28h	MDIO_USER_INT_MASK_SET_REG	MDIO User Interrupt Mask Set Register	3003 2428h	300B 2428h
2Ch	MDIO_USER_INT_MASK_CLEAR_REG	MDIO User Interrupt Mask Clear Register	3003 242Ch	300B 242Ch
30h	MDIO_MANUAL_IF_REG	MDIO Manual Interface Register	3003 2430h	300B 2430h
34h	MDIO_POLL_REG	MDIO Poll Inter Register	3003 2434h	300B 2434h
38h	MDIO_POLL_EN_REG	MDIO Poll Enable Register	3003 2438h	300B 2438h
3Ch	MDIO_CLAUS45_REG	Clause 45 Register	3003 243Ch	300B 243Ch
40h	MDIO_USER_ADDR0_REG	MDIO User Address 0 Register	3003 2440h	300B 2440h
44h	MDIO_USER_ADDR1_REG	MDIO User Address 1 Register	3003 2444h	300B 2444h
80h	MDIO_USER_ACCESS_REG_j	MDIO User Access j Register	3003 2480h	300B 2480h
84h	MDIO_USER_PHY_SEL_REG_j	MDIO User PHY Select j Register	3003 2484h	300B 2484h

1 MDIO_VERSION_REG Register (Offset = 0h) [reset = 00070107h]

MDIO_VERSION_REG is shown in Figure 14-3716 and described in Table 14-7517.

Return to Summary Table.

MDIO Version Register.

Table 14-11231. MDIO_VERSION_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2400h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2400h

Figure 14-3716. MDIO_VERSION_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODID																REVMAJ								REVMINOR							
R-7h																R-1h								R-7h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11233. MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	7h	Module Identification value
15-8	REVMAJ	R	1h	Major revision value
7-0	REVMINOR	R	7h	Minor revision value

2 MDIO_CONTROL_REG Register (Offset = 4h) [reset = X]

MDIO_CONTROL_REG is shown in Figure 14-3717 and described in Table 14-7519.

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MDIO Control Register.

Table 14-11234. MDIO_CONTROL_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2404h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2404h

Figure 14-3717. MDIO_CONTROL_REG Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R-1h	R/W-0h	R/W-X	R-1h				

23	22	21	20	19	18	17	16
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
R/W-X			R/W-0h	R/W1C-0h	R/W-0h	R/W-0h	R/W-X

15	14	13	12	11	10	9	8
CLKDIV							
R/W-FFh							

7	6	5	4	3	2	1	0
CLKDIV							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-11236. MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1h when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1 to this bit enables the MDIO state machine, writing a 0h disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	R/W	X	
28-24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest user access channel that is available in the module and is currently set to 1h. This implies that MDIO_USER_ACCESS_REG_1 is the highest available user access channel.
23-21	RESERVED	R/W	X	

Table 14-11236. MDIO_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1h to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.
19	FAULT	R/W1C	0h	Fault indicator. This bit is set to 1h if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1 to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1h to enable the physical layer fault detection.
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1h to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	R/W	X	
15-0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. MDCLK is disabled when [15-0] CLKDIV is set to 0h. MDCLK frequency = clk frequency/(clkdiv+1).

3 MDIO_ALIVE_REG Register (Offset = 8h) [reset = 0h]

MDIO_ALIVE_REG is shown in Figure 14-3718 and described in Table 14-7521.

Return to Summary Table.

MDIO Alive Register.

Table 14-11237. MDIO_ALIVE_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2408h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2408h

Figure 14-3718. MDIO_ALIVE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIVE																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-11239. MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ALIVE	R/W1C	0h	MDIO Alive. Each of the 32 bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address. Writing a 1 to any bit will clear it, writing a 0 has no effect.

4 MDIO_LINK_REG Register (Offset = Ch) [reset = 0h]

MDIO_LINK_REG is shown in Figure 14-3719 and described in Table 14-7523.

Return to Summary Table.

MDIO Link Register.

Table 14-11240. MDIO_LINK_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 240Ch
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 240Ch

Figure 14-3719. MDIO_LINK_REG Register

31-0
LINK
R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11242. MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LINK	R	0h	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to zero if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIO_USER_PHY_SEL_REG_j register can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIO_USER_PHY_SEL_REG_j register. In State Change Mode the MLINK input pins are unused.

5 MDIO_LINK_INT_RAW_REG Register (Offset = 10h) [reset = X]

MDIO_LINK_INT_RAW_REG is shown in Figure 14-3720 and described in Table 14-7525.

Return to Summary Table.

MDIO Link Interrupt Raw Register.

Table 14-11243. MDIO_LINK_INT_RAW_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2410h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2410h

Figure 14-3720. MDIO_LINK_INT_RAW_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">LINKINTRAW</td></tr>
<tr><td colspan="6">R/W-X</td><td colspan="2">R/W1C-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-11245. MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	

Table 14-11245. MDIO_LINK_INT_RAW_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	LINKINTRAW	R/W1C	0h	MDIO link change event raw value. Normal mode operation: When asserted ‘1’, a bit indicates that there was an MDIO link change event (that is, change in the MDIO_LINK_REG register) corresponding to the PHY address in the MDIO_USER_PHY_SEL_REG_j register. LINKINTRAW[0] and LINKINTRAW[1] correspond to MDIO_USER_PHY_SEL_REG_0 and MDIO_USER_PHY_SEL_REG_1, respectively. Writing a 1h will clear the event and writing 0 has no effect. If the int_test bit in the MDIO_CONTROL_REG register is set, the host may set LINKINTRAW bits to a 1h which may be used for test purposes. MDIO link change event raw value. State Change Mode operation: The LINKINTRAW[0] bit will be asserted ‘1’ when any bit (for any PHY) in the MDIOAlive or MDIO_LINK_REG registers changes due to MDIO operations. The LINKINTRAW[1] bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the int_test bit in the MDIO_CONTROL_REG register is set, the host may set the LINKINTRAW[0] bit to a 1h which may be used for test purposes.

6 MDIO_LINK_INT_MASKED_REG Register (Offset = 14h) [reset = X]

MDIO_LINK_INT_MASKED_REG is shown in Figure 14-3721 and described in Table 14-7527.

Return to Summary Table.

MDIO Link Interrupt Masked Register.

Table 14-11246. MDIO_LINK_INT_MASKED_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2414h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2414h

Figure 14-3721. MDIO_LINK_INT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-11248. MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	

Table 14-11248. MDIO_LINK_INT_MASKED_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	LINKINTMASKED	R/W1C	0h	MDIO link change interrupt masked value. Normal mode operation: When asserted ‘1’, a bit indicates that there was an MDIO link change event (that is, change in the MDIO_LINK_REG register) corresponding to the PHY address in the MDIO_USER_PHY_SEL_REG_j register and the corresponding linkint_enable bit was set. linkintmasked[0] and linkintmasked[1] correspond to MDIO_USER_PHY_SEL_REG_0 and MDIO_USER_PHY_SEL_REG_1, respectively. Writing a 1h will clear the interrupt and writing 0 has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values. MDIO link change interrupt masked value. State Change Mode operation: The linkintmasked[0] bit will be asserted ‘1’ when LINKINTRAW[0] is asserted ‘1’ and when the linkintmaskset bit is set to 1h. Writing a 1h will clear linkintmasked[0] (and the MDIO_LINKINT[0] output) and writing 0h has no effect. The linkintmasked[1] bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode).

7 MDIO_LINK_INT_MASK_SET_REG Register (Offset = 18h) [reset = X]

MDIO_LINK_INT_MASK_SET_REG is shown in Figure 14-3722 and described in Table 14-7529.

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MDIO Link Interrupt Mask Set Register.

Table 14-11249. MDIO_LINK_INT_MASK_SET_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2418h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2418h

Figure 14-3722. MDIO_LINK_INT_MASK_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							LINKINTMASKSET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-11251. MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINKINTMASKSET	R/W1S	0h	MDIO link interrupt mask set. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIO_USER_PHY_SEL_REG_j register. MDIO link interrupt mask set. State Change Mode Operation: Writing this bit to 1h will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when LINKINTRAW[0] is asserted.

8 MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = 1Ch) [reset = X]

MDIO_LINK_INT_MASK_CLEAR_REG is shown in Figure 14-3723 and described in Table 14-7531.

Return to Summary Table.

MDIO Link Interrupt Mask Clear Register.

Table 14-11252. MDIO_LINK_INT_MASK_CLEAR_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 241Ch
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 241Ch

Figure 14-3723. MDIO_LINK_INT_MASK_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED							
R/W-X							

7	6	5	4	3	2	1	0
RESERVED							LINKINTMASKCLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-11254. MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINKINTMASKCLR	R/W1C	0h	MDIO link interrupt mask clear. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIO_USER_PHY_SEL_REG_j register. MDIO link interrupt mask clear. State Change Mode Operation: Writing this bit to 1h will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the LINKINTRAW[0] bit value.

9 MDIO_USER_INT_RAW_REG Register (Offset = 20h) [reset = X]

MDIO_USER_INT_RAW_REG is shown in Figure 14-3724 and described in Table 14-7533.

Return to Summary Table.

MDIO User Interrupt Raw Register.

Table 14-11255. MDIO_USER_INT_RAW_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2420h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2420h

Figure 14-3724. MDIO_USER_INT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-11257. MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTRAW	R/W1C	0h	Raw value of MDIO user command complete event for MDIO_USER_ACCESS_REG_1 through MDIO_USER_ACCESS_REG_0, respectively. When asserted ‘1’, a bit indicates that the previously scheduled PHY read or write command using that particular MDIO_USER_ACCESS_REG_j register has completed. Writing a 1h will clear the event and writing 0h has no effect. If the int_test bit in the MDIO_CONTROL_REG register is set, the host may set the userintraw bits to a 1h. This mode may be used for test purposes.

10 MDIO_USER_INT_MASKED_REG Register (Offset = 24h) [reset = X]

MDIO_USER_INT_MASKED_REG is shown in Figure 14-3725 and described in Table 14-7535.

Return to Summary Table.

MDIO User Interrupt Masked Register.

Table 14-11258. MDIO_USER_INT_MASKED_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2424h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2424h

Figure 14-3725. MDIO_USER_INT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-11260. MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKED	R/W1C	0h	Masked value of MDIO user command complete interrupt for MDIO_USER_ACCESS_REG_1 through MDIO_USER_ACCESS_REG_0, respectively. When asserted ‘1’, a bit indicates that the previously scheduled PHY read or write command using that particular MDIO_USER_ACCESS_REG_j register has completed and the corresponding userintmaskset bit is set to 1h. Writing a 1h will clear the interrupt and writing 0h has no effect. If the int_test bit in the MDIO_CONTROL_REG register is set, the host may set the USERINTMASKED bits to a 1h. This mode may be used for test purposes.

11 MDIO_USER_INT_MASK_SET_REG Register (Offset = 28h) [reset = X]

MDIO_USER_INT_MASK_SET_REG is shown in Figure 14-3726 and described in Table 14-7537.

Return to Summary Table.

MDIO User Interrupt Mask Set Register.

Table 14-11261. MDIO_USER_INT_MASK_SET_REG Instances

Instance	**Physical Address**
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2428h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2428h

Figure 14-3726. MDIO_USER_INT_MASK_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						USERINTMASKSET	
R/W-X						R/W1S-0h	

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-11263. MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKSET	R/W1S	0h	MDIO user interrupt mask set for USERINTMASKED[1:0], respectively. Writing a bit to 1h will enable MDIO user command complete interrupts for that particular MDIO_USER_ACCESS_REG_j register. MDIO user interrupt for a particular MDIO_USER_ACCESS_REG_j register is disabled if the corresponding bit is 0h. Writing a 0h to this register has no effect.

12 MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = 2Ch) [reset = X]

MDIO_USER_INT_MASK_CLEAR_REG is shown in Figure 14-3727 and described in Table 14-7539.

Return to Summary Table.

MDIO User Interrupt Mask Clear Register.

Table 14-11264. MDIO_USER_INT_MASK_CLEAR_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 242Ch
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 242Ch

Figure 14-3727. MDIO_USER_INT_MASK_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
RESERVED							
R/W-X							

7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-11266. MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKCLR	R/W1C	0h	MDIO user command complete interrupt mask clear for USERINTMASKED[1:0], respectively. Writing a bit to 1h will disable further user command complete interrupts for that particular MDIO_USER_ACCESS_REG_j register. Writing a 0h to this register has no effect.

13 MDIO_MANUAL_IF_REG Register (Offset = 30h) [reset = X]

MDIO_MANUAL_IF_REG is shown in Figure 14-3728 and described in Table 14-7541.

Return to Summary Table.

MDIO Manual Interface Register.

Table 14-11267. MDIO_MANUAL_IF_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2430h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2430h

Figure 14-3728. MDIO_MANUAL_IF_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>MDIO_MDCLK_O</td><td>MDIO_OE</td><td>MDIO_PIN</td></tr>
<tr><td colspan="5">R/W-X</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11269. MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output. This value is the MDCLK_O output value when the MANUALMODE bit is set in the MDIO_POLL_REG register.
1	MDIO_OE	R/W	0h	MDIO Output Enable. This value is inverted and output on the MDIO_OE_N output when the MANUALMODE bit is set in the MDIO_POLL_REG register.
0	MDIO_PIN	R/W	0h	MDIO_Pin Value. This is the external MDIO data pin value when the MANUALMODE bit is set in the MDIO_POLL_REG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted ‘1’. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted ‘1’ and MDIO_PIN is written with a 1h then MDIO_PIN should read a 1h if there are no external devices pulling the MDIO data line low.

14 MDIO_POLL_REG Register (Offset = 34h) [reset = X]

MDIO_POLL_REG is shown in Figure 14-3729 and described in Table 14-7543.

Return to Summary Table.

MDIO Poll Inter Register.

Table 14-11270. MDIO_POLL_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2434h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2434h

Figure 14-3729. MDIO_POLL_REG Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANGEMODE	RESERVED					
R/W-0h	R/W-0h	R/W-X					
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
IPG							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11272. MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	Manual Mode. When set 1h, the MDIO pins are directly controlled by software through the bits in the MDIO_MANUAL_IF_REG register
30	STATECHANGEMODE	R/W	0h	State Change Mode. When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations.
29-8	RESERVED	R/W	X	
7-0	IPG	R/W	0h	Polling Inter Packet Gap Value. This value is the number of MDCLK_O clocks between each poll when polling is enabled.

15 MDIO_POLL_EN_REG Register (Offset = 38h) [reset = FFFFFFFFh]

MDIO_POLL_EN_REG is shown in Figure 14-3730 and described in Table 14-7545.

Return to Summary Table.

MDIO Poll Enable Register.

Table 14-11273. MDIO_POLL_EN_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2438h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2438h

Figure 14-3730. MDIO_POLL_EN_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">POLL_EN</td></tr>
<tr><td colspan="32">R/W-FFFFFFFFh</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11275. MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	POLL_EN	R/W	FFFFFFFFh	Poll Enable. When set, the bit indicates that the associated PHY will be included in polling operations. When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set (regardless of the value of the preamble disable bit in the MDIO_CONTROL register. However, there does not have to be a PHY at address 31.

16 MDIO_CLAUS45_REG Register (Offset = 3Ch) [reset = 0h]

MDIO_CLAUS45_REG is shown in Figure 14-3731 and described in Table 14-7547.

Return to Summary Table.

Claus 45 Register.

Table 14-11276. MDIO_CLAUS45_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 243Ch
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 243Ch

Figure 14-3731. MDIO_CLAUS45_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CLAUSE45</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11278. MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAUSE45	R/W	0h	MDIO clause 45 mode. When a CLAUSE45 bit is cleared to 0h, the PHY associated with the CLAUSE45 bit is operating in the clause 22 mode. When set 1h, the PHY associated with the CLAUSE45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on.

17 MDIO_USER_ADDR0_REG Register (Offset = 40h) [reset = X]

MDIO_USER_ADDR0_REG is shown in Figure 14-3732 and described in Table 14-7549.

Return to Summary Table.

MDIO User Address 0 Register.

Table 14-11279. MDIO_USER_ADDR0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2440h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2440h

Figure 14-3732. MDIO_USER_ADDR0_REG Register

31–16	15–0
RESERVED	USER_ADDR0
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11281. MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	USER_ADDR0	R/W	0h	User Address 0. In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIO_USER_ACCESS_REG_0 access. This is not used for PHY’s operating in clause22 mode as there is no address transfer preceding each MDIO_USER_ACCESS_REG_0 access.

18 MDIO_USER_ADDR1_REG Register (Offset = 44h) [reset = X]

MDIO_USER_ADDR1_REG is shown in Figure 14-3733 and described in Table 14-7551.

Return to Summary Table.

MDIO User Address 1 Register.

Table 14-11282. MDIO_USER_ADDR1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2444h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2444h

Figure 14-3733. MDIO_USER_ADDR1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																USER_ADDR1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11284. MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	USER_ADDR1	R/W	0h	User Address 1. In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIO_USER_ACCESS_REG_1 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceding each MDIO_USER_ACCESS_REG_1 access.

19 MDIO_USER_ACCESS_REG_j Register (Offset = 80h) [reset = X]

MDIO_USER_ACCESS_REG_j is shown in Figure 14-3734 and described in Table 14-7553.

Return to Summary Table.

MDIO User Access j Register.

Table 14-11285. MDIO_USER_ACCESS_REG_j Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2480h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2480h

Figure 14-3734. MDIO_USER_ACCESS_REG_j Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W1S-0h	R/W-0h	R/W-0h	R/W-X			R/W-0h	

23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W-0h			R/W-0h				

15	14	13	12	11	10	9	8
DATA							
R/W-0h							

7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-11287. MDIO_USER_ACCESS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W1S	0h	Go. Writing a 1h to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. writing a 0h to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIO_USER_ACCESS_REG_0 register are blocked when the go bit is 1h. If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28-26	RESERVED	R/W	X	

Table 14-11287. MDIO_USER_ACCESS_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.
20-16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

20 MDIO_USER_PHY_SEL_REG_j Register (Offset = 84h) [reset = X]

MDIO_USER_PHY_SEL_REG_j is shown in Figure 14-3735 and described in Table 14-7555.

Return to Summary Table.

MDIO User PHY Select j Register.

Table 14-11288. MDIO_USER_PHY_SEL_REG_j Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	3003 2484h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	300B 2484h

Figure 14-3735. MDIO_USER_PHY_SEL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W-0h	R/W-0h	R/W-X	R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11290. MDIO_USER_PHY_SEL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7	LINKSEL	R/W	0h	Link status determination select. Set to 1h to determine link status using the MLINK pin. Default value is 0h which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1h to enable link change status interrupts for PHY address specified in PHYADR_MON. Link change interrupts are disabled if this bit is set to 0h.
5	RESERVED	R/W	X	
4-0	PHYADR_MON	R/W	0h	PHY address whose link status is to be monitored.

14.3.6.1.27 PRU_MII_RT_MII_RT Registers

Table 14-7557 lists the memory-mapped registers for the PRU_MII_RT_MII_RT registers. All register offset addresses not listed in Table 14-7557 should be considered as reserved locations and the register contents should not be modified.

Table 14-11291. PRU_MII_RT_MII_RT Instances

Instance	Base Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2000h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2000h

Table 14-11292. PRU_MII_RT_MII_RT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG Physical Address
0h	MII_RT_RXCFG0	RX Configuration 0 Register	3003 2000h	300B 2000h
4h	MII_RT_RXCFG1	RX Configuration 1 Register	3003 2004h	300B 2004h
10h	MII_RT_TXCFG0	TX Control Register 0	3003 2010h	300B 2010h
14h	MII_RT_TXCFG1	TX Control Register 1	3003 2014h	300B 2014h
20h	MII_RT_TX_CRC0	Transmit CRC32 Register 0	3003 2020h	300B 2020h
24h	MII_RT_TX_CRC1	Transmit CRC32 Register 1	3003 2024h	300B 2024h
30h	MII_RT_TX_IPG0	TX IPG Register 0	3003 2030h	300B 2030h
34h	MII_RT_TX_IPG1	TX IPG Register 1	3003 2034h	300B 2034h
38h	MII_RT_PRS0	PORT_RAW_STATUS Register 0	3003 2038h	300B 2038h
3Ch	MII_RT_PRS1	PORT_RAW_STATUS Register 1	3003 203Ch	300B 203Ch
40h	MII_RT_RX_FRMS0	RX Frame Size Register 0	3003 2040h	300B 2040h
44h	MII_RT_RX_FRMS1	RX Frame Size Register 1	3003 2044h	300B 2044h
48h	MII_RT_RX_PCNT0	RX Preamble Cnt Register 0	3003 2048h	300B 2048h
4Ch	MII_RT_RX_PCNT1	RX Preamble Cnt Register 1	3003 204Ch	300B 204Ch
50h	MII_RT_RX_ERR0	RX Error Register 0	3003 2050h	300B 2050h
54h	MII_RT_RX_ERR1	RX Error Register 1	3003 2054h	300B 2054h
60h	MII_RT_RX_FIFO_LEVEL0	RX FIFO Level 0 Register	3003 2060h	300B 2060h
64h	MII_RT_RX_FIFO_LEVEL1	RX FIFO Level 1 Register	3003 2064h	300B 2064h
68h	MII_RT_TX_FIFO_LEVEL0	TX FIFO Register 0	3003 2068h	300B 2068h
6Ch	MII_RT_TX_FIFO_LEVEL1	TX FIFO Register 1	3003 206Ch	300B 206Ch

1 MII_RT_RXCFG0 Register (Offset = 0h) [reset = X]

MII_RT_RXCFG0 is shown in Figure 14-3736 and described in Table 14-7559.

Return to Summary Table.

RX Configuration 0 Register. This register contains the configuration variables for the RX path. MII_RT_RXCFG0 is attached to PRU0 core and controls which RX port is attached to PRU0.

Table 14-11293. MII_RT_RXCFG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2000h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2000h

Figure 14-3736. MII_RT_RXCFG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED						RX_EOF_SCLR_DIS0	RX_ERR_RAW0
R-0h						R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
RX_SFD_RAW0	RX_AUTO_FWD_PRE0	RX_BYTE_SWAP0	RX_L2_EN0	RX_MUX_SEL0	RX_CUT_PREAMBLE0	RX_DATA_RDY_MODE_DIS0	RX_ENABLE0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11295. MII_RT_RXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	
9	RX_EOF_SCLR_DIS0	R/W	0h	0h = RX_EOF flag in R31 and RXL2 is selfcleared by HW when RX2L is enabled 1h = RX_EOF flag in R31 and RXL2 is not selfcleared by HW when RX2L is enabled. A RX_EOF_CLR must get issued
8	RX_ERR_RAW0	R/W	0h	0h = ERR Raw Mode Disabled RX_ERR qualified with RX_DV RX_DV must be 1 before RX_ERR action/event is generated 1h = ERR Raw Mode Enabled RX_ERR is not qualified with RX_DV RX_ERR action/event is generated , even if RX_DV = 0
7	RX_SFD_RAW0	R/W	0h	0h = SFD Raw Mode Disabled RX_SFD requires a pattern of 5D 1h = SFD Raw Mode Enable The first byte of any pattern after RX_DV assertion will trigger RX_SFD event. The first nibble of the frame(RX_DV = 1) will be in the RX FIFO

Table 14-11295. MII_RT_RXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RX_AUTO_FWD_PRE0	R/W	0h	Auto Forward Preamble Mode 0h = Disable 1h = Enable If Enabled, RX_CUT_PREAMBLE and TX_AUTO_PREAMBLE must be disabled This will forward the preamble nibbles including the SFD to the TX FIFO that is attached to the PRU. First data byte seen by PRU R31 and/or RX L2 is DA Note: Odd number of preamble nibbles is supported in this mode. For example, 0x55D Note that new RX should only occur after the current TX completes
5	RX_BYTE_SWAP0	R/W	0h	Controls the order of the Byte0/1 placement for RX R31 and RX L2. 0h = Byte1 is the high byte for R31 and RX L2 MSB {Byte1:Byte0} LSB RX R31 15:8 = Byte1 RX R31 7:0 = Byte0 1h = Byte1 is the low byte for R31 and RX L2 MSB {Byte0:Byte1} LSB RX R31 15:8 = Byte0 RX R31 7:0 = Byte1 Must be selected /updated when the port is disabled or no traffic It only effects R31 and RX L2 order Note this cannot get enabled if TX_AUTO_SEQUENCE enabled since TX_BYTE_SWAP on swaps the PRU output.
4	RX_L2_EN0	R/W	0h	0h = Disables RX L2 buffer. Can be used as generic scratch pad. 1h = Enables RX L2 buffer
3	RX_MUX_SEL0	R/W	0h	0h = Select MII RX Data from Port 0 1h = Select MII RX Data from Port 1 The encoding is identical for both MII Ports and PRUs. Typically, the setting for this will not be identical for the two MII Receive Configuration registers.
2	RX_CUT_PREAMBLE0	R/W	0h	0h = All data from Ethernet PHY are passed on to PRU register. This assume Ethernet PHY which does not shorten the preamble 1h = MII interface suppresses preamble and sync frame delimiter. First data byte seen by PRU register is DA
1	RX_DATA_RDY_MODE_DIS0	R/W	0h	0h = R31:16 is DATA_RDY mapped 1h = R31:16 is TX_EOF mapped
0	RX_ENABLE0	R/W	0h	This enables RX traffic which is currently selected by RX_MUX_SELECT

2 MII_RT_RXCFG1 Register (Offset = 4h) [reset = X]

MII_RT_RXCFG1 is shown in Figure 14-3737 and described in Table 14-7561.

Return to Summary Table.

RX Configuration 1 Register. This register contains the configuration variables for the RX path. MII_RT_RXCFG1 is attached to PRU1 core and controls which RX port is attached to PRU1.

Table 14-11296. MII_RT_RXCFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2004h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2004h

Figure 14-3737. MII_RT_RXCFG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						RX_EOF_SCLR_DIS1	RX_ERR_RAW1
R-0h						R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_SFD_RAW1	RX_AUTO_FWD_PRE1	RX_BYTE_SWAP1	RX_L2_EN1	RX_MUX_SEL1	RX_CUT_PREAMBLE1	RX_DATA_RDY_MODE_DIS1	RX_ENABLE1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11298. MII_RT_RXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	
9	RX_EOF_SCLR_DIS1	R/W	0h	0h = RX_EOF flag in R31 and RXL2 is self cleared by HW when RX2L is enabled 1h = RX_EOF flag in R31 and RXL2 is not self cleared by HW when RX2L is enabled. A RX_EOF_CLR must get issued
8	RX_ERR_RAW1	R/W	0h	0h = ERR Raw Mode Disabled RX_ERR qualified with RX_DV RX_DV must be 1 before RX_ERR action/event is generated 1h = ERR Raw Mode Enabled RX_ERR is not qualified with RX_DV RX_ERR action/event is generated , even if RX_DV = 0
7	RX_SFD_RAW1	R/W	0h	0h = SFD Raw Mode Disabled RX_SFD requires a pattern of 5D 1h = SFD Raw Mode Enable The first byte of any pattern after RX_DV assertion will trigger RX_SFD event. The first nibble of the frame(RX_DV = 1) will be in the RX FIFO

Table 14-11298. MII_RT_RXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RX_AUTO_FWD_PRE1	R/W	0h	Auto Forward Preamble Mode 0h = Disable 1h = Enable If Enabled, RX_CUT_PREAMBLE and TX_AUTO_PREAMBLE must be disabled This will forward the preamble nibbles including the SFD to the TX FIFO that is attached to the PRU. First data byte seen by PRU R31 and/or RX L2 is DA Note: Odd number of preamble nibbles is supported in this mode. For example, 0x55D Note that new RX should only occur after the current TX completes
5	RX_BYTE_SWAP1	R/W	0h	Controls the order of the Byte0/1 placement for RX R31 and RX L2. 0h = Byte1 is the high byte for R31 and RX L2 MSB {Byte1:Byte0} LSB RX R31 15:8 = Byte1 RX R31 7:0 = Byte0 1h = Byte1 is the low byte for R31 and RX L2 MSB {Byte0:Byte1} LSB RX R31 15:8 = Byte0 RX R31 7:0 = Byte1 Must be selected /updated when the port is disabled or no traffic It only effects R31 and RX L2 order Note this cannot get enabled if TX_AUTO_SEQUENCE enabled since TX_BYTE_SWAP on swaps the PRU output.
4	RX_L2_EN1	R/W	0h	0h = Disables RX L2 buffer. Can be used as generic scratch pad. 1h = Enables RX L2 buffer
3	RX_MUX_SEL1	R/W	1h	0h = Select MII RX Data from Port 0 1h = Select MII RX Data from Port 1 The encoding is identical for both MII Ports and PRUs. Typically, the setting for this will not be identical for the two MII Receive Configuration registers.
2	RX_CUT_PREAMBLE1	R/W	0h	0h = All data from Ethernet PHY are passed on to PRU register. This assume Ethernet PHY which does not shorten the preamble 1h = MII interface suppresses preamble and sync frame delimiter. First data byte seen by PRU register is DA
1	RX_DATA_RDY_MODE_DIS1	R/W	0h	0h = R31:16 is DATA_RDY mapped 1h = R31:16 is TX_EOF mapped
0	RX_ENABLE1	R/W	0h	This enables RX traffic which is currently selected by RX_MUX_SELECT

3 MII_RT_TXCFG0 Register (Offset = 10h) [reset = X]

MII_RT_TXCFG0 is shown in Figure 14-3738 and described in Table 14-7563.

Return to Summary Table.

TX Control Register 0. This register contains the control information for the transmit path on one of the MII interfaces. MII_RT_TXCFG0 is attached to Port TX0 and controls which PRU core is selected for TX0.

Table 14-11299. MII_RT_TXCFG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2010h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2010h

Figure 14-3738. MII_RT_TXCFG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="3">TX_CLK_DELAY0</td><td colspan="2">RESERVED</td><td colspan="2">TX_START_DELAY0</td></tr>
<tr><td>R-0h</td><td colspan="3">R/W-0h</td><td colspan="2">R-0h</td><td colspan="2">R/W-40h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TX_START_DELAY0</td></tr>
<tr><td colspan="8">R/W-40h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>TX_IPG_WIRE_CLK_EN</td><td>TX_32_MODE_EN0</td><td>PRE_TX_AUTO_ESC_ERR0</td><td>PRE_TX_AUTO_SEQUENCE0</td><td>TX_MUX_SEL0</td></tr>
<tr><td colspan="4">R-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>TX_BYTE_SWAP0</td><td>TX_EN_MODE0</td><td>TX_AUTO_PREAMBLE0</td><td>TX_ENABLE0</td></tr>
<tr><td colspan="4">R-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11301. MII_RT_TXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	
30-28	TX_CLK_DELAY0	R/W	0h	Number of MII_RT clock cycles to wait before launching data on the MII interface. This can be tweaked to meet setup/hold time requirements on the MII TXCLK. The range is one to seven cycles after the MII Transmit edge has been synchronized to MII_RT clock domain. For example TX_CLK_DELAY Delay (ns) 0h = (10-15) + SoC delay 1h = (15-20) + SoC delay <n> (<n>*5 +10/+15) + SoC delay Note that the switch event can get pushed into the next TXCLK cycle.
27-26	RESERVED	R	0h	

Table 14-11301. MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	TX_START_DELAY0	R/W	40h	The time interval after which transmit interface starts sending data to MII interface after receiving RXDV for the current frame. This is programmed in number of MII_RT clock cycles. Default should be to have 320ns of delay which is optimized for min latency at 16 bit processing. Counter is started with RXDV signal going active. Transmit interface stops sending data when no more data is written into transmit interface by PRU along with TX_EOF marker bit set. Uses core_clk Note: it will not start until the TX FIFO is not empty. This delay only defines the minimum delay. If the TX FIFO has data when the delay expires, then TX will start sending data. If the TX FIFO is empty, it will not start until it is not empty. If TX_AUTO_PREAMBLE is enabled, TX FIFO will not get preamble until the first wrt occurs. Note: the TX FIFO size is 64Bytes. It is possible to overflow the TX FIFO with the max delay setting when auto forwarding is enabled since the time delay is larger than the amount of data it needs to store. If TX OVERFLOW occurs, then SW will need to issue a TX_RESET to reset the TX FIFO. The total delay is 64Byte times, but you need to allow delays for synchronization. Due to this fact; a MAX delay should be 80ns less when auto forwarding is enabled. 0x3F0 is the max in this configuration This register is also used in RGMII mode. For 1 Gbit rate the RGMII_CLK used is 250 MHz and the values in TX_START_DELAY0/1 register is multiplied by 4 ns. At 1 Gbit rate there is a min setting of 0xf which means 60 ns. The measured RGMII to RGMII delay is 160 ns with this settings. Additional delay comes from L0 FIFOs.
15-13	RESERVED	R	0h	
12	TX_IPG_WIRE_CLK_EN	R/W	0h	0h = Use ICSSGn_CORE_CLK (where n = 0 to 1) core clock for the TX_IPG counter 1h = Use the TX interface clock for the TX_IPG counter Note: Using TX interface clock the user should see zero jitter as long as the data is ready to transmit.MUST BE SET THE SAME FOR BOTH PORTS
11	TX_32_MODE_EN0	R/W	0h	0h = Disable 32-bit Data Push mode 1h = Enabled 32-bit, 16-bit, and 8-bit Data Push mode with TX_MASK disabled In this mode, the internal PRU R30 byte write strobes are used and NOT the R31 CMD TX_PUSH Any update to R30 will trigger an TX PUSH See TX_PUSH Table
10	PRE_TX_AUTO_ESC_ERR0	R/W	0h	This bit enables the HW actions required to implement the ESC Error handing table.

Table 14-11301. MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PRE_TX_AUTO_SEQUENCE0	R/W	0h	When set to one, it enables automated sequencing of transmit state machine based on events on receiver path that is connected to the respective transmitter. The transmit data source is determined by TX_MUX_SEL setting. When this bit is set, the masking logic that allows for a Boolean combination of PRU or MII data to be transmitted is disabled and only the MII data is used.
8	TX_MUX_SEL0	R/W	1h	0h = TX data from PRU0 is selected 1h = TX data from PRU1 is selected The default/reset setting for TX Port 0 is 1h. This setting permits MII TX Port 0 to receive data from PRU1 and the MII RX Port 1 which is connected to PRU1 by default. For MII TX Port 1, the default is zero which allows it to receive data from PRU0 and MII0 that is connected to PRU0 by default.
7-4	RESERVED	R	0h	
3	TX_BYTE_SWAP0	R/W	0h	Controls the order of the Byte0/1 placement for TX R30. 0h = Byte1 is the high byte for R30 MSB {Byte1:Byte0} LSB TX R30 15:8 = Byte1 TX R30 7:0 = Byte0 TX R30 31:24 = TX_MASK[15:8] TX R30 23:16 = TX_MASK[7:0] 1h = Byte1 is the low byte for R30 MSB {Byte0:Byte1} LSB TX R30 15:8 = Byte0 TX R30 7:0 = Byte1 TX R30 31:24 = TX_MASK[7:0] TX R30 23:16 = TX_MASK[15:8] Must be selected/updated when the port is disabled or no traffic It only effects R30 pulling order
2	TX_EN_MODE0	R/W	0h	0h = Disables TX_ENABLE self clear for a TX_EOF event iep_cmp[3] for TX0 and iep_cmp[4] for TX1 1h = Enables TX_ENABLE self clr for a TX_EOF event iep_cmp[3] for TX0 and iep_cmp[4] for TX1 Note when enabled, iep_cmp[3] must be set before the TX will start for TX0, and iep_cmp[4] for TX1 This is just a new dependency to start transmission to the current set of dependencies, which are FIFO NOT empty and TX_START_DELAY met.
1	TX_AUTO_PREAMBLE0	R/W	0h	0h = PRU will provide full pre-amble 1h = TX FIFO will insert pre-amble automatically Note that the TX FIFO does not get preloaded with the preamble until the first write occurs. This can cause the latency to be larger the min latency.

Table 14-11301. MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TX_ENABLE0	R/W	0h	0h = TX PORT is disabled/stopped immediately 1h = TX PORT is enabled and the frame will start once the IPG counter expired and TX Start Delay counter has expired When read value is zero, TX is disabled When read value is one, TX is enabled If TX_EN_MODE is set then TX_ENABLE will self clear during a TX_EOF event Note: SW can use this to pre-fill the TX FIFO and then start the TX Frame during none ECS operations.

4 MII_RT_TXCFG1 Register (Offset = 14h) [reset = X]

MII_RT_TXCFG1 is shown in Figure 14-3739 and described in Table 14-7565.

Return to Summary Table.

TX Control Register 1. This register contains the control information for the transmit path on one of the MII interfaces. MII_RT_TXCFG1 is attached to Port TX1 and controls which PRU core is selected for TX1.

Table 14-11302. MII_RT_TXCFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2014h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2014h

Figure 14-3739. MII_RT_TXCFG1 Register

31	30	29	28	27	26	25	24
RESERVED	TX_CLK_DELAY1			RESERVED		TX_START_DELAY1	
R-0h	R/W-0h			R-0h		R/W-40h	

23	22	21	20	19	18	17	16
TX_START_DELAY1							
R/W-40h							

15	14	13	12	11	10	9	8
RESERVED			TX_IPG_WIRE_CLK_EN	TX_32_MODE_EN1	PRE_TX_AUTO_ESC_ERR1	PRE_TX_AUTO_SEQUENCE1	TX_MUX_SEL1
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
RESERVED				TX_BYTE_SWAP1	TX_EN_MODE1	TX_AUTO_PREAMBLE1	TX_ENABLE1
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11304. MII_RT_TXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	

Table 14-11304. MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30-28	TX_CLK_DELAY1	R/W	0h	Number of MII_RT clock cycles to wait before launching data on the MII interface. This can be tweaked to meet setup/hold time requirements on the MII TXCLK. The range is one to seven cycles after the MII Transmit edge has been synchronized to MII_RT clock domain. For example TX_CLK_DELAY Delay (ns) 0h = (10-15) + SOC delay 1h = (15-20) + SOC delay <n> (<n>*5 +10/+15) + SOC delay Note that the switch event can get pushed into the next TXCLK cycle. Note: In order to guarantee the MII_G_RT I/O timing values published in the device data sheet, the PRU_ICSSG ICSSGn_CORE_CLK (where n = 0 to 2) core clock must be configured for 200 MHz, 225 MHz or 250 MHz and the TX_CLK_DELAY0 bit field in the MII_RT_TXCFG0 register must be set to 0h (default value).
27-26	RESERVED	R	0h	

Table 14-11304. MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	TX_START_DELAY1	R/W	40h	The time interval after which transmit interface starts sending data to MII interface after receiving RXDV for the current frame. This is programmed in number of MII_RT clock cycles. Default should be to have 320 ns of delay which is optimized for min latency at 16 bit processing. Counter is started with RXDV signal going active. Transmit interface stops sending data when no more data is written into transmit interface by PRU along with TX_EOF marker bit set. Uses core_clk Note it will not start until the TX FIFO is not empty. This delay only defines the minimum delay. If the TX FIFO has data when the delay expires, then TX will start sending data. If the TX FIFO is empty, it will not start until it is not empty. If TX_AUTO_PREAMBLE is enabled, TX FIFO will not get preamble until the first wrt occurs. Note the TX FIFO size is 64 Bytes. It is possible to overflow the TX FIFO with the max delay setting when auto forwarding is enabled since the time delay is larger than the amount of data it needs to store. If TX OVERFLOW occurs, then SW will need to issue a TX_RESET to reset the TX FIFO. The total delay is 64 Byte times, but you need to allow delays for synchronization. Do to this fact; a MAX delay should be 80 ns less when auto forwarding is enabled. 0x3F0 is the max in this configuration This register is also used in RGMII mode. For 1 Gbit rate the RGMII_CLK used is 250 MHz and the values in TX_START_DELAY0/1 register is multiplied by 4 ns. At 1 Gbit rate there is a min setting of 0xf which means 60 ns. The measured RGMII to RGMII delay is 160 ns with this settings. Additional delay comes from L0 FIFOs.
15-13	RESERVED	R	0h	
12	TX_IPG_WIRE_CLK_EN	R/W	0h	0h = Use ICSSGn_CORE_CLK (where n = 0 to 1) core clock for the TX_IPG counter 1h = Use the TX interface clock for the TX_IPG counter Note: Using TX interface clock the user should see zero jitter as long as the data is ready to transmit.MUST BE SET THE SAME FOR BOTH PORTS
11	TX_32_MODE_EN1	R/W	0h	0h = Disable 32-bit Data Push mode 1h = Enabled 32-bit, 16-bit, and 8 Data Push mode with TX_MASK disabled In this mode, the internal PRU R30 byte write strobes are used and NOT the R31 CMD TX_PUSH Any update to R30 will trigger an TX PUSH See TX_PUSH Table
10	PRE_TX_AUTO_ESC_ERR1	R/W	0h	This bit enables the HW actions required to implement the ESC Error handing table.

Table 14-11304. MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PRE_TX_AUTO_SEQUENCE1	R/W	0h	When set to one, it enables automated sequencing of transmit state machine based on events on receiver path that is connected to the respective transmitter. The transmit data source is determined by TX_MUX_SEL setting. When this bit is set, the masking logic that allows for a Boolean combination of PRU or MII data to be transmitted is disabled and only the MII data is used.
8	TX_MUX_SEL1	R/W	0h	0h = TX data from PRU0 is selected 1h = TX data from PRU1 is selected The default/reset setting for TX Port 0 is 1. This setting permits MII TX Port 0 to receive data from PRU1 and the MII RX Port 1 which is connected to PRU1 by default. For MII TX Port 1, the default is zero which allows it to receive data from PRU0 and MII0 that is connected to PRU0 by default.
7-4	RESERVED	R	0h	
3	TX_BYTE_SWAP1	R/W	0h	Controls the order of the Byte0/1 placement for TX R30. 0h = Byte1 is the high byte for R30 MSB {Byte1:Byte0} LSB TX R30 15:8 = Byte1 TX R30 7:0 = Byte0 TX R30 31:24 = TX_MASK[15:8] TX R30 23:16 = TX_MASK[7:0] 1h = Byte1 is the low byte for R30 MSB {Byte0:Byte1} LSB TX R30 15:8 = Byte0 TX R30 7:0 = Byte1 TX R30 31:24 = TX_MASK[7:0] TX R30 23:16 = TX_MASK[15:8] Must be selected /updated when the port is disabled or no traffic It only effects R30 pulling order
2	TX_EN_MODE1	R/W	0h	0h = Disables TX_ENABLE self clr for a TX_EOF event iep_cmp[3] for TX0 and iep_cmp[4] for TX1 1h = Enables TX_ENABLE self clr for a TX_EOF event iep_cmp[3] for TX0 and iep_cmp[4] for TX1 Note when enabled, iep_cmp[3] must be set before the TX will start for TX0, and iep_cmp[4] for TX1 This is just a new dependency to start transmission to the current set of dependencies, which are FIFO NOT empty and TX_START_DELAY met.
1	TX_AUTO_PREAMBLE1	R/W	0h	0h = PRU will provide full pre-amble 1h = TX FIFO will insert pre-amble automatically Note that the TX FIFO does not get preloaded with the preamble until the first write occurs. This can cause the latency to be larger the min latency.

Table 14-11304. MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TX_ENABLE1	R/W	0h	0h = TX PORT is disabled/stopped immediately 1h = TX PORT is enabled and the frame will start once the IPG counter expired and TX Start Delay counter has expired When read value is zero, TX is disabled When read value is one, TX is enabled If TX_EN_MODE is set then TX_ENABLE will self clear during a TX_EOF event Note SW can use this to pre-fill the TX FIFO and then start the TX Frame during none ECS operations.

5 MII_RT_TX_CRC0 Register (Offset = 20h) [reset = 0h]

MII_RT_TX_CRC0 is shown in Figure 14-3740 and described in Table 14-7567.

Return to Summary Table.

Transmit CRC32 Register 0. It contains CRC which PRU core can read.

Table 14-11305. MII_RT_TX_CRC0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2020h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2020h

Figure 14-3740. MII_RT_TX_CRC0 Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">TX_CRC0</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11307. MII_RT_TX_CRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CRC0	R	0h	FCS (CRC32) data can be read by PRU core for diagnostics It is only valid after 6 clocks after a TX_CRC_HIGH command is given.

6 MII_RT_TX_CRC1 Register (Offset = 24h) [reset = 0h]

MII_RT_TX_CRC1 is shown in Figure 14-3741 and described in Table 14-7569.

Return to Summary Table.

Transmit CRC32 Register 1. It contains CRC which PRU core can read.

Table 14-11308. MII_RT_TX_CRC1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2024h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2024h

Figure 14-3741. MII_RT_TX_CRC1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TX_CRC1</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11310. MII_RT_TX_CRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CRC1	R	0h	FCS (CRC32) data can be read by PRU for diagnostics It is only valid after 6 clocks after a TX_CRC_HIGH command is given.

7 MII_RT_TX_IPG0 Register (Offset = 30h) [reset = X]

MII_RT_TX_IPG0 is shown in Figure 14-3742 and described in Table 14-7571.

Return to Summary Table.

TX IPG Register 0.

Table 14-11311. MII_RT_TX_IPG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2030h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2030h

Figure 14-3742. MII_RT_TX_IPG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="22">RESERVED</td><td colspan="10">TX_IPG0</td></tr>
<tr><td colspan="22">R-0h</td><td colspan="10">R/W-28h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11313. MII_RT_TX_IPG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	TX_IPG0	R/W	28h	Define the minimum Inter Packet Gap. When MII_RT_TXCFG0[12] TX_IPG_WIRE_CLK_EN = 0h. This defines the minimum of ICSSGn_CORE_CLK (4 ns/5 ns) cycles between the de-assertion of TX_EN and the assertion of TX_EN. The start of the TX will get delayed when the incoming packet IPG is less than defined minimum. In general, software should program in increments of 8, 40 ns to insure the extra delays takes effect. When TX_IPG_WIRE_CLK_EN = 1h. This defines the minimum of TX interface clock cycles between the end of a frame and the start of a new frame 0h = 1 TX interface clock 3h = 4 TX interface clocks (96 ns for 1G) <n> = <n> +1 TX interface clocks expect for in SGMII 100M mode Note: In SGMII 100M mode, it will be <n> = <n> +5 TX interface clocks When software does an update, it takes 4 SGMII/RGMII/MII TX_CLKs before it goes into effect Min Values: MII >= 10 RGMII/SGMII 1G >= 11 (8 ns period) RGMII 100M >= 8 (40 ns period) SGMII 100M >= 24 (8 ns period) If the user violate, will get a jitter. The root cause most likely is that the data is not ready. TX MII Odd Nibble is NOT supported in this mode.

8 MII_RT_TX_IPG1 Register (Offset = 34h) [reset = X]

MII_RT_TX_IPG1 is shown in Figure 14-3743 and described in Table 14-7573.

Return to Summary Table.

TX IPG Register 1.

Table 14-11314. MII_RT_TX_IPG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2034h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2034h

Figure 14-3743. MII_RT_TX_IPG1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_IPG1</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-28h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11316. MII_RT_TX_IPG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_IPG1	R/W	28h	Define the minimum Inter Packet Gap. When MII_RT_TXCFG0[12] TX_IPG_WIRE_CLK_EN = 0h. This defines the minimum of ICSSGn_CORE_CLK (4 ns/5 ns) cycles between the de-assertion of TX_EN and the assertion of TX_EN. The start of the TX will get delayed when the incoming packet IPG is less than defined minimum. In general, software should program in increments of 8, 40 ns to insure the extra delays takes effect. When TX_IPG_WIRE_CLK_EN = 1h. This defines the minimum of TX interface clock cycles between the end of a frame and the start of a new frame 0h = 1 TX interface clock 3h = 4 TX interface clocks (96 ns for 1G) <n> = <n> +1 TX interface clocks expect for in SGMII 100M mode Note: In SGMII 100M mode, it will be <n> = <n> +5 TX interface clocks When software does an update, it takes 4 SGMII/RGMII/MII TX_CLKs before it goes into effect Min Values: MII >= 10 RGMII/SGMII 1G >= 11 (8 ns period) RGMII 100M >= 8 (40 ns period) SGMII 100M >= 24 (8 ns period) If the user violate, will get a jitter. The root cause most likely is that the data is not ready. TX MII Odd Nibble is NOT supported in this mode.

9 MII_RT_PRS0 Register (Offset = 38h) [reset = X]

MII_RT_PRS0 is shown in Figure 14-3744 and described in Table 14-7575.

Return to Summary Table.

PORT_RAW_STATUS Register 0.

Table 14-11317. MII_RT_PRS0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2038h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2038h

Figure 14-3744. MII_RT_PRS0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						SYNC_MII0_CRS	SYNC_MII0_COL
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11319. MII_RT_PRS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1	SYNC_MII0_CRS	R	0h	Read the current state of PR1_MII0_CRS
0	SYNC_MII0_COL	R	0h	Read the current state of PR1_MII0_COL

10 MII_RT_PRS1 Register (Offset = 3Ch) [reset = X]

MII_RT_PRS1 is shown in Figure 14-3745 and described in Table 14-7577.

Return to Summary Table.

PORT_RAW_STATUS Register 1.

Table 14-11320. MII_RT_PRS1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 203Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 203Ch

Figure 14-3745. MII_RT_PRS1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						SYNC_MII1_CRS	SYNC_MII1_COL
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11322. MII_RT_PRS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1	SYNC_MII1_CRS	R	0h	Read the current state of PR1_MII1_CRS
0	SYNC_MII1_COL	R	0h	Read the current state of PR1_MII1_COL

11 MII_RT_RX_FRMS0 Register (Offset = 40h) [reset = 05F1003Fh]

MII_RT_RX_FRMS0 is shown in Figure 14-3746 and described in Table 14-7579.

Return to Summary Table.

RX Frame Size Register 0.

Table 14-11323. MII_RT_RX_FRMS0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2040h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2040h

Figure 14-3746. MII_RT_RX_FRMS0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_FRM0																RX_MIN_FRM0															
R/W-5F1h																R/W-3Fh															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11325. MII_RT_RX_FRMS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MAX_FRM0	R/W	5F1h	If the FRAME total byte count is more than defined value, RX_MAX_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC Notes if the incoming frame is truncated at the marker. So, RX CRC and RX ODD NIBBLE will not get asserted. If the PRU is moving the data the TX frame size will be aligned to the size of the push. For example push32, mod 4 bytes example push16, mod 2 bytes so, software should set the RX_MAX_FRM_CNT in this mode to align with the max push size. The event is always byte aligned. The final TX size is aligned to the push size.
15-0	RX_MIN_FRM0	R/W	3Fh	If the FRAME total byte count is less than defined value, RX_MIN_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC Notes: If the PRU is moving the data the TX frame size will be aligned to the size of the push. For example push32, mod 4 bytes example push16, mod 2 bytes so, software should set the RX_MIN_FRM_CNT in this mode to align with the max push size. The event is always byte aligned. The final TX size is aligned to the push size

12 MII_RT_RX_FRMS1 Register (Offset = 44h) [reset = 05F1003Fh]

MII_RT_RX_FRMS1 is shown in Figure 14-3747 and described in Table 14-7581.

Return to Summary Table.

RX Frame Size Register 1.

Table 14-11326. MII_RT_RX_FRMS1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2044h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2044h

Figure 14-3747. MII_RT_RX_FRMS1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_FRM1																RX_MIN_FRM1															
R/W-5F1h																R/W-3Fh															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11328. MII_RT_RX_FRMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MAX_FRM1	R/W	5F1h	If the FRAME total byte count is more than defined value, RX_MAX_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC Notes if the incoming frame is truncated at the marker. So, RX CRC and RX ODD NIBBLE will not get asserted. If the PRU is moving the data the TX frame size will be aligned to the size of the push. For example push32, mod 4 bytes example push16, mod 2 bytes so, software should set the RX_MAX_FRM_CNT in this mode to align with the max push size. The event is always byte aligned. The final TX size is aligned to the push size.
15-0	RX_MIN_FRM1	R/W	3Fh	If the FRAME total byte count is less than defined value, RX_MIN_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC Notes: If the PRU is moving the data the TX frame size will be aligned to the size of the push. For example push32, mod 4 bytes example push16, mod 2 bytes so, software should set the RX_MIN_FRM_CNT in this mode to align with the max push size. The event is always byte aligned. The final TX size is aligned to the push size

13 MII_RT_RX_PCNT0 Register (Offset = 48h) [reset = X]

MII_RT_RX_PCNT0 is shown in Figure 14-3748 and described in Table 14-7583.

Return to Summary Table.

RX Preamble Cnt Register 0.

Table 14-11329. MII_RT_RX_PCNT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2048h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2048h

Figure 14-3748. MII_RT_RX_PCNT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td colspan="5">RX_MAX_PCNT0</td><td colspan="4">RX_MIN_PCNT0</td></tr>
<tr><td colspan="7">R-0h</td><td colspan="5">R/W-Eh</td><td colspan="4">R/W-1h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11331. MII_RT_RX_PCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8-4	RX_MAX_PCNT0	R/W	Eh	Define the max number of nibbles until first SFD/SMD is matched. RX_MAX_PRE_COUNT_ERR will set if the preamble count more than 0h= Disabled 1h = Reserved 2h = 4th nibble needs to have built 0xD5/SMD Eh= 16th nibble needs to have built 0xD5/SMD if not matched then 16th nibble will cause the error to assert and truncate the incoming frame. Note the 16th nibble is transmitted Any valid IET SMD or 0xD5 If > max then, hardware will issue a SFD and set error flags CRC can/will be bad for this packet
3-0	RX_MIN_PCNT0	R/W	1h	Define the minimum number of nibbles before SFD 0xD5 RX_MIN_PRE_COUNT_ERR will set if the preamble count less than 0h = is Disabled 1h = Minimum of 1 0x5 before 0xD5 2h = Minimum of 2 0x5 before 0xD5 <n> minimum of <n> 0x5 before 0xD5 Note it does not need to be “0x5”

14 MII_RT_RX_PCNT1 Register (Offset = 4Ch) [reset = X]

MII_RT_RX_PCNT1 is shown in Figure 14-3749 and described in Table 14-7585.

Return to Summary Table.

RX Preamble Cnt Register 1.

Table 14-11332. MII_RT_RX_PCNT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 204Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 204Ch

Figure 14-3749. MII_RT_RX_PCNT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							RX_MAX_PCNT1					RX_MIN_PCNT1			
R-0h							R/W-Eh					R/W-1h			

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11334. MII_RT_RX_PCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8-4	RX_MAX_PCNT1	R/W	Eh	Define the max number of nibbles until first SFD/SMD is matched. RX_MAX_PRE_COUNT_ERR will set if the preamble count more than 0h = Disabled 1h = Reserved 2h = 4th nibble needs to have built 0xD5/SMD Eh= 16th nibble needs to have built 0xD5/SMD if not matched then 16th nibble will cause the error to assert and truncate the incoming frame. Note the 16th nibble is transmitted Any valid IET SMD or 0xD5 If > max then, hardware will issue a SFD and set error flags CRC can/will be bad for this packet
3-0	RX_MIN_PCNT1	R/W	1h	Define the minimum number of nibbles before SFD 0xD5 RX_MIN_PRE_COUNT_ERR will set if the preamble count less than 0h = is Disabled 1h = Minimum of 1 0x5 before 0xD5 2h = Minimum of 2 0x5 before 0xD5 <n> minimum of <n> 0x5 before 0xD5 Note it does not need to be “0x5”

15 MII_RT_RX_ERR0 Register (Offset = 50h) [reset = X]

MII_RT_RX_ERR0 is shown in Figure 14-3750 and described in Table 14-7587.

Return to Summary Table.

RX Error Register 0.

Table 14-11335. MII_RT_RX_ERR0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2050h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2050h

Figure 14-3750. MII_RT_RX_ERR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RX_MAX_FRM_ERR0	RX_MIN_FRM_ERR0	RX_MAX_PCNT_ERR0	RX_MIN_PCNT_ERR0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11337. MII_RT_RX_ERR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	RX_MAX_FRM_ERR0	R/W	0h	Set when the FRAME total byte count is more than defined value. Write 1 to Clear
2	RX_MIN_FRM_ERR0	R/W	0h	Set when the FRAME total byte count is less than defined value. Write 1 to Clear
1	RX_MAX_PCNT_ERR0	R/W	0h	Set when of x nibbles before SFD 0xD5 is more than defined value. Write 1 to Clear
0	RX_MIN_PCNT_ERR0	R/W	0h	Set when of 0x5 before SFD 0xD5 is less than defined value. Write 1 to Clear

16 MII_RT_RX_ERR1 Register (Offset = 54h) [reset = X]

MII_RT_RX_ERR1 is shown in Figure 14-3751 and described in Table 14-7589.

Return to Summary Table.

RX Error Register 1.

Table 14-11338. MII_RT_RX_ERR1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2054h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2054h

Figure 14-3751. MII_RT_RX_ERR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RX_MAX_FRM_ERR1	RX_MIN_FRM_ERR1	RX_MAX_PCNT_ERR1	RX_MIN_PCNT_ERR1
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11340. MII_RT_RX_ERR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	RX_MAX_FRM_ERR1	R/W	0h	Set when the FRAME total byte count is more than defined value. Write 1 to Clear
2	RX_MIN_FRM_ERR1	R/W	0h	Set when the FRAME total byte count is less than defined value. Write 1 to Clear
1	RX_MAX_PCNT_ERR1	R/W	0h	Set when of x nibbles before SFD 0xD5 is more than defined value. Write 1 to Clear
0	RX_MIN_PCNT_ERR1	R/W	0h	Set when of 0x5 before SFD 0xD5 is less than defined value. Write 1 to Clear

17 MII_RT_RX_FIFO_LEVEL0 Register (Offset = 60h) [reset = X]

MII_RT_RX_FIFO_LEVEL0 is shown in Figure 14-3752 and described in Table 14-7591.

Return to Summary Table.

RX FIFO Level 0 Register.

Table 14-11341. MII_RT_RX_FIFO_LEVEL0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2060h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2060h

Figure 14-3752. MII_RT_RX_FIFO_LEVEL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_LEVEL0							
R-0h								R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11343. MII_RT_RX_FIFO_LEVEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RX_FIFO_LEVEL0	R	0h	Define the number of valid bytes in the RX FIFO. 0h = Empty 1h = 1 Byte/ 2 Nibbles 2h = 2 Byte/ 4 Nibble ... 20h = 32 Bytes/ 64 Nibbles

18 MII_RT_RX_FIFO_LEVEL1 Register (Offset = 64h) [reset = X]

MII_RT_RX_FIFO_LEVEL1 is shown in Figure 14-3753 and described in Table 14-7593.

Return to Summary Table.

RX FIFO Level 1 Register.

Table 14-11344. MII_RT_RX_FIFO_LEVEL1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2064h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2064h

Figure 14-3753. MII_RT_RX_FIFO_LEVEL1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">RX_FIFO_LEVEL1</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11346. MII_RT_RX_FIFO_LEVEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RX_FIFO_LEVEL1	R	0h	Define the number of valid bytes in the RX FIFO. 0h = Empty 1h = 1 Byte/ 2 Nibbles 2h = 2 Byte/ 4 Nibble ... 20h = 32 Bytes/ 64 Nibbles

19 MII_RT_TX_FIFO_LEVEL0 Register (Offset = 68h) [reset = X]

MII_RT_TX_FIFO_LEVEL0 is shown in Figure 14-3754 and described in Table 14-7595.

Return to Summary Table.

TX FIFO Register 0.

Table 14-11347. MII_RT_TX_FIFO_LEVEL0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 2068h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 2068h

Figure 14-3754. MII_RT_TX_FIFO_LEVEL0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">TX_FIFO_LEVEL0</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11349. MII_RT_TX_FIFO_LEVEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TX_FIFO_LEVEL0	R	0h	Define the number of valid nibbles in the TX FIFO. 0 = Empty 1 = 1 Nibble 2 = 1 Byte/ 2 Nibble ... 128 = 64 Bytes/ 128 Nibbles

20 MII_RT_TX_FIFO_LEVEL1 Register (Offset = 6Ch) [reset = X]

MII_RT_TX_FIFO_LEVEL1 is shown in Figure 14-3755 and described in Table 14-7597.

Return to Summary Table.

TX FIFO Register 1.

Table 14-11350. MII_RT_TX_FIFO_LEVEL1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	3003 206Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	300B 206Ch

Figure 14-3755. MII_RT_TX_FIFO_LEVEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_FIFO_LEVEL1							
R-X								R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11352. MII_RT_TX_FIFO_LEVEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TX_FIFO_LEVEL1	R	0h	Define the number of valid nibbles in the TX FIFO. 0 = Empty 1 = 1 Nibble 2 = 1 Byte/ 2 Nibble ... 128 = 64 Bytes/ 128 Nibbles

14.3.6.1.28 PRU_MII_G_RT_MII_G_RT Registers

Table 14-7599 lists the memory-mapped registers for the PRU_MII_G_RT_MII_G_RT registers. All register offset addresses not listed in Table 14-7599 should be considered as reserved locations and the register contents should not be modified.

Table 14-11353. PRU_MII_G_RT_MII_G_RT Instances

Instance	Base Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3000h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3000h

Table 14-11354. PRU_MII_G_RT_MII_G_RT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
0h	MII_G_RT_ICSS_G_CFG	ICSSG Configuration Register	3003 3000h	300B 3000h
4h	MII_G_RT_RGMII_CFG	RGMII Configuration Register	3003 3004h	300B 3004h
8h	MII_G_RT_MAC_PRU0_0	PRU0 MAC (DA3:DA0)	3003 3008h	300B 3008h
Ch	MII_G_RT_MAC_PRU0_1	PRU0 MAC (DA5:DA4)	3003 300Ch	300B 300Ch
10h	MII_G_RT_MAC_PRU1_0	PRU1 MAC (DA3:DA0)	3003 3010h	300B 3010h
14h	MII_G_RT_MAC_PRU1_1	PRU0 MAC (DA5:DA4)	3003 3014h	300B 3014h
18h	MII_G_RT_MAC_INTERFACE_0	MAC Host Interface (DA3:DA0)	3003 3018h	300B 3018h
1Ch	MII_G_RT_MAC_INTERFACE_1	MAC Host Interface (DA5:DA4)	3003 301Ch	300B 301Ch
20h	MII_G_RT_PREEMPT_CFG	Preempt Configuration Register	3003 3020h	300B 3020h
24h	MII_G_RT_SMDT1S_CFG	SMD Type1S Preemptable Frame Start Configuration	3003 3024h	300B 3024h
28h	MII_G_RT_SMDT1C_CFG	SMD Type1C None Initial Frag Configuration	3003 3028h	300B 3028h
34h	MII_G_RT_FRAG_CNT_CFG	Frag Count Configuration	3003 3034h	300B 3034h
40h	MII_G_RT_PA_STAT_PUSH0	Pa Stat Push0	3003 3040h	300B 3040h
44h	MII_G_RT_PA_STAT_PUSH1	Pa Stat Push1	3003 3044h	300B 3044h
48h	MII_G_RT_PA_STAT_PUSH2	Pa Stat Push2	3003 3048h	300B 3048h
4Ch	MII_G_RT_PA_STAT_PUSH3	Pa Stat Push3	3003 304Ch	300B 304Ch
60h	MII_G_RT_FDB_GEN_CFG1	FDB Configuration1	3003 3060h	300B 3060h
64h	MII_G_RT_FDB_GEN_CFG2	FDB Configuration2	3003 3064h	300B 3064h
6Ch	MII_G_RT_FDB_DF_VLAN	FDB Default PRU VLAN	3003 306Ch	300B 306Ch
70h	MII_G_RT_FDB_HOST_DA0	FDB HOST DA3:0 Configuration	3003 3070h	300B 3070h
74h	MII_G_RT_FDB_HOST_DA1	FDB HOST DA5:4 Configuration	3003 3074h	300B 3074h
78h	MII_G_RT_FDB_HOST_SA0	FDB HOST SA3:0 Configuration	3003 3078h	300B 3078h
7Ch	MII_G_RT_FDB_HOST_VLAN_SA1	FDB HOST VLAN SA5:4 Configuration	3003 307Ch	300B 307Ch
80h	MII_G_RT_FT1_START_LEN_PRU0	Filter1 Start and Length (PRU0)	3003 3080h	300B 3080h
84h	MII_G_RT_FT1_CFG_PRU0	Filter1 Configuration (PRU0)	3003 3084h	300B 3084h
88h + formula	MII_G_RT_FT1_k_DA0_PRU0	Filter1<k> DA0 (PRU0)	3003 3088h + formula	300B 3088h + formula
8Ch + formula	MII_G_RT_FT1_k_DA1_PRU0	Filter1<k> DA1 (PRU0)	3003 308Ch + formula	300B 308Ch + formula
90h + formula	MII_G_RT_FT1_k_DA_MASK0_PRU0	Filter1<k> DA0 Mask (PRU0)	3003 3090h + formula	300B 3090h + formula

Table 14-11354. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
94h + formula	MII_G_RT_FT1_k_DA_MASK1_PRU0	Filter1<k> DA1 Mask (PRU0)	3003 3094h + formula	300B 3094h + formula
108h + formula	MII_G_RT_FT3_m_START_PRU0	Filter3 Byte Count Start for PRU0	3003 3108h + formula	300B 3108h + formula
10Ch + formula	MII_G_RT_FT3_m_START_AUTO_PRU0	Filter3 Byte Count Start for Auto Skip mode	3003 310Ch + formula	300B 310Ch + formula
110h + formula	MII_G_RT_FT3_m_START_LEN_PRU0	Filter3 Start Offset for PRU0	3003 3110h + formula	300B 3110h + formula
114h + formula	MII_G_RT_FT3_m_JMP_OFFSET_PRU0	Filter3 Jump Offset for PRU0for PRU0	3003 3114h + formula	300B 3114h + formula
118h + formula	MII_G_RT_FT3_m_LEN_PRU0	Filter3 Length Offset for PRU0	3003 3118h + formula	300B 3118h + formula
11Ch + formula	MII_G_RT_FT3_m_CFG_PRU0	Filter3 Configuration for PRU0	3003 311Ch + formula	300B 311Ch + formula
120h + formula	MII_G_RT_FT3_m_T_PRU0	Filter3 Type for PRU0	3003 3120h + formula	300B 3120h + formula
124h + formula	MII_G_RT_FT3_m_T_MASK_PRU0	Filter3 Mask for PRU0	3003 3124h + formula	300B 3124h + formula
308h + formula	MII_G_RT_FT3_m_P0_PRU0	Filter3 PRU0 (P4:P1)	3003 3308h + formula	300B 3308h + formula
30Ch + formula	MII_G_RT_FT3_m_P1_PRU0	Filter3 PRU0 (P8:P5)	3003 330Ch + formula	300B 330Ch + formula
310h + formula	MII_G_RT_FT3_n_P_MASK0_PRU0	Filter3 Mask0 (MP4:MP1)	3003 3310h + formula	300B 3310h + formula
314h + formula	MII_G_RT_FT3_n_P_MASK1_PRU0	Filter3 Mask1 (MP8:MP5)	3003 3314h + formula	300B 3314h + formula
408h	MII_G_RT_FT_RX_PTR_PRU0	RX Current Filter Byte Count (PRU0)	3003 3408h	300B 3408h
40Ch + formula	MII_G_RT_RX_CLASSm_AND_EN_PRU0	RX Class AND Enable Register	3003 340Ch + formula	300B 340Ch + formula
410h + formula	MII_G_RT_RX_CLASSm_OR_EN_PRU0	RX Class OR Enable Register	3003 3410h	300B 3410h
48Ch	MII_G_RT_RX_CLASS_CFG1_PRU0	RX Class Configuration 1 Register	3003 348Ch	300B 348Ch
490h	MII_G_RT_RX_CLASS_CFG2_PRU0	RX Class Configuration 2 Register	3003 3490h	300B 3490h
494h + formula	MII_G_RT_RX_CLASS_GATESm_PRU0	RX Class Gate Configuration PRU0 Register	3003 3494h + formula	300B 3494h + formula
4D4h	MII_G_RT_RX_GREEN_PRU0	RX Green Status PRU0	3003 34D4h	300B 34D4h
4D8h	MII_G_RT_SA_HASH_PRU0	SA Hash Seed PRU0	3003 34D8h	300B 34D8h
4DCh	MII_G_RT_CONN_HASH_PRU0	Connection Hash Seed PRU0	3003 34DCh	300B 34DCh
4E0h	MII_G_RT_CONN_HASH_START_PRU0	Connection Hash Start PRU0	3003 34E0h	300B 34E0h
4E4h + formula	MII_G_RT_RX_RATE_CFGn_PRU0	RX Rate Configuration Register	3003 34E4h + formula	300B 34E4h + formula
504h	MII_G_RT_RX_RATE_SRC_SEL0_PRU0	RX Rate Source Select0	3003 3504h	300B 3504h
508h	MII_G_RT_RX_RATE_SRC_SEL1_PRU0	RX Rate Source Select1	3003 3508h	300B 3508h
50Ch + formula	MII_G_RT_TX_RATE_CFG1_n_PRU0	TX Rate Configuration1 Register	3003 350Ch + formula	300B 350Ch + formula

Table 14-11354. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
510h + formula	MII_G_RT_TX_RATE_CFG2_n_PRU0	TX Rate Configuration2 Register	3003 3510h + formula	300B 3510h + formula
54Ch	MII_G_RT_RX_STAT_GOOD_PRU0	RX Good Frame Count (PRU0)	3003 354Ch	300B 354Ch
550h	MII_G_RT_RX_STAT_BC_PRU0	RX BC Frame Count (PRU0)	3003 3550h	300B 3550h
554h	MII_G_RT_RX_STAT_MC_PRU0	RX MC Frame Count (PRU0)	3003 3554h	300B 3554h
558h	MII_G_RT_RX_STAT_CRC_ERR_PRU0	RX CRC Error Frame Count (PRU0)	3003 3558h	300B 3558h
55Ch	MII_G_RT_RX_STAT_MII_ERR_PRU0	RX MII Error Frame Count (PRU0)	3003 355Ch	300B 355Ch
560h	MII_G_RT_RX_STAT_ODD_ERR_PRU0	RX Odd Nibble Frame Count (PRU0)	3003 3560h	300B 3560h
564h	MII_G_RT_RX_STAT_MAX_SIZE_PRU0	RX Max Size Frame Count (PRU0)	3003 3564h	300B 3564h
568h	MII_G_RT_RX_STAT_MAX_ERR_PRU0	RX Max Size Error Frame Count (PRU0)	3003 3568h	300B 3568h
56Ch	MII_G_RT_RX_STAT_MIN_SIZE_PRU0	RX Min Size Frame Count (PRU0)	3003 356Ch	300B 356Ch
570h	MII_G_RT_RX_STAT_MIN_ERR_PRU0	RX Min Size Error Frame Count (PRU0)	3003 3570h	300B 3570h
574h	MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0	RX Overrun Frame Count (PRU0)	3003 3574h	300B 3574h
578h + formula	MII_G_RT_RX_STAT_CLASSm_HIT_PRU0	RX Class<m> Hit	3003 3578h + formula	300B 3578h + formula
5B8h	MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0	RX SMD Frag Error Count (PRU0)	3003 35B8h	300B 35B8h
5BCh	MII_G_RT_RX_STAT_BKT1_SIZE_PRU0	RX Bucket1 Size Configuration (PRU0)	3003 35BCh	300B 35BCh
5C0h	MII_G_RT_RX_STAT_BKT2_SIZE_PRU0	RX Bucket2 Size Configuration (PRU0)	3003 35C0h	300B 35C0h
5C4h	MII_G_RT_RX_STAT_BKT3_SIZE_PRU0	RX Bucket3 Size Configuration (PRU0)	3003 35C4h	300B 35C4h
5C8h	MII_G_RT_RX_STAT_BKT4_SIZE_PRU0	RX Bucket4 Size Configuration (PRU0)	3003 35C8h	300B 35C8h
5CCh	MII_G_RT_RX_STAT_64_PRU0	RX 64B Sized Frame Count (PRU0)	3003 35CCh	300B 35CCh
5D0h	MII_G_RT_RX_STAT_BKT1_PRU0	RX Bucket1 Sized Frame Count (PRU0)	3003 35D0h	300B 35D0h
5D4h	MII_G_RT_RX_STAT_BKT2_PRU0	RX Bucket2 Sized Frame Count (PRU0)	3003 35D4h	300B 35D4h
5D8h	MII_G_RT_RX_STAT_BKT3_PRU0	RX Bucket3 Sized Frame Count (PRU0)	3003 35D8h	300B 35D8h
5DCh	MII_G_RT_RX_STAT_BKT4_PRU0	RX Bucket4 Sized Frame Count (PRU0)	3003 35DCh	300B 35DCh
5E0h	MII_G_RT_RX_STAT_BKT5_PRU0	RX Bucket5 Sized Frame Count (PRU0)	3003 35E0h	300B 35E0h
5E4h	MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0	RX Total Byte Count (PRU0)	3003 35E4h	300B 35E4h
5E8h	MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0	RX TX Total Byte Count (PRU0)	3003 35E8h	300B 35E8h
5ECh	MII_G_RT_TX_STAT_GOOD_PORT0	TX Good Frame Count Port0	3003 35ECh	300B 35ECh

Table 14-11354. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
5F0h	MII_G_RT_TX_STAT_BC_PORT0	TX BC Frame Count Port0	3003 35F0h	300B 35F0h
5F4h	MII_G_RT_TX_STAT_MC_PORT0	TX MC Frame Count Port0	3003 35F4h	300B 35F4h
5F8h	MII_G_RT_TX_STAT_ODD_ERR_PORT0	TX Odd Nibble Frame Count Port0	3003 35F8h	300B 35F8h
5FCh	MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0	TX Under Flow Error Count Port0	3003 35FCh	300B 35FCh
600h	MII_G_RT_TX_STAT_MAX_SIZE_PORT0	TX Max Size Frame Port0	3003 3600h	300B 3600h
604h	MII_G_RT_TX_STAT_MAX_ERR_PORT0	TX Max Size Error Frame Count Port0	3003 3604h	300B 3604h
608h	MII_G_RT_TX_STAT_MIN_SIZE_PORT0	TX Min Size Frame Port0	3003 3608h	300B 3608h
60Ch	MII_G_RT_TX_STAT_MIN_ERR_PORT0	TX Min Size ErrorFrame Count Port0	3003 360Ch	300B 360Ch
610h	MII_G_RT_TX_STAT_BKT1_SIZE_PORT0	TX Bucket1 Size Configuration Port0	3003 3610h	300B 3610h
614h	MII_G_RT_TX_STAT_BKT2_SIZE_PORT0	TX Bucket2 Size Configuration Port0	3003 3614h	300B 3614h
618h	MII_G_RT_TX_STAT_BKT3_SIZE_PORT0	TX Bucket3 Size Configuration Port0	3003 3618h	300B 3618h
61Ch	MII_G_RT_TX_STAT_BKT4_SIZE_PORT0	TX Bucket4 Size Configuration Port0	3003 361Ch	300B 361Ch
620h	MII_G_RT_TX_STAT_64_PORT0	TX 64B Sized Frame Count Port0	3003 3620h	300B 3620h
624h	MII_G_RT_TX_STAT_BKT1_PORT0	TX Bucket1 Sized Frame Count Port0	3003 3624h	300B 3624h
628h	MII_G_RT_TX_STAT_BKT2_PORT0	TX Bucket2 Sized Frame Count Port0	3003 3628h	300B 3628h
62Ch	MII_G_RT_TX_STAT_BKT3_PORT0	TX Bucket3 Sized Frame Count Port0	3003 362Ch	300B 362Ch
630h	MII_G_RT_TX_STAT_BKT4_PORT0	TX Bucket4 Sized Frame Count Port0	3003 3630h	300B 3630h
634h	MII_G_RT_TX_STAT_BKT5_PORT0	TX Bucket5 Sized Frame Count Port0	3003 3634h	300B 3634h
638h	MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0	TX Total Byte Count Port0	3003 3638h	300B 3638h
63Ch	MII_G_RT_TX_HSR_TAG_PORT0	TX HSR TAG Port0	3003 363Ch	300B 363Ch
640h	MII_G_RT_TX_HSR_SEQ_PORT0	TX HSR Seq Port0	3003 3640h	300B 3640h
644h	MII_G_RT_TX_VLAN_TYPE_TAG_PORT0	TX VLAN Type TAG Port0	3003 3644h	300B 3644h
648h	MII_G_RT_TX_VLAN_INS_TAG_PORT0	TX VLAN Insertion TAG Port0	3003 3648h	300B 3648h
64Ch	MII_G_RT_FT1_START_LEN_PRU1	Filter1 Start and Length (PRU1)	3003 364Ch	300B 364Ch
650h	MII_G_RT_FT1_CFG_PRU1	Filter1 Configuration (PRU1)	3003 3650h	300B 3650h
654h + formula	MII_G_RT_FT1_k_DA0_PRU1	Filter1<k> DA0 (PRU1)	3003 3654h + formula	300B 3654h + formula
658h + formula	MII_G_RT_FT1_k_DA1_PRU1	Filter1<k> DA1 (PRU1)	3003 3658h + formula	300B 3658h + formula
65Ch + formula	MII_G_RT_FT1_k_DA_MASK0_PRU1	Filter1<k> DA0 Mask (PRU1)	3003 365Ch + formula	300B 365Ch + formula
660h + formula	MII_G_RT_FT1_k_DA_MASK1_PRU1	Filter1<k> DA1 Mask (PRU1)	3003 3660h + formula	300B 3660h + formula
6D4h + formula	MII_G_RT_FT3_m_START_PRU1	Filter3<m> Start (PRU1)	3003 36D4h + formula	300B 36D4h + formula

Table 14-11354. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
6D8h + formula	MII_G_RT_FT3_m_START_AUTO_PRU1	Filter3<m> Start Auto (PRU1)	3003 36D8h + formula	300B 36D8h + formula
6DCh + formula	MII_G_RT_FT3_m_START_LEN_PRU1	Filter3<m> Start offset (PRU1)	3003 36DCh + formula	300B 36DCh + formula
6E0h + formula	MII_G_RT_FT3_m_JMP_OFFSET_PRU1	Filter3<m> Jmp offset (PRU1)	3003 36E0h + formula	300B 36E0h + formula
6E4h + formula	MII_G_RT_FT3_m_LEN_PRU1	Filter3 Length Offset for (PRU1)	3003 36E4h + formula	300B 36E4h + formula
6E8h + formula	MII_G_RT_FT3_m_CFG_PRU1	Filter3<m> Configuration (PRU1)	3003 36E8h + formula	300B 36E8h + formula
6ECh + formula	MII_G_RT_FT3_m_T_PRU1	Filter3<m> T (PRU1)	3003 36ECh + formula	300B 36ECh + formula
6F0h + formula	MII_G_RT_FT3_m_T_MASK_PRU1	Filter3<m> T Mask (PRU1)	3003 36F0h + formula	300B 36F0h + formula
8D4h + formula	MII_G_RT_FT3_m_P0_PRU1	Filter3<m>P0 (PRU1)	3003 38D4h + formula	300B 38D4h + formula
8D8h + formula	MII_G_RT_FT3_m_P1_PRU1	Filter3<m>P1 (PRU1)	3003 38D8h + formula	300B 38D8h + formula
8DCh + formula	MII_G_RT_FT3_m_P_MASK0_PRU1	Filter3 P Mask0 (PRU1)	3003 38DCh + formula	300B 38DCh + formula
8E0h + formula	MII_G_RT_FT3_m_P_MASK1_PRU1	Filter3 P Mask1 (PRU1)	3003 38E0h + formula	300B 38E0h + formula
9D4h	MII_G_RT_FT_RX_PTR_PRU1	Filter Byte Count (PRU1)	3003 39D4h	300B 39D4h
9D8h + formula	MII_G_RT_RX_CLASSm_AND_EN_PRU1	RX Class<m> AND Enable (PRU1)	3003 39D8h + formula	300B 39D8h + formula
9DCh + formula	MII_G_RT_RX_CLASSm_OR_EN_PRU1	RX Class<m> OR Enable (PRU1)	3003 39DCh + formula	300B 39DCh + formula
A58h	MII_G_RT_RX_CLASS_CFG1_PRU1	RX Class Configuration 1 Register	3003 3A58h	300B 3A58h
A5Ch	MII_G_RT_RX_CLASS_CFG2_PRU1	RX Class Configuration 2 Register	3003 3A5Ch	300B 3A5Ch
A60h + formula	MII_G_RT_RX_CLASS_GATESm_PRU1	RX Class Gate Configuration PRU1 Register	3003 3A60h + formula	300B 3A60h + formula
AA0h	MII_G_RT_RX_GREEN_PRU1	RX Green Status PRU1	3003 3AA0h	300B 3AA0h
AA4h	MII_G_RT_SA_HASH_PRU1	SA Hash Seed PRU1	3003 3AA4h	300B 3AA4h
AA8h	MII_G_RT_CONN_HASH_PRU1	Connection Hash Seed PRU1	3003 3AA8h	300B 3AA8h
AACh	MII_G_RT_CONN_HASH_START_PRU1	Connection Hash Start PRU1	3003 3AACh	300B 3AACh
AB0h + formula	MII_G_RT_RX_RATE_CFGn_PRU1	RX Rate Configuration Register	3003 3AB0h + formula	300B 3AB0h + formula
AD0h	MII_G_RT_RX_RATE_SRC_SEL0_PRU1	RX Rate Source Select0	3003 3AD0h	300B 3AD0h
AD4h	MII_G_RT_RX_RATE_SRC_SEL1_PRU1	RX Rate Source Select1	3003 3AD4h	300B 3AD4h
AD8h + formula	MII_G_RT_TX_RATE_CFG1_n_PRU1	TX Rate Configuration1 Register	3003 3AD8h + formula	300B 3AD8h + formula
ADCh + formula	MII_G_RT_TX_RATE_CFG2_n_PRU1	TX Rate Configuration2 Register	3003 3ADCh + formula	300B 3ADCh + formula
B18h	MII_G_RT_RX_STAT_GOOD_PRU1	RX Good Frame Count (PRU1)	3003 3B18h	300B 3B18h
B1Ch	MII_G_RT_RX_STAT_BC_PRU1	RX BC Frame Count (PRU1)	3003 3B1Ch	300B 3B1Ch

Table 14-11354. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
B20h	MII_G_RT_RX_STAT_MC_PRU1	RX MC Frame Count (PRU1)	3003 3B20h	300B 3B20h
B24h	MII_G_RT_RX_STAT_CRC_ERR_PRU1	RX CRC Error Frame Count (PRU1)	3003 3B24h	300B 3B24h
B28h	MII_G_RT_RX_STAT_MII_ERR_PRU1	RX MII Error Frame Count (PRU1)	3003 3B28h	300B 3B28h
B2Ch	MII_G_RT_RX_STAT_ODD_ERR_PRU1	RX Odd Nibble Frame Count (PRU1)	3003 3B2Ch	300B 3B2Ch
B30h	MII_G_RT_RX_STAT_MAX_SIZE_PRU1	RX Max Size Frame (PRU1)	3003 3B30h	300B 3B30h
B34h	MII_G_RT_RX_STAT_MAX_ERR_PRU1	RX Max Size Error Frame Count (PRU1)	3003 3B34h	300B 3B34h
B38h	MII_G_RT_RX_STAT_MIN_SIZE_PRU1	RX Min Size Frame (PRU1)	3003 3B38h	300B 3B38h
B3Ch	MII_G_RT_RX_STAT_MIN_ERR_PRU1	RX Min Size Error Frame Count (PRU1)	3003 3B3Ch	300B 3B3Ch
B40h	MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1	RX Overrun Frame Count (PRU1)	3003 3B40h	300B 3B40h
B44h + formula	MII_G_RT_RX_STAT_CLASSm_HIT_PRU1	RX Class<m>	3003 3B44h + formula	300B 3B44h + formula
B84h	MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1	RX SMD Frag Error Count (PRU1)	3003 3B84h	300B 3B84h
B88h	MII_G_RT_RX_STAT_BKT1_SIZE_PRU1	RX Bucket1 Size Configuration (PRU1)	3003 3B88h	300B 3B88h
B8Ch	MII_G_RT_RX_STAT_BKT2_SIZE_PRU1	RX Bucket2 Size Configuration (PRU1)	3003 3B8Ch	300B 3B8Ch
B90h	MII_G_RT_RX_STAT_BKT3_SIZE_PRU1	RX Bucket3 Size Configuration (PRU1)	3003 3B90h	300B 3B90h
B94h	MII_G_RT_RX_STAT_BKT4_SIZE_PRU1	RX Bucket4 Size Configuration (PRU1)	3003 3B94h	300B 3B94h
B98h	MII_G_RT_RX_STAT_64_PRU1	RX 64B Sized Frame Count (PRU1)	3003 3B98h	300B 3B98h
B9Ch	MII_G_RT_RX_STAT_BKT1_PRU1	RX Bucket1 Sized Frame Count (PRU1)	3003 3B9Ch	300B 3B9Ch
BA0h	MII_G_RT_RX_STAT_BKT2_PRU1	RX Bucket2 Sized Frame Count (PRU1)	3003 3BA0h	300B 3BA0h
BA4h	MII_G_RT_RX_STAT_BKT3_PRU1	RX Bucket3 Sized Frame Count (PRU1)	3003 3BA4h	300B 3BA4h
BA8h	MII_G_RT_RX_STAT_BKT4_PRU1	RX Bucket4 Sized Frame Count (PRU1)	3003 3BA8h	300B 3BA8h
BACh	MII_G_RT_RX_STAT_BKT5_PRU1	RX Bucket5 Sized Frame Count (PRU1)	3003 3BACh	300B 3BACh
BB0h	MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1	RX Total Byte Count (PRU1)	3003 3BB0h	300B 3BB0h
BB4h	MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1	RX TX Total Byte Count (PRU1)	3003 3BB4h	300B 3BB4h
BB8h	MII_G_RT_TX_STAT_GOOD_PORT1	TX Good Frame Count Port1	3003 3BB8h	300B 3BB8h
BBCh	MII_G_RT_TX_STAT_BC_PORT1	TX BC Frame Count Port1	3003 3BBCh	300B 3BBCh
BC0h	MII_G_RT_TX_STAT_MC_PORT1	TX MC Frame Count Port1	3003 3BC0h	300B 3BC0h
BC4h	MII_G_RT_TX_STAT_ODD_ERR_PORT1	TX Odd Nibble Frame Count Port1	3003 3BC4h	300B 3BC4h

Table 14-11354. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
BC8h	MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1	TX Under Flow Error Count Port1	3003 3BC8h	300B 3BC8h
BCCh	MII_G_RT_TX_STAT_MAX_SIZE_PORT1	TX Max Size Frame Port1	3003 3BCCh	300B 3BCCh
BD0h	MII_G_RT_TX_STAT_MAX_ERR_PORT1	TX Max Size Error Frame Count Port1	3003 3BD0h	300B 3BD0h
BD4h	MII_G_RT_TX_STAT_MIN_SIZE_PORT1	TX Min Size Frame Port1	3003 3BD4h	300B 3BD4h
BD8h	MII_G_RT_TX_STAT_MIN_ERR_PORT1	TX Min Size Error Frame Count Port1	3003 3BD8h	300B 3BD8h
BDCh	MII_G_RT_TX_STAT_BKT1_SIZE_PORT1	TX Bucket1 Size Configuration Port1	3003 3BDCh	300B 3BDCh
BE0h	MII_G_RT_TX_STAT_BKT2_SIZE_PORT1	TX Bucket2 Size Configuration Port1	3003 3BE0h	300B 3BE0h
BE4h	MII_G_RT_TX_STAT_BKT3_SIZE_PORT1	TX Bucket3 Size Configuration Port1	3003 3BE4h	300B 3BE4h
BE8h	MII_G_RT_TX_STAT_BKT4_SIZE_PORT1	TX Bucket4 Size Configuration Port1	3003 3BE8h	300B 3BE8h
BECh	MII_G_RT_TX_STAT_64_PORT1	TX 64B Sized Frame Count Port1	3003 3BECh	300B 3BECh
BF0h	MII_G_RT_TX_STAT_BKT1_PORT1	TX Bucket1 Sized Frame Count Port1	3003 3BF0h	300B 3BF0h
BF4h	MII_G_RT_TX_STAT_BKT2_PORT1	TX Bucket2 Sized Frame Count Port1	3003 3BF4h	300B 3BF4h
BF8h	MII_G_RT_TX_STAT_BKT3_PORT1	TX Bucket3 Sized Frame Count Port1	3003 3BF8h	300B 3BF8h
BFCh	MII_G_RT_TX_STAT_BKT4_PORT1	TX Bucket4 Sized Frame Count Port1	3003 3BFCh	300B 3BFCh
C00h	MII_G_RT_TX_STAT_BKT5_PORT1	TX Bucket5 Sized Frame Count Port1	3003 3C00h	300B 3C00h
C04h	MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1	TX Total Byte Count Port1	3003 3C04h	300B 3C04h
C08h	MII_G_RT_TX_HSR_TAG_PORT1	TX HSR TAG Port1	3003 3C08h	300B 3C08h
C0Ch	MII_G_RT_TX_HSR_SEQ_PORT1	TX HSR Seq Port1	3003 3C0Ch	300B 3C0Ch
C10h	MII_G_RT_TX_VLAN_TYPE_TAG_PORT1	TX VLAN Type TAG Port1	3003 3C10h	300B 3C10h
C14h	MII_G_RT_TX_VLAN_INS_TAG_PORT1	TX VLAN Insertion TAG Port1	3003 3C14h	300B 3C14h
D00h + formula	MII_G_RT_QUEUEk	Queue<k>	3003 3D00h + formula	300B 3D00h + formula
E00h + formula	MII_G_RT_QUEUE_PEEKm	Queue Peek<m>	3003 3E00h + formula	300B 3E00h + formula
E40h + formula	MII_G_RT_QUEUE_CNTk	Queue Count<k>	3003 3E40h + formula	300B 3E40h + formula
F40h	MII_G_RT_QUEUE_RESET	Queue Reset	3003 3F40h	300B 3F40h

1 MII_G_RT_ICSS_G_CFG Register (Offset = 0h) [reset = X]

MII_G_RT_ICSS_G_CFG is shown in Figure 14-3756 and described in Table 14-7601.

Return to Summary Table.

ICSS_G Config

Table 14-11355. MII_G_RT_ICSS_G_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3000h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3000h

Figure 14-3756. MII_G_RT_ICSS_G_CFG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SGMII_MODE</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W-1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td>TX_PRU_EN</td><td>RX_SFD_TX_SOF_EN</td><td>RTU_PRU_PSI_SHARE_EN</td><td>IEP1_TX_EN</td></tr>
<tr><td colspan="4">R/W-X</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="2">MII1_MODE</td><td colspan="2">MII0_MODE</td><td>RX_L2_G_EN</td><td>TX_L2_EN</td><td>TX_L1_EN</td></tr>
<tr><td>R/W-X</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-1h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11357. MII_G_RT_ICSS_G_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	SGMII_MODE	R/W	1h	SGMII MODE 0: Fiber MODE 1: SGMII MODE
15-12	RESERVED	R/W	X	
11	TX_PRU_EN	R/W	0h	Enable TX_PRU to gain control of MII TXL2
10	RX_SFD_TX_SOF_EN	R/W	0h	Enable the remaping of tx_sof to rx_sfd if auto fwd is enable
9	RTU_PRU_PSI_SHARE_EN	R/W	0h	Enable the sharing of xfr2psi attached to PRU for PRU RTU AND HW FIFO
8	IEP1_TX_EN	R/W	0h	Enable IEP1 for TX Enable 0: Use IEP0 CMP3_4 1: Use IEP1 CMP3_4
7	RESERVED	R/W	X	
6-5	MII1_MODE	R/W	0h	MII1 MODE 0: MII 1: RGMII 2: SGMII **SGMII mode is supported only for PRU_ICSSG instance.**

Table 14-11357. MII_G_RT_ICSS_G_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	MII0_MODE	R/W	0h	MII0 MODE 0: MII 1: RGMII 2: SGMII **SGMII mode is supported only for PRU_ICSSG instance.**
2	RX_L2_G_EN	R/W	0h	Enable new RX L2 mode of operation for non-EtherCAT Target protocols. 0: Disabled 1: Enabled Disable for EtherCAT Target protocols, enable for all other protocols.
1	TX_L2_EN	R/W	0h	Enable the TX L2 FIFO 0: Disabled 1: Enabled
0	TX_L1_EN	R/W	1h	Enable the TX L1 FIFO 0: Disabled 1: Enabled

2 MII_G_RT_RGMII_CFG Register (Offset = 4h) [reset = X]

MII_G_RT_RGMII_CFG is shown in Figure 14-3757 and described in Table 14-7603.

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RGMII

Table 14-11358. MII_G_RT_RGMII_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3004h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3004h

Figure 14-3757. MII_G_RT_RGMII_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	RGMII1_FULLDUPLEX_IN	RGMII1_GIG_IN	RGMII1_INBAND	RESERVED	RGMII0_FULLDUPLEX_IN	RGMII0_GIG_IN	RGMII0_INBAND
R/W-X	R/W-1h	R/W-1h	R/W-0h	R/W-X	R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						RGMII_EEE_PHY_ONLY	RGMII_EEE_EN
R/W-X						R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RGMII1_FULLDUPLEX	RGMII1_SPEED		RGMII1_LINK	RGMII0_FULLDUPLEX	RGMII0_SPEED		RGMII0_LINK
R-0h	R-0h		R-0h	R-0h	R-0h		R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11360. MII_G_RT_RGMII_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	RGMII1_FULLDUPLEX_IN	R/W	1h	RGMII Fullduplex overide 0: half 1: full
21	RGMII1_GIG_IN	R/W	1h	RGMII GigBit Enable 0: 100 Mbs 1: 1000 Mbs
20	RGMII1_INBAND	R/W	0h	RGMII In BandEnable or Force 0: InBAND is Disabled 1: InBAND Enable
19	RESERVED	R/W	X	
18	RGMII0_FULLDUPLEX_IN	R/W	1h	RGMII Fullduplex overide 0: half 1: full
17	RGMII0_GIG_IN	R/W	1h	RGMII GigBit Enable 0: 100 Mbs 1: 1000 Mbs
16	RGMII0_INBAND	R/W	0h	RGMII In BandEnable or Force 0: InBAND is Disabled 1: InBAND Enable
15-10	RESERVED	R/W	X	

Table 14-11360. MII_G_RT_RGMII_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RGMII_EEE_PHY_ONLY	R/W	0h	RGMII Phy Only Low Power 0: disable 1: enable
8	RGMII_EEE_EN	R/W	0h	RGMII Energy Efficient Enable 0: disable 1: enable
7	RGMII1_FULLDUPLEX	R	0h	RGMII Fullduplex 0: half duplex 1: full duplex
6-5	RGMII1_SPEED	R	0h	RGMII Speed 00: 10 Mpbs 01: 100 Mpbs 10: 1000 Mpbs
4	RGMII1_LINK	R	0h	RGMII Link Status 0: link is down 1: link is up
3	RGMII0_FULLDUPLEX	R	0h	RGMII Fullduplex 0: half duplex 1: full duplex
2-1	RGMII0_SPEED	R	0h	RGMII Speed 00: 10 Mpbs 01: 100 Mpbs 10: 1000 Mpbs
0	RGMII0_LINK	R	0h	RGMII Link Status 0: link is down 1: link is up

3 MII_G_RT_MAC_PRU0_0 Register (Offset = 8h) [reset = 0h]

MII_G_RT_MAC_PRU0_0 is shown in Figure 14-3758 and described in Table 14-7605.

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PRU0 MAC (DA3:DA0).

Table 14-11361. MII_G_RT_MAC_PRU0_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3008h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3008h

Figure 14-3758. MII_G_RT_MAC_PRU0_0 Register

31-0
MAC_PRU0_0
R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11363. MII_G_RT_MAC_PRU0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAC_PRU0_0	R/W	0h	MAC PRU0 DA3:DA0 Used for SAV and DA match

4 MII_G_RT_MAC_PRU0_1 Register (Offset = Ch) [reset = X]

MII_G_RT_MAC_PRU0_1 is shown in Figure 14-3759 and described in Table 14-7607.

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PRU0 MAC (DA5:DA4).

Table 14-11364. MII_G_RT_MAC_PRU0_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 300Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 300Ch

Figure 14-3759. MII_G_RT_MAC_PRU0_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MAC_PRU0_1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11366. MII_G_RT_MAC_PRU0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MAC_PRU0_1	R/W	0h	MAC PRU0 DA5:DA4 Used for SAV and DA match

5 MII_G_RT_MAC_PRU1_0 Register (Offset = 10h) [reset = 0h]

MII_G_RT_MAC_PRU1_0 is shown in Figure 14-3760 and described in Table 14-7609.

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PRU1 MAC (DA3:DA0).

Table 14-11367. MII_G_RT_MAC_PRU1_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3010h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3010h

Figure 14-3760. MII_G_RT_MAC_PRU1_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_PRU1_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11369. MII_G_RT_MAC_PRU1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAC_PRU1_0	R/W	0h	MAC PRU1 DA3:DA0 Used for SAV and DA match

6 MII_G_RT_MAC_PRU1_1 Register (Offset = 14h) [reset = X]

MII_G_RT_MAC_PRU1_1 is shown in Figure 14-3761 and described in Table 14-7611.

Return to Summary Table.

PRU1 MAC (DA5:DA4).

Table 14-11370. MII_G_RT_MAC_PRU1_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3014h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3014h

Figure 14-3761. MII_G_RT_MAC_PRU1_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MAC_PRU1_1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11372. MII_G_RT_MAC_PRU1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MAC_PRU1_1	R/W	0h	MAC PRU1 DA5:DA4 Used for SAV and DA match

7 MII_G_RT_MAC_INTERFACE_0 Register (Offset = 18h) [reset = 0h]

MII_G_RT_MAC_INTERFACE_0 is shown in Figure 14-3762 and described in Table 14-7613.

Return to Summary Table.

MAC Host Interface (DA3:DA0).

Table 14-11373. MII_G_RT_MAC_INTERFACE_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3018h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3018h

Figure 14-3762. MII_G_RT_MAC_INTERFACE_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_INF_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11375. MII_G_RT_MAC_INTERFACE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAC_INF_0	R/W	0h	MAC Host interface DA3:DA0 Used for SAV and DA match

8 MII_G_RT_MAC_INTERFACE_1 Register (Offset = 1Ch) [reset = X]

MII_G_RT_MAC_INTERFACE_1 is shown in Figure 14-3763 and described in Table 14-7615.

Return to Summary Table.

MAC Host Interface (DA5:DA4).

Table 14-11376. MII_G_RT_MAC_INTERFACE_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 301Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 301Ch

Figure 14-3763. MII_G_RT_MAC_INTERFACE_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MAC_INF_1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11378. MII_G_RT_MAC_INTERFACE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MAC_INF_1	R/W	0h	MAC Host interface DA 5:DA4 Used for SAV and DA match

9 MII_G_RT_PREEMPT_CFG Register (Offset = 20h) [reset = X]

MII_G_RT_PREEMPT_CFG is shown in Figure 14-3764 and described in Table 14-7617.

Return to Summary Table.

Preempt Configuration Register.

Table 14-11379. MII_G_RT_PREEMPT_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3020h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3020h

Figure 14-3764. MII_G_RT_PREEMPT_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMD_R								SMD_V								EXP_SMD								RESERVED							
R/W-19h								R/W-7h								R/W-D5h								R/W-X							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11381. MII_G_RT_PREEMPT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SMD_R	R/W	19h	Response frame TAG
23-16	SMD_V	R/W	7h	Verification frame TAG
15-8	EXP_SMD	R/W	D5h	None pre-emptable frame start, or express frame
7-0	RESERVED	R/W	X	

10 MII_G_RT_SMDT1S_CFG Register (Offset = 24h) [reset = B37F4CE6h]

MII_G_RT_SMDT1S_CFG is shown in Figure 14-3765 and described in Table 14-7619.

Return to Summary Table.

SMD Type1S Preemptable Frame Start Configuration.

Table 14-11382. MII_G_RT_SMDT1S_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3024h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3024h

Figure 14-3765. MII_G_RT_SMDT1S_CFG Register

31-24	23-16	15-8	7-0
SMDT1S_3	SMDT1S_2	SMDT1S_1	SMDT1S_0
R/W-B3h	R/W-7Fh	R/W-4Ch	R/W-E6h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11384. MII_G_RT_SMDT1S_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SMDT1S_3	R/W	B3h	SMDT1S3 pattern
23-16	SMDT1S_2	R/W	7Fh	SMDT1S2 pattern
15-8	SMDT1S_1	R/W	4Ch	SMDT1S1 pattern
7-0	SMDT1S_0	R/W	E6h	SMDT1S0 pattern

11 MII_G_RT_SMDT1C_CFG Register (Offset = 28h) [reset = 2A9E5261h]

MII_G_RT_SMDT1C_CFG is shown in Figure 14-3766 and described in Table 14-7621.

Return to Summary Table.

SMD Type1C None Initial Frag Configuration.

Table 14-11385. MII_G_RT_SMDT1C_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3028h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3028h

Figure 14-3766. MII_G_RT_SMDT1C_CFG Register

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
SMDT1C_3	SMDT1C_2	SMDT1C_1	SMDT1C_0
R/W-2Ah	R/W-9Eh	R/W-52h	R/W-61h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11387. MII_G_RT_SMDT1C_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SMDT1C_3	R/W	2Ah	SMDT1C3 pattern
23-16	SMDT1C_2	R/W	9Eh	SMDT1C2 pattern
15-8	SMDT1C_1	R/W	52h	SMDT1C1 pattern
7-0	SMDT1C_0	R/W	61h	SMDT1C0 pattern

12 MII_G_RT_FRAG_CNT_CFG Register (Offset = 34h) [reset = B37F4CE6h]

MII_G_RT_FRAG_CNT_CFG is shown in Figure 14-3767 and described in Table 14-7623.

Return to Summary Table.

Frag Count Configuration.

Table 14-11388. MII_G_RT_FRAG_CNT_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3034h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3034h

Figure 14-3767. MII_G_RT_FRAG_CNT_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRAG_CNT_3								FRAG_CNT_2							
R/W-B3h								R/W-7Fh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAG_CNT_1								FRAG_CNT_0							
R/W-4Ch								R/W-E6h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11390. MII_G_RT_FRAG_CNT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	FRAG_CNT_3	R/W	B3h	FRAG Cnt3 pattern
23-16	FRAG_CNT_2	R/W	7Fh	FRAG Cnt2 pattern
15-8	FRAG_CNT_1	R/W	4Ch	FRAG Cnt1 pattern
7-0	FRAG_CNT_0	R/W	E6h	FRAG Cnt0 pattern

13 MII_G_RT_PA_STAT_PUSH0 Register (Offset = 40h) [reset = 0h]

MII_G_RT_PA_STAT_PUSH0 is shown in Figure 14-3768 and described in Table 14-7625.

Return to Summary Table.

Pa Stat Push0.

Table 14-11391. MII_G_RT_PA_STAT_PUSH0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3040h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3040h

Figure 14-3768. MII_G_RT_PA_STAT_PUSH0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PA_STAT_PUSH3_0								PA_STAT_PUSH2_0							
R/W-0h								R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_STAT_PUSH1_0								PA_STAT_PUSH0_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11393. MII_G_RT_PA_STAT_PUSH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PA_STAT_PUSH3_0	R/W	0h	pa stat push3
23-16	PA_STAT_PUSH2_0	R/W	0h	pa stat push2
15-8	PA_STAT_PUSH1_0	R/W	0h	pa stat push1
7-0	PA_STAT_PUSH0_0	R/W	0h	pa stat push0

14 MII_G_RT_PA_STAT_PUSH1 Register (Offset = 44h) [reset = 0h]

MII_G_RT_PA_STAT_PUSH1 is shown in Figure 14-3769 and described in Table 14-7627.

Return to Summary Table.

Pa Stat Push1.

Table 14-11394. MII_G_RT_PA_STAT_PUSH1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3044h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3044h

Figure 14-3769. MII_G_RT_PA_STAT_PUSH1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PA_STAT_PUSH3_1</td><td colspan="8">PA_STAT_PUSH2_1</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PA_STAT_PUSH1_1</td><td colspan="8">PA_STAT_PUSH0_1</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11396. MII_G_RT_PA_STAT_PUSH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PA_STAT_PUSH3_1	R/W	0h	pa stat push3
23-16	PA_STAT_PUSH2_1	R/W	0h	pa stat push2
15-8	PA_STAT_PUSH1_1	R/W	0h	pa stat push1
7-0	PA_STAT_PUSH0_1	R/W	0h	pa stat push0

15 MII_G_RT_PA_STAT_PUSH2 Register (Offset = 48h) [reset = 0h]

MII_G_RT_PA_STAT_PUSH2 is shown in Figure 14-3770 and described in Table 14-7629.

Return to Summary Table.

Pa Stat Push2.

Table 14-11397. MII_G_RT_PA_STAT_PUSH2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3048h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3048h

Figure 14-3770. MII_G_RT_PA_STAT_PUSH2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PA_STAT_PUSH3_2</td><td colspan="8">PA_STAT_PUSH2_2</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PA_STAT_PUSH1_2</td><td colspan="8">PA_STAT_PUSH0_2</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11399. MII_G_RT_PA_STAT_PUSH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PA_STAT_PUSH3_2	R/W	0h	pa stat push3
23-16	PA_STAT_PUSH2_2	R/W	0h	pa stat push2
15-8	PA_STAT_PUSH1_2	R/W	0h	pa stat push1
7-0	PA_STAT_PUSH0_2	R/W	0h	pa stat push0

16 MII_G_RT_PA_STAT_PUSH3 Register (Offset = 4Ch) [reset = 0h]

MII_G_RT_PA_STAT_PUSH3 is shown in Figure 14-3771 and described in Table 14-7631.

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Pa Stat Push3.

Table 14-11400. MII_G_RT_PA_STAT_PUSH3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 304Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 304Ch

Figure 14-3771. MII_G_RT_PA_STAT_PUSH3 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PA_STAT_PUSH3_3</td><td colspan="8">PA_STAT_PUSH2_3</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PA_STAT_PUSH1_3</td><td colspan="8">PA_STAT_PUSH0_3</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11402. MII_G_RT_PA_STAT_PUSH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PA_STAT_PUSH3_3	R/W	0h	pa stat push3
23-16	PA_STAT_PUSH2_3	R/W	0h	pa stat push2
15-8	PA_STAT_PUSH1_3	R/W	0h	pa stat push1
7-0	PA_STAT_PUSH0_3	R/W	0h	pa stat push0

17 MII_G_RT_FDB_GEN_CFG1 Register (Offset = 60h) [reset = X]

MII_G_RT_FDB_GEN_CFG1 is shown in Figure 14-3772 and described in Table 14-7633.

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FDB Configuration1.

Table 14-11403. MII_G_RT_FDB_GEN_CFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3060h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3060h

Figure 14-3772. MII_G_RT_FDB_GEN_CFG1 Register

31	30	29	28	27	26	25	24
RESERVED						SMEM_VLAN_OFFSET	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
SMEM_VLAN_OFFSET							
R/W-0h							
15	14	13	12	11	10	9	8
SMEM_VLAN_OFFSET							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	FDB_HASH_SIZE				RESERVED	FDB_BUCKET_SIZE	
R/W-X	R/W-4h				R/W-X	R/W-2h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11405. MII_G_RT_FDB_GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-8	SMEM_VLAN_OFFSET	R/W	0h	SMEM VLAN FID table base address
7	RESERVED	R/W	X	
6-3	FDB_HASH_SIZE	R/W	4h	FDB hash size (Slots) 0: 64 1: 128 2: 256 3: 512 4: 1024 5: 2048
2	RESERVED	R/W	X	
1-0	FDB_BUCKET_SIZE	R/W	2h	FDB bucket size 0: 1 1: 2 2: 4 3: 8

18 MII_G_RT_FDB_GEN_CFG2 Register (Offset = 64h) [reset = X]

MII_G_RT_FDB_GEN_CFG2 is shown in Figure 14-3773 and described in Table 14-7635.

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FDB Configuration2.

Table 14-11406. MII_G_RT_FDB_GEN_CFG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3064h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3064h

Figure 14-3773. MII_G_RT_FDB_GEN_CFG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			FDB_GEN_MODE_BYTE_EN				FDB_GEN_MODE_EN_BK1
R/W-X			R/W-0h				R/W-0h
7	6	5	4	3	2	1	0
FDB_GEN_MODE_EN_BK0	FDB_VLAN_EN	FDB_HSR_EN	RESERVED		FDB_HOST_EN	FDB_PRU1_EN	FDB_PRU0_EN
R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11408. MII_G_RT_FDB_GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12-9	FDB_GEN_MODE_BYTE_EN	R/W	0h	FDB General Mode Byte compare size 0 = 1 Byte, 15 = 16 Bytes
8	FDB_GEN_MODE_EN_BK1	R/W	0h	FDB General Mode Enable Bank1 if set PRU0/PRU1/HOST will get disabled
7	FDB_GEN_MODE_EN_BK0	R/W	0h	FDB General Mode Enable Bank0 if set PRU0/PRU1/HOST will get disabled
6	FDB_VLAN_EN	R/W	0h	FDB Global VLAN Enable
5	FDB_HSR_EN	R/W	0h	FDB Global HSR Enable Note: VLAN must be disabled
4-3	RESERVED	R/W	X	
2	FDB_HOST_EN	R/W	0h	FDB HOST Enable
1	FDB_PRU1_EN	R/W	0h	FDB PRU1 Enable
0	FDB_PRU0_EN	R/W	0h	FDB PRU0 Enable

19 MII_G_RT_FDB_DF_VLAN Register (Offset = 6Ch) [reset = X]

MII_G_RT_FDB_DF_VLAN is shown in Figure 14-3774 and described in Table 14-7637.

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FDB Default PRU VLAN.

Table 14-11409. MII_G_RT_FDB_DF_VLAN Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 306Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 306Ch

Figure 14-3774. MII_G_RT_FDB_DF_VLAN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				FDB_PRU1_DF_VLAN											
R/W-X				R/W-1h											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				FDB_PRU0_DF_VLAN											
R/W-X				R/W-1h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11411. MII_G_RT_FDB_DF_VLAN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	FDB_PRU1_DF_VLAN	R/W	1h	FDB Default VLAN for PRU1
15-12	RESERVED	R/W	X	
11-0	FDB_PRU0_DF_VLAN	R/W	1h	FDB Default VLAN for PRU0

20 MII_G_RT_FDB_HOST_DA0 Register (Offset = 70h) [reset = 0h]

MII_G_RT_FDB_HOST_DA0 is shown in Figure 14-3775 and described in Table 14-7639.

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FDB HOST DA3:0 Configuration.

Table 14-11412. MII_G_RT_FDB_HOST_DA0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3070h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3070h

Figure 14-3775. MII_G_RT_FDB_HOST_DA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDB_HOST_DA0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11414. MII_G_RT_FDB_HOST_DA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FDB_HOST_DA0	R/W	0h	FDB HOST DA3:0

21 MII_G_RT_FDB_HOST_DA1 Register (Offset = 74h) [reset = X]

MII_G_RT_FDB_HOST_DA1 is shown in Figure 14-3776 and described in Table 14-7641.

Return to Summary Table.

FDB HOST DA5:4 Configuration.

Table 14-11415. MII_G_RT_FDB_HOST_DA1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3074h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3074h

Figure 14-3776. MII_G_RT_FDB_HOST_DA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FDB_HOST_DA1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11417. MII_G_RT_FDB_HOST_DA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FDB_HOST_DA1	R/W	0h	FDB HOST DA 5:4

22 MII_G_RT_FDB_HOST_SA0 Register (Offset = 78h) [reset = 0h]

MII_G_RT_FDB_HOST_SA0 is shown in Figure 14-3777 and described in Table 14-7643.

Return to Summary Table.

FDB HOST SA3:0 Configuration.

Table 14-11418. MII_G_RT_FDB_HOST_SA0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3078h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3078h

Figure 14-3777. MII_G_RT_FDB_HOST_SA0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FDB_HOST_SA0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11420. MII_G_RT_FDB_HOST_SA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FDB_HOST_SA0	R/W	0h	FDB HOST SA3:0

23 MII_G_RT_FDB_HOST_VLAN_SA1 Register (Offset = 7Ch) [reset = 00010000h]

MII_G_RT_FDB_HOST_VLAN_SA1 is shown in Figure 14-3778 and described in Table 14-7645.

Return to Summary Table.

FDB HOST VLAN SA5:4 Configuration.

Table 14-11421. MII_G_RT_FDB_HOST_VLAN_SA1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 307Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 307Ch

Figure 14-3778. MII_G_RT_FDB_HOST_VLAN_SA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FDB_HOST_VLAN_HSR															
R/W-1h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FDB_HOST_SA1															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11423. MII_G_RT_FDB_HOST_VLAN_SA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FDB_HOST_VLAN_HSR	R/W	1h	FDB HOST VLAN[11:0] OR HSR [15:0]
15-0	FDB_HOST_SA1	R/W	0h	FDB HOST SA 5:4

24 MII_G_RT_FT1_START_LEN_PRU0 Register (Offset = 80h) [reset = X]

MII_G_RT_FT1_START_LEN_PRU0 is shown in Figure 14-3779 and described in Table 14-7647.

Return to Summary Table.

Filter1 Start and Length (PRU0).

Table 14-11424. MII_G_RT_FT1_START_LEN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3080h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3080h

Figure 14-3779. MII_G_RT_FT1_START_LEN_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FT1_LEN</td></tr>
<tr><td colspan="4">R/W-X</td><td colspan="4">R/W-6h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">FT1_START</td></tr>
<tr><td>R/W-X</td><td colspan="7">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FT1_START</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11426. MII_G_RT_FT1_START_LEN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	FT1_LEN	R/W	6h	Defines the total number of Bytes Filter1 will check before Valid bit is set
15	RESERVED	R/W	X	
14-0	FT1_START	R/W	0h	Byte count start for Filter1. Any write will clear all Filter1 Status Bits

25 MII_G_RT_FT1_CFG_PRU0 Register (Offset = 84h) [reset = X]

MII_G_RT_FT1_CFG_PRU0 is shown in Figure 14-3780 and described in Table 14-7649.

Return to Summary Table.

Filter1 Configuration (PRU0).

Table 14-11427. MII_G_RT_FT1_CFG_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3084h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3084h

Figure 14-3780. MII_G_RT_FT1_CFG_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
FT1_7CFG		FT1_6CFG		FT1_5CFG		FT1_4CFG	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	
7	6	5	4	3	2	1	0
FT1_3CFG		FT1_2CFG		FT1_1CFG		FT1_0CFG	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11429. MII_G_RT_FT1_CFG_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	FT1_7CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
13-12	FT1_6CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
11-10	FT1_5CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
9-8	FT1_4CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
7-6	FT1_3CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
5-4	FT1_2CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than

Table 14-11429. MII_G_RT_FT1_CFG_PRU0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	FT1_1CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
1-0	FT1_0CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than

26 MII_G_RT_FT1_k_DA0_PRU0 Register (Offset = 88h + formula) [reset = 0h]

MII_G_RT_FT1_k_DA0_PRU0 is shown in Figure 14-3781 and described in Table 14-7651.

Return to Summary Table.

Filter1<k> DA0 (Pru0).

Offset = 88h + (k * 10h); where k = 0h to 7h

Table 14-11430. MII_G_RT_FT1_k_DA0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3088h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3088h + formula

Figure 14-3781. MII_G_RT_FT1_k_DA0_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT1_k_DA0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11432. MII_G_RT_FT1_k_DA0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT1_k_DA0	R/W	0h	Filter1 DA4:DA1

27 MII_G_RT_FT1_k_DA1_PRU0 Register (Offset = 8Ch + formula) [reset = X]

MII_G_RT_FT1_k_DA1_PRU0 is shown in Figure 14-3782 and described in Table 14-7653.

Return to Summary Table.

Filter1<k> DA1 (PRU0).

Offset = 8Ch + (k * 10h); where k = 0h to 7h

Table 14-11433. MII_G_RT_FT1_k_DA1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 308Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 308Ch + formula

Figure 14-3782. MII_G_RT_FT1_k_DA1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT1_k_DA1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11435. MII_G_RT_FT1_k_DA1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FT1_k_DA1	R/W	0h	Filter1 DA6:DA5

28 MII_G_RT_FT1_k_DA_MASK0_PRU0 Register (Offset = 90h + formula) [reset = 0h]

MII_G_RT_FT1_k_DA_MASK0_PRU0 is shown in Figure 14-3783 and described in Table 14-7655.

Return to Summary Table.

Filter1<k> DA0 Mask (PRU0).

Offset = 90h + (k * 10h); where k = 0h to 7h

Table 14-11436. MII_G_RT_FT1_k_DA_MASK0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3090h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3090h + formula

Figure 14-3783. MII_G_RT_FT1_k_DA_MASK0_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT1_k_DA_MASK0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11438. MII_G_RT_FT1_k_DA_MASK0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT1_k_DA_MASK0	R/W	0h	Filter1 MDA4:MDA1 set to 1 to mask corresponding bit

29 MII_G_RT_FT1_k_DA_MASK1_PRU0 Register (Offset = 94h + formula) [reset = X]

MII_G_RT_FT1_k_DA_MASK1_PRU0 is shown in Figure 14-3784 and described in Table 14-7657.

Return to Summary Table.

Filter1<k> DA1 Mask (PRU0).

Offset = 94h + (k * 10h); where k = 0h to 7h

Table 14-11439. MII_G_RT_FT1_k_DA_MASK1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3094h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3094h + formula

Figure 14-3784. MII_G_RT_FT1_k_DA_MASK1_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">FT1_k_DA_MASK1</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11441. MII_G_RT_FT1_k_DA_MASK1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FT1_k_DA_MASK1	R/W	0h	Filter1 MDA6:MDA5 set to 1 to mask corresponding bit

30 MII_G_RT_FT3_m_START_PRU0 Register (Offset = 108h + formula) [reset = X]

MII_G_RT_FT3_m_START_PRU0 is shown in Figure 14-3785 and described in Table 14-7659.

Return to Summary Table.

Filter3 Byte Count Start.

Offset = 108h + (m * 20h); where m = 0h to Fh

Table 14-11442. MII_G_RT_FT3_m_START_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3108h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3108h + formula

Figure 14-3785. MII_G_RT_FT3_m_START_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="17">RESERVED</td><td colspan="15">FT3_START</td></tr>
<tr><td colspan="17">R/W-X</td><td colspan="15">R/W-Ch</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11444. MII_G_RT_FT3_m_START_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-0	FT3_START	R/W	Ch	Byte count start for Filter3. Any write will clear all Filter3 Status Bits SW can read to determine next start during Auto

31 MII_G_RT_FT3_m_START_AUTO_PRU0 Register (Offset = 10Ch + formula) [reset = X]

MII_G_RT_FT3_m_START_AUTO_PRU0 is shown in Figure 14-3786 and described in Table 14-7661.

Return to Summary Table.

Filter3 Byte Count Start for Auto Skip mode.

Offset = 10Ch + (m * 20h); where m = 0h to Fh

Table 14-11445. MII_G_RT_FT3_m_START_AUTO_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 310Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 310Ch + formula

Figure 14-3786. MII_G_RT_FT3_m_START_AUTO_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	FT3_START_AUTO														
R-X																	R-0h														

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11447. MII_G_RT_FT3_m_START_AUTO_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	X	
14-0	FT3_START_AUTO	R	0h	Byte count start for Auto skip mode

32 MII_G_RT_FT3_m_START_LEN_PRU0 Register (Offset = 110h + formula) [reset = X]

MII_G_RT_FT3_m_START_LEN_PRU0 is shown in Figure 14-3787 and described in Table 14-7663.

Return to Summary Table.

Filter3 Start Offset for PRU0.

Offset = 110h + (m * 20h); where m = 0h to Fh

Table 14-11448. MII_G_RT_FT3_m_START_LEN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3110h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3110h + formula

Figure 14-3787. MII_G_RT_FT3_m_START_LEN_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED	FT3_OFFSET_END			RESERVED	FT3_OFFSET_START		
R/W-X	R/W-0h			R/W-X	R/W-0h		

15	14	13	12	11	10	9	8
RESERVED	FT3_OFFSET						
R/W-X	R/W-0h						

7	6	5	4	3	2	1	0
FT3_OFFSET							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11450. MII_G_RT_FT3_m_START_LEN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-20	FT3_OFFSET_END	R/W	0h	Defines which byte within FT3_[N]P[63:0] to end the compare at set the Valid flag, rule ft3_offset_end >= ft3_offset_start To disable pattern compare set start and end to zero
19	RESERVED	R/W	X	
18-16	FT3_OFFSET_START	R/W	0h	Defines which byte within FT3_[N]P[63:0] to start the compare
15	RESERVED	R/W	X	
14-0	FT3_OFFSET	R/W	0h	Determine which byte to start FT3_[N]P[63:0] operation it will start on the next byte after FT3_T completes if set to zero

33 MII_G_RT_FT3_m_JMP_OFFSET_PRU0 Register (Offset = 114h + formula) [reset = X]

MII_G_RT_FT3_m_JMP_OFFSET_PRU0 is shown in Figure 14-3788 and described in Table 14-7665.

Return to Summary Table.

Filter3 Jump Offset for PRU0.

Offset = 114h + (m * 20h); where m = 0h to Fh

Table 14-11451. MII_G_RT_FT3_m_JMP_OFFSET_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3114h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3114h + formula

Figure 14-3788. MII_G_RT_FT3_m_JMP_OFFSET_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED	FT3_m_NJMP_OFFSET_PRU0						
R/W-X	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FT3_m_NJMP_OFFSET_PRU0							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	FT3_m_IJMP_OFFSET_PRU0						
R/W-X	R/W-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FT3_m_IJMP_OFFSET_PRU0							
R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11453. MII_G_RT_FT3_m_JMP_OFFSET_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	FT3_m_NJMP_OFFSET_PRU0	R/W	0h	Defines the Next Offset to compare when auto arm jump is enabled
15	RESERVED	R/W	X	
14-0	FT3_m_IJMP_OFFSET_PRU0	R/W	0h	Defines the Initial Offset to compare when auto arm jump is enabled

34 MII_G_RT_FT3_m_LEN_PRU0 Register (Offset = 118h + formula) [reset = X]

MII_G_RT_FT3_m_LEN_PRU0 is shown in Figure 14-3789 and described in Table 14-7667.

Return to Summary Table.

Filter3 Length Offset for PRU0.

Offset = 118h + (m * 20h); where m = 0h to Fh

Table 14-11454. MII_G_RT_FT3_m_LEN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3118h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3118h + formula

Figure 14-3789. MII_G_RT_FT3_m_LEN_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							FT3_m_LEN_BIG_EN_PRU0
R/W-X							R/W-0h

23	22	21	20	19	18	17	16
RESERVED				FT3_m_LEN_SIZE_BIT_PRU0			
R/W-X				R/W-0h			

15	14	13	12	11	10	9	8
RESERVED							FT3_m_LEN_START_BIT_PRU0
R/W-X							R/W-0h

7	6	5	4	3	2	1	0
FT3_m_LEN_START_BIT_PRU0							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11456. MII_G_RT_FT3_m_LEN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	FT3_m_LEN_BIG_EN_PRU0	R/W	0h	Enable Big Indian on Length
23-20	RESERVED	R/W	X	
19-16	FT3_m_LEN_SIZE_BIT_PRU0	R/W	0h	Defines number of bits to extract the length for the auto skip function
15-9	RESERVED	R/W	X	
8-0	FT3_m_LEN_START_BIT_PRU0	R/W	0h	Defines relative bit offset from the HIT byte location upto 512 bit offset the extraction to determine the on the fly length byte offset

35 MII_G_RT_FT3_m_CFG_PRU0 Register (Offset = 11Ch + formula) [reset = X]

MII_G_RT_FT3_m_CFG_PRU0 is shown in Figure 14-3790 and described in Table 14-7669.

Return to Summary Table.

Filter3 Configuration for PRU0.

Offset = 11Ch + (m * 20h); where m = 0h to Fh

Table 14-11457. MII_G_RT_FT3_m_CFG_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 311Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 311Ch + formula

Figure 14-3790. MII_G_RT_FT3_m_CFG_PRU0 Register

31	30	29	28	27	26	25	24
FT3_m_TRIG_OR_EN							
R/W-0h							
23	22	21	20	19	18	17	16
FT3_m_TRIG_OR_EN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					FT3_m_VLAN_SKIP_EN	FT3_mCFG	
R/W-X					R/W-1h	R/W-1h	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11459. MII_G_RT_FT3_m_CFG_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FT3_m_TRIG_OR_EN	R/W	0h	Trigger ft3 select for auto skip enable, if one or more set the function is enabled note you can not select the same ft3 only others
15-3	RESERVED	R/W	X	
2	FT3_m_VLAN_SKIP_EN	R/W	1h	0: Disabled 1: Enable
1-0	FT3_mCFG	R/W	1h	0: Disabled 1: EQ 2: GT 3: LT

36 MII_G_RT_FT3_m_T_PRU0 Register (Offset = 120h + formula) [reset = 0h]

MII_G_RT_FT3_m_T_PRU0 is shown in Figure 14-3791 and described in Table 14-7671.

Return to Summary Table.

Filter3 Type for PRU0.

Offset = 120h + (m * 20h); where m = 0h to Fh

Table 14-11460. MII_G_RT_FT3_m_T_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3120h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3120h + formula

Figure 14-3791. MII_G_RT_FT3_m_T_PRU0 Register

31-0
FT3_m_T
R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11462. MII_G_RT_FT3_m_T_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_T	R/W	0h	Filter3 T4:T1 Note if Auto Skip is enabled then Type filter is not enabled

37 MII_G_RT_FT3_m_T_MASK_PRU0 Register (Offset = 124h + formula) [reset = 0h]

MII_G_RT_FT3_m_T_MASK_PRU0 is shown in Figure 14-3792 and described in Table 14-7673.

Return to Summary Table.

Filter3 Mask for PRU0.

Offset = 124h + (m * 20h); where m = 0h to Fh

Table 14-11463. MII_G_RT_FT3_m_T_MASK_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3124h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3124h + formula

Figure 14-3792. MII_G_RT_FT3_m_T_MASK_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_T_MASK																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11465. MII_G_RT_FT3_m_T_MASK_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_T_MASK	R/W	0h	Filter3 MT4:MT1 Note: if Auto Skip is enabled then Type filter is not enabled set to 1 to mask corresponding bit

38 MII_G_RT_FT3_m_P0_PRU0 Register (Offset = 308h + formula) [reset = 0h]

MII_G_RT_FT3_m_P0_PRU0 is shown in Figure 14-3793 and described in Table 14-7675.

Return to Summary Table.

Filter3 PRU0 (P4:P1).

Offset = 308h + (m * 10h); where m = 0h to Fh

Table 14-11466. MII_G_RT_FT3_m_P0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3308h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3308h + formula

Figure 14-3793. MII_G_RT_FT3_m_P0_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT3_m_P0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11468. MII_G_RT_FT3_m_P0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P0	R/W	0h	Filter3 P4:P1

39 MII_G_RT_FT3_m_P1_PRU0 Register (Offset = 30Ch + formula) [reset = 0h]

MII_G_RT_FT3_m_P1_PRU0 is shown in Figure 14-3794 and described in Table 14-7677.

Return to Summary Table.

Filter3 PRU0 (P8:P5).

Offset = 30Ch + (m * 10h); where m = 0h to Fh

Table 14-11469. MII_G_RT_FT3_m_P1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 330Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 330Ch + formula

Figure 14-3794. MII_G_RT_FT3_m_P1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_P1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11471. MII_G_RT_FT3_m_P1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P1	R/W	0h	Filter3 P8:P5

40 MII_G_RT_FT3_n_P_MASK0_PRU0 Register (Offset = 310h + formula) [reset = 0h]

MII_G_RT_FT3_n_P_MASK0_PRU0 is shown in Figure 14-3795 and described in Table 14-7679.

Return to Summary Table.

Filter3 Mask0 (MP4:MP1).

Offset = 310h + (n * 10h); where n = 0h to Fh

Table 14-11472. MII_G_RT_FT3_n_P_MASK0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3310h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3310h + formula

Figure 14-3795. MII_G_RT_FT3_n_P_MASK0_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT3_n_P_MASK0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11474. MII_G_RT_FT3_n_P_MASK0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_n_P_MASK0	R/W	0h	Filter3 MP4:MP1 set to 1 to mask corresponding bit

41 MII_G_RT_FT3_n_P_MASK1_PRU0 Register (Offset = 314h + formula) [reset = 0h]

MII_G_RT_FT3_n_P_MASK1_PRU0 is shown in Figure 14-3796 and described in Table 14-7681.

Return to Summary Table.

Filter3 Mask1 (MP8:MP5).

Offset = 314h + (n * 10h); where n = 0h to Fh

Table 14-11475. MII_G_RT_FT3_n_P_MASK1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3314h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3314h + formula

Figure 14-3796. MII_G_RT_FT3_n_P_MASK1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_n_P_MASK1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11477. MII_G_RT_FT3_n_P_MASK1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_n_P_MASK1	R/W	0h	Filter3 MP8:MP5 set to 1 to mask corresponding bit

42 MII_G_RT_FT_RX_PTR_PRU0 Register (Offset = 408h) [reset = 0h]

MII_G_RT_FT_RX_PTR_PRU0 is shown in Figure 14-3797 and described in Table 14-7683.

Return to Summary Table.

RX Current Filter Byte Count (PRU0).

Table 14-11478. MII_G_RT_FT_RX_PTR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3408h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3408h

Figure 14-3797. MII_G_RT_FT_RX_PTR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT_RX_PTR_PRU0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11480. MII_G_RT_FT_RX_PTR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT_RX_PTR_PRU0	R/W	0h	RX current filter Byte Count

43 MII_G_RT_RX_CLASSm_AND_EN_PRU0 Register (Offset = 40Ch + formula) [reset = 0h]

MII_G_RT_RX_CLASSm_AND_EN_PRU0 is shown in Figure 14-3798 and described in Table 14-7685.

Return to Summary Table.

RX Class<m> AND Enable Register.

Offset = 40Ch + (m * 8h); where m = 0h to Fh

Table 14-11481. MII_G_RT_RX_CLASSm_AND_EN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 340Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 340Ch + formula

Figure 14-3798. MII_G_RT_RX_CLASSm_AND_EN_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASSm_AND_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11483. MII_G_RT_RX_CLASSm_AND_EN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CLASSm_AND_EN	R/W	0h	rx class AND enable

44 MII_G_RT_RX_CLASSm_OR_EN_PRU0 Register (Offset = 410h + formula) [reset = 0h]

MII_G_RT_RX_CLASSm_OR_EN_PRU0 is shown in Figure 14-3799 and described in Table 14-7687.

Return to Summary Table.

RX Class<m> OR Enable Register.

Offset = 410h + (m * 8h); where m = 0h to Fh

Table 14-11484. MII_G_RT_RX_CLASSm_OR_EN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3410h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3410h + formula

Figure 14-3799. MII_G_RT_RX_CLASSm_OR_EN_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">RX_CLASSm_OR_EN</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11486. MII_G_RT_RX_CLASSm_OR_EN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CLASSm_OR_EN	R/W	0h	rx class OR enable

45 MII_G_RT_RX_CLASS_CFG1_PRU0 Register (Offset = 48Ch) [reset = 0h]

MII_G_RT_RX_CLASS_CFG1_PRU0 is shown in Figure 14-3800 and described in Table 14-7689.

Return to Summary Table.

RX Class Configuration 1 Register.

Table 14-11487. MII_G_RT_RX_CLASS_CFG1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 348Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 348Ch

Figure 14-3800. MII_G_RT_RX_CLASS_CFG1_PRU0 Register

31	30	29	28	27	26	25	24
RX_CLASS15_SEL		RX_CLASS14_SEL		RX_CLASS13_SEL		RX_CLASS12_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
RX_CLASS11_SEL		RX_CLASS10_SEL		RX_CLASS9_SEL		RX_CLASS8_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RX_CLASS7_SEL		RX_CLASS6_SEL		RX_CLASS5_SEL		RX_CLASS4_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RX_CLASS3_SEL		RX_CLASS2_SEL		RX_CLASS1_SEL		RX_CLASS0_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11489. MII_G_RT_RX_CLASS_CFG1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_CLASS15_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
29-28	RX_CLASS14_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
27-26	RX_CLASS13_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
25-24	RX_CLASS12_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
23-22	RX_CLASS11_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND

Table 14-11489. MII_G_RT_RX_CLASS_CFG1_PRU0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	RX_CLASS10_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
19-18	RX_CLASS9_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
17-16	RX_CLASS8_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
15-14	RX_CLASS7_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
13-12	RX_CLASS6_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
11-10	RX_CLASS5_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
9-8	RX_CLASS4_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
7-6	RX_CLASS3_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
5-4	RX_CLASS2_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
3-2	RX_CLASS1_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
1-0	RX_CLASS0_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND

46 MII_G_RT_RX_CLASS_CFG2_PRU0 Register (Offset = 490h) [reset = 0h]

MII_G_RT_RX_CLASS_CFG2_PRU0 is shown in Figure 14-3801 and described in Table 14-7691.

Return to Summary Table.

RX Class Configuration 2 Register.

Table 14-11490. MII_G_RT_RX_CLASS_CFG2_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3490h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3490h

Figure 14-3801. MII_G_RT_RX_CLASS_CFG2_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASS_OR_NV																RX_CLASS_AND_NV															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11492. MII_G_RT_RX_CLASS_CFG2_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_CLASS_OR_NV	R/W	0h	RX class invert OR not invert enable
15-0	RX_CLASS_AND_NV	R/W	0h	RX class invert AND not invert enable

47 MII_G_RT_RX_CLASS_GATESm_PRU0 Register (Offset = 494h + formula) [reset = X]

MII_G_RT_RX_CLASS_GATESm_PRU0 is shown in Figure 14-3802 and described in Table 14-7693.

Return to Summary Table.

RX Class Gate<m> Configuration PRU0 Register.

Offset = 494h + (m * 4h); where m = 0h to Fh

Table 14-11493. MII_G_RT_RX_CLASS_GATESm_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3494h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3494h + formula

Figure 14-3802. MII_G_RT_RX_CLASS_GATESm_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>RX_RED_PHASE_ENm</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>RX_ALLOW_MASKm</td><td>RX_CLASS_RAW_MASKm</td><td>RX_PHASE_MASKm</td><td>RESERVED</td><td colspan="3">RX_RATE_GATE_SELm</td></tr>
<tr><td>R/W-X</td><td>R/W-1h</td><td>R/W-1h</td><td>R/W-1h</td><td>R/W-X</td><td colspan="3">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11495. MII_G_RT_RX_CLASS_GATESm_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_RED_PHASE_ENm	R/W	0h	red phase enable 0: disable 1: enable
7	RESERVED	R/W	X	
6	RX_ALLOW_MASKm	R/W	1h	allow mask 0: unmask 1: mask
5	RX_CLASS_RAW_MASKm	R/W	1h	class raw mask 0: unmask 1: mask
4	RX_PHASE_MASKm	R/W	1h	time phase mask 0: unmask 1: mask
3	RESERVED	R/W	X	
2-0	RX_RATE_GATE_SELm	R/W	0h	defines which rx_rate will gate rx_class

48 MII_G_RT_RX_GREEN_PRU0 Register (Offset = 4D4h) [reset = X]

MII_G_RT_RX_GREEN_PRU0 is shown in Figure 14-3803 and described in Table 14-7695.

Return to Summary Table.

RX Green Status PRU0.

Table 14-11496. MII_G_RT_RX_GREEN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 34D4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 34D4h

Figure 14-3803. MII_G_RT_RX_GREEN_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>RX_GREEN_VAL</td><td colspan="4">RX_GREEN_CMP_SEL</td></tr>
<tr><td colspan="3">R/W-X</td><td>R-0h</td><td colspan="4">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11498. MII_G_RT_RX_GREEN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	RX_GREEN_VAL	R	0h	0: RED, 1: GREEN status
3-0	RX_GREEN_CMP_SEL	R/W	0h	define which IEP CMP start green

49 MII_G_RT_SA_HASH_PRU0 Register (Offset = 4D8h) [reset = X]

MII_G_RT_SA_HASH_PRU0 is shown in Figure 14-3804 and described in Table 14-7697.

Return to Summary Table.

SA Hash Seed PRU0.

Table 14-11499. MII_G_RT_SA_HASH_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 34D8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 34D8h

Figure 14-3804. MII_G_RT_SA_HASH_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="10">SA_HASH_SEED</td></tr>
<tr><td colspan="6">R/W-X</td><td colspan="10">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11501. MII_G_RT_SA_HASH_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	SA_HASH_SEED	R/W	0h	SA Hash Seed

50 MII_G_RT_CONN_HASH_PRU0 Register (Offset = 4DCh) [reset = X]

MII_G_RT_CONN_HASH_PRU0 is shown in Figure 14-3805 and described in Table 14-7699.

Return to Summary Table.

Connection Hash Seed PRU0.

Table 14-11502. MII_G_RT_CONN_HASH_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 34DCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 34DCh

Figure 14-3805. MII_G_RT_CONN_HASH_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CONN_HASH_SEED									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11504. MII_G_RT_CONN_HASH_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	CONN_HASH_SEED	R/W	0h	Connection Hash Seed

51 MII_G_RT_CONN_HASH_START_PRU0 Register (Offset = 4E0h) [reset = X]

MII_G_RT_CONN_HASH_START_PRU0 is shown in Figure 14-3806 and described in Table 14-7701.

Return to Summary Table.

Connection Hash Start PRU0.

Table 14-11505. MII_G_RT_CONN_HASH_START_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 34E0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 34E0h

Figure 14-3806. MII_G_RT_CONN_HASH_START_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="17">RESERVED</td><td colspan="15">CONN_HASH_START</td></tr>
<tr><td colspan="17">R/W-X</td><td colspan="15">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11507. MII_G_RT_CONN_HASH_START_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-0	CONN_HASH_START	R/W	0h	Connection Hash Start which 4 Bytes to hash

52 MII_G_RT_RX_RATE_CFGn_PRU0 Register (Offset = 4E4h + formula) [reset = 0h]

MII_G_RT_RX_RATE_CFGn_PRU0 is shown in Figure 14-3807 and described in Table 14-7703.

Return to Summary Table.

RX Rate Configuration<n> Register.

Offset = 4E4h + (n * 4h); where n = 0h to 7h

Table 14-11508. MII_G_RT_RX_RATE_CFGn_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 34E4h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 34E4h + formula

Figure 14-3807. MII_G_RT_RX_RATE_CFGn_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_RATE_CIR_IDLEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11510. MII_G_RT_RX_RATE_CFGn_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_RATE_CIR_IDLEn	R/W	0h	RX Rate Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle including EOF. The PIR counter is disabled with a zero value and packets will not be marked RED

53 MII_G_RT_RX_RATE_SRC_SEL0_PRU0 Register (Offset = 504h) [reset = X]

MII_G_RT_RX_RATE_SRC_SEL0_PRU0 is shown in Figure 14-3808 and described in Table 14-7705.

Return to Summary Table.

RX Rate Source Select0.

Table 14-11511. MII_G_RT_RX_RATE_SRC_SEL0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3504h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3504h

Figure 14-3808. MII_G_RT_RX_RATE_SRC_SEL0_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED		RX_RATE_SRC_SEL3					
R/W-X		R/W-0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		RX_RATE_SRC_SEL2					
R/W-X		R/W-0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		RX_RATE_SRC_SEL1					
R/W-X		R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RX_RATE_SRC_SEL0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11513. MII_G_RT_RX_RATE_SRC_SEL0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RX_RATE_SRC_SEL3	R/W	0h	Map which filter/flag/class hit that rate logic uses, see **RX Rate hit Mapping**table for mapping
23-22	RESERVED	R/W	X	
21-16	RX_RATE_SRC_SEL2	R/W	0h	Map which filter/flag/class hit that rate logic uses, see **RX Rate hit Mapping**table for mapping
15-14	RESERVED	R/W	X	
13-8	RX_RATE_SRC_SEL1	R/W	0h	Map which filter/flag/class hit that rate logic uses, see **RX Rate hit Mapping**table for mapping
7-6	RESERVED	R/W	X	
5-0	RX_RATE_SRC_SEL0	R/W	0h	Map which filter/flag/class hit that rate logic uses, see **RX Rate hit Mapping**table for mapping

54 MII_G_RT_RX_RATE_SRC_SEL1_PRU0 Register (Offset = 508h) [reset = X]

MII_G_RT_RX_RATE_SRC_SEL1_PRU0 is shown in Figure 14-3809 and described in Table 14-7707.

Return to Summary Table.

RX Rate Source Select1.

Table 14-11514. MII_G_RT_RX_RATE_SRC_SEL1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3508h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3508h

Figure 14-3809. MII_G_RT_RX_RATE_SRC_SEL1_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED		RX_RATE_SRC_SEL7					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		RX_RATE_SRC_SEL6					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		RX_RATE_SRC_SEL5					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		RX_RATE_SRC_SEL4					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11516. MII_G_RT_RX_RATE_SRC_SEL1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RX_RATE_SRC_SEL7	R/W	0h	Map which filter/flag/class hit that rate logic uses, see **RX Rate hit Mapping**table for mapping
23-22	RESERVED	R/W	X	
21-16	RX_RATE_SRC_SEL6	R/W	0h	Map which filter/flag/class hit that rate logic uses, see **RX Rate hit Mapping**table for mapping
15-14	RESERVED	R/W	X	
13-8	RX_RATE_SRC_SEL5	R/W	0h	Map which filter/flag/class hit that rate logic uses, see **RX Rate hit Mapping**table for mapping
7-6	RESERVED	R/W	X	
5-0	RX_RATE_SRC_SEL4	R/W	0h	Map which filter/flag/class hit that rate logic uses, see **RX Rate hit Mapping**table for mapping

55 MII_G_RT_TX_RATE_CFG1_n_PRU0 Register (Offset = 50Ch + formula) [reset = 0h]

MII_G_RT_TX_RATE_CFG1_n_PRU0 is shown in Figure 14-3810 and described in Table 14-7709.

Return to Summary Table.

TX Rate Configuration1 Registe.

Offset = 50Ch + (n * 8h); where n = 0h to 7h

Table 14-11517. MII_G_RT_TX_RATE_CFG1_n_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 350Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 350Ch + formula

Figure 14-3810. MII_G_RT_TX_RATE_CFG1_n_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_RATE_CIR_IDLEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11519. MII_G_RT_TX_RATE_CFG1_n_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_RATE_CIR_IDLEn	R/W	0h	TX Rate Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle including EOF. The PIR counter is disabled with a zero value and packets will not be marked RED

56 MII_G_RT_TX_RATE_CFG2_n_PRU0 Register (Offset = 510h + formula) [reset = X]

MII_G_RT_TX_RATE_CFG2_n_PRU0 is shown in Figure 14-3811 and described in Table 14-7711.

Return to Summary Table.

TX Rate Configuration2 Register.

Offset = 510h + (n * 8h); where n = 0h to 7h

Table 14-11520. MII_G_RT_TX_RATE_CFG2_n_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3510h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3510h + formula

Figure 14-3811. MII_G_RT_TX_RATE_CFG2_n_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>TX_RATE_ALLOWn</td><td>TX_RATE_ENn</td></tr>
<tr><td colspan="6">R/W-X</td><td>R-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TX_RATE_LENn</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_RATE_LENn</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11522. MII_G_RT_TX_RATE_CFG2_n_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	TX_RATE_ALLOWn	R	0h	TX Rate Pkt Enable
16	TX_RATE_ENn	R/W	0h	TX Rate Pkt Enable
15-0	TX_RATE_LENn	R/W	0h	TX Rate Pkt Length

57 MII_G_RT_RX_STAT_GOOD_PRU0 Register (Offset = 54Ch + formula) [reset = 0h]

MII_G_RT_RX_STAT_GOOD_PRU0 is shown in Figure 14-3812 and described in Table 14-7713.

Return to Summary Table.

RX Good Frame Count (PRU0).

Table 14-11523. MII_G_RT_RX_STAT_GOOD_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 354Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 354Ch + formula

Figure 14-3812. MII_G_RT_RX_STAT_GOOD_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_GOOD_FRM_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11525. MII_G_RT_RX_STAT_GOOD_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_GOOD_FRM_CNT	R/W	0h	RX Good Frame Count Increment on none min err max err CRC err odd err, Write to subtract

58 MII_G_RT_RX_STAT_BC_PRU0 Register (Offset = 550h) [reset = X]

MII_G_RT_RX_STAT_BC_PRU0 is shown in Figure 14-3813 and described in Table 14-7715.

Return to Summary Table.

RX BC Frame Count (PRU0).

Table 14-11526. MII_G_RT_RX_STAT_BC_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3550h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3550h

Figure 14-3813. MII_G_RT_RX_STAT_BC_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_BC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11528. MII_G_RT_RX_STAT_BC_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_BC_FRM_CNT	R/W	0h	RX BC Frame Count Increment on BC type, Write to subtract

59 MII_G_RT_RX_STAT_MC_PRU0 Register (Offset = 554h) [reset = X]

MII_G_RT_RX_STAT_MC_PRU0 is shown in Figure 14-3814 and described in Table 14-7717.

Return to Summary Table.

RX MC Frame Count (PRU0).

Table 14-11529. MII_G_RT_RX_STAT_MC_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3554h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3554h

Figure 14-3814. MII_G_RT_RX_STAT_MC_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_MC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11531. MII_G_RT_RX_STAT_MC_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MC_FRM_CNT	R/W	0h	RX MC Frame Count Increment on MC type, Write to subtract

60 MII_G_RT_RX_STAT_CRC_ERR_PRU0 Register (Offset = 558h) [reset = X]

MII_G_RT_RX_STAT_CRC_ERR_PRU0 is shown in Figure 14-3815 and described in Table 14-7719.

Return to Summary Table.

RX CRC Error Frame Count (PRU0).

Table 14-11532. MII_G_RT_RX_STAT_CRC_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3558h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3558h

Figure 14-3815. MII_G_RT_RX_STAT_CRC_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CRC_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11534. MII_G_RT_RX_STAT_CRC_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_CRC_ERR_FRM_CNT	R/W	0h	RX CRC Err Frame Count Increment on CRC error, Write to subtract

61 MII_G_RT_RX_STAT_MII_ERR_PRU0 Register (Offset = 55Ch) [reset = X]

MII_G_RT_RX_STAT_MII_ERR_PRU0 is shown in Figure 14-3816 and described in Table 14-7721.

Return to Summary Table.

RX MII Error Frame Count (PRU0).

Table 14-11535. MII_G_RT_RX_STAT_MII_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 355Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 355Ch

Figure 14-3816. MII_G_RT_RX_STAT_MII_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MII_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11537. MII_G_RT_RX_STAT_MII_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MII_ERR_FRM_CNT	R/W	0h	RX MII Err Frame Count Increment on MII, SGMII, RGMII error, Write to subtract

62 MII_G_RT_RX_STAT_ODD_ERR_PRU0 Register (Offset = 560h) [reset = X]

MII_G_RT_RX_STAT_ODD_ERR_PRU0 is shown in Figure 14-3817 and described in Table 14-7723.

Return to Summary Table.

RX Odd Nibble Frame Count (PRU0).

Table 14-11538. MII_G_RT_RX_STAT_ODD_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3560h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3560h

Figure 14-3817. MII_G_RT_RX_STAT_ODD_ERR_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RX_ODD_ERR_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11540. MII_G_RT_RX_STAT_ODD_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_ODD_ERR_FRM_CNT	R/W	0h	RX Odd Nibble Frame Count Increment on odd nibble MII, Write to subtract

63 MII_G_RT_RX_STAT_MAX_SIZE_PRU0 Register (Offset = 564h) [reset = X]

MII_G_RT_RX_STAT_MAX_SIZE_PRU0 is shown in Figure 14-3818 and described in Table 14-7725.

Return to Summary Table.

RX Max Size Frame Count (PRU0).

Table 14-11541. MII_G_RT_RX_STAT_MAX_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3564h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3564h

Figure 14-3818. MII_G_RT_RX_STAT_MAX_SIZE_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_MAX_SIZE_FRM</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-7D0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11543. MII_G_RT_RX_STAT_MAX_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MAX_SIZE_FRM	R/W	7D0h	RX MAX Size Frame Count Limit

64 MII_G_RT_RX_STAT_MAX_ERR_PRU0 Register (Offset = 568h) [reset = X]

MII_G_RT_RX_STAT_MAX_ERR_PRU0 is shown in Figure 14-3819 and described in Table 14-7727.

Return to Summary Table.

RX Max Size Error Frame Count (PRU0).

Table 14-11544. MII_G_RT_RX_STAT_MAX_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3568h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3568h

Figure 14-3819. MII_G_RT_RX_STAT_MAX_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_MAX_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11546. MII_G_RT_RX_STAT_MAX_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MAX_ERR_FRM_CNT	R/W	0h	RX MAX Size Err Frame Count Increment if > than Limit, Write to subtract

65 MII_G_RT_RX_STAT_MIN_SIZE_PRU0 Register (Offset = 56Ch) [reset = X]

MII_G_RT_RX_STAT_MIN_SIZE_PRU0 is shown in Figure 14-3820 and described in Table 14-7729.

Return to Summary Table.

RX Min Size Frame Count (PRU0).

Table 14-11547. MII_G_RT_RX_STAT_MIN_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 356Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 356Ch

Figure 14-3820. MII_G_RT_RX_STAT_MIN_SIZE_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_MIN_SIZE_FRM</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-40h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11549. MII_G_RT_RX_STAT_MIN_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MIN_SIZE_FRM	R/W	40h	RX MIN Size Frame Limit

66 MII_G_RT_RX_STAT_MIN_ERR_PRU0 Register (Offset = 570h) [reset = X]

MII_G_RT_RX_STAT_MIN_ERR_PRU0 is shown in Figure 14-3821 and described in Table 14-7731.

Return to Summary Table.

RX Min Size Error Frame Count (PRU0).

Table 14-11550. MII_G_RT_RX_STAT_MIN_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3570h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3570h

Figure 14-3821. MII_G_RT_RX_STAT_MIN_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_MIN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11552. MII_G_RT_RX_STAT_MIN_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MIN_ERR_FRM_CNT	R/W	0h	RX MIN Size Frame Count Increment if < than limit, Write to subtract

67 MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 Register (Offset = 574h) [reset = X]

MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 is shown in Figure 14-3822 and described in Table 14-7733.

Return to Summary Table.

RX Overrun Frame Count (PRU0).

Table 14-11553. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3574h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3574h

Figure 14-3822. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_OVERRUN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11555. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_OVERRUN_ERR_FRM_CNT	R/W	0h	RX L1 FIFO overflow Frame Count. Increment on overflow event, Write to subtract

68 MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 Register (Offset = 578h + formula) [reset = 0h]

MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 is shown in Figure 14-3823 and described in Table 14-7735.

Return to Summary Table.

RX Class<m> Hit.

Offset = 578h + (n * 4h); where m = 0h to Fh

Table 14-11556. MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3578h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3578h + formula

Figure 14-3823. MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_CLASSm_PRU0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11558. MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_STAT_CLASSm_PRU0	R/W	0h	RX Class<m> Hit Count (where m = 0 to 15). Write to subtract

69 MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Register (Offset = 5B8h) [reset = 0h]

MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 is shown in Figure 14-3824 and described in Table 14-7737.

Return to Summary Table.

RX SMD Frag Error Count PRU0.

Table 14-11559. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35B8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35B8h

Figure 14-3824. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_STAT_SMD_ERR_PRU0</td><td colspan="8">RX_STAT_FRAG_ERR_PRU0</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RX_STAT_SMDC_ERR_PRU0</td><td colspan="8">RX_STAT_SMDS_ERR_PRU0</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11561. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_STAT_SMD_ERR_PRU0	R/W	0h	RX SMDS Error Count, Increment when first none 0x55 does not match any valid SMD, Write to subtract
23-16	RX_STAT_FRAG_ERR_PRU0	R/W	0h	RX Frag_Cnt Seq Error Count, Write to subtract
15-8	RX_STAT_SMDC_ERR_PRU0	R/W	0h	RX SMDCx Seq Error Count, Write to subtract
7-0	RX_STAT_SMDS_ERR_PRU0	R/W	0h	RX SMDSx Seq Error Count, Write to subtract

70 MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 Register (Offset = 5BCh) [reset = X]

MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 is shown in Figure 14-3825 and described in Table 14-7739.

Return to Summary Table.

RX Bucket1 Size Configuration (PRU0).

Table 14-11562. MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35BCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35BCh

Figure 14-3825. MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RX_STAT_BKT1_SIZE													
R/W-X		R/W-40h													

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11564. MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT1_SIZE	R/W	40h	RX Bucket1 Byte Size

71 MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 Register (Offset = 5C0h) [reset = X]

MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 is shown in Figure 14-3826 and described in Table 14-7741.

Return to Summary Table.

RX Bucket2 Size Configuration (PRU0).

Table 14-11565. MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35C0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35C0h

Figure 14-3826. MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT2_SIZE													
R/W-X		R/W-80h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11567. MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT2_SIZE	R/W	80h	RX Bucket2 Byte Size

72 MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 Register (Offset = 5C4h) [reset = X]

MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 is shown in Figure 14-3827 and described in Table 14-7743.

Return to Summary Table.

RX Bucket3 Size Configuration (PRU0).

Table 14-11568. MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35C4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35C4h

Figure 14-3827. MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT3_SIZE													
R/W-X		R/W-100h													

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11570. MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT3_SIZE	R/W	100h	RX Bucket3 Byte Size

73 MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 Register (Offset = 5C8h) [reset = X]

MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 is shown in Figure 14-3828 and described in Table 14-7745.

Return to Summary Table.

RX Bucket4 Size Configuration (PRU0).

Table 14-11571. MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35C8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35C8h

Figure 14-3828. MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="14">RX_STAT_BKT4_SIZE</td></tr>
<tr><td colspan="2">R/W-X</td><td colspan="14">R/W-200h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11573. MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT4_SIZE	R/W	200h	RX Bucket4 Byte Size

74 MII_G_RT_RX_STAT_64_PRU0 Register (Offset = 5CCh) [reset = X]

MII_G_RT_RX_STAT_64_PRU0 is shown in Figure 14-3829 and described in Table 14-7747.

Return to Summary Table.

RX 64B Sized Frame Count (PRU0).

Table 14-11574. MII_G_RT_RX_STAT_64_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35CCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35CCh

Figure 14-3829. MII_G_RT_RX_STAT_64_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_64_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11576. MII_G_RT_RX_STAT_64_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_64_FRM_CNT	R/W	0h	RX 64 Byte Frame Count Increment if 64 B size

75 MII_G_RT_RX_STAT_BKT1_PRU0 Register (Offset = 5D0h) [reset = X]

MII_G_RT_RX_STAT_BKT1_PRU0 is shown in Figure 14-3830 and described in Table 14-7749.

Return to Summary Table.

RX Bucket1 Sized Frame Count (PRU0).

Table 14-11577. MII_G_RT_RX_STAT_BKT1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35D0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35D0h

Figure 14-3830. MII_G_RT_RX_STAT_BKT1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11579. MII_G_RT_RX_STAT_BKT1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT1	R/W	0h	RX Bucket1 Frame Count Increment if <= than Bucket1 Byte Size

76 MII_G_RT_RX_STAT_BKT2_PRU0 Register (Offset = 5D4h) [reset = X]

MII_G_RT_RX_STAT_BKT2_PRU0 is shown in Figure 14-3831 and described in Table 14-7751.

Return to Summary Table.

RX Bucket2 Sized Frame Count (PRU0).

Table 14-11580. MII_G_RT_RX_STAT_BKT2_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35D4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35D4h

Figure 14-3831. MII_G_RT_RX_STAT_BKT2_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11582. MII_G_RT_RX_STAT_BKT2_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT2	R/W	0h	RX Bucket2 Frame Count Increment if <= than Bucket2 Byte Size and if > than Bucket1 Byte Size

77 MII_G_RT_RX_STAT_BKT3_PRU0 Register (Offset = 5D8h) [reset = X]

MII_G_RT_RX_STAT_BKT3_PRU0 is shown in Figure 14-3832 and described in Table 14-7753.

Return to Summary Table.

RX Bucket3 Sized Frame Count (PRU0).

Table 14-11583. MII_G_RT_RX_STAT_BKT3_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35D8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35D8h

Figure 14-3832. MII_G_RT_RX_STAT_BKT3_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11585. MII_G_RT_RX_STAT_BKT3_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT3	R/W	0h	RX Bucket3 Frame Count Increment if <= than Bucket3 Byte Size and if > than Bucket2 Byte Size

78 MII_G_RT_RX_STAT_BKT4_PRU0 Register (Offset = 5DCh) [reset = X]

MII_G_RT_RX_STAT_BKT4_PRU0 is shown in Figure 14-3833 and described in Table 14-7755.

Return to Summary Table.

RX Bucket4 Sized Frame Count (PRU0).

Table 14-11586. MII_G_RT_RX_STAT_BKT4_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35DCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35DCh

Figure 14-3833. MII_G_RT_RX_STAT_BKT4_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_STAT_BKT4</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11588. MII_G_RT_RX_STAT_BKT4_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT4	R/W	0h	RX Bucket4 Frame Count Increment if <= than Bucket4 Byte Size and if > than Bucket3 Byte Size

79 MII_G_RT_RX_STAT_BKT5_PRU0 Register (Offset = 5E0h) [reset = X]

MII_G_RT_RX_STAT_BKT5_PRU0 is shown in Figure 14-3834 and described in Table 14-7757.

Return to Summary Table.

RX Bucket5 Sized Frame Count (PRU0).

Table 14-11589. MII_G_RT_RX_STAT_BKT5_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35E0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35E0h

Figure 14-3834. MII_G_RT_RX_STAT_BKT5_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_STAT_BKT5</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11591. MII_G_RT_RX_STAT_BKT5_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT5	R/W	0h	RX Bucket5 Frame Count Increment if > than Bucket4 Byte Size

80 MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 Register (Offset = 5E4h) [reset = 0h]

MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 is shown in Figure 14-3835 and described in Table 14-7759.

Return to Summary Table.

RX Total Byte Count (PRU0).

Table 14-11592. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35E4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35E4h

Figure 14-3835. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">RX_STAT_TOTAL_BYTES_PRU</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11594. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_STAT_TOTAL_BYTES_PRU	R/W	0h	RX Total Byte Count

81 MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Register (Offset = 5E8h) [reset = 0h]

MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 is shown in Figure 14-3836 and described in Table 14-7761.

Return to Summary Table.

RX TX Total Byte Count (PRU0).

Table 14-11595. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35E8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35E8h

Figure 14-3836. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">RXTX_STAT_TOTAL_BYTES_PRU</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11597. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RXTX_STAT_TOTAL_BYTES_PRU	R/W	0h	RX and TX Total Byte Count

82 MII_G_RT_TX_STAT_GOOD_PORT0 Register (Offset = 5ECh) [reset = 0h]

MII_G_RT_TX_STAT_GOOD_PORT0 is shown in Figure 14-3837 and described in Table 14-7763.

Return to Summary Table.

TX Good Frame Count Port0.

Table 14-11598. MII_G_RT_TX_STAT_GOOD_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35ECh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35ECh

Figure 14-3837. MII_G_RT_TX_STAT_GOOD_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_GOOD_FRM_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11600. MII_G_RT_TX_STAT_GOOD_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_GOOD_FRM_CNT	R/W	0h	TX Good Frame Count Increment if no min size err max size err or MII odd nibble

83 MII_G_RT_TX_STAT_BC_PORT0 Register (Offset = 5F0h) [reset = X]

MII_G_RT_TX_STAT_BC_PORT0 is shown in Figure 14-3838 and described in Table 14-7765.

Return to Summary Table.

TX BC Frame Count Port0.

Table 14-11601. MII_G_RT_TX_STAT_BC_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35F0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35F0h

Figure 14-3838. MII_G_RT_TX_STAT_BC_PORT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_BC_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11603. MII_G_RT_TX_STAT_BC_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_BC_FRM_CNT	R/W	0h	TX BC Frame Count Increment if BC

84 MII_G_RT_TX_STAT_MC_PORT0 Register (Offset = 5F4h) [reset = X]

MII_G_RT_TX_STAT_MC_PORT0 is shown in Figure 14-3839 and described in Table 14-7767.

Return to Summary Table.

TX MC Frame Count Port0.

Table 14-11604. MII_G_RT_TX_STAT_MC_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35F4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35F4h

Figure 14-3839. MII_G_RT_TX_STAT_MC_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11606. MII_G_RT_TX_STAT_MC_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MC_FRM_CNT	R/W	0h	TX MC Frame Count. Increment if MC

85 MII_G_RT_TX_STAT_ODD_ERR_PORT0 Register (Offset = 5F8h) [reset = X]

MII_G_RT_TX_STAT_ODD_ERR_PORT0 is shown in Figure 14-3840 and described in Table 14-7769.

Return to Summary Table.

TX Odd Nibble Frame Count Port0.

Table 14-11607. MII_G_RT_TX_STAT_ODD_ERR_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35F8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35F8h

Figure 14-3840. MII_G_RT_TX_STAT_ODD_ERR_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_ODD_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11609. MII_G_RT_TX_STAT_ODD_ERR_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_ODD_ERR_FRM_CNT	R/W	0h	TX Odd Nibble Frame Count Increment if MII odd nibble

86 MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Register (Offset = 5FCh) [reset = X]

MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 is shown in Figure 14-3841 and described in Table 14-7771.

Return to Summary Table.

TX Under Flow Error Count Port0.

Table 14-11610. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 35FCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 35FCh

Figure 14-3841. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_UNDERFLOW_CNT</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11612. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_UNDERFLOW_CNT	R/W	0h	TX MAX Underflow Error Cnt

87 MII_G_RT_TX_STAT_MAX_SIZE_PORT0 Register (Offset = 600h) [reset = X]

MII_G_RT_TX_STAT_MAX_SIZE_PORT0 is shown in Figure 14-3842 and described in Table 14-7773.

Return to Summary Table.

TX Max Size Frame Port0.

Table 14-11613. MII_G_RT_TX_STAT_MAX_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3600h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3600h

Figure 14-3842. MII_G_RT_TX_STAT_MAX_SIZE_PORT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_MAX_SIZE_FRM</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-7D0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11615. MII_G_RT_TX_STAT_MAX_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MAX_SIZE_FRM	R/W	7D0h	TX MAX Size Frame Count Limit

88 MII_G_RT_TX_STAT_MAX_ERR_PORT0 Register (Offset = 604h) [reset = X]

MII_G_RT_TX_STAT_MAX_ERR_PORT0 is shown in Figure 14-3843 and described in Table 14-7775.

Return to Summary Table.

TX Max Size Error Frame Count Port0.

Table 14-11616. MII_G_RT_TX_STAT_MAX_ERR_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3604h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3604h

Figure 14-3843. MII_G_RT_TX_STAT_MAX_ERR_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_MAX_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11618. MII_G_RT_TX_STAT_MAX_ERR_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MAX_ERR_FRM_CNT	R/W	0h	TX MAX Size Err Frame Count Increment if > max Limit

89 MII_G_RT_TX_STAT_MIN_SIZE_PORT0 Register (Offset = 608h) [reset = X]

MII_G_RT_TX_STAT_MIN_SIZE_PORT0 is shown in Figure 14-3844 and described in Table 14-7777.

Return to Summary Table.

TX Min Size Frame Port0.

Table 14-11619. MII_G_RT_TX_STAT_MIN_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3608h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3608h

Figure 14-3844. MII_G_RT_TX_STAT_MIN_SIZE_PORT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_MIN_SIZE_FRM</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-40h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11621. MII_G_RT_TX_STAT_MIN_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MIN_SIZE_FRM	R/W	40h	TX MIN Size Frame Count Limit

90 MII_G_RT_TX_STAT_MIN_ERR_PORT0 Register (Offset = 60Ch) [reset = X]

MII_G_RT_TX_STAT_MIN_ERR_PORT0 is shown in Figure 14-3845 and described in Table 14-7779.

Return to Summary Table.

TX Min Size ErrorFrame Count Port0.

Table 14-11622. MII_G_RT_TX_STAT_MIN_ERR_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 360Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 360Ch

Figure 14-3845. MII_G_RT_TX_STAT_MIN_ERR_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MIN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11624. MII_G_RT_TX_STAT_MIN_ERR_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MIN_ERR_FRM_CNT	R/W	0h	TX MIN Size Err Frame Count Increment if < min Limit

91 MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 Register (Offset = 610h) [reset = X]

MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 is shown in Figure 14-3846 and described in Table 14-7781.

Return to Summary Table.

TX Bucket1 Size Configuration Port0.

Table 14-11625. MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3610h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3610h

Figure 14-3846. MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT1_SIZE													
R/W-X		R/W-40h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11627. MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT1_SIZE	R/W	40h	TX Bucket1 Byte Size

92 MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 Register (Offset = 614h) [reset = X]

MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 is shown in Figure 14-3847 and described in Table 14-7783.

Return to Summary Table.

TX Bucket2 Size Configuration Port0.

Table 14-11628. MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3614h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3614h

Figure 14-3847. MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="14">TX_STAT_BKT2_SIZE</td></tr>
<tr><td colspan="2">R/W-X</td><td colspan="14">R/W-80h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11630. MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT2_SIZE	R/W	80h	TX Bucket2 Byte Size

93 MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 Register (Offset = 618h) [reset = X]

MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 is shown in Figure 14-3848 and described in Table 14-7785.

Return to Summary Table.

TX Bucket3 Size Configuration Port0.

Table 14-11631. MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3618h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3618h

Figure 14-3848. MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT3_SIZE													
R/W-X		R/W-100h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11633. MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT3_SIZE	R/W	100h	TX Bucket3 Byte Size

94 MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 Register (Offset = 61Ch) [reset = X]

MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 is shown in Figure 14-3849 and described in Table 14-7787.

Return to Summary Table.

TX Bucket4 Size Configuration Port0.

Table 14-11634. MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 361Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 361Ch

Figure 14-3849. MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT4_SIZE													
R/W-X		R/W-200h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11636. MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT4_SIZE	R/W	200h	TX Bucket4 Byte Size

95 MII_G_RT_TX_STAT_64_PORT0 Register (Offset = 620h) [reset = X]

MII_G_RT_TX_STAT_64_PORT0 is shown in Figure 14-3850 and described in Table 14-7789.

Return to Summary Table.

TX 64B Sized Frame Count Port0.

Table 14-11637. MII_G_RT_TX_STAT_64_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3620h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3620h

Figure 14-3850. MII_G_RT_TX_STAT_64_PORT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_64_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11639. MII_G_RT_TX_STAT_64_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_64_FRM_CNT	R/W	0h	TX 64 Byte Frame Count. Increment if 64 B

96 MII_G_RT_TX_STAT_BKT1_PORT0 Register (Offset = 624h) [reset = X]

MII_G_RT_TX_STAT_BKT1_PORT0 is shown in Figure 14-3851 and described in Table 14-7791.

Return to Summary Table.

TX Bucket1 Sized Frame Count Port0.

Table 14-11640. MII_G_RT_TX_STAT_BKT1_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3624h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3624h

Figure 14-3851. MII_G_RT_TX_STAT_BKT1_PORT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_STAT_BKT1</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11642. MII_G_RT_TX_STAT_BKT1_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT1	R/W	0h	TX Bucket1 Increment if <= than Bucket1

97 MII_G_RT_TX_STAT_BKT2_PORT0 Register (Offset = 628h) [reset = X]

MII_G_RT_TX_STAT_BKT2_PORT0 is shown in Figure 14-3852 and described in Table 14-7793.

Return to Summary Table.

TX Bucket2 Sized Frame Count Port0.

Table 14-11643. MII_G_RT_TX_STAT_BKT2_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3628h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3628h

Figure 14-3852. MII_G_RT_TX_STAT_BKT2_PORT0 Register

31-16	15-0
RESERVED	TX_STAT_BKT2
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11645. MII_G_RT_TX_STAT_BKT2_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT2	R/W	0h	TX Bucket2 Increment if <= than Bucket2 Byte Size and if > than Bucket1 Byte Size

98 MII_G_RT_TX_STAT_BKT3_PORT0 Register (Offset = 62Ch) [reset = X]

MII_G_RT_TX_STAT_BKT3_PORT0 is shown in Figure 14-3853 and described in Table 14-7795.

Return to Summary Table.

TX Bucket3 Sized Frame Count Port0.

Table 14-11646. MII_G_RT_TX_STAT_BKT3_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 362Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 362Ch

Figure 14-3853. MII_G_RT_TX_STAT_BKT3_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11648. MII_G_RT_TX_STAT_BKT3_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT3	R/W	0h	TX Bucket3 Increment if <= than Bucket3 Byte Size and if > than Bucket2 Byte Size

99 MII_G_RT_TX_STAT_BKT4_PORT0 Register (Offset = 630h) [reset = X]

MII_G_RT_TX_STAT_BKT4_PORT0 is shown in Figure 14-3854 and described in Table 14-7797.

Return to Summary Table.

TX Bucket4 Sized Frame Count Port0.

Table 14-11649. MII_G_RT_TX_STAT_BKT4_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3630h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3630h

Figure 14-3854. MII_G_RT_TX_STAT_BKT4_PORT0 Register

31-16	15-0
RESERVED	TX_STAT_BKT4
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11651. MII_G_RT_TX_STAT_BKT4_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT4	R/W	0h	TX Bucket4 Increment if <= than Bucket4 Byte Size and if > than Bucket3 Byte Size

100 MII_G_RT_TX_STAT_BKT5_PORT0 Register (Offset = 634h) [reset = X]

MII_G_RT_TX_STAT_BKT5_PORT0 is shown in Figure 14-3855 and described in Table 14-7799.

Return to Summary Table.

TX Bucket5 Sized Frame Count Port0.

Table 14-11652. MII_G_RT_TX_STAT_BKT5_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3634h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3634h

Figure 14-3855. MII_G_RT_TX_STAT_BKT5_PORT0 Register

31-16	15-0
RESERVED	TX_STAT_BKT5
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11654. MII_G_RT_TX_STAT_BKT5_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT5	R/W	0h	TX Bucket5 Increment if > than Bucket4 Byte Size

101 MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 Register (Offset = 638h) [reset = 0h]

MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 is shown in Figure 14-3856 and described in Table 14-7801.

Return to Summary Table.

TX Total Byte Count Port0.

Table 14-11655. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3638h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3638h

Figure 14-3856. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">TX_TOTAL_STAT_BYTES_PORT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11657. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_TOTAL_STAT_BYTES_PORT	R/W	0h	TX Total Byte Count of all Frames

102 MII_G_RT_TX_HSR_TAG_PORT0 Register (Offset = 63Ch) [reset = 892Fh]

MII_G_RT_TX_HSR_TAG_PORT0 is shown in Figure 14-3857 and described in Table 14-7803.

Return to Summary Table.

TX HSR TAG Port0.

Table 14-11658. MII_G_RT_TX_HSR_TAG_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 363Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 363Ch

Figure 14-3857. MII_G_RT_TX_HSR_TAG_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_HSR_TAG																															
R/W-892Fh																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11660. MII_G_RT_TX_HSR_TAG_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_HSR_TAG	R/W	892Fh	HSR TAG

103 MII_G_RT_TX_HSR_SEQ_PORT0 Register (Offset = 640h) [reset = X]

MII_G_RT_TX_HSR_SEQ_PORT0 is shown in Figure 14-3858 and described in Table 14-7805.

Return to Summary Table.

TX HSR Seq Port0.

Table 14-11661. MII_G_RT_TX_HSR_SEQ_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3640h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3640h

Figure 14-3858. MII_G_RT_TX_HSR_SEQ_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_HSR_SEQ															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11663. MII_G_RT_TX_HSR_SEQ_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_HSR_SEQ	R/W	0h	HSR Seq count. It will incr for every HSR type

104 MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 Register (Offset = 644h) [reset = X]

MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 is shown in Figure 14-3859 and described in Table 14-7807.

Return to Summary Table.

TX VLAN Type TAG Port0.

Table 14-11664. MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3644h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3644h

Figure 14-3859. MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_VLAN_TYPE_TAG</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-81h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11666. MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_VLAN_TYPE_TAG	R/W	81h	TX VLAN Type Tag, match to enable VLAN removal

105 MII_G_RT_TX_VLAN_INS_TAG_PORT0 Register (Offset = 648h) [reset = 1h]

MII_G_RT_TX_VLAN_INS_TAG_PORT0 is shown in Figure 14-3860 and described in Table 14-7809.

Return to Summary Table.

TX VLAN Insertion TAG Port0.

Table 14-11667. MII_G_RT_TX_VLAN_INS_TAG_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3648h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3648h

Figure 14-3860. MII_G_RT_TX_VLAN_INS_TAG_PORT0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TX_VLAN_INS_TAG</td></tr>
<tr><td colspan="32">R/W-1h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11669. MII_G_RT_TX_VLAN_INS_TAG_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_VLAN_INS_TAG	R/W	1h	TX VLAN Insertion

106 MII_G_RT_FT1_START_LEN_PRU1 Register (Offset = 64Ch) [reset = X]

MII_G_RT_FT1_START_LEN_PRU1 is shown in Figure 14-3861 and described in Table 14-7811.

Return to Summary Table.

Filter1 Start and Length (PRU1).

Table 14-11670. MII_G_RT_FT1_START_LEN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 364Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 364Ch

Figure 14-3861. MII_G_RT_FT1_START_LEN_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				FT1_LEN			
R/W-X				R/W-6h			
15	14	13	12	11	10	9	8
RESERVED	FT1_START						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FT1_START							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11672. MII_G_RT_FT1_START_LEN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	FT1_LEN	R/W	6h	Defines the total number of Bytes Filter1 will check before Valid bit is set
15	RESERVED	R/W	X	
14-0	FT1_START	R/W	0h	Byte count start for Filter1. Any write will clear all Filter1 Status Bits

107 MII_G_RT_FT1_CFG_PRU1 Register (Offset = 650h) [reset = X]

MII_G_RT_FT1_CFG_PRU1 is shown in Figure 14-3862 and described in Table 14-7813.

Return to Summary Table.

Filter1 Configuration (PRU1).

Table 14-11673. MII_G_RT_FT1_CFG_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3650h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3650h

Figure 14-3862. MII_G_RT_FT1_CFG_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
FT1_7CFG		FT1_6CFG		FT1_5CFG		FT1_4CFG	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	
7	6	5	4	3	2	1	0
FT1_3CFG		FT1_2CFG		FT1_1CFG		FT1_0CFG	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11675. MII_G_RT_FT1_CFG_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	FT1_7CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
13-12	FT1_6CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
11-10	FT1_5CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
9-8	FT1_4CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
7-6	FT1_3CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
5-4	FT1_2CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than

Table 14-11675. MII_G_RT_FT1_CFG_PRU1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	FT1_1CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
1-0	FT1_0CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than

108 MII_G_RT_FT1_k_DA0_PRU1 Register (Offset = 654h + formula) [reset = 0h]

MII_G_RT_FT1_k_DA0_PRU1 is shown in Figure 14-3863 and described in Table 14-7815.

Return to Summary Table.

Filter1<k> DA0 (PRU1).

Offset = 654h + (k * 10h); where k = 0h to 7h

Table 14-11676. MII_G_RT_FT1_k_DA0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3654h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3654h + formula

Figure 14-3863. MII_G_RT_FT1_k_DA0_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT1_k_DA0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11678. MII_G_RT_FT1_k_DA0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT1_k_DA0	R/W	0h	Filter1 DA4:DA1

109 MII_G_RT_FT1_k_DA1_PRU1 Register (Offset = 658h + formula) [reset = X]

MII_G_RT_FT1_k_DA1_PRU1 is shown in Figure 14-3864 and described in Table 14-7817.

Return to Summary Table.

Filter1<k> DA1 (PRU1).

Offset = 658h + (k * 10h); where k = 0h to 7h

Table 14-11679. MII_G_RT_FT1_k_DA1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3658h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3658h + formula

Figure 14-3864. MII_G_RT_FT1_k_DA1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT1_k_DA1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11681. MII_G_RT_FT1_k_DA1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FT1_k_DA1	R/W	0h	Filter1 DA6:DA5

110 MII_G_RT_FT1_k_DA_MASK0_PRU1 Register (Offset = 65Ch + formula) [reset = 0h]

MII_G_RT_FT1_k_DA_MASK0_PRU1 is shown in Figure 14-3865 and described in Table 14-7819.

Return to Summary Table.

Filter1<k> DA0 Mask (PRU1).

Offset = 65Ch + (k * 10h); where k = 0h to 7h

Table 14-11682. MII_G_RT_FT1_k_DA_MASK0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 365Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 365Ch + formula

Figure 14-3865. MII_G_RT_FT1_k_DA_MASK0_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT1_k_DA_MASK0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11684. MII_G_RT_FT1_k_DA_MASK0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT1_k_DA_MASK0	R/W	0h	Filter1 MDA4:MDA1 set to 1 to mask corresponding bit

111 MII_G_RT_FT1_k_DA_MASK1_PRU1 Register (Offset = 660h + formula) [reset = X]

MII_G_RT_FT1_k_DA_MASK1_PRU1 is shown in Figure 14-3866 and described in Table 14-7821.

Return to Summary Table.

Filter1<k> DA1 Mask (PRU1).

Offset = 660h + (k * 10h); where k = 0h to 7h

Table 14-11685. MII_G_RT_FT1_k_DA_MASK1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3660h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3660h + formula

Figure 14-3866. MII_G_RT_FT1_k_DA_MASK1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT1_k_DA_MASK1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11687. MII_G_RT_FT1_k_DA_MASK1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FT1_k_DA_MASK1	R/W	0h	Filter1 MDA6:MDA5 set to 1 to mask corresponding bit

112 MII_G_RT_FT3_m_START_PRU1 Register (Offset = 6D4h + formula) [reset = X]

MII_G_RT_FT3_m_START_PRU1 is shown in Figure 14-3867 and described in Table 14-7823.

Return to Summary Table.

Filter3<m> Start (PRU1).

Offset = 6D4h + (m * 20h); where m = 0h to Fh

Table 14-11688. MII_G_RT_FT3_m_START_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 36D4h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 36D4h + formula

Figure 14-3867. MII_G_RT_FT3_m_START_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	FT3_START														
R/W-X																	R/W-Ch														

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11690. MII_G_RT_FT3_m_START_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-0	FT3_START	R/W	Ch	Byte count start for Filter3. Any write will clear all Filter3 Status Bits SW can read to determine next start during Auto

113 MII_G_RT_FT3_m_START_AUTO_PRU1 Register (Offset = 6D8h + formula) [reset = X]

MII_G_RT_FT3_m_START_AUTO_PRU1 is shown in Figure 14-3868 and described in Table 14-7825.

Return to Summary Table.

Filter3<m> Start Auto (PRU1).

Offset = 6D8h + (m * 20h); where m = 0h to Fh

Table 14-11691. MII_G_RT_FT3_m_START_AUTO_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 36D8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 36D8h + formula

Figure 14-3868. MII_G_RT_FT3_m_START_AUTO_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="17">RESERVED</td><td colspan="15">FT3_START_AUTO</td></tr>
<tr><td colspan="17">R-X</td><td colspan="15">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11693. MII_G_RT_FT3_m_START_AUTO_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	X	
14-0	FT3_START_AUTO	R	0h	Byte count start for Auto skip mode

114 MII_G_RT_FT3_m_START_LEN_PRU1 Register (Offset = 6DCh + formula) [reset = X]

MII_G_RT_FT3_m_START_LEN_PRU1 is shown in Figure 14-3869 and described in Table 14-7827.

Return to Summary Table.

Filter3<m> Start offset (PRU1).

Offset = 6DCh + (m * 20h); where m = 0h to Fh

Table 14-11694. MII_G_RT_FT3_m_START_LEN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 36DCh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 36DCh + formula

Figure 14-3869. MII_G_RT_FT3_m_START_LEN_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	FT3_OFFSET_END			RESERVED	FT3_OFFSET_START		
R/W-X	R/W-0h			R/W-X	R/W-0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	FT3_OFFSET						
R/W-X	R/W-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FT3_OFFSET							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11696. MII_G_RT_FT3_m_START_LEN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-20	FT3_OFFSET_END	R/W	0h	Defines which byte within FT3_[N]P[63:0] to end the compare at set the Valid flag, rule ft3_offset_end >= ft3_offset_start To disable pattern compare set start and end to zero
19	RESERVED	R/W	X	
18-16	FT3_OFFSET_START	R/W	0h	Defines which byte within FT3_[N]P[63:0] to start the compare
15	RESERVED	R/W	X	
14-0	FT3_OFFSET	R/W	0h	Determine which byte to start FT3_[N]P[63:0] operation it will start on the next byte after FT3_T completes if set to zero

115 MII_G_RT_FT3_m_JMP_OFFSET_PRU1 Register (Offset = 6E0h + formula) [reset = X]

MII_G_RT_FT3_m_JMP_OFFSET_PRU1 is shown in Figure 14-3870 and described in Table 14-7829.

Return to Summary Table.

Filter3<m> Jmp offset (PRU1).

Offset = 6E0h + (m * 20h); where m = 0h to Fh

Table 14-11697. MII_G_RT_FT3_m_JMP_OFFSET_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 36E0h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 36E0h + formula

Figure 14-3870. MII_G_RT_FT3_m_JMP_OFFSET_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED	FT3_m_NJMP_OFFSET_PRU1						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
FT3_m_NJMP_OFFSET_PRU1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	FT3_m_IJMP_OFFSET_PRU1						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FT3_m_IJMP_OFFSET_PRU1							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11699. MII_G_RT_FT3_m_JMP_OFFSET_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	FT3_m_NJMP_OFFSET_PRU1	R/W	0h	Defines the Next Offset to compare when auto arm jump is enabled
15	RESERVED	R/W	X	
14-0	FT3_m_IJMP_OFFSET_PRU1	R/W	0h	Defines the Initial Offset to compare when auto arm jump is enabled

116 MII_G_RT_FT3_m_LEN_PRU1 Register (Offset = 6E4h + formula) [reset = X]

MII_G_RT_FT3_m_LEN_PRU1 is shown in Figure 14-3871 and described in Table 14-7831.

Return to Summary Table.

Filter3 Length Offset for (PRU1).

Offset = 6E4h + (m * 20h); where m = 0h to Fh

Table 14-11700. MII_G_RT_FT3_m_LEN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 36E4h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 36E4h + formula

Figure 14-3871. MII_G_RT_FT3_m_LEN_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>FT3_m_LEN_BIG_EN_PRU1</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FT3_m_LEN_SIZE_BIT_PRU1</td></tr>
<tr><td colspan="4">R/W-X</td><td colspan="4">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>FT3_m_LEN_START_BIT_PRU1</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FT3_m_LEN_START_BIT_PRU1</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11702. MII_G_RT_FT3_m_LEN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	FT3_m_LEN_BIG_EN_PRU1	R/W	0h	Enable Big Indian on Length
23-20	RESERVED	R/W	X	
19-16	FT3_m_LEN_SIZE_BIT_PRU1	R/W	0h	Defines number of bits to extract the length for the auto skip function
15-9	RESERVED	R/W	X	
8-0	FT3_m_LEN_START_BIT_PRU1	R/W	0h	Defines relative bit offset from the HIT byte location upto 512 bit offset the extraction to determine the on the fly length byte offset

117 MII_G_RT_FT3_m_CFG_PRU1 Register (Offset = 6E8h + formula) [reset = X]

MII_G_RT_FT3_m_CFG_PRU1 is shown in Figure 14-3872 and described in Table 14-7833.

Return to Summary Table.

Filter3<m> Configuration (PRU1).

Offset = 6E8h + (m * 20h); where m = 0h to Fh

Table 14-11703. MII_G_RT_FT3_m_CFG_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 36E8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 36E8h + formula

Figure 14-3872. MII_G_RT_FT3_m_CFG_PRU1 Register

31	30	29	28	27	26	25	24
FT3_m_TRIG_OR_EN							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FT3_m_TRIG_OR_EN							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					FT3_m_VLAN_SKIP_EN	FT3_mCFG	
R/W-X					R/W-1h	R/W-1h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11705. MII_G_RT_FT3_m_CFG_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FT3_m_TRIG_OR_EN	R/W	0h	Trigger ft3 select for auto skip enable, if one or more set the function is enabled note you can not select the same ft3 only others
15-3	RESERVED	R/W	X	
2	FT3_m_VLAN_SKIP_EN	R/W	1h	0: Disabled 1: Enable
1-0	FT3_mCFG	R/W	1h	0: Disabled 1: EQ 2: GT 3: LT

118 MII_G_RT_FT3_m_T_PRU1 Register (Offset = 6ECh + formula) [reset = 0h]

MII_G_RT_FT3_m_T_PRU1 is shown in Figure 14-3873 and described in Table 14-7835.

Return to Summary Table.

Filter3<m> T (PRU1).

Offset = 6ECh + (m * 20h); where m = 0h to Fh

Table 14-11706. MII_G_RT_FT3_m_T_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 36ECh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 36ECh + formula

Figure 14-3873. MII_G_RT_FT3_m_T_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT3_m_T</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11708. MII_G_RT_FT3_m_T_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_T	R/W	0h	Filter3 T4:T1 Note: if Auto Skip is enabled then Type filter is not enabled

119 MII_G_RT_FT3_m_T_MASK_PRU1 Register (Offset = 6F0h + formula) [reset = 0h]

MII_G_RT_FT3_m_T_MASK_PRU1 is shown in Figure 14-3874 and described in Table 14-7837.

Return to Summary Table.

Filter3<m> T Mask (PRU1).

Offset = 6F0h + (m * 20h); where m = 0h to Fh

Table 14-11709. MII_G_RT_FT3_m_T_MASK_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 36F0h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 36F0h + formula

Figure 14-3874. MII_G_RT_FT3_m_T_MASK_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT3_m_T_MASK</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11711. MII_G_RT_FT3_m_T_MASK_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_T_MASK	R/W	0h	Filter3 MT4:MT1 Note: if Auto Skip is enabled then Type filter is not enabled set to 1 to mask corresponding bit

120 MII_G_RT_FT3_m_P0_PRU1 Register (Offset = 8D4h + formula) [reset = 0h]

MII_G_RT_FT3_m_P0_PRU1 is shown in Figure 14-3875 and described in Table 14-7839.

Return to Summary Table.

Filter3<m> P0 (PRU1).

Offset = 8D4h + (m * 10h); where m = 0h to Fh

Table 14-11712. MII_G_RT_FT3_m_P0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 38D4h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 38D4h + formula

Figure 14-3875. MII_G_RT_FT3_m_P0_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT3_m_P0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11714. MII_G_RT_FT3_m_P0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P0	R/W	0h	Filter3 P4:P1

121 MII_G_RT_FT3_m_P1_PRU1 Register (Offset = 8D8h + formula) [reset = 0h]

MII_G_RT_FT3_m_P1_PRU1 is shown in Figure 14-3876 and described in Table 14-7841.

Return to Summary Table.

Filter3<m> P1 (PRU1).

Offset = 8D8h + (m * 10h); where m = 0h to Fh

Table 14-11715. MII_G_RT_FT3_m_P1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 38D8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 38D8h + formula

Figure 14-3876. MII_G_RT_FT3_m_P1_PRU1 Register

31-0
FT3_m_P1
R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11717. MII_G_RT_FT3_m_P1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P1	R/W	0h	Filter3 P8:P5

122 MII_G_RT_FT3_m_P_MASK0_PRU1 Register (Offset = 8DCh + formula) [reset = 0h]

MII_G_RT_FT3_m_P_MASK0_PRU1 is shown in Figure 14-3877 and described in Table 14-7843.

Return to Summary Table.

Filter3<m> P Mask0 (PRU1).

Offset = 8DCh + (m * 10h); where m = 0h to Fh

Table 14-11718. MII_G_RT_FT3_m_P_MASK0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 38DCh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 38DCh + formula

Figure 14-3877. MII_G_RT_FT3_m_P_MASK0_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT3_m_P_MASK0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11720. MII_G_RT_FT3_m_P_MASK0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P_MASK0	R/W	0h	Filter3 MP4:MP1 set to 1 to mask corresponding bit

123 MII_G_RT_FT3_m_P_MASK1_PRU1 Register (Offset = 8E0h + formula) [reset = 0h]

MII_G_RT_FT3_m_P_MASK1_PRU1 is shown in Figure 14-3878 and described in Table 14-7845.

Return to Summary Table.

Filter3<m> P Mask1 (PRU1).

Offset = 8E0h + (m * 10h); where m = 0h to Fh

Table 14-11721. MII_G_RT_FT3_m_P_MASK1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 38E0h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 38E0h + formula

Figure 14-3878. MII_G_RT_FT3_m_P_MASK1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_P_MASK1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11723. MII_G_RT_FT3_m_P_MASK1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P_MASK1	R/W	0h	Filter3 MP8:MP5 set to 1 to mask corresponding bit

124 MII_G_RT_FT_RX_PTR_PRU1 Register (Offset = 9D4h) [reset = 0h]

MII_G_RT_FT_RX_PTR_PRU1 is shown in Figure 14-3879 and described in Table 14-7847.

Return to Summary Table.

Filter Byte Count (PRU1).

Table 14-11724. MII_G_RT_FT_RX_PTR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 39D4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 39D4h

Figure 14-3879. MII_G_RT_FT_RX_PTR_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FT_RX_PTR_PRU1</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11726. MII_G_RT_FT_RX_PTR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT_RX_PTR_PRU1	R/W	0h	RX current filter Byte Count

125 MII_G_RT_RX_CLASSm_AND_EN_PRU1 Register (Offset = 9D8h + formula) [reset = 0h]

MII_G_RT_RX_CLASSm_AND_EN_PRU1 is shown in Figure 14-3880 and described in Table 14-7849.

Return to Summary Table.

RX Class<m> AND Enable (PRU1).

Offset = 9D8h + (m * 8h); where m = 0h to Fh

Table 14-11727. MII_G_RT_RX_CLASSm_AND_EN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 39D8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 39D8h + formula

Figure 14-3880. MII_G_RT_RX_CLASSm_AND_EN_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASSm_AND_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11729. MII_G_RT_RX_CLASSm_AND_EN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CLASSm_AND_EN	R/W	0h	RX class AND enable

126 MII_G_RT_RX_CLASSm_OR_EN_PRU1 Register (Offset = 9DCh + formula) [reset = 0h]

MII_G_RT_RX_CLASSm_OR_EN_PRU1 is shown in Figure 14-3881 and described in Table 14-7851.

Return to Summary Table.

RX Class<m> OR Enable (PRU1).

Offset = 9DCh + (m * 8h); where m = 0h to Fh

Table 14-11730. MII_G_RT_RX_CLASSm_OR_EN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 39DCh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 39DCh + formula

Figure 14-3881. MII_G_RT_RX_CLASSm_OR_EN_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASSm_OR_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11732. MII_G_RT_RX_CLASSm_OR_EN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CLASSm_OR_EN	R/W	0h	RX class OR enable.

127 MII_G_RT_RX_CLASS_CFG1_PRU1 Register (Offset = A58h) [reset = 0h]

MII_G_RT_RX_CLASS_CFG1_PRU1 is shown in Figure 14-3882 and described in Table 14-7853.

Return to Summary Table.

RX Class Configuration 1 Register.

Table 14-11733. MII_G_RT_RX_CLASS_CFG1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3A58h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3A58h

Figure 14-3882. MII_G_RT_RX_CLASS_CFG1_PRU1 Register

31	30	29	28	27	26	25	24
RX_CLASS15_SEL		RX_CLASS14_SEL		RX_CLASS13_SEL		RX_CLASS12_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CLASS11_SEL		RX_CLASS10_SEL		RX_CLASS9_SEL		RX_CLASS8_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_CLASS7_SEL		RX_CLASS6_SEL		RX_CLASS5_SEL		RX_CLASS4_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_CLASS3_SEL		RX_CLASS2_SEL		RX_CLASS1_SEL		RX_CLASS0_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11735. MII_G_RT_RX_CLASS_CFG1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_CLASS15_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
29-28	RX_CLASS14_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
27-26	RX_CLASS13_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
25-24	RX_CLASS12_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
23-22	RX_CLASS11_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND

Table 14-11735. MII_G_RT_RX_CLASS_CFG1_PRU1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	RX_CLASS10_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
19-18	RX_CLASS9_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
17-16	RX_CLASS8_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
15-14	RX_CLASS7_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
13-12	RX_CLASS6_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
11-10	RX_CLASS5_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
9-8	RX_CLASS4_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
7-6	RX_CLASS3_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
5-4	RX_CLASS2_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
3-2	RX_CLASS1_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
1-0	RX_CLASS0_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND

128 MII_G_RT_RX_CLASS_CFG2_PRU1 Register (Offset = A5Ch) [reset = 0h]

MII_G_RT_RX_CLASS_CFG2_PRU1 is shown in Figure 14-3883 and described in Table 14-7855.

Return to Summary Table.

RX Class Configuration 2 Register.

Table 14-11736. MII_G_RT_RX_CLASS_CFG2_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3A5Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3A5Ch

Figure 14-3883. MII_G_RT_RX_CLASS_CFG2_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASS_OR_NV																RX_CLASS_AND_NV															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11738. MII_G_RT_RX_CLASS_CFG2_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_CLASS_OR_NV	R/W	0h	RX class or nv enable
15-0	RX_CLASS_AND_NV	R/W	0h	RX class AND nv enable

129 MII_G_RT_RX_CLASS_GATESm_PRU1 Register (Offset = A60h + formula) [reset = X]

MII_G_RT_RX_CLASS_GATESm_PRU1 is shown in Figure 14-3884 and described in Table 14-7857.

Return to Summary Table.

RX Class Gate Configuration PRU1 Register.

Offset = A60h + (m * 4h); where m = 0h to Fh

Table 14-11739. MII_G_RT_RX_CLASS_GATESm_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3A60h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3A60h + formula

Figure 14-3884. MII_G_RT_RX_CLASS_GATESm_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_RED_PHASE_ENm
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RX_ALLOW_MASKm	RX_CLASS_RAW_MASKm	RX_PHASE_MASKm	RESERVED	RX_RATE_GATE_SELm		
R/W-X	R/W-1h	R/W-1h	R/W-1h	R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11741. MII_G_RT_RX_CLASS_GATESm_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_RED_PHASE_ENm	R/W	0h	red phase enable 0: disable 1: enable
7	RESERVED	R/W	X	
6	RX_ALLOW_MASKm	R/W	1h	allow mask 0: unmask 1: mask
5	RX_CLASS_RAW_MASKm	R/W	1h	class raw mask 0: unmask 1: mask
4	RX_PHASE_MASKm	R/W	1h	time phase mask 0: unmask 1: mask
3	RESERVED	R/W	X	
2-0	RX_RATE_GATE_SELm	R/W	0h	defines which rx_rate will gate rx_class

130 MII_G_RT_RX_GREEN_PRU1 Register (Offset = AA0h) [reset = X]

MII_G_RT_RX_GREEN_PRU1 is shown in Figure 14-3885 and described in Table 14-7859.

Return to Summary Table.

RX Green Status PRU1.

Table 14-11742. MII_G_RT_RX_GREEN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3AA0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3AA0h

Figure 14-3885. MII_G_RT_RX_GREEN_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			RX_GREEN_VAL	RX_GREEN_CMP_SEL			
R/W-X			R-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11744. MII_G_RT_RX_GREEN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	RX_GREEN_VAL	R	0h	0: RED, 1: GREEN status
3-0	RX_GREEN_CMP_SEL	R/W	0h	define which IEP CMP start green

131 MII_G_RT_SA_HASH_PRU1 Register (Offset = AA4h) [reset = X]

MII_G_RT_SA_HASH_PRU1 is shown in Figure 14-3886 and described in Table 14-7861.

Return to Summary Table.

SA Hash Seed PRU1.

Table 14-11745. MII_G_RT_SA_HASH_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3AA4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3AA4h

Figure 14-3886. MII_G_RT_SA_HASH_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SA_HASH_SEED									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11747. MII_G_RT_SA_HASH_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	SA_HASH_SEED	R/W	0h	SA Hash Seed

132 MII_G_RT_CONN_HASH_PRU1 Register (Offset = AA8h) [reset = X]

MII_G_RT_CONN_HASH_PRU1 is shown in Figure 14-3887 and described in Table 14-7863.

Return to Summary Table.

Connection Hash Seed PRU1.

Table 14-11748. MII_G_RT_CONN_HASH_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3AA8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3AA8h

Figure 14-3887. MII_G_RT_CONN_HASH_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="10">CONN_HASH_SEED</td></tr>
<tr><td colspan="6">R/W-X</td><td colspan="10">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11750. MII_G_RT_CONN_HASH_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	CONN_HASH_SEED	R/W	0h	Connection Hash Seed

133 MII_G_RT_CONN_HASH_START_PRU1 Register (Offset = AACh) [reset = X]

MII_G_RT_CONN_HASH_START_PRU1 is shown in Figure 14-3888 and described in Table 14-7865.

Return to Summary Table.

Connection Hash Start PRU1.

Table 14-11751. MII_G_RT_CONN_HASH_START_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3AACh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3AACh

Figure 14-3888. MII_G_RT_CONN_HASH_START_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	CONN_HASH_START														
R/W-X																	R/W-0h														

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11753. MII_G_RT_CONN_HASH_START_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-0	CONN_HASH_START	R/W	0h	Connection Hash Start which 4 Bytes to hash

134 MII_G_RT_RX_RATE_CFGn_PRU1 Register (Offset = AB0h + formula) [reset = 0h]

MII_G_RT_RX_RATE_CFGn_PRU1 is shown in Figure 14-3889 and described in Table 14-7867.

Return to Summary Table.

RX Rate Configuration Register.

Offset = AB0h + (n * 4h); where n = 0h to 7h

Table 14-11754. MII_G_RT_RX_RATE_CFGn_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3AB0h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3AB0h + formula

Figure 14-3889. MII_G_RT_RX_RATE_CFGn_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_RATE_CIR_IDLEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11756. MII_G_RT_RX_RATE_CFGn_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_RATE_CIR_IDLEn	R/W	0h	RX Rate Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle including EOF. The PIR counter is disabled with a zero value and packets will not be marked RED

135 MII_G_RT_RX_RATE_SRC_SEL0_PRU1 Register (Offset = AD0h) [reset = X]

MII_G_RT_RX_RATE_SRC_SEL0_PRU1 is shown in Figure 14-3890 and described in Table 14-7869.

Return to Summary Table.

RX Rate Source Select0.

Table 14-11757. MII_G_RT_RX_RATE_SRC_SEL0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3AD0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3AD0h

Figure 14-3890. MII_G_RT_RX_RATE_SRC_SEL0_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED		RX_RATE_SRC_SEL3					
R/W-X		R/W-0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		RX_RATE_SRC_SEL2					
R/W-X		R/W-0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		RX_RATE_SRC_SEL1					
R/W-X		R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RX_RATE_SRC_SEL0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11759. MII_G_RT_RX_RATE_SRC_SEL0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RX_RATE_SRC_SEL3	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
23-22	RESERVED	R/W	X	
21-16	RX_RATE_SRC_SEL2	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
15-14	RESERVED	R/W	X	
13-8	RX_RATE_SRC_SEL1	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
7-6	RESERVED	R/W	X	
5-0	RX_RATE_SRC_SEL0	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping

136 MII_G_RT_RX_RATE_SRC_SEL1_PRU1 Register (Offset = AD4h) [reset = X]

MII_G_RT_RX_RATE_SRC_SEL1_PRU1 is shown in Figure 14-3891 and described in Table 14-7871.

Return to Summary Table.

RX Rate Source Select1.

Table 14-11760. MII_G_RT_RX_RATE_SRC_SEL1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3AD4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3AD4h

Figure 14-3891. MII_G_RT_RX_RATE_SRC_SEL1_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED		RX_RATE_SRC_SEL7					
R/W-X		R/W-0h					

23	22	21	20	19	18	17	16
RESERVED		RX_RATE_SRC_SEL6					
R/W-X		R/W-0h					

15	14	13	12	11	10	9	8
RESERVED		RX_RATE_SRC_SEL5					
R/W-X		R/W-0h					

7	6	5	4	3	2	1	0
RESERVED		RX_RATE_SRC_SEL4					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11762. MII_G_RT_RX_RATE_SRC_SEL1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RX_RATE_SRC_SEL7	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
23-22	RESERVED	R/W	X	
21-16	RX_RATE_SRC_SEL6	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
15-14	RESERVED	R/W	X	
13-8	RX_RATE_SRC_SEL5	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
7-6	RESERVED	R/W	X	
5-0	RX_RATE_SRC_SEL4	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping

137 MII_G_RT_TX_RATE_CFG1_n_PRU1 Register (Offset = AD8h + formula) [reset = 0h]

MII_G_RT_TX_RATE_CFG1_n_PRU1 is shown in Figure 14-3892 and described in Table 14-7873.

Return to Summary Table.

TX Rate Configuration 1 Register.

Offset = AD8h + (n * 8h); where n = 0h to 7h

Table 14-11763. MII_G_RT_TX_RATE_CFG1_n_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3AD8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3AD8h + formula

Figure 14-3892. MII_G_RT_TX_RATE_CFG1_n_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_RATE_CIR_IDLEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11765. MII_G_RT_TX_RATE_CFG1_n_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_RATE_CIR_IDLEn	R/W	0h	TX Rate Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle including EOF. The PIR counter is disabled with a zero value and packets will not be marked RED

138 MII_G_RT_TX_RATE_CFG2_n_PRU1 Register (Offset = ADCh + formula) [reset = X]

MII_G_RT_TX_RATE_CFG2_n_PRU1 is shown in Figure 14-3893 and described in Table 14-7875.

Return to Summary Table.

TX Rate Configuration 2 Register.

Offset = ADCh + (n * 8h); where n = 0h to 7h

Table 14-11766. MII_G_RT_TX_RATE_CFG2_n_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3ADCh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3ADCh + formula

Figure 14-3893. MII_G_RT_TX_RATE_CFG2_n_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						TX_RATE_ALLOWn	TX_RATE_ENn
R/W-X						R-0h	R/W-0h
15	14	13	12	11	10	9	8
TX_RATE_LENn							
R/W-0h							
7	6	5	4	3	2	1	0
TX_RATE_LENn							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11768. MII_G_RT_TX_RATE_CFG2_n_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	TX_RATE_ALLOWn	R	0h	TX Rate Pkt Enable
16	TX_RATE_ENn	R/W	0h	TX Rate Pkt Enable
15-0	TX_RATE_LENn	R/W	0h	TX Rate Pkt Length

139 MII_G_RT_RX_STAT_GOOD_PRU1 Register (Offset = B18h) [reset = 0h]

MII_G_RT_RX_STAT_GOOD_PRU1 is shown in Figure 14-3894 and described in Table 14-7877.

Return to Summary Table.

RX Good Frame Count (PRU1).

Table 14-11769. MII_G_RT_RX_STAT_GOOD_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B18h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B18h

Figure 14-3894. MII_G_RT_RX_STAT_GOOD_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">RX_GOOD_FRM_CNT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11771. MII_G_RT_RX_STAT_GOOD_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_GOOD_FRM_CNT	R/W	0h	RX Good Frame Count. increment on none min err max err CRC err odd err, Write to subtract

140 MII_G_RT_RX_STAT_BC_PRU1 Register (Offset = B1Ch) [reset = X]

MII_G_RT_RX_STAT_BC_PRU1 is shown in Figure 14-3895 and described in Table 14-7879.

Return to Summary Table.

RX BC Frame Count (PRU1).

Table 14-11772. MII_G_RT_RX_STAT_BC_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B1Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B1Ch

Figure 14-3895. MII_G_RT_RX_STAT_BC_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_BC_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11774. MII_G_RT_RX_STAT_BC_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_BC_FRM_CNT	R/W	0h	RX BC Frame Count increment on BC type, Write to subtract

141 MII_G_RT_RX_STAT_MC_PRU1 Register (Offset = B20h) [reset = X]

MII_G_RT_RX_STAT_MC_PRU1 is shown in Figure 14-3896 and described in Table 14-7881.

Return to Summary Table.

RX MC Frame Count (PRU1).

Table 14-11775. MII_G_RT_RX_STAT_MC_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B20h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B20h

Figure 14-3896. MII_G_RT_RX_STAT_MC_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_MC_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11777. MII_G_RT_RX_STAT_MC_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MC_FRM_CNT	R/W	0h	RX MC Frame Count increment on MC type, Write to subtract

142 MII_G_RT_RX_STAT_CRC_ERR_PRU1 Register (Offset = B24h) [reset = X]

MII_G_RT_RX_STAT_CRC_ERR_PRU1 is shown in Figure 14-3897 and described in Table 14-7883.

Return to Summary Table.

RX CRC Error Frame Count (PRU1).

Table 14-11778. MII_G_RT_RX_STAT_CRC_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B24h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B24h

Figure 14-3897. MII_G_RT_RX_STAT_CRC_ERR_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RX_CRC_ERR_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11780. MII_G_RT_RX_STAT_CRC_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_CRC_ERR_FRM_CNT	R/W	0h	RX CRC Err Frame Count increment on CRC error, Write to subtract

143 MII_G_RT_RX_STAT_MII_ERR_PRU1 Register (Offset = B28h) [reset = X]

MII_G_RT_RX_STAT_MII_ERR_PRU1 is shown in Figure 14-3898 and described in Table 14-7885.

Return to Summary Table.

RX MII Error Frame Count (PRU1).

Table 14-11781. MII_G_RT_RX_STAT_MII_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B28h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B28h

Figure 14-3898. MII_G_RT_RX_STAT_MII_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_MII_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11783. MII_G_RT_RX_STAT_MII_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MII_ERR_FRM_CNT	R/W	0h	RX MII Err Frame Count increment on MII, SGMII, RGMII error, Write to subtract

144 MII_G_RT_RX_STAT_ODD_ERR_PRU1 Register (Offset = B2Ch) [reset = X]

MII_G_RT_RX_STAT_ODD_ERR_PRU1 is shown in Figure 14-3899 and described in Table 14-7887.

Return to Summary Table.

RX Odd Nibble Frame Count (PRU1).

Table 14-11784. MII_G_RT_RX_STAT_ODD_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B2Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B2Ch

Figure 14-3899. MII_G_RT_RX_STAT_ODD_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ODD_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11786. MII_G_RT_RX_STAT_ODD_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_ODD_ERR_FRM_CNT	R/W	0h	RX Odd Nibble Frame Count increment on odd nibble MII, Write to subtract

145 MII_G_RT_RX_STAT_MAX_SIZE_PRU1 Register (Offset = B30h) [reset = X]

MII_G_RT_RX_STAT_MAX_SIZE_PRU1 is shown in Figure 14-3900 and described in Table 14-7889.

Return to Summary Table.

RX Max Size Frame (PRU1).

Table 14-11787. MII_G_RT_RX_STAT_MAX_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B30h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B30h

Figure 14-3900. MII_G_RT_RX_STAT_MAX_SIZE_PRU1 Register

31-16	15-0
RESERVED	RX_MAX_SIZE_FRM
R/W-X	R/W-7D0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11789. MII_G_RT_RX_STAT_MAX_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MAX_SIZE_FRM	R/W	7D0h	RX MAX Size Frame Count Limit

146 MII_G_RT_RX_STAT_MAX_ERR_PRU1 Register (Offset = B34h) [reset = X]

MII_G_RT_RX_STAT_MAX_ERR_PRU1 is shown in Figure 14-3901 and described in Table 14-7891.

Return to Summary Table.

RX Max Size Error Frame Count (PRU1).

Table 14-11790. MII_G_RT_RX_STAT_MAX_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B34h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B34h

Figure 14-3901. MII_G_RT_RX_STAT_MAX_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11792. MII_G_RT_RX_STAT_MAX_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MAX_ERR_FRM_CNT	R/W	0h	RX MAX Size Err Frame Count increment if > than Limit, Write to subtract

147 MII_G_RT_RX_STAT_MIN_SIZE_PRU1 Register (Offset = B38h) [reset = X]

MII_G_RT_RX_STAT_MIN_SIZE_PRU1 is shown in Figure 14-3902 and described in Table 14-7893.

Return to Summary Table.

RX Min Size Frame (PRU1).

Table 14-11793. MII_G_RT_RX_STAT_MIN_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B38h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B38h

Figure 14-3902. MII_G_RT_RX_STAT_MIN_SIZE_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_MIN_SIZE_FRM</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-40h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11795. MII_G_RT_RX_STAT_MIN_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MIN_SIZE_FRM	R/W	40h	RX MIN Size Frame Limit

148 MII_G_RT_RX_STAT_MIN_ERR_PRU1 Register (Offset = B3Ch) [reset = X]

MII_G_RT_RX_STAT_MIN_ERR_PRU1 is shown in Figure 14-3903 and described in Table 14-7895.

Return to Summary Table.

RX Min Size Error Frame Count (PRU1).

Table 14-11796. MII_G_RT_RX_STAT_MIN_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B3Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B3Ch

Figure 14-3903. MII_G_RT_RX_STAT_MIN_ERR_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RX_MIN_ERR_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11798. MII_G_RT_RX_STAT_MIN_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MIN_ERR_FRM_CNT	R/W	0h	RX MIN Size Frame Count increment if < than limit, Write to subtract

149 MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 Register (Offset = B40h) [reset = X]

MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 is shown in Figure 14-3904 and described in Table 14-7897.

Return to Summary Table.

RX Overrun Frame Count (PRU1).

Table 14-11799. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B40h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B40h

Figure 14-3904. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OVERRUN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11801. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_OVERRUN_ERR_FRM_CNT	R/W	0h	RX L1 FIFO overflow Frame Count increment on overflow event, Write to subtract

150 MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 Register (Offset = B44h + formula) [reset = 0h]

MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 is shown in Figure 14-3905 and described in Table 14-7899.

Return to Summary Table.

RX Class<m>.

Offset = B44h + (m * 4h); where m = 0h to Fh

Table 14-11802. MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B44h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B44h + formula

Figure 14-3905. MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_CLASSm_PRU1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11804. MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_STAT_CLASSm_PRU1	R/W	0h	RX Class<m> Hit Count (where m = 0 to 15). Write to subtract

151 MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Register (Offset = B84h) [reset = 0h]

MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 is shown in Figure 14-3906 and described in Table 14-7901.

Return to Summary Table.

RX SMD Frag Error Count (PRU1).

Table 14-11805. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B84h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B84h

Figure 14-3906. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_STAT_SMD_ERR_PRU1								RX_STAT_FRAG_ERR_PRU1							
R/W-0h								R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_STAT_SMDC_ERR_PRU1								RX_STAT_SMDS_ERR_PRU1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11807. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_STAT_SMD_ERR_PRU1	R/W	0h	RX SMDS Error Count, increment when first none 0x55 does not match any valid SMD, Write to subtract
23-16	RX_STAT_FRAG_ERR_PRU1	R/W	0h	RX Frag_Cnt Seq Error Count, Write to subtract
15-8	RX_STAT_SMDC_ERR_PRU1	R/W	0h	RX SMDCx Seq Error Count, Write to subtract
7-0	RX_STAT_SMDS_ERR_PRU1	R/W	0h	RX SMDSx Seq Error Count, Write to subtract

152 MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 Register (Offset = B88h) [reset = X]

MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 is shown in Figure 14-3907 and described in Table 14-7903.

Return to Summary Table.

RX Bucket1 Size Configuration (PRU1).

Table 14-11808. MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B88h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B88h

Figure 14-3907. MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="14">RX_STAT_BKT1_SIZE</td></tr>
<tr><td colspan="2">R/W-X</td><td colspan="14">R/W-40h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11810. MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT1_SIZE	R/W	40h	RX Bucket1 Byte Size

153 MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 Register (Offset = B8Ch) [reset = X]

MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 is shown in Figure 14-3908 and described in Table 14-7905.

Return to Summary Table.

RX Bucket2 Size Configuration (PRU1).

Table 14-11811. MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B8Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B8Ch

Figure 14-3908. MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT2_SIZE													
R/W-X		R/W-80h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11813. MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT2_SIZE	R/W	80h	RX Bucket2 Byte Size

154 MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 Register (Offset = B90h) [reset = X]

MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 is shown in Figure 14-3909 and described in Table 14-7907.

Return to Summary Table.

RX Bucket3 Size Configuration (PRU1).

Table 14-11814. MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B90h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B90h

Figure 14-3909. MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT3_SIZE													
R/W-X		R/W-100h													

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11816. MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT3_SIZE	R/W	100h	RX Bucket3 Byte Size

155 MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 Register (Offset = B94h) [reset = X]

MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 is shown in Figure 14-3910 and described in Table 14-7909.

Return to Summary Table.

RX Bucket4 Size Configuration (PRU1).

Table 14-11817. MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B94h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B94h

Figure 14-3910. MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="14">RX_STAT_BKT4_SIZE</td></tr>
<tr><td colspan="2">R/W-X</td><td colspan="14">R/W-200h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11819. MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT4_SIZE	R/W	200h	RX Bucket4 Byte Size

156 MII_G_RT_RX_STAT_64_PRU1 Register (Offset = B98h) [reset = X]

MII_G_RT_RX_STAT_64_PRU1 is shown in Figure 14-3911 and described in Table 14-7911.

Return to Summary Table.

RX 64B Sized Frame Count (PRU1).

Table 14-11820. MII_G_RT_RX_STAT_64_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B98h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B98h

Figure 14-3911. MII_G_RT_RX_STAT_64_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_64_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11822. MII_G_RT_RX_STAT_64_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_64_FRM_CNT	R/W	0h	RX 64 Byte Frame Count increment if 64 B size

157 MII_G_RT_RX_STAT_BKT1_PRU1 Register (Offset = B9Ch) [reset = X]

MII_G_RT_RX_STAT_BKT1_PRU1 is shown in Figure 14-3912 and described in Table 14-7913.

Return to Summary Table.

RX Bucket1 Sized Frame Count (PRU1).

Table 14-11823. MII_G_RT_RX_STAT_BKT1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3B9Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3B9Ch

Figure 14-3912. MII_G_RT_RX_STAT_BKT1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11825. MII_G_RT_RX_STAT_BKT1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT1	R/W	0h	RX Bucket1 Frame Count increment if <= than Bucket1 Byte Size

158 MII_G_RT_RX_STAT_BKT2_PRU1 Register (Offset = BA0h) [reset = X]

MII_G_RT_RX_STAT_BKT2_PRU1 is shown in Figure 14-3913 and described in Table 14-7915.

Return to Summary Table.

RX Bucket2 Sized Frame Count (PRU1).

Table 14-11826. MII_G_RT_RX_STAT_BKT2_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BA0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BA0h

Figure 14-3913. MII_G_RT_RX_STAT_BKT2_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11828. MII_G_RT_RX_STAT_BKT2_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT2	R/W	0h	RX Bucket2 Frame Count increment if <= than Bucket2 Byte Size and if > than Bucket1 Byte Size

159 MII_G_RT_RX_STAT_BKT3_PRU1 Register (Offset = BA4h) [reset = X]

MII_G_RT_RX_STAT_BKT3_PRU1 is shown in Figure 14-3914 and described in Table 14-7917.

Return to Summary Table.

RX Bucket3 Sized Frame Count (PRU1).

Table 14-11829. MII_G_RT_RX_STAT_BKT3_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BA4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BA4h

Figure 14-3914. MII_G_RT_RX_STAT_BKT3_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11831. MII_G_RT_RX_STAT_BKT3_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT3	R/W	0h	RX Bucket3 Frame Count increment if <= than Bucket3 Byte Size and if > than Bucket2 Byte Size

160 MII_G_RT_RX_STAT_BKT4_PRU1 Register (Offset = BA8h) [reset = X]

MII_G_RT_RX_STAT_BKT4_PRU1 is shown in Figure 14-3915 and described in Table 14-7919.

Return to Summary Table.

RX Bucket4 Sized Frame Count (PRU1).

Table 14-11832. MII_G_RT_RX_STAT_BKT4_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BA8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BA8h

Figure 14-3915. MII_G_RT_RX_STAT_BKT4_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_STAT_BKT4</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11834. MII_G_RT_RX_STAT_BKT4_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT4	R/W	0h	RX Bucket4 Frame Count increment if <= than Bucket4 Byte Size and if > than Bucket3 Byte Size

161 MII_G_RT_RX_STAT_BKT5_PRU1 Register (Offset = BACh) [reset = X]

MII_G_RT_RX_STAT_BKT5_PRU1 is shown in Figure 14-3916 and described in Table 14-7921.

Return to Summary Table.

RX Bucket5 Sized Frame Count (PRU1).

Table 14-11835. MII_G_RT_RX_STAT_BKT5_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BACh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BACh

Figure 14-3916. MII_G_RT_RX_STAT_BKT5_PRU1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RX_STAT_BKT5</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11837. MII_G_RT_RX_STAT_BKT5_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT5	R/W	0h	RX Bucket5 Frame Count increment if > than Bucket4 Byte Size

162 MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 Register (Offset = BB0h) [reset = 0h]

MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 is shown in Figure 14-3917 and described in Table 14-7923.

Return to Summary Table.

RX Total Byte Count (PRU1).

Table 14-11838. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BB0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BB0h

Figure 14-3917. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_TOTAL_BYTES_PRU																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11840. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_STAT_TOTAL_BYTES_PRU	R/W	0h	RX Total Byte Count

163 MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Register (Offset = BB4h) [reset = 0h]

MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 is shown in Figure 14-3918 and described in Table 14-7925.

Return to Summary Table.

RX TX Total Byte Count (PRU1).

Table 14-11841. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BB4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BB4h

Figure 14-3918. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXTX_STAT_TOTAL_BYTES_PRU																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11843. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RXTX_STAT_TOTAL_BYTES_PRU	R/W	0h	RX and TX Total Byte Count

164 MII_G_RT_TX_STAT_GOOD_PORT1 Register (Offset = BB8h) [reset = 0h]

MII_G_RT_TX_STAT_GOOD_PORT1 is shown in Figure 14-3919 and described in Table 14-7927.

Return to Summary Table.

TX Good Frame Count Port1.

Table 14-11844. MII_G_RT_TX_STAT_GOOD_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BB8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BB8h

Figure 14-3919. MII_G_RT_TX_STAT_GOOD_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TX_GOOD_FRM_CNT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11846. MII_G_RT_TX_STAT_GOOD_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_GOOD_FRM_CNT	R/W	0h	TX Good Frame Count increment if no min size err max size err or MII odd nibble

165 MII_G_RT_TX_STAT_BC_PORT1 Register (Offset = BBCh) [reset = X]

MII_G_RT_TX_STAT_BC_PORT1 is shown in Figure 14-3920 and described in Table 14-7929.

Return to Summary Table.

TX BC Frame Count Port1.

Table 14-11847. MII_G_RT_TX_STAT_BC_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BBCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BBCh

Figure 14-3920. MII_G_RT_TX_STAT_BC_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_BC_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11849. MII_G_RT_TX_STAT_BC_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_BC_FRM_CNT	R/W	0h	TX BC Frame Count increment if BC

166 MII_G_RT_TX_STAT_MC_PORT1 Register (Offset = BC0h) [reset = X]

MII_G_RT_TX_STAT_MC_PORT1 is shown in Figure 14-3921 and described in Table 14-7931.

Return to Summary Table.

TX MC Frame Count Port1.

Table 14-11850. MII_G_RT_TX_STAT_MC_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BC0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BC0h

Figure 14-3921. MII_G_RT_TX_STAT_MC_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11852. MII_G_RT_TX_STAT_MC_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MC_FRM_CNT	R/W	0h	TX MC Frame Count increment if MC

167 MII_G_RT_TX_STAT_ODD_ERR_PORT1 Register (Offset = BC4h) [reset = X]

MII_G_RT_TX_STAT_ODD_ERR_PORT1 is shown in Figure 14-3922 and described in Table 14-7933.

Return to Summary Table.

TX Odd Nibble Frame Count Port1.

Table 14-11853. MII_G_RT_TX_STAT_ODD_ERR_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BC4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BC4h

Figure 14-3922. MII_G_RT_TX_STAT_ODD_ERR_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">TX_ODD_ERR_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11855. MII_G_RT_TX_STAT_ODD_ERR_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_ODD_ERR_FRM_CNT	R/W	0h	TX Odd Nibble Frame Count increment if MII odd nibble

168 MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Register (Offset = BC8h) [reset = X]

MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 is shown in Figure 14-3923 and described in Table 14-7935.

Return to Summary Table.

TX Under Flow Error Count Port1.

Table 14-11856. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BC8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BC8h

Figure 14-3923. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Register

31-16	15-0
RESERVED	TX_UNDERFLOW_CNT
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11858. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_UNDERFLOW_CNT	R/W	0h	TX MAX Underflow Error Count

169 MII_G_RT_TX_STAT_MAX_SIZE_PORT1 Register (Offset = BCCh) [reset = X]

MII_G_RT_TX_STAT_MAX_SIZE_PORT1 is shown in Figure 14-3924 and described in Table 14-7937.

Return to Summary Table.

TX Max Size Frame Port1.

Table 14-11859. MII_G_RT_TX_STAT_MAX_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BCCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BCCh

Figure 14-3924. MII_G_RT_TX_STAT_MAX_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MAX_SIZE_FRM															
R/W-X																R/W-7D0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11861. MII_G_RT_TX_STAT_MAX_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MAX_SIZE_FRM	R/W	7D0h	TX MAX Size Frame Count Limit

170 MII_G_RT_TX_STAT_MAX_ERR_PORT1 Register (Offset = BD0h) [reset = X]

MII_G_RT_TX_STAT_MAX_ERR_PORT1 is shown in Figure 14-3925 and described in Table 14-7939.

Return to Summary Table.

TX Max Size Error Frame Count Port1.

Table 14-11862. MII_G_RT_TX_STAT_MAX_ERR_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BD0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BD0h

Figure 14-3925. MII_G_RT_TX_STAT_MAX_ERR_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">TX_MAX_ERR_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11864. MII_G_RT_TX_STAT_MAX_ERR_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MAX_ERR_FRM_CNT	R/W	0h	TX MAX Size Err Frame Count increment if > max Limit

171 MII_G_RT_TX_STAT_MIN_SIZE_PORT1 Register (Offset = BD4h) [reset = X]

MII_G_RT_TX_STAT_MIN_SIZE_PORT1 is shown in Figure 14-3926 and described in Table 14-7941.

Return to Summary Table.

TX Min Size Frame Port1.

Table 14-11865. MII_G_RT_TX_STAT_MIN_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BD4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BD4h

Figure 14-3926. MII_G_RT_TX_STAT_MIN_SIZE_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_MIN_SIZE_FRM</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-40h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11867. MII_G_RT_TX_STAT_MIN_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MIN_SIZE_FRM	R/W	40h	TX MIN Size Frame Count Limit

172 MII_G_RT_TX_STAT_MIN_ERR_PORT1 Register (Offset = BD8h) [reset = X]

MII_G_RT_TX_STAT_MIN_ERR_PORT1 is shown in Figure 14-3927 and described in Table 14-7943.

Return to Summary Table.

TX Min Size Error Frame Count Port1.

Table 14-11868. MII_G_RT_TX_STAT_MIN_ERR_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BD8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BD8h

Figure 14-3927. MII_G_RT_TX_STAT_MIN_ERR_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">TX_MIN_ERR_FRM_CNT</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11870. MII_G_RT_TX_STAT_MIN_ERR_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MIN_ERR_FRM_CNT	R/W	0h	TX MIN Size Err Frame Count increment if < min Limit

173 MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 Register (Offset = BDCh) [reset = X]

MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 is shown in Figure 14-3928 and described in Table 14-7945.

Return to Summary Table.

TX Bucket1 Size Configuration Port1.

Table 14-11871. MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BDCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BDCh

Figure 14-3928. MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TX_STAT_BKT1_SIZE													
R/W-X		R/W-40h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11873. MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT1_SIZE	R/W	40h	TX Bucket1 Byte Size

174 MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 Register (Offset = BE0h) [reset = X]

MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 is shown in Figure 14-3929 and described in Table 14-7947.

Return to Summary Table.

TX Bucket2 Size Configuration Port1.

Table 14-11874. MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BE0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BE0h

Figure 14-3929. MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT2_SIZE													
R/W-X		R/W-80h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11876. MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT2_SIZE	R/W	80h	TX Bucket2 Byte Size

175 MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 Register (Offset = BE4h) [reset = X]

MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 is shown in Figure 14-3930 and described in Table 14-7949.

Return to Summary Table.

TX Bucket3 Size Configuration Port1.

Table 14-11877. MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BE4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BE4h

Figure 14-3930. MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT3_SIZE													
R/W-X		R/W-100h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11879. MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT3_SIZE	R/W	100h	TX Bucket3 Byte Size

176 MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 Register (Offset = BE8h) [reset = X]

MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 is shown in Figure 14-3931 and described in Table 14-7951.

Return to Summary Table.

TX Bucket4 Size Configuration Port1.

Table 14-11880. MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BE8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BE8h

Figure 14-3931. MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT4_SIZE													
R/W-X		R/W-200h													

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11882. MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT4_SIZE	R/W	200h	TX Bucket4 Byte Size

177 MII_G_RT_TX_STAT_64_PORT1 Register (Offset = BECh) [reset = X]

MII_G_RT_TX_STAT_64_PORT1 is shown in Figure 14-3932 and described in Table 14-7953.

Return to Summary Table.

TX 64B Sized Frame Count Port1.

Table 14-11883. MII_G_RT_TX_STAT_64_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BECh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BECh

Figure 14-3932. MII_G_RT_TX_STAT_64_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_64_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11885. MII_G_RT_TX_STAT_64_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_64_FRM_CNT	R/W	0h	TX 64 Byte Frame Count increment if 64 B

178 MII_G_RT_TX_STAT_BKT1_PORT1 Register (Offset = BF0h) [reset = X]

MII_G_RT_TX_STAT_BKT1_PORT1 is shown in Figure 14-3933 and described in Table 14-7955.

Return to Summary Table.

TX Bucket1 Sized Frame Count Port1.

Table 14-11886. MII_G_RT_TX_STAT_BKT1_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BF0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BF0h

Figure 14-3933. MII_G_RT_TX_STAT_BKT1_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_STAT_BKT1</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11888. MII_G_RT_TX_STAT_BKT1_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT1	R/W	0h	TX Bucket1 increment if <= than Bucket1

179 MII_G_RT_TX_STAT_BKT2_PORT1 Register (Offset = BF4h) [reset = X]

MII_G_RT_TX_STAT_BKT2_PORT1 is shown in Figure 14-3934 and described in Table 14-7957.

Return to Summary Table.

TX Bucket2 Sized Frame Count Port1.

Table 14-11889. MII_G_RT_TX_STAT_BKT2_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BF4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BF4h

Figure 14-3934. MII_G_RT_TX_STAT_BKT2_PORT1 Register

31-16	15-0
RESERVED	TX_STAT_BKT2
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11891. MII_G_RT_TX_STAT_BKT2_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT2	R/W	0h	TX Bucket2 increment if <= than Bucket2 Byte Size and if > than Bucket1 Byte Size

180 MII_G_RT_TX_STAT_BKT3_PORT1 Register (Offset = BF8h) [reset = X]

MII_G_RT_TX_STAT_BKT3_PORT1 is shown in Figure 14-3935 and described in Table 14-7959.

Return to Summary Table.

TX Bucket3 Sized Frame Count Port1.

Table 14-11892. MII_G_RT_TX_STAT_BKT3_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BF8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BF8h

Figure 14-3935. MII_G_RT_TX_STAT_BKT3_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11894. MII_G_RT_TX_STAT_BKT3_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT3	R/W	0h	TX Bucket3 increment if <= than Bucket3 Byte Size and if > than Bucket2 Byte Size

181 MII_G_RT_TX_STAT_BKT4_PORT1 Register (Offset = BFCh) [reset = X]

MII_G_RT_TX_STAT_BKT4_PORT1 is shown in Figure 14-3936 and described in Table 14-7961.

Return to Summary Table.

TX Bucket4 Sized Frame Count Port1.

Table 14-11895. MII_G_RT_TX_STAT_BKT4_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3BFCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3BFCh

Figure 14-3936. MII_G_RT_TX_STAT_BKT4_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TX_STAT_BKT4</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11897. MII_G_RT_TX_STAT_BKT4_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT4	R/W	0h	TX Bucket4 increment if <= than Bucket4 Byte Size and if > than Bucket3 Byte Size

182 MII_G_RT_TX_STAT_BKT5_PORT1 Register (Offset = C00h) [reset = X]

MII_G_RT_TX_STAT_BKT5_PORT1 is shown in Figure 14-3937 and described in Table 14-7963.

Return to Summary Table.

TX Bucket5 Sized Frame Count Port1.

Table 14-11898. MII_G_RT_TX_STAT_BKT5_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3C00h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3C00h

Figure 14-3937. MII_G_RT_TX_STAT_BKT5_PORT1 Register

31-16	15-0
RESERVED	TX_STAT_BKT5
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11900. MII_G_RT_TX_STAT_BKT5_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT5	R/W	0h	TX Bucket5 increment if > than Bucket4 Byte Size

183 MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 Register (Offset = C04h) [reset = 0h]

MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 is shown in Figure 14-3938 and described in Table 14-7965.

Return to Summary Table.

TX Total Byte Count Port1.

Table 14-11901. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3C04h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3C04h

Figure 14-3938. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_TOTAL_STAT_BYTES_PORT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11903. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_TOTAL_STAT_BYTES_PORT	R/W	0h	TX Total Byte Count of all Frames

184 MII_G_RT_TX_HSR_TAG_PORT1 Register (Offset = C08h) [reset = 892Fh]

MII_G_RT_TX_HSR_TAG_PORT1 is shown in Figure 14-3939 and described in Table 14-7967.

Return to Summary Table.

TX HSR TAG Port1.

Table 14-11904. MII_G_RT_TX_HSR_TAG_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3C08h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3C08h

Figure 14-3939. MII_G_RT_TX_HSR_TAG_PORT1 Register

31-0
TX_HSR_TAG
R/W-892Fh

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11906. MII_G_RT_TX_HSR_TAG_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_HSR_TAG	R/W	892Fh	HSR TAG

185 MII_G_RT_TX_HSR_SEQ_PORT1 Register (Offset = C0Ch) [reset = X]

MII_G_RT_TX_HSR_SEQ_PORT1 is shown in Figure 14-3940 and described in Table 14-7969.

Return to Summary Table.

TX HSR Seq Port1.

Table 14-11907. MII_G_RT_TX_HSR_SEQ_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3C0Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3C0Ch

Figure 14-3940. MII_G_RT_TX_HSR_SEQ_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_HSR_SEQ															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11909. MII_G_RT_TX_HSR_SEQ_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_HSR_SEQ	R/W	0h	HSR Seq count. It will increment for every HSR type

186 MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 Register (Offset = C10h) [reset = X]

MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 is shown in Figure 14-3941 and described in Table 14-7971.

Return to Summary Table.

TX VLAN Type TAG Port1.

Table 14-11910. MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3C10h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3C10h

Figure 14-3941. MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_VLAN_TYPE_TAG															
R/W-X																R/W-81h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11912. MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_VLAN_TYPE_TAG	R/W	81h	TX VLAN Type Tag, match to enable VLAN removal

187 MII_G_RT_TX_VLAN_INS_TAG_PORT1 Register (Offset = C14h) [reset = 1h]

MII_G_RT_TX_VLAN_INS_TAG_PORT1 is shown in Figure 14-3942 and described in Table 14-7973.

Return to Summary Table.

TX VLAN Insertion TAG Port1.

Table 14-11913. MII_G_RT_TX_VLAN_INS_TAG_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3C14h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3C14h

Figure 14-3942. MII_G_RT_TX_VLAN_INS_TAG_PORT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TX_VLAN_INS_TAG</td></tr>
<tr><td colspan="32">R/W-1h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11915. MII_G_RT_TX_VLAN_INS_TAG_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_VLAN_INS_TAG	R/W	1h	TX VLAN Insertion

188 MII_G_RT_QUEUEk Register (Offset = D00h + formula) [reset = X]

MII_G_RT_QUEUEk is shown in Figure 14-3943 and described in Table 14-7975.

Return to Summary Table.

Queue<k>.

Offset = D00h + (k * 4h); where k = 0h to 3Fh

Table 14-11916. MII_G_RT_QUEUEk Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3D00h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3D00h + formula

Figure 14-3943. MII_G_RT_QUEUEk Register

31-16	15-0
RESERVED	QUEUE_H_PTRk
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11918. MII_G_RT_QUEUEk Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	QUEUE_H_PTRk	R/W	0h	Queue <k> (where k = 0 to 63).

189 MII_G_RT_QUEUE_PEEKm Register (Offset = E00h + formula) [reset = X]

MII_G_RT_QUEUE_PEEKm is shown in Figure 14-3944 and described in Table 14-7977.

Return to Summary Table.

Queue Peek<m>

Offset = E00h + (m * 4h); where m = 0h to Fh

Table 14-11919. MII_G_RT_QUEUE_PEEKm Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3E00h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3E00h + formula

Figure 14-3944. MII_G_RT_QUEUE_PEEKm Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUEUE_H_PEEK_PTRm															
R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11921. MII_G_RT_QUEUE_PEEKm Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	QUEUE_H_PEEK_PTRm	R	0h	Queue <m> Peek portal (where m = 0 to 15).

190 MII_G_RT_QUEUE_CNTk Register (Offset = E40h + formula) [reset = 0h]

MII_G_RT_QUEUE_CNTk is shown in Figure 14-3945 and described in Table 14-7979.

Return to Summary Table.

Queue Count<k>

Offset = E40h + (k * 4h); where k = 0h to 3Fh

Table 14-11922. MII_G_RT_QUEUE_CNTk Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3E40h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3E40h + formula

Figure 14-3945. MII_G_RT_QUEUE_CNTk Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIESk															
R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11924. MII_G_RT_QUEUE_CNTk Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	QUEUE_CNT_ENTRIESk	R	0h	Queue Entry Count<k> (where k = 0 to 63).

191 MII_G_RT_QUEUE_RESET Register (Offset = F40h) [reset = 0h]

MII_G_RT_QUEUE_RESET is shown in Figure 14-3946 and described in Table 14-7981.

Return to Summary Table.

Queue Reset

Table 14-11925. MII_G_RT_QUEUE_RESET Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	3003 3F40h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	300B 3F40h

Figure 14-3946. MII_G_RT_QUEUE_RESET Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="10">RESERVED</td><td colspan="6">RESET_QUEUE_ID</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-11927. MII_G_RT_QUEUE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	RESET_QUEUE_ID	R/W	0h	Reset Queue ID.

14.3.6.1.29 PRU_ICSSG_PA_STAT Registers

Table 14-7983 lists the PRU_ICSSG_PA_STAT registers. All register offset addresses not listed in Table 14-7983 should be considered as reserved locations and the register contents should not be modified.

Control registers

Table 14-11928. PRU_ICSSG_PA_STAT Instances

Instance	Base Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	3003 C000h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	300B C000h

Table 14-11929. PRU_ICSSG_PA_STAT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PA_STAT_WRAP_PA_SLV Physical Address	PRU_ICSSG1_PA_STAT_WRAP_PA_SLV Physical Address
0h	ICSSG_PA_STAT_REVID	Revision Register	3003 C000h	300B C000h
4h	ICSSG_PA_STAT_SRESET	Soft Reset Register	3003 C004h	300B C004h
8h	ICSSG_PA_STAT_EAC	Enable and Allocation Control Register	3003 C008h	300B C008h
10h	ICSSG_PA_STAT_TCTL	Timer Control Register	3003 C010h	300B C010h
14h	ICSSG_PA_STAT_TLD	Timer Load Register	3003 C014h	300B C014h
18h	ICSSG_PA_STAT_TVL	Timer Value Register	3003 C018h	300B C018h

1 ICSSG_PA_STAT_REVID Register (Offset = 0h) [reset = 0EF50100h]

ICSSG_PA_STAT_REVID is shown in Figure 14-3947 and described in Table 14-7985.

Return to the Summary Table.

The Revision Register contains the ID and revision information.

Table 14-11930. ICSSG_PA_STAT_REVID Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	3003 C000h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	300B C000h

Figure 14-3947. ICSSG_PA_STAT_REVID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVID																															
R-0EF50100h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11932. ICSSG_PA_STAT_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVID	R	0EF50100h	Module ID and revision information.

2 ICSSG_PA_STAT_SRESET Register (Offset = 4h) [reset = 0h]

ICSSG_PA_STAT_SRESET is shown in Figure 14-3948 and described in Table 14-7987.

Return to the Summary Table.

The Soft Reset Register is written in order to clear the contents of all statistics.

Table 14-11933. ICSSG_PA_STAT_SRESET Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	3003 C004h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	300B C004h

Figure 14-3948. ICSSG_PA_STAT_SRESET Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TRIGGER</td></tr>
<tr><td colspan="32">W-0h</td></tr>
</table>

LEGEND: W = Write Only; -*n* = value after reset

Table 14-11935. ICSSG_PA_STAT_SRESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TRIGGER	W	0h	Writing anything to this field causes the command FIFOs to be emptied, all statistics to be cleared and all bit masks to be reset to 1. The write to this register will be acknowledged (wready will be asserted) after the reset process is completed.

3 ICSSG_PA_STAT_EAC Register (Offset = 8h) [reset = X]

ICSSG_PA_STAT_EAC is shown in Figure 14-3949 and described in Table 14-7989.

Return to the Summary Table.

The register contains the enable for the engine and controls the allocation of 64-bit counters in the memory. It is possible to configure the engine to only have 32-bit counters by setting the 64-bit cnt field to zero.

Table 14-11936. ICSSG_PA_STAT_EAC Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	3003 C008h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	300B C008h

Figure 14-3949. ICSSG_PA_STAT_EAC Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		CNT					
R/W-X		R/W-200h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CNT							
R/W-200h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11938. ICSSG_PA_STAT_EAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	Enables stat engine. If the module is not in enabled state, no stats increment is processed and both input and output streaming interfaces are disabled.
30-14	RESERVED	R/W	X	Always read as 0. Writes have no effect.
13-0	CNT	R/W	200h	Defines the number of 64-bit counters in the memory (must be even number). If this number multiplied by 8-byte is less than 4 KB (stats memory space), then the remaining space is allocated for 32-bit counters.

4 ICSSG_PA_STAT_TCTL Register (Offset = 10h) [reset = X]

ICSSG_PA_STAT_TCTL is shown in Figure 14-3950 and described in Table 14-7991.

Return to the Summary Table.

The Control Timer Register controls a 16-bit timer.

Table 14-11939. ICSSG_PA_STAT_TCTL Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	3003 C010h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	300B C010h

Figure 14-3950. ICSSG_PA_STAT_TCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							

23	22	21	20	19	18	17	16
RESERVED							
R/W-X							

15	14	13	12	11	10	9	8
CLK_EN	RESERVED						
R/W-0h	R/W-X						

7	6	5	4	3	2	1	0
RESERVED		PRE_VAL				RESERVED	
R/W-X		R/W-0h				R/W-X	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11941. ICSSG_PA_STAT_TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	Always read as 0. Writes have no effect.
15	CLK_EN	R/W	0h	0 = Disable prescaler 1 = Enable prescaler
14-6	RESERVED	R/W	X	Always read as 0. Writes have no effect.
5-2	PRE_VAL	R/W	0h	0000 Divide by 2 0001 Divide by 4 0010 Divide by 8 0011 Divide by 16 0100 Divide by 32 0101 Divide by 64 0110 Divide by 128 0111 Divide by 256 1000 Divide by 512 1001 Divide by 1024 1010 Divide by 2048 1011 Divide by 1024 1100 Divide by 8192 1101 Disable timer 1110 Disable timer 1111 Disable timer
1-0	RESERVED	R/W	X	Always read as 0. Writes have no effect.

5 ICSSG_PA_STAT_TLD Register (Offset = 14h) [reset = X]

ICSSG_PA_STAT_TLD is shown in Figure 14-3951 and described in Table 14-7993.

Return to the Summary Table.

The Load Timer Register contains the starting count down value for the 16-bit timer. This register should be written with some value before the timer is started by write on the timer control register.

Table 14-11942. ICSSG_PA_STAT_TLD Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	3003 C014h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	300B C014h

Figure 14-3951. ICSSG_PA_STAT_TLD Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">LOAD_VAL</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11944. ICSSG_PA_STAT_TLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	Always read as 0. Writes have no effect.
15-0	LOAD_VAL	R/W	0h	16-bit timer value.

6 ICSSG_PA_STAT_TVL Register (Offset = 18h) [reset = X]

ICSSG_PA_STAT_TVL is shown in Figure 14-3952 and described in Table 14-7995.

Return to the Summary Table.

The Timer Value Register contains the current value of the timer.

Table 14-11945. ICSSG_PA_STAT_TVL Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	3003 C018h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	300B C018h

Figure 14-3952. ICSSG_PA_STAT_TVL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CUR_VAL															
R-X																R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11947. ICSSG_PA_STAT_TVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	Always read as 0. Writes have no effect.
15-0	CUR_VAL	R	0h	Current value of the 16-bit timer.

14.3.6.1.30 PRU_ICSSG_PA_STAT_QSTAT Registers

Table 14-7997 lists the PRU_ICSSG_PA_STAT_QSTAT registers. All register offset addresses not listed in Table 14-7997 should be considered as reserved locations and the register contents should not be modified.

Statics query mode RAM stores statistic values

Table 14-11948. PRU_ICSSG_PA_STAT_QSTAT Instances

Instance	Base Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_QSTAT	3002 7000h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_QSTAT	300A 7000h

Table 14-11949. PRU_ICSSG_PA_STAT_QSTAT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_QSTAT Physical Address	PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_QSTAT Physical Address
0h + formula	ICSSG_PA_STAT_QRAM_n	32-bit Statistics (Query Mode)	3002 7000h + formula	300A 7000h + formula

1 ICSSG_PA_STAT_QRAM_n Register (Offset = 0h + formula) [reset = 0h]

ICSSG_PA_STAT_QRAM_n is shown in Figure 14-3953 and described in Table 14-7999.

Return to the Summary Table.

Query mode RAM.

Reading directly to a particular statistics memory address returns the current statistics values. In query mode, the stats are not reset after the read completes. To accommodate debug, setting a counter value in the stats memory via the register write is also allowed. However, if there is a stat bump and a register write on the same stat that occur simultaneously, the value in the register write may be ignored.

"n" is the number of 32-bit stats that are supported in the module.

Offset = 0h + (n * 4h); where n = 0h to 3FFh

Table 14-11950. ICSSG_PA_STAT_QRAM_n Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_QSTAT	3002 7000h + formula
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_QSTAT	300A 7000h + formula

Figure 14-3953. ICSSG_PA_STAT_QRAM_n Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">VALUE</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11952. ICSSG_PA_STAT_QRAM_n Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R/W	0h	Query statistic. 32-bit statistic value at counter "n".

14.3.6.1.31 PRU_ICSSG_PA_STAT_CSTAT Registers

Table 14-8001 lists the PRU_ICSSG_PA_STAT_CSTAT registers. All register offset addresses not listed in Table 14-8001 should be considered as reserved locations and the register contents should not be modified.

Statics collect mode RAM stores statistic values

Table 14-11953. PRU_ICSSG_PA_STAT_CSTAT Instances

Instance	Base Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_CSTAT	3002 C000h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_CSTAT	300A C000h

Table 14-11954. PRU_ICSSG_PA_STAT_CSTAT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_CSTAT Physical Address	PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_CSTAT Physical Address
0h + formula	ICSSG_PA_STAT_CRAM_n	32-bit Statistics (Collect Mode)	3002 C000h + formula	300A C000h + formula

1 ICSSG_PA_STAT_CRAM_n Register (Offset = 0h + formula) [reset = 0h]

ICSSG_PA_STAT_CRAM_n is shown in Figure 14-3954 and described in Table 14-8003.

Return to the Summary Table.

Collect mode RAM.

Reading directly to a particular statistics memory address returns the current statistics values. In collect mode, the stats are reset to 0 after the read completes. To accommodate debug, setting a counter value in the stats memory via the register write is also allowed. However, if there is a stat bump and a register write on the same stat that occur simultaneously, the value in the register write may be ignored.

"n" is the number of 32-bit stats that are supported in the module.

Offset = 0h + (n * 4h); where n = 0h to 3FFh

Table 14-11955. ICSSG_PA_STAT_CRAM_n Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_CSTAT	3002 C000h + formula
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_CSTAT	300A C000h + formula

Figure 14-3954. ICSSG_PA_STAT_CRAM_n Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11957. ICSSG_PA_STAT_CRAM_n Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R/W	0h	Collect statistic. 32-bit statistic value at counter "n".

14.3.6.1.32 PRU_PROT_PROTECT Registers

Table 14-8005 lists the memory-mapped registers for the PRU_PROT_PROTECT registers. All register offset addresses not listed in Table 14-8005 should be considered as reserved locations and the register contents should not be modified.

Table 14-11958. PRU_PROT_PROTECT Instances

Instance	Base Address
PRU_ICSSG0_PR1_PROT_SLV	0x3002 4C00h
PRU_ICSSG1_PR1_PROT_SLV	0x300A 4C00h

Table 14-11959. PRU_PROT_PROTECT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_PROT_SLV Physical Address	PRU_ICSSG1_PR1_PROT_SLV Physical Address
0h	PROT_UNLOCK_KEY	Unlock key	3002 4C00h	300A 4C00h
4h	PROT_CFG	Config	3002 4C04h	300A 4C04h

1 PROT_UNLOCK_KEY Register (Offset = 0h) [reset = 0h]

PROT_UNLOCK_KEY is shown in Figure 14-3955 and described in Table 14-8007.

Return to Summary Table.

Unlock key

Table 14-11960. PROT_UNLOCK_KEY Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PROT_SLV	3002 4C00h
PRU_ICSSG1_PR1_PROT_SLV	300A 4C00h

Figure 14-3955. PROT_UNLOCK_KEY Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">UNLOCK_KEY</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11962. PROT_UNLOCK_KEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UNLOCK_KEY	R/W	0h	UnLock Key Pattern. 0x83E7_0B13 to UnLock. 0x0000_0000 to Lock. Unlock enables update of registers.

2 PROT_CFG Register (Offset = 4h) [reset = X]

PROT_CFG is shown in Figure 14-3956 and described in Table 14-8009.

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Config

Table 14-11963. PROT_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PROT_SLV	3002 4C04h
PRU_ICSSG1_PR1_PROT_SLV	300A 4C04h

Figure 14-3956. PROT_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRU1_DMEM1_LOCK_EN	PRU0_DMEM0_LOCK_EN	ICSS_CFG_WP_EN	RTU1_PRU_WP_EN	RTU0_PRU_WP_EN	PRU1_WP_EN	PRU0_WP_EN
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11965. PROT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	PRU1_DMEM1_LOCK_EN	R/W	0h	Write Protect DMEM1 0: disable 1: enable When enabled only PRU1 can write to DMEM1
5	PRU0_DMEM0_LOCK_EN	R/W	0h	Write Protect DMEM0 0: disable 1: enable When enabled only PRU0 can write to DMEM0
4	ICSS_CFG_WP_EN	R/W	0h	Write Protect ICSS_CFG 0: disable 1: enable
3	RTU1_PRU_WP_EN	R/W	0h	Write Protect RTU1_PRU access Debug IMEM 0: disable 1: enable
2	RTU0_PRU_WP_EN	R/W	0h	Write Protect RTU0_PRU access Debug IMEM 0: disable 1: enable
1	PRU1_WP_EN	R/W	0h	Write Protect PRU1 and TX_PRU1 access Debug IMEM 0: disable 1: enable
0	PRU0_WP_EN	R/W	0h	Write Protect PRU0 and TX_PRU0 access Debug IMEM 0: disable 1: enable

14.3.6.1.33 PRU_RAT_SLICE_RAT_SLICE Registers

Table 14-8011 lists the memory-mapped registers for the PRU_RAT_SLICE_RAT_SLICE registers. All register offset addresses not listed in Table 14-8011 should be considered as reserved locations and the register contents should not be modified.

Table 14-11966. PRU_RAT_SLICE_RAT_SLICE Instances

Instance	Base Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8000h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9000h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8000h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9000h

Table 14-11967. PRU_ICSSG0_RAT_SLICE Registers

Offset	Acronym	Register Name	PRU_ICSSG0_RAT_SLICE0_CFG Physical Address	PRU_ICSSG0_RAT_SLICE1_CFG Physical Address
0h	RAT_SLICE_PID	Revision Register	3000 8000h	3000 9000h
4h	RAT_SLICE_CONFIG	Config Register	3000 8004h	3000 9004h
20h + formula	RAT_SLICE_CTRL_j	Region Control Register	3000 8020h + formula	3000 9020h + formula
24h + formula	RAT_SLICE_BASE_j	Region Base Register	3000 8024h + formula	3000 9024h + formula
28h + formula	RAT_SLICE_TRANS_L_j	Region Translated Lower Address	3000 8028h + formula	3000 9028h + formula
2Ch + formula	RAT_SLICE_TRANS_U_j	Region Translated Upper Address	3000 802Ch + formula	3000 902Ch + formula
804h	RAT_SLICE_DESTINATION_ID	Destination ID Register	3000 8804h	3000 9804h
820h	RAT_SLICE_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	3000 8820h	3000 9820h
824h	RAT_SLICE_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	3000 8824h	3000 9824h
828h	RAT_SLICE_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	3000 8828h	3000 9828h
82Ch	RAT_SLICE_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	3000 882Ch	3000 982Ch
830h	RAT_SLICE_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	3000 8830h	3000 9830h
834h	RAT_SLICE_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	3000 8834h	3000 9834h
838h	RAT_SLICE_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	3000 8838h	3000 9838h
840h	RAT_SLICE_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register	3000 8840h	3000 9840h
844h	RAT_SLICE_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register	3000 8844h	3000 9844h
848h	RAT_SLICE_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register	3000 8848h	3000 9848h
84Ch	RAT_SLICE_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register	3000 884Ch	3000 984Ch
850h	RAT_SLICE_EOI_REG	EOI Register	3000 8850h	3000 9850h

Table 14-11968. PRU_ICSSG1_RAT_SLICE Registers

Offset	Acronym	Register Name	PRU_ICSSG1_RAT_SLICE0_CFG Physical Address	PRU_ICSSG1_RAT_SLICE1_CFG Physical Address
0h	RAT_SLICE_PID	Revision Register	3008 8000h	3008 9000h
4h	RAT_SLICE_CONFIG	Config Register	3008 8004h	3008 9004h
20h	RAT_SLICE_CTRL_j	Region Control Register	3008 8020h	3008 9020h
24h	RAT_SLICE_BASE_j	Region Base Register	3008 8024h	3008 9024h
28h	RAT_SLICE_TRANS_L_j	Region Translated Lower Address	3008 8028h	3008 9028h
2Ch	RAT_SLICE_TRANS_U_j	Region Translated Upper Address	3008 802Ch	3008 902Ch
804h	RAT_SLICE_DESTINATION_ID	Destination ID Register	3008 8804h	3008 9804h
820h	RAT_SLICE_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	3008 8820h	3008 9820h
824h	RAT_SLICE_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	3008 8824h	3008 9824h
828h	RAT_SLICE_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	3008 8828h	3008 9828h
82Ch	RAT_SLICE_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	3008 882Ch	3008 982Ch
830h	RAT_SLICE_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	3008 8830h	3008 9830h
834h	RAT_SLICE_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	3008 8834h	3008 9834h
838h	RAT_SLICE_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	3008 8838h	3008 9838h
840h	RAT_SLICE_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register	3008 8840h	3008 9840h
844h	RAT_SLICE_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register	3008 8844h	3008 9844h
848h	RAT_SLICE_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register	3008 8848h	3008 9848h
84Ch	RAT_SLICE_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register	3008 884Ch	3008 984Ch
850h	RAT_SLICE_EOI_REG	EOI Register	3008 8850h	3008 9850h

1 RAT_SLICE_PID Register (Offset = 0h) [reset = 66802900h]

RAT_SLICE_PID is shown in Figure 14-3957 and described in Table 14-8014.

Return to Summary Table.

The Revision Register contains the major and minor revisions for the module.

Table 14-11969. RAT_SLICE_PID Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8000h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9000h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8000h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9000h

Figure 14-3957. RAT_SLICE_PID Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="12">FUNC</td></tr>
<tr><td colspan="2">R-1h</td><td colspan="2">R-2h</td><td colspan="12">R-680h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="5">R-5h</td><td colspan="3">R-1h</td><td colspan="2">R-0h</td><td colspan="6">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11971. RAT_SLICE_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	RAT_SLICE_PID register scheme
29-28	BU	R	2h	Business Unit: 10 = Processors
27-16	FUNC	R	680h	Module ID
15-11	RTL	R	5h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

2 RAT_SLICE_CONFIG Register (Offset = 4h) [reset = X]

RAT_SLICE_CONFIG is shown in Figure 14-3958 and described in Table 14-8016.

Return to Summary Table.

The Config Register contains the configuration values for the module.

Table 14-11972. RAT_SLICE_CONFIG Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8004h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9004h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8004h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9004h

Figure 14-3958. RAT_SLICE_CONFIG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">ADDR_WIDTH</td></tr>
<tr><td colspan="8">R-X</td><td colspan="8">R-30h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDRS</td><td colspan="8">REGIONS</td></tr>
<tr><td colspan="8">R-3h</td><td colspan="8">R-4h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11974. RAT_SLICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	ADDR_WIDTH	R	30h	Number of address bits
15-8	ADDRS	R	3h	Number of addresses
7-0	REGIONS	R	4h	Number of regions

3 RAT_SLICE_CTRL_j Register (Offset = 20h + formula) [reset = X]

RAT_SLICE_CTRL_j is shown in Figure 14-3959 and described in Table 14-8018.

Return to Summary Table.

The Control for Region a.

Offset = 20h + (j * 10h); where j = 0h to 3h

Table 14-11975. RAT_SLICE_CTRL_j Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8020h + formula
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9020h + formula
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8020h + formula
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9020h + formula

Figure 14-3959. RAT_SLICE_CTRL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	RESERVED														
R/W-0h	R/W-X														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SIZE					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11977. RAT_SLICE_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the Region
30-6	RESERVED	R/W	X	
5-0	SIZE	R/W	0h	Size of the Region in Address Bits. 0 = 1 byte, 1 = 2 B, 2 = 4 B, 3 = 8 B, etc. up to 32 = 4 GB.Note: The Size of the Region in Address Bits is 2 to the power of N, where N is 0..32

4 RAT_SLICE_BASE_j Register (Offset = 24h + formula) [reset = 0h]

RAT_SLICE_BASE_j is shown in Figure 14-3960 and described in Table 14-8020.

Return to Summary Table.

The Base Address for Region a. This is the source address for matching to a region.

Offset = 24h + (j * 10h); where j = 0h to 3h

Table 14-11978. RAT_SLICE_BASE_j Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8024h + formula
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9024h + formula
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8024h + formula
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9024h + formula

Figure 14-3960. RAT_SLICE_BASE_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11980. RAT_SLICE_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size.

5 RAT_SLICE_TRANS_l_j Register (Offset = 28h + formula) [reset = 0h]

RAT_SLICE_TRANS_l_j is shown in Figure 14-3961 and described in Table 14-8022.

Return to Summary Table.

The Translated Lower Address Bits for Region a.

Offset = 28h + (j * 10h); where j = 0h to 3h

Table 14-11981. RAT_SLICE_TRANS_l_j Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8028h + formula
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9028h + formula
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8028h + formula
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9028h + formula

Figure 14-3961. RAT_SLICE_TRANS_l_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOWER																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-11983. RAT_SLICE_TRANS_l_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOWER	R/W	0h	Translated Lower Address Bits for the Region. It must be aligned to the programmed size.

6 RAT_SLICE_TRANS_U_j Register (Offset = 2Ch + formula) [reset = X]

RAT_SLICE_TRANS_U_j is shown in Figure 14-3962 and described in Table 14-8024.

Return to Summary Table.

The Translated Upper Address Bits for Region a.

Offset = 2Ch + (j * 10h); where j = 0h to 3h

Table 14-11984. RAT_SLICE_TRANS_U_j Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 802Ch + formula
PRU_ICSSG0_RAT_SLICE1_CFG	3000 902Ch + formula
PRU_ICSSG1_RAT_SLICE0_CFG	3008 802Ch + formula
PRU_ICSSG1_RAT_SLICE1_CFG	3008 902Ch + formula

Figure 14-3962. RAT_SLICE_TRANS_U_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																UPPER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11986. RAT_SLICE_TRANS_U_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	UPPER	R/W	0h	Translated Upper Address Bits for the Region

7 RAT_SLICE_DESTINATION_ID Register (Offset = 804h) [reset = X]

RAT_SLICE_DESTINATION_ID is shown in Figure 14-3963 and described in Table 14-8026.

Return to Summary Table.

The Destination ID Register defines the destination ID value for error messages.

Table 14-11987. RAT_SLICE_DESTINATION_ID Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8804h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9804h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8804h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9804h

Figure 14-3963. RAT_SLICE_DESTINATION_ID Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="24">R/W-X</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11989. RAT_SLICE_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID.

8 RAT_SLICE_EXCEPTION_LOGGING_CONTROL Register (Offset = 820h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_CONTROL is shown in Figure 14-3964 and described in Table 14-8028.

Return to Summary Table.

The Exception Logging Control Register controls the exception logging.

Table 14-11990. RAT_SLICE_EXCEPTION_LOGGING_CONTROL Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8820h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9820h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8820h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9820h

Figure 14-3964. RAT_SLICE_EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-11992. RAT_SLICE_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

9 RAT_SLICE_EXCEPTION_LOGGING_HEADER0 Register (Offset = 824h) [reset = 0h]

RAT_SLICE_EXCEPTION_LOGGING_HEADER0 is shown in Figure 14-3965 and described in Table 14-8030.

Return to Summary Table.

The Exception Logging Header 0 Register contains the first word of the header.

Table 14-11993. RAT_SLICE_EXCEPTION_LOGGING_HEADER0 Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8824h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9824h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8824h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9824h

Figure 14-3965. RAT_SLICE_EXCEPTION_LOGGING_HEADER0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TYPE_F</td><td colspan="16">SRC_ID</td><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="16">R-0h</td><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11995. RAT_SLICE_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type. 4 = RAT.
23-8	SRC_ID	R	0h	Source ID.
7-0	DEST_ID	R	0h	Destination ID.

10 RAT_SLICE_EXCEPTION_LOGGING_HEADER1 Register (Offset = 828h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_HEADER1 is shown in Figure 14-3966 and described in Table 14-8032.

Return to Summary Table.

The Exception Logging Header 1 Register contains the second word of the header.

Table 14-11996. RAT_SLICE_EXCEPTION_LOGGING_HEADER1 Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8828h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9828h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8828h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9828h

Figure 14-3966. RAT_SLICE_EXCEPTION_LOGGING_HEADER1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GROUP</td><td colspan="8">CODE</td><td colspan="16">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R-0h</td><td colspan="16">R-X</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-11998. RAT_SLICE_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code. 1 = Boundary crossing error.
15-0	RESERVED	R	X	

11 RAT_SLICE_EXCEPTION_LOGGING_DATA0 Register (Offset = 82Ch) [reset = 0h]

RAT_SLICE_EXCEPTION_LOGGING_DATA0 is shown in Figure 14-3967 and described in Table 14-8034.

Return to Summary Table.

The Exception Logging Data 0 Register contains the first word of the data.

Table 14-11999. RAT_SLICE_EXCEPTION_LOGGING_DATA0 Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 882Ch
PRU_ICSSG0_RAT_SLICE1_CFG	3000 982Ch
PRU_ICSSG1_RAT_SLICE0_CFG	3008 882Ch
PRU_ICSSG1_RAT_SLICE1_CFG	3008 982Ch

Figure 14-3967. RAT_SLICE_EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-12001. RAT_SLICE_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Address lower 32 bits.

12 RAT_SLICE_EXCEPTION_LOGGING_DATA1 Register (Offset = 830h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_DATA1 is shown in Figure 14-3968 and described in Table 14-8036.

Return to Summary Table.

The Exception Logging Data 1 Register contains the second word of the data.

Table 14-12002. RAT_SLICE_EXCEPTION_LOGGING_DATA1 Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8830h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9830h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8830h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9830h

Figure 14-3968. RAT_SLICE_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-X																R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-12004. RAT_SLICE_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	Address upper 12 bits.

13 RAT_SLICE_EXCEPTION_LOGGING_DATA2 Register (Offset = 834h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_DATA2 is shown in Figure 14-3969 and described in Table 14-8038.

Return to Summary Table.

The Exception Logging Data 2 Register contains the third word of the data.

Table 14-12005. RAT_SLICE_EXCEPTION_LOGGING_DATA2 Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8834h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9834h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8834h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9834h

Figure 14-3969. RAT_SLICE_EXCEPTION_LOGGING_DATA2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ROUTEID</td></tr>
<tr><td colspan="4">R-X</td><td colspan="4">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROUTEID</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRITE</td><td>READ</td><td>DEBUG</td><td>CACHEABLE</td><td>PRIV</td><td>SECURE</td></tr>
<tr><td colspan="2">R-X</td><td>R-0h</td><td>R-0h</td><td>R-0h</td><td>R-0h</td><td>R-0h</td><td>R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-12007. RAT_SLICE_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

14 RAT_SLICE_EXCEPTION_LOGGING_DATA3 Register (Offset = 838h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_DATA3 is shown in Figure 14-3970 and described in Table 14-8040.

Return to Summary Table.

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

Table 14-12008. RAT_SLICE_EXCEPTION_LOGGING_DATA3 Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8838h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9838h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8838h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9838h

Figure 14-3970. RAT_SLICE_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						BYTECNT									
R-X																						R-0h									

LEGEND: R = Read Only; -*n* = value after reset

Table 14-12010. RAT_SLICE_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count.

15 RAT_SLICE_EXCEPTION_PEND_SET Register (Offset = 840h) [reset = X]

RAT_SLICE_EXCEPTION_PEND_SET is shown in Figure 14-3971 and described in Table 14-8042.

Return to Summary Table.

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Table 14-12011. RAT_SLICE_EXCEPTION_PEND_SET Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8840h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9840h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8840h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9840h

Figure 14-3971. RAT_SLICE_EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-12013. RAT_SLICE_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

16 RAT_SLICE_EXCEPTION_PEND_CLEAR Register (Offset = 844h) [reset = X]

RAT_SLICE_EXCEPTION_PEND_CLEAR is shown in Figure 14-3972 and described in Table 14-8044.

Return to Summary Table.

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Table 14-12014. RAT_SLICE_EXCEPTION_PEND_CLEAR Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8844h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9844h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8844h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9844h

Figure 14-3972. RAT_SLICE_EXCEPTION_PEND_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-12016. RAT_SLICE_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

17 RAT_SLICE_EXCEPTION_ENABLE_SET Register (Offset = 848h) [reset = X]

RAT_SLICE_EXCEPTION_ENABLE_SET is shown in Figure 14-3973 and described in Table 14-8046.

Return to Summary Table.

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

Table 14-12017. RAT_SLICE_EXCEPTION_ENABLE_SET Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8848h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9848h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8848h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9848h

Figure 14-3973. RAT_SLICE_EXCEPTION_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-12019. RAT_SLICE_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_SET	R/W1S	0h	Write a 1 to set the exception interrupt enable signal.

18 RAT_SLICE_EXCEPTION_ENABLE_CLEAR Register (Offset = 84Ch) [reset = X]

RAT_SLICE_EXCEPTION_ENABLE_CLEAR is shown in Figure 14-3974 and described in Table 14-8048.

Return to Summary Table.

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

Table 14-12020. RAT_SLICE_EXCEPTION_ENABLE_CLEAR Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 884Ch
PRU_ICSSG0_RAT_SLICE1_CFG	3000 984Ch
PRU_ICSSG1_RAT_SLICE0_CFG	3008 884Ch
PRU_ICSSG1_RAT_SLICE1_CFG	3008 984Ch

Figure 14-3974. RAT_SLICE_EXCEPTION_ENABLE_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-12022. RAT_SLICE_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_CLR	R/W1C	0h	Write a 1 to clear the exception interrupt enable signal.

19 RAT_SLICE_EOI_REG Register (Offset = 850h) [reset = X]

RAT_SLICE_EOI_REG is shown in Figure 14-3975 and described in Table 14-8050.

Return to Summary Table.

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-12023. RAT_SLICE_EOI_REG Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	3000 8850h
PRU_ICSSG0_RAT_SLICE1_CFG	3000 9850h
PRU_ICSSG1_RAT_SLICE0_CFG	3008 8850h
PRU_ICSSG1_RAT_SLICE1_CFG	3008 9850h

Figure 14-3975. RAT_SLICE_EOI_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">EOI_WR</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12025. RAT_SLICE_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EOI_WR	R/W	0h	EOI Register

14.3.6.1.34 PRU_TASKS_MGR_TASKS_MGR_PRU_RTU_TX Registers

Table 14-8052, Table 14-8053, Table 14-8054, Table 14-8055, Table 14-8056, and Table 14-8057 list the memory-mapped registers for the PRU_TASKS_MGR_TASKS_MGR_PRU0, PRU_TASKS_MGR_TASKS_MGR_RTU0, PRU_TASKS_MGR_TASKS_MGR_PRU1, PRU_TASKS_MGR_TASKS_MGR_RTU1, PRU_TASKS_MGR_TASKS_MGR_PRU_TX0 and PRU_TASKS_MGR_TASKS_MGR_PRU_TX1. All register offset addresses not listed in Table 14-8052 to Table 14-8057 should be considered as reserved locations and the register contents should not be modified.

Table 14-12026. PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Instances

Instance	Base Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A000h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A000h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A100h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A100h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A200h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A200h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A300h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A300h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Table 14-12027. PRU_TASKS_MGR_TASKS_MGR_PRU0 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	3002 A000h	300A A000h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	3002 A004h	300A A004h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	3002 A008h	300A A008h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	3002 A00Ch	300A A00Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	3002 A010h	300A A010h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	3002 A014h	300A A014h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	3002 A018h	300A A018h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	3002 A01Ch	300A A01Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	3002 A020h	300A A020h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	3002 A024h	300A A024h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	3002 A028h	300A A028h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	3002 A02Ch	300A A02Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	3002 A030h	300A A030h
34h	TASKS_MGR_TX_CFG	TX Configuration	3002 A034h	300A A034h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	3002 A038h	300A A038h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	3002 A03Ch	300A A03Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	3002 A040h	300A A040h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	3002 A044h	300A A044h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	3002 A048h	300A A048h

Table 14-12028. PRU_TASKS_MGR_TASKS_MGR_RTU0 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	3002 A100h	300A A100h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	3002 A104h	300A A104h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	3002 A108h	300A A108h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	3002 A10Ch	300A A10Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	3002 A110h	300A A110h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	3002 A114h	300A A114h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	3002 A118h	300A A118h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	3002 A11Ch	300A A11Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	3002 A120h	300A A120h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	3002 A124h	300A A124h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	3002 A128h	300A A128h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	3002 A12Ch	300A A12Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	3002 A130h	300A A130h
34h	TASKS_MGR_TX_CFG	TX Configuration	3002 A134h	300A A134h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	3002 A138h	300A A138h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	3002 A13Ch	300A A13Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	3002 A140h	300A A140h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	3002 A144h	300A A144h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	3002 A148h	300A A148h

Table 14-12029. PRU_TASKS_MGR_TASKS_MGR_PRU1 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	3002 A200h	300A A200h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	3002 A204h	300A A204h
8h	TASKS_MGR_TS1_PC_S0	TS1 Sub0 PC	3002 A208h	300A A208h
Ch	TASKS_MGR_TS1_PC_S1	TS1 Sub1 PC	3002 A20Ch	300A A20Ch
10h	TASKS_MGR_TS1_PC_S2	TS1 Sub2 PC	3002 A210h	300A A210h
14h	TASKS_MGR_TS1_PC_S3	TS1 Sub3 PC	3002 A214h	300A A214h
18h	TASKS_MGR_TS1_PC_S4	TS1 Sub4 PC	3002 A218h	300A A218h
1Ch	TASKS_MGR_TS2_PC_S0	TS2 Sub0 PC	3002 A21Ch	300A A21Ch
20h	TASKS_MGR_TS2_PC_S1	TS2 Sub1 PC	3002 A220h	300A A220h
24h	TASKS_MGR_TS2_PC_S2	TS2 Sub2 PC	3002 A224h	300A A224h
28h	TASKS_MGR_TS2_PC_S3	TS2 Sub3 PC	3002 A228h	300A A228h
2Ch	TASKS_MGR_TS2_PC_S4	TS2 Sub4 PC	3002 A22Ch	300A A22Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	3002 A230h	300A A230h
34h	TASKS_MGR_TX_CFG	TX Configuration	3002 A234h	300A A234h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	3002 A238h	300A A238h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	3002 A23Ch	300A A23Ch

Table 14-12029. PRU_TASKS_MGR_TASKS_MGR_PRU1 Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR Physical Address
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	3002 A240h	300A A240h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	3002 A244h	300A A244h
48h	TASKS_MGR_CAP_EN_CFG	Enable capture new event cfg	3002 A248h	300A A248h

Table 14-12030. PRU_TASKS_MGR_TASKS_MGR_RTU1 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	3002 A300h	300A A300h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	3002 A304h	300A A304h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	3002 A308h	300A A308h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	3002 A30Ch	300A A30Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	3002 A310h	300A A310h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	3002 A314h	300A A314h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	3002 A318h	300A A318h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	3002 A31Ch	300A A31Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	3002 A320h	300A A320h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	3002 A324h	300A A324h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	3002 A328h	300A A328h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	3002 A32Ch	300A A32Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	3002 A330h	300A A330h
34h	TASKS_MGR_TX_CFG	TX Configuration	3002 A334h	300A A334h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	3002 A338h	300A A338h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	3002 A33Ch	300A A33Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	3002 A340h	300A A340h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	3002 A344h	300A A344h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	3002 A348h	300A A348h

Table 14-12031. PRU_TASKS_MGR_TASKS_MGR_PRU_TX0

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	3002 A400h	300A A400h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	3002 A404h	300A A404h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	3002 A408h	300A A408h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	3002 A40Ch	300A A40Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	3002 A410h	300A A410h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	3002 A414h	300A A414h

Table 14-12031. PRU_TASKS_MGR_TASKS_MGR_PRU_TX0 (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR Physical Address
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	3002 A418h	300A A418h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	3002 A41Ch	300A A41Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	3002 A420h	300A A420h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	3002 A424h	300A A424h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	3002 A428h	300A A428h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	3002 A42Ch	300A A42Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	3002 A430h	300A A430h
34h	TASKS_MGR_TX_CFG	TX Configuration	3002 A434h	300A A434h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	3002 A438h	300A A438h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	3002 A43Ch	300A A43Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	3002 A440h	300A A440h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	3002 A444h	300A A444h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	3002 A448h	300A A448h

Table 14-12032. PRU_TASKS_MGR_TASKS_MGR_PRU_TX1

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	3002 A500h	300A A500h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	3002 A504h	300A A504h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	3002 A508h	300A A508h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	3002 A50Ch	300A A50Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	3002 A510h	300A A510h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	3002 A514h	300A A514h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	3002 A518h	300A A518h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	3002 A51Ch	300A A51Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	3002 A520h	300A A520h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	3002 A524h	300A A524h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	3002 A528h	300A A528h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	3002 A52Ch	300A A52Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	3002 A530h	300A A530h
34h	TASKS_MGR_TX_CFG	TX Configuration	3002 A534h	300A A534h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	3002 A538h	300A A538h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	3002 A53Ch	300A A53Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	3002 A540h	300A A540h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	3002 A544h	300A A544h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	3002 A548h	300A A548h

1 TASKS_MGR_GLOBAL_CFG Register (Offset = 0h) [reset = X]

TASKS_MGR_GLOBAL_CFG is shown in Figure 14-3976 and described in Table 14-8059.

Return to Summary Table.

Global Configuration

Table 14-12033. TASKS_MGR_GLOBAL_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A000h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A000h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A100h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A100h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A200h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A200h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A300h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A300h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3976. TASKS_MGR_GLOBAL_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TS2_EN_S4	TS2_EN_S3	TS2_EN_S2	TS2_EN_S1
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS2_EN_S0	TS1_EN_S4	TS1_EN_S3	TS1_EN_S2	TS1_EN_S1	TS1_EN_S0	TASKS_MGR_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12035. TASKS_MGR_GLOBAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11	TS2_EN_S4	R/W	0h	TS2 Sub4 0: Disabled 1: Enabled
10	TS2_EN_S3	R/W	0h	TS2 Sub3 0: Disabled 1: Enabled
9	TS2_EN_S2	R/W	0h	TS2 Sub2 0: Disabled 1: Enabled
8	TS2_EN_S1	R/W	0h	TS2 Sub1 0: Disabled 1: Enabled

Table 14-12035. TASKS_MGR_GLOBAL_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TS2_EN_S0	R/W	0h	TS2 Sub0 0: Disabled 1: Enabled
6	TS1_EN_S4	R/W	0h	TS1 Sub4 0: Disabled 1: Enabled
5	TS1_EN_S3	R/W	0h	TS1 Sub3 0: Disabled 1: Enabled
4	TS1_EN_S2	R/W	0h	TS1 Sub2 0: Disabled 1: Enabled
3	TS1_EN_S1	R/W	0h	TS1 Sub1 0: Disabled 1: Enabled
2	TS1_EN_S0	R/W	0h	TS1 Sub0 0: Disabled 1: Enabled
1-0	TASKS_MGR_MODE	R/W	0h	TaskSwap Mode 0: Disabled 1: RXTX 2: General_HW

2 TASKS_MGR_GLOBAL_STATUS Register (Offset = 4h) [reset = X]

TASKS_MGR_GLOBAL_STATUS is shown in Figure 14-3977 and described in Table 14-8061.

Return to Summary Table.

Global Status

Table 14-12036. TASKS_MGR_GLOBAL_STATUS Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A004h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A004h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A104h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A104h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A204h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A204h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A304h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A304h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3977. TASKS_MGR_GLOBAL_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							

23	22	21	20	19	18	17	16
RESERVED						TS2_SUB_PEND_4	TS2_SUB_PEND_3
R-X						R-0h	R-0h

15	14	13	12	11	10	9	8
TS2_SUB_PEND_2	TS2_SUB_PEND_1	TS2_SUB_PEND_0	TS1_SUB_PEND_4	TS1_SUB_PEND_3	TS1_SUB_PEND_2	TS1_SUB_PEND_1	TS1_SUB_PEND_0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

7	6	5	4	3	2	1	0
TS2_STATE				TS1_STATE			
R-0h				R-0h			

LEGEND: R = Read Only; -*n* = value after reset

Table 14-12038. TASKS_MGR_GLOBAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17	TS2_SUB_PEND_4	R	0h	Task2 Sub4 Pend State
16	TS2_SUB_PEND_3	R	0h	Task2 Sub3 Pend State
15	TS2_SUB_PEND_2	R	0h	Task2 Sub2 Pend State
14	TS2_SUB_PEND_1	R	0h	Task2 Sub1 Pend State
13	TS2_SUB_PEND_0	R	0h	Task2 Sub0 Pend State
12	TS1_SUB_PEND_4	R	0h	Task1 Sub4 Pend State
11	TS1_SUB_PEND_3	R	0h	Task1 Sub3 Pend State
10	TS1_SUB_PEND_2	R	0h	Task1 Sub2 Pend State

Table 14-12038. TASKS_MGR_GLOBAL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	TS1_SUB_PEND_1	R	0h	Task1 Sub1 Pend State
8	TS1_SUB_PEND_0	R	0h	Task1 Sub0 Pend State
7-4	TS2_STATE	R	0h	Indicates the sub-tasks of Task2 State 4b'0000 = TS2_Idle 4b'0001 = TS2_S0 4b'0010 = TS2_S1 4b'0011 = TS2_S2 4b'0100 = TS2_S3 4b'0101 = TS2_S4 4b'0110...4b'1111 = Reserved
3-0	TS1_STATE	R	0h	Indicates the sub-tasks of Task1 State 4b'0000 = TS1_Idle 4b'0001 = TS1_S0 4b'0010 = TS1_S1 4b'0011 = TS1_S2 4b'0100 = TS1_S3 4b'0101 = TS1_S4 4b'0110...4b'1111 = Reserved

3 TASKS_MGR_TS1_PC_S0 Register (Offset = 8h) [reset = X]

TASKS_MGR_TS1_PC_S0 is shown in Figure 14-3978 and described in Table 14-8063.

Return to Summary Table.

TS1 Sub0 PC

Table 14-12039. TASKS_MGR_TS1_PC_S0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A008h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A008h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A108h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A108h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A208h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A208h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A308h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A308h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3978. TASKS_MGR_TS1_PC_S0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="18">RESERVED</td><td colspan="14">TS1_PC_S0</td></tr>
<tr><td colspan="18">R/W-X</td><td colspan="14">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12041. TASKS_MGR_TS1_PC_S0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S0	R/W	0h	TS1 Sub0 Program Counter (function pointer in code word units i.e function offset in byte address/4)

4 TASKS_MGR_TS1_PC_S1 Register (Offset = Ch) [reset = X]

TASKS_MGR_TS1_PC_S1 is shown in Figure 14-3979 and described in Table 14-8065.

Return to Summary Table.

TS1 Sub1 PC

Table 14-12042. TASKS_MGR_TS1_PC_S1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A00Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A00Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A10Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A10Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A20Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A20Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A30Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A30Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3979. TASKS_MGR_TS1_PC_S1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS1_PC_S1													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12044. TASKS_MGR_TS1_PC_S1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S1	R/W	0h	TS1 Sub1 Program Counter (function pointer in code word units i.e function offset in byte address/4)

5 TASKS_MGR_TS1_PC_S2 Register (Offset = 10h) [reset = X]

TASKS_MGR_TS1_PC_S2 is shown in Figure 14-3980 and described in Table 14-8067.

Return to Summary Table.

TS1 Sub2 PC

Table 14-12045. TASKS_MGR_TS1_PC_S2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A010h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A010h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A110h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A110h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A210h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A210h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A310h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A310h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3980. TASKS_MGR_TS1_PC_S2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS1_PC_S2													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12047. TASKS_MGR_TS1_PC_S2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S2	R/W	0h	TS1 Sub2 Program Counter (function pointer in code word units i.e function offset in byte address/4)

6 TASKS_MGR_TS1_PC_S3 Register (Offset = 14h) [reset = X]

TASKS_MGR_TS1_PC_S3 is shown in Figure 14-3981 and described in Table 14-8069.

Return to Summary Table.

TS1 Sub3 PC

Table 14-12048. TASKS_MGR_TS1_PC_S3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A014h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A014h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A114h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A114h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A214h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A214h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A314h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A314h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3981. TASKS_MGR_TS1_PC_S3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS1_PC_S3													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12050. TASKS_MGR_TS1_PC_S3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S3	R/W	0h	TS1 Sub3 Program Counter (function pointer in code word units i.e function offset in byte address/4)

7 TASKS_MGR_TS1_PC_S4 Register (Offset = 18h) [reset = X]

TASKS_MGR_TS1_PC_S4 is shown in Figure 14-3982 and described in Table 14-8071.

Return to Summary Table.

TS1 Sub4 PC

Table 14-12051. TASKS_MGR_TS1_PC_S4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A018h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A018h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A118h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A118h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A218h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A218h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A318h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A318h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3982. TASKS_MGR_TS1_PC_S4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS1_PC_S4													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12053. TASKS_MGR_TS1_PC_S4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S4	R/W	0h	TS1 Sub4 Program Counter (function pointer in code word units i.e function offset in byte address/4)

8 TASKS_MGR_TS2_PC_S0 Register (Offset = 1Ch) [reset = X]

TASKS_MGR_TS2_PC_S0 is shown in Figure 14-3983 and described in Table 14-8073.

Return to Summary Table.

TS2 Sub0 PC

Table 14-12054. TASKS_MGR_TS2_PC_S0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A01Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A01Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A11Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A11Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A21Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A21Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A31Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A31Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3983. TASKS_MGR_TS2_PC_S0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS2_PC_S0														
R/W-X																		R/W-0h														

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-12056. TASKS_MGR_TS2_PC_S0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S0	R/W	0h	TS2 Sub0 Program Counter (function pointer in code word units i.e function offset in byte address/4)

9 TASKS_MGR_TS2_PC_S1 Register (Offset = 20h) [reset = X]

TASKS_MGR_TS2_PC_S1 is shown in Figure 14-3984 and described in Table 14-8075.

Return to Summary Table.

TS2 Sub1 PC

Table 14-12057. TASKS_MGR_TS2_PC_S1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A020h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A020h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A120h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A120h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A220h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A220h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A320h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A320h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3984. TASKS_MGR_TS2_PC_S1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="18">RESERVED</td><td colspan="14">TS2_PC_S1</td></tr>
<tr><td colspan="18">R/W-X</td><td colspan="14">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12059. TASKS_MGR_TS2_PC_S1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S1	R/W	0h	TS2 Sub1 Program Counter (function pointer in code word units i.e function offset in byte address/4)

10 TASKS_MGR_TS2_PC_S2 Register (Offset = 24h) [reset = X]

TASKS_MGR_TS2_PC_S2 is shown in Figure 14-3985 and described in Table 14-8077.

Return to Summary Table.

TS2 Sub2 PC

Table 14-12060. TASKS_MGR_TS2_PC_S2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A024h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A024h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A124h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A124h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A224h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A224h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A324h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A324h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3985. TASKS_MGR_TS2_PC_S2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="18">RESERVED</td><td colspan="14">TS2_PC_S2</td></tr>
<tr><td colspan="18">R/W-X</td><td colspan="14">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12062. TASKS_MGR_TS2_PC_S2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S2	R/W	0h	TS2 Sub2 Program Counter (function pointer in code word units i.e function offset in byte address/4)

11 TASKS_MGR_TS2_PC_S3 Register (Offset = 28h) [reset = X]

TASKS_MGR_TS2_PC_S3 is shown in Figure 14-3986 and described in Table 14-8079.

Return to Summary Table.

TS2 Sub3 PC

Table 14-12063. TASKS_MGR_TS2_PC_S3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A028h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A028h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A128h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A128h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A228h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A228h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A328h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A328h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3986. TASKS_MGR_TS2_PC_S3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS2_PC_S3													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12065. TASKS_MGR_TS2_PC_S3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S3	R/W	0h	TS2 Sub3 Program Counter (function pointer in code word units i.e function offset in byte address/4)

12 TASKS_MGR_TS2_PC_S4 Register (Offset = 2Ch) [reset = X]

TASKS_MGR_TS2_PC_S4 is shown in Figure 14-3987 and described in Table 14-8081.

Return to Summary Table.

TS2 Sub4 PC

Table 14-12066. TASKS_MGR_TS2_PC_S4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A02Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A02Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A12Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A12Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A22Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A22Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A32Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A32Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3987. TASKS_MGR_TS2_PC_S4 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="18">RESERVED</td><td colspan="14">TS2_PC_S4</td></tr>
<tr><td colspan="18">R/W-X</td><td colspan="14">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12068. TASKS_MGR_TS2_PC_S4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S4	R/W	0h	TS2 Sub4 Program Counter (function pointer in code word units i.e function offset in byte address/4)

13 TASKS_MGR_RX_CFG Register (Offset = 30h) [reset = X]

TASKS_MGR_RX_CFG is shown in Figure 14-3988 and described in Table 14-8083.

Return to Summary Table.

RX Configuration

Table 14-12069. TASKS_MGR_RX_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A030h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A030h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A130h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A130h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A230h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A230h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A330h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A330h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3988. TASKS_MGR_RX_CFG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="5">BKN_SIZE</td><td colspan="5">BK2_SIZE</td><td colspan="5">BK1_SIZE</td></tr>
<tr><td>R/W-X</td><td colspan="5">R/W-1Fh</td><td colspan="5">R/W-1Fh</td><td colspan="5">R/W-1Fh</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12071. TASKS_MGR_RX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-10	BKN_SIZE	R/W	1Fh	RX BKN Size, After BK1 and BK2, then after another 1 to 32 Bytes
9-5	BK2_SIZE	R/W	1Fh	RX BK2 Size, The Second 1 to 32 Bytes trigger
4-0	BK1_SIZE	R/W	1Fh	RX BK1 Size, The first 1 to 32 Bytes trigger

14 TASKS_MGR_TX_CFG Register (Offset = 34h) [reset = X]

TASKS_MGR_TX_CFG is shown in Figure 14-3989 and described in Table 14-8085.

Return to Summary Table.

TX Configuration

Table 14-12072. TASKS_MGR_TX_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A034h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A034h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A134h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A134h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A234h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A234h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A334h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A334h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3989. TASKS_MGR_TX_CFG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="26">RESERVED</td><td colspan="6">TX_WM</td></tr>
<tr><td colspan="26">R/W-X</td><td colspan="6">R/W-1Fh</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12074. TASKS_MGR_TX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	TX_WM	R/W	1Fh	TX L2 Water Mark Level 1 to 64 Bytes

15 TASKS_MGR_TS1_GEN_CFG1 Register (Offset = 38h) [reset = 0h]

TASKS_MGR_TS1_GEN_CFG1 is shown in Figure 14-3990 and described in Table 14-8087.

Return to Summary Table.

Generic TS1 Configuration1

Table 14-12075. TASKS_MGR_TS1_GEN_CFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A038h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A038h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A138h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A138h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A238h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A238h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A338h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A338h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3990. TASKS_MGR_TS1_GEN_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS1_GEN_S3_MX								TS1_GEN_S2_MX							
R/W-0h								R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS1_GEN_S1_MX								TS1_GEN_S0_MX							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12077. TASKS_MGR_TS1_GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TS1_GEN_S3_MX	R/W	0h	TS1 Generic Sub3 MX Select
23-16	TS1_GEN_S2_MX	R/W	0h	TS1 Generic Sub2 MX Select
15-8	TS1_GEN_S1_MX	R/W	0h	TS1 Generic Sub1 MX Select
7-0	TS1_GEN_S0_MX	R/W	0h	TS1 Generic Sub0 MX Select

16 TASKS_MGR_TS1_GEN_CFG2 Register (Offset = 3Ch) [reset = X]

TASKS_MGR_TS1_GEN_CFG2 is shown in Figure 14-3991 and described in Table 14-8089.

Return to Summary Table.

Generic TS1 Configuration2

Table 14-12078. TASKS_MGR_TS1_GEN_CFG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A03Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A03Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A13Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A13Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A23Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A23Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A33Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A33Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3991. TASKS_MGR_TS1_GEN_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS1_GEN_S4_MX							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12080. TASKS_MGR_TS1_GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS1_GEN_S4_MX	R/W	0h	TS1 Generic Sub4 MX Select

17 TASKS_MGR_TS2_GEN_CFG1 Register (Offset = 40h) [reset = 0h]

TASKS_MGR_TS2_GEN_CFG1 is shown in Figure 14-3992 and described in Table 14-8091.

Return to Summary Table.

Generic TS2 Configuration1

Table 14-12081. TASKS_MGR_TS2_GEN_CFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A040h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A040h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A140h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A140h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A240h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A240h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A340h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A340h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3992. TASKS_MGR_TS2_GEN_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS2_GEN_S3_MX								TS2_GEN_S2_MX							
R/W-0h								R/W-0h							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS2_GEN_S1_MX								TS2_GEN_S0_MX							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-12083. TASKS_MGR_TS2_GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TS2_GEN_S3_MX	R/W	0h	TS2 Generic Sub3 MX Select
23-16	TS2_GEN_S2_MX	R/W	0h	TS2 Generic Sub2 MX Select
15-8	TS2_GEN_S1_MX	R/W	0h	TS2 Generic Sub1 MX Select
7-0	TS2_GEN_S0_MX	R/W	0h	TS2 Generic Sub0 MX Select

18 TASKS_MGR_TS2_GEN_CFG2 Register (Offset = 44h) [reset = X]

TASKS_MGR_TS2_GEN_CFG2 is shown in Figure 14-3993 and described in Table 14-8093.

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Generic TS2 Configuration2

Table 14-12084. TASKS_MGR_TS2_GEN_CFG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A044h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A044h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A144h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A144h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A244h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A244h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A344h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A344h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3993. TASKS_MGR_TS2_GEN_CFG2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">TS2_GEN_S4_MX</td></tr>
<tr><td colspan="8">R/W-X</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12086. TASKS_MGR_TS2_GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS2_GEN_S4_MX	R/W	0h	TS2 Generic Sub4 MX Select

19 TASKS_MGR_CAP_EN_CFG Register (Offset = 48h) [reset = X]

TASKS_MGR_CAP_EN_CFG is shown in Figure 14-3994 and described in Table 14-8095.

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This register allows you to enable a capture of a new event when you are active in the sub task. By default, all new events to the same active task are masked until you exit that sub task from being captured When disabled (reset state). All new events to the current active task are masked from being captured. Only when this task is completed a new event can get captured for that task. When enabled, a new event which occurs in a current active task will get captured, when that task yields it will reenter that same task if not other higher priority events are pending

Table 14-12087. TASKS_MGR_CAP_EN_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	3002 A048h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	300A A048h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	3002 A148h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	300A A148h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	3002 A248h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	300A A248h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	3002 A348h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	300A A348h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	3002 A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	300A A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	3002 A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	300A A500h

Figure 14-3994. TASKS_MGR_CAP_EN_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			CAP_NEW_TS1_EN_S4	CAP_NEW_TS1_EN_S3	CAP_NEW_TS1_EN_S2	CAP_NEW_TS1_EN_S1	CAP_NEW_TS1_EN_S0
R/W-X			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-12089. TASKS_MGR_CAP_EN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	CAP_NEW_TS1_EN_S4	R/W	0h	Capture new event enable. TS1 Sub4.
3	CAP_NEW_TS1_EN_S3	R/W	0h	Capture new event enable. TS1 Sub3.
2	CAP_NEW_TS1_EN_S2	R/W	0h	Capture new event enable. TS1 Sub2.
1	CAP_NEW_TS1_EN_S1	R/W	0h	Capture new event enable. TS1 Sub1.

Table 14-12089. TASKS_MGR_CAP_EN_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CAP_NEW_TS1_EN_S0	R/W	0h	Capture new event enable. TS1 Sub0.

14.3.6.1.35 PRU_ICSSG_RAM Registers

Table 14-8097 lists the memory-mapped registers for the PRU_ICSSG_RAM registers. All register offset addresses not listed in Table 14-8097 should be considered as reserved locations and the register contents should not be modified.

Table 14-12090. PRU_ICSSG_RAM Instances

Instance	Base Address
PRU_ICSSG0_RAM_SLV_RAM	3001 0000h
PRU_ICSSG1_RAM_SLV_RAM	3009 0000h

Table 14-12091. PRU_ICSSG_RAM Registers

Offset	Acronym	Register Name	PRU_ICSSG0_RAM_SLV_RAM Physical Address	PRU_ICSSG1_RAM_SLV_RAM Physical Address
0h + formula	ICSSG_RAM_REG_y	RAM memory word	3001 0000h + formula	3009 0000h + formula

1 ICSSG_RAM_REG_y Register (Offset = 0h + formula) [reset = 0h]

ICSSG_RAM_REG_y is shown in Figure 14-3995 and described in Table 14-8099.

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The RAM memory words provide memory mapped random access data storage.

Offset = 0h + (y * 4h); where y = 0h to 3FFFh

Table 14-12092. ICSSG_RAM_REG_y Instances

Instance	Physical Address
PRU_ICSSG0_RAM_SLV_RAM	3001 0000h + formula
PRU_ICSSG1_RAM_SLV_RAM	3009 0000h + formula

Figure 14-3995. ICSSG_RAM_REG_y Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTE3</td><td colspan="8">BYTE2</td><td colspan="8">BYTE1</td><td colspan="8">BYTE0</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-12094. ICSSG_RAM_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BYTE3	R/W	0h	This is the MSB (Most Significant Byte)
23-16	BYTE2	R/W	0h	This is the UMB (Upper Middle Byte)
15-8	BYTE1	R/W	0h	This is the LMB (Lower Middle Byte)
7-0	BYTE0	R/W	0h	This is the LSB (Least Significant Byte)

14.4 Interprocessor Communication Registers

14.4.1 MAILBOX_MAILBOX_CLUSTER_0

MAILBOX_MAILBOX_CLUSTER_0

14.4.1.1 MAILBOX_MAILBOX_CLUSTER_0 Summaries

MAILBOX_MAILBOX_CLUSTER_0 Summaries

Table 14-12095. MAILBOX Registers, Base Address=2900 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_0 Physical Address
0h	32	MAILBOX_REVISION	2900 0000h
10h	32	MAILBOX_SYSCONFIG	2900 0010h
40h	32	MAILBOX_MESSAGE_J	2900 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2900 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2900 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2900 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2900 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2900 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2900 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2900 000Ch + formula

14.4.1.2 MAILBOX_MAILBOX_CLUSTER_0 Registers

MAILBOX_MAILBOX_CLUSTER_0 Registers

14.4.1.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12096. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0000h**

Figure 14-3996. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-12098. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.1.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-12099. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0010h**

Figure 14-3997. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-12101. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.1.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12102. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0040h + formula**

Figure 14-3998. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-12104. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.1.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12105. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0080h + formula**

Figure 14-3999. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-12107. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.1.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12108. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 00C0h + formula**

Figure 14-4000. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-12110. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.1.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-12111. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0140h**

Figure 14-4001. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-12113. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.1.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12114. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0000h + formula**

Figure 14-4002. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-12116. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-12116. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-12116. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.1.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12117. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0004h + formula**

Figure 14-4003. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12119. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-12119. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-12119. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.1.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12120. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 0008h + formula**

Figure 14-4004. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12122. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12122. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12122. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.1.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12123. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	**2900 000Ch + formula**

Figure 14-4005. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12125. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12125. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12125. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.2 MAILBOX_MAILBOX_CLUSTER_1

MAILBOX_MAILBOX_CLUSTER_1

14.4.2.1 MAILBOX_MAILBOX_CLUSTER_1 Summaries

MAILBOX_MAILBOX_CLUSTER_1 Summaries

Table 14-12126. MAILBOX Registers, Base Address=2901 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_1 Physical Address
0h	32	MAILBOX_REVISION	2901 0000h
10h	32	MAILBOX_SYSCONFIG	2901 0010h
40h	32	MAILBOX_MESSAGE_J	2901 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2901 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2901 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2901 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2901 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2901 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2901 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2901 000Ch + formula

14.4.2.2 MAILBOX_MAILBOX_CLUSTER_1 Registers

MAILBOX_MAILBOX_CLUSTER_1 Registers

14.4.2.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12127. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0000h

Figure 14-4006. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-12129. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.2.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-12130. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0010h**

Figure 14-4007. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-12132. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.2.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12133. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0040h + formula

Figure 14-4008. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-12135. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.2.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12136. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0080h + formula**

Figure 14-4009. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-12138. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.2.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12139. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 00C0h + formula

Figure 14-4010. MAILBOX_MSG_STATUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_MESSAGES</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-12141. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.2.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-12142. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0140h**

Figure 14-4011. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-12144. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.2.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12145. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0000h + formula**

Figure 14-4012. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-12147. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-12147. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-12147. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.2.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12148. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0004h + formula**

Figure 14-4013. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12150. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-12150. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-12150. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.2.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12151. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 0008h + formula**

Figure 14-4014. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12153. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12153. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12153. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.2.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12154. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	**2901 000Ch + formula**

Figure 14-4015. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12156. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12156. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12156. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.3 MAILBOX_MAILBOX_CLUSTER_2

MAILBOX_MAILBOX_CLUSTER_2

14.4.3.1 MAILBOX_MAILBOX_CLUSTER_2 Summaries

MAILBOX_MAILBOX_CLUSTER_2 Summaries

Table 14-12157. MAILBOX Registers, Base Address=2902 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_2 Physical Address
0h	32	MAILBOX_REVISION	2902 0000h
10h	32	MAILBOX_SYSCONFIG	2902 0010h
40h	32	MAILBOX_MESSAGE_J	2902 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2902 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2902 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2902 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2902 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2902 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2902 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2902 000Ch + formula

14.4.3.2 MAILBOX_MAILBOX_CLUSTER_2 Registers

MAILBOX_MAILBOX_CLUSTER_2 Registers

14.4.3.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12158. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0000h**

Figure 14-4016. MAILBOX_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6FCh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6FCh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">12h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-12160. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.3.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-12161. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0010h**

Figure 14-4017. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-12163. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.3.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12164. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0040h + formula**

Figure 14-4018. MAILBOX_MESSAGE_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MESSAGE_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MESSAGE_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MESSAGE_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MESSAGE_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12166. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.3.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12167. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0080h + formula**

Figure 14-4019. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-12169. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.3.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12170. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 00C0h + formula**

Figure 14-4020. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-12172. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.3.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-12173. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0140h

Figure 14-4021. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-12175. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.3.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12176. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0000h + formula**

Figure 14-4022. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTAT USMB15	NEWMSGSTAT USMB15	NOTFULLSTAT USMB14	NEWMSGSTAT USMB14	NOTFULLSTAT USMB13	NEWMSGSTAT USMB13	NOTFULLSTAT USMB12	NEWMSGSTAT USMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTAT USMB11	NEWMSGSTAT USMB11	NOTFULLSTAT USMB10	NEWMSGSTAT USMB10	NOTFULLSTAT USMB9	NEWMSGSTAT USMB9	NOTFULLSTAT USMB8	NEWMSGSTAT USMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTAT USMB7	NEWMSGSTAT USMB7	NOTFULLSTAT USMB6	NEWMSGSTAT USMB6	NOTFULLSTAT USMB5	NEWMSGSTAT USMB5	NOTFULLSTAT USMB4	NEWMSGSTAT USMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTAT USMB3	NEWMSGSTAT USMB3	NOTFULLSTAT USMB2	NEWMSGSTAT USMB2	NOTFULLSTAT USMB1	NEWMSGSTAT USMB1	NOTFULLSTAT USMB0	NEWMSGSTAT USMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-12178. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-12178. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-12178. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.3.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12179. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0004h + formula**

Figure 14-4023. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12181. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-12181. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-12181. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.3.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12182. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 0008h + formula**

Figure 14-4024. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12184. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12184. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12184. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.3.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12185. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	**2902 000Ch + formula**

Figure 14-4025. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12187. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12187. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12187. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.4 MAILBOX_MAILBOX_CLUSTER_3

MAILBOX_MAILBOX_CLUSTER_3

14.4.4.1 MAILBOX_MAILBOX_CLUSTER_3 Summaries

MAILBOX_MAILBOX_CLUSTER_3 Summaries

Table 14-12188. MAILBOX Registers, Base Address=2903 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_3 Physical Address
0h	32	MAILBOX_REVISION	2903 0000h
10h	32	MAILBOX_SYSCONFIG	2903 0010h
40h	32	MAILBOX_MESSAGE_J	2903 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2903 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2903 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2903 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2903 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2903 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2903 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2903 000Ch + formula

14.4.4.2 MAILBOX_MAILBOX_CLUSTER_3 Registers

MAILBOX_MAILBOX_CLUSTER_3 Registers

14.4.4.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12189. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0000h**

Figure 14-4026. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-12191. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.4.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-12192. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0010h**

Figure 14-4027. MAILBOX_SYSCONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFT_RESET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12194. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.4.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12195. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0040h + formula**

Figure 14-4028. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-12197. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.4.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12198. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0080h + formula**

Figure 14-4029. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-12200. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.4.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12201. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 00C0h + formula**

Figure 14-4030. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-12203. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.4.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-12204. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0140h**

Figure 14-4031. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-12206. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.4.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12207. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0000h + formula**

Figure 14-4032. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-12209. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-12209. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-12209. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.4.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12210. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0004h + formula**

Figure 14-4033. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12212. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-12212. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-12212. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.4.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12213. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 0008h + formula**

Figure 14-4034. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12215. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12215. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12215. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.4.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12216. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	**2903 000Ch + formula**

Figure 14-4035. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12218. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12218. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12218. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.5 MAILBOX_MAILBOX_CLUSTER_4

MAILBOX_MAILBOX_CLUSTER_4

14.4.5.1 MAILBOX_MAILBOX_CLUSTER_4 Summaries

MAILBOX_MAILBOX_CLUSTER_4 Summaries

Table 14-12219. MAILBOX Registers, Base Address=2904 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_4 Physical Address
0h	32	MAILBOX_REVISION	2904 0000h
10h	32	MAILBOX_SYSCONFIG	2904 0010h
40h	32	MAILBOX_MESSAGE_J	2904 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2904 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2904 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2904 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2904 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2904 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2904 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2904 000Ch + formula

14.4.5.2 MAILBOX_MAILBOX_CLUSTER_4 Registers

MAILBOX_MAILBOX_CLUSTER_4 Registers

14.4.5.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12220. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 0000h**

Figure 14-4036. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
6FCh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-12222. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.5.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-12223. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 0010h**

Figure 14-4037. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-12225. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.5.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12226. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 0040h + formula**

Figure 14-4038. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-12228. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.5.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12229. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 0080h + formula**

Figure 14-4039. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-12231. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.5.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12232. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 00C0h + formula**

Figure 14-4040. MAILBOX_MSG_STATUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_MESSAGES</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-12234. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.5.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-12235. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 0140h**

Figure 14-4041. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-12237. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.5.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12238. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 0000h + formula**

Figure 14-4042. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-12240. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-12240. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-12240. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.5.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12241. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 0004h + formula**

Figure 14-4043. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12243. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-12243. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-12243. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.5.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12244. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 0008h + formula**

Figure 14-4044. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12246. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12246. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12246. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.5.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12247. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	**2904 000Ch + formula**

Figure 14-4045. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12249. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12249. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12249. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.6 MAILBOX_MAILBOX_CLUSTER_5

MAILBOX_MAILBOX_CLUSTER_5

14.4.6.1 MAILBOX_MAILBOX_CLUSTER_5 Summaries

MAILBOX_MAILBOX_CLUSTER_5 Summaries

Table 14-12250. MAILBOX Registers, Base Address=2905 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_5 Physical Address
0h	32	MAILBOX_REVISION	2905 0000h
10h	32	MAILBOX_SYSCONFIG	2905 0010h
40h	32	MAILBOX_MESSAGE_J	2905 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2905 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2905 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2905 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2905 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2905 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2905 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2905 000Ch + formula

14.4.6.2 MAILBOX_MAILBOX_CLUSTER_5 Registers

MAILBOX_MAILBOX_CLUSTER_5 Registers

14.4.6.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12251. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 0000h**

Figure 14-4046. MAILBOX_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6FCh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6FCh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">12h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-12253. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.6.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-12254. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 0010h**

Figure 14-4047. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-12256. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.6.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12257. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 0040h + formula**

Figure 14-4048. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-12259. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.6.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12260. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 0080h + formula**

Figure 14-4049. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-12262. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.6.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12263. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 00C0h + formula**

Figure 14-4050. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-12265. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.6.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-12266. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 0140h**

Figure 14-4051. MAILBOX_IRQ_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>EOI3</td><td>EOI2</td><td>EOI1</td><td>EOI0</td></tr>
<tr><td colspan="4">NONE</td><td>W</td><td>W</td><td>W</td><td>W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12268. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.6.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12269. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 0000h + formula**

Figure 14-4052. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-12271. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-12271. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-12271. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.6.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12272. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 0004h + formula**

Figure 14-4053. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12274. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-12274. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-12274. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.6.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12275. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 0008h + formula**

Figure 14-4054. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12277. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12277. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12277. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.6.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12278. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	**2905 000Ch + formula**

Figure 14-4055. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12280. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12280. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12280. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.7 MAILBOX_MAILBOX_CLUSTER_6

MAILBOX_MAILBOX_CLUSTER_6

14.4.7.1 MAILBOX_MAILBOX_CLUSTER_6 Summaries

MAILBOX_MAILBOX_CLUSTER_6 Summaries

Table 14-12281. MAILBOX Registers, Base Address=2906 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_6 Physical Address
0h	32	MAILBOX_REVISION	2906 0000h
10h	32	MAILBOX_SYSCONFIG	2906 0010h
40h	32	MAILBOX_MESSAGE_J	2906 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2906 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2906 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2906 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2906 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2906 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2906 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2906 000Ch + formula

14.4.7.2 MAILBOX_MAILBOX_CLUSTER_6 Registers

MAILBOX_MAILBOX_CLUSTER_6 Registers

14.4.7.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12282. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	**2906 0000h**

Figure 14-4056. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-12284. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.7.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-12285. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	**2906 0010h**

Figure 14-4057. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-12287. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.7.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12288. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0040h + formula

Figure 14-4058. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-12290. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.7.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12291. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	**2906 0080h + formula**

Figure 14-4059. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-12293. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.7.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12294. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	**2906 00C0h + formula**

Figure 14-4060. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-12296. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.7.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-12297. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0140h

Figure 14-4061. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-12299. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.7.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12300. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	**2906 0000h + formula**

Figure 14-4062. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-12302. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-12302. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-12302. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.7.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12303. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	**2906 0004h + formula**

Figure 14-4063. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12305. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-12305. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-12305. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.7.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12306. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	**2906 0008h + formula**

Figure 14-4064. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12308. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12308. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12308. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.7.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12309. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	**2906 000Ch + formula**

Figure 14-4065. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12311. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12311. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12311. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.8 *MAILBOX_MAILBOX_CLUSTER_7*

MAILBOX_MAILBOX_CLUSTER_7

14.4.8.1 MAILBOX_MAILBOX_CLUSTER_7 Summaries

MAILBOX_MAILBOX_CLUSTER_7 Summaries

Table 14-12312. MAILBOX Registers, Base Address=2907 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_7 Physical Address
0h	32	MAILBOX_REVISION	2907 0000h
10h	32	MAILBOX_SYSCONFIG	2907 0010h
40h	32	MAILBOX_MESSAGE_J	2907 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2907 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2907 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2907 0140h
0h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2907 0000h + formula
4h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2907 0004h + formula
8h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2907 0008h + formula
Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2907 000Ch + formula

14.4.8.2 MAILBOX_MAILBOX_CLUSTER_7 Registers

MAILBOX_MAILBOX_CLUSTER_7 Registers

14.4.8.2.1 MAILBOX_REVISION Register

1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12313. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 0000h**

Figure 14-4066. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-12315. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.8.2.2 MAILBOX_SYSCONFIG Register

1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Return to Summary Table

Table 14-12316. Instance Table

Instance Name	**Physical Address**
MAILBOX0_MAILBOX_CLUSTER_7	**2907 0010h**

Figure 14-4067. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-12318. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.8.2.3 MAILBOX_MESSAGE_j Register

1 MAILBOX_MESSAGE_j Register (Offset = 40h + formula) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12319. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 0040h + formula**

Figure 14-4068. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-12321. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.8.2.4 MAILBOX_FIFO_STATUS_j Register

1 MAILBOX_FIFO_STATUS_j Register (Offset = 80h + formula) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12322. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 0080h + formula**

Figure 14-4069. MAILBOX_FIFO_STATUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>FIFO_FULL</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12324. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.8.2.5 MAILBOX_MSG_STATUS_j Register

1 MAILBOX_MSG_STATUS_j Register (Offset = C0h + formula) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Offset = (j * 4h); where j = 0 to 15d

Table 14-12325. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 00C0h + formula**

Figure 14-4070. MAILBOX_MSG_STATUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_MESSAGES</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-12327. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.8.2.6 MAILBOX_IRQ_EOI Register

1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

Return to Summary Table

Table 14-12328. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 0140h**

Figure 14-4071. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-12330. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.8.2.7 MAILBOX_USER_IRQ_STATUS_RAW_j Register

1 MAILBOX_USER_IRQ_STATUS_RAW_j Register (Offset = 0h + formula) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12331. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 0000h + formula**

Figure 14-4072. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-12333. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n

Table 14-12333. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n

Table 14-12333. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.8.2.8 MAILBOX_USER_IRQ_STATUS_CLR_j Register

1 MAILBOX_USER_IRQ_STATUS_CLR_j Register (Offset = 4h + formula) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12334. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 0004h + formula**

Figure 14-4073. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12336. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n

Table 14-12336. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-12336. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.8.2.9 MAILBOX_USER_IRQ_ENABLE_SET_j Register

1 MAILBOX_USER_IRQ_ENABLE_SET_j Register (Offset = 8h + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12337. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 0008h + formula**

Figure 14-4074. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12339. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12339. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12339. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.8.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_j Register

1 MAILBOX_USER_IRQ_ENABLE_CLR_j Register (Offset = Ch + formula) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 3d

Table 14-12340. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	**2907 000Ch + formula**

Figure 14-4075. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12342. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12342. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-12342. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.9 SPINLOCK

SPINLOCK

14.4.9.1 SPINLOCK Summaries

SPINLOCK Summaries

Table 14-12343. SPINLOCK Registers, Base Address=2A00 0000h, Length=32768

Offset	Length	Register Name	SPINLOCK0 Physical Address
0h	32	SPINLOCK_REVISION	2A00 0000h
10h	32	SPINLOCK_SYSCONFIG	2A00 0010h
14h	32	SPINLOCK_SYSTATUS	2A00 0014h
800h	32	SPINLOCK_LOCK_REG_J	2A00 0800h + formula

14.4.9.2 SPINLOCK Registers

SPINLOCK Registers

14.4.9.2.1 SPINLOCK_REVISION Register

1 SPINLOCK_REVISION Register (Offset = 0h) [reset = 66FA6900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-12344. Instance Table

Instance Name	Physical Address
SPINLOCK0	**2A00 0000h**

Figure 14-4076. SPINLOCK_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FAh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FAh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
Dh					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-12346. SPINLOCK_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: core_srst_n
29:28	BU	R	2h	BU identifier Reset Source: core_srst_n
27:16	FUNCTION	R	6FAh	Module family. Reset Source: core_srst_n
15:11	RTL_VER	R	Dh	RTL version. R of X.Y.R.Z Reset Source: core_srst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: core_srst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: core_srst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: core_srst_n

14.4.9.2.2 SPINLOCK_SYSCONFIG Register

1 SPINLOCK_SYSCONFIG Register (Offset = 10h) [reset = 0h]

Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock

Return to Summary Table

Table 14-12347. Instance Table

Instance Name	Physical Address
SPINLOCK0	**2A00 0010h**

Figure 14-4077. SPINLOCK_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT_RESET	RESERVED
NONE						R/W	NONE
0h						0h	0h

Table 14-12349. SPINLOCK_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0 It has the same effect as the hardware reset Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks Reset Source: core_srst_n
0	RESERVED	NONE	0h	Reserved

14.4.9.2.3 SPINLOCK_SYSTATUS Register

1 SPINLOCK_SYSTATUS Register (Offset = 14h) [reset = 8000000h]

Provides information about the Spinlock module

Return to Summary Table

Table 14-12350. Instance Table

Instance Name	Physical Address
SPINLOCK0	**2A00 0014h**

Figure 14-4078. SPINLOCK_SYSTATUS Name Register

31	30	29	28	27	26	25	24
NUM_LOCKS							
R							
8h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IN_USE7	IN_USE6	IN_USE5	IN_USE4	IN_USE3	IN_USE2	IN_USE1	IN_USE0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12352. SPINLOCK_SYSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NUM_LOCKS	R	8h	Module configuration parameter n, the total number of spinlocks divided by 32. e.g. For 256 spin locks, this will return the number 0x08 Reset Source: core_srst_n
23:8	RESERVED	NONE	0h	Reserved
7	IN_USE7	R	0h	In-Use flag 7 covering lock registers 224 - 255. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 224 - 255 are in the Not Taken state Read 1 : At least one of the lock registers 224 - 255 are in the Taken state Reset Source: core_srst_n
6	IN_USE6	R	0h	In-Use flag 6 covering lock registers 192 - 223. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 192 - 223 are in the Not Taken state Read 1 : At least one of the lock registers 192 - 223 are in the Taken state Reset Source: core_srst_n

Table 14-12352. SPINLOCK_SYSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	IN_USE5	R	0h	In-Use flag 5 covering lock registers 160 - 191. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 160 - 191 are in the Not Taken state Read 1 : At least one of the lock registers 160 - 191 are in the Taken state Reset Source: core_srst_n
4	IN_USE4	R	0h	In-Use flag 4 covering lock registers 128 - 159. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 128 - 159 are in the Not Taken state Read 1 : At least one of the lock registers 128 - 159 are in the Taken state Reset Source: core_srst_n
3	IN_USE3	R	0h	In-Use flag 3 covering lock registers 96 - 127. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 96 - 127 are in the Not Taken state Read 1 : At least one of the lock registers 96 - 127 are in the Taken state Reset Source: core_srst_n
2	IN_USE2	R	0h	In-Use flag 2 covering lock registers 64 - 95. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 64 - 95 are in the Not Taken state Read 1 : At least one of the lock registers 64 - 95 are in the Taken state Reset Source: core_srst_n
1	IN_USE1	R	0h	In-Use flag 1 covering lock registers 32 - 63. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 32 - 63 are in the Not Taken state Read 1 : At least one of the lock registers 32 - 63 are in the Taken state Reset Source: core_srst_n
0	IN_USE0	R	0h	In-Use flag 0 covering lock registers 0 - 31. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 0 - 31 are in the Not Taken state Read 1 : At least one of the lock registers 0 - 31 are in the Taken state Reset Source: core_srst_n

14.4.9.2.4 SPINLOCK_LOCK_REG_j Register

1 SPINLOCK_LOCK_REG_j Register (Offset = 800h + formula) [reset = 0h]

The Lock[a] register is read and written to perform lock and unlock operations on lock 'a'

Return to Summary Table

Offset = (j * 4h); where j = 0 to 255d

Table 14-12353. Instance Table

Instance Name	Physical Address
SPINLOCK0	2A00 0800h + formula

Figure 14-4079. SPINLOCK_LOCK_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TAKEN
NONE							R/W
0h							0h

Table 14-12355. SPINLOCK_LOCK_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TAKEN	R/W	0h	Lock Status Read 0 : Lock was previously free. The reader now has been granted the lock. Read 1 : Lock was previously taken. The reader has not been granted the lock and must retry. Write 0 : Free the lock by setting TAKEN to zero. Write 1 : No effect Reset Source: core_srst_n

14.5 Memory Controller Registers

14.5.1 ddr16ss

ddr16ss

14.5.1.1 ddr16ss Summaries

ddr16ss Summaries

Table 14-12356. EMIF_SSCFG Registers, Base Address=0F30 0000h, Length=512

Offset	Length	Register Name	DDR16SS0 Physical Address
0h	32	EMIF_SSCFG_SS_ID_REV_REG	0F30 0000h
4h	32	EMIF_SSCFG_SS_CTL_REG	0F30 0004h
20h	32	EMIF_SSCFG_V2A_CTL_REG	0F30 0020h
24h	32	EMIF_SSCFG_V2A_R1_MAT_REG	0F30 0024h
28h	32	EMIF_SSCFG_V2A_R2_MAT_REG	0F30 0028h
2Ch	32	EMIF_SSCFG_V2A_R3_MAT_REG	0F30 002Ch
30h	32	EMIF_SSCFG_V2A_DEF_PRI_MAP_REG	0F30 0030h
34h	32	EMIF_SSCFG_V2A_R1_PRI_MAP_REG	0F30 0034h
38h	32	EMIF_SSCFG_V2A_R2_PRI_MAP_REG	0F30 0038h
3Ch	32	EMIF_SSCFG_V2A_R3_PRI_MAP_REG	0F30 003Ch
70h	32	EMIF_SSCFG_V2A_AERR_LOG1_REG	0F30 0070h
74h	32	EMIF_SSCFG_V2A_AERR_LOG2_REG	0F30 0074h
9Ch	32	EMIF_SSCFG_V2A_BUS_TO	0F30 009Ch
A0h	32	EMIF_SSCFG_V2A_INT_RAW_REG	0F30 00A0h
A4h	32	EMIF_SSCFG_V2A_INT_STAT_REG	0F30 00A4h
A8h	32	EMIF_SSCFG_V2A_INT_SET_REG	0F30 00A8h
ACh	32	EMIF_SSCFG_V2A_INT_CLR_REG	0F30 00ACh
B0h	32	EMIF_SSCFG_V2A_EOI_REG	0F30 00B0h
100h	32	EMIF_SSCFG_PERF_CNT_SEL_REG	0F30 0100h
104h	32	EMIF_SSCFG_PERF_CNT1_REG	0F30 0104h
108h	32	EMIF_SSCFG_PERF_CNT2_REG	0F30 0108h
10Ch	32	EMIF_SSCFG_PERF_CNT3_REG	0F30 010Ch
110h	32	EMIF_SSCFG_PERF_CNT4_REG	0F30 0110h
120h	32	EMIF_SSCFG_ECC_CTRL_REG	0F30 0120h
124h	32	EMIF_SSCFG_ECC_RID_INDX_REG	0F30 0124h
128h	32	EMIF_SSCFG_ECC_RID_VAL_REG	0F30 0128h
130h	32	EMIF_SSCFG_ECC_R0_STR_ADDR_REG	0F30 0130h
134h	32	EMIF_SSCFG_ECC_R0_END_ADDR_REG	0F30 0134h
138h	32	EMIF_SSCFG_ECC_R1_STR_ADDR_REG	0F30 0138h
13Ch	32	EMIF_SSCFG_ECC_R1_END_ADDR_REG	0F30 013Ch
140h	32	EMIF_SSCFG_ECC_R2_STR_ADDR_REG	0F30 0140h
144h	32	EMIF_SSCFG_ECC_R2_END_ADDR_REG	0F30 0144h
150h	32	EMIF_SSCFG_ECC_1B_ERR_CNT_REG	0F30 0150h
154h	32	EMIF_SSCFG_ECC_1B_ERR_THRSH_REG	0F30 0154h
158h	32	EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG	0F30 0158h
15Ch	32	EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG	0F30 015Ch
160h	32	EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG	0F30 0160h
164h	32	EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG	0F30 0164h

Table 14-12356. EMIF_SSCFG Registers, Base Address=0F30 0000h, Length=512 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
184h	32	EMIF_SSCFG_PHY_TEST_CTRL1_REG	0F30 0184h
188h	32	EMIF_SSCFG_PHY_TEST_CTRL2_REG	0F30 0188h
18Ch	32	EMIF_SSCFG_PHY_TEST_CTRL3_REG	0F30 018Ch
190h	32	EMIF_SSCFG_PHY_TEST_CTRL4_REG	0F30 0190h
194h	32	EMIF_SSCFG_PHY_TEST_CTRL5_REG	0F30 0194h
198h	32	EMIF_SSCFG_PHY_TEST_CTRL6_REG	0F30 0198h
19Ch	32	EMIF_SSCFG_PHY_TEST_CTRL7_REG	0F30 019Ch
1A0h	32	EMIF_SSCFG_PHY_TEST_CTRL8_REG	0F30 01A0h
1A4h	32	EMIF_SSCFG_PHY_TEST_CTRL9_REG	0F30 01A4h
1A8h	32	EMIF_SSCFG_PHY_TEST_CTRL10_REG	0F30 01A8h
1C0h	32	EMIF_SSCFG_PHY_TEST_STAT1_REG	0F30 01C0h
1C4h	32	EMIF_SSCFG_PHY_TEST_STAT2_REG	0F30 01C4h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768

Offset	Length	Register Name	DDR16SS0 Physical Address
0h	32	EMIF_CTLCFG_DENALI_CTL_0	0F30 8000h
4h	32	EMIF_CTLCFG_DENALI_CTL_1	0F30 8004h
8h	32	EMIF_CTLCFG_DENALI_CTL_2	0F30 8008h
Ch	32	EMIF_CTLCFG_DENALI_CTL_3	0F30 800Ch
10h	32	EMIF_CTLCFG_DENALI_CTL_4	0F30 8010h
14h	32	EMIF_CTLCFG_DENALI_CTL_5	0F30 8014h
18h	32	EMIF_CTLCFG_DENALI_CTL_6	0F30 8018h
1Ch	32	EMIF_CTLCFG_DENALI_CTL_7	0F30 801Ch
20h	32	EMIF_CTLCFG_DENALI_CTL_8	0F30 8020h
24h	32	EMIF_CTLCFG_DENALI_CTL_9	0F30 8024h
28h	32	EMIF_CTLCFG_DENALI_CTL_10	0F30 8028h
2Ch	32	EMIF_CTLCFG_DENALI_CTL_11	0F30 802Ch
30h	32	EMIF_CTLCFG_DENALI_CTL_12	0F30 8030h
34h	32	EMIF_CTLCFG_DENALI_CTL_13	0F30 8034h
38h	32	EMIF_CTLCFG_DENALI_CTL_14	0F30 8038h
3Ch	32	EMIF_CTLCFG_DENALI_CTL_15	0F30 803Ch
40h	32	EMIF_CTLCFG_DENALI_CTL_16	0F30 8040h
44h	32	EMIF_CTLCFG_DENALI_CTL_17	0F30 8044h
48h	32	EMIF_CTLCFG_DENALI_CTL_18	0F30 8048h
4Ch	32	EMIF_CTLCFG_DENALI_CTL_19	0F30 804Ch
50h	32	EMIF_CTLCFG_DENALI_CTL_20	0F30 8050h
54h	32	EMIF_CTLCFG_DENALI_CTL_21	0F30 8054h
58h	32	EMIF_CTLCFG_DENALI_CTL_22	0F30 8058h
5Ch	32	EMIF_CTLCFG_DENALI_CTL_23	0F30 805Ch
60h	32	EMIF_CTLCFG_DENALI_CTL_24	0F30 8060h
64h	32	EMIF_CTLCFG_DENALI_CTL_25	0F30 8064h
68h	32	EMIF_CTLCFG_DENALI_CTL_26	0F30 8068h
6Ch	32	EMIF_CTLCFG_DENALI_CTL_27	0F30 806Ch
70h	32	EMIF_CTLCFG_DENALI_CTL_28	0F30 8070h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
74h	32	EMIF_CTLCFG_DENALI_CTL_29	0F30 8074h
78h	32	EMIF_CTLCFG_DENALI_CTL_30	0F30 8078h
7Ch	32	EMIF_CTLCFG_DENALI_CTL_31	0F30 807Ch
80h	32	EMIF_CTLCFG_DENALI_CTL_32	0F30 8080h
84h	32	EMIF_CTLCFG_DENALI_CTL_33	0F30 8084h
88h	32	EMIF_CTLCFG_DENALI_CTL_34	0F30 8088h
8Ch	32	EMIF_CTLCFG_DENALI_CTL_35	0F30 808Ch
90h	32	EMIF_CTLCFG_DENALI_CTL_36	0F30 8090h
94h	32	EMIF_CTLCFG_DENALI_CTL_37	0F30 8094h
98h	32	EMIF_CTLCFG_DENALI_CTL_38	0F30 8098h
9Ch	32	EMIF_CTLCFG_DENALI_CTL_39	0F30 809Ch
A0h	32	EMIF_CTLCFG_DENALI_CTL_40	0F30 80A0h
A4h	32	EMIF_CTLCFG_DENALI_CTL_41	0F30 80A4h
A8h	32	EMIF_CTLCFG_DENALI_CTL_42	0F30 80A8h
ACh	32	EMIF_CTLCFG_DENALI_CTL_43	0F30 80ACh
B0h	32	EMIF_CTLCFG_DENALI_CTL_44	0F30 80B0h
B4h	32	EMIF_CTLCFG_DENALI_CTL_45	0F30 80B4h
B8h	32	EMIF_CTLCFG_DENALI_CTL_46	0F30 80B8h
BCh	32	EMIF_CTLCFG_DENALI_CTL_47	0F30 80BCh
C0h	32	EMIF_CTLCFG_DENALI_CTL_48	0F30 80C0h
C4h	32	EMIF_CTLCFG_DENALI_CTL_49	0F30 80C4h
C8h	32	EMIF_CTLCFG_DENALI_CTL_50	0F30 80C8h
CCh	32	EMIF_CTLCFG_DENALI_CTL_51	0F30 80CCh
D0h	32	EMIF_CTLCFG_DENALI_CTL_52	0F30 80D0h
D4h	32	EMIF_CTLCFG_DENALI_CTL_53	0F30 80D4h
D8h	32	EMIF_CTLCFG_DENALI_CTL_54	0F30 80D8h
DCh	32	EMIF_CTLCFG_DENALI_CTL_55	0F30 80DCh
E0h	32	EMIF_CTLCFG_DENALI_CTL_56	0F30 80E0h
E4h	32	EMIF_CTLCFG_DENALI_CTL_57	0F30 80E4h
E8h	32	EMIF_CTLCFG_DENALI_CTL_58	0F30 80E8h
ECh	32	EMIF_CTLCFG_DENALI_CTL_59	0F30 80ECh
F0h	32	EMIF_CTLCFG_DENALI_CTL_60	0F30 80F0h
F4h	32	EMIF_CTLCFG_DENALI_CTL_61	0F30 80F4h
F8h	32	EMIF_CTLCFG_DENALI_CTL_62	0F30 80F8h
FCh	32	EMIF_CTLCFG_DENALI_CTL_63	0F30 80FCh
100h	32	EMIF_CTLCFG_DENALI_CTL_64	0F30 8100h
104h	32	EMIF_CTLCFG_DENALI_CTL_65	0F30 8104h
108h	32	EMIF_CTLCFG_DENALI_CTL_66	0F30 8108h
10Ch	32	EMIF_CTLCFG_DENALI_CTL_67	0F30 810Ch
110h	32	EMIF_CTLCFG_DENALI_CTL_68	0F30 8110h
114h	32	EMIF_CTLCFG_DENALI_CTL_69	0F30 8114h
118h	32	EMIF_CTLCFG_DENALI_CTL_70	0F30 8118h
11Ch	32	EMIF_CTLCFG_DENALI_CTL_71	0F30 811Ch
120h	32	EMIF_CTLCFG_DENALI_CTL_72	0F30 8120h
124h	32	EMIF_CTLCFG_DENALI_CTL_73	0F30 8124h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
128h	32	EMIF_CTLCFG_DENALI_CTL_74	0F30 8128h
12Ch	32	EMIF_CTLCFG_DENALI_CTL_75	0F30 812Ch
130h	32	EMIF_CTLCFG_DENALI_CTL_76	0F30 8130h
134h	32	EMIF_CTLCFG_DENALI_CTL_77	0F30 8134h
138h	32	EMIF_CTLCFG_DENALI_CTL_78	0F30 8138h
13Ch	32	EMIF_CTLCFG_DENALI_CTL_79	0F30 813Ch
140h	32	EMIF_CTLCFG_DENALI_CTL_80	0F30 8140h
144h	32	EMIF_CTLCFG_DENALI_CTL_81	0F30 8144h
148h	32	EMIF_CTLCFG_DENALI_CTL_82	0F30 8148h
14Ch	32	EMIF_CTLCFG_DENALI_CTL_83	0F30 814Ch
150h	32	EMIF_CTLCFG_DENALI_CTL_84	0F30 8150h
154h	32	EMIF_CTLCFG_DENALI_CTL_85	0F30 8154h
158h	32	EMIF_CTLCFG_DENALI_CTL_86	0F30 8158h
15Ch	32	EMIF_CTLCFG_DENALI_CTL_87	0F30 815Ch
160h	32	EMIF_CTLCFG_DENALI_CTL_88	0F30 8160h
164h	32	EMIF_CTLCFG_DENALI_CTL_89	0F30 8164h
168h	32	EMIF_CTLCFG_DENALI_CTL_90	0F30 8168h
16Ch	32	EMIF_CTLCFG_DENALI_CTL_91	0F30 816Ch
170h	32	EMIF_CTLCFG_DENALI_CTL_92	0F30 8170h
174h	32	EMIF_CTLCFG_DENALI_CTL_93	0F30 8174h
178h	32	EMIF_CTLCFG_DENALI_CTL_94	0F30 8178h
17Ch	32	EMIF_CTLCFG_DENALI_CTL_95	0F30 817Ch
180h	32	EMIF_CTLCFG_DENALI_CTL_96	0F30 8180h
184h	32	EMIF_CTLCFG_DENALI_CTL_97	0F30 8184h
188h	32	EMIF_CTLCFG_DENALI_CTL_98	0F30 8188h
18Ch	32	EMIF_CTLCFG_DENALI_CTL_99	0F30 818Ch
190h	32	EMIF_CTLCFG_DENALI_CTL_100	0F30 8190h
194h	32	EMIF_CTLCFG_DENALI_CTL_101	0F30 8194h
198h	32	EMIF_CTLCFG_DENALI_CTL_102	0F30 8198h
19Ch	32	EMIF_CTLCFG_DENALI_CTL_103	0F30 819Ch
1A0h	32	EMIF_CTLCFG_DENALI_CTL_104	0F30 81A0h
1A4h	32	EMIF_CTLCFG_DENALI_CTL_105	0F30 81A4h
1A8h	32	EMIF_CTLCFG_DENALI_CTL_106	0F30 81A8h
1ACh	32	EMIF_CTLCFG_DENALI_CTL_107	0F30 81ACh
1B0h	32	EMIF_CTLCFG_DENALI_CTL_108	0F30 81B0h
1B4h	32	EMIF_CTLCFG_DENALI_CTL_109	0F30 81B4h
1B8h	32	EMIF_CTLCFG_DENALI_CTL_110	0F30 81B8h
1BCh	32	EMIF_CTLCFG_DENALI_CTL_111	0F30 81BCh
1C0h	32	EMIF_CTLCFG_DENALI_CTL_112	0F30 81C0h
1C4h	32	EMIF_CTLCFG_DENALI_CTL_113	0F30 81C4h
1C8h	32	EMIF_CTLCFG_DENALI_CTL_114	0F30 81C8h
1CCh	32	EMIF_CTLCFG_DENALI_CTL_115	0F30 81CCh
1D0h	32	EMIF_CTLCFG_DENALI_CTL_116	0F30 81D0h
1D4h	32	EMIF_CTLCFG_DENALI_CTL_117	0F30 81D4h
1D8h	32	EMIF_CTLCFG_DENALI_CTL_118	0F30 81D8h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
1DCh	32	EMIF_CTLCFG_DENALI_CTL_119	0F30 81DCh
1E0h	32	EMIF_CTLCFG_DENALI_CTL_120	0F30 81E0h
1E4h	32	EMIF_CTLCFG_DENALI_CTL_121	0F30 81E4h
1E8h	32	EMIF_CTLCFG_DENALI_CTL_122	0F30 81E8h
1ECh	32	EMIF_CTLCFG_DENALI_CTL_123	0F30 81ECh
1F0h	32	EMIF_CTLCFG_DENALI_CTL_124	0F30 81F0h
1F4h	32	EMIF_CTLCFG_DENALI_CTL_125	0F30 81F4h
1F8h	32	EMIF_CTLCFG_DENALI_CTL_126	0F30 81F8h
1FCh	32	EMIF_CTLCFG_DENALI_CTL_127	0F30 81FCh
200h	32	EMIF_CTLCFG_DENALI_CTL_128	0F30 8200h
204h	32	EMIF_CTLCFG_DENALI_CTL_129	0F30 8204h
208h	32	EMIF_CTLCFG_DENALI_CTL_130	0F30 8208h
20Ch	32	EMIF_CTLCFG_DENALI_CTL_131	0F30 820Ch
210h	32	EMIF_CTLCFG_DENALI_CTL_132	0F30 8210h
214h	32	EMIF_CTLCFG_DENALI_CTL_133	0F30 8214h
218h	32	EMIF_CTLCFG_DENALI_CTL_134	0F30 8218h
21Ch	32	EMIF_CTLCFG_DENALI_CTL_135	0F30 821Ch
220h	32	EMIF_CTLCFG_DENALI_CTL_136	0F30 8220h
224h	32	EMIF_CTLCFG_DENALI_CTL_137	0F30 8224h
228h	32	EMIF_CTLCFG_DENALI_CTL_138	0F30 8228h
22Ch	32	EMIF_CTLCFG_DENALI_CTL_139	0F30 822Ch
230h	32	EMIF_CTLCFG_DENALI_CTL_140	0F30 8230h
234h	32	EMIF_CTLCFG_DENALI_CTL_141	0F30 8234h
238h	32	EMIF_CTLCFG_DENALI_CTL_142	0F30 8238h
23Ch	32	EMIF_CTLCFG_DENALI_CTL_143	0F30 823Ch
240h	32	EMIF_CTLCFG_DENALI_CTL_144	0F30 8240h
244h	32	EMIF_CTLCFG_DENALI_CTL_145	0F30 8244h
248h	32	EMIF_CTLCFG_DENALI_CTL_146	0F30 8248h
24Ch	32	EMIF_CTLCFG_DENALI_CTL_147	0F30 824Ch
250h	32	EMIF_CTLCFG_DENALI_CTL_148	0F30 8250h
254h	32	EMIF_CTLCFG_DENALI_CTL_149	0F30 8254h
258h	32	EMIF_CTLCFG_DENALI_CTL_150	0F30 8258h
25Ch	32	EMIF_CTLCFG_DENALI_CTL_151	0F30 825Ch
260h	32	EMIF_CTLCFG_DENALI_CTL_152	0F30 8260h
264h	32	EMIF_CTLCFG_DENALI_CTL_153	0F30 8264h
268h	32	EMIF_CTLCFG_DENALI_CTL_154	0F30 8268h
26Ch	32	EMIF_CTLCFG_DENALI_CTL_155	0F30 826Ch
270h	32	EMIF_CTLCFG_DENALI_CTL_156	0F30 8270h
274h	32	EMIF_CTLCFG_DENALI_CTL_157	0F30 8274h
278h	32	EMIF_CTLCFG_DENALI_CTL_158	0F30 8278h
27Ch	32	EMIF_CTLCFG_DENALI_CTL_159	0F30 827Ch
280h	32	EMIF_CTLCFG_DENALI_CTL_160	0F30 8280h
284h	32	EMIF_CTLCFG_DENALI_CTL_161	0F30 8284h
288h	32	EMIF_CTLCFG_DENALI_CTL_162	0F30 8288h
28Ch	32	EMIF_CTLCFG_DENALI_CTL_163	0F30 828Ch

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
290h	32	EMIF_CTLCFG_DENALI_CTL_164	0F30 8290h
294h	32	EMIF_CTLCFG_DENALI_CTL_165	0F30 8294h
298h	32	EMIF_CTLCFG_DENALI_CTL_166	0F30 8298h
29Ch	32	EMIF_CTLCFG_DENALI_CTL_167	0F30 829Ch
2A0h	32	EMIF_CTLCFG_DENALI_CTL_168	0F30 82A0h
2A4h	32	EMIF_CTLCFG_DENALI_CTL_169	0F30 82A4h
2A8h	32	EMIF_CTLCFG_DENALI_CTL_170	0F30 82A8h
2ACh	32	EMIF_CTLCFG_DENALI_CTL_171	0F30 82ACh
2B0h	32	EMIF_CTLCFG_DENALI_CTL_172	0F30 82B0h
2B4h	32	EMIF_CTLCFG_DENALI_CTL_173	0F30 82B4h
2B8h	32	EMIF_CTLCFG_DENALI_CTL_174	0F30 82B8h
2BCh	32	EMIF_CTLCFG_DENALI_CTL_175	0F30 82BCh
2C0h	32	EMIF_CTLCFG_DENALI_CTL_176	0F30 82C0h
2C4h	32	EMIF_CTLCFG_DENALI_CTL_177	0F30 82C4h
2C8h	32	EMIF_CTLCFG_DENALI_CTL_178	0F30 82C8h
2CCh	32	EMIF_CTLCFG_DENALI_CTL_179	0F30 82CCh
2D0h	32	EMIF_CTLCFG_DENALI_CTL_180	0F30 82D0h
2D4h	32	EMIF_CTLCFG_DENALI_CTL_181	0F30 82D4h
2D8h	32	EMIF_CTLCFG_DENALI_CTL_182	0F30 82D8h
2DCh	32	EMIF_CTLCFG_DENALI_CTL_183	0F30 82DCh
2E0h	32	EMIF_CTLCFG_DENALI_CTL_184	0F30 82E0h
2E4h	32	EMIF_CTLCFG_DENALI_CTL_185	0F30 82E4h
2E8h	32	EMIF_CTLCFG_DENALI_CTL_186	0F30 82E8h
2ECh	32	EMIF_CTLCFG_DENALI_CTL_187	0F30 82ECh
2F0h	32	EMIF_CTLCFG_DENALI_CTL_188	0F30 82F0h
2F4h	32	EMIF_CTLCFG_DENALI_CTL_189	0F30 82F4h
2F8h	32	EMIF_CTLCFG_DENALI_CTL_190	0F30 82F8h
2FCh	32	EMIF_CTLCFG_DENALI_CTL_191	0F30 82FCh
300h	32	EMIF_CTLCFG_DENALI_CTL_192	0F30 8300h
304h	32	EMIF_CTLCFG_DENALI_CTL_193	0F30 8304h
308h	32	EMIF_CTLCFG_DENALI_CTL_194	0F30 8308h
30Ch	32	EMIF_CTLCFG_DENALI_CTL_195	0F30 830Ch
310h	32	EMIF_CTLCFG_DENALI_CTL_196	0F30 8310h
314h	32	EMIF_CTLCFG_DENALI_CTL_197	0F30 8314h
318h	32	EMIF_CTLCFG_DENALI_CTL_198	0F30 8318h
31Ch	32	EMIF_CTLCFG_DENALI_CTL_199	0F30 831Ch
320h	32	EMIF_CTLCFG_DENALI_CTL_200	0F30 8320h
324h	32	EMIF_CTLCFG_DENALI_CTL_201	0F30 8324h
328h	32	EMIF_CTLCFG_DENALI_CTL_202	0F30 8328h
32Ch	32	EMIF_CTLCFG_DENALI_CTL_203	0F30 832Ch
330h	32	EMIF_CTLCFG_DENALI_CTL_204	0F30 8330h
334h	32	EMIF_CTLCFG_DENALI_CTL_205	0F30 8334h
338h	32	EMIF_CTLCFG_DENALI_CTL_206	0F30 8338h
33Ch	32	EMIF_CTLCFG_DENALI_CTL_207	0F30 833Ch
340h	32	EMIF_CTLCFG_DENALI_CTL_208	0F30 8340h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
344h	32	EMIF_CTLCFG_DENALI_CTL_209	0F30 8344h
348h	32	EMIF_CTLCFG_DENALI_CTL_210	0F30 8348h
34Ch	32	EMIF_CTLCFG_DENALI_CTL_211	0F30 834Ch
350h	32	EMIF_CTLCFG_DENALI_CTL_212	0F30 8350h
354h	32	EMIF_CTLCFG_DENALI_CTL_213	0F30 8354h
358h	32	EMIF_CTLCFG_DENALI_CTL_214	0F30 8358h
35Ch	32	EMIF_CTLCFG_DENALI_CTL_215	0F30 835Ch
360h	32	EMIF_CTLCFG_DENALI_CTL_216	0F30 8360h
364h	32	EMIF_CTLCFG_DENALI_CTL_217	0F30 8364h
368h	32	EMIF_CTLCFG_DENALI_CTL_218	0F30 8368h
36Ch	32	EMIF_CTLCFG_DENALI_CTL_219	0F30 836Ch
370h	32	EMIF_CTLCFG_DENALI_CTL_220	0F30 8370h
374h	32	EMIF_CTLCFG_DENALI_CTL_221	0F30 8374h
378h	32	EMIF_CTLCFG_DENALI_CTL_222	0F30 8378h
37Ch	32	EMIF_CTLCFG_DENALI_CTL_223	0F30 837Ch
380h	32	EMIF_CTLCFG_DENALI_CTL_224	0F30 8380h
384h	32	EMIF_CTLCFG_DENALI_CTL_225	0F30 8384h
388h	32	EMIF_CTLCFG_DENALI_CTL_226	0F30 8388h
38Ch	32	EMIF_CTLCFG_DENALI_CTL_227	0F30 838Ch
390h	32	EMIF_CTLCFG_DENALI_CTL_228	0F30 8390h
394h	32	EMIF_CTLCFG_DENALI_CTL_229	0F30 8394h
398h	32	EMIF_CTLCFG_DENALI_CTL_230	0F30 8398h
39Ch	32	EMIF_CTLCFG_DENALI_CTL_231	0F30 839Ch
3A0h	32	EMIF_CTLCFG_DENALI_CTL_232	0F30 83A0h
3A4h	32	EMIF_CTLCFG_DENALI_CTL_233	0F30 83A4h
3A8h	32	EMIF_CTLCFG_DENALI_CTL_234	0F30 83A8h
3ACh	32	EMIF_CTLCFG_DENALI_CTL_235	0F30 83ACh
3B0h	32	EMIF_CTLCFG_DENALI_CTL_236	0F30 83B0h
3B4h	32	EMIF_CTLCFG_DENALI_CTL_237	0F30 83B4h
3B8h	32	EMIF_CTLCFG_DENALI_CTL_238	0F30 83B8h
3BCh	32	EMIF_CTLCFG_DENALI_CTL_239	0F30 83BCh
3C0h	32	EMIF_CTLCFG_DENALI_CTL_240	0F30 83C0h
3C4h	32	EMIF_CTLCFG_DENALI_CTL_241	0F30 83C4h
3C8h	32	EMIF_CTLCFG_DENALI_CTL_242	0F30 83C8h
3CCh	32	EMIF_CTLCFG_DENALI_CTL_243	0F30 83CCh
3D0h	32	EMIF_CTLCFG_DENALI_CTL_244	0F30 83D0h
3D4h	32	EMIF_CTLCFG_DENALI_CTL_245	0F30 83D4h
3D8h	32	EMIF_CTLCFG_DENALI_CTL_246	0F30 83D8h
3DCh	32	EMIF_CTLCFG_DENALI_CTL_247	0F30 83DCh
3E0h	32	EMIF_CTLCFG_DENALI_CTL_248	0F30 83E0h
3E4h	32	EMIF_CTLCFG_DENALI_CTL_249	0F30 83E4h
3E8h	32	EMIF_CTLCFG_DENALI_CTL_250	0F30 83E8h
3ECh	32	EMIF_CTLCFG_DENALI_CTL_251	0F30 83ECh
3F0h	32	EMIF_CTLCFG_DENALI_CTL_252	0F30 83F0h
3F4h	32	EMIF_CTLCFG_DENALI_CTL_253	0F30 83F4h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
3F8h	32	EMIF_CTLCFG_DENALI_CTL_254	0F30 83F8h
3FCh	32	EMIF_CTLCFG_DENALI_CTL_255	0F30 83FCh
400h	32	EMIF_CTLCFG_DENALI_CTL_256	0F30 8400h
404h	32	EMIF_CTLCFG_DENALI_CTL_257	0F30 8404h
408h	32	EMIF_CTLCFG_DENALI_CTL_258	0F30 8408h
40Ch	32	EMIF_CTLCFG_DENALI_CTL_259	0F30 840Ch
410h	32	EMIF_CTLCFG_DENALI_CTL_260	0F30 8410h
414h	32	EMIF_CTLCFG_DENALI_CTL_261	0F30 8414h
418h	32	EMIF_CTLCFG_DENALI_CTL_262	0F30 8418h
41Ch	32	EMIF_CTLCFG_DENALI_CTL_263	0F30 841Ch
420h	32	EMIF_CTLCFG_DENALI_CTL_264	0F30 8420h
424h	32	EMIF_CTLCFG_DENALI_CTL_265	0F30 8424h
428h	32	EMIF_CTLCFG_DENALI_CTL_266	0F30 8428h
42Ch	32	EMIF_CTLCFG_DENALI_CTL_267	0F30 842Ch
430h	32	EMIF_CTLCFG_DENALI_CTL_268	0F30 8430h
434h	32	EMIF_CTLCFG_DENALI_CTL_269	0F30 8434h
438h	32	EMIF_CTLCFG_DENALI_CTL_270	0F30 8438h
43Ch	32	EMIF_CTLCFG_DENALI_CTL_271	0F30 843Ch
440h	32	EMIF_CTLCFG_DENALI_CTL_272	0F30 8440h
444h	32	EMIF_CTLCFG_DENALI_CTL_273	0F30 8444h
448h	32	EMIF_CTLCFG_DENALI_CTL_274	0F30 8448h
44Ch	32	EMIF_CTLCFG_DENALI_CTL_275	0F30 844Ch
450h	32	EMIF_CTLCFG_DENALI_CTL_276	0F30 8450h
454h	32	EMIF_CTLCFG_DENALI_CTL_277	0F30 8454h
458h	32	EMIF_CTLCFG_DENALI_CTL_278	0F30 8458h
45Ch	32	EMIF_CTLCFG_DENALI_CTL_279	0F30 845Ch
460h	32	EMIF_CTLCFG_DENALI_CTL_280	0F30 8460h
464h	32	EMIF_CTLCFG_DENALI_CTL_281	0F30 8464h
468h	32	EMIF_CTLCFG_DENALI_CTL_282	0F30 8468h
46Ch	32	EMIF_CTLCFG_DENALI_CTL_283	0F30 846Ch
470h	32	EMIF_CTLCFG_DENALI_CTL_284	0F30 8470h
474h	32	EMIF_CTLCFG_DENALI_CTL_285	0F30 8474h
478h	32	EMIF_CTLCFG_DENALI_CTL_286	0F30 8478h
47Ch	32	EMIF_CTLCFG_DENALI_CTL_287	0F30 847Ch
480h	32	EMIF_CTLCFG_DENALI_CTL_288	0F30 8480h
484h	32	EMIF_CTLCFG_DENALI_CTL_289	0F30 8484h
488h	32	EMIF_CTLCFG_DENALI_CTL_290	0F30 8488h
48Ch	32	EMIF_CTLCFG_DENALI_CTL_291	0F30 848Ch
490h	32	EMIF_CTLCFG_DENALI_CTL_292	0F30 8490h
494h	32	EMIF_CTLCFG_DENALI_CTL_293	0F30 8494h
498h	32	EMIF_CTLCFG_DENALI_CTL_294	0F30 8498h
49Ch	32	EMIF_CTLCFG_DENALI_CTL_295	0F30 849Ch
4A0h	32	EMIF_CTLCFG_DENALI_CTL_296	0F30 84A0h
4A4h	32	EMIF_CTLCFG_DENALI_CTL_297	0F30 84A4h
4A8h	32	EMIF_CTLCFG_DENALI_CTL_298	0F30 84A8h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
4ACh	32	EMIF_CTLCFG_DENALI_CTL_299	0F30 84ACh
4B0h	32	EMIF_CTLCFG_DENALI_CTL_300	0F30 84B0h
4B4h	32	EMIF_CTLCFG_DENALI_CTL_301	0F30 84B4h
4B8h	32	EMIF_CTLCFG_DENALI_CTL_302	0F30 84B8h
4BCh	32	EMIF_CTLCFG_DENALI_CTL_303	0F30 84BCh
4C0h	32	EMIF_CTLCFG_DENALI_CTL_304	0F30 84C0h
4C4h	32	EMIF_CTLCFG_DENALI_CTL_305	0F30 84C4h
4C8h	32	EMIF_CTLCFG_DENALI_CTL_306	0F30 84C8h
4CCh	32	EMIF_CTLCFG_DENALI_CTL_307	0F30 84CCh
4D0h	32	EMIF_CTLCFG_DENALI_CTL_308	0F30 84D0h
4D4h	32	EMIF_CTLCFG_DENALI_CTL_309	0F30 84D4h
4D8h	32	EMIF_CTLCFG_DENALI_CTL_310	0F30 84D8h
4DCh	32	EMIF_CTLCFG_DENALI_CTL_311	0F30 84DCh
4E0h	32	EMIF_CTLCFG_DENALI_CTL_312	0F30 84E0h
4E4h	32	EMIF_CTLCFG_DENALI_CTL_313	0F30 84E4h
4E8h	32	EMIF_CTLCFG_DENALI_CTL_314	0F30 84E8h
4ECh	32	EMIF_CTLCFG_DENALI_CTL_315	0F30 84ECh
4F0h	32	EMIF_CTLCFG_DENALI_CTL_316	0F30 84F0h
4F4h	32	EMIF_CTLCFG_DENALI_CTL_317	0F30 84F4h
4F8h	32	EMIF_CTLCFG_DENALI_CTL_318	0F30 84F8h
4FCh	32	EMIF_CTLCFG_DENALI_CTL_319	0F30 84FCh
500h	32	EMIF_CTLCFG_DENALI_CTL_320	0F30 8500h
504h	32	EMIF_CTLCFG_DENALI_CTL_321	0F30 8504h
508h	32	EMIF_CTLCFG_DENALI_CTL_322	0F30 8508h
50Ch	32	EMIF_CTLCFG_DENALI_CTL_323	0F30 850Ch
510h	32	EMIF_CTLCFG_DENALI_CTL_324	0F30 8510h
514h	32	EMIF_CTLCFG_DENALI_CTL_325	0F30 8514h
518h	32	EMIF_CTLCFG_DENALI_CTL_326	0F30 8518h
51Ch	32	EMIF_CTLCFG_DENALI_CTL_327	0F30 851Ch
520h	32	EMIF_CTLCFG_DENALI_CTL_328	0F30 8520h
524h	32	EMIF_CTLCFG_DENALI_CTL_329	0F30 8524h
528h	32	EMIF_CTLCFG_DENALI_CTL_330	0F30 8528h
52Ch	32	EMIF_CTLCFG_DENALI_CTL_331	0F30 852Ch
530h	32	EMIF_CTLCFG_DENALI_CTL_332	0F30 8530h
534h	32	EMIF_CTLCFG_DENALI_CTL_333	0F30 8534h
538h	32	EMIF_CTLCFG_DENALI_CTL_334	0F30 8538h
53Ch	32	EMIF_CTLCFG_DENALI_CTL_335	0F30 853Ch
540h	32	EMIF_CTLCFG_DENALI_CTL_336	0F30 8540h
544h	32	EMIF_CTLCFG_DENALI_CTL_337	0F30 8544h
548h	32	EMIF_CTLCFG_DENALI_CTL_338	0F30 8548h
54Ch	32	EMIF_CTLCFG_DENALI_CTL_339	0F30 854Ch
550h	32	EMIF_CTLCFG_DENALI_CTL_340	0F30 8550h
554h	32	EMIF_CTLCFG_DENALI_CTL_341	0F30 8554h
558h	32	EMIF_CTLCFG_DENALI_CTL_342	0F30 8558h
55Ch	32	EMIF_CTLCFG_DENALI_CTL_343	0F30 855Ch

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
560h	32	EMIF_CTLCFG_DENALI_CTL_344	0F30 8560h
564h	32	EMIF_CTLCFG_DENALI_CTL_345	0F30 8564h
568h	32	EMIF_CTLCFG_DENALI_CTL_346	0F30 8568h
56Ch	32	EMIF_CTLCFG_DENALI_CTL_347	0F30 856Ch
570h	32	EMIF_CTLCFG_DENALI_CTL_348	0F30 8570h
574h	32	EMIF_CTLCFG_DENALI_CTL_349	0F30 8574h
578h	32	EMIF_CTLCFG_DENALI_CTL_350	0F30 8578h
57Ch	32	EMIF_CTLCFG_DENALI_CTL_351	0F30 857Ch
580h	32	EMIF_CTLCFG_DENALI_CTL_352	0F30 8580h
584h	32	EMIF_CTLCFG_DENALI_CTL_353	0F30 8584h
588h	32	EMIF_CTLCFG_DENALI_CTL_354	0F30 8588h
58Ch	32	EMIF_CTLCFG_DENALI_CTL_355	0F30 858Ch
590h	32	EMIF_CTLCFG_DENALI_CTL_356	0F30 8590h
594h	32	EMIF_CTLCFG_DENALI_CTL_357	0F30 8594h
598h	32	EMIF_CTLCFG_DENALI_CTL_358	0F30 8598h
59Ch	32	EMIF_CTLCFG_DENALI_CTL_359	0F30 859Ch
5A0h	32	EMIF_CTLCFG_DENALI_CTL_360	0F30 85A0h
5A4h	32	EMIF_CTLCFG_DENALI_CTL_361	0F30 85A4h
5A8h	32	EMIF_CTLCFG_DENALI_CTL_362	0F30 85A8h
5ACh	32	EMIF_CTLCFG_DENALI_CTL_363	0F30 85ACh
5B0h	32	EMIF_CTLCFG_DENALI_CTL_364	0F30 85B0h
5B4h	32	EMIF_CTLCFG_DENALI_CTL_365	0F30 85B4h
5B8h	32	EMIF_CTLCFG_DENALI_CTL_366	0F30 85B8h
5BCh	32	EMIF_CTLCFG_DENALI_CTL_367	0F30 85BCh
5C0h	32	EMIF_CTLCFG_DENALI_CTL_368	0F30 85C0h
5C4h	32	EMIF_CTLCFG_DENALI_CTL_369	0F30 85C4h
5C8h	32	EMIF_CTLCFG_DENALI_CTL_370	0F30 85C8h
5CCh	32	EMIF_CTLCFG_DENALI_CTL_371	0F30 85CCh
5D0h	32	EMIF_CTLCFG_DENALI_CTL_372	0F30 85D0h
5D4h	32	EMIF_CTLCFG_DENALI_CTL_373	0F30 85D4h
5D8h	32	EMIF_CTLCFG_DENALI_CTL_374	0F30 85D8h
5DCh	32	EMIF_CTLCFG_DENALI_CTL_375	0F30 85DCh
5E0h	32	EMIF_CTLCFG_DENALI_CTL_376	0F30 85E0h
5E4h	32	EMIF_CTLCFG_DENALI_CTL_377	0F30 85E4h
5E8h	32	EMIF_CTLCFG_DENALI_CTL_378	0F30 85E8h
5ECh	32	EMIF_CTLCFG_DENALI_CTL_379	0F30 85ECh
5F0h	32	EMIF_CTLCFG_DENALI_CTL_380	0F30 85F0h
5F4h	32	EMIF_CTLCFG_DENALI_CTL_381	0F30 85F4h
5F8h	32	EMIF_CTLCFG_DENALI_CTL_382	0F30 85F8h
5FCh	32	EMIF_CTLCFG_DENALI_CTL_383	0F30 85FCh
600h	32	EMIF_CTLCFG_DENALI_CTL_384	0F30 8600h
604h	32	EMIF_CTLCFG_DENALI_CTL_385	0F30 8604h
608h	32	EMIF_CTLCFG_DENALI_CTL_386	0F30 8608h
60Ch	32	EMIF_CTLCFG_DENALI_CTL_387	0F30 860Ch
610h	32	EMIF_CTLCFG_DENALI_CTL_388	0F30 8610h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
614h	32	EMIF_CTLCFG_DENALI_CTL_389	0F30 8614h
618h	32	EMIF_CTLCFG_DENALI_CTL_390	0F30 8618h
61Ch	32	EMIF_CTLCFG_DENALI_CTL_391	0F30 861Ch
620h	32	EMIF_CTLCFG_DENALI_CTL_392	0F30 8620h
624h	32	EMIF_CTLCFG_DENALI_CTL_393	0F30 8624h
628h	32	EMIF_CTLCFG_DENALI_CTL_394	0F30 8628h
62Ch	32	EMIF_CTLCFG_DENALI_CTL_395	0F30 862Ch
630h	32	EMIF_CTLCFG_DENALI_CTL_396	0F30 8630h
634h	32	EMIF_CTLCFG_DENALI_CTL_397	0F30 8634h
638h	32	EMIF_CTLCFG_DENALI_CTL_398	0F30 8638h
63Ch	32	EMIF_CTLCFG_DENALI_CTL_399	0F30 863Ch
640h	32	EMIF_CTLCFG_DENALI_CTL_400	0F30 8640h
644h	32	EMIF_CTLCFG_DENALI_CTL_401	0F30 8644h
648h	32	EMIF_CTLCFG_DENALI_CTL_402	0F30 8648h
64Ch	32	EMIF_CTLCFG_DENALI_CTL_403	0F30 864Ch
650h	32	EMIF_CTLCFG_DENALI_CTL_404	0F30 8650h
654h	32	EMIF_CTLCFG_DENALI_CTL_405	0F30 8654h
658h	32	EMIF_CTLCFG_DENALI_CTL_406	0F30 8658h
65Ch	32	EMIF_CTLCFG_DENALI_CTL_407	0F30 865Ch
660h	32	EMIF_CTLCFG_DENALI_CTL_408	0F30 8660h
664h	32	EMIF_CTLCFG_DENALI_CTL_409	0F30 8664h
668h	32	EMIF_CTLCFG_DENALI_CTL_410	0F30 8668h
66Ch	32	EMIF_CTLCFG_DENALI_CTL_411	0F30 866Ch
670h	32	EMIF_CTLCFG_DENALI_CTL_412	0F30 8670h
674h	32	EMIF_CTLCFG_DENALI_CTL_413	0F30 8674h
678h	32	EMIF_CTLCFG_DENALI_CTL_414	0F30 8678h
67Ch	32	EMIF_CTLCFG_DENALI_CTL_415	0F30 867Ch
680h	32	EMIF_CTLCFG_DENALI_CTL_416	0F30 8680h
684h	32	EMIF_CTLCFG_DENALI_CTL_417	0F30 8684h
688h	32	EMIF_CTLCFG_DENALI_CTL_418	0F30 8688h
68Ch	32	EMIF_CTLCFG_DENALI_CTL_419	0F30 868Ch
690h	32	EMIF_CTLCFG_DENALI_CTL_420	0F30 8690h
694h	32	EMIF_CTLCFG_DENALI_CTL_421	0F30 8694h
698h	32	EMIF_CTLCFG_DENALI_CTL_422	0F30 8698h
2000h	32	EMIF_CTLCFG_DENALI_PI_0	0F30 A000h
2004h	32	EMIF_CTLCFG_DENALI_PI_1	0F30 A004h
2008h	32	EMIF_CTLCFG_DENALI_PI_2	0F30 A008h
200Ch	32	EMIF_CTLCFG_DENALI_PI_3	0F30 A00Ch
2010h	32	EMIF_CTLCFG_DENALI_PI_4	0F30 A010h
2014h	32	EMIF_CTLCFG_DENALI_PI_5	0F30 A014h
2018h	32	EMIF_CTLCFG_DENALI_PI_6	0F30 A018h
201Ch	32	EMIF_CTLCFG_DENALI_PI_7	0F30 A01Ch
2020h	32	EMIF_CTLCFG_DENALI_PI_8	0F30 A020h
2024h	32	EMIF_CTLCFG_DENALI_PI_9	0F30 A024h
2028h	32	EMIF_CTLCFG_DENALI_PI_10	0F30 A028h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
202Ch	32	EMIF_CTLCFG_DENALI_PI_11	0F30 A02Ch
2030h	32	EMIF_CTLCFG_DENALI_PI_12	0F30 A030h
2034h	32	EMIF_CTLCFG_DENALI_PI_13	0F30 A034h
2038h	32	EMIF_CTLCFG_DENALI_PI_14	0F30 A038h
203Ch	32	EMIF_CTLCFG_DENALI_PI_15	0F30 A03Ch
2040h	32	EMIF_CTLCFG_DENALI_PI_16	0F30 A040h
2044h	32	EMIF_CTLCFG_DENALI_PI_17	0F30 A044h
2048h	32	EMIF_CTLCFG_DENALI_PI_18	0F30 A048h
204Ch	32	EMIF_CTLCFG_DENALI_PI_19	0F30 A04Ch
2050h	32	EMIF_CTLCFG_DENALI_PI_20	0F30 A050h
2054h	32	EMIF_CTLCFG_DENALI_PI_21	0F30 A054h
2058h	32	EMIF_CTLCFG_DENALI_PI_22	0F30 A058h
205Ch	32	EMIF_CTLCFG_DENALI_PI_23	0F30 A05Ch
2060h	32	EMIF_CTLCFG_DENALI_PI_24	0F30 A060h
2064h	32	EMIF_CTLCFG_DENALI_PI_25	0F30 A064h
2068h	32	EMIF_CTLCFG_DENALI_PI_26	0F30 A068h
206Ch	32	EMIF_CTLCFG_DENALI_PI_27	0F30 A06Ch
2070h	32	EMIF_CTLCFG_DENALI_PI_28	0F30 A070h
2074h	32	EMIF_CTLCFG_DENALI_PI_29	0F30 A074h
2078h	32	EMIF_CTLCFG_DENALI_PI_30	0F30 A078h
207Ch	32	EMIF_CTLCFG_DENALI_PI_31	0F30 A07Ch
2080h	32	EMIF_CTLCFG_DENALI_PI_32	0F30 A080h
2084h	32	EMIF_CTLCFG_DENALI_PI_33	0F30 A084h
2088h	32	EMIF_CTLCFG_DENALI_PI_34	0F30 A088h
208Ch	32	EMIF_CTLCFG_DENALI_PI_35	0F30 A08Ch
2090h	32	EMIF_CTLCFG_DENALI_PI_36	0F30 A090h
2094h	32	EMIF_CTLCFG_DENALI_PI_37	0F30 A094h
2098h	32	EMIF_CTLCFG_DENALI_PI_38	0F30 A098h
209Ch	32	EMIF_CTLCFG_DENALI_PI_39	0F30 A09Ch
20A0h	32	EMIF_CTLCFG_DENALI_PI_40	0F30 A0A0h
20A4h	32	EMIF_CTLCFG_DENALI_PI_41	0F30 A0A4h
20A8h	32	EMIF_CTLCFG_DENALI_PI_42	0F30 A0A8h
20ACh	32	EMIF_CTLCFG_DENALI_PI_43	0F30 A0ACh
20B0h	32	EMIF_CTLCFG_DENALI_PI_44	0F30 A0B0h
20B4h	32	EMIF_CTLCFG_DENALI_PI_45	0F30 A0B4h
20B8h	32	EMIF_CTLCFG_DENALI_PI_46	0F30 A0B8h
20BCh	32	EMIF_CTLCFG_DENALI_PI_47	0F30 A0BCh
20C0h	32	EMIF_CTLCFG_DENALI_PI_48	0F30 A0C0h
20C4h	32	EMIF_CTLCFG_DENALI_PI_49	0F30 A0C4h
20C8h	32	EMIF_CTLCFG_DENALI_PI_50	0F30 A0C8h
20CCh	32	EMIF_CTLCFG_DENALI_PI_51	0F30 A0CCh
20D0h	32	EMIF_CTLCFG_DENALI_PI_52	0F30 A0D0h
20D4h	32	EMIF_CTLCFG_DENALI_PI_53	0F30 A0D4h
20D8h	32	EMIF_CTLCFG_DENALI_PI_54	0F30 A0D8h
20DCh	32	EMIF_CTLCFG_DENALI_PI_55	0F30 A0DCh

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
20E0h	32	EMIF_CTLCFG_DENALI_PI_56	0F30 A0E0h
20E4h	32	EMIF_CTLCFG_DENALI_PI_57	0F30 A0E4h
20E8h	32	EMIF_CTLCFG_DENALI_PI_58	0F30 A0E8h
20ECh	32	EMIF_CTLCFG_DENALI_PI_59	0F30 A0ECh
20F0h	32	EMIF_CTLCFG_DENALI_PI_60	0F30 A0F0h
20F4h	32	EMIF_CTLCFG_DENALI_PI_61	0F30 A0F4h
20F8h	32	EMIF_CTLCFG_DENALI_PI_62	0F30 A0F8h
20FCh	32	EMIF_CTLCFG_DENALI_PI_63	0F30 A0FCh
2100h	32	EMIF_CTLCFG_DENALI_PI_64	0F30 A100h
2104h	32	EMIF_CTLCFG_DENALI_PI_65	0F30 A104h
2108h	32	EMIF_CTLCFG_DENALI_PI_66	0F30 A108h
210Ch	32	EMIF_CTLCFG_DENALI_PI_67	0F30 A10Ch
2110h	32	EMIF_CTLCFG_DENALI_PI_68	0F30 A110h
2114h	32	EMIF_CTLCFG_DENALI_PI_69	0F30 A114h
2118h	32	EMIF_CTLCFG_DENALI_PI_70	0F30 A118h
211Ch	32	EMIF_CTLCFG_DENALI_PI_71	0F30 A11Ch
2120h	32	EMIF_CTLCFG_DENALI_PI_72	0F30 A120h
2124h	32	EMIF_CTLCFG_DENALI_PI_73	0F30 A124h
2128h	32	EMIF_CTLCFG_DENALI_PI_74	0F30 A128h
212Ch	32	EMIF_CTLCFG_DENALI_PI_75	0F30 A12Ch
2130h	32	EMIF_CTLCFG_DENALI_PI_76	0F30 A130h
2134h	32	EMIF_CTLCFG_DENALI_PI_77	0F30 A134h
2138h	32	EMIF_CTLCFG_DENALI_PI_78	0F30 A138h
213Ch	32	EMIF_CTLCFG_DENALI_PI_79	0F30 A13Ch
2140h	32	EMIF_CTLCFG_DENALI_PI_80	0F30 A140h
2144h	32	EMIF_CTLCFG_DENALI_PI_81	0F30 A144h
2148h	32	EMIF_CTLCFG_DENALI_PI_82	0F30 A148h
214Ch	32	EMIF_CTLCFG_DENALI_PI_83	0F30 A14Ch
2150h	32	EMIF_CTLCFG_DENALI_PI_84	0F30 A150h
2154h	32	EMIF_CTLCFG_DENALI_PI_85	0F30 A154h
2158h	32	EMIF_CTLCFG_DENALI_PI_86	0F30 A158h
215Ch	32	EMIF_CTLCFG_DENALI_PI_87	0F30 A15Ch
2160h	32	EMIF_CTLCFG_DENALI_PI_88	0F30 A160h
2164h	32	EMIF_CTLCFG_DENALI_PI_89	0F30 A164h
2168h	32	EMIF_CTLCFG_DENALI_PI_90	0F30 A168h
216Ch	32	EMIF_CTLCFG_DENALI_PI_91	0F30 A16Ch
2170h	32	EMIF_CTLCFG_DENALI_PI_92	0F30 A170h
2174h	32	EMIF_CTLCFG_DENALI_PI_93	0F30 A174h
2178h	32	EMIF_CTLCFG_DENALI_PI_94	0F30 A178h
217Ch	32	EMIF_CTLCFG_DENALI_PI_95	0F30 A17Ch
2180h	32	EMIF_CTLCFG_DENALI_PI_96	0F30 A180h
2184h	32	EMIF_CTLCFG_DENALI_PI_97	0F30 A184h
2188h	32	EMIF_CTLCFG_DENALI_PI_98	0F30 A188h
218Ch	32	EMIF_CTLCFG_DENALI_PI_99	0F30 A18Ch
2190h	32	EMIF_CTLCFG_DENALI_PI_100	0F30 A190h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
2194h	32	EMIF_CTLCFG_DENALI_PI_101	0F30 A194h
2198h	32	EMIF_CTLCFG_DENALI_PI_102	0F30 A198h
219Ch	32	EMIF_CTLCFG_DENALI_PI_103	0F30 A19Ch
21A0h	32	EMIF_CTLCFG_DENALI_PI_104	0F30 A1A0h
21A4h	32	EMIF_CTLCFG_DENALI_PI_105	0F30 A1A4h
21A8h	32	EMIF_CTLCFG_DENALI_PI_106	0F30 A1A8h
21ACh	32	EMIF_CTLCFG_DENALI_PI_107	0F30 A1ACh
21B0h	32	EMIF_CTLCFG_DENALI_PI_108	0F30 A1B0h
21B4h	32	EMIF_CTLCFG_DENALI_PI_109	0F30 A1B4h
21B8h	32	EMIF_CTLCFG_DENALI_PI_110	0F30 A1B8h
21BCh	32	EMIF_CTLCFG_DENALI_PI_111	0F30 A1BCh
21C0h	32	EMIF_CTLCFG_DENALI_PI_112	0F30 A1C0h
21C4h	32	EMIF_CTLCFG_DENALI_PI_113	0F30 A1C4h
21C8h	32	EMIF_CTLCFG_DENALI_PI_114	0F30 A1C8h
21CCh	32	EMIF_CTLCFG_DENALI_PI_115	0F30 A1CCh
21D0h	32	EMIF_CTLCFG_DENALI_PI_116	0F30 A1D0h
21D4h	32	EMIF_CTLCFG_DENALI_PI_117	0F30 A1D4h
21D8h	32	EMIF_CTLCFG_DENALI_PI_118	0F30 A1D8h
21DCh	32	EMIF_CTLCFG_DENALI_PI_119	0F30 A1DCh
21E0h	32	EMIF_CTLCFG_DENALI_PI_120	0F30 A1E0h
21E4h	32	EMIF_CTLCFG_DENALI_PI_121	0F30 A1E4h
21E8h	32	EMIF_CTLCFG_DENALI_PI_122	0F30 A1E8h
21ECh	32	EMIF_CTLCFG_DENALI_PI_123	0F30 A1ECh
21F0h	32	EMIF_CTLCFG_DENALI_PI_124	0F30 A1F0h
21F4h	32	EMIF_CTLCFG_DENALI_PI_125	0F30 A1F4h
21F8h	32	EMIF_CTLCFG_DENALI_PI_126	0F30 A1F8h
21FCh	32	EMIF_CTLCFG_DENALI_PI_127	0F30 A1FCh
2200h	32	EMIF_CTLCFG_DENALI_PI_128	0F30 A200h
2204h	32	EMIF_CTLCFG_DENALI_PI_129	0F30 A204h
2208h	32	EMIF_CTLCFG_DENALI_PI_130	0F30 A208h
220Ch	32	EMIF_CTLCFG_DENALI_PI_131	0F30 A20Ch
2210h	32	EMIF_CTLCFG_DENALI_PI_132	0F30 A210h
2214h	32	EMIF_CTLCFG_DENALI_PI_133	0F30 A214h
2218h	32	EMIF_CTLCFG_DENALI_PI_134	0F30 A218h
221Ch	32	EMIF_CTLCFG_DENALI_PI_135	0F30 A21Ch
2220h	32	EMIF_CTLCFG_DENALI_PI_136	0F30 A220h
2224h	32	EMIF_CTLCFG_DENALI_PI_137	0F30 A224h
2228h	32	EMIF_CTLCFG_DENALI_PI_138	0F30 A228h
222Ch	32	EMIF_CTLCFG_DENALI_PI_139	0F30 A22Ch
2230h	32	EMIF_CTLCFG_DENALI_PI_140	0F30 A230h
2234h	32	EMIF_CTLCFG_DENALI_PI_141	0F30 A234h
2238h	32	EMIF_CTLCFG_DENALI_PI_142	0F30 A238h
223Ch	32	EMIF_CTLCFG_DENALI_PI_143	0F30 A23Ch
2240h	32	EMIF_CTLCFG_DENALI_PI_144	0F30 A240h
2244h	32	EMIF_CTLCFG_DENALI_PI_145	0F30 A244h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
2248h	32	EMIF_CTLCFG_DENALI_PI_146	0F30 A248h
224Ch	32	EMIF_CTLCFG_DENALI_PI_147	0F30 A24Ch
2250h	32	EMIF_CTLCFG_DENALI_PI_148	0F30 A250h
2254h	32	EMIF_CTLCFG_DENALI_PI_149	0F30 A254h
2258h	32	EMIF_CTLCFG_DENALI_PI_150	0F30 A258h
225Ch	32	EMIF_CTLCFG_DENALI_PI_151	0F30 A25Ch
2260h	32	EMIF_CTLCFG_DENALI_PI_152	0F30 A260h
2264h	32	EMIF_CTLCFG_DENALI_PI_153	0F30 A264h
2268h	32	EMIF_CTLCFG_DENALI_PI_154	0F30 A268h
226Ch	32	EMIF_CTLCFG_DENALI_PI_155	0F30 A26Ch
2270h	32	EMIF_CTLCFG_DENALI_PI_156	0F30 A270h
2274h	32	EMIF_CTLCFG_DENALI_PI_157	0F30 A274h
2278h	32	EMIF_CTLCFG_DENALI_PI_158	0F30 A278h
227Ch	32	EMIF_CTLCFG_DENALI_PI_159	0F30 A27Ch
2280h	32	EMIF_CTLCFG_DENALI_PI_160	0F30 A280h
2284h	32	EMIF_CTLCFG_DENALI_PI_161	0F30 A284h
2288h	32	EMIF_CTLCFG_DENALI_PI_162	0F30 A288h
228Ch	32	EMIF_CTLCFG_DENALI_PI_163	0F30 A28Ch
2290h	32	EMIF_CTLCFG_DENALI_PI_164	0F30 A290h
2294h	32	EMIF_CTLCFG_DENALI_PI_165	0F30 A294h
2298h	32	EMIF_CTLCFG_DENALI_PI_166	0F30 A298h
229Ch	32	EMIF_CTLCFG_DENALI_PI_167	0F30 A29Ch
22A0h	32	EMIF_CTLCFG_DENALI_PI_168	0F30 A2A0h
22A4h	32	EMIF_CTLCFG_DENALI_PI_169	0F30 A2A4h
22A8h	32	EMIF_CTLCFG_DENALI_PI_170	0F30 A2A8h
22ACh	32	EMIF_CTLCFG_DENALI_PI_171	0F30 A2ACh
22B0h	32	EMIF_CTLCFG_DENALI_PI_172	0F30 A2B0h
22B4h	32	EMIF_CTLCFG_DENALI_PI_173	0F30 A2B4h
22B8h	32	EMIF_CTLCFG_DENALI_PI_174	0F30 A2B8h
22BCh	32	EMIF_CTLCFG_DENALI_PI_175	0F30 A2BCh
22C0h	32	EMIF_CTLCFG_DENALI_PI_176	0F30 A2C0h
22C4h	32	EMIF_CTLCFG_DENALI_PI_177	0F30 A2C4h
22C8h	32	EMIF_CTLCFG_DENALI_PI_178	0F30 A2C8h
22CCh	32	EMIF_CTLCFG_DENALI_PI_179	0F30 A2CCh
22D0h	32	EMIF_CTLCFG_DENALI_PI_180	0F30 A2D0h
22D4h	32	EMIF_CTLCFG_DENALI_PI_181	0F30 A2D4h
22D8h	32	EMIF_CTLCFG_DENALI_PI_182	0F30 A2D8h
22DCh	32	EMIF_CTLCFG_DENALI_PI_183	0F30 A2DCh
22E0h	32	EMIF_CTLCFG_DENALI_PI_184	0F30 A2E0h
22E4h	32	EMIF_CTLCFG_DENALI_PI_185	0F30 A2E4h
22E8h	32	EMIF_CTLCFG_DENALI_PI_186	0F30 A2E8h
22ECh	32	EMIF_CTLCFG_DENALI_PI_187	0F30 A2ECh
22F0h	32	EMIF_CTLCFG_DENALI_PI_188	0F30 A2F0h
22F4h	32	EMIF_CTLCFG_DENALI_PI_189	0F30 A2F4h
22F8h	32	EMIF_CTLCFG_DENALI_PI_190	0F30 A2F8h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
22FCh	32	EMIF_CTLCFG_DENALI_PI_191	0F30 A2FCh
2300h	32	EMIF_CTLCFG_DENALI_PI_192	0F30 A300h
2304h	32	EMIF_CTLCFG_DENALI_PI_193	0F30 A304h
2308h	32	EMIF_CTLCFG_DENALI_PI_194	0F30 A308h
230Ch	32	EMIF_CTLCFG_DENALI_PI_195	0F30 A30Ch
2310h	32	EMIF_CTLCFG_DENALI_PI_196	0F30 A310h
2314h	32	EMIF_CTLCFG_DENALI_PI_197	0F30 A314h
2318h	32	EMIF_CTLCFG_DENALI_PI_198	0F30 A318h
231Ch	32	EMIF_CTLCFG_DENALI_PI_199	0F30 A31Ch
2320h	32	EMIF_CTLCFG_DENALI_PI_200	0F30 A320h
2324h	32	EMIF_CTLCFG_DENALI_PI_201	0F30 A324h
2328h	32	EMIF_CTLCFG_DENALI_PI_202	0F30 A328h
232Ch	32	EMIF_CTLCFG_DENALI_PI_203	0F30 A32Ch
2330h	32	EMIF_CTLCFG_DENALI_PI_204	0F30 A330h
2334h	32	EMIF_CTLCFG_DENALI_PI_205	0F30 A334h
2338h	32	EMIF_CTLCFG_DENALI_PI_206	0F30 A338h
233Ch	32	EMIF_CTLCFG_DENALI_PI_207	0F30 A33Ch
2340h	32	EMIF_CTLCFG_DENALI_PI_208	0F30 A340h
2344h	32	EMIF_CTLCFG_DENALI_PI_209	0F30 A344h
2348h	32	EMIF_CTLCFG_DENALI_PI_210	0F30 A348h
234Ch	32	EMIF_CTLCFG_DENALI_PI_211	0F30 A34Ch
2350h	32	EMIF_CTLCFG_DENALI_PI_212	0F30 A350h
2354h	32	EMIF_CTLCFG_DENALI_PI_213	0F30 A354h
2358h	32	EMIF_CTLCFG_DENALI_PI_214	0F30 A358h
235Ch	32	EMIF_CTLCFG_DENALI_PI_215	0F30 A35Ch
2360h	32	EMIF_CTLCFG_DENALI_PI_216	0F30 A360h
2364h	32	EMIF_CTLCFG_DENALI_PI_217	0F30 A364h
2368h	32	EMIF_CTLCFG_DENALI_PI_218	0F30 A368h
236Ch	32	EMIF_CTLCFG_DENALI_PI_219	0F30 A36Ch
2370h	32	EMIF_CTLCFG_DENALI_PI_220	0F30 A370h
2374h	32	EMIF_CTLCFG_DENALI_PI_221	0F30 A374h
2378h	32	EMIF_CTLCFG_DENALI_PI_222	0F30 A378h
237Ch	32	EMIF_CTLCFG_DENALI_PI_223	0F30 A37Ch
2380h	32	EMIF_CTLCFG_DENALI_PI_224	0F30 A380h
2384h	32	EMIF_CTLCFG_DENALI_PI_225	0F30 A384h
2388h	32	EMIF_CTLCFG_DENALI_PI_226	0F30 A388h
238Ch	32	EMIF_CTLCFG_DENALI_PI_227	0F30 A38Ch
2390h	32	EMIF_CTLCFG_DENALI_PI_228	0F30 A390h
2394h	32	EMIF_CTLCFG_DENALI_PI_229	0F30 A394h
2398h	32	EMIF_CTLCFG_DENALI_PI_230	0F30 A398h
239Ch	32	EMIF_CTLCFG_DENALI_PI_231	0F30 A39Ch
23A0h	32	EMIF_CTLCFG_DENALI_PI_232	0F30 A3A0h
23A4h	32	EMIF_CTLCFG_DENALI_PI_233	0F30 A3A4h
23A8h	32	EMIF_CTLCFG_DENALI_PI_234	0F30 A3A8h
23ACh	32	EMIF_CTLCFG_DENALI_PI_235	0F30 A3ACh

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
23B0h	32	EMIF_CTLCFG_DENALI_PI_236	0F30 A3B0h
23B4h	32	EMIF_CTLCFG_DENALI_PI_237	0F30 A3B4h
23B8h	32	EMIF_CTLCFG_DENALI_PI_238	0F30 A3B8h
23BCh	32	EMIF_CTLCFG_DENALI_PI_239	0F30 A3BCh
23C0h	32	EMIF_CTLCFG_DENALI_PI_240	0F30 A3C0h
23C4h	32	EMIF_CTLCFG_DENALI_PI_241	0F30 A3C4h
23C8h	32	EMIF_CTLCFG_DENALI_PI_242	0F30 A3C8h
23CCh	32	EMIF_CTLCFG_DENALI_PI_243	0F30 A3CCh
23D0h	32	EMIF_CTLCFG_DENALI_PI_244	0F30 A3D0h
23D4h	32	EMIF_CTLCFG_DENALI_PI_245	0F30 A3D4h
23D8h	32	EMIF_CTLCFG_DENALI_PI_246	0F30 A3D8h
23DCh	32	EMIF_CTLCFG_DENALI_PI_247	0F30 A3DCh
23E0h	32	EMIF_CTLCFG_DENALI_PI_248	0F30 A3E0h
23E4h	32	EMIF_CTLCFG_DENALI_PI_249	0F30 A3E4h
23E8h	32	EMIF_CTLCFG_DENALI_PI_250	0F30 A3E8h
23ECh	32	EMIF_CTLCFG_DENALI_PI_251	0F30 A3ECh
23F0h	32	EMIF_CTLCFG_DENALI_PI_252	0F30 A3F0h
23F4h	32	EMIF_CTLCFG_DENALI_PI_253	0F30 A3F4h
23F8h	32	EMIF_CTLCFG_DENALI_PI_254	0F30 A3F8h
23FCh	32	EMIF_CTLCFG_DENALI_PI_255	0F30 A3FCh
2400h	32	EMIF_CTLCFG_DENALI_PI_256	0F30 A400h
2404h	32	EMIF_CTLCFG_DENALI_PI_257	0F30 A404h
2408h	32	EMIF_CTLCFG_DENALI_PI_258	0F30 A408h
240Ch	32	EMIF_CTLCFG_DENALI_PI_259	0F30 A40Ch
2410h	32	EMIF_CTLCFG_DENALI_PI_260	0F30 A410h
2414h	32	EMIF_CTLCFG_DENALI_PI_261	0F30 A414h
2418h	32	EMIF_CTLCFG_DENALI_PI_262	0F30 A418h
241Ch	32	EMIF_CTLCFG_DENALI_PI_263	0F30 A41Ch
2420h	32	EMIF_CTLCFG_DENALI_PI_264	0F30 A420h
2424h	32	EMIF_CTLCFG_DENALI_PI_265	0F30 A424h
2428h	32	EMIF_CTLCFG_DENALI_PI_266	0F30 A428h
242Ch	32	EMIF_CTLCFG_DENALI_PI_267	0F30 A42Ch
2430h	32	EMIF_CTLCFG_DENALI_PI_268	0F30 A430h
2434h	32	EMIF_CTLCFG_DENALI_PI_269	0F30 A434h
2438h	32	EMIF_CTLCFG_DENALI_PI_270	0F30 A438h
243Ch	32	EMIF_CTLCFG_DENALI_PI_271	0F30 A43Ch
2440h	32	EMIF_CTLCFG_DENALI_PI_272	0F30 A440h
2444h	32	EMIF_CTLCFG_DENALI_PI_273	0F30 A444h
2448h	32	EMIF_CTLCFG_DENALI_PI_274	0F30 A448h
244Ch	32	EMIF_CTLCFG_DENALI_PI_275	0F30 A44Ch
2450h	32	EMIF_CTLCFG_DENALI_PI_276	0F30 A450h
2454h	32	EMIF_CTLCFG_DENALI_PI_277	0F30 A454h
2458h	32	EMIF_CTLCFG_DENALI_PI_278	0F30 A458h
245Ch	32	EMIF_CTLCFG_DENALI_PI_279	0F30 A45Ch
2460h	32	EMIF_CTLCFG_DENALI_PI_280	0F30 A460h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
2464h	32	EMIF_CTLCFG_DENALI_PI_281	0F30 A464h
2468h	32	EMIF_CTLCFG_DENALI_PI_282	0F30 A468h
246Ch	32	EMIF_CTLCFG_DENALI_PI_283	0F30 A46Ch
2470h	32	EMIF_CTLCFG_DENALI_PI_284	0F30 A470h
2474h	32	EMIF_CTLCFG_DENALI_PI_285	0F30 A474h
2478h	32	EMIF_CTLCFG_DENALI_PI_286	0F30 A478h
247Ch	32	EMIF_CTLCFG_DENALI_PI_287	0F30 A47Ch
2480h	32	EMIF_CTLCFG_DENALI_PI_288	0F30 A480h
2484h	32	EMIF_CTLCFG_DENALI_PI_289	0F30 A484h
2488h	32	EMIF_CTLCFG_DENALI_PI_290	0F30 A488h
248Ch	32	EMIF_CTLCFG_DENALI_PI_291	0F30 A48Ch
2490h	32	EMIF_CTLCFG_DENALI_PI_292	0F30 A490h
2494h	32	EMIF_CTLCFG_DENALI_PI_293	0F30 A494h
2498h	32	EMIF_CTLCFG_DENALI_PI_294	0F30 A498h
249Ch	32	EMIF_CTLCFG_DENALI_PI_295	0F30 A49Ch
24A0h	32	EMIF_CTLCFG_DENALI_PI_296	0F30 A4A0h
24A4h	32	EMIF_CTLCFG_DENALI_PI_297	0F30 A4A4h
24A8h	32	EMIF_CTLCFG_DENALI_PI_298	0F30 A4A8h
24ACh	32	EMIF_CTLCFG_DENALI_PI_299	0F30 A4ACh
24B0h	32	EMIF_CTLCFG_DENALI_PI_300	0F30 A4B0h
24B4h	32	EMIF_CTLCFG_DENALI_PI_301	0F30 A4B4h
24B8h	32	EMIF_CTLCFG_DENALI_PI_302	0F30 A4B8h
24BCh	32	EMIF_CTLCFG_DENALI_PI_303	0F30 A4BCh
24C0h	32	EMIF_CTLCFG_DENALI_PI_304	0F30 A4C0h
24C4h	32	EMIF_CTLCFG_DENALI_PI_305	0F30 A4C4h
24C8h	32	EMIF_CTLCFG_DENALI_PI_306	0F30 A4C8h
24CCh	32	EMIF_CTLCFG_DENALI_PI_307	0F30 A4CCh
24D0h	32	EMIF_CTLCFG_DENALI_PI_308	0F30 A4D0h
24D4h	32	EMIF_CTLCFG_DENALI_PI_309	0F30 A4D4h
24D8h	32	EMIF_CTLCFG_DENALI_PI_310	0F30 A4D8h
24DCh	32	EMIF_CTLCFG_DENALI_PI_311	0F30 A4DCh
24E0h	32	EMIF_CTLCFG_DENALI_PI_312	0F30 A4E0h
24E4h	32	EMIF_CTLCFG_DENALI_PI_313	0F30 A4E4h
24E8h	32	EMIF_CTLCFG_DENALI_PI_314	0F30 A4E8h
24ECh	32	EMIF_CTLCFG_DENALI_PI_315	0F30 A4ECh
24F0h	32	EMIF_CTLCFG_DENALI_PI_316	0F30 A4F0h
24F4h	32	EMIF_CTLCFG_DENALI_PI_317	0F30 A4F4h
24F8h	32	EMIF_CTLCFG_DENALI_PI_318	0F30 A4F8h
24FCh	32	EMIF_CTLCFG_DENALI_PI_319	0F30 A4FCh
2500h	32	EMIF_CTLCFG_DENALI_PI_320	0F30 A500h
2504h	32	EMIF_CTLCFG_DENALI_PI_321	0F30 A504h
2508h	32	EMIF_CTLCFG_DENALI_PI_322	0F30 A508h
250Ch	32	EMIF_CTLCFG_DENALI_PI_323	0F30 A50Ch
2510h	32	EMIF_CTLCFG_DENALI_PI_324	0F30 A510h
2514h	32	EMIF_CTLCFG_DENALI_PI_325	0F30 A514h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
2518h	32	EMIF_CTLCFG_DENALI_PI_326	0F30 A518h
251Ch	32	EMIF_CTLCFG_DENALI_PI_327	0F30 A51Ch
2520h	32	EMIF_CTLCFG_DENALI_PI_328	0F30 A520h
2524h	32	EMIF_CTLCFG_DENALI_PI_329	0F30 A524h
2528h	32	EMIF_CTLCFG_DENALI_PI_330	0F30 A528h
252Ch	32	EMIF_CTLCFG_DENALI_PI_331	0F30 A52Ch
2530h	32	EMIF_CTLCFG_DENALI_PI_332	0F30 A530h
2534h	32	EMIF_CTLCFG_DENALI_PI_333	0F30 A534h
2538h	32	EMIF_CTLCFG_DENALI_PI_334	0F30 A538h
253Ch	32	EMIF_CTLCFG_DENALI_PI_335	0F30 A53Ch
2540h	32	EMIF_CTLCFG_DENALI_PI_336	0F30 A540h
2544h	32	EMIF_CTLCFG_DENALI_PI_337	0F30 A544h
2548h	32	EMIF_CTLCFG_DENALI_PI_338	0F30 A548h
254Ch	32	EMIF_CTLCFG_DENALI_PI_339	0F30 A54Ch
2550h	32	EMIF_CTLCFG_DENALI_PI_340	0F30 A550h
2554h	32	EMIF_CTLCFG_DENALI_PI_341	0F30 A554h
2558h	32	EMIF_CTLCFG_DENALI_PI_342	0F30 A558h
255Ch	32	EMIF_CTLCFG_DENALI_PI_343	0F30 A55Ch
2560h	32	EMIF_CTLCFG_DENALI_PI_344	0F30 A560h
4000h	32	EMIF_CTLCFG_DENALI_PHY_0	0F30 C000h
4004h	32	EMIF_CTLCFG_DENALI_PHY_1	0F30 C004h
4008h	32	EMIF_CTLCFG_DENALI_PHY_2	0F30 C008h
400Ch	32	EMIF_CTLCFG_DENALI_PHY_3	0F30 C00Ch
4010h	32	EMIF_CTLCFG_DENALI_PHY_4	0F30 C010h
4014h	32	EMIF_CTLCFG_DENALI_PHY_5	0F30 C014h
4018h	32	EMIF_CTLCFG_DENALI_PHY_6	0F30 C018h
401Ch	32	EMIF_CTLCFG_DENALI_PHY_7	0F30 C01Ch
4020h	32	EMIF_CTLCFG_DENALI_PHY_8	0F30 C020h
4024h	32	EMIF_CTLCFG_DENALI_PHY_9	0F30 C024h
4028h	32	EMIF_CTLCFG_DENALI_PHY_10	0F30 C028h
402Ch	32	EMIF_CTLCFG_DENALI_PHY_11	0F30 C02Ch
4030h	32	EMIF_CTLCFG_DENALI_PHY_12	0F30 C030h
4034h	32	EMIF_CTLCFG_DENALI_PHY_13	0F30 C034h
4038h	32	EMIF_CTLCFG_DENALI_PHY_14	0F30 C038h
403Ch	32	EMIF_CTLCFG_DENALI_PHY_15	0F30 C03Ch
4040h	32	EMIF_CTLCFG_DENALI_PHY_16	0F30 C040h
4044h	32	EMIF_CTLCFG_DENALI_PHY_17	0F30 C044h
4048h	32	EMIF_CTLCFG_DENALI_PHY_18	0F30 C048h
404Ch	32	EMIF_CTLCFG_DENALI_PHY_19	0F30 C04Ch
4050h	32	EMIF_CTLCFG_DENALI_PHY_20	0F30 C050h
4054h	32	EMIF_CTLCFG_DENALI_PHY_21	0F30 C054h
4058h	32	EMIF_CTLCFG_DENALI_PHY_22	0F30 C058h
405Ch	32	EMIF_CTLCFG_DENALI_PHY_23	0F30 C05Ch
4060h	32	EMIF_CTLCFG_DENALI_PHY_24	0F30 C060h
4064h	32	EMIF_CTLCFG_DENALI_PHY_25	0F30 C064h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
4068h	32	EMIF_CTLCFG_DENALI_PHY_26	0F30 C068h
406Ch	32	EMIF_CTLCFG_DENALI_PHY_27	0F30 C06Ch
4070h	32	EMIF_CTLCFG_DENALI_PHY_28	0F30 C070h
4074h	32	EMIF_CTLCFG_DENALI_PHY_29	0F30 C074h
4078h	32	EMIF_CTLCFG_DENALI_PHY_30	0F30 C078h
407Ch	32	EMIF_CTLCFG_DENALI_PHY_31	0F30 C07Ch
4080h	32	EMIF_CTLCFG_DENALI_PHY_32	0F30 C080h
4084h	32	EMIF_CTLCFG_DENALI_PHY_33	0F30 C084h
4088h	32	EMIF_CTLCFG_DENALI_PHY_34	0F30 C088h
408Ch	32	EMIF_CTLCFG_DENALI_PHY_35	0F30 C08Ch
4090h	32	EMIF_CTLCFG_DENALI_PHY_36	0F30 C090h
4094h	32	EMIF_CTLCFG_DENALI_PHY_37	0F30 C094h
4098h	32	EMIF_CTLCFG_DENALI_PHY_38	0F30 C098h
409Ch	32	EMIF_CTLCFG_DENALI_PHY_39	0F30 C09Ch
40A0h	32	EMIF_CTLCFG_DENALI_PHY_40	0F30 C0A0h
40A4h	32	EMIF_CTLCFG_DENALI_PHY_41	0F30 C0A4h
40A8h	32	EMIF_CTLCFG_DENALI_PHY_42	0F30 C0A8h
40ACh	32	EMIF_CTLCFG_DENALI_PHY_43	0F30 C0ACh
40B0h	32	EMIF_CTLCFG_DENALI_PHY_44	0F30 C0B0h
40B4h	32	EMIF_CTLCFG_DENALI_PHY_45	0F30 C0B4h
40B8h	32	EMIF_CTLCFG_DENALI_PHY_46	0F30 C0B8h
40BCh	32	EMIF_CTLCFG_DENALI_PHY_47	0F30 C0BCh
40C0h	32	EMIF_CTLCFG_DENALI_PHY_48	0F30 C0C0h
40C4h	32	EMIF_CTLCFG_DENALI_PHY_49	0F30 C0C4h
40C8h	32	EMIF_CTLCFG_DENALI_PHY_50	0F30 C0C8h
40CCh	32	EMIF_CTLCFG_DENALI_PHY_51	0F30 C0CCh
40D0h	32	EMIF_CTLCFG_DENALI_PHY_52	0F30 C0D0h
40D4h	32	EMIF_CTLCFG_DENALI_PHY_53	0F30 C0D4h
40D8h	32	EMIF_CTLCFG_DENALI_PHY_54	0F30 C0D8h
40DCh	32	EMIF_CTLCFG_DENALI_PHY_55	0F30 C0DCh
40E0h	32	EMIF_CTLCFG_DENALI_PHY_56	0F30 C0E0h
40E4h	32	EMIF_CTLCFG_DENALI_PHY_57	0F30 C0E4h
40E8h	32	EMIF_CTLCFG_DENALI_PHY_58	0F30 C0E8h
40ECh	32	EMIF_CTLCFG_DENALI_PHY_59	0F30 C0ECh
40F0h	32	EMIF_CTLCFG_DENALI_PHY_60	0F30 C0F0h
40F4h	32	EMIF_CTLCFG_DENALI_PHY_61	0F30 C0F4h
40F8h	32	EMIF_CTLCFG_DENALI_PHY_62	0F30 C0F8h
40FCh	32	EMIF_CTLCFG_DENALI_PHY_63	0F30 C0FCh
4100h	32	EMIF_CTLCFG_DENALI_PHY_64	0F30 C100h
4104h	32	EMIF_CTLCFG_DENALI_PHY_65	0F30 C104h
4108h	32	EMIF_CTLCFG_DENALI_PHY_66	0F30 C108h
410Ch	32	EMIF_CTLCFG_DENALI_PHY_67	0F30 C10Ch
4110h	32	EMIF_CTLCFG_DENALI_PHY_68	0F30 C110h
4114h	32	EMIF_CTLCFG_DENALI_PHY_69	0F30 C114h
4118h	32	EMIF_CTLCFG_DENALI_PHY_70	0F30 C118h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
411Ch	32	EMIF_CTLCFG_DENALI_PHY_71	0F30 C11Ch
4120h	32	EMIF_CTLCFG_DENALI_PHY_72	0F30 C120h
4124h	32	EMIF_CTLCFG_DENALI_PHY_73	0F30 C124h
4128h	32	EMIF_CTLCFG_DENALI_PHY_74	0F30 C128h
412Ch	32	EMIF_CTLCFG_DENALI_PHY_75	0F30 C12Ch
4130h	32	EMIF_CTLCFG_DENALI_PHY_76	0F30 C130h
4134h	32	EMIF_CTLCFG_DENALI_PHY_77	0F30 C134h
4138h	32	EMIF_CTLCFG_DENALI_PHY_78	0F30 C138h
413Ch	32	EMIF_CTLCFG_DENALI_PHY_79	0F30 C13Ch
4140h	32	EMIF_CTLCFG_DENALI_PHY_80	0F30 C140h
4144h	32	EMIF_CTLCFG_DENALI_PHY_81	0F30 C144h
4148h	32	EMIF_CTLCFG_DENALI_PHY_82	0F30 C148h
414Ch	32	EMIF_CTLCFG_DENALI_PHY_83	0F30 C14Ch
4150h	32	EMIF_CTLCFG_DENALI_PHY_84	0F30 C150h
4154h	32	EMIF_CTLCFG_DENALI_PHY_85	0F30 C154h
4158h	32	EMIF_CTLCFG_DENALI_PHY_86	0F30 C158h
415Ch	32	EMIF_CTLCFG_DENALI_PHY_87	0F30 C15Ch
4160h	32	EMIF_CTLCFG_DENALI_PHY_88	0F30 C160h
4164h	32	EMIF_CTLCFG_DENALI_PHY_89	0F30 C164h
4168h	32	EMIF_CTLCFG_DENALI_PHY_90	0F30 C168h
416Ch	32	EMIF_CTLCFG_DENALI_PHY_91	0F30 C16Ch
4170h	32	EMIF_CTLCFG_DENALI_PHY_92	0F30 C170h
4174h	32	EMIF_CTLCFG_DENALI_PHY_93	0F30 C174h
4178h	32	EMIF_CTLCFG_DENALI_PHY_94	0F30 C178h
417Ch	32	EMIF_CTLCFG_DENALI_PHY_95	0F30 C17Ch
4180h	32	EMIF_CTLCFG_DENALI_PHY_96	0F30 C180h
4184h	32	EMIF_CTLCFG_DENALI_PHY_97	0F30 C184h
4188h	32	EMIF_CTLCFG_DENALI_PHY_98	0F30 C188h
418Ch	32	EMIF_CTLCFG_DENALI_PHY_99	0F30 C18Ch
4190h	32	EMIF_CTLCFG_DENALI_PHY_100	0F30 C190h
4194h	32	EMIF_CTLCFG_DENALI_PHY_101	0F30 C194h
4198h	32	EMIF_CTLCFG_DENALI_PHY_102	0F30 C198h
419Ch	32	EMIF_CTLCFG_DENALI_PHY_103	0F30 C19Ch
41A0h	32	EMIF_CTLCFG_DENALI_PHY_104	0F30 C1A0h
41A4h	32	EMIF_CTLCFG_DENALI_PHY_105	0F30 C1A4h
41A8h	32	EMIF_CTLCFG_DENALI_PHY_106	0F30 C1A8h
41ACh	32	EMIF_CTLCFG_DENALI_PHY_107	0F30 C1ACh
41B0h	32	EMIF_CTLCFG_DENALI_PHY_108	0F30 C1B0h
41B4h	32	EMIF_CTLCFG_DENALI_PHY_109	0F30 C1B4h
41B8h	32	EMIF_CTLCFG_DENALI_PHY_110	0F30 C1B8h
41BCh	32	EMIF_CTLCFG_DENALI_PHY_111	0F30 C1BCh
41C0h	32	EMIF_CTLCFG_DENALI_PHY_112	0F30 C1C0h
41C4h	32	EMIF_CTLCFG_DENALI_PHY_113	0F30 C1C4h
41C8h	32	EMIF_CTLCFG_DENALI_PHY_114	0F30 C1C8h
41CCh	32	EMIF_CTLCFG_DENALI_PHY_115	0F30 C1CCh

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
41D0h	32	EMIF_CTLCFG_DENALI_PHY_116	0F30 C1D0h
41D4h	32	EMIF_CTLCFG_DENALI_PHY_117	0F30 C1D4h
41D8h	32	EMIF_CTLCFG_DENALI_PHY_118	0F30 C1D8h
41DCh	32	EMIF_CTLCFG_DENALI_PHY_119	0F30 C1DCh
41E0h	32	EMIF_CTLCFG_DENALI_PHY_120	0F30 C1E0h
41E4h	32	EMIF_CTLCFG_DENALI_PHY_121	0F30 C1E4h
41E8h	32	EMIF_CTLCFG_DENALI_PHY_122	0F30 C1E8h
41ECh	32	EMIF_CTLCFG_DENALI_PHY_123	0F30 C1ECh
41F0h	32	EMIF_CTLCFG_DENALI_PHY_124	0F30 C1F0h
41F4h	32	EMIF_CTLCFG_DENALI_PHY_125	0F30 C1F4h
4400h	32	EMIF_CTLCFG_DENALI_PHY_256	0F30 C400h
4404h	32	EMIF_CTLCFG_DENALI_PHY_257	0F30 C404h
4408h	32	EMIF_CTLCFG_DENALI_PHY_258	0F30 C408h
440Ch	32	EMIF_CTLCFG_DENALI_PHY_259	0F30 C40Ch
4410h	32	EMIF_CTLCFG_DENALI_PHY_260	0F30 C410h
4414h	32	EMIF_CTLCFG_DENALI_PHY_261	0F30 C414h
4418h	32	EMIF_CTLCFG_DENALI_PHY_262	0F30 C418h
441Ch	32	EMIF_CTLCFG_DENALI_PHY_263	0F30 C41Ch
4420h	32	EMIF_CTLCFG_DENALI_PHY_264	0F30 C420h
4424h	32	EMIF_CTLCFG_DENALI_PHY_265	0F30 C424h
4428h	32	EMIF_CTLCFG_DENALI_PHY_266	0F30 C428h
442Ch	32	EMIF_CTLCFG_DENALI_PHY_267	0F30 C42Ch
4430h	32	EMIF_CTLCFG_DENALI_PHY_268	0F30 C430h
4434h	32	EMIF_CTLCFG_DENALI_PHY_269	0F30 C434h
4438h	32	EMIF_CTLCFG_DENALI_PHY_270	0F30 C438h
443Ch	32	EMIF_CTLCFG_DENALI_PHY_271	0F30 C43Ch
4440h	32	EMIF_CTLCFG_DENALI_PHY_272	0F30 C440h
4444h	32	EMIF_CTLCFG_DENALI_PHY_273	0F30 C444h
4448h	32	EMIF_CTLCFG_DENALI_PHY_274	0F30 C448h
444Ch	32	EMIF_CTLCFG_DENALI_PHY_275	0F30 C44Ch
4450h	32	EMIF_CTLCFG_DENALI_PHY_276	0F30 C450h
4454h	32	EMIF_CTLCFG_DENALI_PHY_277	0F30 C454h
4458h	32	EMIF_CTLCFG_DENALI_PHY_278	0F30 C458h
445Ch	32	EMIF_CTLCFG_DENALI_PHY_279	0F30 C45Ch
4460h	32	EMIF_CTLCFG_DENALI_PHY_280	0F30 C460h
4464h	32	EMIF_CTLCFG_DENALI_PHY_281	0F30 C464h
4468h	32	EMIF_CTLCFG_DENALI_PHY_282	0F30 C468h
446Ch	32	EMIF_CTLCFG_DENALI_PHY_283	0F30 C46Ch
4470h	32	EMIF_CTLCFG_DENALI_PHY_284	0F30 C470h
4474h	32	EMIF_CTLCFG_DENALI_PHY_285	0F30 C474h
4478h	32	EMIF_CTLCFG_DENALI_PHY_286	0F30 C478h
447Ch	32	EMIF_CTLCFG_DENALI_PHY_287	0F30 C47Ch
4480h	32	EMIF_CTLCFG_DENALI_PHY_288	0F30 C480h
4484h	32	EMIF_CTLCFG_DENALI_PHY_289	0F30 C484h
4488h	32	EMIF_CTLCFG_DENALI_PHY_290	0F30 C488h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
448Ch	32	EMIF_CTLCFG_DENALI_PHY_291	0F30 C48Ch
4490h	32	EMIF_CTLCFG_DENALI_PHY_292	0F30 C490h
4494h	32	EMIF_CTLCFG_DENALI_PHY_293	0F30 C494h
4498h	32	EMIF_CTLCFG_DENALI_PHY_294	0F30 C498h
449Ch	32	EMIF_CTLCFG_DENALI_PHY_295	0F30 C49Ch
44A0h	32	EMIF_CTLCFG_DENALI_PHY_296	0F30 C4A0h
44A4h	32	EMIF_CTLCFG_DENALI_PHY_297	0F30 C4A4h
44A8h	32	EMIF_CTLCFG_DENALI_PHY_298	0F30 C4A8h
44ACh	32	EMIF_CTLCFG_DENALI_PHY_299	0F30 C4ACh
44B0h	32	EMIF_CTLCFG_DENALI_PHY_300	0F30 C4B0h
44B4h	32	EMIF_CTLCFG_DENALI_PHY_301	0F30 C4B4h
44B8h	32	EMIF_CTLCFG_DENALI_PHY_302	0F30 C4B8h
44BCh	32	EMIF_CTLCFG_DENALI_PHY_303	0F30 C4BCh
44C0h	32	EMIF_CTLCFG_DENALI_PHY_304	0F30 C4C0h
44C4h	32	EMIF_CTLCFG_DENALI_PHY_305	0F30 C4C4h
44C8h	32	EMIF_CTLCFG_DENALI_PHY_306	0F30 C4C8h
44CCh	32	EMIF_CTLCFG_DENALI_PHY_307	0F30 C4CCh
44D0h	32	EMIF_CTLCFG_DENALI_PHY_308	0F30 C4D0h
44D4h	32	EMIF_CTLCFG_DENALI_PHY_309	0F30 C4D4h
44D8h	32	EMIF_CTLCFG_DENALI_PHY_310	0F30 C4D8h
44DCh	32	EMIF_CTLCFG_DENALI_PHY_311	0F30 C4DCh
44E0h	32	EMIF_CTLCFG_DENALI_PHY_312	0F30 C4E0h
44E4h	32	EMIF_CTLCFG_DENALI_PHY_313	0F30 C4E4h
44E8h	32	EMIF_CTLCFG_DENALI_PHY_314	0F30 C4E8h
44ECh	32	EMIF_CTLCFG_DENALI_PHY_315	0F30 C4ECh
44F0h	32	EMIF_CTLCFG_DENALI_PHY_316	0F30 C4F0h
44F4h	32	EMIF_CTLCFG_DENALI_PHY_317	0F30 C4F4h
44F8h	32	EMIF_CTLCFG_DENALI_PHY_318	0F30 C4F8h
44FCh	32	EMIF_CTLCFG_DENALI_PHY_319	0F30 C4FCh
4500h	32	EMIF_CTLCFG_DENALI_PHY_320	0F30 C500h
4504h	32	EMIF_CTLCFG_DENALI_PHY_321	0F30 C504h
4508h	32	EMIF_CTLCFG_DENALI_PHY_322	0F30 C508h
450Ch	32	EMIF_CTLCFG_DENALI_PHY_323	0F30 C50Ch
4510h	32	EMIF_CTLCFG_DENALI_PHY_324	0F30 C510h
4514h	32	EMIF_CTLCFG_DENALI_PHY_325	0F30 C514h
4518h	32	EMIF_CTLCFG_DENALI_PHY_326	0F30 C518h
451Ch	32	EMIF_CTLCFG_DENALI_PHY_327	0F30 C51Ch
4520h	32	EMIF_CTLCFG_DENALI_PHY_328	0F30 C520h
4524h	32	EMIF_CTLCFG_DENALI_PHY_329	0F30 C524h
4528h	32	EMIF_CTLCFG_DENALI_PHY_330	0F30 C528h
452Ch	32	EMIF_CTLCFG_DENALI_PHY_331	0F30 C52Ch
4530h	32	EMIF_CTLCFG_DENALI_PHY_332	0F30 C530h
4534h	32	EMIF_CTLCFG_DENALI_PHY_333	0F30 C534h
4538h	32	EMIF_CTLCFG_DENALI_PHY_334	0F30 C538h
453Ch	32	EMIF_CTLCFG_DENALI_PHY_335	0F30 C53Ch

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
4540h	32	EMIF_CTLCFG_DENALI_PHY_336	0F30 C540h
4544h	32	EMIF_CTLCFG_DENALI_PHY_337	0F30 C544h
4548h	32	EMIF_CTLCFG_DENALI_PHY_338	0F30 C548h
454Ch	32	EMIF_CTLCFG_DENALI_PHY_339	0F30 C54Ch
4550h	32	EMIF_CTLCFG_DENALI_PHY_340	0F30 C550h
4554h	32	EMIF_CTLCFG_DENALI_PHY_341	0F30 C554h
4558h	32	EMIF_CTLCFG_DENALI_PHY_342	0F30 C558h
455Ch	32	EMIF_CTLCFG_DENALI_PHY_343	0F30 C55Ch
4560h	32	EMIF_CTLCFG_DENALI_PHY_344	0F30 C560h
4564h	32	EMIF_CTLCFG_DENALI_PHY_345	0F30 C564h
4568h	32	EMIF_CTLCFG_DENALI_PHY_346	0F30 C568h
456Ch	32	EMIF_CTLCFG_DENALI_PHY_347	0F30 C56Ch
4570h	32	EMIF_CTLCFG_DENALI_PHY_348	0F30 C570h
4574h	32	EMIF_CTLCFG_DENALI_PHY_349	0F30 C574h
4578h	32	EMIF_CTLCFG_DENALI_PHY_350	0F30 C578h
457Ch	32	EMIF_CTLCFG_DENALI_PHY_351	0F30 C57Ch
4580h	32	EMIF_CTLCFG_DENALI_PHY_352	0F30 C580h
4584h	32	EMIF_CTLCFG_DENALI_PHY_353	0F30 C584h
4588h	32	EMIF_CTLCFG_DENALI_PHY_354	0F30 C588h
458Ch	32	EMIF_CTLCFG_DENALI_PHY_355	0F30 C58Ch
4590h	32	EMIF_CTLCFG_DENALI_PHY_356	0F30 C590h
4594h	32	EMIF_CTLCFG_DENALI_PHY_357	0F30 C594h
4598h	32	EMIF_CTLCFG_DENALI_PHY_358	0F30 C598h
459Ch	32	EMIF_CTLCFG_DENALI_PHY_359	0F30 C59Ch
45A0h	32	EMIF_CTLCFG_DENALI_PHY_360	0F30 C5A0h
45A4h	32	EMIF_CTLCFG_DENALI_PHY_361	0F30 C5A4h
45A8h	32	EMIF_CTLCFG_DENALI_PHY_362	0F30 C5A8h
45ACh	32	EMIF_CTLCFG_DENALI_PHY_363	0F30 C5ACh
45B0h	32	EMIF_CTLCFG_DENALI_PHY_364	0F30 C5B0h
45B4h	32	EMIF_CTLCFG_DENALI_PHY_365	0F30 C5B4h
45B8h	32	EMIF_CTLCFG_DENALI_PHY_366	0F30 C5B8h
45BCh	32	EMIF_CTLCFG_DENALI_PHY_367	0F30 C5BCh
45C0h	32	EMIF_CTLCFG_DENALI_PHY_368	0F30 C5C0h
45C4h	32	EMIF_CTLCFG_DENALI_PHY_369	0F30 C5C4h
45C8h	32	EMIF_CTLCFG_DENALI_PHY_370	0F30 C5C8h
45CCh	32	EMIF_CTLCFG_DENALI_PHY_371	0F30 C5CCh
45D0h	32	EMIF_CTLCFG_DENALI_PHY_372	0F30 C5D0h
45D4h	32	EMIF_CTLCFG_DENALI_PHY_373	0F30 C5D4h
45D8h	32	EMIF_CTLCFG_DENALI_PHY_374	0F30 C5D8h
45DCh	32	EMIF_CTLCFG_DENALI_PHY_375	0F30 C5DCh
45E0h	32	EMIF_CTLCFG_DENALI_PHY_376	0F30 C5E0h
45E4h	32	EMIF_CTLCFG_DENALI_PHY_377	0F30 C5E4h
45E8h	32	EMIF_CTLCFG_DENALI_PHY_378	0F30 C5E8h
45ECh	32	EMIF_CTLCFG_DENALI_PHY_379	0F30 C5ECh
45F0h	32	EMIF_CTLCFG_DENALI_PHY_380	0F30 C5F0h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
45F4h	32	EMIF_CTLCFG_DENALI_PHY_381	0F30 C5F4h
4800h	32	EMIF_CTLCFG_DENALI_PHY_512	0F30 C800h
4804h	32	EMIF_CTLCFG_DENALI_PHY_513	0F30 C804h
4808h	32	EMIF_CTLCFG_DENALI_PHY_514	0F30 C808h
480Ch	32	EMIF_CTLCFG_DENALI_PHY_515	0F30 C80Ch
4810h	32	EMIF_CTLCFG_DENALI_PHY_516	0F30 C810h
4814h	32	EMIF_CTLCFG_DENALI_PHY_517	0F30 C814h
4818h	32	EMIF_CTLCFG_DENALI_PHY_518	0F30 C818h
481Ch	32	EMIF_CTLCFG_DENALI_PHY_519	0F30 C81Ch
4820h	32	EMIF_CTLCFG_DENALI_PHY_520	0F30 C820h
4824h	32	EMIF_CTLCFG_DENALI_PHY_521	0F30 C824h
4828h	32	EMIF_CTLCFG_DENALI_PHY_522	0F30 C828h
482Ch	32	EMIF_CTLCFG_DENALI_PHY_523	0F30 C82Ch
4830h	32	EMIF_CTLCFG_DENALI_PHY_524	0F30 C830h
4834h	32	EMIF_CTLCFG_DENALI_PHY_525	0F30 C834h
4838h	32	EMIF_CTLCFG_DENALI_PHY_526	0F30 C838h
483Ch	32	EMIF_CTLCFG_DENALI_PHY_527	0F30 C83Ch
4840h	32	EMIF_CTLCFG_DENALI_PHY_528	0F30 C840h
4844h	32	EMIF_CTLCFG_DENALI_PHY_529	0F30 C844h
4848h	32	EMIF_CTLCFG_DENALI_PHY_530	0F30 C848h
484Ch	32	EMIF_CTLCFG_DENALI_PHY_531	0F30 C84Ch
4850h	32	EMIF_CTLCFG_DENALI_PHY_532	0F30 C850h
4854h	32	EMIF_CTLCFG_DENALI_PHY_533	0F30 C854h
4858h	32	EMIF_CTLCFG_DENALI_PHY_534	0F30 C858h
485Ch	32	EMIF_CTLCFG_DENALI_PHY_535	0F30 C85Ch
4860h	32	EMIF_CTLCFG_DENALI_PHY_536	0F30 C860h
4864h	32	EMIF_CTLCFG_DENALI_PHY_537	0F30 C864h
4868h	32	EMIF_CTLCFG_DENALI_PHY_538	0F30 C868h
486Ch	32	EMIF_CTLCFG_DENALI_PHY_539	0F30 C86Ch
4870h	32	EMIF_CTLCFG_DENALI_PHY_540	0F30 C870h
4874h	32	EMIF_CTLCFG_DENALI_PHY_541	0F30 C874h
4878h	32	EMIF_CTLCFG_DENALI_PHY_542	0F30 C878h
487Ch	32	EMIF_CTLCFG_DENALI_PHY_543	0F30 C87Ch
4880h	32	EMIF_CTLCFG_DENALI_PHY_544	0F30 C880h
4884h	32	EMIF_CTLCFG_DENALI_PHY_545	0F30 C884h
4888h	32	EMIF_CTLCFG_DENALI_PHY_546	0F30 C888h
488Ch	32	EMIF_CTLCFG_DENALI_PHY_547	0F30 C88Ch
4890h	32	EMIF_CTLCFG_DENALI_PHY_548	0F30 C890h
4894h	32	EMIF_CTLCFG_DENALI_PHY_549	0F30 C894h
4898h	32	EMIF_CTLCFG_DENALI_PHY_550	0F30 C898h
489Ch	32	EMIF_CTLCFG_DENALI_PHY_551	0F30 C89Ch
48A0h	32	EMIF_CTLCFG_DENALI_PHY_552	0F30 C8A0h
48A4h	32	EMIF_CTLCFG_DENALI_PHY_553	0F30 C8A4h
48A8h	32	EMIF_CTLCFG_DENALI_PHY_554	0F30 C8A8h
4C00h	32	EMIF_CTLCFG_DENALI_PHY_768	0F30 CC00h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
4C04h	32	EMIF_CTLCFG_DENALI_PHY_769	0F30 CC04h
4C08h	32	EMIF_CTLCFG_DENALI_PHY_770	0F30 CC08h
4C0Ch	32	EMIF_CTLCFG_DENALI_PHY_771	0F30 CC0Ch
4C10h	32	EMIF_CTLCFG_DENALI_PHY_772	0F30 CC10h
4C14h	32	EMIF_CTLCFG_DENALI_PHY_773	0F30 CC14h
4C18h	32	EMIF_CTLCFG_DENALI_PHY_774	0F30 CC18h
4C1Ch	32	EMIF_CTLCFG_DENALI_PHY_775	0F30 CC1Ch
4C20h	32	EMIF_CTLCFG_DENALI_PHY_776	0F30 CC20h
4C24h	32	EMIF_CTLCFG_DENALI_PHY_777	0F30 CC24h
4C28h	32	EMIF_CTLCFG_DENALI_PHY_778	0F30 CC28h
4C2Ch	32	EMIF_CTLCFG_DENALI_PHY_779	0F30 CC2Ch
4C30h	32	EMIF_CTLCFG_DENALI_PHY_780	0F30 CC30h
4C34h	32	EMIF_CTLCFG_DENALI_PHY_781	0F30 CC34h
4C38h	32	EMIF_CTLCFG_DENALI_PHY_782	0F30 CC38h
4C3Ch	32	EMIF_CTLCFG_DENALI_PHY_783	0F30 CC3Ch
4C40h	32	EMIF_CTLCFG_DENALI_PHY_784	0F30 CC40h
4C44h	32	EMIF_CTLCFG_DENALI_PHY_785	0F30 CC44h
4C48h	32	EMIF_CTLCFG_DENALI_PHY_786	0F30 CC48h
4C4Ch	32	EMIF_CTLCFG_DENALI_PHY_787	0F30 CC4Ch
4C50h	32	EMIF_CTLCFG_DENALI_PHY_788	0F30 CC50h
4C54h	32	EMIF_CTLCFG_DENALI_PHY_789	0F30 CC54h
4C58h	32	EMIF_CTLCFG_DENALI_PHY_790	0F30 CC58h
4C5Ch	32	EMIF_CTLCFG_DENALI_PHY_791	0F30 CC5Ch
4C60h	32	EMIF_CTLCFG_DENALI_PHY_792	0F30 CC60h
4C64h	32	EMIF_CTLCFG_DENALI_PHY_793	0F30 CC64h
4C68h	32	EMIF_CTLCFG_DENALI_PHY_794	0F30 CC68h
4C6Ch	32	EMIF_CTLCFG_DENALI_PHY_795	0F30 CC6Ch
4C70h	32	EMIF_CTLCFG_DENALI_PHY_796	0F30 CC70h
4C74h	32	EMIF_CTLCFG_DENALI_PHY_797	0F30 CC74h
4C78h	32	EMIF_CTLCFG_DENALI_PHY_798	0F30 CC78h
4C7Ch	32	EMIF_CTLCFG_DENALI_PHY_799	0F30 CC7Ch
4C80h	32	EMIF_CTLCFG_DENALI_PHY_800	0F30 CC80h
4C84h	32	EMIF_CTLCFG_DENALI_PHY_801	0F30 CC84h
4C88h	32	EMIF_CTLCFG_DENALI_PHY_802	0F30 CC88h
4C8Ch	32	EMIF_CTLCFG_DENALI_PHY_803	0F30 CC8Ch
4C90h	32	EMIF_CTLCFG_DENALI_PHY_804	0F30 CC90h
4C94h	32	EMIF_CTLCFG_DENALI_PHY_805	0F30 CC94h
4C98h	32	EMIF_CTLCFG_DENALI_PHY_806	0F30 CC98h
4C9Ch	32	EMIF_CTLCFG_DENALI_PHY_807	0F30 CC9Ch
4CA0h	32	EMIF_CTLCFG_DENALI_PHY_808	0F30 CCA0h
4CA4h	32	EMIF_CTLCFG_DENALI_PHY_809	0F30 CCA4h
4CA8h	32	EMIF_CTLCFG_DENALI_PHY_810	0F30 CCA8h
5000h	32	EMIF_CTLCFG_DENALI_PHY_1024	0F30 D000h
5004h	32	EMIF_CTLCFG_DENALI_PHY_1025	0F30 D004h
5008h	32	EMIF_CTLCFG_DENALI_PHY_1026	0F30 D008h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
500Ch	32	EMIF_CTLCFG_DENALI_PHY_1027	0F30 D00Ch
5010h	32	EMIF_CTLCFG_DENALI_PHY_1028	0F30 D010h
5014h	32	EMIF_CTLCFG_DENALI_PHY_1029	0F30 D014h
5018h	32	EMIF_CTLCFG_DENALI_PHY_1030	0F30 D018h
501Ch	32	EMIF_CTLCFG_DENALI_PHY_1031	0F30 D01Ch
5020h	32	EMIF_CTLCFG_DENALI_PHY_1032	0F30 D020h
5024h	32	EMIF_CTLCFG_DENALI_PHY_1033	0F30 D024h
5028h	32	EMIF_CTLCFG_DENALI_PHY_1034	0F30 D028h
502Ch	32	EMIF_CTLCFG_DENALI_PHY_1035	0F30 D02Ch
5030h	32	EMIF_CTLCFG_DENALI_PHY_1036	0F30 D030h
5034h	32	EMIF_CTLCFG_DENALI_PHY_1037	0F30 D034h
5038h	32	EMIF_CTLCFG_DENALI_PHY_1038	0F30 D038h
503Ch	32	EMIF_CTLCFG_DENALI_PHY_1039	0F30 D03Ch
5040h	32	EMIF_CTLCFG_DENALI_PHY_1040	0F30 D040h
5044h	32	EMIF_CTLCFG_DENALI_PHY_1041	0F30 D044h
5048h	32	EMIF_CTLCFG_DENALI_PHY_1042	0F30 D048h
504Ch	32	EMIF_CTLCFG_DENALI_PHY_1043	0F30 D04Ch
5050h	32	EMIF_CTLCFG_DENALI_PHY_1044	0F30 D050h
5054h	32	EMIF_CTLCFG_DENALI_PHY_1045	0F30 D054h
5058h	32	EMIF_CTLCFG_DENALI_PHY_1046	0F30 D058h
505Ch	32	EMIF_CTLCFG_DENALI_PHY_1047	0F30 D05Ch
5060h	32	EMIF_CTLCFG_DENALI_PHY_1048	0F30 D060h
5064h	32	EMIF_CTLCFG_DENALI_PHY_1049	0F30 D064h
5068h	32	EMIF_CTLCFG_DENALI_PHY_1050	0F30 D068h
506Ch	32	EMIF_CTLCFG_DENALI_PHY_1051	0F30 D06Ch
5070h	32	EMIF_CTLCFG_DENALI_PHY_1052	0F30 D070h
5074h	32	EMIF_CTLCFG_DENALI_PHY_1053	0F30 D074h
5078h	32	EMIF_CTLCFG_DENALI_PHY_1054	0F30 D078h
507Ch	32	EMIF_CTLCFG_DENALI_PHY_1055	0F30 D07Ch
5080h	32	EMIF_CTLCFG_DENALI_PHY_1056	0F30 D080h
5084h	32	EMIF_CTLCFG_DENALI_PHY_1057	0F30 D084h
5088h	32	EMIF_CTLCFG_DENALI_PHY_1058	0F30 D088h
508Ch	32	EMIF_CTLCFG_DENALI_PHY_1059	0F30 D08Ch
5090h	32	EMIF_CTLCFG_DENALI_PHY_1060	0F30 D090h
5094h	32	EMIF_CTLCFG_DENALI_PHY_1061	0F30 D094h
5098h	32	EMIF_CTLCFG_DENALI_PHY_1062	0F30 D098h
509Ch	32	EMIF_CTLCFG_DENALI_PHY_1063	0F30 D09Ch
50A0h	32	EMIF_CTLCFG_DENALI_PHY_1064	0F30 D0A0h
50A4h	32	EMIF_CTLCFG_DENALI_PHY_1065	0F30 D0A4h
50A8h	32	EMIF_CTLCFG_DENALI_PHY_1066	0F30 D0A8h
5400h	32	EMIF_CTLCFG_DENALI_PHY_1280	0F30 D400h
5404h	32	EMIF_CTLCFG_DENALI_PHY_1281	0F30 D404h
5408h	32	EMIF_CTLCFG_DENALI_PHY_1282	0F30 D408h
540Ch	32	EMIF_CTLCFG_DENALI_PHY_1283	0F30 D40Ch
5410h	32	EMIF_CTLCFG_DENALI_PHY_1284	0F30 D410h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
5414h	32	EMIF_CTLCFG_DENALI_PHY_1285	0F30 D414h
5418h	32	EMIF_CTLCFG_DENALI_PHY_1286	0F30 D418h
541Ch	32	EMIF_CTLCFG_DENALI_PHY_1287	0F30 D41Ch
5420h	32	EMIF_CTLCFG_DENALI_PHY_1288	0F30 D420h
5424h	32	EMIF_CTLCFG_DENALI_PHY_1289	0F30 D424h
5428h	32	EMIF_CTLCFG_DENALI_PHY_1290	0F30 D428h
542Ch	32	EMIF_CTLCFG_DENALI_PHY_1291	0F30 D42Ch
5430h	32	EMIF_CTLCFG_DENALI_PHY_1292	0F30 D430h
5434h	32	EMIF_CTLCFG_DENALI_PHY_1293	0F30 D434h
5438h	32	EMIF_CTLCFG_DENALI_PHY_1294	0F30 D438h
543Ch	32	EMIF_CTLCFG_DENALI_PHY_1295	0F30 D43Ch
5440h	32	EMIF_CTLCFG_DENALI_PHY_1296	0F30 D440h
5444h	32	EMIF_CTLCFG_DENALI_PHY_1297	0F30 D444h
5448h	32	EMIF_CTLCFG_DENALI_PHY_1298	0F30 D448h
544Ch	32	EMIF_CTLCFG_DENALI_PHY_1299	0F30 D44Ch
5450h	32	EMIF_CTLCFG_DENALI_PHY_1300	0F30 D450h
5454h	32	EMIF_CTLCFG_DENALI_PHY_1301	0F30 D454h
5458h	32	EMIF_CTLCFG_DENALI_PHY_1302	0F30 D458h
545Ch	32	EMIF_CTLCFG_DENALI_PHY_1303	0F30 D45Ch
5460h	32	EMIF_CTLCFG_DENALI_PHY_1304	0F30 D460h
5464h	32	EMIF_CTLCFG_DENALI_PHY_1305	0F30 D464h
5468h	32	EMIF_CTLCFG_DENALI_PHY_1306	0F30 D468h
546Ch	32	EMIF_CTLCFG_DENALI_PHY_1307	0F30 D46Ch
5470h	32	EMIF_CTLCFG_DENALI_PHY_1308	0F30 D470h
5474h	32	EMIF_CTLCFG_DENALI_PHY_1309	0F30 D474h
5478h	32	EMIF_CTLCFG_DENALI_PHY_1310	0F30 D478h
547Ch	32	EMIF_CTLCFG_DENALI_PHY_1311	0F30 D47Ch
5480h	32	EMIF_CTLCFG_DENALI_PHY_1312	0F30 D480h
5484h	32	EMIF_CTLCFG_DENALI_PHY_1313	0F30 D484h
5488h	32	EMIF_CTLCFG_DENALI_PHY_1314	0F30 D488h
548Ch	32	EMIF_CTLCFG_DENALI_PHY_1315	0F30 D48Ch
5490h	32	EMIF_CTLCFG_DENALI_PHY_1316	0F30 D490h
5494h	32	EMIF_CTLCFG_DENALI_PHY_1317	0F30 D494h
5498h	32	EMIF_CTLCFG_DENALI_PHY_1318	0F30 D498h
549Ch	32	EMIF_CTLCFG_DENALI_PHY_1319	0F30 D49Ch
54A0h	32	EMIF_CTLCFG_DENALI_PHY_1320	0F30 D4A0h
54A4h	32	EMIF_CTLCFG_DENALI_PHY_1321	0F30 D4A4h
54A8h	32	EMIF_CTLCFG_DENALI_PHY_1322	0F30 D4A8h
54ACh	32	EMIF_CTLCFG_DENALI_PHY_1323	0F30 D4ACh
54B0h	32	EMIF_CTLCFG_DENALI_PHY_1324	0F30 D4B0h
54B4h	32	EMIF_CTLCFG_DENALI_PHY_1325	0F30 D4B4h
54B8h	32	EMIF_CTLCFG_DENALI_PHY_1326	0F30 D4B8h
54BCh	32	EMIF_CTLCFG_DENALI_PHY_1327	0F30 D4BCh
54C0h	32	EMIF_CTLCFG_DENALI_PHY_1328	0F30 D4C0h
54C4h	32	EMIF_CTLCFG_DENALI_PHY_1329	0F30 D4C4h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
54C8h	32	EMIF_CTLCFG_DENALI_PHY_1330	0F30 D4C8h
54CCh	32	EMIF_CTLCFG_DENALI_PHY_1331	0F30 D4CCh
54D0h	32	EMIF_CTLCFG_DENALI_PHY_1332	0F30 D4D0h
54D4h	32	EMIF_CTLCFG_DENALI_PHY_1333	0F30 D4D4h
54D8h	32	EMIF_CTLCFG_DENALI_PHY_1334	0F30 D4D8h
54DCh	32	EMIF_CTLCFG_DENALI_PHY_1335	0F30 D4DCh
54E0h	32	EMIF_CTLCFG_DENALI_PHY_1336	0F30 D4E0h
54E4h	32	EMIF_CTLCFG_DENALI_PHY_1337	0F30 D4E4h
54E8h	32	EMIF_CTLCFG_DENALI_PHY_1338	0F30 D4E8h
54ECh	32	EMIF_CTLCFG_DENALI_PHY_1339	0F30 D4ECh
54F0h	32	EMIF_CTLCFG_DENALI_PHY_1340	0F30 D4F0h
54F4h	32	EMIF_CTLCFG_DENALI_PHY_1341	0F30 D4F4h
54F8h	32	EMIF_CTLCFG_DENALI_PHY_1342	0F30 D4F8h
54FCh	32	EMIF_CTLCFG_DENALI_PHY_1343	0F30 D4FCh
5500h	32	EMIF_CTLCFG_DENALI_PHY_1344	0F30 D500h
5504h	32	EMIF_CTLCFG_DENALI_PHY_1345	0F30 D504h
5508h	32	EMIF_CTLCFG_DENALI_PHY_1346	0F30 D508h
550Ch	32	EMIF_CTLCFG_DENALI_PHY_1347	0F30 D50Ch
5510h	32	EMIF_CTLCFG_DENALI_PHY_1348	0F30 D510h
5514h	32	EMIF_CTLCFG_DENALI_PHY_1349	0F30 D514h
5518h	32	EMIF_CTLCFG_DENALI_PHY_1350	0F30 D518h
551Ch	32	EMIF_CTLCFG_DENALI_PHY_1351	0F30 D51Ch
5520h	32	EMIF_CTLCFG_DENALI_PHY_1352	0F30 D520h
5524h	32	EMIF_CTLCFG_DENALI_PHY_1353	0F30 D524h
5528h	32	EMIF_CTLCFG_DENALI_PHY_1354	0F30 D528h
552Ch	32	EMIF_CTLCFG_DENALI_PHY_1355	0F30 D52Ch
5530h	32	EMIF_CTLCFG_DENALI_PHY_1356	0F30 D530h
5534h	32	EMIF_CTLCFG_DENALI_PHY_1357	0F30 D534h
5538h	32	EMIF_CTLCFG_DENALI_PHY_1358	0F30 D538h
553Ch	32	EMIF_CTLCFG_DENALI_PHY_1359	0F30 D53Ch
5540h	32	EMIF_CTLCFG_DENALI_PHY_1360	0F30 D540h
5544h	32	EMIF_CTLCFG_DENALI_PHY_1361	0F30 D544h
5548h	32	EMIF_CTLCFG_DENALI_PHY_1362	0F30 D548h
554Ch	32	EMIF_CTLCFG_DENALI_PHY_1363	0F30 D54Ch
5550h	32	EMIF_CTLCFG_DENALI_PHY_1364	0F30 D550h
5554h	32	EMIF_CTLCFG_DENALI_PHY_1365	0F30 D554h
5558h	32	EMIF_CTLCFG_DENALI_PHY_1366	0F30 D558h
555Ch	32	EMIF_CTLCFG_DENALI_PHY_1367	0F30 D55Ch
5560h	32	EMIF_CTLCFG_DENALI_PHY_1368	0F30 D560h
5564h	32	EMIF_CTLCFG_DENALI_PHY_1369	0F30 D564h
5568h	32	EMIF_CTLCFG_DENALI_PHY_1370	0F30 D568h
556Ch	32	EMIF_CTLCFG_DENALI_PHY_1371	0F30 D56Ch
5570h	32	EMIF_CTLCFG_DENALI_PHY_1372	0F30 D570h
5574h	32	EMIF_CTLCFG_DENALI_PHY_1373	0F30 D574h
5578h	32	EMIF_CTLCFG_DENALI_PHY_1374	0F30 D578h

Table 14-12357. EMIF_CTLCFG Registers, Base Address=0F30 8000h, Length=32768 (continued)

Offset	Length	Register Name	DDR16SS0 Physical Address
557Ch	32	EMIF_CTLCFG_DENALI_PHY_1375	0F30 D57Ch
5580h	32	EMIF_CTLCFG_DENALI_PHY_1376	0F30 D580h
5584h	32	EMIF_CTLCFG_DENALI_PHY_1377	0F30 D584h
5588h	32	EMIF_CTLCFG_DENALI_PHY_1378	0F30 D588h
558Ch	32	EMIF_CTLCFG_DENALI_PHY_1379	0F30 D58Ch
5590h	32	EMIF_CTLCFG_DENALI_PHY_1380	0F30 D590h
5594h	32	EMIF_CTLCFG_DENALI_PHY_1381	0F30 D594h
5598h	32	EMIF_CTLCFG_DENALI_PHY_1382	0F30 D598h
559Ch	32	EMIF_CTLCFG_DENALI_PHY_1383	0F30 D59Ch
55A0h	32	EMIF_CTLCFG_DENALI_PHY_1384	0F30 D5A0h
55A4h	32	EMIF_CTLCFG_DENALI_PHY_1385	0F30 D5A4h
55A8h	32	EMIF_CTLCFG_DENALI_PHY_1386	0F30 D5A8h
55ACh	32	EMIF_CTLCFG_DENALI_PHY_1387	0F30 D5ACh
55B0h	32	EMIF_CTLCFG_DENALI_PHY_1388	0F30 D5B0h
55B4h	32	EMIF_CTLCFG_DENALI_PHY_1389	0F30 D5B4h
55B8h	32	EMIF_CTLCFG_DENALI_PHY_1390	0F30 D5B8h
55BCh	32	EMIF_CTLCFG_DENALI_PHY_1391	0F30 D5BCh
55C0h	32	EMIF_CTLCFG_DENALI_PHY_1392	0F30 D5C0h
55C4h	32	EMIF_CTLCFG_DENALI_PHY_1393	0F30 D5C4h
55C8h	32	EMIF_CTLCFG_DENALI_PHY_1394	0F30 D5C8h
55CCh	32	EMIF_CTLCFG_DENALI_PHY_1395	0F30 D5CCh
55D0h	32	EMIF_CTLCFG_DENALI_PHY_1396	0F30 D5D0h
55D4h	32	EMIF_CTLCFG_DENALI_PHY_1397	0F30 D5D4h
55D8h	32	EMIF_CTLCFG_DENALI_PHY_1398	0F30 D5D8h
55DCh	32	EMIF_CTLCFG_DENALI_PHY_1399	0F30 D5DCh
55E0h	32	EMIF_CTLCFG_DENALI_PHY_1400	0F30 D5E0h
55E4h	32	EMIF_CTLCFG_DENALI_PHY_1401	0F30 D5E4h
55E8h	32	EMIF_CTLCFG_DENALI_PHY_1402	0F30 D5E8h
55ECh	32	EMIF_CTLCFG_DENALI_PHY_1403	0F30 D5ECh
55F0h	32	EMIF_CTLCFG_DENALI_PHY_1404	0F30 D5F0h
55F4h	32	EMIF_CTLCFG_DENALI_PHY_1405	0F30 D5F4h

14.5.1.2 ddr16ss Registers

ddr16ss Registers

14.5.1.2.1 EMIF_SSCFG_SS_ID_REV_REG Register

1 EMIF_SSCFG_SS_ID_REV_REG Register (Offset = 0h) [reset = 68034900h]

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem.

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Table 14-12358. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0000h**

Figure 14-4080. EMIF_SSCFG_SS_ID_REV_REG Name Register

31	30	29	28	27	26	25	24
MOD_ID							
R							
6803h							
23	22	21	20	19	18	17	16
MOD_ID							
R							
6803h							
15	14	13	12	11	10	9	8
RTL_VER					MAJ_REV		
R					R		
9h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MIN_REV					
R		R					
0h		0h					

Table 14-12360. EMIF_SSCFG_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MOD_ID	R	6803h	Module ID Reset Source: ctl_smod_g_rst_n
15:11	RTL_VER	R	9h	RTL version Reset Source: ctl_smod_g_rst_n
10:8	MAJ_REV	R	1h	Major revision Reset Source: ctl_smod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: ctl_smod_g_rst_n
5:0	MIN_REV	R	0h	Minor revision Reset Source: ctl_smod_g_rst_n

14.5.1.2.2 EMIF_SSCFG_SS_CTL_REG Register

1 EMIF_SSCFG_SS_CTL_REG Register (Offset = 4h) [reset = 0h]

The Subsystem Control Register contains fields for control functions required for submodules in the subsystem.

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Table 14-12361. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0004h**

Figure 14-4081. EMIF_SSCFG_SS_CTL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_PLL_BYPASS
NONE							R/W
0h							0h

Table 14-12363. EMIF_SSCFG_SS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_PLL_BYPASS	R/W	0h	Cadence PHY De-Skew PLL bypass. Write 1 to bypass PLL. Reset Source: ctl_smod_g_rst_n

14.5.1.2.3 EMIF_SSCFG_V2A_CTL_REG Register

1 EMIF_SSCFG_V2A_CTL_REG Register (Offset = 20h) [reset = 231h]

The VBUSM2AXI Control register contains control functions required for the VBUSM2AXI submodule.

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Table 14-12364. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0020h**

Figure 14-4082. EMIF_SSCFG_V2A_CTL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED					SDRAM_3QT	SDRAM_IDX	
NONE					R/W	R/W	
0h					0h	11h	

7	6	5	4	3	2	1	0
SDRAM_IDX			REGION_IDX				
R/W			R/W				
11h			11h				

Table 14-12366. EMIF_SSCFG_V2A_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	SDRAM_3QT	R/W	0h	Setting this field to a 1 will modify SDRAM Index to be 3/4 its programmed value to support 3, 6, 12 and 24 GB sizes. Reset Source: ctl_smod_g_rst_n
9:5	SDRAM_IDX	R/W	11h	SDRAM Index = log2(connected SDRAM size) - 16. The sdram_idx describes the number of address bits minus 16 that are used to determine the mask used to detect memory rollover and prevent aliasing and false coherency issues. Max size supported is 8GB. A programmed value greater than 0x11 will result in this field being reset to 0x11. Reset Source: ctl_smod_g_rst_n
4:0	REGION_IDX	R/W	11h	Region Index = log2(CBA region size) - 16. The region_idx describes the number of address bits minus 16 that are used to determine the mask used to detect memory rollover and prevent aliasing and false coherency issues. Max size supported is 8GB. A programmed value greater than 0x11 will result in this field being reset to 0x11. Reset Source: ctl_smod_g_rst_n

14.5.1.2.4 EMIF_SSCFG_V2A_R1_MAT_REG Register

1 EMIF_SSCFG_V2A_R1_MAT_REG Register (Offset = 24h) [reset = 0h]

The Range 1 Match Register allows a single controller to a range of controllers to change their priority mapping. This allows selective controllers to be increased or decreased in effective priority. Range 1 Match Register uses the associated Range 1 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

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Table 14-12367. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0024h**

Figure 14-4083. EMIF_SSCFG_V2A_R1_MAT_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RANGE1_RANGEEN_A</td><td colspan="3">RANGE1_MASK_A</td><td colspan="4">RANGE1_ROUTEID_A</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RANGE1_ROUTEID_A</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RANGE1_RANGEEN_B</td><td colspan="3">RANGE1_MASK_B</td><td colspan="4">RANGE1_ROUTEID_B</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RANGE1_ROUTEID_B</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12369. EMIF_SSCFG_V2A_R1_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE1_RANGEEN_A	R/W	0h	The range1_rangeen_a enables the RouteID AND'd with range1_mask_a to match the range1_routeid_a Reset Source: ctl_smod_g_rst_n
30:28	RANGE1_MASK_A	R/W	0h	The range1_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a Reset Source: ctl_smod_g_rst_n
27:16	RANGE1_ROUTEID_A	R/W	0h	The range1_routeid_a is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n
15	RANGE1_RANGEEN_B	R/W	0h	The range1_rangeen_b enables the RouteID AND'd with range1_mask_b to match the range1_routeid_b Reset Source: ctl_smod_g_rst_n
14:12	RANGE1_MASK_B	R/W	0h	The range1_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b Reset Source: ctl_smod_g_rst_n

Table 14-12369. EMIF_SSCFG_V2A_R1_MAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	RANGE1_ROUTEID_B	R/W	0h	The range1_routeid_b is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n

14.5.1.2.5 EMIF_SSCFG_V2A_R2_MAT_REG Register

1 EMIF_SSCFG_V2A_R2_MAT_REG Register (Offset = 28h) [reset = 0h]

The Range 2 Match Register allows a single controller to a range of controllers to change their priority mapping. This allows selective controllers to be increased or decreased in effective priority. Range 2 Match Register uses the associated Range 2 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

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Table 14-12370. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0028h**

Figure 14-4084. EMIF_SSCFG_V2A_R2_MAT_REG Name Register

31	30	29	28	27	26	25	24
RANGE2_RANGEEN_A	RANGE2_MASK_A			RANGE2_ROUTEID_A			
R/W	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
RANGE2_ROUTEID_A							
R/W							
0h							
15	14	13	12	11	10	9	8
RANGE2_RANGEEN_B	RANGE2_MASK_B			RANGE2_ROUTEID_B			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
RANGE2_ROUTEID_B							
R/W							
0h							

Table 14-12372. EMIF_SSCFG_V2A_R2_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE2_RANGEEN_A	R/W	0h	The range2_rangeen_a enables the RouteID AND'd with range2_mask_a to match the range2_routeid_a Reset Source: ctl_smod_g_rst_n
30:28	RANGE2_MASK_A	R/W	0h	The range2_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a Reset Source: ctl_smod_g_rst_n
27:16	RANGE2_ROUTEID_A	R/W	0h	The range2_routeid_a is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n
15	RANGE2_RANGEEN_B	R/W	0h	The range2_rangeen_b enables the RouteID AND'd with range2_mask_b to match the range2_routeid_b Reset Source: ctl_smod_g_rst_n
14:12	RANGE2_MASK_B	R/W	0h	The range2_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b Reset Source: ctl_smod_g_rst_n

Table 14-12372. EMIF_SSCFG_V2A_R2_MAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	RANGE2_ROUTEID_B	R/W	0h	The range2_routeid_b is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n

14.5.1.2.6 EMIF_SSCFG_V2A_R3_MAT_REG Register

1 EMIF_SSCFG_V2A_R3_MAT_REG Register (Offset = 2Ch) [reset = 0h]

The Range 3 Match Register allows a single controller to a range of controllers to change their priority mapping. This allows selective controllers to be increased or decreased in effective priority. Range 3 Match Register uses the associated Range 3 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

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Table 14-12373. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 002Ch**

Figure 14-4085. EMIF_SSCFG_V2A_R3_MAT_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RANGE3_RANGEEN_A</td><td colspan="3">RANGE3_MASK_A</td><td colspan="4">RANGE3_ROUTEID_A</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RANGE3_ROUTEID_A</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RANGE3_RANGEEN_B</td><td colspan="3">RANGE3_MASK_B</td><td colspan="4">RANGE3_ROUTEID_B</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RANGE3_ROUTEID_B</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12375. EMIF_SSCFG_V2A_R3_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE3_RANGEEN_A	R/W	0h	The range3_rangeen_a enables the RouteID AND'd with range3_mask_a to match the range3_routeid_a Reset Source: ctl_smod_g_rst_n
30:28	RANGE3_MASK_A	R/W	0h	The range3_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a Reset Source: ctl_smod_g_rst_n
27:16	RANGE3_ROUTEID_A	R/W	0h	The range3_routeid_a is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n
15	RANGE3_RANGEEN_B	R/W	0h	The range3_rangeen_b enables the RouteID AND'd with range3_mask_b to match the range3_routeid_b Reset Source: ctl_smod_g_rst_n
14:12	RANGE3_MASK_B	R/W	0h	The range3_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b Reset Source: ctl_smod_g_rst_n

Table 14-12375. EMIF_SSCFG_V2A_R3_MAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	RANGE3_ROUTEID_B	R/W	0h	The range3_routeid_b is the value that is compared to the RouteID arriving on the command interface Reset Source: ctl_smod_g_rst_n

14.5.1.2.7 EMIF_SSCFG_V2A_DEF_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_DEF_PRI_MAP_REG Register (Offset = 30h) [reset = 0h]

The Default Priority Mapping Register is the default map for the inbound VBUSM priority to AXI priority.

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Table 14-12376. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0030h**

Figure 14-4086. EMIF_SSCFG_V2A_DEF_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIMAP0			RESERVED	PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	PRIMAP2			RESERVED	PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	PRIMAP4			RESERVED	PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	PRIMAP6			RESERVED	PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-12378. EMIF_SSCFG_V2A_DEF_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-12378. EMIF_SSCFG_V2A_DEF_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.5.1.2.8 EMIF_SSCFG_V2A_R1_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_R1_PRI_MAP_REG Register (Offset = 34h) [reset = 0h]

The Range 1 Priority Mapping Register is used to map the inbound VBUSM priority to AXI priority when a RouteID match 1 occurs. This allows the priority level to be changed from the Default Priority Mapping value.

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Table 14-12379. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 0034h

Figure 14-4087. EMIF_SSCFG_V2A_R1_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RANGE1_PRIMAP0			RESERVED	RANGE1_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	RANGE1_PRIMAP2			RESERVED	RANGE1_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	RANGE1_PRIMAP4			RESERVED	RANGE1_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	RANGE1_PRIMAP6			RESERVED	RANGE1_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-12381. EMIF_SSCFG_V2A_R1_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	RANGE1_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	RANGE1_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	RANGE1_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	RANGE1_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-12381. EMIF_SSCFG_V2A_R1_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	RANGE1_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	RANGE1_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	RANGE1_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RANGE1_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 1. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.5.1.2.9 EMIF_SSCFG_V2A_R2_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_R2_PRI_MAP_REG Register (Offset = 38h) [reset = 0h]

The Range 2 Priority Mapping Register is used to map the inbound VBUSM priority to AXI priority when a RouteID match 2 occurs. This allows the priority level to be changed from the Default Priority Mapping value.

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Table 14-12382. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0038h**

Figure 14-4088. EMIF_SSCFG_V2A_R2_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RANGE2_PRIMAP0			RESERVED	RANGE2_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	RANGE2_PRIMAP2			RESERVED	RANGE2_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	RANGE2_PRIMAP4			RESERVED	RANGE2_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	RANGE2_PRIMAP6			RESERVED	RANGE2_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-12384. EMIF_SSCFG_V2A_R2_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	RANGE2_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	RANGE2_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	RANGE2_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	RANGE2_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-12384. EMIF_SSCFG_V2A_R2_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	RANGE2_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	RANGE2_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	RANGE2_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RANGE2_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 2. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.5.1.2.10 EMIF_SSCFG_V2A_R3_PRI_MAP_REG Register

1 EMIF_SSCFG_V2A_R3_PRI_MAP_REG Register (Offset = 3Ch) [reset = 0h]

The Range 3 Priority Mapping Register is used to map the inbound VBUSM priority to AXI priority when a RouteID match 3 occurs. This allows the priority level to be changed from the Default Priority Mapping value.

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Table 14-12385. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 003Ch**

Figure 14-4089. EMIF_SSCFG_V2A_R3_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RANGE3_PRIMAP0			RESERVED	RANGE3_PRIMAP1		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	RANGE3_PRIMAP2			RESERVED	RANGE3_PRIMAP3		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	RANGE3_PRIMAP4			RESERVED	RANGE3_PRIMAP5		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	RANGE3_PRIMAP6			RESERVED	RANGE3_PRIMAP7		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-12387. EMIF_SSCFG_V2A_R3_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	RANGE3_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM priority 0 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
27	RESERVED	NONE	0h	Reserved
26:24	RANGE3_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM priority 1 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:20	RANGE3_PRIMAP2	R/W	0h	The field contains AXI priority value for VBUSM priority 2 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	RANGE3_PRIMAP3	R/W	0h	The field contains AXI priority value for VBUSM priority 3 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-12387. EMIF_SSCFG_V2A_R3_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	RANGE3_PRIMAP4	R/W	0h	The field contains AXI priority value for VBUSM priority 4 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
11	RESERVED	NONE	0h	Reserved
10:8	RANGE3_PRIMAP5	R/W	0h	The field contains AXI priority value for VBUSM priority 5 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:4	RANGE3_PRIMAP6	R/W	0h	The field contains AXI priority value for VBUSM priority 6 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2:0	RANGE3_PRIMAP7	R/W	0h	The field contains AXI priority value for VBUSM priority 7 for range match 3. 0=highest priority. 7=lowest priority Reset Source: ctl_smod_g_rst_n

14.5.1.2.11 EMIF_SSCFG_V2A_AERR_LOG1_REG Register

1 EMIF_SSCFG_V2A_AERR_LOG1_REG Register (Offset = 70h) [reset = 0h]

The Address Error Log 1 register displays the RouteID and lsb of the address for the first VBUSM command that was outside the programmed addressing range. Writing a 0x1 will clear all fields. Writing any other value has no effect. The Address Error Log 2 register will also be cleared upon writing this register.

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Table 14-12388. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0070h**

Figure 14-4090. EMIF_SSCFG_V2A_AERR_LOG1_REG Name Register

31	30	29	28	27	26	25	24
AERR_ADDR_LSB							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
AERR_ADDR_LSB							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
RESERVED				AERR_ROUTE_ID			
NONE				R/W1TC			
0h				0h			
7	6	5	4	3	2	1	0
AERR_ROUTE_ID							
R/W1TC							
0h							

Table 14-12390. EMIF_SSCFG_V2A_AERR_LOG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	AERR_ADDR_LSB	R/W1TC	0h	Address[15:0] of the VBUSM command Reset Source: ctl_smod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	AERR_ROUTE_ID	R/W1TC	0h	RouteID of the VBUSM write command Reset Source: ctl_smod_g_rst_n

14.5.1.2.12 EMIF_SSCFG_V2A_AERR_LOG2_REG Register

1 EMIF_SSCFG_V2A_AERR_LOG2_REG Register (Offset = 74h) [reset = 0h]

The Address Error Log 2 registers displays the msb of the address for the first VBUSM command that was outside the programmed addressing range. This register will be cleared upon writing the Address Error Log 1 register.

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Table 14-12391. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0074h**

Figure 14-4091. EMIF_SSCFG_V2A_AERR_LOG2_REG Name Register

31	30	29	28	27	26	25	24
AERR_ADDR_MSB							
R							
0h							
23	22	21	20	19	18	17	16
AERR_ADDR_MSB							
R							
0h							
15	14	13	12	11	10	9	8
AERR_ADDR_MSB							
R							
0h							
7	6	5	4	3	2	1	0
AERR_ADDR_MSB							
R							
0h							

Table 14-12393. EMIF_SSCFG_V2A_AERR_LOG2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AERR_ADDR_MSB	R	0h	Address[34:16] of the VBUSM command Reset Source: ctl_smod_g_rst_n

14.5.1.2.13 EMIF_SSCFG_V2A_BUS_TO Register

1 EMIF_SSCFG_V2A_BUS_TO Register (Offset = 9Ch) [reset = FFFFFFh]

VBUSM2AXI Bus Timeout Register

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Table 14-12394. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 009Ch**

Figure 14-4092. EMIF_SSCFG_V2A_BUS_TO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
BUS_TIMER							
R/W							
FFFFFFh							
15	14	13	12	11	10	9	8
BUS_TIMER							
R/W							
FFFFFFh							
7	6	5	4	3	2	1	0
BUS_TIMER							
R/W							
FFFFFFh							

Table 14-12396. EMIF_SSCFG_V2A_BUS_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	BUS_TIMER	R/W	FFFFFFh	AXI bus timeout value. Number of DDR clock cycles after which the VBUSM2AXI bridge times out if a hang on the controller AXI interface is detected. A value of N will be equal to N x 16 clocks. Writing a 0 will disable the timeout feature. Reset Source: ctl_smod_g_rst_n

14.5.1.2.14 EMIF_SSCFG_V2A_INT_RAW_REG Register

1 EMIF_SSCFG_V2A_INT_RAW_REG Register (Offset = A0h) [reset = 0h]

VBUSM2AXI Interrupt Raw Status Register

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Table 14-12397. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 00A0h**

Figure 14-4093. EMIF_SSCFG_V2A_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR	ECC2BERR	ECC1BERR	TOERR	AERR	RESERVED
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	NONE
0h		0h	0h	0h	0h	0h	0h

Table 14-12399. EMIF_SSCFG_V2A_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ECCM1BERR	R/W1TS	0h	Raw status of SDRAM ECC multi 1-bit errors in same SDRAM burst. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
4	ECC2BERR	R/W1TS	0h	Raw status of SDRAM ECC 2-bit error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
3	ECC1BERR	R/W1TS	0h	Raw status of SDRAM ECC 1-bit error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
2	TOERR	R/W1TS	0h	Raw status of VBUSM2AXI interrupt for controller AXI interface timeout. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
1	AERR	R/W1TS	0h	Raw status of VBUSM2AXI interrupt for VBUSM address outside the programmed range. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
0	RESERVED	NONE	0h	Reserved

14.5.1.2.15 EMIF_SSCFG_V2A_INT_STAT_REG Register

1 EMIF_SSCFG_V2A_INT_STAT_REG Register (Offset = A4h) [reset = 0h]

VBUSM2AXI Interrupt Status Register

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Table 14-12400. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 00A4h

Figure 14-4094. EMIF_SSCFG_V2A_INT_STAT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR	ECC2BERR	ECC1BERR	TOERR	AERR	RESERVED
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE
0h		0h	0h	0h	0h	0h	0h

Table 14-12402. EMIF_SSCFG_V2A_INT_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ECCM1BERR	R/W1TC	0h	Enabled status of SDRAM ECC multi 1-bit errors in same SDRAM burst. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
4	ECC2BERR	R/W1TC	0h	Enabled status of SDRAM ECC 2-bit error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
3	ECC1BERR	R/W1TC	0h	Enabled status of SDRAM ECC 1-bit error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
2	TOERR	R/W1TC	0h	Enabled status of VBUSM2AXI interrupt for controller AXI interface timeout. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n

Table 14-12402. EMIF_SSCFG_V2A_INT_STAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR	R/W1TC	0h	Enabled status of VBUSM2AXI interrupt for VBUSM address outside the programmed range. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
0	RESERVED	NONE	0h	Reserved

14.5.1.2.16 EMIF_SSCFG_V2A_INT_SET_REG Register

1 EMIF_SSCFG_V2A_INT_SET_REG Register (Offset = A8h) [reset = 0h]

VBUSM2AXI Interrupt Enable Set Register

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Table 14-12403. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 00A8h**

Figure 14-4095. EMIF_SSCFG_V2A_INT_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR_EN	ECC2BERR_EN	ECC1BERR_EN	TOERR_EN	AERR_EN	RESERVED
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	NONE
0h		0h	0h	0h	0h	0h	0h

Table 14-12405. EMIF_SSCFG_V2A_INT_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ECCM1BERR_EN	R/W1TS	0h	Enable set for SDRAM ECC multi 1-bit errors in same SDRAM burst. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
4	ECC2BERR_EN	R/W1TS	0h	Enable set for SDRAM ECC 2-bit error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
3	ECC1BERR_EN	R/W1TS	0h	Enable set for SDRAM ECC 1-bit error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
2	TOERR_EN	R/W1TS	0h	Enable set for VBUSM2AXI interrupt for controller AXI interface timeout. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n

Table 14-12405. EMIF_SSCFG_V2A_INT_SET_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR_EN	R/W1TS	0h	Enable set for VBUSM2AXI interrupt for VBUSM address outside the programmed range. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
0	RESERVED	NONE	0h	Reserved

14.5.1.2.17 EMIF_SSCFG_V2A_INT_CLR_REG Register

1 EMIF_SSCFG_V2A_INT_CLR_REG Register (Offset = ACh) [reset = 0h]

VBUSM2AXI Interrupt Enable Clear Register

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Table 14-12406. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 00ACh**

Figure 14-4096. EMIF_SSCFG_V2A_INT_CLR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		ECCM1BERR_EN	ECC2BERR_EN	ECC1BERR_EN	TOERR_EN	AERR_EN	RESERVED
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE
0h		0h	0h	0h	0h	0h	0h

Table 14-12408. EMIF_SSCFG_V2A_INT_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	ECCM1BERR_EN	R/W1TC	0h	Enable clear for SDRAM ECC multi 1-bit errors in same SDRAM burst. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
4	ECC2BERR_EN	R/W1TC	0h	Enable clear for SDRAM ECC 2-bit error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
3	ECC1BERR_EN	R/W1TC	0h	Enable clear for SDRAM ECC 1-bit error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
2	TOERR_EN	R/W1TC	0h	Enable clear for VBUSM2AXI interrupt for controller AXI interface timeout. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n

Table 14-12408. EMIF_SSCFG_V2A_INT_CLR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR_EN	R/W1TC	0h	Enable clear for VBUSM2AXI interrupt for VBUSM address outside the programmed range. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect. Reset Source: ctl_smod_g_rst_n
0	RESERVED	NONE	0h	Reserved

14.5.1.2.18 EMIF_SSCFG_V2A_EOI_REG Register

1 EMIF_SSCFG_V2A_EOI_REG Register (Offset = B0h) [reset = 0h]

VBUSM2AXI End of Interrupt Register

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Table 14-12409. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 00B0h**

Figure 14-4097. EMIF_SSCFG_V2A_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EOI	
NONE						W	
0h						0h	

Table 14-12411. EMIF_SSCFG_V2A_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	EOI	W	0h	Software End Of Interrupt (EOI) control. Write 0 for aerr/toerr interrupt. Write 1 for ecc1b interrupt. Write 2 for ecc2b interrupt. This field always reads 0 (no EOI memory). Reset Source: ctl_smod_g_rst_n

14.5.1.2.19 EMIF_SSCFG_PERF_CNT_SEL_REG Register

1 EMIF_SSCFG_PERF_CNT_SEL_REG Register (Offset = 100h) [reset = 3020100h]

The Performance Counter Select register is used to select the statistic type to be counted in the corresponding Performance Counter register.

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Table 14-12412. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0100h**

Figure 14-4098. EMIF_SSCFG_PERF_CNT_SEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		CNT4_SEL					
NONE		R/W					
0h		3h					
23	22	21	20	19	18	17	16
RESERVED		CNT3_SEL					
NONE		R/W					
0h		2h					
15	14	13	12	11	10	9	8
RESERVED		CNT2_SEL					
NONE		R/W					
0h		1h					
7	6	5	4	3	2	1	0
RESERVED		CNT1_SEL					
NONE		R/W					
0h		0h					

Table 14-12414. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved

Table 14-12414. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29:24	CNT4_SEL	R/W	3h	Statistic select for Performance Counter 4 register. 0x0 = Counts every Write command. 0x1 = Counts every Read command. 0x2 = Counts every read as a result of a RMW command. 0x3 = Counts every Activate command. 0x4 = Counts every Precharge command. 0x5 = Counts every Precharge All command. 0x6 = Counts every Mode Register Read command. 0x7 = Counts every Mode Register Write command. 0x8 = Counts every Per Bank Refresh command. 0x9 = Counts every Auto Refresh command. 0xA = Counts every ZQ Calib Long command. 0xB = Counts every ZQ Calib Short command. 0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around. 0xD = Counts every Write-to-Write address collision. 0xE = Counts every Write-to-Read address collision. 0xF = Counts every Read-to-Write address collision. 0x10 = Counts every Read-to-Read address collision. 0x11 = Counts every exit from Power-Down Self-Refresh mode. 0x12 = Counts every entry into Power-Down Self-Refresh mode. 0x13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode. 0x14 = Counts every exit from Power-Down mode. 0x15 = Counts every entry into Power-Down mode. 0x16 = Counts every cycle for which the DDR Controller stays in Power-Down mode. 0x17 = Counts every exit from Self-Refresh mode. 0x18 = Counts every entry into Self-Refresh mode. 0x19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode. 0x1A = Reserved 0x1B = Reserved 0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x24-0x2F = Reserved Reset Source: ctl_smod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-12414. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:16	CNT3_SEL	R/W	2h	Statistic select for Performance Counter 3 register. 0x0 = Counts every Write command. 0x1 = Counts every Read command. 0x2 = Counts every read as a result of a RMW command. 0x3 = Counts every Activate command. 0x4 = Counts every Precharge command. 0x5 = Counts every Precharge All command. 0x6 = Counts every Mode Register Read command. 0x7 = Counts every Mode Register Write command. 0x8 = Counts every Per Bank Refresh command. 0x9 = Counts every Auto Refresh command. 0xA = Counts every ZQ Calib Long command. 0xB = Counts every ZQ Calib Short command. 0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around. 0xD = Counts every Write-to-Write address collision. 0xE = Counts every Write-to-Read address collision. 0xF = Counts every Read-to-Write address collision. 0x10 = Counts every Read-to-Read address collision. 0x11 = Counts every exit from Power-Down Self-Refresh mode. 0x12 = Counts every entry into Power-Down Self-Refresh mode. 0x13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode. 0x14 = Counts every exit from Power-Down mode. 0x15 = Counts every entry into Power-Down mode. 0x16 = Counts every cycle for which the DDR Controller stays in Power-Down mode. 0x17 = Counts every exit from Self-Refresh mode. 0x18 = Counts every entry into Self-Refresh mode. 0x19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode. 0x1A = Reserved 0x1B = Reserved 0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x24-0x2F = Reserved Reset Source: ctl_smod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-12414. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	CNT2_SEL	R/W	1h	Statistic select for Performance Counter 2 register. 0x0 = Counts every Write command. 0x1 = Counts every Read command. 0x2 = Counts every read as a result of a RMW command. 0x3 = Counts every Activate command. 0x4 = Counts every Precharge command. 0x5 = Counts every Precharge All command. 0x6 = Counts every Mode Register Read command. 0x7 = Counts every Mode Register Write command. 0x8 = Counts every Per Bank Refresh command. 0x9 = Counts every Auto Refresh command. 0xA = Counts every ZQ Calib Long command. 0xB = Counts every ZQ Calib Short command. 0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around. 0xD = Counts every Write-to-Write address collision. 0xE = Counts every Write-to-Read address collision. 0xF = Counts every Read-to-Write address collision. 0x10 = Counts every Read-to-Read address collision. 0x11 = Counts every exit from Power-Down Self-Refresh mode. 0x12 = Counts every entry into Power-Down Self-Refresh mode. 0x13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode. 0x14 = Counts every exit from Power-Down mode. 0x15 = Counts every entry into Power-Down mode. 0x16 = Counts every cycle for which the DDR Controller stays in Power-Down mode. 0x17 = Counts every exit from Self-Refresh mode. 0x18 = Counts every entry into Self-Refresh mode. 0x19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode. 0x1A = Reserved 0x1B = Reserved 0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x24-0x2F = Reserved Reset Source: ctl_smod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-12414. EMIF_SSCFG_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	CNT1_SEL	R/W	0h	Statistic select for Performance Counter 1 register. 0x0 = Counts every Write command. 0x1 = Counts every Read command. 0x2 = Counts every read as a result of a RMW command. 0x3 = Counts every Activate command. 0x4 = Counts every Precharge command. 0x5 = Counts every Precharge All command. 0x6 = Counts every Mode Register Read command. 0x7 = Counts every Mode Register Write command. 0x8 = Counts every Per Bank Refresh command. 0x9 = Counts every Auto Refresh command. 0xA = Counts every ZQ Calib Long command. 0xB = Counts every ZQ Calib Short command. 0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around. 0xD = Counts every Write-to-Write address collision. 0xE = Counts every Write-to-Read address collision. 0xF = Counts every Read-to-Write address collision. 0x10 = Counts every Read-to-Read address collision. 0x11 = Counts every exit from Power-Down Self-Refresh mode. 0x12 = Counts every entry into Power-Down Self-Refresh mode. 0x13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode. 0x14 = Counts every exit from Power-Down mode. 0x15 = Counts every entry into Power-Down mode. 0x16 = Counts every cycle for which the DDR Controller stays in Power-Down mode. 0x17 = Counts every exit from Self-Refresh mode. 0x18 = Counts every entry into Self-Refresh mode. 0x19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode. 0x1A = Reserved 0x1B = Reserved 0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x24-0x2F = Reserved Reset Source: ctl_smod_g_rst_n

14.5.1.2.20 EMIF_SSCFG_PERF_CNT1_REG Register

1 EMIF_SSCFG_PERF_CNT1_REG Register (Offset = 104h) [reset = 0h]

Performance Counter 1 Register

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Table 14-12415. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0104h**

Figure 14-4099. EMIF_SSCFG_PERF_CNT1_REG Name Register

31	30	29	28	27	26	25	24
CNT1							
R							
0h							
23	22	21	20	19	18	17	16
CNT1							
R							
0h							
15	14	13	12	11	10	9	8
CNT1							
R							
0h							
7	6	5	4	3	2	1	0
CNT1							
R							
0h							

Table 14-12417. EMIF_SSCFG_PERF_CNT1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNT1	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register. Reset Source: ctl_smod_g_rst_n

14.5.1.2.21 EMIF_SSCFG_PERF_CNT2_REG Register

1 EMIF_SSCFG_PERF_CNT2_REG Register (Offset = 108h) [reset = 0h]

Performance Counter 2 Register

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Table 14-12418. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0108h**

Figure 14-4100. EMIF_SSCFG_PERF_CNT2_REG Name Register

31	30	29	28	27	26	25	24
CNT2							
R							
0h							
23	22	21	20	19	18	17	16
CNT2							
R							
0h							
15	14	13	12	11	10	9	8
CNT2							
R							
0h							
7	6	5	4	3	2	1	0
CNT2							
R							
0h							

Table 14-12420. EMIF_SSCFG_PERF_CNT2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNT2	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register. Reset Source: ctl_smod_g_rst_n

14.5.1.2.22 EMIF_SSCFG_PERF_CNT3_REG Register

1 EMIF_SSCFG_PERF_CNT3_REG Register (Offset = 10Ch) [reset = 0h]

Performance Counter 3 Register

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Table 14-12421. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 010Ch**

Figure 14-4101. EMIF_SSCFG_PERF_CNT3_REG Name Register

31	30	29	28	27	26	25	24
CNT3							
R							
0h							
23	22	21	20	19	18	17	16
CNT3							
R							
0h							
15	14	13	12	11	10	9	8
CNT3							
R							
0h							
7	6	5	4	3	2	1	0
CNT3							
R							
0h							

Table 14-12423. EMIF_SSCFG_PERF_CNT3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNT3	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register. Reset Source: ctl_smod_g_rst_n

14.5.1.2.23 EMIF_SSCFG_PERF_CNT4_REG Register

1 EMIF_SSCFG_PERF_CNT4_REG Register (Offset = 110h) [reset = 0h]

Performance Counter 4 Register

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Table 14-12424. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 0110h

Figure 14-4102. EMIF_SSCFG_PERF_CNT4_REG Name Register

31	30	29	28	27	26	25	24
CNT4							
R							
0h							
23	22	21	20	19	18	17	16
CNT4							
R							
0h							
15	14	13	12	11	10	9	8
CNT4							
R							
0h							
7	6	5	4	3	2	1	0
CNT4							
R							
0h							

Table 14-12426. EMIF_SSCFG_PERF_CNT4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNT4	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register. Reset Source: ctl_smod_g_rst_n

14.5.1.2.24 EMIF_SSCFG_ECC_CTRL_REG Register

1 EMIF_SSCFG_ECC_CTRL_REG Register (Offset = 120h) [reset = 0h]

ECC Control Register

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Table 14-12427. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0120h**

Figure 14-4103. EMIF_SSCFG_ECC_CTRL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					COR_ECC_THRESH		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED			WR_ALLOC	RESERVED	ECC_CK	RMW_EN	ECC_EN
NONE			R/W	NONE	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-12429. EMIF_SSCFG_ECC_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	COR_ECC_THRESH	R/W	0h	Threshold for 1-bit ECC errors in multiple data words in an SDRAM burst that create an uncorrected error fault indication. Value of 0/1 means 2 or more 1-bit errors in multiple data words will result in an uncorrected error fault indication, value of 2 means 3 or more 1-bit errors will result in an uncorrected error fault indication, and so on. Value of 4 or greater disables this feature. This field must always be kept at default, and only changed for debug. Reset Source: ctl_smod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	WR_ALLOC	R/W	0h	When set to 1, an unassigned ECC cache-line will be allocated for a write with routeID that do not match any of the mapped routeID's. Reset Source: ctl_smod_g_rst_n
3	RESERVED	NONE	0h	Reserved
2	ECC_CK	R/W	0h	Set 1 to enable ECC verification for read accesses when ecc_en=1. The value of this field is ignored when ecc_en=0. This bit must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

Table 14-12429. EMIF_SSCFG_ECC_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RMW_EN	R/W	0h	Read modify write enable. Set 1 to enable RMW functionality for sub-quanta accesses when ecc_en=1. This bit must be set to 1 if ecc_en is set to a 1 to ensure subquanta accesses to DRAM do not result in ECC errors. This bit must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n
0	ECC_EN	R/W	0h	DRAM ECC enable. Setting a 1 causes ECC to be written to DRAM. This bit must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.5.1.2.25 EMIF_SSCFG_ECC_RID_INDX_REG Register

1 EMIF_SSCFG_ECC_RID_INDX_REG Register (Offset = 124h) [reset = 0h]

ECC Cache RouteID Index Register

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Table 14-12430. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0124h**

Figure 14-4104. EMIF_SSCFG_ECC_RID_INDX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		ECCRID_ADR					
NONE		R/W					
0h		0h					

Table 14-12432. EMIF_SSCFG_ECC_RID_INDX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	ECCRID_ADR	R/W	0h	This index specifies the ECC cache entry number that the eccrid_val is mapped to. Reset Source: ctl_smod_g_rst_n

14.5.1.2.26 EMIF_SSCFG_ECC_RID_VAL_REG Register

1 EMIF_SSCFG_ECC_RID_VAL_REG Register (Offset = 128h) [reset = 0h]

ECC Cache RouteID Write Value Register

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Table 14-12433. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0128h**

Figure 14-4105. EMIF_SSCFG_ECC_RID_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ECCRID_VAL_VLD	RESERVED			ECCRID_VAL			
R/W	NONE			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECCRID_VAL							
R/W							
0h							

Table 14-12435. EMIF_SSCFG_ECC_RID_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	ECCRID_VAL_VLD	R/W	0h	A 1 in this field indicates that value in eccrid_val is valid. Reset Source: ctl_smod_g_rst_n
14:12	RESERVED	NONE	0h	Reserved
11:0	ECCRID_VAL	R/W	0h	RouteID value written or read. Reset Source: ctl_smod_g_rst_n

14.5.1.2.27 EMIF_SSCFG_ECC_R0_STR_ADDR_REG Register

1 EMIF_SSCFG_ECC_R0_STR_ADDR_REG Register (Offset = 130h) [reset = FFFFh]

ECC Range 0 Start Address Register

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Table 14-12436. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0130h**

Figure 14-4106. EMIF_SSCFG_ECC_R0_STR_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECC_STR_ADR_0
NONE							R/W
0h							FFFFh
15	14	13	12	11	10	9	8
ECC_STR_ADR_0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
ECC_STR_ADR_0							
R/W							
FFFFh							

Table 14-12438. EMIF_SSCFG_ECC_R0_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	ECC_STR_ADR_0	R/W	FFFFh	Start caddress[31:16] for ECC range 0. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.5.1.2.28 EMIF_SSCFG_ECC_R0_END_ADDR_REG Register

1 EMIF_SSCFG_ECC_R0_END_ADDR_REG Register (Offset = 134h) [reset = 0h]

ECC Range 0 End Address Register

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Table 14-12439. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0134h**

Figure 14-4107. EMIF_SSCFG_ECC_R0_END_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECC_END_ADR_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
ECC_END_ADR_0							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_END_ADR_0							
R/W							
0h							

Table 14-12441. EMIF_SSCFG_ECC_R0_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	ECC_END_ADR_0	R/W	0h	End caddress[31:16] for ECC range 0. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.5.1.2.29 EMIF_SSCFG_ECC_R1_STR_ADDR_REG Register

1 EMIF_SSCFG_ECC_R1_STR_ADDR_REG Register (Offset = 138h) [reset = FFFFh]

ECC Range 1 Start Address Register

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Table 14-12442. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0138h**

Figure 14-4108. EMIF_SSCFG_ECC_R1_STR_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECC_STR_ADR_1
NONE							R/W
0h							FFFFh
15	14	13	12	11	10	9	8
ECC_STR_ADR_1							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
ECC_STR_ADR_1							
R/W							
FFFFh							

Table 14-12444. EMIF_SSCFG_ECC_R1_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	ECC_STR_ADR_1	R/W	FFFFh	Start caddress[31:16] for ECC range 1. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.5.1.2.30 EMIF_SSCFG_ECC_R1_END_ADDR_REG Register

1 EMIF_SSCFG_ECC_R1_END_ADDR_REG Register (Offset = 13Ch) [reset = 0h]

ECC Range 1 End Address Register

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Table 14-12445. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 013Ch**

Figure 14-4109. EMIF_SSCFG_ECC_R1_END_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECC_END_ADR_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
ECC_END_ADR_1							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_END_ADR_1							
R/W							
0h							

Table 14-12447. EMIF_SSCFG_ECC_R1_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	ECC_END_ADR_1	R/W	0h	End caddress[31:16] for ECC range 1. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.5.1.2.31 EMIF_SSCFG_ECC_R2_STR_ADDR_REG Register

1 EMIF_SSCFG_ECC_R2_STR_ADDR_REG Register (Offset = 140h) [reset = FFFFh]

ECC Range 2 Start Address Register

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Table 14-12448. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0140h**

Figure 14-4110. EMIF_SSCFG_ECC_R2_STR_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECC_STR_ADR_2
NONE							R/W
0h							FFFFh
15	14	13	12	11	10	9	8
ECC_STR_ADR_2							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
ECC_STR_ADR_2							
R/W							
FFFFh							

Table 14-12450. EMIF_SSCFG_ECC_R2_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	ECC_STR_ADR_2	R/W	FFFFh	Start caddress[31:16] for ECC range 2. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.5.1.2.32 EMIF_SSCFG_ECC_R2_END_ADDR_REG Register

1 EMIF_SSCFG_ECC_R2_END_ADDR_REG Register (Offset = 144h) [reset = 0h]

ECC Range 2 End Address Register

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Table 14-12451. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 0144h

Figure 14-4111. EMIF_SSCFG_ECC_R2_END_ADDR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ECC_END_ADR_2
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
ECC_END_ADR_2							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_END_ADR_2							
R/W							
0h							

Table 14-12453. EMIF_SSCFG_ECC_R2_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	ECC_END_ADR_2	R/W	0h	End caddress[31:16] for ECC range 2. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR. Reset Source: ctl_smod_g_rst_n

14.5.1.2.33 EMIF_SSCFG_ECC_1B_ERR_CNT_REG Register

1 EMIF_SSCFG_ECC_1B_ERR_CNT_REG Register (Offset = 150h) [reset = 0h]

ECC 1-Bit Error Count Register

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Table 14-12454. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 0150h

Figure 14-4112. EMIF_SSCFG_ECC_1B_ERR_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ECC_1B_ERR_CNT							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
ECC_1B_ERR_CNT							
R/W1TC							
0h							

Table 14-12456. EMIF_SSCFG_ECC_1B_ERR_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ECC_1B_ERR_CNT	R/W1TC	0h	16-bit counter that displays number of 1-bit ECC errors on SDRAM data. Writing a 0x1 will clear this count. Writing any other value has no effect. Reset Source: ctl_smod_g_rst_n

14.5.1.2.34 EMIF_SSCFG_ECC_1B_ERR_THRSH_REG Register

1 EMIF_SSCFG_ECC_1B_ERR_THRSH_REG Register (Offset = 154h) [reset = 0h]

ECC 1-Bit Error Threshold Register

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Table 14-12457. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0154h**

Figure 14-4113. EMIF_SSCFG_ECC_1B_ERR_THRSH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ECC_1B_ERR_THRSH							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_1B_ERR_THRSH							
R/W							
0h							

Table 14-12459. EMIF_SSCFG_ECC_1B_ERR_THRSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ECC_1B_ERR_THRSH	R/W	0h	ECC 1-bit error threshold. The bridge will generate an interrupt when the ECC 1-bit error count is equal to or greater than this threshold. A value of 0 will disable the generation of interrupt. Reset Source: ctl_smod_g_rst_n

14.5.1.2.35 EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG Register

1 EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG Register (Offset = 158h) [reset = 0h]

ECC 1-Bit Error Address Log Register

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Table 14-12460. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0158h**

Figure 14-4114. EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			ECC_1B_ERR_ADR				
NONE			R/W1TC				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ECC_1B_ERR_ADR							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ECC_1B_ERR_ADR							
R/W1TC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_1B_ERR_ADR							
R/W1TC							
0h							

Table 14-12462. EMIF_SSCFG_ECC_1B_ERR_ADR_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:0	ECC_1B_ERR_ADR	R/W1TC	0h	ECC 1-bit error address. 16-byte aligned address that had the 1-bit ECC error. This field displays the first address logged in the 2 deep logging FIFO. Writing a 0x1 will pop the top element of the FIFO. Writing any other value has no effect. Reset Source: ctl_smod_g_rst_n

14.5.1.2.36 EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG Register

1 EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG Register (Offset = 15Ch) [reset = 0h]

ECC 1-Bit Error Mask Log Register

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Table 14-12463. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 015Ch**

Figure 14-4115. EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECC_1B_ERR_MSK			
NONE				R			
0h				0h			

Table 14-12465. EMIF_SSCFG_ECC_1B_ERR_MSK_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ECC_1B_ERR_MSK	R	0h	ECC 1-bit error mask. Mask for the 32-byte data block that had the 1-bit ECC errors. Each bit represents an ECC quanta (8 bytes) in the 32-byte data block starting at address specified by ecc_1b_err_adr. Value of 1 on the bit represents an error in that particular 8 bytes. This field displays the first mask logged in the 2 deep logging FIFO along with the ecc_1b_err_adr. The same mechanism used to pop ecc_1b_err_adr is used to pop this field. Reset Source: ctl_smod_g_rst_n

14.5.1.2.37 EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG Register

1 EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG Register (Offset = 160h) [reset = 0h]

ECC 2-Bit Error Address Log Register

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Table 14-12466. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0160h**

Figure 14-4116. EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			ECC_2B_ERR_ADR				
NONE			R/W1TC				
0h			0h				
23	22	21	20	19	18	17	16
ECC_2B_ERR_ADR							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
ECC_2B_ERR_ADR							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
ECC_2B_ERR_ADR							
R/W1TC							
0h							

Table 14-12468. EMIF_SSCFG_ECC_2B_ERR_ADR_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:0	ECC_2B_ERR_ADR	R/W1TC	0h	ECC 2-bit error address. 16-byte aligned address that had the 2-bit ECC error. Writing a 0x1 will clear this field and the ecc_2b_err_msk field. Writing any other value has no effect. Reset Source: ctl_smod_g_rst_n

14.5.1.2.38 EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG Register

1 EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG Register (Offset = 164h) [reset = 0h]

ECC 2-Bit Error Mask Log Register

Return to Summary Table

Table 14-12469. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0164h**

Figure 14-4117. EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECC_2B_ERR_MSK			
NONE				R			
0h				0h			

Table 14-12471. EMIF_SSCFG_ECC_2B_ERR_MSK_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ECC_2B_ERR_MSK	R	0h	ECC 2-bit error mask. Mask for the 32-byte data block that had the 2-bit ECC errors. Each bit represents an ECC quanta (8 bytes) in the 32-byte data block starting at address specified by ecc_2b_err_adr. Value of 1 on the bit represents an error in that particular 8 bytes. Reset Source: ctl_smod_g_rst_n

14.5.1.2.39 EMIF_SSCFG_PHY_TEST_CTRL1_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL1_REG Register (Offset = 184h) [reset = FFFFFFC0h]

PHY Test Control 1 Register

Return to Summary Table

Table 14-12472. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0184h**

Figure 14-4118. EMIF_SSCFG_PHY_TEST_CTRL1_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_TSEL_RD_SEL							
R/W							
FFh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAOUT_TSEL_WR_SEL							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAG_DATAOUT_TSEL_ADDR_SEL							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAOUT_TSEL_ADDR_EN	JTAG_DATAOUT_TSEL_EN	JTAG_ENABLE_TERM	JTAG_ENABLE_OE	JTAG_ENABLE_IE	JTAG_ENABLE_DRIVE	JTAG_ENABLE	HVM_TEST_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	0h	0h	0h	0h	0h	0h

Table 14-12474. EMIF_SSCFG_PHY_TEST_CTRL1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	JTAG_DATAOUT_TSEL_RD_SEL	R/W	FFh	Controls jtag_dataout_tsel_rd_sel port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
23:16	JTAG_DATAOUT_TSEL_WR_SEL	R/W	FFh	Controls jtag_dataout_tsel_wr_sel port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
15:8	JTAG_DATAOUT_TSEL_ADDR_SEL	R/W	FFh	Controls jtag_dataout_tsel_addr_sel port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7	JTAG_DATAOUT_TSEL_ADDR_EN	R/W	1h	Controls jtag_dataout_tsel_addr_en port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAOUT_TSEL_EN	R/W	1h	Controls jtag_dataout_tsel_en port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5	JTAG_ENABLE_TERM	R/W	0h	Controls jtag_enable_term port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-12474. EMIF_SSCFG_PHY_TEST_CTRL1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	JTAG_ENABLE_OE	R/W	0h	Controls jtag_enable_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
3	JTAG_ENABLE_IE	R/W	0h	Controls jtag_enable_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
2	JTAG_ENABLE_DRIVE	R/W	0h	Controls jtag_enable_drive port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
1	JTAG_ENABLE	R/W	0h	Controls jtag_enable port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
0	HVM_TEST_EN	R/W	0h	1=Enable HVM test functionality. 0=Disable HVM test functionality. Setting a 1 will enable control of PHY ports using PHY Test Control registers, and will enable 50 MHz clock to the jtag_dataout_pad_dslice_io_cfg[1], jtag_dataout_pad_acs_io_cfg[1], and jtag_dataout_pad_adr_io_cfg[1] ports on the PHY. Reset Source: ctl_smod_g_rst_n

14.5.1.2.40 EMIF_SSCFG_PHY_TEST_CTRL2_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL2_REG Register (Offset = 188h) [reset = 215FC000h]

PHY Test Control 2 Register

Return to Summary Table

Table 14-12475. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0188h**

Figure 14-4119. EMIF_SSCFG_PHY_TEST_CTRL2_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_PAD_ADR_IO_CFG0	JTAG_DATAOUT_PAD_ACS_IO_CFG0	JTAG_DATAOUT_PAD_DSLICE_IO_CFG2	JTAG_DATAOUT_PAD_DSLICE_IO_CFG0	JTAG_DATAOUT_ATB_EN	JTAG_DATAOUT_VREF_CTRL_DQ		
R/W	R/W	R/W	R/W	R/W	R/W		
0h	0h	1h	0h	0h	2BFh		
23	22	21	20	19	18	17	16
JTAG_DATAOUT_VREF_CTRL_DQ							
R/W							
2BFh							
15	14	13	12	11	10	9	8
JTAG_DATAOUT_VREF_CTRL_DQ	JTAG_DATAOUT_PHY_RX_CAL_CODE						
R/W	R/W						
2BFh	100h						
7	6	5	4	3	2	1	0
JTAG_DATAOUT_PHY_RX_CAL_CODE		JTAG_DATAOUT_PHY_DSLICE_PAD_RX_CTLE_SETTING					
R/W		R/W					
100h		0h					

Table 14-12477. EMIF_SSCFG_PHY_TEST_CTRL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAOUT_PAD_ADR_IO_CFG0	R/W	0h	Controls jtag_dataout_pad_adr_io_cfg[0] port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAOUT_PAD_ACS_IO_CFG0	R/W	0h	Controls jtag_dataout_pad_acs_io_cfg[0] port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
29	JTAG_DATAOUT_PAD_DSLICE_IO_CFG2	R/W	1h	Controls jtag_dataout_pad_dslice_io_cfg[2] port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
28	JTAG_DATAOUT_PAD_DSLICE_IO_CFG0	R/W	0h	Controls jtag_dataout_pad_dslice_io_cfg[0] port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
27	JTAG_DATAOUT_ATB_EN	R/W	0h	Controls jtag_dataout_atb_en port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-12477. EMIF_SSCFG_PHY_TEST_CTRL2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:15	JTAG_DATAOUT_VREF_CTRL_DQ	R/W	2BFh	Controls jtag_dataout_vref_ctrl_dq port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
14:6	JTAG_DATAOUT_PHY_RX_CAL_CODE	R/W	100h	Controls jtag_dataout_phy_rx_cal_code port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5:0	JTAG_DATAOUT_PHY_DSLICE_PAD_RX_CTLE_SETTING	R/W	0h	Controls jtag_dataout_phy_dslice_pad_rx_ctle_setting port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.5.1.2.41 EMIF_SSCFG_PHY_TEST_CTRL3_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL3_REG Register (Offset = 18Ch) [reset = 0h]

PHY Test Control 3 Register

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Table 14-12478. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 018Ch**

Figure 14-4120. EMIF_SSCFG_PHY_TEST_CTRL3_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_ATB_CTRL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAOUT_ATB_CTRL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAG_DATAOUT_PAD_ATB_CTRL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAOUT_PAD_ATB_CTRL							
R/W							
0h							

Table 14-12480. EMIF_SSCFG_PHY_TEST_CTRL3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	JTAG_DATAOUT_ATB_CTRL	R/W	0h	Controls jtag_dataout_atb_ctrl port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
15:0	JTAG_DATAOUT_PAD_ATB_CTRL	R/W	0h	Controls jtag_dataout_pad_atb_ctrl port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.5.1.2.42 EMIF_SSCFG_PHY_TEST_CTRL4_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL4_REG Register (Offset = 190h) [reset = 0h]

PHY Test Control 4 Register

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Table 14-12481. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0190h**

Figure 14-4121. EMIF_SSCFG_PHY_TEST_CTRL4_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_ERROR_N_OE	JTAG_DATAOUT_PARITY_IN_OE	JTAG_DATAOUT_ODT_OE		JTAG_DATAOUT_ADDRESS_OE			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAG_DATAOUT_ADDRESS_OE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAG_DATAOUT_ADDRESS_OE		JTAG_DATAOUT_BANK_OE		JTAG_DATAOUT_BG_OE		JTAG_DATAOUT_WE_N_OE	JTAG_DATAOUT_CAS_N_OE
R/W		R/W		R/W		R/W	R/W
0h		0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAG_DATAOUT_RAS_N_OE	JTAG_DATAOUT_ACT_N_OE	JTAG_DATAOUT_CS_N_OE		JTAG_DATAOUT_MEM_CLK_0_OE	JTAG_DATAOUT_CKE_OE		JTAG_DATAOUT_RESET_N_OE
R/W	R/W	R/W		R/W	R/W		R/W
0h	0h	0h		0h	0h		0h

Table 14-12483. EMIF_SSCFG_PHY_TEST_CTRL4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAOUT_ERROR_N_OE	R/W	0h	Controls jtag_dataout_error_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAOUT_PARITY_IN_OE	R/W	0h	Controls jtag_dataout_parity_in_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
29:28	JTAG_DATAOUT_ODT_OE	R/W	0h	Controls jtag_dataout_odt_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
27:14	JTAG_DATAOUT_ADDRESS_OE	R/W	0h	Controls jtag_dataout_address_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
13:12	JTAG_DATAOUT_BANK_OE	R/W	0h	Controls jtag_dataout_bank_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-12483. EMIF_SSCFG_PHY_TEST_CTRL4_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	JTAG_DATAOUT_BG_OE	R/W	0h	Controls jtag_dataout_bg_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
9	JTAG_DATAOUT_WE_N_OE	R/W	0h	Controls jtag_dataout_we_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
8	JTAG_DATAOUT_CAS_N_OE	R/W	0h	Controls jtag_dataout_cas_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7	JTAG_DATAOUT_RAS_N_OE	R/W	0h	Controls jtag_dataout_ras_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAOUT_ACT_N_OE	R/W	0h	Controls jtag_dataout_act_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5:4	JTAG_DATAOUT_CS_N_OE	R/W	0h	Controls jtag_dataout_cs_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
3	JTAG_DATAOUT_MEM_CLK_0_OE	R/W	0h	Controls jtag_dataout_mem_clk_0_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
2:1	JTAG_DATAOUT_CKE_OE	R/W	0h	Controls jtag_dataout_cke_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
0	JTAG_DATAOUT_RESET_N_OE	R/W	0h	Controls jtag_dataout_reset_n_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.5.1.2.43 EMIF_SSCFG_PHY_TEST_CTRL5_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL5_REG Register (Offset = 194h) [reset = 0h]

PHY Test Control 5 Register

Return to Summary Table

Table 14-12484. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0194h**

Figure 14-4122. EMIF_SSCFG_PHY_TEST_CTRL5_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		JTAG_DATAOUT_DQS_OE		RESERVED		JTAG_DATAOUT_DM_OE	
NONE		R/W		NONE		R/W	
0h		0h		0h		0h	
15	14	13	12	11	10	9	8
JTAG_DATAOUT_DATA_OE							
R/W							
0h							
7	6	5	4	3	2	1	0
JTAG_DATAOUT_DATA_OE							
R/W							
0h							

Table 14-12486. EMIF_SSCFG_PHY_TEST_CTRL5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:20	JTAG_DATAOUT_DQS_OE	R/W	0h	Controls jtag_dataout_dqs_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
19:18	RESERVED	NONE	0h	Reserved
17:16	JTAG_DATAOUT_DM_OE	R/W	0h	Controls jtag_dataout_dm_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
15:0	JTAG_DATAOUT_DATA_OE	R/W	0h	Controls jtag_dataout_data_oe port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.5.1.2.44 EMIF_SSCFG_PHY_TEST_CTRL6_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL6_REG Register (Offset = 198h) [reset = 0h]

PHY Test Control 6 Register

Return to Summary Table

Table 14-12487. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 0198h**

Figure 14-4123. EMIF_SSCFG_PHY_TEST_CTRL6_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_ERROR_N	JTAG_DATAOUT_PARITY_IN	JTAG_DATAOUT_ODT		JTAG_DATAOUT_ADDRESS			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
23	22	21	20	19	18	17	16
JTAG_DATAOUT_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
JTAG_DATAOUT_ADDRESS		JTAG_DATAOUT_BANK		JTAG_DATAOUT_BG		JTAG_DATAOUT_WE_N	JTAG_DATAOUT_CAS_N
R/W		R/W		R/W		R/W	R/W
0h		0h		0h		0h	0h
7	6	5	4	3	2	1	0
JTAG_DATAOUT_RAS_N	JTAG_DATAOUT_ACT_N	JTAG_DATAOUT_CS_N		JTAG_DATAOUT_MEM_CLK_0	JTAG_DATAOUT_CKE		JTAG_DATAOUT_RESET_N
R/W	R/W	R/W		R/W	R/W		R/W
0h	0h	0h		0h	0h		0h

Table 14-12489. EMIF_SSCFG_PHY_TEST_CTRL6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAOUT_ERROR_N	R/W	0h	Controls jtag_dataout_error_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAOUT_PARITY_IN	R/W	0h	Controls jtag_dataout_parity_in port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
29:28	JTAG_DATAOUT_ODT	R/W	0h	Controls jtag_dataout_odt port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
27:14	JTAG_DATAOUT_ADDRESS	R/W	0h	Controls jtag_dataout_address port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
13:12	JTAG_DATAOUT_BANK	R/W	0h	Controls jtag_dataout_bank port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
11:10	JTAG_DATAOUT_BG	R/W	0h	Controls jtag_dataout_bg port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-12489. EMIF_SSCFG_PHY_TEST_CTRL6_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	JTAG_DATAOUT_WE_N	R/W	0h	Controls jtag_dataout_we_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
8	JTAG_DATAOUT_CAS_N	R/W	0h	Controls jtag_dataout_cas_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7	JTAG_DATAOUT_RAS_N	R/W	0h	Controls jtag_dataout_ras_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAOUT_ACT_N	R/W	0h	Controls jtag_dataout_act_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5:4	JTAG_DATAOUT_CS_N	R/W	0h	Controls jtag_dataout_cs_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
3	JTAG_DATAOUT_MEM_CLK_0	R/W	0h	Controls jtag_dataout_mem_clk_0 port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
2:1	JTAG_DATAOUT_CKE	R/W	0h	Controls jtag_dataout_cke port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
0	JTAG_DATAOUT_RESET_N	R/W	0h	Controls jtag_dataout_reset_n port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.5.1.2.45 EMIF_SSCFG_PHY_TEST_CTRL7_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL7_REG Register (Offset = 19Ch) [reset = 0h]

PHY Test Control 7 Register

Return to Summary Table

Table 14-12490. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 019Ch**

Figure 14-4124. EMIF_SSCFG_PHY_TEST_CTRL7_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">JTAG_DATAOUT_DQS</td><td colspan="2">RESERVED</td><td colspan="2">JTAG_DATAOUT_DM</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td colspan="2">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12492. EMIF_SSCFG_PHY_TEST_CTRL7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:20	JTAG_DATAOUT_DQS	R/W	0h	Controls jtag_dataout_dqs port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
19:18	RESERVED	NONE	0h	Reserved
17:16	JTAG_DATAOUT_DM	R/W	0h	Controls jtag_dataout_dm port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
15:0	JTAG_DATAOUT_DATA	R/W	0h	Controls jtag_dataout_data port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.5.1.2.46 EMIF_SSCFG_PHY_TEST_CTRL8_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL8_REG Register (Offset = 1A0h) [reset = FFFFFFFFh]

PHY Test Control 8 Register

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Table 14-12493. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 01A0h**

Figure 14-4125. EMIF_SSCFG_PHY_TEST_CTRL8_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAOUT_ERROR_N_IE	JTAG_DATAOUT_PARITY_IN_IE	JTAG_DATAOUT_ODT_IE		JTAG_DATAOUT_ADDRESS_IE			
R/W	R/W	R/W		R/W			
1h	1h	3h		3FFFh			
23	22	21	20	19	18	17	16
JTAG_DATAOUT_ADDRESS_IE							
R/W							
3FFFh							
15	14	13	12	11	10	9	8
JTAG_DATAOUT_ADDRESS_IE		JTAG_DATAOUT_BANK_IE		JTAG_DATAOUT_BG_IE		JTAG_DATAOUT_WE_N_IE	JTAG_DATAOUT_CAS_N_IE
R/W		R/W		R/W		R/W	R/W
3FFFh		3h		3h		1h	1h
7	6	5	4	3	2	1	0
JTAG_DATAOUT_RAS_N_IE	JTAG_DATAOUT_ACT_N_IE	JTAG_DATAOUT_CS_N_IE		JTAG_DATAOUT_MEM_CLK_0_IE	JTAG_DATAOUT_CKE_IE		JTAG_DATAOUT_RESET_N_IE
R/W	R/W	R/W		R/W	R/W		R/W
1h	1h	3h		1h	3h		1h

Table 14-12495. EMIF_SSCFG_PHY_TEST_CTRL8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAOUT_ERROR_N_IE	R/W	1h	Controls jtag_dataout_error_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAOUT_PARITY_IN_IE	R/W	1h	Controls jtag_dataout_parity_in_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
29:28	JTAG_DATAOUT_ODT_IE	R/W	3h	Controls jtag_dataout_odt_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
27:14	JTAG_DATAOUT_ADDRESS_IE	R/W	3FFFh	Controls jtag_dataout_address_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
13:12	JTAG_DATAOUT_BANK_IE	R/W	3h	Controls jtag_dataout_bank_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

Table 14-12495. EMIF_SSCFG_PHY_TEST_CTRL8_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	JTAG_DATAOUT_BG_IE	R/W	3h	Controls jtag_dataout_bg_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
9	JTAG_DATAOUT_WE_N_IE	R/W	1h	Controls jtag_dataout_we_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
8	JTAG_DATAOUT_CAS_N_IE	R/W	1h	Controls jtag_dataout_cas_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
7	JTAG_DATAOUT_RAS_N_IE	R/W	1h	Controls jtag_dataout_ras_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAOUT_ACT_N_IE	R/W	1h	Controls jtag_dataout_act_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
5:4	JTAG_DATAOUT_CS_N_IE	R/W	3h	Controls jtag_dataout_cs_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
3	JTAG_DATAOUT_MEM_CLK_0_IE	R/W	1h	Controls jtag_dataout_mem_clk_0_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
2:1	JTAG_DATAOUT_CKE_IE	R/W	3h	Controls jtag_dataout_cke_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
0	JTAG_DATAOUT_RESET_N_IE	R/W	1h	Controls jtag_dataout_reset_n_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.5.1.2.47 EMIF_SSCFG_PHY_TEST_CTRL9_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL9_REG Register (Offset = 1A4h) [reset = 33FFFFh]

PHY Test Control 9 Register

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Table 14-12496. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 01A4h**

Figure 14-4126. EMIF_SSCFG_PHY_TEST_CTRL9_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">JTAG_DATAOUT_DQS_IE</td><td colspan="2">RESERVED</td><td colspan="2">JTAG_DATAOUT_DM_IE</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td colspan="2">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">3h</td><td colspan="2">0h</td><td colspan="2">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_DATA_IE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">JTAG_DATAOUT_DATA_IE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-12498. EMIF_SSCFG_PHY_TEST_CTRL9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:20	JTAG_DATAOUT_DQS_IE	R/W	3h	Controls jtag_dataout_dqs_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
19:18	RESERVED	NONE	0h	Reserved
17:16	JTAG_DATAOUT_DM_IE	R/W	3h	Controls jtag_dataout_dm_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n
15:0	JTAG_DATAOUT_DATA_IE	R/W	FFFFh	Controls jtag_dataout_data_ie port on the PHY when ddrss_bs_mode=0 and hvm_test_en=1. Reset Source: ctl_smod_g_rst_n

14.5.1.2.48 EMIF_SSCFG_PHY_TEST_CTRL10_REG Register

1 EMIF_SSCFG_PHY_TEST_CTRL10_REG Register (Offset = 1A8h) [reset = 7h]

PHY Test Control 10 Register

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Table 14-12499. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 01A8h**

Figure 14-4127. EMIF_SSCFG_PHY_TEST_CTRL10_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HVM_CLK_DIV							
R/W							
7h							

Table 14-12501. EMIF_SSCFG_PHY_TEST_CTRL10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	HVM_CLK_DIV	R/W	7h	Divfactor to divide ddrss_ddr_pll_clk to generate PCLK for HVM tests when ddrss_bs_mode=0 and hvm_test_en=1. 0=div by 1, 1=div by 2, and so on. Reset Source: ctl_smod_g_rst_n

14.5.1.2.49 EMIF_SSCFG_PHY_TEST_STAT1_REG Register

1 EMIF_SSCFG_PHY_TEST_STAT1_REG Register (Offset = 1C0h) [reset = 0h]

PHY Test Status 1 Register

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Table 14-12502. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 01C0h**

Figure 14-4128. EMIF_SSCFG_PHY_TEST_STAT1_REG Name Register

31	30	29	28	27	26	25	24
JTAG_DATAIN_ERROR_N	JTAG_DATAIN_PARITY_IN	JTAG_DATAIN_ODT		JTAG_DATAIN_ADDRESS			
R	R	R		R			
0h	0h	0h		0h			
23	22	21	20	19	18	17	16
JTAG_DATAIN_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
JTAG_DATAIN_ADDRESS		JTAG_DATAIN_BANK		JTAG_DATAIN_BG		JTAG_DATAIN_WE_N	JTAG_DATAIN_CAS_N
R		R		R		R	R
0h		0h		0h		0h	0h
7	6	5	4	3	2	1	0
JTAG_DATAIN_RAS_N	JTAG_DATAIN_ACT_N	JTAG_DATAIN_CS_N		JTAG_DATAIN_MEM_CLK_0	JTAG_DATAIN_CKE		JTAG_DATAIN_RESET_N
R	R	R		R	R		R
0h	0h	0h		0h	0h		0h

Table 14-12504. EMIF_SSCFG_PHY_TEST_STAT1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	JTAG_DATAIN_ERROR_N	R	0h	Displays value of jtag_datain_error_n port on the PHY. Reset Source: ctl_smod_g_rst_n
30	JTAG_DATAIN_PARITY_IN	R	0h	Displays value of jtag_datain_parity_in port on the PHY. Reset Source: ctl_smod_g_rst_n
29:28	JTAG_DATAIN_ODT	R	0h	Displays value of jtag_datain_odt port on the PHY. Reset Source: ctl_smod_g_rst_n
27:14	JTAG_DATAIN_ADDRESS	R	0h	Displays value of jtag_datain_address port on the PHY. Reset Source: ctl_smod_g_rst_n
13:12	JTAG_DATAIN_BANK	R	0h	Displays value of jtag_datain_bank port on the PHY. Reset Source: ctl_smod_g_rst_n
11:10	JTAG_DATAIN_BG	R	0h	Displays value of jtag_datain_bg port on the PHY. Reset Source: ctl_smod_g_rst_n
9	JTAG_DATAIN_WE_N	R	0h	Displays value of jtag_datain_we_n port on the PHY. Reset Source: ctl_smod_g_rst_n
8	JTAG_DATAIN_CAS_N	R	0h	Displays value of jtag_datain_cas_n port on the PHY. Reset Source: ctl_smod_g_rst_n

Table 14-12504. EMIF_SSCFG_PHY_TEST_STAT1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	JTAG_DATAIN_RAS_N	R	0h	Displays value of jtag_datain_ras_n port on the PHY. Reset Source: ctl_smod_g_rst_n
6	JTAG_DATAIN_ACT_N	R	0h	Displays value of jtag_datain_act_n port on the PHY. Reset Source: ctl_smod_g_rst_n
5:4	JTAG_DATAIN_CS_N	R	0h	Displays value of jtag_datain_cs_n port on the PHY. Reset Source: ctl_smod_g_rst_n
3	JTAG_DATAIN_MEM_CLK_0	R	0h	Displays value of jtag_datain_mem_clk_0 port on the PHY. Reset Source: ctl_smod_g_rst_n
2:1	JTAG_DATAIN_CKE	R	0h	Displays value of jtag_datain_cke port on the PHY. Reset Source: ctl_smod_g_rst_n
0	JTAG_DATAIN_RESET_N	R	0h	Displays value of jtag_datain_reset_n port on the PHY. Reset Source: ctl_smod_g_rst_n

14.5.1.2.50 EMIF_SSCFG_PHY_TEST_STAT2_REG Register

1 EMIF_SSCFG_PHY_TEST_STAT2_REG Register (Offset = 1C4h) [reset = 0h]

PHY Test Status 2 Register

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Table 14-12505. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 01C4h**

Figure 14-4129. EMIF_SSCFG_PHY_TEST_STAT2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		JTAG_DATAIN_DQS		RESERVED		JTAG_DATAIN_DM	
NONE		R		NONE		R	
0h		0h		0h		0h	
15	14	13	12	11	10	9	8
JTAG_DATAIN_DATA							
R							
0h							
7	6	5	4	3	2	1	0
JTAG_DATAIN_DATA							
R							
0h							

Table 14-12507. EMIF_SSCFG_PHY_TEST_STAT2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:20	JTAG_DATAIN_DQS	R	0h	Displays value of jtag_datain_dqs port on the PHY. Reset Source: ctl_smod_g_rst_n
19:18	RESERVED	NONE	0h	Reserved
17:16	JTAG_DATAIN_DM	R	0h	Displays value of jtag_datain_dm port on the PHY. Reset Source: ctl_smod_g_rst_n
15:0	JTAG_DATAIN_DATA	R	0h	Displays value of jtag_datain_data port on the PHY. Reset Source: ctl_smod_g_rst_n

14.5.1.2.51 EMIF_CTLCFG_DENALI_CTL_0 Register

1 EMIF_CTLCFG_DENALI_CTL_0 Register (Offset = 0h) [reset = 10460000h]

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Table 14-12508. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8000h**

Figure 14-4130. EMIF_CTLCFG_DENALI_CTL_0 Name Register

31	30	29	28	27	26	25	24
CONTROLLER_ID							
R							
1046h							
23	22	21	20	19	18	17	16
CONTROLLER_ID							
R							
1046h							
15	14	13	12	11	10	9	8
RESERVED				DRAM_CLASS			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							START
NONE							R/W
0h							0h

Table 14-12510. EMIF_CTLCFG_DENALI_CTL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CONTROLLER_ID	R	1046h	Holds the controller product id number. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	DRAM_CLASS	R/W	0h	Defines the class of DRAM memory which is connected to the controller. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	START	R/W	0h	Initiate command processing in the controller. Set to 1 to initiate. Reset Source: ctl_amod_g_rst_n

14.5.1.2.52 EMIF_CTLCFG_DENALI_CTL_1 Register

1 EMIF_CTLCFG_DENALI_CTL_1 Register (Offset = 4h) [reset = 5D1AF3C3h]

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Table 14-12511. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8004h**

Figure 14-4131. EMIF_CTLCFG_DENALI_CTL_1 Name Register

31	30	29	28	27	26	25	24
CONTROLLER_VERSION_0							
R							
5D1AF3C3h							
23	22	21	20	19	18	17	16
CONTROLLER_VERSION_0							
R							
5D1AF3C3h							
15	14	13	12	11	10	9	8
CONTROLLER_VERSION_0							
R							
5D1AF3C3h							
7	6	5	4	3	2	1	0
CONTROLLER_VERSION_0							
R							
5D1AF3C3h							

Table 14-12513. EMIF_CTLCFG_DENALI_CTL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTROLLER_VERSION_0	R	5D1AF3C3h	Holds the controller version id. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.53 EMIF_CTLCFG_DENALI_CTL_2 Register

1 EMIF_CTLCFG_DENALI_CTL_2 Register (Offset = 8h) [reset = 171A610h]

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Table 14-12514. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8008h**

Figure 14-4132. EMIF_CTLCFG_DENALI_CTL_2 Name Register

31	30	29	28	27	26	25	24
CONTROLLER_VERSION_1							
R							
171A610h							
23	22	21	20	19	18	17	16
CONTROLLER_VERSION_1							
R							
171A610h							
15	14	13	12	11	10	9	8
CONTROLLER_VERSION_1							
R							
171A610h							
7	6	5	4	3	2	1	0
CONTROLLER_VERSION_1							
R							
171A610h							

Table 14-12516. EMIF_CTLCFG_DENALI_CTL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTROLLER_VERSION_1	R	171A610h	Holds the controller version id. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.54 EMIF_CTLCFG_DENALI_CTL_3 Register

1 EMIF_CTLCFG_DENALI_CTL_3 Register (Offset = Ch) [reset = 40020A11h]

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Table 14-12517. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 800Ch**

Figure 14-4133. EMIF_CTLCFG_DENALI_CTL_3 Name Register

31	30	29	28	27	26	25	24
READ_DATA_FIFO_DEPTH							
R							
40h							
23	22	21	20	19	18	17	16
RESERVED						MAX_CS_REG	
NONE						R	
0h						2h	
15	14	13	12	11	10	9	8
RESERVED				MAX_COL_REG			
NONE				R			
0h				Ah			
7	6	5	4	3	2	1	0
RESERVED			MAX_ROW_REG				
NONE			R				
0h			11h				

Table 14-12519. EMIF_CTLCFG_DENALI_CTL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	READ_DATA_FIFO_DEPTH	R	40h	Reports the depth of the controller core read data queue. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	MAX_CS_REG	R	2h	Holds the maximum number of chip selects available. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MAX_COL_REG	R	Ah	Holds the maximum width of column address in DRAMs. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	MAX_ROW_REG	R	11h	Holds the maximum width of memory address bus. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.55 EMIF_CTLCFG_DENALI_CTL_4 Register

1 EMIF_CTLCFG_DENALI_CTL_4 Register (Offset = 10h) [reset = 52006h]

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Table 14-12520. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8010h

Figure 14-4134. EMIF_CTLCFG_DENALI_CTL_4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
WRITE_DATA_FIFO_PTR_WIDTH							
R							
5h							
15	14	13	12	11	10	9	8
WRITE_DATA_FIFO_DEPTH							
R							
20h							
7	6	5	4	3	2	1	0
READ_DATA_FIFO_PTR_WIDTH							
R							
6h							

Table 14-12522. EMIF_CTLCFG_DENALI_CTL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	WRITE_DATA_FIFO_PTR_WIDTH	R	5h	Reports the width of the controller core write data latency queue pointer. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	WRITE_DATA_FIFO_DEPTH	R	20h	Reports the depth of the controller core write data latency queue. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	READ_DATA_FIFO_PTR_WIDTH	R	6h	Reports the width of the controller core read data queue pointer. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.56 EMIF_CTLCFG_DENALI_CTL_5 Register

1 EMIF_CTLCFG_DENALI_CTL_5 Register (Offset = 14h) [reset = 2050020h]

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Table 14-12523. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8014h

Figure 14-4135. EMIF_CTLCFG_DENALI_CTL_5 Name Register

31	30	29	28	27	26	25	24
ASYNC_CDC_STAGES							
R							
2h							
23	22	21	20	19	18	17	16
MEMCD_RMODW_FIFO_PTR_WIDTH							
R							
5h							
15	14	13	12	11	10	9	8
MEMCD_RMODW_FIFO_DEPTH							
R							
20h							
7	6	5	4	3	2	1	0
MEMCD_RMODW_FIFO_DEPTH							
R							
20h							

Table 14-12525. EMIF_CTLCFG_DENALI_CTL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ASYNC_CDC_STAGES	R	2h	Reports the number of synchronizer delays specified for the asynchronous boundary crossings. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	MEMCD_RMODW_FIFO_PTR_WIDTH	R	5h	Reports the width of the controller core read/modify/write FIFO pointer. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	MEMCD_RMODW_FIFO_DEPTH	R	20h	Reports the depth of the controller core read/modify/write FIFO. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.57 EMIF_CTLCFG_DENALI_CTL_6 Register

1 EMIF_CTLCFG_DENALI_CTL_6 Register (Offset = 18h) [reset = 3070101h]

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Table 14-12526. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8018h**

Figure 14-4136. EMIF_CTLCFG_DENALI_CTL_6 Name Register

31	30	29	28	27	26	25	24
AXI0_WRCMD_PROC_FIFO_LOG2_DEPTH							
R							
3h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AXI0_WR_ARRAY_LOG2_DEPTH							
R							
7h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AXI0_RDFIFO_LOG2_DEPTH							
R							
1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AXI0_CMDFIFO_LOG2_DEPTH							
R							
1h							

Table 14-12528. EMIF_CTLCFG_DENALI_CTL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	AXI0_WRCMD_PROC_FIFO_LOG2_DEPTH	R	3h	Reports the depth of the AXI port 0 write command processing FIFO. Value is the log2 value of the depth. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	AXI0_WR_ARRAY_LOG2_DEPTH	R	7h	Reports the depth of the AXI port 0 write data array. Value is the log2 value of the depth. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	AXI0_RDFIFO_LOG2_DEPTH	R	1h	Reports the depth of the AXI port 0 read data FIFO. Value is the log2 value of the depth. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	AXI0_CMDFIFO_LOG2_DEPTH	R	1h	Reports the depth of the AXI port 0 command FIFO. Value is the log2 value of the depth. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.58 EMIF_CTLCFG_DENALI_CTL_7 Register

1 EMIF_CTLCFG_DENALI_CTL_7 Register (Offset = 1Ch) [reset = 0h]

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Table 14-12529. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 801Ch**

Figure 14-4137. EMIF_CTLCFG_DENALI_CTL_7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT_F0							
R/W							
0h							

Table 14-12531. EMIF_CTLCFG_DENALI_CTL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT_F0	R/W	0h	DRAM TINIT value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.59 EMIF_CTLCFG_DENALI_CTL_8 Register

1 EMIF_CTLCFG_DENALI_CTL_8 Register (Offset = 20h) [reset = 0h]

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Table 14-12532. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8020h**

Figure 14-4138. EMIF_CTLCFG_DENALI_CTL_8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT3_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT3_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT3_F0							
R/W							
0h							

Table 14-12534. EMIF_CTLCFG_DENALI_CTL_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT3_F0	R/W	0h	DRAM TINIT3 value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.60 EMIF_CTLCFG_DENALI_CTL_9 Register

1 EMIF_CTLCFG_DENALI_CTL_9 Register (Offset = 24h) [reset = 0h]

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Table 14-12535. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8024h**

Figure 14-4139. EMIF_CTLCFG_DENALI_CTL_9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TINIT4_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TINIT4_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TINIT4_F0							
R/W							
0h							

Table 14-12537. EMIF_CTLCFG_DENALI_CTL_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT4_F0	R/W	0h	DRAM TINIT4 value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.61 EMIF_CTLCFG_DENALI_CTL_10 Register

1 EMIF_CTLCFG_DENALI_CTL_10 Register (Offset = 28h) [reset = 0h]

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Table 14-12538. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8028h**

Figure 14-4140. EMIF_CTLCFG_DENALI_CTL_10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT5_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT5_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT5_F0							
R/W							
0h							

Table 14-12540. EMIF_CTLCFG_DENALI_CTL_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT5_F0	R/W	0h	DRAM TINIT5 value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.62 EMIF_CTLCFG_DENALI_CTL_11 Register

1 EMIF_CTLCFG_DENALI_CTL_11 Register (Offset = 2Ch) [reset = 0h]

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Table 14-12541. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 802Ch**

Figure 14-4141. EMIF_CTLCFG_DENALI_CTL_11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT_F1							
R/W							
0h							

Table 14-12543. EMIF_CTLCFG_DENALI_CTL_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT_F1	R/W	0h	DRAM TINIT value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.63 EMIF_CTLCFG_DENALI_CTL_12 Register

1 EMIF_CTLCFG_DENALI_CTL_12 Register (Offset = 30h) [reset = 0h]

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Table 14-12544. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8030h**

Figure 14-4142. EMIF_CTLCFG_DENALI_CTL_12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT3_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT3_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT3_F1							
R/W							
0h							

Table 14-12546. EMIF_CTLCFG_DENALI_CTL_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT3_F1	R/W	0h	DRAM TINIT3 value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.64 EMIF_CTLCFG_DENALI_CTL_13 Register

1 EMIF_CTLCFG_DENALI_CTL_13 Register (Offset = 34h) [reset = 0h]

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Table 14-12547. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8034h**

Figure 14-4143. EMIF_CTLCFG_DENALI_CTL_13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT4_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT4_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT4_F1							
R/W							
0h							

Table 14-12549. EMIF_CTLCFG_DENALI_CTL_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT4_F1	R/W	0h	DRAM TINIT4 value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.65 EMIF_CTLCFG_DENALI_CTL_14 Register

1 EMIF_CTLCFG_DENALI_CTL_14 Register (Offset = 38h) [reset = 0h]

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Table 14-12550. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8038h**

Figure 14-4144. EMIF_CTLCFG_DENALI_CTL_14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT5_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT5_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT5_F1							
R/W							
0h							

Table 14-12552. EMIF_CTLCFG_DENALI_CTL_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT5_F1	R/W	0h	DRAM TINIT5 value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.66 EMIF_CTLCFG_DENALI_CTL_15 Register

1 EMIF_CTLCFG_DENALI_CTL_15 Register (Offset = 3Ch) [reset = 0h]

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Table 14-12553. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 803Ch**

Figure 14-4145. EMIF_CTLCFG_DENALI_CTL_15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT_F2							
R/W							
0h							

Table 14-12555. EMIF_CTLCFG_DENALI_CTL_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT_F2	R/W	0h	DRAM TINIT value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.67 EMIF_CTLCFG_DENALI_CTL_16 Register

1 EMIF_CTLCFG_DENALI_CTL_16 Register (Offset = 40h) [reset = 0h]

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Table 14-12556. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8040h**

Figure 14-4146. EMIF_CTLCFG_DENALI_CTL_16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TINIT3_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TINIT3_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TINIT3_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12558. EMIF_CTLCFG_DENALI_CTL_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT3_F2	R/W	0h	DRAM TINIT3 value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.68 EMIF_CTLCFG_DENALI_CTL_17 Register

1 EMIF_CTLCFG_DENALI_CTL_17 Register (Offset = 44h) [reset = 0h]

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Table 14-12559. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8044h

Figure 14-4147. EMIF_CTLCFG_DENALI_CTL_17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TINIT4_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT4_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT4_F2							
R/W							
0h							

Table 14-12561. EMIF_CTLCFG_DENALI_CTL_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TINIT4_F2	R/W	0h	DRAM TINIT4 value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.69 EMIF_CTLCFG_DENALI_CTL_18 Register

1 EMIF_CTLCFG_DENALI_CTL_18 Register (Offset = 48h) [reset = 0h]

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Table 14-12562. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8048h**

Figure 14-4148. EMIF_CTLCFG_DENALI_CTL_18 Name Register

31	30	29	28	27	26	25	24
RESERVED							NO_AUTO_MR R_INIT
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
TINIT5_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TINIT5_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TINIT5_F2							
R/W							
0h							

Table 14-12564. EMIF_CTLCFG_DENALI_CTL_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	NO_AUTO_MRR_INIT	R/W	0h	Disable MRR commands during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:0	TINIT5_F2	R/W	0h	DRAM TINIT5 value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.70 EMIF_CTLCFG_DENALI_CTL_19 Register

1 EMIF_CTLCFG_DENALI_CTL_19 Register (Offset = 4Ch) [reset = 0h]

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Table 14-12565. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 804Ch**

Figure 14-4149. EMIF_CTLCFG_DENALI_CTL_19 Name Register

31	30	29	28	27	26	25	24
RESERVED						DFI_FREQ_RATIO_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						DFI_FREQ_RATIO_F1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						DFI_FREQ_RATIO_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							MRR_ERROR_STATUS
NONE							R
0h							0h

Table 14-12567. EMIF_CTLCFG_DENALI_CTL_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	DFI_FREQ_RATIO_F2	R/W	0h	Defines how dfi_freq_ratio is driven on the DFI bus. For LPDDR5, specifies the DFI clock to WCK ratio. For all other memory classes, specifies the controller clock to DFI PHY clock ratio. Program to zero for a 1:1 ratio, one for a 1:2 ratio, and two for a 1:4 ratio. FC=2 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	DFI_FREQ_RATIO_F1	R/W	0h	Defines how dfi_freq_ratio is driven on the DFI bus. For LPDDR5, specifies the DFI clock to WCK ratio. For all other memory classes, specifies the controller clock to DFI PHY clock ratio. Program to zero for a 1:1 ratio, one for a 1:2 ratio, and two for a 1:4 ratio. FC=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	DFI_FREQ_RATIO_F0	R/W	0h	Defines how dfi_freq_ratio is driven on the DFI bus. For LPDDR5, specifies the DFI clock to WCK ratio. For all other memory classes, specifies the controller clock to DFI PHY clock ratio. Program to zero for a 1:1 ratio, one for a 1:2 ratio, and two for a 1:4 ratio. FC=0 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-12567. EMIF_CTLCFG_DENALI_CTL_19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MRR_ERROR_STATUS	R	0h	Indicates that an MRR was issued while in self-refresh. Value of 1 indicates a violation. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.71 EMIF_CTLCFG_DENALI_CTL_20 Register

1 EMIF_CTLCFG_DENALI_CTL_20 Register (Offset = 50h) [reset = 1h]

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Table 14-12568. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8050h**

Figure 14-4150. EMIF_CTLCFG_DENALI_CTL_20 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_INDEP_TRAIN_MODE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						ODT_VALUE	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NO_MRW_INIT
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							DFI_CMD_RATIO
NONE							R
0h							1h

Table 14-12570. EMIF_CTLCFG_DENALI_CTL_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_INDEP_TRAIN_MODE	R/W	0h	Enable PHY independent training mode commands during initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	ODT_VALUE	R/W	0h	When using LPDDR4, this value will be driven out on the dfi_odt signal. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	NO_MRW_INIT	R/W	0h	Disable MRW commands during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	DFI_CMD_RATIO	R	1h	Indicates the controller clock to DFI PHY clock ratio for the DFI command interface. For LPDDR5, this is always a 1:1 ratio. For all other memory classes, this will be the same as the dfi_freq_ratio. Zero specifies a 1:1 ratio and one specifies a 1:2 ratio. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.72 EMIF_CTLCFG_DENALI_CTL_21 Register

1 EMIF_CTLCFG_DENALI_CTL_21 Register (Offset = 54h) [reset = 0h]

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Table 14-12571. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8054h**

Figure 14-4151. EMIF_CTLCFG_DENALI_CTL_21 Name Register

31	30	29	28	27	26	25	24
RESERVED			DFIBUS_FREQ_F1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			DFIBUS_FREQ_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_INDEP_INIT_MODE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TSREF2PHYMSTR					
NONE		R/W					
0h		0h					

Table 14-12573. EMIF_CTLCFG_DENALI_CTL_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	DFIBUS_FREQ_F1	R/W	0h	Defines the DFI bus frequency. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	DFIBUS_FREQ_F0	R/W	0h	Defines the DFI bus frequency. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_INDEP_INIT_MODE	R/W	0h	Enable PHY independent initailization mode commands during initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	TSREF2PHYMSTR	R/W	0h	Specifies the minimum time after a self-refresh exit command on the DFI bus that the Controller will wait for the PHY to assert the dfi_phymstr_req signal, before completing other commands. Used when the low power control logic is expected to pass control to the PHY for training when exiting SREF. Reset Source: ctl_amod_g_rst_n

14.5.1.2.73 EMIF_CTLCFG_DENALI_CTL_22 Register

1 EMIF_CTLCFG_DENALI_CTL_22 Register (Offset = 58h) [reset = 0h]

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Table 14-12574. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8058h**

Figure 14-4152. EMIF_CTLCFG_DENALI_CTL_22 Name Register

31	30	29	28	27	26	25	24
RESERVED						FREQ_CHANGE_TYPE_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						FREQ_CHANGE_TYPE_F1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						FREQ_CHANGE_TYPE_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED			DFIBUS_FREQ_F2				
NONE			R/W				
0h			0h				

Table 14-12576. EMIF_CTLCFG_DENALI_CTL_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	FREQ_CHANGE_TYPE_F2	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation. FC=2 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	FREQ_CHANGE_TYPE_F1	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation. FC=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	FREQ_CHANGE_TYPE_F0	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	DFIBUS_FREQ_F2	R/W	0h	Defines the DFI bus frequency. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.74 EMIF_CTLCFG_DENALI_CTL_23 Register

1 EMIF_CTLCFG_DENALI_CTL_23 Register (Offset = 5Ch) [reset = 0h]

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Table 14-12577. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 805Ch**

Figure 14-4153. EMIF_CTLCFG_DENALI_CTL_23 Name Register

31	30	29	28	27	26	25	24
TRST_PWRON							
R/W							
0h							
23	22	21	20	19	18	17	16
TRST_PWRON							
R/W							
0h							
15	14	13	12	11	10	9	8
TRST_PWRON							
R/W							
0h							
7	6	5	4	3	2	1	0
TRST_PWRON							
R/W							
0h							

Table 14-12579. EMIF_CTLCFG_DENALI_CTL_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRST_PWRON	R/W	0h	Duration of memory reset during power-on initialization. Reset Source: ctl_amod_g_rst_n

14.5.1.2.75 EMIF_CTLCFG_DENALI_CTL_24 Register

1 EMIF_CTLCFG_DENALI_CTL_24 Register (Offset = 60h) [reset = 0h]

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Table 14-12580. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8060h**

Figure 14-4154. EMIF_CTLCFG_DENALI_CTL_24 Name Register

31	30	29	28	27	26	25	24
CKE_INACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
CKE_INACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
CKE_INACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
CKE_INACTIVE							
R/W							
0h							

Table 14-12582. EMIF_CTLCFG_DENALI_CTL_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CKE_INACTIVE	R/W	0h	Number of cycles after reset before CKE will be active. Reset Source: ctl_amod_g_rst_n

14.5.1.2.76 EMIF_CTLCFG_DENALI_CTL_25 Register

1 EMIF_CTLCFG_DENALI_CTL_25 Register (Offset = 64h) [reset = 0h]

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Table 14-12583. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8064h**

Figure 14-4155. EMIF_CTLCFG_DENALI_CTL_25 Name Register

31	30	29	28	27	26	25	24
TDLL_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDLL_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDLL_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDLL_F0							
R/W							
0h							

Table 14-12585. EMIF_CTLCFG_DENALI_CTL_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TDLL_F1	R/W	0h	DRAM TDLL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	TDLL_F0	R/W	0h	DRAM TDLL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.77 EMIF_CTLCFG_DENALI_CTL_26 Register

1 EMIF_CTLCFG_DENALI_CTL_26 Register (Offset = 68h) [reset = 0h]

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Table 14-12586. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8068h**

Figure 14-4156. EMIF_CTLCFG_DENALI_CTL_26 Name Register

31	30	29	28	27	26	25	24
RESERVED						DQS_OSC_PER_CS_OOV_TRAINING_STATUS	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							LPC_SW_ENTER_DQS_OSC_IN_PROGRESS_ERR_STATUS
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDLL_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDLL_F2							
R/W							
0h							

Table 14-12588. EMIF_CTLCFG_DENALI_CTL_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	DQS_OSC_PER_CS_OOV_TRAINING_STATUS	R	0h	Set the CS information for which DQS oscillator is having out of variance value. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	LPC_SW_ENTER_DQS_OSC_IN_PROGRESS_ERR_STATUS	R	0h	Error response for Software issued Low power command while DQS Oscillator is in progress. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	TDLL_F2	R/W	0h	DRAM TDLL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.78 EMIF_CTLCFG_DENALI_CTL_27 Register

1 EMIF_CTLCFG_DENALI_CTL_27 Register (Offset = 6Ch) [reset = 0h]

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Table 14-12589. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 806Ch**

Figure 14-4157. EMIF_CTLCFG_DENALI_CTL_27 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_MPC_CMD							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_MPC_CMD							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_MPC_CMD							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							DQS_OSC_TST
NONE							R/W
0h							0h

Table 14-12591. EMIF_CTLCFG_DENALI_CTL_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DQS_OSC_MPC_CMD	R/W	0h	Set MPC encoding for DQS Oscillator TEST mode. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	DQS_OSC_TST	R/W	0h	Enable DQS Oscillator TEST mode. Reset Source: ctl_amod_g_rst_n

14.5.1.2.79 EMIF_CTLCFG_DENALI_CTL_28 Register

1 EMIF_CTLCFG_DENALI_CTL_28 Register (Offset = 70h) [reset = 0h]

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Table 14-12592. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8070h**

Figure 14-4158. EMIF_CTLCFG_DENALI_CTL_28 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>DQS_OSC_ENABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MRR_MSB_REG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MRR_LSB_REG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12594. EMIF_CTLCFG_DENALI_CTL_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	DQS_OSC_ENABLE	R/W	0h	Enable DQS oscillator measurement function in DRAM. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:8	MRR_MSB_REG	R/W	0h	Set MSB MRR register number for DQS Oscillator TEST mode. Reset Source: ctl_amod_g_rst_n
7:0	MRR_LSB_REG	R/W	0h	Set LSB MRR register number for DQS Oscillator TEST mode. Reset Source: ctl_amod_g_rst_n

14.5.1.2.80 EMIF_CTLCFG_DENALI_CTL_29 Register

1 EMIF_CTLCFG_DENALI_CTL_29 Register (Offset = 74h) [reset = 0h]

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Table 14-12595. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8074h**

Figure 14-4159. EMIF_CTLCFG_DENALI_CTL_29 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FUNC_VALID_CYCLES</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">DQS_OSC_PERIOD</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DQS_OSC_PERIOD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12597. EMIF_CTLCFG_DENALI_CTL_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	FUNC_VALID_CYCLES	R/W	0h	Number of cycles to hold dfi_function_valid asserted. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:0	DQS_OSC_PERIOD	R/W	0h	Number of cycles to run the oscillator measurement. Must reflect cycles programmed into mode register. Reset Source: ctl_amod_g_rst_n

14.5.1.2.81 EMIF_CTLCFG_DENALI_CTL_30 Register

1 EMIF_CTLCFG_DENALI_CTL_30 Register (Offset = 78h) [reset = 0h]

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Table 14-12598. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8078h

Figure 14-4160. EMIF_CTLCFG_DENALI_CTL_30 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_NORM_THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_NORM_THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_NORM_THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_NORM_THRESHOLD							
R/W							
0h							

Table 14-12600. EMIF_CTLCFG_DENALI_CTL_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DQS_OSC_NORM_THRESHOLD	R/W	0h	Number of long counts until the normal priority request is asserted for DQS Oscillator. Reset Source: ctl_amod_g_rst_n

14.5.1.2.82 EMIF_CTLCFG_DENALI_CTL_31 Register

1 EMIF_CTLCFG_DENALI_CTL_31 Register (Offset = 7Ch) [reset = 0h]

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Table 14-12601. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 807Ch**

Figure 14-4161. EMIF_CTLCFG_DENALI_CTL_31 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_HIGH_THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_HIGH_THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_HIGH_THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_HIGH_THRESHOLD							
R/W							
0h							

Table 14-12603. EMIF_CTLCFG_DENALI_CTL_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DQS_OSC_HIGH_THRESHOLD	R/W	0h	Number of long counts until the high priority request is asserted for DQS Oscillator. Reset Source: ctl_amod_g_rst_n

14.5.1.2.83 EMIF_CTLCFG_DENALI_CTL_32 Register

1 EMIF_CTLCFG_DENALI_CTL_32 Register (Offset = 80h) [reset = 0h]

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Table 14-12604. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8080h**

Figure 14-4162. EMIF_CTLCFG_DENALI_CTL_32 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_TIMEOUT							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_TIMEOUT							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_TIMEOUT							
R/W							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_TIMEOUT							
R/W							
0h							

Table 14-12606. EMIF_CTLCFG_DENALI_CTL_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DQS_OSC_TIMEOUT	R/W	0h	Number of long counts until the timeout is asserted for DQS Oscillator. Reset Source: ctl_amod_g_rst_n

14.5.1.2.84 *EMIF_CTLCFG_DENALI_CTL_33 Register*

1 EMIF_CTLCFG_DENALI_CTL_33 Register (Offset = 84h) [reset = 0h]

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Table 14-12607. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8084h**

Figure 14-4163. EMIF_CTLCFG_DENALI_CTL_33 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_PROMOTE_THRESHOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_PROMOTE_THRESHOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_PROMOTE_THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_PROMOTE_THRESHOLD							
R/W							
0h							

Table 14-12609. EMIF_CTLCFG_DENALI_CTL_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DQS_OSC_PROMOTE_THRESHOLD	R/W	0h	Number of long counts until a software request for the DQS Oscillator is promoted to high priority. Reset Source: ctl_amod_g_rst_n

14.5.1.2.85 EMIF_CTLCFG_DENALI_CTL_34 Register

1 EMIF_CTLCFG_DENALI_CTL_34 Register (Offset = 88h) [reset = 0h]

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Table 14-12610. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8088h**

Figure 14-4164. EMIF_CTLCFG_DENALI_CTL_34 Name Register

31	30	29	28	27	26	25	24
TOSCO_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							DQS_OSC_REQUEST
NONE							W
0h							0h
15	14	13	12	11	10	9	8
OSC_VARIANCE_LIMIT							
R/W							
0h							
7	6	5	4	3	2	1	0
OSC_VARIANCE_LIMIT							
R/W							
0h							

Table 14-12612. EMIF_CTLCFG_DENALI_CTL_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TOSCO_F0	R/W	0h	Number of cycles for tOSCO timing parameter, the time for the DQS Oscillator measurement to be available in the mode registers. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	DQS_OSC_REQUEST	W	0h	Software request for DQS Oscillator measurement function in DRAM. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:0	OSC_VARIANCE_LIMIT	R/W	0h	Allowed difference between base value and DQS Oscillator measurement. Reset Source: ctl_amod_g_rst_n

14.5.1.2.86 EMIF_CTLCFG_DENALI_CTL_35 Register

1 EMIF_CTLCFG_DENALI_CTL_35 Register (Offset = 8Ch) [reset = 0h]

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Table 14-12613. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 808Ch**

Figure 14-4165. EMIF_CTLCFG_DENALI_CTL_35 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_BASE_VALUE_0_CS0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DQS_OSC_BASE_VALUE_0_CS0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TOSCO_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TOSCO_F1							
R/W							
0h							

Table 14-12615. EMIF_CTLCFG_DENALI_CTL_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DQS_OSC_BASE_VALUE_0_CS0	R	0h	Base value for device 0 on chip 0. READ-ONLY DEV=0 Reset Source: ctl_amod_g_rst_n
15:8	TOSCO_F2	R/W	0h	Number of cycles for tOSCO timing parameter, the time for the DQS Oscillator measurement to be available in the mode registers. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TOSCO_F1	R/W	0h	Number of cycles for tOSCO timing parameter, the time for the DQS Oscillator measurement to be available in the mode registers. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.87 EMIF_CTLCFG_DENALI_CTL_36 Register

1 EMIF_CTLCFG_DENALI_CTL_36 Register (Offset = 90h) [reset = 0h]

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Table 14-12616. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8090h**

Figure 14-4166. EMIF_CTLCFG_DENALI_CTL_36 Name Register

31	30	29	28	27	26	25	24
DQS_OSC_BASE_VALUE_0_CS1							
R							
0h							
23	22	21	20	19	18	17	16
DQS_OSC_BASE_VALUE_0_CS1							
R							
0h							
15	14	13	12	11	10	9	8
DQS_OSC_BASE_VALUE_1_CS0							
R							
0h							
7	6	5	4	3	2	1	0
DQS_OSC_BASE_VALUE_1_CS0							
R							
0h							

Table 14-12618. EMIF_CTLCFG_DENALI_CTL_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DQS_OSC_BASE_VALUE_0_CS1	R	0h	Base value for device 0 on chip 1. READ-ONLY DEV=0 Reset Source: ctl_amod_g_rst_n
15:0	DQS_OSC_BASE_VALUE_1_CS0	R	0h	Base value for device 1 on chip 0. READ-ONLY DEV=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.88 EMIF_CTLCFG_DENALI_CTL_37 Register

1 EMIF_CTLCFG_DENALI_CTL_37 Register (Offset = 94h) [reset = 0h]

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Table 14-12619. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8094h**

Figure 14-4167. EMIF_CTLCFG_DENALI_CTL_37 Name Register

31	30	29	28	27	26	25	24
RESERVED							DQS_OSC_IN_PROGRESS_STATUS
NONE							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				DQS_OSC_STATUS			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DQS_OSC_BASE_VALUE_1_CS1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DQS_OSC_BASE_VALUE_1_CS1							
R							
0h							

Table 14-12621. EMIF_CTLCFG_DENALI_CTL_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	DQS_OSC_IN_PROGRESS_STATUS	R	0h	DQS Oscillator is in progress.Set '1' DQS OSC is in progress READ-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	DQS_OSC_STATUS	R	0h	Holds the overflow and out of variance status associated with the resp. interrupts. Bit [0] set indicates overflow of DQS oscillator,bit [1] set indicates overflow of WCKO oscillator,bit [2] set indicates oov of DQS oscillator,bit [3] set indicates oov of WCKO oscillator. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	DQS_OSC_BASE_VALUE_1_CS1	R	0h	Base value for device 1 on chip 1. READ-ONLY DEV=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.89 EMIF_CTLCFG_DENALI_CTL_38 Register

1 EMIF_CTLCFG_DENALI_CTL_38 Register (Offset = 98h) [reset = 0h]

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Table 14-12622. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8098h**

Figure 14-4168. EMIF_CTLCFG_DENALI_CTL_38 Name Register

31	30	29	28	27	26	25	24
RESERVED				CA_PARITY_LAT_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED		ADDITIVE_LAT_F0					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED	WRLAT_F0						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	CASLAT_LIN_F0						
NONE	R/W						
0h	0h						

Table 14-12624. EMIF_CTLCFG_DENALI_CTL_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CA_PARITY_LAT_F0	R/W	0h	DRAM CA parity latency value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	ADDITIVE_LAT_F0	R/W	0h	DRAM additive latency value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	WRLAT_F0	R/W	0h	DRAM WRLAT value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	CASLAT_LIN_F0	R/W	0h	Sets latency from read command send to data receive from/to controller. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.90 EMIF_CTLCFG_DENALI_CTL_39 Register

1 EMIF_CTLCFG_DENALI_CTL_39 Register (Offset = 9Ch) [reset = 0h]

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Table 14-12625. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 809Ch**

Figure 14-4169. EMIF_CTLCFG_DENALI_CTL_39 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TMRD_PAR_MAX_PL_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TMOD_PAR_MAX_PL_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TMRD_PAR_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TMOD_PAR_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12627. EMIF_CTLCFG_DENALI_CTL_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TMRD_PAR_MAX_PL_F0	R/W	0h	DRAM TMRD value with maximum CA parity for frequency copy 2 in cycles. Used during changes of CA parity latency value in DRAM. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TMOD_PAR_MAX_PL_F0	R/W	0h	DRAM TMOD value with maximum CA parity for frequency copy 2 in cycles. Used during changes of CA parity latency value in DRAM. FC=0 Reset Source: ctl_amod_g_rst_n
15:8	TMRD_PAR_F0	R/W	0h	DRAM TMRD value when CA parity is enabled in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TMOD_PAR_F0	R/W	0h	DRAM TMOD value when CA parity is enabled in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.91 EMIF_CTLCFG_DENALI_CTL_40 Register

1 EMIF_CTLCFG_DENALI_CTL_40 Register (Offset = A0h) [reset = 0h]

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Table 14-12628. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80A0h**

Figure 14-4170. EMIF_CTLCFG_DENALI_CTL_40 Name Register

31	30	29	28	27	26	25	24
RESERVED				CA_PARITY_LAT_F1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED		ADDITIVE_LAT_F1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED	WRLAT_F1						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	CASLAT_LIN_F1						
NONE	R/W						
0h	0h						

Table 14-12630. EMIF_CTLCFG_DENALI_CTL_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CA_PARITY_LAT_F1	R/W	0h	DRAM CA parity latency value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	ADDITIVE_LAT_F1	R/W	0h	DRAM additive latency value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	WRLAT_F1	R/W	0h	DRAM WRLAT value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	CASLAT_LIN_F1	R/W	0h	Sets latency from read command send to data receive from/to controller. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.92 EMIF_CTLCFG_DENALI_CTL_41 Register

1 EMIF_CTLCFG_DENALI_CTL_41 Register (Offset = A4h) [reset = 0h]

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Table 14-12631. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 80A4h

Figure 14-4171. EMIF_CTLCFG_DENALI_CTL_41 Name Register

31	30	29	28	27	26	25	24
TMRD_PAR_MAX_PL_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TMOD_PAR_MAX_PL_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TMRD_PAR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TMOD_PAR_F1							
R/W							
0h							

Table 14-12633. EMIF_CTLCFG_DENALI_CTL_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TMRD_PAR_MAX_PL_F1	R/W	0h	DRAM TMRD value with maximum CA parity for frequency copy 2 in cycles. Used during changes of CA parity latency value in DRAM. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TMOD_PAR_MAX_PL_F1	R/W	0h	DRAM TMOD value with maximum CA parity for frequency copy 2 in cycles. Used during changes of CA parity latency value in DRAM. FC=1 Reset Source: ctl_amod_g_rst_n
15:8	TMRD_PAR_F1	R/W	0h	DRAM TMRD value when CA parity is enabled in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TMOD_PAR_F1	R/W	0h	DRAM TMOD value when CA parity is enabled in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.93 EMIF_CTLCFG_DENALI_CTL_42 Register

1 EMIF_CTLCFG_DENALI_CTL_42 Register (Offset = A8h) [reset = 0h]

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Table 14-12634. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 80A8h

Figure 14-4172. EMIF_CTLCFG_DENALI_CTL_42 Name Register

31	30	29	28	27	26	25	24
RESERVED				CA_PARITY_LAT_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED		ADDITIVE_LAT_F2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED	WRLAT_F2						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	CASLAT_LIN_F2						
NONE	R/W						
0h	0h						

Table 14-12636. EMIF_CTLCFG_DENALI_CTL_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CA_PARITY_LAT_F2	R/W	0h	DRAM CA parity latency value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	ADDITIVE_LAT_F2	R/W	0h	DRAM additive latency value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	WRLAT_F2	R/W	0h	DRAM WRLAT value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	CASLAT_LIN_F2	R/W	0h	Sets latency from read command send to data receive from/to controller. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.94 EMIF_CTLCFG_DENALI_CTL_43 Register

1 EMIF_CTLCFG_DENALI_CTL_43 Register (Offset = ACh) [reset = 0h]

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Table 14-12637. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 80ACh

Figure 14-4173. EMIF_CTLCFG_DENALI_CTL_43 Name Register

31	30	29	28	27	26	25	24
TMRD_PAR_MAX_PL_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TMOD_PAR_MAX_PL_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TMRD_PAR_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TMOD_PAR_F2							
R/W							
0h							

Table 14-12639. EMIF_CTLCFG_DENALI_CTL_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TMRD_PAR_MAX_PL_F2	R/W	0h	DRAM TMRD value with maximum CA parity for frequency copy 2 in cycles. Used during changes of CA parity latency value in DRAM. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TMOD_PAR_MAX_PL_F2	R/W	0h	DRAM TMOD value with maximum CA parity for frequency copy 2 in cycles. Used during changes of CA parity latency value in DRAM. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TMRD_PAR_F2	R/W	0h	DRAM TMRD value when CA parity is enabled in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TMOD_PAR_F2	R/W	0h	DRAM TMOD value when CA parity is enabled in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.95 EMIF_CTLCFG_DENALI_CTL_44 Register

1 EMIF_CTLCFG_DENALI_CTL_44 Register (Offset = B0h) [reset = 0h]

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Table 14-12640. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80B0h**

Figure 14-4174. EMIF_CTLCFG_DENALI_CTL_44 Name Register

31	30	29	28	27	26	25	24
TRRD_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCCD_L_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TCCD				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TBST_INT_INTERVAL		
NONE					R/W		
0h					0h		

Table 14-12642. EMIF_CTLCFG_DENALI_CTL_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRRD_F0	R/W	0h	DRAM TRRD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCCD_L_F0	R/W	0h	DRAM CAS-to-CAS value within the same bank group in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCCD	R/W	0h	DRAM CAS-to-CAS value in cycles. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TBST_INT_INTERVAL	R/W	0h	DRAM burst interrupt interval value in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.96 EMIF_CTLCFG_DENALI_CTL_45 Register

1 EMIF_CTLCFG_DENALI_CTL_45 Register (Offset = B4h) [reset = 0h]

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Table 14-12643. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80B4h**

Figure 14-4175. EMIF_CTLCFG_DENALI_CTL_45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>TRC_F0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TRC_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRRD_L_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12645. EMIF_CTLCFG_DENALI_CTL_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:8	TRC_F0	R/W	0h	DRAM TRC value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TRRD_L_F0	R/W	0h	DRAM TRRD_L value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.97 EMIF_CTLCFG_DENALI_CTL_46 Register

1 EMIF_CTLCFG_DENALI_CTL_46 Register (Offset = B8h) [reset = 0h]

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Table 14-12646. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80B8h**

Figure 14-4176. EMIF_CTLCFG_DENALI_CTL_46 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TWTR_L_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TWTR_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>TRAS_MIN_F0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRAS_MIN_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12648. EMIF_CTLCFG_DENALI_CTL_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TWTR_L_F0	R/W	0h	DRAM TWTR_L value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	TWTR_F0	R/W	0h	DRAM TWTR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	TRAS_MIN_F0	R/W	0h	DRAM TRAS_MIN value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.98 EMIF_CTLCFG_DENALI_CTL_47 Register

1 EMIF_CTLCFG_DENALI_CTL_47 Register (Offset = BCh) [reset = 0h]

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Table 14-12649. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80BCh**

Figure 14-4177. EMIF_CTLCFG_DENALI_CTL_47 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCCD_L_F1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							TFAW_F0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
TFAW_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TRP_F0							
R/W							
0h							

Table 14-12651. EMIF_CTLCFG_DENALI_CTL_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCCD_L_F1	R/W	0h	DRAM CAS-to-CAS value within the same bank group in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	TFAW_F0	R/W	0h	DRAM TFAW value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TRP_F0	R/W	0h	DRAM TRP value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.99 EMIF_CTLCFG_DENALI_CTL_48 Register

1 EMIF_CTLCFG_DENALI_CTL_48 Register (Offset = C0h) [reset = 0h]

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Table 14-12652. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80C0h**

Figure 14-4178. EMIF_CTLCFG_DENALI_CTL_48 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRC_F1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
TRC_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TRRD_L_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TRRD_F1							
R/W							
0h							

Table 14-12654. EMIF_CTLCFG_DENALI_CTL_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	TRC_F1	R/W	0h	DRAM TRC value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:8	TRRD_L_F1	R/W	0h	DRAM TRRD_L value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TRRD_F1	R/W	0h	DRAM TRRD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.100 EMIF_CTLCFG_DENALI_CTL_49 Register

1 EMIF_CTLCFG_DENALI_CTL_49 Register (Offset = C4h) [reset = 0h]

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Table 14-12655. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80C4h**

Figure 14-4179. EMIF_CTLCFG_DENALI_CTL_49 Name Register

31	30	29	28	27	26	25	24
RESERVED		TWTR_L_F1					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		TWTR_F1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED							TRAS_MIN_F1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
TRAS_MIN_F1							
R/W							
0h							

Table 14-12657. EMIF_CTLCFG_DENALI_CTL_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TWTR_L_F1	R/W	0h	DRAM TWTR_L value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	TWTR_F1	R/W	0h	DRAM TWTR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	TRAS_MIN_F1	R/W	0h	DRAM TRAS_MIN value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.101 EMIF_CTLCFG_DENALI_CTL_50 Register

1 EMIF_CTLCFG_DENALI_CTL_50 Register (Offset = C8h) [reset = 0h]

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Table 14-12658. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80C8h**

Figure 14-4180. EMIF_CTLCFG_DENALI_CTL_50 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCCD_L_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>TFAW_F1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TFAW_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRP_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12660. EMIF_CTLCFG_DENALI_CTL_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCCD_L_F2	R/W	0h	DRAM CAS-to-CAS value within the same bank group in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	TFAW_F1	R/W	0h	DRAM TFAW value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TRP_F1	R/W	0h	DRAM TRP value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.102 EMIF_CTLCFG_DENALI_CTL_51 Register

1 EMIF_CTLCFG_DENALI_CTL_51 Register (Offset = CCh) [reset = 0h]

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Table 14-12661. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80CCh**

Figure 14-4181. EMIF_CTLCFG_DENALI_CTL_51 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRC_F2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
TRC_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TRRD_L_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TRRD_F2							
R/W							
0h							

Table 14-12663. EMIF_CTLCFG_DENALI_CTL_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	TRC_F2	R/W	0h	DRAM TRC value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TRRD_L_F2	R/W	0h	DRAM TRRD_L value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TRRD_F2	R/W	0h	DRAM TRRD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.103 EMIF_CTLCFG_DENALI_CTL_52 Register

1 EMIF_CTLCFG_DENALI_CTL_52 Register (Offset = D0h) [reset = 0h]

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Table 14-12664. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 80D0h

Figure 14-4182. EMIF_CTLCFG_DENALI_CTL_52 Name Register

31	30	29	28	27	26	25	24
RESERVED		TWTR_L_F2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TWTR_F2					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TRAS_MIN_F2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRAS_MIN_F2							
R/W							
0h							

Table 14-12666. EMIF_CTLCFG_DENALI_CTL_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TWTR_L_F2	R/W	0h	DRAM TWTR_L value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	TWTR_F2	R/W	0h	DRAM TWTR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	TRAS_MIN_F2	R/W	0h	DRAM TRAS_MIN value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.104 EMIF_CTLCFG_DENALI_CTL_53 Register

1 EMIF_CTLCFG_DENALI_CTL_53 Register (Offset = D4h) [reset = 0h]

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Table 14-12667. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80D4h**

Figure 14-4183. EMIF_CTLCFG_DENALI_CTL_53 Name Register

31	30	29	28	27	26	25	24
TRTP_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							TFAW_F2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TFAW_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRP_F2							
R/W							
0h							

Table 14-12669. EMIF_CTLCFG_DENALI_CTL_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRTP_F0	R/W	0h	DRAM TRTP value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	TFAW_F2	R/W	0h	DRAM TFAW value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TRP_F2	R/W	0h	DRAM TRP value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.105 EMIF_CTLCFG_DENALI_CTL_54 Register

1 EMIF_CTLCFG_DENALI_CTL_54 Register (Offset = D8h) [reset = 0h]

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Table 14-12670. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80D8h**

Figure 14-4184. EMIF_CTLCFG_DENALI_CTL_54 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TMOD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TMRD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TRTP_AP_F0							
R/W							
0h							

Table 14-12672. EMIF_CTLCFG_DENALI_CTL_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TMOD_F0	R/W	0h	Number of cycles after MRS command and before any other command. FC=0 Reset Source: ctl_amod_g_rst_n
15:8	TMRD_F0	R/W	0h	DRAM TMRD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TRTP_AP_F0	R/W	0h	DRAM TRTP for auto-precharge value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.106 EMIF_CTLCFG_DENALI_CTL_55 Register

1 EMIF_CTLCFG_DENALI_CTL_55 Register (Offset = DCh) [reset = 0h]

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Table 14-12673. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80DCh**

Figure 14-4185. EMIF_CTLCFG_DENALI_CTL_55 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKE_F0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TRAS_MAX_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRAS_MAX_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRAS_MAX_F0							
R/W							
0h							

Table 14-12675. EMIF_CTLCFG_DENALI_CTL_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKE_F0	R/W	0h	Minimum CKE pulse width. FC=0 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TRAS_MAX_F0	R/W	0h	DRAM TRAS_MAX value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.107 EMIF_CTLCFG_DENALI_CTL_56 Register

1 EMIF_CTLCFG_DENALI_CTL_56 Register (Offset = E0h) [reset = 0h]

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Table 14-12676. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80E0h**

Figure 14-4186. EMIF_CTLCFG_DENALI_CTL_56 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TRTP_AP_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TRTP_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TCCDMW_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TCKESR_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12678. EMIF_CTLCFG_DENALI_CTL_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRTP_AP_F1	R/W	0h	DRAM TRTP for auto-precharge value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TRTP_F1	R/W	0h	DRAM TRTP value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	TCCDMW_F0	R/W	0h	DRAM CAS-to-CAS masked write value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TCKESR_F0	R/W	0h	Minimum CKE low pulse width during a self-refresh. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.108 EMIF_CTLCFG_DENALI_CTL_57 Register

1 EMIF_CTLCFG_DENALI_CTL_57 Register (Offset = E4h) [reset = 0h]

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Table 14-12679. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80E4h**

Figure 14-4187. EMIF_CTLCFG_DENALI_CTL_57 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TMOD_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMRD_F1							
R/W							
0h							

Table 14-12681. EMIF_CTLCFG_DENALI_CTL_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TMOD_F1	R/W	0h	Number of cycles after MRS command and before any other command. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TMRD_F1	R/W	0h	DRAM TMRD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.109 EMIF_CTLCFG_DENALI_CTL_58 Register

1 EMIF_CTLCFG_DENALI_CTL_58 Register (Offset = E8h) [reset = 0h]

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Table 14-12682. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80E8h**

Figure 14-4188. EMIF_CTLCFG_DENALI_CTL_58 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCKE_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRAS_MAX_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TRAS_MAX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRAS_MAX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12684. EMIF_CTLCFG_DENALI_CTL_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKE_F1	R/W	0h	Minimum CKE pulse width. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TRAS_MAX_F1	R/W	0h	DRAM TRAS_MAX value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.110 EMIF_CTLCFG_DENALI_CTL_59 Register

1 EMIF_CTLCFG_DENALI_CTL_59 Register (Offset = ECh) [reset = 0h]

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Table 14-12685. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 80ECh

Figure 14-4189. EMIF_CTLCFG_DENALI_CTL_59 Name Register

31	30	29	28	27	26	25	24
TRTP_AP_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TRTP_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED		TCCDMW_F1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
TCKESR_F1							
R/W							
0h							

Table 14-12687. EMIF_CTLCFG_DENALI_CTL_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRTP_AP_F2	R/W	0h	DRAM TRTP for auto-precharge value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TRTP_F2	R/W	0h	DRAM TRTP value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	TCCDMW_F1	R/W	0h	DRAM CAS-to-CAS masked write value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TCKESR_F1	R/W	0h	Minimum CKE low pulse width during a self-refresh. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.111 EMIF_CTLCFG_DENALI_CTL_60 Register

1 EMIF_CTLCFG_DENALI_CTL_60 Register (Offset = F0h) [reset = 0h]

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Table 14-12688. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 80F0h

Figure 14-4190. EMIF_CTLCFG_DENALI_CTL_60 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TMOD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TMRD_F2							
R/W							
0h							

Table 14-12690. EMIF_CTLCFG_DENALI_CTL_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TMOD_F2	R/W	0h	Number of cycles after MRS command and before any other command. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TMRD_F2	R/W	0h	DRAM TMRD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.112 EMIF_CTLCFG_DENALI_CTL_61 Register

1 EMIF_CTLCFG_DENALI_CTL_61 Register (Offset = F4h) [reset = 0h]

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Table 14-12691. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80F4h**

Figure 14-4191. EMIF_CTLCFG_DENALI_CTL_61 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCKE_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRAS_MAX_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TRAS_MAX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRAS_MAX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12693. EMIF_CTLCFG_DENALI_CTL_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKE_F2	R/W	0h	Minimum CKE pulse width. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TRAS_MAX_F2	R/W	0h	DRAM TRAS_MAX value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.113 EMIF_CTLCFG_DENALI_CTL_62 Register

1 EMIF_CTLCFG_DENALI_CTL_62 Register (Offset = F8h) [reset = 40000h]

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Table 14-12694. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80F8h**

Figure 14-4192. EMIF_CTLCFG_DENALI_CTL_62 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MC_RESERVED0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TPPD</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TCCDMW_F2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TCKESR_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12696. EMIF_CTLCFG_DENALI_CTL_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	MC_RESERVED0	R/W	0h	Reserved
23:19	RESERVED	NONE	0h	Reserved
18:16	TPPD	R/W	4h	DRAM TPPD value in cycles. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	TCCDMW_F2	R/W	0h	DRAM CAS-to-CAS masked write value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TCKESR_F2	R/W	0h	Minimum CKE low pulse width during a self-refresh. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.114 EMIF_CTLCFG_DENALI_CTL_63 Register

1 EMIF_CTLCFG_DENALI_CTL_63 Register (Offset = FCh) [reset = 0h]

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Table 14-12697. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 80FCh**

Figure 14-4193. EMIF_CTLCFG_DENALI_CTL_63 Name Register

31	30	29	28	27	26	25	24
TWR_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TRCD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							WRITEINTERP
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					MC_RESERVED1		
NONE					R/W		
0h					0h		

Table 14-12699. EMIF_CTLCFG_DENALI_CTL_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TWR_F0	R/W	0h	DRAM TWR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TRCD_F0	R/W	0h	DRAM TRCD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	WRITEINTERP	R/W	0h	Allow controller to interrupt a write burst to the DRAMs with a read command. Set to 1 to allow interruption. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MC_RESERVED1	R/W	0h	Reserved

14.5.1.2.115 EMIF_CTLCFG_DENALI_CTL_64 Register

1 EMIF_CTLCFG_DENALI_CTL_64 Register (Offset = 100h) [reset = 0h]

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Table 14-12700. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8100h**

Figure 14-4194. EMIF_CTLCFG_DENALI_CTL_64 Name Register

31	30	29	28	27	26	25	24
TWR_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TRCD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TWR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TRCD_F1							
R/W							
0h							

Table 14-12702. EMIF_CTLCFG_DENALI_CTL_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TWR_F2	R/W	0h	DRAM TWR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TRCD_F2	R/W	0h	DRAM TRCD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TWR_F1	R/W	0h	DRAM TWR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TRCD_F1	R/W	0h	DRAM TRCD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.116 EMIF_CTLCFG_DENALI_CTL_65 Register

1 EMIF_CTLCFG_DENALI_CTL_65 Register (Offset = 104h) [reset = 0h]

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Table 14-12703. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8104h**

Figure 14-4195. EMIF_CTLCFG_DENALI_CTL_65 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRAS_LOCKOUT
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							CONCURRENTAP
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							AP
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TMRR			
NONE				R/W			
0h				0h			

Table 14-12705. EMIF_CTLCFG_DENALI_CTL_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRAS_LOCKOUT	R/W	0h	IF the DRAM supports it, this allows the controller to execute auto pre-charge commands before the TRAS_MIN parameter expires. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	CONCURRENTAP	R/W	0h	IF the DRAM supports it, this allows the controller to issue commands to other banks while a bank is in auto pre-charge. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	AP	R/W	0h	Enable auto pre-charge mode of controller. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TMRR	R/W	0h	DRAM TMRR value in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.117 EMIF_CTLCFG_DENALI_CTL_66 Register

1 EMIF_CTLCFG_DENALI_CTL_66 Register (Offset = 108h) [reset = 2000000h]

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Table 14-12706. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8108h**

Figure 14-4196. EMIF_CTLCFG_DENALI_CTL_66 Name Register

31	30	29	28	27	26	25	24
RESERVED		BSTLEN					
NONE		R/W					
0h		2h					
23	22	21	20	19	18	17	16
TDAL_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDAL_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDAL_F0							
R/W							
0h							

Table 14-12708. EMIF_CTLCFG_DENALI_CTL_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	BSTLEN	R/W	2h	Encoded burst length sent to DRAMs during initialization. Program to 1 for BL2, program to 2 for BL4, program to 3 for BL8, program to 4 for BL16, or program to 5 for BL32. All other settings are reserved. Reset Source: ctl_amod_g_rst_n
23:16	TDAL_F2	R/W	0h	DRAM TDAL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TDAL_F1	R/W	0h	DRAM TDAL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TDAL_F0	R/W	0h	DRAM TDAL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.118 EMIF_CTLCFG_DENALI_CTL_67 Register

1 EMIF_CTLCFG_DENALI_CTL_67 Register (Offset = 10Ch) [reset = 0h]

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Table 14-12709. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 810Ch**

Figure 14-4197. EMIF_CTLCFG_DENALI_CTL_67 Name Register

31	30	29	28	27	26	25	24
TRP_AB_F0_1							
R/W							
0h							
23	22	21	20	19	18	17	16
TRP_AB_F2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
TRP_AB_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
TRP_AB_F0_0							
R/W							
0h							

Table 14-12711. EMIF_CTLCFG_DENALI_CTL_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TRP_AB_F0_1	R/W	0h	DRAM TRP all bank value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TRP_AB_F2_0	R/W	0h	DRAM TRP all bank value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TRP_AB_F1_0	R/W	0h	DRAM TRP all bank value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TRP_AB_F0_0	R/W	0h	DRAM TRP all bank value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.119 EMIF_CTLCFG_DENALI_CTL_68 Register

1 EMIF_CTLCFG_DENALI_CTL_68 Register (Offset = 110h) [reset = 0h]

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Table 14-12712. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8110h**

Figure 14-4198. EMIF_CTLCFG_DENALI_CTL_68 Name Register

31	30	29	28	27	26	25	24
RESERVED						ADDRESS_MIRRORING	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							REG_DIMM_ENABLE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRP_AB_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRP_AB_F1_1							
R/W							
0h							

Table 14-12714. EMIF_CTLCFG_DENALI_CTL_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	ADDRESS_MIRRORING	R/W	0h	Indicates which chip selects support address mirroring. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	REG_DIMM_ENABLE	R/W	0h	Enable registered DIMM operation of the controller. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:8	TRP_AB_F2_1	R/W	0h	DRAM TRP all bank value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TRP_AB_F1_1	R/W	0h	DRAM TRP all bank value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.120 EMIF_CTLCFG_DENALI_CTL_69 Register

1 EMIF_CTLCFG_DENALI_CTL_69 Register (Offset = 114h) [reset = 0h]

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Table 14-12715. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8114h**

Figure 14-4199. EMIF_CTLCFG_DENALI_CTL_69 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							NO_MEMORY_DM
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							MC_RESERVED2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							OPTIMAL_RMODW_EN
NONE							R/W
0h							0h

Table 14-12717. EMIF_CTLCFG_DENALI_CTL_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	NO_MEMORY_DM	R/W	0h	Indicates that the external DRAM does not support DM masking. Set to 1 for no DM masking at the DRAM. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	MC_RESERVED2	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	OPTIMAL_RMODW_EN	R/W	0h	Enables optimized RMODW logic in the controller. A value of 1 enables optimized RMODW operation. All RMODW operations are still supported in a non-optimal manner when the value is 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.121 *EMIF_CTLCFG_DENALI_CTL_70 Register*

1 EMIF_CTLCFG_DENALI_CTL_70 Register (Offset = 118h) [reset = 0h]

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Table 14-12718. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8118h**

Figure 14-4200. EMIF_CTLCFG_DENALI_CTL_70 Name Register

31	30	29	28	27	26	25	24
RESERVED						CA_PARITY_ERROR_INJECT	
NONE						R/W	
0h						0h	

23	22	21	20	19	18	17	16
CA_PARITY_ERROR_INJECT							
R/W							
0h							

15	14	13	12	11	10	9	8
CA_PARITY_ERROR_INJECT							
R/W							
0h							

7	6	5	4	3	2	1	0
CA_PARITY_ERROR_INJECT							
R/W							
0h							

Table 14-12720. EMIF_CTLCFG_DENALI_CTL_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:0	CA_PARITY_ERROR_INJECT	R/W	0h	Selects bit to corrupt on the CA bus for CA parity error injection. Reset Source: ctl_amod_g_rst_n

14.5.1.2.122 EMIF_CTLCFG_DENALI_CTL_71 Register

1 EMIF_CTLCFG_DENALI_CTL_71 Register (Offset = 11Ch) [reset = 0h]

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Table 14-12721. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 811Ch**

Figure 14-4201. EMIF_CTLCFG_DENALI_CTL_71 Name Register

31	30	29	28	27	26	25	24
RESERVED							TREF_ENABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							AREF_STATUS
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							AREFRESH
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CA_PARITY_ERROR
NONE							R
0h							0h

Table 14-12723. EMIF_CTLCFG_DENALI_CTL_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TREF_ENABLE	R/W	0h	Issue auto-refresh commands to the DRAMs at the interval defined in the TREF parameter. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	AREF_STATUS	R	0h	Indicates a SR error associated with the AREF interrupt. Value of 1 indicates a violation. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	AREFRESH	W	0h	Initiate auto-refresh at the end of the current burst boundary. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	CA_PARITY_ERROR	R	0h	Contains one hot indication of registered DIMM parity errors. Value of 1 indicates an error on that DIMM. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.123 EMIF_CTLCFG_DENALI_CTL_72 Register

1 EMIF_CTLCFG_DENALI_CTL_72 Register (Offset = 120h) [reset = 0h]

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Table 14-12724. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8120h**

Figure 14-4202. EMIF_CTLCFG_DENALI_CTL_72 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TRFC_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TRFC_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">CS_COMPARISON_FOR_REFRESH_DEPTH</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TRFC_OPT_THRESHOLD</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-12726. EMIF_CTLCFG_DENALI_CTL_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TRFC_F0	R/W	0h	DRAM TRFC value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	CS_COMPARISON_FOR_REFRESH_DEPTH	R/W	0h	Defines the number of entries of the command queue that the refresh logic will consider for sending a refresh command. A non-zero value limits the decode to a subset of the full command pipeline. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TRFC_OPT_THRESHOLD	R/W	0h	Number of clocks before TRFC expires when the refresh task will deassert its request for optimal command to command turn-around timing. Reset Source: ctl_amod_g_rst_n

14.5.1.2.124 EMIF_CTLCFG_DENALI_CTL_73 Register

1 EMIF_CTLCFG_DENALI_CTL_73 Register (Offset = 124h) [reset = 0h]

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Table 14-12727. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8124h**

Figure 14-4203. EMIF_CTLCFG_DENALI_CTL_73 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TREF_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TREF_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TREF_F0							
R/W							
0h							

Table 14-12729. EMIF_CTLCFG_DENALI_CTL_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREF_F0	R/W	0h	DRAM TREF value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.125 EMIF_CTLCFG_DENALI_CTL_74 Register

1 EMIF_CTLCFG_DENALI_CTL_74 Register (Offset = 128h) [reset = 0h]

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Table 14-12730. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8128h**

Figure 14-4204. EMIF_CTLCFG_DENALI_CTL_74 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TRFC_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TRFC_F1							
R/W							
0h							

Table 14-12732. EMIF_CTLCFG_DENALI_CTL_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_F1	R/W	0h	DRAM TRFC value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.126 EMIF_CTLCFG_DENALI_CTL_75 Register

1 EMIF_CTLCFG_DENALI_CTL_75 Register (Offset = 12Ch) [reset = 0h]

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Table 14-12733. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 812Ch**

Figure 14-4205. EMIF_CTLCFG_DENALI_CTL_75 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TREF_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TREF_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TREF_F1							
R/W							
0h							

Table 14-12735. EMIF_CTLCFG_DENALI_CTL_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREF_F1	R/W	0h	DRAM TREF value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.127 EMIF_CTLCFG_DENALI_CTL_76 Register

1 EMIF_CTLCFG_DENALI_CTL_76 Register (Offset = 130h) [reset = 0h]

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Table 14-12736. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8130h**

Figure 14-4206. EMIF_CTLCFG_DENALI_CTL_76 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TRFC_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRFC_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12738. EMIF_CTLCFG_DENALI_CTL_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_F2	R/W	0h	DRAM TRFC value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.128 EMIF_CTLCFG_DENALI_CTL_77 Register

1 EMIF_CTLCFG_DENALI_CTL_77 Register (Offset = 134h) [reset = 0h]

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Table 14-12739. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8134h**

Figure 14-4207. EMIF_CTLCFG_DENALI_CTL_77 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TREF_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TREF_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TREF_F2							
R/W							
0h							

Table 14-12741. EMIF_CTLCFG_DENALI_CTL_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREF_F2	R/W	0h	DRAM TREF value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.129 *EMIF_CTLCFG_DENALI_CTL_78 Register*

1 EMIF_CTLCFG_DENALI_CTL_78 Register (Offset = 138h) [reset = 0h]

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Table 14-12742. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8138h**

Figure 14-4208. EMIF_CTLCFG_DENALI_CTL_78 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TREF_INTERVAL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TREF_INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TREF_INTERVAL							
R/W							
0h							

Table 14-12744. EMIF_CTLCFG_DENALI_CTL_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREF_INTERVAL	R/W	0h	Defines the cycles between refreshes to different chip selects. Reset Source: ctl_amod_g_rst_n

14.5.1.2.130 EMIF_CTLCFG_DENALI_CTL_79 Register

1 EMIF_CTLCFG_DENALI_CTL_79 Register (Offset = 13Ch) [reset = 0h]

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Table 14-12745. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 813Ch**

Figure 14-4209. EMIF_CTLCFG_DENALI_CTL_79 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TRFC_PB_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TRFC_PB_F0							
R/W							
0h							

Table 14-12747. EMIF_CTLCFG_DENALI_CTL_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_PB_F0	R/W	0h	DRAM TRFC_PB value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.131 EMIF_CTLCFG_DENALI_CTL_80 Register

1 EMIF_CTLCFG_DENALI_CTL_80 Register (Offset = 140h) [reset = 0h]

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Table 14-12748. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8140h**

Figure 14-4210. EMIF_CTLCFG_DENALI_CTL_80 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TREFI_PB_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TREFI_PB_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TREFI_PB_F0							
R/W							
0h							

Table 14-12750. EMIF_CTLCFG_DENALI_CTL_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREFI_PB_F0	R/W	0h	DRAM TREFI_PB value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.132 EMIF_CTLCFG_DENALI_CTL_81 Register

1 EMIF_CTLCFG_DENALI_CTL_81 Register (Offset = 144h) [reset = 0h]

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Table 14-12751. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8144h**

Figure 14-4211. EMIF_CTLCFG_DENALI_CTL_81 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TRFC_PB_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TRFC_PB_F1							
R/W							
0h							

Table 14-12753. EMIF_CTLCFG_DENALI_CTL_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_PB_F1	R/W	0h	DRAM TRFC_PB value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.133 EMIF_CTLCFG_DENALI_CTL_82 Register

1 EMIF_CTLCFG_DENALI_CTL_82 Register (Offset = 148h) [reset = 0h]

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Table 14-12754. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8148h**

Figure 14-4212. EMIF_CTLCFG_DENALI_CTL_82 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TREFI_PB_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TREFI_PB_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TREFI_PB_F1							
R/W							
0h							

Table 14-12756. EMIF_CTLCFG_DENALI_CTL_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TREFI_PB_F1	R/W	0h	DRAM TREFI_PB value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.134 EMIF_CTLCFG_DENALI_CTL_83 Register

1 EMIF_CTLCFG_DENALI_CTL_83 Register (Offset = 14Ch) [reset = 0h]

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Table 14-12757. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 814Ch**

Figure 14-4213. EMIF_CTLCFG_DENALI_CTL_83 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TRFC_PB_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TRFC_PB_F2							
R/W							
0h							

Table 14-12759. EMIF_CTLCFG_DENALI_CTL_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TRFC_PB_F2	R/W	0h	DRAM TRFC_PB value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.135 EMIF_CTLCFG_DENALI_CTL_84 Register

1 EMIF_CTLCFG_DENALI_CTL_84 Register (Offset = 150h) [reset = 0h]

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Table 14-12760. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8150h**

Figure 14-4214. EMIF_CTLCFG_DENALI_CTL_84 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PBR_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TREFI_PB_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TREFI_PB_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TREFI_PB_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12762. EMIF_CTLCFG_DENALI_CTL_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PBR_EN	R/W	0h	Enables the per-bank refresh feature. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TREFI_PB_F2	R/W	0h	DRAM TREFI_PB value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.136 EMIF_CTLCFG_DENALI_CTL_85 Register

1 EMIF_CTLCFG_DENALI_CTL_85 Register (Offset = 154h) [reset = 0h]

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Table 14-12763. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8154h**

Figure 14-4215. EMIF_CTLCFG_DENALI_CTL_85 Name Register

31	30	29	28	27	26	25	24
RESERVED				PBR_BANK_SELECT_DELAY			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PBR_MAX_BANK_WAIT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PBR_MAX_BANK_WAIT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PBR_NUMERIC_ORDER
NONE							R/W
0h							0h

Table 14-12765. EMIF_CTLCFG_DENALI_CTL_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PBR_BANK_SELECT_DELAY	R/W	0h	Defines the PBR bank select to command delay, the time from bank selection to when the command queue bank selection logic is guaranteed to have blocked the bank. Reset Source: ctl_amod_g_rst_n
23:8	PBR_MAX_BANK_WAIT	R/W	0h	Defines the maximum number of cycles that the PBR module will wait for Strategy to release the target bank until the PBR will assert the inhibit and close the target bank. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PBR_NUMERIC_ORDER	R/W	0h	Enables the PBR to run REFpb commands in numeric bank order [0,1,2,3, etc.] When disabled, the order may be modified if supported by the memory type. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.137 EMIF_CTLCFG_DENALI_CTL_86 Register

1 EMIF_CTLCFG_DENALI_CTL_86 Register (Offset = 158h) [reset = 0h]

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Table 14-12766. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8158h**

Figure 14-4216. EMIF_CTLCFG_DENALI_CTL_86 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			AREF_PBR_CONT_DIS_THRESHOLD				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			AREF_PBR_CONT_EN_THRESHOLD				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PBR_CONT_REQ_EN
NONE							R/W
0h							0h

Table 14-12768. EMIF_CTLCFG_DENALI_CTL_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	AREF_PBR_CONT_DIS_THRESHOLD	R/W	0h	Sets the auto-refresh request count threshold when the PBR continuous refresh request enable will be deasserted. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	AREF_PBR_CONT_EN_THRESHOLD	R/W	0h	Sets the auto-refresh request count threshold when the PBR continuous refresh request enable will be asserted. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PBR_CONT_REQ_EN	R/W	0h	Enables the per-bank refresh continuous request feature. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.138 EMIF_CTLCFG_DENALI_CTL_87 Register

1 EMIF_CTLCFG_DENALI_CTL_87 Register (Offset = 15Ch) [reset = 0h]

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Table 14-12769. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 815Ch**

Figure 14-4217. EMIF_CTLCFG_DENALI_CTL_87 Name Register

31	30	29	28	27	26	25	24
TPDEX_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TPDEX_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TPDEX_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TPDEX_F0							
R/W							
0h							

Table 14-12771. EMIF_CTLCFG_DENALI_CTL_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TPDEX_F1	R/W	0h	DRAM TPDEX value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	TPDEX_F0	R/W	0h	DRAM TPDEX value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.139 EMIF_CTLCFG_DENALI_CTL_88 Register

1 EMIF_CTLCFG_DENALI_CTL_88 Register (Offset = 160h) [reset = 0h]

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Table 14-12772. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8160h**

Figure 14-4218. EMIF_CTLCFG_DENALI_CTL_88 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TPDEX_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TPDEX_F2							
R/W							
0h							

Table 14-12774. EMIF_CTLCFG_DENALI_CTL_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TPDEX_F2	R/W	0h	DRAM TPDEX value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.140 EMIF_CTLCFG_DENALI_CTL_89 Register

1 EMIF_CTLCFG_DENALI_CTL_89 Register (Offset = 164h) [reset = 0h]

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Table 14-12775. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8164h**

Figure 14-4219. EMIF_CTLCFG_DENALI_CTL_89 Name Register

31	30	29	28	27	26	25	24
CTL_UNUSED_REG_0							
R							
0h							
23	22	21	20	19	18	17	16
CTL_UNUSED_REG_0							
R							
0h							
15	14	13	12	11	10	9	8
CTL_UNUSED_REG_0							
R							
0h							
7	6	5	4	3	2	1	0
CTL_UNUSED_REG_0							
R							
0h							

Table 14-12777. EMIF_CTLCFG_DENALI_CTL_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTL_UNUSED_REG_0	R	0h	Place-holder for register map preservation Reset Source: ctl_amod_g_rst_n

14.5.1.2.141 EMIF_CTLCFG_DENALI_CTL_90 Register

1 EMIF_CTLCFG_DENALI_CTL_90 Register (Offset = 168h) [reset = 0h]

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Table 14-12778. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8168h**

Figure 14-4220. EMIF_CTLCFG_DENALI_CTL_90 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKELCS_F0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TMRRI_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TMRRI_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMRRI_F0							
R/W							
0h							

Table 14-12780. EMIF_CTLCFG_DENALI_CTL_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKELCS_F0	R/W	0h	DRAM TCKELCS value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TMRRI_F2	R/W	0h	DRAM TMRRI value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TMRRI_F1	R/W	0h	DRAM TMRRI value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TMRRI_F0	R/W	0h	DRAM TMRRI value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.142 EMIF_CTLCFG_DENALI_CTL_91 Register

1 EMIF_CTLCFG_DENALI_CTL_91 Register (Offset = 16Ch) [reset = 0h]

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Table 14-12781. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 816Ch

Figure 14-4221. EMIF_CTLCFG_DENALI_CTL_91 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKELCS_F1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED				TZQCKE_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED			TMRWCKEL_F0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			TCKEHCS_F0				
NONE			R/W				
0h			0h				

Table 14-12783. EMIF_CTLCFG_DENALI_CTL_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKELCS_F1	R/W	0h	DRAM TCKELCS value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TZQCKE_F0	R/W	0h	DRAM TZQCKE value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TMRWCKEL_F0	R/W	0h	DRAM TMRWCKEL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKEHCS_F0	R/W	0h	DRAM TCKEHCS value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.143 EMIF_CTLCFG_DENALI_CTL_92 Register

1 EMIF_CTLCFG_DENALI_CTL_92 Register (Offset = 170h) [reset = 0h]

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Table 14-12784. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8170h**

Figure 14-4222. EMIF_CTLCFG_DENALI_CTL_92 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCKELCS_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TZQCKE_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TMRWCKEL_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TCKEHCS_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-12786. EMIF_CTLCFG_DENALI_CTL_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKELCS_F2	R/W	0h	DRAM TCKELCS value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TZQCKE_F1	R/W	0h	DRAM TZQCKE value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TMRWCKEL_F1	R/W	0h	DRAM TMRWCKEL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKEHCS_F1	R/W	0h	DRAM TCKEHCS value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.144 EMIF_CTLCFG_DENALI_CTL_93 Register

1 EMIF_CTLCFG_DENALI_CTL_93 Register (Offset = 174h) [reset = 0h]

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Table 14-12787. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8174h

Figure 14-4223. EMIF_CTLCFG_DENALI_CTL_93 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCSCKE_F0				
NONE			R/W				
0h			0h				

23	22	21	20	19	18	17	16
RESERVED				TZQCKE_F2			
NONE				R/W			
0h				0h			

15	14	13	12	11	10	9	8
RESERVED			TMRWCKEL_F2				
NONE			R/W				
0h			0h				

7	6	5	4	3	2	1	0
RESERVED			TCKEHCS_F2				
NONE			R/W				
0h			0h				

Table 14-12789. EMIF_CTLCFG_DENALI_CTL_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCSCKE_F0	R/W	0h	DRAM TCSCKE value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TZQCKE_F2	R/W	0h	DRAM TZQCKE value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TMRWCKEL_F2	R/W	0h	DRAM TMRWCKEL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKEHCS_F2	R/W	0h	DRAM TCKEHCS value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.145 EMIF_CTLCFG_DENALI_CTL_94 Register

1 EMIF_CTLCFG_DENALI_CTL_94 Register (Offset = 178h) [reset = 0h]

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Table 14-12790. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8178h**

Figure 14-4224. EMIF_CTLCFG_DENALI_CTL_94 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCSCKE_F2				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							CA_DEFAULT_VAL_F1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			TCSCKE_F1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED							CA_DEFAULT_VAL_F0
NONE							R/W
0h							0h

Table 14-12792. EMIF_CTLCFG_DENALI_CTL_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCSCKE_F2	R/W	0h	DRAM TCSCKE value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	CA_DEFAULT_VAL_F1	R/W	0h	Defines how unused address/command bits are driven. Set to 1 to use last value or clear to 0 to drive low. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCSCKE_F1	R/W	0h	DRAM TCSCKE value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	CA_DEFAULT_VAL_F0	R/W	0h	Defines how unused address/command bits are driven. Set to 1 to use last value or clear to 0 to drive low. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.146 EMIF_CTLCFG_DENALI_CTL_95 Register

1 EMIF_CTLCFG_DENALI_CTL_95 Register (Offset = 17Ch) [reset = 0h]

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Table 14-12793. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 817Ch**

Figure 14-4225. EMIF_CTLCFG_DENALI_CTL_95 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TXSR_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TXSR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							CA_DEFAULT_VAL_F2
NONE							R/W
0h							0h

Table 14-12795. EMIF_CTLCFG_DENALI_CTL_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	TXSR_F0	R/W	0h	DRAM TXSR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	CA_DEFAULT_VAL_F2	R/W	0h	Defines how unused address/command bits are driven. Set to 1 to use last value or clear to 0 to drive low. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.147 EMIF_CTLCFG_DENALI_CTL_96 Register

1 EMIF_CTLCFG_DENALI_CTL_96 Register (Offset = 180h) [reset = 0h]

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Table 14-12796. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8180h**

Figure 14-4226. EMIF_CTLCFG_DENALI_CTL_96 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TXSR_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TXSR_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TXSNR_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TXSNR_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12798. EMIF_CTLCFG_DENALI_CTL_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXSR_F1	R/W	0h	DRAM TXSR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	TXSNR_F0	R/W	0h	DRAM TXSNR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.148 EMIF_CTLCFG_DENALI_CTL_97 Register

1 EMIF_CTLCFG_DENALI_CTL_97 Register (Offset = 184h) [reset = 0h]

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Table 14-12799. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8184h**

Figure 14-4227. EMIF_CTLCFG_DENALI_CTL_97 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TXSR_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TXSR_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TXSNR_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TXSNR_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12801. EMIF_CTLCFG_DENALI_CTL_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXSR_F2	R/W	0h	DRAM TXSR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	TXSNR_F1	R/W	0h	DRAM TXSNR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.149 EMIF_CTLCFG_DENALI_CTL_98 Register

1 EMIF_CTLCFG_DENALI_CTL_98 Register (Offset = 188h) [reset = 0h]

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Table 14-12802. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8188h**

Figure 14-4228. EMIF_CTLCFG_DENALI_CTL_98 Name Register

31	30	29	28	27	26	25	24
TXPR_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXPR_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXSNR_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXSNR_F2							
R/W							
0h							

Table 14-12804. EMIF_CTLCFG_DENALI_CTL_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXPR_F0	R/W	0h	DRAM TXPR value in cycles. This parameter defines reset exit time from CKE HIGH to a valid command. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	TXSNR_F2	R/W	0h	DRAM TXSNR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.150 EMIF_CTLCFG_DENALI_CTL_99 Register

1 EMIF_CTLCFG_DENALI_CTL_99 Register (Offset = 18Ch) [reset = 0h]

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Table 14-12805. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 818Ch**

Figure 14-4229. EMIF_CTLCFG_DENALI_CTL_99 Name Register

31	30	29	28	27	26	25	24
TXPR_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TXPR_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TXPR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TXPR_F1							
R/W							
0h							

Table 14-12807. EMIF_CTLCFG_DENALI_CTL_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXPR_F2	R/W	0h	DRAM TXPR value in cycles. This parameter defines reset exit time from CKE HIGH to a valid command. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	TXPR_F1	R/W	0h	DRAM TXPR value in cycles. This parameter defines reset exit time from CKE HIGH to a valid command. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.151 EMIF_CTLCFG_DENALI_CTL_100 Register

1 EMIF_CTLCFG_DENALI_CTL_100 Register (Offset = 190h) [reset = 0h]

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Table 14-12808. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8190h**

Figure 14-4230. EMIF_CTLCFG_DENALI_CTL_100 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKELCMD_F0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCSCKEH_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					TESCKE_F0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSR_F0							
R/W							
0h							

Table 14-12810. EMIF_CTLCFG_DENALI_CTL_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKELCMD_F0	R/W	0h	DRAM TCKELCMD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCSCKEH_F0	R/W	0h	DRAM TCSCKEH value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TESCKE_F0	R/W	0h	DRAM TESCKE value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TSR_F0	R/W	0h	DRAM TSR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.152 EMIF_CTLCFG_DENALI_CTL_101 Register

1 EMIF_CTLCFG_DENALI_CTL_101 Register (Offset = 194h) [reset = 0h]

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Table 14-12811. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8194h**

Figure 14-4231. EMIF_CTLCFG_DENALI_CTL_101 Name Register

31	30	29	28	27	26	25	24
TSR_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKELPD_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TCKCKEL_F0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TCKEHCMD_F0				
NONE			R/W				
0h			0h				

Table 14-12813. EMIF_CTLCFG_DENALI_CTL_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TSR_F1	R/W	0h	DRAM TSR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKELPD_F0	R/W	0h	DRAM TCKELPD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKCKEL_F0	R/W	0h	DRAM TCKCKEL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKEHCMD_F0	R/W	0h	DRAM TCKEHCMD value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.153 EMIF_CTLCFG_DENALI_CTL_102 Register

1 EMIF_CTLCFG_DENALI_CTL_102 Register (Offset = 198h) [reset = 0h]

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Table 14-12814. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8198h**

Figure 14-4232. EMIF_CTLCFG_DENALI_CTL_102 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKEHCMD_F1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKELCMD_F1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TCSCKEH_F1				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TESCKE_F1		
NONE					R/W		
0h					0h		

Table 14-12816. EMIF_CTLCFG_DENALI_CTL_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKEHCMD_F1	R/W	0h	DRAM TCKEHCMD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKELCMD_F1	R/W	0h	DRAM TCKELCMD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCSCKEH_F1	R/W	0h	DRAM TCSCKEH value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TESCKE_F1	R/W	0h	DRAM TESCKE value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.154 EMIF_CTLCFG_DENALI_CTL_103 Register

1 EMIF_CTLCFG_DENALI_CTL_103 Register (Offset = 19Ch) [reset = 0h]

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Table 14-12817. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 819Ch

Figure 14-4233. EMIF_CTLCFG_DENALI_CTL_103 Name Register

31	30	29	28	27	26	25	24
RESERVED					TESCKE_F2		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
TSR_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED			TCKELPD_F1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			TCKCKEL_F1				
NONE			R/W				
0h			0h				

Table 14-12819. EMIF_CTLCFG_DENALI_CTL_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	TESCKE_F2	R/W	0h	DRAM TESCKE value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TSR_F2	R/W	0h	DRAM TSR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKELPD_F1	R/W	0h	DRAM TCKELPD value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKCKEL_F1	R/W	0h	DRAM TCKCKEL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.155 EMIF_CTLCFG_DENALI_CTL_104 Register

1 EMIF_CTLCFG_DENALI_CTL_104 Register (Offset = 1A0h) [reset = 0h]

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Table 14-12820. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 81A0h

Figure 14-4234. EMIF_CTLCFG_DENALI_CTL_104 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKCKEL_F2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKEHCMD_F2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TCKELCMD_F2				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TCSCKEH_F2				
NONE			R/W				
0h			0h				

Table 14-12822. EMIF_CTLCFG_DENALI_CTL_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKCKEL_F2	R/W	0h	DRAM TCKCKEL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKEHCMD_F2	R/W	0h	DRAM TCKEHCMD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCKELCMD_F2	R/W	0h	DRAM TCKELCMD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCSCKEH_F2	R/W	0h	DRAM TCSCKEH value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.156 EMIF_CTLCFG_DENALI_CTL_105 Register

1 EMIF_CTLCFG_DENALI_CTL_105 Register (Offset = 1A4h) [reset = 0h]

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Table 14-12823. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81A4h**

Figure 14-4235. EMIF_CTLCFG_DENALI_CTL_105 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCMDCKE_F2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCMDCKE_F1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TCMDCKE_F0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TCKELPD_F2				
NONE			R/W				
0h			0h				

Table 14-12825. EMIF_CTLCFG_DENALI_CTL_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCMDCKE_F2	R/W	0h	DRAM TCMDCKE value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCMDCKE_F1	R/W	0h	DRAM TCMDCKE value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TCMDCKE_F0	R/W	0h	DRAM TCMDCKE value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TCKELPD_F2	R/W	0h	DRAM TCKELPD value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.157 EMIF_CTLCFG_DENALI_CTL_106 Register

1 EMIF_CTLCFG_DENALI_CTL_106 Register (Offset = 1A8h) [reset = 0h]

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Table 14-12826. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81A8h**

Figure 14-4236. EMIF_CTLCFG_DENALI_CTL_106 Name Register

31	30	29	28	27	26	25	24
RESERVED					CKE_DELAY		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED							ENABLE_QUICK_SREFRESH
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							SREFRESH_EXIT_NO_REFRESH
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PWRUP_SREFRESH_EXIT
NONE							R/W
0h							0h

Table 14-12828. EMIF_CTLCFG_DENALI_CTL_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	CKE_DELAY	R/W	0h	Additional cycles to delay CKE for status reporting. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	ENABLE_QUICK_SREFRESH	R/W	0h	Allow user to interrupt memory initialization to enter self-refresh mode. Set to 1 to allow interruption. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SREFRESH_EXIT_NO_REFRESH	R/W	0h	Disables the automatic refresh request associated with self-refresh exit. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PWRUP_SREFRESH_EXIT	R/W	0h	Allow powerup via self-refresh instead of full memory initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.158 EMIF_CTLCFG_DENALI_CTL_107 Register

1 EMIF_CTLCFG_DENALI_CTL_107 Register (Offset = 1ACh) [reset = 0h]

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Table 14-12829. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81ACh**

Figure 14-4237. EMIF_CTLCFG_DENALI_CTL_107 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							DFS_ZQ_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED	DFS_STATUS						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DFS_CMD				
NONE			W				
0h			0h				

Table 14-12831. EMIF_CTLCFG_DENALI_CTL_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	DFS_ZQ_EN	R/W	0h	Enables ZQ calibration across all ranks during a DFS exit. Set to 1 to enable. Not valid when operating in ZQ background mode. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	DFS_STATUS	R/W	0h	Contains status and interrupt information related to DFS. Bit [0] set indicates that the DFS request from the hardware interface was ignored because param_dfs_enable was zero or because another HWI-initiated DFS operation was already in progress. Bit [1] set indicates that a DFS operation initiated by the hardware interface was terminated because the PHY did not deassert dfi_init_complete within tDFI_INIT_START after the controller asserted dfi_init_start. Bit [2] set indicates that a hardware interface initiated DFS operation completed successfully. Bit [3] set indicates that the DFS command on the software interface was ignored either because param_dfs_enable was zero or because another SW-initiated DFS operation was already in progress. Bit [4] set indicates that a DFS operation initiated by the software interface was terminated because the PHY did not deassert dfi_init_complete within tDFI_INIT_START after the controller asserted dfi_init_start. Bit [5] set indicates that a software initiated DFS operation completed successfully. Bit [6] set indicates that the DFS logic entered the software wait state after a DFS operation completed. Clear this bit to allow the logic to exit this wait state. Reset Source: ctl_amod_g_rst_n

Table 14-12831. EMIF_CTLCFG_DENALI_CTL_107 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:5	RESERVED	NONE	0h	Reserved
4:0	DFS_CMD	W	0h	It Currently not supported gt DFS software command request interface. Bit [0] sends the DFS exit request when set. Bit [1] sends the DFS enter request when set. Bit [2] tells the controller to gate the memory clock before handing control to the PHY during a DFS operation. Bits [4 Reset Source: ctl_amod_g_rst_n

14.5.1.2.159 EMIF_CTLCFG_DENALI_CTL_108 Register

1 EMIF_CTLCFG_DENALI_CTL_108 Register (Offset = 1B0h) [reset = 0h]

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Table 14-12832. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81B0h**

Figure 14-4238. EMIF_CTLCFG_DENALI_CTL_108 Name Register

31	30	29	28	27	26	25	24
DFS_PROMOTE_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PROMOTE_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-12834. EMIF_CTLCFG_DENALI_CTL_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DFS_PROMOTE_THRESHOLD_F1	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 1. Applies to SW and HW DFS commands. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	DFS_PROMOTE_THRESHOLD_F0	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 0. Applies to SW and HW DFS commands. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.160 EMIF_CTLCFG_DENALI_CTL_109 Register

1 EMIF_CTLCFG_DENALI_CTL_109 Register (Offset = 1B4h) [reset = 0h]

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Table 14-12835. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81B4h**

Figure 14-4239. EMIF_CTLCFG_DENALI_CTL_109 Name Register

31	30	29	28	27	26	25	24
RESERVED					MC_RESERVED3		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED					ZQ_STATUS_LOG		
NONE					R		
0h					0h		
15	14	13	12	11	10	9	8
DFS_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-12837. EMIF_CTLCFG_DENALI_CTL_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	MC_RESERVED3	R/W	0h	Reserved
23:19	RESERVED	NONE	0h	Reserved
18:16	ZQ_STATUS_LOG	R	0h	Indicates what kind of ZQ command was terminated without execution that caused the ZQ status interrupt to assert. Bit [0] correlates to a ZQ cal init, reset, short or long command. Bit [1] correlates to a ZQ cal start command. Bit [2] correlates to a ZQ cal latch command. Value of 1 indicates that that type of command was received, but terminated without execution. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	DFS_PROMOTE_THRESHOLD_F2	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW and HW DFS commands. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.161 EMIF_CTLCFG_DENALI_CTL_110 Register

1 EMIF_CTLCFG_DENALI_CTL_110 Register (Offset = 1B8h) [reset = 0h]

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Table 14-12838. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81B8h**

Figure 14-4240. EMIF_CTLCFG_DENALI_CTL_110 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MC_RESERVED7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MC_RESERVED6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MC_RESERVED5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MC_RESERVED4</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-12840. EMIF_CTLCFG_DENALI_CTL_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MC_RESERVED7	R/W	0h	Reserved
23:16	MC_RESERVED6	R/W	0h	Reserved
15:8	MC_RESERVED5	R/W	0h	Reserved
7:3	RESERVED	NONE	0h	Reserved
2:0	MC_RESERVED4	R/W	0h	Reserved

14.5.1.2.162 EMIF_CTLCFG_DENALI_CTL_111 Register

1 EMIF_CTLCFG_DENALI_CTL_111 Register (Offset = 1BCh) [reset = 0h]

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Table 14-12841. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81BCh**

Figure 14-4241. EMIF_CTLCFG_DENALI_CTL_111 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_HIGH_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_CTRLUPD_HIGH_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_CTRLUPD_NORM_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_CTRLUPD_NORM_THRESHOLD_F0							
R/W							
0h							

Table 14-12843. EMIF_CTLCFG_DENALI_CTL_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_HIGH_THRESHOLD_F0	R/W	0h	DFI control update number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_NORM_THRESHOLD_F0	R/W	0h	DFI control update number of long counts until the normal priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.163 EMIF_CTLCFG_DENALI_CTL_112 Register

1 EMIF_CTLCFG_DENALI_CTL_112 Register (Offset = 1C0h) [reset = 0h]

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Table 14-12844. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81C0h**

Figure 14-4242. EMIF_CTLCFG_DENALI_CTL_112 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_CTRLUPD_TIMEOUT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_CTRLUPD_TIMEOUT_F0							
R/W							
0h							

Table 14-12846. EMIF_CTLCFG_DENALI_CTL_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F0	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_TIMEOUT_F0	R/W	0h	DFI control update number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.164 EMIF_CTLCFG_DENALI_CTL_113 Register

1 EMIF_CTLCFG_DENALI_CTL_113 Register (Offset = 1C4h) [reset = 0h]

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Table 14-12847. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81C4h**

Figure 14-4243. EMIF_CTLCFG_DENALI_CTL_113 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_NORM_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_CTRLUPD_NORM_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-12849. EMIF_CTLCFG_DENALI_CTL_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_NORM_THRESHOLD_F1	R/W	0h	DFI control update number of long counts until the normal priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F0	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.165 EMIF_CTLCFG_DENALI_CTL_114 Register

1 EMIF_CTLCFG_DENALI_CTL_114 Register (Offset = 1C8h) [reset = 0h]

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Table 14-12850. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81C8h**

Figure 14-4244. EMIF_CTLCFG_DENALI_CTL_114 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_TIMEOUT_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_CTRLUPD_TIMEOUT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_CTRLUPD_HIGH_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_CTRLUPD_HIGH_THRESHOLD_F1							
R/W							
0h							

Table 14-12852. EMIF_CTLCFG_DENALI_CTL_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_TIMEOUT_F1	R/W	0h	DFI control update number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_HIGH_THRESHOLD_F1	R/W	0h	DFI control update number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.166 EMIF_CTLCFG_DENALI_CTL_115 Register

1 EMIF_CTLCFG_DENALI_CTL_115 Register (Offset = 1CCh) [reset = 0h]

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Table 14-12853. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81CCh**

Figure 14-4245. EMIF_CTLCFG_DENALI_CTL_115 Name Register

31	30	29	28	27	26	25	24
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-12855. EMIF_CTLCFG_DENALI_CTL_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F1	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F1	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.167 EMIF_CTLCFG_DENALI_CTL_116 Register

1 EMIF_CTLCFG_DENALI_CTL_116 Register (Offset = 1D0h) [reset = 0h]

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Table 14-12856. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81D0h**

Figure 14-4246. EMIF_CTLCFG_DENALI_CTL_116 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_HIGH_THRESHOLD_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UPD_CTRLUPD_HIGH_THRESHOLD_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UPD_CTRLUPD_NORM_THRESHOLD_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPD_CTRLUPD_NORM_THRESHOLD_F2							
R/W							
0h							

Table 14-12858. EMIF_CTLCFG_DENALI_CTL_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_HIGH_THRESHOLD_F2	R/W	0h	DFI control update number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_NORM_THRESHOLD_F2	R/W	0h	DFI control update number of long counts until the normal priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.168 EMIF_CTLCFG_DENALI_CTL_117 Register

1 EMIF_CTLCFG_DENALI_CTL_117 Register (Offset = 1D4h) [reset = 0h]

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Table 14-12859. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81D4h**

Figure 14-4247. EMIF_CTLCFG_DENALI_CTL_117 Name Register

31	30	29	28	27	26	25	24
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
UPD_CTRLUPD_TIMEOUT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_CTRLUPD_TIMEOUT_F2							
R/W							
0h							

Table 14-12861. EMIF_CTLCFG_DENALI_CTL_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F2	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	UPD_CTRLUPD_TIMEOUT_F2	R/W	0h	DFI control update number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.169 EMIF_CTLCFG_DENALI_CTL_118 Register

1 EMIF_CTLCFG_DENALI_CTL_118 Register (Offset = 1D8h) [reset = 0h]

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Table 14-12862. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81D8h**

Figure 14-4248. EMIF_CTLCFG_DENALI_CTL_118 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-12864. EMIF_CTLCFG_DENALI_CTL_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F2	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.170 EMIF_CTLCFG_DENALI_CTL_119 Register

1 EMIF_CTLCFG_DENALI_CTL_119 Register (Offset = 1DCh) [reset = 0h]

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Table 14-12865. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81DCh**

Figure 14-4249. EMIF_CTLCFG_DENALI_CTL_119 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYMSTR_MAX_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYMSTR_MAX_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYMSTR_MAX_F0							
R/W							
0h							

Table 14-12867. EMIF_CTLCFG_DENALI_CTL_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_F0	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.171 EMIF_CTLCFG_DENALI_CTL_120 Register

1 EMIF_CTLCFG_DENALI_CTL_120 Register (Offset = 1E0h) [reset = 0h]

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Table 14-12868. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81E0h**

Figure 14-4250. EMIF_CTLCFG_DENALI_CTL_120 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE0_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE0_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE0_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F0							
R/W							
0h							

Table 14-12870. EMIF_CTLCFG_DENALI_CTL_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE0_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.172 EMIF_CTLCFG_DENALI_CTL_121 Register

1 EMIF_CTLCFG_DENALI_CTL_121 Register (Offset = 1E4h) [reset = 0h]

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Table 14-12871. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 81E4h

Figure 14-4251. EMIF_CTLCFG_DENALI_CTL_121 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE1_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE1_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE1_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE1_F0							
R/W							
0h							

Table 14-12873. EMIF_CTLCFG_DENALI_CTL_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE1_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.173 EMIF_CTLCFG_DENALI_CTL_122 Register

1 EMIF_CTLCFG_DENALI_CTL_122 Register (Offset = 1E8h) [reset = 0h]

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Table 14-12874. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81E8h**

Figure 14-4252. EMIF_CTLCFG_DENALI_CTL_122 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE2_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE2_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE2_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F0							
R/W							
0h							

Table 14-12876. EMIF_CTLCFG_DENALI_CTL_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE2_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.174 EMIF_CTLCFG_DENALI_CTL_123 Register

1 EMIF_CTLCFG_DENALI_CTL_123 Register (Offset = 1ECh) [reset = 0h]

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Table 14-12877. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 81ECh

Figure 14-4253. EMIF_CTLCFG_DENALI_CTL_123 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE3_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE3_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE3_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE3_F0							
R/W							
0h							

Table 14-12879. EMIF_CTLCFG_DENALI_CTL_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE3_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.175 EMIF_CTLCFG_DENALI_CTL_124 Register

1 EMIF_CTLCFG_DENALI_CTL_124 Register (Offset = 1F0h) [reset = 0h]

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Table 14-12880. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 81F0h

Figure 14-4254. EMIF_CTLCFG_DENALI_CTL_124 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-12882. EMIF_CTLCFG_DENALI_CTL_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F0	R/W	0h	Defines the DFI[4.0 and 4.0v2] PHY controller request promotion number of regular [not long] counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.176 EMIF_CTLCFG_DENALI_CTL_125 Register

1 EMIF_CTLCFG_DENALI_CTL_125 Register (Offset = 1F4h) [reset = 0h]

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Table 14-12883. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81F4h**

Figure 14-4255. EMIF_CTLCFG_DENALI_CTL_125 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TDFI_PHYMSTR_RESP_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYMSTR_RESP_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYMSTR_RESP_F0							
R/W							
0h							

Table 14-12885. EMIF_CTLCFG_DENALI_CTL_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TDFI_PHYMSTR_RESP_F0	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] to be set to 1 in the PHYMSTR_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.177 EMIF_CTLCFG_DENALI_CTL_126 Register

1 EMIF_CTLCFG_DENALI_CTL_126 Register (Offset = 1F8h) [reset = 0h]

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Table 14-12886. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81F8h**

Figure 14-4256. EMIF_CTLCFG_DENALI_CTL_126 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TDFI_PHYMSTR_MAX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TDFI_PHYMSTR_MAX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDFI_PHYMSTR_MAX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDFI_PHYMSTR_MAX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12888. EMIF_CTLCFG_DENALI_CTL_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_F1	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.178 EMIF_CTLCFG_DENALI_CTL_127 Register

1 EMIF_CTLCFG_DENALI_CTL_127 Register (Offset = 1FCh) [reset = 0h]

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Table 14-12889. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 81FCh**

Figure 14-4257. EMIF_CTLCFG_DENALI_CTL_127 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE0_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE0_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE0_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F1							
R/W							
0h							

Table 14-12891. EMIF_CTLCFG_DENALI_CTL_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE0_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.179 EMIF_CTLCFG_DENALI_CTL_128 Register

1 EMIF_CTLCFG_DENALI_CTL_128 Register (Offset = 200h) [reset = 0h]

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Table 14-12892. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8200h**

Figure 14-4258. EMIF_CTLCFG_DENALI_CTL_128 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE1_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYMSTR_MAX_TYPE1_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYMSTR_MAX_TYPE1_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYMSTR_MAX_TYPE1_F1							
R/W							
0h							

Table 14-12894. EMIF_CTLCFG_DENALI_CTL_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE1_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.180 EMIF_CTLCFG_DENALI_CTL_129 Register

1 EMIF_CTLCFG_DENALI_CTL_129 Register (Offset = 204h) [reset = 0h]

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Table 14-12895. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8204h**

Figure 14-4259. EMIF_CTLCFG_DENALI_CTL_129 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE2_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE2_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE2_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F1							
R/W							
0h							

Table 14-12897. EMIF_CTLCFG_DENALI_CTL_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE2_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.181 EMIF_CTLCFG_DENALI_CTL_130 Register

1 EMIF_CTLCFG_DENALI_CTL_130 Register (Offset = 208h) [reset = 0h]

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Table 14-12898. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8208h

Figure 14-4260. EMIF_CTLCFG_DENALI_CTL_130 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE3_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE3_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE3_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE3_F1							
R/W							
0h							

Table 14-12900. EMIF_CTLCFG_DENALI_CTL_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE3_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.182 EMIF_CTLCFG_DENALI_CTL_131 Register

1 EMIF_CTLCFG_DENALI_CTL_131 Register (Offset = 20Ch) [reset = 0h]

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Table 14-12901. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 820Ch**

Figure 14-4261. EMIF_CTLCFG_DENALI_CTL_131 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-12903. EMIF_CTLCFG_DENALI_CTL_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F1	R/W	0h	Defines the DFI[4.0 and 4.0v2] PHY controller request promotion number of regular [not long] counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.183 EMIF_CTLCFG_DENALI_CTL_132 Register

1 EMIF_CTLCFG_DENALI_CTL_132 Register (Offset = 210h) [reset = 0h]

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Table 14-12904. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8210h**

Figure 14-4262. EMIF_CTLCFG_DENALI_CTL_132 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TDFI_PHYMSTR_RESP_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_RESP_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_RESP_F1							
R/W							
0h							

Table 14-12906. EMIF_CTLCFG_DENALI_CTL_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TDFI_PHYMSTR_RESP_F1	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] to be set to 1 in the PHYMSTR_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.184 EMIF_CTLCFG_DENALI_CTL_133 Register

1 EMIF_CTLCFG_DENALI_CTL_133 Register (Offset = 214h) [reset = 0h]

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Table 14-12907. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8214h

Figure 14-4263. EMIF_CTLCFG_DENALI_CTL_133 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_F2							
R/W							
0h							

Table 14-12909. EMIF_CTLCFG_DENALI_CTL_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_F2	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.185 EMIF_CTLCFG_DENALI_CTL_134 Register

1 EMIF_CTLCFG_DENALI_CTL_134 Register (Offset = 218h) [reset = 0h]

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Table 14-12910. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8218h**

Figure 14-4264. EMIF_CTLCFG_DENALI_CTL_134 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE0_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE0_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE0_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F2							
R/W							
0h							

Table 14-12912. EMIF_CTLCFG_DENALI_CTL_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE0_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.186 EMIF_CTLCFG_DENALI_CTL_135 Register

1 EMIF_CTLCFG_DENALI_CTL_135 Register (Offset = 21Ch) [reset = 0h]

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Table 14-12913. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 821Ch**

Figure 14-4265. EMIF_CTLCFG_DENALI_CTL_135 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE1_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE1_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE1_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE1_F2							
R/W							
0h							

Table 14-12915. EMIF_CTLCFG_DENALI_CTL_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE1_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.187 EMIF_CTLCFG_DENALI_CTL_136 Register

1 EMIF_CTLCFG_DENALI_CTL_136 Register (Offset = 220h) [reset = 0h]

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Table 14-12916. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8220h**

Figure 14-4266. EMIF_CTLCFG_DENALI_CTL_136 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE2_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE2_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE2_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F2							
R/W							
0h							

Table 14-12918. EMIF_CTLCFG_DENALI_CTL_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE2_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.188 EMIF_CTLCFG_DENALI_CTL_137 Register

1 EMIF_CTLCFG_DENALI_CTL_137 Register (Offset = 224h) [reset = 0h]

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Table 14-12919. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8224h**

Figure 14-4267. EMIF_CTLCFG_DENALI_CTL_137 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYMSTR_MAX_TYPE3_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYMSTR_MAX_TYPE3_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_MAX_TYPE3_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE3_F2							
R/W							
0h							

Table 14-12921. EMIF_CTLCFG_DENALI_CTL_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYMSTR_MAX_TYPE3_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.189 EMIF_CTLCFG_DENALI_CTL_138 Register

1 EMIF_CTLCFG_DENALI_CTL_138 Register (Offset = 228h) [reset = 0h]

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Table 14-12922. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8228h**

Figure 14-4268. EMIF_CTLCFG_DENALI_CTL_138 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-12924. EMIF_CTLCFG_DENALI_CTL_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F2	R/W	0h	Defines the DFI[4.0 and 4.0v2] PHY controller request promotion number of regular [not long] counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.190 EMIF_CTLCFG_DENALI_CTL_139 Register

1 EMIF_CTLCFG_DENALI_CTL_139 Register (Offset = 22Ch) [reset = 0h]

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Table 14-12925. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 822Ch**

Figure 14-4269. EMIF_CTLCFG_DENALI_CTL_139 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHYMSTR_NO_AREF</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TDFI_PHYMSTR_RESP_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDFI_PHYMSTR_RESP_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDFI_PHYMSTR_RESP_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12927. EMIF_CTLCFG_DENALI_CTL_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHYMSTR_NO_AREF	R/W	0h	isables refreshes during the PHY controller interface sequence. Set to 1 to disable. Refreshes during reset are only supported for DFI 4.0 and this parameter may be set or cleared for DFI 4.0. For all other DFI versions, this parameter must be set to 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	TDFI_PHYMSTR_RESP_F2	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] to be set to 1 in the PHYMSTR_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.191 EMIF_CTLCFG_DENALI_CTL_140 Register

1 EMIF_CTLCFG_DENALI_CTL_140 Register (Offset = 230h) [reset = 0h]

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Table 14-12928. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8230h**

Figure 14-4270. EMIF_CTLCFG_DENALI_CTL_140 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHYMSTR_TRAIN_AFTER_INIT_COMPLETE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHYMSTR_DFI_VERSION_4P0V1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						PHYMSTR_ERROR_STATUS	
NONE						R	
0h						0h	

Table 14-12930. EMIF_CTLCFG_DENALI_CTL_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHYMSTR_TRAIN_AFTER_INIT_COMPLETE	R/W	0h	Defines how the PHY will use the PHY Controller Interface for training. Clear to 0 to perform training without the PHY Controller Interface, or set to 1 to use the PHY Controller Interface to gain control over the DFI bus after the dfi_init_complete signal assertion for the initial training. Default is cleared to 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHYMSTR_DFI_VERSION_4P0V1	R/W	0h	Defines the version of the DFI 4.0 specification supported. Clear to 0 for DFI 4.0 version 2 PHY Controller Interface, or set to 1 for DFI 4.0 version 1 PHY Controller Interface. Default is cleared to 0 for version 2. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12930. EMIF_CTLCFG_DENALI_CTL_140 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PHYMSTR_ERROR_STATUS	R	0h	Identifies the source of any DFI PHY Controller Interface errors. Value of 1 indicates a timing violation of the associated timing parameter. Bit [0] set indicates a TDFI_PHYMSTR_MAX or TDFI_PHYMSTR_TYPEn_MAX parmaeter violation and bit [1] set indicates a TDFI_PHYMSTR_RESP parameter violation. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.192 EMIF_CTLCFG_DENALI_CTL_141 Register

1 EMIF_CTLCFG_DENALI_CTL_141 Register (Offset = 234h) [reset = 0h]

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Table 14-12931. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8234h**

Figure 14-4271. EMIF_CTLCFG_DENALI_CTL_141 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_NORM_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_NORM_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_NORM_THRESHOLD_F0							
R/W							
0h							

Table 14-12933. EMIF_CTLCFG_DENALI_CTL_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_NORM_THRESHOLD_F0	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.193 EMIF_CTLCFG_DENALI_CTL_142 Register

1 EMIF_CTLCFG_DENALI_CTL_142 Register (Offset = 238h) [reset = 0h]

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Table 14-12934. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8238h**

Figure 14-4272. EMIF_CTLCFG_DENALI_CTL_142 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_HIGH_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_HIGH_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_HIGH_THRESHOLD_F0							
R/W							
0h							

Table 14-12936. EMIF_CTLCFG_DENALI_CTL_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_HIGH_THRESHOLD_F0	R/W	0h	MRR temp check number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.194 EMIF_CTLCFG_DENALI_CTL_143 Register

1 EMIF_CTLCFG_DENALI_CTL_143 Register (Offset = 23Ch) [reset = 0h]

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Table 14-12937. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 823Ch**

Figure 14-4273. EMIF_CTLCFG_DENALI_CTL_143 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_TIMEOUT_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_TIMEOUT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_TIMEOUT_F0							
R/W							
0h							

Table 14-12939. EMIF_CTLCFG_DENALI_CTL_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_TIMEOUT_F0	R/W	0h	MRR temp check number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.195 EMIF_CTLCFG_DENALI_CTL_144 Register

1 EMIF_CTLCFG_DENALI_CTL_144 Register (Offset = 240h) [reset = 0h]

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Table 14-12940. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8240h**

Figure 14-4274. EMIF_CTLCFG_DENALI_CTL_144 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_NORM_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_NORM_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_NORM_THRESHOLD_F1							
R/W							
0h							

Table 14-12942. EMIF_CTLCFG_DENALI_CTL_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_NORM_THRESHOLD_F1	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.196 EMIF_CTLCFG_DENALI_CTL_145 Register

1 EMIF_CTLCFG_DENALI_CTL_145 Register (Offset = 244h) [reset = 0h]

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Table 14-12943. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8244h**

Figure 14-4275. EMIF_CTLCFG_DENALI_CTL_145 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MRR_TEMPCHK_HIGH_THRESHOLD_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MRR_TEMPCHK_HIGH_THRESHOLD_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MRR_TEMPCHK_HIGH_THRESHOLD_F1							
R/W							
0h							

Table 14-12945. EMIF_CTLCFG_DENALI_CTL_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_HIGH_THRESHOLD_F1	R/W	0h	MRR temp check number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.197 EMIF_CTLCFG_DENALI_CTL_146 Register

1 EMIF_CTLCFG_DENALI_CTL_146 Register (Offset = 248h) [reset = 0h]

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Table 14-12946. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8248h**

Figure 14-4276. EMIF_CTLCFG_DENALI_CTL_146 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_TIMEOUT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_TIMEOUT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_TIMEOUT_F1							
R/W							
0h							

Table 14-12948. EMIF_CTLCFG_DENALI_CTL_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_TIMEOUT_F1	R/W	0h	MRR temp check number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.198 EMIF_CTLCFG_DENALI_CTL_147 Register

1 EMIF_CTLCFG_DENALI_CTL_147 Register (Offset = 24Ch) [reset = 0h]

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Table 14-12949. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 824Ch**

Figure 14-4277. EMIF_CTLCFG_DENALI_CTL_147 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_NORM_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_NORM_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_NORM_THRESHOLD_F2							
R/W							
0h							

Table 14-12951. EMIF_CTLCFG_DENALI_CTL_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_NORM_THRESHOLD_F2	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.199 EMIF_CTLCFG_DENALI_CTL_148 Register

1 EMIF_CTLCFG_DENALI_CTL_148 Register (Offset = 250h) [reset = 0h]

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Table 14-12952. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8250h**

Figure 14-4278. EMIF_CTLCFG_DENALI_CTL_148 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MRR_TEMPCHK_HIGH_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_HIGH_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_HIGH_THRESHOLD_F2							
R/W							
0h							

Table 14-12954. EMIF_CTLCFG_DENALI_CTL_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MRR_TEMPCHK_HIGH_THRESHOLD_F2	R/W	0h	MRR temp check number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.200 EMIF_CTLCFG_DENALI_CTL_149 Register

1 EMIF_CTLCFG_DENALI_CTL_149 Register (Offset = 254h) [reset = 0h]

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Table 14-12955. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8254h**

Figure 14-4279. EMIF_CTLCFG_DENALI_CTL_149 Name Register

31	30	29	28	27	26	25	24
RESERVED							PPR_CONTROL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
MRR_TEMPCHK_TIMEOUT_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_TEMPCHK_TIMEOUT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_TIMEOUT_F2							
R/W							
0h							

Table 14-12957. EMIF_CTLCFG_DENALI_CTL_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PPR_CONTROL	R/W	0h	Enables the post-package repair feature. Set to 1 to enable. This parameter may only be programmed before initialization begins. Reset Source: ctl_amod_g_rst_n
23:0	MRR_TEMPCHK_TIMEOUT_F2	R/W	0h	MRR temp check number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.201 EMIF_CTLCFG_DENALI_CTL_150 Register

1 EMIF_CTLCFG_DENALI_CTL_150 Register (Offset = 258h) [reset = 0h]

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Table 14-12958. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8258h**

Figure 14-4280. EMIF_CTLCFG_DENALI_CTL_150 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PPR_COMMAND_MRW_REGNUM							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED					PPR_COMMAND		
NONE					W		
0h					0h		

Table 14-12960. EMIF_CTLCFG_DENALI_CTL_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PPR_COMMAND_MRW_REGNUM	R/W	0h	Specifies the mode register to be used. Clear to 0 for MRW0 or program to 4 for MRW4. All other values are reserved.. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PPR_COMMAND	W	0h	Specifies the type of PPR command. Program to 1 for pre-charge all, program to 2 for MRW, program to 3 for activate, or program to 5 for write. All other values are reserved. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.202 EMIF_CTLCFG_DENALI_CTL_151 Register

1 EMIF_CTLCFG_DENALI_CTL_151 Register (Offset = 25Ch) [reset = 0h]

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Table 14-12961. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 825Ch**

Figure 14-4281. EMIF_CTLCFG_DENALI_CTL_151 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PPR_COMMAND_MRW_DATA
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PPR_COMMAND_MRW_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PPR_COMMAND_MRW_DATA							
R/W							
0h							

Table 14-12963. EMIF_CTLCFG_DENALI_CTL_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PPR_COMMAND_MRW_DATA	R/W	0h	Specifies the data for the mode register write. Reset Source: ctl_amod_g_rst_n

14.5.1.2.203 EMIF_CTLCFG_DENALI_CTL_152 Register

1 EMIF_CTLCFG_DENALI_CTL_152 Register (Offset = 260h) [reset = 0h]

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Table 14-12964. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8260h**

Figure 14-4282. EMIF_CTLCFG_DENALI_CTL_152 Name Register

31	30	29	28	27	26	25	24
RESERVED				PPR_BANK_ADDRESS			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							PPR_ROW_ADDRESS
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PPR_ROW_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
PPR_ROW_ADDRESS							
R/W							
0h							

Table 14-12966. EMIF_CTLCFG_DENALI_CTL_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PPR_BANK_ADDRESS	R/W	0h	Specifies the bank for the row to be repaired. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PPR_ROW_ADDRESS	R/W	0h	Specifies the encoded row address to be repaired. Reset Source: ctl_amod_g_rst_n

14.5.1.2.204 EMIF_CTLCFG_DENALI_CTL_153 Register

1 EMIF_CTLCFG_DENALI_CTL_153 Register (Offset = 264h) [reset = 0h]

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Table 14-12967. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8264h**

Figure 14-4283. EMIF_CTLCFG_DENALI_CTL_153 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PPR_CS_ADDRESS</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12969. EMIF_CTLCFG_DENALI_CTL_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PPR_CS_ADDRESS	R/W	0h	Specifies the chip select for the row to be repaired. Reset Source: ctl_amod_g_rst_n

14.5.1.2.205 EMIF_CTLCFG_DENALI_CTL_154 Register

1 EMIF_CTLCFG_DENALI_CTL_154 Register (Offset = 268h) [reset = 0h]

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Table 14-12970. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8268h**

Figure 14-4284. EMIF_CTLCFG_DENALI_CTL_154 Name Register

31	30	29	28	27	26	25	24
PPR_DATA_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PPR_DATA_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PPR_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PPR_DATA_0							
R/W							
0h							

Table 14-12972. EMIF_CTLCFG_DENALI_CTL_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPR_DATA_0	R/W	0h	Holds the data pattern to be written to memory for all data phases. This is specific to DDR4 memories. Reset Source: ctl_amod_g_rst_n

14.5.1.2.206 EMIF_CTLCFG_DENALI_CTL_155 Register

1 EMIF_CTLCFG_DENALI_CTL_155 Register (Offset = 26Ch) [reset = 0h]

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Table 14-12973. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 826Ch

Figure 14-4285. EMIF_CTLCFG_DENALI_CTL_155 Name Register

31	30	29	28	27	26	25	24
PPR_DATA_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PPR_DATA_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PPR_DATA_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PPR_DATA_1							
R/W							
0h							

Table 14-12975. EMIF_CTLCFG_DENALI_CTL_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPR_DATA_1	R/W	0h	Holds the data pattern to be written to memory for all data phases. This is specific to DDR4 memories. Reset Source: ctl_amod_g_rst_n

14.5.1.2.207 EMIF_CTLCFG_DENALI_CTL_156 Register

1 EMIF_CTLCFG_DENALI_CTL_156 Register (Offset = 270h) [reset = 0h]

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Table 14-12976. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8270h**

Figure 14-4286. EMIF_CTLCFG_DENALI_CTL_156 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CKSRX_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CKSRE_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>FM_OVRIDE_CONTROL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PPR_STATUS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12978. EMIF_CTLCFG_DENALI_CTL_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CKSRX_F0	R/W	0h	Clock stable delay on self-refresh exit. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	CKSRE_F0	R/W	0h	Clock hold delay on self-refresh entry. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	FM_OVRIDE_CONTROL	R/W	0h	Enables the FM Override feature. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PPR_STATUS	R	0h	Reports the status of the PPR operation. Bit [0] set indicates that PPR operations are now allowed and bit [1] set indicates if the last PPR command is complete. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.208 EMIF_CTLCFG_DENALI_CTL_157 Register

1 EMIF_CTLCFG_DENALI_CTL_157 Register (Offset = 274h) [reset = 0h]

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Table 14-12979. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8274h**

Figure 14-4287. EMIF_CTLCFG_DENALI_CTL_157 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CKSRX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CKSRE_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CKSRX_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CKSRE_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12981. EMIF_CTLCFG_DENALI_CTL_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CKSRX_F2	R/W	0h	Clock stable delay on self-refresh exit. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	CKSRE_F2	R/W	0h	Clock hold delay on self-refresh entry. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	CKSRX_F1	R/W	0h	Clock stable delay on self-refresh exit. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	CKSRE_F1	R/W	0h	Clock hold delay on self-refresh entry. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.209 EMIF_CTLCFG_DENALI_CTL_158 Register

1 EMIF_CTLCFG_DENALI_CTL_158 Register (Offset = 278h) [reset = 0h]

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Table 14-12982. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8278h**

Figure 14-4288. EMIF_CTLCFG_DENALI_CTL_158 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SR_SHORT_WAKEUP_F0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LPI_IDLE_WAKEUP_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	LP_CMD						
NONE	W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						LOWPOWER_REFRESH_ENABLE	
NONE						R/W	
0h						0h	

Table 14-12984. EMIF_CTLCFG_DENALI_CTL_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_SR_SHORT_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when LPDDR4 memory is in the self-refresh short state [with or without memory clock gating]. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted. FC=0 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_IDLE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_CTRL_WAKEUP timing parameter [in DFI clocks] to be driven when controller is idle. FC=0 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	LP_CMD	W	0h	Low power software command request interface. Bit [0] controls exit, bit [1] controls entry, bits [4:2] define the low power state, bit [5] controls memory clock gating, bit [6] controls controller clock gating, and bit [7] controls lock. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-12984. EMIF_CTLCFG_DENALI_CTL_158 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	LOWPOWER_REFRESH_ENABLE	R/W	0h	Enable refreshes while in low power mode. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.210 EMIF_CTLCFG_DENALI_CTL_159 Register

1 EMIF_CTLCFG_DENALI_CTL_159 Register (Offset = 27Ch) [reset = 0h]

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Table 14-12985. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 827Ch

Figure 14-4289. EMIF_CTLCFG_DENALI_CTL_159 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SRPD_SHORT_WAKEUP_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_PD_WAKEUP_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_SR_LONG_WAKEUP_F0			
NONE				R/W			
0h				0h			

Table 14-12987. EMIF_CTLCFG_DENALI_CTL_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_SRPD_SHORT_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down short state [with or without memory clock gating]. FC=0 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_PD_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in any of the power-down states [with or without memory clock gating]. FC=0 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long with memory and controller clock gating state. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_SR_LONG_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long state [with or without memory clock gating]. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.211 EMIF_CTLCFG_DENALI_CTL_160 Register

1 EMIF_CTLCFG_DENALI_CTL_160 Register (Offset = 280h) [reset = 0h]

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Table 14-12988. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8280h**

Figure 14-4290. EMIF_CTLCFG_DENALI_CTL_160 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_IDLE_WAKEUP_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LPI_TIMER_WAKEUP_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LPI_SRPD_LONG_WAKEUP_F0			
NONE				R/W			
0h				0h			

Table 14-12990. EMIF_CTLCFG_DENALI_CTL_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_IDLE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_CTRL_WAKEUP timing parameter [in DFI clocks] to be driven when controller is idle. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_TIMER_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when the LPI timer expires. FC=0 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_SRPD_LONG_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long state [with or without memory clock gating]. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.212 EMIF_CTLCFG_DENALI_CTL_161 Register

1 EMIF_CTLCFG_DENALI_CTL_161 Register (Offset = 284h) [reset = 0h]

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Table 14-12991. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8284h**

Figure 14-4291. EMIF_CTLCFG_DENALI_CTL_161 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_PD_WAKEUP_F1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SR_LONG_WAKEUP_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_SR_SHORT_WAKEUP_F1			
NONE				R/W			
0h				0h			

Table 14-12993. EMIF_CTLCFG_DENALI_CTL_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_PD_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in any of the power-down states [with or without memory clock gating]. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long with memory and controller clock gating state. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SR_LONG_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long state [with or without memory clock gating]. FC=1 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-12993. EMIF_CTLCFG_DENALI_CTL_161 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	LPI_SR_SHORT_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when LPDDR4 memory is in the self-refresh short state [with or without memory clock gating]. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.213 EMIF_CTLCFG_DENALI_CTL_162 Register

1 EMIF_CTLCFG_DENALI_CTL_162 Register (Offset = 288h) [reset = 0h]

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Table 14-12994. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8288h**

Figure 14-4292. EMIF_CTLCFG_DENALI_CTL_162 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_TIMER_WAKEUP_F1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SRPD_LONG_WAKEUP_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_SRPD_SHORT_WAKEUP_F1			
NONE				R/W			
0h				0h			

Table 14-12996. EMIF_CTLCFG_DENALI_CTL_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_TIMER_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when the LPI timer expires. FC=1 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SRPD_LONG_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long state [with or without memory clock gating]. FC=1 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_SRPD_SHORT_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down short state [with or without memory clock gating]. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.214 EMIF_CTLCFG_DENALI_CTL_163 Register

1 EMIF_CTLCFG_DENALI_CTL_163 Register (Offset = 28Ch) [reset = 0h]

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Table 14-12997. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 828Ch**

Figure 14-4293. EMIF_CTLCFG_DENALI_CTL_163 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SR_LONG_WAKEUP_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SR_SHORT_WAKEUP_F2			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_IDLE_WAKEUP_F2			
NONE				R/W			
0h				0h			

Table 14-12999. EMIF_CTLCFG_DENALI_CTL_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long with memory and controller clock gating state. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_SR_LONG_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh long state [with or without memory clock gating]. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SR_SHORT_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when LPDDR4 memory is in the self-refresh short state [with or without memory clock gating]. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_IDLE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_CTRL_WAKEUP timing parameter [in DFI clocks] to be driven when controller is idle. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.215 EMIF_CTLCFG_DENALI_CTL_164 Register

1 EMIF_CTLCFG_DENALI_CTL_164 Register (Offset = 290h) [reset = 0h]

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Table 14-13000. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8290h**

Figure 14-4294. EMIF_CTLCFG_DENALI_CTL_164 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SRPD_LONG_WAKEUP_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SRPD_SHORT_WAKEUP_F2			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_PD_WAKEUP_F2			
NONE				R/W			
0h				0h			

Table 14-13002. EMIF_CTLCFG_DENALI_CTL_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LPI_SRPD_LONG_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down long state [with or without memory clock gating]. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	LPI_SRPD_SHORT_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in the self-refresh power-down short state [with or without memory clock gating]. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_PD_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when memory is in any of the power-down states [with or without memory clock gating]. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.216 EMIF_CTLCFG_DENALI_CTL_165 Register

1 EMIF_CTLCFG_DENALI_CTL_165 Register (Offset = 294h) [reset = 0h]

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Table 14-13003. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8294h**

Figure 14-4295. EMIF_CTLCFG_DENALI_CTL_165 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>LPI_CTRL_REQ_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">LPI_WAKEUP_EN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">LPI_TIMER_WAKEUP_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13005. EMIF_CTLCFG_DENALI_CTL_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	LPI_CTRL_REQ_EN	R/W	0h	Enables the dfi_lpi_ctrl_req signal for the LPI. This signal is only relevant for DFI versions 3.1 and beyond. Set to 1 to enable or clear to 0 to disable. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	LPI_WAKEUP_EN	R/W	0h	Enables the various low power state wakeup parameters for LPI request uses. Bit [0] enables controller idle wakeup, bit [1] enables power-down wakeup, bit [2] enables either self-refresh short, self-refresh long with or without mem clk gating, either self-refresh power-down short, or self-refresh power-down long with or without mem clk gating, bit [3] enables self-refresh long with mem and ctlr clk gating or self-refresh power-down long with mem and ctlr clk gating, bit [4] enables the LPI timer expire wakeup, and bit [5] is reserved. Set each bit to 1 to enable the respective LP_WAKEUP value for the LPI request. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	LPI_TIMER_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter [in DFI clocks] to be driven when the LPI timer expires. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.217 EMIF_CTLCFG_DENALI_CTL_166 Register

1 EMIF_CTLCFG_DENALI_CTL_166 Register (Offset = 298h) [reset = 0h]

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Table 14-13006. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8298h**

Figure 14-4296. EMIF_CTLCFG_DENALI_CTL_166 Name Register

31	30	29	28	27	26	25	24
RESERVED				LPI_WAKEUP_TIMEOUT			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPI_WAKEUP_TIMEOUT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LPI_TIMER_COUNT			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LPI_TIMER_COUNT							
R/W							
0h							

Table 14-13008. EMIF_CTLCFG_DENALI_CTL_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	LPI_WAKEUP_TIMEOUT	R/W	0h	Defines the LPI timeout time, the maximum cycles between a dfi_lp_req de-assertion and a dfi_lp_ack de-assertion. If this value is exceeded, an interrupt will occur. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	LPI_TIMER_COUNT	R/W	0h	Defines the LPI timer count. Reset Source: ctl_amod_g_rst_n

14.5.1.2.218 EMIF_CTLCFG_DENALI_CTL_167 Register

1 EMIF_CTLCFG_DENALI_CTL_167 Register (Offset = 29Ch) [reset = 4000h]

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Table 14-13009. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 829Ch

Figure 14-4297. EMIF_CTLCFG_DENALI_CTL_167 Name Register

31	30	29	28	27	26	25	24
RESERVED				LP_AUTO_EXIT_EN			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LP_AUTO_ENTRY_EN			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	LP_STATE						
NONE	R						
0h	40h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TDFI_LP_RESP		
NONE					R/W		
0h					0h		

Table 14-13011. EMIF_CTLCFG_DENALI_CTL_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	LP_AUTO_EXIT_EN	R/W	0h	Enable auto exit from each of the low power states when a read or write command enters the command queue. Bit [0] controls power-down, bit [1] controls self-refresh long or self-refresh power-down long, bit [2] controls self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating, and bit [3] controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	LP_AUTO_ENTRY_EN	R/W	0h	Enable auto entry into each of the low power states when the associated idle timer expires. Bit [0] controls power-down, bit [1] controls self-refresh long or self-refresh power-down long, bit [2] controls self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating, and bit [3] controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	LP_STATE	R	40h	Low power state status parameter. Bits [5:0] indicate the current low power state and bit [6] set indicates that status bits are valid. READ-ONLY Reset Source: ctl_amod_g_rst_n

Table 14-13011. EMIF_CTLCFG_DENALI_CTL_167 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2:0	TDFI_LP_RESP	R/W	0h	Defines the DFI tLP_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_lp_req assertion and a dfi_lp_ack assertion. Reset Source: ctl_amod_g_rst_n

14.5.1.2.219 EMIF_CTLCFG_DENALI_CTL_168 Register

1 EMIF_CTLCFG_DENALI_CTL_168 Register (Offset = 2A0h) [reset = 0h]

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Table 14-13012. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82A0h**

Figure 14-4298. EMIF_CTLCFG_DENALI_CTL_168 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				LP_AUTO_PD_IDLE			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
LP_AUTO_PD_IDLE							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED					LP_AUTO_MEM_GATE_EN		
NONE					R/W		
0h					0h		

Table 14-13014. EMIF_CTLCFG_DENALI_CTL_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	LP_AUTO_PD_IDLE	R/W	0h	Defines the idle time [in controller clocks] until the controller will automatically issue an entry into one of the power-down low power states. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	LP_AUTO_MEM_GATE_EN	R/W	0h	Enable memory clock gating when entering a low power state via the auto low power counters. Bit [0] controls power-down, bit [1] controls self-refresh long or self-refresh power-down long, and bit [2] controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.220 EMIF_CTLCFG_DENALI_CTL_169 Register

1 EMIF_CTLCFG_DENALI_CTL_169 Register (Offset = 2A4h) [reset = 0h]

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Table 14-13015. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82A4h**

Figure 14-4299. EMIF_CTLCFG_DENALI_CTL_169 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LP_AUTO_SR_LONG_MC_GATE_IDLE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LP_AUTO_SR_LONG_IDLE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">LP_AUTO_SR_SHORT_IDLE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LP_AUTO_SR_SHORT_IDLE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13017. EMIF_CTLCFG_DENALI_CTL_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	LP_AUTO_SR_LONG_MC_GATE_IDLE	R/W	0h	Defines the idle time [in long counts] until the controller will automatically issue an entry into the self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating low power states. Reset Source: ctl_amod_g_rst_n
23:16	LP_AUTO_SR_LONG_IDLE	R/W	0h	Defines the idle time [in long counts] until the controller will automatically issue an entry into the self-refresh long or self-refresh power-down long [with or without memory clock gating] low power states. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	LP_AUTO_SR_SHORT_IDLE	R/W	0h	Defines the idle time [in controller clocks] until the controller will automatically issue an entry into the self-refresh short or self-refresh power-down short [with or without memory clock gating] low power states. Reset Source: ctl_amod_g_rst_n

14.5.1.2.221 EMIF_CTLCFG_DENALI_CTL_170 Register

1 EMIF_CTLCFG_DENALI_CTL_170 Register (Offset = 2A8h) [reset = 0h]

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Table 14-13018. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 82A8h

Figure 14-4300. EMIF_CTLCFG_DENALI_CTL_170 Name Register

31	30	29	28	27	26	25	24
HW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
HW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
HW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
HW_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-13020. EMIF_CTLCFG_DENALI_CTL_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HW_PROMOTE_THRESHOLD_F1	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	HW_PROMOTE_THRESHOLD_F0	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.222 EMIF_CTLCFG_DENALI_CTL_171 Register

1 EMIF_CTLCFG_DENALI_CTL_171 Register (Offset = 2ACh) [reset = 0h]

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Table 14-13021. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82ACh**

Figure 14-4301. EMIF_CTLCFG_DENALI_CTL_171 Name Register

31	30	29	28	27	26	25	24
LPC_PROMOTE_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
LPC_PROMOTE_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
HW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
HW_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-13023. EMIF_CTLCFG_DENALI_CTL_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	LPC_PROMOTE_THRESHOLD_F0	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW and auto low power commands. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	HW_PROMOTE_THRESHOLD_F2	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.223 EMIF_CTLCFG_DENALI_CTL_172 Register

1 EMIF_CTLCFG_DENALI_CTL_172 Register (Offset = 2B0h) [reset = 0h]

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Table 14-13024. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82B0h**

Figure 14-4302. EMIF_CTLCFG_DENALI_CTL_172 Name Register

31	30	29	28	27	26	25	24
LPC_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPC_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LPC_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LPC_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-13026. EMIF_CTLCFG_DENALI_CTL_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	LPC_PROMOTE_THRESHOLD_F2	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW and auto low power commands. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	LPC_PROMOTE_THRESHOLD_F1	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW and auto low power commands. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.224 EMIF_CTLCFG_DENALI_CTL_173 Register

1 EMIF_CTLCFG_DENALI_CTL_173 Register (Offset = 2B4h) [reset = 0h]

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Table 14-13027. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 82B4h

Figure 14-4303. EMIF_CTLCFG_DENALI_CTL_173 Name Register

31	30	29	28	27	26	25	24
RESERVED							LPC_SR_EXIT_CMD_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							LPC_SR_PHYMSTR_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							LPC_SR_PHYUPD_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							LPC_SR_CTRLUPD_EN
NONE							R/W
0h							0h

Table 14-13029. EMIF_CTLCFG_DENALI_CTL_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	LPC_SR_EXIT_CMD_EN	R/W	0h	Enable LPC to execute any of the commands on self-refresh exit while exiting. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	LPC_SR_PHYMSTR_EN	R/W	0h	Enable LPC to execute a DFI PHY Controller request on a self-refresh exit sequence. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	LPC_SR_PHYUPD_EN	R/W	0h	Enable LPC to execute a DFI PHY update on a self-refresh exit sequence. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	LPC_SR_CTRLUPD_EN	R/W	0h	Enable LPC to execute a DFI control update on a self-refresh exit sequence. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.225 EMIF_CTLCFG_DENALI_CTL_174 Register

1 EMIF_CTLCFG_DENALI_CTL_174 Register (Offset = 2B8h) [reset = 0h]

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Table 14-13030. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82B8h**

Figure 14-4304. EMIF_CTLCFG_DENALI_CTL_174 Name Register

31	30	29	28	27	26	25	24
RESERVED							DFS_ENABLE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PWRDN_SHIFT_DELAY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWRDN_SHIFT_DELAY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							LPC_SR_ZQ_EN
NONE							R/W
0h							0h

Table 14-13032. EMIF_CTLCFG_DENALI_CTL_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	DFS_ENABLE	R/W	0h	Enable hardware dynamic frequency scaling. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	PWRDN_SHIFT_DELAY	R/W	0h	This parameter should be programmed to zero. Manual adjustment of inhibit_pwrdn_shift in memcd_strategy_data_delay. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	LPC_SR_ZQ_EN	R/W	0h	Enable LPC to execute a ZQ calibration on a self-refresh exit sequence. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.226 EMIF_CTLCFG_DENALI_CTL_175 Register

1 EMIF_CTLCFG_DENALI_CTL_175 Register (Offset = 2BCh) [reset = 0h]

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Table 14-13033. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 82BCh

Figure 14-4305. EMIF_CTLCFG_DENALI_CTL_175 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							DFS_PHY_REG_WRITE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					DFS_DLL_OFF		
NONE					R/W		
0h					0h		

Table 14-13035. EMIF_CTLCFG_DENALI_CTL_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	DFS_PHY_REG_WRITE_EN	R/W	0h	Enable a register write to the PHY during a frequency change. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	DFS_DLL_OFF	R/W	0h	Defines if the memory DLL must be off for the associated frequency set. Bit [0] corresponds to frequency set 0, bit [1] corresponds to frequency set 1, etc. Set each bit to 1 to require DLL off. Reset Source: ctl_amod_g_rst_n

14.5.1.2.227 EMIF_CTLCFG_DENALI_CTL_176 Register

1 EMIF_CTLCFG_DENALI_CTL_176 Register (Offset = 2C0h) [reset = 0h]

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Table 14-13036. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82C0h**

Figure 14-4306. EMIF_CTLCFG_DENALI_CTL_176 Name Register

31	30	29	28	27	26	25	24
DFS_PHY_REG_WRITE_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PHY_REG_WRITE_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PHY_REG_WRITE_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_ADDR							
R/W							
0h							

Table 14-13038. EMIF_CTLCFG_DENALI_CTL_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFS_PHY_REG_WRITE_ADDR	R/W	0h	Register address which will be written during a frequency change. Must be a PHY register address. Reset Source: ctl_amod_g_rst_n

14.5.1.2.228 EMIF_CTLCFG_DENALI_CTL_177 Register

1 EMIF_CTLCFG_DENALI_CTL_177 Register (Offset = 2C4h) [reset = 0h]

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Table 14-13039. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82C4h**

Figure 14-4307. EMIF_CTLCFG_DENALI_CTL_177 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CURRENT_REG_COPY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DFS_PHY_REG_WRITE_WAIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DFS_PHY_REG_WRITE_WAIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">DFS_PHY_REG_WRITE_MASK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13041. EMIF_CTLCFG_DENALI_CTL_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CURRENT_REG_COPY	R	0h	Indicates the current copy of timing parameters that is in use by the controller. Reset Source: ctl_amod_g_rst_n
23:8	DFS_PHY_REG_WRITE_WAIT	R/W	0h	Defines the number of DFI PHY clocks that the controller will wait after issuing the register write to the PHY during a frequency change. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	DFS_PHY_REG_WRITE_MASK	R/W	0h	Register mask which will be written during a frequency change. Reset Source: ctl_amod_g_rst_n

14.5.1.2.229 EMIF_CTLCFG_DENALI_CTL_178 Register

1 EMIF_CTLCFG_DENALI_CTL_178 Register (Offset = 2C8h) [reset = 0h]

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Table 14-13042. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82C8h**

Figure 14-4308. EMIF_CTLCFG_DENALI_CTL_178 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						DFIBUS_BOOT_FREQ	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
RESERVED						INIT_FREQ	
NONE						R/W	
0h						0h	

Table 14-13044. EMIF_CTLCFG_DENALI_CTL_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	DFIBUS_BOOT_FREQ	R/W	0h	Defines the DFI bus boot frequency register copy Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	INIT_FREQ	R/W	0h	Specifies what frequency register copy will be in use by the memory after initialization completes. Reset Source: ctl_amod_g_rst_n

14.5.1.2.230 EMIF_CTLCFG_DENALI_CTL_179 Register

1 EMIF_CTLCFG_DENALI_CTL_179 Register (Offset = 2CCh) [reset = 0h]

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Table 14-13045. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82CCh**

Figure 14-4309. EMIF_CTLCFG_DENALI_CTL_179 Name Register

31	30	29	28	27	26	25	24
DFS_PHY_REG_WRITE_DATA_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PHY_REG_WRITE_DATA_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PHY_REG_WRITE_DATA_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F0							
R/W							
0h							

Table 14-13047. EMIF_CTLCFG_DENALI_CTL_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFS_PHY_REG_WRITE_DATA_F0	R/W	0h	Register data which will be written during a frequency change. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.231 EMIF_CTLCFG_DENALI_CTL_180 Register

1 EMIF_CTLCFG_DENALI_CTL_180 Register (Offset = 2D0h) [reset = 0h]

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Table 14-13048. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 82D0h

Figure 14-4310. EMIF_CTLCFG_DENALI_CTL_180 Name Register

31	30	29	28	27	26	25	24
DFS_PHY_REG_WRITE_DATA_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PHY_REG_WRITE_DATA_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PHY_REG_WRITE_DATA_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F1							
R/W							
0h							

Table 14-13050. EMIF_CTLCFG_DENALI_CTL_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFS_PHY_REG_WRITE_DATA_F1	R/W	0h	Register data which will be written during a frequency change. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.232 EMIF_CTLCFG_DENALI_CTL_181 Register

1 EMIF_CTLCFG_DENALI_CTL_181 Register (Offset = 2D4h) [reset = 0h]

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Table 14-13051. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82D4h**

Figure 14-4311. EMIF_CTLCFG_DENALI_CTL_181 Name Register

31	30	29	28	27	26	25	24
DFS_PHY_REG_WRITE_DATA_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
DFS_PHY_REG_WRITE_DATA_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
DFS_PHY_REG_WRITE_DATA_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F2							
R/W							
0h							

Table 14-13053. EMIF_CTLCFG_DENALI_CTL_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFS_PHY_REG_WRITE_DATA_F2	R/W	0h	Register data which will be written during a frequency change. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.233 EMIF_CTLCFG_DENALI_CTL_182 Register

1 EMIF_CTLCFG_DENALI_CTL_182 Register (Offset = 2D8h) [reset = 0h]

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Table 14-13054. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82D8h**

Figure 14-4312. EMIF_CTLCFG_DENALI_CTL_182 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_INIT_START_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_INIT_START_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_INIT_START_F0							
R/W							
0h							

Table 14-13056. EMIF_CTLCFG_DENALI_CTL_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_START_F0	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks], the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.234 EMIF_CTLCFG_DENALI_CTL_183 Register

1 EMIF_CTLCFG_DENALI_CTL_183 Register (Offset = 2DCh) [reset = 0h]

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Table 14-13057. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82DCh**

Figure 14-4313. EMIF_CTLCFG_DENALI_CTL_183 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_COMPLETE_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_COMPLETE_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_COMPLETE_F0							
R/W							
0h							

Table 14-13059. EMIF_CTLCFG_DENALI_CTL_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_COMPLETE_F0	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks], the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.235 EMIF_CTLCFG_DENALI_CTL_184 Register

1 EMIF_CTLCFG_DENALI_CTL_184 Register (Offset = 2E0h) [reset = 0h]

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Table 14-13060. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82E0h**

Figure 14-4314. EMIF_CTLCFG_DENALI_CTL_184 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_START_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_START_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_START_F1							
R/W							
0h							

Table 14-13062. EMIF_CTLCFG_DENALI_CTL_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_START_F1	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks], the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.236 EMIF_CTLCFG_DENALI_CTL_185 Register

1 EMIF_CTLCFG_DENALI_CTL_185 Register (Offset = 2E4h) [reset = 0h]

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Table 14-13063. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 82E4h

Figure 14-4315. EMIF_CTLCFG_DENALI_CTL_185 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_COMPLETE_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_COMPLETE_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_COMPLETE_F1							
R/W							
0h							

Table 14-13065. EMIF_CTLCFG_DENALI_CTL_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_COMPLETE_F1	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks], the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.237 EMIF_CTLCFG_DENALI_CTL_186 Register

1 EMIF_CTLCFG_DENALI_CTL_186 Register (Offset = 2E8h) [reset = 0h]

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Table 14-13066. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82E8h**

Figure 14-4316. EMIF_CTLCFG_DENALI_CTL_186 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_START_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_START_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_START_F2							
R/W							
0h							

Table 14-13068. EMIF_CTLCFG_DENALI_CTL_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_START_F2	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks], the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.238 EMIF_CTLCFG_DENALI_CTL_187 Register

1 EMIF_CTLCFG_DENALI_CTL_187 Register (Offset = 2ECh) [reset = 0h]

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Table 14-13069. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82ECh**

Figure 14-4317. EMIF_CTLCFG_DENALI_CTL_187 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_INIT_COMPLETE_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_INIT_COMPLETE_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_INIT_COMPLETE_F2							
R/W							
0h							

Table 14-13071. EMIF_CTLCFG_DENALI_CTL_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	TDFI_INIT_COMPLETE_F2	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks], the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.239 EMIF_CTLCFG_DENALI_CTL_188 Register

1 EMIF_CTLCFG_DENALI_CTL_188 Register (Offset = 2F0h) [reset = 0h]

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Table 14-13072. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82F0h**

Figure 14-4318. EMIF_CTLCFG_DENALI_CTL_188 Name Register

31	30	29	28	27	26	25	24
RESERVED					WRITE_MODEREG		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
WRITE_MODEREG							
R/W							
0h							
15	14	13	12	11	10	9	8
WRITE_MODEREG							
R/W							
0h							
7	6	5	4	3	2	1	0
WRITE_MODEREG							
R/W							
0h							

Table 14-13074. EMIF_CTLCFG_DENALI_CTL_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:0	WRITE_MODEREG	R/W	0h	Write memory mode register data to the DRAMs. Bits [7:0] define the memory mode register number if bit [23] is set, bits [15:8] define the chip select if bit [24] is clear, bits [23:16] define which memory mode register/s to write, bit [24] defines whether all chip selects will be written, and bit [25] triggers the write. Reset Source: ctl_amod_g_rst_n

14.5.1.2.240 EMIF_CTLCFG_DENALI_CTL_189 Register

1 EMIF_CTLCFG_DENALI_CTL_189 Register (Offset = 2F4h) [reset = 0h]

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Table 14-13075. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 82F4h

Figure 14-4319. EMIF_CTLCFG_DENALI_CTL_189 Name Register

31	30	29	28	27	26	25	24
RESERVED							READ_MODEREG
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
READ_MODEREG							
R/W							
0h							
15	14	13	12	11	10	9	8
READ_MODEREG							
R/W							
0h							
7	6	5	4	3	2	1	0
MRW_STATUS							
R							
0h							

Table 14-13077. EMIF_CTLCFG_DENALI_CTL_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	READ_MODEREG	R/W	0h	Read the specified memory mode register from specified chip when start bit set. Bits [7:0] define the memory mode register and bits [15:8] define the chip select. Set bit [16] to 1 to trigger. Reset Source: ctl_amod_g_rst_n
7:0	MRW_STATUS	R	0h	Write memory mode register status. Bit [0] set indicates a WRITE_MODEREG parameter programming error. Bit [1] set indicates a PASR error. Bit [2] is Reserved. Bit [3] set indicates a self-refresh or deep power-down error. Bit [4] set indicates that a write to MR3 or MR11 was attempted [WRITE_MODEREG bit [25] was asserted with bit [17] set, or bit [23] was asserted with bits [7:0] defining MR3 or MR11] during tZQCAL after a ZQ calibration start command. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.241 EMIF_CTLCFG_DENALI_CTL_190 Register

1 EMIF_CTLCFG_DENALI_CTL_190 Register (Offset = 2F8h) [reset = 0h]

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Table 14-13078. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82F8h**

Figure 14-4320. EMIF_CTLCFG_DENALI_CTL_190 Name Register

31	30	29	28	27	26	25	24
AUTO_TEMPCHK_VAL_0							
R							
0h							
23	22	21	20	19	18	17	16
PERIPHERAL_MRR_DATA							
R							
0h							
15	14	13	12	11	10	9	8
PERIPHERAL_MRR_DATA							
R							
0h							
7	6	5	4	3	2	1	0
PERIPHERAL_MRR_DATA							
R							
0h							

Table 14-13080. EMIF_CTLCFG_DENALI_CTL_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	AUTO_TEMPCHK_VAL_0	R	0h	MR4 data for all devices accessed by automatic MRR commands. Bits [3:0] correlate to the device on the lower byte, bits [7:4] correlate to the devices on the 2nd byte etc. Value indicates the OP7, OP2, OP1 and OP0 bits. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:0	PERIPHERAL_MRR_DATA	R	0h	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter. Bits [7:0] indicate the read data and bits [15:8] indicate the chip. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.242 EMIF_CTLCFG_DENALI_CTL_191 Register

1 EMIF_CTLCFG_DENALI_CTL_191 Register (Offset = 2FCh) [reset = 0h]

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Table 14-13081. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 82FCh**

Figure 14-4321. EMIF_CTLCFG_DENALI_CTL_191 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MRW_DFS_UPDATE_FRC</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>DISABLE_UPDATE_TVRCG</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">AUTO_TEMPCHK_VAL_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13083. EMIF_CTLCFG_DENALI_CTL_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	MRW_DFS_UPDATE_FRC	R/W	0h	Defines the frequency register set to use when doing a software MRW with WRITE_MODEREG bit [26]. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	DISABLE_UPDATE_TVRCG	R/W	0h	Bypass changing for TVRCG during a DFS operation. Set to 1 to skip TVRCG. Reset Source: ctl_amod_g_rst_n
7:0	AUTO_TEMPCHK_VAL_1	R	0h	MR4 data for all devices accessed by automatic MRR commands. Bits [3:0] correlate to the device on the lower byte, bits [7:4] correlate to the devices on the 2nd byte etc. Value indicates the OP7, OP2, OP1 and OP0 bits. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.243 EMIF_CTLCFG_DENALI_CTL_192 Register

1 EMIF_CTLCFG_DENALI_CTL_192 Register (Offset = 300h) [reset = 0h]

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Table 14-13084. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8300h**

Figure 14-4322. EMIF_CTLCFG_DENALI_CTL_192 Name Register

31	30	29	28	27	26	25	24
RESERVED						TVRCG_DISABLE_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
TVRCG_DISABLE_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						TVRCG_ENABLE_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TVRCG_ENABLE_F0							
R/W							
0h							

Table 14-13086. EMIF_CTLCFG_DENALI_CTL_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TVRCG_DISABLE_F0	R/W	0h	JEDEC TVRCG_DISABLE time. FC=0 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TVRCG_ENABLE_F0	R/W	0h	JEDEC TVRCG_ENABLE time. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.244 EMIF_CTLCFG_DENALI_CTL_193 Register

1 EMIF_CTLCFG_DENALI_CTL_193 Register (Offset = 304h) [reset = 0h]

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Table 14-13087. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8304h**

Figure 14-4323. EMIF_CTLCFG_DENALI_CTL_193 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKFSPX_F0				
NONE			R/W				
0h			0h				

23	22	21	20	19	18	17	16
RESERVED			TCKFSPE_F0				
NONE			R/W				
0h			0h				

15	14	13	12	11	10	9	8
RESERVED						TFC_F0	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
TFC_F0							
R/W							
0h							

Table 14-13089. EMIF_CTLCFG_DENALI_CTL_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKFSPX_F0	R/W	0h	JEDEC TCKFSPX, the frequency set point switching time. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKFSPE_F0	R/W	0h	JEDEC TCKFSPE, the frequency set point switching time. FC=0 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TFC_F0	R/W	0h	JEDEC TFC, the frequency set point switching time. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.245 EMIF_CTLCFG_DENALI_CTL_194 Register

1 EMIF_CTLCFG_DENALI_CTL_194 Register (Offset = 308h) [reset = 0h]

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Table 14-13090. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8308h**

Figure 14-4324. EMIF_CTLCFG_DENALI_CTL_194 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TVREF_LONG_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TVREF_LONG_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TVREF_LONG_F0							
R/W							
0h							

Table 14-13092. EMIF_CTLCFG_DENALI_CTL_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TVREF_LONG_F0	R/W	0h	JEDEC TVREF, design will always use the long value. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.246 EMIF_CTLCFG_DENALI_CTL_195 Register

1 EMIF_CTLCFG_DENALI_CTL_195 Register (Offset = 30Ch) [reset = 0h]

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Table 14-13093. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 830Ch**

Figure 14-4325. EMIF_CTLCFG_DENALI_CTL_195 Name Register

31	30	29	28	27	26	25	24
RESERVED						TVRCG_DISABLE_F1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
TVRCG_DISABLE_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						TVRCG_ENABLE_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TVRCG_ENABLE_F1							
R/W							
0h							

Table 14-13095. EMIF_CTLCFG_DENALI_CTL_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TVRCG_DISABLE_F1	R/W	0h	JEDEC TVRCG_DISABLE time. FC=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TVRCG_ENABLE_F1	R/W	0h	JEDEC TVRCG_ENABLE time. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.247 EMIF_CTLCFG_DENALI_CTL_196 Register

1 EMIF_CTLCFG_DENALI_CTL_196 Register (Offset = 310h) [reset = 0h]

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Table 14-13096. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8310h**

Figure 14-4326. EMIF_CTLCFG_DENALI_CTL_196 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKFSPX_F1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKFSPE_F1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TFC_F1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TFC_F1							
R/W							
0h							

Table 14-13098. EMIF_CTLCFG_DENALI_CTL_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKFSPX_F1	R/W	0h	JEDEC TCKFSPX, the frequency set point switching time. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKFSPE_F1	R/W	0h	JEDEC TCKFSPE, the frequency set point switching time. FC=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TFC_F1	R/W	0h	JEDEC TFC, the frequency set point switching time. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.248 EMIF_CTLCFG_DENALI_CTL_197 Register

1 EMIF_CTLCFG_DENALI_CTL_197 Register (Offset = 314h) [reset = 0h]

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Table 14-13099. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8314h

Figure 14-4327. EMIF_CTLCFG_DENALI_CTL_197 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TVREF_LONG_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TVREF_LONG_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TVREF_LONG_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13101. EMIF_CTLCFG_DENALI_CTL_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TVREF_LONG_F1	R/W	0h	JEDEC TVREF, design will always use the long value. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.249 EMIF_CTLCFG_DENALI_CTL_198 Register

1 EMIF_CTLCFG_DENALI_CTL_198 Register (Offset = 318h) [reset = 0h]

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Table 14-13102. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8318h**

Figure 14-4328. EMIF_CTLCFG_DENALI_CTL_198 Name Register

31	30	29	28	27	26	25	24
RESERVED						TVRCG_DISABLE_F2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TVRCG_DISABLE_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TVRCG_ENABLE_F2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TVRCG_ENABLE_F2							
R/W							
0h							

Table 14-13104. EMIF_CTLCFG_DENALI_CTL_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TVRCG_DISABLE_F2	R/W	0h	JEDEC TVRCG_DISABLE time. FC=2 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TVRCG_ENABLE_F2	R/W	0h	JEDEC TVRCG_ENABLE time. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.250 EMIF_CTLCFG_DENALI_CTL_199 Register

1 EMIF_CTLCFG_DENALI_CTL_199 Register (Offset = 31Ch) [reset = 0h]

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Table 14-13105. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 831Ch**

Figure 14-4329. EMIF_CTLCFG_DENALI_CTL_199 Name Register

31	30	29	28	27	26	25	24
RESERVED			TCKFSPX_F2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TCKFSPE_F2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TFC_F2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TFC_F2							
R/W							
0h							

Table 14-13107. EMIF_CTLCFG_DENALI_CTL_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	TCKFSPX_F2	R/W	0h	JEDEC TCKFSPX, the frequency set point switching time. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	TCKFSPE_F2	R/W	0h	JEDEC TCKFSPE, the frequency set point switching time. FC=2 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TFC_F2	R/W	0h	JEDEC TFC, the frequency set point switching time. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.251 EMIF_CTLCFG_DENALI_CTL_200 Register

1 EMIF_CTLCFG_DENALI_CTL_200 Register (Offset = 320h) [reset = 0h]

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Table 14-13108. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8320h**

Figure 14-4330. EMIF_CTLCFG_DENALI_CTL_200 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TVREF_LONG_F2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TVREF_LONG_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TVREF_LONG_F2							
R/W							
0h							

Table 14-13110. EMIF_CTLCFG_DENALI_CTL_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	TVREF_LONG_F2	R/W	0h	JEDEC TVREF, design will always use the long value. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.252 EMIF_CTLCFG_DENALI_CTL_201 Register

1 EMIF_CTLCFG_DENALI_CTL_201 Register (Offset = 324h) [reset = 0h]

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Table 14-13111. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8324h**

Figure 14-4331. EMIF_CTLCFG_DENALI_CTL_201 Name Register

31	30	29	28	27	26	25	24
MRR_PROMOTE_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
MRR_PROMOTE_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
MRR_PROMOTE_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
MRR_PROMOTE_THRESHOLD_F0							
R/W							
0h							

Table 14-13113. EMIF_CTLCFG_DENALI_CTL_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MRR_PROMOTE_THRESHOLD_F1	R/W	0h	MRR promotion number of long counts until the high priority request is asserted. Applies to SW MRR commands. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	MRR_PROMOTE_THRESHOLD_F0	R/W	0h	MRR promotion number of long counts until the high priority request is asserted. Applies to SW MRR commands. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.253 EMIF_CTLCFG_DENALI_CTL_202 Register

1 EMIF_CTLCFG_DENALI_CTL_202 Register (Offset = 328h) [reset = 0h]

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Table 14-13114. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8328h**

Figure 14-4332. EMIF_CTLCFG_DENALI_CTL_202 Name Register

31	30	29	28	27	26	25	24
MRW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MRW_PROMOTE_THRESHOLD_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MRR_PROMOTE_THRESHOLD_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MRR_PROMOTE_THRESHOLD_F2							
R/W							
0h							

Table 14-13116. EMIF_CTLCFG_DENALI_CTL_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MRW_PROMOTE_THRESHOLD_F0	R/W	0h	MRW promotion number of long counts until the high priority request is asserted. Applies to SW MRW commands. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	MRR_PROMOTE_THRESHOLD_F2	R/W	0h	MRR promotion number of long counts until the high priority request is asserted. Applies to SW MRR commands. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.254 EMIF_CTLCFG_DENALI_CTL_203 Register

1 EMIF_CTLCFG_DENALI_CTL_203 Register (Offset = 32Ch) [reset = 0h]

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Table 14-13117. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 832Ch**

Figure 14-4333. EMIF_CTLCFG_DENALI_CTL_203 Name Register

31	30	29	28	27	26	25	24
MRW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
MRW_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
MRW_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
MRW_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-13119. EMIF_CTLCFG_DENALI_CTL_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MRW_PROMOTE_THRESHOLD_F2	R/W	0h	MRW promotion number of long counts until the high priority request is asserted. Applies to SW MRW commands. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	MRW_PROMOTE_THRESHOLD_F1	R/W	0h	MRW promotion number of long counts until the high priority request is asserted. Applies to SW MRW commands. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.255 EMIF_CTLCFG_DENALI_CTL_204 Register

1 EMIF_CTLCFG_DENALI_CTL_204 Register (Offset = 330h) [reset = 0h]

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Table 14-13120. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8330h**

Figure 14-4334. EMIF_CTLCFG_DENALI_CTL_204 Name Register

31	30	29	28	27	26	25	24
RESERVED							MR0_DATA_F0_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
MR0_DATA_F0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
MR0_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							MR4_DLL_RST
NONE							R/W
0h							0h

Table 14-13122. EMIF_CTLCFG_DENALI_CTL_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	MR0_DATA_F0_0	R/W	0h	Data to program into memory mode register 0. FC=0 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	MR4_DLL_RST	R/W	0h	Asserted if DRAM DLL Reset bit resides in MR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.256 EMIF_CTLCFG_DENALI_CTL_205 Register

1 EMIF_CTLCFG_DENALI_CTL_205 Register (Offset = 334h) [reset = 0h]

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Table 14-13123. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8334h**

Figure 14-4335. EMIF_CTLCFG_DENALI_CTL_205 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR1_DATA_F0_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR1_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR1_DATA_F0_0							
R/W							
0h							

Table 14-13125. EMIF_CTLCFG_DENALI_CTL_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F0_0	R/W	0h	Data to program into memory mode register 1. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.257 EMIF_CTLCFG_DENALI_CTL_206 Register

1 EMIF_CTLCFG_DENALI_CTL_206 Register (Offset = 338h) [reset = 0h]

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Table 14-13126. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8338h**

Figure 14-4336. EMIF_CTLCFG_DENALI_CTL_206 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR2_DATA_F0_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR2_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR2_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13128. EMIF_CTLCFG_DENALI_CTL_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F0_0	R/W	0h	Data to program into memory mode register 2. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.258 EMIF_CTLCFG_DENALI_CTL_207 Register

1 EMIF_CTLCFG_DENALI_CTL_207 Register (Offset = 33Ch) [reset = 0h]

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Table 14-13129. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 833Ch

Figure 14-4337. EMIF_CTLCFG_DENALI_CTL_207 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR0_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR0_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR0_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13131. EMIF_CTLCFG_DENALI_CTL_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F1_0	R/W	0h	Data to program into memory mode register 0. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.259 EMIF_CTLCFG_DENALI_CTL_208 Register

1 EMIF_CTLCFG_DENALI_CTL_208 Register (Offset = 340h) [reset = 0h]

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Table 14-13132. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8340h**

Figure 14-4338. EMIF_CTLCFG_DENALI_CTL_208 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR1_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR1_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR1_DATA_F1_0							
R/W							
0h							

Table 14-13134. EMIF_CTLCFG_DENALI_CTL_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F1_0	R/W	0h	Data to program into memory mode register 1. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.260 EMIF_CTLCFG_DENALI_CTL_209 Register

1 EMIF_CTLCFG_DENALI_CTL_209 Register (Offset = 344h) [reset = 0h]

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Table 14-13135. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8344h**

Figure 14-4339. EMIF_CTLCFG_DENALI_CTL_209 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR2_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR2_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR2_DATA_F1_0							
R/W							
0h							

Table 14-13137. EMIF_CTLCFG_DENALI_CTL_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F1_0	R/W	0h	Data to program into memory mode register 2. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.261 EMIF_CTLCFG_DENALI_CTL_210 Register

1 EMIF_CTLCFG_DENALI_CTL_210 Register (Offset = 348h) [reset = 0h]

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Table 14-13138. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8348h**

Figure 14-4340. EMIF_CTLCFG_DENALI_CTL_210 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR0_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR0_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR0_DATA_F2_0							
R/W							
0h							

Table 14-13140. EMIF_CTLCFG_DENALI_CTL_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F2_0	R/W	0h	Data to program into memory mode register 0. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.262 EMIF_CTLCFG_DENALI_CTL_211 Register

1 EMIF_CTLCFG_DENALI_CTL_211 Register (Offset = 34Ch) [reset = 0h]

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Table 14-13141. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 834Ch**

Figure 14-4341. EMIF_CTLCFG_DENALI_CTL_211 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR1_DATA_F2_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR1_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR1_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13143. EMIF_CTLCFG_DENALI_CTL_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F2_0	R/W	0h	Data to program into memory mode register 1. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.263 EMIF_CTLCFG_DENALI_CTL_212 Register

1 EMIF_CTLCFG_DENALI_CTL_212 Register (Offset = 350h) [reset = 0h]

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Table 14-13144. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8350h**

Figure 14-4342. EMIF_CTLCFG_DENALI_CTL_212 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR2_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR2_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR2_DATA_F2_0							
R/W							
0h							

Table 14-13146. EMIF_CTLCFG_DENALI_CTL_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F2_0	R/W	0h	Data to program into memory mode register 2. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.264 EMIF_CTLCFG_DENALI_CTL_213 Register

1 EMIF_CTLCFG_DENALI_CTL_213 Register (Offset = 354h) [reset = 0h]

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Table 14-13147. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8354h**

Figure 14-4343. EMIF_CTLCFG_DENALI_CTL_213 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR0_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR0_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR0_DATA_F0_1							
R/W							
0h							

Table 14-13149. EMIF_CTLCFG_DENALI_CTL_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F0_1	R/W	0h	Data to program into memory mode register 0. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.265 EMIF_CTLCFG_DENALI_CTL_214 Register

1 EMIF_CTLCFG_DENALI_CTL_214 Register (Offset = 358h) [reset = 0h]

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Table 14-13150. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8358h**

Figure 14-4344. EMIF_CTLCFG_DENALI_CTL_214 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR1_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR1_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR1_DATA_F0_1							
R/W							
0h							

Table 14-13152. EMIF_CTLCFG_DENALI_CTL_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F0_1	R/W	0h	Data to program into memory mode register 1. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.266 EMIF_CTLCFG_DENALI_CTL_215 Register

1 EMIF_CTLCFG_DENALI_CTL_215 Register (Offset = 35Ch) [reset = 0h]

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Table 14-13153. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 835Ch**

Figure 14-4345. EMIF_CTLCFG_DENALI_CTL_215 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							MR2_DATA_F0_1
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
MR2_DATA_F0_1							
R/W							
0h							

7	6	5	4	3	2	1	0
MR2_DATA_F0_1							
R/W							
0h							

Table 14-13155. EMIF_CTLCFG_DENALI_CTL_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F0_1	R/W	0h	Data to program into memory mode register 2. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.267 EMIF_CTLCFG_DENALI_CTL_216 Register

1 EMIF_CTLCFG_DENALI_CTL_216 Register (Offset = 360h) [reset = 0h]

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Table 14-13156. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8360h

Figure 14-4346. EMIF_CTLCFG_DENALI_CTL_216 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR0_DATA_F1_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR0_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR0_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13158. EMIF_CTLCFG_DENALI_CTL_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F1_1	R/W	0h	Data to program into memory mode register 0. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.268 EMIF_CTLCFG_DENALI_CTL_217 Register

1 EMIF_CTLCFG_DENALI_CTL_217 Register (Offset = 364h) [reset = 0h]

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Table 14-13159. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8364h**

Figure 14-4347. EMIF_CTLCFG_DENALI_CTL_217 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR1_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR1_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR1_DATA_F1_1							
R/W							
0h							

Table 14-13161. EMIF_CTLCFG_DENALI_CTL_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F1_1	R/W	0h	Data to program into memory mode register 1. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.269 EMIF_CTLCFG_DENALI_CTL_218 Register

1 EMIF_CTLCFG_DENALI_CTL_218 Register (Offset = 368h) [reset = 0h]

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Table 14-13162. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8368h**

Figure 14-4348. EMIF_CTLCFG_DENALI_CTL_218 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR2_DATA_F1_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR2_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR2_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13164. EMIF_CTLCFG_DENALI_CTL_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F1_1	R/W	0h	Data to program into memory mode register 2. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.270 EMIF_CTLCFG_DENALI_CTL_219 Register

1 EMIF_CTLCFG_DENALI_CTL_219 Register (Offset = 36Ch) [reset = 0h]

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Table 14-13165. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 836Ch**

Figure 14-4349. EMIF_CTLCFG_DENALI_CTL_219 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR0_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR0_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR0_DATA_F2_1							
R/W							
0h							

Table 14-13167. EMIF_CTLCFG_DENALI_CTL_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR0_DATA_F2_1	R/W	0h	Data to program into memory mode register 0. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.271 EMIF_CTLCFG_DENALI_CTL_220 Register

1 EMIF_CTLCFG_DENALI_CTL_220 Register (Offset = 370h) [reset = 0h]

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Table 14-13168. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8370h**

Figure 14-4350. EMIF_CTLCFG_DENALI_CTL_220 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR1_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR1_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR1_DATA_F2_1							
R/W							
0h							

Table 14-13170. EMIF_CTLCFG_DENALI_CTL_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR1_DATA_F2_1	R/W	0h	Data to program into memory mode register 1. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.272 EMIF_CTLCFG_DENALI_CTL_221 Register

1 EMIF_CTLCFG_DENALI_CTL_221 Register (Offset = 374h) [reset = 0h]

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Table 14-13171. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8374h**

Figure 14-4351. EMIF_CTLCFG_DENALI_CTL_221 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR2_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR2_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR2_DATA_F2_1							
R/W							
0h							

Table 14-13173. EMIF_CTLCFG_DENALI_CTL_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR2_DATA_F2_1	R/W	0h	Data to program into memory mode register 2. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.273 EMIF_CTLCFG_DENALI_CTL_222 Register

1 EMIF_CTLCFG_DENALI_CTL_222 Register (Offset = 378h) [reset = 0h]

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Table 14-13174. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8378h**

Figure 14-4352. EMIF_CTLCFG_DENALI_CTL_222 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MRSINGLE_DATA_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MRSINGLE_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MRSINGLE_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13176. EMIF_CTLCFG_DENALI_CTL_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MRSINGLE_DATA_0	R/W	0h	Data to program into memory mode register single write. Reset Source: ctl_amod_g_rst_n

14.5.1.2.274 EMIF_CTLCFG_DENALI_CTL_223 Register

1 EMIF_CTLCFG_DENALI_CTL_223 Register (Offset = 37Ch) [reset = 0h]

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Table 14-13177. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 837Ch

Figure 14-4353. EMIF_CTLCFG_DENALI_CTL_223 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MRSINGLE_DATA_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MRSINGLE_DATA_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MRSINGLE_DATA_1							
R/W							
0h							

Table 14-13179. EMIF_CTLCFG_DENALI_CTL_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MRSINGLE_DATA_1	R/W	0h	Data to program into memory mode register single write. Reset Source: ctl_amod_g_rst_n

14.5.1.2.275 EMIF_CTLCFG_DENALI_CTL_224 Register

1 EMIF_CTLCFG_DENALI_CTL_224 Register (Offset = 380h) [reset = 0h]

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Table 14-13180. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8380h**

Figure 14-4354. EMIF_CTLCFG_DENALI_CTL_224 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR3_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR3_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR3_DATA_F0_0							
R/W							
0h							

Table 14-13182. EMIF_CTLCFG_DENALI_CTL_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F0_0	R/W	0h	Data to program into memory mode register 3. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.276 EMIF_CTLCFG_DENALI_CTL_225 Register

1 EMIF_CTLCFG_DENALI_CTL_225 Register (Offset = 384h) [reset = 0h]

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Table 14-13183. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8384h**

Figure 14-4355. EMIF_CTLCFG_DENALI_CTL_225 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR3_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR3_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR3_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13185. EMIF_CTLCFG_DENALI_CTL_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F1_0	R/W	0h	Data to program into memory mode register 3. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.277 EMIF_CTLCFG_DENALI_CTL_226 Register

1 EMIF_CTLCFG_DENALI_CTL_226 Register (Offset = 388h) [reset = 0h]

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Table 14-13186. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8388h**

Figure 14-4356. EMIF_CTLCFG_DENALI_CTL_226 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR3_DATA_F2_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR3_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR3_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13188. EMIF_CTLCFG_DENALI_CTL_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F2_0	R/W	0h	Data to program into memory mode register 3. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.278 EMIF_CTLCFG_DENALI_CTL_227 Register

1 EMIF_CTLCFG_DENALI_CTL_227 Register (Offset = 38Ch) [reset = 0h]

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Table 14-13189. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 838Ch

Figure 14-4357. EMIF_CTLCFG_DENALI_CTL_227 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR3_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR3_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR3_DATA_F0_1							
R/W							
0h							

Table 14-13191. EMIF_CTLCFG_DENALI_CTL_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F0_1	R/W	0h	Data to program into memory mode register 3. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.279 EMIF_CTLCFG_DENALI_CTL_228 Register

1 EMIF_CTLCFG_DENALI_CTL_228 Register (Offset = 390h) [reset = 0h]

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Table 14-13192. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8390h

Figure 14-4358. EMIF_CTLCFG_DENALI_CTL_228 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR3_DATA_F1_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR3_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR3_DATA_F1_1							
R/W							
0h							

Table 14-13194. EMIF_CTLCFG_DENALI_CTL_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F1_1	R/W	0h	Data to program into memory mode register 3. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.280 EMIF_CTLCFG_DENALI_CTL_229 Register

1 EMIF_CTLCFG_DENALI_CTL_229 Register (Offset = 394h) [reset = 0h]

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Table 14-13195. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8394h**

Figure 14-4359. EMIF_CTLCFG_DENALI_CTL_229 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR3_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR3_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR3_DATA_F2_1							
R/W							
0h							

Table 14-13197. EMIF_CTLCFG_DENALI_CTL_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR3_DATA_F2_1	R/W	0h	Data to program into memory mode register 3. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.281 EMIF_CTLCFG_DENALI_CTL_230 Register

1 EMIF_CTLCFG_DENALI_CTL_230 Register (Offset = 398h) [reset = 0h]

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Table 14-13198. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8398h

Figure 14-4360. EMIF_CTLCFG_DENALI_CTL_230 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR4_DATA_F0_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR4_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR4_DATA_F0_0							
R/W							
0h							

Table 14-13200. EMIF_CTLCFG_DENALI_CTL_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F0_0	R/W	0h	Data to program into memory mode register 4. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.282 EMIF_CTLCFG_DENALI_CTL_231 Register

1 EMIF_CTLCFG_DENALI_CTL_231 Register (Offset = 39Ch) [reset = 0h]

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Table 14-13201. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 839Ch**

Figure 14-4361. EMIF_CTLCFG_DENALI_CTL_231 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR4_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR4_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR4_DATA_F1_0							
R/W							
0h							

Table 14-13203. EMIF_CTLCFG_DENALI_CTL_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F1_0	R/W	0h	Data to program into memory mode register 4. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.283 EMIF_CTLCFG_DENALI_CTL_232 Register

1 EMIF_CTLCFG_DENALI_CTL_232 Register (Offset = 3A0h) [reset = 0h]

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Table 14-13204. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83A0h**

Figure 14-4362. EMIF_CTLCFG_DENALI_CTL_232 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR4_DATA_F2_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR4_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR4_DATA_F2_0							
R/W							
0h							

Table 14-13206. EMIF_CTLCFG_DENALI_CTL_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F2_0	R/W	0h	Data to program into memory mode register 4. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.284 EMIF_CTLCFG_DENALI_CTL_233 Register

1 EMIF_CTLCFG_DENALI_CTL_233 Register (Offset = 3A4h) [reset = 0h]

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Table 14-13207. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83A4h**

Figure 14-4363. EMIF_CTLCFG_DENALI_CTL_233 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR4_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR4_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR4_DATA_F0_1							
R/W							
0h							

Table 14-13209. EMIF_CTLCFG_DENALI_CTL_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F0_1	R/W	0h	Data to program into memory mode register 4. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.285 EMIF_CTLCFG_DENALI_CTL_234 Register

1 EMIF_CTLCFG_DENALI_CTL_234 Register (Offset = 3A8h) [reset = 0h]

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Table 14-13210. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83A8h**

Figure 14-4364. EMIF_CTLCFG_DENALI_CTL_234 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR4_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR4_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR4_DATA_F1_1							
R/W							
0h							

Table 14-13212. EMIF_CTLCFG_DENALI_CTL_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F1_1	R/W	0h	Data to program into memory mode register 4. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.286 EMIF_CTLCFG_DENALI_CTL_235 Register

1 EMIF_CTLCFG_DENALI_CTL_235 Register (Offset = 3ACh) [reset = 0h]

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Table 14-13213. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 83ACh

Figure 14-4365. EMIF_CTLCFG_DENALI_CTL_235 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR4_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR4_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR4_DATA_F2_1							
R/W							
0h							

Table 14-13215. EMIF_CTLCFG_DENALI_CTL_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR4_DATA_F2_1	R/W	0h	Data to program into memory mode register 4. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.287 EMIF_CTLCFG_DENALI_CTL_236 Register

1 EMIF_CTLCFG_DENALI_CTL_236 Register (Offset = 3B0h) [reset = 0h]

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Table 14-13216. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83B0h**

Figure 14-4366. EMIF_CTLCFG_DENALI_CTL_236 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR5_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR5_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR5_DATA_F0_0							
R/W							
0h							

Table 14-13218. EMIF_CTLCFG_DENALI_CTL_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F0_0	R/W	0h	Data to program into memory mode register 5. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.288 EMIF_CTLCFG_DENALI_CTL_237 Register

1 EMIF_CTLCFG_DENALI_CTL_237 Register (Offset = 3B4h) [reset = 0h]

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Table 14-13219. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83B4h**

Figure 14-4367. EMIF_CTLCFG_DENALI_CTL_237 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR5_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR5_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR5_DATA_F1_0							
R/W							
0h							

Table 14-13221. EMIF_CTLCFG_DENALI_CTL_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F1_0	R/W	0h	Data to program into memory mode register 5. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.289 EMIF_CTLCFG_DENALI_CTL_238 Register

1 EMIF_CTLCFG_DENALI_CTL_238 Register (Offset = 3B8h) [reset = 0h]

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Table 14-13222. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83B8h**

Figure 14-4368. EMIF_CTLCFG_DENALI_CTL_238 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR5_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR5_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR5_DATA_F2_0							
R/W							
0h							

Table 14-13224. EMIF_CTLCFG_DENALI_CTL_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F2_0	R/W	0h	Data to program into memory mode register 5. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.290 EMIF_CTLCFG_DENALI_CTL_239 Register

1 EMIF_CTLCFG_DENALI_CTL_239 Register (Offset = 3BCh) [reset = 0h]

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Table 14-13225. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83BCh**

Figure 14-4369. EMIF_CTLCFG_DENALI_CTL_239 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR5_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR5_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR5_DATA_F0_1							
R/W							
0h							

Table 14-13227. EMIF_CTLCFG_DENALI_CTL_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F0_1	R/W	0h	Data to program into memory mode register 5. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.291 EMIF_CTLCFG_DENALI_CTL_240 Register

1 EMIF_CTLCFG_DENALI_CTL_240 Register (Offset = 3C0h) [reset = 0h]

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Table 14-13228. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83C0h**

Figure 14-4370. EMIF_CTLCFG_DENALI_CTL_240 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR5_DATA_F1_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR5_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR5_DATA_F1_1							
R/W							
0h							

Table 14-13230. EMIF_CTLCFG_DENALI_CTL_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F1_1	R/W	0h	Data to program into memory mode register 5. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.292 EMIF_CTLCFG_DENALI_CTL_241 Register

1 EMIF_CTLCFG_DENALI_CTL_241 Register (Offset = 3C4h) [reset = 0h]

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Table 14-13231. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83C4h**

Figure 14-4371. EMIF_CTLCFG_DENALI_CTL_241 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR5_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR5_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR5_DATA_F2_1							
R/W							
0h							

Table 14-13233. EMIF_CTLCFG_DENALI_CTL_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR5_DATA_F2_1	R/W	0h	Data to program into memory mode register 5. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.293 EMIF_CTLCFG_DENALI_CTL_242 Register

1 EMIF_CTLCFG_DENALI_CTL_242 Register (Offset = 3C8h) [reset = 0h]

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Table 14-13234. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83C8h**

Figure 14-4372. EMIF_CTLCFG_DENALI_CTL_242 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR6_DATA_F0_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR6_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR6_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13236. EMIF_CTLCFG_DENALI_CTL_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F0_0	R/W	0h	Data to program into memory mode register 6. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.294 EMIF_CTLCFG_DENALI_CTL_243 Register

1 EMIF_CTLCFG_DENALI_CTL_243 Register (Offset = 3CCh) [reset = 0h]

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Table 14-13237. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83CCh**

Figure 14-4373. EMIF_CTLCFG_DENALI_CTL_243 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR6_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR6_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR6_DATA_F1_0							
R/W							
0h							

Table 14-13239. EMIF_CTLCFG_DENALI_CTL_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F1_0	R/W	0h	Data to program into memory mode register 6. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.295 EMIF_CTLCFG_DENALI_CTL_244 Register

1 EMIF_CTLCFG_DENALI_CTL_244 Register (Offset = 3D0h) [reset = 0h]

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Table 14-13240. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83D0h**

Figure 14-4374. EMIF_CTLCFG_DENALI_CTL_244 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR6_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR6_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR6_DATA_F2_0							
R/W							
0h							

Table 14-13242. EMIF_CTLCFG_DENALI_CTL_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F2_0	R/W	0h	Data to program into memory mode register 6. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.296 EMIF_CTLCFG_DENALI_CTL_245 Register

1 EMIF_CTLCFG_DENALI_CTL_245 Register (Offset = 3D4h) [reset = 0h]

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Table 14-13243. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83D4h**

Figure 14-4375. EMIF_CTLCFG_DENALI_CTL_245 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR6_DATA_F0_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR6_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR6_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13245. EMIF_CTLCFG_DENALI_CTL_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F0_1	R/W	0h	Data to program into memory mode register 6. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.297 EMIF_CTLCFG_DENALI_CTL_246 Register

1 EMIF_CTLCFG_DENALI_CTL_246 Register (Offset = 3D8h) [reset = 0h]

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Table 14-13246. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83D8h**

Figure 14-4376. EMIF_CTLCFG_DENALI_CTL_246 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR6_DATA_F1_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR6_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR6_DATA_F1_1							
R/W							
0h							

Table 14-13248. EMIF_CTLCFG_DENALI_CTL_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F1_1	R/W	0h	Data to program into memory mode register 6. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.298 EMIF_CTLCFG_DENALI_CTL_247 Register

1 EMIF_CTLCFG_DENALI_CTL_247 Register (Offset = 3DCh) [reset = 0h]

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Table 14-13249. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83DCh**

Figure 14-4377. EMIF_CTLCFG_DENALI_CTL_247 Name Register

31	30	29	28	27	26	25	24
MR8_DATA_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR6_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR6_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR6_DATA_F2_1							
R/W							
0h							

Table 14-13251. EMIF_CTLCFG_DENALI_CTL_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR8_DATA_0	R	0h	Data to program into memory mode register 8 for each chip select. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	MR6_DATA_F2_1	R/W	0h	Data to program into memory mode register 6. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.299 EMIF_CTLCFG_DENALI_CTL_248 Register

1 EMIF_CTLCFG_DENALI_CTL_248 Register (Offset = 3E0h) [reset = 0h]

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Table 14-13252. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83E0h**

Figure 14-4378. EMIF_CTLCFG_DENALI_CTL_248 Name Register

31	30	29	28	27	26	25	24
RESERVED							MR10_DATA_F0_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MR10_DATA_F0_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR10_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR8_DATA_1							
R							
0h							

Table 14-13254. EMIF_CTLCFG_DENALI_CTL_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	MR10_DATA_F0_0	R/W	0h	Data to program into memory mode register 10. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	MR8_DATA_1	R	0h	Data to program into memory mode register 8 for each chip select. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.300 EMIF_CTLCFG_DENALI_CTL_249 Register

1 EMIF_CTLCFG_DENALI_CTL_249 Register (Offset = 3E4h) [reset = 0h]

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Table 14-13255. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83E4h**

Figure 14-4379. EMIF_CTLCFG_DENALI_CTL_249 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR10_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR10_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR10_DATA_F1_0							
R/W							
0h							

Table 14-13257. EMIF_CTLCFG_DENALI_CTL_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F1_0	R/W	0h	Data to program into memory mode register 10. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.301 EMIF_CTLCFG_DENALI_CTL_250 Register

1 EMIF_CTLCFG_DENALI_CTL_250 Register (Offset = 3E8h) [reset = 0h]

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Table 14-13258. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83E8h**

Figure 14-4380. EMIF_CTLCFG_DENALI_CTL_250 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR10_DATA_F2_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR10_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR10_DATA_F2_0							
R/W							
0h							

Table 14-13260. EMIF_CTLCFG_DENALI_CTL_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F2_0	R/W	0h	Data to program into memory mode register 10. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.302 EMIF_CTLCFG_DENALI_CTL_251 Register

1 EMIF_CTLCFG_DENALI_CTL_251 Register (Offset = 3ECh) [reset = 0h]

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Table 14-13261. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83ECh**

Figure 14-4381. EMIF_CTLCFG_DENALI_CTL_251 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR10_DATA_F0_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR10_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR10_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13263. EMIF_CTLCFG_DENALI_CTL_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F0_1	R/W	0h	Data to program into memory mode register 10. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.303 EMIF_CTLCFG_DENALI_CTL_252 Register

1 EMIF_CTLCFG_DENALI_CTL_252 Register (Offset = 3F0h) [reset = 0h]

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Table 14-13264. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83F0h**

Figure 14-4382. EMIF_CTLCFG_DENALI_CTL_252 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR10_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR10_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR10_DATA_F1_1							
R/W							
0h							

Table 14-13266. EMIF_CTLCFG_DENALI_CTL_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F1_1	R/W	0h	Data to program into memory mode register 10. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.304 EMIF_CTLCFG_DENALI_CTL_253 Register

1 EMIF_CTLCFG_DENALI_CTL_253 Register (Offset = 3F4h) [reset = 0h]

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Table 14-13267. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83F4h**

Figure 14-4383. EMIF_CTLCFG_DENALI_CTL_253 Name Register

31	30	29	28	27	26	25	24
MR11_DATA_F0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR10_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR10_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR10_DATA_F2_1							
R/W							
0h							

Table 14-13269. EMIF_CTLCFG_DENALI_CTL_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR11_DATA_F0_0	R/W	0h	Data to program into memory mode register 11. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	MR10_DATA_F2_1	R/W	0h	Data to program into memory mode register 10. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.305 EMIF_CTLCFG_DENALI_CTL_254 Register

1 EMIF_CTLCFG_DENALI_CTL_254 Register (Offset = 3F8h) [reset = 0h]

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Table 14-13270. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 83F8h**

Figure 14-4384. EMIF_CTLCFG_DENALI_CTL_254 Name Register

31	30	29	28	27	26	25	24
MR11_DATA_F1_1							
R/W							
0h							
23	22	21	20	19	18	17	16
MR11_DATA_F0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
MR11_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR11_DATA_F1_0							
R/W							
0h							

Table 14-13272. EMIF_CTLCFG_DENALI_CTL_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR11_DATA_F1_1	R/W	0h	Data to program into memory mode register 11. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	MR11_DATA_F0_1	R/W	0h	Data to program into memory mode register 11. FC=0 Reset Source: ctl_amod_g_rst_n
15:8	MR11_DATA_F2_0	R/W	0h	Data to program into memory mode register 11. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	MR11_DATA_F1_0	R/W	0h	Data to program into memory mode register 11. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.306 EMIF_CTLCFG_DENALI_CTL_255 Register

1 EMIF_CTLCFG_DENALI_CTL_255 Register (Offset = 3FCh) [reset = 0h]

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Table 14-13273. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 83FCh

Figure 14-4385. EMIF_CTLCFG_DENALI_CTL_255 Name Register

31	30	29	28	27	26	25	24
RESERVED							MR12_DATA_F0_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
MR12_DATA_F0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
MR12_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR11_DATA_F2_1							
R/W							
0h							

Table 14-13275. EMIF_CTLCFG_DENALI_CTL_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	MR12_DATA_F0_0	R/W	0h	Data to program into memory mode register 12. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	MR11_DATA_F2_1	R/W	0h	Data to program into memory mode register 11. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.307 EMIF_CTLCFG_DENALI_CTL_256 Register

1 EMIF_CTLCFG_DENALI_CTL_256 Register (Offset = 400h) [reset = 0h]

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Table 14-13276. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8400h**

Figure 14-4386. EMIF_CTLCFG_DENALI_CTL_256 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR12_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR12_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR12_DATA_F1_0							
R/W							
0h							

Table 14-13278. EMIF_CTLCFG_DENALI_CTL_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F1_0	R/W	0h	Data to program into memory mode register 12. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.308 EMIF_CTLCFG_DENALI_CTL_257 Register

1 EMIF_CTLCFG_DENALI_CTL_257 Register (Offset = 404h) [reset = 0h]

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Table 14-13279. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 8404h**

Figure 14-4387. EMIF_CTLCFG_DENALI_CTL_257 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR12_DATA_F2_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR12_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR12_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13281. EMIF_CTLCFG_DENALI_CTL_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F2_0	R/W	0h	Data to program into memory mode register 12. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.309 EMIF_CTLCFG_DENALI_CTL_258 Register

1 EMIF_CTLCFG_DENALI_CTL_258 Register (Offset = 408h) [reset = 0h]

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Table 14-13282. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8408h**

Figure 14-4388. EMIF_CTLCFG_DENALI_CTL_258 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR12_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR12_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR12_DATA_F0_1							
R/W							
0h							

Table 14-13284. EMIF_CTLCFG_DENALI_CTL_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F0_1	R/W	0h	Data to program into memory mode register 12. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.310 EMIF_CTLCFG_DENALI_CTL_259 Register

1 EMIF_CTLCFG_DENALI_CTL_259 Register (Offset = 40Ch) [reset = 0h]

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Table 14-13285. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 840Ch**

Figure 14-4389. EMIF_CTLCFG_DENALI_CTL_259 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR12_DATA_F1_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR12_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR12_DATA_F1_1							
R/W							
0h							

Table 14-13287. EMIF_CTLCFG_DENALI_CTL_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F1_1	R/W	0h	Data to program into memory mode register 12. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.311 EMIF_CTLCFG_DENALI_CTL_260 Register

1 EMIF_CTLCFG_DENALI_CTL_260 Register (Offset = 410h) [reset = 0h]

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Table 14-13288. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8410h**

Figure 14-4390. EMIF_CTLCFG_DENALI_CTL_260 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR12_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR12_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR12_DATA_F2_1							
R/W							
0h							

Table 14-13290. EMIF_CTLCFG_DENALI_CTL_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR12_DATA_F2_1	R/W	0h	Data to program into memory mode register 12. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.312 EMIF_CTLCFG_DENALI_CTL_261 Register

1 EMIF_CTLCFG_DENALI_CTL_261 Register (Offset = 414h) [reset = 0h]

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Table 14-13291. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8414h**

Figure 14-4391. EMIF_CTLCFG_DENALI_CTL_261 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR13_DATA_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR13_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR13_DATA_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13293. EMIF_CTLCFG_DENALI_CTL_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR13_DATA_0	R/W	0h	Data to program into memory mode register 13. Reset Source: ctl_amod_g_rst_n

14.5.1.2.313 EMIF_CTLCFG_DENALI_CTL_262 Register

1 EMIF_CTLCFG_DENALI_CTL_262 Register (Offset = 418h) [reset = 0h]

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Table 14-13294. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8418h

Figure 14-4392. EMIF_CTLCFG_DENALI_CTL_262 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR13_DATA_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR13_DATA_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR13_DATA_1							
R/W							
0h							

Table 14-13296. EMIF_CTLCFG_DENALI_CTL_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR13_DATA_1	R/W	0h	Data to program into memory mode register 13. Reset Source: ctl_amod_g_rst_n

14.5.1.2.314 EMIF_CTLCFG_DENALI_CTL_263 Register

1 EMIF_CTLCFG_DENALI_CTL_263 Register (Offset = 41Ch) [reset = 0h]

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Table 14-13297. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 841Ch**

Figure 14-4393. EMIF_CTLCFG_DENALI_CTL_263 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR14_DATA_F0_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR14_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR14_DATA_F0_0							
R/W							
0h							

Table 14-13299. EMIF_CTLCFG_DENALI_CTL_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F0_0	R/W	0h	Data to program into memory mode register 14. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.315 EMIF_CTLCFG_DENALI_CTL_264 Register

1 EMIF_CTLCFG_DENALI_CTL_264 Register (Offset = 420h) [reset = 0h]

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Table 14-13300. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8420h**

Figure 14-4394. EMIF_CTLCFG_DENALI_CTL_264 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR14_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR14_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR14_DATA_F1_0							
R/W							
0h							

Table 14-13302. EMIF_CTLCFG_DENALI_CTL_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F1_0	R/W	0h	Data to program into memory mode register 14. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.316 EMIF_CTLCFG_DENALI_CTL_265 Register

1 EMIF_CTLCFG_DENALI_CTL_265 Register (Offset = 424h) [reset = 0h]

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Table 14-13303. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8424h**

Figure 14-4395. EMIF_CTLCFG_DENALI_CTL_265 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR14_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR14_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR14_DATA_F2_0							
R/W							
0h							

Table 14-13305. EMIF_CTLCFG_DENALI_CTL_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F2_0	R/W	0h	Data to program into memory mode register 14. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.317 EMIF_CTLCFG_DENALI_CTL_266 Register

1 EMIF_CTLCFG_DENALI_CTL_266 Register (Offset = 428h) [reset = 0h]

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Table 14-13306. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8428h**

Figure 14-4396. EMIF_CTLCFG_DENALI_CTL_266 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR14_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR14_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR14_DATA_F0_1							
R/W							
0h							

Table 14-13308. EMIF_CTLCFG_DENALI_CTL_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F0_1	R/W	0h	Data to program into memory mode register 14. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.318 EMIF_CTLCFG_DENALI_CTL_267 Register

1 EMIF_CTLCFG_DENALI_CTL_267 Register (Offset = 42Ch) [reset = 0h]

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Table 14-13309. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 842Ch

Figure 14-4397. EMIF_CTLCFG_DENALI_CTL_267 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR14_DATA_F1_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR14_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR14_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13311. EMIF_CTLCFG_DENALI_CTL_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F1_1	R/W	0h	Data to program into memory mode register 14. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.319 EMIF_CTLCFG_DENALI_CTL_268 Register

1 EMIF_CTLCFG_DENALI_CTL_268 Register (Offset = 430h) [reset = 0h]

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Table 14-13312. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8430h**

Figure 14-4398. EMIF_CTLCFG_DENALI_CTL_268 Name Register

31	30	29	28	27	26	25	24
MR16_DATA_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR14_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR14_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR14_DATA_F2_1							
R/W							
0h							

Table 14-13314. EMIF_CTLCFG_DENALI_CTL_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR16_DATA_0	R/W	0h	Data to program into memory mode register 16. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	MR14_DATA_F2_1	R/W	0h	Data to program into memory mode register 14. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.320 EMIF_CTLCFG_DENALI_CTL_269 Register

1 EMIF_CTLCFG_DENALI_CTL_269 Register (Offset = 434h) [reset = 0h]

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Table 14-13315. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8434h**

Figure 14-4399. EMIF_CTLCFG_DENALI_CTL_269 Name Register

31	30	29	28	27	26	25	24
MR20_DATA_0							
R/W							
0h							
23	22	21	20	19	18	17	16
MR17_DATA_1							
R/W							
0h							
15	14	13	12	11	10	9	8
MR17_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR16_DATA_1							
R/W							
0h							

Table 14-13317. EMIF_CTLCFG_DENALI_CTL_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MR20_DATA_0	R/W	0h	Data to program into memory mode register 20. Reset Source: ctl_amod_g_rst_n
23:16	MR17_DATA_1	R/W	0h	Data to program into memory mode register 17. Reset Source: ctl_amod_g_rst_n
15:8	MR17_DATA_0	R/W	0h	Data to program into memory mode register 17. Reset Source: ctl_amod_g_rst_n
7:0	MR16_DATA_1	R/W	0h	Data to program into memory mode register 16. Reset Source: ctl_amod_g_rst_n

14.5.1.2.321 EMIF_CTLCFG_DENALI_CTL_270 Register

1 EMIF_CTLCFG_DENALI_CTL_270 Register (Offset = 438h) [reset = 0h]

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Table 14-13318. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8438h**

Figure 14-4400. EMIF_CTLCFG_DENALI_CTL_270 Name Register

31	30	29	28	27	26	25	24
RESERVED							MR22_DATA_F0_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MR22_DATA_F0_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR22_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR20_DATA_1							
R/W							
0h							

Table 14-13320. EMIF_CTLCFG_DENALI_CTL_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	MR22_DATA_F0_0	R/W	0h	Data to program into memory mode register 22. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	MR20_DATA_1	R/W	0h	Data to program into memory mode register 20. Reset Source: ctl_amod_g_rst_n

14.5.1.2.322 EMIF_CTLCFG_DENALI_CTL_271 Register

1 EMIF_CTLCFG_DENALI_CTL_271 Register (Offset = 43Ch) [reset = 0h]

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Table 14-13321. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 843Ch

Figure 14-4401. EMIF_CTLCFG_DENALI_CTL_271 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR22_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR22_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MR22_DATA_F1_0							
R/W							
0h							

Table 14-13323. EMIF_CTLCFG_DENALI_CTL_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F1_0	R/W	0h	Data to program into memory mode register 22. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.323 EMIF_CTLCFG_DENALI_CTL_272 Register

1 EMIF_CTLCFG_DENALI_CTL_272 Register (Offset = 440h) [reset = 0h]

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Table 14-13324. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8440h**

Figure 14-4402. EMIF_CTLCFG_DENALI_CTL_272 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MR22_DATA_F2_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MR22_DATA_F2_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR22_DATA_F2_0							
R/W							
0h							

Table 14-13326. EMIF_CTLCFG_DENALI_CTL_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F2_0	R/W	0h	Data to program into memory mode register 22. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.324 EMIF_CTLCFG_DENALI_CTL_273 Register

1 EMIF_CTLCFG_DENALI_CTL_273 Register (Offset = 444h) [reset = 0h]

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Table 14-13327. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8444h**

Figure 14-4403. EMIF_CTLCFG_DENALI_CTL_273 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR22_DATA_F0_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR22_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR22_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13329. EMIF_CTLCFG_DENALI_CTL_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F0_1	R/W	0h	Data to program into memory mode register 22. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.325 EMIF_CTLCFG_DENALI_CTL_274 Register

1 EMIF_CTLCFG_DENALI_CTL_274 Register (Offset = 448h) [reset = 0h]

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Table 14-13330. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 8448h**

Figure 14-4404. EMIF_CTLCFG_DENALI_CTL_274 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR22_DATA_F1_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR22_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR22_DATA_F1_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13332. EMIF_CTLCFG_DENALI_CTL_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F1_1	R/W	0h	Data to program into memory mode register 22. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.326 EMIF_CTLCFG_DENALI_CTL_275 Register

1 EMIF_CTLCFG_DENALI_CTL_275 Register (Offset = 44Ch) [reset = 0h]

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Table 14-13333. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 844Ch**

Figure 14-4405. EMIF_CTLCFG_DENALI_CTL_275 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MR22_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MR22_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
MR22_DATA_F2_1							
R/W							
0h							

Table 14-13335. EMIF_CTLCFG_DENALI_CTL_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	MR22_DATA_F2_1	R/W	0h	Data to program into memory mode register 22. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.327 EMIF_CTLCFG_DENALI_CTL_276 Register

1 EMIF_CTLCFG_DENALI_CTL_276 Register (Offset = 450h) [reset = 0h]

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Table 14-13336. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8450h**

Figure 14-4406. EMIF_CTLCFG_DENALI_CTL_276 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR_FSP_DATA_VALID_F0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MR23_DATA</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MR23_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MR23_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13338. EMIF_CTLCFG_DENALI_CTL_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MR_FSP_DATA_VALID_F0	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter[s]. Value of 1 means memory was trained. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	MR23_DATA	R/W	0h	Data to program into memory mode register 23. Reset Source: ctl_amod_g_rst_n

14.5.1.2.328 EMIF_CTLCFG_DENALI_CTL_277 Register

1 EMIF_CTLCFG_DENALI_CTL_277 Register (Offset = 454h) [reset = 10000h]

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Table 14-13339. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 8454h**

Figure 14-4407. EMIF_CTLCFG_DENALI_CTL_277 Name Register

31	30	29	28	27	26	25	24
RESERVED							DFS_FSP_INSYNC_INACTIVE
NONE							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							DFS_FSP_INSYNC_ACTIVE
NONE							R
0h							1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							MR_FSP_DATA_VALID_F2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							MR_FSP_DATA_VALID_F1
NONE							R/W
0h							0h

Table 14-13341. EMIF_CTLCFG_DENALI_CTL_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	DFS_FSP_INSYNC_INACTIVE	R	0h	When cleared, this indicates that the contents in memcd_param is new that the values in memory's MRx FSP reg and if a dfs occurs, they need to be updated. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	DFS_FSP_INSYNC_ACTIVE	R	1h	When cleared, this indicates that the contents in memcd_param is new that the values in memory's MRx FSP reg and if a dfs occurs, they need to be updated. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	MR_FSP_DATA_VALID_F2	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter[s]. Value of 1 means memory was trained. FC=2 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-13341. EMIF_CTLCFG_DENALI_CTL_277 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MR_FSP_DATA_VALID_F1	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter[s]. Value of 1 means memory was trained. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.329 EMIF_CTLCFG_DENALI_CTL_278 Register

1 EMIF_CTLCFG_DENALI_CTL_278 Register (Offset = 458h) [reset = 0h]

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Table 14-13342. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8458h**

Figure 14-4408. EMIF_CTLCFG_DENALI_CTL_278 Name Register

31	30	29	28	27	26	25	24
RESERVED							FSP_OP_CURRENT
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							FSP_STATUS
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							DFS_ALWAYS_WRITE_FSP
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							FSP_PHY_UPDATE_MRW
NONE							R/W
0h							0h

Table 14-13344. EMIF_CTLCFG_DENALI_CTL_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	FSP_OP_CURRENT	R/W	0h	Reports which FSP set the memory is currently using. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	FSP_STATUS	R/W	0h	Indicates that a DFS event caused the FSP mode registers to be updated. Value of 1 means that the FSP mode registers were changed. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	DFS_ALWAYS_WRITE_FSP	R/W	0h	Forces all FSP mode registers to be written by the controller during a DFS event. Set to 1 to force the write. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	FSP_PHY_UPDATE_MRW	R/W	0h	Identifies the logic responsible for updating MR12 and MR14 in memory. Clear to 0 for the controller, or set to 1 for the PHY or PI. Reset Source: ctl_amod_g_rst_n

14.5.1.2.330 EMIF_CTLCFG_DENALI_CTL_279 Register

1 EMIF_CTLCFG_DENALI_CTL_279 Register (Offset = 45Ch) [reset = 0h]

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Table 14-13345. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 845Ch**

Figure 14-4409. EMIF_CTLCFG_DENALI_CTL_279 Name Register

31	30	29	28	27	26	25	24
RESERVED						FSP0_FRC	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED							FSP1_FRC_VALID
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							FSP0_FRC_VALID
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							FSP_WR_CURRENT
NONE							R/W
0h							0h

Table 14-13347. EMIF_CTLCFG_DENALI_CTL_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	FSP0_FRC	R/W	0h	Identifies which of the controller's frequency copy is associated with FSP0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	FSP1_FRC_VALID	R/W	0h	Specifies whether the FSP set defined in the FSP1_FRC parameter reflects the frequency used to program the FSP1 registers. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	FSP0_FRC_VALID	R/W	0h	Specifies whether the FSP set defined in the FSP0_FRC parameter reflects the frequency used to program the FSP0 registers. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	FSP_WR_CURRENT	R/W	0h	Reports which FSP set the memory will target with write commands. Reset Source: ctl_amod_g_rst_n

14.5.1.2.331 EMIF_CTLCFG_DENALI_CTL_280 Register

1 EMIF_CTLCFG_DENALI_CTL_280 Register (Offset = 460h) [reset = 0h]

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Table 14-13348. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8460h**

Figure 14-4410. EMIF_CTLCFG_DENALI_CTL_280 Name Register

31	30	29	28	27	26	25	24
RESERVED		ADDR_SPACE					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						BIST_RESULT	
NONE						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							BIST_GO
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						FSP1_FRC	
NONE						R/W	
0h						0h	

Table 14-13350. EMIF_CTLCFG_DENALI_CTL_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	ADDR_SPACE	R/W	0h	Sets the number of address bits to check during BIST operation. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	BIST_RESULT	R	0h	BIST operation status [pass/fail]. Bit [0] indicates data check status and bit [1] indicates address check status. Value of 1 is a passing result. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	BIST_GO	W	0h	Initiate a BIST operation. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	FSP1_FRC	R/W	0h	Identifies which of the controller's frequency copy is associated with FSP1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.332 EMIF_CTLCFG_DENALI_CTL_281 Register

1 EMIF_CTLCFG_DENALI_CTL_281 Register (Offset = 464h) [reset = 0h]

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Table 14-13351. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8464h**

Figure 14-4411. EMIF_CTLCFG_DENALI_CTL_281 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							BIST_ADDR_CHECK
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							BIST_DATA_CHECK
NONE							R/W
0h							0h

Table 14-13353. EMIF_CTLCFG_DENALI_CTL_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	BIST_ADDR_CHECK	R/W	0h	Enable address checking with BIST operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	BIST_DATA_CHECK	R/W	0h	Enable data checking with BIST operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.333 EMIF_CTLCFG_DENALI_CTL_282 Register

1 EMIF_CTLCFG_DENALI_CTL_282 Register (Offset = 468h) [reset = 0h]

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Table 14-13354. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8468h**

Figure 14-4412. EMIF_CTLCFG_DENALI_CTL_282 Name Register

31	30	29	28	27	26	25	24
BIST_START_ADDRESS_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BIST_START_ADDRESS_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIST_START_ADDRESS_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_START_ADDRESS_0							
R/W							
0h							

Table 14-13356. EMIF_CTLCFG_DENALI_CTL_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_START_ADDRESS_0	R/W	0h	Start BIST checking at this address. Reset Source: ctl_amod_g_rst_n

14.5.1.2.334 EMIF_CTLCFG_DENALI_CTL_283 Register

1 EMIF_CTLCFG_DENALI_CTL_283 Register (Offset = 46Ch) [reset = 0h]

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Table 14-13357. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 846Ch**

Figure 14-4413. EMIF_CTLCFG_DENALI_CTL_283 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							BIST_START_ADDRESS_1
NONE							R/W
0h							0h

Table 14-13359. EMIF_CTLCFG_DENALI_CTL_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	BIST_START_ADDRESS_1	R/W	0h	Start BIST checking at this address. Reset Source: ctl_amod_g_rst_n

14.5.1.2.335 EMIF_CTLCFG_DENALI_CTL_284 Register

1 EMIF_CTLCFG_DENALI_CTL_284 Register (Offset = 470h) [reset = 0h]

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Table 14-13360. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8470h**

Figure 14-4414. EMIF_CTLCFG_DENALI_CTL_284 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
BIST_DATA_MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
BIST_DATA_MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
BIST_DATA_MASK							
R/W							
0h							

Table 14-13362. EMIF_CTLCFG_DENALI_CTL_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_MASK	R/W	0h	Mask applied to data for BIST error checking. Bit [0] controls memory data path bit [0], bit [1] controls memory data path bit [1], etc. Set each bit to 1 to mask. Reset Source: ctl_amod_g_rst_n

14.5.1.2.336 EMIF_CTLCFG_DENALI_CTL_285 Register

1 EMIF_CTLCFG_DENALI_CTL_285 Register (Offset = 474h) [reset = 0h]

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Table 14-13363. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8474h**

Figure 14-4415. EMIF_CTLCFG_DENALI_CTL_285 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					BIST_TEST_MODE		
NONE					R/W		
0h					0h		

Table 14-13365. EMIF_CTLCFG_DENALI_CTL_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	BIST_TEST_MODE	R/W	0h	Sets the BIST test mode. Value of 0 specifies standard BIST operation, value of 1 specifies a reduced BIST operation, value of 2 specifies a self-refresh retention test, value of 3 specifies an idle retention test, and value of 4 specifies memory initalization function. All other values are reserved. Reset Source: ctl_amod_g_rst_n

14.5.1.2.337 EMIF_CTLCFG_DENALI_CTL_286 Register

1 EMIF_CTLCFG_DENALI_CTL_286 Register (Offset = 478h) [reset = 0h]

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Table 14-13366. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8478h**

Figure 14-4416. EMIF_CTLCFG_DENALI_CTL_286 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_PATTERN_0							
R/W							
0h							
23	22	21	20	19	18	17	16
BIST_DATA_PATTERN_0							
R/W							
0h							
15	14	13	12	11	10	9	8
BIST_DATA_PATTERN_0							
R/W							
0h							
7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_0							
R/W							
0h							

Table 14-13368. EMIF_CTLCFG_DENALI_CTL_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_PATTERN_0	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4. Only data corresponding to active portion of core word will be used while inactive portion will be ignored. Reset Source: ctl_amod_g_rst_n

14.5.1.2.338 EMIF_CTLCFG_DENALI_CTL_287 Register

1 EMIF_CTLCFG_DENALI_CTL_287 Register (Offset = 47Ch) [reset = 0h]

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Table 14-13369. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 847Ch**

Figure 14-4417. EMIF_CTLCFG_DENALI_CTL_287 Name Register

31	30	29	28	27	26	25	24
BIST_DATA_PATTERN_1							
R/W							
0h							
23	22	21	20	19	18	17	16
BIST_DATA_PATTERN_1							
R/W							
0h							
15	14	13	12	11	10	9	8
BIST_DATA_PATTERN_1							
R/W							
0h							
7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_1							
R/W							
0h							

Table 14-13371. EMIF_CTLCFG_DENALI_CTL_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_DATA_PATTERN_1	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4. Only data corresponding to active portion of core word will be used while inactive portion will be ignored. Reset Source: ctl_amod_g_rst_n

14.5.1.2.339 EMIF_CTLCFG_DENALI_CTL_288 Register

1 EMIF_CTLCFG_DENALI_CTL_288 Register (Offset = 480h) [reset = 0h]

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Table 14-13372. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8480h

Figure 14-4418. EMIF_CTLCFG_DENALI_CTL_288 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				BIST_ERR_STOP			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIST_ERR_STOP							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							BIST_RET_STATE
NONE							R
0h							0h

Table 14-13374. EMIF_CTLCFG_DENALI_CTL_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	BIST_ERR_STOP	R/W	0h	Defines the maximum number of error occurrences allowed prior to quitting when the BIST_TEST_MODE parameter is programmed to 1, 2 or 3. A value of 0 will allow the test to run to completion. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	BIST_RET_STATE	R	0h	Indicates if BIST is in a retention wait state, used when the BIST_TEST_MODE parameter is programmed to 2 or 3. Value of 1 indicates BIST is waiting. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.340 EMIF_CTLCFG_DENALI_CTL_289 Register

1 EMIF_CTLCFG_DENALI_CTL_289 Register (Offset = 484h) [reset = 0h]

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Table 14-13375. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8484h**

Figure 14-4419. EMIF_CTLCFG_DENALI_CTL_289 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">LONG_COUNT_MASK</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>BIST_RET_STATE_EXIT</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">BIST_ERR_COUNT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BIST_ERR_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13377. EMIF_CTLCFG_DENALI_CTL_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	LONG_COUNT_MASK	R/W	0h	Reduces the length of the long counter from 1024 cycles. The only supported values are 0x00 [1024 cycles], 0x10 [512 clocks], 0x18 [256 clocks], 0x1C [128 clocks], 0x1E [64 clocks] and 0x1F [32 clocks]. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	BIST_RET_STATE_EXIT	W	0h	Exit self-refresh or idle retention state, used when the BIST_TEST_MODE parameter is programmed to 2 or 3. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	BIST_ERR_COUNT	R	0h	Indicates the number of BIST errors found when the BIST_TEST_MODE parameter is programmed to 1, 2 or 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.341 EMIF_CTLCFG_DENALI_CTL_290 Register

1 EMIF_CTLCFG_DENALI_CTL_290 Register (Offset = 488h) [reset = 0h]

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Table 14-13378. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8488h

Figure 14-4420. EMIF_CTLCFG_DENALI_CTL_290 Name Register

31	30	29	28	27	26	25	24
RESERVED			AREF_MAX_CREDIT				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			AREF_MAX_DEFICIT				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			AREF_HIGH_THRESHOLD				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			AREF_NORM_THRESHOLD				
NONE			R/W				
0h			0h				

Table 14-13380. EMIF_CTLCFG_DENALI_CTL_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	AREF_MAX_CREDIT	R/W	0h	AREF number of posted refreshes until the maximum number of refresh credits has been reached. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	AREF_MAX_DEFICIT	R/W	0h	AREF number of pending refreshes until the maximum number of refreshes has been exceeded. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	AREF_HIGH_THRESHOLD	R/W	0h	AREF number of pending refreshes until the high priority request is asserted. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	AREF_NORM_THRESHOLD	R/W	0h	AREF number of pending refreshes until the normal priority request is asserted. Reset Source: ctl_amod_g_rst_n

14.5.1.2.342 EMIF_CTLCFG_DENALI_CTL_291 Register

1 EMIF_CTLCFG_DENALI_CTL_291 Register (Offset = 48Ch) [reset = 0h]

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Table 14-13381. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 848Ch**

Figure 14-4421. EMIF_CTLCFG_DENALI_CTL_291 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ZQ_CALSTART_NORM_THRESHOLD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ZQ_CALSTART_NORM_THRESHOLD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">ZQCS_OPT_THRESHOLD</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">AREF_CMD_MAX_PER_TREFI</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13383. EMIF_CTLCFG_DENALI_CTL_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALSTART_NORM_THRESHOLD_F0	R/W	0h	ZQ START number of long counts until the normal priority request is asserted. This value should be scaled based on the number of ranks [chip selects] the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be. FC=0 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	ZQCS_OPT_THRESHOLD	R/W	0h	Number of clocks before ZQCS expires when the ZQ task will deassert its request for optimal command to command turn-around timing. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	AREF_CMD_MAX_PER_TREFI	R/W	0h	Sets the maximum number of auto-refreshes that will be executed in a TREFI period - both normal and high priority. This does not prevent refreshes generated by sub-task requests such as a self-refresh exit and enter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.343 EMIF_CTLCFG_DENALI_CTL_292 Register

1 EMIF_CTLCFG_DENALI_CTL_292 Register (Offset = 490h) [reset = 0h]

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Table 14-13384. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8490h**

Figure 14-4422. EMIF_CTLCFG_DENALI_CTL_292 Name Register

31	30	29	28	27	26	25	24
ZQ_CALLATCH_HIGH_THRESHOLD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALLATCH_HIGH_THRESHOLD_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_HIGH_THRESHOLD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_HIGH_THRESHOLD_F0							
R/W							
0h							

Table 14-13386. EMIF_CTLCFG_DENALI_CTL_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALLATCH_HIGH_THRESHOLD_F0	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_HIGH_THRESHOLD_F0	R/W	0h	ZQ START number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.344 EMIF_CTLCFG_DENALI_CTL_293 Register

1 EMIF_CTLCFG_DENALI_CTL_293 Register (Offset = 494h) [reset = 0h]

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Table 14-13387. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8494h**

Figure 14-4423. EMIF_CTLCFG_DENALI_CTL_293 Name Register

31	30	29	28	27	26	25	24
ZQ_CS_HIGH_THRESHOLD_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQ_CS_HIGH_THRESHOLD_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ZQ_CS_NORM_THRESHOLD_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQ_CS_NORM_THRESHOLD_F0							
R/W							
0h							

Table 14-13389. EMIF_CTLCFG_DENALI_CTL_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CS_HIGH_THRESHOLD_F0	R/W	0h	ZQ CS number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_NORM_THRESHOLD_F0	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.345 EMIF_CTLCFG_DENALI_CTL_294 Register

1 EMIF_CTLCFG_DENALI_CTL_294 Register (Offset = 498h) [reset = 0h]

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Table 14-13390. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8498h**

Figure 14-4424. EMIF_CTLCFG_DENALI_CTL_294 Name Register

31	30	29	28	27	26	25	24
ZQ_CALLATCH_TIMEOUT_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALLATCH_TIMEOUT_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_TIMEOUT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_TIMEOUT_F0							
R/W							
0h							

Table 14-13392. EMIF_CTLCFG_DENALI_CTL_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALLATCH_TIMEOUT_F0	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_TIMEOUT_F0	R/W	0h	ZQ START number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.346 EMIF_CTLCFG_DENALI_CTL_295 Register

1 EMIF_CTLCFG_DENALI_CTL_295 Register (Offset = 49Ch) [reset = 0h]

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Table 14-13393. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 849Ch**

Figure 14-4425. EMIF_CTLCFG_DENALI_CTL_295 Name Register

31	30	29	28	27	26	25	24
ZQ_PROMOTE_THRESHOLD_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQ_PROMOTE_THRESHOLD_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ZQ_CS_TIMEOUT_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQ_CS_TIMEOUT_F0							
R/W							
0h							

Table 14-13395. EMIF_CTLCFG_DENALI_CTL_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_PROMOTE_THRESHOLD_F0	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted. FC=0 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_TIMEOUT_F0	R/W	0h	ZQ CS number of long counts until the timeout is asserted. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.347 EMIF_CTLCFG_DENALI_CTL_296 Register

1 EMIF_CTLCFG_DENALI_CTL_296 Register (Offset = 4A0h) [reset = 0h]

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Table 14-13396. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 84A0h

Figure 14-4426. EMIF_CTLCFG_DENALI_CTL_296 Name Register

31	30	29	28	27	26	25	24
ZQ_CALSTART_HIGH_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALSTART_HIGH_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_NORM_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_NORM_THRESHOLD_F1							
R/W							
0h							

Table 14-13398. EMIF_CTLCFG_DENALI_CTL_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALSTART_HIGH_THRESHOLD_F1	R/W	0h	ZQ START number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_NORM_THRESHOLD_F1	R/W	0h	ZQ START number of long counts until the normal priority request is asserted. This value should be scaled based on the number of ranks [chip selects] the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.348 EMIF_CTLCFG_DENALI_CTL_297 Register

1 EMIF_CTLCFG_DENALI_CTL_297 Register (Offset = 4A4h) [reset = 0h]

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Table 14-13399. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 84A4h

Figure 14-4427. EMIF_CTLCFG_DENALI_CTL_297 Name Register

31	30	29	28	27	26	25	24
ZQ_CS_NORM_THRESHOLD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CS_NORM_THRESHOLD_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALLATCH_HIGH_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALLATCH_HIGH_THRESHOLD_F1							
R/W							
0h							

Table 14-13401. EMIF_CTLCFG_DENALI_CTL_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CS_NORM_THRESHOLD_F1	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALLATCH_HIGH_THRESHOLD_F1	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.349 EMIF_CTLCFG_DENALI_CTL_298 Register

1 EMIF_CTLCFG_DENALI_CTL_298 Register (Offset = 4A8h) [reset = 0h]

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Table 14-13402. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 84A8h

Figure 14-4428. EMIF_CTLCFG_DENALI_CTL_298 Name Register

31	30	29	28	27	26	25	24
ZQ_CALSTART_TIMEOUT_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALSTART_TIMEOUT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CS_HIGH_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CS_HIGH_THRESHOLD_F1							
R/W							
0h							

Table 14-13404. EMIF_CTLCFG_DENALI_CTL_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALSTART_TIMEOUT_F1	R/W	0h	ZQ START number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_HIGH_THRESHOLD_F1	R/W	0h	ZQ CS number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.350 EMIF_CTLCFG_DENALI_CTL_299 Register

1 EMIF_CTLCFG_DENALI_CTL_299 Register (Offset = 4ACh) [reset = 0h]

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Table 14-13405. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84ACh**

Figure 14-4429. EMIF_CTLCFG_DENALI_CTL_299 Name Register

31	30	29	28	27	26	25	24
ZQ_CS_TIMEOUT_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CS_TIMEOUT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALLATCH_TIMEOUT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALLATCH_TIMEOUT_F1							
R/W							
0h							

Table 14-13407. EMIF_CTLCFG_DENALI_CTL_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CS_TIMEOUT_F1	R/W	0h	ZQ CS number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALLATCH_TIMEOUT_F1	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.351 EMIF_CTLCFG_DENALI_CTL_300 Register

1 EMIF_CTLCFG_DENALI_CTL_300 Register (Offset = 4B0h) [reset = 0h]

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Table 14-13408. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84B0h**

Figure 14-4430. EMIF_CTLCFG_DENALI_CTL_300 Name Register

31	30	29	28	27	26	25	24
ZQ_CALSTART_NORM_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALSTART_NORM_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_PROMOTE_THRESHOLD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_PROMOTE_THRESHOLD_F1							
R/W							
0h							

Table 14-13410. EMIF_CTLCFG_DENALI_CTL_300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALSTART_NORM_THRESHOLD_F2	R/W	0h	ZQ START number of long counts until the normal priority request is asserted. This value should be scaled based on the number of ranks [chip selects] the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_PROMOTE_THRESHOLD_F1	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.352 EMIF_CTLCFG_DENALI_CTL_301 Register

1 EMIF_CTLCFG_DENALI_CTL_301 Register (Offset = 4B4h) [reset = 0h]

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Table 14-13411. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84B4h**

Figure 14-4431. EMIF_CTLCFG_DENALI_CTL_301 Name Register

31	30	29	28	27	26	25	24
ZQ_CALLATCH_HIGH_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALLATCH_HIGH_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_HIGH_THRESHOLD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_HIGH_THRESHOLD_F2							
R/W							
0h							

Table 14-13413. EMIF_CTLCFG_DENALI_CTL_301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALLATCH_HIGH_THRESHOLD_F2	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_HIGH_THRESHOLD_F2	R/W	0h	ZQ START number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.353 EMIF_CTLCFG_DENALI_CTL_302 Register

1 EMIF_CTLCFG_DENALI_CTL_302 Register (Offset = 4B8h) [reset = 0h]

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Table 14-13414. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 84B8h**

Figure 14-4432. EMIF_CTLCFG_DENALI_CTL_302 Name Register

31	30	29	28	27	26	25	24
ZQ_CS_HIGH_THRESHOLD_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQ_CS_HIGH_THRESHOLD_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ZQ_CS_NORM_THRESHOLD_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQ_CS_NORM_THRESHOLD_F2							
R/W							
0h							

Table 14-13416. EMIF_CTLCFG_DENALI_CTL_302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CS_HIGH_THRESHOLD_F2	R/W	0h	ZQ CS number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_NORM_THRESHOLD_F2	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.354 EMIF_CTLCFG_DENALI_CTL_303 Register

1 EMIF_CTLCFG_DENALI_CTL_303 Register (Offset = 4BCh) [reset = 0h]

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Table 14-13417. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84BCh**

Figure 14-4433. EMIF_CTLCFG_DENALI_CTL_303 Name Register

31	30	29	28	27	26	25	24
ZQ_CALLATCH_TIMEOUT_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_CALLATCH_TIMEOUT_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CALSTART_TIMEOUT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CALSTART_TIMEOUT_F2							
R/W							
0h							

Table 14-13419. EMIF_CTLCFG_DENALI_CTL_303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_CALLATCH_TIMEOUT_F2	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CALSTART_TIMEOUT_F2	R/W	0h	ZQ START number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.355 EMIF_CTLCFG_DENALI_CTL_304 Register

1 EMIF_CTLCFG_DENALI_CTL_304 Register (Offset = 4C0h) [reset = 0h]

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Table 14-13420. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84C0h**

Figure 14-4434. EMIF_CTLCFG_DENALI_CTL_304 Name Register

31	30	29	28	27	26	25	24
ZQ_PROMOTE_THRESHOLD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
ZQ_PROMOTE_THRESHOLD_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
ZQ_CS_TIMEOUT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
ZQ_CS_TIMEOUT_F2							
R/W							
0h							

Table 14-13422. EMIF_CTLCFG_DENALI_CTL_304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ZQ_PROMOTE_THRESHOLD_F2	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted. FC=2 Reset Source: ctl_amod_g_rst_n
15:0	ZQ_CS_TIMEOUT_F2	R/W	0h	ZQ CS number of long counts until the timeout is asserted. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.356 EMIF_CTLCFG_DENALI_CTL_305 Register

1 EMIF_CTLCFG_DENALI_CTL_305 Register (Offset = 4C4h) [reset = 0h]

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Table 14-13423. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84C4h**

Figure 14-4435. EMIF_CTLCFG_DENALI_CTL_305 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				ZQINIT_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ZQINIT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_TIMER_LOG							
R							
0h							

Table 14-13425. EMIF_CTLCFG_DENALI_CTL_305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	ZQINIT_F0	R/W	0h	Number of cycles needed for a ZQINIT command. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TIMEOUT_TIMER_LOG	R	0h	Reflects which timers experienced a timeout error [or had an uncleared error] when the timeout interrupt fired. Bit [0] correlates to a ZQ cal init, cs, cl, or reset FM timeout. Bit [1] correlates to the ZQ calstart FM timeout. Bit [2] correlates to the ZQ callatch FM timeout. Bit [3] correlates to the MRR temperature check FM timeout. Bit [4] correlates to the DQS oscillator FM timeout. Bit [5] correlates to the DFI update FM timeout. Bit [6] correlates to the low power interface wakeup timeout. Bit [7] correlates to the auto refresh max deficit timeout. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.357 EMIF_CTLCFG_DENALI_CTL_306 Register

1 EMIF_CTLCFG_DENALI_CTL_306 Register (Offset = 4C8h) [reset = 0h]

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Table 14-13426. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 84C8h

Figure 14-4436. EMIF_CTLCFG_DENALI_CTL_306 Name Register

31	30	29	28	27	26	25	24
RESERVED				ZQCS_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ZQCS_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				ZQCL_F0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ZQCL_F0							
R/W							
0h							

Table 14-13428. EMIF_CTLCFG_DENALI_CTL_306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQCS_F0	R/W	0h	Number of cycles needed for a ZQCS command. FC=0 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQCL_F0	R/W	0h	Number of cycles needed for a ZQCL command. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.358 EMIF_CTLCFG_DENALI_CTL_307 Register

1 EMIF_CTLCFG_DENALI_CTL_307 Register (Offset = 4CCh) [reset = 0h]

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Table 14-13429. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 84CCh

Figure 14-4437. EMIF_CTLCFG_DENALI_CTL_307 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	TZQLAT_F0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED				TZQCAL_F0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
TZQCAL_F0							
R/W							
0h							

Table 14-13431. EMIF_CTLCFG_DENALI_CTL_307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	TZQLAT_F0	R/W	0h	Holds the DRAM ZQLAT value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	TZQCAL_F0	R/W	0h	Holds the DRAM ZQCAL value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.359 EMIF_CTLCFG_DENALI_CTL_308 Register

1 EMIF_CTLCFG_DENALI_CTL_308 Register (Offset = 4D0h) [reset = 0h]

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Table 14-13432. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84D0h**

Figure 14-4438. EMIF_CTLCFG_DENALI_CTL_308 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ZQCL_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ZQCL_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ZQINIT_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ZQINIT_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13434. EMIF_CTLCFG_DENALI_CTL_308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQCL_F1	R/W	0h	Number of cycles needed for a ZQCL command. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQINIT_F1	R/W	0h	Number of cycles needed for a ZQINIT command. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.360 EMIF_CTLCFG_DENALI_CTL_309 Register

1 EMIF_CTLCFG_DENALI_CTL_309 Register (Offset = 4D4h) [reset = 0h]

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Table 14-13435. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84D4h**

Figure 14-4439. EMIF_CTLCFG_DENALI_CTL_309 Name Register

31	30	29	28	27	26	25	24
RESERVED				TZQCAL_F1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
TZQCAL_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				ZQCS_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ZQCS_F1							
R/W							
0h							

Table 14-13437. EMIF_CTLCFG_DENALI_CTL_309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	TZQCAL_F1	R/W	0h	Holds the DRAM ZQCAL value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQCS_F1	R/W	0h	Number of cycles needed for a ZQCS command. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.361 EMIF_CTLCFG_DENALI_CTL_310 Register

1 EMIF_CTLCFG_DENALI_CTL_310 Register (Offset = 4D8h) [reset = 0h]

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Table 14-13438. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84D8h**

Figure 14-4440. EMIF_CTLCFG_DENALI_CTL_310 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				ZQINIT_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
ZQINIT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED	TZQLAT_F1						
NONE	R/W						
0h	0h						

Table 14-13440. EMIF_CTLCFG_DENALI_CTL_310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	ZQINIT_F2	R/W	0h	Number of cycles needed for a ZQINIT command. FC=2 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	TZQLAT_F1	R/W	0h	Holds the DRAM ZQLAT value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.362 EMIF_CTLCFG_DENALI_CTL_311 Register

1 EMIF_CTLCFG_DENALI_CTL_311 Register (Offset = 4DCh) [reset = 0h]

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Table 14-13441. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84DCh**

Figure 14-4441. EMIF_CTLCFG_DENALI_CTL_311 Name Register

31	30	29	28	27	26	25	24
RESERVED				ZQCS_F2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQCS_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				ZQCL_F2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ZQCL_F2							
R/W							
0h							

Table 14-13443. EMIF_CTLCFG_DENALI_CTL_311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQCS_F2	R/W	0h	Number of cycles needed for a ZQCS command. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQCL_F2	R/W	0h	Number of cycles needed for a ZQCL command. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.363 EMIF_CTLCFG_DENALI_CTL_312 Register

1 EMIF_CTLCFG_DENALI_CTL_312 Register (Offset = 4E0h) [reset = 0h]

Return to Summary Table

Table 14-13444. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 84E0h

Figure 14-4442. EMIF_CTLCFG_DENALI_CTL_312 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">ZQ_SW_REQ_START_LATCH_MAP</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">TZQLAT_F2</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TZQCAL_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TZQCAL_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13446. EMIF_CTLCFG_DENALI_CTL_312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	ZQ_SW_REQ_START_LATCH_MAP	R/W	0h	Specifies which chip selects will simultaneously receive a ZQ start or latch command once the ZQ_REQ parameter is written with a ZQ Start or ZQ Latch command. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	TZQLAT_F2	R/W	0h	Holds the DRAM ZQLAT value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	TZQCAL_F2	R/W	0h	Holds the DRAM ZQCAL value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.364 EMIF_CTLCFG_DENALI_CTL_313 Register

1 EMIF_CTLCFG_DENALI_CTL_313 Register (Offset = 4E4h) [reset = 0h]

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Table 14-13447. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84E4h**

Figure 14-4443. EMIF_CTLCFG_DENALI_CTL_313 Name Register

31	30	29	28	27	26	25	24
RESERVED				ZQRESET_F0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZQRESET_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ZQ_REQ_PENDING
NONE							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ZQ_REQ			
NONE				W			
0h				0h			

Table 14-13449. EMIF_CTLCFG_DENALI_CTL_313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQRESET_F0	R/W	0h	Number of cycles needed for a ZQRESET command. FC=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	ZQ_REQ_PENDING	R	0h	Indicates that a ZQ command is currently in progress or waiting to run. Value of 1 indicates command in progress or waiting to run. When this is asserted, no writes to ZQ_REQ should occur. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	ZQ_REQ	W	0h	User request to initiate a ZQ calibration. Program to 3 for ZQ Start, program to 4 for ZQ Initialization [ZQINIT], program to 5 for ZQ Latch, or program to 8 for ZQ Reset. Clearing to 0 will not trigger any ZQ command. This parameter should only be written when the ZQ_REQ_PENDING parameter is cleared to 0. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.365 EMIF_CTLCFG_DENALI_CTL_314 Register

1 EMIF_CTLCFG_DENALI_CTL_314 Register (Offset = 4E8h) [reset = 0h]

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Table 14-13450. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84E8h**

Figure 14-4444. EMIF_CTLCFG_DENALI_CTL_314 Name Register

31	30	29	28	27	26	25	24
RESERVED				ZQRESET_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
ZQRESET_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				ZQRESET_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
ZQRESET_F1							
R/W							
0h							

Table 14-13452. EMIF_CTLCFG_DENALI_CTL_314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ZQRESET_F2	R/W	0h	Number of cycles needed for a ZQRESET command. FC=2 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ZQRESET_F1	R/W	0h	Number of cycles needed for a ZQRESET command. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.366 EMIF_CTLCFG_DENALI_CTL_315 Register

1 EMIF_CTLCFG_DENALI_CTL_315 Register (Offset = 4ECh) [reset = 0h]

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Table 14-13453. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 84ECh

Figure 14-4445. EMIF_CTLCFG_DENALI_CTL_315 Name Register

31	30	29	28	27	26	25	24
RESERVED						ZQ_CAL_LATCH_MAP_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						ZQ_CAL_START_MAP_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ZQCS_ROTATE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							NO_ZQ_INIT
NONE							R/W
0h							0h

Table 14-13455. EMIF_CTLCFG_DENALI_CTL_315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	ZQ_CAL_LATCH_MAP_0	R/W	0h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 0 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. CS=0 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	ZQ_CAL_START_MAP_0	R/W	0h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 0 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. CS=0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	ZQCS_ROTATE	R/W	0h	For memories that perform ZQ short commands [ZQCS], selects whether a ZQCS command will calibrate just one chip select or all chip selects. When rotation is off, all chip selects will be calibrated, requiring a longer time frame, but ZQ calibration will need to be performed less frequently. Set to 1 for rotating CS. For ZQ start/latch memories, this parameter is ignored. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-13455. EMIF_CTLCFG_DENALI_CTL_315 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NO_ZQ_INIT	R/W	0h	Disable ZQ operations during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.367 EMIF_CTLCFG_DENALI_CTL_316 Register

1 EMIF_CTLCFG_DENALI_CTL_316 Register (Offset = 4F0h) [reset = 0h]

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Table 14-13456. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84F0h**

Figure 14-4446. EMIF_CTLCFG_DENALI_CTL_316 Name Register

31	30	29	28	27	26	25	24
RESERVED						BANK_DIFF_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						BANK_DIFF_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						ZQ_CAL_LATCH_MAP_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						ZQ_CAL_START_MAP_1	
NONE						R/W	
0h						0h	

Table 14-13458. EMIF_CTLCFG_DENALI_CTL_316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	BANK_DIFF_1	R/W	0h	Encoded number of banks on the DRAM[s]. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	BANK_DIFF_0	R/W	0h	Encoded number of banks on the DRAM[s]. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	ZQ_CAL_LATCH_MAP_1	R/W	0h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 1 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. CS=1 Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	ZQ_CAL_START_MAP_1	R/W	0h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 1 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. CS=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.368 EMIF_CTLCFG_DENALI_CTL_317 Register

1 EMIF_CTLCFG_DENALI_CTL_317 Register (Offset = 4F4h) [reset = 0h]

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Table 14-13459. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84F4h**

Figure 14-4447. EMIF_CTLCFG_DENALI_CTL_317 Name Register

31	30	29	28	27	26	25	24
RESERVED				COL_DIFF_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				COL_DIFF_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					ROW_DIFF_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ROW_DIFF_0		
NONE					R/W		
0h					0h		

Table 14-13461. EMIF_CTLCFG_DENALI_CTL_317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	COL_DIFF_1	R/W	0h	Difference between number of column pins available and number being used. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	COL_DIFF_0	R/W	0h	Difference between number of column pins available and number being used. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	ROW_DIFF_1	R/W	0h	Difference between number of address pins available and number being used. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	ROW_DIFF_0	R/W	0h	Difference between number of address pins available and number being used. Reset Source: ctl_amod_g_rst_n

14.5.1.2.369 EMIF_CTLCFG_DENALI_CTL_318 Register

1 EMIF_CTLCFG_DENALI_CTL_318 Register (Offset = 4F8h) [reset = 0h]

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Table 14-13462. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84F8h**

Figure 14-4448. EMIF_CTLCFG_DENALI_CTL_318 Name Register

31	30	29	28	27	26	25	24
CS_VAL_UPPER_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CS_VAL_UPPER_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CS_VAL_LOWER_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CS_VAL_LOWER_0							
R/W							
0h							

Table 14-13464. EMIF_CTLCFG_DENALI_CTL_318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CS_VAL_UPPER_0	R/W	0h	Upper bound address for chip select 0. Reset Source: ctl_amod_g_rst_n
15:0	CS_VAL_LOWER_0	R/W	0h	Lower bound address for chip select 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.370 EMIF_CTLCFG_DENALI_CTL_319 Register

1 EMIF_CTLCFG_DENALI_CTL_319 Register (Offset = 4FCh) [reset = 0h]

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Table 14-13465. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 84FCh**

Figure 14-4449. EMIF_CTLCFG_DENALI_CTL_319 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CS_MSK_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CS_MSK_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						ROW_START_VAL_0	
NONE						R/W	
0h						0h	

Table 14-13467. EMIF_CTLCFG_DENALI_CTL_319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	CS_MSK_0	R/W	0h	Mask applied to the address decode for chip select 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	ROW_START_VAL_0	R/W	0h	Row start value for chip select 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.371 EMIF_CTLCFG_DENALI_CTL_320 Register

1 EMIF_CTLCFG_DENALI_CTL_320 Register (Offset = 500h) [reset = 0h]

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Table 14-13468. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8500h

Figure 14-4450. EMIF_CTLCFG_DENALI_CTL_320 Name Register

31	30	29	28	27	26	25	24
CS_VAL_UPPER_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CS_VAL_UPPER_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CS_VAL_LOWER_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CS_VAL_LOWER_1							
R/W							
0h							

Table 14-13470. EMIF_CTLCFG_DENALI_CTL_320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CS_VAL_UPPER_1	R/W	0h	Upper bound address for chip select 1. Reset Source: ctl_amod_g_rst_n
15:0	CS_VAL_LOWER_1	R/W	0h	Lower bound address for chip select 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.372 EMIF_CTLCFG_DENALI_CTL_321 Register

1 EMIF_CTLCFG_DENALI_CTL_321 Register (Offset = 504h) [reset = 0h]

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Table 14-13471. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8504h**

Figure 14-4451. EMIF_CTLCFG_DENALI_CTL_321 Name Register

31	30	29	28	27	26	25	24
RESERVED						CS_MAP_NON_POW2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
CS_MSK_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CS_MSK_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						ROW_START_VAL_1	
NONE						R/W	
0h						0h	

Table 14-13473. EMIF_CTLCFG_DENALI_CTL_321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CS_MAP_NON_POW2	R/W	0h	Defines which chip selects are non-power-of-2 memory sizes. Reset Source: ctl_amod_g_rst_n
23:8	CS_MSK_1	R/W	0h	Mask applied to the address decode for chip select 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	ROW_START_VAL_1	R/W	0h	Row start value for chip select 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.373 EMIF_CTLCFG_DENALI_CTL_322 Register

1 EMIF_CTLCFG_DENALI_CTL_322 Register (Offset = 508h) [reset = A000000h]

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Table 14-13474. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8508h**

Figure 14-4452. EMIF_CTLCFG_DENALI_CTL_322 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">APREBIT</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MC_RESERVED9</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">MC_RESERVED8</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>CS_LOWER_ADDR_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13476. EMIF_CTLCFG_DENALI_CTL_322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	APREBIT	R/W	Ah	Location of the auto pre-charge bit in the DRAM address. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MC_RESERVED9	R/W	0h	Reserved
15:13	RESERVED	NONE	0h	Reserved
12:8	MC_RESERVED8	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	CS_LOWER_ADDR_EN	R/W	0h	Enables moving the CS field to lower in the address map. When set to 1, the memory address map will be changed to ROW__CS__BANK. Please refer to the limitations before setting this bit. Reset Source: ctl_amod_g_rst_n

14.5.1.2.374 EMIF_CTLCFG_DENALI_CTL_323 Register

1 EMIF_CTLCFG_DENALI_CTL_323 Register (Offset = 50Ch) [reset = 0h]

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Table 14-13477. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 850Ch**

Figure 14-4453. EMIF_CTLCFG_DENALI_CTL_323 Name Register

31	30	29	28	27	26	25	24
RESERVED							ADDR_COLLISION_MPM_DIS
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							ADDR_CMP_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
COMMAND_AGE_COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
AGE_COUNT							
R/W							
0h							

Table 14-13479. EMIF_CTLCFG_DENALI_CTL_323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	ADDR_COLLISION_MPM_DIS	R/W	0h	Disable address collision detection extension using micro page mask for command queue placement and selection. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	ADDR_CMP_EN	R/W	0h	Enable address collision detection as a rule for command queue placement. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:8	COMMAND_AGE_COUNT	R/W	0h	Initial value of individual command aging counters for command aging. Reset Source: ctl_amod_g_rst_n
7:0	AGE_COUNT	R/W	0h	Initial value of controller aging-rate counter for command aging. Reset Source: ctl_amod_g_rst_n

14.5.1.2.375 EMIF_CTLCFG_DENALI_CTL_324 Register

1 EMIF_CTLCFG_DENALI_CTL_324 Register (Offset = 510h) [reset = 0h]

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Table 14-13480. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8510h**

Figure 14-4454. EMIF_CTLCFG_DENALI_CTL_324 Name Register

31	30	29	28	27	26	25	24
RESERVED							RW_SAME_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PRIORITY_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PLACEMENT_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							BANK_SPLIT_EN
NONE							R/W
0h							0h

Table 14-13482. EMIF_CTLCFG_DENALI_CTL_324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RW_SAME_EN	R/W	0h	Enable read/write grouping as a rule for command queue placement. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PRIORITY_EN	R/W	0h	Enable priority as a rule for command queue placement. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PLACEMENT_EN	R/W	0h	Enable placement logic for command queue. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	BANK_SPLIT_EN	R/W	0h	Enable bank splitting as a rule for command queue placement. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.376 EMIF_CTLCFG_DENALI_CTL_325 Register

1 EMIF_CTLCFG_DENALI_CTL_325 Register (Offset = 514h) [reset = 0h]

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Table 14-13483. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8514h**

Figure 14-4455. EMIF_CTLCFG_DENALI_CTL_325 Name Register

31	30	29	28	27	26	25	24
RESERVED						DISABLE_RW_GROUP_W_BNK_CONFLICT	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							W2R_SPLIT_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CS_SAME_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RW_SAME_PAGE_EN
NONE							R/W
0h							0h

Table 14-13485. EMIF_CTLCFG_DENALI_CTL_325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	DISABLE_RW_GROUP_W_BNK_CONFLICT	R/W	0h	Disables placement to read/write group when grouping creates a bank collision. Bit [0] controls placement next to bank conflict command and bit [1] controls placement 2 away from bank conflict command. Set each bit to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	W2R_SPLIT_EN	R/W	0h	Enable splitting of commands to the same chip select from a write to a read command as a rule for command queue placement. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	CS_SAME_EN	R/W	0h	Enable chip select grouping when read/write grouping as a rule for command queue placement. This is only valid when the RW_SAME_EN parameter is set. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-13485. EMIF_CTLCFG_DENALI_CTL_325 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RW_SAME_PAGE_EN	R/W	0h	Enable page grouping when read/write grouping as a rule for command queue placement. This is only valid when the RW_SAME_EN parameter is set. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.377 EMIF_CTLCFG_DENALI_CTL_326 Register

1 EMIF_CTLCFG_DENALI_CTL_326 Register (Offset = 518h) [reset = 0h]

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Table 14-13486. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8518h**

Figure 14-4456. EMIF_CTLCFG_DENALI_CTL_326 Name Register

31	30	29	28	27	26	25	24
RESERVED						INHIBIT_DRAM_CMD	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED							DISABLE_RD_INTERLEAVE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							SWAP_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED			NUM_Q_ENTRIES_ACT_DISABLE				
NONE			R/W				
0h			0h				

Table 14-13488. EMIF_CTLCFG_DENALI_CTL_326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	INHIBIT_DRAM_CMD	R/W	0h	Inhibit command types from being executed from the command queue. Clear to 0 to enable any command, program to 1 to inhibit read/write and bank commands, program to 2 to inhibit MRR and peripheral MRR commands, or program to 3 to inhibit MRR and read/write commands. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	DISABLE_RD_INTERLEAVE	R/W	0h	Disable read data interleaving for commands from the same port, regardless of the requestor ID. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SWAP_EN	R/W	0h	Enable command swapping logic in execution unit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	NUM_Q_ENTRIES_ACT_DISABLE	R/W	0h	Number of queue entries in which ACT requests will be disabled. Programming to X will disable ACT requests from the X entries lowest in the command queue. Reset Source: ctl_amod_g_rst_n

14.5.1.2.378 EMIF_CTLCFG_DENALI_CTL_327 Register

1 EMIF_CTLCFG_DENALI_CTL_327 Register (Offset = 51Ch) [reset = 0h]

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Table 14-13489. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 851Ch

Figure 14-4457. EMIF_CTLCFG_DENALI_CTL_327 Name Register

31	30	29	28	27	26	25	24
RESERVED					MEMDATA_RATIO_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED							MEM_DP_REDUCTION
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				BURST_ON_FLY_BIT			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED						CS_MAP	
NONE						R/W	
0h						0h	

Table 14-13491. EMIF_CTLCFG_DENALI_CTL_327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	MEMDATA_RATIO_0	R/W	0h	Defines the ratio of the DRAM device size on chip select 0 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. CS=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MEM_DP_REDUCTION	R/W	0h	Enable the half datapath feature of the controller. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	BURST_ON_FLY_BIT	R/W	0h	Identifies the burst-on-fly bit in the memory mode registers. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	CS_MAP	R/W	0h	Defines which chip selects are active. Reset Source: ctl_amod_g_rst_n

14.5.1.2.379 EMIF_CTLCFG_DENALI_CTL_328 Register

1 EMIF_CTLCFG_DENALI_CTL_328 Register (Offset = 520h) [reset = 0h]

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Table 14-13492. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8520h**

Figure 14-4458. EMIF_CTLCFG_DENALI_CTL_328 Name Register

31	30	29	28	27	26	25	24
RESERVED						DEVICE0_BYTE0_CS1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						DEVICE1_BYTE0_CS0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						DEVICE0_BYTE0_CS0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED					MEMDATA_RATIO_1		
NONE					R/W		
0h					0h		

Table 14-13494. EMIF_CTLCFG_DENALI_CTL_328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	DEVICE0_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 0 on chip 1. Used for MRRs to identify where data will be returned. DEV=0 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	DEVICE1_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 1 on chip 0. Used for MRRs to identify where data will be returned. DEV=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	DEVICE0_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 0 on chip 0. Used for MRRs to identify where data will be returned. DEV=0 Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MEMDATA_RATIO_1	R/W	0h	Defines the ratio of the DRAM device size on chip select 1 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. CS=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.380 EMIF_CTLCFG_DENALI_CTL_329 Register

1 EMIF_CTLCFG_DENALI_CTL_329 Register (Offset = 524h) [reset = 0h]

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Table 14-13495. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8524h

Figure 14-4459. EMIF_CTLCFG_DENALI_CTL_329 Name Register

31	30	29	28	27	26	25	24
RESERVED						WR_ORDER_REQ	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED							IN_ORDER_ACCEPT
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			Q_FULLNESS				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED						DEVICE1_BYTE0_CS1	
NONE						R/W	
0h						0h	

Table 14-13497. EMIF_CTLCFG_DENALI_CTL_329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	WR_ORDER_REQ	R/W	0h	Determines if the controller can re-order write commands from the same source ID and/or the same port. Bit [0] controls source ID usage and bit [1] controls port ID usage. Set each bit to 1 to enable usage in placement logic. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	IN_ORDER_ACCEPT	R/W	0h	Forces the controller to accept commands in the order in which they are placed in the command queue. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	Q_FULLNESS	R/W	0h	Quantity that determines when the command queue almost full signal will assert [q_almost_full]. When cleared to 0, the q_almost_full signal will be driven to 0 irrespective of number of entries in the command queue. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-13497. EMIF_CTLCFG_DENALI_CTL_329 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	DEVICE1_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 1 on chip 1. Used for MRRs to identify where data will be returned. DEV=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.381 EMIF_CTLCFG_DENALI_CTL_330 Register

1 EMIF_CTLCFG_DENALI_CTL_330 Register (Offset = 528h) [reset = 0h]

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Table 14-13498. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8528h**

Figure 14-4460. EMIF_CTLCFG_DENALI_CTL_330 Name Register

31	30	29	28	27	26	25	24
RESERVED							CTRLUPD_AREF_HP_ENABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CTRLUPD_REQ_PER_AREF_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CTRLUPD_REQ
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CONTROLLER_BUSY
NONE							R
0h							0h

Table 14-13500. EMIF_CTLCFG_DENALI_CTL_330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CTRLUPD_AREF_HP_ENABLE	R/W	0h	Enable an automatic controller-initiated update [dfi_ctrlupd_req] after every high priority refresh when executing as a subtask request. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	CTRLUPD_REQ_PER_AREF_EN	R/W	0h	Enable an automatic controller-initiated update [dfi_ctrlupd_req] after every refresh. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	CTRLUPD_REQ	W	0h	Assert the DFI controller-initiated update request signal dfi_ctrlupd_req. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-13500. EMIF_CTLCFG_DENALI_CTL_330 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CONTROLLER_BUSY	R	0h	Indicator that the controller is processing a command. Evaluates all ports for outstanding transactions. Value of 1 indicates controller busy. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.382 EMIF_CTLCFG_DENALI_CTL_331 Register

1 EMIF_CTLCFG_DENALI_CTL_331 Register (Offset = 52Ch) [reset = 0h]

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Table 14-13501. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 852Ch

Figure 14-4461. EMIF_CTLCFG_DENALI_CTL_331 Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_PREAMBLE_TRAINING_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PREAMBLE_SUPPORT_F2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PREAMBLE_SUPPORT_F1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PREAMBLE_SUPPORT_F0	
NONE						R/W	
0h						0h	

Table 14-13503. EMIF_CTLCFG_DENALI_CTL_331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_PREAMBLE_TRAINING_EN	R/W	0h	Enable read preamble training during gate training. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PREAMBLE_SUPPORT_F2	R/W	0h	Selection the preamble for read and write burst transfers. FC=2 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PREAMBLE_SUPPORT_F1	R/W	0h	Selection the preamble for read and write burst transfers. FC=1 Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PREAMBLE_SUPPORT_F0	R/W	0h	Selection the preamble for read and write burst transfers. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.383 EMIF_CTLCFG_DENALI_CTL_332 Register

1 EMIF_CTLCFG_DENALI_CTL_332 Register (Offset = 530h) [reset = 0h]

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Table 14-13504. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8530h**

Figure 14-4462. EMIF_CTLCFG_DENALI_CTL_332 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					DFI_ERROR		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							RD_DBI_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							WR_DBI_EN
NONE							R/W
0h							0h

Table 14-13506. EMIF_CTLCFG_DENALI_CTL_332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	DFI_ERROR	R	0h	Indicates that the DFI error flag has been asserted. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	RD_DBI_EN	R/W	0h	Enables controller support of DRAM DBI feature for read data with DDR4 devices. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	WR_DBI_EN	R/W	0h	Enables controller support of DRAM DBI feature for write data with DDR4 devices. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.384 EMIF_CTLCFG_DENALI_CTL_333 Register

1 EMIF_CTLCFG_DENALI_CTL_333 Register (Offset = 534h) [reset = 0h]

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Table 14-13507. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8534h**

Figure 14-4463. EMIF_CTLCFG_DENALI_CTL_333 Name Register

31	30	29	28	27	26	25	24
RESERVED							MC_RESERVED10
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							BG_ROTATE_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				DFI_ERROR_INFO			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
DFI_ERROR_INFO							
R							
0h							

Table 14-13509. EMIF_CTLCFG_DENALI_CTL_333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MC_RESERVED10	W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	BG_ROTATE_EN	R/W	0h	Enable bank group rotation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	DFI_ERROR_INFO	R	0h	Holds the encoded DFI error type associated with the DFI_ERROR parameter assertion. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.385 EMIF_CTLCFG_DENALI_CTL_334 Register

1 EMIF_CTLCFG_DENALI_CTL_334 Register (Offset = 538h) [reset = 0h]

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Table 14-13510. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8538h**

Figure 14-4464. EMIF_CTLCFG_DENALI_CTL_334 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_MASTER							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_MASTER							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_MASTER							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_MASTER							
R							
0h							

Table 14-13512. EMIF_CTLCFG_DENALI_CTL_334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_STATUS_MASTER	R	0h	Controller status reporting register for interrupt status groups. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.386 EMIF_CTLCFG_DENALI_CTL_335 Register

1 EMIF_CTLCFG_DENALI_CTL_335 Register (Offset = 53Ch) [reset = 0h]

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Table 14-13513. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 853Ch**

Figure 14-4465. EMIF_CTLCFG_DENALI_CTL_335 Name Register

31	30	29	28	27	26	25	24
INT_MASK_MASTER							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_MASTER							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_MASTER							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_MASTER							
R/W							
0h							

Table 14-13515. EMIF_CTLCFG_DENALI_CTL_335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_MASK_MASTER	R/W	0h	Controller mask register for interrupt status groups. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.387 EMIF_CTLCFG_DENALI_CTL_336 Register

1 EMIF_CTLCFG_DENALI_CTL_336 Register (Offset = 540h) [reset = 0h]

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Table 14-13516. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8540h**

Figure 14-4466. EMIF_CTLCFG_DENALI_CTL_336 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_TIMEOUT							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_TIMEOUT							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_TIMEOUT							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_TIMEOUT							
R							
0h							

Table 14-13518. EMIF_CTLCFG_DENALI_CTL_336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_STATUS_TIMEOUT	R	0h	Status of interrupts in the controller related to Timeout monitors. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.388 EMIF_CTLCFG_DENALI_CTL_337 Register

1 EMIF_CTLCFG_DENALI_CTL_337 Register (Offset = 544h) [reset = 0h]

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Table 14-13519. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8544h**

Figure 14-4467. EMIF_CTLCFG_DENALI_CTL_337 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_LOWPOWER							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_LOWPOWER							
R							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED11							
R							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED11							
R							
0h							

Table 14-13521. EMIF_CTLCFG_DENALI_CTL_337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	INT_STATUS_LOWPOWER	R	0h	Status of interrupts in the controller related to Low Power. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	MC_RESERVED11	R	0h	Reserved

14.5.1.2.389 EMIF_CTLCFG_DENALI_CTL_338 Register

1 EMIF_CTLCFG_DENALI_CTL_338 Register (Offset = 548h) [reset = 0h]

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Table 14-13522. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8548h**

Figure 14-4468. EMIF_CTLCFG_DENALI_CTL_338 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED13							
R							
0h							
23	22	21	20	19	18	17	16
MC_RESERVED13							
R							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED12							
R							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED12							
R							
0h							

Table 14-13524. EMIF_CTLCFG_DENALI_CTL_338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MC_RESERVED13	R	0h	Reserved
15:0	MC_RESERVED12	R	0h	Reserved

14.5.1.2.390 EMIF_CTLCFG_DENALI_CTL_339 Register

1 EMIF_CTLCFG_DENALI_CTL_339 Register (Offset = 54Ch) [reset = 0h]

Return to Summary Table

Table 14-13525. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 854Ch**

Figure 14-4469. EMIF_CTLCFG_DENALI_CTL_339 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_TRAINING							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_TRAINING							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_TRAINING							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_TRAINING							
R							
0h							

Table 14-13527. EMIF_CTLCFG_DENALI_CTL_339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_STATUS_TRAINING	R	0h	Status of interrupts in the controller related to Training/Calibration. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.391 EMIF_CTLCFG_DENALI_CTL_340 Register

1 EMIF_CTLCFG_DENALI_CTL_340 Register (Offset = 550h) [reset = 0h]

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Table 14-13528. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8550h**

Figure 14-4470. EMIF_CTLCFG_DENALI_CTL_340 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_USERIF							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_USERIF							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_USERIF							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_USERIF							
R							
0h							

Table 14-13530. EMIF_CTLCFG_DENALI_CTL_340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_STATUS_USERIF	R	0h	Status of interrupts in the controller related to ASIC to Controller Interface. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.392 EMIF_CTLCFG_DENALI_CTL_341 Register

1 EMIF_CTLCFG_DENALI_CTL_341 Register (Offset = 554h) [reset = 0h]

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Table 14-13531. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8554h**

Figure 14-4471. EMIF_CTLCFG_DENALI_CTL_341 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED14							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_BIST							
R							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_MISC							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_MISC							
R							
0h							

Table 14-13533. EMIF_CTLCFG_DENALI_CTL_341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MC_RESERVED14	R	0h	Reserved
23:16	INT_STATUS_BIST	R	0h	Status of interrupts in the controller related to BIST. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	INT_STATUS_MISC	R	0h	Status of interrupts in the controller related to Miscellaneous features. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.393 EMIF_CTLCFG_DENALI_CTL_342 Register

1 EMIF_CTLCFG_DENALI_CTL_342 Register (Offset = 558h) [reset = 0h]

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Table 14-13534. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8558h**

Figure 14-4472. EMIF_CTLCFG_DENALI_CTL_342 Name Register

31	30	29	28	27	26	25	24
INT_STATUS_INIT							
R							
0h							
23	22	21	20	19	18	17	16
INT_STATUS_FREQ							
R							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED15							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_DFI							
R							
0h							

Table 14-13536. EMIF_CTLCFG_DENALI_CTL_342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	INT_STATUS_INIT	R	0h	Status of interrupts in the controller related to Initialization. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	INT_STATUS_FREQ	R	0h	Status of interrupts in the controller related to Frequency Scaling. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	MC_RESERVED15	R	0h	Reserved
7:0	INT_STATUS_DFI	R	0h	Status of interrupts in the controller related to DFI. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.394 EMIF_CTLCFG_DENALI_CTL_343 Register

1 EMIF_CTLCFG_DENALI_CTL_343 Register (Offset = 55Ch) [reset = 0h]

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Table 14-13537. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 855Ch

Figure 14-4473. EMIF_CTLCFG_DENALI_CTL_343 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INT_STATUS_PARITY							
R							
0h							
7	6	5	4	3	2	1	0
INT_STATUS_MODE							
R							
0h							

Table 14-13539. EMIF_CTLCFG_DENALI_CTL_343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	INT_STATUS_PARITY	R	0h	Status of interrupts in the controller related to Parity. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	INT_STATUS_MODE	R	0h	Status of interrupts in the controller related to Memory Mode Settings. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.395 EMIF_CTLCFG_DENALI_CTL_344 Register

1 EMIF_CTLCFG_DENALI_CTL_344 Register (Offset = 560h) [reset = 0h]

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Table 14-13540. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8560h**

Figure 14-4474. EMIF_CTLCFG_DENALI_CTL_344 Name Register

31	30	29	28	27	26	25	24
INT_ACK_TIMEOUT							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_TIMEOUT							
W							
0h							
15	14	13	12	11	10	9	8
INT_ACK_TIMEOUT							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_TIMEOUT							
W							
0h							

Table 14-13542. EMIF_CTLCFG_DENALI_CTL_344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_ACK_TIMEOUT	W	0h	Clear status of the INT_STATUS_TIMEOUT parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.396 EMIF_CTLCFG_DENALI_CTL_345 Register

1 EMIF_CTLCFG_DENALI_CTL_345 Register (Offset = 564h) [reset = 0h]

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Table 14-13543. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8564h**

Figure 14-4475. EMIF_CTLCFG_DENALI_CTL_345 Name Register

31	30	29	28	27	26	25	24
INT_ACK_LOWPOWER							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_LOWPOWER							
W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED16							
W							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED16							
W							
0h							

Table 14-13545. EMIF_CTLCFG_DENALI_CTL_345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	INT_ACK_LOWPOWER	W	0h	Clear status of the INT_STATUS_LOWPOWER parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:0	MC_RESERVED16	W	0h	Reserved

14.5.1.2.397 EMIF_CTLCFG_DENALI_CTL_346 Register

1 EMIF_CTLCFG_DENALI_CTL_346 Register (Offset = 568h) [reset = 0h]

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Table 14-13546. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8568h**

Figure 14-4476. EMIF_CTLCFG_DENALI_CTL_346 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED18							
W							
0h							
23	22	21	20	19	18	17	16
MC_RESERVED18							
W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED17							
W							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED17							
W							
0h							

Table 14-13548. EMIF_CTLCFG_DENALI_CTL_346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MC_RESERVED18	W	0h	Reserved
15:0	MC_RESERVED17	W	0h	Reserved

14.5.1.2.398 EMIF_CTLCFG_DENALI_CTL_347 Register

1 EMIF_CTLCFG_DENALI_CTL_347 Register (Offset = 56Ch) [reset = 0h]

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Table 14-13549. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 856Ch

Figure 14-4477. EMIF_CTLCFG_DENALI_CTL_347 Name Register

31	30	29	28	27	26	25	24
INT_ACK_TRAINING							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_TRAINING							
W							
0h							
15	14	13	12	11	10	9	8
INT_ACK_TRAINING							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_TRAINING							
W							
0h							

Table 14-13551. EMIF_CTLCFG_DENALI_CTL_347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_ACK_TRAINING	W	0h	Clear status of the INT_STATUS_TRAINING parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.399 EMIF_CTLCFG_DENALI_CTL_348 Register

1 EMIF_CTLCFG_DENALI_CTL_348 Register (Offset = 570h) [reset = 0h]

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Table 14-13552. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8570h

Figure 14-4478. EMIF_CTLCFG_DENALI_CTL_348 Name Register

31	30	29	28	27	26	25	24
INT_ACK_USERIF							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_USERIF							
W							
0h							
15	14	13	12	11	10	9	8
INT_ACK_USERIF							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_USERIF							
W							
0h							

Table 14-13554. EMIF_CTLCFG_DENALI_CTL_348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_ACK_USERIF	W	0h	Clear status of the INT_STATUS_USERIF parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.400 EMIF_CTLCFG_DENALI_CTL_349 Register

1 EMIF_CTLCFG_DENALI_CTL_349 Register (Offset = 574h) [reset = 0h]

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Table 14-13555. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8574h**

Figure 14-4479. EMIF_CTLCFG_DENALI_CTL_349 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED19							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_BIST							
W							
0h							
15	14	13	12	11	10	9	8
INT_ACK_MISC							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_MISC							
W							
0h							

Table 14-13557. EMIF_CTLCFG_DENALI_CTL_349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MC_RESERVED19	W	0h	Reserved
23:16	INT_ACK_BIST	W	0h	Clear status of the INT_STATUS_BIST parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:0	INT_ACK_MISC	W	0h	Clear status of the INT_STATUS_MISC parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.401 EMIF_CTLCFG_DENALI_CTL_350 Register

1 EMIF_CTLCFG_DENALI_CTL_350 Register (Offset = 578h) [reset = 0h]

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Table 14-13558. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8578h**

Figure 14-4480. EMIF_CTLCFG_DENALI_CTL_350 Name Register

31	30	29	28	27	26	25	24
INT_ACK_INIT							
W							
0h							
23	22	21	20	19	18	17	16
INT_ACK_FREQ							
W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED20							
W							
0h							
7	6	5	4	3	2	1	0
INT_ACK_DFI							
W							
0h							

Table 14-13560. EMIF_CTLCFG_DENALI_CTL_350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	INT_ACK_INIT	W	0h	Clear status of the INT_STATUS_INIT parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:16	INT_ACK_FREQ	W	0h	Clear status of the INT_STATUS_FREQ parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:8	MC_RESERVED20	W	0h	Reserved
7:0	INT_ACK_DFI	W	0h	Clear status of the INT_STATUS_DFI parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.402 EMIF_CTLCFG_DENALI_CTL_351 Register

1 EMIF_CTLCFG_DENALI_CTL_351 Register (Offset = 57Ch) [reset = 0h]

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Table 14-13561. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 857Ch**

Figure 14-4481. EMIF_CTLCFG_DENALI_CTL_351 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INT_ACK_PARITY							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT_ACK_MODE							
W							
0h							

Table 14-13563. EMIF_CTLCFG_DENALI_CTL_351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	INT_ACK_PARITY	W	0h	Clear status of the INT_STATUS_PARITY parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:0	INT_ACK_MODE	W	0h	Clear status of the INT_STATUS_MODE parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.403 EMIF_CTLCFG_DENALI_CTL_352 Register

1 EMIF_CTLCFG_DENALI_CTL_352 Register (Offset = 580h) [reset = 0h]

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Table 14-13564. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8580h**

Figure 14-4482. EMIF_CTLCFG_DENALI_CTL_352 Name Register

31	30	29	28	27	26	25	24
INT_MASK_TIMEOUT							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_TIMEOUT							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_TIMEOUT							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_TIMEOUT							
R/W							
0h							

Table 14-13566. EMIF_CTLCFG_DENALI_CTL_352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_MASK_TIMEOUT	R/W	0h	Mask for the controller_int signal from the INT_MASK_TIMEOUT parameter Reset Source: ctl_amod_g_rst_n

14.5.1.2.404 EMIF_CTLCFG_DENALI_CTL_353 Register

1 EMIF_CTLCFG_DENALI_CTL_353 Register (Offset = 584h) [reset = 0h]

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Table 14-13567. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8584h**

Figure 14-4483. EMIF_CTLCFG_DENALI_CTL_353 Name Register

31	30	29	28	27	26	25	24
INT_MASK_LOWPOWER							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_LOWPOWER							
R/W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED21							
R/W							
0h							
7	6	5	4	3	2	1	0
MC_RESERVED21							
R/W							
0h							

Table 14-13569. EMIF_CTLCFG_DENALI_CTL_353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	INT_MASK_LOWPOWER	R/W	0h	Mask for the controller_int signal from the INT_MASK_LOWPOWER parameter Reset Source: ctl_amod_g_rst_n
15:0	MC_RESERVED21	R/W	0h	Reserved

14.5.1.2.405 EMIF_CTLCFG_DENALI_CTL_354 Register

1 EMIF_CTLCFG_DENALI_CTL_354 Register (Offset = 588h) [reset = 0h]

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Table 14-13570. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8588h

Figure 14-4484. EMIF_CTLCFG_DENALI_CTL_354 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MC_RESERVED23</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MC_RESERVED23</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MC_RESERVED22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MC_RESERVED22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13572. EMIF_CTLCFG_DENALI_CTL_354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MC_RESERVED23	R/W	0h	Reserved
15:0	MC_RESERVED22	R/W	0h	Reserved

14.5.1.2.406 EMIF_CTLCFG_DENALI_CTL_355 Register

1 EMIF_CTLCFG_DENALI_CTL_355 Register (Offset = 58Ch) [reset = 0h]

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Table 14-13573. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 858Ch**

Figure 14-4485. EMIF_CTLCFG_DENALI_CTL_355 Name Register

31	30	29	28	27	26	25	24
INT_MASK_TRAINING							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_TRAINING							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_TRAINING							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_TRAINING							
R/W							
0h							

Table 14-13575. EMIF_CTLCFG_DENALI_CTL_355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_MASK_TRAINING	R/W	0h	Mask for the controller_int signal from the INT_MASK_TRAINING parameter Reset Source: ctl_amod_g_rst_n

14.5.1.2.407 EMIF_CTLCFG_DENALI_CTL_356 Register

1 EMIF_CTLCFG_DENALI_CTL_356 Register (Offset = 590h) [reset = 0h]

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Table 14-13576. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8590h**

Figure 14-4486. EMIF_CTLCFG_DENALI_CTL_356 Name Register

31	30	29	28	27	26	25	24
INT_MASK_USERIF							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_USERIF							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_USERIF							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_USERIF							
R/W							
0h							

Table 14-13578. EMIF_CTLCFG_DENALI_CTL_356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INT_MASK_USERIF	R/W	0h	Mask for the controller_int signal from the INT_MASK_USERIF parameter Reset Source: ctl_amod_g_rst_n

14.5.1.2.408 EMIF_CTLCFG_DENALI_CTL_357 Register

1 EMIF_CTLCFG_DENALI_CTL_357 Register (Offset = 594h) [reset = 0h]

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Table 14-13579. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8594h**

Figure 14-4487. EMIF_CTLCFG_DENALI_CTL_357 Name Register

31	30	29	28	27	26	25	24
MC_RESERVED24							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_BIST							
R/W							
0h							
15	14	13	12	11	10	9	8
INT_MASK_MISC							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_MISC							
R/W							
0h							

Table 14-13581. EMIF_CTLCFG_DENALI_CTL_357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MC_RESERVED24	R/W	0h	Reserved
23:16	INT_MASK_BIST	R/W	0h	Mask for the controller_int signal from the INT_MASK_BIST parameter Reset Source: ctl_amod_g_rst_n
15:0	INT_MASK_MISC	R/W	0h	Mask for the controller_int signal from the INT_MASK_MISC parameter Reset Source: ctl_amod_g_rst_n

14.5.1.2.409 EMIF_CTLCFG_DENALI_CTL_358 Register

1 EMIF_CTLCFG_DENALI_CTL_358 Register (Offset = 598h) [reset = 0h]

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Table 14-13582. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8598h**

Figure 14-4488. EMIF_CTLCFG_DENALI_CTL_358 Name Register

31	30	29	28	27	26	25	24
INT_MASK_INIT							
R/W							
0h							
23	22	21	20	19	18	17	16
INT_MASK_FREQ							
R/W							
0h							
15	14	13	12	11	10	9	8
MC_RESERVED25							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_DFI							
R/W							
0h							

Table 14-13584. EMIF_CTLCFG_DENALI_CTL_358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	INT_MASK_INIT	R/W	0h	Mask for the controller_int signal from the INT_MASK_INIT parameter Reset Source: ctl_amod_g_rst_n
23:16	INT_MASK_FREQ	R/W	0h	Mask for the controller_int signal from the INT_MASK_FREQ parameter Reset Source: ctl_amod_g_rst_n
15:8	MC_RESERVED25	R/W	0h	Reserved
7:0	INT_MASK_DFI	R/W	0h	Mask for the controller_int signal from the INT_MASK_DFI parameter Reset Source: ctl_amod_g_rst_n

14.5.1.2.410 EMIF_CTLCFG_DENALI_CTL_359 Register

1 EMIF_CTLCFG_DENALI_CTL_359 Register (Offset = 59Ch) [reset = 0h]

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Table 14-13585. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 859Ch**

Figure 14-4489. EMIF_CTLCFG_DENALI_CTL_359 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INT_MASK_PARITY							
R/W							
0h							
7	6	5	4	3	2	1	0
INT_MASK_MODE							
R/W							
0h							

Table 14-13587. EMIF_CTLCFG_DENALI_CTL_359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	INT_MASK_PARITY	R/W	0h	Mask for the controller_int signal from the INT_MASK_PARITY parameter Reset Source: ctl_amod_g_rst_n
7:0	INT_MASK_MODE	R/W	0h	Mask for the controller_int signal from the INT_MASK_MODE parameter Reset Source: ctl_amod_g_rst_n

14.5.1.2.411 EMIF_CTLCFG_DENALI_CTL_360 Register

1 EMIF_CTLCFG_DENALI_CTL_360 Register (Offset = 5A0h) [reset = 0h]

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Table 14-13588. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85A0h**

Figure 14-4490. EMIF_CTLCFG_DENALI_CTL_360 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">OUT_OF_RANGE_ADDR_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OUT_OF_RANGE_ADDR_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUT_OF_RANGE_ADDR_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUT_OF_RANGE_ADDR_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13590. EMIF_CTLCFG_DENALI_CTL_360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_OF_RANGE_ADDR_0	R	0h	Address of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.412 EMIF_CTLCFG_DENALI_CTL_361 Register

1 EMIF_CTLCFG_DENALI_CTL_361 Register (Offset = 5A4h) [reset = 0h]

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Table 14-13591. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 85A4h

Figure 14-4491. EMIF_CTLCFG_DENALI_CTL_361 Name Register

31	30	29	28	27	26	25	24
RESERVED	OUT_OF_RANGE_TYPE						
NONE	R						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED					OUT_OF_RANGE_LENGTH		
NONE					R		
0h					0h		

15	14	13	12	11	10	9	8
OUT_OF_RANGE_LENGTH							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							OUT_OF_RANGE_ADDR_1
NONE							R
0h							0h

Table 14-13593. EMIF_CTLCFG_DENALI_CTL_361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	OUT_OF_RANGE_TYPE	R	0h	Type of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	OUT_OF_RANGE_LENGTH	R	0h	Length of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	OUT_OF_RANGE_ADDR_1	R	0h	Address of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.413 EMIF_CTLCFG_DENALI_CTL_362 Register

1 EMIF_CTLCFG_DENALI_CTL_362 Register (Offset = 5A8h) [reset = 0h]

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Table 14-13594. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85A8h**

Figure 14-4492. EMIF_CTLCFG_DENALI_CTL_362 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		OUT_OF_RANGE_SOURCE_ID					
NONE		R					
0h		0h					

Table 14-13596. EMIF_CTLCFG_DENALI_CTL_362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	OUT_OF_RANGE_SOURCE_ID	R	0h	Source ID of command that caused an out-of-range interrupt. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.414 EMIF_CTLCFG_DENALI_CTL_363 Register

1 EMIF_CTLCFG_DENALI_CTL_363 Register (Offset = 5ACh) [reset = 0h]

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Table 14-13597. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85ACh**

Figure 14-4493. EMIF_CTLCFG_DENALI_CTL_363 Name Register

31	30	29	28	27	26	25	24
BIST_EXP_DATA_0							
R							
0h							
23	22	21	20	19	18	17	16
BIST_EXP_DATA_0							
R							
0h							
15	14	13	12	11	10	9	8
BIST_EXP_DATA_0							
R							
0h							
7	6	5	4	3	2	1	0
BIST_EXP_DATA_0							
R							
0h							

Table 14-13599. EMIF_CTLCFG_DENALI_CTL_363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_EXP_DATA_0	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.415 EMIF_CTLCFG_DENALI_CTL_364 Register

1 EMIF_CTLCFG_DENALI_CTL_364 Register (Offset = 5B0h) [reset = 0h]

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Table 14-13600. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 85B0h

Figure 14-4494. EMIF_CTLCFG_DENALI_CTL_364 Name Register

31	30	29	28	27	26	25	24
BIST_EXP_DATA_1							
R							
0h							
23	22	21	20	19	18	17	16
BIST_EXP_DATA_1							
R							
0h							
15	14	13	12	11	10	9	8
BIST_EXP_DATA_1							
R							
0h							
7	6	5	4	3	2	1	0
BIST_EXP_DATA_1							
R							
0h							

Table 14-13602. EMIF_CTLCFG_DENALI_CTL_364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_EXP_DATA_1	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.416 EMIF_CTLCFG_DENALI_CTL_365 Register

1 EMIF_CTLCFG_DENALI_CTL_365 Register (Offset = 5B4h) [reset = 0h]

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Table 14-13603. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85B4h**

Figure 14-4495. EMIF_CTLCFG_DENALI_CTL_365 Name Register

31	30	29	28	27	26	25	24
BIST_FAIL_DATA_0							
R							
0h							
23	22	21	20	19	18	17	16
BIST_FAIL_DATA_0							
R							
0h							
15	14	13	12	11	10	9	8
BIST_FAIL_DATA_0							
R							
0h							
7	6	5	4	3	2	1	0
BIST_FAIL_DATA_0							
R							
0h							

Table 14-13605. EMIF_CTLCFG_DENALI_CTL_365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_FAIL_DATA_0	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.417 EMIF_CTLCFG_DENALI_CTL_366 Register

1 EMIF_CTLCFG_DENALI_CTL_366 Register (Offset = 5B8h) [reset = 0h]

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Table 14-13606. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85B8h**

Figure 14-4496. EMIF_CTLCFG_DENALI_CTL_366 Name Register

31	30	29	28	27	26	25	24
BIST_FAIL_DATA_1							
R							
0h							
23	22	21	20	19	18	17	16
BIST_FAIL_DATA_1							
R							
0h							
15	14	13	12	11	10	9	8
BIST_FAIL_DATA_1							
R							
0h							
7	6	5	4	3	2	1	0
BIST_FAIL_DATA_1							
R							
0h							

Table 14-13608. EMIF_CTLCFG_DENALI_CTL_366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_FAIL_DATA_1	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.418 EMIF_CTLCFG_DENALI_CTL_367 Register

1 EMIF_CTLCFG_DENALI_CTL_367 Register (Offset = 5BCh) [reset = 0h]

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Table 14-13609. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85BCh**

Figure 14-4497. EMIF_CTLCFG_DENALI_CTL_367 Name Register

31	30	29	28	27	26	25	24
BIST_FAIL_ADDR_0							
R							
0h							
23	22	21	20	19	18	17	16
BIST_FAIL_ADDR_0							
R							
0h							
15	14	13	12	11	10	9	8
BIST_FAIL_ADDR_0							
R							
0h							
7	6	5	4	3	2	1	0
BIST_FAIL_ADDR_0							
R							
0h							

Table 14-13611. EMIF_CTLCFG_DENALI_CTL_367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BIST_FAIL_ADDR_0	R	0h	Address of BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.419 EMIF_CTLCFG_DENALI_CTL_368 Register

1 EMIF_CTLCFG_DENALI_CTL_368 Register (Offset = 5C0h) [reset = 0h]

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Table 14-13612. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 85C0h

Figure 14-4498. EMIF_CTLCFG_DENALI_CTL_368 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							BIST_FAIL_ADDR_1
NONE							R
0h							0h

Table 14-13614. EMIF_CTLCFG_DENALI_CTL_368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	BIST_FAIL_ADDR_1	R	0h	Address of BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.420 EMIF_CTLCFG_DENALI_CTL_369 Register

1 EMIF_CTLCFG_DENALI_CTL_369 Register (Offset = 5C4h) [reset = 0h]

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Table 14-13615. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85C4h**

Figure 14-4499. EMIF_CTLCFG_DENALI_CTL_369 Name Register

31	30	29	28	27	26	25	24
PORT_CMD_ERROR_ADDR_0							
R							
0h							
23	22	21	20	19	18	17	16
PORT_CMD_ERROR_ADDR_0							
R							
0h							
15	14	13	12	11	10	9	8
PORT_CMD_ERROR_ADDR_0							
R							
0h							
7	6	5	4	3	2	1	0
PORT_CMD_ERROR_ADDR_0							
R							
0h							

Table 14-13617. EMIF_CTLCFG_DENALI_CTL_369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_CMD_ERROR_ADDR_0	R	0h	Address of command that caused the PORT command error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.421 EMIF_CTLCFG_DENALI_CTL_370 Register

1 EMIF_CTLCFG_DENALI_CTL_370 Register (Offset = 5C8h) [reset = 0h]

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Table 14-13618. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85C8h**

Figure 14-4500. EMIF_CTLCFG_DENALI_CTL_370 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TODTL_2CMD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PORT_CMD_ERROR_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PORT_CMD_ERROR_ID</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PORT_CMD_ERROR_ADDR_1</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13620. EMIF_CTLCFG_DENALI_CTL_370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TODTL_2CMD_F0	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. FC=0 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PORT_CMD_ERROR_TYPE	R	0h	Type of error and access type that caused the PORT command error. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PORT_CMD_ERROR_ID	R	0h	Source ID of command that caused the PORT command error. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PORT_CMD_ERROR_ADDR_1	R	0h	Address of command that caused the PORT command error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.422 EMIF_CTLCFG_DENALI_CTL_371 Register

1 EMIF_CTLCFG_DENALI_CTL_371 Register (Offset = 5CCh) [reset = 0h]

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Table 14-13621. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85CCh**

Figure 14-4501. EMIF_CTLCFG_DENALI_CTL_371 Name Register

31	30	29	28	27	26	25	24
RESERVED				TODTH_WR_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TODTL_2CMD_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TODTH_RD_F0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TODTH_WR_F0			
NONE				R/W			
0h				0h			

Table 14-13623. EMIF_CTLCFG_DENALI_CTL_371 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TODTH_WR_F1	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TODTL_2CMD_F1	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TODTH_RD_F0	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TODTH_WR_F0	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.423 EMIF_CTLCFG_DENALI_CTL_372 Register

1 EMIF_CTLCFG_DENALI_CTL_372 Register (Offset = 5D0h) [reset = 0h]

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Table 14-13624. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85D0h**

Figure 14-4502. EMIF_CTLCFG_DENALI_CTL_372 Name Register

31	30	29	28	27	26	25	24
RESERVED				TODTH_RD_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				TODTH_WR_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
TODTL_2CMD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				TODTH_RD_F1			
NONE				R/W			
0h				0h			

Table 14-13626. EMIF_CTLCFG_DENALI_CTL_372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TODTH_RD_F2	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command. FC=2 Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TODTH_WR_F2	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TODTL_2CMD_F2	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TODTH_RD_F1	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.424 EMIF_CTLCFG_DENALI_CTL_373 Register

1 EMIF_CTLCFG_DENALI_CTL_373 Register (Offset = 5D4h) [reset = 0h]

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Table 14-13627. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85D4h**

Figure 14-4503. EMIF_CTLCFG_DENALI_CTL_373 Name Register

31	30	29	28	27	26	25	24
RESERVED							EN_ODT_ASSERT_EXCEPT_RD
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							ODT_EN_F2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ODT_EN_F1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							ODT_EN_F0
NONE							R/W
0h							0h

Table 14-13629. EMIF_CTLCFG_DENALI_CTL_373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	EN_ODT_ASSERT_EXCEPT_RD	R/W	0h	Enable controller to assert ODT at all times except during reads. Assumes single ODT pin connected. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	ODT_EN_F2	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed. FC=2 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	ODT_EN_F1	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed. FC=1 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	ODT_EN_F0	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.425 EMIF_CTLCFG_DENALI_CTL_374 Register

1 EMIF_CTLCFG_DENALI_CTL_374 Register (Offset = 5D8h) [reset = 0h]

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Table 14-13630. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85D8h**

Figure 14-4504. EMIF_CTLCFG_DENALI_CTL_374 Name Register

31	30	29	28	27	26	25	24
RESERVED						ODT_RD_MAP_CS0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED		WR_TO_ODTH_F2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED		WR_TO_ODTH_F1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		WR_TO_ODTH_F0					
NONE		R/W					
0h		0h					

Table 14-13632. EMIF_CTLCFG_DENALI_CTL_374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	ODT_RD_MAP_CS0	R/W	0h	Determines which chip[s] will have termination when a read occurs. Set bit X to enable termination on csX when a read is performed. CS=0 Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	WR_TO_ODTH_F2	R/W	0h	Defines the delay from a write command to ODT assertion. FC=2 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	WR_TO_ODTH_F1	R/W	0h	Defines the delay from a write command to ODT assertion. FC=1 Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	WR_TO_ODTH_F0	R/W	0h	Defines the delay from a write command to ODT assertion. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.426 EMIF_CTLCFG_DENALI_CTL_375 Register

1 EMIF_CTLCFG_DENALI_CTL_375 Register (Offset = 5DCh) [reset = 0h]

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Table 14-13633. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 85DCh

Figure 14-4505. EMIF_CTLCFG_DENALI_CTL_375 Name Register

31	30	29	28	27	26	25	24
RESERVED		RD_TO_ODTH_F0					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED						ODT_WR_MAP_CS1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						ODT_RD_MAP_CS1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						ODT_WR_MAP_CS0	
NONE						R/W	
0h						0h	

Table 14-13635. EMIF_CTLCFG_DENALI_CTL_375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	RD_TO_ODTH_F0	R/W	0h	Defines the delay from a read command to ODT assertion. FC=0 Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	ODT_WR_MAP_CS1	R/W	0h	Determines which chip[s] will have termination when a write occurs. Set bit X to enable termination on csX when a write is performed. CS=1 Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	ODT_RD_MAP_CS1	R/W	0h	Determines which chip[s] will have termination when a read occurs. Set bit X to enable termination on csX when a read is performed. CS=1 Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	ODT_WR_MAP_CS0	R/W	0h	Determines which chip[s] will have termination when a write occurs. Set bit X to enable termination on csX when a write is performed. CS=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.427 EMIF_CTLCFG_DENALI_CTL_376 Register

1 EMIF_CTLCFG_DENALI_CTL_376 Register (Offset = 5E0h) [reset = 8080000h]

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Table 14-13636. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 85E0h

Figure 14-4506. EMIF_CTLCFG_DENALI_CTL_376 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">RW2MRW_DLY_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">8h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">RW2MRW_DLY_F0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">8h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RD_TO_ODTH_F2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RD_TO_ODTH_F1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-13638. EMIF_CTLCFG_DENALI_CTL_376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	RW2MRW_DLY_F1	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	RW2MRW_DLY_F0	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system. FC=0 Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	RD_TO_ODTH_F2	R/W	0h	Defines the delay from a read command to ODT assertion. FC=2 Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	RD_TO_ODTH_F1	R/W	0h	Defines the delay from a read command to ODT assertion. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.428 EMIF_CTLCFG_DENALI_CTL_377 Register

1 EMIF_CTLCFG_DENALI_CTL_377 Register (Offset = 5E4h) [reset = 1010108h]

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Table 14-13639. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85E4h**

Figure 14-4507. EMIF_CTLCFG_DENALI_CTL_377 Name Register

31	30	29	28	27	26	25	24
RESERVED			W2R_DIFFCS_DLY_F0				
NONE			R/W				
0h			1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R2W_DIFFCS_DLY_F0				
NONE			R/W				
0h			1h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R2R_DIFFCS_DLY_F0				
NONE			R/W				
0h			1h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RW2MRW_DLY_F2				
NONE			R/W				
0h			8h				

Table 14-13641. EMIF_CTLCFG_DENALI_CTL_377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	W2R_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	R2W_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value. FC=0 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	R2R_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between reads to different chip selects. Program to a non-zero value. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	RW2MRW_DLY_F2	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.429 EMIF_CTLCFG_DENALI_CTL_378 Register

1 EMIF_CTLCFG_DENALI_CTL_378 Register (Offset = 5E8h) [reset = 1010101h]

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Table 14-13642. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 85E8h

Figure 14-4508. EMIF_CTLCFG_DENALI_CTL_378 Name Register

31	30	29	28	27	26	25	24
RESERVED			W2R_DIFFCS_DLY_F1				
NONE			R/W				
0h			1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R2W_DIFFCS_DLY_F1				
NONE			R/W				
0h			1h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R2R_DIFFCS_DLY_F1				
NONE			R/W				
0h			1h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			W2W_DIFFCS_DLY_F0				
NONE			R/W				
0h			1h				

Table 14-13644. EMIF_CTLCFG_DENALI_CTL_378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	W2R_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system. FC=1 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	R2W_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	R2R_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between reads to different chip selects. Program to a non-zero value. FC=1 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	W2W_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.430 EMIF_CTLCFG_DENALI_CTL_379 Register

1 EMIF_CTLCFG_DENALI_CTL_379 Register (Offset = 5ECh) [reset = 1010101h]

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Table 14-13645. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 85ECh

Figure 14-4509. EMIF_CTLCFG_DENALI_CTL_379 Name Register

31	30	29	28	27	26	25	24
RESERVED			W2R_DIFFCS_DLY_F2				
NONE			R/W				
0h			1h				
23	22	21	20	19	18	17	16
RESERVED			R2W_DIFFCS_DLY_F2				
NONE			R/W				
0h			1h				
15	14	13	12	11	10	9	8
RESERVED			R2R_DIFFCS_DLY_F2				
NONE			R/W				
0h			1h				
7	6	5	4	3	2	1	0
RESERVED			W2W_DIFFCS_DLY_F1				
NONE			R/W				
0h			1h				

Table 14-13647. EMIF_CTLCFG_DENALI_CTL_379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	W2R_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	R2W_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value. FC=2 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	R2R_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between reads to different chip selects. Program to a non-zero value. FC=2 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	W2W_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.431 EMIF_CTLCFG_DENALI_CTL_380 Register

1 EMIF_CTLCFG_DENALI_CTL_380 Register (Offset = 5F0h) [reset = 2020201h]

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Table 14-13648. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85F0h**

Figure 14-4510. EMIF_CTLCFG_DENALI_CTL_380 Name Register

31	30	29	28	27	26	25	24
RESERVED			R2W_SAMECS_DLY_F2				
NONE			R/W				
0h			2h				
23	22	21	20	19	18	17	16
RESERVED			R2W_SAMECS_DLY_F1				
NONE			R/W				
0h			2h				
15	14	13	12	11	10	9	8
RESERVED			R2W_SAMECS_DLY_F0				
NONE			R/W				
0h			2h				
7	6	5	4	3	2	1	0
RESERVED			W2W_DIFFCS_DLY_F2				
NONE			R/W				
0h			1h				

Table 14-13650. EMIF_CTLCFG_DENALI_CTL_380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	R2W_SAMECS_DLY_F2	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value. FC=2 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	R2W_SAMECS_DLY_F1	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value. FC=1 Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	R2W_SAMECS_DLY_F0	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value. FC=0 Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	W2W_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.432 EMIF_CTLCFG_DENALI_CTL_381 Register

1 EMIF_CTLCFG_DENALI_CTL_381 Register (Offset = 5F4h) [reset = 0h]

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Table 14-13651. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85F4h**

Figure 14-4511. EMIF_CTLCFG_DENALI_CTL_381 Name Register

31	30	29	28	27	26	25	24
RESERVED				TDQSCK_MAX_F0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED			W2W_SAMECS_DLY				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			W2R_SAMECS_DLY				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			R2R_SAMECS_DLY				
NONE			R/W				
0h			0h				

Table 14-13653. EMIF_CTLCFG_DENALI_CTL_381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TDQSCK_MAX_F0	R/W	0h	Additional delay needed for tDQSCK. FC=0 Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	W2W_SAMECS_DLY	R/W	0h	Additional delay to insert between two writes to the same chip select. Any value including 0 supported. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	W2R_SAMECS_DLY	R/W	0h	Additional delay to insert between writes and reads to the same chip select. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	R2R_SAMECS_DLY	R/W	0h	Additional delay to insert between two reads to the same chip select. Any value including 0 supported. Reset Source: ctl_amod_g_rst_n

14.5.1.2.433 EMIF_CTLCFG_DENALI_CTL_382 Register

1 EMIF_CTLCFG_DENALI_CTL_382 Register (Offset = 5F8h) [reset = 0h]

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Table 14-13654. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 85F8h

Figure 14-4512. EMIF_CTLCFG_DENALI_CTL_382 Name Register

31	30	29	28	27	26	25	24
RESERVED				TDQSCK_MAX_F2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					TDQSCK_MIN_F1		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TDQSCK_MAX_F1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TDQSCK_MIN_F0		
NONE					R/W		
0h					0h		

Table 14-13656. EMIF_CTLCFG_DENALI_CTL_382 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TDQSCK_MAX_F2	R/W	0h	Additional delay needed for tDQSCK. FC=2 Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	TDQSCK_MIN_F1	R/W	0h	Additional delay needed for tDQSCK. FC=1 Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TDQSCK_MAX_F1	R/W	0h	Additional delay needed for tDQSCK. FC=1 Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TDQSCK_MIN_F0	R/W	0h	Additional delay needed for tDQSCK. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.434 EMIF_CTLCFG_DENALI_CTL_383 Register

1 EMIF_CTLCFG_DENALI_CTL_383 Register (Offset = 5FCh) [reset = 0h]

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Table 14-13657. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 85FCh**

Figure 14-4513. EMIF_CTLCFG_DENALI_CTL_383 Name Register

31	30	29	28	27	26	25	24
RESERVED					AXI0_R_PRIORITY		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED							AXI0_FIXED_PORT_PRIORITY_ENABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							AXI0_ALL_STROBES_USED_ENABLE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TDQSCK_MIN_F2		
NONE					R/W		
0h					0h		

Table 14-13659. EMIF_CTLCFG_DENALI_CTL_383 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	AXI0_R_PRIORITY	R/W	0h	Priority of read commands from AXI port 0. 0 is the highest priority. This may only be changed before initialization begins or when the controller is quiescent, there is no data in the port FIFOs, and the AXI0_FIXED_PORT_PRIORITY_ENABLE parameter is low. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	AXI0_FIXED_PORT_PRIORITY_ENABLE	R/W	0h	Defines the priority control for AXI port 0 as per-port or per-command. Set to 1 for per-port with priority defined through the AXI.0._R_PRIORITY and AXI.0._W_PRIORITY parameters. Clear to 0 for per-command. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	AXI0_ALL_STROBES_USED_ENABLE	R/W	0h	Enables use of the AWALLSTRB signal for AXI port 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved

Table 14-13659. EMIF_CTLCFG_DENALI_CTL_383 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	TDQSCK_MIN_F2	R/W	0h	Additional delay needed for tDQSCK. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.435 EMIF_CTLCFG_DENALI_CTL_384 Register

1 EMIF_CTLCFG_DENALI_CTL_384 Register (Offset = 600h) [reset = 6000000h]

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Table 14-13660. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8600h**

Figure 14-4514. EMIF_CTLCFG_DENALI_CTL_384 Name Register

31	30	29	28	27	26	25	24
TDFI_PHY_RDLAT_F0							
R/W							
6h							

23	22	21	20	19	18	17	16
RESERVED							MEM_RST_VALID
NONE							R
0h							0h

15	14	13	12	11	10	9	8
RESERVED						CKE_STATUS	
NONE						R	
0h						0h	

7	6	5	4	3	2	1	0
RESERVED					AXI0_W_PRIORITY		
NONE					R/W		
0h					0h		

Table 14-13662. EMIF_CTLCFG_DENALI_CTL_384 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_PHY_RDLAT_F0	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion. FC=0 Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MEM_RST_VALID	R	0h	Register access to mem_rst_valid signal. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	CKE_STATUS	R	0h	Register access to cke_status signal. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	AXI0_W_PRIORITY	R/W	0h	Priority of write commands from AXI port 0. 0 is the highest priority. This may only be changed before initialization begins or when the controller is quiescent, there is no data in the port FIFOs, and the AXI0_FIXED_PORT_PRIORITY_ENABLE parameter is low. Reset Source: ctl_amod_g_rst_n

14.5.1.2.436 EMIF_CTLCFG_DENALI_CTL_385 Register

1 EMIF_CTLCFG_DENALI_CTL_385 Register (Offset = 604h) [reset = 0h]

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Table 14-13663. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8604h**

Figure 14-4515. EMIF_CTLCFG_DENALI_CTL_385 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TDFI_CTRLUPD_MAX_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_CTRLUPD_MAX_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_CTRLUPD_MAX_F0							
R/W							
0h							

Table 14-13665. EMIF_CTLCFG_DENALI_CTL_385 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	TDFI_CTRLUPD_MAX_F0	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.437 EMIF_CTLCFG_DENALI_CTL_386 Register

1 EMIF_CTLCFG_DENALI_CTL_386 Register (Offset = 608h) [reset = 0h]

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Table 14-13666. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8608h**

Figure 14-4516. EMIF_CTLCFG_DENALI_CTL_386 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE0_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE0_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE0_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F0							
R/W							
0h							

Table 14-13668. EMIF_CTLCFG_DENALI_CTL_386 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE0_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.438 EMIF_CTLCFG_DENALI_CTL_387 Register

1 EMIF_CTLCFG_DENALI_CTL_387 Register (Offset = 60Ch) [reset = 0h]

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Table 14-13669. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 860Ch**

Figure 14-4517. EMIF_CTLCFG_DENALI_CTL_387 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE1_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE1_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE1_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE1_F0							
R/W							
0h							

Table 14-13671. EMIF_CTLCFG_DENALI_CTL_387 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE1_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [2] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.439 EMIF_CTLCFG_DENALI_CTL_388 Register

1 EMIF_CTLCFG_DENALI_CTL_388 Register (Offset = 610h) [reset = 0h]

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Table 14-13672. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8610h

Figure 14-4518. EMIF_CTLCFG_DENALI_CTL_388 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE2_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE2_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE2_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE2_F0							
R/W							
0h							

Table 14-13674. EMIF_CTLCFG_DENALI_CTL_388 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE2_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [3] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.440 EMIF_CTLCFG_DENALI_CTL_389 Register

1 EMIF_CTLCFG_DENALI_CTL_389 Register (Offset = 614h) [reset = 0h]

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Table 14-13675. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8614h**

Figure 14-4519. EMIF_CTLCFG_DENALI_CTL_389 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE3_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE3_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE3_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F0							
R/W							
0h							

Table 14-13677. EMIF_CTLCFG_DENALI_CTL_389 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE3_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [4] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.441 EMIF_CTLCFG_DENALI_CTL_390 Register

1 EMIF_CTLCFG_DENALI_CTL_390 Register (Offset = 618h) [reset = 0h]

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Table 14-13678. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8618h**

Figure 14-4520. EMIF_CTLCFG_DENALI_CTL_390 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	TDFI_PHYUPD_RESP_F0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
TDFI_PHYUPD_RESP_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_RESP_F0							
R/W							
0h							

Table 14-13680. EMIF_CTLCFG_DENALI_CTL_390 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	TDFI_PHYUPD_RESP_F0	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [5] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.442 EMIF_CTLCFG_DENALI_CTL_391 Register

1 EMIF_CTLCFG_DENALI_CTL_391 Register (Offset = 61Ch) [reset = 0h]

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Table 14-13681. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 861Ch**

Figure 14-4521. EMIF_CTLCFG_DENALI_CTL_391 Name Register

31	30	29	28	27	26	25	24
TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							

Table 14-13683. EMIF_CTLCFG_DENALI_CTL_391 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_CTRLUPD_INTERVAL_F0	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks], the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [6] set in the UPDATE_ERROR_STATUS parameter. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.443 EMIF_CTLCFG_DENALI_CTL_392 Register

1 EMIF_CTLCFG_DENALI_CTL_392 Register (Offset = 620h) [reset = 2h]

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Table 14-13684. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8620h**

Figure 14-4522. EMIF_CTLCFG_DENALI_CTL_392 Name Register

31	30	29	28	27	26	25	24
TDFI_RDDATA_EN_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_RDCSLAT_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					TDFI_PHY_WRDATA_F0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TDFI_CTRL_DELAY_F0			
NONE				R/W			
0h				2h			

Table 14-13686. EMIF_CTLCFG_DENALI_CTL_392 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_RDDATA_EN_F0	R/W	0h	DFI tRDDATA_EN timing parameter. This is the number of DFI data phases between a read command and the first assertion of dfi_rddata_en_pN. FC=0 Reset Source: ctl_amod_g_rst_n
23:16	TDFI_RDCSLAT_F0	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a read command and a dfi_rddata_cs_n assertion. FC=0 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TDFI_PHY_WRDATA_F0	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TDFI_CTRL_DELAY_F0	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks], the delay between a DFI command change and a memory command. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.444 EMIF_CTLCFG_DENALI_CTL_393 Register

1 EMIF_CTLCFG_DENALI_CTL_393 Register (Offset = 624h) [reset = 60000h]

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Table 14-13687. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8624h**

Figure 14-4523. EMIF_CTLCFG_DENALI_CTL_393 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHY_RDLAT_F1							
R/W							
6h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHY_WRLAT_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_WRCSLAT_F0							
R/W							
0h							

Table 14-13689. EMIF_CTLCFG_DENALI_CTL_393 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TDFI_PHY_RDLAT_F1	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion. FC=1 Reset Source: ctl_amod_g_rst_n
15:8	TDFI_PHY_WRLAT_F0	R/W	0h	DFI tPHY_WRLAT timing parameter. This is the number of DFI data phases between a write command and the first assertion of dfi_wrdata_en_pN. FC=0 Reset Source: ctl_amod_g_rst_n
7:0	TDFI_WRCSLAT_F0	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.445 EMIF_CTLCFG_DENALI_CTL_394 Register

1 EMIF_CTLCFG_DENALI_CTL_394 Register (Offset = 628h) [reset = 0h]

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Table 14-13690. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8628h**

Figure 14-4524. EMIF_CTLCFG_DENALI_CTL_394 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			TDFI_CTRLUPD_MAX_F1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
TDFI_CTRLUPD_MAX_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_CTRLUPD_MAX_F1							
R/W							
0h							

Table 14-13692. EMIF_CTLCFG_DENALI_CTL_394 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	TDFI_CTRLUPD_MAX_F1	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.446 EMIF_CTLCFG_DENALI_CTL_395 Register

1 EMIF_CTLCFG_DENALI_CTL_395 Register (Offset = 62Ch) [reset = 0h]

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Table 14-13693. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 862Ch**

Figure 14-4525. EMIF_CTLCFG_DENALI_CTL_395 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE0_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE0_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE0_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F1							
R/W							
0h							

Table 14-13695. EMIF_CTLCFG_DENALI_CTL_395 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE0_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.447 EMIF_CTLCFG_DENALI_CTL_396 Register

1 EMIF_CTLCFG_DENALI_CTL_396 Register (Offset = 630h) [reset = 0h]

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Table 14-13696. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8630h**

Figure 14-4526. EMIF_CTLCFG_DENALI_CTL_396 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE1_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYUPD_TYPE1_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYUPD_TYPE1_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYUPD_TYPE1_F1							
R/W							
0h							

Table 14-13698. EMIF_CTLCFG_DENALI_CTL_396 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE1_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [2] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.448 EMIF_CTLCFG_DENALI_CTL_397 Register

1 EMIF_CTLCFG_DENALI_CTL_397 Register (Offset = 634h) [reset = 0h]

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Table 14-13699. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8634h**

Figure 14-4527. EMIF_CTLCFG_DENALI_CTL_397 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE2_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYUPD_TYPE2_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYUPD_TYPE2_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYUPD_TYPE2_F1							
R/W							
0h							

Table 14-13701. EMIF_CTLCFG_DENALI_CTL_397 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE2_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [3] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.449 EMIF_CTLCFG_DENALI_CTL_398 Register

1 EMIF_CTLCFG_DENALI_CTL_398 Register (Offset = 638h) [reset = 0h]

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Table 14-13702. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8638h**

Figure 14-4528. EMIF_CTLCFG_DENALI_CTL_398 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE3_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE3_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE3_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F1							
R/W							
0h							

Table 14-13704. EMIF_CTLCFG_DENALI_CTL_398 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE3_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [4] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.450 EMIF_CTLCFG_DENALI_CTL_399 Register

1 EMIF_CTLCFG_DENALI_CTL_399 Register (Offset = 63Ch) [reset = 0h]

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Table 14-13705. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 863Ch**

Figure 14-4529. EMIF_CTLCFG_DENALI_CTL_399 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	TDFI_PHYUPD_RESP_F1						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYUPD_RESP_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYUPD_RESP_F1							
R/W							
0h							

Table 14-13707. EMIF_CTLCFG_DENALI_CTL_399 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	TDFI_PHYUPD_RESP_F1	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [5] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.451 EMIF_CTLCFG_DENALI_CTL_400 Register

1 EMIF_CTLCFG_DENALI_CTL_400 Register (Offset = 640h) [reset = 0h]

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Table 14-13708. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8640h**

Figure 14-4530. EMIF_CTLCFG_DENALI_CTL_400 Name Register

31	30	29	28	27	26	25	24
TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							

Table 14-13710. EMIF_CTLCFG_DENALI_CTL_400 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_CTRLUPD_INTERVAL_F1	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks], the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [6] set in the UPDATE_ERROR_STATUS parameter. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.452 EMIF_CTLCFG_DENALI_CTL_401 Register

1 EMIF_CTLCFG_DENALI_CTL_401 Register (Offset = 644h) [reset = 2h]

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Table 14-13711. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8644h**

Figure 14-4531. EMIF_CTLCFG_DENALI_CTL_401 Name Register

31	30	29	28	27	26	25	24
TDFI_RDDATA_EN_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_RDCSLAT_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					TDFI_PHY_WRDATA_F1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TDFI_CTRL_DELAY_F1			
NONE				R/W			
0h				2h			

Table 14-13713. EMIF_CTLCFG_DENALI_CTL_401 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_RDDATA_EN_F1	R/W	0h	DFI tRDDATA_EN timing parameter. This is the number of DFI data phases between a read command and the first assertion of dfi_rddata_en_pN. FC=1 Reset Source: ctl_amod_g_rst_n
23:16	TDFI_RDCSLAT_F1	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a read command and a dfi_rddata_cs_n assertion. FC=1 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TDFI_PHY_WRDATA_F1	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. FC=1 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TDFI_CTRL_DELAY_F1	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks], the delay between a DFI command change and a memory command. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.453 EMIF_CTLCFG_DENALI_CTL_402 Register

1 EMIF_CTLCFG_DENALI_CTL_402 Register (Offset = 648h) [reset = 60000h]

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Table 14-13714. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8648h**

Figure 14-4532. EMIF_CTLCFG_DENALI_CTL_402 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDFI_PHY_RDLAT_F2							
R/W							
6h							
15	14	13	12	11	10	9	8
TDFI_PHY_WRLAT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_WRCSLAT_F1							
R/W							
0h							

Table 14-13716. EMIF_CTLCFG_DENALI_CTL_402 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TDFI_PHY_RDLAT_F2	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion. FC=2 Reset Source: ctl_amod_g_rst_n
15:8	TDFI_PHY_WRLAT_F1	R/W	0h	DFI tPHY_WRLAT timing parameter. This is the number of DFI data phases between a write command and the first assertion of dfi_wrdata_en_pN. FC=1 Reset Source: ctl_amod_g_rst_n
7:0	TDFI_WRCSLAT_F1	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. FC=1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.454 EMIF_CTLCFG_DENALI_CTL_403 Register

1 EMIF_CTLCFG_DENALI_CTL_403 Register (Offset = 64Ch) [reset = 0h]

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Table 14-13717. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 864Ch**

Figure 14-4533. EMIF_CTLCFG_DENALI_CTL_403 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			TDFI_CTRLUPD_MAX_F2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
TDFI_CTRLUPD_MAX_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_CTRLUPD_MAX_F2							
R/W							
0h							

Table 14-13719. EMIF_CTLCFG_DENALI_CTL_403 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	TDFI_CTRLUPD_MAX_F2	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks], the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.455 EMIF_CTLCFG_DENALI_CTL_404 Register

1 EMIF_CTLCFG_DENALI_CTL_404 Register (Offset = 650h) [reset = 0h]

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Table 14-13720. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8650h**

Figure 14-4534. EMIF_CTLCFG_DENALI_CTL_404 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE0_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE0_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE0_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F2							
R/W							
0h							

Table 14-13722. EMIF_CTLCFG_DENALI_CTL_404 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE0_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.456 EMIF_CTLCFG_DENALI_CTL_405 Register

1 EMIF_CTLCFG_DENALI_CTL_405 Register (Offset = 654h) [reset = 0h]

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Table 14-13723. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8654h**

Figure 14-4535. EMIF_CTLCFG_DENALI_CTL_405 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE1_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYUPD_TYPE1_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYUPD_TYPE1_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYUPD_TYPE1_F2							
R/W							
0h							

Table 14-13725. EMIF_CTLCFG_DENALI_CTL_405 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE1_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit [2] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.457 EMIF_CTLCFG_DENALI_CTL_406 Register

1 EMIF_CTLCFG_DENALI_CTL_406 Register (Offset = 658h) [reset = 0h]

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Table 14-13726. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8658h

Figure 14-4536. EMIF_CTLCFG_DENALI_CTL_406 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE2_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDFI_PHYUPD_TYPE2_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHYUPD_TYPE2_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_PHYUPD_TYPE2_F2							
R/W							
0h							

Table 14-13728. EMIF_CTLCFG_DENALI_CTL_406 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE2_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit [3] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.458 EMIF_CTLCFG_DENALI_CTL_407 Register

1 EMIF_CTLCFG_DENALI_CTL_407 Register (Offset = 65Ch) [reset = 0h]

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Table 14-13729. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 865Ch**

Figure 14-4537. EMIF_CTLCFG_DENALI_CTL_407 Name Register

31	30	29	28	27	26	25	24
TDFI_PHYUPD_TYPE3_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_PHYUPD_TYPE3_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_PHYUPD_TYPE3_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F2							
R/W							
0h							

Table 14-13731. EMIF_CTLCFG_DENALI_CTL_407 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_PHYUPD_TYPE3_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter [in DFI clocks], the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit [4] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.459 EMIF_CTLCFG_DENALI_CTL_408 Register

1 EMIF_CTLCFG_DENALI_CTL_408 Register (Offset = 660h) [reset = 0h]

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Table 14-13732. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8660h**

Figure 14-4538. EMIF_CTLCFG_DENALI_CTL_408 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	TDFI_PHYUPD_RESP_F2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
TDFI_PHYUPD_RESP_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_PHYUPD_RESP_F2							
R/W							
0h							

Table 14-13734. EMIF_CTLCFG_DENALI_CTL_408 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	TDFI_PHYUPD_RESP_F2	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit [5] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.460 EMIF_CTLCFG_DENALI_CTL_409 Register

1 EMIF_CTLCFG_DENALI_CTL_409 Register (Offset = 664h) [reset = 0h]

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Table 14-13735. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8664h

Figure 14-4539. EMIF_CTLCFG_DENALI_CTL_409 Name Register

31	30	29	28	27	26	25	24
TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							

Table 14-13737. EMIF_CTLCFG_DENALI_CTL_409 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDFI_CTRLUPD_INTERVAL_F2	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks], the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [6] set in the UPDATE_ERROR_STATUS parameter. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.461 EMIF_CTLCFG_DENALI_CTL_410 Register

1 EMIF_CTLCFG_DENALI_CTL_410 Register (Offset = 668h) [reset = 2h]

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Table 14-13738. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8668h**

Figure 14-4540. EMIF_CTLCFG_DENALI_CTL_410 Name Register

31	30	29	28	27	26	25	24
TDFI_RDDATA_EN_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
TDFI_RDCSLAT_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					TDFI_PHY_WRDATA_F2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				TDFI_CTRL_DELAY_F2			
NONE				R/W			
0h				2h			

Table 14-13740. EMIF_CTLCFG_DENALI_CTL_410 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TDFI_RDDATA_EN_F2	R/W	0h	DFI tRDDATA_EN timing parameter. This is the number of DFI data phases between a read command and the first assertion of dfi_rddata_en_pN. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	TDFI_RDCSLAT_F2	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a read command and a dfi_rddata_cs_n assertion. FC=2 Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	TDFI_PHY_WRDATA_F2	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks], the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. FC=2 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TDFI_CTRL_DELAY_F2	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks], the delay between a DFI command change and a memory command. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.462 EMIF_CTLCFG_DENALI_CTL_411 Register

1 EMIF_CTLCFG_DENALI_CTL_411 Register (Offset = 66Ch) [reset = 0h]

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Table 14-13741. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 866Ch**

Figure 14-4541. EMIF_CTLCFG_DENALI_CTL_411 Name Register

31	30	29	28	27	26	25	24
DLL_RST_DELAY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DLL_RST_DELAY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_PHY_WRLAT_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_WRCSLAT_F2							
R/W							
0h							

Table 14-13743. EMIF_CTLCFG_DENALI_CTL_411 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DLL_RST_DELAY	R/W	0h	Minimum cycles required for DLL reset signal dll_rst_n to be held. If this signal is not being used by the PHY, this parameter may be ignored. Reset Source: ctl_amod_g_rst_n
15:8	TDFI_PHY_WRLAT_F2	R/W	0h	DFI tPHY_WRLAT timing parameter. This is the number of DFI data phases between a write command and the first assertion of dfi_wrdata_en_pN. FC=2 Reset Source: ctl_amod_g_rst_n
7:0	TDFI_WRCSLAT_F2	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter [in DFI PHY clocks], the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. FC=2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.463 EMIF_CTLCFG_DENALI_CTL_412 Register

1 EMIF_CTLCFG_DENALI_CTL_412 Register (Offset = 670h) [reset = 0h]

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Table 14-13744. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8670h**

Figure 14-4542. EMIF_CTLCFG_DENALI_CTL_412 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">DRAM_CLK_DISABLE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">UPDATE_ERROR_STATUS</td></tr>
<tr><td>NONE</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DLL_RST_ADJ_DLY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13746. EMIF_CTLCFG_DENALI_CTL_412 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	DRAM_CLK_DISABLE	R/W	0h	Set value for the dfi_dram_clk_disable signal. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to disable. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	UPDATE_ERROR_STATUS	R	0h	Identifies the source of any DFI MC-initiated or PHY-initiated update errors. Value of 1 indicates a timing violation of the associated timing parameter. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	DLL_RST_ADJ_DLY	R/W	0h	Minimum cycles after setting controller delay in DLL until the DLL reset signal dll_rst_n may be asserted. If this signal is not being used by the PHY, this parameter may be ignored. Reset Source: ctl_amod_g_rst_n

14.5.1.2.464 EMIF_CTLCFG_DENALI_CTL_413 Register

1 EMIF_CTLCFG_DENALI_CTL_413 Register (Offset = 674h) [reset = 0h]

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Table 14-13747. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8674h

Figure 14-4543. EMIF_CTLCFG_DENALI_CTL_413 Name Register

31	30	29	28	27	26	25	24
RESERVED				TDFI_DRAM_CLK_ENABLE			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TDFI_DRAM_CLK_DISABLE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_CTRLUPD_MIN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDFI_CTRLUPD_MIN							
R/W							
0h							

Table 14-13749. EMIF_CTLCFG_DENALI_CTL_413 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TDFI_DRAM_CLK_ENABLE	R/W	0h	Defines the DFI tDRAM_CLK_ENABLE timing parameter [in DFI clocks], the delay between a dfi_dram_clk_disable de-assertion and the memory clock enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TDFI_DRAM_CLK_DISABLE	R/W	0h	Defines the DFI tDRAM_CLK_DISABLE timing parameter [in DFI clocks], the delay between a dfi_dram_clock_disable assertion and the memory clock disable. Reset Source: ctl_amod_g_rst_n
15:0	TDFI_CTRLUPD_MIN	R/W	0h	Defines the DFI tCTRLUPD_MIN timing parameter [in DFI clocks], the minimum cycles that dfi_ctrlupd_req must be asserted. Reset Source: ctl_amod_g_rst_n

14.5.1.2.465 EMIF_CTLCFG_DENALI_CTL_414 Register

1 EMIF_CTLCFG_DENALI_CTL_414 Register (Offset = 678h) [reset = 0h]

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Table 14-13750. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8678h

Figure 14-4544. EMIF_CTLCFG_DENALI_CTL_414 Name Register

31	30	29	28	27	26	25	24
RESERVED					STRATEGY_2TICK_COUNT		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							DISABLE_MEMORY_MASKED_WRITE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDFI_WRDATA_DELAY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TDFI_PARIN_LAT		
NONE					R/W		
0h					0h		

Table 14-13752. EMIF_CTLCFG_DENALI_CTL_414 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	STRATEGY_2TICK_COUNT	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	DISABLE_MEMORY_MASKED_WRITE	R/W	0h	Restricts the controller from masked write commands. Set to 1 to not issue these commands. Only used if connected to an LPDDR4 device. Reset Source: ctl_amod_g_rst_n
15:8	TDFI_WRDATA_DELAY	R/W	0h	Defines the tWRDATA_DELAY timing parameter [in DFI PHY clocks], the maximum cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TDFI_PARIN_LAT	R/W	0h	Defines the DFI tPARIN_LAT timing parameter [in DFI PHY clocks], the maximum cycles between a DFI command and a dfi_parity_in signal assertion. Reset Source: ctl_amod_g_rst_n

14.5.1.2.466 EMIF_CTLCFG_DENALI_CTL_415 Register

1 EMIF_CTLCFG_DENALI_CTL_415 Register (Offset = 67Ch) [reset = 1010000h]

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Table 14-13753. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 867Ch**

Figure 14-4545. EMIF_CTLCFG_DENALI_CTL_415 Name Register

31	30	29	28	27	26	25	24
RESERVED					BANK_ACTIVATE_4TICK_COUNT		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					STRATEGY_4TICK_COUNT		
NONE					R/W		
0h					1h		
15	14	13	12	11	10	9	8
RESERVED					PRE_2TICK_COUNT		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED					BANK_ACTIVATE_2TICK_COUNT		
NONE					R/W		
0h					0h		

Table 14-13755. EMIF_CTLCFG_DENALI_CTL_415 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	BANK_ACTIVATE_4TICK_COUNT	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	STRATEGY_4TICK_COUNT	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PRE_2TICK_COUNT	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	BANK_ACTIVATE_2TICK_COUNT	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.5.1.2.467 EMIF_CTLCFG_DENALI_CTL_416 Register

1 EMIF_CTLCFG_DENALI_CTL_416 Register (Offset = 680h) [reset = 10001h]

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Table 14-13756. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8680h**

Figure 14-4546. EMIF_CTLCFG_DENALI_CTL_416 Name Register

31	30	29	28	27	26	25	24
RESERVED				TMP_NXN_TICK_PLUS_ADJ			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TMP_2X4_TICK_MINUS_ADJ			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TMP_2X4_TICK_PLUS_ADJ			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PRE_4TICK_COUNT		
NONE					R/W		
0h					1h		

Table 14-13758. EMIF_CTLCFG_DENALI_CTL_416 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TMP_NXN_TICK_PLUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TMP_2X4_TICK_MINUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TMP_2X4_TICK_PLUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PRE_4TICK_COUNT	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.5.1.2.468 EMIF_CTLCFG_DENALI_CTL_417 Register

1 EMIF_CTLCFG_DENALI_CTL_417 Register (Offset = 684h) [reset = 1010001h]

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Table 14-13759. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8684h**

Figure 14-4547. EMIF_CTLCFG_DENALI_CTL_417 Name Register

31	30	29	28	27	26	25	24
RESERVED				TRAS_TICK_PLUS_ADJ			
NONE				R/W			
0h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				ODT_TICK_MINUS_ADJ			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				ODT_TICK_PLUS_ADJ			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TMP_NXN_TICK_MINUS_ADJ			
NONE				R/W			
0h				1h			

Table 14-13761. EMIF_CTLCFG_DENALI_CTL_417 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TRAS_TICK_PLUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	ODT_TICK_MINUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	ODT_TICK_PLUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TMP_NXN_TICK_MINUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.5.1.2.469 EMIF_CTLCFG_DENALI_CTL_418 Register

1 EMIF_CTLCFG_DENALI_CTL_418 Register (Offset = 688h) [reset = 2000100h]

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Table 14-13762. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8688h

Figure 14-4548. EMIF_CTLCFG_DENALI_CTL_418 Name Register

31	30	29	28	27	26	25	24
RESERVED				TWR_TICK_PLUS_ADJ			
NONE				R/W			
0h				2h			
23	22	21	20	19	18	17	16
RESERVED				TRP_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				TRP_TICK_PLUS_ADJ			
NONE				R/W			
0h				1h			
7	6	5	4	3	2	1	0
RESERVED				TRAS_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			

Table 14-13764. EMIF_CTLCFG_DENALI_CTL_418 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TWR_TICK_PLUS_ADJ	R/W	2h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TRP_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TRP_TICK_PLUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TRAS_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.5.1.2.470 EMIF_CTLCFG_DENALI_CTL_419 Register

1 EMIF_CTLCFG_DENALI_CTL_419 Register (Offset = 68Ch) [reset = 200h]

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Table 14-13765. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 868Ch**

Figure 14-4549. EMIF_CTLCFG_DENALI_CTL_419 Name Register

31	30	29	28	27	26	25	24
RESERVED				TRFC_TICK_PLUS_ADJ			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				TMP_4X2_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				TMP_4X2_TICK_PLUS_ADJ			
NONE				R/W			
0h				2h			
7	6	5	4	3	2	1	0
RESERVED				TWR_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			

Table 14-13767. EMIF_CTLCFG_DENALI_CTL_419 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	TRFC_TICK_PLUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	TMP_4X2_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	TMP_4X2_TICK_PLUS_ADJ	R/W	2h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TWR_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.5.1.2.471 EMIF_CTLCFG_DENALI_CTL_420 Register

1 EMIF_CTLCFG_DENALI_CTL_420 Register (Offset = 690h) [reset = 2000201h]

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Table 14-13768. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8690h

Figure 14-4550. EMIF_CTLCFG_DENALI_CTL_420 Name Register

31	30	29	28	27	26	25	24
RESERVED				WL_TICK_PLUS_ADJ			
NONE				R/W			
0h				2h			
23	22	21	20	19	18	17	16
RESERVED				RL_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				RL_TICK_PLUS_ADJ			
NONE				R/W			
0h				2h			
7	6	5	4	3	2	1	0
RESERVED				TRFC_TICK_MINUS_ADJ			
NONE				R/W			
0h				1h			

Table 14-13770. EMIF_CTLCFG_DENALI_CTL_420 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	WL_TICK_PLUS_ADJ	R/W	2h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	RL_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	RL_TICK_PLUS_ADJ	R/W	2h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	TRFC_TICK_MINUS_ADJ	R/W	1h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.5.1.2.472 EMIF_CTLCFG_DENALI_CTL_421 Register

1 EMIF_CTLCFG_DENALI_CTL_421 Register (Offset = 694h) [reset = 28282800h]

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Table 14-13771. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 8694h**

Figure 14-4551. EMIF_CTLCFG_DENALI_CTL_421 Name Register

31	30	29	28	27	26	25	24
NWR_F2							
R/W							
28h							
23	22	21	20	19	18	17	16
NWR_F1							
R/W							
28h							
15	14	13	12	11	10	9	8
NWR_F0							
R/W							
28h							
7	6	5	4	3	2	1	0
RESERVED				WL_TICK_MINUS_ADJ			
NONE				R/W			
0h				0h			

Table 14-13773. EMIF_CTLCFG_DENALI_CTL_421 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NWR_F2	R/W	28h	DRAM NWR value in cycles. FC=2 Reset Source: ctl_amod_g_rst_n
23:16	NWR_F1	R/W	28h	DRAM NWR value in cycles. FC=1 Reset Source: ctl_amod_g_rst_n
15:8	NWR_F0	R/W	28h	DRAM NWR value in cycles. FC=0 Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	WL_TICK_MINUS_ADJ	R/W	0h	NEED TO FiLL IN . Reset Source: ctl_amod_g_rst_n

14.5.1.2.473 *EMIF_CTLCFG_DENALI_CTL_422 Register*

1 EMIF_CTLCFG_DENALI_CTL_422 Register (Offset = 698h) [reset = 0h]

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Table 14-13774. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 8698h

Figure 14-4552. EMIF_CTLCFG_DENALI_CTL_422 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	TDFI_CTRLMSG_RESP_F2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	TDFI_CTRLMSG_RESP_F1						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	TDFI_CTRLMSG_RESP_F0						
NONE	R/W						
0h	0h						

Table 14-13776. EMIF_CTLCFG_DENALI_CTL_422 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	TDFI_CTRLMSG_RESP_F2	R/W	0h	Defines the DFI tCTRLMSG_RESP timing parameter [in DFI clocks], the maximum number of DFI clocks allowed for dfi_ctrlmsg_ack to assert after dfi_ctrlmsg_req goes high. FC=2 Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	TDFI_CTRLMSG_RESP_F1	R/W	0h	Defines the DFI tCTRLMSG_RESP timing parameter [in DFI clocks], the maximum number of DFI clocks allowed for dfi_ctrlmsg_ack to assert after dfi_ctrlmsg_req goes high. FC=1 Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	TDFI_CTRLMSG_RESP_F0	R/W	0h	Defines the DFI tCTRLMSG_RESP timing parameter [in DFI clocks], the maximum number of DFI clocks allowed for dfi_ctrlmsg_ack to assert after dfi_ctrlmsg_req goes high. FC=0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.474 EMIF_CTLCFG_DENALI_PI_0 Register

1 EMIF_CTLCFG_DENALI_PI_0 Register (Offset = 2000h) [reset = 0h]

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Table 14-13777. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A000h**

Figure 14-4553. EMIF_CTLCFG_DENALI_PI_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_DRAM_CLASS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_START</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13779. EMIF_CTLCFG_DENALI_PI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PI_DRAM_CLASS	R/W	0h	Defines the memory class for the PI. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_START	R/W	0h	Initiate command processing in the PI. Set to 1 to initiate. Reset Source: ctl_amod_g_rst_n

14.5.1.2.475 EMIF_CTLCFG_DENALI_PI_1 Register

1 EMIF_CTLCFG_DENALI_PI_1 Register (Offset = 2004h) [reset = AE8D79E2h]

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Table 14-13780. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A004h**

Figure 14-4554. EMIF_CTLCFG_DENALI_PI_1 Name Register

31	30	29	28	27	26	25	24
PI_VERSION_0							
R							
AE8D79E2h							
23	22	21	20	19	18	17	16
PI_VERSION_0							
R							
AE8D79E2h							
15	14	13	12	11	10	9	8
PI_VERSION_0							
R							
AE8D79E2h							
7	6	5	4	3	2	1	0
PI_VERSION_0							
R							
AE8D79E2h							

Table 14-13782. EMIF_CTLCFG_DENALI_PI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_VERSION_0	R	AE8D79E2h	Holds the PI version number. This is a unique number for each PHY IP delivery. This will help in identifying different version of the PHY IP. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.476 EMIF_CTLCFG_DENALI_PI_2 Register

1 EMIF_CTLCFG_DENALI_PI_2 Register (Offset = 2008h) [reset = 714B570h]

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Table 14-13783. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A008h**

Figure 14-4555. EMIF_CTLCFG_DENALI_PI_2 Name Register

31	30	29	28	27	26	25	24
PI_VERSION_1							
R							
714B570h							
23	22	21	20	19	18	17	16
PI_VERSION_1							
R							
714B570h							
15	14	13	12	11	10	9	8
PI_VERSION_1							
R							
714B570h							
7	6	5	4	3	2	1	0
PI_VERSION_1							
R							
714B570h							

Table 14-13785. EMIF_CTLCFG_DENALI_PI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_VERSION_1	R	714B570h	Holds the PI version number. This is a unique number for each PHY IP delivery. This will help in identifying different version of the PHY IP. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.477 EMIF_CTLCFG_DENALI_PI_3 Register

1 EMIF_CTLCFG_DENALI_PI_3 Register (Offset = 200Ch) [reset = 11387h]

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Table 14-13786. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A00Ch

Figure 14-4556. EMIF_CTLCFG_DENALI_PI_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_NORMAL_LVL_SEQ
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RELEASE_DFI
NONE							R
0h							1h
15	14	13	12	11	10	9	8
PI_ID							
R							
1387h							
7	6	5	4	3	2	1	0
PI_ID							
R							
1387h							

Table 14-13788. EMIF_CTLCFG_DENALI_PI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_NORMAL_LVL_SEQ	R/W	0h	Enable the PI to finish all the pending leveling before releasing the DFI bus. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RELEASE_DFI	R	1h	This is a status whether PI has release DFI. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:0	PI_ID	R	1387h	Holds the PI ID number. This is a Cadence DDR PHY IP identifier. It is set to 0x1387. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.478 EMIF_CTLCFG_DENALI_PI_4 Register

1 EMIF_CTLCFG_DENALI_PI_4 Register (Offset = 2010h) [reset = 0h]

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Table 14-13789. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A010h**

Figure 14-4557. EMIF_CTLCFG_DENALI_PI_4 Name Register

31	30	29	28	27	26	25	24
PI_TCMD_GAP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TCMD_GAP							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_NOTCARE_PHYUPD	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PI_INIT_LVL_EN
NONE							R/W
0h							0h

Table 14-13791. EMIF_CTLCFG_DENALI_PI_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TCMD_GAP	R/W	0h	Specifies the minimum gap in DFI clocks between two commands. Used to guard the timing from the last command of MC and the first command of PI when MC hand over the control of DFI to PI. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_NOTCARE_PHYUPD	R/W	0h	Allow the PI to issue a controller request to the controller if a phyupd_req from the PHY has been detected.bit[1] represents supports in normal state;bit[0] represents supports in initialization state. Set to 1 to issue the controller request. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_INIT_LVL_EN	R/W	0h	Enables the initial leveling sequence after PI initialization procedure. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.479 EMIF_CTLCFG_DENALI_PI_5 Register

1 EMIF_CTLCFG_DENALI_PI_5 Register (Offset = 2014h) [reset = 64h]

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Table 14-13792. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A014h

Figure 14-4558. EMIF_CTLCFG_DENALI_PI_5 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_DFI_PHYMSTR_TYPE	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_DFI_VERSION
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_TRAIN_ALL_FREQ_REQ
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_RESERVED0							
R/W							
64h							

Table 14-13794. EMIF_CTLCFG_DENALI_PI_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_DFI_PHYMSTR_TYPE	R/W	0h	DFI Controller Request Type used for dfi 4.1 verision: This signal indicates the required state of DRAM when PHY becomes the controller. Each memory rank uses one bit. 1'b0: IDLE. The MC should close all the pages. 1'b1: IDLE or Self Refresh. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DFI_VERSION	R/W	0h	Define the DFI controller version, set 1 for DFI4.1, set 0 for DFI4.0 Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_TRAIN_ALL_FREQ_REQ	W	0h	Triggers training for all supported frequencies in PI_FREQ_MAP. Applies to LPDDR4 devices onlyh. Set to 1 to trigger. Only applicable after memory initialization has been completed. Can be used to train new frequencies that were not available at initialization time. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PI_RESERVED0	R/W	64h	Reserved

14.5.1.2.480 EMIF_CTLCFG_DENALI_PI_6 Register

1 EMIF_CTLCFG_DENALI_PI_6 Register (Offset = 2018h) [reset = 0h]

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Table 14-13795. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A018h**

Figure 14-4559. EMIF_CTLCFG_DENALI_PI_6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_DFI_PHYMSTR_STATE_SEL_R
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_DFI_PHYMSTR_CS_STATE_R
NONE							R/W
0h							0h

Table 14-13797. EMIF_CTLCFG_DENALI_PI_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PI_DFI_PHYMSTR_STATE_SEL_R	R/W	0h	DFI PHY Controller State Select: Indication from the PHY to the MC whether the requested memory state is IDLE or Self refresh. 'b0: indicates that the corresponding CS must be put into the IDLE state. 'b1: indicates that the corresponding CS must be put into the Self refresh state. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_DFI_PHYMSTR_CS_STATE_R	R/W	0h	This signal indicates the state of the DRAM when the PHY becomes the controller. 'b0: The PHY specifies the required state, using the dfi_phymstr_state_sel signal. 'b1: is reserved. Reset Source: ctl_amod_g_rst_n

14.5.1.2.481 EMIF_CTLCFG_DENALI_PI_7 Register

1 EMIF_CTLCFG_DENALI_PI_7 Register (Offset = 201Ch) [reset = 0h]

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Table 14-13798. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A01Ch**

Figure 14-4560. EMIF_CTLCFG_DENALI_PI_7 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_PHYMSTR_MAX							
R							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_PHYMSTR_MAX							
R							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_PHYMSTR_MAX							
R							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_PHYMSTR_MAX							
R							
0h							

Table 14-13800. EMIF_CTLCFG_DENALI_PI_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_PHYMSTR_MAX	R	0h	Indicates the maximum number of DFI clock cycles registered while the dfi_phymstr_req signal is asserted and the dfi_phymstr_ack signal is asserted. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.482 EMIF_CTLCFG_DENALI_PI_8 Register

1 EMIF_CTLCFG_DENALI_PI_8 Register (Offset = 2020h) [reset = 0h]

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Table 14-13801. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A020h

Figure 14-4561. EMIF_CTLCFG_DENALI_PI_8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_TDFI_PHYMSTR_RESP			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_PHYMSTR_RESP							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_PHYMSTR_RESP							
R							
0h							

Table 14-13803. EMIF_CTLCFG_DENALI_PI_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TDFI_PHYMSTR_RESP	R	0h	Indicates the maximum number of DFI clock cycles registered between a dfi_phymstr_req signal assertion and a dfi_phymstr_ack signal assertion. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.483 EMIF_CTLCFG_DENALI_PI_9 Register

1 EMIF_CTLCFG_DENALI_PI_9 Register (Offset = 2024h) [reset = 0h]

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Table 14-13804. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A024h**

Figure 14-4562. EMIF_CTLCFG_DENALI_PI_9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TDFI_PHYUPD_RESP</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_PHYUPD_RESP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_PHYUPD_RESP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13806. EMIF_CTLCFG_DENALI_PI_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TDFI_PHYUPD_RESP	R	0h	Indicates the maximum number of DFI clock cycles registered between a dfi_phyupd_req signal assertion and a dfi_phyupd_ack signal assertion. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.484 EMIF_CTLCFG_DENALI_PI_10 Register

1 EMIF_CTLCFG_DENALI_PI_10 Register (Offset = 2028h) [reset = 0h]

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Table 14-13807. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A028h**

Figure 14-4563. EMIF_CTLCFG_DENALI_PI_10 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_PHYUPD_MAX							
R							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_PHYUPD_MAX							
R							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_PHYUPD_MAX							
R							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_PHYUPD_MAX							
R							
0h							

Table 14-13809. EMIF_CTLCFG_DENALI_PI_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_PHYUPD_MAX	R	0h	Indicates the maximum number of DFI clock cycles registered while the dfi_phyupd_req signal is asserted and the dfi_phy_ack signal is asserted. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.485 EMIF_CTLCFG_DENALI_PI_11 Register

1 EMIF_CTLCFG_DENALI_PI_11 Register (Offset = 202Ch) [reset = 0h]

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Table 14-13810. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A02Ch

Figure 14-4564. EMIF_CTLCFG_DENALI_PI_11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_INIT_DFS_CALVL_ONLY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED			PI_INIT_WORK_FREQ				
NONE			R/W				
0h			0h				

Table 14-13812. EMIF_CTLCFG_DENALI_PI_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PI_INIT_DFS_CALVL_ONLY	R/W	0h	Enables frequency training for CA leveling only. Other trainings are not performed. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_INIT_WORK_FREQ	R/W	0h	Indicates the initial work frequency after initialization and initial leveling sequence. Reset Source: ctl_amod_g_rst_n

14.5.1.2.486 EMIF_CTLCFG_DENALI_PI_12 Register

1 EMIF_CTLCFG_DENALI_PI_12 Register (Offset = 2030h) [reset = 0h]

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Table 14-13813. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A030h**

Figure 14-4565. EMIF_CTLCFG_DENALI_PI_12 Name Register

31	30	29	28	27	26	25	24
PI_FREQ_MAP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_FREQ_MAP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_FREQ_MAP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_FREQ_MAP							
R/W							
0h							

Table 14-13815. EMIF_CTLCFG_DENALI_PI_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_FREQ_MAP	R/W	0h	Frequency map for supported working frequencies. Each bit represents one supported frequency. Reset Source: ctl_amod_g_rst_n

14.5.1.2.487 EMIF_CTLCFG_DENALI_PI_13 Register

1 EMIF_CTLCFG_DENALI_PI_13 Register (Offset = 2034h) [reset = 30001h]

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Table 14-13816. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 A034h**

Figure 14-4566. EMIF_CTLCFG_DENALI_PI_13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_SWLVL_CS_SEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_CS_MAP</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RESERVED1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_SW_RST_N</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
</table>

Table 14-13818. EMIF_CTLCFG_DENALI_PI_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_CS_SEL	R/W	0h	Defines which chip selects are active in swlvl, 0 for binary, 1 for one-hot. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_CS_MAP	R/W	3h	Defines which chip selects are active. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED1	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_SW_RST_N	R/W	1h	User request to reset the whole PI except the parameter modules. Set 0 to reset, set to 1 to release. Reset Source: ctl_amod_g_rst_n

14.5.1.2.488 EMIF_CTLCFG_DENALI_PI_14 Register

1 EMIF_CTLCFG_DENALI_PI_14 Register (Offset = 2038h) [reset = 0h]

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Table 14-13819. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A038h**

Figure 14-4567. EMIF_CTLCFG_DENALI_PI_14 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TMRR			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_SRX_LVL_TARGET_CS_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PI_RANK_NUM_PER_CKE				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_CS_MASK	
NONE						R/W	
0h						0h	

Table 14-13821. EMIF_CTLCFG_DENALI_PI_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_TMRR	R/W	0h	DRAM tMRR value in memory clock cycles. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SRX_LVL_TARGET_CS_EN	R/W	0h	Defines self refresh exit trigger target rank/ranks training or all ranks training. 1: The rank/ranks exit from self refresh will trigger the corresponding rank/ranks training. Note: If multiple ranks exit from self refresh, current design only support the multiple ranks srx command issues at the same time. 0: Any rank/ranks exit from self refresh will trigger all ranks training Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_RANK_NUM_PER_CKE	R/W	0h	Defines the number of chip selects share one cke Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_CS_MASK	R/W	0h	Defines which chip selects are active. Reset Source: ctl_amod_g_rst_n

14.5.1.2.489 EMIF_CTLCFG_DENALI_PI_15 Register

1 EMIF_CTLCFG_DENALI_PI_15 Register (Offset = 203Ch) [reset = 0h]

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Table 14-13822. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A03Ch

Figure 14-4568. EMIF_CTLCFG_DENALI_PI_15 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_MCAREF_FORWARD_ONLY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED					PI_VRCG_EN		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				PI_TMPRR			
NONE				R/W			
0h				0h			

Table 14-13824. EMIF_CTLCFG_DENALI_PI_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED2	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_MCAREF_FORWARD_ONLY	R/W	0h	Controls the generation of AREF from the PI module or forward the MC received value. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PI_VRCG_EN	R/W	0h	Whether enable VRCG mode in two cases: bit0 - when DFS. bit1-when setting DQ Vref. bit2-when setting CBT. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_TMPRR	R/W	0h	DRAM tMPRR value in memory clock cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.490 EMIF_CTLCFG_DENALI_PI_16 Register

1 EMIF_CTLCFG_DENALI_PI_16 Register (Offset = 2040h) [reset = 0h]

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Table 14-13825. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A040h**

Figure 14-4569. EMIF_CTLCFG_DENALI_PI_16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_ON_DFIBUS</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TREF_INTERVAL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TREF_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TREF_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13827. EMIF_CTLCFG_DENALI_PI_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_ON_DFIBUS	R	0h	Monitors the state of the PI controlling the DFI bus. 1 means PI is in control. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	PI_TREF_INTERVAL	R/W	0h	Defines the cycles between refreshes to different chip selects. Reset Source: ctl_amod_g_rst_n

14.5.1.2.491 EMIF_CTLCFG_DENALI_PI_17 Register

1 EMIF_CTLCFG_DENALI_PI_17 Register (Offset = 2044h) [reset = 0h]

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Table 14-13828. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A044h**

Figure 14-4570. EMIF_CTLCFG_DENALI_PI_17 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SW_WRLVL_RESP_0
NONE							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_SWLVL_OP_DONE
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_LOAD
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_DATA_RETENTION
NONE							R
0h							0h

Table 14-13830. EMIF_CTLCFG_DENALI_PI_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SW_WRLVL_RESP_0	R	0h	Write leveling response for data slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SWLVL_OP_DONE	R	0h	Reports the status of the software leveling operation. Value of 1 indicates operation complete. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_LOAD	W	0h	User request to load delays and execute software leveling. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_DATA_RETENTION	R	0h	Monitors the readiness for the PHY to be put into data retention mode after pi_sref_entry req parameter has been written. 1 means ready for data retention. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.492 EMIF_CTLCFG_DENALI_PI_18 Register

1 EMIF_CTLCFG_DENALI_PI_18 Register (Offset = 2048h) [reset = 0h]

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Table 14-13831. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A048h**

Figure 14-4571. EMIF_CTLCFG_DENALI_PI_18 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_SW_CALVL_RESP_0	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_SW_RDLVL_RESP_1	
NONE						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_SW_RDLVL_RESP_0	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_SW_WRLVL_RESP_1
NONE							R
0h							0h

Table 14-13833. EMIF_CTLCFG_DENALI_PI_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_SW_CALVL_RESP_0	R	0h	CA leveling response for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SW_RDLVL_RESP_1	R	0h	Read leveling response for data slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_SW_RDLVL_RESP_0	R	0h	Read leveling response for data slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SW_WRLVL_RESP_1	R	0h	Write leveling response for data slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.493 EMIF_CTLCFG_DENALI_PI_19 Register

1 EMIF_CTLCFG_DENALI_PI_19 Register (Offset = 204Ch) [reset = 0h]

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Table 14-13834. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A04Ch**

Figure 14-4572. EMIF_CTLCFG_DENALI_PI_19 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_0
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_SWLVL_EXIT
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_START
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					PI_SW_LEVELING_MODE		
NONE					R/W		
0h					0h		

Table 14-13836. EMIF_CTLCFG_DENALI_PI_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_WR_SLICE_0	W	0h	SW leveling write command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SWLVL_EXIT	W	0h	User request to exit software leveling. Set to 1 to exit. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_START	W	0h	User request to initiate software leveling of type in the SW_LEVELING_MODE parameter. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_SW_LEVELING_MODE	R/W	0h	Defines the leveling operation for software leveling. Set to 'b111 for DDR4 VREF training, set to b001 for write leveling, set to b010 for read data eye training, or set to b011 for read gate training, set to b100 for ca training, set to b101 for wdq training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.494 EMIF_CTLCFG_DENALI_PI_20 Register

1 EMIF_CTLCFG_DENALI_PI_20 Register (Offset = 2050h) [reset = 0h]

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Table 14-13837. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A050h

Figure 14-4573. EMIF_CTLCFG_DENALI_PI_20 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_1
NONE							W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_SW_WDQLVL_RESP_0	
NONE						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_0
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_SWLVL_RD_SLICE_0
NONE							W
0h							0h

Table 14-13839. EMIF_CTLCFG_DENALI_PI_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_WR_SLICE_1	W	0h	SW leveling write command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SW_WDQLVL_RESP_0	R	0h	Leveling response for data slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_VREF_UPDATE_SLICE_0	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SWLVL_RD_SLICE_0	W	0h	SW leveling read command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.495 EMIF_CTLCFG_DENALI_PI_21 Register

1 EMIF_CTLCFG_DENALI_PI_21 Register (Offset = 2054h) [reset = 0h]

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Table 14-13840. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A054h

Figure 14-4574. EMIF_CTLCFG_DENALI_PI_21 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_SM2_START
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PI_SW_WDQLVL_RESP_1	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_1
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_RD_SLICE_1
NONE							W
0h							0h

Table 14-13842. EMIF_CTLCFG_DENALI_PI_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SWLVL_SM2_START	W	0h	SW leveling start command for stage 2. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_SW_WDQLVL_RESP_1	R	0h	Leveling response for data slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_VREF_UPDATE_SLICE_1	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SWLVL_RD_SLICE_1	W	0h	SW leveling read command in WDQ training. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.496 EMIF_CTLCFG_DENALI_PI_22 Register

1 EMIF_CTLCFG_DENALI_PI_22 Register (Offset = 2058h) [reset = 0h]

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Table 14-13843. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A058h**

Figure 14-4575. EMIF_CTLCFG_DENALI_PI_22 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_DFS_PERIOD_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_SEQUENTIAL_LVL_REQ
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_SM2_RD
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_SM2_WR
NONE							W
0h							0h

Table 14-13845. EMIF_CTLCFG_DENALI_PI_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_DFS_PERIOD_EN	R/W	0h	Enable the DFS triggered periodic leveling. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SEQUENTIAL_LVL_REQ	W	0h	User request to initiate all possible leveling sequences. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_SWLVL_SM2_RD	W	0h	SW leveling read command for stage 2. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SWLVL_SM2_WR	W	0h	SW leveling write command for stage 2. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.497 EMIF_CTLCFG_DENALI_PI_23 Register

1 EMIF_CTLCFG_DENALI_PI_23 Register (Offset = 205Ch) [reset = 0h]

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Table 14-13846. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A05Ch

Figure 14-4576. EMIF_CTLCFG_DENALI_PI_23 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WRLVL_REQ
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_DFI40_POLARITY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_MPD_PERIOD_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_SRE_PERIOD_EN
NONE							R/W
0h							0h

Table 14-13848. EMIF_CTLCFG_DENALI_PI_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WRLVL_REQ	W	0h	User request to initiate write leveling. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DFI40_POLARITY	R/W	0h	Defines the polarity of the dfi_wrdata_cs_n/dfi_rddata_cs_n signals. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_MPD_PERIOD_EN	R/W	0h	Enable the max power saving mode exit triggered periodic leveling. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_SRE_PERIOD_EN	R/W	0h	Enable the self refresh exit triggered periodic leveling. Reset Source: ctl_amod_g_rst_n

14.5.1.2.498 EMIF_CTLCFG_DENALI_PI_24 Register

1 EMIF_CTLCFG_DENALI_PI_24 Register (Offset = 2060h) [reset = 0h]

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Table 14-13849. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A060h**

Figure 14-4577. EMIF_CTLCFG_DENALI_PI_24 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_WLMRD					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		PI_WLDQSEN					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED							PI_WRLVL_CS
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						PI_WRLVL_CS_SW	
NONE						R/W	
0h						0h	

Table 14-13851. EMIF_CTLCFG_DENALI_PI_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_WLMRD	R/W	0h	Delay from issuing MRS to first write leveling strobe. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_WLDQSEN	R/W	0h	Delay from issuing MRS to first DQS strobe for write leveling. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WRLVL_CS	R/W	0h	Specifies the target chip select for the write leveling operation initiated through the WRLVL_REQ parameter. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_WRLVL_CS_SW	R/W	0h	Specifies the target chip select for the write leveling operation initiated through the WRLVL_REQ parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.499 EMIF_CTLCFG_DENALI_PI_25 Register

1 EMIF_CTLCFG_DENALI_PI_25 Register (Offset = 2064h) [reset = 0h]

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Table 14-13852. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A064h**

Figure 14-4578. EMIF_CTLCFG_DENALI_PI_25 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WRLVL_DISABLE_DFS
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_WRLVL_ON_SREF_EXIT
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_WRLVL_INTERVAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_WRLVL_INTERVAL							
R/W							
0h							

Table 14-13854. EMIF_CTLCFG_DENALI_PI_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WRLVL_DISABLE_DFS	R/W	0h	Disable automatic write leveling on freq change. Set to 1 to disable wrlvl on dfs,set 0 enable wrlvl on dfs. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_WRLVL_ON_SREF_EXIT	R/W	0h	Enables automatic write leveling on a self-refresh exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:0	PI_WRLVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic write leveling commands. Reset Source: ctl_amod_g_rst_n

14.5.1.2.500 EMIF_CTLCFG_DENALI_PI_26 Register

1 EMIF_CTLCFG_DENALI_PI_26 Register (Offset = 2068h) [reset = 0h]

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Table 14-13855. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A068h**

Figure 14-4579. EMIF_CTLCFG_DENALI_PI_26 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WRLVL_ON_MPD_EXIT
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_WRLVL_CS_MAP	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_WRLVL_ROTATE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_WRLVL_RESP_MASK	
NONE						R/W	
0h						0h	

Table 14-13857. EMIF_CTLCFG_DENALI_PI_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WRLVL_ON_MPD_EXIT	R/W	0h	Enables automatic write leveling on a maximum power down mode exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_WRLVL_CS_MAP	R/W	0h	Defines the chip select map for write leveling operations. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable chip for write leveling. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WRLVL_ROTATE	R/W	0h	Enables rotational CS for counter triggered automatic write leveling. Set to 1, only one rank's write levling will process, the rank number is rotational for each time that write leveling been triggered by counter expiring. Set to 0 or not a short pattern leveling [indicated by dfi_lvl_periodic], the counter expired write leveling will process all the ranks. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-13857. EMIF_CTLCFG_DENALI_PI_26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PI_WRLVL_RESP_MASK	R/W	0h	Mask for the dfi_wrlvl_resp signal during write leveling. Reset Source: ctl_amod_g_rst_n

14.5.1.2.501 EMIF_CTLCFG_DENALI_PI_27 Register

1 EMIF_CTLCFG_DENALI_PI_27 Register (Offset = 206Ch) [reset = 0h]

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Table 14-13858. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A06Ch**

Figure 14-4580. EMIF_CTLCFG_DENALI_PI_27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WRLVL_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PI_WRLVL_ERROR_STATUS
NONE							R
0h							0h

Table 14-13860. EMIF_CTLCFG_DENALI_PI_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TDFI_WRLVL_EN	R/W	0h	Defines the DFI tWRLVL_EN timing parameter [in DFI clocks], the minimum cycles from a dfi_wrlvl_en assertion to the first dfi_wrlvl_strobe assertion. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WRLVL_ERROR_STATUS	R	0h	Holds the error associated with the write level error interrupt. Bit [0] set indicates a TDFI_WRLVL_MAX parameter violation and bit [1] set indicates a TDFI_WRLVL_RESP parameter violation. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.502 EMIF_CTLCFG_DENALI_PI_28 Register

1 EMIF_CTLCFG_DENALI_PI_28 Register (Offset = 2070h) [reset = 0h]

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Table 14-13861. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A070h**

Figure 14-4581. EMIF_CTLCFG_DENALI_PI_28 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_WRLVL_RESP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WRLVL_RESP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WRLVL_RESP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WRLVL_RESP							
R/W							
0h							

Table 14-13863. EMIF_CTLCFG_DENALI_PI_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_WRLVL_RESP	R/W	0h	Defines the DFI tWRLVL_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_wrlvl_req assertion and a dfi_wrlvl_en assertion. Reset Source: ctl_amod_g_rst_n

14.5.1.2.503 EMIF_CTLCFG_DENALI_PI_29 Register

1 EMIF_CTLCFG_DENALI_PI_29 Register (Offset = 2074h) [reset = 0h]

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Table 14-13864. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A074h**

Figure 14-4582. EMIF_CTLCFG_DENALI_PI_29 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_WRLVL_MAX							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WRLVL_MAX							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WRLVL_MAX							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WRLVL_MAX							
R/W							
0h							

Table 14-13866. EMIF_CTLCFG_DENALI_PI_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_WRLVL_MAX	R/W	0h	Defines the DFI tWRLVL_MAX timing parameter [in DFI clocks], the maximum cycles between a dfi_wrlvl_en assertion and a valid dfi_wrlvl_resp. Reset Source: ctl_amod_g_rst_n

14.5.1.2.504 EMIF_CTLCFG_DENALI_PI_30 Register

1 EMIF_CTLCFG_DENALI_PI_30 Register (Offset = 2078h) [reset = 0h]

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Table 14-13867. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A078h

Figure 14-4583. EMIF_CTLCFG_DENALI_PI_30 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_ODT_VALUE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TODTH_RD</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TODTH_WR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_WRLVL_STROBE_NUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-13869. EMIF_CTLCFG_DENALI_PI_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_ODT_VALUE	R/W	0h	When using LPDDR4, this value will be driven out on the dfi_odt signal. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_TODTH_RD	R/W	0h	Defines the minimum DRAM cycles of ODT high time for a read command, in memory clocks. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TODTH_WR	R/W	0h	Defines the minimum DRAM cycles of ODT high time for a write command, in memory clocks. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_WRLVL_STROBE_NUM	R/W	0h	Defines the number of write leveling strobes generated. Reset Source: ctl_amod_g_rst_n

14.5.1.2.505 EMIF_CTLCFG_DENALI_PI_31 Register

1 EMIF_CTLCFG_DENALI_PI_31 Register (Offset = 207Ch) [reset = 0h]

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Table 14-13870. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A07Ch**

Figure 14-4584. EMIF_CTLCFG_DENALI_PI_31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_ADDRESS_MIRRORING	
NONE						R/W	
0h						0h	

Table 14-13872. EMIF_CTLCFG_DENALI_PI_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_ADDRESS_MIRRORING	R/W	0h	Indicates which chip selects support address mirroring. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.506 EMIF_CTLCFG_DENALI_PI_32 Register

1 EMIF_CTLCFG_DENALI_PI_32 Register (Offset = 2080h) [reset = 0h]

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Table 14-13873. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A080h**

Figure 14-4585. EMIF_CTLCFG_DENALI_PI_32 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_CA_PARITY_ERROR_INJECT	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_CA_PARITY_ERROR_INJECT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_CA_PARITY_ERROR_INJECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_CA_PARITY_ERROR_INJECT							
R/W							
0h							

Table 14-13875. EMIF_CTLCFG_DENALI_PI_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:0	PI_CA_PARITY_ERROR_INJECT	R/W	0h	Selects bit to corrupt on the CA bus for CA parity error injection. Reset Source: ctl_amod_g_rst_n

14.5.1.2.507 EMIF_CTLCFG_DENALI_PI_33 Register

1 EMIF_CTLCFG_DENALI_PI_33 Register (Offset = 2084h) [reset = 0h]

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Table 14-13876. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A084h

Figure 14-4586. EMIF_CTLCFG_DENALI_PI_33 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RDLVL_GATE_REQ
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RDLVL_REQ
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED4			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED					PI_RESERVED3		
NONE					R/W		
0h					0h		

Table 14-13878. EMIF_CTLCFG_DENALI_PI_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RDLVL_GATE_REQ	W	0h	User request to initiate gate training. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RDLVL_REQ	W	0h	User request to initiate data eye training. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED4	R/W	0h	Reserved
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_RESERVED3	R/W	0h	Reserved

14.5.1.2.508 EMIF_CTLCFG_DENALI_PI_34 Register

1 EMIF_CTLCFG_DENALI_PI_34 Register (Offset = 2088h) [reset = 0h]

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Table 14-13879. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A088h

Figure 14-4587. EMIF_CTLCFG_DENALI_PI_34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_RDLVL_CS
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_RDLVL_CS_SW	
NONE						R/W	
0h						0h	

Table 14-13881. EMIF_CTLCFG_DENALI_PI_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PI_RDLVL_CS	R/W	0h	Specifies the target chip select for the data eye training operation initiated through the RDLVL_REQ parameter or the gate training operation initiated through the RDLVL_GATE_REQ parameter. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_CS_SW	R/W	0h	Specifies the target chip select for the data eye training operation initiated through the RDLVL_REQ parameter or the gate training operation initiated through the RDLVL_GATE_REQ parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.509 EMIF_CTLCFG_DENALI_PI_35 Register

1 EMIF_CTLCFG_DENALI_PI_35 Register (Offset = 208Ch) [reset = 0h]

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Table 14-13882. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A08Ch**

Figure 14-4588. EMIF_CTLCFG_DENALI_PI_35 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_0							
R/W							
0h							

Table 14-13884. EMIF_CTLCFG_DENALI_PI_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_0	R/W	0h	Non-default pattern 0 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.510 EMIF_CTLCFG_DENALI_PI_36 Register

1 EMIF_CTLCFG_DENALI_PI_36 Register (Offset = 2090h) [reset = 0h]

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Table 14-13885. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A090h**

Figure 14-4589. EMIF_CTLCFG_DENALI_PI_36 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_1							
R/W							
0h							

Table 14-13887. EMIF_CTLCFG_DENALI_PI_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_1	R/W	0h	Non-default pattern 1 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.511 EMIF_CTLCFG_DENALI_PI_37 Register

1 EMIF_CTLCFG_DENALI_PI_37 Register (Offset = 2094h) [reset = 0h]

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Table 14-13888. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A094h**

Figure 14-4590. EMIF_CTLCFG_DENALI_PI_37 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_2							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_2							
R/W							
0h							

Table 14-13890. EMIF_CTLCFG_DENALI_PI_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_2	R/W	0h	Non-default pattern 2 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.512 EMIF_CTLCFG_DENALI_PI_38 Register

1 EMIF_CTLCFG_DENALI_PI_38 Register (Offset = 2098h) [reset = 0h]

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Table 14-13891. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A098h**

Figure 14-4591. EMIF_CTLCFG_DENALI_PI_38 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_3							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_3							
R/W							
0h							

Table 14-13893. EMIF_CTLCFG_DENALI_PI_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_3	R/W	0h	Non-default pattern 3 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.513 EMIF_CTLCFG_DENALI_PI_39 Register

1 EMIF_CTLCFG_DENALI_PI_39 Register (Offset = 209Ch) [reset = 0h]

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Table 14-13894. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A09Ch**

Figure 14-4592. EMIF_CTLCFG_DENALI_PI_39 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_4							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_4							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_4							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_4							
R/W							
0h							

Table 14-13896. EMIF_CTLCFG_DENALI_PI_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_4	R/W	0h	Non-default pattern 4 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.514 EMIF_CTLCFG_DENALI_PI_40 Register

1 EMIF_CTLCFG_DENALI_PI_40 Register (Offset = 20A0h) [reset = 0h]

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Table 14-13897. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0A0h**

Figure 14-4593. EMIF_CTLCFG_DENALI_PI_40 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_5							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_5							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_5							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_5							
R/W							
0h							

Table 14-13899. EMIF_CTLCFG_DENALI_PI_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_5	R/W	0h	Non-default pattern 5 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.515 EMIF_CTLCFG_DENALI_PI_41 Register

1 EMIF_CTLCFG_DENALI_PI_41 Register (Offset = 20A4h) [reset = 0h]

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Table 14-13900. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0A4h**

Figure 14-4594. EMIF_CTLCFG_DENALI_PI_41 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_RDLVL_PAT_6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_RDLVL_PAT_6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_RDLVL_PAT_6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_RDLVL_PAT_6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13902. EMIF_CTLCFG_DENALI_PI_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_6	R/W	0h	Non-default pattern 6 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.516 EMIF_CTLCFG_DENALI_PI_42 Register

1 EMIF_CTLCFG_DENALI_PI_42 Register (Offset = 20A8h) [reset = 0h]

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Table 14-13903. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0A8h

Figure 14-4595. EMIF_CTLCFG_DENALI_PI_42 Name Register

31	30	29	28	27	26	25	24
PI_RDLVL_PAT_7							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_RDLVL_PAT_7							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLVL_PAT_7							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_PAT_7							
R/W							
0h							

Table 14-13905. EMIF_CTLCFG_DENALI_PI_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_RDLVL_PAT_7	R/W	0h	Non-default pattern 7 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.517 EMIF_CTLCFG_DENALI_PI_43 Register

1 EMIF_CTLCFG_DENALI_PI_43 Register (Offset = 20ACh) [reset = 0h]

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Table 14-13906. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0ACh**

Figure 14-4596. EMIF_CTLCFG_DENALI_PI_43 Name Register

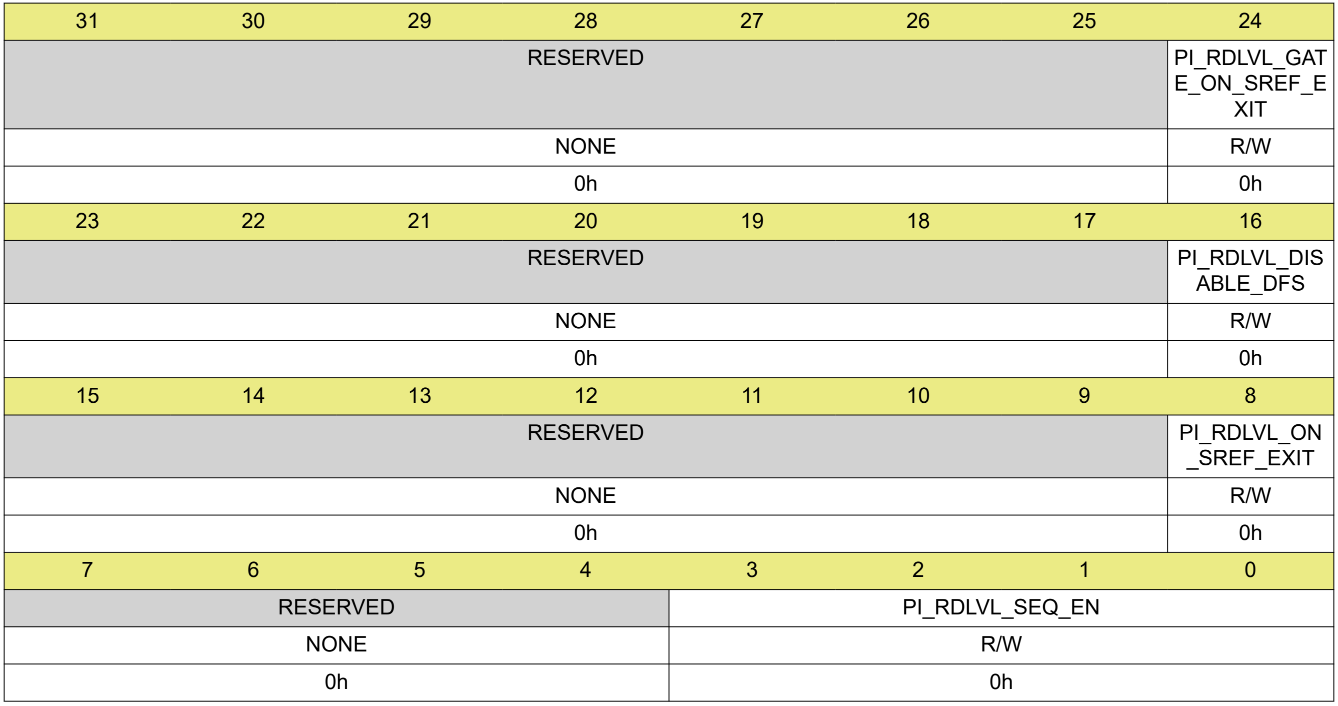

31	30	29	28	27	26	25	24
RESERVED							PI_RDLVL_GATE_ON_SREF_EXIT
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RDLVL_DISABLE_DFS
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RDLVL_ON_SREF_EXIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PI_RDLVL_SEQ_EN			
NONE				R/W			
0h				0h			

Table 14-13908. EMIF_CTLCFG_DENALI_PI_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RDLVL_GATE_ON_SREF_EXIT	R/W	0h	Enables automatic gate training on a self-refresh exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RDLVL_DISABLE_DFS	R/W	0h	Disables automatic data eye training on freq change. Set to 1 to disable rdlvl on dfs,Set to 0 to enable rdlvl on dfs. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RDLVL_ON_SREF_EXIT	R/W	0h	Enables automatic data eye training on a self-refresh exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RDLVL_SEQ_EN	R/W	0h	Specifies the pattern, format and MPR for data eye training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.518 EMIF_CTLCFG_DENALI_PI_44 Register

1 EMIF_CTLCFG_DENALI_PI_44 Register (Offset = 20B0h) [reset = 0h]

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Table 14-13909. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0B0h**

Figure 14-4597. EMIF_CTLCFG_DENALI_PI_44 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RDLVL_ROTATE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RDLVL_GATE_ON_MPD_EXIT
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RDLVL_ON_MPD_EXIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RDLVL_GATE_DISABLE_DFS
NONE							R/W
0h							0h

Table 14-13911. EMIF_CTLCFG_DENALI_PI_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RDLVL_ROTATE	R/W	0h	Enables rotational CS for interval data eye training. Set to 1 for rotating CS. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RDLVL_GATE_ON_MPD_EXIT	R/W	0h	Enables automatic gate training on a maximum power down mode exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RDLVL_ON_MPD_EXIT	R/W	0h	Enables automatic data eye training on a maximum power down mode exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-13911. EMIF_CTLCFG_DENALI_PI_44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PI_RDLVL_GATE_DISABLE_DFS	R/W	0h	Disables automatic gate training on freq change. Set to 1 to disable rdlvl_gate on dfs,Set to 0 to enable rdlvl_gate on dfs. Reset Source: ctl_amod_g_rst_n

14.5.1.2.519 EMIF_CTLCFG_DENALI_PI_45 Register

1 EMIF_CTLCFG_DENALI_PI_45 Register (Offset = 20B4h) [reset = 0h]

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Table 14-13912. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0B4h**

Figure 14-4598. EMIF_CTLCFG_DENALI_PI_45 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_GATE_CS_MAP	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_CS_MAP	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PI_RDLVL_GATE_ROTATE
NONE							R/W
0h							0h

Table 14-13914. EMIF_CTLCFG_DENALI_PI_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_GATE_CS_MAP	R/W	0h	Defines the chip select map for gate training operations. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable chip for gate training. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_CS_MAP	R/W	0h	Defines the chip select map for data eye training operations. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable chip for data eye training. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_RDLVL_GATE_ROTATE	R/W	0h	Enables rotational CS for interval gate training. Set to 1 for rotating CS. Reset Source: ctl_amod_g_rst_n

14.5.1.2.520 EMIF_CTLCFG_DENALI_PI_46 Register

1 EMIF_CTLCFG_DENALI_PI_46 Register (Offset = 20B8h) [reset = 0h]

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Table 14-13915. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0B8h**

Figure 14-4599. EMIF_CTLCFG_DENALI_PI_46 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_RDLVL_RR</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_RDLVL_RR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13917. EMIF_CTLCFG_DENALI_PI_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_RDLVL_RR	R/W	0h	Defines the DFI tRDLVL_RR timing parameter [in DFI clocks], the minimum cycles between read commands. Reset Source: ctl_amod_g_rst_n

14.5.1.2.521 EMIF_CTLCFG_DENALI_PI_47 Register

1 EMIF_CTLCFG_DENALI_PI_47 Register (Offset = 20BCh) [reset = 0h]

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Table 14-13918. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0BCh

Figure 14-4600. EMIF_CTLCFG_DENALI_PI_47 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_RDLVL_RESP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_RDLVL_RESP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_RDLVL_RESP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_RDLVL_RESP							
R/W							
0h							

Table 14-13920. EMIF_CTLCFG_DENALI_PI_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_RDLVL_RESP	R/W	0h	Defines the DFI tRDLVL_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_rdlvl_req or dfi_rdlvl_gate_req assertion and a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion. Reset Source: ctl_amod_g_rst_n

14.5.1.2.522 EMIF_CTLCFG_DENALI_PI_48 Register

1 EMIF_CTLCFG_DENALI_PI_48 Register (Offset = 20C0h) [reset = 0h]

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Table 14-13921. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0C0h**

Figure 14-4601. EMIF_CTLCFG_DENALI_PI_48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_RDLVL_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_RESP_MASK	
NONE						R/W	
0h						0h	

Table 14-13923. EMIF_CTLCFG_DENALI_PI_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TDFI_RDLVL_EN	R/W	0h	Defines the DFI tRDLVL_EN timing parameter [in DFI clocks], the minimum cycles from a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion to the first read or MRR. Set to 1 means the minium value[1 cycle], set to 0 means the maxium value Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_RESP_MASK	R/W	0h	Mask for the dfi_rdlvl_resp signal during data eye training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.523 EMIF_CTLCFG_DENALI_PI_49 Register

1 EMIF_CTLCFG_DENALI_PI_49 Register (Offset = 20C4h) [reset = 0h]

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Table 14-13924. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0C4h**

Figure 14-4602. EMIF_CTLCFG_DENALI_PI_49 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TDFI_RDLVL_MAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TDFI_RDLVL_MAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_RDLVL_MAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_RDLVL_MAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13926. EMIF_CTLCFG_DENALI_PI_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_RDLVL_MAX	R/W	0h	Defines the DFI tRDLVL_MAX timing parameter [in DFI clocks], the maximum cycles between a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion and a valid dfi_rdlvl_resp. Reset Source: ctl_amod_g_rst_n

14.5.1.2.524 EMIF_CTLCFG_DENALI_PI_50 Register

1 EMIF_CTLCFG_DENALI_PI_50 Register (Offset = 20C8h) [reset = 0h]

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Table 14-13927. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0C8h**

Figure 14-4603. EMIF_CTLCFG_DENALI_PI_50 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_RDLVL_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_RDLVL_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RDLVL_ERROR_STATUS</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13929. EMIF_CTLCFG_DENALI_PI_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	PI_RDLVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic data eye training commands. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_RDLVL_ERROR_STATUS	R	0h	Holds the error associated with the data eye training error or gate training error interrupt. Uppermost bit set indicates a TDFI_RDLVL_RESP parameter violation. Next uppermost bit set indicates a TDFI_RDLVL_MAX parameter violation. Lower bits are reserved. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.525 EMIF_CTLCFG_DENALI_PI_51 Register

1 EMIF_CTLCFG_DENALI_PI_51 Register (Offset = 20CCh) [reset = 0h]

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Table 14-13930. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0CCh

Figure 14-4604. EMIF_CTLCFG_DENALI_PI_51 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RDLVL_PATTERN_NUM			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_RDLVL_PATTERN_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_RDLVL_GATE_INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLVL_GATE_INTERVAL							
R/W							
0h							

Table 14-13932. EMIF_CTLCFG_DENALI_PI_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RDLVL_PATTERN_NUM	R/W	0h	Defines the number of pattern supported in read leveling. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RDLVL_PATTERN_START	R/W	0h	Defines the start pattern in read leveling. Reset Source: ctl_amod_g_rst_n
15:0	PI_RDLVL_GATE_INTERVAL	R/W	0h	Number of long count sequences counted between automatic gate training commands. Reset Source: ctl_amod_g_rst_n

14.5.1.2.526 EMIF_CTLCFG_DENALI_PI_52 Register

1 EMIF_CTLCFG_DENALI_PI_52 Register (Offset = 20D0h) [reset = 0h]

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Table 14-13933. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0D0h

Figure 14-4605. EMIF_CTLCFG_DENALI_PI_52 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_REG_DIMM_ENABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RD_PREAMBLE_TRAINING_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_RDLVL_GATE_STROBE_NUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_RDLVL_STROBE_NUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-13935. EMIF_CTLCFG_DENALI_PI_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_REG_DIMM_ENABLE	R/W	0h	Enable registered DIMM operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_RD_PREAMBLE_TRAINING_EN	R/W	0h	Enable read preamble training during gate training. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_RDLVL_GATE_STROBE_NUM	R/W	0h	Defines the number of back to back MPC command in one read process in read gate training. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_RDLVL_STROBE_NUM	R/W	0h	Defines the number of back to back MPC command in one read process in read eye training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.527 EMIF_CTLCFG_DENALI_PI_53 Register

1 EMIF_CTLCFG_DENALI_PI_53 Register (Offset = 20D4h) [reset = 0h]

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Table 14-13936. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0D4h

Figure 14-4606. EMIF_CTLCFG_DENALI_PI_53 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_CALVL_CS_SW	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_CALVL_REQ
NONE							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_PHY_WRLAT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_RDDATA_EN							
R							
0h							

Table 14-13938. EMIF_CTLCFG_DENALI_PI_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_CALVL_CS_SW	R/W	0h	Specifies the target chip select for the CA training operation initiated through the CALVL_REQ parameter. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_CALVL_REQ	W	0h	User request to initiate CA training. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PI_TDFI_PHY_WRLAT	R	0h	Holds the calculated DFI tPHY_WRLAT timing parameter [in DFI PHY clocks], the maximum cycles between a write command and a dfi_wrdata_en assertion. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PI_TDFI_RDDATA_EN	R	0h	Holds the calculated DFI tRDDATA_EN timing parameter [in DFI PHY clocks], the maximum cycles between a read command and a dfi_rddata_en assertion. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.528 EMIF_CTLCFG_DENALI_PI_54 Register

1 EMIF_CTLCFG_DENALI_PI_54 Register (Offset = 20D8h) [reset = 0h]

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Table 14-13939. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0D8h**

Figure 14-4607. EMIF_CTLCFG_DENALI_PI_54 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_CALVL_SEQ_EN	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_RESERVED6			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_RESERVED5
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_CALVL_CS
NONE							R/W
0h							0h

Table 14-13941. EMIF_CTLCFG_DENALI_PI_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_CALVL_SEQ_EN	R/W	0h	Specifies which CA training patterns will be used. Set to 0 for pattern 0 only, set to 1 for patterns 0 and 1, set to 2 for patterns 0, 1 and 2, or set to 3 for all patterns. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED6	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED5	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_CALVL_CS	R/W	0h	Specifies the target chip select for the CA training operation initiated through the CALVL_REQ parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.529 EMIF_CTLCFG_DENALI_PI_55 Register

1 EMIF_CTLCFG_DENALI_PI_55 Register (Offset = 20DCh) [reset = 0h]

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Table 14-13942. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0DCh**

Figure 14-4608. EMIF_CTLCFG_DENALI_PI_55 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_CALVL_ROTATE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_CALVL_DISABLE_DFS
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_CALVL_ON_SREF_EXIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_CALVL_PERIODIC
NONE							R/W
0h							0h

Table 14-13944. EMIF_CTLCFG_DENALI_PI_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_CALVL_ROTATE	R/W	0h	Enables rotational CS for interval CA training. Set to 1 for rotating CS. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_CALVL_DISABLE_DFS	R/W	0h	Disables automatic CA training on freq change. Set to 1 to disable CA training on dfs, Set to 0 to enable CA training . Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_CALVL_ON_SREF_EXIT	R/W	0h	Enables automatic CA training on a self-refresh exit. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_CALVL_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during CA training. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.530 EMIF_CTLCFG_DENALI_PI_56 Register

1 EMIF_CTLCFG_DENALI_PI_56 Register (Offset = 20E0h) [reset = 0h]

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Table 14-13945. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0E0h

Figure 14-4609. EMIF_CTLCFG_DENALI_PI_56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CALVL_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_CALVL_CS_MAP	
NONE						R/W	
0h						0h	

Table 14-13947. EMIF_CTLCFG_DENALI_PI_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TDFI_CALVL_EN	R/W	0h	Defines the DFI tCALVL_EN timing parameter [in DFI clocks], the minimum cycles between a dfi_calvl_en assertion and a dfi_cke de-assertion. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_CALVL_CS_MAP	R/W	0h	Defines the chip select map for CA training operations. Bit [0] controls cs0, bit [1] controls cs1, etc. Set each bit to 1 to enable chip for CA training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.531 EMIF_CTLCFG_DENALI_PI_57 Register

1 EMIF_CTLCFG_DENALI_PI_57 Register (Offset = 20E4h) [reset = 0h]

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Table 14-13948. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0E4h

Figure 14-4610. EMIF_CTLCFG_DENALI_PI_57 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CALVL_RESP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_CALVL_RESP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CALVL_RESP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CALVL_RESP							
R/W							
0h							

Table 14-13950. EMIF_CTLCFG_DENALI_PI_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CALVL_RESP	R/W	0h	Defines the DFI tCALVL_RESP timing parameter [in DFI clocks], the maximum cycles between a dfi_calvl_req assertion and a dfi_calvl_en assertion. Reset Source: ctl_amod_g_rst_n

14.5.1.2.532 EMIF_CTLCFG_DENALI_PI_58 Register

1 EMIF_CTLCFG_DENALI_PI_58 Register (Offset = 20E8h) [reset = 0h]

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Table 14-13951. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0E8h**

Figure 14-4611. EMIF_CTLCFG_DENALI_PI_58 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CALVL_MAX							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_CALVL_MAX							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CALVL_MAX							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CALVL_MAX							
R/W							
0h							

Table 14-13953. EMIF_CTLCFG_DENALI_PI_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CALVL_MAX	R/W	0h	Defines the DFI tCALVL_MAX timing parameter [in DFI clocks], the maximum cycles between a dfi_calvl_en assertion and a valid dfi_calvl_resp. Reset Source: ctl_amod_g_rst_n

14.5.1.2.533 EMIF_CTLCFG_DENALI_PI_59 Register

1 EMIF_CTLCFG_DENALI_PI_59 Register (Offset = 20ECh) [reset = 0h]

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Table 14-13954. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0ECh**

Figure 14-4612. EMIF_CTLCFG_DENALI_PI_59 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_CALVL_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_CALVL_INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_CALVL_ERROR_STATUS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_CALVL_RESP_MASK</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13956. EMIF_CTLCFG_DENALI_PI_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_CALVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic CA training commands. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_CALVL_ERROR_STATUS	R	0h	Holds the error associated with the CA training error interrupt. Bit [0] set indicates a TDFI_CALVL_RESP parameter violation and bit [1] set indicates a TDFI_CALVL_MAX parameter violation. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_CALVL_RESP_MASK	R/W	0h	Mask for the dfi_calvl_resp signal during CA training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.534 EMIF_CTLCFG_DENALI_PI_60 Register

1 EMIF_CTLCFG_DENALI_PI_60 Register (Offset = 20F0h) [reset = 0h]

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Table 14-13957. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0F0h

Figure 14-4613. EMIF_CTLCFG_DENALI_PI_60 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_TCAEXT				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_TCACKEH				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED		PI_TCAMRD					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED			PI_TCACKEL				
NONE			R/W				
0h			0h				

Table 14-13959. EMIF_CTLCFG_DENALI_PI_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TCAEXT	R/W	0h	DRAM tCAEXT value in memory cycles. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TCACKEH	R/W	0h	DRAM tCACKEH value in memory cycles. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_TCAMRD	R/W	0h	DRAM tCAMRD value in memory cycles. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCACKEL	R/W	0h	DRAM tCACKEL value in memory cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.535 EMIF_CTLCFG_DENALI_PI_61 Register

1 EMIF_CTLCFG_DENALI_PI_61 Register (Offset = 20F4h) [reset = 0h]

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Table 14-13960. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0F4h

Figure 14-4614. EMIF_CTLCFG_DENALI_PI_61 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_INIT_START_MIN							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_CALVL_VREF_NORMAL_STEPSIZE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_CALVL_VREF_INITIAL_STEPSIZE			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_CA_TRAIN_VREF_EN
NONE							R/W
0h							0h

Table 14-13962. EMIF_CTLCFG_DENALI_PI_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TDFI_INIT_START_MIN	R/W	0h	Minimum number of DFI clocks before dfi_init_start can be driven after a previous command/training event. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_CALVL_VREF_NORMAL_STEPSIZE	R/W	0h	The adjust step for the post-initial Vref[ca] training. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_CALVL_VREF_INITIAL_STEPSIZE	R/W	0h	The adjust step for the initial Vref[ca] training. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_CA_TRAIN_VREF_EN	R/W	0h	Control for VREF training during CA training post power-on initialization. Set to enable VREF training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.536 EMIF_CTLCFG_DENALI_PI_62 Register

1 EMIF_CTLCFG_DENALI_PI_62 Register (Offset = 20F8h) [reset = 1000000h]

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Table 14-13963. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A0F8h**

Figure 14-4615. EMIF_CTLCFG_DENALI_PI_62 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_REFRESH_BETWEEN_SEGMENT_DISABLE
NONE							R/W
0h							1h

23	22	21	20	19	18	17	16
RESERVED	PI_SW_CA_TRAIN_VREF						
NONE	R/W						
0h	0h						

15	14	13	12	11	10	9	8
RESERVED			PI_CALVL_STROBE_NUM				
NONE			R/W				
0h			0h				

7	6	5	4	3	2	1	0
PI_TCKCKEH							
R/W							
0h							

Table 14-13965. EMIF_CTLCFG_DENALI_PI_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_REFRESH_BETWEEN_SEGMENT_DISABLE	R/W	1h	Disable the refresh between CA first and second segment training. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_SW_CA_TRAIN_VREF	R/W	0h	The Vref value which is set for SW step by step CA training. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_CALVL_STROBE_NUM	R/W	0h	The consecutive dfi_calvl_strobe number when updating the CA vref data. Reset Source: ctl_amod_g_rst_n
7:0	PI_TCKCKEH	R/W	0h	DRAM tCKELCK Clock and command valid before CKE HIGH. Reset Source: ctl_amod_g_rst_n

14.5.1.2.537 EMIF_CTLCFG_DENALI_PI_63 Register

1 EMIF_CTLCFG_DENALI_PI_63 Register (Offset = 20FCh) [reset = 0h]

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Table 14-13966. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A0FCh

Figure 14-4616. EMIF_CTLCFG_DENALI_PI_63 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TDFI_INIT_COMPLETE_MIN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_DRAM_CLK_DISABLE_DEASSERT_SEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_INIT_STARTORCOMPLETE_2_CLKDISABLE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_CLKDISABLE_2_INIT_START</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13968. EMIF_CTLCFG_DENALI_PI_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TDFI_INIT_COMPLETE_MIN	R/W	0h	Minimum number of DFI clocks from dfi_init_complete to a command/training event. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DRAM_CLK_DISABLE_DEASSERT_SEL	R/W	0h	Indicate dfi_dram_clk_disable deassert following dfi_init_start deassert or dfi_init_complete assert. Set to 0: dfi_dram_clk_disable deassert following dfi_init_start deassert. Set to 1: dfi_dram_clk_disable deassert following dfi_init_complete assert. Reset Source: ctl_amod_g_rst_n
15:8	PI_INIT_STARTORCOMPLETE_2_CLKDISABLE	R/W	0h	Defines the delay from deasserting of dfi_init_start or asserting of dfi_init_complete to deasserting of dfi_dram_clk_disable in DFI clock. Reset Source: ctl_amod_g_rst_n
7:0	PI_CLKDISABLE_2_INIT_START	R/W	0h	Defines the delay from the asserting of dfi_dram_clk_disable to the asserting of dfi_init_start in DFI clock. Reset Source: ctl_amod_g_rst_n

14.5.1.2.538 EMIF_CTLCFG_DENALI_PI_64 Register

1 EMIF_CTLCFG_DENALI_PI_64 Register (Offset = 2100h) [reset = 0h]

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Table 14-13969. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A100h**

Figure 14-4617. EMIF_CTLCFG_DENALI_PI_64 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MC_DFS_PI_SET_VREF_ENABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_VREFLVL_DISABLE_DFS
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_VREF_PDA_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_VREF_CS
NONE							R/W
0h							0h

Table 14-13971. EMIF_CTLCFG_DENALI_PI_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_MC_DFS_PI_SET_VREF_ENABLE	R/W	0h	Enable the PI to set VREF value after DFS issued by MC. MR12 and MR14 for LPDDR4. MR6 for DDR4. 1 means disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_VREFLVL_DISABLE_DFS	R/W	0h	Disables automatic VREF training on freq change. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_VREF_PDA_EN	R/W	0h	Enable per-DRAM addressability during VREF training. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_VREF_CS	R/W	0h	Specifies the target chip select for the VREF training operation. Reset Source: ctl_amod_g_rst_n

14.5.1.2.539 EMIF_CTLCFG_DENALI_PI_65 Register

1 EMIF_CTLCFG_DENALI_PI_65 Register (Offset = 2104h) [reset = 0h]

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Table 14-13972. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A104h**

Figure 14-4618. EMIF_CTLCFG_DENALI_PI_65 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_WDQLVL_RESP_MASK	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PI_WDQLVL_BST_NUM		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_WDQLVL_VREF_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_INIT_COMPLETE_TO_MC_DELAY_COUNT							
R/W							
0h							

Table 14-13974. EMIF_CTLCFG_DENALI_PI_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_WDQLVL_RESP_MASK	R/W	0h	Write DQ training response mask. When set to 1, the dfi_wdqlvl_en of the slice is not asserted. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PI_WDQLVL_BST_NUM	R/W	0h	Defines the number of write/read bursts issued at each step in write DQ training. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WDQLVL_VREF_EN	R/W	0h	Control for VREF training as part of non-initialization write DQ training. Reset Source: ctl_amod_g_rst_n
7:0	PI_INIT_COMPLETE_TO_MC_DELAY_COUNT	R/W	0h	It controls the time PI bypass CKE at the beginning of PI mask dfi_init_complete to controller. Reset Source: ctl_amod_g_rst_n

14.5.1.2.540 EMIF_CTLCFG_DENALI_PI_66 Register

1 EMIF_CTLCFG_DENALI_PI_66 Register (Offset = 2108h) [reset = 0h]

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Table 14-13975. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A108h**

Figure 14-4619. EMIF_CTLCFG_DENALI_PI_66 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_WDQLVL_VREF_NORMAL_STEPSIZE</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_WDQLVL_VREF_INITIAL_STEPSIZE</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_WDQLVL_CS_MAP</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_WDQLVL_ROTATE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13977. EMIF_CTLCFG_DENALI_PI_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_WDQLVL_VREF_NORMAL_STEPSIZE	R/W	0h	Write DQ training vref step size for post_initial training. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_WDQLVL_VREF_INITIAL_STEPSIZE	R/W	0h	Write DQ training vref step size for initial training. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_CS_MAP	R/W	0h	Map of CS's included in write DQ training sequence. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_ROTATE	R/W	0h	Enables write DQ training rotate for interval training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.541 EMIF_CTLCFG_DENALI_PI_67 Register

1 EMIF_CTLCFG_DENALI_PI_67 Register (Offset = 210Ch) [reset = 0h]

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Table 14-13978. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A10Ch

Figure 14-4620. EMIF_CTLCFG_DENALI_PI_67 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_CS
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PI_WDQLVL_CS_SW	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED							PI_WDQLVL_REQ
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_WDQLVL_PERIODIC
NONE							R/W
0h							0h

Table 14-13980. EMIF_CTLCFG_DENALI_PI_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WDQLVL_CS	R/W	0h	Write DQ training target chip select. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_WDQLVL_CS_SW	R/W	0h	Write DQ training target chip select. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WDQLVL_REQ	W	0h	SW write to initiate Write DQ training request. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_PERIODIC	R/W	0h	Enables periodic write DQ training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.542 EMIF_CTLCFG_DENALI_PI_68 Register

1 EMIF_CTLCFG_DENALI_PI_68 Register (Offset = 2110h) [reset = 0h]

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Table 14-13981. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A110h**

Figure 14-4621. EMIF_CTLCFG_DENALI_PI_68 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_EN							
R/W							
0h							

Table 14-13983. EMIF_CTLCFG_DENALI_PI_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_TDFI_WDQLVL_EN	R/W	0h	DFI timing param tWDQLVL_EN. Minimum number of DFI clocks required after the write DQ training enable signal is asserted until the first write command may be asserted. Reset Source: ctl_amod_g_rst_n

14.5.1.2.543 EMIF_CTLCFG_DENALI_PI_69 Register

1 EMIF_CTLCFG_DENALI_PI_69 Register (Offset = 2114h) [reset = 0h]

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Table 14-13984. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A114h**

Figure 14-4622. EMIF_CTLCFG_DENALI_PI_69 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_WDQLVL_RESP							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WDQLVL_RESP							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WDQLVL_RESP							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RESP							
R/W							
0h							

Table 14-13986. EMIF_CTLCFG_DENALI_PI_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_WDQLVL_RESP	R/W	0h	DFI timing param tWDQLVL_RESP. Maximum number of DFI clocks that may occur between a write DQ training request and the associated mode enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.544 EMIF_CTLCFG_DENALI_PI_70 Register

1 EMIF_CTLCFG_DENALI_PI_70 Register (Offset = 2118h) [reset = 0h]

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Table 14-13987. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A118h**

Figure 14-4623. EMIF_CTLCFG_DENALI_PI_70 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_WDQLVL_MAX							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_WDQLVL_MAX							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_WDQLVL_MAX							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_MAX							
R/W							
0h							

Table 14-13989. EMIF_CTLCFG_DENALI_PI_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_WDQLVL_MAX	R/W	0h	DFI timing param tWDQLVL_MAX. Maximum number of DFI clocks that the PI will wait for a response from the PHY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.545 EMIF_CTLCFG_DENALI_PI_71 Register

1 EMIF_CTLCFG_DENALI_PI_71 Register (Offset = 211Ch) [reset = 0h]

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Table 14-13990. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A11Ch**

Figure 14-4624. EMIF_CTLCFG_DENALI_PI_71 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_ON_MPD_EXIT
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_WDQLVL_ON_SREF_EXIT
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_WDQLVL_INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_WDQLVL_INTERVAL							
R/W							
0h							

Table 14-13992. EMIF_CTLCFG_DENALI_PI_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WDQLVL_ON_MPD_EXIT	R/W	0h	Issue a write DQ training command on maximum power saving mode exit. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_WDQLVL_ON_SREF_EXIT	R/W	0h	Issue a write DQ training command on self-refresh exit. Reset Source: ctl_amod_g_rst_n
15:0	PI_WDQLVL_INTERVAL	R/W	0h	Sets the maximum number of long count sequences allowed between automatic write DQ training operations. Reset Source: ctl_amod_g_rst_n

14.5.1.2.546 EMIF_CTLCFG_DENALI_PI_72 Register

1 EMIF_CTLCFG_DENALI_PI_72 Register (Offset = 2120h) [reset = 0h]

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Table 14-13993. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A120h**

Figure 14-4625. EMIF_CTLCFG_DENALI_PI_72 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_WDQLVL_NEED_SAVE_RESTORE	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_WDQLVL_ERROR_STATUS	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_WDQLVL_DISABLE_DFS
NONE							R/W
0h							0h

Table 14-13995. EMIF_CTLCFG_DENALI_PI_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PI_WDQLVL_NEED_SAVE_RESTORE	R/W	0h	Enables the use of functional DRAM address space for write DQ training, 1 = enable, not for LPDDR4. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_ERROR_STATUS	R	0h	Holds the error associated with the write dq level error interrupt. Bit [0] set indicates a PI_TDFI_WDQLVL_MAX parameter violation and bit [1] set indicates a PI_TDFI_WDQLVL_RESP parameter violation. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_DISABLE_DFS	R/W	0h	Disable automatic write DQ training on freq change. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.547 EMIF_CTLCFG_DENALI_PI_73 Register

1 EMIF_CTLCFG_DENALI_PI_73 Register (Offset = 2124h) [reset = 0h]

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Table 14-13996. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A124h**

Figure 14-4626. EMIF_CTLCFG_DENALI_PI_73 Name Register

31	30	29	28	27	26	25	24
PI_WDQLVL_DRAM_LVL_START_ADDR_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_WDQLVL_DRAM_LVL_START_ADDR_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_WDQLVL_DRAM_LVL_START_ADDR_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_WDQLVL_DRAM_LVL_START_ADDR_0							
R/W							
0h							

Table 14-13998. EMIF_CTLCFG_DENALI_PI_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_WDQLVL_DRAM_LVL_START_ADDR_0	R/W	0h	Start address of WDQ leveling, not for LPDDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.548 EMIF_CTLCFG_DENALI_PI_74 Register

1 EMIF_CTLCFG_DENALI_PI_74 Register (Offset = 2128h) [reset = 0h]

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Table 14-13999. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A128h

Figure 14-4627. EMIF_CTLCFG_DENALI_PI_74 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_NO_MEMORY_DM
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_WDQLVL_DM_LEVEL_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_WDQLVL_DRAM_LVL_START_ADDR_1
NONE							R/W
0h							0h

Table 14-14001. EMIF_CTLCFG_DENALI_PI_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PI_NO_MEMORY_DM	R/W	0h	Defines if the attached memory supports the Data Mask function, 1 = not supported. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_WDQLVL_DM_LEVEL_EN	R/W	0h	Enable for write DM training as part of the write DQ training, not for LPDDR4. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_DRAM_LVL_START_ADDR_1	R/W	0h	Start address of WDQ leveling, not for LPDDR4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.549 EMIF_CTLCFG_DENALI_PI_75 Register

1 EMIF_CTLCFG_DENALI_PI_75 Register (Offset = 212Ch) [reset = 0h]

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Table 14-14002. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A12Ch

Figure 14-4628. EMIF_CTLCFG_DENALI_PI_75 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_WDQLVL_NIBBLE_MODE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_SWLVL_SM2_DM_NIBBLE_START</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_WDQLVL_WW</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_WDQLVL_WW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14004. EMIF_CTLCFG_DENALI_PI_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WDQLVL_NIBBLE_MODE	R/W	0h	WDQ Training Nibble mode indication. When set to 1, nibble mode is enabled, and the training timing is doubled. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SWLVL_SM2_DM_NIBBLE_START	W	0h	Start command for stage 2, when in the process of DM leveling or nibble mode. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WDQLVL_WW	R/W	0h	Minimum number of DFI clocks to be inserted between write commands during the DM portion of write DQ training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.550 EMIF_CTLCFG_DENALI_PI_76 Register

1 EMIF_CTLCFG_DENALI_PI_76 Register (Offset = 2130h) [reset = 0h]

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Table 14-14005. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A130h**

Figure 14-4629. EMIF_CTLCFG_DENALI_PI_76 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_PDA_VREF_TRAIN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_WDQLVL_PDA_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_DQS_OSC_PERIOD_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_WDQLVL_OSC_EN
NONE							R/W
0h							0h

Table 14-14007. EMIF_CTLCFG_DENALI_PI_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_WDQLVL_PDA_VREF_TRAIN	R/W	0h	Enable for the use of PDA to set the VREF during write DQ training, 1 = enabled. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_WDQLVL_PDA_EN	R/W	0h	Enable for the use of write DQ training for PDA mode, 1 = enabled. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_DQS_OSC_PERIOD_EN	R/W	0h	Enable for DQS oscillator triggered periodic write DQ training, 1 = enabled. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_WDQLVL_OSC_EN	R/W	0h	Enable for DQS oscillator triggered write DQ training, 1 = enabled. Reset Source: ctl_amod_g_rst_n

14.5.1.2.551 EMIF_CTLCFG_DENALI_PI_77 Register

1 EMIF_CTLCFG_DENALI_PI_77 Register (Offset = 2134h) [reset = 0h]

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Table 14-14008. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A134h

Figure 14-4630. EMIF_CTLCFG_DENALI_PI_77 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_TCCD				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED					PI_ROW_DIFF		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED						PI_BANK_DIFF	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_DBILVL_RESP_MASK	
NONE						R/W	
0h						0h	

Table 14-14010. EMIF_CTLCFG_DENALI_PI_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TCCD	R/W	0h	DRAM CAS-to-CAS value in cycles. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PI_ROW_DIFF	R/W	0h	Difference between number of address pins available and number being used. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_BANK_DIFF	R/W	0h	Difference between number of bank pins available and number being used. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_DBILVL_RESP_MASK	R/W	0h	Mask for the dfi_rdlvl_resp signal during read dbi training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.552 EMIF_CTLCFG_DENALI_PI_78 Register

1 EMIF_CTLCFG_DENALI_PI_78 Register (Offset = 2138h) [reset = 20000h]

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Table 14-14011. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A138h**

Figure 14-4631. EMIF_CTLCFG_DENALI_PI_78 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED10			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED9			
NONE				R/W			
0h				2h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED8			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PI_RESERVED7			
NONE				R/W			
0h				0h			

Table 14-14013. EMIF_CTLCFG_DENALI_PI_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED10	R/W	0h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED9	R/W	2h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED8	R/W	0h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED7	R/W	0h	Reserved

14.5.1.2.553 EMIF_CTLCFG_DENALI_PI_79 Register

1 EMIF_CTLCFG_DENALI_PI_79 Register (Offset = 213Ch) [reset = 10002h]

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Table 14-14014. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A13Ch**

Figure 14-4632. EMIF_CTLCFG_DENALI_PI_79 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED14</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED13</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED12</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED11</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
</table>

Table 14-14016. EMIF_CTLCFG_DENALI_PI_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED14	R/W	0h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED13	R/W	1h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED12	R/W	0h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED11	R/W	2h	Reserved

14.5.1.2.554 EMIF_CTLCFG_DENALI_PI_80 Register

1 EMIF_CTLCFG_DENALI_PI_80 Register (Offset = 2140h) [reset = 1h]

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Table 14-14017. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A140h**

Figure 14-4633. EMIF_CTLCFG_DENALI_PI_80 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED18			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED17			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED16			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PI_RESERVED15			
NONE				R/W			
0h				1h			

Table 14-14019. EMIF_CTLCFG_DENALI_PI_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED18	R/W	0h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED17	R/W	0h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED16	R/W	0h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED15	R/W	1h	Reserved

14.5.1.2.555 EMIF_CTLCFG_DENALI_PI_81 Register

1 EMIF_CTLCFG_DENALI_PI_81 Register (Offset = 2144h) [reset = 20001h]

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Table 14-14020. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A144h**

Figure 14-4634. EMIF_CTLCFG_DENALI_PI_81 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED22			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED21			
NONE				R/W			
0h				2h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED20			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PI_RESERVED19			
NONE				R/W			
0h				1h			

Table 14-14022. EMIF_CTLCFG_DENALI_PI_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED22	R/W	0h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED21	R/W	2h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED20	R/W	0h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED19	R/W	1h	Reserved

14.5.1.2.556 EMIF_CTLCFG_DENALI_PI_82 Register

1 EMIF_CTLCFG_DENALI_PI_82 Register (Offset = 2148h) [reset = 20002h]

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Table 14-14023. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A148h

Figure 14-4635. EMIF_CTLCFG_DENALI_PI_82 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED26</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED25</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED24</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED23</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
</table>

Table 14-14025. EMIF_CTLCFG_DENALI_PI_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_RESERVED26	R/W	0h	Reserved
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_RESERVED25	R/W	2h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED24	R/W	0h	Reserved
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_RESERVED23	R/W	2h	Reserved

14.5.1.2.557 EMIF_CTLCFG_DENALI_PI_83 Register

1 EMIF_CTLCFG_DENALI_PI_83 Register (Offset = 214Ch) [reset = 0h]

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Table 14-14026. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A14Ch

Figure 14-4636. EMIF_CTLCFG_DENALI_PI_83 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_INT_STATUS					
NONE		R					
0h		0h					
23	22	21	20	19	18	17	16
PI_INT_STATUS							
R							
0h							
15	14	13	12	11	10	9	8
PI_INT_STATUS							
R							
0h							
7	6	5	4	3	2	1	0
PI_INT_STATUS							
R							
0h							

Table 14-14028. EMIF_CTLCFG_DENALI_PI_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_INT_STATUS	R	0h	Status of interrupt features in the PI. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.558 EMIF_CTLCFG_DENALI_PI_84 Register

1 EMIF_CTLCFG_DENALI_PI_84 Register (Offset = 2150h) [reset = 0h]

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Table 14-14029. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A150h**

Figure 14-4637. EMIF_CTLCFG_DENALI_PI_84 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_INT_ACK				
NONE			W				
0h			0h				
23	22	21	20	19	18	17	16
PI_INT_ACK							
W							
0h							
15	14	13	12	11	10	9	8
PI_INT_ACK							
W							
0h							
7	6	5	4	3	2	1	0
PI_INT_ACK							
W							
0h							

Table 14-14031. EMIF_CTLCFG_DENALI_PI_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:0	PI_INT_ACK	W	0h	Clear the corresponding interrupt bit of the PI_INT_STATUS parameter. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.559 EMIF_CTLCFG_DENALI_PI_85 Register

1 EMIF_CTLCFG_DENALI_PI_85 Register (Offset = 2154h) [reset = 0h]

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Table 14-14032. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A154h**

Figure 14-4638. EMIF_CTLCFG_DENALI_PI_85 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_INT_MASK</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_INT_MASK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_INT_MASK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_INT_MASK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14034. EMIF_CTLCFG_DENALI_PI_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_INT_MASK	R/W	0h	Mask for PI_int signals from the PI_INT_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.560 EMIF_CTLCFG_DENALI_PI_86 Register

1 EMIF_CTLCFG_DENALI_PI_86 Register (Offset = 2158h) [reset = 0h]

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Table 14-14035. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A158h**

Figure 14-4639. EMIF_CTLCFG_DENALI_PI_86 Name Register

31	30	29	28	27	26	25	24
PI_BIST_EXP_DATA_0							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_EXP_DATA_0							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_EXP_DATA_0							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_0							
R							
0h							

Table 14-14037. EMIF_CTLCFG_DENALI_PI_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_EXP_DATA_0	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.561 EMIF_CTLCFG_DENALI_PI_87 Register

1 EMIF_CTLCFG_DENALI_PI_87 Register (Offset = 215Ch) [reset = 0h]

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Table 14-14038. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A15Ch**

Figure 14-4640. EMIF_CTLCFG_DENALI_PI_87 Name Register

31	30	29	28	27	26	25	24
PI_BIST_EXP_DATA_1							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_EXP_DATA_1							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_EXP_DATA_1							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_1							
R							
0h							

Table 14-14040. EMIF_CTLCFG_DENALI_PI_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_EXP_DATA_1	R	0h	Expected data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.562 EMIF_CTLCFG_DENALI_PI_88 Register

1 EMIF_CTLCFG_DENALI_PI_88 Register (Offset = 2160h) [reset = 0h]

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Table 14-14041. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A160h**

Figure 14-4641. EMIF_CTLCFG_DENALI_PI_88 Name Register

31	30	29	28	27	26	25	24
PI_BIST_FAIL_DATA_0							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_FAIL_DATA_0							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_FAIL_DATA_0							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_0							
R							
0h							

Table 14-14043. EMIF_CTLCFG_DENALI_PI_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_FAIL_DATA_0	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.563 EMIF_CTLCFG_DENALI_PI_89 Register

1 EMIF_CTLCFG_DENALI_PI_89 Register (Offset = 2164h) [reset = 0h]

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Table 14-14044. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A164h**

Figure 14-4642. EMIF_CTLCFG_DENALI_PI_89 Name Register

31	30	29	28	27	26	25	24
PI_BIST_FAIL_DATA_1							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_FAIL_DATA_1							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_FAIL_DATA_1							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_1							
R							
0h							

Table 14-14046. EMIF_CTLCFG_DENALI_PI_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_FAIL_DATA_1	R	0h	Actual data on BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.564 EMIF_CTLCFG_DENALI_PI_90 Register

1 EMIF_CTLCFG_DENALI_PI_90 Register (Offset = 2168h) [reset = 0h]

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Table 14-14047. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A168h**

Figure 14-4643. EMIF_CTLCFG_DENALI_PI_90 Name Register

31	30	29	28	27	26	25	24
PI_BIST_FAIL_ADDR_0							
R							
0h							
23	22	21	20	19	18	17	16
PI_BIST_FAIL_ADDR_0							
R							
0h							
15	14	13	12	11	10	9	8
PI_BIST_FAIL_ADDR_0							
R							
0h							
7	6	5	4	3	2	1	0
PI_BIST_FAIL_ADDR_0							
R							
0h							

Table 14-14049. EMIF_CTLCFG_DENALI_PI_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_FAIL_ADDR_0	R	0h	The burst aligned address of BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.565 EMIF_CTLCFG_DENALI_PI_91 Register

1 EMIF_CTLCFG_DENALI_PI_91 Register (Offset = 216Ch) [reset = 200h]

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Table 14-14050. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A16Ch

Figure 14-4644. EMIF_CTLCFG_DENALI_PI_91 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_CMD_SWAP_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_LONG_COUNT_MASK</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_BSTLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_BIST_FAIL_ADDR_1</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14052. EMIF_CTLCFG_DENALI_PI_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_CMD_SWAP_EN	R/W	0h	Command pin swap function enable Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_LONG_COUNT_MASK	R/W	0h	Reduces the length of the long counter from 1024 cycles. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_BSTLEN	R/W	2h	Encoded burst length sent to DRAMs during initialization. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_BIST_FAIL_ADDR_1	R	0h	The burst aligned address of BIST error. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.566 EMIF_CTLCFG_DENALI_PI_92 Register

1 EMIF_CTLCFG_DENALI_PI_92 Register (Offset = 2170h) [reset = 0h]

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Table 14-14053. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A170h**

Figure 14-4645. EMIF_CTLCFG_DENALI_PI_92 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_BG_MUX_1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_BG_MUX_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PI_ACT_N_MUX				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_PARITY_IN_MUX				
NONE			R/W				
0h			0h				

Table 14-14055. EMIF_CTLCFG_DENALI_PI_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_BG_MUX_1	R/W	0h	Command pin BG_1 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_BG_MUX_0	R/W	0h	Command pin BG_0 mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_ACT_N_MUX	R/W	0h	Command pin ACT_N mux selector Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_PARITY_IN_MUX	R/W	0h	Command pin parity mux selector Reset Source: ctl_amod_g_rst_n

14.5.1.2.567 EMIF_CTLCFG_DENALI_PI_93 Register

1 EMIF_CTLCFG_DENALI_PI_93 Register (Offset = 2174h) [reset = 0h]

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Table 14-14056. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A174h**

Figure 14-4646. EMIF_CTLCFG_DENALI_PI_93 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_BANK_MUX_0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PI_WE_N_MUX				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PI_CAS_N_MUX				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PI_RAS_N_MUX				
NONE			R/W				
0h			0h				

Table 14-14058. EMIF_CTLCFG_DENALI_PI_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_BANK_MUX_0	R/W	0h	Command pin BANK_0 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_WE_N_MUX	R/W	0h	Command pin WE_N mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_CAS_N_MUX	R/W	0h	Command pin CAS_N mux selector Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_RAS_N_MUX	R/W	0h	Command pin RAS_N mux selector Reset Source: ctl_amod_g_rst_n

14.5.1.2.568 EMIF_CTLCFG_DENALI_PI_94 Register

1 EMIF_CTLCFG_DENALI_PI_94 Register (Offset = 2178h) [reset = 0h]

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Table 14-14059. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A178h**

Figure 14-4647. EMIF_CTLCFG_DENALI_PI_94 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_DATA_BYTE_SWAP_SLICE1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_DATA_BYTE_SWAP_SLICE0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_DATA_BYTE_SWAP_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_BANK_MUX_1				
NONE			R/W				
0h			0h				

Table 14-14061. EMIF_CTLCFG_DENALI_PI_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_DATA_BYTE_SWAP_SLICE1	R/W	0h	DATA pin 1 mux selector Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DATA_BYTE_SWAP_SLICE0	R/W	0h	DATA pin 0 mux selector Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_DATA_BYTE_SWAP_EN	R/W	0h	DATA pin swap function enable Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_BANK_MUX_1	R/W	0h	Command pin BANK_1 mux selector Reset Source: ctl_amod_g_rst_n

14.5.1.2.569 EMIF_CTLCFG_DENALI_PI_95 Register

1 EMIF_CTLCFG_DENALI_PI_95 Register (Offset = 217Ch) [reset = 0h]

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Table 14-14062. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A17Ch**

Figure 14-4648. EMIF_CTLCFG_DENALI_PI_95 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_UPDATE_ERROR_STATUS	
NONE						R	
0h						0h	
23	22	21	20	19	18	17	16
PI_TDFI_CTRLUPD_MIN							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_MIN							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PI_CTRLUPD_REQ_PER_AREF_EN
NONE							R/W
0h							0h

Table 14-14064. EMIF_CTLCFG_DENALI_PI_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_UPDATE_ERROR_STATUS	R	0h	Identifies the source of any DFI PI-initiated update errors. Value of 1 indicates a timing violation of the associated timing parameter. Bit 1-0: ctrlupd_max_error, ctrlupd_interval_error. Bit 6-2: reserved. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:8	PI_TDFI_CTRLUPD_MIN	R/W	0h	Reports the DFI tCTRLUPD_MIN timing parameter [in DFI clocks], the minimum cycles that dfi_ctrlupd_req must be asserted. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_CTRLUPD_REQ_PER_AREF_EN	R/W	0h	Enable an automatic PI initiated update [dfi_ctrlupd_req] after every refresh. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.570 EMIF_CTLCFG_DENALI_PI_96 Register

1 EMIF_CTLCFG_DENALI_PI_96 Register (Offset = 2180h) [reset = 0h]

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Table 14-14065. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A180h**

Figure 14-4649. EMIF_CTLCFG_DENALI_PI_96 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_BIST_LFSR_PATTERN_DONE
NONE							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_BIST_RESULT	
NONE						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_BIST_GO
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PI_TDFI_PARIN_LAT		
NONE					R/W		
0h					0h		

Table 14-14067. EMIF_CTLCFG_DENALI_PI_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_BIST_LFSR_PATTERN_DONE	R	0h	BIST operation lfsr pattern, data pattern 1'b0 means the data is useful,1'b1 means next pattern sequence can ingore. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_BIST_RESULT	R	0h	BIST operation status [pass/fail]. Bit [0] indicates data check status and bit [1] indicates address check status. Value of 1 is a passing result. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_BIST_GO	R/W	0h	Initiate a BIST operation. Set to 1 to trigger. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_TDFI_PARIN_LAT	R/W	0h	Defines the DFI tPARIN_LAT timing parameter [in DFI PHY clocks], the maximum cycles between a DFI command and a dfi_parity_in signal assertion. Reset Source: ctl_amod_g_rst_n

14.5.1.2.571 EMIF_CTLCFG_DENALI_PI_97 Register

1 EMIF_CTLCFG_DENALI_PI_97 Register (Offset = 2184h) [reset = 0h]

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Table 14-14068. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A184h**

Figure 14-4650. EMIF_CTLCFG_DENALI_PI_97 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_BIST_ADDR_CHECK
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_BIST_DATA_CHECK
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PI_ADDR_SPACE							
R/W							
0h							

Table 14-14070. EMIF_CTLCFG_DENALI_PI_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PI_BIST_ADDR_CHECK	R/W	0h	Enable address checking with BIST operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_BIST_DATA_CHECK	R/W	0h	Enable data checking with BIST operation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:0	PI_ADDR_SPACE	R/W	0h	Sets the number of address bits to check during BIST operation. The end address of BIST is start_address+[1 shifted up by PI_ADDR_SPACE]-1. The end address should not beyond the actual memory address range. Reset Source: ctl_amod_g_rst_n

14.5.1.2.572 EMIF_CTLCFG_DENALI_PI_98 Register

1 EMIF_CTLCFG_DENALI_PI_98 Register (Offset = 2188h) [reset = 0h]

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Table 14-14071. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A188h**

Figure 14-4651. EMIF_CTLCFG_DENALI_PI_98 Name Register

31	30	29	28	27	26	25	24
PI_BIST_START_ADDRESS_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_START_ADDRESS_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_START_ADDRESS_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_START_ADDRESS_0							
R/W							
0h							

Table 14-14073. EMIF_CTLCFG_DENALI_PI_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_START_ADDRESS_0	R/W	0h	Start BIST checking at this address. Reset Source: ctl_amod_g_rst_n

14.5.1.2.573 EMIF_CTLCFG_DENALI_PI_99 Register

1 EMIF_CTLCFG_DENALI_PI_99 Register (Offset = 218Ch) [reset = 0h]

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Table 14-14074. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A18Ch**

Figure 14-4652. EMIF_CTLCFG_DENALI_PI_99 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MBIST_INIT_PATTERN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_BIST_START_ADDRESS_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14076. EMIF_CTLCFG_DENALI_PI_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_MBIST_INIT_PATTERN	R/W	0h	PI mbist data check, random lfsr pattern mode init pattern seed. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_BIST_START_ADDRESS_1	R/W	0h	Start BIST checking at this address. Reset Source: ctl_amod_g_rst_n

14.5.1.2.574 EMIF_CTLCFG_DENALI_PI_100 Register

1 EMIF_CTLCFG_DENALI_PI_100 Register (Offset = 2190h) [reset = 0h]

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Table 14-14077. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A190h

Figure 14-4653. EMIF_CTLCFG_DENALI_PI_100 Name Register

31	30	29	28	27	26	25	24
PI_BIST_DATA_MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_DATA_MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_DATA_MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_DATA_MASK							
R/W							
0h							

Table 14-14079. EMIF_CTLCFG_DENALI_PI_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_DATA_MASK	R/W	0h	Mask applied to data for BIST error checking. Bit [0] controls memory data path bit [0], bit [1] controls memory data path bit [1], etc. The mask range is the data transfer size in each memory clock cycle [The data on a rising edge and a failing edge]. Set each bit to 1 to mask. Reset Source: ctl_amod_g_rst_n

14.5.1.2.575 EMIF_CTLCFG_DENALI_PI_101 Register

1 EMIF_CTLCFG_DENALI_PI_101 Register (Offset = 2194h) [reset = 0h]

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Table 14-14080. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A194h**

Figure 14-4654. EMIF_CTLCFG_DENALI_PI_101 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_BIST_ERR_STOP</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_BIST_ERR_STOP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_BIST_ERR_COUNT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_BIST_ERR_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14082. EMIF_CTLCFG_DENALI_PI_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_BIST_ERR_STOP	R/W	0h	Defines the maximum number of error occurrences allowed prior to quitting when the BIST_TEST_MODE parameter is set to 1, 2 or 3. A value of 0 will allow the test to run to completion. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_BIST_ERR_COUNT	R	0h	Indicates the number of BIST errors found when the BIST_TEST_MODE parameter is set to 1, 2 or 3. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.576 EMIF_CTLCFG_DENALI_PI_102 Register

1 EMIF_CTLCFG_DENALI_PI_102 Register (Offset = 2198h) [reset = 0h]

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Table 14-14083. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A198h**

Figure 14-4655. EMIF_CTLCFG_DENALI_PI_102 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_0_0							
R/W							
0h							

Table 14-14085. EMIF_CTLCFG_DENALI_PI_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_0_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.577 EMIF_CTLCFG_DENALI_PI_103 Register

1 EMIF_CTLCFG_DENALI_PI_103 Register (Offset = 219Ch) [reset = 0h]

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Table 14-14086. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A19Ch

Figure 14-4656. EMIF_CTLCFG_DENALI_PI_103 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_BIST_ADDR_MASK_0_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14088. EMIF_CTLCFG_DENALI_PI_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_0_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.578 EMIF_CTLCFG_DENALI_PI_104 Register

1 EMIF_CTLCFG_DENALI_PI_104 Register (Offset = 21A0h) [reset = 0h]

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Table 14-14089. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1A0h**

Figure 14-4657. EMIF_CTLCFG_DENALI_PI_104 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_1_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_1_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_1_0							
R/W							
0h							

Table 14-14091. EMIF_CTLCFG_DENALI_PI_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_1_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.579 EMIF_CTLCFG_DENALI_PI_105 Register

1 EMIF_CTLCFG_DENALI_PI_105 Register (Offset = 21A4h) [reset = 0h]

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Table 14-14092. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A1A4h

Figure 14-4658. EMIF_CTLCFG_DENALI_PI_105 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_BIST_ADDR_MASK_1_1	
NONE						R/W	
0h						0h	

Table 14-14094. EMIF_CTLCFG_DENALI_PI_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_1_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.580 EMIF_CTLCFG_DENALI_PI_106 Register

1 EMIF_CTLCFG_DENALI_PI_106 Register (Offset = 21A8h) [reset = 0h]

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Table 14-14095. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1A8h**

Figure 14-4659. EMIF_CTLCFG_DENALI_PI_106 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_2_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_2_0							
R/W							
0h							

Table 14-14097. EMIF_CTLCFG_DENALI_PI_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_2_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.581 EMIF_CTLCFG_DENALI_PI_107 Register

1 EMIF_CTLCFG_DENALI_PI_107 Register (Offset = 21ACh) [reset = 0h]

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Table 14-14098. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A1ACh

Figure 14-4660. EMIF_CTLCFG_DENALI_PI_107 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_BIST_ADDR_MASK_2_1	
NONE						R/W	
0h						0h	

Table 14-14100. EMIF_CTLCFG_DENALI_PI_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_2_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.582 EMIF_CTLCFG_DENALI_PI_108 Register

1 EMIF_CTLCFG_DENALI_PI_108 Register (Offset = 21B0h) [reset = 0h]

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Table 14-14101. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1B0h**

Figure 14-4661. EMIF_CTLCFG_DENALI_PI_108 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_3_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_3_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_3_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_3_0							
R/W							
0h							

Table 14-14103. EMIF_CTLCFG_DENALI_PI_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_3_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.583 EMIF_CTLCFG_DENALI_PI_109 Register

1 EMIF_CTLCFG_DENALI_PI_109 Register (Offset = 21B4h) [reset = 0h]

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Table 14-14104. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1B4h**

Figure 14-4662. EMIF_CTLCFG_DENALI_PI_109 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_BIST_ADDR_MASK_3_1	
NONE						R/W	
0h						0h	

Table 14-14106. EMIF_CTLCFG_DENALI_PI_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_3_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.584 EMIF_CTLCFG_DENALI_PI_110 Register

1 EMIF_CTLCFG_DENALI_PI_110 Register (Offset = 21B8h) [reset = 0h]

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Table 14-14107. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1B8h**

Figure 14-4663. EMIF_CTLCFG_DENALI_PI_110 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_4_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_4_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_4_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_4_0							
R/W							
0h							

Table 14-14109. EMIF_CTLCFG_DENALI_PI_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_4_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.585 EMIF_CTLCFG_DENALI_PI_111 Register

1 EMIF_CTLCFG_DENALI_PI_111 Register (Offset = 21BCh) [reset = 0h]

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Table 14-14110. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A1BCh

Figure 14-4664. EMIF_CTLCFG_DENALI_PI_111 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_BIST_ADDR_MASK_4_1	
NONE						R/W	
0h						0h	

Table 14-14112. EMIF_CTLCFG_DENALI_PI_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_4_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.586 EMIF_CTLCFG_DENALI_PI_112 Register

1 EMIF_CTLCFG_DENALI_PI_112 Register (Offset = 21C0h) [reset = 0h]

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Table 14-14113. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1C0h**

Figure 14-4665. EMIF_CTLCFG_DENALI_PI_112 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_5_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_5_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_5_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_5_0							
R/W							
0h							

Table 14-14115. EMIF_CTLCFG_DENALI_PI_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_5_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.587 EMIF_CTLCFG_DENALI_PI_113 Register

1 EMIF_CTLCFG_DENALI_PI_113 Register (Offset = 21C4h) [reset = 0h]

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Table 14-14116. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1C4h**

Figure 14-4666. EMIF_CTLCFG_DENALI_PI_113 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_BIST_ADDR_MASK_5_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14118. EMIF_CTLCFG_DENALI_PI_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_5_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.588 EMIF_CTLCFG_DENALI_PI_114 Register

1 EMIF_CTLCFG_DENALI_PI_114 Register (Offset = 21C8h) [reset = 0h]

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Table 14-14119. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1C8h**

Figure 14-4667. EMIF_CTLCFG_DENALI_PI_114 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_6_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_6_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_6_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_6_0							
R/W							
0h							

Table 14-14121. EMIF_CTLCFG_DENALI_PI_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_6_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.589 EMIF_CTLCFG_DENALI_PI_115 Register

1 EMIF_CTLCFG_DENALI_PI_115 Register (Offset = 21CCh) [reset = 0h]

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Table 14-14122. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A1CCh

Figure 14-4668. EMIF_CTLCFG_DENALI_PI_115 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_BIST_ADDR_MASK_6_1	
NONE						R/W	
0h						0h	

Table 14-14124. EMIF_CTLCFG_DENALI_PI_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_6_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.590 EMIF_CTLCFG_DENALI_PI_116 Register

1 EMIF_CTLCFG_DENALI_PI_116 Register (Offset = 21D0h) [reset = 0h]

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Table 14-14125. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1D0h**

Figure 14-4669. EMIF_CTLCFG_DENALI_PI_116 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_7_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_7_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_7_0							
R/W							
0h							

Table 14-14127. EMIF_CTLCFG_DENALI_PI_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_7_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.591 EMIF_CTLCFG_DENALI_PI_117 Register

1 EMIF_CTLCFG_DENALI_PI_117 Register (Offset = 21D4h) [reset = 0h]

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Table 14-14128. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A1D4h

Figure 14-4670. EMIF_CTLCFG_DENALI_PI_117 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_BIST_ADDR_MASK_7_1	
NONE						R/W	
0h						0h	

Table 14-14130. EMIF_CTLCFG_DENALI_PI_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_7_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.592 EMIF_CTLCFG_DENALI_PI_118 Register

1 EMIF_CTLCFG_DENALI_PI_118 Register (Offset = 21D8h) [reset = 0h]

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Table 14-14131. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1D8h**

Figure 14-4671. EMIF_CTLCFG_DENALI_PI_118 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_8_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_8_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_8_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_8_0							
R/W							
0h							

Table 14-14133. EMIF_CTLCFG_DENALI_PI_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_8_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.593 EMIF_CTLCFG_DENALI_PI_119 Register

1 EMIF_CTLCFG_DENALI_PI_119 Register (Offset = 21DCh) [reset = 0h]

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Table 14-14134. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1DCh**

Figure 14-4672. EMIF_CTLCFG_DENALI_PI_119 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PI_BIST_ADDR_MASK_8_1	
NONE						R/W	
0h						0h	

Table 14-14136. EMIF_CTLCFG_DENALI_PI_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PI_BIST_ADDR_MASK_8_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.594 EMIF_CTLCFG_DENALI_PI_120 Register

1 EMIF_CTLCFG_DENALI_PI_120 Register (Offset = 21E0h) [reset = 0h]

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Table 14-14137. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1E0h**

Figure 14-4673. EMIF_CTLCFG_DENALI_PI_120 Name Register

31	30	29	28	27	26	25	24
PI_BIST_ADDR_MASK_9_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_ADDR_MASK_9_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_ADDR_MASK_9_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_9_0							
R/W							
0h							

Table 14-14139. EMIF_CTLCFG_DENALI_PI_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_ADDR_MASK_9_0	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.595 EMIF_CTLCFG_DENALI_PI_121 Register

1 EMIF_CTLCFG_DENALI_PI_121 Register (Offset = 21E4h) [reset = 0h]

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Table 14-14140. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1E4h**

Figure 14-4674. EMIF_CTLCFG_DENALI_PI_121 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_BIST_PAT_MODE	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_BIST_ADDR_MODE	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED					PI_BIST_MODE		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED						PI_BIST_ADDR_MASK_9_1	
NONE						R/W	
0h						0h	

Table 14-14142. EMIF_CTLCFG_DENALI_PI_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_BIST_PAT_MODE	R/W	0h	Sets the pattern mode of BIST. 'b00 indicates using built-in pattern. 'b01 indicates checkerboard pattern, each data transfer inverts the last data transfer based on the built-in pattern. 'b10 indicates using both user pattern and built-in pattern. 'b11 indicates using pi lfsr random pattern. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_BIST_ADDR_MODE	R/W	0h	Sets the address traversing order of BIST. 'b00 indicates fast column order [burst-column-bank-row-rank]. 'b01 indicates fast row order [burst-row-column-bank-rank]. 'b10 indicates fast bank order [burst-bank-column-row-rank]. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PI_BIST_MODE	R/W	0h	Sets the BIST data checking mode. 'b00 indicates MOVI13N mode. 'b01 indicates March C mode. 'b10 indicates GALPAT mode. 'b11 indicates PRBS mode. 'b100 indicates programmable March data check mode. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved

Table 14-14142. EMIF_CTLCFG_DENALI_PI_121 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PI_BIST_ADDR_MASK_9_1	R/W	0h	Defines an address to be masked during the BIST operation.. Reset Source: ctl_amod_g_rst_n

14.5.1.2.596 EMIF_CTLCFG_DENALI_PI_122 Register

1 EMIF_CTLCFG_DENALI_PI_122 Register (Offset = 21E8h) [reset = 0h]

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Table 14-14143. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1E8h**

Figure 14-4675. EMIF_CTLCFG_DENALI_PI_122 Name Register

31	30	29	28	27	26	25	24
PI_BIST_USER_PAT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_BIST_USER_PAT_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_USER_PAT_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_USER_PAT_0							
R/W							
0h							

Table 14-14145. EMIF_CTLCFG_DENALI_PI_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_USER_PAT_0	R/W	0h	Sets the user-specified pattern of BIST. Reset Source: ctl_amod_g_rst_n

14.5.1.2.597 EMIF_CTLCFG_DENALI_PI_123 Register

1 EMIF_CTLCFG_DENALI_PI_123 Register (Offset = 21ECh) [reset = 0h]

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Table 14-14146. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1ECh**

Figure 14-4676. EMIF_CTLCFG_DENALI_PI_123 Name Register

31	30	29	28	27	26	25	24
PI_BIST_USER_PAT_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_USER_PAT_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_USER_PAT_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_USER_PAT_1							
R/W							
0h							

Table 14-14148. EMIF_CTLCFG_DENALI_PI_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_BIST_USER_PAT_1	R/W	0h	Sets the user-specified pattern of BIST. Reset Source: ctl_amod_g_rst_n

14.5.1.2.598 EMIF_CTLCFG_DENALI_PI_124 Register

1 EMIF_CTLCFG_DENALI_PI_124 Register (Offset = 21F0h) [reset = 0h]

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Table 14-14149. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A1F0h

Figure 14-4677. EMIF_CTLCFG_DENALI_PI_124 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PI_BIST_PAT_NUM					
NONE		R/W					
0h		0h					

Table 14-14151. EMIF_CTLCFG_DENALI_PI_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PI_BIST_PAT_NUM	R/W	0h	Sets the max used pattern number of BIST from a total of 8 built-in patterns. Ex. set to 3, The BIST would use pattern 1, 2 and 3. Reset Source: ctl_amod_g_rst_n

14.5.1.2.599 EMIF_CTLCFG_DENALI_PI_125 Register

1 EMIF_CTLCFG_DENALI_PI_125 Register (Offset = 21F4h) [reset = 0h]

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Table 14-14152. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A1F4h

Figure 14-4678. EMIF_CTLCFG_DENALI_PI_125 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_STAGE_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_STAGE_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_STAGE_0							
R/W							
0h							

Table 14-14154. EMIF_CTLCFG_DENALI_PI_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_0	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.600 EMIF_CTLCFG_DENALI_PI_126 Register

1 EMIF_CTLCFG_DENALI_PI_126 Register (Offset = 21F8h) [reset = 0h]

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Table 14-14155. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A1F8h**

Figure 14-4679. EMIF_CTLCFG_DENALI_PI_126 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_1					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_1							
R/W							
0h							

Table 14-14157. EMIF_CTLCFG_DENALI_PI_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_1	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.601 EMIF_CTLCFG_DENALI_PI_127 Register

1 EMIF_CTLCFG_DENALI_PI_127 Register (Offset = 21FCh) [reset = 0h]

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Table 14-14158. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A1FCh

Figure 14-4680. EMIF_CTLCFG_DENALI_PI_127 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_2					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_2							
R/W							
0h							

Table 14-14160. EMIF_CTLCFG_DENALI_PI_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_2	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.602 EMIF_CTLCFG_DENALI_PI_128 Register

1 EMIF_CTLCFG_DENALI_PI_128 Register (Offset = 2200h) [reset = 0h]

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Table 14-14161. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A200h**

Figure 14-4681. EMIF_CTLCFG_DENALI_PI_128 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_3					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_3							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_3							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_3							
R/W							
0h							

Table 14-14163. EMIF_CTLCFG_DENALI_PI_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_3	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.603 EMIF_CTLCFG_DENALI_PI_129 Register

1 EMIF_CTLCFG_DENALI_PI_129 Register (Offset = 2204h) [reset = 0h]

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Table 14-14164. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A204h

Figure 14-4682. EMIF_CTLCFG_DENALI_PI_129 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_4					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_4							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_4							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_4							
R/W							
0h							

Table 14-14166. EMIF_CTLCFG_DENALI_PI_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_4	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.604 EMIF_CTLCFG_DENALI_PI_130 Register

1 EMIF_CTLCFG_DENALI_PI_130 Register (Offset = 2208h) [reset = 0h]

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Table 14-14167. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A208h**

Figure 14-4683. EMIF_CTLCFG_DENALI_PI_130 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_5					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_BIST_STAGE_5							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_BIST_STAGE_5							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_BIST_STAGE_5							
R/W							
0h							

Table 14-14169. EMIF_CTLCFG_DENALI_PI_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_5	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.605 EMIF_CTLCFG_DENALI_PI_131 Register

1 EMIF_CTLCFG_DENALI_PI_131 Register (Offset = 220Ch) [reset = 0h]

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Table 14-14170. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A20Ch**

Figure 14-4684. EMIF_CTLCFG_DENALI_PI_131 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_6					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_6							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_6							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_6							
R/W							
0h							

Table 14-14172. EMIF_CTLCFG_DENALI_PI_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_6	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.606 EMIF_CTLCFG_DENALI_PI_132 Register

1 EMIF_CTLCFG_DENALI_PI_132 Register (Offset = 2210h) [reset = 0h]

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Table 14-14173. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A210h**

Figure 14-4685. EMIF_CTLCFG_DENALI_PI_132 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_BIST_STAGE_7					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PI_BIST_STAGE_7							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_BIST_STAGE_7							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_BIST_STAGE_7							
R/W							
0h							

Table 14-14175. EMIF_CTLCFG_DENALI_PI_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PI_BIST_STAGE_7	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.607 EMIF_CTLCFG_DENALI_PI_133 Register

1 EMIF_CTLCFG_DENALI_PI_133 Register (Offset = 2214h) [reset = 0h]

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Table 14-14176. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A214h**

Figure 14-4686. EMIF_CTLCFG_DENALI_PI_133 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SELF_REFRESH_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_CRC_CALC
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_BG_ROTATE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PI_COL_DIFF			
NONE				R/W			
0h				0h			

Table 14-14178. EMIF_CTLCFG_DENALI_PI_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SELF_REFRESH_EN	R/W	0h	Control for PI to enable self refresh mode. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_CRC_CALC	R/W	0h	Defines where CRC is performed; set to 1 for PI responsibility or clear to 0 for PHY responsibility. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_BG_ROTATE_EN	R/W	0h	Enable bank group rotation. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_COL_DIFF	R/W	0h	Difference between number of column pins available and number being used. Reset Source: ctl_amod_g_rst_n

14.5.1.2.608 EMIF_CTLCFG_DENALI_PI_134 Register

1 EMIF_CTLCFG_DENALI_PI_134 Register (Offset = 2218h) [reset = 0h]

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Table 14-14179. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A218h

Figure 14-4687. EMIF_CTLCFG_DENALI_PI_134 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_SREF_ENTRY_REQ
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_SREFRESH_EXIT_NO_REFRESH
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_PWRUP_SREFRESH_EXIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_MC_PWRUP_SREFRESH_EXIT
NONE							R/W
0h							0h

Table 14-14181. EMIF_CTLCFG_DENALI_PI_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_SREF_ENTRY_REQ	W	0h	In PI power up data retention, PI can issued sref entry command. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_SREFRESH_EXIT_NO_REFRESH	R/W	0h	Disables the automatic refresh request associated with self-refresh exit. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_PWRUP_SREFRESH_EXIT	R/W	0h	PI control powerup via self-refresh instead of full memory initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-14181. EMIF_CTLCFG_DENALI_PI_134 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PI_MC_PWRUP_SREFRESH_EXIT	R/W	0h	It indicates MC control powerup via self-refresh instead of full memory initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.609 EMIF_CTLCFG_DENALI_PI_135 Register

1 EMIF_CTLCFG_DENALI_PI_135 Register (Offset = 221Ch) [reset = 0h]

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Table 14-14182. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A21Ch

Figure 14-4688. EMIF_CTLCFG_DENALI_PI_135 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_NO_AUTO_MRR_INIT
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_NO_PHY_IND_TRAIN_INIT
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_NO_MRW_INIT
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_NO_MRW_BT_INIT
NONE							R/W
0h							0h

Table 14-14184. EMIF_CTLCFG_DENALI_PI_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_NO_AUTO_MRR_INIT	R/W	0h	Disable MRR commands during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_NO_PHY_IND_TRAIN_INIT	R/W	0h	Disable PHY Independent Training during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_NO_MRW_INIT	R/W	0h	Disable MRW commands after training during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_NO_MRW_BT_INIT	R/W	0h	Disable MRW commands before training during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.610 EMIF_CTLCFG_DENALI_PI_136 Register

1 EMIF_CTLCFG_DENALI_PI_136 Register (Offset = 2220h) [reset = 0h]

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Table 14-14185. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A220h**

Figure 14-4689. EMIF_CTLCFG_DENALI_PI_136 Name Register

31	30	29	28	27	26	25	24
PI_TRST_PWRON							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TRST_PWRON							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TRST_PWRON							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TRST_PWRON							
R/W							
0h							

Table 14-14187. EMIF_CTLCFG_DENALI_PI_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TRST_PWRON	R/W	0h	Duration of memory reset during power-on initialization. Reset Source: ctl_amod_g_rst_n

14.5.1.2.611 EMIF_CTLCFG_DENALI_PI_137 Register

1 EMIF_CTLCFG_DENALI_PI_137 Register (Offset = 2224h) [reset = 0h]

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Table 14-14188. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A224h**

Figure 14-4690. EMIF_CTLCFG_DENALI_PI_137 Name Register

31	30	29	28	27	26	25	24
PI_CKE_INACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_CKE_INACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_CKE_INACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_CKE_INACTIVE							
R/W							
0h							

Table 14-14190. EMIF_CTLCFG_DENALI_PI_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_CKE_INACTIVE	R/W	0h	Number of cycles after reset before CKE will be active. Reset Source: ctl_amod_g_rst_n

14.5.1.2.612 EMIF_CTLCFG_DENALI_PI_138 Register

1 EMIF_CTLCFG_DENALI_PI_138 Register (Offset = 2228h) [reset = 0h]

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Table 14-14191. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A228h**

Figure 14-4691. EMIF_CTLCFG_DENALI_PI_138 Name Register

31	30	29	28	27	26	25	24
PI_DLL_RST_DELAY							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_DLL_RST_DELAY							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_DRAM_INIT_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_DLL_RST
NONE							R/W
0h							0h

Table 14-14193. EMIF_CTLCFG_DENALI_PI_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_DLL_RST_DELAY	R/W	0h	Minimum cycles required for DLL reset signal dll_rst_n to be held. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_DRAM_INIT_EN	R/W	0h	Control for the initialization of DRAM by the PI. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_DLL_RST	R/W	0h	Enables use of the DLL reset [dll_rst_n]. Reset Source: ctl_amod_g_rst_n

14.5.1.2.613 EMIF_CTLCFG_DENALI_PI_139 Register

1 EMIF_CTLCFG_DENALI_PI_139 Register (Offset = 222Ch) [reset = 0h]

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Table 14-14194. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A22Ch**

Figure 14-4692. EMIF_CTLCFG_DENALI_PI_139 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_DLL_RST_ADJ_DLY							
R/W							
0h							

Table 14-14196. EMIF_CTLCFG_DENALI_PI_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_DLL_RST_ADJ_DLY	R/W	0h	Minimum cycles after setting controller delay in DLL until the DLL reset signal dll_rst_n may be asserted. Reset Source: ctl_amod_g_rst_n

14.5.1.2.614 EMIF_CTLCFG_DENALI_PI_140 Register

1 EMIF_CTLCFG_DENALI_PI_140 Register (Offset = 2230h) [reset = 0h]

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Table 14-14197. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A230h

Figure 14-4693. EMIF_CTLCFG_DENALI_PI_140 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_WRITE_MODEREG	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_WRITE_MODEREG							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_WRITE_MODEREG							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_WRITE_MODEREG							
R/W							
0h							

Table 14-14199. EMIF_CTLCFG_DENALI_PI_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:0	PI_WRITE_MODEREG	R/W	0h	Write memory mode register data to the DRAMs. Bits [7:0] define the memory mode register number if bit [23] is set, bits [15:8] define the chip select if bit [24] is clear, bits [23:16] define which memory mode register/s to write, bit [24] defines whether all chip selects will be written, and bit [25] triggers the write. Reset Source: ctl_amod_g_rst_n

14.5.1.2.615 EMIF_CTLCFG_DENALI_PI_141 Register

1 EMIF_CTLCFG_DENALI_PI_141 Register (Offset = 2234h) [reset = 0h]

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Table 14-14200. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A234h

Figure 14-4694. EMIF_CTLCFG_DENALI_PI_141 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED 27
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PI_MRW_STATUS							
R							
0h							

Table 14-14202. EMIF_CTLCFG_DENALI_PI_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED27	R/W	0h	Reserved
7:0	PI_MRW_STATUS	R	0h	Write memory mode register status. Bit [0] set indicates a WRITE_MODEREG parameter programming error. Bit [1] set indicates a PASR error. Bit [2] is Reserved. Bit [3] set indicates a self refresh or deep power down error. Bit [4] set indicates that a write to MR3 or MR11 was attempted [write_modereg bit [25] was asserted with bit [17] set, or bit [23] was asserted with bits [7:0] defining MR3 or MR11] during tZQCAL after a ZQ calibration start command. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.616 EMIF_CTLCFG_DENALI_PI_142 Register

1 EMIF_CTLCFG_DENALI_PI_142 Register (Offset = 2238h) [reset = 0h]

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Table 14-14203. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A238h**

Figure 14-4695. EMIF_CTLCFG_DENALI_PI_142 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_READ_MODEREG</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_READ_MODEREG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_READ_MODEREG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14205. EMIF_CTLCFG_DENALI_PI_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_READ_MODEREG	R/W	0h	Read the specified memory mode register from specified chip when start bit set. Bits [7:0] define the memory mode register and bits [15:8] define the chip select. Set bit [16] to 1 to trigger. Reset Source: ctl_amod_g_rst_n

14.5.1.2.617 EMIF_CTLCFG_DENALI_PI_143 Register

1 EMIF_CTLCFG_DENALI_PI_143 Register (Offset = 223Ch) [reset = 0h]

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Table 14-14206. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A23Ch**

Figure 14-4696. EMIF_CTLCFG_DENALI_PI_143 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_NO_ZQ_INIT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_PERIPHERAL_MRR_DATA_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_PERIPHERAL_MRR_DATA_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_PERIPHERAL_MRR_DATA_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14208. EMIF_CTLCFG_DENALI_PI_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_NO_ZQ_INIT	R/W	0h	Disable ZQ operations during initialization. Set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:0	PI_PERIPHERAL_MRR_DATA_0	R	0h	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter, Bits [15:0] define MRR data, [23:16] define the chip select. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.618 EMIF_CTLCFG_DENALI_PI_144 Register

1 EMIF_CTLCFG_DENALI_PI_144 Register (Offset = 2240h) [reset = 0h]

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Table 14-14209. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A240h**

Figure 14-4697. EMIF_CTLCFG_DENALI_PI_144 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED30
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_ZQ_REQ_PENDING
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED29			
NONE				W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED						PI_RESERVED28	
NONE						R/W	
0h						0h	

Table 14-14211. EMIF_CTLCFG_DENALI_PI_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED30	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_ZQ_REQ_PENDING	R	0h	Indicates that a ZQ command is currently in progress or waiting to run. When this is asserted, no writes to ZQ_REQ should occur. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_RESERVED29	W	0h	Reserved
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RESERVED28	R/W	0h	Reserved

14.5.1.2.619 EMIF_CTLCFG_DENALI_PI_145 Register

1 EMIF_CTLCFG_DENALI_PI_145 Register (Offset = 2244h) [reset = 0h]

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Table 14-14212. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A244h**

Figure 14-4698. EMIF_CTLCFG_DENALI_PI_145 Name Register

31	30	29	28	27	26	25	24
PI_MONITOR_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MONITOR_CAP_SEL_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				PI_MONITOR_SRC_SEL_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED					PI_RESERVED31		
NONE					R/W		
0h					0h		

Table 14-14214. EMIF_CTLCFG_DENALI_PI_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MONITOR_0	R	0h	Monitor register 0. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_MONITOR_CAP_SEL_0	R/W	0h	Selection of captures for pi_monitor_0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_MONITOR_SRC_SEL_0	R/W	0h	Selection of sources for pi_monitor_0. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_RESERVED31	R/W	0h	Reserved

14.5.1.2.620 EMIF_CTLCFG_DENALI_PI_146 Register

1 EMIF_CTLCFG_DENALI_PI_146 Register (Offset = 2248h) [reset = 0h]

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Table 14-14215. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A248h**

Figure 14-4699. EMIF_CTLCFG_DENALI_PI_146 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_MONITOR_SRC_SEL_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MONITOR_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_MONITOR_CAP_SEL_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_MONITOR_SRC_SEL_1			
NONE				R/W			
0h				0h			

Table 14-14217. EMIF_CTLCFG_DENALI_PI_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_MONITOR_SRC_SEL_2	R/W	0h	Selection of sources for pi_monitor_2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MONITOR_1	R	0h	Monitor register 1. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_MONITOR_CAP_SEL_1	R/W	0h	Selection of captures for pi_monitor_1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_MONITOR_SRC_SEL_1	R/W	0h	Selection of sources for pi_monitor_1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.621 EMIF_CTLCFG_DENALI_PI_147 Register

1 EMIF_CTLCFG_DENALI_PI_147 Register (Offset = 224Ch) [reset = 0h]

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Table 14-14218. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A24Ch**

Figure 14-4700. EMIF_CTLCFG_DENALI_PI_147 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MONITOR_CAP_SEL_3
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_MONITOR_SRC_SEL_3			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MONITOR_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_MONITOR_CAP_SEL_2
NONE							R/W
0h							0h

Table 14-14220. EMIF_CTLCFG_DENALI_PI_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_MONITOR_CAP_SEL_3	R/W	0h	Selection of captures for pi_monitor_3. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_MONITOR_SRC_SEL_3	R/W	0h	Selection of sources for pi_monitor_3. Reset Source: ctl_amod_g_rst_n
15:8	PI_MONITOR_2	R	0h	Monitor register 2. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_MONITOR_CAP_SEL_2	R/W	0h	Selection of captures for pi_monitor_2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.622 EMIF_CTLCFG_DENALI_PI_148 Register

1 EMIF_CTLCFG_DENALI_PI_148 Register (Offset = 2250h) [reset = 0h]

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Table 14-14221. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A250h**

Figure 14-4701. EMIF_CTLCFG_DENALI_PI_148 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_MONITOR_4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MONITOR_CAP_SEL_4</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_MONITOR_SRC_SEL_4</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MONITOR_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14223. EMIF_CTLCFG_DENALI_PI_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MONITOR_4	R	0h	Monitor register 4. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_MONITOR_CAP_SEL_4	R/W	0h	Selection of captures for pi_monitor_4. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_MONITOR_SRC_SEL_4	R/W	0h	Selection of sources for pi_monitor_4. Reset Source: ctl_amod_g_rst_n
7:0	PI_MONITOR_3	R	0h	Monitor register 3. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.623 EMIF_CTLCFG_DENALI_PI_149 Register

1 EMIF_CTLCFG_DENALI_PI_149 Register (Offset = 2254h) [reset = 0h]

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Table 14-14224. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A254h**

Figure 14-4702. EMIF_CTLCFG_DENALI_PI_149 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_MONITOR_SRC_SEL_6			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MONITOR_5							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_MONITOR_CAP_SEL_5
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_MONITOR_SRC_SEL_5			
NONE				R/W			
0h				0h			

Table 14-14226. EMIF_CTLCFG_DENALI_PI_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_MONITOR_SRC_SEL_6	R/W	0h	Selection of sources for pi_monitor_6. Reset Source: ctl_amod_g_rst_n
23:16	PI_MONITOR_5	R	0h	Monitor register 5. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_MONITOR_CAP_SEL_5	R/W	0h	Selection of captures for pi_monitor_5. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_MONITOR_SRC_SEL_5	R/W	0h	Selection of sources for pi_monitor_5. Reset Source: ctl_amod_g_rst_n

14.5.1.2.624 EMIF_CTLCFG_DENALI_PI_150 Register

1 EMIF_CTLCFG_DENALI_PI_150 Register (Offset = 2258h) [reset = 0h]

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Table 14-14227. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A258h**

Figure 14-4703. EMIF_CTLCFG_DENALI_PI_150 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MONITOR_CAP_SEL_7</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_MONITOR_SRC_SEL_7</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MONITOR_6</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MONITOR_CAP_SEL_6</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14229. EMIF_CTLCFG_DENALI_PI_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_MONITOR_CAP_SEL_7	R/W	0h	Selection of captures for pi_monitor_7. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_MONITOR_SRC_SEL_7	R/W	0h	Selection of sources for pi_monitor_7. Reset Source: ctl_amod_g_rst_n
15:8	PI_MONITOR_6	R	0h	Monitor register 6. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_MONITOR_CAP_SEL_6	R/W	0h	Selection of captures for pi_monitor_6. Reset Source: ctl_amod_g_rst_n

14.5.1.2.625 EMIF_CTLCFG_DENALI_PI_151 Register

1 EMIF_CTLCFG_DENALI_PI_151 Register (Offset = 225Ch) [reset = 0h]

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Table 14-14230. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A25Ch**

Figure 14-4704. EMIF_CTLCFG_DENALI_PI_151 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_MONITOR_7							
R							
0h							

Table 14-14232. EMIF_CTLCFG_DENALI_PI_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_MONITOR_7	R	0h	Monitor register 7. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.626 EMIF_CTLCFG_DENALI_PI_152 Register

1 EMIF_CTLCFG_DENALI_PI_152 Register (Offset = 2260h) [reset = 0h]

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Table 14-14233. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A260h

Figure 14-4705. EMIF_CTLCFG_DENALI_PI_152 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_MONITOR_STROBE							
W							
0h							

Table 14-14235. EMIF_CTLCFG_DENALI_PI_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_MONITOR_STROBE	W	0h	Strobe the pi_monitor once. Every bit corresponds respectively with a pi_monitor. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.627 EMIF_CTLCFG_DENALI_PI_153 Register

1 EMIF_CTLCFG_DENALI_PI_153 Register (Offset = 2264h) [reset = 0h]

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Table 14-14236. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A264h**

Figure 14-4706. EMIF_CTLCFG_DENALI_PI_153 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED32
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_FREQ_RETENTION_NUM				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PI_FREQ_NUMBER_STATUS				
NONE			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PI_DLL_LOCK
NONE							R
0h							0h

Table 14-14238. EMIF_CTLCFG_DENALI_PI_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED32	R/W	0h	Reserved
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_FREQ_RETENTION_NUM	R/W	0h	Monitor active freq number in PI for data_retention Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_FREQ_NUMBER_STATUS	R	0h	Monitor active freq number in PI. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_DLL_LOCK	R	0h	Monitor dfi_init_complete from PHY. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.628 EMIF_CTLCFG_DENALI_PI_154 Register

1 EMIF_CTLCFG_DENALI_PI_154 Register (Offset = 2268h) [reset = 0h]

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Table 14-14239. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A268h

Figure 14-4707. EMIF_CTLCFG_DENALI_PI_154 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED34
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_POWER_REDUC_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED33
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED						PI_PHYMSTR_TYPE	
NONE						R/W	
0h						0h	

Table 14-14241. EMIF_CTLCFG_DENALI_PI_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED34	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_POWER_REDUC_EN	R/W	0h	PI Power reduction enable, 1 = enabled. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED33	R/W	0h	Reserved
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_PHYMSTR_TYPE	R/W	0h	Defines how the controller should set the state of DRAM before turning control of the DFI bus over to the PI. Reset Source: ctl_amod_g_rst_n

14.5.1.2.629 EMIF_CTLCFG_DENALI_PI_155 Register

1 EMIF_CTLCFG_DENALI_PI_155 Register (Offset = 226Ch) [reset = 0h]

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Table 14-14242. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A26Ch**

Figure 14-4708. EMIF_CTLCFG_DENALI_PI_155 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED38
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RESERVED37
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED36
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RESERVED35
NONE							R/W
0h							0h

Table 14-14244. EMIF_CTLCFG_DENALI_PI_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED38	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_RESERVED37	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED36	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED35	R/W	0h	Reserved

14.5.1.2.630 EMIF_CTLCFG_DENALI_PI_156 Register

1 EMIF_CTLCFG_DENALI_PI_156 Register (Offset = 2270h) [reset = 0h]

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Table 14-14245. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A270h**

Figure 14-4709. EMIF_CTLCFG_DENALI_PI_156 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED42
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RESERVED41
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED40
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RESERVED39
NONE							R/W
0h							0h

Table 14-14247. EMIF_CTLCFG_DENALI_PI_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED42	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_RESERVED41	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED40	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED39	R/W	0h	Reserved

14.5.1.2.631 EMIF_CTLCFG_DENALI_PI_157 Register

1 EMIF_CTLCFG_DENALI_PI_157 Register (Offset = 2274h) [reset = 0h]

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Table 14-14248. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A274h

Figure 14-4710. EMIF_CTLCFG_DENALI_PI_157 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED46
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RESERVED45
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED44
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RESERVED43
NONE							R/W
0h							0h

Table 14-14250. EMIF_CTLCFG_DENALI_PI_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED46	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_RESERVED45	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED44	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED43	R/W	0h	Reserved

14.5.1.2.632 EMIF_CTLCFG_DENALI_PI_158 Register

1 EMIF_CTLCFG_DENALI_PI_158 Register (Offset = 2278h) [reset = 0h]

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Table 14-14251. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A278h**

Figure 14-4711. EMIF_CTLCFG_DENALI_PI_158 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_RESERVED 50
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_RESERVED 49
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_RESERVED 48
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_RESERVED 47
NONE							R/W
0h							0h

Table 14-14253. EMIF_CTLCFG_DENALI_PI_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_RESERVED50	R/W	0h	Reserved
23:17	RESERVED	NONE	0h	Reserved
16	PI_RESERVED49	R/W	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED48	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED47	R/W	0h	Reserved

14.5.1.2.633 EMIF_CTLCFG_DENALI_PI_159 Register

1 EMIF_CTLCFG_DENALI_PI_159 Register (Offset = 227Ch) [reset = 0h]

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Table 14-14254. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A27Ch**

Figure 14-4712. EMIF_CTLCFG_DENALI_PI_159 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_WRLVL_MAX_STROBE_PEND</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RESERVED52</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_RESERVED51</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14256. EMIF_CTLCFG_DENALI_PI_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_WRLVL_MAX_STROBE_PEND	R/W	0h	Defines the maximum number of wrlvl_strobes that be accumulated before an AREF is prevented from being generated. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_RESERVED52	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_RESERVED51	R/W	0h	Reserved

14.5.1.2.634 EMIF_CTLCFG_DENALI_PI_160 Register

1 EMIF_CTLCFG_DENALI_PI_160 Register (Offset = 2280h) [reset = 0h]

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Table 14-14257. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A280h**

Figure 14-4713. EMIF_CTLCFG_DENALI_PI_160 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PI_TREFBW_THR
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PI_TREFBW_THR							
R/W							
0h							

Table 14-14259. EMIF_CTLCFG_DENALI_PI_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PI_TREFBW_THR	R/W	0h	Threshold value to control the AREF command interval. When the number of pending AREF is over this value, the interval is expanded to be tREF/8. Reset Source: ctl_amod_g_rst_n

14.5.1.2.635 EMIF_CTLCFG_DENALI_PI_161 Register

1 EMIF_CTLCFG_DENALI_PI_161 Register (Offset = 2284h) [reset = 0h]

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Table 14-14260. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A284h

Figure 14-4714. EMIF_CTLCFG_DENALI_PI_161 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PI_FREQ_CHANGE_REG_COPY				
NONE			R/W				
0h			0h				

Table 14-14262. EMIF_CTLCFG_DENALI_PI_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	PI_FREQ_CHANGE_REG_COPY	R/W	0h	In non-DFI 4.0 mode, contains the frequency copy value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.636 EMIF_CTLCFG_DENALI_PI_162 Register

1 EMIF_CTLCFG_DENALI_PI_162 Register (Offset = 2288h) [reset = 0h]

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Table 14-14263. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A288h**

Figure 14-4715. EMIF_CTLCFG_DENALI_PI_162 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_NO_CATR_READ
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PI_CATR	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED			PI_RESERVED53				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED							PI_FREQ_SEL_FROM_REGIF
NONE							R/W
0h							0h

Table 14-14265. EMIF_CTLCFG_DENALI_PI_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_NO_CATR_READ	R/W	0h	Defines how the LPDDR4 termination status is determined. 1: PI use PI_CATR to get DRAM CA Termination status. 0: PI reads DRAM MR0.OP7 to get DRAM CA Termination status. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_CATR	R/W	0h	It indicates LP4 DRAM CA terminition ON/OFF state. Each bit corresponds to each chip select. 1:ON 0:OFF. This parameter is active when PI_NO_CATR_READ==1. When PI_NO_CATR_READ==0, this param is inactive Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_RESERVED53	R/W	0h	Reserved
7:1	RESERVED	NONE	0h	Reserved
0	PI_FREQ_SEL_FROM_REGIF	R/W	0h	In non-DFI 4.0 mode, user select the frequency copies from pi_freq_change_reg_copy. Reset Source: ctl_amod_g_rst_n

14.5.1.2.637 EMIF_CTLCFG_DENALI_PI_163 Register

1 EMIF_CTLCFG_DENALI_PI_163 Register (Offset = 228Ch) [reset = 0h]

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Table 14-14266. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A28Ch

Figure 14-4716. EMIF_CTLCFG_DENALI_PI_163 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_NOTCARE_MC_INIT_START
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PI_DISABLE_PHYMSTR_REQ
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PI_DISCONNECT_MC
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PI_MASK_INIT_COMPLETE
NONE							R/W
0h							0h

Table 14-14268. EMIF_CTLCFG_DENALI_PI_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_NOTCARE_MC_INIT_START	R/W	0h	Defines whether PI waits for the controller to initiate dfi_init_start before PI memory initialization, 1: wait for dfi_init_start Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PI_DISABLE_PHYMSTR_REQ	R/W	0h	PI mask dfi_phymstr_req to the controller and get dfi bus without dfi_phymstr_ack, 1: disconnect Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_DISCONNECT_MC	R/W	0h	PI disconnects the controller from the PHY, 1: disconnect Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PI_MASK_INIT_COMPLETE	R/W	0h	Enable the masking of the dfi_init_complete signal back to the controller, 1: mask. Reset Source: ctl_amod_g_rst_n

14.5.1.2.638 EMIF_CTLCFG_DENALI_PI_164 Register

1 EMIF_CTLCFG_DENALI_PI_164 Register (Offset = 2290h) [reset = 0h]

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Table 14-14269. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A290h

Figure 14-4717. EMIF_CTLCFG_DENALI_PI_164 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TVREF_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TVREF_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED					PI_PHYMSTR_REQ_ACK_LOOP_DELAY		
NONE					R/W		
0h					0h		

Table 14-14271. EMIF_CTLCFG_DENALI_PI_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	PI_TVREF_F0	R/W	0h	Defines the number of cycles that the PI should wait before issuing the next command after a VREF training MRW command for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PI_PHYMSTR_REQ_ACK_LOOP_DELAY	R/W	0h	The delay between phymstr_req and inner phymstr_ack when PI_DISABLE_PHYMSTR_REQ set 1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.639 EMIF_CTLCFG_DENALI_PI_165 Register

1 EMIF_CTLCFG_DENALI_PI_165 Register (Offset = 2294h) [reset = 0h]

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Table 14-14272. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A294h**

Figure 14-4718. EMIF_CTLCFG_DENALI_PI_165 Name Register

31	30	29	28	27	26	25	24
PI_TVREF_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TVREF_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TVREF_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TVREF_F1							
R/W							
0h							

Table 14-14274. EMIF_CTLCFG_DENALI_PI_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TVREF_F2	R/W	0h	Defines the number of cycles that the PI should wait before issuing the next command after a VREF training MRW command for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:0	PI_TVREF_F1	R/W	0h	Defines the number of cycles that the PI should wait before issuing the next command after a VREF training MRW command for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.640 EMIF_CTLCFG_DENALI_PI_166 Register

1 EMIF_CTLCFG_DENALI_PI_166 Register (Offset = 2298h) [reset = 0h]

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Table 14-14275. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A298h

Figure 14-4719. EMIF_CTLCFG_DENALI_PI_166 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TSDO_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TSDO_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TSDO_F0							
R/W							
0h							

Table 14-14277. EMIF_CTLCFG_DENALI_PI_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_TSDO_F2	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 2, in PI clocks Reset Source: ctl_amod_g_rst_n
15:8	PI_TSDO_F1	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 1, in PI clocks Reset Source: ctl_amod_g_rst_n
7:0	PI_TSDO_F0	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 0, in PI clocks Reset Source: ctl_amod_g_rst_n

14.5.1.2.641 EMIF_CTLCFG_DENALI_PI_167 Register

1 EMIF_CTLCFG_DENALI_PI_167 Register (Offset = 229Ch) [reset = 0h]

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Table 14-14278. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A29Ch

Figure 14-4720. EMIF_CTLCFG_DENALI_PI_167 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_TDELAY_RDWR_2_BUS_IDLE_F0							
R/W							
0h							

Table 14-14280. EMIF_CTLCFG_DENALI_PI_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_TDELAY_RDWR_2_BUS_IDLE_F0	R/W	0h	The delay from read or write to bus idle for frequency set 0. Recommend setting is: delay time from read command issued to last read data received. Reset Source: ctl_amod_g_rst_n

14.5.1.2.642 EMIF_CTLCFG_DENALI_PI_168 Register

1 EMIF_CTLCFG_DENALI_PI_168 Register (Offset = 22A0h) [reset = 0h]

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Table 14-14281. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2A0h**

Figure 14-4721. EMIF_CTLCFG_DENALI_PI_168 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PI_TDELAY_RDWR_2_BUS_IDLE_F1							
R/W							
0h							

Table 14-14283. EMIF_CTLCFG_DENALI_PI_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PI_TDELAY_RDWR_2_BUS_IDLE_F1	R/W	0h	The delay from read or write to bus idle for frequency set 1. Recommend setting is: delay time from read command issued to last read data received. Reset Source: ctl_amod_g_rst_n

14.5.1.2.643 EMIF_CTLCFG_DENALI_PI_169 Register

1 EMIF_CTLCFG_DENALI_PI_169 Register (Offset = 22A4h) [reset = 0h]

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Table 14-14284. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2A4h**

Figure 14-4722. EMIF_CTLCFG_DENALI_PI_169 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_ZQINIT_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_ZQINIT_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDELAY_RDWR_2_BUS_IDLE_F2							
R/W							
0h							

Table 14-14286. EMIF_CTLCFG_DENALI_PI_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	PI_ZQINIT_F0	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_TDELAY_RDWR_2_BUS_IDLE_F2	R/W	0h	The delay from read or write to bus idle for frequency set 2. Recommend setting is: delay time from read command issued to last read data received. Reset Source: ctl_amod_g_rst_n

14.5.1.2.644 EMIF_CTLCFG_DENALI_PI_170 Register

1 EMIF_CTLCFG_DENALI_PI_170 Register (Offset = 22A8h) [reset = 0h]

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Table 14-14287. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2A8h**

Figure 14-4723. EMIF_CTLCFG_DENALI_PI_170 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_ZQINIT_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PI_ZQINIT_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PI_ZQINIT_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PI_ZQINIT_F1							
R/W							
0h							

Table 14-14289. EMIF_CTLCFG_DENALI_PI_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_ZQINIT_F2	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_ZQINIT_F1	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.645 EMIF_CTLCFG_DENALI_PI_171 Register

1 EMIF_CTLCFG_DENALI_PI_171 Register (Offset = 22ACh) [reset = 0h]

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Table 14-14290. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2ACh**

Figure 14-4724. EMIF_CTLCFG_DENALI_PI_171 Name Register

31	30	29	28	27	26	25	24
PI_TPARITY_ERROR_CMD_INHIBIT_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_CA_PARITY_LAT_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PI_ADDITIVE_LAT_F0					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PI_WRLAT_F0						
NONE	R/W						
0h	0h						

Table 14-14292. EMIF_CTLCFG_DENALI_PI_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TPARITY_ERROR_CMD_INHIBIT_F0	R/W	0h	Defines the window after the PI receives a parity error during which DRAM commands will not execute for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_CA_PARITY_LAT_F0	R/W	0h	DRAM CA parity latency value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_ADDITIVE_LAT_F0	R/W	0h	DRAM additive latency value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_WRLAT_F0	R/W	0h	DRAM WRLAT value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.646 EMIF_CTLCFG_DENALI_PI_172 Register

1 EMIF_CTLCFG_DENALI_PI_172 Register (Offset = 22B0h) [reset = 0h]

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Table 14-14293. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2B0h**

Figure 14-4725. EMIF_CTLCFG_DENALI_PI_172 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_CA_PARITY_LAT_F1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PI_ADDITIVE_LAT_F1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PI_WRLAT_F1						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PI_CASLAT_LIN_F0						
NONE	R/W						
0h	0h						

Table 14-14295. EMIF_CTLCFG_DENALI_PI_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_CA_PARITY_LAT_F1	R/W	0h	DRAM CA parity latency value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_ADDITIVE_LAT_F1	R/W	0h	DRAM additive latency value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_WRLAT_F1	R/W	0h	DRAM WRLAT value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_CASLAT_LIN_F0	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 0. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. Reset Source: ctl_amod_g_rst_n

14.5.1.2.647 EMIF_CTLCFG_DENALI_PI_173 Register

1 EMIF_CTLCFG_DENALI_PI_173 Register (Offset = 22B4h) [reset = 0h]

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Table 14-14296. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2B4h**

Figure 14-4726. EMIF_CTLCFG_DENALI_PI_173 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_ADDITIVE_LAT_F2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PI_WRLAT_F2						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PI_CASLAT_LIN_F1						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TPARITY_ERROR_CMD_INHIBIT_F1							
R/W							
0h							

Table 14-14298. EMIF_CTLCFG_DENALI_PI_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_ADDITIVE_LAT_F2	R/W	0h	DRAM additive latency value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_WRLAT_F2	R/W	0h	DRAM WRLAT value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_CASLAT_LIN_F1	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 1. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. Reset Source: ctl_amod_g_rst_n
7:0	PI_TPARITY_ERROR_CMD_INHIBIT_F1	R/W	0h	Defines the window after the PI receives a parity error during which DRAM commands will not execute for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.648 EMIF_CTLCFG_DENALI_PI_174 Register

1 EMIF_CTLCFG_DENALI_PI_174 Register (Offset = 22B8h) [reset = 0h]

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Table 14-14299. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2B8h**

Figure 14-4727. EMIF_CTLCFG_DENALI_PI_174 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PI_CASLAT_LIN_F2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
PI_TPARITY_ERROR_CMD_INHIBIT_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				PI_CA_PARITY_LAT_F2			
NONE				R/W			
0h				0h			

Table 14-14301. EMIF_CTLCFG_DENALI_PI_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PI_CASLAT_LIN_F2	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 2. Bit [0] is half-cycle increment and the upper bits define memory CAS latency for the controller. Reset Source: ctl_amod_g_rst_n
15:8	PI_TPARITY_ERROR_CMD_INHIBIT_F2	R/W	0h	Defines the window after the PI receives a parity error during which DRAM commands will not execute for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_CA_PARITY_LAT_F2	R/W	0h	DRAM CA parity latency value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.649 EMIF_CTLCFG_DENALI_PI_175 Register

1 EMIF_CTLCFG_DENALI_PI_175 Register (Offset = 22BCh) [reset = 0h]

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Table 14-14302. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2BCh**

Figure 14-4728. EMIF_CTLCFG_DENALI_PI_175 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TRFC_F0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TRFC_F0							
R/W							
0h							

Table 14-14304. EMIF_CTLCFG_DENALI_PI_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PI_TRFC_F0	R/W	0h	DRAM tRFC value in memory clocks for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.650 EMIF_CTLCFG_DENALI_PI_176 Register

1 EMIF_CTLCFG_DENALI_PI_176 Register (Offset = 22C0h) [reset = 0h]

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Table 14-14305. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2C0h**

Figure 14-4729. EMIF_CTLCFG_DENALI_PI_176 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_TREF_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TREF_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TREF_F0							
R/W							
0h							

Table 14-14307. EMIF_CTLCFG_DENALI_PI_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TREF_F0	R/W	0h	DRAM tREF value in memory clocks for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.651 EMIF_CTLCFG_DENALI_PI_177 Register

1 EMIF_CTLCFG_DENALI_PI_177 Register (Offset = 22C4h) [reset = 0h]

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Table 14-14308. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2C4h**

Figure 14-4730. EMIF_CTLCFG_DENALI_PI_177 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_TRFC_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TRFC_F1							
R/W							
0h							

Table 14-14310. EMIF_CTLCFG_DENALI_PI_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PI_TRFC_F1	R/W	0h	DRAM tRFC value in memory clocks for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.652 EMIF_CTLCFG_DENALI_PI_178 Register

1 EMIF_CTLCFG_DENALI_PI_178 Register (Offset = 22C8h) [reset = 0h]

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Table 14-14311. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A2C8h

Figure 14-4731. EMIF_CTLCFG_DENALI_PI_178 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TREF_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_TREF_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TREF_F1							
R/W							
0h							

Table 14-14313. EMIF_CTLCFG_DENALI_PI_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TREF_F1	R/W	0h	DRAM tREF value in memory clocks for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.653 EMIF_CTLCFG_DENALI_PI_179 Register

1 EMIF_CTLCFG_DENALI_PI_179 Register (Offset = 22CCh) [reset = 0h]

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Table 14-14314. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2CCh**

Figure 14-4732. EMIF_CTLCFG_DENALI_PI_179 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_TRFC_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TRFC_F2							
R/W							
0h							

Table 14-14316. EMIF_CTLCFG_DENALI_PI_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PI_TRFC_F2	R/W	0h	DRAM tRFC value in memory clocks for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.654 EMIF_CTLCFG_DENALI_PI_180 Register

1 EMIF_CTLCFG_DENALI_PI_180 Register (Offset = 22D0h) [reset = 2000000h]

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Table 14-14317. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2D0h**

Figure 14-4733. EMIF_CTLCFG_DENALI_PI_180 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TDFI_CTRL_DELAY_F0			
NONE				R/W			
0h				2h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_TREF_F2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TREF_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TREF_F2							
R/W							
0h							

Table 14-14319. EMIF_CTLCFG_DENALI_PI_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_TDFI_CTRL_DELAY_F0	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks] for frequency set 0, the delay between a DFI command change and a memory command. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	PI_TREF_F2	R/W	0h	DRAM tREF value in memory clocks for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.655 EMIF_CTLCFG_DENALI_PI_181 Register

1 EMIF_CTLCFG_DENALI_PI_181 Register (Offset = 22D4h) [reset = 202h]

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Table 14-14320. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A2D4h

Figure 14-4734. EMIF_CTLCFG_DENALI_PI_181 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_WRLVL_EN_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_WRLVL_EN_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TDFI_CTRL_DELAY_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TDFI_CTRL_DELAY_F1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
</table>

Table 14-14322. EMIF_CTLCFG_DENALI_PI_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_WRLVL_EN_F1	R/W	0h	Enable the PI write leveling module for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_WRLVL_EN_F0	R/W	0h	Enable the PI write leveling module for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TDFI_CTRL_DELAY_F2	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks] for frequency set 2, the delay between a DFI command change and a memory command. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_TDFI_CTRL_DELAY_F1	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter [in DFI clocks] for frequency set 1, the delay between a DFI command change and a memory command. Reset Source: ctl_amod_g_rst_n

14.5.1.2.656 EMIF_CTLCFG_DENALI_PI_182 Register

1 EMIF_CTLCFG_DENALI_PI_182 Register (Offset = 22D8h) [reset = 0h]

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Table 14-14323. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2D8h**

Figure 14-4735. EMIF_CTLCFG_DENALI_PI_182 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_WRLVL_WW_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_WRLVL_WW_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_WRLVL_EN_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14325. EMIF_CTLCFG_DENALI_PI_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PI_TDFI_WRLVL_WW_F0	R/W	0h	Defines the DFI tWRLVL_WW timing parameter [in DFI clocks] for frequency set 0, the minimum cycles between dfi_wrlvl_strobe assertions. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_WRLVL_EN_F2	R/W	0h	Enable the PI write leveling module for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.657 EMIF_CTLCFG_DENALI_PI_183 Register

1 EMIF_CTLCFG_DENALI_PI_183 Register (Offset = 22DCh) [reset = 0h]

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Table 14-14326. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2DCh**

Figure 14-4736. EMIF_CTLCFG_DENALI_PI_183 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_WRLVL_WW_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TDFI_WRLVL_WW_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_WRLVL_WW_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_WRLVL_WW_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14328. EMIF_CTLCFG_DENALI_PI_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_WRLVL_WW_F2	R/W	0h	Defines the DFI tWRLVL_WW timing parameter [in DFI clocks] for frequency set 2, the minimum cycles between dfi_wrlvl_strobe assertions. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WRLVL_WW_F1	R/W	0h	Defines the DFI tWRLVL_WW timing parameter [in DFI clocks] for frequency set 1, the minimum cycles between dfi_wrlvl_strobe assertions. Reset Source: ctl_amod_g_rst_n

14.5.1.2.658 EMIF_CTLCFG_DENALI_PI_184 Register

1 EMIF_CTLCFG_DENALI_PI_184 Register (Offset = 22E0h) [reset = 0h]

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Table 14-14329. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2E0h**

Figure 14-4737. EMIF_CTLCFG_DENALI_PI_184 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_ODT_EN_F1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TODTL_2CMD_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_ODT_EN_F0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TODTL_2CMD_F0							
R/W							
0h							

Table 14-14331. EMIF_CTLCFG_DENALI_PI_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PI_ODT_EN_F1	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_TODTL_2CMD_F1	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_ODT_EN_F0	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_TODTL_2CMD_F0	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.659 EMIF_CTLCFG_DENALI_PI_185 Register

1 EMIF_CTLCFG_DENALI_PI_185 Register (Offset = 22E4h) [reset = 0h]

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Table 14-14332. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2E4h**

Figure 14-4738. EMIF_CTLCFG_DENALI_PI_185 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TODTON_MIN_F0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_ODTLON_F0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PI_ODT_EN_F2
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TODTL_2CMD_F2							
R/W							
0h							

Table 14-14334. EMIF_CTLCFG_DENALI_PI_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_TODTON_MIN_F0	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_ODTLON_F0	R/W	0h	Defines the latency from a CAS-2 command to the tODTon reference for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PI_ODT_EN_F2	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_TODTL_2CMD_F2	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.660 EMIF_CTLCFG_DENALI_PI_186 Register

1 EMIF_CTLCFG_DENALI_PI_186 Register (Offset = 22E8h) [reset = 0h]

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Table 14-14335. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A2E8h

Figure 14-4739. EMIF_CTLCFG_DENALI_PI_186 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TODTON_MIN_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_ODTLON_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TODTON_MIN_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PI_ODTLON_F1			
NONE				R/W			
0h				0h			

Table 14-14337. EMIF_CTLCFG_DENALI_PI_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_TODTON_MIN_F2	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_ODTLON_F2	R/W	0h	Defines the latency from a CAS-2 command to the tODTon reference for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TODTON_MIN_F1	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_ODTLON_F1	R/W	0h	Defines the latency from a CAS-2 command to the tODTon reference for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.661 EMIF_CTLCFG_DENALI_PI_187 Register

1 EMIF_CTLCFG_DENALI_PI_187 Register (Offset = 22ECh) [reset = 0h]

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Table 14-14338. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 A2ECh**

Figure 14-4740. EMIF_CTLCFG_DENALI_PI_187 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_RD_TO_ODTH_F0					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		PI_WR_TO_ODTH_F2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED		PI_WR_TO_ODTH_F1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PI_WR_TO_ODTH_F0					
NONE		R/W					
0h		0h					

Table 14-14340. EMIF_CTLCFG_DENALI_PI_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_RD_TO_ODTH_F0	R/W	0h	Defines the delay from a read command to ODT assertion for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_WR_TO_ODTH_F2	R/W	0h	Defines the delay from a write command to ODT assertion for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_WR_TO_ODTH_F1	R/W	0h	Defines the delay from a write command to ODT assertion for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_WR_TO_ODTH_F0	R/W	0h	Defines the delay from a write command to ODT assertion for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.662 EMIF_CTLCFG_DENALI_PI_188 Register

1 EMIF_CTLCFG_DENALI_PI_188 Register (Offset = 22F0h) [reset = 0h]

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Table 14-14341. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A2F0h

Figure 14-4741. EMIF_CTLCFG_DENALI_PI_188 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_GATE_EN_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_EN_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED		PI_RD_TO_ODTH_F2					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PI_RD_TO_ODTH_F1					
NONE		R/W					
0h		0h					

Table 14-14343. EMIF_CTLCFG_DENALI_PI_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_GATE_EN_F0	R/W	0h	Enable the PI gate training module for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_EN_F0	R/W	0h	Enable the PI data eye training module for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_RD_TO_ODTH_F2	R/W	0h	Defines the delay from a read command to ODT assertion for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_RD_TO_ODTH_F1	R/W	0h	Defines the delay from a read command to ODT assertion for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.663 EMIF_CTLCFG_DENALI_PI_189 Register

1 EMIF_CTLCFG_DENALI_PI_189 Register (Offset = 22F4h) [reset = 0h]

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Table 14-14344. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A2F4h

Figure 14-4742. EMIF_CTLCFG_DENALI_PI_189 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_GATE_EN_F2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_RDLVL_EN_F2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_RDLVL_GATE_EN_F1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_RDLVL_EN_F1	
NONE						R/W	
0h						0h	

Table 14-14346. EMIF_CTLCFG_DENALI_PI_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_GATE_EN_F2	R/W	0h	Enable the PI gate training module for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_EN_F2	R/W	0h	Enable the PI data eye training module for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_GATE_EN_F1	R/W	0h	Enable the PI gate training module for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_EN_F1	R/W	0h	Enable the PI data eye training module for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.664 EMIF_CTLCFG_DENALI_PI_190 Register

1 EMIF_CTLCFG_DENALI_PI_190 Register (Offset = 22F8h) [reset = 0h]

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Table 14-14347. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A2F8h**

Figure 14-4743. EMIF_CTLCFG_DENALI_PI_190 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_PAT0_EN_F0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TWR_MPR_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TWR_MPR_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TWR_MPR_F0							
R/W							
0h							

Table 14-14349. EMIF_CTLCFG_DENALI_PI_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_PAT0_EN_F0	R/W	0h	Enable PATTERN-0 for read training for frequency set 0. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
23:16	PI_TWR_MPR_F2	R/W	0h	Number of cycles after MPR write command and before any other command for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_TWR_MPR_F1	R/W	0h	Number of cycles after MPR write command and before any other command for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_TWR_MPR_F0	R/W	0h	Number of cycles after MPR write command and before any other command for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.665 EMIF_CTLCFG_DENALI_PI_191 Register

1 EMIF_CTLCFG_DENALI_PI_191 Register (Offset = 22FCh) [reset = 0h]

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Table 14-14350. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A2FCh

Figure 14-4744. EMIF_CTLCFG_DENALI_PI_191 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_PAT0_EN_F1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_MULTI_EN_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_DFE_EN_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_RXCAL_EN_F0	
NONE						R/W	
0h						0h	

Table 14-14352. EMIF_CTLCFG_DENALI_PI_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_PAT0_EN_F1	R/W	0h	Enable PATTERN-0 for read training for frequency set 1. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_MULTI_EN_F0	R/W	0h	Enable Multi-pattern [from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM] for read training for frequency set 0. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_DFE_EN_F0	R/W	0h	Enable DFE [PATTERN 8,9] for read training for frequency set 0. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_RXCAL_EN_F0	R/W	0h	Enable RX Offset calibration [PATTERN 14,15] for read training for frequency set 0. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n

14.5.1.2.666 EMIF_CTLCFG_DENALI_PI_192 Register

1 EMIF_CTLCFG_DENALI_PI_192 Register (Offset = 2300h) [reset = 0h]

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Table 14-14353. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A300h**

Figure 14-4745. EMIF_CTLCFG_DENALI_PI_192 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_PAT0_EN_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_MULTI_EN_F1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_DFE_EN_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_RXCAL_EN_F1	
NONE						R/W	
0h						0h	

Table 14-14355. EMIF_CTLCFG_DENALI_PI_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RDLVL_PAT0_EN_F2	R/W	0h	Enable PATTERN-0 for read training for frequency set 2. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_MULTI_EN_F1	R/W	0h	Enable Multi-pattern [from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM] for read training for frequency set 1. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_DFE_EN_F1	R/W	0h	Enable DFE [PATTERN 8,9] for read training for frequency set 1. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_RXCAL_EN_F1	R/W	0h	Enable RX Offset calibration [PATTERN 14,15] for read training for frequency set 1. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n

14.5.1.2.667 EMIF_CTLCFG_DENALI_PI_193 Register

1 EMIF_CTLCFG_DENALI_PI_193 Register (Offset = 2304h) [reset = 0h]

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Table 14-14356. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A304h**

Figure 14-4746. EMIF_CTLCFG_DENALI_PI_193 Name Register

31	30	29	28	27	26	25	24
PI_RDLAT_ADJ_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_RDLVL_MULTI_EN_F2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_RDLVL_DFE_EN_F2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_RDLVL_RXCAL_EN_F2	
NONE						R/W	
0h						0h	

Table 14-14358. EMIF_CTLCFG_DENALI_PI_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_RDLAT_ADJ_F0	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RDLVL_MULTI_EN_F2	R/W	0h	Enable Multi-pattern [from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM] for read training for frequency set 2. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_RDLVL_DFE_EN_F2	R/W	0h	Enable DFE [PATTERN 8,9] for read training for frequency set 2. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RDLVL_RXCAL_EN_F2	R/W	0h	Enable RX Offset calibration [PATTERN 14,15] for read training for frequency set 2. bit1 for normal; bit0 for initialization. Reset Source: ctl_amod_g_rst_n

14.5.1.2.668 EMIF_CTLCFG_DENALI_PI_194 Register

1 EMIF_CTLCFG_DENALI_PI_194 Register (Offset = 2308h) [reset = 0h]

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Table 14-14359. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A308h

Figure 14-4747. EMIF_CTLCFG_DENALI_PI_194 Name Register

31	30	29	28	27	26	25	24
PI_WRLAT_ADJ_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_WRLAT_ADJ_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_RDLAT_ADJ_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_RDLAT_ADJ_F1							
R/W							
0h							

Table 14-14361. EMIF_CTLCFG_DENALI_PI_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_WRLAT_ADJ_F1	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_WRLAT_ADJ_F0	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_RDLAT_ADJ_F2	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_RDLAT_ADJ_F1	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.669 EMIF_CTLCFG_DENALI_PI_195 Register

1 EMIF_CTLCFG_DENALI_PI_195 Register (Offset = 230Ch) [reset = 0h]

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Table 14-14362. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A30Ch

Figure 14-4748. EMIF_CTLCFG_DENALI_PI_195 Name Register

31	30	29	28	27	26	25	24
RESERVED					PI_TDFI_PHY_WRDATA_F2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PI_TDFI_PHY_WRDATA_F1		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PI_TDFI_PHY_WRDATA_F0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_WRLAT_ADJ_F2							
R/W							
0h							

Table 14-14364. EMIF_CTLCFG_DENALI_PI_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PI_TDFI_PHY_WRDATA_F2	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks] for frequency set 2, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PI_TDFI_PHY_WRDATA_F1	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks] for frequency set 1, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PI_TDFI_PHY_WRDATA_F0	R/W	0h	Defines the DFI tPHY_WRDATA timing parameter [in DFI PHY clocks] for frequency set 0, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal. Reset Source: ctl_amod_g_rst_n
7:0	PI_WRLAT_ADJ_F2	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.670 EMIF_CTLCFG_DENALI_PI_196 Register

1 EMIF_CTLCFG_DENALI_PI_196 Register (Offset = 2310h) [reset = 0h]

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Table 14-14365. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A310h

Figure 14-4749. EMIF_CTLCFG_DENALI_PI_196 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TDFI_CALVL_CAPTURE_F0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDFI_CALVL_CAPTURE_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TDFI_CALVL_CC_F0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_CALVL_CC_F0							
R/W							
0h							

Table 14-14367. EMIF_CTLCFG_DENALI_PI_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_CALVL_CAPTURE_F0	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter [in DFI clocks] for frequency set 0, the minimum cycles between a calibration command and a dfi_calvl_capture pulse. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_CALVL_CC_F0	R/W	0h	Defines the DFI tCALVL_CC timing parameter [in DFI clocks] for frequency set 0, the minimum cycles between calibration commands. Reset Source: ctl_amod_g_rst_n

14.5.1.2.671 EMIF_CTLCFG_DENALI_PI_197 Register

1 EMIF_CTLCFG_DENALI_PI_197 Register (Offset = 2314h) [reset = 0h]

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Table 14-14368. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A314h**

Figure 14-4750. EMIF_CTLCFG_DENALI_PI_197 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_CALVL_CAPTURE_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TDFI_CALVL_CAPTURE_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_CALVL_CC_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_CALVL_CC_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14370. EMIF_CTLCFG_DENALI_PI_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_CALVL_CAPTURE_F1	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter [in DFI clocks] for frequency set 1, the minimum cycles between a calibration command and a dfi_calvl_capture pulse. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_CALVL_CC_F1	R/W	0h	Defines the DFI tCALVL_CC timing parameter [in DFI clocks] for frequency set 1, the minimum cycles between calibration commands. Reset Source: ctl_amod_g_rst_n

14.5.1.2.672 EMIF_CTLCFG_DENALI_PI_198 Register

1 EMIF_CTLCFG_DENALI_PI_198 Register (Offset = 2318h) [reset = 0h]

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Table 14-14371. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A318h**

Figure 14-4751. EMIF_CTLCFG_DENALI_PI_198 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TDFI_CALVL_CAPTURE_F2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDFI_CALVL_CAPTURE_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TDFI_CALVL_CC_F2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_CALVL_CC_F2							
R/W							
0h							

Table 14-14373. EMIF_CTLCFG_DENALI_PI_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_CALVL_CAPTURE_F2	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter [in DFI clocks] for frequency set 2, the minimum cycles between a calibration command and a dfi_calvl_capture pulse. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_CALVL_CC_F2	R/W	0h	Defines the DFI tCALVL_CC timing parameter [in DFI clocks] for frequency set 2, the minimum cycles between calibration commands. Reset Source: ctl_amod_g_rst_n

14.5.1.2.673 EMIF_CTLCFG_DENALI_PI_199 Register

1 EMIF_CTLCFG_DENALI_PI_199 Register (Offset = 231Ch) [reset = 0h]

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Table 14-14374. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A31Ch**

Figure 14-4752. EMIF_CTLCFG_DENALI_PI_199 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_TMRZ_F0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED						PI_CALVL_EN_F2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_CALVL_EN_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_CALVL_EN_F0	
NONE						R/W	
0h						0h	

Table 14-14376. EMIF_CTLCFG_DENALI_PI_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TMRZ_F0	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_CALVL_EN_F2	R/W	0h	Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 2. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_CALVL_EN_F1	R/W	0h	Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 1. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_CALVL_EN_F0	R/W	0h	Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 0. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.674 EMIF_CTLCFG_DENALI_PI_200 Register

1 EMIF_CTLCFG_DENALI_PI_200 Register (Offset = 2320h) [reset = 0h]

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Table 14-14377. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A320h**

Figure 14-4753. EMIF_CTLCFG_DENALI_PI_200 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_TMRZ_F1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TCAENT_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TCAENT_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14379. EMIF_CTLCFG_DENALI_PI_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PI_TMRZ_F1	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	PI_TCAENT_F0	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.675 EMIF_CTLCFG_DENALI_PI_201 Register

1 EMIF_CTLCFG_DENALI_PI_201 Register (Offset = 2324h) [reset = 0h]

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Table 14-14380. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A324h**

Figure 14-4754. EMIF_CTLCFG_DENALI_PI_201 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_TMRZ_F2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TCAENT_F1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TCAENT_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14382. EMIF_CTLCFG_DENALI_PI_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PI_TMRZ_F2	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	PI_TCAENT_F1	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.676 EMIF_CTLCFG_DENALI_PI_202 Register

1 EMIF_CTLCFG_DENALI_PI_202 Register (Offset = 2328h) [reset = 0h]

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Table 14-14383. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A328h**

Figure 14-4755. EMIF_CTLCFG_DENALI_PI_202 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_TDFI_CASEL_F0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TDFI_CACSCA_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PI_TCAENT_F2					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TCAENT_F2							
R/W							
0h							

Table 14-14385. EMIF_CTLCFG_DENALI_PI_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TDFI_CASEL_F0	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TDFI_CACSCA_F0	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	PI_TCAENT_F2	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.677 EMIF_CTLCFG_DENALI_PI_203 Register

1 EMIF_CTLCFG_DENALI_PI_203 Register (Offset = 232Ch) [reset = 0h]

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Table 14-14386. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A32Ch

Figure 14-4756. EMIF_CTLCFG_DENALI_PI_203 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TVREF_LONG_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_TVREF_LONG_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PI_TVREF_SHORT_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TVREF_SHORT_F0							
R/W							
0h							

Table 14-14388. EMIF_CTLCFG_DENALI_PI_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TVREF_LONG_F0	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TVREF_SHORT_F0	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.678 EMIF_CTLCFG_DENALI_PI_204 Register

1 EMIF_CTLCFG_DENALI_PI_204 Register (Offset = 2330h) [reset = 0h]

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Table 14-14389. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A330h**

Figure 14-4757. EMIF_CTLCFG_DENALI_PI_204 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TVREF_SHORT_F1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_TVREF_SHORT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED			PI_TDFI_CASEL_F1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PI_TDFI_CACSCA_F1				
NONE			R/W				
0h			0h				

Table 14-14391. EMIF_CTLCFG_DENALI_PI_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TVREF_SHORT_F1	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_TDFI_CASEL_F1	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TDFI_CACSCA_F1	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.679 EMIF_CTLCFG_DENALI_PI_205 Register

1 EMIF_CTLCFG_DENALI_PI_205 Register (Offset = 2334h) [reset = 0h]

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Table 14-14392. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A334h**

Figure 14-4758. EMIF_CTLCFG_DENALI_PI_205 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_TDFI_CASEL_F2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TDFI_CACSCA_F2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TVREF_LONG_F1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TVREF_LONG_F1							
R/W							
0h							

Table 14-14394. EMIF_CTLCFG_DENALI_PI_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_TDFI_CASEL_F2	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TDFI_CACSCA_F2	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TVREF_LONG_F1	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.680 EMIF_CTLCFG_DENALI_PI_206 Register

1 EMIF_CTLCFG_DENALI_PI_206 Register (Offset = 2338h) [reset = 0h]

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Table 14-14395. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A338h

Figure 14-4759. EMIF_CTLCFG_DENALI_PI_206 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TVREF_LONG_F2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TVREF_LONG_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_TVREF_SHORT_F2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TVREF_SHORT_F2							
R/W							
0h							

Table 14-14397. EMIF_CTLCFG_DENALI_PI_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TVREF_LONG_F2	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TVREF_SHORT_F2	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.681 EMIF_CTLCFG_DENALI_PI_207 Register

1 EMIF_CTLCFG_DENALI_PI_207 Register (Offset = 233Ch) [reset = 0h]

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Table 14-14398. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A33Ch

Figure 14-4760. EMIF_CTLCFG_DENALI_PI_207 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_CALVL_VREF_INITIAL_STOP_POINT_F1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_CALVL_VREF_INITIAL_START_POINT_F1						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	PI_CALVL_VREF_INITIAL_STOP_POINT_F0						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PI_CALVL_VREF_INITIAL_START_POINT_F0						
NONE	R/W						
0h	0h						

Table 14-14400. EMIF_CTLCFG_DENALI_PI_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_CALVL_VREF_INITIAL_STOP_POINT_F1	R/W	0h	The end point of initial training for the Vref[ca] training for frequency set 1 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_CALVL_VREF_INITIAL_START_POINT_F1	R/W	0h	The start point of initial training for the Vref[ca] training for frequency set 1 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_CALVL_VREF_INITIAL_STOP_POINT_F0	R/W	0h	The end point of initial training for the Vref[ca] training for frequency set 0 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_CALVL_VREF_INITIAL_START_POINT_F0	R/W	0h	The start point of initial training for the Vref[ca] training for frequency set 0 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n

14.5.1.2.682 EMIF_CTLCFG_DENALI_PI_208 Register

1 EMIF_CTLCFG_DENALI_PI_208 Register (Offset = 2340h) [reset = 0h]

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Table 14-14401. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A340h**

Figure 14-4761. EMIF_CTLCFG_DENALI_PI_208 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_CALVL_VREF_DELTA_F1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PI_CALVL_VREF_DELTA_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED	PI_CALVL_VREF_INITIAL_STOP_POINT_F2						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PI_CALVL_VREF_INITIAL_START_POINT_F2						
NONE	R/W						
0h	0h						

Table 14-14403. EMIF_CTLCFG_DENALI_PI_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PI_CALVL_VREF_DELTA_F1	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_CALVL_VREF_DELTA_F0	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_CALVL_VREF_INITIAL_STOP_POINT_F2	R/W	0h	The end point of initial training for the Vref[ca] training for frequency set 2 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_CALVL_VREF_INITIAL_START_POINT_F2	R/W	0h	The start point of initial training for the Vref[ca] training for frequency set 2 { vrefca_range, vref_ca_setting[5:0]}. Reset Source: ctl_amod_g_rst_n

14.5.1.2.683 EMIF_CTLCFG_DENALI_PI_209 Register

1 EMIF_CTLCFG_DENALI_PI_209 Register (Offset = 2344h) [reset = 0h]

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Table 14-14404. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A344h**

Figure 14-4762. EMIF_CTLCFG_DENALI_PI_209 Name Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TXP_F0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_TDFI_CALVL_STROBE_F0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_CALVL_VREF_DELTA_F2			
NONE				R/W			
0h				0h			

Table 14-14406. EMIF_CTLCFG_DENALI_PI_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMRWCKEL_F0	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TXP_F0	R/W	0h	CKE assert to next valid command delay for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TDFI_CALVL_STROBE_F0	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_CALVL_VREF_DELTA_F2	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.684 EMIF_CTLCFG_DENALI_PI_210 Register

1 EMIF_CTLCFG_DENALI_PI_210 Register (Offset = 2348h) [reset = 0h]

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Table 14-14407. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A348h**

Figure 14-4763. EMIF_CTLCFG_DENALI_PI_210 Name Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED			PI_TXP_F1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED				PI_TDFI_CALVL_STROBE_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED			PI_TCKELCK_F0				
NONE			R/W				
0h			0h				

Table 14-14409. EMIF_CTLCFG_DENALI_PI_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMRWCKEL_F1	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TXP_F1	R/W	0h	CKE assert to next valid command delay for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TDFI_CALVL_STROBE_F1	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCKELCK_F0	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.685 EMIF_CTLCFG_DENALI_PI_211 Register

1 EMIF_CTLCFG_DENALI_PI_211 Register (Offset = 234Ch) [reset = 0h]

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Table 14-14410. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A34Ch

Figure 14-4764. EMIF_CTLCFG_DENALI_PI_211 Name Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TXP_F2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PI_TDFI_CALVL_STROBE_F2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_TCKELCK_F1				
NONE			R/W				
0h			0h				

Table 14-14412. EMIF_CTLCFG_DENALI_PI_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMRWCKEL_F2	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_TXP_F2	R/W	0h	CKE assert to next valid command delay for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_TDFI_CALVL_STROBE_F2	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCKELCK_F1	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.686 EMIF_CTLCFG_DENALI_PI_212 Register

1 EMIF_CTLCFG_DENALI_PI_212 Register (Offset = 2350h) [reset = 0h]

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Table 14-14413. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A350h**

Figure 14-4765. EMIF_CTLCFG_DENALI_PI_212 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_INIT_START_F0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDFI_INIT_START_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_INIT_START_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_TCKELCK_F2				
NONE			R/W				
0h			0h				

Table 14-14415. EMIF_CTLCFG_DENALI_PI_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	PI_TDFI_INIT_START_F0	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks] for frequency set 0, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCKELCK_F2	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.687 EMIF_CTLCFG_DENALI_PI_213 Register

1 EMIF_CTLCFG_DENALI_PI_213 Register (Offset = 2354h) [reset = 0h]

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Table 14-14416. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A354h

Figure 14-4766. EMIF_CTLCFG_DENALI_PI_213 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_INIT_COMPLETE_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_INIT_COMPLETE_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_INIT_COMPLETE_F0							
R/W							
0h							

Table 14-14418. EMIF_CTLCFG_DENALI_PI_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TDFI_INIT_COMPLETE_F0	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks] for frequency set 0, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.688 EMIF_CTLCFG_DENALI_PI_214 Register

1 EMIF_CTLCFG_DENALI_PI_214 Register (Offset = 2358h) [reset = 0h]

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Table 14-14419. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A358h**

Figure 14-4767. EMIF_CTLCFG_DENALI_PI_214 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_INIT_START_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_INIT_START_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_INIT_START_F1							
R/W							
0h							

Table 14-14421. EMIF_CTLCFG_DENALI_PI_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TDFI_INIT_START_F1	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks] for frequency set 1, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.689 EMIF_CTLCFG_DENALI_PI_215 Register

1 EMIF_CTLCFG_DENALI_PI_215 Register (Offset = 235Ch) [reset = 0h]

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Table 14-14422. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A35Ch

Figure 14-4768. EMIF_CTLCFG_DENALI_PI_215 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDFI_INIT_COMPLETE_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_INIT_COMPLETE_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_INIT_COMPLETE_F1							
R/W							
0h							

Table 14-14424. EMIF_CTLCFG_DENALI_PI_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TDFI_INIT_COMPLETE_F1	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks] for frequency set 1, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.690 EMIF_CTLCFG_DENALI_PI_216 Register

1 EMIF_CTLCFG_DENALI_PI_216 Register (Offset = 2360h) [reset = 0h]

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Table 14-14425. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A360h**

Figure 14-4769. EMIF_CTLCFG_DENALI_PI_216 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_INIT_START_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_INIT_START_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_INIT_START_F2							
R/W							
0h							

Table 14-14427. EMIF_CTLCFG_DENALI_PI_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TDFI_INIT_START_F2	R/W	0h	Defines the DFI tINIT_START timing parameter [in DFI clocks] for frequency set 2, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.691 EMIF_CTLCFG_DENALI_PI_217 Register

1 EMIF_CTLCFG_DENALI_PI_217 Register (Offset = 2364h) [reset = 0h]

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Table 14-14428. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A364h**

Figure 14-4770. EMIF_CTLCFG_DENALI_PI_217 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TCKEHDQS_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TDFI_INIT_COMPLETE_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TDFI_INIT_COMPLETE_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TDFI_INIT_COMPLETE_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14430. EMIF_CTLCFG_DENALI_PI_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TCKEHDQS_F0	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:0	PI_TDFI_INIT_COMPLETE_F2	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter [in DFI clocks] for frequency set 2, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.692 EMIF_CTLCFG_DENALI_PI_218 Register

1 EMIF_CTLCFG_DENALI_PI_218 Register (Offset = 2368h) [reset = 0h]

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Table 14-14431. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 A368h**

Figure 14-4771. EMIF_CTLCFG_DENALI_PI_218 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TCKEHDQS_F1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TFC_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TFC_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14433. EMIF_CTLCFG_DENALI_PI_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PI_TCKEHDQS_F1	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TFC_F0	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.693 EMIF_CTLCFG_DENALI_PI_219 Register

1 EMIF_CTLCFG_DENALI_PI_219 Register (Offset = 236Ch) [reset = 0h]

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Table 14-14434. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A36Ch**

Figure 14-4772. EMIF_CTLCFG_DENALI_PI_219 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		PI_TCKEHDQS_F2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED						PI_TFC_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TFC_F1							
R/W							
0h							

Table 14-14436. EMIF_CTLCFG_DENALI_PI_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PI_TCKEHDQS_F2	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TFC_F1	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.694 EMIF_CTLCFG_DENALI_PI_220 Register

1 EMIF_CTLCFG_DENALI_PI_220 Register (Offset = 2370h) [reset = 0h]

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Table 14-14437. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A370h

Figure 14-4773. EMIF_CTLCFG_DENALI_PI_220 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_VREF_EN_F1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_VREF_EN_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_TFC_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TFC_F2							
R/W							
0h							

Table 14-14439. EMIF_CTLCFG_DENALI_PI_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_VREF_EN_F1	R/W	0h	Enable VREF training during power-up initialization for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_VREF_EN_F0	R/W	0h	Enable VREF training during power-up initialization for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TFC_F2	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.695 EMIF_CTLCFG_DENALI_PI_221 Register

1 EMIF_CTLCFG_DENALI_PI_221 Register (Offset = 2374h) [reset = 0h]

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Table 14-14440. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A374h**

Figure 14-4774. EMIF_CTLCFG_DENALI_PI_221 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_TDFI_WDQLVL_WR_F0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_WDQLVL_WR_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_VREF_EN_F2	
NONE						R/W	
0h						0h	

Table 14-14442. EMIF_CTLCFG_DENALI_PI_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PI_TDFI_WDQLVL_WR_F0	R/W	0h	Switch time from write to read for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_VREF_EN_F2	R/W	0h	Enable VREF training during power-up initialization for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.696 EMIF_CTLCFG_DENALI_PI_222 Register

1 EMIF_CTLCFG_DENALI_PI_222 Register (Offset = 2378h) [reset = 0h]

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Table 14-14443. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A378h

Figure 14-4775. EMIF_CTLCFG_DENALI_PI_222 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F0						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_WDQLVL_VREF_INITIAL_START_POINT_F0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED						PI_TDFI_WDQLVL_RW_F0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RW_F0							
R/W							
0h							

Table 14-14445. EMIF_CTLCFG_DENALI_PI_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F0	R/W	0h	Write DQ training vref initial training stop value for frequency set 0. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_WDQLVL_VREF_INITIAL_START_POINT_F0	R/W	0h	Write DQ training vref initial training start value for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WDQLVL_RW_F0	R/W	0h	Switch time from read to write for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.697 EMIF_CTLCFG_DENALI_PI_223 Register

1 EMIF_CTLCFG_DENALI_PI_223 Register (Offset = 237Ch) [reset = 0h]

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Table 14-14446. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A37Ch**

Figure 14-4776. EMIF_CTLCFG_DENALI_PI_223 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PI_WDQLVL_CL_F0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_NTP_TRAIN_EN_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_WDQLVL_EN_F0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_WDQLVL_VREF_DELTA_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14448. EMIF_CTLCFG_DENALI_PI_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_WDQLVL_CL_F0	R/W	0h	CL when the Read DBI disabled while doing WDQ training for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_NTP_TRAIN_EN_F0	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_EN_F0	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_WDQLVL_VREF_DELTA_F0	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.698 EMIF_CTLCFG_DENALI_PI_224 Register

1 EMIF_CTLCFG_DENALI_PI_224 Register (Offset = 2380h) [reset = 0h]

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Table 14-14449. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A380h**

Figure 14-4777. EMIF_CTLCFG_DENALI_PI_224 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_TDFI_WDQLVL_WR_F1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TDFI_WDQLVL_WR_F1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_WDQLVL_WRLAT_ADJ_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_WDQLVL_RDLAT_ADJ_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14451. EMIF_CTLCFG_DENALI_PI_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_WDQLVL_WR_F1	R/W	0h	Switch time from write to read for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_WDQLVL_WRLAT_ADJ_F0	R/W	0h	Adjusted Tdfi_wrdata_en value for PHY read timing when read dbi disabled for frequency set 0, used for WDQ training. Reset Source: ctl_amod_g_rst_n
7:0	PI_WDQLVL_RDLAT_ADJ_F0	R/W	0h	Adjusted Tdfi_rddata_en value for PHY read timing when read dbi disabled for frequency set 0, used for WDQ training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.699 EMIF_CTLCFG_DENALI_PI_225 Register

1 EMIF_CTLCFG_DENALI_PI_225 Register (Offset = 2384h) [reset = 0h]

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Table 14-14452. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A384h**

Figure 14-4778. EMIF_CTLCFG_DENALI_PI_225 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_WDQLVL_VREF_INITIAL_START_POINT_F1						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED						PI_TDFI_WDQLVL_RW_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RW_F1							
R/W							
0h							

Table 14-14454. EMIF_CTLCFG_DENALI_PI_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F1	R/W	0h	Write DQ training vref initial training stop value for frequency set 1. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_WDQLVL_VREF_INITIAL_START_POINT_F1	R/W	0h	Write DQ training vref initial training start value for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WDQLVL_RW_F1	R/W	0h	Switch time from read to write for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.700 EMIF_CTLCFG_DENALI_PI_226 Register

1 EMIF_CTLCFG_DENALI_PI_226 Register (Offset = 2388h) [reset = 0h]

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Table 14-14455. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A388h**

Figure 14-4779. EMIF_CTLCFG_DENALI_PI_226 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_WDQLVL_CL_F1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED						PI_NTP_TRAIN_EN_F1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PI_WDQLVL_EN_F1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED				PI_WDQLVL_VREF_DELTA_F1			
NONE				R/W			
0h				0h			

Table 14-14457. EMIF_CTLCFG_DENALI_PI_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_WDQLVL_CL_F1	R/W	0h	CL when the Read DBI disabled while doing WDQ training for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_NTP_TRAIN_EN_F1	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_EN_F1	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_WDQLVL_VREF_DELTA_F1	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.701 EMIF_CTLCFG_DENALI_PI_227 Register

1 EMIF_CTLCFG_DENALI_PI_227 Register (Offset = 238Ch) [reset = 0h]

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Table 14-14458. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A38Ch**

Figure 14-4780. EMIF_CTLCFG_DENALI_PI_227 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_TDFI_WDQLVL_WR_F2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PI_TDFI_WDQLVL_WR_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_WDQLVL_WRLAT_ADJ_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_WDQLVL_RDLAT_ADJ_F1							
R/W							
0h							

Table 14-14460. EMIF_CTLCFG_DENALI_PI_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PI_TDFI_WDQLVL_WR_F2	R/W	0h	Switch time from write to read for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_WDQLVL_WRLAT_ADJ_F1	R/W	0h	Adjusted Tdfi_wrdata_en value for PHY read timing when read dbi disabled for frequency set 1, used for WDQ training. Reset Source: ctl_amod_g_rst_n
7:0	PI_WDQLVL_RDLAT_ADJ_F1	R/W	0h	Adjusted Tdfi_rddata_en value for PHY read timing when read dbi disabled for frequency set 1, used for WDQ training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.702 EMIF_CTLCFG_DENALI_PI_228 Register

1 EMIF_CTLCFG_DENALI_PI_228 Register (Offset = 2390h) [reset = 0h]

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Table 14-14461. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A390h**

Figure 14-4781. EMIF_CTLCFG_DENALI_PI_228 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F2						
NONE	R/W						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED	PI_WDQLVL_VREF_INITIAL_START_POINT_F2						
NONE	R/W						
0h	0h						

15	14	13	12	11	10	9	8
RESERVED						PI_TDFI_WDQLVL_RW_F2	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RW_F2							
R/W							
0h							

Table 14-14463. EMIF_CTLCFG_DENALI_PI_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F2	R/W	0h	Write DQ training vref initial training stop value for frequency set 2. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_WDQLVL_VREF_INITIAL_START_POINT_F2	R/W	0h	Write DQ training vref initial training start value for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PI_TDFI_WDQLVL_RW_F2	R/W	0h	Switch time from read to write for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.703 EMIF_CTLCFG_DENALI_PI_229 Register

1 EMIF_CTLCFG_DENALI_PI_229 Register (Offset = 2394h) [reset = 0h]

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Table 14-14464. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A394h**

Figure 14-4782. EMIF_CTLCFG_DENALI_PI_229 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_WDQLVL_CL_F2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_NTP_TRAIN_EN_F2	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_WDQLVL_EN_F2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PI_WDQLVL_VREF_DELTA_F2			
NONE				R/W			
0h				0h			

Table 14-14466. EMIF_CTLCFG_DENALI_PI_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_WDQLVL_CL_F2	R/W	0h	CL when the Read DBI disabled while doing WDQ training for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_NTP_TRAIN_EN_F2	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_WDQLVL_EN_F2	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_WDQLVL_VREF_DELTA_F2	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.704 EMIF_CTLCFG_DENALI_PI_230 Register

1 EMIF_CTLCFG_DENALI_PI_230 Register (Offset = 2398h) [reset = 0h]

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Table 14-14467. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A398h**

Figure 14-4783. EMIF_CTLCFG_DENALI_PI_230 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_RD_DBI_LEVEL_EN_F1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RD_DBI_LEVEL_EN_F0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PI_WDQLVL_WRLAT_ADJ_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_WDQLVL_RDLAT_ADJ_F2							
R/W							
0h							

Table 14-14469. EMIF_CTLCFG_DENALI_PI_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_RD_DBI_LEVEL_EN_F1	R/W	0h	Read DBI leveling enable, only can be enabled when READ DBI supported for DDR4, and PI_WDQLVL_EN or PI_RDLVL_EN configured by 1 for frequency set 1. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_RD_DBI_LEVEL_EN_F0	R/W	0h	Read DBI leveling enable, only can be enabled when READ DBI supported for DDR4, and PI_WDQLVL_EN or PI_RDLVL_EN configured by 1 for frequency set 0. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n
15:8	PI_WDQLVL_WRLAT_ADJ_F2	R/W	0h	Adjusted Tdfi_wrdata_en value for PHY read timing when read dbi disabled for frequency set 2, used for WDQ training. Reset Source: ctl_amod_g_rst_n
7:0	PI_WDQLVL_RDLAT_ADJ_F2	R/W	0h	Adjusted Tdfi_rddata_en value for PHY read timing when read dbi disabled for frequency set 2, used for WDQ training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.705 EMIF_CTLCFG_DENALI_PI_231 Register

1 EMIF_CTLCFG_DENALI_PI_231 Register (Offset = 239Ch) [reset = 0h]

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Table 14-14470. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A39Ch**

Figure 14-4784. EMIF_CTLCFG_DENALI_PI_231 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_TRCD_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TRP_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TRTP_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PI_RD_DBI_LEVEL_EN_F2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14472. EMIF_CTLCFG_DENALI_PI_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TRCD_F0	R/W	0h	DRAM tRCD value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_TRP_F0	R/W	0h	DRAM tRP value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_TRTP_F0	R/W	0h	DRAM tRTP value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_RD_DBI_LEVEL_EN_F2	R/W	0h	Read DBI leveling enable, only can be enabled when READ DBI supported for DDR4, and PI_WDQLVL_EN or PI_RDLVL_EN configured by 1 for frequency set 2. Bit[1] represents the support when non-initialization. Bit[0]represents the support when initialization. Reset Source: ctl_amod_g_rst_n

14.5.1.2.706 EMIF_CTLCFG_DENALI_PI_232 Register

1 EMIF_CTLCFG_DENALI_PI_232 Register (Offset = 23A0h) [reset = 0h]

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Table 14-14473. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A3A0h

Figure 14-4785. EMIF_CTLCFG_DENALI_PI_232 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TWR_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED		PI_TWTR_F0					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED			PI_TCCD_L_F0				
NONE			R/W				
0h			0h				

Table 14-14475. EMIF_CTLCFG_DENALI_PI_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_TWR_F0	R/W	0h	DRAM tWR value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_TWTR_F0	R/W	0h	DRAM tWTR value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_TCCD_L_F0	R/W	0h	DRAM CAS-to_CAS value within the same bank group in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.707 EMIF_CTLCFG_DENALI_PI_233 Register

1 EMIF_CTLCFG_DENALI_PI_233 Register (Offset = 23A4h) [reset = 0h]

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Table 14-14476. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3A4h**

Figure 14-4786. EMIF_CTLCFG_DENALI_PI_233 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TRAS_MAX_F0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_TRAS_MAX_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TRAS_MAX_F0							
R/W							
0h							

Table 14-14478. EMIF_CTLCFG_DENALI_PI_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TRAS_MAX_F0	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.708 EMIF_CTLCFG_DENALI_PI_234 Register

1 EMIF_CTLCFG_DENALI_PI_234 Register (Offset = 23A8h) [reset = 0h]

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Table 14-14479. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3A8h**

Figure 14-4787. EMIF_CTLCFG_DENALI_PI_234 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PI_TCCDMW_F0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TDQSCK_MAX_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_TRAS_MIN_F0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TRAS_MIN_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14481. EMIF_CTLCFG_DENALI_PI_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TCCDMW_F0	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_TDQSCK_MAX_F0	R/W	0h	Additional delay needed for tDQSCK for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PI_TRAS_MIN_F0	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.709 EMIF_CTLCFG_DENALI_PI_235 Register

1 EMIF_CTLCFG_DENALI_PI_235 Register (Offset = 23ACh) [reset = 0h]

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Table 14-14482. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3ACh**

Figure 14-4788. EMIF_CTLCFG_DENALI_PI_235 Name Register

31	30	29	28	27	26	25	24
PI_TMOD_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TMRW_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TSR_F0							
R/W							
0h							

Table 14-14484. EMIF_CTLCFG_DENALI_PI_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMOD_F0	R/W	0h	DRAM tMOD value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_TMRW_F0	R/W	0h	DRAM tMRW value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_F0	R/W	0h	DRAM tMRD value in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_TSR_F0	R/W	0h	Min cycles from sref entry to sref exit for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.710 EMIF_CTLCFG_DENALI_PI_236 Register

1 EMIF_CTLCFG_DENALI_PI_236 Register (Offset = 23B0h) [reset = 0h]

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Table 14-14485. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3B0h**

Figure 14-4789. EMIF_CTLCFG_DENALI_PI_236 Name Register

31	30	29	28	27	26	25	24
PI_TRP_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TRTP_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_PAR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TMOD_PAR_F0							
R/W							
0h							

Table 14-14487. EMIF_CTLCFG_DENALI_PI_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TRP_F1	R/W	0h	DRAM tRP value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_TRTP_F1	R/W	0h	DRAM tRTP value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_PAR_F0	R/W	0h	DRAM tMRD value when CA parity is enabled in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_TMOD_PAR_F0	R/W	0h	DRAM tMOD value when CA parity is enabled in cycles for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.711 EMIF_CTLCFG_DENALI_PI_237 Register

1 EMIF_CTLCFG_DENALI_PI_237 Register (Offset = 23B4h) [reset = 0h]

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Table 14-14488. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3B4h**

Figure 14-4790. EMIF_CTLCFG_DENALI_PI_237 Name Register

31	30	29	28	27	26	25	24
PI_TWR_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PI_TWTR_F1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED			PI_TCCD_L_F1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PI_TRCD_F1							
R/W							
0h							

Table 14-14490. EMIF_CTLCFG_DENALI_PI_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TWR_F1	R/W	0h	DRAM tWR value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_TWTR_F1	R/W	0h	DRAM tWTR value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_TCCD_L_F1	R/W	0h	DRAM CAS-to_CAS value within the same bank group in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_TRCD_F1	R/W	0h	DRAM tRCD value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.712 EMIF_CTLCFG_DENALI_PI_238 Register

1 EMIF_CTLCFG_DENALI_PI_238 Register (Offset = 23B8h) [reset = 0h]

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Table 14-14491. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3B8h**

Figure 14-4791. EMIF_CTLCFG_DENALI_PI_238 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PI_TRAS_MAX_F1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TRAS_MAX_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TRAS_MAX_F1							
R/W							
0h							

Table 14-14493. EMIF_CTLCFG_DENALI_PI_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TRAS_MAX_F1	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.713 EMIF_CTLCFG_DENALI_PI_239 Register

1 EMIF_CTLCFG_DENALI_PI_239 Register (Offset = 23BCh) [reset = 0h]

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Table 14-14494. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3BCh**

Figure 14-4792. EMIF_CTLCFG_DENALI_PI_239 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_TCCDMW_F1					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED				PI_TDQSCK_MAX_F1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							PI_TRAS_MIN_F1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PI_TRAS_MIN_F1							
R/W							
0h							

Table 14-14496. EMIF_CTLCFG_DENALI_PI_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TCCDMW_F1	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_TDQSCK_MAX_F1	R/W	0h	Additional delay needed for tDQSCK for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PI_TRAS_MIN_F1	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.714 EMIF_CTLCFG_DENALI_PI_240 Register

1 EMIF_CTLCFG_DENALI_PI_240 Register (Offset = 23C0h) [reset = 0h]

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Table 14-14497. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3C0h**

Figure 14-4793. EMIF_CTLCFG_DENALI_PI_240 Name Register

31	30	29	28	27	26	25	24
PI_TMOD_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TMRW_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TSR_F1							
R/W							
0h							

Table 14-14499. EMIF_CTLCFG_DENALI_PI_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMOD_F1	R/W	0h	DRAM tMOD value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_TMRW_F1	R/W	0h	DRAM tMRW value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_F1	R/W	0h	DRAM tMRD value in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_TSR_F1	R/W	0h	Min cycles from sref entry to sref exit for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.715 EMIF_CTLCFG_DENALI_PI_241 Register

1 EMIF_CTLCFG_DENALI_PI_241 Register (Offset = 23C4h) [reset = 0h]

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Table 14-14500. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3C4h**

Figure 14-4794. EMIF_CTLCFG_DENALI_PI_241 Name Register

31	30	29	28	27	26	25	24
PI_TRP_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TRTP_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TMRD_PAR_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TMOD_PAR_F1							
R/W							
0h							

Table 14-14502. EMIF_CTLCFG_DENALI_PI_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TRP_F2	R/W	0h	DRAM tRP value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_TRTP_F2	R/W	0h	DRAM tRTP value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_PAR_F1	R/W	0h	DRAM tMRD value when CA parity is enabled in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_TMOD_PAR_F1	R/W	0h	DRAM tMOD value when CA parity is enabled in cycles for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.716 EMIF_CTLCFG_DENALI_PI_242 Register

1 EMIF_CTLCFG_DENALI_PI_242 Register (Offset = 23C8h) [reset = 0h]

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Table 14-14503. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A3C8h

Figure 14-4795. EMIF_CTLCFG_DENALI_PI_242 Name Register

31	30	29	28	27	26	25	24
PI_TWR_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PI_TWTR_F2					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED			PI_TCCD_L_F2				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PI_TRCD_F2							
R/W							
0h							

Table 14-14505. EMIF_CTLCFG_DENALI_PI_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TWR_F2	R/W	0h	DRAM tWR value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_TWTR_F2	R/W	0h	DRAM tWTR value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_TCCD_L_F2	R/W	0h	DRAM CAS-to_CAS value within the same bank group in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_TRCD_F2	R/W	0h	DRAM tRCD value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.717 EMIF_CTLCFG_DENALI_PI_243 Register

1 EMIF_CTLCFG_DENALI_PI_243 Register (Offset = 23CCh) [reset = 0h]

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Table 14-14506. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A3CCh

Figure 14-4796. EMIF_CTLCFG_DENALI_PI_243 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TRAS_MAX_F2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TRAS_MAX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TRAS_MAX_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14508. EMIF_CTLCFG_DENALI_PI_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PI_TRAS_MAX_F2	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.718 EMIF_CTLCFG_DENALI_PI_244 Register

1 EMIF_CTLCFG_DENALI_PI_244 Register (Offset = 23D0h) [reset = 0h]

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Table 14-14509. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3D0h**

Figure 14-4797. EMIF_CTLCFG_DENALI_PI_244 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_TCCDMW_F2					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED				PI_TDQSCK_MAX_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							PI_TRAS_MIN_F2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PI_TRAS_MIN_F2							
R/W							
0h							

Table 14-14511. EMIF_CTLCFG_DENALI_PI_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TCCDMW_F2	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_TDQSCK_MAX_F2	R/W	0h	Additional delay needed for tDQSCK for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PI_TRAS_MIN_F2	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.719 EMIF_CTLCFG_DENALI_PI_245 Register

1 EMIF_CTLCFG_DENALI_PI_245 Register (Offset = 23D4h) [reset = 0h]

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Table 14-14512. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3D4h**

Figure 14-4798. EMIF_CTLCFG_DENALI_PI_245 Name Register

31	30	29	28	27	26	25	24
PI_TMOD_F2							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TMRW_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TSR_F2							
R/W							
0h							

Table 14-14514. EMIF_CTLCFG_DENALI_PI_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TMOD_F2	R/W	0h	DRAM tMOD value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_TMRW_F2	R/W	0h	DRAM tMRW value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_TMRD_F2	R/W	0h	DRAM tMRD value in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_TSR_F2	R/W	0h	Min cycles from sref entry to sref exit for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.720 EMIF_CTLCFG_DENALI_PI_246 Register

1 EMIF_CTLCFG_DENALI_PI_246 Register (Offset = 23D8h) [reset = 0h]

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Table 14-14515. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3D8h**

Figure 14-4799. EMIF_CTLCFG_DENALI_PI_246 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TMRD_PAR_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TMOD_PAR_F2							
R/W							
0h							

Table 14-14517. EMIF_CTLCFG_DENALI_PI_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TMRD_PAR_F2	R/W	0h	DRAM tMRD value when CA parity is enabled in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_TMOD_PAR_F2	R/W	0h	DRAM tMOD value when CA parity is enabled in cycles for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.721 EMIF_CTLCFG_DENALI_PI_247 Register

1 EMIF_CTLCFG_DENALI_PI_247 Register (Offset = 23DCh) [reset = 0h]

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Table 14-14518. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3DCh**

Figure 14-4800. EMIF_CTLCFG_DENALI_PI_247 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PI_TDFI_CTRLUPD_MAX_F0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_MAX_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_MAX_F0							
R/W							
0h							

Table 14-14520. EMIF_CTLCFG_DENALI_PI_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PI_TDFI_CTRLUPD_MAX_F0	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks] for frequency set 0, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.722 EMIF_CTLCFG_DENALI_PI_248 Register

1 EMIF_CTLCFG_DENALI_PI_248 Register (Offset = 23E0h) [reset = 0h]

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Table 14-14521. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3E0h**

Figure 14-4801. EMIF_CTLCFG_DENALI_PI_248 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_INTERVAL_F0							
R/W							
0h							

Table 14-14523. EMIF_CTLCFG_DENALI_PI_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CTRLUPD_INTERVAL_F0	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks] for frequency set 0, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.723 EMIF_CTLCFG_DENALI_PI_249 Register

1 EMIF_CTLCFG_DENALI_PI_249 Register (Offset = 23E4h) [reset = 0h]

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Table 14-14524. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3E4h**

Figure 14-4802. EMIF_CTLCFG_DENALI_PI_249 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED			PI_TDFI_CTRLUPD_MAX_F1				
NONE			R/W				
0h			0h				

15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_MAX_F1							
R/W							
0h							

7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_MAX_F1							
R/W							
0h							

Table 14-14526. EMIF_CTLCFG_DENALI_PI_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PI_TDFI_CTRLUPD_MAX_F1	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks] for frequency set 1, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.724 EMIF_CTLCFG_DENALI_PI_250 Register

1 EMIF_CTLCFG_DENALI_PI_250 Register (Offset = 23E8h) [reset = 0h]

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Table 14-14527. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3E8h**

Figure 14-4803. EMIF_CTLCFG_DENALI_PI_250 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_INTERVAL_F1							
R/W							
0h							

Table 14-14529. EMIF_CTLCFG_DENALI_PI_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CTRLUPD_INTERVAL_F1	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks] for frequency set 1, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.725 EMIF_CTLCFG_DENALI_PI_251 Register

1 EMIF_CTLCFG_DENALI_PI_251 Register (Offset = 23ECh) [reset = 0h]

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Table 14-14530. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3ECh**

Figure 14-4804. EMIF_CTLCFG_DENALI_PI_251 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_TDFI_CTRLUPD_MAX_F2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_CTRLUPD_MAX_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_CTRLUPD_MAX_F2							
R/W							
0h							

Table 14-14532. EMIF_CTLCFG_DENALI_PI_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PI_TDFI_CTRLUPD_MAX_F2	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter [in DFI clocks] for frequency set 2, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit [1] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.726 EMIF_CTLCFG_DENALI_PI_252 Register

1 EMIF_CTLCFG_DENALI_PI_252 Register (Offset = 23F0h) [reset = 0h]

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Table 14-14533. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3F0h**

Figure 14-4805. EMIF_CTLCFG_DENALI_PI_252 Name Register

31	30	29	28	27	26	25	24
PI_TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDFI_CTRLUPD_INTERVAL_F2							
R/W							
0h							

Table 14-14535. EMIF_CTLCFG_DENALI_PI_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PI_TDFI_CTRLUPD_INTERVAL_F2	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter [in DFI clocks] for frequency set 2, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit [0] set in the PI_UPDATE_ERROR_STATUS parameter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.727 EMIF_CTLCFG_DENALI_PI_253 Register

1 EMIF_CTLCFG_DENALI_PI_253 Register (Offset = 23F4h) [reset = 0h]

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Table 14-14536. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3F4h**

Figure 14-4806. EMIF_CTLCFG_DENALI_PI_253 Name Register

31	30	29	28	27	26	25	24
PI_TXSR_F1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_TXSR_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TXSR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TXSR_F0							
R/W							
0h							

Table 14-14538. EMIF_CTLCFG_DENALI_PI_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TXSR_F1	R/W	0h	DRAM TXSR value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n
15:0	PI_TXSR_F0	R/W	0h	DRAM TXSR value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.728 EMIF_CTLCFG_DENALI_PI_254 Register

1 EMIF_CTLCFG_DENALI_PI_254 Register (Offset = 23F8h) [reset = 0h]

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Table 14-14539. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A3F8h

Figure 14-4807. EMIF_CTLCFG_DENALI_PI_254 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_TEXCKE_F1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PI_TEXCKE_F0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TXSR_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TXSR_F2							
R/W							
0h							

Table 14-14541. EMIF_CTLCFG_DENALI_PI_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_TEXCKE_F1	R/W	0h	DRAM CKE low after SREF command timing for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_TEXCKE_F0	R/W	0h	DRAM CKE low after SREF command timing for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:0	PI_TXSR_F2	R/W	0h	DRAM TXSR value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.729 EMIF_CTLCFG_DENALI_PI_255 Register

1 EMIF_CTLCFG_DENALI_PI_255 Register (Offset = 23FCh) [reset = 0h]

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Table 14-14542. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A3FCh**

Figure 14-4808. EMIF_CTLCFG_DENALI_PI_255 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDLL_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDLL_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PI_TEXCKE_F2					
NONE		R/W					
0h		0h					

Table 14-14544. EMIF_CTLCFG_DENALI_PI_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:8	PI_TDLL_F0	R/W	0h	DRAM tDLL value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_TEXCKE_F2	R/W	0h	DRAM CKE low after SREF command timing for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.730 EMIF_CTLCFG_DENALI_PI_256 Register

1 EMIF_CTLCFG_DENALI_PI_256 Register (Offset = 2400h) [reset = 0h]

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Table 14-14545. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A400h**

Figure 14-4809. EMIF_CTLCFG_DENALI_PI_256 Name Register

31	30	29	28	27	26	25	24
PI_TDLL_F2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TDLL_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TDLL_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TDLL_F1							
R/W							
0h							

Table 14-14547. EMIF_CTLCFG_DENALI_PI_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_TDLL_F2	R/W	0h	DRAM tDLL value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n
15:0	PI_TDLL_F1	R/W	0h	DRAM tDLL value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.731 EMIF_CTLCFG_DENALI_PI_257 Register

1 EMIF_CTLCFG_DENALI_PI_257 Register (Offset = 2404h) [reset = 0h]

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Table 14-14548. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A404h**

Figure 14-4810. EMIF_CTLCFG_DENALI_PI_257 Name Register

31	30	29	28	27	26	25	24
PI_TCKSRE_F1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TCKSRX_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TCKSRE_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TCKSRX_F0							
R/W							
0h							

Table 14-14550. EMIF_CTLCFG_DENALI_PI_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_TCKSRE_F1	R/W	0h	DRAM tCKSRE value. Reset Source: ctl_amod_g_rst_n
23:16	PI_TCKSRX_F1	R/W	0h	DRAM tCKSRX value. Reset Source: ctl_amod_g_rst_n
15:8	PI_TCKSRE_F0	R/W	0h	DRAM tCKSRE value. Reset Source: ctl_amod_g_rst_n
7:0	PI_TCKSRX_F0	R/W	0h	DRAM tCKSRX value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.732 EMIF_CTLCFG_DENALI_PI_258 Register

1 EMIF_CTLCFG_DENALI_PI_258 Register (Offset = 2408h) [reset = 0h]

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Table 14-14551. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A408h

Figure 14-4811. EMIF_CTLCFG_DENALI_PI_258 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TCKSRE_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TCKSRX_F2							
R/W							
0h							

Table 14-14553. EMIF_CTLCFG_DENALI_PI_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PI_TCKSRE_F2	R/W	0h	DRAM tCKSRE value. Reset Source: ctl_amod_g_rst_n
7:0	PI_TCKSRX_F2	R/W	0h	DRAM tCKSRX value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.733 EMIF_CTLCFG_DENALI_PI_259 Register

1 EMIF_CTLCFG_DENALI_PI_259 Register (Offset = 240Ch) [reset = 0h]

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Table 14-14554. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A40Ch**

Figure 14-4812. EMIF_CTLCFG_DENALI_PI_259 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TINIT_F0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TINIT_F0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TINIT_F0							
R/W							
0h							

Table 14-14556. EMIF_CTLCFG_DENALI_PI_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT_F0	R/W	0h	DRAM tINIT value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.734 EMIF_CTLCFG_DENALI_PI_260 Register

1 EMIF_CTLCFG_DENALI_PI_260 Register (Offset = 2410h) [reset = 0h]

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Table 14-14557. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A410h**

Figure 14-4813. EMIF_CTLCFG_DENALI_PI_260 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT3_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT3_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT3_F0							
R/W							
0h							

Table 14-14559. EMIF_CTLCFG_DENALI_PI_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT3_F0	R/W	0h	DRAM tINIT3 value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.735 EMIF_CTLCFG_DENALI_PI_261 Register

1 EMIF_CTLCFG_DENALI_PI_261 Register (Offset = 2414h) [reset = 0h]

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Table 14-14560. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A414h**

Figure 14-4814. EMIF_CTLCFG_DENALI_PI_261 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT4_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT4_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT4_F0							
R/W							
0h							

Table 14-14562. EMIF_CTLCFG_DENALI_PI_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT4_F0	R/W	0h	DRAM tINIT4 value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.736 EMIF_CTLCFG_DENALI_PI_262 Register

1 EMIF_CTLCFG_DENALI_PI_262 Register (Offset = 2418h) [reset = 0h]

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Table 14-14563. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A418h**

Figure 14-4815. EMIF_CTLCFG_DENALI_PI_262 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT5_F0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT5_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT5_F0							
R/W							
0h							

Table 14-14565. EMIF_CTLCFG_DENALI_PI_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT5_F0	R/W	0h	DRAM tINIT5 value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.737 EMIF_CTLCFG_DENALI_PI_263 Register

1 EMIF_CTLCFG_DENALI_PI_263 Register (Offset = 241Ch) [reset = 0h]

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Table 14-14566. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A41Ch**

Figure 14-4816. EMIF_CTLCFG_DENALI_PI_263 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TXSNR_F0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TXSNR_F0							
R/W							
0h							

Table 14-14568. EMIF_CTLCFG_DENALI_PI_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PI_TXSNR_F0	R/W	0h	DRAM tXSNR value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.738 EMIF_CTLCFG_DENALI_PI_264 Register

1 EMIF_CTLCFG_DENALI_PI_264 Register (Offset = 2420h) [reset = 0h]

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Table 14-14569. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A420h**

Figure 14-4817. EMIF_CTLCFG_DENALI_PI_264 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT_F1							
R/W							
0h							

Table 14-14571. EMIF_CTLCFG_DENALI_PI_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT_F1	R/W	0h	DRAM tINIT value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.739 EMIF_CTLCFG_DENALI_PI_265 Register

1 EMIF_CTLCFG_DENALI_PI_265 Register (Offset = 2424h) [reset = 0h]

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Table 14-14572. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A424h**

Figure 14-4818. EMIF_CTLCFG_DENALI_PI_265 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT3_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT3_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT3_F1							
R/W							
0h							

Table 14-14574. EMIF_CTLCFG_DENALI_PI_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT3_F1	R/W	0h	DRAM tINIT3 value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.740 EMIF_CTLCFG_DENALI_PI_266 Register

1 EMIF_CTLCFG_DENALI_PI_266 Register (Offset = 2428h) [reset = 0h]

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Table 14-14575. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A428h**

Figure 14-4819. EMIF_CTLCFG_DENALI_PI_266 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TINIT4_F1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TINIT4_F1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TINIT4_F1							
R/W							
0h							

Table 14-14577. EMIF_CTLCFG_DENALI_PI_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT4_F1	R/W	0h	DRAM tINIT4 value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.741 EMIF_CTLCFG_DENALI_PI_267 Register

1 EMIF_CTLCFG_DENALI_PI_267 Register (Offset = 242Ch) [reset = 0h]

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Table 14-14578. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A42Ch**

Figure 14-4820. EMIF_CTLCFG_DENALI_PI_267 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT5_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT5_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT5_F1							
R/W							
0h							

Table 14-14580. EMIF_CTLCFG_DENALI_PI_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT5_F1	R/W	0h	DRAM tINIT5 value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.742 EMIF_CTLCFG_DENALI_PI_268 Register

1 EMIF_CTLCFG_DENALI_PI_268 Register (Offset = 2430h) [reset = 0h]

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Table 14-14581. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A430h**

Figure 14-4821. EMIF_CTLCFG_DENALI_PI_268 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PI_TXSNR_F1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TXSNR_F1							
R/W							
0h							

Table 14-14583. EMIF_CTLCFG_DENALI_PI_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PI_TXSNR_F1	R/W	0h	DRAM tXSNR value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.743 EMIF_CTLCFG_DENALI_PI_269 Register

1 EMIF_CTLCFG_DENALI_PI_269 Register (Offset = 2434h) [reset = 0h]

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Table 14-14584. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A434h

Figure 14-4822. EMIF_CTLCFG_DENALI_PI_269 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TINIT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_TINIT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_TINIT_F2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14586. EMIF_CTLCFG_DENALI_PI_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT_F2	R/W	0h	DRAM tINIT value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.744 EMIF_CTLCFG_DENALI_PI_270 Register

1 EMIF_CTLCFG_DENALI_PI_270 Register (Offset = 2438h) [reset = 0h]

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Table 14-14587. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A438h

Figure 14-4823. EMIF_CTLCFG_DENALI_PI_270 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT3_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT3_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT3_F2							
R/W							
0h							

Table 14-14589. EMIF_CTLCFG_DENALI_PI_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT3_F2	R/W	0h	DRAM tINIT3 value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.745 EMIF_CTLCFG_DENALI_PI_271 Register

1 EMIF_CTLCFG_DENALI_PI_271 Register (Offset = 243Ch) [reset = 0h]

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Table 14-14590. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A43Ch**

Figure 14-4824. EMIF_CTLCFG_DENALI_PI_271 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_TINIT4_F2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_TINIT4_F2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_TINIT4_F2							
R/W							
0h							

Table 14-14592. EMIF_CTLCFG_DENALI_PI_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT4_F2	R/W	0h	DRAM tINIT4 value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.746 EMIF_CTLCFG_DENALI_PI_272 Register

1 EMIF_CTLCFG_DENALI_PI_272 Register (Offset = 2440h) [reset = 0h]

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Table 14-14593. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A440h**

Figure 14-4825. EMIF_CTLCFG_DENALI_PI_272 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_TINIT5_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TINIT5_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TINIT5_F2							
R/W							
0h							

Table 14-14595. EMIF_CTLCFG_DENALI_PI_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PI_TINIT5_F2	R/W	0h	DRAM tINIT5 value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.747 EMIF_CTLCFG_DENALI_PI_273 Register

1 EMIF_CTLCFG_DENALI_PI_273 Register (Offset = 2444h) [reset = 0h]

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Table 14-14596. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A444h

Figure 14-4826. EMIF_CTLCFG_DENALI_PI_273 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED54			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PI_RESERVED54							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_TXSNR_F2							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_TXSNR_F2							
R/W							
0h							

Table 14-14598. EMIF_CTLCFG_DENALI_PI_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_RESERVED54	R/W	0h	Reserved
15:0	PI_TXSNR_F2	R/W	0h	DRAM tXSNR value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.748 EMIF_CTLCFG_DENALI_PI_274 Register

1 EMIF_CTLCFG_DENALI_PI_274 Register (Offset = 2448h) [reset = 0h]

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Table 14-14599. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A448h**

Figure 14-4827. EMIF_CTLCFG_DENALI_PI_274 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_TZQCAL_F0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PI_TZQCAL_F0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED55</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_RESERVED55</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14601. EMIF_CTLCFG_DENALI_PI_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_TZQCAL_F0	R/W	0h	Holds the DRAM ZQCAL value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_RESERVED55	R/W	0h	Reserved

14.5.1.2.749 EMIF_CTLCFG_DENALI_PI_275 Register

1 EMIF_CTLCFG_DENALI_PI_275 Register (Offset = 244Ch) [reset = 0h]

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Table 14-14602. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A44Ch**

Figure 14-4828. EMIF_CTLCFG_DENALI_PI_275 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED56			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_RESERVED56							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED	PI_TZQLAT_F0						
NONE	R/W						
0h	0h						

Table 14-14604. EMIF_CTLCFG_DENALI_PI_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	PI_RESERVED56	R/W	0h	Reserved
7	RESERVED	NONE	0h	Reserved
6:0	PI_TZQLAT_F0	R/W	0h	Holds the DRAM ZQLAT value for frequency set 0 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.750 EMIF_CTLCFG_DENALI_PI_276 Register

1 EMIF_CTLCFG_DENALI_PI_276 Register (Offset = 2450h) [reset = 0h]

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Table 14-14605. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A450h

Figure 14-4829. EMIF_CTLCFG_DENALI_PI_276 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TZQCAL_F1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PI_TZQCAL_F1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED57			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PI_RESERVED57							
R/W							
0h							

Table 14-14607. EMIF_CTLCFG_DENALI_PI_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_TZQCAL_F1	R/W	0h	Holds the DRAM ZQCAL value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_RESERVED57	R/W	0h	Reserved

14.5.1.2.751 EMIF_CTLCFG_DENALI_PI_277 Register

1 EMIF_CTLCFG_DENALI_PI_277 Register (Offset = 2454h) [reset = 0h]

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Table 14-14608. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A454h**

Figure 14-4830. EMIF_CTLCFG_DENALI_PI_277 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PI_RESERVED58			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PI_RESERVED58							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED	PI_TZQLAT_F1						
NONE	R/W						
0h	0h						

Table 14-14610. EMIF_CTLCFG_DENALI_PI_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	PI_RESERVED58	R/W	0h	Reserved
7	RESERVED	NONE	0h	Reserved
6:0	PI_TZQLAT_F1	R/W	0h	Holds the DRAM ZQLAT value for frequency set 1 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.752 EMIF_CTLCFG_DENALI_PI_278 Register

1 EMIF_CTLCFG_DENALI_PI_278 Register (Offset = 2458h) [reset = 0h]

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Table 14-14611. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A458h**

Figure 14-4831. EMIF_CTLCFG_DENALI_PI_278 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_TZQCAL_F2			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PI_TZQCAL_F2							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED59			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PI_RESERVED59							
R/W							
0h							

Table 14-14613. EMIF_CTLCFG_DENALI_PI_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_TZQCAL_F2	R/W	0h	Holds the DRAM ZQCAL value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_RESERVED59	R/W	0h	Reserved

14.5.1.2.753 EMIF_CTLCFG_DENALI_PI_279 Register

1 EMIF_CTLCFG_DENALI_PI_279 Register (Offset = 245Ch) [reset = 0h]

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Table 14-14614. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A45Ch**

Figure 14-4832. EMIF_CTLCFG_DENALI_PI_279 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PI_RESERVED60</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_RESERVED60</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">PI_TZQLAT_F2</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-14616. EMIF_CTLCFG_DENALI_PI_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	PI_RESERVED60	R/W	0h	Reserved
7	RESERVED	NONE	0h	Reserved
6:0	PI_TZQLAT_F2	R/W	0h	Holds the DRAM ZQLAT value for frequency set 2 in cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.754 EMIF_CTLCFG_DENALI_PI_280 Register

1 EMIF_CTLCFG_DENALI_PI_280 Register (Offset = 2460h) [reset = 0h]

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Table 14-14617. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A460h

Figure 14-4833. EMIF_CTLCFG_DENALI_PI_280 Name Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESERVED62			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PI_RESERVED62							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PI_RESERVED61			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PI_RESERVED61							
R/W							
0h							

Table 14-14619. EMIF_CTLCFG_DENALI_PI_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PI_RESERVED62	R/W	0h	Reserved
15:12	RESERVED	NONE	0h	Reserved
11:0	PI_RESERVED61	R/W	0h	Reserved

14.5.1.2.755 EMIF_CTLCFG_DENALI_PI_281 Register

1 EMIF_CTLCFG_DENALI_PI_281 Register (Offset = 2464h) [reset = 0h]

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Table 14-14620. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A464h

Figure 14-4834. EMIF_CTLCFG_DENALI_PI_281 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_PREAMBLE_SUPPORT_F0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F0			
NONE				R/W			
0h				0h			

Table 14-14622. EMIF_CTLCFG_DENALI_PI_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_PREAMBLE_SUPPORT_F0	R/W	0h	bit0: Selection of one or two cycle preamble for read burst transfers. bit1: Selection of one or two cycles write burst transfers for NON-DDR5,one or multi[up to four] cycles write burst transfers for DDR5. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PI_WDQ_OSC_DELTA_INDEX_F2	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 2. If the value is n, the delay is 2^n/512 cycle. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PI_WDQ_OSC_DELTA_INDEX_F1	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 1. If the value is n, the delay is 2^n/512 cycle. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PI_WDQ_OSC_DELTA_INDEX_F0	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 0. If the value is n, the delay is 2^n/512 cycle. Reset Source: ctl_amod_g_rst_n

14.5.1.2.756 EMIF_CTLCFG_DENALI_PI_282 Register

1 EMIF_CTLCFG_DENALI_PI_282 Register (Offset = 2468h) [reset = 0h]

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Table 14-14623. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A468h

Figure 14-4835. EMIF_CTLCFG_DENALI_PI_282 Name Register

31	30	29	28	27	26	25	24
RESERVED					PI_MEMDATA_RATIO_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED					PI_MEMDATA_RATIO_0		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED						PI_PREAMBLE_SUPPORT_F2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PI_PREAMBLE_SUPPORT_F1	
NONE						R/W	
0h						0h	

Table 14-14625. EMIF_CTLCFG_DENALI_PI_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PI_MEMDATA_RATIO_1	R/W	0h	Defines the ratio of the DRAM device size on chip select 1 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PI_MEMDATA_RATIO_0	R/W	0h	Defines the ratio of the DRAM device size on chip select 0 to the memory data width. Program with the log2 ratio of the memory data width to the device data width. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_PREAMBLE_SUPPORT_F2	R/W	0h	bit0: Selection of one or two cycle preamble for read burst transfers. bit1: Selection of one or two cycles write burst transfers for NON-DDR5,one or multi[up to four] cycles write burst transfers for DDR5. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_PREAMBLE_SUPPORT_F1	R/W	0h	bit0: Selection of one or two cycle preamble for read burst transfers. bit1: Selection of one or two cycles write burst transfers for NON-DDR5,one or multi[up to four] cycles write burst transfers for DDR5. Reset Source: ctl_amod_g_rst_n

14.5.1.2.757 EMIF_CTLCFG_DENALI_PI_283 Register

1 EMIF_CTLCFG_DENALI_PI_283 Register (Offset = 246Ch) [reset = 0h]

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Table 14-14626. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A46Ch**

Figure 14-4836. EMIF_CTLCFG_DENALI_PI_283 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_ODT_WR_MAP_CS1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PI_ODT_RD_MAP_CS1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_ODT_WR_MAP_CS0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_ODT_RD_MAP_CS0	
NONE						R/W	
0h						0h	

Table 14-14628. EMIF_CTLCFG_DENALI_PI_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_ODT_WR_MAP_CS1	R/W	0h	Determines which chip[s] will have termination when a write occurs on chip select 1. Set bit X to enable termination on csX when cs1 is performing a write. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PI_ODT_RD_MAP_CS1	R/W	0h	Determines which chip[s] will have termination when a read occurs on chip select 1. Set bit X to enable termination on csX when cs1 is performing a read. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_ODT_WR_MAP_CS0	R/W	0h	Determines which chip[s] will have termination when a write occurs on chip select 0. Set bit X to enable termination on csX when cs0 is performing a write. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_ODT_RD_MAP_CS0	R/W	0h	Determines which chip[s] will have termination when a read occurs on chip select 0. Set bit X to enable termination on csX when cs0 is performing a read. Reset Source: ctl_amod_g_rst_n

14.5.1.2.758 EMIF_CTLCFG_DENALI_PI_284 Register

1 EMIF_CTLCFG_DENALI_PI_284 Register (Offset = 2470h) [reset = 0h]

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Table 14-14629. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A470h

Figure 14-4837. EMIF_CTLCFG_DENALI_PI_284 Name Register

31	30	29	28	27	26	25	24
RESERVED	PI_VREF_VAL_DEV1_1						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	PI_VREF_VAL_DEV1_0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED	PI_VREF_VAL_DEV0_1						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PI_VREF_VAL_DEV0_0						
NONE	R/W						
0h	0h						

Table 14-14631. EMIF_CTLCFG_DENALI_PI_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PI_VREF_VAL_DEV1_1	R/W	0h	Defines the range and value for VREF training for DRAM 1 for CS 1. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PI_VREF_VAL_DEV1_0	R/W	0h	Defines the range and value for VREF training for DRAM 1 for CS 0. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PI_VREF_VAL_DEV0_1	R/W	0h	Defines the range and value for VREF training for DRAM 0 for CS 1. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PI_VREF_VAL_DEV0_0	R/W	0h	Defines the range and value for VREF training for DRAM 0 for CS 0. If the PI_VREF_PDA_EN parameter is not set, device 0 values are used for all devices. Reset Source: ctl_amod_g_rst_n

14.5.1.2.759 EMIF_CTLCFG_DENALI_PI_285 Register

1 EMIF_CTLCFG_DENALI_PI_285 Register (Offset = 2474h) [reset = 0h]

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Table 14-14632. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A474h**

Figure 14-4838. EMIF_CTLCFG_DENALI_PI_285 Name Register

31	30	29	28	27	26	25	24
RESERVED		PI_MR6_VREF_0_1					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PI_MR6_VREF_0_0					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PI_SLICE_PER_DEV_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PI_SLICE_PER_DEV_0	
NONE						R/W	
0h						0h	

Table 14-14634. EMIF_CTLCFG_DENALI_PI_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PI_MR6_VREF_0_1	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PI_MR6_VREF_0_0	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_SLICE_PER_DEV_1	R/W	0h	Indicates the number of data slices per memory device. The device width divided by 8. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_SLICE_PER_DEV_0	R/W	0h	Indicates the number of data slices per memory device. The device width divided by 8. Reset Source: ctl_amod_g_rst_n

14.5.1.2.760 EMIF_CTLCFG_DENALI_PI_286 Register

1 EMIF_CTLCFG_DENALI_PI_286 Register (Offset = 2478h) [reset = 0h]

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Table 14-14635. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A478h

Figure 14-4839. EMIF_CTLCFG_DENALI_PI_286 Name Register

31	30	29	28	27	26	25	24
PI_MR15_DATA_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR13_DATA_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PI_MR6_VREF_1_1					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PI_MR6_VREF_1_0					
NONE		R					
0h		0h					

Table 14-14637. EMIF_CTLCFG_DENALI_PI_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR15_DATA_0	R/W	0h	Data to program into memory mode register 15 for chip select 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR13_DATA_0	R/W	0h	Data to program into memory mode register 13 for chip select 0. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PI_MR6_VREF_1_1	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PI_MR6_VREF_1_0	R	0h	The parameter stores the vref value of every devices of the same CS. It is updated after WDQLVL PDA mode completed. READ-ONLY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.761 EMIF_CTLCFG_DENALI_PI_287 Register

1 EMIF_CTLCFG_DENALI_PI_287 Register (Offset = 247Ch) [reset = 0h]

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Table 14-14638. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A47Ch**

Figure 14-4840. EMIF_CTLCFG_DENALI_PI_287 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PI_MR20_DATA_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR17_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR16_DATA_0							
R/W							
0h							

Table 14-14640. EMIF_CTLCFG_DENALI_PI_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PI_MR20_DATA_0	R/W	0h	Data to program into memory mode register 20 for chip select 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR17_DATA_0	R/W	0h	Data to program into memory mode register 17 for chip select 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR16_DATA_0	R/W	0h	Data to program into memory mode register 16 for chip select 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.762 EMIF_CTLCFG_DENALI_PI_288 Register

1 EMIF_CTLCFG_DENALI_PI_288 Register (Offset = 2480h) [reset = 0h]

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Table 14-14641. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A480h**

Figure 14-4841. EMIF_CTLCFG_DENALI_PI_288 Name Register

31	30	29	28	27	26	25	24
PI_MR40_DATA_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR32_DATA_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR32_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR32_DATA_0							
R/W							
0h							

Table 14-14643. EMIF_CTLCFG_DENALI_PI_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR40_DATA_0	R/W	0h	Data to program into memory mode register 40 for chip select 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR32_DATA_0	R/W	0h	Data to program into memory mode register 32 for chip select 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.763 EMIF_CTLCFG_DENALI_PI_289 Register

1 EMIF_CTLCFG_DENALI_PI_289 Register (Offset = 2484h) [reset = 0h]

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Table 14-14644. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A484h**

Figure 14-4842. EMIF_CTLCFG_DENALI_PI_289 Name Register

31	30	29	28	27	26	25	24
PI_MR17_DATA_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR16_DATA_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR15_DATA_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR13_DATA_1							
R/W							
0h							

Table 14-14646. EMIF_CTLCFG_DENALI_PI_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR17_DATA_1	R/W	0h	Data to program into memory mode register 17 for chip select 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR16_DATA_1	R/W	0h	Data to program into memory mode register 16 for chip select 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR15_DATA_1	R/W	0h	Data to program into memory mode register 15 for chip select 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR13_DATA_1	R/W	0h	Data to program into memory mode register 13 for chip select 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.764 EMIF_CTLCFG_DENALI_PI_290 Register

1 EMIF_CTLCFG_DENALI_PI_290 Register (Offset = 2488h) [reset = 0h]

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Table 14-14647. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A488h**

Figure 14-4843. EMIF_CTLCFG_DENALI_PI_290 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MR32_DATA_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR32_DATA_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR32_DATA_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR20_DATA_1							
R/W							
0h							

Table 14-14649. EMIF_CTLCFG_DENALI_PI_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	PI_MR32_DATA_1	R/W	0h	Data to program into memory mode register 32 for chip select 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR20_DATA_1	R/W	0h	Data to program into memory mode register 20 for chip select 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.765 EMIF_CTLCFG_DENALI_PI_291 Register

1 EMIF_CTLCFG_DENALI_PI_291 Register (Offset = 248Ch) [reset = 0h]

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Table 14-14650. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A48Ch**

Figure 14-4844. EMIF_CTLCFG_DENALI_PI_291 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_CS_MUX_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_CKE_MUX_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PI_CKE_MUX_0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR40_DATA_1							
R/W							
0h							

Table 14-14652. EMIF_CTLCFG_DENALI_PI_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_CS_MUX_0	R/W	0h	Command pin CS_0 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_CKE_MUX_1	R/W	0h	Command pin CKE_1 mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_CKE_MUX_0	R/W	0h	Command pin CKE_0 mux selector Reset Source: ctl_amod_g_rst_n
7:0	PI_MR40_DATA_1	R/W	0h	Data to program into memory mode register 40 for chip select 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.766 EMIF_CTLCFG_DENALI_PI_292 Register

1 EMIF_CTLCFG_DENALI_PI_292 Register (Offset = 2490h) [reset = 0h]

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Table 14-14653. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A490h**

Figure 14-4845. EMIF_CTLCFG_DENALI_PI_292 Name Register

31	30	29	28	27	26	25	24
RESERVED			PI_RESET_N_MUX_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PI_ODT_MUX_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PI_ODT_MUX_0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_CS_MUX_1				
NONE			R/W				
0h			0h				

Table 14-14655. EMIF_CTLCFG_DENALI_PI_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PI_RESET_N_MUX_0	R/W	0h	Command pin RESET_N_0 mux selector Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PI_ODT_MUX_1	R/W	0h	Command pin ODT_1 mux selector Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PI_ODT_MUX_0	R/W	0h	Command pin ODT_0 mux selector Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_CS_MUX_1	R/W	0h	Command pin CS_1 mux selector Reset Source: ctl_amod_g_rst_n

14.5.1.2.767 EMIF_CTLCFG_DENALI_PI_293 Register

1 EMIF_CTLCFG_DENALI_PI_293 Register (Offset = 2494h) [reset = 0h]

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Table 14-14656. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A494h

Figure 14-4846. EMIF_CTLCFG_DENALI_PI_293 Name Register

31	30	29	28	27	26	25	24
RESERVED							PI_MRSINGLE_DATA_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MRSINGLE_DATA_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MRSINGLE_DATA_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PI_RESET_N_MUX_1				
NONE			R/W				
0h			0h				

Table 14-14658. EMIF_CTLCFG_DENALI_PI_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:8	PI_MRSINGLE_DATA_0	R/W	0h	Data to program into memory mode register single write to chip select 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PI_RESET_N_MUX_1	R/W	0h	Command pin RESET_N_1 mux selector Reset Source: ctl_amod_g_rst_n

14.5.1.2.768 EMIF_CTLCFG_DENALI_PI_294 Register

1 EMIF_CTLCFG_DENALI_PI_294 Register (Offset = 2498h) [reset = 1000000h]

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Table 14-14659. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A498h

Figure 14-4847. EMIF_CTLCFG_DENALI_PI_294 Name Register

31	30	29	28	27	26	25	24
RESERVED						PI_ZQ_CAL_START_MAP_0	
NONE						R/W	
0h						1h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MRSINGLE_DATA_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MRSINGLE_DATA_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MRSINGLE_DATA_1							
R/W							
0h							

Table 14-14661. EMIF_CTLCFG_DENALI_PI_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PI_ZQ_CAL_START_MAP_0	R/W	1h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 0 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MRSINGLE_DATA_1	R/W	0h	Data to program into memory mode register single write to chip select 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.769 EMIF_CTLCFG_DENALI_PI_295 Register

1 EMIF_CTLCFG_DENALI_PI_295 Register (Offset = 249Ch) [reset = 20201h]

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Table 14-14662. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A49Ch

Figure 14-4848. EMIF_CTLCFG_DENALI_PI_295 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PI_ZQ_CAL_LATCH_MAP_1	
NONE						R/W	
0h						2h	
15	14	13	12	11	10	9	8
RESERVED						PI_ZQ_CAL_START_MAP_1	
NONE						R/W	
0h						2h	
7	6	5	4	3	2	1	0
RESERVED						PI_ZQ_CAL_LATCH_MAP_0	
NONE						R/W	
0h						1h	

Table 14-14664. EMIF_CTLCFG_DENALI_PI_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PI_ZQ_CAL_LATCH_MAP_1	R/W	2h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 1 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PI_ZQ_CAL_START_MAP_1	R/W	2h	Defines which chip select[s] will receive ZQ calibration start commands simultaneously on iteration 1 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PI_ZQ_CAL_LATCH_MAP_0	R/W	1h	Defines which chip select[s] will receive ZQ calibration latch commands simultaneously on iteration 0 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands. Reset Source: ctl_amod_g_rst_n

14.5.1.2.770 EMIF_CTLCFG_DENALI_PI_296 Register

1 EMIF_CTLCFG_DENALI_PI_296 Register (Offset = 24A0h) [reset = 0h]

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Table 14-14665. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A4A0h

Figure 14-4849. EMIF_CTLCFG_DENALI_PI_296 Name Register

31	30	29	28	27	26	25	24
PI_DQS_OSC_BASE_VALUE_0_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_DQS_OSC_BASE_VALUE_0_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_DQS_OSC_BASE_VALUE_0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_DQS_OSC_BASE_VALUE_0_0							
R/W							
0h							

Table 14-14667. EMIF_CTLCFG_DENALI_PI_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PI_DQS_OSC_BASE_VALUE_0_1	R/W	0h	Base value for comparison of oscillator measurement for device 0 of rank 1 Reset Source: ctl_amod_g_rst_n
15:0	PI_DQS_OSC_BASE_VALUE_0_0	R/W	0h	Base value for comparison of oscillator measurement for device 0 of rank 0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.771 EMIF_CTLCFG_DENALI_PI_297 Register

1 EMIF_CTLCFG_DENALI_PI_297 Register (Offset = 24A4h) [reset = 0h]

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Table 14-14668. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A4A4h

Figure 14-4850. EMIF_CTLCFG_DENALI_PI_297 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR0_DATA_F0_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR0_DATA_F0_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR0_DATA_F0_0							
R/W							
0h							

Table 14-14670. EMIF_CTLCFG_DENALI_PI_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F0_0	R/W	0h	Data to program into memory mode register 0 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.772 EMIF_CTLCFG_DENALI_PI_298 Register

1 EMIF_CTLCFG_DENALI_PI_298 Register (Offset = 24A8h) [reset = 0h]

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Table 14-14671. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4A8h**

Figure 14-4851. EMIF_CTLCFG_DENALI_PI_298 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR1_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR1_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR1_DATA_F0_0							
R/W							
0h							

Table 14-14673. EMIF_CTLCFG_DENALI_PI_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F0_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.773 EMIF_CTLCFG_DENALI_PI_299 Register

1 EMIF_CTLCFG_DENALI_PI_299 Register (Offset = 24ACh) [reset = 0h]

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Table 14-14674. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4ACh**

Figure 14-4852. EMIF_CTLCFG_DENALI_PI_299 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F0_0							
R/W							
0h							

Table 14-14676. EMIF_CTLCFG_DENALI_PI_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F0_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.774 EMIF_CTLCFG_DENALI_PI_300 Register

1 EMIF_CTLCFG_DENALI_PI_300 Register (Offset = 24B0h) [reset = 0h]

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Table 14-14677. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A4B0h

Figure 14-4853. EMIF_CTLCFG_DENALI_PI_300 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR3_DATA_F0_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR3_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR3_DATA_F0_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14679. EMIF_CTLCFG_DENALI_PI_300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F0_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.775 EMIF_CTLCFG_DENALI_PI_301 Register

1 EMIF_CTLCFG_DENALI_PI_301 Register (Offset = 24B4h) [reset = 0h]

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Table 14-14680. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4B4h**

Figure 14-4854. EMIF_CTLCFG_DENALI_PI_301 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR4_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR4_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR4_DATA_F0_0							
R/W							
0h							

Table 14-14682. EMIF_CTLCFG_DENALI_PI_301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F0_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.776 EMIF_CTLCFG_DENALI_PI_302 Register

1 EMIF_CTLCFG_DENALI_PI_302 Register (Offset = 24B8h) [reset = 0h]

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Table 14-14683. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A4B8h

Figure 14-4855. EMIF_CTLCFG_DENALI_PI_302 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F0_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F0_0							
R/W							
0h							

Table 14-14685. EMIF_CTLCFG_DENALI_PI_302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F0_0	R/W	0h	Data to program into memory mode register 5 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.777 EMIF_CTLCFG_DENALI_PI_303 Register

1 EMIF_CTLCFG_DENALI_PI_303 Register (Offset = 24BCh) [reset = 0h]

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Table 14-14686. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4BCh**

Figure 14-4856. EMIF_CTLCFG_DENALI_PI_303 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F0_0							
R/W							
0h							

23	22	21	20	19	18	17	16
RESERVED							PI_MR6_DATA_F0_0
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
PI_MR6_DATA_F0_0							
R/W							
0h							

7	6	5	4	3	2	1	0
PI_MR6_DATA_F0_0							
R/W							
0h							

Table 14-14688. EMIF_CTLCFG_DENALI_PI_303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F0_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F0_0	R/W	0h	Data to program into memory mode register 6 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.778 EMIF_CTLCFG_DENALI_PI_304 Register

1 EMIF_CTLCFG_DENALI_PI_304 Register (Offset = 24C0h) [reset = 0h]

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Table 14-14689. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4C0h**

Figure 14-4857. EMIF_CTLCFG_DENALI_PI_304 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F0_0							
R/W							
0h							

Table 14-14691. EMIF_CTLCFG_DENALI_PI_304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F0_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F0_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F0_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F0_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.779 EMIF_CTLCFG_DENALI_PI_305 Register

1 EMIF_CTLCFG_DENALI_PI_305 Register (Offset = 24C4h) [reset = 0h]

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Table 14-14692. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A4C4h

Figure 14-4858. EMIF_CTLCFG_DENALI_PI_305 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR0_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR0_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR0_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14694. EMIF_CTLCFG_DENALI_PI_305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F1_0	R/W	0h	Data to program into memory mode register 0 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.780 EMIF_CTLCFG_DENALI_PI_306 Register

1 EMIF_CTLCFG_DENALI_PI_306 Register (Offset = 24C8h) [reset = 0h]

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Table 14-14695. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4C8h**

Figure 14-4859. EMIF_CTLCFG_DENALI_PI_306 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR1_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR1_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR1_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14697. EMIF_CTLCFG_DENALI_PI_306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F1_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.781 EMIF_CTLCFG_DENALI_PI_307 Register

1 EMIF_CTLCFG_DENALI_PI_307 Register (Offset = 24CCh) [reset = 0h]

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Table 14-14698. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A4CCh

Figure 14-4860. EMIF_CTLCFG_DENALI_PI_307 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F1_0							
R/W							
0h							

Table 14-14700. EMIF_CTLCFG_DENALI_PI_307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F1_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.782 EMIF_CTLCFG_DENALI_PI_308 Register

1 EMIF_CTLCFG_DENALI_PI_308 Register (Offset = 24D0h) [reset = 0h]

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Table 14-14701. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4D0h**

Figure 14-4861. EMIF_CTLCFG_DENALI_PI_308 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F1_0							
R/W							
0h							

Table 14-14703. EMIF_CTLCFG_DENALI_PI_308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F1_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.783 EMIF_CTLCFG_DENALI_PI_309 Register

1 EMIF_CTLCFG_DENALI_PI_309 Register (Offset = 24D4h) [reset = 0h]

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Table 14-14704. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A4D4h

Figure 14-4862. EMIF_CTLCFG_DENALI_PI_309 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR4_DATA_F1_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR4_DATA_F1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR4_DATA_F1_0							
R/W							
0h							

Table 14-14706. EMIF_CTLCFG_DENALI_PI_309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F1_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.784 EMIF_CTLCFG_DENALI_PI_310 Register

1 EMIF_CTLCFG_DENALI_PI_310 Register (Offset = 24D8h) [reset = 0h]

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Table 14-14707. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4D8h**

Figure 14-4863. EMIF_CTLCFG_DENALI_PI_310 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F1_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F1_0							
R/W							
0h							

Table 14-14709. EMIF_CTLCFG_DENALI_PI_310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F1_0	R/W	0h	Data to program into memory mode register 5 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.785 EMIF_CTLCFG_DENALI_PI_311 Register

1 EMIF_CTLCFG_DENALI_PI_311 Register (Offset = 24DCh) [reset = 0h]

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Table 14-14710. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4DCh**

Figure 14-4864. EMIF_CTLCFG_DENALI_PI_311 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_MR11_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR6_DATA_F1_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR6_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR6_DATA_F1_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14712. EMIF_CTLCFG_DENALI_PI_311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F1_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F1_0	R/W	0h	Data to program into memory mode register 6 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.786 EMIF_CTLCFG_DENALI_PI_312 Register

1 EMIF_CTLCFG_DENALI_PI_312 Register (Offset = 24E0h) [reset = 0h]

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Table 14-14713. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4E0h**

Figure 14-4865. EMIF_CTLCFG_DENALI_PI_312 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F1_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F1_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F1_0							
R/W							
0h							

Table 14-14715. EMIF_CTLCFG_DENALI_PI_312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F1_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F1_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F1_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F1_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.787 EMIF_CTLCFG_DENALI_PI_313 Register

1 EMIF_CTLCFG_DENALI_PI_313 Register (Offset = 24E4h) [reset = 0h]

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Table 14-14716. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4E4h**

Figure 14-4866. EMIF_CTLCFG_DENALI_PI_313 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F2_0							
R/W							
0h							

Table 14-14718. EMIF_CTLCFG_DENALI_PI_313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F2_0	R/W	0h	Data to program into memory mode register 0 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.788 EMIF_CTLCFG_DENALI_PI_314 Register

1 EMIF_CTLCFG_DENALI_PI_314 Register (Offset = 24E8h) [reset = 0h]

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Table 14-14719. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4E8h**

Figure 14-4867. EMIF_CTLCFG_DENALI_PI_314 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR1_DATA_F2_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR1_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR1_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14721. EMIF_CTLCFG_DENALI_PI_314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F2_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.789 EMIF_CTLCFG_DENALI_PI_315 Register

1 EMIF_CTLCFG_DENALI_PI_315 Register (Offset = 24ECh) [reset = 0h]

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Table 14-14722. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A4ECh

Figure 14-4868. EMIF_CTLCFG_DENALI_PI_315 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_0							
R/W							
0h							

Table 14-14724. EMIF_CTLCFG_DENALI_PI_315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F2_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.790 EMIF_CTLCFG_DENALI_PI_316 Register

1 EMIF_CTLCFG_DENALI_PI_316 Register (Offset = 24F0h) [reset = 0h]

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Table 14-14725. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4F0h**

Figure 14-4869. EMIF_CTLCFG_DENALI_PI_316 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F2_0							
R/W							
0h							

Table 14-14727. EMIF_CTLCFG_DENALI_PI_316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F2_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.791 EMIF_CTLCFG_DENALI_PI_317 Register

1 EMIF_CTLCFG_DENALI_PI_317 Register (Offset = 24F4h) [reset = 0h]

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Table 14-14728. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4F4h**

Figure 14-4870. EMIF_CTLCFG_DENALI_PI_317 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR4_DATA_F2_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14730. EMIF_CTLCFG_DENALI_PI_317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F2_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.792 EMIF_CTLCFG_DENALI_PI_318 Register

1 EMIF_CTLCFG_DENALI_PI_318 Register (Offset = 24F8h) [reset = 0h]

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Table 14-14731. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4F8h**

Figure 14-4871. EMIF_CTLCFG_DENALI_PI_318 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F2_0							
R/W							
0h							

Table 14-14733. EMIF_CTLCFG_DENALI_PI_318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F2_0	R/W	0h	Data to program into memory mode register 5 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.793 EMIF_CTLCFG_DENALI_PI_319 Register

1 EMIF_CTLCFG_DENALI_PI_319 Register (Offset = 24FCh) [reset = 0h]

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Table 14-14734. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A4FCh**

Figure 14-4872. EMIF_CTLCFG_DENALI_PI_319 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F2_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR6_DATA_F2_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR6_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR6_DATA_F2_0							
R/W							
0h							

Table 14-14736. EMIF_CTLCFG_DENALI_PI_319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F2_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F2_0	R/W	0h	Data to program into memory mode register 6 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.794 EMIF_CTLCFG_DENALI_PI_320 Register

1 EMIF_CTLCFG_DENALI_PI_320 Register (Offset = 2500h) [reset = 0h]

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Table 14-14737. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A500h**

Figure 14-4873. EMIF_CTLCFG_DENALI_PI_320 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F2_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F2_0							
R/W							
0h							

Table 14-14739. EMIF_CTLCFG_DENALI_PI_320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F2_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F2_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F2_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F2_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.795 EMIF_CTLCFG_DENALI_PI_321 Register

1 EMIF_CTLCFG_DENALI_PI_321 Register (Offset = 2504h) [reset = 0h]

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Table 14-14740. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A504h**

Figure 14-4874. EMIF_CTLCFG_DENALI_PI_321 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F0_1							
R/W							
0h							

Table 14-14742. EMIF_CTLCFG_DENALI_PI_321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F0_1	R/W	0h	Data to program into memory mode register 0 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.796 EMIF_CTLCFG_DENALI_PI_322 Register

1 EMIF_CTLCFG_DENALI_PI_322 Register (Offset = 2508h) [reset = 0h]

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Table 14-14743. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A508h

Figure 14-4875. EMIF_CTLCFG_DENALI_PI_322 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR1_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR1_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR1_DATA_F0_1							
R/W							
0h							

Table 14-14745. EMIF_CTLCFG_DENALI_PI_322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F0_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.797 EMIF_CTLCFG_DENALI_PI_323 Register

1 EMIF_CTLCFG_DENALI_PI_323 Register (Offset = 250Ch) [reset = 0h]

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Table 14-14746. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A50Ch

Figure 14-4876. EMIF_CTLCFG_DENALI_PI_323 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR2_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR2_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR2_DATA_F0_1							
R/W							
0h							

Table 14-14748. EMIF_CTLCFG_DENALI_PI_323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F0_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.798 EMIF_CTLCFG_DENALI_PI_324 Register

1 EMIF_CTLCFG_DENALI_PI_324 Register (Offset = 2510h) [reset = 0h]

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Table 14-14749. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A510h**

Figure 14-4877. EMIF_CTLCFG_DENALI_PI_324 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR3_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR3_DATA_F0_1							
R/W							
0h							

Table 14-14751. EMIF_CTLCFG_DENALI_PI_324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F0_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.799 EMIF_CTLCFG_DENALI_PI_325 Register

1 EMIF_CTLCFG_DENALI_PI_325 Register (Offset = 2514h) [reset = 0h]

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Table 14-14752. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A514h**

Figure 14-4878. EMIF_CTLCFG_DENALI_PI_325 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR4_DATA_F0_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR4_DATA_F0_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14754. EMIF_CTLCFG_DENALI_PI_325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F0_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.800 EMIF_CTLCFG_DENALI_PI_326 Register

1 EMIF_CTLCFG_DENALI_PI_326 Register (Offset = 2518h) [reset = 0h]

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Table 14-14755. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A518h**

Figure 14-4879. EMIF_CTLCFG_DENALI_PI_326 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F0_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F0_1							
R/W							
0h							

Table 14-14757. EMIF_CTLCFG_DENALI_PI_326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F0_1	R/W	0h	Data to program into memory mode register 5 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.801 EMIF_CTLCFG_DENALI_PI_327 Register

1 EMIF_CTLCFG_DENALI_PI_327 Register (Offset = 251Ch) [reset = 0h]

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Table 14-14758. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A51Ch**

Figure 14-4880. EMIF_CTLCFG_DENALI_PI_327 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F0_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR6_DATA_F0_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR6_DATA_F0_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR6_DATA_F0_1							
R/W							
0h							

Table 14-14760. EMIF_CTLCFG_DENALI_PI_327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F0_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F0_1	R/W	0h	Data to program into memory mode register 6 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.802 EMIF_CTLCFG_DENALI_PI_328 Register

1 EMIF_CTLCFG_DENALI_PI_328 Register (Offset = 2520h) [reset = 0h]

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Table 14-14761. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A520h**

Figure 14-4881. EMIF_CTLCFG_DENALI_PI_328 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F0_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F0_1							
R/W							
0h							

Table 14-14763. EMIF_CTLCFG_DENALI_PI_328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F0_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F0_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F0_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F0_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.803 EMIF_CTLCFG_DENALI_PI_329 Register

1 EMIF_CTLCFG_DENALI_PI_329 Register (Offset = 2524h) [reset = 0h]

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Table 14-14764. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A524h**

Figure 14-4882. EMIF_CTLCFG_DENALI_PI_329 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR0_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR0_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR0_DATA_F1_1							
R/W							
0h							

Table 14-14766. EMIF_CTLCFG_DENALI_PI_329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F1_1	R/W	0h	Data to program into memory mode register 0 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.804 EMIF_CTLCFG_DENALI_PI_330 Register

1 EMIF_CTLCFG_DENALI_PI_330 Register (Offset = 2528h) [reset = 0h]

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Table 14-14767. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A528h**

Figure 14-4883. EMIF_CTLCFG_DENALI_PI_330 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR1_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR1_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR1_DATA_F1_1							
R/W							
0h							

Table 14-14769. EMIF_CTLCFG_DENALI_PI_330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F1_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.805 EMIF_CTLCFG_DENALI_PI_331 Register

1 EMIF_CTLCFG_DENALI_PI_331 Register (Offset = 252Ch) [reset = 0h]

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Table 14-14770. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A52Ch**

Figure 14-4884. EMIF_CTLCFG_DENALI_PI_331 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F1_1							
R/W							
0h							

Table 14-14772. EMIF_CTLCFG_DENALI_PI_331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F1_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.806 EMIF_CTLCFG_DENALI_PI_332 Register

1 EMIF_CTLCFG_DENALI_PI_332 Register (Offset = 2530h) [reset = 0h]

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Table 14-14773. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A530h**

Figure 14-4885. EMIF_CTLCFG_DENALI_PI_332 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							PI_MR3_DATA_F1_1
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
PI_MR3_DATA_F1_1							
R/W							
0h							

7	6	5	4	3	2	1	0
PI_MR3_DATA_F1_1							
R/W							
0h							

Table 14-14775. EMIF_CTLCFG_DENALI_PI_332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F1_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.807 EMIF_CTLCFG_DENALI_PI_333 Register

1 EMIF_CTLCFG_DENALI_PI_333 Register (Offset = 2534h) [reset = 0h]

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Table 14-14776. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A534h

Figure 14-4886. EMIF_CTLCFG_DENALI_PI_333 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR4_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR4_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR4_DATA_F1_1							
R/W							
0h							

Table 14-14778. EMIF_CTLCFG_DENALI_PI_333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F1_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.808 EMIF_CTLCFG_DENALI_PI_334 Register

1 EMIF_CTLCFG_DENALI_PI_334 Register (Offset = 2538h) [reset = 0h]

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Table 14-14779. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A538h**

Figure 14-4887. EMIF_CTLCFG_DENALI_PI_334 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR5_DATA_F1_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR5_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR5_DATA_F1_1							
R/W							
0h							

Table 14-14781. EMIF_CTLCFG_DENALI_PI_334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F1_1	R/W	0h	Data to program into memory mode register 5 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.809 EMIF_CTLCFG_DENALI_PI_335 Register

1 EMIF_CTLCFG_DENALI_PI_335 Register (Offset = 253Ch) [reset = 0h]

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Table 14-14782. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A53Ch**

Figure 14-4888. EMIF_CTLCFG_DENALI_PI_335 Name Register

31	30	29	28	27	26	25	24
PI_MR11_DATA_F1_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR6_DATA_F1_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR6_DATA_F1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR6_DATA_F1_1							
R/W							
0h							

Table 14-14784. EMIF_CTLCFG_DENALI_PI_335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F1_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F1_1	R/W	0h	Data to program into memory mode register 6 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.810 EMIF_CTLCFG_DENALI_PI_336 Register

1 EMIF_CTLCFG_DENALI_PI_336 Register (Offset = 2540h) [reset = 0h]

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Table 14-14785. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A540h**

Figure 14-4889. EMIF_CTLCFG_DENALI_PI_336 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F1_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PI_MR22_DATA_F1_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR14_DATA_F1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR12_DATA_F1_1							
R/W							
0h							

Table 14-14787. EMIF_CTLCFG_DENALI_PI_336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F1_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F1_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F1_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F1_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.811 EMIF_CTLCFG_DENALI_PI_337 Register

1 EMIF_CTLCFG_DENALI_PI_337 Register (Offset = 2544h) [reset = 0h]

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Table 14-14788. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A544h**

Figure 14-4890. EMIF_CTLCFG_DENALI_PI_337 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR0_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR0_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR0_DATA_F2_1							
R/W							
0h							

Table 14-14790. EMIF_CTLCFG_DENALI_PI_337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR0_DATA_F2_1	R/W	0h	Data to program into memory mode register 0 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.812 EMIF_CTLCFG_DENALI_PI_338 Register

1 EMIF_CTLCFG_DENALI_PI_338 Register (Offset = 2548h) [reset = 0h]

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Table 14-14791. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A548h

Figure 14-4891. EMIF_CTLCFG_DENALI_PI_338 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR1_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR1_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR1_DATA_F2_1							
R/W							
0h							

Table 14-14793. EMIF_CTLCFG_DENALI_PI_338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR1_DATA_F2_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.813 EMIF_CTLCFG_DENALI_PI_339 Register

1 EMIF_CTLCFG_DENALI_PI_339 Register (Offset = 254Ch) [reset = 0h]

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Table 14-14794. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A54Ch**

Figure 14-4892. EMIF_CTLCFG_DENALI_PI_339 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR2_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR2_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_1							
R/W							
0h							

Table 14-14796. EMIF_CTLCFG_DENALI_PI_339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR2_DATA_F2_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.814 EMIF_CTLCFG_DENALI_PI_340 Register

1 EMIF_CTLCFG_DENALI_PI_340 Register (Offset = 2550h) [reset = 0h]

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Table 14-14797. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 A550h

Figure 14-4893. EMIF_CTLCFG_DENALI_PI_340 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PI_MR3_DATA_F2_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PI_MR3_DATA_F2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PI_MR3_DATA_F2_1							
R/W							
0h							

Table 14-14799. EMIF_CTLCFG_DENALI_PI_340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR3_DATA_F2_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.815 EMIF_CTLCFG_DENALI_PI_341 Register

1 EMIF_CTLCFG_DENALI_PI_341 Register (Offset = 2554h) [reset = 0h]

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Table 14-14800. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A554h**

Figure 14-4894. EMIF_CTLCFG_DENALI_PI_341 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR4_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR4_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR4_DATA_F2_1							
R/W							
0h							

Table 14-14802. EMIF_CTLCFG_DENALI_PI_341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR4_DATA_F2_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.816 EMIF_CTLCFG_DENALI_PI_342 Register

1 EMIF_CTLCFG_DENALI_PI_342 Register (Offset = 2558h) [reset = 0h]

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Table 14-14803. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A558h**

Figure 14-4895. EMIF_CTLCFG_DENALI_PI_342 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MR5_DATA_F2_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PI_MR5_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR5_DATA_F2_1							
R/W							
0h							

Table 14-14805. EMIF_CTLCFG_DENALI_PI_342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR5_DATA_F2_1	R/W	0h	Data to program into memory mode register 5 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.817 EMIF_CTLCFG_DENALI_PI_343 Register

1 EMIF_CTLCFG_DENALI_PI_343 Register (Offset = 255Ch) [reset = 0h]

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Table 14-14806. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A55Ch**

Figure 14-4896. EMIF_CTLCFG_DENALI_PI_343 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PI_MR11_DATA_F2_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PI_MR6_DATA_F2_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PI_MR6_DATA_F2_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PI_MR6_DATA_F2_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14808. EMIF_CTLCFG_DENALI_PI_343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR11_DATA_F2_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PI_MR6_DATA_F2_1	R/W	0h	Data to program into memory mode register 6 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.818 EMIF_CTLCFG_DENALI_PI_344 Register

1 EMIF_CTLCFG_DENALI_PI_344 Register (Offset = 2560h) [reset = 0h]

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Table 14-14809. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 A560h**

Figure 14-4897. EMIF_CTLCFG_DENALI_PI_344 Name Register

31	30	29	28	27	26	25	24
PI_MR23_DATA_F2_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PI_MR22_DATA_F2_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PI_MR14_DATA_F2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PI_MR12_DATA_F2_1							
R/W							
0h							

Table 14-14811. EMIF_CTLCFG_DENALI_PI_344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PI_MR23_DATA_F2_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
23:16	PI_MR22_DATA_F2_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
15:8	PI_MR14_DATA_F2_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n
7:0	PI_MR12_DATA_F2_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.819 EMIF_CTLCFG_DENALI_PHY_0 Register

1 EMIF_CTLCFG_DENALI_PHY_0 Register (Offset = 4000h) [reset = 0h]

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Table 14-14812. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C000h

Figure 14-4898. EMIF_CTLCFG_DENALI_PHY_0 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WR_BYPASS_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_0						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_LP4_BOOT_RX_PCLK_CLK_SEL_0		
NONE					R/W		
0h					0h		

Table 14-14814. EMIF_CTLCFG_DENALI_PHY_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WR_BYPASS_SLAVE_DELAY_0	R/W	0h	Write data clock bypass mode target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_0	R/W	0h	Controls PCLK/PARK pin for pad for slice 0 with boot frequency. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_LP4_BOOT_RX_PCLK_CLK_SEL_0	R/W	0h	RX_PCLK boot clock frequency selection for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.820 EMIF_CTLCFG_DENALI_PHY_1 Register

1 EMIF_CTLCFG_DENALI_PHY_1 Register (Offset = 4004h) [reset = 0h]

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Table 14-14815. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C004h

Figure 14-4899. EMIF_CTLCFG_DENALI_PHY_1 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_0			
NONE				R/W			
0h				0h			

Table 14-14817. EMIF_CTLCFG_DENALI_PHY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_WRITE_PATH_LAT_ADD_BYPASS_0	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0	R/W	0h	Write DQS bypass mode target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_BYPASS_0	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.821 EMIF_CTLCFG_DENALI_PHY_2 Register

1 EMIF_CTLCFG_DENALI_PHY_2 Register (Offset = 4008h) [reset = 0h]

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Table 14-14818. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C008h**

Figure 14-4900. EMIF_CTLCFG_DENALI_PHY_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_BYPASS_TWO_CYC_PREAMBLE_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0							
R/W							
0h							

Table 14-14820. EMIF_CTLCFG_DENALI_PHY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CLK_BYPASS_OVERRIDE_0	R/W	0h	Bypass mode override setting for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_BYPASS_TWO_CYC_PREAMBLE_0	R/W	0h	Two_cycle_preamble for bypass mode for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0	R/W	0h	Read DQS bypass mode target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.822 EMIF_CTLCFG_DENALI_PHY_3 Register

1 EMIF_CTLCFG_DENALI_PHY_3 Register (Offset = 400Ch) [reset = 0h]

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Table 14-14821. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C00Ch**

Figure 14-4901. EMIF_CTLCFG_DENALI_PHY_3 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ2_SHIFT_0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ1_SHIFT_0					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ0_SHIFT_0					
NONE		R/W					
0h		0h					

Table 14-14823. EMIF_CTLCFG_DENALI_PHY_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ3_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ2_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ1_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-14823. EMIF_CTLCFG_DENALI_PHY_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ0_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.823 EMIF_CTLCFG_DENALI_PHY_4 Register

1 EMIF_CTLCFG_DENALI_PHY_4 Register (Offset = 4010h) [reset = 0h]

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Table 14-14824. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C010h

Figure 14-4902. EMIF_CTLCFG_DENALI_PHY_4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_SW_WRDQ7_SHIFT_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_SW_WRDQ6_SHIFT_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_SW_WRDQ5_SHIFT_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_SW_WRDQ4_SHIFT_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-14826. EMIF_CTLCFG_DENALI_PHY_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ7_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ6_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ5_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-14826. EMIF_CTLCFG_DENALI_PHY_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ4_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.824 EMIF_CTLCFG_DENALI_PHY_5 Register

1 EMIF_CTLCFG_DENALI_PHY_5 Register (Offset = 4014h) [reset = 0h]

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Table 14-14827. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C014h**

Figure 14-4903. EMIF_CTLCFG_DENALI_PHY_5 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_LP4_BOOT_RDDATA_EN_DLY_0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED						PHY_LP4_BOOT_RDDATA_EN_IE_DLY_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_WRDQS_SHIFT_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDM_SHIFT_0					
NONE		R/W					
0h		0h					

Table 14-14829. EMIF_CTLCFG_DENALI_PHY_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SW_WRDQS_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bit [3] is the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-14829. EMIF_CTLCFG_DENALI_PHY_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDM_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.825 EMIF_CTLCFG_DENALI_PHY_6 Register

1 EMIF_CTLCFG_DENALI_PHY_6 Register (Offset = 4018h) [reset = 0h]

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Table 14-14830. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C018h**

Figure 14-4904. EMIF_CTLCFG_DENALI_PHY_6 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED			PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_0				
NONE			R/W				
0h			0h				

Table 14-14832. EMIF_CTLCFG_DENALI_PHY_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_0	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 0. Bit [0]: disable pull in wrdata_en; Bit [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_LP4_BOOT_RPTR_UPDATE_0	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.826 EMIF_CTLCFG_DENALI_PHY_7 Register

1 EMIF_CTLCFG_DENALI_PHY_7 Register (Offset = 401Ch) [reset = 0h]

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Table 14-14833. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C01Ch**

Figure 14-4905. EMIF_CTLCFG_DENALI_PHY_7 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_CONTROL_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_LPBK_CONTROL_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_CTRL_LPBK_EN_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_LP4_BOOT_RDDATA_EN_OE_DLY_0				
NONE			R/W				
0h			0h				

Table 14-14835. EMIF_CTLCFG_DENALI_PHY_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_LPBK_CONTROL_0	R/W	0h	Loopback control bits for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_CTRL_LPBK_EN_0	R/W	0h	Loopback control en for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.827 EMIF_CTLCFG_DENALI_PHY_8 Register

1 EMIF_CTLCFG_DENALI_PHY_8 Register (Offset = 4020h) [reset = 0h]

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Table 14-14836. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C020h**

Figure 14-4906. EMIF_CTLCFG_DENALI_PHY_8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_GATE_DELAY_COMP_DISABLE_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_LPBK_DFX_TIMEOUT_EN_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14838. EMIF_CTLCFG_DENALI_PHY_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_GATE_DELAY_COMP_DISABLE_0	R/W	0h	use the control whether to compensate half_cycle when gate_target_delay is larger than half_cycle for the gate close for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPBK_DFX_TIMEOUT_EN_0	R/W	0h	Loopback read only test timeout mechanism enable for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.828 EMIF_CTLCFG_DENALI_PHY_9 Register

1 EMIF_CTLCFG_DENALI_PHY_9 Register (Offset = 4024h) [reset = 0h]

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Table 14-14839. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C024h**

Figure 14-4907. EMIF_CTLCFG_DENALI_PHY_9 Name Register

31	30	29	28	27	26	25	24
PHY_AUTO_TIMING_MARGIN_CONTROL_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_AUTO_TIMING_MARGIN_CONTROL_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_AUTO_TIMING_MARGIN_CONTROL_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_AUTO_TIMING_MARGIN_CONTROL_0							
R/W							
0h							

Table 14-14841. EMIF_CTLCFG_DENALI_PHY_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_AUTO_TIMING_MARGIN_CONTROL_0	R/W	0h	Auto timing marging control bits for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.829 EMIF_CTLCFG_DENALI_PHY_10 Register

1 EMIF_CTLCFG_DENALI_PHY_10 Register (Offset = 4028h) [reset = 0h]

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Table 14-14842. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C028h**

Figure 14-4908. EMIF_CTLCFG_DENALI_PHY_10 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_0			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_AUTO_TIMING_MARGIN_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_AUTO_TIMING_MARGIN_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_AUTO_TIMING_MARGIN_OBS_0							
R							
0h							

Table 14-14844. EMIF_CTLCFG_DENALI_PHY_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_AUTO_TIMING_MARGIN_OBS_0	R	0h	Observation register for the auto_timing_margin for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.830 EMIF_CTLCFG_DENALI_PHY_11 Register

1 EMIF_CTLCFG_DENALI_PHY_11 Register (Offset = 402Ch) [reset = 1000000h]

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Table 14-14845. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C02Ch

Figure 14-4909. EMIF_CTLCFG_DENALI_PHY_11 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_PRBS_PATTERN_START_0						
NONE	R/W						
0h	1h						
23	22	21	20	19	18	17	16
RESERVED							PHY_PDA_MODE_EN_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_DQ_IDLE_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_DQ_IDLE_0							
R/W							
0h							

Table 14-14847. EMIF_CTLCFG_DENALI_PHY_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_PRBS_PATTERN_START_0	R/W	1h	PRBS7 start pattern for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_PDA_MODE_EN_0	R/W	0h	When set to 1, the invalid DQs will be driven by the dfi_wrdata to make sure the tpda_s and tpda_h's timing is meet for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_DQ_IDLE_0	R/W	0h	When set to 1, the inavlid DQ will be driven to high, when set to 0, the invalid DQ will be driven to low for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.831 EMIF_CTLCFG_DENALI_PHY_12 Register

1 EMIF_CTLCFG_DENALI_PHY_12 Register (Offset = 4030h) [reset = 0h]

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Table 14-14848. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C030h

Figure 14-4910. EMIF_CTLCFG_DENALI_PHY_12 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTI_PATT_RST_DISABLE_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_RDLVL_MULTI_PATT_ENABLE_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							PHY_PRBS_PATTERN_MASK_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_PRBS_PATTERN_MASK_0							
R/W							
0h							

Table 14-14850. EMIF_CTLCFG_DENALI_PHY_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDLVL_MULTI_PATT_RST_DISABLE_0	R/W	0h	Read Leveling read level windows disable reset for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_RDLVL_MULTI_PATT_ENABLE_0	R/W	0h	Read Leveling Multi-pattern enable for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_PRBS_PATTERN_MASK_0	R/W	0h	PRBS7 mask signal for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.832 EMIF_CTLCFG_DENALI_PHY_13 Register

1 EMIF_CTLCFG_DENALI_PHY_13 Register (Offset = 4034h) [reset = 0h]

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Table 14-14851. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C034h**

Figure 14-4911. EMIF_CTLCFG_DENALI_PHY_13 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_VREF_TRAIN_OBS_0						
NONE	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_VREF_INITIAL_STEPSIZE_0					
NONE		R/W					
0h		0h					

Table 14-14853. EMIF_CTLCFG_DENALI_PHY_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0	R/W	0h	Read DQS data clock bypass mode target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_VREF_TRAIN_OBS_0	R	0h	Observation register for best vref value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_VREF_INITIAL_STEPSIZE_0	R/W	0h	Data slice initial VREF training step size for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.833 EMIF_CTLCFG_DENALI_PHY_14 Register

1 EMIF_CTLCFG_DENALI_PHY_14 Register (Offset = 4038h) [reset = 0h]

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Table 14-14854. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C038h**

Figure 14-4912. EMIF_CTLCFG_DENALI_PHY_14 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL1_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_SNAP_OBS_REGS_0
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_0			
NONE				R/W			
0h				0h			

Table 14-14856. EMIF_CTLCFG_DENALI_PHY_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL1_SLAVE_DELAY_0	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_SNAP_OBS_REGS_0	W	0h	Initiates a snapshot of the internal observation registers for slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_GATE_ERROR_DELAY_SELECT_0	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.834 EMIF_CTLCFG_DENALI_PHY_15 Register

1 EMIF_CTLCFG_DENALI_PHY_15 Register (Offset = 403Ch) [reset = 0h]

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Table 14-14857. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C03Ch**

Figure 14-4913. EMIF_CTLCFG_DENALI_PHY_15 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL2_SLAVE_DELAY_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL2_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_MEM_CLASS_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_LPDDR_0
NONE							R/W
0h							0h

Table 14-14859. EMIF_CTLCFG_DENALI_PHY_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL2_SLAVE_DELAY_0	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_MEM_CLASS_0	R/W	0h	Indicates the type of DRAM for slice 0. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPDDR_0	R/W	0h	Adds a cycle of delay for the slice 0 to match the address slice. Set to 1 to add a cycle Reset Source: ctl_amod_g_rst_n

14.5.1.2.835 EMIF_CTLCFG_DENALI_PHY_16 Register

1 EMIF_CTLCFG_DENALI_PHY_16 Register (Offset = 4040h) [reset = 0h]

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Table 14-14860. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C040h**

Figure 14-4914. EMIF_CTLCFG_DENALI_PHY_16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ON_FLY_GATE_ADJUST_EN_0	
NONE						R/W	
0h						0h	

Table 14-14862. EMIF_CTLCFG_DENALI_PHY_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ON_FLY_GATE_ADJUST_EN_0	R/W	0h	Control the on-the-fly gate adjustment for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.836 EMIF_CTLCFG_DENALI_PHY_17 Register

1 EMIF_CTLCFG_DENALI_PHY_17 Register (Offset = 4044h) [reset = 0h]

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Table 14-14863. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C044h**

Figure 14-4915. EMIF_CTLCFG_DENALI_PHY_17 Name Register

31	30	29	28	27	26	25	24
PHY_GATE_TRACKING_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_GATE_TRACKING_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_GATE_TRACKING_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_0							
R							
0h							

Table 14-14865. EMIF_CTLCFG_DENALI_PHY_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_GATE_TRACKING_OBS_0	R	0h	Report the on-the-fly gate measurement result for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.837 EMIF_CTLCFG_DENALI_PHY_18 Register

1 EMIF_CTLCFG_DENALI_PHY_18 Register (Offset = 4048h) [reset = 0h]

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Table 14-14866. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C048h

Figure 14-4916. EMIF_CTLCFG_DENALI_PHY_18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_LP4_PST_AMBLE_0	
NONE						R/W	
0h						0h	

Table 14-14868. EMIF_CTLCFG_DENALI_PHY_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_LP4_PST_AMBLE_0	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.838 EMIF_CTLCFG_DENALI_PHY_19 Register

1 EMIF_CTLCFG_DENALI_PHY_19 Register (Offset = 404Ch) [reset = 0h]

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Table 14-14869. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C04Ch**

Figure 14-4917. EMIF_CTLCFG_DENALI_PHY_19 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT8_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT8_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT8_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_0							
R/W							
0h							

Table 14-14871. EMIF_CTLCFG_DENALI_PHY_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT8_0	R/W	0h	Read leveling pattern 8 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.839 EMIF_CTLCFG_DENALI_PHY_20 Register

1 EMIF_CTLCFG_DENALI_PHY_20 Register (Offset = 4050h) [reset = 0h]

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Table 14-14872. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C050h**

Figure 14-4918. EMIF_CTLCFG_DENALI_PHY_20 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT9_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT9_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT9_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_0							
R/W							
0h							

Table 14-14874. EMIF_CTLCFG_DENALI_PHY_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT9_0	R/W	0h	Read leveling pattern 9 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.840 EMIF_CTLCFG_DENALI_PHY_21 Register

1 EMIF_CTLCFG_DENALI_PHY_21 Register (Offset = 4054h) [reset = 0h]

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Table 14-14875. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C054h**

Figure 14-4919. EMIF_CTLCFG_DENALI_PHY_21 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT10_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT10_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT10_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT10_0							
R/W							
0h							

Table 14-14877. EMIF_CTLCFG_DENALI_PHY_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT10_0	R/W	0h	Read leveling pattern 10 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.841 EMIF_CTLCFG_DENALI_PHY_22 Register

1 EMIF_CTLCFG_DENALI_PHY_22 Register (Offset = 4058h) [reset = 0h]

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Table 14-14878. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C058h**

Figure 14-4920. EMIF_CTLCFG_DENALI_PHY_22 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT11_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT11_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT11_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_0							
R/W							
0h							

Table 14-14880. EMIF_CTLCFG_DENALI_PHY_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT11_0	R/W	0h	Read leveling pattern 11 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.842 EMIF_CTLCFG_DENALI_PHY_23 Register

1 EMIF_CTLCFG_DENALI_PHY_23 Register (Offset = 405Ch) [reset = 0h]

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Table 14-14881. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C05Ch**

Figure 14-4921. EMIF_CTLCFG_DENALI_PHY_23 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT12_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT12_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT12_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_0							
R/W							
0h							

Table 14-14883. EMIF_CTLCFG_DENALI_PHY_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT12_0	R/W	0h	Read leveling pattern 12 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.843 EMIF_CTLCFG_DENALI_PHY_24 Register

1 EMIF_CTLCFG_DENALI_PHY_24 Register (Offset = 4060h) [reset = 0h]

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Table 14-14884. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C060h**

Figure 14-4922. EMIF_CTLCFG_DENALI_PHY_24 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT13_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT13_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT13_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT13_0							
R/W							
0h							

Table 14-14886. EMIF_CTLCFG_DENALI_PHY_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT13_0	R/W	0h	Read leveling pattern 13 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.844 EMIF_CTLCFG_DENALI_PHY_25 Register

1 EMIF_CTLCFG_DENALI_PHY_25 Register (Offset = 4064h) [reset = 0h]

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Table 14-14887. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C064h**

Figure 14-4923. EMIF_CTLCFG_DENALI_PHY_25 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT14_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT14_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT14_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_0							
R/W							
0h							

Table 14-14889. EMIF_CTLCFG_DENALI_PHY_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT14_0	R/W	0h	Read leveling pattern 14 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.845 EMIF_CTLCFG_DENALI_PHY_26 Register

1 EMIF_CTLCFG_DENALI_PHY_26 Register (Offset = 4068h) [reset = 0h]

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Table 14-14890. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C068h**

Figure 14-4924. EMIF_CTLCFG_DENALI_PHY_26 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT15_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT15_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT15_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_0							
R/W							
0h							

Table 14-14892. EMIF_CTLCFG_DENALI_PHY_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT15_0	R/W	0h	Read leveling pattern 15 data for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.846 EMIF_CTLCFG_DENALI_PHY_27 Register

1 EMIF_CTLCFG_DENALI_PHY_27 Register (Offset = 406Ch) [reset = 0h]

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Table 14-14893. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C06Ch

Figure 14-4925. EMIF_CTLCFG_DENALI_PHY_27 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED				PHY_MASTER_DLY_LOCK_OBS_SELECT_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_0		
NONE					R/W		
0h					0h		

Table 14-14895. EMIF_CTLCFG_DENALI_PHY_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_RDDQ_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal read DQ target delay encoded settings to the accessible read DQ encoded target delay observation register for slice 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_MASTER_DLY_LOCK_OBS_SELECT_0	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_SW_FIFO_PTR_RST_DISABLE_0	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 0. Set to 1 to disable automatic resets. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_SLAVE_LOOP_CNT_UPDATE_0	R/W	0h	Reserved for future use for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.847 EMIF_CTLCFG_DENALI_PHY_28 Register

1 EMIF_CTLCFG_DENALI_PHY_28 Register (Offset = 4070h) [reset = 0h]

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Table 14-14896. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C070h

Figure 14-4926. EMIF_CTLCFG_DENALI_PHY_28 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WR_SHIFT_OBS_SELECT_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WR_ENC_OBS_SELECT_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_0			
NONE				R/W			
0h				0h			

Table 14-14898. EMIF_CTLCFG_DENALI_PHY_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_FIFO_PTR_OBS_SELECT_0	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WR_SHIFT_OBS_SELECT_0	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WR_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal write DQ target delay encoded settings to the accessible write DQ encoded target delay observation register for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_DQ_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal read DQS DQ rise/fall target delay encoded settings to the accessible read DQS DQ rise/fall encoded target delay observation registers for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.848 EMIF_CTLCFG_DENALI_PHY_29 Register

1 EMIF_CTLCFG_DENALI_PHY_29 Register (Offset = 4074h) [reset = 0h]

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Table 14-14899. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C074h**

Figure 14-4927. EMIF_CTLCFG_DENALI_PHY_29 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_WRLVL_CAPTURE_CNT_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_WRLVL_ALGO_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_LVL_DEBUG_CONT_0
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_LVL_DEBUG_MODE_0
NONE							R/W
0h							0h

Table 14-14901. EMIF_CTLCFG_DENALI_PHY_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_WRLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS target delay setting during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_WRLVL_ALGO_0	R/W	0h	Write leveling algorithm selection for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_LVL_DEBUG_CONT_0	W	0h	Allows the leveling state machine to advance [when in debug mode] for slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LVL_DEBUG_MODE_0	R/W	0h	Enables leveling debug mode for slice 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.849 EMIF_CTLCFG_DENALI_PHY_30 Register

1 EMIF_CTLCFG_DENALI_PHY_30 Register (Offset = 4078h) [reset = 0h]

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Table 14-14902. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C078h**

Figure 14-4928. EMIF_CTLCFG_DENALI_PHY_30 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_CAPTURE_CNT_0					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
PHY_DQ_MASK_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_0			
NONE				R/W			
0h				0h			

Table 14-14904. EMIF_CTLCFG_DENALI_PHY_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_GTLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles + 4 to wait after changing DQS target delay setting during gate training for slice 0. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_GTLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS target delay setting during gate training for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_MASK_0	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_WRLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing DQS target delay setting during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.850 EMIF_CTLCFG_DENALI_PHY_31 Register

1 EMIF_CTLCFG_DENALI_PHY_31 Register (Offset = 407Ch) [reset = 0h]

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Table 14-14905. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C07Ch**

Figure 14-4929. EMIF_CTLCFG_DENALI_PHY_31 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_RDLVL_RDDQS_DQ_OBS_SELECT_0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDLVL_OP_MODE_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_RDLVL_UPDT_WAIT_CNT_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_RDLVL_CAPTURE_CNT_0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-14907. EMIF_CTLCFG_DENALI_PHY_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_0	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_RDLVL_OP_MODE_0	R/W	0h	Read leveling algorithm select for slice 0. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing DQS target delay setting during read leveling for slice 0. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_RDLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS target delay setting during read leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.851 EMIF_CTLCFG_DENALI_PHY_32 Register

1 EMIF_CTLCFG_DENALI_PHY_32 Register (Offset = 4080h) [reset = 0h]

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Table 14-14908. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C080h**

Figure 14-4930. EMIF_CTLCFG_DENALI_PHY_32 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_DATA_SWIZZLE_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDLVL_DATA_SWIZZLE_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_DATA_SWIZZLE_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_DATA_MASK_0							
R/W							
0h							

Table 14-14910. EMIF_CTLCFG_DENALI_PHY_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:8	PHY_RDLVL_DATA_SWIZZLE_0	R/W	0h	Read level bit swizzling for DDR4 operation for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDLVL_DATA_MASK_0	R/W	0h	Per-bit mask for read leveling for slice 0. If all bits are not used, only 1 bit should be cleared to 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.852 EMIF_CTLCFG_DENALI_PHY_33 Register

1 EMIF_CTLCFG_DENALI_PHY_33 Register (Offset = 4084h) [reset = 0h]

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Table 14-14911. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C084h

Figure 14-4931. EMIF_CTLCFG_DENALI_PHY_33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_PATT_0		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED		PHY_WDQLVL_BURST_CNT_0					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
PHY_WDQLVL_CLK_JITTER_TOLERANCE_0							
R/W							
0h							

Table 14-14913. EMIF_CTLCFG_DENALI_PHY_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WDQLVL_PATT_0	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 0. Bit [0] corresponds to the LFSR data training pattern. Bit [1] corresponds to the CLK data training pattern. Bit [2] corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_WDQLVL_BURST_CNT_0	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_CLK_JITTER_TOLERANCE_0	R/W	0h	Defines the minimum gap requirment for the LE and TE window for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.853 EMIF_CTLCFG_DENALI_PHY_34 Register

1 EMIF_CTLCFG_DENALI_PHY_34 Register (Offset = 4088h) [reset = 0h]

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Table 14-14914. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C088h**

Figure 14-4932. EMIF_CTLCFG_DENALI_PHY_34 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0							
R/W							
0h							

Table 14-14916. EMIF_CTLCFG_DENALI_PHY_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WDQLVL_DQDM_OBS_SELECT_0	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing the DQ target delay setting during write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0	R/W	0h	Defines the target delay jump value when the TE window is found and begin to serch TE window for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.854 EMIF_CTLCFG_DENALI_PHY_35 Register

1 EMIF_CTLCFG_DENALI_PHY_35 Register (Offset = 408Ch) [reset = 0h]

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Table 14-14917. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C08Ch**

Figure 14-4933. EMIF_CTLCFG_DENALI_PHY_35 Name Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_WDQLVL_CLR_PREV_RESULTS_0
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				PHY_WDQLVL_DM_DLY_STEP_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_WDQLVL_DQ_SLV_DELTA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_SELECT_0							
R/W							
0h							

Table 14-14919. EMIF_CTLCFG_DENALI_PHY_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SC_PHY_WDQLVL_CLR_PREV_RESULTS_0	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_DM_DLY_STEP_0	R/W	0h	The target delay line step for DM training for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_WDQLVL_DQ_SLV_DELTA_0	R/W	0h	The margin for DQ0-7's LE and TE dealy to make sure the DQ bits can work during DM training for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_PERIODIC_OBS_SELECT_0	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.855 EMIF_CTLCFG_DENALI_PHY_36 Register

1 EMIF_CTLCFG_DENALI_PHY_36 Register (Offset = 4090h) [reset = 0h]

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Table 14-14920. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C090h**

Figure 14-4934. EMIF_CTLCFG_DENALI_PHY_36 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_WDQLVL_DATADM_MASK_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_WDQLVL_DATADM_MASK_0							
R/W							
0h							

Table 14-14922. EMIF_CTLCFG_DENALI_PHY_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_WDQLVL_DATADM_MASK_0	R/W	0h	Per-bit mask for write data leveling for slice 0. Set to 1 to mask any bit from the leveling process. Reset Source: ctl_amod_g_rst_n

14.5.1.2.856 EMIF_CTLCFG_DENALI_PHY_37 Register

1 EMIF_CTLCFG_DENALI_PHY_37 Register (Offset = 4094h) [reset = 0h]

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Table 14-14923. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C094h**

Figure 14-4935. EMIF_CTLCFG_DENALI_PHY_37 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT0_0							
R/W							
0h							

Table 14-14925. EMIF_CTLCFG_DENALI_PHY_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT0_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 3 to 0 written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.857 EMIF_CTLCFG_DENALI_PHY_38 Register

1 EMIF_CTLCFG_DENALI_PHY_38 Register (Offset = 4098h) [reset = 0h]

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Table 14-14926. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C098h**

Figure 14-4936. EMIF_CTLCFG_DENALI_PHY_38 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT1_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT1_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT1_0							
R/W							
0h							

Table 14-14928. EMIF_CTLCFG_DENALI_PHY_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT1_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 7 to 4 written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.858 EMIF_CTLCFG_DENALI_PHY_39 Register

1 EMIF_CTLCFG_DENALI_PHY_39 Register (Offset = 409Ch) [reset = 0h]

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Table 14-14929. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C09Ch**

Figure 14-4937. EMIF_CTLCFG_DENALI_PHY_39 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT2_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT2_0							
R/W							
0h							

Table 14-14931. EMIF_CTLCFG_DENALI_PHY_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT2_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 11 to 8 written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.859 EMIF_CTLCFG_DENALI_PHY_40 Register

1 EMIF_CTLCFG_DENALI_PHY_40 Register (Offset = 40A0h) [reset = 0h]

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Table 14-14932. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0A0h**

Figure 14-4938. EMIF_CTLCFG_DENALI_PHY_40 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT3_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT3_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT3_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT3_0							
R/W							
0h							

Table 14-14934. EMIF_CTLCFG_DENALI_PHY_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT3_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 15 to 12 written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.860 EMIF_CTLCFG_DENALI_PHY_41 Register

1 EMIF_CTLCFG_DENALI_PHY_41 Register (Offset = 40A4h) [reset = 0h]

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Table 14-14935. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C0A4h

Figure 14-4939. EMIF_CTLCFG_DENALI_PHY_41 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_MULT_TRAIN_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PHY_USER_PATT4_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT4_0							
R/W							
0h							

Table 14-14937. EMIF_CTLCFG_DENALI_PHY_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_MULT_TRAIN_0	R/W	0h	Control for single pass only No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n
15:0	PHY_USER_PATT4_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the DM bit for the 15 to 0 DQ written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.861 EMIF_CTLCFG_DENALI_PHY_42 Register

1 EMIF_CTLCFG_DENALI_PHY_42 Register (Offset = 40A8h) [reset = 0h]

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Table 14-14938. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C0A8h

Figure 14-4940. EMIF_CTLCFG_DENALI_PHY_42 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_NTP_PERIOD_THRESHOLD_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_NTP_PERIOD_THRESHOLD_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_NTP_EARLY_THRESHOLD_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_NTP_EARLY_THRESHOLD_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14940. EMIF_CTLCFG_DENALI_PHY_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_0	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_EARLY_THRESHOLD_0	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.862 EMIF_CTLCFG_DENALI_PHY_43 Register

1 EMIF_CTLCFG_DENALI_PHY_43 Register (Offset = 40ACh) [reset = 0h]

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Table 14-14941. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0ACh**

Figure 14-4941. EMIF_CTLCFG_DENALI_PHY_43 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_NTP_PERIOD_THRESHOLD_MAX_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_NTP_PERIOD_THRESHOLD_MIN_0							
R/W							
0h							

Table 14-14943. EMIF_CTLCFG_DENALI_PHY_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_MAX_0	R/W	0h	Maximum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_PERIOD_THRESHOLD_MIN_0	R/W	0h	Minimum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.863 EMIF_CTLCFG_DENALI_PHY_44 Register

1 EMIF_CTLCFG_DENALI_PHY_44 Register (Offset = 40B0h) [reset = 0h]

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Table 14-14944. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0B0h**

Figure 14-4942. EMIF_CTLCFG_DENALI_PHY_44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_FIFO_PTR_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_MANUAL_CLEAR_0					
NONE		W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_0
NONE							R/W
0h							0h

Table 14-14946. EMIF_CTLCFG_DENALI_PHY_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_FIFO_PTR_OBS_0	R	0h	Observation register containing read entry FIFO pointers for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	SC_PHY_MANUAL_CLEAR_0	W	0h	Manual reset/clear of internal logic for slice 0. Bit [0] initiates manual setup of the read DQS gate. Bit [1] is reset of read entry FIFO pointers. Bit [2] is reset of controller delay min/max lock values. Bit [3] is manual reset of controller delay unlock counter. Bit [4] is reset of leveling error bit in the leveling status registers. Bit [5] is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_CALVL_VREF_DRIVING_SLICE_0	R/W	0h	Indicates if slice 0 is used to drive the VREF value to the device during CA training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.864 EMIF_CTLCFG_DENALI_PHY_45 Register

1 EMIF_CTLCFG_DENALI_PHY_45 Register (Offset = 40B4h) [reset = 100000h]

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Table 14-14947. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C0B4h

Figure 14-4943. EMIF_CTLCFG_DENALI_PHY_45 Name Register

31	30	29	28	27	26	25	24
PHY_LPBK_RESULT_OBS_0							
R							
100000h							
23	22	21	20	19	18	17	16
PHY_LPBK_RESULT_OBS_0							
R							
100000h							
15	14	13	12	11	10	9	8
PHY_LPBK_RESULT_OBS_0							
R							
100000h							
7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_0							
R							
100000h							

Table 14-14949. EMIF_CTLCFG_DENALI_PHY_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_LPBK_RESULT_OBS_0	R	100000h	Observation register containing loopback status/results for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.865 EMIF_CTLCFG_DENALI_PHY_46 Register

1 EMIF_CTLCFG_DENALI_PHY_46 Register (Offset = 40B8h) [reset = 0h]

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Table 14-14950. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0B8h**

Figure 14-4944. EMIF_CTLCFG_DENALI_PHY_46 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MASTER_DLY_LOCK_OBS_0		
NONE					R		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MASTER_DLY_LOCK_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_LPBK_ERROR_COUNT_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_LPBK_ERROR_COUNT_OBS_0							
R							
0h							

Table 14-14952. EMIF_CTLCFG_DENALI_PHY_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_MASTER_DLY_LOCK_OBS_0	R	0h	Observation register containing controller delay results for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_LPBK_ERROR_COUNT_OBS_0	R	0h	Observation register containing total number of loopback error data for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.866 EMIF_CTLCFG_DENALI_PHY_47 Register

1 EMIF_CTLCFG_DENALI_PHY_47 Register (Offset = 40BCh) [reset = 0h]

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Table 14-14953. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0BCh**

Figure 14-4945. EMIF_CTLCFG_DENALI_PHY_47 Name Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MEAS_DLY_STEP_VALUE_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_0						
NONE	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_0						
NONE	R						
0h	0h						

Table 14-14955. EMIF_CTLCFG_DENALI_PHY_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS DQ rising edge adder target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	PHY_MEAS_DLY_STEP_VALUE_0	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with demominator of 512, for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS base target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_RDDQ_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQ target delay encoded values for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.867 EMIF_CTLCFG_DENALI_PHY_48 Register

1 EMIF_CTLCFG_DENALI_PHY_48 Register (Offset = 40C0h) [reset = 0h]

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Table 14-14956. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0C0h**

Figure 14-4946. EMIF_CTLCFG_DENALI_PHY_48 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_0						
NONE	R						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED					PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0		
NONE					R		
0h					0h		

15	14	13	12	11	10	9	8
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0							
R							
0h							

7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_0							
R							
0h							

Table 14-14958. EMIF_CTLCFG_DENALI_PHY_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write DQS base target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS gate target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS DQ falling edge adder target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.868 EMIF_CTLCFG_DENALI_PHY_49 Register

1 EMIF_CTLCFG_DENALI_PHY_49 Register (Offset = 40C4h) [reset = 0h]

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Table 14-14959. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0C4h**

Figure 14-4947. EMIF_CTLCFG_DENALI_PHY_49 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_WR_SHIFT_OBS_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_WR_ADDER_SLV_DLY_ENC_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14961. EMIF_CTLCFG_DENALI_PHY_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WR_SHIFT_OBS_0	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write adder target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write DQ base target delay encoded value for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.869 EMIF_CTLCFG_DENALI_PHY_50 Register

1 EMIF_CTLCFG_DENALI_PHY_50 Register (Offset = 40C8h) [reset = 0h]

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Table 14-14962. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0C8h**

Figure 14-4948. EMIF_CTLCFG_DENALI_PHY_50 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_0	
NONE						R	
0h						0h	
23	22	21	20	19	18	17	16
PHY_WRLVL_HARD1_DELAY_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_0	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_HARD0_DELAY_OBS_0							
R							
0h							

Table 14-14964. EMIF_CTLCFG_DENALI_PHY_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_HARD1_DELAY_OBS_0	R	0h	Observation register containing write leveling first hard 1 DQS target delay for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_HARD0_DELAY_OBS_0	R	0h	Observation register containing write leveling last hard 0 DQS target delay for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.870 EMIF_CTLCFG_DENALI_PHY_51 Register

1 EMIF_CTLCFG_DENALI_PHY_51 Register (Offset = 40CCh) [reset = 0h]

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Table 14-14965. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0CCh**

Figure 14-4949. EMIF_CTLCFG_DENALI_PHY_51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_WRLVL_STATUS_OBS_0				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
PHY_WRLVL_STATUS_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WRLVL_STATUS_OBS_0							
R							
0h							

Table 14-14967. EMIF_CTLCFG_DENALI_PHY_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PHY_WRLVL_STATUS_OBS_0	R	0h	Observation register containing write leveling status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.871 EMIF_CTLCFG_DENALI_PHY_52 Register

1 EMIF_CTLCFG_DENALI_PHY_52 Register (Offset = 40D0h) [reset = 0h]

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Table 14-14968. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0D0h**

Figure 14-4950. EMIF_CTLCFG_DENALI_PHY_52 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0							
R							
0h							

Table 14-14970. EMIF_CTLCFG_DENALI_PHY_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing gate sample2 target delay encoded values for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing gate sample1 target delay encoded values for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.872 EMIF_CTLCFG_DENALI_PHY_53 Register

1 EMIF_CTLCFG_DENALI_PHY_53 Register (Offset = 40D4h) [reset = 0h]

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Table 14-14971. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0D4h**

Figure 14-4951. EMIF_CTLCFG_DENALI_PHY_53 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_0					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GTLVL_HARD1_DELAY_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_0					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_HARD0_DELAY_OBS_0							
R							
0h							

Table 14-14973. EMIF_CTLCFG_DENALI_PHY_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	PHY_GTLVL_HARD1_DELAY_OBS_0	R	0h	Observation register containing gate training last hard 1 DQS target delay for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	PHY_GTLVL_HARD0_DELAY_OBS_0	R	0h	Observation register containing gate training first hard 0 DQS target delay for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.873 *EMIF_CTLCFG_DENALI_PHY_54 Register*

1 EMIF_CTLCFG_DENALI_PHY_54 Register (Offset = 40D8h) [reset = 0h]

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Table 14-14974. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0D8h**

Figure 14-4952. EMIF_CTLCFG_DENALI_PHY_54 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_GTLVL_STATUS_OBS_0	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
PHY_GTLVL_STATUS_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GTLVL_STATUS_OBS_0							
R							
0h							

Table 14-14976. EMIF_CTLCFG_DENALI_PHY_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_GTLVL_STATUS_OBS_0	R	0h	Observation register containing gate training status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.874 EMIF_CTLCFG_DENALI_PHY_55 Register

1 EMIF_CTLCFG_DENALI_PHY_55 Register (Offset = 40DCh) [reset = 0h]

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Table 14-14977. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0DCh**

Figure 14-4953. EMIF_CTLCFG_DENALI_PHY_55 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14979. EMIF_CTLCFG_DENALI_PHY_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0	R	0h	Observation register containing read leveling data window trailing edge target delay setting for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0	R	0h	Observation register containing read leveling data window leading edge target delay setting for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.875 EMIF_CTLCFG_DENALI_PHY_56 Register

1 EMIF_CTLCFG_DENALI_PHY_56 Register (Offset = 40E0h) [reset = 0h]

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Table 14-14980. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C0E0h

Figure 14-4954. EMIF_CTLCFG_DENALI_PHY_56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_0	
NONE						R	
0h						0h	

Table 14-14982. EMIF_CTLCFG_DENALI_PHY_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_0	R	0h	Observation register containing read leveling number of windows found for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.876 EMIF_CTLCFG_DENALI_PHY_57 Register

1 EMIF_CTLCFG_DENALI_PHY_57 Register (Offset = 40E4h) [reset = 0h]

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Table 14-14983. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0E4h**

Figure 14-4955. EMIF_CTLCFG_DENALI_PHY_57 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_STATUS_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_STATUS_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_STATUS_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_0							
R							
0h							

Table 14-14985. EMIF_CTLCFG_DENALI_PHY_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_STATUS_OBS_0	R	0h	Observation register containing read leveling status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.877 EMIF_CTLCFG_DENALI_PHY_58 Register

1 EMIF_CTLCFG_DENALI_PHY_58 Register (Offset = 40E8h) [reset = 7FF0000h]

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Table 14-14986. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0E8h**

Figure 14-4956. EMIF_CTLCFG_DENALI_PHY_58 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_0		
NONE					R		
0h					7FFh		

23	22	21	20	19	18	17	16
PHY_WDQLVL_DQDM_TE_DLY_OBS_0							
R							
7FFh							

15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_0		
NONE					R		
0h					0h		

7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_LE_DLY_OBS_0							
R							
0h							

Table 14-14988. EMIF_CTLCFG_DENALI_PHY_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_WDQLVL_DQDM_TE_DLY_OBS_0	R	7FFh	Observation register containing write data leveling data window trailing edge target delay setting for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_LE_DLY_OBS_0	R	0h	Observation register containing write data leveling data window leading edge target delay setting for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.878 EMIF_CTLCFG_DENALI_PHY_59 Register

1 EMIF_CTLCFG_DENALI_PHY_59 Register (Offset = 40ECh) [reset = 0h]

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Table 14-14989. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0ECh**

Figure 14-4957. EMIF_CTLCFG_DENALI_PHY_59 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_STATUS_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_STATUS_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_STATUS_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_0							
R							
0h							

Table 14-14991. EMIF_CTLCFG_DENALI_PHY_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_STATUS_OBS_0	R	0h	Observation register containing write data leveling status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.879 EMIF_CTLCFG_DENALI_PHY_60 Register

1 EMIF_CTLCFG_DENALI_PHY_60 Register (Offset = 40F0h) [reset = 0h]

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Table 14-14992. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0F0h**

Figure 14-4958. EMIF_CTLCFG_DENALI_PHY_60 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_PERIODIC_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_PERIODIC_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_PERIODIC_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_0							
R							
0h							

Table 14-14994. EMIF_CTLCFG_DENALI_PHY_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_PERIODIC_OBS_0	R	0h	Observation register containing periodic write data leveling status for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.880 EMIF_CTLCFG_DENALI_PHY_61 Register

1 EMIF_CTLCFG_DENALI_PHY_61 Register (Offset = 40F4h) [reset = 0h]

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Table 14-14995. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0F4h**

Figure 14-4959. EMIF_CTLCFG_DENALI_PHY_61 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_DDL_MODE_0						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_MODE_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DDL_MODE_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_MODE_0							
R/W							
0h							

Table 14-14997. EMIF_CTLCFG_DENALI_PHY_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	PHY_DDL_MODE_0	R/W	0h	DDL mode for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.881 EMIF_CTLCFG_DENALI_PHY_62 Register

1 EMIF_CTLCFG_DENALI_PHY_62 Register (Offset = 40F8h) [reset = 0h]

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Table 14-14998. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C0F8h

Figure 14-4960. EMIF_CTLCFG_DENALI_PHY_62 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DDL_MASK_0					
NONE		R/W					
0h		0h					

Table 14-15000. EMIF_CTLCFG_DENALI_PHY_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DDL_MASK_0	R/W	0h	DDL mask for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.882 EMIF_CTLCFG_DENALI_PHY_63 Register

1 EMIF_CTLCFG_DENALI_PHY_63 Register (Offset = 40FCh) [reset = 0h]

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Table 14-15001. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C0FCh**

Figure 14-4961. EMIF_CTLCFG_DENALI_PHY_63 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_OBS_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_TEST_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DDL_TEST_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_TEST_OBS_0							
R							
0h							

Table 14-15003. EMIF_CTLCFG_DENALI_PHY_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_OBS_0	R	0h	DDL test observation for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.883 EMIF_CTLCFG_DENALI_PHY_64 Register

1 EMIF_CTLCFG_DENALI_PHY_64 Register (Offset = 4100h) [reset = 0h]

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Table 14-15004. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C100h

Figure 14-4962. EMIF_CTLCFG_DENALI_PHY_64 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							

Table 14-15006. EMIF_CTLCFG_DENALI_PHY_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_MSTR_DLY_OBS_0	R	0h	DDL test observation delays for slice 0 controller DDL. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.884 EMIF_CTLCFG_DENALI_PHY_65 Register

1 EMIF_CTLCFG_DENALI_PHY_65 Register (Offset = 4104h) [reset = 0h]

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Table 14-15007. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C104h**

Figure 14-4963. EMIF_CTLCFG_DENALI_PHY_65 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_LP4_WDQS_OE_EXTEND_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_DDL_TRACK_UPD_THRESHOLD_0							
R/W							
0h							

Table 14-15009. EMIF_CTLCFG_DENALI_PHY_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ0_0	R/W	0h	RX Calibration codes for DQ0 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LP4_WDQS_OE_EXTEND_0	R/W	0h	LPDDR4 write preamble extension enable for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DDL_TRACK_UPD_THRESHOLD_0	R/W	0h	Specify threshold value for PHY init update tracking for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.885 EMIF_CTLCFG_DENALI_PHY_66 Register

1 EMIF_CTLCFG_DENALI_PHY_66 Register (Offset = 4108h) [reset = 0h]

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Table 14-15010. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C108h**

Figure 14-4964. EMIF_CTLCFG_DENALI_PHY_66 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ2_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ1_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ1_0							
R/W							
0h							

Table 14-15012. EMIF_CTLCFG_DENALI_PHY_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ2_0	R/W	0h	RX Calibration codes for DQ2 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ1_0	R/W	0h	RX Calibration codes for DQ1 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.886 EMIF_CTLCFG_DENALI_PHY_67 Register

1 EMIF_CTLCFG_DENALI_PHY_67 Register (Offset = 410Ch) [reset = 0h]

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Table 14-15013. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C10Ch

Figure 14-4965. EMIF_CTLCFG_DENALI_PHY_67 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ4_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ4_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ3_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ3_0							
R/W							
0h							

Table 14-15015. EMIF_CTLCFG_DENALI_PHY_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ4_0	R/W	0h	RX Calibration codes for DQ4 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ3_0	R/W	0h	RX Calibration codes for DQ3 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.887 EMIF_CTLCFG_DENALI_PHY_68 Register

1 EMIF_CTLCFG_DENALI_PHY_68 Register (Offset = 4110h) [reset = 0h]

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Table 14-15016. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C110h**

Figure 14-4966. EMIF_CTLCFG_DENALI_PHY_68 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ6_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ6_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ5_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ5_0							
R/W							
0h							

Table 14-15018. EMIF_CTLCFG_DENALI_PHY_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ6_0	R/W	0h	RX Calibration codes for DQ6 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ5_0	R/W	0h	RX Calibration codes for DQ5 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.888 EMIF_CTLCFG_DENALI_PHY_69 Register

1 EMIF_CTLCFG_DENALI_PHY_69 Register (Offset = 4114h) [reset = 0h]

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Table 14-15019. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C114h**

Figure 14-4967. EMIF_CTLCFG_DENALI_PHY_69 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ7_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ7_0							
R/W							
0h							

Table 14-15021. EMIF_CTLCFG_DENALI_PHY_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ7_0	R/W	0h	RX Calibration codes for DQ7 for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.889 EMIF_CTLCFG_DENALI_PHY_70 Register

1 EMIF_CTLCFG_DENALI_PHY_70 Register (Offset = 4118h) [reset = 0h]

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Table 14-15022. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C118h**

Figure 14-4968. EMIF_CTLCFG_DENALI_PHY_70 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_RX_CAL_DM_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_RX_CAL_DM_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RX_CAL_DM_0							
R/W							
0h							

Table 14-15024. EMIF_CTLCFG_DENALI_PHY_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_RX_CAL_DM_0	R/W	0h	RX Calibration codes for DM for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.890 EMIF_CTLCFG_DENALI_PHY_71 Register

1 EMIF_CTLCFG_DENALI_PHY_71 Register (Offset = 411Ch) [reset = 0h]

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Table 14-15025. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C11Ch

Figure 14-4969. EMIF_CTLCFG_DENALI_PHY_71 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_FDBK_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_FDBK_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQS_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQS_0							
R/W							
0h							

Table 14-15027. EMIF_CTLCFG_DENALI_PHY_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_FDBK_0	R/W	0h	RX Calibration codes for FDBK for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQS_0	R/W	0h	RX Calibration codes for DQS for slice 0. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.891 EMIF_CTLCFG_DENALI_PHY_72 Register

1 EMIF_CTLCFG_DENALI_PHY_72 Register (Offset = 4120h) [reset = 0h]

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Table 14-15028. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C120h**

Figure 14-4970. EMIF_CTLCFG_DENALI_PHY_72 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_FDBK_PWR_CTRL_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_STATIC_TOG_DISABLE_0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_PAD_RX_BIAS_EN_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_RX_BIAS_EN_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15030. EMIF_CTLCFG_DENALI_PHY_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_FDBK_PWR_CTRL_0	R/W	0h	Shutoff gate feedback IO to reduce power for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_STATIC_TOG_DISABLE_0	R/W	0h	Control to disable toggle during static activity for slice 0. bit0: Write path delay line disable; bit1: Read path delay line disable; bit2: Read data path disable; bit3: clk_phy disable; bit4: controller delay line disable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_PAD_RX_BIAS_EN_0	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.892 EMIF_CTLCFG_DENALI_PHY_73 Register

1 EMIF_CTLCFG_DENALI_PHY_73 Register (Offset = 4124h) [reset = 0h]

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Table 14-15031. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C124h**

Figure 14-4971. EMIF_CTLCFG_DENALI_PHY_73 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RDPATH_GATE_DISABLE_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_0
NONE							R/W
0h							0h

Table 14-15033. EMIF_CTLCFG_DENALI_PHY_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_SLICE_PWR_RDC_DISABLE_0	R/W	0h	Data slice power reduction disable for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_0	R/W	0h	Data slice RX_CAL block power reduction disable for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_RDPATH_GATE_DISABLE_0	R/W	0h	Data slice read path power reduction disable for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_SLV_DLY_CTRL_GATE_DISABLE_0	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.893 EMIF_CTLCFG_DENALI_PHY_74 Register

1 EMIF_CTLCFG_DENALI_PHY_74 Register (Offset = 4128h) [reset = 0h]

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Table 14-15034. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C128h

Figure 14-4972. EMIF_CTLCFG_DENALI_PHY_74 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_SELECT_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_SELECT_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_DQ_TSEL_ENABLE_0		
NONE					R/W		
0h					0h		

Table 14-15036. EMIF_CTLCFG_DENALI_PHY_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_DQS_TSEL_ENABLE_0	R/W	0h	Operation type tsel enables for DQS signals for slice 0. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:8	PHY_DQ_TSEL_SELECT_0	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DQ_TSEL_ENABLE_0	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 0. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.894 EMIF_CTLCFG_DENALI_PHY_75 Register

1 EMIF_CTLCFG_DENALI_PHY_75 Register (Offset = 412Ch) [reset = 0h]

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Table 14-15037. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C12Ch**

Figure 14-4973. EMIF_CTLCFG_DENALI_PHY_75 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_VREF_INITIAL_START_POINT_0</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_TWO_CYC_PREAMBLE_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DQS_TSEL_SELECT_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DQS_TSEL_SELECT_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15039. EMIF_CTLCFG_DENALI_PHY_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_VREF_INITIAL_START_POINT_0	R/W	0h	Data slice initial VREF training start value for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_TWO_CYC_PREAMBLE_0	R/W	0h	2 cycle preamble support for slice 0. Bit [0] controls the 2 cycle read preamble. Bit [1] controls the 2 cycle write preamble. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_DQS_TSEL_SELECT_0	R/W	0h	Operation type tsel select values for DQS signals for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.895 EMIF_CTLCFG_DENALI_PHY_76 Register

1 EMIF_CTLCFG_DENALI_PHY_76 Register (Offset = 4130h) [reset = 0h]

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Table 14-15040. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C130h**

Figure 14-4974. EMIF_CTLCFG_DENALI_PHY_76 Name Register

31	30	29	28	27	26	25	24
PHY_NTP_WDQ_STEP_SIZE_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_TRAIN_EN_0
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PHY_VREF_TRAINING_CTRL_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED	PHY_VREF_INITIAL_STOP_POINT_0						
NONE	R/W						
0h	0h						

Table 14-15042. EMIF_CTLCFG_DENALI_PHY_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_NTP_WDQ_STEP_SIZE_0	R/W	0h	Step size of WR DQ target delay during No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_TRAIN_EN_0	R/W	0h	Enable for No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_VREF_TRAINING_CTRL_0	R/W	0h	Data slice vref training enable control for slice 0. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_VREF_INITIAL_STOP_POINT_0	R/W	0h	Data slice initial VREF training stop value for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.896 EMIF_CTLCFG_DENALI_PHY_77 Register

1 EMIF_CTLCFG_DENALI_PHY_77 Register (Offset = 4134h) [reset = 0h]

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Table 14-15043. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C134h**

Figure 14-4975. EMIF_CTLCFG_DENALI_PHY_77 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_NTP_WDQ_STOP_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_NTP_WDQ_STOP_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_NTP_WDQ_START_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_WDQ_START_0							
R/W							
0h							

Table 14-15045. EMIF_CTLCFG_DENALI_PHY_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_NTP_WDQ_STOP_0	R/W	0h	End of WR DQ target delay in No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_NTP_WDQ_START_0	R/W	0h	Starting WR DQ target delay in No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.897 EMIF_CTLCFG_DENALI_PHY_78 Register

1 EMIF_CTLCFG_DENALI_PHY_78 Register (Offset = 4138h) [reset = 0h]

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Table 14-15046. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C138h**

Figure 14-4976. EMIF_CTLCFG_DENALI_PHY_78 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED						PHY_WDQLVL_DVW_MIN_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_WDQLVL_DVW_MIN_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_BIT_EN_0							
R/W							
0h							

Table 14-15048. EMIF_CTLCFG_DENALI_PHY_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_SW_WDQLVL_DVW_MIN_EN_0	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_WDQLVL_DVW_MIN_0	R/W	0h	Minimum data valid window across DQs and ranks for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_NTP_WDQ_BIT_EN_0	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.898 EMIF_CTLCFG_DENALI_PHY_79 Register

1 EMIF_CTLCFG_DENALI_PHY_79 Register (Offset = 413Ch) [reset = 0h]

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Table 14-15049. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C13Ch**

Figure 14-4977. EMIF_CTLCFG_DENALI_PHY_79 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_0_0				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_TX_DCD_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED				PHY_FAST_LVL_EN_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQLVL_PER_START_OFFSET_0					
NONE		R/W					
0h		0h					

Table 14-15051. EMIF_CTLCFG_DENALI_PHY_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_0_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_TX_DCD_0	R/W	0h	Controls TX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_FAST_LVL_EN_0	R/W	0h	Enable for fast multi-pattern window search for slice 0. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WDQLVL_PER_START_OFFSET_0	R/W	0h	Peridic training start point offset for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.899 EMIF_CTLCFG_DENALI_PHY_80 Register

1 EMIF_CTLCFG_DENALI_PHY_80 Register (Offset = 4140h) [reset = 0h]

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Table 14-15052. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C140h

Figure 14-4978. EMIF_CTLCFG_DENALI_PHY_80 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_4_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_RX_DCD_3_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_RX_DCD_2_0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_RX_DCD_1_0				
NONE			R/W				
0h			0h				

Table 14-15054. EMIF_CTLCFG_DENALI_PHY_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_4_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_3_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_2_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_1_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.900 EMIF_CTLCFG_DENALI_PHY_81 Register

1 EMIF_CTLCFG_DENALI_PHY_81 Register (Offset = 4144h) [reset = 0h]

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Table 14-15055. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C144h**

Figure 14-4979. EMIF_CTLCFG_DENALI_PHY_81 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_DM_RX_DCD_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_RX_DCD_7_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_RX_DCD_6_0				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_RX_DCD_5_0				
NONE			R/W				
0h			0h				

Table 14-15057. EMIF_CTLCFG_DENALI_PHY_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_DM_RX_DCD_0	R/W	0h	Controls RX_DCD pin for dm pad for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_7_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_6_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_5_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.901 EMIF_CTLCFG_DENALI_PHY_82 Register

1 EMIF_CTLCFG_DENALI_PHY_82 Register (Offset = 4148h) [reset = 0h]

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Table 14-15058. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C148h

Figure 14-4980. EMIF_CTLCFG_DENALI_PHY_82 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PHY_PAD_DSLICE_IO_CFG_0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_FDBK_RX_DCD_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_DQS_RX_DCD_0				
NONE			R/W				
0h			0h				

Table 14-15060. EMIF_CTLCFG_DENALI_PHY_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PHY_PAD_DSLICE_IO_CFG_0	R/W	0h	Controls PCLK/PARK pin for pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_FDBK_RX_DCD_0	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_DQS_RX_DCD_0	R/W	0h	Controls RX_DCD pin for dqs pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.902 EMIF_CTLCFG_DENALI_PHY_83 Register

1 EMIF_CTLCFG_DENALI_PHY_83 Register (Offset = 414Ch) [reset = 0h]

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Table 14-15061. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C14Ch**

Figure 14-4981. EMIF_CTLCFG_DENALI_PHY_83 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ1_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ1_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ0_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ0_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15063. EMIF_CTLCFG_DENALI_PHY_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ1_SLAVE_DELAY_0	R/W	0h	Read DQ1 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ0_SLAVE_DELAY_0	R/W	0h	Read DQ0 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.903 EMIF_CTLCFG_DENALI_PHY_84 Register

1 EMIF_CTLCFG_DENALI_PHY_84 Register (Offset = 4150h) [reset = 0h]

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Table 14-15064. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C150h**

Figure 14-4982. EMIF_CTLCFG_DENALI_PHY_84 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ3_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ3_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ2_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ2_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15066. EMIF_CTLCFG_DENALI_PHY_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ3_SLAVE_DELAY_0	R/W	0h	Read DQ3 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ2_SLAVE_DELAY_0	R/W	0h	Read DQ2 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.904 EMIF_CTLCFG_DENALI_PHY_85 Register

1 EMIF_CTLCFG_DENALI_PHY_85 Register (Offset = 4154h) [reset = 0h]

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Table 14-15067. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C154h**

Figure 14-4983. EMIF_CTLCFG_DENALI_PHY_85 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ5_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ5_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ4_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ4_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15069. EMIF_CTLCFG_DENALI_PHY_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ5_SLAVE_DELAY_0	R/W	0h	Read DQ5 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ4_SLAVE_DELAY_0	R/W	0h	Read DQ4 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.905 EMIF_CTLCFG_DENALI_PHY_86 Register

1 EMIF_CTLCFG_DENALI_PHY_86 Register (Offset = 4158h) [reset = 0h]

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Table 14-15070. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C158h**

Figure 14-4984. EMIF_CTLCFG_DENALI_PHY_86 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ7_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ7_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ6_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ6_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15072. EMIF_CTLCFG_DENALI_PHY_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ7_SLAVE_DELAY_0	R/W	0h	Read DQ7 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ6_SLAVE_DELAY_0	R/W	0h	Read DQ6 target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.906 EMIF_CTLCFG_DENALI_PHY_87 Register

1 EMIF_CTLCFG_DENALI_PHY_87 Register (Offset = 415Ch) [reset = 0h]

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Table 14-15073. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C15Ch

Figure 14-4985. EMIF_CTLCFG_DENALI_PHY_87 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RX_CAL_ALL_DLY_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_RX_PCLK_CLK_SEL_0		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDM_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDM_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15075. EMIF_CTLCFG_DENALI_PHY_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RX_CAL_ALL_DLY_0	R/W	0h	Defines the number of cycles/half cycles that the rx_cal_all_opad signal should be asserted for. There is a phy_rx_cal_all_dly_X parameter for each of the slices of data sent on the DFI data bus for slice 0. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_RX_PCLK_CLK_SEL_0	R/W	0h	RX_PCLK clock frequency selection for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDM_SLAVE_DELAY_0	R/W	0h	Read DM/DBI target delay setting for slice 0. May be used for data swap. Reset Source: ctl_amod_g_rst_n

14.5.1.2.907 EMIF_CTLCFG_DENALI_PHY_88 Register

1 EMIF_CTLCFG_DENALI_PHY_88 Register (Offset = 4160h) [reset = 0h]

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Table 14-15076. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C160h**

Figure 14-4986. EMIF_CTLCFG_DENALI_PHY_88 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_DQS_OE_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_DQ_TSEL_WR_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DQ_TSEL_RD_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_DQ_OE_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15078. EMIF_CTLCFG_DENALI_PHY_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_OE_TIMING_0	R/W	0h	Start/end timing values for DQS output enable signals for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQ_TSEL_WR_TIMING_0	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_TSEL_RD_TIMING_0	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DQ_OE_TIMING_0	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.908 EMIF_CTLCFG_DENALI_PHY_89 Register

1 EMIF_CTLCFG_DENALI_PHY_89 Register (Offset = 4164h) [reset = 0h]

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Table 14-15079. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C164h**

Figure 14-4987. EMIF_CTLCFG_DENALI_PHY_89 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_DQS_TSEL_WR_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_DQS_OE_RD_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DQS_TSEL_RD_TIMING_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_IO_PAD_DELAY_TIMING_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15081. EMIF_CTLCFG_DENALI_PHY_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_TSEL_WR_TIMING_0	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_OE_RD_TIMING_0	R/W	0h	Start/end timing values for DQS read based OE extension for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQS_TSEL_RD_TIMING_0	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_0	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.909 EMIF_CTLCFG_DENALI_PHY_90 Register

1 EMIF_CTLCFG_DENALI_PHY_90 Register (Offset = 4168h) [reset = 0h]

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Table 14-15082. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C168h**

Figure 14-4988. EMIF_CTLCFG_DENALI_PHY_90 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_VREF_CTRL_DQ_0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_VREF_CTRL_DQ_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_VREF_SETTING_TIME_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_VREF_SETTING_TIME_0							
R/W							
0h							

Table 14-15084. EMIF_CTLCFG_DENALI_PHY_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_PAD_VREF_CTRL_DQ_0	R/W	0h	Pad VREF control settings for DQ slice 0. Reset Source: ctl_amod_g_rst_n
15:0	PHY_VREF_SETTING_TIME_0	R/W	0h	Number of cycles for vref settle after setting is changed for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.910 EMIF_CTLCFG_DENALI_PHY_91 Register

1 EMIF_CTLCFG_DENALI_PHY_91 Register (Offset = 416Ch) [reset = 0h]

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Table 14-15085. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C16Ch**

Figure 14-4989. EMIF_CTLCFG_DENALI_PHY_91 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_IE_MODE_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDATA_EN_IE_DLY_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_DQS_IE_TIMING_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQ_IE_TIMING_0							
R/W							
0h							

Table 14-15087. EMIF_CTLCFG_DENALI_PHY_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_IE_MODE_0	R/W	0h	Input enable mode bits for slice 0. Bit [0] enables the mode where the input enables are always on; set to 1 to enable. Bit [1] disables the input enable on the DM signal; set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_RDDATA_EN_IE_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 0. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQS_IE_TIMING_0	R/W	0h	Start/end timing values for DQS input enable signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DQ_IE_TIMING_0	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.911 EMIF_CTLCFG_DENALI_PHY_92 Register

1 EMIF_CTLCFG_DENALI_PHY_92 Register (Offset = 4170h) [reset = 0h]

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Table 14-15088. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C170h

Figure 14-4990. EMIF_CTLCFG_DENALI_PHY_92 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_WDQLVL_RDDATA_EN_TSEL_DLY_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_WDQLVL_RDDATA_EN_DLY_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_WDQLVL_IE_ON_0
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_DBI_MODE_0	
NONE						R/W	
0h						0h	

Table 14-15090. EMIF_CTLCFG_DENALI_PHY_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_WDQLVL_RDDATA_EN_TSEL_DLY_0	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_WDQLVL_RDDATA_EN_DLY_0	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is early for slice 0. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_WDQLVL_IE_ON_0	R/W	0h	IE control, 1 meams IE is always on during WR DQ training for slice 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_DBI_MODE_0	R/W	0h	DBI mode for slice 0. Bit [0] enables return of DBI read data. Reset Source: ctl_amod_g_rst_n

14.5.1.2.912 EMIF_CTLCFG_DENALI_PHY_93 Register

1 EMIF_CTLCFG_DENALI_PHY_93 Register (Offset = 4174h) [reset = 0h]

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Table 14-15091. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C174h

Figure 14-4991. EMIF_CTLCFG_DENALI_PHY_93 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_SW_MASTER_MODE_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED			PHY_RDDATA_EN_OE_DLY_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_RDDATA_EN_TSEL_DLY_0				
NONE			R/W				
0h			0h				

Table 14-15093. EMIF_CTLCFG_DENALI_PHY_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_SW_MASTER_MODE_0	R/W	0h	Controller delay line override settings for slice 0. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_RDDATA_EN_OE_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_RDDATA_EN_TSEL_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.913 EMIF_CTLCFG_DENALI_PHY_94 Register

1 EMIF_CTLCFG_DENALI_PHY_94 Register (Offset = 4178h) [reset = 0h]

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Table 14-15094. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C178h

Figure 14-4992. EMIF_CTLCFG_DENALI_PHY_94 Name Register

31	30	29	28	27	26	25	24
PHY_MASTER_DELAY_WAIT_0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_MASTER_DELAY_STEP_0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_MASTER_DELAY_START_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_DELAY_START_0							
R/W							
0h							

Table 14-15096. EMIF_CTLCFG_DENALI_PHY_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_MASTER_DELAY_WAIT_0	R/W	0h	Wait cycles for controller delay line locking algorithm for slice 0. Bits [3:0] are the cycle wait count after a calibration clock setting change. Bits [7:4] are the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_MASTER_DELAY_STEP_0	R/W	0h	Incremental step size for controller delay line locking algorithm for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_MASTER_DELAY_START_0	R/W	0h	Start value for controller delay line locking algorithm for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.914 EMIF_CTLCFG_DENALI_PHY_95 Register

1 EMIF_CTLCFG_DENALI_PHY_95 Register (Offset = 417Ch) [reset = 0h]

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Table 14-15097. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C17Ch

Figure 14-4993. EMIF_CTLCFG_DENALI_PHY_95 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WRLVL_DLY_FINE_STEP_0			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PHY_WRLVL_DLY_STEP_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_RPTR_UPDATE_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PHY_MASTER_DELAY_HALF_MEASURE_0							
R/W							
0h							

Table 14-15099. EMIF_CTLCFG_DENALI_PHY_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WRLVL_DLY_FINE_STEP_0	R/W	0h	DQS target delay fine step size during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_WRLVL_DLY_STEP_0	R/W	0h	DQS target delay step size during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RPTR_UPDATE_0	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_MASTER_DELAY_HALF_MEASURE_0	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle in the data slice controller for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.915 EMIF_CTLCFG_DENALI_PHY_96 Register

1 EMIF_CTLCFG_DENALI_PHY_96 Register (Offset = 4180h) [reset = 0h]

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Table 14-15100. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C180h**

Figure 14-4994. EMIF_CTLCFG_DENALI_PHY_96 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_GTLVL_RESP_WAIT_CNT_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED				PHY_GTLVL_DLY_STEP_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WRLVL_RESP_WAIT_CNT_0					
NONE		R/W					
0h		0h					

Table 14-15102. EMIF_CTLCFG_DENALI_PHY_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_GTLVL_RESP_WAIT_CNT_0	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 0. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_GTLVL_DLY_STEP_0	R/W	0h	DQS target delay step size during gate training for slice 0. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WRLVL_RESP_WAIT_CNT_0	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.916 EMIF_CTLCFG_DENALI_PHY_97 Register

1 EMIF_CTLCFG_DENALI_PHY_97 Register (Offset = 4184h) [reset = 0h]

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Table 14-15103. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C184h**

Figure 14-4995. EMIF_CTLCFG_DENALI_PHY_97 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_GTLVL_FINAL_STEP_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_GTLVL_FINAL_STEP_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_GTLVL_BACK_STEP_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_GTLVL_BACK_STEP_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15105. EMIF_CTLCFG_DENALI_PHY_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GTLVL_FINAL_STEP_0	R/W	0h	Final backup step delay used in gate training algorithm for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_BACK_STEP_0	R/W	0h	Interim backup step delay used in gate training algorithm for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.917 EMIF_CTLCFG_DENALI_PHY_98 Register

1 EMIF_CTLCFG_DENALI_PHY_98 Register (Offset = 4188h) [reset = 0h]

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Table 14-15106. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C188h**

Figure 14-4996. EMIF_CTLCFG_DENALI_PHY_98 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_WDQLVL_DM_SEARCH_RANGE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WDQLVL_DM_SEARCH_RANGE_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DLY_STEP_0							
R/W							
0h							

Table 14-15108. EMIF_CTLCFG_DENALI_PHY_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_WDQLVL_DM_SEARCH_RANGE_0	R/W	0h	The dm target delay search range for non-lpddr4 DM training for slice 0. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WDQLVL_QTR_DLY_STEP_0	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 0. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_DLY_STEP_0	R/W	0h	DQ target delay step size during write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.918 EMIF_CTLCFG_DENALI_PHY_99 Register

1 EMIF_CTLCFG_DENALI_PHY_99 Register (Offset = 418Ch) [reset = 0h]

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Table 14-15109. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C18Ch**

Figure 14-4997. EMIF_CTLCFG_DENALI_PHY_99 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_RDLVL_DLY_STEP_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_TOGGLE_PRE_SUPPORT_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-15111. EMIF_CTLCFG_DENALI_PHY_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_DLY_STEP_0	R/W	0h	DQS target delay step size during read leveling for slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_TOGGLE_PRE_SUPPORT_0	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.919 EMIF_CTLCFG_DENALI_PHY_100 Register

1 EMIF_CTLCFG_DENALI_PHY_100 Register (Offset = 4190h) [reset = 0h]

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Table 14-15112. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C190h

Figure 14-4998. EMIF_CTLCFG_DENALI_PHY_100 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDLVL_MAX_EDGE_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_MAX_EDGE_0							
R/W							
0h							

Table 14-15114. EMIF_CTLCFG_DENALI_PHY_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_MAX_EDGE_0	R/W	0h	The maximun rdlvl target delay search window for read eye training for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.920 EMIF_CTLCFG_DENALI_PHY_101 Register

1 EMIF_CTLCFG_DENALI_PHY_101 Register (Offset = 4194h) [reset = 0h]

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Table 14-15115. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C194h**

Figure 14-4999. EMIF_CTLCFG_DENALI_PHY_101 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_MEAS_DLY_STEP_ENABLE_0						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PHY_WDQ_OSC_DELTA_0						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WRPATH_GATE_TIMING_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_WRPATH_GATE_DISABLE_0	
NONE						R/W	
0h						0h	

Table 14-15117. EMIF_CTLCFG_DENALI_PHY_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_MEAS_DLY_STEP_ENABLE_0	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 0. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PHY_WDQ_OSC_DELTA_0	R/W	0h	Target delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRPATH_GATE_TIMING_0	R/W	0h	Write path clock gating timing for slice 0. it means additional clock number to write path clock gate Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRPATH_GATE_DISABLE_0	R/W	0h	Write path clock gating disable for slice 0. [0]: disable pull in wrdata_en; [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n

14.5.1.2.921 EMIF_CTLCFG_DENALI_PHY_102 Register

1 EMIF_CTLCFG_DENALI_PHY_102 Register (Offset = 4198h) [reset = 0h]

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Table 14-15118. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C198h**

Figure 14-5000. EMIF_CTLCFG_DENALI_PHY_102 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PHY_RDDATA_EN_DLY_0				
NONE			R/W				
0h			0h				

Table 14-15120. EMIF_CTLCFG_DENALI_PHY_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	PHY_RDDATA_EN_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.922 EMIF_CTLCFG_DENALI_PHY_103 Register

1 EMIF_CTLCFG_DENALI_PHY_103 Register (Offset = 419Ch) [reset = 0h]

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Table 14-15121. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C19Ch**

Figure 14-5001. EMIF_CTLCFG_DENALI_PHY_103 Name Register

31	30	29	28	27	26	25	24
PHY_DQ_DM_SWIZZLE0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DQ_DM_SWIZZLE0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DQ_DM_SWIZZLE0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_0							
R/W							
0h							

Table 14-15123. EMIF_CTLCFG_DENALI_PHY_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DQ_DM_SWIZZLE0_0	R/W	0h	DQ/DM bit swizzling 0 for slice 0. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DQ0, Bits [7:4] inform the PHY which bit in {DM,DQ} map to DQ1, etc. Reset Source: ctl_amod_g_rst_n

14.5.1.2.923 EMIF_CTLCFG_DENALI_PHY_104 Register

1 EMIF_CTLCFG_DENALI_PHY_104 Register (Offset = 41A0h) [reset = 0h]

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Table 14-15124. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1A0h

Figure 14-5002. EMIF_CTLCFG_DENALI_PHY_104 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_DM_SWIZZLE1_0			
NONE				R/W			
0h				0h			

Table 14-15126. EMIF_CTLCFG_DENALI_PHY_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_DQ_DM_SWIZZLE1_0	R/W	0h	DQ/DM bit swizzling 1 for slice 0. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DM. Reset Source: ctl_amod_g_rst_n

14.5.1.2.924 EMIF_CTLCFG_DENALI_PHY_105 Register

1 EMIF_CTLCFG_DENALI_PHY_105 Register (Offset = 41A4h) [reset = 0h]

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Table 14-15127. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 C1A4h**

Figure 14-5003. EMIF_CTLCFG_DENALI_PHY_105 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ1_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ0_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15129. EMIF_CTLCFG_DENALI_PHY_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ1_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ1 for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ0_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ0 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.925 EMIF_CTLCFG_DENALI_PHY_106 Register

1 EMIF_CTLCFG_DENALI_PHY_106 Register (Offset = 41A8h) [reset = 0h]

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Table 14-15130. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1A8h**

Figure 14-5004. EMIF_CTLCFG_DENALI_PHY_106 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WRDQ3_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDQ2_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15132. EMIF_CTLCFG_DENALI_PHY_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ3_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ3 for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ2_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ2 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.926 EMIF_CTLCFG_DENALI_PHY_107 Register

1 EMIF_CTLCFG_DENALI_PHY_107 Register (Offset = 41ACh) [reset = 0h]

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Table 14-15133. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1ACh**

Figure 14-5005. EMIF_CTLCFG_DENALI_PHY_107 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WRDQ5_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDQ4_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15135. EMIF_CTLCFG_DENALI_PHY_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ5_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ5 for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ4_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ4 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.927 EMIF_CTLCFG_DENALI_PHY_108 Register

1 EMIF_CTLCFG_DENALI_PHY_108 Register (Offset = 41B0h) [reset = 0h]

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Table 14-15136. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1B0h

Figure 14-5006. EMIF_CTLCFG_DENALI_PHY_108 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WRDQ7_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDQ6_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15138. EMIF_CTLCFG_DENALI_PHY_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ7_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ7 for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ6_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQ6 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.928 EMIF_CTLCFG_DENALI_PHY_109 Register

1 EMIF_CTLCFG_DENALI_PHY_109 Register (Offset = 41B4h) [reset = 0h]

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Table 14-15139. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1B4h

Figure 14-5007. EMIF_CTLCFG_DENALI_PHY_109 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_CLK_WRDQS_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDM_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDM_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15141. EMIF_CTLCFG_DENALI_PHY_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_CLK_WRDQS_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DQS for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDM_SLAVE_DELAY_0	R/W	0h	Write clock target delay setting for DM for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.929 EMIF_CTLCFG_DENALI_PHY_110 Register

1 EMIF_CTLCFG_DENALI_PHY_110 Register (Offset = 41B8h) [reset = 0h]

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Table 14-15142. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1B8h

Figure 14-5008. EMIF_CTLCFG_DENALI_PHY_110 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_0	
NONE						R/W	
0h						0h	

Table 14-15144. EMIF_CTLCFG_DENALI_PHY_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ0 for slice 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRLVL_THRESHOLD_ADJUST_0	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.930 EMIF_CTLCFG_DENALI_PHY_111 Register

1 EMIF_CTLCFG_DENALI_PHY_111 Register (Offset = 41BCh) [reset = 0h]

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Table 14-15145. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1BCh

Figure 14-5009. EMIF_CTLCFG_DENALI_PHY_111 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15147. EMIF_CTLCFG_DENALI_PHY_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ1 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ0 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.931 EMIF_CTLCFG_DENALI_PHY_112 Register

1 EMIF_CTLCFG_DENALI_PHY_112 Register (Offset = 41C0h) [reset = 0h]

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Table 14-15148. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1C0h**

Figure 14-5010. EMIF_CTLCFG_DENALI_PHY_112 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15150. EMIF_CTLCFG_DENALI_PHY_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ2 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ1 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.932 EMIF_CTLCFG_DENALI_PHY_113 Register

1 EMIF_CTLCFG_DENALI_PHY_113 Register (Offset = 41C4h) [reset = 0h]

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Table 14-15151. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1C4h**

Figure 14-5011. EMIF_CTLCFG_DENALI_PHY_113 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15153. EMIF_CTLCFG_DENALI_PHY_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ3 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ2 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.933 EMIF_CTLCFG_DENALI_PHY_114 Register

1 EMIF_CTLCFG_DENALI_PHY_114 Register (Offset = 41C8h) [reset = 0h]

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Table 14-15154. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1C8h**

Figure 14-5012. EMIF_CTLCFG_DENALI_PHY_114 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15156. EMIF_CTLCFG_DENALI_PHY_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ4 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ3 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.934 EMIF_CTLCFG_DENALI_PHY_115 Register

1 EMIF_CTLCFG_DENALI_PHY_115 Register (Offset = 41CCh) [reset = 0h]

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Table 14-15157. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1CCh

Figure 14-5013. EMIF_CTLCFG_DENALI_PHY_115 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15159. EMIF_CTLCFG_DENALI_PHY_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ5 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ4 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.935 EMIF_CTLCFG_DENALI_PHY_116 Register

1 EMIF_CTLCFG_DENALI_PHY_116 Register (Offset = 41D0h) [reset = 0h]

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Table 14-15160. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1D0h

Figure 14-5014. EMIF_CTLCFG_DENALI_PHY_116 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15162. EMIF_CTLCFG_DENALI_PHY_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ6 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ5 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.936 EMIF_CTLCFG_DENALI_PHY_117 Register

1 EMIF_CTLCFG_DENALI_PHY_117 Register (Offset = 41D4h) [reset = 0h]

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Table 14-15163. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1D4h

Figure 14-5015. EMIF_CTLCFG_DENALI_PHY_117 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15165. EMIF_CTLCFG_DENALI_PHY_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DQ7 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ6 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.937 EMIF_CTLCFG_DENALI_PHY_118 Register

1 EMIF_CTLCFG_DENALI_PHY_118 Register (Offset = 41D8h) [reset = 0h]

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Table 14-15166. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1D8h**

Figure 14-5016. EMIF_CTLCFG_DENALI_PHY_118 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DM_RISE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15168. EMIF_CTLCFG_DENALI_PHY_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS target delay setting for DM for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DQ7 for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.938 EMIF_CTLCFG_DENALI_PHY_119 Register

1 EMIF_CTLCFG_DENALI_PHY_119 Register (Offset = 41DCh) [reset = 0h]

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Table 14-15169. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1DCh**

Figure 14-5017. EMIF_CTLCFG_DENALI_PHY_119 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_GATE_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DM_FALL_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15171. EMIF_CTLCFG_DENALI_PHY_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_GATE_SLAVE_DELAY_0	R/W	0h	Read DQS target delay setting for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS target delay setting for DM for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.939 EMIF_CTLCFG_DENALI_PHY_120 Register

1 EMIF_CTLCFG_DENALI_PHY_120 Register (Offset = 41E0h) [reset = 0h]

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Table 14-15172. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1E0h**

Figure 14-5018. EMIF_CTLCFG_DENALI_PHY_120 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_DELAY_EARLY_THRESHOLD_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WRITE_PATH_LAT_ADD_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_RDDQS_LATENCY_ADJUST_0			
NONE				R/W			
0h				0h			

Table 14-15174. EMIF_CTLCFG_DENALI_PHY_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_0	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRITE_PATH_LAT_ADD_0	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_LATENCY_ADJUST_0	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.940 EMIF_CTLCFG_DENALI_PHY_121 Register

1 EMIF_CTLCFG_DENALI_PHY_121 Register (Offset = 41E4h) [reset = 0h]

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Table 14-15175. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1E4h

Figure 14-5019. EMIF_CTLCFG_DENALI_PHY_121 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							PHY_WRLVL_EARLY_FORCE_ZERO_0
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0							
R/W							
0h							

Table 14-15177. EMIF_CTLCFG_DENALI_PHY_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_WRLVL_EARLY_FORCE_ZERO_0	R/W	0h	Force the final write level delay value [that meets the early threshold] to 0 for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.941 EMIF_CTLCFG_DENALI_PHY_122 Register

1 EMIF_CTLCFG_DENALI_PHY_122 Register (Offset = 41E8h) [reset = 0h]

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Table 14-15178. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1E8h**

Figure 14-5020. EMIF_CTLCFG_DENALI_PHY_122 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_LAT_ADJ_START_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_RDDQS_SLV_DLY_START_0							
R/W							
0h							

Table 14-15180. EMIF_CTLCFG_DENALI_PHY_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_GTLVL_LAT_ADJ_START_0	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 0. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_RDDQS_SLV_DLY_START_0	R/W	0h	Initial read DQS gate target delay setting during gate training for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.942 EMIF_CTLCFG_DENALI_PHY_123 Register

1 EMIF_CTLCFG_DENALI_PHY_123 Register (Offset = 41ECh) [reset = 0h]

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Table 14-15181. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1ECh**

Figure 14-5021. EMIF_CTLCFG_DENALI_PHY_123 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PASS_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_NTP_WRLAT_START_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_SLV_DLY_START_0							
R/W							
0h							

Table 14-15183. EMIF_CTLCFG_DENALI_PHY_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_NTP_PASS_0	R/W	0h	Indicates if No-topology training found a passing result for slice 0. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_NTP_WRLAT_START_0	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_START_0	R/W	0h	Initial DQ/DM target delay setting during write data leveling for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.943 EMIF_CTLCFG_DENALI_PHY_124 Register

1 EMIF_CTLCFG_DENALI_PHY_124 Register (Offset = 41F0h) [reset = 0h]

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Table 14-15184. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C1F0h

Figure 14-5022. EMIF_CTLCFG_DENALI_PHY_124 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0							
R/W							
0h							

Table 14-15186. EMIF_CTLCFG_DENALI_PHY_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0	R/W	0h	Read leveling starting value for the DQS/DQ target delay settings for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.944 EMIF_CTLCFG_DENALI_PHY_125 Register

1 EMIF_CTLCFG_DENALI_PHY_125 Register (Offset = 41F4h) [reset = 0h]

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Table 14-15187. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C1F4h**

Figure 14-5023. EMIF_CTLCFG_DENALI_PHY_125 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_DSLICE_PAD_RX_CTLE_SETTING_0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DSLICE_PAD_BOOSTPN_SETTING_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DSLICE_PAD_BOOSTPN_SETTING_0							
R/W							
0h							

Table 14-15189. EMIF_CTLCFG_DENALI_PHY_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PHY_DSLICE_PAD_RX_CTLE_SETTING_0	R/W	0h	Setting for RX ctle P/N of pad for slice 0. Reset Source: ctl_amod_g_rst_n
15:0	PHY_DSLICE_PAD_BOOSTPN_SETTING_0	R/W	0h	Setting for boost P/N of pad for slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.945 EMIF_CTLCFG_DENALI_PHY_256 Register

1 EMIF_CTLCFG_DENALI_PHY_256 Register (Offset = 4400h) [reset = 0h]

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Table 14-15190. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C400h**

Figure 14-5024. EMIF_CTLCFG_DENALI_PHY_256 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WR_BYPASS_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_1						
NONE	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PHY_LP4_BOOT_RX_PCLK_CLK_SEL_1		
NONE					R/W		
0h					0h		

Table 14-15192. EMIF_CTLCFG_DENALI_PHY_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WR_BYPASS_SLAVE_DELAY_1	R/W	0h	Write data clock bypass mode target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_LP4_BOOT_PAD_DSLICE_IO_CFG_1	R/W	0h	Controls PCLK/PARK pin for pad for slice 1 with boot frequency. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_LP4_BOOT_RX_PCLK_CLK_SEL_1	R/W	0h	RX_PCLK boot clock frequency selection for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.946 EMIF_CTLCFG_DENALI_PHY_257 Register

1 EMIF_CTLCFG_DENALI_PHY_257 Register (Offset = 4404h) [reset = 0h]

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Table 14-15193. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C404h

Figure 14-5025. EMIF_CTLCFG_DENALI_PHY_257 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_1			
NONE				R/W			
0h				0h			

Table 14-15195. EMIF_CTLCFG_DENALI_PHY_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_WRITE_PATH_LAT_ADD_BYPASS_1	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1	R/W	0h	Write DQS bypass mode target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_BYPASS_1	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.947 EMIF_CTLCFG_DENALI_PHY_258 Register

1 EMIF_CTLCFG_DENALI_PHY_258 Register (Offset = 4408h) [reset = 0h]

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Table 14-15196. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C408h**

Figure 14-5026. EMIF_CTLCFG_DENALI_PHY_258 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_BYPASS_TWO_CYC_PREAMBLE_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15198. EMIF_CTLCFG_DENALI_PHY_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CLK_BYPASS_OVERRIDE_1	R/W	0h	Bypass mode override setting for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_BYPASS_TWO_CYC_PREAMBLE_1	R/W	0h	Two_cycle_preamble for bypass mode for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1	R/W	0h	Read DQS bypass mode target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.948 EMIF_CTLCFG_DENALI_PHY_259 Register

1 EMIF_CTLCFG_DENALI_PHY_259 Register (Offset = 440Ch) [reset = 0h]

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Table 14-15199. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C40Ch

Figure 14-5027. EMIF_CTLCFG_DENALI_PHY_259 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ2_SHIFT_1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ1_SHIFT_1					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ0_SHIFT_1					
NONE		R/W					
0h		0h					

Table 14-15201. EMIF_CTLCFG_DENALI_PHY_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ3_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ2_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ1_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-15201. EMIF_CTLCFG_DENALI_PHY_259 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ0_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.949 EMIF_CTLCFG_DENALI_PHY_260 Register

1 EMIF_CTLCFG_DENALI_PHY_260 Register (Offset = 4410h) [reset = 0h]

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Table 14-15202. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C410h**

Figure 14-5028. EMIF_CTLCFG_DENALI_PHY_260 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_SW_WRDQ6_SHIFT_1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_SW_WRDQ5_SHIFT_1					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDQ4_SHIFT_1					
NONE		R/W					
0h		0h					

Table 14-15204. EMIF_CTLCFG_DENALI_PHY_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_SW_WRDQ7_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_SW_WRDQ6_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_SW_WRDQ5_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-15204. EMIF_CTLCFG_DENALI_PHY_260 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDQ4_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.950 EMIF_CTLCFG_DENALI_PHY_261 Register

1 EMIF_CTLCFG_DENALI_PHY_261 Register (Offset = 4414h) [reset = 0h]

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Table 14-15205. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C414h**

Figure 14-5029. EMIF_CTLCFG_DENALI_PHY_261 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_LP4_BOOT_RDDATA_EN_DLY_1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_LP4_BOOT_RDDATA_EN_IE_DLY_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_SW_WRDQS_SHIFT_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_SW_WRDM_SHIFT_1					
NONE		R/W					
0h		0h					

Table 14-15207. EMIF_CTLCFG_DENALI_PHY_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_LP4_BOOT_RDDATA_EN_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SW_WRDQS_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bit [3] is the cycle_shift value. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-15207. EMIF_CTLCFG_DENALI_PHY_261 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PHY_SW_WRDM_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] are the cycle_shift value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.951 EMIF_CTLCFG_DENALI_PHY_262 Register

1 EMIF_CTLCFG_DENALI_PHY_262 Register (Offset = 4418h) [reset = 0h]

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Table 14-15208. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C418h**

Figure 14-5030. EMIF_CTLCFG_DENALI_PHY_262 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED			PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_1				
NONE			R/W				
0h			0h				

Table 14-15210. EMIF_CTLCFG_DENALI_PHY_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_1	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 1. Bit [0]: disable pull in wrdata_en; Bit [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_LP4_BOOT_RPTR_UPDATE_1	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.952 EMIF_CTLCFG_DENALI_PHY_263 Register

1 EMIF_CTLCFG_DENALI_PHY_263 Register (Offset = 441Ch) [reset = 0h]

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Table 14-15211. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C41Ch

Figure 14-5031. EMIF_CTLCFG_DENALI_PHY_263 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_CONTROL_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_LPBK_CONTROL_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_CTRL_LPBK_EN_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_LP4_BOOT_RDDATA_EN_OE_DLY_1				
NONE			R/W				
0h			0h				

Table 14-15213. EMIF_CTLCFG_DENALI_PHY_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_LPBK_CONTROL_1	R/W	0h	Loopback control bits for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_CTRL_LPBK_EN_1	R/W	0h	Loopback control en for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.953 EMIF_CTLCFG_DENALI_PHY_264 Register

1 EMIF_CTLCFG_DENALI_PHY_264 Register (Offset = 4420h) [reset = 0h]

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Table 14-15214. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C420h

Figure 14-5032. EMIF_CTLCFG_DENALI_PHY_264 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_GATE_DELAY_COMP_DISABLE_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_LPBK_DFX_TIMEOUT_EN_1
NONE							R/W
0h							0h

Table 14-15216. EMIF_CTLCFG_DENALI_PHY_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_GATE_DELAY_COMP_DISABLE_1	R/W	0h	use the control whether to compensate half_cycle when gate_target_delay is larger than half_cycle for the gate close for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPBK_DFX_TIMEOUT_EN_1	R/W	0h	Loopback read only test timeout mechanism enable for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.954 EMIF_CTLCFG_DENALI_PHY_265 Register

1 EMIF_CTLCFG_DENALI_PHY_265 Register (Offset = 4424h) [reset = 0h]

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Table 14-15217. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C424h**

Figure 14-5033. EMIF_CTLCFG_DENALI_PHY_265 Name Register

31	30	29	28	27	26	25	24
PHY_AUTO_TIMING_MARGIN_CONTROL_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_AUTO_TIMING_MARGIN_CONTROL_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_AUTO_TIMING_MARGIN_CONTROL_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_AUTO_TIMING_MARGIN_CONTROL_1							
R/W							
0h							

Table 14-15219. EMIF_CTLCFG_DENALI_PHY_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_AUTO_TIMING_MARGIN_CONTROL_1	R/W	0h	Auto timing marging control bits for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.955 EMIF_CTLCFG_DENALI_PHY_266 Register

1 EMIF_CTLCFG_DENALI_PHY_266 Register (Offset = 4428h) [reset = 0h]

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Table 14-15220. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C428h**

Figure 14-5034. EMIF_CTLCFG_DENALI_PHY_266 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_1			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_AUTO_TIMING_MARGIN_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_AUTO_TIMING_MARGIN_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_AUTO_TIMING_MARGIN_OBS_1							
R							
0h							

Table 14-15222. EMIF_CTLCFG_DENALI_PHY_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_AUTO_TIMING_MARGIN_OBS_1	R	0h	Observation register for the auto_timing_margin for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.956 EMIF_CTLCFG_DENALI_PHY_267 Register

1 EMIF_CTLCFG_DENALI_PHY_267 Register (Offset = 442Ch) [reset = 1000000h]

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Table 14-15223. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C42Ch**

Figure 14-5035. EMIF_CTLCFG_DENALI_PHY_267 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_PRBS_PATTERN_START_1						
NONE	R/W						
0h	1h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_PDA_MODE_EN_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_DQ_IDLE_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_IDLE_1							
R/W							
0h							

Table 14-15225. EMIF_CTLCFG_DENALI_PHY_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_PRBS_PATTERN_START_1	R/W	1h	PRBS7 start pattern for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_PDA_MODE_EN_1	R/W	0h	When set to 1, the invalid DQs will be driven by the dfi_wrdata to make sure the tpda_s and tpda_h's timing is meet for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_DQ_IDLE_1	R/W	0h	When set to 1, the inavlid DQ will be driven to high, when set to 0, the invalid DQ will be driven to low for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.957 EMIF_CTLCFG_DENALI_PHY_268 Register

1 EMIF_CTLCFG_DENALI_PHY_268 Register (Offset = 4430h) [reset = 0h]

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Table 14-15226. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C430h**

Figure 14-5036. EMIF_CTLCFG_DENALI_PHY_268 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_RDLVL_MULTI_PATT_RST_DISABLE_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_RDLVL_MULTI_PATT_ENABLE_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_PRBS_PATTERN_MASK_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PRBS_PATTERN_MASK_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15228. EMIF_CTLCFG_DENALI_PHY_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_RDLVL_MULTI_PATT_RST_DISABLE_1	R/W	0h	Read Leveling read level windows disable reset for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_RDLVL_MULTI_PATT_ENABLE_1	R/W	0h	Read Leveling Multi-pattern enable for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_PRBS_PATTERN_MASK_1	R/W	0h	PRBS7 mask signal for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.958 EMIF_CTLCFG_DENALI_PHY_269 Register

1 EMIF_CTLCFG_DENALI_PHY_269 Register (Offset = 4434h) [reset = 0h]

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Table 14-15229. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C434h**

Figure 14-5037. EMIF_CTLCFG_DENALI_PHY_269 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED	PHY_VREF_TRAIN_OBS_1						
NONE	R						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED		PHY_VREF_INITIAL_STEPSIZE_1					
NONE		R/W					
0h		0h					

Table 14-15231. EMIF_CTLCFG_DENALI_PHY_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1	R/W	0h	Read DQS data clock bypass mode target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_VREF_TRAIN_OBS_1	R	0h	Observation register for best vref value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_VREF_INITIAL_STEPSIZE_1	R/W	0h	Data slice initial VREF training step size for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.959 EMIF_CTLCFG_DENALI_PHY_270 Register

1 EMIF_CTLCFG_DENALI_PHY_270 Register (Offset = 4438h) [reset = 0h]

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Table 14-15232. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C438h**

Figure 14-5038. EMIF_CTLCFG_DENALI_PHY_270 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL1_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_SNAP_OBS_REGS_1
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_1			
NONE				R/W			
0h				0h			

Table 14-15234. EMIF_CTLCFG_DENALI_PHY_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL1_SLAVE_DELAY_1	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_SNAP_OBS_REGS_1	W	0h	Initiates a snapshot of the internal observation registers for slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_GATE_ERROR_DELAY_SELECT_1	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.960 EMIF_CTLCFG_DENALI_PHY_271 Register

1 EMIF_CTLCFG_DENALI_PHY_271 Register (Offset = 443Ch) [reset = 0h]

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Table 14-15235. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C43Ch**

Figure 14-5039. EMIF_CTLCFG_DENALI_PHY_271 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GATE_SMPL2_SLAVE_DELAY_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_MEM_CLASS_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							PHY_LPDDR_1
NONE							R/W
0h							0h

Table 14-15237. EMIF_CTLCFG_DENALI_PHY_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_GATE_SMPL2_SLAVE_DELAY_1	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_MEM_CLASS_1	R/W	0h	Indicates the type of DRAM for slice 1. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4 Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPDDR_1	R/W	0h	Adds a cycle of delay for the slice 1 to match the address slice. Set to 1 to add a cycle Reset Source: ctl_amod_g_rst_n

14.5.1.2.961 *EMIF_CTLCFG_DENALI_PHY_272 Register*

1 EMIF_CTLCFG_DENALI_PHY_272 Register (Offset = 4440h) [reset = 0h]

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Table 14-15238. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C440h**

Figure 14-5040. EMIF_CTLCFG_DENALI_PHY_272 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ON_FLY_GATE_ADJUST_EN_1	
NONE						R/W	
0h						0h	

Table 14-15240. EMIF_CTLCFG_DENALI_PHY_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ON_FLY_GATE_ADJUST_EN_1	R/W	0h	Control the on-the-fly gate adjustment for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.962 EMIF_CTLCFG_DENALI_PHY_273 Register

1 EMIF_CTLCFG_DENALI_PHY_273 Register (Offset = 4444h) [reset = 0h]

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Table 14-15241. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C444h

Figure 14-5041. EMIF_CTLCFG_DENALI_PHY_273 Name Register

31	30	29	28	27	26	25	24
PHY_GATE_TRACKING_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_GATE_TRACKING_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_GATE_TRACKING_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_1							
R							
0h							

Table 14-15243. EMIF_CTLCFG_DENALI_PHY_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_GATE_TRACKING_OBS_1	R	0h	Report the on-the-fly gate measurement result for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.963 EMIF_CTLCFG_DENALI_PHY_274 Register

1 EMIF_CTLCFG_DENALI_PHY_274 Register (Offset = 4448h) [reset = 0h]

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Table 14-15244. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C448h

Figure 14-5042. EMIF_CTLCFG_DENALI_PHY_274 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_LP4_PST_AMBLE_1	
NONE						R/W	
0h						0h	

Table 14-15246. EMIF_CTLCFG_DENALI_PHY_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_LP4_PST_AMBLE_1	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.964 EMIF_CTLCFG_DENALI_PHY_275 Register

1 EMIF_CTLCFG_DENALI_PHY_275 Register (Offset = 444Ch) [reset = 0h]

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Table 14-15247. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C44Ch

Figure 14-5043. EMIF_CTLCFG_DENALI_PHY_275 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT8_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT8_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT8_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_1							
R/W							
0h							

Table 14-15249. EMIF_CTLCFG_DENALI_PHY_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT8_1	R/W	0h	Read leveling pattern 8 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.965 EMIF_CTLCFG_DENALI_PHY_276 Register

1 EMIF_CTLCFG_DENALI_PHY_276 Register (Offset = 4450h) [reset = 0h]

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Table 14-15250. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C450h**

Figure 14-5044. EMIF_CTLCFG_DENALI_PHY_276 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT9_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT9_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT9_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_1							
R/W							
0h							

Table 14-15252. EMIF_CTLCFG_DENALI_PHY_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT9_1	R/W	0h	Read leveling pattern 9 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.966 EMIF_CTLCFG_DENALI_PHY_277 Register

1 EMIF_CTLCFG_DENALI_PHY_277 Register (Offset = 4454h) [reset = 0h]

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Table 14-15253. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C454h**

Figure 14-5045. EMIF_CTLCFG_DENALI_PHY_277 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT10_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT10_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT10_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT10_1							
R/W							
0h							

Table 14-15255. EMIF_CTLCFG_DENALI_PHY_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT10_1	R/W	0h	Read leveling pattern 10 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.967 EMIF_CTLCFG_DENALI_PHY_278 Register

1 EMIF_CTLCFG_DENALI_PHY_278 Register (Offset = 4458h) [reset = 0h]

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Table 14-15256. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C458h**

Figure 14-5046. EMIF_CTLCFG_DENALI_PHY_278 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT11_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT11_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT11_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_1							
R/W							
0h							

Table 14-15258. EMIF_CTLCFG_DENALI_PHY_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT11_1	R/W	0h	Read leveling pattern 11 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.968 EMIF_CTLCFG_DENALI_PHY_279 Register

1 EMIF_CTLCFG_DENALI_PHY_279 Register (Offset = 445Ch) [reset = 0h]

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Table 14-15259. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C45Ch**

Figure 14-5047. EMIF_CTLCFG_DENALI_PHY_279 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT12_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT12_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT12_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_1							
R/W							
0h							

Table 14-15261. EMIF_CTLCFG_DENALI_PHY_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT12_1	R/W	0h	Read leveling pattern 12 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.969 EMIF_CTLCFG_DENALI_PHY_280 Register

1 EMIF_CTLCFG_DENALI_PHY_280 Register (Offset = 4460h) [reset = 0h]

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Table 14-15262. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C460h**

Figure 14-5048. EMIF_CTLCFG_DENALI_PHY_280 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT13_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT13_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT13_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT13_1							
R/W							
0h							

Table 14-15264. EMIF_CTLCFG_DENALI_PHY_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT13_1	R/W	0h	Read leveling pattern 13 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.970 EMIF_CTLCFG_DENALI_PHY_281 Register

1 EMIF_CTLCFG_DENALI_PHY_281 Register (Offset = 4464h) [reset = 0h]

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Table 14-15265. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C464h**

Figure 14-5049. EMIF_CTLCFG_DENALI_PHY_281 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT14_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT14_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT14_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_1							
R/W							
0h							

Table 14-15267. EMIF_CTLCFG_DENALI_PHY_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT14_1	R/W	0h	Read leveling pattern 14 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.971 EMIF_CTLCFG_DENALI_PHY_282 Register

1 EMIF_CTLCFG_DENALI_PHY_282 Register (Offset = 4468h) [reset = 0h]

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Table 14-15268. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C468h

Figure 14-5050. EMIF_CTLCFG_DENALI_PHY_282 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_PATT15_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_PATT15_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_PATT15_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_1							
R/W							
0h							

Table 14-15270. EMIF_CTLCFG_DENALI_PHY_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_PATT15_1	R/W	0h	Read leveling pattern 15 data for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.972 EMIF_CTLCFG_DENALI_PHY_283 Register

1 EMIF_CTLCFG_DENALI_PHY_283 Register (Offset = 446Ch) [reset = 0h]

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Table 14-15271. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C46Ch**

Figure 14-5051. EMIF_CTLCFG_DENALI_PHY_283 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_RDDQ_ENC_OBS_SELECT_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_MASTER_DLY_LOCK_OBS_SELECT_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_SW_FIFO_PTR_RST_DISABLE_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_SLAVE_LOOP_CNT_UPDATE_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-15273. EMIF_CTLCFG_DENALI_PHY_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_RDDQ_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal read DQ target delay encoded settings to the accessible read DQ encoded target delay observation register for slice 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_MASTER_DLY_LOCK_OBS_SELECT_1	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_SW_FIFO_PTR_RST_DISABLE_1	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 1. Set to 1 to disable automatic resets. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_SLAVE_LOOP_CNT_UPDATE_1	R/W	0h	Reserved for future use for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.973 EMIF_CTLCFG_DENALI_PHY_284 Register

1 EMIF_CTLCFG_DENALI_PHY_284 Register (Offset = 4470h) [reset = 0h]

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Table 14-15274. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C470h**

Figure 14-5052. EMIF_CTLCFG_DENALI_PHY_284 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_1			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WR_SHIFT_OBS_SELECT_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WR_ENC_OBS_SELECT_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_1			
NONE				R/W			
0h				0h			

Table 14-15276. EMIF_CTLCFG_DENALI_PHY_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_FIFO_PTR_OBS_SELECT_1	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WR_SHIFT_OBS_SELECT_1	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WR_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal write DQ target delay encoded settings to the accessible write DQ encoded target delay observation register for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_DQ_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal read DQS DQ rise/fall target delay encoded settings to the accessible read DQS DQ rise/fall encoded target delay observation registers for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.974 EMIF_CTLCFG_DENALI_PHY_285 Register

1 EMIF_CTLCFG_DENALI_PHY_285 Register (Offset = 4474h) [reset = 0h]

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Table 14-15277. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C474h**

Figure 14-5053. EMIF_CTLCFG_DENALI_PHY_285 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_WRLVL_CAPTURE_CNT_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_WRLVL_ALGO_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_LVL_DEBUG_CONT_1
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_LVL_DEBUG_MODE_1
NONE							R/W
0h							0h

Table 14-15279. EMIF_CTLCFG_DENALI_PHY_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_WRLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS target delay setting during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_WRLVL_ALGO_1	R/W	0h	Write leveling algorithm selection for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_LVL_DEBUG_CONT_1	W	0h	Allows the leveling state machine to advance [when in debug mode] for slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LVL_DEBUG_MODE_1	R/W	0h	Enables leveling debug mode for slice 1. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.975 EMIF_CTLCFG_DENALI_PHY_286 Register

1 EMIF_CTLCFG_DENALI_PHY_286 Register (Offset = 4478h) [reset = 0h]

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Table 14-15280. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C478h**

Figure 14-5054. EMIF_CTLCFG_DENALI_PHY_286 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_GTLVL_CAPTURE_CNT_1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_MASK_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_1			
NONE				R/W			
0h				0h			

Table 14-15282. EMIF_CTLCFG_DENALI_PHY_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_GTLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles + 4 to wait after changing DQS target delay setting during gate training for slice 1. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_GTLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS target delay setting during gate training for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_MASK_1	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_WRLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing DQS target delay setting during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.976 EMIF_CTLCFG_DENALI_PHY_287 Register

1 EMIF_CTLCFG_DENALI_PHY_287 Register (Offset = 447Ch) [reset = 0h]

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Table 14-15283. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C47Ch**

Figure 14-5055. EMIF_CTLCFG_DENALI_PHY_287 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RDLVL_RDDQS_DQ_OBS_SELECT_1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_RDLVL_OP_MODE_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_RDLVL_UPDT_WAIT_CNT_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_RDLVL_CAPTURE_CNT_1					
NONE		R/W					
0h		0h					

Table 14-15285. EMIF_CTLCFG_DENALI_PHY_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_1	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_RDLVL_OP_MODE_1	R/W	0h	Read leveling algorithm select for slice 1. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing DQS target delay setting during read leveling for slice 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_RDLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS target delay setting during read leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.977 EMIF_CTLCFG_DENALI_PHY_288 Register

1 EMIF_CTLCFG_DENALI_PHY_288 Register (Offset = 4480h) [reset = 0h]

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Table 14-15286. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C480h**

Figure 14-5056. EMIF_CTLCFG_DENALI_PHY_288 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_DATA_SWIZZLE_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_DATA_SWIZZLE_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_RDLVL_DATA_SWIZZLE_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_DATA_MASK_1							
R/W							
0h							

Table 14-15288. EMIF_CTLCFG_DENALI_PHY_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:8	PHY_RDLVL_DATA_SWIZZLE_1	R/W	0h	Read level bit swizzling for DDR4 operation for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDLVL_DATA_MASK_1	R/W	0h	Per-bit mask for read leveling for slice 1. If all bits are not used, only 1 bit should be cleared to 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.978 EMIF_CTLCFG_DENALI_PHY_289 Register

1 EMIF_CTLCFG_DENALI_PHY_289 Register (Offset = 4484h) [reset = 0h]

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Table 14-15289. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C484h**

Figure 14-5057. EMIF_CTLCFG_DENALI_PHY_289 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_PATT_1		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED		PHY_WDQLVL_BURST_CNT_1					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
PHY_WDQLVL_CLK_JITTER_TOLERANCE_1							
R/W							
0h							

Table 14-15291. EMIF_CTLCFG_DENALI_PHY_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WDQLVL_PATT_1	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 1. Bit [0] corresponds to the LFSR data training pattern. Bit [1] corresponds to the CLK data training pattern. Bit [2] corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_WDQLVL_BURST_CNT_1	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_CLK_JITTER_TOLERANCE_1	R/W	0h	Defines the minimum gap requirment for the LE and TE window for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.979 EMIF_CTLCFG_DENALI_PHY_290 Register

1 EMIF_CTLCFG_DENALI_PHY_290 Register (Offset = 4488h) [reset = 0h]

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Table 14-15292. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C488h**

Figure 14-5058. EMIF_CTLCFG_DENALI_PHY_290 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1							
R/W							
0h							

Table 14-15294. EMIF_CTLCFG_DENALI_PHY_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WDQLVL_DQDM_OBS_SELECT_1	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing the DQ target delay setting during write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1	R/W	0h	Defines the target delay jump value when the TE window is found and begin to serch TE window for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.980 EMIF_CTLCFG_DENALI_PHY_291 Register

1 EMIF_CTLCFG_DENALI_PHY_291 Register (Offset = 448Ch) [reset = 0h]

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Table 14-15295. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C48Ch**

Figure 14-5059. EMIF_CTLCFG_DENALI_PHY_291 Name Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_WDQLVL_CLR_PREV_RESULTS_1
NONE							W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_WDQLVL_DM_DLY_STEP_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_DQ_SLV_DELTA_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_PERIODIC_OBS_SELECT_1							
R/W							
0h							

Table 14-15297. EMIF_CTLCFG_DENALI_PHY_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SC_PHY_WDQLVL_CLR_PREV_RESULTS_1	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_WDQLVL_DM_DLY_STEP_1	R/W	0h	The target delay line step for DM training for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_WDQLVL_DQ_SLV_DELTA_1	R/W	0h	The margin for DQ0-7's LE and TE dealy to make sure the DQ bits can work during DM training for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_PERIODIC_OBS_SELECT_1	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.981 EMIF_CTLCFG_DENALI_PHY_292 Register

1 EMIF_CTLCFG_DENALI_PHY_292 Register (Offset = 4490h) [reset = 0h]

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Table 14-15298. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C490h

Figure 14-5060. EMIF_CTLCFG_DENALI_PHY_292 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_WDQLVL_DATADM_MASK_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DATADM_MASK_1							
R/W							
0h							

Table 14-15300. EMIF_CTLCFG_DENALI_PHY_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_WDQLVL_DATADM_MASK_1	R/W	0h	Per-bit mask for write data leveling for slice 1. Set to 1 to mask any bit from the leveling process. Reset Source: ctl_amod_g_rst_n

14.5.1.2.982 EMIF_CTLCFG_DENALI_PHY_293 Register

1 EMIF_CTLCFG_DENALI_PHY_293 Register (Offset = 4494h) [reset = 0h]

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Table 14-15301. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C494h**

Figure 14-5061. EMIF_CTLCFG_DENALI_PHY_293 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT0_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT0_1							
R/W							
0h							

Table 14-15303. EMIF_CTLCFG_DENALI_PHY_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT0_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 3 to 0 written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.983 EMIF_CTLCFG_DENALI_PHY_294 Register

1 EMIF_CTLCFG_DENALI_PHY_294 Register (Offset = 4498h) [reset = 0h]

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Table 14-15304. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C498h

Figure 14-5062. EMIF_CTLCFG_DENALI_PHY_294 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT1_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT1_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT1_1							
R/W							
0h							

Table 14-15306. EMIF_CTLCFG_DENALI_PHY_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT1_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 7 to 4 written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.984 EMIF_CTLCFG_DENALI_PHY_295 Register

1 EMIF_CTLCFG_DENALI_PHY_295 Register (Offset = 449Ch) [reset = 0h]

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Table 14-15307. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C49Ch**

Figure 14-5063. EMIF_CTLCFG_DENALI_PHY_295 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT2_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT2_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT2_1							
R/W							
0h							

Table 14-15309. EMIF_CTLCFG_DENALI_PHY_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT2_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 11 to 8 written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.985 EMIF_CTLCFG_DENALI_PHY_296 Register

1 EMIF_CTLCFG_DENALI_PHY_296 Register (Offset = 44A0h) [reset = 0h]

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Table 14-15310. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4A0h**

Figure 14-5064. EMIF_CTLCFG_DENALI_PHY_296 Name Register

31	30	29	28	27	26	25	24
PHY_USER_PATT3_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_USER_PATT3_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_USER_PATT3_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT3_1							
R/W							
0h							

Table 14-15312. EMIF_CTLCFG_DENALI_PHY_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_USER_PATT3_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 15 to 12 written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.986 EMIF_CTLCFG_DENALI_PHY_297 Register

1 EMIF_CTLCFG_DENALI_PHY_297 Register (Offset = 44A4h) [reset = 0h]

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Table 14-15313. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4A4h**

Figure 14-5065. EMIF_CTLCFG_DENALI_PHY_297 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_MULT_TRAIN_1
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PHY_USER_PATT4_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT4_1							
R/W							
0h							

Table 14-15315. EMIF_CTLCFG_DENALI_PHY_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_MULT_TRAIN_1	R/W	0h	Control for single pass only No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n
15:0	PHY_USER_PATT4_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the DM bit for the 15 to 0 DQ written/read from device. Reset Source: ctl_amod_g_rst_n

14.5.1.2.987 EMIF_CTLCFG_DENALI_PHY_298 Register

1 EMIF_CTLCFG_DENALI_PHY_298 Register (Offset = 44A8h) [reset = 0h]

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Table 14-15316. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4A8h**

Figure 14-5066. EMIF_CTLCFG_DENALI_PHY_298 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_NTP_PERIOD_THRESHOLD_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_NTP_PERIOD_THRESHOLD_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_NTP_EARLY_THRESHOLD_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_NTP_EARLY_THRESHOLD_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15318. EMIF_CTLCFG_DENALI_PHY_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_1	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_EARLY_THRESHOLD_1	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.988 EMIF_CTLCFG_DENALI_PHY_299 Register

1 EMIF_CTLCFG_DENALI_PHY_299 Register (Offset = 44ACh) [reset = 0h]

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Table 14-15319. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C4ACh

Figure 14-5067. EMIF_CTLCFG_DENALI_PHY_299 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_NTP_PERIOD_THRESHOLD_MAX_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_PERIOD_THRESHOLD_MIN_1							
R/W							
0h							

Table 14-15321. EMIF_CTLCFG_DENALI_PHY_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_NTP_PERIOD_THRESHOLD_MAX_1	R/W	0h	Maximum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_NTP_PERIOD_THRESHOLD_MIN_1	R/W	0h	Minimum Threshold that phy_clk_wrdqs_target_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.989 EMIF_CTLCFG_DENALI_PHY_300 Register

1 EMIF_CTLCFG_DENALI_PHY_300 Register (Offset = 44B0h) [reset = 0h]

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Table 14-15322. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 C4B0h**

Figure 14-5068. EMIF_CTLCFG_DENALI_PHY_300 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_FIFO_PTR_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">SC_PHY_MANUAL_CLEAR_1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_CALVL_VREF_DRIVING_SLICE_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-15324. EMIF_CTLCFG_DENALI_PHY_300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_FIFO_PTR_OBS_1	R	0h	Observation register containing read entry FIFO pointers for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	SC_PHY_MANUAL_CLEAR_1	W	0h	Manual reset/clear of internal logic for slice 1. Bit [0] initiates manual setup of the read DQS gate. Bit [1] is reset of read entry FIFO pointers. Bit [2] is reset of controller delay min/max lock values. Bit [3] is manual reset of controller delay unlock counter. Bit [4] is reset of leveling error bit in the leveling status registers. Bit [5] is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_CALVL_VREF_DRIVING_SLICE_1	R/W	0h	Indicates if slice 1 is used to drive the VREF value to the device during CA training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.990 EMIF_CTLCFG_DENALI_PHY_301 Register

1 EMIF_CTLCFG_DENALI_PHY_301 Register (Offset = 44B4h) [reset = 100000h]

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Table 14-15325. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4B4h**

Figure 14-5069. EMIF_CTLCFG_DENALI_PHY_301 Name Register

31	30	29	28	27	26	25	24
PHY_LPBK_RESULT_OBS_1							
R							
100000h							
23	22	21	20	19	18	17	16
PHY_LPBK_RESULT_OBS_1							
R							
100000h							
15	14	13	12	11	10	9	8
PHY_LPBK_RESULT_OBS_1							
R							
100000h							
7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_1							
R							
100000h							

Table 14-15327. EMIF_CTLCFG_DENALI_PHY_301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_LPBK_RESULT_OBS_1	R	100000h	Observation register containing loopback status/results for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.991 EMIF_CTLCFG_DENALI_PHY_302 Register

1 EMIF_CTLCFG_DENALI_PHY_302 Register (Offset = 44B8h) [reset = 0h]

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Table 14-15328. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4B8h**

Figure 14-5070. EMIF_CTLCFG_DENALI_PHY_302 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MASTER_DLY_LOCK_OBS_1		
NONE					R		
0h					0h		
23	22	21	20	19	18	17	16
PHY_MASTER_DLY_LOCK_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_LPBK_ERROR_COUNT_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_LPBK_ERROR_COUNT_OBS_1							
R							
0h							

Table 14-15330. EMIF_CTLCFG_DENALI_PHY_302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_MASTER_DLY_LOCK_OBS_1	R	0h	Observation register containing controller delay results for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_LPBK_ERROR_COUNT_OBS_1	R	0h	Observation register containing total number of loopback error data for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.992 EMIF_CTLCFG_DENALI_PHY_303 Register

1 EMIF_CTLCFG_DENALI_PHY_303 Register (Offset = 44BCh) [reset = 0h]

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Table 14-15331. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4BCh**

Figure 14-5071. EMIF_CTLCFG_DENALI_PHY_303 Name Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_MEAS_DLY_STEP_VALUE_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_1						
NONE	R						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_1						
NONE	R						
0h	0h						

Table 14-15333. EMIF_CTLCFG_DENALI_PHY_303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS DQ rising edge adder target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:16	PHY_MEAS_DLY_STEP_VALUE_1	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with demominator of 512, for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS base target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_RDDQ_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQ target delay encoded values for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.993 EMIF_CTLCFG_DENALI_PHY_304 Register

1 EMIF_CTLCFG_DENALI_PHY_304 Register (Offset = 44C0h) [reset = 0h]

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Table 14-15334. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4C0h**

Figure 14-5072. EMIF_CTLCFG_DENALI_PHY_304 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_1</td></tr>
<tr><td>NONE</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15336. EMIF_CTLCFG_DENALI_PHY_304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write DQS base target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS gate target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS DQ falling edge adder target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.994 EMIF_CTLCFG_DENALI_PHY_305 Register

1 EMIF_CTLCFG_DENALI_PHY_305 Register (Offset = 44C4h) [reset = 0h]

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Table 14-15337. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4C4h**

Figure 14-5073. EMIF_CTLCFG_DENALI_PHY_305 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_WR_SHIFT_OBS_1		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WR_ADDER_SLV_DLY_ENC_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_1							
R							
0h							

Table 14-15339. EMIF_CTLCFG_DENALI_PHY_305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_WR_SHIFT_OBS_1	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write adder target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
7:0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write DQ base target delay encoded value for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.995 EMIF_CTLCFG_DENALI_PHY_306 Register

1 EMIF_CTLCFG_DENALI_PHY_306 Register (Offset = 44C8h) [reset = 0h]

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Table 14-15340. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 C4C8h**

Figure 14-5074. EMIF_CTLCFG_DENALI_PHY_306 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_1	
NONE						R	
0h						0h	
23	22	21	20	19	18	17	16
PHY_WRLVL_HARD1_DELAY_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_1	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_HARD0_DELAY_OBS_1							
R							
0h							

Table 14-15342. EMIF_CTLCFG_DENALI_PHY_306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_HARD1_DELAY_OBS_1	R	0h	Observation register containing write leveling first hard 1 DQS target delay for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_HARD0_DELAY_OBS_1	R	0h	Observation register containing write leveling last hard 0 DQS target delay for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.996 EMIF_CTLCFG_DENALI_PHY_307 Register

1 EMIF_CTLCFG_DENALI_PHY_307 Register (Offset = 44CCh) [reset = 0h]

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Table 14-15343. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4CCh**

Figure 14-5075. EMIF_CTLCFG_DENALI_PHY_307 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_WRLVL_STATUS_OBS_1				
NONE			R				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WRLVL_STATUS_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_STATUS_OBS_1							
R							
0h							

Table 14-15345. EMIF_CTLCFG_DENALI_PHY_307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	PHY_WRLVL_STATUS_OBS_1	R	0h	Observation register containing write leveling status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.997 EMIF_CTLCFG_DENALI_PHY_308 Register

1 EMIF_CTLCFG_DENALI_PHY_308 Register (Offset = 44D0h) [reset = 0h]

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Table 14-15346. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4D0h**

Figure 14-5076. EMIF_CTLCFG_DENALI_PHY_308 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1							
R							
0h							

Table 14-15348. EMIF_CTLCFG_DENALI_PHY_308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing gate sample2 target delay encoded values for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing gate sample1 target delay encoded values for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.998 EMIF_CTLCFG_DENALI_PHY_309 Register

1 EMIF_CTLCFG_DENALI_PHY_309 Register (Offset = 44D4h) [reset = 0h]

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Table 14-15349. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4D4h**

Figure 14-5077. EMIF_CTLCFG_DENALI_PHY_309 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_1					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GTLVL_HARD1_DELAY_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_1					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_HARD0_DELAY_OBS_1							
R							
0h							

Table 14-15351. EMIF_CTLCFG_DENALI_PHY_309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	PHY_GTLVL_HARD1_DELAY_OBS_1	R	0h	Observation register containing gate training last hard 1 DQS target delay for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	PHY_GTLVL_HARD0_DELAY_OBS_1	R	0h	Observation register containing gate training first hard 0 DQS target delay for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.999 EMIF_CTLCFG_DENALI_PHY_310 Register

1 EMIF_CTLCFG_DENALI_PHY_310 Register (Offset = 44D8h) [reset = 0h]

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Table 14-15352. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4D8h**

Figure 14-5078. EMIF_CTLCFG_DENALI_PHY_310 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_GTLVL_STATUS_OBS_1	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
PHY_GTLVL_STATUS_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_GTLVL_STATUS_OBS_1							
R							
0h							

Table 14-15354. EMIF_CTLCFG_DENALI_PHY_310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_GTLVL_STATUS_OBS_1	R	0h	Observation register containing gate training status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1000 EMIF_CTLCFG_DENALI_PHY_311 Register

1 EMIF_CTLCFG_DENALI_PHY_311 Register (Offset = 44DCh) [reset = 0h]

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Table 14-15355. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4DCh**

Figure 14-5079. EMIF_CTLCFG_DENALI_PHY_311 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1							
R							
0h							

Table 14-15357. EMIF_CTLCFG_DENALI_PHY_311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1	R	0h	Observation register containing read leveling data window trailing edge target delay setting for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1	R	0h	Observation register containing read leveling data window leading edge target delay setting for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1001 EMIF_CTLCFG_DENALI_PHY_312 Register

1 EMIF_CTLCFG_DENALI_PHY_312 Register (Offset = 44E0h) [reset = 0h]

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Table 14-15358. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4E0h**

Figure 14-5080. EMIF_CTLCFG_DENALI_PHY_312 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_1	
NONE						R	
0h						0h	

Table 14-15360. EMIF_CTLCFG_DENALI_PHY_312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_1	R	0h	Observation register containing read leveling number of windows found for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1002 EMIF_CTLCFG_DENALI_PHY_313 Register

1 EMIF_CTLCFG_DENALI_PHY_313 Register (Offset = 44E4h) [reset = 0h]

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Table 14-15361. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4E4h**

Figure 14-5081. EMIF_CTLCFG_DENALI_PHY_313 Name Register

31	30	29	28	27	26	25	24
PHY_RDLVL_STATUS_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_RDLVL_STATUS_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_STATUS_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_1							
R							
0h							

Table 14-15363. EMIF_CTLCFG_DENALI_PHY_313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_RDLVL_STATUS_OBS_1	R	0h	Observation register containing read leveling status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1003 EMIF_CTLCFG_DENALI_PHY_314 Register

1 EMIF_CTLCFG_DENALI_PHY_314 Register (Offset = 44E8h) [reset = 7FF0000h]

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Table 14-15364. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4E8h**

Figure 14-5082. EMIF_CTLCFG_DENALI_PHY_314 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_1		
NONE					R		
0h					7FFh		
23	22	21	20	19	18	17	16
PHY_WDQLVL_DQDM_TE_DLY_OBS_1							
R							
7FFh							
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_1		
NONE					R		
0h					0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_LE_DLY_OBS_1							
R							
0h							

Table 14-15366. EMIF_CTLCFG_DENALI_PHY_314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_WDQLVL_DQDM_TE_DLY_OBS_1	R	7FFh	Observation register containing write data leveling data window trailing edge target delay setting for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_LE_DLY_OBS_1	R	0h	Observation register containing write data leveling data window leading edge target delay setting for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1004 EMIF_CTLCFG_DENALI_PHY_315 Register

1 EMIF_CTLCFG_DENALI_PHY_315 Register (Offset = 44ECh) [reset = 0h]

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Table 14-15367. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C4ECh

Figure 14-5083. EMIF_CTLCFG_DENALI_PHY_315 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_STATUS_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_STATUS_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_STATUS_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_1							
R							
0h							

Table 14-15369. EMIF_CTLCFG_DENALI_PHY_315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_STATUS_OBS_1	R	0h	Observation register containing write data leveling status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1005 EMIF_CTLCFG_DENALI_PHY_316 Register

1 EMIF_CTLCFG_DENALI_PHY_316 Register (Offset = 44F0h) [reset = 0h]

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Table 14-15370. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4F0h**

Figure 14-5084. EMIF_CTLCFG_DENALI_PHY_316 Name Register

31	30	29	28	27	26	25	24
PHY_WDQLVL_PERIODIC_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_WDQLVL_PERIODIC_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_WDQLVL_PERIODIC_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_1							
R							
0h							

Table 14-15372. EMIF_CTLCFG_DENALI_PHY_316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_WDQLVL_PERIODIC_OBS_1	R	0h	Observation register containing periodic write data leveling status for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1006 EMIF_CTLCFG_DENALI_PHY_317 Register

1 EMIF_CTLCFG_DENALI_PHY_317 Register (Offset = 44F4h) [reset = 0h]

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Table 14-15373. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4F4h**

Figure 14-5085. EMIF_CTLCFG_DENALI_PHY_317 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_DDL_MODE_1						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_MODE_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DDL_MODE_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_MODE_1							
R/W							
0h							

Table 14-15375. EMIF_CTLCFG_DENALI_PHY_317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	PHY_DDL_MODE_1	R/W	0h	DDL mode for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1007 EMIF_CTLCFG_DENALI_PHY_318 Register

1 EMIF_CTLCFG_DENALI_PHY_318 Register (Offset = 44F8h) [reset = 0h]

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Table 14-15376. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4F8h**

Figure 14-5086. EMIF_CTLCFG_DENALI_PHY_318 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DDL_MASK_1					
NONE		R/W					
0h		0h					

Table 14-15378. EMIF_CTLCFG_DENALI_PHY_318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DDL_MASK_1	R/W	0h	DDL mask for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1008 EMIF_CTLCFG_DENALI_PHY_319 Register

1 EMIF_CTLCFG_DENALI_PHY_319 Register (Offset = 44FCh) [reset = 0h]

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Table 14-15379. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C4FCh**

Figure 14-5087. EMIF_CTLCFG_DENALI_PHY_319 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_1							
R							
0h							

Table 14-15381. EMIF_CTLCFG_DENALI_PHY_319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_OBS_1	R	0h	DDL test observation for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1009 EMIF_CTLCFG_DENALI_PHY_320 Register

1 EMIF_CTLCFG_DENALI_PHY_320 Register (Offset = 4500h) [reset = 0h]

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Table 14-15382. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C500h**

Figure 14-5088. EMIF_CTLCFG_DENALI_PHY_320 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							

Table 14-15384. EMIF_CTLCFG_DENALI_PHY_320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_TEST_MSTR_DLY_OBS_1	R	0h	DDL test observation delays for slice 1 controller DDL. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1010 EMIF_CTLCFG_DENALI_PHY_321 Register

1 EMIF_CTLCFG_DENALI_PHY_321 Register (Offset = 4504h) [reset = 0h]

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Table 14-15385. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C504h**

Figure 14-5089. EMIF_CTLCFG_DENALI_PHY_321 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ0_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_LP4_WDQS_OE_EXTEND_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_TRACK_UPD_THRESHOLD_1							
R/W							
0h							

Table 14-15387. EMIF_CTLCFG_DENALI_PHY_321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ0_1	R/W	0h	RX Calibration codes for DQ0 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LP4_WDQS_OE_EXTEND_1	R/W	0h	LPDDR4 write preamble extension enable for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DDL_TRACK_UPD_THRESHOLD_1	R/W	0h	Specify threshold value for PHY init update tracking for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1011 EMIF_CTLCFG_DENALI_PHY_322 Register

1 EMIF_CTLCFG_DENALI_PHY_322 Register (Offset = 4508h) [reset = 0h]

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Table 14-15388. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C508h**

Figure 14-5090. EMIF_CTLCFG_DENALI_PHY_322 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ2_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ2_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_RX_CAL_DQ1_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_DQ1_1							
R/W							
0h							

Table 14-15390. EMIF_CTLCFG_DENALI_PHY_322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ2_1	R/W	0h	RX Calibration codes for DQ2 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ1_1	R/W	0h	RX Calibration codes for DQ1 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1012 EMIF_CTLCFG_DENALI_PHY_323 Register

1 EMIF_CTLCFG_DENALI_PHY_323 Register (Offset = 450Ch) [reset = 0h]

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Table 14-15391. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C50Ch

Figure 14-5091. EMIF_CTLCFG_DENALI_PHY_323 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ4_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ4_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ3_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ3_1							
R/W							
0h							

Table 14-15393. EMIF_CTLCFG_DENALI_PHY_323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ4_1	R/W	0h	RX Calibration codes for DQ4 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ3_1	R/W	0h	RX Calibration codes for DQ3 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1013 EMIF_CTLCFG_DENALI_PHY_324 Register

1 EMIF_CTLCFG_DENALI_PHY_324 Register (Offset = 4510h) [reset = 0h]

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Table 14-15394. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C510h**

Figure 14-5092. EMIF_CTLCFG_DENALI_PHY_324 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ6_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_DQ6_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQ5_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQ5_1							
R/W							
0h							

Table 14-15396. EMIF_CTLCFG_DENALI_PHY_324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_DQ6_1	R/W	0h	RX Calibration codes for DQ6 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ5_1	R/W	0h	RX Calibration codes for DQ5 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1014 EMIF_CTLCFG_DENALI_PHY_325 Register

1 EMIF_CTLCFG_DENALI_PHY_325 Register (Offset = 4514h) [reset = 0h]

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Table 14-15397. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C514h

Figure 14-5093. EMIF_CTLCFG_DENALI_PHY_325 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_RX_CAL_DQ7_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RX_CAL_DQ7_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15399. EMIF_CTLCFG_DENALI_PHY_325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQ7_1	R/W	0h	RX Calibration codes for DQ7 for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1015 EMIF_CTLCFG_DENALI_PHY_326 Register

1 EMIF_CTLCFG_DENALI_PHY_326 Register (Offset = 4518h) [reset = 0h]

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Table 14-15400. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C518h

Figure 14-5094. EMIF_CTLCFG_DENALI_PHY_326 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_RX_CAL_DM_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_RX_CAL_DM_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_RX_CAL_DM_1							
R/W							
0h							

Table 14-15402. EMIF_CTLCFG_DENALI_PHY_326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_RX_CAL_DM_1	R/W	0h	RX Calibration codes for DM for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1016 EMIF_CTLCFG_DENALI_PHY_327 Register

1 EMIF_CTLCFG_DENALI_PHY_327 Register (Offset = 451Ch) [reset = 0h]

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Table 14-15403. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C51Ch**

Figure 14-5095. EMIF_CTLCFG_DENALI_PHY_327 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_FDBK_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RX_CAL_FDBK_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RX_CAL_DQS_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RX_CAL_DQS_1							
R/W							
0h							

Table 14-15405. EMIF_CTLCFG_DENALI_PHY_327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_RX_CAL_FDBK_1	R/W	0h	RX Calibration codes for FDBK for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	PHY_RX_CAL_DQS_1	R/W	0h	RX Calibration codes for DQS for slice 1. Bits [5:0] contain rx_cal_code_down. Bits [11:6] contain rx_cal_code_up. Bits [17:12] contain rx_cal_code2_down. Bits [23:18] contain rx_cal_code2_up. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1017 EMIF_CTLCFG_DENALI_PHY_328 Register

1 EMIF_CTLCFG_DENALI_PHY_328 Register (Offset = 4520h) [reset = 0h]

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Table 14-15406. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C520h**

Figure 14-5096. EMIF_CTLCFG_DENALI_PHY_328 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_FDBK_PWR_CTRL_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_STATIC_TOG_DISABLE_1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_PAD_RX_BIAS_EN_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_RX_BIAS_EN_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15408. EMIF_CTLCFG_DENALI_PHY_328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_FDBK_PWR_CTRL_1	R/W	0h	Shutoff gate feedback IO to reduce power for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_STATIC_TOG_DISABLE_1	R/W	0h	Control to disable toggle during static activity for slice 1. bit0: Write path delay line disable; bit1: Read path delay line disable; bit2: Read data path disable; bit3: clk_phy disable; bit4: controller delay line disable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_PAD_RX_BIAS_EN_1	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1018 EMIF_CTLCFG_DENALI_PHY_329 Register

1 EMIF_CTLCFG_DENALI_PHY_329 Register (Offset = 4524h) [reset = 0h]

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Table 14-15409. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C524h

Figure 14-5097. EMIF_CTLCFG_DENALI_PHY_329 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_RDPATH_GATE_DISABLE_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_1
NONE							R/W
0h							0h

Table 14-15411. EMIF_CTLCFG_DENALI_PHY_329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_SLICE_PWR_RDC_DISABLE_1	R/W	0h	Data slice power reduction disable for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_1	R/W	0h	Data slice RX_CAL block power reduction disable for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_RDPATH_GATE_DISABLE_1	R/W	0h	Data slice read path power reduction disable for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_SLV_DLY_CTRL_GATE_DISABLE_1	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1019 EMIF_CTLCFG_DENALI_PHY_330 Register

1 EMIF_CTLCFG_DENALI_PHY_330 Register (Offset = 4528h) [reset = 0h]

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Table 14-15412. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C528h**

Figure 14-5098. EMIF_CTLCFG_DENALI_PHY_330 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_DQS_TSEL_ENABLE_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_DQ_TSEL_SELECT_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_DQ_TSEL_SELECT_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_DQ_TSEL_ENABLE_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-15414. EMIF_CTLCFG_DENALI_PHY_330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_DQS_TSEL_ENABLE_1	R/W	0h	Operation type tsel enables for DQS signals for slice 1. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
23:8	PHY_DQ_TSEL_SELECT_1	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_DQ_TSEL_ENABLE_1	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 1. Bit [0] enables tsel_en during read cycles. Bit [1] enables tsel_en during write cycles. Bit [2] enables tsel_en during idle cycles. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1020 EMIF_CTLCFG_DENALI_PHY_331 Register

1 EMIF_CTLCFG_DENALI_PHY_331 Register (Offset = 452Ch) [reset = 0h]

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Table 14-15415. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C52Ch**

Figure 14-5099. EMIF_CTLCFG_DENALI_PHY_331 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_VREF_INITIAL_START_POINT_1						
NONE	R/W						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED						PHY_TWO_CYC_PREAMBLE_1	
NONE						R/W	
0h						0h	

15	14	13	12	11	10	9	8
PHY_DQS_TSEL_SELECT_1							
R/W							
0h							

7	6	5	4	3	2	1	0
PHY_DQS_TSEL_SELECT_1							
R/W							
0h							

Table 14-15417. EMIF_CTLCFG_DENALI_PHY_331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_VREF_INITIAL_START_POINT_1	R/W	0h	Data slice initial VREF training start value for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_TWO_CYC_PREAMBLE_1	R/W	0h	2 cycle preamble support for slice 1. Bit [0] controls the 2 cycle read preamble. Bit [1] controls the 2 cycle write preamble. Set each bit to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_DQS_TSEL_SELECT_1	R/W	0h	Operation type tsel select values for DQS signals for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1021 EMIF_CTLCFG_DENALI_PHY_332 Register

1 EMIF_CTLCFG_DENALI_PHY_332 Register (Offset = 4530h) [reset = 0h]

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Table 14-15418. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C530h**

Figure 14-5100. EMIF_CTLCFG_DENALI_PHY_332 Name Register

31	30	29	28	27	26	25	24
PHY_NTP_WDQ_STEP_SIZE_1							
R/W							
0h							

23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_TRAIN_EN_1
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED						PHY_VREF_TRAINING_CTRL_1	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
RESERVED	PHY_VREF_INITIAL_STOP_POINT_1						
NONE	R/W						
0h	0h						

Table 14-15420. EMIF_CTLCFG_DENALI_PHY_332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_NTP_WDQ_STEP_SIZE_1	R/W	0h	Step size of WR DQ target delay during No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_NTP_TRAIN_EN_1	R/W	0h	Enable for No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_VREF_TRAINING_CTRL_1	R/W	0h	Data slice vref training enable control for slice 1. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_VREF_INITIAL_STOP_POINT_1	R/W	0h	Data slice initial VREF training stop value for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1022 EMIF_CTLCFG_DENALI_PHY_333 Register

1 EMIF_CTLCFG_DENALI_PHY_333 Register (Offset = 4534h) [reset = 0h]

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Table 14-15421. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C534h

Figure 14-5101. EMIF_CTLCFG_DENALI_PHY_333 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_NTP_WDQ_STOP_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_NTP_WDQ_STOP_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_NTP_WDQ_START_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_WDQ_START_1							
R/W							
0h							

Table 14-15423. EMIF_CTLCFG_DENALI_PHY_333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_NTP_WDQ_STOP_1	R/W	0h	End of WR DQ target delay in No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_NTP_WDQ_START_1	R/W	0h	Starting WR DQ target delay in No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1023 EMIF_CTLCFG_DENALI_PHY_334 Register

1 EMIF_CTLCFG_DENALI_PHY_334 Register (Offset = 4538h) [reset = 0h]

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Table 14-15424. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C538h**

Figure 14-5102. EMIF_CTLCFG_DENALI_PHY_334 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_WDQLVL_DVW_MIN_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_WDQLVL_DVW_MIN_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_NTP_WDQ_BIT_EN_1							
R/W							
0h							

Table 14-15426. EMIF_CTLCFG_DENALI_PHY_334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_SW_WDQLVL_DVW_MIN_EN_1	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_WDQLVL_DVW_MIN_1	R/W	0h	Minimum data valid window across DQs and ranks for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_NTP_WDQ_BIT_EN_1	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1024 EMIF_CTLCFG_DENALI_PHY_335 Register

1 EMIF_CTLCFG_DENALI_PHY_335 Register (Offset = 453Ch) [reset = 0h]

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Table 14-15427. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C53Ch

Figure 14-5103. EMIF_CTLCFG_DENALI_PHY_335 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_0_1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_PAD_TX_DCD_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_FAST_LVL_EN_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_WDQLVL_PER_START_OFFSET_1					
NONE		R/W					
0h		0h					

Table 14-15429. EMIF_CTLCFG_DENALI_PHY_335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_0_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_TX_DCD_1	R/W	0h	Controls TX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_FAST_LVL_EN_1	R/W	0h	Enable for fast multi-pattern window search for slice 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WDQLVL_PER_START_OFFSET_1	R/W	0h	Peridic training start point offset for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1025 EMIF_CTLCFG_DENALI_PHY_336 Register

1 EMIF_CTLCFG_DENALI_PHY_336 Register (Offset = 4540h) [reset = 0h]

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Table 14-15430. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C540h**

Figure 14-5104. EMIF_CTLCFG_DENALI_PHY_336 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_RX_DCD_4_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_RX_DCD_3_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_RX_DCD_2_1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_RX_DCD_1_1				
NONE			R/W				
0h			0h				

Table 14-15432. EMIF_CTLCFG_DENALI_PHY_336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_RX_DCD_4_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_3_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_2_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_1_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1026 EMIF_CTLCFG_DENALI_PHY_337 Register

1 EMIF_CTLCFG_DENALI_PHY_337 Register (Offset = 4544h) [reset = 0h]

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Table 14-15433. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C544h

Figure 14-5105. EMIF_CTLCFG_DENALI_PHY_337 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_PAD_DM_RX_DCD_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_PAD_RX_DCD_7_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_RX_DCD_6_1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_RX_DCD_5_1				
NONE			R/W				
0h			0h				

Table 14-15435. EMIF_CTLCFG_DENALI_PHY_337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_PAD_DM_RX_DCD_1	R/W	0h	Controls RX_DCD pin for dm pad for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_PAD_RX_DCD_7_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_RX_DCD_6_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_RX_DCD_5_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1027 EMIF_CTLCFG_DENALI_PHY_338 Register

1 EMIF_CTLCFG_DENALI_PHY_338 Register (Offset = 4548h) [reset = 0h]

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Table 14-15436. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C548h**

Figure 14-5106. EMIF_CTLCFG_DENALI_PHY_338 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PHY_PAD_DSLICE_IO_CFG_1						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_PAD_FDBK_RX_DCD_1				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_PAD_DQS_RX_DCD_1				
NONE			R/W				
0h			0h				

Table 14-15438. EMIF_CTLCFG_DENALI_PHY_338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PHY_PAD_DSLICE_IO_CFG_1	R/W	0h	Controls PCLK/PARK pin for pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_PAD_FDBK_RX_DCD_1	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_PAD_DQS_RX_DCD_1	R/W	0h	Controls RX_DCD pin for dqs pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1028 EMIF_CTLCFG_DENALI_PHY_339 Register

1 EMIF_CTLCFG_DENALI_PHY_339 Register (Offset = 454Ch) [reset = 0h]

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Table 14-15439. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C54Ch

Figure 14-5107. EMIF_CTLCFG_DENALI_PHY_339 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ1_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQ1_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQ0_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQ0_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15441. EMIF_CTLCFG_DENALI_PHY_339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ1_SLAVE_DELAY_1	R/W	0h	Read DQ1 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ0_SLAVE_DELAY_1	R/W	0h	Read DQ0 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1029 EMIF_CTLCFG_DENALI_PHY_340 Register

1 EMIF_CTLCFG_DENALI_PHY_340 Register (Offset = 4550h) [reset = 0h]

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Table 14-15442. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C550h**

Figure 14-5108. EMIF_CTLCFG_DENALI_PHY_340 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ3_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ3_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ2_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ2_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15444. EMIF_CTLCFG_DENALI_PHY_340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ3_SLAVE_DELAY_1	R/W	0h	Read DQ3 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ2_SLAVE_DELAY_1	R/W	0h	Read DQ2 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1030 EMIF_CTLCFG_DENALI_PHY_341 Register

1 EMIF_CTLCFG_DENALI_PHY_341 Register (Offset = 4554h) [reset = 0h]

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Table 14-15445. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C554h**

Figure 14-5109. EMIF_CTLCFG_DENALI_PHY_341 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ5_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ5_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ4_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ4_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15447. EMIF_CTLCFG_DENALI_PHY_341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ5_SLAVE_DELAY_1	R/W	0h	Read DQ5 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ4_SLAVE_DELAY_1	R/W	0h	Read DQ4 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1031 EMIF_CTLCFG_DENALI_PHY_342 Register

1 EMIF_CTLCFG_DENALI_PHY_342 Register (Offset = 4558h) [reset = 0h]

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Table 14-15448. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C558h**

Figure 14-5110. EMIF_CTLCFG_DENALI_PHY_342 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQ7_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQ7_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQ6_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQ6_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15450. EMIF_CTLCFG_DENALI_PHY_342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQ7_SLAVE_DELAY_1	R/W	0h	Read DQ7 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQ6_SLAVE_DELAY_1	R/W	0h	Read DQ6 target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1032 EMIF_CTLCFG_DENALI_PHY_343 Register

1 EMIF_CTLCFG_DENALI_PHY_343 Register (Offset = 455Ch) [reset = 0h]

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Table 14-15451. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C55Ch

Figure 14-5111. EMIF_CTLCFG_DENALI_PHY_343 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_RX_CAL_ALL_DLY_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED					PHY_RX_PCLK_CLK_SEL_1		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDM_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDM_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15453. EMIF_CTLCFG_DENALI_PHY_343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_RX_CAL_ALL_DLY_1	R/W	0h	Defines the number of cycles/half cycles that the rx_cal_all_opad signal should be asserted for. There is a phy_rx_cal_all_dly_X parameter for each of the slices of data sent on the DFI data bus for slice 1. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_RX_PCLK_CLK_SEL_1	R/W	0h	RX_PCLK clock frequency selection for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDM_SLAVE_DELAY_1	R/W	0h	Read DM/DBI target delay setting for slice 1. May be used for data swap. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1033 EMIF_CTLCFG_DENALI_PHY_344 Register

1 EMIF_CTLCFG_DENALI_PHY_344 Register (Offset = 4560h) [reset = 0h]

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Table 14-15454. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C560h**

Figure 14-5112. EMIF_CTLCFG_DENALI_PHY_344 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_OE_TIMING_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQ_TSEL_WR_TIMING_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQ_TSEL_RD_TIMING_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_OE_TIMING_1							
R/W							
0h							

Table 14-15456. EMIF_CTLCFG_DENALI_PHY_344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_OE_TIMING_1	R/W	0h	Start/end timing values for DQS output enable signals for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQ_TSEL_WR_TIMING_1	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQ_TSEL_RD_TIMING_1	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DQ_OE_TIMING_1	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1034 EMIF_CTLCFG_DENALI_PHY_345 Register

1 EMIF_CTLCFG_DENALI_PHY_345 Register (Offset = 4564h) [reset = 0h]

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Table 14-15457. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C564h**

Figure 14-5113. EMIF_CTLCFG_DENALI_PHY_345 Name Register

31	30	29	28	27	26	25	24
PHY_DQS_TSEL_WR_TIMING_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DQS_OE_RD_TIMING_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQS_TSEL_RD_TIMING_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_IO_PAD_DELAY_TIMING_1			
NONE				R/W			
0h				0h			

Table 14-15459. EMIF_CTLCFG_DENALI_PHY_345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_DQS_TSEL_WR_TIMING_1	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_DQS_OE_RD_TIMING_1	R/W	0h	Start/end timing values for DQS read based OE extension for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQS_TSEL_RD_TIMING_1	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_IO_PAD_DELAY_TIMING_1	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1035 EMIF_CTLCFG_DENALI_PHY_346 Register

1 EMIF_CTLCFG_DENALI_PHY_346 Register (Offset = 4568h) [reset = 0h]

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Table 14-15460. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C568h**

Figure 14-5114. EMIF_CTLCFG_DENALI_PHY_346 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_VREF_CTRL_DQ_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_VREF_CTRL_DQ_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_VREF_SETTING_TIME_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_VREF_SETTING_TIME_1							
R/W							
0h							

Table 14-15462. EMIF_CTLCFG_DENALI_PHY_346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_PAD_VREF_CTRL_DQ_1	R/W	0h	Pad VREF control settings for DQ slice 1. Reset Source: ctl_amod_g_rst_n
15:0	PHY_VREF_SETTING_TIME_1	R/W	0h	Number of cycles for vref settle after setting is changed for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1036 EMIF_CTLCFG_DENALI_PHY_347 Register

1 EMIF_CTLCFG_DENALI_PHY_347 Register (Offset = 456Ch) [reset = 0h]

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Table 14-15463. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C56Ch

Figure 14-5115. EMIF_CTLCFG_DENALI_PHY_347 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_IE_MODE_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_RDDATA_EN_IE_DLY_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DQS_IE_TIMING_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DQ_IE_TIMING_1							
R/W							
0h							

Table 14-15465. EMIF_CTLCFG_DENALI_PHY_347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_IE_MODE_1	R/W	0h	Input enable mode bits for slice 1. Bit [0] enables the mode where the input enables are always on; set to 1 to enable. Bit [1] disables the input enable on the DM signal; set to 1 to disable. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_RDDATA_EN_IE_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 1. Reset Source: ctl_amod_g_rst_n
15:8	PHY_DQS_IE_TIMING_1	R/W	0h	Start/end timing values for DQS input enable signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_DQ_IE_TIMING_1	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1037 EMIF_CTLCFG_DENALI_PHY_348 Register

1 EMIF_CTLCFG_DENALI_PHY_348 Register (Offset = 4570h) [reset = 0h]

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Table 14-15466. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C570h**

Figure 14-5116. EMIF_CTLCFG_DENALI_PHY_348 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_WDQLVL_RDDATA_EN_TSEL_DLY_1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_WDQLVL_RDDATA_EN_DLY_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_WDQLVL_IE_ON_1
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_DBI_MODE_1	
NONE						R/W	
0h						0h	

Table 14-15468. EMIF_CTLCFG_DENALI_PHY_348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_WDQLVL_RDDATA_EN_TSEL_DLY_1	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_WDQLVL_RDDATA_EN_DLY_1	R/W	0h	For WR DQ training, the number of cycles that the dfi_rddata_en signal is early for slice 1. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_WDQLVL_IE_ON_1	R/W	0h	IE control, 1 meams IE is always on during WR DQ training for slice 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_DBI_MODE_1	R/W	0h	DBI mode for slice 1. Bit [0] enables return of DBI read data. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1038 EMIF_CTLCFG_DENALI_PHY_349 Register

1 EMIF_CTLCFG_DENALI_PHY_349 Register (Offset = 4574h) [reset = 0h]

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Table 14-15469. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C574h

Figure 14-5117. EMIF_CTLCFG_DENALI_PHY_349 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_SW_MASTER_MODE_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED			PHY_RDDATA_EN_OE_DLY_1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_RDDATA_EN_TSEL_DLY_1				
NONE			R/W				
0h			0h				

Table 14-15471. EMIF_CTLCFG_DENALI_PHY_349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_SW_MASTER_MODE_1	R/W	0h	Controller delay line override settings for slice 1. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_RDDATA_EN_OE_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_RDDATA_EN_TSEL_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1039 EMIF_CTLCFG_DENALI_PHY_350 Register

1 EMIF_CTLCFG_DENALI_PHY_350 Register (Offset = 4578h) [reset = 0h]

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Table 14-15472. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C578h**

Figure 14-5118. EMIF_CTLCFG_DENALI_PHY_350 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_MASTER_DELAY_WAIT_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_MASTER_DELAY_STEP_1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_MASTER_DELAY_START_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_MASTER_DELAY_START_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15474. EMIF_CTLCFG_DENALI_PHY_350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_MASTER_DELAY_WAIT_1	R/W	0h	Wait cycles for controller delay line locking algorithm for slice 1. Bits [3:0] are the cycle wait count after a calibration clock setting change. Bits [7:4] are the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_MASTER_DELAY_STEP_1	R/W	0h	Incremental step size for controller delay line locking algorithm for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_MASTER_DELAY_START_1	R/W	0h	Start value for controller delay line locking algorithm for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1040 EMIF_CTLCFG_DENALI_PHY_351 Register

1 EMIF_CTLCFG_DENALI_PHY_351 Register (Offset = 457Ch) [reset = 0h]

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Table 14-15475. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C57Ch**

Figure 14-5119. EMIF_CTLCFG_DENALI_PHY_351 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WRLVL_DLY_FINE_STEP_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_DLY_STEP_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_RPTR_UPDATE_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_DELAY_HALF_MEASURE_1							
R/W							
0h							

Table 14-15477. EMIF_CTLCFG_DENALI_PHY_351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_WRLVL_DLY_FINE_STEP_1	R/W	0h	DQS target delay fine step size during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_WRLVL_DLY_STEP_1	R/W	0h	DQS target delay step size during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RPTR_UPDATE_1	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_MASTER_DELAY_HALF_MEASURE_1	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle in the data slice controller for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1041 EMIF_CTLCFG_DENALI_PHY_352 Register

1 EMIF_CTLCFG_DENALI_PHY_352 Register (Offset = 4580h) [reset = 0h]

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Table 14-15478. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C580h**

Figure 14-5120. EMIF_CTLCFG_DENALI_PHY_352 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_GTLVL_RESP_WAIT_CNT_1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_GTLVL_DLY_STEP_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_WRLVL_RESP_WAIT_CNT_1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-15480. EMIF_CTLCFG_DENALI_PHY_352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_GTLVL_RESP_WAIT_CNT_1	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 1. The valid range is 0x0 to 0xB. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_GTLVL_DLY_STEP_1	R/W	0h	DQS target delay step size during gate training for slice 1. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_WRLVL_RESP_WAIT_CNT_1	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1042 EMIF_CTLCFG_DENALI_PHY_353 Register

1 EMIF_CTLCFG_DENALI_PHY_353 Register (Offset = 4584h) [reset = 0h]

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Table 14-15481. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C584h**

Figure 14-5121. EMIF_CTLCFG_DENALI_PHY_353 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_GTLVL_FINAL_STEP_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_GTLVL_FINAL_STEP_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_GTLVL_BACK_STEP_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_GTLVL_BACK_STEP_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15483. EMIF_CTLCFG_DENALI_PHY_353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_GTLVL_FINAL_STEP_1	R/W	0h	Final backup step delay used in gate training algorithm for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_BACK_STEP_1	R/W	0h	Interim backup step delay used in gate training algorithm for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1043 EMIF_CTLCFG_DENALI_PHY_354 Register

1 EMIF_CTLCFG_DENALI_PHY_354 Register (Offset = 4588h) [reset = 0h]

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Table 14-15484. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C588h**

Figure 14-5122. EMIF_CTLCFG_DENALI_PHY_354 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_WDQLVL_DM_SEARCH_RANGE_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_WDQLVL_DM_SEARCH_RANGE_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PHY_WDQLVL_DLY_STEP_1							
R/W							
0h							

Table 14-15486. EMIF_CTLCFG_DENALI_PHY_354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_WDQLVL_DM_SEARCH_RANGE_1	R/W	0h	The dm target delay search range for non-lpddr4 DM training for slice 1. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_WDQLVL_QTR_DLY_STEP_1	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 1. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value. Reset Source: ctl_amod_g_rst_n
7:0	PHY_WDQLVL_DLY_STEP_1	R/W	0h	DQ target delay step size during write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1044 EMIF_CTLCFG_DENALI_PHY_355 Register

1 EMIF_CTLCFG_DENALI_PHY_355 Register (Offset = 458Ch) [reset = 0h]

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Table 14-15487. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C58Ch**

Figure 14-5123. EMIF_CTLCFG_DENALI_PHY_355 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_DLY_STEP_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							PHY_TOGGLE_PRE_SUPPORT_1
NONE							R/W
0h							0h

Table 14-15489. EMIF_CTLCFG_DENALI_PHY_355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PHY_RDLVL_DLY_STEP_1	R/W	0h	DQS target delay step size during read leveling for slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_TOGGLE_PRE_SUPPORT_1	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1045 EMIF_CTLCFG_DENALI_PHY_356 Register

1 EMIF_CTLCFG_DENALI_PHY_356 Register (Offset = 4590h) [reset = 0h]

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Table 14-15490. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C590h**

Figure 14-5124. EMIF_CTLCFG_DENALI_PHY_356 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_MAX_EDGE_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_MAX_EDGE_1							
R/W							
0h							

Table 14-15492. EMIF_CTLCFG_DENALI_PHY_356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_MAX_EDGE_1	R/W	0h	The maximun rdlvl target delay search window for read eye training for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1046 EMIF_CTLCFG_DENALI_PHY_357 Register

1 EMIF_CTLCFG_DENALI_PHY_357 Register (Offset = 4594h) [reset = 0h]

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Table 14-15493. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C594h**

Figure 14-5125. EMIF_CTLCFG_DENALI_PHY_357 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_MEAS_DLY_STEP_ENABLE_1</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_WDQ_OSC_DELTA_1</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_WRPATH_GATE_TIMING_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_WRPATH_GATE_DISABLE_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-15495. EMIF_CTLCFG_DENALI_PHY_357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_MEAS_DLY_STEP_ENABLE_1	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 1. Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PHY_WDQ_OSC_DELTA_1	R/W	0h	Target delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRPATH_GATE_TIMING_1	R/W	0h	Write path clock gating timing for slice 1. it means additional clock number to write path clock gate Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRPATH_GATE_DISABLE_1	R/W	0h	Write path clock gating disable for slice 1. [0]: disable pull in wrdata_en; [1]: disable write path clock gating, clock always on Reset Source: ctl_amod_g_rst_n

14.5.1.2.1047 EMIF_CTLCFG_DENALI_PHY_358 Register

1 EMIF_CTLCFG_DENALI_PHY_358 Register (Offset = 4598h) [reset = 0h]

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Table 14-15496. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C598h**

Figure 14-5126. EMIF_CTLCFG_DENALI_PHY_358 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PHY_RDDATA_EN_DLY_1				
NONE			R/W				
0h			0h				

Table 14-15498. EMIF_CTLCFG_DENALI_PHY_358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	PHY_RDDATA_EN_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1048 EMIF_CTLCFG_DENALI_PHY_359 Register

1 EMIF_CTLCFG_DENALI_PHY_359 Register (Offset = 459Ch) [reset = 0h]

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Table 14-15499. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C59Ch**

Figure 14-5127. EMIF_CTLCFG_DENALI_PHY_359 Name Register

31	30	29	28	27	26	25	24
PHY_DQ_DM_SWIZZLE0_1							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DQ_DM_SWIZZLE0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DQ_DM_SWIZZLE0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_1							
R/W							
0h							

Table 14-15501. EMIF_CTLCFG_DENALI_PHY_359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DQ_DM_SWIZZLE0_1	R/W	0h	DQ/DM bit swizzling 0 for slice 1. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DQ0, Bits [7:4] inform the PHY which bit in {DM,DQ} map to DQ1, etc. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1049 EMIF_CTLCFG_DENALI_PHY_360 Register

1 EMIF_CTLCFG_DENALI_PHY_360 Register (Offset = 45A0h) [reset = 0h]

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Table 14-15502. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5A0h**

Figure 14-5128. EMIF_CTLCFG_DENALI_PHY_360 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_DM_SWIZZLE1_1			
NONE				R/W			
0h				0h			

Table 14-15504. EMIF_CTLCFG_DENALI_PHY_360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_DQ_DM_SWIZZLE1_1	R/W	0h	DQ/DM bit swizzling 1 for slice 1. Bits [3:0] inform the PHY which bit in {DM,DQ]} map to DM. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1050 EMIF_CTLCFG_DENALI_PHY_361 Register

1 EMIF_CTLCFG_DENALI_PHY_361 Register (Offset = 45A4h) [reset = 0h]

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Table 14-15505. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5A4h**

Figure 14-5129. EMIF_CTLCFG_DENALI_PHY_361 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CLK_WRDQ1_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CLK_WRDQ0_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15507. EMIF_CTLCFG_DENALI_PHY_361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ1_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ1 for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ0_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ0 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1051 EMIF_CTLCFG_DENALI_PHY_362 Register

1 EMIF_CTLCFG_DENALI_PHY_362 Register (Offset = 45A8h) [reset = 0h]

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Table 14-15508. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5A8h**

Figure 14-5130. EMIF_CTLCFG_DENALI_PHY_362 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WRDQ3_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDQ2_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15510. EMIF_CTLCFG_DENALI_PHY_362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ3_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ3 for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ2_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ2 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1052 EMIF_CTLCFG_DENALI_PHY_363 Register

1 EMIF_CTLCFG_DENALI_PHY_363 Register (Offset = 45ACh) [reset = 0h]

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Table 14-15511. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5ACh**

Figure 14-5131. EMIF_CTLCFG_DENALI_PHY_363 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WRDQ5_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDQ4_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15513. EMIF_CTLCFG_DENALI_PHY_363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ5_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ5 for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ4_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ4 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1053 EMIF_CTLCFG_DENALI_PHY_364 Register

1 EMIF_CTLCFG_DENALI_PHY_364 Register (Offset = 45B0h) [reset = 0h]

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Table 14-15514. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5B0h**

Figure 14-5132. EMIF_CTLCFG_DENALI_PHY_364 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_CLK_WRDQ7_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDQ6_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15516. EMIF_CTLCFG_DENALI_PHY_364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CLK_WRDQ7_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ7 for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDQ6_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQ6 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1054 EMIF_CTLCFG_DENALI_PHY_365 Register

1 EMIF_CTLCFG_DENALI_PHY_365 Register (Offset = 45B4h) [reset = 0h]

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Table 14-15517. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5B4h**

Figure 14-5133. EMIF_CTLCFG_DENALI_PHY_365 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_CLK_WRDQS_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WRDM_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CLK_WRDM_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15519. EMIF_CTLCFG_DENALI_PHY_365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_CLK_WRDQS_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DQS for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CLK_WRDM_SLAVE_DELAY_1	R/W	0h	Write clock target delay setting for DM for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1055 EMIF_CTLCFG_DENALI_PHY_366 Register

1 EMIF_CTLCFG_DENALI_PHY_366 Register (Offset = 45B8h) [reset = 0h]

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Table 14-15520. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5B8h**

Figure 14-5134. EMIF_CTLCFG_DENALI_PHY_366 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_1	
NONE						R/W	
0h						0h	

Table 14-15522. EMIF_CTLCFG_DENALI_PHY_366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ0 for slice 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_WRLVL_THRESHOLD_ADJUST_1	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1056 EMIF_CTLCFG_DENALI_PHY_367 Register

1 EMIF_CTLCFG_DENALI_PHY_367 Register (Offset = 45BCh) [reset = 0h]

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Table 14-15523. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5BCh**

Figure 14-5135. EMIF_CTLCFG_DENALI_PHY_367 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15525. EMIF_CTLCFG_DENALI_PHY_367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ1 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ0 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1057 EMIF_CTLCFG_DENALI_PHY_368 Register

1 EMIF_CTLCFG_DENALI_PHY_368 Register (Offset = 45C0h) [reset = 0h]

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Table 14-15526. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5C0h**

Figure 14-5136. EMIF_CTLCFG_DENALI_PHY_368 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15528. EMIF_CTLCFG_DENALI_PHY_368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ2 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ1 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1058 EMIF_CTLCFG_DENALI_PHY_369 Register

1 EMIF_CTLCFG_DENALI_PHY_369 Register (Offset = 45C4h) [reset = 0h]

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Table 14-15529. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5C4h**

Figure 14-5137. EMIF_CTLCFG_DENALI_PHY_369 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15531. EMIF_CTLCFG_DENALI_PHY_369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ3 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ2 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1059 EMIF_CTLCFG_DENALI_PHY_370 Register

1 EMIF_CTLCFG_DENALI_PHY_370 Register (Offset = 45C8h) [reset = 0h]

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Table 14-15532. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5C8h**

Figure 14-5138. EMIF_CTLCFG_DENALI_PHY_370 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15534. EMIF_CTLCFG_DENALI_PHY_370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ4 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ3 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1060 EMIF_CTLCFG_DENALI_PHY_371 Register

1 EMIF_CTLCFG_DENALI_PHY_371 Register (Offset = 45CCh) [reset = 0h]

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Table 14-15535. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 C5CCh**

Figure 14-5139. EMIF_CTLCFG_DENALI_PHY_371 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15537. EMIF_CTLCFG_DENALI_PHY_371 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ5 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ4 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1061 EMIF_CTLCFG_DENALI_PHY_372 Register

1 EMIF_CTLCFG_DENALI_PHY_372 Register (Offset = 45D0h) [reset = 0h]

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Table 14-15538. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5D0h**

Figure 14-5140. EMIF_CTLCFG_DENALI_PHY_372 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15540. EMIF_CTLCFG_DENALI_PHY_372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ6 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ5 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1062 EMIF_CTLCFG_DENALI_PHY_373 Register

1 EMIF_CTLCFG_DENALI_PHY_373 Register (Offset = 45D4h) [reset = 0h]

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Table 14-15541. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5D4h**

Figure 14-5141. EMIF_CTLCFG_DENALI_PHY_373 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15543. EMIF_CTLCFG_DENALI_PHY_373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DQ7 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ6 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1063 EMIF_CTLCFG_DENALI_PHY_374 Register

1 EMIF_CTLCFG_DENALI_PHY_374 Register (Offset = 45D8h) [reset = 0h]

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Table 14-15544. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5D8h**

Figure 14-5142. EMIF_CTLCFG_DENALI_PHY_374 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_DM_RISE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15546. EMIF_CTLCFG_DENALI_PHY_374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS target delay setting for DM for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DQ7 for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1064 EMIF_CTLCFG_DENALI_PHY_375 Register

1 EMIF_CTLCFG_DENALI_PHY_375 Register (Offset = 45DCh) [reset = 0h]

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Table 14-15547. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5DCh**

Figure 14-5143. EMIF_CTLCFG_DENALI_PHY_375 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_RDDQS_GATE_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDDQS_DM_FALL_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15549. EMIF_CTLCFG_DENALI_PHY_375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_RDDQS_GATE_SLAVE_DELAY_1	R/W	0h	Read DQS target delay setting for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS target delay setting for DM for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1065 EMIF_CTLCFG_DENALI_PHY_376 Register

1 EMIF_CTLCFG_DENALI_PHY_376 Register (Offset = 45E0h) [reset = 0h]

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Table 14-15550. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5E0h**

Figure 14-5144. EMIF_CTLCFG_DENALI_PHY_376 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_WRLVL_DELAY_EARLY_THRESHOLD_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WRITE_PATH_LAT_ADD_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_RDDQS_LATENCY_ADJUST_1			
NONE				R/W			
0h				0h			

Table 14-15552. EMIF_CTLCFG_DENALI_PHY_376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_1	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_WRITE_PATH_LAT_ADD_1	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_RDDQS_LATENCY_ADJUST_1	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1066 *EMIF_CTLCFG_DENALI_PHY_377 Register*

1 EMIF_CTLCFG_DENALI_PHY_377 Register (Offset = 45E4h) [reset = 0h]

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Table 14-15553. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5E4h**

Figure 14-5145. EMIF_CTLCFG_DENALI_PHY_377 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_WRLVL_EARLY_FORCE_ZERO_1
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1							
R/W							
0h							

Table 14-15555. EMIF_CTLCFG_DENALI_PHY_377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_WRLVL_EARLY_FORCE_ZERO_1	R/W	0h	Force the final write level delay value [that meets the early threshold] to 0 for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1067 EMIF_CTLCFG_DENALI_PHY_378 Register

1 EMIF_CTLCFG_DENALI_PHY_378 Register (Offset = 45E8h) [reset = 0h]

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Table 14-15556. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C5E8h

Figure 14-5146. EMIF_CTLCFG_DENALI_PHY_378 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_GTLVL_LAT_ADJ_START_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GTLVL_RDDQS_SLV_DLY_START_1							
R/W							
0h							

Table 14-15558. EMIF_CTLCFG_DENALI_PHY_378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_GTLVL_LAT_ADJ_START_1	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 1. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_GTLVL_RDDQS_SLV_DLY_START_1	R/W	0h	Initial read DQS gate target delay setting during gate training for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1068 EMIF_CTLCFG_DENALI_PHY_379 Register

1 EMIF_CTLCFG_DENALI_PHY_379 Register (Offset = 45ECh) [reset = 0h]

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Table 14-15559. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5ECh**

Figure 14-5147. EMIF_CTLCFG_DENALI_PHY_379 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PASS_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_NTP_WRLAT_START_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_WDQLVL_DQDM_SLV_DLY_START_1							
R/W							
0h							

Table 14-15561. EMIF_CTLCFG_DENALI_PHY_379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_NTP_PASS_1	R/W	0h	Indicates if No-topology training found a passing result for slice 1. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_NTP_WRLAT_START_1	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_WDQLVL_DQDM_SLV_DLY_START_1	R/W	0h	Initial DQ/DM target delay setting during write data leveling for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1069 EMIF_CTLCFG_DENALI_PHY_380 Register

1 EMIF_CTLCFG_DENALI_PHY_380 Register (Offset = 45F0h) [reset = 0h]

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Table 14-15562. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C5F0h

Figure 14-5148. EMIF_CTLCFG_DENALI_PHY_380 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1							
R/W							
0h							

Table 14-15564. EMIF_CTLCFG_DENALI_PHY_380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1	R/W	0h	Read leveling starting value for the DQS/DQ target delay settings for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1070 EMIF_CTLCFG_DENALI_PHY_381 Register

1 EMIF_CTLCFG_DENALI_PHY_381 Register (Offset = 45F4h) [reset = 0h]

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Table 14-15565. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C5F4h**

Figure 14-5149. EMIF_CTLCFG_DENALI_PHY_381 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_DSLICE_PAD_RX_CTLE_SETTING_1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
PHY_DSLICE_PAD_BOOSTPN_SETTING_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DSLICE_PAD_BOOSTPN_SETTING_1							
R/W							
0h							

Table 14-15567. EMIF_CTLCFG_DENALI_PHY_381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PHY_DSLICE_PAD_RX_CTLE_SETTING_1	R/W	0h	Setting for RX ctle P/N of pad for slice 1. Reset Source: ctl_amod_g_rst_n
15:0	PHY_DSLICE_PAD_BOOSTPN_SETTING_1	R/W	0h	Setting for boost P/N of pad for slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1071 EMIF_CTLCFG_DENALI_PHY_512 Register

1 EMIF_CTLCFG_DENALI_PHY_512 Register (Offset = 4800h) [reset = 0h]

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Table 14-15568. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C800h**

Figure 14-5150. EMIF_CTLCFG_DENALI_PHY_512 Name Register

31	30	29	28	27	26	25	24
RESERVED					SC_PHY_ADR_MANUAL_CLEAR_0		
NONE					W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_ADR_CLK_BYPASS_OVERRIDE_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15570. EMIF_CTLCFG_DENALI_PHY_512 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	SC_PHY_ADR_MANUAL_CLEAR_0	W	0h	Manual reset/clear of internal logic for address slice 0. Bit [0] is reset of controller delay min/max lock values. Bit [1] is manual reset of controller delay unlock counter. Bit [2] clears the loopback error/results registers. Set each bit to 1 to reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_CLK_BYPASS_OVERRIDE_0	R/W	0h	Bypass mode override setting for address slice 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0	R/W	0h	Command/Address clock bypass mode target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1072 EMIF_CTLCFG_DENALI_PHY_513 Register

1 EMIF_CTLCFG_DENALI_PHY_513 Register (Offset = 4804h) [reset = 1000h]

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Table 14-15571. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C804h**

Figure 14-5151. EMIF_CTLCFG_DENALI_PHY_513 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_LPBK_RESULT_OBS_0							
R							
1000h							
23	22	21	20	19	18	17	16
PHY_ADR_LPBK_RESULT_OBS_0							
R							
1000h							
15	14	13	12	11	10	9	8
PHY_ADR_LPBK_RESULT_OBS_0							
R							
1000h							
7	6	5	4	3	2	1	0
PHY_ADR_LPBK_RESULT_OBS_0							
R							
1000h							

Table 14-15573. EMIF_CTLCFG_DENALI_PHY_513 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_LPBK_RESULT_OBS_0	R	1000h	Observation register containing loopback status/results for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1073 EMIF_CTLCFG_DENALI_PHY_514 Register

1 EMIF_CTLCFG_DENALI_PHY_514 Register (Offset = 4808h) [reset = 0h]

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Table 14-15574. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C808h**

Figure 14-5152. EMIF_CTLCFG_DENALI_PHY_514 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_MEAS_DLY_STEP_VALUE_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_LPBK_ERROR_COUNT_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LPBK_ERROR_COUNT_OBS_0							
R							
0h							

Table 14-15576. EMIF_CTLCFG_DENALI_PHY_514 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_0	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for address slice 0. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_MEAS_DLY_STEP_VALUE_0	R	0h	Contains the fraction of a cycle in 1 delay element numerator with demominator of 512, for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_ADR_LPBK_ERROR_COUNT_OBS_0	R	0h	Observation register containing total number of loopback error data for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1074 EMIF_CTLCFG_DENALI_PHY_515 Register

1 EMIF_CTLCFG_DENALI_PHY_515 Register (Offset = 480Ch) [reset = 0h]

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Table 14-15577. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C80Ch**

Figure 14-5153. EMIF_CTLCFG_DENALI_PHY_515 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_ADR_ADDER_SLV_DLY_ENC_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="7">PHY_ADR_BASE_SLV_DLY_ENC_OBS_0</td></tr>
<tr><td>NONE</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_MASTER_DLY_LOCK_OBS_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_MASTER_DLY_LOCK_OBS_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15579. EMIF_CTLCFG_DENALI_PHY_515 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing addr target delay for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PHY_ADR_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing base target delay for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DLY_LOCK_OBS_0	R	0h	Observation register containing controller delay results for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1075 EMIF_CTLCFG_DENALI_PHY_516 Register

1 EMIF_CTLCFG_DENALI_PHY_516 Register (Offset = 4810h) [reset = 0h]

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Table 14-15580. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C810h

Figure 14-5154. EMIF_CTLCFG_DENALI_PHY_516 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_TSEL_ENABLE_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_ADR_SNAP_OBS_REGS_0
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_SLV_DLY_ENC_OBS_SELECT_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED					PHY_ADR_SLAVE_LOOP_CNT_UPDATE_0		
NONE					R/W		
0h					0h		

Table 14-15582. EMIF_CTLCFG_DENALI_PHY_516 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_TSEL_ENABLE_0	R/W	0h	Enables tsel_en for address slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_SNAP_OBS_REGS_0	W	0h	Initiates a snapshot of the internal observation registers for address slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_0	R/W	0h	Select value to map the addr bits delay observation registers to the accessible delay observation register for address slice 0. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_ADR_SLAVE_LOOP_CNT_UPDATE_0	R/W	0h	Reserved for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1076 EMIF_CTLCFG_DENALI_PHY_517 Register

1 EMIF_CTLCFG_DENALI_PHY_517 Register (Offset = 4814h) [reset = 100h]

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Table 14-15583. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C814h**

Figure 14-5155. EMIF_CTLCFG_DENALI_PHY_517 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_PWR_RDC_DISABLE_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR_PRBS_PATTERN_MASK_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_ADR_PRBS_PATTERN_START_0						
NONE	R/W						
0h	1h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_ADR_LPBK_CONTROL_0						
NONE	R/W						
0h	0h						

Table 14-15585. EMIF_CTLCFG_DENALI_PHY_517 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_PWR_RDC_DISABLE_0	R/W	0h	Power reduction disable for address slice 0. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR_PRBS_PATTERN_MASK_0	R/W	0h	PRBS7 mask signal for address slice 0. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_ADR_PRBS_PATTERN_START_0	R/W	1h	PRBS7 start pattern for address slice 0. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_ADR_LPBK_CONTROL_0	R/W	0h	Loopback control bits for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1077 EMIF_CTLCFG_DENALI_PHY_518 Register

1 EMIF_CTLCFG_DENALI_PHY_518 Register (Offset = 4818h) [reset = 0h]

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Table 14-15586. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C818h**

Figure 14-5156. EMIF_CTLCFG_DENALI_PHY_518 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_IE_MODE_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_WRADDR_SHIFT_OBS_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_TYPE_0</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_0</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-15588. EMIF_CTLCFG_DENALI_PHY_518 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_IE_MODE_0	R/W	0h	Input enable control for address slice 0. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ADR_WRADDR_SHIFT_OBS_0	R	0h	Observation register containing automatic half cycle and cycle shift values for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_ADR_TYPE_0	R/W	0h	DRAM type for address slice 0. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_0	R/W	0h	Power reduction slv_dly_control block gate disable for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1078 EMIF_CTLCFG_DENALI_PHY_519 Register

1 EMIF_CTLCFG_DENALI_PHY_519 Register (Offset = 481Ch) [reset = 0h]

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Table 14-15589. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C81Ch**

Figure 14-5157. EMIF_CTLCFG_DENALI_PHY_519 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_DDL_MODE_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_MODE_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_MODE_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_MODE_0							
R/W							
0h							

Table 14-15591. EMIF_CTLCFG_DENALI_PHY_519 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:0	PHY_ADR_DDL_MODE_0	R/W	0h	DDL mode for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1079 EMIF_CTLCFG_DENALI_PHY_520 Register

1 EMIF_CTLCFG_DENALI_PHY_520 Register (Offset = 4820h) [reset = 0h]

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Table 14-15592. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C820h**

Figure 14-5158. EMIF_CTLCFG_DENALI_PHY_520 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_ADR_DDL_MASK_0					
NONE		R/W					
0h		0h					

Table 14-15594. EMIF_CTLCFG_DENALI_PHY_520 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_DDL_MASK_0	R/W	0h	DDL mask for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1080 EMIF_CTLCFG_DENALI_PHY_521 Register

1 EMIF_CTLCFG_DENALI_PHY_521 Register (Offset = 4824h) [reset = 0h]

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Table 14-15595. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C824h**

Figure 14-5159. EMIF_CTLCFG_DENALI_PHY_521 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_DDL_TEST_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_TEST_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_OBS_0							
R							
0h							

Table 14-15597. EMIF_CTLCFG_DENALI_PHY_521 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_OBS_0	R	0h	Observation register containing DDL test bits for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1081 EMIF_CTLCFG_DENALI_PHY_522 Register

1 EMIF_CTLCFG_DENALI_PHY_522 Register (Offset = 4828h) [reset = 0h]

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Table 14-15598. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C828h**

Figure 14-5160. EMIF_CTLCFG_DENALI_PHY_522 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0							
R							
0h							

Table 14-15600. EMIF_CTLCFG_DENALI_PHY_522 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0	R	0h	Observation register containing controller DDL bits for address slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1082 EMIF_CTLCFG_DENALI_PHY_523 Register

1 EMIF_CTLCFG_DENALI_PHY_523 Register (Offset = 482Ch) [reset = 0h]

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Table 14-15601. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C82Ch**

Figure 14-5161. EMIF_CTLCFG_DENALI_PHY_523 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_COARSE_DLY_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_COARSE_DLY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_CALVL_START_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_START_0							
R/W							
0h							

Table 14-15603. EMIF_CTLCFG_DENALI_PHY_523 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR_CALVL_COARSE_DLY_0	R/W	0h	Coarse CA training DDL increment value for address slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_START_0	R/W	0h	CA training DDL start value for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1083 EMIF_CTLCFG_DENALI_PHY_524 Register

1 EMIF_CTLCFG_DENALI_PHY_524 Register (Offset = 4830h) [reset = 0h]

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Table 14-15604. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C830h**

Figure 14-5162. EMIF_CTLCFG_DENALI_PHY_524 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_CALVL_QTR_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_QTR_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15606. EMIF_CTLCFG_DENALI_PHY_524 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_QTR_0	R/W	0h	CA training DDL quarter cycle delay value for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1084 EMIF_CTLCFG_DENALI_PHY_525 Register

1 EMIF_CTLCFG_DENALI_PHY_525 Register (Offset = 4834h) [reset = 0h]

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Table 14-15607. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C834h**

Figure 14-5163. EMIF_CTLCFG_DENALI_PHY_525 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_SWIZZLE0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_SWIZZLE0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_SWIZZLE0_0							
R/W							
0h							

Table 14-15609. EMIF_CTLCFG_DENALI_PHY_525 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_ADR_CALVL_SWIZZLE0_0	R/W	0h	CA training RD DQ bit swizzle map 0 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1085 EMIF_CTLCFG_DENALI_PHY_526 Register

1 EMIF_CTLCFG_DENALI_PHY_526 Register (Offset = 4838h) [reset = 0h]

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Table 14-15610. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C838h

Figure 14-5164. EMIF_CTLCFG_DENALI_PHY_526 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_CALVL_RANK_CTRL_0	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_SWIZZLE1_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_SWIZZLE1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_SWIZZLE1_0							
R/W							
0h							

Table 14-15612. EMIF_CTLCFG_DENALI_PHY_526 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_ADR_CALVL_RANK_CTRL_0	R/W	0h	CA training rank aggregation control bits for address slice 0. Reset Source: ctl_amod_g_rst_n
23:0	PHY_ADR_CALVL_SWIZZLE1_0	R/W	0h	CA training RD DQ bit swizzle map 1 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1086 EMIF_CTLCFG_DENALI_PHY_527 Register

1 EMIF_CTLCFG_DENALI_PHY_527 Register (Offset = 483Ch) [reset = 0h]

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Table 14-15613. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C83Ch

Figure 14-5165. EMIF_CTLCFG_DENALI_PHY_527 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_CALVL_PERIODIC_START_OFFSET_0
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_PERIODIC_START_OFFSET_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_ADR_CALVL_RESP_WAIT_CNT_0			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED						PHY_ADR_CALVL_NUM_PATTERNS_0	
NONE						R/W	
0h						0h	

Table 14-15615. EMIF_CTLCFG_DENALI_PHY_527 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_ADR_CALVL_PERIODIC_START_OFFSET_0	R/W	0h	Relative offset to start periodic CALVL from previous result Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_ADR_CALVL_RESP_WAIT_CNT_0	R/W	0h	Number of samples to wait before sampling response during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_CALVL_NUM_PATTERNS_0	R/W	0h	Number of patterns to use during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1087 EMIF_CTLCFG_DENALI_PHY_528 Register

1 EMIF_CTLCFG_DENALI_PHY_528 Register (Offset = 4840h) [reset = 0h]

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Table 14-15616. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C840h**

Figure 14-5166. EMIF_CTLCFG_DENALI_PHY_528 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_OBS_SELECT_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_ADR_CALVL_ERROR_CLR_0
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_ADR_CALVL_DEBUG_CONT_0
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_CALVL_DEBUG_MODE_0
NONE							R/W
0h							0h

Table 14-15618. EMIF_CTLCFG_DENALI_PHY_528 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ADR_CALVL_OBS_SELECT_0	R/W	0h	CA bit lane to observe result from OBS0 during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_CALVL_ERROR_CLR_0	W	0h	Clears the CA training state machine error status for address slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_ADR_CALVL_DEBUG_CONT_0	W	0h	Allows the CA training state machine to advance [when in debug mode] for address slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-15618. EMIF_CTLCFG_DENALI_PHY_528 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_ADR_CALVL_DEBUG_MODE_0	R/W	0h	Enables CA training debug mode for address slice 0. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1088 EMIF_CTLCFG_DENALI_PHY_529 Register

1 EMIF_CTLCFG_DENALI_PHY_529 Register (Offset = 4844h) [reset = 0h]

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Table 14-15619. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C844h**

Figure 14-5167. EMIF_CTLCFG_DENALI_PHY_529 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS0_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS0_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS0_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS0_0							
R							
0h							

Table 14-15621. EMIF_CTLCFG_DENALI_PHY_529 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS0_0	R	0h	Observation register contains lane specific CA training bits for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1089 EMIF_CTLCFG_DENALI_PHY_530 Register

1 EMIF_CTLCFG_DENALI_PHY_530 Register (Offset = 4848h) [reset = 0h]

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Table 14-15622. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C848h**

Figure 14-5168. EMIF_CTLCFG_DENALI_PHY_530 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS1_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS1_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS1_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS1_0							
R							
0h							

Table 14-15624. EMIF_CTLCFG_DENALI_PHY_530 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS1_0	R	0h	Observation register contains general CA training bits for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1090 EMIF_CTLCFG_DENALI_PHY_531 Register

1 EMIF_CTLCFG_DENALI_PHY_531 Register (Offset = 484Ch) [reset = 100h]

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Table 14-15625. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C84Ch**

Figure 14-5169. EMIF_CTLCFG_DENALI_PHY_531 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS2_0							
R							
100h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS2_0							
R							
100h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS2_0							
R							
100h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS2_0							
R							
100h							

Table 14-15627. EMIF_CTLCFG_DENALI_PHY_531 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS2_0	R	100h	Observation register contains periodic CA training bits for slice 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1091 EMIF_CTLCFG_DENALI_PHY_532 Register

1 EMIF_CTLCFG_DENALI_PHY_532 Register (Offset = 4850h) [reset = 0h]

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Table 14-15628. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C850h**

Figure 14-5170. EMIF_CTLCFG_DENALI_PHY_532 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_0_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_0_0							
R/W							
0h							

Table 14-15630. EMIF_CTLCFG_DENALI_PHY_532 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_0_0	R/W	0h	CA training foreground pattern 0 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1092 EMIF_CTLCFG_DENALI_PHY_533 Register

1 EMIF_CTLCFG_DENALI_PHY_533 Register (Offset = 4854h) [reset = 0h]

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Table 14-15631. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C854h**

Figure 14-5171. EMIF_CTLCFG_DENALI_PHY_533 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_0_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_0_0							
R/W							
0h							

Table 14-15633. EMIF_CTLCFG_DENALI_PHY_533 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_0_0	R/W	0h	CA training background pattern 0 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1093 EMIF_CTLCFG_DENALI_PHY_534 Register

1 EMIF_CTLCFG_DENALI_PHY_534 Register (Offset = 4858h) [reset = 0h]

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Table 14-15634. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C858h**

Figure 14-5172. EMIF_CTLCFG_DENALI_PHY_534 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_1_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_1_0							
R/W							
0h							

Table 14-15636. EMIF_CTLCFG_DENALI_PHY_534 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_1_0	R/W	0h	CA training foreground pattern 1 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1094 EMIF_CTLCFG_DENALI_PHY_535 Register

1 EMIF_CTLCFG_DENALI_PHY_535 Register (Offset = 485Ch) [reset = 0h]

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Table 14-15637. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C85Ch**

Figure 14-5173. EMIF_CTLCFG_DENALI_PHY_535 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_1_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_1_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_1_0							
R/W							
0h							

Table 14-15639. EMIF_CTLCFG_DENALI_PHY_535 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_1_0	R/W	0h	CA training background pattern 1 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1095 EMIF_CTLCFG_DENALI_PHY_536 Register

1 EMIF_CTLCFG_DENALI_PHY_536 Register (Offset = 4860h) [reset = 0h]

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Table 14-15640. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C860h**

Figure 14-5174. EMIF_CTLCFG_DENALI_PHY_536 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_FG_2_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_2_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15642. EMIF_CTLCFG_DENALI_PHY_536 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_2_0	R/W	0h	CA training foreground pattern 2 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1096 EMIF_CTLCFG_DENALI_PHY_537 Register

1 EMIF_CTLCFG_DENALI_PHY_537 Register (Offset = 4864h) [reset = 0h]

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Table 14-15643. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C864h**

Figure 14-5175. EMIF_CTLCFG_DENALI_PHY_537 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_2_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_2_0							
R/W							
0h							

Table 14-15645. EMIF_CTLCFG_DENALI_PHY_537 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_2_0	R/W	0h	CA training background pattern 2 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1097 EMIF_CTLCFG_DENALI_PHY_538 Register

1 EMIF_CTLCFG_DENALI_PHY_538 Register (Offset = 4868h) [reset = 0h]

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Table 14-15646. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C868h**

Figure 14-5176. EMIF_CTLCFG_DENALI_PHY_538 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_FG_3_0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_3_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_3_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15648. EMIF_CTLCFG_DENALI_PHY_538 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_3_0	R/W	0h	CA training foreground pattern 3 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1098 EMIF_CTLCFG_DENALI_PHY_539 Register

1 EMIF_CTLCFG_DENALI_PHY_539 Register (Offset = 486Ch) [reset = 0h]

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Table 14-15649. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C86Ch**

Figure 14-5177. EMIF_CTLCFG_DENALI_PHY_539 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_3_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_3_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_3_0							
R/W							
0h							

Table 14-15651. EMIF_CTLCFG_DENALI_PHY_539 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_3_0	R/W	0h	CA training background pattern 3 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1099 EMIF_CTLCFG_DENALI_PHY_540 Register

1 EMIF_CTLCFG_DENALI_PHY_540 Register (Offset = 4870h) [reset = 0h]

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Table 14-15652. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C870h**

Figure 14-5178. EMIF_CTLCFG_DENALI_PHY_540 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_ADDR_SEL_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_ADDR_SEL_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_ADDR_SEL_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_ADDR_SEL_0							
R/W							
0h							

Table 14-15654. EMIF_CTLCFG_DENALI_PHY_540 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_ADR_ADDR_SEL_0	R/W	0h	Selects which DFI address pins connect to which CA pins for LPDDR3/4 for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1100 EMIF_CTLCFG_DENALI_PHY_541 Register

1 EMIF_CTLCFG_DENALI_PHY_541 Register (Offset = 4874h) [reset = 0h]

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Table 14-15655. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C874h

Figure 14-5179. EMIF_CTLCFG_DENALI_PHY_541 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SEG_MASK_0					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_ADR_BIT_MASK_0					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED						PHY_ADR_LP4_BOOT_SLV_DELAY_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PHY_ADR_LP4_BOOT_SLV_DELAY_0							
R/W							
0h							

Table 14-15657. EMIF_CTLCFG_DENALI_PHY_541 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SEG_MASK_0	R/W	0h	Segment mask bit for address slice 0. Set to 1 to indicate that the bit is either CA 4 or CA 9. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_BIT_MASK_0	R/W	0h	Mask bit for address slice 0. Set to 1 to indicate that the bit is used. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_ADR_LP4_BOOT_SLV_DELAY_0	R/W	0h	Address target delay setting during the LPDDR4 boot frequency operation for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1101 EMIF_CTLCFG_DENALI_PHY_542 Register

1 EMIF_CTLCFG_DENALI_PHY_542 Register (Offset = 4878h) [reset = 0h]

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Table 14-15658. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C878h**

Figure 14-5180. EMIF_CTLCFG_DENALI_PHY_542 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SW_TXIO_CTRL_0					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_STATIC_TOG_DISABLE_0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_ADR_CSLVL_TRAIN_MASK_0					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_ADR_CALVL_TRAIN_MASK_0					
NONE		R/W					
0h		0h					

Table 14-15660. EMIF_CTLCFG_DENALI_PHY_542 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SW_TXIO_CTRL_0	R/W	0h	Controls address pad output enable for address slice 0. Set to 1 to disable output enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_STATIC_TOG_DISABLE_0	R/W	0h	Toggle control during static activity for address slice 0. Set bit to dsiable toggling, bit0: Write path delay line, bit1: Read path delay line, bit2: Read data path, bit3: clk_phy, bit4: controller delay line. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_CSLVL_TRAIN_MASK_0	R/W	0h	Mask bit for CS training participation for address slice 0. Set to 1 to indicate that the bit is participating in CS training. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_CALVL_TRAIN_MASK_0	R/W	0h	Mask bit for CA training participation for address slice 0. Set to 1 to indicate that the bit is participating in CA training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1102 EMIF_CTLCFG_DENALI_PHY_543 Register

1 EMIF_CTLCFG_DENALI_PHY_543 Register (Offset = 487Ch) [reset = 0h]

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Table 14-15661. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C87Ch

Figure 14-5181. EMIF_CTLCFG_DENALI_PHY_543 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_ADR_SW_TXPWR_CTRL_0					
NONE		R/W					
0h		0h					

Table 14-15663. EMIF_CTLCFG_DENALI_PHY_543 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_SW_TXPWR_CTRL_0	R/W	0h	Disable address output enables in deep sleep mode for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1103 EMIF_CTLCFG_DENALI_PHY_544 Register

1 EMIF_CTLCFG_DENALI_PHY_544 Register (Offset = 4880h) [reset = 0h]

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Table 14-15664. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C880h**

Figure 14-5182. EMIF_CTLCFG_DENALI_PHY_544 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PAD_ADR_RX_PCLK_CLK_SEL_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_PAD_ADR_IO_CFG_0		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ADR_IO_CFG_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_TSEL_SELECT_0							
R/W							
0h							

Table 14-15666. EMIF_CTLCFG_DENALI_PHY_544 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_PAD_ADR_RX_PCLK_CLK_SEL_0	R/W	0h	Reserved for address slice 0. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_PAD_ADR_IO_CFG_0	R/W	0h	Controls I/O pads for address pad for address slice 0. Bits [10:5] = Park value, bits [4] park override, bits [2:0] clk divider. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_TSEL_SELECT_0	R/W	0h	Tsel select values for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1104 EMIF_CTLCFG_DENALI_PHY_545 Register

1 EMIF_CTLCFG_DENALI_PHY_545 Register (Offset = 4884h) [reset = 0h]

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Table 14-15667. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C884h**

Figure 14-5183. EMIF_CTLCFG_DENALI_PHY_545 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_ADR1_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR0_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR0_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_ADR0_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				

Table 14-15669. EMIF_CTLCFG_DENALI_PHY_545 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_ADR1_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 1 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_ADR0_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 0 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_ADR0_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 0 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1105 EMIF_CTLCFG_DENALI_PHY_546 Register

1 EMIF_CTLCFG_DENALI_PHY_546 Register (Offset = 4888h) [reset = 0h]

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Table 14-15670. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C888h**

Figure 14-5184. EMIF_CTLCFG_DENALI_PHY_546 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADR2_SW_WRADDR_SHIFT_0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR1_CLK_WR_SLAVE_DELAY_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR1_CLK_WR_SLAVE_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15672. EMIF_CTLCFG_DENALI_PHY_546 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR2_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 2 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR1_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 1 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1106 EMIF_CTLCFG_DENALI_PHY_547 Register

1 EMIF_CTLCFG_DENALI_PHY_547 Register (Offset = 488Ch) [reset = 0h]

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Table 14-15673. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C88Ch**

Figure 14-5185. EMIF_CTLCFG_DENALI_PHY_547 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADR3_SW_WRADDR_SHIFT_0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR2_CLK_WR_SLAVE_DELAY_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR2_CLK_WR_SLAVE_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15675. EMIF_CTLCFG_DENALI_PHY_547 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR3_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 3 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR2_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 2 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1107 EMIF_CTLCFG_DENALI_PHY_548 Register

1 EMIF_CTLCFG_DENALI_PHY_548 Register (Offset = 4890h) [reset = 0h]

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Table 14-15676. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C890h**

Figure 14-5186. EMIF_CTLCFG_DENALI_PHY_548 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR4_SW_WRADDR_SHIFT_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR3_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR3_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15678. EMIF_CTLCFG_DENALI_PHY_548 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR4_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 4 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR3_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 3 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1108 EMIF_CTLCFG_DENALI_PHY_549 Register

1 EMIF_CTLCFG_DENALI_PHY_549 Register (Offset = 4894h) [reset = 0h]

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Table 14-15679. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C894h**

Figure 14-5187. EMIF_CTLCFG_DENALI_PHY_549 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADR5_SW_WRADDR_SHIFT_0</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR4_CLK_WR_SLAVE_DELAY_0</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR4_CLK_WR_SLAVE_DELAY_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15681. EMIF_CTLCFG_DENALI_PHY_549 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR5_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 5 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR4_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 4 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1109 EMIF_CTLCFG_DENALI_PHY_550 Register

1 EMIF_CTLCFG_DENALI_PHY_550 Register (Offset = 4898h) [reset = 0h]

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Table 14-15682. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 C898h**

Figure 14-5188. EMIF_CTLCFG_DENALI_PHY_550 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_SW_MASTER_MODE_0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR5_CLK_WR_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR5_CLK_WR_SLAVE_DELAY_0							
R/W							
0h							

Table 14-15684. EMIF_CTLCFG_DENALI_PHY_550 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_SW_MASTER_MODE_0	R/W	0h	Controller delay line override settings for address slice 0. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR5_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 5 target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1110 EMIF_CTLCFG_DENALI_PHY_551 Register

1 EMIF_CTLCFG_DENALI_PHY_551 Register (Offset = 489Ch) [reset = 0h]

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Table 14-15685. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C89Ch**

Figure 14-5189. EMIF_CTLCFG_DENALI_PHY_551 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_MASTER_DELAY_WAIT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_ADR_MASTER_DELAY_STEP_0					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_MASTER_DELAY_START_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DELAY_START_0							
R/W							
0h							

Table 14-15687. EMIF_CTLCFG_DENALI_PHY_551 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_MASTER_DELAY_WAIT_0	R/W	0h	Wait cycles for controller delay line locking algorithm for address slice 0. Bits [3:0] is the cycle wait count after a calibration clock setting change. Bits [7:4] is the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_MASTER_DELAY_STEP_0	R/W	0h	Incremental step size for controller delay line locking algorithm for address slice 0. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DELAY_START_0	R/W	0h	Start value for controller delay line locking algorithm for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1111 EMIF_CTLCFG_DENALI_PHY_552 Register

1 EMIF_CTLCFG_DENALI_PHY_552 Register (Offset = 48A0h) [reset = 0h]

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Table 14-15688. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C8A0h**

Figure 14-5190. EMIF_CTLCFG_DENALI_PHY_552 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_SW_CALVL_DVW_MIN_EN_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_ADR_SW_CALVL_DVW_MIN_0	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_SW_CALVL_DVW_MIN_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_MASTER_DELAY_HALF_MEASURE_0							
R/W							
0h							

Table 14-15690. EMIF_CTLCFG_DENALI_PHY_552 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_SW_CALVL_DVW_MIN_EN_0	R/W	0h	Enables the software override data valid window size during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_ADR_SW_CALVL_DVW_MIN_0	R/W	0h	Sets the software override data valid window size during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_MASTER_DELAY_HALF_MEASURE_0	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle for the controller in address slice 0 Reset Source: ctl_amod_g_rst_n

14.5.1.2.1112 EMIF_CTLCFG_DENALI_PHY_553 Register

1 EMIF_CTLCFG_DENALI_PHY_553 Register (Offset = 48A4h) [reset = 0h]

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Table 14-15691. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 C8A4h**

Figure 14-5191. EMIF_CTLCFG_DENALI_PHY_553 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_DLY_STEP_0			
NONE				R/W			
0h				0h			

Table 14-15693. EMIF_CTLCFG_DENALI_PHY_553 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_DLY_STEP_0	R/W	0h	Sets the delay step size plus 1 during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1113 EMIF_CTLCFG_DENALI_PHY_554 Register

1 EMIF_CTLCFG_DENALI_PHY_554 Register (Offset = 48A8h) [reset = 0h]

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Table 14-15694. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 C8A8h

Figure 14-5192. EMIF_CTLCFG_DENALI_PHY_554 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_ADR_MEAS_DLY_STEP_ENABLE_0
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_CAPTURE_CNT_0			
NONE				R/W			
0h				0h			

Table 14-15696. EMIF_CTLCFG_DENALI_PHY_554 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_ADR_MEAS_DLY_STEP_ENABLE_0	R/W	0h	Enables delay parameter setting using phy_adr_meas_dly_step_value for address slice 0. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each ADDR target delay setting during CA training for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1114 EMIF_CTLCFG_DENALI_PHY_768 Register

1 EMIF_CTLCFG_DENALI_PHY_768 Register (Offset = 4C00h) [reset = 0h]

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Table 14-15697. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC00h

Figure 14-5193. EMIF_CTLCFG_DENALI_PHY_768 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">SC_PHY_ADR_MANUAL_CLEAR_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_CLK_BYPASS_OVERRIDE_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15699. EMIF_CTLCFG_DENALI_PHY_768 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	SC_PHY_ADR_MANUAL_CLEAR_1	W	0h	Manual reset/clear of internal logic for address slice 1. Bit [0] is reset of controller delay min/max lock values. Bit [1] is manual reset of controller delay unlock counter. Bit [2] clears the loopback error/ results registers. Set each bit to 1 to reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_CLK_BYPASS_OVERRIDE_1	R/W	0h	Bypass mode override setting for address slice 1. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_1	R/W	0h	Command/Address clock bypass mode target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1115 EMIF_CTLCFG_DENALI_PHY_769 Register

1 EMIF_CTLCFG_DENALI_PHY_769 Register (Offset = 4C04h) [reset = 1000h]

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Table 14-15700. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC04h**

Figure 14-5194. EMIF_CTLCFG_DENALI_PHY_769 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_LPBK_RESULT_OBS_1							
R							
1000h							
23	22	21	20	19	18	17	16
PHY_ADR_LPBK_RESULT_OBS_1							
R							
1000h							
15	14	13	12	11	10	9	8
PHY_ADR_LPBK_RESULT_OBS_1							
R							
1000h							
7	6	5	4	3	2	1	0
PHY_ADR_LPBK_RESULT_OBS_1							
R							
1000h							

Table 14-15702. EMIF_CTLCFG_DENALI_PHY_769 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_LPBK_RESULT_OBS_1	R	1000h	Observation register containing loopback status/results for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1116 EMIF_CTLCFG_DENALI_PHY_770 Register

1 EMIF_CTLCFG_DENALI_PHY_770 Register (Offset = 4C08h) [reset = 0h]

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Table 14-15703. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC08h**

Figure 14-5195. EMIF_CTLCFG_DENALI_PHY_770 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_MEAS_DLY_STEP_VALUE_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_LPBK_ERROR_COUNT_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_LPBK_ERROR_COUNT_OBS_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15705. EMIF_CTLCFG_DENALI_PHY_770 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_1	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for address slice 1. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_MEAS_DLY_STEP_VALUE_1	R	0h	Contains the fraction of a cycle in 1 delay element numerator with demominator of 512, for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_ADR_LPBK_ERROR_COUNT_OBS_1	R	0h	Observation register containing total number of loopback error data for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1117 EMIF_CTLCFG_DENALI_PHY_771 Register

1 EMIF_CTLCFG_DENALI_PHY_771 Register (Offset = 4C0Ch) [reset = 0h]

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Table 14-15706. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC0Ch

Figure 14-5196. EMIF_CTLCFG_DENALI_PHY_771 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_ADDER_SLV_DLY_ENC_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED	PHY_ADR_BASE_SLV_DLY_ENC_OBS_1						
NONE	R						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_MASTER_DLY_LOCK_OBS_1		
NONE					R		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DLY_LOCK_OBS_1							
R							
0h							

Table 14-15708. EMIF_CTLCFG_DENALI_PHY_771 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing addr target delay for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PHY_ADR_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing base target delay for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DLY_LOCK_OBS_1	R	0h	Observation register containing controller delay results for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1118 EMIF_CTLCFG_DENALI_PHY_772 Register

1 EMIF_CTLCFG_DENALI_PHY_772 Register (Offset = 4C10h) [reset = 0h]

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Table 14-15709. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC10h

Figure 14-5197. EMIF_CTLCFG_DENALI_PHY_772 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_TSEL_ENABLE_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_ADR_SNAP_OBS_REGS_1
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_SLV_DLY_ENC_OBS_SELECT_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED					PHY_ADR_SLAVE_LOOP_CNT_UPDATE_1		
NONE					R/W		
0h					0h		

Table 14-15711. EMIF_CTLCFG_DENALI_PHY_772 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_TSEL_ENABLE_1	R/W	0h	Enables tsel_en for address slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_SNAP_OBS_REGS_1	W	0h	Initiates a snapshot of the internal observation registers for address slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_1	R/W	0h	Select value to map the addr bits delay observation registers to the accessible delay observation register for address slice 1. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_ADR_SLAVE_LOOP_CNT_UPDATE_1	R/W	0h	Reserved for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1119 EMIF_CTLCFG_DENALI_PHY_773 Register

1 EMIF_CTLCFG_DENALI_PHY_773 Register (Offset = 4C14h) [reset = 100h]

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Table 14-15712. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC14h

Figure 14-5198. EMIF_CTLCFG_DENALI_PHY_773 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_PWR_RDC_DISABLE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR_PRBS_PATTERN_MASK_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PHY_ADR_PRBS_PATTERN_START_1						
NONE	R/W						
0h	1h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PHY_ADR_LPBK_CONTROL_1						
NONE	R/W						
0h	0h						

Table 14-15714. EMIF_CTLCFG_DENALI_PHY_773 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_PWR_RDC_DISABLE_1	R/W	0h	Power reduction disable for address slice 1. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR_PRBS_PATTERN_MASK_1	R/W	0h	PRBS7 mask signal for address slice 1. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_ADR_PRBS_PATTERN_START_1	R/W	1h	PRBS7 start pattern for address slice 1. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_ADR_LPBK_CONTROL_1	R/W	0h	Loopback control bits for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1120 EMIF_CTLCFG_DENALI_PHY_774 Register

1 EMIF_CTLCFG_DENALI_PHY_774 Register (Offset = 4C18h) [reset = 0h]

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Table 14-15715. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC18h**

Figure 14-5199. EMIF_CTLCFG_DENALI_PHY_774 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_IE_MODE_1
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR_WRADDR_SHIFT_OBS_1		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADR_TYPE_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_1
NONE							R/W
0h							0h

Table 14-15717. EMIF_CTLCFG_DENALI_PHY_774 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_IE_MODE_1	R/W	0h	Input enable control for address slice 1. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ADR_WRADDR_SHIFT_OBS_1	R	0h	Observation register containing automatic half cycle and cycle shift values for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_ADR_TYPE_1	R/W	0h	DRAM type for address slice 1. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_1	R/W	0h	Power reduction slv_dly_control block gate disable for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1121 EMIF_CTLCFG_DENALI_PHY_775 Register

1 EMIF_CTLCFG_DENALI_PHY_775 Register (Offset = 4C1Ch) [reset = 0h]

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Table 14-15718. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC1Ch**

Figure 14-5200. EMIF_CTLCFG_DENALI_PHY_775 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_DDL_MODE_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_MODE_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_MODE_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_MODE_1							
R/W							
0h							

Table 14-15720. EMIF_CTLCFG_DENALI_PHY_775 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:0	PHY_ADR_DDL_MODE_1	R/W	0h	DDL mode for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1122 EMIF_CTLCFG_DENALI_PHY_776 Register

1 EMIF_CTLCFG_DENALI_PHY_776 Register (Offset = 4C20h) [reset = 0h]

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Table 14-15721. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC20h

Figure 14-5201. EMIF_CTLCFG_DENALI_PHY_776 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_ADR_DDL_MASK_1					
NONE		R/W					
0h		0h					

Table 14-15723. EMIF_CTLCFG_DENALI_PHY_776 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_DDL_MASK_1	R/W	0h	DDL mask for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1123 EMIF_CTLCFG_DENALI_PHY_777 Register

1 EMIF_CTLCFG_DENALI_PHY_777 Register (Offset = 4C24h) [reset = 0h]

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Table 14-15724. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC24h**

Figure 14-5202. EMIF_CTLCFG_DENALI_PHY_777 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_OBS_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_DDL_TEST_OBS_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_TEST_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_OBS_1							
R							
0h							

Table 14-15726. EMIF_CTLCFG_DENALI_PHY_777 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_OBS_1	R	0h	Observation register containing DDL test bits for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1124 EMIF_CTLCFG_DENALI_PHY_778 Register

1 EMIF_CTLCFG_DENALI_PHY_778 Register (Offset = 4C28h) [reset = 0h]

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Table 14-15727. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC28h**

Figure 14-5203. EMIF_CTLCFG_DENALI_PHY_778 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1							
R							
0h							

Table 14-15729. EMIF_CTLCFG_DENALI_PHY_778 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1	R	0h	Observation register containing controller DDL bits for address slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1125 EMIF_CTLCFG_DENALI_PHY_779 Register

1 EMIF_CTLCFG_DENALI_PHY_779 Register (Offset = 4C2Ch) [reset = 0h]

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Table 14-15730. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC2Ch**

Figure 14-5204. EMIF_CTLCFG_DENALI_PHY_779 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_COARSE_DLY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_COARSE_DLY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CALVL_START_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_START_1							
R/W							
0h							

Table 14-15732. EMIF_CTLCFG_DENALI_PHY_779 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR_CALVL_COARSE_DLY_1	R/W	0h	Coarse CA training DDL increment value for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_START_1	R/W	0h	CA training DDL start value for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1126 EMIF_CTLCFG_DENALI_PHY_780 Register

1 EMIF_CTLCFG_DENALI_PHY_780 Register (Offset = 4C30h) [reset = 0h]

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Table 14-15733. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC30h**

Figure 14-5205. EMIF_CTLCFG_DENALI_PHY_780 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR_CALVL_QTR_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_QTR_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15735. EMIF_CTLCFG_DENALI_PHY_780 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_QTR_1	R/W	0h	CA training DDL quarter cycle delay value for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1127 EMIF_CTLCFG_DENALI_PHY_781 Register

1 EMIF_CTLCFG_DENALI_PHY_781 Register (Offset = 4C34h) [reset = 0h]

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Table 14-15736. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC34h

Figure 14-5206. EMIF_CTLCFG_DENALI_PHY_781 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_SWIZZLE0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_SWIZZLE0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_SWIZZLE0_1							
R/W							
0h							

Table 14-15738. EMIF_CTLCFG_DENALI_PHY_781 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_ADR_CALVL_SWIZZLE0_1	R/W	0h	CA training RD DQ bit swizzle map 0 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1128 EMIF_CTLCFG_DENALI_PHY_782 Register

1 EMIF_CTLCFG_DENALI_PHY_782 Register (Offset = 4C38h) [reset = 0h]

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Table 14-15739. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC38h**

Figure 14-5207. EMIF_CTLCFG_DENALI_PHY_782 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_CALVL_RANK_CTRL_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_SWIZZLE1_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_SWIZZLE1_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_SWIZZLE1_1							
R/W							
0h							

Table 14-15741. EMIF_CTLCFG_DENALI_PHY_782 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_ADR_CALVL_RANK_CTRL_1	R/W	0h	CA training rank aggregation control bits for address slice 1. Reset Source: ctl_amod_g_rst_n
23:0	PHY_ADR_CALVL_SWIZZLE1_1	R/W	0h	CA training RD DQ bit swizzle map 1 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1129 EMIF_CTLCFG_DENALI_PHY_783 Register

1 EMIF_CTLCFG_DENALI_PHY_783 Register (Offset = 4C3Ch) [reset = 0h]

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Table 14-15742. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC3Ch**

Figure 14-5208. EMIF_CTLCFG_DENALI_PHY_783 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_CALVL_PERIODIC_START_OFFSET_1
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_PERIODIC_START_OFFSET_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_ADR_CALVL_RESP_WAIT_CNT_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED						PHY_ADR_CALVL_NUM_PATTERNS_1	
NONE						R/W	
0h						0h	

Table 14-15744. EMIF_CTLCFG_DENALI_PHY_783 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_ADR_CALVL_PERIODIC_START_OFFSET_1	R/W	0h	Relative offset to start periodic CALVL from previous result Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_ADR_CALVL_RESP_WAIT_CNT_1	R/W	0h	Number of samples to wait before sampling response during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_CALVL_NUM_PATTERNS_1	R/W	0h	Number of patterns to use during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1130 EMIF_CTLCFG_DENALI_PHY_784 Register

1 EMIF_CTLCFG_DENALI_PHY_784 Register (Offset = 4C40h) [reset = 0h]

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Table 14-15745. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC40h**

Figure 14-5209. EMIF_CTLCFG_DENALI_PHY_784 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_OBS_SELECT_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							SC_PHY_ADR_CALVL_ERROR_CLR_1
NONE							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_ADR_CALVL_DEBUG_CONT_1
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_ADR_CALVL_DEBUG_MODE_1
NONE							R/W
0h							0h

Table 14-15747. EMIF_CTLCFG_DENALI_PHY_784 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ADR_CALVL_OBS_SELECT_1	R/W	0h	CA bit lane to observe result from OBS0 during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_CALVL_ERROR_CLR_1	W	0h	Clears the CA training state machine error status for address slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_ADR_CALVL_DEBUG_CONT_1	W	0h	Allows the CA training state machine to advance [when in debug mode] for address slice 1. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-15747. EMIF_CTLCFG_DENALI_PHY_784 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_ADR_CALVL_DEBUG_MODE_1	R/W	0h	Enables CA training debug mode for address slice 1. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1131 EMIF_CTLCFG_DENALI_PHY_785 Register

1 EMIF_CTLCFG_DENALI_PHY_785 Register (Offset = 4C44h) [reset = 0h]

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Table 14-15748. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC44h**

Figure 14-5210. EMIF_CTLCFG_DENALI_PHY_785 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS0_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS0_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS0_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS0_1							
R							
0h							

Table 14-15750. EMIF_CTLCFG_DENALI_PHY_785 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS0_1	R	0h	Observation register contains lane specific CA training bits for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1132 EMIF_CTLCFG_DENALI_PHY_786 Register

1 EMIF_CTLCFG_DENALI_PHY_786 Register (Offset = 4C48h) [reset = 0h]

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Table 14-15751. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC48h

Figure 14-5211. EMIF_CTLCFG_DENALI_PHY_786 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS1_1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS1_1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS1_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS1_1							
R							
0h							

Table 14-15753. EMIF_CTLCFG_DENALI_PHY_786 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS1_1	R	0h	Observation register contains general CA training bits for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1133 EMIF_CTLCFG_DENALI_PHY_787 Register

1 EMIF_CTLCFG_DENALI_PHY_787 Register (Offset = 4C4Ch) [reset = 100h]

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Table 14-15754. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC4Ch**

Figure 14-5212. EMIF_CTLCFG_DENALI_PHY_787 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_OBS2_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_OBS2_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_OBS2_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_OBS2_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
</table>

Table 14-15756. EMIF_CTLCFG_DENALI_PHY_787 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS2_1	R	100h	Observation register contains periodic CA training bits for slice 1. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1134 EMIF_CTLCFG_DENALI_PHY_788 Register

1 EMIF_CTLCFG_DENALI_PHY_788 Register (Offset = 4C50h) [reset = 0h]

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Table 14-15757. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC50h**

Figure 14-5213. EMIF_CTLCFG_DENALI_PHY_788 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_0_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_0_1							
R/W							
0h							

Table 14-15759. EMIF_CTLCFG_DENALI_PHY_788 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_0_1	R/W	0h	CA training foreground pattern 0 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1135 EMIF_CTLCFG_DENALI_PHY_789 Register

1 EMIF_CTLCFG_DENALI_PHY_789 Register (Offset = 4C54h) [reset = 0h]

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Table 14-15760. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC54h**

Figure 14-5214. EMIF_CTLCFG_DENALI_PHY_789 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_0_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_0_1							
R/W							
0h							

Table 14-15762. EMIF_CTLCFG_DENALI_PHY_789 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_0_1	R/W	0h	CA training background pattern 0 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1136 EMIF_CTLCFG_DENALI_PHY_790 Register

1 EMIF_CTLCFG_DENALI_PHY_790 Register (Offset = 4C58h) [reset = 0h]

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Table 14-15763. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC58h**

Figure 14-5215. EMIF_CTLCFG_DENALI_PHY_790 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_1_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_1_1							
R/W							
0h							

Table 14-15765. EMIF_CTLCFG_DENALI_PHY_790 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_1_1	R/W	0h	CA training foreground pattern 1 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1137 EMIF_CTLCFG_DENALI_PHY_791 Register

1 EMIF_CTLCFG_DENALI_PHY_791 Register (Offset = 4C5Ch) [reset = 0h]

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Table 14-15766. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC5Ch**

Figure 14-5216. EMIF_CTLCFG_DENALI_PHY_791 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_1_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_1_1							
R/W							
0h							

Table 14-15768. EMIF_CTLCFG_DENALI_PHY_791 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_1_1	R/W	0h	CA training background pattern 1 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1138 EMIF_CTLCFG_DENALI_PHY_792 Register

1 EMIF_CTLCFG_DENALI_PHY_792 Register (Offset = 4C60h) [reset = 0h]

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Table 14-15769. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC60h**

Figure 14-5217. EMIF_CTLCFG_DENALI_PHY_792 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_FG_2_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_FG_2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_FG_2_1							
R/W							
0h							

Table 14-15771. EMIF_CTLCFG_DENALI_PHY_792 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_2_1	R/W	0h	CA training foreground pattern 2 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1139 EMIF_CTLCFG_DENALI_PHY_793 Register

1 EMIF_CTLCFG_DENALI_PHY_793 Register (Offset = 4C64h) [reset = 0h]

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Table 14-15772. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC64h**

Figure 14-5218. EMIF_CTLCFG_DENALI_PHY_793 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_2_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_2_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_2_1							
R/W							
0h							

Table 14-15774. EMIF_CTLCFG_DENALI_PHY_793 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_2_1	R/W	0h	CA training background pattern 2 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1140 EMIF_CTLCFG_DENALI_PHY_794 Register

1 EMIF_CTLCFG_DENALI_PHY_794 Register (Offset = 4C68h) [reset = 0h]

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Table 14-15775. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC68h**

Figure 14-5219. EMIF_CTLCFG_DENALI_PHY_794 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_3_1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_3_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_3_1							
R/W							
0h							

Table 14-15777. EMIF_CTLCFG_DENALI_PHY_794 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_3_1	R/W	0h	CA training foreground pattern 3 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1141 EMIF_CTLCFG_DENALI_PHY_795 Register

1 EMIF_CTLCFG_DENALI_PHY_795 Register (Offset = 4C6Ch) [reset = 0h]

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Table 14-15778. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC6Ch**

Figure 14-5220. EMIF_CTLCFG_DENALI_PHY_795 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_3_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_3_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_3_1							
R/W							
0h							

Table 14-15780. EMIF_CTLCFG_DENALI_PHY_795 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_3_1	R/W	0h	CA training background pattern 3 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1142 EMIF_CTLCFG_DENALI_PHY_796 Register

1 EMIF_CTLCFG_DENALI_PHY_796 Register (Offset = 4C70h) [reset = 0h]

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Table 14-15781. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC70h

Figure 14-5221. EMIF_CTLCFG_DENALI_PHY_796 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_ADDR_SEL_1					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PHY_ADR_ADDR_SEL_1							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_ADDR_SEL_1							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_ADDR_SEL_1							
R/W							
0h							

Table 14-15783. EMIF_CTLCFG_DENALI_PHY_796 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_ADR_ADDR_SEL_1	R/W	0h	Selects which DFI address pins connect to which CA pins for LPDDR3/4 for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1143 EMIF_CTLCFG_DENALI_PHY_797 Register

1 EMIF_CTLCFG_DENALI_PHY_797 Register (Offset = 4C74h) [reset = 0h]

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Table 14-15784. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC74h**

Figure 14-5222. EMIF_CTLCFG_DENALI_PHY_797 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SEG_MASK_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_ADR_BIT_MASK_1					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADR_LP4_BOOT_SLV_DELAY_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LP4_BOOT_SLV_DELAY_1							
R/W							
0h							

Table 14-15786. EMIF_CTLCFG_DENALI_PHY_797 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SEG_MASK_1	R/W	0h	Segment mask bit for address slice 1. Set to 1 to indicate that the bit is either CA 4 or CA 9. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_BIT_MASK_1	R/W	0h	Mask bit for address slice 1. Set to 1 to indicate that the bit is used. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_ADR_LP4_BOOT_SLV_DELAY_1	R/W	0h	Address target delay setting during the LPDDR4 boot frequency operation for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1144 EMIF_CTLCFG_DENALI_PHY_798 Register

1 EMIF_CTLCFG_DENALI_PHY_798 Register (Offset = 4C78h) [reset = 0h]

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Table 14-15787. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC78h

Figure 14-5223. EMIF_CTLCFG_DENALI_PHY_798 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SW_TXIO_CTRL_1					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_STATIC_TOG_DISABLE_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_ADR_CSLVL_TRAIN_MASK_1					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_ADR_CALVL_TRAIN_MASK_1					
NONE		R/W					
0h		0h					

Table 14-15789. EMIF_CTLCFG_DENALI_PHY_798 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SW_TXIO_CTRL_1	R/W	0h	Controls address pad output enable for address slice 1. Set to 1 to disable output enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_STATIC_TOG_DISABLE_1	R/W	0h	Toggle control during static activity for address slice 1. Set bit to dsiable toggling, bit0: Write path delay line, bit1: Read path delay line, bit2: Read data path, bit3: clk_phy, bit4: controller delay line. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_CSLVL_TRAIN_MASK_1	R/W	0h	Mask bit for CS training participation for address slice 1. Set to 1 to indicate that the bit is participating in CS training. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_CALVL_TRAIN_MASK_1	R/W	0h	Mask bit for CA training participation for address slice 1. Set to 1 to indicate that the bit is participating in CA training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1145 EMIF_CTLCFG_DENALI_PHY_799 Register

1 EMIF_CTLCFG_DENALI_PHY_799 Register (Offset = 4C7Ch) [reset = 0h]

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Table 14-15790. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC7Ch**

Figure 14-5224. EMIF_CTLCFG_DENALI_PHY_799 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_ADR_SW_TXPWR_CTRL_1					
NONE		R/W					
0h		0h					

Table 14-15792. EMIF_CTLCFG_DENALI_PHY_799 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_SW_TXPWR_CTRL_1	R/W	0h	Disable address output enables in deep sleep mode for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1146 EMIF_CTLCFG_DENALI_PHY_800 Register

1 EMIF_CTLCFG_DENALI_PHY_800 Register (Offset = 4C80h) [reset = 0h]

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Table 14-15793. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC80h**

Figure 14-5225. EMIF_CTLCFG_DENALI_PHY_800 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PAD_ADR_RX_PCLK_CLK_SEL_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_PAD_ADR_IO_CFG_1		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ADR_IO_CFG_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_TSEL_SELECT_1							
R/W							
0h							

Table 14-15795. EMIF_CTLCFG_DENALI_PHY_800 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_PAD_ADR_RX_PCLK_CLK_SEL_1	R/W	0h	Reserved for address slice 1. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_PAD_ADR_IO_CFG_1	R/W	0h	Controls I/O pads for address pad for address slice 1. Bits [10:5] = Park value, bits [4] park override, bits [2:0] clk divider. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_TSEL_SELECT_1	R/W	0h	Tsel select values for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1147 EMIF_CTLCFG_DENALI_PHY_801 Register

1 EMIF_CTLCFG_DENALI_PHY_801 Register (Offset = 4C84h) [reset = 0h]

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Table 14-15796. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC84h**

Figure 14-5226. EMIF_CTLCFG_DENALI_PHY_801 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_ADR1_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR0_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR0_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_ADR0_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				

Table 14-15798. EMIF_CTLCFG_DENALI_PHY_801 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_ADR1_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 1 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_ADR0_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 0 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_ADR0_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 0 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1148 EMIF_CTLCFG_DENALI_PHY_802 Register

1 EMIF_CTLCFG_DENALI_PHY_802 Register (Offset = 4C88h) [reset = 0h]

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Table 14-15799. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC88h**

Figure 14-5227. EMIF_CTLCFG_DENALI_PHY_802 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADR2_SW_WRADDR_SHIFT_1</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR1_CLK_WR_SLAVE_DELAY_1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR1_CLK_WR_SLAVE_DELAY_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15801. EMIF_CTLCFG_DENALI_PHY_802 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR2_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 2 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR1_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 1 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1149 EMIF_CTLCFG_DENALI_PHY_803 Register

1 EMIF_CTLCFG_DENALI_PHY_803 Register (Offset = 4C8Ch) [reset = 0h]

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Table 14-15802. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CC8Ch

Figure 14-5228. EMIF_CTLCFG_DENALI_PHY_803 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR3_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR2_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR2_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15804. EMIF_CTLCFG_DENALI_PHY_803 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR3_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 3 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR2_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 2 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1150 EMIF_CTLCFG_DENALI_PHY_804 Register

1 EMIF_CTLCFG_DENALI_PHY_804 Register (Offset = 4C90h) [reset = 0h]

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Table 14-15805. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC90h**

Figure 14-5229. EMIF_CTLCFG_DENALI_PHY_804 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR4_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR3_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR3_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15807. EMIF_CTLCFG_DENALI_PHY_804 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR4_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 4 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR3_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 3 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1151 EMIF_CTLCFG_DENALI_PHY_805 Register

1 EMIF_CTLCFG_DENALI_PHY_805 Register (Offset = 4C94h) [reset = 0h]

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Table 14-15808. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC94h**

Figure 14-5230. EMIF_CTLCFG_DENALI_PHY_805 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR5_SW_WRADDR_SHIFT_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR4_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR4_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15810. EMIF_CTLCFG_DENALI_PHY_805 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR5_SW_WRADDR_SHIFT_1	R/W	0h	Manual override of CA bit 5 of automatic half_cycle_shift/cycle_shift for address slice 1. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR4_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 4 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1152 EMIF_CTLCFG_DENALI_PHY_806 Register

1 EMIF_CTLCFG_DENALI_PHY_806 Register (Offset = 4C98h) [reset = 0h]

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Table 14-15811. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC98h**

Figure 14-5231. EMIF_CTLCFG_DENALI_PHY_806 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_SW_MASTER_MODE_1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR5_CLK_WR_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR5_CLK_WR_SLAVE_DELAY_1							
R/W							
0h							

Table 14-15813. EMIF_CTLCFG_DENALI_PHY_806 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_SW_MASTER_MODE_1	R/W	0h	Controller delay line override settings for address slice 1. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR5_CLK_WR_SLAVE_DELAY_1	R/W	0h	CA bit 5 target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1153 EMIF_CTLCFG_DENALI_PHY_807 Register

1 EMIF_CTLCFG_DENALI_PHY_807 Register (Offset = 4C9Ch) [reset = 0h]

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Table 14-15814. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CC9Ch**

Figure 14-5232. EMIF_CTLCFG_DENALI_PHY_807 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_MASTER_DELAY_WAIT_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_ADR_MASTER_DELAY_STEP_1					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_MASTER_DELAY_START_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DELAY_START_1							
R/W							
0h							

Table 14-15816. EMIF_CTLCFG_DENALI_PHY_807 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_MASTER_DELAY_WAIT_1	R/W	0h	Wait cycles for controller delay line locking algorithm for address slice 1. Bits [3:0] is the cycle wait count after a calibration clock setting change. Bits [7:4] is the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_MASTER_DELAY_STEP_1	R/W	0h	Incremental step size for controller delay line locking algorithm for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DELAY_START_1	R/W	0h	Start value for controller delay line locking algorithm for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1154 EMIF_CTLCFG_DENALI_PHY_808 Register

1 EMIF_CTLCFG_DENALI_PHY_808 Register (Offset = 4CA0h) [reset = 0h]

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Table 14-15817. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 CCA0h**

Figure 14-5233. EMIF_CTLCFG_DENALI_PHY_808 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_SW_CALVL_DVW_MIN_EN_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_SW_CALVL_DVW_MIN_1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_SW_CALVL_DVW_MIN_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_MASTER_DELAY_HALF_MEASURE_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15819. EMIF_CTLCFG_DENALI_PHY_808 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_SW_CALVL_DVW_MIN_EN_1	R/W	0h	Enables the software override data valid window size during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_ADR_SW_CALVL_DVW_MIN_1	R/W	0h	Sets the software override data valid window size during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_MASTER_DELAY_HALF_MEASURE_1	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle for the controller in address slice 1 Reset Source: ctl_amod_g_rst_n

14.5.1.2.1155 EMIF_CTLCFG_DENALI_PHY_809 Register

1 EMIF_CTLCFG_DENALI_PHY_809 Register (Offset = 4CA4h) [reset = 0h]

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Table 14-15820. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CCA4h

Figure 14-5234. EMIF_CTLCFG_DENALI_PHY_809 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_DLY_STEP_1			
NONE				R/W			
0h				0h			

Table 14-15822. EMIF_CTLCFG_DENALI_PHY_809 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_DLY_STEP_1	R/W	0h	Sets the delay step size plus 1 during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1156 EMIF_CTLCFG_DENALI_PHY_810 Register

1 EMIF_CTLCFG_DENALI_PHY_810 Register (Offset = 4CA8h) [reset = 0h]

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Table 14-15823. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 CCA8h

Figure 14-5235. EMIF_CTLCFG_DENALI_PHY_810 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_ADR_MEAS_DLY_STEP_ENABLE_1
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_CAPTURE_CNT_1			
NONE				R/W			
0h				0h			

Table 14-15825. EMIF_CTLCFG_DENALI_PHY_810 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_ADR_MEAS_DLY_STEP_ENABLE_1	R/W	0h	Enables delay parameter setting using phy_adr_meas_dly_step_value for address slice 1. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each ADDR target delay setting during CA training for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1157 EMIF_CTLCFG_DENALI_PHY_1024 Register

1 EMIF_CTLCFG_DENALI_PHY_1024 Register (Offset = 5000h) [reset = 0h]

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Table 14-15826. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D000h

Figure 14-5236. EMIF_CTLCFG_DENALI_PHY_1024 Name Register

31	30	29	28	27	26	25	24
RESERVED					SC_PHY_ADR_MANUAL_CLEAR_2		
NONE					W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_ADR_CLK_BYPASS_OVERRIDE_2
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_2							
R/W							
0h							

Table 14-15828. EMIF_CTLCFG_DENALI_PHY_1024 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	SC_PHY_ADR_MANUAL_CLEAR_2	W	0h	Manual reset/clear of internal logic for address slice 2. Bit [0] is reset of controller delay min/max lock values. Bit [1] is manual reset of controller delay unlock counter. Bit [2] clears the loopback error/ results registers. Set each bit to 1 to reset. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADR_CLK_BYPASS_OVERRIDE_2	R/W	0h	Bypass mode override setting for address slice 2. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_2	R/W	0h	Command/Address clock bypass mode target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1158 EMIF_CTLCFG_DENALI_PHY_1025 Register

1 EMIF_CTLCFG_DENALI_PHY_1025 Register (Offset = 5004h) [reset = 1000h]

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Table 14-15829. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D004h**

Figure 14-5237. EMIF_CTLCFG_DENALI_PHY_1025 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_LPBK_RESULT_OBS_2							
R							
1000h							
23	22	21	20	19	18	17	16
PHY_ADR_LPBK_RESULT_OBS_2							
R							
1000h							
15	14	13	12	11	10	9	8
PHY_ADR_LPBK_RESULT_OBS_2							
R							
1000h							
7	6	5	4	3	2	1	0
PHY_ADR_LPBK_RESULT_OBS_2							
R							
1000h							

Table 14-15831. EMIF_CTLCFG_DENALI_PHY_1025 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_LPBK_RESULT_OBS_2	R	1000h	Observation register containing loopback status/results for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1159 EMIF_CTLCFG_DENALI_PHY_1026 Register

1 EMIF_CTLCFG_DENALI_PHY_1026 Register (Offset = 5008h) [reset = 0h]

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Table 14-15832. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D008h**

Figure 14-5238. EMIF_CTLCFG_DENALI_PHY_1026 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_2			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_MEAS_DLY_STEP_VALUE_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_LPBK_ERROR_COUNT_OBS_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LPBK_ERROR_COUNT_OBS_2							
R							
0h							

Table 14-15834. EMIF_CTLCFG_DENALI_PHY_1026 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_2	R/W	0h	Select value to map the internal controller delay observation registers to the accessible controller delay observation register for address slice 2. Reset Source: ctl_amod_g_rst_n
23:16	PHY_ADR_MEAS_DLY_STEP_VALUE_2	R	0h	Contains the fraction of a cycle in 1 delay element numerator with demominator of 512, for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_ADR_LPBK_ERROR_COUNT_OBS_2	R	0h	Observation register containing total number of loopback error data for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1160 EMIF_CTLCFG_DENALI_PHY_1027 Register

1 EMIF_CTLCFG_DENALI_PHY_1027 Register (Offset = 500Ch) [reset = 0h]

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Table 14-15835. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D00Ch

Figure 14-5239. EMIF_CTLCFG_DENALI_PHY_1027 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_ADDER_SLV_DLY_ENC_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED	PHY_ADR_BASE_SLV_DLY_ENC_OBS_2						
NONE	R						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_MASTER_DLY_LOCK_OBS_2		
NONE					R		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DLY_LOCK_OBS_2							
R							
0h							

Table 14-15837. EMIF_CTLCFG_DENALI_PHY_1027 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_ADDER_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing addr target delay for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:16	PHY_ADR_BASE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing base target delay for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DLY_LOCK_OBS_2	R	0h	Observation register containing controller delay results for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1161 EMIF_CTLCFG_DENALI_PHY_1028 Register

1 EMIF_CTLCFG_DENALI_PHY_1028 Register (Offset = 5010h) [reset = 0h]

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Table 14-15838. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D010h**

Figure 14-5240. EMIF_CTLCFG_DENALI_PHY_1028 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_TSEL_ENABLE_2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_ADR_SNAP_OBS_REGS_2
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_SLV_DLY_ENC_OBS_SELECT_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED					PHY_ADR_SLAVE_LOOP_CNT_UPDATE_2		
NONE					R/W		
0h					0h		

Table 14-15840. EMIF_CTLCFG_DENALI_PHY_1028 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_TSEL_ENABLE_2	R/W	0h	Enables tsel_en for address slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_SNAP_OBS_REGS_2	W	0h	Initiates a snapshot of the internal observation registers for address slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_2	R/W	0h	Select value to map the addr bits delay observation registers to the accessible delay observation register for address slice 2. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_ADR_SLAVE_LOOP_CNT_UPDATE_2	R/W	0h	Reserved for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1162 EMIF_CTLCFG_DENALI_PHY_1029 Register

1 EMIF_CTLCFG_DENALI_PHY_1029 Register (Offset = 5014h) [reset = 100h]

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Table 14-15841. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D014h**

Figure 14-5241. EMIF_CTLCFG_DENALI_PHY_1029 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_PWR_RDC_DISABLE_2
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR_PRBS_PATTERN_MASK_2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED	PHY_ADR_PRBS_PATTERN_START_2						
NONE	R/W						
0h	1h						
7	6	5	4	3	2	1	0
RESERVED	PHY_ADR_LPBK_CONTROL_2						
NONE	R/W						
0h	0h						

Table 14-15843. EMIF_CTLCFG_DENALI_PHY_1029 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_PWR_RDC_DISABLE_2	R/W	0h	Power reduction disable for address slice 2. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR_PRBS_PATTERN_MASK_2	R/W	0h	PRBS7 mask signal for address slice 2. Reset Source: ctl_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14:8	PHY_ADR_PRBS_PATTERN_START_2	R/W	1h	PRBS7 start pattern for address slice 2. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_ADR_LPBK_CONTROL_2	R/W	0h	Loopback control bits for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1163 EMIF_CTLCFG_DENALI_PHY_1030 Register

1 EMIF_CTLCFG_DENALI_PHY_1030 Register (Offset = 5018h) [reset = 0h]

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Table 14-15844. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D018h**

Figure 14-5242. EMIF_CTLCFG_DENALI_PHY_1030 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_IE_MODE_2
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR_WRADDR_SHIFT_OBS_2		
NONE					R		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADR_TYPE_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_2
NONE							R/W
0h							0h

Table 14-15846. EMIF_CTLCFG_DENALI_PHY_1030 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_IE_MODE_2	R/W	0h	Input enable control for address slice 2. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ADR_WRADDR_SHIFT_OBS_2	R	0h	Observation register containing automatic half cycle and cycle shift values for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_ADR_TYPE_2	R/W	0h	DRAM type for address slice 2. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_2	R/W	0h	Power reduction slv_dly_control block gate disable for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1164 EMIF_CTLCFG_DENALI_PHY_1031 Register

1 EMIF_CTLCFG_DENALI_PHY_1031 Register (Offset = 501Ch) [reset = 0h]

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Table 14-15847. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D01Ch

Figure 14-5243. EMIF_CTLCFG_DENALI_PHY_1031 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_DDL_MODE_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_MODE_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_MODE_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_MODE_2							
R/W							
0h							

Table 14-15849. EMIF_CTLCFG_DENALI_PHY_1031 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:0	PHY_ADR_DDL_MODE_2	R/W	0h	DDL mode for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1165 EMIF_CTLCFG_DENALI_PHY_1032 Register

1 EMIF_CTLCFG_DENALI_PHY_1032 Register (Offset = 5020h) [reset = 0h]

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Table 14-15850. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D020h**

Figure 14-5244. EMIF_CTLCFG_DENALI_PHY_1032 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_ADR_DDL_MASK_2					
NONE		R/W					
0h		0h					

Table 14-15852. EMIF_CTLCFG_DENALI_PHY_1032 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_DDL_MASK_2	R/W	0h	DDL mask for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1166 EMIF_CTLCFG_DENALI_PHY_1033 Register

1 EMIF_CTLCFG_DENALI_PHY_1033 Register (Offset = 5024h) [reset = 0h]

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Table 14-15853. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D024h**

Figure 14-5245. EMIF_CTLCFG_DENALI_PHY_1033 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_OBS_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_DDL_TEST_OBS_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_DDL_TEST_OBS_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_OBS_2							
R							
0h							

Table 14-15855. EMIF_CTLCFG_DENALI_PHY_1033 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_OBS_2	R	0h	Observation register containing DDL test bits for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1167 EMIF_CTLCFG_DENALI_PHY_1034 Register

1 EMIF_CTLCFG_DENALI_PHY_1034 Register (Offset = 5028h) [reset = 0h]

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Table 14-15856. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D028h**

Figure 14-5246. EMIF_CTLCFG_DENALI_PHY_1034 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2							
R							
0h							

Table 14-15858. EMIF_CTLCFG_DENALI_PHY_1034 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2	R	0h	Observation register containing controller DDL bits for address slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1168 EMIF_CTLCFG_DENALI_PHY_1035 Register

1 EMIF_CTLCFG_DENALI_PHY_1035 Register (Offset = 502Ch) [reset = 0h]

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Table 14-15859. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D02Ch**

Figure 14-5247. EMIF_CTLCFG_DENALI_PHY_1035 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_COARSE_DLY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_COARSE_DLY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CALVL_START_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_START_2							
R/W							
0h							

Table 14-15861. EMIF_CTLCFG_DENALI_PHY_1035 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_ADR_CALVL_COARSE_DLY_2	R/W	0h	Coarse CA training DDL increment value for address slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_START_2	R/W	0h	CA training DDL start value for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1169 EMIF_CTLCFG_DENALI_PHY_1036 Register

1 EMIF_CTLCFG_DENALI_PHY_1036 Register (Offset = 5030h) [reset = 0h]

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Table 14-15862. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D030h**

Figure 14-5248. EMIF_CTLCFG_DENALI_PHY_1036 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_CALVL_QTR_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_QTR_2							
R/W							
0h							

Table 14-15864. EMIF_CTLCFG_DENALI_PHY_1036 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_CALVL_QTR_2	R/W	0h	CA training DDL quarter cycle delay value for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1170 EMIF_CTLCFG_DENALI_PHY_1037 Register

1 EMIF_CTLCFG_DENALI_PHY_1037 Register (Offset = 5034h) [reset = 0h]

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Table 14-15865. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D034h

Figure 14-5249. EMIF_CTLCFG_DENALI_PHY_1037 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_SWIZZLE0_2							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_SWIZZLE0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_SWIZZLE0_2							
R/W							
0h							

Table 14-15867. EMIF_CTLCFG_DENALI_PHY_1037 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_ADR_CALVL_SWIZZLE0_2	R/W	0h	CA training RD DQ bit swizzle map 0 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1171 EMIF_CTLCFG_DENALI_PHY_1038 Register

1 EMIF_CTLCFG_DENALI_PHY_1038 Register (Offset = 5038h) [reset = 0h]

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Table 14-15868. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D038h**

Figure 14-5250. EMIF_CTLCFG_DENALI_PHY_1038 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_CALVL_RANK_CTRL_2	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_SWIZZLE1_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_SWIZZLE1_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_SWIZZLE1_2							
R/W							
0h							

Table 14-15870. EMIF_CTLCFG_DENALI_PHY_1038 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_ADR_CALVL_RANK_CTRL_2	R/W	0h	CA training rank aggregation control bits for address slice 2. Reset Source: ctl_amod_g_rst_n
23:0	PHY_ADR_CALVL_SWIZZLE1_2	R/W	0h	CA training RD DQ bit swizzle map 1 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1172 EMIF_CTLCFG_DENALI_PHY_1039 Register

1 EMIF_CTLCFG_DENALI_PHY_1039 Register (Offset = 503Ch) [reset = 0h]

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Table 14-15871. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D03Ch**

Figure 14-5251. EMIF_CTLCFG_DENALI_PHY_1039 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_CALVL_PERIODIC_START_OFFSET_2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_PERIODIC_START_OFFSET_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_RESP_WAIT_CNT_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_CALVL_NUM_PATTERNS_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-15873. EMIF_CTLCFG_DENALI_PHY_1039 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_ADR_CALVL_PERIODIC_START_OFFSET_2	R/W	0h	Relative offset to start periodic CALVL from previous result Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_ADR_CALVL_RESP_WAIT_CNT_2	R/W	0h	Number of samples to wait before sampling response during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADR_CALVL_NUM_PATTERNS_2	R/W	0h	Number of patterns to use during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1173 EMIF_CTLCFG_DENALI_PHY_1040 Register

1 EMIF_CTLCFG_DENALI_PHY_1040 Register (Offset = 5040h) [reset = 0h]

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Table 14-15874. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D040h

Figure 14-5252. EMIF_CTLCFG_DENALI_PHY_1040 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_OBS_SELECT_2		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_ADR_CALVL_ERROR_CLR_2
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_ADR_CALVL_DEBUG_CONT_2
NONE							W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_CALVL_DEBUG_MODE_2
NONE							R/W
0h							0h

Table 14-15876. EMIF_CTLCFG_DENALI_PHY_1040 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ADR_CALVL_OBS_SELECT_2	R/W	0h	CA bit lane to observe result from OBS0 during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	SC_PHY_ADR_CALVL_ERROR_CLR_2	W	0h	Clears the CA training state machine error status for address slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_ADR_CALVL_DEBUG_CONT_2	W	0h	Allows the CA training state machine to advance [when in debug mode] for address slice 2. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-15876. EMIF_CTLCFG_DENALI_PHY_1040 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_ADR_CALVL_DEBUG_MODE_2	R/W	0h	Enables CA training debug mode for address slice 2. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1174 EMIF_CTLCFG_DENALI_PHY_1041 Register

1 EMIF_CTLCFG_DENALI_PHY_1041 Register (Offset = 5044h) [reset = 0h]

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Table 14-15877. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D044h**

Figure 14-5253. EMIF_CTLCFG_DENALI_PHY_1041 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS0_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_CALVL_OBS0_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_OBS0_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_OBS0_2							
R							
0h							

Table 14-15879. EMIF_CTLCFG_DENALI_PHY_1041 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS0_2	R	0h	Observation register contains lane specific CA training bits for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1175 EMIF_CTLCFG_DENALI_PHY_1042 Register

1 EMIF_CTLCFG_DENALI_PHY_1042 Register (Offset = 5048h) [reset = 0h]

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Table 14-15880. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D048h**

Figure 14-5254. EMIF_CTLCFG_DENALI_PHY_1042 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS1_2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS1_2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS1_2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS1_2							
R							
0h							

Table 14-15882. EMIF_CTLCFG_DENALI_PHY_1042 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS1_2	R	0h	Observation register contains general CA training bits for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1176 EMIF_CTLCFG_DENALI_PHY_1043 Register

1 EMIF_CTLCFG_DENALI_PHY_1043 Register (Offset = 504Ch) [reset = 100h]

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Table 14-15883. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D04Ch**

Figure 14-5255. EMIF_CTLCFG_DENALI_PHY_1043 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_CALVL_OBS2_2							
R							
100h							
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_OBS2_2							
R							
100h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_OBS2_2							
R							
100h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS2_2							
R							
100h							

Table 14-15885. EMIF_CTLCFG_DENALI_PHY_1043 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_ADR_CALVL_OBS2_2	R	100h	Observation register contains periodic CA training bits for slice 2. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1177 EMIF_CTLCFG_DENALI_PHY_1044 Register

1 EMIF_CTLCFG_DENALI_PHY_1044 Register (Offset = 5050h) [reset = 0h]

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Table 14-15886. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D050h**

Figure 14-5256. EMIF_CTLCFG_DENALI_PHY_1044 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_FG_0_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_0_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_FG_0_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15888. EMIF_CTLCFG_DENALI_PHY_1044 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_0_2	R/W	0h	CA training foreground pattern 0 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1178 EMIF_CTLCFG_DENALI_PHY_1045 Register

1 EMIF_CTLCFG_DENALI_PHY_1045 Register (Offset = 5054h) [reset = 0h]

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Table 14-15889. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D054h**

Figure 14-5257. EMIF_CTLCFG_DENALI_PHY_1045 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_0_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_0_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_0_2							
R/W							
0h							

Table 14-15891. EMIF_CTLCFG_DENALI_PHY_1045 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_0_2	R/W	0h	CA training background pattern 0 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1179 EMIF_CTLCFG_DENALI_PHY_1046 Register

1 EMIF_CTLCFG_DENALI_PHY_1046 Register (Offset = 5058h) [reset = 0h]

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Table 14-15892. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D058h**

Figure 14-5258. EMIF_CTLCFG_DENALI_PHY_1046 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_FG_1_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_FG_1_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_FG_1_2							
R/W							
0h							

Table 14-15894. EMIF_CTLCFG_DENALI_PHY_1046 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_1_2	R/W	0h	CA training foreground pattern 1 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1180 EMIF_CTLCFG_DENALI_PHY_1047 Register

1 EMIF_CTLCFG_DENALI_PHY_1047 Register (Offset = 505Ch) [reset = 0h]

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Table 14-15895. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D05Ch**

Figure 14-5259. EMIF_CTLCFG_DENALI_PHY_1047 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_ADR_CALVL_BG_1_2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_BG_1_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_CALVL_BG_1_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15897. EMIF_CTLCFG_DENALI_PHY_1047 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_1_2	R/W	0h	CA training background pattern 1 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1181 EMIF_CTLCFG_DENALI_PHY_1048 Register

1 EMIF_CTLCFG_DENALI_PHY_1048 Register (Offset = 5060h) [reset = 0h]

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Table 14-15898. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D060h**

Figure 14-5260. EMIF_CTLCFG_DENALI_PHY_1048 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_2_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_2_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_2_2							
R/W							
0h							

Table 14-15900. EMIF_CTLCFG_DENALI_PHY_1048 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_2_2	R/W	0h	CA training foreground pattern 2 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1182 EMIF_CTLCFG_DENALI_PHY_1049 Register

1 EMIF_CTLCFG_DENALI_PHY_1049 Register (Offset = 5064h) [reset = 0h]

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Table 14-15901. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D064h**

Figure 14-5261. EMIF_CTLCFG_DENALI_PHY_1049 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADR_CALVL_BG_2_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_CALVL_BG_2_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_CALVL_BG_2_2							
R/W							
0h							

Table 14-15903. EMIF_CTLCFG_DENALI_PHY_1049 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_2_2	R/W	0h	CA training background pattern 2 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1183 EMIF_CTLCFG_DENALI_PHY_1050 Register

1 EMIF_CTLCFG_DENALI_PHY_1050 Register (Offset = 5068h) [reset = 0h]

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Table 14-15904. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D068h**

Figure 14-5262. EMIF_CTLCFG_DENALI_PHY_1050 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_FG_3_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_FG_3_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_FG_3_2							
R/W							
0h							

Table 14-15906. EMIF_CTLCFG_DENALI_PHY_1050 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_FG_3_2	R/W	0h	CA training foreground pattern 3 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1184 EMIF_CTLCFG_DENALI_PHY_1051 Register

1 EMIF_CTLCFG_DENALI_PHY_1051 Register (Offset = 506Ch) [reset = 0h]

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Table 14-15907. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D06Ch**

Figure 14-5263. EMIF_CTLCFG_DENALI_PHY_1051 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_CALVL_BG_3_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_BG_3_2							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_BG_3_2							
R/W							
0h							

Table 14-15909. EMIF_CTLCFG_DENALI_PHY_1051 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_ADR_CALVL_BG_3_2	R/W	0h	CA training background pattern 3 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1185 EMIF_CTLCFG_DENALI_PHY_1052 Register

1 EMIF_CTLCFG_DENALI_PHY_1052 Register (Offset = 5070h) [reset = 0h]

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Table 14-15910. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D070h**

Figure 14-5264. EMIF_CTLCFG_DENALI_PHY_1052 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_ADDR_SEL_2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_ADR_ADDR_SEL_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR_ADDR_SEL_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_ADDR_SEL_2							
R/W							
0h							

Table 14-15912. EMIF_CTLCFG_DENALI_PHY_1052 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_ADR_ADDR_SEL_2	R/W	0h	Selects which DFI address pins connect to which CA pins for LPDDR3/4 for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1186 EMIF_CTLCFG_DENALI_PHY_1053 Register

1 EMIF_CTLCFG_DENALI_PHY_1053 Register (Offset = 5074h) [reset = 0h]

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Table 14-15913. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D074h

Figure 14-5265. EMIF_CTLCFG_DENALI_PHY_1053 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SEG_MASK_2					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_ADR_BIT_MASK_2					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_ADR_LP4_BOOT_SLV_DELAY_2	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_LP4_BOOT_SLV_DELAY_2							
R/W							
0h							

Table 14-15915. EMIF_CTLCFG_DENALI_PHY_1053 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SEG_MASK_2	R/W	0h	Segment mask bit for address slice 2. Set to 1 to indicate that the bit is either CA 4 or CA 9. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_BIT_MASK_2	R/W	0h	Mask bit for address slice 2. Set to 1 to indicate that the bit is used. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_ADR_LP4_BOOT_SLV_DELAY_2	R/W	0h	Address target delay setting during the LPDDR4 boot frequency operation for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1187 EMIF_CTLCFG_DENALI_PHY_1054 Register

1 EMIF_CTLCFG_DENALI_PHY_1054 Register (Offset = 5078h) [reset = 0h]

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Table 14-15916. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D078h**

Figure 14-5266. EMIF_CTLCFG_DENALI_PHY_1054 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SW_TXIO_CTRL_2					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_STATIC_TOG_DISABLE_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED		PHY_ADR_CSLVL_TRAIN_MASK_2					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_ADR_CALVL_TRAIN_MASK_2					
NONE		R/W					
0h		0h					

Table 14-15918. EMIF_CTLCFG_DENALI_PHY_1054 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_ADR_SW_TXIO_CTRL_2	R/W	0h	Controls address pad output enable for address slice 2. Set to 1 to disable output enable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_STATIC_TOG_DISABLE_2	R/W	0h	Toggle control during static activity for address slice 2. Set bit to dsiable toggling, bit0: Write path delay line, bit1: Read path delay line, bit2: Read data path, bit3: clk_phy, bit4: controller delay line. Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_ADR_CSLVL_TRAIN_MASK_2	R/W	0h	Mask bit for CS training participation for address slice 2. Set to 1 to indicate that the bit is participating in CS training. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_CALVL_TRAIN_MASK_2	R/W	0h	Mask bit for CA training participation for address slice 2. Set to 1 to indicate that the bit is participating in CA training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1188 EMIF_CTLCFG_DENALI_PHY_1055 Register

1 EMIF_CTLCFG_DENALI_PHY_1055 Register (Offset = 507Ch) [reset = 0h]

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Table 14-15919. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D07Ch**

Figure 14-5267. EMIF_CTLCFG_DENALI_PHY_1055 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_ADR_SW_TXPWR_CTRL_2					
NONE		R/W					
0h		0h					

Table 14-15921. EMIF_CTLCFG_DENALI_PHY_1055 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PHY_ADR_SW_TXPWR_CTRL_2	R/W	0h	Disable address output enables in deep sleep mode for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1189 EMIF_CTLCFG_DENALI_PHY_1056 Register

1 EMIF_CTLCFG_DENALI_PHY_1056 Register (Offset = 5080h) [reset = 0h]

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Table 14-15922. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D080h**

Figure 14-5268. EMIF_CTLCFG_DENALI_PHY_1056 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PAD_ADR_RX_PCLK_CLK_SEL_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_PAD_ADR_IO_CFG_2		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ADR_IO_CFG_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_TSEL_SELECT_2							
R/W							
0h							

Table 14-15924. EMIF_CTLCFG_DENALI_PHY_1056 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_PAD_ADR_RX_PCLK_CLK_SEL_2	R/W	0h	Reserved for address slice 2. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_PAD_ADR_IO_CFG_2	R/W	0h	Controls I/O pads for address pad for address slice 2. Bits [10:5] = Park value, bits [4] park override, bits [2:0] clk divider. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_TSEL_SELECT_2	R/W	0h	Tsel select values for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1190 EMIF_CTLCFG_DENALI_PHY_1057 Register

1 EMIF_CTLCFG_DENALI_PHY_1057 Register (Offset = 5084h) [reset = 0h]

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Table 14-15925. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D084h**

Figure 14-5269. EMIF_CTLCFG_DENALI_PHY_1057 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_ADR1_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ADR0_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_ADR0_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_ADR0_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				

Table 14-15927. EMIF_CTLCFG_DENALI_PHY_1057 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_ADR1_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 1 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:8	PHY_ADR0_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 0 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_ADR0_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 0 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1191 EMIF_CTLCFG_DENALI_PHY_1058 Register

1 EMIF_CTLCFG_DENALI_PHY_1058 Register (Offset = 5088h) [reset = 0h]

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Table 14-15928. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D088h**

Figure 14-5270. EMIF_CTLCFG_DENALI_PHY_1058 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR2_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR1_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR1_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							

Table 14-15930. EMIF_CTLCFG_DENALI_PHY_1058 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR2_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 2 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR1_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 1 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1192 EMIF_CTLCFG_DENALI_PHY_1059 Register

1 EMIF_CTLCFG_DENALI_PHY_1059 Register (Offset = 508Ch) [reset = 0h]

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Table 14-15931. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D08Ch**

Figure 14-5271. EMIF_CTLCFG_DENALI_PHY_1059 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADR3_SW_WRADDR_SHIFT_2</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_ADR2_CLK_WR_SLAVE_DELAY_2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR2_CLK_WR_SLAVE_DELAY_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15933. EMIF_CTLCFG_DENALI_PHY_1059 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR3_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 3 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR2_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 2 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1193 EMIF_CTLCFG_DENALI_PHY_1060 Register

1 EMIF_CTLCFG_DENALI_PHY_1060 Register (Offset = 5090h) [reset = 0h]

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Table 14-15934. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D090h

Figure 14-5272. EMIF_CTLCFG_DENALI_PHY_1060 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR4_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR3_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR3_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							

Table 14-15936. EMIF_CTLCFG_DENALI_PHY_1060 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR4_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 4 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR3_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 3 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1194 EMIF_CTLCFG_DENALI_PHY_1061 Register

1 EMIF_CTLCFG_DENALI_PHY_1061 Register (Offset = 5094h) [reset = 0h]

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Table 14-15937. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D094h

Figure 14-5273. EMIF_CTLCFG_DENALI_PHY_1061 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_ADR5_SW_WRADDR_SHIFT_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR4_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR4_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							

Table 14-15939. EMIF_CTLCFG_DENALI_PHY_1061 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_ADR5_SW_WRADDR_SHIFT_2	R/W	0h	Manual override of CA bit 5 of automatic half_cycle_shift/cycle_shift for address slice 2. Bit [0] enables override of half_cycle_shift. Bit [1] is the half_cycle_shift value. Bit [2] enables override of cycle shift. Bits [4:3] is the cycle_shift value. For bits [4:3], clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR4_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 4 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1195 EMIF_CTLCFG_DENALI_PHY_1062 Register

1 EMIF_CTLCFG_DENALI_PHY_1062 Register (Offset = 5098h) [reset = 0h]

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Table 14-15940. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D098h

Figure 14-5274. EMIF_CTLCFG_DENALI_PHY_1062 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_SW_MASTER_MODE_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR5_CLK_WR_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_ADR5_CLK_WR_SLAVE_DELAY_2							
R/W							
0h							

Table 14-15942. EMIF_CTLCFG_DENALI_PHY_1062 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADR_SW_MASTER_MODE_2	R/W	0h	Controller delay line override settings for address slice 2. Bit [0] enables software half clock mode. Bit [1] is the software half clock mode value. Bit [2] enables software bypass mode. Bit [3] is the software bypass mode value. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR5_CLK_WR_SLAVE_DELAY_2	R/W	0h	CA bit 5 target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1196 EMIF_CTLCFG_DENALI_PHY_1063 Register

1 EMIF_CTLCFG_DENALI_PHY_1063 Register (Offset = 509Ch) [reset = 0h]

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Table 14-15943. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D09Ch

Figure 14-5275. EMIF_CTLCFG_DENALI_PHY_1063 Name Register

31	30	29	28	27	26	25	24
PHY_ADR_MASTER_DELAY_WAIT_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_ADR_MASTER_DELAY_STEP_2					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_ADR_MASTER_DELAY_START_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADR_MASTER_DELAY_START_2							
R/W							
0h							

Table 14-15945. EMIF_CTLCFG_DENALI_PHY_1063 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_ADR_MASTER_DELAY_WAIT_2	R/W	0h	Wait cycles for controller delay line locking algorithm for address slice 2. Bits [3:0] is the cycle wait count after a calibration clock setting change. Bits [7:4] is the cycle wait count after a controller delay setting change. Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_ADR_MASTER_DELAY_STEP_2	R/W	0h	Incremental step size for controller delay line locking algorithm for address slice 2. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_ADR_MASTER_DELAY_START_2	R/W	0h	Start value for controller delay line locking algorithm for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1197 EMIF_CTLCFG_DENALI_PHY_1064 Register

1 EMIF_CTLCFG_DENALI_PHY_1064 Register (Offset = 50A0h) [reset = 0h]

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Table 14-15946. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D0A0h**

Figure 14-5276. EMIF_CTLCFG_DENALI_PHY_1064 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADR_SW_CALVL_DVW_MIN_EN_2</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADR_SW_CALVL_DVW_MIN_2</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_ADR_SW_CALVL_DVW_MIN_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADR_MASTER_DELAY_HALF_MEASURE_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15948. EMIF_CTLCFG_DENALI_PHY_1064 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_ADR_SW_CALVL_DVW_MIN_EN_2	R/W	0h	Enables the software override data valid window size during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:8	PHY_ADR_SW_CALVL_DVW_MIN_2	R/W	0h	Sets the software override data valid window size during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADR_MASTER_DELAY_HALF_MEASURE_2	R/W	0h	Defines the number of delay line elements to be considered in determing whether to lock to a half clock cycle for the controller in address slice 2 Reset Source: ctl_amod_g_rst_n

14.5.1.2.1198 EMIF_CTLCFG_DENALI_PHY_1065 Register

1 EMIF_CTLCFG_DENALI_PHY_1065 Register (Offset = 50A4h) [reset = 0h]

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Table 14-15949. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D0A4h**

Figure 14-5277. EMIF_CTLCFG_DENALI_PHY_1065 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_DLY_STEP_2			
NONE				R/W			
0h				0h			

Table 14-15951. EMIF_CTLCFG_DENALI_PHY_1065 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_DLY_STEP_2	R/W	0h	Sets the delay step size plus 1 during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1199 EMIF_CTLCFG_DENALI_PHY_1066 Register

1 EMIF_CTLCFG_DENALI_PHY_1066 Register (Offset = 50A8h) [reset = 0h]

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Table 14-15952. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D0A8h**

Figure 14-5278. EMIF_CTLCFG_DENALI_PHY_1066 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_ADR_MEAS_DLY_STEP_ENABLE_2
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_CAPTURE_CNT_2			
NONE				R/W			
0h				0h			

Table 14-15954. EMIF_CTLCFG_DENALI_PHY_1066 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	PHY_ADR_MEAS_DLY_STEP_ENABLE_2	R/W	0h	Enables delay parameter setting using phy_adr_meas_dly_step_value for address slice 2. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADR_CALVL_CAPTURE_CNT_2	R/W	0h	Number of samples to take at each ADDR target delay setting during CA training for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1200 EMIF_CTLCFG_DENALI_PHY_1280 Register

1 EMIF_CTLCFG_DENALI_PHY_1280 Register (Offset = 5400h) [reset = 0h]

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Table 14-15955. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D400h**

Figure 14-5279. EMIF_CTLCFG_DENALI_PHY_1280 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_FREQ_SEL	
NONE						R/W	
0h						0h	

Table 14-15957. EMIF_CTLCFG_DENALI_PHY_1280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PHY_FREQ_SEL	R/W	0h	Specifies which copy of the frequency-dependent timing parameters will be used by the PHY. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1201 EMIF_CTLCFG_DENALI_PHY_1281 Register

1 EMIF_CTLCFG_DENALI_PHY_1281 Register (Offset = 5404h) [reset = 100h]

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Table 14-15958. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D404h**

Figure 14-5280. EMIF_CTLCFG_DENALI_PHY_1281 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_SW_GRP0_SHIFT_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_FREQ_SEL_INDEX	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_FREQ_SEL_MULTICAST_EN
NONE							R/W
0h							1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_FREQ_SEL_FROM_REGIF
NONE							R/W
0h							0h

Table 14-15960. EMIF_CTLCFG_DENALI_PHY_1281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_SW_GRP0_SHIFT_0	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_FREQ_SEL_INDEX	R/W	0h	Selects which frequency set to update when PHY_FREQ_SEL_MULTICAST_EN is not set. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_FREQ_SEL_MULTICAST_EN	R/W	1h	When set, a register write will update parameters for all frequency sets simultaneously. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_FREQ_SEL_FROM_REGIF	R/W	0h	Indicates which source is used to select the frequency copy. When set to 1, the frequency select source is given by parameter PHY_FREQ_SEL from register I/F. When cleared to 0, the frequency select source is the PHY input signal dfi_frequency Reset Source: ctl_amod_g_rst_n

14.5.1.2.1202 EMIF_CTLCFG_DENALI_PHY_1282 Register

1 EMIF_CTLCFG_DENALI_PHY_1282 Register (Offset = 5408h) [reset = 0h]

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Table 14-15961. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D408h**

Figure 14-5281. EMIF_CTLCFG_DENALI_PHY_1282 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_SW_GRP0_SHIFT_1				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_SW_GRP3_SHIFT_0				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_SW_GRP2_SHIFT_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_SW_GRP1_SHIFT_0				
NONE			R/W				
0h			0h				

Table 14-15963. EMIF_CTLCFG_DENALI_PHY_1282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_SW_GRP0_SHIFT_1	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP3_SHIFT_0	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_SW_GRP2_SHIFT_0	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_SW_GRP1_SHIFT_0	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1203 EMIF_CTLCFG_DENALI_PHY_1283 Register

1 EMIF_CTLCFG_DENALI_PHY_1283 Register (Offset = 540Ch) [reset = 0h]

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Table 14-15964. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D40Ch

Figure 14-5282. EMIF_CTLCFG_DENALI_PHY_1283 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_SW_GRP0_SHIFT_2				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PHY_SW_GRP3_SHIFT_1				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PHY_SW_GRP2_SHIFT_1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_SW_GRP1_SHIFT_1				
NONE			R/W				
0h			0h				

Table 14-15966. EMIF_CTLCFG_DENALI_PHY_1283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_SW_GRP0_SHIFT_2	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP3_SHIFT_1	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_SW_GRP2_SHIFT_1	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_SW_GRP1_SHIFT_1	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1204 EMIF_CTLCFG_DENALI_PHY_1284 Register

1 EMIF_CTLCFG_DENALI_PHY_1284 Register (Offset = 5410h) [reset = 0h]

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Table 14-15967. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D410h**

Figure 14-5283. EMIF_CTLCFG_DENALI_PHY_1284 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_SW_GRP0_SHIFT_3				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_SW_GRP3_SHIFT_2				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_SW_GRP2_SHIFT_2				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_SW_GRP1_SHIFT_2				
NONE			R/W				
0h			0h				

Table 14-15969. EMIF_CTLCFG_DENALI_PHY_1284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_SW_GRP0_SHIFT_3	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP3_SHIFT_2	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_SW_GRP2_SHIFT_2	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_SW_GRP1_SHIFT_2	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1205 EMIF_CTLCFG_DENALI_PHY_1285 Register

1 EMIF_CTLCFG_DENALI_PHY_1285 Register (Offset = 5414h) [reset = 0h]

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Table 14-15970. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D414h**

Figure 14-5284. EMIF_CTLCFG_DENALI_PHY_1285 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_SW_GRP3_SHIFT_3				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PHY_SW_GRP2_SHIFT_3				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_SW_GRP1_SHIFT_3				
NONE			R/W				
0h			0h				

Table 14-15972. EMIF_CTLCFG_DENALI_PHY_1285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP3_SHIFT_3	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_SW_GRP2_SHIFT_3	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_SW_GRP1_SHIFT_3	R/W	0h	Address slice target delay setting for address slice 4. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1206 EMIF_CTLCFG_DENALI_PHY_1286 Register

1 EMIF_CTLCFG_DENALI_PHY_1286 Register (Offset = 5418h) [reset = 0h]

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Table 14-15973. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D418h**

Figure 14-5285. EMIF_CTLCFG_DENALI_PHY_1286 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GRP_BYPASS_OVERRIDE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_SW_GRP_BYPASS_SHIFT				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP_BYPASS_SLAVE_DELAY		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP_BYPASS_SLAVE_DELAY							
R/W							
0h							

Table 14-15975. EMIF_CTLCFG_DENALI_PHY_1286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_GRP_BYPASS_OVERRIDE	R/W	0h	Address/control group slice bypass mode override setting. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_SW_GRP_BYPASS_SHIFT	R/W	0h	Address/control group slice bypass mode shift settings. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP_BYPASS_SLAVE_DELAY	R/W	0h	Address/control group slice bypass mode target delay setting. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1207 EMIF_CTLCFG_DENALI_PHY_1287 Register

1 EMIF_CTLCFG_DENALI_PHY_1287 Register (Offset = 541Ch) [reset = 100h]

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Table 14-15976. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D41Ch**

Figure 14-5286. EMIF_CTLCFG_DENALI_PHY_1287 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CSLVL_START		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CSLVL_START							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_MANUAL_UPDATE_PHYUPD_ENABLE
NONE							R/W
0h							1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SC_PHY_MANUAL_UPDATE
NONE							W
0h							0h

Table 14-15978. EMIF_CTLCFG_DENALI_PHY_1287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_CSLVL_START	R/W	0h	Defines the CS training DDL start value. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_MANUAL_UPDATE_PHYUPD_ENABLE	R/W	1h	Manual update selection of all target delay line settings. Set 1 to assert phyupd_req and wait phyupd_ack to update delay line, set 0 to update delay line directly. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	SC_PHY_MANUAL_UPDATE	W	0h	Manual update of all target delay line settings. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1208 EMIF_CTLCFG_DENALI_PHY_1288 Register

1 EMIF_CTLCFG_DENALI_PHY_1288 Register (Offset = 5420h) [reset = 0h]

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Table 14-15979. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D420h**

Figure 14-5287. EMIF_CTLCFG_DENALI_PHY_1288 Name Register

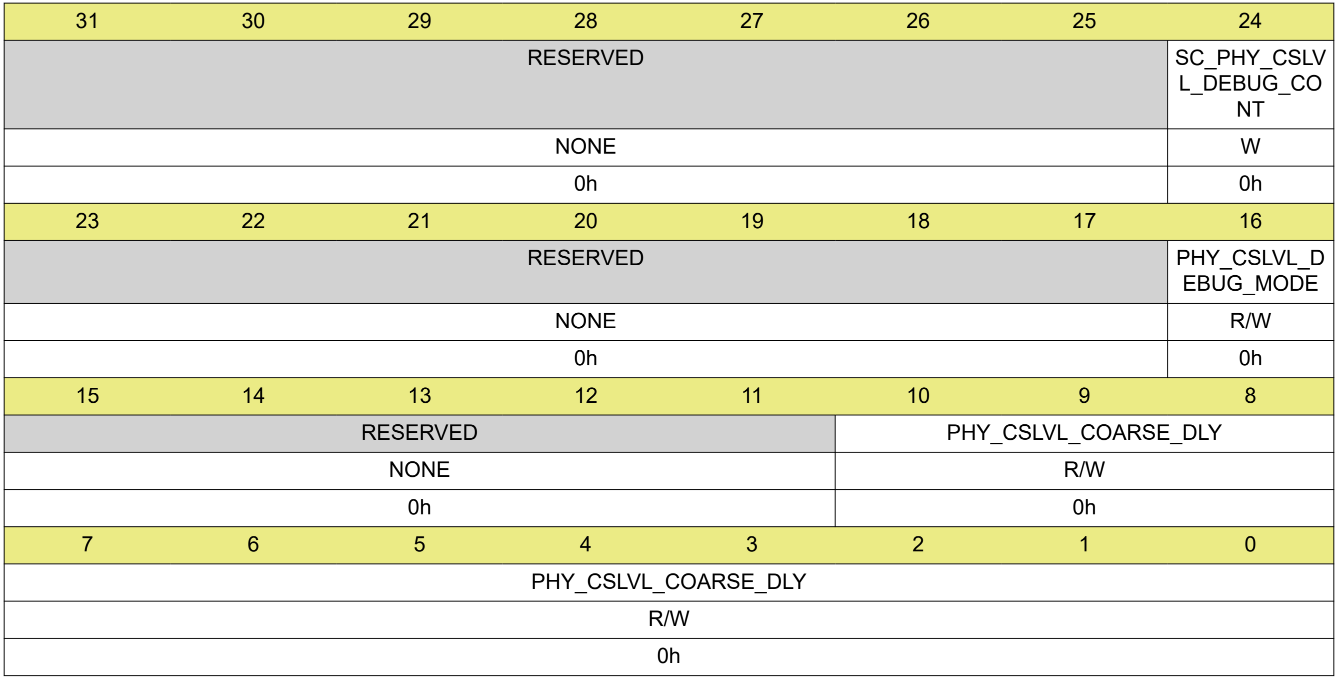

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_CSLVL_DEBUG_CONT
NONE							W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_CSLVL_DEBUG_MODE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_CSLVL_COARSE_DLY		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CSLVL_COARSE_DLY							
R/W							
0h							

Table 14-15981. EMIF_CTLCFG_DENALI_PHY_1288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	SC_PHY_CSLVL_DEBUG_CONT	W	0h	Allows the CS training state machine to advance [when in debug mode]. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_CSLVL_DEBUG_MODE	R/W	0h	Enables CS training debug mode. Set to 1 to enable. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CSLVL_COARSE_DLY	R/W	0h	Defines the CS training DDL coarse cycle delay value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1209 EMIF_CTLCFG_DENALI_PHY_1289 Register

1 EMIF_CTLCFG_DENALI_PHY_1289 Register (Offset = 5424h) [reset = 0h]

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Table 14-15982. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D424h**

Figure 14-5288. EMIF_CTLCFG_DENALI_PHY_1289 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SC_PHY_CSLVL_ERROR_CLR
NONE							W
0h							0h

Table 14-15984. EMIF_CTLCFG_DENALI_PHY_1289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SC_PHY_CSLVL_ERROR_CLR	W	0h	Clears the CS training state machine error status. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1210 EMIF_CTLCFG_DENALI_PHY_1290 Register

1 EMIF_CTLCFG_DENALI_PHY_1290 Register (Offset = 5428h) [reset = 6800000h]

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Table 14-15985. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D428h**

Figure 14-5289. EMIF_CTLCFG_DENALI_PHY_1290 Name Register

31	30	29	28	27	26	25	24
PHY_CSLVL_OBS0							
R							
6800000h							
23	22	21	20	19	18	17	16
PHY_CSLVL_OBS0							
R							
6800000h							
15	14	13	12	11	10	9	8
PHY_CSLVL_OBS0							
R							
6800000h							
7	6	5	4	3	2	1	0
PHY_CSLVL_OBS0							
R							
6800000h							

Table 14-15987. EMIF_CTLCFG_DENALI_PHY_1290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CSLVL_OBS0	R	6800000h	Observation register for CS training delay values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1211 EMIF_CTLCFG_DENALI_PHY_1291 Register

1 EMIF_CTLCFG_DENALI_PHY_1291 Register (Offset = 542Ch) [reset = 0h]

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Table 14-15988. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D42Ch

Figure 14-5290. EMIF_CTLCFG_DENALI_PHY_1291 Name Register

31	30	29	28	27	26	25	24
PHY_CSLVL_OBS1							
R							
0h							
23	22	21	20	19	18	17	16
PHY_CSLVL_OBS1							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CSLVL_OBS1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CSLVL_OBS1							
R							
0h							

Table 14-15990. EMIF_CTLCFG_DENALI_PHY_1291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CSLVL_OBS1	R	0h	Observation register for CS training algorithm status. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1212 EMIF_CTLCFG_DENALI_PHY_1292 Register

1 EMIF_CTLCFG_DENALI_PHY_1292 Register (Offset = 5430h) [reset = 0h]

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Table 14-15991. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D430h**

Figure 14-5291. EMIF_CTLCFG_DENALI_PHY_1292 Name Register

31	30	29	28	27	26	25	24
PHY_CSLVL_OBS2							
R							
0h							
23	22	21	20	19	18	17	16
PHY_CSLVL_OBS2							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CSLVL_OBS2							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CSLVL_OBS2							
R							
0h							

Table 14-15993. EMIF_CTLCFG_DENALI_PHY_1292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CSLVL_OBS2	R	0h	Observation register for periodic CS training delay values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1213 EMIF_CTLCFG_DENALI_PHY_1293 Register

1 EMIF_CTLCFG_DENALI_PHY_1293 Register (Offset = 5434h) [reset = 0h]

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Table 14-15994. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 D434h**

Figure 14-5292. EMIF_CTLCFG_DENALI_PHY_1293 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LP4_BOOT_DISABLE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_CSLVL_PERIODIC_START_OFFSET
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CSLVL_PERIODIC_START_OFFSET							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_CSLVL_ENABLE
NONE							R/W
0h							0h

Table 14-15996. EMIF_CTLCFG_DENALI_PHY_1293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LP4_BOOT_DISABLE	R/W	0h	Controls the handling of the DFI frequency. When set to 1, DFI frequency 0 is considered the first operational frequency. When cleared to 0, DFI frequency 0 is the boot frequency and other DFI frequency values are operational frequencies. Must be cleared to 0 for LPDDR3 devices operating in an LPDDR4 capable configuration. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:8	PHY_CSLVL_PERIODIC_START_OFFSET	R/W	0h	Defines the relative offset from previous LE and TE to start periodic CSLVL with. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_CSLVL_ENABLE	R/W	0h	CS training enable. Set to 1 to enable CS training during CA training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1214 EMIF_CTLCFG_DENALI_PHY_1294 Register

1 EMIF_CTLCFG_DENALI_PHY_1294 Register (Offset = 5438h) [reset = 0h]

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Table 14-15997. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D438h**

Figure 14-5293. EMIF_CTLCFG_DENALI_PHY_1294 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_CSLVL_QTR</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_CSLVL_QTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_CSLVL_CS_MAP</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-15999. EMIF_CTLCFG_DENALI_PHY_1294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:8	PHY_CSLVL_QTR	R/W	0h	Defines the CS training DDL 1/4 cycle delay value. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CSLVL_CS_MAP	R/W	0h	CS training map. Set each CS bit to 1 to allow that CS to participate in CS training results. NOT CURRENTLY USED. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1215 EMIF_CTLCFG_DENALI_PHY_1295 Register

1 EMIF_CTLCFG_DENALI_PHY_1295 Register (Offset = 543Ch) [reset = 0h]

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Table 14-16000. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D43Ch**

Figure 14-5294. EMIF_CTLCFG_DENALI_PHY_1295 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADRCTL_SLAVE_LOOP_CNT_UPDATE		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED				PHY_CSLVL_COARSE_CAPTURE_CNT			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_CSLVL_COARSE_CHK		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CSLVL_COARSE_CHK							
R/W							
0h							

Table 14-16002. EMIF_CTLCFG_DENALI_PHY_1295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ADRCTL_SLAVE_LOOP_CNT_UPDATE	R/W	0h	Reserved for the address/control controller. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_CSLVL_COARSE_CAPTURE_CNT	R/W	0h	Defines the number of samples to take at each GRP target delay setting during CS training coarse CA training. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_CSLVL_COARSE_CHK	R/W	0h	Defines the CS training coarse CA training DDL 1/16th cycle delay value. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1216 EMIF_CTLCFG_DENALI_PHY_1296 Register

1 EMIF_CTLCFG_DENALI_PHY_1296 Register (Offset = 5440h) [reset = 0h]

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Table 14-16003. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D440h**

Figure 14-5295. EMIF_CTLCFG_DENALI_PHY_1296 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LP4_ACTIVE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_ADRCTL_LPDDR
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PHY_DFI_PHYUPD_TYPE	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_ADRCTL_SNAP_OBS_REGS
NONE							W
0h							0h

Table 14-16005. EMIF_CTLCFG_DENALI_PHY_1296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LP4_ACTIVE	R/W	0h	Indicates an LPDDR4 device is connected to the PHY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADRCTL_LPDDR	R/W	0h	Adds a cycle of delay for the address/control slices to match the address slice. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_DFI_PHYUPD_TYPE	R/W	0h	Defines the value of the dfi_phyupd_type output signal to MC. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_ADRCTL_SNAP_OBS_REGS	W	0h	Initiates a snapshot of the internal observation registers for the address/control block. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1217 EMIF_CTLCFG_DENALI_PHY_1297 Register

1 EMIF_CTLCFG_DENALI_PHY_1297 Register (Offset = 5444h) [reset = 1h]

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Table 14-16006. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D444h

Figure 14-5296. EMIF_CTLCFG_DENALI_PHY_1297 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_TXIO_CTRL_0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_CONTINUOUS_CLK_CAL_UPDATE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							SC_PHY_UPDATE_CLK_CAL_VALUES
NONE							W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_LPDDR3_CS
NONE							R/W
0h							1h

Table 14-16008. EMIF_CTLCFG_DENALI_PHY_1297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_SW_TXIO_CTRL_0	R/W	0h	This register is used to control if command pad [CS/RAS...] should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_CONTINUOUS_CLK_CAL_UPDATE	R/W	0h	Continuous update of all latest PVTP,PVTN and PVTR values to the CLK IO pads. Set to 1 to keep this enabled. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	SC_PHY_UPDATE_CLK_CAL_VALUES	W	0h	Manual update of all latest PVTP,PVTN and PVTR values to the CLK IO pads. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LPDDR3_CS	R/W	1h	Alters reset state polarity for LPDDR chip selects. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1218 EMIF_CTLCFG_DENALI_PHY_1298 Register

1 EMIF_CTLCFG_DENALI_PHY_1298 Register (Offset = 5448h) [reset = 0h]

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Table 14-16009. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D448h

Figure 14-5297. EMIF_CTLCFG_DENALI_PHY_1298 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_MEMCLK_SW_TXIO_CTRL
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_SW_TXIO_CTRL_3			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_SW_TXIO_CTRL_2			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_SW_TXIO_CTRL_1			
NONE				R/W			
0h				0h			

Table 14-16011. EMIF_CTLCFG_DENALI_PHY_1298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_MEMCLK_SW_TXIO_CTRL	R/W	0h	This register is used to control if clk pads should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_SW_TXIO_CTRL_3	R/W	0h	This register is used to control if command pad [CS/RAS...] should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SW_TXIO_CTRL_2	R/W	0h	This register is used to control if command pad [CS/RAS...] should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_SW_TXIO_CTRL_1	R/W	0h	This register is used to control if command pad [CS/RAS...] should be shutoff for TX mode. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1219 EMIF_CTLCFG_DENALI_PHY_1299 Register

1 EMIF_CTLCFG_DENALI_PHY_1299 Register (Offset = 544Ch) [reset = 0h]

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Table 14-16012. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D44Ch

Figure 14-5298. EMIF_CTLCFG_DENALI_PHY_1299 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_3			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_0			
NONE				R/W			
0h				0h			

Table 14-16014. EMIF_CTLCFG_DENALI_PHY_1299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_ADRCTL_SW_TXPWR_CTRL_3	R/W	0h	This register is used to control if address/command pad [address/CS/RAS...] should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADRCTL_SW_TXPWR_CTRL_2	R/W	0h	This register is used to control if address/command pad [address/CS/RAS...] should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_ADRCTL_SW_TXPWR_CTRL_1	R/W	0h	This register is used to control if address/command pad [address/CS/RAS...] should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_ADRCTL_SW_TXPWR_CTRL_0	R/W	0h	This register is used to control if address/command pad [address/CS/RAS...] should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1220 EMIF_CTLCFG_DENALI_PHY_1300 Register

1 EMIF_CTLCFG_DENALI_PHY_1300 Register (Offset = 5450h) [reset = 0h]

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Table 14-16015. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D450h**

Figure 14-5299. EMIF_CTLCFG_DENALI_PHY_1300 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_BYTE_DISABLE_STATIC_TOG_DISABLE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_TOP_STATIC_TOG_DISABLE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_MEMCLK_SW_TXPWR_CTRL
NONE							R/W
0h							0h

Table 14-16017. EMIF_CTLCFG_DENALI_PHY_1300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_BYTE_DISABLE_STATIC_TOG_DISABLE	R/W	0h	Control to disable the toggle signal for data slice during static activity when dfi_data_byte_disable is asserted. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_TOP_STATIC_TOG_DISABLE	R/W	0h	Disables the generation of the toggle for static clock based paths in the PHY to prevent assymetric aging. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_MEMCLK_SW_TXPWR_CTRL	R/W	0h	This register is used to control if clk pads should be shutoff for TX mode in deep sleep mode. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1221 EMIF_CTLCFG_DENALI_PHY_1301 Register

1 EMIF_CTLCFG_DENALI_PHY_1301 Register (Offset = 5454h) [reset = 0h]

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Table 14-16018. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D454h**

Figure 14-5300. EMIF_CTLCFG_DENALI_PHY_1301 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_MEMCLK_STATIC_TOG_DISABLE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED				PHY_ADRCTL_STATIC_TOG_DISABLE			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PHY_STATIC_TOG_CONTROL							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_STATIC_TOG_CONTROL							
R/W							
0h							

Table 14-16020. EMIF_CTLCFG_DENALI_PHY_1301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_MEMCLK_STATIC_TOG_DISABLE	R/W	0h	Control to disable toggle during static activity. bit0: clock disable. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_ADRCTL_STATIC_TOG_DISABLE	R/W	0h	Control to disable toggle during static activity. bit0: Write path delay line disable; bit1: clock disable; bit2: adrctl controller delay line disable [if exists]; bit3: adrctl misc core clk disable.[if exists] Reset Source: ctl_amod_g_rst_n
15:0	PHY_STATIC_TOG_CONTROL	R/W	0h	Clock divider to create toggle signal. Use long counter as the base. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1222 EMIF_CTLCFG_DENALI_PHY_1302 Register

1 EMIF_CTLCFG_DENALI_PHY_1302 Register (Offset = 5458h) [reset = 0h]

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Table 14-16021. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D458h**

Figure 14-5301. EMIF_CTLCFG_DENALI_PHY_1302 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_LP4_BOOT_PLL_BYPASS
NONE							R/W
0h							0h

Table 14-16023. EMIF_CTLCFG_DENALI_PHY_1302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_LP4_BOOT_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1223 EMIF_CTLCFG_DENALI_PHY_1303 Register

1 EMIF_CTLCFG_DENALI_PHY_1303 Register (Offset = 545Ch) [reset = 10082650h]

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Table 14-16024. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D45Ch**

Figure 14-5302. EMIF_CTLCFG_DENALI_PHY_1303 Name Register

31	30	29	28	27	26	25	24
PHY_CLK_SWITCH_OBS							
R							
10082650h							
23	22	21	20	19	18	17	16
PHY_CLK_SWITCH_OBS							
R							
10082650h							
15	14	13	12	11	10	9	8
PHY_CLK_SWITCH_OBS							
R							
10082650h							
7	6	5	4	3	2	1	0
PHY_CLK_SWITCH_OBS							
R							
10082650h							

Table 14-16026. EMIF_CTLCFG_DENALI_PHY_1303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CLK_SWITCH_OBS	R	10082650h	Observation register for Clock switch state machine READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1224 EMIF_CTLCFG_DENALI_PHY_1304 Register

1 EMIF_CTLCFG_DENALI_PHY_1304 Register (Offset = 5460h) [reset = 0h]

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Table 14-16027. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D460h**

Figure 14-5303. EMIF_CTLCFG_DENALI_PHY_1304 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHY_PLL_WAIT							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_PLL_WAIT							
R/W							
0h							

Table 14-16029. EMIF_CTLCFG_DENALI_PHY_1304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHY_PLL_WAIT	R/W	0h	PHY clock PLL wait time after locking. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1225 EMIF_CTLCFG_DENALI_PHY_1305 Register

1 EMIF_CTLCFG_DENALI_PHY_1305 Register (Offset = 5464h) [reset = 0h]

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Table 14-16030. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D464h**

Figure 14-5304. EMIF_CTLCFG_DENALI_PHY_1305 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_SW_PLL_BYPASS
NONE							R/W
0h							0h

Table 14-16032. EMIF_CTLCFG_DENALI_PHY_1305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_SW_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1226 EMIF_CTLCFG_DENALI_PHY_1306 Register

1 EMIF_CTLCFG_DENALI_PHY_1306 Register (Offset = 5468h) [reset = 0h]

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Table 14-16033. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D468h**

Figure 14-5305. EMIF_CTLCFG_DENALI_PHY_1306 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SET_DFI_INPUT_3			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_SET_DFI_INPUT_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_SET_DFI_INPUT_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_SET_DFI_INPUT_0			
NONE				R/W			
0h				0h			

Table 14-16035. EMIF_CTLCFG_DENALI_PHY_1306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_SET_DFI_INPUT_3	R/W	0h	Used to indicate the default value of the adrctl slice bits. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_SET_DFI_INPUT_2	R/W	0h	Used to indicate the default value of the adrctl slice bits. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_SET_DFI_INPUT_1	R/W	0h	Used to indicate the default value of the adrctl slice bits. Reset Source: ctl_amod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	PHY_SET_DFI_INPUT_0	R/W	0h	Used to indicate the default value of the adrctl slice bits. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1227 EMIF_CTLCFG_DENALI_PHY_1307 Register

1 EMIF_CTLCFG_DENALI_PHY_1307 Register (Offset = 546Ch) [reset = 0h]

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Table 14-16036. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D46Ch**

Figure 14-5306. EMIF_CTLCFG_DENALI_PHY_1307 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CS_ACS_ALLOCATION_BIT3_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PHY_CS_ACS_ALLOCATION_BIT2_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_CS_ACS_ALLOCATION_BIT1_0	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PHY_CS_ACS_ALLOCATION_BIT0_0	
NONE						R/W	
0h						0h	

Table 14-16038. EMIF_CTLCFG_DENALI_PHY_1307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_CS_ACS_ALLOCATION_BIT3_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_0 bit3, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_CS_ACS_ALLOCATION_BIT2_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_0 bit2 , 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved

Table 14-16038. EMIF_CTLCFG_DENALI_PHY_1307 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	PHY_CS_ACS_ALLOCATION_BIT1_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_0 bit1, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CS_ACS_ALLOCATION_BIT0_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_0 bit0, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1228 EMIF_CTLCFG_DENALI_PHY_1308 Register

1 EMIF_CTLCFG_DENALI_PHY_1308 Register (Offset = 5470h) [reset = 0h]

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Table 14-16039. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D470h**

Figure 14-5307. EMIF_CTLCFG_DENALI_PHY_1308 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CS_ACS_ALLOCATION_BIT3_1	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_CS_ACS_ALLOCATION_BIT2_1	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_CS_ACS_ALLOCATION_BIT1_1	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_CS_ACS_ALLOCATION_BIT0_1	
NONE						R/W	
0h						0h	

Table 14-16041. EMIF_CTLCFG_DENALI_PHY_1308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_CS_ACS_ALLOCATION_BIT3_1	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 1. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_1 bit3, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_CS_ACS_ALLOCATION_BIT2_1	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 1. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_1 bit2 , 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved

Table 14-16041. EMIF_CTLCFG_DENALI_PHY_1308 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	PHY_CS_ACS_ALLOCATION_BIT1_1	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 1. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_1 bit1, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CS_ACS_ALLOCATION_BIT0_1	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 1. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_1 bit0, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1229 EMIF_CTLCFG_DENALI_PHY_1309 Register

1 EMIF_CTLCFG_DENALI_PHY_1309 Register (Offset = 5474h) [reset = 0h]

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Table 14-16042. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 D474h**

Figure 14-5308. EMIF_CTLCFG_DENALI_PHY_1309 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CS_ACS_ALLOCATION_BIT3_2	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						PHY_CS_ACS_ALLOCATION_BIT2_2	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_CS_ACS_ALLOCATION_BIT1_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PHY_CS_ACS_ALLOCATION_BIT0_2	
NONE						R/W	
0h						0h	

Table 14-16044. EMIF_CTLCFG_DENALI_PHY_1309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_CS_ACS_ALLOCATION_BIT3_2	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 2. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_2 bit3, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_2, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_CS_ACS_ALLOCATION_BIT2_2	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 2. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_2 bit2 , 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_2, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved

Table 14-16044. EMIF_CTLCFG_DENALI_PHY_1309 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	PHY_CS_ACS_ALLOCATION_BIT1_2	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 2. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_2 bit1, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_2, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CS_ACS_ALLOCATION_BIT0_2	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 2. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_2 bit0, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_2, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1230 EMIF_CTLCFG_DENALI_PHY_1310 Register

1 EMIF_CTLCFG_DENALI_PHY_1310 Register (Offset = 5478h) [reset = 0h]

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Table 14-16045. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D478h**

Figure 14-5309. EMIF_CTLCFG_DENALI_PHY_1310 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_CS_ACS_ALLOCATION_BIT3_3	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_CS_ACS_ALLOCATION_BIT2_3	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_CS_ACS_ALLOCATION_BIT1_3	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PHY_CS_ACS_ALLOCATION_BIT0_3	
NONE						R/W	
0h						0h	

Table 14-16047. EMIF_CTLCFG_DENALI_PHY_1310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_CS_ACS_ALLOCATION_BIT3_3	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 3. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_3 bit3, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_3, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17:16	PHY_CS_ACS_ALLOCATION_BIT2_3	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 3. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_3 bit2 , 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_3, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved

Table 14-16047. EMIF_CTLCFG_DENALI_PHY_1310 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	PHY_CS_ACS_ALLOCATION_BIT1_3	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 3. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_3 bit1, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_3, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_CS_ACS_ALLOCATION_BIT0_3	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 3. Bit [n], 1 means cs[n]'s signal[CS/CKE/ODT/RST] is allocated on ACS_3 bit0, 0 means cs[n]'s signal[CS/CKE/ODT/RST] is not tranfser on ACS_3, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1231 EMIF_CTLCFG_DENALI_PHY_1311 Register

1 EMIF_CTLCFG_DENALI_PHY_1311 Register (Offset = 547Ch) [reset = 0h]

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Table 14-16048. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D47Ch**

Figure 14-5310. EMIF_CTLCFG_DENALI_PHY_1311 Name Register

31	30	29	28	27	26	25	24
PHY_PLL_CTRL_OVERRIDE							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_PLL_CTRL_OVERRIDE							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED			PHY_LP4_BOOT_PLL_CTRL				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PHY_LP4_BOOT_PLL_CTRL							
R/W							
0h							

Table 14-16050. EMIF_CTLCFG_DENALI_PHY_1311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHY_PLL_CTRL_OVERRIDE	R/W	0h	Individual PHY clock PLL control overrides. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:0	PHY_LP4_BOOT_PLL_CTRL	R/W	0h	PHY deskew PLL controls for LPDDR4 boot frequency. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1232 EMIF_CTLCFG_DENALI_PHY_1312 Register

1 EMIF_CTLCFG_DENALI_PHY_1312 Register (Offset = 5480h) [reset = 0h]

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Table 14-16051. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D480h**

Figure 14-5311. EMIF_CTLCFG_DENALI_PHY_1312 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						SC_PHY_PLL_SPO_CAL_SNAP_OBS	
NONE						W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_PLL_SPO_CAL_CTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_USE_PLL_DSKEWCALLOCK
NONE							R/W
0h							0h

Table 14-16053. EMIF_CTLCFG_DENALI_PHY_1312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	SC_PHY_PLL_SPO_CAL_SNAP_OBS	W	0h	Register command to take a snapshot of PLL output. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:8	PHY_PLL_SPO_CAL_CTRL	R/W	0h	PLL SPO Cal controls. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_USE_PLL_DSKEWCALLOCK	R/W	0h	Use DSKEWCALLOCK or not. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1233 EMIF_CTLCFG_DENALI_PHY_1313 Register

1 EMIF_CTLCFG_DENALI_PHY_1313 Register (Offset = 5484h) [reset = 0h]

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Table 14-16054. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D484h**

Figure 14-5312. EMIF_CTLCFG_DENALI_PHY_1313 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PLL_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PLL_OBS_0							
R							
0h							

Table 14-16056. EMIF_CTLCFG_DENALI_PHY_1313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHY_PLL_OBS_0	R	0h	PHY TOP level clock PLL_0 observe values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1234 EMIF_CTLCFG_DENALI_PHY_1314 Register

1 EMIF_CTLCFG_DENALI_PHY_1314 Register (Offset = 5488h) [reset = 0h]

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Table 14-16057. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D488h

Figure 14-5313. EMIF_CTLCFG_DENALI_PHY_1314 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_PLL_SPO_CAL_OBS_0
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PLL_SPO_CAL_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PLL_SPO_CAL_OBS_0							
R							
0h							

Table 14-16059. EMIF_CTLCFG_DENALI_PHY_1314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PHY_PLL_SPO_CAL_OBS_0	R	0h	PHY TOP level PLL_0 SPO Cal observe values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1235 EMIF_CTLCFG_DENALI_PHY_1315 Register

1 EMIF_CTLCFG_DENALI_PHY_1315 Register (Offset = 548Ch) [reset = 0h]

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Table 14-16060. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D48Ch**

Figure 14-5314. EMIF_CTLCFG_DENALI_PHY_1315 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_PLL_DESKEWCALIN_0			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_LP4_BOOT_PLL_DESKEWCALIN_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_PLL_DESKEWCALIN_0			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PLL_DESKEWCALIN_0							
R/W							
0h							

Table 14-16062. EMIF_CTLCFG_DENALI_PHY_1315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_LP4_BOOT_PLL_DESKEWCALIN_0	R/W	0h	PHY TOP level PLL_0 lpddr4 boot deskewcal in values. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PHY_PLL_DESKEWCALIN_0	R/W	0h	PHY TOP level PLL_0 deskewcal in values. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1236 EMIF_CTLCFG_DENALI_PHY_1316 Register

1 EMIF_CTLCFG_DENALI_PHY_1316 Register (Offset = 5490h) [reset = 0h]

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Table 14-16063. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D490h**

Figure 14-5315. EMIF_CTLCFG_DENALI_PHY_1316 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PHY_PLL_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_PLL_OBS_1							
R							
0h							

Table 14-16065. EMIF_CTLCFG_DENALI_PHY_1316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PHY_PLL_OBS_1	R	0h	PHY TOP level clock PLL_1 observe values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1237 EMIF_CTLCFG_DENALI_PHY_1317 Register

1 EMIF_CTLCFG_DENALI_PHY_1317 Register (Offset = 5494h) [reset = 0h]

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Table 14-16066. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D494h**

Figure 14-5316. EMIF_CTLCFG_DENALI_PHY_1317 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_PLL_SPO_CAL_OBS_1
NONE							R
0h							0h
15	14	13	12	11	10	9	8
PHY_PLL_SPO_CAL_OBS_1							
R							
0h							
7	6	5	4	3	2	1	0
PHY_PLL_SPO_CAL_OBS_1							
R							
0h							

Table 14-16068. EMIF_CTLCFG_DENALI_PHY_1317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PHY_PLL_SPO_CAL_OBS_1	R	0h	PHY TOP level PLL_1 SPO Cal observe values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1238 EMIF_CTLCFG_DENALI_PHY_1318 Register

1 EMIF_CTLCFG_DENALI_PHY_1318 Register (Offset = 5498h) [reset = 0h]

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Table 14-16069. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D498h**

Figure 14-5317. EMIF_CTLCFG_DENALI_PHY_1318 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_PLL_DESKEWCALIN_1			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_LP4_BOOT_PLL_DESKEWCALIN_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PHY_PLL_DESKEWCALIN_1			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PLL_DESKEWCALIN_1							
R/W							
0h							

Table 14-16071. EMIF_CTLCFG_DENALI_PHY_1318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	PHY_LP4_BOOT_PLL_DESKEWCALIN_1	R/W	0h	PHY TOP level PLL_1 lpddr4 boot deskewcal in values. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PHY_PLL_DESKEWCALIN_1	R/W	0h	PHY TOP level PLL_1 deskewcal in values. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1239 EMIF_CTLCFG_DENALI_PHY_1319 Register

1 EMIF_CTLCFG_DENALI_PHY_1319 Register (Offset = 549Ch) [reset = 0h]

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Table 14-16072. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D49Ch

Figure 14-5318. EMIF_CTLCFG_DENALI_PHY_1319 Name Register

31	30	29	28	27	26	25	24
PHY_LP_WAKEUP							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PHY_TCKSRE_WAIT			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_LP4_BOOT_LOW_FREQ_SEL
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_PLL_REFOUT_SEL
NONE							R/W
0h							0h

Table 14-16074. EMIF_CTLCFG_DENALI_PHY_1319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PHY_LP_WAKEUP	R/W	0h	Specifies the number of cycles the PHY takes to wakeup in low power mode. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_TCKSRE_WAIT	R/W	0h	Specifies the number of cycles the PHY should wait before turning off the PLL for a deep sleep or DFS event. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_LP4_BOOT_LOW_FREQ_SEL	R/W	0h	Control the PLL domain enter/exit from the negative clock edge for LPDDR4 boot frequency. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_PLL_REFOUT_SEL	R/W	0h	PHY PLL refout select. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1240 EMIF_CTLCFG_DENALI_PHY_1320 Register

1 EMIF_CTLCFG_DENALI_PHY_1320 Register (Offset = 54A0h) [reset = 0h]

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Table 14-16075. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4A0h**

Figure 14-5319. EMIF_CTLCFG_DENALI_PHY_1320 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_LP_CTRLUPD_CNTR_CFG	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_LP_CTRLUPD_CNTR_CFG							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_LS_IDLE_EN
NONE							R/W
0h							0h

Table 14-16077. EMIF_CTLCFG_DENALI_PHY_1320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	PHY_LP_CTRLUPD_CNTR_CFG	R/W	0h	Specifies the number of cycles the PHY takes from light sleep req deassert to ack deassert in low power mode. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_LS_IDLE_EN	R/W	0h	Indicates the Reduced Idle Power State is enabled in low power mode. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1241 EMIF_CTLCFG_DENALI_PHY_1321 Register

1 EMIF_CTLCFG_DENALI_PHY_1321 Register (Offset = 54A4h) [reset = 0h]

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Table 14-16078. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D4A4h

Figure 14-5320. EMIF_CTLCFG_DENALI_PHY_1321 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_TDFI_PHY_WRDELAY
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_DS_EXIT_CTRL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
PHY_DS_EXIT_CTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DS_EXIT_CTRL							
R/W							
0h							

Table 14-16080. EMIF_CTLCFG_DENALI_PHY_1321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_TDFI_PHY_WRDELAY	R/W	0h	DFI timing parameter TDFI_PHY_WRDELAY. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16:0	PHY_DS_EXIT_CTRL	R/W	0h	Controls to reduce the deep sleep exit latency, when bit 16 is 1 deep sleep exit ack won't wait controller delay line lock. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1242 EMIF_CTLCFG_DENALI_PHY_1322 Register

1 EMIF_CTLCFG_DENALI_PHY_1322 Register (Offset = 54A8h) [reset = 4410h]

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Table 14-16081. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4A8h**

Figure 14-5321. EMIF_CTLCFG_DENALI_PHY_1322 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_FDBK_TERM	
NONE						R/W	
0h						4410h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_FDBK_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_FDBK_TERM							
R/W							
4410h							

Table 14-16083. EMIF_CTLCFG_DENALI_PHY_1322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_FDBK_TERM	R/W	4410h	Controls term settings for gate feedback pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1243 EMIF_CTLCFG_DENALI_PHY_1323 Register

1 EMIF_CTLCFG_DENALI_PHY_1323 Register (Offset = 54ACh) [reset = 4410h]

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Table 14-16084. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4ACh**

Figure 14-5322. EMIF_CTLCFG_DENALI_PHY_1323 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_PAD_DATA_TERM</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>4410h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PAD_DATA_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_DATA_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
</table>

Table 14-16086. EMIF_CTLCFG_DENALI_PHY_1323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PHY_PAD_DATA_TERM	R/W	4410h	Controls term settings for data pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1244 EMIF_CTLCFG_DENALI_PHY_1324 Register

1 EMIF_CTLCFG_DENALI_PHY_1324 Register (Offset = 54B0h) [reset = 4410h]

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Table 14-16087. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D4B0h

Figure 14-5323. EMIF_CTLCFG_DENALI_PHY_1324 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_PAD_DQS_TERM
NONE							R/W
0h							4410h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_DQS_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_DQS_TERM							
R/W							
4410h							

Table 14-16089. EMIF_CTLCFG_DENALI_PHY_1324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	PHY_PAD_DQS_TERM	R/W	4410h	Controls term settings for dqs pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1245 EMIF_CTLCFG_DENALI_PHY_1325 Register

1 EMIF_CTLCFG_DENALI_PHY_1325 Register (Offset = 54B4h) [reset = 4410h]

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Table 14-16090. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4B4h**

Figure 14-5324. EMIF_CTLCFG_DENALI_PHY_1325 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_ADDR_TERM	
NONE						R/W	
0h						4410h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ADDR_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ADDR_TERM							
R/W							
4410h							

Table 14-16092. EMIF_CTLCFG_DENALI_PHY_1325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_ADDR_TERM	R/W	4410h	Controls term settings for the address/control pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1246 EMIF_CTLCFG_DENALI_PHY_1326 Register

1 EMIF_CTLCFG_DENALI_PHY_1326 Register (Offset = 54B8h) [reset = 4410h]

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Table 14-16093. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D4B8h

Figure 14-5325. EMIF_CTLCFG_DENALI_PHY_1326 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_CLK_TERM	
NONE						R/W	
0h						4410h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_CLK_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_CLK_TERM							
R/W							
4410h							

Table 14-16095. EMIF_CTLCFG_DENALI_PHY_1326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_CLK_TERM	R/W	4410h	Controls term settings for clock pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1247 EMIF_CTLCFG_DENALI_PHY_1327 Register

1 EMIF_CTLCFG_DENALI_PHY_1327 Register (Offset = 54BCh) [reset = 4410h]

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Table 14-16096. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4BCh**

Figure 14-5326. EMIF_CTLCFG_DENALI_PHY_1327 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_ERR_TERM	
NONE						R/W	
0h						4410h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ERR_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ERR_TERM							
R/W							
4410h							

Table 14-16098. EMIF_CTLCFG_DENALI_PHY_1327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_ERR_TERM	R/W	4410h	Controls term settings for error pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1248 EMIF_CTLCFG_DENALI_PHY_1328 Register

1 EMIF_CTLCFG_DENALI_PHY_1328 Register (Offset = 54C0h) [reset = 4410h]

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Table 14-16099. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4C0h**

Figure 14-5327. EMIF_CTLCFG_DENALI_PHY_1328 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_PAD_CKE_TERM	
NONE						R/W	
0h						4410h	
15	14	13	12	11	10	9	8
PHY_PAD_CKE_TERM							
R/W							
4410h							
7	6	5	4	3	2	1	0
PHY_PAD_CKE_TERM							
R/W							
4410h							

Table 14-16101. EMIF_CTLCFG_DENALI_PHY_1328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_CKE_TERM	R/W	4410h	Controls term settings for cke pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1249 EMIF_CTLCFG_DENALI_PHY_1329 Register

1 EMIF_CTLCFG_DENALI_PHY_1329 Register (Offset = 54C4h) [reset = 4410h]

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Table 14-16102. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4C4h**

Figure 14-5328. EMIF_CTLCFG_DENALI_PHY_1329 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_PAD_RST_TERM</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">4410h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PAD_RST_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_RST_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
</table>

Table 14-16104. EMIF_CTLCFG_DENALI_PHY_1329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_RST_TERM	R/W	4410h	Controls term settings for reset_n pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1250 EMIF_CTLCFG_DENALI_PHY_1330 Register

1 EMIF_CTLCFG_DENALI_PHY_1330 Register (Offset = 54C8h) [reset = 4410h]

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Table 14-16105. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4C8h**

Figure 14-5329. EMIF_CTLCFG_DENALI_PHY_1330 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_PAD_CS_TERM</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">4410h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PAD_CS_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_CS_TERM</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4410h</td></tr>
</table>

Table 14-16107. EMIF_CTLCFG_DENALI_PHY_1330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_CS_TERM	R/W	4410h	Controls term settings for cs pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1251 EMIF_CTLCFG_DENALI_PHY_1331 Register

1 EMIF_CTLCFG_DENALI_PHY_1331 Register (Offset = 54CCh) [reset = 4410h]

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Table 14-16108. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4CCh**

Figure 14-5330. EMIF_CTLCFG_DENALI_PHY_1331 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_ODT_TERM	
NONE						R/W	
0h						4410h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ODT_TERM							
R/W							
4410h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ODT_TERM							
R/W							
4410h							

Table 14-16110. EMIF_CTLCFG_DENALI_PHY_1331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_ODT_TERM	R/W	4410h	Controls term settings for odt pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1252 EMIF_CTLCFG_DENALI_PHY_1332 Register

1 EMIF_CTLCFG_DENALI_PHY_1332 Register (Offset = 54D0h) [reset = 0h]

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Table 14-16111. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4D0h**

Figure 14-5331. EMIF_CTLCFG_DENALI_PHY_1332 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PHY_ADRCTL_LP3_RX_CAL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_ADRCTL_LP3_RX_CAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_ADRCTL_RX_CAL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_ADRCTL_RX_CAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16113. EMIF_CTLCFG_DENALI_PHY_1332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:16	PHY_ADRCTL_LP3_RX_CAL	R/W	0h	PHY CKE/RESET_N RX calibration controls. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_ADRCTL_RX_CAL	R/W	0h	PHY address/control RX calibration controls. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1253 EMIF_CTLCFG_DENALI_PHY_1333 Register

1 EMIF_CTLCFG_DENALI_PHY_1333 Register (Offset = 54D4h) [reset = 0h]

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Table 14-16114. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4D4h**

Figure 14-5332. EMIF_CTLCFG_DENALI_PHY_1333 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CAL_START_0
NONE							W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							PHY_CAL_CLEAR_0
NONE							W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			PHY_CAL_MODE_0				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PHY_CAL_MODE_0							
R/W							
0h							

Table 14-16116. EMIF_CTLCFG_DENALI_PHY_1333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CAL_START_0	W	0h	Manual start for the pad calibration state machine for block 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_CAL_CLEAR_0	W	0h	Clear the pad calibration state machine and results for block 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:0	PHY_CAL_MODE_0	R/W	0h	Pad calibration mode bits for block 0. Bit [0] disables pad calibration upon initialization. Bit [1] enables automatic interval based calibration. Bits [3:2] set the base interval for the interval counter. Bits [7:4] are direct connections to pad control signals. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1254 EMIF_CTLCFG_DENALI_PHY_1334 Register

1 EMIF_CTLCFG_DENALI_PHY_1334 Register (Offset = 54D8h) [reset = 0h]

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Table 14-16117. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4D8h**

Figure 14-5333. EMIF_CTLCFG_DENALI_PHY_1334 Name Register

31	30	29	28	27	26	25	24
PHY_CAL_INTERVAL_COUNT_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_INTERVAL_COUNT_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_INTERVAL_COUNT_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_INTERVAL_COUNT_0							
R/W							
0h							

Table 14-16119. EMIF_CTLCFG_DENALI_PHY_1334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CAL_INTERVAL_COUNT_0	R/W	0h	Pad calibration interval counter compare value for block 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1255 EMIF_CTLCFG_DENALI_PHY_1335 Register

1 EMIF_CTLCFG_DENALI_PHY_1335 Register (Offset = 54DCh) [reset = 0h]

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Table 14-16120. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4DCh**

Figure 14-5334. EMIF_CTLCFG_DENALI_PHY_1335 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_LP4_BOOT_CAL_CLK_SELECT_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_CAL_SAMPLE_WAIT_0							
R/W							
0h							

Table 14-16122. EMIF_CTLCFG_DENALI_PHY_1335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	PHY_LP4_BOOT_CAL_CLK_SELECT_0	R/W	0h	Pad calibration pad clock frequency select setting for LPDDR4 boot frequency for block 0. Reset Source: ctl_amod_g_rst_n
7:0	PHY_CAL_SAMPLE_WAIT_0	R/W	0h	Pad calibration state machine wait count in pad clock cycles for block 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1256 EMIF_CTLCFG_DENALI_PHY_1336 Register

1 EMIF_CTLCFG_DENALI_PHY_1336 Register (Offset = 54E0h) [reset = 0h]

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Table 14-16123. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4E0h**

Figure 14-5335. EMIF_CTLCFG_DENALI_PHY_1336 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CAL_RESULT_OBS_0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CAL_RESULT_OBS_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CAL_RESULT_OBS_0							
R							
0h							

Table 14-16125. EMIF_CTLCFG_DENALI_PHY_1336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT_OBS_0	R	0h	Pad calibration results observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1257 EMIF_CTLCFG_DENALI_PHY_1337 Register

1 EMIF_CTLCFG_DENALI_PHY_1337 Register (Offset = 54E4h) [reset = 0h]

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Table 14-16126. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D4E4h

Figure 14-5336. EMIF_CTLCFG_DENALI_PHY_1337 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT2_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT2_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT2_OBS_0							
R							
0h							

Table 14-16128. EMIF_CTLCFG_DENALI_PHY_1337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT2_OBS_0	R	0h	Pad calibration results [CKE/RESET_N] observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1258 EMIF_CTLCFG_DENALI_PHY_1338 Register

1 EMIF_CTLCFG_DENALI_PHY_1338 Register (Offset = 54E8h) [reset = 0h]

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Table 14-16129. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D4E8h

Figure 14-5337. EMIF_CTLCFG_DENALI_PHY_1338 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT4_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT4_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT4_OBS_0							
R							
0h							

Table 14-16131. EMIF_CTLCFG_DENALI_PHY_1338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT4_OBS_0	R	0h	Pad calibration pass1 shadow results observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1259 EMIF_CTLCFG_DENALI_PHY_1339 Register

1 EMIF_CTLCFG_DENALI_PHY_1339 Register (Offset = 54ECh) [reset = 0h]

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Table 14-16132. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D4ECh

Figure 14-5338. EMIF_CTLCFG_DENALI_PHY_1339 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT5_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT5_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT5_OBS_0							
R							
0h							

Table 14-16134. EMIF_CTLCFG_DENALI_PHY_1339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT5_OBS_0	R	0h	Pad calibration pass2 shadow results observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1260 EMIF_CTLCFG_DENALI_PHY_1340 Register

1 EMIF_CTLCFG_DENALI_PHY_1340 Register (Offset = 54F0h) [reset = 0h]

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Table 14-16135. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4F0h**

Figure 14-5339. EMIF_CTLCFG_DENALI_PHY_1340 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT6_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT6_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT6_OBS_0							
R							
0h							

Table 14-16137. EMIF_CTLCFG_DENALI_PHY_1340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PHY_CAL_RESULT6_OBS_0	R	0h	Pad calibration internal results observation delta values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1261 EMIF_CTLCFG_DENALI_PHY_1341 Register

1 EMIF_CTLCFG_DENALI_PHY_1341 Register (Offset = 54F4h) [reset = 0h]

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Table 14-16138. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D4F4h

Figure 14-5340. EMIF_CTLCFG_DENALI_PHY_1341 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_CAL_CPTR_CNT_0						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
PHY_CAL_RESULT7_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT7_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT7_OBS_0							
R							
0h							

Table 14-16140. EMIF_CTLCFG_DENALI_PHY_1341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_CAL_CPTR_CNT_0	R/W	0h	defines sample capture number in pad calibration process Reset Source: ctl_amod_g_rst_n
23:0	PHY_CAL_RESULT7_OBS_0	R	0h	Pad calibration internal results observation delta values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1262 EMIF_CTLCFG_DENALI_PHY_1342 Register

1 EMIF_CTLCFG_DENALI_PHY_1342 Register (Offset = 54F8h) [reset = 0h]

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Table 14-16141. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4F8h**

Figure 14-5341. EMIF_CTLCFG_DENALI_PHY_1342 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CAL_DBG_CFG_0
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CAL_RCV_FINE_ADJ_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CAL_PD_FINE_ADJ_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CAL_PU_FINE_ADJ_0							
R/W							
0h							

Table 14-16143. EMIF_CTLCFG_DENALI_PHY_1342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_CAL_DBG_CFG_0	R/W	0h	defines debug configuration in pad calibration process Reset Source: ctl_amod_g_rst_n
23:16	PHY_CAL_RCV_FINE_ADJ_0	R/W	0h	defines adjustment for RCV code in pad calibration process Reset Source: ctl_amod_g_rst_n
15:8	PHY_CAL_PD_FINE_ADJ_0	R/W	0h	defines adjustment for PD code in pad calibration process Reset Source: ctl_amod_g_rst_n
7:0	PHY_CAL_PU_FINE_ADJ_0	R/W	0h	defines adjustment for PU code in pad calibration process Reset Source: ctl_amod_g_rst_n

14.5.1.2.1263 EMIF_CTLCFG_DENALI_PHY_1343 Register

1 EMIF_CTLCFG_DENALI_PHY_1343 Register (Offset = 54FCh) [reset = 0h]

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Table 14-16144. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D4FCh**

Figure 14-5342. EMIF_CTLCFG_DENALI_PHY_1343 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SC_PHY_PAD_DBG_CONT_0
NONE							W
0h							0h

Table 14-16146. EMIF_CTLCFG_DENALI_PHY_1343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SC_PHY_PAD_DBG_CONT_0	W	0h	Allows the pad calibration state machine to advance [when in debug mode] for slice 0. Set to 1 to trigger. WRITE-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1264 EMIF_CTLCFG_DENALI_PHY_1344 Register

1 EMIF_CTLCFG_DENALI_PHY_1344 Register (Offset = 5500h) [reset = 0h]

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Table 14-16147. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D500h**

Figure 14-5343. EMIF_CTLCFG_DENALI_PHY_1344 Name Register

31	30	29	28	27	26	25	24
PHY_CAL_RESULT3_OBS_0							
R							
0h							
23	22	21	20	19	18	17	16
PHY_CAL_RESULT3_OBS_0							
R							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_RESULT3_OBS_0							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_RESULT3_OBS_0							
R							
0h							

Table 14-16149. EMIF_CTLCFG_DENALI_PHY_1344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_CAL_RESULT3_OBS_0	R	0h	Pad calibration results first/last0/1 observation values for block 0. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1265 EMIF_CTLCFG_DENALI_PHY_1345 Register

1 EMIF_CTLCFG_DENALI_PHY_1345 Register (Offset = 5504h) [reset = 4102000h]

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Table 14-16150. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D504h**

Figure 14-5344. EMIF_CTLCFG_DENALI_PHY_1345 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CAL_SLOPE_ADJ_0			
NONE				R/W			
0h				41020h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CAL_SLOPE_ADJ_0							
R/W							
41020h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CAL_SLOPE_ADJ_0							
R/W							
41020h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_ADRCTL_PVT_MAP_0							
R/W							
0h							

Table 14-16152. EMIF_CTLCFG_DENALI_PHY_1345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:8	PHY_CAL_SLOPE_ADJ_0	R/W	41020h	defines slope configure in pad calibration process Reset Source: ctl_amod_g_rst_n
7:0	PHY_ADRCTL_PVT_MAP_0	R/W	0h	defines slope configure in pad calibration process Reset Source: ctl_amod_g_rst_n

14.5.1.2.1266 EMIF_CTLCFG_DENALI_PHY_1346 Register

1 EMIF_CTLCFG_DENALI_PHY_1346 Register (Offset = 5508h) [reset = 41020h]

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Table 14-16153. Instance Table

Instance Name	**Physical Address**
DDR16SS0	**0F30 D508h**

Figure 14-5345. EMIF_CTLCFG_DENALI_PHY_1346 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_CAL_SLOPE_ADJ_PASS2_0			
NONE				R/W			
0h				41020h			
15	14	13	12	11	10	9	8
PHY_CAL_SLOPE_ADJ_PASS2_0							
R/W							
41020h							
7	6	5	4	3	2	1	0
PHY_CAL_SLOPE_ADJ_PASS2_0							
R/W							
41020h							

Table 14-16155. EMIF_CTLCFG_DENALI_PHY_1346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	PHY_CAL_SLOPE_ADJ_PASS2_0	R/W	41020h	defines slope configure for pass2 in pad calibration process Reset Source: ctl_amod_g_rst_n

14.5.1.2.1267 EMIF_CTLCFG_DENALI_PHY_1347 Register

1 EMIF_CTLCFG_DENALI_PHY_1347 Register (Offset = 550Ch) [reset = C98C98h]

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Table 14-16156. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D50Ch**

Figure 14-5346. EMIF_CTLCFG_DENALI_PHY_1347 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CAL_TWO_PASS_CFG_0
NONE							R/W
0h							C98C98h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CAL_TWO_PASS_CFG_0							
R/W							
C98C98h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CAL_TWO_PASS_CFG_0							
R/W							
C98C98h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CAL_TWO_PASS_CFG_0							
R/W							
C98C98h							

Table 14-16158. EMIF_CTLCFG_DENALI_PHY_1347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:0	PHY_CAL_TWO_PASS_CFG_0	R/W	C98C98h	defines cal_en configure in pad calibration process Reset Source: ctl_amod_g_rst_n

14.5.1.2.1268 EMIF_CTLCFG_DENALI_PHY_1348 Register

1 EMIF_CTLCFG_DENALI_PHY_1348 Register (Offset = 5510h) [reset = 3F000000h]

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Table 14-16159. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D510h**

Figure 14-5347. EMIF_CTLCFG_DENALI_PHY_1348 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_CAL_RANGE_PASS1_PU_MAX_DELTA_0					
NONE		R/W					
0h		3Fh					
23	22	21	20	19	18	17	16
RESERVED	PHY_CAL_SW_CAL_CFG_0						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
PHY_CAL_SW_CAL_CFG_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_CAL_SW_CAL_CFG_0							
R/W							
0h							

Table 14-16161. EMIF_CTLCFG_DENALI_PHY_1348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_CAL_RANGE_PASS1_PU_MAX_DELTA_0	R/W	3Fh	Pad calibration pass1 pu results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n
23	RESERVED	NONE	0h	Reserved
22:0	PHY_CAL_SW_CAL_CFG_0	R/W	0h	defines firmware based pad calibration process Reset Source: ctl_amod_g_rst_n

14.5.1.2.1269 EMIF_CTLCFG_DENALI_PHY_1349 Register

1 EMIF_CTLCFG_DENALI_PHY_1349 Register (Offset = 5514h) [reset = 3F3F1F3Fh]

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Table 14-16162. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D514h**

Figure 14-5348. EMIF_CTLCFG_DENALI_PHY_1349 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_CAL_RANGE_PASS2_PD_MAX_DELTA_0					
NONE		R/W					
0h		3Fh					
23	22	21	20	19	18	17	16
RESERVED		PHY_CAL_RANGE_PASS2_PU_MAX_DELTA_0					
NONE		R/W					
0h		3Fh					
15	14	13	12	11	10	9	8
RESERVED			PHY_CAL_RANGE_PASS1_RX_MAX_DELTA_0				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED		PHY_CAL_RANGE_PASS1_PD_MAX_DELTA_0					
NONE		R/W					
0h		3Fh					

Table 14-16164. EMIF_CTLCFG_DENALI_PHY_1349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	PHY_CAL_RANGE_PASS2_PD_MAX_DELTA_0	R/W	3Fh	Pad calibration pass2 pd results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_CAL_RANGE_PASS2_PU_MAX_DELTA_0	R/W	3Fh	Pad calibration pass2 pu results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_CAL_RANGE_PASS1_RX_MAX_DELTA_0	R/W	1Fh	Pad calibration pass1 rx results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_CAL_RANGE_PASS1_PD_MAX_DELTA_0	R/W	3Fh	Pad calibration pass1 pd results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n

14.5.1.2.1270 EMIF_CTLCFG_DENALI_PHY_1350 Register

1 EMIF_CTLCFG_DENALI_PHY_1350 Register (Offset = 5518h) [reset = 1Fh]

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Table 14-16165. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D518h**

Figure 14-5349. EMIF_CTLCFG_DENALI_PHY_1350 Name Register

31	30	29	28	27	26	25	24
RESERVED			PHY_CAL_RANGE_PASS1_RX_MIN_DELTA_0				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PHY_CAL_RANGE_PASS1_PD_MIN_DELTA_0					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_CAL_RANGE_PASS1_PU_MIN_DELTA_0					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PHY_CAL_RANGE_PASS2_RX_MAX_DELTA_0				
NONE			R/W				
0h			1Fh				

Table 14-16167. EMIF_CTLCFG_DENALI_PHY_1350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PHY_CAL_RANGE_PASS1_RX_MIN_DELTA_0	R/W	0h	Pad calibration pass1 rx results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21:16	PHY_CAL_RANGE_PASS1_PD_MIN_DELTA_0	R/W	0h	Pad calibration pass1 pd results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_CAL_RANGE_PASS1_PU_MIN_DELTA_0	R/W	0h	Pad calibration pass1 pu results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	PHY_CAL_RANGE_PASS2_RX_MAX_DELTA_0	R/W	1Fh	Pad calibration pass2 rx results won't update if out of max delta range . Reset Source: ctl_amod_g_rst_n

14.5.1.2.1271 EMIF_CTLCFG_DENALI_PHY_1351 Register

1 EMIF_CTLCFG_DENALI_PHY_1351 Register (Offset = 551Ch) [reset = 0h]

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Table 14-16168. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D51Ch**

Figure 14-5350. EMIF_CTLCFG_DENALI_PHY_1351 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_CAL_RANGE_PASS2_RX_MIN_DELTA_0				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PHY_CAL_RANGE_PASS2_PD_MIN_DELTA_0					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PHY_CAL_RANGE_PASS2_PU_MIN_DELTA_0					
NONE		R/W					
0h		0h					

Table 14-16170. EMIF_CTLCFG_DENALI_PHY_1351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PHY_CAL_RANGE_PASS2_RX_MIN_DELTA_0	R/W	0h	Pad calibration pass2 rx results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	PHY_CAL_RANGE_PASS2_PD_MIN_DELTA_0	R/W	0h	Pad calibration pass2 pd results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_CAL_RANGE_PASS2_PU_MIN_DELTA_0	R/W	0h	Pad calibration pass2 pu results won't update if out of min delta range . Reset Source: ctl_amod_g_rst_n

14.5.1.2.1272 EMIF_CTLCFG_DENALI_PHY_1352 Register

1 EMIF_CTLCFG_DENALI_PHY_1352 Register (Offset = 5520h) [reset = 0h]

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Table 14-16171. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D520h**

Figure 14-5351. EMIF_CTLCFG_DENALI_PHY_1352 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_AC_LPBK_ERR_CLEAR</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PHY_ADRCTL_MANUAL_UPDATE</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_PAD_ATB_CTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PHY_PAD_ATB_CTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16173. EMIF_CTLCFG_DENALI_PHY_1352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_AC_LPBK_ERR_CLEAR	W	0h	Address/control loopback error clear. Set to 1 to clear error. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_ADRCTL_MANUAL_UPDATE	W	0h	Address/control manual update of target delay lines. Set to 1 to update. WRITE-ONLY Reset Source: ctl_amod_g_rst_n
15:0	PHY_PAD_ATB_CTRL	R/W	0h	Pad ATB control settings. Bit [0] is the enable signal. Bits [5:1] are the ATB data signals. Bits [15:8] are the 1 hot select for which pad is selected. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1273 EMIF_CTLCFG_DENALI_PHY_1353 Register

1 EMIF_CTLCFG_DENALI_PHY_1353 Register (Offset = 5524h) [reset = 0h]

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Table 14-16174. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D524h**

Figure 14-5352. EMIF_CTLCFG_DENALI_PHY_1353 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_AC_LPBK _CONTROL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
PHY_AC_LPBK_CONTROL							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_AC_LPBK_ENABLE			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED						PHY_AC_LPBK_OBS_SELECT	
NONE						R/W	
0h						0h	

Table 14-16176. EMIF_CTLCFG_DENALI_PHY_1353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	PHY_AC_LPBK_CONTROL	R/W	0h	Address/control slice loopback control setting. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	PHY_AC_LPBK_ENABLE	R/W	0h	Loopback enable for the address/control slices. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_AC_LPBK_OBS_SELECT	R/W	0h	Select value to map an individual loopback address/control slice observation register to the global observation register. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1274 EMIF_CTLCFG_DENALI_PHY_1354 Register

1 EMIF_CTLCFG_DENALI_PHY_1354 Register (Offset = 5528h) [reset = 1h]

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Table 14-16177. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D528h**

Figure 14-5353. EMIF_CTLCFG_DENALI_PHY_1354 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_AC_PRBS_PATTERN_MASK			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED	PHY_AC_PRBS_PATTERN_START						
NONE	R/W						
0h	1h						

Table 14-16179. EMIF_CTLCFG_DENALI_PHY_1354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	PHY_AC_PRBS_PATTERN_MASK	R/W	0h	PRBS7 mask signal for address/control slice. Reset Source: ctl_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PHY_AC_PRBS_PATTERN_START	R/W	1h	PRBS7 start pattern for address/control slice. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1275 EMIF_CTLCFG_DENALI_PHY_1355 Register

1 EMIF_CTLCFG_DENALI_PHY_1355 Register (Offset = 552Ch) [reset = 0h]

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Table 14-16180. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D52Ch**

Figure 14-5354. EMIF_CTLCFG_DENALI_PHY_1355 Name Register

31	30	29	28	27	26	25	24
PHY_AC_LPBK_RESULT_OBS							
R							
0h							
23	22	21	20	19	18	17	16
PHY_AC_LPBK_RESULT_OBS							
R							
0h							
15	14	13	12	11	10	9	8
PHY_AC_LPBK_RESULT_OBS							
R							
0h							
7	6	5	4	3	2	1	0
PHY_AC_LPBK_RESULT_OBS							
R							
0h							

Table 14-16182. EMIF_CTLCFG_DENALI_PHY_1355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_AC_LPBK_RESULT_OBS	R	0h	Observation register for the loopback address/control slices. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1276 EMIF_CTLCFG_DENALI_PHY_1356 Register

1 EMIF_CTLCFG_DENALI_PHY_1356 Register (Offset = 5530h) [reset = 0h]

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Table 14-16183. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D530h

Figure 14-5355. EMIF_CTLCFG_DENALI_PHY_1356 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_AC_CLK_LPBK_CONTROL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED							PHY_AC_CLK_LPBK_ENABLE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							PHY_AC_CLK_LPBK_OBS_SELECT
NONE							R/W
0h							0h

Table 14-16185. EMIF_CTLCFG_DENALI_PHY_1356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PHY_AC_CLK_LPBK_CONTROL	R/W	0h	Mem clk block loopback control setting. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_AC_CLK_LPBK_ENABLE	R/W	0h	Loopback enable for mem clk blocks. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_AC_CLK_LPBK_OBS_SELECT	R/W	0h	Select value to map an individual loopback mem clk block observation register to the global observation register. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1277 EMIF_CTLCFG_DENALI_PHY_1357 Register

1 EMIF_CTLCFG_DENALI_PHY_1357 Register (Offset = 5534h) [reset = 0h]

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Table 14-16186. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D534h

Figure 14-5356. EMIF_CTLCFG_DENALI_PHY_1357 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_TOP_PWR_RDC_DISABLE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_AC_PWR_RDC_DISABLE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_AC_CLK_LPBK_RESULT_OBS							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_AC_CLK_LPBK_RESULT_OBS							
R							
0h							

Table 14-16188. EMIF_CTLCFG_DENALI_PHY_1357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_TOP_PWR_RDC_DISABLE	R/W	0h	top param power reduction disable. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_AC_PWR_RDC_DISABLE	R/W	0h	ac slice power reduction disable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_AC_CLK_LPBK_RESULT_OBS	R	0h	Observation register for loopback mem clk blocks. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1278 EMIF_CTLCFG_DENALI_PHY_1358 Register

1 EMIF_CTLCFG_DENALI_PHY_1358 Register (Offset = 5538h) [reset = 0h]

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Table 14-16189. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D538h**

Figure 14-5357. EMIF_CTLCFG_DENALI_PHY_1358 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_AC_SLV_DLY_CTRL_GATE_DISABLE
NONE							R/W
0h							0h

Table 14-16191. EMIF_CTLCFG_DENALI_PHY_1358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_AC_SLV_DLY_CTRL_GATE_DISABLE	R/W	0h	ac slice slv_dly_control block power reduction disable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1279 EMIF_CTLCFG_DENALI_PHY_1359 Register

1 EMIF_CTLCFG_DENALI_PHY_1359 Register (Offset = 553Ch) [reset = 0h]

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Table 14-16192. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D53Ch**

Figure 14-5358. EMIF_CTLCFG_DENALI_PHY_1359 Name Register

31	30	29	28	27	26	25	24
PHY_DATA_BYTE_ORDER_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DATA_BYTE_ORDER_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DATA_BYTE_ORDER_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DATA_BYTE_ORDER_SEL							
R/W							
0h							

Table 14-16194. EMIF_CTLCFG_DENALI_PHY_1359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DATA_BYTE_ORDER_SEL	R/W	0h	Used to define the data slice's byte swap for CA bits 7:0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1280 EMIF_CTLCFG_DENALI_PHY_1360 Register

1 EMIF_CTLCFG_DENALI_PHY_1360 Register (Offset = 5540h) [reset = 0h]

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Table 14-16195. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D540h**

Figure 14-5359. EMIF_CTLCFG_DENALI_PHY_1360 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_0	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED					PHY_ADR_DISABLE		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED			PHY_CALVL_DEVICE_MAP				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PHY_DATA_BYTE_ORDER_SEL_HIGH							
R/W							
0h							

Table 14-16197. EMIF_CTLCFG_DENALI_PHY_1360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_ADRCTL_MSTR_DLY_ENC_SEL_0	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 0 . Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ADR_DISABLE	R/W	0h	Disable the unused adr slice to save power. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	PHY_CALVL_DEVICE_MAP	R/W	0h	Define which device's DQ feedback data bits should be used during CA training Reset Source: ctl_amod_g_rst_n
7:0	PHY_DATA_BYTE_ORDER_SEL_HIGH	R/W	0h	Used to define the data slice's byte swap for CA bits 9:8. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1281 EMIF_CTLCFG_DENALI_PHY_1361 Register

1 EMIF_CTLCFG_DENALI_PHY_1361 Register (Offset = 5544h) [reset = 0h]

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Table 14-16198. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D544h**

Figure 14-5360. EMIF_CTLCFG_DENALI_PHY_1361 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_3	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_2	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_1	
NONE						R/W	
0h						0h	

Table 14-16200. EMIF_CTLCFG_DENALI_PHY_1361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PHY_ADRCTL_MSTR_DLY_ENC_SEL_3	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 3 . Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:8	PHY_ADRCTL_MSTR_DLY_ENC_SEL_2	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 2 . Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_ADRCTL_MSTR_DLY_ENC_SEL_1	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 1 . Reset Source: ctl_amod_g_rst_n

14.5.1.2.1282 EMIF_CTLCFG_DENALI_PHY_1362 Register

1 EMIF_CTLCFG_DENALI_PHY_1362 Register (Offset = 5548h) [reset = 0h]

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Table 14-16201. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D548h**

Figure 14-5361. EMIF_CTLCFG_DENALI_PHY_1362 Name Register

31	30	29	28	27	26	25	24
PHY_DDL_AC_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_DDL_AC_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_DDL_AC_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_DDL_AC_ENABLE							
R/W							
0h							

Table 14-16203. EMIF_CTLCFG_DENALI_PHY_1362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DDL_AC_ENABLE	R/W	0h	PHY Address/Control DDL BIST mode enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1283 EMIF_CTLCFG_DENALI_PHY_1363 Register

1 EMIF_CTLCFG_DENALI_PHY_1363 Register (Offset = 554Ch) [reset = 0h]

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Table 14-16204. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D54Ch**

Figure 14-5362. EMIF_CTLCFG_DENALI_PHY_1363 Name Register

31	30	29	28	27	26	25	24
RESERVED						PHY_DDL_AC_MODE	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_DDL_AC_MODE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_DDL_AC_MODE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_DDL_AC_MODE							
R/W							
0h							

Table 14-16206. EMIF_CTLCFG_DENALI_PHY_1363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:0	PHY_DDL_AC_MODE	R/W	0h	PHY Address/Control DDL BIST mode. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1284 EMIF_CTLCFG_DENALI_PHY_1364 Register

1 EMIF_CTLCFG_DENALI_PHY_1364 Register (Offset = 5550h) [reset = 0h]

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Table 14-16207. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D550h**

Figure 14-5363. EMIF_CTLCFG_DENALI_PHY_1364 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PHY_DDL_TRACK_UPD_THRESHOLD_AC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PHY_INIT_UPDATE_CONFIG</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PHY_DDL_AC_MASK</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-16209. EMIF_CTLCFG_DENALI_PHY_1364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PHY_DDL_TRACK_UPD_THRESHOLD_AC	R/W	0h	Specify threshold value for PHY init update tracking for AC slice. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:8	PHY_INIT_UPDATE_CONFIG	R/W	0h	PHY init update function configuration. Reset Source: ctl_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	PHY_DDL_AC_MASK	R/W	0h	PHY Address/Control DDL BIST mask. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1285 EMIF_CTLCFG_DENALI_PHY_1365 Register

1 EMIF_CTLCFG_DENALI_PHY_1365 Register (Offset = 5554h) [reset = 0h]

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Table 14-16210. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D554h**

Figure 14-5364. EMIF_CTLCFG_DENALI_PHY_1365 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ERR_STATUS		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					PHY_ERR_MASK_EN		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CA_PARITY_ERR_PULSE_MIN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CA_PARITY_ERR_PULSE_MIN							
R/W							
0h							

Table 14-16212. EMIF_CTLCFG_DENALI_PHY_1365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	PHY_ERR_STATUS	R/W	0h	PHY ERROR information. Reset Source: ctl_amod_g_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	PHY_ERR_MASK_EN	R/W	0h	PHY ERROR information report mask enable. Reset Source: ctl_amod_g_rst_n
15:0	PHY_CA_PARITY_ERR_PULSE_MIN	R/W	0h	PHY alert_n pulse width minimux value for CA parity error. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1286 EMIF_CTLCFG_DENALI_PHY_1366 Register

1 EMIF_CTLCFG_DENALI_PHY_1366 Register (Offset = 5558h) [reset = 0h]

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Table 14-16213. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D558h**

Figure 14-5365. EMIF_CTLCFG_DENALI_PHY_1366 Name Register

31	30	29	28	27	26	25	24
PHY_DS0_DQS_ERR_COUNTER							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DS0_DQS_ERR_COUNTER							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DS0_DQS_ERR_COUNTER							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DS0_DQS_ERR_COUNTER							
R							
0h							

Table 14-16215. EMIF_CTLCFG_DENALI_PHY_1366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DS0_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 0 DQS ERROR counter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1287 EMIF_CTLCFG_DENALI_PHY_1367 Register

1 EMIF_CTLCFG_DENALI_PHY_1367 Register (Offset = 555Ch) [reset = 0h]

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Table 14-16216. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D55Ch**

Figure 14-5366. EMIF_CTLCFG_DENALI_PHY_1367 Name Register

31	30	29	28	27	26	25	24
PHY_DS1_DQS_ERR_COUNTER							
R							
0h							
23	22	21	20	19	18	17	16
PHY_DS1_DQS_ERR_COUNTER							
R							
0h							
15	14	13	12	11	10	9	8
PHY_DS1_DQS_ERR_COUNTER							
R							
0h							
7	6	5	4	3	2	1	0
PHY_DS1_DQS_ERR_COUNTER							
R							
0h							

Table 14-16218. EMIF_CTLCFG_DENALI_PHY_1367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_DS1_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 1 DQS ERROR counter. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1288 EMIF_CTLCFG_DENALI_PHY_1368 Register

1 EMIF_CTLCFG_DENALI_PHY_1368 Register (Offset = 5560h) [reset = 2h]

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Table 14-16219. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D560h**

Figure 14-5367. EMIF_CTLCFG_DENALI_PHY_1368 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_DS_INIT_COMPLETE_OBS</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PHY_AC_INIT_COMPLETE_OBS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_AC_INIT_COMPLETE_OBS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PHY_DLL_RST_EN</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">2h</td></tr>
</table>

Table 14-16221. EMIF_CTLCFG_DENALI_PHY_1368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	PHY_DS_INIT_COMPLETE_OBS	R	0h	Observation register for dfi_init_complete for data slice. Bit0 is for data_slice0; bit1 is for data_slice 1,... READ-ONLY. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:8	PHY_AC_INIT_COMPLETE_OBS	R	0h	Observation register for dfi_init_complete for adr and ac slice. Bit 0 is for dfi_init_complete for all slices. Bit[7:4] is for adr slice, bit4 is adr_slice0..., if the adr slice number is 3, bit7 is 0. Bit8 is for ac_slice0; bit9 is for ac_slice 1,... READ-ONLY. Reset Source: ctl_amod_g_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PHY_DLL_RST_EN	R/W	2h	PHY DDL reset software interface enable. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1289 EMIF_CTLCFG_DENALI_PHY_1369 Register

1 EMIF_CTLCFG_DENALI_PHY_1369 Register (Offset = 5564h) [reset = 0h]

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Table 14-16222. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D564h

Figure 14-5368. EMIF_CTLCFG_DENALI_PHY_1369 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GRP_SHIFT_OBS_SELECT			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PHY_GRP_SLV_DLY_ENC_OBS_SELECT				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PHY_ERR_IE
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PHY_UPDATE_MASK
NONE							R/W
0h							0h

Table 14-16224. EMIF_CTLCFG_DENALI_PHY_1369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_GRP_SHIFT_OBS_SELECT	R/W	0h	Select value to map an individual address/control group slice automatic cycle/half_cycle shift settings to the observation register. Reset Source: ctl_amod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20:16	PHY_GRP_SLV_DLY_ENC_OBS_SELECT	R/W	0h	Select value to map an individual address/control group slice target delay to the encoded value observation register. Reset Source: ctl_amod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	PHY_ERR_IE	R/W	0h	Control the IE signal of IO error pad. Reset Source: ctl_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	PHY_UPDATE_MASK	R/W	0h	Control to disable the generation of dfi_phyupd_req and use of dfi_ctrlupd_req. If this is 0 the PHY is normal mode; if this is 1, the PHY will not respond to dfi_ctrlupd_req or not to send dfi_phyupd_req Reset Source: ctl_amod_g_rst_n

14.5.1.2.1290 EMIF_CTLCFG_DENALI_PHY_1370 Register

1 EMIF_CTLCFG_DENALI_PHY_1370 Register (Offset = 5568h) [reset = 0h]

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Table 14-16225. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D568h**

Figure 14-5369. EMIF_CTLCFG_DENALI_PHY_1370 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_GRP_SHIFT_OBS		
NONE					R		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED					PHY_GRP_SLV_DLY_ENC_OBS		
NONE					R		
0h					0h		
7	6	5	4	3	2	1	0
PHY_GRP_SLV_DLY_ENC_OBS							
R							
0h							

Table 14-16227. EMIF_CTLCFG_DENALI_PHY_1370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_GRP_SHIFT_OBS	R	0h	Observation register for the address/control group automatic half cycle and cycle shift values. READ-ONLY Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP_SLV_DLY_ENC_OBS	R	0h	Observation register for all address/control group slice target delay encoded values. READ-ONLY Reset Source: ctl_amod_g_rst_n

14.5.1.2.1291 EMIF_CTLCFG_DENALI_PHY_1371 Register

1 EMIF_CTLCFG_DENALI_PHY_1371 Register (Offset = 556Ch) [reset = 0h]

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Table 14-16228. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D56Ch**

Figure 14-5370. EMIF_CTLCFG_DENALI_PHY_1371 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_PAD_CAL_IO_CFG_0	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
PHY_PAD_CAL_IO_CFG_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_PAD_CAL_IO_CFG_0							
R/W							
0h							

Table 14-16230. EMIF_CTLCFG_DENALI_PHY_1371 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_CAL_IO_CFG_0	R/W	0h	Pad calibration Controls PCLK/PARK pin and vref switch. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1292 EMIF_CTLCFG_DENALI_PHY_1372 Register

1 EMIF_CTLCFG_DENALI_PHY_1372 Register (Offset = 5570h) [reset = 0h]

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Table 14-16231. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D570h**

Figure 14-5371. EMIF_CTLCFG_DENALI_PHY_1372 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_PAD_ACS_RX_PCLK_CLK_SEL		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
PHY_PAD_ACS_IO_CFG							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_PAD_ACS_IO_CFG							
R/W							
0h							

Table 14-16233. EMIF_CTLCFG_DENALI_PHY_1372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	PHY_PAD_ACS_RX_PCLK_CLK_SEL	R/W	0h	Controls rx_pclk clk selection for acs pad. Reset Source: ctl_amod_g_rst_n
15:0	PHY_PAD_ACS_IO_CFG	R/W	0h	Controls PCLK/PARK pin for acs pad. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1293 EMIF_CTLCFG_DENALI_PHY_1373 Register

1 EMIF_CTLCFG_DENALI_PHY_1373 Register (Offset = 5574h) [reset = 0h]

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Table 14-16234. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D574h**

Figure 14-5372. EMIF_CTLCFG_DENALI_PHY_1373 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_PLL_BYPASS
NONE							R/W
0h							0h

Table 14-16236. EMIF_CTLCFG_DENALI_PHY_1373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PHY_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1294 EMIF_CTLCFG_DENALI_PHY_1374 Register

1 EMIF_CTLCFG_DENALI_PHY_1374 Register (Offset = 5578h) [reset = 0h]

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Table 14-16237. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D578h**

Figure 14-5373. EMIF_CTLCFG_DENALI_PHY_1374 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_LOW_FREQ_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED			PHY_PLL_CTRL				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
PHY_PLL_CTRL							
R/W							
0h							

Table 14-16239. EMIF_CTLCFG_DENALI_PHY_1374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PHY_LOW_FREQ_SEL	R/W	0h	Enables the PHY to enter/exit the PLL domain from the negative clock edge. Set to 1 at low frequencies to enable. Reset Source: ctl_amod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:0	PHY_PLL_CTRL	R/W	0h	PHY clock PLL controls. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1295 EMIF_CTLCFG_DENALI_PHY_1375 Register

1 EMIF_CTLCFG_DENALI_PHY_1375 Register (Offset = 557Ch) [reset = 0h]

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Table 14-16240. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D57Ch**

Figure 14-5374. EMIF_CTLCFG_DENALI_PHY_1375 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CSLVL_DLY_STEP			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CSLVL_CAPTURE_CNT			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_VREF_CTRL_AC			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PHY_PAD_VREF_CTRL_AC							
R/W							
0h							

Table 14-16242. EMIF_CTLCFG_DENALI_PHY_1375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	PHY_CSLVL_DLY_STEP	R/W	0h	Sets the delay step size plus 1 during CS training. Reset Source: ctl_amod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved
19:16	PHY_CSLVL_CAPTURE_CNT	R/W	0h	Defines the number of samples to take at each GRP target delay setting during CS training. Reset Source: ctl_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	PHY_PAD_VREF_CTRL_AC	R/W	0h	Pad VREF control settings for the address/control. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1296 EMIF_CTLCFG_DENALI_PHY_1376 Register

1 EMIF_CTLCFG_DENALI_PHY_1376 Register (Offset = 5580h) [reset = 0h]

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Table 14-16243. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D580h

Figure 14-5375. EMIF_CTLCFG_DENALI_PHY_1376 Name Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LVL_MEAS_DLY_STEP_ENABLE
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PHY_SW_CSLVL_DVW_MIN_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PHY_SW_CSLVL_DVW_MIN	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_SW_CSLVL_DVW_MIN							
R/W							
0h							

Table 14-16245. EMIF_CTLCFG_DENALI_PHY_1376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	PHY_LVL_MEAS_DLY_STEP_ENABLE	R/W	0h	Enables the phy_adr_meas_dly_step_value to be used instead of the phy_cslvl_dly_step parameter. Reset Source: ctl_amod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PHY_SW_CSLVL_DVW_MIN_EN	R/W	0h	Enables the software override data valid window size during CS training. Reset Source: ctl_amod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	PHY_SW_CSLVL_DVW_MIN	R/W	0h	Sets the software override data valid window size during CS training. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1297 EMIF_CTLCFG_DENALI_PHY_1377 Register

1 EMIF_CTLCFG_DENALI_PHY_1377 Register (Offset = 5584h) [reset = 0h]

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Table 14-16246. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D584h**

Figure 14-5376. EMIF_CTLCFG_DENALI_PHY_1377 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP1_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP1_SLAVE_DELAY_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP0_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP0_SLAVE_DELAY_0							
R/W							
0h							

Table 14-16248. EMIF_CTLCFG_DENALI_PHY_1377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP1_SLAVE_DELAY_0	R/W	0h	Address slice target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP0_SLAVE_DELAY_0	R/W	0h	Address slice target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1298 EMIF_CTLCFG_DENALI_PHY_1378 Register

1 EMIF_CTLCFG_DENALI_PHY_1378 Register (Offset = 5588h) [reset = 0h]

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Table 14-16249. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D588h**

Figure 14-5377. EMIF_CTLCFG_DENALI_PHY_1378 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP3_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_GRP3_SLAVE_DELAY_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_GRP2_SLAVE_DELAY_0		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_GRP2_SLAVE_DELAY_0							
R/W							
0h							

Table 14-16251. EMIF_CTLCFG_DENALI_PHY_1378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP3_SLAVE_DELAY_0	R/W	0h	Address slice target delay setting for address slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP2_SLAVE_DELAY_0	R/W	0h	Address slice target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1299 EMIF_CTLCFG_DENALI_PHY_1379 Register

1 EMIF_CTLCFG_DENALI_PHY_1379 Register (Offset = 558Ch) [reset = 0h]

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Table 14-16252. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D58Ch**

Figure 14-5378. EMIF_CTLCFG_DENALI_PHY_1379 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP1_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
PHY_GRP1_SLAVE_DELAY_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_GRP0_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_GRP0_SLAVE_DELAY_1							
R/W							
0h							

Table 14-16254. EMIF_CTLCFG_DENALI_PHY_1379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP1_SLAVE_DELAY_1	R/W	0h	Address slice target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP0_SLAVE_DELAY_1	R/W	0h	Address slice target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1300 EMIF_CTLCFG_DENALI_PHY_1380 Register

1 EMIF_CTLCFG_DENALI_PHY_1380 Register (Offset = 5590h) [reset = 0h]

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Table 14-16255. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D590h

Figure 14-5379. EMIF_CTLCFG_DENALI_PHY_1380 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP3_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP3_SLAVE_DELAY_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP2_SLAVE_DELAY_1		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP2_SLAVE_DELAY_1							
R/W							
0h							

Table 14-16257. EMIF_CTLCFG_DENALI_PHY_1380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP3_SLAVE_DELAY_1	R/W	0h	Address slice target delay setting for address slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP2_SLAVE_DELAY_1	R/W	0h	Address slice target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1301 EMIF_CTLCFG_DENALI_PHY_1381 Register

1 EMIF_CTLCFG_DENALI_PHY_1381 Register (Offset = 5594h) [reset = 0h]

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Table 14-16258. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D594h**

Figure 14-5380. EMIF_CTLCFG_DENALI_PHY_1381 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP1_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP1_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP0_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP0_SLAVE_DELAY_2							
R/W							
0h							

Table 14-16260. EMIF_CTLCFG_DENALI_PHY_1381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP1_SLAVE_DELAY_2	R/W	0h	Address slice target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP0_SLAVE_DELAY_2	R/W	0h	Address slice target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1302 EMIF_CTLCFG_DENALI_PHY_1382 Register

1 EMIF_CTLCFG_DENALI_PHY_1382 Register (Offset = 5598h) [reset = 0h]

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Table 14-16261. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D598h**

Figure 14-5381. EMIF_CTLCFG_DENALI_PHY_1382 Name Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP3_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_GRP3_SLAVE_DELAY_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP2_SLAVE_DELAY_2		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP2_SLAVE_DELAY_2							
R/W							
0h							

Table 14-16263. EMIF_CTLCFG_DENALI_PHY_1382 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:16	PHY_GRP3_SLAVE_DELAY_2	R/W	0h	Address slice target delay setting for address slice 3. Reset Source: ctl_amod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP2_SLAVE_DELAY_2	R/W	0h	Address slice target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1303 EMIF_CTLCFG_DENALI_PHY_1383 Register

1 EMIF_CTLCFG_DENALI_PHY_1383 Register (Offset = 559Ch) [reset = 0h]

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Table 14-16264. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D59Ch**

Figure 14-5382. EMIF_CTLCFG_DENALI_PHY_1383 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP0_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP0_SLAVE_DELAY_3							
R/W							
0h							

Table 14-16266. EMIF_CTLCFG_DENALI_PHY_1383 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP0_SLAVE_DELAY_3	R/W	0h	Address slice target delay setting for address slice 0. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1304 EMIF_CTLCFG_DENALI_PHY_1384 Register

1 EMIF_CTLCFG_DENALI_PHY_1384 Register (Offset = 55A0h) [reset = 0h]

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Table 14-16267. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5A0h**

Figure 14-5383. EMIF_CTLCFG_DENALI_PHY_1384 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_GRP1_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_GRP1_SLAVE_DELAY_3							
R/W							
0h							

Table 14-16269. EMIF_CTLCFG_DENALI_PHY_1384 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP1_SLAVE_DELAY_3	R/W	0h	Address slice target delay setting for address slice 1. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1305 EMIF_CTLCFG_DENALI_PHY_1385 Register

1 EMIF_CTLCFG_DENALI_PHY_1385 Register (Offset = 55A4h) [reset = 0h]

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Table 14-16270. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D5A4h

Figure 14-5384. EMIF_CTLCFG_DENALI_PHY_1385 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PHY_GRP2_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_GRP2_SLAVE_DELAY_3							
R/W							
0h							

Table 14-16272. EMIF_CTLCFG_DENALI_PHY_1385 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP2_SLAVE_DELAY_3	R/W	0h	Address slice target delay setting for address slice 2. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1306 EMIF_CTLCFG_DENALI_PHY_1386 Register

1 EMIF_CTLCFG_DENALI_PHY_1386 Register (Offset = 55A8h) [reset = 0h]

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Table 14-16273. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5A8h**

Figure 14-5385. EMIF_CTLCFG_DENALI_PHY_1386 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_GRP3_SLAVE_DELAY_3		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PHY_GRP3_SLAVE_DELAY_3							
R/W							
0h							

Table 14-16275. EMIF_CTLCFG_DENALI_PHY_1386 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	PHY_GRP3_SLAVE_DELAY_3	R/W	0h	Address slice target delay setting for address slice 3. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1307 EMIF_CTLCFG_DENALI_PHY_1387 Register

1 EMIF_CTLCFG_DENALI_PHY_1387 Register (Offset = 55ACh) [reset = FFh]

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Table 14-16276. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5ACh**

Figure 14-5386. EMIF_CTLCFG_DENALI_PHY_1387 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_FDBK_DRIVE					
NONE		R/W					
0h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_FDBK_DRIVE							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_FDBK_DRIVE							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_FDBK_DRIVE							
R/W							
FFh							

Table 14-16278. EMIF_CTLCFG_DENALI_PHY_1387 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_FDBK_DRIVE	R/W	FFh	Controls drive settings for gate feedback pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1308 EMIF_CTLCFG_DENALI_PHY_1388 Register

1 EMIF_CTLCFG_DENALI_PHY_1388 Register (Offset = 55B0h) [reset = FFh]

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Table 14-16279. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5B0h**

Figure 14-5387. EMIF_CTLCFG_DENALI_PHY_1388 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PHY_PAD_FDBK_DRIVE2	
NONE						R/W	
0h						FFh	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_FDBK_DRIVE2							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_FDBK_DRIVE2							
R/W							
FFh							

Table 14-16281. EMIF_CTLCFG_DENALI_PHY_1388 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:0	PHY_PAD_FDBK_DRIVE2	R/W	FFh	Controls drive settings [enslice/boost] for gate feedback pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1309 EMIF_CTLCFG_DENALI_PHY_1389 Register

1 EMIF_CTLCFG_DENALI_PHY_1389 Register (Offset = 55B4h) [reset = 0h]

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Table 14-16282. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5B4h**

Figure 14-5388. EMIF_CTLCFG_DENALI_PHY_1389 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_PAD_DATA_DRIVE						
NONE	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_DATA_DRIVE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_DATA_DRIVE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_DATA_DRIVE							
R/W							
0h							

Table 14-16284. EMIF_CTLCFG_DENALI_PHY_1389 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:0	PHY_PAD_DATA_DRIVE	R/W	0h	Controls drive settings for data pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1310 EMIF_CTLCFG_DENALI_PHY_1390 Register

1 EMIF_CTLCFG_DENALI_PHY_1390 Register (Offset = 55B8h) [reset = 0h]

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Table 14-16285. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5B8h**

Figure 14-5389. EMIF_CTLCFG_DENALI_PHY_1390 Name Register

31	30	29	28	27	26	25	24
PHY_PAD_DQS_DRIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
PHY_PAD_DQS_DRIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_PAD_DQS_DRIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
PHY_PAD_DQS_DRIVE							
R/W							
0h							

Table 14-16287. EMIF_CTLCFG_DENALI_PHY_1390 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_PAD_DQS_DRIVE	R/W	0h	Controls drive settings for dqs pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1311 EMIF_CTLCFG_DENALI_PHY_1391 Register

1 EMIF_CTLCFG_DENALI_PHY_1391 Register (Offset = 55BCh) [reset = FFh]

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Table 14-16288. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5BCh**

Figure 14-5390. EMIF_CTLCFG_DENALI_PHY_1391 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_ADDR_DRIVE					
NONE		R/W					
0h		FFh					
23	22	21	20	19	18	17	16
PHY_PAD_ADDR_DRIVE							
R/W							
FFh							
15	14	13	12	11	10	9	8
PHY_PAD_ADDR_DRIVE							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_ADDR_DRIVE							
R/W							
FFh							

Table 14-16290. EMIF_CTLCFG_DENALI_PHY_1391 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_ADDR_DRIVE	R/W	FFh	Controls drive settings for the address/control pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1312 EMIF_CTLCFG_DENALI_PHY_1392 Register

1 EMIF_CTLCFG_DENALI_PHY_1392 Register (Offset = 55C0h) [reset = FFFF00h]

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Table 14-16291. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5C0h**

Figure 14-5391. EMIF_CTLCFG_DENALI_PHY_1392 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_ADDR_DRIVE2			
NONE				R/W			
0h				FFFF00h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ADDR_DRIVE2							
R/W							
FFFF00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ADDR_DRIVE2							
R/W							
FFFF00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ADDR_DRIVE2							
R/W							
FFFF00h							

Table 14-16293. EMIF_CTLCFG_DENALI_PHY_1392 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_ADDR_DRIVE2	R/W	FFFF00h	Controls drive settings for the address/control pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1313 EMIF_CTLCFG_DENALI_PHY_1393 Register

1 EMIF_CTLCFG_DENALI_PHY_1393 Register (Offset = 55C4h) [reset = FFh]

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Table 14-16294. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D5C4h

Figure 14-5392. EMIF_CTLCFG_DENALI_PHY_1393 Name Register

31	30	29	28	27	26	25	24
PHY_PAD_CLK_DRIVE							
R/W							
FFh							
23	22	21	20	19	18	17	16
PHY_PAD_CLK_DRIVE							
R/W							
FFh							
15	14	13	12	11	10	9	8
PHY_PAD_CLK_DRIVE							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_CLK_DRIVE							
R/W							
FFh							

Table 14-16296. EMIF_CTLCFG_DENALI_PHY_1393 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PHY_PAD_CLK_DRIVE	R/W	FFh	Controls drive settings for clock pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1314 EMIF_CTLCFG_DENALI_PHY_1394 Register

1 EMIF_CTLCFG_DENALI_PHY_1394 Register (Offset = 55C8h) [reset = FFh]

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Table 14-16297. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5C8h**

Figure 14-5393. EMIF_CTLCFG_DENALI_PHY_1394 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					PHY_PAD_CLK_DRIVE2		
NONE					R/W		
0h					FFh		
15	14	13	12	11	10	9	8
PHY_PAD_CLK_DRIVE2							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_CLK_DRIVE2							
R/W							
FFh							

Table 14-16299. EMIF_CTLCFG_DENALI_PHY_1394 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:0	PHY_PAD_CLK_DRIVE2	R/W	FFh	Controls drive settings for clock pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1315 EMIF_CTLCFG_DENALI_PHY_1395 Register

1 EMIF_CTLCFG_DENALI_PHY_1395 Register (Offset = 55CCh) [reset = FFh]

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Table 14-16300. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5CCh**

Figure 14-5394. EMIF_CTLCFG_DENALI_PHY_1395 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_ERR_DRIVE					
NONE		R/W					
0h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ERR_DRIVE							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ERR_DRIVE							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ERR_DRIVE							
R/W							
FFh							

Table 14-16302. EMIF_CTLCFG_DENALI_PHY_1395 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_ERR_DRIVE	R/W	FFh	Controls drive settings for error pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1316 EMIF_CTLCFG_DENALI_PHY_1396 Register

1 EMIF_CTLCFG_DENALI_PHY_1396 Register (Offset = 55D0h) [reset = FFFF00h]

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Table 14-16303. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D5D0h

Figure 14-5395. EMIF_CTLCFG_DENALI_PHY_1396 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_ERR_DRIVE2			
NONE				R/W			
0h				FFFF00h			
23	22	21	20	19	18	17	16
PHY_PAD_ERR_DRIVE2							
R/W							
FFFF00h							
15	14	13	12	11	10	9	8
PHY_PAD_ERR_DRIVE2							
R/W							
FFFF00h							
7	6	5	4	3	2	1	0
PHY_PAD_ERR_DRIVE2							
R/W							
FFFF00h							

Table 14-16305. EMIF_CTLCFG_DENALI_PHY_1396 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_ERR_DRIVE2	R/W	FFFF00h	Controls drive settings for error pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1317 EMIF_CTLCFG_DENALI_PHY_1397 Register

1 EMIF_CTLCFG_DENALI_PHY_1397 Register (Offset = 55D4h) [reset = FFh]

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Table 14-16306. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5D4h**

Figure 14-5396. EMIF_CTLCFG_DENALI_PHY_1397 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_CKE_DRIVE					
NONE		R/W					
0h		FFh					
23	22	21	20	19	18	17	16
PHY_PAD_CKE_DRIVE							
R/W							
FFh							
15	14	13	12	11	10	9	8
PHY_PAD_CKE_DRIVE							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_CKE_DRIVE							
R/W							
FFh							

Table 14-16308. EMIF_CTLCFG_DENALI_PHY_1397 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_CKE_DRIVE	R/W	FFh	Controls drive settings for cke pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1318 EMIF_CTLCFG_DENALI_PHY_1398 Register

1 EMIF_CTLCFG_DENALI_PHY_1398 Register (Offset = 55D8h) [reset = 1FFFF00h]

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Table 14-16309. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5D8h**

Figure 14-5397. EMIF_CTLCFG_DENALI_PHY_1398 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_CKE_DRIVE2			
NONE				R/W			
0h				1FFFF00h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_CKE_DRIVE2							
R/W							
1FFFF00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_CKE_DRIVE2							
R/W							
1FFFF00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_CKE_DRIVE2							
R/W							
1FFFF00h							

Table 14-16311. EMIF_CTLCFG_DENALI_PHY_1398 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_CKE_DRIVE2	R/W	1FFFF00h	Controls drive settings for cke pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1319 EMIF_CTLCFG_DENALI_PHY_1399 Register

1 EMIF_CTLCFG_DENALI_PHY_1399 Register (Offset = 55DCh) [reset = FFh]

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Table 14-16312. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5DCh**

Figure 14-5398. EMIF_CTLCFG_DENALI_PHY_1399 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_RST_DRIVE					
NONE		R/W					
0h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_RST_DRIVE							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_RST_DRIVE							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_RST_DRIVE							
R/W							
FFh							

Table 14-16314. EMIF_CTLCFG_DENALI_PHY_1399 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_RST_DRIVE	R/W	FFh	Controls drive settings for reset_n pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1320 EMIF_CTLCFG_DENALI_PHY_1400 Register

1 EMIF_CTLCFG_DENALI_PHY_1400 Register (Offset = 55E0h) [reset = 1FFFF00h]

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Table 14-16315. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5E0h**

Figure 14-5399. EMIF_CTLCFG_DENALI_PHY_1400 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RST_DRIVE2			
NONE				R/W			
0h				1FFFF00h			
23	22	21	20	19	18	17	16
PHY_PAD_RST_DRIVE2							
R/W							
1FFFF00h							
15	14	13	12	11	10	9	8
PHY_PAD_RST_DRIVE2							
R/W							
1FFFF00h							
7	6	5	4	3	2	1	0
PHY_PAD_RST_DRIVE2							
R/W							
1FFFF00h							

Table 14-16317. EMIF_CTLCFG_DENALI_PHY_1400 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_RST_DRIVE2	R/W	1FFFF00h	Controls drive settings for reset_n pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1321 EMIF_CTLCFG_DENALI_PHY_1401 Register

1 EMIF_CTLCFG_DENALI_PHY_1401 Register (Offset = 55E4h) [reset = FFh]

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Table 14-16318. Instance Table

Instance Name	Physical Address
DDR16SS0	0F30 D5E4h

Figure 14-5400. EMIF_CTLCFG_DENALI_PHY_1401 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_CS_DRIVE					
NONE		R/W					
0h		FFh					
23	22	21	20	19	18	17	16
PHY_PAD_CS_DRIVE							
R/W							
FFh							
15	14	13	12	11	10	9	8
PHY_PAD_CS_DRIVE							
R/W							
FFh							
7	6	5	4	3	2	1	0
PHY_PAD_CS_DRIVE							
R/W							
FFh							

Table 14-16320. EMIF_CTLCFG_DENALI_PHY_1401 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_CS_DRIVE	R/W	FFh	Controls drive settings for cs pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1322 EMIF_CTLCFG_DENALI_PHY_1402 Register

1 EMIF_CTLCFG_DENALI_PHY_1402 Register (Offset = 55E8h) [reset = 1FFFF00h]

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Table 14-16321. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5E8h**

Figure 14-5401. EMIF_CTLCFG_DENALI_PHY_1402 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_CS_DRIVE2			
NONE				R/W			
0h				1FFFF00h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_CS_DRIVE2							
R/W							
1FFFF00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_CS_DRIVE2							
R/W							
1FFFF00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_CS_DRIVE2							
R/W							
1FFFF00h							

Table 14-16323. EMIF_CTLCFG_DENALI_PHY_1402 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_CS_DRIVE2	R/W	1FFFF00h	Controls drive settings for cs pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1323 EMIF_CTLCFG_DENALI_PHY_1403 Register

1 EMIF_CTLCFG_DENALI_PHY_1403 Register (Offset = 55ECh) [reset = FFh]

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Table 14-16324. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5ECh**

Figure 14-5402. EMIF_CTLCFG_DENALI_PHY_1403 Name Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PAD_ODT_DRIVE					
NONE		R/W					
0h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ODT_DRIVE							
R/W							
FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ODT_DRIVE							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ODT_DRIVE							
R/W							
FFh							

Table 14-16326. EMIF_CTLCFG_DENALI_PHY_1403 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PHY_PAD_ODT_DRIVE	R/W	FFh	Controls drive settings for odt pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1324 EMIF_CTLCFG_DENALI_PHY_1404 Register

1 EMIF_CTLCFG_DENALI_PHY_1404 Register (Offset = 55F0h) [reset = 1FFFF00h]

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Table 14-16327. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5F0h**

Figure 14-5403. EMIF_CTLCFG_DENALI_PHY_1404 Name Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_ODT_DRIVE2			
NONE				R/W			
0h				1FFFF00h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_PAD_ODT_DRIVE2							
R/W							
1FFFF00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_PAD_ODT_DRIVE2							
R/W							
1FFFF00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_PAD_ODT_DRIVE2							
R/W							
1FFFF00h							

Table 14-16329. EMIF_CTLCFG_DENALI_PHY_1404 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PHY_PAD_ODT_DRIVE2	R/W	1FFFF00h	Controls drive settings for odt pads. Reset Source: ctl_amod_g_rst_n

14.5.1.2.1325 EMIF_CTLCFG_DENALI_PHY_1405 Register

1 EMIF_CTLCFG_DENALI_PHY_1405 Register (Offset = 55F4h) [reset = 0h]

Return to Summary Table

Table 14-16330. Instance Table

Instance Name	Physical Address
DDR16SS0	**0F30 D5F4h**

Figure 14-5404. EMIF_CTLCFG_DENALI_PHY_1405 Name Register

31	30	29	28	27	26	25	24
RESERVED	PHY_CAL_SETTLING_PRD_0						
NONE	R/W						
0h	0h						
23	22	21	20	19	18	17	16
PHY_CAL_VREF_SWITCH_TIMER_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PHY_CAL_VREF_SWITCH_TIMER_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_CAL_CLK_SELECT_0		
NONE					R/W		
0h					0h		

Table 14-16332. EMIF_CTLCFG_DENALI_PHY_1405 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:24	PHY_CAL_SETTLING_PRD_0	R/W	0h	Number of clock cycles to extend dfi_phyupd_req after the ack is received for settling of final values Reset Source: ctl_amod_g_rst_n
23:8	PHY_CAL_VREF_SWITCH_TIMER_0	R/W	0h	The settling time for a switch in VREF during IO pad calibration. Reset Source: ctl_amod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	PHY_CAL_CLK_SELECT_0	R/W	0h	Pad calibration pad clock frequency select setting for block 0. Reset Source: ctl_amod_g_rst_n

14.5.2 RAT Registers

Table 14-10929 lists the memory-mapped registers for a RAT module. All register offset addresses not listed in Table 14-10929 should be considered as reserved locations and the register contents should not be modified.

Note

This section contains only the RAT register descriptions. For specific physical addresses associated with a RAT module, see the corresponding *Registers* section of the modules and subsystems listed in Table 8-9 that have integrated RAT.

Table 14-16333. RAT Registers

Offset	Acronym	Register Name
0h	RAT_PID	Revision Register
4h	RAT_CONFIG	Configuration Register
20h + formula	RAT_CTRL_k	Region Control Register
24h + formula	RAT_BASE_k	Region Base Register
28h + formula	RAT_TRANS_L_k	Region Translated Lower Address
2Ch + formula	RAT_TRANS_U_k	Region Translated Upper Address
804h	RAT_DESTINATION_ID	Destination ID Register
820h	RAT_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register
824h	RAT_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register
828h	RAT_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register
82Ch	RAT_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register
830h	RAT_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register
834h	RAT_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register
838h	RAT_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register
840h	RAT_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register
844h	RAT_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register
848h	RAT_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register
84Ch	RAT_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register
850h	RAT_EOI_REG	EOI Register

1 RAT_PID Register (Offset = 0h) [reset = 66802900h]

RAT_PID is shown in Figure 14-5405 and described in Table 14-10930.

Return to Summary Table.

The Revision Register contains the major and minor revisions for the module.

Figure 14-5405. RAT_PID Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R-1h		R-2h		R-680h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R-680h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R-5h					R-1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16335. RAT_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	Business Unit: 2h = Processors
27-16	FUNC	R	680h	Module ID
15-11	RTL	R	5h	RTL Revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor Revision

2 RAT_CONFIG Register (Offset = 4h) [reset = X]

RAT_CONFIG is shown in Figure 14-5406 and described in Table 14-10931.

Return to Summary Table.

The Configuration Register contains the configuration values for the module.

Figure 14-5406. RAT_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								ADDR_WIDTH							
R-X								R-30h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDRS								REGIONS							
R-1h								R-10h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16337. RAT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	ADDR_WIDTH	R	30h	Number of address bits
15-8	ADDRS	R	1h	Number of addresses
7-0	REGIONS	R	10h	Number of regions

3 RAT_CTRL_k Register (Offset = 20h + formula) [reset = X]

RAT_CTRL_k is shown in Figure 14-5407 and described in Table 14-10932.

Return to Summary Table.

The Control for Region a

Offset = 1020h + (k * 10h); where k = 0h to Fh

Figure 14-5407. RAT_CTRL_k Register

31	30	29	28	27	26	25	24
EN	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		SIZE					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-16339. RAT_CTRL_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the Region 0h = Region disabled 1h = Region enabled
30-6	RESERVED	R/W	X	
5-0	SIZE	R/W	0h	Size of the Region in Address Bits. 0h = 1 byte, 1h = 2B, 2h = 4B, 3h = 8B, etc. up to 20h = 4GB.

4 RAT_BASE_k Register (Offset = 24h + formula) [reset = 0h]

RAT_BASE_k is shown in Figure 14-5408 and described in Table 14-10933.

Return to Summary Table.

The Base Address for Region a. This is the source address for matching to a region.

Offset = 1024h + (k * 10h); where k = 0h to Fh

Figure 14-5408. RAT_BASE_k Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">BASE</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-16341. RAT_BASE_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size.

5 RAT_TRANS_L_k Register (Offset = 28h + formula) [reset = 0h]

RAT_TRANS_L_k is shown in Figure 14-5409 and described in Table 14-10934.

Return to Summary Table.

The Translated Lower Address Bits for Region a

Offset = 1028h + (k * 10h); where k = 0h to Fh

Figure 14-5409. RAT_TRANS_L_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOWER																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-16343. RAT_TRANS_L_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOWER	R/W	0h	Translated Lower Address Bits for the Region. It must be aligned to the programmed size.

6 RAT_TRANS_U_k Register (Offset = 2Ch + formula) [reset = X]

RAT_TRANS_U_k is shown in Figure 14-5410 and described in Table 14-10935.

Return to Summary Table.

The Translated Upper Address Bits for Region a

Offset = 102Ch + (k * 10h); where k = 0h to Fh

Figure 14-5410. RAT_TRANS_U_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																UPPER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-16345. RAT_TRANS_U_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	UPPER	R/W	0h	Translated Upper Address Bits for the Region

7 RAT_DESTINATION_ID Register (Offset = 1804h) [reset = X]

RAT_DESTINATION_ID is shown in Figure 14-5411 and described in Table 14-10936.

Return to Summary Table.

The Destination ID Register defines the destination ID value for error messages.

Figure 14-5411. RAT_DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEST_ID							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-16347. RAT_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID. This field can be used for identifying a destination tag so that software can identify who should process the error message. In case of single consumer of the error messages this field is not useful and can be programmed to any value.

8 RAT_EXCEPTION_LOGGING_CONTROL Register (Offset = 1820h) [reset = X]

RAT_EXCEPTION_LOGGING_CONTROL is shown in Figure 14-5412 and described in Table 14-10937.

Return to Summary Table.

The Exception Logging Control Register controls the exception logging.

Figure 14-5412. RAT_EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-16349. RAT_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

9 RAT_EXCEPTION_LOGGING_HEADER0 Register (Offset = 1824h) [reset = 0h]

RAT_EXCEPTION_LOGGING_HEADER0 is shown in Figure 14-5413 and described in Table 14-10938.

Return to Summary Table.

The Exception Logging Header 0 Register contains the first word of the header.

Figure 14-5413. RAT_EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24
TYPE_F							
R-0h							
23	22	21	20	19	18	17	16
SRC_ID							
R-0h							
15	14	13	12	11	10	9	8
SRC_ID							
R-0h							
7	6	5	4	3	2	1	0
DEST_ID							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 14-16351. RAT_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type. 4h = RAT.
23-8	SRC_ID	R	0h	Source ID. This field uniquely identifies the particular RAT and region that caused the error. Each RAT has a unique source ID value (see Table 8-10). The error message increments that value by the region number associated with the error.
7-0	DEST_ID	R	0h	Destination ID.

10 RAT_EXCEPTION_LOGGING_HEADER1 Register (Offset = 1828h) [reset = X]

RAT_EXCEPTION_LOGGING_HEADER1 is shown in Figure 14-5414 and described in Table 14-10939.

Return to Summary Table.

The Exception Logging Header 1 Register contains the second word of the header.

Figure 14-5414. RAT_EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24
GROUP							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CODE							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-X							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16353. RAT_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code. 1h = Boundary crossing error.
15-0	RESERVED	R	X	

11 RAT_EXCEPTION_LOGGING_DATA0 Register (Offset = 182Ch) [reset = 0h]

RAT_EXCEPTION_LOGGING_DATA0 is shown in Figure 14-5415 and described in Table 14-10940.

Return to Summary Table.

The Exception Logging Data 0 Register contains the first word of the data.

Figure 14-5415. RAT_EXCEPTION_LOGGING_DATA0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">ADDR_L</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16355. RAT_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	The lower 32 bits of the address attempted to be accessed.

12 RAT_EXCEPTION_LOGGING_DATA1 Register (Offset = 1830h) [reset = X]

RAT_EXCEPTION_LOGGING_DATA1 is shown in Figure 14-5416 and described in Table 14-10941.

Return to Summary Table.

The Exception Logging Data 1 Register contains the second word of the data.

Figure 14-5416. RAT_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_H															
R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16357. RAT_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	The upper 12 bits of the address attempted to be accessed.

13 RAT_EXCEPTION_LOGGING_DATA2 Register (Offset = 1834h) [reset = X]

RAT_EXCEPTION_LOGGING_DATA2 is shown in Figure 14-5417 and described in Table 14-10942.

Return to Summary Table.

The Exception Logging Data 2 Register contains the third word of the data.

Figure 14-5417. RAT_EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16359. RAT_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID transaction attribute.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Indicates write transaction. 0h = No write transaction 1h = Write transaction
12	READ	R	0h	Indicates read transaction. 0h = No read transaction 1h = Read transaction
11	DEBUG	R	0h	Indicates debug access. 0h = No debug access 1h = Debug access
10	CACHEABLE	R	0h	Cacheable transaction attribute. 0h = The transaction could not cache the data for the CPU 1h = The transaction could cache the data for the CPU
9	PRIV	R	0h	Indicates privilege access. 0h = No privilege access 1h = Privilege access

Table 14-16359. RAT_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SECURE	R	0h	Indicates secure access. 0h = No secure access 1h = Secure access
7-0	PRIV_ID	R	0h	Priv ID transaction attribute.

14 RAT_EXCEPTION_LOGGING_DATA3 Register (Offset = 1838h) [reset = X]

RAT_EXCEPTION_LOGGING_DATA3 is shown in Figure 14-5418 and described in Table 14-10943.

Return to Summary Table.

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

Figure 14-5418. RAT_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
R-X						R-0h	
7	6	5	4	3	2	1	0
BYTECNT							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-16361. RAT_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count transaction attribute.

15 RAT_EXCEPTION_PEND_SET Register (Offset = 1840h) [reset = X]

RAT_EXCEPTION_PEND_SET is shown in Figure 14-5419 and described in Table 14-10944.

Return to Summary Table.

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Figure 14-5419. RAT_EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-16363. RAT_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

16 RAT_EXCEPTION_PEND_CLEAR Register (Offset = 1844h) [reset = X]

RAT_EXCEPTION_PEND_CLEAR is shown in Figure 14-5420 and described in Table 14-10945.

Return to Summary Table.

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Figure 14-5420. RAT_EXCEPTION_PEND_CLEAR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PEND_CLR</td></tr>
<tr><td colspan="7">R/W-X</td><td>R/W1C-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-16365. RAT_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

17 RAT_EXCEPTION_ENABLE_SET Register (Offset = 1848h) [reset = X]

RAT_EXCEPTION_ENABLE_SET is shown in Figure 14-5421 and described in Table 14-10946.

Return to Summary Table.

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

Figure 14-5421. RAT_EXCEPTION_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-16367. RAT_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_SET	R/W1S	0h	Write a 1 to set the exception interrupt enable signal.

18 RAT_EXCEPTION_ENABLE_CLEAR Register (Offset = 184Ch) [reset = X]

RAT_EXCEPTION_ENABLE_CLEAR is shown in Figure 14-5422 and described in Table 14-10947.

Return to Summary Table.

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

Figure 14-5422. RAT_EXCEPTION_ENABLE_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-16369. RAT_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_CLR	R/W1C	0h	Write a 1 to clear the exception interrupt enable signal.

19 RAT_EOI_REG Register (Offset = 850h) [reset = X]

RAT_EOI_REG is shown in Figure 14-5423 and described in Table 14-10948.

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EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Figure 14-5423. RAT_EOI_REG Register

31-16	15-0
RESERVED	EOI_WR
R/W-X	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-16371. RAT_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EOI_WR	R/W	0h	EOI Register

14.6 Interrupt Router Registers

14.6.1 MAIN_GPIOMUX_INTROUTER Registers

14.6.1.1 MAIN_GPIOMUX_INTROUTER Summary Table

Table 14-16372. MAIN_GPIOMUX_INTROUTER0_intr_router_cfg Registers, Base Address=00A0 0000h, Length=2048

Offset	Length	Register Name	MAIN_GPIOMUX_INTROUTER Physical Address
0h	32	INTR_ROUTER_CFG_PID	00A0 0000h
4h + formula	32	INTR_ROUTER_CFG_MUXCNTL_j	00A0 0004h

14.6.1.2 INTR_ROUTER_CFG_PID Register

INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Register Description: Identification register

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Table 14-16373. Instance Table

Instance Name	Physical Address
MAIN_GPIOMUX_INTROUTER0_intr_router_cfg	00A0 0000h

Figure 14-5424. INTR_ROUTER_CFG_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">694h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">694h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTLVER</td><td colspan="3">MAJREV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">10h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINREV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-16375. INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	bu Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

14.6.1.3 INTR_ROUTER_CFG_MUXCNTL_j Register

INTR_ROUTER_CFG_MUXCNTL_j Register (Offset = 4h + formula) [reset = 0h]

Register Description: Interrupt mux control register

Formula = (j * 4h); where j = 0 to 53d

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Table 14-16376. Instance Table

Instance Name	Physical Address
MAIN_GPIOMUX_INTROUTER0_intr_router_cfg	00A0 0004h + formula

Figure 14-5425. INTR_ROUTER_CFG_MUXCNTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>INT_ENABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MUX_CNTL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16378. INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:8	RESERVED	NONE	0h	Reserved
7:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

14.7 DMA Controller Registers

14.7.1 DMSS Top-Level Registers

14.7.1.1 DMASS_PKTDMA_0

DMASS_PKTDMA_0

14.7.1.1.1 DMASS_PKTDMA_0 Summaries

DMASS_PKTDMA_0 Summaries

Table 14-16379. LCDMA_RINGACC_CRED Registers, Base Address=4841 0000h, Length=8192

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	LCDMA_RINGACC_CRED_RING_CRED_J	4841 0000h + formula

Table 14-16380. PKTDMA_RXFCFG Registers, Base Address=4843 0000h, Length=16384

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_RXFCFG_FLOW_RFA_J	4843 0000h + formula

Table 14-16381. PKTDMA_TXCCFG Registers, Base Address=484A 0000h, Length=16384

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_TXCCFG_CHAN_TCFG_J	484A 0000h + formula
64h	32	PKTDMA_TXCCFG_CHAN_TPRI_CTRL_J	484A 0064h + formula
68h	32	PKTDMA_TXCCFG_CHAN_THREAD_J	484A 0068h + formula
70h	32	PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_J	484A 0070h + formula
80h	32	PKTDMA_TXCCFG_CHAN_TST_SCHED_J	484A 0080h + formula

Table 14-16382. PKTDMA_RXCCFG Registers, Base Address=484C 0000h, Length=8192

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_RXCCFG_CHAN_RCFG_J	484C 0000h + formula
64h	32	PKTDMA_RXCCFG_CHAN_RPRI_CTRL_J	484C 0064h + formula
68h	32	PKTDMA_RXCCFG_CHAN_THREAD_J	484C 0068h + formula
80h	32	PKTDMA_RXCCFG_CHAN_RST_SCHED_J	484C 0080h + formula

Table 14-16383. PKTDMA_GCFG Registers, Base Address=485C 0000h, Length=256

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_GCFG_REVISION	485C 0000h
4h	32	PKTDMA_GCFG_PERF_CTRL	485C 0004h
8h	32	PKTDMA_GCFG_EMU_CTRL	485C 0008h
10h	32	PKTDMA_GCFG_PSIL_TO	485C 0010h
20h	32	PKTDMA_GCFG_CAP0	485C 0020h
24h	32	PKTDMA_GCFG_CAP1	485C 0024h
28h	32	PKTDMA_GCFG_CAP2	485C 0028h
2Ch	32	PKTDMA_GCFG_CAP3	485C 002Ch
30h	32	PKTDMA_GCFG_CAP4	485C 0030h
60h	32	PKTDMA_GCFG_PM0	485C 0060h
64h	32	PKTDMA_GCFG_PM1	485C 0064h
78h	32	PKTDMA_GCFG_DBGADDR	485C 0078h
7Ch	32	PKTDMA_GCFG_DBGDATA	485C 007Ch

Table 14-16383. PKTDMA_GCFG Registers, Base Address=485C 0000h, Length=256 (continued)

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
88h	32	PKTDMA_GCFG_RFLOWFWSTAT	485C 0088h

Table 14-16384. LCDMA_RINGACC_RING_CFG Registers, Base Address=485E 0000h, Length=131072

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
40h	32	LCDMA_RINGACC_RING_CFG_RING_BA_LO_J	485E 0040h + formula
44h	32	LCDMA_RINGACC_RING_CFG_RING_BA_HI_J	485E 0044h + formula
48h	32	LCDMA_RINGACC_RING_CFG_RING_SIZE_J	485E 0048h + formula

Table 14-16385. PKTDMA_RXCRT Registers, Base Address=4A80 0000h, Length=131072

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_RXCRT_CHAN_CTL_J	4A80 0000h + formula
40h	32	PKTDMA_RXCRT_CHAN_STATUS0_J	4A80 0040h + formula
44h	32	PKTDMA_RXCRT_CHAN_STATUS1_J	4A80 0044h + formula
80h	32	PKTDMA_RXCRT_CHAN_STDATA_J_K	4A80 0080h + formula
200h	32	PKTDMA_RXCRT_CHAN_PEER0_J	4A80 0200h + formula
204h	32	PKTDMA_RXCRT_CHAN_PEER1_J	4A80 0204h + formula
208h	32	PKTDMA_RXCRT_CHAN_PEER2_J	4A80 0208h + formula
20Ch	32	PKTDMA_RXCRT_CHAN_PEER3_J	4A80 020Ch + formula
210h	32	PKTDMA_RXCRT_CHAN_PEER4_J	4A80 0210h + formula
214h	32	PKTDMA_RXCRT_CHAN_PEER5_J	4A80 0214h + formula
218h	32	PKTDMA_RXCRT_CHAN_PEER6_J	4A80 0218h + formula
21Ch	32	PKTDMA_RXCRT_CHAN_PEER7_J	4A80 021Ch + formula
220h	32	PKTDMA_RXCRT_CHAN_PEER8_J	4A80 0220h + formula
224h	32	PKTDMA_RXCRT_CHAN_PEER9_J	4A80 0224h + formula
228h	32	PKTDMA_RXCRT_CHAN_PEER10_J	4A80 0228h + formula
22Ch	32	PKTDMA_RXCRT_CHAN_PEER11_J	4A80 022Ch + formula
230h	32	PKTDMA_RXCRT_CHAN_PEER12_J	4A80 0230h + formula
234h	32	PKTDMA_RXCRT_CHAN_PEER13_J	4A80 0234h + formula
238h	32	PKTDMA_RXCRT_CHAN_PEER14_J	4A80 0238h + formula
23Ch	32	PKTDMA_RXCRT_CHAN_PEER15_J	4A80 023Ch + formula
400h	32	PKTDMA_RXCRT_CHAN_PCNT_J	4A80 0400h + formula
404h	32	PKTDMA_RXCRT_CHAN_DCNT_J	4A80 0404h + formula
408h	32	PKTDMA_RXCRT_CHAN_BCNT_J	4A80 0408h + formula
410h	32	PKTDMA_RXCRT_CHAN_SBCNT_J	4A80 0410h + formula

Table 14-16386. PKTDMA_TXCRT Registers, Base Address=4AA0 0000h, Length=262144

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_TXCRT_CHAN_CTL_J	4AA0 0000h + formula
40h	32	PKTDMA_TXCRT_CHAN_STATUS0_J	4AA0 0040h + formula
44h	32	PKTDMA_TXCRT_CHAN_STATUS1_J	4AA0 0044h + formula
80h	32	PKTDMA_TXCRT_CHAN_STDATA_J_K	4AA0 0080h + formula
200h	32	PKTDMA_TXCRT_CHAN_PEER0_J	4AA0 0200h + formula
204h	32	PKTDMA_TXCRT_CHAN_PEER1_J	4AA0 0204h + formula

Table 14-16386. PKTDMA_TXCRT Registers, Base Address=4AA0 0000h, Length=262144 (continued)

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
208h	32	PKTDMA_TXCRT_CHAN_PEER2_J	4AA0 0208h + formula
20Ch	32	PKTDMA_TXCRT_CHAN_PEER3_J	4AA0 020Ch + formula
210h	32	PKTDMA_TXCRT_CHAN_PEER4_J	4AA0 0210h + formula
214h	32	PKTDMA_TXCRT_CHAN_PEER5_J	4AA0 0214h + formula
218h	32	PKTDMA_TXCRT_CHAN_PEER6_J	4AA0 0218h + formula
21Ch	32	PKTDMA_TXCRT_CHAN_PEER7_J	4AA0 021Ch + formula
220h	32	PKTDMA_TXCRT_CHAN_PEER8_J	4AA0 0220h + formula
224h	32	PKTDMA_TXCRT_CHAN_PEER9_J	4AA0 0224h + formula
228h	32	PKTDMA_TXCRT_CHAN_PEER10_J	4AA0 0228h + formula
22Ch	32	PKTDMA_TXCRT_CHAN_PEER11_J	4AA0 022Ch + formula
230h	32	PKTDMA_TXCRT_CHAN_PEER12_J	4AA0 0230h + formula
234h	32	PKTDMA_TXCRT_CHAN_PEER13_J	4AA0 0234h + formula
238h	32	PKTDMA_TXCRT_CHAN_PEER14_J	4AA0 0238h + formula
23Ch	32	PKTDMA_TXCRT_CHAN_PEER15_J	4AA0 023Ch + formula
400h	32	PKTDMA_TXCRT_CHAN_PCNT_J	4AA0 0400h + formula
408h	32	PKTDMA_TXCRT_CHAN_BCNT_J	4AA0 0408h + formula
410h	32	PKTDMA_TXCRT_CHAN_SBCNT_J	4AA0 0410h + formula

Table 14-16387. LCDMA_RINGACC_RINGRT Registers, Base Address=4B80 0000h, Length=4194304

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
10h	32	LCDMA_RINGACC_RINGRT_RING_FDB_J	4B80 0010h + formula
18h	32	LCDMA_RINGACC_RINGRT_RING_FOCC_J	4B80 0018h + formula
1010h	32	LCDMA_RINGACC_RINGRT_RING_RDB_J	4B80 1010h + formula
1018h	32	LCDMA_RINGACC_RINGRT_RING_ROCC_J	4B80 1018h + formula

14.7.1.1.2 DMASS_PKTDMA_0 Registers

DMASS_PKTDMA_0 Registers

14.7.1.1.2.1 LCDMA_RINGACC_CRED_RING_CRED_j Register

1 LCDMA_RINGACC_CRED_RING_CRED_j Register (Offset = 0h + formula) [reset = 0h]

The Credentials Register provides credentials to be used when performing memory accesses using this flow.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 287d

Table 14-16388. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4841 0000h + formula**

Figure 14-5426. LCDMA_RINGACC_CRED_RING_CRED_j Name Register

31	30	29	28	27	26	25	24
CHK_SECURE	RESERVED				SECURE	PRIV	
R/W	NONE				R/W	R/W	
0h	0h				0h	0h	
23	22	21	20	19	18	17	16
PRIVID							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16390. LCDMA_RINGACC_CRED_RING_CRED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CHK_SECURE	R/W	0h	Check secure control bit Reset Source: rst_mod_g_rst_n
30:27	RESERVED	NONE	0h	Reserved
26	SECURE	R/W	0h	Secure attribute Reset Source: rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Privelege attribute Reset Source: rst_mod_g_rst_n
23:16	PRIVID	R/W	0h	Privelege ID attribute Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.2 PKTDMA_RXFCFG_FLOW_RFA_j Register

1 PKTDMA_RXFCFG_FLOW_RFA_j Register (Offset = 0h + formula) [reset = 0h]

The Rx Flow N Configuration Register A contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. The fields in this register are as follows:

Return to Summary Table

Offset = (j * 40h); where j = 0 to 175d

Table 14-16391. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4843 0000h + formula**

Figure 14-5427. PKTDMA_RXFCFG_FLOW_RFA_j Name Register

31	30	29	28	27	26	25	24
RESERVED	RX_EINFO_PRESENT	RX_PSINFO_PRESENT	RX_ERROR_HANDLING	RESERVED			RX_SOP_OFFSET
NONE	R/W	R/W	R/W	NONE			R/W
0h	0h	0h	0h	0h			0h
23	22	21	20	19	18	17	16
RX_SOP_OFFSET							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16393. PKTDMA_RXFCFG_FLOW_RFA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30	RX_EINFO_PRESENT	R/W	0h	Rx Extended Packet Info Block Present: This bit controls whether or not the Extended Packet Info Block will be present in the Rx Packet Descriptor. If this bit is clear, the port DMA will clear the Extended Packet Info Present bit in the PD and will drop any Timestamp or SW Data words that are presented from the back end application. If this bit is set, the port DMA will set the Extended Packet Info Block Present bit in the PD and will copy any Timestamp or SW Data words that are presented across the Rx streaming interface into the Extended Packet Info Block words in the descriptor. If no Timestamp or SW Data words are presented from the back end application, the port DMA will overwrite the fields in the PD with zeroes. Reset Source: rst_mod_g_rst_n

Table 14-16393. PKTDMA_RXFCFG_FLOW_RFA_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	RX_PSINFO_PRESENT	R/W	0h	Rx PS Words Present: This bit controls whether or not the Protocol Specific words will be present in the Rx Packet Descriptor. If this bit is clear, the port DMA will set the PS word count to 0 in the PD and will drop any PS words that are presented from the back end application. If this bit is set, the port DMA will set the PS word count to the value given by the back end application and will copy the PS words from the back end application to the location Reset Source: rst_mod_g_rst_n
28	RX_ERROR_HANDLING	R/W	0h	Rx Error Handling Mode: This bit controls the error handling mode for the flow and is only used when channel errors (i.e. descriptor starvation) occurs. 0 = Starvation errors result in dropping packet and incrementing dropped packet count. 1 = Starvation errors result in the channel waiting until descriptors are added to the free queue before the channel will be scheduled. Reset Source: rst_mod_g_rst_n
27:25	RESERVED	NONE	0h	Reserved
24:16	RX_SOP_OFFSET	R/W	0h	Rx Start of Packet Offset: This field specifies the number of bytes that are to be skipped in the SOP buffer before beginning to write the payload or protocol specific bytes(if they are in the sop buffer). This value must be less than the minimum size of a buffer in the system. Valid values are 0 - 255 bytes. The primary purpose of this field is to ensure that space is left in the descriptor to place the protocol specific information without overwriting or being overwritten by the Rx data. The secondary purpose of this field is to allow space to be left prior to the data in the descriptor in case header information needs to be added as the packet is passed thorough the system. Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.3 PKTDMA_TXCCFG_CHAN_TCFG_j Register

1 PKTDMA_TXCCFG_CHAN_TCFG_j Register (Offset = 0h + formula) [reset = 20400h]

The Tx Channel Configuration Register is used to initialize static mode settings for the Tx DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

Return to Summary Table

Offset = (j * 100h); where j = 0 to 41d

Table 14-16394. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484A 0000h + formula**

Figure 14-5428. PKTDMA_TXCCFG_CHAN_TCFG_j Name Register

31	30	29	28	27	26	25	24
TX_PAUSE_ON_ERR	TX_FILT_EINFO	TX_FILT_PSWORDS	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED				TX_CHAN_TYPE			
NONE				R			
0h				2h			
15	14	13	12	11	10	9	8
RESERVED				TX_BURST_SIZE		TX_TDTYPE	TX_NOTDPKT
NONE				R/W		R/W	R/W
0h				1h		0h	0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16396. PKTDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30	TX_FILT_EINFO	R/W	0h	This field controls whether or not the DMA controller will pass the extended packet information fields (if present) from the descriptor to the back end application. This field is encoded as follows: 0=DMA controller will pass extended packet info words if they are present in the descriptor 1=DMA controller will filter extended packet info words. Reset Source: rst_mod_g_rst_n
29	TX_FILT_PSWORDS	R/W	0h	This field controls whether or not the DMA controller will pass the protocol specific words (if present) from the descriptor to the back end application. This field is encoded as follows: 0=DMA controller will pass PS words if present in descriptor 1=DMA controller will filter PS words. Reset Source: rst_mod_g_rst_n
28:20	RESERVED	NONE	0h	Reserved

Table 14-16396. PKTDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	TX_CHAN_TYPE	R	2h	Tx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 2 = Channel performs packet oriented data transfers using pass by reference rings. Channels configured in this mode can only use Host and Monolithic descriptors and the pointers to those descriptors are passed from/to SW using rings in the Ring Accelerator. Reset Source: rst_mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:10	TX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0,1 = 64 Bytes 2 = 128 Bytes All other values are reserved Reset Source: rst_mod_g_rst_n
9	TX_TDTYPE	R/W	0h	Specifies whether or not the channel should immediately return a teardown completion response to the default completion queue or wait until a status message is returned from the remote PSI-L paired peripheral. 0 = return immediately once all traffic is complete in PKTDMA. 1 = wait until remote peer sends back a completion message. Reset Source: rst_mod_g_rst_n
8	TX_NOTDPKT	R/W	0h	Specifies whether or not the channel should suppress sending the single data phase teardown packet when teardown is complete. 0 = TD packet is sent 1 = Suppress sending TD packet Reset Source: rst_mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.4 PKTDMA_TXCCFG_CHAN_TPRI_CTRL_j Register

1 PKTDMA_TXCCFG_CHAN_TPRI_CTRL_j Register (Offset = 64h + formula) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 41d

Table 14-16397. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484A 0064h + formula**

Figure 14-5429. PKTDMA_TXCCFG_CHAN_TPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-16399. PKTDMA_TXCCFG_CHAN_TPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Tx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Tx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.5 PKTDMA_TXCCFG_CHAN_THREAD_j Register

1 PKTDMA_TXCCFG_CHAN_THREAD_j Register (Offset = 68h + formula) [reset = 0h]

The thread ID mapping register is used to pair the Tx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 41d

Table 14-16400. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484A 0068h + formula**

Figure 14-5430. PKTDMA_TXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-16402. PKTDMA_TXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.6 PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register

1 PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register (Offset = 70h + formula) [reset = C0h]

The fifo depth register is used to specify how many FIFO data phases deep the Tx per channel FIFO will be for the channel. While the maximum depth of the Tx FIFO is set at design time, the FIFO depth can be artificially reduced in order to control the maximum latency which can be introduced due to buffering effects.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 41d

Table 14-16403. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484A 0070h + formula**

Figure 14-5431. PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FDEPTH							
R/W							
C0h							

Table 14-16405. PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDEPTH	R/W	C0h	FIFO Depth: This field contains the number of Tx FIFO bytes which will be allowed to be stored for the channel. The minimum value is equal to the PSI-L interface data path width but must be greater than 32 bytes + the burst size, the maximum value varies by channel class (ultra-high capacity/high capacity/normal capacity) and is equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L data path width (tstrm_wdth). The fdepth must always be an integer multiple of tstrm_wdth. The reset value of this register varies by channel class (ultra-high capacity/high capacity/normal capacity) but will be equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L interface data width (tstrm_wdth). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.7 PKTDMA_TXCCFG_CHAN_TST_SCHED_j Register

1 PKTDMA_TXCCFG_CHAN_TST_SCHED_j Register (Offset = 80h + formula) [reset = 0h]

The Tx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Return to Summary Table

Offset = (j * 100h); where j = 0 to 41d

Table 14-16406. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484A 0080h + formula**

Figure 14-5432. PKTDMA_TXCCFG_CHAN_TST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-16408. PKTDMA_TXCCFG_CHAN_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Tx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.8 PKTDMA_RXCCFG_CHAN_RCFG_j Register

1 PKTDMA_RXCCFG_CHAN_RCFG_j Register (Offset = 0h + formula) [reset = 20400h]

The Rx Channel Configuration Register is used to initialize static mode settings for the Rx DMA channel. This register may only be written when the channel is disabled (rx_enable in realtime control reg is 0).

Return to Summary Table

Offset = (j * 100h); where j = 0 to 28d

Table 14-16409. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484C 0000h + formula**

Figure 14-5433. PKTDMA_RXCCFG_CHAN_RCFG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RX_PAUSE_ON_ERR</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">RX_CHAN_TYPE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">RX_BURST_SIZE</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">1h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16411. PKTDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved

Table 14-16411. PKTDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	RX_CHAN_TYPE	R/W	2h	Rx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 2 = Channel performs packet oriented data transfers using pass by reference rings. Channels configured in this mode can only use Host and Monolithic descriptors and the pointers to those descriptors are passed from/to SW using rings in the Ring Accelerator. 3 = Channel performs packet oriented data transfers using pass by reference rings with single buffer packet mode enabled. Channels configured in this mode can only use Host descriptors and each descriptor will be processed as an independent packet (no buffer chaining). This is the only packet oriented mode that can be used with data sources that are infinite streams (no EOP) Reset Source: rst_mod_g_rst_n 2 `Normal channel` 3 `Single buffer mode channel`
15:12	RESERVED	NONE	0h	Reserved
11:10	RX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0,1 = 64 Bytes 2 = 128 Bytes All other values are reserved Reset Source: rst_mod_g_rst_n
9:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.9 PKTDMA_RXCCFG_CHAN_RPRI_CTRL_j Register

1 PKTDMA_RXCCFG_CHAN_RPRI_CTRL_j Register (Offset = 64h + formula) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 28d

Table 14-16412. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484C 0064h + formula**

Figure 14-5434. PKTDMA_RXCCFG_CHAN_RPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-16414. PKTDMA_RXCCFG_CHAN_RPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Rx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem*_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Rx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.10 PKTDMA_RXCCFG_CHAN_THREAD_j Register

1 PKTDMA_RXCCFG_CHAN_THREAD_j Register (Offset = 68h + formula) [reset = 0h]

The thread ID mapping register is used to pair the Rx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 28d

Table 14-16415. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484C 0068h + formula**

Figure 14-5435. PKTDMA_RXCCFG_CHAN_THREAD_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">THREAD_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">THREAD_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16417. PKTDMA_RXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.11 PKTDMA_RXCCFG_CHAN_RST_SCHED_j Register

1 PKTDMA_RXCCFG_CHAN_RST_SCHED_j Register (Offset = 80h + formula) [reset = 0h]

The Rx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Return to Summary Table

Offset = (j * 100h); where j = 0 to 28d

Table 14-16418. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**484C 0080h + formula**

Figure 14-5436. PKTDMA_RXCCFG_CHAN_RST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-16420. PKTDMA_RXCCFG_CHAN_RST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Rx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Rx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.12 PKTDMA_GCFG_REVISION Register

1 PKTDMA_GCFG_REVISION Register (Offset = 0h) [reset = 662A8901h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-16421. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0000h**

Figure 14-5437. PKTDMA_GCFG_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">662Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">662Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">11h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-16423. PKTDMA_GCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	662Ah	Module ID field Reset Source: rst_mod_g_rst_n
15:11	REVRTL	R	11h	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: rst_mod_g_rst_n

14.7.1.1.2.13 PKTDMA_GCFG_PERF_CTRL Register

1 PKTDMA_GCFG_PERF_CTRL Register (Offset = 4h) [reset = 40h]

The performance control register contains fields which can be used to adjust the performance of the PKTDMA in the system.

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Table 14-16424. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0004h**

Figure 14-5438. PKTDMA_GCFG_PERF_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TIMEOUT_CNT							
R/W							
40h							
7	6	5	4	3	2	1	0
TIMEOUT_CNT							
R/W							
40h							

Table 14-16426. PKTDMA_GCFG_PERF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TIMEOUT_CNT	R/W	40h	This feature is not currently supported Reset Source: rst_mod_g_rst_n

14.7.1.1.2.14 PKTDMA_GCFG_EMU_CTRL Register

1 PKTDMA_GCFG_EMU_CTRL Register (Offset = 8h) [reset = 0h]

The emulation control register is used to control the behavior of the DMA when the emususp input is asserted.

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Table 14-16427. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0008h**

Figure 14-5439. PKTDMA_GCFG_EMU_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-16429. PKTDMA_GCFG_EMU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Soft Reset Source: rst_mod_g_rst_n
0	FREE	R/W	0h	Free Reset Source: rst_mod_g_rst_n

14.7.1.1.2.15 PKTDMA_GCFG_PSIL_TO Register

1 PKTDMA_GCFG_PSIL_TO Register (Offset = 10h) [reset = 400h]

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrances on PSI-L configuration transactions issued by the built in PSI-L proxy.

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Table 14-16430. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0010h**

Figure 14-5440. PKTDMA_GCFG_PSIL_TO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>TOUT</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TOUT_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">400h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TOUT_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">400h</td></tr>
</table>

Table 14-16432. PKTDMA_GCFG_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a conifiguration read or write transaction and asserting the tout bit Reset Source: rst_mod_g_rst_n

14.7.1.1.2.16 PKTDMA_GCFG_CAP0 Register

1 PKTDMA_GCFG_CAP0 Register (Offset = 20h) [reset = 0h]

The Capabilities Register 0 specifies which standard features this PKTDMA instance supports.

Return to Summary Table

Table 14-16433. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0020h**

Figure 14-5441. PKTDMA_GCFG_CAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16435. PKTDMA_GCFG_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.17 PKTDMA_GCFG_CAP1 Register

1 PKTDMA_GCFG_CAP1 Register (Offset = 24h) [reset = 0h]

The Capabilities Register 1 specifies which standard features this PKTDMA instance supports.

Return to Summary Table

Table 14-16436. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0024h**

Figure 14-5442. PKTDMA_GCFG_CAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16438. PKTDMA_GCFG_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.18 PKTDMA_GCFG_CAP2 Register

1 PKTDMA_GCFG_CAP2 Register (Offset = 28h) [reset = 74002Ah]

The Capabilities Register 2 specifies how many resources this PKTDMA instance supports.

Return to Summary Table

Table 14-16439. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0028h**

Figure 14-5443. PKTDMA_GCFG_CAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED					RCHAN_CNT		
NONE					R		
0h					1Dh		
23	22	21	20	19	18	17	16
RCHAN_CNT						RESERVED	
R						NONE	
1Dh						0h	
15	14	13	12	11	10	9	8
RESERVED							TCHAN_CNT
NONE							R
0h							2Ah
7	6	5	4	3	2	1	0
TCHAN_CNT							
R							
2Ah							

Table 14-16441. PKTDMA_GCFG_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:18	RCHAN_CNT	R	1Dh	Rx internal channel count Reset Source: rst_mod_g_rst_n
17:9	RESERVED	NONE	0h	Reserved
8:0	TCHAN_CNT	R	2Ah	Tx internal channel count Reset Source: rst_mod_g_rst_n

14.7.1.1.2.19 PKTDMA_GCFG_CAP3 Register

1 PKTDMA_GCFG_CAP3 Register (Offset = 2Ch) [reset = B0h]

The Capabilities Register 3 specifies how many resources this PKTDMA instance supports.

Return to Summary Table

Table 14-16442. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 002Ch**

Figure 14-5444. PKTDMA_GCFG_CAP3 Name Register

31	30	29	28	27	26	25	24
UCHAN_CNT							
R							
0h							
23	22	21	20	19	18	17	16
UCHAN_CNT	HCHAN_CNT						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
HCHAN_CNT		RFLOW_CNT					
R		R					
0h		B0h					
7	6	5	4	3	2	1	0
RFLOW_CNT							
R							
B0h							

Table 14-16444. PKTDMA_GCFG_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	UCHAN_CNT	R	0h	Tx ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
22:14	HCHAN_CNT	R	0h	Tx high capacity internal channel count Reset Source: rst_mod_g_rst_n
13:0	RFLOW_CNT	R	B0h	Rx flow table entry count Reset Source: rst_mod_g_rst_n

14.7.1.1.2.20 PKTDMA_GCFG_CAP4 Register

1 PKTDMA_GCFG_CAP4 Register (Offset = 30h) [reset = 70h]

The Capabilities Register 4 specifies how many resources this PKTDMA instance supports.

Return to Summary Table

Table 14-16445. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0030h**

Figure 14-5445. PKTDMA_GCFG_CAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TFLOW_CNT					
NONE		R					
0h		70h					
7	6	5	4	3	2	1	0
TFLOW_CNT							
R							
70h							

Table 14-16447. PKTDMA_GCFG_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TFLOW_CNT	R	70h	Tx flow table entry count Reset Source: rst_mod_g_rst_n

14.7.1.1.2.21 PKTDMA_GCFG_PM0 Register

1 PKTDMA_GCFG_PM0 Register (Offset = 60h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

Return to Summary Table

Table 14-16448. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0060h**

Figure 14-5446. PKTDMA_GCFG_PM0 Name Register

31	30	29	28	27	26	25	24
NOGATE_RDU3	NOGATE_RDU2	NOGATE_RDU1	NOGATE_RDU0	NOGATE_TDU3	NOGATE_TDU2	NOGATE_TDU1	NOGATE_TDU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOGATE_RSVD4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOGATE_RSVD4			NOGATE_RDEC	NOGATE_RSVD3			NOGATE_SDEC
R/W			R/W	R/W			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOGATE_RSVD2			NOGATE_WARB	NOGATE_RSVD1			NOGATE_CARB
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 14-16450. PKTDMA_GCFG_PM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOGATE_RDU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
30	NOGATE_RDU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
29	NOGATE_RDU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
28	NOGATE_RDU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
27	NOGATE_TDU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
26	NOGATE_TDU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
25	NOGATE_TDU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
24	NOGATE_TDU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-16450. PKTDMA_GCFG_PM0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:13	NOGATE_RSVD4	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
12	NOGATE_RDEC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
11:9	NOGATE_RSVD3	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
8	NOGATE_SDEC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
7:5	NOGATE_RSVD2	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
4	NOGATE_WARB	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
3:1	NOGATE_RSVD1	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
0	NOGATE_CARB	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.22 PKTDMA_GCFG_PM1 Register

1 PKTDMA_GCFG_PM1 Register (Offset = 64h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

Return to Summary Table

Table 14-16451. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0064h**

Figure 14-5447. PKTDMA_GCFG_PM1 Name Register

31	30	29	28	27	26	25	24
NOGATE_RSVD12	NOGATE_STATS	NOGATE_PROXY	NOGATE_RSVD11	NOGATE_P2P	NOGATE_RSVD10	NOGATE_EHANDLER	NOGATE_RINGOCC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOGATE_RSVD9	NOGATE_TPCF	NOGATE_RSVD8			NOGATE_CFG	NOGATE_RSVD7	
R/W	R/W	R/W			R/W	R/W	
0h	0h	0h			0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOGATE_RFLOWFW	NOGATE_RSVD6	NOGATE_RCU	NOGATE_TCU	NOGATE_RSVD5			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOGATE_RSVD5							
R/W							
0h							

Table 14-16453. PKTDMA_GCFG_PM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOGATE_RSVD12	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
30	NOGATE_STATS	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
29	NOGATE_PROXY	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
28	NOGATE_RSVD11	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
27	NOGATE_P2P	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
26	NOGATE_RSVD10	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
25	NOGATE_EHANDLER	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
24	NOGATE_RINGOCC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-16453. PKTDMA_GCFG_PM1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	NOGATE_RSVD9	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
22	NOGATE_TPCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
21:19	NOGATE_RSVD8	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
18	NOGATE_CFG	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
17:16	NOGATE_RSVD7	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
15	NOGATE_RFLOWFW	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
14	NOGATE_RSVD6	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
13	NOGATE_RCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
12	NOGATE_TCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
11:0	NOGATE_RSVD5	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.23 PKTDMA_GCFG_DBGADDR Register

1 PKTDMA_GCFG_DBGADDR Register (Offset = 78h) [reset = 0h]

This register provides a writable address which allows debug information to be read from the Debug Data Register

Return to Summary Table

Table 14-16454. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0078h**

Figure 14-5448. PKTDMA_GCFG_DBGADDR Name Register

31	30	29	28	27	26	25	24
DBG_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DBG_UNIT							
R/W							
0h							
7	6	5	4	3	2	1	0
DBG_ADDR							
R/W							
0h							

Table 14-16456. PKTDMA_GCFG_DBGADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBG_EN	R/W	0h	Debug enable Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	DBG_UNIT	R/W	0h	Selects which unit to read debug information from Reset Source: rst_mod_g_rst_n
7:0	DBG_ADDR	R/W	0h	Selects offset within unit to access seperate debug registers Reset Source: rst_mod_g_rst_n

14.7.1.1.2.24 PKTDMA_GCFG_DBGDATA Register

1 PKTDMA_GCFG_DBGDATA Register (Offset = 7Ch) [reset = 0h]

This register provides read only debug data

Return to Summary Table

Table 14-16457. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 007Ch**

Figure 14-5449. PKTDMA_GCFG_DBGDATA Name Register

31	30	29	28	27	26	25	24
DBG_DATA							
R							
0h							
23	22	21	20	19	18	17	16
DBG_DATA							
R							
0h							
15	14	13	12	11	10	9	8
DBG_DATA							
R							
0h							
7	6	5	4	3	2	1	0
DBG_DATA							
R							
0h							

Table 14-16459. PKTDMA_GCFG_DBGDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBG_DATA	R	0h	Provides debug information from various internal units. The value which is read back depends on which unit and register are selected in the Debug Address Register Reset Source: rst_mod_g_rst_n

14.7.1.1.2.25 PKTDMA_GCFG_RFLOWFWSTAT Register

1 PKTDMA_GCFG_RFLOWFWSTAT Register (Offset = 88h) [reset = 0h]

The Rx Flow FW Status Register 0 captures information about the thread/channel and received flow ID which failed a range check. Values in this register will remain persistent once an exception has been detected until the pend bit is written back to 0

Return to Summary Table

Table 14-16460. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485C 0088h**

Figure 14-5450. PKTDMA_GCFG_RFLOWFWSTAT Name Register

31	30	29	28	27	26	25	24
PEND	RESERVED	FLOWID					
R/W	NONE	R/W					
0h	0h	0h					
23	22	21	20	19	18	17	16
FLOWID							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							CHANNEL
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
CHANNEL							
R/W							
0h							

Table 14-16462. PKTDMA_GCFG_RFLOWFWSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PEND	R/W	0h	This bit is set whenever the Flow ID firewall detects a Flow ID is out of range for an incoming packet. Once this bit is set, the remaining fields in this register will not be modified. SW is required to write this bit to 0 to allow another exception to be captured. Reset Source: rst_mod_g_rst_n
30	RESERVED	NONE	0h	Reserved
29:16	FLOWID	R/W	0h	This is the flow ID that was received on the trapped packet Reset Source: rst_mod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	CHANNEL	R/W	0h	This is the channel number on which the trapped packet was received Reset Source: rst_mod_g_rst_n

14.7.1.1.2.26 LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register

1 LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register (Offset = 40h + formula) [reset = 0h]

The Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 287d

Table 14-16463. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485E 0040h + formula**

Figure 14-5451. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16465. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_LO	R/W	0h	Ring base address (LSBs) Reset Source: rst_mod_g_rst_n

14.7.1.1.2.27 LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register

1 LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register (Offset = 44h + formula) [reset = 0h]

The Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 287d

Table 14-16466. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485E 0044h + formula**

Figure 14-5452. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				ASEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADDR_HI			
NONE				R/W			
0h				0h			

Table 14-16468. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	ASEL	R/W	0h	Ring base address select Reset Source: rst_mod_g_rst_n
15:4	RESERVED	NONE	0h	Reserved
3:0	ADDR_HI	R/W	0h	Ring base address (MSBs) Reset Source: rst_mod_g_rst_n

14.7.1.1.2.28 LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register

1 LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register (Offset = 48h + formula) [reset = 21000000h]

The Ring Size Register contains the element count for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 287d

Table 14-16469. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**485E 0048h + formula**

Figure 14-5453. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Name Register

31	30	29	28	27	26	25	24
QMODE			RESERVED		RING_ELSIZE		
R/NA			NONE		R/NA		
1h			0h		1h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SIZE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE							
R/W							
0h							

Table 14-16471. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	QMODE	R/NA	1h	Defines the mode for this ring or queue. Reset Source: rst_mod_g_rst_n `1 exposed ring mode with dual queues (forward/reverse) for SW direct access`
28:27	RESERVED	NONE	0h	Reserved
26:24	RING_ELSIZE	R/NA	1h	Reset Source: rst_mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:0	SIZE	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.29 PKTDMA_RXCRT_CHAN_CTL_j Register

1 PKTDMA_RXCRT_CHAN_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Rx Channel Realtime Control Register contains real-time control and status information for the Rx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16472. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0000h + formula**

Figure 14-5454. PKTDMA_RXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
RX_ENABLE	RX_TEARDOWN	RX_PAUSE	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RX_ERROR
NONE							R/W
0h							0h

Table 14-16474. PKTDMA_RXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in overflow conditions in the attached application and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate tha the channel teardown is complete. If the host is enabling a channel that is just being set up, the host must initialize all of the other channel configuration fields before setting this bit. Reset Source: rst_mod_g_rst_n
30	RX_TEARDOWN	R/W	0h	This field indicates whether or not an Rx teardown operation is complete. This field should be cleared when a channel is initialized. This field will be set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n

Table 14-16474. PKTDMA_RXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	RX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n
28:1	RESERVED	NONE	0h	Reserved
0	RX_ERROR	R/W	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared when the channel is disabled and re-enabled. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.30 PKTDMA_RXCRT_CHAN_STATUS0_j Register

1 PKTDMA_RXCRT_CHAN_STATUS0_j Register (Offset = 40h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16475. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0040h + formula

Figure 14-5455. PKTDMA_RXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
RRING_PEND	RXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	RX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16477. PKTDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	RXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-16477. PKTDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.31 PKTDMA_RXCRT_CHAN_STATUS1_j Register

1 PKTDMA_RXCRT_CHAN_STATUS1_j Register (Offset = 44h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16478. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0044h + formula**

Figure 14-5456. PKTDMA_RXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
RX_REQS	RESERVED					FIFO_PEND	FIFO_BUSY
R	NONE					R	R
0h	0h					0h	0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-16480. PKTDMA_RXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	FIFO_PEND	R	0h	The FIFO has enough data for a burst Reset Source: rst_mod_g_rst_n
24	FIFO_BUSY	R	0h	The fifo has data Reset Source: rst_mod_g_rst_n
23:8	RESERVED	NONE	0h	Reserved
7	CHANNEL_OK	R	0h	The channel is trying to schedule work Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	The channel has active work Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n

Table 14-16480. PKTDMA_RXCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.32 PKTDMA_RXCRT_CHAN_STDATA_j_k Register

1 PKTDMA_RXCRT_CHAN_STDATA_j_k Register (Offset = 80h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the PKTDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 28d, k = 0 to 31d

Table 14-16481. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0080h + formula**

Figure 14-5457. PKTDMA_RXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/W							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/W							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/W							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/W							
0h							

Table 14-16483. PKTDMA_RXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/W	0h	See RX State Mapping Table Reset Source: rst_mod_g_rst_n

14.7.1.1.2.33 PKTDMA_RXCRT_CHAN_PEER0_j Register

1 PKTDMA_RXCRT_CHAN_PEER0_j Register (Offset = 200h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16484. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0200h + formula**

Figure 14-5458. PKTDMA_RXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16486. PKTDMA_RXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.34 PKTDMA_RXCRT_CHAN_PEER1_j Register

1 PKTDMA_RXCRT_CHAN_PEER1_j Register (Offset = 204h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16487. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0204h + formula

Figure 14-5459. PKTDMA_RXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16489. PKTDMA_RXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.35 PKTDMA_RXCRT_CHAN_PEER2_j Register

1 PKTDMA_RXCRT_CHAN_PEER2_j Register (Offset = 208h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16490. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0208h + formula**

Figure 14-5460. PKTDMA_RXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16492. PKTDMA_RXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.36 PKTDMA_RXCRT_CHAN_PEER3_j Register

1 PKTDMA_RXCRT_CHAN_PEER3_j Register (Offset = 20Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16493. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 020Ch + formula

Figure 14-5461. PKTDMA_RXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16495. PKTDMA_RXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.37 PKTDMA_RXCRT_CHAN_PEER4_j Register

1 PKTDMA_RXCRT_CHAN_PEER4_j Register (Offset = 210h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16496. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0210h + formula**

Figure 14-5462. PKTDMA_RXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16498. PKTDMA_RXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.38 PKTDMA_RXCRT_CHAN_PEER5_j Register

1 PKTDMA_RXCRT_CHAN_PEER5_j Register (Offset = 214h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16499. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0214h + formula**

Figure 14-5463. PKTDMA_RXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16501. PKTDMA_RXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.39 PKTDMA_RXCRT_CHAN_PEER6_j Register

1 PKTDMA_RXCRT_CHAN_PEER6_j Register (Offset = 218h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16502. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0218h + formula

Figure 14-5464. PKTDMA_RXCRT_CHAN_PEER6_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16504. PKTDMA_RXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.40 PKTDMA_RXCRT_CHAN_PEER7_j Register

1 PKTDMA_RXCRT_CHAN_PEER7_j Register (Offset = 21Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16505. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 021Ch + formula

Figure 14-5465. PKTDMA_RXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16507. PKTDMA_RXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.41 PKTDMA_RXCRT_CHAN_PEER8_j Register

1 PKTDMA_RXCRT_CHAN_PEER8_j Register (Offset = 220h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16508. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0220h + formula**

Figure 14-5466. PKTDMA_RXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16510. PKTDMA_RXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.42 PKTDMA_RXCRT_CHAN_PEER9_j Register

1 PKTDMA_RXCRT_CHAN_PEER9_j Register (Offset = 224h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16511. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0224h + formula

Figure 14-5467. PKTDMA_RXCRT_CHAN_PEER9_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16513. PKTDMA_RXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.43 PKTDMA_RXCRT_CHAN_PEER10_j Register

1 PKTDMA_RXCRT_CHAN_PEER10_j Register (Offset = 228h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16514. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0228h + formula

Figure 14-5468. PKTDMA_RXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16516. PKTDMA_RXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.44 PKTDMA_RXCRT_CHAN_PEER11_j Register

1 PKTDMA_RXCRT_CHAN_PEER11_j Register (Offset = 22Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16517. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 022Ch + formula**

Figure 14-5469. PKTDMA_RXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16519. PKTDMA_RXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.45 PKTDMA_RXCRT_CHAN_PEER12_j Register

1 PKTDMA_RXCRT_CHAN_PEER12_j Register (Offset = 230h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16520. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0230h + formula**

Figure 14-5470. PKTDMA_RXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16522. PKTDMA_RXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.46 PKTDMA_RXCRT_CHAN_PEER13_j Register

1 PKTDMA_RXCRT_CHAN_PEER13_j Register (Offset = 234h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16523. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0234h + formula**

Figure 14-5471. PKTDMA_RXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16525. PKTDMA_RXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.47 PKTDMA_RXCRT_CHAN_PEER14_j Register

1 PKTDMA_RXCRT_CHAN_PEER14_j Register (Offset = 238h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16526. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0238h + formula

Figure 14-5472. PKTDMA_RXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16528. PKTDMA_RXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.48 PKTDMA_RXCRT_CHAN_PEER15_j Register

1 PKTDMA_RXCRT_CHAN_PEER15_j Register (Offset = 23Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16529. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 023Ch + formula

Figure 14-5473. PKTDMA_RXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16531. PKTDMA_RXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.49 PKTDMA_RXCRT_CHAN_PCNT_j Register

1 PKTDMA_RXCRT_CHAN_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16532. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4A80 0400h + formula**

Figure 14-5474. PKTDMA_RXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-16534. PKTDMA_RXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.50 PKTDMA_RXCRT_CHAN_DCNT_j Register

1 PKTDMA_RXCRT_CHAN_DCNT_j Register (Offset = 404h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16535. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0404h + formula

Figure 14-5475. PKTDMA_RXCRT_CHAN_DCNT_j Name Register

31	30	29	28	27	26	25	24
DCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
DCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
DCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
DCNT							
R/WTD							
0h							

Table 14-16537. PKTDMA_RXCRT_CHAN_DCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DCNT	R/WTD	0h	Current dropped packet count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.51 PKTDMA_RXCRT_CHAN_BCNT_j Register

1 PKTDMA_RXCRT_CHAN_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16538. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0408h + formula

Figure 14-5476. PKTDMA_RXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-16540. PKTDMA_RXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.52 PKTDMA_RXCRT_CHAN_SBCNT_j Register

1 PKTDMA_RXCRT_CHAN_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 28d

Table 14-16541. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0410h + formula

Figure 14-5477. PKTDMA_RXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-16543. PKTDMA_RXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.53 PKTDMA_TXCRT_CHAN_CTL_j Register

1 PKTDMA_TXCRT_CHAN_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16544. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0000h + formula**

Figure 14-5478. PKTDMA_TXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
TX_ENABLE	TX_TEARDOWN	TX_PAUSE	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TX_ERROR
NONE							R/W
0h							0h

Table 14-16546. PKTDMA_TXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete. Reset Source: rst_mod_g_rst_n
30	TX_TEARDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	TX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n
28:1	RESERVED	NONE	0h	Reserved

Table 14-16546. PKTDMA_TXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TX_ERROR	R/W	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared by writing back a 0. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.54 PKTDMA_TXCRT_CHAN_STATUS0_j Register

1 PKTDMA_TXCRT_CHAN_STATUS0_j Register (Offset = 40h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16547. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0040h + formula

Figure 14-5479. PKTDMA_TXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
TRING_PEND	TXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	TX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16549. PKTDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	TXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-16549. PKTDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.55 PKTDMA_TXCRT_CHAN_STATUS1_j Register

1 PKTDMA_TXCRT_CHAN_STATUS1_j Register (Offset = 44h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16550. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0044h + formula

Figure 14-5480. PKTDMA_TXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
TX_REQS	RESERVED				SOP_WAVAIL	MOP_WAVAIL	WAVAIL
R	NONE				R	R	R
0h	0h				0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TDNULL
NONE							R
0h							0h
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-16552. PKTDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:27	RESERVED	NONE	0h	Reserved
26	SOP_WAVAIL	R	0h	The FIFO has space for the start of a packet Reset Source: rst_mod_g_rst_n
25	MOP_WAVAIL	R	0h	The FIFO has space for the middle of a packet Reset Source: rst_mod_g_rst_n
24	WAVAIL	R	0h	The fifo has space for a burst size Reset Source: rst_mod_g_rst_n
23:9	RESERVED	NONE	0h	Reserved
8	TDNULL	R	0h	The channel has met the conditions to attempt to teardown Reset Source: rst_mod_g_rst_n
7	CHANNEL_OK	R	0h	The channel is trying to schedule work Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	The channel has active work Reset Source: rst_mod_g_rst_n

Table 14-16552. PKTDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.56 PKTDMA_TXCRT_CHAN_STDATA_j_k Register

1 PKTDMA_TXCRT_CHAN_STDATA_j_k Register (Offset = 80h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the PKTDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 41d, k = 0 to 31d

Table 14-16553. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0080h + formula**

Figure 14-5481. PKTDMA_TXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/NA							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/NA							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/NA							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/NA							
0h							

Table 14-16555. PKTDMA_TXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/NA	0h	See TX State Mapping Table Reset Source: rst_mod_g_rst_n

14.7.1.1.2.57 PKTDMA_TXCRT_CHAN_PEER0_j Register

1 PKTDMA_TXCRT_CHAN_PEER0_j Register (Offset = 200h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16556. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0200h + formula**

Figure 14-5482. PKTDMA_TXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16558. PKTDMA_TXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.58 PKTDMA_TXCRT_CHAN_PEER1_j Register

1 PKTDMA_TXCRT_CHAN_PEER1_j Register (Offset = 204h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16559. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0204h + formula**

Figure 14-5483. PKTDMA_TXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16561. PKTDMA_TXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.59 PKTDMA_TXCRT_CHAN_PEER2_j Register

1 PKTDMA_TXCRT_CHAN_PEER2_j Register (Offset = 208h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16562. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0208h + formula

Figure 14-5484. PKTDMA_TXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16564. PKTDMA_TXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.60 PKTDMA_TXCRT_CHAN_PEER3_j Register

1 PKTDMA_TXCRT_CHAN_PEER3_j Register (Offset = 20Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16565. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 020Ch + formula**

Figure 14-5485. PKTDMA_TXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16567. PKTDMA_TXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.61 PKTDMA_TXCRT_CHAN_PEER4_j Register

1 PKTDMA_TXCRT_CHAN_PEER4_j Register (Offset = 210h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16568. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0210h + formula**

Figure 14-5486. PKTDMA_TXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16570. PKTDMA_TXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.62 PKTDMA_TXCRT_CHAN_PEER5_j Register

1 PKTDMA_TXCRT_CHAN_PEER5_j Register (Offset = 214h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16571. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0214h + formula**

Figure 14-5487. PKTDMA_TXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16573. PKTDMA_TXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.63 PKTDMA_TXCRT_CHAN_PEER6_j Register

1 PKTDMA_TXCRT_CHAN_PEER6_j Register (Offset = 218h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16574. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0218h + formula

Figure 14-5488. PKTDMA_TXCRT_CHAN_PEER6_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16576. PKTDMA_TXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.64 PKTDMA_TXCRT_CHAN_PEER7_j Register

1 PKTDMA_TXCRT_CHAN_PEER7_j Register (Offset = 21Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16577. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 021Ch + formula**

Figure 14-5489. PKTDMA_TXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16579. PKTDMA_TXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.65 PKTDMA_TXCRT_CHAN_PEER8_j Register

1 PKTDMA_TXCRT_CHAN_PEER8_j Register (Offset = 220h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16580. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0220h + formula**

Figure 14-5490. PKTDMA_TXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16582. PKTDMA_TXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.66 PKTDMA_TXCRT_CHAN_PEER9_j Register

1 PKTDMA_TXCRT_CHAN_PEER9_j Register (Offset = 224h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16583. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0224h + formula**

Figure 14-5491. PKTDMA_TXCRT_CHAN_PEER9_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16585. PKTDMA_TXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.67 PKTDMA_TXCRT_CHAN_PEER10_j Register

1 PKTDMA_TXCRT_CHAN_PEER10_j Register (Offset = 228h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16586. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0228h + formula

Figure 14-5492. PKTDMA_TXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16588. PKTDMA_TXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.68 PKTDMA_TXCRT_CHAN_PEER11_j Register

1 PKTDMA_TXCRT_CHAN_PEER11_j Register (Offset = 22Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16589. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 022Ch + formula**

Figure 14-5493. PKTDMA_TXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16591. PKTDMA_TXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.69 PKTDMA_TXCRT_CHAN_PEER12_j Register

1 PKTDMA_TXCRT_CHAN_PEER12_j Register (Offset = 230h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16592. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0230h + formula**

Figure 14-5494. PKTDMA_TXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16594. PKTDMA_TXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.70 PKTDMA_TXCRT_CHAN_PEER13_j Register

1 PKTDMA_TXCRT_CHAN_PEER13_j Register (Offset = 234h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16595. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0234h + formula**

Figure 14-5495. PKTDMA_TXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PEER_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PEER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PEER_DATA							
R/W							
0h							

Table 14-16597. PKTDMA_TXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.71 PKTDMA_TXCRT_CHAN_PEER14_j Register

1 PKTDMA_TXCRT_CHAN_PEER14_j Register (Offset = 238h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16598. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0238h + formula**

Figure 14-5496. PKTDMA_TXCRT_CHAN_PEER14_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16600. PKTDMA_TXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.72 PKTDMA_TXCRT_CHAN_PEER15_j Register

1 PKTDMA_TXCRT_CHAN_PEER15_j Register (Offset = 23Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16601. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 023Ch + formula**

Figure 14-5497. PKTDMA_TXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16603. PKTDMA_TXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.73 PKTDMA_TXCRT_CHAN_PCNT_j Register

1 PKTDMA_TXCRT_CHAN_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16604. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0400h + formula

Figure 14-5498. PKTDMA_TXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-16606. PKTDMA_TXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.74 PKTDMA_TXCRT_CHAN_BCNT_j Register

1 PKTDMA_TXCRT_CHAN_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16607. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4AA0 0408h + formula**

Figure 14-5499. PKTDMA_TXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-16609. PKTDMA_TXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.75 PKTDMA_TXCRT_CHAN_SBCNT_j Register

1 PKTDMA_TXCRT_CHAN_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 41d

Table 14-16610. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0410h + formula

Figure 14-5500. PKTDMA_TXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-16612. PKTDMA_TXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.76 LCDMA_RINGACC_RINGRT_RING_FDB_j Register

1 LCDMA_RINGACC_RINGRT_RING_FDB_j Register (Offset = 10h + formula) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Offset = (j * 2000h); where j = 0 to 287d

Table 14-16613. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4B80 0010h + formula**

Figure 14-5501. LCDMA_RINGACC_RINGRT_RING_FDB_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-16615. LCDMA_RINGACC_RINGRT_RING_FDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.77 LCDMA_RINGACC_RINGRT_RING_FOCC_j Register

1 LCDMA_RINGACC_RINGRT_RING_FOCC_j Register (Offset = 18h + formula) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = (j * 2000h); where j = 0 to 287d

Table 14-16616. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4B80 0018h + formula**

Figure 14-5502. LCDMA_RINGACC_RINGRT_RING_FOCC_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>OCC</td></tr>
<tr><td colspan="7">NONE</td><td>R/NA</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OCC</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OCC</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16618. LCDMA_RINGACC_RINGRT_RING_FOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.7.1.1.2.78 LCDMA_RINGACC_RINGRT_RING_RDB_j Register

1 LCDMA_RINGACC_RINGRT_RING_RDB_j Register (Offset = 1010h + formula) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Offset = (j * 2000h); where j = 0 to 287d

Table 14-16619. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4B80 1010h + formula**

Figure 14-5503. LCDMA_RINGACC_RINGRT_RING_RDB_j Name Register

31	30	29	28	27	26	25	24
TDOWN_ACK	RESERVED						
NA/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-16621. LCDMA_RINGACC_RINGRT_RING_RDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_ACK	NA/W	0h	This bit is set to 1 to ackowledge (and clear) the tdown_complete bit in the corresponding Ring N Occupancy Register. this bit is only valid on the reverse rings (rings consumed by the Host SW) Reset Source: rst_mod_g_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.7.1.1.2.79 LCDMA_RINGACC_RINGRT_RING_ROCC_j Register

1 LCDMA_RINGACC_RINGRT_RING_ROCC_j Register (Offset = 1018h + formula) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = (j * 2000h); where j = 0 to 287d

Table 14-16622. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	**4B80 1018h + formula**

Figure 14-5504. LCDMA_RINGACC_RINGRT_RING_ROCC_j Name Register

31	30	29	28	27	26	25	24
TDOWN_COMPLETE	RESERVED						
R/NA	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							OCC
NONE							R/NA
0h							0h
15	14	13	12	11	10	9	8
OCC							
R/NA							
0h							
7	6	5	4	3	2	1	0
OCC							
R/NA							
0h							

Table 14-16624. LCDMA_RINGACC_RINGRT_RING_ROCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_COMPLETE	R/NA	0h	This bit when set indicates that a teardown is complete on the channel. This bit is cleared anytime the tdown_ack bit is written as a 1 in the corresponding Ring N Doorbell Register. This bit is only valid on the reverse rings (rings consumed by the Host SW). Reset Source: rst_mod_g_rst_n
30:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.7.1.2 DMASS_BCDMA_0

DMASS_BCDMA_0

14.7.1.2.1 DMASS_BCDMA_0 Summaries

DMASS_BCDMA_0 Summaries

Table 14-16625. LCDMA_RINGACC_CRED Registers, Base Address=4840 0000h, Length=2048

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	LCDMA_RINGACC_CRED_RING_CRED_J	4840 0000h + formula

Table 14-16626. BCDMA_BCCFG Registers, Base Address=4842 0000h, Length=8192

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_BCCFG_CHAN_CFG_J	4842 0000h + formula
64h	32	BCDMA_BCCFG_CHAN_PRI_CTRL_J	4842 0064h + formula
80h	32	BCDMA_BCCFG_CHAN_TST_SCHED_J	4842 0080h + formula

Table 14-16627. BCDMA_TXCCFG Registers, Base Address=484A 4000h, Length=8192

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_TXCCFG_CHAN_TCFG_J	484A 4000h + formula
64h	32	BCDMA_TXCCFG_CHAN_TPRI_CTRL_J	484A 4064h + formula
68h	32	BCDMA_TXCCFG_CHAN_THREAD_J	484A 4068h + formula
70h	32	BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_J	484A 4070h + formula
80h	32	BCDMA_TXCCFG_CHAN_TST_SCHED_J	484A 4080h + formula

Table 14-16628. BCDMA_RXCCFG Registers, Base Address=484C 2000h, Length=8192

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_RXCCFG_CHAN_RCFG_J	484C 2000h + formula
64h	32	BCDMA_RXCCFG_CHAN_RPRI_CTRL_J	484C 2064h + formula
68h	32	BCDMA_RXCCFG_CHAN_THREAD_J	484C 2068h + formula
80h	32	BCDMA_RXCCFG_CHAN_RST_SCHED_J	484C 2080h + formula

Table 14-16629. BCDMA_GCFG Registers, Base Address=485C 0100h, Length=256

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_GCFG_REVISION	485C 0100h
4h	32	BCDMA_GCFG_PERF_CTRL	485C 0104h
8h	32	BCDMA_GCFG_EMU_CTRL	485C 0108h
10h	32	BCDMA_GCFG_PSIL_TO	485C 0110h
20h	32	BCDMA_GCFG_CAP0	485C 0120h
24h	32	BCDMA_GCFG_CAP1	485C 0124h
28h	32	BCDMA_GCFG_CAP2	485C 0128h
2Ch	32	BCDMA_GCFG_CAP3	485C 012Ch
30h	32	BCDMA_GCFG_CAP4	485C 0130h
60h	32	BCDMA_GCFG_PM0	485C 0160h
64h	32	BCDMA_GCFG_PM1	485C 0164h

Table 14-16629. BCDMA_GCFG Registers, Base Address=485C 0100h, Length=256 (continued)

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
78h	32	BCDMA_GCFG_DBGADDR	485C 0178h
7Ch	32	BCDMA_GCFG_DBGDATA	485C 017Ch

Table 14-16630. LCDMA_RINGACC_RING_CFG Registers, Base Address=4860 0000h, Length=32768

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
40h	32	LCDMA_RINGACC_RING_CFG_RING_BA_LO_J	4860 0040h + formula
44h	32	LCDMA_RINGACC_RING_CFG_RING_BA_HI_J	4860 0044h + formula
48h	32	LCDMA_RINGACC_RING_CFG_RING_SIZE_J	4860 0048h + formula

Table 14-16631. BCDMA_RXCRT Registers, Base Address=4A82 0000h, Length=131072

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_RXCRT_CHAN_CTL_J	4A82 0000h + formula
8h	32	BCDMA_RXCRT_CHAN_SWTRIG_J	4A82 0008h + formula
40h	32	BCDMA_RXCRT_CHAN_STATUS0_J	4A82 0040h + formula
44h	32	BCDMA_RXCRT_CHAN_STATUS1_J	4A82 0044h + formula
80h	32	BCDMA_RXCRT_CHAN_STDATA_J_K	4A82 0080h + formula
200h	32	BCDMA_RXCRT_CHAN_PEER0_J	4A82 0200h + formula
204h	32	BCDMA_RXCRT_CHAN_PEER1_J	4A82 0204h + formula
208h	32	BCDMA_RXCRT_CHAN_PEER2_J	4A82 0208h + formula
20Ch	32	BCDMA_RXCRT_CHAN_PEER3_J	4A82 020Ch + formula
210h	32	BCDMA_RXCRT_CHAN_PEER4_J	4A82 0210h + formula
214h	32	BCDMA_RXCRT_CHAN_PEER5_J	4A82 0214h + formula
218h	32	BCDMA_RXCRT_CHAN_PEER6_J	4A82 0218h + formula
21Ch	32	BCDMA_RXCRT_CHAN_PEER7_J	4A82 021Ch + formula
220h	32	BCDMA_RXCRT_CHAN_PEER8_J	4A82 0220h + formula
224h	32	BCDMA_RXCRT_CHAN_PEER9_J	4A82 0224h + formula
228h	32	BCDMA_RXCRT_CHAN_PEER10_J	4A82 0228h + formula
22Ch	32	BCDMA_RXCRT_CHAN_PEER11_J	4A82 022Ch + formula
230h	32	BCDMA_RXCRT_CHAN_PEER12_J	4A82 0230h + formula
234h	32	BCDMA_RXCRT_CHAN_PEER13_J	4A82 0234h + formula
238h	32	BCDMA_RXCRT_CHAN_PEER14_J	4A82 0238h + formula
23Ch	32	BCDMA_RXCRT_CHAN_PEER15_J	4A82 023Ch + formula
400h	32	BCDMA_RXCRT_CHAN_PCNT_J	4A82 0400h + formula
408h	32	BCDMA_RXCRT_CHAN_BCNT_J	4A82 0408h + formula
410h	32	BCDMA_RXCRT_CHAN_SBCNT_J	4A82 0410h + formula

Table 14-16632. BCDMA_TXCRT Registers, Base Address=4AA4 0000h, Length=131072

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_TXCRT_CHAN_CTL_J	4AA4 0000h + formula
8h	32	BCDMA_TXCRT_CHAN_SWTRIG_J	4AA4 0008h + formula
40h	32	BCDMA_TXCRT_CHAN_STATUS0_J	4AA4 0040h + formula
44h	32	BCDMA_TXCRT_CHAN_STATUS1_J	4AA4 0044h + formula
80h	32	BCDMA_TXCRT_CHAN_STDATA_J_K	4AA4 0080h + formula

Table 14-16632. BCDMA_TXCRT Registers, Base Address=4AA4 0000h, Length=131072 (continued)

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
200h	32	BCDMA_TXCRT_CHAN_PEER0_J	4AA4 0200h + formula
204h	32	BCDMA_TXCRT_CHAN_PEER1_J	4AA4 0204h + formula
208h	32	BCDMA_TXCRT_CHAN_PEER2_J	4AA4 0208h + formula
20Ch	32	BCDMA_TXCRT_CHAN_PEER3_J	4AA4 020Ch + formula
210h	32	BCDMA_TXCRT_CHAN_PEER4_J	4AA4 0210h + formula
214h	32	BCDMA_TXCRT_CHAN_PEER5_J	4AA4 0214h + formula
218h	32	BCDMA_TXCRT_CHAN_PEER6_J	4AA4 0218h + formula
21Ch	32	BCDMA_TXCRT_CHAN_PEER7_J	4AA4 021Ch + formula
220h	32	BCDMA_TXCRT_CHAN_PEER8_J	4AA4 0220h + formula
224h	32	BCDMA_TXCRT_CHAN_PEER9_J	4AA4 0224h + formula
228h	32	BCDMA_TXCRT_CHAN_PEER10_J	4AA4 0228h + formula
22Ch	32	BCDMA_TXCRT_CHAN_PEER11_J	4AA4 022Ch + formula
230h	32	BCDMA_TXCRT_CHAN_PEER12_J	4AA4 0230h + formula
234h	32	BCDMA_TXCRT_CHAN_PEER13_J	4AA4 0234h + formula
238h	32	BCDMA_TXCRT_CHAN_PEER14_J	4AA4 0238h + formula
23Ch	32	BCDMA_TXCRT_CHAN_PEER15_J	4AA4 023Ch + formula
400h	32	BCDMA_TXCRT_CHAN_PCNT_J	4AA4 0400h + formula
408h	32	BCDMA_TXCRT_CHAN_BCNT_J	4AA4 0408h + formula
410h	32	BCDMA_TXCRT_CHAN_SBCNT_J	4AA4 0410h + formula

Table 14-16633. LCDMA_RINGACC_RINGRT Registers, Base Address=4BC0 0000h, Length=1048576

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
10h	32	LCDMA_RINGACC_RINGRT_RING_FDB_J	4BC0 0010h + formula
18h	32	LCDMA_RINGACC_RINGRT_RING_FOCC_J	4BC0 0018h + formula
1010h	32	LCDMA_RINGACC_RINGRT_RING_RDB_J	4BC0 1010h + formula
1018h	32	LCDMA_RINGACC_RINGRT_RING_ROCC_J	4BC0 1018h + formula

Table 14-16634. BCDMA_BCRT Registers, Base Address=4C00 0000h, Length=131072

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_BCRT_CHAN_CTL_J	4C00 0000h + formula
8h	32	BCDMA_BCRT_CHAN_SWTRIG_J	4C00 0008h + formula
40h	32	BCDMA_BCRT_CHAN_STATUS0_J	4C00 0040h + formula
44h	32	BCDMA_BCRT_CHAN_STATUS1_J	4C00 0044h + formula
48h	32	BCDMA_BCRT_CHAN_STATUS2_J	4C00 0048h + formula
4Ch	32	BCDMA_BCRT_CHAN_STATUS3_J	4C00 004Ch + formula
80h	32	BCDMA_BCRT_CHAN_STDATA_J_K	4C00 0080h + formula
100h	32	BCDMA_BCRT_CHAN_STDATAW_J_K	4C00 0100h + formula
400h	32	BCDMA_BCRT_CHAN_PCNT_J	4C00 0400h + formula
408h	32	BCDMA_BCRT_CHAN_BCNT_J	4C00 0408h + formula
410h	32	BCDMA_BCRT_CHAN_SBCNT_J	4C00 0410h + formula

14.7.1.2.2 DMASS_BCDMA_0 Registers

DMASS_BCDMA_0 Registers

14.7.1.2.2.1 LCDMA_RINGACC_CRED_RING_CRED_j Register

1 LCDMA_RINGACC_CRED_RING_CRED_j Register (Offset = 0h + formula) [reset = 0h]

The Credentials Register provides credentials to be used when performing memory accesses using this flow.

Return to Summary Table

Offset = (j * 10h); where j = 0 to 67d

Table 14-16635. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4840 0000h + formula**

Figure 14-5505. LCDMA_RINGACC_CRED_RING_CRED_j Name Register

31	30	29	28	27	26	25	24
RESERVED					SECURE	PRIV	
NONE					R/W	R/W	
0h					0h	0h	
23	22	21	20	19	18	17	16
PRIVID							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16637. LCDMA_RINGACC_CRED_RING_CRED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	SECURE	R/W	0h	Secure attribute Reset Source: rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Privelege attribute Reset Source: rst_mod_g_rst_n
23:16	PRIVID	R/W	0h	Privelege ID attribute Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.2 BCDMA_BCCFG_CHAN_CFG_j Register

1 BCDMA_BCCFG_CHAN_CFG_j Register (Offset = 0h + formula) [reset = C0400h]

The Channel Configuration Register is used to initialize static mode settings for the Block Copy DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

Return to Summary Table

Offset = (j * 100h); where j = 0 to 27d

Table 14-16638. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4842 0000h + formula**

Figure 14-5506. BCDMA_BCCFG_CHAN_CFG_j Name Register

31	30	29	28	27	26	25	24
PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				CHAN_TYPE			
NONE				R/NA			
0h				Ch			
15	14	13	12	11	10	9	8
RESERVED				BURST_SIZE		RESERVED	
NONE				R/W		NONE	
0h				1h		0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16640. BCDMA_BCCFG_CHAN_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	CHAN_TYPE	R/NA	Ch	Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-11 = RESERVED 12 = Channel performs Third Party Block Copy DMA transfers from memory to memory using pass by reference rings. 13-15 = RESERVED Reset Source: rst_mod_g_rst_n 12 `Pass by reference block copy`
15:12	RESERVED	NONE	0h	Reserved

Table 14-16640. BCDMA_BCCFG_CHAN_CFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes All other values are reserved The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n
9:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.3 BCDMA_BCCFG_CHAN_PRI_CTRL_j Register

1 BCDMA_BCCFG_CHAN_PRI_CTRL_j Register (Offset = 64h + formula) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 27d

Table 14-16641. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4842 0064h + formula**

Figure 14-5507. BCDMA_BCCFG_CHAN_PRI_CTRL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="3">PRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ORDERID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-16643. BCDMA_BCCFG_CHAN_PRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.4 BCDMA_BCCFG_CHAN_TST_SCHED_j Register

1 BCDMA_BCCFG_CHAN_TST_SCHED_j Register (Offset = 80h + formula) [reset = 0h]

The Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Return to Summary Table

Offset = (j * 100h); where j = 0 to 27d

Table 14-16644. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4842 0080h + formula

Figure 14-5508. BCDMA_BCCFG_CHAN_TST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-16646. BCDMA_BCCFG_CHAN_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx/Rx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.5 BCDMA_TXCCFG_CHAN_TCFG_j Register

1 BCDMA_TXCCFG_CHAN_TCFG_j Register (Offset = 0h + formula) [reset = A0400h]

The Tx Channel Configuration Register is used to initialize static mode settings for the Tx DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16647. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484A 4000h + formula**

Figure 14-5509. BCDMA_TXCCFG_CHAN_TCFG_j Name Register

31	30	29	28	27	26	25	24
TX_PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				TX_CHAN_TYPE			
NONE				R/NA			
0h				Ah			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TX_BURST_SIZE		TX_TDTYPE	TX_NOTDPKT
NONE				R/W		R/W	R/W
0h				1h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-16649. BCDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	TX_CHAN_TYPE	R/NA	Ah	Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-9 = RESERVED 10 = Channel performs Third Party Block Copy DMA transfers from memory to PSI-L using pass by reference rings. 11-15 = RESERVED Reset Source: rst_mod_g_rst_n `12      Pass by reference block copy`
15:12	RESERVED	NONE	0h	Reserved

Table 14-16649. BCDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	TX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes All other values are reserved The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n
9	TX_TDTYPE	R/W	0h	Specifies whether or not the channel should immediately return a teardown completion response to the default completion queue or wait until a status message is returned from the remote PSI-L paired peripheral. 0 = return immediately once all traffic is complete in BCDMA. 1 = wait until remote peer sends back a completion message. Reset Source: rst_mod_g_rst_n
8	TX_NOTDPKT	R/W	0h	Specifies whether or not the channel should suppress sending the single data phase teardown packet when teardown is complete. 0 = TD packet is sent 1 = Suppress sending TD packet Reset Source: rst_mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.6 BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Register

1 BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Register (Offset = 64h + formula) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16650. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484A 4064h + formula**

Figure 14-5510. BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-16652. BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Tx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Tx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.7 BCDMA_TXCCFG_CHAN_THREAD_j Register

1 BCDMA_TXCCFG_CHAN_THREAD_j Register (Offset = 68h + formula) [reset = 0h]

The thread ID mapping register is used to pair the Tx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16653. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484A 4068h + formula**

Figure 14-5511. BCDMA_TXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-16655. BCDMA_TXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.8 BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register

1 BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register (Offset = 70h + formula) [reset = C0h]

The fifo depth register is used to specify how many FIFO data phases deep the Tx per channel FIFO will be for the channel. While the maximum depth of the Tx FIFO is set at design time, the FIFO depth can be artificially reduced in order to control the maximum latency which can be introduced due to buffering effects.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16656. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484A 4070h + formula**

Figure 14-5512. BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FDEPTH							
R/W							
C0h							

Table 14-16658. BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDEPTH	R/W	C0h	FIFO Depth: This field contains the number of Tx FIFO bytes which will be allowed to be stored for the channel. The minimum value is equal to the PSI-L interface data path width (tstrm_wdth), the maximum value varies by channel class (ultra-high capacity/high capacity/normal capacity) and is equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L data path width (tstrm_wdth). The fdepth must always be an integer multiple of tstrm_wdth. The reset value of this register varies by channel class (ultra-high capacity/high capacity/normal capacity) but will be equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L interface data width (tstrm_wdth). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.9 BCDMA_TXCCFG_CHAN_TST_SCHED_j Register

1 BCDMA_TXCCFG_CHAN_TST_SCHED_j Register (Offset = 80h + formula) [reset = 0h]

The Tx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16659. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484A 4080h + formula**

Figure 14-5513. BCDMA_TXCCFG_CHAN_TST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-16661. BCDMA_TXCCFG_CHAN_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Tx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.10 BCDMA_RXCCFG_CHAN_RCFG_j Register

1 BCDMA_RXCCFG_CHAN_RCFG_j Register (Offset = 0h + formula) [reset = A0400h]

The Rx Channel Configuration Register is used to initialize static mode settings for the Rx DMA channel. This register may only be written when the channel is disabled (rx_enable in realtime control reg is 0).

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16662. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484C 2000h + formula

Figure 14-5514. BCDMA_RXCCFG_CHAN_RCFG_j Name Register

31	30	29	28	27	26	25	24
RX_PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				RX_CHAN_TYPE			
NONE				R/NA			
0h				Ah			
15	14	13	12	11	10	9	8
RESERVED	RX_IGNORE_LONG	RESERVED		RX_BURST_SIZE		RESERVED	
NONE	R/W	NONE		R/W		NONE	
0h	0h	0h		1h		0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16664. BCDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	RX_CHAN_TYPE	R/NA	Ah	Rx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-9 = RESERVED 10 = Channel performs Third Party Block Copy DMA transfers from PSI-L to memory using pass by reference rings. 11-15 = RESERVED Reset Source: rst_mod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-16664. BCDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RX_IGNORE_LONG	R/W	0h	This field controls whether or not long packets will be treated as exceptions or ignored for the channel. This field is only used when the channel is in split UTC mode. The values are encoded as follows: 0 = Long packets are treated as exceptions and handled appropriately. 1 = Long packets are ignored and the next TR will be fetched even if the current TR is marked or interpreted as EOP. Reset Source: rst_mod_g_rst_n
13:12	RESERVED	NONE	0h	Reserved
11:10	RX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes only if the channel buffer size is greater than 128 bytes All other values are reserved The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n
9:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.11 BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Register

1 BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Register (Offset = 64h + formula) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16665. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484C 2064h + formula**

Figure 14-5515. BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-16667. BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Rx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem*_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Rx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.12 BCDMA_RXCCFG_CHAN_THREAD_j Register

1 BCDMA_RXCCFG_CHAN_THREAD_j Register (Offset = 68h + formula) [reset = 0h]

The thread ID mapping register is used to pair the Rx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16668. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**484C 2068h + formula**

Figure 14-5516. BCDMA_RXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-16670. BCDMA_RXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.13 BCDMA_RXCCFG_CHAN_RST_SCHED_j Register

1 BCDMA_RXCCFG_CHAN_RST_SCHED_j Register (Offset = 80h + formula) [reset = 0h]

The Rx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Return to Summary Table

Offset = (j * 100h); where j = 0 to 19d

Table 14-16671. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484C 2080h + formula

Figure 14-5517. BCDMA_RXCCFG_CHAN_RST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-16673. BCDMA_RXCCFG_CHAN_RST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Rx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Rx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.14 BCDMA_GCFG_REVISION Register

1 BCDMA_GCFG_REVISION Register (Offset = 0h) [reset = 662EB101h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-16674. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0100h**

Figure 14-5518. BCDMA_GCFG_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
662Eh							
23	22	21	20	19	18	17	16
MODID							
R							
662Eh							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
16h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-16676. BCDMA_GCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	662Eh	Module ID field Reset Source: rst_mod_g_rst_n
15:11	REVRTL	R	16h	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: rst_mod_g_rst_n

14.7.1.2.2.15 BCDMA_GCFG_PERF_CTRL Register

1 BCDMA_GCFG_PERF_CTRL Register (Offset = 4h) [reset = 40h]

The performance control register contains fields which can be used to adjust the performance of the BCDMA in the system.

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Table 14-16677. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0104h**

Figure 14-5519. BCDMA_GCFG_PERF_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TIMEOUT_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">40h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TIMEOUT_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">40h</td></tr>
</table>

Table 14-16679. BCDMA_GCFG_PERF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TIMEOUT_CNT	R/W	40h	This feature is not currently supported. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.16 BCDMA_GCFG_EMU_CTRL Register

1 BCDMA_GCFG_EMU_CTRL Register (Offset = 8h) [reset = 0h]

The emulation control register is used to control the behavior of the DMA when the emususp input is asserted.

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Table 14-16680. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0108h**

Figure 14-5520. BCDMA_GCFG_EMU_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-16682. BCDMA_GCFG_EMU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Soft Reset Source: rst_mod_g_rst_n
0	FREE	R/W	0h	Free Reset Source: rst_mod_g_rst_n

14.7.1.2.2.17 BCDMA_GCFG_PSIL_TO Register

1 BCDMA_GCFG_PSIL_TO Register (Offset = 10h) [reset = 400h]

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrances on PSI-L configuration transactions issued by the built in PSI-L proxy.

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Table 14-16683. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0110h

Figure 14-5521. BCDMA_GCFG_PSIL_TO Name Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W							
400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W							
400h							

Table 14-16685. BCDMA_GCFG_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a conifiguration read or write transaction and asserting the tout bit Reset Source: rst_mod_g_rst_n

14.7.1.2.2.18 BCDMA_GCFG_CAP0 Register

1 BCDMA_GCFG_CAP0 Register (Offset = 20h) [reset = A800Fh]

The Capabilities Register 0 specifies which standard features this BCDMA instance supports.

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Table 14-16686. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0120h**

Figure 14-5522. BCDMA_GCFG_CAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				GLOBAL_TRIG	LOCAL_TRIG	EOL	STATIC
NONE				R	R	R	R
0h				1h	0h	1h	0h
15	14	13	12	11	10	9	8
TYPE15	TYPE14	TYPE13	TYPE12	TYPE11	TYPE10	TYPE9	TYPE8
R	R	R	R	R	R	R	R
1h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TYPE7	TYPE6	TYPE5	TYPE4	TYPE3	TYPE2	TYPE1	TYPE0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	1h	1h	1h	1h

Table 14-16688. BCDMA_GCFG_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GLOBAL_TRIG	R	1h	Global triggers 0 and 1 are supported Reset Source: rst_mod_g_rst_n
18	LOCAL_TRIG	R	0h	Dedicated local trigger is supported Reset Source: rst_mod_g_rst_n
17	EOL	R	1h	EOL field is supported Reset Source: rst_mod_g_rst_n
16	STATIC	R	0h	STATIC field is supported Reset Source: rst_mod_g_rst_n
15	TYPE15	R	1h	Type 15 TR is supported Reset Source: rst_mod_g_rst_n
14	TYPE14	R	0h	Type 14 TR is supported Reset Source: rst_mod_g_rst_n
13	TYPE13	R	0h	Type 13 TR is supported Reset Source: rst_mod_g_rst_n
12	TYPE12	R	0h	Type 12 TR is supported Reset Source: rst_mod_g_rst_n

Table 14-16688. BCDMA_GCFG_CAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TYPE11	R	0h	Type 11 TR is supported Reset Source: rst_mod_g_rst_n
10	TYPE10	R	0h	Type 10 TR is supported Reset Source: rst_mod_g_rst_n
9	TYPE9	R	0h	Type 9 TR is supported Reset Source: rst_mod_g_rst_n
8	TYPE8	R	0h	Type 8 TR is supported Reset Source: rst_mod_g_rst_n
7	TYPE7	R	0h	Type 7 TR is supported Reset Source: rst_mod_g_rst_n
6	TYPE6	R	0h	Type 6 TR is supported Reset Source: rst_mod_g_rst_n
5	TYPE5	R	0h	Type 5 TR is supported Reset Source: rst_mod_g_rst_n
4	TYPE4	R	0h	Type 4 TR is supported Reset Source: rst_mod_g_rst_n
3	TYPE3	R	1h	Type 3 TR is supported Reset Source: rst_mod_g_rst_n
2	TYPE2	R	1h	Type 2 TR is supported Reset Source: rst_mod_g_rst_n
1	TYPE1	R	1h	Type 1 TR is supported Reset Source: rst_mod_g_rst_n
0	TYPE0	R	1h	Type 0 TR is supported Reset Source: rst_mod_g_rst_n

14.7.1.2.2.19 BCDMA_GCFG_CAP1 Register

1 BCDMA_GCFG_CAP1 Register (Offset = 24h) [reset = 0h]

The Capabilities Register 1 specifies which standard features this BCDMA instance supports.

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Table 14-16689. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0124h**

Figure 14-5523. BCDMA_GCFG_CAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SECTR	DFMT	ELTYPE	AMODE
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-16691. BCDMA_GCFG_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	SECTR	R	0h	Maximum second TR function that is supported Reset Source: rst_mod_g_rst_n
2	DFMT	R	0h	Maximum data reformatting function that is supported Reset Source: rst_mod_g_rst_n
1	ELTYPE	R	0h	Maximum element type value that is supported. Reset Source: rst_mod_g_rst_n
0	AMODE	R	0h	The maximum AMODE that is supported. If AMODE is supported then DIR field must be supported for that AMODE. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.20 BCDMA_GCFG_CAP2 Register

1 BCDMA_GCFG_CAP2 Register (Offset = 28h) [reset = 50281Ch]

The Capabilities Register 2 specifies how many resources this BCDMA instance supports.

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Table 14-16692. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0128h**

Figure 14-5524. BCDMA_GCFG_CAP2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">RCHAN_CNT</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">14h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RCHAN_CNT</td><td colspan="2">TCHAN_CNT</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">14h</td><td colspan="2">14h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">TCHAN_CNT</td><td>CHAN_CNT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">14h</td><td>1Ch</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CHAN_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1Ch</td></tr>
</table>

Table 14-16694. BCDMA_GCFG_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:18	RCHAN_CNT	R	14h	Rx split channel count Reset Source: rst_mod_g_rst_n
17:9	TCHAN_CNT	R	14h	Tx split channel count Reset Source: rst_mod_g_rst_n
8:0	CHAN_CNT	R	1Ch	BC channel count Reset Source: rst_mod_g_rst_n

14.7.1.2.2.21 BCDMA_GCFG_CAP3 Register

1 BCDMA_GCFG_CAP3 Register (Offset = 2Ch) [reset = 0h]

The Capabilities Register 3 specifies how many resources this BCDMA instance supports.

Return to Summary Table

Table 14-16695. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 012Ch**

Figure 14-5525. BCDMA_GCFG_CAP3 Name Register

31	30	29	28	27	26	25	24
UCHAN_CNT							
R							
0h							
23	22	21	20	19	18	17	16
UCHAN_CNT	HCHAN_CNT						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
HCHAN_CNT		RESERVED					
R		NONE					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16697. BCDMA_GCFG_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	UCHAN_CNT	R	0h	BC ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
22:14	HCHAN_CNT	R	0h	BC high capacity internal channel count Reset Source: rst_mod_g_rst_n
13:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.22 BCDMA_GCFG_CAP4 Register

1 BCDMA_GCFG_CAP4 Register (Offset = 30h) [reset = 0h]

The Capabilities Register 4 specifies how many resources this BCDMA instance supports.

Return to Summary Table

Table 14-16698. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0130h**

Figure 14-5526. BCDMA_GCFG_CAP4 Name Register

31	30	29	28	27	26	25	24
TUCHAN_CNT							
R							
0h							
23	22	21	20	19	18	17	16
THCHAN_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RUCHAN_CNT							
R							
0h							
7	6	5	4	3	2	1	0
RHCHAN_CNT							
R							
0h							

Table 14-16700. BCDMA_GCFG_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TUCHAN_CNT	R	0h	TX ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
23:16	THCHAN_CNT	R	0h	TX high capacity internal channel count Reset Source: rst_mod_g_rst_n
15:8	RUCHAN_CNT	R	0h	RX ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
7:0	RHCHAN_CNT	R	0h	RX high capacity internal channel count Reset Source: rst_mod_g_rst_n

14.7.1.2.2.23 BCDMA_GCFG_PM0 Register

1 BCDMA_GCFG_PM0 Register (Offset = 60h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

Return to Summary Table

Table 14-16701. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0160h**

Figure 14-5527. BCDMA_GCFG_PM0 Name Register

31	30	29	28	27	26	25	24
NOGATE_RSVD4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOGATE_RSVD4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOGATE_RSVD4	NOGATE_RDEC2	NOGATE_RSVD3		NOGATE_SDEC3	NOGATE_RSVD2		
R/W	R/W	R/W		R/W	R/W		
0h	0h	0h		0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOGATE_WARB3	NOGATE_RSVD1			NOGATE_CARB3	NOGATE_CARB2	NOGATE_RSVD0	
R/W	R/W			R/W	R/W	R/W	
0h	0h			0h	0h	0h	

Table 14-16703. BCDMA_GCFG_PM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	NOGATE_RSVD4	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
14	NOGATE_RDEC2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
13:12	NOGATE_RSVD3	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
11	NOGATE_SDEC3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
10:8	NOGATE_RSVD2	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
7	NOGATE_WARB3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
6:4	NOGATE_RSVD1	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
3	NOGATE_CARB3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-16703. BCDMA_GCFG_PM0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NOGATE_CARB2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
1:0	NOGATE_RSVD0	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.24 BCDMA_GCFG_PM1 Register

1 BCDMA_GCFG_PM1 Register (Offset = 64h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

Return to Summary Table

Table 14-16704. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0164h**

Figure 14-5528. BCDMA_GCFG_PM1 Name Register

31	30	29	28	27	26	25	24
NOGATE_EDC	NOGATE_STATS	NOGATE_PROXY	NOGATE_PSILIF	NOGATE_P2P	NOGATE_RSVD8	NOGATE_EHANDLER	NOGATE_RINGOCC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOGATE_RPCF	NOGATE_TPCF	NOGATE_PCF	NOGATE_RSVD7		NOGATE_CFG	NOGATE_RSVD6	
R/W	R/W	R/W	R/W		R/W	R/W	
0h	0h	0h	0h		0h	0h	
15	14	13	12	11	10	9	8
NOGATE_RSVD6					NOGATE_TRCU	NOGATE_RSVD5	NOGATE_EVTCU
R/W					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
NOGATE_RWU3	NOGATE_RWU2	NOGATE_RWU1	NOGATE_RWU0	NOGATE_TRU3	NOGATE_TRU2	NOGATE_TRU1	NOGATE_TRU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-16706. BCDMA_GCFG_PM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOGATE_EDC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
30	NOGATE_STATS	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
29	NOGATE_PROXY	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
28	NOGATE_PSILIF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
27	NOGATE_P2P	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
26	NOGATE_RSVD8	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
25	NOGATE_EHANDLER	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-16706. BCDMA_GCFG_PM1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NOGATE_RINGOCC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
23	NOGATE_RPCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
22	NOGATE_TPCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
21	NOGATE_PCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
20:19	NOGATE_RSVD7	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
18	NOGATE_CFG	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
17:11	NOGATE_RSVD6	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
10	NOGATE_TRCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
9	NOGATE_RSVD5	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
8	NOGATE_EVTCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
7	NOGATE_RWU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
6	NOGATE_RWU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
5	NOGATE_RWU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
4	NOGATE_RWU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
3	NOGATE_TRU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
2	NOGATE_TRU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
1	NOGATE_TRU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
0	NOGATE_TRU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.25 BCDMA_GCFG_DBGADDR Register

1 BCDMA_GCFG_DBGADDR Register (Offset = 78h) [reset = 0h]

This register provides a writable address which allows debug information to be read from the Debug Data Register

Return to Summary Table

Table 14-16707. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 0178h**

Figure 14-5529. BCDMA_GCFG_DBGADDR Name Register

31	30	29	28	27	26	25	24
DBG_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DBG_UNIT							
R/W							
0h							
7	6	5	4	3	2	1	0
DBG_ADDR							
R/W							
0h							

Table 14-16709. BCDMA_GCFG_DBGADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBG_EN	R/W	0h	Debug enable Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	DBG_UNIT	R/W	0h	Selects which unit to read debug information from Reset Source: rst_mod_g_rst_n
7:0	DBG_ADDR	R/W	0h	Selects offset within unit to access seperate debug registers Reset Source: rst_mod_g_rst_n

14.7.1.2.2.26 BCDMA_GCFG_DBGDATA Register

1 BCDMA_GCFG_DBGDATA Register (Offset = 7Ch) [reset = 0h]

This register provides read only debug data

Return to Summary Table

Table 14-16710. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**485C 017Ch**

Figure 14-5530. BCDMA_GCFG_DBGDATA Name Register

31	30	29	28	27	26	25	24
DBG_DATA							
R/NA							
0h							
23	22	21	20	19	18	17	16
DBG_DATA							
R/NA							
0h							
15	14	13	12	11	10	9	8
DBG_DATA							
R/NA							
0h							
7	6	5	4	3	2	1	0
DBG_DATA							
R/NA							
0h							

Table 14-16712. BCDMA_GCFG_DBGDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBG_DATA	R/NA	0h	Provides debug information from various internal units. The value which is read back depends on which unit and register are selected in the Debug Address Register Reset Source: rst_mod_g_rst_n

14.7.1.2.2.27 LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register

1 LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register (Offset = 40h + formula) [reset = 0h]

The Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 67d

Table 14-16713. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4860 0040h + formula**

Figure 14-5531. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Name Register

31	30	29	28	27	26	25	24
ADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_LO							
R/W							
0h							

Table 14-16715. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_LO	R/W	0h	Ring base address (LSBs) Reset Source: rst_mod_g_rst_n

14.7.1.2.2.28 LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register

1 LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register (Offset = 44h + formula) [reset = 0h]

The Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 67d

Table 14-16716. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4860 0044h + formula**

Figure 14-5532. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				ASEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADDR_HI			
NONE				R/W			
0h				0h			

Table 14-16718. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	ASEL	R/W	0h	Ring base address select Reset Source: rst_mod_g_rst_n
15:4	RESERVED	NONE	0h	Reserved
3:0	ADDR_HI	R/W	0h	Ring base address (MSBs) Reset Source: rst_mod_g_rst_n

14.7.1.2.2.29 LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register

1 LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register (Offset = 48h + formula) [reset = 21000000h]

The Ring Size Register contains the element count for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 67d

Table 14-16719. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4860 0048h + formula**

Figure 14-5533. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Name Register

31	30	29	28	27	26	25	24
QMODE			RESERVED		RING_ELSIZE		
R/NA			NONE		R/NA		
1h			0h		1h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SIZE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE							
R/W							
0h							

Table 14-16721. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	QMODE	R/NA	1h	Defines the mode for this ring or queue. Reset Source: rst_mod_g_rst_n `1 exposed ring mode with dual queues (forward/reverse) for SW direct access`
28:27	RESERVED	NONE	0h	Reserved
26:24	RING_ELSIZE	R/NA	1h	Reset Source: rst_mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:0	SIZE	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.30 BCDMA_RXCRT_CHAN_CTL_j Register

1 BCDMA_RXCRT_CHAN_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Rx Channel Realtime Control Register contains real-time control and status information for the Rx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16722. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0000h + formula**

Figure 14-5534. BCDMA_RXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
RX_ENABLE	RX_TEARDOWN	RX_PAUSE	RX_FORCED_TEARDOWN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						RX_STARVATION	RX_ERROR
NONE						R	R
0h						0h	0h

Table 14-16724. BCDMA_RXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in overflow conditions in the attached application and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit shoudl be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate tha the channel teardown is complete. If the host is enabling a channel that is just being set up, the host must initialize all of the other channel configuration fields before setting this bit. Reset Source: rst_mod_g_rst_n
30	RX_TEARDOWN	R/W	0h	This field indicates whether or not an Rx teardown operation is complete. This field should be cleared when a channel is initialized. This field will be set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n

Table 14-16724. BCDMA_RXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	RX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n
28	RX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Uso fo this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:2	RESERVED	NONE	0h	Reserved
1	RX_STARVATION	R	0h	Rx starvation. This bit is set if the port receives a packet and the ring is empty. The bit clears when the doorbell is written with a positive value. Reset Source: rst_mod_g_rst_n
0	RX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared when the channel is disabled and re-enabled. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.31 BCDMA_RXCRT_CHAN_SWTRIG_j Register

1 BCDMA_RXCRT_CHAN_SWTRIG_j Register (Offset = 8h + formula) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16725. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0008h + formula**

Figure 14-5535. BCDMA_RXCRT_CHAN_SWTRIG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TRIGGER</td></tr>
<tr><td colspan="7">NONE</td><td>NA/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-16727. BCDMA_RXCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.7.1.2.2.32 BCDMA_RXCRT_CHAN_STATUS0_j Register

1 BCDMA_RXCRT_CHAN_STATUS0_j Register (Offset = 40h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16728. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0040h + formula**

Figure 14-5536. BCDMA_RXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
RRING_PEND	RXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	RX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-16730. BCDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	RXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-16730. BCDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.33 BCDMA_RXCRT_CHAN_STATUS1_j Register

1 BCDMA_RXCRT_CHAN_STATUS1_j Register (Offset = 44h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16731. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 0044h + formula

Figure 14-5537. BCDMA_RXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
RX_REQS	RESERVED					FIFO_PEND	FIFO_BUSY
R	NONE					R	R
0h	0h					0h	0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-16733. BCDMA_RXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	FIFO_PEND	R	0h	The FIFO has enough data for a burst Reset Source: rst_mod_g_rst_n
24	FIFO_BUSY	R	0h	The fifo has data Reset Source: rst_mod_g_rst_n
23:8	RESERVED	NONE	0h	Reserved
7	CHANNEL_OK	R	0h	Channel is trying to send data Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Channel has active transactions Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n

Table 14-16733. BCDMA_RXCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.34 BCDMA_RXCRT_CHAN_STDATA_j_k Register

1 BCDMA_RXCRT_CHAN_STDATA_j_k Register (Offset = 80h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 19d, k = 0 to 31d

Table 14-16734. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0080h + formula**

Figure 14-5538. BCDMA_RXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/W							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/W							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/W							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/W							
0h							

Table 14-16736. BCDMA_RXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/W	0h	See BCDMA Mapping Table Reset Source: rst_mod_g_rst_n

14.7.1.2.2.35 BCDMA_RXCRT_CHAN_PEER0_j Register

1 BCDMA_RXCRT_CHAN_PEER0_j Register (Offset = 200h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16737. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0200h + formula**

Figure 14-5539. BCDMA_RXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16739. BCDMA_RXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.36 BCDMA_RXCRT_CHAN_PEER1_j Register

1 BCDMA_RXCRT_CHAN_PEER1_j Register (Offset = 204h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16740. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0204h + formula**

Figure 14-5540. BCDMA_RXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16742. BCDMA_RXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.37 BCDMA_RXCRT_CHAN_PEER2_j Register

1 BCDMA_RXCRT_CHAN_PEER2_j Register (Offset = 208h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16743. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0208h + formula**

Figure 14-5541. BCDMA_RXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16745. BCDMA_RXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.38 BCDMA_RXCRT_CHAN_PEER3_j Register

1 BCDMA_RXCRT_CHAN_PEER3_j Register (Offset = 20Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16746. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 020Ch + formula**

Figure 14-5542. BCDMA_RXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16748. BCDMA_RXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.39 BCDMA_RXCRT_CHAN_PEER4_j Register

1 BCDMA_RXCRT_CHAN_PEER4_j Register (Offset = 210h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16749. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0210h + formula**

Figure 14-5543. BCDMA_RXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16751. BCDMA_RXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.40 BCDMA_RXCRT_CHAN_PEER5_j Register

1 BCDMA_RXCRT_CHAN_PEER5_j Register (Offset = 214h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16752. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0214h + formula**

Figure 14-5544. BCDMA_RXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16754. BCDMA_RXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.41 BCDMA_RXCRT_CHAN_PEER6_j Register

1 BCDMA_RXCRT_CHAN_PEER6_j Register (Offset = 218h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16755. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0218h + formula**

Figure 14-5545. BCDMA_RXCRT_CHAN_PEER6_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16757. BCDMA_RXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.42 BCDMA_RXCRT_CHAN_PEER7_j Register

1 BCDMA_RXCRT_CHAN_PEER7_j Register (Offset = 21Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16758. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 021Ch + formula**

Figure 14-5546. BCDMA_RXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16760. BCDMA_RXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.43 BCDMA_RXCRT_CHAN_PEER8_j Register

1 BCDMA_RXCRT_CHAN_PEER8_j Register (Offset = 220h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16761. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 0220h + formula

Figure 14-5547. BCDMA_RXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16763. BCDMA_RXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.44 BCDMA_RXCRT_CHAN_PEER9_j Register

1 BCDMA_RXCRT_CHAN_PEER9_j Register (Offset = 224h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16764. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0224h + formula**

Figure 14-5548. BCDMA_RXCRT_CHAN_PEER9_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16766. BCDMA_RXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.45 BCDMA_RXCRT_CHAN_PEER10_j Register

1 BCDMA_RXCRT_CHAN_PEER10_j Register (Offset = 228h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16767. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0228h + formula**

Figure 14-5549. BCDMA_RXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16769. BCDMA_RXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.46 BCDMA_RXCRT_CHAN_PEER11_j Register

1 BCDMA_RXCRT_CHAN_PEER11_j Register (Offset = 22Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16770. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 022Ch + formula

Figure 14-5550. BCDMA_RXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16772. BCDMA_RXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.47 BCDMA_RXCRT_CHAN_PEER12_j Register

1 BCDMA_RXCRT_CHAN_PEER12_j Register (Offset = 230h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16773. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0230h + formula**

Figure 14-5551. BCDMA_RXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16775. BCDMA_RXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.48 BCDMA_RXCRT_CHAN_PEER13_j Register

1 BCDMA_RXCRT_CHAN_PEER13_j Register (Offset = 234h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16776. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A82 0234h + formula

Figure 14-5552. BCDMA_RXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16778. BCDMA_RXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.49 BCDMA_RXCRT_CHAN_PEER14_j Register

1 BCDMA_RXCRT_CHAN_PEER14_j Register (Offset = 238h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16779. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0238h + formula**

Figure 14-5553. BCDMA_RXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16781. BCDMA_RXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.50 BCDMA_RXCRT_CHAN_PEER15_j Register

1 BCDMA_RXCRT_CHAN_PEER15_j Register (Offset = 23Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16782. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 023Ch + formula**

Figure 14-5554. BCDMA_RXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16784. BCDMA_RXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.51 BCDMA_RXCRT_CHAN_PCNT_j Register

1 BCDMA_RXCRT_CHAN_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16785. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0400h + formula**

Figure 14-5555. BCDMA_RXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-16787. BCDMA_RXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.52 BCDMA_RXCRT_CHAN_BCNT_j Register

1 BCDMA_RXCRT_CHAN_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16788. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0408h + formula**

Figure 14-5556. BCDMA_RXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-16790. BCDMA_RXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.53 BCDMA_RXCRT_CHAN_SBCNT_j Register

1 BCDMA_RXCRT_CHAN_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16791. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4A82 0410h + formula**

Figure 14-5557. BCDMA_RXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-16793. BCDMA_RXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.54 BCDMA_TXCRT_CHAN_CTL_j Register

1 BCDMA_TXCRT_CHAN_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16794. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0000h + formula**

Figure 14-5558. BCDMA_TXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
TX_ENABLE	TX_TEARDOWN	TX_PAUSE	TX_FORCED_TEARDOWN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TX_ERROR
NONE							R
0h							0h

Table 14-16796. BCDMA_TXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete. Reset Source: rst_mod_g_rst_n
30	TX_TEARDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	TX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n

Table 14-16796. BCDMA_TXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	TX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Uso fo this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:1	RESERVED	NONE	0h	Reserved
0	TX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared by writing back a 0. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.55 BCDMA_TXCRT_CHAN_SWTRIG_j Register

1 BCDMA_TXCRT_CHAN_SWTRIG_j Register (Offset = 8h + formula) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16797. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0008h + formula**

Figure 14-5559. BCDMA_TXCRT_CHAN_SWTRIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
NONE							NA/W
0h							0h

Table 14-16799. BCDMA_TXCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.7.1.2.2.56 BCDMA_TXCRT_CHAN_STATUS0_j Register

1 BCDMA_TXCRT_CHAN_STATUS0_j Register (Offset = 40h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16800. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0040h + formula

Figure 14-5560. BCDMA_TXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
TRING_PEND	TXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	TX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-16802. BCDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	TXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-16802. BCDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.57 BCDMA_TXCRT_CHAN_STATUS1_j Register

1 BCDMA_TXCRT_CHAN_STATUS1_j Register (Offset = 44h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16803. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0044h + formula

Figure 14-5561. BCDMA_TXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
TX_REQS	RESERVED						WAVAIL
R	NONE						R
0h	0h						0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TDNULL
NONE							R
0h							0h
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-16805. BCDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:25	RESERVED	NONE	0h	Reserved
24	WAVAIL	R	0h	The fifo has space for a burst size Reset Source: rst_mod_g_rst_n
23:9	RESERVED	NONE	0h	Reserved
8	TDNULL	R	0h	The channel has met the conditions to do teardown Reset Source: rst_mod_g_rst_n
7	CHANNEL_OK	R	0h	Channel is trying to schedule work Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Channel has outstanding work to do Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n

Table 14-16805. BCDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.58 BCDMA_TXCRT_CHAN_STDATA_j_k Register

1 BCDMA_TXCRT_CHAN_STDATA_j_k Register (Offset = 80h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 19d, k = 0 to 31d

Table 14-16806. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0080h + formula**

Figure 14-5562. BCDMA_TXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/NA							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/NA							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/NA							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/NA							
0h							

Table 14-16808. BCDMA_TXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/NA	0h	See BCDMA Mapping Table Reset Source: rst_mod_g_rst_n

14.7.1.2.2.59 BCDMA_TXCRT_CHAN_PEER0_j Register

1 BCDMA_TXCRT_CHAN_PEER0_j Register (Offset = 200h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16809. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0200h + formula**

Figure 14-5563. BCDMA_TXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16811. BCDMA_TXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.60 BCDMA_TXCRT_CHAN_PEER1_j Register

1 BCDMA_TXCRT_CHAN_PEER1_j Register (Offset = 204h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16812. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0204h + formula**

Figure 14-5564. BCDMA_TXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16814. BCDMA_TXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.61 BCDMA_TXCRT_CHAN_PEER2_j Register

1 BCDMA_TXCRT_CHAN_PEER2_j Register (Offset = 208h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16815. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0208h + formula**

Figure 14-5565. BCDMA_TXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16817. BCDMA_TXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.62 BCDMA_TXCRT_CHAN_PEER3_j Register

1 BCDMA_TXCRT_CHAN_PEER3_j Register (Offset = 20Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16818. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 020Ch + formula**

Figure 14-5566. BCDMA_TXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16820. BCDMA_TXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.63 BCDMA_TXCRT_CHAN_PEER4_j Register

1 BCDMA_TXCRT_CHAN_PEER4_j Register (Offset = 210h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16821. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0210h + formula**

Figure 14-5567. BCDMA_TXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16823. BCDMA_TXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.64 BCDMA_TXCRT_CHAN_PEER5_j Register

1 BCDMA_TXCRT_CHAN_PEER5_j Register (Offset = 214h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16824. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0214h + formula**

Figure 14-5568. BCDMA_TXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16826. BCDMA_TXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.65 BCDMA_TXCRT_CHAN_PEER6_j Register

1 BCDMA_TXCRT_CHAN_PEER6_j Register (Offset = 218h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16827. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0218h + formula**

Figure 14-5569. BCDMA_TXCRT_CHAN_PEER6_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16829. BCDMA_TXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.66 BCDMA_TXCRT_CHAN_PEER7_j Register

1 BCDMA_TXCRT_CHAN_PEER7_j Register (Offset = 21Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16830. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 021Ch + formula**

Figure 14-5570. BCDMA_TXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16832. BCDMA_TXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.67 BCDMA_TXCRT_CHAN_PEER8_j Register

1 BCDMA_TXCRT_CHAN_PEER8_j Register (Offset = 220h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16833. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0220h + formula**

Figure 14-5571. BCDMA_TXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16835. BCDMA_TXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.68 BCDMA_TXCRT_CHAN_PEER9_j Register

1 BCDMA_TXCRT_CHAN_PEER9_j Register (Offset = 224h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16836. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0224h + formula**

Figure 14-5572. BCDMA_TXCRT_CHAN_PEER9_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16838. BCDMA_TXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.69 BCDMA_TXCRT_CHAN_PEER10_j Register

1 BCDMA_TXCRT_CHAN_PEER10_j Register (Offset = 228h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16839. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0228h + formula**

Figure 14-5573. BCDMA_TXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16841. BCDMA_TXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.70 BCDMA_TXCRT_CHAN_PEER11_j Register

1 BCDMA_TXCRT_CHAN_PEER11_j Register (Offset = 22Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16842. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 022Ch + formula**

Figure 14-5574. BCDMA_TXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16844. BCDMA_TXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.71 BCDMA_TXCRT_CHAN_PEER12_j Register

1 BCDMA_TXCRT_CHAN_PEER12_j Register (Offset = 230h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16845. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0230h + formula**

Figure 14-5575. BCDMA_TXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16847. BCDMA_TXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.72 BCDMA_TXCRT_CHAN_PEER13_j Register

1 BCDMA_TXCRT_CHAN_PEER13_j Register (Offset = 234h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16848. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0234h + formula**

Figure 14-5576. BCDMA_TXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16850. BCDMA_TXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.73 BCDMA_TXCRT_CHAN_PEER14_j Register

1 BCDMA_TXCRT_CHAN_PEER14_j Register (Offset = 238h + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16851. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0238h + formula**

Figure 14-5577. BCDMA_TXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16853. BCDMA_TXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.74 BCDMA_TXCRT_CHAN_PEER15_j Register

1 BCDMA_TXCRT_CHAN_PEER15_j Register (Offset = 23Ch + formula) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16854. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 023Ch + formula**

Figure 14-5578. BCDMA_TXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-16856. BCDMA_TXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.75 BCDMA_TXCRT_CHAN_PCNT_j Register

1 BCDMA_TXCRT_CHAN_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16857. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4AA4 0400h + formula**

Figure 14-5579. BCDMA_TXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-16859. BCDMA_TXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.76 BCDMA_TXCRT_CHAN_BCNT_j Register

1 BCDMA_TXCRT_CHAN_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16860. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0408h + formula

Figure 14-5580. BCDMA_TXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-16862. BCDMA_TXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.77 BCDMA_TXCRT_CHAN_SBCNT_j Register

1 BCDMA_TXCRT_CHAN_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 19d

Table 14-16863. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0410h + formula

Figure 14-5581. BCDMA_TXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-16865. BCDMA_TXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.78 LCDMA_RINGACC_RINGRT_RING_FDB_j Register

1 LCDMA_RINGACC_RINGRT_RING_FDB_j Register (Offset = 10h + formula) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Offset = (j * 2000h); where j = 0 to 67d

Table 14-16866. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4BC0 0010h + formula**

Figure 14-5582. LCDMA_RINGACC_RINGRT_RING_FDB_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-16868. LCDMA_RINGACC_RINGRT_RING_FDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.79 LCDMA_RINGACC_RINGRT_RING_FOCC_j Register

1 LCDMA_RINGACC_RINGRT_RING_FOCC_j Register (Offset = 18h + formula) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = (j * 2000h); where j = 0 to 67d

Table 14-16869. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4BC0 0018h + formula**

Figure 14-5583. LCDMA_RINGACC_RINGRT_RING_FOCC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							OCC
NONE							R/NA
0h							0h
15	14	13	12	11	10	9	8
OCC							
R/NA							
0h							
7	6	5	4	3	2	1	0
OCC							
R/NA							
0h							

Table 14-16871. LCDMA_RINGACC_RINGRT_RING_FOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.80 LCDMA_RINGACC_RINGRT_RING_RDB_j Register

1 LCDMA_RINGACC_RINGRT_RING_RDB_j Register (Offset = 1010h + formula) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Offset = (j * 2000h); where j = 0 to 67d

Table 14-16872. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4BC0 1010h + formula

Figure 14-5584. LCDMA_RINGACC_RINGRT_RING_RDB_j Name Register

31	30	29	28	27	26	25	24
TDOWN_ACK	RESERVED						
NA/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-16874. LCDMA_RINGACC_RINGRT_RING_RDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_ACK	NA/W	0h	This bit is set to 1 to ackowledge (and clear) the tdown_complete bit in the corresponding Ring N Occupancy Register. this bit is only valid on the reverse rings (rings consumed by the Host SW) Reset Source: rst_mod_g_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.7.1.2.2.81 LCDMA_RINGACC_RINGRT_RING_ROCC_j Register

1 LCDMA_RINGACC_RINGRT_RING_ROCC_j Register (Offset = 1018h + formula) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = (j * 2000h); where j = 0 to 67d

Table 14-16875. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4BC0 1018h + formula**

Figure 14-5585. LCDMA_RINGACC_RINGRT_RING_ROCC_j Name Register

31	30	29	28	27	26	25	24
TDOWN_COMPLETE	RESERVED						
R/NA	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OCC
NONE							R/NA
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OCC							
R/NA							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OCC							
R/NA							
0h							

Table 14-16877. LCDMA_RINGACC_RINGRT_RING_ROCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_COMPLETE	R/NA	0h	This bit when set indicates that a teardown is complete on the channel. This bit is cleared anytime the tdown_ack bit is written as a 1 in the corresponding Ring N Doorbell Register. This bit is only valid on the reverse rings (rings consumed by the Host SW). Reset Source: rst_mod_g_rst_n
30:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.82 BCDMA_BCRT_CHAN_CTL_j Register

1 BCDMA_BCRT_CHAN_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16878. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0000h + formula**

Figure 14-5586. BCDMA_BCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
TX_ENABLE	TX_TEARDOWN	TX_PAUSE	TX_FORCED_TEARDOWN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TX_ERROR
NONE							R
0h							0h

Table 14-16880. BCDMA_BCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete. Reset Source: rst_mod_g_rst_n
30	TX_TEARDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	TX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n

Table 14-16880. BCDMA_BCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	TX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Uso fo this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:1	RESERVED	NONE	0h	Reserved
0	TX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared by writing back a 0. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.83 BCDMA_BCRT_CHAN_SWTRIG_j Register

1 BCDMA_BCRT_CHAN_SWTRIG_j Register (Offset = 8h + formula) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16881. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0008h + formula**

Figure 14-5587. BCDMA_BCRT_CHAN_SWTRIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
NONE							NA/W
0h							0h

Table 14-16883. BCDMA_BCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.7.1.2.2.84 BCDMA_BCRT_CHAN_STATUS0_j Register

1 BCDMA_BCRT_CHAN_STATUS0_j Register (Offset = 40h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16884. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0040h + formula**

Figure 14-5588. BCDMA_BCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
TRING_PEND	TXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	TX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-16886. BCDMA_BCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	TXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-16886. BCDMA_BCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.85 BCDMA_BCRT_CHAN_STATUS1_j Register

1 BCDMA_BCRT_CHAN_STATUS1_j Register (Offset = 44h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16887. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0044h + formula**

Figure 14-5589. BCDMA_BCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
TX_REQS	RESERVED						WAVAIL
R	NONE						R
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TDNULL
NONE							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-16889. BCDMA_BCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:25	RESERVED	NONE	0h	Reserved
24	WAVAIL	R	0h	The fifo has space for a burst size Reset Source: rst_mod_g_rst_n
23:9	RESERVED	NONE	0h	Reserved
8	TDNULL	R	0h	Channel is trying to teardown and has met conditions Reset Source: rst_mod_g_rst_n
7	CHANNEL_OK	R	0h	Channel is trying to schedule a transaction Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	The channel is active Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n

Table 14-16889. BCDMA_BCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.86 BCDMA_BCRT_CHAN_STATUS2_j Register

1 BCDMA_BCRT_CHAN_STATUS2_j Register (Offset = 48h + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16890. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0048h + formula

Figure 14-5590. BCDMA_BCRT_CHAN_STATUS2_j Name Register

31	30	29	28	27	26	25	24
RRING_PEND	RXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	RX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-16892. BCDMA_BCRT_CHAN_STATUS2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	RXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n

Table 14-16892. BCDMA_BCRT_CHAN_STATUS2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.87 BCDMA_BCRT_CHAN_STATUS3_j Register

1 BCDMA_BCRT_CHAN_STATUS3_j Register (Offset = 4Ch + formula) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16893. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 004Ch + formula**

Figure 14-5591. BCDMA_BCRT_CHAN_STATUS3_j Name Register

31	30	29	28	27	26	25	24
RX_REQS	RESERVED					FIFO_PEND	FIFO_BUSY
R	NONE					R	R
0h	0h					0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-16895. BCDMA_BCRT_CHAN_STATUS3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	FIFO_PEND	R	0h	The FIFO has enough data for a burst Reset Source: rst_mod_g_rst_n
24	FIFO_BUSY	R	0h	The fifo has data Reset Source: rst_mod_g_rst_n
23:8	RESERVED	NONE	0h	Reserved
7	CHANNEL_OK	R	0h	Reserved Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Reserved Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	Reserved Reset Source: rst_mod_g_rst_n

Table 14-16895. BCDMA_BCRT_CHAN_STATUS3_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.7.1.2.2.88 BCDMA_BCRT_CHAN_STDATA_j_k Register

1 BCDMA_BCRT_CHAN_STDATA_j_k Register (Offset = 80h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 27d, k = 0 to 31d

Table 14-16896. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0080h + formula**

Figure 14-5592. BCDMA_BCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/NA							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/NA							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/NA							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/NA							
0h							

Table 14-16898. BCDMA_BCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/NA	0h	See BCDMA Mapping Table Reset Source: rst_mod_g_rst_n

14.7.1.2.2.89 BCDMA_BCRT_CHAN_STDATAW_j_k Register

1 BCDMA_BCRT_CHAN_STDATAW_j_k Register (Offset = 100h + formula) [reset = 0h]

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 27d, k = 0 to 31d

Table 14-16899. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0100h + formula**

Figure 14-5593. BCDMA_BCRT_CHAN_STDATAW_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/W							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/W							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/W							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/W							
0h							

Table 14-16901. BCDMA_BCRT_CHAN_STDATAW_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/W	0h	See BCDMA Mapping Table Reset Source: rst_mod_g_rst_n

14.7.1.2.2.90 BCDMA_BCRT_CHAN_PCNT_j Register

1 BCDMA_BCRT_CHAN_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16902. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0400h + formula**

Figure 14-5594. BCDMA_BCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-16904. BCDMA_BCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.91 BCDMA_BCRT_CHAN_BCNT_j Register

1 BCDMA_BCRT_CHAN_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16905. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0408h + formula**

Figure 14-5595. BCDMA_BCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-16907. BCDMA_BCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.1.2.2.92 BCDMA_BCRT_CHAN_SBCNT_j Register

1 BCDMA_BCRT_CHAN_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 27d

Table 14-16908. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	**4C00 0410h + formula**

Figure 14-5596. BCDMA_BCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-16910. BCDMA_BCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.7.2 RINGACC Registers

14.7.2.1 DMASS_RINGACC_0

DMASS_RINGACC_0

14.7.2.1.1 DMASS_RINGACC_0 Summaries

DMASS_RINGACC_0 Summaries

Table 14-16911. RINGACC_ISC Registers, Base Address=4584 8000h, Length=1024

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
0h	32	RINGACC_ISC_EP_CONTROL_J	4584 8000h + formula
4h	32	RINGACC_ISC_EP_CONTROL2_J	4584 8004h + formula

Table 14-16912. RINGACC_GCFG Registers, Base Address=4824 0000h, Length=1024

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
0h	32	RINGACC_GCFG_REVISION	4824 0000h
10h	32	RINGACC_GCFG_TRACE_CTL	4824 0010h
20h	32	RINGACC_GCFG_OVRFLOW	4824 0020h
40h	32	RINGACC_GCFG_ERROR_EVT	4824 0040h
44h	32	RINGACC_GCFG_ERROR_LOG	4824 0044h

Table 14-16913. RINGACC_RT Registers, Base Address=4900 0000h, Length=4194304

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
10h	32	RINGACC_RT_RINGRT_DB_J	4900 0010h + formula
18h	32	RINGACC_RT_RINGRT_OCC_J	4900 0018h + formula
1Ch	32	RINGACC_RT_RINGRT_INDX_J	4900 001Ch + formula
20h	32	RINGACC_RT_RINGRT_HWOCC_J	4900 0020h + formula
24h	32	RINGACC_RT_RINGRT_HWINDX_J	4900 0024h + formula

Table 14-16914. RINGACC_CFG Registers, Base Address=4980 0000h, Length=262144

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
40h	32	RINGACC_CFG_RING_BA_LO_J	4980 0040h + formula
44h	32	RINGACC_CFG_RING_BA_HI_J	4980 0044h + formula
48h	32	RINGACC_CFG_RING_SIZE_J	4980 0048h + formula
4Ch	32	RINGACC_CFG_RING_EVENT_J	4980 004Ch + formula
50h	32	RINGACC_CFG_RING_ORDERID_J	4980 0050h + formula

Table 14-16915. RINGACC_FIFOS Registers, Base Address=4E00 0000h, Length=4194304

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
0h	32	RINGACC_FIFOS_FIFO_RINGHEADDATA_J_K	4E00 0000h + formula
200h	32	RINGACC_FIFOS_FIFO_RINGTAILDATA_J_K	4E00 0200h + formula
400h	32	RINGACC_FIFOS_FIFO_PEEKHEADDATA_J_K	4E00 0400h + formula
600h	32	RINGACC_FIFOS_FIFO_PEEKTAILDATA_J_K	4E00 0600h + formula

14.7.2.1.2 DMASS_RINGACC_0 Registers

DMASS_RINGACC_0 Registers

14.7.2.1.2.1 RINGACC_ISC_EP_CONTROL_j Register

1 RINGACC_ISC_EP_CONTROL_j Register (Offset = 0h + formula) [reset = 0h]

The ISC a Region b Control Register defines the control fields for the ISC.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 31d

Table 14-16916. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4584 8000h + formula**

Figure 14-5597. RINGACC_ISC_EP_CONTROL_j Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-16918. RINGACC_ISC_EP_CONTROL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Has precedence over priv set bits. Reset Source: srst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: srst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: srst_n
20	NONSEC	R/W	0h	Make outgoing non-secure. Has precedence over secure enable bits. Reset Source: srst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: srst_n
15:8	PRIV_ID	R/W	X	Priv ID. Reset Source: srst_n
7:5	RESERVED	NONE	0h	Reserved

Table 14-16918. RINGACC_ISC_EP_CONTROL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: srst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: srst_n

14.7.2.1.2.2 RINGACC_ISC_EP_CONTROL2_j Register

1 RINGACC_ISC_EP_CONTROL2_j Register (Offset = 4h + formula) [reset = 0h]

The ISC a Region b Control Register 2 defines the control fields for the ISC.

Return to Summary Table

Offset = (j * 20h); where j = 0 to 31d

Table 14-16919. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4584 8004h + formula

Figure 14-5598. RINGACC_ISC_EP_CONTROL2_j Name Register

31	30	29	28	27	26	25	24
PASS_V	RESERVED	ATYPE		VIRTID			
R/W	NONE	R/W		R/W			
0h	0h	0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VIRTID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-16921. RINGACC_ISC_EP_CONTROL2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PASS_V	R/W	0h	No virtID replacement, pass through value. Reset Source: srst_n
30	RESERVED	NONE	0h	Reserved
29:28	ATYPE	R/W	0h	Defines the output address type. 0 = physical no memory attributes. 1 = intermediate. 2 = virtual. 3 = physical with memory attributes. Reset Source: srst_n
27:16	VIRTID	R/W	0h	Virt ID. Reset Source: srst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.2.1.2.3 RINGACC_GCFG_REVISION Register

1 RINGACC_GCFG_REVISION Register (Offset = 0h) [reset = 663C0101h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-16922. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0000h**

Figure 14-5599. RINGACC_GCFG_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
663Ch							
23	22	21	20	19	18	17	16
MODID							
R							
663Ch							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
0h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-16924. RINGACC_GCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	663Ch	Module ID field Reset Source: srst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: srst_n

14.7.2.1.2.4 RINGACC_GCFG_TRACE_CTL Register

1 RINGACC_GCFG_TRACE_CTL Register (Offset = 10h) [reset = 0h]

Trace Control Register

Return to Summary Table

Table 14-16925. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0010h**

Figure 14-5600. RINGACC_GCFG_TRACE_CTL Name Register

31	30	29	28	27	26	25	24
EN	ALL_QUEUES	MSG	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE							
R/W							
0h							

Table 14-16927. RINGACC_GCFG_TRACE_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Trace enable 0 = disable 1 = enable. Reset Source: srst_n
30	ALL_QUEUES	R/W	0h	Trace everything 0 = only the selected queue 1 = every queue. Reset Source: srst_n
29	MSG	R/W	0h	Trace message data 0 = include only the operation 1 = include message data. Reset Source: srst_n
28:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R/W	0h	Queue number when tracing a single queue. Reset Source: srst_n

14.7.2.1.2.5 RINGACC_GCFG_OVRFLOW Register

1 RINGACC_GCFG_OVRFLOW Register (Offset = 20h) [reset = 0h]

Overflow Queue Register

Return to Summary Table

Table 14-16928. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0020h**

Figure 14-5601. RINGACC_GCFG_OVRFLOW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE							
R/W							
0h							

Table 14-16930. RINGACC_GCFG_OVRFLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R/W	0h	Queue to send overflow messages. A value of 0xffff will disable the overflow function. Reset Source: srst_n

14.7.2.1.2.6 RINGACC_GCFG_ERROR_EVT Register

1 RINGACC_GCFG_ERROR_EVT Register (Offset = 40h) [reset = FFFFh]

The Error Event Register is an Output Event Steering 'OES' register that specifies the event number used to denote detection of a ring memory transaction bus error.

Return to Summary Table

Table 14-16931. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0040h**

Figure 14-5602. RINGACC_GCFG_ERROR_EVT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EVT							
R/W							
FFFFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVT							
R/W							
FFFFh							

Table 14-16933. RINGACC_GCFG_ERROR_EVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	Event to send when detecting a bus error. Reset Source: srst_n

14.7.2.1.2.7 RINGACC_GCFG_ERROR_LOG Register

1 RINGACC_GCFG_ERROR_LOG Register (Offset = 44h) [reset = 0h]

Error Log Register. A read of this register will clear the pending error log event and allow a new error to be captured. It does not clear the contents of this register which are only valid while the error event is pending.

Return to Summary Table

Table 14-16934. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4824 0044h**

Figure 14-5603. RINGACC_GCFG_ERROR_LOG Name Register

31	30	29	28	27	26	25	24
PUSH	RESERVED						
R	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
QUEUE							
R							
0h							

7	6	5	4	3	2	1	0
QUEUE							
R							
0h							

Table 14-16936. RINGACC_GCFG_ERROR_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PUSH	R	0h	Bus error was caused by a push. 0 = pop. 1 = push. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R	0h	Queue that received the bus error. Reset Source: srst_n

14.7.2.1.2.8 RINGACC_RT_RINGRT_DB_j Register

1 RINGACC_RT_RINGRT_DB_j Register (Offset = 10h + formula) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 31d

Table 14-16937. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4900 0010h + formula**

Figure 14-5604. RINGACC_RT_RINGRT_DB_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-16939. RINGACC_RT_RINGRT_DB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: srst_n

14.7.2.1.2.9 RINGACC_RT_RINGRT_OCC_j Register

1 RINGACC_RT_RINGRT_OCC_j Register (Offset = 18h + formula) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 31d

Table 14-16940. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4900 0018h + formula**

Figure 14-5605. RINGACC_RT_RINGRT_OCC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			OCC				
NONE			R/NA				
0h			0h				
15	14	13	12	11	10	9	8
OCC							
R/NA							
0h							
7	6	5	4	3	2	1	0
OCC							
R/NA							
0h							

Table 14-16942. RINGACC_RT_RINGRT_OCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: srst_n

14.7.2.1.2.10 RINGACC_RT_RINGRT_INDX_j Register

1 RINGACC_RT_RINGRT_INDX_j Register (Offset = 1Ch + formula) [reset = 0h]

The Ring N Current Index Register can be read by software for debug purposes to determine the current SW read index for the Ring for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 31d

Table 14-16943. Instance Table

Instance Name	**Physical Address**
DMASS0_RINGACC_0	**4900 001Ch + formula**

Figure 14-5606. RINGACC_RT_RINGRT_INDX_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">INDX</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/NA</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">INDX</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INDX</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16945. RINGACC_RT_RINGRT_INDX_j Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:20	RESERVED	NONE	0h	Reserved
19:0	INDX	R/NA	0h	Current SW owned read index for the ring. This value is initialized to 0 when the ring is set up and will be incremented by SW each time SW processes a ring entry. When the index is incremented to a value equal to the size field in the Ring Size Register for the ring the index will be reset back to 0. Reset Source: srst_n

14.7.2.1.2.11 RINGACC_RT_RINGRT_HWOCC_j Register

1 RINGACC_RT_RINGRT_HWOCC_j Register (Offset = 20h + formula) [reset = 0h]

The Ring N Hardware Occupancy Register contains the early increment/decrement version of the the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 31d

Table 14-16946. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4900 0020h + formula**

Figure 14-5607. RINGACC_RT_RINGRT_HWOCC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			OCC				
NONE			R/NA				
0h			0h				
15	14	13	12	11	10	9	8
OCC							
R/NA							
0h							
7	6	5	4	3	2	1	0
OCC							
R/NA							
0h							

Table 14-16948. RINGACC_RT_RINGRT_HWOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: srst_n

14.7.2.1.2.12 RINGACC_RT_RINGRT_HWINDX_j Register

1 RINGACC_RT_RINGRT_HWINDX_j Register (Offset = 24h + formula) [reset = 0h]

The Ring N Current Index Register can be read by software for debug purposes to determine the current HW read index for the Ring for the channel.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 31d

Table 14-16949. Instance Table

Instance Name	**Physical Address**
DMASS0_RINGACC_0	**4900 0024h + formula**

Figure 14-5608. RINGACC_RT_RINGRT_HWINDX_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">INDX</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/NA</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">INDX</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INDX</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16951. RINGACC_RT_RINGRT_HWINDX_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INDX	R/NA	0h	Current HW owned read index for the ring. This value is initialized to 0 when the ring is set up and will be incremented by HW each time HW processes a ring entry. When the index is incremented to a value equal to the size field in the Ring Size Register for the ring the index will be reset back to 0. Reset Source: srst_n

14.7.2.1.2.13 RINGACC_CFG_RING_BA_LO_j Register

1 RINGACC_CFG_RING_BA_LO_j Register (Offset = 40h + formula) [reset = 0h]

The Tx Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to the element size of the ring, or to double the element size of the ring if the qmode is CREDENTIALS or QM modes. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 31d

Table 14-16952. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 0040h + formula**

Figure 14-5609. RINGACC_CFG_RING_BA_LO_j Name Register

31	30	29	28	27	26	25	24
ADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_LO							
R/W							
0h							

Table 14-16954. RINGACC_CFG_RING_BA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_LO	R/W	0h	Tx Ring base address (LSBs) Reset Source: srst_n

14.7.2.1.2.14 RINGACC_CFG_RING_BA_HI_j Register

1 RINGACC_CFG_RING_BA_HI_j Register (Offset = 44h + formula) [reset = 0h]

The Tx Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to the element size of the ring, or to double the element size of the ring if the qmode is CREDENTIALS or QM modes. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 31d

Table 14-16955. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 0044h + formula**

Figure 14-5610. RINGACC_CFG_RING_BA_HI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_HI							
R/W							
0h							

Table 14-16957. RINGACC_CFG_RING_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_HI	R/W	0h	Tx Ring base address (MSBs) Reset Source: srst_n

14.7.2.1.2.15 RINGACC_CFG_RING_SIZE_j Register

1 RINGACC_CFG_RING_SIZE_j Register (Offset = 48h + formula) [reset = 0h]

The Tx Ring Size Register contains the element size and element counts for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 31d

Table 14-16958. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 0048h + formula**

Figure 14-5611. RINGACC_CFG_RING_SIZE_j Name Register

31	30	29	28	27	26	25	24
QMODE		RESERVED			ELSIZE		
R/W		NONE			R/W		
0h		0h			0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				SIZE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SIZE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE							
R/W							
0h							

Table 14-16960. RINGACC_CFG_RING_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	QMODE	R/W	0h	Defines the mode for this ring or queue. Reset Source: srst_n 0 exposed ring mode for SW direct access 1 messaging mode when all operations are through bus accesses, allowing multiple producers or consumers. 2 credentials mode is message mode plus stores credentials with each message, requiring the ring size to be doubled to fit the credentials along with the same number of elements when using the first 2 modes. Any exposed memory should be protected by a firewall from unwanted access.
29:27	RESERVED	NONE	0h	Reserved
26:24	ELSIZE	R/W	0h	Ring element size. This field is encoded as follows: 0 = 4 bytes 1 = 8 bytes 2 = 16 bytes 3 = 32 bytes 4 = 64 bytes 5 = 128 bytes 6 = 256 bytes 7 = RESERVED Reset Source: srst_n
23:20	RESERVED	NONE	0h	Reserved

Table 14-16960. RINGACC_CFG_RING_SIZE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	SIZE	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. For rings in CREDENTIALS or QM modes the size must be an even number. Reset Source: srst_n

14.7.2.1.2.16 RINGACC_CFG_RING_EVENT_j Register

1 RINGACC_CFG_RING_EVENT_j Register (Offset = 4Ch + formula) [reset = FFFFh]

The Ring Event Register is an Output Event Steering 'OES' register that specifies the event number used to denote the occurrence of an up event [empty to not-empty] or a down event [non-empty to empty] for this ring.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 31d

Table 14-16961. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4980 004Ch + formula**

Figure 14-5612. RINGACC_CFG_RING_EVENT_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-16963. RINGACC_CFG_RING_EVENT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	Defines the event for this ring or queue. Reset Source: srst_n

14.7.2.1.2.17 RINGACC_CFG_RING_ORDERID_j Register

1 RINGACC_CFG_RING_ORDERID_j Register (Offset = 50h + formula) [reset = 0h]

The Ring OrderID Register contains the bus orderid value for the ring memory access.

Return to Summary Table

Offset = (j * 100h); where j = 0 to 31d

Table 14-16964. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4980 0050h + formula

Figure 14-5613. RINGACC_CFG_RING_ORDERID_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>REPLACE</td><td colspan="4">ORDERID</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-16966. RINGACC_CFG_RING_ORDERID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REPLACE	R/W	0h	Indicates to replace the bus orderid value for this ring or queue with the orderid MMR field. This allows control over the orderid value when it must be restricted due to the topology for QoS reasons. 0 = bypass and use the orderid from the source transaction for the destination transaction. 1 = use the orderid MMR field value for the destination transaction. Reset Source: srst_n
3:0	ORDERID	R/W	0h	Defines the bus orderid value for this ring or queue. Reset Source: srst_n

14.7.2.1.2.18 RINGACC_FIFOS_FIFO_RINGHEADDATA_j_k Register

1 RINGACC_FIFOS_FIFO_RINGHEADDATA_j_k Register (Offset = 0h + formula) [reset = 0h]

The Ring Head Entry Data Registers contain the data which is to be written or which was read from the ring head. These registers are virtual and non-static (i.e. they are just address locations that are used to access the ring head element for reads or writes. The data is right justified.)

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 31d, k = 0 to 127d

Table 14-16967. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4E00 0000h + formula**

Figure 14-5614. RINGACC_FIFOS_FIFO_RINGHEADDATA_j_k Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-16969. RINGACC_FIFOS_FIFO_RINGHEADDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Block of ring head or tail element data Reset Source: srst_n

14.7.2.1.2.19 RINGACC_FIFOS_FIFO_RINGTAILDATA_j_k Register

1 RINGACC_FIFOS_FIFO_RINGTAILDATA_j_k Register (Offset = 200h + formula) [reset = 0h]

The Ring Tail Entry Data Registers contain the data which is to be written or which was read from the ring tail. These registers are virtual and non-static (i.e. they are just address locations that are used to access the ring tail element for reads or writes. The data is right justified.)

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 31d, k = 0 to 127d

Table 14-16970. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4E00 0200h + formula**

Figure 14-5615. RINGACC_FIFOS_FIFO_RINGTAILDATA_j_k Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-16972. RINGACC_FIFOS_FIFO_RINGTAILDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Block of ring head or tail element data Reset Source: srst_n

14.7.2.1.2.20 RINGACC_FIFOS_FIFO_PEEKHEADDATA_j_k Register

1 RINGACC_FIFOS_FIFO_PEEKHEADDATA_j_k Register (Offset = 400h + formula) [reset = 0h]

The Ring Peek Head Entry Data Registers contain the data which is to be read from the ring head without removing the element. These registers are virtual and non-static (i.e. they are just address locations that are used to access the ring head element for reads. Writes are ignored. The data is right justified.)

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 31d, k = 0 to 127d

Table 14-16973. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4E00 0400h + formula**

Figure 14-5616. RINGACC_FIFOS_FIFO_PEEKHEADDATA_j_k Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-16975. RINGACC_FIFOS_FIFO_PEEKHEADDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Block of ring head or tail element data. Reserved for rings in ring mode. Reset Source: srst_n

14.7.2.1.2.21 RINGACC_FIFOS_FIFO_PEEKTAILDATA_j_k Register

1 RINGACC_FIFOS_FIFO_PEEKTAILDATA_j_k Register (Offset = 600h + formula) [reset = 0h]

The Ring Peek Tail Entry Data Registers contain the data which is to be read from the ring tail without removing the element. These registers are virtual and non-static (i.e. they are just address locations that are used to access the ring tail element for reads. Writes are ignored. The data is right justified.)

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 31d, k = 0 to 127d

Table 14-16976. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	**4E00 0600h + formula**

Figure 14-5617. RINGACC_FIFOS_FIFO_PEEKTAILDATA_j_k Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-16978. RINGACC_FIFOS_FIFO_PEEKTAILDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Block of ring head or tail element data. Reserved for rings in ring mode. Reset Source: srst_n

14.7.3 Secure Proxy Registers

14.7.3.1 DMASS_SEC_PROXY_0

DMASS_SEC_PROXY_0

14.7.3.1.1 DMASS_SEC_PROXY_0 Summaries

DMASS_SEC_PROXY_0 Summaries

Table 14-16979. SEC_PROXY Registers, Base Address=4825 0000h, Length=256

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_PID	4825 0000h
4h	32	SEC_PROXY_CONFIG	4825 0004h
14h	32	SEC_PROXY_GLB_EVT	4825 0014h

Table 14-16980. SEC_PROXY_SCFG Registers, Base Address=4A40 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_SCFG_BUFFER_L	4A40 0000h
4h	32	SEC_PROXY_SCFG_BUFFER_H	4A40 0004h
8h	32	SEC_PROXY_SCFG_TARGET_L	4A40 0008h
Ch	32	SEC_PROXY_SCFG_TARGET_H	4A40 000Ch
10h	32	SEC_PROXY_SCFG_ORDERID	4A40 0010h
0h	32	SEC_PROXY_SCFG_THREAD_CTL_J	4A40 0000h + formula
4h	32	SEC_PROXY_SCFG_THREAD_EVT_MAP_J	4A40 0004h + formula
8h	32	SEC_PROXY_SCFG_THREAD_DST_J	4A40 0008h + formula

Table 14-16981. SEC_PROXY_RT Registers, Base Address=4A60 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_RT_THREAD_STATUS_J	4A60 0000h + formula
4h	32	SEC_PROXY_RT_THREAD_THR_J	4A60 0004h + formula

Table 14-16982. PROXY_TARGET Registers, Base Address=4D00 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	PROXY_TARGET_THREAD_DATA_J	4D00 0000h + formula
4h	32	PROXY_TARGET_THREAD_MESSAGE_J_K	4D00 0004h + formula

14.7.3.1.2 DMASS_SEC_PROXY_0 Registers

DMASS_SEC_PROXY_0 Registers

14.7.3.1.2.1 SEC_PROXY_PID Register

1 SEC_PROXY_PID Register (Offset = 0h) [reset = 66367100h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-16983. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4825 0000h**

Figure 14-5618. SEC_PROXY_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		636h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
636h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Eh					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-16985. SEC_PROXY_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	636h	Module ID Reset Source: rst_mod_g_rst_n
15:11	RTL	R	Eh	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: rst_mod_g_rst_n

14.7.3.1.2.2 SEC_PROXY_CONFIG Register

1 SEC_PROXY_CONFIG Register (Offset = 4h) [reset = 40004Ch]

The Config Register shows configured params.

Return to Summary Table

Table 14-16986. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4825 0004h**

Figure 14-5619. SEC_PROXY_CONFIG Name Register

31	30	29	28	27	26	25	24
MSG_SIZE							
R							
40h							
23	22	21	20	19	18	17	16
MSG_SIZE							
R							
40h							
15	14	13	12	11	10	9	8
THREADS							
R							
4Ch							
7	6	5	4	3	2	1	0
THREADS							
R							
4Ch							

Table 14-16988. SEC_PROXY_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MSG_SIZE	R	40h	Supported message size in bytes. Reset Source: rst_mod_g_rst_n
15:0	THREADS	R	4Ch	Number of proxy threads supported. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.3 SEC_PROXY_GLB_EVT Register

1 SEC_PROXY_GLB_EVT Register (Offset = 14h) [reset = FFFFh]

The Global Event Register defines the event to send for a global error.

Return to Summary Table

Table 14-16989. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4825 0014h**

Figure 14-5620. SEC_PROXY_GLB_EVT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ERR_EVENT							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
ERR_EVENT							
R/W							
FFFFh							

Table 14-16991. SEC_PROXY_GLB_EVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ERR_EVENT	R/W	FFFFh	Global error event destination. 0xFFFF disables the event Reset Source: rst_mod_g_rst_n

14.7.3.1.2.4 SEC_PROXY_SCFG_BUFFER_L Register

1 SEC_PROXY_SCFG_BUFFER_L Register (Offset = 0h) [reset = 0h]

The Buffer Register defines the pointer for the external buffer.

Return to Summary Table

Table 14-16992. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0000h**

Figure 14-5621. SEC_PROXY_SCFG_BUFFER_L Name Register

31	30	29	28	27	26	25	24
BASE_L							
R/W							
0h							
23	22	21	20	19	18	17	16
BASE_L							
R/W							
0h							
15	14	13	12	11	10	9	8
BASE_L							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE_L							
R/W							
0h							

Table 14-16994. SEC_PROXY_SCFG_BUFFER_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE_L	R/W	0h	The base address for the external buffer, lower 32 bits. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.5 SEC_PROXY_SCFG_BUFFER_H Register

1 SEC_PROXY_SCFG_BUFFER_H Register (Offset = 4h) [reset = 0h]

The Buffer Register defines the pointer for the external buffer.

Return to Summary Table

Table 14-16995. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0004h**

Figure 14-5622. SEC_PROXY_SCFG_BUFFER_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
BASE_H							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE_H							
R/W							
0h							

Table 14-16997. SEC_PROXY_SCFG_BUFFER_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BASE_H	R/W	0h	The base address for the external buffer, upper 16 bits. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.6 SEC_PROXY_SCFG_TARGET_L Register

1 SEC_PROXY_SCFG_TARGET_L Register (Offset = 8h) [reset = 4E000000h]

The Target Register defines the pointer for the external target.

Return to Summary Table

Table 14-16998. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0008h**

Figure 14-5623. SEC_PROXY_SCFG_TARGET_L Name Register

31	30	29	28	27	26	25	24
BASE_L							
R/W							
4E000000h							
23	22	21	20	19	18	17	16
BASE_L							
R/W							
4E000000h							
15	14	13	12	11	10	9	8
BASE_L							
R/W							
4E000000h							
7	6	5	4	3	2	1	0
BASE_L							
R/W							
4E000000h							

Table 14-17000. SEC_PROXY_SCFG_TARGET_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE_L	R/W	4E000000h	The base address for the external target, lower 32 bits. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.7 SEC_PROXY_SCFG_TARGET_H Register

1 SEC_PROXY_SCFG_TARGET_H Register (Offset = Ch) [reset = 0h]

The Target Register defines the pointer for the external target.

Return to Summary Table

Table 14-17001. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 000Ch**

Figure 14-5624. SEC_PROXY_SCFG_TARGET_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BASE_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BASE_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17003. SEC_PROXY_SCFG_TARGET_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BASE_H	R/W	0h	The base address for the external target, upper 16 bits. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.8 SEC_PROXY_SCFG_ORDERID Register

1 SEC_PROXY_SCFG_ORDERID Register (Offset = 10h) [reset = 0h]

The Buffer OrderID Register contains the bus orderid value for the buffer memory access.

Return to Summary Table

Table 14-17004. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0010h**

Figure 14-5625. SEC_PROXY_SCFG_ORDERID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			REPLACE	ORDERID			
NONE			R/W	R/W			
0h			0h	0h			

Table 14-17006. SEC_PROXY_SCFG_ORDERID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REPLACE	R/W	0h	Indicates to replace the bus orderid value for the buffer access with the orderid MMR field. This allows control over the orderid value when it must be restricted due to the topology for QoS reasons. 0 = bypass and use the orderid from the source transaction for the destination transaction. 1 = use the orderid MMR field value for the destination transaction. Reset Source: rst_mod_g_rst_n
3:0	ORDERID	R/W	0h	Defines the bus orderid value for the buffer access. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.9 SEC_PROXY_SCFG_THREAD_CTL_j Register

1 SEC_PROXY_SCFG_THREAD_CTL_j Register (Offset = 0h + formula) [reset = 0h]

The Control Register defines controls for proxy thread a.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 75d

Table 14-17007. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0000h + formula**

Figure 14-5626. SEC_PROXY_SCFG_THREAD_CTL_j Name Register

31	30	29	28	27	26	25	24
DIR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAX_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
QUEUE							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE							
R/W							
0h							

Table 14-17009. SEC_PROXY_SCFG_THREAD_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIR	R/W	0h	Direction for the proxy thread. 0 = outbound, write only. 1 = inbound, read only. Reset Source: rst_mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	MAX_CNT	R/W	0h	Max message count allowed for an outbound proxy thread. Is not used otherwise. Reset Source: rst_mod_g_rst_n
15:0	QUEUE	R/W	0h	Queue number in the target to use for the proxy thread. If the target base does not start at queue 0 then this is the relative queue number from that base queue. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.10 SEC_PROXY_SCFG_THREAD_EVT_MAP_j Register

1 SEC_PROXY_SCFG_THREAD_EVT_MAP_j Register (Offset = 4h + formula) [reset = FFFFFFFFh]

The Event Map Register defines the event numbers for proxy thread a.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 75d

Table 14-17010. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A40 0004h + formula**

Figure 14-5627. SEC_PROXY_SCFG_THREAD_EVT_MAP_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ERR_EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ERR_EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">THR_EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">THR_EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-17012. SEC_PROXY_SCFG_THREAD_EVT_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ERR_EVT	R/W	FFFFh	Event number for an error from the proxy thread. Reset Source: rst_mod_g_rst_n
15:0	THR_EVT	R/W	FFFFh	Event number for a threshold event from the proxy thread. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.11 SEC_PROXY_SCFG_THREAD_DST_j Register

1 SEC_PROXY_SCFG_THREAD_DST_j Register (Offset = 8h + formula) [reset = 0h]

The Destination Register defines the destination proxy thread for outbound proxy thread a.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 75d

Table 14-17013. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	4A40 0008h + formula

Figure 14-5628. SEC_PROXY_SCFG_THREAD_DST_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD							
R/W							
0h							

Table 14-17015. SEC_PROXY_SCFG_THREAD_DST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD	R/W	0h	The proxy thread that is the destination of messages from this outbound proxy thread, based on the queue numbers. This is ignored for inbound proxy threads. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.12 SEC_PROXY_RT_THREAD_STATUS_j Register

1 SEC_PROXY_RT_THREAD_STATUS_j Register (Offset = 0h + formula) [reset = 0h]

The Status Register gives status for proxy thread a.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 75d

Table 14-17016. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	4A60 0000h + formula

Figure 14-5629. SEC_PROXY_RT_THREAD_STATUS_j Name Register

31	30	29	28	27	26	25	24
ERROR	DIR	RESERVED					
R/W	R	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAX_CNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUR_CNT							
R							
0h							

Table 14-17018. SEC_PROXY_RT_THREAD_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERROR	R/W	0h	Error detected on proxy thread. The error will also use the err_evt field to generate an error event which can generate an interrupt. While in error a proxy thread will not process any operations. Write a 0 to clear the error and reset the proxy thread. Reset Source: rst_mod_g_rst_n
30	DIR	R	0h	Direction for the proxy thread. 0 = outbound, write only. 1 = inbound, read only. Reset Source: rst_mod_g_rst_n
29:24	RESERVED	NONE	0h	Reserved
23:16	MAX_CNT	R	0h	Max message count allowed for an outbound proxy thread. Reset Source: rst_mod_g_rst_n
15:8	RESERVED	NONE	0h	Reserved

Table 14-17018. SEC_PROXY_RT_THREAD_STATUS_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	CUR_CNT	R	0h	Current message count for the proxy thread. For an inbound proxy this is the number of available messages. For an outbound proxy this is the number of free messages that can be written. This value will initialize itself to 0 if the THREAD[a]_CTL register is written with dir set to inbound, or to the max_cnt value if the THREAD[a]_CTL register is written with dir set to outbound, as these are the starting values for a newly configured thread. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.13 SEC_PROXY_RT_THREAD_THR_j Register

1 SEC_PROXY_RT_THREAD_THR_j Register (Offset = 4h + formula) [reset = 0h]

The Threshold Register controls the threshold for proxy thread a events.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 75d

Table 14-17019. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4A60 0004h + formula**

Figure 14-5630. SEC_PROXY_RT_THREAD_THR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
THR_CNT							
R/W							
0h							

Table 14-17021. SEC_PROXY_RT_THREAD_THR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	THR_CNT	R/W	0h	Threshold count that causes proxy thread events. For an outbound proxy this will be the number of free messages to cause an event. For an inbound proxy this will be the number of available messages to cause an event. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.14 PROXY_TARGET_THREAD_DATA_j Register

1 PROXY_TARGET_THREAD_DATA_j Register (Offset = 0h + formula) [reset = 0h]

The Proxy Private register contains private information for the proxy thread a and should not be written, writes are ignored. Reads are allowed to know the source thread of the message.

Return to Summary Table

Offset = (j * 1000h); where j = 0 to 75d

Table 14-17022. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4D00 0000h + formula**

Figure 14-5631. PROXY_TARGET_THREAD_DATA_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						SRC_THR	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
SRC_THR							
R							
0h							

Table 14-17024. PROXY_TARGET_THREAD_DATA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	SRC_THR	R	0h	Proxy source thread of message. Reset Source: rst_mod_g_rst_n

14.7.3.1.2.15 PROXY_TARGET_THREAD_MESSAGE_j_k Register

1 PROXY_TARGET_THREAD_MESSAGE_j_k Register (Offset = 4h + formula) [reset = 0h]

The Message Data for proxy thread a. The word with index b = 14 contains the completion final byte.

Return to Summary Table

Offset = (j * 1000h) + (k * 4h); where j = 0 to 75d, k = 0 to 14d

Table 14-17025. Instance Table

Instance Name	Physical Address
DMASS0_SEC_PROXY_0	**4D00 0004h + formula**

Figure 14-5632. PROXY_TARGET_THREAD_MESSAGE_j_k Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17027. PROXY_TARGET_THREAD_MESSAGE_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Proxy Message Data Reset Source: rst_mod_g_rst_n

14.7.4 INTAGGR Registers

14.7.4.1 DMASS_INTAGGR_0 Registers

14.7.4.1.1 DMASS_INTAGGR_0 Summary Table

Table 14-17028. DMASS0_INTAGGR_INTR Registers, Base Address=4800 0000h, Length=1048576

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
0h + formula	64	INTAGGR_INTR_VINT_ENABLE_SET_j	4800 0000h
8h + formula	64	INTAGGR_INTR_VINT_ENABLE_CLEAR_j	4800 0008h
10h + formula	64	INTAGGR_INTR_VINT_STATUS_SET_j	4800 0010h
18h + formula	64	INTAGGR_INTR_VINT_STATUS_CLEAR_j	4800 0018h
20h + formula	64	INTAGGR_INTR_VINT_STATUSM_j	4800 0020h

Table 14-17029. DMASS0_INTAGGR_IMAP Registers, Base Address=4810 0000h, Length=16384

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
0h + formula	64	INTAGGR_IMAP_GEVI_IMAP_j	4810 0000h

Table 14-17030. DMASS0_INTAGGR_CFG Registers, Base Address=4811 0000h, Length=32

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
0h	64	INTAGGR_CFG_REVISION	4811 0000h
8h	64	INTAGGR_CFG_INTCAP	4811 0008h
10h	64	INTAGGR_CFG_AUXCAP	4811 0010h

Table 14-17031. DMASS0_INTAGGR_L2G Registers, Base Address=4812 0000h, Length=1024

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
0h + formula	64	INTAGGR_L2G_LEVI_MAP_j	4812 0000h

Table 14-17032. DMASS0_INTAGGR_UNMAP Registers, Base Address=4818 0000h, Length=131072

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
0h + formula	64	INTAGGR_UNMAP_UNMAP0_MAP_j	4818 0000h
8000h + formula	64	INTAGGR_UNMAP_UNMAP1_MAP_j	4818 8000h
9000h + formula	64	INTAGGR_UNMAP_UNMAP2_MAP_j	4818 9000h
A000h + formula	64	INTAGGR_UNMAP_UNMAP3_MAP_j	4818 A000h
B000h + formula	64	INTAGGR_UNMAP_UNMAP4_MAP_j	4818 B000h
C000h + formula	64	INTAGGR_UNMAP_UNMAP5_MAP_j	4818 C000h
D000h + formula	64	INTAGGR_UNMAP_UNMAP6_MAP_j	4818 D000h
10000h + formula	64	INTAGGR_UNMAP_UNMAP7_MAP_j	4819 0000h
11000h + formula	64	INTAGGR_UNMAP_UNMAP8_MAP_j	4819 1000h
12000h + formula	64	INTAGGR_UNMAP_UNMAP9_MAP_j	4819 2000h
13000h + formula	64	INTAGGR_UNMAP_UNMAP10_MAP_j	4819 3000h
14000h + formula	64	INTAGGR_UNMAP_UNMAP11_MAP_j	4819 4000h
15000h + formula	64	INTAGGR_UNMAP_UNMAP12_MAP_j	4819 5000h
16000h + formula	64	INTAGGR_UNMAP_UNMAP13_MAP_j	4819 6000h

Table 14-17032. DMASS0_INTAGGR_UNMAP Registers, Base Address=4818 0000h, Length=131072 (continued)

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
17000h + formula	64	INTAGGR_UNMAP_UNMAP14_MAP_j	4819 7000h
18000h + formula	64	INTAGGR_UNMAP_UNMAP15_MAP_j	4819 8000h

Table 14-17033. DMASS0_INTAGGR_MCAST Registers, Base Address=4821 0000h, Length=4096

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
0h + formula	64	INTAGGR_MCAST_GEVI_MCMAP_j	4821 0000h

Table 14-17034. DMASS0_INTAGGR_GCNTCFG Registers, Base Address=4822 0000h, Length=8192

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
0h + formula	64	INTAGGR_GCNTCFG_GEVI_MAP_j	4822 0000h

Table 14-17035. DMASS0_INTAGGR_GCNTRTI Registers, Base Address=4A00 0000h, Length=1048576

Offset	Length	Register Name	DMASS_INTAGGR_0 Physical Address
0h + formula	64	INTAGGR_GCNTRTI_GEVI_COUNT_j	4A00 0000h

14.7.4.1.2 INTAGGR_INTR_VINT_ENABLE_SET_j Register

INTAGGR_INTR_VINT_ENABLE_SET_j Register (Offset = 0h + formula) [reset = 0h]

Register Description: The Interrupt Enable Set register is written by software to enable (i.e. unmask) specified bits to allow their current status to be considered in the generation of the corresponding level sensitive virtual interrupt output.

Formula = (j * 1000h); where j = 0 to 183d

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Table 14-17036. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_INTR	4800 0000h + formula

Figure 14-5633. INTAGGR_INTR_VINT_ENABLE_SET_j Name Register

63	62	61	60	59	58	57	56
INTR_ENABLE							
R/W1TS							
0h							
55	54	53	52	51	50	49	48
INTR_ENABLE							
R/W1TS							
0h							
47	46	45	44	43	42	41	40
INTR_ENABLE							
R/W1TS							
0h							
39	38	37	36	35	34	33	32
INTR_ENABLE							
R/W1TS							
0h							
31	30	29	28	27	26	25	24
INTR_ENABLE							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
INTR_ENABLE							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
INTR_ENABLE							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
INTR_ENABLE							
R/W1TS							
0h							

Table 14-17038. INTAGGR_INTR_VINT_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_ENABLE	R/W1TS	0h	Interrupt enable set value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be set. Reads will reflect back the current status of the internal interrupt enable register. Reset Source: srst_n

14.7.4.1.3 INTAGGR_INTR_VINT_ENABLE_CLEAR_j Register

INTAGGR_INTR_VINT_ENABLE_CLEAR_j Register (Offset = 8h + formula) [reset = 0h]

Register Description: The Interrupt Enable Clear register is written by software to disable (i.e. mask) specified bits to disallow their current status from be considered in the generation of the corresponding level sensitive virtual interrupt output.

Formula = (j * 1000h); where j = 0 to 183d

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Table 14-17039. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_INTR	4800 0008h + formula

Figure 14-5634. INTAGGR_INTR_VINT_ENABLE_CLEAR_j Name Register

63	62	61	60	59	58	57	56
INTR_ENABLE							
R/W1TC							
0h							
55	54	53	52	51	50	49	48
INTR_ENABLE							
R/W1TC							
0h							
47	46	45	44	43	42	41	40
INTR_ENABLE							
R/W1TC							
0h							
39	38	37	36	35	34	33	32
INTR_ENABLE							
R/W1TC							
0h							
31	30	29	28	27	26	25	24
INTR_ENABLE							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
INTR_ENABLE							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
INTR_ENABLE							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
INTR_ENABLE							
R/W1TC							
0h							

Table 14-17041. INTAGGR_INTR_VINT_ENABLE_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_ENABLE	R/W1TC	0h	Interrupt enable clear value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be cleared. Reads will reflect back the current status of the internal interrupt enable register. Reset Source: srst_n

14.7.4.1.4 INTAGGR_INTR_VINT_STATUS_SET_j Register

INTAGGR_INTR_VINT_STATUS_SET_j Register (Offset = 10h + formula) [reset = 0h]

Register Description: The Interrupt Status register is read by software to determine the cause of an interrupt.

Formula = (j * 1000h); where j = 0 to 183d

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Table 14-17042. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_INTR	4800 0010h + formula

Figure 14-5635. INTAGGR_INTR_VINT_STATUS_SET_j Name Register

63	62	61	60	59	58	57	56
INTR_STATUS							
R/W1TS							
0h							
55	54	53	52	51	50	49	48
INTR_STATUS							
R/W1TS							
0h							
47	46	45	44	43	42	41	40
INTR_STATUS							
R/W1TS							
0h							
39	38	37	36	35	34	33	32
INTR_STATUS							
R/W1TS							
0h							
31	30	29	28	27	26	25	24
INTR_STATUS							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
INTR_STATUS							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
INTR_STATUS							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
INTR_STATUS							
R/W1TS							
0h							

Table 14-17044. INTAGGR_INTR_VINT_STATUS_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUS	R/W1TS	0h	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be set Reset Source: srst_n

14.7.4.1.5 INTAGGR_INTR_VINT_STATUS_CLEAR_j Register

INTAGGR_INTR_VINT_STATUS_CLEAR_j Register (Offset = 18h + formula) [reset = 0h]

Register Description: The Interrupt Status register is read by software to determine the cause of an interrupt.

Formula = (j * 1000h); where j = 0 to 183d

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Table 14-17045. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_INTR	4800 0018h + formula

Figure 14-5636. INTAGGR_INTR_VINT_STATUS_CLEAR_j Name Register

63	62	61	60	59	58	57	56
INTR_STATUS							
R/W1TC							
0h							
55	54	53	52	51	50	49	48
INTR_STATUS							
R/W1TC							
0h							
47	46	45	44	43	42	41	40
INTR_STATUS							
R/W1TC							
0h							
39	38	37	36	35	34	33	32
INTR_STATUS							
R/W1TC							
0h							
31	30	29	28	27	26	25	24
INTR_STATUS							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
INTR_STATUS							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
INTR_STATUS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
INTR_STATUS							
R/W1TC							
0h							

Table 14-17047. INTAGGR_INTR_VINT_STATUS_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUS	R/W1TC	0h	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be cleared Reset Source: srst_n

14.7.4.1.6 INTAGGR_INTR_VINT_STATUSM_j Register

INTAGGR_INTR_VINT_STATUSM_j Register (Offset = 20h + formula) [reset = 0h]

Register Description: The Interrupt Masked Status register can be read by software to determine the cause of an interrupt.

Formula = (j * 1000h); where j = 0 to 183d

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Table 14-17048. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_INTR	4800 0020h + formula

Figure 14-5637. INTAGGR_INTR_VINT_STATUSM_j Name Register

63	62	61	60	59	58	57	56
INTR_STATUSM							
R/NA							
0h							
55	54	53	52	51	50	49	48
INTR_STATUSM							
R/NA							
0h							
47	46	45	44	43	42	41	40
INTR_STATUSM							
R/NA							
0h							
39	38	37	36	35	34	33	32
INTR_STATUSM							
R/NA							
0h							
31	30	29	28	27	26	25	24
INTR_STATUSM							
R/NA							
0h							
23	22	21	20	19	18	17	16
INTR_STATUSM							
R/NA							
0h							
15	14	13	12	11	10	9	8
INTR_STATUSM							
R/NA							
0h							
7	6	5	4	3	2	1	0
INTR_STATUSM							
R/NA							
0h							

Table 14-17050. INTAGGR_INTR_VINT_STATUSM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUSM	R/NA	0h	Masked state of bits in internal interrupt status register. This value is the result of bitwise ANDing the interrupt enable and status registers Reset Source: srst_n

14.7.4.1.7 INTAGGR_IMAP_GEVI_IMAP_j Register

INTAGGR_IMAP_GEVI_IMAP_j Register (Offset = 0h + formula) [reset = 0h]

Register Description: The Interrupt Mapping Register controls which of N virtual interrupt source outputs this channels physical interrupt sources will map onto.

Formula = (j * 8h); where j = 0 to 1535d

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Table 14-17051. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_IMAP	4810 0000h + formula

Figure 14-5638. INTAGGR_IMAP_GEVI_IMAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							REGNUM
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
REGNUM							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED		BITNUM					
NONE		R/W					
0h		0h					

Table 14-17053. INTAGGR_IMAP_GEVI_IMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:17	RESERVED	NONE	0h	Reserved
16:8	REGNUM	R/W	0h	Virtual interrupt status register number: this field specifies which of the potential virtual interrupt cause registers the event pending bit will appear in. Reset Source: srst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	BITNUM	R/W	0h	Virtual interrupt cause register bit number: this field specifies which of the 64 bits in the specified virtual interrupt cause register the event pending bit will appear in. Reset Source: srst_n

14.7.4.1.8 INTAGGR_CFG_REVISION Register

INTAGGR_CFG_REVISION Register (Offset = 0h) [reset = 66961101h]

Register Description: The Revision Register contains the major and minor revisions for the module.

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Table 14-17054. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_CFG	4811 0000h

Figure 14-5639. INTAGGR_CFG_REVISION Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
MODID							
R							
6696h							
23	22	21	20	19	18	17	16
MODID							
R							
6696h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
2h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-17056. INTAGGR_CFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved

Table 14-17056. INTAGGR_CFG_REVISION Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31:16	MODID	R	6696h	Module ID field Reset Source: srst_n
15:11	REVRTL	R	2h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: srst_n

14.7.4.1.9 INTAGGR_CFG_INTCAP Register

INTAGGR_CFG_INTCAP Register (Offset = 8h) [reset = B80600h]

Register Description: The IntCap Register contains information on virtual interrupts.

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Table 14-17057. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_CFG	4811 0008h

Figure 14-5640. INTAGGR_CFG_INTCAP Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
VINTR_CNT							
R							
B8h							
23	22	21	20	19	18	17	16
VINTR_CNT							
R							
B8h							
15	14	13	12	11	10	9	8
SEVT_CNT							
R							
600h							
7	6	5	4	3	2	1	0
SEVT_CNT							
R							
600h							

Table 14-17059. INTAGGR_CFG_INTCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved

Table 14-17059. INTAGGR_CFG_INTCAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31:16	VINTR_CNT	R	B8h	Virtual interrupt register/pin count Reset Source: srst_n
15:0	SEVT_CNT	R	600h	Number of 'event to virt int' mapping registers Reset Source: srst_n

14.7.4.1.10 INTAGGR_CFG_AUXCAP Register

INTAGGR_CFG_AUXCAP Register (Offset = 10h) [reset = 30140080001FFFA8h]

Register Description: The AuxCap Register contains information on additional capabilities.

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Table 14-17060. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_CFG	4811 0010h

Figure 14-5641. INTAGGR_CFG_AUXCAP Name Register

63	62	61	60	59	58	57	56
UNMAP_CNT							
R							
3014h							
55	54	53	52	51	50	49	48
UNMAP_CNT							
R							
3014h							
47	46	45	44	43	42	41	40
MEVI_CNT							
R							
80h							
39	38	37	36	35	34	33	32
MEVI_CNT							
R							
80h							
31	30	29	28	27	26	25	24
LEVI_CNT							
R							
20h							
23	22	21	20	19	18	17	16
LEVI_CNT							
R							
20h							
15	14	13	12	11	10	9	8
GEVI_CNT							
R							
100h							
7	6	5	4	3	2	1	0
GEVI_CNT							
R							
100h							

Table 14-17062. INTAGGR_CFG_AUXCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	UNMAP_CNT	R	3014h	Number of multicast event registers. Not all registers in the range are necessarily valid. Reset Source: srst_n
47:32	MEVI_CNT	R	80h	Number of multicast event registers Reset Source: srst_n
31:16	LEVI_CNT	R	20h	Local input events for local to global translation Reset Source: srst_n
15:0	GEVI_CNT	R	100h	Number of event counting registers Reset Source: srst_n

14.7.4.1.11 INTAGGR_L2G_LEVI_MAP_j Register

INTAGGR_L2G_LEVI_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

Register Description: This register determines how the ordinal local event is translated to a global event on the outgoing event transport lane. Both pulse and rising edge local event types are supported. With pulsed events, the event count is determined by the number of cycles for which the event signal remains high. For rising edge events, the count represents the total number of rising edge transitions. The index field of the register determines the outgoing global event index, and the mode bit specifies either pulsed or rising edge local event detection.

Formula = (j * 20h); where j = 0 to 31d

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Table 14-17063. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_L2G	4812 0000h + formula

Figure 14-5642. INTAGGR_L2G_LEVI_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
MODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
GEVIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
GEVIDX							

Figure 14-5642. INTAGGR_L2G_LEVI_MAP_j Name Register (continued)

R/W
FFFFh

Table 14-17065. INTAGGR_L2G_LEVI_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	MODE	R/W	0h	Local event detection mode. This field is set to 0 for pulsed events, and to 1 for rising edge eventss Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	GEVIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.12 INTAGGR_UNMAP_UNMAP0_MAP_j Register

INTAGGR_UNMAP_UNMAP0_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 1023d

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Table 14-17066. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4818 0000h + formula

Figure 14-5643. INTAGGR_UNMAP_UNMAP0_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17068. INTAGGR_UNMAP_UNMAP0_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.13 INTAGGR_UNMAP_UNMAP1_MAP_j Register

INTAGGR_UNMAP_UNMAP1_MAP_j Register (Offset = 8000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 41d

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Table 14-17069. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4818 8000h + formula

Figure 14-5644. INTAGGR_UNMAP_UNMAP1_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17071. INTAGGR_UNMAP_UNMAP1_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.14 INTAGGR_UNMAP_UNMAP2_MAP_j Register

INTAGGR_UNMAP_UNMAP2_MAP_j Register (Offset = 9000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 111d

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Table 14-17072. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4818 9000h + formula

Figure 14-5645. INTAGGR_UNMAP_UNMAP2_MAP_j Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>56</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>IRQMODE</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-17074. INTAGGR_UNMAP_UNMAP2_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.15 INTAGGR_UNMAP_UNMAP3_MAP_j Register

INTAGGR_UNMAP_UNMAP3_MAP_j Register (Offset = A000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 28d

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Table 14-17075. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4818 A000h + formula

Figure 14-5646. INTAGGR_UNMAP_UNMAP3_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17077. INTAGGR_UNMAP_UNMAP3_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.16 INTAGGR_UNMAP_UNMAP4_MAP_j Register

INTAGGR_UNMAP_UNMAP4_MAP_j Register (Offset = B000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 175d

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Table 14-17078. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4818 B000h + formula

Figure 14-5647. INTAGGR_UNMAP_UNMAP4_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17080. INTAGGR_UNMAP_UNMAP4_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.17 INTAGGR_UNMAP_UNMAP5_MAP_j Register

INTAGGR_UNMAP_UNMAP5_MAP_j Register (Offset = C000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 175d

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Table 14-17081. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4818 C000h + formula

Figure 14-5648. INTAGGR_UNMAP_UNMAP5_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17083. INTAGGR_UNMAP_UNMAP5_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.18 INTAGGR_UNMAP_UNMAP6_MAP_j Register

INTAGGR_UNMAP_UNMAP6_MAP_j Register (Offset = D000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 175d

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Table 14-17084. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4818 D000h + formula

Figure 14-5649. INTAGGR_UNMAP_UNMAP6_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17086. INTAGGR_UNMAP_UNMAP6_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.19 INTAGGR_UNMAP_UNMAP7_MAP_j Register

INTAGGR_UNMAP_UNMAP7_MAP_j Register (Offset = 10000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 27d

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Table 14-17087. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 0000h + formula

Figure 14-5650. INTAGGR_UNMAP_UNMAP7_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17089. INTAGGR_UNMAP_UNMAP7_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.20 INTAGGR_UNMAP_UNMAP8_MAP_j Register

INTAGGR_UNMAP_UNMAP8_MAP_j Register (Offset = 11000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 27d

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Table 14-17090. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 1000h + formula

Figure 14-5651. INTAGGR_UNMAP_UNMAP8_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17092. INTAGGR_UNMAP_UNMAP8_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.21 INTAGGR_UNMAP_UNMAP9_MAP_j Register

INTAGGR_UNMAP_UNMAP9_MAP_j Register (Offset = 12000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 27d

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Table 14-17093. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 2000h + formula

Figure 14-5652. INTAGGR_UNMAP_UNMAP9_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17095. INTAGGR_UNMAP_UNMAP9_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.22 INTAGGR_UNMAP_UNMAP10_MAP_j Register

INTAGGR_UNMAP_UNMAP10_MAP_j Register (Offset = 13000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 19d

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Table 14-17096. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 3000h + formula

Figure 14-5653. INTAGGR_UNMAP_UNMAP10_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17098. INTAGGR_UNMAP_UNMAP10_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.23 INTAGGR_UNMAP_UNMAP11_MAP_j Register

INTAGGR_UNMAP_UNMAP11_MAP_j Register (Offset = 14000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 19d

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Table 14-17099. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 4000h + formula

Figure 14-5654. INTAGGR_UNMAP_UNMAP11_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17101. INTAGGR_UNMAP_UNMAP11_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.24 INTAGGR_UNMAP_UNMAP12_MAP_j Register

INTAGGR_UNMAP_UNMAP12_MAP_j Register (Offset = 15000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 19d

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Table 14-17102. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 5000h + formula

Figure 14-5655. INTAGGR_UNMAP_UNMAP12_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17104. INTAGGR_UNMAP_UNMAP12_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.25 INTAGGR_UNMAP_UNMAP13_MAP_j Register

INTAGGR_UNMAP_UNMAP13_MAP_j Register (Offset = 16000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 19d

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Table 14-17105. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 6000h + formula

Figure 14-5656. INTAGGR_UNMAP_UNMAP13_MAP_j Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>56</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>IRQMODE</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-17107. INTAGGR_UNMAP_UNMAP13_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.26 INTAGGR_UNMAP_UNMAP14_MAP_j Register

INTAGGR_UNMAP_UNMAP14_MAP_j Register (Offset = 17000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 19d

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Table 14-17108. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 7000h + formula

Figure 14-5657. INTAGGR_UNMAP_UNMAP14_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17110. INTAGGR_UNMAP_UNMAP14_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.27 INTAGGR_UNMAP_UNMAP15_MAP_j Register

INTAGGR_UNMAP_UNMAP15_MAP_j Register (Offset = 18000h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 8h); where j = 0 to 19d

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Table 14-17111. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_UNMAP	4819 8000h + formula

Figure 14-5658. INTAGGR_UNMAP_UNMAP15_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-17113. INTAGGR_UNMAP_UNMAP15_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.28 INTAGGR_MCAST_GEVI_MCMAP_j Register

INTAGGR_MCAST_GEVI_MCMAP_j Register (Offset = 0h + formula) [reset = FFFF0000FFFFh]

Register Description: This register determines how ingress global events from the ingress global event ETL are written out to the two egress global event ETL intefaces. The index of each of the two egress events is stored in this register, which is selected based in the ingress event index value.

Formula = (j * 20h); where j = 0 to 127d

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Table 14-17114. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_MCAST	4821 0000h + formula

Figure 14-5659. INTAGGR_MCAST_GEVI_MCMAP_j Name Register

63	62	61	60	59	58	57	56
IRQMODE1	RESERVED						
R/W	NONE						
0h	0h						
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
GEVIDX1							
R/W							
FFFFh							
39	38	37	36	35	34	33	32
GEVIDX1							
R/W							
FFFFh							
31	30	29	28	27	26	25	24
IRQMODE0	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
GEVIDX0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
GEVIDX0							
R/W							
FFFFh							

Table 14-17116. INTAGGR_MCAST_GEVI_MCMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63	IRQMODE1	R/W	0h	IRQ Mode Flag 1. When set, this register act like a mapper with bitnum in 37:32 and regnum in 46:38. Reset Source: srst_n
62:48	RESERVED	NONE	0h	Reserved
47:32	GEVIDX1	R/W	FFFFh	Global event index 1. This field specifies the index of the outgoing global event on ETL 1. Set to 0xFFFF to disable. Reset Source: srst_n
31	IRQMODE0	R/W	0h	IRQ Mode Flag 0. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	GEVIDX0	R/W	FFFFh	Global event index 0. This field specifies the index of the outgoing global event on ETL 0. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.29 INTAGGR_GCNTCFG_GEVI_MAP_j Register

INTAGGR_GCNTCFG_GEVI_MAP_j Register (Offset = 0h + formula) [reset = FFFFh]

Register Description: The Global Event Mapping register controls the egress global event index for this event count. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Formula = (j * 20h); where j = 0 to 255d

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Table 14-17117. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_GCNTCFG	4822 0000h + formula

Figure 14-5660. INTAGGR_GCNTCFG_GEVI_MAP_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
IRQMODE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
GEVIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
GEVIDX							
R/W							
FFFFh							

Table 14-17119. INTAGGR_GCNTCFG_GEVI_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	GEVIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.7.4.1.30 INTAGGR_GCNTRTI_GEVI_COUNT_j Register

INTAGGR_GCNTRTI_GEVI_COUNT_j Register (Offset = 0h + formula) [reset = 0h]

Register Description: The ETL Count register is read by software to determine how many times the event message has been received. This register can be written to decrement the count by a specified amount to acknowledge that a count has been processed by the host.

Formula = (j * 1000h); where j = 0 to 255d

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Table 14-17120. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_GCNTRTI	4A00 0000h + formula

Figure 14-5661. INTAGGR_GCNTRTI_GEVI_COUNT_j Name Register

63	62	61	60	59	58	57	56
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
31	30	29	28	27	26	25	24
CCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
CCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/WTD							
0h							

Table 14-17122. INTAGGR_GCNTRTI_GEVI_COUNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31:0	CCNT	R/WTD	0h	Current count. This field is incremented by the event count for each message received with this event on the Counted ETL Interface. On write, this field will be decremented by the value written. Writing a value greater than the current count is illegal. Reset Source: srst_n

14.7.5 PSI-L Configuration Registers

14.7.5.1 DMASS_PSILCFG_0

DMASS_PSILCFG_0

14.7.5.1.1 DMASS_PSILCFG_0 Summaries

DMASS_PSILCFG_0 Summaries

Table 14-17123. PSILCFG Registers, Base Address=4813 0000h, Length=512

Offset	Length	Register Name	DMASS0_PSILCFG_0 Physical Address
0h	32	PSILCFG_REVISION	4813 0000h
10h	32	PSILCFG_PSIL_TO	4813 0010h
100h	32	PSILCFG_CMDA	4813 0100h
104h	32	PSILCFG_CMDB	4813 0104h
108h	32	PSILCFG_WDATA	4813 0108h
140h	32	PSILCFG_RDATA	4813 0140h

14.7.5.1.2 DMASS_PSILCFG_0 Registers

DMASS_PSILCFG_0 Registers

14.7.5.1.2.1 PSILCFG_REVISION Register

1 PSILCFG_REVISION Register (Offset = 0h) [reset = 66C00100h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-17124. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0000h**

Figure 14-5662. PSILCFG_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">66C0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">66C0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-17126. PSILCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	66C0h	Module ID field Reset Source: srst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: srst_n

14.7.5.1.2.2 PSILCFG_PSIL_TO Register

1 PSILCFG_PSIL_TO Register (Offset = 10h) [reset = 400h]

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrances on PSI-L configuration transactions issued by the built in PSI-L proxy.

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Table 14-17127. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0010h**

Figure 14-5663. PSILCFG_PSIL_TO Name Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W							
400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W							
400h							

Table 14-17129. PSILCFG_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access. Once set, this bit is persistent until manually cleared Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a conifiguration read or write transaction and asserting the tout bit Reset Source: srst_n

14.7.5.1.2.3 PSILCFG_CMDA Register

1 PSILCFG_CMDA Register (Offset = 100h) [reset = 0h]

The Command Register A contains the busy indicator, direction, and thread number for the configuration transaction.

Return to Summary Table

Table 14-17130. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	4813 0100h

Figure 14-5664. PSILCFG_CMDA Name Register

31	30	29	28	27	26	25	24
PROXY_BUSY	PROXY_DIR	PROXY_TOUT	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PROXY_THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
PROXY_THREAD_ID							
R/W							
0h							

Table 14-17132. PSILCFG_CMDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PROXY_BUSY	R/W	0h	Indication that a configuration read or write is in progress Reset Source: srst_n 0 No transaction is in progress 1 Transaction is in progress
30	PROXY_DIR	R/W	0h	Direction of configuration transaction Reset Source: srst_n 0 Write transaction 1 Read transaction
29	PROXY_TOUT	R/W	0h	Indication that a timeout occurred. This bit should be written to 0 on each new transaction. Reset Source: srst_n 0 Transaction completed normally 1 Timeout occurred
28:16	RESERVED	NONE	0h	Reserved
15:0	PROXY_THREAD_ID	R/W	0h	Thread ID to which configuration read or write is being sent Reset Source: srst_n

14.7.5.1.2.4 PSILCFG_CMDB Register

1 PSILCFG_CMDB Register (Offset = 104h) [reset = 0h]

The Command Register B contains the byte enables and word address for the configuration transaction.

Return to Summary Table

Table 14-17133. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0104h**

Figure 14-5665. PSILCFG_CMDB Name Register

31	30	29	28	27	26	25	24
PROXY_BYTEN				RESERVED			
R/W				NONE			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PROXY_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
PROXY_ADDRESS							
R/W							
0h							

Table 14-17135. PSILCFG_CMDB Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PROXY_BYTEN	R/W	0h	Byte enables to use for configuration read or write Reset Source: srst_n
27:16	RESERVED	NONE	0h	Reserved
15:0	PROXY_ADDRESS	R/W	0h	Word (32-bit) address within thread configuration space for transaction Reset Source: srst_n 0 Peer thread ID register. Implemented for src threads only. 1 Peer credit register. Implemented for src threads only. 2 Enable register 64 Capabilities register 1024 Static TR register

14.7.5.1.2.5 PSILCFG_WDATA Register

1 PSILCFG_WDATA Register (Offset = 108h) [reset = 0h]

The Write Data Register contains the data which is to be written during the configuration transaction.

Return to Summary Table

Table 14-17136. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0108h**

Figure 14-5666. PSILCFG_WDATA Name Register

31	30	29	28	27	26	25	24
PROXY_WDATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PROXY_WDATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PROXY_WDATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PROXY_WDATA							
R/W							
0h							

Table 14-17138. PSILCFG_WDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PROXY_WDATA	R/W	0h	Configuration data word to be written Reset Source: srst_n

14.7.5.1.2.6 PSILCFG_RDATA Register

1 PSILCFG_RDATA Register (Offset = 140h) [reset = 0h]

The Read Data Register contains the data which which was read back during the configuration transaction.

Return to Summary Table

Table 14-17139. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	**4813 0140h**

Figure 14-5667. PSILCFG_RDATA Name Register

31	30	29	28	27	26	25	24
PROXY_RDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PROXY_RDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PROXY_RDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PROXY_RDATA							
R/W							
0h							

Table 14-17141. PSILCFG_RDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PROXY_RDATA	R/W	0h	Configuration data word that was read Reset Source: srst_n

14.7.5.2 DMASS_PSILSS_0 Registers

Table 14-17142. psilss_mmrs, DMASS0_PSILSS_0_PSILSS_MMRS Registers, Base Address=4814 0000H, Length=4096

Offset	Length	Acronym	Register Name	DMASS0_PSILSS_0 Physical Address
0h	32	DMASS0_PSILSS_0_pid	Revision Register	4814 0000h
4h	32	DMASS0_PSILSS_0_config	Config Register	4814 0004h
10h	32	DMASS0_PSILSS_0_event	Event Register	4814 0010h
20h	32	DMASS0_PSILSS_0_link	Link Register	4814 0020h
40h	32	DMASS0_PSILSS_0_down	Link Down Register	4814 0040h

Table 14-17143. etlsw_mmrs, DMASS0_PSILSS_0_ETLSW_MMRS Registers, Base Address=4823 0000H, Length=4096

Offset	Length	Acronym	Register Name	DMASS0_PSILSS_0 Physical Address
0h	32	DMASS0_PSILSS_0_pid	Revision Register	4823 0000h
4h	32	DMASS0_PSILSS_0_config	Config Register	4823 0004h
10h	32	DMASS0_PSILSS_0_event	Event Register	4823 0010h
20h	32	DMASS0_PSILSS_0_link	Link Register	4823 0020h
40h	32	DMASS0_PSILSS_0_down	Link Down Register	4823 0040h

1 DMASS0_PSILSS_0_PID Register (Offset = 0h) [reset = 1724168448]

Short Description: Revision Register

Long Description:

Return to Summary Table

Table 14-17144. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4814 0000h**

Figure 14-5668. DMASS0_PSILSS_0_PID Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="12">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="12">R</td></tr>
<tr><td colspan="2">1</td><td colspan="2">10</td><td colspan="12">11011000100</td></tr>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="5">10111</td><td colspan="3">1</td><td colspan="2">0</td><td colspan="6">0</td></tr>
</table>

Access Types Legend

Table 14-17146. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	1h	PID register scheme
29 - 28	BU	R	2h	Business Unit: 10 = Processors
27 - 16	FUNC	R	6C4h	Module ID
15 - 11	RTL	R	17h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	R	1h	Major revision
7 - 6	CUSTOM	R	0h	Custom
5 - 0	MINOR	R	0h	Minor revision

2 DMASS0_PSILSS_0_CONFIG Register (Offset = 4h) [reset = 22]

Short Description: Config Register

Long Description:

Return to Summary Table

Table 14-17147. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4814 0004h**

Figure 14-5669. DMASS0_PSILSS_0_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENDPOINTS															
R															
10110															

Access Types Legend

Table 14-17149. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	ENDPOINTS	R	16h	Number of endpoints supported.

3 DMASS0_PSILSS_0_EVENT Register (Offset = 10h) [reset = 65535]

Short Description: Event Register

Long Description:

Return to Summary Table

Table 14-17150. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4814 0010h**

Figure 14-5670. DMASS0_PSILSS_0_EVENT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVT															
R/W															
1111111111111111															

Access Types Legend

Table 14-17152. EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	EVT	R/W	FFFFh	The event to produce.

4 DMASS0_PSILSS_0_LINK Register (Offset = 20h) [reset = 0]

Short Description: Link Register

Long Description:

Return to Summary Table

Table 14-17153. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4814 0020h**

Figure 14-5671. DMASS0_PSILSS_0_LINK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STATUS															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS															
R															
0															

Access Types Legend

Table 14-17155. LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STATUS	R	0h	The status of the endpoint links.

5 DMASS0_PSILSS_0_DOWN Register (Offset = 40h) [reset = 0]

Short Description: Link Down Register

Long Description:

Return to Summary Table

Table 14-17156. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4814 0040h**

Figure 14-5672. DMASS0_PSILSS_0_DOWN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STATUS															
R/W1TC															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS															
R/W1TC															
0															

Access Types Legend

Table 14-17158. DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STATUS	R/W1TC	0h	The down status of the endpoint links.

6 DMASS0_PSILSS_0_PID Register (Offset = 0h) [reset = 1724168448]

Short Description: Revision Register

Long Description:

Return to Summary Table

Table 14-17159. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4823 0000h**

Figure 14-5673. DMASS0_PSILSS_0_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R		R		R											
1		10		11011000100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R					R			R		R					
10111					1			0		0					

Access Types Legend

Table 14-17161. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	1h	PID register scheme
29 - 28	BU	R	2h	Business Unit: 10 = Processors
27 - 16	FUNC	R	6C4h	Module ID
15 - 11	RTL	R	17h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	R	1h	Major revision
7 - 6	CUSTOM	R	0h	Custom
5 - 0	MINOR	R	0h	Minor revision

7 DMASS0_PSILSS_0_CONFIG Register (Offset = 4h) [reset = 4]

Short Description: Config Register

Long Description:

Return to Summary Table

Table 14-17162. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4823 0004h**

Figure 14-5674. DMASS0_PSILSS_0_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENDPOINTS															
R															
100															

Access Types Legend

Table 14-17164. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	ENDPOINTS	R	4h	Number of endpoints supported.

8 DMASS0_PSILSS_0_EVENT Register (Offset = 10h) [reset = 65535]

Short Description: Event Register

Long Description:

Return to Summary Table

Table 14-17165. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4823 0010h**

Figure 14-5675. DMASS0_PSILSS_0_EVENT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">NONE</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">EVT</td></tr>
<tr><td colspan="16">R/W</td></tr>
<tr><td colspan="16">1111111111111111</td></tr>
</table>

Access Types Legend

Table 14-17167. EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	EVT	R/W	FFFFh	The event to produce.

9 DMASS0_PSILSS_0_LINK Register (Offset = 20h) [reset = 0]

Short Description: Link Register

Long Description:

Return to Summary Table

Table 14-17168. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4823 0020h**

Figure 14-5676. DMASS0_PSILSS_0_LINK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STATUS															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS															
R															
0															

Access Types Legend

Table 14-17170. LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STATUS	R	0h	The status of the endpoint links.

10 DMASS0_PSILSS_0_DOWN Register (Offset = 40h) [reset = 0]

Short Description: Link Down Register

Long Description:

Return to Summary Table

Table 14-17171. Instance Table

Instance Name	Base Address
DMASS0_PSILSS_0	**4823 0040h**

Figure 14-5677. DMASS0_PSILSS_0_DOWN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STATUS															
R/W1TC															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS															
R/W1TC															
0															

Access Types Legend

Table 14-17173. DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STATUS	R/W1TC	0h	The down status of the endpoint links.

Table 14-17174. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear

14.7.6 PDMA Registers

14.7.6.1 PDMA

PDMA

14.7.6.1.1 PDMA Summaries

PDMA Summaries

Table 14-17175. ECC_AGGR Registers, Base Address=00C0 0000h, Length=1024

Offset	Length	Register Name	PDMA0 Physical Address	PDMA1 Physical Address
0h	32	ECC_AGGR_REV	00C0 0000h	00C0 1000h
8h	32	ECC_AGGR_VECTOR	00C0 0008h	00C0 1008h
Ch	32	ECC_AGGR_STAT	00C0 000Ch	00C0 100Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	00C0 0010h + formula	00C0 1010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	00C0 003Ch	00C0 103Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	00C0 0040h	00C0 1040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	00C0 0080h	00C0 1080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	00C0 00C0h	00C0 10C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	00C0 013Ch	00C0 113Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	00C0 0140h	00C0 1140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	00C0 0180h	00C0 1180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	00C0 01C0h	00C0 11C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	00C0 0200h	00C0 1200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	00C0 0204h	00C0 1204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	00C0 0208h	00C0 1208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	00C0 020Ch	00C0 120Ch

14.7.6.1.2 PDMA Registers

PDMA Registers

14.7.6.1.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

Return to Summary Table

Table 14-17176. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0000h**
PDMA1	**00C0 1000h**

Figure 14-5678. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-17178. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.6.1.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

Return to Summary Table

Table 14-17179. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0008h**
PDMA1	**00C0 1008h**

Figure 14-5679. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h

23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							

15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		

7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-17181. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.6.1.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

Return to Summary Table

Table 14-17182. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 000Ch**
PDMA1	**00C0 100Ch**

Figure 14-5680. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-17184. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.6.1.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 7d

Table 14-17185. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0010h + formula
PDMA1	00C0 1010h + formula

Figure 14-5681. ECC_AGGR_RESERVED_SVBUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17187. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.6.1.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-17188. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 003Ch**
PDMA1	**00C0 103Ch**

Figure 14-5682. ECC_AGGR_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-17190. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.6.1.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-17191. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0040h**
PDMA1	**00C0 1040h**

Figure 14-5683. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_PEND	RPCF0_RAMECC_PEND	TPCF1_RAMECC_PEND	TPCF0_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-17193. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf1_ramecc_pend
2	RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf0_ramecc_pend
1	TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf1_ramecc_pend
0	TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf0_ramecc_pend

14.7.6.1.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-17194. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0080h**
PDMA1	**00C0 1080h**

Figure 14-5684. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-17196. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf0_ramecc_pend

14.7.6.1.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-17197. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 00C0h**
PDMA1	**00C0 10C0h**

Figure 14-5685. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_CLR	RPCF0_RAMECC_ENABLE_CLR	TPCF1_RAMECC_ENABLE_CLR	TPCF0_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-17199. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf0_ramecc_pend

14.7.6.1.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-17200. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 013Ch**
PDMA1	**00C0 113Ch**

Figure 14-5686. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-17202. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.6.1.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-17203. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0140h**
PDMA1	**00C0 1140h**

Figure 14-5687. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_PEND	RPCF0_RAMECC_PEND	TPCF1_RAMECC_PEND	TPCF0_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-17205. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf1_ramecc_pend
2	RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf0_ramecc_pend
1	TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf1_ramecc_pend
0	TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf0_ramecc_pend

14.7.6.1.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-17206. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0180h**
PDMA1	**00C0 1180h**

Figure 14-5688. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-17208. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf0_ramecc_pend

14.7.6.1.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-17209. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 01C0h**
PDMA1	**00C0 11C0h**

Figure 14-5689. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RPCF1_RAMECC_ENABLE_CLR	RPCF0_RAMECC_ENABLE_CLR	TPCF1_RAMECC_ENABLE_CLR	TPCF0_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-17211. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf0_ramecc_pend

14.7.6.1.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 14-17212. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0200h**
PDMA1	**00C0 1200h**

Figure 14-5690. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-17214. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.6.1.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-17215. Instance Table

Instance Name	**Physical Address**
PDMA0	**00C0 0204h**
PDMA1	**00C0 1204h**

Figure 14-5691. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-17217. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.6.1.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-17218. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 0208h**
PDMA1	**00C0 1208h**

Figure 14-5692. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-17220. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.6.1.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-17221. Instance Table

Instance Name	Physical Address
PDMA0	**00C0 020Ch**
PDMA1	**00C0 120Ch**

Figure 14-5693. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-17223. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.6.2 PDMA PSI-L TX Configuration Registers

Table 14-11532 lists the PDMA PSI-L TX configuration registers (PDMA_PSILCFG_TX). These registers are not memory mapped and are accessed indirectly via CFG_PROXY modules in DMSS.

Table 14-17224. PDMA_PSILCFG_TX Instances

Instance	Base Address
PDMA_PSILCFG_TX	N/A

Table 14-17225. PDMA_PSILCFG_TX Registers

Offset	Acronym	Register Name	PDMA_PSILCFG_TX Physical Address
2h	PDMA_PSILCFG_TX_ENABLE	TX enable register	N/A
40h	PDMA_PSILCFG_TX_CAPABILITIES	TX local capabilities register	N/A
400h	PDMA_PSILCFG_TX_STATIC_TR	TX static transfer request (X, Y) register	N/A
402h	PDMA_PSILCFG_TX_DEBUG_1	TX debug/state register 1	N/A
403h	PDMA_PSILCFG_TX_DEBUG_2	TX debug/state register 2	N/A
404h	PDMA_PSILCFG_TX_BYTE_COUNT	TX byte count register	N/A

1 PDMA_PSILCFG_TX_ENABLE Register (Offset = 2h) [reset = 0h]

PDMA_PSILCFG_TX_ENABLE is shown in Figure 14-5694 and described in Table 14-11534.

Return to Summary Table.

Enable Register. This register contains enable control for the thread.

Table 14-17226. PDMA_PSILCFG_TX_ENABLE Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 14-5694. PDMA_PSILCFG_TX_ENABLE Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17228. PDMA_PSILCFG_TX_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	When set, the TX channel is enabled. When cleared, the TX channel is disabled. When disabled, the channel discards all ingress data. A one-to-zero transition on this bit fully resets the channel.
30-0	RESERVED	R	0h	Reserved

2 PDMA_PSILCFG_TX_CAPABILITIES Register (Offset = 40h) [reset = Xh]

PDMA_PSILCFG_TX_CAPABILITIES is shown in Figure 14-5695 and described in Table 14-11536.

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Local Capabilities Register. This register provides the width and count of the credits for which buffering is available in the local thread. This register can be read by the system configuration software to determine what values to place in the following registers of the source paired thread:

- PDMA_PSILCFG_RX_PEER_CREDIT and PDMA_PSILCFG_RX_PEER_THREAD_ID

This register is only implemented for destination threads.

Table 14-17229. PDMA_PSILCFG_TX_CAPABILITIES Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 14-5695. PDMA_PSILCFG_TX_CAPABILITIES Register

31	30	29	28	27	26	25	24
RESERVED			LOCAL_THREAD_WIDTH				
R-0h			R-2h				

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
LOCAL_CREDIT_CNT							
R-8h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17231. PDMA_PSILCFG_TX_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	LOCAL_THREAD_WIDTH	R	2h	Read-only element width for the local thread used for pairing purposes. 0h = 4 bytes 1h = 8 bytes 2h = 16 bytes 3h to 1Fh = Reserved
23-8	RESERVED	R	0h	Reserved
7-0	LOCAL_CREDIT_CNT	R	7h	Read-only local thread free entry count used for pairing purposes. This field is encoded as follows: 0h to 80h = Available count in elements 81h to FFh = Reserved

3 PDMA_PSILCFG_TX_STATIC_TR Register (Offset = 400h) [reset = 0h]

PDMA_PSILCFG_TX_STATIC_TR is shown in Figure 14-5696 and described in Table 14-11538.

Return to Summary Table.

Static Transfer Request (X, Y) Register. This register is used to define the 'X' and 'Y' parameters in a static TR.

Table 14-17232. PDMA_PSILCFG_TX_STATIC_TR Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 14-5696. PDMA_PSILCFG_TX_STATIC_TR Register

31	30	29	28	27	26	25	24
BURST	ACC32	RESERVED			X		
R/W-0h	R/W-0h	R-0h			R/W-0h		

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED				Y			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
Y							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17234. PDMA_PSILCFG_TX_STATIC_TR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BURST	R/W	0h	**X-Y FIFO mode static TR:** When set, enables VBUSP burst mode on this channel. See the XY burst description for more information. **MCAN mode static TR:** When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information. **AASRC mode static TR:** Not used.
30	ACC32	R/W	0h	**X-Y FIFO mode static TR:** When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide. **MCAN mode static TR:** Not used.

Table 14-17234. PDMA_PSILCFG_TX_STATIC_TR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				AASRC mode static TR: When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
29-27	RESERVED	R	0h	Reserved
26-24	X	R/W	0h	**X-Y FIFO mode static TR:** Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0h = 8 bits; 1h =16 bits; 2h = 24 bits; 3h = 32 bits; 4h = 64 bits; 5h-7h = RESERVED.
				MCAN mode static TR: Not used.
				AASRC mode static TR: Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0h = 8 bits; 1h =16 bits; 2h = 24 bits; 3h = 32 bits; 4h = 64 bits; 5h-7h = RESERVED.
23-12	RESERVED	R	0h	Reserved
11-0	Y	R/W	0h	**X-Y FIFO mode static TR:** Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
				MCAN mode static TR: Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8-byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8-byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
				AASRC mode static TR: FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.

4 PDMA_PSILCFG_TX_DEBUG_1 Register (Offset = 402h) [reset = 0h]

PDMA_PSILCFG_TX_DEBUG_1 is shown in Figure 14-5697 and described in Table 14-11540.

Return to Summary Table.

Debug/State Register 1. The debug/state registers give software applications additional information about the PDMA than they would need in regular opteration, but which may be useful in debug situations.

Table 14-17235. PDMA_PSILCFG_TX_DEBUG_1 Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 14-5697. PDMA_PSILCFG_TX_DEBUG_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESEREVD							
R-0h							

15	14	13	12	11	10	9	8
Y							
R/W-0h							

7	6	5	4	3	2	1	0
Y							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17237. PDMA_PSILCFG_TX_DEBUG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	Y	R/W	0h	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.

5 PDMA_PSILCFG_TX_DEBUG_2 Register (Offset = 403h) [reset = 0h]

PDMA_PSILCFG_TX_DEBUG_2 is shown in Figure 14-5698 and described in Table 14-11542.

Return to Summary Table.

Debug/State Register 2. The debug/state registers give software applications additional information about the PDMA than they would need in regular opteration, but which may be useful in debug situations.

Table 14-17238. PDMA_PSILCFG_TX_DEBUG_2 Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 14-5698. PDMA_PSILCFG_TX_DEBUG_2 Register

31	30	29	28	27	26	25	24
INEVENT	FLUSH	PAUSE	DATA	XDATA	RESERVED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STATE				EVENTCNT			
R/W-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17240. PDMA_PSILCFG_TX_DEBUG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INEVENT	R/W	0h	When set, the PDMA is in the middle of processing a FIFO event.
30	FLUSH	R/W	0h	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
29	PAUSE	R/W	0h	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the paired-DMA.
28	DATA	R/W	0h	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
27	XDATA	R/W	0h	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
26-24	RESERVED	R	0h	Reserved
23-20	STATE	R/W	0h	This code reflects the current state of the PDMA channel, and is specific to the current implementation.

Table 14-17240. PDMA_PSILCFG_TX_DEBUG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	EVENTCNT	R/W	0h	This field holds the number of backlogged DMA events yet to be serviced.
15-0	RESERVED	R	0h	Reserved

6 PDMA_PSILCFG_TX_BYTE_COUNT Register (Offset = 404h) [reset = 0h]

PDMA_PSILCFG_TX_BYTE_COUNT is shown in Figure 14-5699 and described in Table 14-11544.

Return to Summary Table.

Byte Count Register. This register contains the number of bytes that have been written to the VBUSP mapped peripheral.

Table 14-17241. PDMA_PSILCFG_TX_BYTE_COUNT Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 14-5699. PDMA_PSILCFG_TX_BYTE_COUNT Register

31	30	29	28	27	26	25	24
BYTES							
R/W-0h							
23	22	21	20	19	18	17	16
BYTES							
R/W-0h							
15	14	13	12	11	10	9	8
BYTES							
R/W-0h							
7	6	5	4	3	2	1	0
BYTES							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17243. PDMA_PSILCFG_TX_BYTE_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BYTES	R/W	0h	This register contains the number of bytes that have been read from the VBUSP mapped peripheral. The register is write-to-decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

7 PDMA_PSILCFG_TX_RT_ENABLE Register (Offset = 408h) [reset = 0h]

PDMA_PSILCFG_TX_RT_ENABLE is shown in Figure 14-5700 and described in Figure 14-5700.

Return to Summary Table.

Real Time Enable Register. This register allows enabling various channel settings in real time.

Table 14-17244. PDMA_PSILCFG_TX_RT_ENABLE Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 14-5700. PDMA_PSILCFG_TX_RT_ENABLE Register

31	30	29	28	27	26	25	24
ENABLE	TDOWN	PAUSE	FLUSH	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ERROR	IDLE	FREE
R-0h					R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17246. PDMA_PSILCFG_TX_RT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	When set, the TX channel is enabled. When cleared, the TX channel is disabled. When disabled, it discards all held data. It clears DMA event counts and ignores all future DMA events from the peripheral. It maintains data exchange with the paired-DMA so that credit handshake is not disrupted. A 'hard teardown' can be performed by directly clearing this bit. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.
30	TDOWN	R/W	0h	When set, the channel will commence a TX channel teardown procedure. To perform a TX teardown, the teardown bit should be set in the paired-DMA and it will automatically propagate to this register bit with the normal flow of peripheral data. Once the channel is fully stopped and ready to be reused (including returning all credits), the ENABLE bit is cleared.
29	PAUSE	R/W	0h	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals but will not act on them. The PAUSE bit can be cleared and data will resume.

Table 14-17246. PDMA_PSILCFG_TX_RT_ENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	FLUSH	R/W	0h	When set, causes all TX channel data to be discarded instead of being written to the peripheral. It essentially allows the TX engine to 'free run' without DMA requests from the peripheral (it will also override 'pause'). This bit should be set only when a channel fails to complete its teardown procedure normally because a peripheral is no longer functioning or because data flow was halted on a boundary that is not compatible with the static TR configuration.
27-3	RESERVED	R	0h	Reserved
2	ERROR	R/W	0h	When set, the channel has encountered a PSI-L protocol violation. The ERROR bit can only be set by hardware and can only be cleared by software. Once this bit is set, the channel should be fully reset and re-initialized via the PSI-L pairing registers.
1	IDLE	R	0h	This is a read-only bit that signifies that the disabled thread is also idle. This bit is read only and can only become set if the ENABLE bit is cleared.
0	FREE	R/W	0h	When cleared, the channel honors the debug suspend signal. When set, the channel will 'free run', regardless of the value of debug suspend.

14.7.6.3 PDMA PSI-L RX Configuration Registers

Table 14-11548 lists the PDMA PSI-L RX configuration registers (PDMA_PSILCFG_RX). These registers are not memory mapped and are accessed indirectly via CFG_PROXY modules in DMSS.

Table 14-17247. PDMA_PSILCFG_RX Instances

Instance	Base Address
PDMA_PSILCFG_RX	N/A

Table 14-17248. PDMA_PSILCFG_RX Registers

Offset	Acronym	Register Name	PDMA_PSILCFG_RX Physical Address
0h	PDMA_PSILCFG_RX_PEER_THREAD_ID	RX peer thread ID register	N/A
1h	PDMA_PSILCFG_RX_PEER_CREDIT	RX peer credit register	N/A
2h	PDMA_PSILCFG_RX_ENABLE	RX enable register	N/A
400h	PDMA_PSILCFG_RX_STATIC_TR	RX static transfer request (X, Y) register	N/A
401h	PDMA_PSILCFG_RX_STATIC_TR_Z	RX static transfer request (Z) register	N/A
402h	PDMA_PSILCFG_RX_DEBUG_1	RX debug/state register 1	N/A
403h	PDMA_PSILCFG_RX_DEBUG_2	RX debug/state register 2	N/A
404h	PDMA_PSILCFG_RX_BYTE_COUNT	RX byte count register	N/A
405h	PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG	RX AASRC Rx FIFO configuration register	N/A
406h	PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0	RX AASRC Rx order table 0	N/A
407h	PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1	RX AASRC Rx order table 1	N/A
408h	PDMA_PSILCFG_RX_RT_ENABLE	RX real-time enable register	N/A
40Fh	PDMA_PSILCFG_RX_DEBUG_3	RX debug/state register 3	N/A

1 PDMA_PSILCFG_RX_PEER_THREAD_ID Register (Offset = 0h) [reset = 0h]

PDMA_PSILCFG_RX_PEER_THREAD_ID is shown in Figure 14-5701 and described in Table 14-11550.

Return to Summary Table.

Peer Thread ID Register. This register contains the thread ID of the thread destination which is used for routing the messages. This register is only implemented for source threads.

Table 14-17249. PDMA_PSILCFG_RX_PEER_THREAD_ID Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5701. PDMA_PSILCFG_RX_PEER_THREAD_ID

31	30	29	28	27	26	25	24
THREAD_PRIORITY			PEER_THREAD_WIDTH				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
PEER_THREAD_ID							
R/W-0h							
7	6	5	4	3	2	1	0
PEER_THREAD_ID							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17251. PDMA_PSILCFG_RX_PEER_THREAD_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	THREAD_PRIORITY	R	0h	Priority level to use for this source thread in arbitration. This field is hard coded to 0h and is not writable
28-24	PEER_THREAD_WIDTH	R/W	0h	Datapath width of paired peer destination thread. This field is encoded as follows: 0h = 32-bit 1h = 64-bit 2h = 128-bit 3h = 256-bit 4h = 512-bit
23-16	RESERVED	R	0h	Reserved
15-0	PEER_THREAD_ID	R/W	0h	Thread ID to which all nontransfer response, nonconfiguration messages from this thread are sent

2 PDMA_PSILCFG_RX_PEER_CREDIT Register (Offset = 1h) [reset = 0h]

PDMA_PSILCFG_RX_PEER_CREDIT is shown in Figure 14-5702 and described in Table 14-11552.

Return to Summary Table.

Peer Credit Register. This register contains a free credit count in completed destination data phases for the thread destination. This register is only implemented for source threads.

Table 14-17252. PDMA_PSILCFG_RX_PEER_CREDIT Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5702. PDMA_PSILCFG_RX_PEER_CREDIT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CREDIT_CNT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17254. PDMA_PSILCFG_RX_PEER_CREDIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	CREDIT_CNT	R/W	0h	Free entries in destination thread. This field is encoded as follows: 0h to 80h = Actual count in data phases 81h to FFh = Reserved

3 PDMA_PSILCFG_RX_ENABLE Register (Offset = 2h) [reset = 0h]

PDMA_PSILCFG_RX_ENABLE is shown in Figure 14-5703 and described in Table 14-11554.

Return to Summary Table.

Enable Register. This register contains enable control for the thread.

Table 14-17255. PDMA_PSILCFG_RX_ENABLE Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5703. PDMA_PSILCFG_RX_ENABLE Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17257. PDMA_PSILCFG_RX_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	When set, the RX channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all credit returns, and will not generate egress data. A one-to-zero transition on this bit fully resets the channel.
30-0	RESERVED	R	0h	Reserved

4 PDMA_PSILCFG_RX_STATIC_TR Register (Offset = 400h) [reset = 0h]

PDMA_PSILCFG_RX_STATIC_TR is shown in Figure 14-5704 and described in Table 14-11556.

Return to Summary Table.

Static Transfer Request (X, Y) Register. This register is used to define the 'X' and 'Y' parameters in a static TR.

Table 14-17258. PDMA_PSILCFG_RX_STATIC_TR Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5704. PDMA_PSILCFG_RX_STATIC_TR Register

31	30	29	28	27	26	25	24
BURST	ACC32	RESERVED			X		
R/W-0h	R/W-0h	R-0h			R/W-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				Y			
R-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17260. PDMA_PSILCFG_RX_STATIC_TR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BURST	R/W	0h	**X-Y FIFO mode static TR:** When set, enables VBUSP burst mode on this channel. See the XY burst description for more information. **MCAN mode static TR:** When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information. **AASRC mode static TR:** Not used.
30	ACC32	R/W	0h	**X-Y FIFO mode static TR:** When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide. **MCAN mode static TR:** Not used.

Table 14-17260. PDMA_PSILCFG_RX_STATIC_TR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				AASRC mode static TR: When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
29-27	RESERVED	R	0h	Reserved
26-24	X	R/W	0h	**X-Y FIFO mode static TR:** Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0h = 8 bits; 1h =16 bits; 2h = 24 bits; 3h = 32 bits; 4h = 64 bits; 5h-7h = RESERVED. **MCAN mode static TR:** Not used. **AASRC mode static TR:** Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0h = 8 bits; 1h =16 bits; 2h = 24 bits; 3h = 32 bits; 4h = 64 bits; 5h-7h = RESERVED.
23-12	RESERVED	R	0h	Reserved
11-0	Y	R/W	0h	**X-Y FIFO mode static TR:** Element count. This field specifies how many elements to transfer each time a trigger is received on the channel. **MCAN mode static TR:** Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72. **AASRC mode static TR:** FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.

5 PDMA_PSILCFG_RX_STATIC_TR_Z Register (Offset = 401h) [reset = 0h]

PDMA_PSILCFG_RX_STATIC_TR_Z is shown in Figure 14-5705 and described in Table 14-11558.

Return to Summary Table.

Static Transfer Request (Z) Register. This register is used to define the 'Z' parameter in a static TR.

Table 14-17261. PDMA_PSILCFG_RX_STATIC_TR_Z Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5705. PDMA_PSILCFG_RX_STATIC_TR_Z Register

31	30	29	28	27	26	25	24
EOL	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
Z							
R-0h							
15	14	13	12	11	10	9	8
Z				Z			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
Z							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17263. PDMA_PSILCFG_RX_STATIC_TR_Z Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EOL	R/W	0h	EOL mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
30-24	RESERVED	R	0h	Reserved
23-0	Z	R/W	0h	**X-Y FIFO mode static TR:** FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an EOP indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the paired-DMA TR.
				MCAN mode static TR: Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an EOP indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8-byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

Table 14-17263. PDMA_PSILCFG_RX_STATIC_TR_Z Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				AASRC mode static TR: FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an EOP indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the paired-DMA TR.

6 PDMA_PSILCFG_RX_DEBUG_1 Register (Offset = 402h) [reset = 0h]

PDMA_PSILCFG_RX_DEBUG_1 is shown in Figure 14-5706 and described in Table 14-11560.

Return to Summary Table.

Debug/State Register 1. The debug/state registers give software applications additional information about the PDMA than they would need in regular opteration, but which may be useful in debug situations.

Table 14-17264. PDMA_PSILCFG_RX_DEBUG_1 Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5706. PDMA_PSILCFG_RX_DEBUG_1 Register

31	30	29	28	27	26	25	24
Z							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Z							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Y							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17266. PDMA_PSILCFG_RX_DEBUG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Z	R/W	0h	This field holds the lower 12 bits of the current Z count for legacy pursposes. See PDMA_PSILCFG_RX_DEBUG_3 Register (Offset = 40Fh) [reset = 0h] for the full width version of the Z count field. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.
15-0	Y	R/W	0h	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.

7 PDMA_PSILCFG_RX_DEBUG_2 Register (Offset = 403h) [reset = 0h]

PDMA_PSILCFG_RX_DEBUG_2 is shown in Figure 14-5707 and described in Table 14-11562.

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Debug/State Register 2. The debug/state registers give software applications additional information about the PDMA than they would need in regular opteration, but which may be useful in debug situations.

Table 14-17267. PDMA_PSILCFG_RX_DEBUG_2 Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5707. PDMA_PSILCFG_RX_DEBUG_2 Register

31	30	29	28	27	26	25	24
INEVENT	TDOWN	PAUSE	SPACE	XSPACE	BUFFER	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STATE				EVENTCNT			
R/W-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17269. PDMA_PSILCFG_RX_DEBUG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INEVENT	R/W	0h	When set, the PDMA is in the middle of processing a FIFO event.
30	TDOWN	R/W	0h	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the paired-DMA and its full completion status can be checked there.
29	PAUSE	R/W	0h	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is unpaused or disabled.
28	SPACE	R/W	0h	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
27	XSPACE	R/W	0h	When set, there is enough internal FIFO space available to start servicing a peripheral DMA event.
26	BUFFER	R/W	0h	This is the current RX buffer (0/1) for the current MCAN receive operation.
25-24	RESERVED	R	0h	Reserved

Table 14-17269. PDMA_PSILCFG_RX_DEBUG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-20	STATE	R/W	0h	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
19-16	EVENTCNT	R/W	0h	This field holds the number of backlogged DMA events yet to be serviced.
15-0	RESERVED	R	0h	Reserved

8 PDMA_PSILCFG_RX_BYTE_COUNT Register (Offset = 404h) [reset = 0h]

PDMA_PSILCFG_RX_BYTE_COUNT is shown in Figure 14-5708 and described in Table 14-11564.

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Byte Count Register. This register contains the number of bytes that have been written to the VBUSP mapped peripheral.

Table 14-17270. PDMA_PSILCFG_RX_BYTE_COUNT Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5708. PDMA_PSILCFG_RX_BYTE_COUNT Register

31	30	29	28	27	26	25	24
BYTES							
R/W-0h							

23	22	21	20	19	18	17	16
BYTES							
R/W-0h							

15	14	13	12	11	10	9	8
BYTES							
R/W-0h							

7	6	5	4	3	2	1	0
BYTES							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17272. PDMA_PSILCFG_RX_BYTE_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BYTES	R/W	0h	This register contains the number of bytes that have been read from the VBUSP mapped peripheral. The register is write-to-decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

9 PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Register (Offset = 405h) [reset = 0h]

PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG is shown in Figure 14-5709 and described in Table 14-11566.

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AASRC Rx FIFO configuration register.

Table 14-17273. PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5709. PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Register

31	30	29	28	27	26	25	24
GROUPMODE	DMAREQRESET	RESERVED					
R/W-0h	R/W-0h	R-0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LASTSLOT				FIRSTSLOT			
R/W-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAREQMASK							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DMAREQMASK							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17275. PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GROUPMODE	R/W	0h	When set, the channel is in 'group mode'. It will look for group mode DMA requests, and access the group mode FIFOs. When clear, the channel is 'stream mode'. It will look for stream FIFO DMA requests, and access the stream mode FIFOs.
30	DMAREQRESET	R/W	0h	When set, resets any latched DMA request using the DMAREQMASK. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
29-24	RESERVED	R	0h	Reserved
23-20	LASTSLOT	R/W	0h	This is the index (0-15) of the last slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.

Table 14-17275. PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	FIRSTSLOT	R/W	0h	This is the index (0-15) of the first slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
15-0	DMAREQMASK	R/W	0h	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In steam mode, these 16 flags correspond to the 16 DMA requests for each RX FIFO. The flags corresponding to all RX FIFOs involved with the channel should be set to 1. In group mode, these flags indicate which group mode DMA requests must fire. In this case, only bits [3:0] are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

10 PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 Register (Offset = 406h) [reset = 0h]

PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 is shown in Figure 14-5710 and described in Table 14-11568.

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AASRC RX order table 0 register.

Table 14-17276. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5710. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 Register

31	30	29	28	27	26	25	24
ENTRY7				ENTRY6			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
ENTRY5				ENTRY4			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
ENTRY3				ENTRY2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ENTRY1				ENTRY0			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17278. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ENTRY7	R/W	7h	RX FIFO index for slot 7
27-24	ENTRY6	R/W	6h	RX FIFO index for slot 6
23-20	ENTRY5	R/W	5h	RX FIFO index for slot 5
19-16	ENTRY4	R/W	4h	RX FIFO index for slot 4
15-12	ENTRY3	R/W	3h	RX FIFO index for slot 3
11-8	ENTRY2	R/W	2h	RX FIFO index for slot 2
7-4	ENTRY1	R/W	1h	RX FIFO index for slot 1
3-0	ENTRY0	R/W	0h	RX FIFO index for slot 0

11 PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 Register (Offset = 407h) [reset = 0h]

PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 is shown in Figure 14-5711 and described in Table 14-11570.

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AASRC RX order table 1 register.

Table 14-17279. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5711. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 Register

31	30	29	28	27	26	25	24
ENTRY15				ENTRY14			
R/W-0h				R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ENTRY13				ENTRY12			
R/W-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENTRY11				ENTRY10			
R/W-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ENTRY9				ENTRY8			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17281. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ENTRY15	R/W	Fh	RX FIFO index for slot 15
27-24	ENTRY14	R/W	Eh	RX FIFO index for slot 14
23-20	ENTRY13	R/W	Dh	RX FIFO index for slot 13
19-16	ENTRY12	R/W	Ch	RX FIFO index for slot 12
15-12	ENTRY11	R/W	Bh	RX FIFO index for slot 11
11-8	ENTRY10	R/W	Ah	RX FIFO index for slot 10
7-4	ENTRY9	R/W	9h	RX FIFO index for slot 9
3-0	ENTRY8	R/W	8h	RX FIFO index for slot 8

12 PDMA_PSILCFG_RX_RT_ENABLE Register (Offset = 408h) [reset = 0h]

PDMA_PSILCFG_RX_RT_ENABLE is shown in Figure 14-5712 and described in Figure 14-5712.

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Real Time Enable Register. This register allows enabling various channel settings in real time.

Table 14-17282. PDMA_PSILCFG_RX_RT_ENABLE Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5712. PDMA_PSILCFG_RX_RT_ENABLE Register

31	30	29	28	27	26	25	24
ENABLE	TDOWN	PAUSE	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R-0h				
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						IDLE	FREE
R-0h						R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17284. PDMA_PSILCFG_RX_RT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	When set, the RX channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all DMA events from the peripheral. It maintains proper data transfers with the paired-DMA such that the credit handshake is not disrupted. However, unlike teardown, it does not close out the current open packet. Thus the TDOWN bit should always be used to disable an RX channel instead of manually clearing this bit. Failing to use teardown may result in stale data remaining in the internal RX FIFO, which would also prevent the channel from going idle without a channel reset. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.
30	TDOWN	R/W	0h	When set, the channel will commence a RX channel teardown procedure. It will stop on the next FIFO boundary. It then clears the DMA event count and ignores all future DMA events from the peripheral. After stopping peripheral reads, the PDMA sends a teardown message to the paired-DMA that also closes the current packet with an EOP. If no packet is open at the time of the teardown, the message also includes SOP. The EOP teardown message may or may not contain final packet data. Once the channel teardown is complete and ready to be reused, the ENABLE bit is cleared.

Table 14-17284. PDMA_PSILCFG_RX_RT_ENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	PAUSE	R/W	0h	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals but will not act on them. The PAUSE bit can be cleared and data will resume. Pause will not stop teardown from completing.
28-2	RESERVED	R	0h	Reserved
1	IDLE	R	0h	This is a read-only bit that signifies that the paused or disabled channel is also idle. It can only become set if PAUSE is set or ENABLE is cleared.
0	FREE	R/W	0h	When cleared, the channel honors the debug suspend signal. When set, the channel will 'free run', regardless of the value of debug suspend.

13 PDMA_PSILCFG_RX_DEBUG_3 Register (Offset = 40Fh) [reset = 0h]

PDMA_PSILCFG_RX_DEBUG_3 is shown in Figure 14-5713 and described in Table 14-11574.

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Debug/State Register 3. The debug/state registers give software applications additional information about the PDMA than they would need in regular opteration, but which may be useful in debug situations.

Table 14-17285. PDMA_PSILCFG_RX_DEBUG_3 Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 14-5713. PDMA_PSILCFG_RX_DEBUG_3 Register

31	30	29	28	27	26	25	24
Z							
R/W-0h							
23	22	21	20	19	18	17	16
Z							
R/W-0h							
15	14	13	12	11	10	9	8
Z							
R/W-0h							
7	6	5	4	3	2	1	0
Z							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17287. PDMA_PSILCFG_RX_DEBUG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z	R/W	0h	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

14.8 Time Sync Registers

14.8.1 CPTS Registers

Table 14-11576 lists the memory-mapped registers for the CPTS. All register offset addresses not listed in Table 14-11576 should be considered as reserved locations and the register contents should not be modified.

Table 14-17288. CPTS Instances

Instance	Base Address
CPTS0	3900 0000h

Table 14-17289. NAVSS0_CPTS Registers

Offset	Acronym	Register Name	CPTS0 Physical Address
0h	CPTS_IDVER_REG	Identification and Version	3900 0000h
4h	CPTS_CONTROL_REG	Time Sync Control	3900 0004h
8h	CPTS_RFTCLK_SEL_REG	RFTCLK Select	3900 0008h
Ch	CPTS_TS_PUSH_REG	Time Stamp Event Push	3900 000Ch
10h	CPTS_TS_LOAD_VAL_REG	Time Stamp Load Low Value	3900 0010h
14h	CPTS_TS_LOAD_EN_REG	Time Stamp Load Enable	3900 0014h
18h	CPTS_TS_COMP_VAL_REG	Time Stamp Comparison Low Value	3900 0018h
1Ch	CPTS_TS_COMP_LEN_REG	Time Stamp Comparison Length	3900 001Ch
20h	CPTS_INTSTAT_RAW_REG	Interrupt Status Register Raw	3900 0020h
24h	CPTS_INTSTAT_MASKED_REG	Interrupt Status Register Masked	3900 0024h
28h	CPTS_INT_ENABLE_REG	Interrupt Enable Register	3900 0028h
2Ch	CPTS_TS_COMP_NUDGE_REG	Time Stamp Comparison Nudge	3900 002Ch
30h	CPTS_EVENT_POP_REG	Event Pop	3900 0030h
34h	CPTS_EVENT_0_REG	Event Register 0	3900 0034h
38h	CPTS_EVENT_1_REG	Event Register 1	3900 0038h
3Ch	CPTS_EVENT_2_REG	Event Register 2	3900 003Ch
40h	CPTS_EVENT_3_REG	Event Register 3	3900 0040h
44h	CPTS_TS_LOAD_HIGH_VAL_REG	Time Stamp Load High Value	3900 0044h
48h	CPTS_TS_COMP_HIGH_VAL_REG	Time Stamp Comparison High Value	3900 0048h
4Ch	CPTS_TS_ADD_VAL_REG	Time Stamp Add Value	3900 004Ch
50h	CPTS_TS_PPM_LOW_VAL_REG	Time Stamp PPM Low Value	3900 0050h
54h	CPTS_TS_PPM_HIGH_VAL_REG	Time Stamp PPM High Value	3900 0054h
58h	CPTS_TS_NUDGE_VAL_REG	Time Stamp Nudge Value	3900 0058h
D0h	CPTS_TS_CONFIG_REG	Time Stamp Configuration Read	3900 00D0h
E0h + formula	CPTS_TS_GENF_COMP_LOW_REG_j	Time Stamp Generate Function j Comparison Low Value	3900 00E0h + formula
E4h + formula	CPTS_TS_GENF_COMP_HIGH_REG_j	Time Stamp Generate Function j Comparison high Value	3900 00E4h + formula
E8h + formula	CPTS_TS_GENF_CONTROL_REG_j	Time Stamp Generate Function j Control	3900 00E8h + formula
ECh + formula	CPTS_TS_GENF_LENGTH_REG_j	Time Stamp Generate Function j Length Value	3900 00ECh + formula
F0h + formula	CPTS_TS_GENF_PPM_LOW_REG_j	Time Stamp Generate Function j PPM Low Value	3900 00F0h + formula
F4h + formula	CPTS_TS_GENF_PPM_HIGH_REG_j	Time Stamp Generate Function j PPM High Value	3900 00F4h + formula
F8h + formula	CPTS_TS_GENF_NUDGE_REG_j	Time Stamp Generate Function j Nudge Value	3900 00F8h + formula
200h	CPTS_TS_ESTF_COMP_LOW_REG	Time Stamp ESTF Generate Function Comparison Low Value	3900 0200h
204h	CPTS_TS_ESTF_COMP_HIGH_REG	Time Stamp ESTF Generate Function Comparison high Value	3900 0204h

Table 14-17289. NAVSS0_CPTS Registers (continued)

Offset	Acronym	Register Name	CPTS0 Physical Address
208h	CPTS_TS_ESTF_CONTROL_REG	Time Stamp ESTF Generate Function Control	3900 0208h
20Ch	CPTS_TS_ESTF_LENGTH_REG	Time Stamp ESTF Generate Function Length Value	3900 020Ch
210h	CPTS_TS_ESTF_PPM_LOW_REG	Time Stamp ESTF Generate Function PPM Low Value	3900 0210h
214h	CPTS_TS_ESTF_PPM_HIGH_REG	Time Stamp ESTF Generate Function PPM High Value	3900 0214h
218h	CPTS_TS_ESTF_NUDGE_REG	Time Stamp ESTF Generate Function Nudge Value	3900 0218h

1 CPTS_IDVER_REG Register (Offset = 0h) [reset = X]

CPTS_IDVER_REG is shown in Figure 14-5714 and described in Table 14-11578.

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Identification and Version Register

Table 14-17290. CPTS_IDVER_REG Instances

Instance	Physical Address
CPTS0	3900 0000h

Figure 14-5714. CPTS_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R-4E8Ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
R-1h								R-Ch							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17292. CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_IDENT	R	4E8Ah	Identification value
15-11	RTL_VER	R		RTL version value
10-8	MAJOR_VER	R	1h	Major version value
7-0	MINOR_VER	R	R-Ch	Minor version value

2 CPTS_CONTROL_REG Register (Offset = 4h) [reset = X]

CPTS_CONTROL_REG is shown in Figure 14-5715 and described in Table 14-11580.

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Time Sync Control Register

Table 14-17293. CPTS_CONTROL_REG Instances

Instance	Physical Address
CPTS0	3900 0004h

Figure 14-5715. CPTS_CONTROL_REG Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED						TX_GENF_CLR_EN	TS_RX_NO_EVENT
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
HW8_TS_PUSH_EN	HW7_TS_PUSH_EN	HW6_TS_PUSH_EN	HW5_TS_PUSH_EN	HW4_TS_PUSH_EN	HW3_TS_PUSH_EN	HW2_TS_PUSH_EN	HW1_TS_PUSH_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TS_PPM_DIR	TS_COMP_TOG	MODE	SEQUENCE_EN	TSTAMP_EN	TS_COMP_POLARITY	INT_TEST	CPTS_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17295. CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TS_SYNC_SEL	R/W	0h	TS_SYNC output timestamp counter bit select 0000 – TS_SYNC disabled 0001 0001..1111 - TS_SYNC is timestamp counter bits 31 (1111) down to 17 (0001)
27-18	RESERVED	R/W	X	
17	TX_GENF_CLR_EN	R/W	0h	GENF (and ESTF) Clear Enable. 0 - A TS_GENFn output is not cleared when the associated CPTS_TS_GENF_LENGTH_REG_j[31:0] LENGTH field is cleared to zero. 1 - A TS_GENFn output is cleared when the associated CPTS_TS_GENF_LENGTH_REG_j[31:0] LENGTH field is cleared to zero.
16	TS_RX_NO_EVENT	R/W	0h	Timestamp Ethernet Receive produces no events. 0 - Ethernet receive timesync events enabled 1 - Ethernet receive timesync events disabled
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable

Table 14-17295. CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable
7	TS_PPM_DIR	R/W	0h	Timestamp PPM Direction 0 – Increase the time_stamp[63:0] value by the PPM value 1 – Decrease the time_stamp[63:0] value by the PPM value
6	TS_COMP_TOG	R/W	0h	Timestamp Compare Toggle mode: 0=TS_COMP is in non-toggle mode 1=TS_COMP is in toggle mode
5	MODE	R/W	0h	Timestamp mode 0 – The timestamp is 32-bits with the upper 32-bits forced to zero. 1 – The timestamp is 64-bits.
4	SEQUENCE_EN	R/W	0h	Sequence Enable 0 – The timestamp value increments with the selected RFTCLK 1 - The timestamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc).
3	TSTAMP_EN	R/W	0h	Host Receive Timestamp Enable 0 – Timestamps are disabled on received packets to host 1 – Timestamps enabled on received packets to host (cpts_en must be set)
2	TS_COMP_POLARITY	R/W	1h	TS_COMP polarity 0 – TS_COMP is asserted low 1 – TS_COMP is asserted high
1	INT_TEST	R/W	0h	Interrupt test When set, this bit allows the raw interrupt to be written to facilitate interrupt test.
0	CPTS_EN	R/W	0h	Time sync enable When disabled (cleared to zero), the RCLK domain is held in reset.

3 CPTS_RFTCLK_SEL_REG Register (Offset = 8h) [reset = X]

CPTS_RFTCLK_SEL_REG is shown in Figure 14-5716 and described in Table 14-11582.

Return to Summary Table.

RFTCLK Select Register

Table 14-17296. CPTS_RFTCLK_SEL_REG Instances

Instance	Physical Address
CPTS0	3900 0008h

Figure 14-5716. CPTS_RFTCLK_SEL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											RFTCLK_SEL				
R/W-X											R/W-0h				

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17298. CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	RFTCLK_SEL	R/W	0h	Reference clock select. Not Used. See CTRLMMR_CPTS_CLKSEL[2-0] CPTS_CLKSEL_CPTS_CLKSEL instead.

4 CPTS_TS_PUSH_REG Register (Offset = Ch) [reset = X]

CPTS_TS_PUSH_REG is shown in Figure 14-5717 and described in Table 14-11584.

Return to Summary Table.

Time Stamp Event Push Register

Table 14-17299. CPTS_TS_PUSH_REG Instances

Instance	Physical Address
CPTS0	3900 000Ch

Figure 14-5717. CPTS_TS_PUSH_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							

23	22	21	20	19	18	17	16
RESERVED							
W-X							

15	14	13	12	11	10	9	8
RESERVED							
W-X							

7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
W-X							W-0h

LEGEND: W = Write Only; -*n* = value after reset

Table 14-17301. CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_PUSH	W	0h	Time stamp event push When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time).

5 CPTS_TS_LOAD_VAL_REG Register (Offset = 10h) [reset = 0h]

CPTS_TS_LOAD_VAL_REG is shown in Figure 14-5718 and described in Table 14-11586.

Return to Summary Table.

Time Stamp Load Low Value Register

Table 14-17302. CPTS_TS_LOAD_VAL_REG Instances

Instance	Physical Address
CPTS0	3900 0010h

Figure 14-5718. CPTS_TS_LOAD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17304. CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	Time stamp load low value Writing the ts_load_en bit causes ts_load[63:0] to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register.

6 CPTS_TS_LOAD_EN_REG Register (Offset = 14h) [reset = X]

CPTS_TS_LOAD_EN_REG is shown in Figure 14-5719 and described in Table 14-11588.

Return to Summary Table.

Time Stamp Load Enable Register

Table 14-17305. CPTS_TS_LOAD_EN_REG Instances

Instance	Physical Address
CPTS0	3900 0014h

Figure 14-5719. CPTS_TS_LOAD_EN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
W-X							W-0h

LEGEND: W = Write Only; -*n* = value after reset

Table 14-17307. CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_LOAD_EN	W	0h	Time stamp load enable Writing a one to this bit enables the time stamp value to be written with the value in ts_load[63:0]. This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the timestamp are forced to zero in 32-bit mode.

7 CPTS_TS_COMP_VAL_REG Register (Offset = 18h) [reset = 0h]

CPTS_TS_COMP_VAL_REG is shown in Figure 14-5720 and described in Table 14-11590.

Return to Summary Table.

Time Stamp Comparison Low Value Register

Table 14-17308. CPTS_TS_COMP_VAL_REG Instances

Instance	Physical Address
CPTS0	3900 0018h

Figure 14-5720. CPTS_TS_COMP_VAL_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TS_COMP_VAL</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17310. CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_VAL	R/W	0h	Time stamp comparison low value Writing a non-zero value to the TS_Comp_Length[31:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val.

8 CPTS_TS_COMP_LEN_REG Register (Offset = 1Ch) [reset = 0h]

CPTS_TS_COMP_LEN_REG is shown in Figure 14-5721 and described in Table 14-11592.

Return to Summary Table.

Time Stamp Comparison Length Register

Table 14-17311. CPTS_TS_COMP_LEN_REG Instances

Instance	Physical Address
CPTS0	3900 001Ch

Figure 14-5721. CPTS_TS_COMP_LEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17313. CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_LENGTH	R/W	0h	Time stamp comparison length Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the TS_Comp_Low and TS_Comp_High registers are written.

9 CPTS_INTSTAT_RAW_REG Register (Offset = 20h) [reset = X]

CPTS_INTSTAT_RAW_REG is shown in Figure 14-5722 and described in Table 14-11594.

Return to Summary Table.

Interrupt Status Register Raw

Table 14-17314. CPTS_INTSTAT_RAW_REG Instances

Instance	Physical Address
CPTS0	3900 0020h

Figure 14-5722. CPTS_INTSTAT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TS_PEND_RAW
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17316. CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable) Writable when int_test = 1. A one in this bit indicates that there are one or more events in the event FIFO.

10 CPTS_INTSTAT_MASKED_REG Register (Offset = 24h) [reset = X]

CPTS_INTSTAT_MASKED_REG is shown in Figure 14-5723 and described in Table 14-11596.

Return to Summary Table.

Interrupt Status Register Masked

Table 14-17317. CPTS_INTSTAT_MASKED_REG Instances

Instance	Physical Address
CPTS0	3900 0024h

Figure 14-5723. CPTS_INTSTAT_MASKED_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TS_PEND</td></tr>
<tr><td colspan="7">R-X</td><td>R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17319. CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

11 CPTS_INT_ENABLE_REG Register (Offset = 28h) [reset = X]

CPTS_INT_ENABLE_REG is shown in Figure 14-5724 and described in Table 14-11598.

Return to Summary Table.

Interrupt Enable Register

Table 14-17320. CPTS_INT_ENABLE_REG Instances

Instance	Physical Address
CPTS0	3900 0028h

Figure 14-5724. CPTS_INT_ENABLE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17322. CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

12 CPTS_TS_COMP_NUDGE_REG Register (Offset = 2Ch) [reset = X]

CPTS_TS_COMP_NUDGE_REG is shown in Figure 14-5725 and described in Table 14-11600.

Return to Summary Table.

Time Stamp Comparison Nudge Register

Table 14-17323. CPTS_TS_COMP_NUDGE_REG Instances

Instance	Physical Address
CPTS0	3900 002Ch

Figure 14-5725. CPTS_TS_COMP_NUDGE_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">NUDGE</td></tr>
<tr><td colspan="24">R/W-X</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17325. CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	This 2s complement number is added to the ts_comp_length value to increase or decrease the TS_COMP length by the nudge amount Only a single high or low time is adjusted and the ts_comp_nudge value is cleared to zero when the nudge has occurred.

13 CPTS_EVENT_POP_REG Register (Offset = 30h) [reset = X]

CPTS_EVENT_POP_REG is shown in Figure 14-5726 and described in Table 14-11602.

Return to Summary Table.

Event Pop Register

Table 14-17326. CPTS_EVENT_POP_REG Instances

Instance	Physical Address
CPTS0	3900 0030h

Figure 14-5726. CPTS_EVENT_POP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
W-X							W-0h

LEGEND: W = Write Only; -*n* = value after reset

Table 14-17328. CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	EVENT_POP	W	0h	Event pop When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read from the Event_0-3 registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.

14 CPTS_EVENT_0_REG Register (Offset = 34h) [reset = 0h]

CPTS_EVENT_0_REG is shown in Figure 14-5727 and described in Table 14-11604.

Return to Summary Table.

Event 0 Register

Table 14-17329. CPTS_EVENT_0_REG Instances

Instance	Physical Address
CPTS0	3900 0034h

Figure 14-5727. CPTS_EVENT_0_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TIME_STAMP</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17331. CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp The timestamp is valid for transmit, receive, and time stamp push event types. The timestamp value is not valid for counter roll event types.

15 CPTS_EVENT_1_REG Register (Offset = 38h) [reset = X]

CPTS_EVENT_1_REG is shown in Figure 14-5728 and described in Table 14-11606.

Return to Summary Table.

Event 1 Register

Table 14-17332. CPTS_EVENT_1_REG Instances

Instance	Physical Address
CPTS0	3900 0038h

Figure 14-5728. CPTS_EVENT_1_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td>PREMPT_QUEUE</td><td colspan="5">PORT_NUMBER</td></tr>
<tr><td colspan="2">R-X</td><td>R-0h</td><td colspan="5">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">EVENT_TYPE</td><td colspan="4">MESSAGE_TYPE</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SEQUENCE_ID</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SEQUENCE_ID</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17334. CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29	PREMPT_QUEUE	R	0h	Prempt QUEUE 0 – The packet was received/transmitted on the express queue. 1 – The packet was received/transmitted on the prempt queue.
28-24	PORT_NUMBER	R	0h	Port number indicates the port number (encoded) of an Ethernet event or the encoded hardware timestamp number.
23-20	EVENT_TYPE	R	0h	Event type 0000 – Time Stamp Push Event 0001 – Time Stamp Rollover Event 0010 – Time Stamp Half Rollover Event 0011 – Hardware Time Stamp Push Event 0100 – Ethernet Receive Event 0101 – Ethernet Transmit Event 0110 – Time Stamp Compare Event 0111 – Host Transmit Event 1000 1111 reserved
19-16	MESSAGE_TYPE	R	0h	Message type The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

Table 14-17334. CPTS_EVENT_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	SEQUENCE_ID	R	0h	Sequence ID The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

16 CPTS_EVENT_2_REG Register (Offset = 3Ch) [reset = X]

CPTS_EVENT_2_REG is shown in Figure 14-5729 and described in Table 14-11608.

Return to Summary Table.

Event 2 Register

Table 14-17335. CPTS_EVENT_2_REG Instances

Instance	Physical Address
CPTS0	3900 003Ch

Figure 14-5729. CPTS_EVENT_2_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">DOMAIN</td></tr>
<tr><td colspan="24">R-X</td><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17337. CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	DOMAIN	R	0h	Domain The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

17 CPTS_EVENT_3_REG Register (Offset = 40h) [reset = 0h]

CPTS_EVENT_3_REG is shown in Figure 14-5730 and described in Table 14-11610.

Return to Summary Table.

Event 3 Register

Table 14-17338. CPTS_EVENT_3_REG Instances

Instance	Physical Address
CPTS0	3900 0040h

Figure 14-5730. CPTS_EVENT_3_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TIME_STAMP</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17340. CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp The timestamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode.

18 CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 44h) [reset = 0h]

CPTS_TS_LOAD_HIGH_VAL_REG is shown in Figure 14-5731 and described in Table 14-11612.

Return to Summary Table.

Time Stamp Load High Value Register

Table 14-17341. CPTS_TS_LOAD_HIGH_VAL_REG Instances

Instance	Physical Address
CPTS0	3900 0044h

Figure 14-5731. CPTS_TS_LOAD_HIGH_VAL_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TS_LOAD_VAL</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17343. CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	Time stamp load high value Writing the ts_load_en bit causes the value contained in this register (and the ts_load[63:0]) to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode

19 CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 48h) [reset = 0h]

CPTS_TS_COMP_HIGH_VAL_REG is shown in Figure 14-5732 and described in Table 14-11614.

Return to Summary Table.

Time Stamp Comparison High Value Register

Table 14-17344. CPTS_TS_COMP_HIGH_VAL_REG Instances

Instance	Physical Address
CPTS0	3900 0048h

Figure 14-5732. CPTS_TS_COMP_HIGH_VAL_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">TS_COMP_HIGH_VAL</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17346. CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_HIGH_VAL	R/W	0h	Time stamp comparison high value Writing a non-zero value to the TS_Comp_Length[31:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val[63:0]. This value is unused in 32-bit mode. The upper 32-bits in this register should be written before the lower 32-bits in the TS_Comp_Low register.

20 CPTS_TS_ADD_VAL_REG Register (Offset = 4Ch) [reset = X]

CPTS_TS_ADD_VAL_REG is shown in Figure 14-5733 and described in Table 14-11616.

Return to Summary Table.

TS Add Value Register

Table 14-17347. CPTS_TS_ADD_VAL_REG Instances

Instance	Physical Address
CPTS0	3900 004Ch

Figure 14-5733. CPTS_TS_ADD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED													ADD_VAL		
R/W-X													R/W-0h		

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17349. CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	ADD_VAL	R/W	0h	Add Value Add Value is added to 1 to comprise the timestamp increment value. The timestamp increment value is added to the current timestamp (time_stamp[63:0]) on each RCLK. The timestamp increment value can be adjusted by nudge and ppm also. The ts_add_val[2:0] value may be non-zero in 64-bit mode only.

21 CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 50h) [reset = 0h]

CPTS_TS_PPM_LOW_VAL_REG is shown in Figure 14-5734 and described in Table 14-11618.

Return to Summary Table.

Time Stamp PPM Low Value Register

Table 14-17350. CPTS_TS_PPM_LOW_VAL_REG Instances

Instance	Physical Address
CPTS0	3900 0050h

Figure 14-5734. CPTS_TS_PPM_LOW_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17352. CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_PPM_LOW_VAL	R/W	0h	Time stamp PPM Low value The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen

22 CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 54h) [reset = X]

CPTS_TS_PPM_HIGH_VAL_REG is shown in Figure 14-5735 and described in Table 14-11620.

Return to Summary Table.

Time Stamp PPM High Value Register

Table 14-17353. CPTS_TS_PPM_HIGH_VAL_REG Instances

Instance	Physical Address
CPTS0	3900 0054h

Figure 14-5735. CPTS_TS_PPM_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TS_PPM_HIGH_VAL									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17355. CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TS_PPM_HIGH_VAL	R/W	0h	Time stamp PPM High value This value should be written first (before the low value is written). The minimum value of the ts_ppm is 0x400 (all 42 bits).

23 CPTS_TS_NUDGE_VAL_REG Register (Offset = 58h) [reset = X]

CPTS_TS_NUDGE_VAL_REG is shown in Figure 14-5736 and described in Table 14-11622.

Return to Summary Table.

Time Stamp Nudge Value Register

Table 14-17356. CPTS_TS_NUDGE_VAL_REG Instances

Instance	Physical Address
CPTS0	3900 0058h

Figure 14-5736. CPTS_TS_NUDGE_VAL_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">TS_NUDGE_VAL</td></tr>
<tr><td colspan="8">R/W-X</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17358. CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge value This two's complement number is added to the time_stamp[63:0] value to increase or decrease the timestamp value by the ts_nudge amount. The ts_nudge value is cleared to zero when the nudge has occurred.

24 CPTS_TS_CONFIG_REG Register (Offset = D0h) [reset = X]

CPTS_TS_CONFIG_REG is shown in Figure 14-5737 and described in Table 14-11624.

Return to Summary Table.

Time Stamp Configuration Read

Table 14-17359. CPTS_TS_CONFIG_REG Instances

Instance	Physical Address
CPTS0	3900 00D0h

Figure 14-5737. CPTS_TS_CONFIG_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EVNT_FIFO_DEPTH</td><td colspan="8">NUM_GENF</td></tr>
<tr><td colspan="8">R-20h</td><td colspan="8">R-6h</td></tr>
</table>

LEGEND: R = Read; -*n* = value after reset

Table 14-17361. CPTS_TS_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	EVNT_FIFO_DEPTH	R	20h	The event FIFO depth.
7-0	NUM_GENF	R	6h	The number of CPTS GENF outputs.

25 CPTS_TS_GENF_COMP_LOW_REG_j Register (Offset = E0h + formula) [reset = 0h]

CPTS_COMP_LOW_REG_j is shown in Figure 14-5738 and described in Table 14-11626.

Return to Summary Table.

Time Stamp Generate Function Comparison Low Value

Offset = E0h + (j * 20h); where j = 0h to 5h

Table 14-17362. CPTS_TS_GENF_COMP_LOW_REG_j Instances

Instance	Physical Address
CPTS0	3900 00E0h + formula

Figure 14-5738. CPTS_TS_GENF_COMP_LOW_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17364. CPTS_TS_GENF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value This value should be written after the upper 32-bits. The ts_GENFn_comp high and low should only be written when the ts_GENFn_length value is zero.

26 CPTS_TS_GENF_COMP_HIGH_REG_j Register (Offset = E4h + formula) [reset = 0h]

CPTS_COMP_HIGH_REG_j is shown in Figure 14-5739 and described in Table 14-11628.

Return to Summary Table.

Time Stamp Generate Function Comparison high Value

Offset = E4h + (j * 20h); where j = 0h to 5h

Table 14-17365.
CPTS_TS_GENF_COMP_HIGH_REG_j Instances

Instance	Physical Address
CPTS0	3900 00E4h + formula

Figure 14-5739. CPTS_TS_GENF_COMP_HIGH_REG_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">COMP_HIGH</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17367. CPTS_TS_GENF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value This value should be written before the lower 32-bits are written. The ts_GENFn_comp high and low should only be written when the ts_GENFn_length value is zero.

27 CPTS_TS_GENF_CONTROL_REG_j Register (Offset = E8h + formula) [reset = X]

CPTS_CONTROL_REG_j is shown in Figure 14-5740 and described in Table 14-11630.

Return to Summary Table.

Time Stamp Generate Function Control

Offset = E8h + (j * 20h); where j = 0h to 5h

Table 14-17368. CPTS_TS_GENF_CONTROL_REG_j Instances

Instance	Physical Address
CPTS0	3900 00E8h + formula

Figure 14-5740. CPTS_TS_GENF_CONTROL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PPM_DIR	POLARITY_INV
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17370. CPTS_TS_GENF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction 0 – A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1 – A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.
0	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert 0 – The output TS_GENFn signal asserts high 1 – The output TS_GENFn signal asserts low

28 CPTS_TS_GENF_LENGTH_REG_j Register (Offset = ECh + formula) [reset = 0h]

CPTS_LENGTH_REG_j is shown in Figure 14-5741 and described in Table 14-11632.

Return to Summary Table.

Time Stamp Generate Function Length Value

Offset = ECh + (j * 20h); where j = 0h to 5h

Table 14-17371. CPTS_TS_GENF_LENGTH_REG_j Instances

Instance	Physical Address
CPTS0	3900 00ECh + formula

Figure 14-5741. CPTS_TS_GENF_LENGTH_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17373. CPTS_TS_GENF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value The minimum value is decimal 5

29 CPTS_TS_GENF_PPM_LOW_REG_j Register (Offset = F0h + formula) [reset = 0h]

CPTS_PPM_LOW_REG_j is shown in Figure 14-5742 and described in Table 14-11634.

Return to Summary Table.

Time Stamp Generate Function PPM Low Value

Offset = F0h + (j * 20h); where j = 0h to 5h

Table 14-17374. CPTS_TS_GENF_PPM_LOW_REG_j Instances

Instance	Physical Address
CPTS0	3900 00F0h + formula

Figure 14-5742. CPTS_TS_GENF_PPM_LOW_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17376. CPTS_TS_GENF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp Generate Function PPM Low Value The 64-bit PPM value takes effect when this low value is written. The high value should be written first

30 CPTS_TS_GENF_PPM_HIGH_REG_j Register (Offset = F4h + formula) [reset = X]

CPTS_PPM_HIGH_REG_j is shown in Figure 14-5743 and described in Table 14-11636.

Return to Summary Table.

Time Stamp Generate Function PPM High Value

Offset = F4h + (j * 20h); where j = 0h to 5h

Table 14-17377. CPTS_TS_GENF_PPM_HIGH_REG_j Instances

Instance	Physical Address
CPTS0	3900 00F4h + formula

Figure 14-5743. CPTS_TS_GENF_PPM_HIGH_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						PPM_HIGH									
R/W-X																						R/W-0h									

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17379. CPTS_TS_GENF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value This value should be written first (before the low value is written).

31 CPTS_TS_GENF_NUDGE_REG_j Register (Offset = F8h + formula) [reset = X]

CPTS_NUDGE_REG_j is shown in Figure 14-5744 and described in Table 14-11638.

Return to Summary Table.

Time Stamp Generate Function Nudge Value

Offset = F8h + (j * 20h); where j = 0h to 5h

Table 14-17380. CPTS_TS_GENF_NUDGE_REG_j Instances

Instance	Physical Address
CPTS0	3900 00F8h + formula

Figure 14-5744. CPTS_TS_GENF_NUDGE_REG_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">NUDGE</td></tr>
<tr><td colspan="24">R/W-X</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17382. CPTS_TS_GENF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value This two's complement number is added to the generate counter value to increase or decrease the length by the ts_genfN_nudge amount. Only a single high or low time is adjusted and the ts_genfN_nudge value is cleared to zero when the nudge has occurred.

32 CPTS_TS_ESTF_COMP_LOW_REG Register (Offset = 200h) [reset = 0h]

CPTS_COMP_LOW_REG is shown in Figure 14-5745 and described in Table 14-11640.

Return to Summary Table.

Time Stamp ESTF Generate Function Comparison Low Value

Table 14-17383. CPTS_TS_ESTF_COMP_LOW_REG Instances

Instance	Physical Address
CPTS0	3900 0200h

Figure 14-5745. CPTS_TS_ESTF_COMP_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17385. CPTS_TS_ESTF_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp ESTF Generate Function Comparison Low Value This value should be written after the upper 32-bits. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

33 CPTS_TS_ESTF_COMP_HIGH_REG Register (Offset = 204h) [reset = 0h]

CPTS_COMP_HIGH_REG is shown in Figure 14-5746 and described in Table 14-11642.

Return to Summary Table.

Time Stamp ESTF Generate Function Comparison high Value

Table 14-17386. CPTS_TS_ESTF_COMP_HIGH_REG Instances

Instance	Physical Address
CPTS0	3900 0204h

Figure 14-5746. CPTS_TS_ESTF_COMP_HIGH_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">COMP_HIGH</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17388. CPTS_TS_ESTF_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp ESTF Generate Function Comparison High Value This value should be written before the lower 32-bits are written. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero

34 CPTS_TS_ESTF_CONTROL_REG Register (Offset = 208h) [reset = X]

CPTS_CONTROL_REG is shown in Figure 14-5747 and described in Table 14-11644.

Return to Summary Table.

Time Stamp ESTF Generate Function Control

Table 14-17389. CPTS_TS_ESTF_CONTROL_REG Instances

Instance	Physical Address
CPTS0	3900 0208h

Figure 14-5747. CPTS_TS_ESTF_CONTROL_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>PPM_DIR</td><td>POLARITY_INV</td></tr>
<tr><td colspan="6">R/W-X</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17391. CPTS_TS_ESTF_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	PPM_DIR	R/W	0h	Time Stamp ESTF Generate Function PPM Direction 0 – A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1 – A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.
0	POLARITY_INV	R/W	0h	Time Stamp ESTF Generate Function Polarity Invert 0 – The output TS_ESTFn signal asserts low 1 – The output TS_ESTFn signal asserts high

35 CPTS_TS_ESTF_LENGTH_REG Register (Offset = 20Ch) [reset = 0h]

CPTS_LENGTH_REG is shown in Figure 14-5748 and described in Table 14-11646.

Return to Summary Table.

Time Stamp ESTF Generate Function Length Value

Table 14-17392. CPTS_TS_ESTF_LENGTH_REG Instances

Instance	Physical Address
CPTS0	3900 020Ch

Figure 14-5748. CPTS_TS_ESTF_LENGTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17394. CPTS_TS_ESTF_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp ESTF Generate Function Length Value

36 CPTS_TS_ESTF_PPM_LOW_REG Register (Offset = 210h) [reset = 0h]

CPTS_PPM_LOW_REG is shown in Figure 14-5749 and described in Table 14-11648.

Return to Summary Table.

Time Stamp ESTF Generate Function PPM Low Value

Table 14-17395. CPTS_TS_ESTF_PPM_LOW_REG Instances

Instance	Physical Address
CPTS0	3900 0210h

Figure 14-5749. CPTS_TS_ESTF_PPM_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17397. CPTS_TS_ESTF_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp ESTF Generate Function PPM Low Value The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

37 CPTS_TS_ESTF_PPM_HIGH_REG Register (Offset = 214h) [reset = X]

CPTS_PPM_HIGH_REG is shown in Figure 14-5750 and described in Table 14-11650.

Return to Summary Table.

Time Stamp ESTF Generate Function PPM High Value

Table 14-17398. CPTS_TS_ESTF_PPM_HIGH_REG Instances

Instance	Physical Address
CPTS0	3900 0214h

Figure 14-5750. CPTS_TS_ESTF_PPM_HIGH_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="22">RESERVED</td><td colspan="10">PPM_HIGH</td></tr>
<tr><td colspan="22">R/W-X</td><td colspan="10">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17400. CPTS_TS_ESTF_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp ESTF Generate Function PPM High Value This value should be written first (before the low value is written).

38 CPTS_TS_ESTF_NUDGE_REG Register (Offset = 218h) [reset = X]

CPTS_NUDGE_REG is shown in Figure 14-5751 and described in Table 14-11652.

Return to Summary Table.

Time Stamp ESTF Generate Function Nudge Value

Table 14-17401. CPTS_TS_ESTF_NUDGE_REG Instances

Instance	Physical Address
CPTS0	3900 0218h

Figure 14-5751. CPTS_TS_ESTF_NUDGE_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">NUDGE</td></tr>
<tr><td colspan="24">R/W-X</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17403. CPTS_TS_ESTF_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp ESTF Generate Function Nudge Value This two’s complement number is added to the generate counter value to increase or decrease the length by the ts_estfN_nudge amount. Only a single high or low time is adjusted and the ts_estfN_nudge value is cleared to zero when the nudge has occurred.

14.8.2 Timer Manager Registers

14.8.2.1 TIMERMGR

TIMERMGR

14.8.2.1.1 TIMERMGR Summaries

TIMERMGR Summaries

Table 14-17404. TIMER_MGR_TIMERS Registers, Base Address=3700 0000h, Length=262144

Offset	Length	Register Name	TIMERMGR0 Physical Address
0h	32	TIMER_MGR_TIMERS_PAGE_ENTRY_SETUP_J_K	3700 0000h + formula
4h	32	TIMER_MGR_TIMERS_PAGE_ENTRY_CONTROL_J_K	3700 0004h + formula

Table 14-17405. TIMER_MGR Registers, Base Address=3CD0 0000h, Length=512

Offset	Length	Register Name	TIMERMGR0 Physical Address
0h	32	TIMER_MGR_PID	3CD0 0000h
4h	32	TIMER_MGR_CNTL	3CD0 0004h
8h	32	TIMER_MGR_COUNTER	3CD0 0008h
A0h	32	TIMER_MGR_TIMEOUT_STATUS0	3CD0 00A0h
A4h	32	TIMER_MGR_TIMEOUT_STATUS1	3CD0 00A4h
A8h	32	TIMER_MGR_TIMEOUT_STATUS_BANK0	3CD0 00A8h
100h	32	TIMER_MGR_STATUS_J	3CD0 0100h + formula

14.8.2.1.2 TIMERMGR Registers

TIMERMGR Registers

14.8.2.1.2.1 TIMER_MGR_TIMERS_PAGE_ENTRY_SETUP_j_k Register

1 TIMER_MGR_TIMERS_PAGE_ENTRY_SETUP_j_k Register (Offset = 0h + formula) [reset = 0h]

This reprograms timer N with the written value. This number will be the number of ticks of the timer_clock before the timer expires, if timer N and the timer manager itself are both enabled via TM_CTRL and TIMER_CONTROL_N

Return to Summary Table

Offset = (j * 1000h) + (k * 100h);; where j = 0 to 63d, k = 0 to 15d

Table 14-17406. Instance Table

Instance Name	Physical Address
TIMERMGR0	**3700 0000h + formula**

Figure 14-5752. TIMER_MGR_TIMERS_PAGE_ENTRY_SETUP_j_k Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-17408. TIMER_MGR_TIMERS_PAGE_ENTRY_SETUP_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	The number of ticks of the timer_clock before this timer would expire when reprogrammed Reset Source: core_srst_n

14.8.2.1.2.2 TIMER_MGR_TIMERS_PAGE_ENTRY_CONTROL_j_k Register

1 TIMER_MGR_TIMERS_PAGE_ENTRY_CONTROL_j_k Register (Offset = 4h + formula) [reset = 0h]

Modifies the behavior of timer N with control signals below

Return to Summary Table

Offset = (j * 1000h) + (k * 100h);; where j = 0 to 63d, k = 0 to 15d

Table 14-17409. Instance Table

Instance Name	Physical Address
TIMERMGR0	**3700 0004h + formula**

Figure 14-5753. TIMER_MGR_TIMERS_PAGE_ENTRY_CONTROL_j_k Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							AUTO_RESET
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TIMER_EXPIRED	SET_TIMER	TIMER_ENABLED
NONE					R	W	R/W
0h					0h	0h	0h

Table 14-17411. TIMER_MGR_TIMERS_PAGE_ENTRY_CONTROL_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	AUTO_RESET	R/W	0h	Automatically reset the timer when it expires. Provides the option of a periodic timer, rather than one that needs to be cleared after each expiration. Added for hardware usage of the timers, so the expirations can occur regularly without software reprogramming them. Reset Source: core_srst_n
7:3	RESERVED	NONE	0h	Reserved
2	TIMER_EXPIRED	R	0h	The status of the current timer. 1 = expired Reset Source: core_srst_n
1	SET_TIMER	W	0h	This may be used to touch/set a timer. When a 1 is written, the corresponding timer will be refreshed with the current value in its TIMER_SETUP_VALUES register. Will always read 0 Reset Source: core_srst_n
0	TIMER_ENABLED	R/W	0h	Write 1 to enable, 0 to disable the timer. Reset Source: core_srst_n

14.8.2.1.2.3 TIMER_MGR_PID Register

1 TIMER_MGR_PID Register (Offset = 0h) [reset = 66F82901h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Return to Summary Table

Table 14-17412. Instance Table

Instance Name	Physical Address
TIMERMGR0	**3CD0 0000h**

Figure 14-5754. TIMER_MGR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6F8h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6F8h							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
5h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		1h					

Table 14-17414. TIMER_MGR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID scheme Reset Source: core_srst_n
29:28	BU	R	2h	PID bu identifier Reset Source: core_srst_n
27:16	FUNCTION	R	6F8h	PID function identifier Reset Source: core_srst_n
15:11	RTL_VER	R	5h	PID RTL version number Reset Source: core_srst_n
10:8	MAJOR_REV	R	1h	PID Major revision number Reset Source: core_srst_n
7:6	CUSTOM	R	0h	PID custom Reset Source: core_srst_n
5:0	MINOR_REV	R	1h	PID Minor revision number Reset Source: core_srst_n

14.8.2.1.2.4 TIMER_MGR_CNTL Register

1 TIMER_MGR_CNTL Register (Offset = 4h) [reset = 7FEh]

This register controls the overall behavior of the timer manager module

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Table 14-17415. Instance Table

Instance Name	Physical Address
TIMERMGR0	**3CD0 0004h**

Figure 14-5755. TIMER_MGR_CNTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>MASS_ENABLE</td><td>RESERVED</td><td colspan="3">MAX_TIMER</td></tr>
<tr><td colspan="3">NONE</td><td>W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">3FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">MAX_TIMER</td><td>ENABLE</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">3FFh</td><td>0h</td></tr>
</table>

Table 14-17417. TIMER_MGR_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	MASS_ENABLE	W	0h	Always reads zero. When a 1 is written to this bit, all timers from 0 to the TM_CNTL.max_timer will be enabled. Useful for initial programming, to not need to loop over every TIMER_CONTROL register to enable every timer if many or all are being used. This should only be used during initialization, or when TM_CNTL.enable is set to 0, as this does not set the timers, only enable them Reset Source: core_srst_n
11	RESERVED	NONE	0h	Reserved
10:1	MAX_TIMER	R/W	3FFh	The maximum timer that will be checked - e.g. if only using 512 timers, set this to 511. All timers above this number will be ignored. Should be set once during initialization Reset Source: core_srst_n
0	ENABLE	R/W	0h	Enables the timer manager. When this bit is zero, the timers will all be halted and will not count Reset Source: core_srst_n 0 Timer Manager is disabled 1 Timer Manager is enabled

14.8.2.1.2.5 TIMER_MGR_COUNTER Register

1 TIMER_MGR_COUNTER Register (Offset = 8h) [reset = 0h]

This register contains the current counter value

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Table 14-17418. Instance Table

Instance Name	Physical Address
TIMERMGR0	**3CD0 0008h**

Figure 14-5756. TIMER_MGR_COUNTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17420. TIMER_MGR_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	The current timer_counter value, in the timebase being used by all timers in this module Reset Source: core_srst_n

14.8.2.1.2.6 TIMER_MGR_TIMEOUT_STATUS0 Register

1 TIMER_MGR_TIMEOUT_STATUS0 Register (Offset = A0h) [reset = 0h]

This register should be read whenever the timer interrupt fires. It indicates the total number of timers that have expired and the ID of the first timer to expire. If NUM_EXPIRED_TIMERS is 1, this is the only MMR that needs to be read. Depending on the value of NUM_EXPIRED_TIMERS, either TIMEOUT_STATUS_1 or TIMEOUT_STATUS_BANK may be read by the software to avoid needing to read all 32 TIMEOUT_STATUS_N registers.

Return to Summary Table

Table 14-17421. Instance Table

Instance Name	Physical Address
TIMERMGR0	**3CD0 00A0h**

Figure 14-5757. TIMER_MGR_TIMEOUT_STATUS0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
VALID0	EXPIRED_TIMER0						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
EXPIRED_TIMER0				NUM_EXPIRED_TIMERS			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
NUM_EXPIRED_TIMERS							
R							
0h							

Table 14-17423. TIMER_MGR_TIMEOUT_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	VALID0	R	0h	1 indicates that expired_timer0 is a valid expired timer. If num_expired_timers > 0, this should always be a 1 Reset Source: core_srst_n
22:12	EXPIRED_TIMER0	R	0h	The ID of the first timer to expire Reset Source: core_srst_n
11:0	NUM_EXPIRED_TIMERS	R	0h	The total number of expired timers Reset Source: core_srst_n

14.8.2.1.2.7 TIMER_MGR_TIMEOUT_STATUS1 Register

1 TIMER_MGR_TIMEOUT_STATUS1 Register (Offset = A4h) [reset = 0h]

This register contains the IDs of the second and third timers to expire. It is indended as a more efficient way of finding the first few timers to expire rather than needing to read the status of all 1024 timers.

Return to Summary Table

Table 14-17424. Instance Table

Instance Name	Physical Address
TIMERMGR0	3CD0 00A4h

Figure 14-5758. TIMER_MGR_TIMEOUT_STATUS1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VALID2	EXPIRED_TIMER2						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXPIRED_TIMER2				VALID1	EXPIRED_TIMER1		
R				R	R		
0h				0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXPIRED_TIMER1							
R							
0h							

Table 14-17426. TIMER_MGR_TIMEOUT_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	VALID2	R	0h	1 indicates that expired_timer2 is valid Reset Source: core_srst_n
22:12	EXPIRED_TIMER2	R	0h	The ID of the third timer to expire Reset Source: core_srst_n
11	VALID1	R	0h	1 indicates that expired_timer1 is valid Reset Source: core_srst_n
10:0	EXPIRED_TIMER1	R	0h	The ID of the second timer to expire Reset Source: core_srst_n

14.8.2.1.2.8 TIMER_MGR_TIMEOUT_STATUS_BANK0 Register

1 TIMER_MGR_TIMEOUT_STATUS_BANK0 Register (Offset = A8h) [reset = 0h]

This register contains the status of each timer bank for banks 31:0. When servicing the timer interrupt, if the num_expired_timers bit is greater than 3, this register may be read to see which banks contain expired timers. The TIMER_STATUS_N registers corresponding to those banks may then be read.

Return to Summary Table

Table 14-17427. Instance Table

Instance Name	Physical Address
TIMERMGR0	**3CD0 00A8h**

Figure 14-5759. TIMER_MGR_TIMEOUT_STATUS_BANK0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANK_STATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANK_STATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANK_STATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANK_STATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17429. TIMER_MGR_TIMEOUT_STATUS_BANK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANK_STATUS	R	0h	A 1 in bit N indicates that the corresponding bank has expired timers Reset Source: core_srst_n

14.8.2.1.2.9 TIMER_MGR_STATUS_j Register

1 TIMER_MGR_STATUS_j Register (Offset = 100h + formula) [reset = 0h]

Each bit is the timeout status for an individual timer. 0 = timer has not timed out or is disabled, 1 = timer has timed out

Return to Summary Table

Offset = (j * 4h); where j = 0 to 31d

Table 14-17430. Instance Table

Instance Name	Physical Address
TIMERMGR0	**3CD0 0100h + formula**

Figure 14-5760. TIMER_MGR_STATUS_j Name Register

31	30	29	28	27	26	25	24
STATUS							
R							
0h							
23	22	21	20	19	18	17	16
STATUS							
R							
0h							
15	14	13	12	11	10	9	8
STATUS							
R							
0h							
7	6	5	4	3	2	1	0
STATUS							
R							
0h							

Table 14-17432. TIMER_MGR_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATUS	R	0h	Each bit is the timeout status for an individual timer Reset Source: core_srst_n

14.8.3 Time Sync Routers Registers

14.8.3.1 TIMESYNC_EVENT_INTROUTER Registers

14.8.3.1.1 TIMESYNC_EVENT_INTROUTER Summary Table

Table 14-17433. TIMESYNC_EVENT_INTROUTER0_intr_router_cfg Registers, Base Address=00A4 0000h, Length=2048

Offset	Length	Register Name	TIMESYNC_EVENT_INTROUTER Physical Address
0h	32	INTR_ROUTER_CFG_PID	00A4 0000h
4h + formula	32	INTR_ROUTER_CFG_MUXCNTL_j	00A4 0004h

14.8.3.1.2 INTR_ROUTER_CFG_PID Register

INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Register Description: Identification register

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Table 14-17434. Instance Table

Instance Name	Physical Address
TIMESYNC_EVENT_INTROUTER0_intr_router_cfg	00A4 0000h

Figure 14-5761. INTR_ROUTER_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
694h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLVER					MAJREV		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-17436. INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	bu Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

14.8.3.1.3 INTR_ROUTER_CFG_MUXCNTL_j Register

INTR_ROUTER_CFG_MUXCNTL_j Register (Offset = 4h + formula) [reset = 0h]

Register Description: Interrupt mux control register

Formula = (j * 4h); where j = 0 to 40d

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Table 14-17437. Instance Table

Instance Name	Physical Address
TIMESYNC_EVENT_INTROUTER0_intr_router_cfg	00A4 0004h + formula

Figure 14-5762. INTR_ROUTER_CFG_MUXCNTL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							INT_ENABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		MUX_CNTL					
NONE		R/W					
0h		0h					

Table 14-17439. INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

14.8.3.2 CMP_EVENT_INTROUTER Registers

14.8.3.2.1 CMP_EVENT_INTROUTER Summary Table

Table 14-17440. CMP_EVENT_INTROUTER0_intr_router_cfg Registers, Base Address=00A3 0000h, Length=2048

Offset	Length	Register Name	CMP_EVENT_INTROUTER Physical Address
0h	32	INTR_ROUTER_CFG_PID	00A3 0000h
4h + formula	32	INTR_ROUTER_CFG_MUXCNTL_j	00A3 0004h

14.8.3.2.2 INTR_ROUTER_CFG_PID Register

INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Register Description: Identification register

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Table 14-17441. Instance Table

Instance Name	Physical Address
CMP_EVENT_INTROUTER0_intr_router_cfg	00A3 0000h

Figure 14-5763. INTR_ROUTER_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
694h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLVER					MAJREV		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-17443. INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	bu Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

14.8.3.2.3 INTR_ROUTER_CFG_MUXCNTL_j Register

INTR_ROUTER_CFG_MUXCNTL_j Register (Offset = 4h + formula) [reset = 0h]

Register Description: Interrupt mux control register

Formula = (j * 4h); where j = 0 to 42d

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Table 14-17444. Instance Table

Instance Name	Physical Address
CMP_EVENT_INTROUTER0_intr_router_cfg	00A3 0004h + formula

Figure 14-5764. INTR_ROUTER_CFG_MUXCNTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>INT_ENABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">MUX_CNTL</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-17446. INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:7	RESERVED	NONE	0h	Reserved
6:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

14.9 Peripherals Registers

14.9.1 General Connectivity Registers

14.9.1.1 ADC Registers

1 ADC Configuration Registers

Table 14-11684 lists the memory-mapped registers for the ADC. All register offset addresses not listed in Table 14-11684 should be considered as reserved locations and the register contents should not be modified.

Table 14-17447. ADC Instances

Instance	Base Address
ADC0	2800 1000h

Table 14-17448. ADC Registers

Offset	Acronym	Register Name	ADC0 Physical Address
0h	ADC_REVISION	Revision Identifier Register	2800 1000h
20h	ADC_EOI	End of Interrupt Register	2800 1020h
24h	ADC_STATUS_RAW	Raw Interrupt Status Register	2800 1024h
28h	ADC_STATUS	Interrupt Status Register	2800 1028h
2Ch	ADC_ENABLE_SET	Interrupt Enable Register	2800 102Ch
30h	ADC_ENABLE_CLR	Interrupt Disable Register	2800 1030h
38h	ADC_DMAENABLE_SET	DMA Request Enable Register	2800 1038h
3Ch	ADC_DMAENABLE_CLR	DMA Request Disable Register	2800 103Ch
40h	ADC_CONTROL	Control Register	2800 1040h
44h	ADC_SEQUENCER_STAT	Sequencer Status Register	2800 1044h
48h	ADC_RANGE	Range Check Register	2800 1048h
50h	ADC_MISC	AFE Input/Output Control Register	2800 1050h
54h	ADC_STEPENABLE	Sequencer Step Enable Register	2800 1054h
64h + formula	ADC_STEPCONFIG_j	Step Configuration Register	2800 1000h
68h + formula	ADC_STEPDELAY_j	Step Delay Register	2800 1000h
E4h	ADC_FIFO0WC	FIFO0 Word Count Register	2800 10E4h
E8h	ADC_FIFO0THRESHOLD	FIFO0 Threshold Level Register	2800 10E8h
ECh	ADC_FIFO0DMAREQ	FIFO0 DMA Request Level Register	2800 10ECh
F0h	ADC_FIFO1WC	FIFO1 Word Count Register	2800 10F0h
F4h	ADC_FIFO1THRESHOLD	FIFO1 Threshold Level Register	2800 10F4h
F8h	ADC_FIFO1DMAREQ	FIFO1 DMA Request Level Register	2800 10F8h
100h	ADC_FIFO0DATA	FIFO0 Read Data Register	2800 1100h
200h	ADC_FIFO1DATA	FIFO1 Read Data Register	2800 1200h

2 ADC_REVISION Register (Offset = 0h) [reset = 69C03900h]

ADC_REVISION is shown in Figure 14-5765 and described in Table 14-11686.

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IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility.

Table 14-17449. ADC_REVISION Instances

Instance	Physical Address
ADC0	2800 1000h

Figure 14-5765. ADC_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-69C0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-7h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17451. ADC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	69C0h	Module ID field
15-11	REVRTL	R	7h	RTL ADC_REVISION. Will vary depending on release.
10-8	REVMAJ	R	1h	Major ADC_REVISION
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	0h	Minor ADC_REVISION

3 ADC_EOI Register (Offset = 20h) [reset = 0h]

ADC_EOI is shown in Figure 14-5766 and described in Table 14-11688.

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The End of Interrupt (ADC_EOI) ADC_MISC Register allows the CPU to acknowledge completion of an interrupt by writing to the ADC_EOI for ADC_MISC interrupt sources. An eoi_write signal will be generated and another interrupt will be triggered if interrupt sources remain. This register will be reset one cycle after it has been written to.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-17452. ADC_EOI Instances

Instance	Physical Address
ADC0	2800 1020h

Figure 14-5766. ADC_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							LINENUMEOI
R-0h							W-0h

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 14-17454. ADC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	LINENUMEOI	W	0h	Software End Of Interrupt (EOI) control. 0h = EOI for interrupt line number 0. Read returns 0.

4 ADC_STATUS_RAW Register (Offset = 24h) [reset = 0h]

ADC_STATUS_RAW is shown in Figure 14-5767 and described in Table 14-11690.

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The ADC_STATUS_RAW register allows the ADC0 interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

Table 14-17455. ADC_STATUS_RAW Instances

Instance	Physical Address
ADC0	2800 1024h

Figure 14-5767. ADC_STATUS_RAW Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							OUTOFRANGE
R-0h							R/W1S-0h

7	6	5	4	3	2	1	0
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUENCE	AFE_EOC_MISSING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17457. ADC_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUTOFRANGE	R/W1S	0h	Status raw for out of range interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
7	FIFO1UNFL	R/W1S	0h	Status raw for FIFO1 under-flow interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
6	FIFO1OVFL	R/W1S	0h	Status raw for FIFO1 over-flow interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending

Table 14-17457. ADC_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FIFO1THRS	R/W1S	0h	Status raw for FIFO1 threshold interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
4	FIFO0UNFL	R/W1S	0h	Status raw for FIFO0 under-flow interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
3	FIFO0OVFL	R/W1S	0h	Status raw for FIFO0 over-flow interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
2	FIFO0THRS	R/W1S	0h	Status raw for FIFO0 threshold interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
1	ENDOFEQUENCE	R/W1S	0h	Status raw for end of sequence interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
0	AFE_EOC_MISSING	R/W1S	0h	Status raw for missing AFE EOC interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending

5 ADC_STATUS Register (Offset = 28h) [reset = 0h]

ADC_STATUS is shown in Figure 14-5768 and described in Table 14-11692.

Return to Summary Table.

The ADC_STATUS register allows the ADC0 interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

Table 14-17458. ADC_STATUS Instances

Instance	Physical Address
ADC0	2800 1028h

Figure 14-5768. ADC_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							OUTOFRANGE
R-0h							R/W1C-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUENCE	AFE_EOC_MISSING
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-17460. ADC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUTOFRANGE	R/W1C	0h	Enabled status for out of range interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
7	FIFO1UNFL	R/W1C	0h	Enabled status for FIFO1 under-flow interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
6	FIFO1OVFL	R/W1C	0h	Enabled status for FIFO1 over-flow interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending

Table 14-17460. ADC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FIFO1THRS	R/W1C	0h	Enabled status for FIFO1 threshold interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
4	FIFO0UNFL	R/W1C	0h	Enabled status for FIFO0 under-flow interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
3	FIFO0OVFL	R/W1C	0h	Enabled status for FIFO0 over-flow interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
2	FIFO0THRS	R/W1C	0h	Enabled status for FIFO0 threshold interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
1	ENDOFEQUENCE	R/W1C	0h	Enabled status for end of sequence interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
0	AFE_EOC_MISSING	R/W1C	0h	Enable status for missing AFE EOC interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending

6 ADC_ENABLE_SET Register (Offset = 2Ch) [reset = 0h]

ADC_ENABLE_SET is shown in Figure 14-5769 and described in Table 14-11694.

Return to Summary Table.

The ADC_ENABLE_SET register allows the ADC0 interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

Table 14-17461. ADC_ENABLE_SET Instances

Instance	Physical Address
ADC0	2800 102Ch

Figure 14-5769. ADC_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUTOFRANGE
R-0h							R/W1S-0h
7	6	5	4	3	2	1	0
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUENCE	AFE_EOC_MISSING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17463. ADC_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUTOFRANGE	R/W1S	0h	Out of range interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
7	FIFO1UNFL	R/W1S	0h	FIFO1 under-flow interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
6	FIFO1OVFL	R/W1S	0h	FIFO1 over-flow interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled

Table 14-17463. ADC_ENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FIFO1THRS	R/W1S	0h	FIFO1 threshold interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
4	FIFO0UNFL	R/W1S	0h	FIFO0 under-flow interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
3	FIFO0OVFL	R/W1S	0h	FIFO0 over-flow interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
2	FIFO0THRS	R/W1S	0h	FIFO0 threshold interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
1	ENDOFEQUENCE	R/W1S	0h	End of sequence interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
0	AFE_EOC_MISSING	R/W1S	0h	Missing AFE EOC interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled

7 ADC_ENABLE_CLR Register (Offset = 30h) [reset = 0h]

ADC_ENABLE_CLR is shown in Figure 14-5770 and described in Table 14-11696.

Return to Summary Table.

The ADC_ENABLE_CLR register allows the ADC0 interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

Table 14-17464. ADC_ENABLE_CLR Instances

Instance	Physical Address
ADC0	2800 1030h

Figure 14-5770. ADC_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUTOFRANGE
R-0h							R/W1C-0h
7	6	5	4	3	2	1	0
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUENCE	AFE_EOC_MISSING
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-17466. ADC_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUTOFRANGE	R/W1C	0h	Out of range interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
7	FIFO1UNFL	R/W1C	0h	FIFO1 under-flow interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
6	FIFO1OVFL	R/W1C	0h	FIFO1 over-flow interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled

Table 14-17466. ADC_ENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FIFO1THRS	R/W1C	0h	FIFO1 threshold interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
4	FIFO0UNFL	R/W1C	0h	FIFO0 under-flow interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
3	FIFO0OVFL	R/W1C	0h	FIFO0 over-flow interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
2	FIFO0THRS	R/W1C	0h	FIFO0 threshold interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
1	ENDOFEQUENCE	R/W1C	0h	End of sequence interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
0	AFE_EOC_MISSING	R/W1C	0h	Missing AFE EOC interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled

8 ADC_DMAENABLE_SET Register (Offset = 38h) [reset = 0h]

ADC_DMAENABLE_SET is shown in Figure 14-5771 and described in Table 14-11698.

Return to Summary Table.

The ADC_DMAENABLE_SET register allows the enabling of DMA requests.

Table 14-17467. ADC_DMAENABLE_SET Instances

Instance	Physical Address
ADC0	2800 1038h

Figure 14-5771. ADC_DMAENABLE_SET Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="7">RESERVED</td></tr>
<tr><td>R-0h</td><td colspan="7">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>ENABLE1</td><td>ENABLE0</td></tr>
<tr><td colspan="6">R-0h</td><td>R/W1S-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17469. ADC_DMAENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-2	RESERVED	R	0h	Reserved
1	ENABLE1	R/W1S	0h	Enable DMA event to FIFO1 Write 0h = No action Write 1h = Enable DMA event Read 0h = DMA event disabled Read 1h = DMA event enabled
0	ENABLE0	R/W1S	0h	Enable DMA event to FIFO0 Write 0h = No action Write 1h = Enable DMA event Read 0h = DMA event disabled Read 1h = DMA event enabled

9 ADC_DMAENABLE_CLR Register (Offset = 3Ch) [reset = X]

ADC_DMAENABLE_CLR is shown in Figure 14-5772 and described in Table 14-11700.

Return to Summary Table.

The ADC_DMAENABLE_CLR register allows the disabling of DMA requests.

Table 14-17470. ADC_DMAENABLE_CLR Instances

Instance	Physical Address
ADC0	2800 103Ch

Figure 14-5772. ADC_DMAENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						ENABLE1	ENABLE0
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-17472. ADC_DMAENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-2	RESERVED	R	0h	Reserved
1	ENABLE1	R/W1C	0h	Clears the enable of the DMA event to FIFO1. Disable DMA event to FIFO1 Write 0h = No action Write 1h = Disable DMA event Read 0h = DMA event disabled Read 1h = DMA event enabled
0	ENABLE0	R/W1C	0h	Clears the enable of the DMA event to FIFO0. Disable DMA event to FIFO0 Write 0h = No action Write 1h = Disable DMA event Read 0h = DMA event disabled Read 1h = DMA event enabled

10 ADC_CONTROL Register (Offset = 40h) [reset = 10h]

ADC_CONTROL is shown in Figure 14-5773 and described in Table 14-11702.

Return to Summary Table.

Controls various parameters of the cotroller state.

Table 14-17473. ADC_CONTROL Instances

Instance	Physical Address
ADC0	2800 1040h

Figure 14-5773. ADC_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				HI_MID_SEL	HI_MID_EN	HW_PREEMPT	HW_MAP
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			PD	RESERVED		STEP_ID_EN	MODULE_ENABLE
R-0h			R/W-1h	R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17475. ADC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	HI_MID_SEL	R/W	0h	Reference select for functional internal diagnostic debug mode. 0h = VMID 1h = REFP
10	HI_MID_EN	R/W	0h	Functional internal diagnostic debug mode. 0h = disabled 1h = enabled
9	HW_PREEMPT	R/W	0h	0h = SW steps are not preempted by HW events 1h = SW steps are preempted by HW events
8	HW_MAP	R/W	0h	0h = HW events are disabled 1h = HW events are enabled
7-5	RESERVED	R	0h	Reserved
4	PD	R/W	1h	ADC Power Down control. 0h = AFE is powered up 1h = AFE is powered down (default) At default, AFE is powered down; Software must write 0 to turn on the power and wait 4 us before starting a conversion
3	BIAS_SEL	R/W	0h	AFE select bias ADC control register
2	RESERVED	R	0h	Reserved

Table 14-17475. ADC_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	STEP_ID_EN	R/W	0h	Writing 1 to this bit will store the Step ID number with the captured ADC data in the FIFO. 0h = Write zeros 1h = Store the input (channel) ID tag
0	MODULE_ENABLE	R/W	0h	ADC module enable bit. After programming all the configuration and step enable registers, write a 1 to this bit to start conversion. Writing a 0 will disable the module after the current conversion. Before turning on again, the ADC_SEQUENCER_STAT register show read back STEP_IDLE = 10h and FSM_BUSY = 0h. Enabling the controller will be held off until MEM_INIT_DONE = 1h.

11 ADC_SEQUENCER_STAT Register (Offset = 44h) [reset = 20h]

ADC_SEQUENCER_STAT is shown in Figure 14-5774 and described in Table 14-11704.

Return to Summary Table.

SW can read this register to find out the currently scheduled step id being converted on the ADC port. If you want to turn the controller off and then back on, the step_id bit should be checked and compared to IDLE before enabling the ADC module again. Also, before enabling the controller again, the user should wait for the FSM bit 5 to read idl.

Table 14-17476. ADC_SEQUENCER_STAT Instances

Instance	Physical Address
ADC0	2800 1044h

Figure 14-5774. ADC_SEQUENCER_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	MEM_INIT_DONE	FSM_BUSY	STEP_IDLE				
R-0h	R-0h	R-1h	R-0h				

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17478. ADC_SEQUENCER_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	GPADC_BUSY	R	0h	Monitor the AFE internal calibration (busy bit)
7	RESERVED	R	0h	Reserved
6	MEM_INIT_DONE	R	0h	ADC_STATUS of RAM initialization for ECC. 1h = RAM initialization to 0 after reset is done.
5	FSM_BUSY	R	1h	ADC_STATUS of FSM. 0h = Idle 1h = Conversion in progress
4-0	STEP_IDLE	R	0h	10h = Idle 0h - Fh = Corresponds to Step 1 - Step 16

12 ADC_RANGE Register (Offset = 48h) [reset = 0h]

ADC_RANGE is shown in Figure 14-5775 and described in Table 14-11706.

Return to Summary Table.

This feature requires the ADC_RANGE check interrupt bit to be enabled first. The user can decide which input (channel) is compared by programming the RangeCheck bit of the ADC_STEPCONFIG_j Registers. It is up to software to sort through FIFO data to determine which input (channel) data was out of ADC_RANGE.

Table 14-17479. ADC_RANGE Instances

Instance	Physical Address
ADC0	2800 1048h

Figure 14-5775. ADC_RANGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HIRANGE											
R-0h				R/W-0h											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LOWRANGE											
R-0h				R/W-0h											

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17481. ADC_RANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-16	HIRANGE	R/W	0h	Sampled ADC data is compared to this value. If the sampled data is > HIRANGE, then interrupt is generated.
15-12	RESERVED	R	0h	Reserved
11-0	LOWRANGE	R/W	0h	Sampled ADC data is compared to this value. If the sampled data is < LOWRANGE, then interrupt is generated.

13 ADC_MISC Register (Offset = 50h) [reset = 0h]

ADC_MISC is shown in Figure 14-5776 and described in Table 14-11708.

Return to Summary Table.

Spare inputs of the AFE are driven by this register, spare outputs from the AFE are read.

Table 14-17482. ADC_MISC Instances

Instance	Physical Address
ADC0	2800 1050h

Figure 14-5776. ADC_MISC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				AFE_SPARE_OUT			
R-0h				R-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				AFE_SPARE_IN			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17484. ADC_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AFE_SPARE_OUT	R	0h	Connected to AFE Spare Output pins, reserved in normal operation.
7-4	RESERVED	R	0h	Reserved
3-0	AFE_SPARE_IN	R/W	0h	Connected to AFE Spare Input pins, reserved in normal operation.

14 ADC_STEPENABLE Register (Offset = 54h) [reset = 0h]

ADC_STEPENABLE is shown in Figure 14-5777 and described in Table 14-11710.

Return to Summary Table.

Contains the enable bit for each step in the sequencer. When all steps are disabled, the FSM will stay in IDLE state.

Table 14-17485. ADC_STEPENABLE Instances

Instance	Physical Address
ADC0	2800 1054h

Figure 14-5777. ADC_STEPENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							STEP16
R-0h							R/W-0h
15	14	13	12	11	10	9	8
STEP15	STEP14	STEP13	STEP12	STEP11	STEP10	STEP9	STEP8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
STEP7	STEP6	STEP5	STEP4	STEP3	STEP2	STEP1	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17487. ADC_STEPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	STEP16	R/W	0h	Enable step 16
15	STEP15	R/W	0h	Enable step 15
14	STEP14	R/W	0h	Enable step 14
13	STEP13	R/W	0h	Enable step 13
12	STEP12	R/W	0h	Enable step 12
11	STEP11	R/W	0h	Enable step 11
10	STEP10	R/W	0h	Enable step 10
9	STEP9	R/W	0h	Enable step 9
8	STEP8	R/W	0h	Enable step 8
7	STEP7	R/W	0h	Enable step 7
6	STEP6	R/W	0h	Enable step 6

Table 14-17487. ADC_STEPENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	STEP5	R/W	0h	Enable step 5
4	STEP4	R/W	0h	Enable step 4
3	STEP3	R/W	0h	Enable step 3
2	STEP2	R/W	0h	Enable step 2
1	STEP1	R/W	0h	Enable step 1
0	RESERVED	R	0h	Reserved

15 ADC_STEPCONFIG_j Register (Offset = 64h + formula) [reset = 00040000h]

ADC_STEPCONFIG_j is shown in Figure 14-5778 and described in Table 14-11712.

Return to Summary Table.

The user should write the appropriate value to this register that is required to configure the various functions of each step.

Offset = 64h + (j * 8h); where j = 0h to Fh

Table 14-17488. ADC_STEPCONFIG_j Instances

Instance	Physical Address
ADC0	2800 1000h

Figure 14-5778. ADC_STEPCONFIG_j Register

31	30	29	28	27	26	25	24
RESERVED				RANGECHECK	FIFOSEL	DIFF_CNTRL	RESERVED
R-0h				R/W-0h	R/W-0h	R/W-0h	R-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SEL_INP_SWC				SEL_INM_SWM		
R-0h	R/W-0h				R/W-8h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SEL_INM_SWM	RESERVED						
R/W-8h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			AVERAGING			MODE	
R-0h			R/W-0h			R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17490. ADC_STEPCONFIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	RANGECHECK	R/W	0h	0h = Disable ADC_RANGE check 1h = compare ADC data with ADC_RANGE
26	FIFOSEL	R/W	0h	Sampled data will be stored in FIFO. 0h = FIFO0 1h = FIFO1
25	DIFF_CNTRL	R/W	0h	Differential ADC_CONTROL. 0h = Single ended input, SEL_INM_SWM must be 8h 1h = Differential input
24-23	RESERVED	R	0h	Reserved
22-19	SEL_INP_SWC	R/W	0h	Select source for positive ADC input (INP). 0h = Input (channel) 0 1h = Input (channel) 1 2h = Input (channel) 2 3h = Input (channel) 3 4h = Input (channel) 4 5h = Input (channel) 5 6h = Input (channel) 6 7h = Input (channel) 7 8h = REFN

Table 14-17490. ADC_STEPCONFIG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	SEL_INM_SWM	R/W	8h	Select source for negative ADC input (INM). 0h = Input (channel) 0 1h = Input (channel) 1 2h = Input (channel) 2 3h = Input (channel) 3 4h = Input (channel) 4 5h = Input (channel) 5 6h = Input (channel) 6 7h = Input (channel) 7 8h = REFN
14-5	RESERVED	R	0h	Reserved
4-2	AVERAGING	R/W	0h	Number of samplings to average. 0h = no average 1h = 2 samples average 2h = 4 samples average 3h = 8 samples average 4h = 16 samples average
1-0	MODE	R/W	0h	0h = SW enabled, one-shot 1h = SW enabled, continuous 2h = HW synchronized, one-shot 3h = HW synchronized, continuous

16 ADC_STEPDELAY_j Register (Offset = 68h + formula) [reset = 0h]

ADC_STEPDELAY_j is shown in Figure 14-5779 and described in Table 14-11714.

Return to Summary Table.

Controls number of SMPL_CLK periods to sample and delay.

Offset = 68h + (j × 8h); where j = 0h to Fh

Table 14-17491. ADC_STEPDELAY_j Instances

Instance	Physical Address
ADC0	2800 1000h

Figure 14-5779. ADC_STEPDELAY_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SAMPLEDELAY</td><td colspan="6">RESERVED</td><td colspan="2">OPENDELAY</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="6">R-0h</td><td colspan="2">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">OPENDELAY</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17493. ADC_STEPDELAY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SAMPLEDELAY	R/W	0h	This register will control the number of SMPL_CLK cycles to sample the input signal (hold SOC high). Any value programmed here will be added to the minimum time of 2 SMPL_CLK cycles.
23-18	RESERVED	R	0h	Reserved
17-0	OPENDELAY	R/W	0h	Program the number of SMPL_CLK cycles to wait after applying the step configuration registers and before sending the start of ADC conversion.

17 ADC_FIFO0WC Register (Offset = E4h) [reset = 0h]

ADC_FIFO0WC is shown in Figure 14-5780 and described in Table 14-11716.

Return to Summary Table.

FIFO word count ADC_STATUS

Table 14-17494. ADC_FIFO0WC Instances

Instance	Physical Address
ADC0	2800 10E4h

Figure 14-5780. ADC_FIFO0WC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							NUMWDS								
R-0h																							R-0h								

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17496. ADC_FIFO0WC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	NUMWDS	R	0h	Number of words currently in the FIFO0.

18 ADC_FIFO0THRESHOLD Register (Offset = E8h) [reset = 0h]

ADC_FIFO0THRESHOLD is shown in Figure 14-5781 and described in Table 14-11718.

Return to Summary Table.

FIFO threshold

Table 14-17497. ADC_FIFO0THRESHOLD Instances

Instance	Physical Address
ADC0	2800 10E8h

Figure 14-5781. ADC_FIFO0THRESHOLD Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">THRESHOLD</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17499. ADC_FIFO0THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	THRESHOLD	R/W	0h	Program the desired FIFO0 data sample level minus 1 to reach before generating interrupt to CPU.

19 ADC_FIFO0DMAREQ Register (Offset = ECh) [reset = 0h]

ADC_FIFO0DMAREQ is shown in Figure 14-5782 and described in Table 14-11720.

Return to Summary Table.

DMA request.

Table 14-17500. ADC_FIFO0DMAREQ Instances

Instance	Physical Address
ADC0	2800 10ECh

Figure 14-5782. ADC_FIFO0DMAREQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DMAREQLEVEL							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17502. ADC_FIFO0DMAREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DMAREQLEVEL	R/W	0h	Number of words in FIFO0 before generating a DMA request.

20 ADC_FIFO1WC Register (Offset = F0h) [reset = 0h]

ADC_FIFO1WC is shown in Figure 14-5783 and described in Table 14-11722.

Return to Summary Table.

FIFO word count ADC_STATUS

Table 14-17503. ADC_FIFO1WC Instances

Instance	Physical Address
ADC0	2800 10F0h

Figure 14-5783. ADC_FIFO1WC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							NUMWDS								
R-0h																							R-0h								

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17505. ADC_FIFO1WC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	NUMWDS	R	0h	Number of words currently in the FIFO1.

21 ADC_FIFO1THRESHOLD Register (Offset = F4h) [reset = 0h]

ADC_FIFO1THRESHOLD is shown in Figure 14-5784 and described in Table 14-11724.

Return to Summary Table.

FIFO threshold

Table 14-17506. ADC_FIFO1THRESHOLD Instances

Instance	Physical Address
ADC0	2800 10F4h

Figure 14-5784. ADC_FIFO1THRESHOLD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRESHOLD							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17508. ADC_FIFO1THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	THRESHOLD	R/W	0h	Program the desired FIFO1 data sample level minus 1 to reach before generating interrupt to CPU.

22 ADC_FIFO1DMAREQ Register (Offset = F8h) [reset = 0h]

ADC_FIFO1DMAREQ is shown in Figure 14-5785 and described in Table 14-11726.

Return to Summary Table.

DMA request.

Table 14-17509. ADC_FIFO1DMAREQ Instances

Instance	Physical Address
ADC0	2800 10F8h

Figure 14-5785. ADC_FIFO1DMAREQ Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">DMAREQLEVEL</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17511. ADC_FIFO1DMAREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DMAREQLEVEL	R/W	0h	Number of words in FIFO1 before generating a DMA request.

23 ADC_FIFO0DATA Register (Offset = 100h) [reset = X]

ADC_FIFO0DATA is shown in Figure 14-5786 and described in Table 14-11728.

Return to Summary Table.

A read from this register will auto increment the FIFO read pointer. If you read when FIFO is empty, it will trigger an underflow interrupt.

Table 14-17512. ADC_FIFO0DATA Instances

Instance	Physical Address
ADC0	2800 1100h

Figure 14-5786. ADC_FIFO0DATA Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="12">RESERVED</td><td colspan="4">ADCCHANLID</td></tr>
<tr><td colspan="12">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="12">ADCDATA</td></tr>
<tr><td colspan="4">R-X</td><td colspan="12">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17514. ADC_FIFO0DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	ADCCHANLID	R	0h	Optional ID tag of input (channel) that captured the data. If tag option is disabled, these bits will be 0.
15-12	RESERVED	R	X	Reserved
11-0	ADCDATA	R	0h	Sampled ADC converted data value stored in FIFO0.

24 ADC_FIFO1DATA Register (Offset = 200h) [reset = X]

ADC_FIFO1DATA is shown in Figure 14-5787 and described in Table 14-11730.

Return to Summary Table.

A read from this register will auto increment the FIFO read pointer. If you read when FIFO is empty, it will trigger an underflow interrupt.

Table 14-17515. ADC_FIFO1DATA Instances

Instance	Physical Address
ADC0	2800 1200h

Figure 14-5787. ADC_FIFO1DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ADCCHANLID			
R-0h												R-0h			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ADCDATA											
R-X				R-0h											

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17517. ADC_FIFO1DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	ADCCHANLID	R	0h	Optional ID tag of input (channel) that captured the data. If tag option is disabled, these bits will be 0.
15-12	RESERVED	R	X	Reserved
11-0	ADCDATA	R	0h	Sampled ADC converted data value stored in FIFO1.

25 ADC FIFO and DMA Registers

Table 14-11732 lists the memory-mapped registers for the ADC0_FIFO0/1. All register offset addresses not listed in Table 14-11732 should be considered as reserved locations and the register contents should not be modified.

Table 14-17518. ADC FIFO and DMA Instances

Instance	Base Address
ADC0_FIFO	2800 0000h

Table 14-17519. ADC FIFO and DMA Registers

Offset	Acronym	Register Name	ADC0_FIFO Physical Address
100h	ADC_FIFO0DMADATA	ADC0_FIFO0 Memory Register	2800 0100h
200h	ADC_FIFO1DMADATA	ADC0_FIFO1 Memory Register	2800 0200h

26 ADC_FIFO0DMADATA Register (Offset = 100h) [reset = 0h]

ADC_FIFO0DMADATA is shown in Figure 14-5788 and described in Table 14-11734.

Return to Summary Table.

DMA sample FIFO

Table 14-17520. ADC_FIFO0DMADATA Instances

Instance	Physical Address
ADC0_FIFO	2800 0100h

Figure 14-5788. ADC_FIFO0DMADATA Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="12">RESERVED</td><td colspan="4">ADCCHANLID</td></tr>
<tr><td colspan="12">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="12">ADCDATA</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="12">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-17522. ADC_FIFO0DMADATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	ADCCHANLID	R	0h	Optional ID tag of input (channel) that captured the data. If tag option is disabled, these bits will be 0.
15-12	RESERVED	R	0h	Reserved
11-0	ADCDATA	R	0h	Sampled ADC converted data value stored in FIFO0.

27 ADC_FIFO1DMADATA Register (Offset = 200h) [reset = 0h]

ADC_FIFO1DMADATA is shown in Figure 14-5789 and described in Table 14-11736.

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DMA sample FIFO

Table 14-17523. ADC_FIFO1DMADATA Instances

Instance	Physical Address
ADC0_FIFO	2800 0200h

Figure 14-5789. ADC_FIFO1DMADATA Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="12">RESERVED</td><td colspan="4">ADCCHANLID</td></tr>
<tr><td colspan="12">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="12">ADCDATA</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="12">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17525. ADC_FIFO1DMADATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	ADCCHANLID	R	0h	Optional ID tag of input (channel) that captured the data. If tag option is disabled, these bits will be 0.
15-12	RESERVED	R	0h	Reserved
11-0	ADCDATA	R	0h	Sampled ADC converted data value stored in FIFO1.

28 ADC ECC Registers

Table 14-11738 lists the memory-mapped registers for the ADC ECC. All register offset addresses not listed in Table 14-11738 should be considered as reserved locations and the register contents should not be modified.

Table 14-17526. ADC ECC Instances

Instance	Base Address
ADC0_ECC	0071 A000h

Table 14-17527. ADC ECC Registers

Offset	Acronym	Register Name	ADC0_ECC Physical Address
0h	ADC_AGGR_REVISION	Aggregator Revision Register	0071 A000h
8h	ADC_ECC_VECTOR	ECC Vector Register	0071 A008h
Ch	ADC_MISC_STATUS	Misc Status Register	0071 A00Ch
3Ch	ADC_ECC_SEC_EOI_REG	SEC End of Interrupt Register	0071 A03Ch
40h	ADC_ECC_SEC_STATUS_REG0	Interrupt Status Register	0071 A040h
80h	ADC_ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register	0071 A080h
C0h	ADC_ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register	0071 A0C0h
13Ch	ADC_ECC_DED_EOI_REG	DED End of Interrupt Register	0071 A13Ch
140h	ADC_ECC_DED_STATUS_REG0	Interrupt Status Register	0071 A140h
180h	ADC_ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register	0071 A180h
1C0h	ADC_ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register	0071 A1C0h
200h	ADC_AGGR_ENABLE_SET	AGGR interrupt enable set Register	0071 A200h
204h	ADC_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	0071 A204h
208h	ADC_AGGR_STATUS_SET	AGGR interrupt status set Register	0071 A208h
20Ch	ADC_AGGR_STATUS_CLR	AGGR interrupt status clear Register	0071 A20Ch

29 ADC_AGGR_REVISION Register (Offset = 0h) [reset = 66A0EA00h]

ADC_AGGR_REVISION is shown in Figure 14-5790 and described in Table 14-11740.

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Revision parameters

Table 14-17528. ADC_AGGR_REVISION Instances

Instance	Physical Address
ADC0_ECC	0071 A000h

Figure 14-5790. ADC_AGGR_REVISION Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="12">MODULE_ID</td></tr>
<tr><td colspan="2">R-1h</td><td colspan="2">R-2h</td><td colspan="12">R-6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="5">R-1Dh</td><td colspan="3">R-2h</td><td colspan="2">R-0h</td><td colspan="6">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17530. ADC_AGGR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

30 ADC_ECC_VECTOR Register (Offset = 8h) [reset = X]

ADC_ECC_VECTOR is shown in Figure 14-5791 and described in Table 14-11742.

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ECC Vector Register

Table 14-17531. ADC_ECC_VECTOR Instances

Instance	Physical Address
ADC0_ECC	0071 A008h

Figure 14-5791. ADC_ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R-0h							R/W1C-0h

23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							

15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		

7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17533. ADC_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1h = Trigger a read on the serial VBUS
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for ADC_CONTROL or ADC_STATUS

31 ADC_MISC_STATUS Register (Offset = Ch) [reset = 2h]

ADC_MISC_STATUS is shown in Figure 14-5792 and described in Table 14-11744.

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Misc Status

Table 14-17534. ADC_MISC_STATUS Instances

Instance	Physical Address
ADC0_ECC	0071 A00Ch

Figure 14-5792. ADC_MISC_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-0h																					R-2h										

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17536. ADC_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	2h	Indicates the number of RAMS serviced by the ECC aggregator

32 ADC_ECC_WRAP_REV Register (Offset = 10h) [reset = 60060900h]

ADC_ECC_WRAP_REV is shown in Figure 14-5793 and described in Table 14-11746.

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Revision parameters

Table 14-17537. ADC_ECC_WRAP_REV Instances

Instance	Physical Address
ADC0_ECC	0071 A010h

Figure 14-5793. ADC_ECC_WRAP_REV Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="12">MODULE_ID</td></tr>
<tr><td colspan="2">R-1h</td><td colspan="2">R-2h</td><td colspan="12">R-6h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="5">R-1h</td><td colspan="3">R-1h</td><td colspan="2">R-0h</td><td colspan="6">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17539. ADC_ECC_WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6h	Module ID
15-11	REVRTL	R	1h	RTL version
10-8	REVMAJ	R	1h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

33 ADC_ECC_CTRL Register (Offset = 14h) [reset = X]

ADC_ECC_CTRL is shown in Figure 14-5794 and described in Table 14-11748.

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ECC Control Register

Table 14-17540. ADC_ECC_CTRL Instances

Instance	Physical Address
ADC0_ECC	0071 A014h

Figure 14-5794. ADC_ECC_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17542. ADC_ECC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	ERROR_ONCE	R/W	0h	Force Error only once
5	FORCE_N_ROW	R/W	0h	Force Error on any RAM read
4	FORCE_DED	R/W	0h	Force Double Bit Error
3	FORCE_SEC	R/W	0h	Force Single Bit Error
2	ENABLE_RMW	R/W	1h	Enable rmw
1	ECC_CHECK	R/W	1h	Enable ECC check
0	ECC_ENABLE	R/W	1h	Enable ECC

34 ADC_ECC_ERR_CTRL1 Register (Offset = 18h) [reset = 0h]

ADC_ECC_ERR_CTRL1 is shown in Figure 14-5795 and described in Table 14-11750.

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ECC Error Control1 Register

Table 14-17543. ADC_ECC_ERR_CTRL1 Instances

Instance	Physical Address
ADC0_ECC	0071 A018h

Figure 14-5795. ADC_ECC_ERR_CTRL1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">ECC_ROW</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17545. ADC_ECC_ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R/W	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

35 ADC_ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ADC_ECC_ERR_CTRL2 is shown in Figure 14-5796 and described in Table 14-11752.

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ECC Error Control2 Register

Table 14-17546. ADC_ECC_ERR_CTRL2 Instances

Instance	Physical Address
ADC0_ECC	0071 A01Ch

Figure 14-5796. ADC_ECC_ERR_CTRL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT2																ECC_BIT1															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17548. ADC_ECC_ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT2	R/W	0h	Data bit that needs to be flipped if double bit error needs to be forced
15-0	ECC_BIT1	R/W	0h	Data bit that needs to be flipped when force_sec is set

36 ADC_ECC_ERR_STAT1 Register (Offset = 20h) [reset = 0h]

ADC_ECC_ERR_STAT1 is shown in Figure 14-5797 and described in Table 14-11754.

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ECC Error Status1 Register

Table 14-17549. ADC_ECC_ERR_STAT1 Instances

Instance	Physical Address
ADC0_ECC	0071 A020h

Figure 14-5797. ADC_ECC_ERR_STAT1 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ECC_BIT1</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ECC_BIT1</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>CLR_ECC_OTHER</td><td>CLR_ECC_DED</td><td>CLR_ECC_SEC</td></tr>
<tr><td colspan="5">R-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>ECC_OTHER</td><td>ECC_DED</td><td>ECC_SEC</td></tr>
<tr><td colspan="5">R-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17551. ADC_ECC_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT1	R	0h	Data bit that corresponds to the single-bit error
15-11	RESERVED	R	0h	Reserved
10	CLR_ECC_OTHER	R/W	0h	Clear other Error Status
9	CLR_ECC_DED	R/W	0h	Clear Double Bit Error Status
8	CLR_ECC_SEC	R/W	0h	Clear Single Bit Error Status
7-3	RESERVED	R	0h	Reserved
2	ECC_OTHER	R/W	0h	Successive single-bit errors have occurred while a writeback is still pending, Level interrupt
1	ECC_DED	R/W	0h	Level Double Bit Error Status
0	ECC_SEC	R/W	0h	Level Single Bit Error Status

37 ADC_ECC_ERR_STAT2 Register (Offset = 24h) [reset = 0h]

ADC_ECC_ERR_STAT2 is shown in Figure 14-5798 and described in Table 14-11756.

Return to Summary Table.

ECC Error Status1 Register

Table 14-17552. ADC_ECC_ERR_STAT2 Instances

Instance	Physical Address
ADC0_ECC	0071 A024h

Figure 14-5798. ADC_ECC_ERR_STAT2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">ECC_ROW</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17554. ADC_ECC_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R	0h	Row address where the single or double-bit error has occurred

38 ADC_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

ADC_ECC_SEC_EOI_REG is shown in Figure 14-5799 and described in Table 14-11758.

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ADC_EOI Register

Table 14-17555. ADC_ECC_SEC_EOI_REG Instances

Instance	Physical Address
ADC0_ECC	0071 A03Ch

Figure 14-5799. ADC_ECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17557. ADC_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	ADC_EOI Register

39 ADC_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

ADC_ECC_SEC_STATUS_REG0 is shown in Figure 14-5800 and described in Table 14-11760.

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Interrupt Status Register 0

Table 14-17558. ADC_ECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
ADC0_ECC	0071 A040h

Figure 14-5800. ADC_ECC_SEC_STATUS_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>RAM1_PEND</td><td>RAM0_PEND</td></tr>
<tr><td colspan="6">R-0h</td><td>R/W1S-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17560. ADC_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	RAM1_PEND	R/W1S	0h	Interrupt Pending Status for ram1_pend
0	RAM0_PEND	R/W1S	0h	Interrupt Pending Status for ram0_pend

40 ADC_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

ADC_ECC_SEC_ENABLE_SET_REG0 is shown in Figure 14-5801 and described in Table 14-11762.

Return to Summary Table.

Interrupt Enable Set Register 0

Table 14-17561. ADC_ECC_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
ADC0_ECC	0071 A080h

Figure 14-5801. ADC_ECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						RAM1_ENABLE_SET	RAM0_ENABLE_SET
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17563. ADC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	RAM1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ram1_pend
0	RAM0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ram0_pend

41 ADC_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

ADC_ECC_SEC_ENABLE_CLR_REG0 is shown in Figure 14-5802 and described in Table 14-11764.

Return to Summary Table.

Interrupt Enable Clear Register 0

Table 14-17564. ADC_ECC_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
ADC0_ECC	0071 A0C0h

Figure 14-5802. ADC_ECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						RAM1_ENABLE_CLR	RAM0_ENABLE_CLR
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-17566. ADC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	RAM1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ram1_pend
0	RAM0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ram0_pend

42 ADC_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

ADC_ECC_DED_EOI_REG is shown in Figure 14-5803 and described in Table 14-11766.

Return to Summary Table.

ADC_EOI Register

Table 14-17567. ADC_ECC_DED_EOI_REG Instances

Instance	Physical Address
ADC0_ECC	0071 A13Ch

Figure 14-5803. ADC_ECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17569. ADC_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	ADC_EOI Register

43 ADC_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

ADC_ECC_DED_STATUS_REG0 is shown in Figure 14-5804 and described in Table 14-11768.

Return to Summary Table.

Interrupt Status Register 0

Table 14-17570. ADC_ECC_DED_STATUS_REG0 Instances

Instance	Physical Address
ADC0_ECC	0071 A140h

Figure 14-5804. ADC_ECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						RAM1_PEND	RAM0_PEND
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17572. ADC_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	RAM1_PEND	R/W1S	0h	Interrupt Pending Status for ram1_pend
0	RAM0_PEND	R/W1S	0h	Interrupt Pending Status for ram0_pend

44 ADC_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

ADC_ECC_DED_ENABLE_SET_REG0 is shown in Figure 14-5805 and described in Table 14-11770.

Return to Summary Table.

Interrupt Enable Set Register 0

Table 14-17573. ADC_ECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
ADC0_ECC	0071 A180h

Figure 14-5805. ADC_ECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						RAM1_ENABLE_SET	RAM0_ENABLE_SET
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17575. ADC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	RAM1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ram1_pend
0	RAM0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ram0_pend

45 ADC_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

ADC_ECC_DED_ENABLE_CLR_REG0 is shown in Figure 14-5806 and described in Table 14-11772.

Return to Summary Table.

Interrupt Enable Clear Register 0

Table 14-17576. ADC_ECC_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
ADC0_ECC	0071 A1C0h

Figure 14-5806. ADC_ECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						RAM1_ENABLE_CLR	RAM0_ENABLE_CLR
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-17578. ADC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	RAM1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ram1_pend
0	RAM0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ram0_pend

46 ADC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

aggr_enable_set is shown in Figure 14-5807 and described in Table 14-11774.

Return to the Summary Table.

AGGR interrupt enable set Register

Table 14-17579. ADC_AGGR_ENABLE_SET Instances

Instance	Physical Address
ADC0_ECC	0071 A200h

Figure 14-5807. ADC_AGGR_ENABLE_SET Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">R-0h</td><td>R/W1S-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-17581. ADC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

47 ADC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

aggr_enable_clr is shown in Figure 14-5808 and described in Table 14-11776.

Return to the Summary Table.

AGGR interrupt enable clear Register

Table 14-17582. ADC_AGGR_ENABLE_CLR Instances

Instance	Physical Address
ADC0_ECC	0071 A204h

Figure 14-5808. ADC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-17584. ADC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

48 ADC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

aggr_status_set is shown in Figure 14-5809 and described in Table 14-11778.

Return to the Summary Table.

AGGR interrupt status set Register

Table 14-17585. ADC_AGGR_STATUS_SET Instances

Instance	Physical Address
ADC0_ECC	0071 A208h

Figure 14-5809. ADC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wincr-0h		R/Wincr-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -*n* = value after reset

Table 14-17587. ADC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

49 ADC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

aggr_status_clr is shown in Figure 14-5810 and described in Table 14-11780.

Return to the Summary Table.

AGGR interrupt status clear Register

Table 14-17588. ADC_AGGR_STATUS_CLR Instances

Instance	Physical Address
ADC0_ECC	0071 A20Ch

Figure 14-5810. ADC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -*n* = value after reset

Table 14-17590. ADC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

14.9.1.2 GPIO

GPIO

14.9.1.2.1 GPIO Summaries

GPIO Summaries

Table 14-17591. GPIO Registers, Base Address=0060 0000h, Length=256

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	MCU_GPIO0 Physical Address
0h	32	GPIO_PID	0060 0000h	0060 1000h	0420 1000h
4h	32	GPIO_PCR	0060 0004h	0060 1004h	0420 1004h
8h	32	GPIO_BINTEN	0060 0008h	0060 1008h	0420 1008h
10h	32	GPIO_DIR01	0060 0010h	0060 1010h	0420 1010h
14h	32	GPIO_OUT_DATA01	0060 0014h	0060 1014h	0420 1014h
18h	32	GPIO_SET_DATA01	0060 0018h	0060 1018h	0420 1018h
1Ch	32	GPIO_CLR_DATA01	0060 001Ch	0060 101Ch	0420 101Ch
20h	32	GPIO_IN_DATA01	0060 0020h	0060 1020h	0420 1020h
24h	32	GPIO_SET_RIS_TRIG01	0060 0024h	0060 1024h	0420 1024h
28h	32	GPIO_CLR_RIS_TRIG01	0060 0028h	0060 1028h	0420 1028h
2Ch	32	GPIO_SET_FAL_TRIG01	0060 002Ch	0060 102Ch	0420 102Ch
30h	32	GPIO_CLR_FAL_TRIG01	0060 0030h	0060 1030h	0420 1030h
34h	32	GPIO_INTSTAT01	0060 0034h	0060 1034h	0420 1034h
38h	32	GPIO_DIR23	0060 0038h	0060 1038h	0420 1038h
3Ch	32	GPIO_OUT_DATA23	0060 003Ch	0060 103Ch	0420 103Ch
40h	32	GPIO_SET_DATA23	0060 0040h	0060 1040h	0420 1040h
44h	32	GPIO_CLR_DATA23	0060 0044h	0060 1044h	0420 1044h
48h	32	GPIO_IN_DATA23	0060 0048h	0060 1048h	0420 1048h
4Ch	32	GPIO_SET_RIS_TRIG23	0060 004Ch	0060 104Ch	0420 104Ch
50h	32	GPIO_CLR_RIS_TRIG23	0060 0050h	0060 1050h	0420 1050h
54h	32	GPIO_SET_FAL_TRIG23	0060 0054h	0060 1054h	0420 1054h
58h	32	GPIO_CLR_FAL_TRIG23	0060 0058h	0060 1058h	0420 1058h
5Ch	32	GPIO_INTSTAT23	0060 005Ch	0060 105Ch	0420 105Ch
60h	32	GPIO_DIR45	0060 0060h	0060 1060h	0420 1060h
64h	32	GPIO_OUT_DATA45	0060 0064h	0060 1064h	0420 1064h
68h	32	GPIO_SET_DATA45	0060 0068h	0060 1068h	0420 1068h
6Ch	32	GPIO_CLR_DATA45	0060 006Ch	0060 106Ch	0420 106Ch
70h	32	GPIO_IN_DATA45	0060 0070h	0060 1070h	0420 1070h
74h	32	GPIO_SET_RIS_TRIG45	0060 0074h	0060 1074h	0420 1074h
78h	32	GPIO_CLR_RIS_TRIG45	0060 0078h	0060 1078h	0420 1078h
7Ch	32	GPIO_SET_FAL_TRIG45	0060 007Ch	0060 107Ch	0420 107Ch
80h	32	GPIO_CLR_FAL_TRIG45	0060 0080h	0060 1080h	0420 1080h
84h	32	GPIO_INTSTAT45	0060 0084h	0060 1084h	0420 1084h
88h	32	GPIO_DIR67	0060 0088h	0060 1088h	0420 1088h
8Ch	32	GPIO_OUT_DATA67	0060 008Ch	0060 108Ch	0420 108Ch
90h	32	GPIO_SET_DATA67	0060 0090h	0060 1090h	0420 1090h
94h	32	GPIO_CLR_DATA67	0060 0094h	0060 1094h	0420 1094h

Table 14-17591. GPIO Registers, Base Address=0060 0000h, Length=256 (continued)

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	MCU_GPIO0 Physical Address
98h	32	GPIO_IN_DATA67	0060 0098h	0060 1098h	0420 1098h
9Ch	32	GPIO_SET_RIS_TRIG67	0060 009Ch	0060 109Ch	0420 109Ch
A0h	32	GPIO_CLR_RIS_TRIG67	0060 00A0h	0060 10A0h	0420 10A0h
A4h	32	GPIO_SET_FAL_TRIG67	0060 00A4h	0060 10A4h	0420 10A4h
A8h	32	GPIO_CLR_FAL_TRIG67	0060 00A8h	0060 10A8h	0420 10A8h
ACh	32	GPIO_INTSTAT67	0060 00ACh	0060 10ACh	0420 10ACh
B0h	32	GPIO_DIR8	0060 00B0h	0060 10B0h	0420 10B0h
B4h	32	GPIO_OUT_DATA8	0060 00B4h	0060 10B4h	0420 10B4h
B8h	32	GPIO_SET_DATA8	0060 00B8h	0060 10B8h	0420 10B8h
BCh	32	GPIO_CLR_DATA8	0060 00BCh	0060 10BCh	0420 10BCh
C0h	32	GPIO_IN_DATA8	0060 00C0h	0060 10C0h	0420 10C0h
C4h	32	GPIO_SET_RIS_TRIG8	0060 00C4h	0060 10C4h	0420 10C4h
C8h	32	GPIO_CLR_RIS_TRIG8	0060 00C8h	0060 10C8h	0420 10C8h
CCh	32	GPIO_SET_FAL_TRIG8	0060 00CCh	0060 10CCh	0420 10CCh
D0h	32	GPIO_CLR_FAL_TRIG8	0060 00D0h	0060 10D0h	0420 10D0h
D4h	32	GPIO_INTSTAT8	0060 00D4h	0060 10D4h	0420 10D4h

14.9.1.2.2 GPIO Registers

GPIO Registers

14.9.1.2.2.1 GPIO_PID Register

1 GPIO_PID Register (Offset = 0h) [reset = 44832905h]

GPIO Periperal ID Register

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Table 14-17592. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0000h**
GPIO1	**0060 1000h**
MCU_GPIO0	**0420 1000h**

Figure 14-5811. GPIO_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		R		R			
1h		0h		483h			

23	22	21	20	19	18	17	16
FUNC							
R							
483h							

15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
5h					1h		

7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		5h					

Table 14-17594. GPIO_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Current scheme Reset Source: mod_g_srst_n
29:28	RESERVED	R	0h	RESERVED
27:16	FUNC	R	483h	Function code assigned to TCP3 Reset Source: mod_g_srst_n
15:11	RTL	R	5h	RTL Version R code Reset Source: mod_g_srst_n
10:8	MAJOR	R	1h	Major revision X code Reset Source: mod_g_srst_n
7:6	CUSTOM	R	0h	Custom version code Reset Source: mod_g_srst_n
5:0	MINOR	R	5h	Minor revision Y code Reset Source: mod_g_srst_n

14.9.1.2.2.2 GPIO_PCR Register

1 GPIO_PCR Register (Offset = 4h) [reset = 1h]

Peripheral Control Register

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Table 14-17595. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0004h**
GPIO1	**0060 1004h**
MCU_GPIO0	**0420 1004h**

Figure 14-5812. GPIO_PCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R	R
0h						0h	1h

Table 14-17597. GPIO_PCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R	0h	Used in conjunction with FREE bit to determine the emulation suspend mode. Reset Source: mod_g_srst_n
0	FREE	R	1h	For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend. Reset Source: mod_g_srst_n

14.9.1.2.2.3 GPIO_BINTEN Register

1 GPIO_BINTEN Register (Offset = 8h) [reset = 0h]

Bit Interrupt Enable Register

Return to Summary Table

Table 14-17598. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0008h**
GPIO1	**0060 1008h**
MCU_GPIO0	**0420 1008h**

Figure 14-5813. GPIO_BINTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
EN							
R/W							
0h							
7	6	5	4	3	2	1	0
EN							
R/W							
0h							

Table 14-17600. GPIO_BINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	EN	R/W	0h	Per bank interrupt enable. 0 = disable, 1 = enable. Reset Source: mod_g_srst_n

14.9.1.2.2.4 GPIO_DIR01 Register

1 GPIO_DIR01 Register (Offset = 10h) [reset = FFFFFFFFh]

Direction Register

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Table 14-17601. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0010h**
GPIO1	**0060 1010h**
MCU_GPIO0	**0420 1010h**

Figure 14-5814. GPIO_DIR01 Name Register

31	30	29	28	27	26	25	24
DIR1							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR1							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR0							
R/W							
FFFFh							

Table 14-17603. GPIO_DIR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR1	R/W	FFFFh	Direction of GPIO bank 1 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR0	R/W	FFFFh	Direction of GPIO bank 0 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.1.2.2.5 GPIO_OUT_DATA01 Register

1 GPIO_OUT_DATA01 Register (Offset = 14h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-17604. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0014h**
GPIO1	**0060 1014h**
MCU_GPIO0	**0420 1014h**

Figure 14-5815. GPIO_OUT_DATA01 Name Register

31	30	29	28	27	26	25	24
OUT1							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT1							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT0							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT0							
R/W							
0h							

Table 14-17606. GPIO_OUT_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT1	R/W	0h	Output drive state of GPIO bank 1 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT0	R/W	0h	Output drive state of GPIO bank 0 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.6 GPIO_SET_DATA01 Register

1 GPIO_SET_DATA01 Register (Offset = 18h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-17607. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0018h**
GPIO1	**0060 1018h**
MCU_GPIO0	**0420 1018h**

Figure 14-5816. GPIO_SET_DATA01 Name Register

31	30	29	28	27	26	25	24
SET1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET0							
R/W1TS							
0h							

Table 14-17609. GPIO_SET_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET1	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 1 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET0	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 0 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.7 GPIO_CLR_DATA01 Register

1 GPIO_CLR_DATA01 Register (Offset = 1Ch) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-17610. Instance Table

Instance Name	Physical Address
GPIO0	**0060 001Ch**
GPIO1	**0060 101Ch**
MCU_GPIO0	**0420 101Ch**

Figure 14-5817. GPIO_CLR_DATA01 Name Register

31	30	29	28	27	26	25	24
CLR1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR0							
R/W1TC							
0h							

Table 14-17612. GPIO_CLR_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR1	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR0	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.8 GPIO_IN_DATA01 Register

1 GPIO_IN_DATA01 Register (Offset = 20h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-17613. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0020h**
GPIO1	**0060 1020h**
MCU_GPIO0	**0420 1020h**

Figure 14-5818. GPIO_IN_DATA01 Name Register

31	30	29	28	27	26	25	24
IN1							
R							
0h							
23	22	21	20	19	18	17	16
IN1							
R							
0h							
15	14	13	12	11	10	9	8
IN0							
R							
0h							
7	6	5	4	3	2	1	0
IN0							
R							
0h							

Table 14-17615. GPIO_IN_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN1	R	0h	Status of GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	IN0	R	0h	Status of GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.9 GPIO_SET_RIS_TRIG01 Register

1 GPIO_SET_RIS_TRIG01 Register (Offset = 24h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-17616. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0024h**
GPIO1	**0060 1024h**
MCU_GPIO0	**0420 1024h**

Figure 14-5819. GPIO_SET_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24
SETRIS1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS0							
R/W1TS							
0h							

Table 14-17618. GPIO_SET_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS1	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	SETRIS0	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.10 GPIO_CLR_RIS_TRIG01 Register

1 GPIO_CLR_RIS_TRIG01 Register (Offset = 28h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-17619. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0028h**
GPIO1	**0060 1028h**
MCU_GPIO0	**0420 1028h**

Figure 14-5820. GPIO_CLR_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24
CLRRIS1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS0							
R/W1TC							
0h							

Table 14-17621. GPIO_CLR_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS1	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS0	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.11 GPIO_SET_FAL_TRIG01 Register

1 GPIO_SET_FAL_TRIG01 Register (Offset = 2Ch) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-17622. Instance Table

Instance Name	Physical Address
GPIO0	**0060 002Ch**
GPIO1	**0060 102Ch**
MCU_GPIO0	**0420 102Ch**

Figure 14-5821. GPIO_SET_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24
SETFAL1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL0							
R/W1TS							
0h							

Table 14-17624. GPIO_SET_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL1	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	SETFAL0	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.12 GPIO_CLR_FAL_TRIG01 Register

1 GPIO_CLR_FAL_TRIG01 Register (Offset = 30h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-17625. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0030h**
GPIO1	**0060 1030h**
MCU_GPIO0	**0420 1030h**

Figure 14-5822. GPIO_CLR_FAL_TRIG01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLRFAL1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLRFAL1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLRFAL0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLRFAL0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17627. GPIO_CLR_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL1	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL0	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.13 GPIO_INTSTAT01 Register

1 GPIO_INTSTAT01 Register (Offset = 34h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-17628. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0034h**
GPIO1	**0060 1034h**
MCU_GPIO0	**0420 1034h**

Figure 14-5823. GPIO_INTSTAT01 Name Register

31	30	29	28	27	26	25	24
STAT1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT0							
R/W1TC							
0h							

Table 14-17630. GPIO_INTSTAT01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT1	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT0	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.1.2.2.14 GPIO_DIR23 Register

1 GPIO_DIR23 Register (Offset = 38h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-17631. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0038h**
GPIO1	**0060 1038h**
MCU_GPIO0	**0420 1038h**

Figure 14-5824. GPIO_DIR23 Name Register

31	30	29	28	27	26	25	24
DIR3							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR3							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR2							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR2							
R/W							
FFFFh							

Table 14-17633. GPIO_DIR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR3	R/W	FFFFh	Direction of GPIO bank 3 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR2	R/W	FFFFh	Direction of GPIO bank 2 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.1.2.2.15 GPIO_OUT_DATA23 Register

1 GPIO_OUT_DATA23 Register (Offset = 3Ch) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-17634. Instance Table

Instance Name	Physical Address
GPIO0	**0060 003Ch**
GPIO1	**0060 103Ch**
MCU_GPIO0	**0420 103Ch**

Figure 14-5825. GPIO_OUT_DATA23 Name Register

31	30	29	28	27	26	25	24
OUT3							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT3							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT2							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT2							
R/W							
0h							

Table 14-17636. GPIO_OUT_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT3	R/W	0h	Output drive state of GPIO bank 3 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT2	R/W	0h	Output drive state of GPIO bank 2 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.16 GPIO_SET_DATA23 Register

1 GPIO_SET_DATA23 Register (Offset = 40h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-17637. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0040h**
GPIO1	**0060 1040h**
MCU_GPIO0	**0420 1040h**

Figure 14-5826. GPIO_SET_DATA23 Name Register

31	30	29	28	27	26	25	24
SET3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET2							
R/W1TS							
0h							

Table 14-17639. GPIO_SET_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET3	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 3 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET2	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 2 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.17 GPIO_CLR_DATA23 Register

1 GPIO_CLR_DATA23 Register (Offset = 44h) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-17640. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0044h**
GPIO1	**0060 1044h**
MCU_GPIO0	**0420 1044h**

Figure 14-5827. GPIO_CLR_DATA23 Name Register

31	30	29	28	27	26	25	24
CLR3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR2							
R/W1TC							
0h							

Table 14-17642. GPIO_CLR_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR3	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR2	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.18 GPIO_IN_DATA23 Register

1 GPIO_IN_DATA23 Register (Offset = 48h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-17643. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0048h**
GPIO1	**0060 1048h**
MCU_GPIO0	**0420 1048h**

Figure 14-5828. GPIO_IN_DATA23 Name Register

31	30	29	28	27	26	25	24
IN3							
R							
0h							
23	22	21	20	19	18	17	16
IN3							
R							
0h							
15	14	13	12	11	10	9	8
IN2							
R							
0h							
7	6	5	4	3	2	1	0
IN2							
R							
0h							

Table 14-17645. GPIO_IN_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN3	R	0h	Status of GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	IN2	R	0h	Status of GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.19 GPIO_SET_RIS_TRIG23 Register

1 GPIO_SET_RIS_TRIG23 Register (Offset = 4Ch) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-17646. Instance Table

Instance Name	Physical Address
GPIO0	**0060 004Ch**
GPIO1	**0060 104Ch**
MCU_GPIO0	**0420 104Ch**

Figure 14-5829. GPIO_SET_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24
SETRIS3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS2							
R/W1TS							
0h							

Table 14-17648. GPIO_SET_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS3	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	SETRIS2	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.20 GPIO_CLR_RIS_TRIG23 Register

1 GPIO_CLR_RIS_TRIG23 Register (Offset = 50h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-17649. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0050h**
GPIO1	**0060 1050h**
MCU_GPIO0	**0420 1050h**

Figure 14-5830. GPIO_CLR_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24
CLRRIS3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS2							
R/W1TC							
0h							

Table 14-17651. GPIO_CLR_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS3	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS2	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.21 GPIO_SET_FAL_TRIG23 Register

1 GPIO_SET_FAL_TRIG23 Register (Offset = 54h) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-17652. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0054h**
GPIO1	**0060 1054h**
MCU_GPIO0	**0420 1054h**

Figure 14-5831. GPIO_SET_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24
SETFAL3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL2							
R/W1TS							
0h							

Table 14-17654. GPIO_SET_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL3	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	SETFAL2	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.22 GPIO_CLR_FAL_TRIG23 Register

1 GPIO_CLR_FAL_TRIG23 Register (Offset = 58h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-17655. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0058h**
GPIO1	**0060 1058h**
MCU_GPIO0	**0420 1058h**

Figure 14-5832. GPIO_CLR_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24
CLRFAL3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL2							
R/W1TC							
0h							

Table 14-17657. GPIO_CLR_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL3	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL2	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.23 GPIO_INTSTAT23 Register

1 GPIO_INTSTAT23 Register (Offset = 5Ch) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-17658. Instance Table

Instance Name	Physical Address
GPIO0	**0060 005Ch**
GPIO1	**0060 105Ch**
MCU_GPIO0	**0420 105Ch**

Figure 14-5833. GPIO_INTSTAT23 Name Register

31	30	29	28	27	26	25	24
STAT3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT2							
R/W1TC							
0h							

Table 14-17660. GPIO_INTSTAT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT3	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT2	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.1.2.2.24 GPIO_DIR45 Register

1 GPIO_DIR45 Register (Offset = 60h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-17661. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0060h**
GPIO1	**0060 1060h**
MCU_GPIO0	**0420 1060h**

Figure 14-5834. GPIO_DIR45 Name Register

31	30	29	28	27	26	25	24
DIR5							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR5							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR4							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR4							
R/W							
FFFFh							

Table 14-17663. GPIO_DIR45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR5	R/W	FFFFh	Direction of GPIO bank 5 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR4	R/W	FFFFh	Direction of GPIO bank 4 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.1.2.2.25 GPIO_OUT_DATA45 Register

1 GPIO_OUT_DATA45 Register (Offset = 64h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-17664. Instance Table

Instance Name	**Physical Address**
GPIO0	**0060 0064h**
GPIO1	**0060 1064h**
MCU_GPIO0	**0420 1064h**

Figure 14-5835. GPIO_OUT_DATA45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">OUT5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OUT5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUT4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUT4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17666. GPIO_OUT_DATA45 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:16	OUT5	R/W	0h	Output drive state of GPIO bank 5 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT4	R/W	0h	Output drive state of GPIO bank 4 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.26 GPIO_SET_DATA45 Register

1 GPIO_SET_DATA45 Register (Offset = 68h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-17667. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0068h**
GPIO1	**0060 1068h**
MCU_GPIO0	**0420 1068h**

Figure 14-5836. GPIO_SET_DATA45 Name Register

31	30	29	28	27	26	25	24
SET5							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET5							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET4							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET4							
R/W1TS							
0h							

Table 14-17669. GPIO_SET_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET5	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 5 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET4	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 4 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.27 GPIO_CLR_DATA45 Register

1 GPIO_CLR_DATA45 Register (Offset = 6Ch) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-17670. Instance Table

Instance Name	Physical Address
GPIO0	**0060 006Ch**
GPIO1	**0060 106Ch**
MCU_GPIO0	**0420 106Ch**

Figure 14-5837. GPIO_CLR_DATA45 Name Register

31	30	29	28	27	26	25	24
CLR5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR4							
R/W1TC							
0h							

Table 14-17672. GPIO_CLR_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR5	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR4	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.28 GPIO_IN_DATA45 Register

1 GPIO_IN_DATA45 Register (Offset = 70h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-17673. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0070h**
GPIO1	**0060 1070h**
MCU_GPIO0	**0420 1070h**

Figure 14-5838. GPIO_IN_DATA45 Name Register

31	30	29	28	27	26	25	24
IN5							
R							
0h							
23	22	21	20	19	18	17	16
IN5							
R							
0h							
15	14	13	12	11	10	9	8
IN4							
R							
0h							
7	6	5	4	3	2	1	0
IN4							
R							
0h							

Table 14-17675. GPIO_IN_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN5	R	0h	Status of GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	IN4	R	0h	Status of GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.29 GPIO_SET_RIS_TRIG45 Register

1 GPIO_SET_RIS_TRIG45 Register (Offset = 74h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-17676. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0074h**
GPIO1	**0060 1074h**
MCU_GPIO0	**0420 1074h**

Figure 14-5839. GPIO_SET_RIS_TRIG45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SETRIS5</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SETRIS5</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SETRIS4</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SETRIS4</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17678. GPIO_SET_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS5	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	SETRIS4	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.30 GPIO_CLR_RIS_TRIG45 Register

1 GPIO_CLR_RIS_TRIG45 Register (Offset = 78h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-17679. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0078h**
GPIO1	**0060 1078h**
MCU_GPIO0	**0420 1078h**

Figure 14-5840. GPIO_CLR_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24
CLRRIS5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS4							
R/W1TC							
0h							

Table 14-17681. GPIO_CLR_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS5	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS4	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.31 GPIO_SET_FAL_TRIG45 Register

1 GPIO_SET_FAL_TRIG45 Register (Offset = 7Ch) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-17682. Instance Table

Instance Name	Physical Address
GPIO0	**0060 007Ch**
GPIO1	**0060 107Ch**
MCU_GPIO0	**0420 107Ch**

Figure 14-5841. GPIO_SET_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24
SETFAL5							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL5							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL4							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL4							
R/W1TS							
0h							

Table 14-17684. GPIO_SET_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL5	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	SETFAL4	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.32 GPIO_CLR_FAL_TRIG45 Register

1 GPIO_CLR_FAL_TRIG45 Register (Offset = 80h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-17685. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0080h**
GPIO1	**0060 1080h**
MCU_GPIO0	**0420 1080h**

Figure 14-5842. GPIO_CLR_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24
CLRFAL5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL4							
R/W1TC							
0h							

Table 14-17687. GPIO_CLR_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL5	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL4	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.33 GPIO_INTSTAT45 Register

1 GPIO_INTSTAT45 Register (Offset = 84h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-17688. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0084h**
GPIO1	**0060 1084h**
MCU_GPIO0	**0420 1084h**

Figure 14-5843. GPIO_INTSTAT45 Name Register

31	30	29	28	27	26	25	24
STAT5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT4							
R/W1TC							
0h							

Table 14-17690. GPIO_INTSTAT45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT5	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT4	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.1.2.2.34 GPIO_DIR67 Register

1 GPIO_DIR67 Register (Offset = 88h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-17691. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0088h**
GPIO1	**0060 1088h**
MCU_GPIO0	**0420 1088h**

Figure 14-5844. GPIO_DIR67 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DIR7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DIR7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DIR6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DIR6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-17693. GPIO_DIR67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR7	R/W	FFFFh	Direction of GPIO bank 7 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR6	R/W	FFFFh	Direction of GPIO bank 6 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.1.2.2.35 GPIO_OUT_DATA67 Register

1 GPIO_OUT_DATA67 Register (Offset = 8Ch) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-17694. Instance Table

Instance Name	Physical Address
GPIO0	**0060 008Ch**
GPIO1	**0060 108Ch**
MCU_GPIO0	**0420 108Ch**

Figure 14-5845. GPIO_OUT_DATA67 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">OUT7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OUT7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUT6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUT6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17696. GPIO_OUT_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT7	R/W	0h	Output drive state of GPIO bank 7 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT6	R/W	0h	Output drive state of GPIO bank 6 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.36 GPIO_SET_DATA67 Register

1 GPIO_SET_DATA67 Register (Offset = 90h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-17697. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0090h**
GPIO1	**0060 1090h**
MCU_GPIO0	**0420 1090h**

Figure 14-5846. GPIO_SET_DATA67 Name Register

31	30	29	28	27	26	25	24
SET7							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET7							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET6							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET6							
R/W1TS							
0h							

Table 14-17699. GPIO_SET_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET7	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 7 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET6	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 6 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.37 GPIO_CLR_DATA67 Register

1 GPIO_CLR_DATA67 Register (Offset = 94h) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-17700. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0094h**
GPIO1	**0060 1094h**
MCU_GPIO0	**0420 1094h**

Figure 14-5847. GPIO_CLR_DATA67 Name Register

31	30	29	28	27	26	25	24
CLR7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR6							
R/W1TC							
0h							

Table 14-17702. GPIO_CLR_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR7	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR6	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.38 GPIO_IN_DATA67 Register

1 GPIO_IN_DATA67 Register (Offset = 98h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-17703. Instance Table

Instance Name	Physical Address
GPIO0	**0060 0098h**
GPIO1	**0060 1098h**
MCU_GPIO0	**0420 1098h**

Figure 14-5848. GPIO_IN_DATA67 Name Register

31	30	29	28	27	26	25	24
IN7							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN7							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IN6							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IN6							
R							
0h							

Table 14-17705. GPIO_IN_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN7	R	0h	Status of GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	IN6	R	0h	Status of GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.39 GPIO_SET_RIS_TRIG67 Register

1 GPIO_SET_RIS_TRIG67 Register (Offset = 9Ch) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-17706. Instance Table

Instance Name	Physical Address
GPIO0	**0060 009Ch**
GPIO1	**0060 109Ch**
MCU_GPIO0	**0420 109Ch**

Figure 14-5849. GPIO_SET_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24
SETRIS7							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS7							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS6							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS6							
R/W1TS							
0h							

Table 14-17708. GPIO_SET_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS7	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	SETRIS6	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.40 GPIO_CLR_RIS_TRIG67 Register

1 GPIO_CLR_RIS_TRIG67 Register (Offset = A0h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-17709. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00A0h**
GPIO1	**0060 10A0h**
MCU_GPIO0	**0420 10A0h**

Figure 14-5850. GPIO_CLR_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24
CLRRIS7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS6							
R/W1TC							
0h							

Table 14-17711. GPIO_CLR_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS7	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS6	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.41 GPIO_SET_FAL_TRIG67 Register

1 GPIO_SET_FAL_TRIG67 Register (Offset = A4h) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-17712. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00A4h**
GPIO1	**0060 10A4h**
MCU_GPIO0	**0420 10A4h**

Figure 14-5851. GPIO_SET_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24
SETFAL7							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL7							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL6							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL6							
R/W1TS							
0h							

Table 14-17714. GPIO_SET_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL7	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	SETFAL6	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.42 GPIO_CLR_FAL_TRIG67 Register

1 GPIO_CLR_FAL_TRIG67 Register (Offset = A8h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-17715. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00A8h**
GPIO1	**0060 10A8h**
MCU_GPIO0	**0420 10A8h**

Figure 14-5852. GPIO_CLR_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24
CLRFAL7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL6							
R/W1TC							
0h							

Table 14-17717. GPIO_CLR_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL7	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL6	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.43 GPIO_INTSTAT67 Register

1 GPIO_INTSTAT67 Register (Offset = ACh) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-17718. Instance Table

Instance Name	Physical Address
GPIO0	0060 00ACh
GPIO1	0060 10ACh
MCU_GPIO0	0420 10ACh

Figure 14-5853. GPIO_INTSTAT67 Name Register

31	30	29	28	27	26	25	24
STAT7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT6							
R/W1TC							
0h							

Table 14-17720. GPIO_INTSTAT67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT7	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT6	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.1.2.2.44 GPIO_DIR8 Register

1 GPIO_DIR8 Register (Offset = B0h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-17721. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00B0h**
GPIO1	**0060 10B0h**
MCU_GPIO0	**0420 10B0h**

Figure 14-5854. GPIO_DIR8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
FFFFh							
23	22	21	20	19	18	17	16
RESERVED							
R							
FFFFh							
15	14	13	12	11	10	9	8
DIR8							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR8							
R/W							
FFFFh							

Table 14-17723. GPIO_DIR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	FFFFh	RESERVED
15:0	DIR8	R/W	FFFFh	Direction of GPIO bank 8 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.9.1.2.2.45 GPIO_OUT_DATA8 Register

1 GPIO_OUT_DATA8 Register (Offset = B4h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-17724. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00B4h**
GPIO1	**0060 10B4h**
MCU_GPIO0	**0420 10B4h**

Figure 14-5855. GPIO_OUT_DATA8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUT8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUT8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17726. GPIO_OUT_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	OUT8	R/W	0h	Output drive state of GPIO bank 8 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.46 GPIO_SET_DATA8 Register

1 GPIO_SET_DATA8 Register (Offset = B8h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-17727. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00B8h**
GPIO1	**0060 10B8h**
MCU_GPIO0	**0420 10B8h**

Figure 14-5856. GPIO_SET_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
SET8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET8							
R/W1TS							
0h							

Table 14-17729. GPIO_SET_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	SET8	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 8 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.47 GPIO_CLR_DATA8 Register

1 GPIO_CLR_DATA8 Register (Offset = BCh) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-17730. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00BCh**
GPIO1	**0060 10BCh**
MCU_GPIO0	**0420 10BCh**

Figure 14-5857. GPIO_CLR_DATA8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLR8</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLR8</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17732. GPIO_CLR_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	CLR8	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.9.1.2.2.48 GPIO_IN_DATA8 Register

1 GPIO_IN_DATA8 Register (Offset = C0h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-17733. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00C0h**
GPIO1	**0060 10C0h**
MCU_GPIO0	**0420 10C0h**

Figure 14-5858. GPIO_IN_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
IN8							
R							
0h							
7	6	5	4	3	2	1	0
IN8							
R							
0h							

Table 14-17735. GPIO_IN_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	IN8	R	0h	Status of GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.49 GPIO_SET_RIS_TRIG8 Register

1 GPIO_SET_RIS_TRIG8 Register (Offset = C4h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-17736. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00C4h**
GPIO1	**0060 10C4h**
MCU_GPIO0	**0420 10C4h**

Figure 14-5859. GPIO_SET_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SETRIS8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS8							
R/W1TS							
0h							

Table 14-17738. GPIO_SET_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SETRIS8	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.50 GPIO_CLR_RIS_TRIG8 Register

1 GPIO_CLR_RIS_TRIG8 Register (Offset = C8h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-17739. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00C8h**
GPIO1	**0060 10C8h**
MCU_GPIO0	**0420 10C8h**

Figure 14-5860. GPIO_CLR_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLRRIS8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS8							
R/W1TC							
0h							

Table 14-17741. GPIO_CLR_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLRRIS8	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.51 GPIO_SET_FAL_TRIG8 Register

1 GPIO_SET_FAL_TRIG8 Register (Offset = CCh) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-17742. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00CCh**
GPIO1	**0060 10CCh**
MCU_GPIO0	**0420 10CCh**

Figure 14-5861. GPIO_SET_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SETFAL8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL8							
R/W1TS							
0h							

Table 14-17744. GPIO_SET_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SETFAL8	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.52 GPIO_CLR_FAL_TRIG8 Register

1 GPIO_CLR_FAL_TRIG8 Register (Offset = D0h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-17745. Instance Table

Instance Name	Physical Address
GPIO0	0060 00D0h
GPIO1	0060 10D0h
MCU_GPIO0	0420 10D0h

Figure 14-5862. GPIO_CLR_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLRFAL8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL8							
R/W1TC							
0h							

Table 14-17747. GPIO_CLR_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLRFAL8	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.9.1.2.2.53 GPIO_INTSTAT8 Register

1 GPIO_INTSTAT8 Register (Offset = D4h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-17748. Instance Table

Instance Name	Physical Address
GPIO0	**0060 00D4h**
GPIO1	**0060 10D4h**
MCU_GPIO0	**0420 10D4h**

Figure 14-5863. GPIO_INTSTAT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAT8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT8							
R/W1TC							
0h							

Table 14-17750. GPIO_INTSTAT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	STAT8	R/W1TC	0h	Status of GPIO bank 8 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.9.1.3 I2C Registers

Table 14-11889 lists the memory-mapped registers for the I2C registers. All register offset addresses not listed in Table 14-11889 should be considered as reserved locations and the register contents should not be modified.

Table 14-17751. I2C Instances

Instance	Base Address
I2C0_CFG	2000 0000h
I2C1_CFG	2001 0000h
I2C2_CFG	2002 0000h
I2C3_CFG	2003 0000h
MCU_I2C0_CFG	0490 0000h
MCU_I2C1_CFG	0491 0000h

Table 14-17752. I2C Registers

Offset	Acronym	Register Name	I2C0_CFG Physical Address	I2C1_CFG Physical Address	I2C2_CFG Physical Address
0h	I2C_REVNB_LO		2000 0000h	2001 0000h	2002 0000h
4h	I2C_REVNB_HI		2000 0004h	2001 0004h	2002 0004h
10h	I2C_SYSC		2000 0010h	2001 0010h	2002 0010h
20h	I2C_EOI		2000 0020h	2001 0020h	2002 0020h
24h	I2C_IRQSTATUS_RAW		2000 0024h	2001 0024h	2002 0024h
28h	I2C_IRQSTATUS		2000 0028h	2001 0028h	2002 0028h
2Ch	I2C_IRQENABLE_SET		2000 002Ch	2001 002Ch	2002 002Ch
30h	I2C_IRQENABLE_CLR		2000 0030h	2001 0030h	2002 0030h
34h	I2C_WE		2000 0034h	2001 0034h	2002 0034h
38h	I2C_DMARXENABLE_SET		2000 0038h	2001 0038h	2002 0038h
3Ch	I2C_DMATXENABLE_SET		2000 003Ch	2001 003Ch	2002 003Ch
40h	I2C_DMARXENABLE_CLR		2000 0040h	2001 0040h	2002 0040h
44h	I2C_DMATXENABLE_CLR		2000 0044h	2001 0044h	2002 0044h
48h	I2C_DMARXWAKE_EN		2000 0048h	2001 0048h	2002 0048h
4Ch	I2C_DMATXWAKE_EN		2000 004Ch	2001 004Ch	2002 004Ch
84h	I2C_IE		2000 0084h	2001 0084h	2002 0084h
88h	I2C_STAT		2000 0088h	2001 0088h	2002 0088h
90h	I2C_SYSS		2000 0090h	2001 0090h	2002 0090h
94h	I2C_BUF		2000 0094h	2001 0094h	2002 0094h
98h	I2C_CNT		2000 0098h	2001 0098h	2002 0098h
9Ch	I2C_DATA		2000 009Ch	2001 009Ch	2002 009Ch
A4h	I2C_CON		2000 00A4h	2001 00A4h	2002 00A4h
A8h	I2C_OA		2000 00A8h	2001 00A8h	2002 00A8h
ACh	I2C_SA		2000 00ACh	2001 00ACh	2002 00ACh
B0h	I2C_PSC		2000 00B0h	2001 00B0h	2002 00B0h
B4h	I2C_SCLL		2000 00B4h	2001 00B4h	2002 00B4h
B8h	I2C_SCLH		2000 00B8h	2001 00B8h	2002 00B8h
BCh	I2C_SYSTEST		2000 00BCh	2001 00BCh	2002 00BCh
C0h	I2C_BUFSTAT		2000 00C0h	2001 00C0h	2002 00C0h
C4h	I2C_OA1		2000 00C4h	2001 00C4h	2002 00C4h
C8h	I2C_OA2		2000 00C8h	2001 00C8h	2002 00C8h
CCh	I2C_OA3		2000 00CCh	2001 00CCh	2002 00CCh

Table 14-17752. I2C Registers (continued)

Offset	Acronym	Register Name	I2C0_CFG Physical Address	I2C1_CFG Physical Address	I2C2_CFG Physical Address
D0h	I2C_ACTOA		2000 00D0h	2001 00D0h	2002 00D0h
D4h	I2C_SBLOCK		2000 00D4h	2001 00D4h	2002 00D4h

Table 14-17753. I2C Registers

Offset	Acronym	Register Name	I2C3_CFG Physical Address	MCU_I2C0_CFG Physical Address	MCU_I2C1_CFG Physical Address
0h	I2C_REVNB_LO		2003 0000h	0490 0000h	0491 0000h
4h	I2C_REVNB_HI		2003 0004h	0490 0004h	0491 0004h
10h	I2C_SYSC		2003 0010h	0490 0010h	0491 0010h
20h	I2C_EOI		2003 0020h	0490 0020h	0491 0020h
24h	I2C_IRQSTATUS_RAW		2003 0024h	0490 0024h	0491 0024h
28h	I2C_IRQSTATUS		2003 0028h	0490 0028h	0491 0028h
2Ch	I2C_IRQENABLE_SET		2003 002Ch	0490 002Ch	0491 002Ch
30h	I2C_IRQENABLE_CLR		2003 0030h	0490 0030h	0491 0030h
34h	I2C_WE		2003 0034h	0490 0034h	0491 0034h
38h	I2C_DMARXENABLE_SET		2003 0038h	0490 0038h	0491 0038h
3Ch	I2C_DMATXENABLE_SET		2003 003Ch	0490 003Ch	0491 003Ch
40h	I2C_DMARXENABLE_CLR		2003 0040h	0490 0040h	0491 0040h
44h	I2C_DMATXENABLE_CLR		2003 0044h	0490 0044h	0491 0044h
48h	I2C_DMARXWAKE_EN		2003 0048h	0490 0048h	0491 0048h
4Ch	I2C_DMATXWAKE_EN		2003 004Ch	0490 004Ch	0491 004Ch
84h	I2C_IE		2003 0084h	0490 0084h	0491 0084h
88h	I2C_STAT		2003 0088h	0490 0088h	0491 0088h
90h	I2C_SYSS		2003 0090h	0490 0090h	0491 0090h
94h	I2C_BUF		2003 0094h	0490 0094h	0491 0094h
98h	I2C_CNT		2003 0098h	0490 0098h	0491 0098h
9Ch	I2C_DATA		2003 009Ch	0490 009Ch	0491 009Ch
A4h	I2C_CON		2003 00A4h	0490 00A4h	0491 00A4h
A8h	I2C_OA		2003 00A8h	0490 00A8h	0491 00A8h
ACh	I2C_SA		2003 00ACh	0490 00ACh	0491 00ACh
B0h	I2C_PSC		2003 00B0h	0490 00B0h	0491 00B0h
B4h	I2C_SCLL		2003 00B4h	0490 00B4h	0491 00B4h
B8h	I2C_SCLH		2003 00B8h	0490 00B8h	0491 00B8h
BCh	I2C_SYSTEST		2003 00BCh	0490 00BCh	0491 00BCh
C0h	I2C_BUFSTAT		2003 00C0h	0490 00C0h	0491 00C0h
C4h	I2C_OA1		2003 00C4h	0490 00C4h	0491 00C4h
C8h	I2C_OA2		2003 00C8h	0490 00C8h	0491 00C8h
CCh	I2C_OA3		2003 00CCh	0490 00CCh	0491 00CCh
D0h	I2C_ACTOA		2003 00D0h	0490 00D0h	0491 00D0h
D4h	I2C_SBLOCK		2003 00D4h	0490 00D4h	0491 00D4h

1 I2C_REVNB_LO Register (Offset = 0h) [reset = X]

I2C_REVNB_LO is shown in Figure 14-5864 and described in Table 14-11892.

Return to Summary Table.

Revision Number register (Low)

Table 14-17754. I2C_REVNB_LO Instances

Instance	Physical Address
I2C0_CFG	2000 0000h
I2C1_CFG	2001 0000h
I2C2_CFG	2002 0000h
I2C3_CFG	2003 0000h
MCU_I2C0_CFG	0490 0000h
MCU_I2C1_CFG	0491 0000h

Figure 14-5864. I2C_REVNB_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-1h					R-0h			R-0h		R-Ch					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17756. I2C_REVNB_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-11	RTL	R	1h	RTL version.
10-8	MAJOR	R	0h	Major Revision. This field changes when there is a major feature change. This field does not change due to bug fix, or minor feature change.
7-6	CUSTOM	R	0h	Indicates a special version for a particular device. Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers. 0 if non-custom.
5-0	MINOR	R	Ch	Minor Revision. This field changes when features are scaled up or down. This field does not change due to bug fix, or major feature change.

2 I2C_REVNB_HI Register (Offset = 4h) [reset = X]

I2C_REVNB_HI is shown in Figure 14-5865 and described in Table 14-11894.

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Revision Number register (High)

Table 14-17757. I2C_REVNB_HI Instances

Instance	Physical Address
I2C0_CFG	2000 0004h
I2C1_CFG	2001 0004h
I2C2_CFG	2002 0004h
I2C3_CFG	2003 0004h
MCU_I2C0_CFG	0490 0004h
MCU_I2C1_CFG	0491 0004h

Figure 14-5865. I2C_REVNB_HI Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SCHEME		RESERVED		FUNC			
R-1h		R-1h		R-40h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FUNC							
R-40h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17759. I2C_REVNB_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-14	SCHEME	R	1h	Used to distinguish between old Scheme and current. Spare bit to encode future schemes.
13-12	RESERVED	R	1h	Reads return 0x1.
11-0	FUNC	R	40h	Function: Indicates a software compatible module family.

3 I2C_SYSC Register (Offset = 10h) [reset = X]

I2C_SYSC is shown in Figure 14-5866 and described in Table 14-11896.

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System Configuration register

Table 14-17760. I2C_SYSC Instances

Instance	Physical Address
I2C0_CFG	2000 0010h
I2C1_CFG	2001 0010h
I2C2_CFG	2002 0010h
I2C3_CFG	2003 0010h
MCU_I2C0_CFG	0490 0010h
MCU_I2C1_CFG	0491 0010h

Figure 14-5866. I2C_SYSC Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CLKACTIVITY	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED			IDLEMODE		ENAWAKEUP	SRST	AUTOIDLE
R-0h			R/W-0h		R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17762. I2C_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved.
9-8	CLKACTIVITY	R/W	0h	Clock Activity selection bits. 0x0: Both clocks can be cut off. 0x1: Only OCP clock must be kept active; system clock can be cut off. 0x2: Only system clock must be kept active; OCP clock can be cut off. 0x3: Both clocks must be kept off.
7-5	RESERVED	R	0h	Reads return 0.

Table 14-17762. I2C_SYSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	IDLEMODE	R/W	0h	Idle Mode selection bits. 0x0: Force Idle mode. 0x1: No Idle mode. 0x2: Smart Idle mode. 0x3: smartidle_wakeup.
2	ENAWAKEUP	R/W	0h	Enable Wakeup control bit. 0: Wakeup mechanism is disabled. 1: Wakeup mechanism is enabled.
1	SRST	R/W	0h	SoftReset bit. 0: Normal mode. 1: The module is reset.
0	AUTOIDLE	R/W	1h	Autoidle bit.

4 I2C_EOI Register (Offset = 20h) [reset = X]

I2C_EOI is shown in Figure 14-5867 and described in Table 14-11898.

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End Of Interrupt number specification

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-17763. I2C_EOI Instances

Instance	Physical Address
I2C0_CFG	2000 0020h
I2C1_CFG	2001 0020h
I2C2_CFG	2002 0020h
I2C3_CFG	2003 0020h
MCU_I2C0_CFG	0490 0020h
MCU_I2C1_CFG	0491 0020h

Figure 14-5867. I2C_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							LINE_NUMBER
R-0h							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 14-17765. I2C_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved.
0	LINE_NUMBER	W	0h	Software End Of Interrupt [EOI] control. Write number of interrupt output.

5 I2C_IRQSTATUS_RAW Register (Offset = 24h) [reset = X]

I2C_IRQSTATUS_RAW is shown in Figure 14-5868 and described in Table 14-11900.

Return to Summary Table.

Per-event raw interrupt status vector

Table 14-17766. I2C_IRQSTATUS_RAW Instances

Instance	Physical Address
I2C0_CFG	2000 0024h
I2C1_CFG	2001 0024h
I2C2_CFG	2002 0024h
I2C3_CFG	2003 0024h
MCU_I2C0_CFG	0490 0024h
MCU_I2C1_CFG	0491 0024h

Figure 14-5868. I2C_IRQSTATUS_RAW Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17768. I2C_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility. Read returns 0.
14	XDR	R/W	0h	Transmit draining IRQ status. 0: Transmit draining inactive. 1: Transmit draining enabled.
13	RDR	R/W	0h	Receive draining IRQ status. 0: Receive draining inactive. 1: Receive draining enabled.
12	BB	R	0h	Bus busy status. Writing into this bit has no effect. Read 0: Bus is free. Read 1: Bus is occupied.

Table 14-17768. I2C_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ROVR	R/W	0h	Receive overrun status. Writing into this bit has no effect. Read 0: Normal operation. Read 1: Receiver overrun.
10	XUDF	R/W	0h	Transmit underflow status. Writing into this bit has no effect. Read 0: Normal operation. Read 1: Transmit underflow.
9	AAS	R/W	0h	Address recognized as target IRQ status. 0: No action. 1: Address recognized.
8	BF	R/W	0h	Bus Free IRQ status. 0: No action. 1: BusFree.
7	AERR	R/W	0h	Access Error IRQ status. 0: No action. 1: Access Error.
6	STC	R/W	0h	Start Condition IRQ status. 0: No action. 1: Start Condition detected.
5	GC	R/W	0h	General call IRQ status. Set to '1' by core when General call address detected and interrupt signaled to MPUSS. Write '1' to clear. 0: No general call detected. 1: General call address detected.
4	XRDY	R/W	0h	Transmit data ready IRQ status. Set to '1' by core when transmitter and when new data is requested. When set to '1' by core, an interrupt is signaled to MPUSS. Write '1' to clear. 0: Transmission ongoing. 1: Transmit data ready.
3	RRDY	R/W	0h	Receive data ready IRQ status. Set to '1' by core when receiver mode, a new data is able to be read. When set to '1' by core, an interrupt is signaled to MPUSS. Write '1' to clear. 0: No data available. 1: Receive data available.

Table 14-17768. I2C_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ARDY	R/W	0h	Register access ready IRQ status. When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPUSS. Write '1' to clear. 0: Module busy. 1: Access ready.
1	NACK	R/W	0h	No acknowledgement IRQ status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS. Write '1' to clear this bit. 0: Normal operation. 1: Not Acknowledge detected.
0	AL	R/W	0h	Arbitration lost IRQ status. This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS. During reads, it always returns 0. 0: Normal operation. 1: Arbitration lost detected.

6 I2C_IRQSTATUS Register (Offset = 28h) [reset = X]

I2C_IRQSTATUS is shown in Figure 14-5869 and described in Table 14-11902.

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Per-event enabled interrupt status vector

Table 14-17769. I2C_IRQSTATUS Instances

Instance	Physical Address
I2C0_CFG	2000 0028h
I2C1_CFG	2001 0028h
I2C2_CFG	2002 0028h
I2C3_CFG	2003 0028h
MCU_I2C0_CFG	0490 0028h
MCU_I2C1_CFG	0491 0028h

Figure 14-5869. I2C_IRQSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17771. I2C_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility. Read returns 0.
14	XDR	R/W	0h	Transmit draining IRQ enabled status. Write '1' to clear. 0: Transmit draining inactive. 1: Transmit draining enabled.
13	RDR	R/W	0h	Receive draining IRQ enabled status. Write '1' to clear. 0: Receive draining inactive. 1: Receive draining enabled.
12	BB	R	0h	Bus busy enabled status. Writing into this bit has no effect. Read 0: Bus is free. Read 1: Bus is occupied.

Table 14-17771. I2C_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ROVR	R/W	0h	Receive overrun enabled status. Writing into this bit has no effect. Read 0: Normal operation. Read 1: Receiver overrun.
10	XUDF	R/W	0h	Transmit underflow enabled status. Writing into this bit has no effect. Read 0: Normal operation. Read 1: Transmit underflow.
9	AAS	R/W	0h	Address recognized as target IRQ enabled status. Write '1' to clear. 0: No action. 1: Address recognized.
8	BF	R/W	0h	Bus Free IRQ enabled status. Write '1' to clear. 0: No action. 1: Bus Free.
7	AERR	R/W	0h	Access Error IRQ enabled status. Write '1' to clear. 0: No action. 1: Access Error.
6	STC	R/W	0h	Start Condition IRQ enabled status. Write '1' to clear. 0: No action. 1: Start Condition detected.
5	GC	R/W	0h	General call IRQ enabled status. Set to '1' by core when General call address detected and interrupt signaled to MPUSS. Write '1' to clear. 0: No general call detected. 1: General call address detected.
4	XRDY	R/W	0h	Transmit data ready IRQ enabled status. Set to '1' by core when transmitter and when new data is requested. When set to '1' by core, an interrupt is signaled to MPUSS. Write '1' to clear. 0: Transmission ongoing. 1: Transmit data ready.
3	RRDY	R/W	0h	Receive data ready IRQ enabled status. Set to '1' by core when receiver mode, a new data is able to be read. When set to '1' by core, an interrupt is signaled to MPUSS. Write '1' to clear. 0: No data available. 1: Receive data available.

Table 14-17771. I2C_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ARDY	R/W	0h	Register access ready IRQ enabled status. When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPUSS. Write '1' to clear. 0: Module busy. 1: Access ready.
1	NACK	R/W	0h	No acknowledgement IRQ enabled status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS. Write '1' to clear this bit. 0: Normal operation. 1: Not Acknowledge detected.
0	AL	R/W	0h	Arbitration lost IRQ enabled status. This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS. During reads, it always returns 0. Write '1' to clear. 0: Normal operation. 1: Arbitration lost detected.

7 I2C_IRQENABLE_SET Register (Offset = 2Ch) [reset = X]

I2C_IRQENABLE_SET is shown in Figure 14-5870 and described in Table 14-11904.

Return to Summary Table.

Per-event interrupt enable bit vector.

Table 14-17772. I2C_IRQENABLE_SET Instances

Instance	Physical Address
I2C0_CFG	2000 002Ch
I2C1_CFG	2001 002Ch
I2C2_CFG	2002 002Ch
I2C3_CFG	2003 002Ch
MCU_I2C0_CFG	0490 002Ch
MCU_I2C1_CFG	0491 002Ch

Figure 14-5870. I2C_IRQENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17774. I2C_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility. Read returns 0.
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]. 0: Transmit Draining interrupt disabled. 1: Transmit Draining interrupt enabled.
13	RDR_IE	R/W	0h	Receive Draining interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]. Receive Draining interrupt disbaled. Receive Draining interrupt enabled.
12	RESERVED	R	0h	Reserved.

Table 14-17774. I2C_IRQENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ROVR	R/W	0h	Receive overrun enable set. 0: Receive overrun interrupt disabled. 1: Receive overrun interrupt enabled.
10	XUDF	R/W	0h	Transmit underflow enable set. 0: Transmit underflow interrupt disabled. 1: Transmit underflow interrupt enabled.
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]. 0: Addressed as Target interrupt disabled. 1: Addressed as Target interrupt enabled.
8	BF_IE	R/W	0h	Bus Free interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]. 0: Bus Free interrupt disabled. 1: Bus Free interrupt enabled.
7	AERR_IE	R/W	0h	Access Error interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]. 0: Access Error interrupt disabled. 1: Access Error interrupt enabled.
6	STC_IE	R/W	0h	Start Condition interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]. 0: Start Condition interrupt disabled. 1: Start Condition interrupt enabled.
5	GC_IE	R/W	0h	General call Interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]. 0: General call interrupt disabled. 1: General call interrupt enabled.
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]. 0: Transmit data ready interrupt disabled. 1: Transmit data ready interrupt enabled.
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]. 0: Receive data ready interrupt disabled. 1: Receive data ready interrupt enabled.

Table 14-17774. I2C_IRQENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ARDY_IE	R/W	0h	Register access ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]. 0: Register access ready interrupt disabled. 1: Register access ready interrupt enabled.
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]. 0: Not acknowledge interrupt disabled. 1: Not acknowledge interrupt enabled.
0	AL_IE	R/W	0h	Arbitration lost interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]. 0: Arbitration lost interrupt disabled. 1: Arbitration lost interrupt enabled.

8 I2C_IRQENABLE_CLR Register (Offset = 30h) [reset = X]

I2C_IRQENABLE_CLR is shown in Figure 14-5871 and described in Table 14-11906.

Return to Summary Table.

Per-event interrupt clear bit vector.

Table 14-17775. I2C_IRQENABLE_CLR Instances

Instance	Physical Address
I2C0_CFG	2000 0030h
I2C1_CFG	2001 0030h
I2C2_CFG	2002 0030h
I2C3_CFG	2003 0030h
MCU_I2C0_CFG	0490 0030h
MCU_I2C1_CFG	0491 0030h

Figure 14-5871. I2C_IRQENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17777. I2C_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility. Read returns 0.
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]. 0: Transmit Draining interrupt disabled. 1: Transmit Draining interrupt enabled.
13	RDR_IE	R/W	0h	Receive Draining interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]. 0: Receive Draining interrupt disabled. 1: Receive Draining interrupt enabled.
12	RESERVED	R	0h	Reserved.

Table 14-17777. I2C_IRQENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ROVR	R/W	0h	Receive overrun enable clear. 0: Receive overrun interrupt disabled. 1: Receive overrup interrupt enabled.
10	XUDF	R/W	0h	Transmit underflow enable clear. 0: Transmit underflow interrupt disabled. 1: Transmit underflow interrupt enabled.
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]. 0: Addressed as Target interrupt disabled. 1: Addressed as Target interrupt enabled.
8	BF_IE	R/W	0h	Bus Free interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]. 0: Bus Free interrupt disabled. 1: Bus Free interrupt enabled.
7	AERR_IE	R/W	0h	Access Error interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]. 0: Access Error interrupt disabled. 1: Access Error interrupt enabled.
6	STC_IE	R/W	0h	Start Condition interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]. 0: Start Condition interrupt disabled. 1: Start Condition interrupt enabled.
5	GC_IE	R/W	0h	General call Interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]. 0: General call interrupt disabled. 1: General call interrupt enabled.
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]. 0: Transmit data ready interrupt disabled. 1: Transmit data ready interrupt enabled.
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]. 0: Receive data ready interrupt disabled. 1: Receive data ready interrupt enabled.

Table 14-17777. I2C_IRQENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ARDY_IE	R/W	0h	Register access ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]. 0: Register access ready interrupt disabled. 1: Register access ready interrupt enabled.
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]. 0: Not Acknowledge interrupt disabled. 1: Not Acknowledge interrupt enabled.
0	AL_IE	R/W	0h	Arbitration lost interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]. 0: Arbitration lost interrupt disabled. 1: Arbitration lost interrupt enabled.

9 I2C_WE Register (Offset = 34h) [reset = X]

I2C_WE is shown in Figure 14-5872 and described in Table 14-11908.

Return to Summary Table.

I2C wakeup enable vector (legacy).

Table 14-17778. I2C_WE Instances

Instance	Physical Address
I2C0_CFG	2000 0034h
I2C1_CFG	2001 0034h
I2C2_CFG	2002 0034h
I2C3_CFG	2003 0034h
MCU_I2C0_CFG	0490 0034h
MCU_I2C1_CFG	0491 0034h

Figure 14-5872. I2C_WE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17780. I2C_WE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R	0h	Reserved.
14	XDR	R/W	0h	Transmit Draining wakeup set. 0: Transmit draining wakeup disabled. 1: Transmit draining wakeup enabled.
13	RDR	R/W	0h	Receive Draining wakeup set. 0: Receive draining wakeup disabled. 1: Receive draining wakeup enabled.
12	RESERVED	R	0h	Reserved.

Table 14-17780. I2C_WE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ROVR	R/W	0h	Receive overrun wakeup set. 0: Receive overrun wakeup disabled. 1: Receive overrun wakeup enabled.
10	XUDF	R/W	0h	Transmit underflow wakeup set. 0: Transmit underflow wakeup disabled. 1: Transmit underflow wakeup enabled.
9	AAS	R/W	0h	Address as target IRQ wakeup set. 0: Addressed as target wakeup disabled. 1: Addressed as target wakeup enabled.
8	BF	R/W	0h	Bus Free IRQ wakeup set. 0: Bus Free wakeup disabled. 1: Bus Free wakeup enabled.
7	RESERVED	R	0h	Reserved.
6	STC	R/W	0h	Start Condition IRQ wakeup set. 0: Start condition wakeup disbaled. 1: Start condition wakeup enabled.
5	GC	R/W	0h	General call IRQ wakeup set. 0: General call wakeup disabled. 1: General call wakeup enabled.
4	RESERVED	R	0h	Reserved.
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set. 0: Transmit/receive data ready wakeup disabled. 1: Transmit/receive data ready wakeup enabled.
2	ARDY	R/W	0h	Register access ready IRQ wakeup set. 0: Register access ready wakeup disabled. 1: Register access ready wakeup enabled.
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set. 0: Not Acknowledge wakeup disabled. 1: Not Acknowledge wakeup enabled.
0	AL	R/W	0h	Arbitration lost IRQ wakeup set. 0: Arbitration lost wakeup disabled. 1: Arbitration lost wakeup enabled.

10 I2C_DMARXENABLE_SET Register (Offset = 38h) [reset = X]

I2C_DMARXENABLE_SET is shown in Figure 14-5873 and described in Table 14-11910.

Return to Summary Table.

Per-event DMA RX enable set.

Table 14-17781. I2C_DMARXENABLE_SET Instances

Instance	Physical Address
I2C0_CFG	2000 0038h
I2C1_CFG	2001 0038h
I2C2_CFG	2002 0038h
I2C3_CFG	2003 0038h
MCU_I2C0_CFG	0490 0038h
MCU_I2C1_CFG	0491 0038h

Figure 14-5873. I2C_DMARXENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DMARX_ENABLE_SET
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17783. I2C_DMARXENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved.
0	DMARX_ENABLE_SET	R/W	0h	Receive DMA channel enable set.

11 I2C_DMATXENABLE_SET Register (Offset = 3Ch) [reset = X]

I2C_DMATXENABLE_SET is shown in Figure 14-5874 and described in Table 14-11912.

Return to Summary Table.

Per-event DMA TX enable set.

Table 14-17784. I2C_DMATXENABLE_SET Instances

Instance	Physical Address
I2C0_CFG	2000 003Ch
I2C1_CFG	2001 003Ch
I2C2_CFG	2002 003Ch
I2C3_CFG	2003 003Ch
MCU_I2C0_CFG	0490 003Ch
MCU_I2C1_CFG	0491 003Ch

Figure 14-5874. I2C_DMATXENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							DMATX_ENABLE_SET
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17786. I2C_DMATXENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved.
0	DMATX_ENABLE_SET	R/W	0h	Transmit DMA channel enable set.

12 I2C_DMARXENABLE_CLR Register (Offset = 40h) [reset = X]

I2C_DMARXENABLE_CLR is shown in Figure 14-5875 and described in Table 14-11914.

Return to Summary Table.

Per-event DMA RX enable clear.

Table 14-17787. I2C_DMARXENABLE_CLR Instances

Instance	Physical Address
I2C0_CFG	2000 0040h
I2C1_CFG	2001 0040h
I2C2_CFG	2002 0040h
I2C3_CFG	2003 0040h
MCU_I2C0_CFG	0490 0040h
MCU_I2C1_CFG	0491 0040h

Figure 14-5875. I2C_DMARXENABLE_CLR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>DMARX_ENABLE_CLEAR</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17789. I2C_DMARXENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved.
0	DMARX_ENABLE_CLEAR	R/W	0h	Receive DMA channel enable clear.

13 I2C_DMATXENABLE_CLR Register (Offset = 44h) [reset = X]

I2C_DMATXENABLE_CLR is shown in Figure 14-5876 and described in Table 14-11916.

Return to Summary Table.

Per-event DMA TX enable clear.

Table 14-17790. I2C_DMATXENABLE_CLR Instances

Instance	Physical Address
I2C0_CFG	2000 0044h
I2C1_CFG	2001 0044h
I2C2_CFG	2002 0044h
I2C3_CFG	2003 0044h
MCU_I2C0_CFG	0490 0044h
MCU_I2C1_CFG	0491 0044h

Figure 14-5876. I2C_DMATXENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DMATX_ENABLE_CLEAR
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17792. I2C_DMATXENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved.
0	DMATX_ENABLE_CLEAR	R/W	0h	Transmit DMA channel enable clear.

14 I2C_DMARXWAKE_EN Register (Offset = 48h) [reset = X]

I2C_DMARXWAKE_EN is shown in Figure 14-5877 and described in Table 14-11918.

Return to Summary Table.

Per-event DMA RX wakeup enable.

Table 14-17793. I2C_DMARXWAKE_EN Instances

Instance	Physical Address
I2C0_CFG	2000 0048h
I2C1_CFG	2001 0048h
I2C2_CFG	2002 0048h
I2C3_CFG	2003 0048h
MCU_I2C0_CFG	0490 0048h
MCU_I2C1_CFG	0491 0048h

Figure 14-5877. I2C_DMARXWAKE_EN Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17795. I2C_DMARXWAKE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R	0h	Reserved.
14	XDR	R/W	0h	Transmit Draining wakeup set. 0: Transmit draining wakeup disabled. 1: Transmit draining wakeup enabled.
13	RDR	R/W	0h	Receive Draining wakeup set. 0: Receive draining wakeup disabled. 1: Receive draining wakeup enabled.
12	RESERVED	R	0h	Reserved.

Table 14-17795. I2C_DMARXWAKE_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ROVR	R/W	0h	Receive overrun wakeup set. 0: Receive overrun wakeup disabled. 1: Receive overrun wakeup enabled.
10	XUDF	R/W	0h	Transmit underflow wakeup set. 0: Transmit underflow wakeup disabled. 1: Transmit underflow wakeup enabled.
9	AAS	R/W	0h	Address as target IRQ wakeup set. 0: Addressed as target wakeup disabled. 1: Addressed as target wakeup enabled.
8	BF	R/W	0h	Bus Free IRQ wakeup set. 0: Bus Free wakeup disabled. 1: Bus Free wakeup enabled.
7	RESERVED	R	0h	Reserved.
6	STC	R/W	0h	Start Condition IRQ wakeup set. 0: Start condition wakeup disabled. 1: Start condition wakeup enabled.
5	GC	R/W	0h	General call IRQ wakeup set. 0: General call wakeup disabled. 1: General call wakeup enabled.
4	RESERVED	R	0h	Reserved.
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set. 0: Transmit/Receive data ready wakeup disabled. 1: Transmit/Receive data ready wakeup enabled
2	ARDY	R/W	0h	Register access ready IRQ wakeup set. 0: Register access ready wakeup disabled. 1: Register access ready wakeup enabled.
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set. 0: Not Acknowledge wakeup disbaled. 1: Not Acknowledge wakeup enabled.
0	AL	R/W	0h	Arbitration lost IRQ wakeup set. 0: Arbitration lost wakeup disabled. 1: Arbitration lost wakeup enabled.

15 I2C_DMATXWAKE_EN Register (Offset = 4Ch) [reset = X]

I2C_DMATXWAKE_EN is shown in Figure 14-5878 and described in Table 14-11920.

Return to Summary Table.

Per-event DMA TX wakeup enable.

Table 14-17796. I2C_DMATXWAKE_EN Instances

Instance	Physical Address
I2C0_CFG	2000 004Ch
I2C1_CFG	2001 004Ch
I2C2_CFG	2002 004Ch
I2C3_CFG	2003 004Ch
MCU_I2C0_CFG	0490 004Ch
MCU_I2C1_CFG	0491 004Ch

Figure 14-5878. I2C_DMATXWAKE_EN Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17798. I2C_DMATXWAKE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R	0h	Reserved.
14	XDR	R/W	0h	Transmit Draining wakeup set. 0: Transmit draining wakeup disabled. 1: Transmit draining wakeup enabled.
13	RDR	R/W	0h	Receive Draining wakeup set. 0: Receive draining wakeup disabled. 1: Receive draining wakeup enabled.
12	RESERVED	R	0h	Reserved.

Table 14-17798. I2C_DMATXWAKE_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ROVR	R/W	0h	Receive overrun wakeup set. 0: Receive overrun wakeup disabled. 1: Receive overrun wakeup enabled.
10	XUDF	R/W	0h	Transmit underflow wakeup set. 0: Transmit underflow wakeup disabled. 1: Transmit underflow wakeup enabled.
9	AAS	R/W	0h	Address as target IRQ wakeup set. 0: Addressed as target wakeup disabled. 1: Addressed as target wakeup enabled.
8	BF	R/W	0h	Bus Free IRQ wakeup set. 0: Bus Free wakeup disabled. 1: Bus Free wakeup enabled.
7	RESERVED	R	0h	Reserved.
6	STC	R/W	0h	Start Condition IRQ wakeup set. 0: Start condition wakeup disabled. 1: Start condition wakeup enabled.
5	GC	R/W	0h	General call IRQ wakeup set. 0: General call wakeup disabled. 1: General call wakeup enabled.
4	RESERVED	R	0h	Reserved.
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set. 0: Transmit/receive data ready wakeup. 1: Transmit/receive data ready wakeup.
2	ARDY	R/W	0h	Register access ready IRQ wakeup set. 0: Register access ready wakeup disabled. 1: Register access ready wakeup enabled.
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set. 0: Not Acknowledge wakeup disabled. 1: Not Acknowledge wakeup enabled.
0	AL	R/W	0h	Arbitration lost IRQ wakeup set. 0: Arbitration lost wakeup disabled. 1: Arbitration lost wakeup enabled.

16 I2C_IE Register (Offset = 84h) [reset = X]

I2C_IE is shown in Figure 14-5879 and described in Table 14-11922.

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I2C interrupt enable vector (legacy).

Table 14-17799. I2C_IE Instances

Instance	Physical Address
I2C0_CFG	2000 0084h
I2C1_CFG	2001 0084h
I2C2_CFG	2002 0084h
I2C3_CFG	2003 0084h
MCU_I2C0_CFG	0490 0084h
MCU_I2C1_CFG	0491 0084h

Figure 14-5879. I2C_IE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17801. I2C_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility. Read returns 0.
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR].
13	RDR_IE	R/W	0h	Receive Draining interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR].
12	RESERVED	R	0h	Reserved.
11	ROVR	R/W	0h	Receive overrun enable set.
10	XUDF	R/W	0h	Transmit underflow enable set.
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS].

Table 14-17801. I2C_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	BF_IE	R/W	0h	Bus Free interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[BF].
7	AERR_IE	R/W	0h	Access Error interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR].
6	STC_IE	R/W	0h	Start Condition interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[STC].
5	GC_IE	R/W	0h	General call Interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[GC].
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY].
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY].
2	ARDY_IE	R/W	0h	Register access ready interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY].
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK].
0	AL_IE	R/W	0h	Arbitration lost interrupt enable. Mask or unmask the interrupt signaled by bit in I2C_STAT[AL].

17 I2C_STAT Register (Offset = 88h) [reset = X]

I2C_STAT is shown in Figure 14-5880 and described in Table 14-11924.

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I2C interrupt status vector (legacy).

Table 14-17802. I2C_STAT Instances

Instance	Physical Address
I2C0_CFG	2000 0088h
I2C1_CFG	2001 0088h
I2C2_CFG	2002 0088h
I2C3_CFG	2003 0088h
MCU_I2C0_CFG	0490 0088h
MCU_I2C1_CFG	0491 0088h

Figure 14-5880. I2C_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17804. I2C_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility. Read returns 0.
14	XDR	R/W	0h	Transmit draining IRQ status.
13	RDR	R/W	0h	Receive draining IRQ status.
12	BB	R	0h	Bus busy status. Writing into this bit has no effect.
11	ROVR	R/W	0h	Receive overrun status. Writing into this bit has no effect.
10	XUDF	R/W	0h	Transmit underflow status. Writing into this bit has no effect.
9	AAS	R/W	0h	Address recognized as target IRQ status.
8	BF	R/W	0h	Bus Free IRQ status.
7	AERR	R/W	0h	Access Error IRQ status.

Table 14-17804. I2C_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	STC	R/W	0h	Start Condition IRQ status.
5	GC	R/W	0h	General call IRQ status. Set to '1' by core when General call address detected and interrupt signaled to MPUSS. Write '1' to clear.
4	XRDY	R/W	0h	Transmit data ready IRQ status. Set to '1' by core when transmitter and when new data is requested. When set to '1' by core, an interrupt is signaled to MPUSS. Write '1' to clear.
3	RRDY	R/W	0h	Receive data ready IRQ status. Set to '1' by core when receiver mode, a new data is able to be read. When set to '1' by core, an interrupt is signaled to MPUSS. Write '1' to clear.
2	ARDY	R/W	0h	Register access ready IRQ status. When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPUSS. Write '1' to clear.
1	NACK	R/W	0h	No acknowledgement IRQ status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS. Write '1' to clear this bit.
0	AL	R/W	0h	Arbitration lost IRQ status. This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS. During reads, it always returns 0.

18 I2C_SYSS Register (Offset = 90h) [reset = X]

I2C_SYSS is shown in Figure 14-5881 and described in Table 14-11926.

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System Status register

Table 14-17805. I2C_SYSS Instances

Instance	Physical Address
I2C0_CFG	2000 0090h
I2C1_CFG	2001 0090h
I2C2_CFG	2002 0090h
I2C3_CFG	2003 0090h
MCU_I2C0_CFG	0490 0090h
MCU_I2C1_CFG	0491 0090h

Figure 14-5881. I2C_SYSS Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RDONE
R-0h							R-1h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17807. I2C_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-1	RESERVED	R	0h	Reserved.
0	RDONE	R	1h	Reset done bit. Read 0: Internal module reset in on-going. Read 1: Reset completed.

19 I2C_BUF Register (Offset = 94h) [reset = X]

I2C_BUF is shown in Figure 14-5882 and described in Table 14-11928.

Return to Summary Table.

Buffer Configuration register

Table 14-17808. I2C_BUF Instances

Instance	Physical Address
I2C0_CFG	2000 0094h
I2C1_CFG	2001 0094h
I2C2_CFG	2002 0094h
I2C3_CFG	2003 0094h
MCU_I2C0_CFG	0490 0094h
MCU_I2C1_CFG	0491 0094h

Figure 14-5882. I2C_BUF Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RDMA_EN	RXFIFO_CLR	RXTRSH					
R/W-0h	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
XDMA_EN	TXFIFO_CLR	TXTRSH					
R/W-0h	R/W-0h	R/W-0h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-17810. I2C_BUF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RDMA_EN	R/W	0h	Receive DMA channel enable. 0: Receive DMA channel disabled. 1: Receive DMA channel enabled.
14	RXFIFO_CLR	R/W	0h	Receive FIFO clear. 0: Normal mode. 1: Rx FIFO is reset.
13-8	RXTRSH	R/W	0h	Threshold value for FIFO buffer in RX mode.
7	XDMA_EN	R/W	0h	Transmit DMA channel enable. 0: Transmit DMA channel disabled. 1: Transmit DMA channel enabled.

Table 14-17810. I2C_BUF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TXFIFO_CLR	R/W	0h	Transmit FIFO clear. 0: Normal mode. 1: Tx FIFO is reset.
5-0	TXTRSH	R/W	0h	Threshold value for FIFO buffer in TX mode.

20 I2C_CNT Register (Offset = 98h) [reset = X]

I2C_CNT is shown in Figure 14-5883 and described in Table 14-11930.

Return to Summary Table.

Data counter register

Table 14-17811. I2C_CNT Instances

Instance	Physical Address
I2C0_CFG	2000 0098h
I2C1_CFG	2001 0098h
I2C2_CFG	2002 0098h
I2C3_CFG	2003 0098h
MCU_I2C0_CFG	0490 0098h
MCU_I2C1_CFG	0491 0098h

Figure 14-5883. I2C_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DCOUNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17813. I2C_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	DCOUNT	R/W	0h	Data count.

21 I2C_DATA Register (Offset = 9Ch) [reset = X]

I2C_DATA is shown in Figure 14-5884 and described in Table 14-11932.

Return to Summary Table.

Data access register

Table 14-17814. I2C_DATA Instances

Instance	Physical Address
I2C0_CFG	2000 009Ch
I2C1_CFG	2001 009Ch
I2C2_CFG	2002 009Ch
I2C3_CFG	2003 009Ch
MCU_I2C0_CFG	0490 009Ch
MCU_I2C1_CFG	0491 009Ch

Figure 14-5884. I2C_DATA Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="8">RESERVED</td><td colspan="8">DATA</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="8">R-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17816. I2C_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	RESERVED	R	0h	Reserved.
7-0	DATA	R/W	0h	Transmit/Receive data FIFO endpoint.

22 I2C_CON Register (Offset = A4h) [reset = X]

I2C_CON is shown in Figure 14-5885 and described in Table 14-11934.

Return to Summary Table.

I2C configuration register.

Table 14-17817. I2C_CON Instances

Instance	Physical Address
I2C0_CFG	2000 00A4h
I2C1_CFG	2001 00A4h
I2C2_CFG	2002 00A4h
I2C3_CFG	2003 00A4h
MCU_I2C0_CFG	0490 00A4h
MCU_I2C1_CFG	0491 00A4h

Figure 14-5885. I2C_CON Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
I2C_EN	RESERVED	OPMODE		STB	MST	TRX	XSA
R/W-0h	R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
XOA0	XOA1	XOA2	XOA3	RESERVED		STP	STT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17819. I2C_CON Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	I2C_EN	R/W	0h	I2C module enable. 0: controller in reset. FIFO are cleared and status bits are set to their default value. 1: Module enabled.
14	RESERVED	R	0h	Reserved
13-12	OPMODE	R/W	0h	Operation mode selection. 0x0: I2C Fast/Standard mode. 0x1: I2C High Speed mode. 0x2: SCCB mode. 0x3: Reserved.

Table 14-17819. I2C_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	STB	R/W	0h	Start byte mode [controller mode only]. 0: Normal mode. 1: Start byte mode.
10	MST	R/W	0h	Controller/target mode. 0: Target mode. 1: Controller mode.
9	TRX	R/W	0h	Transmitter/Receiver mode [controller mode only]. 0: Received mode. 1: Transmitter mode.
8	XSA	R/W	0h	Expand Target address. 0: 7-bit address mode. 1: 10-bit address mode.
7	XOA0	R/W	0h	Expand Own address 0. 0: 7-bit address mode. 1: 10-bit address mode.
6	XOA1	R/W	0h	Expand Own address 1. 0: 7-bit address mode. 1: 10-bit address mode.
5	XOA2	R/W	0h	Expand Own address 2. 0: 7-bit address mode. 1: 10-bit address mode.
4	XOA3	R/W	0h	Expand Own address 3. 0: 7-bit address mode. 1: 10-bit address mode.
3-2	RESERVED	R	0h	Reserved.
1	STP	R/W	0h	Stop condition [controller mode only]. 0: No action or stop condition detected. 1: Stop condition queried.
0	STT	R/W	0h	Start condition [controller mode only]. 0: No action or start condition detected. 1: Start condition queried.

23 I2C_OA Register (Offset = A8h) [reset = X]

I2C_OA is shown in Figure 14-5886 and described in Table 14-11936.

Return to Summary Table.

Own address register

Table 14-17820. I2C_OA Instances

Instance	Physical Address
I2C0_CFG	2000 00A8h
I2C1_CFG	2001 00A8h
I2C2_CFG	2002 00A8h
I2C3_CFG	2003 00A8h
MCU_I2C0_CFG	0490 00A8h
MCU_I2C1_CFG	0491 00A8h

Figure 14-5886. I2C_OA Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">MCODE</td><td colspan="3">RESERVED</td><td colspan="10">OA</td></tr>
<tr><td colspan="3">R/W-0h</td><td colspan="3">R-0h</td><td colspan="10">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17822. I2C_OA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	MCODE	R/W	0h	Controller Code.
12-10	RESERVED	R	0h	Reserved.
9-0	OA	R/W	0h	Own address.

24 I2C_SA Register (Offset = ACh) [reset = X]

I2C_SA is shown in Figure 14-5887 and described in Table 14-11938.

Return to Summary Table.

Target address register

Table 14-17823. I2C_SA Instances

Instance	Physical Address
I2C0_CFG	2000 00ACh
I2C1_CFG	2001 00ACh
I2C2_CFG	2002 00ACh
I2C3_CFG	2003 00ACh
MCU_I2C0_CFG	0490 00ACh
MCU_I2C1_CFG	0491 00ACh

Figure 14-5887. I2C_SA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SA									
R-0h						R/W-3FFh									

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17825. I2C_SA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved.
9-0	SA	R/W	3FFh	Target address.

25 I2C_PSC Register (Offset = B0h) [reset = X]

I2C_PSC is shown in Figure 14-5888 and described in Table 14-11940.

Return to Summary Table.

I2C Clock Prescaler Register

Table 14-17826. I2C_PSC Instances

Instance	Physical Address
I2C0_CFG	2000 00B0h
I2C1_CFG	2001 00B0h
I2C2_CFG	2002 00B0h
I2C3_CFG	2003 00B0h
MCU_I2C0_CFG	0490 00B0h
MCU_I2C1_CFG	0491 00B0h

Figure 14-5888. I2C_PSC Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="8">RESERVED</td><td colspan="8">PSC</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="8">R-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17828. I2C_PSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	RESERVED	R	0h	Reserved.
7-0	PSC	R/W	0h	Fast/Standard mode prescale sampling clock divider value. 0x0: Divide by 1. 0x1: Divide by 2. .... 0xFF: Divide by 256.

26 I2C_SCLL Register (Offset = B4h) [reset = X]

I2C_SCLL is shown in Figure 14-5889 and described in Table 14-11942.

Return to Summary Table.

I2C SCL Low Time Register.

Table 14-17829. I2C_SCLL Instances

Instance	Physical Address
I2C0_CFG	2000 00B4h
I2C1_CFG	2001 00B4h
I2C2_CFG	2002 00B4h
I2C3_CFG	2003 00B4h
MCU_I2C0_CFG	0490 00B4h
MCU_I2C1_CFG	0491 00B4h

Figure 14-5889. I2C_SCLL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSSCLL								SCLL							
R/W-X																R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17831. I2C_SCLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	HSSCLL	R/W	0h	High Speed mode SCL low time.
7-0	SCLL	R/W	0h	Fast/Standard mode SCL low time.

27 I2C_SCLH Register (Offset = B8h) [reset = X]

I2C_SCLH is shown in Figure 14-5890 and described in Table 14-11944.

Return to Summary Table.

I2C SCL High Time Register.

Table 14-17832. I2C_SCLH Instances

Instance	Physical Address
I2C0_CFG	2000 00B8h
I2C1_CFG	2001 00B8h
I2C2_CFG	2002 00B8h
I2C3_CFG	2003 00B8h
MCU_I2C0_CFG	0490 00B8h
MCU_I2C1_CFG	0491 00B8h

Figure 14-5890. I2C_SCLH Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="8">HSSCLH</td><td colspan="8">SCLH</td></tr>
<tr><td colspan="16">R/W-X</td><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-17834. I2C_SCLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	HSSCLH	R/W	0h	High Speed mode SCL high time.
7-0	SCLH	R/W	0h	Fast/Standard mode SCL high time.

28 I2C_SYSTEST Register (Offset = BCh) [reset = X]

I2C_SYSTEST is shown in Figure 14-5891 and described in Table 14-11946.

Return to Summary Table.

I2C System Test Register.

Table 14-17835. I2C_SYSTEST Instances

Instance	Physical Address
I2C0_CFG	2000 00BCh
I2C1_CFG	2001 00BCh
I2C2_CFG	2002 00BCh
I2C3_CFG	2003 00BCh
MCU_I2C0_CFG	0490 00BCh
MCU_I2C1_CFG	0491 00BCh

Figure 14-5891. I2C_SYSTEST Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ST_EN	FREE	TMODE		SSB	RESERVED		SCL_I_FUNC
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R-0h		R-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SCL_O_FUNC	SDA_I_FUNC	SDA_O_FUNC	SCCB_E_O	SCL_I	SCL_O	SDA_I	SDA_O
R-1h	R-1h	R-1h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17837. I2C_SYSTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	ST_EN	R/W	0h	System test enable. 0: Normal mode. All other bits in register are read only. 1: System test enabled. Permit other sytsem test register bits to be set.
14	FREE	R/W	0h	Free running mode [on breakpoint]. 0: Stop mode [on breakpoint condition]. If Controller mode, it stops after completion of the on-going bit transfer. In target mode, it stops during the phase transfer when 1 byte is completely transmitted/ received. 1: Free running mode

Table 14-17837. I2C_SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	TMODE	R/W	0h	Test mode select. 0x0: Functional mode [default]. 0x1: Reserved. 0x2: Test of SCL counters [SCLL, SCLH, PSC]. SCL provides a permanent clock with controller mode. 0x3: Loop back mode select + SDA/SCL IO mode select.
11	SSB	R/W	0h	Set status bits. 0: No action. 1: Set all interrupt status bits to 1.
10-9	RESERVED	R	0h	Reserved
8	SCL_I_FUNC	R	1h	SCL line input value [functional mode]. Read 0: Read 0 from SCL line. Read 1: Read 1 from SCL line.
7	SCL_O_FUNC	R	1h	SCL line output value [functional mode]. Read 0: Driven 0 on SCL line. Read 1: Driven 1 on SCL line.
6	SDA_I_FUNC	R	1h	SDA line input value [functional mode]. Read 0: Read 0 from SDA line. Read 1: Read 1 from SDA line.
5	SDA_O_FUNC	R	1h	SDA line output value [functional mode]. Read 0: Driven 0 to SDA line. Read 1: Driven 1 to SDA line.
4	SCCB_E_O	R/W	0h	SCCB_E line sense output value. 0: Write 0 to SCCBE line. 1: Write 1 to SCCBE line.
3	SCL_I	R	0h	SCL line sense input value. Read 0: Read 0 from SCL line. Read 1: Read 1 from SCL line.
2	SCL_O	R/W	0h	SCL line drive output value. 0: Write 0 to SCL line. 1: Write 1 to SCL line.
1	SDA_I	R	0h	SDA line sense input value. Read 0: Read 0 from SDA line. Read 1: Read 1 from SDA line.

Table 14-17837. I2C_SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SDA_O	R/W	0h	SDA line drive output value. 0: Write 0 to SDA line. 1: Write 1 to SDA line.

29 I2C_BUFSTAT Register (Offset = C0h) [reset = X]

I2C_BUFSTAT is shown in Figure 14-5892 and described in Table 14-11948.

Return to Summary Table.

I2C Buffer Status Register.

Table 14-17838. I2C_BUFSTAT Instances

Instance	Physical Address
I2C0_CFG	2000 00C0h
I2C1_CFG	2001 00C0h
I2C2_CFG	2002 00C0h
I2C3_CFG	2003 00C0h
MCU_I2C0_CFG	0490 00C0h
MCU_I2C1_CFG	0491 00C0h

Figure 14-5892. I2C_BUFSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FIFODEPTH		RXSTAT					
R-2h		R-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TXSTAT					
R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17840. I2C_BUFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-14	FIFODEPTH	R	2h	Internal FIFO buffers depth. Read 0x0: 8-bytes FIFO. Read 0x1: 16-bytes FIFO. Read 0x2: 32-bytes FIFO. Read 0x3: 64-bytes FIFO.
13-8	RXSTAT	R	0h	RX Buffer Status.
7-6	RESERVED	R	0h	Reserved.
5-0	TXSTAT	R	0h	TX Buffer Status.

30 I2C_OA1 Register (Offset = C4h) [reset = X]

I2C_OA1 is shown in Figure 14-5893 and described in Table 14-11950.

Return to Summary Table.

I2C Own Address 1 Register

Table 14-17841. I2C_OA1 Instances

Instance	Physical Address
I2C0_CFG	2000 00C4h
I2C1_CFG	2001 00C4h
I2C2_CFG	2002 00C4h
I2C3_CFG	2003 00C4h
MCU_I2C0_CFG	0490 00C4h
MCU_I2C1_CFG	0491 00C4h

Figure 14-5893. I2C_OA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						OA1									
R-0h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17843. I2C_OA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved.
9-0	OA1	R/W	0h	Own address 1.

31 I2C_OA2 Register (Offset = C8h) [reset = X]

I2C_OA2 is shown in Figure 14-5894 and described in Table 14-11952.

Return to Summary Table.

I2C Own Address 2 Register

Table 14-17844. I2C_OA2 Instances

Instance	Physical Address
I2C0_CFG	2000 00C8h
I2C1_CFG	2001 00C8h
I2C2_CFG	2002 00C8h
I2C3_CFG	2003 00C8h
MCU_I2C0_CFG	0490 00C8h
MCU_I2C1_CFG	0491 00C8h

Figure 14-5894. I2C_OA2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R/W-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="10">OA2</td></tr>
<tr><td colspan="6">R-0h</td><td colspan="10">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17846. I2C_OA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved.
9-0	OA2	R/W	0h	Own address 2.

32 I2C_OA3 Register (Offset = CCh) [reset = X]

I2C_OA3 is shown in Figure 14-5895 and described in Table 14-11954.

Return to Summary Table.

I2C Own Address 3 Register

Table 14-17847. I2C_OA3 Instances

Instance	Physical Address
I2C0_CFG	2000 00CCh
I2C1_CFG	2001 00CCh
I2C2_CFG	2002 00CCh
I2C3_CFG	2003 00CCh
MCU_I2C0_CFG	0490 00CCh
MCU_I2C1_CFG	0491 00CCh

Figure 14-5895. I2C_OA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						OA3									
R-0h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17849. I2C_OA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved.
9-0	OA3	R/W	0h	Own address 3.

33 I2C_ACTOA Register (Offset = D0h) [reset = X]

I2C_ACTOA is shown in Figure 14-5896 and described in Table 14-11956.

Return to Summary Table.

I2C Active Own Address Register.

Table 14-17850. I2C_ACTOA Instances

Instance	Physical Address
I2C0_CFG	2000 00D0h
I2C1_CFG	2001 00D0h
I2C2_CFG	2002 00D0h
I2C3_CFG	2003 00D0h
MCU_I2C0_CFG	0490 00D0h
MCU_I2C1_CFG	0491 00D0h

Figure 14-5896. I2C_ACTOA Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				OA3_ACT	OA2_ACT	OA1_ACT	OA0_ACT
R-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-17852. I2C_ACTOA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-4	RESERVED	R	0h	Reserved.
3	OA3_ACT	R	0h	Own Address 3 active. Read 0: Own Address inactive. Read 1: Own Address active.
2	OA2_ACT	R	0h	Own Address 2 active. Read 0: Own Address inactive. Read 1: Own Address active.
1	OA1_ACT	R	0h	Own Address 1 active. Read 0: Own Address inactive. Read 1: Own Address active.

Table 14-17852. I2C_ACTOA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OA0_ACT	R	0h	Own Address 0 active. Read 0: Own Address inactive. Read 1: Own Address active.

34 I2C_SBLOCK Register (Offset = D4h) [reset = X]

I2C_SBLOCK is shown in Figure 14-5897 and described in Table 14-11958.

Return to Summary Table.

I2C Clock Blocking Enable Register.

Table 14-17853. I2C_SBLOCK Instances

Instance	Physical Address
I2C0_CFG	2000 00D4h
I2C1_CFG	2001 00D4h
I2C2_CFG	2002 00D4h
I2C3_CFG	2003 00D4h
MCU_I2C0_CFG	0490 00D4h
MCU_I2C1_CFG	0491 00D4h

Figure 14-5897. I2C_SBLOCK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				OA3_EN	OA2_EN	OA1_EN	OA0_EN
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-17855. I2C_SBLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-4	RESERVED	R	0h	Reserved.
3	OA3_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 3. 0: I2C Clock Released. 1: I2C Clock Blocked.
2	OA2_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 2. 0: I2C Clock Released. 1: I2C Clock Blocked.
1	OA1_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 1. 0: I2C Clock Released. 1: I2C Clock Blocked.

Table 14-17855. I2C_SBLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OA0_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 0. 0: I2C Clock Released. 1: I2C Clock Blocked.

14.9.1.4 MCSPI

MCSPI

14.9.1.4.1 MCSPI Summaries

MCSPI Summaries

Table 14-17856. MCSPI Registers, Base Address=2010 0000h, Length=1024

Offset	Length	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
0h	32	MCSPI_HL_REV	2010 0000h	2011 0000h	2012 0000h
4h	32	MCSPI_HL_HWINFO	2010 0004h	2011 0004h	2012 0004h
10h	32	MCSPI_HL_SYSCONFIG	2010 0010h	2011 0010h	2012 0010h
100h	32	MCSPI_REVISION	2010 0100h	2011 0100h	2012 0100h
110h	32	MCSPI_SYSCONFIG	2010 0110h	2011 0110h	2012 0110h
114h	32	MCSPI_SYSSTATUS	2010 0114h	2011 0114h	2012 0114h
118h	32	MCSPI_IRQSTATUS	2010 0118h	2011 0118h	2012 0118h
11Ch	32	MCSPI_IRQENABLE	2010 011Ch	2011 011Ch	2012 011Ch
120h	32	MCSPI_WAKEUPENABLE	2010 0120h	2011 0120h	2012 0120h
124h	32	MCSPI_SYST	2010 0124h	2011 0124h	2012 0124h
128h	32	MCSPI_MODULCTRL	2010 0128h	2011 0128h	2012 0128h
12Ch	32	MCSPI_CH0CONF	2010 012Ch	2011 012Ch	2012 012Ch
130h	32	MCSPI_CH0STAT	2010 0130h	2011 0130h	2012 0130h
134h	32	MCSPI_CH0CTRL	2010 0134h	2011 0134h	2012 0134h
138h	32	MCSPI_TX0	2010 0138h	2011 0138h	2012 0138h
13Ch	32	MCSPI_RX0	2010 013Ch	2011 013Ch	2012 013Ch
140h	32	MCSPI_CH1CONF	2010 0140h	2011 0140h	2012 0140h
144h	32	MCSPI_CH1STAT	2010 0144h	2011 0144h	2012 0144h
148h	32	MCSPI_CH1CTRL	2010 0148h	2011 0148h	2012 0148h
14Ch	32	MCSPI_TX1	2010 014Ch	2011 014Ch	2012 014Ch
150h	32	MCSPI_RX1	2010 0150h	2011 0150h	2012 0150h
154h	32	MCSPI_CH2CONF	2010 0154h	2011 0154h	2012 0154h
158h	32	MCSPI_CH2STAT	2010 0158h	2011 0158h	2012 0158h
15Ch	32	MCSPI_CH2CTRL	2010 015Ch	2011 015Ch	2012 015Ch
160h	32	MCSPI_TX2	2010 0160h	2011 0160h	2012 0160h
164h	32	MCSPI_RX2	2010 0164h	2011 0164h	2012 0164h
168h	32	MCSPI_CH3CONF	2010 0168h	2011 0168h	2012 0168h
16Ch	32	MCSPI_CH3STAT	2010 016Ch	2011 016Ch	2012 016Ch
170h	32	MCSPI_CH3CTRL	2010 0170h	2011 0170h	2012 0170h
174h	32	MCSPI_TX3	2010 0174h	2011 0174h	2012 0174h
178h	32	MCSPI_RX3	2010 0178h	2011 0178h	2012 0178h
17Ch	32	MCSPI_XFERLEVEL	2010 017Ch	2011 017Ch	2012 017Ch
180h	32	MCSPI_DAFTX	2010 0180h	2011 0180h	2012 0180h
1A0h	32	MCSPI_DAFRX	2010 01A0h	2011 01A0h	2012 01A0h

Table 14-17857. MCSPI Registers, Base Address=2010 0000h, Length=1024

Offset	Length	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address	MCU_MCSPI0 Physical Address
0h	32	MCSPI_HL_REV	2013 0000h	2014 0000h	04B0 0000h
4h	32	MCSPI_HL_HWINFO	2013 0004h	2014 0004h	04B0 0004h
10h	32	MCSPI_HL_SYSCONFIG	2013 0010h	2014 0010h	04B0 0010h
100h	32	MCSPI_REVISION	2013 0100h	2014 0100h	04B0 0100h
110h	32	MCSPI_SYSCONFIG	2013 0110h	2014 0110h	04B0 0110h
114h	32	MCSPI_SYSSTATUS	2013 0114h	2014 0114h	04B0 0114h
118h	32	MCSPI_IRQSTATUS	2013 0118h	2014 0118h	04B0 0118h
11Ch	32	MCSPI_IRQENABLE	2013 011Ch	2014 011Ch	04B0 011Ch
120h	32	MCSPI_WAKEUPENABLE	2013 0120h	2014 0120h	04B0 0120h
124h	32	MCSPI_SYST	2013 0124h	2014 0124h	04B0 0124h
128h	32	MCSPI_MODULCTRL	2013 0128h	2014 0128h	04B0 0128h
12Ch	32	MCSPI_CH0CONF	2013 012Ch	2014 012Ch	04B0 012Ch
130h	32	MCSPI_CH0STAT	2013 0130h	2014 0130h	04B0 0130h
134h	32	MCSPI_CH0CTRL	2013 0134h	2014 0134h	04B0 0134h
138h	32	MCSPI_TX0	2013 0138h	2014 0138h	04B0 0138h
13Ch	32	MCSPI_RX0	2013 013Ch	2014 013Ch	04B0 013Ch
140h	32	MCSPI_CH1CONF	2013 0140h	2014 0140h	04B0 0140h
144h	32	MCSPI_CH1STAT	2013 0144h	2014 0144h	04B0 0144h
148h	32	MCSPI_CH1CTRL	2013 0148h	2014 0148h	04B0 0148h
14Ch	32	MCSPI_TX1	2013 014Ch	2014 014Ch	04B0 014Ch
150h	32	MCSPI_RX1	2013 0150h	2014 0150h	04B0 0150h
154h	32	MCSPI_CH2CONF	2013 0154h	2014 0154h	04B0 0154h
158h	32	MCSPI_CH2STAT	2013 0158h	2014 0158h	04B0 0158h
15Ch	32	MCSPI_CH2CTRL	2013 015Ch	2014 015Ch	04B0 015Ch
160h	32	MCSPI_TX2	2013 0160h	2014 0160h	04B0 0160h
164h	32	MCSPI_RX2	2013 0164h	2014 0164h	04B0 0164h
168h	32	MCSPI_CH3CONF	2013 0168h	2014 0168h	04B0 0168h
16Ch	32	MCSPI_CH3STAT	2013 016Ch	2014 016Ch	04B0 016Ch
170h	32	MCSPI_CH3CTRL	2013 0170h	2014 0170h	04B0 0170h
174h	32	MCSPI_TX3	2013 0174h	2014 0174h	04B0 0174h
178h	32	MCSPI_RX3	2013 0178h	2014 0178h	04B0 0178h
17Ch	32	MCSPI_XFERLEVEL	2013 017Ch	2014 017Ch	04B0 017Ch
180h	32	MCSPI_DAFTX	2013 0180h	2014 0180h	04B0 0180h
1A0h	32	MCSPI_DAFRX	2013 01A0h	2014 01A0h	04B0 01A0h

Table 14-17858. MCSPI Registers, Base Address=2010 0000h, Length=1024

Offset	Length	Register Name	MCU_MCSPI1 Physical Address
0h	32	MCSPI_HL_REV	04B1 0000h
4h	32	MCSPI_HL_HWINFO	04B1 0004h
10h	32	MCSPI_HL_SYSCONFIG	04B1 0010h
100h	32	MCSPI_REVISION	04B1 0100h
110h	32	MCSPI_SYSCONFIG	04B1 0110h
114h	32	MCSPI_SYSSTATUS	04B1 0114h
118h	32	MCSPI_IRQSTATUS	04B1 0118h

Table 14-17858. MCSPI Registers, Base Address=2010 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCU_MCSPI1 Physical Address
11Ch	32	MCSPI_IRQENABLE	04B1 011Ch
120h	32	MCSPI_WAKEUPENABLE	04B1 0120h
124h	32	MCSPI_SYST	04B1 0124h
128h	32	MCSPI_MODULCTRL	04B1 0128h
12Ch	32	MCSPI_CH0CONF	04B1 012Ch
130h	32	MCSPI_CH0STAT	04B1 0130h
134h	32	MCSPI_CH0CTRL	04B1 0134h
138h	32	MCSPI_TX0	04B1 0138h
13Ch	32	MCSPI_RX0	04B1 013Ch
140h	32	MCSPI_CH1CONF	04B1 0140h
144h	32	MCSPI_CH1STAT	04B1 0144h
148h	32	MCSPI_CH1CTRL	04B1 0148h
14Ch	32	MCSPI_TX1	04B1 014Ch
150h	32	MCSPI_RX1	04B1 0150h
154h	32	MCSPI_CH2CONF	04B1 0154h
158h	32	MCSPI_CH2STAT	04B1 0158h
15Ch	32	MCSPI_CH2CTRL	04B1 015Ch
160h	32	MCSPI_TX2	04B1 0160h
164h	32	MCSPI_RX2	04B1 0164h
168h	32	MCSPI_CH3CONF	04B1 0168h
16Ch	32	MCSPI_CH3STAT	04B1 016Ch
170h	32	MCSPI_CH3CTRL	04B1 0170h
174h	32	MCSPI_TX3	04B1 0174h
178h	32	MCSPI_RX3	04B1 0178h
17Ch	32	MCSPI_XFERLEVEL	04B1 017Ch
180h	32	MCSPI_DAFTX	04B1 0180h
1A0h	32	MCSPI_DAFRX	04B1 01A0h

14.9.1.4.2 MCSPI Registers

MCSPI Registers

14.9.1.4.2.1 MCSPI_HL_REV Register

1 MCSPI_HL_REV Register (Offset = 0h) [reset = 40301A0Bh]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-17859. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0000h**
MCSPI1	**2011 0000h**
MCSPI2	**2012 0000h**
MCSPI3	**2013 0000h**
MCSPI4	**2014 0000h**
MCU_MCSPI0	**04B0 0000h**
MCU_MCSPI1	**04B1 0000h**

Figure 14-5898. MCSPI_HL_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		RSVD		FUNC			
R		R		R			
1h		0h		30h			
23	22	21	20	19	18	17	16
FUNC							
R							
30h							
15	14	13	12	11	10	9	8
R_RTL					X_MAJOR		
R					R		
3h					2h		
7	6	5	4	3	2	1	0
CUSTOM		Y_MINOR					
R		R					
0h		Bh					

Table 14-17861. MCSPI_HL_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old scheme and current
29:28	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
27:16	FUNC	R	30h	Function indicates a software compatible module family If there is no level of software compatibility a new Func number [and hence REVISION] should be assigned
15:11	R_RTL	R	3h	RTL Version [R], maintained by IP design owner RTL follows a numbering such as XYRZ which are explained in this table R changes ONLY when: [1] PDS uploads occur which may have been due to spec changes [2] Bug fixes occur [3] Resets to '0' when X or Y changes Design team has an internal 'Z' [customer invisible] number which increments on every drop that happens due to DV and RTL updates Z resets to 0 when R increments

Table 14-17861. MCSPI_HL_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	X_MAJOR	R	2h	Major Revision [X], maintained by IP specification owner X changes ONLY when: [1] There is a major feature addition An example would be adding Controller Mode to Utopia Level2 The Func field [or Class/ Type in old PID format] will remain the same X does NOT change due to: [1] Bug fixes [2] Change in feature parameters
7:6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers
5:0	Y_MINOR	R	Bh	Minor Revision [Y], maintained by IP specification owner Y changes ONLY when: [1] Features are scaled [up or down] Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available [2] When feature creeps from Is-Not list to Is list But this may not be the case once it sees silicon; in which case X will change Y does NOT change due to: [1] Bug fixes [2] Typos or clarifications [3] major functional/feature change/addition/ deletion Instead these changes may be reflected via R, S, X as applicable Spec owner maintains a customer-invisible number 'S' which changes due to: [1] Typos/clarifications [2] Bug documentation Note that this bug is not due to a spec change but due to implementation Nevertheless, the spec tracks the IP bugs An RTL release [say for silicon PG11] that occurs due to bug fix should document the corresponding spec number [XYS] in its release notes

14.9.1.4.2.2 MCSPI_HL_HWINFO Register

1 MCSPI_HL_HWINFO Register (Offset = 4h) [reset = 9h]

Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

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Table 14-17862. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0004h**
MCSPI1	**2011 0004h**
MCSPI2	**2012 0004h**
MCSPI3	**2013 0004h**
MCSPI4	**2014 0004h**
MCU_MCSPI0	**04B0 0004h**
MCU_MCSPI1	**04B1 0004h**

Figure 14-5899. MCSPI_HL_HWINFO Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD	RETMODE	FFNBYTE					USEFIFO
R	R	R					R
0h	0h	4h					1h

Table 14-17864. MCSPI_HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
6	RETMODE	R	0h	This bit field indicates whether the retention mode is supported using the pin PIRFFRET 0 `Retention mode disabled` 1 `Retention mode enabled`
5:1	FFNBYTE	R	4h	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account 1 `FIFO 16 bytes depth` 2 `FIFO 32 bytes depth` 4 `FIFO 64 bytes depth` 8 `FIFO 128 bytes depth` 10 `FIFO 256 bytes depth`

Table 14-17864. MCSPI_HL_HWINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	USEFIFO	R	1h	Use of a FIFO enable: This bit field indicates if a FIFO is integrated within controller design with its management 0 `FIFO not implemented in design` 1 `FIFO and its management implemented in design with depth defined by FFNBYTE generic`

14.9.1.4.2.3 MCSPI_HL_SYSCONFIG Register

1 MCSPI_HL_SYSCONFIG Register (Offset = 10h) [reset = 8h]

Clock management configuration

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Table 14-17865. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0010h**
MCSPI1	**2011 0010h**
MCSPI2	**2012 0010h**
MCSPI3	**2013 0010h**
MCSPI4	**2014 0010h**
MCU_MCSPI0	**04B0 0010h**
MCU_MCSPI1	**04B1 0010h**

Figure 14-5900. MCSPI_HL_SYSCONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RSVD</td><td colspan="2">IDLEMODE</td><td>FREEEMU</td><td>SOFTRESET</td></tr>
<tr><td colspan="4">R</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">2h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-17867. MCSPI_HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD	R	0h	Reserved

Table 14-17867. MCSPI_HL_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	IDLEMODE	R/W	2h	Configuration of the local target state management mode By definition, target can handle read/write transaction as long as it is out of IDLE state 0 `Force-idle mode: local target's IDLE state follows (acknowledges) the system's clock stop requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only.` 1 `No-idle mode: local target never enters IDLE state. Backup mode, for debug only.` 2 `Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events.` 3 `Smart-idle wake-up-capable mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state.`
1	FREEEMU	R/W	0h	Sensitivity to emulation [debug] suspend input signal 0 `IP module is sensitive to emulation suspend.` 1 `IP module is not sensitive to emulation suspend.`
0	SOFTRESET	R/W	0h	Software reset [Optional] 0 `Reset done, no pending action` 1 `Initiate software reset`

14.9.1.4.2.4 MCSPI_REVISION Register

1 MCSPI_REVISION Register (Offset = 100h) [reset = 2Bh]

This register contains the hard coded RTL revision number.

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Table 14-17868. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0100h**
MCSPI1	**2011 0100h**
MCSPI2	**2012 0100h**
MCSPI3	**2013 0100h**
MCSPI4	**2014 0100h**
MCU_MCSPI0	**04B0 0100h**
MCU_MCSPI1	**04B1 0100h**

Figure 14-5901. MCSPI_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">REV</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2Bh</td></tr>
</table>

Table 14-17870. MCSPI_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_13	R	0h	Reads returns 0
7:0	REV	R	2Bh	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 10, 0x21 for 21

14.9.1.4.2.5 MCSPI_SYSCONFIG Register

1 MCSPI_SYSCONFIG Register (Offset = 110h) [reset = 15h]

This register allows controlling various parameters of the OCP interface.

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Table 14-17871. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0110h**
MCSPI1	**2011 0110h**
MCSPI2	**2012 0110h**
MCSPI3	**2013 0110h**
MCSPI4	**2014 0110h**
MCU_MCSPI0	**04B0 0110h**
MCU_MCSPI1	**04B1 0110h**

Figure 14-5902. MCSPI_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_14							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_14							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_14						CLOCKACTIVITY	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED_15			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R			R/W		R/W	R/W	R/W
0h			2h		1h	0h	1h

Table 14-17873. MCSPI_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_14	R	0h	Reads returns 0
9:8	CLOCKACTIVITY	R/W	0h	Clocks activity during wake up mode period 0 `Interface and functional clocks may be switched off.` 1 `Interface clock is maintained. Functional clock may be switched off.` 2 `Functional clock is maintained. Interface clock may be switched off.` 3 `Interface and functional clocks are maintained.`
7:5	RESERVED_15	R	0h	Reads returns 0

Table 14-17873. MCSPI_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	SIDLEMODE	R/W	2h	Power management 0 If an IDLE request is detected, the MCSPI acknowledges it unconditionally and goes in inactive mode. Interrupt, DMA requests and wake-up lines are unconditionally deasserted and the module wake-up capability is deactivated even if the MCSPI_SYSCONFIG[2] ENAWAKEUP bit is set. 1 If an IDLE request is detected, the request is ignored and the module does not switch to wake-up mode, and keeps on behaving normally. 2 If an IDLE request is detected, the module will switch to wake-up mode based on its internal activity, and the wake-up capability can be used if the bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set. 3 Reserved - do not use.
2	ENAWAKEUP	R/W	1h	WakeUp feature control 0 Wake-up capability is disabled. 1 Wake-up capability is enabled.
1	SOFTRESET	R/W	0h	Software reset During reads it always returns 0 0 (write) Normal mode 1 (write) Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware.
0	AUTOIDLE	R/W	1h	Internal OCP Clock gating strategy 0 Interface clock is free-running. 1 Automatic interface clock gating strategy is applied, based on the configuration interface activity.

14.9.1.4.2.6 MCSPI_SYSSTATUS Register

1 MCSPI_SYSSTATUS Register (Offset = 114h) [reset = 1h]

This register provides status information about the module excluding the interrupt status information

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Table 14-17874. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0114h**
MCSPI1	**2011 0114h**
MCSPI2	**2012 0114h**
MCSPI3	**2013 0114h**
MCSPI4	**2014 0114h**
MCU_MCSPI0	**04B0 0114h**
MCU_MCSPI1	**04B1 0114h**

Figure 14-5903. MCSPI_SYSSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_16							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_16							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_16							RESETDONE
R							R
0h							1h

Table 14-17876. MCSPI_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_16	R	0h	Reserved for module specific status information Read returns 0
0	RESETDONE	R	1h	Internal Reset Monitoring 0 Internal module reset is ongoing 1 Reset completed

14.9.1.4.2.7 MCSPI_IRQSTATUS Register

1 MCSPI_IRQSTATUS Register (Offset = 118h) [reset = 0h]

The interrupt status regroups all the status of the module internal events that can generate an interrupt

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Table 14-17877. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0118h**
MCSPI1	**2011 0118h**
MCSPI2	**2012 0118h**
MCSPI3	**2013 0118h**
MCSPI4	**2014 0118h**
MCU_MCSPI0	**04B0 0118h**
MCU_MCSPI1	**04B1 0118h**

Figure 14-5904. MCSPI_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_8							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED_8						EOW	WKS
R						R/W1TS	R/W1TS
0h						0h	0h

15	14	13	12	11	10	9	8
RESERVED_7	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED_9	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY
R	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
RESERVED_10	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY
R	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17879. MCSPI_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_8	R	0h	Reads returns 0
17	EOW	R/W1TS	0h	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT] 0 `Event false` 1 `Event status bit is reset`
16	WKS	R/W1TS	0h	Wake Up event in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 `Event status bit unchanged` 1 `Event is pending`
15	RESERVED_7	R	0h	Reads returns 0

Table 14-17879. MCSPI_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RX3_FULL	R/W1TS	0h	Receiver register is full or almost full Only when Channel 3 is enabled 0 Event status bit unchanged 1 Event is pending
13	TX3_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Only when Channel 3 is enabled The transmitter register is empty [not updated by Host or DMA with new data] before its time slot assignment Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled 0 Event status bit unchanged 1 Event is pending
12	TX3_EMPTY	R/W1TS	0h	Transmitter register is empty or almost empty Note: Enabling the channel automatically rises this event 0 Event status bit unchanged 1 Event is pending
11	RESERVED_9	R	0h	Reads returns 0
10	RX2_FULL	R/W1TS	0h	Receiver register full or almost full Channel 2 0 Event status bit unchanged 1 Event is pending
9	TX2_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 2 0 Event status bit unchanged 1 Event is pending
8	TX2_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 2 0 Event status bit unchanged 1 Event is pending
7	RESERVED_10	R	0h	Reads returns 0
6	RX1_FULL	R/W1TS	0h	Receiver register full or almost full Channel 1 0 Event status bit unchanged 1 Event is pending
5	TX1_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 1 0 Event status bit unchanged 1 Event is pending
4	TX1_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 1 0 Event status bit unchanged 1 Event is pending
3	RX0_OVERFLOW	R/W1TS	0h	Receiver register overflow [responder mode only] Channel 0 0 Event status bit unchanged 1 Event is pending
2	RX0_FULL	R/W1TS	0h	Receiver register full or almost full Channel 0 0 Event status bit unchanged 1 Event is pending
1	TX0_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 0 0 Event status bit unchanged 1 Event is pending
0	TX0_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 0 0 Event status bit unchanged 1 Event is pending

14.9.1.4.2.8 MCSPI_IRQENABLE Register

1 MCSPI_IRQENABLE Register (Offset = 11Ch) [reset = 0h]

This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.

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Table 14-17880. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 011Ch**
MCSPI1	**2011 011Ch**
MCSPI2	**2012 011Ch**
MCSPI3	**2013 011Ch**
MCSPI4	**2014 011Ch**
MCU_MCSPI0	**04B0 011Ch**
MCU_MCSPI1	**04B1 011Ch**

Figure 14-5905. MCSPI_IRQENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED_5							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_5						EOW_ENABLE	WKE
R						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED_4	RX3_FULL_ENABLE	TX3_UNDERFLOW_ENABLE	TX3_EMPTY_ENABLE	RESERVED_6	RX2_FULL_ENABLE	TX2_UNDERFLOW_ENABLE	TX2_EMPTY_ENABLE
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_3	RX1_FULL_ENABLE	TX1_UNDERFLOW_ENABLE	TX1_EMPTY_ENABLE	RX0_OVERFLOW_ENABLE	RX0_FULL_ENABLE	TX0_UNDERFLOW_ENABLE	TX0_EMPTY_ENABLE
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17882. MCSPI_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_5	R	0h	Reads return 0
17	EOW_ENABLE	R/W	0h	End of Word count Interrupt Enable 0 `Interrupt disabled` 1 `Interrupt enabled`
16	WKE	R/W	0h	Wake Up event interrupt Enable in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 `Interrupt disabled` 1 `Interrupt enabled`
15	RESERVED_4	R	0h	Reads returns 0

Table 14-17882. MCSPI_IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RX3_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 3 0 `Interrupt disabled` 1 `Interrupt enabled`
13	TX3_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 3 0 `Interrupt disabled` 1 `Interrupt enabled`
12	TX3_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch3 0 `Interrupt disabled` 1 `Interrupt enabled`
11	RESERVED_6	R	0h	Reads return 0
10	RX2_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
9	TX2_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
8	TX2_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
7	RESERVED_3	R	0h	Reads return 0
6	RX1_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
5	TX1_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
4	TX1_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
3	RX0_OVERFLOW_ENABLE	R/W	0h	Receiver register Overflow Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
2	RX0_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
1	TX0_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
0	TX0_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`

14.9.1.4.2.9 MCSPI_WAKEUPENABLE Register

1 MCSPI_WAKEUPENABLE Register (Offset = 120h) [reset = 0h]

The wakeup enable register allows to enable/disable the module internal sources of wakeup on event-by-event basis.

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Table 14-17883. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0120h**
MCSPI1	**2011 0120h**
MCSPI2	**2012 0120h**
MCSPI3	**2013 0120h**
MCSPI4	**2014 0120h**
MCU_MCSPI0	**04B0 0120h**
MCU_MCSPI1	**04B1 0120h**

Figure 14-5906. MCSPI_WAKEUPENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED_18							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_18							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_18							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_18							WKEN
R							R/W
0h							0h

Table 14-17885. MCSPI_WAKEUPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_18	R	0h	Reads returns 0
0	WKEN	R/W	0h	WakeUp functionality in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 The event is not allowed to wake-up the system, even if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUPis set. 1 The event is allowed to wake-up the system if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set.

14.9.1.4.2.10 MCSPI_SYST Register

1 MCSPI_SYST Register (Offset = 124h) [reset = 0h]

This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.

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Table 14-17886. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0124h**
MCSPI1	**2011 0124h**
MCSPI2	**2012 0124h**
MCSPI3	**2013 0124h**
MCSPI4	**2014 0124h**
MCU_MCSPI0	**04B0 0124h**
MCU_MCSPI1	**04B1 0124h**

Figure 14-5907. MCSPI_SYST Name Register

31	30	29	28	27	26	25	24
RESERVED_17							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_17							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_17				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17888. MCSPI_SYST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_17	R	0h	Reads returns 0
11	SSB	R/W	0h	Set status bit 0 `No action. Writing 0 does not clear already set status bits. This bit must be cleared before trying to clear a status bit of the MCSPI_IRQSTATUS register.` 1 `Force to 1 all status bits of MCSPI_IRQSTATUS register. Writing 1 into this bit sets to 1 all status bits in the MCSPI_IRQSTATUS register.`
10	SPIENDIR	R/W	0h	Set the direction of the SPIEN[3:0] lines and SPICLK line 0 `Output (as in controller mode)` 1 `Input (as in peripheral mode)`

Table 14-17888. MCSPI_SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SPIDATDIR1	R/W	0h	Set the direction of the SPIDAT[1] 0 Output 1 Input
8	SPIDATDIR0	R/W	0h	Set the direction of the SPIDAT[0] 0 Output 1 Input
7	WAKD	R/W	0h	SWAKEUP output [signal data value of internal signal to system] The signal is driven high or low according to the value written into this register bit 0 The pin is driven low. 1 The pin is driven high.
6	SPICLK	R/W	0h	SPICLK line [signal data value] If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the CLKSPI line [high or low], and a write into this bit has no effect If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the CLKSPI line is driven high or low according to the value written into this register
5	SPIDAT_1	R/W	0h	SPIDAT[1] line [signal data value] If MCSPI_SYST[SPIDATDIR1] = 0 [output mode direction], the SPIDAT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR1] = 1 [input mode direction], this bit returns the value on the SPIDAT[1] line [high or low], and a write into this bit has no effect
4	SPIDAT_0	R/W	0h	SPIDAT[0] line [signal data value] If MCSPI_SYST[SPIDATDIR0] = 0 [output mode direction], the SPIDAT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR0] = 1 [input mode direction], this bit returns the value on the SPIDAT[0] line [high or low], and a write into this bit has no effect
3	SPIEN_3	R/W	0h	SPIEN[3] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[3] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[3] line [high or low], and a write into this bit has no effect
2	SPIEN_2	R/W	0h	SPIEN[2] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[2] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[2] line [high or low], and a write into this bit has no effect
1	SPIEN_1	R/W	0h	SPIEN[1] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[1] line [high or low], and a write into this bit has no effect
0	SPIEN_0	R/W	0h	SPIEN[0] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[0] line [high or low], and a write into this bit has no effect

14.9.1.4.2.11 MCSPI_MODULCTRL Register

1 MCSPI_MODULCTRL Register (Offset = 128h) [reset = 4h]

This register is dedicated to the configuration of the serial port interface.

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Table 14-17889. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0128h**
MCSPI1	**2011 0128h**
MCSPI2	**2012 0128h**
MCSPI3	**2013 0128h**
MCSPI4	**2014 0128h**
MCU_MCSPI0	**04B0 0128h**
MCU_MCSPI1	**04B1 0128h**

Figure 14-5908. MCSPI_MODULCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_11							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_11							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_11							FDAA
R							R/W
0h							0h
7	6	5	4	3	2	1	0
MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			0h	1h	0h	0h

Table 14-17891. MCSPI_MODULCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_11	R	0h	Reads returns 0
8	FDAA	R/W	0h	FIFO DMA Address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256 bit aligned address If this bit is set the enabled channel which uses the FIFO has its datas managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX[i] and MCSPI_RX[i] registers 0 `FIFO data managed by MCSPI_TX(i) and MCSPI_RX(i) registers.` 1 `FIFO data managed by MCSPI_DAFTX and MCSPI_DAFRX registers.`

Table 14-17891. MCSPI_MODULCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	MOA	R/W	0h	Multiple word ocp access: This register can only be used when a channel is enabled using a FIFO It allows the system to perform multiple SPI word access for a single 32-bit OCP word access This is possible for WL < 16 0 `Multiple word access disabled` 1 `Multiple word access enabled with FIFO`
6:4	INITDLY	R/W	0h	Initial spi delay for first transfer: This register is an option only available in SINGLE controller mode, The controller waits for a delay to transmit the first spi word after channel enabled and corresponding TX register filled This Delay is based on SPI output frequency clock, No clock output provided to the boundary and chip select is not active in 4 pin mode within this period 0 `No delay for first MCSPI transfer.` 1 `The controller wait 4 MCSPI bus clock` 2 `The controller wait 8 MCSPI bus clock` 3 `The controller wait 16 MCSPI bus clock` 4 `The controller wait 32 MCSPI bus clock`
3	SYSTEM_TEST	R/W	0h	Enables the system test mode 0 `Functional mode` 1 `System test mode (SYSTEST)`
2	MS	R/W	1h	Controller/ Responder 0 `Controller - The module generates the SPICLK and SPIEN[3:0].` 1 `Peripheral - The module receives the SPICLK and SPIEN[3:0].`
1	PIN34	R/W	0h	Pin mode selection: This register is used to configure the SPI pin mode, in controller or responder mode If asserted the controller only use SIMO,SOMI and SPICLK clock pin for spi transfers 0 `SPIEN is used as a chip-select.` 1 `SPIEN is not used. In this mode all related options to chip-select have no meaning.`
0	SINGLE	R/W	0h	Single channel / Multi Channel [controller mode only] 0 `More than one channel will be used in controller mode.` 1 `Only one channel will be used in controller mode. This bit must be set in Force SPIEN[i] mode.`

14.9.1.4.2.12 MCSPI_CH0CONF Register

1 MCSPI_CH0CONF Register (Offset = 12Ch) [reset = 60000h]

This register is dedicated to the configuration of the channel 0

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Table 14-17892. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 012Ch**
MCSPI1	**2011 012Ch**
MCSPI2	**2012 012Ch**
MCSPI3	**2013 012Ch**
MCSPI4	**2014 012Ch**
MCU_MCSPI0	**04B0 012Ch**
MCU_MCSPI1	**04B1 012Ch**

Figure 14-5909. MCSPI_CH0CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS0		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
R/W	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-17894. MCSPI_CH0CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.

Table 14-17894. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.
26:25	TCS0	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	SPIENSLV	R/W	0h	Channel 0 only and responder mode only: SPI responder select signal detection Reserved bits for other cases 0 Detection enabled only on SPIEN[0] 1 Detection enabled only on SPIEN[1] 2 Detection enabled only on SPIEN[2] 3 Detection enabled only on SPIEN[3]
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])

Table 14-17894. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

Table 14-17894. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 2 3 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.9.1.4.2.13 MCSPI_CH0STAT Register

1 MCSPI_CH0STAT Register (Offset = 130h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 0

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Table 14-17895. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0130h**
MCSPI1	**2011 0130h**
MCSPI2	**2012 0130h**
MCSPI3	**2013 0130h**
MCSPI4	**2014 0130h**
MCU_MCSPI0	**04B0 0130h**
MCU_MCSPI1	**04B1 0130h**

Figure 14-5910. MCSPI_CH0STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17897. MCSPI_CH0STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 `FIFO receive buffer is not full` 1 `FIFO receive buffer is full`
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 `FIFO receive buffer is not empty` 1 `FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 `FIFO transmit buffer is not full` 1 `FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 `FIFO transmit buffer is not empty` 1 `FIFO transmit buffer is empty`

Table 14-17897. MCSPI_CH0STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1 This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 Register is full. 1 Register is empty.
0	RXS	R	0h	Channel "i" Receiver Register Status 0 Register is empty. 1 Register is full.

14.9.1.4.2.14 MCSPI_CH0CTRL Register

1 MCSPI_CH0CTRL Register (Offset = 134h) [reset = 0h]

This register is dedicated to enable the channel 0

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Table 14-17898. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0134h**
MCSPI1	**2011 0134h**
MCSPI2	**2012 0134h**
MCSPI3	**2013 0134h**
MCSPI4	**2014 0134h**
MCU_MCSPI0	**04B0 0134h**
MCU_MCSPI1	**04B1 0134h**

Figure 14-5911. MCSPI_CH0CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 14-17900. MCSPI_CH0CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.9.1.4.2.15 MCSPI_TX0 Register

1 MCSPI_TX0 Register (Offset = 138h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-17901. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0138h**
MCSPI1	**2011 0138h**
MCSPI2	**2012 0138h**
MCSPI3	**2013 0138h**
MCSPI4	**2014 0138h**
MCU_MCSPI0	**04B0 0138h**
MCU_MCSPI1	**04B1 0138h**

Figure 14-5912. MCSPI_TX0 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDATA							
R/W							
0h							

Table 14-17903. MCSPI_TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 0 Data to transmit

14.9.1.4.2.16 MCSPI_RX0 Register

1 MCSPI_RX0 Register (Offset = 13Ch) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-17904. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 013Ch**
MCSPI1	**2011 013Ch**
MCSPI2	**2012 013Ch**
MCSPI3	**2013 013Ch**
MCSPI4	**2014 013Ch**
MCU_MCSPI0	**04B0 013Ch**
MCU_MCSPI1	**04B1 013Ch**

Figure 14-5913. MCSPI_RX0 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-17906. MCSPI_RX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 0 Received Data

14.9.1.4.2.17 MCSPI_CH1CONF Register

1 MCSPI_CH1CONF Register (Offset = 140h) [reset = 60000h]

This register is dedicated to the configuration of the channel.

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Table 14-17907. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0140h**
MCSPI1	**2011 0140h**
MCSPI2	**2012 0140h**
MCSPI3	**2013 0140h**
MCSPI4	**2014 0140h**
MCU_MCSPI0	**04B0 0140h**
MCU_MCSPI1	**04B1 0140h**

Figure 14-5914. MCSPI_CH1CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS1		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-17909. MCSPI_CH1CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.

Table 14-17909. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.
26:25	TCS1	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])

Table 14-17909. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 `DMA read request disabled` 1 `DMA read request enabled`
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 `DMA write request disabled` 1 `DMA write request enabled`
13:12	TRM	R/W	0h	Transmit/Receive modes 0 `Transmit-and-receive mode` 1 `Receive-only mode` 2 `Transmit-only mode` 3 `Reserved`
11:7	WL	R/W	0h	SPI word length 0 `Reserved` 1 `Reserved` 2 `Reserved` 3 `The MCSPI word is 4 bits long` 4 `The MCSPI word is 5 bits long` 5 `The MCSPI word is 6 bits long` 6 `The MCSPI word is 7 bits long` 7 `The MCSPI word is 8 bits long` 8 `The MCSPI word is 9 bits long` 9 `The MCSPI word is 10 bits long` A `The MCSPI word is 11 bits long` B `The MCSPI word is 12 bits long` C `The MCSPI word is 13 bits long` D `The MCSPI word is 14 bits long` E `The MCSPI word is 15 bits long` F `The MCSPI word is 16 bits long` 10 `The MCSPI word is 17 bits long` 11 `The MCSPI word is 18 bits long` 12 `The MCSPI word is 19 bits long` 13 `The MCSPI word is 20 bits long` 14 `The MCSPI word is 21 bits long` 15 `The MCSPI word is 22 bits long` 16 `The MCSPI word is 23 bits long` 17 `The MCSPI word is 24 bits long` 18 `The MCSPI word is 25 bits long` 19 `The MCSPI word is 26 bits long` 1A `The MCSPI word is 27 bits long` 1B `The MCSPI word is 28 bits long` 1C `The MCSPI word is 29 bits long` 1D `The MCSPI word is 30 bits long` 1E `The MCSPI word is 31 bits long` 1F `The MCSPI word is 32 bits long`
6	EPOL	R/W	0h	SPIEN polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`

Table 14-17909. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 2 3 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`
0	PHA	R/W	0h	SPICLK phase 0 `Data are latched on odd-numbered edges of SPICLK.` 1 `Data are latched on even-numbered edges of SPICLK.`

14.9.1.4.2.18 MCSPI_CH1STAT Register

1 MCSPI_CH1STAT Register (Offset = 144h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 1

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Table 14-17910. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0144h**
MCSPI1	**2011 0144h**
MCSPI2	**2012 0144h**
MCSPI3	**2013 0144h**
MCSPI4	**2014 0144h**
MCU_MCSPI0	**04B0 0144h**
MCU_MCSPI1	**04B1 0144h**

Figure 14-5915. MCSPI_CH1STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17912. MCSPI_CH1STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 `FIFO receive buffer is not full` 1 `FIFO receive buffer is full`
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 `FIFO receive buffer is not empty` 1 `FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 `FIFO transmit buffer is not full` 1 `FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 `FIFO transmit buffer is not empty` 1 `FIFO transmit buffer is empty`

Table 14-17912. MCSPI_CH1STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.9.1.4.2.19 MCSPI_CH1CTRL Register

1 MCSPI_CH1CTRL Register (Offset = 148h) [reset = 0h]

This register is dedicated to enable the channel 1

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Table 14-17913. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0148h**
MCSPI1	**2011 0148h**
MCSPI2	**2012 0148h**
MCSPI3	**2013 0148h**
MCSPI4	**2014 0148h**
MCU_MCSPI0	**04B0 0148h**
MCU_MCSPI1	**04B1 0148h**

Figure 14-5916. MCSPI_CH1CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXTCLK							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							EN
R							R/W
0h							0h

Table 14-17915. MCSPI_CH1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.9.1.4.2.20 MCSPI_TX1 Register

1 MCSPI_TX1 Register (Offset = 14Ch) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-17916. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 014Ch**
MCSPI1	**2011 014Ch**
MCSPI2	**2012 014Ch**
MCSPI3	**2013 014Ch**
MCSPI4	**2014 014Ch**
MCU_MCSPI0	**04B0 014Ch**
MCU_MCSPI1	**04B1 014Ch**

Figure 14-5917. MCSPI_TX1 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 14-17918. MCSPI_TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 1 Data to transmit

14.9.1.4.2.21 MCSPI_RX1 Register

1 MCSPI_RX1 Register (Offset = 150h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-17919. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0150h**
MCSPI1	**2011 0150h**
MCSPI2	**2012 0150h**
MCSPI3	**2013 0150h**
MCSPI4	**2014 0150h**
MCU_MCSPI0	**04B0 0150h**
MCU_MCSPI1	**04B1 0150h**

Figure 14-5918. MCSPI_RX1 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-17921. MCSPI_RX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 1 Received Data

14.9.1.4.2.22 MCSPI_CH2CONF Register

1 MCSPI_CH2CONF Register (Offset = 154h) [reset = 60000h]

This register is dedicated to the configuration of the channel 2

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Table 14-17922. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0154h**
MCSPI1	**2011 0154h**
MCSPI2	**2012 0154h**
MCSPI3	**2013 0154h**
MCSPI4	**2014 0154h**
MCU_MCSPI0	**04B0 0154h**
MCU_MCSPI1	**04B1 0154h**

Figure 14-5919. MCSPI_CH2CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS2		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	22	21	20	19	18	17	16
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	14	13	12	11	10	9	8
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	6	5	4	3	2	1	0
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-17924. MCSPI_CH2CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.

Table 14-17924. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.
26:25	TCS2	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])

Table 14-17924. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 `DMA read request disabled` 1 `DMA read request enabled`
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 `DMA write request disabled` 1 `DMA write request enabled`
13:12	TRM	R/W	0h	Transmit/Receive modes 0 `Transmit-and-receive mode` 1 `Receive-only mode` 2 `Transmit-only mode` 3 `Reserved`
11:7	WL	R/W	0h	SPI word length 0 `Reserved` 1 `Reserved` 2 `Reserved` 3 `The MCSPI word is 4 bits long` 4 `The MCSPI word is 5 bits long` 5 `The MCSPI word is 6 bits long` 6 `The MCSPI word is 7 bits long` 7 `The MCSPI word is 8 bits long` 8 `The MCSPI word is 9 bits long` 9 `The MCSPI word is 10 bits long` A `The MCSPI word is 11 bits long` B `The MCSPI word is 12 bits long` C `The MCSPI word is 13 bits long` D `The MCSPI word is 14 bits long` E `The MCSPI word is 15 bits long` F `The MCSPI word is 16 bits long` 10 `The MCSPI word is 17 bits long` 11 `The MCSPI word is 18 bits long` 12 `The MCSPI word is 19 bits long` 13 `The MCSPI word is 20 bits long` 14 `The MCSPI word is 21 bits long` 15 `The MCSPI word is 22 bits long` 16 `The MCSPI word is 23 bits long` 17 `The MCSPI word is 24 bits long` 18 `The MCSPI word is 25 bits long` 19 `The MCSPI word is 26 bits long` 1A `The MCSPI word is 27 bits long` 1B `The MCSPI word is 28 bits long` 1C `The MCSPI word is 29 bits long` 1D `The MCSPI word is 30 bits long` 1E `The MCSPI word is 31 bits long` 1F `The MCSPI word is 32 bits long`
6	EPOL	R/W	0h	SPIEN polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`

Table 14-17924. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 2 3 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.9.1.4.2.23 MCSPI_CH2STAT Register

1 MCSPI_CH2STAT Register (Offset = 158h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 2

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Table 14-17925. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0158h**
MCSPI1	**2011 0158h**
MCSPI2	**2012 0158h**
MCSPI3	**2013 0158h**
MCSPI4	**2014 0158h**
MCU_MCSPI0	**04B0 0158h**
MCU_MCSPI1	**04B1 0158h**

Figure 14-5920. MCSPI_CH2STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17927. MCSPI_CH2STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 `FIFO receive buffer is not full` 1 `FIFO receive buffer is full`
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 `FIFO receive buffer is not empty` 1 `FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 `FIFO transmit buffer is not full` 1 `FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 `FIFO transmit buffer is not empty` 1 `FIFO transmit buffer is empty`

Table 14-17927. MCSPI_CH2STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.9.1.4.2.24 MCSPI_CH2CTRL Register

1 MCSPI_CH2CTRL Register (Offset = 15Ch) [reset = 0h]

This register is dedicated to enable the channel 2

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Table 14-17928. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 015Ch**
MCSPI1	**2011 015Ch**
MCSPI2	**2012 015Ch**
MCSPI3	**2013 015Ch**
MCSPI4	**2014 015Ch**
MCU_MCSPI0	**04B0 015Ch**
MCU_MCSPI1	**04B1 015Ch**

Figure 14-5921. MCSPI_CH2CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 14-17930. MCSPI_CH2CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0

15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
				`0 Clock ratio is CLKD + 1.`
				`1 Clock ratio is CLKD + 1 + 16.`
				`FF Clock ratio is CLKD + 1 + 4080.`

7:1	RESERVED_1	R	0h	Read returns 0

0	EN	R/W	0h	Channel Enable
				`0 Channel i is not active.`
				`1 Channel i is active.`

14.9.1.4.2.25 MCSPI_TX2 Register

1 MCSPI_TX2 Register (Offset = 160h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-17931. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0160h**
MCSPI1	**2011 0160h**
MCSPI2	**2012 0160h**
MCSPI3	**2013 0160h**
MCSPI4	**2014 0160h**
MCU_MCSPI0	**04B0 0160h**
MCU_MCSPI1	**04B1 0160h**

Figure 14-5922. MCSPI_TX2 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 14-17933. MCSPI_TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 2 Data to transmit

14.9.1.4.2.26 MCSPI_RX2 Register

1 MCSPI_RX2 Register (Offset = 164h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-17934. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0164h**
MCSPI1	**2011 0164h**
MCSPI2	**2012 0164h**
MCSPI3	**2013 0164h**
MCSPI4	**2014 0164h**
MCU_MCSPI0	**04B0 0164h**
MCU_MCSPI1	**04B1 0164h**

Figure 14-5923. MCSPI_RX2 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-17936. MCSPI_RX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 2 Received Data

14.9.1.4.2.27 MCSPI_CH3CONF Register

1 MCSPI_CH3CONF Register (Offset = 168h) [reset = 60000h]

This register is dedicated to the configuration of the channel 3

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Table 14-17937. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0168h**
MCSPI1	**2011 0168h**
MCSPI2	**2012 0168h**
MCSPI3	**2013 0168h**
MCSPI4	**2014 0168h**
MCU_MCSPI0	**04B0 0168h**
MCU_MCSPI1	**04B1 0168h**

Figure 14-5924. MCSPI_CH3CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS3		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-17939. MCSPI_CH3CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.

Table 14-17939. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.
26:25	TCS3	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])

Table 14-17939. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

Table 14-17939. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 2 3 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.9.1.4.2.28 MCSPI_CH3STAT Register

1 MCSPI_CH3STAT Register (Offset = 16Ch) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 3

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Table 14-17940. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 016Ch**
MCSPI1	**2011 016Ch**
MCSPI2	**2012 016Ch**
MCSPI3	**2013 016Ch**
MCSPI4	**2014 016Ch**
MCU_MCSPI0	**04B0 016Ch**
MCU_MCSPI1	**04B1 016Ch**

Figure 14-5925. MCSPI_CH3STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17942. MCSPI_CH3STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 `FIFO receive buffer is not full` 1 `FIFO receive buffer is full`
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 `FIFO receive buffer is not empty` 1 `FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 `FIFO transmit buffer is not full` 1 `FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 `FIFO transmit buffer is not empty` 1 `FIFO transmit buffer is empty`

Table 14-17942. MCSPI_CH3STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.9.1.4.2.29 MCSPI_CH3CTRL Register

1 MCSPI_CH3CTRL Register (Offset = 170h) [reset = 0h]

This register is dedicated to enable the channel 3

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Table 14-17943. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0170h**
MCSPI1	**2011 0170h**
MCSPI2	**2012 0170h**
MCSPI3	**2013 0170h**
MCSPI4	**2014 0170h**
MCU_MCSPI0	**04B0 0170h**
MCU_MCSPI1	**04B1 0170h**

Figure 14-5926. MCSPI_CH3CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 14-17945. MCSPI_CH3CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0

15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
				`0 Clock ratio is CLKD + 1.`
				`1 Clock ratio is CLKD + 1 + 16.`
				`FF Clock ratio is CLKD + 1 + 4080.`

7:1	RESERVED_1	R	0h	Read returns 0

0	EN	R/W	0h	Channel Enable
				`0 Channel i is not active.`
				`1 Channel i is active.`

14.9.1.4.2.30 MCSPI_TX3 Register

1 MCSPI_TX3 Register (Offset = 174h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Return to Summary Table

Table 14-17946. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0174h**
MCSPI1	**2011 0174h**
MCSPI2	**2012 0174h**
MCSPI3	**2013 0174h**
MCSPI4	**2014 0174h**
MCU_MCSPI0	**04B0 0174h**
MCU_MCSPI1	**04B1 0174h**

Figure 14-5927. MCSPI_TX3 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TDATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDATA							
R/W							
0h							

Table 14-17948. MCSPI_TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 3 Data to transmit

14.9.1.4.2.31 MCSPI_RX3 Register

1 MCSPI_RX3 Register (Offset = 178h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

Return to Summary Table

Table 14-17949. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0178h**
MCSPI1	**2011 0178h**
MCSPI2	**2012 0178h**
MCSPI3	**2013 0178h**
MCSPI4	**2014 0178h**
MCU_MCSPI0	**04B0 0178h**
MCU_MCSPI1	**04B1 0178h**

Figure 14-5928. MCSPI_RX3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17951. MCSPI_RX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 3 Received Data

14.9.1.4.2.32 MCSPI_XFERLEVEL Register

1 MCSPI_XFERLEVEL Register (Offset = 17Ch) [reset = 0h]

This register provides transfer levels needed while using FIFO buffer during transfer.

Return to Summary Table

Table 14-17952. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 017Ch**
MCSPI1	**2011 017Ch**
MCSPI2	**2012 017Ch**
MCSPI3	**2013 017Ch**
MCSPI4	**2014 017Ch**
MCU_MCSPI0	**04B0 017Ch**
MCU_MCSPI1	**04B1 017Ch**

Figure 14-5929. MCSPI_XFERLEVEL Name Register

31	30	29	28	27	26	25	24
WCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
WCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
AFL							
R/W							
0h							
7	6	5	4	3	2	1	0
AEL							
R/W							
0h							

Table 14-17954. MCSPI_XFERLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WCNT	R/W	0h	Spi word counterThis register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO bufferWhen transfer had started, a read back in this register returns the current SPI word transfer index 0 Counter not used 1 One word FFFE 65534 MCSPI word FFFF 65535 MCSPI word

Table 14-17954. MCSPI_XFERLEVEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	AFL	R/W	0h	Buffer Almost Full This register holds the programmable almost full level value used to determine almost full buffer condition If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n-1The size of this register is defined by the generic parameter FFNBYTE 0 1 byte 1 2 bytes FE 255bytes FF 256bytes
7:0	AEL	R/W	0h	Buffer Almost EmptyThis register holds the programmable almost empty level value used to determine almost empty buffer condition If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with n-1 0 1 byte 1 2 bytes FE 255 bytes FF 256bytes

14.9.1.4.2.33 MCSPI_DAFTX Register

1 MCSPI_DAFTX Register (Offset = 180h) [reset = 0h]

This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_TX(i) register corresponding to the channel which have its FIFO enabled.

Return to Summary Table

Table 14-17955. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 0180h**
MCSPI1	**2011 0180h**
MCSPI2	**2012 0180h**
MCSPI3	**2013 0180h**
MCSPI4	**2014 0180h**
MCU_MCSPI0	**04B0 0180h**
MCU_MCSPI1	**04B1 0180h**

Figure 14-5930. MCSPI_DAFTX Name Register

31	30	29	28	27	26	25	24
DAFTDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DAFTDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DAFTDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DAFTDATA							
R/W							
0h							

Table 14-17957. MCSPI_DAFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFTDATA	R/W	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

14.9.1.4.2.34 MCSPI_DAFRX Register

1 MCSPI_DAFRX Register (Offset = 1A0h) [reset = 0h]

This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_RX(i) register corresponding to the channel which have its FIFO enabled.

Return to Summary Table

Table 14-17958. Instance Table

Instance Name	Physical Address
MCSPI0	**2010 01A0h**
MCSPI1	**2011 01A0h**
MCSPI2	**2012 01A0h**
MCSPI3	**2013 01A0h**
MCSPI4	**2014 01A0h**
MCU_MCSPI0	**04B0 01A0h**
MCU_MCSPI1	**04B1 01A0h**

Figure 14-5931. MCSPI_DAFRX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-17960. MCSPI_DAFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFRDATA	R	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

14.9.1.5 UART

UART

14.9.1.5.1 UART Summaries

UART Summaries

Table 14-17961. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	MCU_UART0 Physical Address	MCU_UART1 Physical Address	UART0 Physical Address
0h	32	UART_DLL	04A0 0000h	04A1 0000h	0280 0000h
0h	32	UART_RHR	04A0 0000h	04A1 0000h	0280 0000h
0h	32	UART_THR	04A0 0000h	04A1 0000h	0280 0000h
4h	32	UART_DLH	04A0 0004h	04A1 0004h	0280 0004h
4h	32	UART_IER_CIR	04A0 0004h	04A1 0004h	0280 0004h
4h	32	UART_IER_IRDA	04A0 0004h	04A1 0004h	0280 0004h
4h	32	UART_IER_UART	04A0 0004h	04A1 0004h	0280 0004h
8h	32	UART_EFR	04A0 0008h	04A1 0008h	0280 0008h
8h	32	UART_FCR	04A0 0008h	04A1 0008h	0280 0008h
8h	32	UART_IIR_CIR	04A0 0008h	04A1 0008h	0280 0008h
8h	32	UART_IIR_IRDA	04A0 0008h	04A1 0008h	0280 0008h
8h	32	UART_IIR_UART	04A0 0008h	04A1 0008h	0280 0008h
Ch	32	UART_LCR	04A0 000Ch	04A1 000Ch	0280 000Ch
10h	32	UART_MCR	04A0 0010h	04A1 0010h	0280 0010h
10h	32	UART_XON1_ADDR1	04A0 0010h	04A1 0010h	0280 0010h
14h	32	UART_LSR_CIR	04A0 0014h	04A1 0014h	0280 0014h
14h	32	UART_LSR_IRDA	04A0 0014h	04A1 0014h	0280 0014h
14h	32	UART_LSR_UART	04A0 0014h	04A1 0014h	0280 0014h
14h	32	UART_XON2_ADDR2	04A0 0014h	04A1 0014h	0280 0014h
18h	32	UART_MSR	04A0 0018h	04A1 0018h	0280 0018h
18h	32	UART_TCR	04A0 0018h	04A1 0018h	0280 0018h
18h	32	UART_XOFF1	04A0 0018h	04A1 0018h	0280 0018h
1Ch	32	UART_SPR	04A0 001Ch	04A1 001Ch	0280 001Ch
1Ch	32	UART_TLR	04A0 001Ch	04A1 001Ch	0280 001Ch
1Ch	32	UART_XOFF2	04A0 001Ch	04A1 001Ch	0280 001Ch
20h	32	UART_MDR1	04A0 0020h	04A1 0020h	0280 0020h
24h	32	UART_MDR2	04A0 0024h	04A1 0024h	0280 0024h
28h	32	UART_SFLSR	04A0 0028h	04A1 0028h	0280 0028h
28h	32	UART_TXFLL	04A0 0028h	04A1 0028h	0280 0028h
2Ch	32	UART_RESUME	04A0 002Ch	04A1 002Ch	0280 002Ch
2Ch	32	UART_TXFLH	04A0 002Ch	04A1 002Ch	0280 002Ch
30h	32	UART_RXFLL	04A0 0030h	04A1 0030h	0280 0030h
30h	32	UART_SFREGL	04A0 0030h	04A1 0030h	0280 0030h
34h	32	UART_RXFLH	04A0 0034h	04A1 0034h	0280 0034h
34h	32	UART_SFREGH	04A0 0034h	04A1 0034h	0280 0034h
38h	32	UART_BLR	04A0 0038h	04A1 0038h	0280 0038h
38h	32	UART_UASR	04A0 0038h	04A1 0038h	0280 0038h

Table 14-17961. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	MCU_UART0 Physical Address	MCU_UART1 Physical Address	UART0 Physical Address
3Ch	32	UART_ACREG	04A0 003Ch	04A1 003Ch	0280 003Ch
40h	32	UART_SCR	04A0 0040h	04A1 0040h	0280 0040h
44h	32	UART_SSR	04A0 0044h	04A1 0044h	0280 0044h
48h	32	UART_EBLR	04A0 0048h	04A1 0048h	0280 0048h
50h	32	UART_MVR	04A0 0050h	04A1 0050h	0280 0050h
54h	32	UART_SYSC	04A0 0054h	04A1 0054h	0280 0054h
58h	32	UART_SYSS	04A0 0058h	04A1 0058h	0280 0058h
5Ch	32	UART_WER	04A0 005Ch	04A1 005Ch	0280 005Ch
60h	32	UART_CFPS	04A0 0060h	04A1 0060h	0280 0060h
64h	32	UART_RXFIFO_LVL	04A0 0064h	04A1 0064h	0280 0064h
68h	32	UART_TXFIFO_LVL	04A0 0068h	04A1 0068h	0280 0068h
6Ch	32	UART_IER2	04A0 006Ch	04A1 006Ch	0280 006Ch
70h	32	UART_ISR2	04A0 0070h	04A1 0070h	0280 0070h
74h	32	UART_FREQ_SEL	04A0 0074h	04A1 0074h	0280 0074h
78h	32	UART_ABAUD_1ST_CHAR	04A0 0078h	04A1 0078h	0280 0078h
7Ch	32	UART_BAUD_2ND_CHAR	04A0 007Ch	04A1 007Ch	0280 007Ch
80h	32	UART_MDR3	04A0 0080h	04A1 0080h	0280 0080h
84h	32	UART_TX_DMA_THRESHOLD	04A0 0084h	04A1 0084h	0280 0084h
88h	32	UART_MDR4	04A0 0088h	04A1 0088h	0280 0088h
8Ch	32	UART_EFR2	04A0 008Ch	04A1 008Ch	0280 008Ch
90h	32	UART_ECR	04A0 0090h	04A1 0090h	0280 0090h
94h	32	UART_TIMEGUARD	04A0 0094h	04A1 0094h	0280 0094h
98h	32	UART_TIMEOUTL	04A0 0098h	04A1 0098h	0280 0098h
9Ch	32	UART_TIMEOUTH	04A0 009Ch	04A1 009Ch	0280 009Ch
A0h	32	UART_SCCR	04A0 00A0h	04A1 00A0h	0280 00A0h
A4h	32	UART_ERHR	04A0 00A4h	04A1 00A4h	0280 00A4h
A4h	32	UART_ETHR	04A0 00A4h	04A1 00A4h	0280 00A4h
A8h	32	UART_MAR	04A0 00A8h	04A1 00A8h	0280 00A8h
ACh	32	UART_MMR	04A0 00ACh	04A1 00ACh	0280 00ACh
B0h	32	UART_MBR	04A0 00B0h	04A1 00B0h	0280 00B0h

Table 14-17962. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	UART1 Physical Address	UART2 Physical Address	UART3 Physical Address
0h	32	UART_DLL	0281 0000h	0282 0000h	0283 0000h
0h	32	UART_RHR	0281 0000h	0282 0000h	0283 0000h
0h	32	UART_THR	0281 0000h	0282 0000h	0283 0000h
4h	32	UART_DLH	0281 0004h	0282 0004h	0283 0004h
4h	32	UART_IER_CIR	0281 0004h	0282 0004h	0283 0004h
4h	32	UART_IER_IRDA	0281 0004h	0282 0004h	0283 0004h
4h	32	UART_IER_UART	0281 0004h	0282 0004h	0283 0004h
8h	32	UART_EFR	0281 0008h	0282 0008h	0283 0008h
8h	32	UART_FCR	0281 0008h	0282 0008h	0283 0008h
8h	32	UART_IIR_CIR	0281 0008h	0282 0008h	0283 0008h

Table 14-17962. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART1 Physical Address	UART2 Physical Address	UART3 Physical Address
8h	32	UART_IIR_IRDA	0281 0008h	0282 0008h	0283 0008h
8h	32	UART_IIR_UART	0281 0008h	0282 0008h	0283 0008h
Ch	32	UART_LCR	0281 000Ch	0282 000Ch	0283 000Ch
10h	32	UART_MCR	0281 0010h	0282 0010h	0283 0010h
10h	32	UART_XON1_ADDR1	0281 0010h	0282 0010h	0283 0010h
14h	32	UART_LSR_CIR	0281 0014h	0282 0014h	0283 0014h
14h	32	UART_LSR_IRDA	0281 0014h	0282 0014h	0283 0014h
14h	32	UART_LSR_UART	0281 0014h	0282 0014h	0283 0014h
14h	32	UART_XON2_ADDR2	0281 0014h	0282 0014h	0283 0014h
18h	32	UART_MSR	0281 0018h	0282 0018h	0283 0018h
18h	32	UART_TCR	0281 0018h	0282 0018h	0283 0018h
18h	32	UART_XOFF1	0281 0018h	0282 0018h	0283 0018h
1Ch	32	UART_SPR	0281 001Ch	0282 001Ch	0283 001Ch
1Ch	32	UART_TLR	0281 001Ch	0282 001Ch	0283 001Ch
1Ch	32	UART_XOFF2	0281 001Ch	0282 001Ch	0283 001Ch
20h	32	UART_MDR1	0281 0020h	0282 0020h	0283 0020h
24h	32	UART_MDR2	0281 0024h	0282 0024h	0283 0024h
28h	32	UART_SFLSR	0281 0028h	0282 0028h	0283 0028h
28h	32	UART_TXFLL	0281 0028h	0282 0028h	0283 0028h
2Ch	32	UART_RESUME	0281 002Ch	0282 002Ch	0283 002Ch
2Ch	32	UART_TXFLH	0281 002Ch	0282 002Ch	0283 002Ch
30h	32	UART_RXFLL	0281 0030h	0282 0030h	0283 0030h
30h	32	UART_SFREGL	0281 0030h	0282 0030h	0283 0030h
34h	32	UART_RXFLH	0281 0034h	0282 0034h	0283 0034h
34h	32	UART_SFREGH	0281 0034h	0282 0034h	0283 0034h
38h	32	UART_BLR	0281 0038h	0282 0038h	0283 0038h
38h	32	UART_UASR	0281 0038h	0282 0038h	0283 0038h
3Ch	32	UART_ACREG	0281 003Ch	0282 003Ch	0283 003Ch
40h	32	UART_SCR	0281 0040h	0282 0040h	0283 0040h
44h	32	UART_SSR	0281 0044h	0282 0044h	0283 0044h
48h	32	UART_EBLR	0281 0048h	0282 0048h	0283 0048h
50h	32	UART_MVR	0281 0050h	0282 0050h	0283 0050h
54h	32	UART_SYSC	0281 0054h	0282 0054h	0283 0054h
58h	32	UART_SYSS	0281 0058h	0282 0058h	0283 0058h
5Ch	32	UART_WER	0281 005Ch	0282 005Ch	0283 005Ch
60h	32	UART_CFPS	0281 0060h	0282 0060h	0283 0060h
64h	32	UART_RXFIFO_LVL	0281 0064h	0282 0064h	0283 0064h
68h	32	UART_TXFIFO_LVL	0281 0068h	0282 0068h	0283 0068h
6Ch	32	UART_IER2	0281 006Ch	0282 006Ch	0283 006Ch
70h	32	UART_ISR2	0281 0070h	0282 0070h	0283 0070h
74h	32	UART_FREQ_SEL	0281 0074h	0282 0074h	0283 0074h
78h	32	UART_ABAUD_1ST_CHAR	0281 0078h	0282 0078h	0283 0078h
7Ch	32	UART_BAUD_2ND_CHAR	0281 007Ch	0282 007Ch	0283 007Ch
80h	32	UART_MDR3	0281 0080h	0282 0080h	0283 0080h

Table 14-17962. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART1 Physical Address	UART2 Physical Address	UART3 Physical Address
84h	32	UART_TX_DMA_THRESHOLD	0281 0084h	0282 0084h	0283 0084h
88h	32	UART_MDR4	0281 0088h	0282 0088h	0283 0088h
8Ch	32	UART_EFR2	0281 008Ch	0282 008Ch	0283 008Ch
90h	32	UART_ECR	0281 0090h	0282 0090h	0283 0090h
94h	32	UART_TIMEGUARD	0281 0094h	0282 0094h	0283 0094h
98h	32	UART_TIMEOUTL	0281 0098h	0282 0098h	0283 0098h
9Ch	32	UART_TIMEOUTH	0281 009Ch	0282 009Ch	0283 009Ch
A0h	32	UART_SCCR	0281 00A0h	0282 00A0h	0283 00A0h
A4h	32	UART_ERHR	0281 00A4h	0282 00A4h	0283 00A4h
A4h	32	UART_ETHR	0281 00A4h	0282 00A4h	0283 00A4h
A8h	32	UART_MAR	0281 00A8h	0282 00A8h	0283 00A8h
ACh	32	UART_MMR	0281 00ACh	0282 00ACh	0283 00ACh
B0h	32	UART_MBR	0281 00B0h	0282 00B0h	0283 00B0h

Table 14-17963. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	UART4 Physical Address	UART5 Physical Address	UART6 Physical Address
0h	32	UART_DLL	0284 0000h	0285 0000h	0286 0000h
0h	32	UART_RHR	0284 0000h	0285 0000h	0286 0000h
0h	32	UART_THR	0284 0000h	0285 0000h	0286 0000h
4h	32	UART_DLH	0284 0004h	0285 0004h	0286 0004h
4h	32	UART_IER_CIR	0284 0004h	0285 0004h	0286 0004h
4h	32	UART_IER_IRDA	0284 0004h	0285 0004h	0286 0004h
4h	32	UART_IER_UART	0284 0004h	0285 0004h	0286 0004h
8h	32	UART_EFR	0284 0008h	0285 0008h	0286 0008h
8h	32	UART_FCR	0284 0008h	0285 0008h	0286 0008h
8h	32	UART_IIR_CIR	0284 0008h	0285 0008h	0286 0008h
8h	32	UART_IIR_IRDA	0284 0008h	0285 0008h	0286 0008h
8h	32	UART_IIR_UART	0284 0008h	0285 0008h	0286 0008h
Ch	32	UART_LCR	0284 000Ch	0285 000Ch	0286 000Ch
10h	32	UART_MCR	0284 0010h	0285 0010h	0286 0010h
10h	32	UART_XON1_ADDR1	0284 0010h	0285 0010h	0286 0010h
14h	32	UART_LSR_CIR	0284 0014h	0285 0014h	0286 0014h
14h	32	UART_LSR_IRDA	0284 0014h	0285 0014h	0286 0014h
14h	32	UART_LSR_UART	0284 0014h	0285 0014h	0286 0014h
14h	32	UART_XON2_ADDR2	0284 0014h	0285 0014h	0286 0014h
18h	32	UART_MSR	0284 0018h	0285 0018h	0286 0018h
18h	32	UART_TCR	0284 0018h	0285 0018h	0286 0018h
18h	32	UART_XOFF1	0284 0018h	0285 0018h	0286 0018h
1Ch	32	UART_SPR	0284 001Ch	0285 001Ch	0286 001Ch
1Ch	32	UART_TLR	0284 001Ch	0285 001Ch	0286 001Ch
1Ch	32	UART_XOFF2	0284 001Ch	0285 001Ch	0286 001Ch
20h	32	UART_MDR1	0284 0020h	0285 0020h	0286 0020h
24h	32	UART_MDR2	0284 0024h	0285 0024h	0286 0024h

Table 14-17963. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART4 Physical Address	UART5 Physical Address	UART6 Physical Address
28h	32	UART_SFLSR	0284 0028h	0285 0028h	0286 0028h
28h	32	UART_TXFLL	0284 0028h	0285 0028h	0286 0028h
2Ch	32	UART_RESUME	0284 002Ch	0285 002Ch	0286 002Ch
2Ch	32	UART_TXFLH	0284 002Ch	0285 002Ch	0286 002Ch
30h	32	UART_RXFLL	0284 0030h	0285 0030h	0286 0030h
30h	32	UART_SFREGL	0284 0030h	0285 0030h	0286 0030h
34h	32	UART_RXFLH	0284 0034h	0285 0034h	0286 0034h
34h	32	UART_SFREGH	0284 0034h	0285 0034h	0286 0034h
38h	32	UART_BLR	0284 0038h	0285 0038h	0286 0038h
38h	32	UART_UASR	0284 0038h	0285 0038h	0286 0038h
3Ch	32	UART_ACREG	0284 003Ch	0285 003Ch	0286 003Ch
40h	32	UART_SCR	0284 0040h	0285 0040h	0286 0040h
44h	32	UART_SSR	0284 0044h	0285 0044h	0286 0044h
48h	32	UART_EBLR	0284 0048h	0285 0048h	0286 0048h
50h	32	UART_MVR	0284 0050h	0285 0050h	0286 0050h
54h	32	UART_SYSC	0284 0054h	0285 0054h	0286 0054h
58h	32	UART_SYSS	0284 0058h	0285 0058h	0286 0058h
5Ch	32	UART_WER	0284 005Ch	0285 005Ch	0286 005Ch
60h	32	UART_CFPS	0284 0060h	0285 0060h	0286 0060h
64h	32	UART_RXFIFO_LVL	0284 0064h	0285 0064h	0286 0064h
68h	32	UART_TXFIFO_LVL	0284 0068h	0285 0068h	0286 0068h
6Ch	32	UART_IER2	0284 006Ch	0285 006Ch	0286 006Ch
70h	32	UART_ISR2	0284 0070h	0285 0070h	0286 0070h
74h	32	UART_FREQ_SEL	0284 0074h	0285 0074h	0286 0074h
78h	32	UART_ABAUD_1ST_CHAR	0284 0078h	0285 0078h	0286 0078h
7Ch	32	UART_BAUD_2ND_CHAR	0284 007Ch	0285 007Ch	0286 007Ch
80h	32	UART_MDR3	0284 0080h	0285 0080h	0286 0080h
84h	32	UART_TX_DMA_THRESHOLD	0284 0084h	0285 0084h	0286 0084h
88h	32	UART_MDR4	0284 0088h	0285 0088h	0286 0088h
8Ch	32	UART_EFR2	0284 008Ch	0285 008Ch	0286 008Ch
90h	32	UART_ECR	0284 0090h	0285 0090h	0286 0090h
94h	32	UART_TIMEGUARD	0284 0094h	0285 0094h	0286 0094h
98h	32	UART_TIMEOUTL	0284 0098h	0285 0098h	0286 0098h
9Ch	32	UART_TIMEOUTH	0284 009Ch	0285 009Ch	0286 009Ch
A0h	32	UART_SCCR	0284 00A0h	0285 00A0h	0286 00A0h
A4h	32	UART_ERHR	0284 00A4h	0285 00A4h	0286 00A4h
A4h	32	UART_ETHR	0284 00A4h	0285 00A4h	0286 00A4h
A8h	32	UART_MAR	0284 00A8h	0285 00A8h	0286 00A8h
ACh	32	UART_MMR	0284 00ACh	0285 00ACh	0286 00ACh
B0h	32	UART_MBR	0284 00B0h	0285 00B0h	0286 00B0h

14.9.1.5.2 UART Registers

UART Registers

14.9.1.5.2.1 UART_DLL Register

1 UART_DLL Register (Offset = 0h) [reset = 0h]

Divisor Latches Low Register

Return to Summary Table

Table 14-17964. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0000h**
MCU_UART1	**04A1 0000h**
UART0	**0280 0000h**
UART1	**0281 0000h**
UART2	**0282 0000h**
UART3	**0283 0000h**
UART4	**0284 0000h**
UART5	**0285 0000h**
UART6	**0286 0000h**

Figure 14-5932. UART_DLL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLOCK_LSB							
R/W							
0h							

Table 14-17966. UART_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CLOCK_LSB	R/W	0h	Used to store the 8-bit LSB divisor value Reset Source: mod_g_arstn

14.9.1.5.2.2 UART_RHR Register

1 UART_RHR Register (Offset = 0h) [reset = 0h]

The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.

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Table 14-17967. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0000h**
MCU_UART1	**04A1 0000h**
UART0	**0280 0000h**
UART1	**0281 0000h**
UART2	**0282 0000h**
UART3	**0283 0000h**
UART4	**0284 0000h**
UART5	**0285 0000h**
UART6	**0286 0000h**

Figure 14-5933. UART_RHR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RHR							
R							
0h							

Table 14-17969. UART_RHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RHR	R	0h	Receive holding register Reset Source: mod_g_arstn

14.9.1.5.2.3 UART_THR Register

1 UART_THR Register (Offset = 0h) [reset = 0h]

The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.

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Table 14-17970. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0000h**
MCU_UART1	**04A1 0000h**
UART0	**0280 0000h**
UART1	**0281 0000h**
UART2	**0282 0000h**
UART3	**0283 0000h**
UART4	**0284 0000h**
UART5	**0285 0000h**
UART6	**0286 0000h**

Figure 14-5934. UART_THR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
THR							
W							
0h							

Table 14-17972. UART_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	THR	W	0h	TRANSMIT HOLDING REGISTER Reset Source: mod_g_arstn

14.9.1.5.2.4 UART_DLH Register

1 UART_DLH Register (Offset = 4h) [reset = 0h]

Divisor Latches High Register

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Table 14-17973. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0004h**
MCU_UART1	**04A1 0004h**
UART0	**0280 0004h**
UART1	**0281 0004h**
UART2	**0282 0004h**
UART3	**0283 0004h**
UART4	**0284 0004h**
UART5	**0285 0004h**
UART6	**0286 0004h**

Figure 14-5935. UART_DLH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLOCK_MSB							
R/W							
0h							

Table 14-17975. UART_DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CLOCK_MSB	R/W	0h	Used to store the 8-bit MSB divisor value Reset Source: mod_g_arstn

14.9.1.5.2.5 UART_IER_CIR Register

1 UART_IER_CIR Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 14-17976. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0004h**
MCU_UART1	**04A1 0004h**
UART0	**0280 0004h**
UART1	**0281 0004h**
UART2	**0282 0004h**
UART3	**0283 0004h**
UART4	**0284 0004h**
UART5	**0285 0004h**
UART6	**0286 0004h**

Figure 14-5936. UART_IER_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NOT_USED2		TX_STATUS_IT	NOT_USED1	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-17978. UART_IER_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	NOT_USED2	R/W	0h	Reset Source: mod_g_arstn

5	TX_STATUS_IT	R/W	0h	Reset Source: mod_g_arstn
				`0 Disables the TX status interrupt.`
				`1 Enables the TX status interrupt.`

4	NOT_USED1	R/W	0h	Reset Source: mod_g_arstn

Table 14-17978. UART_IER_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RX_OVERRUN_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the RX overrun interrupt.` 1 `Enables the RX overrun interrupt.`
2	RX_STOP_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the receive stop interrupt.` 1 `Enables the receive stop interrupt.`
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the THR interrupt.` 1 `Enables the THR interrupt.`
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the RHR interrupt.` 1 `Enables the RHR interrupt.`

14.9.1.5.2.6 UART_IER_IRDA Register

1 UART_IER_IRDA Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 14-17979. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0004h**
MCU_UART1	**04A1 0004h**
UART0	**0280 0004h**
UART1	**0281 0004h**
UART2	**0282 0004h**
UART3	**0283 0004h**
UART4	**0284 0004h**
UART5	**0285 0004h**
UART6	**0286 0004h**

Figure 14-5937. UART_IER_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17981. UART_IER_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EOF_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the received EOF interrupt.` 1 `Enables the received EOF interrupt.`
6	LINE_STS_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the receiver line status interrupt.` 1 `Enables the receiver line status interrupt.`

Table 14-17981. UART_IER_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX_STATUS_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the TX status interrupt.` 1 `Enables the TX status interrupt.`
4	STS_FIFO_TRIG_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the status FIFO trigger level interrupt.` 1 `Enables the status FIFO trigger level interrupt.`
3	RX_OVERRUN_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the RX overrun interrupt.` 1 `Enables the RX overrun interrupt.`
2	LAST_RX_BYTE_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the last byte of frame in RX FIFO interrupt.` 1 `Enables the last byte of frame in RX FIFO interrupt.`
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the THR interrupt.` 1 `Enables the THR interrupt.`
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the RHR interrupt.` 1 `Enables the RHR interrupt.`

14.9.1.5.2.7 UART_IER_UART Register

1 UART_IER_UART Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.

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Table 14-17982. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0004h**
MCU_UART1	**04A1 0004h**
UART0	**0280 0004h**
UART1	**0281 0004h**
UART2	**0282 0004h**
UART3	**0283 0004h**
UART4	**0284 0004h**
UART5	**0285 0004h**
UART6	**0286 0004h**

Figure 14-5938. UART_IER_UART Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17984. UART_IER_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7	CTS_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the CTS* interrupt` 1 `Enables the CTS* interrupt`
6	RTS_IT	R/W	0h	Reset Source: mod_g_arstn 0 `Disables the RTS* interrupt` 1 `Enables the RTS* interrupt`

Table 14-17984. UART_IER_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	XOFF_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the XOFF interrupt 1 Enables the XOFF interrupt
4	SLEEP_MODE	R/W	0h	Reset Source: mod_g_arstn 0 Disables sleep mode 1 Enables sleep mode (stop baud rate clock when the module is inactive)
3	MODEM_STS_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the modem status register interrupt 1 Enables the modem status register interrupt
2	LINE_STS_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the receiver line status interrupt 1 Enables the receiver line status interrupt
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the THR interrupt 1 Enables the THR interrupt
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 0 Disables the RHR interrupt and time out interrupt. 1 Enables the RHR interrupt and time out interrupt.

14.9.1.5.2.8 UART_EFR Register

1 UART_EFR Register (Offset = 8h) [reset = 0h]

Enhanced Feature Register

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Table 14-17985. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
MCU_UART1	**04A1 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**

Figure 14-5939. UART_EFR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 14-17987. UART_EFR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	AUTO_CTS_EN	R/W	0h	Auto-CTS enable bit. 0: Normal operation. 1: Auto-CTS flow control is enabled i.e. transmission is halted when the CTS* pin is high (inactive). Reset Source: mod_g_arstn
6	AUTO_RTS_EN	R/W	0h	Auto-RTS enable bit. 0: Normal operation. 1: Auto- RTS flow control is enabled i.e. RTS* pin goes high (inactive) when the receiver FIFO HALT trigger level, TCR[3:0], is reached, and goes low (active) when the receiver FIFO RESTORE transmission trigger level is reached. Reset Source: mod_g_arstn

Table 14-17987. UART_EFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SPECIAL_CHAR_DETECT	R/W	0h	0: Normal operation. 1: Special character detect enable. Received data is compared with XOFF2 data. If a match occurs the received data is transferred to RX FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected. Reset Source: mod_g_arstn
4	ENHANCED_EN	R/W	0h	Enhanced functions write enable bit. 0: Disables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. 1: Enables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. Reset Source: mod_g_arstn
3:0	SW_FLOW_CONTROL	R/W	0h	Combinations of Software flow control can be selected by programming bit 3 - bit 0. See Software Flow Control Options Reset Source: mod_g_arstn

14.9.1.5.2.9 UART_FCR Register

1 UART_FCR Register (Offset = 8h) [reset = 0h]

FIFO Control Register
Notes:
Bits 4 and 5 can only be written to when EFR[4] = 1
Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0)
Always make sure that the FIFO is empty when disabling or enabling the FIFO, or reset it if this can't be guaranteed.
See the Transmit FIFO Trigger section of the device TRM for FCR[5:4] setting restriction when SCR[6]=1
See the Recieve FIFO Trigger section of the device TRM for FCR[7:6] setting restriction when SCR[7]=1

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Table 14-17988. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
MCU_UART1	**04A1 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**

Figure 14-5940. UART_FCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN
W		W		W	W	W	W
0h		0h		0h	0h	0h	0h

Table 14-17990. UART_FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	

Table 14-17990. UART_FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	RX_FIFO_TRIG	W	0h	Sets the trigger level for the RX FIFO: If SCR[7] = 0 and TLR[7:4] = 0000: 00: 8 characters 01: 16 characters 10: 56 characters 11: 60 characters If SCR[7] = 0 and TLR[7:4] != 0000, RX_FIFO_TRIG is not considered. If SCR[7]=1, RX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1. Reset Source: mod_g_arstn
5:4	TX_FIFO_TRIG	W	0h	Sets the trigger level for the TX FIFO: If SCR[6] = 0 and TLR[3:0] = 0000: 00: 8 spaces 01: 16 spaces 10: 32 spaces 11: 56 spaces If SCR[6] = 0 and TLR[3:0] != 0000, TX_FIFO_TRIG is not considered. If SCR[6]=1, TX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1 Reset Source: mod_g_arstn
3	DMA_MODE	W	0h	This register is considered if SCR[0] = 0. Reset Source: mod_g_arstn 0 `DMA_MODE 0 (No DMA)` 1 `DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)`
2	TX_FIFO_CLEAR	W	0h	Reset Source: mod_g_arstn 0 `No change` 1 `Clears the transmit FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.`
1	RX_FIFO_CLEAR	W	0h	Reset Source: mod_g_arstn 0 `No change` 1 `Clears the receive FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.`
0	FIFO_EN	W	0h	Reset Source: mod_g_arstn 0 `Disables the transmit and receive FIFOs. The transmit and receive holding registers are one byte FIFOs.` 1 `: Enables the transmit and receive FIFOs.The transmit and receive holding registers are 64-bytes FIFOs.`

14.9.1.5.2.10 UART_IIR_CIR Register

1 UART_IIR_CIR Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 14-17991. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
MCU_UART1	**04A1 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**

Figure 14-5941. UART_IIR_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE		R	NONE	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-17993. UART_IIR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	TX_STATUS_IT	R	0h	Reset Source: mod_g_arstn 0 TX status interrupt inactive 1 TX status interrupt active
4	RESERVED	NONE	0h	Reserved
3	RX_OE_IT	R	0h	Reset Source: mod_g_arstn 0 RX overrun interrupt inactive 1 RX overrun interrupt active

Table 14-17993. UART_IIR_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RX_STOP_IT	R	0h	Reset Source: mod_g_arstn 0 Receive stop interrupt inactive 1 Receive stop interrupt active
1	THR_IT	R	0h	Reset Source: mod_g_arstn 0 THR interrupt inactive 1 THR interrupt active
0	RHR_IT	R	0h	Reset Source: mod_g_arstn 0 RHR interrupt inactive 1 RHR interrupt active

14.9.1.5.2.11 UART_IIR_IRDA Register

1 UART_IIR_IRDA Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Return to Summary Table

Table 14-17994. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
MCU_UART1	**04A1 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**

Figure 14-5942. UART_IIR_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-17996. UART_IIR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EOF_IT	R	0h	Reset Source: mod_g_arstn 0 `Received EOF interrupt inactive` 1 `Received EOF interrupt active`
6	LINE_STS_IT	R	0h	Reset Source: mod_g_arstn 0 `Receiver line status interrupt inactive` 1 `Receiver line status interrupt active`

Table 14-17996. UART_IIR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX_STATUS_IT	R	0h	Reset Source: mod_g_arstn 0 `TX status interrupt inactive` 1 `TX status interrupt active`
4	STS_FIFO_IT	R	0h	Reset Source: mod_g_arstn 0 `Status FIFO trigger level interrupt inactive` 1 `Status FIFO trigger level interrupt active`
3	RX_OE_IT	R	0h	Reset Source: mod_g_arstn 0 `RX overrun interrupt inactive` 1 `RX overrun interrupt active`
2	RX_FIFO_LAST_BYTE_IT	R	0h	Reset Source: mod_g_arstn 0 `Last byte of frame in RX FIFO interrupt inactive` 1 `Last byte of frame in RX FIFO interrupt active`
1	THR_IT	R	0h	Reset Source: mod_g_arstn 0 `THR interrupt inactive` 1 `THR interrupt active`
0	RHR_IT	R	0h	Reset Source: mod_g_arstn 0 `RHR interrupt inactive` 1 `RHR interrupt active`

14.9.1.5.2.12 UART_IIR_UART Register

1 UART_IIR_UART Register (Offset = 8h) [reset = 1h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Return to Summary Table

Table 14-17997. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0008h**
MCU_UART1	**04A1 0008h**
UART0	**0280 0008h**
UART1	**0281 0008h**
UART2	**0282 0008h**
UART3	**0283 0008h**
UART4	**0284 0008h**
UART5	**0285 0008h**
UART6	**0286 0008h**

Figure 14-5943. UART_IIR_UART Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">FCR_MIRROR</td><td colspan="5">IT_TYPE</td><td>IT_PENDING</td></tr>
<tr><td colspan="2">R</td><td colspan="5">R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td colspan="5">0h</td><td>1h</td></tr>
</table>

Table 14-17999. UART_IIR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:6	FCR_MIRROR	R	0h	Mirror the contents of FCR[0] on both bits. Reset Source: mod_g_arstn
5:1	IT_TYPE	R	0h	Reset Source: mod_g_arstn 0 Modem Interrupt. Priority=4 1 THR interrupt. Priority=3 2 RHR interrupt. Priority=2 3 Receiver line status error. Priority=3 6 Rx timeout. Priority=2 8 Xoff/Special character. Priority=5 16 CTS, RTS, DSR change state from active (low) to inactive (high). Priority=6

Table 14-17999. UART_IIR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IT_PENDING	R	1h	Reset Source: mod_g_arstn 0 An interrupt is pending 1 No interrupt is pending

14.9.1.5.2.13 UART_LCR Register

1 UART_LCR Register (Offset = Ch) [reset = 0h]

LCR[6:0] define parameters of the transmission and reception. Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.

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Table 14-18000. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 000Ch**
MCU_UART1	**04A1 000Ch**
UART0	**0280 000Ch**
UART1	**0281 000Ch**
UART2	**0282 000Ch**
UART3	**0283 000Ch**
UART4	**0284 000Ch**
UART5	**0285 000Ch**
UART6	**0286 000Ch**

Figure 14-5944. UART_LCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DIV_EN	BREAK_EN	PARITY_TYPE 2	PARITY_TYPE 1	PARITY_EN	NB_STOP	CHAR_LENGTH	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-18002. UART_LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	DIV_EN	R/W	0h	Reset Source: mod_g_arstn 0 Normal operating condition 1 Divisor latch enable. Allows to access to DLL, DLH and other registers (refer to the registers mapping)

Table 14-18002. UART_LCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BREAK_EN	R/W	0h	Break control bit. Reset Source: mod_g_arstn 0 Normal operating condition. 1 Forces the transmitter output to go low to alert the communication terminal
5	PARITY_TYPE2	R/W	0h	Selects the forced parity format [if LCR[3] = 1]. If LCR[5] = 1 and LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data. Reset Source: mod_g_arstn
4	PARITY_TYPE1	R/W	0h	Reset Source: mod_g_arstn 0 Odd parity is generated (if LCR[3] = 1) 1 Even parity is generated (if LCR[3] = 1)
3	PARITY_EN	R/W	0h	Reset Source: mod_g_arstn 0 No parity 1 A parity bit is generated during transmission and the receiver checks for received parity.
2	NB_STOP	R/W	0h	Specifies the number of stop bits: Reset Source: mod_g_arstn 0 1 stop bits (word length = 5, 6, 7, 8) 1 1.5 stop bits (word length = 5) in USART mode. 2 stop bits (word length = 6, 7, 8)
1:0	CHAR_LENGTH	R/W	0h	Specifies the word length to be transmitted or received. Reset Source: mod_g_arstn 0 5 bits 1 6 bits 2 7 bits 3 8 bits

14.9.1.5.2.14 UART_MCR Register

1 UART_MCR Register (Offset = 10h) [reset = 0h]

MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.

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Table 14-18003. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0010h**
MCU_UART1	**04A1 0010h**
UART0	**0280 0010h**
UART1	**0281 0010h**
UART2	**0282 0010h**
UART3	**0283 0010h**
UART4	**0284 0010h**
UART5	**0285 0010h**
UART6	**0286 0010h**

Figure 14-5945. UART_MCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>TCR_TLR</td><td>XON_EN</td><td>LOOPBACK_EN</td><td>CD_STS_CH</td><td>RI_STS_CH</td><td>RTS</td><td>DTR</td></tr>
<tr><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-18005. UART_MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RESERVED	R	0h	
6	TCR_TLR	R/W	0h	Reset Source: mod_g_arstn 0 No action 1 Enables access to the TCR and TLR registers.
5	XON_EN	R/W	0h	Reset Source: mod_g_arstn 0 Disable 'XON any' function 1 Enable 'XON any' function

Table 14-18005. UART_MCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LOOPBACK_EN	R/W	0h	Reset Source: mod_g_arstn 0 `Normal operating mode` 1 `Enable local loopback mode (internal). In this mode the MCR[3:0] signals are looped back into MSR[7:4]. The transmit output is looped back to the receive input internally`
3	CD_STS_CH	R/W	0h	Reset Source: mod_g_arstn 0 `In loopback forces DCD* input high and IRQ outputs to inactive state.` 1 `In loopback forces DCD* input low and IRQ outputs to inactive state.`
2	RI_STS_CH	R/W	0h	Reset Source: mod_g_arstn 0 `In loopback forces RI* input high.` 1 `In loopback forces RI* input low.`
1	RTS	R/W	0h	In loop back controls MSR[4]. If auto-RTS is enabled the RTS* output is controlled by hardware flow control. Reset Source: mod_g_arstn 0 `Force RTS* output to inactive (high).` 1 `Force RTS* output to active (low).`
0	DTR	R/W	0h	Reset Source: mod_g_arstn 0 `Force DTR* output to inactive (high).` 1 `Force DTR* output to active (low).`

14.9.1.5.2.15 UART_XON1_ADDR1 Register

1 UART_XON1_ADDR1 Register (Offset = 10h) [reset = 0h]

XON1/ADDR1 Register

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Table 14-18006. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0010h**
MCU_UART1	**04A1 0010h**
UART0	**0280 0010h**
UART1	**0281 0010h**
UART2	**0282 0010h**
UART3	**0283 0010h**
UART4	**0284 0010h**
UART5	**0285 0010h**
UART6	**0286 0010h**

Figure 14-5946. UART_XON1_ADDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XON_WORD1							
R/W							
0h							

Table 14-18008. UART_XON1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XON_WORD1	R/W	0h	Used to store the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes. Reset Source: mod_g_arstn

14.9.1.5.2.16 UART_LSR_CIR Register

1 UART_LSR_CIR Register (Offset = 14h) [reset = 81h]

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Table 14-18009. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0014h**
MCU_UART1	**04A1 0014h**
UART0	**0280 0014h**
UART1	**0281 0014h**
UART2	**0282 0014h**
UART3	**0283 0014h**
UART4	**0284 0014h**
UART5	**0285 0014h**
UART6	**0286 0014h**

Figure 14-5947. UART_LSR_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E
R	R	R	NONE				R
1h	0h	0h	0h				1h

Table 14-18011. UART_LSR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	THR_EMPTY	R	1h	Reset Source: mod_g_arstn 0 `Transmit holding register (TX FIFO) is not empty` 1 `Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed`
6	RESERVED	R	0h	

Table 14-18011. UART_LSR_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RX_STOP	R	0h	The RX_STOP is generated based on the value set in the BOF Length register (EBLR). It is cleared on a single read of the LSR register Reset Source: mod_g_arstn 0 `Reception is on going or waiting for a new frame` 1 `Reception is completed`
4:1	RESERVED	NONE	0h	Reserved
0	RX_FIFO_E	R	1h	Reset Source: mod_g_arstn 0 `No data in the receive FIFO` 1 `At least one data character in the RX FIFO`

14.9.1.5.2.17 UART_LSR_IRDA Register

1 UART_LSR_IRDA Register (Offset = 14h) [reset = 83h]

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Table 14-18012. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0014h**
MCU_UART1	**04A1 0014h**
UART0	**0280 0014h**
UART1	**0281 0014h**
UART2	**0282 0014h**
UART3	**0283 0014h**
UART4	**0284 0014h**
UART5	**0285 0014h**
UART6	**0286 0014h**

Figure 14-5948. UART_LSR_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E
R	R	R	R	R	R	R	R
1h	0h	0h	0h	0h	0h	1h	1h

Table 14-18014. UART_LSR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	THR_EMPTY	R	1h	Reset Source: mod_g_arstn 0 Transmit holding register (TX FIFO) is not empty 1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	STS_FIFO_FULL	R	0h	Reset Source: mod_g_arstn 0 Status FIFO not full 1 Status FIFO full

Table 14-18014. UART_LSR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RX_LAST_BYTE	R	0h	Reset Source: mod_g_arstn 0 `The RX FIFO (RHR) does not contain the last byte of the frame to be read` 1 `The RX FIFO (RHR) contains the last byte of the frame to be read.This bit is only set when the last byte of a frame is available to be read. It is used to determine the frame boundary. It is cleared on a single read of the LSR register`
4	FRAME_TOO_LONG	R	0h	Reset Source: mod_g_arstn 0 `No frame-too-long error in frame` 1 `Frame-too-long error in the frame at the top of the STATUS FIFO, [next character to be read]. This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) has been received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected`
3	ABORT	R	0h	Reset Source: mod_g_arstn 0 `No abort pattern error in frame` 1 `Abort pattern is received. SIR & MIR: Abort pattern. FIR: Illegal symbol`
2	CRC	R	0h	Reset Source: mod_g_arstn 0 `No CRC error in frame` 1 `CRC error in the frame at the top of the STATUS FIFO (next character to be read)`
1	STS_FIFO_E	R	1h	Reset Source: mod_g_arstn 0 `Status FIFO not empty` 1 `Status FIFO empty`
0	RX_FIFO_E	R	1h	Reset Source: mod_g_arstn 0 `No data in the receive FIFO` 1 `At least one data character in the RX FIFO`

14.9.1.5.2.18 UART_LSR_UART Register

1 UART_LSR_UART Register (Offset = 14h) [reset = 60h]

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Table 14-18015. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0014h**
MCU_UART1	**04A1 0014h**
UART0	**0280 0014h**
UART1	**0281 0014h**
UART2	**0282 0014h**
UART3	**0283 0014h**
UART4	**0284 0014h**
UART5	**0285 0014h**
UART6	**0286 0014h**

Figure 14-5949. UART_LSR_UART Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E
R	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-18017. UART_LSR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RX_FIFO_STS	R	0h	Reset Source: mod_g_arstn 0 Normal operation 1 At least one parity error, framing error or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.
6	TX_SR_E	R	1h	Reset Source: mod_g_arstn 0 Transmitter hold (TX FIFO) and shift registers are not empty. 1 Transmitter hold (TX FIFO) and shift registers are empty

Table 14-18017. UART_LSR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX_FIFO_E	R	1h	Reset Source: mod_g_arstn 0 Transmit hold register (TX FIFO) is not empty 1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed.
4	RX_BI	R	0h	Reset Source: mod_g_arstn 0 No break condition 1 A break was detected while the data being read from the RX FIFO was being received. (i.e. RX input was low for one character + 1 bit time frame).
3	RX_FE	R	0h	Reset Source: mod_g_arstn 0 No framing error in data being read from RX FIFO. 1 Framing error occurred in data being read from RX FIFO.(received data did not have a valid stop bit)
2	RX_PE	R	0h	Reset Source: mod_g_arstn 0 No parity error in data being read from RX FIFO. 1 Parity error in data being read from RX FIFO
1	RX_OE	R	0h	Reset Source: mod_g_arstn 0 No overrun error 1 Overrun error has occurred. Set when the character held in the receive shift register is not transferred to the RX FIFO. This case can occurs only when receive FIFO is full.
0	RX_FIFO_E	R	0h	Reset Source: mod_g_arstn 0 No data in the receive FIFO 1 At least one data character in the RX FIFO

14.9.1.5.2.19 UART_XON2_ADDR2 Register

1 UART_XON2_ADDR2 Register (Offset = 14h) [reset = 0h]

XON2/ADDR2 Register

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Table 14-18018. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0014h**
MCU_UART1	**04A1 0014h**
UART0	**0280 0014h**
UART1	**0281 0014h**
UART2	**0282 0014h**
UART3	**0283 0014h**
UART4	**0284 0014h**
UART5	**0285 0014h**
UART6	**0286 0014h**

Figure 14-5950. UART_XON2_ADDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XON_WORD2							
R/W							
0h							

Table 14-18020. UART_XON2_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XON_WORD2	R/W	0h	Used to store the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes. Reset Source: mod_g_arstn

14.9.1.5.2.20 UART_MSR Register

1 UART_MSR Register (Offset = 18h) [reset = 0h]

This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.

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Table 14-18021. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0018h**
MCU_UART1	**04A1 0018h**
UART0	**0280 0018h**
UART1	**0281 0018h**
UART2	**0282 0018h**
UART3	**0283 0018h**
UART4	**0284 0018h**
UART5	**0285 0018h**
UART6	**0286 0018h**

Figure 14-5951. UART_MSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18023. UART_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	NCD_STS	R	0h	This bit is the complement of the DCD* input. In loop-back mode it is equivalent to MCR[3] Reset Source: mod_g_arstn
6	NRI_STS	R	0h	This bit is the complement of the RI* input. In loop-back mode it is equivalent to MCR[2] Reset Source: mod_g_arstn
5	NDSR_STS	R	0h	This bit is the complement of the DSR* input. In loop-back mode, it is equivalent to MCR[0] Reset Source: mod_g_arstn

Table 14-18023. UART_MSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	NCTS_STS	R	0h	This bit is the complement of the CTS* input. In loop-back mode it is equivalent to MCR[1] Reset Source: mod_g_arstn
3	DCD_STS	R	0h	Indicates that DCD* input [or MCR[3] in loop back] has changed. Cleared on a read. Reset Source: mod_g_arstn
2	RI_STS	R	0h	Indicates that RI* input [or MCR[2] in loop back] has changed state from low to high. Cleared on a read. Reset Source: mod_g_arstn
1	DSR_STS	R	0h	Reset Source: mod_g_arstn 1 `Indicates that DSR* input (or MCR[0] in loop back) has changed state. Cleared on a read`
0	CTS_STS	R	0h	Reset Source: mod_g_arstn 1 `Indicates that CTS* input (or MCR[1] in loop back) has changed state. Cleared on a read.`

14.9.1.5.2.21 UART_TCR Register

1 UART_TCR Register (Offset = 18h) [reset = Fh]

Transmission Control Register

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Table 14-18024. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0018h**
MCU_UART1	**04A1 0018h**
UART0	**0280 0018h**
UART1	**0281 0018h**
UART2	**0282 0018h**
UART3	**0283 0018h**
UART4	**0284 0018h**
UART5	**0285 0018h**
UART6	**0286 0018h**

Figure 14-5952. UART_TCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			
R/W				R/W			
0h				Fh			

Table 14-18026. UART_TCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	RX_FIFO_TRIG_START	R/W	0h	RX FIFO trigger level to RESTORE transmission (0 - 60) Reset Source: mod_g_arstn
3:0	RX_FIFO_TRIG_HALT	R/W	Fh	RX FIFO trigger level to HALT transmission (0 - 60) Reset Source: mod_g_arstn

14.9.1.5.2.22 UART_XOFF1 Register

1 UART_XOFF1 Register (Offset = 18h) [reset = 0h]

XOFF1 Register

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Table 14-18027. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0018h**
MCU_UART1	**04A1 0018h**
UART0	**0280 0018h**
UART1	**0281 0018h**
UART2	**0282 0018h**
UART3	**0283 0018h**
UART4	**0284 0018h**
UART5	**0285 0018h**
UART6	**0286 0018h**

Figure 14-5953. UART_XOFF1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XOFF_WORD1							
R/W							
0h							

Table 14-18029. UART_XOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XOFF_WORD1	R/W	0h	Used to store the 8-bit XOFF1 character in used in UART modes. Reset Source: mod_g_arstn

14.9.1.5.2.23 UART_SPR Register

1 UART_SPR Register (Offset = 1Ch) [reset = 0h]

This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

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Table 14-18030. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 001Ch**
MCU_UART1	**04A1 001Ch**
UART0	**0280 001Ch**
UART1	**0281 001Ch**
UART2	**0282 001Ch**
UART3	**0283 001Ch**
UART4	**0284 001Ch**
UART5	**0285 001Ch**
UART6	**0286 001Ch**

Figure 14-5954. UART_SPR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SPR_WORD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18032. UART_SPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	SPR_WORD	R/W	0h	Scratchpad register Reset Source: mod_g_arstn

14.9.1.5.2.24 UART_TLR Register

1 UART_TLR Register (Offset = 1Ch) [reset = 0h]

Trigger Level Register

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Table 14-18033. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 001Ch**
MCU_UART1	**04A1 001Ch**
UART0	**0280 001Ch**
UART1	**0281 001Ch**
UART2	**0282 001Ch**
UART3	**0283 001Ch**
UART4	**0284 001Ch**
UART5	**0285 001Ch**
UART6	**0286 001Ch**

Figure 14-5955. UART_TLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			
R/W				R/W			
0h				0h			

Table 14-18035. UART_TLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	RX_FIFO_TRIG_DMA	R/W	0h	Receive FIFO trigger level Reset Source: mod_g_arstn
3:0	TX_FIFO_TRIG_DMA	R/W	0h	Transmit FIFO trigger level Reset Source: mod_g_arstn

14.9.1.5.2.25 UART_XOFF2 Register

1 UART_XOFF2 Register (Offset = 1Ch) [reset = 0h]

XOFF2 Register

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Table 14-18036. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 001Ch**
MCU_UART1	**04A1 001Ch**
UART0	**0280 001Ch**
UART1	**0281 001Ch**
UART2	**0282 001Ch**
UART3	**0283 001Ch**
UART4	**0284 001Ch**
UART5	**0285 001Ch**
UART6	**0286 001Ch**

Figure 14-5956. UART_XOFF2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XOFF_WORD2							
R/W							
0h							

Table 14-18038. UART_XOFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XOFF_WORD2	R/W	0h	Used to store the 8-bit XOFF2 character in used in UART modes. Reset Source: mod_g_arstn

14.9.1.5.2.26 UART_MDR1 Register

1 UART_MDR1 Register (Offset = 20h) [reset = 7h]

The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation.
Note: If the module is disabled by setting the MODE_SELECT field to 111, interrupt requests can still be generated unless disabled through the interrupt enable register (UART_IER). In this case, UART mode interrupts are visible. Reading the interrupt identification register (UART_IIR) shows UART mode interrupt flags.

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Table 14-18039. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0020h**
MCU_UART1	**04A1 0020h**
UART0	**0280 0020h**
UART1	**0281 0020h**
UART2	**0282 0020h**
UART3	**0283 0020h**
UART4	**0284 0020h**
UART5	**0285 0020h**
UART6	**0286 0020h**

Figure 14-5957. UART_MDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		
R/W	R/W	R/W	R/W	R/W	R/W		
0h	0h	0h	0h	0h	7h		

Table 14-18041. UART_MDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	FRAME_END_MODE	R/W	0h	IrDA mode only. Reset Source: mod_g_arstn 0 `Frame-length method` 1 `Set EOT bit method`

Table 14-18041. UART_MDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SIP_MODE	R/W	0h	MIR/FIR modes only. Reset Source: mod_g_arstn 0 `Manual SIP mode: SIP is generated with the control of ACREG[3]` 1 `Automatic SIP mode: SIP is generated after each transmission.`
5	SCT	R/W	0h	Store and control the transmission Reset Source: mod_g_arstn 0 `Starts the Infrared transmission as soon as a value is written to THR` 1 `Starts the Infrared transmission with the control of ACREG[2]. Note: before starting any transmission, there must be no reception on going.`
4	SET_TXIR	R/W	0h	Used to configure the infrared transceiver. Reset Source: mod_g_arstn 0 `No action if MDR2[7]=0. TXIR pin output is forced low if MDR2[7]=1` 1 `TXIR pin output is forced high (not dependant of MDR2[7] value).`
3	IR_SLEEP	R/W	0h	Reset Source: mod_g_arstn 0 `IrDA/CIR sleep mode disabled` 1 `IrDA/CIR sleep mode enabled`
2:0	MODE_SELECT	R/W	7h	Reset Source: mod_g_arstn 0 `UART 16x mode` 1 `SIR mode` 2 `UART 16x auto-baud` 3 `UART 13x mode` 4 `MIR mode` 5 `FIR mode` 6 `CIR mode` 7 `Disable (default state)`

14.9.1.5.2.27 UART_MDR2 Register

1 UART_MDR2 Register (Offset = 24h) [reset = 0h]

IR-IrDA and IR-CIR modes only. MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0]. Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.

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Table 14-18042. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0024h**
MCU_UART1	**04A1 0024h**
UART0	**0280 0024h**
UART1	**0281 0024h**
UART2	**0282 0024h**
UART3	**0283 0024h**
UART4	**0284 0024h**
UART5	**0285 0024h**
UART6	**0286 0024h**

Figure 14-5958. UART_MDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN
R/W	R/W	R/W		R/W	R/W		R
0h	0h	0h		0h	0h		0h

Table 14-18044. UART_MDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	SET_TXIR_ALT	R/W	0h	Provide alternate functionnality for MDR1[4] [SET_TXIR] Reset Source: mod_g_arstn 0 Normal mode 1 Alternate mode for SET_TXIR

Table 14-18044. UART_MDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	IRRXINVERT	R/W	0h	Only for IR mode [IRDA & CIR]Invert RX pin inside the module before the voting or sampling system logic of the infra red block. This will not affect the RX path in UART Modem modes. Reset Source: mod_g_arstn 0 `inversion is performed` 1 `No inversion is performed`
5:4	CIR_PULSE_MODE	R/W	0h	CIR Pulse modulation definition. It defines high level of the pulse width associated with a digit: Reset Source: mod_g_arstn 0 `Pulse width of 3 from 12 cycles` 1 `Pulse width of 4 from 12 cycles` 2 `Pulse width of 5 from 12 cycles` 3 `Pulse width of 6 from 12 cycles`
3	UART_PULSE	R/W	0h	UART mode only. Used to allow pulse shaping in UART mode. Reset Source: mod_g_arstn 0 `normal UART mode` 1 `UART mode with a pulse shaping`
2:1	STS_FIFO_TRIG	R/W	0h	Only for IR-IRDA mode. Frame Status FIFO Threshold select: Reset Source: mod_g_arstn 0 `1 entry` 1 `4 entries` 2 `7 entries` 3 `8 entries`
0	IRTX_UNDERRUN	R	0h	IRDA Transmission status interrupt.When the IIR[5] interrupt occurs, the meaning of the interrupt is : Reset Source: mod_g_arstn 0 `the last bit of the frame has been transmitted successfully without error.` 1 `an underrun has occurred. The last bit of the frame has been transmitted but with an underrun error present. The bit is reset to '0' when the RESUME register is read.`

14.9.1.5.2.28 UART_SFLSR Register

1 UART_SFLSR Register (Offset = 28h) [reset = 0h]

IrDA modes only. Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).

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Table 14-18045. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0028h**
MCU_UART1	**04A1 0028h**
UART0	**0280 0028h**
UART1	**0281 0028h**
UART2	**0282 0028h**
UART3	**0283 0028h**
UART4	**0284 0028h**
UART5	**0285 0028h**
UART6	**0286 0028h**

Figure 14-5959. UART_SFLSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED5</td><td>OE_ERROR</td><td>FRAME_TOO_LONG_ERROR</td><td>ABORT_DETECT</td><td>CRC_ERROR</td><td>RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-18047. UART_SFLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED5	R	0h	
4	OE_ERROR	R	0h	Reset Source: mod_g_arstn 1 Overrun error in RX FIFO when frame at top of RX FIFO was received.
3	FRAME_TOO_LONG_ERROR	R	0h	Reset Source: mod_g_arstn 1 Frame-length too long error in frame at top of RX FIFO.

Table 14-18047. UART_SFLSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ABORT_DETECT	R	0h	Reset Source: mod_g_arstn 1 `Abort pattern detected in frame at top of RX FIFO`
1	CRC_ERROR	R	0h	Reset Source: mod_g_arstn 1 `CRC error in frame at top of RX FIFO. top of RX FIFO = Next frame to be read from RX FIFO`
0	RESERVED0	R	0h	

14.9.1.5.2.29 UART_TXFLL Register

1 UART_TXFLL Register (Offset = 28h) [reset = 0h]

IrDA modes only. The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 14-18048. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0028h**
MCU_UART1	**04A1 0028h**
UART0	**0280 0028h**
UART1	**0281 0028h**
UART2	**0282 0028h**
UART3	**0283 0028h**
UART4	**0284 0028h**
UART5	**0285 0028h**
UART6	**0286 0028h**

Figure 14-5960. UART_TXFLL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
TXFLL							
W							
0h							

Table 14-18050. UART_TXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	TXFLL	W	0h	LSB register used to specify the frame length Reset Source: mod_g_arstn

14.9.1.5.2.30 UART_RESUME Register

1 UART_RESUME Register (Offset = 2Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only. This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

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Table 14-18051. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 002Ch**
MCU_UART1	**04A1 002Ch**
UART0	**0280 002Ch**
UART1	**0281 002Ch**
UART2	**0282 002Ch**
UART3	**0283 002Ch**
UART4	**0284 002Ch**
UART5	**0285 002Ch**
UART6	**0286 002Ch**

Figure 14-5961. UART_RESUME Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESUME							
R							
0h							

Table 14-18053. UART_RESUME Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RESUME	R	0h	Dummy read to restart the TX or RX Reset Source: mod_g_arstn

14.9.1.5.2.31 UART_TXFLH Register

1 UART_TXFLH Register (Offset = 2Ch) [reset = 0h]

IrDA modes only. The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 14-18054. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 002Ch**
MCU_UART1	**04A1 002Ch**
UART0	**0280 002Ch**
UART1	**0281 002Ch**
UART2	**0282 002Ch**
UART3	**0283 002Ch**
UART4	**0284 002Ch**
UART5	**0285 002Ch**
UART6	**0286 002Ch**

Figure 14-5962. UART_TXFLH Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			TXFLH				
R			W				
0h			0h				

Table 14-18056. UART_TXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED	R	0h	
4:0	TXFLH	W	0h	MSB register used to specify the frame length Reset Source: mod_g_arstn

14.9.1.5.2.32 UART_RXFLL Register

1 UART_RXFLL Register (Offset = 30h) [reset = 0h]

IrDA modes only. The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 14-18057. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0030h**
MCU_UART1	**04A1 0030h**
UART0	**0280 0030h**
UART1	**0281 0030h**
UART2	**0282 0030h**
UART3	**0283 0030h**
UART4	**0284 0030h**
UART5	**0285 0030h**
UART6	**0286 0030h**

Figure 14-5963. UART_RXFLL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RXFLL							
W							
0h							

Table 14-18059. UART_RXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RXFLL	W	0h	LSB register used to specify the frame length in reception Reset Source: mod_g_arstn

14.9.1.5.2.33 UART_SFREGL Register

1 UART_SFREGL Register (Offset = 30h) [reset = 0h]

IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 14-18060. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0030h**
MCU_UART1	**04A1 0030h**
UART0	**0280 0030h**
UART1	**0281 0030h**
UART2	**0282 0030h**
UART3	**0283 0030h**
UART4	**0284 0030h**
UART5	**0285 0030h**
UART6	**0286 0030h**

Figure 14-5964. UART_SFREGL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SFREGL							
R							
0h							

Table 14-18062. UART_SFREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	SFREGL	R	0h	LSB part of the frame length Reset Source: mod_g_arstn

14.9.1.5.2.34 UART_RXFLH Register

1 UART_RXFLH Register (Offset = 34h) [reset = 0h]

IrDA modes only. The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 14-18063. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0034h**
MCU_UART1	**04A1 0034h**
UART0	**0280 0034h**
UART1	**0281 0034h**
UART2	**0282 0034h**
UART3	**0283 0034h**
UART4	**0284 0034h**
UART5	**0285 0034h**
UART6	**0286 0034h**

Figure 14-5965. UART_RXFLH Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RXFLH			
R				W			
0h				0h			

Table 14-18065. UART_RXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:4	RESERVED	R	0h	
3:0	RXFLH	W	0h	MSB register used to specify the frame length in reception Reset Source: mod_g_arstn

14.9.1.5.2.35 UART_SFREGH Register

1 UART_SFREGH Register (Offset = 34h) [reset = 0h]

IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 14-18066. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0034h**
MCU_UART1	**04A1 0034h**
UART0	**0280 0034h**
UART1	**0281 0034h**
UART2	**0282 0034h**
UART3	**0283 0034h**
UART4	**0284 0034h**
UART5	**0285 0034h**
UART6	**0286 0034h**

Figure 14-5966. UART_SFREGH Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				SFREGH			
R				R			
0h				0h			

Table 14-18068. UART_SFREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:4	RESERVED	R	0h	
3:0	SFREGH	R	0h	MSB part of the frame length Reset Source: mod_g_arstn

14.9.1.5.2.36 UART_BLR Register

1 UART_BLR Register (Offset = 38h) [reset = 40h]

IrDA modes only. Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

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Table 14-18069. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0038h**
MCU_UART1	**04A1 0038h**
UART0	**0280 0038h**
UART1	**0281 0038h**
UART2	**0282 0038h**
UART3	**0283 0038h**
UART4	**0284 0038h**
UART5	**0285 0038h**
UART6	**0286 0038h**

Figure 14-5967. UART_BLR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
STS_FIFO_RESET	XBOF_TYPE	RESERVED					
R/W1TS	R/W	R					
0h	1h	0h					

Table 14-18071. UART_BLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	STS_FIFO_RESET	R/W1TS	0h	Status FIFO reset. This bit is self-clearing Reset Source: mod_g_arstn
6	XBOF_TYPE	R/W	1h	SIR xBOF select. Reset Source: mod_g_arstn 0 0xFF 1 0xC0

Table 14-18071. UART_BLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	RESERVED	R	0h	

14.9.1.5.2.37 UART_UASR Register

1 UART_UASR Register (Offset = 38h) [reset = 0h]

UART Autobauding Status Register

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Table 14-18072. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0038h**
MCU_UART1	**04A1 0038h**
UART0	**0280 0038h**
UART1	**0281 0038h**
UART2	**0282 0038h**
UART3	**0283 0038h**
UART4	**0284 0038h**
UART5	**0285 0038h**
UART6	**0286 0038h**

Figure 14-5968. UART_UASR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PARITY_TYPE		BIT_BY_CHAR	SPEED				
R		R	R				
0h		0h	0h				

Table 14-18074. UART_UASR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	PARITY_TYPE	R	0h	00 => No Parity identified. 01 => Parity space. 10 => Even Parity. 11 => Odd Parity Reset Source: mod_g_arstn
5	BIT_BY_CHAR	R	0h	0 => 7 bits character identified. 1 => 8 bits character identified Reset Source: mod_g_arstn

Table 14-18074. UART_UASR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	SPEED	R	0h	Used to report the speed identified. 00000 => No speed identified. 00001 => 115200 bauds. 00010 => 57600 bauds. 00011 => 38400 bauds. 00100 => 28800 bauds. 00101 => 19200 bauds. 00110 => 14400 bauds. 00111 => 9600 bauds. 01000 => 4800 bauds. 01001 => 2400 bauds. 01010 => 1200 bauds Reset Source: mod_g_arstn

14.9.1.5.2.38 UART_ACREG Register

1 UART_ACREG Register (Offset = 3Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only.

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Table 14-18075. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 003Ch**
MCU_UART1	**04A1 003Ch**
UART0	**0280 003Ch**
UART1	**0281 003Ch**
UART2	**0282 003Ch**
UART3	**0283 003Ch**
UART4	**0284 003Ch**
UART5	**0285 003Ch**
UART6	**0286 003Ch**

Figure 14-5969. UART_ACREG Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN
R/W	R/W	R/W	R/W	R/W1TS	R/W1TS	R/W	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18077. UART_ACREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	PULSE_TYPE	R/W	0h	SIR pulse width select: Reset Source: mod_g_arstn 0 3/16 of baud-rate pulse width 1 1.6us
6	SD_MOD	R/W	0h	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers. Reset Source: mod_g_arstn 0 SD pin is set to high 1 SD pin is set to low

Table 14-18077. UART_ACREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DIS_IR_RX	R/W	0h	Reset Source: mod_g_arstn 0 `Normal operation (RX input automatically disabled during transmit but enabled outside of transmit operation).` 1 `Disables RX input (permanent state - independent of transmit).`
4	DIS_TX_UNDERRUN	R/W	0h	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4]=1, garbage data is sent over TX line. Reset Source: mod_g_arstn 0 `Long stop bits cannot be transmitted, TX underrun is enabled` 1 `Long stop bits can be transmitted, TX underrun is disabled`
3	SEND_SIP	R/W1TS	0h	MIR/FIR Modes only.Send Serial Infrared Interaction Pulse [SIP] If this bit is set during a MIR/FIR transmission, the SIP will be send at the end of it.This bit automatically gets cleared at the end of the SIP transmission. Reset Source: mod_g_arstn 0 `No action` 1 `Send SIP pulse.`
2	SCTX_EN	R/W1TS	0h	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit the TX state machine starts frame transmission. This bit is self-clearing. Reset Source: mod_g_arstn
1	ABORT_EN	R/W	0h	Frame Abort. The LH can intentionally abort transmission of a frame by Writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If transmit FIFO is not empty and MDR1[5]=1, UART IrDA will start a new transfer with data of previous frame as soon as abort frame has been sent. Therefore, TX FIFO must be reset before sending an abort frame. Reset Source: mod_g_arstn
0	EOT_EN	R/W1TS	0h	EOT [end of transmission] bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit automatically gets cleared when the LH writes to the THR [TX FIFO]. Reset Source: mod_g_arstn

14.9.1.5.2.39 UART_SCR Register

1 UART_SCR Register (Offset = 40h) [reset = 0h]

Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.

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Table 14-18078. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0040h**
MCU_UART1	**04A1 0040h**
UART0	**0280 0040h**
UART1	**0281 0040h**
UART2	**0282 0040h**
UART3	**0283 0040h**
UART4	**0284 0040h**
UART5	**0285 0040h**
UART6	**0286 0040h**

Figure 14-5970. UART_SCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2		DMA_MODE_CTL
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		0h

Table 14-18080. UART_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RX_TRIG_GRANU1	R/W	0h	Reset Source: mod_g_arstn 0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL. 1 ENABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL.

Table 14-18080. UART_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TX_TRIG_GRANU1	R/W	0h	Reset Source: mod_g_arstn 0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER TX LEVEL. 1 Enables the granularity of 1 for trigger TX level.
5	DSR_IT	R/W	0h	Reset Source: mod_g_arstn 0 DISABLES DSR* INTERRUPT. 1 ENABLES DSR* INTERRUPT.
4	RX_CTS_DSR_WAKE_UP_ENABLE	R/W	0h	Reset Source: mod_g_arstn 0 DISABLES THE WAKE UP INTERRUPT AND CLEARS SSR[1]. 1 Waits for a falling edge of pins RX, CTS* or DSR* to generate an interrupt
3	TX_EMPTY_CTL_IT	R/W	0h	Reset Source: mod_g_arstn 0 Normal mode for THR interrupt (See UART mode interrupts table). 1 THE THR INTERRUPT IS GENERATED WHEN TX FIFO AND TX SHIFT REGISTER ARE EMPTY.
2:1	DMA_MODE_2	R/W	0h	Used to specify the DMA mode valid if SCR[0] = 1 Reset Source: mod_g_arstn 0 DMA mode 0 (no DMA) 1 DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX) 2 DMA mode 2 (UART_nDMA_REQ[0] in RX) 3 DMA mode 3 (UART_nDMA_REQ[0] in TX)
0	DMA_MODE_CTL	R/W	0h	Reset Source: mod_g_arstn 0 The DMA_MODE is set with FCR[3] 1 The DMA_MODE is set with SCR[2:1]

14.9.1.5.2.40 UART_SSR Register

1 UART_SSR Register (Offset = 44h) [reset = 4h]

Note: Bit 1 is reset only when SCR[4] is reset to 0.

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Table 14-18081. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0044h**
MCU_UART1	**04A1 0044h**
UART0	**0280 0044h**
UART1	**0281 0044h**
UART2	**0282 0044h**
UART3	**0283 0044h**
UART4	**0284 0044h**
UART5	**0285 0044h**
UART6	**0286 0044h**

Figure 14-5971. UART_SSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL
R					R/W	R	R
0h					1h	0h	0h

Table 14-18083. UART_SSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:3	RESERVED	R	0h	
2	DMA_COUNTER_RST	R/W	1h	Reset Source: mod_g_arstn 0 The DMA counter will not be reset if the corresponding FIFO is reset (via FCR[1] or FCR[2]) 1 The DMA counter will be reset if corresponding FIFO is reset (via FCR[1] or FCR[2])

Table 14-18083. UART_SSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RX_CTS_DSR_WAKE_UP_STS	R	0h	Reset Source: mod_g_arstn 0 `No falling edge event on RX, CTS* and DSR*` 1 `A falling edge occurred on RX, CTS* or DSR*`
0	TX_FIFO_FULL	R	0h	Reset Source: mod_g_arstn 0 `TX FIFO is not full` 1 `TX FIFO is full.`

14.9.1.5.2.41 UART_EBLR Register

1 UART_EBLR Register (Offset = 48h) [reset = 0h]

IR-IrDA and IR-CIR modes only.
In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.
In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).
In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the UART_ACREG[5] to 1. Note: If the RX_STOP interrupt occurs before a byte boundary, the remaining bits of the last byte are filled with 0s and passed into the RX FIFO.

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Table 14-18084. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0048h**
MCU_UART1	**04A1 0048h**
UART0	**0280 0048h**
UART1	**0281 0048h**
UART2	**0282 0048h**
UART3	**0283 0048h**
UART4	**0284 0048h**
UART5	**0285 0048h**
UART6	**0286 0048h**

Figure 14-5972. UART_EBLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EBLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18086. UART_EBLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	

Table 14-18086. UART_EBLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	EBLR	R/W	0h	IR-IRDA mode: This register allows to define up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt [IIR[2]]. 0x00: feature disabled. 0x01: generate RX_STOP interrupt after receiving one zero bit. ... 0xFF: generate RX_STOP interrupt after receiving 255 zero bits. Reset Source: mod_g_arstn

14.9.1.5.2.42 UART_MVR Register

1 UART_MVR Register (Offset = 50h) [reset = 47424603h]

The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned Notes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification). For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8

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Table 14-18087. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0050h**
MCU_UART1	**04A1 0050h**
UART0	**0280 0050h**
UART1	**0281 0050h**
UART2	**0282 0050h**
UART3	**0283 0050h**
UART4	**0284 0050h**
UART5	**0285 0050h**
UART6	**0286 0050h**

Figure 14-5973. UART_MVR Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		R		R			
1h		0h		742h			
23	22	21	20	19	18	17	16
FUNC							
R							
742h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
8h					6h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		3h					

Table 14-18089. UART_MVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme revision number of module Reset Source: mod_g_arstn
29:28	RESERVED	R	0h	
27:16	FUNC	R	742h	Function revision number of module Reset Source: mod_g_arstn

Table 14-18089. UART_MVR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:11	RTL	R	8h	Rtl revision number of module Reset Source: mod_g_arstn
10:8	MAJOR	R	6h	Major revision number of the module. Reset Source: mod_g_arstn
7:6	CUSTOM	R	0h	Custom revision number of the module. Reset Source: mod_g_arstn
5:0	MINOR	R	3h	Minor revision number of the module. Reset Source: mod_g_arstn

14.9.1.5.2.43 UART_SYSC Register

1 UART_SYSC Register (Offset = 54h) [reset = 0h]

The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.

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Table 14-18090. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0054h**
MCU_UART1	**04A1 0054h**
UART0	**0280 0054h**
UART1	**0281 0054h**
UART2	**0282 0054h**
UART3	**0283 0054h**
UART4	**0284 0054h**
UART5	**0285 0054h**
UART6	**0286 0054h**

Figure 14-5974. UART_SYSC Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R			R/W		R/W	W	R/W
0h			0h		0h	0h	0h

Table 14-18092. UART_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED	R	0h	

Table 14-18092. UART_SYSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	IDLEMODE	R/W	0h	POWER MANAGEMENT REQ/ACK CONTROL REF: OCP DESIGN GUIDELINES VERSION 1.1 Reset Source: mod_g_arstn 0 `Force idle. An idle request is acknowledged unconditionally` 1 `No-idle. An idle request is never acknowledged.` 2 `Smart idle. Acknowledgement to an idle request is given based in the internal activity of the module.` 3 `reserved`
2	ENAWAKEUP	R/W	0h	WAKE UP FEATURE CONTROL Reset Source: mod_g_arstn 0 `Wake up is disabled` 1 `Wake up capability is enabled`
1	SOFTRESET	W	0h	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. During reads it always returns a 0. Reset Source: mod_g_arstn 0 `Normal mode` 1 `The module is reset`
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy Reset Source: mod_g_arstn 0 `Clock is running` 1 `Automatic OCP clock gating strategy is applied, based on the OCP interface activity`

14.9.1.5.2.44 UART_SYSS Register

1 UART_SYSS Register (Offset = 58h) [reset = 0h]

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Table 14-18093. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0058h**
MCU_UART1	**04A1 0058h**
UART0	**0280 0058h**
UART1	**0281 0058h**
UART2	**0282 0058h**
UART3	**0283 0058h**
UART4	**0284 0058h**
UART5	**0285 0058h**
UART6	**0286 0058h**

Figure 14-5975. UART_SYSS Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							0h

Table 14-18095. UART_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:1	RESERVED	R	0h	
0	RESETDONE	R	0h	Internal Reset Monitoring Reset Source: mod_g_arstn 0 Internal Module Reset is ongoing 1 Reset completed

14.9.1.5.2.45 UART_WER Register

1 UART_WER Register (Offset = 5Ch) [reset = FFh]

The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.

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Table 14-18096. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 005Ch**
MCU_UART1	**04A1 005Ch**
UART0	**0280 005Ch**
UART1	**0281 005Ch**
UART2	**0282 005Ch**
UART3	**0283 005Ch**
UART4	**0284 005Ch**
UART5	**0285 005Ch**
UART6	**0286 005Ch**

Figure 14-5976. UART_WER Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
EVENT_7_TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RI_ACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h

Table 14-18098. UART_WER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	EVENT_7_TX_WAKEUP_EN	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 EVENT CAN WAKE UP THE SYSTEM: Event can be: THR_IT or TX_DMA request and/or TX_SATUS_IT

Table 14-18098. UART_WER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
5	EVENT_5_RHR_INTERRUPT	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
4	EVENT_4_RX_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
3	EVENT_3_DCD_CD_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
2	EVENT_2_RI_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
1	EVENT_1_DSR_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system
0	EVENT_0_CTS_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 0 Event is not allowed to wake up the system 1 Event can wake up the system

14.9.1.5.2.46 UART_CFPS Register

1 UART_CFPS Register (Offset = 60h) [reset = 69h]

Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.

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Table 14-18099. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0060h**
MCU_UART1	**04A1 0060h**
UART0	**0280 0060h**
UART1	**0281 0060h**
UART2	**0282 0060h**
UART3	**0283 0060h**
UART4	**0284 0060h**
UART5	**0285 0060h**
UART6	**0286 0060h**

Figure 14-5977. UART_CFPS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CFPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">69h</td></tr>
</table>

Table 14-18101. UART_CFPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	

Table 14-18101. UART_CFPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	CFPS	R/W	69h	System clock frequency prescaler at [12x multiple]. Examples for CFPS values are given in the table below. Target Freq [KHz] CFPS [decimal] Actual Freq[KHz] 30 133 30.08 32.75 122 32.79 36 111 36.04 36.7 109 36.69 38* 105 38.1 40 100 40 56.8 70 57.14 * configured at reset to this value Note: CFPS = 0 is not supported. Reset Source: mod_g_arstn

14.9.1.5.2.47 UART_RXFIFO_LVL Register

1 UART_RXFIFO_LVL Register (Offset = 64h) [reset = 0h]

Level of the RX FIFO

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Table 14-18102. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0064h**
MCU_UART1	**04A1 0064h**
UART0	**0280 0064h**
UART1	**0281 0064h**
UART2	**0282 0064h**
UART3	**0283 0064h**
UART4	**0284 0064h**
UART5	**0285 0064h**
UART6	**0286 0064h**

Figure 14-5978. UART_RXFIFO_LVL Name Register

31	30	29	28	27	26	25	24
RESERVED24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED24							
R							
0h							
7	6	5	4	3	2	1	0
RXFIFO_LVL							
R							
0h							

Table 14-18104. UART_RXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	
7:0	RXFIFO_LVL	R	0h	Reset Source: mod_g_arstn

14.9.1.5.2.48 UART_TXFIFO_LVL Register

1 UART_TXFIFO_LVL Register (Offset = 68h) [reset = 0h]

Level of the TX FIFO

Return to Summary Table

Table 14-18105. Instance Table

Instance Name	Physical Address
MCU_UART0	04A0 0068h
MCU_UART1	04A1 0068h
UART0	0280 0068h
UART1	0281 0068h
UART2	0282 0068h
UART3	0283 0068h
UART4	0284 0068h
UART5	0285 0068h
UART6	0286 0068h

Figure 14-5979. UART_TXFIFO_LVL Name Register

31	30	29	28	27	26	25	24
RESERVED24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED24							
R							
0h							
7	6	5	4	3	2	1	0
TXFIFO_LVL							
R							
0h							

Table 14-18107. UART_TXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	
7:0	TXFIFO_LVL	R	0h	Reset Source: mod_g_arstn

14.9.1.5.2.49 UART_IER2 Register

1 UART_IER2 Register (Offset = 6Ch) [reset = 0h]

Enables RX/TX FIFOs empty corresponding interrupts.

Return to Summary Table

Table 14-18108. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 006Ch**
MCU_UART1	**04A1 006Ch**
UART0	**0280 006Ch**
UART1	**0281 006Ch**
UART2	**0282 006Ch**
UART3	**0283 006Ch**
UART4	**0284 006Ch**
UART5	**0285 006Ch**
UART6	**0286 006Ch**

Figure 14-5980. UART_IER2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					RHR_IT_DIS	EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-18110. UART_IER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:3	RESERVED	R	0h	
2	RHR_IT_DIS	R/W	0h	Reset Source: mod_g_arstn 0 Enables the RHR interrupt. 1 Disables the RHR interrupt.
1	EN_TXFIFO_EMPTY	R/W	0h	Enables[1]/DISABLES[00 EN_TXFIFO_EMPTY interrupt. Reset Source: mod_g_arstn
0	EN_RXFIFO_EMPTY	R/W	0h	Enables[1]/disables[0] EN_RXFIFO_EMPTY interrupt. Reset Source: mod_g_arstn

14.9.1.5.2.50 UART_ISR2 Register

1 UART_ISR2 Register (Offset = 70h) [reset = 3h]

Status of RX/TX FIFOs empty corresponding interrupts.

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Table 14-18111. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0070h**
MCU_UART1	**04A1 0070h**
UART0	**0280 0070h**
UART1	**0281 0070h**
UART2	**0282 0070h**
UART3	**0283 0070h**
UART4	**0284 0070h**
UART5	**0285 0070h**
UART6	**0286 0070h**

Figure 14-5981. UART_ISR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TXFIFO_EMPTY_STS</td><td>RXFIFO_EMPTY_STS</td></tr>
<tr><td colspan="6">R</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-18113. UART_ISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:2	RESERVED	R	0h	
1	TXFIFO_EMPTY_STS	R/W1TC	1h	TXFIFO interrupt pending Reset Source: mod_g_arstn 0 TXFIFO_EMPTY interrupt not pending. 1 TXFIFO_EMPTY interrupt pending.

Table 14-18113. UART_ISR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RXFIFO_EMPTY_STS	R/W1TC	1h	RXFIFO interrupt pending Reset Source: mod_g_arstn 0 `RXFIFO_EMPTY interrupt not pending.` 1 `RXFIFO_EMPTY interrupt pending.`

14.9.1.5.2.51 UART_FREQ_SEL Register

1 UART_FREQ_SEL Register (Offset = 74h) [reset = 1Ah]

Sample per bit value selector

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Table 14-18114. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0074h**
MCU_UART1	**04A1 0074h**
UART0	**0280 0074h**
UART1	**0281 0074h**
UART2	**0282 0074h**
UART3	**0283 0074h**
UART4	**0284 0074h**
UART5	**0285 0074h**
UART6	**0286 0074h**

Figure 14-5982. UART_FREQ_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
FREQ_SEL							
R/W							
1Ah							

Table 14-18116. UART_FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	RESERVED
7:0	FREQ_SEL	R/W	1Ah	Sets the sample per bit if non default frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal or higher then 6. Reset Source: mod_g_arstn

14.9.1.5.2.52 UART_ABAUD_1ST_CHAR Register

1 UART_ABAUD_1ST_CHAR Register (Offset = 78h) [reset = 0h]

Unused

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Table 14-18117. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0078h**
MCU_UART1	**04A1 0078h**
UART0	**0280 0078h**
UART1	**0281 0078h**
UART2	**0282 0078h**
UART3	**0283 0078h**
UART4	**0284 0078h**
UART5	**0285 0078h**
UART6	**0286 0078h**

Figure 14-5983. UART_ABAUD_1ST_CHAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-18119. UART_ABAUD_1ST_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	

14.9.1.5.2.53 UART_BAUD_2ND_CHAR Register

1 UART_BAUD_2ND_CHAR Register (Offset = 7Ch) [reset = 0h]

Unused

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Table 14-18120. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 007Ch**
MCU_UART1	**04A1 007Ch**
UART0	**0280 007Ch**
UART1	**0281 007Ch**
UART2	**0282 007Ch**
UART3	**0283 007Ch**
UART4	**0284 007Ch**
UART5	**0285 007Ch**
UART6	**0286 007Ch**

Figure 14-5984. UART_BAUD_2ND_CHAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-18122. UART_BAUD_2ND_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	

14.9.1.5.2.54 UART_MDR3 Register

1 UART_MDR3 Register (Offset = 80h) [reset = 0h]

Mode definition register 3.

Return to Summary Table

Table 14-18123. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0080h**
MCU_UART1	**04A1 0080h**
UART0	**0280 0080h**
UART1	**0281 0080h**
UART2	**0282 0080h**
UART3	**0283 0080h**
UART4	**0284 0080h**
UART5	**0285 0080h**
UART6	**0286 0080h**

Figure 14-5985. UART_MDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			DIR_EN	DIR_POL	SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-18125. UART_MDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	
7:5	RESERVED1	R	0h	Reserved
4	DIR_EN	R/W	0h	RS-485 External Transceiver Direction Enable Reset Source: mod_g_arstn
3	DIR_POL	R/W	0h	RS-485 External Transceiver Direction Polarity. 0 => TX: RTS=0, RX: RTS=1. 1 => TX: RTS=1, RX: RTS=0 Reset Source: mod_g_arstn
2	SET_DMA_TX_THRESHOLD	R/W	0h	Enable to set different TX DMA threshold then 64-trigger [usage of new register TX_DNA_THRESHOLD] Reset Source: mod_g_arstn

Table 14-18125. UART_MDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NONDEFAULT_FREQ	R/W	0h	Enables[1]/Disables[0] using NONDEFAULT fclk frequencies Reset Source: mod_g_arstn
0	DISABLE_CIR_RX_DEMOD	R/W	0h	Disables[1]/Enables[0] CIR RX demodulation Reset Source: mod_g_arstn 0 Enables CIR RX demodulation 1 Disables CIR RX demodulation

14.9.1.5.2.55 UART_TX_DMA_THRESHOLD Register

1 UART_TX_DMA_THRESHOLD Register (Offset = 84h) [reset = 0h]

Use to manually set the TX DMA threshold level. MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size). If not, 64-tx_trigger_level will be used w/o modifying the value of this register.

Return to Summary Table

Table 14-18126. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0084h**
MCU_UART1	**04A1 0084h**
UART0	**0280 0084h**
UART1	**0281 0084h**
UART2	**0282 0084h**
UART3	**0283 0084h**
UART4	**0284 0084h**
UART5	**0285 0084h**
UART6	**0286 0084h**

Figure 14-5986. UART_TX_DMA_THRESHOLD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TX_DMA_THRESHOLD</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-18128. UART_TX_DMA_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	RESERVED
7:6	RESERVED	R	0h	Reserved
5:0	TX_DMA_THRESHOLD	R/W	0h	Use to manually set the TX DMA threshold level. Reset Source: mod_g_arstn

14.9.1.5.2.56 UART_MDR4 Register

1 UART_MDR4 Register (Offset = 88h) [reset = 0h]

Mode definition register 4

Return to Summary Table

Table 14-18129. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0088h**
MCU_UART1	**04A1 0088h**
UART0	**0280 0088h**
UART1	**0281 0088h**
UART2	**0282 0088h**
UART3	**0283 0088h**
UART4	**0284 0088h**
UART5	**0285 0088h**
UART6	**0286 0088h**

Figure 14-5987. UART_MDR4 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	MODE9	FREQ_SEL_H			MODE		
R	R/W	R/W			R/W		
0h	0h	0h			0h		

Table 14-18131. UART_MDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	RESERVED	R	0h	
6	MODE9	R/W	0h	9-bit character length. When '1', overrides character length setting in LCR Reset Source: mod_g_arstn
5:3	FREQ_SEL_H	R/W	0h	Upper 3 bits of FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode Reset Source: mod_g_arstn

Table 14-18131. UART_MDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	MODE	R/W	0h	New modes [when set, overrides MDR1 modes] Reset Source: mod_g_arstn 0 disabled (no override) 1 reserved 2 Synchronous mode with external clock 3 Synchronous mode with generated clock 4 ISO 7816 mode T=0 5 ISO 7816 mode T=1 6 reserved 7 reserved

14.9.1.5.2.57 UART_EFR2 Register

1 UART_EFR2 Register (Offset = 8Ch) [reset = 0h]

Enhanced Features Register 2

Return to Summary Table

Table 14-18132. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 008Ch**
MCU_UART1	**04A1 008Ch**
UART0	**0280 008Ch**
UART1	**0281 008Ch**
UART2	**0282 008Ch**
UART3	**0283 008Ch**
UART4	**0284 008Ch**
UART5	**0285 008Ch**
UART6	**0286 008Ch**

Figure 14-5988. UART_EFR2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
BROADCAST	TIMEOUT_BEHAVE	C8	C4	C2	MULTIDROP	RHR_OVERRUN	ENDIAN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18134. UART_EFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	BROADCAST	R/W	0h	Enables broadcast address matching in multi-drop address match mode Reset Source: mod_g_arstn
6	TIMEOUT_BEHAVE	R/W	0h	Specifies how timeout is measured Reset Source: mod_g_arstn 0 `timeout after at least one character has been received` 1 `periodic timeout even when no character has been received`

Table 14-18134. UART_EFR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	C8	R/W	0h	Value for ISO 7816 C8 pin for software control Reset Source: mod_g_arstn
4	C4	R/W	0h	Value for ISO 7816 C4 pin for software control Reset Source: mod_g_arstn
3	C2	R/W	0h	Value for ISO 7816 reset pin [software controllable] Reset Source: mod_g_arstn
2	MULTIDROP	R/W	0h	Enables parity Multi-drop mode [overrides LCR[5..3]] when '1' Reset Source: mod_g_arstn

1	RHR_OVERRUN	R/W	0h	RHR Overrun behaviour when buffer full
				Reset Source: mod_g_arstn
				`0 data in RHR is not overwritten (standard)`
				`1 data in RHR is overwritten when buffer full (and FIFO disabled)`

0	ENDIAN	R/W	0h	Endianness
				Reset Source: mod_g_arstn
				`0 Little Endian (LSB First)`
				`1 Big Endian (MSB First)`

14.9.1.5.2.58 UART_ECR Register

1 UART_ECR Register (Offset = 90h) [reset = 18h]

Enhanced Control register

Return to Summary Table

Table 14-18135. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0090h**
MCU_UART1	**04A1 0090h**
UART0	**0280 0090h**
UART1	**0281 0090h**
UART2	**0282 0090h**
UART3	**0283 0090h**
UART4	**0284 0090h**
UART5	**0285 0090h**
UART6	**0286 0090h**

Figure 14-5989. UART_ECR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		CLEAR_TX_PE	TX_EN	RX_EN	TX_RST	RX_RST	A_MULTIDROP
R		W	R/W	R/W	W	W	W
0h		0h	1h	1h	0h	0h	0h

Table 14-18137. UART_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:6	RESERVED	R	0h	
5	CLEAR_TX_PE	W	0h	Write 1 to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only] Reset Source: mod_g_arstn
4	TX_EN	R/W	1h	Enables/Disables the transmitter Reset Source: mod_g_arstn 0 Transmitter is shut down 1 Transmitter is working

Table 14-18137. UART_ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

3	RX_EN	R/W	1h	Enables/Disables the receiver
				Reset Source: mod_g_arstn
				`0      Receiver is shut down`
				`1      Receiver is operating`

2	TX_RST	W	0h	Writing '1' resets the transmitter Reset Source: mod_g_arstn
1	RX_RST	W	0h	Writing '1' resets the receiver Reset Source: mod_g_arstn
0	A_MULTIDROP	W	0h	In multi-drop mode, when written with the value '1' causes the next byte written into THR to be transmitted with the parity bit set, signaling an address Reset Source: mod_g_arstn

14.9.1.5.2.59 UART_TIMEGUARD Register

1 UART_TIMEGUARD Register (Offset = 94h) [reset = 0h]

Timeguard

Return to Summary Table

Table 14-18138. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0094h**
MCU_UART1	**04A1 0094h**
UART0	**0280 0094h**
UART1	**0281 0094h**
UART2	**0282 0094h**
UART3	**0283 0094h**
UART4	**0284 0094h**
UART5	**0285 0094h**
UART6	**0286 0094h**

Figure 14-5990. UART_TIMEGUARD Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEGUARD							
R/W							
0h							

Table 14-18140. UART_TIMEGUARD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEGUARD	R/W	0h	Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when comunicating with slower devices Reset Source: mod_g_arstn

14.9.1.5.2.60 UART_TIMEOUTL Register

1 UART_TIMEOUTL Register (Offset = 98h) [reset = 0h]

Timeout lower byte

Return to Summary Table

Table 14-18141. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 0098h**
MCU_UART1	**04A1 0098h**
UART0	**0280 0098h**
UART1	**0281 0098h**
UART2	**0282 0098h**
UART3	**0283 0098h**
UART4	**0284 0098h**
UART5	**0285 0098h**
UART6	**0286 0098h**

Figure 14-5991. UART_TIMEOUTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_L							
R/W							
0h							

Table 14-18143. UART_TIMEOUTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEOUT_L	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Lower byte of the 16 bit value] Reset Source: mod_g_arstn

14.9.1.5.2.61 UART_TIMEOUTH Register

1 UART_TIMEOUTH Register (Offset = 9Ch) [reset = 0h]

Timeout higher byte

Return to Summary Table

Table 14-18144. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 009Ch**
MCU_UART1	**04A1 009Ch**
UART0	**0280 009Ch**
UART1	**0281 009Ch**
UART2	**0282 009Ch**
UART3	**0283 009Ch**
UART4	**0284 009Ch**
UART5	**0285 009Ch**
UART6	**0286 009Ch**

Figure 14-5992. UART_TIMEOUTH Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_H							
R/W							
0h							

Table 14-18146. UART_TIMEOUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEOUT_H	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Higher byte of the 16 bit value] Reset Source: mod_g_arstn

14.9.1.5.2.62 UART_SCCR Register

1 UART_SCCR Register (Offset = A0h) [reset = 7h]

Smartcard (ISO7816) mode Control Register

Return to Summary Table

Table 14-18147. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00A0h**
MCU_UART1	**04A1 00A0h**
UART0	**0280 00A0h**
UART1	**0281 00A0h**
UART2	**0282 00A0h**
UART3	**0283 00A0h**
UART4	**0284 00A0h**
UART5	**0285 00A0h**
UART6	**0286 00A0h**

Figure 14-5993. UART_SCCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>DSNACK</td><td>INACK</td><td colspan="3">RESERVED</td><td colspan="3">MAX_ITERATION</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="3">R</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="3">0h</td><td colspan="3">7h</td></tr>
</table>

Table 14-18149. UART_SCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	DSNACK	R/W	0h	Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error. The data will be loaded into the receiver FIFO and PE will be set when Reading it. Reset Source: mod_g_arstn
6	INACK	R/W	0h	Inhibit NACK when receiving, even if an error is received. The data will be loaded into the receiver FIFO and PE will be set when Reading it. Reset Source: mod_g_arstn
5:3	RESERVED	R	0h	

Table 14-18149. UART_SCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	MAX_ITERATION	R/W	7h	Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the USART transmitter will set parity error, stop and not continue until it is cleared. Reset Source: mod_g_arstn

14.9.1.5.2.63 UART_ERHR Register

1 UART_ERHR Register (Offset = A4h) [reset = 0h]

Extended Receive Holding Register

Return to Summary Table

Table 14-18150. Instance Table

Instance Name	Physical Address
MCU_UART0	04A0 00A4h
MCU_UART1	04A1 00A4h
UART0	0280 00A4h
UART1	0281 00A4h
UART2	0282 00A4h
UART3	0283 00A4h
UART4	0284 00A4h
UART5	0285 00A4h
UART6	0286 00A4h

Figure 14-5994. UART_ERHR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>ERHR</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ERHR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18152. UART_ERHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R	0h	
8:0	ERHR	R	0h	Extended Receive Holding Register - allows accessing the full 9bit RHR Reset Source: mod_g_arstn

14.9.1.5.2.64 UART_ETHR Register

1 UART_ETHR Register (Offset = A4h) [reset = 0h]

Extended Transmit Holding Register

Return to Summary Table

Table 14-18153. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00A4h**
MCU_UART1	**04A1 00A4h**
UART0	**0280 00A4h**
UART1	**0281 00A4h**
UART2	**0282 00A4h**
UART3	**0283 00A4h**
UART4	**0284 00A4h**
UART5	**0285 00A4h**
UART6	**0286 00A4h**

Figure 14-5995. UART_ETHR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>ETHR</td></tr>
<tr><td colspan="7">R</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ETHR</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18155. UART_ETHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R	0h	
8:0	ETHR	W	0h	Extended Transmit Holding Register - allows Writing the full 9bit RHR Reset Source: mod_g_arstn

14.9.1.5.2.65 UART_MAR Register

1 UART_MAR Register (Offset = A8h) [reset = 0h]

Multidrop Address Register

Return to Summary Table

Table 14-18156. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00A8h**
MCU_UART1	**04A1 00A8h**
UART0	**0280 00A8h**
UART1	**0281 00A8h**
UART2	**0282 00A8h**
UART3	**0283 00A8h**
UART4	**0284 00A8h**
UART5	**0285 00A8h**
UART6	**0286 00A8h**

Figure 14-5996. UART_MAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-18158. UART_MAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ADDRESS	R/W	0h	Multidrop match address value Reset Source: mod_g_arstn

14.9.1.5.2.66 UART_MMR Register

1 UART_MMR Register (Offset = ACh) [reset = 0h]

Multidrop Mask Register

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Table 14-18159. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00ACh**
MCU_UART1	**04A1 00ACh**
UART0	**0280 00ACh**
UART1	**0281 00ACh**
UART2	**0282 00ACh**
UART3	**0283 00ACh**
UART4	**0284 00ACh**
UART5	**0285 00ACh**
UART6	**0286 00ACh**

Figure 14-5997. UART_MMR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 14-18161. UART_MMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MASK	R/W	0h	Address match masking value ? Writing a 0 to a bit means that the corresponding address bit will be ignored in matching Reset Source: mod_g_arstn

14.9.1.5.2.67 UART_MBR Register

1 UART_MBR Register (Offset = B0h) [reset = 0h]

Multidrop Broadcast Address Register

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Table 14-18162. Instance Table

Instance Name	Physical Address
MCU_UART0	**04A0 00B0h**
MCU_UART1	**04A1 00B0h**
UART0	**0280 00B0h**
UART1	**0281 00B0h**
UART2	**0282 00B0h**
UART3	**0283 00B0h**
UART4	**0284 00B0h**
UART5	**0285 00B0h**
UART6	**0286 00B0h**

Figure 14-5998. UART_MBR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BROADCAST_ADDRESS							
R/W							
0h							

Table 14-18164. UART_MBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BROADCAST_ADDRESS	R/W	0h	Broadcast address for address matching Reset Source: mod_g_arstn

14.9.2 High-speed Serial Interfaces Registers

14.9.2.1 CPSW Registers

14.9.2.1.1 CPSW Summary Table

Table 14-18165. CPSW0_cpsw3_ecc Registers, Base Address=0070 4000h, Length=1024

Offset	Length	Register Name	CPSW Physical Address
0h	32	CPSW3_ECC_ECC_REV	0070 4000h
8h	32	CPSW3_ECC_ECC_VECTOR	0070 4008h
Ch	32	CPSW3_ECC_ECC_STAT	0070 400Ch
10h + formula	32	CPSW3_ECC_ECC_RESERVED_SVBUS_j	0070 4010h
3Ch	32	CPSW3_ECC_ECC_SEC_EOI_REG	0070 403Ch
40h	32	CPSW3_ECC_ECC_SEC_STATUS_REG0	0070 4040h
80h	32	CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0	0070 4080h
C0h	32	CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0	0070 40C0h
13Ch	32	CPSW3_ECC_ECC_DED_EOI_REG	0070 413Ch
140h	32	CPSW3_ECC_ECC_DED_STATUS_REG0	0070 4140h
180h	32	CPSW3_ECC_ECC_DED_ENABLE_SET_REG0	0070 4180h
1C0h	32	CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0	0070 41C0h
200h	32	CPSW3_ECC_ECC_AGGR_ENABLE_SET	0070 4200h
204h	32	CPSW3_ECC_ECC_AGGR_ENABLE_CLR	0070 4204h
208h	32	CPSW3_ECC_ECC_AGGR_STATUS_SET	0070 4208h
20Ch	32	CPSW3_ECC_ECC_AGGR_STATUS_CLR	0070 420Ch

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152

Offset	Length	Register Name	CPSW Physical Address
0h	32	CPSW3_CPSW_NUSS_IDVER_REG	0800 0000h
4h	32	CPSW3_SYNCE_COUNT_REG	0800 0004h
8h	32	CPSW3_SYNCE_MUX_REG	0800 0008h
Ch	32	CPSW3_CONTROL_REG	0800 000Ch
10h	32	CPSW3_SGMII_NON_FIBER_MODE_REG	0800 0010h
14h	32	CPSW3_SERDES_RESET_ISO_REG	0800 0014h
1Ch	32	CPSW3_SUBSSYSTEM_STATUS_REG	0800 001Ch
20h	32	CPSW3_SUBSYSTEM_CONFIG_REG	0800 0020h
30h	32	CPSW3_RGMII1_STATUS_REG	0800 0030h
34h	32	CPSW3_RGMII2_STATUS_REG	0800 0034h
100h + formula	32	CPSW3_CPSGMII_SGMII_IDVER_REG_j	0800 0100h
104h + formula	32	CPSW3_CPSGMII_SOFT_RESET_REG_j	0800 0104h
110h + formula	32	CPSW3_CPSGMII_CONTROL_REG_j	0800 0110h
114h + formula	32	CPSW3_CPSGMII_STATUS_REG_j	0800 0114h
118h + formula	32	CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j	0800 0118h
11Ch + formula	32	CPSW3_CPSGMII_MR_NP_TX_REG_j	0800 011Ch
120h + formula	32	CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j	0800 0120h
124h + formula	32	CPSW3_CPSGMII_MR_LP_NP_RX_REG_j	0800 0124h
140h + formula	32	CPSW3_CPSGMII_DIAG_CLEAR_REG_j	0800 0140h
144h + formula	32	CPSW3_CPSGMII_DIAG_CONTROL_REG_j	0800 0144h
148h + formula	32	CPSW3_CPSGMII_DIAG_STATUS_REG_j	0800 0148h
F00h	32	CPSW3_MDIO_MDIO_VERSION_REG	0800 0F00h
F04h	32	CPSW3_MDIO_CONTROL_REG	0800 0F04h
F08h	32	CPSW3_MDIO_ALIVE_REG	0800 0F08h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
F0Ch	32	CPSW3_MDIO_LINK_REG	0800 0F0Ch
F10h	32	CPSW3_MDIO_LINK_INT_RAW_REG	0800 0F10h
F14h	32	CPSW3_MDIO_LINK_INT_MASKED_REG	0800 0F14h
F18h	32	CPSW3_MDIO_LINK_INT_MASK_SET_REG	0800 0F18h
F1Ch	32	CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG	0800 0F1Ch
F20h	32	CPSW3_MDIO_USER_INT_RAW_REG	0800 0F20h
F24h	32	CPSW3_MDIO_USER_INT_MASKED_REG	0800 0F24h
F28h	32	CPSW3_MDIO_USER_INT_MASK_SET_REG	0800 0F28h
F2Ch	32	CPSW3_MDIO_USER_INT_MASK_CLEAR_REG	0800 0F2Ch
F30h	32	CPSW3_MDIO_MANUAL_IF_REG	0800 0F30h
F34h	32	CPSW3_MDIO_POLL_REG	0800 0F34h
F38h	32	CPSW3_MDIO_POLL_EN_REG	0800 0F38h
F3Ch	32	CPSW3_MDIO_CLAUS45_REG	0800 0F3Ch
F40h	32	CPSW3_MDIO_USER_ADDR0_REG	0800 0F40h
F44h	32	CPSW3_MDIO_USER_ADDR1_REG	0800 0F44h
F80h + formula	32	CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j	0800 0F80h
F84h + formula	32	CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j	0800 0F84h
1000h	32	CPSW3_INTD_REVISION	0800 1000h
1010h	32	CPSW3_INTD_EOI_REG	0800 1010h
1014h	32	CPSW3_INTD_INTR_VECTOR_REG	0800 1014h
1100h	32	CPSW3_INTD_ENABLE_REG_OUT_PULSE_0	0800 1100h
1300h	32	CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0	0800 1300h
1500h	32	CPSW3_INTD_STATUS_REG_OUT_PULSE_0	0800 1500h
1A80h	32	CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE	0800 1A80h
20000h	32	CPSW3_CPSW_NU_CPSW_ID_VER_REG	0802 0000h
20004h	32	CPSW3_CPSW_NU_CONTROL_REG	0802 0004h
20010h	32	CPSW3_CPSW_NU_EM_CONTROL_REG	0802 0010h
20014h	32	CPSW3_CPSW_NU_STAT_PORT_EN_REG	0802 0014h
20018h	32	CPSW3_CPSW_NU_PTYPE_REG	0802 0018h
2001Ch	32	CPSW3_CPSW_NU_SOFT_IDLE_REG	0802 001Ch
20020h	32	CPSW3_CPSW_NU_THRU_RATE_REG	0802 0020h
20024h	32	CPSW3_CPSW_NU_GAP_THRESH_REG	0802 0024h
2002Ch	32	CPSW3_CPSW_NU_EEE_PRESCALE_REG	0802 002Ch
20030h	32	CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG	0802 0030h
20034h	32	CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG	0802 0034h
20038h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG	0802 0038h
2003Ch	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG	0802 003Ch
20040h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG	0802 0040h
20044h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG	0802 0044h
20050h	32	CPSW3_CPSW_NU_VLAN_LTYPE_REG	0802 0050h
20054h	32	CPSW3_CPSW_NU_EST_TS_DOMAIN_REG	0802 0054h
20058h	32	CPSW3_CPSW_NU_CUT_THRESHOLD_REG	0802 0058h
2005Ch	32	CPSW3_CPSW_NU_FREQUENCY_REG	0802 005Ch
20060h	32	CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG	0802 0060h
20100h	32	CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG	0802 0100h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
20104h	32	CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG	0802 0104h
20108h	32	CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG	0802 0108h
2010Ch	32	CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG	0802 010Ch
20110h	32	CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG	0802 0110h
20114h	32	CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG	0802 0114h
20118h	32	CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG	0802 0118h
2011Ch	32	CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG	0802 011Ch
21004h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG	0802 1004h
21008h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG	0802 1008h
21010h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG	0802 1010h
21014h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG	0802 1014h
21018h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG	0802 1018h
2101Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG	0802 101Ch
21020h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG	0802 1020h
21024h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG	0802 1024h
21028h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG	0802 1028h
21030h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG	0802 1030h
21034h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG	0802 1034h
21038h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG	0802 1038h
21050h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG	0802 1050h
21120h + formula	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j	0802 1120h
21140h + formula	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j	0802 1140h
21160h + formula	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j	0802 1160h
21180h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG	0802 1180h
21184h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG	0802 1184h
21188h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG	0802 1188h
2118Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG	0802 118Ch
21190h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG	0802 1190h
21194h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG	0802 1194h
21198h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG	0802 1198h
2119Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG	0802 119Ch
21300h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG	0802 1300h
21304h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG	0802 1304h
21320h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG	0802 1320h
22000h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG	0802 2000h
22004h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG	0802 2004h
22008h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG	0802 2008h
22010h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG	0802 2010h
22014h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG	0802 2014h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
22018h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG	0802 2018h
2201Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG	0802 201Ch
22020h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG	0802 2020h
22024h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG	0802 2024h
22028h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG	0802 2028h
22030h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG	0802 2030h
22034h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG	0802 2034h
22038h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG	0802 2038h
22040h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG	0802 2040h
22044h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG	0802 2044h
22048h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG	0802 2048h
22050h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG	0802 2050h
22060h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG	0802 2060h
22120h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j	0802 2120h
22140h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j	0802 2140h
22160h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j	0802 2160h
22180h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG	0802 2180h
22184h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG	0802 2184h
22188h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG	0802 2188h
2218Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG	0802 218Ch
22190h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG	0802 2190h
22194h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG	0802 2194h
22198h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG	0802 2198h
2219Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG	0802 219Ch
22300h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG	0802 2300h
22304h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG	0802 2304h
22308h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG	0802 2308h
2230Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG	0802 230Ch
22310h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG	0802 2310h
22314h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG	0802 2314h
22318h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG	0802 2318h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
2231Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG	0802 231Ch
22320h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG	0802 2320h
22330h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG	0802 2330h
22334h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG	0802 2334h
22338h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG	0802 2338h
2233Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG	0802 233Ch
22340h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG	0802 2340h
22350h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j	0802 2350h
22370h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG	0802 2370h
22380h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j	0802 2380h
223A0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG	0802 23A0h
223A4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG	0802 23A4h
223A8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG	0802 23A8h
223ACh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG	0802 23ACh
223B0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG	0802 23B0h
223B4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG	0802 23B4h
223B8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG	0802 23B8h
223BCh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG	0802 23BCh
223C0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG	0802 23C0h
223C4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG	0802 23C4h
23000h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG	0802 3000h
23004h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG	0802 3004h
23008h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG	0802 3008h
23010h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG	0802 3010h
23014h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG	0802 3014h
23018h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG	0802 3018h
2301Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG	0802 301Ch
23020h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG	0802 3020h
23024h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG	0802 3024h
23028h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG	0802 3028h
23030h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG	0802 3030h
23034h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG	0802 3034h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
23038h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG	0802 3038h
23040h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG	0802 3040h
23044h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG	0802 3044h
23048h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG	0802 3048h
23050h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG	0802 3050h
23060h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG	0802 3060h
23120h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j	0802 3120h
23140h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j	0802 3140h
23160h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j	0802 3160h
23180h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG	0802 3180h
23184h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG	0802 3184h
23188h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG	0802 3188h
2318Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG	0802 318Ch
23190h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG	0802 3190h
23194h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG	0802 3194h
23198h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG	0802 3198h
2319Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG	0802 319Ch
23300h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG	0802 3300h
23304h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG	0802 3304h
23308h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG	0802 3308h
2330Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG	0802 330Ch
23310h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG	0802 3310h
23314h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG	0802 3314h
23318h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG	0802 3318h
2331Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG	0802 331Ch
23320h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG	0802 3320h
23330h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG	0802 3330h
23334h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG	0802 3334h
23338h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG	0802 3338h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
2333Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG	0802 333Ch
23340h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG	0802 3340h
23350h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j	0802 3350h
23370h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG	0802 3370h
23380h + formula	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j	0802 3380h
233A0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG	0802 33A0h
233A4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG	0802 33A4h
233A8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG	0802 33A8h
233ACh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG	0802 33ACh
233B0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG	0802 33B0h
233B4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG	0802 33B4h
233B8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG	0802 33B8h
233BCh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG	0802 33BCh
233C0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG	0802 33C0h
233C4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG	0802 33C4h
32000h + formula	32	CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j	0803 2000h
3A000h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j	0803 A000h
3A004h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j	0803 A004h
3A008h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j	0803 A008h
3A00Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j	0803 A00Ch
3A010h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j	0803 A010h
3A014h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j	0803 A014h
3A018h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j	0803 A018h
3A01Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j	0803 A01Ch
3A020h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j	0803 A020h
3A024h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j	0803 A024h
3A028h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j	0803 A028h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3A02Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j	0803 A02Ch
3A030h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j	0803 A030h
3A034h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j	0803 A034h
3A038h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j	0803 A038h
3A03Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j	0803 A03Ch
3A040h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j	0803 A040h
3A044h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j	0803 A044h
3A048h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j	0803 A048h
3A04Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j	0803 A04Ch
3A050h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j	0803 A050h
3A054h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j	0803 A054h
3A058h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j	0803 A058h
3A05Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j	0803 A05Ch
3A060h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j	0803 A060h
3A064h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j	0803 A064h
3A068h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j	0803 A068h
3A06Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j	0803 A06Ch
3A070h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j	0803 A070h
3A074h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j	0803 A074h
3A078h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j	0803 A078h
3A07Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j	0803 A07Ch
3A080h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j	0803 A080h
3A084h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j	0803 A084h
3A088h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j	0803 A088h
3A08Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j	0803 A08Ch
3A090h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j	0803 A090h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3A094h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j	0803 A094h
3A098h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j	0803 A098h
3A09Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j	0803 A09Ch
3A0A0h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j	0803 A0A0h
3A0A4h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j	0803 A0A4h
3A0A8h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j	0803 A0A8h
3A0ACh + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j	0803 A0ACh
3A0B0h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j	0803 A0B0h
3A0B4h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j	0803 A0B4h
3A0B8h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j	0803 A0B8h
3A0BCh + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j	0803 A0BCh
3A0C0h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j	0803 A0C0h
3A0C4h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j	0803 A0C4h
3A0C8h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j	0803 A0C8h
3A0CCh + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j	0803 A0CCh
3A0D0h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j	0803 A0D0h
3A0D4h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j	0803 A0D4h
3A0D8h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j	0803 A0D8h
3A0DCh + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j	0803 A0DCh
3A140h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j	0803 A140h
3A144h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j	0803 A144h
3A148h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j	0803 A148h
3A14Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j	0803 A14Ch
3A150h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j	0803 A150h
3A154h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j	0803 A154h
3A17Ch + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j	0803 A17Ch

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3A180h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k	0803 A180h
3A1A0h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k	0803 A1A0h
3A1C0h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k	0803 A1C0h
3A1E0h + formula	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k	0803 A1E0h
3D000h	32	CPSW3_CPSW_NU_CPTS_IDVER_REG	0803 D000h
3D004h	32	CPSW3_CPSW_NU_CPTS_CONTROL_REG	0803 D004h
3D008h	32	CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG	0803 D008h
3D00Ch	32	CPSW3_CPSW_NU_CPTS_TS_PUSH_REG	0803 D00Ch
3D010h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG	0803 D010h
3D014h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG	0803 D014h
3D018h	32	CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG	0803 D018h
3D01Ch	32	CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG	0803 D01Ch
3D020h	32	CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG	0803 D020h
3D024h	32	CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG	0803 D024h
3D028h	32	CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG	0803 D028h
3D02Ch	32	CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG	0803 D02Ch
3D030h	32	CPSW3_CPSW_NU_CPTS_EVENT_POP_REG	0803 D030h
3D034h	32	CPSW3_CPSW_NU_CPTS_EVENT_0_REG	0803 D034h
3D038h	32	CPSW3_CPSW_NU_CPTS_EVENT_1_REG	0803 D038h
3D03Ch	32	CPSW3_CPSW_NU_CPTS_EVENT_2_REG	0803 D03Ch
3D040h	32	CPSW3_CPSW_NU_CPTS_EVENT_3_REG	0803 D040h
3D044h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG	0803 D044h
3D048h	32	CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG	0803 D048h
3D04Ch	32	CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG	0803 D04Ch
3D050h	32	CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG	0803 D050h
3D054h	32	CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG	0803 D054h
3D058h	32	CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG	0803 D058h
3D0D0h	32	CPSW3_CPSW_NU_CPTS_TS_CONFIG	0803 D0D0h
3D0E0h + formula	32	CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j	0803 D0E0h
3D0E4h + formula	32	CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j	0803 D0E4h
3D0E8h + formula	32	CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j	0803 D0E8h
3D0ECh + formula	32	CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j	0803 D0ECh
3D0F0h + formula	32	CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j	0803 D0F0h
3D0F4h + formula	32	CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j	0803 D0F4h
3D0F8h + formula	32	CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j	0803 D0F8h
3D200h + formula	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j	0803 D200h

Table 14-18166. CPSW0_cpsw3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3D204h + formula	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j	0803 D204h
3D208h + formula	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j	0803 D208h
3D20Ch + formula	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j	0803 D20Ch
3D210h + formula	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j	0803 D210h
3D214h + formula	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j	0803 D214h
3D218h + formula	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j	0803 D218h
3E000h	32	CPSW3_CPSW_NU_ALE_MOD_VER	0803 E000h
3E004h	32	CPSW3_CPSW_NU_ALE_ALE_STATUS	0803 E004h
3E008h	32	CPSW3_CPSW_NU_ALE_ALE_CONTROL	0803 E008h
3E00Ch	32	CPSW3_CPSW_NU_ALE_ALE_CTRL2	0803 E00Ch
3E010h	32	CPSW3_CPSW_NU_ALE_ALE_PRESCALE	0803 E010h
3E014h	32	CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL	0803 E014h
3E01Ch	32	CPSW3_CPSW_NU_ALE_ALE_NXT_HDR	0803 E01Ch
3E020h	32	CPSW3_CPSW_NU_ALE_ALE_TBLCTL	0803 E020h
3E034h	32	CPSW3_CPSW_NU_ALE_ALE_TBLW2	0803 E034h
3E038h	32	CPSW3_CPSW_NU_ALE_ALE_TBLW1	0803 E038h
3E03Ch	32	CPSW3_CPSW_NU_ALE_ALE_TBLW0	0803 E03Ch
3E040h + formula	32	CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j	0803 E040h
3E090h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER	0803 E090h
3E094h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST	0803 E094h
3E098h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST	0803 E098h
3E09Ch	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG	0803 E09Ch
3E0B8h	32	CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG	0803 E0B8h
3E0BCh	32	CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL	0803 E0BCh
3E0FCh	32	CPSW3_CPSW_NU_ALE_EGRESSOP	0803 E0FCh
3E100h	32	CPSW3_CPSW_NU_ALE_POLICECFG0	0803 E100h
3E104h	32	CPSW3_CPSW_NU_ALE_POLICECFG1	0803 E104h
3E108h	32	CPSW3_CPSW_NU_ALE_POLICECFG2	0803 E108h
3E10Ch	32	CPSW3_CPSW_NU_ALE_POLICECFG3	0803 E10Ch
3E110h	32	CPSW3_CPSW_NU_ALE_POLICECFG4	0803 E110h
3E118h	32	CPSW3_CPSW_NU_ALE_POLICECFG6	0803 E118h
3E11Ch	32	CPSW3_CPSW_NU_ALE_POLICECFG7	0803 E11Ch
3E120h	32	CPSW3_CPSW_NU_ALE_POLICETBLCTL	0803 E120h
3E124h	32	CPSW3_CPSW_NU_ALE_POLICECONTROL	0803 E124h
3E128h	32	CPSW3_CPSW_NU_ALE_POLICETESTCTL	0803 E128h
3E12Ch	32	CPSW3_CPSW_NU_ALE_POLICEHSTAT	0803 E12Ch
3E134h	32	CPSW3_CPSW_NU_ALE_THREADMAPDEF	0803 E134h
3E138h	32	CPSW3_CPSW_NU_ALE_THREADMAPCTL	0803 E138h
3E13Ch	32	CPSW3_CPSW_NU_ALE_THREADMAPVAL	0803 E13Ch

14.9.2.1.2 CPSW3_ECC_ECC_REV Register

CPSW3_ECC_ECC_REV Register (Offset = 0h) [reset = 66A02A01h]

Register Description: Revision parameters

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Table 14-18167. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4000h

Figure 14-5999. CPSW3_ECC_ECC_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-18169. CPSW3_ECC_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.2.1.3 CPSW3_ECC_ECC_VECTOR Register

CPSW3_ECC_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

Register Description: ECC Vector Register

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Table 14-18170. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4008h

Figure 14-6000. CPSW3_ECC_ECC_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18172. CPSW3_ECC_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.2.1.4 CPSW3_ECC_ECC_STAT Register

CPSW3_ECC_ECC_STAT Register (Offset = Ch) [reset = 14h]

Register Description: Misc Status

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Table 14-18173. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 400Ch

Figure 14-6001. CPSW3_ECC_ECC_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">14h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">14h</td></tr>
</table>

Table 14-18175. CPSW3_ECC_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	14h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.2.1.5 CPSW3_ECC_ECC_RESERVED_SVBUS_j Register

CPSW3_ECC_ECC_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Register Description: Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18176. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4010h + formula

Figure 14-6002. CPSW3_ECC_ECC_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-18178. CPSW3_ECC_ECC_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.2.1.6 CPSW3_ECC_ECC_SEC_EOI_REG Register

CPSW3_ECC_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

Register Description: EOI Register

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Table 14-18179. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 403Ch

Figure 14-6003. CPSW3_ECC_ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-18181. CPSW3_ECC_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.2.1.7 CPSW3_ECC_ECC_SEC_STATUS_REG0 Register

CPSW3_ECC_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Register Description: Interrupt Status Register 0

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Table 14-18182. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4040h

Figure 14-6004. CPSW3_ECC_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18184. CPSW3_ECC_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend

Table 14-18184. CPSW3_ECC_ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.9.2.1.8 CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register

CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Register Description: Interrupt Enable Set Register 0

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Table 14-18185. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4080h

Figure 14-6005. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18187. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend

Table 14-18187. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.9.2.1.9 CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register

CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Register Description: Interrupt Enable Clear Register 0

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Table 14-18188. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 40C0h

Figure 14-6006. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

15	14	13	12	11	10	9	8
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18190. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend

Table 14-18190. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.9.2.1.10 CPSW3_ECC_ECC_DED_EOI_REG Register

CPSW3_ECC_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

Register Description: EOI Register

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Table 14-18191. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 413Ch

Figure 14-6007. CPSW3_ECC_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-18193. CPSW3_ECC_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.2.1.11 CPSW3_ECC_ECC_DED_STATUS_REG0 Register

CPSW3_ECC_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Register Description: Interrupt Status Register 0

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Table 14-18194. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4140h

Figure 14-6008. CPSW3_ECC_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18196. CPSW3_ECC_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend

Table 14-18196. CPSW3_ECC_ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.9.2.1.12 CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register

CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Register Description: Interrupt Enable Set Register 0

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Table 14-18197. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4180h

Figure 14-6009. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18199. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend

Table 14-18199. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.9.2.1.13 CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register

CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Register Description: Interrupt Enable Clear Register 0

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Table 14-18200. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 41C0h

Figure 14-6010. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18202. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend

Table 14-18202. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.9.2.1.14 CPSW3_ECC_ECC_AGGR_ENABLE_SET Register

CPSW3_ECC_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

Register Description: AGGR interrupt enable set Register

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Table 14-18203. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4200h

Figure 14-6011. CPSW3_ECC_ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-18205. CPSW3_ECC_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.2.1.15 CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register

CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

Register Description: AGGR interrupt enable clear Register

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Table 14-18206. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4204h

Figure 14-6012. CPSW3_ECC_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-18208. CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.2.1.16 CPSW3_ECC_ECC_AGGR_STATUS_SET Register

CPSW3_ECC_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

Register Description: AGGR interrupt status set Register

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Table 14-18209. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 4208h

Figure 14-6013. CPSW3_ECC_ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-18211. CPSW3_ECC_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.2.1.17 CPSW3_ECC_ECC_AGGR_STATUS_CLR Register

CPSW3_ECC_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

Register Description: AGGR interrupt status clear Register

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Table 14-18212. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3_ecc	0070 420Ch

Figure 14-6014. CPSW3_ECC_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-18214. CPSW3_ECC_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.2.1.18 CPSW3_CPSW_NUSS_IDVER_REG Register

CPSW3_CPSW_NUSS_IDVER_REG Register (Offset = 0h) [reset = 6BA00103h]

Register Description: ID Version Register

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Table 14-18215. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0000h

Figure 14-6015. CPSW3_CPSW_NUSS_IDVER_REG Name Register

31	30	29	28	27	26	25	24
IDENT							
R							
6BA0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IDENT							
R							
6BA0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VER					MAJOR_VER		
R					R		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MINOR_VER							
R							
3h							

Table 14-18217. CPSW3_CPSW_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6BA0h	Identification value
15:11	RTL_VER	R	0h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	3h	Minor version value

14.9.2.1.19 CPSW3_SYNCE_COUNT_REG Register

CPSW3_SYNCE_COUNT_REG Register (Offset = 4h) [reset = 0h]

Register Description: SyncE Count Register

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Table 14-18218. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0004h

Figure 14-6016. CPSW3_SYNCE_COUNT_REG Name Register

31	30	29	28	27	26	25	24
SYNCE_CNT							
R/W							
0h							
23	22	21	20	19	18	17	16
SYNCE_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
SYNCE_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNCE_CNT							
R/W							
0h							

Table 14-18220. CPSW3_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNCE_CNT	R/W	0h	Sync E Count Value

14.9.2.1.20 CPSW3_SYNCE_MUX_REG Register

CPSW3_SYNCE_MUX_REG Register (Offset = 8h) [reset = 0h]

Register Description: SyncE Mux Register

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Table 14-18221. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0008h

Figure 14-6017. CPSW3_SYNCE_MUX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		SYNCE_SEL		SYNCE_PORT_SEL			
NONE		R/W		R/W			
0h		0h		0h			

Table 14-18223. CPSW3_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

5:4	SYNCE_SEL	R/W	0h	Sync E Interface Select.
				`0h GMIIn_MRCLK_I input clock from selected port.`
				`1h RMII_MHZ_50_CLK (same for all ports).`
				`2h RGMIIn_RXC_I input clock from selected port.`
				`3h SERDESn_RXCLK from selected port.`

3:0	SYNCE_PORT_SEL	R/W	0h	Sync E Port Select
				This field selects the port that will be used for Synchronous Ethernet receive clock. The port interface is selected with synce_sel.
				`0h Port 1.`
				`1h Port 2.`
				`2h-Fh Reserved.`

14.9.2.1.21 CPSW3_CONTROL_REG Register

CPSW3_CONTROL_REG Register (Offset = Ch) [reset = 0h]

Register Description: Control Register

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Table 14-18224. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 000Ch

Figure 14-6018. CPSW3_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>EEE_PHY_ONLY</td><td>EEE_EN</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-18226. CPSW3_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EEE_PHY_ONLY	R/W	0h	Energy Efficient Enable Phy Only Mode: 0h The low power indicate state includes gating off the CPPI_GCLK to the CPSW. 1h The low power indicate state does not gate the clock to the CPSW.
0	EEE_EN	R/W	0h	Energy Efficient Ethernet Enable: 0h EEE is disabled 1h EEE is enabled

14.9.2.1.22 CPSW3_SGMII_NON_FIBER_MODE_REG Register

CPSW3_SGMII_NON_FIBER_MODE_REG Register (Offset = 10h) [reset = 3h]

Register Description: SGMII NON FIBER Mode Register

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Table 14-18227. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0010h

Figure 14-6019. CPSW3_SGMII_NON_FIBER_MODE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SGMII_NON_FIBER_MODE	
NONE						R/W	
0h						3h	

Table 14-18229. CPSW3_SGMII_NON_FIBER_MODE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SGMII_NON_FIBER_MODE	R/W	3h	This register bit goes to the CPSGMII mode input only

14.9.2.1.23 CPSW3_SERDES_RESET_ISO_REG Register

CPSW3_SERDES_RESET_ISO_REG Register (Offset = 14h) [reset = 0h]

Register Description: SyncE Mux Register

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Table 14-18230. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0014h

Figure 14-6020. CPSW3_SERDES_RESET_ISO_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SERDES_RESET_ISO	
NONE						R/W	
0h						0h	

Table 14-18232. CPSW3_SERDES_RESET_ISO_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	SERDES_RESET_ISO	R/W	0h	These bits control whether the SERDES ignores the hard reset for isolation or not

14.9.2.1.24 CPSW3_SUBSSYSTEM_STATUS_REG Register

CPSW3_SUBSSYSTEM_STATUS_REG Register (Offset = 1Ch) [reset = 0h]

Register Description: Subsystem Status Register

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Table 14-18233. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 001Ch

Figure 14-6021. CPSW3_SUBSSYSTEM_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EEE_CLKSTOP_ACK
NONE							R
0h							0h

Table 14-18235. CPSW3_SUBSSYSTEM_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EEE_CLKSTOP_ACK	R	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

14.9.2.1.25 CPSW3_SUBSYSTEM_CONFIG_REG Register

CPSW3_SUBSYSTEM_CONFIG_REG Register (Offset = 20h) [reset = 70203h]

Register Description: Subsystem Configuration Register

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Table 14-18236. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0020h

Figure 14-6022. CPSW3_SUBSYSTEM_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED				XGMII			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
XGMII				QSGMII	SGMII	RGMII	RMII
R				R	R	R	R
0h				0h	1h	1h	1h
15	14	13	12	11	10	9	8
RESERVED			NUM_GENF				
NONE			R				
0h			2h				
7	6	5	4	3	2	1	0
NUM_PORTS							
R							
3h							

Table 14-18238. CPSW3_SUBSYSTEM_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:20	XGMII	R	0h	The Number of XGMII Ports included in the CPSW_NUSS
19	QSGMII	R	0h	QSGMII is included in the CPSW_NUSS
18	SGMII	R	1h	SGMII is included in the CPSW_NUSS
17	RGMII	R	1h	RGMII is included in the CPSW_NUSS
16	RMII	R	1h	RMII is included in the CPSW_NUSS
15:13	RESERVED	NONE	0h	Reserved
12:8	NUM_GENF	R	2h	The number of CPTS GENF outputs
7:0	NUM_PORTS	R	3h	The total number of ports including the host port 0

14.9.2.1.26 CPSW3_RGMII1_STATUS_REG Register

CPSW3_RGMII1_STATUS_REG Register (Offset = 30h) [reset = 0h]

Register Description: RGMII1 Status Register

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Table 14-18239. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0030h

Figure 14-6023. CPSW3_RGMII1_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
NONE				R	R		R
0h				0h	0h		0h

Table 14-18241. CPSW3_RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	FULLDUPLEX	R	0h	RGMII Port 1 full duplex: 0h `Half-duplex` 1h `Full-duplex`
2:1	SPEED	R	0h	RGMII Port 1 speed: 0h `10Mbps` 1h `100Mbps` 2h `1000Mbps` 3h `Reserved`
0	LINK	R	0h	RGMII Port 1 link indicator: 0h `Link is down,` 1h `Link is up`

14.9.2.1.27 CPSW3_RGMII2_STATUS_REG Register

CPSW3_RGMII2_STATUS_REG Register (Offset = 34h) [reset = 0h]

Register Description: RGMII2 Status Register

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Table 14-18242. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0034h

Figure 14-6024. CPSW3_RGMII2_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
NONE				R	R		R
0h				0h	0h		0h

Table 14-18244. CPSW3_RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	FULLDUPLEX	R	0h	RGMII Port 2 full dulex: 0h Half-duplex 1h Full-duplex
2:1	SPEED	R	0h	RGMII Port 2 speed: 0h 10Mbps 1h 100Mbps 2h 1000Mbps 3h Reserved
0	LINK	R	0h	RGMII Port 2 link indicator: 0h Link is down 1h Link is up

14.9.2.1.28 CPSW3_CPSGMII_SGMII_IDVER_REG_j Register

CPSW3_CPSGMII_SGMII_IDVER_REG_j Register (Offset = 100h + formula) [reset = 4EC21102h]

Register Description: SGMII IDVER register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18245. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0100h + formula

Figure 14-6025. CPSW3_CPSGMII_SGMII_IDVER_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4EC2h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TX_IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4EC2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_VER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">2h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MINOR_VER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-18247. CPSW3_CPSGMII_SGMII_IDVER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TX_IDENT	R	4EC2h	MODULE value
15:11	RTL_VER	R	2h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	2h	Minor version value

14.9.2.1.29 CPSW3_CPSGMII_SOFT_RESET_REG_j Register

CPSW3_CPSGMII_SOFT_RESET_REG_j Register (Offset = 104h + formula) [reset = 0h]

Register Description: SGMII Soft Reset Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18248. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0104h + formula

Figure 14-6026. CPSW3_CPSGMII_SOFT_RESET_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>RT_SOFT_RESET</td><td>SOFT_RESET</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-18250. CPSW3_CPSGMII_SOFT_RESET_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	RT_SOFT_RESET	R/W	0h	Transmit and receive software reset
0	SOFT_RESET	R/W	0h	Software reset

14.9.2.1.30 CPSW3_CPSGMII_CONTROL_REG_j Register

CPSW3_CPSGMII_CONTROL_REG_j Register (Offset = 110h + formula) [reset = 0h]

Register Description: SGMII Control Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18251. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0110h + formula

Figure 14-6027. CPSW3_CPSGMII_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TEST_PATTERN_EN	MASTER	LOOPBACK	MR_NP_LOADED	FAST_LINK_TIMER	MR_AN_RESTART	MR_AN_ENABLE
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18253. CPSW3_CPSGMII_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TEST_PATTERN_EN	R/W	0h	Test pattern enable
5	MASTER	R/W	0h	Master mode
4	LOOPBACK	R/W	0h	Loopback mode
3	MR_NP_LOADED	R/W	0h	Next page loaded
2	FAST_LINK_TIMER	R/W	0h	Fast link timer
1	MR_AN_RESTART	R/W	0h	Auto-negotiation restart
0	MR_AN_ENABLE	R/W	0h	Auto-negotiation enable

14.9.2.1.31 CPSW3_CPSGMII_STATUS_REG_j Register

CPSW3_CPSGMII_STATUS_REG_j Register (Offset = 114h + formula) [reset = 0h]

Register Description: SGMII Status Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18254. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0114h + formula

Figure 14-6028. CPSW3_CPSGMII_STATUS_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		FIB_SIG_DETECT	LOCK	MR_PAGE_RX	MR_AN_COMPLETE	AN_ERROR	LINK
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-18256. CPSW3_CPSGMII_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	FIB_SIG_DETECT	R	0h	Fiber signal detect
4	LOCK	R	0h	Lock
3	MR_PAGE_RX	R	0h	Next page received
2	MR_AN_COMPLETE	R	0h	Auto-negotiation complete
1	AN_ERROR	R	0h	Auto-negotiation error
0	LINK	R	0h	Link indicator

14.9.2.1.32 CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j Register

CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j Register (Offset = 118h + formula) [reset = 0h]

Register Description: SGMII MR Advertized Ability Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18257. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0118h + formula

Figure 14-6029. CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MR_ADV_ABILITY							
R/W							
0h							
7	6	5	4	3	2	1	0
MR_ADV_ABILITY							
R/W							
0h							

Table 14-18259. CPSW3_CPSGMII_MR_ADV_ABILITY_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MR_ADV_ABILITY	R/W	0h	Advertised ability

14.9.2.1.33 CPSW3_CPSGMII_MR_NP_TX_REG_j Register

CPSW3_CPSGMII_MR_NP_TX_REG_j Register (Offset = 11Ch + formula) [reset = 0h]

Register Description: SGMII Next Pate Transmit Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18260. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 011Ch + formula

Figure 14-6030. CPSW3_CPSGMII_MR_NP_TX_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MR_NP_TX							
R/W							
0h							
7	6	5	4	3	2	1	0
MR_NP_TX							
R/W							
0h							

Table 14-18262. CPSW3_CPSGMII_MR_NP_TX_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MR_NP_TX	R/W	0h	Next page transmit

14.9.2.1.34 CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j Register

CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j Register (Offset = 120h + formula) [reset = 0h]

Register Description: SGMII Link Partner Advertized Ability Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18263. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0120h + formula

Figure 14-6031. CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MR_LP_ADV_ABILITY							
R							
0h							
7	6	5	4	3	2	1	0
MR_LP_ADV_ABILITY							
R							
0h							

Table 14-18265. CPSW3_CPSGMII_MR_LP_ADV_ABILITY_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MR_LP_ADV_ABILITY	R	0h	Link partner advertised ability

14.9.2.1.35 CPSW3_CPSGMII_MR_LP_NP_RX_REG_j Register

CPSW3_CPSGMII_MR_LP_NP_RX_REG_j Register (Offset = 124h + formula) [reset = 0h]

Register Description: SGMII Link Partner Next Page Receive Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18266. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0124h + formula

Figure 14-6032. CPSW3_CPSGMII_MR_LP_NP_RX_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MR_LP_NP_RX							
R							
0h							
7	6	5	4	3	2	1	0
MR_LP_NP_RX							
R							
0h							

Table 14-18268. CPSW3_CPSGMII_MR_LP_NP_RX_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MR_LP_NP_RX	R	0h	Link Partner Next Page Received

14.9.2.1.36 CPSW3_CPSGMII_DIAG_CLEAR_REG_j Register

CPSW3_CPSGMII_DIAG_CLEAR_REG_j Register (Offset = 140h + formula) [reset = 0h]

Register Description: SGMII Diagnostics Clear Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18269. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0140h + formula

Figure 14-6033. CPSW3_CPSGMII_DIAG_CLEAR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DIAG_CLEAR
NONE							R/W
0h							0h

Table 14-18271. CPSW3_CPSGMII_DIAG_CLEAR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DIAG_CLEAR	R/W	0h	Diagnostics clear

14.9.2.1.37 CPSW3_CPSGMII_DIAG_CONTROL_REG_j Register

CPSW3_CPSGMII_DIAG_CONTROL_REG_j Register (Offset = 144h + formula) [reset = 0h]

Register Description: SGMII Diagnostics Control Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18272. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0144h + formula

Figure 14-6034. CPSW3_CPSGMII_DIAG_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DIAG_SM_SEL			RESERVED		DIAG_EDGE_SEL	
NONE	R/W			NONE		R/W	
0h	0h			0h		0h	

Table 14-18274. CPSW3_CPSGMII_DIAG_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:4	DIAG_SM_SEL	R/W	0h	Diagnostic select
3:2	RESERVED	NONE	0h	Reserved
1:0	DIAG_EDGE_SEL	R/W	0h	Diagnostics hold signals edge select

14.9.2.1.38 CPSW3_CPSGMII_DIAG_STATUS_REG_j Register

CPSW3_CPSGMII_DIAG_STATUS_REG_j Register (Offset = 148h + formula) [reset = 0h]

Register Description: SGMII Diagnostics Status Register

Formula = (j * 100h); where j = 0 to 1d

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Table 14-18275. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0148h + formula

Figure 14-6035. CPSW3_CPSGMII_DIAG_STATUS_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DIAG_STATUS							
R							
0h							
7	6	5	4	3	2	1	0
DIAG_STATUS							
R							
0h							

Table 14-18277. CPSW3_CPSGMII_DIAG_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	DIAG_STATUS	R	0h	Diagnostics status

14.9.2.1.39 CPSW3_MDIO_MDIO_VERSION_REG Register

CPSW3_MDIO_MDIO_VERSION_REG Register (Offset = F00h) [reset = 70907h]

Register Description: MDIO Version Register

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Table 14-18278. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F00h

Figure 14-6036. CPSW3_MDIO_MDIO_VERSION_REG Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
0h		0h		7h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
7h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
1h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		7h					

Table 14-18280. CPSW3_MDIO_MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	0h	Scheme
29:28	BU	R	0h	bu
27:16	MODULE_ID	R	7h	Module ID
15:11	REVRTL	R	1h	RTL version
10:8	REVMAJ	R	1h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	7h	Minor version

14.9.2.1.40 CPSW3_MDIO_CONTROL_REG Register

CPSW3_MDIO_CONTROL_REG Register (Offset = F04h) [reset = 810000FFh]

Register Description: MDIO Control Register

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Table 14-18281. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F04h

Figure 14-6037. CPSW3_MDIO_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R	R/W	NONE	R				
1h	0h	1h	1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
NONE			R/W	R/W	R/W	R/W	NONE
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKDIV							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKDIV							
R/W							
FFh							

Table 14-18283. CPSW3_MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1h when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1h to this bit enables the MDIO state machine, writing a 0h disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	NONE	1h	Reserved
28:24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest useraccess channel that is available in the module and is currently set to 1h. This implies that MDIOUserAccess1 is the highest available user access channel.
23:21	RESERVED	NONE	0h	Reserved
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1h to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.

Table 14-18283. CPSW3_MDIO_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	FAULT	R/W	0h	Fault indicator. This bit is set to 1h if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1h to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1h to enable the physical layer fault detection.
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1h to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	NONE	0h	Reserved
15:0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. When clkdiv is set to 0h, MDCLK is disabled and output is driven to a high logic state. MDCLK frequency = clk frequency/(clkdiv+1).

14.9.2.1.41 CPSW3_MDIO_ALIVE_REG Register

CPSW3_MDIO_ALIVE_REG Register (Offset = F08h) [reset = 0h]

Register Description: MDIO Alive Register

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Table 14-18284. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F08h

Figure 14-6038. CPSW3_MDIO_ALIVE_REG Name Register

31	30	29	28	27	26	25	24
ALIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
ALIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
ALIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
ALIVE							
R/W							
0h							

Table 14-18286. CPSW3_MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ALIVE	R/W	0h	MDIO Alive. Each of the 32-bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address. Writing a 1h to any bit will clear it, writing a 0h has no effect.

14.9.2.1.42 CPSW3_MDIO_LINK_REG Register

CPSW3_MDIO_LINK_REG Register (Offset = F0Ch) [reset = 0h]

Register Description: MDIO Link Register

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Table 14-18287. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F0Ch

Figure 14-6039. CPSW3_MDIO_LINK_REG Name Register

31	30	29	28	27	26	25	24
LINK							
R							
0h							
23	22	21	20	19	18	17	16
LINK							
R							
0h							
15	14	13	12	11	10	9	8
LINK							
R							
0h							
7	6	5	4	3	2	1	0
LINK							
R							
0h							

Table 14-18289. CPSW3_MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LINK	R	0h	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to 0h if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIOUserPhySel registers can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIOUserPhySel register. In State Change Mode the MLINK input pins are unused.

14.9.2.1.43 CPSW3_MDIO_LINK_INT_RAW_REG Register

CPSW3_MDIO_LINK_INT_RAW_REG Register (Offset = F10h) [reset = 0h]

Register Description: MDIO Link Interrupt Raw Register

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Table 14-18290. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F10h

Figure 14-6040. CPSW3_MDIO_LINK_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
NONE						R/W	
0h						0h	

Table 14-18292. CPSW3_MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTRAW	R/W	0h	MDIO link change event raw value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register. [0]LINKINTRAW and [1]LINKINTRAW correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set LINKINTRAW bits to a 1h which may be used for test purposes. MDIO link change event raw value. State Change Mode operation: The [0]LINKINTRAW bit will be asserted '1' when any bit (for any PHY) in the MDIOAlive or MDIOLink registers changes due to MDIO operations. The [1]LINKINTRAW bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the [0]LINKINTRAW bit to a 1h which may be used for test purposes.

14.9.2.1.44 CPSW3_MDIO_LINK_INT_MASKED_REG Register

CPSW3_MDIO_LINK_INT_MASKED_REG Register (Offset = F14h) [reset = 0h]

Register Description: MDIO Link Interrupt Masked Register

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Table 14-18293. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F14h

Figure 14-6041. CPSW3_MDIO_LINK_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						LINKINTMASKED	
NONE						R/W	
0h						0h	

Table 14-18295. CPSW3_MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTMASKED	R/W	0h	MDIO link change interrupt masked value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding CPSW_MDIO_USER_PHY_SEL_REG_k[6] LINKINT_ENABLE bit was set. CPSW_MDIO_LINK_INT_MASKED_REG[0] LINKINTMASKED and [1] LINKINTMASKED correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1h will clear the interrupt and writing 0h has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values. MDIO link change interrupt masked value. State Change Mode operation: The [0] LINKINTMASKED bit will be asserted '1' when CPSW_MDIO_LINK_INT_RAW_REG[0] LINKINTRAW is asserted '1' and when the CPSW_MDIO_LINK_INT_MASK_SET_REG[0] LINKINTMASKSET bit is set to 1h. Writing a 1h will clear [0] LINKINTMASKED (and the MDIO_LINKINT[0] output) and writing 0h has no effect. The [1] LINKINTMASKED bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode).

14.9.2.1.45 CPSW3_MDIO_LINK_INT_MASK_SET_REG Register

CPSW3_MDIO_LINK_INT_MASK_SET_REG Register (Offset = F18h) [reset = 0h]

Register Description: MDIO Link Interrupt Mask Set Register

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Table 14-18296. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F18h

Figure 14-6042. CPSW3_MDIO_LINK_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK SET
NONE							R/W
0h							0h

Table 14-18298. CPSW3_MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKSET	R/W	0h	MDIO link interrupt mask set. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask set. State Change Mode Operation: Writing this bit to 1h will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when [0] LINKINTRAW is asserted.

14.9.2.1.46 CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register

CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = F1Ch) [reset = 0h]

Register Description: MDIO Link Interrupt Mask Clear Register

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Table 14-18299. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F1Ch

Figure 14-6043. CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							LINKINTMASK CLR
NONE							R/W
0h							0h

Table 14-18301. CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKCLR	R/W	0h	MDIO link interrupt mask clear. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask clear. State Change Mode Operation: Writing this bit to 1h will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the [0] LINKINTRAW bit value.

14.9.2.1.47 CPSW3_MDIO_USER_INT_RAW_REG Register

CPSW3_MDIO_USER_INT_RAW_REG Register (Offset = F20h) [reset = 0h]

Register Description: MDIO User Interrupt Raw Register

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Table 14-18302. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F20h

Figure 14-6044. CPSW3_MDIO_USER_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
NONE						R/W	
0h						0h	

Table 14-18304. CPSW3_MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTRAW	R/W	0h	Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the userintraw bits to a 1h. This mode may be used for test purposes.

14.9.2.1.48 CPSW3_MDIO_USER_INT_MASKED_REG Register

CPSW3_MDIO_USER_INT_MASKED_REG Register (Offset = F24h) [reset = 0h]

Register Description: MDIO User Interrupt Masked Register

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Table 14-18305. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F24h

Figure 14-6045. CPSW3_MDIO_USER_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
NONE						R/W	
0h						0h	

Table 14-18307. CPSW3_MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKED	R/W	0h	Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1h. Writing a 1h will clear the interrupt and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED bits to a 1h. This mode may be used for test purposes.

14.9.2.1.49 CPSW3_MDIO_USER_INT_MASK_SET_REG Register

CPSW3_MDIO_USER_INT_MASK_SET_REG Register (Offset = F28h) [reset = 0h]

Register Description: MDIO User Interrupt Mask Set Register

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Table 14-18308. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F28h

Figure 14-6046. CPSW3_MDIO_USER_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKSET	
NONE						R/W	
0h						0h	

Table 14-18310. CPSW3_MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKSET	R/W	0h	MDIO user interrupt mask set for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0h. Writing a 0h to this register has no effect.

14.9.2.1.50 CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register

CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = F2Ch) [reset = 0h]

Register Description: MDIO User Interrupt Mask Clear Register

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Table 14-18311. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F2Ch

Figure 14-6047. CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
NONE						R/W	
0h						0h	

Table 14-18313. CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKCLR	R/W	0h	MDIO user command complete interrupt mask clear for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0h to this register has no effect.

14.9.2.1.51 CPSW3_MDIO_MANUAL_IF_REG Register

CPSW3_MDIO_MANUAL_IF_REG Register (Offset = F30h) [reset = 0h]

Register Description: MDIO Manual Interface Register

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Table 14-18314. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F30h

Figure 14-6048. CPSW3_MDIO_MANUAL_IF_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-18316. CPSW3_MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output. This value is the MDCLK_O output value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
1	MDIO_OE	R/W	0h	MDIO Output Enable. This value is inverted and output on the MDIO_OE_N output when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
0	MDIO_PIN	R/W	0h	MDIO Pin Value. This is the external MDIO data pin value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted '1'. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted '1' and MDIO_PIN is written with a 1h then MDIO_PIN should read a 1h if there are no external devices pulling the MDIO data line low.

14.9.2.1.52 CPSW3_MDIO_POLL_REG Register

CPSW3_MDIO_POLL_REG Register (Offset = F34h) [reset = 0h]

Register Description: MDIO Poll Register

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Table 14-18317. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F34h

Figure 14-6049. CPSW3_MDIO_POLL_REG Name Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANGEMODE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPG							
R/W							
0h							

Table 14-18319. CPSW3_MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	MDIO Manual Mode. When set 1h, the MDIO pins are directly controlled by software through the bits in the CPSW_MDIO_MANUAL_IF_REG register `1h Manual Mode.`

30	STATECHANGEMODE	R/W	0h	MDIO State Change Mode.
				When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations.
				`0h Normal Mode.`
				`1h State Change Mode.`

29:8	RESERVED	NONE	0h	Reserved
7:0	IPG	R/W	0h	Polling Inter Packet Gap Value. This value is the number of MDCLK_O clocks between each poll when polling is enabled.

14.9.2.1.53 CPSW3_MDIO_POLL_EN_REG Register

CPSW3_MDIO_POLL_EN_REG Register (Offset = F38h) [reset = FFFFFFFFh]

Register Description: MDIO Poll Enable Register

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Table 14-18320. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F38h

Figure 14-6050. CPSW3_MDIO_POLL_EN_REG Name Register

31	30	29	28	27	26	25	24
POLL_EN							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
POLL_EN							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
POLL_EN							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
POLL_EN							
R/W							
FFFFFFFFh							

Table 14-18322. CPSW3_MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POLL_EN	R/W	FFFFFFFFh	MDIO Poll Enable. When set, the bit indicates that the associated PHY will be included in polling operations. When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set (regardless of the value of the preamble disable bit ([20] PREAMBLE) in the CPSW_MDIO_CONTROL_REG register. However, there does not have to be a PHY at address 31.

14.9.2.1.54 CPSW3_MDIO_CLAUS45_REG Register

CPSW3_MDIO_CLAUS45_REG Register (Offset = F3Ch) [reset = 0h]

Register Description: MDIO Clause45 Register

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Table 14-18323. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F3Ch

Figure 14-6051. CPSW3_MDIO_CLAUS45_REG Name Register

31	30	29	28	27	26	25	24
CLAUSE45							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAUSE45							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAUSE45							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAUSE45							
R/W							
0h							

Table 14-18325. CPSW3_MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAUSE45	R/W	0h	MDIO clause 45 mode. When a clause45 bit is cleared 0h, the PHY associated with the clause45 bit is operating in the clause 22 mode. When set 1h, the PHY associated with the clause45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on.

14.9.2.1.55 CPSW3_MDIO_USER_ADDR0_REG Register

CPSW3_MDIO_USER_ADDR0_REG Register (Offset = F40h) [reset = 0h]

Register Description: MDIO Address 0 Register

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Table 14-18326. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F40h

Figure 14-6052. CPSW3_MDIO_USER_ADDR0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
USER_ADDR0							
R/W							
0h							
7	6	5	4	3	2	1	0
USER_ADDR0							
R/W							
0h							

Table 14-18328. CPSW3_MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR0	R/W	0h	MDIO User Address 0. In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIOUserAccess0 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess0 access.

14.9.2.1.56 CPSW3_MDIO_USER_ADDR1_REG Register

CPSW3_MDIO_USER_ADDR1_REG Register (Offset = F44h) [reset = 0h]

Register Description: MDIO Address 1 Register

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Table 14-18329. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F44h

Figure 14-6053. CPSW3_MDIO_USER_ADDR1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
USER_ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
USER_ADDR1							
R/W							
0h							

Table 14-18331. CPSW3_MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR1	R/W	0h	MDIO User Address 1. In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIOUserAccess1 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess1 access.

14.9.2.1.57 CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register

CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register (Offset = F80h + formula) [reset = 0h]

Register Description: MDIO User Access Register

Formula = (j * 8h); where j = 0 to 1d

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Table 14-18332. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F80h + formula

Figure 14-6054. CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>GO</td><td>WRITE</td><td>ACK</td><td colspan="3">RESERVED</td><td colspan="2">REGADR</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="3">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">REGADR</td><td colspan="5">PHYADR</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18334. CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go. Writing a 1h to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0h to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1h. If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1h causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28:26	RESERVED	NONE	0h	Reserved
25:21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.
20:16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.

Table 14-18334. CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

14.9.2.1.58 CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register

CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register (Offset = F84h + formula) [reset = 0h]

Register Description: MDIO User PHY Select Register

Formula = (j * 8h); where j = 0 to 1d

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Table 14-18335. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 0F84h + formula

Figure 14-6055. CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>LINKSEL</td><td>LINKINT_ENABLE</td><td>RESERVED</td><td colspan="5">PHYADR_MON</td></tr>
<tr><td>R/W</td><td>R/W</td><td>NONE</td><td colspan="5">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-18337. CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select. Set to 1h to determine link status using the MLINK pin. Default value is 0h which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1h to enable link change status interrupts for PHY address specified in [4-0] PHYADR_MON. Link change interrupts are disabled if this bit is set to 0h.
5	RESERVED	NONE	0h	Reserved
4:0	PHYADR_MON	R/W	0h	PHY address whose link status is monitored.

14.9.2.1.59 CPSW3_INTD_REVISION Register

CPSW3_INTD_REVISION Register (Offset = 1000h) [reset = 6690A200h]

Register Description: Revision Register

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Table 14-18338. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 1000h

Figure 14-6056. CPSW3_INTD_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">690h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">690h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTLVER</td><td colspan="3">MAJREV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">14h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINREV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-18340. CPSW3_INTD_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	BU
27:16	FUNCTION	R	690h	Module ID
15:11	RTLVER	R	14h	RTL revisions
10:8	MAJREV	R	2h	Major revision
7:6	CUSTOM	R	0h	Custom revision
5:0	MINREV	R	0h	Minor revision

14.9.2.1.60 CPSW3_INTD_EOI_REG Register

CPSW3_INTD_EOI_REG Register (Offset = 1010h) [reset = 0h]

Register Description: End of Interrupt Register

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Table 14-18341. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 1010h

Figure 14-6057. CPSW3_INTD_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-18343. CPSW3_INTD_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	End of Interrupt Vector

14.9.2.1.61 CPSW3_INTD_INTR_VECTOR_REG Register

CPSW3_INTD_INTR_VECTOR_REG Register (Offset = 1014h) [reset = 0h]

Register Description: Interrupt Vector Register

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Table 14-18344. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 1014h

Figure 14-6058. CPSW3_INTD_INTR_VECTOR_REG Name Register

31	30	29	28	27	26	25	24
INTR_VECTOR							
R							
0h							
23	22	21	20	19	18	17	16
INTR_VECTOR							
R							
0h							
15	14	13	12	11	10	9	8
INTR_VECTOR							
R							
0h							
7	6	5	4	3	2	1	0
INTR_VECTOR							
R							
0h							

Table 14-18346. CPSW3_INTD_INTR_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTR_VECTOR	R	0h	Interrupt Vector Register

14.9.2.1.62 CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register

CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register (Offset = 1100h) [reset = 0h]

Register Description: Enable Register 0

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Table 14-18347. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 1100h

Figure 14-6059. CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA	ENABLE_OUT_PULSE_EN_MDIO_PENDA	ENABLE_OUT_PULSE_EN_EVNT_PENDA
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-18349. CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_OUT_PULSE_EN_STAT_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVNT_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_evnt_penda

14.9.2.1.63 CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register

CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register (Offset = 1300h) [reset = 0h]

Register Description: Enable Clear Register 0

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Table 14-18350. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 1300h

Figure 14-6060. CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	ENABLE_OUT_PULSE_EN_EVNT_PENDA_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-18352. CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVNT_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_evnt_penda

14.9.2.1.64 CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register

CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register (Offset = 1500h) [reset = 0h]

Register Description: Status Register 0

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Table 14-18353. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 1500h

Figure 14-6061. CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					STATUS_OUT_PULSE_STAT_PENDA	STATUS_OUT_PULSE_MDIO_PENDA	STATUS_OUT_PULSE_EVNT_PENDA
NONE					R	R	R
0h					0h	0h	0h

Table 14-18355. CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	STATUS_OUT_PULSE_STAT_PENDA	R	0h	Status for out_pulse_en_stat_penda
1	STATUS_OUT_PULSE_MDIO_PENDA	R	0h	Status for out_pulse_en_mdio_penda
0	STATUS_OUT_PULSE_EVNT_PENDA	R	0h	Status for out_pulse_en_evnt_penda

14.9.2.1.65 CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register

CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register (Offset = 1A80h) [reset = 0h]

Register Description: Interrupt Vector for out_pulse

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Table 14-18356. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0800 1A80h

Figure 14-6062. CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Name Register

31	30	29	28	27	26	25	24
INTR_VECTOR_OUT_PULSE							
R							
0h							
23	22	21	20	19	18	17	16
INTR_VECTOR_OUT_PULSE							
R							
0h							
15	14	13	12	11	10	9	8
INTR_VECTOR_OUT_PULSE							
R							
0h							
7	6	5	4	3	2	1	0
INTR_VECTOR_OUT_PULSE							
R							
0h							

Table 14-18358. CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTR_VECTOR_OUT_PULSE	R	0h	Interrupt Vector

14.9.2.1.66 CPSW3_CPSW_NU_CPSW_ID_VER_REG Register

CPSW3_CPSW_NU_CPSW_ID_VER_REG Register (Offset = 20000h) [reset = 6BA80103h]

Register Description: CPSW ID Version

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Table 14-18359. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0000h

Figure 14-6063. CPSW3_CPSW_NU_CPSW_ID_VER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6BA8h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6BA8h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_VER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MINOR_VER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
</table>

Table 14-18361. CPSW3_CPSW_NU_CPSW_ID_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6BA8h	Identification Value
15:11	RTL_VER	R	0h	RTL Version Value
10:8	MAJOR_VER	R	1h	Major Version Value
7:0	MINOR_VER	R	3h	Minor Version Value

14.9.2.1.67 CPSW3_CPSW_NU_CONTROL_REG Register

CPSW3_CPSW_NU_CONTROL_REG Register (Offset = 20004h) [reset = 0h]

Register Description: CPSW Switch Control

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Table 14-18362. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0004h

Figure 14-6064. CPSW3_CPSW_NU_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
ECC_CRC_MODE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				CUT_THRU_ENABLE	EST_ENABLE	IET_ENABLE	EEE_ENABLE
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P0_RX_PASS_CRC_ERR	P0_RX_PAD	P0_TX_CRC_REMOVE	P0_TX_CRC_TYPE	P8_PASS_PRI_TAGGED	P7_PASS_PRI_TAGGED	P6_PASS_PRI_TAGGED	P5_PASS_PRI_TAGGED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P4_PASS_PRI_TAGGED	P3_PASS_PRI_TAGGED	P2_PASS_PRI_TAGGED	P1_PASS_PRI_TAGGED	P0_PASS_PRI_TAGGED	P0_ENABLE	VLAN_AWARE	S_CN_SWITCH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18364. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_CRC_MODE	R/W	0h	ECC CRC Mode. 0h `ECC errors induced through the ECC aggregator flip bits in the packet headers (not in packet data).` 1h `ECC errors induced through the ECC aggregator flip bits in the packet data (not in the packet headers).`
30:20	RESERVED	NONE	0h	Reserved
19	CUT_THRU_ENABLE	R/W	0h	Cut Thru Enable. 0h `Cut Thru disabled` 1h `Cut Thru enabled`
18	EST_ENABLE	R/W	0h	Enhanced Scheduled Traffic enable (EST) 0h `EST is disabled` 1h `EST is enabled`
17	IET_ENABLE	R/W	0h	Intersperced Express Traffic enable (IET) 0h `IET is disabled` 1h `IET is enabled`

Table 14-18364. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EEE_ENABLE	R/W	0h	Energy Efficient Ethernet enable 0h Energy Efficient Ethernet is disabled 1h Energy Efficient Ethernet is enabled
15	P0_RX_PASS_CRC_ERR	R/W	0h	Port 0 Pass Received CRC errors 0h Packets received with CRC errors on Port 0 are dropped. 1h Packets received with CRC errors on Port 0 are transferred to the destination ports.
14	P0_RX_PAD	R/W	0h	Port 0 Receive Short Packet Pad 0h Short packets are dropped. 1h Short packets are padded to 64-bytes (with pad and added CRC) if the CRC is not passed in. Short packets are dropped if the CRC is passed (in the Info0 word).
13	P0_TX_CRC_REMOVE	R/W	0h	Port 0 Transmit CRC remove. 0h Do not remove the CRC on Port 0 transmit (egress) packets. 1h Remove the CRC on all Port 0 transmit (egress) packets.
12	P0_TX_CRC_TYPE	R/W	0h	
11	P8_PASS_PRI_TAGGED	R/W	0h	Port 8 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P8_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
10	P7_PASS_PRI_TAGGED	R/W	0h	Port 7 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P7_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
9	P6_PASS_PRI_TAGGED	R/W	0h	Port 6 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P6_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
8	P5_PASS_PRI_TAGGED	R/W	0h	Port 5 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P5_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
7	P4_PASS_PRI_TAGGED	R/W	0h	Port 4 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P4_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
6	P3_PASS_PRI_TAGGED	R/W	0h	Port 3 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P3_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.

Table 14-18364. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	P2_PASS_PRI_TAGGED	R/W	0h	Port 2 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P2_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
4	P1_PASS_PRI_TAGGED	R/W	0h	Port 1 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P1_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
3	P0_PASS_PRI_TAGGED	R/W	0h	Port 0 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port P0_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
2	P0_ENABLE	R/W	0h	Port 0 Enable 0h CPPI port (port 0) packet operations are disabled 1h CPPI port (port 0) packet operations are enabled
1	VLAN_AWARE	R/W	0h	VLAN Aware Mode: 0h CPSW_NU is in the VLAN unaware mode. 1h CPSW_NU is in the VLAN aware mode.
0	S_CN_SWITCH	R/W	0h	Service or Customer VLAN switch. 0h Customer switch. VLAN processing uses the inner_vlan_ltype. 1h Service switch. VLAN processing uses the outer_vlan_ltype.

14.9.2.1.68 CPSW3_CPSW_NU_EM_CONTROL_REG Register

CPSW3_CPSW_NU_EM_CONTROL_REG Register (Offset = 20010h) [reset = 0h]

Register Description: CPSW Emulation Control

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Table 14-18365. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0010h

Figure 14-6065. CPSW3_CPSW_NU_EM_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-18367. CPSW3_CPSW_NU_EM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.9.2.1.69 CPSW3_CPSW_NU_STAT_PORT_EN_REG Register

CPSW3_CPSW_NU_STAT_PORT_EN_REG Register (Offset = 20014h) [reset = 0h]

Register Description: CPSW Statistics Port Enable

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Table 14-18368. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0014h

Figure 14-6066. CPSW3_CPSW_NU_STAT_PORT_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							P8_STAT_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18370. CPSW3_CPSW_NU_STAT_PORT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved

8	P8_STAT_EN	R/W	0h	Port 8 Statistics Enable (if N > 8)
				`0h Port 8 statistics are not enabled`
				`1h Port 8 statistics are enabled.`

7	P7_STAT_EN	R/W	0h	Port 7 Statistics Enable (if N > 7)
				`0h Port 7 statistics are not enabled`
				`1h Port 7 statistics are enabled.`

6	P6_STAT_EN	R/W	0h	Port 6 Statistics Enable (if N > 6)
				`0h Port 6 statistics are not enabled`
				`1h Port 6 statistics are enabled.`

5	P5_STAT_EN	R/W	0h	Port 5 Statistics Enable (if N > 5)
				`0h Port 5 statistics are not enabled`
				`1h Port 5 statistics are enabled.`

4	P4_STAT_EN	R/W	0h	Port 4 Statistics Enable (if N > 4)
				`0h Port 4 statistics are not enabled`
				`1h Port 4 statistics are enabled.`

3	P3_STAT_EN	R/W	0h	Port 3 Statistics Enable (if N > 3)
				`0h Port 3 statistics are not enabled`
				`1h Port 3 statistics are enabled.`

Table 14-18370. CPSW3_CPSW_NU_STAT_PORT_EN_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2	P2_STAT_EN	R/W	0h	Port 2 Statistics Enable (if N > 2)
				`0h Port 2 statistics are not enabled`
				`1h Port 2 statistics are enabled.`

1	P1_STAT_EN	R/W	0h	Port 1 Statistics Enable
				`0h Port 1 statistics are not enabled`
				`1h Port 1 statistics are enabled.`

0	P0_STAT_EN	R/W	0h	Port 0 Statistics Enable
				`0h Port 0 statistics are not enabled`
				`1h Port 0 statistics are enabled.`

14.9.2.1.70 CPSW3_CPSW_NU_PTYPE_REG Register

CPSW3_CPSW_NU_PTYPE_REG Register (Offset = 20018h) [reset = 0h]

Register Description: CPSW Transmit Priority Type

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Table 14-18371. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0018h

Figure 14-6067. CPSW3_CPSW_NU_PTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							P8_PTYPE_ESC
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC	P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			ESC_PRI_LD_VAL				
NONE			R/W				
0h			0h				

Table 14-18373. CPSW3_CPSW_NU_PTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved

16	P8_PTYPE_ESC	R/W	0h	Port 8 Priority Type Escalate (if N > 8)
				`0h Port 8 priority type fixed`
				`1h Port 8 priority type escalate`

15	P7_PTYPE_ESC	R/W	0h	Port 7 Priority Type Escalate (if N > 7)
				`0h Port 7 priority type fixed`
				`1h Port 7 priority type escalate`

14	P6_PTYPE_ESC	R/W	0h	Port 6 Priority Type Escalate (if N > 6)
				`0h Port 6 priority type fixed`
				`1h Port 6 priority type escalate`

13	P5_PTYPE_ESC	R/W	0h	Port 5 Priority Type Escalate (if N > 5)
				`0h Port 5 priority type fixed`
				`1h Port 5 priority type escalate`

12	P4_PTYPE_ESC	R/W	0h	Port 4 Priority Type Escalate (if N > 4)
				`0h Port 4 priority type fixed`
				`1h Port 4 priority type escalate`

Table 14-18373. CPSW3_CPSW_NU_PTYPE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	P3_PTYPE_ESC	R/W	0h	Port 3 Priority Type Escalate (if N > 3) 0h Port 3 priority type fixed 1h Port 3 priority type escalate
10	P2_PTYPE_ESC	R/W	0h	Port 2 Priority Type Escalate (if N > 2) 0h Port 2 priority type fixed 1h Port 2 priority type escalate
9	P1_PTYPE_ESC	R/W	0h	Port 1 Priority Type Escalate 0h Port 1 priority type fixed 1h Port 1 priority type escalate
8	P0_PTYPE_ESC	R/W	0h	Port 0 Priority Type Escalate 0h Port 0 priority type fixed 1h Port 0 priority type escalate
7:5	RESERVED	NONE	0h	Reserved
4:0	ESC_PRI_LD_VAL	R/W	0h	Escalate Priority Load Value. When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority. The min value of ESC_PRI_LD_VAL = 2h.

14.9.2.1.71 CPSW3_CPSW_NU_SOFT_IDLE_REG Register

CPSW3_CPSW_NU_SOFT_IDLE_REG Register (Offset = 2001Ch) [reset = 0h]

Register Description: CPSW Software Idle

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Table 14-18374. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 001Ch

Figure 14-6068. CPSW3_CPSW_NU_SOFT_IDLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_IDLE
NONE							R/W
0h							0h

Table 14-18376. CPSW3_CPSW_NU_SOFT_IDLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_IDLE	R/W	0h	Software Idle. 0h Not in Idle. 1h Command a MCU_CPSW0 software Idle. #br#When set, no packets will be started to be unloaded from ports 0 through 4 receive unload. Packets that are currently being unloaded are unaffected.

14.9.2.1.72 CPSW3_CPSW_NU_THRU_RATE_REG Register

CPSW3_CPSW_NU_THRU_RATE_REG Register (Offset = 20020h) [reset = 3001h]

Register Description: CPSW Thru Rate

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Table 14-18377. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0020h

Figure 14-6069. CPSW3_CPSW_NU_THRU_RATE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SL_RX_THRU_RATE				RESERVED			
R/W				NONE			
3h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				P0_RX_THRU_RATE			
NONE				R/W			
0h				1h			

Table 14-18379. CPSW3_CPSW_NU_THRU_RATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	SL_RX_THRU_RATE	R/W	3h	Ethernet Port Switch FIFO receive through rate. This register value is the maximum throughput of the Ethernet ports to the crossbar SCR. The default is one 8-byte word for every 3 VBUSP_GCLK periods maximum. The minimum value is 2. This is not a field that is intended to be changed by a user.
11:4	RESERVED	NONE	0h	Reserved
3:0	P0_RX_THRU_RATE	R/W	1h	CPPI FIFO (port 0) receive through rate. This register value is the maximum throughput of the CPPI FIFO (port 0) into the MCU_CPSW0. The minimum value is 1. This field is not intended to be changed by the user.

14.9.2.1.73 CPSW3_CPSW_NU_GAP_THRESH_REG Register

CPSW3_CPSW_NU_GAP_THRESH_REG Register (Offset = 20024h) [reset = Bh]

Register Description: CPSW Transmit FIFO Short Gap Threshold

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Table 14-18380. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0024h

Figure 14-6070. CPSW3_CPSW_NU_GAP_THRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			GAP_THRESH				
NONE			R/W				
0h			Bh				

Table 14-18382. CPSW3_CPSW_NU_GAP_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	GAP_THRESH	R/W	Bh	Ethernet Port Short Gap Threshold. This is the Ethernet port associated FIFO transmit block usage value for triggering transmit short gap (when short gap is enabled).

14.9.2.1.74 CPSW3_CPSW_NU_EEE_PRESCALE_REG Register

CPSW3_CPSW_NU_EEE_PRESCALE_REG Register (Offset = 2002Ch) [reset = 0h]

Register Description: CPSW Energy Efficient Ethernet Prescale Value

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Table 14-18383. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 002Ch

Figure 14-6071. CPSW3_CPSW_NU_EEE_PRESCALE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				EEE_PRESCALE			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
EEE_PRESCALE							
R/W							
0h							

Table 14-18385. CPSW3_CPSW_NU_EEE_PRESCALE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	EEE_PRESCALE	R/W	0h	Energy Efficient Ethernet Pre-scale count load value

14.9.2.1.75 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register

CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register (Offset = 20030h) [reset = FFFFFFFFh]

Register Description: CPSW PFC Tx Global Out Flow Threshold Set

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Table 14-18386. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0030h

Figure 14-6072. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
Fh				Fh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI5				PRI4			
R/W				R/W			
Fh				Fh			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI3				PRI2			
R/W				R/W			
Fh				Fh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI1				PRI0			
R/W				R/W			
Fh				Fh			

Table 14-18388. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

14.9.2.1.76 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register

CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register (Offset = 20034h) [reset = 0h]

Register Description: CPSW PFC Tx Global Out Flow Threshold Clear

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Table 14-18389. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0034h

Figure 14-6073. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
0h				0h			

Table 14-18391. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

14.9.2.1.77 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register

CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 20038h) [reset = FFFFFFFFh]

Register Description: CPSW PFC Global Tx Buffer Threshold Set Low

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Table 14-18392. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0038h

Figure 14-6074. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
PRI3							
R/W							
FFh							
23	22	21	20	19	18	17	16
PRI2							
R/W							
FFh							
15	14	13	12	11	10	9	8
PRI1							
R/W							
FFh							
7	6	5	4	3	2	1	0
PRI0							
R/W							
FFh							

Table 14-18394. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

14.9.2.1.78 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register

CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 2003Ch) [reset = FFFFFFFFh]

Register Description: CPSW PFC Global Tx Buffer Threshold Set High

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Table 14-18395. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 003Ch

Figure 14-6075. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
PRI7							
R/W							
FFh							
23	22	21	20	19	18	17	16
PRI6							
R/W							
FFh							
15	14	13	12	11	10	9	8
PRI5							
R/W							
FFh							
7	6	5	4	3	2	1	0
PRI4							
R/W							
FFh							

Table 14-18397. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

14.9.2.1.79 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register

CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 20040h) [reset = 0h]

Register Description: CPSW PFC Global Tx Buffer Threshold Clear Low

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Table 14-18398. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0040h

Figure 14-6076. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
PRI3							
R/W							
0h							
23	22	21	20	19	18	17	16
PRI2							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI1							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI0							
R/W							
0h							

Table 14-18400. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

14.9.2.1.80 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register

CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 20044h) [reset = 0h]

Register Description: CPSW PFC Global Tx Buffer Threshold Clear High

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Table 14-18401. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0044h

Figure 14-6077. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
PRI7							
R/W							
0h							
23	22	21	20	19	18	17	16
PRI6							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI5							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI4							
R/W							
0h							

Table 14-18403. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

14.9.2.1.81 CPSW3_CPSW_NU_VLAN_LTYPE_REG Register

CPSW3_CPSW_NU_VLAN_LTYPE_REG Register (Offset = 20050h) [reset = 88A88100h]

Register Description: VLAN Length/type

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Table 14-18404. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0050h

Figure 14-6078. CPSW3_CPSW_NU_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
VLAN_LTYPE_OUTER							
R/W							
88A8h							
23	22	21	20	19	18	17	16
VLAN_LTYPE_OUTER							
R/W							
88A8h							
15	14	13	12	11	10	9	8
VLAN_LTYPE_INNER							
R/W							
8100h							
7	6	5	4	3	2	1	0
VLAN_LTYPE_INNER							
R/W							
8100h							

Table 14-18406. CPSW3_CPSW_NU_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	VLAN_LTYPE_OUTER	R/W	88A8h	Outer VLAN LType
15:0	VLAN_LTYPE_INNER	R/W	8100h	Inner VLAN LType

14.9.2.1.82 CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register

CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register (Offset = 20054h) [reset = 0h]

Register Description: Enhanced Scheduled Traffic Host Event Domain

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Table 14-18407. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0054h

Figure 14-6079. CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EST_TS_DOMAIN							
R/W							
0h							

Table 14-18409. CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EST_TS_DOMAIN	R/W	0h	Enhanced Scheduled Traffic Host Event Domain. This value is used as the domain in the CPTS event to indicate that the event came from EST.

14.9.2.1.83 CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register

CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register (Offset = 20058h) [reset = 0h]

Register Description: Cut-thru Threshold

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Table 14-18410. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0058h

Figure 14-6080. CPSW3_CPSW_NU_CUT_THRESHOLD_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CUT_THRESH			
NONE				R/W			
0h				0h			

Table 14-18412. CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CUT_THRESH	R/W	0h	Cut_thru_threshold. This is not intended to be changed by software.

14.9.2.1.84 CPSW3_CPSW_NU_FREQUENCY_REG Register

CPSW3_CPSW_NU_FREQUENCY_REG Register (Offset = 2005Ch) [reset = 0h]

Register Description: CPSW CPPI_CLK Frequency in Mhz

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Table 14-18413. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 005Ch

Figure 14-6081. CPSW3_CPSW_NU_FREQUENCY_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CPSW_FREQUENCY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CPSW_FREQUENCY							
R/W							
0h							

Table 14-18415. CPSW3_CPSW_NU_FREQUENCY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	CPSW_FREQUENCY	R/W	0h	CPSW Frequency. This is the frequency in Mhz of the VBUSP_GCLK. The frequency is rounded to the nearest Mhz. This value is used in auto speed detection for cut-thru operations.

14.9.2.1.85 CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register

CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register (Offset = 20060h) [reset = 64h]

Register Description: IET Hold Count Load Value

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Table 14-18416. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0060h

Figure 14-6082. CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IET_HOLD_CNT_LD_VAL							
R/W							
64h							

Table 14-18418. CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	IET_HOLD_CNT_LD_VAL	R/W	64h	Cut-thru IET Hold Count Load Value. This value is loaded into counters to count the time that cut-thru packets are allowed to prempt traffic in advance in order to reduce cut-thru latency with IET operations. This is not intended to be changed by software.

14.9.2.1.86 CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register

CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register (Offset = 20100h) [reset = 7E8h]

Register Description: Transmit Priority 0 Maximum Length

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Table 14-18419. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0100h

Figure 14-6083. CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI0_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI0_MAXLEN							
R/W							
7E8h							

Table 14-18421. CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI0_MAXLEN	R/W	7E8h	Transmit Priority 0 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on egress for all ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.2.1.87 CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register

CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register (Offset = 20104h) [reset = 7E8h]

Register Description: Transmit Priority 1 Maximum Length

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Table 14-18422. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0104h

Figure 14-6084. CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI1_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI1_MAXLEN							
R/W							
7E8h							

Table 14-18424. CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI1_MAXLEN	R/W	7E8h	Transmit Priority 1 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.2.1.88 CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register

CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register (Offset = 20108h) [reset = 7E8h]

Register Description: Transmit Priority 2 Maximum Length

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Table 14-18425. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0108h

Figure 14-6085. CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI2_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI2_MAXLEN							
R/W							
7E8h							

Table 14-18427. CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI2_MAXLEN	R/W	7E8h	Transmit Priority 2 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.2.1.89 CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register

CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register (Offset = 2010Ch) [reset = 7E8h]

Register Description: Transmit Priority 3 Maximum Length

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Table 14-18428. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 010Ch

Figure 14-6086. CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI3_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI3_MAXLEN							
R/W							
7E8h							

Table 14-18430. CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI3_MAXLEN	R/W	7E8h	Transmit Priority 3 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.2.1.90 CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register

CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register (Offset = 20110h) [reset = 7E8h]

Register Description: Transmit Priority 4 Maximum Length

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Table 14-18431. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0110h

Figure 14-6087. CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI4_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI4_MAXLEN							
R/W							
7E8h							

Table 14-18433. CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI4_MAXLEN	R/W	7E8h	Transmit Priority 4 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.2.1.91 CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register

CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register (Offset = 20114h) [reset = 7E8h]

Register Description: Transmit Priority 5 Maximum Length

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Table 14-18434. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0114h

Figure 14-6088. CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TX_PRI5_MAXLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">7E8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_PRI5_MAXLEN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E8h</td></tr>
</table>

Table 14-18436. CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI5_MAXLEN	R/W	7E8h	Transmit Priority 5 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.2.1.92 CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register

CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register (Offset = 20118h) [reset = 7E8h]

Register Description: Transmit Priority 6 Maximum Length

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Table 14-18437. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 0118h

Figure 14-6089. CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TX_PRI6_MAXLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">7E8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_PRI6_MAXLEN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E8h</td></tr>
</table>

Table 14-18439. CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI6_MAXLEN	R/W	7E8h	Transmit Priority 6 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.2.1.93 CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register

CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register (Offset = 2011Ch) [reset = 7E8h]

Register Description: Transmit Priority 7 Maximum Length

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Table 14-18440. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 011Ch

Figure 14-6090. CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI7_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI7_MAXLEN							
R/W							
7E8h							

Table 14-18442. CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI7_MAXLEN	R/W	7E8h	Transmit Priority 7 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.9.2.1.94 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register (Offset = 21004h) [reset = 0h]

Register Description: CPPI Port 0 Control

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Table 14-18443. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1004h

Figure 14-6091. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CUT_THRU_MODE_ETH	RX_REMAP_DSCP_V6	RX_REMAP_DSCP_V4	RX_REMAP_VLAN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RX_CHECKSUM_EN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-18445. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	CUT_THRU_MODE_ETH	R/W	0h	Port 0 Cut-Thru Mode. Packets always egress from the host port (CPPI egress) store-and-forward regardless of this bit setting. This bit determines how a receive port operates when the host port is in a cut-thru packet destination mask. 0h Force packets with the host port in the destination mask to be store-and-forward to all destination ports. 1h The host port operates similar to Ethernet ports. A cut-thru packet with the host in the destination mask will not force the packet to be store-and-forward unless the cut-thru packet is held off due to word counts or because another cut-thru packet on the host port priority.
18	RX_REMAP_DSCP_V6	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
17	RX_REMAP_DSCP_V4	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
16	RX_REMAP_VLAN	R/W	0h	Port 0 receive remap thread to VLAN.

Table 14-18445. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RX_ECC_ERR_EN	R/W	0h	Port 0 receive ECC Error Enable. This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port 0 transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations
13:3	RESERVED	NONE	0h	Reserved

2	DSCP_IPV6_EN	R/W	0h	Port 0 IPv6 DSCP enable
				`0h IPV6 DSCP priority mapping is disabled`
				`1h IPV6 DSCP priority mapping is enabled`

1	DSCP_IPV4_EN	R/W	0h	Port 0 IPV4 DSCP enable
				`0h IPV4 DSCP priority mapping is disabled`
				`1h IPV4 DSCP priority mapping is enabled`

0	RX_CHECKSUM_EN	R/W	0h	Port 0 Receive (port 0 ingress) Checksum Enable
				`0h Port 0 receive checksum is disabled`
				`1h Port 0 receive checksum is enabled`

14.9.2.1.95 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register (Offset = 21008h) [reset = 0h]

Register Description: CPPI Port 0 Flow ID Offset

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Table 14-18446. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1008h

Figure 14-6092. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		VALUE					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 14-18448. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	VALUE	R/W	0h	This value is added to the thread/Flow_ID in CPPI transmit PSI Info Word 0

14.9.2.1.96 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register (Offset = 21010h) [reset = 1h]

Register Description: CPPI Port 0 FIFO Block Usage Count

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Table 14-18449. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1010h

Figure 14-6093. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT					
NONE		R					
0h		1h					

Table 14-18451. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Port 0 Transmit Block Count Usage. This value is the number of blocks allocated to the FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT	R	1h	Port 0 Receive Block Count Usage. This value is the number of blocks allocated in the receive FIFO.

14.9.2.1.97 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register (Offset = 21014h) [reset = 0h]

Register Description: CPPI Port 0 VLAN

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Table 14-18452. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1014h

Figure 14-6094. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W			R/W	R/W			
0h			0h	0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W							
0h							

Table 14-18454. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.9.2.1.98 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register (Offset = 21018h) [reset = 76543210h]

Register Description: CPPI Port 0 Tx Header Pri to Switch Pri Mapping

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Table 14-18455. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1018h

Figure 14-6095. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
aah	7h			55h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
2ah	5h			15h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
ah	3h			5h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
2h	1h			1h	0h		

Table 14-18457. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	aah	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	55h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	2ah	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	15h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	ah	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	5h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	NONE	2h	Reserved

Table 14-18457. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	NONE	1h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.9.2.1.99 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register (Offset = 2101Ch) [reset = 0h]

Register Description: CPPI Port 0 Priority Control

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Table 14-18458. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 101Ch

Figure 14-6096. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>RX_PTYPE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18460. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority).
15:9	RESERVED	NONE	0h	Reserved

8	RX_PTYPE	R/W	0h	Receive Priority Type
				`0h Fixed priority`
				`1h Round Robin priority`

7:0	RESERVED	NONE	0h	Reserved

14.9.2.1.100 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register (Offset = 21020h) [reset = 76543210h]

Register Description: CPPI Port 0 RX Pkt Pri to Header Pri Map

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Table 14-18461. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1020h

Figure 14-6097. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
aah	7h			55h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
2ah	5h			15h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
ah	3h			5h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
2h	1h			1h	0h		

Table 14-18463. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	aah	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	55h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	2ah	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	15h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	ah	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	5h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	NONE	2h	Reserved

Table 14-18463. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	NONE	1h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.9.2.1.101 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register (Offset = 21024h) [reset = 5EEh]

Register Description: CPPI Port 0 Receive Frame Max Length

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Table 14-18464. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1024h

Figure 14-6098. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RX_MAXLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">5EEh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RX_MAXLEN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5EEh</td></tr>
</table>

Table 14-18466. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_P0_RX_MAXLEN_REG are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN) when fifo_blk_size = 4. When fifo_blk_size = 1 the maximum value is 2024 (including VLAN).

14.9.2.1.102 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register (Offset = 21028h) [reset = 1245678h]

Register Description: CPPI Port 0 Transmit Block Sub Per Priority

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Table 14-18467. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1028h

Figure 14-6099. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-18469. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 7 frames (value 0 means use all).
27:24	PRI6	R/W	1h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 6 frames (value 0 means use all).
23:20	PRI5	R/W	2h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 5 frames (value 0 means use all).
19:16	PRI4	R/W	4h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 4 frames (value 0 means use all).
15:12	PRI3	R/W	5h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 3 frames (value 0 means use all).
11:8	PRI2	R/W	6h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 2 frames (value 0 means use all).

Table 14-18469. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	PRI1	R/W	7h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 1 frames (value 0 means use all).
3:0	PRI0	R/W	8h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 0 frames (value 0 means use all).

14.9.2.1.103 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register (Offset = 21030h) [reset = 0h]

Register Description: Port 0 EEE Idle to LPI counter

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Table 14-18470. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1030h

Figure 14-6100. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18472. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Port 0 EEE Idle to LPI counter load value

14.9.2.1.104 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register (Offset = 21034h) [reset = 0h]

Register Description: Port 0 EEE LPI to wake counter

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Table 14-18473. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1034h

Figure 14-6101. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18475. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Port 0 EEE LPI to wake counter load value

14.9.2.1.105 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register (Offset = 21038h) [reset = 60h]

Register Description: Port 0 EEE status

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Table 14-18476. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1038h

Figure 14-6102. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-18478. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	CPPI port 0 transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	CPPI port 0 receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	CPPI port 0 transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	CPPI port 0 transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	CPPI port 0 transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	0h	CPPI port 0 receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.9.2.1.106 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register (Offset = 21050h) [reset = 0h]

Register Description: Port 0 FIFO Status

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Table 14-18479. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1050h

Figure 14-6103. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_PRI_ACTIVE							
R							
0h							

Table 14-18481. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_PRI_ACTIVE	R	0h	Port 0 Transmit FIFO Priority Active. Each bit indicates whether the corresponding FIFO priority has one or more queued packets on it or not. Note: For N=2 this field is always zero (there is no transmit FIFO).

14.9.2.1.107 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register (Offset = 21120h + formula) [reset = 0h]

Register Description: CPPI Port 0 Receive IPV4/IPV6 DSCP Map N

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18482. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1120h + formula

Figure 14-6104. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-18484. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved

Table 14-18484. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.9.2.1.108 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Register (Offset = 21140h + formula) [reset = 0h]

Register Description: CPPI Port 0 Rx Priority P Committed Information Rate

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18485. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1140h + formula

Figure 14-6105. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PRI_CIR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td colspan="8">PRI_CIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td colspan="8">PRI_CIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">PRI_CIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18487. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N Committed Information Rate Count Value

14.9.2.1.109 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Register (Offset = 21160h + formula) [reset = 0h]

Register Description: CPPI Port 0 Rx Priority P Excess Information Rate

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18488. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1160h + formula

Figure 14-6106. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 14-18490. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N EIR

14.9.2.1.110 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register (Offset = 21180h) [reset = 1F1F1F1Fh]

Register Description: CPPI Port 0 Tx PFC Destination Threshold Set Low

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Table 14-18491. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1180h

Figure 14-6107. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-18493. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.2.1.111 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register (Offset = 21184h) [reset = 1F1F1F1Fh]

Register Description: CPPI Port 0 Tx PFC Destination Threshold Set High

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Table 14-18494. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1184h

Figure 14-6108. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-18496. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.2.1.112 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register (Offset = 21188h) [reset = 0h]

Register Description: CPPI Port 0 Tx PFC Destination Threshold Clr Low

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Table 14-18497. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1188h

Figure 14-6109. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-18499. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.2.1.113 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register (Offset = 2118Ch) [reset = 0h]

Register Description: CPPI Port 0 Tx PFC Destination Threshold Clr High

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Table 14-18500. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 118Ch

Figure 14-6110. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-18502. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.2.1.114 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 21190h) [reset = 1F1F1F1Fh]

Register Description: CPPI Port 0 Tx PFC Global Buffer Threshold Set Low

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Table 14-18503. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1190h

Figure 14-6111. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-18505. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.2.1.115 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 21194h) [reset = 1F1F1F1Fh]

Register Description: CPPI Port 0 Tx PFC Global Buffer Threshold Set High

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Table 14-18506. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1194h

Figure 14-6112. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-18508. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.2.1.116 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 21198h) [reset = 0h]

Register Description: CPPI Port 0 Tx PFC Global Buffer Threshold Clr Low

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Table 14-18509. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1198h

Figure 14-6113. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-18511. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.2.1.117 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2119Ch) [reset = 0h]

Register Description: CPPI Port 0 Tx PFC Global Buffer Threshold Clr High

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Table 14-18512. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 119Ch

Figure 14-6114. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-18514. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.2.1.118 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register (Offset = 21300h) [reset = 4030201h]

Register Description: CPPI Port 0 CPPI Source ID A

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Table 14-18515. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1300h

Figure 14-6115. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Name Register

31	30	29	28	27	26	25	24
PORT4							
R/W							
4h							
23	22	21	20	19	18	17	16
PORT3							
R/W							
3h							
15	14	13	12	11	10	9	8
PORT2							
R/W							
2h							
7	6	5	4	3	2	1	0
PORT1							
R/W							
1h							

Table 14-18517. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT4	R/W	4h	Port 4 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 4.
23:16	PORT3	R/W	3h	Port 3 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 3.
15:8	PORT2	R/W	2h	Port 2 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 2.
7:0	PORT1	R/W	1h	Port 1 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 1.

14.9.2.1.119 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register (Offset = 21304h) [reset = 8070605h]

Register Description: CPPI Port 0 CPPI Source ID B

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Table 14-18518. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1304h

Figure 14-6116. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Name Register

31	30	29	28	27	26	25	24
PORT8							
R/W							
8h							
23	22	21	20	19	18	17	16
PORT7							
R/W							
7h							
15	14	13	12	11	10	9	8
PORT6							
R/W							
6h							
7	6	5	4	3	2	1	0
PORT5							
R/W							
5h							

Table 14-18520. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT8	R/W	8h	Port 8 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 8.
23:16	PORT7	R/W	7h	Port 7 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 7.
15:8	PORT6	R/W	6h	Port 6 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 6.
7:0	PORT5	R/W	5h	Port 5 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 5.

14.9.2.1.120 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register

CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register (Offset = 21320h) [reset = 0h]

Register Description: CPPI Port 0 Host Blocks Priority

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Table 14-18521. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 1320h

Figure 14-6117. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI5				PRI4			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI3				PRI2			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI1				PRI0			
R/W				R/W			
0h				0h			

Table 14-18523. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Host Blocks
27:24	PRI6	R/W	0h	Priority 6 Host Blocks
23:20	PRI5	R/W	0h	Priority 5 Host Blocks
19:16	PRI4	R/W	0h	Priority 4 Host Blocks
15:12	PRI3	R/W	0h	Priority 3 Host Blocks
11:8	PRI2	R/W	0h	Priority 2 Host Blocks
7:4	PRI1	R/W	0h	Priority 1 Host Blocks
3:0	PRI0	R/W	0h	Priority 0 Host Blocks

14.9.2.1.121 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register (Offset = 22000h) [reset = 0h]

Register Description: Reserved

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Table 14-18524. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2000h

Figure 14-6118. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-18526. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved register for memory map alignment

14.9.2.1.122 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register (Offset = 22004h) [reset = 0h]

Register Description: Enet Port N Control

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Table 14-18527. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2004h

Figure 14-6119. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EST_PORT_EN	IET_PORT_EN
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	TX_CUT_IET_HOLD_DIS	TX_LPI_CLKSTOP_EN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
NONE					R/W	R/W	NONE
0h					0h	0h	0h

Table 14-18529. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable. 0h `EST is disabled on the port` 1h `EST is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.`
16	IET_PORT_EN	R/W	0h	Intersperced Express Traffic (IET) Port Enable. 0h `IET is disabled on the port` 1h `IET is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.`
15	RX_ECC_ERR_EN	R/W	0h	Port N receive ECC Error Enable. This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port N transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations

Table 14-18529. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TX_CUT_IET_HOLD_DIS	R/W	0h	Port N transmit IET hold due to cut-thru disable 0h Cut-thru packets to the port will cause premptable traffic to be prempted as early as possible minimizing cut-thru latency 1h Cut-thru packets to the port will be prempted as usual by the express MAC
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable. When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11:3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	IPV6 DSCP enable 0h IPV6 DSCP priority mapping is disabled 1h IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	IPV4 DSCP enable 0h IPV4 DSCP priority mapping is disabled 1h IPV4 DSCP priority mapping is enabled
0	RESERVED	NONE	0h	Reserved

14.9.2.1.123 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register (Offset = 22008h) [reset = 1004h]

Register Description: Enet Port N FIFO Max Blocks

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Table 14-18530. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2008h

Figure 14-6120. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_MAX_BLKS							
R/W							
10h							
7	6	5	4	3	2	1	0
RX_MAX_BLKS							
R/W							
4h							

Table 14-18532. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit Max Blocks. The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive, when Fullduplex flow control is enabled (CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX = 1h) to allow for flow control runout.
7:0	RX_MAX_BLKS	R/W	4h	Receive Max Blocks. The maximum number of blocks allowed on the express and prempt receive FIFOs (transmit and receive FIFO's combined when fifo_oneram = 1)

14.9.2.1.124 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register (Offset = 22010h) [reset = 1h]

Register Description: Enet Port N FIFO Block Usage Count

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Table 14-18533. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2010h

Figure 14-6121. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		RX_BLK_CNT_P					
NONE		R					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT_E					
NONE		R					
0h		1h					

Table 14-18535. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO prempt receive queue. No blocks are allocated until the CPSW_CONTROL_REG[17] IET_ENABLE is set.
15:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage. This value is the number of blocks allocated to the port's FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO express receive queue.

14.9.2.1.125 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register (Offset = 22014h) [reset = 0h]

Register Description: Enet Port N VLAN

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Table 14-18536. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2014h

Figure 14-6122. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">PORT_PRI</td><td>PORT_CFI</td><td colspan="4">PORT_VID</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PORT_VID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18538. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.9.2.1.126 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register (Offset = 22018h) [reset = 76543210h]

Register Description: Enet Port N Tx Header Pri to Switch Pri Mapping

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Table 14-18539. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2018h

Figure 14-6123. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
aah	7h			55h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
2ah	5h			15h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
ah	3h			5h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
2h	1h			1h	0h		

Table 14-18541. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	aah	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	55h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	2ah	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	15h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	ah	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	5h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.

Table 14-18541. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	2h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	NONE	1h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.9.2.1.127 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register (Offset = 2201Ch) [reset = 9000h]

Register Description: Enet Port N Priority Control

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Table 14-18542. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 201Ch

Figure 14-6124. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24
TX_FLOW_PRI							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_FLOW_PRI							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TX_HOST_BLKS_REM				RESERVED			
R/W				NONE			
9h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-18544. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE	0h	Reserved

14.9.2.1.128 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register (Offset = 22020h) [reset = 76543210h]

Register Description: Enet Port N RX Pkt Pri to Header Pri Map

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Table 14-18545. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2020h

Figure 14-6125. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
aah	7h			55h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
2ah	5h			15h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
ah	3h			5h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
2h	1h			1h	0h		

Table 14-18547. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	aah	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	55h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	2ah	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	15h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	ah	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	5h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.

Table 14-18547. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	2h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	NONE	1h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.9.2.1.129 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register (Offset = 22024h) [reset = 5EEh]

Register Description: Enet Port N Receive Frame Max Length

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Table 14-18548. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2024h

Figure 14-6126. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		RX_MAXLEN					
NONE		R/W					
0h		5EEh					
7	6	5	4	3	2	1	0
RX_MAXLEN							
R/W							
5EEh							

Table 14-18550. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).

14.9.2.1.130 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register (Offset = 22028h) [reset = 1245678h]

Register Description: Enet Port N Transmit Block Sub Per Priority

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Table 14-18551. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2028h

Figure 14-6127. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-18553. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

14.9.2.1.131 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register (Offset = 22030h) [reset = 0h]

Register Description: Enet Port N EEE Idle to LPI counter

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Table 14-18554. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2030h

Figure 14-6128. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18556. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value

14.9.2.1.132 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register (Offset = 22034h) [reset = 0h]

Register Description: Enet Port N EEE LPI to wake counter

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Table 14-18557. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2034h

Figure 14-6129. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18559. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value

14.9.2.1.133 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register (Offset = 22038h) [reset = 62h]

Register Description: Enet Port N EEE status

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Table 14-18560. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2038h

Figure 14-6130. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	1h	0h

Table 14-18562. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.9.2.1.134 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register (Offset = 22040h) [reset = 8h]

Register Description: Enet Port N IET Control

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Table 14-18563. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2040h

Figure 14-6131. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_PREMPT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					MAC_ADDFRAGSIZE		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				MAC_LINKFAIL	MAC_DISABLEVERIFY	MAC_HOLD	MAC_PENABLE
NONE				R/W	R/W	R/W	R/W
0h				1h	0h	0h	0h

Table 14-18565. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAC_PREMPT	R/W	0h	Mac Preempt Queue - Indicates which transmit FIFO queues are sent to the preempt MAC. Bit 0 indicates queue zero, bit 1 queue 1 and so on. Packets will be sent to the preempt MAC only when MAC_PENABLE is set, and when MAC_VERIFIED (from CPSW_PN_IET_STATUS_REG_k) or MAC_DISABLEVERIFY is set, and when IET_PORT_EN is set.
15:11	RESERVED	NONE	0h	Reserved
10:8	MAC_ADDFRAGSIZE	R/W	0h	Mac Fragment Size - An integer in the range 0:7 indicating, as a multiple of 64, the minimum additional length for nonfinal mPackets. 0 64 1 128 2 81 3 256 4 320 5 384 6 448 7 512
7:4	RESERVED	NONE	0h	Reserved

Table 14-18565. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MAC_LINKFAIL	R/W	1h	Mac Link Fail - Link Fail Indicator to reset the verify state machine. This bit is reset high. Verify and response frames will be sent/allowed when this bit is cleared.
2	MAC_DISABLEVERIFY	R/W	0h	Mac Disable Verify - Disables verification on the port when set. If this bit is set then packets will be sent to the preempt Mac when MAC_PENABLE is set (This is a forced mode with no IET verification).
1	MAC_HOLD	R/W	0h	Mac Hold - Hold Preemption on the port.
0	MAC_PENABLE	R/W	0h	Mac Preemption Enable - Port Preemption Enable. This takes effect only when IET_PORT_EN is set.

14.9.2.1.135 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register (Offset = 22044h) [reset = 0h]

Register Description: Enet Port N IET Status

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Table 14-18566. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2044h

Figure 14-6132. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MAC_VERIFY_ERR	MAC_RESPOND_ERR	MAC_VERIFY_FAIL	MAC_VERIFIED
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-18568. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MAC_VERIFY_ERR	R	0h	Mac Received Verify Packet with Errors - Set when a verify packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
2	MAC_RESPOND_ERR	R	0h	Mac Received Respond Packet with Errors - Set when a respond packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
1	MAC_VERIFY_FAIL	R	0h	Mac Verification Failed - Indication that verification was unsuccessful.
0	MAC_VERIFIED	R	0h	Mac Verified - Indication that verification was successful.

14.9.2.1.136 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register (Offset = 22048h) [reset = 1312D0h]

Register Description: Enet Port N IET VERIFY

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Table 14-18569. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2048h

Figure 14-6133. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_VERIFY_CNT							
R/W							
1312D0h							
15	14	13	12	11	10	9	8
MAC_VERIFY_CNT							
R/W							
1312D0h							
7	6	5	4	3	2	1	0
MAC_VERIFY_CNT							
R/W							
1312D0h							

Table 14-18571. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MAC_VERIFY_CNT	R/W	1312D0h	Mac Verify Timeout Count - The number of wireside clocks contained in the verify timeout counter. The default is 0x1312D0 (10ms at 125MHz in gig mode).

14.9.2.1.137 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register (Offset = 22050h) [reset = FF00h]

Register Description: Enet Port N FIFO STATUS

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Table 14-18572. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2050h

Figure 14-6134. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE					R	R	R
0h					0h	0h	0h
15	14	13	12	11	10	9	8
TX_E_MAC_ALLOW							
R							
FFh							
7	6	5	4	3	2	1	0
TX_PRI_ACTIVE							
R							
0h							

Table 14-18574. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	EST_BUFACT	R	0h	EST RAM active buffer. Indicates the active 64-word fetch buffer when CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared to zero. Indicates the fetch RAM address MSB when bit [0] EST_ONEBUF is set to one.
17	EST_ADD_ERR	R	0h	EST Address Error. Indicates that the fetch RAM was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error. Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15:8	TX_E_MAC_ALLOW	R	FFh	EST transmit MAC allow. Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the prempt queue).
7:0	TX_PRI_ACTIVE	R	0h	EST Transmit Priority Active. Bus that indicates which priorities have packets (non-empty) at the time of the register read.

14.9.2.1.138 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register (Offset = 22060h) [reset = 0h]

Register Description: Enet Port N EST CONTROL

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Table 14-18575. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2060h

Figure 14-6135. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED						EST_FILL_MARGIN	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
EST_FILL_MARGIN							
R/W							
0h							
15	14	13	12	11	10	9	8
EST_PREMPT_COMP							EST_FILL_EN
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-18577. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin. Sets the fill margin required to ensure that the Ethernet wire is clear (including IPG) so that the timed EST express packet can egress at the required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended.
15:9	EST_PREMPT_COMP	R/W	0h	EST Prempt Comparison Value. When the count in a zero allow is less than or equal to this value in bytes (times 8), prempt packets are cleared from the wire. This is the prempt clear margin value.
8	EST_FILL_EN	R/W	0h	EST Fill Enable. Enable EST fill mode.
7:5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority. Selects the express priority that timestamp(s) will be generated on when CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI bit is set.
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority. When set, timestamp only enabled packets on the express priority selected by CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI bit field. When cleared to zero, express packet selection for timestamp is independent of priority.

Table 14-18577. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only. Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI is also set then the timestamp is generated only on the first packet on CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI).
2	EST_TS_EN	R/W	0h	EST Timestamp Enable. Enable express timestamps (when CPSW_CONTROL_REG[18] EST_ENABLE and CPSW_PN_CONTROL_REG_k[17] EST_PORT_EN bits are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select. If CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the CPSW_PN_FIFO_STATUS_REG_k register, bit [18] EST_BUFACT.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer. When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The CPSW_PN_EST_CONTROL_REG_k[1] EST_BUFSEL bit selects the buffer to be used when bit [0] EST_ONEBUF is cleared to zero.

14.9.2.1.139 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register (Offset = 22120h + formula) [reset = 0h]

Register Description: Enet Port N Receive IPV4/IPV6 DSCP Map M

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18578. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2120h + formula

Figure 14-6136. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-18580. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved

Table 14-18580. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.9.2.1.140 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Register (Offset = 22140h + formula) [reset = 0h]

Register Description: Enet Port N Rx Priority P Committed Information Rate Value

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18581. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2140h + formula

Figure 14-6137. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_CIR							
R/W							
0h							

Table 14-18583. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

14.9.2.1.141 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Register (Offset = 22160h + formula) [reset = 0h]

Register Description: Enet Port N Rx Priority P Excess Informatoin Rate Value

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18584. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2160h + formula

Figure 14-6138. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 14-18586. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

14.9.2.1.142 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register (Offset = 22180h) [reset = 1F1F1F1Fh]

Register Description: Enet Port N Tx PFC Destination Threshold Set Low

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Table 14-18587. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2180h

Figure 14-6139. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-18589. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.2.1.143 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register (Offset = 22184h) [reset = 1F1F1F1Fh]

Register Description: Enet Port N Tx PFC Destination Threshold Set High

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Table 14-18590. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2184h

Figure 14-6140. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-18592. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.2.1.144 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 22188h) [reset = 0h]

Register Description: Enet Port N Tx PFC Destination Threshold Clr Low

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Table 14-18593. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2188h

Figure 14-6141. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-18595. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.2.1.145 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 2218Ch) [reset = 0h]

Register Description: Enet Port N Tx PFC Destination Threshold Clr High

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Table 14-18596. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 218Ch

Figure 14-6142. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-18598. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.2.1.146 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 22190h) [reset = 1F1F1F1Fh]

Register Description: Enet Port N Tx PFC Global Buffer Threshold Set Low

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Table 14-18599. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2190h

Figure 14-6143. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-18601. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.2.1.147 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 22194h) [reset = 1F1F1F1Fh]

Register Description: Enet Port N Tx PFC Global Buffer Threshold Set High

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Table 14-18602. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2194h

Figure 14-6144. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-18604. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.2.1.148 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 22198h) [reset = 0h]

Register Description: Enet Port N Tx PFC Global Buffer Threshold Clr Low

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Table 14-18605. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2198h

Figure 14-6145. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-18607. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.2.1.149 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2219Ch) [reset = 0h]

Register Description: Enet Port N Tx PFC Global Buffer Threshold Clr High

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Table 14-18608. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 219Ch

Figure 14-6146. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-18610. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.2.1.150 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 22300h) [reset = 0h]

Register Description: Enet Port N Tx Destination Out Flow Add Values Low

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Table 14-18611. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2300h

Figure 14-6147. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-18613. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

14.9.2.1.151 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 22304h) [reset = 0h]

Register Description: Enet Port N Tx Destination Out Flow Add Values High

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Table 14-18614. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2304h

Figure 14-6148. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-18616. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

14.9.2.1.152 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register (Offset = 22308h) [reset = 0h]

Register Description: Enet Port N Tx Pause Frame Source Address Low

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Table 14-18617. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2308h

Figure 14-6149. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_15_8							
R/W							
0h							

Table 14-18619. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

14.9.2.1.153 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register (Offset = 2230Ch) [reset = 0h]

Register Description: Enet Port N Tx Pause Frame Source Address High

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Table 14-18620. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 230Ch

Figure 14-6150. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24
MACSRCADDR_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
MACSRCADDR_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_47_40							
R/W							
0h							

Table 14-18622. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

14.9.2.1.154 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register (Offset = 22310h) [reset = 0h]

Register Description: Enet Port N Time Sync Control

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Table 14-18623. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2310h

Figure 14-6151. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_MSG_TYPE_EN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18625. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
15:12	RESERVED	NONE	0h	Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable

Table 14-18625. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

14.9.2.1.155 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register (Offset = 22314h) [reset = 1E0000h]

Register Description: Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

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Table 14-18626. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2314h

Figure 14-6152. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		TS_SEQ_ID_OFFSET					
NONE		R/W					
0h		1Eh					
15	14	13	12	11	10	9	8
TS_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LTYPE1							
R/W							
0h							

Table 14-18628. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6h.
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1. This is the port's time sync LTYPE1 value.

14.9.2.1.156 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register (Offset = 22318h) [reset = 0h]

Register Description: Enet Port N Time Sync VLAN2 and VLAN2

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Table 14-18629. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2318h

Figure 14-6153. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
TS_VLAN_LTYPE2							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_VLAN_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1							
R/W							
0h							

Table 14-18631. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for the port TX and RX time sync decode.
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for the port TX and RX time sync decode.

14.9.2.1.157 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register (Offset = 2231Ch) [reset = 0h]

Register Description: Enet Port N Time Sync Control and LTYPE 2

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Table 14-18632. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 231Ch

Figure 14-6154. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_LTYPE2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_LTYPE2							
R/W							
0h							

Table 14-18634. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable 0h Unicast disabled 1h Unicast enabled
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable 0h TTL must be 1h 1h TTL may be any value
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable 0h Disabled 1h Destination port number (decimal) 320 is enabled
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable 0h Disabled 1h Destination port number (decimal) 319 is enabled

Table 14-18634. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.132 is enabled
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.131 is enabled
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.130 is enabled
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.129 is enabled
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable 0h Disabled 1h Destination port number (decimal) 224.0.0.107 is enabled
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2. This is the time sync LTYPE1 value for port 1.

14.9.2.1.158 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register (Offset = 22320h) [reset = 40000h]

Register Description: Enet Port N Time Sync Control 2

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Table 14-18635. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2320h

Figure 14-6155. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TS_DOMAIN_OFFSET					
NONE		R/W					
0h		4h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_MCAST_TYPE_EN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_MCAST_TYPE_EN							
R/W							
0h							

Table 14-18637. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

14.9.2.1.159 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register (Offset = 22330h) [reset = 0h]

Register Description: Enet Port N Mac Control

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Table 14-18638. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2330h

Figure 14-6156. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							RX_CMF_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED	
R/W	NONE		R/W	R/W	R/W	NONE	
0h	0h		0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18640. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the CPSW_PN_MAC_CONTROL_REG_k register, regardless of the value of [24] RX_CMF_EN bit. Frames transferred to memory due to [24] RX_CMF_EN will have the control bit set in their EOP buffer descriptor. 0h `MAC control frames are filtered (but acted upon if enabled).` 1h `MAC control frames are transferred to memory.`

Table 14-18640. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable. Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to CPSW_PN_MAC_CONTROL_REG_k[23] RX_CSF_EN will have the fragment or undersized bit set in their receive footer. Fragments are short frames that contain CRC/align/ code errors and undersized are short frames without errors. 0h Short frames are filtered. 1h Short frames are transferred to memory.
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable. Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is not set. 0h Frames containing errors are filtered. 1h Frames containing errors are transferred to memory.
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable When set this bit limits the number of short gap packets transmitted to 100ppm. The TX_SHORT_GAP_ENABLE bit must also be set. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable. Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the [4] TX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG_k register.
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable. Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the CPSW_PN_MAC_CONTROL_REG_k[3] RX_FLOW_EN bit in this register.
18	EXT_EN	R/W	0h	External Control Enable. Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the [0] FULLDUPLEX and [7] GIG bits in the CPSW_PN_MAC_CONTROL_REG_k register. The [0] FULLDUPLEX bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	R/W	0h	Gigabit Mode Force. This bit is used to force the Ethernet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.
16	RESERVED	NONE	0h	Reserved
15	IFCTL_A	R/W	0h	Determines the RMII link speed. 0h 10Mbps operation 0h 100Mbps operation
14:13	RESERVED	NONE	0h	Reserved
12	CRC_TYPE	R/W	0h	Port CRC Type. 0h Ethernet CRC 1h Castagnoli CRC
11	CMD_IDLE	R/W	0h	Command Idle. 0h Idle not commanded 1h Idle Commanded (read bit [31] IDLE in CPSW_PN_MAC_STATUS_REG_k register)

Table 14-18640. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable. 0h Transmit with a short IPG is disabled 1h Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.
9:8	RESERVED	NONE	0h	Reserved
7	GIG	R/W	0h	Gigabit Mode. 0h 10/100 mode 1h Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit.
6	TX_PACE	R/W	0h	Transmit Pacing Enable 0h Transmit Pacing Disabled 1h Transmit Pacing Enabled
5	GMII_EN	R/W	0h	GMII Enable. 0h GMII RX and TX held in reset. 1h GMII RX and TX released from reset.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0h Transmit Flow Control Disabled. Full-duplex mode - Incoming pause frames are not acted upon. 1h Transmit Flow Control Enabled. Full-duplex mode - Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable. 0h Receive Flow Control Disabled Half-duplex mode - No flow control generated collisions are sent. Full-duplex mode - No outgoing pause frames are sent. 1h Receive Flow Control Enabled Half-duplex mode - Collisions are initiated when receive flow control is triggered. Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode. This bit must be set to allow writes to the CPSW_PN_MAC_BOFFTEST_REG_k and CPSW_PN_MAC_RX_PAUSETIMER_REG_k registers.
1	LOOPBACK	R/W	0h	Loop Back Mode. Loopback mode forces internal fullduplex mode regardless of whether the CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX bit is set or not. The [1] LOOPBACK bit should be changed only when [5] GMII_EN is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS). 0h Not looped back mode 1h Loop Back mode enabled
0	FULLDUPLEX	R/W	0h	Full Duplex mode. Gigabit mode forces fullduplex mode regardless of whether the [0] FULLDUPLEX bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit 0h Half duplex mode 1h Full duplex mode

14.9.2.1.160 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register (Offset = 22334h) [reset = F0000000h]

Register Description: Enet Port N Mac Status

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Table 14-18641. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2334h

Figure 14-6157. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	P_IDLE	MAC_TX_IDLE	TORF	TORF_PRI		
R	R	R	R	R	R		
1h	1h	1h	1h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_PFC_FLOW_ACT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_PFC_FLOW_ACT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
NONE	R	R	R	R	NONE	R	R
2h	0h	0h	0h	0h	1h	0h	0h

Table 14-18643. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description

31	IDLE	R	1h	Enet IDLE. The Ethernet port (express and prempt) are in the Idle state (valid after an Idle command)
				`0h The port is not in the Idle state.`
				`1h The port is in the Idle state.`

30	E_IDLE	R	1h	Express MAC is Idle.
29	P_IDLE	R	1h	Prempt MAC is Idle.
28	MAC_TX_IDLE	R	1h	Mac Transmit Idle. Both Prempt and Express MAC Transmit are in Idle state. The transmit clock must be running for this to go idle.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 7h to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15:8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	NONE	2h	Reserved

Table 14-18643. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[19] EXT_RX_FLOW_EN input bit.
5	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[20] EXT_TX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG. This is the value of the [4] EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Fullduplex. This is the value of the [3] EXT_FULLDUPLEX input bit.
2	RESERVED	NONE	1h	Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

14.9.2.1.161 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register (Offset = 22338h) [reset = 0h]

Register Description: Enet Port N Mac Soft Reset

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Table 14-18644. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2338h

Figure 14-6158. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-18646. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Software reset. Writing a 1h to this bit causes the Ethernet Mac logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a 1h is read, the reset has not yet occurred. If a 0h is read then reset has occurred.

14.9.2.1.162 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register (Offset = 2233Ch) [reset = 0h]

Register Description: Enet Port N Mac Backoff Test

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Table 14-18647. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 233Ch

Figure 14-6159. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
NONE	R/W					R/W	
0h	0h					0h	
23	22	21	20	19	18	17	16
RNDNUM							
R/W							
0h							
15	14	13	12	11	10	9	8
COLL_COUNT				RESERVED		TX_BACKOFF	
R				NONE		R	
0h				0h		0h	
7	6	5	4	3	2	1	0
TX_BACKOFF							
R							
0h							

Table 14-18649. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:26	PACEVAL	R/W	0h	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce 'capture' effects improving overall network bandwidth.
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when CPSW_PN_MAC_CONTROL_REG_k[2] MTEST bit has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15:12	COLL_COUNT	R	0h	Collision Count.
11:10	RESERVED	NONE	0h	Reserved

Table 14-18649. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	TX_BACKOFF	R	0h	Backoff Count. This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.

14.9.2.1.163 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 22340h) [reset = 0h]

Register Description: Enet Port N 802.3 Receive Pause Timer

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Table 14-18650. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2340h

Figure 14-6160. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-18652. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.9.2.1.164 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Register (Offset = 22350h + formula) [reset = 0h]

Register Description: Enet Port N PFC Priority P Rx Pause Timer

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18653. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2350h + formula

Figure 14-6161. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-18655. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	Rx Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

14.9.2.1.165 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 22370h) [reset = 0h]

Register Description: Enet Port N 802.3 Tx Pause Timer

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Table 14-18656. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2370h

Figure 14-6162. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-18658. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.9.2.1.166 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Register (Offset = 22380h + formula) [reset = 0h]

Register Description: Enet Port N PFC Priority P Tx Pause Timer

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18659. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 2380h + formula

Figure 14-6163. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-18661. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	PFC Tx 'y' Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

14.9.2.1.167 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register (Offset = 223A0h) [reset = 0h]

Register Description: Enet Port N Emulation Control

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Table 14-18662. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23A0h

Figure 14-6164. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-18664. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.9.2.1.168 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register (Offset = 223A4h) [reset = Ch]

Register Description: Enet Port N Tx Inter Packet Gap

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Table 14-18665. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23A4h

Figure 14-6165. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_GAP							
R/W							
Ch							
7	6	5	4	3	2	1	0
TX_GAP							
R/W							
Ch							

Table 14-18667. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap GMII modes - This is the default gap value and only bits [8-0] are used. This can be increased from 12 to increase the gap between packets. XGMII mode - In 10 Gigabit mode this is the short gap rate and should be changed to 5000 (1388h) to get approximately 200ppm faster when short gap is triggered and enabled.

14.9.2.1.169 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register (Offset = 223A8h) [reset = 204h]

Register Description: Enet Port N Port Configuration

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Table 14-18668. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23A8h

Figure 14-6166. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						IET	XGMII
NONE						R	R
0h						1h	0h
7	6	5	4	3	2	1	0
INTERVLAN_ROUTES							
R							
4h							

Table 14-18670. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	IET	R	1h	Interspersed Express Traffic (IET) is supported on this port when read high.
8	XGMII	R	0h	XGMII is supported on this port when set.
7:0	INTERVLAN_ROUTES	R	4h	This is the number of InterVLAN routes supported on this port (egress).

14.9.2.1.170 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 223ACh) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN Operation Pointer

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Table 14-18671. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23ACh

Figure 14-6167. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					POINTER		
NONE					R/W		
0h					0h		

Table 14-18673. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

14.9.2.1.171 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register (Offset = 223B0h) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN A

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Table 14-18674. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23B0h

Figure 14-6168. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24
DA_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
DA_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_47_40							
R/W							
0h							

Table 14-18676. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16 - DA byte 4 on wire
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24 - DA byte 3 on wire
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32 - DA byte 2 on wire
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40 - DA byte 1 on wire

14.9.2.1.172 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register (Offset = 223B4h) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN B

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Table 14-18677. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23B4h

Figure 14-6169. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Name Register

31	30	29	28	27	26	25	24
SA_39_32							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_47_40							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_15_8							
R/W							
0h							

Table 14-18679. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32 - SA byte 2 on wire
23:16	SA_47_40	R/W	0h	Source Address bits 47:40 - SA byte 1 on wire
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0 - DA byte 6 on wire
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8 - DA byte 5 on wire

14.9.2.1.173 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register (Offset = 223B8h) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN C

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Table 14-18680. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23B8h

Figure 14-6170. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24
SA_7_0							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_15_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SA_23_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SA_31_24							
R/W							
0h							

Table 14-18682. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0 - DA byte 6 on wire
23:16	SA_15_8	R/W	0h	Source Address bits 15:8 - DA byte 5 on wire
15:8	SA_23_16	R/W	0h	Source Address bits 23:16 - DA byte 4 on wire
7:0	SA_31_24	R/W	0h	Source Address bits 31:24 - DA byte 3 on wire

14.9.2.1.174 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register (Offset = 223BCh) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN D

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Table 14-18683. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23BCh

Figure 14-6171. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VID							
R/W							
0h							

Table 14-18685. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

14.9.2.1.175 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register (Offset = 223C0h) [reset = 0h]

Register Description: Enet Port N Cut Thru Priority Enable

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Table 14-18686. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23C0h

Figure 14-6172. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_PRI_CUT_THRU_EN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI_CUT_THRU_EN							
R/W							
0h							

Table 14-18688. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RX_PRI_CUT_THRU_EN	R/W	0h	Receive Cut Thru Priority Enable
7:0	TX_PRI_CUT_THRU_EN	R/W	0h	Transmit Cut Thru Priority Enable

14.9.2.1.176 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register (Offset = 223C4h) [reset = 0h]

Register Description: Enet Port Speed

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Table 14-18689. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 23C4h

Figure 14-6173. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PORT_SPEED_CHANGED	RESERVED			
NONE			R	NONE			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PORT_AUTO_SPEED				RESERVED			PORT_SPEED_AUTO_EN
R				NONE			R/W
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PORT_SPEED_MANUAL			
NONE				R/W			
0h				0h			

Table 14-18691. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	PORT_SPEED_CHANGED	R	0h	Port Speed Changed
19:16	RESERVED	NONE	0h	Reserved
15:12	PORT_AUTO_SPEED	R	0h	Detected Auto Speed
11:9	RESERVED	NONE	0h	Reserved
8	PORT_SPEED_AUTO_EN	R/W	0h	Automatic Port Speed Enable
7:4	RESERVED	NONE	0h	Reserved
3:0	PORT_SPEED_MANUAL	R/W	0h	Manual Port Speed

14.9.2.1.177 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register (Offset = 23000h) [reset = 0h]

Register Description: Reserved

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Table 14-18692. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3000h

Figure 14-6174. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-18694. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved register for memory map alignment

14.9.2.1.178 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register (Offset = 23004h) [reset = 0h]

Register Description: Enet Port N Control

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Table 14-18695. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3004h

Figure 14-6175. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						EST_PORT_EN	IET_PORT_EN
NONE						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_ECC_ERR_EN	TX_ECC_ERR_EN	TX_CUT_IET_HOLD_DIS	TX_LPI_CLKSTOP_EN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
NONE					R/W	R/W	NONE
0h					0h	0h	0h

Table 14-18697. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable. 0h `EST is disabled on the port` 1h `EST is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.`
16	IET_PORT_EN	R/W	0h	Intersperced Express Traffic (IET) Port Enable. 0h `IET is disabled on the port` 1h `IET is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.`
15	RX_ECC_ERR_EN	R/W	0h	Port N receive ECC Error Enable. This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port N transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations

Table 14-18697. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TX_CUT_IET_HOLD_DIS	R/W	0h	Port N transmit IET hold due to cut-thru disable 0h `Cut-thru packets to the port will cause premptable traffic to be prempted as early as possible minimizing cut-thru latency` 1h `Cut-thru packets to the port will be prempted as usual by the express MAC`
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable. When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11:3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	IPV6 DSCP enable 0h `IPV6 DSCP priority mapping is disabled` 1h `IPV6 DSCP priority mapping is enabled`
1	DSCP_IPV4_EN	R/W	0h	IPV4 DSCP enable 0h `IPV4 DSCP priority mapping is disabled` 1h `IPV4 DSCP priority mapping is enabled`
0	RESERVED	NONE	0h	Reserved

14.9.2.1.179 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register (Offset = 23008h) [reset = 1004h]

Register Description: Enet Port N FIFO Max Blocks

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Table 14-18698. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3008h

Figure 14-6176. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_MAX_BLKS							
R/W							
10h							
7	6	5	4	3	2	1	0
RX_MAX_BLKS							
R/W							
4h							

Table 14-18700. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit Max Blocks. The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive, when Fullduplex flow control is enabled (CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX = 1h) to allow for flow control runout.
7:0	RX_MAX_BLKS	R/W	4h	Receive Max Blocks. The maximum number of blocks allowed on the express and prempt receive FIFOs (transmit and receive FIFO's combined when fifo_oneram = 1)

14.9.2.1.180 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register (Offset = 23010h) [reset = 1h]

Register Description: Enet Port N FIFO Block Usage Count

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Table 14-18701. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3010h

Figure 14-6177. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		RX_BLK_CNT_P					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TX_BLK_CNT				
NONE			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RX_BLK_CNT_E					
NONE		R					
0h		1h					

Table 14-18703. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO prempt receive queue. No blocks are allocated until the CPSW_CONTROL_REG[17] IET_ENABLE is set.
15:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage. This value is the number of blocks allocated to the port's FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO express receive queue.

14.9.2.1.181 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register (Offset = 23014h) [reset = 0h]

Register Description: Enet Port N VLAN

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Table 14-18704. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3014h

Figure 14-6178. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W			R/W	R/W			
0h			0h	0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W							
0h							

Table 14-18706. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.9.2.1.182 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register (Offset = 23018h) [reset = 76543210h]

Register Description: Enet Port N Tx Header Pri to Switch Pri Mapping

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Table 14-18707. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3018h

Figure 14-6179. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
aah	7h			55h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
2ah	5h			15h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
ah	3h			5h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
2h	1h			1h	0h		

Table 14-18709. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	aah	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	55h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	2ah	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	15h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	ah	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	5h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.

Table 14-18709. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	2h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	NONE	1h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.9.2.1.183 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register (Offset = 2301Ch) [reset = 9000h]

Register Description: Enet Port N Priority Control

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Table 14-18710. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 301Ch

Figure 14-6180. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24
TX_FLOW_PRI							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_FLOW_PRI							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_HOST_BLKS_REM				RESERVED			
R/W				NONE			
9h				0h			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-18712. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE	0h	Reserved

14.9.2.1.184 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register (Offset = 23020h) [reset = 76543210h]

Register Description: Enet Port N RX Pkt Pri to Header Pri Map

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Table 14-18713. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3020h

Figure 14-6181. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
aah	7h			55h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
2ah	5h			15h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
ah	3h			5h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
2h	1h			1h	0h		

Table 14-18715. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	aah	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	55h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	2ah	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	15h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	ah	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	5h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.

Table 14-18715. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	NONE	2h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	NONE	1h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.9.2.1.185 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register (Offset = 23024h) [reset = 5EEh]

Register Description: Enet Port N Receive Frame Max Length

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Table 14-18716. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3024h

Figure 14-6182. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		RX_MAXLEN					
NONE		R/W					
0h		5EEh					
7	6	5	4	3	2	1	0
RX_MAXLEN							
R/W							
5EEh							

Table 14-18718. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).

14.9.2.1.186 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register (Offset = 23028h) [reset = 1245678h]

Register Description: Enet Port N Transmit Block Sub Per Priority

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Table 14-18719. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3028h

Figure 14-6183. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-18721. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

14.9.2.1.187 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register (Offset = 23030h) [reset = 0h]

Register Description: Enet Port N EEE Idle to LPI counter

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Table 14-18722. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3030h

Figure 14-6184. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18724. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value

14.9.2.1.188 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register (Offset = 23034h) [reset = 0h]

Register Description: Enet Port N EEE LPI to wake counter

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Table 14-18725. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3034h

Figure 14-6185. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18727. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value

14.9.2.1.189 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register (Offset = 23038h) [reset = 62h]

Register Description: Enet Port N EEE status

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Table 14-18728. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3038h

Figure 14-6186. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	1h	0h

Table 14-18730. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.9.2.1.190 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register (Offset = 23040h) [reset = 8h]

Register Description: Enet Port N IET Control

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Table 14-18731. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3040h

Figure 14-6187. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_PREMPT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					MAC_ADDFRAGSIZE		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				MAC_LINKFAIL	MAC_DISABLEVERIFY	MAC_HOLD	MAC_PENABLE
NONE				R/W	R/W	R/W	R/W
0h				1h	0h	0h	0h

Table 14-18733. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAC_PREMPT	R/W	0h	Mac Preempt Queue - Indicates which transmit FIFO queues are sent to the preempt MAC. Bit 0 indicates queue zero, bit 1 queue 1 and so on. Packets will be sent to the preempt MAC only when MAC_PENABLE is set, and when MAC_VERIFIED (from CPSW_PN_IET_STATUS_REG_k) or MAC_DISABLEVERIFY is set, and when IET_PORT_EN is set.
15:11	RESERVED	NONE	0h	Reserved
10:8	MAC_ADDFRAGSIZE	R/W	0h	Mac Fragment Size - An integer in the range 0:7 indicating, as a multiple of 64, the minimum additional length for nonfinal mPackets. 0 64 1 128 2 81 3 256 4 320 5 384 6 448 7 512
7:4	RESERVED	NONE	0h	Reserved

Table 14-18733. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MAC_LINKFAIL	R/W	1h	Mac Link Fail - Link Fail Indicator to reset the verify state machine. This bit is reset high. Verify and response frames will be sent/allowed when this bit is cleared.
2	MAC_DISABLEVERIFY	R/W	0h	Mac Disable Verify - Disables verification on the port when set. If this bit is set then packets will be sent to the preempt Mac when MAC_PENABLE is set (This is a forced mode with no IET verification).
1	MAC_HOLD	R/W	0h	Mac Hold - Hold Preemption on the port.
0	MAC_PENABLE	R/W	0h	Mac Preemption Enable - Port Preemption Enable. This takes effect only when IET_PORT_EN is set.

14.9.2.1.191 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register (Offset = 23044h) [reset = 0h]

Register Description: Enet Port N IET Status

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Table 14-18734. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3044h

Figure 14-6188. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MAC_VERIFY_ERR	MAC_RESPOND_ERR	MAC_VERIFY_FAIL	MAC_VERIFIED
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-18736. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MAC_VERIFY_ERR	R	0h	Mac Received Verify Packet with Errors - Set when a verify packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
2	MAC_RESPOND_ERR	R	0h	Mac Received Respond Packet with Errors - Set when a respond packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
1	MAC_VERIFY_FAIL	R	0h	Mac Verification Failed - Indication that verification was unsuccessful.
0	MAC_VERIFIED	R	0h	Mac Verified - Indication that verification was successful.

14.9.2.1.192 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register (Offset = 23048h) [reset = 1312D0h]

Register Description: Enet Port N IET VERIFY

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Table 14-18737. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3048h

Figure 14-6189. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_VERIFY_CNT							
R/W							
1312D0h							
15	14	13	12	11	10	9	8
MAC_VERIFY_CNT							
R/W							
1312D0h							
7	6	5	4	3	2	1	0
MAC_VERIFY_CNT							
R/W							
1312D0h							

Table 14-18739. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MAC_VERIFY_CNT	R/W	1312D0h	Mac Verify Timeout Count - The number of wireside clocks contained in the verify timeout counter. The default is 0x1312D0 (10ms at 125MHz in gig mode).

14.9.2.1.193 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register (Offset = 23050h) [reset = FF00h]

Register Description: Enet Port N FIFO STATUS

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Table 14-18740. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3050h

Figure 14-6190. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE					R	R	R
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TX_E_MAC_ALLOW							
R							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI_ACTIVE							
R							
0h							

Table 14-18742. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	EST_BUFACT	R	0h	EST RAM active buffer. Indicates the active 64-word fetch buffer when CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared to zero. Indicates the fetch RAM address MSB when bit [0] EST_ONEBUF is set to one.
17	EST_ADD_ERR	R	0h	EST Address Error. Indicates that the fetch RAM was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error. Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15:8	TX_E_MAC_ALLOW	R	FFh	EST transmit MAC allow. Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the prempt queue).
7:0	TX_PRI_ACTIVE	R	0h	EST Transmit Priority Active. Bus that indicates which priorities have packets (non-empty) at the time of the register read.

14.9.2.1.194 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register (Offset = 23060h) [reset = 0h]

Register Description: Enet Port N EST CONTROL

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Table 14-18743. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3060h

Figure 14-6191. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">EST_FILL_MARGIN</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">EST_FILL_MARGIN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">EST_PREMPT_COMP</td><td>EST_FILL_EN</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">EST_TS_PRI</td><td>EST_TS_ONEPRI</td><td>EST_TS_FIRST</td><td>EST_TS_EN</td><td>EST_BUFSEL</td><td>EST_ONEBUF</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-18745. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin. Sets the fill margin required to ensure that the Ethernet wire is clear (including IPG) so that the timed EST express packet can egress at the required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended.
15:9	EST_PREMPT_COMP	R/W	0h	EST Prempt Comparison Value. When the count in a zero allow is less than or equal to this value in bytes (times 8), prempt packets are cleared from the wire. This is the prempt clear margin value.
8	EST_FILL_EN	R/W	0h	EST Fill Enable. Enable EST fill mode.
7:5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority. Selects the express priority that timestamp(s) will be generated on when CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI bit is set.
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority. When set, timestamp only enabled packets on the express priority selected by CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI bit field. When cleared to zero, express packet selection for timestamp is independent of priority.

Table 14-18745. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only. Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI is also set then the timestamp is generated only on the first packet on CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI).
2	EST_TS_EN	R/W	0h	EST Timestamp Enable. Enable express timestamps (when CPSW_CONTROL_REG[18] EST_ENABLE and CPSW_PN_CONTROL_REG_k[17] EST_PORT_EN bits are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select. If CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the CPSW_PN_FIFO_STATUS_REG_k register, bit [18] EST_BUFACT.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer. When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The CPSW_PN_EST_CONTROL_REG_k[1] EST_BUFSEL bit selects the buffer to be used when bit [0] EST_ONEBUF is cleared to zero.

14.9.2.1.195 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register (Offset = 23120h + formula) [reset = 0h]

Register Description: Enet Port N Receive IPV4/IPV6 DSCP Map M

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18746. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3120h + formula

Figure 14-6192. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-18748. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved

Table 14-18748. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.9.2.1.196 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Register (Offset = 23140h + formula) [reset = 0h]

Register Description: Enet Port N Rx Priority P Committed Information Rate Value

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18749. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3140h + formula

Figure 14-6193. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_CIR							
R/W							
0h							

Table 14-18751. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

14.9.2.1.197 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Register (Offset = 23160h + formula) [reset = 0h]

Register Description: Enet Port N Rx Priority P Excess Informatoin Rate Value

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18752. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3160h + formula

Figure 14-6194. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 14-18754. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

14.9.2.1.198 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register (Offset = 23180h) [reset = 1F1F1F1Fh]

Register Description: Enet Port N Tx PFC Destination Threshold Set Low

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Table 14-18755. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3180h

Figure 14-6195. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-18757. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.2.1.199 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register (Offset = 23184h) [reset = 1F1F1F1Fh]

Register Description: Enet Port N Tx PFC Destination Threshold Set High

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Table 14-18758. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3184h

Figure 14-6196. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-18760. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.2.1.200 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 23188h) [reset = 0h]

Register Description: Enet Port N Tx PFC Destination Threshold Clr Low

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Table 14-18761. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3188h

Figure 14-6197. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-18763. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.2.1.201 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 2318Ch) [reset = 0h]

Register Description: Enet Port N Tx PFC Destination Threshold Clr High

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Table 14-18764. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 318Ch

Figure 14-6198. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-18766. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.2.1.202 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 23190h) [reset = 1F1F1F1Fh]

Register Description: Enet Port N Tx PFC Global Buffer Threshold Set Low

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Table 14-18767. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3190h

Figure 14-6199. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-18769. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.9.2.1.203 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 23194h) [reset = 1F1F1F1Fh]

Register Description: Enet Port N Tx PFC Global Buffer Threshold Set High

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Table 14-18770. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3194h

Figure 14-6200. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-18772. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.9.2.1.204 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 23198h) [reset = 0h]

Register Description: Enet Port N Tx PFC Global Buffer Threshold Clr Low

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Table 14-18773. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3198h

Figure 14-6201. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-18775. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.9.2.1.205 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2319Ch) [reset = 0h]

Register Description: Enet Port N Tx PFC Global Buffer Threshold Clr High

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Table 14-18776. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 319Ch

Figure 14-6202. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-18778. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.9.2.1.206 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 23300h) [reset = 0h]

Register Description: Enet Port N Tx Destination Out Flow Add Values Low

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Table 14-18779. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3300h

Figure 14-6203. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-18781. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

14.9.2.1.207 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 23304h) [reset = 0h]

Register Description: Enet Port N Tx Destination Out Flow Add Values High

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Table 14-18782. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3304h

Figure 14-6204. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-18784. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

14.9.2.1.208 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register (Offset = 23308h) [reset = 0h]

Register Description: Enet Port N Tx Pause Frame Source Address Low

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Table 14-18785. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3308h

Figure 14-6205. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_15_8							
R/W							
0h							

Table 14-18787. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

14.9.2.1.209 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register (Offset = 2330Ch) [reset = 0h]

Register Description: Enet Port N Tx Pause Frame Source Address High

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Table 14-18788. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 330Ch

Figure 14-6206. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24
MACSRCADDR_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
MACSRCADDR_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_47_40							
R/W							
0h							

Table 14-18790. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

14.9.2.1.210 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register (Offset = 23310h) [reset = 0h]

Register Description: Enet Port N Time Sync Control

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Table 14-18791. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3310h

Figure 14-6207. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_MSG_TYPE_EN							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18793. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
15:12	RESERVED	NONE	0h	Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable

Table 14-18793. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

14.9.2.1.211 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register (Offset = 23314h) [reset = 1E0000h]

Register Description: Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

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Table 14-18794. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3314h

Figure 14-6208. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		TS_SEQ_ID_OFFSET					
NONE		R/W					
0h		1Eh					
15	14	13	12	11	10	9	8
TS_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LTYPE1							
R/W							
0h							

Table 14-18796. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6h.
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1. This is the port's time sync LTYPE1 value.

14.9.2.1.212 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register (Offset = 23318h) [reset = 0h]

Register Description: Enet Port N Time Sync VLAN2 and VLAN2

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Table 14-18797. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3318h

Figure 14-6209. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
TS_VLAN_LTYPE2							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_VLAN_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1							
R/W							
0h							

Table 14-18799. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for the port TX and RX time sync decode.
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for the port TX and RX time sync decode.

14.9.2.1.213 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register (Offset = 2331Ch) [reset = 0h]

Register Description: Enet Port N Time Sync Control and LTYPE 2

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Table 14-18800. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 331Ch

Figure 14-6210. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TS_LTYPE2							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LTYPE2							
R/W							
0h							

Table 14-18802. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable 0h Unicast disabled 1h Unicast enabled
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable 0h TTL must be 1h 1h TTL may be any value
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable 0h Disabled 1h Destination port number (decimal) 320 is enabled
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable 0h Disabled 1h Destination port number (decimal) 319 is enabled

Table 14-18802. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.132 is enabled
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.131 is enabled
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.130 is enabled
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.129 is enabled
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable 0h Disabled 1h Destination port number (decimal) 224.0.0.107 is enabled
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2. This is the time sync LTYPE1 value for port 1.

14.9.2.1.214 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register (Offset = 23320h) [reset = 40000h]

Register Description: Enet Port N Time Sync Control 2

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Table 14-18803. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3320h

Figure 14-6211. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TS_DOMAIN_OFFSET					
NONE		R/W					
0h		4h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_MCAST_TYPE_EN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_MCAST_TYPE_EN							
R/W							
0h							

Table 14-18805. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

14.9.2.1.215 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register (Offset = 23330h) [reset = 0h]

Register Description: Enet Port N Mac Control

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Table 14-18806. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3330h

Figure 14-6212. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							RX_CMF_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED	
R/W	NONE		R/W	R/W	R/W	NONE	
0h	0h		0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-18808. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the CPSW_PN_MAC_CONTROL_REG_k register, regardless of the value of [24] RX_CMF_EN bit. Frames transferred to memory due to [24] RX_CMF_EN will have the control bit set in their EOP buffer descriptor. 0h `MAC control frames are filtered (but acted upon if enabled).` 1h `MAC control frames are transferred to memory.`

Table 14-18808. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable. Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to CPSW_PN_MAC_CONTROL_REG_k[23] RX_CSF_EN will have the fragment or undersized bit set in their receive footer. Fragments are short frames that contain CRC/align/ code errors and undersized are short frames without errors. 0h Short frames are filtered. 1h Short frames are transferred to memory.
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable. Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is not set. 0h Frames containing errors are filtered. 1h Frames containing errors are transferred to memory.
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable When set this bit limits the number of short gap packets transmitted to 100ppm. The TX_SHORT_GAP_ENABLE bit must also be set. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable. Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the [4] TX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG_k register.
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable. Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the CPSW_PN_MAC_CONTROL_REG_k[3] RX_FLOW_EN bit in this register.
18	EXT_EN	R/W	0h	External Control Enable. Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the [0] FULLDUPLEX and [7] GIG bits in the CPSW_PN_MAC_CONTROL_REG_k register. The [0] FULLDUPLEX bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	R/W	0h	Gigabit Mode Force. This bit is used to force the Ethernet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.
16	RESERVED	NONE	0h	Reserved
15	IFCTL_A	R/W	0h	Determines the RMII link speed. 0h 10Mbps operation 0h 100Mbps operation
14:13	RESERVED	NONE	0h	Reserved
12	CRC_TYPE	R/W	0h	Port CRC Type. 0h Ethernet CRC 1h Castagnoli CRC
11	CMD_IDLE	R/W	0h	Command Idle. 0h Idle not commanded 1h Idle Commanded (read bit [31] IDLE in CPSW_PN_MAC_STATUS_REG_k register)

Table 14-18808. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable. 0h Transmit with a short IPG is disabled 1h Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.
9:8	RESERVED	NONE	0h	Reserved
7	GIG	R/W	0h	Gigabit Mode. 0h 10/100 mode 1h Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit.
6	TX_PACE	R/W	0h	Transmit Pacing Enable 0h Transmit Pacing Disabled 1h Transmit Pacing Enabled
5	GMII_EN	R/W	0h	GMII Enable. 0h GMII RX and TX held in reset. 1h GMII RX and TX released from reset.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0h Transmit Flow Control Disabled. Full-duplex mode - Incoming pause frames are not acted upon. 1h Transmit Flow Control Enabled. Full-duplex mode - Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable. 0h Receive Flow Control Disabled Half-duplex mode - No flow control generated collisions are sent. Full-duplex mode - No outgoing pause frames are sent. 1h Receive Flow Control Enabled Half-duplex mode - Collisions are initiated when receive flow control is triggered. Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode. This bit must be set to allow writes to the CPSW_PN_MAC_BOFFTEST_REG_k and CPSW_PN_MAC_RX_PAUSETIMER_REG_k registers.
1	LOOPBACK	R/W	0h	Loop Back Mode. Loopback mode forces internal fullduplex mode regardless of whether the CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX bit is set or not. The [1] LOOPBACK bit should be changed only when [5] GMII_EN is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS). 0h Not looped back mode 1h Loop Back mode enabled
0	FULLDUPLEX	R/W	0h	Full Duplex mode. Gigabit mode forces fullduplex mode regardless of whether the [0] FULLDUPLEX bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit 0h Half duplex mode 1h Full duplex mode

14.9.2.1.216 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register (Offset = 23334h) [reset = F0000000h]

Register Description: Enet Port N Mac Status

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Table 14-18809. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3334h

Figure 14-6213. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	P_IDLE	MAC_TX_IDLE	TORF	TORF_PRI		
R	R	R	R	R	R		
1h	1h	1h	1h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_PFC_FLOW_ACT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_PFC_FLOW_ACT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
NONE	R	R	R	R	NONE	R	R
2h	0h	0h	0h	0h	1h	0h	0h

Table 14-18811. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description

31	IDLE	R	1h	Enet IDLE. The Ethernet port (express and prempt) are in the Idle state (valid after an Idle command)
				`0h The port is not in the Idle state.`
				`1h The port is in the Idle state.`

30	E_IDLE	R	1h	Express MAC is Idle.
29	P_IDLE	R	1h	Prempt MAC is Idle.
28	MAC_TX_IDLE	R	1h	Mac Transmit Idle. Both Prempt and Express MAC Transmit are in Idle state. The transmit clock must be running for this to go idle.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 7h to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15:8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	NONE	2h	Reserved

Table 14-18811. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[19] EXT_RX_FLOW_EN input bit.
5	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[20] EXT_TX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG. This is the value of the [4] EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Fullduplex. This is the value of the [3] EXT_FULLDUPLEX input bit.
2	RESERVED	NONE	1h	Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

14.9.2.1.217 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register (Offset = 23338h) [reset = 0h]

Register Description: Enet Port N Mac Soft Reset

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Table 14-18812. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3338h

Figure 14-6214. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFT_RESET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-18814. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Software reset. Writing a 1h to this bit causes the Ethernet Mac logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a 1h is read, the reset has not yet occurred. If a 0h is read then reset has occurred.

14.9.2.1.218 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register (Offset = 2333Ch) [reset = 0h]

Register Description: Enet Port N Mac Backoff Test

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Table 14-18815. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 333Ch

Figure 14-6215. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
NONE	R/W					R/W	
0h	0h					0h	
23	22	21	20	19	18	17	16
RNDNUM							
R/W							
0h							
15	14	13	12	11	10	9	8
COLL_COUNT				RESERVED		TX_BACKOFF	
R				NONE		R	
0h				0h		0h	
7	6	5	4	3	2	1	0
TX_BACKOFF							
R							
0h							

Table 14-18817. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:26	PACEVAL	R/W	0h	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce 'capture' effects improving overall network bandwidth.
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when CPSW_PN_MAC_CONTROL_REG_k[2] MTEST bit has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15:12	COLL_COUNT	R	0h	Collision Count.
11:10	RESERVED	NONE	0h	Reserved

Table 14-18817. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	TX_BACKOFF	R	0h	Backoff Count. This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.

14.9.2.1.219 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 23340h) [reset = 0h]

Register Description: Enet Port N 802.3 Receive Pause Timer

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Table 14-18818. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3340h

Figure 14-6216. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-18820. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.9.2.1.220 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Register (Offset = 23350h + formula) [reset = 0h]

Register Description: Enet Port N PFC Priority P Rx Pause Timer

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18821. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3350h + formula

Figure 14-6217. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-18823. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	Rx Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

14.9.2.1.221 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 23370h) [reset = 0h]

Register Description: Enet Port N 802.3 Tx Pause Timer

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Table 14-18824. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3370h

Figure 14-6218. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-18826. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.9.2.1.222 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Register (Offset = 23380h + formula) [reset = 0h]

Register Description: Enet Port N PFC Priority P Tx Pause Timer

Formula = (j * 4h); where j = 0 to 7d

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Table 14-18827. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 3380h + formula

Figure 14-6219. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-18829. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	PFC Tx 'y' Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

14.9.2.1.223 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register (Offset = 233A0h) [reset = 0h]

Register Description: Enet Port N Emulation Control

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Table 14-18830. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33A0h

Figure 14-6220. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>SOFT</td><td>FREE</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-18832. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.9.2.1.224 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register (Offset = 233A4h) [reset = Ch]

Register Description: Enet Port N Tx Inter Packet Gap

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Table 14-18833. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33A4h

Figure 14-6221. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_GAP							
R/W							
Ch							
7	6	5	4	3	2	1	0
TX_GAP							
R/W							
Ch							

Table 14-18835. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap GMII modes - This is the default gap value and only bits [8-0] are used. This can be increased from 12 to increase the gap between packets. XGMII mode - In 10 Gigabit mode this is the short gap rate and should be changed to 5000 (1388h) to get approximately 200ppm faster when short gap is triggered and enabled.

14.9.2.1.225 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register (Offset = 233A8h) [reset = 204h]

Register Description: Enet Port N Port Configuration

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Table 14-18836. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33A8h

Figure 14-6222. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						IET	XGMII
NONE						R	R
0h						1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTERVLAN_ROUTES							
R							
4h							

Table 14-18838. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	IET	R	1h	Intersperced Express Traffic (IET) is supported on this port when read high.
8	XGMII	R	0h	XGMII is supported on this port when set.
7:0	INTERVLAN_ROUTES	R	4h	This is the number of InterVLAN routes supported on this port (egress).

14.9.2.1.226 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 233ACh) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN Operation Pointer

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Table 14-18839. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33ACh

Figure 14-6223. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					POINTER		
NONE					R/W		
0h					0h		

Table 14-18841. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

14.9.2.1.227 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register (Offset = 233B0h) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN A

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Table 14-18842. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33B0h

Figure 14-6224. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24
DA_23_16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DA_31_24							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DA_39_32							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DA_47_40							
R/W							
0h							

Table 14-18844. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16 - DA byte 4 on wire
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24 - DA byte 3 on wire
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32 - DA byte 2 on wire
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40 - DA byte 1 on wire

14.9.2.1.228 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register (Offset = 233B4h) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN B

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Table 14-18845. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33B4h

Figure 14-6225. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Name Register

31	30	29	28	27	26	25	24
SA_39_32							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_47_40							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_15_8							
R/W							
0h							

Table 14-18847. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32 - SA byte 2 on wire
23:16	SA_47_40	R/W	0h	Source Address bits 47:40 - SA byte 1 on wire
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0 - DA byte 6 on wire
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8 - DA byte 5 on wire

14.9.2.1.229 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register (Offset = 233B8h) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN C

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Table 14-18848. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33B8h

Figure 14-6226. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24
SA_7_0							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_15_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SA_23_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SA_31_24							
R/W							
0h							

Table 14-18850. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0 - DA byte 6 on wire
23:16	SA_15_8	R/W	0h	Source Address bits 15:8 - DA byte 5 on wire
15:8	SA_23_16	R/W	0h	Source Address bits 23:16 - DA byte 4 on wire
7:0	SA_31_24	R/W	0h	Source Address bits 31:24 - DA byte 3 on wire

14.9.2.1.230 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register (Offset = 233BCh) [reset = 0h]

Register Description: Enet Port N Tx Egress InterVLAN D

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Table 14-18851. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33BCh

Figure 14-6227. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
VID							
R/W							
0h							

Table 14-18853. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

14.9.2.1.231 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register (Offset = 233C0h) [reset = 0h]

Register Description: Enet Port N Cut Thru Priority Enable

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Table 14-18854. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33C0h

Figure 14-6228. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_PRI_CUT_THRU_EN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI_CUT_THRU_EN							
R/W							
0h							

Table 14-18856. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RX_PRI_CUT_THRU_EN	R/W	0h	Receive Cut Thru Priority Enable
7:0	TX_PRI_CUT_THRU_EN	R/W	0h	Transmit Cut Thru Priority Enable

14.9.2.1.232 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register (Offset = 233C4h) [reset = 0h]

Register Description: Enet Port Speed

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Table 14-18857. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0802 33C4h

Figure 14-6229. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>PORT_SPEED_CHANGED</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">PORT_AUTO_SPEED</td><td colspan="3">RESERVED</td><td>PORT_SPEED_AUTO_EN</td></tr>
<tr><td colspan="4">R</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PORT_SPEED_MANUAL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-18859. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	PORT_SPEED_CHANGED	R	0h	Port Speed Changed
19:16	RESERVED	NONE	0h	Reserved
15:12	PORT_AUTO_SPEED	R	0h	Detected Auto Speed
11:9	RESERVED	NONE	0h	Reserved
8	PORT_SPEED_AUTO_EN	R/W	0h	Automatic Port Speed Enable
7:4	RESERVED	NONE	0h	Reserved
3:0	PORT_SPEED_MANUAL	R/W	0h	Manual Port Speed

14.9.2.1.233 CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Register

CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Register (Offset = 32000h + formula) [reset = 0h]

Register Description: The Revision Register contains the ID and revision information.

Formula = (j * 4h); where j = 0 to 255d

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Table 14-18860. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 2000h + formula

Figure 14-6230. CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		LOC					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
LOC							
R/W							
0h							
7	6	5	4	3	2	1	0
LOC							
R/W							
0h							

Table 14-18862. CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	LOC	R/W	0h	RAM Location

14.9.2.1.234 CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Register (Offset = 3A000h + formula) [reset = 0h]

Register Description: Total number of good frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18863. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A000h + formula

Figure 14-6231. CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18865. CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames received

14.9.2.1.235 CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Register (Offset = 3A004h + formula) [reset = 0h]

Register Description: Total number of good broadcast frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18866. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A004h + formula

Figure 14-6232. CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18868. CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames received

14.9.2.1.236 CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Register (Offset = 3A008h + formula) [reset = 0h]

Register Description: Total number of good multicast frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18869. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A008h + formula

Figure 14-6233. CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18871. CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames received

14.9.2.1.237 CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Register (Offset = 3A00Ch + formula) [reset = 0h]

Register Description: Total number of pause frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18872. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A00Ch + formula

Figure 14-6234. CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18874. CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames received

14.9.2.1.238 CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Register (Offset = 3A010h + formula) [reset = 0h]

Register Description: Total number of CRC errors frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18875. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A010h + formula

Figure 14-6235. CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18877. CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of CRC errors frames received

14.9.2.1.239 CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Register (Offset = 3A014h + formula) [reset = 0h]

Register Description: Total number of alignment/code errors received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18878. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A014h + formula

Figure 14-6236. CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18880. CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of alignment/code errors received

14.9.2.1.240 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Register (Offset = 3A018h + formula) [reset = 0h]

Register Description: Total number of oversized frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18881. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A018h + formula

Figure 14-6237. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18883. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of oversized frames received

14.9.2.1.241 CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Register (Offset = 3A01Ch + formula) [reset = 0h]

Register Description: Total number of jabber frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18884. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A01Ch + formula

Figure 14-6238. CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18886. CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of jabber frames received

14.9.2.1.242 CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Register (Offset = 3A020h + formula) [reset = 0h]

Register Description: Total number of undersized frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18887. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A020h + formula

Figure 14-6239. CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18889. CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of undersized frames received

14.9.2.1.243 CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Register (Offset = 3A024h + formula) [reset = 0h]

Register Description: Total number of fragmented frames received

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18890. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A024h + formula

Figure 14-6240. CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18892. CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of fragmented frames received

14.9.2.1.244 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Register (Offset = 3A028h + formula) [reset = 0h]

Register Description: Total number of frames dropped by the ALE

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18893. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A028h + formula

Figure 14-6241. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18895. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames dropped by the ALE

14.9.2.1.245 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Register (Offset = 3A02Ch + formula) [reset = 0h]

Register Description: Total number of overrun frames dropped by the ALE

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18896. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A02Ch + formula

Figure 14-6242. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18898. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE

14.9.2.1.246 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Register (Offset = 3A030h + formula) [reset = 0h]

Register Description: Total number of received bytes in good frames

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18899. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A030h + formula

Figure 14-6243. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18901. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of received bytes in good frames

14.9.2.1.247 CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Register (Offset = 3A034h + formula) [reset = 0h]

Register Description: Total number of good frames transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18902. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A034h + formula

Figure 14-6244. CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18904. CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames transmitted

14.9.2.1.248 CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Register (Offset = 3A038h + formula) [reset = 0h]

Register Description: Total number of good broadcast frames transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18905. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A038h + formula

Figure 14-6245. CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18907. CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames transmitted

14.9.2.1.249 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Register (Offset = 3A03Ch + formula) [reset = 0h]

Register Description: Total number of good multicast frames transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18908. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A03Ch + formula

Figure 14-6246. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18910. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames transmitted

14.9.2.1.250 CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Register (Offset = 3A040h + formula) [reset = 0h]

Register Description: Total number of pause frames transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18911. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A040h + formula

Figure 14-6247. CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18913. CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames transmitted

14.9.2.1.251 CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Register (Offset = 3A044h + formula) [reset = 0h]

Register Description: Total number of deferred frames transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18914. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A044h + formula

Figure 14-6248. CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18916. CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of deferred frames transmitted

14.9.2.1.252 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Register (Offset = 3A048h + formula) [reset = 0h]

Register Description: Total number of transmitted frames experiencing a collision

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18917. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A048h + formula

Figure 14-6249. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18919. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a collision

14.9.2.1.253 CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Register (Offset = 3A04Ch + formula) [reset = 0h]

Register Description: Total number of transmitted frames experiencing a single collision

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18920. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A04Ch + formula

Figure 14-6250. CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18922. CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a single collision

14.9.2.1.254 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Register (Offset = 3A050h + formula) [reset = 0h]

Register Description: Total number of transmitted frames experiencing multiple collisions

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18923. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A050h + formula

Figure 14-6251. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18925. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing multiple collisions

14.9.2.1.255 CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Register (Offset = 3A054h + formula) [reset = 0h]

Register Description: Total number of transmitted frames abandoned due to excessive collisions

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18926. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A054h + formula

Figure 14-6252. CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18928. CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to excessive collisions

14.9.2.1.256 CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Register (Offset = 3A058h + formula) [reset = 0h]

Register Description: Total number of transmitted frames abandoned due to a late collision

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18929. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A058h + formula

Figure 14-6253. CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18931. CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to a late collision

14.9.2.1.257 CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Register (Offset = 3A05Ch + formula) [reset = 0h]

Register Description: Total number of receive inter-packet gap errors (10G only)

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18932. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A05Ch + formula

Figure 14-6254. CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18934. CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of receive inter-packet gap errors (10G only)

14.9.2.1.258 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Register (Offset = 3A060h + formula) [reset = 0h]

Register Description: Total number of transmitted frames that experienced a carrier loss

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18935. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A060h + formula

Figure 14-6255. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18937. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames that experienced a carrier loss

14.9.2.1.259 CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Register (Offset = 3A064h + formula) [reset = 0h]

Register Description: Total number of bytes in all good frames transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18938. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A064h + formula

Figure 14-6256. CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18940. CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

14.9.2.1.260 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Register (Offset = 3A068h + formula) [reset = 0h]

Register Description: Total number of 64-byte frames received and transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18941. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A068h + formula

Figure 14-6257. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18943. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

14.9.2.1.261 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Register (Offset = 3A06Ch + formula) [reset = 0h]

Register Description: Total number of frames of size 65 to 127 bytes received and transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18944. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A06Ch + formula

Figure 14-6258. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18946. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

14.9.2.1.262 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Register (Offset = 3A070h + formula) [reset = 0h]

Register Description: Total number of frames of size 128 to 255 bytes received and transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18947. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A070h + formula

Figure 14-6259. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18949. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

14.9.2.1.263 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Register (Offset = 3A074h + formula) [reset = 0h]

Register Description: Total number of frames of size 256 to 511 bytes received and transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18950. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A074h + formula

Figure 14-6260. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18952. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted

14.9.2.1.264 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Register (Offset = 3A078h + formula) [reset = 0h]

Register Description: Total number of frames of size 512 to 1023 bytes received and transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18953. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A078h + formula

Figure 14-6261. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18955. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted

14.9.2.1.265 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Register (Offset = 3A07Ch + formula) [reset = 0h]

Register Description: Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18956. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A07Ch + formula

Figure 14-6262. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18958. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

14.9.2.1.266 CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Register (Offset = 3A080h + formula) [reset = 0h]

Register Description: Total number of bytes received and transmitted

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18959. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A080h + formula

Figure 14-6263. CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18961. CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes received and transmitted

14.9.2.1.267 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Register (Offset = 3A084h + formula) [reset = 0h]

Register Description: Receive Bottom of FIFO Drop

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18962. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A084h + formula

Figure 14-6264. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18964. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Bottom of FIFO Drop

14.9.2.1.268 CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Register (Offset = 3A088h + formula) [reset = 0h]

Register Description: Total number of dropped frames received due to portmask

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18965. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A088h + formula

Figure 14-6265. CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-18967. CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames received due to portmask

14.9.2.1.269 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Register (Offset = 3A08Ch + formula) [reset = 0h]

Register Description: Receive Top of FIFO Drop

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18968. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A08Ch + formula

Figure 14-6266. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18970. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Top of FIFO Drop

14.9.2.1.270 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Register (Offset = 3A090h + formula) [reset = 0h]

Register Description: Total number of dropped frames due to ALE Rate Limiting

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18971. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A090h + formula

Figure 14-6267. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18973. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting

14.9.2.1.271 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Register (Offset = 3A094h + formula) [reset = 0h]

Register Description: Total number of dropped frames due to ALE VID Ingress

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18974. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A094h + formula

Figure 14-6268. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18976. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress

14.9.2.1.272 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Register (Offset = 3A098h + formula) [reset = 0h]

Register Description: Total number of dropped frames due to DA=SA

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18977. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A098h + formula

Figure 14-6269. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18979. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA

14.9.2.1.273 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Register (Offset = 3A09Ch + formula) [reset = 0h]

Register Description: Total number of dropped frames due to ALE Block Mode

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18980. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A09Ch + formula

Figure 14-6270. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18982. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode

14.9.2.1.274 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Register (Offset = 3A0A0h + formula) [reset = 0h]

Register Description: Total number of dropped frames due to ALE Secure Mode

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18983. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0A0h + formula

Figure 14-6271. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18985. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode

14.9.2.1.275 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Register (Offset = 3A0A4h + formula) [reset = 0h]

Register Description: Total number of dropped frames due to ALE Authentication

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18986. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0A4h + formula

Figure 14-6272. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18988. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication

14.9.2.1.276 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Register (Offset = 3A0A8h + formula) [reset = 0h]

Register Description: ALE Receive Unknown Unicast

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18989. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0A8h + formula

Figure 14-6273. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18991. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast

14.9.2.1.277 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Register (Offset = 3A0ACh + formula) [reset = 0h]

Register Description: ALE Receive Unknown Unicast Bytecount

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18992. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0ACh + formula

Figure 14-6274. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18994. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount

14.9.2.1.278 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Register (Offset = 3A0B0h + formula) [reset = 0h]

Register Description: ALE Receive Unknown Multicast

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18995. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0B0h + formula

Figure 14-6275. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-18997. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast

14.9.2.1.279 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Register (Offset = 3A0B4h + formula) [reset = 0h]

Register Description: ALE Receive Unknown Multicast Bytecount

Formula = (j * 200h); where j = 0 to 2d

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Table 14-18998. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0B4h + formula

Figure 14-6276. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19000. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount

14.9.2.1.280 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Register (Offset = 3A0B8h + formula) [reset = 0h]

Register Description: ALE Receive Unknown Broadcast

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19001. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0B8h + formula

Figure 14-6277. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19003. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast

14.9.2.1.281 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Register (Offset = 3A0BCh + formula) [reset = 0h]

Register Description: ALE Receive Unknown Broadcast Bytecount

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19004. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0BCh + formula

Figure 14-6278. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19006. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount

14.9.2.1.282 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Register (Offset = 3A0C0h + formula) [reset = 0h]

Register Description: ALE Policer Matched

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19007. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0C0h + formula

Figure 14-6279. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19009. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched

14.9.2.1.283 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Register (Offset = 3A0C4h + formula) [reset = 0h]

Register Description: ALE Policer Matched and Condition Red

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19010. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0C4h + formula

Figure 14-6280. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19012. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Red

14.9.2.1.284 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Register (Offset = 3A0C8h + formula) [reset = 0h]

Register Description: ALE Policer Matched and Condition Yellow

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19013. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0C8h + formula

Figure 14-6281. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19015. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow

14.9.2.1.285 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Register (Offset = 3A0CCh + formula) [reset = 0h]

Register Description: ALE Multicast Source Address Drop

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19016. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0CCh + formula

Figure 14-6282. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19018. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Multicast Source Address drop

14.9.2.1.286 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Register (Offset = 3A0D0h + formula) [reset = 0h]

Register Description: ALE Dual VLAN Drop

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19019. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0D0h + formula

Figure 14-6283. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19021. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Dual VLAN drop

14.9.2.1.287 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Register (Offset = 3A0D4h + formula) [reset = 0h]

Register Description: ALE Length Error Drop

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19022. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0D4h + formula

Figure 14-6284. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19024. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Length Error drop

14.9.2.1.288 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Register (Offset = 3A0D8h + formula) [reset = 0h]

Register Description: ALE IP Next Header Drop

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19025. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0D8h + formula

Figure 14-6285. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19027. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Next Header drop

14.9.2.1.289 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Register (Offset = 3A0DCh + formula) [reset = 0h]

Register Description: ALE IPV4 Frag Drop

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19028. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A0DCh + formula

Figure 14-6286. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19030. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE IPV4 Fragment drop

14.9.2.1.290 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Register (Offset = 3A140h + formula) [reset = 0h]

Register Description: IET Receive Assembly Error

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19031. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A140h + formula

Figure 14-6287. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_ASSEMBLY_ERROR							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_RX_ASSEMBLY_ERROR							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_RX_ASSEMBLY_ERROR							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_ERROR							
R/W							
0h							

Table 14-19033. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_ASSEMBLY_ERROR	R/W	0h	IET Receive Assembly Error

14.9.2.1.291 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Register (Offset = 3A144h + formula) [reset = 0h]

Register Description: IET Receive Assembly Ok

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19034. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A144h + formula

Figure 14-6288. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_ASSEMBLY_OK							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_RX_ASSEMBLY_OK							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_RX_ASSEMBLY_OK							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_OK							
R/W							
0h							

Table 14-19036. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_ASSEMBLY_OK	R/W	0h	IET Receive Assembly Ok

14.9.2.1.292 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Register (Offset = 3A148h + formula) [reset = 0h]

Register Description: IET Receive Smd Error

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19037. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A148h + formula

Figure 14-6289. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_SMD_ERROR							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_RX_SMD_ERROR							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_RX_SMD_ERROR							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_RX_SMD_ERROR							
R/W							
0h							

Table 14-19039. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_SMD_ERROR	R/W	0h	IET Receive Smd Error

14.9.2.1.293 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Register (Offset = 3A14Ch + formula) [reset = 0h]

Register Description: IET Receive Frag

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19040. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A14Ch + formula

Figure 14-6290. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_FRAG							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_RX_FRAG							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_RX_FRAG							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_RX_FRAG							
R/W							
0h							

Table 14-19042. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_FRAG	R/W	0h	IET Receive Frag

14.9.2.1.294 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Register (Offset = 3A150h + formula) [reset = 0h]

Register Description: IET Transmit Hold

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19043. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A150h + formula

Figure 14-6291. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Name Register

31	30	29	28	27	26	25	24
IET_TX_HOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_TX_HOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_TX_HOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_TX_HOLD							
R/W							
0h							

Table 14-19045. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_TX_HOLD	R/W	0h	IET Transmit Hold

14.9.2.1.295 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Register (Offset = 3A154h + formula) [reset = 0h]

Register Description: IET Transmit Frag

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19046. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A154h + formula

Figure 14-6292. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Name Register

31	30	29	28	27	26	25	24
IET_TX_FRAG							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_TX_FRAG							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_TX_FRAG							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_TX_FRAG							
R/W							
0h							

Table 14-19048. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_TX_FRAG	R/W	0h	IET Transmit Frag

14.9.2.1.296 CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Register

CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Register (Offset = 3A17Ch + formula) [reset = 0h]

Register Description: Transmit Memory Protect CRC Error

Formula = (j * 200h); where j = 0 to 2d

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Table 14-19049. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A17Ch + formula

Figure 14-6293. CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-19051. CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COUNT	R/W	0h	Transmit Memory Protect CRC Error

14.9.2.1.297 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Register (Offset = 3A180h + formula) [reset = 0h]

Register Description: ENET Port n PRIORITY N Packet Count

Formula = (j * 200h) + (k * 4h); where j = 0 to 2d, k = 0 to 7d

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Table 14-19052. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A180h + formula

Figure 14-6294. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN							
R/W							
0h							

Table 14-19054. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN	R/W	0h	ENET TX Priority Packet Count

14.9.2.1.298 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Register (Offset = 3A1A0h + formula) [reset = 0h]

Register Description: ENET Port n PRIORITY N Packet Byte Count

Formula = (j * 200h) + (k * 4h); where j = 0 to 2d, k = 0 to 7d

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Table 14-19055. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A1A0h + formula

Figure 14-6295. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PN_TX_PRIN_BCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PN_TX_PRIN_BCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PN_TX_PRIN_BCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PN_TX_PRIN_BCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19057. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Byte Count

14.9.2.1.299 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Register (Offset = 3A1C0h + formula) [reset = 0h]

Register Description: ENET Port n PRIORITY N Packet Drop Count

Formula = (j * 200h) + (k * 4h); where j = 0 to 2d, k = 0 to 7d

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Table 14-19058. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A1C0h + formula

Figure 14-6296. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_DROP							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_DROP							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP							
R/W							
0h							

Table 14-19060. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP	R/W	0h	ENET Port n PRIORITY N Packet Drop Count

14.9.2.1.300 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Register

CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Register (Offset = 3A1E0h + formula) [reset = 0h]

Register Description: ENET Port n PRIORITY N Packet Drop Byte Count

Formula = (j * 200h) + (k * 4h); where j = 0 to 2d, k = 0 to 7d

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Table 14-19061. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 A1E0h + formula

Figure 14-6297. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							

Table 14-19063. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Drop Byte Count

14.9.2.1.301 CPSW3_CPSW_NU_CPTS_IDVER_REG Register

CPSW3_CPSW_NU_CPTS_IDVER_REG Register (Offset = 3D000h) [reset = 4E8A010Ch]

Register Description: Identification and Version Register

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Table 14-19064. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D000h

Figure 14-6298. CPSW3_CPSW_NU_CPTS_IDVER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4E8Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TX_IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4E8Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_VER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MINOR_VER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Ch</td></tr>
</table>

Table 14-19066. CPSW3_CPSW_NU_CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TX_IDENT	R	4E8Ah	Identification value
15:11	RTL_VER	R	0h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	Ch	Minor version value

14.9.2.1.302 CPSW3_CPSW_NU_CPTS_CONTROL_REG Register

CPSW3_CPSW_NU_CPTS_CONTROL_REG Register (Offset = 3D004h) [reset = 4h]

Register Description: Time Sync Control Register

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Table 14-19067. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D004h

Figure 14-6299. CPSW3_CPSW_NU_CPTS_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W				NONE			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						TS_GENF_CLR_EN	TS_RX_NO_EVENT
NONE						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HW8_TS_PUSH_EN	HW7_TS_PUSH_EN	HW6_TS_PUSH_EN	HW5_TS_PUSH_EN	HW4_TS_PUSH_EN	HW3_TS_PUSH_EN	HW2_TS_PUSH_EN	HW1_TS_PUSH_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_PPM_DIR	TS_COMP_TOG	MODE	SEQUENCE_EN	TSTAMP_EN	TS_COMP_POLARITY	INT_TEST	CPTS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	0h

Table 14-19069. CPSW3_CPSW_NU_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description

31:28	TS_SYNC_SEL	R/W	0h	TS_SYNC output time stamp counter bit select.
				`0h TS_SYNC disabled.`
				`1h-Fh TS_SYNC is time stamp counter bits 31 (Fh) down to 17 (1h).`

27:18	RESERVED	NONE	0h	Reserved

17	TS_GENF_CLR_EN	R/W	0h	GENF (and ESTF) Clear Enable.
				`0h A CPTS_GENFn output is not cleared when the associated CPSW_GENF_LENGTH_REG_l[31:0] is cleared to zero.`
				`1h A CPTS_GENFn output is cleared when the associated CPSW_GENF_LENGTH_REG_l[31:0] is cleared to zero.`

16	TS_RX_NO_EVENT	R/W	0h	Timestamp Ethernet Receive produces no events.
				`0h Ethernet receive timesync events enabled.`
				`1h Ethernet receive timesync events disabled.`

15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable.
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable.

Table 14-19069. CPSW3_CPSW_NU_CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable.
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable.
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable.
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable.
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable.
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable.
7	TS_PPM_DIR	R/W	0h	PPM Correction Direction. 0h Increase the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG) by the PPM value. 1h Decrease the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG and) by the PPM value.
6	TS_COMP_TOG	R/W	0h	Time Stamp Compare Toggle mode. 0h TS_COMP is in non-toggle mode. 1h TS_COMP is in toggle mode.
5	MODE	R/W	0h	64-Bit Mode. 0h The time stamp is 32-bits with the upper 32-bits forced to zero. 1h The time stamp is 64-bits.
4	SEQUENCE_EN	R/W	0h	Sequence Enable. 0h The time stamp value increments with the selected RFTCLK 1h The time stamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc).
3	TSTAMP_EN	R/W	0h	Host Receive Time Stamp Enable. 0h Time stamps are disabled on received packets to host. 1h Time stamps enabled on received packets to host (PCIE_CPTS_CONTROL_REG[0] CPTS_EN must be set).
2	TS_COMP_POLARITY	R/W	1h	TS_COMP Polarity. 0h TS_COMP is asserted low. 1h TS_COMP is asserted high.
1	INT_TEST	R/W	0h	Interrupt Test. When set, this bit allows the raw interrupt to be written to facilitate interrupt test.
0	CPTS_EN	R/W	0h	Time Sync Enable. When disabled (cleared to zero), the RCLK domain is held in reset.

14.9.2.1.303 CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register

CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register (Offset = 3D008h) [reset = 0h]

Register Description: RFTCLK Select Register

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Table 14-19070. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D008h

Figure 14-6300. CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RFTCLK_SEL				
NONE			R/W				
0h			0h				

Table 14-19072. CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	RFTCLK_SEL	R/W	0h	Reference clock select. This bit field is used to control an external multiplexer that selects one out of 8 clocks for time sync reference. 0h Selects CPSWHSDIV_CLKOUT2 clock 1h Selects MAINHSDIV_CLKOUT3 clock 2h Selects MCU_CPTS0_RFT_CLK I/O pin 3h Selects CPTS0_RFT_CLK I/O pin 4h Selects MCU_EXT_REFCLK0 I/O pin 5h Selects EXT_REFCLK1 I/O pin 6h Selects PCIE0_TXI0_CLK clock 7h Selects PCIE1_TXI0_CLK clock The RFTCLK_SEL value can be written only when the [0] CPTS_EN and [3] TSTAMP_EN bits are cleared to zero in the CPSW_CPTS_CONTROL_REG register.

14.9.2.1.304 CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register

CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register (Offset = 3D00Ch) [reset = 0h]

Register Description: Time Stamp Event Push Register

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Table 14-19073. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D00Ch

Figure 14-6301. CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
NONE							W
0h							0h

Table 14-19075. CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PUSH	W	0h	Time stamp event push. When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads zero.

14.9.2.1.305 CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register

CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register (Offset = 3D010h) [reset = 0h]

Register Description: Time Stamp Load Low Value Register

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Table 14-19076. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D010h

Figure 14-6302. CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 14-19078. CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time stamp load low value

14.9.2.1.306 CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register

CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register (Offset = 3D014h) [reset = 0h]

Register Description: Time Stamp Load Enable Register

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Table 14-19079. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D014h

Figure 14-6303. CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
NONE							W
0h							0h

Table 14-19081. CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_LOAD_EN	W	0h	Time Stamp Load Enable. Writing a one to this bit enables the time stamp value to be written with the value in CPSW_CPTS_TS_LOAD_VAL_REG/ CPSW_CPTS_TS_LOAD_HIGH_VAL_REG. This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the time stamp (CPSW_CPTS_TS_LOAD_HIGH_VAL_REG) are forced to zero in 32-bit mode.

14.9.2.1.307 CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register

CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register (Offset = 3D018h) [reset = 0h]

Register Description: Time Stamp Comparison Low Value Register

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Table 14-19082. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D018h

Figure 14-6304. CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_VAL							
R/W							
0h							

Table 14-19084. CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_VAL	R/W	0h	Time Stamp Comparison Low Value. Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL.

14.9.2.1.308 CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register

CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register (Offset = 3D01Ch) [reset = 0h]

Register Description: Time Stamp Comparison Length Register

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Table 14-19085. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D01Ch

Figure 14-6305. CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_LENGTH							
R/W							
0h							

Table 14-19087. CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_LENGTH	R/W	0h	Time Stamp Comparison Length. Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the CPSW_GENF_COMP_LOW_REG_L[31-0] COMP_LOW and CPSW_GENF_COMP_HIGH_REG_L[31-0] COMP_HIGH registers are written.

14.9.2.1.309 CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register

CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register (Offset = 3D020h) [reset = 0h]

Register Description: Interrupt Status Register Raw

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Table 14-19088. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D020h

Figure 14-6306. CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TS_PEND_RAW
NONE							R/W
0h							0h

Table 14-19090. CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable). Writable when CPSW_CPTS_CONTROL_REG[1] INT_TEST = 1h A one in this bit indicates that there are one or more events in the event FIFO.

14.9.2.1.310 CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register

CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register (Offset = 3D024h) [reset = 0h]

Register Description: Interrupt Status Register Masked

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Table 14-19091. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D024h

Figure 14-6307. CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND
NONE							R
0h							0h

Table 14-19093. CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

14.9.2.1.311 CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register

CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register (Offset = 3D028h) [reset = 0h]

Register Description: Interrupt Enable Register

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Table 14-19094. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D028h

Figure 14-6308. CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
NONE							R/W
0h							0h

Table 14-19096. CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

14.9.2.1.312 CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register

CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register (Offset = 3D02Ch) [reset = 0h]

Register Description: Time Stamp Comparison Nudge Register

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Table 14-19097. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D02Ch

Figure 14-6309. CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-19099. CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time stamp Comparison Nudge Value. This two's complement number is added to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH value to increase or decrease the TS_COMP length by the CPSW_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_CPTS_TS_COMP_NUDGE_REG value is cleared to zero when the nudge has occurred.

14.9.2.1.313 CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register

CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register (Offset = 3D030h) [reset = 0h]

Register Description: Event Pop Register

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Table 14-19100. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D030h

Figure 14-6310. CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
NONE							W
0h							0h

Table 14-19102. CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EVENT_POP	W	0h	Event Pop. When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read from the CPSW_CPTS_EVENT_0_REG to CPSW_CPTS_EVENT_3_REG registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.

14.9.2.1.314 CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register

CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register (Offset = 3D034h) [reset = 0h]

Register Description: Event 0 Register

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Table 14-19103. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D034h

Figure 14-6311. CPSW3_CPSW_NU_CPTS_EVENT_0_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 14-19105. CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp. The time stamp is valid for transmit, receive, and time stamp push event types. The time stamp value is not valid for counter roll event types.

14.9.2.1.315 CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register

CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register (Offset = 3D038h) [reset = 0h]

Register Description: Event 1 Register

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Table 14-19106. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D038h

Figure 14-6312. CPSW3_CPSW_NU_CPTS_EVENT_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
NONE		R	R				
0h		0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EVENT_TYPE				MESSAGE_TYPE			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SEQUENCE_ID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEQUENCE_ID							
R							
0h							

Table 14-19108. CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	PREMPT_QUEUE	R	0h	Prempt QUEUE
28:24	PORT_NUMBER	R	0h	Port Number. Indicates the port number (encoded) of an Ethernet event or the encoded hardware time stamp number.

23:20	EVENT_TYPE	R	0h	Time Sync Event Type
				`0h    Time Stamp Push Event`
				`1h    Time Stamp Rollover Event`
				`2h    Time Stamp Half Rollover Event`
				`3h    Hardware Time Stamp Push Event`
				`4h    Ethernet Receive Event`
				`5h    Ethernet Transmit Event`
				`6h    Time Stamp Compare Event`
				`7h    Host Transmit Event`
				`8h-Fh Reserved`

19:16	MESSAGE_TYPE	R	0h	Message type. The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

Table 14-19108. CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SEQUENCE_ID	R	0h	Sequence ID. The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

14.9.2.1.316 CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register

CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register (Offset = 3D03Ch) [reset = 0h]

Register Description: Event 2 Register

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Table 14-19109. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D03Ch

Figure 14-6313. CPSW3_CPSW_NU_CPTS_EVENT_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DOMAIN							
R							
0h							

Table 14-19111. CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DOMAIN	R	0h	Domain. The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

14.9.2.1.317 CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register

CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register (Offset = 3D040h) [reset = 0h]

Register Description: Event 3 Register

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Table 14-19112. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D040h

Figure 14-6314. CPSW3_CPSW_NU_CPTS_EVENT_3_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 14-19114. CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp. The time stamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode.

14.9.2.1.318 CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register

CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 3D044h) [reset = 0h]

Register Description: Time Stamp Load High Value Register

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Table 14-19115. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D044h

Figure 14-6315. CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 14-19117. CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time Stamp Load high Value. Writing the CPSW_CPTS_TS_LOAD_EN_REG[0] TS_LOAD_EN bit causes the value contained in this register to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode

14.9.2.1.319 CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register

CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 3D048h) [reset = 0h]

Register Description: Time Stamp Comparison High Value Register

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Table 14-19118. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D048h

Figure 14-6316. CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_HIGH_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_HIGH_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_HIGH_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL							
R/W							
0h							

Table 14-19120. CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_HIGH_VAL	R/W	0h	Time Stamp Comparison High Value. Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the [31-0]TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL and CPSW_CPTS_TS_COMP_HIGH_VAL_REG[31-0] TS_COMP_HIGH_VAL. This value is unused in 32-bit mode. The upper 32-bits in CPSW_CPTS_TS_COMP_HIGH_VAL_REG register should be written before the lower 32-bits in the CPSW_CPTS_TS_COMP_VAL_REG register.

14.9.2.1.320 CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register

CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register (Offset = 3D04Ch) [reset = 0h]

Register Description: TS Add Value Register

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Table 14-19121. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D04Ch

Figure 14-6317. CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED					ADD_VAL		
NONE					R/W		
0h					0h		

Table 14-19123. CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADD_VAL	R/W	0h	The ts_add_value[2:0] is added to 1 to comprise the time stamp increment value. The time stamp increment value is added to the current time stamp (time_stamp[63:0]) on each RCLK. The time stamp increment value can be adjusted by nudge and ppm also. The CPSW_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL value may be non-zero in 64-bit mode only.

14.9.2.1.321 CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register

CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 3D050h) [reset = 0h]

Register Description: Time Stamp PPM Low Value Register

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Table 14-19124. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D050h

Figure 14-6318. CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_PPM_LOW_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_PPM_LOW_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_PPM_LOW_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL							
R/W							
0h							

Table 14-19126. CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_PPM_LOW_VAL	R/W	0h	Time Stamp PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen.

14.9.2.1.322 CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register

CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 3D054h) [reset = 0h]

Register Description: Time Stamp PPM High Value Register

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Table 14-19127. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D054h

Figure 14-6319. CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TS_PPM_HIGH_VAL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TS_PPM_HIGH_VAL							
R/W							
0h							

Table 14-19129. CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TS_PPM_HIGH_VAL	R/W	0h	Time Stamp PPM High Value. This value should be written first (before the low value is written). The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).

14.9.2.1.323 CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register

CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register (Offset = 3D058h) [reset = 0h]

Register Description: Time Stamp Nudge Value Register

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Table 14-19130. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D058h

Figure 14-6320. CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TS_NUDGE_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19132. CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge Value. This two's complement number is added to the CPSW_CPTS_EVENT_0_REG[31-0] TIME_STAMP and CPSW_CPTS_EVENT_3_REG[[31-0] TIME_STAMP value to increase or decrease the time stamp value by the CPSW_CPTS_TS_NUDGE_VAL_REG[7-0] TS_NUDGE_VAL amount. The TS_NUDGE_VAL value is cleared to zero when the nudge has occurred. The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).

14.9.2.1.324 CPSW3_CPSW_NU_CPTS_TS_CONFIG Register

CPSW3_CPSW_NU_CPTS_TS_CONFIG Register (Offset = 3D0D0h) [reset = 2002h]

Register Description: Time Stamp Configuration Read

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Table 14-19133. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D0D0h

Figure 14-6321. CPSW3_CPSW_NU_CPTS_TS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EVNT_FIFO_DEPTH							
R							
20h							
7	6	5	4	3	2	1	0
NUM_GENF							
R							
2h							

Table 14-19135. CPSW3_CPSW_NU_CPTS_TS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	EVNT_FIFO_DEPTH	R	20h	The Event FIFO Depth
7:0	NUM_GENF	R	2h	The number of CPTS GENF outputs

14.9.2.1.325 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Register (Offset = 3D0E0h + formula) [reset = 0h]

Register Description: Time Stamp Generate Function Comparison Low Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19136. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D0E0h + formula

Figure 14-6322. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 14-19138. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_GENF_COMP_HIGH_REG_l and CPSW_GENF_COMP_LOW_REG_l should only be written when the CPSW_GENF_LENGTH_REG_l[31-0] LENGTH value is zero.

14.9.2.1.326 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Register (Offset = 3D0E4h + formula) [reset = 0h]

Register Description: Time Stamp Generate Function Comparison high Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19139. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D0E4h + formula

Figure 14-6323. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 14-19141. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits. The CPSW_GENF_COMP_HIGH_REG_l and CPSW_GENF_COMP_LOW_REG_l should only be written when the CPSW_GENF_LENGTH_REG_l[31-0] LENGTH value is zero.

14.9.2.1.327 CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Register (Offset = 3D0E8h + formula) [reset = 0h]

Register Description: Time Stamp Generate Function Control

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19142. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D0E8h + formula

Figure 14-6324. CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
NONE						R/W	R/W
0h						0h	0h

Table 14-19144. CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert 0h The output TS_GENFn signal asserts low 1h The output TS_GENFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction. 0h A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

14.9.2.1.328 CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Register (Offset = 3D0ECh + formula) [reset = 0h]

Register Description: Time Stamp Generate Function Length Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19145. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D0ECh + formula

Figure 14-6325. CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 14-19147. CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value

14.9.2.1.329 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Register (Offset = 3D0F0h + formula) [reset = 0h]

Register Description: Time Stamp Generate Function PPM Low Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19148. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D0F0h + formula

Figure 14-6326. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 14-19150. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

14.9.2.1.330 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Register (Offset = 3D0F4h + formula) [reset = 0h]

Register Description: Time Stamp Generate Function PPM High Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19151. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D0F4h + formula

Figure 14-6327. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PPM_HIGH	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPM_HIGH							
R/W							
0h							

Table 14-19153. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value. This value should be written first (before the low value is written).

14.9.2.1.331 CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Register (Offset = 3D0F8h + formula) [reset = 0h]

Register Description: Time Stamp Generate Function Nudge Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19154. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D0F8h + formula

Figure 14-6328. CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-19156. CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_GENF_NUDGE_REG_I[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_GENF_NUDGE_REG_I value is cleared to zero when the nudge has occurred.

14.9.2.1.332 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Register (Offset = 3D200h + formula) [reset = 0h]

Register Description: Time Stamp ESTF Generate Function Comparison Low Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19157. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D200h + formula

Figure 14-6329. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 14-19159. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	ESTFn comparison value lower 32-bits. This value should be written after the upper 32-bits. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

14.9.2.1.333 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Register (Offset = 3D204h + formula) [reset = 0h]

Register Description: Time Stamp ESTF Generate Function Comparison high Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19160. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D204h + formula

Figure 14-6330. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 14-19162. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	ESTFn comparison value upper 32-bits. This value should be written before the lower 32-bits are written. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

14.9.2.1.334 CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Register (Offset = 3D208h + formula) [reset = 0h]

Register Description: Time Stamp ESTF Generate Function Control

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19163. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D208h + formula

Figure 14-6331. CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
NONE						R/W	R/W
0h						0h	0h

Table 14-19165. CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 2) Polarity Invert. 0h The output TS_ESTFn signal asserts low 1h The output TS_ESTFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 2) PPM Direction. 0h A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

14.9.2.1.335 CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Register (Offset = 3D20Ch + formula) [reset = 0h]

Register Description: Time Stamp ESTF Generate Function Length Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19166. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D20Ch + formula

Figure 14-6332. CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 14-19168. CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function Length Value.

14.9.2.1.336 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Register (Offset = 3D210h + formula) [reset = 0h]

Register Description: Time Stamp ESTF Generate Function PPM Low Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19169. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D210h + formula

Figure 14-6333. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 14-19171. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

14.9.2.1.337 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Register (Offset = 3D214h + formula) [reset = 0h]

Register Description: Time Stamp ESTF Generate Function PPM High Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19172. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D214h + formula

Figure 14-6334. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PPM_HIGH</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PPM_HIGH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19174. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM High Value. This value should be written first (before the low value is written).

14.9.2.1.338 CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Register

CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Register (Offset = 3D218h + formula) [reset = 0h]

Register Description: Time Stamp ESTF Generate Function Nudge Value

Formula = (j * 20h); where j = 0 to 1d

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Table 14-19175. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 D218h + formula

Figure 14-6335. CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUDGE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19177. CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_ESTF_NUDGE_REG_l[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_ESTF_NUDGE_REG_l value is cleared to zero when the nudge has occurred.

14.9.2.1.339 CPSW3_CPSW_NU_ALE_MOD_VER Register

CPSW3_CPSW_NU_ALE_MOD_VER Register (Offset = 3E000h) [reset = 294104h]

Register Description: The Module and Version Register identifies the module identifier and revision of the ALE_3g512ie module.

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Table 14-19178. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E000h

Figure 14-6336. CPSW3_CPSW_NU_ALE_MOD_VER Name Register

31	30	29	28	27	26	25	24
MODULE_ID							
R							
29h							

23	22	21	20	19	18	17	16
MODULE_ID							
R							
29h							

15	14	13	12	11	10	9	8
RTL_VERSION					MAJOR_REVISION		
R					R		
8h					1h		

7	6	5	4	3	2	1	0
CUSTOM_REVISION		MINOR_REVISION					
R		R					
0h		4h					

Table 14-19180. CPSW3_CPSW_NU_ALE_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODULE_ID	R	29h	ALE_3g512ie module ID.
15:11	RTL_VERSION	R	8h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	4h	Minor Revision.

14.9.2.1.340 CPSW3_CPSW_NU_ALE_ALE_STATUS Register

CPSW3_CPSW_NU_ALE_ALE_STATUS Register (Offset = 3E004h) [reset = 80000400h]

Register Description: The ALE status provides information on the ALE configuration and state. The ~iramdepth is used to determine how IPv6 entries are stored in the table. IPv6 entries are stored in two entries where IPv6 Entry hi is designated by the odd slice index and lo is designated by the even slice index. The slice index is above the ram depth like {SlixeIndex,RamIndex}. So for a 64 deep RAM index of 0x005, the Hi portion of the IPv6 entry is located at 0x005|0x040 and the Lo portion is located at 0x005&(~0x040).

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Table 14-19181. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E004h

Figure 14-6337. CPSW3_CPSW_NU_ALE_ALE_STATUS Name Register

31	30	29	28	27	26	25	24
UREGANDREGMSK12	UREGANDREGMSK08	RESERVED					
R	R	NONE					
1h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POLCNTDIV8							
R							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMDEPTH128	RAMDEPTH32	RESERVED	KLUENTRIES				
R	R	NONE	R				
0h	0h	0h	0h				

Table 14-19183. CPSW3_CPSW_NU_ALE_ALE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UREGANDREGMSK12	R	1h	When set, the unregistered multicast field is a mask versus an index on 12 bit boundary in the ALE table.
30	UREGANDREGMSK08	R	0h	When set, the unregistered multicast field is a mask versus an index on 8 bit boundary in the ALE table.
29:16	RESERVED	NONE	0h	Reserved
15:8	POLCNTDIV8	R	4h	This is the number of policer engines the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.
7	RAMDEPTH128	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both ramdepth128 and ramdepth32 are zero the depth is 64.
6	RAMDEPTH32	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both ramdepth128 and ramdepth32 are zero the depth is 64.
5	RESERVED	NONE	0h	Reserved

Table 14-19183. CPSW3_CPSW_NU_ALE_ALE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	KLUENTRIES	R	0h	This is the number of table entries total divided by 1024. A value of 1 indicates 1024 table entries. A value of 8 indicates 8192 table entries.

14.9.2.1.341 CPSW3_CPSW_NU_ALE_ALE_CONTROL Register

CPSW3_CPSW_NU_ALE_ALE_CONTROL Register (Offset = 3E008h) [reset = 0h]

Register Description: The ALE Control Register is used to set the ALE modes used for all ports.

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Table 14-19184. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E008h

Figure 14-6338. CPSW3_CPSW_NU_ALE_ALE_CONTROL Name Register

31	30	29	28	27	26	25	24
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NOW	RESERVED			MIRROR_DP	
R/W	R/W	R/W	NONE			R/W	
0h	0h	0h	0h			0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UPD_BW_CTRL			RESERVED			MIRROR_TOP	
R/W			NONE			R/W	
0h			0h			0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UPD_STATIC	LRN_HOST_DST	UVLAN_NO_LEARN	MIRROR_MEN	MIRROR_DEN	MIRROR_SEN	RESERVED	EN_HOST_UNI_FLOOD
R/W	R/W	R/W	R/W	R/W	R/W	NONE	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LEARN_NO_VLANID	ENABLE_VID0_MODE	ENABLE_OUI_DENY	ENABLE_BYPASS	BCAST_MCAST_CTL	ALE_VLAN_AWARE	ENABLE_AUTH_MODE	ENABLE_RATE_LIMIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19186. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_ALE	R/W	0h	Enable ALE 0 - Drop all packets 1 - Enable ALE packet processing
30	CLEAR_TABLE	R/W	0h	Clear ALE address table - Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.
29	AGE_OUT_NOW	R/W	0h	Age Out Address Table Now - Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.
28:26	RESERVED	NONE	0h	Reserved

Table 14-19186. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:24	MIRROR_DP	R/W	0h	Mirror Destination Port - This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the ~imirror_top port.
23:21	UPD_BW_CTRL	R/W	0h	The ~iupd_bw_ctrl field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the ~iupd_bw_ctrl can be programmed more aggressive. If the ~iupd_bw_ctrl is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. 0 - 350Mhz, 5M 1 - 359Mhz, 11M 2 - 367Mhz, 16M 3 - 375Mhz, 22M 4 - 384Mhz, 28M 5 - 392Mhz, 34M 6 - 400Mhz, 39M 7 - 409Mhz, 45M
20:18	RESERVED	NONE	0h	Reserved
17:16	MIRROR_TOP	R/W	0h	Mirror To Port - This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.
15	UPD_STATIC	R/W	0h	Update Static Entries - A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be '0' for most switch configurations.
14	LRN_HOST_DST	R/W	0h	Learn Host Destination - This field is set to only learn unicast packet source addresses that are destined to the host port. This bit is only valid for 3 port switches and allows the ALE table to only contain addresses the host port is concerned about. This bit is affectively disabled when ~ien_host_uni_flood is set since any unknown unicast is also sent to the host port for extended bridging operations.
13	UVLAN_NO_LEARN	R/W	0h	Unknown VLAN No Learn - This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.
12	MIRROR_MEN	R/W	0h	Mirror Match Entry Enable - This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the ~imirror_midx entry index will have that traffic also sent to the ~imirror_top port.
11	MIRROR_DEN	R/W	0h	Mirror Destination Port Enable - This field enables the destination port mirror option. When this bit is set any traffic destined for the ~imirror_dp port will have its transmit traffic also sent to the ~imirror_top port.
10	MIRROR_SEN	R/W	0h	Mirror Source Port Enable - This field enables the source port mirror option. When this bit is set any port with the ~ipX_mirror_sp set in the ALE Port Control registers set will have its received traffic also sent to the ~imirror_top port.
9	RESERVED	NONE	0h	Reserved
8	EN_HOST_UNI_FLOOD	R/W	0h	Unknown unicast packets flood to host 0 - unknown unicast packets are not sent to the host 1 - unknown unicast packets flood to host port as well as other ports
7	LEARN_NO_VLANID	R/W	0h	Learn No VID - 0 - VID is learned with the source address 1 - VID is not learned with the source address (source address is not tied to VID). Determines the entry type.

Table 14-19186. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ENABLE_VID0_MODE	R/W	0h	Enable VLAN ID = 0 Mode 0 - Process the priority tagged packet with VID = PORT_VLAN[11:0]. 1 - Process the priority tagged packet with VID = 0.
5	ENABLE_OUI_DENY	R/W	0h	Enable OUI Deny Mode - When set, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.
4	ENABLE_BYPASS	R/W	0h	ALE Bypass - When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port. 0 - no bypass 1 - bypass the ALE
3	BCAST_MCAST_CTL	R/W	0h	Rate Limit Transmit mode 0 - Broadcast and multicast rate limit counters are received port based 1 - Broadcast and multicast rate limit counters are transmit port based
2	ALE_VLAN_AWARE	R/W	0h	ALE VLAN Aware - Determines how traffic is forwarded using VLAN rules. 0 - Simple switch rules, packets forwarded to all ports for unknown destinations. 1 - VLAN Aware rules, packets forwarded based on VLAN members
1	ENABLE_AUTH_MODE	R/W	0h	Enable MAC Authorization Mode - Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set). 0 - The ALE is not in MAC authorization mode 1 - The ALE is in MAC authorization mode
0	ENABLE_RATE_LIMIT	R/W	0h	Enable Broadcast and Multicast Rate Limit 0 - Broadcast/Multicast rates not limited 1 - Broadcast/Multicast packet reception limited to the port control register rate limit fields.

14.9.2.1.342 CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register

CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register (Offset = 3E00Ch) [reset = 0h]

Register Description: The ALE Control 2 Register is used to set the extended features used for all ports.

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Table 14-19187. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E00Ch

Figure 14-6339. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Name Register

31	30	29	28	27	26	25	24
TRK_EN_DST	TRK_EN_SRC	TRK_EN_PRI	RESERVED	TRK_EN_IVLAN	RESERVED	TRK_EN_SIP	TRK_EN_DIP
R/W	R/W	R/W	NONE	R/W	NONE	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
DROP_BADLEN	NODROP_SRCMCST	DEFNOFRAG	DEFLMTNXTHDR	RESERVED	TRK_BASE		
R/W	R/W	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		

15	14	13	12	11	10	9	8
RESERVED							MIRROR_MIDX
NONE							R/W
0h							0h

7	6	5	4	3	2	1	0
MIRROR_MIDX							
R/W							
0h							

Table 14-19189. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK_EN_DST	R/W	0h	Trunk Enable Destination Address - This field enables the destination MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
30	TRK_EN_SRC	R/W	0h	Trunk Enable Source Address - This field enables the source MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
29	TRK_EN_PRI	R/W	0h	Trunk Enable Priority - This field enables the VLAN Priority bits to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used.
28	RESERVED	NONE	0h	Reserved
27	TRK_EN_IVLAN	R/W	0h	Trunk Enable Inner VLAN - This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
26	RESERVED	NONE	0h	Reserved
25	TRK_EN_SIP	R/W	0h	Trunk Enable Source IP Address - This field enables the source IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.

Table 14-19189. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	TRK_EN_DIP	R/W	0h	Trunk Enable Destination IP Address - This field enables the destination IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
23	DROP_BADLEN	R/W	0h	Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.
22	NODROP_SRCMCST	R/W	0h	No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.
21	DEFNOFRAG	R/W	0h	Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.
20	DEFLMTNXTHDR	R/W	0h	Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the ~iALE_NXT_HDR register values.
19	RESERVED	NONE	0h	Reserved
18:16	TRK_BASE	R/W	0h	Trunk Base - This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the ~itrk_en_dst, ~itrk_en_src, ~itrk_en_pri and ~itrk_en_vlan are '0', this value is used as the distribution index. That is a '0' will select the 1st bit of an 'N' link trunk, a '1' will select the second, etc. Below is the distribution across the trunk links. The first number in the ~iitalic sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0 will go to the base port (0), hash result 1 will go to the highest port of the trunk group (2), hash result 2 will go to the middle port (1), etc. 1 - ~i00000000 2 - ~i01010101 3 - ~i02102102 4 - ~i03210321
15:9	RESERVED	NONE	0h	Reserved
8:0	MIRROR_MIDX	R/W	0h	Mirror Index - This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the ~imirror_top port. That is any VLAN, ONU or address with or withou VLAN can be selected for traffic mirroring.

14.9.2.1.343 CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register

CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register (Offset = 3E010h) [reset = 0h]

Register Description: The ALE Prescale Register is used to set the Broadcast and Multicast rate limiting prescaler value.

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Table 14-19190. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E010h

Figure 14-6340. CPSW3_CPSW_NU_ALE_ALE_PRESCALE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ALE_PRESCALE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ALE_PRESCALE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ALE_PRESCALE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19192. CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	ALE_PRESCALE	R/W	0h	ALE Prescale - The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 0x10. The prescaler is off when the value is zero.

14.9.2.1.344 CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register

CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register (Offset = 3E014h) [reset = 0h]

Register Description: The ALE Aging Control sets the aging interval which will cause periodic aging to occur. This value specifies the minimum time between aging starts.

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Table 14-19193. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E014h

Figure 14-6341. CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Name Register

31	30	29	28	27	26	25	24
PRESCALE_2_DISABLE	PRESCALE_1_DISABLE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ALE_AGING_TIMER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ALE_AGING_TIMER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ALE_AGING_TIMER							
R/W							
0h							

Table 14-19195. CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESCALE_2_DISABLE	R/W	0h	ALE Prescaler 2 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
30	PRESCALE_1_DISABLE	R/W	0h	ALE Prescaler 1 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
29:24	RESERVED	NONE	0h	Reserved
23:0	ALE_AGING_TIMER	R/W	0h	ALE Aging Timer - This field specifies the number of clock cycles times 1,000,000 between aging operations.

14.9.2.1.345 CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register

CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register (Offset = 3E01Ch) [reset = 0h]

Register Description: The ALE Next Header is used to limit the IPv6 Next header or IPv4 Protocol values found in the IP header. It is enabled via the ~iLmtNxtHdr bit in the VLAN entry. All four ~iip_nxt_hdr0-3 are compared when enabled, so if only one is required, set them all to the one value to be tested.

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Table 14-19196. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E01Ch

Figure 14-6342. CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Name Register

31	30	29	28	27	26	25	24
IP_NXT_HDR3							
R/W							
0h							
23	22	21	20	19	18	17	16
IP_NXT_HDR2							
R/W							
0h							
15	14	13	12	11	10	9	8
IP_NXT_HDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
IP_NXT_HDR0							
R/W							
0h							

Table 14-19198. CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IP_NXT_HDR3	R/W	0h	The ~iip_nxt_hdr3 is the forth protocol or next header compared when enabled.
23:16	IP_NXT_HDR2	R/W	0h	The ~iip_nxt_hdr2 is the third protocol or next header compared when enabled.
15:8	IP_NXT_HDR1	R/W	0h	The ~iip_nxt_hdr1 is the second protocol or next header compared when enabled.
7:0	IP_NXT_HDR0	R/W	0h	The ~iip_nxt_hdr0 is the first protocol or next header compared when enabled.

14.9.2.1.346 CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register

CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register (Offset = 3E020h) [reset = 0h]

Register Description: The ALE table control register is used to read or write that ALE table entries. After writing to this register any read or write to any ALE register will be stalled until the read or write operation completes.

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Table 14-19199. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E020h

Figure 14-6343. CPSW3_CPSW_NU_ALE_ALE_TBLCTL Name Register

31	30	29	28	27	26	25	24
TABLEWR	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TABLEIDX
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TABLEIDX							
R/W							
0h							

Table 14-19201. CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TABLEWR	R/W	0h	Table Write - This bit is used to write the table words to the lookup table. 0 - Table Read Operation is performed. The contents of the ~b TABLEIDX entry will be read into the ~b ALE_TBLWx registers 1 - Table write operation is performed. This will take the current contents from the ~b ALE_TBLWx registers and write them to the table at the specified ~b TABLEIDX.
30:9	RESERVED	NONE	0h	Reserved
8:0	TABLEIDX	R/W	0h	The table index is used to determine which lookup table entry is read or written.

14.9.2.1.347 CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register

CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register (Offset = 3E034h) [reset = 0h]

Register Description: The ALE Table Word 2 is the most significant word of an ALE table entry.

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Table 14-19202. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E034h

Figure 14-6344. CPSW3_CPSW_NU_ALE_ALE_TBLW2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TABLEWRD2						
NONE	R/W						
0h	0h						

Table 14-19204. CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	TABLEWRD2	R/W	0h	Table Entry bits [70:64]

14.9.2.1.348 CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register

CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register (Offset = 3E038h) [reset = 0h]

Register Description: The ALE Table Word 1 is the middle word of an ALE table entry.

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Table 14-19205. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E038h

Figure 14-6345. CPSW3_CPSW_NU_ALE_ALE_TBLW1 Name Register

31	30	29	28	27	26	25	24
TABLEWRD1							
R/W							
0h							
23	22	21	20	19	18	17	16
TABLEWRD1							
R/W							
0h							
15	14	13	12	11	10	9	8
TABLEWRD1							
R/W							
0h							
7	6	5	4	3	2	1	0
TABLEWRD1							
R/W							
0h							

Table 14-19207. CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD1	R/W	0h	Table Entry bits [63:32]

14.9.2.1.349 CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register

CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register (Offset = 3E03Ch) [reset = 0h]

Register Description: The ALE Table Word 0 is the least significant word of an ALE table entry.

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Table 14-19208. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E03Ch

Figure 14-6346. CPSW3_CPSW_NU_ALE_ALE_TBLW0 Name Register

31	30	29	28	27	26	25	24
TABLEWRD0							
R/W							
0h							
23	22	21	20	19	18	17	16
TABLEWRD0							
R/W							
0h							
15	14	13	12	11	10	9	8
TABLEWRD0							
R/W							
0h							
7	6	5	4	3	2	1	0
TABLEWRD0							
R/W							
0h							

Table 14-19210. CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD0	R/W	0h	Table Entry bits [31:0]

14.9.2.1.350 CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register

CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register (Offset = 3E040h + formula) [reset = 0h]

Register Description: The ALE Port Control Register sets the port specific modes of operation.

Formula = (j * 4h); where j = 0 to 2d

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Table 14-19211. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E040h + formula

Figure 14-6347. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Name Register

31	30	29	28	27	26	25	24
I0_REG_P0_BCAST_LIMIT							
R/W							
0h							
23	22	21	20	19	18	17	16
I0_REG_P0_MCAST_LIMIT							
R/W							
0h							
15	14	13	12	11	10	9	8
I0_REG_P0_DROP_DOUBLE_VLAN	I0_REG_P0_DROP_DUAL_VLAN	I0_REG_P0_MACONLY_CAF	I0_REG_P0_DIS_PAUTHMOD	I0_REG_P0_MACONLY	I0_REG_P0_TRUNKEN	I0_REG_P0_TRUNKNUM	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
7	6	5	4	3	2	1	0
I0_REG_P0_MIRROR_SP	RESERVED	I0_REG_P0_NO_SA_UPDATE	I0_REG_P0_NO_LEARN	I0_REG_P0_VID_INGRESS_CHECK	I0_REG_P0_DROP_UN_TAGGED	I0_REG_P0_PORTSTATE	
R/W	NONE	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-19213. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	I0_REG_P0_BCAST_LIMIT	R/W	0h	Broadcast Packet Rate Limit. Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23:16	I0_REG_P0_MCAST_LIMIT	R/W	0h	Multicast Packet Rate Limit. Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.The Iy_REG_Py_MCAST_LIMIT bit field is the number of Multicast packets that will be forwarded per CPSW_ALE_PRESCALE time.

Table 14-19213. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	I0_REG_P0_DROP_DOUBLE_VLAN	R/W	0h	Drop Double VLAN. When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.
14	I0_REG_P0_DROP_DUAL_VLAN	R/W	0h	Drop Dual VLAN - When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.
13	I0_REG_P0_MACONLY_CAF	R/W	0h	Mac Only Copy All Frames. When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with Iy_REG_Py_MACONLY set.
12	I0_REG_P0_DIS_PAUTHMOD	R/W	0h	Disable Port authorization. When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.
11	I0_REG_P0_MACONLY	R/W	0h	MAC Only. When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the Iy_REG_Py_MACONLY bit set and the Iy_REG_Py_NO_LEARN also set. If Iy_REG_Py_MACONLY bit is set and the Iy_REG_Py_NO_LEARN is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that The host can broadcast to all ports including MacOnly ports in this mode.
10	I0_REG_P0_TRUNKEN	R/W	0h	Trunk Enable. This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the Iy_REG_Py_TRUNKEN its set and having the same Iy_REG_Py_TRUNKNUM will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never trasnmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry.
9:8	I0_REG_P0_TRUNKNUM	R/W	0h	Trunk Number. This field is used as the trunk number when the Iy_REG_Py_TRUNKEN is also set. Ports with the same trunk number that have the Iy_REG_Py_TRUNKEN also set will have traffic distributed within the trunk based on the result of the hash function descrived above.
7	I0_REG_P0_MIRROR_SP	R/W	0h	Mirror Source Port. This field enables the source port mirror option. When this bit is set any traffic received on the port with the Iy_REG_Py_MIRROR_SP bit set will have its received traffic also sent to the MIRROR_TOP port.
6	RESERVED	NONE	0h	Reserved
5	I0_REG_P0_NO_SA_UPDATE	R/W	0h	No Source Address Update. When set will not update the source addresses for this port.
4	I0_REG_P0_NO_LEARN	R/W	0h	No Learn. When set will not learn the source addresses for this port.
3	I0_REG_P0_VID_INGRESS_CHECK	R/W	0h	VLAN Ingress Check. When set if a packet received is not a member of the VLAN, the packet will be dropped.
2	I0_REG_P0_DROP_UNTAGGED	R/W	0h	If Drop Untagged. When set will drop packets without a VLAN tag.
1:0	I0_REG_P0_PORTSTATE	R/W	0h	Port State. Defines the current port state used for lookup operations. 0h Disabled 1h Blocked 2h Learning 3h Forwarding

14.9.2.1.351 CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register

CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register (Offset = 3E090h) [reset = 0h]

Register Description: The ALE Unknown VLAN Member Mask Register is used to specify the member list for unknown VLAN ID.

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Table 14-19214. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E090h

Figure 14-6348. CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					UVLAN_MEMBER_LIST		
NONE					R/W		
0h					0h		

Table 14-19216. CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_MEMBER_LIST	R/W	0h	Unknown VLAN Member List - Each bit represents the port member status for unknown VLANs.

14.9.2.1.352 CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register

CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register (Offset = 3E094h) [reset = 0h]

Register Description: The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is used to specify which egress ports unregistered multicast addresses egress for the unregistered VLAN ID.

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Table 14-19217. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E094h

Figure 14-6349. CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_UNREG_MCAST_FLOOD_MASK		
NONE					R/W		
0h					0h		

Table 14-19219. CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_UNREG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Unregister Multicast Flood Mask - Each bit represents the port to which unregistered multicast are sent for unregistered VLANs.

14.9.2.1.353 CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register

CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register (Offset = 3E098h) [reset = 0h]

Register Description: The ALE Unknown VLAN Registered Multicast Flood Mask Register is used to specify which egress ports registered multicast addresses egress for the unregistered VLAN ID.

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Table 14-19220. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E098h

Figure 14-6350. CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">UVLAN_REG_MCAST_FLOOD_MASK</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-19222. CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_REG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Register Multicast Flood Mask - Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs.

14.9.2.1.354 CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register

CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register (Offset = 3E09Ch) [reset = 0h]

Register Description: The ALE Unknown VLAN force Untagged Egress Mask Register is used to specify which egress ports the VLAN ID will be removed.

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Table 14-19223. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E09Ch

Figure 14-6351. CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_FORCE_UNTAGGED_EGRESS		
NONE					R/W		
0h					0h		

Table 14-19225. CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_FORCE_UNTAGGED_EGRESS	R/W	0h	Unknown VLAN Force Untagged Egress Mask - Each bit represents the port where the VLAN will be removed for unregistered VLANs.

14.9.2.1.355 CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register

CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register (Offset = 3E0B8h) [reset = 0h]

Register Description: The ALE Statistic Output Diagnostic Register allows the output statistics to diagnose the SW counters. This register is for diagnostice only.

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Table 14-19226. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E0B8h

Figure 14-6352. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PBCAST_DIAG	RESERVED					PORT_DIAG	
R/W	NONE					R/W	
0h	0h					0h	
7	6	5	4	3	2	1	0
RESERVED				STAT_DIAG			
NONE				R/W			
0h				0h			

Table 14-19228. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	PBCAST_DIAG	R/W	0h	When set and the ~iport_diag is set to zero, will allow all ports to see the same stat diagnostic increment.
14:10	RESERVED	NONE	0h	Reserved
9:8	PORT_DIAG	R/W	0h	The port selected that a received packet will cause the selected error to increment
7:4	RESERVED	NONE	0h	Reserved

Table 14-19228. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	STAT_DIAG	R/W	0h	When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port. 0: Disabled 1: Destination Equal Source Drop Stat will count 2: VLAN Ingress Check Drop Stat will count 3: Source Multicast Drop Stat will count 4: Dual VLAN Drop Stat will count 5: Ether Type length error Drop Stat will count 6: Next Hop Limit Drop Stat will count 7: IPv4 Fragment Drop Stat will count 8: Classifier Hit Stat will count 9: Classifier Red Drop Stat will count 10: Classifier Yellow Drop Stat will count 11: ALE Overflow Drop Stat will count 12: Rate Limit Drop Stat will count 13: Blocked Address Drop Stat will count 14: Secure Address Drop Stat will count 15: Authorization Drop Stat will count

14.9.2.1.356 CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register

CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register (Offset = 3E0BCh) [reset = 0h]

Register Description: The ALE OAM Control allows ports to be put into OAM Loopback, only non-supervisor packet are looped back to the source port.

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Table 14-19229. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E0BCh

Figure 14-6353. CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OAM_LB_CTRL		
NONE					R/W		
0h					0h		

Table 14-19231. CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OAM_LB_CTRL	R/W	0h	The ~ioam_lb_ctrl allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an egressop of 0xFF which swaps the source and destination address. BPDUs will still flow through as normal so that OAM can be remotly requested and disabled.

14.9.2.1.357 CPSW3_CPSW_NU_ALE_EGRESSOP Register

CPSW3_CPSW_NU_ALE_EGRESSOP Register (Offset = 3E0FCh) [reset = 0h]

Register Description: The Egress Operation register allows enabled classifiers with any match like IPSA or IPDA match to use the CPSW Egress Packet Operations Inter VLAN Routing sub functions. If the packet was destined for the host or is destined to any port without any errors, but matches a clasifier that has a programmed egress opcode, it will be forwarded to the destination ports where the destination ports will use the thier egress opcode entry to modify the packet. InterVLAN Routing and mirroring need to be understood, they are orthogonal functions. Care must be taken not to violate VLAN rules as this can redirect packets based on classifier matches.

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Table 14-19232. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E0FCh

Figure 14-6354. CPSW3_CPSW_NU_ALE_EGRESSOP Name Register

31	30	29	28	27	26	25	24
EGRESS_OP							
R/W							
0h							
23	22	21	20	19	18	17	16
EGRESS_TRK			TTL_CHECK	RESERVED			
R/W			R/W	NONE			
0h			0h	0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DEST_PORTS		
NONE					R/W		
0h					0h		

Table 14-19234. CPSW3_CPSW_NU_ALE_EGRESSOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EGRESS_OP	R/W	0h	The Egress Operation defines the operation performed by the CPSW Egress Packet Operations 0: NOP : 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load. 0xff: Swap SA and DA of packet, this is intended to allow OAM diagnostics for a link.
23:21	EGRESS_TRK	R/W	0h	The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.
20	TTL_CHECK	R/W	0h	The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.
19:3	RESERVED	NONE	0h	Reserved

Table 14-19234. CPSW3_CPSW_NU_ALE_EGRESSOP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DEST_PORTS	R/W	0h	The Destination Ports is a list of the ports the classified packet will be set to. If a destination is a Trunk, all the port bits for that trunck must be set.

14.9.2.1.358 CPSW3_CPSW_NU_ALE_POLICECFG0 Register

CPSW3_CPSW_NU_ALE_POLICECFG0 Register (Offset = 3E100h) [reset = 0h]

Register Description: The Policing Config 0 holds the port, frame priority and ONU address index as well as match enables for port, frame priority and ONU address matching.

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Table 14-19235. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E100h

Figure 14-6355. CPSW3_CPSW_NU_ALE_POLICECFG0 Name Register

31	30	29	28	27	26	25	24
PORT_MEN	TRUNKID	RESERVED			PORT_NUM		RESERVED
R/W	R/W	NONE			R/W		NONE
0h	0h	0h			0h		0h
23	22	21	20	19	18	17	16
RESERVED				PRI_MEN	PRI_VAL		
NONE				R/W	R/W		
0h				0h	0h		
15	14	13	12	11	10	9	8
ONU_MEN	RESERVED						ONU_INDEX
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
ONU_INDEX							
R/W							
0h							

Table 14-19237. CPSW3_CPSW_NU_ALE_POLICECFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PORT_MEN	R/W	0h	Port Match Enable - Enabled port match for the selected policing/ classifier entry
30	TRUNKID	R/W	0h	Trunk ID - When set indicates the port number is a trunk group.
29:27	RESERVED	NONE	0h	Reserved
26:25	PORT_NUM	R/W	0h	Port Number - Specifies the port address to match for the selected policing/classifier entry
24:20	RESERVED	NONE	0h	Reserved
19	PRI_MEN	R/W	0h	Priority Match Enable - Enables frame priority match for the selected policing/classifier entry
18:16	PRI_VAL	R/W	0h	Priority Value - Specifies the frame priority to match for the selected policing/classifier entry
15	ONU_MEN	R/W	0h	OUI Match Enable - Enables frame ONU address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	ONU_INDEX	R/W	0h	OUI Table Entry Index - Specifies the ALE ONU address lookup table index to match for the selected policing/classifier entry

14.9.2.1.359 CPSW3_CPSW_NU_ALE_POLICECFG1 Register

CPSW3_CPSW_NU_ALE_POLICECFG1 Register (Offset = 3E104h) [reset = 0h]

Register Description: The Policing Config 1 holds the match enable/match index for the L2 Destination and L2 source addresses

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Table 14-19238. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E104h

Figure 14-6356. CPSW3_CPSW_NU_ALE_POLICECFG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DST_MEN</td><td colspan="6">RESERVED</td><td>DST_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DST_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>SRC_MEN</td><td colspan="6">RESERVED</td><td>SRC_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SRC_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19240. CPSW3_CPSW_NU_ALE_POLICECFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DST_MEN	R/W	0h	Destination Address Match Enable - Enables frame L2 destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	DST_INDEX	R/W	0h	Destination Address Table Entry Index - Specifies the ALE L2 destination address lookup table index to match for the selected policing/classifier entry
15	SRC_MEN	R/W	0h	Source Address Match Enable - Enables frame L2 source address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	SRC_INDEX	R/W	0h	Source Address Table Entry Index - Specifies the ALE L2 source address lookup table index to match for the selected policing/classifier entry

14.9.2.1.360 CPSW3_CPSW_NU_ALE_POLICECFG2 Register

CPSW3_CPSW_NU_ALE_POLICECFG2 Register (Offset = 3E108h) [reset = 0h]

Register Description: The Policing Config 2 holds the match enable/match index for the Outer VLAN and Inner VLAN addresses

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Table 14-19241. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E108h

Figure 14-6357. CPSW3_CPSW_NU_ALE_POLICECFG2 Name Register

31	30	29	28	27	26	25	24
OVLAN_MEN	RESERVED						OVLAN_INDEX
R/W	NONE						R/W
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OVLAN_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IVLAN_MEN	RESERVED						IVLAN_INDEX
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IVLAN_INDEX							
R/W							
0h							

Table 14-19243. CPSW3_CPSW_NU_ALE_POLICECFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVLAN_MEN	R/W	0h	Outer VLAN Match Enable - Enables frame Outer VLAN address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	OVLAN_INDEX	R/W	0h	Outer VLAN Table Entry Index - Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/ classifier entry
15	IVLAN_MEN	R/W	0h	Inner VLAN Match Enable - Enables frame Inner VLAN address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	IVLAN_INDEX	R/W	0h	Inner VLAN Table Entry Index - Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/ classifier entry

14.9.2.1.361 CPSW3_CPSW_NU_ALE_POLICECFG3 Register

CPSW3_CPSW_NU_ALE_POLICECFG3 Register (Offset = 3E10Ch) [reset = 0h]

Register Description: The Policing Config 3 holds the match enable/match index for the Ether Type and IP Source address

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Table 14-19244. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E10Ch

Figure 14-6358. CPSW3_CPSW_NU_ALE_POLICECFG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>ETHERTYPE_MEN</td><td colspan="6">RESERVED</td><td>ETHERTYPE_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ETHERTYPE_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>IPSRC_MEN</td><td colspan="6">RESERVED</td><td>IPSRC_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IPSRC_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19246. CPSW3_CPSW_NU_ALE_POLICECFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ETHERTYPE_MEN	R/W	0h	EtherType Match Enable - Enables frame Ether Type match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	ETHERTYPE_INDEX	R/W	0h	EtherType Table Entry Index - Specifies the ALE Ether Type lookup table index to match for the selected policing/classifier entry
15	IPSRC_MEN	R/W	0h	IP Source Address Match Enable - Enables frame IP Source address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	IPSRC_INDEX	R/W	0h	IP Source Address Table Entry Index - Specifies the ALE IP Source address lookup table index to match for the selected policing/classifier entry

14.9.2.1.362 CPSW3_CPSW_NU_ALE_POLICECFG4 Register

CPSW3_CPSW_NU_ALE_POLICECFG4 Register (Offset = 3E110h) [reset = 0h]

Register Description: The Policing Config 4 holds the match enable/match index for the IP Destination address

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Table 14-19247. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E110h

Figure 14-6359. CPSW3_CPSW_NU_ALE_POLICECFG4 Name Register

31	30	29	28	27	26	25	24
IPDST_MEN	RESERVED						IPDST_INDEX
R/W	NONE						R/W
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPDST_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-19249. CPSW3_CPSW_NU_ALE_POLICECFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPDST_MEN	R/W	0h	IP Destination Address Match Enable - Enables frame IP Destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	IPDST_INDEX	R/W	0h	IP Destination Address Table Entry Index - Specifies the ALE IP Destination address lookup table index to match for the selected policing/classifier entry
15:0	RESERVED	NONE	0h	Reserved

14.9.2.1.363 CPSW3_CPSW_NU_ALE_POLICECFG6 Register

CPSW3_CPSW_NU_ALE_POLICECFG6 Register (Offset = 3E118h) [reset = 0h]

Register Description: The PIR counter is a 37 bit internal counter where ~ipir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED at LUT time. If the counter is negative the packet will be marked RED, else it can be YELLOW or GREEN based on the CIR counter. If only this counter is used (aka cir_idle_inc_val==0) Packet are marked RED or GREEN based on PIR counter only.

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Table 14-19250. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E118h

Figure 14-6360. CPSW3_CPSW_NU_ALE_POLICECFG6 Name Register

31	30	29	28	27	26	25	24
PIR_IDLE_INC_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
PIR_IDLE_INC_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
PIR_IDLE_INC_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
PIR_IDLE_INC_VAL							
R/W							
0h							

Table 14-19252. CPSW3_CPSW_NU_ALE_POLICECFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR_IDLE_INC_VAL	R/W	0h	Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED.

14.9.2.1.364 CPSW3_CPSW_NU_ALE_POLICECFG7 Register

CPSW3_CPSW_NU_ALE_POLICECFG7 Register (Offset = 3E11Ch) [reset = 0h]

Register Description: The CIR counter is a 37 bit internal counter where ~icir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED or YELLOW at LUT time. If the counter is positive the packet will be marked GREEN, else it can be YELLOW or RED based on the PIR counter. If only this counter is used (aka pir_idle_inc_val==0) Packet are marked YELLOW or GREEN based on CIR counter only.

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Table 14-19253. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E11Ch

Figure 14-6361. CPSW3_CPSW_NU_ALE_POLICECFG7 Name Register

31	30	29	28	27	26	25	24
CIR_IDLE_INC_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
CIR_IDLE_INC_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
CIR_IDLE_INC_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
CIR_IDLE_INC_VAL							
R/W							
0h							

Table 14-19255. CPSW3_CPSW_NU_ALE_POLICECFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR_IDLE_INC_VAL	R/W	0h	Committed Information Idle Increment Value - The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW.

14.9.2.1.365 CPSW3_CPSW_NU_ALE_POLICETBLCTL Register

CPSW3_CPSW_NU_ALE_POLICETBLCTL Register (Offset = 3E120h) [reset = 0h]

Register Description: The Policing Table Control is used to read or write the selected policing/classifier entry. The selected policing/classifier entry is only read or written after this register is written based on the value of the ~iwrite_enable bit.

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Table 14-19256. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E120h

Figure 14-6362. CPSW3_CPSW_NU_ALE_POLICETBLCTL Name Register

31	30	29	28	27	26	25	24
WRITE_ENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			POL_TBL_IDX				
NONE			R/W				
0h			0h				

Table 14-19258. CPSW3_CPSW_NU_ALE_POLICETBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRITE_ENABLE	R/W	0h	Write Enable - Setting this bit will write the POLICECFG0-7 to the ~ipol_tbl_idx selected policing/classifier entry. Clearing this bit will read the ~ipol_tbl_idx selected policing/classifier entry into the POLICECFG0-7 registers.
30:5	RESERVED	NONE	0h	Reserved
4:0	POL_TBL_IDX	R/W	0h	Policer Entry Index - This field specifies the policing/classifier entry to be read or written. When writing to this field without setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be loaded into the POLICECFG0-7 registers. When writing to this field with setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be updated from the POLICECFG0-7 registers.

14.9.2.1.366 CPSW3_CPSW_NU_ALE_POLICECONTROL Register

CPSW3_CPSW_NU_ALE_POLICECONTROL Register (Offset = 3E124h) [reset = 0h]

Register Description: The Control Enables color marking as well as internal ALE packet dropping rules.

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Table 14-19259. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E124h

Figure 14-6363. CPSW3_CPSW_NU_ALE_POLICECONTROL Name Register

31	30	29	28	27	26	25	24
POLICING_EN	RESERVED	RED_DROP_EN	YELLOW_DROP_EN	RESERVED	YELLOWTHRESH		
R/W	NONE	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		
23	22	21	20	19	18	17	16
POLMCHMODE		PRIORITY_THREAD_EN	MAC_ONLY_DEF_DIS	RESERVED			
R/W		R/W	R/W	NONE			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19261. CPSW3_CPSW_NU_ALE_POLICECONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLICING_EN	R/W	0h	Policing Enable - Enables the policing to color the packets, this also enables red or yellow drop capabilities.
30	RESERVED	NONE	0h	Reserved
29	RED_DROP_EN	R/W	0h	RED Drop Enable - Enables the ALE to drop the red colored packets.
28	YELLOW_DROP_EN	R/W	0h	WELLOW Drop Enable - Enables the ALE to drop yellow packets based on the ~iyellowthresh value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature.
27	RESERVED	NONE	0h	Reserved
26:24	YELLOWTHRESH	R/W	0h	Yellow Threshold - When set enables a portion of the yellow packets to be dropped based on the ~iyellow_drop_en enable. 0-100% 1=50% 2-33% 3-25% 4=20% 5-17% 6-14% 7-13%

Table 14-19261. CPSW3_CPSW_NU_ALE_POLICECONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	POLMCHMODE	R/W	0h	Policing Match Mode - This field determines what happens to packets that fail to hit any policing/classifier entry. 0 - No Hit packets are marked GREEN 1 - No Hit packets are marked YELLOW 2 - No Hit packets are marked RED 3 - No Hit packets are marked based on policing/classifier entry=0 state.
21	PRIORITY_THREAD_EN	R/W	0h	Priority Thread Enable - This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.
20	MAC_ONLY_DEF_DIS	R/W	0h	MAC Only Default Disable - This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}. If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.
19:0	RESERVED	NONE	0h	Reserved

14.9.2.1.367 CPSW3_CPSW_NU_ALE_POLICETESTCTL Register

CPSW3_CPSW_NU_ALE_POLICETESTCTL Register (Offset = 3E128h) [reset = 0h]

Register Description: The Policing Test Control enables the ability to determine which policing entry has been hit and whether they reported a red or yellow rate condition.

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Table 14-19262. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E128h

Figure 14-6364. CPSW3_CPSW_NU_ALE_POLICETESTCTL Name Register

31	30	29	28	27	26	25	24
POL_CLRALL_HIT	POL_CLRALL_REDHIT	POL_CLRALL_YELLOWHIT	POL_CLRSEL_ALL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			POL_TEST_IDX				
NONE			R/W				
0h			0h				

Table 14-19264. CPSW3_CPSW_NU_ALE_POLICETESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_CLRALL_HIT	R/W	0h	Policer Clear - This bit clears all the policing/classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/ classifier entry has been hit.
30	POL_CLRALL_REDHIT	R/W	0h	Policer Clear RED - This bit clears all the policing/classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.
29	POL_CLRALL_YELLOWHIT	R/W	0h	Policer Clear YELLOW - This bit clears all the policing/classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition.
28	POL_CLRSEL_ALL	R/W	0h	Police Clear Selected - This bit clears the selected policing/classifier hit, redhit and yellowhit bits. This bit is self clearing.
27:5	RESERVED	NONE	0h	Reserved
4:0	POL_TEST_IDX	R/W	0h	Policer Test Index - This field selects which policing/classifier hit bits will be read or written.

14.9.2.1.368 CPSW3_CPSW_NU_ALE_POLICEHSTAT Register

CPSW3_CPSW_NU_ALE_POLICEHSTAT Register (Offset = 3E12Ch) [reset = 0h]

Register Description: The policing hit status is a read only register that reads the hit bits of the selected policing/ classifier.

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Table 14-19265. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E12Ch

Figure 14-6365. CPSW3_CPSW_NU_ALE_POLICEHSTAT Name Register

31	30	29	28	27	26	25	24
POL_HIT	POL_REDHIT	POL_YELLOW HIT	RESERVED				
R	R	R	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-19267. CPSW3_CPSW_NU_ALE_POLICEHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_HIT	R	0h	Policer Hit - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit by a packet seen on any port that matches the policing/classifier entry match.
30	POL_REDHIT	R	0h	Policer Hit RED - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a RED condition by a packet seen on any port that matches the policing/classifier entry match.
29	POL_YELLOWHIT	R	0h	Policer Hit YELLOW - This indicates that the selected policing/ classifier via the ~ipol_test_idx field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/ classifier entry match.
28:0	RESERVED	NONE	0h	Reserved

14.9.2.1.369 CPSW3_CPSW_NU_ALE_THREADMAPDEF Register

CPSW3_CPSW_NU_ALE_THREADMAPDEF Register (Offset = 3E134h) [reset = 0h]

Register Description: The THREAD Mapping Default Value register is used to set the default thread ID when no classifier is matched,

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Table 14-19268. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E134h

Figure 14-6366. CPSW3_CPSW_NU_ALE_THREADMAPDEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DEFTHREAD_EN	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		DEFTHREADVAL					
NONE		R/W					
0h		0h					

Table 14-19270. CPSW3_CPSW_NU_ALE_THREADMAPDEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DEFTHREAD_EN	R/W	0h	Default Tread Enable - When set the switch will use the ~idefthreadval for the host interface thread ID if no classifier is matched. If clear the switch will generate its own thread ID based on port and priority if there is no classifier match.
14:6	RESERVED	NONE	0h	Reserved
5:0	DEFTHREADVAL	R/W	0h	Default Thread Value - This field specifies the default thread ID value.

14.9.2.1.370 CPSW3_CPSW_NU_ALE_THREADMAPCTL Register

CPSW3_CPSW_NU_ALE_THREADMAPCTL Register (Offset = 3E138h) [reset = 0h]

Register Description: The THREAD Mapping Control register allows the highest matched classifier to return a particular thread ID for traffic sent to the host. This allows particular classifier matched traffic to be placed an a particular hosts queue.

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Table 14-19271. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E138h

Figure 14-6367. CPSW3_CPSW_NU_ALE_THREADMAPCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			CLASSINDEX				
NONE			R/W				
0h			0h				

Table 14-19273. CPSW3_CPSW_NU_ALE_THREADMAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	CLASSINDEX	R/W	0h	Classifier Index - This is the classifier index entry that the thread enable and thread value will be read or written by the ~bTHREADMAPVAL register.

14.9.2.1.371 CPSW3_CPSW_NU_ALE_THREADMAPVAL Register

CPSW3_CPSW_NU_ALE_THREADMAPVAL Register (Offset = 3E13Ch) [reset = 0h]

Register Description: The THREAD Mapping Value register is used to set the thread ID for a particular classifier entry.

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Table 14-19274. Instance Table

Instance Name	Physical Address
CPSW0_cpsw3	0803 E13Ch

Figure 14-6368. CPSW3_CPSW_NU_ALE_THREADMAPVAL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>THREAD_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">THREADVAL</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-19276. CPSW3_CPSW_NU_ALE_THREADMAPVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	THREAD_EN	R/W	0h	Thread Enable - When set the switch will use the ~ithreadval for the selected classifier match. If clear the the thread ID will be determined by the ~bTHREADMAPDEF register settings.
14:6	RESERVED	NONE	0h	Reserved
5:0	THREADVAL	R/W	0h	Thread Value - This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.

14.9.2.2 PCIe

PCIe

14.9.2.2.1 PCIe Summaries

PCIe Summaries

Table 14-19277. ECC_AGGR Registers, Base Address=0071 8000h, Length=1024

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	ECC_AGGR_REV	0071 8000h
8h	32	ECC_AGGR_VECTOR	0071 8008h
Ch	32	ECC_AGGR_STAT	0071 800Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 8010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 803Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 8040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 8080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 80C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 813Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 8140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 8180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 81C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 8200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 8204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 8208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 820Ch

Table 14-19278. ECC_AGGR Registers, Base Address=0071 9000h, Length=1024

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	ECC_AGGR_REV	0071 9000h
8h	32	ECC_AGGR_VECTOR	0071 9008h
Ch	32	ECC_AGGR_STAT	0071 900Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 9010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 903Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 9040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 9080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 90C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 913Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 9140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 9180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 91C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 9200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 9204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 9208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 920Ch

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_VENDOR_ID_DEVICE_ID	0D00 0000h
4h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_COMMAND_STATUS	0D00 0004h
8h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_REVISION_ID_CLASS_CODE	0D00 0008h
Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_BIST_HEADER_LATENCY_CACHE_LINE	0D00 000Ch
10h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_0	0D00 0010h
14h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_1	0D00 0014h
18h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_BUS_NUMBERS	0D00 0018h
1Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT	0D00 001Ch
20h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_MEM_BASE_LIMIT	0D00 0020h
24h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_LIMIT	0D00 0024h
28h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_UPPER	0D00 0028h
2Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_LIMIT_UPPER	0D00 002Ch
30h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT_UPPER	0D00 0030h
34h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_CAPABILITIES_POINTER	0D00 0034h
38h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_RSVD_0E	0D00 0038h
3Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_INTRPT_LINE_INTRPT_PIN	0D00 003Ch
80h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CAP	0D00 0080h
84h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CTRL_STAT_REP	0D00 0084h
90h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_CTRL_REG	0D00 0090h
94h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_LOW_ADDR	0D00 0094h
98h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_HI_ADDR	0D00 0098h
9Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_DATA	0D00 009Ch
A0h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MASK	0D00 00A0h
A4h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_PENDING_BITS	0D00 00A4h
B0h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_CTRL	0D00 00B0h
B4h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_TBL_OFFSET	0D00 00B4h
B8h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_PENDING_INTRPT	0D00 00B8h
C0h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_LIST	0D00 00C0h
C4h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP	0D00 00C4h
C8h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS	0D00 00C8h
CCh	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP	0D00 00CCh

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
D0h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS	0D00 00D0h
D4h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CAPABILITY	0D00 00D4h
D8h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CTRL_STATUS	0D00 00D8h
DCh	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_CTRL_CAP	0D00 00DCh
E0h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_STATUS	0D00 00E0h
E4h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_2	0D00 00E4h
E8h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS_2	0D00 00E8h
ECh	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP_2	0D00 00ECh
F0h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS_2	0D00 00F0h
100h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_AER_ENHNCD_CAP	0D00 0100h
104h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_STATUS	0D00 0104h
108h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_MASK	0D00 0108h
10Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_SEVERITY	0D00 010Ch
110h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_STATUS	0D00 0110h
114h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_MASK	0D00 0114h
118h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_ADV_ERR_CAP_CTL	0D00 0118h
11Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_0	0D00 011Ch
120h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_1	0D00 0120h
124h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_2	0D00 0124h
128h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_3	0D00 0128h
12Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_CMD	0D00 012Ch
130h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_STAT	0D00 0130h
134h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_ERR_SRC_ID	0D00 0134h
138h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_TLP_PRE_LOG_0	0D00 0138h
150h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_CAP_HDR	0D00 0150h
154h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_0	0D00 0154h
158h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_1	0D00 0158h
300h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_SEC_PCIE_CAP_HDR_REG	0D00 0300h
304h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CONTROL3	0D00 0304h
308h	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_ERROR_STATUS	0D00 0308h
30Ch	32	PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_EQUALIZATION_CONTROL_0	0D00 030Ch

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_ENH_CAP_HEADER_REG	0D00 0000h
4h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_1	0D00 0004h
8h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_2	0D00 0008h
Ch	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CTRL_STS_REG	0D00 000Ch
10h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_0	0D00 0010h
14h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_0	0D00 0014h
18h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_0	0D00 0018h
1Ch	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_1	0D00 001Ch
20h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_1	0D00 0020h
24h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_1	0D00 0024h
28h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_2	0D00 0028h
2Ch	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_2	0D00 002Ch
30h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_2	0D00 0030h
34h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_3	0D00 0034h
38h	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_3	0D00 0038h
3Ch	32	PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_3	0D00 003Ch
0h	32	PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_EXT_CAP_HDR	0D00 0000h
4h	32	PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CAP	0D00 0004h
8h	32	PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_1	0D00 0008h
Ch	32	PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_2	0D00 000Ch
0h	32	PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG	0D00 0000h
4h	32	PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CAPABILITIES_REG	0D00 0004h
8h	32	PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CONTROL_REG	0D00 0008h
0h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_0_REG	0D00 0000h
4h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_1_REG	0D00 0004h
8h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DLL_TMR_CONFIG_REG	0D00 0008h

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG	0D00 000Ch
10h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG	0D00 0010h
14h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG	0D00 0014h
18h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG	0D00 0018h
1Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG	0D00 001Ch
20h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG	0D00 0020h
24h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L0S_TIMEOUT_LIMIT_REG	0D00 0024h
28h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_COUNT_REG	0D00 0028h
2Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG	0D00 002Ch
30h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_COUNT_REG	0D00 0030h
34h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG	0D00 0034h
38h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_0_REG	0D00 0038h
3Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_1_REG	0D00 003Ch
40h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L1_ST_REENTRY_DELAY_REG	0D00 0040h
44h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_ID_REG	0D00 0044h
48h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG	0D00 0048h
4Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_TURNOFF_ACK_DELAY_REG	0D00 004Ch
50h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINKWIDTH_CONTROL_REG	0D00 0050h
54h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_2_REG	0D00 0054h
70h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_MULTI_VC_CONROL_REG	0D00 0070h
74h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SRIS_CONTROL_REG	0D00 0074h
80h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC1	0D00 0080h
84h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC1	0D00 0084h
88h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC1	0D00 0088h
8Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC1	0D00 008Ch
90h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC2	0D00 0090h

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
94h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC2	0D00 0094h
98h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC2	0D00 0098h
9Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC2	0D00 009Ch
A0h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC3	0D00 00A0h
A4h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC3	0D00 00A4h
A8h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC3	0D00 00A8h
ACh	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC3	0D00 00ACh
F0h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_FC_INIT_DELAY_REG	0D00 00F0h
100h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_0_REG	0D00 0100h
104h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_1_REG	0D00 0104h
108h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_2_REG	0D00 0108h
10Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_3_REG	0D00 010Ch
110h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_FUNC_NUM_REG	0D00 0110h
114h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_UR_ERR_REG	0D00 0114h
140h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PM_CLK_FREQUENCY_REG	0D00 0140h
144h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN1_REG	0D00 0144h
148h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN2_REG	0D00 0148h
14Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN3_REG	0D00 014Ch
158h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_DEFINED_MESSAGE_TAG_REG	0D00 0158h
200h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_NEGOTIATED_LANE_MAP_REG	0D00 0200h
204h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_FTS_COUNT_REG	0D00 0204h
208h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_REG	0D00 0208h
20Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_REGISTER	0D00 020Ch
210h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_REG	0D00 0210h
214h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LCRC_ERR_COUNT_REG	0D00 0214h
218h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG	0D00 0218h

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
21Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_SNOOP_LAT_REG	0D00 021Ch
220h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_MSG_GEN_CTL_REG	0D00 0220h
224h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_SERVICE_TIMEOUT_DELAY_REG	0D00 0224h
228h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ROOT_PORT_REQUESTOR_ID_REG	0D00 0228h
22Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EP_BUS_DEVICE_NUMBER_REG	0D00 022Ch
234h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_2_REG	0D00 0234h
238h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PHY_STATUS_1_REG	0D00 0238h
23Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_3_REG	0D00 023Ch
300h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RC_BAR_CONFIG_REG	0D00 0300h
360h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_DEFAULT_PRESET_REG	0D00 0360h
364h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_TIMEOUT_2MS_REG	0D00 0364h
368h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PIPE_FIFO_LATENCY_CTRL_REG	0D00 0368h
37Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_CTRL_REG	0D00 037Ch
380h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0	0D00 0380h
C80h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG_AXI	0D00 0C80h
C88h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL0	0D00 0C88h
C8Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL1	0D00 0C8Ch
C90h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL2	0D00 0C90h
C94h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_TL_INTERNAL_CONTROL	0D00 0C94h
D00h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_2_REGISTER	0D00 0D00h
D04h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_2_REG	0D00 0D04h
DA0h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LD_CTRL	0D00 0DA0h
DA4h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_RX_ELEC_IDLE_FILTER_CONTROL	0D00 0DA4h
DA8h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_CONTROL_REG	0D00 0DA8h
DACh	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_STATUS_REG	0D00 0DACh
DB0h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_INDEX_REG	0D00 0DB0h
DB4h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_REG	0D00 0DB4h

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
DB8h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_1_REG	0D00 0DB8h
DBCh	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_2_REG	0D00 0DBCh
DC0h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_3_REG	0D00 0DC0h
DC4h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_4_REG	0D00 0DC4h
DC8h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_5_REG	0D00 0DC8h
DCCh	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_6_REG	0D00 0DCCh
DD0h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_7_REG	0D00 0DD0h
DD4h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_8_REG	0D00 0DD4h
DD8h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_9_REG	0D00 0DD8h
DDCh	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_10_REG	0D00 0DDCh
DE0h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_11_REG	0D00 0DE0h
E4Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_CONTROL_REG	0D00 0E4Ch
E50h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS0_REG	0D00 0E50h
E54h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS_REG	0D00 0E54h
E5Ch	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_AXI_FEATURE_REG	0D00 0E5Ch
E60h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINK_EQ_CONTROL_2_REG	0D00 0E60h
E64h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_CORE_FEATURE_REG	0D00 0E64h
E88h	32	PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RX_INVERT_POLARITY_REG	0D00 0E88h
0h	32	PCIE_CORE_ATU_WRAPPER_OB_0_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_0_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_0_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_0_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_0_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_1_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_1_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_1_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_1_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_1_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_2_ADDR0	0D00 0000h

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
4h	32	PCIE_CORE_ATU_WRAPPER_OB_2_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_2_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_2_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_2_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_3_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_3_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_3_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_3_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_3_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_4_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_4_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_4_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_4_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_4_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_5_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_5_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_5_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_5_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_5_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_6_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_6_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_6_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_6_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_6_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_7_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_7_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_7_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_7_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_7_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_8_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_8_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_8_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_8_DESC1	0D00 000Ch

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
14h	32	PCIE_CORE_ATU_WRAPPER_OB_8_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_9_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_9_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_9_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_9_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_9_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_10_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_10_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_10_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_10_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_10_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_11_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_11_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_11_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_11_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_11_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_12_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_12_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_12_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_12_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_12_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_13_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_13_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_13_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_13_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_13_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_14_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_14_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_14_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_14_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_14_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR1	0D00 001Ch

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	PCIE_CORE_ATU_WRAPPER_OB_15_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_15_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_15_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_15_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_15_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_16_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_16_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_16_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_16_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_16_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_17_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_17_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_17_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_17_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_17_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_18_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_18_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_18_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_18_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_18_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_19_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_19_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_19_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_19_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_19_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_20_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_20_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_20_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_20_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_20_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_21_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_21_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_21_DESC0	0D00 0008h

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_21_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_21_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_22_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_22_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_22_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_22_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_22_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_23_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_23_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_23_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_23_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_23_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_24_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_24_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_24_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_24_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_24_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_25_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_25_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_25_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_25_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_25_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_26_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_26_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_26_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_26_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_26_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_27_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_27_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_27_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_27_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_27_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR0	0D00 0018h

Table 14-19279. PCIE_CORE Registers, Base Address=0D00 0000h, Length=8388608 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_28_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_28_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_28_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_28_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_28_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_29_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_29_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_29_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_29_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_29_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_30_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_30_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_30_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_30_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_30_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_OB_31_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_OB_31_ADDR1	0D00 0004h
8h	32	PCIE_CORE_ATU_WRAPPER_OB_31_DESC0	0D00 0008h
Ch	32	PCIE_CORE_ATU_WRAPPER_OB_31_DESC1	0D00 000Ch
14h	32	PCIE_CORE_ATU_WRAPPER_OB_31_DESC3	0D00 0014h
18h	32	PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR0	0D00 0018h
1Ch	32	PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR1	0D00 001Ch
0h	32	PCIE_CORE_ATU_WRAPPER_IB_0_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_IB_0_ADDR1	0D00 0004h
0h	32	PCIE_CORE_ATU_WRAPPER_IB_1_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_IB_1_ADDR1	0D00 0004h
0h	32	PCIE_CORE_ATU_WRAPPER_IB_7_ADDR0	0D00 0000h
4h	32	PCIE_CORE_ATU_WRAPPER_IB_7_ADDR1	0D00 0004h
0h	32	PCIE_CORE_ATU_CREDIT_THRESHOLD_C0	0D00 0000h
0h	32	PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0	0D00 0000h

Table 14-19280. USER_CFG Registers, Base Address=0F10 0000h, Length=1024

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	USER_CFG_REVID	0F10 0000h
4h	32	USER_CFG_CMD_STATUS	0F10 0004h
8h	32	USER_CFG_RSTCMD	0F10 0008h
Ch	32	USER_CFG_INITCFG	0F10 000Ch

Table 14-19280. USER_CFG Registers, Base Address=0F10 0000h, Length=1024 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
10h	32	USER_CFG_PMCMD	0F10 0010h
14h	32	USER_CFG_LINKSTATUS	0F10 0014h
18h	32	USER_CFG_LEGACY_INTR_SET	0F10 0018h
1Ch	32	USER_CFG_LEGACY_INT_PENDING	0F10 001Ch
20h	32	USER_CFG_MSI_STAT	0F10 0020h
24h	32	USER_CFG_MSI_VECTOR	0F10 0024h
28h	32	USER_CFG_MSI_MASK_PF0	0F10 0028h
40h	32	USER_CFG_MSI_PENDING_STATUS_PF0	0F10 0040h
A4h	32	USER_CFG_MSIX_STAT	0F10 00A4h
A8h	32	USER_CFG_MSIX_MASK	0F10 00A8h
B4h	32	USER_CFG_FLR_DONE	0F10 00B4h
BCh	32	USER_CFG_PTM_CFG	0F10 00BCh
C0h	32	USER_CFG_PTM_TIMER_LOW	0F10 00C0h
C4h	32	USER_CFG_PTM_TIMER_HIGH	0F10 00C4h
C8h	32	USER_CFG_EOI_VECTOR	0F10 00C8h

Table 14-19281. VMAP Registers, Base Address=0F10 1000h, Length=4096

Offset	Length	Register Name	PCIE0 Physical Address
400h	32	VMAP_OB_VIRTID_MATCH	0F10 1400h
0h	32	VMAP_EXT_DESC_J	0F10 1000h + formula

Table 14-19282. INTD_CFG Registers, Base Address=0F10 2000h, Length=4096

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	INTD_CFG_REVISION	0F10 2000h
100h	32	INTD_CFG_ENABLE_REG_SYS_0	0F10 2100h
104h	32	INTD_CFG_ENABLE_REG_SYS_1	0F10 2104h
108h	32	INTD_CFG_ENABLE_REG_SYS_2	0F10 2108h
300h	32	INTD_CFG_ENABLE_CLR_REG_SYS_0	0F10 2300h
304h	32	INTD_CFG_ENABLE_CLR_REG_SYS_1	0F10 2304h
308h	32	INTD_CFG_ENABLE_CLR_REG_SYS_2	0F10 2308h
500h	32	INTD_CFG_STATUS_REG_SYS_0	0F10 2500h
504h	32	INTD_CFG_STATUS_REG_SYS_1	0F10 2504h
508h	32	INTD_CFG_STATUS_REG_SYS_2	0F10 2508h
708h	32	INTD_CFG_STATUS_CLR_REG_SYS_2	0F10 2708h
A80h	32	INTD_CFG_INTR_VECTOR_REG_SYS	0F10 2A80h

Table 14-19283. CPTS Registers, Base Address=0F10 3000h, Length=1024

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	CPTS_IDVER_REG	0F10 3000h
4h	32	CPTS_CONTROL_REG	0F10 3004h
8h	32	CPTS_RFTCLK_SEL_REG	0F10 3008h
Ch	32	CPTS_TS_PUSH_REG	0F10 300Ch
10h	32	CPTS_TS_LOAD_VAL_REG	0F10 3010h

Table 14-19283. CPTS Registers, Base Address=0F10 3000h, Length=1024 (continued)

Offset	Length	Register Name	PCIE0 Physical Address
14h	32	CPTS_TS_LOAD_EN_REG	0F10 3014h
18h	32	CPTS_TS_COMP_VAL_REG	0F10 3018h
1Ch	32	CPTS_TS_COMP_LEN_REG	0F10 301Ch
20h	32	CPTS_INTSTAT_RAW_REG	0F10 3020h
24h	32	CPTS_INTSTAT_MASKED_REG	0F10 3024h
28h	32	CPTS_INT_ENABLE_REG	0F10 3028h
2Ch	32	CPTS_TS_COMP_NUDGE_REG	0F10 302Ch
30h	32	CPTS_EVENT_POP_REG	0F10 3030h
34h	32	CPTS_EVENT_0_REG	0F10 3034h
38h	32	CPTS_EVENT_1_REG	0F10 3038h
3Ch	32	CPTS_EVENT_2_REG	0F10 303Ch
40h	32	CPTS_EVENT_3_REG	0F10 3040h
44h	32	CPTS_TS_LOAD_HIGH_VAL_REG	0F10 3044h
48h	32	CPTS_TS_COMP_HIGH_VAL_REG	0F10 3048h
4Ch	32	CPTS_TS_ADD_VAL_REG	0F10 304Ch
50h	32	CPTS_TS_PPM_LOW_VAL_REG	0F10 3050h
54h	32	CPTS_TS_PPM_HIGH_VAL_REG	0F10 3054h
58h	32	CPTS_TS_NUDGE_VAL_REG	0F10 3058h
D0h	32	CPTS_TS_CONFIG	0F10 30D0h
0h	32	CPTS_TS_GENF_COMP_LOW_REG	0F10 3000h
4h	32	CPTS_TS_GENF_COMP_HIGH_REG	0F10 3004h
8h	32	CPTS_TS_GENF_CONTROL_REG	0F10 3008h
Ch	32	CPTS_TS_GENF_LENGTH_REG	0F10 300Ch
10h	32	CPTS_TS_GENF_PPM_LOW_REG	0F10 3010h
14h	32	CPTS_TS_GENF_PPM_HIGH_REG	0F10 3014h
18h	32	CPTS_TS_GENF_NUDGE_REG	0F10 3018h
0h	32	CPTS_TS_ESTF_COMP_LOW_REG	0F10 3000h
4h	32	CPTS_TS_ESTF_COMP_HIGH_REG	0F10 3004h
8h	32	CPTS_TS_ESTF_CONTROL_REG	0F10 3008h
Ch	32	CPTS_TS_ESTF_LENGTH_REG	0F10 300Ch
10h	32	CPTS_TS_ESTF_PPM_LOW_REG	0F10 3010h
14h	32	CPTS_TS_ESTF_PPM_HIGH_REG	0F10 3014h
18h	32	CPTS_TS_ESTF_NUDGE_REG	0F10 3018h

Table 14-19284. PCIE_DAT0 Registers, Base Address=6800 0000h, Length=134217728

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	PCIE_DAT0_PCIE_DATA_MEM_J	6800 0000h + formula

Table 14-19285. PCIE_DAT1 Registers, Base Address=0006 0000 0000h, Length=4294967296

Offset	Length	Register Name	PCIE0 Physical Address
0h	32	PCIE_DAT1_PCIE_DATA_MEM_J	0006 0000 0000h + formula

14.9.2.2.2 PCIe Registers

PCIe Registers

14.9.2.2.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-19286. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9000h**

Figure 14-6369. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">5h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-19288. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.2.2.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-19289. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9008h**

Figure 14-6370. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19291. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.2.2.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

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Table 14-19292. Instance Table

Instance Name	Physical Address
PCIE0	**0071 900Ch**

Figure 14-6371. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					4h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
4h							

Table 14-19294. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.2.2.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-19295. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9010h + formula**

Figure 14-6372. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19297. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.2.2.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-19298. Instance Table

Instance Name	Physical Address
PCIE0	0071 903Ch

Figure 14-6373. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19300. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.2.2.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-19301. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9040h**

Figure 14-6374. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_PEND	RPLYBUF_RAMECC_PEND	RXCPLFIFO_RAMECC_PEND	PNPFIFO_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-19303. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pnpfifo_ramecc_pend

14.9.2.2.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-19304. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9080h**

Figure 14-6375. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_ENABLE_SET	RPLYBUF_RAMECC_ENABLE_SET	RXCPLFIFO_RAMECC_ENABLE_SET	PNPFIFO_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-19306. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pnpfifo_ramecc_pend

14.9.2.2.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19307. Instance Table

Instance Name	Physical Address
PCIE0	**0071 90C0h**

Figure 14-6376. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_ENABLE_CLR	RPLYBUF_RAMECC_ENABLE_CLR	RXCPLFIFO_RAMECC_ENABLE_CLR	PNPFIFO_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-19309. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pnpfifo_ramecc_pend

14.9.2.2.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-19310. Instance Table

Instance Name	Physical Address
PCIE0	**0071 913Ch**

Figure 14-6377. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19312. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.2.2.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19313. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9140h**

Figure 14-6378. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_PEND	RPLYBUF_RAMECC_PEND	RXCPLFIFO_RAMECC_PEND	PNPFIFO_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-19315. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pnpfifo_ramecc_pend

14.9.2.2.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19316. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9180h**

Figure 14-6379. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>AXISRODR_RAMECC_ENABLE_SET</td><td>RPLYBUF_RAMECC_ENABLE_SET</td><td>RXCPLFIFO_RAMECC_ENABLE_SET</td><td>PNPFIFO_RAMECC_ENABLE_SET</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-19318. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pnpfifo_ramecc_pend

14.9.2.2.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19319. Instance Table

Instance Name	Physical Address
PCIE0	**0071 91C0h**

Figure 14-6380. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_ENABLE_CLR	RPLYBUF_RAMECC_ENABLE_CLR	RXCPLFIFO_RAMECC_ENABLE_CLR	PNPFIFO_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-19321. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pnpfifo_ramecc_pend

14.9.2.2.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-19322. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9200h**

Figure 14-6381. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-19324. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.2.2.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-19325. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9204h**

Figure 14-6382. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-19327. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.2.2.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-19328. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9208h**

Figure 14-6383. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-19330. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.2.2.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-19331. Instance Table

Instance Name	Physical Address
PCIE0	**0071 920Ch**

Figure 14-6384. ECC_AGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-19333. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.2.2.2.17 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-19334. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9000h**

Figure 14-6385. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
5h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-19336. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.2.2.2.18 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-19337. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9008h**

Figure 14-6386. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-19339. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.2.2.2.19 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

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Table 14-19340. Instance Table

Instance Name	Physical Address
PCIE0	**0071 900Ch**

Figure 14-6387. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					4h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
4h							

Table 14-19342. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.2.2.2.20 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-19343. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9010h + formula**

Figure 14-6388. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19345. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.2.2.2.21 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-19346. Instance Table

Instance Name	Physical Address
PCIE0	**0071 903Ch**

Figure 14-6389. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19348. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.2.2.2.22 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19349. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9040h**

Figure 14-6390. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_PEND	RPLYBUF_RAMECC_PEND	RXCPLFIFO_RAMECC_PEND	PNPFIFO_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-19351. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pnpfifo_ramecc_pend

14.9.2.2.2.23 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19352. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9080h**

Figure 14-6391. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				AXISRODR_RAMECC_ENABLE_SET	RPLYBUF_RAMECC_ENABLE_SET	RXCPLFIFO_RAMECC_ENABLE_SET	PNPFIFO_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-19354. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pnpfifo_ramecc_pend

14.9.2.2.2.24 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19355. Instance Table

Instance Name	Physical Address
PCIE0	**0071 90C0h**

Figure 14-6392. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_ENABLE_CLR	RPLYBUF_RAMECC_ENABLE_CLR	RXCPLFIFO_RAMECC_ENABLE_CLR	PNPFIFO_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-19357. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pnpfifo_ramecc_pend

14.9.2.2.2.25 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-19358. Instance Table

Instance Name	Physical Address
PCIE0	**0071 913Ch**

Figure 14-6393. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-19360. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.2.2.2.26 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-19361. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9140h**

Figure 14-6394. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_PEND	RPLYBUF_RAMECC_PEND	RXCPLFIFO_RAMECC_PEND	PNPFIFO_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-19363. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pnpfifo_ramecc_pend

14.9.2.2.2.27 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-19364. Instance Table

Instance Name	**Physical Address**
PCIE0	**0071 9180h**

Figure 14-6395. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_ENABLE_SET	RPLYBUF_RAMECC_ENABLE_SET	RXCPLFIFO_RAMECC_ENABLE_SET	PNPFIFO_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-19366. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pnpfifo_ramecc_pend

14.9.2.2.2.28 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-19367. Instance Table

Instance Name	Physical Address
PCIE0	**0071 91C0h**

Figure 14-6396. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				AXISRODR_RAMECC_ENABLE_CLR	RPLYBUF_RAMECC_ENABLE_CLR	RXCPLFIFO_RAMECC_ENABLE_CLR	PNPFIFO_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-19369. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	AXISRODR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for axisrodr_ramecc_pend
2	RPLYBUF_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rplybuf_ramecc_pend
1	RXCPLFIFO_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rxcplfifo_ramecc_pend
0	PNPFIFO_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pnpfifo_ramecc_pend

14.9.2.2.2.29 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-19370. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9200h**

Figure 14-6397. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-19372. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.2.2.2.30 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-19373. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9204h**

Figure 14-6398. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-19375. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.2.2.2.31 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-19376. Instance Table

Instance Name	Physical Address
PCIE0	**0071 9208h**

Figure 14-6399. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-19378. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.2.2.2.32 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-19379. Instance Table

Instance Name	Physical Address
PCIE0	**0071 920Ch**

Figure 14-6400. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-19381. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.2.2.2.33 PCIE_CORE_RC_I_RC_PCIE_BASE_I_VENDOR_ID_DEVICE_ID Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_VENDOR_ID_DEVICE_ID Register (Offset = 0h) [reset = 10017CDh]

16-bit Vendor ID register and 16-bit Device ID register.

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Table 14-19382. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6401. PCIE_CORE_RC_I_RC_PCIE_BASE_I_VENDOR_ID_DEVICE_ID Name Register

31	30	29	28	27	26	25	24
DID							
R							
100h							
23	22	21	20	19	18	17	16
DID							
R							
100h							
15	14	13	12	11	10	9	8
VID							
R							
17CDh							
7	6	5	4	3	2	1	0
VID							
R							
17CDh							

Table 14-19384. PCIE_CORE_RC_I_RC_PCIE_BASE_I_VENDOR_ID_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DID	R	100h	Device ID assigned by the manufacturer of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
15:0	VID	R	17CDh	This is the Vendor ID assigned by PCI SIG to the manufacturer of the device. The Vendor ID is set in the Vendor ID Register within the local management register block.

14.9.2.2.2.34 PCIE_CORE_RC_I_RC_PCIE_BASE_I_COMMAND_STATUS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_COMMAND_STATUS Register (Offset = 4h) [reset = 100000h]

16-bit Command Register and 16-bit Status Register.

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Table 14-19385. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6402. PCIE_CORE_RC_I_RC_PCIE_BASE_I_COMMAND_STATUS Name Register

31	30	29	28	27	26	25	24
DPE	SSE	RMA	RTA	STA	R6		MDPE
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R		R/W1TC
0h	0h	0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R5			CL	IS	R4		
R			R	R	R		
0h			1h	0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R3					IMD	R2	SE
R					R/W	R	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R1	PERE	R0			BE	MSE	ISE
R	R/W	R			R/W	R/W	R/W
0h	0h	0h			0h	0h	0h

Table 14-19387. PCIE_CORE_RC_I_RC_PCIE_BASE_I_COMMAND_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DPE	R/W1TC	0h	This bit is set when the Controller has received a poisoned TLP. The Parity Error Response enable bit [bit 6] has no effect on the setting of this bit. This field can also be cleared from the local management bus APB by writing a 1 into this bit position. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
30	SSE	R/W1TC	0h	The Controller sets this bit [i]On receiving an error message from the link, if SERR-Enable in PCI Command Register is 1 and SERR-Enable in the Bridge Control Register is also 1. [ii]On any internal Fatal/Non-Fatal error detected, if SERR-Enable in PCI Command Register is 1. This field can also be cleared from the local management APB bus by writing a 1 into this bit position. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 14-19387. PCIE_CORE_RC_I_RC_PCIE_BASE_I_COMMAND_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	RMA	R/W1TC	0h	This bit is set when the Controller has received a completion from the link with the Unsupported Request status. This field can also be cleared from the local management APB bus by writing a 1 into this bit position This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
28	RTA	R/W1TC	0h	This bit is set when the Controller has received a completion from the link with the Completer Abort status. This field can also be cleared from the local management APB bus by writing a 1 into this bit position. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
27	STA	R/W1TC	0h	This bit is set when the Controller has sent a completion to the link with the Completer Abort status. This field can also be cleared from the local management APB bus by writing a 1 into this bit position. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
26:25	R6	R	0h	Reserved
24	MDPE	R/W1TC	0h	When the Parity Error Response enable bit is 1, the Controller sets this bit when it detects the following error conditions: [i] The Controller receives a poisoned request from the link. [ii] The Controller has sent a Poisoned Completion downstream to the link This bit remains 0 when the Parity Error Response enable bit is 0. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
23:21	R5	R	0h	Reserved
20	CL	R	1h	Indicates the presence of PCI Extended Capabilities registers. This bit is hardwired to 1.
19	IS	R	0h	This bit is valid only when the Controller is configured to support legacy interrupts. Indicates that the Controller has a pending interrupt, that is, the Controller has sent an Assert_INTx message but has not transmitted a corresponding Deassert_INTx message.
18:16	R4	R	0h	Reserved
15:11	R3	R	0h	Reserved
10	IMD	R/W	0h	Enables or disables the transmission of INTx Assert and De-assert messages from the Controller. The setting of this bit has no effect on the operation of the Controller in the RC mode.
9	R2	R	0h	Reserved
8	SE	R/W	0h	Enables the reporting of fatal and non-fatal errors detected by the Controller to the Root Complex.
7	R1	R	0h	Reserved

Table 14-19387. PCIE_CORE_RC_I_RC_PCIE_BASE_I_COMMAND_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PERE	R/W	0h	When this bit is 1, the Controller sets the Master Data Parity Error status bit when it detects the following error conditions: [i] The Controller receives a poisoned completion from the link in response to a request. [ii] The Controller sends out a poisoned write request on the link [this may be because an underflow occurred during the packet transfer at the host interface of the Controller.]. When this bit is 0, the Master Data Parity Error status bit is never set.
5:3	R0	R	0h	Reserved
2	BE	R/W	0h	For a Function with a Type 1 Configurations Space header[Controller in RP Mode], this bit controls forwarding of Memory or I/O Requests by a Port in the Upstream direction. Note: The Controller does not generate any response based on this bit. Client application logic must use this bit and respond to requests appropriately: - When this bit is '1', Client logic can process the Memory and IO Requests received from PCIe Link normally. - When this bit is '0', Client logic must handle Memory and IO Requests received from PCIe Link as Unsupported Requests.
1	MSE	R/W	0h	For a Function with a Type 1 Configuration Space header[Controller in RP Mode], this bit controls the response to Memory Space accesses received on its Primary Side. Note: The Controller does not generate any response based on this bit. - Client must check for this bit to be '1' before initiating any Memory requests on the pcie_master_AXI interface.
0	ISE	R/W	0h	For a Function with a Type 1 Configuration Space header [Controller in RP Mode] , this bit controls the response to I/O Space accesses received on its Primary Side. Note: The Controller does not generate any response based on this bit. - Client must check for this bit to be '1' before initiating any IO requests on the pcie_master_AXI interface.

14.9.2.2.2.35 PCIE_CORE_RC_I_RC_PCIE_BASE_I_REVISION_ID_CLASS_CODE Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_REVISION_ID_CLASS_CODE Register (Offset = 8h) [reset = 0h]

This register contains the Revision ID and Class Code associated with the device incorporating the Cadence PCIe Controller.

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Table 14-19388. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0008h

Figure 14-6403. PCIE_CORE_RC_I_RC_PCIE_BASE_I_REVISION_ID_CLASS_CODE Name Register

31	30	29	28	27	26	25	24
CC							
R							
0h							
23	22	21	20	19	18	17	16
SCC							
R							
0h							
15	14	13	12	11	10	9	8
PIB							
R							
0h							
7	6	5	4	3	2	1	0
RID							
R							
0h							

Table 14-19390. PCIE_CORE_RC_I_RC_PCIE_BASE_I_REVISION_ID_CLASS_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CC	R	0h	Identifies the function of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
23:16	SCC	R	0h	Identifies a sub-category within the selected function. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
15:8	PIB	R	0h	Identifies the register set layout of the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
7:0	RID	R	0h	Assigned by the manufacturer of the device to identify the revision number of the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

14.9.2.2.2.36 PCIE_CORE_RC_I_RC_PCIE_BASE_I_BIST_HEADER_LATENCY_CACHE_LINE Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_BIST_HEADER_LATENCY_CACHE_LINE Register (Offset = Ch) [reset = 10000h]

This location contains the BIST, header-type, Latency Timer and Cache Line Size Registers.

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Table 14-19391. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6404. PCIE_CORE_RC_I_RC_PCIE_BASE_I_BIST_HEADER_LATENCY_CACHE_LINE Name Register

31	30	29	28	27	26	25	24
BR							
R							
0h							
23	22	21	20	19	18	17	16
DT	HT						
R	R						
0h	1h						
15	14	13	12	11	10	9	8
LT							
R							
0h							
7	6	5	4	3	2	1	0
CLS							
R/W							
0h							

Table 14-19393. PCIE_CORE_RC_I_RC_PCIE_BASE_I_BIST_HEADER_LATENCY_CACHE_LINE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BR	R	0h	BIST control register. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
23	DT	R	0h	Identifies whether the device supports a single Function or multiple Functions. Hardwired to zero
22:16	HT	R	1h	Identifies format of header. This field is hardwired to 1.
15:8	LT	R	0h	This is an unused field and is hardwired to 0.
7:0	CLS	R/W	0h	Cache Line Size Register defined in PCI Specifications 3.0. This field can be read or written, both from the link and from the local management bus, but its value is not used.

14.9.2.2.2.37 PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_0 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_0 Register (Offset = 10h) [reset = 0h]

This is the Base Address Register 0 in the Type-1 Config Space. It can be configured as a 32-bit memory BAR, a 32-bit IO BAR, or can be paired with RC BAR 1 to form a 64-bit memory BAR. The parameters of this BAR are configured in the local management register Root Complex BAR Configuration Register.

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Table 14-19394. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0010h**

Figure 14-6405. PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_0 Name Register

31	30	29	28	27	26	25	24
BAMRW							
R/W							
0h							
23	22	21	20	19	18	17	16
BAMRW		BAMR0					
R/W		R					
0h		0h					
15	14	13	12	11	10	9	8
BAMR0							
R							
0h							
7	6	5	4	3	2	1	0
BAMR0				P0	S0	R7	MSI0
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-19396. PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	BAMRW	R/W	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in Root Complex BAR Configuration Register. All other bits are not writeable, and are read as 0's.
21:4	BAMR0	R	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in Root Complex BAR Configuration Register. All other bits are not writeable, and are read as 0's.
3	P0	R	0h	For memory BAR: This bit reads as 1 when BAR 0 is configured as a prefetchable BAR, and as 0 when configured as a non-prefetchable BAR. For IO BAR: This is bit 3 of the base address. The value read in this field is determined by the setting of Root Complex BAR Configuration Register.
2	S0	R	0h	For memory BAR:This bit reads as 0 when BAR 0 is configured as a 32-bit BAR, and as 1 when configured as a 64-bit BAR. For IO BAR: This is bit 3 of the base address. The value read in this field is determined by the setting of Root Complex BAR Configuration Register.

Table 14-19396. PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R7	R	0h	This bit is hardwired to 0 for both memory and I/O BARs.
0	MSI0	R	0h	Specifies whether this BAR defines a memory address range or an I/O address range [0 = memory, 1 = I/O]. The value read in this field is determined by the setting of Root Complex BAR Configuration Register.

14.9.2.2.2.38 PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_1 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_1 Register (Offset = 14h) [reset = 0h]

This is the Base Address Register 1 in the Type-1 Config Space. It can be configured as a 32-bit memory BAR, a 32-bit IO BAR, or can be paired with RC BAR 0 to form a 64-bit memory BAR. The parameters of this BAR are configured in the local management register Root Complex BAR Configuration Register.

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Table 14-19397. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6406. PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_1 Name Register

31	30	29	28	27	26	25	24
R7							
R							
0h							
23	22	21	20	19	18	17	16
R7							
R							
0h							
15	14	13	12	11	10	9	8
R7							
R							
0h							
7	6	5	4	3	2	1	0
R7							
R							
0h							

Table 14-19399. PCIE_CORE_RC_I_RC_PCIE_BASE_I_RC_BAR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration regsiter in LM space.

14.9.2.2.2.39 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_BUS_NUMBERS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_BUS_NUMBERS Register (Offset = 18h) [reset = 0h]

This location contains the 8-bit fields: Primary Bus Number, Secondary Bus Number,Subordinate Bus Number, Secondary Latency Timer.

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Table 14-19400. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6407. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_BUS_NUMBERS Name Register

31	30	29	28	27	26	25	24
SLTN							
R							
0h							
23	22	21	20	19	18	17	16
SUBN							
R/W							
0h							
15	14	13	12	11	10	9	8
SBN							
R/W							
0h							
7	6	5	4	3	2	1	0
PBN							
R/W							
0h							

Table 14-19402. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_BUS_NUMBERS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SLTN	R	0h	This field is not implemented.
23:16	SUBN	R/W	0h	This field can be read and written from the local management bus, but its value is not used within the Controller.
15:8	SBN	R/W	0h	This field can be read and written from the local management bus, but its value is not used within the Controller.
7:0	PBN	R/W	0h	This field can be read and written from the local management bus, but its value is not used within the Controller.

14.9.2.2.2.40 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT Register (Offset = 1Ch) [reset = 0h]

This location contains the 8-bit IO Base Register, the 8-bit IO Limit Register and the 16-bit Secondary Status Registers.

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Table 14-19403. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6408. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT Name Register

31	30	29	28	27	26	25	24
DPE	RSE	RMA	RTA	STA	R4		MPE
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R		R/W1TC
0h	0h	0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ILR				R2			IOBS2
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IBR				R1			IOBS1
R				R			R
0h				0h			0h

Table 14-19405. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DPE	R/W1TC	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
30	RSE	R/W1TC	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
29	RMA	R/W1TC	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 14-19405. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	RTA	R/W1TC	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
27	STA	R/W1TC	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
26:25	R4	R	0h	Reserved
24	MPE	R/W1TC	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write. Note that this bit can be set only when the Parity Error Response Enable bit is set in the Bridge Control Register
23:16	R3	R	0h	Reserved
15:12	ILR	R	0h	This field can be read and written from the local management bus if IO BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.
11:9	R2	R	0h	Reserved
8	IOBS2	R	0h	value set in Type1 cfg IO bar size[bit 20 of RC BAR CONFIG register].If type1 cfg IObar enable bit[bit 19 in RC BAR CONFIG register] is not set, then this field will be hard coded to 0.
7:4	IBR	R	0h	This field can be read and written from the local management bus if IO BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.
3:1	R1	R	0h	Reserved
0	IOBS1	R	0h	value set in Type1 cfg IO bar size[bit 20 of RC BAR CONFIG register]. If type1 cfg IObar enable bit[bit 19 in RC BAR CONFIG register] is not set, then this field will be hard coded to 0.

14.9.2.2.2.41 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_MEM_BASE_LIMIT Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_MEM_BASE_LIMIT Register (Offset = 20h) [reset = 0h]

This location contains the 16-bit Memory Base Register and the 16-bit Memory Limit Register

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Table 14-19406. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0020h**

Figure 14-6409. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_MEM_BASE_LIMIT Name Register

31	30	29	28	27	26	25	24
MLR							
R/W							
0h							
23	22	21	20	19	18	17	16
MLR				R2			
R/W				R			
0h				0h			
15	14	13	12	11	10	9	8
MBR							
R/W							
0h							
7	6	5	4	3	2	1	0
MBR				R1			
R/W				R			
0h				0h			

Table 14-19408. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_MEM_BASE_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	MLR	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
19:16	R2	R	0h	Reserved
15:4	MBR	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
3:0	R1	R	0h	Reserved

14.9.2.2.2.42 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_LIMIT Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_LIMIT Register (Offset = 24h) [reset = 0h]

This location contains the Prefetchable Memory Base Register and the Prefetchable Memory Limit Register. This register is enabled by programming the Root Complex BAR configuration register in the Local Management space

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Table 14-19409. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0024h**

Figure 14-6410. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_LIMIT Name Register

31	30	29	28	27	26	25	24
PMLR							
R							
0h							
23	22	21	20	19	18	17	16
PMLR							
R							
0h							
15	14	13	12	11	10	9	8
PMBR							
R							
0h							
7	6	5	4	3	2	1	0
PMBR							
R							
0h							

Table 14-19411. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PMLR	R	0h	This field can be read and written from the local management APB bus if prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.
15:0	PMBR	R	0h	This field can be read and written from the local management APB bus if prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.

14.9.2.2.2.43 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_UPPER Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_UPPER Register (Offset = 28h) [reset = 0h]

This location contains the upper 32 bits of the Prefetchable Base Register. This register is enabled by programming the Root Complex BAR configuration register in the Local Management space.

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Table 14-19412. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0028h**

Figure 14-6411. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_UPPER Name Register

31	30	29	28	27	26	25	24
PBRU							
R							
0h							
23	22	21	20	19	18	17	16
PBRU							
R							
0h							
15	14	13	12	11	10	9	8
PBRU							
R							
0h							
7	6	5	4	3	2	1	0
PBRU							
R							
0h							

Table 14-19414. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_BASE_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PBRU	R	0h	This field can be read and written from the local management APB bus if 64bit prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.

14.9.2.2.2.44 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_LIMIT_UPPER Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_LIMIT_UPPER Register (Offset = 2Ch) [reset = 0h]

This location contains the upper 32 bits of the Prefetchable Limit Register. This register is enabled by programming the Root Complex BAR configuration register in the Local Management space.

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Table 14-19415. Instance Table

Instance Name	Physical Address
PCIE0	0D00 002Ch

Figure 14-6412. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_LIMIT_UPPER Name Register

31	30	29	28	27	26	25	24
PLRU							
R							
0h							
23	22	21	20	19	18	17	16
PLRU							
R							
0h							
15	14	13	12	11	10	9	8
PLRU							
R							
0h							
7	6	5	4	3	2	1	0
PLRU							
R							
0h							

Table 14-19417. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_PREFETCH_LIMIT_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PLRU	R	0h	This field can be read and written from the local management APB bus if 64bit prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.

14.9.2.2.2.45 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT_UPPER Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT_UPPER Register (Offset = 30h) [reset = 0h]

This location contains the upper 16 bits of the IO Base and IO Limit Registers

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Table 14-19418. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0030h

Figure 14-6413. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT_UPPER Name Register

31	30	29	28	27	26	25	24
ILR							
R							
0h							
23	22	21	20	19	18	17	16
ILR							
R							
0h							
15	14	13	12	11	10	9	8
IBRU							
R							
0h							
7	6	5	4	3	2	1	0
IBRU							
R							
0h							

Table 14-19420. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_IO_BASE_LIMIT_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ILR	R	0h	This field can be read and written from the local management bus if 32bit IO BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.
15:0	IBRU	R	0h	This field can be read and written from the local management bus if 32bit IO BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.

14.9.2.2.2.46 PCIE_CORE_RC_I_RC_PCIE_BASE_I_CAPABILITIES_POINTER Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_CAPABILITIES_POINTER Register (Offset = 34h) [reset = 80h]

This location contains the pointer to the first PCI Capabilities Structure.

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Table 14-19421. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0034h**

Figure 14-6414. PCIE_CORE_RC_I_RC_PCIE_BASE_I_CAPABILITIES_POINTER Name Register

31	30	29	28	27	26	25	24
R15							
R							
0h							
23	22	21	20	19	18	17	16
R15							
R							
0h							
15	14	13	12	11	10	9	8
R15							
R							
0h							
7	6	5	4	3	2	1	0
CP							
R							
80h							

Table 14-19423. PCIE_CORE_RC_I_RC_PCIE_BASE_I_CAPABILITIES_POINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	R15	R	0h	Reserved
7:0	CP	R	80h	Contains pointer to the first PCI Capability Structure. This field is set by default to the value defined in the RTL file reg_defaults.h. It can be re-written independently for every Function from the local management APB bus.

14.9.2.2.2.47 PCIE_CORE_RC_I_RC_PCIE_BASE_RSVD_0E Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_RSVD_0E Register (Offset = 38h) [reset = 0h]

Reserved

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Table 14-19424. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0038h**

Figure 14-6415. PCIE_CORE_RC_I_RC_PCIE_BASE_RSVD_0E Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD							
R							
0h							

Table 14-19426. PCIE_CORE_RC_I_RC_PCIE_BASE_RSVD_0E Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	0h	Reserved

14.9.2.2.2.48 PCIE_CORE_RC_I_RC_PCIE_BASE_I_INTRPT_LINE_INTRPT_PIN Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_INTRPT_LINE_INTRPT_PIN Register (Offset = 3Ch) [reset = 1FFh]

This location contains the Interrupt Line Register, the Interrupt Pin Register, and the Bridge Control Register

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Table 14-19427. Instance Table

Instance Name	Physical Address
PCIE0	0D00 003Ch

Figure 14-6416. PCIE_CORE_RC_I_RC_PCIE_BASE_I_INTRPT_LINE_INTRPT_PIN Name Register

31	30	29	28	27	26	25	24
R23							
R							
0h							
23	22	21	20	19	18	17	16
R23	BCRSBR	R21	VGA16D	VGAE	ISAE	BCSE	PERE
R	R/W	R	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
R5					IPR		
R					R		
0h					1h		
7	6	5	4	3	2	1	0
ILR							
R/W							
FFh							

Table 14-19429. PCIE_CORE_RC_I_RC_PCIE_BASE_I_INTRPT_LINE_INTRPT_PIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	R23	R	0h	Reserved
22	BCRSBR	R/W	0h	This field can be read and written from the local management APB bus. When set, it initiates a hot reset on the link.
21	R21	R	0h	Reserved
20	VGA16D	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
19	VGAE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
18	ISAE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
17	BCSE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
16	PERE	R/W	0h	This field can be read and written from the local management APB bus. It is used only to enable the Master Data Parity Error bit in the Secondary Status Register.
15:11	R5	R	0h	Reserved

Table 14-19429. PCIE_CORE_RC_I_RC_PCIE_BASE_I_INTRPT_LINE_INTRPT_PIN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	IPR	R	1h	Identifies the interrupt input [A, B, C, D] to which this Functions interrupt output is connected to [01 = INTA, 02 = INTB, 03 = INTC, 04 = INTD]. The assignment of interrupt inputs to Functions is fixed when the Controller is configured. This field can be re-written independently for each Function from the local management bus. Default values - PF0: 01 [INTA], PF1: 02 [INTB].
7:0	ILR	R/W	FFh	This field can be read and written from the local management bus, but its value is not used within the Controller.The given reset value is for PF0.

14.9.2.2.2.49 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CAP Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CAP Register (Offset = 80h) [reset = 5A039001h]

This location contains the Power Management Capabilities Register, its Capability ID, and a pointer to the next capability. In the RC mode, the settings of the fields of this register have no effect on the operation of the Controller

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Table 14-19430. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0080h**

Figure 14-6417. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CAP Name Register

31	30	29	28	27	26	25	24
PSDCS	PSDHS	PSD2S	PSD1S	PSD0S	D2S	D1S	MCRAPS
R	R	R	R	R	R	R	R
0h	1h	0h	1h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
MCRAPS		DSI	R0	PC	VID		
R		R	R	R	R		
0h		0h	0h	0h	3h		
15	14	13	12	11	10	9	8
CP							
R							
90h							
7	6	5	4	3	2	1	0
CID							
R							
1h							

Table 14-19432. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PSDCS	R	0h	Indicates whether the Function is capable of sending PME messages when in the D3cold state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
30	PSDHS	R	1h	Indicates whether the Function is capable of sending PME messages when in the D3hot state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
29	PSD2S	R	0h	Indicates whether the Function is capable of sending PME messages when in the D2 state. This bit is hardwired to 0 because D2 state is not supported.
28	PSD1S	R	1h	Indicates whether the Function is capable of sending PME messages when in the D1 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.

Table 14-19432. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	PSD0S	R	1h	Indicates whether the Function is capable of sending PME messages when in the D0 state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
26	D2S	R	0h	Set if the Function supports the D2 power state. Currently hardwired to 0.
25	D1S	R	1h	Set if the Function supports the D1 power state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
24:22	MCRAPS	R	0h	Specifies the maximum current drawn by the device from the aux power source in the D3cold state. This field is not implemented in devices not supporting PME notification when in the D3cold state, and is therefore hardwired to 0.
21	DSI	R	0h	This bit, when set, indicates that the device requires additional configuration steps beyond setting up its PCI configuration space, to bring it to the D0 active state from the D0 uninitialized state. This bit is hardwired to 0.
20	R0	R	0h	Reserved
19	PC	R	0h	Not applicable to PCI Express. This bit is hardwired to 0.
18:16	VID	R	3h	Indicates the version of the PCI Bus Power Management Specifications that the Function implements. This field is set by default to 011 [Version 1.2]. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
15:8	CP	R	90h	Contains pointer to the next PCI Capability Structure. The Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
7:0	CID	R	1h	Identifies that the capability structure is for Power Management. This field is set by default to 01 hex. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

14.9.2.2.2.50 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CTRL_STAT_REP Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CTRL_STAT_REP Register (Offset = 84h) [reset = 8h]

This location contains the Power Management Control/Status and Data Registers.

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Table 14-19433. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0084h**

Figure 14-6418. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CTRL_STAT_REP Name Register

31	30	29	28	27	26	25	24
DR							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMES	R2						PE
R/W1TC	R						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R3				NSR	R4	PS	
R				R	R	R/W	
0h				1h	0h	0h	

Table 14-19435. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PWR_MGMT_CTRL_STAT_REP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DR	R	0h	This optional register is not implemented in the Cadence PCIe Controller. This field is hardwired to 0.
23:16	R1	R	0h	Reserved
15	PMES	R/W1TC	0h	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write..
14:9	R2	R	0h	Reserved
8	PE	R/W	0h	This bit can be set or cleared from the local management APB bus, by writing a 1 or 0, respectively.
7:4	R3	R	0h	Reserved
3	NSR	R	1h	This bit is set to 1 by default. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
2	R4	R	0h	Reserved
1:0	PS	R/W	0h	This field can also be read or written from the local management APBbus.

14.9.2.2.2.51 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_CTRL_REG Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_CTRL_REG Register (Offset = 90h) [reset = 180B005h]

This register is used only when the Controller is configured to support Message Signaled Interrupts (MSIs). In addition to the MSI control bits, this location also contains the Capability ID for MSI and the pointer to the next PCI Capability Structure.

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Table 14-19436. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0090h**

Figure 14-6419. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_CTRL_REG Name Register

31	30	29	28	27	26	25	24
R0							MC
R							R
0h							1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BAC64	MME			MMC			ME
R	R/W			R			R/W
1h	0h			0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CP1							
R							
B0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CID1							
R							
5h							

Table 14-19438. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	R0	R	0h	Reserved
24	MC	R	1h	can be modified using localmanagement interface
23	BAC64	R	1h	Set to 1 to indicate that the device is capable of generating 64-bit addresses for MSI messages.Can be modified using local management interface
22:20	MME	R/W	0h	Encodes the number of distinct messages that the Controller is programmed to generate for this Function [000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32]. This setting must be based on the number of interrupt inputs of the Controller that are actually used by this Function. This field can be written from the local management bus.

Table 14-19438. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:17	MMC	R	0h	Encodes the number of distinct messages that the Controller is capable of generating for this Function [000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32]. Thus, this field defines the number of the interrupt vectors for this Function. The Controller allows up to 32 distinct messages, but the setting of this field must be based on the number of interrupt inputs of the Controller that are actually used by the client. For example, if the client logic uses 8 of the 32 distinct MSI interrupt inputs of the Controller for this Function, then the value of this field must be set to 011. This field can be written from the local management bus. Please see the define den_db_Fx_MSI_MULTIPLE_MSG_CAPABLE values [where x is the function number] for default values of each function in the reg_defaults.v files.
16	ME	R/W	0h	Set by the configuration program to enable the MSI feature. This field can also be written from the local management bus.
15:8	CP1	R	B0h	Pointer to the next PCI Capability Structure. This can be modified from the local management bus. This field can be written from the local management bus.
7:0	CID1	R	5h	Specifies that the capability structure is for MSI. Hardwired to 05 hex.

14.9.2.2.2.52 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_LOW_ADDR Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_LOW_ADDR Register (Offset = 94h) [reset = 0h]

This register contains the first 32 bits of the address to be used in the MSI messages generated by the Controller for this Function. This address is taken as a 32-bit address if the value programmed in the MSI Message High Address Register is 0. Otherwise, this address is taken as the least significant 32 bits of the 64-bit address sent in MSI messages.

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Table 14-19439. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0094h**

Figure 14-6420. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_LOW_ADDR Name Register

31	30	29	28	27	26	25	24
MAL							
R/W							
0h							
23	22	21	20	19	18	17	16
MAL							
R/W							
0h							
15	14	13	12	11	10	9	8
MAL							
R/W							
0h							
7	6	5	4	3	2	1	0
MAL						R1	
R/W						R	
0h						0h	

Table 14-19441. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_LOW_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	MAL	R/W	0h	Lower bits of the address to be used in MSI messages. This field can also be written from the local management bus.
1:0	R1	R	0h	The two lower bits of the address are hardwired to 0 to align the address on a double-word boundary.

14.9.2.2.2.53 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_HI_ADDR Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_HI_ADDR Register (Offset = 98h) [reset = 0h]

This register contains the most significant 32 bits of the 64-bit address sent by the Controller in MSI messages. A value of all zeroes in this register is taken to mean that the Controller should use 32-bit addresses in the messages.

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Table 14-19442. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0098h**

Figure 14-6421. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_HI_ADDR Name Register

31	30	29	28	27	26	25	24
MAH							
R/W							
0h							
23	22	21	20	19	18	17	16
MAH							
R/W							
0h							
15	14	13	12	11	10	9	8
MAH							
R/W							
0h							
7	6	5	4	3	2	1	0
MAH							
R/W							
0h							

Table 14-19444. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_HI_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAH	R/W	0h	Contains bits 63:32 of the 64-bit address to be used in MSI Messages. A value of 0 specifies that 32-bit addresses are to be used in the messages. This field can also be written from the local management bus.

14.9.2.2.2.54 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_DATA Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_DATA Register (Offset = 9Ch) [reset = 0h]

This register contains the write data to be used in the MSI messages to be generated for the associated PCI Function. When the number of distinct messages programmed in the MSI Control Register is 1, the 32-bit value from this register is used as the data value in the MSI packets generated by the Controller for this Function. If the number of distinct messages is more than 1, the least significant bits of the programmed value are replaced with the encoded interrupt vector [31:0] of the specific message to generate the write data value for the message.

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Table 14-19445. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 009Ch**

Figure 14-6422. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_DATA Name Register

31	30	29	28	27	26	25	24
R2							
R							
0h							
23	22	21	20	19	18	17	16
R2							
R							
0h							
15	14	13	12	11	10	9	8
MD							
R/W							
0h							
7	6	5	4	3	2	1	0
MD							
R/W							
0h							

Table 14-19447. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MSG_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R2	R	0h	Hardwired to 0
15:0	MD	R/W	0h	Message data to be used for this Function. This field can also be written from the local management bus.

14.9.2.2.2.55 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MASK Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MASK Register (Offset = A0h) [reset = 0h]

This register contains the MSI mask bits, one for each of the interrupt levels.

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Table 14-19448. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00A0h**

Figure 14-6423. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MM
NONE							R/W
0h							0h

Table 14-19450. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MM	R/W	0h	Mask bits for MSI interrupts. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid mask bits.

14.9.2.2.2.56 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_PENDING_BITS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_PENDING_BITS Register (Offset = A4h) [reset = 0h]

This register contains the MSI pending interrupt bits, one for each of the interrupt levels.

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Table 14-19451. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00A4h**

Figure 14-6424. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_PENDING_BITS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MP
NONE							R
0h							0h

Table 14-19453. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSI_PENDING_BITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MP	R	0h	Pending bits for MSI interrupts. This field can be written from the APB interface to refelct the current pending status.

14.9.2.2.2.57 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_CTRL Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_CTRL Register (Offset = B0h) [reset = C011h]

This register contains the MSI-X configuration bits, the Capability ID for MSI-X and the pointer to the next PCI Capability Structure.

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Table 14-19454. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00B0h**

Figure 14-6425. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_CTRL Name Register

31	30	29	28	27	26	25	24
MSIXE	FM	R0			MSIXTS		
R/W	R/W	R			R		
0h	0h	0h			0h		
23	22	21	20	19	18	17	16
MSIXTS							
R							
0h							
15	14	13	12	11	10	9	8
CP							
R							
C0h							
7	6	5	4	3	2	1	0
CID							
R							
11h							

Table 14-19456. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSIXE	R/W	0h	Set by the configuration program to enable the MSI-X feature. This field can also be written from the local management bus.
30	FM	R/W	0h	This bit serves as a global mask to all the interrupt conditions associated with this Function. When this bit is set, the Controller will not send out MSI-X messages from this Function. This field can also be written from the local management bus.
29:27	R0	R	0h	Reserved
26:16	MSIXTS	R	0h	Specifies the size of the MSI-X Table, that is, the number of interrupt vectors defined for the Function. The programmed value is 1 minus the size of the table [that is, this field is set to 0 if the table size is 1.]. It can be re-written independently for each Function from the local management bus. Please see the define den_db_Fx_MSIX_TABLE_SIZE values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 14-19456. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	CP	R	C0h	Contains pointer to the next PCI Capability Structure. This is set to point to the PCI Express Capability Structure at 30 hex. This can be rewritten independently for each Function from the local management bus.
7:0	CID	R	11h	Identifies that the capability structure is for MSI-X. This field is set by default to 11 hex. It can be rewritten independently for each Function from the local management bus.

14.9.2.2.2.58 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_TBL_OFFSET Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_TBL_OFFSET Register (Offset = B4h) [reset = 0h]

This register is used to specify the location of the MSI-X Table in memory. All the 32 bits of this register can be re-written independently for each Function from the local management bus.

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Table 14-19457. Instance Table

Instance Name	Physical Address
PCIE0	0D00 00B4h

Figure 14-6426. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_TBL_OFFSET Name Register

31	30	29	28	27	26	25	24
TO							
R							
0h							
23	22	21	20	19	18	17	16
TO							
R							
0h							
15	14	13	12	11	10	9	8
TO							
R							
0h							
7	6	5	4	3	2	1	0
TO					BARI		
R					R		
0h					0h		

Table 14-19459. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_TBL_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	TO	R	0h	Offset of the memory address where the MSI-X Table is located, relative to the selected BAR. The three least significant bits of the address are omitted, as the addresses are QWORD aligned. Please see the define den_db_Fx_MSIX_TABLE_OFFSET values [where x is the function number] for default values of each function in the reg_defaults.v files.
2:0	BARI	R	0h	Identifies the BAR corresponding to the memory address range where the MSI-X Table is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. Please see the define den_db_Fx_MSIX_TABLE_BIR values [where x is the function number] for default values of each function in the reg_defaults.v files.

14.9.2.2.2.59 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_PENDING_INTRPT Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_PENDING_INTRPT Register (Offset = B8h) [reset = 8h]

This register is used to specify the location of the MSI-X Pending Bit Array (PBA). The PBA is a structure in memory containing the pending interrupt bits. All the 32 bits of this register can be rewritten independently for each Function from the local management bus.

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Table 14-19460. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00B8h**

Figure 14-6427. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_PENDING_INTRPT Name Register

31	30	29	28	27	26	25	24
PBAO							
R							
1h							
23	22	21	20	19	18	17	16
PBAO							
R							
1h							
15	14	13	12	11	10	9	8
PBAO							
R							
1h							
7	6	5	4	3	2	1	0
PBAO					BARI1		
R					R		
1h					0h		

Table 14-19462. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_PENDING_INTRPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	PBAO	R	1h	Offset of the memory address where the PBA is located, relative to the selected BAR. The three least significant bits of the address are omitted, as the addresses are QWORD aligned. Please see the define den_db_Fx_MSIX_PBA_OFFSET values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 14-19462. PCIE_CORE_RC_I_RC_PCIE_BASE_I_MSIX_PENDING_INTRPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	BARI1	R	0h	Identifies the BAR corresponding to the memory address range where the PBA Structure is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register.Identifies the BAR corresponding to the memory address range where the PBA Structure is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register. Please see the define den_db_Fx_MSIX_PBA_BIR values [where x is the function number] for default values of each function in the reg_defaults.v files.

14.9.2.2.2.60 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_LIST Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_LIST Register (Offset = C0h) [reset = 1420010h]

This location identifies the PCI Express device type and its capabilities. It also contains the Capability ID for the PCI Express Structure and the pointer to the next capability structure.

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Table 14-19463. Instance Table

Instance Name	Physical Address
PCIE0	0D00 00C0h

Figure 14-6428. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_LIST Name Register

31	30	29	28	27	26	25	24
R0	TRS	IMN					SI
R	R	R					R
0h	0h	0h					1h
23	22	21	20	19	18	17	16
DT				PCV			
R				R			
4h				2h			
15	14	13	12	11	10	9	8
NCP							
R							
0h							
7	6	5	4	3	2	1	0
CID							
R							
10h							

Table 14-19465. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_LIST Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R0	R	0h	Reserved
30	TRS	R	0h	When set to 1, this bit indicates that the device supports routing of Trusted Configuration Requests. Not valid for Endpoints. Hardwired to 0.
29:25	IMN	R	0h	Identifies the MSI or MSI-X interrupt vector for the interrupt message generated corresponding to the status bits in the Slot Status Register, Root Status Register, or this capability structure. This field must be defined based on the chosen interrupt mode - MSI or MSI-X. This field is hardwired to 0.
24	SI	R	1h	When Set, this bit indicates that the Link associated with this Port is connected to a slot
23:20	DT	R	4h	Indicates the type of device implementing this Function. This field is hardwired to 4 in the RP mode.
19:16	PCV	R	2h	Identifies the version number of the capability structure. This field is set to 2 by default to indicate that the Controller is compatible to PCI Express Base Specification Revision 3.0. Can be modified using local management interface after asserting input signal MGMT_TYPE1_CONFIG_REG_ACCESS high.

Table 14-19465. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_LIST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	NCP	R	0h	Points to the next PCI capability structure. Set to 0 because this is the last capability structure.
7:0	CID	R	10h	Specifies Capability ID assigned by PCI SIG for this structure. This field is hardwired to 10 hex.

14.9.2.2.2.61 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP Register (Offset = C4h) [reset = 8000h]

This register advertises the capabilities of the PCI Express device.

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Table 14-19466. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00C4h**

Figure 14-6429. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">R5</td><td>FLRC</td><td colspan="2">CPLS</td><td colspan="2">CSP</td></tr>
<tr><td colspan="3">R</td><td>R</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">CSP</td><td colspan="2">R4</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RER</td><td colspan="3">R3</td><td colspan="3">AL1L</td><td>AL0L</td></tr>
<tr><td>R</td><td colspan="3">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td>1h</td><td colspan="3">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">AL0L</td><td>ETFS</td><td colspan="2">PFS</td><td colspan="3">MP</td></tr>
<tr><td colspan="2">R</td><td>R</td><td colspan="2">R</td><td colspan="3">R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-19468. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	R5	R	0h	Reserved
28	FLRC	R	0h	A value of 1b indicates the Function supports the optional Function Level Reset mechanism
27:26	CPLS	R	0h	Specifies the scale used by Slot Power Limit Value. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write. .
25:18	CSP	R	0h	Specifies upper limit on power supplied by slot. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write. .
17:16	R4	R	0h	Reserved
15	RER	R	1h	Enables role-based errer reporting. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
14:12	R3	R	0h	Reserved

Table 14-19468. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	AL1L	R	0h	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L1 to L0. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
8:6	AL0L	R	0h	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L0S to L0. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
5	ETFS	R	0h	hard coded to zero .
4:3	PFS	R	0h	This field is used to extend the tag field by combining unused Function bits with the tag bits. This field is hardwired to 00 to disable this feature.
2:0	MP	R	0h	Specifies maximum payload size supported by the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

14.9.2.2.2.62 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS Register (Offset = C8h) [reset = 2810h]

This register contains control and status bits associated with the device.

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Table 14-19469. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00C8h**

Figure 14-6430. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS Name Register

31	30	29	28	27	26	25	24
R8							
R							
0h							
23	22	21	20	19	18	17	16
R8		TP	APD	URD	FED	NFED	CED
R		R	R	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
R7	MRR			ENS	APPME	PFE	ETE
R	R/W			R/W	R	R	R
0h	2h			1h	0h	0h	0h
7	6	5	4	3	2	1	0
MP			ERO	EURR	EFER	ENFER	ECER
R/W			R/W	R/W	R/W	R/W	R/W
0h			1h	0h	0h	0h	0h

Table 14-19471. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	R8	R	0h	N/A
21	TP	R	0h	Indicates if any of the Non-Posted requests issued by the RC are still pending.
20	APD	R	0h	Set when auxiliary power is detected by the device. This is an unused field.
19	URD	R/W1TC	0h	Set to 1 by the Controller when it receives an unsupported request.
18	FED	R/W1TC	0h	Set to 1 by the Controller when it detects a fatal error, regardless of whether the error is masked.
17	NFED	R/W1TC	0h	Set to 1 by the Controller when it detects a non-fatal error, regardless of whether the error is masked.
16	CED	R/W1TC	0h	Set to 1 by the Controller when it detects a correctable error, regardless of whether the error is masked.
15	R7	R	0h	Hardwired to 0.
14:12	MRR	R/W	2h	Specifies the maximum size allowed in read requests generated by the device.

Table 14-19471. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ENS	R/W	1h	If this bit is Set, the Function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency.
10	APPME	R	0h	Hardwired to 0
9	PFE	R	0h	Hardwired to 0
8	ETE	R	0h	extended tag not enabled. Hence hard coded to zero .
7:5	MP	R/W	0h	Specifies the maximum TLP payload size configured. The device must be able to receive a TLP of this maximum size, and should not generate TLP's larger than this value. Software must set this field based on the maximum payload size in the Device Capabilities Register, and the capability of the other side.
4	ERO	R/W	1h	When set, this bit indicates that the device is allowed to set the Relaxed Ordering bit in the Attributes field of transactions initiated from it., when the transactions do not require Strong Ordering.
3	EURR	R/W	0h	This bit is used to gate the CORRECTABLE_ERROR_OUT, NON_FATAL_ERROR_OUT, FATAL_ERROR_OUT output in Root Port mode on receiving unsupported requests. Note: Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of FATAL_ERROR_OUT on receiving uncorrectable unsupported requests.
2	EFER	R/W	0h	This bit is used to gate the FATAL_ERROR_OUT output of the Controller in Root Port mode. When an Uncorrectable, Unmasked Error with Uncorrectable Error Severity set to 1 is detected Internally or when a ERR_FATAL message is received by the Controller, in Root Port mode, this bit gates the assertion of FATAL_ERROR_OUT output. Note: Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of FATAL_ERROR_OUT.
1	ENFER	R/W	0h	This bit is used to gate the NON_FATAL_ERROR_OUT output of the Controller in Root Port mode. When an Uncorrectable, Unmasked Error with Uncorrectable Error Severity set to 0 is detected Internally or when a ERR_NON_FATAL message is received by the Controller, in Root Port mode, this bit gates the assertion of NON_FATAL_ERROR_OUT output. Note: Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of NON_FATAL_ERROR_OUT.
0	ECER	R/W	0h	This bit is used to gate the CORRECTABLE_ERROR_OUT output of the Controller in Root Port mode. When a Correctable and Unmasked Error is detected Internally or when a ERR_CORR message is received by the Controller, in Root Port mode, this bit gates the assertion of CORRECTABLE_ERROR_OUT output.

14.9.2.2.2.63 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP Register (Offset = CCh) [reset = 61AC13h]

This register advertises the link-specific capabilities of the device incorporating the Cadence PCIe Controller.

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Table 14-19472. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00CCh**

Figure 14-6431. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PN</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>R9</td><td>ASPMOC</td><td>LBNC</td><td>DARC</td><td>SERC</td><td>CPM</td><td colspan="2">L1EL</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td colspan="2">R</td></tr>
<tr><td>0h</td><td>1h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>L1EL</td><td colspan="3">L0EL</td><td colspan="2">ASPM</td><td colspan="2">MLW</td></tr>
<tr><td>R</td><td colspan="3">R</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td>3h</td><td colspan="3">2h</td><td colspan="2">3h</td><td colspan="2">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">MLW</td><td colspan="4">MLS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">3h</td></tr>
</table>

Table 14-19474. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PN	R	0h	Specifies the port number assigned to the PCI Express link connected to this device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
23	R9	R	0h	Reserved
22	ASPMOC	R	1h	A 1 in this position indicates the device supports the ASPM Optionality feature. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
21	LBNC	R	1h	A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
20	DARC	R	0h	Set to 1 if the device is capable of reporting that the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0, as this version of the Controller does not support the feature.

Table 14-19474. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	SERC	R	0h	Indicates the capability of the device to report a Surprise Down error condition. This bit is hardwired to 0, as this version of the Controller does not support the feature.
18	CPM	R	0h	Indicates that the device supports removal of reference clocks. Not supported in this version of the Controller. Hardwired to 0.
17:15	L1EL	R	3h	Specifies the exit latency from L1 state. This parameter is dependent on the Physical Layer implementation. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
14:12	L0EL	R	2h	Specifies the time required for the device to transition from L0S to L0. This parameter is dependent on the Physical Layer implementation. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
11:10	ASPM	R	3h	Indicates the level of ASPM support provided by the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
9:4	MLW	R	1h	Indicates the maximum number of lanes supported by the device.
3:0	MLS	R	3h	Indicates the speeds supported by the link [2.5 GT/s , 5 GT/s , 8 GT/s per lane]. This field is hardwired to 0001 [2.5GT/s] when the strap input PCIE_GENERATION_SEL is set to 0, to 0010 [5 GT/s] when the strap is set to 1 , and to 0011 [8 GT/s] when the strap input is set to 10 .

14.9.2.2.2.64 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS Register (Offset = D0h) [reset = 110000h]

This register contains control and status bits specific to the PCI Express link.

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Table 14-19475. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00D0h**

Figure 14-6432. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS Name Register

31	30	29	28	27	26	25	24
LABS	LBMS	DA	SCC	LTS	R12	NLW	
R/W1TC	R/W1TC	R	R	R	R	R	
0h	0h	0h	0h	0h	0h	1h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NLW				NLS			
R				R			
1h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R11				LABIE	LBMIE	HAWD	ECPM
R				R/W	R/W	R/W	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ES	CCC	RL	LD	RCB	R10	ASPMC	
R/W	R/W	R	R/W	R	R	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-19477. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LABS	R/W1TC	0h	This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0.
30	LBMS	R/W1TC	0h	This bit is Set by hardware to indicate that either link training has completed following write to retrain link bit, or when HW has changed link speed or width to attempt to correct unreliable link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0.
29	DA	R	0h	Indicates the status of the Data Link Layer. Set to 1 when the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0 in this version of the Controller.
28	SCC	R	0h	Indicates that the device uses the reference clock provided by the connector. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 14-19477. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	LTS	R	0h	This bit is set to 1 when the LTSSM is in the Recovery or Configuration states, or if a 1 has been written to the Retrain Link bit but the link training has not yet begun.
26	R12	R	0h	Reserved
25:20	NLW	R	1h	Set at the end of link training to the actual link width negotiated between the two sides.
19:16	NLS	R	1h	Negotiated link speed of the device. The only supported speed ids are 2.5 GT/s per lane [0001],5 GT/s per lane [0010] ,8 GT/s per lane [0011].
15:12	R11	R	0h	Reserved
11	LABIE	R/W	0h	When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0.
10	LBMIE	R/W	0h	When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0.
9	HAWD	R/W	0h	When this bit is set, the local application must not request to change the operating width of the link, other than attempting to correct unreliable Link operation by reducing Link width.
8	ECPM	R	0h	This field is hardwired to 0 when the Controller is in the RC mode.
7	ES	R/W	0h	Set to 1 to extend the sequence of ordered sets transmitted while exiting from the L0S state.
6	CCC	R/W	0h	A value of 0 indicates that the reference clock of this device is asynchronous to that of the upstream device. A value of 1 indicates that the reference clock is common.
5	RL	R	0h	Setting this bit to 1 causes the LTSSM to initiate link training. This bit always reads as 0. This bit can be set by Host SW at any time independent of the LTSSM state. If the LTSSM is not in L0 state, the Controller will internally register the retrain command and initiate the link retrain immediately after the LTSSM reaches L0. For example, if the LTSSM is already in Recovery, the Controller will initiate Retrain Link after the LTSSM transitions back to L0 state.
4	LD	R/W	0h	Writing a 1 to this bit position causes the LTSSM to go to the Disable Link state. The LTSSM stays in the Disable Link state while this bit is set.
3	RCB	R	0h	Indicates the Read Completion Boundary of the Root Port [0 = 64 bytes, 1 = 128 bytes]. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
2	R10	R	0h	Reserved

Table 14-19477. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	ASPMC	R/W	0h	Controls the level of ASPM support on the PCI Express link associated with the function. The valid setting are 00: ASPM disabled 01: L0s entry enabled, L1 disabled 10: L1 entry enabled, L0s disabled 11: Both L0s and L1 enabled. Note that the ASPM Control bits can be enabled only if the corresponding ASPM Support[1:0] bit is 1 in the Link Capabilities Register.

14.9.2.2.2.65 PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CAPABILITY Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CAPABILITY Register (Offset = D4h) [reset = 0h]

The Slot Capabilities register identifies PCI Express slot specific capabilities.

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Table 14-19478. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00D4h**

Figure 14-6433. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CAPABILITY Name Register

31	30	29	28	27	26	25	24
PSN							
R							
0h							
23	22	21	20	19	18	17	16
PSN					NCCS	EIP	SPLS
R					R	R	R
0h					0h	0h	0h
15	14	13	12	11	10	9	8
SPLS	SPLV						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
SPLV	HPC	HPS	PIP	AIP	MRLSP	PCP	ABPRSNT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19480. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	PSN	R	0h	This field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to zero for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port.
18	NCCS	R	0h	When Set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be Set if the hot-plug capable Port is able to accept writes to all fields of the Slot Control register without delay between successive writes.
17	EIP	R	0h	When Set, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot.

Table 14-19480. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CAPABILITY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:15	SPLS	R	0h	Specifies the scale used for the Slot Power Limit Value . Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x This register must be implemented if the Slot Implemented bit is Set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 00b.
14:7	SPLV	R	0h	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot [see Section 6.9] or by other means to the adapter. Power limit [in Watts] is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b [1.0x] and Slot Power Limit Value exceeds EFh, the following alternative encodings are used: F0h = 250 W Slot Power Limit F1h = 275 W Slot Power Limit F2h = 300 W Slot Power Limit F3h to FFh = Reserved for Slot Power Limit values above 300 W This register must be implemented if the Slot Implemented bit is Set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 0000 0000b.
6	HPC	R	0h	When Set, this bit indicates that this slot is capable of supporting hot-plug operations.
5	HPS	R	0h	When Set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation.
4	PIP	R	0h	When Set, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot.
3	AIP	R	0h	When Set, this bit indicates that an Attention Indicator is electrically controlled by the chassis.
2	MRLSP	R	0h	When Set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot.
1	PCP	R	0h	When Set, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter [depending on form factor].
0	ABPRSNT	R	0h	When Set, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis.

14.9.2.2.2.66 PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CTRL_STATUS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CTRL_STATUS Register (Offset = D8h) [reset = 2007C0h]

This register contains control bits specific to PCI Express slot parameters and status bits specific to the PCI Express Slot. All the read-write bits in this register can also be written from the local management APB bus.

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Table 14-19481. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00D8h**

Figure 14-6434. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CTRL_STATUS Name Register

31	30	29	28	27	26	25	24
RSCS2							DLLSC
R							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
EMIS	PDS	MRLSS	CMDCMPL	PDC	MRLSC	PFD	ABPRSD
R	R	R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	1h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RSCS1			DLLSCE	EMIC	PCC	PIC	
R			R/W	R	R/W	R/W	
0h			0h	0h	1h	3h	
7	6	5	4	3	2	1	0
AIC		HPIE	CCIE	PDCE	MSCE	PFDE	ABPE
R/W		R/W	R/W	R/W	R/W	R/W	R/W
3h		0h	0h	0h	0h	0h	0h

Table 14-19483. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RSCS2	R	0h	N/A
24	DLLSC	R/W1TC	0h	This bit is Set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active bit of the Link Status register to determine if the Link is active before initiating configuration cycles to the hot plugged device.
23	EMIS	R	0h	If an Electromechanical Interlock is implemented, this bit indicates the status of the Electromechanical Interlock. Defined encodings are: 0b Electromechanical Interlock Disengaged 1b Electromechanical Interlock Engaged

Table 14-19483. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	PDS	R	0h	This bit indicates the presence of an adapter in the slot, reflected by the logical 'OR' of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. Defined encodings are: 0b Slot Empty 1b Card Present in slot.
21	MRLSS	R	1h	This bit reports the status of the MRL sensor if implemented. Defined encodings are: 0b MRL Closed 1b MRL Open
20	CMDCMPL	R/W1TC	0h	If Command Completed notification is supported [if the No Command Completed Support bit in the Slot Capabilities register is 0b], this bit is Set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is Set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. If Command Completed notification is not supported, this bit must be hardwired to 0b.
19	PDC	R/W1TC	0h	This bit is set when the value reported in the Presence Detect State bit is changed.
18	MRLSC	R/W1TC	0h	If an MRL sensor is implemented, this bit is Set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be Set.
17	PFD	R/W1TC	0h	If a Power Controller that supports power fault detection is implemented, this bit is Set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be Set.
16	ABPRSD	R/W1TC	0h	If an Attention Button is implemented, this bit is Set when the attention button is pressed. If an Attention Button is not supported, this bit must not be Set.
15:13	RSCS1	R	0h	Reserved
12	DLLSCE	R/W	0h	If the Data Link Layer Link Active Reporting capability is 1b, this bit enables software notification when Data Link Layer Link Active bit is changed. If the Data Link Layer Link Active Reporting Capable bit is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.
11	EMIC	R	0h	If an Electromechanical Interlock is implemented, a write of 1b to this bit causes the state of the interlock to toggle. A write of 0b to this bit has no effect. A read of this bit always returns a 0b.

Table 14-19483. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PCC	R/W	1h	If a Power Controller is implemented, this bit when written sets the power state of the slot per the defined encodings. Reads of this bit must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write, if required to, without waiting for the previous command to complete in which case the read value is undefined. The defined encodings are: 0b Power On 1b Power Off
9:8	PIC	R/W	3h	If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write,Defined encodings are: 00b Reserved 01b On 10b Blink 11b Off
7:6	AIC	R/W	3h	If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write,Defined encodings are: 00b Reserved 01b On 10b Blink 11b Off
5	HPIE	R/W	0h	When Set, this bit enables generation of an interrupt on enabled hot-plug events. If the Hot Plug Capable bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.
4	CCIE	R/W	0h	If Command Completed notification is supported [if the No Command Completed Support bit in the Slot Capabilities register is 0b], when Set, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, this bit must be hardwired to 0b. Default value of this bit is 0b.
3	PDCE	R/W	0h	When Set, this bit enables software notification on a presence detect changed event. If the Hot-Plug Capable bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.
2	MSCE	R/W	0h	When Set, this bit enables software notification on a MRL sensor changed event If the MRL Sensor Present bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.
1	PFDE	R/W	0h	When Set, this bit enables software notification on a power fault event If a Power Controller that supports power fault detection is not implemented, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.

Table 14-19483. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SLOT_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ABPE	R/W	0h	When Set to 1b, this bit enables software notification on an attention button pressed event. If the Attention Button Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.

14.9.2.2.2.67 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_CTRL_CAP Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_CTRL_CAP Register (Offset = DCh) [reset = 0h]

This register controls and identifies PCI Express Root Complex specific parameters.

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Table 14-19484. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00DCh**

Figure 14-6435. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_CTRL_CAP Name Register

31	30	29	28	27	26	25	24
R27							
R							
0h							
23	22	21	20	19	18	17	16
R27							
R							
0h							
15	14	13	12	11	10	9	8
R27							
R							
0h							
7	6	5	4	3	2	1	0
R27			CRSSVE	PMEIE	SEFEE	SENFEE	SECEE
R			R	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-19486. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_CTRL_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	R27	R	0h	Reserved
4	CRSSVE	R	0h	This capability is not implemented and this bit is hardwired to 0b.
3	PMEIE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
2	SEFEE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
1	SENFEE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
0	SECEE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.

14.9.2.2.2.68 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_STATUS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_STATUS Register (Offset = E0h) [reset = 0h]

This register controls and identifies PCI Express Root Complex specific parameters.

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Table 14-19487. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00E0h**

Figure 14-6436. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R18</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">R18</td><td>PMEP</td><td>PMES</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PMERID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PMERID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19489. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	R18	R	0h	Reserved
17	PMEP	R	0h	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
16	PMES	R/W1TC	0h	This field is not set by the Controller but can be cleared by writing a 1 from the local management APB bus. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
15:0	PMERID	R	0h	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

14.9.2.2.2.69 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_2 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_2 Register (Offset = E4h) [reset = 740812h]

This register advertises the capabilities of the PCI Express device.

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Table 14-19490. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00E4h**

Figure 14-6437. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_2 Name Register

31	30	29	28	27	26	25	24
R16							
R							
0h							

23	22	21	20	19	18	17	16
MEEP		EEPS	EXFS	OBFF		RESERVED	
R		R	R	R		NONE	
1h		1h	1h	1h		0h	

15	14	13	12	11	10	9	8
R15		RESERVED	TPHC	LMS	R14	ACS128	ACS64
R		NONE	R	R	R	R	R
0h		0h	0h	1h	0h	0h	0h

7	6	5	4	3	2	1	0
ACS32	AOPRS	AFS	CTDS	CTR			
R	R	R	R	R			
0h	0h	0h	1h	2h			

Table 14-19492. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	R16	R	0h	Reserved
23:22	MEEP	R	1h	Indicates the maximum number of End-End TLP Prefixes supported by the Function. The supported values are: 01b 1 End-End TLP Prefix 10b 2 End-End TLP Prefixes. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write
21	EEPS	R	1h	Indicates whether the Function supports End-End TLP Prefixes. A 1 in this field indicates that the Function supports receiving TLPs containing End-End TLP Prefixes. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write
20	EXFS	R	1h	Indicates that the Function supports the 3-bit definition of the Fmt field in the TLP header. This bit is hardwired to 1 for all Physical Functions.
19:18	OBFF	R	1h	A 1 in this bit position indicates that the Function supports the Optimized Buffer Flush/Fill [OBFF] capability using message signaling. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write
17:16	RESERVED	NONE	0h	Reserved

Table 14-19492. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_CAP_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	R15	R	0h	Reserved
13	RESERVED	NONE	0h	Reserved
12	TPHC	R	0h	Hardwired to 0.
11	LMS	R	1h	A value of 1b indicates support for the optional Latency Tolerance Reporting [LTR] mechanism. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
10	R14	R	0h	Reserved
9	ACS128	R	0h	Hardwired to 0.
8	ACS64	R	0h	Hardwired to 0.
7	ACS32	R	0h	Hardwired to 0.
6	AOPRS	R	0h	Applicable only to Switch Upstream Ports, Switch Downstream Ports, and Root Ports; must be 0b for other Function types. This bit must be set to 1b if the Port supports this optional capability. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
5	AFS	R	0h	hard coded to zero
4	CTDS	R	1h	A 1 in this field indicates that the associated Function supports the capability to turn off its Completion timeout. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
3:0	CTR	R	2h	Specifies the Completion Timeout values supported by the device. This field is set by default to 0010 [10 ms - 250 ms], but can be modified from the local management APB bus. The actual timeout values are in two programmable local management registers, which allow the timeout settings of the two sub-ranges within Range B to be programmed independently. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

14.9.2.2.2.70 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS_2 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS_2 Register (Offset = E8h) [reset = 0h]

This register contains control and status bits associated with the device.

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Table 14-19493. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00E8h**

Figure 14-6438. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS_2 Name Register

31	30	29	28	27	26	25	24
R20							
R							
0h							
23	22	21	20	19	18	17	16
R20							
R							
0h							
15	14	13	12	11	10	9	8
R20	OBFFE		RESERVED	R19	LTRME	ICE	IRE
R	R/W		NONE	R	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
R18	AORE	AFE	CTD	CTV			
R	R	R	R/W	R/W			
0h	0h	0h	0h	0h			

Table 14-19495. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	R20	R	0h	N/A
14:13	OBFFE	R/W	0h	Enables the Optimized Buffer Flush/Fill [OBFF] capability in the device. Valid settings are 00 [disabled], 01 [Variation A], and 10 [Variation B].
12	RESERVED	NONE	0h	Reserved
11	R19	R	0h	Reserved
10	LTRME	R/W	0h	This must be set to 1 to enable the Latency Tolerance Reporting Mechanism. This bit is implemented only in PF 0. Its default value is 1, but can be modified from the local management bus. This bit is read-only in PF 1.
9	ICE	R/W	0h	When this bit is 1, the RC is allowed to set the ID-based Ordering [IDO] Attribute bit in the Completions it generates.
8	IRE	R/W	0h	When this bit is 1, the RC is allowed to set the ID-based Ordering [IDO] Attribute bit in the requests it generates.
7	R18	R	0h	Reserved

Table 14-19495. PCIE_CORE_RC_I_RC_PCIE_BASE_I_PCIE_DEV_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AORE	R	0h	This bit must be set to enable the generation of Atomic Op Requests. If the client logic attempts to send an Atomic Op when this bit is not set, logic in the Controller will nullify the TLP on its way to the link.
5	AFE	R	0h	A 1 in this filed indicates that the port treats fields 7:0 of the ID as function number while converting a Type 1 config packet to type 0 config packet.
4	CTD	R/W	0h	Setting this bit disables the Completion Timeout in the device.
3:0	CTV	R/W	0h	Specifies the Completion Timeout value for the device. Allowable values are 0101 [sub-range 1] and 0110 [sub-range 2]. The corresponding timeout values are stored in the local management register's Completion Timeout Interval Registers 0 and 1, respectively. Value of 0 selects completion timeout from Completion-Timeout-Interval-Registers-0 in local management register.

14.9.2.2.2.71 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP_2 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP_2 Register (Offset = ECh) [reset = Eh]

This register advertises the supported link speeds of the Controller.

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Table 14-19496. Instance Table

Instance Name	**Physical Address**
PCIE0	**0D00 00ECh**

Figure 14-6439. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP_2 Name Register

31	30	29	28	27	26	25	24
R31	R25						R23
R	R						R
0h	0h						0h
23	22	21	20	19	18	17	16
R23	R3			RESERVED	LSORSSV		
R	R			NONE	R		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
R2				LSOGSSV			R1
R				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
R1			RESERVED	SLSV			RESERVED
R			NONE	R			NONE
0h			0h	7h			0h

Table 14-19498. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R31	R	0h	Indicates support for the optional Device Readiness Status [DRS] capability. This capability is currently not supported in the Controller.
30:25	R25	R	0h	Reserved
24:23	R23	R	0h	Reserved
22:20	R3	R	0h	Reserved
19	RESERVED	NONE	0h	Reserved
18:16	LSORSSV	R	0h	If this field is non-zero, it indicates that the Port, when operating at the indicated speed[s] supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS.
15:12	R2	R	0h	Reserved
11:9	LSOGSSV	R	0h	If this field is non-zero, it indicates that the Port, when operating at the indicated speed[s] supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate.
8:5	R1	R	0h	Reserved
4	RESERVED	NONE	0h	Reserved

Table 14-19498. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CAP_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:1	SLSV	R	7h	This field indicates the supported link speeds of the Controller. For each bit, a value of 1 indicates that the corresponding link speed is supported, while a value of 0 indicates that the corresponding speed is not supported. The bits corresponding to various link speeds are: Bit 1 = Link Speed 2.5 GT/s, Bit 2 = Link Speed 5 GT/s, Bit 3 = Link Speed 8 GT/s. This field is hardwired to 0001 [2.5 GT/s] when the PCIE_GENERATION_SEL strap pins of the Controller are set to 0, 0011 [2.5 and 5 GT/s] when the strap is set to 1, and 0111 [2.5, 5, and 8 GT/s] when the strap pin is set to 10.
0	RESERVED	NONE	0h	Reserved

14.9.2.2.2.72 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS_2 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS_2 Register (Offset = F0h) [reset = 10003h]

This register contains control and status bits specific to the PCI Express link.

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Table 14-19499. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00F0h**

Figure 14-6440. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS_2 Name Register

31	30	29	28	27	26	25	24
R21							
R							
0h							
23	22	21	20	19	18	17	16
R21		LE	EP3S	EP2S	EP1S	EQC	CDEL
R		R/W1TC	R	R	R	R	R
0h		0h	0h	0h	0h	0h	1h
15	14	13	12	11	10	9	8
CD				CS	EMC	TM	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
7	6	5	4	3	2	1	0
TM	SD	HASD	EC	TLS			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	3h			

Table 14-19501. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	R21	R	0h	Reserved
21	LE	R/W1TC	0h	When the Controller [RP] receives an 8GTs equalization request from an Upstream Port the Controller internally sets this bit to 1. [i.e. when RP is in the Recovery.RcvrCfg state and receives 8 consecutive TS2 Ordered Sets with the Request Equalization bit set to 1b] The LOCAL_INTERRUPT output is also asserted if Link Equalization Request Interrupt Enable is enabled.
20	EP3S	R	0h	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully. STICKY
19	EP2S	R	0h	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully. STICKY
18	EP1S	R	0h	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully. STICKY
17	EQC	R	0h	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed. STICKY

Table 14-19501. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CDEL	R	1h	This status bit indicates the current operating de-emphasis level of the transmitter [0 = -6dB, 1 = -3.5dB].
15:12	CD	R/W	0h	This bit sets the de-emphasis level [for 5 GT/s operation] or the Transmitter Preset level [for 8 GT/s operation] when the LTSSM enters the Polling.Compliance state because of software setting the Enter Compliance bit in this register. It is used only when the link is running at 5 GT/s or 8 GT/s. At 5 GT/s, the only valid setting are 0 [-6 dB] and 1 [-3.5 dB]. STICKY
11	CS	R/W	0h	When this bit is set to 1, the device will transmit SKP ordered sets between compliance patterns. STICKY
10	EMC	R/W	0h	This field is intended for debug and compliance testing purposes only. If this bit is set to 1, the device will transmit the Modified Compliance Pattern when the LTSSM enters the Polling.Compliance substate. STICKY
9:7	TM	R/W	0h	This field is intended for debug and compliance testing purposes only. It controls the non-deemphasized voltage level at the transmitter outputs. Its encodings are: 000 = Normal operating range, 001 = 800 - 1200 mV for full swing and 400 - 700 mV for half swing, 010 - 111 = See PCI Express Base Specification 2.0. This field is reset to 0 when th LTSSM enters the Polling.Configuration substate during link training. STICKY.
6	SD	R/W	0h	This bit selects the de-emphasis level when the Controller is operating at 5 GT/s [0 = -6 dB, 1 = -3.5 dB].
5	HASD	R/W	0h	When this bit is set, the LTSSM is prevented from changing the operating speed of the link, other than reducing the speed to correct unreliable operation of the link. STICKY
4	EC	R/W	0h	This bit is used to force the Endpoint device to enter the Compliance mode. Software sets this bit to 1 and initiates a hot reset to force the device into the Compliance mode. The target speed for the Compliance mode is determined by the Target Link Speed field of this register. STICKY.
3:0	TLS	R/W	3h	This field sets the target speed when the software forces the link into Compliance mode by setting the Enter Compliance bit in this register [0001 = 2.5 GT/s, 0010 = 5 GT/s, 0100 = 8 GT/s]. The default value of this field is 0001 [2.5 GT/s] when the PCIE_GENERATION_SEL[1:0] strap pins of the Controller are set to 0, 0010 [5 GT/s] when the strap is set to 1, and 0011 [8 GT/s] when the strap pin is set to 10 . STICKY.

14.9.2.2.2.73 PCIE_CORE_RC_I_RC_PCIE_BASE_I_AER_ENHNCD_CAP Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_AER_ENHNCD_CAP Register (Offset = 100h) [reset = 15020001h]

This is the first register in the PCI Express Advanced Error Reporting Capability Structure. This register contains the PCI Express Extended Capability ID, the capability version , and the pointer to the next capability structure.

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Table 14-19502. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0100h**

Figure 14-6441. PCIE_CORE_RC_I_RC_PCIE_BASE_I_AER_ENHNCD_CAP Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NCO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">150h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">NCO</td><td colspan="4">CV</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">150h</td><td colspan="4">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PECID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PECID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-19504. PCIE_CORE_RC_I_RC_PCIE_BASE_I_AER_ENHNCD_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NCO	R	150h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19:16	CV	R	2h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 4'h2.
15:0	PECID	R	1h	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express AER Extended Capability Structure [0001 hex].

14.9.2.2.2.74 PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_STATUS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_STATUS Register (Offset = 104h) [reset = 0h]

This register provides the status of the various uncorrectable errors detected by the PCI Express Controller. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Uncorrectable Error Mask Register have no effect on the status bits of this register. In the case of certain errors detected by the Transaction Layer, the associated TLP header is logged in the Header Log Registers.

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Table 14-19505. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0104h**

Figure 14-6442. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_STATUS Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td colspan="8">R28</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td>R28</td><td>UIE</td><td>R27</td><td>URE</td><td>EE</td><td>MT</td><td>RO</td><td>UC</td></tr>
<tr><td>R</td><td>R/W1TC</td><td>R</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td>CA</td><td>CT</td><td>FCPE</td><td>PT</td><td colspan="4">R26</td></tr>
<tr><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="2">R26</td><td>SDES</td><td>DLPE</td><td colspan="3">R25</td><td>LTE</td></tr>
<tr><td colspan="2">R</td><td>R/W1TC</td><td>R/W1TC</td><td colspan="3">R</td><td>R/W1TC</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-19507. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	R28	R	0h	Reserved
22	UIE	R/W1TC	0h	This bit is set when the Controller has detected an internal uncorrectable error [HAL parity error or an uncorrectable ECC error while reading from any of the RAMs]. This bit is also set in response to the client signaling an internal error through the input UNCORRECTABLE_ERROR_IN. This error is considered fatal by default.
21	R27	R	0h	Reserved
20	URE	R/W1TC	0h	This bit is set when the Controller has received a request from the link that it does not support. This error is not Function-specific. This error is considered non-fatal by default, except for the special case outlined in PCI Express Base Specification 2.0. The header of the received request that caused the error is logged in the Header Log Registers.

Table 14-19507. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	EE	R/W1TC	0h	This bit is set when the Controller has detected an ECRC error in a received TLP.
18	MT	R/W1TC	0h	This bit is set when the Controller receives a malformed TLP from the link. This error is considered fatal by default. The header of the received TLP with error is logged in the Header Log Registers.
17	RO	R/W1TC	0h	This bit is set when the Controller receives a TLP in violation of the receive credit currently available.
16	UC	R/W1TC	0h	This bit is set when the Controller has received an unexpected Completion packet from the link.
15	CA	R/W1TC	0h	This bit is set when the Controller has returned the Completer Abort [CA] status to a request received from the link. This error is considered non-fatal by default, except for the special cases outlined in PCI Express Base Specification 2.0. The header of the received request that caused the error is logged in the Header Log Registers.
14	CT	R/W1TC	0h	This bit is set when the completion timer associated with an outstanding request times out. This error is considered non-fatal by default.
13	FCPE	R/W1TC	0h	This bit is set when certain violations of the flow control protocol are detected by the Controller.
12	PT	R/W1TC	0h	This bit is set when the Controller receives a poisoned TLP from the link. This error is considered non-fatal by default. The header of the received TLP with error is logged in the Header Log Registers.
11:6	R26	R	0h	Reserved
5	SDES	R/W1TC	0h	This error status indicates Link up to Link down event. So Status bit is set upon LINK_DOWN_RESET_OUT event. This field is applicable to RC only and not for EP as per PCIE-spec.
4	DLPE	R/W1TC	0h	This bit is set when the Controller receives an Ack or Nak DLLP whose sequence does not correspond to that of an unacknowledged TLP or that of the last acknowledged TLP [for details, refer to the PCI Express Base Specifications].
3:1	R25	R	0h	N/A
0	LTE	R/W1TC	0h	This error indicates that link training is not successful and transition back to detect state. This Status bit is set on any LTSSM transition from Configuration to Detect or Recovery to Detect. This field is applicable to RC only and not for EP as per PCIE-spec.

14.9.2.2.2.75 PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_MASK Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_MASK Register (Offset = 108h) [reset = 400000h]

The mask bits in this register control the reporting of uncorrectable errors. For each error type in the Uncorrectable Error Status Register, there is a corresponding bit in this register to mask its reporting. Setting the mask bit has the following effects: (1) The occurrence of the error does not cause activation of the FATAL_ERROR_OUT or NON_FATAL_ERROR_OUT output of the Controller, depending on the severity of the error. (2) The header of the TLP in which the error was detected is not logged in the Header Log Registers. (3) The First Error Pointer in the Advanced Error Capabilities and Control Register is not updated on the detection of the error. The individual bits of the mask register are described below.

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Table 14-19508. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0108h**

Figure 14-6443. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_MASK Name Register

31	30	29	28	27	26	25	24
R32							
R							
0h							
23	22	21	20	19	18	17	16
R32	UIEM	R31	UREM	EEM	MTM	ROM	UCM
R	R/W	R	R/W	R/W	R/W	R/W	R/W
0h	1h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CAM	CTM	FCPER	PTM	R30			
R/W	R/W	R/W	R/W	R			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
R30		SDESM	DLPER	R29			LTEM
R		R/W	R/W	R			R/W
0h		0h	0h	0h			0h

Table 14-19510. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	R32	R	0h	Reserved
22	UIEM	R/W	1h	This bit is set to mask the reporting of internal errors. STICKY.
21	R31	R	0h	Reserved
20	UREM	R/W	0h	This bit is set to mask the reporting of unexpected requests received from the link. STICKY.
19	EEM	R/W	0h	This bit is set to mask the reporting of ECRC errors. STICKY.
18	MTM	R/W	0h	This bit is set to mask the reporting of malformed TLPs received from the link. STICKY.
17	ROM	R/W	0h	This bit is set to mask the reporting of violations of receive credit. STICKY.
16	UCM	R/W	0h	This bit is set to mask the reporting of unexpected Completions received by the Controller. STICKY.
15	CAM	R/W	0h	This bit is set to mask the reporting of the Controller sending a Completer Abort. STICKY.

Table 14-19510. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	CTM	R/W	0h	This bit is set to mask the reporting of Completion Timeouts. STICKY.
13	FCPER	R/W	0h	This bit is set to mask the reporting of Flow Control Protocol Errors. STICKY.
12	PTM	R/W	0h	This bit is set to mask the reporting of a Poisoned TLP. STICKY.
11:6	R30	R	0h	Reserved
5	SDESM	R/W	0h	This bit is set to mask the reporting of Surprise Down Error Status Mask. STICKY. This field is applicable to RC only and not for EP as per PCIE-spec.
4	DLPER	R/W	0h	This bit is set to mask the reporting of Data Link Protocol Errors. STICKY.
3:1	R29	R	0h	Reserved
0	LTEM	R/W	0h	This bit is set to mask the reporting of Link Training Error Mask. STICKY. This field is applicable to RC only and not for EP as per PCIE-spec.

14.9.2.2.2.76 PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_SEVERITY Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_SEVERITY Register (Offset = 10Ch) [reset = 462030h]

The setting of this register determines whether an uncorrectable error is reported as a fatal error or non-fatal, that is, whether the FATAL_ERROR_OUT or NON_FATAL_ERROR_OUT output of the Controller is activated. If a severity bit of this register is 0,the corresponding error is reported by the Controller by asserting NON_FATAL_ERROR_OUT. Otherwise, it is reported by asserting FATAL_ERROR_OUT.

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Table 14-19511. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 010Ch**

Figure 14-6444. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_SEVERITY Name Register

31	30	29	28	27	26	25	24
R37							
R							
0h							
23	22	21	20	19	18	17	16
R37	UNCORR_INTRNL_ERR_SVRTY	R36	URES	EES	MTS	ROS	UCS
R	R/W	R	R/W	R/W	R/W	R/W	R/W
0h	1h	0h	0h	0h	1h	1h	0h
15	14	13	12	11	10	9	8
CAS	CTS	FCPES	PTS	R35			
R/W	R/W	R/W	R/W	R			
0h	0h	1h	0h	0h			
7	6	5	4	3	2	1	0
R35		SDES	DLPES	R33			LTES
R		R/W	R/W	R			R/W
0h		1h	1h	0h			0h

Table 14-19513. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_SEVERITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	R37	R	0h	N/A
22	UNCORR_INTRNL_ERR_SVRTY	R/W	1h	Severity of internal errors [0 = Non-Fatal, 1 = Fatal].
21	R36	R	0h	Reserved
20	URES	R/W	0h	Severity of unexpected requests received from the link [0 = Non-Fatal, 1 = Fatal]. STICKY.
19	EES	R/W	0h	Severity of ECRC errors [0 = Non-Fatal, 1 = Fatal]. STICKY.
18	MTS	R/W	1h	Severity of malformed TLPs received from the link [0 = Non-Fatal, 1 = Fatal]. STICKY.
17	ROS	R/W	1h	Severity of receive credit violations [0 = Non-Fatal, 1 = Fatal]. STICKY.
16	UCS	R/W	0h	Severity of unexpected Completions received by the Controller [0 = Non-Fatal, 1 = Fatal]. STICKY.

Table 14-19513. PCIE_CORE_RC_I_RC_PCIE_BASE_I_UNCORR_ERR_SEVERITY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	CAS	R/W	0h	Severity of sending a Completer Abort [0 = Non-Fatal, 1 = Fatal]. STICKY.
14	CTS	R/W	0h	Severity of Completion Timeouts [0 = Non-Fatal, 1 = Fatal]. STICKY.
13	FCPES	R/W	1h	Severity of a Flow Control Protocol Error [0 = Non-Fatal, 1 = Fatal]. STICKY.
12	PTS	R/W	0h	Severity of a Poisoned TLP error [0 = Non-Fatal, 1 = Fatal]. STICKY.
11:6	R35	R	0h	N/A
5	SDES	R/W	1h	surprise down error severity [0 = Non-Fatal, 1 = Fatal]. STICKY. This field is applicable to RC only and not for EP as per PCIE-spec.
4	DLPES	R/W	1h	Severity of Data Link Protocol Errors [0 = Non-Fatal, 1 = Fatal]. STICKY.
3:1	R33	R	0h	Reserved
0	LTES	R/W	0h	Severity of Link Training Error [0 = Non-Fatal, 1 = Fatal]. STICKY. This field is applicable to RC only and not for EP as per PCIE-spec.

14.9.2.2.2.77 PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_STATUS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_STATUS Register (Offset = 110h) [reset = 0h]

This register provides the status of the various correctable errors detected by the PCI Express Controller. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Correctable Error Mask Register have no effect on the status bits of this register. The setting of a correctable error status bit causes the Controller to assert the CORRECTABLE_ERROR_OUT output if the error is not masked in the Correctable Error Mask Register. Header logging of received TLPs does not apply to correctable errors.

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Table 14-19514. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0110h**

Figure 14-6445. PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R39</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R39</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>HLOS</td><td>CIES</td><td>ANES</td><td>RTTS</td><td colspan="3">R38</td><td>RNRS</td></tr>
<tr><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td colspan="3">R</td><td>R/W1TC</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>BDS</td><td>BTS</td><td colspan="5">R37</td><td>RES</td></tr>
<tr><td>R/W1TC</td><td>R/W1TC</td><td colspan="5">R</td><td>R/W1TC</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
</table>

Table 14-19516. PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R39	R	0h	Reserved
15	HLOS	R/W1TC	0h	This bit is set on a Header Log Register overflow, that is, when the header could not be logged in the Header Log Register because it is occupied by a previous header.
14	CIES	R/W1TC	0h	This bit is set when the Controller has detected an internal correctable error condition [a correctable ECC error while reading from any of the RAMs]. This bit is also set in response to the client signaling an internal error through the input CORRECTABLE_ERROR_IN.
13	ANES	R/W1TC	0h	This bit is set when an uncorrectable error occurs, which is determined to belong to one of the special cases described in the PCI Express Base Specification 2.0. This causes the Controller to assert the CORRECTABLE_ERROR_OUT output in place of NON_FATAL_ERROR_OUT.

Table 14-19516. PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RTTS	R/W1TC	0h	This bit is set when the replay timer in the Data Link Layer of the Controller times out, causing the Controller to re-transmit a TLP.
11:9	R38	R	0h	Reserved
8	RNRS	R/W1TC	0h	This bit is set when the replay count rolls over after three re-transmissions of a TLP at the Data Link Layer of the Controller.
7	BDS	R/W1TC	0h	This bit is set when an LCRC error is detected in a received DLLP, and no errors were detected by the Physical Layer.
6	BTS	R/W1TC	0h	This bit is set when an error is detected in a received TLP by the Data Link Layer of the Controller the conditions causing this error are [1] an LCRC error, [2] the packet terminates with EDB symbol, but its LCRC field does not equal the inverted value of the calculated CRC.
5:1	R37	R	0h	Reserved
0	RES	R/W1TC	0h	This bit is set when an error is detected in the receive side of the Physical Layer of the Controller [e.g. an 8b10b decode error].

14.9.2.2.2.78 PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_MASK Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_MASK Register (Offset = 114h) [reset = E000h]

The mask bits in this register control the reporting of correctable errors. For each error type in the Correctable Error Status Register, there is a corresponding bit in this register to mask its reporting. When a mask bit is set the occurrence of the error is not reported (by asserting the CORRECTABLE_ERROR_OUT output).

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Table 14-19517. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0114h**

Figure 14-6446. PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_MASK Name Register

31	30	29	28	27	26	25	24
R42							
R							
0h							
23	22	21	20	19	18	17	16
R42							
R							
0h							
15	14	13	12	11	10	9	8
HLOM	CIEM	ANEM	RTTM	R41			RNRM
R/W	R/W	R/W	R/W	R			R/W
1h	1h	1h	0h	0h			0h
7	6	5	4	3	2	1	0
BDM	BTM	R40					REM
R/W	R/W	R					R/W
0h	0h	0h					0h

Table 14-19519. PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R42	R	0h	Reserved
15	HLOM	R/W	1h	This bit, when set, masks the reporting of an error in response to a Header Log register overflow. STICKY.
14	CIEM	R/W	1h	This bit, when set, masks the reporting of an error in response to a corrected internal error condition. STICKY.
13	ANEM	R/W	1h	This bit, when set, masks the reporting of an error in response to an uncorrectable error occurence, which is determined to belong to one of the special cases in the PCI Express Base Specification 2.0. STICKY.
12	RTTM	R/W	0h	This bit, when set, masks the reporting of an error in response to a Replay Timer timeout event. STICKY.
11:9	R41	R	0h	Reserved
8	RNRM	R/W	0h	This bit, when set, masks the reporting of an error in response to a Replay Number Rollover event. STICKY.

Table 14-19519. PCIE_CORE_RC_I_RC_PCIE_BASE_I_CORR_ERR_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	BDM	R/W	0h	This bit, when set, masks the reporting of an error in response to a 'Bad DLLP' received. STICKY.
6	BTM	R/W	0h	This bit,when set, masks the reporting of an error in response to a 'Bad TLP' received. STICKY.
5:1	R40	R	0h	Reserved
0	REM	R/W	0h	This bit, when set, masks the reporting of Physical Layer errors. STICKY.

14.9.2.2.2.79 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ADV_ERR_CAP_CTL Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ADV_ERR_CAP_CTL Register (Offset = 118h) [reset = A0h]

This register contains a pointer to the first error that is reported in the Uncorrectable Error Status Register, and bits to enable ECRC generation and checking.

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Table 14-19520. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0118h**

Figure 14-6447. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ADV_ERR_CAP_CTL Name Register

31	30	29	28	27	26	25	24
R43							
R							
0h							
23	22	21	20	19	18	17	16
R43							
R							
0h							
15	14	13	12	11	10	9	8
R43				TPLP	MHRE	MHRC	EEC
R				R	R	R	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
ECC	EEG	EGC	FEP				
R	R/W	R	R				
1h	0h	1h	0h				

Table 14-19522. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ADV_ERR_CAP_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	R43	R	0h	Reserved
11	TPLP	R	0h	If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is RsvdP if the End-End TLP Prefix Supported bit is CIf Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined.
10	MHRE	R	0h	Setting this bit enables the RC to log multiple error headers in its Header Log Registers. It is hardwired to 0.
9	MHRC	R	0h	This bit is set when the RC has the capability to log more than one error header in its Header Log Registers. It is hardwired to 0.
8	EEC	R/W	0h	Setting this bit enables ECRC checking on the receive side of the Controller. This bit is writable from the local management bus. STICKY.

Table 14-19522. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ADV_ERR_CAP_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ECC	R	1h	This read-only bit indicates to the software that the device is capable of checking ECRC in packets received from the link.
6	EEG	R/W	0h	Setting this bit enables the ECRC generation on the transmit side of the Controller. This bit is writable from the local management bus. STICKY.
5	EGC	R	1h	This read-only bit indicates to the software that the device is capable of generating ECRC in packets transmitted on the link.
4:0	FEP	R	0h	This is a 5-bit pointer to the bit position in the Uncorrectable Error Status Register corresponding to the error that was detected first. When there are multiple bits set in the Uncorrectable Error Status Register, this field informs the software which error was observed first. To prevent the field from being overwritten before the software is able to read it, this field is not updated while the status bit it points to in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will update the First Error Pointer. Any uncorrectable error type, including the special cases where the error is reported using an ERR_COR message, will set the First Error Pointer [assuming the software has reset the error pointed by it in the Uncorrectable Error Status Register]. STICKY.

14.9.2.2.2.80 PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_0 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_0 Register (Offset = 11Ch) [reset = 0h]

This is the first of a set of four registers used to capture the header of a TLP received by the Controller from the link upon detection of an uncorrectable error. When multiple bits are set in the Uncorrectable Error Status Register, the captured header corresponds the the error that was detected first, that is, the error pointed by the First Error Pointer. To prevent the captured header from being over-written before software is able to read it, this register is not updated while the status bit pointed to by the First Error Pointer in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will also cause the Header Log Registers to be updated. The doublewords of the TLP header are stored in the Header Log Registers with their bytes transposed. That is, the byte containing the Type/Format fields of the header is stored at bit positions 31:24 of the Header Log Register 0.

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Table 14-19523. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 011Ch**

Figure 14-6448. PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_0 Name Register

31	30	29	28	27	26	25	24
HD0							
R							
0h							
23	22	21	20	19	18	17	16
HD0							
R							
0h							
15	14	13	12	11	10	9	8
HD0							
R							
0h							
7	6	5	4	3	2	1	0
HD0							
R							
0h							

Table 14-19525. PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HD0	R	0h	First Dword of captured TLP header. STICKY.

14.9.2.2.2.81 PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_1 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_1 Register (Offset = 120h) [reset = 0h]

This register contains the second Dword of the captured TLP header. The bytes are stored in transposed order.

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Table 14-19526. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0120h**

Figure 14-6449. PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_1 Name Register

31	30	29	28	27	26	25	24
HD1							
R							
0h							
23	22	21	20	19	18	17	16
HD1							
R							
0h							
15	14	13	12	11	10	9	8
HD1							
R							
0h							
7	6	5	4	3	2	1	0
HD1							
R							
0h							

Table 14-19528. PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HD1	R	0h	Second Dword of captured TLP header. STICKY.

14.9.2.2.2.82 PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_2 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_2 Register (Offset = 124h) [reset = 0h]

This register contains the third Dword of the captured TLP header. The bytes are stored in transposed order.

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Table 14-19529. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0124h**

Figure 14-6450. PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_2 Name Register

31	30	29	28	27	26	25	24
HD2							
R							
0h							
23	22	21	20	19	18	17	16
HD2							
R							
0h							
15	14	13	12	11	10	9	8
HD2							
R							
0h							
7	6	5	4	3	2	1	0
HD2							
R							
0h							

Table 14-19531. PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HD2	R	0h	Third Dword of captured TLP header. STICKY.

14.9.2.2.2.83 PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_3 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_3 Register (Offset = 128h) [reset = 0h]

If the captured TLP header is 4 Dwords long, this register contains its fourth Dword. If the captured header is a 3-Dword header, this register is unused. The bytes of the Dword are stored in this register in transposed order.

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Table 14-19532. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0128h**

Figure 14-6451. PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_3 Name Register

31	30	29	28	27	26	25	24
HD3							
R							
0h							
23	22	21	20	19	18	17	16
HD3							
R							
0h							
15	14	13	12	11	10	9	8
HD3							
R							
0h							
7	6	5	4	3	2	1	0
HD3							
R							
0h							

Table 14-19534. PCIE_CORE_RC_I_RC_PCIE_BASE_I_HDR_LOG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HD3	R	0h	Fourth Dword of captured TLP header. STICKY.

14.9.2.2.2.84 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_CMD Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_CMD Register (Offset = 12Ch) [reset = 0h]

This register contains bits that control how the RC responds to errors reported by remote devices.

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Table 14-19535. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 012Ch**

Figure 14-6452. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_CMD Name Register

31	30	29	28	27	26	25	24
R44							
R							
0h							
23	22	21	20	19	18	17	16
R44							
R							
0h							
15	14	13	12	11	10	9	8
R44							
R							
0h							
7	6	5	4	3	2	1	0
R44					FERE	NFERE	CERE
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-19537. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	R44	R	0h	Reserved
2	FERE	R/W	0h	If this bit is set, the Controller will active its FATAL_ERROR_OUT output in response to an error message received from the link.
1	NFERE	R/W	0h	If this bit is set, the Controller will active its NON_FATAL_ERROR_OUT output in response to an error message received from the link.
0	CERE	R/W	0h	If this bit is set, the Controller will active its CORRECTABLE_ERROR_OUT output in response to an error message received from the link.

14.9.2.2.2.85 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_STAT Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_STAT Register (Offset = 130h) [reset = 0h]

This register contains status information on error messages received from the link (that is, errors reported by remote devices attached to this Root Complex).

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Table 14-19538. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0130h**

Figure 14-6453. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_STAT Name Register

31	30	29	28	27	26	25	24
R45							
R							
0h							
23	22	21	20	19	18	17	16
R45							
R							
0h							
15	14	13	12	11	10	9	8
R45							
R							
0h							
7	6	5	4	3	2	1	0
R45	FEMR	NEMR	FUF	MEFNR	EFNR	MECR	ECR
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19540. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	R45	R	0h	Reserved
6	FEMR	R/W1TC	0h	This bit, when set, indicates that the RC has received one or more Fatal error messages from the link. STICKY
5	NEMR	R/W1TC	0h	This bit, when set, indicates that the RC has received one or more Non-Fatal error messages from the link. STICKY
4	FUF	R/W1TC	0h	This bit, when set, indicates that the first Uncorrectable error message received was for a Fatal error. STICKY
3	MEFNR	R/W1TC	0h	This bit is set when the RC receives either a Fatal or Non-Fatal error message from the link, and the ERR_FATAL/NONFATAL Received bit is already set. STICKY
2	EFNR	R/W1TC	0h	This bit is set when the RC receives either a Fatal or Non-Fatal error message from the link. STICKY
1	MECR	R/W1TC	0h	This bit is set when the RC receives a Correctable error message from the link, if the ERR_COR received bit is already set. STICKY

Table 14-19540. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ROOT_ERR_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECR	R/W1TC	0h	This bit is set when the RC receives a Correctable error message from the link. STICKY

14.9.2.2.2.86 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ERR_SRC_ID Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_ERR_SRC_ID Register (Offset = 134h) [reset = 0h]

This register stores the Register IDs extracted from error messages received by the Root Complex from the link.

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Table 14-19541. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0134h**

Figure 14-6454. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ERR_SRC_ID Name Register

31	30	29	28	27	26	25	24
EFNSI							
R							
0h							
23	22	21	20	19	18	17	16
EFNSI							
R							
0h							
15	14	13	12	11	10	9	8
ECSI							
R							
0h							
7	6	5	4	3	2	1	0
ECSI							
R							
0h							

Table 14-19543. PCIE_CORE_RC_I_RC_PCIE_BASE_I_ERR_SRC_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	EFNSI	R	0h	This field captures and stores the Requester ID from an ERR_FATAL or ERROR_NONFATAL message received by the RC, if the ERR_FATAL or NONFATAL Received bit was not set at the time the message was received. STICKY
15:0	ECSI	R	0h	This field captures and stores the Requester ID from an ERR_COR message received by the RC, if the ERR_COR bit was not set at the time the message was received. STICKY

14.9.2.2.2.87 PCIE_CORE_RC_I_RC_PCIE_BASE_I_TLP_PRE_LOG_0 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_TLP_PRE_LOG_0 Register (Offset = 138h) [reset = 0h]

First TLP Prefix (if present) associated with the TLP whose header is in the Header Log Register. The bytes are in transposed order.

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Table 14-19544. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0138h

Figure 14-6455. PCIE_CORE_RC_I_RC_PCIE_BASE_I_TLP_PRE_LOG_0 Name Register

31	30	29	28	27	26	25	24
HD1							
R							
0h							
23	22	21	20	19	18	17	16
HD1							
R							
0h							
15	14	13	12	11	10	9	8
HD1							
R							
0h							
7	6	5	4	3	2	1	0
HD1							
R							
0h							

Table 14-19546. PCIE_CORE_RC_I_RC_PCIE_BASE_I_TLP_PRE_LOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HD1	R	0h	First TLP Prefix of captured TLP STICKY.

14.9.2.2.2.88 PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_CAP_HDR Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_CAP_HDR Register (Offset = 150h) [reset = 30010003h]

This register contains the PCI Express Extended Capability ID for Device Serial Number Capability, the capability version, and the pointer to the next capability structure.

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Table 14-19547. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0150h**

Figure 14-6456. PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_CAP_HDR Name Register

31	30	29	28	27	26	25	24
SNNCO							
R							
300h							
23	22	21	20	19	18	17	16
SNNCO				DSNCV			
R				R			
300h				1h			
15	14	13	12	11	10	9	8
PECID							
R							
3h							
7	6	5	4	3	2	1	0
PECID							
R							
3h							

Table 14-19549. PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	SNNCO	R	300h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19:16	DSNCV	R	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus by writing into Function 0 from the local management bus.
15:0	PECID	R	3h	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express Device Serial Number Capability [0001 hex].

14.9.2.2.2.89 PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_0 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_0 Register (Offset = 154h) [reset = 0h]

This read-only register stored the first 32 bits of the device's serial number.

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Table 14-19550. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0154h**

Figure 14-6457. PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_0 Name Register

31	30	29	28	27	26	25	24
DSND0							
R							
0h							
23	22	21	20	19	18	17	16
DSND0							
R							
0h							
15	14	13	12	11	10	9	8
DSND0							
R							
0h							
7	6	5	4	3	2	1	0
DSND0							
R							
0h							

Table 14-19552. PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DSND0	R	0h	This field contains the first 32 bits of the device's serial number. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

14.9.2.2.2.90 PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_1 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_1 Register (Offset = 158h) [reset = 0h]

This read-only register stored the last 32 bits of the device's serial number.

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Table 14-19553. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0158h

Figure 14-6458. PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_1 Name Register

31	30	29	28	27	26	25	24
DSND1							
R							
0h							
23	22	21	20	19	18	17	16
DSND1							
R							
0h							
15	14	13	12	11	10	9	8
DSND1							
R							
0h							
7	6	5	4	3	2	1	0
DSND1							
R							
0h							

Table 14-19555. PCIE_CORE_RC_I_RC_PCIE_BASE_I_DEV_SER_NUM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DSND1	R	0h	This field contains the last 32 bits of the device's serial number. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

14.9.2.2.2.91 PCIE_CORE_RC_I_RC_PCIE_BASE_I_SEC_PCIE_CAP_HDR_REG Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_SEC_PCIE_CAP_HDR_REG Register (Offset = 300h) [reset = 4C010019h]

This register contains the PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability, its capability version, and the pointer to the next capability structure. This register is implemented only in the configuration space of PF 0 or RC.

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Table 14-19556. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0300h**

Figure 14-6459. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SEC_PCIE_CAP_HDR_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NCO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4C0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">NCO</td><td colspan="4">CV</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">4C0h</td><td colspan="4">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PECI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">19h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PECI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">19h</td></tr>
</table>

Table 14-19558. PCIE_CORE_RC_I_RC_PCIE_BASE_I_SEC_PCIE_CAP_HDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NCO	R	4C0h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19:16	CV	R	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1 , but can be modified independently for each PF from [the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write] .
15:0	PECI	R	19h	This field is hardwired to the Capability ID assigned by PCI SIG to the Secondary PCI Express Capability

14.9.2.2.2.92 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CONTROL3 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CONTROL3 Register (Offset = 304h) [reset = 0h]

This register is part of the Secondary PCI Express Extended Capability Structure. It contains bits to control the link equalization procedure at 8 GT/s speed.

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Table 14-19559. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0304h**

Figure 14-6460. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CONTROL3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">R2</td><td colspan="3">ELSOSGV</td><td>R1</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R/W</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">R1</td><td>LERIE</td><td>PE</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-19561. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LINK_CONTROL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	R2	R	0h	Reserved
11:9	ELSOSGV	R/W	0h	When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture.
8:2	R1	R	0h	Reserved
1	LERIE	R/W	0h	This bit enables the activation of the LOCAL_INTERRUPT_OUT output of the Controller when the Link Equalization Request bit in the Link Status 2 Register Or the Link Equalization Request 16.0 GT/s in the 16GTs Status Register is set.
0	PE	R/W	0h	The state of this bit determines whether the Controller performs link equalization when the link is retrained by the local software. If this bit is set to 1 when the local software sets the Link Retrain bit in the Link Control Register, and the target link speed is 8 GT/s, the LTSSM of the Controller will go through the link equalization states during the retraining.

14.9.2.2.2.93 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_ERROR_STATUS Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_ERROR_STATUS Register (Offset = 308h) [reset = 0h]

This register contains one bit per lane indicating the physical-layer error status of the corresponding lane. A 1 indicates that a physical-layer error was detected by the Controller in the corresponding lane. The error can be cleared by writing a 1 into the bit position, either through a Configuration Write transaction from the link or from the local management APB bus.

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Table 14-19562. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0308h**

Figure 14-6461. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_ERROR_STATUS Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
R0							LES
R							R/W1TC
0h							0h

Table 14-19564. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_ERROR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	R0	R	0h	N/A
0	LES	R/W1TC	0h	Each of these bits indicates the error status for the corresponding lane. STICKY.

14.9.2.2.2.94 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_EQUALIZATION_CONTROL_0 Register

1 PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_EQUALIZATION_CONTROL_0 Register (Offset = 30Ch) [reset = 7F7Fh]

This register contains the 8.0GT/s Transmitter Preset and the Receiver Preset Hint values for lanes 0 and 1, for use during the Link Equalization procedure.

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Table 14-19565. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 030Ch**

Figure 14-6462. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_EQUALIZATION_CONTROL_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R2_11</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R2_11</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>R1</td><td colspan="3">UPRPH0</td><td colspan="4">UPTP0</td></tr>
<tr><td>R</td><td colspan="3">R</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>R0_1</td><td colspan="3">DNRPH0</td><td colspan="4">DNTP0</td></tr>
<tr><td>R</td><td colspan="3">R</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-19567. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_EQUALIZATION_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R2_11	R	0h	Reserved
15	R1	R	0h	Reserved
14:12	UPRPH0	R	7h	8.0GT/s Value sent by the Controller as the Receiver Preset Hint for the remote receiver associated with Lane 0. The remote node may use this value to adapt its receiver at the start of the link equalization procedure.
11:8	UPTP0	R	Fh	8.0GT/s Value sent by the Controller as the Transmitter Preset for the remote transmitter associated with Lane 0. The remote node uses this value to set up its transmitter at the start of the link equalization procedure.
7	R0_1	R	0h	Reserved
6:4	DNRPH0	R	7h	8.0GT/s Receiver Preset Hint value to be used for the local receiver associated with Lane 0. The Controller uses this value to set up the receiver attached to Lane 0

Table 14-19567. PCIE_CORE_RC_I_RC_PCIE_BASE_I_LANE_EQUALIZATION_CONTROL_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	DNTP0	R	Fh	8.0GT/s Transmitter Preset value to be used for the local transmitter associated with Lane 0. The Controller uses this value to set up the Lane 0 transmitter during link equalization.

14.9.2.2.2.95 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_ENH_CAP_HEADER_REG Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_ENH_CAP_HEADER_REG Register (Offset = 0h) [reset = 90010002h]

This is the first register in the Virtual Channel Capability Structure. The VC Capability is present only in the configuration space of Physical Function 0. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

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Table 14-19568. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6463. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_ENH_CAP_HEADER_REG Name Register

31	30	29	28	27	26	25	24
NCO							
R							
900h							
23	22	21	20	19	18	17	16
NCO				CV			
R				R			
900h				1h			
15	14	13	12	11	10	9	8
PECID							
R							
2h							
7	6	5	4	3	2	1	0
PECID							
R							
2h							

Table 14-19570. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_ENH_CAP_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NCO	R	900h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19:16	CV	R	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.
15:0	PECID	R	2h	This field is hardwired to the Capability ID assigned by PCI SIG to the VC Capability.

14.9.2.2.2.96 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_1 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_1 Register (Offset = 4h) [reset = 3h]

This register has fields that describe the capabilities of the device with respect to the virtual channels.

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Table 14-19571. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6464. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_1 Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
R0				RESERVED	EVC		
R				NONE	R		
0h				0h	3h		

Table 14-19573. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	R0	R	0h	N/A
3	RESERVED	NONE	0h	Reserved
2:0	EVC	R	3h	N/A

14.9.2.2.2.97 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_2 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_2 Register (Offset = 8h) [reset = 0h]

This register has fields that describe the capabilities of the device with respect to the virtual channels. This register is not implemented. A read from this location returns all zeroes.

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Table 14-19574. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6465. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_2 Name Register

31	30	29	28	27	26	25	24
R1							
R							
0h							
23	22	21	20	19	18	17	16
R1							
R							
0h							
15	14	13	12	11	10	9	8
R1							
R							
0h							
7	6	5	4	3	2	1	0
R1							
R							
0h							

Table 14-19576. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CAP_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R1	R	0h	N/A

14.9.2.2.2.98 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CTRL_STS_REG Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CTRL_STS_REG Register (Offset = Ch) [reset = 0h]

This location contains the 16-bit VC Control Register and the 16-bit VC Status Register. These registers are not implemented. A read from this location returns all zeroes.

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Table 14-19577. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6466. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CTRL_STS_REG Name Register

31	30	29	28	27	26	25	24
R2							
R							
0h							
23	22	21	20	19	18	17	16
R2							
R							
0h							
15	14	13	12	11	10	9	8
R2							
R							
0h							
7	6	5	4	3	2	1	0
R2							
R							
0h							

Table 14-19579. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_PORT_VC_CTRL_STS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R2	R	0h	N/A

14.9.2.2.2.99 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_0 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_0 Register (Offset = 10h) [reset = 0h]

This register describes the capabilities associated with VC 0.

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Table 14-19580. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0010h

Figure 14-6467. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RST</td><td colspan="7">R1</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19582. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R3	R	0h	N/A
15	RST	R	0h	N/A
14:0	R1	R	0h	N/A

14.9.2.2.2.100 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_0 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_0 Register (Offset = 14h) [reset = 800000FFh]

This register contains bits to configure VC 0.

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Table 14-19583. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6468. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_0 Name Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R	R				R		
1h	0h				0h		
23	22	21	20	19	18	17	16
R5				PARS			LPAT
R				R			R
0h				0h			0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TVM							TVM0
R/W							R
7Fh							1h

Table 14-19585. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R	1h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30:27	R6	R	0h	N/A
26:24	VCI	R	0h	VC ID assigned to VC0. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23:20	R5	R	0h	N/A
19:17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 0. This bit is not implemented, and hardwired to 0.
15:8	RESERVED	NONE	0h	Reserved
7:1	TVM	R/W	7Fh	Indicates the TCs that are mapped to this VC. When bit 0 of this field is set, it indicates that TC 0 is mapped to VC 0.By default, all TCs are mapped to VC 0.
0	TVM0	R	1h	Indicates the TC0 always mapped to VC0.

14.9.2.2.2.101 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_0 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_0 Register (Offset = 18h) [reset = 0h]

This register contains status bits associated with VC 0.

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Table 14-19586. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6469. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						VCNP	PATS
NONE						R	R
0h						0h	0h

Table 14-19588. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

14.9.2.2.2.102 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_1 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_1 Register (Offset = 1Ch) [reset = 0h]

This register describes the capabilities associated with VC 1.

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Table 14-19589. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6470. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_1 Name Register

31	30	29	28	27	26	25	24
R3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RST	R1						
R	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R1							
R							
0h							

Table 14-19591. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R3	R	0h	N/A
15	RST	R	0h	N/A
14:0	R1	R	0h	N/A

14.9.2.2.2.103 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_1 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_1 Register (Offset = 20h) [reset = 1000000h]

This register contains bits to configure VC 1.

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Table 14-19592. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0020h**

Figure 14-6471. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_1 Name Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W	R				R/W		
0h	0h				1h		
23	22	21	20	19	18	17	16
R5				PARS			LPAT
R				R			R
0h				0h			0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TVM							TVM0
R/W							R
0h							0h

Table 14-19594. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30:27	R6	R	0h	N/A
26:24	VCI	R/W	1h	VC ID assigned to VC1. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23:20	R5	R	0h	N/A
19:17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 1. This bit is not implemented, and hardwired to 0.
15:8	RESERVED	NONE	0h	Reserved
7:1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 1 of this field is set, it indicates that TC 1 is mapped to VC 1.By default, all TCs are mapped to VC 0.
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

14.9.2.2.2.104 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_1 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_1 Register (Offset = 24h) [reset = 0h]

This register contains status bits associated with VC 1.

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Table 14-19595. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0024h**

Figure 14-6472. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						VCNP	PATS
NONE						R	R
0h						0h	0h

Table 14-19597. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

14.9.2.2.2.105 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_2 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_2 Register (Offset = 28h) [reset = 0h]

This register describes the capabilities associated with VC 2.

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Table 14-19598. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0028h**

Figure 14-6473. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_2 Name Register

31	30	29	28	27	26	25	24
R3							
R							
0h							
23	22	21	20	19	18	17	16
R3							
R							
0h							
15	14	13	12	11	10	9	8
RST	R1						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
R1							
R							
0h							

Table 14-19600. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R3	R	0h	N/A
15	RST	R	0h	N/A
14:0	R1	R	0h	N/A

14.9.2.2.2.106 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_2 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_2 Register (Offset = 2Ch) [reset = 2000000h]

This register contains bits to configure VC 2.

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Table 14-19601. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 002Ch**

Figure 14-6474. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_2 Name Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W	R				R/W		
0h	0h				2h		
23	22	21	20	19	18	17	16
R5				PARS			LPAT
R				R			R
0h				0h			0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TVM							TVM0
R/W							R
0h							0h

Table 14-19603. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30:27	R6	R	0h	N/A
26:24	VCI	R/W	2h	VC ID assigned to VC2. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23:20	R5	R	0h	N/A
19:17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 2. This bit is not implemented, and hardwired to 0.
15:8	RESERVED	NONE	0h	Reserved
7:1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 2 of this field is set, it indicates that TC 2 is mapped to VC 2.By default, all TCs are mapped to VC 0.
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

14.9.2.2.2.107 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_2 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_2 Register (Offset = 30h) [reset = 0h]

This register contains status bits associated with VC 2.

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Table 14-19604. Instance Table

Instance Name	**Physical Address**
PCIE0	**0D00 0030h**

Figure 14-6475. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						VCNP	PATS
NONE						R	R
0h						0h	0h

Table 14-19606. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

14.9.2.2.2.108 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_3 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_3 Register (Offset = 34h) [reset = 0h]

This register describes the capabilities associated with VC 3.

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Table 14-19607. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0034h**

Figure 14-6476. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RST</td><td colspan="7">R1</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19609. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CAP_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R3	R	0h	N/A
15	RST	R	0h	N/A
14:0	R1	R	0h	N/A

14.9.2.2.2.109 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_3 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_3 Register (Offset = 38h) [reset = 3000000h]

This register contains bits to configure VC 3.

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Table 14-19610. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0038h**

Figure 14-6477. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_3 Name Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W	R				R/W		
0h	0h				3h		
23	22	21	20	19	18	17	16
R5				PARS			LPAT
R				R			R
0h				0h			0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TVM							TVM0
R/W							R
0h							0h

Table 14-19612. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_CTRL_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30:27	R6	R	0h	N/A
26:24	VCI	R/W	3h	VC ID assigned to VC3. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23:20	R5	R	0h	N/A
19:17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 3. This bit is not implemented, and hardwired to 0.
15:8	RESERVED	NONE	0h	Reserved
7:1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 3 of this field is set, it indicates that TC 3 is mapped to VC 3.By default, all TCs are mapped to VC 0.
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

14.9.2.2.2.110 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_3 Register

1 PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_3 Register (Offset = 3Ch) [reset = 0h]

This register contains status bits associated with VC 3.

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Table 14-19613. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 003Ch**

Figure 14-6478. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						VCNP	PATS
NONE						R	R
0h						0h	0h

Table 14-19615. PCIE_CORE_RC_I_VC_CAP_STRUCT_I_VC_RES_STS_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

14.9.2.2.2.111 PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_EXT_CAP_HDR Register

1 PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_EXT_CAP_HDR Register (Offset = 0h) [reset = A201001Eh]

L1 PM Substates Extended Capability Header Register.

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Table 14-19616. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0000h

Figure 14-6479. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_EXT_CAP_HDR Name Register

31	30	29	28	27	26	25	24
NCO							
R							
A20h							
23	22	21	20	19	18	17	16
NCO				CV			
R				R			
A20h				1h			
15	14	13	12	11	10	9	8
PECID							
R							
1Eh							
7	6	5	4	3	2	1	0
PECID							
R							
1Eh							

Table 14-19618. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_EXT_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NCO	R	A20h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19:16	CV	R	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.
15:0	PECID	R	1Eh	This field is hardwired to the Capability ID assigned by PCI SIG to the L1 PM Substates Extended Capability Structure [001E hex].

14.9.2.2.2.112 PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CAP Register

1 PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CAP Register (Offset = 4h) [reset = 68FF1Fh]

This register advertises the L1 PM Substates Capabilities.

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Table 14-19619. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6480. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CAP Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">R0</td><td>RESERVED</td><td colspan="2">L1PRTPVRONSCALE</td></tr>
<tr><td colspan="5">R</td><td>NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="5">Dh</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">L1PRTCMMDRESTRTIME</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>L1PMSUPP</td><td>L1ASPML11SUPP</td><td>L1ASPML12SUPP</td><td>L1PML11SUPP</td><td>L1PML12SUPP</td></tr>
<tr><td colspan="3">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-19621. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:19	R0	R	Dh	Along with the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register sets the time [in us] that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register. T Power On is the minimum amount of time that each component must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. This is to ensure no device is ever actively driving into an unpowered component.
18	RESERVED	NONE	0h	Reserved

Table 14-19621. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	L1PRTPVRONSCALE	R	0h	Specifies the scale used for the Port T_POWER_ON Value field in the L1 PM Substates Capabilities register. Range of Values 00b = 2us 01b = 10us 10b = 100us 11b = Reserved Default value is 00.
15:8	L1PRTCMMDRESTRTIME	R	FFh	Time [in us] required for this Port to re-establish common mode during exit from PM or ASPM L1.2 substate
7:5	RESERVED	NONE	0h	Reserved
4	L1PMSUPP	R	1h	When Set this bit indicates that this Port supports L1 PM Substates.
3	L1ASPML11SUPP	R	1h	When Set this bit indicates that ASPM L1.1 is supported.
2	L1ASPML12SUPP	R	1h	When Set this bit indicates that ASPM L1.2 is supported.
1	L1PML11SUPP	R	1h	When Set this bit indicates that PCI-PM L1.1 is supported.
0	L1PML12SUPP	R	1h	When Set this bit indicates that PCI-PM L1.2 is supported.

14.9.2.2.2.113 PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_1 Register

1 PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_1 Register (Offset = 8h) [reset = 0h]

L1 PM Substates Control 1 Register

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Table 14-19622. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6481. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_1 Name Register

31	30	29	28	27	26	25	24
L1THRSHLDSC			RESERVED			L1THRSHLDVAL	
R/W			NONE			R/W	
0h			0h			0h	
23	22	21	20	19	18	17	16
L1THRSHLDVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
L1CMMDRESTRTIME							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				L1ASPML11EN	L1ASPML12EN	L1PML11EN	L1PML12EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-19624. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	L1THRSHLDSC	R/W	0h	This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. 000 - Value times 1 ns 001 - Value times 32 ns 010 - Value times 1024 ns 011 - Value times 32,768 ns 100 - Value times 1,048,576 ns 101 - Value times 33,554,422ns 110-111 - Not permitted
28:26	RESERVED	NONE	0h	Reserved
25:16	L1THRSHLDVAL	R/W	0h	Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 [if enabled] or L1.2 [if enabled].
15:8	L1CMMDRESTRTIME	R/W	0h	Sets value of TCOMMONMODE [in us], which must be used by the Downstream Port for timing the re-establishment of common mode. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. This field is reserved since both PCI-PM L1.2 and ASPM L1.2 are Not Supported in this configuration of the Controller.
7:4	RESERVED	NONE	0h	Reserved
3	L1ASPML11EN	R/W	0h	When Set this bit enables ASPM L1.1.
2	L1ASPML12EN	R/W	0h	When Set this bit enables ASPM L1.2.

Table 14-19624. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	L1PML11EN	R/W	0h	When Set this bit enables PCI-PM L1.1.
0	L1PML12EN	R/W	0h	When Set this bit enables PCI-PM L1.2.

14.9.2.2.2.114 PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_2 Register

1 PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_2 Register (Offset = Ch) [reset = 28h]

L1 PM Substates Control 2 Register

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Table 14-19625. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6482. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
L1PWRONVAL					RESERVED	L1PWRONSC	
R/W					NONE	R/W	
5h					0h	0h	

Table 14-19627. PCIE_CORE_RC_I_REGF_L1_PM_CAP_STRUCT_I_L1_PM_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	L1PWRONVAL	R/W	5h	Along with the T_POWER_ON Scale sets the minimum amount of time [in us] that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON Scale field.
2	RESERVED	NONE	0h	Reserved
1:0	L1PWRONSC	R/W	0h	Specifies the scale used for T_POWER_ON Value. Range of Values 00b = 2us 01b = 10us 10b = 100us 11b = Reserved

14.9.2.2.2.115 PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register

1 PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = 0h) [reset = 1001Fh]

Precision Time Measurement Extended Capability Structure is used discovering and controlling the distribution of a PTM hierarchy.

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Table 14-19628. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6483. PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Name Register

31	30	29	28	27	26	25	24
PTMNXCAP							
R							
0h							
23	22	21	20	19	18	17	16
PTMNXCAP				PTMCAPVER			
R				R			
0h				1h			
15	14	13	12	11	10	9	8
PTMCAPID							
R							
1Fh							
7	6	5	4	3	2	1	0
PTMCAPID							
R							
1Fh							

Table 14-19630. PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	PTMNXCAP	R	0h	The offset to the next PCIe Extended Capability structure.
19:16	PTMCAPVER	R	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	PTMCAPID	R	1Fh	Indicates that the associated extended capability structure is for Precision Time Measurement capability. This field returns a Capability ID of 001Fh.

14.9.2.2.2.116 PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CAPABILITIES_REG Register

1 PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CAPABILITIES_REG Register (Offset = 4h) [reset = 406h]

PTM Capabilities Register.

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Table 14-19631. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6484. PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CAPABILITIES_REG Name Register

31	30	29	28	27	26	25	24
R16							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R16							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCCLKGR							
R							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R3					PTMRTCAP	PTMRSCAP	PTMRQCAP
R					R	R	R
0h					1h	1h	0h

Table 14-19633. PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CAPABILITIES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R16	R	0h	Reserved
15:8	LOCCLKGR	R	4h	In RC Mode: The Controller uses the CORE_CLK as the Local Clock for PTM. This field is used to indicate the Time Period of the CORE_CLK. If the PTM Root Select is 1, then CORE_CLK is used to provide PTM Master Time. If the PTM Root Select is 0, then CORE_CLK is used to locally track the PTM Master Time received on the PTM_LOCAL_TIMER_IN[63:0] input. By default, this field is set to 8'd4. This bit can be programmed through the local management APB interface if required.
7:3	R3	R	0h	Reserved
2	PTMRTCAP	R	1h	This bit is used to indicate that the Controller implements PTM Time Source Role and is capable of serving as PTM Root. By default, this bit is set to 1 when the Controller is in RC Mode. This bit can be programmed through the local management APB interface if required. Note: If this bit is programmed to 1, then the PTM Responder Capable bit must also be programmed to 1 by FW.

Table 14-19633. PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CAPABILITIES_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PTMRSCAP	R	1h	This bit is used to indicate support for PTM Responder Role. By default, this bit is set to 1 when the Controller is in RC Mode. This bit can be programmed through the local management APB interface if required. Note: If the PTM Root Capable is programmed to 1, then this bit must also be programmed to 1 by FW.
0	PTMRQCAP	R	0h	This bit is used to indicate support for PTM Requester Role. By default, this bit is set to 0 when the Controller is in RC Mode. This bit can be programmed through the local management APB interface if required.

14.9.2.2.2.117 PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CONTROL_REG Register

1 PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CONTROL_REG Register (Offset = 8h) [reset = 0h]

PTM Control Register.

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Table 14-19634. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6485. PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EFFGRN</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">R2</td><td>RTSEL</td><td>PTMEN</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-19636. PCIE_CORE_RC_I_REGF_PTM_CAP_I_PTM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R16	R	0h	Reserved
15:8	EFFGRN	R	0h	This field is used only in PTM Requester Mode and is not used in RC Mode. This field is set to 00 by default in RC Mode.
7:2	R2	R	0h	Reserved
1	RTSEL	R/W	0h	This field is configured by System SW. When set to 1 and when PTM Enable bit is aslo set to 1, this PTM Source is the PTM Root. Default value of this bit is 0.
0	PTMEN	R/W	0h	When Set, this function is permitted to participate in the PTM mechanism as PTM Requester. By default, this bit is set to 0.

14.9.2.2.2.118 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_0_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_0_REG Register (Offset = 0h) [reset = 20h]

This register contains the configured parameters at the Physical Layer of the link, and status information from the Physical Layer.

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Table 14-19637. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0000h

Figure 14-6486. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_0_REG Name Register

31	30	29	28	27	26	25	24
MLE	R0	LTSSM					
R/W	R	R					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RLID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RFC							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSS	APER	LTD	NS		NLC		LS
R/W	R/W	R	R		R		R
0h	0h	1h	0h		0h		0h

Table 14-19639. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MLE	R/W	0h	When the Controller is operating as a Root Port, setting this to 1 causes the LTSSM to initiate a loopback and become the loopback master. This bit is not used in the EndPoint Mode.
30	R0	R	0h	A 1 in this field indicates that the remote node advertised Linkwidth Upconfigure Capability in the training sequences in the Configuration.Complete state when the link came up. A 0 indicates that the remote node did not set the Link Upconfigure bit.
29:24	LTSSM	R	0h	Current state of the LTSSM. The encoding of the states is given in Appendix C.
23:16	RLID	R	0h	Link ID received from other side during link training.
15:8	RFC	R	0h	FTS count received from the other side during link training for use at the 2.5 GT/s link speed. The Controller transmits this many FTS sequences while exiting the L0S state, when operating at the 2.5 GT/s speed.
7	TSS	R/W	0h	This bit drives the PIPE_TX_SWING output of the Controller.

Table 14-19639. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	APER	R/W	0h	This bit controls the reporting of Errors Detected by the PHY. The Errors Detected by the PHY include:- - Received errors indicated on PIPE RxStatus interface, - 8.0 GT/s Invalid Sync Header received error, If PHY Error Reporting bit is set to 0, the Controller will only report those errors that caused a TLP or DLLP to be dropped because of a Detected PHY Error. If PHY Error Reporting bit is set to 1, the Controller will report all Detected PHY Errors regardless of whether a TLP or DLLP was dropped. The following registers report PHY error in conjunction with this bit: - Correctable Error Status Register, i_corr_err_status, bit-0, Receiver Error Status - Local Error and Status Register, i_local_error_status_register, bit-7, Phy Error In addition to the Errors Detected by the PHY[PCS], the Controller detects the following Physical Layer Protocol Framing Errors: - Framing Errors in the received DLLP and TLP - Ordered Set Block Received Without EDS - Data Block Received After EDS - Illegal Ordered Set Block Received After EDS - Ordered Set Block Received After Skip OS Note: These Errors are always reported independent of the setting of this bit.
5	LTD	R	1h	The state of this bit indicates whether the Controller completed link training as an upstream port[EndPoint][=0] or a downstream port[Root Port][=1]. Default value depends on CORE_TYPE strap pin.
4:3	NS	R	0h	Current operating speed of link [00 = 2.5G, 01 = 5G, 10 = 8G, 11 = 16G].
2:1	NLC	R	0h	N/A
0	LS	R	0h	Current state of link [1 = link training complete, 0 = link training not complete].

14.9.2.2.2.119 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_1_REG Register (Offset = 4h) [reset = 80808000h]

This register contains additional configured parameters at the Physical Layer of the link, and command bits for various Physical Layer functions.

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Table 14-19640. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6487. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_1_REG Name Register

31	30	29	28	27	26	25	24
TFC3							
R/W							
80h							
23	22	21	20	19	18	17	16
TFC2							
R/W							
80h							
15	14	13	12	11	10	9	8
TFC1							
R/W							
80h							
7	6	5	4	3	2	1	0
TLI							
R/W							
0h							

Table 14-19642. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TFC3	R/W	80h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from L0S state.
23:16	TFC2	R/W	80h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from L0S state.
15:8	TFC1	R/W	80h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from L0S state.
7:0	TLI	R/W	0h	Link ID transmitted by the device in training sequences in the Root Port mode.

14.9.2.2.2.120 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DLL_TMR_CONFIG_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DLL_TMR_CONFIG_REG Register (Offset = 8h) [reset = 0h]

This register defines the replay timeout values used by the DL receive and transmit sides of the link. It can be read or written via the local management APB bus.

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Table 14-19643. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6488. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DLL_TMR_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
R25							RSART
R							R/W
0h							0h
23	22	21	20	19	18	17	16
RSART							
R/W							
0h							
15	14	13	12	11	10	9	8
R9							TSRT
R							R/W
0h							0h
7	6	5	4	3	2	1	0
TSRT							
R/W							
0h							

Table 14-19645. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DLL_TMR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	R25	R	0h	Reserved
24:16	RSART	R/W	0h	Additional receive side ACK-NAK timer timeout interval. This 9-bit value is added as a signed 2's complement number to the internal ACK-NAK timer timeout value computed by the Controller based on the PCI Express Specifications. This enables the user to make minor adjustments to the spec-defined replay timer settings.Its value is in multiples of [2 Symbol Times] At Gen1 adjustment range = [+2040 ns to -2048 ns]. At Gen2 adjustment range = [+1020 ns to -1024 ns]. At Gen3 adjustment range = [+510 ns to -512 ns].
15:9	R9	R	0h	Reserved

Table 14-19645. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DLL_TMR_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:0	TSRT	R/W	0h	Additional transmit-side replay timer timeout interval. This 9-bit value is added as a signed 2's complement number to the internal replay timer timeout value computed by the Controller based on the PCI Express Specifications. This enables the user to make minor adjustments to the spec-defined replay timer settings. Its value is in multiples of [2 Symbol Times] At Gen1 adjustment range = [+2040 ns to -2048 ns]. At Gen2 adjustment range = [+1020 ns to -1024 ns]. At Gen3 adjustment range = [+510 ns to -512 ns].

14.9.2.2.2.121 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG Register (Offset = Ch) [reset = 2020040h]

This register contains the initial credit limits advertised by the Controller during th DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. Note: This may result in receiver overflow if received data is back pressured on the Client interface.

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Table 14-19646. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6489. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NPPC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">NPPC</td><td colspan="4">PHC</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">20h</td><td colspan="4">20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">PHC</td><td colspan="4">PPC</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">20h</td><td colspan="4">40h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PPC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">40h</td></tr>
</table>

Table 14-19648. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NPPC	R/W	20h	Non-Posted payload credit limit advertised by the Controller for VC 0 . [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
19:12	PHC	R/W	20h	Posted header credit limit advertised by the Controller for VC 0. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 14-19648. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	PPC	R/W	40h	Posted payload credit limit advertised by the Controller for VC 0. [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

14.9.2.2.2.122 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG Register (Offset = 10h) [reset = 20h]

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. Note: This may result in receiver overflow if received data is back pressured on the Client interface.

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Table 14-19649. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0010h**

Figure 14-6490. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG Name Register

31	30	29	28	27	26	25	24
CHC							
R/W							
0h							
23	22	21	20	19	18	17	16
R2				CPC			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NPHCL							
R/W							
20h							

Table 14-19651. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 0 [in number of packets]. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23:20	R2	R	0h	Reserved
19:8	CPC	R/W	0h	Completion payload credit limit advertised by the Controller for VC 0 . [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 14-19651. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	NPHCL	R/W	20h	Non-Posted header credit limit advertised by the Controller for VC 0 [in number of packets]. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

14.9.2.2.2.123 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG Register (Offset = 14h) [reset = 0h]

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

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Table 14-19652. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6491. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG Name Register

31	30	29	28	27	26	25	24
NPPC							
R							
0h							
23	22	21	20	19	18	17	16
NPPC				PHC			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
PHC				PPC			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
PPC							
R							
0h							

Table 14-19654. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . [in units of 4 Dwords]
19:12	PHC	R	0h	Posted header credit limit received by the Controller for this link . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11:0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . [in units of 4 Dwords]

14.9.2.2.2.124 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG Register (Offset = 18h) [reset = 0h]

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

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Table 14-19655. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6492. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CHC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">R3</td><td colspan="4">CPC</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CPC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NPHC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19657. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CHC	R	0h	Completion header credit limit received by the Controller for VC 0 . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23:20	R3	R	0h	Reserved
19:8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 0 . [in units of 4 Dwords]
7:0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 0 . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

14.9.2.2.2.125 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register (Offset = 1Ch) [reset = 40004h]

This register contains parameters that control how frequently the Controller sends a credit update to the opposite node.

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Table 14-19658. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6493. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Name Register

31	30	29	28	27	26	25	24
MNUI							
R/W							
4h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MNUI							
R/W							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPUI							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPUI							
R/W							
4h							

Table 14-19660. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MNUI	R/W	4h	Minimum credit update interval for non-posted transactions. The Controller follows this minimum interval between issuing posted credit updates on the link. This is to limit the bandwidth use of credit updates. If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update. The value is in units of 16 ns. This field is re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h. The user may override this default value by writing into this register field. The value written will be lost on a change in the negotiated link width/speed.

Table 14-19660. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	MPUI	R/W	4h	Minimum credit update interval for posted transactions. The Controller follows this minimum interval between issuing posted credit updates on the link. This is to limit the bandwidth use of credit updates. If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update. The value is in units of 16 ns. This field is re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h. The user may override this default value by writing into this register field. The value written will be lost on a change in the negotiated link width/ speed.

14.9.2.2.2.126 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register (Offset = 20h) [reset = 3AA0004h]

This register contains parameters that control how frequently the Controller sends a credit update to the opposite node.

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Table 14-19661. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0020h**

Figure 14-6494. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MUI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3AAh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MUI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3AAh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CUI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CUI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-19663. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MUI	R/W	3AAh	Maximum credit update interval for all transactions. If no new credit has become available since the last update, the Controller will repeat the last update after this interval. This is to recover from any losses of credit update packets. The value is in units of 16 ns. This field could be re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h. The user may override this default value by writing into this register field. The value written will be lost on a change in the negotiated link width/speed.

Table 14-19663. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	CUI	R/W	4h	Minimum credit update interval for Completion packets. The Controller follows this minimum interval between issuing completion credit updates on the link. This is to limit the bandwidth use of credit updates. If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update. The value is in units of 16 ns. This parameter is not used when the Completion credit is infinity.

14.9.2.2.2.127 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L0S_TIMEOUT_LIMIT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L0S_TIMEOUT_LIMIT_REG Register (Offset = 24h) [reset = 177h]

This register defines the timeout value for transitioning to the L0S power state. If the transmit side has been idle for this interval, the Controller will transmit the idle sequence on the link and transition the state of the link to L0S .

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Table 14-19664. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0024h**

Figure 14-6495. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L0S_TIMEOUT_LIMIT_REG Name Register

31	30	29	28	27	26	25	24
R4							
R							
0h							
23	22	21	20	19	18	17	16
R4							
R							
0h							
15	14	13	12	11	10	9	8
LT							
R/W							
177h							
7	6	5	4	3	2	1	0
LT							
R/W							
177h							

Table 14-19666. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L0S_TIMEOUT_LIMIT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R4	R	0h	Reserved
15:0	LT	R/W	177h	Contains the timeout value [in units of 16 ns] for transitioning to the L0S power state. Setting this parameter to 0 permanently disables the transition to the L0S power state.

14.9.2.2.2.128 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_COUNT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_COUNT_REG Register (Offset = 28h) [reset = 0h]

This register contains the number of Transaction-Layer packets transmitted by the Controller on the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing all 1's to this register causes it to be reset to 0.

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Table 14-19667. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0028h**

Figure 14-6496. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_COUNT_REG Name Register

31	30	29	28	27	26	25	24
TTC							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
TTC							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
TTC							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
TTC							
R/W1TC							
0h							

Table 14-19669. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TTC	R/W1TC	0h	Count of TLPs transmitted

14.9.2.2.2.129 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register (Offset = 2Ch) [reset = 0h]

This register contains the aggregate number of payload double-words transmitted in Transaction-Layer Packets by the Controller on the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing all 1's to this register causes it to be reset to 0.

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Table 14-19670. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 002Ch**

Figure 14-6497. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Name Register

31	30	29	28	27	26	25	24
TTPBC							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
TTPBC							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
TTPBC							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
TTPBC							
R/W1TC							
0h							

Table 14-19672. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TTPBC	R/W1TC	0h	Count of TLPs payload Dwords transmitted

14.9.2.2.2.130 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_COUNT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_COUNT_REG Register (Offset = 30h) [reset = 0h]

This register contains the number of Transaction-Layer packets received by the Controller from the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing all 1's to this register causes it to be reset to 0.

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Table 14-19673. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0030h**

Figure 14-6498. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_COUNT_REG Name Register

31	30	29	28	27	26	25	24
RTC							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
RTC							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
RTC							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
RTC							
R/W1TC							
0h							

Table 14-19675. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RTC	R/W1TC	0h	Count of TLPs received

14.9.2.2.2.131 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register (Offset = 34h) [reset = 0h]

This register contains the aggregate number of payload double-words received in Transaction-Layer packets by the Controller from the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing all 1's to this register causes it to be reset to 0.

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Table 14-19676. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0034h**

Figure 14-6499. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Name Register

31	30	29	28	27	26	25	24
RTPDC							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
RTPDC							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
RTPDC							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
RTPDC							
R/W1TC							
0h							

Table 14-19678. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RTPDC	R/W1TC	0h	Count of TLP payload Dwords received

14.9.2.2.2.132 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_0_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_0_REG Register (Offset = 38h) [reset = BEBC20h]

This register contains the timeout value used to detect a completion timeout event for a request originated by the Controller from it master interface, when sub-range 1 is programmed in the Device Control 2 Register.

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Table 14-19679. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0038h**

Figure 14-6500. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_0_REG Name Register

31	30	29	28	27	26	25	24
R5							
R							
0h							
23	22	21	20	19	18	17	16
CTL							
R/W							
BEBC20h							
15	14	13	12	11	10	9	8
CTL							
R/W							
BEBC20h							
7	6	5	4	3	2	1	0
CTL							
R/W							
BEBC20h							

Table 14-19681. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	R5	R	0h	Reserved
23:0	CTL	R/W	BEBC20h	Timeout limit for completion timers [in 4 ns cycles]. Default value is 50 ms in 4 ns cycles. Please note that there could be a variation of 0 to +8us on the programmed Completion Timeout.

14.9.2.2.2.133 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_1_REG Register (Offset = 3Ch) [reset = 2FAF080h]

This register contains the timeout value used to detect a completion timeout event for a request originated by the Controller from its master interface, when sub-range 2 is programmed in the Device Control 2 Register.

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Table 14-19682. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 003Ch**

Figure 14-6501. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_1_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">R6</td><td colspan="4">CTL</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2FAF080h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CTL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2FAF080h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CTL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2FAF080h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2FAF080h</td></tr>
</table>

Table 14-19684. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_COMPLN_TMOUT_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	R6	R	0h	Reserved
27:0	CTL	R/W	2FAF080h	Timeout limit for completion timers [in 4 ns cycles]. Default value is 200ms in 4ns cycles. Please note that there could be a variation of 0 to +8us on the programmed Completion Timeout.

14.9.2.2.2.134 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L1_ST_REENTRY_DELAY_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L1_ST_REENTRY_DELAY_REG Register (Offset = 40h) [reset = 0h]

This register specifies the time the Controller will wait before it re-enters the L1 state if its link partner transitions the link to L0 while all the Functions of the Controller are in D3 power state. The Controller will change the power state of the link from L0 to L1 if no activity is detected both on the transmit and receive sides before this interval, while all Functions are in D3 state and the link is in L0. Setting this register to 0 disables re-entry to L1 state if the link partner returns the link to L0 from L1 when all the Functions of the Controller are in D3 state. This register controls only the re-entry to L1. The initial transition to L1 always occurs when all of the Functions of the Controller are set to the D3 state.

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Table 14-19685. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0040h**

Figure 14-6502. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L1_ST_REENTRY_DELAY_REG Name Register

31	30	29	28	27	26	25	24
L1RD							
R/W							
0h							
23	22	21	20	19	18	17	16
L1RD							
R/W							
0h							
15	14	13	12	11	10	9	8
L1RD							
R/W							
0h							
7	6	5	4	3	2	1	0
L1RD							
R/W							
0h							

Table 14-19687. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_L1_ST_REENTRY_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L1RD	R/W	0h	Delay to re-enter L1 after no activity [in units of 16 ns].

14.9.2.2.2.135 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_ID_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_ID_REG Register (Offset = 44h) [reset = 17CD17CDh]

This register contains the Vendor ID and Subsystem Vendor ID that the device advertises during its enumeration of the PCI configuration space.

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Table 14-19688. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0044h**

Figure 14-6503. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_ID_REG Name Register

31	30	29	28	27	26	25	24
SVID							
R/W							
17CDh							
23	22	21	20	19	18	17	16
SVID							
R/W							
17CDh							
15	14	13	12	11	10	9	8
VID							
R/W							
17CDh							
7	6	5	4	3	2	1	0
VID							
R/W							
17CDh							

Table 14-19690. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SVID	R/W	17CDh	Subsystem Vendor ID
15:0	VID	R/W	17CDh	Vendor ID

14.9.2.2.2.136 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register (Offset = 48h) [reset = 2EEh]

This register defines the timeout value for transitioning to the L1 power state under Active State Power management. If the transmit side has been idle for this interval, the Controller will initiate a transition of its link to the L1 power state.

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Table 14-19691. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0048h**

Figure 14-6504. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Name Register

31	30	29	28	27	26	25	24
DISLNRXCHK	R7						
R/W	R						
0h	0h						
23	22	21	20	19	18	17	16
R7				L1T			
R				R/W			
0h				2EEh			
15	14	13	12	11	10	9	8
L1T							
R/W							
2EEh							
7	6	5	4	3	2	1	0
L1T							
R/W							
2EEh							

Table 14-19693. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISLNRXCHK	R/W	0h	This bit is used to configure the ASPM L1 Entry mechanism: 1: Link is checked for IDLE only on the TX to determine ASPM L1 Entry. ASPM L1 entry is initiated if no TLP is transmitted for the L1 timeout period. 0: Link is checked for IDLE both on the TX and RX to determine ASPM L1 Entry. ASPM L1 entry is initiated if no TLP is transmitted/received for the L1 timeout period.
30:20	R7	R	0h	Reserved
19:0	L1T	R/W	2EEh	Contains the timeout value[in units of 16 ns] for transitioning to the L1 power state. Setting it to 0 permanently disables the transition to the L1 power state.

14.9.2.2.2.137 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_TURNOFF_ACK_DELAY_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_TURNOFF_ACK_DELAY_REG Register (Offset = 4Ch) [reset = 64h]

Defines the time interval between the Controller receiving a PME_Turn_Off message from the link and generating an ack for it.

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Table 14-19694. Instance Table

Instance Name	**Physical Address**
PCIE0	**0D00 004Ch**

Figure 14-6505. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_TURNOFF_ACK_DELAY_REG Name Register

31	30	29	28	27	26	25	24
R7							
R							
0h							
23	22	21	20	19	18	17	16
R7							
R							
0h							
15	14	13	12	11	10	9	8
PTOAD							
R/W							
64h							
7	6	5	4	3	2	1	0
PTOAD							
R/W							
64h							

Table 14-19696. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_TURNOFF_ACK_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R7	R	0h	Reserved
15:0	PTOAD	R/W	64h	Time in microseconds between the Controller receiving a PME_TurnOff message TLP and the Controller sending a PME_TO_Ack response to it. This field must be set to a non-zero value in order for the Controller to send a response. Setting this field to 0 suppresses the Controller's response to PME_TurnOff message, so that the client may transmit the PME_TO_Ack message through the master interface.

14.9.2.2.2.138 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINKWIDTH_CONTROL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINKWIDTH_CONTROL_REG Register (Offset = 50h) [reset = 0h]

This register can be used to retrain the link to a different width, without bringing the link down. This register can also be used to retrain the link to a different speed, without bringing the link down.

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Table 14-19697. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0050h**

Figure 14-6506. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINKWIDTH_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>EPLSCRL</td><td colspan="5">R2</td><td colspan="2">EPTLS</td></tr>
<tr><td>R/W</td><td colspan="5">R</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="5">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">R20</td><td>DSAG4SC</td><td>DSAG3SC</td><td>DSAG2SC</td><td>R1</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19699. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINKWIDTH_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EPLSCRL	R/W	0h	Writing a 1 into this field results in the Controller re-training the link to change its speed. When setting this bit to 1, the software must also set the EP Target Link Speed field to indicate the speed that the EP desires to change on the link. The EP Controller will attempt to change the link to this speed. This bit is cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. Software must wait for the bit to be clear before setting it again to change the link speed.
30:26	R2	R	0h	Reserved

Table 14-19699. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINKWIDTH_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:24	EPTLS	R/W	0h	This field contains the Link Speed that the EP intends to change to during the re-training. Client needs to ensure that this field is programmed to a speed which is lesser than or equal to the Target Link Speed field of PF0 Configuration Link Control 2 Register. Client also needs to ensure that this does not exceed PCIE_GENERATION_SEL strap input. Defined encodings of this field are: 00 - GEN1 01 - GEN2 10 - GEN3 11 - Reserved
23:20	R20	R	0h	Reserved
19	DSAG4SC	R/W	0h	This bit is used Only in RP mode. This bit is not used in EP mode of the Controller. During initial link training, if both components advertise Gen4 capability and if Gen3 speed change, equalization was successful, the Controller [RP] autonomously initiates Gen3 to Gen4 speed change, equalization. If Gen4 autonomous speed change/equalization was unsuccessful, then the Link transitions back to Gen3 L0. Software can re-initiate Gen4 speed change. Autonomous Speed Change to Gen4 can be disabled by programming this bit to 1. Note: If Disable Auto Gen3 Speed Change is disabled, then Auto Gen4 Speed Change must also be disabled by setting this bit to 1.
18	DSAG3SC	R/W	0h	This bit is used Only in RP mode. This bit is not used in EP mode of the Controller. During initial link training, if both components advertise Gen3 capability, the Controller [RP] autonomously initiates Gen1 to Gen3 speed change, equalization. If Gen3 autonomous speed change/equalization was unsuccessful, then the Link transitions back to Gen1 L0. Software can re-initiate Gen3 speed change. Autonomous Speed Change to Gen3 can be disabled by programming this bit to 1.
17	DSAG2SC	R/W	0h	This bit is used Only in RP mode. This bit is not used in EP mode of the Controller. During initial link training, if both components advertise Gen2 capability and if Gen2 is the highest common supported speed the Controller [RP] autonomously initiates Gen1 to Gen2 speed change. If Gen2 autonomous speed change was unsuccessful, then the Link transitions back to Gen1 L0. Software can re-initiate Gen2 speed change. Autonomous Speed Change to Gen2 can be disabled by programming this bit to 1.
16:0	R1	R	0h	Reserved

14.9.2.2.2.139 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_2_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_2_REG Register (Offset = 54h) [reset = 1h]

This register controls various LTSSM related capabilities.

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Table 14-19700. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0054h**

Figure 14-6507. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_2_REG Name Register

31	30	29	28	27	26	25	24
R3							
R							
0h							
23	22	21	20	19	18	17	16
R3							
R							
0h							
15	14	13	12	11	10	9	8
R3							
R							
0h							
7	6	5	4	3	2	1	0
R3					DQMDC		LK_TRN
R					R/W		R/W
0h					0h		1h

Table 14-19702. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PL_CONFIG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	R3	R	0h	Reserved
2:1	DQMDC	R/W	0h	As per PCIe specification, All Receivers must meet the the Z-RX-DC specification for 2.5 GT/s within 1ms of entering Detect.Quiet LTSSM substate. The LTSSM must stay in this substate until the ZRX-DC specification for 2.5 GT/s is met. This register field can be used to program the minimum time that LTSSM waits on entering Detect.Quiet state. 00 : 0us minimum wait time in Detect.Quiet state. 01 : 100us minimum wait time in Detect.Quiet state. 10 : 1ms minimum wait time in Detect.Quiet state. 11 : 2ms minimum wait time in Detect.Quiet state.
0	LK_TRN	R/W	1h	This bit is AND'ed with the input LINK_TRAINING_ENABLE strap to enable Link Training.

14.9.2.2.2.140 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_MULTI_VC_CONROL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_MULTI_VC_CONROL_REG Register (Offset = 70h) [reset = 2h]

This register contains control bits to control certain multi VC features

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Table 14-19703. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0070h**

Figure 14-6508. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_MULTI_VC_CONROL_REG Name Register

31	30	29	28	27	26	25	24
R31							
R							
0h							
23	22	21	20	19	18	17	16
R31							
R							
0h							
15	14	13	12	11	10	9	8
R31							
R							
0h							
7	6	5	4	3	2	1	0
R31			RES4	RES2		WAIT_4_ALL_VC_CC_RDY	DMAAM
R			R	R		R/W	R
0h			0h	0h		1h	0h

Table 14-19705. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_MULTI_VC_CONROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	R31	R	0h	Reserved
4	RES4	R	0h	Reserved
3:2	RES2	R	0h	Reserved
1	WAIT_4_ALL_VC_CC_RDY	R/W	1h	When this bit is set, the controller waits for credits to be available to be able to send atleast 1 max payload TLP in all enabled VCs. When this bit is not set, the controller waits for credits to be available to be able to send atleast 1 max payload TLP in any of the enabled VCs [PCI-SIG recommedned].
0	DMAAM	R	0h	Reserved

14.9.2.2.2.141 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SRIS_CONTROL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SRIS_CONTROL_REG Register (Offset = 74h) [reset = 0h]

This register contains control bits to enable the SRIS operation in the PHY Layer

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Table 14-19706. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0074h**

Figure 14-6509. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SRIS_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
R31							
R							
0h							
23	22	21	20	19	18	17	16
R31							
R							
0h							
15	14	13	12	11	10	9	8
R31							
R							
0h							
7	6	5	4	3	2	1	0
R31							SRISE
R							R/W
0h							0h

Table 14-19708. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SRIS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	R31	R	0h	Reserved
0	SRISE	R/W	0h	Setting this bit enables SRIS mode in the PHY layer. This bit should be changed before link training begins by holding the LINK_TRAINING_ENABLE input to 1'b0. When SRIS is disabled using this bit the Lower SKP OS Generation Supported Speeds Vector and Lower SKP OS Reception Supported Speeds Vector in the Link Capabilities Register 2 will be forced to ZERO. The default value of this register can be controlled using the SRIS_ENABLE strap input.

14.9.2.2.2.142 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC1 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC1 Register (Offset = 80h) [reset = 2020040h]

This register contains the initial credit limits advertised by the Controller during th DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. Note: This may result in receiver overflow if received data is back pressured on the Client interface.

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Table 14-19709. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0080h**

Figure 14-6510. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC1 Name Register

31	30	29	28	27	26	25	24
NPPC							
R/W							
20h							
23	22	21	20	19	18	17	16
NPPC				PHC			
R/W				R/W			
20h				20h			
15	14	13	12	11	10	9	8
PHC				PPC			
R/W				R/W			
20h				40h			
7	6	5	4	3	2	1	0
PPC							
R/W							
40h							

Table 14-19711. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NPPC	R/W	20h	Non-Posted payload credit limit advertised by the Controller for VC 1 . [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
19:12	PHC	R/W	20h	Posted header credit limit advertised by the Controller for VC 1. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 14-19711. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	PPC	R/W	40h	Posted payload credit limit advertised by the Controller for VC 1. [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

14.9.2.2.2.143 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC1 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC1 Register (Offset = 84h) [reset = 20h]

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. Note: This may result in receiver overflow if received data is back pressured on the Client interface.

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Table 14-19712. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0084h**

Figure 14-6511. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC1 Name Register

31	30	29	28	27	26	25	24
CHC							
R/W							
0h							
23	22	21	20	19	18	17	16
R2				CPC			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CPC							
R/W							
0h							
7	6	5	4	3	2	1	0
NPHCL							
R/W							
20h							

Table 14-19714. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 1 [in number of packets]. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23:20	R2	R	0h	Reserved
19:8	CPC	R/W	0h	Completion payload credit limit advertised by the Controller for VC 1 . [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 14-19714. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	NPHCL	R/W	20h	Non-Posted header credit limit advertised by the Controller for VC 1 [in number of packets]. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

14.9.2.2.2.144 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC1 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC1 Register (Offset = 88h) [reset = 0h]

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

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Table 14-19715. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0088h**

Figure 14-6512. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC1 Name Register

31	30	29	28	27	26	25	24
NPPC							
R							
0h							
23	22	21	20	19	18	17	16
NPPC				PHC			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
PHC				PPC			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
PPC							
R							
0h							

Table 14-19717. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . [in units of 4 Dwords]
19:12	PHC	R	0h	Posted header credit limit received by the Controller for this link . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11:0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . [in units of 4 Dwords]

14.9.2.2.2.145 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC1 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC1 Register (Offset = 8Ch) [reset = 0h]

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

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Table 14-19718. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 008Ch**

Figure 14-6513. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CHC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">R3</td><td colspan="4">CPC</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CPC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NPHC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19720. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CHC	R	0h	Completion header credit limit received by the Controller for VC 1 . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23:20	R3	R	0h	Reserved
19:8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 1 . [in units of 4 Dwords]
7:0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 1 . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

14.9.2.2.2.146 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC2 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC2 Register (Offset = 90h) [reset = 2020040h]

This register contains the initial credit limits advertised by the Controller during th DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. Note: This may result in receiver overflow if received data is back pressured on the Client interface.

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Table 14-19721. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0090h

Figure 14-6514. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC2 Name Register

31	30	29	28	27	26	25	24
NPPC							
R/W							
20h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NPPC				PHC			
R/W				R/W			
20h				20h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHC				PPC			
R/W				R/W			
20h				40h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPC							
R/W							
40h							

Table 14-19723. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NPPC	R/W	20h	Non-Posted payload credit limit advertised by the Controller for VC 2 . [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
19:12	PHC	R/W	20h	Posted header credit limit advertised by the Controller for VC 2. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 14-19723. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	PPC	R/W	40h	Posted payload credit limit advertised by the Controller for VC 2. [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

14.9.2.2.2.147 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC2 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC2 Register (Offset = 94h) [reset = 20h]

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. Note: This may result in receiver overflow if received data is back pressured on the Client interface.

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Table 14-19724. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0094h**

Figure 14-6515. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC2 Name Register

31	30	29	28	27	26	25	24
CHC							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R2				CPC			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NPHCL							
R/W							
20h							

Table 14-19726. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 2 [in number of packets]. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23:20	R2	R	0h	Reserved
19:8	CPC	R/W	0h	Completion payload credit limit advertised by the Controller for VC 2 . [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 14-19726. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	NPHCL	R/W	20h	Non-Posted header credit limit advertised by the Controller for VC 2 [in number of packets]. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

14.9.2.2.2.148 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC2 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC2 Register (Offset = 98h) [reset = 0h]

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

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Table 14-19727. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0098h**

Figure 14-6516. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC2 Name Register

31	30	29	28	27	26	25	24
NPPC							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NPPC				PHC			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHC				PPC			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPC							
R							
0h							

Table 14-19729. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . [in units of 4 Dwords]
19:12	PHC	R	0h	Posted header credit limit received by the Controller for this link . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11:0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . [in units of 4 Dwords]

14.9.2.2.2.149 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC2 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC2 Register (Offset = 9Ch) [reset = 0h]

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

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Table 14-19730. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 009Ch**

Figure 14-6517. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC2 Name Register

31	30	29	28	27	26	25	24
CHC							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R3				CPC			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPC							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NPHC							
R							
0h							

Table 14-19732. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CHC	R	0h	Completion header credit limit received by the Controller for VC 2 . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23:20	R3	R	0h	Reserved
19:8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 2 . [in units of 4 Dwords]
7:0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 2 . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

14.9.2.2.2.150 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC3 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC3 Register (Offset = A0h) [reset = 2020040h]

This register contains the initial credit limits advertised by the Controller during th DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. Note: This may result in receiver overflow if received data is back pressured on the Client interface.

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Table 14-19733. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00A0h**

Figure 14-6518. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC3 Name Register

31	30	29	28	27	26	25	24
NPPC							
R/W							
20h							
23	22	21	20	19	18	17	16
NPPC				PHC			
R/W				R/W			
20h				20h			
15	14	13	12	11	10	9	8
PHC				PPC			
R/W				R/W			
20h				40h			
7	6	5	4	3	2	1	0
PPC							
R/W							
40h							

Table 14-19735. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NPPC	R/W	20h	Non-Posted payload credit limit advertised by the Controller for VC 3 . [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
19:12	PHC	R/W	20h	Posted header credit limit advertised by the Controller for VC 3. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 14-19735. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_0_REG_VC3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	PPC	R/W	40h	Posted payload credit limit advertised by the Controller for VC 3. [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

14.9.2.2.2.151 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC3 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC3 Register (Offset = A4h) [reset = 20h]

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. Note: This may result in receiver overflow if received data is back pressured on the Client interface.

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Table 14-19736. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00A4h**

Figure 14-6519. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC3 Name Register

31	30	29	28	27	26	25	24
CHC							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R2				CPC			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NPHCL							
R/W							
20h							

Table 14-19738. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 3 [in number of packets]. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23:20	R2	R	0h	Reserved
19:8	CPC	R/W	0h	Completion payload credit limit advertised by the Controller for VC 3 . [in units of 4 Dwords] Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 14-19738. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RCV_CRED_LIM_1_REG_VC3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	NPHCL	R/W	20h	Non-Posted header credit limit advertised by the Controller for VC 3 [in number of packets]. [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

14.9.2.2.2.152 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC3 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC3 Register (Offset = A8h) [reset = 0h]

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

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Table 14-19739. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00A8h**

Figure 14-6520. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC3 Name Register

31	30	29	28	27	26	25	24
NPPC							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NPPC				PHC			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHC				PPC			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPC							
R							
0h							

Table 14-19741. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_0_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . [in units of 4 Dwords]
19:12	PHC	R	0h	Posted header credit limit received by the Controller for this link . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11:0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . [in units of 4 Dwords]

14.9.2.2.2.153 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC3 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC3 Register (Offset = ACh) [reset = 0h]

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

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Table 14-19742. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00ACh**

Figure 14-6521. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC3 Name Register

31	30	29	28	27	26	25	24
CHC							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R3				CPC			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPC							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NPHC							
R							
0h							

Table 14-19744. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_TRANSM_CRED_LIM_1_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CHC	R	0h	Completion header credit limit received by the Controller for VC 3 . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23:20	R3	R	0h	Reserved
19:8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 3 . [in units of 4 Dwords]
7:0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 3 . [in units of 1 Packet Header] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

14.9.2.2.2.154 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_FC_INIT_DELAY_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_FC_INIT_DELAY_REG Register (Offset = F0h) [reset = 32h]

This register defines the delay value in between successive FC_INIT DLLPs for VCx.

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Table 14-19745. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 00F0h**

Figure 14-6522. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_FC_INIT_DELAY_REG Name Register

31	30	29	28	27	26	25	24
R4							
R							
0h							
23	22	21	20	19	18	17	16
R4							
R							
0h							
15	14	13	12	11	10	9	8
FCINITDLY							
R/W							
32h							
7	6	5	4	3	2	1	0
FCINITDLY							
R/W							
32h							

Table 14-19747. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_FC_INIT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R4	R	0h	Reserved
15:0	FCINITDLY	R/W	32h	Delay between successive sets of P, NP, CPL FC_INIT DLLP transmissions for VCx.

14.9.2.2.2.155 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_0_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_0_REG Register (Offset = 100h) [reset = 0h]

N/A

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Table 14-19748. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0100h**

Figure 14-6523. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_0_REG Name Register

31	30	29	28	27	26	25	24
SHDW_HDR_LOG_0							
R/W							
0h							
23	22	21	20	19	18	17	16
SHDW_HDR_LOG_0							
R/W							
0h							
15	14	13	12	11	10	9	8
SHDW_HDR_LOG_0							
R/W							
0h							
7	6	5	4	3	2	1	0
SHDW_HDR_LOG_0							
R/W							
0h							

Table 14-19750. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SHDW_HDR_LOG_0	R/W	0h	The value here will be reflected in the target function's header log register when f/w sets any bit in the the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [31:0] value of the TLP header.

14.9.2.2.2.156 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_1_REG Register (Offset = 104h) [reset = 0h]

N/A

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Table 14-19751. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0104h**

Figure 14-6524. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_1_REG Name Register

31	30	29	28	27	26	25	24
SHDW_HDR_LOG_1							
R/W							
0h							
23	22	21	20	19	18	17	16
SHDW_HDR_LOG_1							
R/W							
0h							
15	14	13	12	11	10	9	8
SHDW_HDR_LOG_1							
R/W							
0h							
7	6	5	4	3	2	1	0
SHDW_HDR_LOG_1							
R/W							
0h							

Table 14-19753. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SHDW_HDR_LOG_1	R/W	0h	The value here will be reflected in the target function's header log register when f/w sets any bit in the the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [63:32] value of the TLP header.

14.9.2.2.2.157 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_2_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_2_REG Register (Offset = 108h) [reset = 0h]

N/A

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Table 14-19754. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0108h**

Figure 14-6525. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_2_REG Name Register

31	30	29	28	27	26	25	24
SHDW_HDR_LOG_2							
R/W							
0h							
23	22	21	20	19	18	17	16
SHDW_HDR_LOG_2							
R/W							
0h							
15	14	13	12	11	10	9	8
SHDW_HDR_LOG_2							
R/W							
0h							
7	6	5	4	3	2	1	0
SHDW_HDR_LOG_2							
R/W							
0h							

Table 14-19756. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SHDW_HDR_LOG_2	R/W	0h	The value here will be reflected in the target function's header log register when f/w sets any bit in the the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [95:64] value of the TLP header.

14.9.2.2.2.158 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_3_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_3_REG Register (Offset = 10Ch) [reset = 0h]

N/A

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Table 14-19757. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 010Ch**

Figure 14-6526. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_3_REG Name Register

31	30	29	28	27	26	25	24
SHDW_HDR_LOG_3							
R/W							
0h							
23	22	21	20	19	18	17	16
SHDW_HDR_LOG_3							
R/W							
0h							
15	14	13	12	11	10	9	8
SHDW_HDR_LOG_3							
R/W							
0h							
7	6	5	4	3	2	1	0
SHDW_HDR_LOG_3							
R/W							
0h							

Table 14-19759. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_HDR_LOG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SHDW_HDR_LOG_3	R/W	0h	The value here will be reflected in the target function's header log register when f/w sets any bit in the the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [127:96] value of the TLP header.

14.9.2.2.2.159 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_FUNC_NUM_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_FUNC_NUM_REG Register (Offset = 110h) [reset = 0h]

N/A

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Table 14-19760. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0110h**

Figure 14-6527. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_FUNC_NUM_REG Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
SHDW_FUNC_NUM							
R/W							
0h							

Table 14-19762. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_FUNC_NUM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	R0	R	0h	Reserved
7:0	SHDW_FUNC_NUM	R/W	0h	The value here will be the target function number when f/w sets any bit in the shadow error register.

14.9.2.2.2.160 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_UR_ERR_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_UR_ERR_REG Register (Offset = 114h) [reset = 0h]

Shadow register to create UR error via local f/w. Please make sure this register is written to last, after writing to all the header log and function number registers. A write to this register with any bits set, will internally create a single cycle pulse with the corresponding error type and the header log will reflect the value written in the shadow header log registers.

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Table 14-19763. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0114h**

Figure 14-6528. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_UR_ERR_REG Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
R0						NP_UR_ERR	P_UR_ERR
R						W	W
0h						0h	0h

Table 14-19765. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_SHDW_UR_ERR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	R0	R	0h	Reserved
1	NP_UR_ERR	W	0h	If this bit is set, the corresponding non-posted UR error bits will be set in the AER and device status registers of the target function.
0	P_UR_ERR	W	0h	If this bit is set, the corresponding posted UR error bits will be set in the AER and device status registers of the target function.

14.9.2.2.2.161 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PM_CLK_FREQUENCY_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PM_CLK_FREQUENCY_REG Register (Offset = 140h) [reset = 19h]

This register should be programmed with the frequency of the PM_CLK input to the Controller. The Controller supports the frequency range of 2MHz to 60MHz for PM_CLK. The reset value reflects the PM_CLK frequency chosen during Controller configuration. NOTE: PM_CLK will be timed at 60Mhz and the Controller SDC file will be generated accordingly. If timing is to be closed at a different frequency, then the user needs to update the SDC accordingly.

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Table 14-19766. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0140h**

Figure 14-6529. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PM_CLK_FREQUENCY_REG Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
PMCLKFRQ							
R/W							
19h							

Table 14-19768. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PM_CLK_FREQUENCY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	R0	R	0h	Reserved

Table 14-19768. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PM_CLK_FREQUENCY_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PMCLKFRQ	R/W	19h	This field specifies the PM_CLK Frequency selected. The encoding is described below: 000000: Reserved 000001: Reserved 000010: PM_CLK is 2 MHz 000011: PM_CLK is 3 MHz 000100: PM_CLK is 4 MHz 000101: PM_CLK is 5 MHz .. 111010: PM_CLK is 58 MHz 111011: PM_CLK is 59 MHz 111100: PM_CLK is 60 MHz 111101 : Reserved 111110 : Reserved 111111 : Reserved .

14.9.2.2.2.162 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN1_REG Register (Offset = 144h) [reset = 0h]

This register indicates the total number of DLLPs received by the Controller in GEN1. This counter rolls over back to 0 after 4G DLLPs are received. This register can be used for Debug purposes.

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Table 14-19769. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0144h**

Figure 14-6530. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN1_REG Name Register

31	30	29	28	27	26	25	24
DLLPCNT1							
R							
0h							
23	22	21	20	19	18	17	16
DLLPCNT1							
R							
0h							
15	14	13	12	11	10	9	8
DLLPCNT1							
R							
0h							
7	6	5	4	3	2	1	0
DLLPCNT1							
R							
0h							

Table 14-19771. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DLLPCNT1	R	0h	Reflects the total number of DLLPs received by the Controller at GEN1 speed.

14.9.2.2.2.163 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN2_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN2_REG Register (Offset = 148h) [reset = 0h]

This register indicates the total number of DLLPs received by the Controller in GEN2. This counter rolls over back to 0 after 4G DLLPs are received. This register can be used for Debug purposes.

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Table 14-19772. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0148h**

Figure 14-6531. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN2_REG Name Register

31	30	29	28	27	26	25	24
DLLPCNT2							
R							
0h							
23	22	21	20	19	18	17	16
DLLPCNT2							
R							
0h							
15	14	13	12	11	10	9	8
DLLPCNT2							
R							
0h							
7	6	5	4	3	2	1	0
DLLPCNT2							
R							
0h							

Table 14-19774. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DLLPCNT2	R	0h	Reflects the total number of DLLPs received by the Controller at GEN2 speed.

14.9.2.2.2.164 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN3_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN3_REG Register (Offset = 14Ch) [reset = 0h]

This register indicates the total number of DLLPs received by the Controller in GEN3. This counter rolls over back to 0 after 4G DLLPs are received. This register can be used for Debug purposes.

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Table 14-19775. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 014Ch**

Figure 14-6532. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN3_REG Name Register

31	30	29	28	27	26	25	24
DLLPCNT3							
R							
0h							
23	22	21	20	19	18	17	16
DLLPCNT3							
R							
0h							
15	14	13	12	11	10	9	8
DLLPCNT3							
R							
0h							
7	6	5	4	3	2	1	0
DLLPCNT3							
R							
0h							

Table 14-19777. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_DLLP_COUNT_GEN3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DLLPCNT3	R	0h	Reflects the total number of DLLPs received by the Controller at GEN3 speed.

14.9.2.2.2.165 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register (Offset = 158h) [reset = 0h]

The 8-bit Tag field of the Outbound Vendor Defined Messages, transmitted by the Controller, can be programmed in this register.

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Table 14-19778. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0158h**

Figure 14-6533. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_DEFINED_MESSAGE_TAG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
VDMTAG							
R/W							
0h							

Table 14-19780. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	VDMTAG	R/W	0h	The Controller will use the tag programed in this register for all Outbound Vendor Defined Messages.

14.9.2.2.2.166 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_NEGOTIATED_LANE_MAP_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_NEGOTIATED_LANE_MAP_REG Register (Offset = 200h) [reset = 1h]

This register contains a map of the active lanes used by the Controller to form the link during link training. It also contains a bit to indicate whether the Controller reversed the lane number on its lanes during link training.

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Table 14-19781. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0200h**

Figure 14-6534. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_NEGOTIATED_LANE_MAP_REG Name Register

31	30	29	28	27	26	25	24
R71							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R71							LRS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R70							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R70							NLM
R							R
0h							1h

Table 14-19783. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_NEGOTIATED_LANE_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	R71	R	0h	Reserved
16	LRS	R	0h	This bit set by the Controller at the end of link training if the LTSSM had to reverse the lane numbers to form the link.
15:1	R70	R	0h	Reserved
0	NLM	R	1h	Bit i of this field is set to 1 at the end of link training if Lane i is part of the PCIe link. The value of this field is valid only when the link is in L0 or L0s states.

14.9.2.2.2.167 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_FTS_COUNT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_FTS_COUNT_REG Register (Offset = 204h) [reset = 0h]

This register contains the FTS count values received from the link partner during link training for use at the 5 GT/sand 8 GT/s speeds. These values determine the number of Fast Training Sequences transmitted by the Controller when it exits the L0s link power state.

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Table 14-19784. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0204h**

Figure 14-6535. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_FTS_COUNT_REG Name Register

31	30	29	28	27	26	25	24
R24							
R							
0h							
23	22	21	20	19	18	17	16
R16							
R							
0h							
15	14	13	12	11	10	9	8
RFC8S							
R							
0h							
7	6	5	4	3	2	1	0
RFC5S							
R							
0h							

Table 14-19786. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RECEIVE_FTS_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	R24	R	0h	Reserved
23:16	R16	R	0h	Reserved
15:8	RFC8S	R	0h	FTS count received from the other side during link training for use at the 8 GT/s link speed. The Controller transmits this many FTS sequences while exiting the L0S state, when operating at the 8 GT/s speed.
7:0	RFC5S	R	0h	FTS count received from the other side during link training for use at the 5 GT/s link speed. The Controller transmits this many FTS sequences while exiting the L0S state, when operating at the 5 GT/s speed.

14.9.2.2.2.168 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_REG Register (Offset = 208h) [reset = 80000000h]

N/A

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Table 14-19787. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0208h

Figure 14-6536. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
EFSRTCA	DOC	DFCUT	DEI	DGLUS	IEDPPE	ESPC	EFLT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
DLUC	DLRFE	DSHEC	DCIVMC	DIOAEFC	DOASFC	HPRSUPP	AWRPRI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
FDS	DSSPLM	R1313	R1212	R1111	DRXNPSP	MSIVCMS	DIDBOC
R/W	R/W	R	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
R77	R6		MS				
R/W	R		R/W				
0h	0h		0h				

Table 14-19789. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EFSRTCA	R/W	1h	Setting this bit to 0 causes all the enabled Functions to report an error when a Type-1 configuration access is received by the Controller, targeted at any Function. Setting it to 1 limits the error reporting to the type-0 Function whose number matches with the Function number specified in the request. If the Function number in the request refers to an unimplemented or disabled Function, all enabled Functions report the error regardless of the setting of this bit.
30	DOC	R/W	0h	Setting this bit to 1 disables the ordering check in the Controller between Completions and Posted requests received from the link.

Table 14-19789. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	DFCUT	R/W	0h	When this bit is 0, the Controller will time out and re-train the link when no Flow Control Update DLLPs are received from the link within an interval of 128 us. Setting this bit to 1 disables this timeout. When the advertised receive credit of the link partner is infinity for the header and payload of all credit types, this timeout is always suppressed. The setting of this bit has no effect in this case. This bit should not be set during normal operation, but is useful for testing.
28	DEI	R/W	0h	Setting this bit to 1 disables the inferring of electrical idle in the L0 state. Electrical idle is inferred when no flow control updates and no SKP sequences are received within an interval of 128 us. This bit should not be set during normal operation, but is useful for testing.
27	DGLUS	R/W	0h	Setting this bit to 1 disables the update of the LFSRs in the Gen3 descramblers of the Controller, from the values received in SKP sequences. This bit should not be set during normal operation, but is useful for testing.
26	IEDPPE	R/W	0h	When set to 1, this bit inverts the parity bits generated by the Controller for end-to-end data protection. This will result in the inversion of parity bits for data payloads delivered through the HAL Target Interface request descriptor. This bit is to be used for diagnostics only, and should not be set during normal operation.
25	ESPC	R/W	0h	When this bit is set to 1, the Controller will capture the Slot Power Limit Value and Slot Power Limit Scale parameters from a Set_Slot_Power_Limit message received in the Device Capabilities Register. When this bit is 0, the capture is disabled. This bit is valid only when the Controller is configured as an EndPoint. It has no effect when the Controller is a Root Complex.
24	EFLT	R/W	0h	This bit is provided to shorten the link training time to facilitate fast simulation of the design, especially at the gate level. Enabling this bit has the following effects: 1. The 1 ms, 2 ms, 12 ms, 24 ms, 32 ms and 48 ms timeout intervals in the LTSSM are shortened by a factor of 500. 2. In the Polling.Active state of the LTSSM, only 16 training sequences are required to be transmitted [Instead of 1024] to make the transition to the Configuration state. This bit should not be set during normal operation of the Controller.

Table 14-19789. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	DLUC	R/W	0h	The user may set this bit to turn off the link upconfigure capability of the Controller. Setting this bit prevents the Controller from advertising the link upconfigure capability in training sequences transmitted in the Configuration.Complete state. In addition, setting this bit causes the Controller to put the unused lanes into Turn Off mode. When disable_link_upconfigure_capability==1: Controller drives PIPE_TX_ELEC_IDLE==1 AND PIPE_TX_COMPLIANCE==1 for the Unused upper lanes. The Unused upper lanes are put into Turn Off mode by the PHY as per PIPE specification. When disable_link_upconfigure_capability==0: Controller drives PIPE_TX_ELEC_IDLE==1 AND PIPE_TX_COMPLIANCE==0 for the Unused upper lanes. The Unused upper lanes are put into Electrical Idle by the PHY.
22	DLRFE	R/W	0h	When this bit is 1, the Controller will not transition its LTSSM into the Recovery state when it detects a Framing Error at 8 GT/s speed [as defined in Section 4.2.2.3.3 of the PCIe Base Specification 3.0. This bit must normally be set to 0 so that a Framing Error will cause the LTSSM to enter Recovery. The setting of this bit has no effect on the operation of the Controller at 2.5 and 5 GT/s speeds.
21	DSHEC	R/W	0h	When this bit is 0, the Controller will signal a framing error if it detects a sync header error in the received blocks at 8 GT/s speed [A 00 or 11 binary setting of the sync header on the received blocks in any lane constitutes a framing error]. Setting this bit to 1 suppresses this error check. This bit should normally be set to 0, as the sync header check is mandatory in the PCIe 3.0 Specifications.
20	DCIVMC	R/W	0h	When this bit is 1, the Controller will not check for invalid message codes. This bit should normally set to 0, as the invalid message code checking is mandatory in the PCIe 3.0 specifications.
19	DIOAEFC	R/W	0h	When this bit is 1, the Controller will not check for illegal OS after EDS as part of Gen3 Framing Error Checks. This bit should normally set to 0, as this is a mandatory Gen3 Framing Error check in the PCIe 3.0 specifications.
18	DOASFC	R/W	0h	When this bit is 1, the Controller will not check for OS after SKIP OS as part of Gen3 Framing Error Checks. This bit should normally set to 0, as this is a mandatory Gen3 Framing Error check in the PCIe 3.0 specifications.
17	HPRSUPP	R/W	0h	When this bit is 1, data path parity check is disabled on the TX side of the Controller.
16	AWRPRI	R/W	0h	When this bit is 1, the AXI bridge places a write request on the HAL Master interface in preference over a read request if both AXI write and AXI read requests are available to be asserted on the same clock cycle.
15	FDS	R/W	0h	Disable Scrambling/Descrambling in Gen1/Gen2.
14	DSSPLM	R/W	0h	Disable sending Set Slot Power Limit Message if the Slot Capabilitied register is configured
13	R1313	R	0h	N/A
12	R1212	R	0h	N/A

Table 14-19789. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	R1111	R/W	0h	When this bit is 1, Disable Client TX MUX Completion and PNP request arbitartion,roundrobin priority logic added to prevent PNP requests from starving when completions are present
10	DRXNPSP	R/W	0h	As per PCIe specification, Non Posted packets should not pass ahead of a Posted packet. Posted and Non Posted packets are stored in a common Receive PNP FIFO. Controller ensures that the P and NP are delivered to the HAL/AXI target interface without violating the Ordering rules. When a mix of P and NP requests are received over the link, the NP packets can be starved if multiple Posted packets are stored in the PNP RX FIFO. Controller implements a mechanism to prevent NP Starvation Prevention which can be programmed through this bit: 0: Send P and NP in the received order, instead of giving priority only for P and starve NP when continous P, NP packets are received. 1: Priority only for P. Starve NP when continous P, NP packets are received. NP packets sent to HAL/AXI target interface only when all P packets in the PNP FIFO are delivered.
9	MSIVCMS	R/W	0h	Sets the mode of generating MSI_VECTOR_COUNT output for all functions. 0 - MSI_VECTOR_COUNT always outputs the configured value of MSI Multiple Message Enable[2:0] register. 1 - MSI_VECTOR_COUNT outputs the lesser of the MSI Multiple Message Enable[2:0] and MSI Multiple Message Capable[2:0] This mode can be used to handle any programming error form the Host software.
8	DIDBOC	R/W	0h	Setting this bit to 1 disables the ID Based Ordering check in the Controller between Completions and Posted requests received from the link.
7	R77	R/W	0h	This bit should be set to 0 for backward compatibility.
6:5	R6	R	0h	N/A
4:0	MS	R/W	0h	Bits 4:3 select the module and bits 2:0 select the group of signals within the module that are driven on the debug bus. The assignments of signals on the debug outputs of the Controller are given in Appendix B.

14.9.2.2.2.169 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_REGISTER Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_REGISTER Register (Offset = 20Ch) [reset = 0h]

This register contains the status of the various events, errors and abnormal conditions in the Controller. Any of the status bits can be reset by writing a 1 into the bit position. This register does not capture any errors signaled by remote devices using PCIe error messages when the Controller is operating in the RC mode. Unless masked by the setting of the Local Interrupt Mask Register, the occurrence of any of these conditions causes the Controller to activate the LOCAL_INTERRUPT output.

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Table 14-19790. Instance Table

Instance Name	Physical Address
PCIE0	0D00 020Ch

Figure 14-6537. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_REGISTER Name Register

31	30	29	28	27	26	25	24
REORDER_ER_UN	AXISLAVE_WFIFO_ER_UN	AXIMASTER_RFIFO_ER_UN	AXIMASTER_DIB_ER_UN	R27		MSIXMSKST	R24
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R		R/W1TC	R
0h	0h	0h	0h	0h		0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R24	R23_1	HAWCD	R22	MMVC	UTC	EEPE	R13
R	R	R/W1TC	R	R/W1TC	R/W1TC	R/W1TC	R
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R13			R12	CT	FCE	UCR	MTR
R			R	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PE	RTR	RT	CRFO	PRFO	RRPE	CRFPE	PRFPE
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19792. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REORDER_ER_UN	R/W1TC	0h	This indicates an uncorrectbale axi slave reorder ram parity/ecc error
30	AXISLAVE_WFIFO_ER_UN	R/W1TC	0h	This indicates an uncorrectbale axi slave write fifo ram parity/ecc error
29	AXIMASTER_RFIFO_ER_UN	R/W1TC	0h	This indicates an uncorrectbale axi master write fifo ram parity/ecc error
28	AXIMASTER_DIB_ER_UN	R/W1TC	0h	This indicates an uncorrectbale axi slave write fifo ram parity/ecc error
27:26	R27	R	0h	Reserved
25	MSIXMSKST	R/W1TC	0h	This status bit indicates that the MSIX Function Mask bit of any function, PF or VF, was programmed or configured by Local Firmware Or Host SW.
24:23	R24	R	0h	Reserved
22	R23_1	R	0h	Reserved

Table 14-19792. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	HAWCD	R/W1TC	0h	This interrupt status bit indicates that the Host toggled the Hardware Autonomous Width Change bit in the Link Control Register through a Config Write. Upon this interrupt, the Client firmware must read the Link Control Register to check the value set by Host in the Hardware Autonomous Width Change bit. The Host Software may disable autonomous width change by setting Hardware Autonomous Width Disable bit in the Link Control register. If disabled by the Host and if the Endpoint firmware had initiated an autonomous width downsizing prior to this interrupt, then the local Client firmware is responsible to upconfigure the Link to go to its full functional width by initiating the link_upconfigure_retrain_link within 1 ms of this interrupt.
20	R22	R	0h	Reserved
19	MMVC	R/W1TC	0h	This status bit is set whenever the MSI mask register value in the MSI capability register changes value in ANY of the functions in the controller
18	UTC	R/W1TC	0h	Unmapped TC error.
17	EEPE	R/W1TC	0h	The Controller detected an End to End Parity Error
16:13	R13	R	0h	Reserved
12	R12	R	0h	Reserved
11	CT	R/W1TC	0h	A request timed out waiting for completion.
10	FCE	R/W1TC	0h	An error was observed in the flow control advertisements from the other side.
9	UCR	R/W1TC	0h	Unexpected Completion received from the link.
8	MTR	R/W1TC	0h	Malformed TLP received from the link.
7	PE	R/W1TC	0h	Phy error detected on receive side. This bit is set when an error is detected in the receive side of the Physical Layer of the Controller [e.g. a bit error or coding violation]. This bit is set upon any of the following errors: [1] PHY reported 8B10B error, Disparity Error, Elastic Buffer Overflow Error, Underflow Error [2] GEN3 TLP, DLLP Framing Errors [3] OS Block Received Without EDS [4] Data Block Received After EDS [5] Illegal OS Block After EDS [6] OS Block Received After SKIP OS [7] OS Block Received After SDS [8] Sync Header Error [9] Loss of Gen3 Block Alignment This error is not Function-specific..
6	RTR	R/W1TC	0h	Replay timer rolled over after 4 transmissions of the same TLP.
5	RT	R/W1TC	0h	Replay timer timed out
4	CRFO	R/W1TC	0h	Overflow occurred in the Completion Receive FIFO.
3	PRFO	R/W1TC	0h	Overflow occurred in the PNP Receive FIFO.
2	RRPE	R/W1TC	0h	Parity error detected while reading from Replay Buffer RAM.
1	CRFPE	R/W1TC	0h	Parity error detected while reading from the Completion Receive FIFO RAM.
0	PRFPE	R/W1TC	0h	Parity error detected while reading from the PNP Receive FIFO RAM.

14.9.2.2.2.170 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_REG Register (Offset = 210h) [reset = 22E0FFFh]

This register contains a mask bit for each interrupting condition. Setting the bit to 1 prevents the corresponding condition in the Local Error Status Register from activating the LOCAL_INTERRUPT output.

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Table 14-19793. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0210h**

Figure 14-6538. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_REG Name Register

31	30	29	28	27	26	25	24
REORDER_ER_UN	AXISLAVE_WFIFO_ER_UN	AXIMASTER_RFIFO_ER_UN	AXIMASTER_DIB_ER_UN	R27		MSIXMSK	R24
R/W	R/W	R/W	R/W	R		R/W	R
0h	0h	0h	0h	0h		1h	0h
23	22	21	20	19	18	17	16
R24	R23_1	HAWCD	R45	MMVC	UTC	EEPE	R13
R	R	R/W	R	R/W	R/W	R/W	R
0h	0h	1h	0h	1h	1h	1h	0h
15	14	13	12	11	10	9	8
R13			R12	CT	FCE	UCR	MTR
R			R	R/W	R/W	R/W	R/W
0h			0h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
PE	RTR	RT	CRFO	PRFO	RRPE	CRFPE	PRFPE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h

Table 14-19795. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REORDER_ER_UN	R/W	0h	mask for uncorrectbale axi slave reorder ram parity/ecc error
30	AXISLAVE_WFIFO_ER_UN	R/W	0h	mask for uncorrectbale axi slave write fifo ram parity/ecc error
29	AXIMASTER_RFIFO_ER_UN	R/W	0h	mask for uncorrectbale axi master write fifo ram parity/ecc error
28	AXIMASTER_DIB_ER_UN	R/W	0h	mask for uncorrectbale axi slave write fifo ram parity/ecc error
27:26	R27	R	0h	Reserved
25	MSIXMSK	R/W	1h	This bit is used to mask interrupt that indicates that the MSIX Function Mask bit of any function, PF or VF, was programmed or configured by Local Firmware Or Host SW.
24:23	R24	R	0h	Reserved
22	R23_1	R	0h	Reserved
21	HAWCD	R/W	1h	This bit is used to mask interrupt that indicates that the Host toggled the Hardware Autonomous Width Change in the Endpoint Link Control Register through a Config Write.

Table 14-19795. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	R45	R	0h	Reserved
19	MMVC	R/W	1h	MSI mask register value in the MSI capability register changes value in ANY of the functions in the controller
18	UTC	R/W	1h	Unmapped TC error
17	EEPE	R/W	1h	The Controller detected an End to End Parity Error
16:13	R13	R	0h	Reserved
12	R12	R	0h	Reserved
11	CT	R/W	1h	A request timed out waiting for completion.
10	FCE	R/W	1h	An error was observed in the flow control advertisements from the other side.
9	UCR	R/W	1h	Unexpected Completion received from the link.
8	MTR	R/W	1h	Malformed TLP received from the link.
7	PE	R/W	1h	Phy error detected on receive side.
6	RTR	R/W	1h	Replay timer rolled over after 4 transmissions of the same TLP.
5	RT	R/W	1h	Replay timer timed out
4	CRFO	R/W	1h	Overflow occurred in the Completion Receive FIFO.
3	PRFO	R/W	1h	Overflow occurred in the PNP Receive FIFO.
2	RRPE	R/W	1h	Parity error detected while reading from Replay Buffer RAM.
1	CRFPE	R/W	1h	Parity error detected while reading from the Completion Receive FIFO RAM.
0	PRFPE	R/W	1h	Parity error detected while reading from the PNP Receive FIFO RAM.

14.9.2.2.2.171 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LCRC_ERR_COUNT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LCRC_ERR_COUNT_REG Register (Offset = 214h) [reset = 0h]

This register contains the count of the number of TLPs received by the Controller with LCRC errors in them. This is a 16-bit saturating counter that can be reset to 0 by writing all 1's into it.

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Table 14-19796. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0214h**

Figure 14-6539. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LCRC_ERR_COUNT_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R11</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R11</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LEC</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LEC</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19798. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LCRC_ERR_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R11	R	0h	Reserved
15:0	LEC	R/W1TC	0h	Number of TLPs received with LCRC errors.

14.9.2.2.2.172 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG Register (Offset = 218h) [reset = 0h]

This register contains the count of the number of ECC errors detected and corrected during reads from the PCIe core external RAMs.

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Table 14-19799. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0218h**

Figure 14-6540. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG Name Register

31	30	29	28	27	26	25	24
R31_2							
R							
0h							
23	22	21	20	19	18	17	16
RRCER							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
SFRCER							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
PFRCER							
R/W1TC							
0h							

Table 14-19801. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	R31_2	R	0h	Reserved
23:16	RRCER	R/W1TC	0h	Number of correctable errors detected while reading from the Replay Buffer RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
15:8	SFRCER	R/W1TC	0h	Number of correctable errors detected while reading from the SC FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
7:0	PFRCER	R/W1TC	0h	Number of correctable errors detected while reading from the PNP FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.

14.9.2.2.2.173 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_SNOOP_LAT_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_SNOOP_LAT_REG Register (Offset = 21Ch) [reset = 0h]

This register contains the Snoop and No-Snoop Latency parameters used by the Controller when sending Latency Tolerance Reporting (LTR) Message. When the Controller is configured in the EndPoint mode, client software can program these fields to the desired latency settings and then set the Send LTR Message bit in the LTR Message Generation Control Register to send an LTR message to the Root Complex. The fields in this register should not be changed when the Send LTR Message bit in the LTR Message Generation Control Register is 1, which indicates that an LTR message is pending to be transmitted.

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Table 14-19802. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 021Ch**

Figure 14-6541. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_SNOOP_LAT_REG Name Register

31	30	29	28	27	26	25	24
SL	R13		SLS			SLV	
R/W	R		R/W			R/W	
0h	0h		0h			0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SLV							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NSLR	R12		NSLS			NSLV	
R/W	R		R/W			R/W	
0h	0h		0h			0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NSLV							
R/W							
0h							

Table 14-19804. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_SNOOP_LAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SL	R/W	0h	The client software must set this bit to 1 to set the Snoop Latency Requirement bit in the LTR message to be sent.
30:29	R13	R	0h	Reserved
28:26	SLS	R/W	0h	The client software must program this field with the value to be sent in the Snoop Latency Scale field of the LTR message.
25:16	SLV	R/W	0h	The client software must program this field with the value to be sent in the Snoop Latency Value field of the LTR message.
15	NSLR	R/W	0h	The client software must set this bit to 1 to set the No-Snoop Latency Requirement bit in the LTR message to be sent.
14:13	R12	R	0h	N/A

Table 14-19804. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_SNOOP_LAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:10	NSLS	R/W	0h	The client software must program this field with the value to be sent in the No-Snoop Latency Scale field of the LTR message.
9:0	NSLV	R/W	0h	The client software must program this field with the value to be sent in the No-Snoop Latency Value field of the LTR message.

14.9.2.2.2.174 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_MSG_GEN_CTL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_MSG_GEN_CTL_REG Register (Offset = 220h) [reset = 18FAh]

This register contains fields for the generation of Latency Tolerance Reporting (LTR) Messages. This register is to be used only when the Controller is configured in the EndPoint mode.

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Table 14-19805. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0220h

Figure 14-6542. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_MSG_GEN_CTL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			TMFPSC	TMLMET	SLM	MLI	
NONE			R/W	R/W	R	R/W	
0h			1h	1h	0h	FAh	
7	6	5	4	3	2	1	0
MLI							
R/W							
FAh							

Table 14-19807. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_MSG_GEN_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	TMFPSC	R/W	1h	When this bit is set to 1, the Controller will automatically transmit an LTR message when all the Functions in the Controller have transitioned to a non-D0 power state, provided that the following conditions are both true: 1. The Controller sent at least one LTR message since the Data Link layer last transitioned from down to up state. 2. The most recent LTR message transmitted by the Controller had as least one of the Requirement bits set. The Controller will set the Requirement bits in this LTR message to 0. When this bit 12 is 0, the Controller will not, by itself, send any LTR messages in response to Function Power State changes. Client logic may monitor the FUNCTION_POWER_STATE outputs of the Controller and transmit LTR messages through the master interface, in response to changes in their states.

Table 14-19807. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LTR_MSG_GEN_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TMLMET	R/W	1h	When this bit is set to 1, the Controller will automatically transmit an LTR message whenever the LTR Mechanism Enable bit in the Device Control 2 Register changes from 0 to 1, with the parameters specified in the LTR Snoop/No-Snoop Latency Register. When this bit is 1, the Controller will also transmit an LTR message whenever the LTR Mechanism Enable bit is cleared, if the following conditions are both true: 1. The Controller sent at least one LTR message since the LTR Mechanism Enable bit was last set. 2. The most recent LTR message transmitted by the Controller had as least one of the Requirement bits set. The Controller will set the Requirement bits in this LTR message to 0. When this bit 11 is 0, the Controller will not, by itself, send any LTR messages in response to state changes of the LTR Mechanism Enable bit. Client logic may monitor the state of the LTR_MECHANISM_ ENABLE output of the Controller and transmit LTR messages through the master interface, in response to its state changes.
10	SLM	R	0h	Setting this bit causes the Controller to transmit an LTR message with the parameters specified in the LTR Snoop/No-Snoop Latency Register [Section 8.4.2.9]. This bit is cleared by the Controller on transmitting the LTR message, and stays set until then. Client software must read this register and verify that this bit is 0 before setting it again to send a new message. This field becomes writable when LTR mechanism is enabled in device control-2 register.
9:0	MLI	R/W	FAh	This field specifies the minimum spacing between LTR messages transmitted by the Controller in units of microseconds. The PCI Express Specifications recommend sending no more than two LTR messages within a 500 microsecond interval. The Controller will wait for the minimum delay specified by this field after sending an LTR message, before transmitting a new LTR message. NOTE: The LINK can be in low power states[L0s and L1] when send LTR Message is trigered. So, the user has to consider the exit latencies while programming this field. It is recommended to program this field with about 2 us higher than the required interval to account for the L0s/L1 exit latencies.

14.9.2.2.2.175 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_SERVICE_TIMEOUT_DELAY_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_SERVICE_TIMEOUT_DELAY_REG Register (Offset = 224h) [reset = 186A0h]

This register stores the timeout delay parameter for the service timeout mechanism associated with the generation of PM_PME messages. In the EndPoint mode, the Controller will retransmit a PM_PME message after the expiration of this delay, if the Root Complex did not clear the PME Status bit in the Power Management Control and Status Register. This register is not used when the Controller is configured as Root Complex.

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Table 14-19808. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0224h**

Figure 14-6543. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_SERVICE_TIMEOUT_DELAY_REG Name Register

31	30	29	28	27	26	25	24
R21							
R							
0h							
23	22	21	20	19	18	17	16
R21			DPMOPS	PSTD			
R			R/W	R/W			
0h			0h	186A0h			
15	14	13	12	11	10	9	8
PSTD							
R/W							
186A0h							
7	6	5	4	3	2	1	0
PSTD							
R/W							
186A0h							

Table 14-19810. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PME_SERVICE_TIMEOUT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	R21	R	0h	Reserved
20	DPMOPS	R/W	0h	When this bit is set, Controller will not automatically send a PME message, when PM Status bit in PMCSR register is set
19:0	PSTD	R/W	186A0h	Specifies the timeout delay for retransmission of PM_PME messages. The value is in units of microseconds. The actual time elapsed has a +1 microseconds tolerance from the value programmed.

14.9.2.2.2.176 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ROOT_PORT_REQUESTOR_ID_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ROOT_PORT_REQUESTOR_ID_REG Register (Offset = 228h) [reset = 0h]

When the Controller is configured as Root Complex, this ID will be used for all internally generated messages.

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Table 14-19811. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0228h**

Figure 14-6544. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ROOT_PORT_REQUESTOR_ID_REG Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
RPRI							
R/W							
0h							
7	6	5	4	3	2	1	0
RPRI							
R/W							
0h							

Table 14-19813. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ROOT_PORT_REQUESTOR_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R0	R	0h	Reserved
15:0	RPRI	R/W	0h	RID [bus, device and function numbers] for all TLPs internally generated by Root Port

14.9.2.2.2.177 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EP_BUS_DEVICE_NUMBER_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EP_BUS_DEVICE_NUMBER_REG Register (Offset = 22Ch) [reset = 0h]

When the Controller is configured as End Point, this register holds the Bus and Device number captured for Function 0

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Table 14-19814. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 022Ch**

Figure 14-6545. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EP_BUS_DEVICE_NUMBER_REG Name Register

31	30	29	28	27	26	25	24
R16							
R							
0h							
23	22	21	20	19	18	17	16
R16							
R							
0h							
15	14	13	12	11	10	9	8
EPBN							
R							
0h							
7	6	5	4	3	2	1	0
R5			EPDN				
R			R				
0h			0h				

Table 14-19816. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EP_BUS_DEVICE_NUMBER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R16	R	0h	Reserved
15:8	EPBN	R	0h	Bus Number captured by Function 0 in End Point mode
7:5	R5	R	0h	Reserved
4:0	EPDN	R	0h	Device Number captured by Function 0 in End Point mode

14.9.2.2.2.178 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_2_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_2_REG Register (Offset = 234h) [reset = 10010840h]

N/A

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Table 14-19817. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0234h**

Figure 14-6546. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_2_REG Name Register

31	30	29	28	27	26	25	24
HRLT	R30	DRXRMFR	DFLRTRB	DTAE2EP	R26	R25	R24
R/W	R	R/W	R/W	R/W	R	R	R
0h	0h	0h	1h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VARCCLKEN	MAXNPREQ						
R/W	R/W						
0h	8h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAXNPREQ			AXINPSPEN_RSVD	CMPTOADV	PSNADV	MSIPIMS	R8
R/W			R	R/W	R/W	R/W	R
8h			0h	1h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BLKALNWIN		BLKALNCHK	R4	ENLNCHK	DISSDSCHK	EXTSNP	DLFFS
R/W		R/W	R	R/W	R/W	R/W	R/W
1h		0h	0h	0h	0h	0h	0h

Table 14-19819. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HRLT	R/W	0h	If set this bit makes the HOT_RESET_OUT signal behave as a level signal rather than a pulse. When set , the HOT_RESET_OUT will be asserted as long as the controller is in the HOT Reset state.
30	R30	R	0h	Reserved
29	DRXRMFR	R/W	0h	By default, when an Uncorrectable error is detected on a receive FIFO RAM, then no packets are read out of the RAM subsequent to the error and the RAMs are frozen. 0 : Receive FIFO RAMs are frozen after an uncorrectable error. 1 : Receive FIFO RAMs continue to read subsequent packets after an uncorrectable error.
28	DFLRTRB	R/W	1h	1 : NP Termination due to FLR/Completion Timeout is delayed till the RX Completion FIFO is Empty. 0 : NP Termination due to FLR is done immediately on receiving FLR/Completion Timeout.

Table 14-19819. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	DTAE2EP	R/W	0h	By default, when End to End Parity error is detected on inbound/ outbound data streams, then all the transmitted outbound packets will be Nullified by the Controller. This bit can be used to turn off nullifying Tx packets on End to End Parity Error.
26	R26	R	0h	Reserved
25	R25	R	0h	Reserved
24	R24	R	0h	Reserved
23	VARCCLKEN	R/W	0h	If this bit is set the CORE_CLK input can be driven with Variable Clock depending on the Link Speed,similar to the PIPE_PCLK.
22:13	MAXNPREQ	R/W	8h	The Controller supports 8 outstanding NP requests that can be initiated by the User. However, the number of split completion TLPs that can be stored in the Controller is limited to 128. The Completion FIFO will overflow if more than 128 split completion packets are pending. If the User interface can accept inbound Posted and Completion packets at the same rate as received from PCIe link, then the split completion FIFO will never reach the FULL condition. However, if the User cannot guarantee this, then this register needs to be programmed as described in the Programming Guide section of the Controller User guide. The Controller will limit the maximum number of outstanding NP requests to the value programmed in this register. Example: 8 : Controller will limit maximum number of outstanding NP requests to 8. 0-7 : Reserved Default Value is 8
12	AXINPSPEN_RSVD	R	0h	RESERVED
11	CMPTOADV	R/W	1h	As per PCIe specification on Error Signaling, the Requester detecting a Completion Timeout is allowed to handle this as an Advisory Non Fatal Error. 1: Completion Timeout is handled as Advisory Non-Fatal Error. 0: Completion Timeout is handled as normally as a Non-Fatal Error.
10	PSNADV	R/W	0h	As per PCIe specification 2.7.2.2, the following Poisoned TLP requests must be handled as Uncorrectable and not as Advisory: I/O Write Request, Memory Write Request, or non-vendor-defined Message with data that target a Control structure. Since it is not possible for the Controller to determine if the target is a Control or a non-Control strusture, the Controller implements this bit for the user to determine the required handling. 1: Poisoned TLP of type IOWr, MemWr, MsgD will be handled as Advisory Non-Fatal Error. 0: Poisoned TLP of type IOWr, MemWr, MsgD will be handled as Uncorrectable Error. Note: Poisoned CplD will always be reported as Advisory Non-Fatal and is not controlled by this register setting.
9	MSIPIMS	R/W	0h	If the Client wishes to use the MSI_PENDING_STATUS_IN Signal to Update the MSI pending Bits register, this bit needs to be set to 1. Otherwise the Pending Bits register is updated via the APB Interface
8	R8	R	0h	Reserved

Table 14-19819. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	BLKALNWIN	R/W	1h	When in the data stream at Gen3 or higher speeds, the pipe_rx_valid is asserted by the PHY. If the block alignment is lost, then the PHY may deassert pipe_rx_valid. Controller reports loss of block alignment if pipe_rx_valid or pipe_rx_data_valid=0 for a period consecutive clock cycles as programmed in this field. 00: 8 CORE_CLK cycles 01: 16 CORE_CLK cycles 10: 64 CORE_CLK cycles 11: 256 CORE_CLK cycles
5	BLKALNCHK	R/W	0h	When in the data stream at Gen3 or higher speeds, the pipe_rx_valid is asserted by the PHY. If the block alignment is lost, then the PHY may deassert pipe_rx_valid. Block Alignment may be lost if the received sync header is invalid. Controller supports detecting loss of block alignment while in a data stream in Gen3. 0: Enable check for loss of Gen3 Block Alignment during data stream. 1: Disable check for loss of Gen3 Block Alignment.
4	R4	R	0h	Reserved
3	ENLNCHK	R/W	0h	As per PCIe specification, LTSSM should transition to Disabled after any Lanes that are transmitting TS1 Ordered Sets receive two consecutive TS1 Ordered Sets with the Disable Link bit asserted. Similarly, LTSSM should transition to Loopback after all Lanes that are transmitting TS1 Ordered Sets, that are also receiving TS1 Ordered Sets, receive the Loopback bit asserted in two consecutive TS1 Ordered Sets. Controller ignores the Link and Lane Number in the Received TS1s with Loopback/Disable bit set. Setting this bit to 1 turns on the check for link number [assigned by RC in Recovery.Idle] and lane number [PAD in Config.LW.Start or as assigned by RC in Recovery.Idle]. This bit is recommended to be kept at the default value of 0.
2	DISSDSCHK	R/W	0h	As per PCIe specification, When using 128b/130b encoding, next state is L0 if eight consecutive Symbol Times of Idle data are received on all configured Lanes. The Controller checks to ensure that the Idle symbols of data are received in Data Blocks after SDS OS. This check is enabled by default. Setting this bit to 1 turns off this check. This bit is recommended to be kept at the default value of 0.
1	EXTSNP	R/W	0h	This bit can be set if an extra clock cycle is required by the Client Application logic to respond with the Read Data on Configuration Snoop Interface. Please refer to the user guide section on Configuration Snoop Interface for timing diagrams.
0	DLFFS	R/W	0h	As per PIPE 4.2 specification, the LOCALLF, LOCALFS outputs from PHY can be sampled uponf PHYSTATUS pulse after Reset# OR upon the first PHYSTATUS pulse after speed change to GEN3. This bit can be set to 1 to disable sampling after speed change to GEN3 or higher

14.9.2.2.2.179 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PHY_STATUS_1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PHY_STATUS_1_REG Register (Offset = 238h) [reset = 0h]

This status register provides additional debug information about the PHY. Bits 8:0 provide information to debug Receiver Errors.

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Table 14-19820. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0238h

Figure 14-6547. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PHY_STATUS_1_REG Name Register

31	30	29	28	27	26	25	24
R31							
R							
0h							
23	22	21	20	19	18	17	16
R31							
R							
0h							
15	14	13	12	11	10	9	8
R31							LOSBLKALN
R							R/W1TC
0h							0h
7	6	5	4	3	2	1	0
INVSYNHR	OSAFSDS	G3FRERR	OSWOEDS	DATEDS	ILOSEDS	OSASKP	TLPPHYER
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-19822. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PHY_STATUS_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	R31	R	0h	Reserved
8	LOSBLKALN	R/W1TC	0h	This bit is set if the PHY Loses Block Alignment during data stream. This is detected based upon an unexpected PIPE_RX_VALID input deassertion during data stream. Write a 1 to clear this error.
7	INVSYNHR	R/W1TC	0h	This bit is set if an invalid Sync Header is detected. 00 and 11 are Invalid Sync Headers. Write a 1 to clear this error. .
6	OSAFSDS	R/W1TC	0h	This bit is set if an SDS is received after an SDS. This is a framing error. Write a 1 to clear this error.
5	G3FRERR	R/W1TC	0h	This bit is set if a framing error is detected while receiving a TLP in Gen3. Example, if an invalid token is received in a data stream, this error is flagged. Write a 1 to clear this error.
4	OSWOEDS	R/W1TC	0h	This bit is set if an Ordered Set Block is received without an EDS. This is a framing error. Write a 1 to clear this error.

Table 14-19822. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PHY_STATUS_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DATEDS	R/W1TC	0h	This bit is set if a Data Block is received after an EDS. Write a 1 to clear this error.
2	ILOSEDS	R/W1TC	0h	The Valid OS blocks after an EDS are EIOS, EIEOS and SKP. If any other OS blocks are received after EDS, then it is a framing error and this bit is asserted.
1	OSASKP	R/W1TC	0h	This bit indicates that an Ordered Set BLock was received immediately after a SKIP OS. This is a framing error. Write a 1 to clear this field.
0	TLPPHYER	R/W1TC	0h	This bit indicates that a PHY Error was detected on the PIPE_RX_STATUS within a TLP. Write a 1 to clear this field.

14.9.2.2.2.180 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_3_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_3_REG Register (Offset = 23Ch) [reset = 0h]

N/A

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Table 14-19823. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 023Ch**

Figure 14-6548. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_3_REG Name Register

31	30	29	28	27	26	25	24
R2							
R							
0h							
23	22	21	20	19	18	17	16
R2							
R							
0h							
15	14	13	12	11	10	9	8
R2							
R							
0h							
7	6	5	4	3	2	1	0
R2			R4	DSDES	DLTE	R1	R0
R			R	R/W	R/W	R	R
0h			0h	0h	0h	0h	0h

Table 14-19825. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_DEBUG_MUX_CONTROL_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	R2	R	0h	Reserved
4	R4	R	0h	Reserved
3	DSDES	R/W	0h	Used to disable and enable Surprise Down Error status logging and by default it is enabled
2	DLTE	R/W	0h	Used to disable and enable link training error logging and by default it is enabled
1	R1	R	0h	Reserved
0	R0	R	0h	Reserved

14.9.2.2.2.181 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RC_BAR_CONFIG_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RC_BAR_CONFIG_REG Register (Offset = 300h) [reset = 2914h]

The root complex side of the Controller contains two memory BARs that can be used for address-range checking of incoming requests from devices connected to it. The fields in this register determine the configuration of these BARs.

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Table 14-19826. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0300h**

Figure 14-6549. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RC_BAR_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RCBCE	R10						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R10			RCBARPIS	RCBARPIE	RCBARPMS	RCBARPME	RCBAR1C
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RCBAR1C		RCBAR1A					RCBAR0C
R/W		R/W					R/W
0h		14h					4h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RCBAR0C		RCBAR0A					
R/W		R/W					
4h		14h					

Table 14-19828. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RC_BAR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RCBCE	R/W	0h	This bit must be set to 1 to enable BAR checking in the RC mode. When this bit is set to 0, the Controller will forward all incoming memory requests to the client logic without checking their address ranges.
30:21	R10	R	0h	Reserved
20	RCBARPIS	R/W	0h	Width of IO Base and Limit registers in type1 config space. 0=32 bits, 1=64bits
19	RCBARPIE	R/W	0h	Enable for IO Base and Limit registers in type1 config space
18	RCBARPMS	R/W	0h	Width of Prefetchable Memory Base and Limit registers in type1 config space. 0=32 bits, 1=64bits
17	RCBARPME	R/W	0h	Enable for Prefetchable memory base and limit registers in type1 config space

Table 14-19828. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RC_BAR_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:14	RCBAR1C	R/W	0h	Specifies the configuration of RC BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110-111: Reserved
13:9	RCBAR1A	R/W	14h	This field specifies the aperture of the RC BAR 1. The encodings are: 0000 = 4, 00001 =8B,..... 1_1101 = 2G
8:6	RCBAR0C	R/W	4h	Specifies the configuration of RC BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable
5:0	RCBAR0A	R/W	14h	This field specifies the aperture of the RC BAR 0. The encodings are: 0000 = 4, 00001 =8B,..... 01_1111 = 8G, ...10_0100 = 256G.

14.9.2.2.2.182 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_DEFAULT_PRESET_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_DEFAULT_PRESET_REG Register (Offset = 360h) [reset = 7FF00h]

This is register specifies the default transmitter preset and default receiver preset hint used by Controller for lanes that have not received EQ TS2s during Recovery.RcvrConfig LTSSM state

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Table 14-19829. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0360h**

Figure 14-6550. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_DEFAULT_PRESET_REG Name Register

31	30	29	28	27	26	25	24
R31							
R							
0h							
23	22	21	20	19	18	17	16
R31					S8GPR		
R					R/W		
0h					7FFh		
15	14	13	12	11	10	9	8
S8GPR							
R/W							
7FFh							
7	6	5	4	3	2	1	0
R7	GDRXPH			GDTXP			
R	R/W			R/W			
0h	0h			0h			

Table 14-19831. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_DEFAULT_PRESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	R31	R	0h	Reserved
18:8	S8GPR	R/W	7FFh	This register can be used to program the Presets that are supported by local Transmitter at 8Gbps. Default value of this register is determined by the SUPPORTED_PRESET strap input. Note: At 8.0 GT/s and 16.0 GT/s all preset values must be supported for Full swing signaling. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3.
7	R7	R	0h	Reserved
6:4	GDRXPH	R/W	0h	Default receiver preset hint value used for a lane that did not receive EQ TS2 in Recovery.RcvrCfg LTSSM state
3:0	GDTXP	R/W	0h	Default transmitter preset value used for a lane that did not receive EQ TS2 in Recovery.RcvrCfg LTSSM state

14.9.2.2.2.183 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_TIMEOUT_2MS_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_TIMEOUT_2MS_REG Register (Offset = 364h) [reset = C001E848h]

This register is used to tune the time spent for evaluation per TX Setting in Endpoint Phase 2 (RC Mode Phase 3) of GEN3 Link Equalization. The PCIe Spec defines a timeout of 2ms per TX setting and hence the default value for this register is set to 2ms. This can be tweaked based on the total number of iterations done and the time required for the PHY to respond with feedback for RXEQEVAL request. The total time taken in Endpoint Phase 2 (RC Mode Phase 3) must be less than 24 ms as defined by spec. Guideline: (Total Number of iterations)*(link_eq_timeout_2ms_reg + max time required for PHY to respond to RXEQEVAL) less than 24ms

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Table 14-19832. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0364h**

Figure 14-6551. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_TIMEOUT_2MS_REG Name Register

31	30	29	28	27	26	25	24
RXEQABM		RXEQABD	R28	LEQT2MS			
R/W		R/W	R	R/W			
3h		0h	0h	1E848h			
23	22	21	20	19	18	17	16
LEQT2MS							
R/W							
1E848h							
15	14	13	12	11	10	9	8
LEQT2MS							
R/W							
1E848h							
7	6	5	4	3	2	1	0
LEQT2MS							
R/W							
1E848h							

Table 14-19834. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_TIMEOUT_2MS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RXEQABM	R/W	3h	When a 24ms timeout occurs in the LTSSM Equalization Phase 2, the Controller aborts Equalization Phase 2 and transitions to Recovery.Rcvr.Lock. In this case, the RxEqEval output on the PIPE Interface will be de-asserted immediately [if it was asserted]. The RxEqInProgress output will stay high and waits for PhyStatus pulse. Controller implements a timer to select an upper limit to wait for this PhyStatus pulse during an abort to de-assert RxEqInProgress. 00: Wait for a maximum of 4 PIPE_PCLK period. 01: Wait for a maximum of 8 PIPE_PCLK period. 10: Wait for a maximum of 16 PIPE_PCLK period. 11: Disabled. Wait till PhyStatus Pulse is received. Note: This register is used only if RxEqEval was asserted when LTSSM 24ms timeout occured in Equalization.

Table 14-19834. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_TIMEOUT_2MS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	RXEQABD	R/W	0h	In an unexpected case where the PIPE_PCLK stops due to error in equalization, this bit can be set to de-couple RxEqInProgress from the rest of the equalization state machine. This bit should not be set for normal usage.
28	R28	R	0h	Reserved
27:0	LEQT2MS	R/W	1E848h	Time spent for evaluation per TX Setting in Endpoint Phase 2 [RC Mode Phase 3] of Link Equalization specified in multiples of 16ns. eg. the value 125000 will result in 125000*16ns = 2ms. Simulation with reduced time mode[PCIE_SIM define] will give a samller value of 300 as power on reset value.

14.9.2.2.2.184 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PIPE_FIFO_LATENCY_CTRL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PIPE_FIFO_LATENCY_CTRL_REG Register (Offset = 368h) [reset = 8000h]

This is register includes bits to control pipe fifo latency

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Table 14-19835. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0368h**

Figure 14-6552. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PIPE_FIFO_LATENCY_CTRL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R31</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R31</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>DPTFWF</td><td colspan="7">R14</td></tr>
<tr><td>R/W</td><td colspan="7">R</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">R14</td><td>DPRFLR</td><td>DPTFCE</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-19837. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PIPE_FIFO_LATENCY_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	R31	R	0h	Reserved
15	DPTFWF	R/W	1h	This bit can be used to prevent PIPE_TX_FIFO from reaching full during TX Electrical Idle. 0: During TX Electrical Idle, the PIPE_TX_FIFO is kept at half fill level by filtering the writes into the PIPE_TX_FIFO. 1: The PIPE_TX_FIFO write filtering logic is turned off. Default value of this bit is 1.
14:2	R14	R	0h	Reserved
1	DPRFLR	R/W	0h	0: If FIFO empty is reached, the PIPE RX FIFO accumulates 2 entries before reading the FIFO again. 1: If FIFO empty is reached, the PIPE RX FIFO accumulates 6 entries before reading the FIFO again. This is to prevent FIFO from reaching empty again. Default value of this bit is 0, in order to reduce the latency through the PIPE RX FIFO.

Table 14-19837. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PIPE_FIFO_LATENCY_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPTFCE	R/W	0h	By default, if FIFO empty is reached, the PIPE TX FIFO accumulates 2 entries before reading the FIFO again. This is to prevent FIFO from reaching empty again. This bit must remain at 0 to allow the PIPE TX FIFO to recover effectively from a Empty condition.

14.9.2.2.2.185 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_CTRL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_CTRL_REG Register (Offset = 37Ch) [reset = 0h]

This register is used to Control GEN3 Link Equalization Procedure.

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Table 14-19838. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 037Ch**

Figure 14-6553. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_CTRL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RES20</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RES20</td><td colspan="4">RES19</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MX8GERL</td><td colspan="2">RES10</td><td>RES9</td><td>QG8GT</td></tr>
<tr><td colspan="4">R/W</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RES6</td><td>RES5</td><td>EP8GRE</td><td>RES3</td><td colspan="3">MXECC</td></tr>
<tr><td colspan="2">R</td><td>R</td><td>R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-19840. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RES20	R	0h	Reserved
19:16	RES19	R	0h	Reserved
15:12	MX8GERL	R/W	0h	The number of 8GT/s Equalization Requests must be finite as per PCIe specification. This register can be used to program the maximum number of 8GT/s equalization requests automatically initiated by the Endpoint. 0000: Automatic 8GT/s Equalization Request Disabled. 0001: Automatic 8GT/s Equalization request limit is 1. 0010: Automatic 8GT/s Equalization request limit is 2. .... 1111: Automatic 8GT/s Equalization request limit is 15,
11:10	RES10	R	0h	Reserved
9	RES9	R	0h	Reserved
8	QG8GT	R/W	0h	This bit can be used to program the Quiesce Guarantee bit of the TS2 in Recovery.Rcvr.Cfg state during 8GT/s Request Equalization.
7:6	RES6	R	0h	Reserved
5	RES5	R	0h	Reserved

Table 14-19840. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EP8GRE	R/W	0h	This bit can be used by Endpoint Device FW to request for 8GT/s Equalization redo. This bit can be set at any time after the Link is Up. Writing a 1 into this field results in the Controller to transition to Recovery. The Request Equalization bit in TS2 Ordered Sets will be set to 1 in Recovery.Rcvr.Cfg to request equalization at 8GTs. This bit is auto-cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. This bit is also auto-cleared when not in Gen3 or Gen4. Device Firmware must wait for the bit to be clear before any subsequent retrain requests.
3	RES3	R	0h	Reserved
2:0	MXECC	R/W	0h	Controls the number of consecutive RxEqEval iterations with direction change feedback of 00s before Equalization Convergence is inferred. 0 : Infer Convergence after 1 feedback of 000000 1 : Infer Convergence after 2 feedback of 000000 2 : Infer Convergence after 3 consecutive feedback of 000000 .. 7 : Infer Convergence after 8 consecutive feedback of 000000. Note: Each lane independently counts consecutive feedback of 000000. Note: Count is reset after a non-000000 feedback on each lane.

14.9.2.2.2.186 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register (Offset = 380h) [reset = B4004h]

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN3 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen3 Equalization Phase 3. When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen3 Equalization Phase 2.

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Table 14-19841. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0380h**

Figure 14-6554. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Name Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R						R	
0h						B40h	
23	22	21	20	19	18	17	16
LEQTXCO							
R							
B40h							
15	14	13	12	11	10	9	8
LEQTXCO							
R							
B40h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV	LEQTXPR			
R			R	R			
0h			0h	4h			

Table 14-19843. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES3126	R	0h	Reserved
25:8	LEQTXCO	R	B40h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cusror Coefficient
7:5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3:0	LEQTXPR	R	4h	TX Preset agreed upon for this lane

14.9.2.2.2.187 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG_AXI Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG_AXI Register (Offset = C80h) [reset = 0h]

This register contains the count of the number of ECC errors detected and corrected during reads from PCIe core AXI external RAMs.

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Table 14-19844. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0C80h**

Figure 14-6555. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG_AXI Name Register

31	30	29	28	27	26	25	24
AXI_MASTER_DIB_CER							
R/W1TC							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AXI_MASTER_RFIFO_CER							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AXI_SLAVE_WFIFO_CER							
R/W1TC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REORDER_CER							
R/W1TC							
0h							

Table 14-19846. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_ECC_CORR_ERR_COUNT_REG_AXI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	AXI_MASTER_DIB_CER	R/W1TC	0h	Number of correctable errors detected while reading from the AXI Master Read Data interleave RAM. This is an 8-bit saturating counter that can be cleared by writing all 1s into it.
23:16	AXI_MASTER_RFIFO_CER	R/W1TC	0h	Number of correctable errors detected while reading from the AXI master read fifo RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
15:8	AXI_SLAVE_WFIFO_CER	R/W1TC	0h	Number of correctable errors detected while reading from the AXI slave write fifo RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
7:0	REORDER_CER	R/W1TC	0h	Number of correctable errors detected while reading from the AXI slave reorder RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.

14.9.2.2.2.188 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL0 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL0 Register (Offset = C88h) [reset = 0h]

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

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Table 14-19847. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0C88h**

Figure 14-6556. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL0 Name Register

31	30	29	28	27	26	25	24
RESERVED				L1DLEUP	L1EM		L1DBRI
NONE				R/W	R		R/W
0h				0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L1XDELAY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
L1XDELAY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
L1XDELAY							
R/W							
0h							

Table 14-19849. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	L1DLEUP	R/W	0h	Pending Tlps trigger a L1 exit by default. This includes internaly generated messages and internaly blocked TLPs. Setting this bit changes the default behavior. This is required only for debug purpose.
26:25	L1EM	R	0h	This field shows the last entered L1 mode. This is useful for debug. bit 0 - Entry mode was ASPM. Bit 1 - Entry mode was PM. This is reset before any new L1 entry.
24	L1DBRI	R/W	0h	Before entering L1, controller internally blocks all TLP and Register Request interface entering controller. interfaces are internally unblocked while exiting L1. This field control this behavior. '1' in this field makes the controler to do not perform any blocking to interfaces. '0' makes the controller behaves normaly. This is required only for debug purpose. Power shutoff feature has to be disabled while using this field.

Table 14-19849. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	L1XDELAY	R/W	0h	Normaly L1 substate entry process is initiated immedaitely after LTSSM enters L1. A delay in micro-seconds can be given in this field to delay L1 substate entry process. This timeout has 0-1us margin of error. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_L1_SUBSTATE_ENTRY_DELAY

14.9.2.2.2.189 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL1 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL1 Register (Offset = C8Ch) [reset = 0h]

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

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Table 14-19850. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0C8Ch**

Figure 14-6557. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
L1ER							
R							
0h							

Table 14-19852. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	L1ER	R	0h	This field shows the values of possible L1 or L1-substate exit triggers. This is useful for debug. this is captured during L1 or L1-substate exit process. this field is reset during L1 entry. 0 : CLIENT_REQ_EXIT_L1 asserted; 1 : Electrical Idle exit detected at link; 2 : New TLP request detected; 3 : Internal request to send TLP. This includes CFG completions. internal messages. INTx messages; 4 : Pending TX traffic available. This could be traffic from DMA and blocked traffic due to credits at AXI.; 5 : #CLKREQ assert detected; 6 : CLIENT_REQ_EXIT_L1_SUBSTATE asserted 7 : Reg Access request detected; Triggers #5,6,7 are valid only with L1-substate supported configs.

14.9.2.2.2.190 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL2 Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL2 Register (Offset = C90h) [reset = A8000000h]

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

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Table 14-19853. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0C90h**

Figure 14-6558. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL2 Name Register

31	30	29	28	27	26	25	24
L1UPACR	L1CSC	L1DAET	L1TROW	L1PS	L1ERC	L1EOC	RESERVED
R/W	R/W	R/W	R	R/W	R/W	R/W	NONE
1h	0h	1h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
L1TWROI							
R/W							
0h							
15	14	13	12	11	10	9	8
L1TWROI							
R/W							
0h							
7	6	5	4	3	2	1	0
L1TWROI							
R/W							
0h							

Table 14-19855. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	L1UPACR	R/W	1h	Setting this field make the state machine to consider LP_CTRL_POWER_RECOVER_ACK as Client system recovery Complete ACK instead of the Controller power stable ACK. This field is ignored if LP_CTRL_BYPASS_ENABLE unset. If this field is set, L1-substate machines expect that the client system finishes power up of the controller within power_on time in the L1-substate capability register and Controller will be waiting in recovery state for ACK. This ensure that the PHY PLL lock and client system initialization goes on in parallel. Default value of this register can be set with the define:den_db_LP_DBG_CTRL_RECOVER_ACK_AS_CLIENT_RECOVER_ACK. Setting this field gives the best system performance.

Table 14-19855. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	L1CSC	R/W	0h	L1-substate removes CORE_CLK. since the registers are implemented in core-clk, register access is not possible during L1-substate. If client can supply a slow clock to core[CORE_CLK] during L1-substates, APB/mgmt access is possible in L1.x. set this bit if client can supply slow clock to CORE_CLK when CLKREQ_IN_N is 1[de-asserted]. If this bit is set, Controller neither wake-up from L1 or generate error response for APB access during L1.x. Controller behavior is undefined if register write is performed while slow clock is supplied to core_clk. Recommended flow is to first exit from L1-substate and perform register writes. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_CLIENT_SUPPLIES_SLOW_CLK_TO_CORE_DURING_L1
29	L1DAET	R/W	1h	L1.x turns off clocks to the controller. Default behavior is made to exit L1.x if Register access request is present at register interface. Setting this bit disables this feature. If this bit is set and CLKREQ_IN_N is 1[de-asserted], Controller responds with ERROR response to APB requests. Client can use CLIENT_EXIT_L1_SUBSTATE pin to trigger L1.x exit if autonomous exit is disabled for register access. This bit is ignored if L1 substate is disabled. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_DISABLE_AUTONOMOUS_L1_EXIT_ON_NEW_REG_REQ
28	L1TROW	R	0h	This is a debug status field. '1' in this field indicates that a timeout has occured while waiting for RX path or OUTstanding packet IDLE conditions. This is cleared on new entry to L1.
27	L1PS	R/W	1h	This field enabled power shutoff mechanism in L1.2 state. This field is ignored if L1.x is not enabled. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_POWER_SHUTOFF_ENABLE
26	L1ERC	R/W	0h	Enables waiting for RX path IDLE condition before entering L1.x. This checks that all packets from PCIE link has reached client side before entering L1.x. This only a tuning register. Not setting this regsiter will cause controller to enter L1.x to save power without checking this. controller will resume transferring RX data once it exit from L1.x state if RX buffers were not empty. This field is ignored if Power shutoff mechanism is enabled for L1.x and Controller will always check RX path idle condition before turning off internal power[with cpf flow]. If timeout is enabled, controller enters L1.x without internal power shutoff after timeout. This bit is ignored if L1 substate is disabled. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_WAIT_FOR_RX_BUFFER_IDLE

Table 14-19855. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	L1EOC	R/W	0h	Enable waiting for outstanding completions before entering L1.x. Outstanding packets expected from pcie link as well as from AXI side is checked. FOR HAL configurations client has to assert PREVENT_L1x_ENTRY signal to prevent L1x entry. This only a tuning register. Not setting this regsiter will cause controller to enter L1.x to save power without checking this. controller exit from L1.x as soon as it receives expected TLps. This field is ignored if Power shutoff mechanism is selected for L1.x and Controller will always wait for outstanding packets before turning off internal power[with cpf flow]. If timeout is enabled, controller enters L1.x without internal power shutoff after timeout. This bit is ignored if L1 substate is disabled. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_WAIT_FOR_OUTSTANDING_CPLS
24	RESERVED	NONE	0h	Reserved
23:0	L1TWROI	R/W	0h	This field enables a timeout mechanism while waiting for RX buffers and Outstanding Pkts before turning off power. Controller enters L1 substate after timeout. A value of 0x0 disables this timeout mechanism. Controller do not select internal power shutoff if it enters L1.x with this timeout. User can give timeout in micro-seconds using this register. This field is ignored if L1 substate is disabled. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_RX_CPL_IDLE_CHECK_TIMEOUT

14.9.2.2.2.191 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_TL_INTERNAL_CONTROL Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_TL_INTERNAL_CONTROL Register (Offset = C94h) [reset = 2h]

This register controls internal behavior of Transaction layer of controller. Adjustment of this register is not required for normal operations.

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Table 14-19856. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0C94h**

Figure 14-6559. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_TL_INTERNAL_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DOOC	ECFLR
NONE						R/W	R/W
0h						1h	0h

Table 14-19858. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_TL_INTERNAL_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DOOC	R/W	1h	Ordering between outbound Completions and posted packets are maintainted in transaction layer. This is achieved by blocking Completions if required. Completions arrived after EOP of a posted packet are blocked till that posted packet is transmitted. This Ordering check is required to conform to the PCIe ordering rules. This ordering check can be disabled by setting this field. Power on reset value of this register can be adjusted by modifying the define den_db_TL_CTRL_DISABLE_OB_ORDERING_CHECK
0	ECFLR	R/W	0h	By default controller ignores config request if a function is under going FLR. Setting this bit Makes the controller to respond with CRS response. Power on reset value of this register can be adjusted by modifying the define den_db_TL_CTRL_ENABLE_CRS_UNDER_FLR

14.9.2.2.2.192 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_2_REGISTER Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_2_REGISTER Register (Offset = D00h) [reset = 0h]

This is an extension of the Local Error and Status Register. This register contains the status of the various events, errors and abnormal conditions in the Controller. Any of the status bits can be reset by writing a 1 into the bit position. Unless masked by the setting of the Local Interrupt Mask 2 Register, the occurrence of any of these conditions causes the Controller to activate the LOCAL_INTERRUPT output.

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Table 14-19859. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0D00h

Figure 14-6560. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_2_REGISTER Name Register

31	30	29	28	27	26	25	24
R31							
R							
0h							
23	22	21	20	19	18	17	16
R31							
R							
0h							
15	14	13	12	11	10	9	8
R31	LEQRQIN	R13_11			R10	PTMCNTAINV	NFTSTOS
R	R/W1TC	R			R	R/W1TC	R/W1TC
0h	0h	0h			0h	0h	0h
7	6	5	4	3	2	1	0
R4				R23		R01	
R				R		R	
0h				0h		0h	

Table 14-19861. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	R31	R	0h	Reserved
14	LEQRQIN	R/W1TC	0h	EP Mode: Indicates that the Controller hardware detected a problem with equalization and automatically requested for equalization redo at the end of the equalization. Controller checks for problems in Recovery.Rcvr.Lock state by comparing the Tx Coefficients agreed at end of Eq Phase2 with the Tx Coefficients received in TS1s in Recovery.Rcvr.Lock state at the end of equalization. Any mismatch is detected and the Request Equalization bit is set in Recovery.Rcvg.Cfg. RC Mode: Indicates that the Controller received Equalization Request from downstream component.
13:11	R13_11	R	0h	Reserved
10	R10	R	0h	Reserved

Table 14-19861. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PTMCNTAINV	R/W1TC	0h	This status bit indicates that the Controller automatically invalidated PTM Context because of PCIe Link exit from L0 State.
8	NFTSTOS	R/W1TC	0h	This status bit indicates that a NFTS Timeout occured. This could occur if the PHY failed to achieve lock on the receive data before the NFTS Timeout during Rx_L0s.FTS state. Local Firmware should consider increasing the advertized NFTS values if this event occurs.
7:4	R4	R	0h	Reserved
3:2	R23	R	0h	Reserved
1:0	R01	R	0h	Reserved

14.9.2.2.2.193 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_2_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_2_REG Register (Offset = D04h) [reset = 4200h]

This is an extension of the Local Interrupt Mask Register. This register contains a mask bit for each interrupting condition in local_error_status_2_register. Setting the bit to 1 prevents the corresponding condition in the Local Error Status 2 Register from activating the LOCAL_INTERRUPT output.

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Table 14-19862. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0D04h**

Figure 14-6561. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_2_REG Name Register

31	30	29	28	27	26	25	24
R31							
R							
0h							
23	22	21	20	19	18	17	16
R31							
R							
0h							
15	14	13	12	11	10	9	8
R31	LEQRQINM	R13_11			R10	PCAIM	NFTSTOM
R	R/W	R			R	R/W	R/W
0h	1h	0h			0h	1h	0h
7	6	5	4	3	2	1	0
R4				R23		R01	
R				R		R	
0h				0h		0h	

Table 14-19864. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LOCAL_INTRPT_MASK_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	R31	R	0h	Reserved
14	LEQRQINM	R/W	1h	Mask for Link Equalization Request Interrupt.
13:11	R13_11	R	0h	Reserved
10	R10	R	0h	Reserved
9	PCAIM	R/W	1h	Mask for PTM Context Auto Invalidated event.
8	NFTSTOM	R/W	0h	Mask for NFTS Timeout.
7:4	R4	R	0h	Reserved
3:2	R23	R	0h	Reserved
1:0	R01	R	0h	Reserved

14.9.2.2.2.194 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LD_CTRL Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LD_CTRL Register (Offset = DA0h) [reset = 15F5E10h]

This register is for the control of Link Down Indication Auto Reset behavior

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Table 14-19865. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DA0h**

Figure 14-6562. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LD_CTRL Name Register

31	30	29	28	27	26	25	24
R7							AUTO_EN
R							R/W
0h							1h
23	22	21	20	19	18	17	16
LDTIMER							
R/W							
5F5E10h							
15	14	13	12	11	10	9	8
LDTIMER							
R/W							
5F5E10h							
7	6	5	4	3	2	1	0
LDTIMER							
R/W							
5F5E10h							

Table 14-19867. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	R7	R	0h	Reserved
24	AUTO_EN	R/W	1h	This bit when set indicates that the link down indication auto reset is enabled
23:0	LDTIMER	R/W	5F5E10h	This is a counter timeout value which triggers the internal logic to reset the link down indication bit in the AXI Configuration registers

14.9.2.2.2.195 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_RX_ELEC_IDLE_FILTER_CONTROL Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_RX_ELEC_IDLE_FILTER_CONTROL Register (Offset = DA4h) [reset = 4200000h]

This register controls the behavior of glitch filter on the pipe rx Electrical Idle signal from the PHY/PCS. Adjustment of this register is not required for normal operations.

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Table 14-19868. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DA4h**

Figure 14-6563. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_RX_ELEC_IDLE_FILTER_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GFLCP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GFLCC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVGFLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RSVGFLD</td><td>GFLD</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-19870. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_RX_ELEC_IDLE_FILTER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GFLCP	R/W	4h	This controls the glitch filter on PM Clock domain. This counter indicates the number of PM Clocks the glitch will be filtered out. The total delay of the glitch filter is calculated as [PM Clock Period * Number of PM Clocks] this delay should be same or close enough for both Core Clock[GFLCC] and PM Clock[GFLCP]
23:16	GFLCC	R/W	20h	This controls the glitch filter on CORE Clock domain. This counter indicates the number of CORE Clocks the glitch will be filtered out. The total delay of the glitch filter is calculated as [CORE Clock Period * Number of CORE Clocks] this delay should be same or close enough for both CORE Clock[GFLCC] and PM Clock[GFLCP]
15:1	RSVGFLD	R	0h	Reserved

Table 14-19870. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_RX_ELEC_IDLE_FILTER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GFLD	R/W	0h	By default controller enables glitch filter on all lanes. Setting this bit to one makes the controller to disable the glitch filter on that corresponding lanes in which the bit is set. When all bits are set to one the Glitch filter is completely bypassed, When any bit is zero glitch filter is enabled, and de-glitching is done only on the lanes that are set to zero

14.9.2.2.2.196 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_CONTROL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_CONTROL_REG Register (Offset = DA8h) [reset = 1110h]

The register bits to Control PTM operation are implemented in this Register.

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Table 14-19871. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DA8h**

Figure 14-6564. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RES29			DAINVCNT	INVPTMCNT	RES18		
R			R/W	W	R		
0h			0h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES18						PTMRSEN	PTMRSM
R						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PTMRINT				PTMRFRVL			
R/W				R/W			
1h				1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PTMRFRSC				RES2		PTMRQEN	PTMRQM
R/W				R		R/W	R/W
1h				0h		0h	0h

Table 14-19873. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RES29	R	0h	Reserved
28	DAINVCNT	R/W	0h	By default, the Controller automatically invalidates PTM Context when the LTSSM exits L0 state. Client may disable this by writing a 1 to this register.
27	INVPTMCNT	W	0h	Client Firmware may write a 1 to this bit in order to reset the PTM Context. This is a write-only bit. Controller internally clears this bit. Read from this bit returns 0. EP Mode: Resets the PTM Request State Machine. PTM Context is Cleared. RP Mode: Resets the PTM Response State Machine. PTM Context is Cleared.
26:18	RES18	R	0h	Reserved

Table 14-19873. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	PTMRSEN	R/W	0h	EP Mode: Reserved RP Mode: This bit enables Controller [RP] to respond to the received PTM Requests. PTM Response/PTM ResponseD is determined by the PTM Response Mode bit. 1 : Controller automatically responds with Response/ResponseD messages. 0 : Controller does not respond for PTM Requests. [PTM Feature is Bypassed.]
16	PTMRSM	R/W	0h	EP Mode: Reserved. RP Mode: This bit is used to control the number of PTM dialogs used during each PTM Master Time Request. 1 : Two Dialog Mode - Each PTM Context will have Response followed by ResponseD. Example: Dialog0: Request -> Response. Dialog1: Request -> ResponseD Dialog2: Request -> Response Dialog3: Request -> ResponseD 0 : Continuous Dialog Mode - Each PTM Context will have Only ResponseD. Example: Dialog0: Request -> Response. Dialog1: Request -> ResponseD Dialog2: Request -> ResponseD Dialog3: Request -> ResponseD
15:12	PTMRINT	R/W	1h	EP Mode: In Single,Periodic Request Mode, this field is used to control the time interval [in us] between PTM Requests within a PTM Context. This represents the time the Requester State Machine waits in the WAIT_1US_STATE. 0001 - 1 0010 - 2 0011 - 3 0100 - 4 0101 - 5 0110 - 6 0111 - 7 1000 - 8 1001 - 9 .. 1111 - 15 This value is in [us]. RP Mode: Reserved.

Table 14-19873. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	PTMRFRVL	R/W	1h	EP Mode: In Periodic Request Mode, this field is used to control the time interval [value] between successive PTM Context Refresh. This represents the time the Requester State Machine waits in the VALID_PTM_CONTEXT_STATE. 0001 - 1 0010 - 2 0011 - 3 0100 - 4 0101 - 5 0110 - 6 0111 - 7 1000 - 8 1001 - 9 1010 - 1111 Reserved This value is multiplied with the scale to determine the PTM Request Time Interval. RP Mode: Reserved.
7:4	PTMRFRSC	R/W	1h	EP Mode: In Periodic Request Mode, this field is used to control the time interval [scale] between successive PTM Context Refresh. This represents the time the Requester State Machine waits in the VALID_PTM_CONTEXT_STATE. 0000 - 1 us 0001 - 10 us 0010 - 100 us 0011 - 1 ms 0100 - 10 ms 0101 - 100 ms 0110 - 1 s 0111 - 10 s 1000 - 100 s 1001 - 1111 - Reserved RP Mode: Reserved.
3:2	RES2	R	0h	Reserved
1	PTMRQEN	R/W	0h	EP Mode: This enables Endpoint to request for PTM Master Time. 1 : PTM Requests are Enabled. In Single Request Mode, this bit is used to trigger PTM dialog to obtain PTM Master time exactly once. This bit is auto-cleared after the PTM Master time is obtained. In Periodic Request Mode, this bit enables periodic requests for PTM Master Time. This bit remains set till it is cleared by the EP local firmware. 0 : PTM Requests are Disabled. [PTM Feature is Bypassed.] User may disable PTM requests in the Controller and, if required, generate requests from Client Master Interface. RP Mode: Reserved.

Table 14-19873. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PTMRQM	R/W	0h	EP Mode: This bit controls the pattern of PTM Requests issued by the Endpoint. 0: Single Request Mode. 1: Periodic Request Mode. In Single Request Mode, Endpoint initiates one or two PTM Dialogs till the PTM Master Time is obtained. In Periodic Request Mode, Endpoint initiates PTM Dialogs and obtains PTM Master at periodic intervals. The period is programmable. RP Mode: Reserved.

14.9.2.2.2.197 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_STATUS_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_STATUS_REG Register (Offset = DACh) [reset = 0h]

The status of PTM Dialog is reflected in this Register.

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Table 14-19874. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DACh**

Figure 14-6565. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RES3							
R							
0h							
23	22	21	20	19	18	17	16
RES3							
R							
0h							
15	14	13	12	11	10	9	8
RES3							
R							
0h							
7	6	5	4	3	2	1	0
RES3				PTMCNST			
R				R			
0h				0h			

Table 14-19876. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LOCAL_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES3	R	0h	Reserved
3:0	PTMCNST	R	0h	Reflects the current status of the PTM Context. In EP Mode: 0000 - Invalid PTM Context 0001 - Dialog 1 PTM Request Sent 0011 - Dialog 1 PTM Response Received 0111 - Dialog 2 PTM Request Sent 1111 - Dialog 2 PTM ResponseD Received and PTM Context Valid In RP Mode: 0000 - Invalid PTM Context 0001 - Dialog 1 PTM Request Received 0011 - Dialog 1 PTM Response Sent 0111 - Dialog 2 PTM Request Received 1111 - Dialog 2 PTM ResponseD Sent and PTM Context Valid

14.9.2.2.2.198 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register (Offset = DB0h) [reset = 0h]

The latency parameters of the PHY may be different at different speeds of operation. Hence, the Controller implements multiple instances of the PTM Latency Parameters Register, one instance for each speed of operation. This register is used to select the speed prior to programming the speed-specific delay parameter registers.

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Table 14-19877. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DB0h**

Figure 14-6566. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_INDEX_REG Name Register

31	30	29	28	27	26	25	24
RES4							
R							
0h							
23	22	21	20	19	18	17	16
RES4							
R							
0h							
15	14	13	12	11	10	9	8
RES4							
R							
0h							
7	6	5	4	3	2	1	0
RES4				PTMLATIN			
R				R/W			
0h				0h			

Table 14-19879. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES4	R	0h	Reserved
3:0	PTMLATIN	R/W	0h	This is used by FW to select the speed for which the Latency parameters are to be programmed. FW is required to set this to each of the supported speeds and program the corresponding latency parameters in the PTM Latency Parameters Register. 0000 - Gen1 Speed Select 0001 - Gen2 Speed Select 0010 - Gen3 Speed Select 0011 - Gen4 Speed Select Others - Reserved

14.9.2.2.2.199 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_REG Register (Offset = DB4h) [reset = 0h]

This register is used to define the PHY specific delay parameters. This register also implements control bits to fine-tune timestamps that are captured by the Controller. Internally, one instance of this register is implemented for each of the speeds supported by the Controller and is indexed by the PTM Latency Parameters Index Register.

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Table 14-19880. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DB4h**

Figure 14-6567. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RXDLTUN</td><td colspan="4">TXDLTUN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RES20</td><td colspan="4">PTMRXLAT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">PTMRXLAT</td><td colspan="2">PTMTXLAT</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PTMTXLAT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19882. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RXDLTUN	R/W	0h	In EP Mode: This field can be used to add a fixed offset to the captured timestamps t4 and t4_tick. In RP Mode: This field can be used to add a fixed offset to the captured timestamps t2 and t2_tick. Encoding: 0000: + 0 ns 0001: + 1ns 0010: + 2ns .... 1111: + 15ns Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding value be programmed into this register.

Table 14-19882. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_LATENCY_PARAMETERS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:24	TXDLTUN	R/W	0h	In EP Mode: This field can be used to add a fixed offset to the captured timestamps t1 and t1_tick. In RP Mode: This field can be used to add a fixed offset to the captured timestamps t3 and t3_tick. Encoding: 0000: + 0 ns 0001: + 1ns 0010: + 2ns .... 1111: + 15ns Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding value be programmed into this register.
23:20	RES20	R	0h	Reserved
19:10	PTMRXLAT	R/W	0h	This field should be programmed with the parameter Receive Latency in [ns] from the PHY Datasheet. Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding latency be programmed into this register.
9:0	PTMTXLAT	R/W	0h	This field should be programmed with the parameter Transmit Latency in [ns] from the PHY Datasheet. Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding latency be programmed into this register.

14.9.2.2.2.200 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_1_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_1_REG Register (Offset = DB8h) [reset = 0h]

PTM Context 1 Register.

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Table 14-19883. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0DB8h

Figure 14-6568. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_1_REG Name Register

31	30	29	28	27	26	25	24
PTMT1T2							
R							
0h							
23	22	21	20	19	18	17	16
PTMT1T2							
R							
0h							
15	14	13	12	11	10	9	8
PTMT1T2							
R							
0h							
7	6	5	4	3	2	1	0
PTMT1T2							
R							
0h							

Table 14-19885. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT1T2	R	0h	EP Mode : Represents the lower 32-bits of timestamp t1 in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t2 in [ns] as recorded by RP.

14.9.2.2.2.201 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_2_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_2_REG Register (Offset = DBCh) [reset = 0h]

PTM Context 2 Register.

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Table 14-19886. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0DBCh

Figure 14-6569. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_2_REG Name Register

31	30	29	28	27	26	25	24
PTMT1T2U							
R							
0h							
23	22	21	20	19	18	17	16
PTMT1T2U							
R							
0h							
15	14	13	12	11	10	9	8
PTMT1T2U							
R							
0h							
7	6	5	4	3	2	1	0
PTMT1T2U							
R							
0h							

Table 14-19888. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT1T2U	R	0h	EP Mode : Represents the upper 32-bits of timestamp t1 in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t2 in [ns] as recorded by RP.

14.9.2.2.2.202 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_3_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_3_REG Register (Offset = DC0h) [reset = 0h]

PTM Context 3 Register.

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Table 14-19889. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DC0h**

Figure 14-6570. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_3_REG Name Register

31	30	29	28	27	26	25	24
PTMT4T3							
R							
0h							
23	22	21	20	19	18	17	16
PTMT4T3							
R							
0h							
15	14	13	12	11	10	9	8
PTMT4T3							
R							
0h							
7	6	5	4	3	2	1	0
PTMT4T3							
R							
0h							

Table 14-19891. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT4T3	R	0h	EP Mode : Represents the lower 32-bits of timestamp t4 in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t3 in [ns] as recorded by RP.

14.9.2.2.2.203 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_4_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_4_REG Register (Offset = DC4h) [reset = 0h]

PTM Context 4 Register.

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Table 14-19892. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0DC4h

Figure 14-6571. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_4_REG Name Register

31	30	29	28	27	26	25	24
PTMT4T3U							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PTMT4T3U							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PTMT4T3U							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PTMT4T3U							
R							
0h							

Table 14-19894. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT4T3U	R	0h	EP Mode : Represents the upper 32-bits of timestamp t4 in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t3 in [ns] as recorded by RP.

14.9.2.2.2.204 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_5_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_5_REG Register (Offset = DC8h) [reset = 0h]

PTM Context 5 Register.

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Table 14-19895. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0DC8h

Figure 14-6572. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_5_REG Name Register

31	30	29	28	27	26	25	24
PTMT1KT2K							
R							
0h							
23	22	21	20	19	18	17	16
PTMT1KT2K							
R							
0h							
15	14	13	12	11	10	9	8
PTMT1KT2K							
R							
0h							
7	6	5	4	3	2	1	0
PTMT1KT2K							
R							
0h							

Table 14-19897. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT1KT2K	R	0h	EP Mode : Represents the lower 32-bits of timestamp t1_tick in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t2_tick in [ns] as recorded by RP.

14.9.2.2.2.205 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_6_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_6_REG Register (Offset = DCCh) [reset = 0h]

PTM Context 6 Register.

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Table 14-19898. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0DCCh

Figure 14-6573. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_6_REG Name Register

31	30	29	28	27	26	25	24
PTMT1KT2KU							
R							
0h							
23	22	21	20	19	18	17	16
PTMT1KT2KU							
R							
0h							
15	14	13	12	11	10	9	8
PTMT1KT2KU							
R							
0h							
7	6	5	4	3	2	1	0
PTMT1KT2KU							
R							
0h							

Table 14-19900. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT1KT2KU	R	0h	EP Mode : Represents the upper 32-bits of timestamp t1_tick in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t2_tick in [ns] as recorded by RP.

14.9.2.2.2.206 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_7_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_7_REG Register (Offset = DD0h) [reset = 0h]

PTM Context 7 Register.

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Table 14-19901. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0DD0h

Figure 14-6574. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_7_REG Name Register

31	30	29	28	27	26	25	24
PTMT4KT3K							
R							
0h							
23	22	21	20	19	18	17	16
PTMT4KT3K							
R							
0h							
15	14	13	12	11	10	9	8
PTMT4KT3K							
R							
0h							
7	6	5	4	3	2	1	0
PTMT4KT3K							
R							
0h							

Table 14-19903. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT4KT3K	R	0h	EP Mode : Represents the lower 32-bits of timestamp t4_tick in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t3_tick in [ns] as recorded by RP.

14.9.2.2.2.207 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_8_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_8_REG Register (Offset = DD4h) [reset = 0h]

PTM Context 8 Register.

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Table 14-19904. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0DD4h

Figure 14-6575. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_8_REG Name Register

31	30	29	28	27	26	25	24
PTMT4KT3KU							
R							
0h							
23	22	21	20	19	18	17	16
PTMT4KT3KU							
R							
0h							
15	14	13	12	11	10	9	8
PTMT4KT3KU							
R							
0h							
7	6	5	4	3	2	1	0
PTMT4KT3KU							
R							
0h							

Table 14-19906. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT4KT3KU	R	0h	EP Mode : Represents the upper 32-bits of timestamp t4_tick in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t3_tick in [ns] as recorded by RP.

14.9.2.2.2.208 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_9_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_9_REG Register (Offset = DD8h) [reset = 0h]

PTM Context 9 Register.

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Table 14-19907. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DD8h**

Figure 14-6576. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_9_REG Name Register

31	30	29	28	27	26	25	24
PTMT3MT2							
R							
0h							
23	22	21	20	19	18	17	16
PTMT3MT2							
R							
0h							
15	14	13	12	11	10	9	8
PTMT3MT2							
R							
0h							
7	6	5	4	3	2	1	0
PTMT3MT2							
R							
0h							

Table 14-19909. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMT3MT2	R	0h	Propagation Delay. EP Mode : Represents the Propagation Delay [t3 - t2] in [ns] as received in ResponseD Message by Endpoint. RP Mode - Reserved.

14.9.2.2.2.209 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_10_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_10_REG Register (Offset = DDCh) [reset = 0h]

PTM Context 10 Register.

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Table 14-19910. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0DDCh**

Figure 14-6577. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_10_REG Name Register

31	30	29	28	27	26	25	24
PTMMSTT1T							
R							
0h							
23	22	21	20	19	18	17	16
PTMMSTT1T							
R							
0h							
15	14	13	12	11	10	9	8
PTMMSTT1T							
R							
0h							
7	6	5	4	3	2	1	0
PTMMSTT1T							
R							
0h							

Table 14-19912. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMMSTT1T	R	0h	EP Mode - Represents the lower 32-bits of PTM Master Time at timestamp t1_tick in [ns] as computed by Endpoint. RP Mode - Reserved.

14.9.2.2.2.210 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_11_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_11_REG Register (Offset = DE0h) [reset = 0h]

PTM Context 11 Register.

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Table 14-19913. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0DE0h

Figure 14-6578. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_11_REG Name Register

31	30	29	28	27	26	25	24
PTMMSTT1TU							
R							
0h							
23	22	21	20	19	18	17	16
PTMMSTT1TU							
R							
0h							
15	14	13	12	11	10	9	8
PTMMSTT1TU							
R							
0h							
7	6	5	4	3	2	1	0
PTMMSTT1TU							
R							
0h							

Table 14-19915. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_PTM_CONTEXT_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTMMSTT1TU	R	0h	EP Mode - Represents the upper 32-bits of PTM Master Time at timestamp t1_tick in [ns] as computed by Endpoint. RP Mode - Reserved.

14.9.2.2.2.211 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_CONTROL_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_CONTROL_REG Register (Offset = E4Ch) [reset = 460h]

The register bits to Control EQ debug Monitor operation are implemented in this Register.

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Table 14-19916. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0E4Ch

Figure 14-6579. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
R1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R1					CAPTBEH	CAPTSPDSEL	
R					R	R/W	
0h					1h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAPTSPDSEL	CAPTPHSEL		CAPTLNSEL				CLRCAPT
R/W	R/W		R/W				R/W
0h	3h		0h				0h

Table 14-19918. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	R1	R	0h	Reserved
10	CAPTBEH	R	1h	If this is set , the first 64 equalization info events are captured else the last 64 events are captured
9:7	CAPTSPDSEL	R/W	0h	Selects the Link Speed at which capture is to be done 000 : Any speed, 001 : Gen 3, 010 : Gen 4, 100 : Gen 5
6:5	CAPTPHSEL	R/W	3h	Selects the Equalization Phase when capture is to be done 01 : Phase 2, 10 : Phase 3, 11 : Phase 2 and 3
4:1	CAPTLNSEL	R/W	0h	Selects the Lane whose Equalization Debug information is to be captured.Please note,this signifies the physical lane number.
0	CLRCAPT	R/W	0h	Setting this bit clears all captured information in the EQ Debug Status Registers. If it is unset then capture is allowed in status registers.

14.9.2.2.2.212 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS0_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS0_REG Register (Offset = E50h) [reset = 0h]

Both the Local and Remote EQ FS and LF values are captured in this Register.

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Table 14-19919. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0E50h

Figure 14-6580. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS0_REG Name Register

31	30	29	28	27	26	25	24
R1							
R							
0h							
23	22	21	20	19	18	17	16
REMLF						REMFS	
R						R	
0h						0h	
15	14	13	12	11	10	9	8
REMFS				LCLLF			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
LCLLF		LCLFS					
R		R					
0h		0h					

Table 14-19921. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	R1	R	0h	Reserved
23:18	REMLF	R	0h	Remote PHY's LF Value Of the Lane and Speed Selected.
17:12	REMFS	R	0h	Remote PHY's FS Value Of the Lane and Speed Selected.
11:6	LCLLF	R	0h	Local PHY's LF Value Of the Lane and Speed Selected.
5:0	LCLFS	R	0h	Local PHY's FS Value Of the Lane and Speed Selected.

14.9.2.2.2.213 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS_REG Register (Offset = E54h) [reset = 0h]

All the Dynamic Equalization information is captured in this Register.This is implemented using a synchronous FIFO which stores all the captured events as sepereate 32 bit entries.The define den_db_EQ_DEBUG_FIFO_NUM_ENTRIES in defines.h controls the number of entries of the FIFO.Every read increments the read pointer and the client must store the data read.The FIFO can be cleared using the 'Clear all Capture bit in the EQ Debug Monitor Control Register.

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Table 14-19922. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0E54h

Figure 14-6581. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS_REG Name Register

31	30	29	28	27	26	25	24
EQPHASE		DIRFED					
R		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COEFFREJ	EQPREVD	EQPRE				EQCOEFF	
R	R	R				R	
0h	0h	0h				0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EQCOEFF							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EQCOEFF							
R							
0h							

Table 14-19924. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	EQPHASE	R	0h	Equalization Phase during Capture 00 : Phase 0, 01 : Phase 1, 10 : Phase 2, 11 : Phase 3
29:24	DIRFED	R	0h	EP Ph2/RC Ph3: Stores Direction Change Feedback or Preset feedback Transmitted to Remote Device. Bit-22, EQPREVD, indicates if this is a Preset feedback or Direction Change Feedback. EP Ph3/RC Ph2: Reserved

Table 14-19924. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_EQ_DEBUG_MON_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	COEFFREJ	R	0h	Phase0: Set to '1' if an unsupported preset is received in Phase0. Phase1: Set to '0' since no reject in phase1. EP Ph2/RC Ph3: Indicates Reject by the Remote end device. This bit indicates that the current Coefficient or Preset was rejected by the remote end device. EP Ph3/RC Ph2: Indicates that Controller Rejected the received settings to Remote Device in the TX TS1/TS2. This Reject indicates the current Coefficients or Preset received from Remote Device are rejected
22	EQPREVD	R	0h	1: Preset Valid, Indicates [21:18] is valid. Phase0: Set to '1' to indicate that the intial Local Preset is Valid. Phase1: Set to '1' to indicate that the advertised Remote Preset is Valid. EP Ph2/RC Ph3: Set to 1 if controller provide preset feedback and to 0 for coefficient feedback. EP Ph3/RC Ph2: Reflects the use preset bit received from the remote end.
21:18	EQPRE	R	0h	Phase0: Stores Initial Local TX Preset received in Phase0. Phase1: Stores Initial Remote Preset advertised in Phase1. EP Ph2/RC Phase3: Stores Current Preset of the Remote Device. EP Ph3/RC Phase2: Stores Preset Received from Remote Device.
17:0	EQCOEFF	R	0h	Phase0: Stores Initial Local TX Coefficients mapped from Initial Preset. Phase1: Stores Initial Remote Coefficients advertised in Phase1. [Cp, LF, FS] , EP Ph2/RC Phase3: Stores Current Coefficients of the Remote Device. EP Ph3/RC Phase2: Stores Coefficients Received from Remote Device.

14.9.2.2.2.214 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_AXI_FEATURE_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_AXI_FEATURE_REG Register (Offset = E5Ch) [reset = 2h]

This register is for the control of AXI Features

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Table 14-19925. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0E5Ch**

Figure 14-6582. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_AXI_FEATURE_REG Name Register

31	30	29	28	27	26	25	24
R30							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R30							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R30							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R30						SLVERRCTRL	R0
R						R/W	R
0h						1h	0h

Table 14-19927. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_AXI_FEATURE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	R30	R	0h	Reserved
1	SLVERRCTRL	R/W	1h	This bit if set to 1, AXI Slave masks the SLVERR response to be given in case of UR or CRS completion for configuration requests. If this bit is set to 0,UR and CRS completions from the link causes SLVERR at AXI.
0	R0	R	0h	Reserved

14.9.2.2.2.215 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINK_EQ_CONTROL_2_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINK_EQ_CONTROL_2_REG Register (Offset = E60h) [reset = 0h]

This register implements fields to control and override Link Equalization.

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Table 14-19928. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0E60h**

Figure 14-6583. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINK_EQ_CONTROL_2_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">R2</td><td colspan="5">R1</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">R1</td><td colspan="2">G3OVRRPR</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">G3OVRRPR</td><td>G3OVRREN</td><td colspan="4">G3RMTXPR</td><td>G3PRRMEN</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
</table>

Table 14-19930. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINK_EQ_CONTROL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	R2	R	0h	Reserved
20:10	R1	R	0h	Reserved
9:6	G3OVRRPR	R/W	0h	This is a debug register field. Can be used in both EP and RP Mode. When enabled using bit-5, this Tx Preset will be applied to the local Transmitter throughout Gen3 regardless of Gen3 Equalization.
5	G3OVRREN	R/W	0h	This is a debug bit. Can be used in both EP and RP Mode. If enabled, the Controller locally applies the Gen3 Local Override Tx Preset to the Local Transmitter throughout Gen3. The Controller performs the Override Preset to Coefficient mapping and then drives on PIPE_TX_DEEMPHASIS signal on the PIPE Interface.
4:1	G3RMTXPR	R/W	0h	Used only in EP Mode. When enabled using bit-0, this Tx Preset will be transmitted in TS1s for the Remote end Transmitter in the first iteration of Gen3 Equalization Phase2. Reserved for RP Mode.

Table 14-19930. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_LINK_EQ_CONTROL_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	G3PRRMEN	R/W	0h	Used only in EP Mode. This bit enables the Controller, to feedback a Tx Preset for the Remote end Transmitter in the first iteration of Link Equalization Phase2 at Gen3 speed. The Gen3 Tx Preset that is used for feedback is programmable in bits [4:1] of this register. Reserved for RP Mode.

14.9.2.2.2.216 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_CORE_FEATURE_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_CORE_FEATURE_REG Register (Offset = E64h) [reset = 0h]

This register is for the control of Core Features

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Table 14-19931. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0E64h**

Figure 14-6584. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_CORE_FEATURE_REG Name Register

31	30	29	28	27	26	25	24
R30							
R							
0h							
23	22	21	20	19	18	17	16
R30							
R							
0h							
15	14	13	12	11	10	9	8
R30							
R							
0h							
7	6	5	4	3	2	1	0
R30					R2	APBCTRL	R0
R					R	R/W	R
0h					0h	0h	0h

Table 14-19933. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_CORE_FEATURE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	R30	R	0h	Reserved
2	R2	R	0h	Reserved
1	APBCTRL	R/W	0h	When set the Core will return SLVERR on the APB bus for Read or Writes to Configuration or Local Management registers
0	R0	R	0h	Reserved

14.9.2.2.2.217 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RX_INVERT_POLARITY_REG Register

1 PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RX_INVERT_POLARITY_REG Register (Offset = E88h) [reset = 0h]

This register shows the polarity inversion status of each lane

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Table 14-19934. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0E88h**

Figure 14-6585. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RX_INVERT_POLARITY_REG Name Register

31	30	29	28	27	26	25	24
R30							
R							
0h							
23	22	21	20	19	18	17	16
R30							
R							
0h							
15	14	13	12	11	10	9	8
R30							
R							
0h							
7	6	5	4	3	2	1	0
R30							RIPR
R							R
0h							0h

Table 14-19936. PCIE_CORE_LM_I_REGF_LM_PCIE_BASE_I_RX_INVERT_POLARITY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	R30	R	0h	Reserved
0	RIPR	R	0h	shows the polarity inversion status of each lane

14.9.2.2.2.218 PCIE_CORE_ATU_WRAPPER_OB_0_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_0_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-19937. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6586. PCIE_CORE_ATU_WRAPPER_OB_0_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-19939. PCIE_CORE_ATU_WRAPPER_OB_0_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.219 PCIE_CORE_ATU_WRAPPER_OB_0_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_0_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-19940. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6587. PCIE_CORE_ATU_WRAPPER_OB_0_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19942. PCIE_CORE_ATU_WRAPPER_OB_0_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.220 PCIE_CORE_ATU_WRAPPER_OB_0_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_0_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-19943. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0008h

Figure 14-6588. PCIE_CORE_ATU_WRAPPER_OB_0_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19945. PCIE_CORE_ATU_WRAPPER_OB_0_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.221 PCIE_CORE_ATU_WRAPPER_OB_0_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_0_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-19946. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6589. PCIE_CORE_ATU_WRAPPER_OB_0_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19948. PCIE_CORE_ATU_WRAPPER_OB_0_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.222 PCIE_CORE_ATU_WRAPPER_OB_0_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_0_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-19949. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6590. PCIE_CORE_ATU_WRAPPER_OB_0_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19951. PCIE_CORE_ATU_WRAPPER_OB_0_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.223 PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-19952. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6591. PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-19954. PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.224 PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-19955. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6592. PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19957. PCIE_CORE_ATU_WRAPPER_OB_0_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.225 PCIE_CORE_ATU_WRAPPER_OB_1_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_1_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-19958. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6593. PCIE_CORE_ATU_WRAPPER_OB_1_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-19960. PCIE_CORE_ATU_WRAPPER_OB_1_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.226 PCIE_CORE_ATU_WRAPPER_OB_1_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_1_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-19961. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6594. PCIE_CORE_ATU_WRAPPER_OB_1_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19963. PCIE_CORE_ATU_WRAPPER_OB_1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.227 PCIE_CORE_ATU_WRAPPER_OB_1_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_1_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-19964. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6595. PCIE_CORE_ATU_WRAPPER_OB_1_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19966. PCIE_CORE_ATU_WRAPPER_OB_1_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.228 PCIE_CORE_ATU_WRAPPER_OB_1_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_1_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-19967. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6596. PCIE_CORE_ATU_WRAPPER_OB_1_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19969. PCIE_CORE_ATU_WRAPPER_OB_1_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.229 PCIE_CORE_ATU_WRAPPER_OB_1_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_1_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-19970. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6597. PCIE_CORE_ATU_WRAPPER_OB_1_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19972. PCIE_CORE_ATU_WRAPPER_OB_1_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.230 PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-19973. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6598. PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-19975. PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.231 PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-19976. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6599. PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19978. PCIE_CORE_ATU_WRAPPER_OB_1_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.232 PCIE_CORE_ATU_WRAPPER_OB_2_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_2_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-19979. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6600. PCIE_CORE_ATU_WRAPPER_OB_2_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-19981. PCIE_CORE_ATU_WRAPPER_OB_2_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.233 PCIE_CORE_ATU_WRAPPER_OB_2_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_2_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-19982. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6601. PCIE_CORE_ATU_WRAPPER_OB_2_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19984. PCIE_CORE_ATU_WRAPPER_OB_2_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.234 PCIE_CORE_ATU_WRAPPER_OB_2_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_2_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-19985. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6602. PCIE_CORE_ATU_WRAPPER_OB_2_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19987. PCIE_CORE_ATU_WRAPPER_OB_2_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.235 PCIE_CORE_ATU_WRAPPER_OB_2_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_2_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-19988. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6603. PCIE_CORE_ATU_WRAPPER_OB_2_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19990. PCIE_CORE_ATU_WRAPPER_OB_2_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.236 PCIE_CORE_ATU_WRAPPER_OB_2_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_2_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-19991. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6604. PCIE_CORE_ATU_WRAPPER_OB_2_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19993. PCIE_CORE_ATU_WRAPPER_OB_2_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.237 PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-19994. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6605. PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-19996. PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.238 PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-19997. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6606. PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-19999. PCIE_CORE_ATU_WRAPPER_OB_2_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.239 PCIE_CORE_ATU_WRAPPER_OB_3_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_3_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20000. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6607. PCIE_CORE_ATU_WRAPPER_OB_3_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20002. PCIE_CORE_ATU_WRAPPER_OB_3_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.240 PCIE_CORE_ATU_WRAPPER_OB_3_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_3_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20003. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6608. PCIE_CORE_ATU_WRAPPER_OB_3_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20005. PCIE_CORE_ATU_WRAPPER_OB_3_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.241 PCIE_CORE_ATU_WRAPPER_OB_3_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_3_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20006. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6609. PCIE_CORE_ATU_WRAPPER_OB_3_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20008. PCIE_CORE_ATU_WRAPPER_OB_3_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.242 PCIE_CORE_ATU_WRAPPER_OB_3_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_3_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20009. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6610. PCIE_CORE_ATU_WRAPPER_OB_3_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20011. PCIE_CORE_ATU_WRAPPER_OB_3_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.243 PCIE_CORE_ATU_WRAPPER_OB_3_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_3_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-20012. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6611. PCIE_CORE_ATU_WRAPPER_OB_3_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20014. PCIE_CORE_ATU_WRAPPER_OB_3_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.244 PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20015. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6612. PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20017. PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.245 PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20018. Instance Table

Instance Name	Physical Address
PCIE0	0D00 001Ch

Figure 14-6613. PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20020. PCIE_CORE_ATU_WRAPPER_OB_3_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.246 PCIE_CORE_ATU_WRAPPER_OB_4_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_4_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20021. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6614. PCIE_CORE_ATU_WRAPPER_OB_4_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20023. PCIE_CORE_ATU_WRAPPER_OB_4_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.247 PCIE_CORE_ATU_WRAPPER_OB_4_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_4_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20024. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6615. PCIE_CORE_ATU_WRAPPER_OB_4_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20026. PCIE_CORE_ATU_WRAPPER_OB_4_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.248 PCIE_CORE_ATU_WRAPPER_OB_4_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_4_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20027. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6616. PCIE_CORE_ATU_WRAPPER_OB_4_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20029. PCIE_CORE_ATU_WRAPPER_OB_4_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.249 PCIE_CORE_ATU_WRAPPER_OB_4_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_4_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20030. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6617. PCIE_CORE_ATU_WRAPPER_OB_4_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20032. PCIE_CORE_ATU_WRAPPER_OB_4_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.250 PCIE_CORE_ATU_WRAPPER_OB_4_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_4_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20033. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6618. PCIE_CORE_ATU_WRAPPER_OB_4_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20035. PCIE_CORE_ATU_WRAPPER_OB_4_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.251 PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20036. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6619. PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">REGION_SIZE</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20038. PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.252 PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20039. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6620. PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20041. PCIE_CORE_ATU_WRAPPER_OB_4_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.253 PCIE_CORE_ATU_WRAPPER_OB_5_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_5_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20042. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6621. PCIE_CORE_ATU_WRAPPER_OB_5_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20044. PCIE_CORE_ATU_WRAPPER_OB_5_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.254 PCIE_CORE_ATU_WRAPPER_OB_5_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_5_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20045. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6622. PCIE_CORE_ATU_WRAPPER_OB_5_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20047. PCIE_CORE_ATU_WRAPPER_OB_5_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.255 PCIE_CORE_ATU_WRAPPER_OB_5_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_5_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20048. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6623. PCIE_CORE_ATU_WRAPPER_OB_5_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20050. PCIE_CORE_ATU_WRAPPER_OB_5_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.256 PCIE_CORE_ATU_WRAPPER_OB_5_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_5_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20051. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6624. PCIE_CORE_ATU_WRAPPER_OB_5_DESC1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20053. PCIE_CORE_ATU_WRAPPER_OB_5_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.257 PCIE_CORE_ATU_WRAPPER_OB_5_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_5_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-20054. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6625. PCIE_CORE_ATU_WRAPPER_OB_5_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20056. PCIE_CORE_ATU_WRAPPER_OB_5_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.258 PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20057. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6626. PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20059. PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.259 PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20060. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6627. PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20062. PCIE_CORE_ATU_WRAPPER_OB_5_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.260 PCIE_CORE_ATU_WRAPPER_OB_6_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_6_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20063. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6628. PCIE_CORE_ATU_WRAPPER_OB_6_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20065. PCIE_CORE_ATU_WRAPPER_OB_6_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.261 PCIE_CORE_ATU_WRAPPER_OB_6_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_6_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20066. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6629. PCIE_CORE_ATU_WRAPPER_OB_6_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20068. PCIE_CORE_ATU_WRAPPER_OB_6_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.262 PCIE_CORE_ATU_WRAPPER_OB_6_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_6_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20069. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6630. PCIE_CORE_ATU_WRAPPER_OB_6_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20071. PCIE_CORE_ATU_WRAPPER_OB_6_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.263 PCIE_CORE_ATU_WRAPPER_OB_6_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_6_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20072. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6631. PCIE_CORE_ATU_WRAPPER_OB_6_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20074. PCIE_CORE_ATU_WRAPPER_OB_6_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.264 PCIE_CORE_ATU_WRAPPER_OB_6_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_6_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20075. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6632. PCIE_CORE_ATU_WRAPPER_OB_6_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD	DATA						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20077. PCIE_CORE_ATU_WRAPPER_OB_6_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.265 PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20078. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6633. PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20080. PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.266 PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20081. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6634. PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20083. PCIE_CORE_ATU_WRAPPER_OB_6_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.267 PCIE_CORE_ATU_WRAPPER_OB_7_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_7_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20084. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6635. PCIE_CORE_ATU_WRAPPER_OB_7_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20086. PCIE_CORE_ATU_WRAPPER_OB_7_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.268 PCIE_CORE_ATU_WRAPPER_OB_7_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_7_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20087. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6636. PCIE_CORE_ATU_WRAPPER_OB_7_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20089. PCIE_CORE_ATU_WRAPPER_OB_7_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.269 PCIE_CORE_ATU_WRAPPER_OB_7_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_7_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20090. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6637. PCIE_CORE_ATU_WRAPPER_OB_7_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20092. PCIE_CORE_ATU_WRAPPER_OB_7_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.270 PCIE_CORE_ATU_WRAPPER_OB_7_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_7_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20093. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6638. PCIE_CORE_ATU_WRAPPER_OB_7_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20095. PCIE_CORE_ATU_WRAPPER_OB_7_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.271 PCIE_CORE_ATU_WRAPPER_OB_7_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_7_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20096. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6639. PCIE_CORE_ATU_WRAPPER_OB_7_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20098. PCIE_CORE_ATU_WRAPPER_OB_7_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.272 PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20099. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6640. PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20101. PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.273 PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20102. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6641. PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20104. PCIE_CORE_ATU_WRAPPER_OB_7_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.274 PCIE_CORE_ATU_WRAPPER_OB_8_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_8_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20105. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6642. PCIE_CORE_ATU_WRAPPER_OB_8_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20107. PCIE_CORE_ATU_WRAPPER_OB_8_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.275 PCIE_CORE_ATU_WRAPPER_OB_8_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_8_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20108. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6643. PCIE_CORE_ATU_WRAPPER_OB_8_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20110. PCIE_CORE_ATU_WRAPPER_OB_8_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.276 PCIE_CORE_ATU_WRAPPER_OB_8_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_8_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20111. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6644. PCIE_CORE_ATU_WRAPPER_OB_8_DESC0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20113. PCIE_CORE_ATU_WRAPPER_OB_8_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.277 PCIE_CORE_ATU_WRAPPER_OB_8_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_8_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20114. Instance Table

Instance Name	Physical Address
PCIE0	0D00 000Ch

Figure 14-6645. PCIE_CORE_ATU_WRAPPER_OB_8_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20116. PCIE_CORE_ATU_WRAPPER_OB_8_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.278 PCIE_CORE_ATU_WRAPPER_OB_8_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_8_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20117. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6646. PCIE_CORE_ATU_WRAPPER_OB_8_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20119. PCIE_CORE_ATU_WRAPPER_OB_8_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.279 PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20120. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6647. PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20122. PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.280 PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20123. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6648. PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20125. PCIE_CORE_ATU_WRAPPER_OB_8_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.281 PCIE_CORE_ATU_WRAPPER_OB_9_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_9_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20126. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6649. PCIE_CORE_ATU_WRAPPER_OB_9_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20128. PCIE_CORE_ATU_WRAPPER_OB_9_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.282 PCIE_CORE_ATU_WRAPPER_OB_9_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_9_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20129. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6650. PCIE_CORE_ATU_WRAPPER_OB_9_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20131. PCIE_CORE_ATU_WRAPPER_OB_9_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.283 PCIE_CORE_ATU_WRAPPER_OB_9_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_9_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20132. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6651. PCIE_CORE_ATU_WRAPPER_OB_9_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20134. PCIE_CORE_ATU_WRAPPER_OB_9_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.284 PCIE_CORE_ATU_WRAPPER_OB_9_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_9_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20135. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6652. PCIE_CORE_ATU_WRAPPER_OB_9_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20137. PCIE_CORE_ATU_WRAPPER_OB_9_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.285 PCIE_CORE_ATU_WRAPPER_OB_9_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_9_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20138. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6653. PCIE_CORE_ATU_WRAPPER_OB_9_DESC3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RSVD</td><td colspan="7">DATA</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20140. PCIE_CORE_ATU_WRAPPER_OB_9_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.286 PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20141. Instance Table

Instance Name	**Physical Address**
PCIE0	**0D00 0018h**

Figure 14-6654. PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">REGION_SIZE</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20143. PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.287 PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20144. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6655. PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20146. PCIE_CORE_ATU_WRAPPER_OB_9_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.288 PCIE_CORE_ATU_WRAPPER_OB_10_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_10_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20147. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6656. PCIE_CORE_ATU_WRAPPER_OB_10_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20149. PCIE_CORE_ATU_WRAPPER_OB_10_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.289 PCIE_CORE_ATU_WRAPPER_OB_10_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_10_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20150. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0004h

Figure 14-6657. PCIE_CORE_ATU_WRAPPER_OB_10_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20152. PCIE_CORE_ATU_WRAPPER_OB_10_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.290 PCIE_CORE_ATU_WRAPPER_OB_10_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_10_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20153. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6658. PCIE_CORE_ATU_WRAPPER_OB_10_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20155. PCIE_CORE_ATU_WRAPPER_OB_10_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.291 PCIE_CORE_ATU_WRAPPER_OB_10_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_10_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20156. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6659. PCIE_CORE_ATU_WRAPPER_OB_10_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20158. PCIE_CORE_ATU_WRAPPER_OB_10_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.292 PCIE_CORE_ATU_WRAPPER_OB_10_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_10_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20159. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6660. PCIE_CORE_ATU_WRAPPER_OB_10_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20161. PCIE_CORE_ATU_WRAPPER_OB_10_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.293 PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20162. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6661. PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20164. PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.294 PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20165. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6662. PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20167. PCIE_CORE_ATU_WRAPPER_OB_10_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.295 PCIE_CORE_ATU_WRAPPER_OB_11_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_11_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20168. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6663. PCIE_CORE_ATU_WRAPPER_OB_11_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20170. PCIE_CORE_ATU_WRAPPER_OB_11_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.296 PCIE_CORE_ATU_WRAPPER_OB_11_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_11_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20171. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6664. PCIE_CORE_ATU_WRAPPER_OB_11_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20173. PCIE_CORE_ATU_WRAPPER_OB_11_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.297 PCIE_CORE_ATU_WRAPPER_OB_11_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_11_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20174. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6665. PCIE_CORE_ATU_WRAPPER_OB_11_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20176. PCIE_CORE_ATU_WRAPPER_OB_11_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.298 PCIE_CORE_ATU_WRAPPER_OB_11_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_11_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20177. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6666. PCIE_CORE_ATU_WRAPPER_OB_11_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20179. PCIE_CORE_ATU_WRAPPER_OB_11_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.299 PCIE_CORE_ATU_WRAPPER_OB_11_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_11_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20180. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0014h

Figure 14-6667. PCIE_CORE_ATU_WRAPPER_OB_11_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20182. PCIE_CORE_ATU_WRAPPER_OB_11_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.300 PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20183. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6668. PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20185. PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.301 PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20186. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6669. PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20188. PCIE_CORE_ATU_WRAPPER_OB_11_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.302 PCIE_CORE_ATU_WRAPPER_OB_12_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_12_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20189. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6670. PCIE_CORE_ATU_WRAPPER_OB_12_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20191. PCIE_CORE_ATU_WRAPPER_OB_12_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.303 PCIE_CORE_ATU_WRAPPER_OB_12_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_12_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20192. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6671. PCIE_CORE_ATU_WRAPPER_OB_12_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20194. PCIE_CORE_ATU_WRAPPER_OB_12_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.304 PCIE_CORE_ATU_WRAPPER_OB_12_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_12_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20195. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6672. PCIE_CORE_ATU_WRAPPER_OB_12_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20197. PCIE_CORE_ATU_WRAPPER_OB_12_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.305 PCIE_CORE_ATU_WRAPPER_OB_12_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_12_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20198. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6673. PCIE_CORE_ATU_WRAPPER_OB_12_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20200. PCIE_CORE_ATU_WRAPPER_OB_12_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.306 PCIE_CORE_ATU_WRAPPER_OB_12_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_12_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20201. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6674. PCIE_CORE_ATU_WRAPPER_OB_12_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20203. PCIE_CORE_ATU_WRAPPER_OB_12_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.307 PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20204. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6675. PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20206. PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.308 PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20207. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6676. PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20209. PCIE_CORE_ATU_WRAPPER_OB_12_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.309 PCIE_CORE_ATU_WRAPPER_OB_13_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_13_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20210. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6677. PCIE_CORE_ATU_WRAPPER_OB_13_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20212. PCIE_CORE_ATU_WRAPPER_OB_13_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.310 PCIE_CORE_ATU_WRAPPER_OB_13_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_13_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20213. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6678. PCIE_CORE_ATU_WRAPPER_OB_13_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20215. PCIE_CORE_ATU_WRAPPER_OB_13_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.311 PCIE_CORE_ATU_WRAPPER_OB_13_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_13_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20216. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6679. PCIE_CORE_ATU_WRAPPER_OB_13_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20218. PCIE_CORE_ATU_WRAPPER_OB_13_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.312 PCIE_CORE_ATU_WRAPPER_OB_13_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_13_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20219. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6680. PCIE_CORE_ATU_WRAPPER_OB_13_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20221. PCIE_CORE_ATU_WRAPPER_OB_13_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.313 PCIE_CORE_ATU_WRAPPER_OB_13_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_13_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20222. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6681. PCIE_CORE_ATU_WRAPPER_OB_13_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20224. PCIE_CORE_ATU_WRAPPER_OB_13_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.314 PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20225. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6682. PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20227. PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.315 PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20228. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6683. PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20230. PCIE_CORE_ATU_WRAPPER_OB_13_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.316 PCIE_CORE_ATU_WRAPPER_OB_14_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_14_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20231. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6684. PCIE_CORE_ATU_WRAPPER_OB_14_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">NUM_BITS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20233. PCIE_CORE_ATU_WRAPPER_OB_14_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.317 PCIE_CORE_ATU_WRAPPER_OB_14_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_14_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20234. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6685. PCIE_CORE_ATU_WRAPPER_OB_14_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20236. PCIE_CORE_ATU_WRAPPER_OB_14_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.318 PCIE_CORE_ATU_WRAPPER_OB_14_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_14_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20237. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6686. PCIE_CORE_ATU_WRAPPER_OB_14_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20239. PCIE_CORE_ATU_WRAPPER_OB_14_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.319 PCIE_CORE_ATU_WRAPPER_OB_14_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_14_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20240. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6687. PCIE_CORE_ATU_WRAPPER_OB_14_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20242. PCIE_CORE_ATU_WRAPPER_OB_14_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.320 PCIE_CORE_ATU_WRAPPER_OB_14_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_14_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20243. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6688. PCIE_CORE_ATU_WRAPPER_OB_14_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD	DATA						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20245. PCIE_CORE_ATU_WRAPPER_OB_14_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.321 PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20246. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6689. PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20248. PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.322 PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20249. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6690. PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20251. PCIE_CORE_ATU_WRAPPER_OB_14_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.323 PCIE_CORE_ATU_WRAPPER_OB_15_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_15_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20252. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6691. PCIE_CORE_ATU_WRAPPER_OB_15_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20254. PCIE_CORE_ATU_WRAPPER_OB_15_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.324 PCIE_CORE_ATU_WRAPPER_OB_15_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_15_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20255. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6692. PCIE_CORE_ATU_WRAPPER_OB_15_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20257. PCIE_CORE_ATU_WRAPPER_OB_15_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.325 PCIE_CORE_ATU_WRAPPER_OB_15_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_15_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20258. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6693. PCIE_CORE_ATU_WRAPPER_OB_15_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20260. PCIE_CORE_ATU_WRAPPER_OB_15_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.326 PCIE_CORE_ATU_WRAPPER_OB_15_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_15_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20261. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6694. PCIE_CORE_ATU_WRAPPER_OB_15_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20263. PCIE_CORE_ATU_WRAPPER_OB_15_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.327 PCIE_CORE_ATU_WRAPPER_OB_15_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_15_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20264. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6695. PCIE_CORE_ATU_WRAPPER_OB_15_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20266. PCIE_CORE_ATU_WRAPPER_OB_15_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.328 PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20267. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6696. PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							

23	22	21	20	19	18	17	16
DATA							
R/W							
0h							

15	14	13	12	11	10	9	8
DATA							
R/W							
0h							

7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20269. PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.329 PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20270. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6697. PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20272. PCIE_CORE_ATU_WRAPPER_OB_15_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.330 PCIE_CORE_ATU_WRAPPER_OB_16_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_16_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20273. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6698. PCIE_CORE_ATU_WRAPPER_OB_16_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20275. PCIE_CORE_ATU_WRAPPER_OB_16_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.331 PCIE_CORE_ATU_WRAPPER_OB_16_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_16_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20276. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6699. PCIE_CORE_ATU_WRAPPER_OB_16_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20278. PCIE_CORE_ATU_WRAPPER_OB_16_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.332 PCIE_CORE_ATU_WRAPPER_OB_16_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_16_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20279. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6700. PCIE_CORE_ATU_WRAPPER_OB_16_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20281. PCIE_CORE_ATU_WRAPPER_OB_16_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.333 PCIE_CORE_ATU_WRAPPER_OB_16_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_16_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20282. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6701. PCIE_CORE_ATU_WRAPPER_OB_16_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20284. PCIE_CORE_ATU_WRAPPER_OB_16_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.334 PCIE_CORE_ATU_WRAPPER_OB_16_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_16_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20285. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6702. PCIE_CORE_ATU_WRAPPER_OB_16_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20287. PCIE_CORE_ATU_WRAPPER_OB_16_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.335 PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20288. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6703. PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20290. PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.336 PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20291. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6704. PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20293. PCIE_CORE_ATU_WRAPPER_OB_16_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.337 PCIE_CORE_ATU_WRAPPER_OB_17_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_17_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20294. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6705. PCIE_CORE_ATU_WRAPPER_OB_17_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20296. PCIE_CORE_ATU_WRAPPER_OB_17_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.338 PCIE_CORE_ATU_WRAPPER_OB_17_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_17_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20297. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6706. PCIE_CORE_ATU_WRAPPER_OB_17_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20299. PCIE_CORE_ATU_WRAPPER_OB_17_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.339 PCIE_CORE_ATU_WRAPPER_OB_17_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_17_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20300. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6707. PCIE_CORE_ATU_WRAPPER_OB_17_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20302. PCIE_CORE_ATU_WRAPPER_OB_17_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.340 PCIE_CORE_ATU_WRAPPER_OB_17_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_17_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20303. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6708. PCIE_CORE_ATU_WRAPPER_OB_17_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20305. PCIE_CORE_ATU_WRAPPER_OB_17_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.341 PCIE_CORE_ATU_WRAPPER_OB_17_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_17_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-20306. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6709. PCIE_CORE_ATU_WRAPPER_OB_17_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20308. PCIE_CORE_ATU_WRAPPER_OB_17_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.342 PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20309. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6710. PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20311. PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.343 PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20312. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6711. PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20314. PCIE_CORE_ATU_WRAPPER_OB_17_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.344 PCIE_CORE_ATU_WRAPPER_OB_18_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_18_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20315. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6712. PCIE_CORE_ATU_WRAPPER_OB_18_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20317. PCIE_CORE_ATU_WRAPPER_OB_18_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.345 PCIE_CORE_ATU_WRAPPER_OB_18_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_18_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20318. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6713. PCIE_CORE_ATU_WRAPPER_OB_18_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20320. PCIE_CORE_ATU_WRAPPER_OB_18_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.346 PCIE_CORE_ATU_WRAPPER_OB_18_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_18_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20321. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6714. PCIE_CORE_ATU_WRAPPER_OB_18_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20323. PCIE_CORE_ATU_WRAPPER_OB_18_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.347 PCIE_CORE_ATU_WRAPPER_OB_18_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_18_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20324. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6715. PCIE_CORE_ATU_WRAPPER_OB_18_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20326. PCIE_CORE_ATU_WRAPPER_OB_18_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.348 PCIE_CORE_ATU_WRAPPER_OB_18_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_18_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20327. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6716. PCIE_CORE_ATU_WRAPPER_OB_18_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20329. PCIE_CORE_ATU_WRAPPER_OB_18_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.349 PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20330. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6717. PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20332. PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.350 PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20333. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6718. PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20335. PCIE_CORE_ATU_WRAPPER_OB_18_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.351 PCIE_CORE_ATU_WRAPPER_OB_19_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_19_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20336. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6719. PCIE_CORE_ATU_WRAPPER_OB_19_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20338. PCIE_CORE_ATU_WRAPPER_OB_19_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.352 PCIE_CORE_ATU_WRAPPER_OB_19_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_19_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20339. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6720. PCIE_CORE_ATU_WRAPPER_OB_19_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20341. PCIE_CORE_ATU_WRAPPER_OB_19_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.353 PCIE_CORE_ATU_WRAPPER_OB_19_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_19_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20342. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6721. PCIE_CORE_ATU_WRAPPER_OB_19_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20344. PCIE_CORE_ATU_WRAPPER_OB_19_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.354 PCIE_CORE_ATU_WRAPPER_OB_19_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_19_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20345. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6722. PCIE_CORE_ATU_WRAPPER_OB_19_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20347. PCIE_CORE_ATU_WRAPPER_OB_19_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.355 PCIE_CORE_ATU_WRAPPER_OB_19_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_19_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20348. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6723. PCIE_CORE_ATU_WRAPPER_OB_19_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20350. PCIE_CORE_ATU_WRAPPER_OB_19_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.356 PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20351. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6724. PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20353. PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.357 PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20354. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6725. PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20356. PCIE_CORE_ATU_WRAPPER_OB_19_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.358 PCIE_CORE_ATU_WRAPPER_OB_20_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_20_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20357. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6726. PCIE_CORE_ATU_WRAPPER_OB_20_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20359. PCIE_CORE_ATU_WRAPPER_OB_20_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.359 PCIE_CORE_ATU_WRAPPER_OB_20_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_20_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20360. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6727. PCIE_CORE_ATU_WRAPPER_OB_20_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20362. PCIE_CORE_ATU_WRAPPER_OB_20_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.360 PCIE_CORE_ATU_WRAPPER_OB_20_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_20_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20363. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6728. PCIE_CORE_ATU_WRAPPER_OB_20_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20365. PCIE_CORE_ATU_WRAPPER_OB_20_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.361 PCIE_CORE_ATU_WRAPPER_OB_20_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_20_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20366. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6729. PCIE_CORE_ATU_WRAPPER_OB_20_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20368. PCIE_CORE_ATU_WRAPPER_OB_20_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.362 PCIE_CORE_ATU_WRAPPER_OB_20_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_20_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20369. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6730. PCIE_CORE_ATU_WRAPPER_OB_20_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD	DATA						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20371. PCIE_CORE_ATU_WRAPPER_OB_20_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.363 PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20372. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6731. PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20374. PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.364 PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20375. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6732. PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20377. PCIE_CORE_ATU_WRAPPER_OB_20_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.365 PCIE_CORE_ATU_WRAPPER_OB_21_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_21_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20378. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6733. PCIE_CORE_ATU_WRAPPER_OB_21_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">NUM_BITS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20380. PCIE_CORE_ATU_WRAPPER_OB_21_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.366 PCIE_CORE_ATU_WRAPPER_OB_21_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_21_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20381. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6734. PCIE_CORE_ATU_WRAPPER_OB_21_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20383. PCIE_CORE_ATU_WRAPPER_OB_21_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.367 PCIE_CORE_ATU_WRAPPER_OB_21_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_21_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20384. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6735. PCIE_CORE_ATU_WRAPPER_OB_21_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20386. PCIE_CORE_ATU_WRAPPER_OB_21_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.368 PCIE_CORE_ATU_WRAPPER_OB_21_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_21_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20387. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6736. PCIE_CORE_ATU_WRAPPER_OB_21_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20389. PCIE_CORE_ATU_WRAPPER_OB_21_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.369 PCIE_CORE_ATU_WRAPPER_OB_21_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_21_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20390. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6737. PCIE_CORE_ATU_WRAPPER_OB_21_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20392. PCIE_CORE_ATU_WRAPPER_OB_21_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.370 PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20393. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6738. PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20395. PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.371 PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20396. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6739. PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20398. PCIE_CORE_ATU_WRAPPER_OB_21_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.372 PCIE_CORE_ATU_WRAPPER_OB_22_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_22_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20399. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0000h

Figure 14-6740. PCIE_CORE_ATU_WRAPPER_OB_22_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20401. PCIE_CORE_ATU_WRAPPER_OB_22_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.373 PCIE_CORE_ATU_WRAPPER_OB_22_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_22_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20402. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6741. PCIE_CORE_ATU_WRAPPER_OB_22_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20404. PCIE_CORE_ATU_WRAPPER_OB_22_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.374 PCIE_CORE_ATU_WRAPPER_OB_22_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_22_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20405. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6742. PCIE_CORE_ATU_WRAPPER_OB_22_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20407. PCIE_CORE_ATU_WRAPPER_OB_22_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.375 PCIE_CORE_ATU_WRAPPER_OB_22_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_22_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20408. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6743. PCIE_CORE_ATU_WRAPPER_OB_22_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20410. PCIE_CORE_ATU_WRAPPER_OB_22_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.376 PCIE_CORE_ATU_WRAPPER_OB_22_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_22_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20411. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6744. PCIE_CORE_ATU_WRAPPER_OB_22_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20413. PCIE_CORE_ATU_WRAPPER_OB_22_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.377 PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20414. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6745. PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20416. PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.378 PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20417. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6746. PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20419. PCIE_CORE_ATU_WRAPPER_OB_22_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.379 PCIE_CORE_ATU_WRAPPER_OB_23_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_23_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20420. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6747. PCIE_CORE_ATU_WRAPPER_OB_23_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">NUM_BITS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20422. PCIE_CORE_ATU_WRAPPER_OB_23_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.380 PCIE_CORE_ATU_WRAPPER_OB_23_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_23_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20423. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6748. PCIE_CORE_ATU_WRAPPER_OB_23_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20425. PCIE_CORE_ATU_WRAPPER_OB_23_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.381 PCIE_CORE_ATU_WRAPPER_OB_23_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_23_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20426. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6749. PCIE_CORE_ATU_WRAPPER_OB_23_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20428. PCIE_CORE_ATU_WRAPPER_OB_23_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.382 PCIE_CORE_ATU_WRAPPER_OB_23_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_23_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20429. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6750. PCIE_CORE_ATU_WRAPPER_OB_23_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20431. PCIE_CORE_ATU_WRAPPER_OB_23_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.383 PCIE_CORE_ATU_WRAPPER_OB_23_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_23_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-20432. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6751. PCIE_CORE_ATU_WRAPPER_OB_23_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20434. PCIE_CORE_ATU_WRAPPER_OB_23_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.384 PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20435. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6752. PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20437. PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.385 PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20438. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6753. PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20440. PCIE_CORE_ATU_WRAPPER_OB_23_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.386 PCIE_CORE_ATU_WRAPPER_OB_24_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_24_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20441. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6754. PCIE_CORE_ATU_WRAPPER_OB_24_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20443. PCIE_CORE_ATU_WRAPPER_OB_24_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.387 PCIE_CORE_ATU_WRAPPER_OB_24_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_24_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20444. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6755. PCIE_CORE_ATU_WRAPPER_OB_24_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20446. PCIE_CORE_ATU_WRAPPER_OB_24_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.388 PCIE_CORE_ATU_WRAPPER_OB_24_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_24_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20447. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6756. PCIE_CORE_ATU_WRAPPER_OB_24_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20449. PCIE_CORE_ATU_WRAPPER_OB_24_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.389 PCIE_CORE_ATU_WRAPPER_OB_24_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_24_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20450. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6757. PCIE_CORE_ATU_WRAPPER_OB_24_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20452. PCIE_CORE_ATU_WRAPPER_OB_24_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.390 PCIE_CORE_ATU_WRAPPER_OB_24_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_24_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20453. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6758. PCIE_CORE_ATU_WRAPPER_OB_24_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD	DATA						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20455. PCIE_CORE_ATU_WRAPPER_OB_24_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.391 PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20456. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6759. PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">REGION_SIZE</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20458. PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.392 PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20459. Instance Table

Instance Name	Physical Address
PCIE0	0D00 001Ch

Figure 14-6760. PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20461. PCIE_CORE_ATU_WRAPPER_OB_24_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.393 PCIE_CORE_ATU_WRAPPER_OB_25_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_25_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20462. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6761. PCIE_CORE_ATU_WRAPPER_OB_25_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">NUM_BITS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20464. PCIE_CORE_ATU_WRAPPER_OB_25_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.394 PCIE_CORE_ATU_WRAPPER_OB_25_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_25_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20465. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6762. PCIE_CORE_ATU_WRAPPER_OB_25_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20467. PCIE_CORE_ATU_WRAPPER_OB_25_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.395 PCIE_CORE_ATU_WRAPPER_OB_25_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_25_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20468. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6763. PCIE_CORE_ATU_WRAPPER_OB_25_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20470. PCIE_CORE_ATU_WRAPPER_OB_25_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.396 PCIE_CORE_ATU_WRAPPER_OB_25_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_25_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20471. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6764. PCIE_CORE_ATU_WRAPPER_OB_25_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20473. PCIE_CORE_ATU_WRAPPER_OB_25_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.397 PCIE_CORE_ATU_WRAPPER_OB_25_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_25_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-20474. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6765. PCIE_CORE_ATU_WRAPPER_OB_25_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20476. PCIE_CORE_ATU_WRAPPER_OB_25_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.398 PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20477. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6766. PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20479. PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.399 PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20480. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6767. PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20482. PCIE_CORE_ATU_WRAPPER_OB_25_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.400 PCIE_CORE_ATU_WRAPPER_OB_26_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_26_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20483. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6768. PCIE_CORE_ATU_WRAPPER_OB_26_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">NUM_BITS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20485. PCIE_CORE_ATU_WRAPPER_OB_26_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.401 PCIE_CORE_ATU_WRAPPER_OB_26_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_26_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20486. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6769. PCIE_CORE_ATU_WRAPPER_OB_26_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20488. PCIE_CORE_ATU_WRAPPER_OB_26_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.402 PCIE_CORE_ATU_WRAPPER_OB_26_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_26_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20489. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6770. PCIE_CORE_ATU_WRAPPER_OB_26_DESC0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20491. PCIE_CORE_ATU_WRAPPER_OB_26_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.403 PCIE_CORE_ATU_WRAPPER_OB_26_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_26_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20492. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6771. PCIE_CORE_ATU_WRAPPER_OB_26_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20494. PCIE_CORE_ATU_WRAPPER_OB_26_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.404 PCIE_CORE_ATU_WRAPPER_OB_26_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_26_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20495. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6772. PCIE_CORE_ATU_WRAPPER_OB_26_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20497. PCIE_CORE_ATU_WRAPPER_OB_26_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.405 PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20498. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6773. PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20500. PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.406 PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20501. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6774. PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20503. PCIE_CORE_ATU_WRAPPER_OB_26_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.407 PCIE_CORE_ATU_WRAPPER_OB_27_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_27_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20504. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6775. PCIE_CORE_ATU_WRAPPER_OB_27_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20506. PCIE_CORE_ATU_WRAPPER_OB_27_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.408 PCIE_CORE_ATU_WRAPPER_OB_27_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_27_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20507. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6776. PCIE_CORE_ATU_WRAPPER_OB_27_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20509. PCIE_CORE_ATU_WRAPPER_OB_27_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.409 PCIE_CORE_ATU_WRAPPER_OB_27_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_27_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20510. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6777. PCIE_CORE_ATU_WRAPPER_OB_27_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20512. PCIE_CORE_ATU_WRAPPER_OB_27_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.410 PCIE_CORE_ATU_WRAPPER_OB_27_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_27_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20513. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6778. PCIE_CORE_ATU_WRAPPER_OB_27_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20515. PCIE_CORE_ATU_WRAPPER_OB_27_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.411 PCIE_CORE_ATU_WRAPPER_OB_27_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_27_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20516. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6779. PCIE_CORE_ATU_WRAPPER_OB_27_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20518. PCIE_CORE_ATU_WRAPPER_OB_27_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.412 PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20519. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6780. PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20521. PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.413 PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20522. Instance Table

Instance Name	Physical Address
PCIE0	0D00 001Ch

Figure 14-6781. PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20524. PCIE_CORE_ATU_WRAPPER_OB_27_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.414 PCIE_CORE_ATU_WRAPPER_OB_28_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_28_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20525. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6782. PCIE_CORE_ATU_WRAPPER_OB_28_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">NUM_BITS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20527. PCIE_CORE_ATU_WRAPPER_OB_28_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.415 PCIE_CORE_ATU_WRAPPER_OB_28_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_28_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20528. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6783. PCIE_CORE_ATU_WRAPPER_OB_28_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20530. PCIE_CORE_ATU_WRAPPER_OB_28_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.416 PCIE_CORE_ATU_WRAPPER_OB_28_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_28_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20531. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6784. PCIE_CORE_ATU_WRAPPER_OB_28_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20533. PCIE_CORE_ATU_WRAPPER_OB_28_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.417 PCIE_CORE_ATU_WRAPPER_OB_28_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_28_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

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Table 14-20534. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6785. PCIE_CORE_ATU_WRAPPER_OB_28_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20536. PCIE_CORE_ATU_WRAPPER_OB_28_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.418 PCIE_CORE_ATU_WRAPPER_OB_28_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_28_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

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Table 14-20537. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6786. PCIE_CORE_ATU_WRAPPER_OB_28_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD	DATA						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20539. PCIE_CORE_ATU_WRAPPER_OB_28_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.419 PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20540. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6787. PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20542. PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.420 PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20543. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6788. PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20545. PCIE_CORE_ATU_WRAPPER_OB_28_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.421 PCIE_CORE_ATU_WRAPPER_OB_29_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_29_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

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Table 14-20546. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6789. PCIE_CORE_ATU_WRAPPER_OB_29_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20548. PCIE_CORE_ATU_WRAPPER_OB_29_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.422 PCIE_CORE_ATU_WRAPPER_OB_29_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_29_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20549. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6790. PCIE_CORE_ATU_WRAPPER_OB_29_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20551. PCIE_CORE_ATU_WRAPPER_OB_29_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.423 PCIE_CORE_ATU_WRAPPER_OB_29_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_29_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

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Table 14-20552. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6791. PCIE_CORE_ATU_WRAPPER_OB_29_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20554. PCIE_CORE_ATU_WRAPPER_OB_29_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.424 PCIE_CORE_ATU_WRAPPER_OB_29_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_29_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20555. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6792. PCIE_CORE_ATU_WRAPPER_OB_29_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20557. PCIE_CORE_ATU_WRAPPER_OB_29_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.425 PCIE_CORE_ATU_WRAPPER_OB_29_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_29_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20558. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6793. PCIE_CORE_ATU_WRAPPER_OB_29_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD	DATA						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20560. PCIE_CORE_ATU_WRAPPER_OB_29_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.426 PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20561. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6794. PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20563. PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.427 PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20564. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6795. PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20566. PCIE_CORE_ATU_WRAPPER_OB_29_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.428 PCIE_CORE_ATU_WRAPPER_OB_30_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_30_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20567. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6796. PCIE_CORE_ATU_WRAPPER_OB_30_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD</td><td colspan="6">NUM_BITS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-20569. PCIE_CORE_ATU_WRAPPER_OB_30_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.429 PCIE_CORE_ATU_WRAPPER_OB_30_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_30_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

Return to Summary Table

Table 14-20570. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6797. PCIE_CORE_ATU_WRAPPER_OB_30_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20572. PCIE_CORE_ATU_WRAPPER_OB_30_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.430 PCIE_CORE_ATU_WRAPPER_OB_30_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_30_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20573. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6798. PCIE_CORE_ATU_WRAPPER_OB_30_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20575. PCIE_CORE_ATU_WRAPPER_OB_30_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.431 PCIE_CORE_ATU_WRAPPER_OB_30_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_30_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20576. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6799. PCIE_CORE_ATU_WRAPPER_OB_30_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20578. PCIE_CORE_ATU_WRAPPER_OB_30_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.432 PCIE_CORE_ATU_WRAPPER_OB_30_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_30_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20579. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6800. PCIE_CORE_ATU_WRAPPER_OB_30_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD	DATA						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20581. PCIE_CORE_ATU_WRAPPER_OB_30_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.433 PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Return to Summary Table

Table 14-20582. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6801. PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20584. PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.434 PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

Return to Summary Table

Table 14-20585. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6802. PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20587. PCIE_CORE_ATU_WRAPPER_OB_30_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.435 PCIE_CORE_ATU_WRAPPER_OB_31_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_31_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Return to Summary Table

Table 14-20588. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6803. PCIE_CORE_ATU_WRAPPER_OB_31_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20590. PCIE_CORE_ATU_WRAPPER_OB_31_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7:6	RSVD	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

14.9.2.2.2.436 PCIE_CORE_ATU_WRAPPER_OB_31_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_31_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the PCIe address

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Table 14-20591. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6804. PCIE_CORE_ATU_WRAPPER_OB_31_ADDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20593. PCIE_CORE_ATU_WRAPPER_OB_31_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

14.9.2.2.2.437 PCIE_CORE_ATU_WRAPPER_OB_31_DESC0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_31_DESC0 Register (Offset = 8h) [reset = 0h]

Provides bits 31:0 of the Outbound PCIe Descriptor

Return to Summary Table

Table 14-20594. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0008h**

Figure 14-6805. PCIE_CORE_ATU_WRAPPER_OB_31_DESC0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20596. PCIE_CORE_ATU_WRAPPER_OB_31_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.438 PCIE_CORE_ATU_WRAPPER_OB_31_DESC1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_31_DESC1 Register (Offset = Ch) [reset = 0h]

Provides bits 63:32 of the PCIe Descriptor

Return to Summary Table

Table 14-20597. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 000Ch**

Figure 14-6806. PCIE_CORE_ATU_WRAPPER_OB_31_DESC1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20599. PCIE_CORE_ATU_WRAPPER_OB_31_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

14.9.2.2.2.439 PCIE_CORE_ATU_WRAPPER_OB_31_DESC3 Register

1 PCIE_CORE_ATU_WRAPPER_OB_31_DESC3 Register (Offset = 14h) [reset = 0h]

Provides PASID Value and The present bit

Return to Summary Table

Table 14-20600. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0014h**

Figure 14-6807. PCIE_CORE_ATU_WRAPPER_OB_31_DESC3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD	DATA						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-20602. PCIE_CORE_ATU_WRAPPER_OB_31_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RSVD	R	0h	reserved
22:0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

14.9.2.2.2.440 PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR0 Register (Offset = 18h) [reset = 0h]

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

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Table 14-20603. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0018h**

Figure 14-6808. PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD		REGION_SIZE					
R/W		R/W					
0h		0h					

Table 14-20605. PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7:6	RSVD	R/W	0h	These needs to be forced to 0
5:0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

14.9.2.2.2.441 PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR1 Register (Offset = 1Ch) [reset = 0h]

holds the base address [63:32] of this region.

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Table 14-20606. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 001Ch**

Figure 14-6809. PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20608. PCIE_CORE_ATU_WRAPPER_OB_31_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

14.9.2.2.2.442 PCIE_CORE_ATU_WRAPPER_IB_0_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_IB_0_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the AXI Address and the number of PCIE address bits passed through

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Table 14-20609. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6810. PCIE_CORE_ATU_WRAPPER_IB_0_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD0		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20611. PCIE_CORE_ATU_WRAPPER_IB_0_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of AXI Address Register for BAR N
7:6	RSVD0	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	The value programmed in this register +1 bits are passed through from PCIe to AXI

14.9.2.2.2.443 PCIE_CORE_ATU_WRAPPER_IB_0_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_IB_0_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the AXI Address

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Table 14-20612. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6811. PCIE_CORE_ATU_WRAPPER_IB_0_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20614. PCIE_CORE_ATU_WRAPPER_IB_0_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

14.9.2.2.2.444 PCIE_CORE_ATU_WRAPPER_IB_1_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_IB_1_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the AXI Address and the number of PCIE address bits passed through

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Table 14-20615. Instance Table

Instance Name	Physical Address
PCIE0	0D00 0000h

Figure 14-6812. PCIE_CORE_ATU_WRAPPER_IB_1_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD0		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20617. PCIE_CORE_ATU_WRAPPER_IB_1_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of AXI Address Register for BAR N
7:6	RSVD0	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	The value programmed in this register +1 bits are passed through from PCIe to AXI

14.9.2.2.2.445 PCIE_CORE_ATU_WRAPPER_IB_1_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_IB_1_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the AXI Address

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Table 14-20618. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6813. PCIE_CORE_ATU_WRAPPER_IB_1_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20620. PCIE_CORE_ATU_WRAPPER_IB_1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

14.9.2.2.2.446 PCIE_CORE_ATU_WRAPPER_IB_7_ADDR0 Register

1 PCIE_CORE_ATU_WRAPPER_IB_7_ADDR0 Register (Offset = 0h) [reset = 0h]

Provides bits 31:8 of the AXI Address and the number of PCIE address bits passed through

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Table 14-20621. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6814. PCIE_CORE_ATU_WRAPPER_IB_7_ADDR0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RSVD0		NUM_BITS					
R		R/W					
0h		0h					

Table 14-20623. PCIE_CORE_ATU_WRAPPER_IB_7_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	DATA	R/W	0h	Bits [31:8] of AXI Address Register for BAR N
7:6	RSVD0	R	0h	Bits 7 and 6 are reserved
5:0	NUM_BITS	R/W	0h	The value programmed in this register +1 bits are passed through from PCIe to AXI

14.9.2.2.2.447 PCIE_CORE_ATU_WRAPPER_IB_7_ADDR1 Register

1 PCIE_CORE_ATU_WRAPPER_IB_7_ADDR1 Register (Offset = 4h) [reset = 0h]

Provides bits 63:32 of the AXI Address

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Table 14-20624. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0004h**

Figure 14-6815. PCIE_CORE_ATU_WRAPPER_IB_7_ADDR1 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20626. PCIE_CORE_ATU_WRAPPER_IB_7_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

14.9.2.2.2.448 PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 Register

1 PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 Register (Offset = 0h) [reset = 1008h]

N/A

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Table 14-20627. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6816. PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				HEADER			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
HEADER				DATA			
R/W				R/W			
1h				8h			
7	6	5	4	3	2	1	0
DATA							
R/W							
8h							

Table 14-20629. PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:12	HEADER	R/W	1h	This is the threshold value of the header credits required which is used to flag credit availability in AXI wrapper
11:0	DATA	R/W	8h	This is the threshold value of the payload credits required which is used to flag credit availability in AXI wrapper

14.9.2.2.2.449 PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 Register

1 PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 Register (Offset = 0h) [reset = 0h]

N/A

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Table 14-20630. Instance Table

Instance Name	Physical Address
PCIE0	**0D00 0000h**

Figure 14-6817. PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLEAR_LINK_DOWN_BIT_TO_PROCEED
NONE							R/W
0h							0h

Table 14-20632. PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLEAR_LINK_DOWN_BIT_TO_PROCEED	R/W	0h	This bit will be set when link down reset comes. client should clear this bit before issueing new traffic to the core

14.9.2.2.2.450 USER_CFG_REVID Register

1 USER_CFG_REVID Register (Offset = 0h) [reset = 68141900h]

Module ID register

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Table 14-20633. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0000h**

Figure 14-6818. USER_CFG_REVID Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6814h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODID							
R							
6814h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
3h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-20635. USER_CFG_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6814h	Module ID field Reset Source: cba_mod_g_rst_n
15:11	REVRTL	R	3h	RTL revision. Will vary depending on release Reset Source: cba_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: cba_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: cba_mod_g_rst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: cba_mod_g_rst_n

14.9.2.2.2.451 USER_CFG_CMD_STATUS Register

1 USER_CFG_CMD_STATUS Register (Offset = 4h) [reset = 0h]

Command Status register

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Table 14-20636. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0004h**

Figure 14-6819. USER_CFG_CMD_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINK_TRAINING_ENABLE
NONE							R/W
0h							0h

Table 14-20638. USER_CFG_CMD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINK_TRAINING_ENABLE	R/W	0h	This bit must be set to 1 to enable the LTSSM to bring up the link. Setting it to 0 forces the LTSSM to stay in the Detect.Quiet state. Reset Source: cba_mod_g_rst_n

14.9.2.2.2.452 USER_CFG_RSTCMD Register

1 USER_CFG_RSTCMD Register (Offset = 8h) [reset = 0h]

Reset Command and Status register

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Table 14-20639. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0008h**

Figure 14-6820. USER_CFG_RSTCMD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INIT_HOT_RESET
NONE							R/W
0h							0h

Table 14-20641. USER_CFG_RSTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INIT_HOT_RESET	R/W	0h	When this bit is set to 1'b1 in the RP mode, the core initiates a Hot Reset sequence on the PCIe link. The controller will keep the PCIe link in hot reset when this bit is asserted. When de-asserted, controller will bring the PCIe link out of hot reset and initiate link training. Valid in RP mode only Reset Source: cba_mod_g_rst_n

14.9.2.2.2.453 USER_CFG_INITCFG Register

1 USER_CFG_INITCFG Register (Offset = Ch) [reset = 1C41FFDh]

Initialization configuration register

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Table 14-20642. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 000Ch**

Figure 14-6821. USER_CFG_INITCFG Name Register

31	30	29	28	27	26	25	24
RESERVED							CONFIG_ENABLE
NONE							R/W
0h							1h
23	22	21	20	19	18	17	16
VC_COUNT		MAX_EVAL_ITERATION					
R/W		R/W					
3h		8h					
15	14	13	12	11	10	9	8
MAX_EVAL_ITERATION	BYPASS_PHASE23	BYPASS_REMOTE_TX_EQUALIZATION	SUPPORTED_PRESET				
R/W	R/W	R/W	R/W				
8h	0h	0h	7FFh				
7	6	5	4	3	2	1	0
SUPPORTED_PRESET						DISABLE_GEN3_DC_BALANCE	SRIS_ENABLE
R/W						R/W	R/W
7FFh						0h	1h

Table 14-20644. USER_CFG_INITCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CONFIG_ENABLE	R/W	1h	When this bit is set to 0 in the EP mode, the Controller will generate a CRS Completion in response to Configuration Requests. When this bit is set to 1 in the EP mode, the Controller will generate SC/UR Completion in response to Configuration Requests based on the target function. In systems where the Controller configuration registers are loaded from RAM on power-up, this prevents the Controller from responding to Configuration Requests before all the registers are loaded. This bit is unused in RP Mode. The default value of this bit will be 1 in EP mode and 0 in RP mode Reset Source: cba_mod_g_rst_n
23:22	VC_COUNT	R/W	3h	Number of VCs configured. 00 = 1 VC 01 = 2 VCs, 10 = 3 VCs, 11 = 4 VCs, .. and so on Reset Source: cba_mod_g_rst_n

Table 14-20644. USER_CFG_INITCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:15	MAX_EVAL_ITERATION	R/W	8h	Denotes the maximum number of iterations to be performed during the DirectionChange Feedback Link Equalization in case the direction change feedback does not converge to 00. Supported values are 8-63. Recommended Value is from 8-16 to avoid the 24ms timeout as defined in PCIe spec. Reset Source: cba_mod_g_rst_n
14	BYPASS_PHASE23	R/W	0h	This MMR should be programmed during system boot or initialization. This is used only in Root Port Mode of the PCIe Core. If BYPASS_PHASE23==1: * Phase 2 AND Phase 3 of Link Equalization are bypassed during link equalization If BYPASS_PHASE23==0: * Phase 2 AND Phase 3 of Link Equalization are performed during link equalization Reset Source: cba_mod_g_rst_n
13	BYPASS_REMOTE_TX_EQUALIZATION	R/W	0h	This MMR should be programmed during system boot or initialization. IF BYPASS_REMOTE_TX_EQUALIZATION==1: * In End-Point mode, Phase 2 of link equalization is bypassed * In Root-Port mode, Phase 3 of link equalization is bypassed IF BYPASS_REMOTE_TX_EQUALIZATION==0: * Remote TX Equalization is performed during link equalization Reset Source: cba_mod_g_rst_n

12:2	SUPPORTED_PRESET	R/W	7FFh	This MMR should be programmed during system boot or initialization.
				SUPPORTED_PRESET[i]=1. Indicates Preset #i supported by PHY.
				SUPPORTED_PRESET[i]=0. Indicates Preset #i is not supported by PHY.
				* For Full Swing, all presets [P0 - P10] must be supported.
				* For Reduced Swing, [P4, P1, P9, P5, P6, P3] must be supported, others are optional as per PCIe spec.
				Reset Source: cba_mod_g_rst_n

1	DISABLE_GEN3_DC_BALANCE	R/W	0h	This bit it is used to disable the transmission of special DC Balance symbols in TS1 training sequences for improving the DC balance of the bit stream at 8.0 GT/s or higher speed. This feature was introduced in the 0.71 version of the Gen3 spec. Setting this input to 1 disables the transmission of the special DC Balance symbols by the Controller. Note that the Controller can decode received training sequences with the special DC balance symbols in them correctly regardless of the setting of this input. Reset Source: cba_mod_g_rst_n
0	SRIS_ENABLE	R/W	1h	Should be set as per the System Reference Clocking Implementation. 0 = Separate Tx and Rx Reference Clocks with No Spread Spectum Clocking - SRNS Mode 1 = Separate Tx and Rx Reference Clocks with Spread Spectum Clocking - SRIS Mode. This is the default setting. Note that the common Refclk architecture utilizes the same Refclk for Tx and Rx and so does not introduce any difference between the Tx and Rx Refclk rates. SRIS_ENABLE should be tied to 0 in this case also. Reset Source: cba_mod_g_rst_n

14.9.2.2.2.454 USER_CFG_PMCMD Register

1 USER_CFG_PMCMD Register (Offset = 10h) [reset = 0h]

Power Management command register

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Table 14-20645. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0010h**

Figure 14-6822. USER_CFG_PMCMD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					POWER_STATE_CHANGE_ACK	CLIENT_REQ_EXIT_L1_SUBSTATE	CLIENT_REQ_EXIT_L1
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-20647. USER_CFG_PMCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	POWER_STATE_CHANGE_ACK	R/W	0h	Software must assert this bit for a minimum of one cycle in response to the assertion of POWER_STATE_CHANGE_INTERRUPT, when it is ready to transition to the low-power state requested by the configuration write request. Software may maintain this input high if it does not need to delay the return of the completions for the configuration write transactions causing power-state changes. Reset Source: cba_mod_g_rst_n
1	CLIENT_REQ_EXIT_L1_SUBSTATE	R/W	0h	Client logic can trigger an explicit L1-substate exit by setting this bit. This bit triggers an exit from L1-substates to L0 if controller is already in L1- substates. Controller waits in L1 state for this signal to become de-asserted before entering L1-substate. Controller will respond to normal L1-exit triggers while it waits for de-assertion of this bit. Reset Source: cba_mod_g_rst_n
0	CLIENT_REQ_EXIT_L1	R/W	0h	Client logic can trigger an explicit L1 exit by setting this bit. This bit triggers an exit to L0 from L1 or from L1-substates. This bit can also be used to block L1 entry in End point controllers. Reset Source: cba_mod_g_rst_n

14.9.2.2.2.455 USER_CFG_LINKSTATUS Register

1 USER_CFG_LINKSTATUS Register (Offset = 14h) [reset = 0h]

Link Status register

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Table 14-20648. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0014h**

Figure 14-6823. USER_CFG_LINKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED		LTSSM_STATE					
NONE		R					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	L1_PM_SUBSTATE			LINK_POWER_STATE			
NONE	R			R			
0h	0h			0h			
7	6	5	4	3	2	1	0
RESERVED		NEGOTIATED_SPEED		NEGOTIATED_LINK_WIDTH		LINK_STATUS	
NONE		R		R		R	
0h		0h		0h		0h	

Table 14-20650. USER_CFG_LINKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	LTSSM_STATE	R	0h	Current state of the Link Training and Status State Machine within the core. The encodings of this output are described in Appendix C of the Cadence User guide. Reset Source: cba_mod_g_rst_n
23:15	RESERVED	NONE	0h	Reserved
14:12	L1_PM_SUBSTATE	R	0h	This register provides the current state of the L1 PM substates state machine. Its encodings are: 000 = L1-substate machine not active 001 = L1.0 substate. L1_PM_SUBSTATE shows "L1.0" after the delay programmed in L1 substate entry delay in reg:low_power_debug_control0 010 = L1.1 substate 011 = Reserved 100 = L1.2.Entry substate 101 = L1.2.Idle substate 110 = L1.2.Exit substate 111 = Reserved Reset Source: cba_mod_g_rst_n

Table 14-20650. USER_CFG_LINKSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	LINK_POWER_STATE	R	0h	Current power state of the PCIe link. 0001 = L0 0010 = L0s 0100 = L1 1000 = L2 Reset Source: cba_mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:4	NEGOTIATED_SPEED	R	0h	Current operating speed of the link is as follows: 11: 16 GT/s 10: 8GT/s 01: 5GT/s 00: 2.5GT/s Reset Source: cba_mod_g_rst_n
3:2	NEGOTIATED_LINK_WIDTH	R	0h	Current link width are as follows: 10: x4 01: x2 00: x1 Others: Reserved Reset Source: cba_mod_g_rst_n
1:0	LINK_STATUS	R	0h	Status of the PCI Express link. 00 = No receivers detected. 01 = Link training in progress. 10 = Link up, DL initialization in progress. 11 = Link up, DL initialization completed. Reset Source: cba_mod_g_rst_n

14.9.2.2.2.456 USER_CFG_LEGACY_INTR_SET Register

1 USER_CFG_LEGACY_INTR_SET Register (Offset = 18h) [reset = 0h]

Legacy interrupt set register

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Table 14-20651. Instance Table

Instance Name	Physical Address
PCIE0	0F10 0018h

Figure 14-6824. USER_CFG_LEGACY_INTR_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTA_IN
NONE							R/W
0h							0h

Table 14-20653. USER_CFG_LEGACY_INTR_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTA_IN	R/W	0h	When the core is configured as EP, this bit is used by the client application to signal an interrupt from any of its PCI Functions to the RP using the Legacy PCI Express Interrupt Delivery mechanism of PCI Express. This bit corresponds to INTA of the PCI bus. Asserting this bit causes the core to send out an Assert_INTx message, and de-asserting this bit causes the core to transmit a Deassert_INTx message. Reset Source: cba_mod_g_rst_n

14.9.2.2.2.457 USER_CFG_LEGACY_INT_PENDING Register

1 USER_CFG_LEGACY_INT_PENDING Register (Offset = 1Ch) [reset = 0h]

Legacy interrupt pending set register

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Table 14-20654. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 001Ch**

Figure 14-6825. USER_CFG_LEGACY_INT_PENDING Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							INT_ACK
NONE							R/W1TC
0h							0h
7	6	5	4	3	2	1	0
RESERVED							INT_PENDING_STATUS
NONE							R/W
0h							0h

Table 14-20656. USER_CFG_LEGACY_INT_PENDING Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	INT_ACK	R/W1TC	0h	When using legacy interrupts, this bit indicates that the core has sent an INTx Assert or Deassert message in response to a change in the state of one of the INTx inputs. Reset Source: cba_mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	INT_PENDING_STATUS	R/W	0h	When using legacy interrupts, this input is used to indicate the interrupt pending status of the Physical Functions. The bit i must be set when an interrupt is pending in Function i. Reset Source: cba_mod_g_rst_n

14.9.2.2.2.458 USER_CFG_MSI_STAT Register

1 USER_CFG_MSI_STAT Register (Offset = 20h) [reset = 0h]

MSI status register

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Table 14-20657. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0020h**

Figure 14-6826. USER_CFG_MSI_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MSI_ENABLE
NONE							R
0h							0h

Table 14-20659. USER_CFG_MSI_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MSI_ENABLE	R	0h	When the core is configured in the EndPoint mode to support MSI interrupts, this output is driven by the MSI Enable bit of the MSI Control Registers of the Physical Functions. Bit0 represents the MSI Enable for Physical Function0 and Bit1 represents the MSI Enable for Physical Function 1 Reset Source: cba_mod_g_rst_n

14.9.2.2.2.459 USER_CFG_MSI_VECTOR Register

1 USER_CFG_MSI_VECTOR Register (Offset = 24h) [reset = 0h]

MSI vector register

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Table 14-20660. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0024h**

Figure 14-6827. USER_CFG_MSI_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSI_VECTOR_COUNT		
NONE					R		
0h					0h		

Table 14-20662. USER_CFG_MSI_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSI_VECTOR_COUNT	R	0h	When the core is configured in the EndPoint mode to support MSI interrupts, these outputs are driven by the Multiple Message Enable bits of the MSI Control Registers associated with Physical Functions. These bits encode the number of allocated MSI interrupt vectors for the corresponding Function. Bits[2:0] represents Physical Function0 and Bits[5:3] represents Physical Function 1 Reset Source: cba_mod_g_rst_n

14.9.2.2.2.460 USER_CFG_MSI_MASK_PF0 Register

1 USER_CFG_MSI_MASK_PF0 Register (Offset = 28h) [reset = 0h]

PF0 MSI mask register

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Table 14-20663. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0028h**

Figure 14-6828. USER_CFG_MSI_MASK_PF0 Name Register

31	30	29	28	27	26	25	24
MSI_MASK_PF0							
R							
0h							
23	22	21	20	19	18	17	16
MSI_MASK_PF0							
R							
0h							
15	14	13	12	11	10	9	8
MSI_MASK_PF0							
R							
0h							
7	6	5	4	3	2	1	0
MSI_MASK_PF0							
R							
0h							

Table 14-20665. USER_CFG_MSI_MASK_PF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSI_MASK_PF0	R	0h	These bits provide the setting of the MSI Mask registers of the Physical Function0. Reset Source: cba_mod_g_rst_n

14.9.2.2.2.461 USER_CFG_MSI_PENDING_STATUS_PF0 Register

1 USER_CFG_MSI_PENDING_STATUS_PF0 Register (Offset = 40h) [reset = 0h]

PF0 MSI pending status input register

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Table 14-20666. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 0040h**

Figure 14-6829. USER_CFG_MSI_PENDING_STATUS_PF0 Name Register

31	30	29	28	27	26	25	24
MSI_PENDING_STATUS_PF0							
R/W							
0h							
23	22	21	20	19	18	17	16
MSI_PENDING_STATUS_PF0							
R/W							
0h							
15	14	13	12	11	10	9	8
MSI_PENDING_STATUS_PF0							
R/W							
0h							
7	6	5	4	3	2	1	0
MSI_PENDING_STATUS_PF0							
R/W							
0h							

Table 14-20668. USER_CFG_MSI_PENDING_STATUS_PF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSI_PENDING_STATUS_PF0	R/W	0h	These inputs provide the status of the MSI pending interrupts for the Physical Function0 from the client to the core. If MSI Pending Status In Mode Select is set to 1 in the Debug Mux Control 2 register in local management,the setting of this register determines the value read from the MSI Pending Bits Register PF0. Reset Source: cba_mod_g_rst_n

14.9.2.2.2.462 USER_CFG_MSIX_STAT Register

1 USER_CFG_MSIX_STAT Register (Offset = A4h) [reset = 0h]

MSIX status register

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Table 14-20669. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 00A4h**

Figure 14-6830. USER_CFG_MSIX_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MSIX_ENABLE
NONE							R
0h							0h

Table 14-20671. USER_CFG_MSIX_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MSIX_ENABLE	R	0h	These bits reflect the states of the MSI-X Enable bits in the PCI configuration space of Physical Functions.Bit0 represents the MSIX Enable for Physical Function0 and Bit1 represents the MSIX Enable for Physical Function 1 Reset Source: cba_mod_g_rst_n

14.9.2.2.2.463 USER_CFG_MSIX_MASK Register

1 USER_CFG_MSIX_MASK Register (Offset = A8h) [reset = 0h]

MSIX mask register

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Table 14-20672. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 00A8h**

Figure 14-6831. USER_CFG_MSIX_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MSIX_MASK
NONE							R
0h							0h

Table 14-20674. USER_CFG_MSIX_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MSIX_MASK	R	0h	These bits reflect the states of the MSI-X Function Mask bits in the PCI configuration space of Physical Functions. Bit0 represents Physical Function0 and Bit1 represents Physical Function1 Reset Source: cba_mod_g_rst_n

14.9.2.2.2.464 USER_CFG_FLR_DONE Register

1 USER_CFG_FLR_DONE Register (Offset = B4h) [reset = 0h]

Physical Function-Level Reset Done register

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Table 14-20675. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 00B4h**

Figure 14-6832. USER_CFG_FLR_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FLR_DONE
NONE							W
0h							0h

Table 14-20677. USER_CFG_FLR_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FLR_DONE	W	0h	These bits are connected to the FLR_DONE bits on the PCIe controller core. In EP mode, software needs to write a 1 to bit0 within 100ms after PF0 function-level reset interrupt is asserted. The FLR_DONE[0] input of the PCIe controller is pulsed for one cycle to acknowledge to the core that the application level function level reset processing is complete. This bit will self-clear once the FLR_DONE[0] is pulsed. The PCIe controller will maintain FLR_IN_PROGRESS[0] output high until it is acknowledged by asserting FLR_DONE. Bit 1 is used to acknowledge FLR_DONE for PF1. These bits are not used in RP mode Reset Source: cba_mod_g_rst_n

14.9.2.2.2.465 USER_CFG_PTM_CFG Register

1 USER_CFG_PTM_CFG Register (Offset = BCh) [reset = 100h]

PTM Timestamp configuration register

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Table 14-20678. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 00BCh**

Figure 14-6833. USER_CFG_PTM_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PTM_EP_TIMER_ADJ</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">PTM_CLK_SEL</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-20680. USER_CFG_PTM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	PTM_EP_TIMER_ADJ	R/W	1h	PTM EP Timer tick adjust value. 1 will increment ptm_ep_timer by 1 each clock cycle, 2 will increment the timer by 2 .. 7 will increment the timer by 7. The adjust value should be set prior to enabling PTM operation in the PCIe controller. Reset Source: cba_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	PTM_CLK_SEL	R/W	0h	Select CPTS HW1 push input. 0 will select ptm_local_timer[0], 1 will select ptm_local_timer[1] ... 63 will select ptm_local_timer[63] and 64 will select ptm_local_timer_out_valid. The values 65 to 127 are unused. The PTM clock select bit should be set prior to enabling the PTM operation in the PCIe controller Reset Source: cba_mod_g_rst_n

14.9.2.2.2.466 USER_CFG_PTM_TIMER_LOW Register

1 USER_CFG_PTM_TIMER_LOW Register (Offset = C0h) [reset = 0h]

PTM timer value lower 32-bits

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Table 14-20681. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 00C0h**

Figure 14-6834. USER_CFG_PTM_TIMER_LOW Name Register

31	30	29	28	27	26	25	24
PTM_TIMER_OUT_LOW							
R							
0h							
23	22	21	20	19	18	17	16
PTM_TIMER_OUT_LOW							
R							
0h							
15	14	13	12	11	10	9	8
PTM_TIMER_OUT_LOW							
R							
0h							
7	6	5	4	3	2	1	0
PTM_TIMER_OUT_LOW							
R							
0h							

Table 14-20683. USER_CFG_PTM_TIMER_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTM_TIMER_OUT_LOW	R	0h	ptm_timer_out[31:0] value from PCIe core. Valid in EP mode only Reset Source: cba_mod_g_rst_n

14.9.2.2.2.467 USER_CFG_PTM_TIMER_HIGH Register

1 USER_CFG_PTM_TIMER_HIGH Register (Offset = C4h) [reset = 0h]

PTM timer value upper 32-bits

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Table 14-20684. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 00C4h**

Figure 14-6835. USER_CFG_PTM_TIMER_HIGH Name Register

31	30	29	28	27	26	25	24
PTM_TIMER_OUT_HIGH							
R							
0h							
23	22	21	20	19	18	17	16
PTM_TIMER_OUT_HIGH							
R							
0h							
15	14	13	12	11	10	9	8
PTM_TIMER_OUT_HIGH							
R							
0h							
7	6	5	4	3	2	1	0
PTM_TIMER_OUT_HIGH							
R							
0h							

Table 14-20686. USER_CFG_PTM_TIMER_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PTM_TIMER_OUT_HIGH	R	0h	ptm_timer_out[63:32] value from PCIe core. Valid in EP mode only Reset Source: cba_mod_g_rst_n

14.9.2.2.2.468 USER_CFG_EOI_VECTOR Register

1 USER_CFG_EOI_VECTOR Register (Offset = C8h) [reset = 0h]

EOI vector for re-triggering interrupts

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Table 14-20687. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 00C8h**

Figure 14-6836. USER_CFG_EOI_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-20689. USER_CFG_EOI_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector for level interrupts. Writing the EOI value as specfied to this register will re-trigger a pending interrupt. 0 - Downstream interrupt, 1 - FLR interrupt, 2 - Legacy interrupt, 3 - Power state interrupt Reset Source: cba_mod_g_rst_n

14.9.2.2.2.469 VMAP_OB_VIRTID_MATCH Register

1 VMAP_OB_VIRTID_MATCH Register (Offset = 400h) [reset = 0h]

Outbound virtid match register

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Table 14-20690. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 1400h**

Figure 14-6837. VMAP_OB_VIRTID_MATCH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">VAL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">VAL</td><td colspan="5">RESERVED</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">NONE</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-20692. VMAP_OB_VIRTID_MATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:5	VAL	R/W	0h	Outbound virtid[11:5] match value. When outbound VBUSM slave interface virtid[11:5] matches the value in this register and the ASEL value is non-zero, the PCIe controller address translation unit (ATU) is bypassed. The PCIe TLP descriptor values are taken from the ext_desc registers. Reset Source: mod_g_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.9.2.2.2.470 VMAP_EXT_DESC_j Register

1 VMAP_EXT_DESC_j Register (Offset = 0h + formula) [reset = 0h]

Outbound ASEL non-zero descriptor register

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Offset = (j * 4h); where j = 0 to 31d

Table 14-20693. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 1000h + formula**

Figure 14-6838. VMAP_EXT_DESC_j Name Register

31	30	29	28	27	26	25	24
TRAFFIC_CLASS			RESERVED				
R/W			NONE				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BD_EN
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BUS_NUM							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEV_FUNC_NUM							
R/W							
0h							

Table 14-20695. VMAP_EXT_DESC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	TRAFFIC_CLASS	R/W	0h	PCIe Traffic Class (TC) associated with the non-zero ASEL request. Reset Source: mod_g_rst_n
28:17	RESERVED	NONE	0h	Reserved
16	BD_EN	R/W	0h	External bus and device number enable. This bit enables the client to supply the bus and device numbers to be used in the requester ID. If this bit is 0, the core uses the captured values of the bus and device numbers to form the Requester ID. If this bit is 1, the core uses the bus and device numbers supplied by the client on dev_func_num[7:4] and bus_num[15:8] to form the Requester ID. This bit must always be set while originating requests in the RP mode, and the corresponding Requester ID must be placed on dev_func_num[7:4] and bus_num[15:8]. Reset Source: mod_g_rst_n
15:8	BUS_NUM	R/W	0h	PCI Bus Number associated with the request. When descriptor bit[16] is set, this field must specify the bus number to be used for the Requester ID. Otherwise, this field is ignored by the core. Reset Source: mod_g_rst_n

Table 14-20695. VMAP_EXT_DESC_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	DEV_FUNC_NUM	R/W	0h	PCI Function and Device Number associated with the request. In ARI mode, all 8 bits are used to indicate the requesting function number. In legacy mode, dev_func_num[2:0] are used to specified the function number and dev_func_num[7:3] are used to specify the device number to be used within the Requester ID, if the descriptor bit[16] is set. If the descriptor bit[16] is not set, then bits dev_func_num[7:3] are ignored. Reset Source: mod_g_rst_n

14.9.2.2.2.471 INTD_CFG_REVISION Register

1 INTD_CFG_REVISION Register (Offset = 0h) [reset = 6690A200h]

Revision Register

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Table 14-20696. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2000h**

Figure 14-6839. INTD_CFG_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		690h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
690h							
15	14	13	12	11	10	9	8
RTLVER					MAJREV		
R					R		
14h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-20698. INTD_CFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	BU
27:16	FUNCTION	R	690h	Module ID
15:11	RTLVER	R	14h	RTL revisions
10:8	MAJREV	R	2h	Major revision
7:6	CUSTOM	R	0h	Custom revision
5:0	MINREV	R	0h	Minor revision

14.9.2.2.2.472 INTD_CFG_ENABLE_REG_SYS_0 Register

1 INTD_CFG_ENABLE_REG_SYS_0 Register (Offset = 100h) [reset = 0h]

Enable Register 0

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Table 14-20699. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2100h**

Figure 14-6840. INTD_CFG_ENABLE_REG_SYS_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SYS_EN_PCIE_DOWNSTREAM
NONE							R/W1TS
0h							0h

Table 14-20701. INTD_CFG_ENABLE_REG_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SYS_EN_PCIE_DOWNSTREAM	R/W1TS	0h	Enable Set for sys_en_pcie_downstream

14.9.2.2.2.473 INTD_CFG_ENABLE_REG_SYS_1 Register

1 INTD_CFG_ENABLE_REG_SYS_1 Register (Offset = 104h) [reset = 0h]

Enable Register 1

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Table 14-20702. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2104h**

Figure 14-6841. INTD_CFG_ENABLE_REG_SYS_1 Name Register

31	30	29	28	27	26	25	24
RESERVED					ENABLE_SYS_EN_PCIE_PWR_STATE	ENABLE_SYS_EN_PCIE_LEGACY_3	ENABLE_SYS_EN_PCIE_LEGACY_2
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
23	22	21	20	19	18	17	16
ENABLE_SYS_EN_PCIE_LEGACY_1	ENABLE_SYS_EN_PCIE_LEGACY_0	RESERVED					
R/W1TS	R/W1TS	NONE					
0h	0h	0h					
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SYS_EN_PCIE_FLR
NONE							R/W1TS
0h							0h

Table 14-20704. INTD_CFG_ENABLE_REG_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	ENABLE_SYS_EN_PCIE_PWR_STATE	R/W1TS	0h	Enable Set for sys_en_pcie_pwr_state
25	ENABLE_SYS_EN_PCIE_LEGACY_3	R/W1TS	0h	Enable Set for sys_en_pcie_legacy_3
24	ENABLE_SYS_EN_PCIE_LEGACY_2	R/W1TS	0h	Enable Set for sys_en_pcie_legacy_2
23	ENABLE_SYS_EN_PCIE_LEGACY_1	R/W1TS	0h	Enable Set for sys_en_pcie_legacy_1
22	ENABLE_SYS_EN_PCIE_LEGACY_0	R/W1TS	0h	Enable Set for sys_en_pcie_legacy_0
21:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SYS_EN_PCIE_FLR	R/W1TS	0h	Enable Set for sys_en_pcie_flr

14.9.2.2.2.474 INTD_CFG_ENABLE_REG_SYS_2 Register

1 INTD_CFG_ENABLE_REG_SYS_2 Register (Offset = 108h) [reset = 0h]

Enable Register 2

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Table 14-20705. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2108h**

Figure 14-6842. INTD_CFG_ENABLE_REG_SYS_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				ENABLE_SYS_EN_PCIE_PTM	ENABLE_SYS_EN_PCIE_LINK_STATE	ENABLE_SYS_EN_PCIE_HOT_RESET	ENABLE_SYS_EN_PCIE_ERROR_2
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
ENABLE_SYS_EN_PCIE_ERROR_1	ENABLE_SYS_EN_PCIE_ERROR_0	RESERVED					ENABLE_SYS_EN_PCIE_DPA
R/W1TS	R/W1TS	NONE					R/W1TS
0h	0h	0h					0h

Table 14-20707. INTD_CFG_ENABLE_REG_SYS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	ENABLE_SYS_EN_PCIE_PTM	R/W1TS	0h	Enable Set for sys_en_pcie_ptm
10	ENABLE_SYS_EN_PCIE_LINK_STATE	R/W1TS	0h	Enable Set for sys_en_pcie_link_state
9	ENABLE_SYS_EN_PCIE_HOT_RESET	R/W1TS	0h	Enable Set for sys_en_pcie_hot_reset
8	ENABLE_SYS_EN_PCIE_ERROR_2	R/W1TS	0h	Enable Set for sys_en_pcie_error_2
7	ENABLE_SYS_EN_PCIE_ERROR_1	R/W1TS	0h	Enable Set for sys_en_pcie_error_1
6	ENABLE_SYS_EN_PCIE_ERROR_0	R/W1TS	0h	Enable Set for sys_en_pcie_error_0
5:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SYS_EN_PCIE_DPA	R/W1TS	0h	Enable Set for sys_en_pcie_dpa

14.9.2.2.2.475 INTD_CFG_ENABLE_CLR_REG_SYS_0 Register

1 INTD_CFG_ENABLE_CLR_REG_SYS_0 Register (Offset = 300h) [reset = 0h]

Enable Clear Register 0

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Table 14-20708. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2300h**

Figure 14-6843. INTD_CFG_ENABLE_CLR_REG_SYS_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SYS_EN_PCIE_DOWNSTREAM_CLR
NONE							R/W1TC
0h							0h

Table 14-20710. INTD_CFG_ENABLE_CLR_REG_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SYS_EN_PCIE_DOWNSTREAM_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_downstream

14.9.2.2.2.476 INTD_CFG_ENABLE_CLR_REG_SYS_1 Register

1 INTD_CFG_ENABLE_CLR_REG_SYS_1 Register (Offset = 304h) [reset = 0h]

Enable Clear Register 1

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Table 14-20711. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2304h**

Figure 14-6844. INTD_CFG_ENABLE_CLR_REG_SYS_1 Name Register

31	30	29	28	27	26	25	24
RESERVED					ENABLE_SYS_EN_PCIE_PWR_STATE_CLR	ENABLE_SYS_EN_PCIE_LEGACY_3_CLR	ENABLE_SYS_EN_PCIE_LEGACY_2_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
ENABLE_SYS_EN_PCIE_LEGACY_1_CLR	ENABLE_SYS_EN_PCIE_LEGACY_0_CLR	RESERVED					
R/W1TC	R/W1TC	NONE					
0h	0h	0h					
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SYS_EN_PCIE_FLR_CLR
NONE							R/W1TC
0h							0h

Table 14-20713. INTD_CFG_ENABLE_CLR_REG_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	ENABLE_SYS_EN_PCIE_PWR_STATE_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_pwr_state
25	ENABLE_SYS_EN_PCIE_LEGACY_3_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_legacy_3
24	ENABLE_SYS_EN_PCIE_LEGACY_2_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_legacy_2
23	ENABLE_SYS_EN_PCIE_LEGACY_1_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_legacy_1
22	ENABLE_SYS_EN_PCIE_LEGACY_0_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_legacy_0
21:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SYS_EN_PCIE_FLR_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_flr

14.9.2.2.2.477 INTD_CFG_ENABLE_CLR_REG_SYS_2 Register

1 INTD_CFG_ENABLE_CLR_REG_SYS_2 Register (Offset = 308h) [reset = 0h]

Enable Clear Register 2

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Table 14-20714. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2308h**

Figure 14-6845. INTD_CFG_ENABLE_CLR_REG_SYS_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED				ENABLE_SYS_EN_PCIE_PTM_CLR	ENABLE_SYS_EN_PCIE_LINK_STATE_CLR	ENABLE_SYS_EN_PCIE_HOT_RESET_CLR	ENABLE_SYS_EN_PCIE_ERROR_2_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

7	6	5	4	3	2	1	0
ENABLE_SYS_EN_PCIE_ERROR_1_CLR	ENABLE_SYS_EN_PCIE_ERROR_0_CLR	RESERVED					ENABLE_SYS_EN_PCIE_DPA_CLR
R/W1TC	R/W1TC	NONE					R/W1TC
0h	0h	0h					0h

Table 14-20716. INTD_CFG_ENABLE_CLR_REG_SYS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	ENABLE_SYS_EN_PCIE_PTM_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_ptm
10	ENABLE_SYS_EN_PCIE_LINK_STATE_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_link_state
9	ENABLE_SYS_EN_PCIE_HOT_RESET_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_hot_reset
8	ENABLE_SYS_EN_PCIE_ERROR_2_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_error_2
7	ENABLE_SYS_EN_PCIE_ERROR_1_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_error_1
6	ENABLE_SYS_EN_PCIE_ERROR_0_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_error_0
5:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SYS_EN_PCIE_DPA_CLR	R/W1TC	0h	Enable Clear for sys_en_pcie_dpa

14.9.2.2.2.478 INTD_CFG_STATUS_REG_SYS_0 Register

1 INTD_CFG_STATUS_REG_SYS_0 Register (Offset = 500h) [reset = 0h]

Status Register 0

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Table 14-20717. Instance Table

Instance Name	**Physical Address**
PCIE0	**0F10 2500h**

Figure 14-6846. INTD_CFG_STATUS_REG_SYS_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							STATUS_SYS_PCIE_DOWNSTREAM
NONE							R
0h							0h

Table 14-20719. INTD_CFG_STATUS_REG_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	STATUS_SYS_PCIE_DOWNSTREAM	R	0h	Status for sys_en_pcie_downstream

14.9.2.2.2.479 INTD_CFG_STATUS_REG_SYS_1 Register

1 INTD_CFG_STATUS_REG_SYS_1 Register (Offset = 504h) [reset = 0h]

Status Register 1

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Table 14-20720. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2504h**

Figure 14-6847. INTD_CFG_STATUS_REG_SYS_1 Name Register

31	30	29	28	27	26	25	24
RESERVED					STATUS_SYS_PCIE_PWR_STATE	STATUS_SYS_PCIE_LEGACY_3	STATUS_SYS_PCIE_LEGACY_2
NONE					R	R	R
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STATUS_SYS_PCIE_LEGACY_1	STATUS_SYS_PCIE_LEGACY_0	RESERVED					
R	R	NONE					
0h	0h	0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							STATUS_SYS_PCIE_FLR
NONE							R
0h							0h

Table 14-20722. INTD_CFG_STATUS_REG_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	STATUS_SYS_PCIE_PWR_STATE	R	0h	Status for sys_en_pcie_pwr_state
25	STATUS_SYS_PCIE_LEGACY_3	R	0h	Status for sys_en_pcie_legacy_3
24	STATUS_SYS_PCIE_LEGACY_2	R	0h	Status for sys_en_pcie_legacy_2
23	STATUS_SYS_PCIE_LEGACY_1	R	0h	Status for sys_en_pcie_legacy_1
22	STATUS_SYS_PCIE_LEGACY_0	R	0h	Status for sys_en_pcie_legacy_0
21:1	RESERVED	NONE	0h	Reserved
0	STATUS_SYS_PCIE_FLR	R	0h	Status for sys_en_pcie_flr

14.9.2.2.2.480 INTD_CFG_STATUS_REG_SYS_2 Register

1 INTD_CFG_STATUS_REG_SYS_2 Register (Offset = 508h) [reset = 0h]

Status Register 2

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Table 14-20723. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2508h**

Figure 14-6848. INTD_CFG_STATUS_REG_SYS_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				STATUS_SYS_PCIE_PTM	STATUS_SYS_PCIE_LINK_STATE	STATUS_SYS_PCIE_HOT_RESET	STATUS_SYS_PCIE_ERROR_2
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
STATUS_SYS_PCIE_ERROR_1	STATUS_SYS_PCIE_ERROR_0	RESERVED					STATUS_SYS_PCIE_DPA
R/W1TS	R/W1TS	NONE					R/W1TS
0h	0h	0h					0h

Table 14-20725. INTD_CFG_STATUS_REG_SYS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	STATUS_SYS_PCIE_PTM	R/W1TS	0h	Status ,write 1 to set, for sys_en_pcie_ptm
10	STATUS_SYS_PCIE_LINK_STATE	R/W1TS	0h	Status ,write 1 to set, for sys_en_pcie_link_state
9	STATUS_SYS_PCIE_HOT_RESET	R/W1TS	0h	Status ,write 1 to set, for sys_en_pcie_hot_reset
8	STATUS_SYS_PCIE_ERROR_2	R/W1TS	0h	Status ,write 1 to set, for sys_en_pcie_error_2
7	STATUS_SYS_PCIE_ERROR_1	R/W1TS	0h	Status ,write 1 to set, for sys_en_pcie_error_1
6	STATUS_SYS_PCIE_ERROR_0	R/W1TS	0h	Status ,write 1 to set, for sys_en_pcie_error_0
5:1	RESERVED	NONE	0h	Reserved
0	STATUS_SYS_PCIE_DPA	R/W1TS	0h	Status ,write 1 to set, for sys_en_pcie_dpa

14.9.2.2.2.481 INTD_CFG_STATUS_CLR_REG_SYS_2 Register

1 INTD_CFG_STATUS_CLR_REG_SYS_2 Register (Offset = 708h) [reset = 0h]

Status Clear Register 2

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Table 14-20726. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2708h**

Figure 14-6849. INTD_CFG_STATUS_CLR_REG_SYS_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				STATUS_SYS_PCIE_PTM_CLR	STATUS_SYS_PCIE_LINK_STATE_CLR	STATUS_SYS_PCIE_HOT_RESET_CLR	STATUS_SYS_PCIE_ERROR_2_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
STATUS_SYS_PCIE_ERROR_1_CLR	STATUS_SYS_PCIE_ERROR_0_CLR	RESERVED					STATUS_SYS_PCIE_DPA_CLR
R/W1TC	R/W1TC	NONE					R/W1TC
0h	0h	0h					0h

Table 14-20728. INTD_CFG_STATUS_CLR_REG_SYS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	STATUS_SYS_PCIE_PTM_CLR	R/W1TC	0h	Status ,write 1 to clear, for sys_en_pcie_ptm
10	STATUS_SYS_PCIE_LINK_STATE_CLR	R/W1TC	0h	Status ,write 1 to clear, for sys_en_pcie_link_state
9	STATUS_SYS_PCIE_HOT_RESET_CLR	R/W1TC	0h	Status ,write 1 to clear, for sys_en_pcie_hot_reset
8	STATUS_SYS_PCIE_ERROR_2_CLR	R/W1TC	0h	Status ,write 1 to clear, for sys_en_pcie_error_2
7	STATUS_SYS_PCIE_ERROR_1_CLR	R/W1TC	0h	Status ,write 1 to clear, for sys_en_pcie_error_1
6	STATUS_SYS_PCIE_ERROR_0_CLR	R/W1TC	0h	Status ,write 1 to clear, for sys_en_pcie_error_0
5:1	RESERVED	NONE	0h	Reserved
0	STATUS_SYS_PCIE_DPA_CLR	R/W1TC	0h	Status ,write 1 to clear, for sys_en_pcie_dpa

14.9.2.2.2.482 INTD_CFG_INTR_VECTOR_REG_SYS Register

1 INTD_CFG_INTR_VECTOR_REG_SYS Register (Offset = A80h) [reset = 0h]

Interrupt Vector for sys

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Table 14-20729. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 2A80h**

Figure 14-6850. INTD_CFG_INTR_VECTOR_REG_SYS Name Register

31	30	29	28	27	26	25	24
INTR_VECTOR_SYS							
R							
0h							
23	22	21	20	19	18	17	16
INTR_VECTOR_SYS							
R							
0h							
15	14	13	12	11	10	9	8
INTR_VECTOR_SYS							
R							
0h							
7	6	5	4	3	2	1	0
INTR_VECTOR_SYS							
R							
0h							

Table 14-20731. INTD_CFG_INTR_VECTOR_REG_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTR_VECTOR_SYS	R	0h	Interrupt Vector

14.9.2.2.2.483 CPTS_IDVER_REG Register

1 CPTS_IDVER_REG Register (Offset = 0h) [reset = 4E8A010Ch]

Identification and Version Register

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Table 14-20732. Instance Table

Instance Name	**Physical Address**
PCIE0	**0F10 3000h**

Figure 14-6851. CPTS_IDVER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4E8Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TX_IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4E8Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_VER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MINOR_VER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Ch</td></tr>
</table>

Table 14-20734. CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TX_IDENT	R	4E8Ah	Identification value
15:11	RTL_VER	R	0h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	Ch	Minor version value

14.9.2.2.2.484 CPTS_CONTROL_REG Register

1 CPTS_CONTROL_REG Register (Offset = 4h) [reset = 4h]

Time Sync Control Register

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Table 14-20735. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3004h**

Figure 14-6852. CPTS_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W				NONE			
0h				0h			

23	22	21	20	19	18	17	16
RESERVED						TS_GENF_CLR_EN	TS_RX_NO_EVENT
NONE						R/W	R/W
0h						0h	0h

15	14	13	12	11	10	9	8
HW8_TS_PUSH_EN	HW7_TS_PUSH_EN	HW6_TS_PUSH_EN	HW5_TS_PUSH_EN	HW4_TS_PUSH_EN	HW3_TS_PUSH_EN	HW2_TS_PUSH_EN	HW1_TS_PUSH_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
TS_PPM_DIR	TS_COMP_TOG	MODE	SEQUENCE_EN	TSTAMP_EN	TS_COMP_POLARITY	INT_TEST	CPTS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	0h

Table 14-20737. CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TS_SYNC_SEL	R/W	0h	TS_SYNC output timestamp counter bit select
27:18	RESERVED	NONE	0h	Reserved
17	TS_GENF_CLR_EN	R/W	0h	Enable for GENF clear when length is zero
16	TS_RX_NO_EVENT	R/W	0h	Receive Produces no Events
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable
7	TS_PPM_DIR	R/W	0h	Timestamp PPM Direction
6	TS_COMP_TOG	R/W	0h	Timestamp Compare Toggle mode: 0=TS_COMP is in non-toggle mode, 1=TS_COMP is in toggle mode
5	MODE	R/W	0h	Timestamp mode

Table 14-20737. CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEQUENCE_EN	R/W	0h	Sequence Enable
3	TSTAMP_EN	R/W	0h	Host Receive Timestamp Enable
2	TS_COMP_POLARITY	R/W	1h	TS_COMP polarity
1	INT_TEST	R/W	0h	Interrupt test
0	CPTS_EN	R/W	0h	Time sync enable

14.9.2.2.2.485 CPTS_RFTCLK_SEL_REG Register

1 CPTS_RFTCLK_SEL_REG Register (Offset = 8h) [reset = 0h]

RFTCLK Select Register

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Table 14-20738. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3008h**

Figure 14-6853. CPTS_RFTCLK_SEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RFTCLK_SEL				
NONE			R/W				
0h			0h				

Table 14-20740. CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	RFTCLK_SEL	R/W	0h	Reference clock select

14.9.2.2.2.486 CPTS_TS_PUSH_REG Register

1 CPTS_TS_PUSH_REG Register (Offset = Ch) [reset = 0h]

Time Stamp Event Push Register

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Table 14-20741. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 300Ch**

Figure 14-6854. CPTS_TS_PUSH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
NONE							W
0h							0h

Table 14-20743. CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PUSH	W	0h	Time stamp event push

14.9.2.2.2.487 CPTS_TS_LOAD_VAL_REG Register

1 CPTS_TS_LOAD_VAL_REG Register (Offset = 10h) [reset = 0h]

Time Stamp Load Low Value Register

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Table 14-20744. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3010h**

Figure 14-6855. CPTS_TS_LOAD_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 14-20746. CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time stamp load low value

14.9.2.2.2.488 CPTS_TS_LOAD_EN_REG Register

1 CPTS_TS_LOAD_EN_REG Register (Offset = 14h) [reset = 0h]

Time Stamp Load Enable Register

Return to Summary Table

Table 14-20747. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3014h**

Figure 14-6856. CPTS_TS_LOAD_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
NONE							W
0h							0h

Table 14-20749. CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_LOAD_EN	W	0h	Time stamp load enable

14.9.2.2.2.489 CPTS_TS_COMP_VAL_REG Register

1 CPTS_TS_COMP_VAL_REG Register (Offset = 18h) [reset = 0h]

Time Stamp Comparison Low Value Register

Return to Summary Table

Table 14-20750. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3018h**

Figure 14-6857. CPTS_TS_COMP_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_VAL							
R/W							
0h							

Table 14-20752. CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_VAL	R/W	0h	Time stamp comparison low value

14.9.2.2.2.490 CPTS_TS_COMP_LEN_REG Register

1 CPTS_TS_COMP_LEN_REG Register (Offset = 1Ch) [reset = 0h]

Time Stamp Comparison Length Register

Return to Summary Table

Table 14-20753. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 301Ch**

Figure 14-6858. CPTS_TS_COMP_LEN_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_LENGTH							
R/W							
0h							

Table 14-20755. CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_LENGTH	R/W	0h	Time stamp comparison length

14.9.2.2.2.491 CPTS_INTSTAT_RAW_REG Register

1 CPTS_INTSTAT_RAW_REG Register (Offset = 20h) [reset = 0h]

Interrupt Status Register Raw

Return to Summary Table

Table 14-20756. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3020h**

Figure 14-6859. CPTS_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_RAW
NONE							R/W
0h							0h

Table 14-20758. CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable)

14.9.2.2.2.492 CPTS_INTSTAT_MASKED_REG Register

1 CPTS_INTSTAT_MASKED_REG Register (Offset = 24h) [reset = 0h]

Interrupt Status Register Masked

Return to Summary Table

Table 14-20759. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3024h**

Figure 14-6860. CPTS_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND
NONE							R
0h							0h

Table 14-20761. CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

14.9.2.2.2.493 CPTS_INT_ENABLE_REG Register

1 CPTS_INT_ENABLE_REG Register (Offset = 28h) [reset = 0h]

Interrupt Enable Register

Return to Summary Table

Table 14-20762. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3028h**

Figure 14-6861. CPTS_INT_ENABLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
NONE							R/W
0h							0h

Table 14-20764. CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

14.9.2.2.2.494 CPTS_TS_COMP_NUDGE_REG Register

1 CPTS_TS_COMP_NUDGE_REG Register (Offset = 2Ch) [reset = 0h]

Time Stamp Comparison Nudge Register

Return to Summary Table

Table 14-20765. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 302Ch**

Figure 14-6862. CPTS_TS_COMP_NUDGE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-20767. CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	This 2s complement number is added to the ts_comp_length value to increase or decrease the TS_COMP length by the nudge amount

14.9.2.2.2.495 CPTS_EVENT_POP_REG Register

1 CPTS_EVENT_POP_REG Register (Offset = 30h) [reset = 0h]

Event Pop Register

Return to Summary Table

Table 14-20768. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3030h**

Figure 14-6863. CPTS_EVENT_POP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
NONE							W
0h							0h

Table 14-20770. CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EVENT_POP	W	0h	Event pop

14.9.2.2.2.496 CPTS_EVENT_0_REG Register

1 CPTS_EVENT_0_REG Register (Offset = 34h) [reset = 0h]

Event 0 Register

Return to Summary Table

Table 14-20771. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3034h**

Figure 14-6864. CPTS_EVENT_0_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 14-20773. CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp

14.9.2.2.2.497 CPTS_EVENT_1_REG Register

1 CPTS_EVENT_1_REG Register (Offset = 38h) [reset = 0h]

Event 1 Register

Return to Summary Table

Table 14-20774. Instance Table

Instance Name	**Physical Address**
PCIE0	**0F10 3038h**

Figure 14-6865. CPTS_EVENT_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
NONE		R	R				
0h		0h	0h				
23	22	21	20	19	18	17	16
EVENT_TYPE				MESSAGE_TYPE			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
SEQUENCE_ID							
R							
0h							
7	6	5	4	3	2	1	0
SEQUENCE_ID							
R							
0h							

Table 14-20776. CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	PREMPT_QUEUE	R	0h	Prempt QUEUE
28:24	PORT_NUMBER	R	0h	Port number
23:20	EVENT_TYPE	R	0h	Event type
19:16	MESSAGE_TYPE	R	0h	Message type
15:0	SEQUENCE_ID	R	0h	Sequence ID

14.9.2.2.2.498 CPTS_EVENT_2_REG Register

1 CPTS_EVENT_2_REG Register (Offset = 3Ch) [reset = 0h]

Event 2 Register

Return to Summary Table

Table 14-20777. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 303Ch**

Figure 14-6866. CPTS_EVENT_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DOMAIN							
R							
0h							

Table 14-20779. CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DOMAIN	R	0h	Domain

14.9.2.2.2.499 CPTS_EVENT_3_REG Register

1 CPTS_EVENT_3_REG Register (Offset = 40h) [reset = 0h]

Event 3 Register

Return to Summary Table

Table 14-20780. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3040h**

Figure 14-6867. CPTS_EVENT_3_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 14-20782. CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp

14.9.2.2.2.500 CPTS_TS_LOAD_HIGH_VAL_REG Register

1 CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 44h) [reset = 0h]

Time Stamp Load High Value Register

Return to Summary Table

Table 14-20783. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3044h**

Figure 14-6868. CPTS_TS_LOAD_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 14-20785. CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time stamp load high value

14.9.2.2.2.501 CPTS_TS_COMP_HIGH_VAL_REG Register

1 CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 48h) [reset = 0h]

Time Stamp Comparison High Value Register

Return to Summary Table

Table 14-20786. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3048h**

Figure 14-6869. CPTS_TS_COMP_HIGH_VAL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TS_COMP_HIGH_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TS_COMP_HIGH_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TS_COMP_HIGH_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TS_COMP_HIGH_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20788. CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_HIGH_VAL	R/W	0h	Time stamp comparison high value

14.9.2.2.2.502 CPTS_TS_ADD_VAL_REG Register

1 CPTS_TS_ADD_VAL_REG Register (Offset = 4Ch) [reset = 0h]

TS Add Value Register

Return to Summary Table

Table 14-20789. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 304Ch**

Figure 14-6870. CPTS_TS_ADD_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADD_VAL		
NONE					R/W		
0h					0h		

Table 14-20791. CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADD_VAL	R/W	0h	Add Value

14.9.2.2.2.503 CPTS_TS_PPM_LOW_VAL_REG Register

1 CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 50h) [reset = 0h]

Time Stamp PPM Low Value Register

Return to Summary Table

Table 14-20792. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3050h**

Figure 14-6871. CPTS_TS_PPM_LOW_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_PPM_LOW_VAL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_PPM_LOW_VAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_PPM_LOW_VAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_PPM_LOW_VAL							
R/W							
0h							

Table 14-20794. CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_PPM_LOW_VAL	R/W	0h	Time stamp PPM Low value

14.9.2.2.2.504 CPTS_TS_PPM_HIGH_VAL_REG Register

1 CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 54h) [reset = 0h]

Time Stamp PPM High Value Register

Return to Summary Table

Table 14-20795. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3054h**

Figure 14-6872. CPTS_TS_PPM_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TS_PPM_HIGH_VAL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_PPM_HIGH_VAL							
R/W							
0h							

Table 14-20797. CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TS_PPM_HIGH_VAL	R/W	0h	Time stamp PPM High value

14.9.2.2.2.505 CPTS_TS_NUDGE_VAL_REG Register

1 CPTS_TS_NUDGE_VAL_REG Register (Offset = 58h) [reset = 0h]

Time Stamp Nudge Value Register

Return to Summary Table

Table 14-20798. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3058h**

Figure 14-6873. CPTS_TS_NUDGE_VAL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TS_NUDGE_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20800. CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge value

14.9.2.2.2.506 CPTS_TS_CONFIG Register

1 CPTS_TS_CONFIG Register (Offset = D0h) [reset = 2001h]

Time Stamp Configuration Read

Return to Summary Table

Table 14-20801. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 30D0h**

Figure 14-6874. CPTS_TS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EVNT_FIFO_DEPTH							
R							
20h							
7	6	5	4	3	2	1	0
NUM_GENF							
R							
1h							

Table 14-20803. CPTS_TS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	EVNT_FIFO_DEPTH	R	20h	The Event FIFO Depth
7:0	NUM_GENF	R	1h	The number of CPTS GENF outputs

14.9.2.2.2.507 CPTS_TS_GENF_COMP_LOW_REG Register

1 CPTS_TS_GENF_COMP_LOW_REG Register (Offset = 0h) [reset = 0h]

Time Stamp Generate Function Comparison Low Value

Return to Summary Table

Table 14-20804. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3000h**

Figure 14-6875. CPTS_TS_GENF_COMP_LOW_REG Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 14-20806. CPTS_TS_GENF_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value

14.9.2.2.2.508 CPTS_TS_GENF_COMP_HIGH_REG Register

1 CPTS_TS_GENF_COMP_HIGH_REG Register (Offset = 4h) [reset = 0h]

Time Stamp Generate Function Comparison high Value

Return to Summary Table

Table 14-20807. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3004h**

Figure 14-6876. CPTS_TS_GENF_COMP_HIGH_REG Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 14-20809. CPTS_TS_GENF_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value

14.9.2.2.2.509 CPTS_TS_GENF_CONTROL_REG Register

1 CPTS_TS_GENF_CONTROL_REG Register (Offset = 8h) [reset = 0h]

Time Stamp Generate Function Control

Return to Summary Table

Table 14-20810. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3008h**

Figure 14-6877. CPTS_TS_GENF_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
NONE						R/W	R/W
0h						0h	0h

Table 14-20812. CPTS_TS_GENF_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert
0	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction

14.9.2.2.2.510 CPTS_TS_GENF_LENGTH_REG Register

1 CPTS_TS_GENF_LENGTH_REG Register (Offset = Ch) [reset = 0h]

Time Stamp Generate Function Length Value

Return to Summary Table

Table 14-20813. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 300Ch**

Figure 14-6878. CPTS_TS_GENF_LENGTH_REG Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 14-20815. CPTS_TS_GENF_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value

14.9.2.2.2.511 CPTS_TS_GENF_PPM_LOW_REG Register

1 CPTS_TS_GENF_PPM_LOW_REG Register (Offset = 10h) [reset = 0h]

Time Stamp Generate Function PPM Low Value

Return to Summary Table

Table 14-20816. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3010h**

Figure 14-6879. CPTS_TS_GENF_PPM_LOW_REG Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 14-20818. CPTS_TS_GENF_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp Generate Function PPM Low Value

14.9.2.2.2.512 CPTS_TS_GENF_PPM_HIGH_REG Register

1 CPTS_TS_GENF_PPM_HIGH_REG Register (Offset = 14h) [reset = 0h]

Time Stamp Generate Function PPM High Value

Return to Summary Table

Table 14-20819. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3014h**

Figure 14-6880. CPTS_TS_GENF_PPM_HIGH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PPM_HIGH	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PPM_HIGH							
R/W							
0h							

Table 14-20821. CPTS_TS_GENF_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value

14.9.2.2.2.513 CPTS_TS_GENF_NUDGE_REG Register

1 CPTS_TS_GENF_NUDGE_REG Register (Offset = 18h) [reset = 0h]

Time Stamp Generate Function Nudge Value

Return to Summary Table

Table 14-20822. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3018h**

Figure 14-6881. CPTS_TS_GENF_NUDGE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-20824. CPTS_TS_GENF_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value

14.9.2.2.2.514 CPTS_TS_ESTF_COMP_LOW_REG Register

1 CPTS_TS_ESTF_COMP_LOW_REG Register (Offset = 0h) [reset = 0h]

Time Stamp ESTF Generate Function Comparison Low Value

Return to Summary Table

Table 14-20825. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3000h**

Figure 14-6882. CPTS_TS_ESTF_COMP_LOW_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COMP_LOW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COMP_LOW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COMP_LOW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP_LOW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-20827. CPTS_TS_ESTF_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	Time Stamp ESTF Generate Function Comparison Low Value

14.9.2.2.2.515 CPTS_TS_ESTF_COMP_HIGH_REG Register

1 CPTS_TS_ESTF_COMP_HIGH_REG Register (Offset = 4h) [reset = 0h]

Time Stamp ESTF Generate Function Comparison high Value

Return to Summary Table

Table 14-20828. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3004h**

Figure 14-6883. CPTS_TS_ESTF_COMP_HIGH_REG Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 14-20830. CPTS_TS_ESTF_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	Time Stamp ESTF Generate Function Comparison High Value

14.9.2.2.2.516 CPTS_TS_ESTF_CONTROL_REG Register

1 CPTS_TS_ESTF_CONTROL_REG Register (Offset = 8h) [reset = 0h]

Time Stamp ESTF Generate Function Control

Return to Summary Table

Table 14-20831. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3008h**

Figure 14-6884. CPTS_TS_ESTF_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>POLARITY_INV</td><td>PPM_DIR</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-20833. CPTS_TS_ESTF_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	POLARITY_INV	R/W	0h	Time Stamp ESTF Generate Function Polarity Invert
0	PPM_DIR	R/W	0h	Time Stamp ESTF Generate Function PPM Direction

14.9.2.2.2.517 CPTS_TS_ESTF_LENGTH_REG Register

1 CPTS_TS_ESTF_LENGTH_REG Register (Offset = Ch) [reset = 0h]

Time Stamp ESTF Generate Function Length Value

Return to Summary Table

Table 14-20834. Instance Table

Instance Name	Physical Address
PCIE0	0F10 300Ch

Figure 14-6885. CPTS_TS_ESTF_LENGTH_REG Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 14-20836. CPTS_TS_ESTF_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp ESTF Generate Function Length Value

14.9.2.2.2.518 CPTS_TS_ESTF_PPM_LOW_REG Register

1 CPTS_TS_ESTF_PPM_LOW_REG Register (Offset = 10h) [reset = 0h]

Time Stamp ESTF Generate Function PPM Low Value

Return to Summary Table

Table 14-20837. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3010h**

Figure 14-6886. CPTS_TS_ESTF_PPM_LOW_REG Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 14-20839. CPTS_TS_ESTF_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp ESTF Generate Function PPM Low Value

14.9.2.2.2.519 CPTS_TS_ESTF_PPM_HIGH_REG Register

1 CPTS_TS_ESTF_PPM_HIGH_REG Register (Offset = 14h) [reset = 0h]

Time Stamp ESTF Generate Function PPM High Value

Return to Summary Table

Table 14-20840. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3014h**

Figure 14-6887. CPTS_TS_ESTF_PPM_HIGH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PPM_HIGH	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PPM_HIGH							
R/W							
0h							

Table 14-20842. CPTS_TS_ESTF_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp ESTF Generate Function PPM High Value

14.9.2.2.2.520 CPTS_TS_ESTF_NUDGE_REG Register

1 CPTS_TS_ESTF_NUDGE_REG Register (Offset = 18h) [reset = 0h]

Time Stamp ESTF Generate Function Nudge Value

Return to Summary Table

Table 14-20843. Instance Table

Instance Name	Physical Address
PCIE0	**0F10 3018h**

Figure 14-6888. CPTS_TS_ESTF_NUDGE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUDGE							
R/W							
0h							

Table 14-20845. CPTS_TS_ESTF_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time Stamp ESTF Generate Function Nudge Value

14.9.2.2.2.521 PCIE_DAT0_PCIE_DATA_MEM_j Register

1 PCIE_DAT0_PCIE_DATA_MEM_j Register (Offset = 0h + formula) [reset = 0h]

PCIE data region0

Return to Summary Table

Offset = (j * 4h); where j = 0 to 67108863d

Table 14-20846. Instance Table

Instance Name	Physical Address
PCIE0	**6800 0000h + formula**

Figure 14-6889. PCIE_DAT0_PCIE_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
PCIE_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PCIE_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PCIE_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PCIE_DATA							
R/W							
0h							

Table 14-20848. PCIE_DAT0_PCIE_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCIE_DATA	R/W	0h	PCIE data region0 Reset Source: cba_mod_g_rst_n

14.9.2.2.2.522 PCIE_DAT1_PCIE_DATA_MEM_j Register

1 PCIE_DAT1_PCIE_DATA_MEM_j Register (Offset = 0h + formula) [reset = 0h]

PCIE data region1

Return to Summary Table

Offset = (j * 4h); where j = 0 to 67108863d

Table 14-20849. Instance Table

Instance Name	Physical Address
PCIE0	**0006 0000 0000h + formula**

Figure 14-6890. PCIE_DAT1_PCIE_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
PCIE_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PCIE_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PCIE_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PCIE_DATA							
R/W							
0h							

Table 14-20851. PCIE_DAT1_PCIE_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCIE_DATA	R/W	0h	PCIE data region1 Reset Source: cba_mod_g_rst_n

14.9.2.3 USB

USB

14.9.2.3.1 USB Summaries

USB Summaries

Table 14-20852. ECC_AGGR Registers, Base Address=0070 3000h, Length=1024

Offset	Length	Register Name	USB0 Physical Address
0h	32	ECC_AGGR_REV	0070 3000h
8h	32	ECC_AGGR_VECTOR	0070 3008h
Ch	32	ECC_AGGR_STAT	0070 300Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0070 3010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0070 303Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0070 3040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0070 3080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0070 30C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0070 313Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0070 3140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0070 3180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0070 31C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0070 3200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0070 3204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0070 3208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0070 320Ch

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB3P0SS_CTRL_DRD_CDNS_DID	0F40 0000h
4h	32	USB3P0SS_CTRL_DRD_CDNS_RID	0F40 0004h
8h	32	USB3P0SS_CTRL_DRD_OTGCAPABILITY	0F40 0008h
10h	32	USB3P0SS_CTRL_DRD_OTGCMD	0F40 0010h
14h	32	USB3P0SS_CTRL_DRD_OTGSTS	0F40 0014h
18h	32	USB3P0SS_CTRL_DRD_OTGSTATE	0F40 0018h
20h	32	USB3P0SS_CTRL_DRD_OTGIEN	0F40 0020h
24h	32	USB3P0SS_CTRL_DRD_OTGIVECT	0F40 0024h
28h	32	USB3P0SS_CTRL_DRD_CLK_FREQ	0F40 0028h
2Ch	32	USB3P0SS_CTRL_DRD_OTGTMR	0F40 002Ch
40h	32	USB3P0SS_CTRL_DRD_OTGSIMULATE	0F40 0040h
44h	32	USB3P0SS_CTRL_DRD_OVERRIDE	0F40 0044h
48h	32	USB3P0SS_CTRL_DRD_SUSP_CTRL	0F40 0048h
4Ch	32	USB3P0SS_CTRL_DRD_PHYRST_CFG	0F40 004Ch
50h	32	USB3P0SS_CTRL_DRD_OTGANASTS	0F40 0050h
54h	32	USB3P0SS_CTRL_DRD_ADP_RAMP_TIME	0F40 0054h
58h	32	USB3P0SS_CTRL_DRD_OTGCTRL1	0F40 0058h
5Ch	32	USB3P0SS_CTRL_DRD_OTGCTRL2	0F40 005Ch

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
60h	32	USB3P0SS_CTRL_DRD_VBUSVALID_DBNC_CFG	0F40 0060h
64h	32	USB3P0SS_CTRL_DRD_SESSVALID_DBNC_CFG	0F40 0064h
68h	32	USB3P0SS_CTRL_DRD_IDDIG_DBNC_CFG	0F40 0068h
8Ch	32	USB3P0SS_CTRL_DRD_DB_ASF_MEM_MASK	0F40 008Ch
0h	32	USB3P0SS_CTRL_ASF_ASF_INT_STATUS	0F40 0000h
4h	32	USB3P0SS_CTRL_ASF_ASF_INT_RAW_STATUS	0F40 0004h
8h	32	USB3P0SS_CTRL_ASF_ASF_INT_MASK	0F40 0008h
Ch	32	USB3P0SS_CTRL_ASF_ASF_INT_TEST	0F40 000Ch
10h	32	USB3P0SS_CTRL_ASF_ASF_FATAL_NONFATAL_SELECT	0F40 0010h
14h	32	USB3P0SS_CTRL_ASF_RSVD_6_ASF	0F40 0014h
18h	32	USB3P0SS_CTRL_ASF_RSVD_7_ASF	0F40 0018h
1Ch	32	USB3P0SS_CTRL_ASF_RSVD_8_ASF	0F40 001Ch
20h	32	USB3P0SS_CTRL_ASF_ASF_SRAM_CORR_FAULT_STATUS	0F40 0020h
24h	32	USB3P0SS_CTRL_ASF_ASF_SRAM_UNCORR_FAULT_STATUS	0F40 0024h
28h	32	USB3P0SS_CTRL_ASF_ASF_SRAM_FAULT_STATS	0F40 0028h
2Ch	32	USB3P0SS_CTRL_ASF_RSVD_12_ASF	0F40 002Ch
30h	32	USB3P0SS_CTRL_ASF_ASF_TRANS_TO_CTRL	0F40 0030h
34h	32	USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_MASK	0F40 0034h
38h	32	USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_STATUS	0F40 0038h
3Ch	32	USB3P0SS_CTRL_ASF_RSVD_16_ASF	0F40 003Ch
40h	32	USB3P0SS_CTRL_ASF_RSVD_17_ASF	0F40 0040h
44h	32	USB3P0SS_CTRL_ASF_RSVD_18_ASF	0F40 0044h
0h	32	USB3P0SS_CTRL_XHCI_HCIVERSION_CAPLENGTH	0F40 0000h
4h	32	USB3P0SS_CTRL_XHCI_HCSPARAMS1	0F40 0004h
8h	32	USB3P0SS_CTRL_XHCI_HCSPARAMS2	0F40 0008h
Ch	32	USB3P0SS_CTRL_XHCI_HCSPARAMS3	0F40 000Ch
10h	32	USB3P0SS_CTRL_XHCI_HCCPARAMS	0F40 0010h
14h	32	USB3P0SS_CTRL_XHCI_DBOFF	0F40 0014h
18h	32	USB3P0SS_CTRL_XHCI_RTSOFF	0F40 0018h
1Ch	32	USB3P0SS_CTRL_XHCI_HCCPARAMS2	0F40 001Ch
20h	32	USB3P0SS_CTRL_XHCI_RSVD_CR_J	0F40 0020h + formula
80h	32	USB3P0SS_CTRL_XHCI_USBCMD	0F40 0080h
84h	32	USB3P0SS_CTRL_XHCI_USBSTS	0F40 0084h
88h	32	USB3P0SS_CTRL_XHCI_PAGESIZE	0F40 0088h
8Ch	32	USB3P0SS_CTRL_XHCI_RSVDZ8C	0F40 008Ch
90h	32	USB3P0SS_CTRL_XHCI_RSVDZ90	0F40 0090h
94h	32	USB3P0SS_CTRL_XHCI_DNCTRL	0F40 0094h
98h	32	USB3P0SS_CTRL_XHCI_CRCR_LO	0F40 0098h
9Ch	32	USB3P0SS_CTRL_XHCI_CRCR_HI	0F40 009Ch
A0h	32	USB3P0SS_CTRL_XHCI_RSVDZA0	0F40 00A0h
A4h	32	USB3P0SS_CTRL_XHCI_RSVDZA4	0F40 00A4h
A8h	32	USB3P0SS_CTRL_XHCI_RSVDZA8	0F40 00A8h

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
ACh	32	USB3P0SS_CTRL_XHCI_RSVDZAC	0F40 00ACh
B0h	32	USB3P0SS_CTRL_XHCI_DCBAAP_LO	0F40 00B0h
B4h	32	USB3P0SS_CTRL_XHCI_DCBAAP_HI	0F40 00B4h
B8h	32	USB3P0SS_CTRL_XHCI_CONFIG	0F40 00B8h
BCh	32	USB3P0SS_CTRL_XHCI_RSVDZBC	0F40 00BCh
C0h	32	USB3P0SS_CTRL_XHCI_RSVDZ_OP_J	0F40 00C0h + formula
480h	32	USB3P0SS_CTRL_XHCI_PORTSC1USB2	0F40 0480h
484h	32	USB3P0SS_CTRL_XHCI_PORTPMSC1USB2	0F40 0484h
488h	32	USB3P0SS_CTRL_XHCI_RSVDP1USB2	0F40 0488h
48Ch	32	USB3P0SS_CTRL_XHCI_PORT1HLPMC	0F40 048Ch
490h	32	USB3P0SS_CTRL_XHCI_PORTSC1USB3	0F40 0490h
494h	32	USB3P0SS_CTRL_XHCI_PORTPMSC1USB3	0F40 0494h
498h	32	USB3P0SS_CTRL_XHCI_PORTLI1	0F40 0498h
49Ch	32	USB3P0SS_CTRL_XHCI_RSVDP1USB3	0F40 049Ch
2000h	32	USB3P0SS_CTRL_XHCI_MFINDEX	0F40 2000h
2004h	32	USB3P0SS_CTRL_XHCI_RSVDZ_RT_J	0F40 2004h + formula
2020h	32	USB3P0SS_CTRL_XHCI_IMAN0	0F40 2020h
2024h	32	USB3P0SS_CTRL_XHCI_IMOD0	0F40 2024h
2028h	32	USB3P0SS_CTRL_XHCI_ERSTSZ0	0F40 2028h
202Ch	32	USB3P0SS_CTRL_XHCI_RESERVED0	0F40 202Ch
2030h	32	USB3P0SS_CTRL_XHCI_ERSTBA0_LO	0F40 2030h
2034h	32	USB3P0SS_CTRL_XHCI_ERSTBA0_HI	0F40 2034h
2038h	32	USB3P0SS_CTRL_XHCI_ERDP0_LO	0F40 2038h
203Ch	32	USB3P0SS_CTRL_XHCI_ERDP0_HI	0F40 203Ch
2040h	32	USB3P0SS_CTRL_XHCI_IMAN1	0F40 2040h
2044h	32	USB3P0SS_CTRL_XHCI_IMOD1	0F40 2044h
2048h	32	USB3P0SS_CTRL_XHCI_ERSTSZ1	0F40 2048h
204Ch	32	USB3P0SS_CTRL_XHCI_RESERVED1	0F40 204Ch
2050h	32	USB3P0SS_CTRL_XHCI_ERSTBA1_LO	0F40 2050h
2054h	32	USB3P0SS_CTRL_XHCI_ERSTBA1_HI	0F40 2054h
2058h	32	USB3P0SS_CTRL_XHCI_ERDP1_LO	0F40 2058h
205Ch	32	USB3P0SS_CTRL_XHCI_ERDP1_HI	0F40 205Ch
2060h	32	USB3P0SS_CTRL_XHCI_IMAN2	0F40 2060h
2064h	32	USB3P0SS_CTRL_XHCI_IMOD2	0F40 2064h
2068h	32	USB3P0SS_CTRL_XHCI_ERSTSZ2	0F40 2068h
206Ch	32	USB3P0SS_CTRL_XHCI_RESERVED2	0F40 206Ch
2070h	32	USB3P0SS_CTRL_XHCI_ERSTBA2_LO	0F40 2070h
2074h	32	USB3P0SS_CTRL_XHCI_ERSTBA2_HI	0F40 2074h
2078h	32	USB3P0SS_CTRL_XHCI_ERDP2_LO	0F40 2078h
207Ch	32	USB3P0SS_CTRL_XHCI_ERDP2_HI	0F40 207Ch
2080h	32	USB3P0SS_CTRL_XHCI_IMAN3	0F40 2080h
2084h	32	USB3P0SS_CTRL_XHCI_IMOD3	0F40 2084h
2088h	32	USB3P0SS_CTRL_XHCI_ERSTSZ3	0F40 2088h
208Ch	32	USB3P0SS_CTRL_XHCI_RESERVED3	0F40 208Ch
2090h	32	USB3P0SS_CTRL_XHCI_ERSTBA3_LO	0F40 2090h

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
2094h	32	USB3P0SS_CTRL_XHCI_ERSTBA3_HI	0F40 2094h
2098h	32	USB3P0SS_CTRL_XHCI_ERDP3_LO	0F40 2098h
209Ch	32	USB3P0SS_CTRL_XHCI_ERDP3_HI	0F40 209Ch
20A0h	32	USB3P0SS_CTRL_XHCI_IMAN4	0F40 20A0h
20A4h	32	USB3P0SS_CTRL_XHCI_IMOD4	0F40 20A4h
20A8h	32	USB3P0SS_CTRL_XHCI_ERSTSZ4	0F40 20A8h
20ACh	32	USB3P0SS_CTRL_XHCI_RESERVED4	0F40 20ACh
20B0h	32	USB3P0SS_CTRL_XHCI_ERSTBA4_LO	0F40 20B0h
20B4h	32	USB3P0SS_CTRL_XHCI_ERSTBA4_HI	0F40 20B4h
20B8h	32	USB3P0SS_CTRL_XHCI_ERDP4_LO	0F40 20B8h
20BCh	32	USB3P0SS_CTRL_XHCI_ERDP4_HI	0F40 20BCh
20C0h	32	USB3P0SS_CTRL_XHCI_IMAN5	0F40 20C0h
20C4h	32	USB3P0SS_CTRL_XHCI_IMOD5	0F40 20C4h
20C8h	32	USB3P0SS_CTRL_XHCI_ERSTSZ5	0F40 20C8h
20CCh	32	USB3P0SS_CTRL_XHCI_RESERVED5	0F40 20CCh
20D0h	32	USB3P0SS_CTRL_XHCI_ERSTBA5_LO	0F40 20D0h
20D4h	32	USB3P0SS_CTRL_XHCI_ERSTBA5_HI	0F40 20D4h
20D8h	32	USB3P0SS_CTRL_XHCI_ERDP5_LO	0F40 20D8h
20DCh	32	USB3P0SS_CTRL_XHCI_ERDP5_HI	0F40 20DCh
20E0h	32	USB3P0SS_CTRL_XHCI_IMAN6	0F40 20E0h
20E4h	32	USB3P0SS_CTRL_XHCI_IMOD6	0F40 20E4h
20E8h	32	USB3P0SS_CTRL_XHCI_ERSTSZ6	0F40 20E8h
20ECh	32	USB3P0SS_CTRL_XHCI_RESERVED6	0F40 20ECh
20F0h	32	USB3P0SS_CTRL_XHCI_ERSTBA6_LO	0F40 20F0h
20F4h	32	USB3P0SS_CTRL_XHCI_ERSTBA6_HI	0F40 20F4h
20F8h	32	USB3P0SS_CTRL_XHCI_ERDP6_LO	0F40 20F8h
20FCh	32	USB3P0SS_CTRL_XHCI_ERDP6_HI	0F40 20FCh
2100h	32	USB3P0SS_CTRL_XHCI_IMAN7	0F40 2100h
2104h	32	USB3P0SS_CTRL_XHCI_IMOD7	0F40 2104h
2108h	32	USB3P0SS_CTRL_XHCI_ERSTSZ7	0F40 2108h
210Ch	32	USB3P0SS_CTRL_XHCI_RESERVED7	0F40 210Ch
2110h	32	USB3P0SS_CTRL_XHCI_ERSTBA7_LO	0F40 2110h
2114h	32	USB3P0SS_CTRL_XHCI_ERSTBA7_HI	0F40 2114h
2118h	32	USB3P0SS_CTRL_XHCI_ERDP7_LO	0F40 2118h
211Ch	32	USB3P0SS_CTRL_XHCI_ERDP7_HI	0F40 211Ch
3000h	32	USB3P0SS_CTRL_XHCI_DB0	0F40 3000h
3004h	32	USB3P0SS_CTRL_XHCI_DB_J	0F40 3004h + formula
8000h	32	USB3P0SS_CTRL_XHCI_XECP_PORT_CAP_REG	0F40 8000h
8004h	32	USB3P0SS_CTRL_XHCI_XECP_PORT_1_REG	0F40 8004h
8008h	32	USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CAP	0F40 8008h
800Ch	32	USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CTRL	0F40 800Ch
8010h	32	USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_STATUS	0F40 8010h
8014h	32	USB3P0SS_CTRL_XHCI_XECP_PM_CAP	0F40 8014h

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
8018h	32	USB3P0SS_CTRL_XHCI_XECP_PM_PMCSR	0F40 8018h
801Ch	32	USB3P0SS_CTRL_XHCI_XECP_MSI_CAP	0F40 801Ch
8020h	32	USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_L	0F40 8020h
8024h	32	USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_H	0F40 8024h
8028h	32	USB3P0SS_CTRL_XHCI_XECP_MSI_DATA	0F40 8028h
802Ch	32	USB3P0SS_CTRL_XHCI_XECP_AXI_CAP	0F40 802Ch
8030h	32	USB3P0SS_CTRL_XHCI_XECP_AXI_CFG0	0F40 8030h
8034h	32	USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL0	0F40 8034h
8038h	32	USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL1	0F40 8038h
803Ch	32	USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL2	0F40 803Ch
8040h	32	USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP0	0F40 8040h
8044h	32	USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP1	0F40 8044h
8048h	32	USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP2	0F40 8048h
804Ch	32	USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_PROTOCOL_SLOT_TYPE	0F40 804Ch
8050h	32	USB3P0SS_CTRL_XHCI_XECP_PSI_FULL_SPEED	0F40 8050h
8054h	32	USB3P0SS_CTRL_XHCI_XECP_PSI_LOW_SPEED	0F40 8054h
8058h	32	USB3P0SS_CTRL_XHCI_XECP_PSI_HIGH_SPEED	0F40 8058h
8060h	32	USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP0	0F40 8060h
8064h	32	USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP1	0F40 8064h
8068h	32	USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP2	0F40 8068h
806Ch	32	USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_PROTOCOL_SLOT_TYPE	0F40 806Ch
8070h	32	USB3P0SS_CTRL_XHCI_PSI_SUPER_SPEED	0F40 8070h
8080h	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_STS0	0F40 8080h
8084h	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_1	0F40 8084h
8088h	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_2	0F40 8088h
808Ch	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_3	0F40 808Ch
8090h	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_4	0F40 8090h
8094h	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_5	0F40 8094h
8098h	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG1	0F40 8098h
809Ch	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG2	0F40 809Ch
80A0h	32	USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG3	0F40 80A0h
80B0h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_CAP	0F40 80B0h
80B4h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_RSVD	0F40 80B4h
80B8h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_MASK_REG	0F40 80B8h
80BCh	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_IN_EP_VALID_REG	0F40 80BCh
80C0h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_PMASK_REG	0F40 80C0h
80C4h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_OCRD_REG	0F40 80C4h
80C8h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_LO	0F40 80C8h
80CCh	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_HI	0F40 80CCh

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
80D0h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1	0F40 80D0h
80D4h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG1	0F40 80D4h
80D8h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_ODMA_REG	0F40 80D8h
80DCh	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_IDMA_REG	0F40 80DCh
80E0h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_CTRL	0F40 80E0h
8100h	32	USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG	0F40 8100h
8104h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SS_REG	0F40 8104h
8108h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_HS_REG	0F40 8108h
810Ch	32	USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_FS_LS_REG	0F40 810Ch
8110h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SYS_REG	0F40 8110h
8114h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_ASYNC_DELAY_REG	0F40 8114h
8118h	32	USB3P0SS_CTRL_XHCI_XECP_UPORTS_PON_RST_REG	0F40 8118h
811Ch	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG3	0F40 811Ch
8120h	32	USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG1	0F40 8120h
8128h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_WATERMARK_REG	0F40 8128h
812Ch	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG	0F40 812Ch
8130h	32	USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG1	0F40 8130h
8134h	32	USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG2	0F40 8134h
8138h	32	USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG3	0F40 8138h
813Ch	32	USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG4	0F40 813Ch
8140h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_CTRL_REG	0F40 8140h
8144h	32	USB3P0SS_CTRL_XHCI_XECP_FPGA_REVISION_REG	0F40 8144h
8148h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_INTF_CTRL_REG	0F40 8148h
814Ch	32	USB3P0SS_CTRL_XHCI_XECP_BW_OV_SS_BURST_REG	0F40 814Ch
8150h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2	0F40 8150h
8168h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX1_REG	0F40 8168h
816Ch	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX2_REG	0F40 816Ch
8170h	32	USB3P0SS_CTRL_XHCI_XECP_USB2_LINESTATE_REG	0F40 8170h

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
8174h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER1_REG	0F40 8174h
8178h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER2_REG	0F40 8178h
817Ch	32	USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_BTO_TIMER_REG	0F40 817Ch
8180h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH_REG	0F40 8180h
8184h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH1_REG	0F40 8184h
8190h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG	0F40 8190h
8194h	32	USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG2	0F40 8194h
8198h	32	USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG3	0F40 8198h
819Ch	32	USB3P0SS_CTRL_XHCI_XECP_DEBUG_CTRL_REG	0F40 819Ch
81A0h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG2	0F40 81A0h
81A4h	32	USB3P0SS_CTRL_XHCI_XECP_AUX_DEBUG_READ_ONLY	0F40 81A4h
81A8h	32	USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_PORTNUM_REG	0F40 81A8h
81ACh	32	USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_DEV_REMOVE_REG	0F40 81ACh
81E0h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TTE_REG1	0F40 81E0h
81E4h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG1	0F40 81E4h
81E8h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG2	0F40 81E8h
8200h	32	USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_0	0F40 8200h
8204h	32	USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_1	0F40 8204h
8210h	32	USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG	0F40 8210h
8214h	32	USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG1	0F40 8214h
8218h	32	USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG2	0F40 8218h
821Ch	32	USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG3	0F40 821Ch
8220h	32	USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG1	0F40 8220h
8370h	32	USB3P0SS_CTRL_XHCI_XECP_USBLEGSUP	0F40 8370h
8374h	32	USB3P0SS_CTRL_XHCI_XECP_USBLEGCTLSTS	0F40 8374h
8800h	32	USB3P0SS_CTRL_XHCI_XECP_USB3_TEST_PORT0_REG	0F40 8800h
0h	32	USB3P0SS_CTRL_DEV_USB_CONF	0F40 0000h
4h	32	USB3P0SS_CTRL_DEV_USB_STS	0F40 0004h
8h	32	USB3P0SS_CTRL_DEV_USB_CMD	0F40 0008h
Ch	32	USB3P0SS_CTRL_DEV_USB_IPTN	0F40 000Ch
10h	32	USB3P0SS_CTRL_DEV_USB_LPM	0F40 0010h
14h	32	USB3P0SS_CTRL_DEV_USB_IEN	0F40 0014h
18h	32	USB3P0SS_CTRL_DEV_USB_ISTS	0F40 0018h

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
1Ch	32	USB3P0SS_CTRL_DEV_EP_SEL	0F40 001Ch
20h	32	USB3P0SS_CTRL_DEV_EP_TRADDR	0F40 0020h
24h	32	USB3P0SS_CTRL_DEV_EP_CFG	0F40 0024h
28h	32	USB3P0SS_CTRL_DEV_EP_CMD	0F40 0028h
2Ch	32	USB3P0SS_CTRL_DEV_EP_STS	0F40 002Ch
30h	32	USB3P0SS_CTRL_DEV_EP_STS_SID	0F40 0030h
34h	32	USB3P0SS_CTRL_DEV_EP_STS_EN	0F40 0034h
38h	32	USB3P0SS_CTRL_DEV_DRBL	0F40 0038h
3Ch	32	USB3P0SS_CTRL_DEV_EP_IEN	0F40 003Ch
40h	32	USB3P0SS_CTRL_DEV_EP_ISTS	0F40 0040h
44h	32	USB3P0SS_CTRL_DEV_USB_PWR	0F40 0044h
48h	32	USB3P0SS_CTRL_DEV_USB_CONF2	0F40 0048h
4Ch	32	USB3P0SS_CTRL_DEV_USB_CAP1	0F40 004Ch
50h	32	USB3P0SS_CTRL_DEV_USB_CAP2	0F40 0050h
54h	32	USB3P0SS_CTRL_DEV_USB_CAP3	0F40 0054h
58h	32	USB3P0SS_CTRL_DEV_USB_CAP4	0F40 0058h
5Ch	32	USB3P0SS_CTRL_DEV_USB_CAP5	0F40 005Ch
60h	32	USB3P0SS_CTRL_DEV_USB_CAP6	0F40 0060h
64h	32	USB3P0SS_CTRL_DEV_USB_CPKT1	0F40 0064h
68h	32	USB3P0SS_CTRL_DEV_USB_CPKT2	0F40 0068h
6Ch	32	USB3P0SS_CTRL_DEV_USB_CPKT3	0F40 006Ch
70h	32	USB3P0SS_CTRL_DEV_EP_DMA_EXT_ADDR	0F40 0070h
74h	32	USB3P0SS_CTRL_DEV_BUF_ADDR	0F40 0074h
78h	32	USB3P0SS_CTRL_DEV_BUF_DATA	0F40 0078h
7Ch	32	USB3P0SS_CTRL_DEV_BUF_CTRL	0F40 007Ch
80h	32	USB3P0SS_CTRL_DEV_DTRANS	0F40 0080h
84h	32	USB3P0SS_CTRL_DEV_TDL_FROM_TRB	0F40 0084h
88h	32	USB3P0SS_CTRL_DEV_TDL_BEH	0F40 0088h
8Ch	32	USB3P0SS_CTRL_DEV_EP_TDL	0F40 008Ch
90h	32	USB3P0SS_CTRL_DEV_TDL_BEH2	0F40 0090h
94h	32	USB3P0SS_CTRL_DEV_DMA_ADV_TD	0F40 0094h
100h	32	USB3P0SS_CTRL_DEV_CFG_REG1	0F40 0100h
104h	32	USB3P0SS_CTRL_DEV_DBG_LINK1	0F40 0104h
108h	32	USB3P0SS_CTRL_DEV_DBG_LINK2	0F40 0108h
10Ch	32	USB3P0SS_CTRL_DEV_CFG_REG4	0F40 010Ch
110h	32	USB3P0SS_CTRL_DEV_CFG_REG5	0F40 0110h
114h	32	USB3P0SS_CTRL_DEV_CFG_REG6	0F40 0114h
118h	32	USB3P0SS_CTRL_DEV_CFG_REG7	0F40 0118h
11Ch	32	USB3P0SS_CTRL_DEV_CFG_REG8	0F40 011Ch
120h	32	USB3P0SS_CTRL_DEV_CFG_REG9	0F40 0120h
124h	32	USB3P0SS_CTRL_DEV_CFG_REG10	0F40 0124h
128h	32	USB3P0SS_CTRL_DEV_CFG_REG11	0F40 0128h
12Ch	32	USB3P0SS_CTRL_DEV_CFG_REG12	0F40 012Ch
130h	32	USB3P0SS_CTRL_DEV_CFG_REG13	0F40 0130h
134h	32	USB3P0SS_CTRL_DEV_CFG_REG14	0F40 0134h

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
138h	32	USB3P0SS_CTRL_DEV_CFG_REG15	0F40 0138h
13Ch	32	USB3P0SS_CTRL_DEV_CFG_REG16	0F40 013Ch
140h	32	USB3P0SS_CTRL_DEV_CFG_REG17	0F40 0140h
144h	32	USB3P0SS_CTRL_DEV_CFG_REG18	0F40 0144h
148h	32	USB3P0SS_CTRL_DEV_CFG_REG19	0F40 0148h
14Ch	32	USB3P0SS_CTRL_DEV_CFG_REG20	0F40 014Ch
150h	32	USB3P0SS_CTRL_DEV_CFG_REG21	0F40 0150h
154h	32	USB3P0SS_CTRL_DEV_CFG_REG22	0F40 0154h
158h	32	USB3P0SS_CTRL_DEV_CFG_REG23	0F40 0158h
15Ch	32	USB3P0SS_CTRL_DEV_CFG_REG24	0F40 015Ch
160h	32	USB3P0SS_CTRL_DEV_CFG_REG25	0F40 0160h
164h	32	USB3P0SS_CTRL_DEV_CFG_REG26	0F40 0164h
168h	32	USB3P0SS_CTRL_DEV_CFG_REG27	0F40 0168h
16Ch	32	USB3P0SS_CTRL_DEV_CFG_REG28	0F40 016Ch
170h	32	USB3P0SS_CTRL_DEV_CFG_REG29	0F40 0170h
174h	32	USB3P0SS_CTRL_DEV_CFG_REG30	0F40 0174h
178h	32	USB3P0SS_CTRL_DEV_CFG_REG31	0F40 0178h
17Ch	32	USB3P0SS_CTRL_DEV_CFG_REG32	0F40 017Ch
180h	32	USB3P0SS_CTRL_DEV_CFG_REG33	0F40 0180h
184h	32	USB3P0SS_CTRL_DEV_CFG_REG34	0F40 0184h
188h	32	USB3P0SS_CTRL_DEV_CFG_REG35	0F40 0188h
1ACh	32	USB3P0SS_CTRL_DEV_CFG_REG36	0F40 01ACh
1B0h	32	USB3P0SS_CTRL_DEV_CFG_REG37	0F40 01B0h
1B4h	32	USB3P0SS_CTRL_DEV_CFG_REG38	0F40 01B4h
1B8h	32	USB3P0SS_CTRL_DEV_CFG_REG39	0F40 01B8h
1BCh	32	USB3P0SS_CTRL_DEV_CFG_REG40	0F40 01BCh
1C0h	32	USB3P0SS_CTRL_DEV_CFG_REG41	0F40 01C0h
1C4h	32	USB3P0SS_CTRL_DEV_CFG_REG42	0F40 01C4h
1C8h	32	USB3P0SS_CTRL_DEV_CFG_REG43	0F40 01C8h
1CCh	32	USB3P0SS_CTRL_DEV_CFG_REG44	0F40 01CCh
1D0h	32	USB3P0SS_CTRL_DEV_CFG_REG45	0F40 01D0h
1D4h	32	USB3P0SS_CTRL_DEV_CFG_REG46	0F40 01D4h
1D8h	32	USB3P0SS_CTRL_DEV_CFG_REG47	0F40 01D8h
1DCh	32	USB3P0SS_CTRL_DEV_CFG_REG48	0F40 01DCh
1E0h	32	USB3P0SS_CTRL_DEV_CFG_REG49	0F40 01E0h
1E4h	32	USB3P0SS_CTRL_DEV_CFG_REG50	0F40 01E4h
1E8h	32	USB3P0SS_CTRL_DEV_CFG_REG51	0F40 01E8h
1ECh	32	USB3P0SS_CTRL_DEV_CFG_REG52	0F40 01ECh
1F0h	32	USB3P0SS_CTRL_DEV_CFG_REG53	0F40 01F0h
1F4h	32	USB3P0SS_CTRL_DEV_CFG_REG54	0F40 01F4h
1F8h	32	USB3P0SS_CTRL_DEV_CFG_REG55	0F40 01F8h
1FCh	32	USB3P0SS_CTRL_DEV_CFG_REG56	0F40 01FCh
200h	32	USB3P0SS_CTRL_DEV_CFG_REG57	0F40 0200h
204h	32	USB3P0SS_CTRL_DEV_CFG_REG58	0F40 0204h
208h	32	USB3P0SS_CTRL_DEV_CFG_REG59	0F40 0208h

Table 14-20853. USB3P0SS_CTRL Registers, Base Address=0F40 0000h, Length=262144 (continued)

Offset	Length	Register Name	USB0 Physical Address
20Ch	32	USB3P0SS_CTRL_DEV_CFG_REG60	0F40 020Ch
210h	32	USB3P0SS_CTRL_DEV_CFG_REG61	0F40 0210h
214h	32	USB3P0SS_CTRL_DEV_CFG_REG62	0F40 0214h
218h	32	USB3P0SS_CTRL_DEV_CFG_REG63	0F40 0218h
220h	32	USB3P0SS_CTRL_DEV_CFG_REG64	0F40 0220h
224h	32	USB3P0SS_CTRL_DEV_CFG_REG65	0F40 0224h
228h	32	USB3P0SS_CTRL_DEV_CFG_REG66	0F40 0228h
300h	32	USB3P0SS_CTRL_DEV_DMA_AXI_CTRL	0F40 0300h
304h	32	USB3P0SS_CTRL_DEV_DMA_AXI_ID	0F40 0304h
308h	32	USB3P0SS_CTRL_DEV_DMA_AXI_CAP	0F40 0308h
30Ch	32	USB3P0SS_CTRL_DEV_DMA_AXI_CTRL0	0F40 030Ch
310h	32	USB3P0SS_CTRL_DEV_DMA_AXI_CTRL1	0F40 0310h
314h	32	USB3P0SS_CTRL_DEV_DMA_AXI_CTRL2	0F40 0314h

Table 14-20854. USB3P0SS_CMN Registers, Base Address=0F90 0000h, Length=256

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB3P0SS_CMN_PID	0F90 0000h
4h	32	USB3P0SS_CMN_USB3P0SS_W1	0F90 0004h
8h	32	USB3P0SS_CMN_STATIC_CONFIG	0F90 0008h
Ch	32	USB3P0SS_CMN_PHY_TEST	0F90 000Ch
10h	32	USB3P0SS_CMN_USB3P0SS_DEBUG_CTRL	0F90 0010h
14h	32	USB3P0SS_CMN_USB3P0SS_DEBUG_INFO	0F90 0014h
18h	32	USB3P0SS_CMN_USB3P0SS_DEBUG_LINK_STATE	0F90 0018h
1Ch	32	USB3P0SS_CMN_USB3P0SS_DEVICE_CTRL	0F90 001Ch

Table 14-20855. USB3P0SS_ERR_INJ Registers, Base Address=0F90 1000h, Length=1024

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB3P0SS_ERR_INJ_PID	0F90 1000h
4h	32	USB3P0SS_ERR_INJ_INFO	0F90 1004h
8h	32	USB3P0SS_ERR_INJ_SFT_RST	0F90 1008h
10h	32	USB3P0SS_ERR_INJ_BIT1	0F90 1010h
14h	32	USB3P0SS_ERR_INJ_BIT2	0F90 1014h
18h	32	USB3P0SS_ERR_INJ_TRGT	0F90 1018h
1Ch	32	USB3P0SS_ERR_INJ_CTRL	0F90 101Ch
20h	32	USB3P0SS_ERR_INJ_STATUS	0F90 1020h

Table 14-20856. USB3P0SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB3P0SS_PHY2_AFE_TX_REG0	0F90 8000h
4h	32	USB3P0SS_PHY2_AFE_TX_REG1	0F90 8004h
8h	32	USB3P0SS_PHY2_AFE_TX_REG2	0F90 8008h
Ch	32	USB3P0SS_PHY2_AFE_TX_REG3	0F90 800Ch
10h	32	USB3P0SS_PHY2_AFE_TX_REG4	0F90 8010h

Table 14-20856. USB3P0SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
14h	32	USB3P0SS_PHY2_AFE_TX_REG5	0F90 8014h
18h	32	USB3P0SS_PHY2_AFE_TX_REG6	0F90 8018h
1Ch	32	USB3P0SS_PHY2_AFE_TX_REG7	0F90 801Ch
20h	32	USB3P0SS_PHY2_AFE_TX_REG8	0F90 8020h
24h	32	USB3P0SS_PHY2_AFE_TX_REG9	0F90 8024h
28h	32	USB3P0SS_PHY2_AFE_TX_REG10	0F90 8028h
2Ch	32	USB3P0SS_PHY2_AFE_TX_REG11	0F90 802Ch
30h	32	USB3P0SS_PHY2_AFE_TX_REG12	0F90 8030h
34h	32	USB3P0SS_PHY2_AFE_RX_REG0	0F90 8034h
38h	32	USB3P0SS_PHY2_AFE_RX_REG1	0F90 8038h
3Ch	32	USB3P0SS_PHY2_AFE_RX_REG2	0F90 803Ch
40h	32	USB3P0SS_PHY2_AFE_RX_REG3	0F90 8040h
44h	32	USB3P0SS_PHY2_AFE_RX_REG4	0F90 8044h
48h	32	USB3P0SS_PHY2_AFE_RX_REG5	0F90 8048h
4Ch	32	USB3P0SS_PHY2_AFE_RX_REG6	0F90 804Ch
50h	32	USB3P0SS_PHY2_AFE_TX_REG13	0F90 8050h
54h	32	USB3P0SS_PHY2_AFE_TX_REG14	0F90 8054h
58h	32	USB3P0SS_PHY2_AFE_RX_REG7	0F90 8058h
5Ch	32	USB3P0SS_PHY2_AFE_RX_REG8	0F90 805Ch
60h	32	USB3P0SS_PHY2_AFE_UNUSED_REG0	0F90 8060h
64h	32	USB3P0SS_PHY2_AFE_UNUSED_REG1	0F90 8064h
80h	32	USB3P0SS_PHY2_AFE_BG_REG0	0F90 8080h
84h	32	USB3P0SS_PHY2_AFE_BG_REG1	0F90 8084h
88h	32	USB3P0SS_PHY2_AFE_BG_REG2	0F90 8088h
8Ch	32	USB3P0SS_PHY2_AFE_BG_REG3	0F90 808Ch
90h	32	USB3P0SS_PHY2_AFE_CALIB_REG0	0F90 8090h
94h	32	USB3P0SS_PHY2_AFE_BC_REG0	0F90 8094h
98h	32	USB3P0SS_PHY2_AFE_BC_REG1	0F90 8098h
9Ch	32	USB3P0SS_PHY2_AFE_BC_REG2	0F90 809Ch
A0h	32	USB3P0SS_PHY2_AFE_BC_REG3	0F90 80A0h
A4h	32	USB3P0SS_PHY2_AFE_BC_REG4	0F90 80A4h
A8h	32	USB3P0SS_PHY2_AFE_BC_REG5	0F90 80A8h
ACh	32	USB3P0SS_PHY2_AFE_BC_REG6	0F90 80ACh
B0h	32	USB3P0SS_PHY2_AFE_PLL_REG0	0F90 80B0h
B4h	32	USB3P0SS_PHY2_AFE_PLL_REG1	0F90 80B4h
B8h	32	USB3P0SS_PHY2_AFE_PLL_REG2	0F90 80B8h
BCh	32	USB3P0SS_PHY2_AFE_PLL_REG3	0F90 80BCh
C0h	32	USB3P0SS_PHY2_AFE_PLL_REG4	0F90 80C0h
C4h	32	USB3P0SS_PHY2_AFE_PLL_REG5	0F90 80C4h
C8h	32	USB3P0SS_PHY2_AFE_BG_REG4	0F90 80C8h
CCh	32	USB3P0SS_PHY2_AFE_CALIB_REG1	0F90 80CCh
D0h	32	USB3P0SS_PHY2_AFE_BC_REG7	0F90 80D0h
D4h	32	USB3P0SS_PHY2_AFE_PLL_REG6	0F90 80D4h
D8h	32	USB3P0SS_PHY2_AFE_UNUSED_REG2	0F90 80D8h
DCh	32	USB3P0SS_PHY2_AFE_UNUSED_REG3	0F90 80DCh

Table 14-20856. USB3P0SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
100h	32	USB3P0SS_PHY2_PLL_REG0	0F90 8100h
104h	32	USB3P0SS_PHY2_PLL_REG1	0F90 8104h
108h	32	USB3P0SS_PHY2_PLL_REG2	0F90 8108h
10Ch	32	USB3P0SS_PHY2_PLL_REG3	0F90 810Ch
110h	32	USB3P0SS_PHY2_PLL_REG4	0F90 8110h
114h	32	USB3P0SS_PHY2_PLL_REG5	0F90 8114h
118h	32	USB3P0SS_PHY2_PLL_REG6	0F90 8118h
11Ch	32	USB3P0SS_PHY2_PLL_REG7	0F90 811Ch
120h	32	USB3P0SS_PHY2_PLL_REG8	0F90 8120h
124h	32	USB3P0SS_PHY2_PLL_REG9	0F90 8124h
128h	32	USB3P0SS_PHY2_PLL_REG10	0F90 8128h
12Ch	32	USB3P0SS_PHY2_PLL_REG11	0F90 812Ch
130h	32	USB3P0SS_PHY2_PLL_REG12	0F90 8130h
134h	32	USB3P0SS_PHY2_PLL_REG13	0F90 8134h
138h	32	USB3P0SS_PHY2_PLL_REG14	0F90 8138h
13Ch	32	USB3P0SS_PHY2_PLL_UNUSED_REG0	0F90 813Ch
140h	32	USB3P0SS_PHY2_PLL_UNUSED_REG1	0F90 8140h
144h	32	USB3P0SS_PHY2_PLL_REG15	0F90 8144h
148h	32	USB3P0SS_PHY2_PLL_REG16	0F90 8148h
14Ch	32	USB3P0SS_PHY2_PLL_UNUSED_REG2	0F90 814Ch
180h	32	USB3P0SS_PHY2_CALIB_REG0	0F90 8180h
184h	32	USB3P0SS_PHY2_CALIB_REG1	0F90 8184h
188h	32	USB3P0SS_PHY2_BC_REG0	0F90 8188h
18Ch	32	USB3P0SS_PHY2_BC_REG1	0F90 818Ch
190h	32	USB3P0SS_PHY2_BC_REG2	0F90 8190h
194h	32	USB3P0SS_PHY2_BC_REG3	0F90 8194h
198h	32	USB3P0SS_PHY2_BC_REG4	0F90 8198h
19Ch	32	USB3P0SS_PHY2_BC_REG5	0F90 819Ch
1A0h	32	USB3P0SS_PHY2_BC_REG6	0F90 81A0h
1A4h	32	USB3P0SS_PHY2_BC_REG7	0F90 81A4h
1A8h	32	USB3P0SS_PHY2_TED_REG0	0F90 81A8h
1ACh	32	USB3P0SS_PHY2_TED_REG1	0F90 81ACh
1B0h	32	USB3P0SS_PHY2_TED_REG2	0F90 81B0h
1B4h	32	USB3P0SS_PHY2_CALIB_REG2	0F90 81B4h
1B8h	32	USB3P0SS_PHY2_CALIB_REG3	0F90 81B8h
1BCh	32	USB3P0SS_PHY2_BC_REG8	0F90 81BCh
1C0h	32	USB3P0SS_PHY2_BC_REG9	0F90 81C0h
1C4h	32	USB3P0SS_PHY2_BC_REG10	0F90 81C4h
1C8h	32	USB3P0SS_PHY2_BC_REG11	0F90 81C8h
1CCh	32	USB3P0SS_PHY2_BC_REG12	0F90 81CCh
1D0h	32	USB3P0SS_PHY2_TED_REG3	0F90 81D0h
1D4h	32	USB3P0SS_PHY2_TED_REG4	0F90 81D4h
1D8h	32	USB3P0SS_PHY2_DIG_UNUSED_REG0	0F90 81D8h
1DCh	32	USB3P0SS_PHY2_DIG_UNUSED_REG1	0F90 81DCh
1E0h	32	USB3P0SS_PHY2_DIG_UNUSED_REG2	0F90 81E0h

Table 14-20856. USB3P0SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
1E4h	32	USB3P0SS_PHY2_DIG_UNUSED_REG3	0F90 81E4h
1E8h	32	USB3P0SS_PHY2_INTERRUPT_REG1	0F90 81E8h
1ECh	32	USB3P0SS_PHY2_INTERRUPT_REG2	0F90 81ECh
200h	32	USB3P0SS_PHY2_RX_REG0	0F90 8200h
204h	32	USB3P0SS_PHY2_RX_REG1	0F90 8204h
208h	32	USB3P0SS_PHY2_TX_REG0	0F90 8208h
20Ch	32	USB3P0SS_PHY2_TX_REG1	0F90 820Ch
210h	32	USB3P0SS_PHY2_CDR_REG0	0F90 8210h
214h	32	USB3P0SS_PHY2_CDR_REG1	0F90 8214h
218h	32	USB3P0SS_PHY2_CDR_REG2	0F90 8218h
21Ch	32	USB3P0SS_PHY2_CDR_REG3	0F90 821Ch
220h	32	USB3P0SS_PHY2_CDR_REG4	0F90 8220h
224h	32	USB3P0SS_PHY2_CDR_REG5	0F90 8224h
228h	32	USB3P0SS_PHY2_CDR_REG6	0F90 8228h
22Ch	32	USB3P0SS_PHY2_CDR_REG7	0F90 822Ch
230h	32	USB3P0SS_PHY2_CDR_REG8	0F90 8230h
234h	32	USB3P0SS_PHY2_RX_REG2	0F90 8234h
238h	32	USB3P0SS_PHY2_RX_REG3	0F90 8238h
23Ch	32	USB3P0SS_PHY2_RX_REG4	0F90 823Ch
240h	32	USB3P0SS_PHY2_RX_REG5	0F90 8240h
244h	32	USB3P0SS_PHY2_RX_REG6	0F90 8244h
248h	32	USB3P0SS_PHY2_RX_REG7	0F90 8248h
24Ch	32	USB3P0SS_PHY2_TX_REG2	0F90 824Ch
250h	32	USB3P0SS_PHY2_TX_REG3	0F90 8250h
254h	32	USB3P0SS_PHY2_TX_REG4	0F90 8254h
258h	32	USB3P0SS_PHY2_CDR_REG9	0F90 8258h
25Ch	32	USB3P0SS_PHY2_CDR_REG10	0F90 825Ch
260h	32	USB3P0SS_PHY2_CDR_REG11	0F90 8260h
264h	32	USB3P0SS_PHY2_CDR_RE12	0F90 8264h
268h	32	USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG0	0F90 8268h
26Ch	32	USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG1	0F90 826Ch
270h	32	USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG2	0F90 8270h
274h	32	USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG3	0F90 8274h
280h	32	USB3P0SS_PHY2_UTMI_REG0	0F90 8280h
284h	32	USB3P0SS_PHY2_UTMI_REG1	0F90 8284h
288h	32	USB3P0SS_PHY2_UTMI_REG2	0F90 8288h
28Ch	32	USB3P0SS_PHY2_UTMI_REG3	0F90 828Ch
290h	32	USB3P0SS_PHY2_UTMI_REG4	0F90 8290h
294h	32	USB3P0SS_PHY2_UTMI_REG5	0F90 8294h
298h	32	USB3P0SS_PHY2_UTMI_REG6	0F90 8298h
29Ch	32	USB3P0SS_PHY2_UTMI_REG7	0F90 829Ch
2A0h	32	USB3P0SS_PHY2_UTMI_REG8	0F90 82A0h
2A4h	32	USB3P0SS_PHY2_UTMI_REG9	0F90 82A4h
2A8h	32	USB3P0SS_PHY2_UTMI_REG10	0F90 82A8h
2ACh	32	USB3P0SS_PHY2_UTMI_REG11	0F90 82ACh

Table 14-20856. USB3P0SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
2B0h	32	USB3P0SS_PHY2_UTMI_REG12	0F90 82B0h
2B4h	32	USB3P0SS_PHY2_UTMI_REG13	0F90 82B4h
2B8h	32	USB3P0SS_PHY2_UTMI_REG14	0F90 82B8h
2BCh	32	USB3P0SS_PHY2_UTMI_REG15	0F90 82BCh
2C0h	32	USB3P0SS_PHY2_UTMI_REG16	0F90 82C0h
2C4h	32	USB3P0SS_PHY2_UTMI_REG17	0F90 82C4h
2C8h	32	USB3P0SS_PHY2_UTMI_REG18	0F90 82C8h
2CCh	32	USB3P0SS_PHY2_UTMI_REG19	0F90 82CCh
2D0h	32	USB3P0SS_PHY2_UTMI_REG20	0F90 82D0h
2D4h	32	USB3P0SS_PHY2_UTMI_REG21	0F90 82D4h
2D8h	32	USB3P0SS_PHY2_UTMI_REG22	0F90 82D8h
2DCh	32	USB3P0SS_PHY2_UTMI_REG23	0F90 82DCh
2E0h	32	USB3P0SS_PHY2_UTMI_REG24	0F90 82E0h
2E4h	32	USB3P0SS_PHY2_UTMI_REG25	0F90 82E4h
2E8h	32	USB3P0SS_PHY2_UTMI_REG26	0F90 82E8h
2ECh	32	USB3P0SS_PHY2_UTMI_REG27	0F90 82ECh
2F0h	32	USB3P0SS_PHY2_UTMI_REG28	0F90 82F0h
2F4h	32	USB3P0SS_PHY2_UTMI_REG29	0F90 82F4h
2F8h	32	USB3P0SS_PHY2_UTMI_REG30	0F90 82F8h
2FCh	32	USB3P0SS_PHY2_UTMI_UNUSED_REG0	0F90 82FCh
300h	32	USB3P0SS_PHY2_UTMI_UNUSED_REG1	0F90 8300h
304h	32	USB3P0SS_PHY2_UTMI_UNUSED_REG2	0F90 8304h
308h	32	USB3P0SS_PHY2_UTMI_UNUSED_REG3	0F90 8308h
30Ch	32	USB3P0SS_PHY2_UTMI_REG31	0F90 830Ch
310h	32	USB3P0SS_PHY2_UTMI_REG32	0F90 8310h
314h	32	USB3P0SS_PHY2_UTMI_REG33	0F90 8314h
318h	32	USB3P0SS_PHY2_UTMI_REG34	0F90 8318h
31Ch	32	USB3P0SS_PHY2_UTMI_REG35	0F90 831Ch
320h	32	USB3P0SS_PHY2_UTMI_REG36	0F90 8320h
324h	32	USB3P0SS_PHY2_UTMI_REG37	0F90 8324h
328h	32	USB3P0SS_PHY2_UTMI_REG38	0F90 8328h
32Ch	32	USB3P0SS_PHY2_UTMI_REG39	0F90 832Ch
330h	32	USB3P0SS_PHY2_UTMI_REG40	0F90 8330h
334h	32	USB3P0SS_PHY2_UTMI_REG41	0F90 8334h
338h	32	USB3P0SS_PHY2_UTMI_REG42	0F90 8338h
33Ch	32	USB3P0SS_PHY2_UTMI_REG43	0F90 833Ch
340h	32	USB3P0SS_PHY2_UTMI_REG44	0F90 8340h
344h	32	USB3P0SS_PHY2_UTMI_REG45	0F90 8344h
348h	32	USB3P0SS_PHY2_UTMI_REG46	0F90 8348h
34Ch	32	USB3P0SS_PHY2_UTMI_REG47	0F90 834Ch
350h	32	USB3P0SS_PHY2_UTMI_REG48	0F90 8350h
354h	32	USB3P0SS_PHY2_UTMI_REG49	0F90 8354h
358h	32	USB3P0SS_PHY2_UTMI_REG50	0F90 8358h
35Ch	32	USB3P0SS_PHY2_UTMI_REG51	0F90 835Ch
360h	32	USB3P0SS_PHY2_UTMI_REG52	0F90 8360h

Table 14-20856. USB3P0SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
364h	32	USB3P0SS_PHY2_UTMI_REG53	0F90 8364h
368h	32	USB3P0SS_PHY2_UTMI_REG54	0F90 8368h
36Ch	32	USB3P0SS_PHY2_UTMI_REG55	0F90 836Ch
370h	32	USB3P0SS_PHY2_UTMI_REG56	0F90 8370h
374h	32	USB3P0SS_PHY2_UTMI_REG57	0F90 8374h
378h	32	USB3P0SS_PHY2_UTMI_REG58	0F90 8378h
37Ch	32	USB3P0SS_PHY2_UTMI_REG59	0F90 837Ch
380h	32	USB3P0SS_PHY2_UTMI_UNUSED_REG6	0F90 8380h
384h	32	USB3P0SS_PHY2_UTMI_UNUSED_REG7	0F90 8384h

14.9.2.3.2 USB Registers

USB Registers

14.9.2.3.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-20857. Instance Table

Instance Name	Physical Address
USB0	**0070 3000h**

Figure 14-6891. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-20859. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.2.3.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-20860. Instance Table

Instance Name	Physical Address
USB0	**0070 3008h**

Figure 14-6892. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-20862. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.2.3.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-20863. Instance Table

Instance Name	Physical Address
USB0	**0070 300Ch**

Figure 14-6893. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1h							

Table 14-20865. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.2.3.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-20866. Instance Table

Instance Name	Physical Address
USB0	**0070 3010h + formula**

Figure 14-6894. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-20868. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.2.3.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-20869. Instance Table

Instance Name	Physical Address
USB0	**0070 303Ch**

Figure 14-6895. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-20871. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.2.3.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-20872. Instance Table

Instance Name	Physical Address
USB0	**0070 3040h**

Figure 14-6896. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_PEND
NONE							R/W1TS
0h							0h

Table 14-20874. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.9.2.3.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-20875. Instance Table

Instance Name	Physical Address
USB0	**0070 3080h**

Figure 14-6897. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>RAMECC_ENABLE_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-20877. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.9.2.3.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-20878. Instance Table

Instance Name	Physical Address
USB0	**0070 30C0h**

Figure 14-6898. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-20880. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.9.2.3.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-20881. Instance Table

Instance Name	Physical Address
USB0	**0070 313Ch**

Figure 14-6899. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-20883. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.2.3.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-20884. Instance Table

Instance Name	Physical Address
USB0	**0070 3140h**

Figure 14-6900. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_PEND
NONE							R/W1TS
0h							0h

Table 14-20886. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.9.2.3.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-20887. Instance Table

Instance Name	Physical Address
USB0	**0070 3180h**

Figure 14-6901. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-20889. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.9.2.3.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-20890. Instance Table

Instance Name	Physical Address
USB0	**0070 31C0h**

Figure 14-6902. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-20892. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.9.2.3.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-20893. Instance Table

Instance Name	Physical Address
USB0	**0070 3200h**

Figure 14-6903. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-20895. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.2.3.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-20896. Instance Table

Instance Name	Physical Address
USB0	**0070 3204h**

Figure 14-6904. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-20898. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.2.3.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-20899. Instance Table

Instance Name	Physical Address
USB0	**0070 3208h**

Figure 14-6905. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-20901. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.2.3.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-20902. Instance Table

Instance Name	Physical Address
USB0	**0070 320Ch**

Figure 14-6906. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-20904. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.2.3.2.17 USB3P0SS_CTRL_DRD_CDNS_DID Register

1 USB3P0SS_CTRL_DRD_CDNS_DID Register (Offset = 0h) [reset = 4024Eh]

Cadence Device ID Register ASF parity-protected: no

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Table 14-20905. Instance Table

Instance Name	Physical Address
USB0	**0F40 0000h**

Figure 14-6907. USB3P0SS_CTRL_DRD_CDNS_DID Name Register

31	30	29	28	27	26	25	24
DID							
R							
4024Eh							
23	22	21	20	19	18	17	16
DID							
R							
4024Eh							
15	14	13	12	11	10	9	8
DID							
R							
4024Eh							
7	6	5	4	3	2	1	0
DID							
R							
4024Eh							

Table 14-20907. USB3P0SS_CTRL_DRD_CDNS_DID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DID	R	4024Eh	Cadence Device ID Register IP4024E Reset Source: rst_mod_g_rst_n

14.9.2.3.2.18 USB3P0SS_CTRL_DRD_CDNS_RID Register

1 USB3P0SS_CTRL_DRD_CDNS_RID Register (Offset = 4h) [reset = 200h]

Cadence Revision ID Register ASF parity-protected: no

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Table 14-20908. Instance Table

Instance Name	Physical Address
USB0	**0F40 0004h**

Figure 14-6908. USB3P0SS_CTRL_DRD_CDNS_RID Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CDNS_RID							
R							
200h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CDNS_RID							
R							
200h							

Table 14-20910. USB3P0SS_CTRL_DRD_CDNS_RID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	CDNS_RID	R	200h	CDNS_RID Reset Source: rst_mod_g_rst_n

14.9.2.3.2.19 USB3P0SS_CTRL_DRD_OTGCAPABILITY Register

1 USB3P0SS_CTRL_DRD_OTGCAPABILITY Register (Offset = 8h) [reset = 1102002Bh]

OTG Capabilities register

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Table 14-20911. Instance Table

Instance Name	Physical Address
USB0	**0F40 0008h**

Figure 14-6909. USB3P0SS_CTRL_DRD_OTGCAPABILITY Name Register

31	30	29	28	27	26	25	24
OTG3REVISION							
R							
110h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OTG3REVISION				OTG2REVISION			
R				R			
110h				200h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OTG2REVISION							
R							
200h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD1		REFCLK_DISABLE	RSP_SUPPORT	BC_SUPPORT	ADP_SUPPORT	HNP_SUPPORT	SRP_SUPPORT
R		R	R	R	R	R	R
0h		1h	0h	1h	0h	1h	1h

Table 14-20913. USB3P0SS_CTRL_DRD_OTGCAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	OTG3REVISION	R	110h	Specifies implemeted OTG3.0 specification revision Reset Source: rst_mod_g_rst_n
19:8	OTG2REVISION	R	200h	Specifies implemeted OTG2.0 specification revision Reset Source: rst_mod_g_rst_n
7:6	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
5	REFCLK_DISABLE	R	1h	PHY Reference clock control disable. 0 - PHY Reference clock control supported 1 - PHY Reference clock control not supported Reset Source: rst_mod_g_rst_n
4	RSP_SUPPORT	R	0h	RSP support. 0 - RSP not supported 1 - RSP supported Reset Source: rst_mod_g_rst_n

Table 14-20913. USB3P0SS_CTRL_DRD_OTGCAPABILITY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BC_SUPPORT	R	1h	BC Support [Battery Charging specification rev 1.2]. 0 - BC not supported 1 - BC supported Reset Source: rst_mod_g_rst_n
2	ADP_SUPPORT	R	0h	ADP support. 0 - ADP not supported 1 - ADP supported Reset Source: rst_mod_g_rst_n
1	HNP_SUPPORT	R	1h	HNP support. 0 - HNP not supported 1 - HNP supported Reset Source: rst_mod_g_rst_n
0	SRP_SUPPORT	R	1h	SRP support. 0 - SRP not supported 1 - SRP supported Reset Source: rst_mod_g_rst_n

14.9.2.3.2.20 USB3P0SS_CTRL_DRD_OTGCMD Register

1 USB3P0SS_CTRL_DRD_OTGCMD Register (Offset = 10h) [reset = 0h]

OTGCMD

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Table 14-20914. Instance Table

Instance Name	Physical Address
USB0	0F40 0010h

Figure 14-6910. USB3P0SS_CTRL_DRD_OTGCMD Name Register

31	30	29	28	27	26	25	24
RSVD2	DEV_VBUS_DEB_SHORT_CLR	DEV_VBUS_DEB_SHORT_SET	INIT_SRP	OTG2_SWITCH_TO_PERIPH	B_HNP_EN_CLR	B_HNP_EN_SET	A_SET_B_HNP_EN_CLR
R	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
A_SET_B_HNP_EN_SET	SS_PERIPH_DISABLED_CLR	SS_PERIPH_DISABLED_SET	SS_HOST_DISABLED_CLR	SS_HOST_DISABLED_SET	D_WRST_FOR_SWAP_CLR	D_WRST_FOR_SWAP_SET	H_WRST_FOR_SWAP_CLR
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
H_WRST_FOR_SWAP_SET	DEV_DEVEN_FORCE_CLR	DEV_DEVEN_FORCE_SET	HOST_POWER_OFF	DEV_POWER_OFF	DIS_VBUS_DROP	HOST_BUS_DROP	DEV_BUS_DROP
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
DEV_SESS_VLD_USE_CLR	DEV_SESS_VLD_USE_SET	A_DEV_DIS	A_DEV_EN	OTG_DIS	OTG_EN	HOST_BUS_REQ	DEV_BUS_REQ
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-20916. USB3P0SS_CTRL_DRD_OTGCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
30	DEV_VBUS_DEB_SHORT_CLR	W	0h	Disable forcing Device short VBUS debounce time. Setting this bit causes DEV_VBUS_DEB_SHORT bit in OTGSTS clear. Reset Source: rst_mod_g_rst_n
29	DEV_VBUS_DEB_SHORT_SET	W	0h	Enable forcing Device short VBUS debounce time. This bit should be set while switching from Host to Device mode takes place. Setting this bit should be done in the same time when Device mode is activated [DEV_BUS_REQ]. Setting this bit causes DEV_VBUS_DEB_SHORT bit in OTGSTS set. Reset Source: rst_mod_g_rst_n

Table 14-20916. USB3P0SS_CTRL_DRD_OTGCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	INIT_SRP	W	0h	Initiate SRP Reset Source: rst_mod_g_rst_n
27	OTG2_SWITCH_TO_PERIPH	W	0h	Switch to Peripheral mode when operating at USB 2.0 Reset Source: rst_mod_g_rst_n
26	B_HNP_EN_CLR	W	0h	This bit should be written if software wants to clear b_hnp_enable Reset Source: rst_mod_g_rst_n
25	B_HNP_EN_SET	W	0h	This bit should be written if SetFeature[b_hnp_enable] has been accepted. Reset Source: rst_mod_g_rst_n
24	A_SET_B_HNP_EN_CLR	W	0h	This bit should be written if upcoming USB 2.0 bus suspend should not cause Role Swap. Reset Source: rst_mod_g_rst_n
23	A_SET_B_HNP_EN_SET	W	0h	This bit should be written if SetFeature[b_hnp_enable] has been sent. Reset Source: rst_mod_g_rst_n
22	SS_PERIPH_DISABLED_CLR	W	0h	Enable SuperSpeed peripheral device functionality. Reset Source: rst_mod_g_rst_n
21	SS_PERIPH_DISABLED_SET	W	0h	Disable SuperSpeed peripheral device functionality. Can be used only if Peripheral mode is not active. Reset Source: rst_mod_g_rst_n
20	SS_HOST_DISABLED_CLR	W	0h	Enable SuperSpeed host functionality. Reset Source: rst_mod_g_rst_n
19	SS_HOST_DISABLED_SET	W	0h	Disable SuperSpeed host functionality. Can be used only if Host mode is not active. Reset Source: rst_mod_g_rst_n
18	D_WRST_FOR_SWAP_CLR	W	0h	Upcoming received Warm Reset should not be treated as Role Swapping indication. This bit should be set after Warm Reset for Role Swap is received on the Port Reset Source: rst_mod_g_rst_n
17	D_WRST_FOR_SWAP_SET	W	0h	Upcoming Warm Reset will be received for Role Swapping. This bit should be set before Warm Reset for Role Swap is received on the Port Reset Source: rst_mod_g_rst_n
16	H_WRST_FOR_SWAP_CLR	W	0h	Upcoming Warm Reset will not be generated for Role Swapping. This bit should be set after Warm Reset for Role Swap is generated on the Port Reset Source: rst_mod_g_rst_n
15	H_WRST_FOR_SWAP_SET	W	0h	Upcoming Warm Reset will be generated for Role Swapping. This bit should be set before Warm Reset for Role Swap is generated on the Port Reset Source: rst_mod_g_rst_n
14	DEV_DEVEN_FORCE_CLR	W	0h	Clear forcing Device DEVEN bit to 1. Setting this bit causes DEV_DEVEN_FORCE bit in OTGSTS clear. Reset Source: rst_mod_g_rst_n

Table 14-20916. USB3P0SS_CTRL_DRD_OTGCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	DEV_DEVEN_FORCE_SET	W	0h	Set forcing Device DEVEN bit to 1. This bit may be set while switching from Host to Device mode takes place. Setting this bit should be done in the same time when Device mode is activated [DEV_BUS_REQ]. Setting this bit causes DEV_DEVEN_FORCE bit in OTGSTS set. Reset Source: rst_mod_g_rst_n
12	HOST_POWER_OFF	W	0h	Power Down CDNSXHCI. Reset Source: rst_mod_g_rst_n
11	DEV_POWER_OFF	W	0h	Power Down USBSS-DEV. Reset Source: rst_mod_g_rst_n
10	DIS_VBUS_DROP	W	0h	Do not disable vbus while bus is dropped. This bit is valid only if DEV_BUS_DROP or HOST_BUS_DROP are set. Reset Source: rst_mod_g_rst_n
9	HOST_BUS_DROP	W	0h	Drop the bus for Host mode. This bit should be set when Host mode is no longer needed. It will clear HOST_ACTIVE bit is OTGSTS register Reset Source: rst_mod_g_rst_n
8	DEV_BUS_DROP	W	0h	Drop the bus for Device mode. This bit should be set when Device mode is no longer needed. It will clear DEV_ACTIVE bit is OTGSTS register Reset Source: rst_mod_g_rst_n
7	DEV_SESS_VLD_USE_CLR	W	0h	Device should use a_vbus_vld as vbus valid indication. This bit should be set in the same time when DEV_BUS_REQ Reset Source: rst_mod_g_rst_n
6	DEV_SESS_VLD_USE_SET	W	0h	Device should use b_sess_vld as vbus valid indication. This bit should be set in the same time when DEV_BUS_REQ Reset Source: rst_mod_g_rst_n
5	A_DEV_DIS	W	0h	Configure OTG as B-Device. It is only valid if OTG mode is enabled. This bit should be set in the same time when OTG_EN Reset Source: rst_mod_g_rst_n
4	A_DEV_EN	W	0h	Configure OTG as A-Device. It is only valid if OTG mode is enabled. This bit should be set in the same time when OTG_EN Reset Source: rst_mod_g_rst_n
3	OTG_DIS	W	0h	Disable OTG mode. It will clear OTG_IS_ENABLED bit is OTGSTS register Reset Source: rst_mod_g_rst_n
2	OTG_EN	W	0h	Enable OTG mode. It will set OTG_IS_ENABLED bit is OTGSTS register Reset Source: rst_mod_g_rst_n
1	HOST_BUS_REQ	W	0h	Request the bus for Host mode. It will set HOST_ACTIVE bit is OTGSTS register Reset Source: rst_mod_g_rst_n
0	DEV_BUS_REQ	W	0h	Request the bus for Device mode. It will set DEV_ACTIVE bit is OTGSTS register Reset Source: rst_mod_g_rst_n

14.9.2.3.2.21 USB3P0SS_CTRL_DRD_OTGSTS Register

1 USB3P0SS_CTRL_DRD_OTGSTS Register (Offset = 14h) [reset = 400h]

OTGSTS

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Table 14-20917. Instance Table

Instance Name	Physical Address
USB0	**0F40 0014h**

Figure 14-6911. USB3P0SS_CTRL_DRD_OTGSTS Name Register

31	30	29	28	27	26	25	24
VBUS_VALID_PHY	SESS_VALID_PHY	HOST_DISCONNECT_PHY	IDDIG_PHY	DEV_READY	XHC_READY	B_HNP_EN	RSVD4
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
A_SET_B_HNP_EN	RSVD3	LINESTATE		SRP_DET_NOT_COMPLIANT_DEV	SRP_INITIAL_CONDITION_MET	D_WRST_FOR_SWAP	DEV_DEVEN_FORCE
R	R	R		R	R	R	R
0h	0h	0h		0h	0h	0h	0h
15	14	13	12	11	10	9	8
H_WRST_FOR_SWAP	STRAP			OTG_NRDY	DEV_SESS_VLD_USE	DEV_VBUS_DEB_SHORT	SS_PERIPH_DISABLED
R	R			R	R	R	R
0h	0h			0h	1h	0h	0h
7	6	5	4	3	2	1	0
SS_HOST_DISABLED	OTG_MODE	OTG_IS_ENABLED	HOST_ACTIVE	DEV_ACTIVE	SESSION_VALID	VBUS_VALID	ID_VALUE
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-20919. USB3P0SS_CTRL_DRD_OTGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VBUS_VALID_PHY	R	0h	PHY VBUS valid comparator status Reset Source: rst_mod_g_rst_n
30	SESS_VALID_PHY	R	0h	PHY Session valid comparator status Reset Source: rst_mod_g_rst_n
29	HOST_DISCONNECT_PHY	R	0h	PHY hostdisconnect status Reset Source: rst_mod_g_rst_n
28	IDDIG_PHY	R	0h	PHY UTMI iddig status Reset Source: rst_mod_g_rst_n
27	DEV_READY	R	0h	Device mode is turned on. registers in USBSS-DEV domain are accessible through APB Reset Source: rst_mod_g_rst_n
26	XHC_READY	R	0h	Host mode is turned on. registers in CDNSXHCI AUX domain are accessible through APB Reset Source: rst_mod_g_rst_n

Table 14-20919. USB3P0SS_CTRL_DRD_OTGSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	B_HNP_EN	R	0h	SetFeature[b_hnp_enable] has been accepted. Reset Source: rst_mod_g_rst_n
24	RSVD4	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
23	A_SET_B_HNP_EN	R	0h	SetFeature[b_hnp_enable] has been sent and is valid. Reset Source: rst_mod_g_rst_n
22	RSVD3	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
21:20	LINESTATE	R	0h	PHY UTMI linestate status Reset Source: rst_mod_g_rst_n
19	SRP_DET_NOT_COMPLIANT_DEV	R	0h	OTG A-device detected not compilant device. If this bit is set then OTG A-device should disable SRP detection until not compilant device is disconnected [SRP_NOT_COMP_DEV_REMOVED_INT] Reset Source: rst_mod_g_rst_n
18	SRP_INITIAL_CONDITION_MET	R	0h	SRP initial condition are met. OTG B-device software should issue SRP puluse onli if this bit is set. Reset Source: rst_mod_g_rst_n
17	D_WRST_FOR_SWAP	R	0h	Upcoming Warm Reset will be received for Role Swapping from Peripheral to Host. Reset Source: rst_mod_g_rst_n
16	DEV_DEVEN_FORCE	R	0h	Device forcing DEVEN bit is enabled. Reset Source: rst_mod_g_rst_n
15	H_WRST_FOR_SWAP	R	0h	Upcoming Warm Reset will be generated for Role Swapping from Host to Peripheral. Reset Source: rst_mod_g_rst_n
14:12	STRAP	R	0h	Value of the strap pins. 000 - no default configuration 010 - Controller initiall configured as Host 100 - Controller initially configured as Device other - Reserved [might be used for Type-C] Reset Source: rst_mod_g_rst_n
11	OTG_NRDY	R	0h	OTG Controller not ready. Software shall not read nor write any register except OTGISTS if this bit is set. Reset Source: rst_mod_g_rst_n
10	DEV_SESS_VLD_USE	R	1h	Device mode vbus valid indication: 0: a_vbus_vld is used as vbus valid 1: b_sess_vld is used as vbus valid Reset Source: rst_mod_g_rst_n
9	DEV_VBUS_DEB_SHORT	R	0h	Device forcing short VBUS decounce is enabled. Reset Source: rst_mod_g_rst_n

Table 14-20919. USB3P0SS_CTRL_DRD_OTGSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SS_PERIPH_DISABLED	R	0h	SuperSpeed device functionality is disabled. Port will be operating at USB 2.0 speed. Reset Source: rst_mod_g_rst_n
7	SS_HOST_DISABLED	R	0h	SuperSpeed host functionality is disabled. Port will be operating at USB 2.0 speed. Reset Source: rst_mod_g_rst_n
6	OTG_MODE	R	0h	OTG mode: 0 - A-Device 1 - B-Device Valid only if OTG_IS_ENABLED is 1. Reset Source: rst_mod_g_rst_n
5	OTG_IS_ENABLED	R	0h	OTG functionality is enabled Reset Source: rst_mod_g_rst_n
4	HOST_ACTIVE	R	0h	Device mode is active. NOTE: It is possible that Host is in inactive state [even turned off] while HOST_ACTIVE is 1. Reset Source: rst_mod_g_rst_n
3	DEV_ACTIVE	R	0h	Device mode is active. NOTE: It is possible that Device is in inactive state [even turned off] while DEV_ACTIVE is 1. Reset Source: rst_mod_g_rst_n
2	SESSION_VALID	R	0h	The sessionvalid status visible to the controller Reset Source: rst_mod_g_rst_n
1	VBUS_VALID	R	0h	The vbusvalid status visible to the controller Reset Source: rst_mod_g_rst_n
0	ID_VALUE	R	0h	Current value of the ID pin visible to the controller. It is only valid when idpullup in PORTOVERRIDE_TYPE register is set to '1'. ID_VALUE must be valid within 50ms after idpullup is set to '1' Reset Source: rst_mod_g_rst_n

14.9.2.3.2.22 USB3P0SS_CTRL_DRD_OTGSTATE Register

1 USB3P0SS_CTRL_DRD_OTGSTATE Register (Offset = 18h) [reset = 2D0000h]

OTGSTATE

Return to Summary Table

Table 14-20920. Instance Table

Instance Name	Physical Address
USB0	**0F40 0018h**

Figure 14-6912. USB3P0SS_CTRL_DRD_OTGSTATE Name Register

31	30	29	28	27	26	25	24
RSVD3							
R							
0h							
23	22	21	20	19	18	17	16
RSVD3		HOST_POWER_STATE			DEV_POWER_STATE		
R		R			R		
0h		5h			5h		
15	14	13	12	11	10	9	8
RSVD2		UTMI_CTRL		PIPE_CTRL		APB_AXI_CTRL	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
RSVD1		HOST_OTG_STATE			DEV_OTG_STATE		
R		R			R		
0h		0h			0h		

Table 14-20922. USB3P0SS_CTRL_DRD_OTGSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RSVD3	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
21:19	HOST_POWER_STATE	R	5h	Current state of the Host power controlling FSM: 3'b000 : POWER_IDLE 3'b001 : POWER_OFF_ACK 3'b010 : POWER_OFF_MAIN_ACK 3'b011 : POWER_OFF 3'b100 : POWER_ON_REQ 3'b101 : POWER_ISO_DIS 3'b110 : POWER_ON 3'b111 : POWER_ON_READY Reset Source: rst_mod_g_rst_n

Table 14-20922. USB3P0SS_CTRL_DRD_OTGSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:16	DEV_POWER_STATE	R	5h	Current state of the Device power controlling FSM: 3'b000 : POWER_IDLE 3'b001 : POWER_OFF_ACK 3'b010 : POWER_OFF_MAIN_ACK 3'b011 : POWER_OFF 3'b100 : POWER_ON_REQ 3'b101 : POWER_ISO_DIS 3'b110 : POWER_ON 3'b111 : POWER_ON_READY Reset Source: rst_mod_g_rst_n
15:14	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
13:12	UTMI_CTRL	R	0h	Current state of the USB2 UTMI mux selector. 2'b00 : Both modes off. OTG takes control over UTMI [SRP,BC] 2'b01 : Host active. 2'b10 : Device active. 2'b11 : Illegal [both modes off] Reset Source: rst_mod_g_rst_n
11:10	PIPE_CTRL	R	0h	Current state of the USB3 PIPE mux selector. 2'b00 : Both modes off. 2'b01 : Host active. 2'b10 : Device active. 2'b11 : Illegal [both modes off] Reset Source: rst_mod_g_rst_n
9:8	APB_AXI_CTRL	R	0h	Current state of the ABP/AXI mux selector. 2'b00 : Both modes off. 2'b01 : Host active. 2'b10 : Device active. 2'b11 : Illegal [both modes off] Reset Source: rst_mod_g_rst_n
7:6	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
5:3	HOST_OTG_STATE	R	0h	Current state of the OTG Host FSM. 3'b000 : H_IDLE 3'b001 : H_VBUS_ON 3'b010 : H_VBUS_FAILED 3'b011 : H_OTG_HOST_MODE 3'b100 : H_HOST_MODE 3'b101 : H_SWITCH_TO_DEVICE 3'b110 : H_A_SUSPEND 3'b111 : H_WAIT_VBUS_FALL Reset Source: rst_mod_g_rst_n

Table 14-20922. USB3P0SS_CTRL_DRD_OTGSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DEV_OTG_STATE	R	0h	Current state of the OTG Device FSM. 3'b000 : DEV_IDLE 3'b001 : DEV_MODE 3'b010 : DEV_SRP 3'b011 : DEV_WAIT_VBUS_FALL 3'b100 : DEV_SWITCH_TO_HOST 3'b101 : DEV_WAIT_FOR_CONN Reset Source: rst_mod_g_rst_n

14.9.2.3.2.23 USB3P0SS_CTRL_DRD_OTGIEN Register

1 USB3P0SS_CTRL_DRD_OTGIEN Register (Offset = 20h) [reset = 0h]

OTGIEN

Return to Summary Table

Table 14-20923. Instance Table

Instance Name	Physical Address
USB0	0F40 0020h

Figure 14-6913. USB3P0SS_CTRL_DRD_OTGIEN Name Register

31	30	29	28	27	26	25	24
DM_VLGC_COMP_RISE_INT_EN	DCD_COMP_FALL_INT_EN	DCD_COMP_RISE_INT_EN	DP_VDAT_REF_RISE_INT_EN	DM_VDAT_REF_RISE_INT_EN	RID_A_RISE_INT_EN	RID_B_RISE_INT_EN	RID_C_RISE_INT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RID_GND_RISE_INT_EN	RID_FLOAT_RISE_INT_EN	RID_FLOAT_FALL_INT_EN	H_WRST_GEN_CMPL_INT_EN	H_POLL_ENTRY_INT_EN	TIMER_TMOUT_INT_EN	TB_AIDL_BDIS_MIN_TMOUT_INT_EN	TB_ASE0_BRST_TMOUT_INT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
SRP_CMPL_INT_EN	SRP_FAIL_INT_EN	OVERCURRENT_INT_EN	SRP_NOT_COMP_DEV_REMOVED_INT_EN	SRP_DET_INT_EN	TA_BIDL_ADIS_TMOUT_INT_EN	TA_AIDL_BDIS_TMOUT_INT_EN	ADP_PROBE_COMPLETED_INT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PROBE_RISE_INT_EN	SENSE_RISE_INT_EN	VBUSVALID_FALL_INT_EN	VBUSVALID_RISE_INT_EN	OTGSESSVALID_FALL_INT_EN	OTGSESSVALID_RISE_INT_EN	VBUS_ON_FAILED_INT_EN	ID_CHANGE_INT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-20925. USB3P0SS_CTRL_DRD_OTGIEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DM_VLGC_COMP_RISE_INT_EN	R/W	0h	DM VLGC comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n
30	DCD_COMP_FALL_INT_EN	R/W	0h	DCD comparator fall detect interrupt enable Reset Source: rst_mod_g_rst_n
29	DCD_COMP_RISE_INT_EN	R/W	0h	DCD comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n
28	DP_VDAT_REF_RISE_INT_EN	R/W	0h	DP VDAT comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n
27	DM_VDAT_REF_RISE_INT_EN	R/W	0h	DM VDAT comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n
26	RID_A_RISE_INT_EN	R/W	0h	RID A comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n

Table 14-20925. USB3P0SS_CTRL_DRD_OTGIEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	RID_B_RISE_INT_EN	R/W	0h	RID B comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n
24	RID_C_RISE_INT_EN	R/W	0h	RID C comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n
23	RID_GND_RISE_INT_EN	R/W	0h	RID GND comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n
22	RID_FLOAT_RISE_INT_EN	R/W	0h	RID floating comparator rise detect interrupt enable Reset Source: rst_mod_g_rst_n
21	RID_FLOAT_FALL_INT_EN	R/W	0h	RID floating comparator detect interrupt enable Reset Source: rst_mod_g_rst_n
20	H_WRST_GEN_CMPL_INT_EN	R/W	0h	Host Warm Reset generation completed interrupt enable. Reset Source: rst_mod_g_rst_n
19	H_POLL_ENTRY_INT_EN	R/W	0h	Host Polling state entry interrupt enable. Reset Source: rst_mod_g_rst_n
18	TIMER_TMOUT_INT_EN	R/W	0h	Timer timeout interrupt enable. Reset Source: rst_mod_g_rst_n
17	TB_AIDL_BDIS_MIN_TMOUT_INT_EN	R/W	0h	The bus has been in Idle state for the required time during HNP interrupt enable. Reset Source: rst_mod_g_rst_n
16	TB_ASE0_BRST_TMOUT_INT_EN	R/W	0h	No response from A-Device to HNP interrupt enable. Reset Source: rst_mod_g_rst_n
15	SRP_CMPL_INT_EN	R/W	0h	SRP completed interrupt enable. Reset Source: rst_mod_g_rst_n
14	SRP_FAIL_INT_EN	R/W	0h	No response from SRP from A-Device interrupt enable. Reset Source: rst_mod_g_rst_n
13	OVERCURRENT_INT_EN	R/W	0h	Overcurrent condition detected interrupt enable. Reset Source: rst_mod_g_rst_n
12	SRP_NOT_COMP_DEV_REMOVED_INT_EN	R/W	0h	Non cmpliant device disconnect interrupt enable Reset Source: rst_mod_g_rst_n
11	SRP_DET_INT_EN	R/W	0h	SRP pulse detected interrupt enable. NOTE: SRP detection can be enabled only if core is enabled to work as a A-device [OTGSTS.OTG_MODE=0] Reset Source: rst_mod_g_rst_n
10	TA_BIDL_ADIS_TMOUT_INT_EN	R/W	0h	No activity from B-Device timeout interrupt enable. Reset Source: rst_mod_g_rst_n
9	TA_AIDL_BDIS_TMOUT_INT_EN	R/W	0h	No response from B-Device for HNP interrupt enable. Reset Source: rst_mod_g_rst_n
8	ADP_PROBE_COMPLETED_INT_EN	R/W	0h	ADP probe completed interrupt enable Reset Source: rst_mod_g_rst_n
7	PROBE_RISE_INT_EN	R/W	0h	ADP probe comparator rise detected interrupt enable Reset Source: rst_mod_g_rst_n
6	SENSE_RISE_INT_EN	R/W	0h	ADP sense comparator rise detected interrupt enable Reset Source: rst_mod_g_rst_n
5	VBUSVALID_FALL_INT_EN	R/W	0h	Vbusvalid fall detected interrupt enable. Reset Source: rst_mod_g_rst_n

Table 14-20925. USB3P0SS_CTRL_DRD_OTGIEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	VBUSVALID_RISE_INT_EN	R/W	0h	Vbusvalid fall detected interrupt enable. Reset Source: rst_mod_g_rst_n
3	OTGSESSVALID_FALL_INT_EN	R/W	0h	Otgsessvalid fall detected interrupt enable. Reset Source: rst_mod_g_rst_n
2	OTGSESSVALID_RISE_INT_EN	R/W	0h	Otgsessvalid rise detected interrupt enable. Reset Source: rst_mod_g_rst_n
1	VBUS_ON_FAILED_INT_EN	R/W	0h	Enabling Vbus by A-Device has failed interrupt enable. Reset Source: rst_mod_g_rst_n
0	ID_CHANGE_INT_EN	R/W	0h	ID change interrupt enable Reset Source: rst_mod_g_rst_n

14.9.2.3.2.24 USB3P0SS_CTRL_DRD_OTGIVECT Register

1 USB3P0SS_CTRL_DRD_OTGIVECT Register (Offset = 24h) [reset = 0h]

OTGIVECT

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Table 14-20926. Instance Table

Instance Name	Physical Address
USB0	**0F40 0024h**

Figure 14-6914. USB3P0SS_CTRL_DRD_OTGIVECT Name Register

31	30	29	28	27	26	25	24
DM_VLGC_COMP_RISE_INT	DCD_COMP_FALL_INT	DCD_COMP_RISE_INT	DP_VDAT_REF_RISE_INT	DM_VDAT_REF_RISE_INT	RID_A_RISE_INT	RID_B_RISE_INT	RID_C_RISE_INT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RID_GND_RISE_INT	RID_FLOAT_RISE_INT	RID_FLOAT_FALL_INT	H_WRST_GEN_CMPL_INT	H_POLLTRY_INT	TIMER_TMOUT_INT	TB_AIDL_BDIS_MIN_TMOUT_INT	TB_ASE0_BRST_TMOUT_INT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SRP_CMPL_INT	SRP_FAIL_INT	OVERCURRENT_INT	SRP_NOT_COMP_DEV_REMOVED_INT	SRP_DET_INT	TA_BIDL_ADIS_TMOUT_INT	TA_AIDL_BDIS_TMOUT_INT	ADP_PROBE_COMPLETED_INT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PROBE_RISE_INT	SENSE_RISE_INT	VBUSVALID_FALL_INT	VBUSVALID_RISE_INT	OTGSESSVALID_FALL_INT	OTGSESSVALID_RISE_INT	VBUS_ON_FAILED_INT	ID_CHANGE_INT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-20928. USB3P0SS_CTRL_DRD_OTGIVECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DM_VLGC_COMP_RISE_INT	R/W1TC	0h	DM VLGC comparator rise detect interrupt Reset Source: rst_mod_g_rst_n
30	DCD_COMP_FALL_INT	R/W1TC	0h	DCD comparator fall detect interrupt Reset Source: rst_mod_g_rst_n
29	DCD_COMP_RISE_INT	R/W1TC	0h	DCD comparator rise detect interrupt Reset Source: rst_mod_g_rst_n
28	DP_VDAT_REF_RISE_INT	R/W1TC	0h	DP VDAT comparator rise detect interrupt Reset Source: rst_mod_g_rst_n
27	DM_VDAT_REF_RISE_INT	R/W1TC	0h	DM VDAT comparator rise detect interrupt Reset Source: rst_mod_g_rst_n
26	RID_A_RISE_INT	R/W1TC	0h	RID A comparator rise detect interrupt Reset Source: rst_mod_g_rst_n
25	RID_B_RISE_INT	R/W1TC	0h	RID B comparator rise detect interrupt Reset Source: rst_mod_g_rst_n

Table 14-20928. USB3P0SS_CTRL_DRD_OTGIVECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	RID_C_RISE_INT	R/W1TC	0h	RID C comparator rise detect interrupt Reset Source: rst_mod_g_rst_n
23	RID_GND_RISE_INT	R/W1TC	0h	RID GND comparator rise detect interrupt Reset Source: rst_mod_g_rst_n
22	RID_FLOAT_RISE_INT	R/W1TC	0h	RID floating comparator rise detect interrupt Reset Source: rst_mod_g_rst_n
21	RID_FLOAT_FALL_INT	R/W1TC	0h	RID floating comparator detect interrupt Reset Source: rst_mod_g_rst_n
20	H_WRST_GEN_CMPL_INT	R/W1TC	0h	Host Warm Reset generation completed interrupt. Reset Source: rst_mod_g_rst_n
19	H_POLLTRY_INT	R/W1TC	0h	Host Polling state entry interrupt. Reset Source: rst_mod_g_rst_n
18	TIMER_TMOUT_INT	R/W1TC	0h	Timer timeout interrupt. Reset Source: rst_mod_g_rst_n
17	TB_AIDL_BDIS_MIN_TMOUT_INT	R/W1TC	0h	The bus has been in Idle state for the required time during HNP interrupt. Reset Source: rst_mod_g_rst_n
16	TB_ASE0_BRST_TMOUT_INT	R/W1TC	0h	No response from A-Device to HNP interrupt. Reset Source: rst_mod_g_rst_n
15	SRP_CMPL_INT	R/W1TC	0h	SRP completed interrupt. Reset Source: rst_mod_g_rst_n
14	SRP_FAIL_INT	R/W1TC	0h	No response from SRP from A-Device interrupt. Reset Source: rst_mod_g_rst_n
13	OVERCURRENT_INT	R/W1TC	0h	Overcurrent condition detected interrupt. Reset Source: rst_mod_g_rst_n
12	SRP_NOT_COMP_DEV_REMOVED_INT	R/W1TC	0h	Not cmpliant device disconnect detect interrupt. Reset Source: rst_mod_g_rst_n
11	SRP_DET_INT	R/W1TC	0h	SRP pulse detected interrupt. Reset Source: rst_mod_g_rst_n
10	TA_BIDL_ADIS_TMOUT_INT	R/W1TC	0h	No activity from B-Device timeout interrupt. Reset Source: rst_mod_g_rst_n
9	TA_AIDL_BDIS_TMOUT_INT	R/W1TC	0h	No response from B-Device for HNP interrupt. Reset Source: rst_mod_g_rst_n
8	ADP_PROBE_COMPLETED_INT	R/W1TC	0h	ADP completed. Status is reported in OTGADPSTS register. Reset Source: rst_mod_g_rst_n
7	PROBE_RISE_INT	R/W1TC	0h	ADP probe comparator rise detected interrupt Reset Source: rst_mod_g_rst_n
6	SENSE_RISE_INT	R/W1TC	0h	ADP sense comparator rise detected interrupt Reset Source: rst_mod_g_rst_n
5	VBUSVALID_FALL_INT	R/W1TC	0h	Vbusvalid fall detected interrupt. Reset Source: rst_mod_g_rst_n
4	VBUSVALID_RISE_INT	R/W1TC	0h	Vbusvalid fall detected interrupt. Reset Source: rst_mod_g_rst_n
3	OTGSESSVALID_FALL_INT	R/W1TC	0h	Otgsessvalid fall detected interrupt. Reset Source: rst_mod_g_rst_n

Table 14-20928. USB3P0SS_CTRL_DRD_OTGIVECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OTGSESSVALID_RISE_INT	R/W1TC	0h	Otgsessvalid rise detected interrupt. Reset Source: rst_mod_g_rst_n
1	VBUS_ON_FAILED_INT	R/W1TC	0h	Enabling Vbus by A-Device has failed. This bit should be cleared before enabling subsequent connection as host. Reset Source: rst_mod_g_rst_n
0	ID_CHANGE_INT	R/W1TC	0h	ID change interrupt Reset Source: rst_mod_g_rst_n

14.9.2.3.2.25 USB3P0SS_CTRL_DRD_CLK_FREQ Register

1 USB3P0SS_CTRL_DRD_CLK_FREQ Register (Offset = 28h) [reset = 200000h]

CLK_FREQ

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Table 14-20929. Instance Table

Instance Name	Physical Address
USB0	0F40 0028h

Figure 14-6915. USB3P0SS_CTRL_DRD_CLK_FREQ Name Register

31	30	29	28	27	26	25	24
CLK_FREQ_KHZ							
R/W							
20h							
23	22	21	20	19	18	17	16
CLK_FREQ_KHZ							
R/W							
20h							
15	14	13	12	11	10	9	8
RSVD1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD1							
R							
0h							

Table 14-20931. USB3P0SS_CTRL_DRD_CLK_FREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLK_FREQ_KHZ	R/W	20h	CLK_FREQ_KHZ defines how many cycles are needed to determine 1 ms clock base for stb_clk_predft. Example: Let's say that stb_clk_predft frequency is 32kHz. With CLK_FREQ_KHZ set to 32 time base would be 32 cycles of 32khz clock which gives 1 ms Reset Source: rst_mod_g_rst_n
15:0	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.26 USB3P0SS_CTRL_DRD_OTGTMR Register

1 USB3P0SS_CTRL_DRD_OTGTMR Register (Offset = 2Ch) [reset = 0h]

OTGTMR

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Table 14-20932. Instance Table

Instance Name	Physical Address
USB0	**0F40 002Ch**

Figure 14-6916. USB3P0SS_CTRL_DRD_OTGTMR Name Register

31	30	29	28	27	26	25	24
ITC_EN	RSVD1						
W	R						
0h	0h						
23	22	21	20	19	18	17	16
RSVD1			TIMER_STOP	TIMER_START	TIMER_WRITE	TIMEOUT_UNITS	
R			W	W	W	W	
0h			0h	0h	0h	0h	
15	14	13	12	11	10	9	8
TIMEOUT_VALUE							
W							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_VALUE							
W							
0h							

Table 14-20934. USB3P0SS_CTRL_DRD_OTGTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ITC_EN	W	0h	ITC ENABLE for device mode 0 - Device IOC and ISP interrupts moderation by OTG_IVECT interrupt from OTGTMR is disabled. 1 - The OTGTMR is used for Device IOC and ISP interrupts moderation. The OTG_IVECT from OTGTMR is not requested. Reset Source: rst_mod_g_rst_n
30:21	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
20	TIMER_STOP	W	0h	Stop timer Reset Source: rst_mod_g_rst_n
19	TIMER_START	W	0h	Start timer Reset Source: rst_mod_g_rst_n
18	TIMER_WRITE	W	0h	Timer value and units write strobe Reset Source: rst_mod_g_rst_n

Table 14-20934. USB3P0SS_CTRL_DRD_OTGTMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	TIMEOUT_UNITS	W	0h	Time units: 0 - hundreds of microseconds [valid only if otg controller clock is in MHz range] 1 - milliseconds 2 - tens of milliseconds 3 - hundreds of milliseconds Valid only if TIMER_WRITE is 1. Reset Source: rst_mod_g_rst_n
15:0	TIMEOUT_VALUE	W	0h	Timeout value for timer. Valid only if TIMER_WRITE is 1. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.27 USB3P0SS_CTRL_DRD_OTGSIMULATE Register

1 USB3P0SS_CTRL_DRD_OTGSIMULATE Register (Offset = 40h) [reset = 0h]

OTGSIMULATE

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Table 14-20935. Instance Table

Instance Name	Physical Address
USB0	**0F40 0040h**

Figure 14-6917. USB3P0SS_CTRL_DRD_OTGSIMULATE Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD1							OTG_CFG_FAST_SIMS
R							R/W
0h							0h

Table 14-20937. USB3P0SS_CTRL_DRD_OTGSIMULATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
0	OTG_CFG_FAST_SIMS	R/W	0h	Debug Feature. This bit is for simulation modes only. It enables reductions to OTG timings. '0': Normal timings '1': Enable fast simulation timing modes This bit should be written '0' in normal operation Reset Source: rst_mod_g_rst_n

14.9.2.3.2.28 USB3P0SS_CTRL_DRD_OVERRIDE Register

1 USB3P0SS_CTRL_DRD_OVERRIDE Register (Offset = 44h) [reset = 0h]

PORT_OVERRIDE register can be written when UTMI clock is disabled, ASF parity-protected: no

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Table 14-20938. Instance Table

Instance Name	Physical Address
USB0	**0F40 0044h**

Figure 14-6918. USB3P0SS_CTRL_DRD_OVERRIDE Name Register

31	30	29	28	27	26	25	24
RSVD3				OVERRIDE_SLEEPM_SFR	OVERRIDE_SLEEPM_SEL	OVERRIDE_SUSPENDM_SFR	OVERRIDE_SUSPENDM_SEL
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OVERRIDE_XCVRSEL_SFR		OVERRIDE_XCVRSEL_SEL	OVERRIDE_TXBITSTUFF_SFR	OVERRIDE_TXBITSTUFF_SEL	OVERRIDE_OPMODE_SFR		OVERRIDE_OPMODE_SEL
R/W		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OVERRIDE_TERMSEL_SFR	OVERRIDE_TERMSEL_SEL	OVERCURRENT_SFR	OVERCURRENT_SEL	SESS_VLD_SFR	SESS_VLD_SEL	IDDIG_SFR	IDDIG_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD2	DRIVE_VBUS_SFR	DRIVE_VBUS_SEL	RSVD1	BC_DMPULLDOWN	BC_DPPULLDOWN	BC_PULLDOWNCTRL	IDPULLUP
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-20940. USB3P0SS_CTRL_DRD_OVERRIDE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RSVD3	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
27	OVERRIDE_SLEEPM_SFR	R/W	0h	SFR sleepm control. Value this bit is passed to PHY sleepm signal. This bit is valid only with PORT_OVERRIDE. override_sleepm_sel set to '1'. Reset Source: rst_mod_g_rst_n
26	OVERRIDE_SLEEPM_SEL	R/W	0h	sleepm override select. This register allows SW driver override sleepm pin as follows: 0: sleepm is controlled from active controller [host/device/none] 1: sleepm controlled from SFR Reset Source: rst_mod_g_rst_n

Table 14-20940. USB3P0SS_CTRL_DRD_OVERRIDE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	OVERRIDE_SUSPENDM_SFR	R/W	0h	SFR suspendm control. Value this bit is passed to PHY suspendm signal. This bit is valid only with PORT_OVERRIDE. override_suspendm_sel set to '1'. Reset Source: rst_mod_g_rst_n
24	OVERRIDE_SUSPENDM_SEL	R/W	0h	suspendm override select. This register allows SW driver override suspendm pin as follows: 0: suspendm is controlled from active controller [host/device/none] 1: suspendm controlled from SFR Reset Source: rst_mod_g_rst_n
23:22	OVERRIDE_XCVRSEL_SFR	R/W	0h	SFR xcvrselect control. Value of these bits is passed to PHY xcvrselect signal. This bit is valid only with PORT_OVERRRIDE. override_opmode_sel set to 1 Reset Source: rst_mod_g_rst_n
21	OVERRIDE_XCVRSEL_SEL	R/W	0h	xcvrselect override select. This register allows SW driver override xcvrselect pin as follows: 0: xcvrselect is controlled from active controller [host/device] 1: xcvrselect controlled from SFR Reset Source: rst_mod_g_rst_n
20	OVERRIDE_TXBITSTUFF_SFR	R/W	0h	SFR txbitstuffenable control. Value this bit is passed to PHY txbitstuffenable signal. This bit is valid only with PORT_OVERRRIDE. override_txbitstuff_sel set to 1. Reset Source: rst_mod_g_rst_n
19	OVERRIDE_TXBITSTUFF_SEL	R/W	0h	txbitstuffenable override select. This register allows SW driver override txbitstuffenable pin as follows: 0: txbitstuffenable is controlled from active controller [host/device] 1: txbitstuffenable controlled from SFR Reset Source: rst_mod_g_rst_n
18:17	OVERRIDE_OPMODE_SFR	R/W	0h	SFR opmode control. Value these bits is passed to PHY opmode signal. This bit is valid only with PORT_OVERRRIDE. override_opmode_sel set to 1. Reset Source: rst_mod_g_rst_n
16	OVERRIDE_OPMODE_SEL	R/W	0h	opmode override select. This register allows SW driver override opmode pin as follows: 0: opmode is controlled from active controller [host/device] 1: opmode controlled from SFR Reset Source: rst_mod_g_rst_n
15	OVERRIDE_TERMSEL_SFR	R/W	0h	SFR overcurrent control. 0: overcurrent = 0 1: overcurrent = 1 This bit is valid only with PORT_OVERRRIDE.overcurrent_sel set to '1'. Note: overcurrent active state is low. Reset Source: rst_mod_g_rst_n
14	OVERRIDE_TERMSEL_SEL	R/W	0h	termselect override select. This register allows SW driver override termselect pin as follows: 0: txbitstuffenable is controlled from active controller [host/device] 1: txbitstuffenable controlled from SFR Reset Source: rst_mod_g_rst_n

Table 14-20940. USB3P0SS_CTRL_DRD_OVERRIDE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	OVERCURRENT_SFR	R/W	0h	SFR termselect control. Value this bit is passed to PHY termselect signal. This bit is valid only with PORT_OVERRRIDE. override_termsel_sel set to 1. Reset Source: rst_mod_g_rst_n
12	OVERCURRENT_SEL	R/W	0h	Overcurrent override select This register allows SW driver override overcurrent pin as follows: 0: overcurrent is controlled from external FAULT detector 1: overcurrent controlled from SFR Reset Source: rst_mod_g_rst_n
11	SESS_VLD_SFR	R/W	0h	SFR Vbusvalid/Sessvalid control. 0: Vbusvalid/Sessvalid = 0 1: Vbusvalid/Sessvalid = 1 This bit is valid only with PORT_OVERRRIDE.sess_vld_sel set to '1'. Reset Source: rst_mod_g_rst_n
10	SESS_VLD_SEL	R/W	0h	Vbusvalid/Sessvalid override select. This register allows SW driver override Vbusvalid/Sessvalid pins as follows: 0: Vbusvalid/Sessvalid are controlled from OTG PHY 1: Vbusvalid/Sessvalid are controlled from SFR Reset Source: rst_mod_g_rst_n
9	IDDIG_SFR	R/W	0h	SFR iddig control. 0: iddig = 0 1: iddig = 1 This bit is valid only with PORT_OVERRRIDE.iddig_sel set to '1'. Reset Source: rst_mod_g_rst_n
8	IDDIG_SEL	R/W	0h	IDDIG override select. This register allows SW driver override iddig pin as follows: 0: iddig is controlled from OTG PHY 1: iddig controlled from SFR Reset Source: rst_mod_g_rst_n
7	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
6	DRIVE_VBUS_SFR	R/W	0h	0: drive_vbus = 0 1: drive_vbus = 1 This bit is valid only with USB2_PORT_OVERRRIDE.drive_vbus_sel set to '1'. This bit is auto-cleared upon over-current condition. Over-current doesn't disable vbus forcing. Reset Source: rst_mod_g_rst_n
5	DRIVE_VBUS_SEL	R/W	0h	This register allows SW driver take control over drive_vbus as follows: 0: drive_vbus controlled from OTG controller 1: drive_vbus controlled from SFR Reset Source: rst_mod_g_rst_n
4	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-20940. USB3P0SS_CTRL_DRD_OVERRIDE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BC_DMPULLDOWN	R/W	0h	dmpulldown enable This bit is valid only with PORT_OVERRRIDE.pulldownctrl_sel set to 1 Reset Source: rst_mod_g_rst_n
2	BC_DPPULLDOWN	R/W	0h	BC dppulldown enable This bit is valid only with PORT_OVERRRIDE.pulldownctrl_sel set to 1 Reset Source: rst_mod_g_rst_n
1	BC_PULLDOWNCTRL	R/W	0h	pulldowncotrol 1: puldowns are controlled by dppulldown_sfr and dmpulldown_sfr 0: puldowns are controlled by OTG Reset Source: rst_mod_g_rst_n
0	IDPULLUP	R/W	0h	ID Pin Sample Enable: Active High. Signal that enables the sampling of the analog ID line. 0: Sampling of ID pin is disabled, iddig is not valid 1: Sampling of ID pin is enabled Reset Source: rst_mod_g_rst_n

14.9.2.3.2.29 USB3P0SS_CTRL_DRD_SUSP_CTRL Register

1 USB3P0SS_CTRL_DRD_SUSP_CTRL Register (Offset = 48h) [reset = 80310h]

SUSP_TIMING_CTRL. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes. This is a configuration only register, therefore it can be changed by Software only during configuration phase when Power-On Reset (pwrup_rst_n) is asserted. ASF parity-protected: no

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Table 14-20941. Instance Table

Instance Name	Physical Address
USB0	**0F40 0048h**

Figure 14-6919. USB3P0SS_CTRL_DRD_SUSP_CTRL Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD1				SUSPEND_DELAY_CAPABILITY	SLEEP_RESIDENCY_ENABLE	SUSPEND_RESIDENCY_ENABLE	SUSPEND_DELAY_ENABLE
R				R	R/W	R/W	R/W
0h				1h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SUSPEND_RESIDENCY							
R/W							
3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUSPEND_DELAY							
R/W							
10h							

Table 14-20943. USB3P0SS_CTRL_DRD_SUSP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
19	SUSPEND_DELAY_CAPABILITY	R	1h	Suspend delay capability. This is a configuration only field, therefore it can be changed by Software only during configuration phase when Power-On Reset [pwrup_rst_n] is asserted. Reset Source: rst_mod_g_rst_n
18	SLEEP_RESIDENCY_ENABLE	R/W	0h	sleep minimum residency enable. This is a configuration only field, therefore it can be changed by Software only during configuration phase when Power-On Reset [pwrup_rst_n] is asserted. Reset Source: rst_mod_g_rst_n

Table 14-20943. USB3P0SS_CTRL_DRD_SUSP_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	SUSPEND_RESIDENCY_ENABLE	R/W	0h	suspend minimum residency enable. This is a configuration only field, therefore it can be changed by Software only during configuration phase when Power-On Reset [pwrup_rst_n] is asserted. Reset Source: rst_mod_g_rst_n
16	SUSPEND_DELAY_ENABLE	R/W	0h	suspend delay enable. This is a configuration only field, therefore it can be changed by Software only during configuration phase when Power-On Reset [pwrup_rst_n] is asserted. Reset Source: rst_mod_g_rst_n
15:8	SUSPEND_RESIDENCY	R/W	3h	Suspend/Sleep minimum residency time [us]. This is a configuration only field, therefore it can be changed by Software only during configuration phase when Power-On Reset [pwrup_rst_n] is asserted. Reset Source: rst_mod_g_rst_n
7:0	SUSPEND_DELAY	R/W	10h	Suspend assertion delay time [us]. This is a configuration only field, therefore it can be changed by Software only during configuration phase when Power-On Reset [pwrup_rst_n] is asserted. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.30 USB3P0SS_CTRL_DRD_PHYRST_CFG Register

1 USB3P0SS_CTRL_DRD_PHYRST_CFG Register (Offset = 4Ch) [reset = E00h]

USB20 PHY reset workaround config ASF parity-protected: no

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Table 14-20944. Instance Table

Instance Name	Physical Address
USB0	**0F40 004Ch**

Figure 14-6920. USB3P0SS_CTRL_DRD_PHYRST_CFG Name Register

31	30	29	28	27	26	25	24
RSVD3							PHYRST_SFR_RST
R							R/W
0h							0h
23	22	21	20	19	18	17	16
RSVD2							
R							
0h							
15	14	13	12	11	10	9	8
RSVD2			PHYRST_A_VALUE				
R			R/W				
0h			Eh				
7	6	5	4	3	2	1	0
RSVD1				PHYRST_D_ENABLE	PHYRST_C_ENABLE	PHYRST_B_ENABLE	PHYRST_A_ENABLE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-20946. USB3P0SS_CTRL_DRD_PHYRST_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RSVD3	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
24	PHYRST_SFR_RST	R/W	0h	Software USB20 PHy reset: 0 - SW utmi_reset not asserted 1 - SW utmi_reset asserted Reset Source: rst_mod_g_rst_n
23:13	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-20946. USB3P0SS_CTRL_DRD_PHYRST_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:8	PHYRST_A_VALUE	R/W	Eh	phyrst_a Rx fail timeout value. Value of this register is used as a timeout value for detecting Rx fail [utmi_rxactive is not up during Rx] Value of this register represent maximum number of UTMI clock cycles where utmi_rxactive is expected to rise with respect to Rx start judged by non-idle state utmi_linestate Reset Source: rst_mod_g_rst_n
7:4	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
3	PHYRST_D_ENABLE	R/W	0h	Reset PHY after each utmi_opmode change from 2'b10 to any other value: 0 - disabled 1 - enabled Reset Source: rst_mod_g_rst_n
2	PHYRST_C_ENABLE	R/W	0h	Reset PHY after each utmi_opmode change from 2'b01 to any other value: 0 - disabled 1 - enabled Reset Source: rst_mod_g_rst_n
1	PHYRST_B_ENABLE	R/W	0h	Reset PHY after each transmitted packet in High-Speed: 0 - disabled 1 - enabled Reset Source: rst_mod_g_rst_n
0	PHYRST_A_ENABLE	R/W	0h	Reset PHY if Rx fail is detected: 0 - disabled 1 - enabled Reset Source: rst_mod_g_rst_n

14.9.2.3.2.31 USB3P0SS_CTRL_DRD_OTGANASTS Register

1 USB3P0SS_CTRL_DRD_OTGANASTS Register (Offset = 50h) [reset = 0h]

OTGADPBCSTS

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Table 14-20947. Instance Table

Instance Name	Physical Address
USB0	**0F40 0050h**

Figure 14-6921. USB3P0SS_CTRL_DRD_OTGANASTS Name Register

31	30	29	28	27	26	25	24
RSVD2							ADP_CHRG_TMOUT_DET
R							R
0h							0h
23	22	21	20	19	18	17	16
RSVD1			RID_A	RID_B	RID_C	RID_GND	RID_FLOAT
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
LINESTATE		IDDIG	RID_A_COMP_STS	RID_B_COMP_STS	RID_C_COMP_STS	RID_GND_COMP_STS	RID_FLOAT_COMP_STS
R		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SESSEND	ADP_SENSE_ANA	ADP_PROBE_ANA	OTGSESSVALID	DCD_COMP_STS	DM_VLGC_COMP_STS	DM_VDAT_REF_COMP_STS	DP_VDAT_REF_COMP_STS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-20949. USB3P0SS_CTRL_DRD_OTGANASTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
24	ADP_CHRG_TMOUT_DET	R	0h	ADP charge timeout detected Reset Source: rst_mod_g_rst_n
23:21	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
20	RID_A	R	0h	RID A status reg Reset Source: rst_mod_g_rst_n
19	RID_B	R	0h	RID B status reg Reset Source: rst_mod_g_rst_n

Table 14-20949. USB3P0SS_CTRL_DRD_OTGANASTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	RID_C	R	0h	RID C status reg Reset Source: rst_mod_g_rst_n
17	RID_GND	R	0h	RID GND status reg Reset Source: rst_mod_g_rst_n
16	RID_FLOAT	R	0h	RID float status reg Reset Source: rst_mod_g_rst_n
15:14	LINESTATE	R	0h	Line State: These signals reflect the current state of the single ended receivers. They are combinatorial until a 'usable' sieclock is available, then they are synchronized to sieclock. They reflect the current state of the DP [linestate [0]] and DM [linestate [1]] signals. 00: SE0 [Single Ended Zero] 01: 'J' State 10: 'K' State 11: SE1 [Single Ended One] Reset Source: rst_mod_g_rst_n
13	IDDIG	R	0h	ID Pin Status: Indicates whether the connected USB plug is Micro-A or Micro-B. This is only valid when idpullup is set to '1'. It must be valid within 50ms after idpullup is set to '1'. 0: Connected plug is a Micro-A 1: Connected plug is a Micro-B Reset Source: rst_mod_g_rst_n
12	RID_A_COMP_STS	R	0h	RID A comparator status 1: RID_A Detected on ID Pin 0: RID_A not Detected on ID Pin Reset Source: rst_mod_g_rst_n
11	RID_B_COMP_STS	R	0h	RID B comparator status 1: RID_B Detected on ID Pin 0: RID_B not Detected on ID Pin Reset Source: rst_mod_g_rst_n
10	RID_C_COMP_STS	R	0h	RID C comparator status 1: RID_C Detected on ID Pin 0: RID_C not Detected on ID Pin Reset Source: rst_mod_g_rst_n
9	RID_GND_COMP_STS	R	0h	RID GND comparator status 1: RID_GND Detected on ID Pin 0: RID_GND not Detected on ID Pin Reset Source: rst_mod_g_rst_n
8	RID_FLOAT_COMP_STS	R	0h	RID float comparator status 1: RID_FLOAT Detected on ID Pin 0: RID_FLOAT not Detected on ID Pin Reset Source: rst_mod_g_rst_n
7	SESSEND	R	0h	VBUS Valid: Indicates if the voltage on VBUS is at a valid level for operation [4.4V less than VTH less than 4.75V]. 0: VBUS less than 4.4V 1: VBUS > 4.75V Reset Source: rst_mod_g_rst_n
6	ADP_SENSE_ANA	R	0h	Output of ADP Sense Comparator. 0: VBUS less than 0.2V 1: VBUS > 0.55V Reset Source: rst_mod_g_rst_n

Table 14-20949. USB3P0SS_CTRL_DRD_OTGANASTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ADP_PROBE_ANA	R	0h	Output of ADP Probe Comparator. 0: VBUS less than 0.6V 1: VBUS > 0.75V Reset Source: rst_mod_g_rst_n
4	OTGSESSVALID	R	0h	B-Peripheral is Valid: Indicates if the session for a B-Peripheral is valid [0.8V less than VTH less than 4.0V]. The signal bvalid from OTG 1.3 is now renamed as otgsessvalid. 0: VBUS less than 0.8V 1: VBUS > 4.0V Reset Source: rst_mod_g_rst_n
3	DCD_COMP_STS	R	0h	Data Contact Detect [DCD] Comparator Status 1: DP line is asserted 0: DP line is not asserted Reset Source: rst_mod_g_rst_n
2	DM_VLGC_COMP_STS	R	0h	1: DM > VLGC Detected 0: DM less than VLGC Detected Note: This status shall be re-used from the single ended receiver output of D- whenever dm_vlgc_comp_en is '1'. Reset Source: rst_mod_g_rst_n
1	DM_VDAT_REF_COMP_STS	R	0h	1: DM > VDAT_REF Detected 0: DM less than VDAT_REF Detected Note: This status shall be re-used from the single ended receiver output of D- whenever dm_vdat_ref_comp_en is '1'. Reset Source: rst_mod_g_rst_n
0	DP_VDAT_REF_COMP_STS	R	0h	1: DP > VDAT_REF Detected 0: DP less than VDAT_REF Detected Note: This status shall be re-used from the single ended receiver output of D+ whenever dp_vdat_ref_comp_en is '1'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.32 USB3P0SS_CTRL_DRD_ADP_RAMP_TIME Register

1 USB3P0SS_CTRL_DRD_ADP_RAMP_TIME Register (Offset = 54h) [reset = 0h]

ADP_RAMP_TIME

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Table 14-20950. Instance Table

Instance Name	Physical Address
USB0	**0F40 0054h**

Figure 14-6922. USB3P0SS_CTRL_DRD_ADP_RAMP_TIME Name Register

31	30	29	28	27	26	25	24
ADP_RAMP_TIME							
R							
0h							
23	22	21	20	19	18	17	16
ADP_RAMP_TIME							
R							
0h							
15	14	13	12	11	10	9	8
ADP_RAMP_TIME							
R							
0h							
7	6	5	4	3	2	1	0
ADP_RAMP_TIME							
R							
0h							

Table 14-20952. USB3P0SS_CTRL_DRD_ADP_RAMP_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADP_RAMP_TIME	R	0h	ADP ramp time measurement value. Software should read this register upon ADP_PROBE_COMPLETED_INT_EN interrupt detection Reset Source: rst_mod_g_rst_n

14.9.2.3.2.33 USB3P0SS_CTRL_DRD_OTGCTRL1 Register

1 USB3P0SS_CTRL_DRD_OTGCTRL1 Register (Offset = 58h) [reset = 0h]

OTGCTRL1

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Table 14-20953. Instance Table

Instance Name	Physical Address
USB0	**0F40 0058h**

Figure 14-6923. USB3P0SS_CTRL_DRD_OTGCTRL1 Name Register

31	30	29	28	27	26	25	24
RSVD2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD2			RID_NONFLOAT_COMP_EN	RID_FLOAT_COMP_EN	DP_VDAT_REF_COMP_EN	DM_VLGC_COMP_EN	DM_VDAT_REF_COMP_EN
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD1		VDP_SRC_EN	VDM_SRC_EN	IDP_SRC_EN	IDP_SINK_EN	IDM_SINK_EN	BC_EN
R		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADP_AUTO	DO_ADP_SNS	DO_ADP_PRB	ADP_SOURCE_CURRENT_EN	ADP_SINK_CURRENT_EN	ADP_SENSE_EN	ADP_PROBE_EN	ADP_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-20955. USB3P0SS_CTRL_DRD_OTGCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
20	RID_NONFLOAT_COMP_EN	R/W	0h	1: RID Non-Float Comparator Enabled 0: RID Non-Float Comparator Disabled Note: This ID Comparator enable is used to detect the presence of RID_A or RID_B or RID_C or RID_GND when the ID pin is non-floating. Reset Source: rst_mod_g_rst_n
19	RID_FLOAT_COMP_EN	R/W	0h	1: RID Float Comparator Enabled 0: RID Float Comparator Disabled Note: This ID Comparator enable is used to detect whether the ID line is floating or non-floating. If it is identified to be non-floating, then rid_nonfloat_comp_en is enabled to check for RID_A or RID_B or RID_C or RID_GND. Reset Source: rst_mod_g_rst_n

Table 14-20955. USB3P0SS_CTRL_DRD_OTGCTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	DP_VDAT_REF_COMP_EN	R/W	0h	1: DP to VDAT_REF Comparator Enabled 0: DP to VDAT_REF Comparator Disabled Reset Source: rst_mod_g_rst_n
17	DM_VLGC_COMP_EN	R/W	0h	1: DM to VLGC Comparator Enabled 0: DM to VLGC Comparator Disabled Reset Source: rst_mod_g_rst_n
16	DM_VDAT_REF_COMP_EN	R/W	0h	1: DM to VDAT_REF Comparator Enabled 0: DM to VDAT_REF Comparator Disabled Reset Source: rst_mod_g_rst_n
15:14	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
13	VDP_SRC_EN	R/W	0h	1: Voltage Source on DP Enabled 0: Voltage Source on DP Disabled Reset Source: rst_mod_g_rst_n
12	VDM_SRC_EN	R/W	0h	1: Voltage Source on DM Enabled 0: Voltage Source on DM Disabled Reset Source: rst_mod_g_rst_n
11	IDP_SRC_EN	R/W	0h	1: Current Source on DP Enabled 0: Current Source on DP Disabled Reset Source: rst_mod_g_rst_n
10	IDP_SINK_EN	R/W	0h	1: Current Sink on DP Enabled 0: Current Sink on DP Disabled Reset Source: rst_mod_g_rst_n
9	IDM_SINK_EN	R/W	0h	1: Current Sink on DM Enabled 0: Current Sink on DM Disabled Reset Source: rst_mod_g_rst_n
8	BC_EN	R/W	0h	Battery Charging Circuits Master Enable. 1: BC Enabled 0: BC Disabled Reset Source: rst_mod_g_rst_n
7	ADP_AUTO	R/W	0h	ADP mode. If set to 1 ADP probing is controlled by internal FSM. If set to 0 then software should control ADP sequence. Reset Source: rst_mod_g_rst_n
6	DO_ADP_SNS	R/W	0h	ADP sensing enable in automated mode Reset Source: rst_mod_g_rst_n
5	DO_ADP_PRB	R/W	0h	ADP probing enable in automated mode Reset Source: rst_mod_g_rst_n
4	ADP_SOURCE_CURRENT_EN	R/W	0h	When this signal is high, VBUS is charged to the probe threshold [0.75V]. This signal should be asserted 5us after the assertion of adp_en. 0: ADP Source Current Enable OFF 1: ADP Source Current Enable ON Reset Source: rst_mod_g_rst_n

Table 14-20955. USB3P0SS_CTRL_DRD_OTGCTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ADP_SINK_CURRENT_EN	R/W	0h	When this signal is high, VBUS is discharged to ground. This signal should be asserted 5us after the assertion of adp_en. 0: ADP Sink Current Enable OFF 1: ADP Sink Current Enable ON Reset Source: rst_mod_g_rst_n
2	ADP_SENSE_EN	R/W	0h	This signal enables the probe mode of the ADP. During this mode, sense comparators and the current sources will be ON based on the source and sink current enables. 0: ADP Probe Sense OFF 1: ADP Probe Sense ON Reset Source: rst_mod_g_rst_n
1	ADP_PROBE_EN	R/W	0h	This signal enables the probe mode of the ADP. During this mode, probe comparators and the current sources will be ON based on the source and sink current enables. 0: ADP Probe Mode OFF 1: ADP Probe Mode ON Reset Source: rst_mod_g_rst_n
0	ADP_EN	R/W	0h	ADP Feature Enable. This signal is the master enable for all the ADP PHY logics. 0: ADP Logics are powered OFF 1: ADP Logics are powered ON Reset Source: rst_mod_g_rst_n

14.9.2.3.2.34 USB3P0SS_CTRL_DRD_OTGCTRL2 Register

1 USB3P0SS_CTRL_DRD_OTGCTRL2 Register (Offset = 5Ch) [reset = 420C8AFh]

OTGCTRL2

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Table 14-20956. Instance Table

Instance Name	Physical Address
USB0	**0F40 005Ch**

Figure 14-6924. USB3P0SS_CTRL_DRD_OTGCTRL2 Name Register

31	30	29	28	27	26	25	24
T_ADP_DSCHG							
R/W							
4h							
23	22	21	20	19	18	17	16
ADP_CHRG_TMOUT							
R/W							
20h							
15	14	13	12	11	10	9	8
TB_ADP_PRB							
R/W							
C8h							
7	6	5	4	3	2	1	0
TA_ADP_PRB							
R/W							
AFh							

Table 14-20958. USB3P0SS_CTRL_DRD_OTGCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	T_ADP_DSCHG	R/W	4h	ADP probing discharge time. T_ADP_DSCHG = {reg_value} * 1 ms Reset Source: rst_mod_g_rst_n
23:16	ADP_CHRG_TMOUT	R/W	20h	ADP probing timeout value. Defines maximum time for ADP charging. If this time is reached during charging then adp_chrg_tmout_det bit in OTGADPBCSTS is set ADP_CHRG_TMOUT = {reg_value} * 1 ms Reset Source: rst_mod_g_rst_n
15:8	TB_ADP_PRB	R/W	C8h	B-device ADP probing period. TB_ADP_PRB = {reg_value} * 10 ms Reset Source: rst_mod_g_rst_n
7:0	TA_ADP_PRB	R/W	AFh	A-device ADP probing period. TA_ADP_PRB = {reg_value} * 10 ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.35 USB3P0SS_CTRL_DRD_VBUSVALID_DBNC_CFG Register

1 USB3P0SS_CTRL_DRD_VBUSVALID_DBNC_CFG Register (Offset = 60h) [reset = 800A000Ah]

VBUSVALID_DBNC_CFG ASF parity-protected: no

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Table 14-20959. Instance Table

Instance Name	Physical Address
USB0	**0F40 0060h**

Figure 14-6925. USB3P0SS_CTRL_DRD_VBUSVALID_DBNC_CFG Name Register

31	30	29	28	27	26	25	24
VBUSVALID_DBNC_DIS	RSVD2					VBUSVALID_FALL_DBNC_VAL	
R/W	R					R/W	
1h	0h					Ah	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VBUSVALID_FALL_DBNC_VAL							
R/W							
Ah							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD1						VBUSVALID_RISE_DBNC_VAL	
R						R/W	
0h						Ah	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBUSVALID_RISE_DBNC_VAL							
R/W							
Ah							

Table 14-20961. USB3P0SS_CTRL_DRD_VBUSVALID_DBNC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VBUSVALID_DBNC_DIS	R/W	1h	Vbusvalid debounce disable Reset Source: rst_mod_g_rst_n
30:26	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
25:16	VBUSVALID_FALL_DBNC_VAL	R/W	Ah	Vbusvalid off debounce: Debounce timer value = reg value x 100us Reset Source: rst_mod_g_rst_n
15:10	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
9:0	VBUSVALID_RISE_DBNC_VAL	R/W	Ah	Vbusvalid on debounce: Debounce timer value = reg value x 100us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.36 USB3P0SS_CTRL_DRD_SESSVALID_DBNC_CFG Register

1 USB3P0SS_CTRL_DRD_SESSVALID_DBNC_CFG Register (Offset = 64h) [reset = 800A0100h]

SESSVALID_DBNC_CFG ASF parity-protected: no

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Table 14-20962. Instance Table

Instance Name	Physical Address
USB0	**0F40 0064h**

Figure 14-6926. USB3P0SS_CTRL_DRD_SESSVALID_DBNC_CFG Name Register

31	30	29	28	27	26	25	24
SESSVALID_DBNC_DIS	RSVD2					SESSVALID_OFF_DBNC_VAL	
R/W	R					R/W	
1h	0h					Ah	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SESSVALID_OFF_DBNC_VAL							
R/W							
Ah							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD1						SESSVALID_ON_DBNC_VAL	
R						R/W	
0h						100h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SESSVALID_ON_DBNC_VAL							
R/W							
100h							

Table 14-20964. USB3P0SS_CTRL_DRD_SESSVALID_DBNC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SESSVALID_DBNC_DIS	R/W	1h	Sessvalid debounce disable Reset Source: rst_mod_g_rst_n
30:26	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
25:16	SESSVALID_OFF_DBNC_VAL	R/W	Ah	Sessvalid off debounce: Debounce timer value = reg value x 100us Reset Source: rst_mod_g_rst_n
15:10	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
9:0	SESSVALID_ON_DBNC_VAL	R/W	100h	Sessvalid on debounce: Debounce timer value = reg value x 100us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.37 USB3P0SS_CTRL_DRD_IDDIG_DBNC_CFG Register

1 USB3P0SS_CTRL_DRD_IDDIG_DBNC_CFG Register (Offset = 68h) [reset = 800A000Ah]

IDDIG_DBNC_CFG ASF parity-protected: no

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Table 14-20965. Instance Table

Instance Name	Physical Address
USB0	**0F40 0068h**

Figure 14-6927. USB3P0SS_CTRL_DRD_IDDIG_DBNC_CFG Name Register

31	30	29	28	27	26	25	24
IDDIG_DBNC_DIS	RSVD2					IDDIG_OFF_DBNC_VAL	
R/W	R					R/W	
1h	0h					Ah	
23	22	21	20	19	18	17	16
IDDIG_OFF_DBNC_VAL							
R/W							
Ah							
15	14	13	12	11	10	9	8
RSVD1						IDDIG_ON_DBNC_VAL	
R						R/W	
0h						Ah	
7	6	5	4	3	2	1	0
IDDIG_ON_DBNC_VAL							
R/W							
Ah							

Table 14-20967. USB3P0SS_CTRL_DRD_IDDIG_DBNC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDDIG_DBNC_DIS	R/W	1h	Iddig debounce disable Reset Source: rst_mod_g_rst_n
30:26	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
25:16	IDDIG_OFF_DBNC_VAL	R/W	Ah	Sessvalid off debounce: Debounce timer value = reg value x 100us Reset Source: rst_mod_g_rst_n
15:10	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
9:0	IDDIG_ON_DBNC_VAL	R/W	Ah	Sessvalid on debounce: Debounce timer value = reg value x 100us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.38 USB3P0SS_CTRL_DRD_DB_ASF_MEM_MASK Register

1 USB3P0SS_CTRL_DRD_DB_ASF_MEM_MASK Register (Offset = 8Ch) [reset = FFFFFFFFh]

Cadence Device ID Register ASF parity-protected: no

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Table 14-20968. Instance Table

Instance Name	Physical Address
USB0	**0F40 008Ch**

Figure 14-6928. USB3P0SS_CTRL_DRD_DB_ASF_MEM_MASK Name Register

31	30	29	28	27	26	25	24
DB_ASF_MEM_MASK							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
DB_ASF_MEM_MASK							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
DB_ASF_MEM_MASK							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
DB_ASF_MEM_MASK							
R/W							
FFFFFFFFh							

Table 14-20970. USB3P0SS_CTRL_DRD_DB_ASF_MEM_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DB_ASF_MEM_MASK	R/W	FFFFFFFFh	Debug Feature. 0-DISABLE/1-ENABLE ECC check for memories Reset Source: rst_mod_g_rst_n

14.9.2.3.2.39 USB3P0SS_CTRL_ASF_ASF_INT_STATUS Register

1 USB3P0SS_CTRL_ASF_ASF_INT_STATUS Register (Offset = 0h) [reset = 0h]

ASF Interrupt Status Register. This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_fatal or asf_nonfatal signal will be asserted. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register. ASF parity-protected: no

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Table 14-20971. Instance Table

Instance Name	Physical Address
USB0	**0F40 0000h**

Figure 14-6929. USB3P0SS_CTRL_ASF_ASF_INT_STATUS Name Register

31	30	29	28	27	26	25	24
RSVD2							
R							
0h							
23	22	21	20	19	18	17	16
RSVD2							
R							
0h							
15	14	13	12	11	10	9	8
RSVD2							
R							
0h							
7	6	5	4	3	2	1	0
RSVD2			ASF_TRANS_TO_ERR	RSVD1		ASF_SRAM_UNCORR_ERR	ASF_SRAM_CORR_ERR
R			R/W1TC	R		R/W1TC	R/W1TC
0h			0h	0h		0h	0h

Table 14-20973. USB3P0SS_CTRL_ASF_ASF_INT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4	ASF_TRANS_TO_ERR	R/W1TC	0h	Transaction timeouts error interrupt Reset Source: rst_mod_g_rst_n
3:2	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	ASF_SRAM_UNCORR_ERR	R/W1TC	0h	SRAM uncorrectable error interrupt Reset Source: rst_mod_g_rst_n

Table 14-20973. USB3P0SS_CTRL_ASF_ASF_INT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASF_SRAM_CORR_ERR	R/W1TC	0h	SRAM correctable error interrupt Reset Source: rst_mod_g_rst_n

14.9.2.3.2.40 USB3P0SS_CTRL_ASF_ASF_INT_RAW_STATUS Register

1 USB3P0SS_CTRL_ASF_ASF_INT_RAW_STATUS Register (Offset = 4h) [reset = 0h]

ASF Interrupt Raw Status Register. A bit set in this raw register indicates a source of ASF fault in the correspoding feature. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrrupt status test register. ASF parity-protected: no

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Table 14-20974. Instance Table

Instance Name	Physical Address
USB0	**0F40 0004h**

Figure 14-6930. USB3P0SS_CTRL_ASF_ASF_INT_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RSVD2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD2			ASF_TRANS_TO_ERR	RSVD1		ASF_SRAM_UNCORR_ERR	ASF_SRAM_CORR_ERR
R			R/W1TC	R		R/W1TC	R/W1TC
0h			0h	0h		0h	0h

Table 14-20976. USB3P0SS_CTRL_ASF_ASF_INT_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4	ASF_TRANS_TO_ERR	R/W1TC	0h	Transaction timeouts error interrupt Reset Source: rst_mod_g_rst_n
3:2	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	ASF_SRAM_UNCORR_ERR	R/W1TC	0h	SRAM uncorrectable error interrupt Reset Source: rst_mod_g_rst_n

Table 14-20976. USB3P0SS_CTRL_ASF_ASF_INT_RAW_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASF_SRAM_CORR_ERR	R/W1TC	0h	SRAM correctable error interrupt Reset Source: rst_mod_g_rst_n

14.9.2.3.2.41 USB3P0SS_CTRL_ASF_ASF_INT_MASK Register

1 USB3P0SS_CTRL_ASF_ASF_INT_MASK Register (Offset = 8h) [reset = 13h]

The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt status register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt. ASF parity-protected: yes (only byte 0 protected)

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Table 14-20977. Instance Table

Instance Name	Physical Address
USB0	**0F40 0008h**

Figure 14-6931. USB3P0SS_CTRL_ASF_ASF_INT_MASK Name Register

31	30	29	28	27	26	25	24
RSVD2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD2			ASF_TRANS_TO_ERR_MASK	RSVD1		ASF_SRAM_UNCORR_ERR_MASK	ASF_SRAM_CORR_ERR_MASK
R			R/W	R		R/W	R/W
0h			1h	0h		1h	1h

Table 14-20979. USB3P0SS_CTRL_ASF_ASF_INT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4	ASF_TRANS_TO_ERR_MASK	R/W	1h	Mask bit for transaction timeouts error interrupt. Reset Source: rst_mod_g_rst_n
3:2	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	ASF_SRAM_UNCORR_ERR_MASK	R/W	1h	Mask bit for SRAM uncorrectable error interrupt. Reset Source: rst_mod_g_rst_n

Table 14-20979. USB3P0SS_CTRL_ASF_ASF_INT_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASF_SRAM_CORR_ERR_MASK	R/W	1h	Mask bit for SRAM correctable error interrupt. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.42 USB3P0SS_CTRL_ASF_ASF_INT_TEST Register

1 USB3P0SS_CTRL_ASF_ASF_INT_TEST Register (Offset = Ch) [reset = 0h]

The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) status registers according to mask and will generate interrrupt accordingly. ASF parity-protected: no

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Table 14-20980. Instance Table

Instance Name	Physical Address
USB0	**0F40 000Ch**

Figure 14-6932. USB3P0SS_CTRL_ASF_ASF_INT_TEST Name Register

31	30	29	28	27	26	25	24
RSVD2							
R							
0h							
23	22	21	20	19	18	17	16
RSVD2							
R							
0h							
15	14	13	12	11	10	9	8
RSVD2							
R							
0h							
7	6	5	4	3	2	1	0
RSVD2			ASF_TRANS_TO_ERR_TEST	RSVD1		ASF_SRAM_UNCORR_ERR_TEST	ASF_SRAM_CORR_ERR_TEST
R			W	R		W	W
0h			0h	0h		0h	0h

Table 14-20982. USB3P0SS_CTRL_ASF_ASF_INT_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4	ASF_TRANS_TO_ERR_TEST	W	0h	Test bit for transaction timeouts error interrupt. Reset Source: rst_mod_g_rst_n
3:2	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	ASF_SRAM_UNCORR_ERR_TEST	W	0h	Test bit for SRAM uncorrectable error interrupt. Reset Source: rst_mod_g_rst_n

Table 14-20982. USB3P0SS_CTRL_ASF_ASF_INT_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASF_SRAM_CORR_ERR_TEST	W	0h	Test bit for SRAM correctable error interrupt. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.43 USB3P0SS_CTRL_ASF_ASF_FATAL_NONFATAL_SELECT Register

1 USB3P0SS_CTRL_ASF_ASF_FATAL_NONFATAL_SELECT Register (Offset = 10h) [reset = 13h]

The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered. ASF parity-protected: yes (only byte 0 protected)

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Table 14-20983. Instance Table

Instance Name	Physical Address
USB0	**0F40 0010h**

Figure 14-6933. USB3P0SS_CTRL_ASF_ASF_FATAL_NONFATAL_SELECT Name Register

31	30	29	28	27	26	25	24
RSVD2							
R							
0h							
23	22	21	20	19	18	17	16
RSVD2							
R							
0h							
15	14	13	12	11	10	9	8
RSVD2							
R							
0h							
7	6	5	4	3	2	1	0
RSVD2			ASF_TRANS_TO_ERR	RSVD1		ASF_SRAM_UNCORR_ERR	ASF_SRAM_CORR_ERR
R			R/W	R		R/W	R/W
0h			1h	0h		1h	1h

Table 14-20985. USB3P0SS_CTRL_ASF_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4	ASF_TRANS_TO_ERR	R/W	1h	Enable transaction timeouts error interrupt as fatal. Reset Source: rst_mod_g_rst_n
3:2	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	ASF_SRAM_UNCORR_ERR	R/W	1h	Enable SRAM uncorrectable error interrupt as fatal. Reset Source: rst_mod_g_rst_n

Table 14-20985. USB3P0SS_CTRL_ASF_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASF_SRAM_CORR_ERR	R/W	1h	Enable SRAM correctable error interrupt as fatal. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.44 USB3P0SS_CTRL_ASF_RSVD_6_ASF Register

1 USB3P0SS_CTRL_ASF_RSVD_6_ASF Register (Offset = 14h) [reset = 0h]

Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits.

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Table 14-20986. Instance Table

Instance Name	Physical Address
USB0	**0F40 0014h**

Figure 14-6934. USB3P0SS_CTRL_ASF_RSVD_6_ASF Name Register

31	30	29	28	27	26	25	24
RSVD_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD_1							
R							
0h							

Table 14-20988. USB3P0SS_CTRL_ASF_RSVD_6_ASF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD_1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.45 USB3P0SS_CTRL_ASF_RSVD_7_ASF Register

1 USB3P0SS_CTRL_ASF_RSVD_7_ASF Register (Offset = 18h) [reset = 0h]

Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits.

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Table 14-20989. Instance Table

Instance Name	Physical Address
USB0	0F40 0018h

Figure 14-6935. USB3P0SS_CTRL_ASF_RSVD_7_ASF Name Register

31	30	29	28	27	26	25	24
RSVD_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD_1							
R							
0h							

Table 14-20991. USB3P0SS_CTRL_ASF_RSVD_7_ASF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD_1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.46 USB3P0SS_CTRL_ASF_RSVD_8_ASF Register

1 USB3P0SS_CTRL_ASF_RSVD_8_ASF Register (Offset = 1Ch) [reset = 0h]

Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits.

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Table 14-20992. Instance Table

Instance Name	Physical Address
USB0	0F40 001Ch

Figure 14-6936. USB3P0SS_CTRL_ASF_RSVD_8_ASF Name Register

31	30	29	28	27	26	25	24
RSVD_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD_1							
R							
0h							

Table 14-20994. USB3P0SS_CTRL_ASF_RSVD_8_ASF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD_1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.47 USB3P0SS_CTRL_ASF_ASF_SRAM_CORR_FAULT_STATUS Register

1 USB3P0SS_CTRL_ASF_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 20h) [reset = 0h]

Status register for SRAM correctable fault. These fields are updated whenever asf_sram_corr_fault input is active. ASF parity-protected: no

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Table 14-20995. Instance Table

Instance Name	Physical Address
USB0	**0F40 0020h**

Figure 14-6937. USB3P0SS_CTRL_ASF_ASF_SRAM_CORR_FAULT_STATUS Name Register

31	30	29	28	27	26	25	24
ASF_SRAM_CORR_FAULT_INST							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ASF_SRAM_CORR_FAULT_ADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ASF_SRAM_CORR_FAULT_ADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ASF_SRAM_CORR_FAULT_ADDR							
R							
0h							

Table 14-20997. USB3P0SS_CTRL_ASF_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ASF_SRAM_CORR_FAULT_INST	R	0h	Last SRAM instance that generated fault. Reset Source: rst_mod_g_rst_n
23:0	ASF_SRAM_CORR_FAULT_ADDR	R	0h	Last SRAM address that generated fault. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.48 USB3P0SS_CTRL_ASF_ASF_SRAM_UNCORR_FAULT_STATUS Register

1 USB3P0SS_CTRL_ASF_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 24h) [reset = 0h]

Status register for SRAM uncorrectable fault. These fields are updated whenever asf_sram_uncorr_fault input is active. ASF parity-protected: no

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Table 14-20998. Instance Table

Instance Name	Physical Address
USB0	**0F40 0024h**

Figure 14-6938. USB3P0SS_CTRL_ASF_ASF_SRAM_UNCORR_FAULT_STATUS Name Register

31	30	29	28	27	26	25	24
ASF_SRAM_UNCORR_FAULT_INST							
R							
0h							
23	22	21	20	19	18	17	16
ASF_SRAM_UNCORR_FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ASF_SRAM_UNCORR_FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ASF_SRAM_UNCORR_FAULT_ADDR							
R							
0h							

Table 14-21000. USB3P0SS_CTRL_ASF_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ASF_SRAM_UNCORR_FAULT_INST	R	0h	Last SRAM instance that generated fault. Reset Source: rst_mod_g_rst_n
23:0	ASF_SRAM_UNCORR_FAULT_ADDR	R	0h	Last SRAM address that generated fault. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.49 USB3P0SS_CTRL_ASF_ASF_SRAM_FAULT_STATS Register

1 USB3P0SS_CTRL_ASF_ASF_SRAM_FAULT_STATS Register (Offset = 28h) [reset = 0h]

Statistics register for SRAM faults. Note that this register clears when software writes to any field. ASF parity-protected: no

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Table 14-21001. Instance Table

Instance Name	Physical Address
USB0	**0F40 0028h**

Figure 14-6939. USB3P0SS_CTRL_ASF_ASF_SRAM_FAULT_STATS Name Register

31	30	29	28	27	26	25	24
ASF_SRAM_FAULT_UNCORR_STATS							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
ASF_SRAM_FAULT_UNCORR_STATS							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
ASF_SRAM_FAULT_CORR_STATS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
ASF_SRAM_FAULT_CORR_STATS							
R/W1TC							
0h							

Table 14-21003. USB3P0SS_CTRL_ASF_ASF_SRAM_FAULT_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ASF_SRAM_FAULT_UNCORR_STATS	R/W1TC	0h	Count of number of uncorrectable errors if implemented. Count value will saturate at 0xffff. Reset Source: rst_mod_g_rst_n
15:0	ASF_SRAM_FAULT_CORR_STATS	R/W1TC	0h	Count of number of correctable errors if implemented. Count value will saturate at 0xffff. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.50 USB3P0SS_CTRL_ASF_RSVD_12_ASF Register

1 USB3P0SS_CTRL_ASF_RSVD_12_ASF Register (Offset = 2Ch) [reset = 0h]

Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits.

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Table 14-21004. Instance Table

Instance Name	Physical Address
USB0	0F40 002Ch

Figure 14-6940. USB3P0SS_CTRL_ASF_RSVD_12_ASF Name Register

31	30	29	28	27	26	25	24
RSVD_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD_1							
R							
0h							

Table 14-21006. USB3P0SS_CTRL_ASF_RSVD_12_ASF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD_1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.51 USB3P0SS_CTRL_ASF_ASF_TRANS_TO_CTRL Register

1 USB3P0SS_CTRL_ASF_ASF_TRANS_TO_CTRL Register (Offset = 30h) [reset = 0h]

Control register to configure the ASF transaction timeout monitors. ASF parity-protected: yes (only bytes 0, 1 and 3 protected. Byte 2 is not protected)

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Table 14-21007. Instance Table

Instance Name	Physical Address
USB0	**0F40 0030h**

Figure 14-6941. USB3P0SS_CTRL_ASF_ASF_TRANS_TO_CTRL Name Register

31	30	29	28	27	26	25	24
ASF_TRANS_TO_EN	RSVD1						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ASF_TRANS_TO_CTRL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ASF_TRANS_TO_CTRL							
R/W							
0h							

Table 14-21009. USB3P0SS_CTRL_ASF_ASF_TRANS_TO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ASF_TRANS_TO_EN	R/W	0h	Enable transaction timeout monitoring. Reset Source: rst_mod_g_rst_n
30:16	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ASF_TRANS_TO_CTRL	R/W	0h	Timer value to use for transaction timeout monitor. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.52 USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_MASK Register

1 USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_MASK Register (Offset = 34h) [reset = FFFFFFFFh]

Control register to mask out ASF transaction timeout faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parametrisable and the bit definitions are implementation specific. ASF parity-protected: yes

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Table 14-21010. Instance Table

Instance Name	Physical Address
USB0	**0F40 0034h**

Figure 14-6942. USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_MASK Name Register

31	30	29	28	27	26	25	24
ASF_TRANS_TO_FAULT_MASK							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
ASF_TRANS_TO_FAULT_MASK							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
ASF_TRANS_TO_FAULT_MASK							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
ASF_TRANS_TO_FAULT_MASK							
R/W							
FFFFFFFFh							

Table 14-21012. USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ASF_TRANS_TO_FAULT_MASK	R/W	FFFFFFFFh	Mask register for each ASF transaction timeout fault source. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.53 USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_STATUS Register

1 USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 38h) [reset = 0h]

Status register for transaction timeouts fault. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit. ASF parity-protected: no

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Table 14-21013. Instance Table

Instance Name	Physical Address
USB0	**0F40 0038h**

Figure 14-6943. USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_STATUS Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD1		ASF_TRANS_TIMEOUT_BAXI	ASF_TRANS_TIMEOUT_RAXI	ASF_TRANS_TIMEOUT_ARAXI	ASF_TRANS_TIMEOUT_WAXI	ASF_TRANS_TIMEOUT_AWAXI	ASF_TRANS_TIMEOUT_APB
R		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h

Table 14-21015. USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
5	ASF_TRANS_TIMEOUT_BAXI	R/W1TC	0h	Status bits for transaction timeouts faults - AXI Timeout [BAXI] Reset Source: rst_mod_g_rst_n
4	ASF_TRANS_TIMEOUT_RAXI	R/W1TC	0h	Status bits for transaction timeouts faults - AXI Timeout [RAXI] Reset Source: rst_mod_g_rst_n
3	ASF_TRANS_TIMEOUT_ARAXI	R/W1TC	0h	Status bits for transaction timeouts faults - AXI Timeout [ARAXI] Reset Source: rst_mod_g_rst_n
2	ASF_TRANS_TIMEOUT_WAXI	R/W1TC	0h	Status bits for transaction timeouts faults - AXI Timeout [WAXI] Reset Source: rst_mod_g_rst_n
1	ASF_TRANS_TIMEOUT_AWAXI	R/W1TC	0h	Status bits for transaction timeouts faults - AXI Timeout [AWAXI] Reset Source: rst_mod_g_rst_n

Table 14-21015. USB3P0SS_CTRL_ASF_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASF_TRANS_TIMEOUT_APB	R/W1TC	0h	Status bit for transaction timeout faults - APB timeout. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.54 USB3P0SS_CTRL_ASF_RSVD_16_ASF Register

1 USB3P0SS_CTRL_ASF_RSVD_16_ASF Register (Offset = 3Ch) [reset = 0h]

Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits.

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Table 14-21016. Instance Table

Instance Name	Physical Address
USB0	0F40 003Ch

Figure 14-6944. USB3P0SS_CTRL_ASF_RSVD_16_ASF Name Register

31	30	29	28	27	26	25	24
RSVD_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD_1							
R							
0h							

Table 14-21018. USB3P0SS_CTRL_ASF_RSVD_16_ASF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD_1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.55 USB3P0SS_CTRL_ASF_RSVD_17_ASF Register

1 USB3P0SS_CTRL_ASF_RSVD_17_ASF Register (Offset = 40h) [reset = 0h]

Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits.

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Table 14-21019. Instance Table

Instance Name	Physical Address
USB0	**0F40 0040h**

Figure 14-6945. USB3P0SS_CTRL_ASF_RSVD_17_ASF Name Register

31	30	29	28	27	26	25	24
RSVD_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD_1							
R							
0h							

Table 14-21021. USB3P0SS_CTRL_ASF_RSVD_17_ASF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD_1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.56 USB3P0SS_CTRL_ASF_RSVD_18_ASF Register

1 USB3P0SS_CTRL_ASF_RSVD_18_ASF Register (Offset = 44h) [reset = 0h]

Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits.

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Table 14-21022. Instance Table

Instance Name	Physical Address
USB0	0F40 0044h

Figure 14-6946. USB3P0SS_CTRL_ASF_RSVD_18_ASF Name Register

31	30	29	28	27	26	25	24
RSVD_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD_1							
R							
0h							

Table 14-21024. USB3P0SS_CTRL_ASF_RSVD_18_ASF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD_1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.57 USB3P0SS_CTRL_XHCI_HCIVERSION_CAPLENGTH Register

1 USB3P0SS_CTRL_XHCI_HCIVERSION_CAPLENGTH Register (Offset = 0h) [reset = 1000080h]

HCIVERSION_CAPLENGTH

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Table 14-21025. Instance Table

Instance Name	Physical Address
USB0	**0F40 0000h**

Figure 14-6947. USB3P0SS_CTRL_XHCI_HCIVERSION_CAPLENGTH Name Register

31	30	29	28	27	26	25	24
HCIVERSION							
R							
100h							
23	22	21	20	19	18	17	16
HCIVERSION							
R							
100h							
15	14	13	12	11	10	9	8
RSVD1							
R							
0h							
7	6	5	4	3	2	1	0
CAPLENGTH							
R							
80h							

Table 14-21027. USB3P0SS_CTRL_XHCI_HCIVERSION_CAPLENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HCIVERSION	R	100h	Host Controller Interface Version Number [HCIVERSION]. This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0. Reset Source: rst_mod_g_rst_n
15:8	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
7:0	CAPLENGTH	R	80h	Capability Registers Length [CAPLENGTH]. This register is used as an offset to add to register base to find the beginning of the Operational Register Space. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.58 USB3P0SS_CTRL_XHCI_HCSPARAMS1 Register

1 USB3P0SS_CTRL_XHCI_HCSPARAMS1 Register (Offset = 4h) [reset = 2000840h]

Structural Parameters 1 (HCSPARAMS1). This register defines basic structural parameters supported by this xHC implementation: Number of Device Slots support, Interrupters, Root Hub ports.

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Table 14-21028. Instance Table

Instance Name	Physical Address
USB0	**0F40 0004h**

Figure 14-6948. USB3P0SS_CTRL_XHCI_HCSPARAMS1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MAXPORTS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RSVD1</td><td colspan="3">MAXINTRS</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">8h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MAXINTRS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MAXSLOTS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">40h</td></tr>
</table>

Table 14-21030. USB3P0SS_CTRL_XHCI_HCSPARAMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAXPORTS	R	2h	Number of Ports [MaxPorts]. This field specifies the maximum Port Number value, i.e. the highest numbered Port Register Set that are addressable in the Operational Register Space. Valid values are in the range of 1h to FFh. The value in this field shall reflect the maximum Port Number value assigned by an xHCI Supported Protocol Capability, described in section 7.2 of xHCI specification. Software shall refer to these capabilities to identify whether a specific Port Number is valid, and the protocol supported by the associated Port Register Set. Reset Source: rst_mod_g_rst_n
23:19	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21030. USB3P0SS_CTRL_XHCI_HCSPARAMS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:8	MAXINTRS	R	8h	Number of Interrupters [MaxIntrs]. This field specifies the number of Interrupters implemented on this host controller. Each Interrupter may be allocated to a MSI or MSI-X vector and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space [refer to section 5.5 of xHCI specification]. Valid values are in the range of 1h to 400h. A '0' in this field is undefined. Reset Source: rst_mod_g_rst_n
7:0	MAXSLOTS	R	40h	Number of Device Slots [MaxSlots]. This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of 0 is reserved. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.59 USB3P0SS_CTRL_XHCI_HCSPARAMS2 Register

1 USB3P0SS_CTRL_XHCI_HCSPARAMS2 Register (Offset = 8h) [reset = 4200054h]

Structural Parameters 2 (HCSPARAMS 2). This register defines additional xHC structural parameters.

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Table 14-21031. Instance Table

Instance Name	Physical Address
USB0	0F40 0008h

Figure 14-6949. USB3P0SS_CTRL_XHCI_HCSPARAMS2 Name Register

31	30	29	28	27	26	25	24
MAXSPBUFLO					SPR	MAXSPBUFHI	
R					R	R	
0h					1h	1h	
23	22	21	20	19	18	17	16
MAXSPBUFHI			RSVD1				
R			R				
1h			0h				
15	14	13	12	11	10	9	8
RSVD1							
R							
0h							
7	6	5	4	3	2	1	0
ERSTMAX				IST			
R				R			
5h				4h			

Table 14-21033. USB3P0SS_CTRL_XHCI_HCSPARAMS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	MAXSPBUFLO	R	0h	Max Scratchpad Buffers [Max Scratchpad Bufs Lo]. Default = implementation dependent. Valid values for Max Scratchpad Buffers [Hi and Lo] are 0-1023. This field indicates the low order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC. Refer to section 4.20 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
26	SPR	R	1h	Scratchpad Restore [SPR]. Default = implementation dependent. If Max Scratchpad Buffers is > 0 then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If Max Scratchpad Buffers is = 0 then this flag shall be 0. Refer to section 4.23.2 of xHCI specification for more information. A value of '1' indicates that the xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events. A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events. Reset Source: rst_mod_g_rst_n
25:21	MAXSPBUFHI	R	1h	Max Scratchpad Buffers [Max Scratchpad Bufs Hi]. Default = implementation dependent. This field indicates the high order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC. Refer to section 4.20 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n

Table 14-21033. USB3P0SS_CTRL_XHCI_HCSPARAMS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:8	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
7:4	ERSTMAX	R	5h	Event Ring Segment Table Max [ERST Max]. Default = implementation dependent. Valid values are 0-15. This field determines the maximum value supported the Event Ring Segment Table Base Size registers [5.5.2.3.1], where: The maximum number of Event Ring Segment Table entries = 2 ^[ERSTMax], e.g. if the ERST Max = 7, then the xHC Event Ring Segment Table[s] supports up to 128 entries, 15 then 32K entries, etc. Reset Source: rst_mod_g_rst_n
3:0	IST	R	4h	Isochronous Scheduling Threshold [IST]. Default = implementation dependent. The value in this field indicates to system software the minimum distance [in time] that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/microframes. If bit [3] of IST is cleared to '0', software can add a TRB no later than IST[2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to '1', software can add a TRB no later than IST[2:0] Frames before that TRB is scheduled to be executed. Refer to Section 4.14.2 of xHCI specification for details on how software uses this information for scheduling isochronous transfers. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.60 USB3P0SS_CTRL_XHCI_HCSPARAMS3 Register

1 USB3P0SS_CTRL_XHCI_HCSPARAMS3 Register (Offset = Ch) [reset = 40001h]

Structural Parameters 3 (HCSPARAMS3). This register defines link exit latency related structural parameters.

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Table 14-21034. Instance Table

Instance Name	Physical Address
USB0	**0F40 000Ch**

Figure 14-6950. USB3P0SS_CTRL_XHCI_HCSPARAMS3 Name Register

31	30	29	28	27	26	25	24
U2DEVEXITLAT							
R							
4h							
23	22	21	20	19	18	17	16
U2DEVEXITLAT							
R							
4h							
15	14	13	12	11	10	9	8
RSVD1							
R							
0h							
7	6	5	4	3	2	1	0
U1DEVEXITLAT							
R							
1h							

Table 14-21036. USB3P0SS_CTRL_XHCI_HCSPARAMS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	U2DEVEXITLAT	R	4h	U2 Device Exit Latency. Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: 0000h Zero, 0001h Less than 1 s., 0002h Less than 2 s., ... 07FFh Less than 2047 s., 0800-FFFFh Reserved Reset Source: rst_mod_g_rst_n
15:8	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21036. USB3P0SS_CTRL_XHCI_HCSPARAMS3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	U1DEVEXITLAT	R	1h	U1 Device Exit Latency. Worst case latency to transition a root hub Port Link State [PLS] from U1 to U0. Applies to all root hub ports. The following are permissible values: 00h Zero, 01h Less than 1 s., 02h Less than 2 s., ... 0Ah Less than 10 s., 0B-FFh Reserved. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.61 USB3P0SS_CTRL_XHCI_HCCPARAMS Register

1 USB3P0SS_CTRL_XHCI_HCCPARAMS Register (Offset = 10h) [reset = 200073C9h]

Capability Parameters (HCCPARAMS). This register defines optional capabilities supported by the xHCI. The default values for all fields in this register are implementation dependent.

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Table 14-21037. Instance Table

Instance Name	Physical Address
USB0	**0F40 0010h**

Figure 14-6951. USB3P0SS_CTRL_XHCI_HCCPARAMS Name Register

31	30	29	28	27	26	25	24
XECP							
R							
2000h							
23	22	21	20	19	18	17	16
XECP							
R							
2000h							
15	14	13	12	11	10	9	8
MAXPSASIZE				RSVD1		SPC	PAE
R				R		R	R
7h				0h		1h	1h
7	6	5	4	3	2	1	0
NSS	LTC	LHRC	PIND	PPC	CSZ	BNC	AC64
R	R	R	R	R	R	R	R
1h	1h	0h	0h	1h	0h	0h	1h

Table 14-21039. USB3P0SS_CTRL_XHCI_HCCPARAMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XECP	R	2000h	xHCI Extended Capabilities Pointer [xECP]. This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability. For example, using the offset of Base is 1000h and the xECP value of 0068h, we can calculate the following effective address of the first extended capability: 1000h + [0068h shifted left 2] -> 1000h + 01A0h -> 11A0h Reset Source: rst_mod_g_rst_n
15:12	MAXPSASIZE	R	7h	Maximum Primary Stream Array Size [MaxPSASize]. This fields identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = 2^[MaxPSASize+1]. Valid MaxPSASize values are 0 to 15, where 0 indicates that Streams are not supported. Reset Source: rst_mod_g_rst_n
11:10	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21039. USB3P0SS_CTRL_XHCI_HCCPARAMS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SPC	R	1h	Stopped - Short Packet Capability [SPC]. This flag indicates that the host controller implementation is capable of generating a Stopped - Short Packet Completion Code. Refer to section 4.6.9 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
8	PAE	R	1h	Parse All Event Data [PAE]. This flag indicates whether the host controller implementation Parses all Event Data TRBs while advancing to the next TD after a Short Packet, or it skips all but the first Event Data TRB. A '1' in this bit indicates that all Event Data TRBs are parsed. A '0' in this bit indicates that only the first Event Data TRB is parsed [refer to section 4.10.1.1 of xHCI specification]. Reset Source: rst_mod_g_rst_n
7	NSS	R	1h	No Secondary SID Support [NSS]. This flag indicates whether the host controller implementation supports Secondary Stream IDs. A '1'in this bit indicates that Secondary Stream ID decoding is not supported. A '0' in this bit indicates that Secondary Stream ID decoding is supported. [refer to Sections 4.12.2 and 6.2.3 of xHCI specification]. Reset Source: rst_mod_g_rst_n
6	LTC	R	1h	Latency Tolerance Messaging Capability [LTC]. This flag indicates whether the host controller implementation supports Latency Tolerance Messaging [LTM]. A '1' in this bit indicates that LTM is supported. A 0 in this bit indicates that LTM is not supported. Refer to section 4.13.1 of xHCI specification for more information on LTM. Reset Source: rst_mod_g_rst_n
5	LHRC	R	0h	Light HC Reset Capability [LHRC]. This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A '1' in this bit indicates that Light Host Controller Reset is supported. A '0' in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the Light Host Controller Reset [LHCRST] flag in the USBCMD register [refer to Section 5.4.1 of xHCI specification]. Reset Source: rst_mod_g_rst_n
4	PIND	R	0h	Port Indicators [PIND]. This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator. Refer to Section 5.4.8 of xHCI specification for definition of the Port Indicator Control field [PIC field of PORTSC register]. Reset Source: rst_mod_g_rst_n
3	PPC	R	1h	Port Power Control [PPC]. This flag indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register [refer to Section 5.4.8 of xHCI specification]. When DEBUG_CTRL_REG capability is used [CDNS_RM_CBIT_DEBUG_CTRL_REG is not defined] then this bit is treated as RW. Its value can be changed only by writes to bit 8 of DEBUG_CTRL_REG [port_pwr_ctrl_toggle]. Direct writes to this bit are not possible. Reset Source: rst_mod_g_rst_n
2	CSZ	R	0h	Context Size [CSZ]. If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is cleared to 0, then the xHC uses 32 byte Context data structures. Note: This flag does not apply to Stream Contexts. Reset Source: rst_mod_g_rst_n

Table 14-21039. USB3P0SS_CTRL_XHCI_HCCPARAMS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BNC	R	0h	BW Negotiation Capability [BNC]. This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: '0': BW Negotiation not implemented '1': BW Negotiation implemented Refer to section 4.16 of xHCI specification for more information on Bandwidth Negotiation. Reset Source: rst_mod_g_rst_n
0	AC64	R	1h	64-bit Addressing Capability [AC64]. This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this flag have the following interpretation: '0': 32-bit address memory pointers implemented, '1': 64-bit address memory pointers implemented. If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.62 USB3P0SS_CTRL_XHCI_DBOFF Register

1 USB3P0SS_CTRL_XHCI_DBOFF Register (Offset = 14h) [reset = 3000h]

This register defines the offset of the Doorbell Array base address from the Base.

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Table 14-21040. Instance Table

Instance Name	Physical Address
USB0	**0F40 0014h**

Figure 14-6952. USB3P0SS_CTRL_XHCI_DBOFF Name Register

31	30	29	28	27	26	25	24
DAO							
R							
C00h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DAO							
R							
C00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DAO							
R							
C00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DAO						RSVD1	
R						R	
C00h						0h	

Table 14-21042. USB3P0SS_CTRL_XHCI_DBOFF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	DAO	R	C00h	Doorbell Array Offset, RO. Default = implementation dependent. This field defines the offset in Dwords of the Doorbell Array base address from the Base [i.e. the base address of the xHCI Capability register address space]. Reset Source: rst_mod_g_rst_n
1:0	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.63 USB3P0SS_CTRL_XHCI_RTSOFF Register

1 USB3P0SS_CTRL_XHCI_RTSOFF Register (Offset = 18h) [reset = 2000h]

This register defines the offset of the xHCI Runtime Registers from the Base.

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Table 14-21043. Instance Table

Instance Name	Physical Address
USB0	**0F40 0018h**

Figure 14-6953. USB3P0SS_CTRL_XHCI_RTSOFF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RRSO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RRSO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RRSO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RRSO</td><td colspan="5">RSVD1</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">100h</td><td colspan="5">0h</td></tr>
</table>

Table 14-21045. USB3P0SS_CTRL_XHCI_RTSOFF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RRSO	R	100h	Runtime Register Space Offset, RO. Default = implementation dependent. This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. i.e. Runtime Register Base Address = Base + Runtime Register Set Offset. Reset Source: rst_mod_g_rst_n
4:0	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.64 USB3P0SS_CTRL_XHCI_HCCPARAMS2 Register

1 USB3P0SS_CTRL_XHCI_HCCPARAMS2 Register (Offset = 1Ch) [reset = 8h]

Capability Parameters 2 (HCCPARAMS2). This register defines optional capabilities supported by the xHCI. The default values for all fields in this register are implementation dependent.

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Table 14-21046. Instance Table

Instance Name	Physical Address
USB0	0F40 001Ch

Figure 14-6954. USB3P0SS_CTRL_XHCI_HCCPARAMS2 Name Register

31	30	29	28	27	26	25	24
RSVD2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD2				CTC	RSVD1		
R				R	R		
0h				1h	0h		

Table 14-21048. USB3P0SS_CTRL_XHCI_HCCPARAMS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
3	CTC	R	1h	This bit indicates whether the xHC USB3 Root Hub ports support the Compliance Transition Enabled [CTE] flag. When this bit is 1 USB3 Root Hub port state machine transitions to the Compliance substate shall be explicitly enabled software. When this bit is 0. USB3 Root Hub port state machine transitions to the Compliance substate are automatically enabled. Reset Source: rst_mod_g_rst_n
2:0	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.65 USB3P0SS_CTRL_XHCI_RSVD_CR_j Register

1 USB3P0SS_CTRL_XHCI_RSVD_CR_j Register (Offset = 20h + formula) [reset = 0h]

Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits.

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Offset = (j * 4h); where j = 0 to 23d

Table 14-21049. Instance Table

Instance Name	Physical Address
USB0	**0F40 0020h + formula**

Figure 14-6955. USB3P0SS_CTRL_XHCI_RSVD_CR_j Name Register

31	30	29	28	27	26	25	24
RSVD_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD_1							
R							
0h							

Table 14-21051. USB3P0SS_CTRL_XHCI_RSVD_CR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD_1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.66 USB3P0SS_CTRL_XHCI_USBCMD Register

1 USB3P0SS_CTRL_XHCI_USBCMD Register (Offset = 80h) [reset = 0h]

USB Command Register (USBCMD). The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

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Table 14-21052. Instance Table

Instance Name	Physical Address
USB0	**0F40 0080h**

Figure 14-6956. USB3P0SS_CTRL_XHCI_USBCMD Name Register

31	30	29	28	27	26	25	24
RSVDP2							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP2							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP2				EU3S	EWE	CRS	CSS
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
LHCRST	RSVDP1			HSEE	INTE	HCRST	R_S
R	R			R/W	R/W	R/W	R/W
0h	0h			0h	0h	0h	0h

Table 14-21054. USB3P0SS_CTRL_XHCI_USBCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RSVDP2	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
11	EU3S	R/W	0h	Enable U3 MFINDEX Stop [EU3S], RW. Default = '0'. When set to '1', the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to '0' the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, Training, or Powered-off state. Refer to section 4.14.2 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
10	EWE	R/W	0h	Enable Wrap Event [EWE], RW. Default = '0'. When set to '1', the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to '0' no MFINDEX Wrap Events are generated. Refer to section 4.14.2 of xHCI specification for more information. When this register is exposed by a Virtual Function [VF], the generation of MFINDEX Wrap Events to VFs shall be emulated by the VMM. Reset Source: rst_mod_g_rst_n

Table 14-21054. USB3P0SS_CTRL_XHCI_USBCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CRS	R/W	0h	Controller Restore State [CRS], RW. Default = '0'. When set to '1', and HCHalted [HCH] = '1', then the xHC shall perform a Restore State operation and restore its internal state. When set to '1' and Run/Stop [R/S] = '1' or HCHalted [HCH] = '0', or when cleared to '0', no Restore State operation shall be performed. This flag always returns '0' when read. Refer to the Restore State Status [RSS] flag in the USBSTS register for information on Restore State completion. Refer to section 4.23.2 of xHCI specification for more information. Note that undefined behavior may occur if a Restore State operation is initiated while Save State Status [SSS] = '1'. When this register is exposed by a Virtual Function [VF], this bit only controls restoring the state of the xHC instance presented by the selected VF. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
8	CSS	R/W	0h	Controller Save State [CSS], RW. Default = '0'. When written by software with '1' and HCHalted [HCH] = '1', then the xHC shall save any internal state that may be restored by a subsequent Restore State operation. When written by software with '1' and HCHalted [HCH] = '0', or written with '0', no Save State operation shall be performed. This flag always returns '0' when read. Refer to the Save State Status [SSS] flag in the USBSTS register for information on Save State completion. Refer to section 4.23.2 of xHCI specification for more information on xHC Save/Restore operation. Note that undefined behavior may occur if a Save State operation is initiated while Restore State Status [RSS] ='1'. When this register is exposed by a Virtual Function [VF], this bit only controls saving the state of the xHC instance presented by the selected VF. Refer to section 8 of xHCI specifications for more information. Reset Source: rst_mod_g_rst_n
7	LHCRST	R	0h	Light Host Controller Reset [LHCRST], RO or RW. Optional normative. Default = '0'. If the Light HC Reset Capability [LHRC] bit in the HCCPARAMS register is '1', then this flag allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as '0' indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a '1' indicates that the Light Host Controller Reset has not yet completed. If not implemented, a read of this flag shall always return a '0'. All registers in the Aux Power well shall maintain the values that had been asserted prior to the Light Host Controller Reset. Refer to section 4.23.1 of xHCI specification for more information. When this register is exposed by a Virtual Function [VF], this bit only generates a Light Reset to the xHC instance presented by the selected VF, e.g. Disable the VFs device slots and set the associated VF Run bit to Stopped. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
6:4	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21054. USB3P0SS_CTRL_XHCI_USBCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	HSEE	R/W	0h	Host System Error Enable [HSEE], RW. Default = '0'. When this bit is a '1', and the HSE bit in the USBSTS register is a '1', the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit. Refer to section 4.10.2.6 of xHCI specification for more information. When this register is exposed by a Virtual Function [VF], the effect of the assertion of this bit on the Physical Function [PF0] is determined by the VMM. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
2	INTE	R/W	0h	Interrupter Enable [INTE], RW. Default = '0'. This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a '1', then Interrupter host system interrupt generation is allowed, e.g. the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism [e.g. MSI, MSIX, etc.] is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism. When this register is exposed by a Virtual Function [VF], this bit only enables the set of Interrupters assigned to the selected VF. Refer to section 7.7.2 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
1	HCRST	R/W	0h	Host Controller Reset [HCRST], RW. Default = '0'. This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset. When software writes a '1' to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on the USB is immediately terminated. A USB reset shall not be driven on USB2 downstream ports, however a Hot or Warm Reset shall be initiated on USB3 Root Hub downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Software shall reinitialize the host controller as described in Section 4.1 of xHCI specification in order to return the host controller to an operational state. This bit is cleared to '0' by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a '0' to this bit and shall not write any xHC Operational or Runtime registers until while HCRST is '1'. Note, the completion of the xHC reset process is not gated by the Root Hub port reset process. Software shall not set this bit to '1' when the HCHalted [HCH] bit in the USBSTS register is a '0'. Attempting to reset an actively running host controller may result in undefined behavior. When this register is exposed by a Virtual Function [VF], this bit only resets the xHC instance presented by the selected VF. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n

Table 14-21054. USB3P0SS_CTRL_XHCI_USBCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R_S	R/W	0h	Run/Stop [R/S], RW. Default = '0'. '1' = Run. '0' = Stop. When set to a '1', the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a '1'. When this bit is cleared to '0', the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. Refer to section 5.4.1.1 of xHCI specification for more information on how R/S shall be managed. The xHC shall halt within 16 ms after software clears the Run/Stop bit if the above conditions have been met. The HCHalted [HCH] bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state [i.e. HCH in the USBSTS register is '1']. Doing so may yield undefined results. Writing a '0' to this flag when the xHC is in the Running state [i.e. HCH = '0'] and any Event Rings are in the Event Ring Full state [refer to section 4.9.4 of xHCI specification] may result in lost events. When this register is exposed by a Virtual Function [VF], this bit only controls the run state of the xHC instance presented by the selected VF. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.67 USB3P0SS_CTRL_XHCI_USBSTS Register

1 USB3P0SS_CTRL_XHCI_USBSTS Register (Offset = 84h) [reset = 801h]

USB Status Register (USBSTS). This register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to '0' in this register by writing a '1' to it (RW1C). Refer to Section 4.17 of xHCI specification for additional information concerning USB interrupt conditions.

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Table 14-21055. Instance Table

Instance Name	Physical Address
USB0	**0F40 0084h**

Figure 14-6957. USB3P0SS_CTRL_XHCI_USBSTS Name Register

31	30	29	28	27	26	25	24
RSVDP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP			HCE	CNR	SRE	RSS	SSS
R			R	R	R/W1TC	R	R
0h			0h	1h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVDZ2			PCD	EINT	HSE	RSVDZ1	HCH
R			R/W1TC	R/W1TC	R/W1TC	R	R
0h			0h	0h	0h	0h	1h

Table 14-21057. USB3P0SS_CTRL_XHCI_USBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RSVDP	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
12	HCE	R	0h	Host Controller Error [HCE], RO. Default = '0'. '0' = No internal xHC error conditions exist and '1' = Internal xHC error condition. This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC. Refer to section 4.24.1 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
11	CNR	R	1h	Controller Not Ready [CNR], RO. Default = '1'. '0' = Ready and '1' = Not Ready. When this bit is '1', software shall not read or write any register of the xHC, other than those explicitly listed in the Design Specification section titled Register Accessibility. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register reads or writes to all registers. This flag shall remain cleared ['0'] until the next Chip Hardware Reset. Reset Source: rst_mod_g_rst_n

Table 14-21057. USB3P0SS_CTRL_XHCI_USBSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SRE	R/W1TC	0h	Save/Restore Error [SRE], RW1C. Default = '0'. If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'. Refer to section 4.23.2 of xHCI specification for more information. When this register is exposed by a Virtual Function [VF], the VMM determines the state of this bit as a function of the Save/Restore completion status for the selected VF. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
9	RSS	R	0h	Restore State Status [RSS], RO. Default = '0'. When the Controller Restore State [CRS] flag in the USBCMD register is written with '1' this bit shall be set to '1' and remain '1' while the xHC restores its internal state. When the Restore State operation is complete, this bit shall be cleared to '0'. Refer to section 4.23.2 of xHCI specification for more information. When this register is exposed by a Virtual Function [VF], the VMM determines the state of this bit as a function of the restoring the state for the selected VF. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
8	SSS	R	0h	Save State Status [SSS], RO. Default = '0'. When the Controller Save State [CSS] flag in the USBCMD register is written with '1' this bit shall be set to '1' and remain '1' while the xHC saves its internal state. When the Save State operation is complete, this bit shall be cleared to '0'. Refer to section 4.23.2 of xHCI specification for more information. When this register is exposed by a Virtual Function [VF], the VMM determines the state of this bit as a function of the saving the state for the selected VF. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
7:5	RSVDZ2	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4	PCD	R/W1TC	0h	Port Change Detect [PCD], RW1C. Default = '0'. The xHC sets this bit to a '1' when any port has a change bit transition from a '0' to a '1'. This bit is allowed to be maintained in the Aux Power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits. Refer to section 4.19.3 of xHCI specification. This bit provides system software an efficient means of determining if there has been Root Hub port activity. Refer to section 4.15.2.3 of xHCI specification for more information. When this register is exposed by a Virtual Function [VF], the VMM determines the state of this bit as a function of the Root Hub Ports associated with the Device Slots assigned to the selected VF. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n

Table 14-21057. USB3P0SS_CTRL_XHCI_USBSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EINT	R/W1TC	0h	Event Interrupt [EINT], RW1C. Default = '0'. The xHC sets this bit to '1' when the Interrupt Pending [IP] bit of any Interrupter transitions from '0' to '1'. Refer to section 7.1.2 of xHCI specification for use. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition may occur if software clears the IP flags then clears the EINT flag, and between the operations another IP '0' to '1' transition occurs. In this case the new IP transition shall be lost. When this register is exposed by a Virtual Function [VF], this bit is the logical 'OR' of the IP bits for the Interrupters assigned to the selected VF. And it shall be cleared to '0' when all associated interrupter IP bits are cleared, i.e. all the VFs Interrupter Event Ring[s] are empty. Refer to section 8 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2	HSE	R/W1TC	0h	Host System Error [HSE], RW1C. Default = '0'. The xHC sets this bit to '1' when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. [In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort.] When this error occurs, the xHC clears the Run/Stop [R/S] bit in the USBCMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USBCMD register is a '1', the xHC shall also assert out-of-band error signaling to the host. Refer to section 4.10.2.6 of xHCI specification for more information. When this register is exposed by a Virtual Function [VF], the assertion of this bit affects all VFs and reflects the Host System Error state of the Physical Function [PF0]. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
1	RSVDZ1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
0	HCH	R	1h	HCHalted [HCH], RO. Default = '1'. This bit is a '0' whenever the Run/Stop [R/S] bit is a '1'. The xHC sets this bit to '1' after it has stopped executing as a result of the Run/Stop [R/S] bit being cleared to '0', either by software or by the xHC hardware [e.g. internal error]. If this bit is '1', then SOFs, microSOFs, or Isochronous Timestamp Packets [ITP] shall not be generated by the xHC, and any received Transaction Packet shall be dropped. When this register is exposed by a Virtual Function [VF], this bit only reflects the Halted state of the xHC instance presented by the selected VF. Refer to section 8 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.68 USB3P0SS_CTRL_XHCI_PAGESIZE Register

1 USB3P0SS_CTRL_XHCI_PAGESIZE Register (Offset = 88h) [reset = 1h]

Page Size Register (PAGESIZE).

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Table 14-21058. Instance Table

Instance Name	Physical Address
USB0	**0F40 0088h**

Figure 14-6958. USB3P0SS_CTRL_XHCI_PAGESIZE Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD1							
R							
0h							
15	14	13	12	11	10	9	8
PAGESIZE							
R							
1h							
7	6	5	4	3	2	1	0
PAGESIZE							
R							
1h							

Table 14-21060. USB3P0SS_CTRL_XHCI_PAGESIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	PAGESIZE	R	1h	Page Size, RO. Default = Implementation defined. This field defines the page size supported by the xHC implementation. This xHC supports a page size of 2^[n+12] if bit n is Set. For example, if bit 0 is Set, the xHC supports 4k byte page sizes. For a Virtual Function, this register reflects the page size selected in the System Page Size field of the SR-IOV Extended Capability structure. For the Physical Function 0, this register reflects the implementation dependent default xHC page size. Various xHC resources reference PAGESIZE to describe their minimum alignment requirements. The maximum possible page size is 128M. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.69 USB3P0SS_CTRL_XHCI_RSVDZ8C Register

1 USB3P0SS_CTRL_XHCI_RSVDZ8C Register (Offset = 8Ch) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Table 14-21061. Instance Table

Instance Name	Physical Address
USB0	**0F40 008Ch**

Figure 14-6959. USB3P0SS_CTRL_XHCI_RSVDZ8C Name Register

31	30	29	28	27	26	25	24
RSVDZ_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDZ_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDZ_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDZ_1							
R							
0h							

Table 14-21063. USB3P0SS_CTRL_XHCI_RSVDZ8C Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.70 USB3P0SS_CTRL_XHCI_RSVDZ90 Register

1 USB3P0SS_CTRL_XHCI_RSVDZ90 Register (Offset = 90h) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Table 14-21064. Instance Table

Instance Name	Physical Address
USB0	0F40 0090h

Figure 14-6960. USB3P0SS_CTRL_XHCI_RSVDZ90 Name Register

31	30	29	28	27	26	25	24
RSVDZ_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDZ_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDZ_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDZ_1							
R							
0h							

Table 14-21066. USB3P0SS_CTRL_XHCI_RSVDZ90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.71 USB3P0SS_CTRL_XHCI_DNCTRL Register

1 USB3P0SS_CTRL_XHCI_DNCTRL Register (Offset = 94h) [reset = 0h]

Device Notification Control Register (DNCTRL). This register is used by software to enable or disable the reporting of the reception of specific USB Device Notification Transaction Packets. A Notification Enable (Nx, where x = 0 to 15) flag is defined for each of the 16 possible device notification types. If a flag is set for a specific notification type, a Device Notification Event shall be generated when the respective notification packet is received. After reset all notifications are disabled. Refer to section 6.4.2.7 of xHCI specification. This register shall be written as a Dword. Byte writes produce undefined results. When a Notification Enable bit is set, a Device Notification Event shall be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), etc. Note: Of the currently defined USB3 Device Notification Types, only the FUNCTION_WAKE type should not be handled automatically by the xHC. Only under debug conditions would software write the DNCTRL register with a value other than 0002h. Refer to section 8.5.6 in the USB3 specification for more information on Notification Types. If new Device Notification Types are defined, software may receive them by setting the respective Notification Enable bit.

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Table 14-21067. Instance Table

Instance Name	Physical Address
USB0	0F40 0094h

Figure 14-6961. USB3P0SS_CTRL_XHCI_DNCTRL Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
N15	N14	N13	N12	N11	N10	N9	N8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
N7	N6	N5	N4	N3	N2	N1	N0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21069. USB3P0SS_CTRL_XHCI_DNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15	N15	R/W	0h	Notification Enable flag 15 Reset Source: rst_mod_g_rst_n

Table 14-21069. USB3P0SS_CTRL_XHCI_DNCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	N14	R/W	0h	Notification Enable flag 14 Reset Source: rst_mod_g_rst_n
13	N13	R/W	0h	Notification Enable flag 13 Reset Source: rst_mod_g_rst_n
12	N12	R/W	0h	Notification Enable flag 12 Reset Source: rst_mod_g_rst_n
11	N11	R/W	0h	Notification Enable flag 11 Reset Source: rst_mod_g_rst_n
10	N10	R/W	0h	Notification Enable flag 10 Reset Source: rst_mod_g_rst_n
9	N9	R/W	0h	Notification Enable flag 9 Reset Source: rst_mod_g_rst_n
8	N8	R/W	0h	Notification Enable flag 8 Reset Source: rst_mod_g_rst_n
7	N7	R/W	0h	Notification Enable flag 7 Reset Source: rst_mod_g_rst_n
6	N6	R/W	0h	Notification Enable flag 6 Reset Source: rst_mod_g_rst_n
5	N5	R/W	0h	Notification Enable flag 5 Reset Source: rst_mod_g_rst_n
4	N4	R/W	0h	Notification Enable flag 4 Reset Source: rst_mod_g_rst_n
3	N3	R/W	0h	Notification Enable flag 3. BUS_INTERVAL_ADJUSTMENT_MESSAGE. Reset Source: rst_mod_g_rst_n
2	N2	R/W	0h	Notification Enable flag 2. LATENCY_TOLERANCE_MESSAGE. Reset Source: rst_mod_g_rst_n
1	N1	R/W	0h	Notification Enable flag 1 Reset Source: rst_mod_g_rst_n
0	N0	R/W	0h	Notification Enable flag 0 Reset Source: rst_mod_g_rst_n

14.9.2.3.2.72 USB3P0SS_CTRL_XHCI_CRCR_LO Register

1 USB3P0SS_CTRL_XHCI_CRCR_LO Register (Offset = 98h) [reset = 0h]

Command Ring Control Register Low (CRCR_L). The Command Ring Control Register provides Command Ring control and status capabilities, and identifies the address and Cycle bit state of the Command Ring Dequeue Pointer.

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Table 14-21070. Instance Table

Instance Name	Physical Address
USB0	0F40 0098h

Figure 14-6962. USB3P0SS_CTRL_XHCI_CRCR_LO Name Register

31	30	29	28	27	26	25	24
CRPTR_L							
R/W							
0h							
23	22	21	20	19	18	17	16
CRPTR_L							
R/W							
0h							
15	14	13	12	11	10	9	8
CRPTR_L							
R/W							
0h							
7	6	5	4	3	2	1	0
CRPTR_L		RSVD1		CRR	CA	CS	RCS
R/W		R		R	R/W1TS	R/W1TS	R/W
0h		0h		0h	0h	0h	0h

Table 14-21072. USB3P0SS_CTRL_XHCI_CRCR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	CRPTR_L	R/W	0h	Command Ring Pointer Low, RW. Default = 0. This field defines low order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running [CRR] = '1'. If the CRCR is written while the Command Ring is stopped [CCR = '0'], the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped [CCR = '0'] then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns zero. Reset Source: rst_mod_g_rst_n
5:4	RSVD1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21072. USB3P0SS_CTRL_XHCI_CRCR_LO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CRR	R	0h	Command Ring Running [CRR], RO. Default = '0'. This flag is set to '1' if the Run/Stop [R/S] bit is '1' and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to '0' when the Command Ring is stopped after writing a '1' to the Command Stop [CS] or Command Abort [CA] flags, or if the R/S bit is cleared to '0'. Reset Source: rst_mod_g_rst_n
2	CA	R/W1TS	0h	Command Abort [CA], RW1S. Default = '0'. Writing a '1' to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. Refer to section 4.6.1.2 of xHCI specification for more information on aborting a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running [CRR] = '0'. Reading this bit always returns '0'. Reset Source: rst_mod_g_rst_n
1	CS	R/W1TS	0h	Command Stop [CS], RW1S. Default = '0'. Writing a '1' to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. Refer to section 4.6.1.1 of xHCI specification for more information on stopping a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running [CRR] = '0'. Reading this bit shall always return '0'. Reset Source: rst_mod_g_rst_n
0	RCS	R/W	0h	Ring Cycle State [RCS], RW. This bit identifies the value of the xHC Consumer Cycle State [CCS] flag for the TRB referenced by the Command Ring Pointer. Refer to section 4.9.3 of xHCI specification for more information. Writes to this flag are ignored if Command Ring Running [CRR] is '1'. If the CRCR is written while the Command Ring is stopped [CRR = '0'], then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped [CRR = '0'], then the Command Ring shall begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.73 USB3P0SS_CTRL_XHCI_CRCR_HI Register

1 USB3P0SS_CTRL_XHCI_CRCR_HI Register (Offset = 9Ch) [reset = 0h]

Command Ring Control Register High (CRCR_HI). The Command Ring Control Register provides high order bits of the Command Ring Dequeue Pointer.

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Table 14-21073. Instance Table

Instance Name	Physical Address
USB0	0F40 009Ch

Figure 14-6963. USB3P0SS_CTRL_XHCI_CRCR_HI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CRPTR_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CRPTR_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRPTR_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRPTR_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21075. USB3P0SS_CTRL_XHCI_CRCR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRPTR_H	R/W	0h	Command Ring Pointer High, RW. Default = 0. This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running [CRR] = '1'. If the CRCR is written while the Command Ring is stopped [CCR = '0'], the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped [CCR = '0'] then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns zero. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.74 USB3P0SS_CTRL_XHCI_RSVDZA0 Register

1 USB3P0SS_CTRL_XHCI_RSVDZA0 Register (Offset = A0h) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Table 14-21076. Instance Table

Instance Name	Physical Address
USB0	**0F40 00A0h**

Figure 14-6964. USB3P0SS_CTRL_XHCI_RSVDZA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVDZ_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVDZ_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVDZ_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSVDZ_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21078. USB3P0SS_CTRL_XHCI_RSVDZA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.75 USB3P0SS_CTRL_XHCI_RSVDZA4 Register

1 USB3P0SS_CTRL_XHCI_RSVDZA4 Register (Offset = A4h) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Table 14-21079. Instance Table

Instance Name	Physical Address
USB0	**0F40 00A4h**

Figure 14-6965. USB3P0SS_CTRL_XHCI_RSVDZA4 Name Register

31	30	29	28	27	26	25	24
RSVDZ_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDZ_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDZ_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDZ_1							
R							
0h							

Table 14-21081. USB3P0SS_CTRL_XHCI_RSVDZA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.76 USB3P0SS_CTRL_XHCI_RSVDZA8 Register

1 USB3P0SS_CTRL_XHCI_RSVDZA8 Register (Offset = A8h) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Table 14-21082. Instance Table

Instance Name	Physical Address
USB0	0F40 00A8h

Figure 14-6966. USB3P0SS_CTRL_XHCI_RSVDZA8 Name Register

31	30	29	28	27	26	25	24
RSVDZ_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDZ_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDZ_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDZ_1							
R							
0h							

Table 14-21084. USB3P0SS_CTRL_XHCI_RSVDZA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.77 USB3P0SS_CTRL_XHCI_RSVDZAC Register

1 USB3P0SS_CTRL_XHCI_RSVDZAC Register (Offset = ACh) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Table 14-21085. Instance Table

Instance Name	Physical Address
USB0	**0F40 00ACh**

Figure 14-6967. USB3P0SS_CTRL_XHCI_RSVDZAC Name Register

31	30	29	28	27	26	25	24
RSVDZ_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDZ_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDZ_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDZ_1							
R							
0h							

Table 14-21087. USB3P0SS_CTRL_XHCI_RSVDZAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.78 USB3P0SS_CTRL_XHCI_DCBAAP_LO Register

1 USB3P0SS_CTRL_XHCI_DCBAAP_LO Register (Offset = B0h) [reset = 0h]

Device Context Base Address Array Pointer Register (DCBAAP_LO). The Device Context Base Address Array Pointer Register identifies the base address of the Device Context Base Address Array. The memory structure referenced by this physical memory pointer is assumed to be physically contiguous and 64-byte aligned.

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Table 14-21088. Instance Table

Instance Name	Physical Address
USB0	**0F40 00B0h**

Figure 14-6968. USB3P0SS_CTRL_XHCI_DCBAAP_LO Name Register

31	30	29	28	27	26	25	24
DCBAAPTR_L							
R/W							
0h							
23	22	21	20	19	18	17	16
DCBAAPTR_L							
R/W							
0h							
15	14	13	12	11	10	9	8
DCBAAPTR_L							
R/W							
0h							
7	6	5	4	3	2	1	0
DCBAAPTR_L		RSVDZ1					
R/W		R					
0h		0h					

Table 14-21090. USB3P0SS_CTRL_XHCI_DCBAAP_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	DCBAAPTR_L	R/W	0h	Device Context Base Address Array Pointer, RW. Default = 0. This field defines low order bits of the 64-bit base address of the Device Context Pointer Array. A table of address pointers that reference Device Context structures for the devices attached to the host. Reset Source: rst_mod_g_rst_n
5:0	RSVDZ1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.79 USB3P0SS_CTRL_XHCI_DCBAAP_HI Register

1 USB3P0SS_CTRL_XHCI_DCBAAP_HI Register (Offset = B4h) [reset = 0h]

Device Context Base Address Array Pointer Register (DCBAAP_HI). The Device Context Base Address Array Pointer Register identifies the base address of the Device Context Base Address Array. The memory structure referenced by this physical memory pointer is assumed to be physically contiguous and 64-byte aligned.

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Table 14-21091. Instance Table

Instance Name	Physical Address
USB0	**0F40 00B4h**

Figure 14-6969. USB3P0SS_CTRL_XHCI_DCBAAP_HI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DCBAAPTR_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DCBAAPTR_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DCBAAPTR_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DCBAAPTR_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21093. USB3P0SS_CTRL_XHCI_DCBAAP_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DCBAAPTR_H	R/W	0h	Device Context Base Address Array Pointer, RW. Default = 0. This field defines high order bits of the 64-bit base address of the Device Context Pointer Array. A table of address pointers that reference Device Context structures for the devices attached to the host. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.80 USB3P0SS_CTRL_XHCI_CONFIG Register

1 USB3P0SS_CTRL_XHCI_CONFIG Register (Offset = B8h) [reset = 0h]

Configure Register (CONFIG). This register defines runtime xHC configuration parameters.

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Table 14-21094. Instance Table

Instance Name	Physical Address
USB0	**0F40 00B8h**

Figure 14-6970. USB3P0SS_CTRL_XHCI_CONFIG Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
MAXSLOTSEN							
R/W							
0h							

Table 14-21096. USB3P0SS_CTRL_XHCI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
7:0	MAXSLOTSEN	R/W	0h	Max Device Slots Enabled [MaxSlotsEn], RW. Default = 0. This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously. e.g. A value of 16 specifies that Device Slots 1 to 16 are active. A value of 0 disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references. This field shall not be modified by software if the xHC is running [Run/Stop [R/S] = 1]. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.81 USB3P0SS_CTRL_XHCI_RSVDZBC Register

1 USB3P0SS_CTRL_XHCI_RSVDZBC Register (Offset = BCh) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Table 14-21097. Instance Table

Instance Name	Physical Address
USB0	**0F40 00BCh**

Figure 14-6971. USB3P0SS_CTRL_XHCI_RSVDZBC Name Register

31	30	29	28	27	26	25	24
RSVDZ_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDZ_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDZ_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDZ_1							
R							
0h							

Table 14-21099. USB3P0SS_CTRL_XHCI_RSVDZBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.82 USB3P0SS_CTRL_XHCI_RSVDZ_OP_j Register

1 USB3P0SS_CTRL_XHCI_RSVDZ_OP_j Register (Offset = C0h + formula) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Offset = (j * 4h); where j = 0 to 239d

Table 14-21100. Instance Table

Instance Name	Physical Address
USB0	0F40 00C0h + formula

Figure 14-6972. USB3P0SS_CTRL_XHCI_RSVDZ_OP_j Name Register

31	30	29	28	27	26	25	24
RSVDZ_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDZ_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDZ_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDZ_1							
R							
0h							

Table 14-21102. USB3P0SS_CTRL_XHCI_RSVDZ_OP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.83 USB3P0SS_CTRL_XHCI_PORTSC1USB2 Register

1 USB3P0SS_CTRL_XHCI_PORTSC1USB2 Register (Offset = 480h) [reset = 2A0h]

Port Status and Control Register for USB2 protocol port. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21103. Instance Table

Instance Name	Physical Address
USB0	**0F40 0480h**

Figure 14-6973. USB3P0SS_CTRL_XHCI_PORTSC1USB2 Name Register

31	30	29	28	27	26	25	24
RSVDZ_4	DR	RSVDZ_3		WOE	WDE	WCE	CAS
R	R	R		R/W	R/W	R/W	R
0h	0h	0h		0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDZ_2	PLC	PRC	OCC	WRC	PEC	CSC	LWS
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PIC		PORTSPEED				PP	PLS
R/W		R				R/W	R/W
0h		0h				1h	5h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLS			PR	OCA	RSVDZ_1	PED	CCS
R/W			R/W1TS	R	R	R/W1TC	R
5h			0h	0h	0h	0h	0h

Table 14-21105. USB3P0SS_CTRL_XHCI_PORTSC1USB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RSVDZ_4	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
30	DR	R	0h	Device Removable [DR], RO. This flag indicates if this port has a removable device attached. '0' = Device is removable. '1' = Device is non-removable. Reset Source: rst_mod_g_rst_n
29:28	RSVDZ_3	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
27	WOE	R/W	0h	Wake on Over-current Enable [WOE], RWS. Default = '0'. Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up events. Refer to section 4.15 of xHCI specification for operational model. Reset Source: rst_mod_g_rst_n

Table 14-21105. USB3P0SS_CTRL_XHCI_PORTSC1USB2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	WDE	R/W	0h	Wake on Disconnect Enable [WDE], RWS. Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up events. Refer to section 4.15 of xHCI specification for operational model. Reset Source: rst_mod_g_rst_n
25	WCE	R/W	0h	Wake on Connect Enable [WCE], RWS. Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up events. Refer to section 4.15 of xHCI specification for operational model. Reset Source: rst_mod_g_rst_n
24	CAS	R	0h	Cold Attach Status [CAS], RO. Default = '0'. '1' = Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Refer to sections 4.19.8 of xHCI specification for more details on the Cold Attach Status [CAS] assertion conditions. Software shall clear this bit by writing a '1' to WPR or the xHC shall clear this bit if CCS transitions to '1'. This flag is '0' for USB2 protocol ports. Reset Source: rst_mod_g_rst_n
23	RSVDZ_2	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
22	PLC	R/W1TC	0h	Port Link State Change [PLC], RW1CS. Default = '0'. This flag is set to '1' due to the following PLS transitions: U3 -> Resume [Wakeup signaling from a device], Resume -> Recovery -> U0 [Device Resume complete [USB3 protocol ports only]], Resume -> U0 [Device Resume complete [USB2 protocol ports only]], U3 -> Recovery -> U0 [Software Resume complete [USB3 protocol ports only]], U3 -> U0 [Software Resume complete [USB2 protocol ports only]], U2 -> U0 [L1 Resume complete [USB2 protocol ports only]], U0 -> U0 [L1 Entry Reject [USB2 protocol ports only]], Any state -> Inactive [Error [USB3 protocol ports only]]. Note that this flag shall not be set if the PLS transition was due to software setting PP to 0. Refer to section 4.23.5 of xHCI specification for more information. '0' = No change. '1' = Link Status Changed. Software shall clear this bit by writing a '1' to it. Refer to PLC Condition: references in section 4.19.1 for the specific port state transitions that set this flag. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n
21	PRC	R/W1TC	0h	Port Reset Change [PRC], RW1CS. Default = '0'. This flag is set to '1' due to a '1' to '0' transition of Port Reset [PR], e.g. when any reset processing [Warm or Hot] on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5 of xHCI specification. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n

Table 14-21105. USB3P0SS_CTRL_XHCI_PORTSC1USB2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	OCC	R/W1TC	0h	Over-current Change [OCC], RW1CS. Default = '0'. This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active [OCA]. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n
19	WRC	R/W1TC	0h	Warm Port Reset Change [WRC], RW1CS/RsvdZ. Default = '0'. This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.1 of xHCI specification. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ. Reset Source: rst_mod_g_rst_n
18	PEC	R/W1TC	0h	Port Enabled/Disabled Change [PEC], RW1CS. Default = '0'. '1' = change in PED. '0' = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. This bit shall be set to '1' only when the port is disabled due to the appropriate conditions existing at the EOF2 point [refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error]. Reset Source: rst_mod_g_rst_n
17	CSC	R/W1TC	0h	Connect Status Change [CSC], RW1CS. Default = '0'. '1' = Change in CCS. '0' = No change. This flag indicates a change has occurred in the ports Current Connect Status [CCS] or Cold Attach Status [CAS] bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to '0', or the CAS transition was due to software setting WPR to '1'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be setting an already-set bit [i.e., the bit will remain 1]. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n
16	LWS	R/W	0h	Port Link State Write Strobe [LWS], RW. Default = '0'. When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'. Reset Source: rst_mod_g_rst_n
15:14	PIC	R/W	0h	Port Indicator Control [PIC], RWS. Default = '0'. Writing to these bits has no effect if the Port Indicators [PIND] bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: 0: Port indicators are off, 1: Amber, 2: Green, 3: Undefined. Refer to the USB2 Specification section 11.5.3 for a description on how these bits shall be used. This field is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n

Table 14-21105. USB3P0SS_CTRL_XHCI_PORTSC1USB2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:10	PORTSPEED	R	0h	Port Speed [Port Speed], ROS. Default = '0'. This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected [CCS = '1'] in all other cases this field shall indicate Undefined Speed. Possible values: 0: Undefined Speed 1-15: Protocol Speed ID [PSI], refer to section 7.2.1 of xHCI specification for the definition of PSIV field in the PSI Dword. Note: This field is invalid on a USB2 protocol port until after the port is reset. Reset Source: rst_mod_g_rst_n
9	PP	R/W	1h	Port Power [PP], RWS. Default = '1'. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether [VBus] power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State [PLS] changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. After modifying PP, software shall read PP and confirm that it has reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. '0' = This port is in the Powered-off state. '1' = This port is not in the Powered-off state. If the Port Power Control [PPC] flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ['0' = off, '1'=on]. If the Port Power Control [PPC] flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' [removing power from the port]. Refer to section 4.19.4 for more information. Reset Source: rst_mod_g_rst_n

Table 14-21105. USB3P0SS_CTRL_XHCI_PORTSC1USB2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	PLS	R/W	5h	Port Link State [PLS], RWS. Default = RxDetect ['5']. This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Values: 0: The link shall transition to a U0 state from any of the U states. 2: The link should transition to the U2 State. 3: The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: USB3 protocol ports only. If the port is in the Disabled state [PLS = Disabled, PP = 1], then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 10: USB3 protocol ports only. If CTC bit in HCCPARAMS2 is 2, it shall enable a link transition to the Compliance state, i.e. CTE = 1. Refer to section 4.19.1.2.4.1 of xHCI specification for more information. 15: If the port is in the U3 state [PLS = U3], then the link shall remain in the U3 state and the port shall transition to the Resume substate, else ignored. Refer to section 4.15.2 of xHCI specification for more information. others: Ignored. State Encoding: 0: Link is in the U0 State, 1: Link is in the U1 State, 2: Link is in the U2 State, 3: Link is in the U3 State [Device Suspended], 4: Link is in the Disabled State, 5: Link is in the RxDetect State, 6: Link is in the Inactive State, 7: Link is in the Polling State, 8: Link is in the Recovery State, 9: Link is in the Hot Reset State, 10 Link is in the Compliance Mode State, 11: Link is in the Test Mode State, 12-14: Reserved, 15: Link is in the Resume State. Note: The Port Link State Write Strobe [LWS] shall also be set to '1' to write this field. This field is undefined if PP = '0'. Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of '0' shall deassert L1 signaling on the USB. Writing a value of '1' shall have no effect. The U1 state shall never be reported by a USB2 protocol port. Note: Transitions between different states are not reflected until the transition is complete. Refer to section 4.19 of xHCI specification for PLS transition conditions. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field. Refer to the USB2 LPM ECR for more information on USB link power management operation. Reset Source: rst_mod_g_rst_n

Table 14-21105. USB3P0SS_CTRL_XHCI_PORTSC1USB2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PR	R/W1TS	0h	Port Reset [PR], RW1S. Default = '0'. '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit generating a '0' to '1' transition, the bus reset sequence is initiated. USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1 of xHCI specification. This flag is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n
3	OCA	R	0h	Over-current Active [OCA], RO. Default = '0'. '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed. Reset Source: rst_mod_g_rst_n
2	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	PED	R/W1TC	0h	Port Enabled/Disabled [PED], RW1CS. Default = '0'. '1' = Enabled. '0' = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled [PED = '0'] downstream propagation of data is blocked on this port, except for reset. When the port is in the Disabled state, software shall reset the port [PR = '1'] to transition PED to '1' and the port to the Enabled state. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bit. This flag is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n
0	CCS	R	0h	Current Connect Status [CCS], ROS. Default = '0'. '1' = A device is connected to the port. '0' = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change [CSC] bit to be set to '1'. Refer to sections 4.19.3 and 4.19.4 of xHCI specification for more details on the Connect Status Change [CSC] assertion conditions. This flag is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.84 USB3P0SS_CTRL_XHCI_PORTPMSC1USB2 Register

1 USB3P0SS_CTRL_XHCI_PORTPMSC1USB2 Register (Offset = 484h) [reset = 0h]

The USB2 Port Power Management Status and Control register. Provides the USB2 LPM parameters necessary for the xHC to generate a LPM Token to the downstream device. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21106. Instance Table

Instance Name	Physical Address
USB0	**0F40 0484h**

Figure 14-6974. USB3P0SS_CTRL_XHCI_PORTPMSC1USB2 Name Register

31	30	29	28	27	26	25	24
PTC				RSVDP			
R/W				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP							HLE
R							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
L1DS							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BESL				RWE	L1S		
R/W				R/W	R		
0h				0h	0h		

Table 14-21108. USB3P0SS_CTRL_XHCI_PORTPMSC1USB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PTC	R/W	0h	Port Test Control, RW. Default = '0'. When this field is '0', the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state [PLS = Disabled]. If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 for the operational model for using these test modes. The encoding of the Test Mode bits for a USB2 protocol port are: 0: Test mode not enabled 1: Test J_STATE 2: Test K_STATE 3: Test SE0_NAK 4: Test Packet 5: Test FORCE_ENABLE 6-14: Reserved. 15: Port Test Control Error. Refer to the sections 7.1.20 and 11.24.2.13 of the USB2 spec for more information on Test Modes. Reset Source: rst_mod_g_rst_n

Table 14-21108. USB3P0SS_CTRL_XHCI_PORTPMSC1USB2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:17	RSVDP	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
16	HLE	R/W	0h	Hardware LPM Enable [HLE], RW. Default = '0'. If this bit is set to '1', then hardware controlled LPM shall be enabled for this port. Refer to section 4.23.5.1.1.1 of xHCI specification. If the USB2 Hardware LPM Capability is not supported [HLC = '0'] this field shall be RsvdZ. Reset Source: rst_mod_g_rst_n
15:8	L1DS	R/W	0h	L1 Device Slot, RW. Default = 0. System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of '0' indicates no device is present. The xHC uses this field to lookup information necessary to generate the LPM Token packet. Reset Source: rst_mod_g_rst_n
7:4	BESL	R/W	0h	Best Effort Service Latency [BESL], RW. Default = 0. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it [the xHC] initiates an exit from L1. The BESL value encoding is defined in Table 13. Note that the BESL field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 of xHCI specification for more information on BESL use. Refer to section 5.2.5 of xHCI specification for information on how DBESL may be used to establish an initial value for BESL. Reset Source: rst_mod_g_rst_n
3	RWE	R/W	0h	Remote Wake Enable [RWE], RW. Default = '0'. System software sets this flag to enable or disable the device for remote wake from L1. The value of this flag shall temporarily [while in L1] override the current setting of the Remote Wake feature set by the standard Set/ClearFeature[] commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9. Reset Source: rst_mod_g_rst_n
2:0	L1S	R	0h	L1 Status [L1S], RO. Default = 0. This field is used by software to determine whether an L1-based suspend request [LPM transaction] was successful, specifically: 0: Invalid - This field shall be ignored by software. 1: Success - Port successfully transitioned to L1 [ACK] 2: Not Yet - Device is unable to enter L1 at this time [NYET] 3: Not Supported - Device does not support L1 transitions [STALL] 4: Timeout/Error - Device failed to respond to the LPM Transaction or an error occurred 5-7: Reserved The value of this field is only valid when the port resides in the L0 or L1 state [PLS = 0 or 2]. Refer to section 4.23.5.1.1 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.85 USB3P0SS_CTRL_XHCI_RSVDP1USB2 Register

1 USB3P0SS_CTRL_XHCI_RSVDP1USB2 Register (Offset = 488h) [reset = 0h]

Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits.

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Table 14-21109. Instance Table

Instance Name	Physical Address
USB0	**0F40 0488h**

Figure 14-6975. USB3P0SS_CTRL_XHCI_RSVDP1USB2 Name Register

31	30	29	28	27	26	25	24
RSVDP_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP_1							
R							
0h							

Table 14-21111. USB3P0SS_CTRL_XHCI_RSVDP1USB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP_1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.86 USB3P0SS_CTRL_XHCI_PORT1HLPMC Register

1 USB3P0SS_CTRL_XHCI_PORT1HLPMC Register (Offset = 48Ch) [reset = 0h]

The optional normative USB2 Port Hardware LPM Control register provides the USB2 LPM parameters necessary for the xHC to automatically generate a LPM Token to the downstream device. Refer to section 4.23.5.1.1.1 of xHCI specification for more information. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21112. Instance Table

Instance Name	Physical Address
USB0	**0F40 048Ch**

Figure 14-6976. USB3P0SS_CTRL_XHCI_PORT1HLPMC Name Register

31	30	29	28	27	26	25	24
RSVDP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP		BESLD				L1_TIMEOUT	
R		R/W				R/W	
0h		0h				0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
L1_TIMEOUT						HIRDM	
R/W						R/W	
0h						0h	

Table 14-21114. USB3P0SS_CTRL_XHCI_PORT1HLPMC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RSVDP	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
13:10	BESLD	R/W	0h	Best Effort Service Latency Deep [BESLD], RWS. Default = '0'. System software sets this field to indicate to the recipient device how long the xHC will drive resume on an exit from U2. Refer to section 4.23.5.1.1.1 of xHCI specification for more information on BESLD use. The BESLD value encoding is defined in Table 13. Refer to section 5.2.6 of xHCI specification for information on how DBESLD may be used to establish an initial value for BESLD. Reset Source: rst_mod_g_rst_n

Table 14-21114. USB3P0SS_CTRL_XHCI_PORT1HLPMC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:2	L1_TIMEOUT	R/W	0h	L1 Timeout, RWS. Default = 00h. Timeout value for the L1 inactivity timer [LPM Timer]. This field shall be set to 00h by the assertion of PR to '1'. Refer to section 4.23.5.1.1.1 of xHci specification for more information on L1 Timeout operation. The following are permissible values: 00h 128 us. [default] 01h 256 us. 02h 512 us. 03h 768 us. ... FFh 65,280 us. Reset Source: rst_mod_g_rst_n
1:0	HIRDM	R/W	0h	Host Initiated Resume Duration Mode [HIRDM], RWS. Default = 0h. Indicates which HIRD value should be used. The following are permissible values: 0: Initiate L1 using BESL only on timeout. [default] 1: Initiate L1 using BESLD on timeout. If rejected by device, initiate L1 using BESL. 3-2: Reserved. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.87 USB3P0SS_CTRL_XHCI_PORTSC1USB3 Register

1 USB3P0SS_CTRL_XHCI_PORTSC1USB3 Register (Offset = 490h) [reset = 2A0h]

Port Status and Control Register for USB3 protocol port. The register cannot be accessed if USB3 PHY is not active (i.e. when there is no USB3 PHY or when USB3 PHY has not started providing USB3 PIPE PCLK after reset).

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Table 14-21115. Instance Table

Instance Name	Physical Address
USB0	**0F40 0490h**

Figure 14-6977. USB3P0SS_CTRL_XHCI_PORTSC1USB3 Name Register

31	30	29	28	27	26	25	24
WPR	DR	RSVDZ_2		WOE	WDE	WCE	CAS
R/W1TS	R	R		R/W	R/W	R/W	R
0h	0h	0h		0h	0h	0h	0h
23	22	21	20	19	18	17	16
CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PIC		PORTSPEED				PP	PLS
R/W		R				R/W	R/W
0h		0h				1h	5h
7	6	5	4	3	2	1	0
PLS			PR	OCA	RSVDZ_1	PED	CCS
R/W			R/W1TS	R	R	R/W1TC	R
5h			0h	0h	0h	0h	0h

Table 14-21117. USB3P0SS_CTRL_XHCI_PORTSC1USB3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WPR	R/W1TS	0h	Warm Port Reset [WPR], RW1S. Default = '0'. When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return 0 when read. Refer to section 4.19.5.1 of xHCI specification. Reset Source: rst_mod_g_rst_n
30	DR	R	0h	Device Removable [DR], RO. This flag indicates if this port has a removable device attached. '0' = Device is removable. '1' = Device is non-removable. Reset Source: rst_mod_g_rst_n
29:28	RSVDZ_2	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21117. USB3P0SS_CTRL_XHCI_PORTSC1USB3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	WOE	R/W	0h	Wake on Over-current Enable [WOE], RWS. Default = '0'. Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up events. Refer to section 4.15 of xHCI specification for operational model. Reset Source: rst_mod_g_rst_n
26	WDE	R/W	0h	Wake on Disconnect Enable [WDE], RWS. Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up events. Refer to section 4.15 of xHCI specification for operational model. Reset Source: rst_mod_g_rst_n
25	WCE	R/W	0h	Wake on Connect Enable [WCE], RWS. Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up events. Refer to section 4.15 of xHCI specification for operational model. Reset Source: rst_mod_g_rst_n
24	CAS	R	0h	Cold Attach Status [CAS], RO. Default = '0'. '1' = Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Refer to sections 4.19.8 of xHCI specification for more details on the Cold Attach Status [CAS] assertion conditions. Software shall clear this bit by writing a '1' to WPR or the xHC shall clear this bit if CCS transitions to '1'. This flag is 0 if PP is 0 or for USB2 protocol ports. Note: Additionally to the xHCI spec the CAS may be set in D1/D2 state. If customer's PLL lock time ensures finishing LFPS in tPollingLFPSTimeout [360ms] the SW driver may ignore the CAS and wait for PORTSC.CCS. It prevents additional reset on USB port. However, handling CAS in normal way should not have any negative impact on the device. Reset Source: rst_mod_g_rst_n
23	CEC	R/W1TC	0h	Port Config Error Change [CEC], RW1CS. Default = '0'. This flag indicates that the port failed to configure its link partner. '0' = No change. '1' = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n
22	PLC	R/W1TC	0h	Port Link State Change [PLC], RW1CS. Default = '0'. This flag is set to '1' due to the following PLS transitions: U3 -> Resume [Wakeup signaling from a device], Resume -> Recovery -> U0 [Device Resume complete [USB3 protocol ports only]], Resume -> U0 [Device Resume complete [USB2 protocol ports only]], U3 -> Recovery -> U0 [Software Resume complete [USB3 protocol ports only]], U3 -> U0 [Software Resume complete [USB2 protocol ports only]], U2 -> U0 [L1 Resume complete [USB2 protocol ports only]], U0 -> U0 [L1 Entry Reject [USB2 protocol ports only]], Any state -> Inactive [Error [USB3 protocol ports only]]. Note that this flag shall not be set if the PLS transition was due to software setting PP to 0. Refer to section 4.23.5 of xHCI specification for more information. '0' = No change. '1' = Link Status Changed. Software shall clear this bit by writing a '1' to it. Refer to PLC Condition: references in section 4.19.1 for the specific port state transitions that set this flag. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n

Table 14-21117. USB3P0SS_CTRL_XHCI_PORTSC1USB3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PRC	R/W1TC	0h	Port Reset Change [PRC], RW1CS. Default = '0'. This flag is set to '1' due to a '1' to '0' transition of Port Reset [PR], e.g. when any reset processing [Warm or Hot] on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5 of xHCI specification. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n
20	OCC	R/W1TC	0h	Over-current Change [OCC], RW1CS. Default = '0'. This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active [OCA]. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n
19	WRC	R/W1TC	0h	Warm Port Reset Change [WRC], RW1CS. Default = '0'. This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.1 of xHCI specification. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n
18	PEC	R/W1TC	0h	Port Enabled/Disabled Change [PEC], RW1CS. Default = '0'. '1' = change in PED. '0' = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. This bit shall never be set to '1'. Reset Source: rst_mod_g_rst_n
17	CSC	R/W1TC	0h	Connect Status Change [CSC], RW1CS. Default = '0'. '1' = Change in CCS. '0' = No change. This flag indicates a change has occurred in the ports Current Connect Status [CCS] or Cold Attach Status [CAS] bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to '0', or the CAS transition was due to software setting WPR to '1'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be setting an already-set bit [i.e., the bit will remain 1]. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of xHCI specification for more information on change bit usage. Reset Source: rst_mod_g_rst_n
16	LWS	R/W	0h	Port Link State Write Strobe [LWS], RW. Default = '0'. When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'. Reset Source: rst_mod_g_rst_n

Table 14-21117. USB3P0SS_CTRL_XHCI_PORTSC1USB3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	PIC	R/W	0h	Port Indicator Control [PIC], RWS. Default = '0'. Writing to these bits has no effect if the Port Indicators [PIND] bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: 0: Port indicators are off, 1: Amber, 2: Green, 3: Undefined. This field is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n
13:10	PORTSPEED	R	0h	Port Speed [Port Speed], ROS. Default = '0'. This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected [CCS = '1'] in all other cases this field shall indicate Undefined Speed. Possible values: 0: Undefined Speed 1-15: Protocol Speed ID [PSI], refer to section 7.2.1 of xHCI specification for the definition of PSIV field in the PSI Dword. Reset Source: rst_mod_g_rst_n
9	PP	R/W	1h	Port Power [PP], RWS. Default = '1'. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether [VBus] power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State [PLS] changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. After modifying PP, software shall read PP and confirm that it has reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. '0' = This port is in the Powered-off state. '1' = This port is not in the Powered-off state. If the Port Power Control [PPC] flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ['0' = off, '1'=on]. If the Port Power Control [PPC] flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' [removing power from the port]. Refer to section 4.19.4 for more information. Reset Source: rst_mod_g_rst_n

Table 14-21117. USB3P0SS_CTRL_XHCI_PORTSC1USB3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	PLS	R/W	5h	Port Link State [PLS], RWS. Default = RxDetect ['5']. This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Values: 0: The link shall transition to a U0 state from any of the U states. 3: The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: If the port is in the Disabled state [PLS = Disabled, PP = '1'], then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 1-2,4,6-15: Ignored. State Encoding: 0: Link is in the U0 State, 1: Link is in the U1 State, 2: Link is in the U2 State, 3: Link is in the U3 State [Device Suspended], 4: Link is in the Disabled State, 5: Link is in the RxDetect State, 6: Link is in the Inactive State, 7: Link is in the Polling State, 8: Link is in the Recovery State, 9: Link is in the Hot Reset State, 10 Link is in the Compliance Mode State, 11: Link is in the Test Mode State, 12-14: Reserved, 15: Link is in the Resume State. Note: The Port Link State Write Strobe [LWS] shall also be set to '1' to write this field. This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until the transition is complete. Refer to section 4.19 of xHCI specification for PLS transition conditions. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field. Reset Source: rst_mod_g_rst_n
4	PR	R/W1TS	0h	Port Reset [PR], RW1S. Default = '0'. '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit generating a '0' to '1' transition, the bus reset sequence is initiated. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. This flag is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n
3	OCA	R	0h	Over-current Active [OCA], RO. Default = '0'. '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed. Reset Source: rst_mod_g_rst_n
2	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21117. USB3P0SS_CTRL_XHCI_PORTSC1USB3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PED	R/W1TC	0h	Port Enabled/Disabled [PED], RW1CS. Default = '0'. '1' = Enabled. '0' = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled [PED = '0'] downstream propagation of data is blocked on this port, except for reset. When the port is in the Polling state [after detecting an attach], the port shall automatically transition to the Enabled state and set PED to '1' upon the completion of successful link training. When the port is in the Disabled state, software shall write a 5 [RxDetect] to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2 of xHCI specification. PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. Refer to Port Reset [PR] bit for more information on how the PED bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bit. This flag is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n
0	CCS	R	0h	Current Connect Status [CCS], ROS. Default = '0'. '1' = A device is connected to the port. '0' = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change [CSC] bit to be set to '1'. Refer to sections 4.19.3 and 4.19.4 of xHCI specification for more details on the Connect Status Change [CSC] assertion conditions. This flag is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.88 USB3P0SS_CTRL_XHCI_PORTPMSC1USB3 Register

1 USB3P0SS_CTRL_XHCI_PORTPMSC1USB3 Register (Offset = 494h) [reset = 0h]

USB3 Port Power Management Status and Control register. Controls the SuperSpeed USB link U-State timeouts. The register cannot be accessed if USB3 PHY is not active (i.e. when there is no USB3 PHY or when USB3 PHY has not started providing USB3 PIPE PCLK after reset).

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Table 14-21118. Instance Table

Instance Name	Physical Address
USB0	**0F40 0494h**

Figure 14-6978. USB3P0SS_CTRL_XHCI_PORTPMSC1USB3 Name Register

31	30	29	28	27	26	25	24
RSVDP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP							FLA
R							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
U2_TIMEOUT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
U1_TIMEOUT							
R/W							
0h							

Table 14-21120. USB3P0SS_CTRL_XHCI_PORTPMSC1USB3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RSVDP	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21120. USB3P0SS_CTRL_XHCI_PORTPMSC1USB3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	FLA	R/W	0h	Force Link PM Accept [FLA], RW. Default = '0'. When this bit is set to '1', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit asserted ['1']. When this bit is cleared to '0', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit de-asserted ['0']. This flag shall be set to '0' by the assertion of PR to '1' or when CCS = transitions from '0' to '1'. Writes to this flag have no effect if PP = '0'. The Set Link Function LMP is sent by the xHC to the device connected on this port when this bit transitions from '0' to '1' or '1' to '0'. Refer to Sections 8.4.2 and 10.14.2.2 of the USB3 specification for more details. Improper use of the SS Force_LinkPM_Accept functionality can impact the performance of the link significantly. This bit shall only be used for compliance and testing purposes. Software shall ensure that there are no pending packets at the link level before setting this bit. This flag is '0' if PP is '0'. Reset Source: rst_mod_g_rst_n
15:8	U2_TIMEOUT	R/W	0h	U2 Timeout, RWS. Default = 0. Timeout value for U2 inactivity timer. If equal to FFh, the port is disabled from initiating U2 entry. This field shall be set to '0' by the assertion of PR to '1'. Refer to section 4.19.4.1 of xHCI specification for more information on U2 Timeout operation. The following are permissible values: 00h Zero [default] 01h 256 us 02h 512 us ... FEh 65,.024 ms FFh Infinite A U2 Inactivity Timeout LMP shall be sent by the xHC to the device connected on this port when this field is written. Refer to Sections 8.4.3 and 10.4.2.10 of the USB3 specification for more details. Reset Source: rst_mod_g_rst_n
7:0	U1_TIMEOUT	R/W	0h	U1 Timeout, RWS. Default = 0. Timeout value for U1 inactivity timer. If equal to FFh, the port is disabled from initiating U1 entry. This field shall be set to '0' by the assertion of PR to '1'. Refer to section 4.19.4.1 of xHCI specification for more information on U1 Timeout operation. The following are permissible values: 00h Zero [default] 01h 1 us. 02h 2 us. ... 7Fh 127 us. 80h - FEh Reserved FFh Infinite Reset Source: rst_mod_g_rst_n

14.9.2.3.2.89 USB3P0SS_CTRL_XHCI_PORTLI1 Register

1 USB3P0SS_CTRL_XHCI_PORTLI1 Register (Offset = 498h) [reset = 0h]

The USB3 Port Link Info register reports the Link Error Count.

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Table 14-21121. Instance Table

Instance Name	Physical Address
USB0	**0F40 0498h**

Figure 14-6979. USB3P0SS_CTRL_XHCI_PORTLI1 Name Register

31	30	29	28	27	26	25	24
RSVDP							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP							
R							
0h							
15	14	13	12	11	10	9	8
LEC							
R							
0h							
7	6	5	4	3	2	1	0
LEC							
R							
0h							

Table 14-21123. USB3P0SS_CTRL_XHCI_PORTLI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	LEC	R	0h	Link Error Count, RO. Default = '0'. This field returns the number of link errors detected by the port. This value shall be reset to '0' by the assertion of a Chip Hardware Reset, HCRST, when PR transitions from 1 to 0, or when CCS = transitions from '0' to '1'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.90 USB3P0SS_CTRL_XHCI_RSVDP1USB3 Register

1 USB3P0SS_CTRL_XHCI_RSVDP1USB3 Register (Offset = 49Ch) [reset = 0h]

Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits.

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Table 14-21124. Instance Table

Instance Name	Physical Address
USB0	**0F40 049Ch**

Figure 14-6980. USB3P0SS_CTRL_XHCI_RSVDP1USB3 Name Register

31	30	29	28	27	26	25	24
RSVDP_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP_1							
R							
0h							

Table 14-21126. USB3P0SS_CTRL_XHCI_RSVDP1USB3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP_1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.91 USB3P0SS_CTRL_XHCI_MFINDEX Register

1 USB3P0SS_CTRL_XHCI_MFINDEX Register (Offset = 2000h) [reset = 0h]

This register is used by the system software to determine the current periodic frame. The register value is incremented every 125 microseconds (once each microframe). This register is only incremented while Run/Stop (R/S) = '1'. The value of this register affects the SOF value generated by USB2 Bus Instances.

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Table 14-21127. Instance Table

Instance Name	Physical Address
USB0	**0F40 2000h**

Figure 14-6981. USB3P0SS_CTRL_XHCI_MFINDEX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVDZ1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVDZ1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RSVDZ1</td><td colspan="6">MFINDEX</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MFINDEX</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21129. USB3P0SS_CTRL_XHCI_MFINDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RSVDZ1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
13:0	MFINDEX	R	0h	Microframe Index, RO. The value in this register increments at the end of each microframe [e.g. 125us.]. Bits [13:3] may be used to determine the current 1ms Frame Index. Note: Setting frindex_wr_en to '1' [bit 31 of XECP_CMDM_CTRL_REG3] enables software writes to this field. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.92 USB3P0SS_CTRL_XHCI_RSVDZ_RT_j Register

1 USB3P0SS_CTRL_XHCI_RSVDZ_RT_j Register (Offset = 2004h + formula) [reset = 0h]

Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits.

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Offset = (j * 4h); where j = 0 to 6d

Table 14-21130. Instance Table

Instance Name	Physical Address
USB0	**0F40 2004h + formula**

Figure 14-6982. USB3P0SS_CTRL_XHCI_RSVDZ_RT_j Name Register

31	30	29	28	27	26	25	24
RSVDZ_1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDZ_1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDZ_1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDZ_1							
R							
0h							

Table 14-21132. USB3P0SS_CTRL_XHCI_RSVDZ_RT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDZ_1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.93 USB3P0SS_CTRL_XHCI_IMAN0 Register

1 USB3P0SS_CTRL_XHCI_IMAN0 Register (Offset = 2020h) [reset = 0h]

Interrupter Management Register (IMAN). The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

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Table 14-21133. Instance Table

Instance Name	Physical Address
USB0	**0F40 2020h**

Figure 14-6983. USB3P0SS_CTRL_XHCI_IMAN0 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVDP1						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-21135. USB3P0SS_CTRL_XHCI_IMAN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	IE	R/W	0h	Interrupt Enable [IE], RW. Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ['1'], the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is '0', then the Interrupter is prohibited from generating interrupts. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	Interrupt Pending [IP], RW1C. Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of the xHCI specification for the conditions that modify the state of this flag. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.94 USB3P0SS_CTRL_XHCI_IMOD0 Register

1 USB3P0SS_CTRL_XHCI_IMOD0 Register (Offset = 2024h) [reset = FA0h]

Interrupter Moderation Register (IMOD). The Interrupter Moderation Register controls the interrupt moderation feature of an Interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

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Table 14-21136. Instance Table

Instance Name	Physical Address
USB0	0F40 2024h

Figure 14-6984. USB3P0SS_CTRL_XHCI_IMOD0 Name Register

31	30	29	28	27	26	25	24
IMODC							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IMODC							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IMODI							
R/W							
FA0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IMODI							
R/W							
FA0h							

Table 14-21138. USB3P0SS_CTRL_XHCI_IMOD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC], RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is zero, the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI], RW. Default = 'hFA0' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of zero disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The IMODI field shall default to 'hFA0' [1 ms] upon initialization and reset. It may be loaded with an alternative value by software when the Interrupter is initialized. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.95 USB3P0SS_CTRL_XHCI_ERSTSZ0 Register

1 USB3P0SS_CTRL_XHCI_ERSTSZ0 Register (Offset = 2028h) [reset = 0h]

Event Ring Segment Table Size Register (ERSTSZ). The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment Table.

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Table 14-21139. Instance Table

Instance Name	Physical Address
USB0	0F40 2028h

Figure 14-6985. USB3P0SS_CTRL_XHCI_ERSTSZ0 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERSTS							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERSTS							
R/W							
0h							

Table 14-21141. USB3P0SS_CTRL_XHCI_ERSTSZ0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ERSTS	R/W	0h	Event Ring Segment Table Size, RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.96 USB3P0SS_CTRL_XHCI_RESERVED0 Register

1 USB3P0SS_CTRL_XHCI_RESERVED0 Register (Offset = 202Ch) [reset = 0h]

Reserved

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Table 14-21142. Instance Table

Instance Name	Physical Address
USB0	**0F40 202Ch**

Figure 14-6986. USB3P0SS_CTRL_XHCI_RESERVED0 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1							
R							
0h							

Table 14-21144. USB3P0SS_CTRL_XHCI_RESERVED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.97 USB3P0SS_CTRL_XHCI_ERSTBA0_LO Register

1 USB3P0SS_CTRL_XHCI_ERSTBA0_LO Register (Offset = 2030h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21145. Instance Table

Instance Name	Physical Address
USB0	0F40 2030h

Figure 14-6987. USB3P0SS_CTRL_XHCI_ERSTBA0_LO Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_LO		RSVDP1					
R/W		R					
0h		0h					

Table 14-21147. USB3P0SS_CTRL_XHCI_ERSTBA0_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERSTBADDR_LO	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the low order bit [25:0] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n
5:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.98 USB3P0SS_CTRL_XHCI_ERSTBA0_HI Register

1 USB3P0SS_CTRL_XHCI_ERSTBA0_HI Register (Offset = 2034h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21148. Instance Table

Instance Name	Physical Address
USB0	**0F40 2034h**

Figure 14-6988. USB3P0SS_CTRL_XHCI_ERSTBA0_HI Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_HI							
R/W							
0h							

Table 14-21150. USB3P0SS_CTRL_XHCI_ERSTBA0_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERSTBADDR_HI	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the high order bits [57:26] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 in xHCI specificationfor more information. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.99 USB3P0SS_CTRL_XHCI_ERDP0_LO Register

1 USB3P0SS_CTRL_XHCI_ERDP0_LO Register (Offset = 2038h) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21151. Instance Table

Instance Name	Physical Address
USB0	**0F40 2038h**

Figure 14-6989. USB3P0SS_CTRL_XHCI_ERDP0_LO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ERDPTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ERDPTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ERDPTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ERDPTR</td><td>EHB</td><td colspan="3">DESI</td></tr>
<tr><td colspan="4">R/W</td><td>R/W1TC</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-21153. USB3P0SS_CTRL_XHCI_ERDP0_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERDPTR	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 28 low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	Event Handler Busy [EHB], RW1C. Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	Dequeue ERST Segment Index [DESI]. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.100 USB3P0SS_CTRL_XHCI_ERDP0_HI Register

1 USB3P0SS_CTRL_XHCI_ERDP0_HI Register (Offset = 203Ch) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21154. Instance Table

Instance Name	Physical Address
USB0	**0F40 203Ch**

Figure 14-6990. USB3P0SS_CTRL_XHCI_ERDP0_HI Name Register

31	30	29	28	27	26	25	24
ERDPTR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR_HI							
R/W							
0h							

Table 14-21156. USB3P0SS_CTRL_XHCI_ERDP0_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERDPTR_HI	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 32 high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.101 USB3P0SS_CTRL_XHCI_IMAN1 Register

1 USB3P0SS_CTRL_XHCI_IMAN1 Register (Offset = 2040h) [reset = 0h]

Interrupter Management Register (IMAN). The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

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Table 14-21157. Instance Table

Instance Name	Physical Address
USB0	**0F40 2040h**

Figure 14-6991. USB3P0SS_CTRL_XHCI_IMAN1 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-21159. USB3P0SS_CTRL_XHCI_IMAN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	IE	R/W	0h	Interrupt Enable [IE], RW. Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ['1'], the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is '0', then the Interrupter is prohibited from generating interrupts. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	Interrupt Pending [IP], RW1C. Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of the xHCI specification for the conditions that modify the state of this flag. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.102 USB3P0SS_CTRL_XHCI_IMOD1 Register

1 USB3P0SS_CTRL_XHCI_IMOD1 Register (Offset = 2044h) [reset = FA0h]

Interrupter Moderation Register (IMOD). The Interrupter Moderation Register controls the interrupt moderation feature of an Interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

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Table 14-21160. Instance Table

Instance Name	Physical Address
USB0	0F40 2044h

Figure 14-6992. USB3P0SS_CTRL_XHCI_IMOD1 Name Register

31	30	29	28	27	26	25	24
IMODC							
R/W							
0h							
23	22	21	20	19	18	17	16
IMODC							
R/W							
0h							
15	14	13	12	11	10	9	8
IMODI							
R/W							
FA0h							
7	6	5	4	3	2	1	0
IMODI							
R/W							
FA0h							

Table 14-21162. USB3P0SS_CTRL_XHCI_IMOD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC], RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is zero, the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI], RW. Default = 'hFA0' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of zero disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The IMODI field shall default to 'hFA0' [1 ms] upon initialization and reset. It may be loaded with an alternative value by software when the Interrupter is initialized. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.103 USB3P0SS_CTRL_XHCI_ERSTSZ1 Register

1 USB3P0SS_CTRL_XHCI_ERSTSZ1 Register (Offset = 2048h) [reset = 0h]

Event Ring Segment Table Size Register (ERSTSZ). The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment Table.

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Table 14-21163. Instance Table

Instance Name	Physical Address
USB0	0F40 2048h

Figure 14-6993. USB3P0SS_CTRL_XHCI_ERSTSZ1 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
ERSTS							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTS							
R/W							
0h							

Table 14-21165. USB3P0SS_CTRL_XHCI_ERSTSZ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ERSTS	R/W	0h	Event Ring Segment Table Size, RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.104 USB3P0SS_CTRL_XHCI_RESERVED1 Register

1 USB3P0SS_CTRL_XHCI_RESERVED1 Register (Offset = 204Ch) [reset = 0h]

Reserved

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Table 14-21166. Instance Table

Instance Name	Physical Address
USB0	**0F40 204Ch**

Figure 14-6994. USB3P0SS_CTRL_XHCI_RESERVED1 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1							
R							
0h							

Table 14-21168. USB3P0SS_CTRL_XHCI_RESERVED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.105 USB3P0SS_CTRL_XHCI_ERSTBA1_LO Register

1 USB3P0SS_CTRL_XHCI_ERSTBA1_LO Register (Offset = 2050h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21169. Instance Table

Instance Name	Physical Address
USB0	**0F40 2050h**

Figure 14-6995. USB3P0SS_CTRL_XHCI_ERSTBA1_LO Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_LO		RSVDP1					
R/W		R					
0h		0h					

Table 14-21171. USB3P0SS_CTRL_XHCI_ERSTBA1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERSTBADDR_LO	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the low order bit [25:0] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n
5:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.106 USB3P0SS_CTRL_XHCI_ERSTBA1_HI Register

1 USB3P0SS_CTRL_XHCI_ERSTBA1_HI Register (Offset = 2054h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21172. Instance Table

Instance Name	Physical Address
USB0	**0F40 2054h**

Figure 14-6996. USB3P0SS_CTRL_XHCI_ERSTBA1_HI Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_HI							
R/W							
0h							

Table 14-21174. USB3P0SS_CTRL_XHCI_ERSTBA1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERSTBADDR_HI	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the high order bits [57:26] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 in xHCI specificationfor more information. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.107 USB3P0SS_CTRL_XHCI_ERDP1_LO Register

1 USB3P0SS_CTRL_XHCI_ERDP1_LO Register (Offset = 2058h) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21175. Instance Table

Instance Name	Physical Address
USB0	**0F40 2058h**

Figure 14-6997. USB3P0SS_CTRL_XHCI_ERDP1_LO Name Register

31	30	29	28	27	26	25	24
ERDPTR							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR				EHB	DESI		
R/W				R/W1TC	R/W		
0h				0h	0h		

Table 14-21177. USB3P0SS_CTRL_XHCI_ERDP1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERDPTR	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 28 low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	Event Handler Busy [EHB], RW1C. Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	Dequeue ERST Segment Index [DESI]. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.108 USB3P0SS_CTRL_XHCI_ERDP1_HI Register

1 USB3P0SS_CTRL_XHCI_ERDP1_HI Register (Offset = 205Ch) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21178. Instance Table

Instance Name	Physical Address
USB0	**0F40 205Ch**

Figure 14-6998. USB3P0SS_CTRL_XHCI_ERDP1_HI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ERDPTR_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ERDPTR_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ERDPTR_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ERDPTR_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21180. USB3P0SS_CTRL_XHCI_ERDP1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERDPTR_HI	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 32 high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.109 USB3P0SS_CTRL_XHCI_IMAN2 Register

1 USB3P0SS_CTRL_XHCI_IMAN2 Register (Offset = 2060h) [reset = 0h]

Interrupter Management Register (IMAN). The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

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Table 14-21181. Instance Table

Instance Name	Physical Address
USB0	**0F40 2060h**

Figure 14-6999. USB3P0SS_CTRL_XHCI_IMAN2 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-21183. USB3P0SS_CTRL_XHCI_IMAN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	IE	R/W	0h	Interrupt Enable [IE], RW. Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ['1'], the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is '0', then the Interrupter is prohibited from generating interrupts. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	Interrupt Pending [IP], RW1C. Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of the xHCI specification for the conditions that modify the state of this flag. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.110 USB3P0SS_CTRL_XHCI_IMOD2 Register

1 USB3P0SS_CTRL_XHCI_IMOD2 Register (Offset = 2064h) [reset = FA0h]

Interrupter Moderation Register (IMOD). The Interrupter Moderation Register controls the interrupt moderation feature of an Interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

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Table 14-21184. Instance Table

Instance Name	Physical Address
USB0	0F40 2064h

Figure 14-7000. USB3P0SS_CTRL_XHCI_IMOD2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IMODC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IMODC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IMODI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FA0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IMODI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FA0h</td></tr>
</table>

Table 14-21186. USB3P0SS_CTRL_XHCI_IMOD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC], RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is zero, the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI], RW. Default = 'hFA0' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of zero disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The IMODI field shall default to 'hFA0' [1 ms] upon initialization and reset. It may be loaded with an alternative value by software when the Interrupter is initialized. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.111 USB3P0SS_CTRL_XHCI_ERSTSZ2 Register

1 USB3P0SS_CTRL_XHCI_ERSTSZ2 Register (Offset = 2068h) [reset = 0h]

Event Ring Segment Table Size Register (ERSTSZ). The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment Table.

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Table 14-21187. Instance Table

Instance Name	Physical Address
USB0	**0F40 2068h**

Figure 14-7001. USB3P0SS_CTRL_XHCI_ERSTSZ2 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
ERSTS							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTS							
R/W							
0h							

Table 14-21189. USB3P0SS_CTRL_XHCI_ERSTSZ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ERSTS	R/W	0h	Event Ring Segment Table Size, RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.112 USB3P0SS_CTRL_XHCI_RESERVED2 Register

1 USB3P0SS_CTRL_XHCI_RESERVED2 Register (Offset = 206Ch) [reset = 0h]

Reserved

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Table 14-21190. Instance Table

Instance Name	Physical Address
USB0	**0F40 206Ch**

Figure 14-7002. USB3P0SS_CTRL_XHCI_RESERVED2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21192. USB3P0SS_CTRL_XHCI_RESERVED2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.113 USB3P0SS_CTRL_XHCI_ERSTBA2_LO Register

1 USB3P0SS_CTRL_XHCI_ERSTBA2_LO Register (Offset = 2070h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21193. Instance Table

Instance Name	Physical Address
USB0	**0F40 2070h**

Figure 14-7003. USB3P0SS_CTRL_XHCI_ERSTBA2_LO Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_LO		RSVDP1					
R/W		R					
0h		0h					

Table 14-21195. USB3P0SS_CTRL_XHCI_ERSTBA2_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERSTBADDR_LO	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the low order bit [25:0] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n
5:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.114 USB3P0SS_CTRL_XHCI_ERSTBA2_HI Register

1 USB3P0SS_CTRL_XHCI_ERSTBA2_HI Register (Offset = 2074h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21196. Instance Table

Instance Name	Physical Address
USB0	**0F40 2074h**

Figure 14-7004. USB3P0SS_CTRL_XHCI_ERSTBA2_HI Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_HI							
R/W							
0h							

Table 14-21198. USB3P0SS_CTRL_XHCI_ERSTBA2_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERSTBADDR_HI	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the high order bits [57:26] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 in xHCI specificationfor more information. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.115 USB3P0SS_CTRL_XHCI_ERDP2_LO Register

1 USB3P0SS_CTRL_XHCI_ERDP2_LO Register (Offset = 2078h) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21199. Instance Table

Instance Name	Physical Address
USB0	0F40 2078h

Figure 14-7005. USB3P0SS_CTRL_XHCI_ERDP2_LO Name Register

31	30	29	28	27	26	25	24
ERDPTR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ERDPTR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERDPTR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERDPTR				EHB	DESI		
R/W				R/W1TC	R/W		
0h				0h	0h		

Table 14-21201. USB3P0SS_CTRL_XHCI_ERDP2_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERDPTR	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 28 low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	Event Handler Busy [EHB], RW1C. Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	Dequeue ERST Segment Index [DESI]. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.116 USB3P0SS_CTRL_XHCI_ERDP2_HI Register

1 USB3P0SS_CTRL_XHCI_ERDP2_HI Register (Offset = 207Ch) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21202. Instance Table

Instance Name	Physical Address
USB0	**0F40 207Ch**

Figure 14-7006. USB3P0SS_CTRL_XHCI_ERDP2_HI Name Register

31	30	29	28	27	26	25	24
ERDPTR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR_HI							
R/W							
0h							

Table 14-21204. USB3P0SS_CTRL_XHCI_ERDP2_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERDPTR_HI	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 32 high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.117 USB3P0SS_CTRL_XHCI_IMAN3 Register

1 USB3P0SS_CTRL_XHCI_IMAN3 Register (Offset = 2080h) [reset = 0h]

Interrupter Management Register (IMAN). The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

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Table 14-21205. Instance Table

Instance Name	Physical Address
USB0	0F40 2080h

Figure 14-7007. USB3P0SS_CTRL_XHCI_IMAN3 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-21207. USB3P0SS_CTRL_XHCI_IMAN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	IE	R/W	0h	Interrupt Enable [IE], RW. Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ['1'], the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is '0', then the Interrupter is prohibited from generating interrupts. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	Interrupt Pending [IP], RW1C. Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of the xHCI specification for the conditions that modify the state of this flag. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.118 USB3P0SS_CTRL_XHCI_IMOD3 Register

1 USB3P0SS_CTRL_XHCI_IMOD3 Register (Offset = 2084h) [reset = FA0h]

Interrupter Moderation Register (IMOD). The Interrupter Moderation Register controls the interrupt moderation feature of an Interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

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Table 14-21208. Instance Table

Instance Name	Physical Address
USB0	0F40 2084h

Figure 14-7008. USB3P0SS_CTRL_XHCI_IMOD3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IMODC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IMODC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IMODI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FA0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IMODI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FA0h</td></tr>
</table>

Table 14-21210. USB3P0SS_CTRL_XHCI_IMOD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC], RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is zero, the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI], RW. Default = 'hFA0' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of zero disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The IMODI field shall default to 'hFA0' [1 ms] upon initialization and reset. It may be loaded with an alternative value by software when the Interrupter is initialized. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.119 USB3P0SS_CTRL_XHCI_ERSTSZ3 Register

1 USB3P0SS_CTRL_XHCI_ERSTSZ3 Register (Offset = 2088h) [reset = 0h]

Event Ring Segment Table Size Register (ERSTSZ). The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment Table.

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Table 14-21211. Instance Table

Instance Name	Physical Address
USB0	**0F40 2088h**

Figure 14-7009. USB3P0SS_CTRL_XHCI_ERSTSZ3 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
ERSTS							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTS							
R/W							
0h							

Table 14-21213. USB3P0SS_CTRL_XHCI_ERSTSZ3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ERSTS	R/W	0h	Event Ring Segment Table Size, RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.120 USB3P0SS_CTRL_XHCI_RESERVED3 Register

1 USB3P0SS_CTRL_XHCI_RESERVED3 Register (Offset = 208Ch) [reset = 0h]

Reserved

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Table 14-21214. Instance Table

Instance Name	Physical Address
USB0	0F40 208Ch

Figure 14-7010. USB3P0SS_CTRL_XHCI_RESERVED3 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVDP1							
R							
0h							

Table 14-21216. USB3P0SS_CTRL_XHCI_RESERVED3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.121 USB3P0SS_CTRL_XHCI_ERSTBA3_LO Register

1 USB3P0SS_CTRL_XHCI_ERSTBA3_LO Register (Offset = 2090h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21217. Instance Table

Instance Name	Physical Address
USB0	**0F40 2090h**

Figure 14-7011. USB3P0SS_CTRL_XHCI_ERSTBA3_LO Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_LO		RSVDP1					
R/W		R					
0h		0h					

Table 14-21219. USB3P0SS_CTRL_XHCI_ERSTBA3_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERSTBADDR_LO	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the low order bit [25:0] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n
5:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.122 USB3P0SS_CTRL_XHCI_ERSTBA3_HI Register

1 USB3P0SS_CTRL_XHCI_ERSTBA3_HI Register (Offset = 2094h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21220. Instance Table

Instance Name	Physical Address
USB0	**0F40 2094h**

Figure 14-7012. USB3P0SS_CTRL_XHCI_ERSTBA3_HI Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_HI							
R/W							
0h							

Table 14-21222. USB3P0SS_CTRL_XHCI_ERSTBA3_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERSTBADDR_HI	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the high order bits [57:26] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 in xHCI specificationfor more information. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.123 USB3P0SS_CTRL_XHCI_ERDP3_LO Register

1 USB3P0SS_CTRL_XHCI_ERDP3_LO Register (Offset = 2098h) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21223. Instance Table

Instance Name	Physical Address
USB0	**0F40 2098h**

Figure 14-7013. USB3P0SS_CTRL_XHCI_ERDP3_LO Name Register

31	30	29	28	27	26	25	24
ERDPTR							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR				EHB	DESI		
R/W				R/W1TC	R/W		
0h				0h	0h		

Table 14-21225. USB3P0SS_CTRL_XHCI_ERDP3_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERDPTR	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 28 low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	Event Handler Busy [EHB], RW1C. Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	Dequeue ERST Segment Index [DESI]. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.124 USB3P0SS_CTRL_XHCI_ERDP3_HI Register

1 USB3P0SS_CTRL_XHCI_ERDP3_HI Register (Offset = 209Ch) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21226. Instance Table

Instance Name	Physical Address
USB0	0F40 209Ch

Figure 14-7014. USB3P0SS_CTRL_XHCI_ERDP3_HI Name Register

31	30	29	28	27	26	25	24
ERDPTR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR_HI							
R/W							
0h							

Table 14-21228. USB3P0SS_CTRL_XHCI_ERDP3_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERDPTR_HI	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 32 high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.125 USB3P0SS_CTRL_XHCI_IMAN4 Register

1 USB3P0SS_CTRL_XHCI_IMAN4 Register (Offset = 20A0h) [reset = 0h]

Interrupter Management Register (IMAN). The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

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Table 14-21229. Instance Table

Instance Name	Physical Address
USB0	**0F40 20A0h**

Figure 14-7015. USB3P0SS_CTRL_XHCI_IMAN4 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-21231. USB3P0SS_CTRL_XHCI_IMAN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	IE	R/W	0h	Interrupt Enable [IE], RW. Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ['1'], the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is '0', then the Interrupter is prohibited from generating interrupts. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	Interrupt Pending [IP], RW1C. Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of the xHCI specification for the conditions that modify the state of this flag. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.126 USB3P0SS_CTRL_XHCI_IMOD4 Register

1 USB3P0SS_CTRL_XHCI_IMOD4 Register (Offset = 20A4h) [reset = FA0h]

Interrupter Moderation Register (IMOD). The Interrupter Moderation Register controls the interrupt moderation feature of an Interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

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Table 14-21232. Instance Table

Instance Name	Physical Address
USB0	0F40 20A4h

Figure 14-7016. USB3P0SS_CTRL_XHCI_IMOD4 Name Register

31	30	29	28	27	26	25	24
IMODC							
R/W							
0h							
23	22	21	20	19	18	17	16
IMODC							
R/W							
0h							
15	14	13	12	11	10	9	8
IMODI							
R/W							
FA0h							
7	6	5	4	3	2	1	0
IMODI							
R/W							
FA0h							

Table 14-21234. USB3P0SS_CTRL_XHCI_IMOD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC], RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is zero, the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI], RW. Default = 'hFA0' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of zero disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The IMODI field shall default to 'hFA0' [1 ms] upon initialization and reset. It may be loaded with an alternative value by software when the Interrupter is initialized. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.127 USB3P0SS_CTRL_XHCI_ERSTSZ4 Register

1 USB3P0SS_CTRL_XHCI_ERSTSZ4 Register (Offset = 20A8h) [reset = 0h]

Event Ring Segment Table Size Register (ERSTSZ). The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment Table.

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Table 14-21235. Instance Table

Instance Name	Physical Address
USB0	**0F40 20A8h**

Figure 14-7017. USB3P0SS_CTRL_XHCI_ERSTSZ4 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
ERSTS							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTS							
R/W							
0h							

Table 14-21237. USB3P0SS_CTRL_XHCI_ERSTSZ4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ERSTS	R/W	0h	Event Ring Segment Table Size, RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.128 USB3P0SS_CTRL_XHCI_RESERVED4 Register

1 USB3P0SS_CTRL_XHCI_RESERVED4 Register (Offset = 20ACh) [reset = 0h]

Reserved

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Table 14-21238. Instance Table

Instance Name	**Physical Address**
USB0	**0F40 20ACh**

Figure 14-7018. USB3P0SS_CTRL_XHCI_RESERVED4 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1							
R							
0h							

Table 14-21240. USB3P0SS_CTRL_XHCI_RESERVED4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.129 USB3P0SS_CTRL_XHCI_ERSTBA4_LO Register

1 USB3P0SS_CTRL_XHCI_ERSTBA4_LO Register (Offset = 20B0h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21241. Instance Table

Instance Name	Physical Address
USB0	**0F40 20B0h**

Figure 14-7019. USB3P0SS_CTRL_XHCI_ERSTBA4_LO Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_LO		RSVDP1					
R/W		R					
0h		0h					

Table 14-21243. USB3P0SS_CTRL_XHCI_ERSTBA4_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERSTBADDR_LO	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the low order bit [25:0] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n
5:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.130 USB3P0SS_CTRL_XHCI_ERSTBA4_HI Register

1 USB3P0SS_CTRL_XHCI_ERSTBA4_HI Register (Offset = 20B4h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21244. Instance Table

Instance Name	Physical Address
USB0	**0F40 20B4h**

Figure 14-7020. USB3P0SS_CTRL_XHCI_ERSTBA4_HI Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_HI							
R/W							
0h							

Table 14-21246. USB3P0SS_CTRL_XHCI_ERSTBA4_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERSTBADDR_HI	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the high order bits [57:26] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 in xHCI specificationfor more information. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.131 USB3P0SS_CTRL_XHCI_ERDP4_LO Register

1 USB3P0SS_CTRL_XHCI_ERDP4_LO Register (Offset = 20B8h) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21247. Instance Table

Instance Name	Physical Address
USB0	**0F40 20B8h**

Figure 14-7021. USB3P0SS_CTRL_XHCI_ERDP4_LO Name Register

31	30	29	28	27	26	25	24
ERDPTR							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR				EHB	DESI		
R/W				R/W1TC	R/W		
0h				0h	0h		

Table 14-21249. USB3P0SS_CTRL_XHCI_ERDP4_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERDPTR	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 28 low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	Event Handler Busy [EHB], RW1C. Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	Dequeue ERST Segment Index [DESI]. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.132 USB3P0SS_CTRL_XHCI_ERDP4_HI Register

1 USB3P0SS_CTRL_XHCI_ERDP4_HI Register (Offset = 20BCh) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21250. Instance Table

Instance Name	Physical Address
USB0	0F40 20BCh

Figure 14-7022. USB3P0SS_CTRL_XHCI_ERDP4_HI Name Register

31	30	29	28	27	26	25	24
ERDPTR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR_HI							
R/W							
0h							

Table 14-21252. USB3P0SS_CTRL_XHCI_ERDP4_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERDPTR_HI	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 32 high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.133 USB3P0SS_CTRL_XHCI_IMAN5 Register

1 USB3P0SS_CTRL_XHCI_IMAN5 Register (Offset = 20C0h) [reset = 0h]

Interrupter Management Register (IMAN). The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

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Table 14-21253. Instance Table

Instance Name	Physical Address
USB0	**0F40 20C0h**

Figure 14-7023. USB3P0SS_CTRL_XHCI_IMAN5 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVDP1						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-21255. USB3P0SS_CTRL_XHCI_IMAN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	IE	R/W	0h	Interrupt Enable [IE], RW. Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ['1'], the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is '0', then the Interrupter is prohibited from generating interrupts. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	Interrupt Pending [IP], RW1C. Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of the xHCI specification for the conditions that modify the state of this flag. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.134 USB3P0SS_CTRL_XHCI_IMOD5 Register

1 USB3P0SS_CTRL_XHCI_IMOD5 Register (Offset = 20C4h) [reset = FA0h]

Interrupter Moderation Register (IMOD). The Interrupter Moderation Register controls the interrupt moderation feature of an Interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

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Table 14-21256. Instance Table

Instance Name	Physical Address
USB0	0F40 20C4h

Figure 14-7024. USB3P0SS_CTRL_XHCI_IMOD5 Name Register

31	30	29	28	27	26	25	24
IMODC							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IMODC							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IMODI							
R/W							
FA0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IMODI							
R/W							
FA0h							

Table 14-21258. USB3P0SS_CTRL_XHCI_IMOD5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC], RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is zero, the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI], RW. Default = 'hFA0' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of zero disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The IMODI field shall default to 'hFA0' [1 ms] upon initialization and reset. It may be loaded with an alternative value by software when the Interrupter is initialized. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.135 USB3P0SS_CTRL_XHCI_ERSTSZ5 Register

1 USB3P0SS_CTRL_XHCI_ERSTSZ5 Register (Offset = 20C8h) [reset = 0h]

Event Ring Segment Table Size Register (ERSTSZ). The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment Table.

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Table 14-21259. Instance Table

Instance Name	Physical Address
USB0	0F40 20C8h

Figure 14-7025. USB3P0SS_CTRL_XHCI_ERSTSZ5 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
ERSTS							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTS							
R/W							
0h							

Table 14-21261. USB3P0SS_CTRL_XHCI_ERSTSZ5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ERSTS	R/W	0h	Event Ring Segment Table Size, RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.136 USB3P0SS_CTRL_XHCI_RESERVED5 Register

1 USB3P0SS_CTRL_XHCI_RESERVED5 Register (Offset = 20CCh) [reset = 0h]

Reserved

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Table 14-21262. Instance Table

Instance Name	Physical Address
USB0	**0F40 20CCh**

Figure 14-7026. USB3P0SS_CTRL_XHCI_RESERVED5 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1							
R							
0h							

Table 14-21264. USB3P0SS_CTRL_XHCI_RESERVED5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.137 USB3P0SS_CTRL_XHCI_ERSTBA5_LO Register

1 USB3P0SS_CTRL_XHCI_ERSTBA5_LO Register (Offset = 20D0h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21265. Instance Table

Instance Name	Physical Address
USB0	**0F40 20D0h**

Figure 14-7027. USB3P0SS_CTRL_XHCI_ERSTBA5_LO Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_LO		RSVDP1					
R/W		R					
0h		0h					

Table 14-21267. USB3P0SS_CTRL_XHCI_ERSTBA5_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERSTBADDR_LO	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the low order bit [25:0] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n
5:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.138 USB3P0SS_CTRL_XHCI_ERSTBA5_HI Register

1 USB3P0SS_CTRL_XHCI_ERSTBA5_HI Register (Offset = 20D4h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21268. Instance Table

Instance Name	Physical Address
USB0	**0F40 20D4h**

Figure 14-7028. USB3P0SS_CTRL_XHCI_ERSTBA5_HI Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_HI							
R/W							
0h							

Table 14-21270. USB3P0SS_CTRL_XHCI_ERSTBA5_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERSTBADDR_HI	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the high order bits [57:26] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 in xHCI specificationfor more information. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.139 USB3P0SS_CTRL_XHCI_ERDP5_LO Register

1 USB3P0SS_CTRL_XHCI_ERDP5_LO Register (Offset = 20D8h) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21271. Instance Table

Instance Name	Physical Address
USB0	0F40 20D8h

Figure 14-7029. USB3P0SS_CTRL_XHCI_ERDP5_LO Name Register

31	30	29	28	27	26	25	24
ERDPTR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ERDPTR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERDPTR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERDPTR				EHB	DESI		
R/W				R/W1TC	R/W		
0h				0h	0h		

Table 14-21273. USB3P0SS_CTRL_XHCI_ERDP5_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERDPTR	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 28 low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	Event Handler Busy [EHB], RW1C. Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	Dequeue ERST Segment Index [DESI]. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.140 USB3P0SS_CTRL_XHCI_ERDP5_HI Register

1 USB3P0SS_CTRL_XHCI_ERDP5_HI Register (Offset = 20DCh) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21274. Instance Table

Instance Name	Physical Address
USB0	**0F40 20DCh**

Figure 14-7030. USB3P0SS_CTRL_XHCI_ERDP5_HI Name Register

31	30	29	28	27	26	25	24
ERDPTR_HI							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ERDPTR_HI							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERDPTR_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERDPTR_HI							
R/W							
0h							

Table 14-21276. USB3P0SS_CTRL_XHCI_ERDP5_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERDPTR_HI	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 32 high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.141 USB3P0SS_CTRL_XHCI_IMAN6 Register

1 USB3P0SS_CTRL_XHCI_IMAN6 Register (Offset = 20E0h) [reset = 0h]

Interrupter Management Register (IMAN). The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

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Table 14-21277. Instance Table

Instance Name	Physical Address
USB0	**0F40 20E0h**

Figure 14-7031. USB3P0SS_CTRL_XHCI_IMAN6 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVDP1						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-21279. USB3P0SS_CTRL_XHCI_IMAN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	IE	R/W	0h	Interrupt Enable [IE], RW. Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ['1'], the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is '0', then the Interrupter is prohibited from generating interrupts. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	Interrupt Pending [IP], RW1C. Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of the xHCI specification for the conditions that modify the state of this flag. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.142 USB3P0SS_CTRL_XHCI_IMOD6 Register

1 USB3P0SS_CTRL_XHCI_IMOD6 Register (Offset = 20E4h) [reset = FA0h]

Interrupter Moderation Register (IMOD). The Interrupter Moderation Register controls the interrupt moderation feature of an Interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

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Table 14-21280. Instance Table

Instance Name	Physical Address
USB0	0F40 20E4h

Figure 14-7032. USB3P0SS_CTRL_XHCI_IMOD6 Name Register

31	30	29	28	27	26	25	24
IMODC							
R/W							
0h							
23	22	21	20	19	18	17	16
IMODC							
R/W							
0h							
15	14	13	12	11	10	9	8
IMODI							
R/W							
FA0h							
7	6	5	4	3	2	1	0
IMODI							
R/W							
FA0h							

Table 14-21282. USB3P0SS_CTRL_XHCI_IMOD6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC], RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is zero, the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI], RW. Default = 'hFA0' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of zero disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The IMODI field shall default to 'hFA0' [1 ms] upon initialization and reset. It may be loaded with an alternative value by software when the Interrupter is initialized. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.143 USB3P0SS_CTRL_XHCI_ERSTSZ6 Register

1 USB3P0SS_CTRL_XHCI_ERSTSZ6 Register (Offset = 20E8h) [reset = 0h]

Event Ring Segment Table Size Register (ERSTSZ). The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment Table.

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Table 14-21283. Instance Table

Instance Name	Physical Address
USB0	**0F40 20E8h**

Figure 14-7033. USB3P0SS_CTRL_XHCI_ERSTSZ6 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
ERSTS							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTS							
R/W							
0h							

Table 14-21285. USB3P0SS_CTRL_XHCI_ERSTSZ6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ERSTS	R/W	0h	Event Ring Segment Table Size, RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.144 USB3P0SS_CTRL_XHCI_RESERVED6 Register

1 USB3P0SS_CTRL_XHCI_RESERVED6 Register (Offset = 20ECh) [reset = 0h]

Reserved

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Table 14-21286. Instance Table

Instance Name	Physical Address
USB0	**0F40 20ECh**

Figure 14-7034. USB3P0SS_CTRL_XHCI_RESERVED6 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1							
R							
0h							

Table 14-21288. USB3P0SS_CTRL_XHCI_RESERVED6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.145 USB3P0SS_CTRL_XHCI_ERSTBA6_LO Register

1 USB3P0SS_CTRL_XHCI_ERSTBA6_LO Register (Offset = 20F0h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21289. Instance Table

Instance Name	Physical Address
USB0	0F40 20F0h

Figure 14-7035. USB3P0SS_CTRL_XHCI_ERSTBA6_LO Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_LO		RSVDP1					
R/W		R					
0h		0h					

Table 14-21291. USB3P0SS_CTRL_XHCI_ERSTBA6_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERSTBADDR_LO	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the low order bit [25:0] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n
5:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.146 USB3P0SS_CTRL_XHCI_ERSTBA6_HI Register

1 USB3P0SS_CTRL_XHCI_ERSTBA6_HI Register (Offset = 20F4h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21292. Instance Table

Instance Name	Physical Address
USB0	0F40 20F4h

Figure 14-7036. USB3P0SS_CTRL_XHCI_ERSTBA6_HI Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERSTBADDR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERSTBADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERSTBADDR_HI							
R/W							
0h							

Table 14-21294. USB3P0SS_CTRL_XHCI_ERSTBA6_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERSTBADDR_HI	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the high order bits [57:26] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 in xHCI specificationfor more information. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.147 USB3P0SS_CTRL_XHCI_ERDP6_LO Register

1 USB3P0SS_CTRL_XHCI_ERDP6_LO Register (Offset = 20F8h) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21295. Instance Table

Instance Name	Physical Address
USB0	**0F40 20F8h**

Figure 14-7037. USB3P0SS_CTRL_XHCI_ERDP6_LO Name Register

31	30	29	28	27	26	25	24
ERDPTR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ERDPTR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERDPTR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERDPTR				EHB	DESI		
R/W				R/W1TC	R/W		
0h				0h	0h		

Table 14-21297. USB3P0SS_CTRL_XHCI_ERDP6_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERDPTR	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 28 low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	Event Handler Busy [EHB], RW1C. Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	Dequeue ERST Segment Index [DESI]. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.148 USB3P0SS_CTRL_XHCI_ERDP6_HI Register

1 USB3P0SS_CTRL_XHCI_ERDP6_HI Register (Offset = 20FCh) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21298. Instance Table

Instance Name	Physical Address
USB0	**0F40 20FCh**

Figure 14-7038. USB3P0SS_CTRL_XHCI_ERDP6_HI Name Register

31	30	29	28	27	26	25	24
ERDPTR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR_HI							
R/W							
0h							

Table 14-21300. USB3P0SS_CTRL_XHCI_ERDP6_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERDPTR_HI	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 32 high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.149 USB3P0SS_CTRL_XHCI_IMAN7 Register

1 USB3P0SS_CTRL_XHCI_IMAN7 Register (Offset = 2100h) [reset = 0h]

Interrupter Management Register (IMAN). The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

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Table 14-21301. Instance Table

Instance Name	Physical Address
USB0	**0F40 2100h**

Figure 14-7039. USB3P0SS_CTRL_XHCI_IMAN7 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1						IE	IP
R						R/W	R/W1TC
0h						0h	0h

Table 14-21303. USB3P0SS_CTRL_XHCI_IMAN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
1	IE	R/W	0h	Interrupt Enable [IE], RW. Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ['1'], the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is '0', then the Interrupter is prohibited from generating interrupts. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	Interrupt Pending [IP], RW1C. Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of the xHCI specification for the conditions that modify the state of this flag. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.150 USB3P0SS_CTRL_XHCI_IMOD7 Register

1 USB3P0SS_CTRL_XHCI_IMOD7 Register (Offset = 2104h) [reset = FA0h]

Interrupter Moderation Register (IMOD). The Interrupter Moderation Register controls the interrupt moderation feature of an Interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

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Table 14-21304. Instance Table

Instance Name	Physical Address
USB0	0F40 2104h

Figure 14-7040. USB3P0SS_CTRL_XHCI_IMOD7 Name Register

31	30	29	28	27	26	25	24
IMODC							
R/W							
0h							
23	22	21	20	19	18	17	16
IMODC							
R/W							
0h							
15	14	13	12	11	10	9	8
IMODI							
R/W							
FA0h							
7	6	5	4	3	2	1	0
IMODI							
R/W							
FA0h							

Table 14-21306. USB3P0SS_CTRL_XHCI_IMOD7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC], RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is zero, the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI], RW. Default = 'hFA0' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of zero disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The IMODI field shall default to 'hFA0' [1 ms] upon initialization and reset. It may be loaded with an alternative value by software when the Interrupter is initialized. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.151 USB3P0SS_CTRL_XHCI_ERSTSZ7 Register

1 USB3P0SS_CTRL_XHCI_ERSTSZ7 Register (Offset = 2108h) [reset = 0h]

Event Ring Segment Table Size Register (ERSTSZ). The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment Table.

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Table 14-21307. Instance Table

Instance Name	Physical Address
USB0	0F40 2108h

Figure 14-7041. USB3P0SS_CTRL_XHCI_ERSTSZ7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ERSTS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ERSTS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21309. USB3P0SS_CTRL_XHCI_ERSTSZ7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:0	ERSTS	R/W	0h	Event Ring Segment Table Size, RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.152 USB3P0SS_CTRL_XHCI_RESERVED7 Register

1 USB3P0SS_CTRL_XHCI_RESERVED7 Register (Offset = 210Ch) [reset = 0h]

Reserved

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Table 14-21310. Instance Table

Instance Name	Physical Address
USB0	**0F40 210Ch**

Figure 14-7042. USB3P0SS_CTRL_XHCI_RESERVED7 Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVDP1							
R							
0h							

Table 14-21312. USB3P0SS_CTRL_XHCI_RESERVED7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.153 USB3P0SS_CTRL_XHCI_ERSTBA7_LO Register

1 USB3P0SS_CTRL_XHCI_ERSTBA7_LO Register (Offset = 2110h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21313. Instance Table

Instance Name	Physical Address
USB0	**0F40 2110h**

Figure 14-7043. USB3P0SS_CTRL_XHCI_ERSTBA7_LO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ERSTBADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ERSTBADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ERSTBADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">ERSTBADDR_LO</td><td colspan="6">RSVDP1</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-21315. USB3P0SS_CTRL_XHCI_ERSTBA7_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERSTBADDR_LO	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the low order bit [25:0] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n
5:0	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.154 USB3P0SS_CTRL_XHCI_ERSTBA7_HI Register

1 USB3P0SS_CTRL_XHCI_ERSTBA7_HI Register (Offset = 2114h) [reset = 0h]

The Event Ring Segment Table Base Address Register identifies the start address of the Event Ring Segment Table.

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Table 14-21316. Instance Table

Instance Name	Physical Address
USB0	**0F40 2114h**

Figure 14-7044. USB3P0SS_CTRL_XHCI_ERSTBA7_HI Name Register

31	30	29	28	27	26	25	24
ERSTBADDR_HI							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ERSTBADDR_HI							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERSTBADDR_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERSTBADDR_HI							
R/W							
0h							

Table 14-21318. USB3P0SS_CTRL_XHCI_ERSTBA7_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERSTBADDR_HI	R/W	0h	Event Ring Segment Table Base Address Register, RW. Default = 0. This field defines the high order bits [57:26] of the start address of the Event Ring Segment Table [the address is 58 bits wide] . Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 in xHCI specificationfor more information. This field shall not be modified if HCHalted [HCH] = '0'. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.155 USB3P0SS_CTRL_XHCI_ERDP7_LO Register

1 USB3P0SS_CTRL_XHCI_ERDP7_LO Register (Offset = 2118h) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21319. Instance Table

Instance Name	Physical Address
USB0	0F40 2118h

Figure 14-7045. USB3P0SS_CTRL_XHCI_ERDP7_LO Name Register

31	30	29	28	27	26	25	24
ERDPTR							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDPTR							
R/W							
0h							
15	14	13	12	11	10	9	8
ERDPTR							
R/W							
0h							
7	6	5	4	3	2	1	0
ERDPTR				EHB	DESI		
R/W				R/W1TC	R/W		
0h				0h	0h		

Table 14-21321. USB3P0SS_CTRL_XHCI_ERDP7_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERDPTR	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 28 low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	Event Handler Busy [EHB], RW1C. Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of xHCI specification for more information Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	Dequeue ERST Segment Index [DESI]. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.156 USB3P0SS_CTRL_XHCI_ERDP7_HI Register

1 USB3P0SS_CTRL_XHCI_ERDP7_HI Register (Offset = 211Ch) [reset = 0h]

Event Ring Dequeue Pointer Register (ERDP). The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Event Ring.

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Table 14-21322. Instance Table

Instance Name	Physical Address
USB0	**0F40 211Ch**

Figure 14-7046. USB3P0SS_CTRL_XHCI_ERDP7_HI Name Register

31	30	29	28	27	26	25	24
ERDPTR_HI							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ERDPTR_HI							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERDPTR_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERDPTR_HI							
R/W							
0h							

Table 14-21324. USB3P0SS_CTRL_XHCI_ERDP7_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERDPTR_HI	R/W	0h	Event Ring Dequeue Pointer, RW. Default = 0. This field defines the 32 high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.157 USB3P0SS_CTRL_XHCI_DB0 Register

1 USB3P0SS_CTRL_XHCI_DB0 Register (Offset = 3000h) [reset = 0h]

Host Controller Doorbell. The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform. The number of Doorbell Registers implemented by a particular instantiation of a host controller is documented in the Number of Device Slots (MaxSlots) field of the HCSPARAMS1 register (section 5.3.3 of xHCI specification). These registers are pointed to by the Doorbell Offset Register (DBOFF) in the xHC Capability register space. The Doorbell Array base address shall be Dword aligned and is calculated by adding the value in the DBOFF register (section 5.3.7 of xHCI specification) to Base (the base address of the xHCI Capability register address space). Doorbell Register 0 is dedicated to the Host Controller.

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Table 14-21325. Instance Table

Instance Name	Physical Address
USB0	**0F40 3000h**

Figure 14-7047. USB3P0SS_CTRL_XHCI_DB0 Name Register

31	30	29	28	27	26	25	24
DB_STREAM_ID							
R/W							
0h							
23	22	21	20	19	18	17	16
DB_STREAM_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
RSVDZ1							
R							
0h							
7	6	5	4	3	2	1	0
DB_TARGET							
R/W							
0h							

Table 14-21327. USB3P0SS_CTRL_XHCI_DB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DB_STREAM_ID	R/W	0h	DB Stream ID, RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams [MaxPStreams > 0], then 0, 65535 [No Stream] and 65534 [Prime] are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams [MaxPStreams = 0] and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to zero for Host Controller Command Doorbells. This field returns zero when read. Reset Source: rst_mod_g_rst_n

Table 14-21327. USB3P0SS_CTRL_XHCI_DB0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	RSVDZ1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
7:0	DB_TARGET	R/W	0h	DB Target, RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Possible values [For this register, there is only one valid value for the DB Target field, 0 [Host Controller Command]. The remaining values [1-255] are reserved.]: 0: Command Doorbell 1:247 Reserved 248:255 Vendor Defined This field returns zero when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to zero. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.158 USB3P0SS_CTRL_XHCI_DB_j Register

1 USB3P0SS_CTRL_XHCI_DB_j Register (Offset = 3004h + formula) [reset = 0h]

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform. The number of Doorbell Registers implemented by a particular instantiation of a host controller is documented in the Number of Device Slots (MaxSlots) field of the HCSPARAMS1 register (section 5.3.3 of xHCI specification). These registers are pointed to by the Doorbell Offset Register (DBOFF) in the xHC Capability register space. The Doorbell Array base address shall be Dword aligned and is calculated by adding the value in the DBOFF register (section 5.3.7 of xHCI specification) to Base (the base address of the xHCI Capability register address space).

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Offset = (j * 4h); where j = 0 to 63d

Table 14-21328. Instance Table

Instance Name	**Physical Address**
USB0	**0F40 3004h + formula**

Figure 14-7048. USB3P0SS_CTRL_XHCI_DB_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DB_STREAM_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DB_STREAM_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVDZ1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DB_TARGET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21330. USB3P0SS_CTRL_XHCI_DB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DB_STREAM_ID	R/W	0h	DB Stream ID, RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams [MaxPStreams > 0], then 0, 65535 [No Stream] and 65534 [Prime] are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams [MaxPStreams = 0] and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to zero for Host Controller Command Doorbells. This field returns zero when read. Reset Source: rst_mod_g_rst_n

Table 14-21330. USB3P0SS_CTRL_XHCI_DB_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	RSVDZ1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
7:0	DB_TARGET	R/W	0h	DB Target, RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Possible values: 0: Reserved 1: Control EP 0 Enqueue Pointer Update 2: EP 1 OUT Enqueue Pointer Update 3: EP 1 IN Enqueue Pointer Update 4: EP 2 OUT Enqueue Pointer Update 5: EP 2 IN Enqueue Pointer Update ... 30: EP 15 OUT Enqueue Pointer Update 31: EP 15 IN Enqueue Pointer Update 32:247: Reserved 248:255: Vendor Defined This field returns zero when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to zero. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.159 USB3P0SS_CTRL_XHCI_XECP_PORT_CAP_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_PORT_CAP_REG Register (Offset = 8000h) [reset = 10102C3h]

Extended capability for USB 3.0 Port. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be modified by software. It is described only for informative purposes.

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Table 14-21331. Instance Table

Instance Name	Physical Address
USB0	**0F40 8000h**

Figure 14-7049. USB3P0SS_CTRL_XHCI_XECP_PORT_CAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED1						LPM_2_STB_SWITCH_EN	LPM_2_STB_SWITCH_CAPABLE
R						R/W	R
0h						0h	1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XHCI_PORT_CAP_REV							
R							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XHCI_PORT_CAPABILITY_DW							
R							
2h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XHCI_PORT_CAP_ID							
R							
C3h							

Table 14-21333. USB3P0SS_CTRL_XHCI_XECP_PORT_CAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED1	R	0h	Reserved, RO
25	LPM_2_STB_SWITCH_EN	R/W	0h	Enable switching to stb_clk. Reset Source: rst_mod_g_rst_n
24	LPM_2_STB_SWITCH_CAPABLE	R	1h	xHC is capable of switching to stb_clk. Reset Source: rst_mod_g_rst_n
23:16	XHCI_PORT_CAP_REV	R	1h	XHCI_PORT_CAP_REV : revision of the Port Capability structure . Reset Source: rst_mod_g_rst_n
15:8	XHCI_PORT_CAPABILITY_DW	R	2h	XHCI_PORT_CAPABILITY_DW. Next Item Pointer. This field provides an offset pointing to the location of next item in the functions capability list. Reset Source: rst_mod_g_rst_n
7:0	XHCI_PORT_CAP_ID	R	C3h	XHCI_PORT_CAP_ID. Port capability ID. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.160 USB3P0SS_CTRL_XHCI_XECP_PORT_1_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_PORT_1_REG Register (Offset = 8004h) [reset = 7D40h]

Extended capability for USB 3.0 Port. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21334. Instance Table

Instance Name	Physical Address
USB0	**0F40 8004h**

Figure 14-7050. USB3P0SS_CTRL_XHCI_XECP_PORT_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
U1_LFPS_TIME_WR_STROBE	U1_LFPS_MINGEN_TIME						
R/W	R/W						
0h	7Dh						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED5	CPOLLINGTIMEOUT_EN	TTIME_FOR_RESET_EN	SKP_OS_FIX	U3_SPUR_LFPS_FIX	TERM_DEB_MAX		TRAINING_FAIL
R	R/W	R/W	R/W	R/W	R/W		R/W1TC
0h	1h	0h	0h	0h	0h		0h

Table 14-21336. USB3P0SS_CTRL_XHCI_XECP_PORT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, RO
15	U1_LFPS_TIME_WR_STROBE	R/W	0h	Minimum U1 LFPS generation time write stobe. Returns '0' when read. Reset Source: rst_mod_g_rst_n
14:8	U1_LFPS_MINGEN_TIME	R/W	7Dh	Minimum U1 LFPS generation time. Written only if U1_LFPS_TIME_WR_STROBE is 1. Reset Source: rst_mod_g_rst_n
7	RESERVED5	R	0h	Reserved, RO
6	CPOLLINGTIMEOUT_EN	R/W	1h	Enable cPollingTimeout Reset Source: rst_mod_g_rst_n
5	TTIME_FOR_RESET_EN	R/W	0h	Enable tTimeForResetError timer Reset Source: rst_mod_g_rst_n
4	SKP_OS_FIX	R/W	0h	Change counting number of symbols for SKP OS insertion [only for the 1st SKP OS] Reset Source: rst_mod_g_rst_n

Table 14-21336. USB3P0SS_CTRL_XHCI_XECP_PORT_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	U3_SPUR_LFPS_FIX	R/W	0h	Enable filtering out spurious LFPS when entering U3 state Reset Source: rst_mod_g_rst_n
2:1	TERM_DEB_MAX	R/W	0h	Number of the consecutive lack of Far-end Rx Termination detected that causes transition from SS.Inactive to RxDetect state Reset Source: rst_mod_g_rst_n
0	TRAINING_FAIL	R/W1TC	0h	When reading: Link Polling training error flag status, When writing '1': clear the Link Polling training error flag, When writing '0': no effect Reset Source: rst_mod_g_rst_n

14.9.2.3.2.161 USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CAP Register

1 USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CAP Register (Offset = 8008h) [reset = 3C4h]

xHCI Debug Bus Capability. This is a vendor defined capability. Please refer to Integration Guide for further details of debug bus usage.

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Table 14-21337. Instance Table

Instance Name	Physical Address
USB0	**0F40 8008h**

Figure 14-7051. USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CAP Name Register

31	30	29	28	27	26	25	24
CPU_DEBUG_EN	RSVDP1						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XHCI_DEBUG_BUS_DW							
R							
3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XHCI_DEBUG_BUS_CAP_ID							
R							
C4h							

Table 14-21339. USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU_DEBUG_EN	R/W	0h	Debug Bus Enable, RW. When 0, allows the xhci_debug_sel primary input to control selection of Debug Bus sources. When 1, allows the cpu_debug_bus_sel field in the XECP_CDNS_DEBUG_BUS_CTRL register to control selection of Debug Bus sources. Default value after reset is '0'. Reset Source: rst_mod_g_rst_n
30:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:8	XHCI_DEBUG_BUS_DW	R	3h	Next Capability Pointer, RO. This field indicates the location of the next capability with respect to the effective address of this capability. Reset Source: rst_mod_g_rst_n
7:0	XHCI_DEBUG_BUS_CAP_ID	R	C4h	Capability ID, RO. This field identifies the extended capability. For xHCI Debug Bus its' value is 196. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.162 USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CTRL Register

1 USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CTRL Register (Offset = 800Ch) [reset = 0h]

xHCI Debug Bus Control. This is a vendor defined capability. Please refer to Integration Guide for further details of debug bus usage.

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Table 14-21340. Instance Table

Instance Name	Physical Address
USB0	**0F40 800Ch**

Figure 14-7052. USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RSVDP1</td><td colspan="5">CPU_DEBUG_BUS_SEL</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-21342. USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4:0	CPU_DEBUG_BUS_SEL	R/W	0h	Debug Bus Select, RW. Value of this field determines a source of Debug Bus. Default value after reset is 0. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.163 USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_STATUS Register

1 USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_STATUS Register (Offset = 8010h) [reset = 0h]

xHCI Debug Bus Status. This is a vendor defined capability. Please refer to Integration Guide for further details of debug bus usage.

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Table 14-21343. Instance Table

Instance Name	Physical Address
USB0	**0F40 8010h**

Figure 14-7053. USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_STATUS Name Register

31	30	29	28	27	26	25	24
XHCI_DEBUG_BUS							
R							
0h							
23	22	21	20	19	18	17	16
XHCI_DEBUG_BUS							
R							
0h							
15	14	13	12	11	10	9	8
XHCI_DEBUG_BUS							
R							
0h							
7	6	5	4	3	2	1	0
XHCI_DEBUG_BUS							
R							
0h							

Table 14-21345. USB3P0SS_CTRL_XHCI_XECP_CDNS_DEBUG_BUS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XHCI_DEBUG_BUS	R	0h	Debug Bus, RO. Debug Bus current value. Note for multi-bit probes, this register is only suitable for analysing a static value due to simplified clock domain synchronisation Reset Source: rst_mod_g_rst_n

14.9.2.3.2.164 USB3P0SS_CTRL_XHCI_XECP_PM_CAP Register

1 USB3P0SS_CTRL_XHCI_XECP_PM_CAP Register (Offset = 8014h) [reset = FFCB0203h]

Extended Power Management capability register. Defined in section 7.3 of xHCI specification. Reuses power management structures defined in PCI bus Power Management specification. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21346. Instance Table

Instance Name	Physical Address
USB0	**0F40 8014h**

Figure 14-7054. USB3P0SS_CTRL_XHCI_XECP_PM_CAP Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">PME_SUPPORT</td><td>D2_SUPPORT</td><td>D1_SUPPORT</td><td>AUX_CURRENT</td></tr>
<tr><td colspan="5">R</td><td>R</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="5">1Fh</td><td>1h</td><td>1h</td><td>7h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">AUX_CURRENT</td><td>DSI</td><td>RESERVED</td><td>PME_CLOCK</td><td colspan="3">VERSION</td></tr>
<tr><td colspan="2">R/W</td><td>R</td><td>R</td><td>R</td><td colspan="3">R</td></tr>
<tr><td colspan="2">7h</td><td>0h</td><td>0h</td><td>1h</td><td colspan="3">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">XHCI_PM_CAPABILITY_DW</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">XHCI_PM_CAP_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
</table>

Table 14-21348. USB3P0SS_CTRL_XHCI_XECP_PM_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	PME_SUPPORT	R	1Fh	Power Management Capabilities: PME_Support. Default = device specific. This 5-bit field indicates the power states in which the function may assert PME#. A value of '0' for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. Encodings: Bit 0 set: X XXX1b - PME# can be asserted from D0, Bit 1 set: X XX1Xb - PME# can be asserted from D1, Bit 2 set: X X1XXb - PME# can be asserted from D2, Bit 3 set: X 1XXXb - PME# can be asserted from D3hot, Bit 4 set: 1 XXXXb - PME# can be asserted from D3cold Reset Source: rst_mod_g_rst_n
26	D2_SUPPORT	R	1h	Power Management Capabilities: D2_Support. Default = device specific. If this bit is a '1', this function supports the D2 Power Management State. Functions that do not support D2 must always return a value of '0' for this bit. Reset Source: rst_mod_g_rst_n

Table 14-21348. USB3P0SS_CTRL_XHCI_XECP_PM_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	D1_SUPPORT	R	1h	Power Management Capabilities: D1_Support. Default = device specific. If this bit is a '1', this function supports the D1 Power Management State. Functions that do not support D1 must always return a value of '0' for this bit. Reset Source: rst_mod_g_rst_n
24:22	AUX_CURRENT	R/W	7h	Power Management Capabilities: Aux_Current. Default = device specific. This 3 bit field reports the 3.3Vaux auxiliary current requirements for the PCI function. If the Data Register field of XECP_PM_PMCSR has been implemented by this function: - reads of this field must return a value of '000', - the Data Register takes precedence over this field for 3.3Vaux current requirement reporting. If PME# generation from D3cold is not supported by the Function [XECP_PM_CAP[15]='0'], this field must return a value of '000' when read. For functions that support PME# from D3cold, and do not implement the Data Register, the following bit encoding for maximum current required apply : '111': 375 mA, '110': 320 mA, '101': 270 mA, '100': 220 mA, '011': 160 mA, '010': 100 mA, '001': 55 mA, '000': 0 [self powered]. Reset Source: rst_mod_g_rst_n
21	DSI	R	0h	Power Management Capabilities: DSI. Default = device specific. The Device Specific Initialization bit indicates whether special initialization of this function is required [beyond the standard PCI configuration header] before the generic class device driver is able to use it. Note that this bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, they use the drivers capabilities to determine this. A '1' indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. For more information refer to Section 8.3. of PCI bus Power Management specification. Reset Source: rst_mod_g_rst_n
20	RESERVED	R	0h	reserved
19	PME_CLOCK	R	1h	Power Management Capabilities: PME Clock. Default = '0'. When this bit is a '1', it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a '0', it indicates that no PCI clock is required for the function to generate PME#. Functions that do not support PME# generation in any state must return '0' for this field. Reset Source: rst_mod_g_rst_n
18:16	VERSION	R	3h	Power Management Capabilities: Version. Default = '011'. A value of '011' indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification. Reset Source: rst_mod_g_rst_n
15:8	XHCI_PM_CAPABILITY_DW	R	2h	XHCI_PM_CAPABILITY_DW. Next Item Pointer. This field provides an offset pointing to the location of next item in the functions capability list. Reset Source: rst_mod_g_rst_n

Table 14-21348. USB3P0SS_CTRL_XHCI_XECP_PM_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	XHCI_PM_CAP_ID	R	3h	XHCI_PM_CAP_ID. Power Management capability ID. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.165 USB3P0SS_CTRL_XHCI_XECP_PM_PMCSR Register

1 USB3P0SS_CTRL_XHCI_XECP_PM_PMCSR Register (Offset = 8018h) [reset = 0h]

Extended Power Management Control/Status register. Defined in section 7.3 of xHCI specification. Reuses power management structures defined in PCI bus Power Management specification. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21349. Instance Table

Instance Name	Physical Address
USB0	**0F40 8018h**

Figure 14-7055. USB3P0SS_CTRL_XHCI_XECP_PM_PMCSR Name Register

31	30	29	28	27	26	25	24
DATA_REGISTER							
R							
0h							

23	22	21	20	19	18	17	16
BPCC_EN	B2_B3	RESERVED3					
R	R	R					
0h	0h	0h					

15	14	13	12	11	10	9	8
PME_STATUS	DATA_SCALE		DATA_SELECT				PME_EN
R/W1TC	R		R/W				R/W
0h	0h		0h				0h

7	6	5	4	3	2	1	0
RESERVED2				NO_SOFT_RESET	RESERVED1	POWERSTATE	
R				R	R	R/W	
0h				0h	0h	0h	

Table 14-21351. USB3P0SS_CTRL_XHCI_XECP_PM_PMCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DATA_REGISTER	R	0h	Data register. This register is used to report the state dependent data requested by the Data_Select field of XECP_PM_PMCSR register. The value of Data register is scaled by the value reported by the Data_Scale field of XECP_PM_PMCSR register. Reset Source: rst_mod_g_rst_n
23	BPCC_EN	R	0h	PMCSR Bridge Support Extensions: BPCC_En [Bus Power/Clock Control Enable]. External strap or internally hardwired. A '1' indicates that the bus power/clock control mechanism as defined in Section 4.7.1 PCI bus Power Management specification is enabled. A '0' indicates that the bus power/clock control policies defined in Section 4.7.1 PCI bus Power Management specification have been disabled. When the Bus Power/Clock Control mechanism is disabled, the bridges Power Management Control/Status Register PowerState field cannot be used by the system software to control the power or clock of the bridges secondary bus. Reset Source: rst_mod_g_rst_n

Table 14-21351. USB3P0SS_CTRL_XHCI_XECP_PM_PMCSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	B2_B3	R	0h	PMCSR Bridge Support Extensions: B2_B3# [B2/B3 support for D3hot]. External strap or internally hardwired. The state of this bit determines the action that is to occur as a direct result of programming the function to D3hot. A '1' indicates that when the bridge function is programmed to D3hot, its secondary buss PCI clock will be stopped [B2]. A '0' indicates that when the bridge function is programmed to D3hot, its secondary bus will have its power removed [B3]. This bit is only meaningful if bit BPCC_En of XECP_PM_PMCSR register is a '1'. Refer to Section 4.7.1 of PCI bus Power Management specification for details. Reset Source: rst_mod_g_rst_n
21:16	RESERVED3	R	0h	PMCSR Bridge Support Extensions: reserved
15	PME_STATUS	R/W1TC	0h	Power Management Control/Status Register: PME_Status. This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing a '1' to this bit will clear it and cause the function to stop asserting a PME# [if enabled]. Writing a '0' has no effect. This bit defaults to '0' if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded. Reset Source: rst_mod_g_rst_n
14:13	DATA_SCALE	R	0h	Power Management Control/Status Register: Data_Scale. Default = device specific. This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register field of XECP_PM_PMCSR register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field of this register. This field is a required component of the Data register and must be implemented if the Data register is implemented. If the Data register has not been implemented, this field must return zero when read. Refer to Section 3.2.6 of PCI bus Power Management specification for more details. Reset Source: rst_mod_g_rst_n
12:9	DATA_SELECT	R/W	0h	Power Management Control/Status Register: Data_Select. Default = zero. This 4-bit field is used to select, which data is to be reported through the Data register and Data_Scale fields of XECP_PM_PMCSR register. This field is a required component of the Data register and must be implemented if the Data register is implemented. If the Data register field of XECP_PM_PMCSR is not implemented, this field should be read only and return zero when read. Refer to Section 3.2.6 of PCI bus Power Management for more details. Reset Source: rst_mod_g_rst_n

Table 14-21351. USB3P0SS_CTRL_XHCI_XECP_PM_PMCSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	PME_EN	R/W	0h	Power Management Control/Status Register: PME_En. A '1' in this field enables the function to assert PME#. When '0', PME# assertion is disabled. This bit defaults to '0' if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Functions that do not support PME# generation from any D-state [i.e., XECP_PM_CAP[15:11] = '00000'], may hardwire this bit to be read-only always returning a '0' when read by system software. Reset Source: rst_mod_g_rst_n
7:4	RESERVED2	R	0h	Power Management Control/Status Register: reserved
3	NO_SOFT_RESET	R	0h	Power Management Control/Status Register: No_Soft_Reset. Default = device specific. When set to '1', this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When cleared to '0', devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Reset Source: rst_mod_g_rst_n
2	RESERVED1	R	0h	Power Management Control/Status Register: reserved
1:0	POWERSTATE	R/W	0h	Power Management Control/Status Register: PowerState. Default = zero. This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. Possible values: '00': D0, '01': D1, '10': D2, '11': D3hot. If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus. however, the data is discarded and no state change occurs. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.166 USB3P0SS_CTRL_XHCI_XECP_MSI_CAP Register

1 USB3P0SS_CTRL_XHCI_XECP_MSI_CAP Register (Offset = 801Ch) [reset = 860405h]

Message Signaled Interrupts (MSI) configuration register. This register may be read at any time, including whilst the CNR field in the USBSTS register is high. It can be written only when controller is stopped (bit HCH of USBSTS register is '0').

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Table 14-21352. Instance Table

Instance Name	Physical Address
USB0	**0F40 801Ch**

Figure 14-7056. USB3P0SS_CTRL_XHCI_XECP_MSI_CAP Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>PER_VECTOR_MASKING</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>AC64</td><td colspan="3">MSI_MME</td><td colspan="3">MSI_MMC</td><td>MSI_EN</td></tr>
<tr><td>R</td><td colspan="3">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td>1h</td><td colspan="3">0h</td><td colspan="3">3h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">XECP_MSI_CAP_OFFSET</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MSI_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5h</td></tr>
</table>

Table 14-21354. USB3P0SS_CTRL_XHCI_XECP_MSI_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	R	0h	MSI Message Control: Reserved. Always returns 0 on a read and a write operation has no effect.
24	PER_VECTOR_MASKING	R	0h	MSI Message Control: Per-vector masking capable. If '1', the function supports MSI per-vector masking. If '0', the function does not support MSI per-vector masking. This bit is read only. Not Supported in this configuration Reset Source: rst_mod_g_rst_n
23	AC64	R	1h	MSI Message Control: 64 bit address capable. If '1', the function is capable of generating sending a 64-bit message address. If '0', the function is not capable of generating sending a 64-bit message address. This bit is read only. Reset Source: rst_mod_g_rst_n

Table 14-21354. USB3P0SS_CTRL_XHCI_XECP_MSI_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:20	MSI_MME	R/W	0h	MSI Message Control: Multiple Message Enable. Software writes to this field to indicate the number of allocated vectors [equal to or less than the number of requested vectors]. The number of allocated vectors is aligned to a power of two. If a function requests four vectors [indicated by a Multiple Message Capable encoding of 010], system software can allocate either four, two, or one vector by writing a '010', '001', or '000' to this field, respectively. When MSI is enabled, a function will be allocated at least one vector. The encoding is defined as: '000': 1, '001': 2, '010': 4, '011': 8, '100': 16, '101': 32, '110': Reserved, '111': Reserved. This fields state after reset is '000'. Reset Source: rst_mod_g_rst_n
19:17	MSI_MMC	R	3h	MSI Message Control: Multiple Message Capable. System software reads this field to determine the number of requested vectors. The number of requested vectors must be aligned to a power of two [if a function requires three vectors, it requests four by initializing this field to '010']. The encoding is defined as: '000': 1, '001': 2, '010': 4, '011': 8, '100': 16, '101': 32, '110': Reserved, '111': Reserved. This field is read only. Reset Source: rst_mod_g_rst_n
16	MSI_EN	R/W	0h	MSI Message Control: MSI enable. System configuration software sets this bit to enable MSI. A device driver is prohibited from writing this bit to mask a functions service request. If '0', the function is prohibited from using MSI to request service. This bits state after reset is '0' [MSI is disabled]. Reset Source: rst_mod_g_rst_n
15:8	XECP_MSI_CAP_OFFSET	R	4h	Pointer to the next item in the capabilities list. A non-zero value in this field indicates a relative offset, in 32-bit words, from this 32-bit word to the beginning of the next extended capability. Reset Source: rst_mod_g_rst_n
7:0	MSI_ID	R	5h	Capability ID for Message Signaled Interrupts. The value of 05h in this field identifies the function as being MSI capable. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.167 USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_L Register

1 USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_L Register (Offset = 8020h) [reset = 0h]

Message Lower Address for MSI. If the Message Enable bit of MSI Message Control (bit 16 of the XCEP_MSI_CAP register) is set, the contents of this register specify the DWORD-aligned address (bits [31:02]) for the MSI memory write transaction. bits [1:0] are driven to zero during the address phase. This register may be read from at any time, including whilst the CNR field in the USBSTS register is high. It can be written only when controller is stopped (bit HCH of USBSTS register is '0').

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Table 14-21355. Instance Table

Instance Name	Physical Address
USB0	0F40 8020h

Figure 14-7057. USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_L Name Register

31	30	29	28	27	26	25	24
MSI_ADDR_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
MSI_ADDR_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
MSI_ADDR_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
MSI_ADDR_LOW						RESERVED	
R/W						R	
0h						0h	

Table 14-21357. USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	MSI_ADDR_LOW	R/W	0h	Message Lower Address for MSI. System-specified message address. If the Message Enable bit of MSI Message Control [bit 16 of the XCEP_MSI_CAP register] is set, the contents of this register specify the DWORD-aligned address for the MSI memory write transaction. Note: This field should not be written unless the Message Enable bit of MSI Message Control [bit 16 of the XCEP_MSI_CAP register] is cleared. This field is read/write. Reset Source: rst_mod_g_rst_n
1:0	RESERVED	R	0h	Reserved. Always returns zero on read. Write operations have no effect. Those bits are driven to zero during the address phase.

14.9.2.3.2.168 USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_H Register

1 USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_H Register (Offset = 8024h) [reset = 0h]

Message Upper Address for MSI. System-specified message upper address. This register is optional and is implemented only if the function supports a 64-bit message address (AC64 bit of MSI Message Control, see XCEP_MSI_CAP register). If the Message Enable bit of MSI Message Control (bit 16 of the XCEP_MSI_CAP register), the contents of this register (if nonzero) specify the upper 32-bits of a 64-bit message address (bits [63:32]). If the contents of this register are zero, the function uses the 32 bit address specified by the message address register. It can be written only when controller is stopped (bit HCH of USBSTS register is '0').

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Table 14-21358. Instance Table

Instance Name	Physical Address
USB0	**0F40 8024h**

Figure 14-7058. USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_H Name Register

31	30	29	28	27	26	25	24
MSI_ADDR_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
MSI_ADDR_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
MSI_ADDR_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
MSI_ADDR_HI							
R/W							
0h							

Table 14-21360. USB3P0SS_CTRL_XHCI_XECP_MSI_ADDR_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSI_ADDR_HI	R/W	0h	Message Upper Address for MSI. System-specified message upper address. Note: This field should not be written unless the Message Enable bit of MSI Message Control [bit 16 of the XCEP_MSI_CAP register] is cleared. This field is read/write. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.169 USB3P0SS_CTRL_XHCI_XECP_MSI_DATA Register

1 USB3P0SS_CTRL_XHCI_XECP_MSI_DATA Register (Offset = 8028h) [reset = 0h]

Message data for MSI. This register may be read from to at any time, including whilst the CNR field in the USBSTS register is high. It can be written only when controller is stopped (bit HCH of USBSTS register is '0').

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Table 14-21361. Instance Table

Instance Name	Physical Address
USB0	**0F40 8028h**

Figure 14-7059. USB3P0SS_CTRL_XHCI_XECP_MSI_DATA Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
MSI_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
MSI_DATA							
R/W							
0h							

Table 14-21363. USB3P0SS_CTRL_XHCI_XECP_MSI_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVD	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21363. USB3P0SS_CTRL_XHCI_XECP_MSI_DATA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	MSI_DATA	R/W	0h	System-specified message data. If the Message Enable bit of MSI Message Control [bit 16 of the XCEP_MSI_CAP register] is set, the message data is driven onto the lower word [bits [15:0]] of the memory write transactions data phase. Bits [31:16] are driven to zero during the memory write transactions data phase. C/BE[3::0]# are asserted during the data phase of the memory write transaction. The Multiple Message Enable field of MSI Message Control [see MSI_MME field of XCEP_MSI_CAP register] defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of '010' indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 [a function modifies the lower message data bits to generate the allocated number of vectors]. If the Multiple Message Enable field is '000', the function is not permitted to modify the message data. Note: This field should not be written unless the Message Enable bit of MSI Message Control [bit 16 of the XCEP_MSI_CAP register] is cleared. This field is read/write. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.170 USB3P0SS_CTRL_XHCI_XECP_AXI_CAP Register

1 USB3P0SS_CTRL_XHCI_XECP_AXI_CAP Register (Offset = 802Ch) [reset = 434105C2h]

AXI Initiator Wrapper Extended Capability. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability.

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Table 14-21364. Instance Table

Instance Name	Physical Address
USB0	0F40 802Ch

Figure 14-7060. USB3P0SS_CTRL_XHCI_XECP_AXI_CAP Name Register

31	30	29	28	27	26	25	24
AXI_HALT	AXI_IDLE	AXI_ERROR	RSVDP2		AXI_DATA_BUS_SIZE		
R/W	R	R/W1TC	R		R		
0h	1h	0h	0h		3h		
23	22	21	20	19	18	17	16
AXI_DISABLE_OOO	AXI_MASTER_WRAPPER_SPLIT_BYTE_BURSTS	RSVDP1					AXI_ADDRESS_WIDTH_64
R	R	R					R
0h	1h	0h					1h
15	14	13	12	11	10	9	8
XECP_AXI_CAP_OFFSET							
R							
5h							
7	6	5	4	3	2	1	0
AXI_CAP_ID							
R							
C2h							

Table 14-21366. USB3P0SS_CTRL_XHCI_XECP_AXI_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AXI_HALT	R/W	0h	AXI HALT, RW. The AXI Master wrapper's control bit. When set, the AXI Master wrapper will complete current CORE REQ [or IRQ] and stop acknowledging next ones. If the xHC is stopped the AXI Master wrapper is halted automatically. If the xHC is started the AXI Master wrapper is resumed automatically. Software should set this bit to stop the AXI Master issuing new AXI transactions. It may then use the IDLE bit to determine when all previous transactions were completed. Note: The AXI Master wrapper will execute halted only if xHC stopped its internal operation. Reset Source: rst_mod_g_rst_n
30	AXI_IDLE	R	1h	AXI IDLE, RO. Information about the AXI Master wrapper state: '0': no pending action required by the AXI Master wrapper, '1': the AXI Master wrapper has outstanding transactions. Note: HCH halted bit will not be asserted if the AXI Master wrapper is not idle. Reset Source: rst_mod_g_rst_n

Table 14-21366. USB3P0SS_CTRL_XHCI_XECP_AXI_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	AXI_ERROR	R/W1TC	0h	AXI ERROR, RW1C. Provides an information about AXI ERROR response on B or R channel. This flag is cleared by writing '1' to it. Once set it is held until cleared. The condition setting this register will also assert HSE. This flag may be read by software while handling HSE assertion to determine if the case was AXI ERROR reponse. Reset Source: rst_mod_g_rst_n
28:27	RSVDP2	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
26:24	AXI_DATA_BUS_SIZE	R	3h	AXI_DATA_WORD_SIZE, RO. AXI data buses size capability. It uses AXI AxSIZE Encoding. Values of 64-bit ['011'] or 128-bit ['100'] are supported through compile time configuration. Reset Source: rst_mod_g_rst_n
23	AXI_DISABLE_OOO	R	0h	Disable Out-Of-Order R channel responses [AXI_MASTER_WRAPPER_DISABLE_OOO], RO. This relates to number of IDs used at AXI IF. If Out-Of-Order R channel responses are not disabled this count may be greater than one and in such a case the R channel responses may come Out-Of-Order. The flag gives information about number of used AXI IDs: '0': single ID, '1': multiple IDs. Reset Source: rst_mod_g_rst_n
22	AXI_MASTER_WRAPPER_SPLIT_BYTE_BURSTS	R	1h	AXI_MASTER_WRAPPER_SPLIT_BYTE_BURSTS, RO. Presents information about AXI byte burst capability: '0': no byte bursts, '1': byte bursts enabled. Reset Source: rst_mod_g_rst_n
21:17	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
16	AXI_ADDRESS_WIDTH_64	R	1h	AXI address bus width capability, RO. '0': 32-bit address bus width, '1': 64-bit address bus width. Reset Source: rst_mod_g_rst_n
15:8	XECP_AXI_CAP_OFFSET	R	5h	Next capability Offset, RO. This field points to the xHC MMIO space offset of the next xHCI extended capability pointer. A value of 00h indicates the end of the extended capability list. A non-zero value in this register indicates a relative offset, in Dwords, from this Dword to the beginning of the next extended capability. Reset Source: rst_mod_g_rst_n
7:0	AXI_CAP_ID	R	C2h	VEND_DEF_AXI_MASTER_WRAPPER_CAP_ID, RO. Vendor defined xHCI Extended Capability: 0xC2. This field identifies the AXI wrapper xHCI Extended capability. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.171 USB3P0SS_CTRL_XHCI_XECP_AXI_CFG0 Register

1 USB3P0SS_CTRL_XHCI_XECP_AXI_CFG0 Register (Offset = 8030h) [reset = 80F080Fh]

AXI Initiator Wrapper Extended Capability Configuration Register. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21367. Instance Table

Instance Name	Physical Address
USB0	0F40 8030h

Figure 14-7061. USB3P0SS_CTRL_XHCI_XECP_AXI_CFG0 Name Register

31	30	29	28	27	26	25	24
AXI_RD_DEPTH							
R							
8h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDZ2		AXI_MAX_RD_OT					
R		R					
0h		Fh					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AXI_WR_DEPTH							
R							
8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVDZ1		AXI_MAX_WR_OT					
R		R					
0h		Fh					

Table 14-21369. USB3P0SS_CTRL_XHCI_XECP_AXI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	AXI_RD_DEPTH	R	8h	AXI READ_BUFFER_DEPTH, RO. Number of AXI Read beats that can be buffered by the AXI Master wrapper. The value written to this field should be the Number of AXI Read beats that can be buffered by the AXI Master wrapper minus 1. Reset Source: rst_mod_g_rst_n
23:22	RSVDZ2	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
21:16	AXI_MAX_RD_OT	R	Fh	AXI MAX_READ_OUTSTANDING, RO. Maximum number of Outstanding Read Transactions initiated by the AXI Master wrapper in AR channel. The value written to this field should be the Maximum number of Outstanding Read Transactions initiated by the AXI Master wrapper minus 1, thus the Maximum number of Outstanding Read Transactions is 1 more than the programmed value. Reset Source: rst_mod_g_rst_n
15:8	AXI_WR_DEPTH	R	8h	AXI WRITE_BUFFER_DEPTH, RO. Number of AXI Write beats that can be buffered by the AXI Master wrapper. The value written to this field should be the number of AXI Write beats that can be buffered by the AXI Master wrapper minus 1. Reset Source: rst_mod_g_rst_n

Table 14-21369. USB3P0SS_CTRL_XHCI_XECP_AXI_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	RSVDZ1	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
5:0	AXI_MAX_WR_OT	R	Fh	AXI MAX_WRITE_OUTSTANDING, RO. Maximum number of Outstanding Write Transactions initiated by the AXI Master wrapper in AW channel. The value written to this field should be the Maximum number of Outstanding Write Transactions initiated by the AXI Master wrapper minus 1, thus the Maximum number of Outstanding Write Transactions is 1 more than the programmed value. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.172 USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL0 Register

1 USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL0 Register (Offset = 8034h) [reset = Fh]

AXI Initiator Wrapper Extended Capability Control Register 0. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21370. Instance Table

Instance Name	Physical Address
USB0	**0F40 8034h**

Figure 14-7062. USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL0 Name Register

31	30	29	28	27	26	25	24
RSVDP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVDP				AXI_BMAX			
R				R/W			
0h				Fh			

Table 14-21372. USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVDP	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
3:0	AXI_BMAX	R/W	Fh	AXI BMAX, RW. The register controls maximum burst length - it is used by the AXI Master wrapper to determine maximum value of AxLEN. It uses AXI AxLEN encoding. Default value is the maximum supported one and it is implementation specific. Writing value greater than maximum will result in setting the register to its defaults. This register can be written only when the AXI Master wrapper is halted [AXI_HALT set to '1'] and idle [AXI_IDLE is '1']. Note: This register should only be written to during the register initialisation process Reset Source: rst_mod_g_rst_n

14.9.2.3.2.173 USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL1 Register

1 USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL1 Register (Offset = 8038h) [reset = F000Fh]

AXI Initiator Wrapper Extended Capability Control Register 1. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21373. Instance Table

Instance Name	Physical Address
USB0	0F40 8038h

Figure 14-7063. USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL1 Name Register

31	30	29	28	27	26	25	24
RSVDP2							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP2		AXI_ROT					
R		R/W					
0h		Fh					
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1		AXI_WOT					
R		R/W					
0h		Fh					

Table 14-21375. USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RSVDP2	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
21:16	AXI_ROT	R/W	Fh	AXI READ_OUTSTANDING, RW. Number of outstanding read transactions that can be initiated by the AXI Master wrapper. Default value of this field is MAX_READ_OUTSTANDING-1 [see AXI_MAX_RD_OT field of XECP_AXI_CFG0 register]. Writing value greater than the default will result in setting the register to its defaults. This register can be written only when the AXI Master wrapper is halted [AXI_HALT set to '1'] and idle [AXI_IDLE is '1']. The value written to this field should be the requested number of outstanding read transactions minus 1, thus the actual number of possible outstanding read transactions is one more than the programmed value. Note: This register should only be written to during the register initialisation process Reset Source: rst_mod_g_rst_n
15:6	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21375. USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	AXI_WOT	R/W	Fh	AXI WRITE_OUTSTANDING, RW. Number of outstanding write transactions that can be initiated by the AXI Master wrapper. Default value of this field is MAX_WRITE_OUTSTANDING-1 [see AXI_MAX_WR_OT field of XECP_AXI_CFG0]. Writing value greater than the default will result in setting the register to its defaults. This register can be written only when the AXI Master wrapper is halted [AXI_HALT set to '1'] and idle [AXI_IDLE is '1']. The value written to this field should be the requested number of outstanding write transactions minus 1, thus the actual number of possible outstanding write transactions is one more than the programmed value. Note: This register should only be written to during the register initialisation process Reset Source: rst_mod_g_rst_n

14.9.2.3.2.174 USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL2 Register

1 USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL2 Register (Offset = 803Ch) [reset = 1h]

AXI Initiator Wrapper Extended Capability Control Register 2. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21376. Instance Table

Instance Name	Physical Address
USB0	0F40 803Ch

Figure 14-7064. USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL2 Name Register

31	30	29	28	27	26	25	24
RSVDP							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP							
R							
0h							
7	6	5	4	3	2	1	0
AXI_WTHRES							
R/W							
1h							

Table 14-21378. USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RSVDP	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21378. USB3P0SS_CTRL_XHCI_XECP_AXI_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	AXI_WTHRES	R/W	1h	AXI Write Buffer Threshold, RW. When performing an AXI write burst this field specifies the minimum number of required AXI beats buffered prior to starting the burst on AXI W-Channel by asserting wvalid. This allows a user to balance the requirement for minimal latency with the requirement for low bus utilisation during bursts. Burst lengths smaller than or equal to this threshold will be buffered completely and then output on W-Channel. Burst lengths greater than this threshold will output the burst on the W-Channel such that the first AXI_WTHRES beats will be continuously with no drop of WVALID, beats thereafter may or may not be continuous depending on availability of data. Legal values are between 1 and [AXI_WDD-1]. A value of 1 means that the burst is started on W-Channel as soon as any data is available without any additional delay. A value of 0 is reserved and should not be used as may lead to unpredictable behaviour. This register can be written only when the AXI Master wrapper is halted [AXI_HALT set to '1'] and idle [AXI_IDLE is '1']. Note: This register should only be written to during the register initialisation process. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.175 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP0 Register

1 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP0 Register (Offset = 8040h) [reset = 2000802h]

xHCI Supported Protocol Capability.

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Table 14-21379. Instance Table

Instance Name	Physical Address
USB0	**0F40 8040h**

Figure 14-7065. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP0 Name Register

31	30	29	28	27	26	25	24
MAJOR_REV							
R							
2h							
23	22	21	20	19	18	17	16
MINOR_REV							
R							
0h							
15	14	13	12	11	10	9	8
NEXTCAPID							
R							
8h							
7	6	5	4	3	2	1	0
PID							
R							
2h							

Table 14-21381. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAJOR_REV	R	2h	Major Specification Release Number in Binary-Coded Decimal [i.e.,version 3.x is 03h]. This field identifies the major release number component of the specification with which the xHC is compliant. Reset Source: rst_mod_g_rst_n
23:16	MINOR_REV	R	0h	Minor Specification Release Number in Binary-Coded Decimal [i.e.,version x.10 is 10h]. This field identifies the minor release number component of the specification with which the xHC is compliant. Reset Source: rst_mod_g_rst_n
15:8	NEXTCAPID	R	8h	This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 142 of xHCI specification for more information on this field. Reset Source: rst_mod_g_rst_n
7:0	PID	R	2h	Capability ID. The value identifies the capability as Supported Protocol. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.176 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP1 Register

1 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP1 Register (Offset = 8044h) [reset = 20425355h]

xHCI Supported Protocol Capability.

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Table 14-21382. Instance Table

Instance Name	Physical Address
USB0	**0F40 8044h**

Figure 14-7066. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP1 Name Register

31	30	29	28	27	26	25	24
USB_STRING							
R							
20425355h							
23	22	21	20	19	18	17	16
USB_STRING							
R							
20425355h							
15	14	13	12	11	10	9	8
USB_STRING							
R							
20425355h							
7	6	5	4	3	2	1	0
USB_STRING							
R							
20425355h							

Table 14-21384. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USB_STRING	R	20425355h	Name String, RO. This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive. Refer to section 7.2.2 of xHCI specification for defined values. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.177 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP2 Register

1 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP2 Register (Offset = 8048h) [reset = 30190101h]

xHCI Supported Protocol Capability. USB 2.0 protocol

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Table 14-21385. Instance Table

Instance Name	Physical Address
USB0	**0F40 8048h**

Figure 14-7067. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP2 Name Register

31	30	29	28	27	26	25	24
PSIC				RSVDP_2			
R				R			
3h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVDP_2			HLC_BESL	HLC	IHI	HSO	L1C
R			R	R	R	R	R
0h			1h	1h	0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COMPATIBLE_PORT_COUNT							
R							
1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMPATIBLE_PORT_OFFSET							
R							
1h							

Table 14-21387. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PSIC	R	3h	Protocol Speed ID Count: 3, USB 2.0 Speed [High, Full, Low]. This field indicates the number of Protocol Speed ID [PSI] Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply. Reset Source: rst_mod_g_rst_n
27:21	RSVDP_2	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21387. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_CAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	HLC_BESL	R	1h	HLC_BESL. In xHCI 1.0 specification this field is reserved RsvdP, see section 7.2.2.1.3. The field is described in xHCI 1.1 specification: BESL LPM Capability [BLC], RO. Default = Implementation dependent. If this bit is set to '1', the ports described by this xHCI Supported Protocol Capability shall apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers, as defined in Table 13. If this bit is cleared to '0', the ports described by this xHCI Supported Protocol Capability shall apply HIRD timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers, as defined in Table 13. Refer to section 4.23.5.1.1.1 for more information. Note the BESL LMP Capability support [i.e. HLE = 1 and BLC = 1] shall be mandatory for all xHCI 1.1 compliant xHCs. Reset Source: rst_mod_g_rst_n
19	HLC	R	1h	Hardware LPM Capability. Default = Implementation dependent. If this bit is set to '1', the ports described by this xHCI Supported Protocol Capability support hardware controlled USB2 Link Power Management. Refer to section 4.23.5.1.1.1 of xHCI specification. Reset Source: rst_mod_g_rst_n
18	IHI	R	0h	Integrated Hub Implemented. Default = Implementation dependent. If this bit is cleared to '0', the Root Hub to External xHC port mapping adheres to the default mapping described in section 4.24.2.1 of xHCI specification. If this bit is set to '1', the Root Hub to External xHC port mapping does not adhere to the default mapping described in section 4.24.2.1 of xHCI specification, and an ACPI or other mechanism is required to define the mapping. Reset Source: rst_mod_g_rst_n
17	HSO	R	0h	High-speed Only. Default = Implementation dependent. If this bit is cleared to '0', the USB2 ports described by this capability are Low-, Full-, and High-speed capable. If this bit is set to '1', the USB2 ports described by this capability are High-speed only, e.g. the ports do not support Low- or Full-speed operation. High-speed only implementations may introduce a Tier mismatch, refer to section 4.24.2 of xHCI specification for more information. Reset Source: rst_mod_g_rst_n
16	L1C	R	1h	If '1'LPM is supported [mandatory in xHCI1_00]. In xHCI specification this field is reserved RsvdP, see section 7.2.2.1.3 Reset Source: rst_mod_g_rst_n
15:8	COMPATIBLE_PORT_COUNT	R	1h	This field identifies the number of consecutive Root Hub Ports [starting at the Compatible Port Offset] that support this protocol. Valid values are 1 to MaxPorts. Reset Source: rst_mod_g_rst_n
7:0	COMPATIBLE_PORT_OFFSET	R	1h	This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are 1 to MaxPorts. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.178 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_PROTOCOL_SLOT_TYPE Register

1 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_PROTOCOL_SLOT_TYPE Register (Offset = 804Ch) [reset = 0h]

Protocol Slot Type. xHCI Supported Protocol Capability

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Table 14-21388. Instance Table

Instance Name	Physical Address
USB0	0F40 804Ch

Figure 14-7068. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_PROTOCOL_SLOT_TYPE Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1			PST				
R			R				
0h			0h				

Table 14-21390. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB2_PROTOCOL_SLOT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4:0	PST	R	0h	This field specifies the Protocol Slot Type value, which may be specified when allocating Device Slots that support this protocol. Valid values are 0 to 31. Refer to sections 4.6.3 and 7.2.2.1.4 of xHCI specification. The value of the Protocol Slot Type field declared by a xHCI Supported Protocol Capability structure is unique to an xHC implementation. Software shall not assume a fixed mapping of the Protocol Slot Type value to a specific type of Supported Protocol. Note that for compatibility reasons, the Protocol Slot Type value of 0 is the exception to this rule and reserved for the USB Protocol Device Slot type. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.179 USB3P0SS_CTRL_XHCI_XECP_PSI_FULL_SPEED Register

1 USB3P0SS_CTRL_XHCI_XECP_PSI_FULL_SPEED Register (Offset = 8050h) [reset = C0021h]

Protocol Speed ID, xHCI Supported Protocol Capability

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Table 14-21391. Instance Table

Instance Name	Physical Address
USB0	**0F40 8050h**

Figure 14-7069. USB3P0SS_CTRL_XHCI_XECP_PSI_FULL_SPEED Name Register

31	30	29	28	27	26	25	24
PSIM							
R							
Ch							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PSIM							
R							
Ch							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP1							PFD
R							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLT		PSIE		PSIV			
R		R		R			
0h		2h		1h			

Table 14-21393. USB3P0SS_CTRL_XHCI_XECP_PSI_FULL_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PSIM	R	Ch	Protocol Speed ID Mantissa. This field defines the mantissa that shall be applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword. Reset Source: rst_mod_g_rst_n
15:9	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
8	PFD	R	0h	PSI Full-duplex. If this bit is '1' the link is full-duplex, and if '0' the link is half-duplex. Reset Source: rst_mod_g_rst_n

Table 14-21393. USB3P0SS_CTRL_XHCI_XECP_PSI_FULL_SPEED Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	PLT	R	0h	PSI Type. This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV. PLT Values and corresponding bit rate: 0: Symmetric [Single PSI Dword] 1: Reserved 2: Asymmetric Rx [Paired with Asymmetric Tx PSI Dword] 3: Asymmetric Tx [Immediately follows Rx Asymmetric PSI Dword]. Reset Source: rst_mod_g_rst_n
5:4	PSIE	R	2h	Protocol Speed ID Exponent. This field defines the base 10 exponent times 3, that shall be applied to the Protocol Speed ID Mantissa when calculating the maximum bit rate represented by this PSI Dword. PSIE Values and corresponding bit rates: 0: Bits per second 1: Kb/s 2: Mb/s 3: Gb/s . Reset Source: rst_mod_g_rst_n
3:0	PSIV	R	1h	Protocol Speed ID Value. If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field shall be reported in the Port Speed field of PORTSC register [5.4.8 of xHCI specification] of a compatible port. Note, the PSIV value of 0 is reserved and shall not be defined by a PSI. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.180 USB3P0SS_CTRL_XHCI_XECP_PSI_LOW_SPEED Register

1 USB3P0SS_CTRL_XHCI_XECP_PSI_LOW_SPEED Register (Offset = 8054h) [reset = 5DC0012h]

Protocol Speed ID, xHCI Supported Protocol Capability

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Table 14-21394. Instance Table

Instance Name	Physical Address
USB0	**0F40 8054h**

Figure 14-7070. USB3P0SS_CTRL_XHCI_XECP_PSI_LOW_SPEED Name Register

31	30	29	28	27	26	25	24
PSIM							
R							
5DCh							
23	22	21	20	19	18	17	16
PSIM							
R							
5DCh							
15	14	13	12	11	10	9	8
RSVDP1							PFD
R							R
0h							0h
7	6	5	4	3	2	1	0
PLT		PSIE		PSIV			
R		R		R			
0h		1h		2h			

Table 14-21396. USB3P0SS_CTRL_XHCI_XECP_PSI_LOW_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PSIM	R	5DCh	Protocol Speed ID Mantissa. This field defines the mantissa that shall be applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword. Reset Source: rst_mod_g_rst_n
15:9	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
8	PFD	R	0h	PSI Full-duplex. If this bit is '1' the link is full-duplex, and if '0' the link is half-duplex. Reset Source: rst_mod_g_rst_n

Table 14-21396. USB3P0SS_CTRL_XHCI_XECP_PSI_LOW_SPEED Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	PLT	R	0h	PSI Type. This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV. PLT Values and corresponding bit rate: 0: Symmetric Single [PSI Dword] 1: Reserved 2: Asymmetric Rx [Paired with Asymmetric Tx PSI Dword] 3: Asymmetric Tx [Immediately follows Rx Asymmetric PSI Dword]. Reset Source: rst_mod_g_rst_n
5:4	PSIE	R	1h	Protocol Speed ID Exponent. This field defines the base 10 exponent times 3, that shall be applied to the Protocol Speed ID Mantissa when calculating the maximum bit rate represented by this PSI Dword. PSIE Values and corresponding bit rates: 0: Bits per second 1: Kb/s 2: Mb/s 3: Gb/s . Reset Source: rst_mod_g_rst_n
3:0	PSIV	R	2h	Protocol Speed ID Value. If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field shall be reported in the Port Speed field of PORTSC register [5.4.8 of xHCI specification] of a compatible port. Note, the PSIV value of 0 is reserved and shall not be defined by a PSI. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.181 USB3P0SS_CTRL_XHCI_XECP_PSI_HIGH_SPEED Register

1 USB3P0SS_CTRL_XHCI_XECP_PSI_HIGH_SPEED Register (Offset = 8058h) [reset = 1E00023h]

Protocol Speed ID, xHCI Supported Protocol Capability

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Table 14-21397. Instance Table

Instance Name	Physical Address
USB0	**0F40 8058h**

Figure 14-7071. USB3P0SS_CTRL_XHCI_XECP_PSI_HIGH_SPEED Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PSIM</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1E0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PSIM</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1E0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RSVDP1</td><td>PFD</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PLT</td><td colspan="2">PSIE</td><td colspan="4">PSIV</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">2h</td><td colspan="4">3h</td></tr>
</table>

Table 14-21399. USB3P0SS_CTRL_XHCI_XECP_PSI_HIGH_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PSIM	R	1E0h	Protocol Speed ID Mantissa. This field defines the mantissa that shall be applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword. Reset Source: rst_mod_g_rst_n
15:9	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
8	PFD	R	0h	PSI Full-duplex. If this bit is '1' the link is full-duplex, and if '0' the link is half-duplex. Reset Source: rst_mod_g_rst_n

Table 14-21399. USB3P0SS_CTRL_XHCI_XECP_PSI_HIGH_SPEED Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	PLT	R	0h	PSI Type. This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV. PLT Values and corresponding bit rate: 0: Symmetric Single [PSI Dword] 1: Reserved 2: Asymmetric Rx [Paired with Asymmetric Tx PSI Dword] 3: Asymmetric Tx [Immediately follows Rx Asymmetric PSI Dword]. Reset Source: rst_mod_g_rst_n
5:4	PSIE	R	2h	Protocol Speed ID Exponent. This field defines the base 10 exponent times 3, that shall be applied to the Protocol Speed ID Mantissa when calculating the maximum bit rate represented by this PSI Dword. PSIE Values and corresponding bit rates: 0: Bits per second 1: Kb/s 2: Mb/s 3: Gb/s . Reset Source: rst_mod_g_rst_n
3:0	PSIV	R	3h	Protocol Speed ID Value. If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field shall be reported in the Port Speed field of PORTSC register [5.4.8 of xHCI specification] of a compatible port. Note, the PSIV value of 0 is reserved and shall not be defined by a PSI. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.182 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP0 Register

1 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP0 Register (Offset = 8060h) [reset = 3000802h]

xHCI Supported Protocol Capability.

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Table 14-21400. Instance Table

Instance Name	Physical Address
USB0	**0F40 8060h**

Figure 14-7072. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP0 Name Register

31	30	29	28	27	26	25	24
MAJOR_REV							
R							
3h							
23	22	21	20	19	18	17	16
MINOR_REV							
R							
0h							
15	14	13	12	11	10	9	8
NEXTCAPID							
R							
8h							
7	6	5	4	3	2	1	0
PID							
R							
2h							

Table 14-21402. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAJOR_REV	R	3h	Major Specification Release Number in Binary-Coded Decimal [i.e.,version 3.x is 03h]. This field identifies the major release number component of the specification with which the xHC is compliant. Reset Source: rst_mod_g_rst_n
23:16	MINOR_REV	R	0h	Minor Specification Release Number in Binary-Coded Decimal [i.e.,version x.10 is 10h]. This field identifies the minor release number component of the specification with which the xHC is compliant. Reset Source: rst_mod_g_rst_n
15:8	NEXTCAPID	R	8h	This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 142 of xHCI specification for more information on this field. Reset Source: rst_mod_g_rst_n
7:0	PID	R	2h	Capability ID. The value identifies the capability as Supported Protocol. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.183 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP1 Register

1 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP1 Register (Offset = 8064h) [reset = 20425355h]

xHCI Supported Protocol Capability.

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Table 14-21403. Instance Table

Instance Name	Physical Address
USB0	**0F40 8064h**

Figure 14-7073. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP1 Name Register

31	30	29	28	27	26	25	24
USB_STRING							
R							
20425355h							
23	22	21	20	19	18	17	16
USB_STRING							
R							
20425355h							
15	14	13	12	11	10	9	8
USB_STRING							
R							
20425355h							
7	6	5	4	3	2	1	0
USB_STRING							
R							
20425355h							

Table 14-21405. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USB_STRING	R	20425355h	Name String, RO. This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive. Refer to section 7.2.2 of xHCI specification for defined values. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.184 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP2 Register

1 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP2 Register (Offset = 8068h) [reset = 10000102h]

xHCI Supported Protocol Capability. USB 3.0 protocol

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Table 14-21406. Instance Table

Instance Name	Physical Address
USB0	**0F40 8068h**

Figure 14-7074. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">PSIC</td><td colspan="4">RSVDP1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVDP1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COMPATIBLE_PORT_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMPATIBLE_PORT_OFFSET</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-21408. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PSIC	R	1h	Protocol Speed ID CountCount : 1, USB 3.0 Speed [Super Speed]. This field indicates the number of Protocol Speed ID [PSI] Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply. Reset Source: rst_mod_g_rst_n
27:16	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
15:8	COMPATIBLE_PORT_COUNT	R	1h	This field identifies the number of consecutive Root Hub Ports [starting at the Compatible Port Offset] that support this protocol. Valid values are 1 to MaxPorts. Reset Source: rst_mod_g_rst_n
7:0	COMPATIBLE_PORT_OFFSET	R	2h	This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are 1 to MaxPorts. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.185 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_PROTOCOL_SLOT_TYPE Register

1 USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_PROTOCOL_SLOT_TYPE Register (Offset = 806Ch) [reset = 0h]

Protocol Slot Type. xHCI Supported Protocol Capability

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Table 14-21409. Instance Table

Instance Name	Physical Address
USB0	0F40 806Ch

Figure 14-7075. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_PROTOCOL_SLOT_TYPE Name Register

31	30	29	28	27	26	25	24
RSVDP1							
R							
0h							
23	22	21	20	19	18	17	16
RSVDP1							
R							
0h							
15	14	13	12	11	10	9	8
RSVDP1							
R							
0h							
7	6	5	4	3	2	1	0
RSVDP1			PST				
R			R				
0h			0h				

Table 14-21411. USB3P0SS_CTRL_XHCI_XECP_SUPP_USB3_PROTOCOL_SLOT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4:0	PST	R	0h	This field specifies the Protocol Slot Type value, which may be specified when allocating Device Slots that support this protocol. Valid values are 0 to 31. Refer to sections 4.6.3 and 7.2.2.1.4 of xHCI specification. The value of the Protocol Slot Type field declared by a xHCI Supported Protocol Capability structure is unique to an xHC implementation. Software shall not assume a fixed mapping of the Protocol Slot Type value to a specific type of Supported Protocol. Note that for compatibility reasons, the Protocol Slot Type value of 0 is the exception to this rule and reserved for the USB Protocol Device Slot type. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.186 USB3P0SS_CTRL_XHCI_PSI_SUPER_SPEED Register

1 USB3P0SS_CTRL_XHCI_PSI_SUPER_SPEED Register (Offset = 8070h) [reset = 50134h]

Protocol Speed ID, xHCI Supported Protocol Capability

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Table 14-21412. Instance Table

Instance Name	Physical Address
USB0	**0F40 8070h**

Figure 14-7076. USB3P0SS_CTRL_XHCI_PSI_SUPER_SPEED Name Register

31	30	29	28	27	26	25	24
PSIM							
R							
5h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PSIM							
R							
5h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVDP1							PFD
R							R
0h							1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLT		PSIE		PSIV			
R		R		R			
0h		3h		4h			

Table 14-21414. USB3P0SS_CTRL_XHCI_PSI_SUPER_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PSIM	R	5h	Protocol Speed ID Mantissa. This field defines the mantissa that shall be applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword. Reset Source: rst_mod_g_rst_n
15:9	RSVDP1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
8	PFD	R	1h	PSI Full-duplex. If this bit is '1' the link is full-duplex, and if '0' the link is half-duplex. Reset Source: rst_mod_g_rst_n

Table 14-21414. USB3P0SS_CTRL_XHCI_PSI_SUPER_SPEED Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	PLT	R	0h	PSI Type. This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV. PLT Values and corresponding bit rate: 0: Symmetric Single [PSI Dword] 1: Reserved 2: Asymmetric Rx [Paired with Asymmetric Tx PSI Dword] 3: Asymmetric Tx [Immediately follows Rx Asymmetric PSI Dword]. Reset Source: rst_mod_g_rst_n
5:4	PSIE	R	3h	Protocol Speed ID Exponent. This field defines the base 10 exponent times 3, that shall be applied to the Protocol Speed ID Mantissa when calculating the maximum bit rate represented by this PSI Dword. PSIE Values and corresponding bit rates: 0: Bits per second 1: Kb/s 2: Mb/s 3: Gb/s . Reset Source: rst_mod_g_rst_n
3:0	PSIV	R	4h	Protocol Speed ID Value. If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field shall be reported in the Port Speed field of PORTSC register [5.4.8 of xHCI specification] of a compatible port. Note, the PSIV value of 0 is reserved and shall not be defined by a PSI. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.187 USB3P0SS_CTRL_XHCI_XECP_CMDM_STS0 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_STS0 Register (Offset = 8080h) [reset = CC1h]

Command Ring related status register. Command manager status debug register. This is a vendor defined capability. This register is reserved. This register should not be modified by software. It is described only for informative purposes.

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Table 14-21415. Instance Table

Instance Name	Physical Address
USB0	0F40 8080h

Figure 14-7077. USB3P0SS_CTRL_XHCI_XECP_CMDM_STS0 Name Register

31	30	29	28	27	26	25	24
IDMA_CNTX_IN_USE	ODMA_CNTX_IN_USE	TRM_CNTX_IN_USE	CMDM_CNTX_LOCK_REQ	CMDM_STOP_REQ	CMDM_CLR_DB_REQ	ODMA_ADDRESS_DEV_DONE	ODMA_ADDRESS_DEV_PENDING
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
UPDATE_ENDPT_ACTIVE	DBM_EP_UPD_REQ	TRM_EPERR_UPD_REQ	TRM_STALL_REQ	RESERVED_R	STOPPING_CMD_RING	HOST_CMD_DB_RANG_STICKY	CMD_RUNNING
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
XECP_CMDM_NEXT_CAP_OFFSET							
R							
Ch							
7	6	5	4	3	2	1	0
VEND_DEF_CMDM_CAP_ID_193							
R							
C1h							

Table 14-21417. USB3P0SS_CTRL_XHCI_XECP_CMDM_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDMA_CNTX_IN_USE	R	0h	Indicates that IDMA module currently owns the context access : Reset Source: rst_mod_g_rst_n
30	ODMA_CNTX_IN_USE	R	0h	Indicates that ODMA module currently owns currently the context access Reset Source: rst_mod_g_rst_n
29	TRM_CNTX_IN_USE	R	0h	Indicates that TRM modules owns the context access currently Reset Source: rst_mod_g_rst_n
28	CMDM_CNTX_LOCK_REQ	R	0h	Indicates that Command Manager has requested a context lock. Reset Source: rst_mod_g_rst_n
27	CMDM_STOP_REQ	R	0h	Indicates that Command Ring stop command is in progress. Reset Source: rst_mod_g_rst_n
26	CMDM_CLR_DB_REQ	R	0h	Indicates that clearing an EP out of schedule is in progress. Reset Source: rst_mod_g_rst_n

Table 14-21417. USB3P0SS_CTRL_XHCI_XECP_CMDM_STS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	ODMA_ADDRESS_DEV_DONE	R	0h	Indicates that current address device command is done by ODMA. Reset Source: rst_mod_g_rst_n
24	ODMA_ADDRESS_DEV_PENDING	R	0h	Indicates that ODMA has an address device command in progress. Reset Source: rst_mod_g_rst_n
23	UPDATE_ENDPT_ACTIVE	R	0h	Indicates that updating of EP state is in progress Reset Source: rst_mod_g_rst_n
22	DBM_EP_UPD_REQ	R	0h	Indicates that Doorbell Manager is issuing and EP update due to a doorbell ring on an EP that is in stop state Reset Source: rst_mod_g_rst_n
21	TRM_EPERR_UPD_REQ	R	0h	Indicates that Transfer Ring Manager is issuing and EP update due to an EP error condition detected Reset Source: rst_mod_g_rst_n
20	TRM_STALL_REQ	R	0h	Indicates that transfer ring manager is issuing and EP state update due to stall received Reset Source: rst_mod_g_rst_n
19	RESERVED_R	R	0h	Reserved field, RO
18	STOPPING_CMD_RING	R	0h	Indicates that a STOP on the Command Ring is in progress Reset Source: rst_mod_g_rst_n
17	HOST_CMD_DB_RANG_STICKY	R	0h	Indicates that command ring has a doorbell pending Reset Source: rst_mod_g_rst_n
16	CMD_RUNNING	R	0h	Indicates that the command ring is running Reset Source: rst_mod_g_rst_n
15:8	XECP_CMDM_NEXT_CAP_OFFSET	R	Ch	Next capability offset Reset Source: rst_mod_g_rst_n
7:0	VEND_DEF_CMDM_CAP_ID_193	R	C1h	Vendor defined capability ID. Command Ring Manager capability ID. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.188 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_1 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_1 Register (Offset = 8084h) [reset = 0h]

Event ring manager module reserved space. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21418. Instance Table

Instance Name	Physical Address
USB0	**0F40 8084h**

Figure 14-7078. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_1 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_R							
R							
0h							

Table 14-21420. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_R	R	0h	Reserved field, RO.

14.9.2.3.2.189 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_2 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_2 Register (Offset = 8088h) [reset = 0h]

Event ring manager module reserved space. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21421. Instance Table

Instance Name	Physical Address
USB0	**0F40 8088h**

Figure 14-7079. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_2 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_R							
R							
0h							

Table 14-21423. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_R	R	0h	Reserved field, RO.

14.9.2.3.2.190 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_3 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_3 Register (Offset = 808Ch) [reset = 0h]

Event ring manager module reserved space. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21424. Instance Table

Instance Name	Physical Address
USB0	**0F40 808Ch**

Figure 14-7080. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_3 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_R							
R							
0h							

Table 14-21426. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_R	R	0h	Reserved field, RO.

14.9.2.3.2.191 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_4 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_4 Register (Offset = 8090h) [reset = 0h]

Event ring manager module reserved space. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21427. Instance Table

Instance Name	Physical Address
USB0	**0F40 8090h**

Figure 14-7081. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_4 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_R							
R							
0h							

Table 14-21429. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_R	R	0h	Reserved field, RO.

14.9.2.3.2.192 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_5 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_5 Register (Offset = 8094h) [reset = 0h]

Event ring manager module reserved space. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21430. Instance Table

Instance Name	Physical Address
USB0	**0F40 8094h**

Figure 14-7082. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_5 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_R							
R							
0h							

Table 14-21432. USB3P0SS_CTRL_XHCI_XECP_CMDM_RESERVED_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_R	R	0h	Reserved field, RO.

14.9.2.3.2.193 USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG1 Register (Offset = 8098h) [reset = 3580AFFCh]

Command Manager Control register 1. This register contains fields which control the behavior of the Command Manager in the xHCI. The functions controlled by this register are made available largely for debug/diagnostic purposes. This functionality is above and beyond that defined in the xHCI specification. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21433. Instance Table

Instance Name	Physical Address
USB0	**0F40 8098h**

Figure 14-7083. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG1 Name Register

31	30	29	28	27	26	25	24
DEFAULT_INTR_EP_BANDWIDTH				DEFAULT_ISOCH_EP_BANDWIDTH			
R/W				R/W			
3h				5h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EVAL_CNTX_BW_SCAN_EN	FEATURE_RETRY_EN	CFG_ENDPT_CNTX_LOCK_DIS	ENABLE_MAX_EP_CACHE	REPORT_BANDWIDTH_SKIP_SCAN	FORCE_BANDWIDTH_SYS_PASS	FORCE_BANDWIDTH_PASS	CLR_SPLIT_STATE_WITH_TSPSET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLR_EP_CNTX_4DIS_SLOT	EVAL_EPST_CHECK_EN	INIT_RETRY	GLOB_TSP_EN	CLR_EP_CNTX_4CFG_ENDPT	CLR_EP_CNTX_4RST_DEVICE	CLR_EP_CNTX_4RST_ENDPT	CLR_EP_CNTX_4EN_SLOT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	1h	1h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLR_CNTX_4ENCFGENDPT	CLR_CNTX_4ENADDR	CLR_CNTX_4ENSLOT_REG	CLR_CNTX_4RSTDEV	ADDR_DEV_SLST_BSR_CHECK_EN	CLR_CNTX_4SETDQPTR	FORCE_BANDWIDTH_FAIL	UPDATE_ENDPT_EVENT_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	0h	0h

Table 14-21435. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	DEFAULT_INTR_EP_BANDWIDTH	R/W	3h	Bandwidth calculation parameter: Default bandwidth for an Interrupt Endpoint. Reset Source: rst_mod_g_rst_n
27:24	DEFAULT_ISOCH_EP_BANDWIDTH	R/W	5h	Bandwidth calculation parameter: Default bandwidth for an Isochronous Endpoint. Reset Source: rst_mod_g_rst_n
23	EVAL_CNTX_BW_SCAN_EN	R/W	1h	Enable the Host Controller's Bandwidth checks for the Evaluate Context Command. Rescan the BW during evaluate context Reset Source: rst_mod_g_rst_n

Table 14-21435. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	FEATURE_RETRY_EN	R/W	0h	Enable the EOB and NPKT==0 [called NYET condition for USB3] to be used to update a retry bit during stream switching operation. This is an internal safety feature. It should be treated as reserved bit. Reset Source: rst_mod_g_rst_n
21	CFG_ENDPT_CNTX_LOCK_DIS	R/W	0h	Context lock mechanism to ensure command manager has exclusive access to internal context. This is a disable bit to allow software to turn off the context lock for configure endpoint command. This is a test/debug feature. '1': indicates disabled. '0': Indicates enabled Reset Source: rst_mod_g_rst_n
20	ENABLE_MAX_EP_CACHE	R/W	0h	enable_max_ep_cache Reset Source: rst_mod_g_rst_n
19	REPORT_BANDWIDTH_SKIP_SCAN	R/W	0h	report_bandwidth_skip_scan Reset Source: rst_mod_g_rst_n
18	FORCE_BANDWIDTH_SYS_PASS	R/W	0h	force_bandwidth_sys_pass Reset Source: rst_mod_g_rst_n
17	FORCE_BANDWIDTH_PASS	R/W	0h	force_bandwidth_pass Reset Source: rst_mod_g_rst_n
16	CLR_SPLIT_STATE_WITH_TSPSET	R/W	0h	This bit allows engine to reset the split states when reset endpoint with TSP is posted. The split state is an internal context field in DMA engine. '0': Indicates that reset endpoint with TSP will preserve the split state. '1': Indicates that the reset endpoint with TSP will not preserve the split state. Reset Source: rst_mod_g_rst_n
15	CLR_EP_CNTX_4DIS_SLOT	R/W	1h	'0': Disable clearing internal TRM and DMA context as well as the internal EP status signals during a disable slot command. '1': Enable clearing internal TRM and DMA context as well as the internal EP status signals during a disable slot command. Reset Source: rst_mod_g_rst_n
14	EVAL_EPST_CHECK_EN	R/W	0h	'0': Disable evaluating the endpoint state during an Evaluate Context command, '1': Enable EP state check during an Evaluate Context command. If failed, context error will be returned. Reset Source: rst_mod_g_rst_n
13	INIT_RETRY	R/W	1h	init_retry. Reserved to always read value of '1'. Reset Source: rst_mod_g_rst_n
12	GLOB_TSP_EN	R/W	0h	'0': Disable the global context preservation. '1': Enable the internal context preservation for all commands that needs to preserve some of the internal context fields as a command with TSP would. Reset Source: rst_mod_g_rst_n
11	CLR_EP_CNTX_4CFG_ENDPT	R/W	1h	'0': Disable clearing other internal EP status signals during a configure endpoint command. '1': Enable clearing other internal EP related status signals such as EP scheduled array, credit stored per EP, etc. during a configure endpoint command. Reset Source: rst_mod_g_rst_n

Table 14-21435. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	CLR_EP_CNTX_4RST_DEVICE	R/W	1h	'0': Disable clearing other internal EP status signals during a reset device command. '1': Enable clearing other internal EP related status signals such as EP scheduled array, credit stored per EP, etc. during a reset device command. Reset Source: rst_mod_g_rst_n
9	CLR_EP_CNTX_4RST_ENDPT	R/W	1h	'0': Disable clearing other internal EP status signals during a reset endpoint command. '1': Enable clearing other internal EP related status signals such as EP scheduled array, credit stored per EP. etc. during a reset endpoint command. Reset Source: rst_mod_g_rst_n
8	CLR_EP_CNTX_4EN_SLOT	R/W	1h	'0': Disable clearing other internal EP status signals during an enable slot command. '1': Enable clearing other internal EP related status signals such as EP scheduled array, credit stored per EP. etc., during an enable slot command. Reset Source: rst_mod_g_rst_n
7	CLR_CNTX_4ENCFGENDPT	R/W	1h	'0': Disable clearing internal TRM and DMA context during a configure endpoint command. '1': Enable clearing internal TRM and DMA context during a configure endpoint command. Reset Source: rst_mod_g_rst_n
6	CLR_CNTX_4ENADDR	R/W	1h	'0': Disable clearing internal TRM and DMA context during an address device command. '1': Enable clearing internal TRM and DMA context during an address device command. Reset Source: rst_mod_g_rst_n
5	CLR_CNTX_4ENSLOT_REG	R/W	1h	'0': Disable clearing internal TRM and DMA context during an enable slot command. '1': Enable clearing internal TRM and DMA context during an enable slot command. Reset Source: rst_mod_g_rst_n
4	CLR_CNTX_4RSTDEV	R/W	1h	'0': Disable clearing internal TRM and DMA context during a reset device command. '1': Enable clearing internal TRM and DMA context during a reset device command. Reset Source: rst_mod_g_rst_n
3	ADDR_DEV_SLST_BSR_CHECK_EN	R/W	1h	'0': Address device does not return the error for this condition. '1': Enable the EP state [default state] check with address device command with BSR. If failed, an event with context state error will be generated. Reset Source: rst_mod_g_rst_n
2	CLR_CNTX_4SETDQPTR	R/W	1h	'0': Disable clearing internal TRM and DMA context during a set TR DQ pointer command. '1': Enable clearing internal TRM and DMA context during a set TR DQ pointer command. Reset Source: rst_mod_g_rst_n
1	FORCE_BANDWIDTH_FAIL	R/W	0h	'0': Bandwidth calculation handled normally. '1': Forces a failure in the endpoint bandwidth calculation so that engine will reject a configure EP command. Reset Source: rst_mod_g_rst_n

Table 14-21435. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	UPDATE_ENDPT_EVENT_ENABLE	R/W	0h	'0': Disable generation of the completion event. '1': Enable the command manager to generate a completion event after an EP state update due to internal error. This bit is for test debug. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.194 USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG2 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG2 Register (Offset = 809Ch) [reset = 6C60000h]

Command Manager Control register 2. This register contains fields which control the behavior of the Command Manager in the xHCI. The functions controlled by this register are made available largely for debug/diagnostic purposes. This functionality is above and beyond that defined in the xHCI specification. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21436. Instance Table

Instance Name	Physical Address
USB0	0F40 809Ch

Figure 14-7084. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG2 Name Register

31	30	29	28	27	26	25	24
DOING_2DW_OCNTX_WR_EN	STOP_ENDPT_2MS_TIMEOUT_EN	SLOT_ID_OVERIDE_EN	SRE	ALL_CLK_GATE_DIS	CLR_EP_CNTX_4STOP_ENDPT	CLR_EP_CNTX_4STALL_UPD	MOVE_XFER_DQPTR_2CPL_DQPTR_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLR_CNTX_4RST_ENDPT_REG	ENABLE_BW_CAL	CMD_ST_DIS_REG	SET_DQPTR_CLR_EP_ARYS	FORCE_RESET_ENDPT_REG	TSP_4SET_DQPTR_REG	TRM_BREAK_LOOP_EN	INCREASE_UPDATE_EP_PRIORITY_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	0h	0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DISABLE_STALL_CLR_EP	BURST_SIZE_DEFAULT_EN	CLR_ST					
R/W	R/W	R/W					
0h	0h	0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLR_ST							
R/W							
0h							

Table 14-21438. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DOING_2DW_OCNTX_WR_EN	R/W	0h	Enable only to update the EP state to output context on every EP output context update condition. This is to allow to have a control over either update the entire EPoutput context field or only update the first two DWORDs. '0': update the entire output context field. '1': update only 2 DWORDs Reset Source: rst_mod_g_rst_n
30	STOP_ENDPT_2MS_TIMEOUT_EN	R/W	0h	Enable a delay to stop endpoint command that is executed in XFER engine. '0': XFER engine will not wait. '1': XFER engine will always wait for 2 ms before it checks whether an EP transfer ring is at a stop of packet boundary Reset Source: rst_mod_g_rst_n

Table 14-21438. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	SLOT_ID_OVERIDE_EN	R/W	0h	Force '0' on slot ID when a command transfer event is generated. '0': not forced, '1': Forced to 0. Reset Source: rst_mod_g_rst_n
28	SRE	R/W	0h	Force and error on save command always. '0': do not force, '1': always force return save error. Reset Source: rst_mod_g_rst_n
27	ALL_CLK_GATE_DIS	R/W	0h	'0': Turn ON the TTE clock. '1': Turn OFF the TTE clock. Reset Source: rst_mod_g_rst_n
26	CLR_EP_CNTX_4STOP_ENDPT	R/W	1h	'0': Disable clearing other internal per EP status signal during a stop endpoint command. '1': Enable clearing other internal per EP status signal during a stop endpoint command. Reset Source: rst_mod_g_rst_n
25	CLR_EP_CNTX_4STALL_UPD	R/W	1h	'0': Disable clearing other internal EP status signal during stall handling. '1': Enable clearing other internal EP status signal during stall handling. Reset Source: rst_mod_g_rst_n
24	MOVE_XFER_DQPTR_2CPL_DQPTR_EN	R/W	0h	'0': The internal context write DQ pointer moved to internal read pointer during reset EP command. '1': The write DQ pointer stays as it was during reset endpoint command. Reset Source: rst_mod_g_rst_n
23	CLR_CNTX_4RST_ENDPT_REG	R/W	1h	'0': Disable clearing internal TRM and DMA context during a reset endpoint command. '1': Enable clearing internal TRM and DMA context during a reset endpoint command. Reset Source: rst_mod_g_rst_n
22	ENABLE_BW_CAL	R/W	1h	'0': Disable hardware bandwidth calculations. '1': Enable hardware bandwidth calculations. Reset Source: rst_mod_g_rst_n
21	CMD_ST_DIS_REG	R/W	0h	'0': Delay processing command ring TRB while internal context requests are pending. '1': Process command ring TRBs normally. Reset Source: rst_mod_g_rst_n
20	SET_DQPTR_CLR_EP_ARYS	R/W	0h	'0': Disable clearing other internal EP status signals during a set DQ pointer command. '1': Enable clearing other internal EP status signals during a set DQ pointer command. Reset Source: rst_mod_g_rst_n
19	FORCE_RESET_ENDPT_REG	R/W	0h	'0': Check the slot and endpoint state prior to processing a reset endpoint command. '1': Ignore the slot and endpoint state when processing a reset endpoint command. Reset Source: rst_mod_g_rst_n
18	TSP_4SET_DQPTR_REG	R/W	1h	'0': Disable sequence number preservation during set DQ pointer command. '1': Enable sequence number to be preserved during set DQ pointer command. Reset Source: rst_mod_g_rst_n

Table 14-21438. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	TRM_BREAK_LOOP_EN	R/W	1h	trm_break_loop_en. This is an internal safeguard register. It enables a different mechanism of handling stop endpoint command. It should be treated as a reserved field. The default should not be alternate unless specific purpose. '0': Disable. '1': Enable. Reset Source: rst_mod_g_rst_n
16	INCREASE_UPDATE_EP_PRIORITY_EN	R/W	0h	Increase Update EP priority over commands in the command ring to avoid prolonging STALL handling. '0': Pending commands have a higher priority than update endpoint processing. '1': Update endpoint processing in the command manager has a higher priority than pending commands. Note: Enabling this bit can prevent prolonged stall handling. Reset Source: rst_mod_g_rst_n
15	DISABLE_STALL_CLR_EP	R/W	0h	'0': Stall handling does clear the internal EP status signals. '1': Disable the clear function when stall response received. Reset Source: rst_mod_g_rst_n
14	BURST_SIZE_DEFAULT_EN	R/W	0h	When context is first initialized, it is assumed one remote NPKT. It is also assumed that max burst size as remote NPKT. This bit enables to assume max burst size as remote NPKT. '0': Assume 1 NPKT. '1': Assume max burst size as NPKT. Reset Source: rst_mod_g_rst_n
13:0	CLR_ST	R/W	0h	Clear state machine present state: Setting a specified bit to '1', will reset the corresponding command manager state machine to the starting/idle state. bit-0: disable slot state machine. bit-1: enable slot state machine. bit-2: reset endpoint state machine. bit-3: reset device state machine. bit-4: command ring state machine. bit-5: stop endpoint state machine. bit-6: set dq pointer state machine. bit-7: force header state machine. bit-8: evaluate context state machine. bit-9: update endpoint state machine. bit-10: address device state machine. bit-11: port bandwidth state machine. bit-12: read output context state machine. bit-13: configure endpoint state machine. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.195 USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG3 Register

1 USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG3 Register (Offset = 80A0h) [reset = 2220505Ah]

Command Manager Control register 3. This register contains fields which control the behavior of the Command Manager in the xHCI. The functions controlled by this register are made available largely for debug/diagnostic purposes. This functionality is above and beyond that defined in the xHCI specification. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21439. Instance Table

Instance Name	Physical Address
USB0	**0F40 80A0h**

Figure 14-7085. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG3 Name Register

31	30	29	28	27	26	25	24
FRINDEX_WR_EN	IGNORE_HI_ATOMIC_EN	EXTRA_DB_RM_4STOP_EN	DISABLE_NON0EP_CNTX_CLR	DISABLE_SETDQPTR_CLR_STREAM_ST	UPDATE_CNTX_WHEN_STOPPED	STOP_EP_CLR_LCSTREAM_ID_EN	SET_BURST_SIZE_4PRDC_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	0h	0h	0h	1h	0h

23	22	21	20	19	18	17	16
STREAM_ALWAYS_UPDATE_CNTX	ALLOW_CLR_4STOP	STOP_EP_CLR_STREAM_ST_EN	BREAK_CNTX_LOCK_EN	STOP_2TIMEOUT_EN	CLR_TRM_DMA_CNTX_EN	DISABLE_SLOT_TIMER_SELECT	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	1h	0h	0h	0h	0h	

15	14	13	12	11	10	9	8
DEFAULT_HS_BANDWD_AVAIL							
R/W							
50h							

7	6	5	4	3	2	1	0
DEFAULT_PORT_BANDWD_AVAIL							
R/W							
5Ah							

Table 14-21441. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FRINDEX_WR_EN	R/W	0h	MFIndex register write enable. For debug purposes. Reset Source: rst_mod_g_rst_n
30	IGNORE_HI_ATOMIC_EN	R/W	0h	ignore_hi_atomic_en Reset Source: rst_mod_g_rst_n
29	EXTRA_DB_RM_4STOP_EN	R/W	1h	extra_db_rm_4stop_en Reset Source: rst_mod_g_rst_n
28	DISABLE_NON0EP_CNTX_CLR	R/W	0h	disable_non0ep_cntx_clr Reset Source: rst_mod_g_rst_n
27	DISABLE_SETDQPTR_CLR_STREAM_ST	R/W	0h	disable_setdqptr_clr_stream_st. Disable setTRDQPtr from clearing the current stream state. Reset Source: rst_mod_g_rst_n

Table 14-21441. USB3P0SS_CTRL_XHCI_XECP_CMDM_CTRL_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	UPDATE_CNTX_WHEN_STOPPED	R/W	0h	update_cntx_when_stopped. Allow setTRDQPtr cmd to update the local context anytime the EP is not running [otherwise checks CSTREAMID]. Reset Source: rst_mod_g_rst_n
25	STOP_EP_CLR_LCSTREAM_ID_EN	R/W	1h	stop_ep_clr_lcstream_id_en. Enable stop endpoint command to return stream st to disabled [0] in EP context. Reset Source: rst_mod_g_rst_n
24	SET_BURST_SIZE_4PRDC_DIS	R/W	0h	set_burst_size_4prdc_dis Reset Source: rst_mod_g_rst_n
23	STREAM_ALWAYS_UPDATE_CNTX	R/W	0h	stream_always_update_cntx Reset Source: rst_mod_g_rst_n
22	ALLOW_CLR_4STOP	R/W	0h	allow_clr_4stop Reset Source: rst_mod_g_rst_n
21	STOP_EP_CLR_STREAM_ST_EN	R/W	1h	stop_ep_clr_stream_st_en. Enable stop endpoint command to return stream st to disabled [0] in EP context. Reset Source: rst_mod_g_rst_n
20	BREAK_CNTX_LOCK_EN	R/W	0h	break_cntx_lock_en Reset Source: rst_mod_g_rst_n
19	STOP_2TIMEOUT_EN	R/W	0h	stop_2timeout_en. Stop transaction timeout. Reset Source: rst_mod_g_rst_n
18	CLR_TRM_DMA_CNTX_EN	R/W	0h	clr_trm_dma_cntx_en Reset Source: rst_mod_g_rst_n
17:16	DISABLE_SLOT_TIMER_SELECT	R/W	0h	These two bits specify the delay that we can have for disable slot state to be completed. We can delay the generation of the command transfer event during disable slot command. Possible values: '00': delay is disabled, '01': 100us delay, '10': 8ms delay, '11': 10ms delay. Reset Source: rst_mod_g_rst_n
15:8	DEFAULT_HS_BANDWD_AVAIL	R/W	50h	The default available bandwidth to advertise on each HS port in 10 0ncrements [80%]. Bandwidth Calculation is a reserved field for PPT. Reset Source: rst_mod_g_rst_n
7:0	DEFAULT_PORT_BANDWD_AVAIL	R/W	5Ah	The default available bandwidth to advertise on each LS, FS, SS port in 10 0ncrements [90%]. Bandwidth calculation is a reserved field for PPT. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.196 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_CAP Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_CAP Register (Offset = 80B0h) [reset = B0C0h]

This is a register that describes the host controller's extended capability location. It is modified and maintained by BIOS.

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Table 14-21442. Instance Table

Instance Name	Physical Address
USB0	0F40 80B0h

Figure 14-7086. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_CAP Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
XECP_HOST_NEXT_CAP_OFFSET							
R							
B0h							
7	6	5	4	3	2	1	0
VEND_DEF_HOST_CAP_ID_192							
R							
C0h							

Table 14-21444. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_R	R	0h	Reserved field, RO.
15:8	XECP_HOST_NEXT_CAP_OFFSET	R	B0h	Next xHCI Extended Capability Pointer. This field points to the xHC MMIO space offset of the next xHCI extended capability pointer. A value of 00h indicates the end of the extended capability list. A non-zero value in this register indicates a relative offset, in Dwords, from this Dword to the beginning of the next extended capability. For example, assuming an effective address of this data structure is 350h and assuming a pointer value of 068h, we can calculate the following effective address: 350h + [068h shifted left 2] -> 350h + 1A0h -> 4F0h Reset Source: rst_mod_g_rst_n
7:0	VEND_DEF_HOST_CAP_ID_192	R	C0h	Capability ID. This field identifies the xHCI Extended capability. 192-255 are IDs available for vendor specific extensions to the xHCI. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.197 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_RSVD Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_RSVD Register (Offset = 80B4h) [reset = 0h]

Reserved space. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21445. Instance Table

Instance Name	Physical Address
USB0	0F40 80B4h

Figure 14-7087. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_RSVD Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-21447. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_RSVD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO.

14.9.2.3.2.198 USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_MASK_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_MASK_REG Register (Offset = 80B8h) [reset = 0h]

Override Endpoint Flow Control. This is a register that is used to clear the internal scheduler's mask that is used to stop scheduling a particular Endpoint. Allows software to clear pending mask. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21448. Instance Table

Instance Name	Physical Address
USB0	**0F40 80B8h**

Figure 14-7088. USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_MASK_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_R</td><td colspan="2">SLOT_NUM</td></tr>
<tr><td colspan="6">R</td><td colspan="2">W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">SLOT_NUM</td><td colspan="4">EP_NUM</td><td>EP_DIR</td></tr>
<tr><td colspan="3">W</td><td colspan="4">W</td><td>W</td></tr>
<tr><td colspan="3">0h</td><td colspan="4">0h</td><td>0h</td></tr>
</table>

Table 14-21450. USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_R	R	0h	Reserved field, RO
9:5	SLOT_NUM	W	0h	Slot number. Reset Source: rst_mod_g_rst_n
4:1	EP_NUM	W	0h	Endpoint number Reset Source: rst_mod_g_rst_n
0	EP_DIR	W	0h	Indicates the direction of the Endpoint Reset Source: rst_mod_g_rst_n

14.9.2.3.2.199 USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_IN_EP_VALID_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_IN_EP_VALID_REG Register (Offset = 80BCh) [reset = 0h]

Clear Active IN EP ID Control. This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21451. Instance Table

Instance Name	Physical Address
USB0	**0F40 80BCh**

Figure 14-7089. USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_IN_EP_VALID_REG Name Register

31	30	29	28	27	26	25	24
PORT_NUM							
W							
0h							
23	22	21	20	19	18	17	16
PORT_NUM							
W							
0h							
15	14	13	12	11	10	9	8
PORT_NUM							
W							
0h							
7	6	5	4	3	2	1	0
PORT_NUM							
W							
0h							

Table 14-21453. USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_IN_EP_VALID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_NUM	W	0h	This field indicates the port number. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.200 USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_PMASK_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_PMASK_REG Register (Offset = 80C0h) [reset = 0h]

Clear Poll Mask Control. This is a register that is used to clear the internal scheduler's poll mask that is used to indicate whether we need to poll this EP. This is used for USB2. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21454. Instance Table

Instance Name	Physical Address
USB0	**0F40 80C0h**

Figure 14-7090. USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_PMASK_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_R</td><td colspan="2">SLOT_NUM</td></tr>
<tr><td colspan="6">R</td><td colspan="2">W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">SLOT_NUM</td><td colspan="4">EP_NUM</td><td>EP_DIR</td></tr>
<tr><td colspan="3">W</td><td colspan="4">W</td><td>W</td></tr>
<tr><td colspan="3">0h</td><td colspan="4">0h</td><td>0h</td></tr>
</table>

Table 14-21456. USB3P0SS_CTRL_XHCI_XECP_HOST_CLR_PMASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_R	R	0h	Reserved field, RO
9:5	SLOT_NUM	W	0h	Slot number Reset Source: rst_mod_g_rst_n
4:1	EP_NUM	W	0h	Endpoint number Reset Source: rst_mod_g_rst_n
0	EP_DIR	W	0h	Indicates the direction of the Endpoint Reset Source: rst_mod_g_rst_n

14.9.2.3.2.201 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_OCRD_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_OCRD_REG Register (Offset = 80C4h) [reset = 0h]

Port Credit Control. This is a register that is used to add or subtract a per port credit or to control the TRM's XFER and CPL states. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21457. Instance Table

Instance Name	Physical Address
USB0	**0F40 80C4h**

Figure 14-7091. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_OCRD_REG Name Register

31	30	29	28	27	26	25	24
CLR_XFER_ST	CLR_CPL_ST	PLUS_OCRD	MINUS_OCRD	MINUS_4RFIFO	ST_UPD_REG	RESERVED_R	
W	W	W	W	W	R	R	
0h	0h	0h	0h	0h	0h	0h	
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
PORT_NUM							
W							
0h							

Table 14-21459. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_OCRD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLR_XFER_ST	W	0h	Write '1' to force XFER state return to IDLE Reset Source: rst_mod_g_rst_n
30	CLR_CPL_ST	W	0h	Write '1' to force CPL state return to IDLE Reset Source: rst_mod_g_rst_n
29	PLUS_OCRD	W	0h	Add one credit to a port Reset Source: rst_mod_g_rst_n
28	MINUS_OCRD	W	0h	Subtract one credit from a port Reset Source: rst_mod_g_rst_n
27	MINUS_4RFIFO	W	0h	Indicates whether the subtract command operates on TX FIFO credit or RX FIFO credit. Reset Source: rst_mod_g_rst_n
26	ST_UPD_REG	R	0h	Slot state control. st_upd_reg Reset Source: rst_mod_g_rst_n
25:8	RESERVED_R	R	0h	Reserved field, RO

Table 14-21459. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_OCRD_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	PORT_NUM	W	0h	port number Reset Source: rst_mod_g_rst_n

14.9.2.3.2.202 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_LO Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_LO Register (Offset = 80C8h) [reset = 0h]

Test Bus Low Bits: Host controller test bus low 32 bits. The register is used to read the internal states and other important signals. The host control test bus is gathered from different internal modules for its important states and control/status information. There is a 64-bit register that allows us to read a bus of 64 bits. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21460. Instance Table

Instance Name	Physical Address
USB0	0F40 80C8h

Figure 14-7092. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_LO Name Register

31	30	29	28	27	26	25	24
TEST_BUS_LO							
R							
0h							
23	22	21	20	19	18	17	16
TEST_BUS_LO							
R							
0h							
15	14	13	12	11	10	9	8
TEST_BUS_LO							
R							
0h							
7	6	5	4	3	2	1	0
TEST_BUS_LO							
R							
0h							

Table 14-21462. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_BUS_LO	R	0h	Host controller test bus low 32-bits. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.203 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_HI Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_HI Register (Offset = 80CCh) [reset = 0h]

Test Bus High Bits: Host controller test bus high 32 bits. This register is used to read the internal states and other important signals. The host control test bus is gathered from different internal modules for its important states and control/status information. There is a 64-bit register that allows us to read a bus of 64 bits. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21463. Instance Table

Instance Name	Physical Address
USB0	**0F40 80CCh**

Figure 14-7093. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_HI Name Register

31	30	29	28	27	26	25	24
TEST_BUS_HI							
R							
0h							
23	22	21	20	19	18	17	16
TEST_BUS_HI							
R							
0h							
15	14	13	12	11	10	9	8
TEST_BUS_HI							
R							
0h							
7	6	5	4	3	2	1	0
TEST_BUS_HI							
R							
0h							

Table 14-21465. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TEST_BUS_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_BUS_HI	R	0h	Host controller test bus high 32-bits. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.204 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1 Register (Offset = 80D0h) [reset = 4E1BD105h]

Host Control Transfer Manager (TRM) register. This register contains fields, which control the behavior of the Transfer Manager in the xHCI. The functions controlled by this register are made available largely for debug/ diagnostic purposes. This functionality is above and beyond that defined in the xHCI specification. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21466. Instance Table

Instance Name	Physical Address
USB0	0F40 80D0h

Figure 14-7094. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1 Name Register

31	30	29	28	27	26	25	24
TRB_PACE_EN	USB2_NAK_AUTO_DETECT_REG_EN	DISABLE_CPL_SST_MDATA_ERR	DISABLE_CPL_SST_PPIPE_ERR	ENABLE_NOOP_UPD	EP_HALT_2RETRY_EN	TRB_ERR_RMDB_EN	DISABLE_IMD_4NODMA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	1h	0h	0h	1h	1h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WRITE_ERDP_LO	CPL_DB_RANG_EN	DISABLE_ERDY_DROP	DEADLOCK_DETECT_EN	SHORT_ERR_4MSI_EN	NO_OP_AS_TD	PHASE1_IMD_EN	SET_ADDR_ERR_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	1h	1h	0h	1h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ISO_0LEN_LPF_EN	XFER_BLOCK_EN	SINGLE_BURST_EN	ENT_EN	CTRL_REG_CLR_BNDRY	FLUSH_2CLR_VALID_EN	IN_NPKT_PACE_DISABLE	TRB_CACHE_INVALIDE_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	0h	1h	0h	0h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NPKT0_FC_DISABLE	EN_BB_PORT_DISABLE	CPL_PKT_CLR_MASK_EN	XPORT_CRD_DISABLE	DISABLE_STALL	LINK_NOP_SUCCESS_EN	DISABLE_FC_4INRDY	IN_TD_PACE_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	1h

Table 14-21468. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRB_PACE_EN	R/W	0h	Must be set to '0'. Reset Source: rst_mod_g_rst_n
30	USB2_NAK_AUTO_DETECT_REG_EN	R/W	1h	'0': Disables a special function which detects NAK received and goes into a single packet pace mode so that we do not burst ahead. '1': Enables a special function which detects NAK received and goes into a single packet pace mode so that we do not burst ahead. Reset Source: rst_mod_g_rst_n
29	DISABLE_CPL_SST_MDATA_ERR	R/W	0h	'0': Enable the error check. '1': Disable the error check for Data Move stream state. It will generate a transfer event with prime PIPE error completion code if an error is detected. Reset Source: rst_mod_g_rst_n

Table 14-21468. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	DISABLE_CPL_SST_PPIPE_ERR	R/W	0h	'0': Enable the error check, '1': Disable the error check for prime PIPE stream state. It will generate a transfer event with prime PIPE error completion code if an error is detected. Reset Source: rst_mod_g_rst_n
27	ENABLE_NOOP_UPD	R/W	1h	This bit has been modified for its usage since PPT A0. It is used to allow NO-OP TRB to be treated in a same way as link TRB. In other words, it will update the internal context when it is fetched while the internal context cache TRB FIFO is empty. '0': Disable the function, '1': Enable the cache function. Reset Source: rst_mod_g_rst_n
26	EP_HALT_2RETRY_EN	R/W	1h	This is a special internal condition enable for CPL engine which it enables all EP halt conditions detected to cause the proper actions in a response. '0': Disabled, '1': Enabled. Note: Only default condition of '1' is valid. Reset Source: rst_mod_g_rst_n
25	TRB_ERR_RM_DB_EN	R/W	1h	This is a special internal branch condition control in XFER engine which does the EP transfer ring process. When this bit is set a retry condition identified by completion engine will cause XFER engine to stop what it is currently in progress and start over from IDLE state. '0': Disable, '1': Enable the branch condition. Reset Source: rst_mod_g_rst_n
24	DISABLE_IMD_4NODMA	R/W	0h	This is a special internal branch condition control in XFER engine which does the EP transfer ring process. When this bit is set, the XFER will not continue even if the next TRB is identified as a non DMA TRB. The engine will then wait for the next scheduled request for this EP. '0': Disable, '1': Enable the branch condition. Reset Source: rst_mod_g_rst_n
23	WRITE_ERDP_LO	R/W	0h	When ERDP register is updated by software, it is expected as an atomic function since this is a 64-bit register. It is expected, that the ERDP [64-bit register] is updated together when ERDP high 32 is written. We have this bit designed to ignore the atomic operation required from software for ERDP low 32 bits. When this bit is set to '1', it will update the ERDP low 32 bits when software issues a CPU write to the ERDP low 32 bits. '0': not ignore, '1': ignore atomic operation. Reset Source: rst_mod_g_rst_n
22	CPL_DB_RANG_EN	R/W	0h	Setting this bit to '1' will force an internal doorbell ring on the EP that it has received a response. Reset Source: rst_mod_g_rst_n
21	DISABLE_ERDY_DROP	R/W	0h	'0': Drop ERDYs received when not in a flow control state. '1': Do not drop ERDYs received when not in a flow control state. Note: We typically drop unexpected ERDY Reset Source: rst_mod_g_rst_n

Table 14-21468. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DEADLOCK_DETECT_EN	R/W	1h	'0': Disable timeout of TRB error processing. '1': Enable timeout of a TRB processing in few critical states that possibly have a deadlock for unexpected reason. A vendor defined completion code is generated in the event of a timeout during TRB processing. Reset Source: rst_mod_g_rst_n
19	SHORT_ERR_4MSI_EN	R/W	1h	This bit is modified to enable a feature where we can control whether or not to report an event with completion code of Missed Service Error when a short packet response has been received not in the expected service interval. '0': Disable this function so that the xHC engine will report an event with completion code of Short packet indication and another event with MSE at the end of the TD, '1': Enables all completion event that supposedly is short to the MSE. Reset Source: rst_mod_g_rst_n
18	NO_OP_AS_TD	R/W	0h	This bit is modified to enable the NO_OP TRB as a TD when Missing Service Interval Error has encountered. This is only for PPT B0, LPT and CB. '0': disable, '1': enable. Reset Source: rst_mod_g_rst_n
17	PHASE1_IMD_EN	R/W	1h	Enable a special branch condition of the XFER ring process state. This is to ensure that we have a DMA request issued to DMA engine during a PHASE1 process of the TTE. '0': disabled, '1': enabled Reset Source: rst_mod_g_rst_n
16	SET_ADDR_ERR_EN	R/W	1h	'0': Disable error reporting if a SETUP TRB contains the following: bRequest = SET_ADDRES, bmRequestType = [DTD] Host-to-device, Type = Standard, Recipient = Device. '1': Enable error reporting for this case. Reset Source: rst_mod_g_rst_n
15	ISO_0LEN_LPF_EN	R/W	1h	Enables a special internal state branch condition for periodic EP during its transfer ring process. If we have identified that the next TRB is a non DMAnable TRB such as LINK TRB, or Event data TRB, then this bit enables XFER engine to continue process the next TRB as if the ENT bit of the TRB is set. '0': disable, '1': enable. Reset Source: rst_mod_g_rst_n
14	XFER_BLOCK_EN	R/W	1h	Not used. XFER engine has a new function that provides a support to ISO EP within a long PCIe delayed system. The long delay can cause missing service interval while pending response has not all been returned. This bit enables engine to identify a MSI condition and store the context bit for a pending response so that we can process a MSI event when pending response received. '0': disable this function, '1': enable this function. Reset Source: rst_mod_g_rst_n
13	SINGLE_BURST_EN	R/W	0h	'0': Bulk and interrupt endpoints use burst size defined by endpoint context. '1: Force the Bulk and Interrupt endpoints to use a burst size of 1. Reset Source: rst_mod_g_rst_n

Table 14-21468. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ENT_EN	R/W	1h	'0': ENT bit is ignored. '1': ENT bit is processed. The transfer engine will service the next TRB. Reset Source: rst_mod_g_rst_n
11	CTRL_REG_CLR_BNDRY	R/W	0h	Setting this bit to '1' will force the transfer engine to set the packet boundary flag. This flag is an important flag, which may cause a deadlock. This is a safety feature that we have plugged in. Reset Source: rst_mod_g_rst_n
10	FLUSH_2CLR_VALID_EN	R/W	0h	This bit is modified to support PPTB0, LPT and CP for a feature that we will clear the single IN EP array based on ISO flush or short flush. '0': Indicate that we do not need to clear IN EP array based on flush conditions. '1': indicate that we do clear IN EP array based on flush conditions Reset Source: rst_mod_g_rst_n
9	IN_NPKT_PACE_DISABLE	R/W	0h	Setting this bit to '1' will force the transfer engine state machine to exit the CPL_WAIT state. This is designed to avoid unexpected deadlock in CPL_WAIT state. Reset Source: rst_mod_g_rst_n
8	TRB_CACHE_INVALIDE_EN	R/W	1h	'0': Disable internal TRB cache invalidation. '1': Enable internal TRB cache invalidation auto detect function. This will allow engine to handle more than 4 TRBs per packet. Reset Source: rst_mod_g_rst_n
7	NPKT0_FC_DISABLE	R/W	0h	'0': USB3 responses with NumPkts equal to 0 will be treated as a flow control condition. '1': USB3 responses with NumPkts equal to 0 will not be treated as a flow control condition. Reset Source: rst_mod_g_rst_n
6	EN_BB_PORT_DISABLE	R/W	0h	'0': Babble errors will not disable the port. '1': Babble errors will disable the auto detect function This will allow engine to handle more than 4 TRBs per packet. Reset Source: rst_mod_g_rst_n
5	CPL_PKT_CLR_MASK_EN	R/W	0h	Enable a function, which clears a mask of an EP on any response of that EP. '0': Clear the scheduler mask normally, '1': Clear the scheduler mask on each received packet. Reset Source: rst_mod_g_rst_n
4	XPORT_CRD_DISABLE	R/W	0h	This bit is designed to allow XFER engine to do a transfer without checking against the available port credit. '0': Advertises accurate buffer credit information to the scheduler. '1': Advertises non-zero buffer credits to the scheduler [e.g. never backpressure back on buffer credit information] Reset Source: rst_mod_g_rst_n
3	DISABLE_STALL	R/W	0h	'0': Process stalls reported by the DMA engine. '1': Ignore stall response received reported by the DMA engine. Reset Source: rst_mod_g_rst_n
2	LINK_NOP_SUCESS_EN	R/W	1h	'0': Process transaction errors due to CERR count reached or transaction timeout reported by the DMA engine. '1': Ignore transaction errors reported by the DMA engine. Reset Source: rst_mod_g_rst_n
1	DISABLE_FC_4INRDY	R/W	0h	'0': Obey the NPKT0 and EOB flow control. '1': Ignore received flow control for implied NRDY [e.g EOB or NPKT=0] for USB3 only Reset Source: rst_mod_g_rst_n

Table 14-21468. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IN_TD_PACE_ENABLE	R/W	1h	'0': Disable TD pacing for IN endpoint. '1': Enable TD pacing for IN endpoints. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.205 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG1 Register (Offset = 80D4h) [reset = 8100h]

Host Control Scheduler register. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21469. Instance Table

Instance Name	Physical Address
USB0	0F40 80D4h

Figure 14-7095. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG1 Name Register

31	30	29	28	27	26	25	24
SCH_LIMIT_PRDC				SCH_BLOCK_PENDING_EN	SCH_ASYNC_1PKT_SPLIT_PREF	SCH_TT_OVERLAP_ALL_INS	SCH_ASYNC_PRDC_CC_DIS
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SCH_CCLK_PRDC_DONE_CHECK		SCH_STOP_SERVE_NC	TTE_4	DISABLE_GL_HUB_INT_FIX	DISABLE_GL_HUB_ISO_FIX	TTE_3	
R/W		R/W	R/W	R/W	R/W	R/W	
0h		0h	0h	0h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TTE_2	TTE_1	TTE_0	CACHE_SIZE_CTRL		MAXEP		SCRATCH_PAD_EN
R/W	R/W	R/W	R/W		R/W		R/W
1h	0h	0h	0h		0h		1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SCH_ASYNC_1PKT_PERF	SCH_ASYNC_OUT_MAX_PERF	SCH_SORT_PATTERN		TTE_ENABLE_INTROUT_OVERLAP_STOP	SCH_2	TRM_ACTIVE_IN_EP_VALID	POLL_DELAY_DIS
R/W	R/W	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-21471. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	SCH_LIMIT_PRDC	R/W	0h	Host Control Scheduler: sch_limit_prdc Reset Source: rst_mod_g_rst_n
27	SCH_BLOCK_PENDING_EN	R/W	0h	Host Control Scheduler: sch_block_pending_en Reset Source: rst_mod_g_rst_n
26	SCH_ASYNC_1PKT_SPLIT_PREF	R/W	0h	Host Control Scheduler: sch_async_1pkt_split_pref Reset Source: rst_mod_g_rst_n
25	SCH_TT_OVERLAP_ALL_INS	R/W	0h	Host Control Scheduler: sch_tt_overlap_all_ins Reset Source: rst_mod_g_rst_n
24	SCH_ASYNC_PRDC_CC_DIS	R/W	0h	Host Control Scheduler: sch_async_prdc_cc_dis Reset Source: rst_mod_g_rst_n
23:22	SCH_CCLK_PRDC_DONE_CHECK	R/W	0h	Host Control Scheduler: sch_cclk_prdc_done_check Reset Source: rst_mod_g_rst_n

Table 14-21471. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	SCH_STOP_SERVE_NC	R/W	0h	Host Control Scheduler: Enable Stop serving packets to disabled port Reset Source: rst_mod_g_rst_n
20	TTE_4	R/W	0h	TTE: Reserved Reset Source: rst_mod_g_rst_n
19	DISABLE_GL_HUB_INT_FIX	R/W	0h	TTE: disable_gl_hub_int_fix Reset Source: rst_mod_g_rst_n
18	DISABLE_GL_HUB_ISO_FIX	R/W	0h	TTE: disable_gl_hub_iso_fix Reset Source: rst_mod_g_rst_n
17:16	TTE_3	R/W	0h	TTE: Reserved Reset Source: rst_mod_g_rst_n
15	TTE_2	R/W	1h	TTE: Disable split error request to TRM on unserved interrupt-INs Reset Source: rst_mod_g_rst_n
14	TTE_1	R/W	0h	TTE: Disable checking of missed microframes Reset Source: rst_mod_g_rst_n
13	TTE_0	R/W	0h	TTE: Disable interrupt complete split limit to 3 micro frames Reset Source: rst_mod_g_rst_n
12:11	CACHE_SIZE_CTRL	R/W	0h	Command Manager: Context cache enable Reset Source: rst_mod_g_rst_n
10:9	MAXEP	R/W	0h	Command Manager: Allow dynamically setting different max EP allowed. The max EP supported scales with the scratch pad size. This allows driver to allocate small memory sizes if it needed. 0: 32 EPs, 1: 16 EPs, 2: 8 EPs, 3: 4 EPs. Reset Source: rst_mod_g_rst_n
8	SCRATCH_PAD_EN	R/W	1h	Command Manager: Enables scratch pad function Reset Source: rst_mod_g_rst_n
7	SCH_ASYNC_1PKT_PERF	R/W	0h	Host Control Scheduler: Disable burst limit '1' for async in presence of another port periodic packets. Reset Source: rst_mod_g_rst_n
6	SCH_ASYNC_OUT_MAX_PERF	R/W	0h	Host Control Scheduler: Enable maximal out performance [may cause unfairness or short term starvation]. Reset Source: rst_mod_g_rst_n
5:4	SCH_SORT_PATTERN	R/W	0h	Host Control Scheduler: Search priority. Possible values: '00': Sort by Interval then ISO over interrupt, '01','10','11': Experimental sort algorithms. Reset Source: rst_mod_g_rst_n
3	TTE_ENABLE_INTROUT_OVERLAP_STOP	R/W	0h	Host Control Scheduler: tte_enable_introut_overlap_stop Reset Source: rst_mod_g_rst_n
2	SCH_2	R/W	0h	Host Control Scheduler: Disable TTE IN overlap Reset Source: rst_mod_g_rst_n
1	TRM_ACTIVE_IN_EP_VALID	R/W	0h	Host Control Scheduler: Disable TRM active IN EP valid check function Reset Source: rst_mod_g_rst_n

Table 14-21471. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POLL_DELAY_DIS	R/W	0h	Host Control Scheduler: Disable poll delay function Reset Source: rst_mod_g_rst_n

14.9.2.3.2.206 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_ODMA_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_ODMA_REG Register (Offset = 80D8h) [reset = 14003002h]

Host Control ODMA. This register contains a number of fields that provide a specific level of configurability for the OUT DMA Engine in the xHCI. This functionality is above and beyond that defined in the xHCI specification. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21472. Instance Table

Instance Name	Physical Address
USB0	0F40 80D8h

Figure 14-7096. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_ODMA_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_RW							
R/W							
2800h							
23	22	21	20	19	18	17	16
RESERVED_RW							
R/W							
2800h							
15	14	13	12	11	10	9	8
RESERVED_RW	SPEED_UP_TIMEOUT	ACK_CRD_CHECK_EN	EP_BASE_TIMER	ODMA_11	EP_TIMER_TICK	ODMA_9	CLEAR_CNTX_LOCKS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
2800h	0h	1h	1h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ODMA_7	ODMA_SET_ADDR_TO_IDLE	ODMA_COMPLETION_TO_IDLE	ODMA_RESP_TO_IDLE	ODMA_RD_TO_IDLE	EP_TRANS_TIMEOUT_LEN		EP_TRANS_TIMEOUT_EN
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	1h		0h

Table 14-21474. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_ODMA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED_RW	R/W	2800h	Reserved field, RW
14	SPEED_UP_TIMEOUT	R/W	0h	'0': Disable the speed up transaction timeout function. '1': Enable the transaction timeout speed up based on no-connect detected on a particular port Reset Source: rst_mod_g_rst_n
13	ACK_CRD_CHECK_EN	R/W	1h	'0': Disable the ACK credit check function '1': Enable the ACK credit check function that ODMA provides Reset Source: rst_mod_g_rst_n
12	EP_BASE_TIMER	R/W	1h	'0': Employs a 1us EP Transaction Base Timer. Enables a Timeout range from 16us to 64us '1': Employs a 125us EP Transaction Base Timer. Enables a Timeout range from 2ms to 8ms Reset Source: rst_mod_g_rst_n

Table 14-21474. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_ODMA_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ODMA_11	R/W	0h	Setting this field will prohibit the Set Address Finite State Machine Credit Handshake with TTE Logic Reset Source: rst_mod_g_rst_n
10	EP_TIMER_TICK	R/W	0h	Setting this field will disable the EP Transaction Timer function when the Command Manager is performing a Stop Endpoint Command or when the LTSSM is in Recovery Reset Source: rst_mod_g_rst_n
9	ODMA_9	R/W	0h	Setting this field prohibits the Set Address Finite State Machine from being flow controlled when an ACK with NPKT=0 is received in response to the SETUP DP initiated during SET_ADDRESS Reset Source: rst_mod_g_rst_n
8	CLEAR_CNTX_LOCKS	R/W	0h	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines Reset Source: rst_mod_g_rst_n
7	ODMA_7	R/W	0h	Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports Reset Source: rst_mod_g_rst_n
6	ODMA_SET_ADDR_TO_IDLE	R/W	0h	Setting this field generates a pulse that returns the Out DMA Set Address Finite State Machine into the IDLE state Reset Source: rst_mod_g_rst_n
5	ODMA_COMPLETION_TO_IDLE	R/W	0h	Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state Reset Source: rst_mod_g_rst_n
4	ODMA_RESP_TO_IDLE	R/W	0h	Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state. Reset Source: rst_mod_g_rst_n
3	ODMA_RD_TO_IDLE	R/W	0h	Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state. Reset Source: rst_mod_g_rst_n
2:1	EP_TRANS_TIMEOUT_LEN	R/W	1h	Controls the duration of the EP Transaction Timeout [depends on the settings of EP Transaction Base Timer [bit[12]]]. Possible values: 0: 64us [[12]=0] or 8ms [[12]=1] EP Transaction Timeout, 1: 32us [[12]=0] or 4ms [[12]=1] EP Transaction Timeout, 2: 16us [[12]=0] or 2ms [[12]=1] EP Transaction Timeout, 3: EP Transaction Timer is DISABLED. Reset Source: rst_mod_g_rst_n
0	EP_TRANS_TIMEOUT_EN	R/W	0h	'0': Enables the EP Transaction Timeout Function, '1': Disables the EP Transaction Timeout Function Reset Source: rst_mod_g_rst_n

14.9.2.3.2.207 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_IDMA_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_IDMA_REG Register (Offset = 80DCh) [reset = 402h]

Host Control IDMA. This register contains a number of fields that provide a specific level of configurability for the IN DMA Engine in the xHCI. This functionality is above and beyond that defined in the xHCI specification. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21475. Instance Table

Instance Name	Physical Address
USB0	**0F40 80DCh**

Figure 14-7097. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_IDMA_REG Name Register

31	30	29	28	27	26	25	24
EVENT_FIFO_DIS	EVENT_PRIORITY	DB_EVENT_GEN_EN	IDMA_28	IDMA_27	TIMER_TICK1	IDMA_25	IDMA_24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IDMA_23_19					IDMA_ADDR_FIFO_FLUSH_BIT	IDMA_17	IDMA_PTR_BUF_ROOM_SET
R/W					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IDMA_15	IDMA_14	IDMA_13	SPEED_UP_TIMEOUT	SEQ_NUM_ADJ_ON_NRDY	TIMER_TICK0	IDMA_9	COMPLIANCE_ISO_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLEAR_CNTX_LOCKS	DM_PST_CLR_PULSE	ACK_PST_CLR_PULSE	RESTORE_RDP_CREDITS_PULSE	IDMA_PTR_BUF_ROOM_RESTORE_PULSE	EP_TIMER_TICK		EP_TRANS_TIMEOUT_EN
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	1h		0h

Table 14-21477. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_IDMA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT_FIFO_DIS	R/W	0h	Used in Event Manager. '0': Enable single ring optimization, '1': Disable single ring optimization. Reset Source: rst_mod_g_rst_n
30	EVENT_PRIORITY	R/W	0h	Used in Event Manager. '0': CPL Engine priority over XFER Manager, '1': XFER Manager priority over CPL Engine. Reset Source: rst_mod_g_rst_n
29	DB_EVENT_GEN_EN	R/W	0h	Used in Doorbell Manager. '0': Do not generate an event. '1': Enable an event generated with completion code TRB_CMPL_ENDPOINT_NOT_ENABLED_ERR when a doorbell ring on an EP, which has not running or stop state. Reset Source: rst_mod_g_rst_n

Table 14-21477. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_IDMA_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	IDMA_28	R/W	0h	'0': Drop Deferred Ack/Ack TPs. [default] [Bug #5481], '1': Allow Deferred Ack/Ack TPs. Reset Source: rst_mod_g_rst_n
27	IDMA_27	R/W	0h	'0': Drop Deferred Stream Reject TPs. [default] [Bug #5434], '1': Allow Deferred Stream Reject TPs. Reset Source: rst_mod_g_rst_n
26	TIMER_TICK1	R/W	0h	Allows to select the EP Timer Tick to be either the 1us timer tick or the 125us timer tick or the 1ms timer tick or the 4ms timer tick based on the setting of this bit and bit 10 of this register. The encoding is as follows [bit{[26],[10]}]: '00' : 1us EP Timer Tick, '01' : 125us EP Timer Tick, '10' : 1ms EP Timer Tick, '11' : 4ms EP Timer Tick. Reset Source: rst_mod_g_rst_n
25	IDMA_25	R/W	0h	Flush TTE Address FIFO Reset Source: rst_mod_g_rst_n
24	IDMA_24	R/W	0h	'0': Flush an Async Address FIFO, '1': Flush a Periodic Address FIFO. Reset Source: rst_mod_g_rst_n
23:19	IDMA_23_19	R/W	0h	Port Number of Address FIFO to Flush. Reset Source: rst_mod_g_rst_n
18	IDMA_ADDR_FIFO_FLUSH_BIT	R/W	0h	Flush IDMA Address FIFO strobe. Reset Source: rst_mod_g_rst_n
17	IDMA_17	R/W	0h	'0': All ACK ACKs are put in the Periodic Header FIFO in XPPE, '1': Only Periodic ACK ACKs are put in the Periodic Header FIFO in XPPE. Reset Source: rst_mod_g_rst_n
16	IDMA_PTR_BUF_ROOM_SET	R/W	0h	'0': Default IDMA Pointer Buffer Room to 8 : Requires strobe of host_ctrl_idma_reg[3][idma_ptr_buf_room_restore_pulse] to take effect, '1': Default IDMA Pointer Buffer Room to 4 : Requires strobe of host_ctrl_idma_reg[3][idma_ptr_buf_room_restore_pulse] to take effect. Reset Source: rst_mod_g_rst_n
15	IDMA_15	R/W	0h	Disable drop spurious DP when i_npkt==0 Reset Source: rst_mod_g_rst_n
14	IDMA_14	R/W	0h	Disable drop spurious DP when EP is in flow conrtrol. Reset Source: rst_mod_g_rst_n
13	IDMA_13	R/W	0h	Disable dropping all deferred packets on ISO Endpoints. Reset Source: rst_mod_g_rst_n
12	SPEED_UP_TIMEOUT	R/W	0h	'0': Disable the speed up transaction timeout function. '1': Enable the transaction timeout speed up based on no-connect detected on a particular port Reset Source: rst_mod_g_rst_n
11	SEQ_NUM_ADJ_ON_NRDY	R/W	0h	'0': Enable sequence number adjustment on NRDY received for USB3 when we are expecting a response. '1': Enable sequence number adjustment on any NRDY received for USB3. Reset Source: rst_mod_g_rst_n

Table 14-21477. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_IDMA_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TIMER_TICK0	R/W	1h	'0': Employs a 1us EP Transaction Base Timer. Enables a Timeout range from 16us to 64us. '1': Employs a 125us EP Transaction Base Timer. Enables a Timeout range from 2ms to 8ms. Reset Source: rst_mod_g_rst_n
9	IDMA_9	R/W	0h	Setting this field will disable the EP Transaction Timer function when the Command Manager is performing a Stop Endpoint Command or when the LTSSM is in Recovery Reset Source: rst_mod_g_rst_n
8	COMPLIANCE_ISO_ENABLE	R/W	0h	Setting this field enables the Compliance Isochronous mode of operation. It bounds the upper limit on the NPKT field for all ISO Acknowledgments generated from the Host to the value of 2. Reset Source: rst_mod_g_rst_n
7	CLEAR_CNTX_LOCKS	R/W	0h	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the IN DMA Acknowledge and Data Mover Finite State Machines Reset Source: rst_mod_g_rst_n
6	DM_PST_CLR_PULSE	R/W	0h	Setting this field generates a pulse that returns the IN DMA Data Mover Finite State Machine into the IDLE state Reset Source: rst_mod_g_rst_n
5	ACK_PST_CLR_PULSE	R/W	0h	Setting this field generates a pulse that returns the IN DMA Acknowledge Finite State Machine into the IDLE state. Reset Source: rst_mod_g_rst_n
4	RESTORE_RDP_CREDITS_PULSE	R/W	0h	Setting this field generates a pulse that implicitly returns all of the IN DMA Data Packet credits on all ports. Reset Source: rst_mod_g_rst_n
3	IDMA_PTR_BUF_ROOM_RESTORE_PULSE	R/W	0h	Setting this field generates a pulse that clears all the Read and Write Pointers associated with the various DMA Address FIFOs causing them to appear empty Reset Source: rst_mod_g_rst_n
2:1	EP_TIMER_TICK	R/W	1h	'00': 1us/125us/1ms/4ms EP Timer Tick '01': 2us/250us/2ms/8ms EP Timer Tick '10': 4us/500us/4ms/16ms EP Timer Tick '11': Disabled EP Timer Tick Reset Source: rst_mod_g_rst_n
0	EP_TRANS_TIMEOUT_EN	R/W	0h	'0': Enables the EP Transaction Timeout Function, '1': Disables the EP Transaction Timeout Function. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.208 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_CTRL Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_CTRL Register (Offset = 80E0h) [reset = 780Fh]

Global Port Control. Specific control register for port power management etc. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21478. Instance Table

Instance Name	Physical Address
USB0	**0F40 80E0h**

Figure 14-7098. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED_R</td><td>LOCK_HEADER_DATA_EN</td><td>RD_WR_ADDR_CONFLICT_EN</td><td>OVERFLOW_SYS_ERR_EN</td><td>HBUF_WATER_MARK_REG_CCLK</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">HBUF_WATER_MARK_REG_CCLK</td><td>ENABLE_ITP_XMT</td><td>PCIE_GASKET</td><td colspan="2">RESERVED_RW</td><td>TEST_BUS_SEL_CTRL_BITS</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">3h</td><td>1h</td><td>1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">TEST_BUS_SEL_CTRL_BITS</td><td colspan="4">RES1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-21480. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED_R	R	0h	Reserved field, RO
19	LOCK_HEADER_DATA_EN	R/W	0h	lock_header_data_en Reset Source: rst_mod_g_rst_n
18	RD_WR_ADDR_CONFLICT_EN	R/W	0h	rd_wr_addr_conflict_en Reset Source: rst_mod_g_rst_n
17	OVERFLOW_SYS_ERR_EN	R/W	0h	'0': Disable error generation. '1': Enable to generate a host system error when receive buffer overflow on any ports. Reset Source: rst_mod_g_rst_n

Table 14-21480. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16:13	HBUF_WATER_MARK_REG_CCLK	R/W	3h	This 4-bit register is designed as a water mark for when to turn on link FC credit return disable. This is used in xhc_prot_rppe.v for receive buffer management. We have 8 header credit in per port receive buffer. When buffer received enough packets, it will need to disable the link credit FC return in order to balance the processing delay within DMA engine. 0: Always enable link credit FC return, 1-8: Water mark value. Reset Source: rst_mod_g_rst_n
12	ENABLE_ITP_XMT	R/W	1h	Bit[s] of this field are designated to individually control each USB3 port to enable ITP transmission. 0: Do not Transmit any ITP. 1: Transmit ITP Reset Source: rst_mod_g_rst_n
11	PCIE_GASKET	R/W	1h	Reserved to '1'. Note: An internal register bit for PCIe gasket. It is only valid for value of '1' Reset Source: rst_mod_g_rst_n
10:9	RESERVED_RW	R/W	0h	Reserved field, RW
8:4	TEST_BUS_SEL_CTRL_BITS	R/W	0h	Test bus select control bits. 0: Clock, Reset and Power management Debug bus 1: PCIe PIPE Bus, 2: USB3 PIPE Bus, 3: USB2 UTMI Bus, 4: TRM Debug Bus, 5: Scheduler Debug Bus, 6: ODMA Debug Bus, 7: IDMA Debug Bus. Reset Source: rst_mod_g_rst_n
3:0	RES1	R/W	Fh	Reserved to 1 [reserved for PP] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.209 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG Register (Offset = 8100h) [reset = 2917C0F4h]

AUX Reset Control. Reset Control register. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21481. Instance Table

Instance Name	Physical Address
USB0	**0F40 8100h**

Figure 14-7099. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R	PERST_FILTER_DIS	PCIE_PHY_RST_SEL	PERST_2PWDOWN_EN	PERST_4MAIN_EN	IGNORE_PERST_EN	FAST_SIM_RST	IGNORE_LINKDOWN_RST_4UPORT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	0h	1h	0h	0h	1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IGNORE_MAIN_PWRUP_2USB_PHY	COLD_RST_N_PULSE	IGNORE_HCRESET_4USB2	IGNORE_HC_WARM_RST_4UPHY_PON	IGNORE_MAIN_PWRUP_HC_2PCORE	EEPROM_LOAD_ON_MAIN	IGNORE_HC_RST_2PCIE_PHY	IGNORE_MAC_PHY_PIPE_RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	1h	0h	1h	1h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IGNORE_WARM_RST_4UPHY_PON	PCIE_LINKDOWN_RST_EN	IGNORE_HOT_RST_4U3PORT	IGNORE_WARM_RST_4U3PORT	IGNORE_MAIN_PWRUP_4U3PORT	IGNORE_MAIN_PWRUP_4U2PORT	IGNORE_MAIN_PWRUP_2PCORE	IGNORE_MAIN_PWRUP_2PCIE_PHY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IGNORE_HC_WARM_RST_2USB_PHY	IGNORE_WARM_RST_2USB_PHY	IGNORE_MAIN_PWRUP_RST	PM_CTRL_MAIN_RST_EN	IGNORE_PERST_4MAIN_PWRUP	IGNORE_PERST_4FD_RST	FORCE_FD_RST	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1h	1h	1h	1h	0h	1h	0h	

Table 14-21483. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_R	R	0h	Reserved field, RO This field should not be modified by software.
30	PERST_FILTER_DIS	R/W	0h	reserved. perst_filter_dis This field should not be modified by software. Reset Source: rst_mod_g_rst_n
29	PCIE_PHY_RST_SEL	R/W	1h	This bit enables AUX reset control module to assert the pcie_phy_reset either from PIPE reset or from Aux power up reset only. The pcie_phy_reset is an internal signal for CB PHY only. '0': Aux PowerUp Reset, '1': PIPE PHY reset This field should not be modified by software. Reset Source: rst_mod_g_rst_n

Table 14-21483. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	PERST_2PWDOWN_EN	R/W	0h	This bit enables the AUX PM control module to assert mac_phy_powerdown state to P1 as soon as PERST# is deasserted. If disabled, then the AUX PM control state will follow its nature cause to determine the power down states for PIPE. '0': disabled, '1': enabled. This field should not be modified by software. Reset Source: rst_mod_g_rst_n
27	PERST_4MAIN_EN	R/W	1h	This bit enables the internal reset control module to immediately start a reset assertion process when PERST# is deasserted without waiting for PCIe device is out of D3 state. This is for warm reboot only. The PERST# can still have impact as a reset if the xHC is in D3 and allow PERST# as a powerup reset bit set. '0: disabled '1: enabled PERST# as an immediately reset This field should not be modified by software. Reset Source: rst_mod_g_rst_n
26	IGNORE_PERST_EN	R/W	0h	This bit disables the PERST# to cause an internal reset. '0: enable '1: disable the PERST# This field should not be modified by software. Reset Source: rst_mod_g_rst_n
25	FAST_SIM_RST	R/W	0h	This bit enables a speed up function or AUX reset at startup. Normally we wait for 20ms after AUX power level has reached. When in speed up mode, we wait only around 3-4us. '0: Disabled, '1: Enabled for fast sim. This field should not be modified by software. Reset Source: rst_mod_g_rst_n
24	IGNORE_LINKDOWN_RST_4UPORT	R/W	1h	When set to '1' ignore a port reset that is caused by a USB port link went down. This field should not be modified by software. Reset Source: rst_mod_g_rst_n
23	IGNORE_MAIN_PWRUP_2USB_PHY	R/W	0h	When set to '1' ignore main powerup reset to USB PHY PIPE reset This field should not be modified by software. Reset Source: rst_mod_g_rst_n
22	COLD_RST_N_PULSE	R/W	0h	When set to '1' allow software to fire a cold reset to USB port logic This field should not be modified by software. Reset Source: rst_mod_g_rst_n
21	IGNORE_HCRESET_4USB2	R/W	0h	When set to '1' ignore HC reset to reset the USB2 Port logic This field should not be modified by software. Reset Source: rst_mod_g_rst_n
20	IGNORE_HC_WARM_RST_4UPHY_PON	R/W	1h	When set to '1' ignore HC reset to the USB PHY power-on reset This field should not be modified by software. Reset Source: rst_mod_g_rst_n
19	IGNORE_MAIN_PWRUP_HC_2PCORE	R/W	0h	When set to '1' enable the HC liked reset caused by PCIe link down condition detected. If PCIe link down detected, a link down reset will always be fired to PCIe core. This field should not be modified by software. Reset Source: rst_mod_g_rst_n
18	EEPROM_LOAD_ON_MAIN	R/W	1h	When set to '1' enable EEPROM reload on every main power-up This field should not be modified by software. Reset Source: rst_mod_g_rst_n

Table 14-21483. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	IGNORE_HC_RST_2PCIE_PHY	R/W	1h	When set to '1' ignore HC reset to the PCIe PHY PIPE reset This field should not be modified by software. Reset Source: rst_mod_g_rst_n
16	IGNORE_MAC_PHY_PIPE_RST	R/W	1h	When set to '1' ignore the LTSSM of USB link state transition caused reset to USB PHY PIPE reset This field should not be modified by software. Reset Source: rst_mod_g_rst_n
15	IGNORE_WARM_RST_4UPHY_PON	R/W	1h	When set to '1' ignore warm reset of the portSC to the USB PHY power on reset This field should not be modified by software. Reset Source: rst_mod_g_rst_n
14	PCIE_LINKDOWN_RST_EN	R/W	1h	When set to '1' allow PCIe link down to cause a reset to the rest of the core as the HC reset would. This field should not be modified by software. Reset Source: rst_mod_g_rst_n
13	IGNORE_HOT_RST_4U3PORT	R/W	0h	When set to '1' ignore hot reset to the USB3 port logic This field should not be modified by software. Reset Source: rst_mod_g_rst_n
12	IGNORE_WARM_RST_4U3PORT	R/W	0h	When set to '1' ignore warm reset to the USB3 port logic This field should not be modified by software. Reset Source: rst_mod_g_rst_n
11	IGNORE_MAIN_PWRUP_4U3PORT	R/W	0h	When set to '1' ignore main power up reset to USB3 port logic This field should not be modified by software. Reset Source: rst_mod_g_rst_n
10	IGNORE_MAIN_PWRUP_4U2PORT	R/W	0h	When set to '1' ignore main power up reset to USB2 port logic This field should not be modified by software. Reset Source: rst_mod_g_rst_n
9	IGNORE_MAIN_PWRUP_2PCORE	R/W	0h	When set to '1' ignore main power up reset to PCIe core This field should not be modified by software. Reset Source: rst_mod_g_rst_n
8	IGNORE_MAIN_PWRUP_2PCIE_PHY	R/W	0h	When set to '1' ignore main power up reset to PCIe PHY This field should not be modified by software. Reset Source: rst_mod_g_rst_n
7	IGNORE_HC_WARM_RST_2USB_PHY	R/W	1h	When set to '1' ignore HC reset to the USB PHY This field should not be modified by software. Reset Source: rst_mod_g_rst_n
6	IGNORE_WARM_RST_2USB_PHY	R/W	1h	When set to '1' ignore warm reset to the USB PHY This field should not be modified by software. Reset Source: rst_mod_g_rst_n
5	IGNORE_MAIN_PWRUP_RST	R/W	1h	When set to '1', it enables the reset isolation function that we have added during HC reset or Per port reset. This field should not be modified by software. Reset Source: rst_mod_g_rst_n
4	PM_CTRL_MAIN_RST_EN	R/W	1h	When set to '1' allow main power off condition to trigger a main power domain reset This field should not be modified by software. Reset Source: rst_mod_g_rst_n
3	IGNORE_PERST_4MAIN_PWRUP	R/W	0h	When set to '1' ignore waiting for PERST# deassertion during main power show down. This field should not be modified by software. Reset Source: rst_mod_g_rst_n

Table 14-21483. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	IGNORE_PERST_4FD_RST	R/W	1h	When fundamental reset is asserted during AUX power up, if this bit is set, then we will ignore PERST# such that purely wait for timeout to deassert fundamental reset. This field should not be modified by software. Reset Source: rst_mod_g_rst_n
1:0	FORCE_FD_RST	R/W	0h	Writing to this field a value of 2'b11 will cause a fundamental reset. The only valid write values are 2'b11 or 2'b00 This field should not be modified by software. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.210 USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SS_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SS_REG Register (Offset = 8104h) [reset = 4A4008h]

Super Speed Bandwidth Overload. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21484. Instance Table

Instance Name	Physical Address
USB0	**0F40 8104h**

Figure 14-7100. USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SS_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MAX_TT_BW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4A4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAX_TT_BW</td><td colspan="4">SS_BW_CALC</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">4A4h</td><td colspan="4">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SS_BW_CALC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">8h</td></tr>
</table>

Table 14-21486. USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:12	MAX_TT_BW	R/W	4A4h	Max. TT BW allowed. See white paper Reset Source: rst_mod_g_rst_n
11:0	SS_BW_CALC	R/W	8h	BW calculation: Overhead per packet for SS BW calculations. See white paper. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.211 USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_HS_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_HS_REG Register (Offset = 8108h) [reset = 1A01Fh]

High Speed TT Bandwidth Overload. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21487. Instance Table

Instance Name	Physical Address
USB0	**0F40 8108h**

Figure 14-7101. USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_HS_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BW_OV_HS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BW_OV_HS</td><td colspan="4">BW_OV_HS_TT</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">1Ah</td><td colspan="4">1Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BW_OV_HS_TT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1Fh</td></tr>
</table>

Table 14-21489. USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_HS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:12	BW_OV_HS	R/W	1Ah	BW calculation: Overhead per packet for HS-TT BW calculations. See white paper. Reset Source: rst_mod_g_rst_n
11:0	BW_OV_HS_TT	R/W	1Fh	BW calculation: Overhead per packet for HS BW calculations. See white paper. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.212 USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_FS_LS_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_FS_LS_REG Register (Offset = 810Ch) [reset = 14080h]

Bandwidth Overload Full and Low Speed. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21490. Instance Table

Instance Name	Physical Address
USB0	**0F40 810Ch**

Figure 14-7102. USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_FS_LS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
FS_BW_CALC							
R/W							
14h							
15	14	13	12	11	10	9	8
FS_BW_CALC				LS_BW_CALC			
R/W				R/W			
14h				80h			
7	6	5	4	3	2	1	0
LS_BW_CALC							
R/W							
80h							

Table 14-21492. USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_FS_LS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:12	FS_BW_CALC	R/W	14h	BW calculation: Overhead per packet for FS BW calculations. See white paper. Reset Source: rst_mod_g_rst_n
11:0	LS_BW_CALC	R/W	80h	BW calculation: Overhead per packet for LS BW calculations. See white paper. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.213 USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SYS_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SYS_REG Register (Offset = 8110h) [reset = 32010h]

System Bandwidth Overload. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21493. Instance Table

Instance Name	Physical Address
USB0	**0F40 8110h**

Figure 14-7103. USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SYS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
BW_OV_SYS_TT							
R/W							
32h							
15	14	13	12	11	10	9	8
BW_OV_SYS_TT				SYS_BW_CALC			
R/W				R/W			
32h				10h			
7	6	5	4	3	2	1	0
SYS_BW_CALC							
R/W							
10h							

Table 14-21495. USB3P0SS_CTRL_XHCI_XECP_HOST_BW_OV_SYS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:12	BW_OV_SYS_TT	R/W	32h	BW calculation: Overhead per TT packet for System BW calculations. See white paper. Reset Source: rst_mod_g_rst_n
11:0	SYS_BW_CALC	R/W	10h	BW calculation: Overhead per packet for System BW calculations. See white paper. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.214 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_ASYNC_DELAY_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_ASYNC_DELAY_REG Register (Offset = 8114h) [reset = 0h]

Scheduler Async Delay. Global defaults for inserting delays between packets in the scheduler for asynchronous types. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21496. Instance Table

Instance Name	Physical Address
USB0	**0F40 8114h**

Figure 14-7104. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_ASYNC_DELAY_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED_R</td><td>HS_BULK_DELAY_EN</td><td colspan="3">HS_BULK_DELAY_DEF</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>FS_BULK_DELAY_EN</td><td colspan="3">FS_BULK_DELAY_DEF</td><td>HS_CTRL_DELAY_EN</td><td colspan="3">HS_CTRL_DELAY_DEF</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>FS_CTRL_DELAY_EN</td><td colspan="3">FS_CTRL_DELAY_DEF</td><td>LS_CTRL_DELAY_EN</td><td colspan="3">LS_CTRL_DELAY_DEF</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-21498. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_ASYNC_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED_R	R	0h	Reserved field, RO
19	HS_BULK_DELAY_EN	R/W	0h	High-Speed Bulk Delay Enable Reset Source: rst_mod_g_rst_n
18:16	HS_BULK_DELAY_DEF	R/W	0h	High-Speed Bulk Delay Default [0=125us,1=250us,2=500us,3=1ms,] Reset Source: rst_mod_g_rst_n
15	FS_BULK_DELAY_EN	R/W	0h	Full-Speed Bulk Delay Enable Reset Source: rst_mod_g_rst_n
14:12	FS_BULK_DELAY_DEF	R/W	0h	Full-Speed Bulk Delay Default [0=125us,1=250us,2=500us,3=1ms,] Reset Source: rst_mod_g_rst_n
11	HS_CTRL_DELAY_EN	R/W	0h	High-Speed Control Delay Enable Reset Source: rst_mod_g_rst_n

Table 14-21498. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_ASYNC_DELAY_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	HS_CTRL_DELAY_DEF	R/W	0h	High-Speed Control Delay Default [0=125us,1=250us,2=500us,3=1ms,] Reset Source: rst_mod_g_rst_n
7	FS_CTRL_DELAY_EN	R/W	0h	Full-Speed Control Delay Enable Reset Source: rst_mod_g_rst_n
6:4	FS_CTRL_DELAY_DEF	R/W	0h	Full-Speed Control Default [0=125us,1=250us,2=500us,3=1ms,] Reset Source: rst_mod_g_rst_n
3	LS_CTRL_DELAY_EN	R/W	0h	Low-Speed Control Delay Enable Reset Source: rst_mod_g_rst_n
2:0	LS_CTRL_DELAY_DEF	R/W	0h	Low-Speed Control Delay Default [0=125us,1=250us,2=500us,3=1ms,] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.215 USB3P0SS_CTRL_XHCI_XECP_UPORTS_PON_RST_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_UPORTS_PON_RST_REG Register (Offset = 8118h) [reset = 0h]

AUX Power PHY Reset. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. Allow a USB PHY reset being issued by software. Writing to this register with bit set to 1 will reset the USB PHY that is connected to the port. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21499. Instance Table

Instance Name	Physical Address
USB0	**0F40 8118h**

Figure 14-7105. USB3P0SS_CTRL_XHCI_XECP_UPORTS_PON_RST_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_R				USB_PHY_PORT_NUM			
R				W			
0h				0h			

Table 14-21501. USB3P0SS_CTRL_XHCI_XECP_UPORTS_PON_RST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_R	R	0h	Reserved field, RO
3:0	USB_PHY_PORT_NUM	W	0h	Indicates the port number of the USB PHY Reset Source: rst_mod_g_rst_n

14.9.2.3.2.216 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG3 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG3 Register (Offset = 811Ch) [reset = E7h]

Host Control Transfer Manager (TRM) register. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21502. Instance Table

Instance Name	Physical Address
USB0	**0F40 811Ch**

Figure 14-7106. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_RW							CPL_EXTRA_DB_RANG_EN
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
CFG_EN_MISS_DOUBLE	CFG_EN_DEFER_BC	CFG_EN_LOOK_POS		CFG_CACHE_DEBUG	CFG_EN_HIT_INVALID	CFG_EN_LOOKAHEAD	CFG_EN_CACHE
R/W	R/W	R/W		R/W	R/W	R/W	R/W
1h	1h	2h		0h	1h	1h	1h

Table 14-21504. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_R	R	0h	Reserved field, RO
15:9	RESERVED_RW	R/W	0h	Reserved field, RW
8	CPL_EXTRA_DB_RANG_EN	R/W	0h	cpl_extra_db_rang_en Reset Source: rst_mod_g_rst_n
7	CFG_EN_MISS_DOUBLE	R/W	1h	'0': Do not enable cache control to double fetch on miss. '1': Enable cache control to double fetch on miss. Reset Source: rst_mod_g_rst_n
6	CFG_EN_DEFER_BC	R/W	1h	'0': Disable cache control to defer misses on bulk/control EPs. '1': Enable cache control to defer misses on bulk/control EPs. Reset Source: rst_mod_g_rst_n
5:4	CFG_EN_LOOK_POS	R/W	2h	Enable cache control trigger position lookahead. Reset Source: rst_mod_g_rst_n
3	CFG_CACHE_DEBUG	R/W	0h	cfg_cache_debug. Available when TRB_CACHE_DEBUG_EN is defined Reset Source: rst_mod_g_rst_n

Table 14-21504. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CFG_EN_HIT_INVALID	R/W	1h	'0': Disable cache control hit invalid with invalid CS, '1': Enable cache control hit invalid with invalid CS. Reset Source: rst_mod_g_rst_n
1	CFG_EN_LOOKAHEAD	R/W	1h	'0': Disable cache control lookahead, '1': Enable cache control lookahead. Reset Source: rst_mod_g_rst_n
0	CFG_EN_CACHE	R/W	1h	'0': Disable cache control, '1': Enable cache control. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.217 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG1 Register (Offset = 8120h) [reset = 808C39A0h]

AUX Power Management Control 1. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21505. Instance Table

Instance Name	Physical Address
USB0	0F40 8120h

Figure 14-7107. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG1 Name Register

31	30	29	28	27	26	25	24
D3_HOT_PME_EN	LOW_PWR_CCLK_GATE_EN	EXTEND_PHYSTATUS_EN	DIRECT_RATE_PASS_EN	USE_PERST_4FD_RST	POWERDOWN_P1_EN	SET_SSV_EN	CLR_SSV_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SR_CMD_SAVE_EN	RESERVEDRW	CLR_SAVE_FLAG	CFG_PCIE_TXREG_PD	CFG_IOB_DRIVESTRENGTH		CFG_USB_P2_EN	CFG_CLK_GATE_DIS
R/W	R/W	R/W	R/W	R/W		R/W	R/W
1h	0h	0h	0h	3h		0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CFG_RXDET_P3_EN	CFG_PIPE_RST_EN	ELECIDLE_MASK_EN	PME_STATUS_EN	ISOLATION_EN	NEW_OW_EN	CCLK_GATE_DISABLE	PHYSTATUS_FALL_TIMEOUT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	0h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IGNORE_AUX_PME_EN	P2_OVERWRITE_P1_EN	ENABLE_P2_ENTER	PM_STATE				FORCE_PM_STATE
R/W	R/W	R/W	R/W				R/W
1h	0h	1h	0h				0h

Table 14-21507. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	D3_HOT_PME_EN	R/W	1h	d3_hot_pme_en Reset Source: rst_mod_g_rst_n
30	LOW_PWR_CCLK_GATE_EN	R/W	0h	This bit enables gate-off the core clock when AUX PM control is in low power state. '0': disable this function, '1': enabled to gate off the core clock. Reset Source: rst_mod_g_rst_n
29	EXTEND_PHYSTATUS_EN	R/W	0h	This bit is there for a bug fix where we need to ensure that phystatus did not get lost during the rate change where clock switch logic takes some cycles to complete. such that the PCie's core clock is at half of the PCIe PHY pclk. '0': not extended phystatus, '1': extended phystatus assertion Reset Source: rst_mod_g_rst_n

Table 14-21507. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	DIRECT_RATE_PASS_EN	R/W	0h	Disable the overwrite function in AUX PM control module for its initiated rate change. '0': allows AUX PM control module to initiate its PCIE rate change when it needs to enable P2 overwrite P1 function. '1': AUX PM control module will not alter the PCIe rate change function . Reset Source: rst_mod_g_rst_n
27	USE_PERST_4FD_RST	R/W	0h	Enable AUX reset module to treat every PERST# as a fundamental reset '0': disabled, '1': enabled. This field should not be modified by software Reset Source: rst_mod_g_rst_n
26	POWERDOWN_P1_EN	R/W	0h	This is a test/control bit. This bit is designed to control the lowest powerdown state of the PCIe that AUX PM module signaled to PIPE is P1. '0': drive as normal operation. '1': always drive to P1 instead of P2 Reset Source: rst_mod_g_rst_n
25	SET_SSV_EN	R/W	0h	When set to '1' set the SSV flag. Reset Source: rst_mod_g_rst_n
24	CLR_SSV_EN	R/W	0h	When set to '1' clear the SSV flag Reset Source: rst_mod_g_rst_n
23	SR_CMD_SAVE_EN	R/W	1h	A debug control bit, which is used to enable save'n'restore function. '0': disabled. '1': enabled Reset Source: rst_mod_g_rst_n
22	RESERVEDRW	R/W	0h	reserved, RW
21	CLR_SAVE_FLAG	R/W	0h	This bit sets the internal save_restore_enable flag to '0' when written to '1'. Software is expected to clear this bit after it wrote this bit to '1'. This is for test/debug purpose of the save'n'restore function. '0': allows regular save'n'restore function to proceed. '1': clear the internal flag save_restore_enable Reset Source: rst_mod_g_rst_n
20	CFG_PCIE_TXREG_PD	R/W	0h	cfg_pcie_txreg_pd Reset Source: rst_mod_g_rst_n
19:18	CFG_IOB_DRIVESTRENGTH	R/W	3h	Controls the drive strength of the IO buffer. Set default IO Strength to 8ma Reset Source: rst_mod_g_rst_n
17	CFG_USB_P2_EN	R/W	0h	Cfg_Usb_p2_en Reset Source: rst_mod_g_rst_n
16	CFG_CLK_GATE_DIS	R/W	0h	Cfg_clk_gate_dis Reset Source: rst_mod_g_rst_n
15	CFG_RXDET_P3_EN	R/W	0h	Cfg_rxdet_p3_en. Enable rxdet U3 mode Reset Source: rst_mod_g_rst_n
14	CFG_PIPE_RST_EN	R/W	0h	Cfg_pipe_rst_en_sync. Reset Source: rst_mod_g_rst_n

Table 14-21507. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ELECIDLE_MASK_EN	R/W	1h	This bit enables the AUX PM control state machine to take over txelecidle signal of the PIPE during several special conditions. '0': Disable the mask. '1': Allow mask to mac_phy_txeleidle of PCIe core. Reset Source: rst_mod_g_rst_n
12	PME_STATUS_EN	R/W	1h	This bit enables the PCIe status function. '0': xHC as a PCIe device will not generate any PME nor report PME status. '1': xHC as a PCIe device will generate the PME message. Reset Source: rst_mod_g_rst_n
11	ISOLATION_EN	R/W	1h	When set to '1' enable isolation function for dual power zone. This field should not be modified by software Reset Source: rst_mod_g_rst_n
10	NEW_OW_EN	R/W	0h	This bit allows the AUX PM control module to decide whether we entered into P2 overwrite condition based on the power down state of the PCIe core is at P1 or the LTSSM of PCIe core is in L1. What we used to have is based on P1 of the PCIe core mac_phy_powerdown signal. This is not correct because LTSSM can be in RX detect to result a P1 of power down state. To preserve our old function, we add this chicken bit. '0': P2Pverwrite function based on PCIe core PIPE mac_phy_powerdown is in P1, '1': P2OverWrite function based on LTSSM in L1 This field should not be modified by software Reset Source: rst_mod_g_rst_n
9	CCLK_GATE_DISABLE	R/W	0h	When set to '1' disable core clock gating based on low power state entered. Reset Source: rst_mod_g_rst_n
8	PHYSTATUS_FALL_TIMEOUT_EN	R/W	1h	When set to '1' enable PHY status timeout function, which is designed to cover the PCIePHY issue that we may have not be able to detect the PHY status toggle. This is a safety feature in case we have gotten into a deadlock during PHY status acknowledgement. Reset Source: rst_mod_g_rst_n
7	IGNORE_AUX_PME_EN	R/W	1h	When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support Reset Source: rst_mod_g_rst_n
6	P2_OVERWRITE_P1_EN	R/W	0h	When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state. Reset Source: rst_mod_g_rst_n
5	ENABLE_P2_ENTER	R/W	1h	When set to '1' enables the remote wake function by allowing P2 clock/switching and P2 entering Reset Source: rst_mod_g_rst_n

Table 14-21507. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:1	PM_STATE	R/W	0h	Forced power management state can be set here. States encoding: PM_ACTIVE : 4'h0. REQ_CLK_SWITCH_2AUX : 4'h1. DRIVE_PHY_2P2 : 4'h2. WAIT_4WAKE : 4'h3. WAIT_4PERST_DSRT : 4'h4. RATE_CHANGE_2FAST : 4'h5. REQ_CLK_SWITCH_2PCLK : 4'h6. PM_EXIT : 4'h7. WAIT_4PCLK : 4'h8. DRIVE_PHY_STATUS : 4'h9. PM_IDLE : 4'hA. PWRUP_REQ_CLK_SWITCH_2PCLK : 4'hB. RATE_CHANGE_2SLOW : 4'hC. WAIT_4LTSSM_WAIT_DONE : 4'hD. WAIT_4CLK_GATE : 4'hE. IN_P2_TIMEOUT : 4'hF. Those bits have also another functionality: [1]: always_wake_n_en, [2]: timeout_16ms_en, [3]: always_force_clk_sw_en, ![4]: rc_p2_exit_en Reset Source: rst_mod_g_rst_n
0	FORCE_PM_STATE	R/W	0h	When set to '1' force PM state to go to the state indicated in field pm_state [bits [4:1]]. This bit is the force PM state register, it is a pulse only [read by software will always give '0'] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.218 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_WATERMARK_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_WATERMARK_REG Register (Offset = 8128h) [reset = 800080h]

Port Watermark. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21508. Instance Table

Instance Name	Physical Address
USB0	**0F40 8128h**

Figure 14-7108. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
RBUF_WATER_MARK							
R/W							
80h							
23	22	21	20	19	18	17	16
RBUF_WATER_MARK							
R/W							
80h							
15	14	13	12	11	10	9	8
XBUF_WATER_MARK							
R/W							
80h							
7	6	5	4	3	2	1	0
XBUF_WATER_MARK							
R/W							
80h							

Table 14-21510. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RBUF_WATER_MARK	R/W	80h	RBUF water mark Reset Source: rst_mod_g_rst_n
15:0	XBUF_WATER_MARK	R/W	80h	XBUF water mark Reset Source: rst_mod_g_rst_n

14.9.2.3.2.219 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG Register (Offset = 812Ch) [reset = 18030C10h]

SuperSpeed Port Link Control. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21511. Instance Table

Instance Name	Physical Address
USB0	**0F40 812Ch**

Figure 14-7109. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG Name Register

31	30	29	28	27	26	25	24
FORCE_LTSSM_STATE					FORCE_LTSSM	FORCE_LTSSM_U0	FORCE_COMP_PATTERN
R/W					R/W	R/W	R/W
3h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FORCE_COMP_PATTERN			LINK_ERR_CNT_SLV_EN	DBG_MODE_SEL			CFG_LOWPOWER_LATENCY
R/W			R/W	R/W			R/W
0h			0h	1h			2h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CFG_LOWPOWER_LATENCY	CFG_NORM_RECOV_VAL			CFG_U3_RECOV_VAL			CFG_FORCE_PM_ACCEPT
R/W	R/W			R/W			R/W
2h	0h			6h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CFG_RECOVERY	CFG_FAST_TRAINING	CFG_DIS_SCRMB	CFG_SYMBOL_ERR_EN	CFG_U2_ENABLE	CFG_U1_ENABLE	CFG_LPBK_MODE	CFG_DIS_COMP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	1h	0h	0h	0h	0h

Table 14-21513. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	FORCE_LTSSM_STATE	R/W	3h	LTSSM state to be forced. This value is for test purpose only. Setting bit 4 enables: cfg_relax_rxpolarity_en. Setting bit 3 enables: cfg_relax_linkfunc_en. Setting bit 2 enables: cfg_link_func_en. Reset Source: rst_mod_g_rst_n
26	FORCE_LTSSM	R/W	0h	'0': Normal operation mode, '1': Direct link to a specific state specified by force_ltssm_state field [bits [31:27]]. This bit is for test purpose only. It shall be written '0' in normal operation mode. Reset Source: rst_mod_g_rst_n

Table 14-21513. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	FORCE_LTSSM_U0	R/W	0h	'0': Normal operation mode, '1': Direct link to U0 This bit is for test purpose only. It shall be written '0' in normal operation mode. Reset Source: rst_mod_g_rst_n
24:21	FORCE_COMP_PATTERN	R/W	0h	Compliance pattern to be forced to enter compliance mode. This value is for test purpose only. Reset Source: rst_mod_g_rst_n
20	LINK_ERR_CNT_SLV_EN	R/W	0h	link_err_cnt_slv_en Reset Source: rst_mod_g_rst_n
19:17	DBG_MODE_SEL	R/W	1h	Debug mode select: bit[0]: cfg_port_init_ctrl [if set to '1' tPortConfiguration less than 21us], bit[1]: cfg_relax_ts2_en, bit[2]: cfg_relax_lfps_en. Reset Source: rst_mod_g_rst_n
16:15	CFG_LOWPOWER_LATENCY	R/W	2h	cfg_lowpower_latency Reset Source: rst_mod_g_rst_n
14:12	CFG_NORM_RECOV_VAL	R/W	0h	This value defines the minimum time for the link to stay in Recovery. Active other than from U3. The granuity is 128us. Reset Source: rst_mod_g_rst_n
11:9	CFG_U3_RECOV_VAL	R/W	6h	This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us. Reset Source: rst_mod_g_rst_n
8	CFG_FORCE_PM_ACCEPT	R/W	0h	'0': Normal operation mode. '1': Force link to accept power management command. Reset Source: rst_mod_g_rst_n
7	CFG_RECOVERY	R/W	0h	'0': Normal operation mode, '1': Direct link to Recovery from U0. Reset Source: rst_mod_g_rst_n
6	CFG_FAST_TRAINING	R/W	0h	'0': Normal operation mode, '1': Link fast training mode. This bit should be written '0' in normal operation. Reset Source: rst_mod_g_rst_n
5	CFG_DIS_SCRMB	R/W	0h	'0': Enable link scrambler, '1': Disable link scrambler. Reset Source: rst_mod_g_rst_n
4	CFG_SYMBOL_ERR_EN	R/W	1h	'0': Disable detecting RxData error using RxStatus signal, '1': Enable detecting RxData error using RxStatus signal. Reset Source: rst_mod_g_rst_n
3	CFG_U2_ENABLE	R/W	0h	'0': Normal operation mode, '1': Direct link to U2 from U0. This bit is for test purpose only. It shall be written '0' in normal operation mode. Reset Source: rst_mod_g_rst_n
2	CFG_U1_ENABLE	R/W	0h	'0': Normal operation mode, '1': Direct link to U1 from U0. This bit is for test purpose only. It shall be written '0' in normal operation mode. Reset Source: rst_mod_g_rst_n

Table 14-21513. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CFG_LPBK_MODE	R/W	0h	'0': Disable link loopback master mode, '1': Enable link loopback master mode. Reset Source: rst_mod_g_rst_n
0	CFG_DIS_COMP	R/W	0h	'0': Enable link compliance mode, '1': Disable link compliance mode. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.220 USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG1 Register (Offset = 8130h) [reset = 311803A0h]

USB2 Port Link Control 1,2,3,4. This set of registers is used to control the USB set of timers. They are spread over 4 registers each 32 bits wide. This set of registers may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21514. Instance Table

Instance Name	Physical Address
USB0	**0F40 8130h**

Figure 14-7110. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG1 Name Register

31	30	29	28	27	26	25	24
TIMER_DISCONNECT_DETECT_LO							
R/W							
31h							
23	22	21	20	19	18	17	16
USB2_PM_DEBUG	USB2_PM_DEBUG_LATENCY_TOL_MSG	USB2_PM_DEBUG_RESUME_DEB_DIS	USB2_PM_DEBUG_HW_LPM_ERRATA	USB2_PM_DEBUG_HW_LPM_ERRATA1	USB2_PM_DEBUG_ENABLE_FLUSH_TO	USB2_PM_DEBUG_EOP_DETECT	USB2_PM_DEBUG_FORCE_FULL_SPEED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	1h	1h	0h	0h	0h
15	14	13	12	11	10	9	8
USB2_PM_DEBUG_SPLIT_192_LIMITDIS	USB2_PM_DEBUG_FS_LS_EXT_DISCON	USB2_PM_DEBUG_UTMIRST2	USB2_PM_DEBUG_UTMIRST1	USB2_PM_DEBUG_ENABLE_DISC_WIN	USB2_PM_DEBUG_DIS_PORT_ERR	USB2_PM_DEBUG_DIS_ISO_PEEK	USB2_PM_DEBUG_DIRECT_RESUME
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h
7	6	5	4	3	2	1	0
USB2_PM_DEBUG_DROPPING	USB2_PM_DEBUG_FORCEPING	USB2_PM_DEBUG_AUTOPING	USB2_PM_DEBUG_PHY_SUSDISALL	USB2_PM_DEBUG_PHY_CLKGATEDIS	USB2_PM_DEBUG_PHY_RSTDISCON	USB2_PM_DEBUG_PHY_RST	USB2_PM_DEBUG_QUICK_SIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	0h	0h	0h	0h

Table 14-21516. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TIMER_DISCONNECT_DETECT_LO	R/W	31h	Number of microseconds of SE0 in FS/LS mode to register disconnect had occurred. First 8 MSB. Reset Source: rst_mod_g_rst_n
23	USB2_PM_DEBUG	R/W	0h	USB2_PM_DEBUG. usb2_link_mgr_debug register. Reset Source: rst_mod_g_rst_n
22	USB2_PM_DEBUG_LATENCY_TOL_MSG	R/W	0h	Latency Tolerance Scheme ['0'=when HWLPM is enabled / '1'=when L1 is active]. Reset Source: rst_mod_g_rst_n
21	USB2_PM_DEBUG_RESUME_DEB_DIS	R/W	0h	Clr to eliminate debounce on remote wake detect. Reset Source: rst_mod_g_rst_n

Table 14-21516. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	USB2_PM_DEBUG_HW_LPM_ERRATA	R/W	1h	Set to switch the HIRD to BESL format. Reset Source: rst_mod_g_rst_n
19	USB2_PM_DEBUG_HW_LPM_ERRATA1	R/W	1h	Set to change the scale of HW LPM timeout to 256us increments. Reset Source: rst_mod_g_rst_n
18	USB2_PM_DEBUG_ENABLE_FLUSH_TO	R/W	0h	Set to enable flush state timeouts. Reset Source: rst_mod_g_rst_n
17	USB2_PM_DEBUG_EOP_DETECT	R/W	0h	Set to enable full length SE0 detect. Reset Source: rst_mod_g_rst_n
16	USB2_PM_DEBUG_FORCE_FULL_SPEED	R/W	0h	Set to reject device chirp and force full-speed Reset Source: rst_mod_g_rst_n
15	USB2_PM_DEBUG_SPLIT_192_LIMITDIS	R/W	0h	Use to disable 192 byte limit checking on. Reset Source: rst_mod_g_rst_n
14	USB2_PM_DEBUG_FS_LS_EXT_DISCON	R/W	0h	Use UTMI HostDisconnect input for FS/LS Reset Source: rst_mod_g_rst_n
13	USB2_PM_DEBUG_UTMIRST2	R/W	0h	Select UTMI Reset Source 2 Reset Source: rst_mod_g_rst_n
12	USB2_PM_DEBUG_UTMIRST1	R/W	0h	Select UTMI Reset Source 1 Reset Source: rst_mod_g_rst_n
11	USB2_PM_DEBUG_ENABLE_DISC_WIN	R/W	0h	Enable HS disconnect Window. Reset Source: rst_mod_g_rst_n
10	USB2_PM_DEBUG_DIS_PORT_ERR	R/W	0h	Enable Remote Wake Resume Trap. Reset Source: rst_mod_g_rst_n
9	USB2_PM_DEBUG_DIS_ISO_PEEK	R/W	1h	Disable waiting for last indication for USB2 ISO. Reset Source: rst_mod_g_rst_n
8	USB2_PM_DEBUG_DIRECT_RESUME	R/W	1h	Use FS/LS serial I/F to drive resume. Reset Source: rst_mod_g_rst_n
7	USB2_PM_DEBUG_DROPPING	R/W	1h	If new ping on endpoint that already had PING, drop the PING. Reset Source: rst_mod_g_rst_n
6	USB2_PM_DEBUG_FORCEPING	R/W	0h	If retry on endpoint that should have PING, force the PING. Reset Source: rst_mod_g_rst_n
5	USB2_PM_DEBUG_AUTOPING	R/W	1h	After NYET and new packet coming to same EP - ping N times before give up and flush. Reset Source: rst_mod_g_rst_n
4	USB2_PM_DEBUG_PHY_SUSDISALL	R/W	0h	Disable PHY suspend for all states. Reset Source: rst_mod_g_rst_n
3	USB2_PM_DEBUG_PHY_CLKGATEDIS	R/W	0h	Disable PHY suspend during disconnect. Reset Source: rst_mod_g_rst_n
2	USB2_PM_DEBUG_PHY_RSTDISCON	R/W	0h	Disable Clock Gate Reset Source: rst_mod_g_rst_n
1	USB2_PM_DEBUG_PHY_RST	R/W	0h	Control PHY Reset Directly Reset Source: rst_mod_g_rst_n

Table 14-21516. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	USB2_PM_DEBUG_QUICK_SIM	R/W	0h	Short Timer Values For Simulation of USB2.0 parameters. Please refer to Integration Guide section on Debug Features Reset Source: rst_mod_g_rst_n

14.9.2.3.2.221 USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG2 Register

1 USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG2 Register (Offset = 8134h) [reset = 80C40620h]

USB2 Port Link Control 1, 2, 3, 4. This set of registers is used to control the USB set of timers. They are spread over 4 registers each 32 bits wide. This set of registers may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21517. Instance Table

Instance Name	Physical Address
USB0	**0F40 8134h**

Figure 14-7111. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG2 Name Register

31	30	29	28	27	26	25	24
TIMER_RESET_0	TIMER_CHIRP_K_DETECT						
R/W	R/W						
1h	31h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TIMER_CHIRP_K_DETECT						TIMER_CONNECT_DETECT	
R/W						R/W	
31h						31h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TIMER_CONNECT_DETECT							
R/W							
31h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIMER_CONNECT_DETECT			TIMER_DISCONNECT_DETECT_HI				
R/W			R/W				
31h			0h				

Table 14-21519. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TIMER_RESET_0	R/W	1h	Number of microseconds for total reset duration Reset Source: rst_mod_g_rst_n
30:18	TIMER_CHIRP_K_DETECT	R/W	31h	Number of microseconds of Chirp-K to register that a device is chirping Reset Source: rst_mod_g_rst_n
17:5	TIMER_CONNECT_DETECT	R/W	31h	Number of microseconds of K/J in disconnected state to register connect has occurred. Last 5 LSBs. Reset Source: rst_mod_g_rst_n
4:0	TIMER_DISCONNECT_DETECT_HI	R/W	0h	Number of microseconds of SE0 in FS/LS mode to register disconnect had occurred. Last 5 LSBs. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.222 USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG3 Register

1 USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG3 Register (Offset = 8138h) [reset = F865EB6Bh]

USB2 Port Link Control 1, 2, 3, 4. These set of registers is used to control the USB set of timers. They are spread over 4 registers each 32 bits wide. This set of registers may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21520. Instance Table

Instance Name	Physical Address
USB0	**0F40 8138h**

Figure 14-7112. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG3 Name Register

31	30	29	28	27	26	25	24
TIMER_U2_SETTLE				TIMER_U3_SETTLE			
R/W				R/W			
Fh				10CBh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TIMER_U3_SETTLE							
R/W							
10CBh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TIMER_U3_SETTLE	TIMER_RESET						
R/W	R/W						
10CBh	6B6Bh						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIMER_RESET							
R/W							
6B6Bh							

Table 14-21522. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TIMER_U2_SETTLE	R/W	Fh	Number of microseconds after entering U2. linestate changes are ignored as bus settles. First 4 LSB. Reset Source: rst_mod_g_rst_n
27:15	TIMER_U3_SETTLE	R/W	10CBh	Number of microseconds after entering U3. linestate changes are ignored as bus settles Reset Source: rst_mod_g_rst_n
14:0	TIMER_RESET	R/W	6B6Bh	Number of microseconds for total reset duration Reset Source: rst_mod_g_rst_n

14.9.2.3.2.223 USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG4 Register

1 USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG4 Register (Offset = 813Ch) [reset = 8003h]

USB2 Port Link Control 1, 2, 3, 4. These set of registers is used to control the USB set of timers. They are spread over 4 registers each 32 bits wide. This set of registers may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21523. Instance Table

Instance Name	Physical Address
USB0	**0F40 813Ch**

Figure 14-7113. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							TIMER_RESUME_U2_REFLECT
R							R/W
0h							40h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TIMER_RESUME_U2_REFLECT							
R/W							
40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TIMER_RESUME_U2_REFLECT							TIMER_U2_SETTLE
R/W							R/W
40h							3h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIMER_U2_SETTLE							
R/W							
3h							

Table 14-21525. USB3P0SS_CTRL_XHCI_XECP_USB2_LINK_MGR_CTRL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED_R	R	0h	Reserved field, RO
24:9	TIMER_RESUME_U2_REFLECT	R/W	40h	Number of microseconds after detecting U2 remote wake condition to reflect K Reset Source: rst_mod_g_rst_n
8:0	TIMER_U2_SETTLE	R/W	3h	Number of microseconds after entering U2. linestate changes are ignored as bus settles. Last 9 MSB. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.224 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_CTRL_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_CTRL_REG Register (Offset = 8140h) [reset = 300h]

USB2 Max Bandwidth Control. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21526. Instance Table

Instance Name	Physical Address
USB0	**0F40 8140h**

Figure 14-7114. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_CTRL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BW_CTRL_15_12</td><td colspan="4">BW_SYS_FACTOR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BW_CTRL_7_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21528. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved. For Hardware Bandwidth Calculation Only
15:12	BW_CTRL_15_12	R/W	0h	Max. Percentage BW allowed for SS [default: 80] Reset Source: rst_mod_g_rst_n
11:8	BW_SYS_FACTOR	R/W	3h	System factor for Bandwidth calculation Reset Source: rst_mod_g_rst_n
7:0	BW_CTRL_7_0	R/W	0h	Miscellaneous Bandwidth calculator configuration bits Reset Source: rst_mod_g_rst_n

14.9.2.3.2.225 USB3P0SS_CTRL_XHCI_XECP_FPGA_REVISION_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_FPGA_REVISION_REG Register (Offset = 8144h) [reset = 12000000h]

FPGA_REVISION_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21529. Instance Table

Instance Name	Physical Address
USB0	**0F40 8144h**

Figure 14-7115. USB3P0SS_CTRL_XHCI_XECP_FPGA_REVISION_REG Name Register

31	30	29	28	27	26	25	24
FPGA_REVISION_REG_DEFAULT							
R							
12000000h							
23	22	21	20	19	18	17	16
FPGA_REVISION_REG_DEFAULT							
R							
12000000h							
15	14	13	12	11	10	9	8
FPGA_REVISION_REG_DEFAULT							
R							
12000000h							
7	6	5	4	3	2	1	0
FPGA_REVISION_REG_DEFAULT							
R							
12000000h							

Table 14-21531. USB3P0SS_CTRL_XHCI_XECP_FPGA_REVISION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FPGA_REVISION_REG_DEFAULT	R	12000000h	FPGA_REVISION_REG_DEFAULT Reset Source: rst_mod_g_rst_n

14.9.2.3.2.226 USB3P0SS_CTRL_XHCI_XECP_HOST_INTF_CTRL_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_INTF_CTRL_REG Register (Offset = 8148h) [reset = 1h]

Host interface control register. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes. This field should not be modified by software

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Table 14-21532. Instance Table

Instance Name	Physical Address
USB0	0F40 8148h

Figure 14-7116. USB3P0SS_CTRL_XHCI_XECP_HOST_INTF_CTRL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							PROT_HDR_RBUF_OVERFLOW_CCLK
R							R
0h							0h
7	6	5	4	3	2	1	0
CFG_MAX_NUM_OF_RD		HOST_INTF_CTRL				HC_HALT_TIMEOUT_EN	HOST_ERR_MASK
R/W		R/W				R/W	R/W
0h		0h				0h	1h

Table 14-21534. USB3P0SS_CTRL_XHCI_XECP_HOST_INTF_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_R	R	0h	Reserved field, RO
8	PROT_HDR_RBUF_OVERFLOW_CCLK	R	0h	prot_hdr_rbuf_overflow_cclk. Reset Source: rst_mod_g_rst_n
7:6	CFG_MAX_NUM_OF_RD	R/W	0h	cfg_max_num_of_rd. This is to control how many max number of read that we allow ODMA read to issue. '00': can issue 16 reads '10': can issue 8 reads '01': can issue 4 reads Reset Source: rst_mod_g_rst_n
5:2	HOST_INTF_CTRL	R/W	0h	host_intf_ctrl Reset Source: rst_mod_g_rst_n
1	HC_HALT_TIMEOUT_EN	R/W	0h	hc_halt_timeout_en. An internal register bit used to control whether or not to use the hc halt status timer of 15ms Reset Source: rst_mod_g_rst_n

Table 14-21534. USB3P0SS_CTRL_XHCI_XECP_HOST_INTF_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HOST_ERR_MASK	R/W	1h	host_err_mask. If set to '1' do not mask the host system error Reset Source: rst_mod_g_rst_n

14.9.2.3.2.227 USB3P0SS_CTRL_XHCI_XECP_BW_OV_SS_BURST_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_BW_OV_SS_BURST_REG Register (Offset = 814Ch) [reset = 8020h]

BW_OV_SS_BURST_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes. This field should not be modified by software

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Table 14-21535. Instance Table

Instance Name	Physical Address
USB0	**0F40 814Ch**

Figure 14-7117. USB3P0SS_CTRL_XHCI_XECP_BW_OV_SS_BURST_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
BW_OV_SYS_BURST							
R/W							
8h							
15	14	13	12	11	10	9	8
BW_OV_SYS_BURST				BW_OV_SS_BURST			
R/W				R/W			
8h				20h			
7	6	5	4	3	2	1	0
BW_OV_SS_BURST							
R/W							
20h							

Table 14-21537. USB3P0SS_CTRL_XHCI_XECP_BW_OV_SS_BURST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved. For Hardware Bandwidth Calculation Only
23:12	BW_OV_SYS_BURST	R/W	8h	bw_ov_sys_burst Reset Source: rst_mod_g_rst_n
11:0	BW_OV_SS_BURST	R/W	20h	bw_ov_ss_burst Reset Source: rst_mod_g_rst_n

14.9.2.3.2.228 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2 Register (Offset = 8150h) [reset = F0FD838Ch]

Host Control Transfer Manager (TRM) register. This register contains fields, which control the behavior of the Transfer Manager in the xHCI. The functions controlled by this register are made available largely for debug/diagnostic purposes. This functionality is above and beyond that defined in the xHCI specification. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21538. Instance Table

Instance Name	Physical Address
USB0	0F40 8150h

Figure 14-7118. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2 Name Register

31	30	29	28	27	26	25	24
INSERT_CPL_IDMA_WAIT_EN	PKT_BNDRY_BLOCK_HALT_EN	NON_DMA_IMD_EN	ERR_CPL_CODE_STORE_EN	TRM_ODMA_FIFO_DISABLE	TTE_PKT_BNDRY_EXIT	TTE_IN_EP_BLOCK_EN	IGNORE_NPKT_4PRDC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
DOUBLE_CLR_MASK_DIS	STOP_2MS_4TTE_EN	SECOND_EVENT_FOR_ISP_EN	DEV_MBS_CAP_EN	DEADLOCK_TRB_ERR_EN	MULTI_NON0_CTRL_EP_EN	ENT_AT_END_OF_TD_EN	MSI_CNT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	0h	1h
15	14	13	12	11	10	9	8
SKIP_INTR_4RESP_EN	ODMA_CRD_CAL_EN	RPORT_CRD_CHECK_DIS	DISABLE_CPL_SST_IDEQ0_ERR	STREAM_IDLE2PRIME_EN	STREAM_ID_MATCH_EN	TRM_ADV_DETECT_EN	SUPPORT_0LEN_TTE_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	1h	1h
7	6	5	4	3	2	1	0
PKT_BNDRY_2IGNORE_NTRB_EN	FC_ON_2INCOMPLET_EN	SETADDR_OVERRIDE	USE_EMPTY_4TTE_OVERLAP	CNTX_1ST_TD_EN	UPORT_CRD_UPD_EN	ISO_CNT_2NODMA_EN	RESERVE_TRB_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	1h	1h	0h	0h

Table 14-21540. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INSERT_CPL_IDMA_WAIT_EN	R/W	1h	This bit is added for bug FR2601. It is for cache invalidate case where xHC engine needs to insert wait states for completion engine when the completion has received a short packet before XFER engine has finished the TRB fetch for this packet at its packet boundary. '0': Disables the feature, '1': Enables the feature Reset Source: rst_mod_g_rst_n

Table 14-21540. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	PKT_BNDRY_BLOCK_HALT_EN	R/W	1h	This bit is added for bug FR2642. It is to delay the completion engine to generate an event due to internal error conditions that halted an EP until XFER engine has reached a packet boundary. '0': Disabled '1': Enabled Reset Source: rst_mod_g_rst_n
29	NON_DMA_IMD_EN	R/W	1h	This bit is added for bug FR2639. It enables the internal functions where xHC engine needs to immediately serve the EP again. '0': disabled '1': enabled Reset Source: rst_mod_g_rst_n
28	ERR_CPL_CODE_STORE_EN	R/W	1h	This bit is added for bug FR2495. It enables that error completion code of the first error condition detected within an TD. so that we can report the same error completion codes for all other TRBs within this TD. '0': disabled '1': enables the feature Reset Source: rst_mod_g_rst_n
27	TRM_ODMA_FIFO_DISABLE	R/W	0h	This bit disables a new feature where xHC engine will have an ODMA FIFO added for the commands between TRM and ODMA. so that we can avoid the back-pressure situation due to the number of outstanding PCIe read limitation. This is for performance enhancement. '0': Enables this feature, '1': Disables this feature. Reset Source: rst_mod_g_rst_n
26	TTE_PKT_BNDRY_EXIT	R/W	0h	This bit is added for bug FR2446. It is to enable TRM to only send one IN request for TTE 1st phase request even if it has not reached the packet boundary. '0': Disabled, '1': Enabled Reset Source: rst_mod_g_rst_n
25	TTE_IN_EP_BLOCK_EN	R/W	0h	This bit is added for bug FR2395. It disables the single IN EP for TTE function. '0': Disabled, '1': Allow only single IN EP per port for TTE. Reset Source: rst_mod_g_rst_n
24	IGNORE_NPKT_4PRDC	R/W	0h	This bit is added for bug FR2333 where the xHC engine has always ignored the credit returned from device for its OUT EP buffers when the EP is a periodic EP. '0': Enable the xHC engine to follow the flow control, '1': Disable this feature. Reset Source: rst_mod_g_rst_n
23	DOUBLE_CLR_MASK_DIS	R/W	1h	This bit is added for bug FR2283. This is to ensure only one clear pulse generated when a completion has received [disable CPL engine from sending multiple clear]. '0': Disabled, '1': Enabled. Reset Source: rst_mod_g_rst_n
22	STOP_2MS_4TTE_EN	R/W	1h	This bit enables a 2ms timeout for all TTE related EP stop endpoint command. The xHC engine will not check whether there is a pending response in context. It will only wait for 2ms and indicates that EP has been stopped. '0': Disabled, '1': Enabled. Reset Source: rst_mod_g_rst_n

Table 14-21540. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	SECOND_EVENT_FOR_ISP_EN	R/W	1h	This bit enables xHC engine TRM to report the second or more events on an ISP flush on a second or more TRBs with ISP bit set that are flushed for a short packet response received. '0': Disables this feature, '1': Enables this feature. Reset Source: rst_mod_g_rst_n
20	DEV_MBS_CAP_EN	R/W	1h	This bit enables a new feature where the completion engine of TRM can check the credit returned from remote device to not excceed its max burst size. If it does, we will keep the internal credits in the context to the max burst size so that xHC engine will not transmit more than max burst size. Note: CB has this bit default set to '0'. PPT B0 and LPT will have this bit set to'1'. '0': Disables this feature, '1': Enables this feature. Reset Source: rst_mod_g_rst_n
19	DEADLOCK_TRB_ERR_EN	R/W	1h	This bit enables an internally detected deadlock situation being treated as an TRB_ERR when reports the event. This is an internal debug function. '0': Disables this feature, '1': Enables this feature. Reset Source: rst_mod_g_rst_n
18	MULTI_NON0_CTRL_EP_EN	R/W	1h	This bit enables the xHC engine to fully support the non-0 control EP. This bit allows the xHC TRM to keep track of on non-0 control EP per port so that the responses can be routed to the correct DMA engine. '0': Disables this feature, '1': Enables this feature. Reset Source: rst_mod_g_rst_n
17	ENT_AT_END_OF_TD_EN	R/W	0h	This bit enables xHC engine to evaluate the next TRB even if the EP is at the end of a TD. '0': Disables this feature, '1': Enables this feature. Reset Source: rst_mod_g_rst_n
16	MSI_CNT_EN	R/W	1h	This bit enables the new Missing service interval detection mechanism. xHC engine will count how many service interval that it missed, and skip over that many TDs. '0': Disables this feature, '1': Enables this feature. Reset Source: rst_mod_g_rst_n
15	SKIP_INTR_4RESP_EN	R/W	1h	This bit enables a feature where xHC engine will skip a service interval when an Interrupt EP has missed its service interval. '0': Disables this feature, '1': Enables to skip a service interval. Reset Source: rst_mod_g_rst_n
14	ODMA_CRD_CAL_EN	R/W	0h	New feature added to prevent the back-pressure from ODMA due to the fact that it ran out of ODMA timeout timer resources. This is for performance enhancement. We have put into the ODMA credit is part of resource calculation before TRM allows the next scheduling for OUT EP. '0': Disables this feature, '1': Enables this feature. Reset Source: rst_mod_g_rst_n

Table 14-21540. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RPORT_CRD_CHECK_DIS	R/W	0h	The xHC engine has a feature that can check with Receive Port Credit per root port to whether or not allow the next schedule onto this port [disable the RPORT credit check for IDMA]. This is for performance enhancement. '0': Enables this feature, '1': Disables this feature. Reset Source: rst_mod_g_rst_n
12	DISABLE_CPL_SST_IDEQ0_ERR	R/W	0h	'0': Report received stream ID of 0x0000 as an error. '1': Disable the error reporting for a received stream ID value of 0x0000. Note: only used when an endpoint is configured for stream operation. Reset Source: rst_mod_g_rst_n
11	STREAM_IDLE2PRIME_EN	R/W	0h	Enable the host to transfer to the prime-pipe state [and transmit a prime pipe] on each transfer back to the IDLE state. '0': Feature disabled, '1': Feature enabled. Note: Used only when an endpoint is configured for stream operation. Reset Source: rst_mod_g_rst_n
10	STREAM_ID_MATCH_EN	R/W	0h	stream_id_match_en Reset Source: rst_mod_g_rst_n
9	TRM_ADV_DETECT_EN	R/W	1h	'0': Disable this function in XFER engine. '1': Enable the XFER engine to auto detecting a missing service interval function when there is a long delay such that we missed a service interval due to the pending response. Note: Only value of '0' is validated. Reset Source: rst_mod_g_rst_n
8	SUPPORT_0LEN_TTE_EN	R/W	1h	'0': Disable this function. '1': Enable the function to support 0length TTE second phase request from TTE module. Reset Source: rst_mod_g_rst_n
7	PKT_BNDRY_2IGNORE_NTRB_EN	R/W	1h	'0': Disable this function. '1': Enable a packet pace function under a special condition. This is an internal feature of XFER engine. It is not expected to be used other than default. Reset Source: rst_mod_g_rst_n
6	FC_ON_2INCOMPLET_EN	R/W	0h	'0': do not enable this function. '1': assert the sch_req_incomplete signal in XFER engine when a context FC is ON. This is an internal safety feature for XFER engine. Reset Source: rst_mod_g_rst_n
5	SETADDR_OVERRIDE	R/W	0h	'0': Disable the address device command to query a port credit before it is executed in ODMA engine, '1': Enable the address device command to query a port credit before it is executed in ODMA engine. Reset Source: rst_mod_g_rst_n
4	USE_EMPTY_4TTE_OVERLAP	R/W	0h	'0': Enable XFER engine to use a no-pending response flag as a way of identifying a TTE overlap condition, '1': Enable XFER engine to use context empty flag not assert as a way of identifying a TTE overlap condition. Reset Source: rst_mod_g_rst_n
3	CNTX_1ST_TD_EN	R/W	1h	'0': disable the context storage, '1': enable the context storage for a flag to identify a DMA request as the first of TD DMA request. Reset Source: rst_mod_g_rst_n

Table 14-21540. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TRM_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UPORT_CRD_UPD_EN	R/W	1h	'0': Disable the credit redeem, '1': Enable the credit redeem when a port is in NC state. Reset Source: rst_mod_g_rst_n
1	ISO_CNT_2NODMA_EN	R/W	0h	'0': Disable this non DMA TRB detect function '1': Enable the function where XFER engine uses the remaining burst count as an indication that the next TRB on the transfer ring for an ISO TD is either link TRB or event data TRB. Reset Source: rst_mod_g_rst_n
0	RESERVE_TRB_EN	R/W	0h	'0': report TRB ERR for reserved TRB type, '1': enable XFER engine to process a reserved TRB type as a NO-OP TRB. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.229 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX1_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX1_REG Register (Offset = 8168h) [reset = 5647F42h]

HOST_CTRL_BW_MAX1_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21541. Instance Table

Instance Name	Physical Address
USB0	**0F40 8168h**

Figure 14-7119. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX1_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FSLS_BHUB_MAX_BW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SS_MAX_BW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">64h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">HS_MAX_BW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FSLS_MAX_BW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">42h</td></tr>
</table>

Table 14-21543. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	FSLS_BHUB_MAX_BW	R/W	5h	Max. Percentage BW allowed for FS/LS behind hub [default: 90] Reset Source: rst_mod_g_rst_n
23:16	SS_MAX_BW	R/W	64h	Max. Percentage BW allowed for SS [default: 80] Reset Source: rst_mod_g_rst_n
15:8	HS_MAX_BW	R/W	7Fh	Max. Percentage BW allowed for HS [default: 80] Reset Source: rst_mod_g_rst_n
7:0	FSLS_MAX_BW	R/W	42h	Max. Percentage BW allowed for FS/LS [default: 90] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.230 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX2_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX2_REG Register (Offset = 816Ch) [reset = F425285h]

HOST_CTRL_BW_MAX2_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21544. Instance Table

Instance Name	Physical Address
USB0	**0F40 816Ch**

Figure 14-7120. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R				BW_MAX_REG59_32			
R				R/W			
0h				F425285h			
23	22	21	20	19	18	17	16
BW_MAX_REG59_32							
R/W							
F425285h							
15	14	13	12	11	10	9	8
BW_MAX_REG59_32							
R/W							
F425285h							
7	6	5	4	3	2	1	0
BW_MAX_REG59_32							
R/W							
F425285h							

Table 14-21546. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_BW_MAX2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_R	R	0h	Reserved field, RO
27:0	BW_MAX_REG59_32	R/W	F425285h	bw_max_reg[59:32] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.231 USB3P0SS_CTRL_XHCI_XECP_USB2_LINESTATE_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_USB2_LINESTATE_REG Register (Offset = 8170h) [reset = 0h]

USB2_LINESTATE_REG. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21547. Instance Table

Instance Name	Physical Address
USB0	**0F40 8170h**

Figure 14-7121. USB3P0SS_CTRL_XHCI_XECP_USB2_LINESTATE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
PDOWN_STATUS							
R							
0h							
15	14	13	12	11	10	9	8
PDOWN_STATUS							
R							
0h							
7	6	5	4	3	2	1	0
UTMI_LINESTATE							
R							
0h							

Table 14-21549. USB3P0SS_CTRL_XHCI_XECP_USB2_LINESTATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:8	PDOWN_STATUS	R	0h	pdown_status Reset Source: rst_mod_g_rst_n
7:0	UTMI_LINESTATE	R	0h	utmi_linestate Reset Source: rst_mod_g_rst_n

14.9.2.3.2.232 USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER1_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER1_REG Register (Offset = 8174h) [reset = C05140Ch]

HOST_PROTO_GAP_TIMER1_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21550. Instance Table

Instance Name	Physical Address
USB0	**0F40 8174h**

Figure 14-7122. USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER1_REG Name Register

31	30	29	28	27	26	25	24
USB2_PROTO_PKT_GAP_FS							
R/W							
Ch							
23	22	21	20	19	18	17	16
USB2_PROTO_PKT_GAP_HS_RX							
R/W							
5h							
15	14	13	12	11	10	9	8
USB2_PROTO_PKT_GAP_HS_SOF							
R/W							
14h							
7	6	5	4	3	2	1	0
USB2_PROTO_PKT_GAP_HS							
R/W							
Ch							

Table 14-21552. USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	USB2_PROTO_PKT_GAP_FS	R/W	Ch	USB2_PROTO_PKT_GAP_FS Reset Source: rst_mod_g_rst_n
23:16	USB2_PROTO_PKT_GAP_HS_RX	R/W	5h	USB2_PROTO_PKT_GAP_HS_RX Reset Source: rst_mod_g_rst_n
15:8	USB2_PROTO_PKT_GAP_HS_SOF	R/W	14h	USB2_PROTO_PKT_GAP_HS_SOF Reset Source: rst_mod_g_rst_n
7:0	USB2_PROTO_PKT_GAP_HS	R/W	Ch	USB2_PROTO_PKT_GAP_HS Reset Source: rst_mod_g_rst_n

14.9.2.3.2.233 USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER2_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER2_REG Register (Offset = 8178h) [reset = 2A3C64h]

HOST_PROTO_GAP_TIMER2_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21553. Instance Table

Instance Name	Physical Address
USB0	**0F40 8178h**

Figure 14-7123. USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
USB2_PROTO_PKT_GAP_LS_HTX							
R/W							
2Ah							
15	14	13	12	11	10	9	8
USB2_PROTO_PKT_GAP_LS_HRX							
R/W							
3Ch							
7	6	5	4	3	2	1	0
USB2_PROTO_PKT_GAP_LS							
R/W							
64h							

Table 14-21555. USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_GAP_TIMER2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:16	USB2_PROTO_PKT_GAP_LS_HTX	R/W	2Ah	USB2_PROTO_PKT_GAP_LS_HTX Reset Source: rst_mod_g_rst_n
15:8	USB2_PROTO_PKT_GAP_LS_HRX	R/W	3Ch	USB2_PROTO_PKT_GAP_LS_HRX Reset Source: rst_mod_g_rst_n
7:0	USB2_PROTO_PKT_GAP_LS	R/W	64h	USB2_PROTO_PKT_GAP_LS Reset Source: rst_mod_g_rst_n

14.9.2.3.2.234 USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_BTO_TIMER_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_BTO_TIMER_REG Register (Offset = 817Ch) [reset = 5B4190B8h]

HOST_PROTO_BTO_TIMER_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21556. Instance Table

Instance Name	Physical Address
USB0	**0F40 817Ch**

Figure 14-7124. USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_BTO_TIMER_REG Name Register

31	30	29	28	27	26	25	24
USB2_PROTO_BTO_LS							
R/W							
2DAh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
USB2_PROTO_BTO_LS			USB2_PROTO_BTO_FS				
R/W			R/W				
2DAh			64h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
USB2_PROTO_BTO_FS						USB2_PROTO_BTO_HS	
R/W						R/W	
64h						B8h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
USB2_PROTO_BTO_HS							
R/W							
B8h							

Table 14-21558. USB3P0SS_CTRL_XHCI_XECP_HOST_PROTO_BTO_TIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	USB2_PROTO_BTO_LS	R/W	2DAh	USB2_PROTO_BTO_LS Reset Source: rst_mod_g_rst_n
20:10	USB2_PROTO_BTO_FS	R/W	64h	USB2_PROTO_BTO_FS Reset Source: rst_mod_g_rst_n
9:0	USB2_PROTO_BTO_HS	R/W	B8h	USB2_PROTO_BTO_HS Reset Source: rst_mod_g_rst_n

14.9.2.3.2.235 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH_REG Register (Offset = 8180h) [reset = A000000h]

HOST_CTRL_PSCH_REG. Specific control register for Power Scheduler. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21559. Instance Table

Instance Name	Physical Address
USB0	**0F40 8180h**

Figure 14-7125. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH_REG Name Register

31	30	29	28	27	26	25	24
PSCH_HOST_CTRL_REG_I_31_24							
R/W							
Ah							
23	22	21	20	19	18	17	16
RESERVED_RW							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_RW							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_RW							
R/W							
0h							

Table 14-21561. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PSCH_HOST_CTRL_REG_I_31_24	R/W	Ah	PSCH_HOST_CTRL_REG_I_31_24 Reset Source: rst_mod_g_rst_n
23:0	RESERVED_RW	R/W	0h	Reserved field, RW

14.9.2.3.2.236 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH1_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH1_REG Register (Offset = 8184h) [reset = 0h]

HOST_CTRL_PSCH1_REG. Specific internal used control register for Power Scheduler. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21562. Instance Table

Instance Name	Physical Address
USB0	**0F40 8184h**

Figure 14-7126. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH1_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED_RW2</td><td colspan="2">IDLE_SCALE</td><td colspan="2">RESERVED_RW1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_RW1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21564. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PSCH1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_R	R	0h	Reserved field, RO
15:12	RESERVED_RW2	R/W	0h	Reserved field, RW
11:10	IDLE_SCALE	R/W	0h	PSCH_HOST_CTRL_REG_I_43_42. idle_scale. 0=1c . 1=1us. 2=125us Reset Source: rst_mod_g_rst_n
9:0	RESERVED_RW1	R/W	0h	Reserved field, RW

14.9.2.3.2.237 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG Register (Offset = 8190h) [reset = 0h]

HOST_CTRL_LTM_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21565. Instance Table

Instance Name	Physical Address
USB0	**0F40 8190h**

Figure 14-7127. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED_R</td><td colspan="4">BELT_SELECTED</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BELT_SELECTED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21567. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_R	R	0h	Reserved field, RO
11:0	BELT_SELECTED	R	0h	Reports several of the latencies depending on the last programmed belt_select value: 0: LTV value programmed, 1: Lowest BELT received, 2: Last received LTM per Slot, 3: Last received LTM per Port. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.238 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG2 Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG2 Register (Offset = 8194h) [reset = E339060Ch]

AUX Power Management Control 1. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21568. Instance Table

Instance Name	Physical Address
USB0	0F40 8194h

Figure 14-7128. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG2 Name Register

31	30	29	28	27	26	25	24
UPORTS_CHANGE_DETECT_EN	SNPS_PHYSTATUS_DONE_L23_DIS	SNPS_PHYSTATUS_DONE_L1_DIS	SHADOW_DECODE_DIS	BATT_CHARGE_D3_EN	CFG_DEBOUNCE_EN	CFG_DBGP_DIS_AUTO	AUTO_PM_EXIT_L1_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	0h	0h	0h	1h	1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CFG_PSCEG_DIS_SEL	CFG_LTSSM_IDLE2TS2	P2_OVERWRITE_WHENL1_EN	CFG_U3_AUTO	PDOWN_2LINK_RST_EN_REG	U0_WAKE_TIMEOUT_EN	CFG_U2_P3_LFPS_TIME	WAKE_EXIT_USE_LVL_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CFG_U2_P3_TIMEOUT		CFG_U2_P3_EN	RESERVED_RW2		PRDC_PREVENT_L1_EN	CFG_PSCEG_SEL	RESERVED_RW1
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		1h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_RW1				IDLE_WAKEUP_EN	P0_DRIVE_DIS	CFG_FAST_SIMS	AUTO_P2_OW_EN_REG
R/W				R/W	R/W	R/W	R/W
0h				1h	1h	0h	0h

Table 14-21570. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UPORTS_CHANGE_DETECT_EN	R/W	1h	uports_change_detect_en Reset Source: rst_mod_g_rst_n
30	SNPS_PHYSTATUS_DONE_L23_DIS	R/W	1h	snps_phystatus_done_l23_dis Reset Source: rst_mod_g_rst_n
29	SNPS_PHYSTATUS_DONE_L1_DIS	R/W	1h	snps_phystatus_done_l1_dis Reset Source: rst_mod_g_rst_n
28	SHADOW_DECODE_DIS	R/W	0h	shadow_decode_dis Reset Source: rst_mod_g_rst_n
27	BATT_CHARGE_D3_EN	R/W	0h	batt_charge_d3_en Reset Source: rst_mod_g_rst_n
26	CFG_DEBOUNCE_EN	R/W	0h	cfg_debounce_en Reset Source: rst_mod_g_rst_n

Table 14-21570. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CFG_DBGP_DIS_AUTO	R/W	1h	cfg_dbgp_dis_auto Reset Source: rst_mod_g_rst_n
24	AUTO_PM_EXIT_L1_EN	R/W	1h	This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCie core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit 21 of this register. '0': Disables this feature. '1': Enables this feature Reset Source: rst_mod_g_rst_n
23	CFG_PSCEG_DIS_SEL	R/W	0h	'0': Assert PLC for disconnection, '1': Do not assert PLC for disconnection Reset Source: rst_mod_g_rst_n
22	CFG_LTSSM_IDLE2TS2	R/W	0h	This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. '0': Disable this feature. '1': Treat Logic IDLE as TS2 received when in some PCIe LTSSM state. Reset Source: rst_mod_g_rst_n
21	P2_OVERWRITE_WHEN L1_EN	R/W	1h	We have added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. '0': enables P2 overwrite even if we are in D3Hot. '1': disables P2 overwrite due to the D3HOT where PCIe core enters the L1. Reset Source: rst_mod_g_rst_n
20	CFG_U3_AUTO	R/W	1h	'0': Disables the port to enter U3 automatically when in U1/U2, '1': Enables the port to enter U3 automatically when in U1/U2. Reset Source: rst_mod_g_rst_n
19	PDOWN_2LINK_RST_EN _REG	R/W	1h	pdown_2link_rst_en Reset Source: rst_mod_g_rst_n
18	U0_WAKE_TIMEOUT_EN	R/W	0h	This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. '0': disable this feature, '1': enables this feature. Reset Source: rst_mod_g_rst_n
17	CFG_U2_P3_LFPS_TIME	R/W	0h	This bit selects U2 exit LFPS timer value. '0': 320ns - 400ns in 25MHz domain, '1': 240ns - 320ns in 25MHz domain. Reset Source: rst_mod_g_rst_n

Table 14-21570. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	WAKE_EXIT_USE_LVL_EN	R/W	1h	This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generate a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. '0': Disables this function, which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed. '1': Enables this function. Reset Source: rst_mod_g_rst_n
15:14	CFG_U2_P3_TIMEOUT	R/W	0h	This field defines the timeout value to enter P3 mode in U2. 00: 7us - 8us, 01: 511us - 512us, 10: disables the timer [0us], 11: disables the timer [0us]. Reset Source: rst_mod_g_rst_n
13	CFG_U2_P3_EN	R/W	0h	'0': disables PHY P3 mode in U2. '1': enables PHY P3 mode in U2. Reset Source: rst_mod_g_rst_n
12:11	RESERVED_RW2	R/W	0h	Reserved field, RW
10	PRDC_PREVENT_L1_EN	R/W	1h	This bit enables a function that the SPNS PCIe core is controlled by xHCI engine internal periodic EP traffic conditions. '0': Disabled this function '1': Enables the xHC engine to request an exit of L1 when the service time has reached for an periodic EP. Reset Source: rst_mod_g_rst_n
9	CFG_PSCEG_SEL	R/W	1h	This bit selects the port status change event generation mode. '0': port status change event is only blocked by the individual status change bit. '1': port status change event is blocked until all status change bit are cleared. Reset Source: rst_mod_g_rst_n
8:4	RESERVED_RW1	R/W	0h	Reserved field, RW
3	IDLE_WAKEUP_EN	R/W	1h	This bit enables the AUX PM module to automatically wakeup from deep power down when engine has detected non-idle condition. '0': feature disabled '1': feature enabled Reset Source: rst_mod_g_rst_n
2	P0_DRIVE_DIS	R/W	1h	This bit ensures the P1 drive during PERST#. '0': feature disabled, '1': feature enabled. Reset Source: rst_mod_g_rst_n
1	CFG_FAST_SIMS	R/W	0h	This bit is for simulation modes only. It enables further reductions to simulation timings in addition to cfg_fast_training. Please refer to Integration Guide Debug Features section '0': Normal timings '1': Enable fast simulation timing modes Reset Source: rst_mod_g_rst_n

Table 14-21570. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AUTO_P2_OW_EN_REG	R/W	0h	This bit enables a feature where we can get P2 overwrite to automatically turned on when there is no pending traffic in the engine. '0': feature disabled, '1': feature enabled. This field should not be modified by software Reset Source: rst_mod_g_rst_n

14.9.2.3.2.239 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG3 Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG3 Register (Offset = 8198h) [reset = 83370h]

Configuration bits for USB2 PHY. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21571. Instance Table

Instance Name	Physical Address
USB0	**0F40 8198h**

Figure 14-7129. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_R</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED_R</td><td colspan="4">HS_DC_V_LVL_ADJ</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">8h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">FSLS_SRC_IMPD_ADJ</td><td>HS_TRANS_PRE_EMPH_EN</td><td>HS_TRANS_RS_TIME_ADJ</td><td colspan="2">TRANS_HS_CROSS_ADJ</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">3h</td><td>0h</td><td>0h</td><td colspan="2">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">STA</td><td colspan="3">PHY_MISC_CTRL_REG_4_2</td><td colspan="2">PHY_MISC_CTRL_REG_1_0</td></tr>
<tr><td colspan="3">R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">3h</td><td colspan="3">4h</td><td colspan="2">0h</td></tr>
</table>

Table 14-21573. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED_R	R	0h	Reserved field, RO
19:16	HS_DC_V_LVL_ADJ	R/W	8h	HS DC Voltage Level Adjustment Reset Source: rst_mod_g_rst_n
15:12	FSLS_SRC_IMPD_ADJ	R/W	3h	FS/LS Source Impedance Adjustment Reset Source: rst_mod_g_rst_n
11	HS_TRANS_PRE_EMPH_EN	R/W	0h	HS Transmitter Pre-Emphasis Enable Reset Source: rst_mod_g_rst_n
10	HS_TRANS_RS_TIME_ADJ	R/W	0h	HS Transmitter Rise/Fall Time Adjustment Reset Source: rst_mod_g_rst_n
9:8	TRANS_HS_CROSS_ADJ	R/W	3h	Transmitter High-Speed Crossover Adjustment Reset Source: rst_mod_g_rst_n
7:5	STA	R/W	3h	Squelch Threshold Adjustment Reset Source: rst_mod_g_rst_n
4:2	PHY_MISC_CTRL_REG_4_2	R/W	4h	phy_misc_ctrl_reg[4:2] Reset Source: rst_mod_g_rst_n

Table 14-21573. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PHY_MISC_CTRL_REG_1_0	R/W	0h	phy_misc_ctrl_reg[1:0] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.240 USB3P0SS_CTRL_XHCI_XECP_DEBUG_CTRL_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_DEBUG_CTRL_REG Register (Offset = 819Ch) [reset = 2000000h]

DEBUG_CTRL_REG. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21574. Instance Table

Instance Name	Physical Address
USB0	**0F40 819Ch**

Figure 14-7130. USB3P0SS_CTRL_XHCI_XECP_DEBUG_CTRL_REG Name Register

31	30	29	28	27	26	25	24
CFG_PCIE_GASKET_CTRL			CFG_L1_L0S_CTRL				NEW_NB_CTRL_REG
R/W			R/W				R/W
0h			1h				0h
23	22	21	20	19	18	17	16
NEW_NB_CTRL_REG				CFG_PM_DEBUG_CTRL			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CFG_RESUME_WAKE_DIS	CFG_RESUME_TIMER_EN	RESERVED_RW				SW_EEPROM_EN	PORT_PWR_CTRL_TOGGLE
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h
7	6	5	4	3	2	1	0
DEBUG_EN_TOGGLE	DEBUG_FINE_MODE_SEL		DEBUG_MODE_SEL				
R/W	R/W		R/W				
0h	0h		0h				

Table 14-21576. USB3P0SS_CTRL_XHCI_XECP_DEBUG_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	CFG_PCIE_GASKET_CTRL	R/W	0h	cfg_pcie_gasket_ctrl[2:0] This field should not be modified by software Reset Source: rst_mod_g_rst_n
28:25	CFG_L1_L0S_CTRL	R/W	1h	cfg_l1_l0s_ctrl[3:0] This field should not be modified by software Reset Source: rst_mod_g_rst_n
24:20	NEW_NB_CTRL_REG	R/W	0h	new_nb_ctrl_reg. Used in aux_pm module to keep old NB behavior. This field should not be modified by software Reset Source: rst_mod_g_rst_n
19:16	CFG_PM_DEBUG_CTRL	R/W	0h	cfg_pm_debug_ctrl. Used in aux_power_logic.v for debug. This field should not be modified by software Reset Source: rst_mod_g_rst_n
15	CFG_RESUME_WAKE_DIS	R/W	0h	cfg_resume_wake_dis This field should not be modified by software Reset Source: rst_mod_g_rst_n

Table 14-21576. USB3P0SS_CTRL_XHCI_XECP_DEBUG_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	CFG_RESUME_TIMER_EN	R/W	0h	cfg_resume_timer_en This field should not be modified by software Reset Source: rst_mod_g_rst_n
13:10	RESERVED_RW	R/W	0h	Reserved field, RW This field should not be modified by software
9	SW_EEPROM_EN	R/W	0h	debug control for CoosBay: sw_eeprom_en This field should not be modified by software Reset Source: rst_mod_g_rst_n
8	PORT_PWR_CTRL_TOGGLE	R/W	0h	debug control for CoosBay: port_pwr_ctrl_toggle This field should not be modified by software Reset Source: rst_mod_g_rst_n
7	DEBUG_EN_TOGGLE	R/W	0h	debug control for CoosBay: debug_en_toggle This field should not be modified by software Reset Source: rst_mod_g_rst_n
6:5	DEBUG_FINE_MODE_SEL	R/W	0h	debug_fine_mode_sel This field should not be modified by software Reset Source: rst_mod_g_rst_n
4:0	DEBUG_MODE_SEL	R/W	0h	debug_mode_sel This field should not be modified by software Reset Source: rst_mod_g_rst_n

14.9.2.3.2.241 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG2 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG2 Register (Offset = 81A0h) [reset = 7A00h]

Host Control Scheduler. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21577. Instance Table

Instance Name	Physical Address
USB0	**0F40 81A0h**

Figure 14-7131. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_RW1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_RW1	SERVICE_TIME_WATERMARK						
R/W	R/W						
0h	7Ah						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_RW0				SCH_POLL_DBRANG_DIS	SCH_ALWAYS_RESERVE_DIS	SCH_POLL_RESERVATION_DIS	SCH_PRDC_RETRY_USB2_DIS
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-21579. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_SCH_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:15	RESERVED_RW1	R/W	0h	Reserved field, RW
14:8	SERVICE_TIME_WATERMARK	R/W	7Ah	service_time_watermark Reset Source: rst_mod_g_rst_n
7:4	RESERVED_RW0	R/W	0h	Reserved field, RW
3	SCH_POLL_DBRANG_DIS	R/W	0h	Host Control Scheduler: sch_poll_dbrang_dis Reset Source: rst_mod_g_rst_n
2	SCH_ALWAYS_RESERVE_DIS	R/W	0h	Host Control Scheduler: sch_always_reserve_dis Reset Source: rst_mod_g_rst_n
1	SCH_POLL_RESERVATION_DIS	R/W	0h	Host Control Scheduler: sch_poll_reservation_dis Reset Source: rst_mod_g_rst_n
0	SCH_PRDC_RETRY_USB2_DIS	R/W	0h	Host Control Scheduler: sch_prdc_retry_usb2_dis Reset Source: rst_mod_g_rst_n

14.9.2.3.2.242 USB3P0SS_CTRL_XHCI_XECP_AUX_DEBUG_READ_ONLY Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_DEBUG_READ_ONLY Register (Offset = 81A4h) [reset = 1h]

AUX_DEBUG_READ_ONLY. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21580. Instance Table

Instance Name	Physical Address
USB0	**0F40 81A4h**

Figure 14-7132. USB3P0SS_CTRL_XHCI_XECP_AUX_DEBUG_READ_ONLY Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_R						P2_OVERWRITE_ENTER	ALL_UPORTS_IN_U3NC
R						R	R
0h						0h	1h

Table 14-21582. USB3P0SS_CTRL_XHCI_XECP_AUX_DEBUG_READ_ONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_R	R	0h	Reserved field, RO
1	P2_OVERWRITE_ENTER	R	0h	p2_overwrite_enter, sticky bit Reset Source: rst_mod_g_rst_n
0	ALL_UPORTS_IN_U3NC	R	1h	all_uports_in_u3nc. If set all ports are in U3NC state. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.243 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_PORTNUM_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_PORTNUM_REG Register (Offset = 81A8h) [reset = 40020101h]

AUX_CTRL_PORTNUM_REG. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21583. Instance Table

Instance Name	Physical Address
USB0	**0F40 81A8h**

Figure 14-7133. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_PORTNUM_REG Name Register

31	30	29	28	27	26	25	24
LIMIT_MAX_SLOTS							
R							
40h							
23	22	21	20	19	18	17	16
LIMIT_MAX_NPORTS							
R							
2h							
15	14	13	12	11	10	9	8
LIMIT_NPORTS_USB3							
R							
1h							
7	6	5	4	3	2	1	0
LIMIT_NPORTS_USB2							
R							
1h							

Table 14-21585. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_PORTNUM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	LIMIT_MAX_SLOTS	R	40h	Limit Max slots to fewer then synthesized [strap] Reset Source: rst_mod_g_rst_n
23:16	LIMIT_MAX_NPORTS	R	2h	Limit Max ports to fewer then synthesized [strap] Reset Source: rst_mod_g_rst_n
15:8	LIMIT_NPORTS_USB3	R	1h	Limit USB3 ports to fewer then synthesized [strap] This field should not be modified by software Reset Source: rst_mod_g_rst_n
7:0	LIMIT_NPORTS_USB2	R	1h	Limit USB2 ports to fewer then synthesized [strap] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.244 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_DEV_REMOVE_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_DEV_REMOVE_REG Register (Offset = 81ACh) [reset = 0h]

Feature #3002 (Device Removable in PORTSC). This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This register is reserved. This is a vendor defined capability. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21586. Instance Table

Instance Name	Physical Address
USB0	**0F40 81ACh**

Figure 14-7134. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_DEV_REMOVE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
DEVICE_REMOVABLE_USB3							
R							
0h							
7	6	5	4	3	2	1	0
DEVICE_REMOVABLE_USB2							
R							
0h							

Table 14-21588. USB3P0SS_CTRL_XHCI_XECP_AUX_CTRL_DEV_REMOVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_R	R	0h	Reserved field, RO
15:8	DEVICE_REMOVABLE_USB3	R	0h	Set to 1 if port has non-removable device [strap to 0/1] Reset Source: rst_mod_g_rst_n
7:0	DEVICE_REMOVABLE_USB2	R	0h	Set to 1 if port has non-removable device [strap to 0/1] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.245 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TTE_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TTE_REG1 Register (Offset = 81E0h) [reset = 2h]

Specific control register for SCH. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21589. Instance Table

Instance Name	Physical Address
USB0	**0F40 81E0h**

Figure 14-7135. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TTE_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_RW						EOB_INT_DIS	EOB_ISO_DIS
R/W						R/W	R/W
0h						1h	0h

Table 14-21591. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_TTE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_R	R	0h	Reserved field, RO
7:2	RESERVED_RW	R/W	0h	Reserved field, RW
1	EOB_INT_DIS	R/W	1h	Disable end of burst workaround INT [0 length on final MDATA] Reset Source: rst_mod_g_rst_n
0	EOB_ISO_DIS	R/W	0h	Disable end of burst workaround ISO [0 length on final MDATA] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.246 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG1 Register (Offset = 81E4h) [reset = 0h]

HOST_CTRL_LTM_REG1. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21592. Instance Table

Instance Name	Physical Address
USB0	**0F40 81E4h**

Figure 14-7136. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG1 Name Register

31	30	29	28	27	26	25	24
BELT_SELECT		BELT_USB2_EN	BELT_USB3_EN	BELT_PCIE_EN	BELT_FORCE_RECOMPUTE	BELT_FORCE_DISABLEALL	BELT_FORCE_DISABLESLOT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BELT_PORT_SELECT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BELT_SLOT_SELECT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BELT_SLOT_SELECT							
R/W							
0h							

Table 14-21594. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	BELT_SELECT	R/W	0h	Selects which BELT value should be reported on the belt_selected field when the register is read. 0 - LTV value programmed, 1 - Lowest BELT received, 2 - Last received LTM per Slot, 3 - Last received LTM per Port. Reset Source: rst_mod_g_rst_n
29	BELT_USB2_EN	R/W	0h	belt_usb2_en, active '0', default enabled Reset Source: rst_mod_g_rst_n
28	BELT_USB3_EN	R/W	0h	belt_usb3_en, active '0', default enabled Reset Source: rst_mod_g_rst_n
27	BELT_PCIE_EN	R/W	0h	belt_pcie_en, default disabled Reset Source: rst_mod_g_rst_n
26	BELT_FORCE_RECOMPUTE	R/W	0h	belt_force_recompute Reset Source: rst_mod_g_rst_n
25	BELT_FORCE_DISABLEALL	R/W	0h	belt_force_disable_all Reset Source: rst_mod_g_rst_n

Table 14-21594. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	BELT_FORCE_DISABLE SLOT	R/W	0h	belt_force_disable_slot Reset Source: rst_mod_g_rst_n
23:16	BELT_PORT_SELECT	R/W	0h	Port Number for the BELT reported on the belt_selected field when belt_select is 3 Reset Source: rst_mod_g_rst_n
15:0	BELT_SLOT_SELECT	R/W	0h	Slot-ID for BELT reported on the belt_selected field when belt_select is 2 Reset Source: rst_mod_g_rst_n

14.9.2.3.2.247 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG2 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG2 Register (Offset = 81E8h) [reset = 400h]

HOST_CTRL_LTM_REG2. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21595. Instance Table

Instance Name	Physical Address
USB0	**0F40 81E8h**

Figure 14-7137. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_R							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_R				DEFAULT_PCIE_LTM			
R				R/W			
0h				400h			
7	6	5	4	3	2	1	0
DEFAULT_PCIE_LTM							
R/W							
400h							

Table 14-21597. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_LTM_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_R	R	0h	Reserved field, RO
11:0	DEFAULT_PCIE_LTM	R/W	400h	DEFAULT_PCIE_LTM converted from ns with convert_ns2belt Reset Source: rst_mod_g_rst_n

14.9.2.3.2.248 USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_0 Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_0 Register (Offset = 8200h) [reset = 0h]

For internal use. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21598. Instance Table

Instance Name	Physical Address
USB0	**0F40 8200h**

Figure 14-7138. USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_RW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_RW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_RW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_RW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21600. USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_RW	R/W	0h	Reserved field, RW

14.9.2.3.2.249 USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_1 Register

1 USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_1 Register (Offset = 8204h) [reset = 0h]

For internal use. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21601. Instance Table

Instance Name	Physical Address
USB0	**0F40 8204h**

Figure 14-7139. USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_1 Name Register

31	30	29	28	27	26	25	24
RESERVED_RW							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_RW							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_RW							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_RW							
R/W							
0h							

Table 14-21603. USB3P0SS_CTRL_XHCI_XECP_AUX_SCRATCHPAD_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_RW	R/W	0h	Reserved field, RW

14.9.2.3.2.250 USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG Register (Offset = 8210h) [reset = 0h]

Battery charge mode and enable register. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21604. Instance Table

Instance Name	Physical Address
USB0	**0F40 8210h**

Figure 14-7140. USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG Name Register

31	30	29	28	27	26	25	24
BATTERY_CHARGE_MODE_EN_REG							RESERVEDR
R/W							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVEDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVEDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVEDR							BATTERY_CHARGE_MODE_REG
R							R/W
0h							0h

Table 14-21606. USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	BATTERY_CHARGE_MODE_EN_REG	R/W	0h	The register allows enabling battery charge mode for each USB2 port. Reset Source: rst_mod_g_rst_n
24:1	RESERVEDR	R	0h	Reserved field, RO.
0	BATTERY_CHARGE_MODE_REG	R/W	0h	The register allows setting battery charge mode for each USB2 port. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.251 USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG1 Register (Offset = 8214h) [reset = 13641F4h]

Battery charge control register 1. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21607. Instance Table

Instance Name	Physical Address
USB0	**0F40 8214h**

Figure 14-7141. USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED_R	BATTERY_CHARGE_CTRL_REG1_DEFAULT						
R	R/W						
0h	13641F4h						
23	22	21	20	19	18	17	16
BATTERY_CHARGE_CTRL_REG1_DEFAULT							
R/W							
13641F4h							
15	14	13	12	11	10	9	8
BATTERY_CHARGE_CTRL_REG1_DEFAULT							
R/W							
13641F4h							
7	6	5	4	3	2	1	0
BATTERY_CHARGE_CTRL_REG1_DEFAULT							
R/W							
13641F4h							

Table 14-21609. USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_R	R	0h	Reserved field, RO
30:0	BATTERY_CHARGE_CTRL_REG1_DEFAULT	R/W	13641F4h	BATTERY_CHARGE_CTRL_REG1_DEFAULT Reset Source: rst_mod_g_rst_n

14.9.2.3.2.252 USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG2 Register

1 USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG2 Register (Offset = 8218h) [reset = 1F4014h]

Battery charge control register 2. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21610. Instance Table

Instance Name	Physical Address
USB0	**0F40 8218h**

Figure 14-7142. USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
BATTERY_CHARGE_CTRL_REG2_DEFAULT							
R/W							
1F4014h							
15	14	13	12	11	10	9	8
BATTERY_CHARGE_CTRL_REG2_DEFAULT							
R/W							
1F4014h							
7	6	5	4	3	2	1	0
BATTERY_CHARGE_CTRL_REG2_DEFAULT							
R/W							
1F4014h							

Table 14-21612. USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:0	BATTERY_CHARGE_CTRL_REG2_DEFAULT	R/W	1F4014h	BATTERY_CHARGE_CTRL_REG2_DEFAULT Reset Source: rst_mod_g_rst_n

14.9.2.3.2.253 USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG3 Register

1 USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG3 Register (Offset = 821Ch) [reset = 0h]

Battery charge debug register. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21613. Instance Table

Instance Name	Physical Address
USB0	**0F40 821Ch**

Figure 14-7143. USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED_R							
R							
0h							
23	22	21	20	19	18	17	16
BATTERY_CHARGE_DEBUG							
R							
0h							
15	14	13	12	11	10	9	8
BATTERY_CHARGE_DEBUG							
R							
0h							
7	6	5	4	3	2	1	0
BATTERY_CHARGE_DEBUG							
R							
0h							

Table 14-21615. USB3P0SS_CTRL_XHCI_XECP_BATTERY_CHARGE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_R	R	0h	Reserved field, RO
23:0	BATTERY_CHARGE_DEBUG	R	0h	Battery charge debug Reset Source: rst_mod_g_rst_n

14.9.2.3.2.254 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG1 Register

1 USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG1 Register (Offset = 8220h) [reset = 0h]

Feature #581. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21616. Instance Table

Instance Name	Physical Address
USB0	**0F40 8220h**

Figure 14-7144. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED_RW							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_RW							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_RW		CFG_TIEBREAK_MODE		CFG_TIEBREAK_VAL			
R/W		R/W		R/W			
0h		0h		0h			
7	6	5	4	3	2	1	0
LINK_LTSSM_DEBUG_CTRL						LINK_8B_DEBUG_CTRL	
R/W						R/W	
0h						0h	

Table 14-21618. USB3P0SS_CTRL_XHCI_XECP_HOST_CTRL_PORT_LINK_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_RW	R/W	0h	Reserved field, RW
13:12	CFG_TIEBREAK_MODE	R/W	0h	cfg_tiebreak_mode Reset Source: rst_mod_g_rst_n
11:8	CFG_TIEBREAK_VAL	R/W	0h	cfg_tiebreak_val Reset Source: rst_mod_g_rst_n
7:2	LINK_LTSSM_DEBUG_CTRL	R/W	0h	link_debug_ctrl register:.link_ltssm_debug_ctrl. Possible values: stay_in_idle : bit 0 set. stay_in_ts1 : bit 1 set. stay_in_ts2 : bit 2 set. stay_in_tseq : bit 3 set. stay_in_lfps : bit 4 set. timeout_jumpover_en : bit 5 set. Reset Source: rst_mod_g_rst_n
1:0	LINK_8B_DEBUG_CTRL	R/W	0h	link_debug_ctrl register:.link_8b_debug_ctrl. bit[0]: xmt_d102, bit[1]: xmt_comma. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.255 USB3P0SS_CTRL_XHCI_XECP_USBLEGSUP Register

1 USB3P0SS_CTRL_XHCI_XECP_USBLEGSUP Register (Offset = 8370h) [reset = 1h]

USB Legacy Support Capability. This register is an xHCI extended capability register. This register is used by pre-OS software (BIOS) and the operating system to coordinate ownership of the xHC. This extended capability requires one additional 32-bit register for control/status information (USBLEGCTLSTS). This register is in the Aux Power well. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21619. Instance Table

Instance Name	Physical Address
USB0	**0F40 8370h**

Figure 14-7145. USB3P0SS_CTRL_XHCI_XECP_USBLEGSUP Name Register

31	30	29	28	27	26	25	24
RSVD2							HCOSOS
R							R/W
0h							0h
23	22	21	20	19	18	17	16
RSVD1							HCBIOSOS
R							R/W
0h							0h
15	14	13	12	11	10	9	8
NEXTCP							
R							
0h							
7	6	5	4	3	2	1	0
CID							
R							
1h							

Table 14-21621. USB3P0SS_CTRL_XHCI_XECP_USBLEGSUP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RSVD2	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
24	HCOSOS	R/W	0h	HC OS Owned Semaphore, RW. Default = '0'. System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the HC BIOS Owned Semaphore bit [HCBIOSOS] reads as '0'. Reset Source: rst_mod_g_rst_n
23:17	RSVD1	R	0h	Reserved: Reserved for future RO implementations. Registers or memory that shall be treated as read-only by system software. Rsvd registers shall return zero when read. Software shall ignore the value read from these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21621. USB3P0SS_CTRL_XHCI_XECP_USBLEGSUP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	HCBIOSOS	R/W	0h	HC BIOS Owned Semaphore [HCBIOSOS], RW. Default = '0'. The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to '0' in response to a request for ownership of the xHC by system software. Reset Source: rst_mod_g_rst_n
15:8	NEXTCP	R	0h	Next Capability Pointer, RO. This field indicates the location of the next capability with respect to the effective address of this capability. A non-zero value in this register indicates a relative offset, in Dwords, from this Dword to the beginning of the next extended capability. Reset Source: rst_mod_g_rst_n
7:0	CID	R	1h	USB Legacy Support Capability ID, RO. This capability provides the xHCI Pre-OS to OS Handoff Synchronization support capability. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.256 USB3P0SS_CTRL_XHCI_XECP_USBLEGCTLSTS Register

1 USB3P0SS_CTRL_XHCI_XECP_USBLEGCTLSTS Register (Offset = 8374h) [reset = 0h]

USB Legacy Support Control Status. Pre-OS (BIOS) software uses this register to enable System Management Interrupts (SMIs) for every xHCI/USB event it needs to track. Some bits of this register are simply shadow bit of USBSTS register. This register is in the Aux Power well. This register may be read from or written to at any time, including whilst the CNR field in the USBSTS register is high.

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Table 14-21622. Instance Table

Instance Name	Physical Address
USB0	0F40 8374h

Figure 14-7146. USB3P0SS_CTRL_XHCI_XECP_USBLEGCTLSTS Name Register

31	30	29	28	27	26	25	24
SMIBAR	SMIPCIC	SMIOSOC	RSVD4				
R/W1TC	R/W1TC	R/W1TC	R				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RSVD4			SMIHSE	RSVD3			SMIEI
R			R	R			R
0h			0h	0h			0h
15	14	13	12	11	10	9	8
SMIBARE	SMIPCICE	SMIOSOE	RSVD2				
R/W	R/W	R/W	R				
0h	0h	0h	0h				
7	6	5	4	3	2	1	0
RSVD2			SMIHSEE	RSVD1			USBSMIE
R			R/W	R			R/W
0h			0h	0h			0h

Table 14-21624. USB3P0SS_CTRL_XHCI_XECP_USBLEGCTLSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SMIBAR	R/W1TC	0h	SMI on BAR, RW1C. Default = '0'. This bit is set to '1' whenever the Base Address Register [BAR] is written. Reset Source: rst_mod_g_rst_n
30	SMIPCIC	R/W1TC	0h	SMI on PCI Command, RW1C. Default = '0'. This bit is set to '1' whenever the PCI Command Register is written. Reset Source: rst_mod_g_rst_n
29	SMIOSOC	R/W1TC	0h	SMI on OS Ownership Change, RW1C. Default = '0'. This bit is set to '1' whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from '1' to a '0' or '0' to a '1'. Reset Source: rst_mod_g_rst_n
28:21	RSVD4	R	0h	Reserved and Zero: Reserved for future RW1C implementations. Software shall use zero for writes to these bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n

Table 14-21624. USB3P0SS_CTRL_XHCI_XECP_USBLEGCTLSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	SMIHSE	R	0h	SMI on Host System Error, RO. Default = '0'. Shadow bit of Host System Error [HSE] bit in the USBSTS register. Refer to Section 5.4.2 of xHCI specification for definition and effects of the events associated with this bit being set to '1'. To clear this bit to a '0', system software shall write a '1' to the Host System Error [HSE] bit in the USBSTS register. Reset Source: rst_mod_g_rst_n
19:17	RSVD3	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
16	SMIEI	R	0h	SMI on Event Interrupt, RO. Default = '0'. Shadow bit of Event Interrupt [EINT] bit in the USBSTS register. Refer to Section 5.4.2 of xHCI specification for definition. This bit follows the state the Event Interrupt [EINT] bit in the USBSTS register, e.g. it automatically clears when EINT clears or set when EINT is set. Reset Source: rst_mod_g_rst_n
15	SMIBARE	R/W	0h	SMI on BAR Enable, RW. Default = '0'. When this bit is '1' and SMI on BAR is '1', then the host controller will issue an SMI. Reset Source: rst_mod_g_rst_n
14	SMIPCICE	R/W	0h	SMI on PCI Command Enable, RW. Default = '0'. When this bit is '1' and SMI on PCI Command is '1', then the host controller will issue an SMI. Reset Source: rst_mod_g_rst_n
13	SMIOSOE	R/W	0h	SMI on OS Ownership Enable, RW. Default = '0'. When this bit is a '1' AND the OS Ownership Change bit is '1', the host controller will issue an SMI. Reset Source: rst_mod_g_rst_n
12:5	RSVD2	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
4	SMIHSEE	R/W	0h	SMI on Host System Error Enable, RW. Default = '0'. When this bit is a '1', and the SMI on Host System Error bit [below] in this register is a '1', the host controller will issue an SMI immediately. Reset Source: rst_mod_g_rst_n
3:1	RSVD1	R	0h	Reserved and Preserved: Reserved for future RW implementations. Software shall preserve the value read for writes to bits. Note: At present the fields are implemented as RO. Reset Source: rst_mod_g_rst_n
0	USBSMIE	R/W	0h	USB SMI Enable, RW. Default = '0'. When this bit is a '1', and the SMI on Event Interrupt bit [below] in this register is a '1', the host controller will issue an SMI immediately. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.257 USB3P0SS_CTRL_XHCI_XECP_USB3_TEST_PORT0_REG Register

1 USB3P0SS_CTRL_XHCI_XECP_USB3_TEST_PORT0_REG Register (Offset = 8800h) [reset = 0h]

USB3_TEST_PORT_REG. This is a vendor defined capability. This register is reserved. This register should not be accessed by software. It is described only for informative purposes.

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Table 14-21625. Instance Table

Instance Name	Physical Address
USB0	**0F40 8800h**

Figure 14-7147. USB3P0SS_CTRL_XHCI_XECP_USB3_TEST_PORT0_REG Name Register

31	30	29	28	27	26	25	24
LINK_TEST_LOOP_PASS							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LINK_TEST_LOOP_PASS							LINK_TEST_DONE
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
USB3_TEST_LOOP_NUM							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
USB3_TEST_LOOP_NUM							USB3_TEST_CTRL
R/W							R/W
0h							0h

Table 14-21627. USB3P0SS_CTRL_XHCI_XECP_USB3_TEST_PORT0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	LINK_TEST_LOOP_PASS	R	0h	link_test_loop_pass Reset Source: rst_mod_g_rst_n
16	LINK_TEST_DONE	R	0h	link_test_done This field should not be modified by software Reset Source: rst_mod_g_rst_n
15:1	USB3_TEST_LOOP_NUM	R/W	0h	USB3_test_loop_num Reset Source: rst_mod_g_rst_n
0	USB3_TEST_CTRL	R/W	0h	USB3_test_ctrl Reset Source: rst_mod_g_rst_n

14.9.2.3.2.258 USB3P0SS_CTRL_DEV_USB_CONF Register

1 USB3P0SS_CTRL_DEV_USB_CONF Register (Offset = 0h) [reset = 0h]

Global Configuration Register

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Table 14-21628. Instance Table

Instance Name	Physical Address
USB0	**0F40 0000h**

Figure 14-7148. USB3P0SS_CTRL_DEV_USB_CONF Name Register

31	30	29	28	27	26	25	24
LGO_SSINACT	LGO_U2	LGO_U1	LGO_U0	U2DS	U2EN	U1DS	U1EN
R/W	R/W	R/W	R/W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED3	CLK3OFFDS	CLK3OFFEN	LGO_L0	CLK2OFFDS	CLK2OFFEN	L1DS	L1EN
R	W	W	R/W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
DEVDS	DEVEN	SFORCE_FS	CFORCE_FS	DMAOFFDS	DMAOFFEN	RESERVED2	RESERVED1
W	W	W	W	W	W	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SWRST	BENDIAN	LENDIAN	USB2DIS	USB3DIS	RESERVED0	CFGSET	CFGRST
R/W	W	W	W	W	R	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21630. USB3P0SS_CTRL_DEV_USB_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LGO_SSINACT	R/W	0h	SS.Inactive state entry request [SS mode only]. This bit can be used only if USBSS-DEV is part of the CDNS USB OTG Controller [USB_CAP.OTG_READY bit is 1 while reading]. In other cases should not be used and returns 0 when read. Writing '1' will trigger an attempt to perform transition to SS.Inactive state. Should be used only if Link is in U0 or Recovery state. This bit will be automatically cleared to '0' after link layer finishes SS.Inactive request. Result of the request [link layer enters SS.Inactive or not] can be verified by reading LTS [link state] field in USB_STS register. Writing '0' has no effect Reset Source: rst_mod_g_rst_n
30	LGO_U2	R/W	0h	U2 state entry request [SS mode only]. Writing '1' will trigger an attempt to perform transition to U2 state. This bit will be automatically cleared to '0' after link layer finishes U2 request. Result of the request [link layer enters U2 or not] can be verified by reading LTS [link state] field in USB_STS register. Writing '1' has no effect when USB_STS.LGOU2ENS is set to '0'. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n

Table 14-21630. USB3P0SS_CTRL_DEV_USB_CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	LGO_U1	R/W	0h	U1 state entry request [SS mode only]. Writing '1' will trigger an attempt to perform transition to U1 state. This bit will be automatically cleared to '0' after link layer finishes U1 request. Result of the request [link layer enters U1 or not] can be verified by reading LTS [link state] field in USB_STS register. Writing '1' has no effect when USB_STS.LGOU1ENS is set to '0'. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
28	LGO_U0	R/W	0h	U0 state entry request [SS mode only]. Writing '1' will trigger an attempt to perform transition to U0 state. If the link is suspended [U3 state] and CPU set this bit to'1', link will start driving resume signaling on its upstream link to indicate remote wakeup. The Function Wake Notification should be send using USB_CMD.SDNFW bit. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
27	U2DS	W	0h	U2 state entry disable [SS mode only]. Writing '1' to this bit disables link layer from entering U2 state. Status of this bit can be checked in the USB_STS register. When both U2EN and U2DS bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. Writing '0' has no effect. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
26	U2EN	W	0h	U2 state entry enable [device side, SS mode only]. Writing '1' to this bit enables link layer to enter U2 state. Status of this bit can be checked in the USB_STS register. Writing '0' has no effect. When both U2EN and U2DS bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
25	U1DS	W	0h	U1 state entry disable [SS mode only]. Writing '1' to this bit disables link layer from entering U1 state. Status of this bit can be checked in the USB_STS register. Writing '0' has no effect. When both U1EN and U1DS bits are set to '1' while writing to USB_CONF register, none of the operations associated with these bits will be performed. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
24	U1EN	W	0h	U1 state entry enable [device side, SS mode only], Writing '1' to this bit enables link layer to enter U1 state. Status of this bit can be checked in the USB_STS register. Writing '0' has no effect. When both U1EN and U1DS bits are set to '1' while writing to USB_CONF register, none of the operations associated with these bits will be performed. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
23	RESERVED3	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21630. USB3P0SS_CTRL_DEV_USB_CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	CLK3OFFDS	W	0h	USB 3.0 clock gate enable. Writing '1' to this bit disables pclk clock turning-off when device enters U3 link state in SS mode. The actual 'USB 3.0 clock gate' status in can be checked in the USB_STS.USB3OFF register. When both CLK3OFFDS and CLK3OFFEN bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
21	CLK3OFFEN	W	0h	USB 3.0 clock gate disable. Writing '1' to this bit enables pclk clock turning-off when device enters U3 link state in SS mode. The actual 'USB 3.0 clock gate' status in can be checked in the USB_STS.USB3OFF register. When both CLK3OFFDS and CLK3OFFEN bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
20	LGO_L0	R/W	0h	L0 LPM state entry request [HS/FS mode only]. Writing '1' will trigger an attempt to perform transition to L0 LPM state. This bit will be automatically cleared to '0' after LPM enter L0 state. Result of the request [LPM enters L0 or not] can be verified by reading LPMST [LPM state] field in USB_STS register. Writing '0' has no effect. If the LPM is suspended [L2 state] and CPU set this bit to'1', upstream will start driving resume signaling to indicate remote wakeup. Reset Source: rst_mod_g_rst_n
19	CLK2OFFDS	W	0h	USB 2.0 clock gate enable. Writing '1' to this bit disables hsfs clock turning-off when device enters L2 LPM state in HS/FS mode. The actual 'USB 2.0 clock gate' status in can be checked in the USB_STS.USB2OFF register. When both CLK2OFFDS and CLK2OFFEN bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
18	CLK2OFFEN	W	0h	USB 2.0 clock gate disable. Writing '1' to this bit enables hsfs clock turning-off when device enters L2 LPM state in HS/FS mode. The actual 'USB 2.0 clock gate' status in can be checked in the USB_STS.USB2OFF register. When both CLK2OFFDS and CLK2OFFEN bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
17	L1DS	W	0h	L1 LPM state entry disable [HS/FS mode only]. Writing '1' to this bit disables USB2.0 LPM from entering L1 state. Status of this bit can be checked in the USB_STS register. Writing '0' has no effect. When both L1EN and L1DS bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n

Table 14-21630. USB3P0SS_CTRL_DEV_USB_CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	L1EN	W	0h	L1 LPM state entry enable [device side, HS/FS mode only]. Writing '1' to this bit enables USB2.0 LPM to enter L1 state. Status of this bit can be checked in the USB_STS register. Writing '0' has no effect. When both L1EN and L1DS bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
15	DEVDS	W	0h	Device disable. Writing '1' to the DEVDS bit sets to '0' the USB_STS.DEVS bit. Check also the DEVEN bit description. Writing '0' has no effect. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
14	DEVEN	W	0h	Device enable. After Power-On-Reset the USBSS_DEV is disconnected from the USB bus. To connect the device into the USB bus the software has to write '1' to DEVEN bit - this couse connection of the VBUS input to the internal device logic and connetion to the USB bus as a result [inside of USBSS_DEV an internal VBUS is used which which is the and gate: VBUS input AND USB_STS.DEVS bit in SFRs]. Writing '1' to the DEVEN bit sets to '1' the USB_STS.DEVS bit. Writing '0' has no effect. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
13	SFORCE_FS	W	0h	Set Force Full Speed. Writing '1' to this bit forces Full Speed when USBSS-DEV operates in USB2.0 mode [disables High Speed]. When both SFORCE_FS and CFORCE_FS bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. The status of this settings can be check in the USB_STS.DISABLE_HS bit. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
12	CFORCE_FS	W	0h	Clear Force Full Speed. Writing '1' to this bit stop forcing Full Speed when USBSS-DEV operates in USB2.0 mode [stop disabling High Speed]. When both SFORCE_FS and CFORCE_FS bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. The status of this settings can be check in the USB_STS.DISABLE_HS bit. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
11	DMAOFFDS	W	0h	DMA clock turn-off disable. Writing '1' to this bit disables DMA clock turning-off when device exits U0 link state in SuperSpeed mode. When both DMAOFFDS and DMAOFFEN bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
10	DMAOFFEN	W	0h	DMA clock turn-off enable. Writing '1' to this bit enables DMA clock turning-off when device exits U0 link state in SuperSpeed mode. When both DMAOFFDS and DMAOFFEN bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
9	RESERVED2	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21630. USB3P0SS_CTRL_DEV_USB_CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
7	SWRST	R/W	0h	Device software reset. When set to 1, the entire USBSS-DEV is reset. The SWRST resets most flip-flops in entire USBSS-DEV. This bit is also used to connect disconnected device. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
6	BENDIAN	W	0h	Big Endian Access. Writing '1' to this bit sets Big Endian byte order for SFRs access. Writing '0' has no effect. When both LENDIAN and BENDIAN bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
5	LENDIAN	W	0h	Little Endian access. Writing '1' to this bit sets Little Endian byte order for SFRs access. By default [after hardware reset], USBSS-DEV acts as little-endian device. Writing '0' has no effect. When both LENDIAN and BENDIAN bits are set to '1' while writing to USB_CONF register, the device behaviour is udefined. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
4	USB2DIS	W	0h	Disconnect USB device in HS/FS. Writing '1' to this bit disconnects USB in HS/FS. The actual USB connection status in HS/FS can be checked in the USB_STS register. Writing '0' has no effect. To connect disconnected device, CPU performs software reset [UCB_CFG.SWRST]. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
3	USB3DIS	W	0h	Disconnect USB device in SuperSpeed. Writing '1' to this bit disconnects USB in Super Speed. The actual USB connection status in the SS mode can be checked in the USB_STS register. If link is in U3 [SuperSpeed PHY clock is disabled] while software writes USB3DIS bit, first the hardware automatically wakes up the PHY to the P2 to turn on the PHY clock [clklink], and second, all operations related to device disconnection cease. Writing '0' has no effect. To connect disconnected device, CPU performs software reset [UCB_CFG.SWRST]. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n
2	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
1	CFGSET	W	0h	Set Configuration. Software writes '1' to this bit when it receives SET_CONFIGURATION request with non-zero configuration number. CPU sets this bit after setting requested configuration and before setting REQ_CMPL bit in the EP_CMD register. Configuration will be set internally in the hardware when REQ_CMPL bit will be set. Writing '0' has no effect. The actual configuration status can be checked in the USB_STS register. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n

Table 14-21630. USB3P0SS_CTRL_DEV_USB_CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CFGRST	W	0h	Reset USB device configuration. Writing '1' to this bit resets USB device configuration, leaving only EP0 IN/OUT active [all other EP-related registers will be loaded with default values]. Any configuration/interface change, including adding new IF, must be preceded with configuration reset, adding current IF's as well as new IF. Writing '0' has no effect. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.259 USB3P0SS_CTRL_DEV_USB_STS Register

1 USB3P0SS_CTRL_DEV_USB_STS Register (Offset = 4h) [reset = 3F1C0300h]

Global Status Register

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Table 14-21631. Instance Table

Instance Name	Physical Address
USB0	**0F40 0004h**

Figure 14-7149. USB3P0SS_CTRL_DEV_USB_STS Name Register

31	30	29	28	27	26	25	24
ENDIAN	DMAOFF	LST				U2ENS	U1ENS
R	R	R				R	R
0h	0h	Fh				1h	1h

23	22	21	20	19	18	17	16
RESERVED2		DISABLE_HS	USB2CONS	LPMST		VBUSS	L1ENS
R		R	R	R		R	R
0h		0h	1h	3h		0h	0h

15	14	13	12	11	10	9	8
ADDRESSED	DEVS	RESERVED1			IN_RST	CLK3OFF	CLK2OFF
R	R	R			R	R	R
0h	0h	0h			0h	1h	1h

7	6	5	4	3	2	1	0
ENDIAN_MIRROR	USBSPEED			RESERVED0	USB3CONS	MEM_OV	CFGSTS
R	R			R	R	R	R
0h	0h			0h	0h	0h	0h

Table 14-21633. USB3P0SS_CTRL_DEV_USB_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENDIAN	R	0h	SFR Endian status. Little/Big Endian byte order for SFR access: 0 - Little Endian order [default after hardware reset] 1 - Big Endian order Reset Source: rst_mod_g_rst_n
30	DMAOFF	R	0h	DMA clock turn-off status. DMA clock turn-off/enable status: 0 - DMA clock is always on [default after hardware reset] 1 - DMA clock turn-off in U1, U2 and U3 [SS mode] is enabled. Reset Source: rst_mod_g_rst_n

Table 14-21633. USB3P0SS_CTRL_DEV_USB_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29:26	LST	R	Fh	SuperSpeed Link LTSSM state. This field reflects USBSS-DEV current SuperSpeed link state: 0 - U0 State 1 - U1 State 2 - U2 State 3 - U3 State [Device Suspended] 4 - Disabled State 5 - RxDetect State 6 - Inactive State 7 - Polling State 8 - Recovery State 9 - Hot Reset State 10 - Compliance Mode State 11 - Loopback State 12:14 - Reserved 15 - Uninitialized Reset Source: rst_mod_g_rst_n
25	U2ENS	R	1h	U2 state enable status [valid in SS mode only]: 0 - Entering to U2 state disabled 1 - Entering to U2 state enabled Reset Source: rst_mod_g_rst_n
24	U1ENS	R	1h	U1 state enable status [valid in SS mode only]: 0 - Entering to U1 state disabled 1 - Entering to U1 state enabled Reset Source: rst_mod_g_rst_n
23:22	RESERVED2	R	0h	Reserved field. Write ignored. 0 when read
21	DISABLE_HS	R	0h	DisableHS status [valid for HS/FS mode only] 0 - High Speed operations in USB2.0 [FS/HS] mode not disabled 1 - High Speed operations in USB2.0 [FS/HS] mode disabled Reset Source: rst_mod_g_rst_n
20	USB2CONS	R	1h	HS/FS mode connection enable status [valid for HS/FS mode only]. 0 - the disconnect bit for HS/FS mode is set [USB_CONF.USB2DIS] 1 - the disconnect bit for HS/FS mode is not set [device can be connected in this mode] The actual connection status can be checked in the USB_STS.USBSPEED register Reset Source: rst_mod_g_rst_n
19:18	LPMST	R	3h	HS/FS LPM state [valid for HS/FS mode only]. This field reflects USBSS-DEV current LPM [used in HS/FS mode] state: 0 - L0 State 1 - L1 State 2 - L2 State 3 - L3 State Reset Source: rst_mod_g_rst_n
17	VBUSS	R	0h	Internal VBUS connection status. 0 - internal VBUS is not detected 1 - internal VBUS is detected Reset Source: rst_mod_g_rst_n
16	L1ENS	R	0h	L1 LPM state enable status [valid for HS/FS mode only]. 0 - Entering to L1 LPM state disabled 1 - Entering to L1 LPM state enabled Reset Source: rst_mod_g_rst_n

Table 14-21633. USB3P0SS_CTRL_DEV_USB_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADDRESSED	R	0h	Address status: 0 - USB device is default state 1 - USB device is at least in address state [Function Address was set by the SW] Reset Source: rst_mod_g_rst_n
14	DEVS	R	0h	Device enable Status 0 - USB device is disabled [VBUS input is disconnected from internal logic] 1 - USB device is enabled [VBUS input is connected to the internal logic] This bit can be changed by setting DEVEN or DEVDS bits in USB_CONF register. Reset Source: rst_mod_g_rst_n
13:11	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
10	IN_RST	R	0h	Controler in reset state. This bit indicate that whole [in case of POR] or part of controller [in case of SWRST or USB resets] currently is in reset state. As controller has registers in both clock domains [system, and USB], internal reset synchronization between these domains may take longer than the cause of the reset [e.g active reset_n input]. Thus it is recommended to check if controller is not in reset state, before software starts its operations [especially after POR]. 0 - Internal reset is active 1 - Internal reset is not active and controller is fully operational. Reset Source: rst_mod_g_rst_n
9	CLK3OFF	R	1h	PCLK clock turn-off status. When CLK3OFF bit is '0', the phypowerdown output signal is not set to '11' in U3 link state, thus USB3.0 PHY does not turn off the pclk clock. 0 - pclk clock is always on 1 - pclk clock turn-off in U3 [SS mode] is enabled [default after hardware reset] Reset Source: rst_mod_g_rst_n
8	CLK2OFF	R	1h	HS/FS clock turn-off status. When CLK2OFF bit is '0', the utmisuspendm output signal is not set low in USB2.0 suspend state [L2 state], thus USB2.0 PHY does not turn off the hsfs clock 0 - hsfs clock is always on 1 - hsfs clock turn-off in L2 [HS/FS mode] is enabled [default after hardware reset] Reset Source: rst_mod_g_rst_n
7	ENDIAN_MIRROR	R	0h	Little/Big Endian byte order for SFR access. 0 - Little Endian order [default after hardware reset] 1 - Big Endian order Endian byte order for SFR access can be changed by setting BENDIAN or LEDNIAN bits in USB_CONF register. Reset Source: rst_mod_g_rst_n
6:4	USBSPEED	R	0h	Device speed: 0: undef., 1: LowSpeed [not supported], 2: FullSpeed, 3: HighSpeed, 4: SuperSpeed, 5-7: Reserved Reset Source: rst_mod_g_rst_n
3	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
2	USB3CONS	R	0h	SuperSpeed connection status. 0 - USB in SuperSpeed mode disconnected 1 - USB in SuperSpeed mode connected Reset Source: rst_mod_g_rst_n

Table 14-21633. USB3P0SS_CTRL_DEV_USB_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MEM_OV	R	0h	On-chip memory overflow. 0 - On-chip memory status OK 1 - On-chip memory overflow Memory overflow may occur if, during enumeration [SET_CONFIGURATION request] device software will try to turn on too many endpoints or will try to set too much endpoinds buffers [see EP_CFG.BUFFERING]. After each completion of enumeration software should check this bit, and when a memory overflow occurred, software must delete current configuration [using USB_CONF.CFGRST bit] and then set the one that requires less on-chip memory. For available memory calculation, the CDNS_USBSSDEV_ATTACHED_MEM_SIZE define parameter is used. Reset Source: rst_mod_g_rst_n
0	CFGSTS	R	0h	Configuration status. 1 - device is in the configured state 0 - device is not configured This bit set during SET_CONFIGURATION request means that status stage of this request was finished successfully, thus device configuration was finished successfully. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.260 USB3P0SS_CTRL_DEV_USB_CMD Register

1 USB3P0SS_CTRL_DEV_USB_CMD Register (Offset = 8h) [reset = 0h]

Global Command Register

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Table 14-21634. Instance Table

Instance Name	Physical Address
USB0	**0F40 0008h**

Figure 14-7150. USB3P0SS_CTRL_DEV_USB_CMD Name Register

31	30	29	28	27	26	25	24
RESERVED1				DNLTM_BELT_11_8			
R				W			
0h				0h			
23	22	21	20	19	18	17	16
DNLTM_BELT_7_0							
W							
0h							
15	14	13	12	11	10	9	8
RESERVED0		SPKT	SDNLTM	TMODE_SEL		STMODE	SDNFW
R		R/W	R/W	W		W	R/W
0h		0h	0h	0h		0h	0h
7	6	5	4	3	2	1	0
FADDR							SET_ADDR
W							W
0h							0h

Table 14-21636. USB3P0SS_CTRL_DEV_USB_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
27:24	DNLTM_BELT_11_8	W	0h	Device Notification 'Latency Tolerance Message' - BELT value [11:8] [SS mode only]. If user writes '1' to SDNLTM bit, the device will send Device Notification 'Latency Tolerance Message' with 'BELT[11:8]' field value equal to DNLTM_BELT_11_8. This field must be filled up before the USB_CMD.SDNLTM bit is set, and cannot be changed while USB_CMD.SDNLTM bit is not zero [Device Notification is being sent by the device controller] This field is always '0' while reading. Reset Source: rst_mod_g_rst_n

Table 14-21636. USB3P0SS_CTRL_DEV_USB_CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	DNLTM_BELT_7_0	W	0h	Device Notification 'Latency Tolerance Message' - BELT value [7:0] / Device Notification 'Function Wake' - Interface value [SS mode only]. This field must be filled up before one of the USB_CMD.SDNLTM/ SDNFW bits is set, and cannot be changed while USB_CMD.SDNLTM/SDNFW bits are not zero [Device Notification is being sent by the device controller]. If user writes '1' to SDNFW bit the device will send Device Notification 'Function Wake' with 'Interface[7:0]' field value equal to DNLTM_BELT_7_0. If user writes '1' to SDNLTM bit, the device will send Device Notification 'Latency Tolerance Message' with 'BELT[7:0]' field value equal to DNLTM_BELT_7_0. This field is always '0' while reading. Reset Source: rst_mod_g_rst_n
15:14	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
13	SPKT	R/W	0h	Send Custom Transaction Packet [SS mode only] Writing '1' will trigger an attempt to send Custom TP as defined in the USB3.0 specification. The packet contents that will be send as TP to the host must be previously prepared in the CPKT1 [will be sent as DWORD 0 in the TP], CPKT2 [will be sent as DWORD 1 in the TP] and CPKT3 [will be sent as DWORD 2 in the TP] registers. Note that TP DWORD 3 will be automatically inserted by the device controller. This bit will be automatically cleared if this TP is sent and only then the new Custom TP [by means of SPKT bit] or other Notification TP [by means of SDNLTM or SDNFW bits] can be send again. Writing 0 has no effect. This bit cannot be written by 1 simultaneously with SDNLTM and SDNFW bits. Reset Source: rst_mod_g_rst_n
12	SDNLTM	R/W	0h	Send Latency Tolerance Message Device Notification TP [SS mode only]. Writing '1' will trigger an attempt to send Device Notification 'Latency Tolerance Message' with 'BELT' field set to DNLTM_BELT. This bit will be automatically cleared if the LTM Notification TP is sent and only then the new LTM Notification TP or the other TP [by means of SPKT or SDNFW bits] can be send again. Writing '0' has no effect. This bit cannot be written by '1' simultaneously with SPKT and SDNFW bits. Reset Source: rst_mod_g_rst_n
11:10	TMODE_SEL	W	0h	Test mode selector [HS/FS mode only]. This field contains selected Test Mode - Device will enter this Test mode when '1' is written to STMODE. USB 2.0 Test mode selector: 00 - Test_J, 01 - Test_K, 10 - Test_SE0_NAK, 11 - Test_Packet This field is always '0' while reading. Reset Source: rst_mod_g_rst_n
9	STMODE	W	0h	Set Test Mode [HS/FS mode only]. Writing the value '1 'to this bit causes the device enters into test mode selected by the TMODE_SEL field. Writing '0' has no effect. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n

Table 14-21636. USB3P0SS_CTRL_DEV_USB_CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SDNFW	R/W	0h	Send Function Wake Device Notification TP [SS mode only]. Writing '1' will trigger an attempt to send 'Device Notification' with 'Interface' field set to DNFW_INT. This bit will be automatically cleared if the FW Notification TP is sent and only then the new FW Notification TP or the other TP [by means of SPKT or SDNLTM bits] can be send again. Writing '0' has no effect. This bit cannot be written by '1' simultaneously with SPKT and SDNLTM bits. Reset Source: rst_mod_g_rst_n
7:1	FADDR	W	0h	Function Address. This field is saved to the device only when the field SET_ADDR is set '1 ' during write to USB_CMD register. Software is responsible for entering the address of the device during SET_ADDRESS request service. This field should be set immediately after the SETUP packet is decoded, and prior to confirmation of the status phase [what is done by bit EP_CMD.REQ_CMPL] Verify that the device successfully completed the SET_ADDRESS request and is in ADRESSED state [as defined in USB3 spec] can be realized by checking the bit USB_STS. ADRESSED. USB_CMD.FADDR field can also be read at any time. This field is always '0' while reading. Reset Source: rst_mod_g_rst_n
0	SET_ADDR	W	0h	Set Function Address. Writing the value '1 'to this bit causes the device is assigned to the USB Function Address according to the FADDR field. The device address must be saved by software when operating SET_ADDRESS request. After saving device address, software should set the EP_CMD.ERDY bit [as with all other requests] to quit the setup phase and then set bit EP_CMD.REQ_CMPL to confirm the status of the host phase. Writing '0 'has no effect. This bit is always '0' while reading. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.261 USB3P0SS_CTRL_DEV_USB_IPTN Register

1 USB3P0SS_CTRL_DEV_USB_IPTN Register (Offset = Ch) [reset = 0h]

USB ITPN Reserved

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Table 14-21637. Instance Table

Instance Name	Physical Address
USB0	**0F40 000Ch**

Figure 14-7151. USB3P0SS_CTRL_DEV_USB_IPTN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		ITPN					
R		R					
0h		0h					
7	6	5	4	3	2	1	0
ITPN							
R							
0h							

Table 14-21639. USB3P0SS_CTRL_DEV_USB_IPTN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
13:0	ITPN	R	0h	ITP[SS] / SOF [HS/FS] number. In SS mode this field represent number of last ITP received from host. In HS/FS mode this field represent number of last SOF received from host. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.262 USB3P0SS_CTRL_DEV_USB_LPM Register

1 USB3P0SS_CTRL_DEV_USB_LPM Register (Offset = 10h) [reset = 0h]

USB LPM Register

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Table 14-21640. Instance Table

Instance Name	Physical Address
USB0	**0F40 0010h**

Figure 14-7152. USB3P0SS_CTRL_DEV_USB_LPM Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			BRW	HIRD			
R			R	R			
0h			0h	0h			

Table 14-21642. USB3P0SS_CTRL_DEV_USB_LPM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
4	BRW	R	0h	Remote Wakeup Enable [bRemoteWake] Reset Source: rst_mod_g_rst_n
3:0	HIRD	R	0h	Host Initiated Resume Duration. This is the Resume duration from L1 LPM state, received from the host in the latest Extended Token packet. For more information see chapter: 'HS/FS mode - Link Power Management' Reset Source: rst_mod_g_rst_n

14.9.2.3.2.263 USB3P0SS_CTRL_DEV_USB_IEN Register

1 USB3P0SS_CTRL_DEV_USB_IEN Register (Offset = 14h) [reset = 0h]

Interrupt Enable Register

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Table 14-21643. Instance Table

Instance Name	Physical Address
USB0	**0F40 0014h**

Figure 14-7153. USB3P0SS_CTRL_DEV_USB_IEN Name Register

31	30	29	28	27	26	25	24
RESERVED4		UWRESEIEN	UWRESSIEN	RESERVED3	CFGRESIEN	L1EXTIEN	L1ENTIEN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED2		L2EXTIEN	L2ENTIEN	RESERVED1	U2RESIEN	DIS2IEN	CON2IEN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED0			SPKTIEN	WAKEIEN	ITPIEN	U1EXTIEN	U1ENTIEN
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
U2EXTIEN	U2ENTIEN	U3EXTIEN	U3ENTIEN	UHRESIEN	UWRESIEN	DISIEN	CONIEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21645. USB3P0SS_CTRL_DEV_USB_IEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED4	R	0h	Reserved field. Write ignored. 0 when read
29	UWRESEIEN	R/W	0h	End of the USB SS warm reset interrupt enable. This bit enables requesting a UWRESEI interrupt Reset Source: rst_mod_g_rst_n
28	UWRESSIEN	R/W	0h	Start of the USB SS warm reset interrupt enable. This bit enables requesting a UWRESSI interrupt Reset Source: rst_mod_g_rst_n
27	RESERVED3	R	0h	Reserved field. Write ignored. 0 when read
26	CFGRESIEN	R/W	0h	Configuration reset interrupt enable. This bit enables requesting a CFGRESI interrupt Reset Source: rst_mod_g_rst_n
25	L1EXTIEN	R/W	0h	LPM L1 state exit interrupt enable. This bit enables requesting an L1EXTI interrupt. Reset Source: rst_mod_g_rst_n
24	L1ENTIEN	R/W	0h	LPM L1 state enter interrupt enable. This bit enables requesting an L1ENTI interrupt. Reset Source: rst_mod_g_rst_n
23:22	RESERVED2	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21645. USB3P0SS_CTRL_DEV_USB_IEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	L2EXTIEN	R/W	0h	LPM L2 state exit interrupt enable. This bit enables requesting a L2EXTI interrupt. Reset Source: rst_mod_g_rst_n
20	L2ENTIEN	R/W	0h	LPM L2 state enter interrupt enable. This bit enables requesting a L2ENTI interrupt. Reset Source: rst_mod_g_rst_n
19	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
18	U2RESIEN	R/W	0h	USB reset [HS/FS mode] interrupt enable. This bit enables requesting an U2RESI interrupt. Reset Source: rst_mod_g_rst_n
17	DIS2IEN	R/W	0h	HS/FS mode disconnection interrupt enable. This bit enables requesting a DIS2I interrupt. Reset Source: rst_mod_g_rst_n
16	CON2IEN	R/W	0h	HS/FS mode connection interrupt enable. This bit enables requesting a CON2I interrupt. Reset Source: rst_mod_g_rst_n
15:13	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
12	SPKTIEN	R/W	0h	Send Custom Packet interrupt enable. This bit enables requesting a Send Custom Packet interrupt. Reset Source: rst_mod_g_rst_n
11	WAKEIEN	R/W	0h	Wakeup interrupt enable. This bit enables requesting a Wakeup interrupt. Reset Source: rst_mod_g_rst_n
10	ITPIEN	R/W	0h	ITP/SOF packet detected interrupt enable. This bit enables requesting an ITPI interrupt. Reset Source: rst_mod_g_rst_n
9	U1EXTIEN	R/W	0h	SS link U1 state exit interrupt enable. This bit enables requesting an U1EXTI interrupt. Reset Source: rst_mod_g_rst_n
8	U1ENTIEN	R/W	0h	SS link U1 state enter interrupt enable. This bit enables requesting an U1ENTI interrupt. Reset Source: rst_mod_g_rst_n
7	U2EXTIEN	R/W	0h	SS link U2 state exit interrupt enable. This bit enables requesting an U2EXTI interrupt. Reset Source: rst_mod_g_rst_n
6	U2ENTIEN	R/W	0h	SS link U2 state enter interrupt enable. This bit enables requesting an U2ENTI interrupt. Reset Source: rst_mod_g_rst_n
5	U3EXTIEN	R/W	0h	SS link U3 state exit interrupt enable [wakeup]. This bit enables requesting an U3EXTI interrupt. Reset Source: rst_mod_g_rst_n
4	U3ENTIEN	R/W	0h	SS link U3 state enter interrupt enable [suspend]. This bit enables requesting an U3ENTI interrupt. Reset Source: rst_mod_g_rst_n
3	UHRESIEN	R/W	0h	USB SS hot reset interrupt enable. This bit enables requesting an UHRESI interrupt. Reset Source: rst_mod_g_rst_n

Table 14-21645. USB3P0SS_CTRL_DEV_USB_IEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UWRESIEN	R/W	0h	USB SS warm reset interrupt enable. This bit enables requesting an UWRESI interrupt. Reset Source: rst_mod_g_rst_n
1	DISIEN	R/W	0h	SS disconnection interrupt enable. This bit enables requesting a DISI interrupt. Reset Source: rst_mod_g_rst_n
0	CONIEN	R/W	0h	SS connection interrupt enable. This bit enables requesting a CONI interrupt. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.264 USB3P0SS_CTRL_DEV_USB_ISTS Register

1 USB3P0SS_CTRL_DEV_USB_ISTS Register (Offset = 18h) [reset = 0h]

USB Interrupt Status Register Each bit (interrupt flag) from this register can be cleared by writing '1'.

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Table 14-21646. Instance Table

Instance Name	Physical Address
USB0	0F40 0018h

Figure 14-7154. USB3P0SS_CTRL_DEV_USB_ISTS Name Register

31	30	29	28	27	26	25	24
RESERVED4		UWRESEI	UWRESSI	RESERVED3	CFGRESI	L1EXTI	L1ENTI
R		R/W1TC	R/W1TC	R	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED2		L2EXTI	L2ENTI	RESERVED1	U2RESI	DIS2I	CON2I
R		R/W1TC	R/W1TC	R	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED0			SPKTI	WAKEI	ITPI	U1EXTI	U1ENTI
R			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
U2EXTI	U2ENTI	U3EXTI	U3ENTI	UHRESI	UWRESI	DISI	CONI
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21648. USB3P0SS_CTRL_DEV_USB_ISTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED4	R	0h	Reserved field. Write ignored. 0 when read
29	UWRESEI	R/W1TC	0h	End of the USB warm reset detected. This interrupt is requested after the SuperSpeed warm reset ends. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
28	UWRESSI	R/W1TC	0h	Start of the USB warm reset detected. This interrupt is requested as soon as the SuperSpeed warm reset signalling is detected. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
27	RESERVED3	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21648. USB3P0SS_CTRL_DEV_USB_ISTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	CFGRESI	R/W1TC	0h	USB configuration reset detected. This interrupt is requested after the device internally resets its endpoints onfiguration. This is done after each USB reset [UWRESI, UWRESI or U2RESI], after each connection event [CONI, CON2I] and after configuration reset initiated by software [USB_CONF.CFGRST]. Generally this interrupt is generated in the same time as mentioned interrupts, however due to internal clock domain synchronisation this configuration reset can be performed a little later, so one can use this interrupt to perform some software operations. This interrupt informs that controller did the following operations: disabled all non control endpoints, cleared all pending endpoints transfers and interrupts. The configuration reset does not clear general device configuration [set in USB_CONF] and EP0 configuration settings. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
25	L1EXTI	R/W1TC	0h	LPM L1 state exit detected This interrupt informs that HS/FS LPM exit L1 state. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
24	L1ENTI	R/W1TC	0h	LPM L1 state enter detected This interrupt informs that HS/FS LPM enter L1 state. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
23:22	RESERVED2	R	0h	Reserved field. Write ignored. 0 when read
21	L2EXTI	R/W1TC	0h	LPM L2 state exit detected This interrupt informs that HS/FS LPM exit L2 state. This interrupt is reported on the irqs[1] pin. Reset Source: rst_mod_g_rst_n
20	L2ENTI	R/W1TC	0h	LPM L2 state enter detected This interrupt informs that HS/FS LPM enter L2 state. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
19	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
18	U2RESI	R/W1TC	0h	USB reset [HS/FS mode] detected This interrupt is requested after the USB reset in HS/FS mode ends. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
17	DIS2I	R/W1TC	0h	HS/FS mode disconnection detected This interrupt informs that HS/FS upstream port was disconncted from the USB line. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
16	CON2I	R/W1TC	0h	HS/FS mode connection detected This interrupt informs that HS/FS upstream port was conncted to the USB line This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
15:13	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
12	SPKTI	R/W1TC	0h	Send Custom Packet This interrupt informs that Custom Packet prepared in the USB_CPKT1-3 registers and triggered with USB_CMD.SPKT bit was already sent. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n

Table 14-21648. USB3P0SS_CTRL_DEV_USB_ISTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	WAKEI	R/W1TC	0h	This interrupt informs that at wakeup pin appeared active state. This interrupt is reported on the irqs[1] pin. Reset Source: rst_mod_g_rst_n
10	ITPI	R/W1TC	0h	ITP/SOF packet detected In SuperSpeed mode this interrupt informs that ITP packet was received. In FS/HS mode this interrupt informs that SOF was detected. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
9	U1EXTI	R/W1TC	0h	SS link U1 state exit detected This interrupt informs that SuperSpeed link exit U1 state. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
8	U1ENTI	R/W1TC	0h	SS link U1 state enter detected This interrupt informs that SuperSpeed link enter U1 state. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
7	U2EXTI	R/W1TC	0h	SS link U2 state exit detected This interrupt informs that SuperSpeed link exit U2 state. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
6	U2ENTI	R/W1TC	0h	SS link U2 state enter detected This interrupt informs that SuperSpeed link enter U2 state. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
5	U3EXTI	R/W1TC	0h	SS link U3 state exit detected [wakeup] This interrupt informs that SuperSpeed link exit U3 state. This interrupt is reported on the irqs[1] pin. Reset Source: rst_mod_g_rst_n
4	U3ENTI	R/W1TC	0h	SS link U3 state enter detected [suspend] This interrupt informs that SuperSpeed link enter U3 state. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
3	UHRESI	R/W1TC	0h	USB SS hot reset detected This interrupt is requested after the SuperSpeed hot reset ends. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
2	UWRESI	R/W1TC	0h	USB SS warm reset detected This interrupt is requested after the SuperSpeed warm reset ends or when USBSS-DEVs LTSSM exits Polling.LFPS state. After this reset, SW should reininitialize the controller. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
1	DISI	R/W1TC	0h	SS disconnection detected This interrupt informs that SuperSpeed link was disconncted from the USB line. This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n
0	CONI	R/W1TC	0h	SS connection detected This interrupt informs that SuperSpeed link was conncted to the USB line This interrupt is reported on the irqs[0] pin. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.265 USB3P0SS_CTRL_DEV_EP_SEL Register

1 USB3P0SS_CTRL_DEV_EP_SEL Register (Offset = 1Ch) [reset = 0h]

Endpoint Select Register This register is used in conjunction with Endpoint Configuration, Command, Status, and Transfer ring address registers. If processor wants to access a specific endpoint, it has to first identify this endpoint by selecting it in Endpoint select register.

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Table 14-21649. Instance Table

Instance Name	Physical Address
USB0	**0F40 001Ch**

Figure 14-7155. USB3P0SS_CTRL_DEV_EP_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
DIR	RESERVED0			EPNO			
R/W	R			R/W			
0h	0h			0h			

Table 14-21651. USB3P0SS_CTRL_DEV_EP_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
7	DIR	R/W	0h	Selected Endpoint direction. 0-OUT Endpoint selected, 1-IN Endpoint selected Reset Source: rst_mod_g_rst_n
6:4	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
3:0	EPNO	R/W	0h	Selected Endpoint number Reset Source: rst_mod_g_rst_n

14.9.2.3.2.266 USB3P0SS_CTRL_DEV_EP_TRADDR Register

1 USB3P0SS_CTRL_DEV_EP_TRADDR Register (Offset = 20h) [reset = 0h]

Endpoint Transfer Ring Address Register All bytes of the register must be written, to store the TRADDR value. If all bytes of this register are not written at the same time (e.g. byte access), the MSB must be written at the end of the operation

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Table 14-21652. Instance Table

Instance Name	Physical Address
USB0	0F40 0020h

Figure 14-7156. USB3P0SS_CTRL_DEV_EP_TRADDR Name Register

31	30	29	28	27	26	25	24
TRADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
TRADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
TRADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
TRADDR							
R/W							
0h							

Table 14-21654. USB3P0SS_CTRL_DEV_EP_TRADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRADDR	R/W	0h	Transfer Ring address. Address of transfer ring for endpoint selected by endpoint select register. Based on this address, DMA will fetch transfer descriptors from system memory. This register can be used as dequeue pointer. CPU can use this register [read it or write to it] only when endpoint is configured and enabled [using EP_CFG register] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.267 USB3P0SS_CTRL_DEV_EP_CFG Register

1 USB3P0SS_CTRL_DEV_EP_CFG Register (Offset = 24h) [reset = 0h]

Endpoint Configuration Register The endpoint configuration can be changed only once after reset (or configuration reset: USB_CONF.CFGRST). While the device is not in the CONFIGURED state, each write to EP_CFG register allocates space for endpoint configuration in on-chip memory (this is done automatically by the hardware and invisible to the software). That is why write to this register for one endpoint can be executed only once during setup of the device. When the software finishes the device configuration (i.e. all required endpoints have been enabled), it has to set the USB_CONF.CFGSET bit to inform the hardware that the device is in CONFIGURED state. In this state, writing to EP_CFG register can change only ENABLE, ENDIAN and STREAM_EN bits and does not allocate space for endpoint configuration in on-chip memory. All bytes of the register must be written during endpoint configuration. If all bytes of this register are not written at the same time (e.g. byte access), the MSB must be written at the end of the operation.

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Table 14-21655. Instance Table

Instance Name	Physical Address
USB0	**0F40 0024h**

Figure 14-7157. USB3P0SS_CTRL_DEV_EP_CFG Name Register

31	30	29	28	27	26	25	24
BUFFERING					MAXPKTSIZE		
R/W					R/W		
0h					0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAXPKTSIZE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MULT		RESERVED1		MAXBURST			
R/W		R		R/W			
0h		0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EPENDIAN	RESERVED0	SID_CHK	TDL_CHK	STREAM_EN	EPTYPE		ENABLE
R/W	R	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		0h

Table 14-21657. USB3P0SS_CTRL_DEV_EP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	BUFFERING	R/W	0h	Max number of buffered packets. The maximum number of packets the device can buffer in the on-chip memory for a specified endpoint. Valid values are from 0 to 15. Value 0 means that 1 on-chip buffer is available for the appropriate endpoint. Value 15 means that 16 on-chip buffers are available for the appropriate endpoint. Each IN endpoint has individual buffers associated with it. OUT endpoints have common buffers, so buffering for OUT endpoints is determined by the maximum buffering value along all enabled OUT endpoints. The number of possible endpoint buffers depends on the on-chip memory size and the size of endpoint buffers. Reset Source: rst_mod_g_rst_n

Table 14-21657. USB3P0SS_CTRL_DEV_EP_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:16	MAXPKTSIZE	R/W	0h	Max packet size. The maximum packet size this endpoint is capable of sending or receiving. SuperSpeed mode: For control endpoints, this field is set to 512. For bulk endpoint types, this field is set to 1024. For interrupt and isochronous endpoints, this field is set to 1024 if this endpoint defines a value in the bMaxBurst field greater than zero. If the value in the bMaxBurst field is set to zero, then this field can have any value from 0 to 1024 for an isochronous endpoint, and 1 to 1024 for an interrupt endpoint. High Speed/Full Speed mode: For control endpoints, this field is set to 64. For other endpoint types this field can have any value from 0 to 1024. Reset Source: rst_mod_g_rst_n
15:14	MULT	R/W	0h	ISO max burst SuperSpeed mode: A zero-based value that indicates the maximum number of bursts within a service interval that this endpoint supports. This field is only valid for isochronous endpoints. A value of zero indicates that the device supports one Burst of bMaxBurst packets per service interval. The max value that can be set in this field in SuperSpeed is '2'. HS/FS mode: This field indicates how many packets will be transferred during micro frame. In Full-Speed mode only one ISO IN packet can be transferred per endpoint, per frame, thus this field has to be always '0'. In High-Speed mode, up to three ISO IN packets can be transferred per endpoint, per microframe, so the max value that can be set in this field in HighSpeed is '2'. Reset Source: rst_mod_g_rst_n
13:12	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
11:8	MAXBURST	R/W	0h	Maximum Burst size. The maximum number of packets the endpoint can send or receive as part of a burst. Valid values are from 0 to 15. A value of 0 indicates that the endpoint can only burst one packet at a time, and a value of 15 indicates that the endpoint can burst up to 16 packets at a time. For endpoints of type control this is set to 0. This field is meaningfull only in SuperSpeed mode. Reset Source: rst_mod_g_rst_n
7	EPENDIAN	R/W	0h	DMA transfer endianness. When the conversion is ON, the byte order within DWORD is inverted. While the bit is set, the software confirms that the transfer length is a multiplication of 4 bytes. Enabling the conversion is possible only when SUPPORT_ENDIANESS_CONV is defined. By default this parameter is not defined, so endianess conversion is disabled. 0: Endianess conversion OFF 1: Endianess conversion ON Reset Source: rst_mod_g_rst_n
6	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21657. USB3P0SS_CTRL_DEV_EP_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SID_CHK	R/W	0h	SID check[only in SS mode for BULK OUT EP] This field can be set only for SS bulk OUT endpoints with stream support enabled 1] If SID_CHK bit is set, the device checks whether the incoming packets from the host to the particular OUT endpoint have the SID field set to the expected value. If the packet has an expected SID value is then taken and stored in the on-chip device buffers. If the packet has a different SID than expected, then the packet is rejected [NRDY] and the SIDERROR interrupt is reported to the software. The value of the SID to which incoming packets will be compared, are written to the device during sending ERDY TP [EP_CMD.ERDY and EP_CMD.ERDY_SID]. The SID value from the incoming packet that has been rejected and caused the SIDERR interrupt can be read from the EP_STS_SID register. 2] If SID_CHK bit is not set, then each packet from the host is taken to the on-chip buffers is transmitted by the DMA regardless of the SID field in the TD. 0: SID chceck at device input OFF 1: SID chceck at device input ON Reset Source: rst_mod_g_rst_n
4	TDL_CHK	R/W	0h	TDL check[only in SS mode for BULK OUT EP]. This field has to be set for stream capable SS bulk endpoints and it can be set for other bulk endpoint. The OUT bulk endpoints If the TDL_CHK bit is set if the device takes the packets to the OUT endpoint only when the value of the TDL [EP_CMD.TDL] for this endpoint is different from zero. Each received packet for the particular endpoint decrements the value of a TDL. If the TDL_CHK bit is not set, then each packet from the host to the OUT endpoint is taken as long as it free space in the on-chip device buffers. The IN bulk endpoints This bit is is used by USBSS_DEV to set EOB bit when TDL [programmed value] reach zero. 0: Do not check the TDL value when sending/receiving packets to the endpoints 1: Check the TDL value when sending/receiving packets to the endpoint Reset Source: rst_mod_g_rst_n
3	STREAM_EN	R/W	0h	Stream support enable [only in SS mode]. This bit must be set to enable a stream transfes on a bulk endpoint 0: Stream support OFF 1: Stream support ON Reset Source: rst_mod_g_rst_n

Table 14-21657. USB3P0SS_CTRL_DEV_EP_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:1	EPTYPE	R/W	0h	Endpoint type. 0: control, 1: isochronous, 2: bulk, 3: interrupt. Endpoint type is programmable, however, certain types of transmissions require hardware support that must be incorporated prior to implementation. That can be done only for selected endpoints. Selective inclusion of hardware support is to reduce the size of the controller. Accordingly: - Endpoint-type iso should be set by the software only for those endpoints for which isochronous transmission hardware support is enabled. - A bulk endpoint can handle transmission with Bulk Streams support only for those endpoints for which Bulk Stream transmission hardware support is enabled. For detailed description how to implement hardware support for ISO transfers or Bulk Stream transfers see chapter 'Endpoints Implementation'. Reset Source: rst_mod_g_rst_n
0	ENABLE	R/W	0h	Endpoint enable. If endpoint is disabled [the ENABLE bit is cleared], the endpoint will not: - request any interrupts - start any transmission over the DMA Even if Endpoint is disabled, software can set DRDY bit for it, but the DMA transmission will not begin until the endpoint is enabled. 0: disabled 1: enabled Reset value of this bit for EP0 is 1, for other EP's is 0. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.268 USB3P0SS_CTRL_DEV_EP_CMD Register

1 USB3P0SS_CTRL_DEV_EP_CMD Register (Offset = 28h) [reset = 0h]

Endpoint Command Register

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Table 14-21658. Instance Table

Instance Name	Physical Address
USB0	**0F40 0028h**

Figure 14-7158. USB3P0SS_CTRL_DEV_EP_CMD Name Register

31	30	29	28	27	26	25	24
ERDY_SID							
R/W							
0h							
23	22	21	20	19	18	17	16
ERDY_SID							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
DFLUSH	DRDY	REQ_CMPL	RESERVED0	ERDY	CSTALL	SSTALL	EPRST
R/W	R/W	R/W	R	R/W	R/W1TC	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21660. USB3P0SS_CTRL_DEV_EP_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ERDY_SID	R/W	0h	ERDY Stream ID value [used in SS mode]. This field contains SID - it will be sent to host in ERDY packet [by writing '1' to ERDY]. This field is meaningfull only in SuperSpeed mode. Reset Source: rst_mod_g_rst_n
15:8	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
7	DFLUSH	R/W	0h	Data flush. Writing '1' to this bit performs the following actions for particular endpoint: - clears DRDY bit and stops DMA transfer - flush endpoint data from on chip buffers As in case of Endpoint reset [EPRST bit], after endpoint data flush the software is responsible for it to re-set the Endpoint TRADDR. When DFLUSH operation is started ['1' is written], CPU must wait until this bit becomes again '0' [it indicates that HW finishes all internal opertations related to DFLUSH], and only then can proceed with next software operations. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n

Table 14-21660. USB3P0SS_CTRL_DEV_EP_CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DRDY	R/W	0h	Transfer descriptor ready. Transfer Descriptor Ready for selected endpoint [0 - no effect, 1 - starts transfer]. Writing '1' to this bit informs USBSS-DEV that in-system memory has prepared a new Transfer Descriptor for selected endpoints. If an IN endpoint is 'Not Ready' [NRDY=1 in Endpoint Status Register], then setting the DRDY bit [which is proceeded by DMA transfer to the on-chip buffers] will cause the device to send the ERDY packet. If the TRB error occurs, the DRDY bit is cleared and held in the low state until the TRBERR is not cleared [even if the DTRANS bit is set i.e. the Multiple TRB chain mode is enabled]. This bit is duplicated in the Doorbell register. Writing '1' to this bit while DESCMIS interrupt flag is set for the same endpoint will also clear the DESCMIS flag. Reset Source: rst_mod_g_rst_n
5	REQ_CMPL	R/W	0h	Request complete. 0 : no effect 1 : informs device that Request service is complete Bit valid only for endpoint 0. Writing '1' to this bit informs USBSS-DEV that software finished USB request service and device can send ACK answer for the Status Stage within USB request. This bit is automatically cleared by USBSS-DEV after device answers to the status stage with ACK or STALL. Until software do not set this bit, during proceeding current host request, the device will answer to the status stage with NRDY answer. Reset Source: rst_mod_g_rst_n
4	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
3	ERDY	R/W	0h	Send ERDY TP. Writing '1' to this bit forces the device to send ERDY TP with stream ID equal to ERDY_SID. This bit is necessary to support SS bulk stream transfers. This bit is also used during control transfers [in both modes: HS/FS and SS]: writing '1' instruct device controller HW that it can exit from Setup Stage to the Data Stage [or directly to the Status Stage if USB Request is without Data Stage]. However the ERDY packet is only actually sent in SS mode. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
2	CSTALL	R/W1TC	0h	Endpoint STALL clear. Writing '1' to this bit cause the endpoint becames not halted. 0: no effect 1: clears endpoint STALL Reset Source: rst_mod_g_rst_n
1	SSTALL	R/W	0h	Endpoint STALL set. Writing '1' to this bit cause the endpoint is halted. 0: no effect 1: STALLs endpoint Reset Source: rst_mod_g_rst_n

Table 14-21660. USB3P0SS_CTRL_DEV_EP_CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EPRST	R/W	0h	Endpoint reset. 0: no effect 1: resets endpoint This command performs the following actions for particular endpoint: - clears DRDY bit and stops DMA transfer - clears on-chip buffers - clears sequence number in SS mode or Data Toggle in HS/FS mode This command does not clear Endpoint interrupt if already requested [irq[0] pin was asserted] thus it is recommended first to clear all interrupts from endpoint scheduled to reset. When EPRST operation is started ['1' is written], CPU must wait until this bit becomes again '0' [it indicates that HW finishes all internal opertations related to DFLUSH], and only then can proceed with next software operations. Additionally, when DMA already started processing TD for this EP, the EPRST command cause that DMA engine will once more access the descriptor in external memory. After endpoint reset the software is responsible for it to re-set the Endpoint TRADDR. Writing '0 'has no effect. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.269 USB3P0SS_CTRL_DEV_EP_STS Register

1 USB3P0SS_CTRL_DEV_EP_STS Register (Offset = 2Ch) [reset = C00h]

Endpoint Status Register. The EP_STS register consists of two types of bits: - Interrupt flags (RW1C bits). If any of these bit is active (set to '1') and not masked (with an EP_STS_EN register) then the interrupt is requested (irqs[0] line is set to high). To clear these bits, the software must write a '1' at the apptopriate field. - Status bits (RO bits). These bits are not taken into account for interrupt generation (not reported in EP__ISTS register nor on irqs output), and SW is not expected to clear them

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Table 14-21661. Instance Table

Instance Name	Physical Address
USB0	**0F40 002Ch**

Figure 14-7159. USB3P0SS_CTRL_DEV_EP_STS Name Register

31	30	29	28	27	26	25	24
STPWAIT	RESERVED1		OUTQ_VAL	OUTQ_NO			
R/W1TC	R		R	R			
0h	0h		0h	0h			
23	22	21	20	19	18	17	16
RESERVED0				IOT	SPSMST		HOSTPP
R				R/W1TC	R		R
0h				0h	0h		0h
15	14	13	12	11	10	9	8
ISOERR	OUTSMM	SIDERR	PRIME	CCS	BUFFEMPTY	DBUSY	NRDY
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R	R	R	R/W1TC
0h	0h	0h	0h	1h	1h	0h	0h
7	6	5	4	3	2	1	0
TRBERR	MD_EXIT	STREAMR	DESCMIS	ISP	IOC	STALL	SETUP
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21663. USB3P0SS_CTRL_DEV_EP_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	STPWAIT	R/W1TC	0h	Bit used only for EP0. If setup packet is received correctly and stored in the on-chip buffer, this bit is set to 1 and interrupt is generated. Setup packet is applicable only to control transmissions [EP0]. This interrupt can be masked by the corresponding bit in EP_STS_EN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
30:29	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21663. USB3P0SS_CTRL_DEV_EP_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	OUTQ_VAL	R	0h	OUT queue valid flag. This field indicates whether the endpoint number of the OUT packet waiting for transmission by the DMA, is valid or not. In other words, whether the packet queue is not empty. As there is one buffers queue for all Out Endpoints, this field is not endpoint related, and thus it can be read regardless of current value stored in the EP_SEL register. 0 - queue of out packets is empty thus OUTQ_NO is not valid 1 - queue of out packets is not empty thus OUTQ_NO is valid This bit is only a status bit [not an interrupt flag]. Reset Source: rst_mod_g_rst_n
27:24	OUTQ_NO	R	0h	OUT queue endpoint number. This field shows the number of the endpoint to which the packet, received by the host, currently is waiting to be transmitted by the DMA from the on-chip buffers to the system memory. As there is one buffers queue for all Out Endpoints, this field is not endpoint related, and thus it can be read regardless of current value stored in the EP_SEL register. This bit is only a status bit [not an interrupt flag]. Reset Source: rst_mod_g_rst_n
23:20	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
19	IOT	R/W1TC	0h	Interrupt On Transfer complete. This interrupt is generated when the TDL is decremented to zero. It means that the device - does not expect to have more packets from the host [OUT EP] - does not want to send more packets [IN EP] More information can be found in the description of EP_TDL register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
18:17	SPSMST	R	0h	Stream Protocol State Machine State [only for Bulk stream endpoints] This field is valid only for stream capable bulk endpoints and reflects the current state of the Stream Protocol State Machine for selected endpoint: 0 - DISABLED 1 - IDLE 2 - START_STREAM 3 - MOVE_DATA Soft should check if the SPSM is in IDLE state before sending ERDY TP from stream EP [leading to the transition from IDE to START_STREAM] Before software will order to send an ERDY TP from stream capable endpoint [leading to the transition from IDLE to START_STREAM] it should first check if the SPSM is in IDLE state. This bit is only a status bit [not an interrupt flag]. Reset Source: rst_mod_g_rst_n

Table 14-21663. USB3P0SS_CTRL_DEV_EP_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	HOSTPP	R	0h	Host Packet Pending [only for SS mode]. Depending on whether the endpoint is enabled for streams or not, this bit behaves as follows: 1]For stream enabled bulk endpoints [EP_CFG.EPSTREAM_EN bit set]: This bit reflects the PP bit in the last packet received from the host during Move Data state of the DOSPSM for the OUT endpoint. This bit is updated on exit from the MOVE DATA state of the DOSPSM and can be analyzed during servicing MD_EXIT interrupt for BULK OUT endpoint with Stream support enabled. If this bit is set to '0' during MD_EXIT interrupt, it means that the host terminated current stream. If this bit is set to '1' during MD_EXIT interrupt, it means that the host doesn't terminated current stream and still has data for this stream. 2]Non stream bulk endpoints [EP_CFG.EPSTREAM_EN bit not set]: This bit reflects the PP bit in the packets received from the host. This bit is updated as long as the EP_CMD.TDL is nonzero and it can be analyzed during servicing IOT interrupt for BULK endpoints. This bit is only a status bit [not an interrupt flag]. Reset Source: rst_mod_g_rst_n
15	ISOERR	R/W1TC	0h	ISO transmission error. Error of isochronous transmission. This bit is set during data transmission to/from ISO endpoints while the last data transfer at PIPE IF is in current micro frame. For ISO IN endpoints: If host asks for data packet and device is not ready for sent data immediatelly, then ISOERR flag is set for particular endpoint and core sends a 0-length DATA packet to the host. The next data portion transfer [for the next micro frame] from system memory to on-chip buffers is automatically started [when EP_CMD.DRDY bit is set or DMA works in DMULT mode]. For ISO OUT endpoints: When host issues an OUT data packet for the specific endpoint but the OUT buffers are full, then device is unable to receive data packet and the ISOERR flag is set. For more information about ISO trasfer see chapter 'Isochronous Transfers'. This interrupt can be masked by the corresponding bit in EP_STS_EN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
14	OUTSMM	R/W1TC	0h	OUT size mismatch. This bit is set when host sends a different data size than device was anticipating [according to Data Length field in TRB]. In such a case, the DMA updates length field in current TRB, updates TRADDR [next TRB address], and triggers the interrupt. DMA will not start processing TRB ring of this EP until its DRDY is set. This interrupt can be masked by the corresponding bit in EP_STS_EN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n

Table 14-21663. USB3P0SS_CTRL_DEV_EP_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SIDERR	R/W1TC	0h	Stream error [used only in SS mode] If host requested IN [sent OUT] packet with particular Stream ID, and device is actually programmed to transfer packets with different Stream ID [SID written in the EP_CMD.ERDY_SID field] the host IN request [OUT packet] is rejected [NRDY] and the SIDERR interrupt is requested. In case of IN direction, the SIDERR interrupt will not be requested when device is not prepared for any transfer [EP_CMD.TDL= 0 for this endpoint]. In this case [and additionally when EP_CMD.DRDY= 0 and EP_STS.DBUSY=0], the DESCMIS interrupt will be requested. This interrupt can be masked by the corresponding bit in EP_STS_EN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
12	PRIME	R/W1TC	0h	Prime [used only in SS mode]. This bit is set when the device receives the packet with PRIME ID. This interrupt can be masked by the corresponding bit in EP_STS_EN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
11	CCS	R	1h	Current Cycle Status. Informs about current value of C bit corresponding to DMA ownership of TRBs for selected endpoint. For more information about TRBs C bit see chapter 2.11.3. This bit is only a status bit [not an interrupt flag]. Reset Source: rst_mod_g_rst_n
10	BUFFEMPTY	R	1h	Endpoint Buffer Empty. When this bit is set to '1', there are no packets for the particular endpoint in the on-chip buffers. This bit is only a status bit [not an interrupt flag]. Reset Source: rst_mod_g_rst_n
9	DBUSY	R	0h	DMA busy. This bit is set to '1' while the DMA services the endpoint. Through the service means either actual transmission of data between on-chip cache and system memory for particular endpoint or a pending data transmission which has already begun but was interrupted by endpoint with a higher priority. Such pending transmissions will begin automatically themselves after these higher priority. This bit is only a status bit [not an interrupt flag]. Reset Source: rst_mod_g_rst_n
8	NRDY	R/W1TC	0h	Not ready [used only in SS mode]. This bit is automatically set to 1 when for some reason endpoint enters Flow Control. If ERDY is sent automatically by the endpoint [what is done when current TDL value is greater then zero], this interrupt bit is not automatically cleared [although the endpoint itself leaves FlowControl]. Note: For BULK OUT endpoints with TDL_CHK bit seting this interrupt should be used instead of DESCMIS interrupt. See also DESCMIS description. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n

Table 14-21663. USB3P0SS_CTRL_DEV_EP_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TRBERR	R/W1TC	0h	TRB error. This bit is set if DMA read corrupted TRB [wrong C bit value or TRB type]. Address of the TRB is stored in the EP_TRADDR register. This interrupt can be masked by the corresponding bit in EP_STS_EN register. If this error occurs, the bit DRDY is cleared and held in the low state until the TRBERR is not cleared. To start the DMA again, the software has to clear this interrupt and set the DRDY bit once more. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
6	MD_EXIT	R/W1TC	0h	EXIT from MOVE DATA State [used only for stream transfers in SS mode] This bit is set to '1' if stream capable endpoint exits from MOVE DATA state of Bulk IN/OUT Stream Ptrotocol State Machine [ISPSM/OSPSM]. Stream support is class-dependent. This interrupt can be masked by the corresponding bit in MD_EXITEN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
5	STREAMR	R/W1TC	0h	Stream Rejected [used only in SS mode]. This bit is set to '1' if device tries to initiate stream number and host does not accept it. Stream support is class-dependent. This interrupt can be masked by the corresponding bit in STREAMREN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
4	DESCMIS	R/W1TC	0h	Transfer descriptor missing. This bit is set to 1 and interrupt is generated when any of the following conditions are met: - device is requested to send data to host and none of Transfer Descriptor is prepared [IN transfer] - device receives OUT packet and cannot transmit it using DMA as Transfer Descriptor has not been prepared [DRDY was not set] for it [OUT transfer] Note1: This interrupt is not generated for ISO IN endpoints. For such endpoints the ISOERR interrupt should be used. Note2: DMA will not start operating on transfer descriptor array until the OUT packet is received [or host requests IN packet] and processor has not previously notified DMA [by writing to EP_CMD register of DRDY register]. Note2: For BULK OUT endpoints with TDL_CHK bit set this interrupt will not by requested as device will not accept any packet from host when TRB is not prepared [and TDL is not written with non-zero value]. In this case the NRDY interrupt should be used instead of DESMIS. Writing '1' to this bit or writing '1' to EP_CMD.DRDY bit of endpoints which generated interrupt will delete the interrupt. This interrupt can be masked by the corresponding bit in EP_STS_EN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n

Table 14-21663. USB3P0SS_CTRL_DEV_EP_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ISP	R/W1TC	0h	Interrupt on Short Packet. This bit is set to 1 and interrupt is generated when a transfer containing less data than MaxPacket for a given endpoint has been completed and transfer descriptor has been updated.Enabling or disabling of interrupt is realized by ISP bit in transfer descriptor. Additionally, this interrupt can be masked for a particular endpoint in EP__ISTS register. When in given transfer descriptor both interrupts are enabled [IOC and ISP], then in the case of short packet only one interrupt is generated - SP. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
2	IOC	R/W1TC	0h	Interrupt On Complete When DMA transfer is completed and transfer descriptor is updated, then this bit is set to 1 and interrupt is generated. Enabling or disabling of this interrupt is realized by IOC bit in transfer descriptor. Additionally, this interrupt can be masked for a particular endpoint in EP__ISTS register. When in given transfer descriptor both interrupts [IOC and ISP interrupts] are enabled, then in the case of short packet, only one interrupt is generated - SP. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n
1	STALL	R	0h	Endpoint STALL status 0 - endpoint is not stalled 1 - endpoint is stalled This bit is not treated as an interrupt [not reported in the EP__ISTS register]. This bit is read-only. Reset Source: rst_mod_g_rst_n
0	SETUP	R/W1TC	0h	Setup transfer complete. Bit used only for EP0. If setup type transmission has been completed and data from host has been received and copied to system memory, this bit is set to '1' and interrupt is generated. Setup packet is applicable only to control transmissions [EP0]. This interrupt can be masked by the corresponding bit in EP_STS_EN register. Writing '1' to this bit clears the interrupt. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.270 USB3P0SS_CTRL_DEV_EP_STS_SID Register

1 USB3P0SS_CTRL_DEV_EP_STS_SID Register (Offset = 30h) [reset = 0h]

Endpoint Status Register

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Table 14-21664. Instance Table

Instance Name	Physical Address
USB0	**0F40 0030h**

Figure 14-7160. USB3P0SS_CTRL_DEV_EP_STS_SID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SID							
R							
0h							

Table 14-21666. USB3P0SS_CTRL_DEV_EP_STS_SID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
15:0	SID	R	0h	Stream ID [used only in SS mode]. Stream ID of packet, which generates interrupt. The interrupts that update the SID field are: - SIDERR for EP OUT - SIDERR/DESCMIS for EP IN For the above interrupts, the values of the SID field reflects: - in case of SIDERR for EP OUT this field reflects the Stream ID of OUT packet sent by host which was rejected by the device, due to SID_CHK bit set - in case of SIDERR/DESCMIS for EP IN this field reflects the Stream ID of ACK TP sent by host which was rejected by the device. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.271 USB3P0SS_CTRL_DEV_EP_STS_EN Register

1 USB3P0SS_CTRL_DEV_EP_STS_EN Register (Offset = 34h) [reset = 0h]

Endpoint Status Register Enable

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Table 14-21667. Instance Table

Instance Name	Physical Address
USB0	0F40 0034h

Figure 14-7161. USB3P0SS_CTRL_DEV_EP_STS_EN Name Register

31	30	29	28	27	26	25	24
STPWAITEN	RESERVED3						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED3				IOTEN	RESERVED2		
R				R/W	R		
0h				0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ISOERREN	OUTSMMEN	SIDERREN	PRIMEEN	RESERVED1			NRDYEN
R/W	R/W	R/W	R/W	R			R/W
0h	0h	0h	0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRBERREN	MD_EXITEN	STREAMREN	DESCMISEN	RESERVED0			SETUPEN
R/W	R/W	R/W	R/W	R			R/W
0h	0h	0h	0h	0h			0h

Table 14-21669. USB3P0SS_CTRL_DEV_EP_STS_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	STPWAITEN	R/W	0h	Setup Wait interrupt enable. This bit enables the STPWAIT interrupt. Valid only for EP0 Reset Source: rst_mod_g_rst_n
30:20	RESERVED3	R	0h	Reserved field. Write ignored. 0 when read
19	IOTEN	R/W	0h	Interrupt on Transmission complete enable. This bit enables the IOT interrupt. Reset Source: rst_mod_g_rst_n
18:16	RESERVED2	R	0h	Reserved field. Write ignored. 0 when read
15	ISOERREN	R/W	0h	ISO transmission error enable. This bit enables the ISOERR interrupt. Reset Source: rst_mod_g_rst_n
14	OUTSMMEN	R/W	0h	OUT size mismatch enable. This bit enables the OUTSMM interrupt. Reset Source: rst_mod_g_rst_n
13	SIDERREN	R/W	0h	Stream error enable. This bit enables the SIDERR interrupt. Reset Source: rst_mod_g_rst_n
12	PRIMEEN	R/W	0h	Prime enable. This bit enables the PRIME interrupt. Reset Source: rst_mod_g_rst_n
11:9	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21669. USB3P0SS_CTRL_DEV_EP_STS_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NRDYEN	R/W	0h	NRDY enable. This bit enables the NRDY interrupt. Reset Source: rst_mod_g_rst_n
7	TRBERREN	R/W	0h	TRB enable. This bit enables the TRBERR interrupt. Reset Source: rst_mod_g_rst_n
6	MD_EXITEN	R/W	0h	Move Data Exit enable. This bit enables the MD_EXIT interrupt. Reset Source: rst_mod_g_rst_n
5	STREAMREN	R/W	0h	Stream Rejected enable. This bit enables the STREAMR interrupt. Reset Source: rst_mod_g_rst_n
4	DESCMISEN	R/W	0h	OUT transfer missing descriptor enable. This bit enables the DESCMIS interrupt. Reset Source: rst_mod_g_rst_n
3:1	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
0	SETUPEN	R/W	0h	Setup transfer complete. This bit enables the SETUP interrupt. Valid only for EP0. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.272 USB3P0SS_CTRL_DEV_DRBL Register

1 USB3P0SS_CTRL_DEV_DRBL Register (Offset = 38h) [reset = 0h]

Doorbell Register - used for initiating transfers with one access to USBSS-DEV, without use of the EP_SEL register(+EP_CMD.DRDY)

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Table 14-21670. Instance Table

Instance Name	Physical Address
USB0	0F40 0038h

Figure 14-7162. USB3P0SS_CTRL_DEV_DRBL Name Register

31	30	29	28	27	26	25	24
DRBL15I	DRBL14I	DRBL13I	DRBL12I	DRBL11I	DRBL10I	DRBL9I	DRBL8I
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
DRBL7I	DRBL6I	DRBL5I	DRBL4I	DRBL3I	DRBL2I	DRBL1I	DRBL0I
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
DRBL15O	DRBL14O	DRBL13O	DRBL12O	DRBL11O	DRBL10O	DRBL9O	DRBL8O
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
DRBL7O	DRBL6O	DRBL5O	DRBL4O	DRBL3O	DRBL2O	DRBL1O	DRBL0O
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21672. USB3P0SS_CTRL_DEV_DRBL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRBL15I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
30	DRBL14I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
29	DRBL13I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
28	DRBL12I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
27	DRBL11I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
26	DRBL10I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
25	DRBL9I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
24	DRBL8I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n

Table 14-21672. USB3P0SS_CTRL_DEV_DRBL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	DRBL7I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
22	DRBL6I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
21	DRBL5I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
20	DRBL4I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
19	DRBL3I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
18	DRBL2I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
17	DRBL1I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
16	DRBL0I	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
15	DRBL15O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
14	DRBL14O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
13	DRBL13O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
12	DRBL12O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
11	DRBL11O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
10	DRBL10O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
9	DRBL9O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
8	DRBL8O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
7	DRBL7O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
6	DRBL6O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
5	DRBL5O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
4	DRBL4O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
3	DRBL3O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
2	DRBL2O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n

Table 14-21672. USB3P0SS_CTRL_DEV_DRBL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DRBL1O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n
0	DRBL0O	R/W1TS	0h	Dorbel Bit - used for initiating transfers for selected Endpoint Reset Source: rst_mod_g_rst_n

14.9.2.3.2.273 USB3P0SS_CTRL_DEV_EP_IEN Register

1 USB3P0SS_CTRL_DEV_EP_IEN Register (Offset = 3Ch) [reset = 10001h]

Endpoints Interrupt Enable Register (1 - enables interrupt, 0 - disables interrupt)

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Table 14-21673. Instance Table

Instance Name	Physical Address
USB0	**0F40 003Ch**

Figure 14-7163. USB3P0SS_CTRL_DEV_EP_IEN Name Register

31	30	29	28	27	26	25	24
EINEN15	EINEN14	EINEN13	EINEN12	EINEN11	EINEN10	EINEN9	EINEN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EINEN7	EINEN6	EINEN5	EINEN4	EINEN3	EINEN2	EINEN1	EINEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h
15	14	13	12	11	10	9	8
EOUTEN15	EOUTEN14	EOUTEN13	EOUTEN12	EOUTEN11	EOUTEN10	EOUTEN9	EOUTEN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EOUTEN7	EOUTEN6	EOUTEN5	EOUTEN4	EOUTEN3	EOUTEN2	EOUTEN1	EOUTEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h

Table 14-21675. USB3P0SS_CTRL_DEV_EP_IEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EINEN15	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
30	EINEN14	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
29	EINEN13	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
28	EINEN12	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
27	EINEN11	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
26	EINEN10	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n

Table 14-21675. USB3P0SS_CTRL_DEV_EP_IEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	EINEN9	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
24	EINEN8	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
23	EINEN7	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
22	EINEN6	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
21	EINEN5	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
20	EINEN4	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
19	EINEN3	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
18	EINEN2	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
17	EINEN1	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
16	EINEN0	R/W	1h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
15	EOUTEN15	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
14	EOUTEN14	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
13	EOUTEN13	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
12	EOUTEN12	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
11	EOUTEN11	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
10	EOUTEN10	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n

Table 14-21675. USB3P0SS_CTRL_DEV_EP_IEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EOUTEN9	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
8	EOUTEN8	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
7	EOUTEN7	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
6	EOUTEN6	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
5	EOUTEN5	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
4	EOUTEN4	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
3	EOUTEN3	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
2	EOUTEN2	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
1	EOUTEN1	R/W	0h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n
0	EOUTEN0	R/W	1h	Endpoints Interrupt Enable Bit [1 - enables interrupt, 0 - disables interrupt] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.274 USB3P0SS_CTRL_DEV_EP_ISTS Register

1 USB3P0SS_CTRL_DEV_EP_ISTS Register (Offset = 40h) [reset = 0h]

Endpoints Interrupt Status Register. The EIN.n/EOUT.n bit corresponds to interrupt request of n-number endpoint. The reason for interrupt can be read from EP_STS. Interrupt remains valid until given EP_STS.n is cleared by writing in the corresponding bit. NOTE: before access to EP_STS register, EP_SEL must be written with appropriate endpoint number

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Table 14-21676. Instance Table

Instance Name	Physical Address
USB0	**0F40 0040h**

Figure 14-7164. USB3P0SS_CTRL_DEV_EP_ISTS Name Register

31	30	29	28	27	26	25	24
EIN15	EIN14	EIN13	EIN12	EIN11	EIN10	EIN9	EIN8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EIN7	EIN6	EIN5	EIN4	EIN3	EIN2	EIN1	EIN0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EOUT15	EOUT14	EOUT13	EOUT12	EOUT11	EOUT10	EOUT9	EOUT8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EOUT7	EOUT6	EOUT5	EOUT4	EOUT3	EOUT2	EOUT1	EOUT0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21678. USB3P0SS_CTRL_DEV_EP_ISTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EIN15	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
30	EIN14	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
29	EIN13	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
28	EIN12	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
27	EIN11	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
26	EIN10	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
25	EIN9	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n

Table 14-21678. USB3P0SS_CTRL_DEV_EP_ISTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	EIN8	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
23	EIN7	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
22	EIN6	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
21	EIN5	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
20	EIN4	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
19	EIN3	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
18	EIN2	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
17	EIN1	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
16	EIN0	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
15	EOUT15	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
14	EOUT14	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
13	EOUT13	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
12	EOUT12	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
11	EOUT11	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
10	EOUT10	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
9	EOUT9	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
8	EOUT8	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
7	EOUT7	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
6	EOUT6	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
5	EOUT5	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
4	EOUT4	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
3	EOUT3	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n

Table 14-21678. USB3P0SS_CTRL_DEV_EP_ISTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOUT2	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
1	EOUT1	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n
0	EOUT0	R	0h	Endpoints Interrupt Status Bit. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.275 USB3P0SS_CTRL_DEV_USB_PWR Register

1 USB3P0SS_CTRL_DEV_USB_PWR Register (Offset = 44h) [reset = 2h]

Global power configuration register

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Table 14-21679. Instance Table

Instance Name	Physical Address
USB0	**0F40 0044h**

Figure 14-7165. USB3P0SS_CTRL_DEV_USB_PWR Name Register

31	30	29	28	27	26	25	24
FAST_REG_ACCESS	FAST_REG_ACCESS_STAT	RESERVED1					
R/W	R	R					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1						STB_CLK_SWITCH_DONE	STB_CLK_SWITCH_EN
R						R	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED0						PSO_DS	PSO_EN
R						R/W1TS	R/W1TC
0h						1h	0h

Table 14-21681. USB3P0SS_CTRL_DEV_USB_PWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FAST_REG_ACCESS	R/W	0h	Fast Registers Access. When Device Port is in a low power state [U3/L2/Not Connected], accesses to registers listed in section 2.3 of USBSS-DEV design specification may take long time. In order to enable fast register access in that case, user can use this register in the following way: - set FAST_REG_ACCESS bit - wait until FAST_REG_ACCESS_STAT bit is set - perform required accesses - clear FAST_REG_ACCESS bit Note that to enable USBSS-DEV low power state entry [U3/L2], the FAST_REG_ACCESS bit has to be cleared. Reset Source: rst_mod_g_rst_n
30	FAST_REG_ACCESS_STAT	R	0h	Fast Registers Access status. This bit informs if Fast Registers Access is enabled. It should be used as described in FAST_REG_ACCESS bit. Reset Source: rst_mod_g_rst_n
29:10	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21681. USB3P0SS_CTRL_DEV_USB_PWR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	STB_CLK_SWITCH_DONE	R	0h	Status bit indicating that operation required by STB_CLK_SWITCH_EN write is completed. This bit is optional and implemented only when support for OTG is implemented [indicated by OTG_READY bit set to 1]. Reset Source: rst_mod_g_rst_n
8	STB_CLK_SWITCH_EN	R/W	0h	Enables turning-off Reference Clock. This bit is optional and implemented only when support for OTG is implemented [indicated by OTG_READY bit set to 1]. Should not be used when PHY Reference clock control is not supported Reset Source: rst_mod_g_rst_n
7:2	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
1	PSO_DS	R/W1TS	1h	Power Shut Off capability disable. Writing '1' to this bit disables power domains switching capability and clears the PSO_EN bit. It is recommended to set this bit after during U3EXTI interrupt service. Reset Source: rst_mod_g_rst_n
0	PSO_EN	R/W1TC	0h	Power Shut Off capability enable. Writing '1' to this bit enables dower domains switching capability and clears the PSO_DS bit. The Domain will be switched off if both PSO_EN will be set and the USB controller will be in the in the U3 state. It is recommended to set this bit in U3ENTI interrupt service, after software ensures that no data transfer is pending. If this bit will be always set, the controller will automatically switch off the power in the switchable PD after USB controller will enter U3 state. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.276 USB3P0SS_CTRL_DEV_USB_CONF2 Register

1 USB3P0SS_CTRL_DEV_USB_CONF2 Register (Offset = 48h) [reset = 0h]

USB configuration register 2

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Table 14-21682. Instance Table

Instance Name	Physical Address
USB0	**0F40 0048h**

Figure 14-7166. USB3P0SS_CTRL_DEV_USB_CONF2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							AHB_RETRY_EN
R							R/W
0h							0h

Table 14-21684. USB3P0SS_CTRL_DEV_USB_CONF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
0	AHB_RETRY_EN	R/W	0h	AHB retry enable. This bit enables the AHB retrys for AHB slave interface. This bit has no effect when AHB slave interface is not implemented. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.277 USB3P0SS_CTRL_DEV_USB_CAP1 Register

1 USB3P0SS_CTRL_DEV_USB_CAP1 Register (Offset = 4Ch) [reset = 19203324h]

USB Capability Register 1

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Table 14-21685. Instance Table

Instance Name	Physical Address
USB0	**0F40 004Ch**

Figure 14-7167. USB3P0SS_CTRL_DEV_USB_CAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED			TDL_FROM_TRB	OTG_READY	U2PHY_WIDTH	U2PHY_TYPE	U2PHY_EN
R			R	R	R	R	R
0h			1h	1h	0h	0h	1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
U3PHY_WIDTH				U3PHY_TYPE			
R				R			
2h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMA_WIDTH				DMA_TYPE			
R				R			
3h				3h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SFR_WIDTH				SFR_TYPE			
R				R			
2h				4h			

Table 14-21687. USB3P0SS_CTRL_DEV_USB_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	R	0h	This field is reserved and it is always 0 when reading.
28	TDL_FROM_TRB	R	1h	This field informs if device controller supports automatic internal TDL calculation basing on the size provided in TRB for DMULT mode: - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation Reset Source: rst_mod_g_rst_n
27	OTG_READY	R	1h	This field informs if device is OTG ready: - pure device mode: 0x0, - some features and ports for CDNS USB OTG controller are implemented: 0x1. Reset Source: rst_mod_g_rst_n
26	U2PHY_WIDTH	R	0h	USB2 PHY Interface width. This field reflects width of USB2 PHY interface implemented: - 8 bit interface: 0x0, - 16 bit interface: 0x1. Note: The ULPI interface is always 8-bit wide. Reset Source: rst_mod_g_rst_n

Table 14-21687. USB3P0SS_CTRL_DEV_USB_CAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	U2PHY_TYPE	R	0h	USB2 PHY Interface type. This field reflects type of USB2 PHY interface implemented: - UTMI: 0x0, - ULPI: 0x1. Reset Source: rst_mod_g_rst_n
24	U2PHY_EN	R	1h	USB2 PHY Interface enable. This field informs if USB2 PHY interface is implemented: - interface NOT implemented: 0x0, - interface implemented: 0x1. Reset Source: rst_mod_g_rst_n
23:20	U3PHY_WIDTH	R	2h	USB3 PHY Interface width. This field reflects width of USB3 PHY interface implemented: - 0x0: 8 bit PIPE interface, - 0x1: 16 bit PIPE interface, - 0x2: 32 bit PIPE interface, - 0x3: 64 bit PIPE interface, - 0x4-0xF: reserved. Note: When SSIC interface is implemented this field shows the width of internal PIPE interface. The RMMI interface is always 20-bit wide. Reset Source: rst_mod_g_rst_n
19:16	U3PHY_TYPE	R	0h	USB3 PHY Interface type. This field reflects type of USB3 PHY interface implemented: - 0x0: USB PIPE, - 0x1: RMMI, - 0x2-0xF: reserved Reset Source: rst_mod_g_rst_n
15:12	DMA_WIDTH	R	3h	DMA Interface width. This field reflects width of DMA interface implemented: - 0x0: reserved, - 0x1: reserved, - 0x2: 32 bit interface, - 0x3: 64 bit interface, - 0x4-0xF: reserved Reset Source: rst_mod_g_rst_n
11:8	DMA_TYPE	R	3h	DMA Interface type. This field reflects type of DMA interface implemented: - 0x0: OCP, - 0x1: AHB, - 0x2: PLB, - 0x3: AXI, - 0x4-0xF: reserved Reset Source: rst_mod_g_rst_n
7:4	SFR_WIDTH	R	2h	SFR Interface width. This field reflects width of SFR interface implemented: - 0x0: 8 bit interface, - 0x1: 16 bit interface, - 0x2: 32 bit interface, - 0x3: 64 bit interface, - 0x4-0xF: reserved Reset Source: rst_mod_g_rst_n
3:0	SFR_TYPE	R	4h	SFR Interface type. This field reflects type of SFR interface implemented: 0x0 - OCP, 0x1 - AHB, 0x2 - PLB, 0x3 - AXI, 0x4 - APB, 0x5-0xF - reserved. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.278 USB3P0SS_CTRL_DEV_USB_CAP2 Register

1 USB3P0SS_CTRL_DEV_USB_CAP2 Register (Offset = 50h) [reset = C00h]

USB Capability Register

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Table 14-21688. Instance Table

Instance Name	Physical Address
USB0	**0F40 0050h**

Figure 14-7168. USB3P0SS_CTRL_DEV_USB_CAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED			MAX_MEM_SIZE				
R			R				
0h			Ch				

7	6	5	4	3	2	1	0
ACTUAL_MEM_SIZE							
R							
0h							

Table 14-21690. USB3P0SS_CTRL_DEV_USB_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	R	0h	This field is reserved and it is always 0 when reading.
12:8	MAX_MEM_SIZE	R	Ch	Max supported mem size. This field reflects width of on-chip RAM address bus width, which determines max supported mem size: 0x0-0x7 reserved, 0x8 - support for 4kB mem, 0x9 - support for 8kB mem, 0xA - support for 16kB mem, 0xB - support for 32kB mem, 0xC - support for 64kB mem, 0xD - support for 128kB mem, 0xE - support for 256kB mem, 0xF - reserved. Reset Source: rst_mod_g_rst_n
7:0	ACTUAL_MEM_SIZE	R	0h	The actual size of the connected On-chip RAM memory in kB: - 0 means 256 kB [max supported mem size] - value other than 0 reflects the mem size in kB. This value reflects the CDNS_USBSSDEV_ATTACHED_MEM_SIZE parameter defined in the usbss_dev_defines.v file. This value has to be adequately set before synthesis by engineer who connects the on-chip memory for controller. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.279 USB3P0SS_CTRL_DEV_USB_CAP3 Register

1 USB3P0SS_CTRL_DEV_USB_CAP3 Register (Offset = 54h) [reset = FFFFFFFFh]

USB Capability Register 3. Implemented Endpoints. EPIN.n/EPOUT.n bit informs if n-number endpoint is implemented in the hardware. Default: all EP

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Table 14-21691. Instance Table

Instance Name	Physical Address
USB0	**0F40 0054h**

Figure 14-7169. USB3P0SS_CTRL_DEV_USB_CAP3 Name Register

31	30	29	28	27	26	25	24
EPIN_N							
R							
FFFFh							
23	22	21	20	19	18	17	16
EPIN_N							
R							
FFFFh							
15	14	13	12	11	10	9	8
EPOUT_N							
R							
FFFFh							
7	6	5	4	3	2	1	0
EPOUT_N							
R							
FFFFh							

Table 14-21693. USB3P0SS_CTRL_DEV_USB_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	EPIN_N	R	FFFFh	Endpoints IN Reset Source: rst_mod_g_rst_n
15:0	EPOUT_N	R	FFFFh	Endpoints OUT Reset Source: rst_mod_g_rst_n

14.9.2.3.2.280 USB3P0SS_CTRL_DEV_USB_CAP4 Register

1 USB3P0SS_CTRL_DEV_USB_CAP4 Register (Offset = 58h) [reset = FFFEFFFEh]

ISO HW support for Endpoints implemented EPINI.n/EPOUTI.n bit informs if n- number endpoint has ISO support implemented in the hardware. Note that EP0 is not intended for isochronous transfers, so both EPINI.0 and EPOUTI.0 must be always set to 0.

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Table 14-21694. Instance Table

Instance Name	Physical Address
USB0	0F40 0058h

Figure 14-7170. USB3P0SS_CTRL_DEV_USB_CAP4 Name Register

31	30	29	28	27	26	25	24
EPINI_N							
R							
FFFEh							
23	22	21	20	19	18	17	16
EPINI_N							
R							
FFFEh							
15	14	13	12	11	10	9	8
EPOUTI_N							
R							
FFFEh							
7	6	5	4	3	2	1	0
EPOUTI_N							
R							
FFFEh							

Table 14-21696. USB3P0SS_CTRL_DEV_USB_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	EPINI_N	R	FFFEh	Endpoints IN Reset Source: rst_mod_g_rst_n
15:0	EPOUTI_N	R	FFFEh	Endpoints OUT Reset Source: rst_mod_g_rst_n

14.9.2.3.2.281 USB3P0SS_CTRL_DEV_USB_CAP5 Register

1 USB3P0SS_CTRL_DEV_USB_CAP5 Register (Offset = 5Ch) [reset = FFFEFFFEh]

Bulk Stream HW support for Endpoints implemented. EPINS.n/EPOUTS.n bit informs if n-number endpoint has Bulk Stream support implemented in the hardware. Note that EP0 is not intended for stream transfers, so both EPINS.0 and EPOUTS.0 must be always set to '0'.

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Table 14-21697. Instance Table

Instance Name	Physical Address
USB0	**0F40 005Ch**

Figure 14-7171. USB3P0SS_CTRL_DEV_USB_CAP5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">EPINI_N</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFEh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">EPINI_N</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFEh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EPOUTI_N</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFEh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EPOUTI_N</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFEh</td></tr>
</table>

Table 14-21699. USB3P0SS_CTRL_DEV_USB_CAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	EPINI_N	R	FFFEh	Endpoints IN Reset Source: rst_mod_g_rst_n
15:0	EPOUTI_N	R	FFFEh	Endpoints OUT Reset Source: rst_mod_g_rst_n

14.9.2.3.2.282 USB3P0SS_CTRL_DEV_USB_CAP6 Register

1 USB3P0SS_CTRL_DEV_USB_CAP6 Register (Offset = 60h) [reset = 2450Dh]

Device controller version.

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Table 14-21700. Instance Table

Instance Name	Physical Address
USB0	**0F40 0060h**

Figure 14-7172. USB3P0SS_CTRL_DEV_USB_CAP6 Name Register

31	30	29	28	27	26	25	24
VERSION							
R							
2450Dh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VERSION							
R							
2450Dh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VERSION							
R							
2450Dh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VERSION							
R							
2450Dh							

Table 14-21702. USB3P0SS_CTRL_DEV_USB_CAP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VERSION	R	2450Dh	Device controller version. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.283 USB3P0SS_CTRL_DEV_USB_CPKT1 Register

1 USB3P0SS_CTRL_DEV_USB_CPKT1 Register (Offset = 64h) [reset = 0h]

Custom Packet value. If the USB_CMD.SPKT bit is set, then this field is sent to the host as DWORD 0 in the Transaction Packet. Refer to USB3.0 specification, chapter 8.5 Transaction Packet for more details. This field must be filled up before the USB_CMD.SPKT bit is set, and cannot be changed while USB_CMD.SPKT bit is not zero (TP is being sent by the device controller)

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Table 14-21703. Instance Table

Instance Name	Physical Address
USB0	**0F40 0064h**

Figure 14-7173. USB3P0SS_CTRL_DEV_USB_CPKT1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CPKT1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CPKT1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CPKT1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CPKT1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21705. USB3P0SS_CTRL_DEV_USB_CPKT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPKT1	R/W	0h	Custom Packet value 1. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.284 USB3P0SS_CTRL_DEV_USB_CPKT2 Register

1 USB3P0SS_CTRL_DEV_USB_CPKT2 Register (Offset = 68h) [reset = 0h]

Custom Packet value. If the USB_CMD.SPKT bit is set, then this field is sent to the host as DWORD 1 in the Transaction Packet. Refer to USB3.0 specification, chapter 8.5 Transaction Packet for more details. This field must be filled up before the USB_CMD.SPKT bit is set, and cannot be changed while USB_CMD.SPKT bit is not zero (TP is being sent by the device controller)

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Table 14-21706. Instance Table

Instance Name	Physical Address
USB0	**0F40 0068h**

Figure 14-7174. USB3P0SS_CTRL_DEV_USB_CPKT2 Name Register

31	30	29	28	27	26	25	24
CPKT2							
R/W							
0h							
23	22	21	20	19	18	17	16
CPKT2							
R/W							
0h							
15	14	13	12	11	10	9	8
CPKT2							
R/W							
0h							
7	6	5	4	3	2	1	0
CPKT2							
R/W							
0h							

Table 14-21708. USB3P0SS_CTRL_DEV_USB_CPKT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPKT2	R/W	0h	Custom Packet value 2. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.285 USB3P0SS_CTRL_DEV_USB_CPKT3 Register

1 USB3P0SS_CTRL_DEV_USB_CPKT3 Register (Offset = 6Ch) [reset = 0h]

Custom Packet value. If the USB_CMD.SPKT bit is set, then this field is sent to the host as DWORD 2 in the Transaction Packet. Refer to USB3.0 specification, chapter 8.5 Transaction Packet for more details. This field must be filled up before the USB_CMD.SPKT bit is set, and cannot be changed while USB_CMD.SPKT bit is not zero (TP is being sent by the device controller)

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Table 14-21709. Instance Table

Instance Name	Physical Address
USB0	**0F40 006Ch**

Figure 14-7175. USB3P0SS_CTRL_DEV_USB_CPKT3 Name Register

31	30	29	28	27	26	25	24
CPKT3							
R/W							
0h							
23	22	21	20	19	18	17	16
CPKT3							
R/W							
0h							
15	14	13	12	11	10	9	8
CPKT3							
R/W							
0h							
7	6	5	4	3	2	1	0
CPKT3							
R/W							
0h							

Table 14-21711. USB3P0SS_CTRL_DEV_USB_CPKT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPKT3	R/W	0h	Custom Packet value 3. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.286 USB3P0SS_CTRL_DEV_EP_DMA_EXT_ADDR Register

1 USB3P0SS_CTRL_DEV_EP_DMA_EXT_ADDR Register (Offset = 70h) [reset = 0h]

Upper address for DMA This register is optional and is implemented only if the DMA supports address bigger than 32-bit address

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Table 14-21712. Instance Table

Instance Name	Physical Address
USB0	0F40 0070h

Figure 14-7176. USB3P0SS_CTRL_DEV_EP_DMA_EXT_ADDR Name Register

31	30	29	28	27	26	25	24
RESERVED0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED0							
R							
0h							
15	14	13	12	11	10	9	8
EP_DMA_ADDR_H							
R/W							
0h							
7	6	5	4	3	2	1	0
EP_DMA_ADDR_H							
R/W							
0h							

Table 14-21714. USB3P0SS_CTRL_DEV_EP_DMA_EXT_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
15:0	EP_DMA_ADDR_H	R/W	0h	Transfer Ring address. This register specify upper [above 32-bits] DMA address for each endpoint separatelly. This part of DMA address, is not modified by the DMA. CPU can use this register [read it or write to it] only when endpoint is selected [using EP_SEL register] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.287 USB3P0SS_CTRL_DEV_BUF_ADDR Register

1 USB3P0SS_CTRL_DEV_BUF_ADDR Register (Offset = 74h) [reset = 0h]

Address for On-chip Buffer operations. Used for accessing device controller on-chip memory via SFR interface. This register is used together with BUF_DATA and BUF_CTRL registers.

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Table 14-21715. Instance Table

Instance Name	Physical Address
USB0	0F40 0074h

Figure 14-7177. USB3P0SS_CTRL_DEV_BUF_ADDR Name Register

31	30	29	28	27	26	25	24
BUF_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
BUF_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
BUF_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
BUF_ADDR							
R/W							
0h							

Table 14-21717. USB3P0SS_CTRL_DEV_BUF_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUF_ADDR	R/W	0h	On-chip Memory Address. This register specify the address of the on-chip memory cell which is accessed using BUF_CTRL register. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.288 USB3P0SS_CTRL_DEV_BUF_DATA Register

1 USB3P0SS_CTRL_DEV_BUF_DATA Register (Offset = 78h) [reset = 0h]

Data for On-chip Buffer operations. Used for accessing device controller on-chip memory via SFR interface. This register is used together with BUF_ADDR and BUF_CTRL registers.

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Table 14-21718. Instance Table

Instance Name	Physical Address
USB0	0F40 0078h

Figure 14-7178. USB3P0SS_CTRL_DEV_BUF_DATA Name Register

31	30	29	28	27	26	25	24
BUF_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
BUF_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
BUF_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
BUF_DATA							
R/W							
0h							

Table 14-21720. USB3P0SS_CTRL_DEV_BUF_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUF_DATA	R/W	0h	Data for On-chip Buffer operations. This register specify the address of the on-chip memory cell which is accessed using BUF_CTRL register. For write operation this register must be written before WRITE command is issued using BUF_CTRL register. For read operation, this register must be read after READ command is issued using BUF_CTRL register. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.289 USB3P0SS_CTRL_DEV_BUF_CTRL Register

1 USB3P0SS_CTRL_DEV_BUF_CTRL Register (Offset = 7Ch) [reset = 0h]

On-chip Buffer Access register. Used for accessing device controller on-chip memory via SFR interface. This register is used together with BUF_ADDR and BUF_DATA registers.

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Table 14-21721. Instance Table

Instance Name	Physical Address
USB0	0F40 007Ch

Figure 14-7179. USB3P0SS_CTRL_DEV_BUF_CTRL Name Register

31	30	29	28	27	26	25	24
BUF_CMD_STS	RESERVED0						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED0		BUF_CMD_IWD	BUF_CMD_IWU	BUF_CMD_WR4	BUF_CMD_RD	BUF_CMD_WR	BUF_CMD_SET
R		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-21723. USB3P0SS_CTRL_DEV_BUF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BUF_CMD_STS	R	0h	Status of BUF_CMD operations. This bit is set high when controller performs BUF CMD IWD and IWU operations. When it is set, no other SFR or DMA operation can be issued to the controller. Reset Source: rst_mod_g_rst_n
30:6	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
5	BUF_CMD_IWD	R/W	0h	Incremental write counting down to device on-chip mem. Used for incremental writing data into device on-chip memory starting from address pointed by BUF_ADDR register [two lsb rounded down to 0]. To write data to memory, the following order must be maintained: 1] BUF_ADDR register must be set with start address, 2] The BUF_DATA must be set with data expected to be written to on-chip mem 3] BUF_CMD_IWD with BUF_CMD_SET must be set to perform write operation. This write operation is effective only when this BUF_CMD_IWD bit is set together with the BUF_CMD_SET bit. As long as controller performs this command, the BUF_CMD_STS status bit is set, and no other SFR or DMA operation can be issued to the controller. This command can be useful during memory initialization Reset Source: rst_mod_g_rst_n

Table 14-21723. USB3P0SS_CTRL_DEV_BUF_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	BUF_CMD_IWU	R/W	0h	Incremental write counting up to device on-chip mem. Used for incremental writing data into device on-chip memory starting from address pointed by BUF_ADDR register [two lsb rounded down to 0]. To write data to memory, the following order must be maintained: 1] BUF_ADDR register must be set with start address, 2] The BUF_DATA must be set with data expected to be written to on-chip mem 3] BUF_CMD_IWD with BUF_CMD_SET must be set to perform write operation. This write operation is effective only when this BUF_CMD_IWU bit is set together with the BUF_CMD_SET bit. As long as controller performs this command, the BUF_CMD_STS status bit is set, and no other SFR or DMA operation can be issued to the controller. This command can be useful during memory initialization Reset Source: rst_mod_g_rst_n
3	BUF_CMD_WR4	R/W	0h	Write 4 words [16B] to device on-chip mem. Used for writing 4 words [4x duplicated BUF_DATA data] into device on-chip memory at address pointed by BUF_ADDR register [two lsb rounded down to 0]. To write data to memory, the following order must be maintained: 1] BUF_ADDR register must be set with address to be accessed, 2] The BUF_DATA must be set with data expected to be written to on-chip mem 3] BUF_CMD_WR4 with BUF_CMD_SET must be set to perform write operation. During this operation the BUF_DATA [duplicated 4 times] register is written to memory. This write operation is effective only when this BUF_CMD_WR4 bit is set together with the BUF_CMD_SET bit. This command can be useful during memory initialization Reset Source: rst_mod_g_rst_n
2	BUF_CMD_RD	R/W	0h	Read data [32B] from device on-chip mem. Used for reading data [1 word] from device on-chip memory from address pointed by BUF_ADDR register. To read data from memory,the following order must be maintained: 1] BUF_ADDR register must be set with address to be accessed, 2] BUF_CMD_RD with BUF_CMD_SET must be set to perform read operation. During this operation the BUF_DATA register is loaded with data readed from memory 3] The BUF_DATA can be read. This read operation is effective only when this BUF_CMD_RD bit is set together with the BUF_CMD_SET bit. Reset Source: rst_mod_g_rst_n
1	BUF_CMD_WR	R/W	0h	Write 1 word [4B] to device on-chip mem. Used for writing 1 word [as prepared in BUF_DATA register] into device on-chip memory at address pointed by BUF_ADDR register. To write data to memory,the following order must be maintained: 1] BUF_ADDR register must be set with address to be accessed, 2] The BUF_DATA must be set with data expected to be written to on-chip mem 3] BUF_CMD_WR with BUF_CMD_SET must be set to perform write operation. During this operation the BUF_DATA register is written to memory. This write operation is effective only when this BUF_CMD_WR bit is set together with the BUF_CMD_SET bit. Reset Source: rst_mod_g_rst_n
0	BUF_CMD_SET	R/W	0h	Buffer Command Set. This bit must be written 1 in conjuction with one of WR, RD, WR4 IWD or IWU commands to make command effective. Only one command can be set at a moment. Commands WR, WR4 and RD are executed immediatelly, but after issuing commands IWD and IWU, the BUF_CMD_STS bit must be check before going forward to other SW operations Reset Source: rst_mod_g_rst_n

14.9.2.3.2.290 USB3P0SS_CTRL_DEV_DTRANS Register

1 USB3P0SS_CTRL_DEV_DTRANS Register (Offset = 80h) [reset = 0h]

DMA transfer configuration Register (1 - DMULT mode, 0 - DSINGLE mode). Bits 0..15 applies to EPOUT0..EPOUT15 and bits 16..31 applies to EPIN0..EPIN15

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Table 14-21724. Instance Table

Instance Name	Physical Address
USB0	0F40 0080h

Figure 14-7180. USB3P0SS_CTRL_DEV_DTRANS Name Register

31	30	29	28	27	26	25	24
DTRANS15I	DTRANS14I	DTRANS13I	DTRANS12I	DTRANS11I	DTRANS10I	DTRANS9I	DTRANS8I
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
DTRANS7I	DTRANS6I	DTRANS5I	DTRANS4I	DTRANS3I	DTRANS2I	DTRANS1I	DTRANS0I
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
DTRANS15O	DTRANS14O	DTRANS13O	DTRANS12O	DTRANS11O	DTRANS10O	DTRANS9O	DTRANS8O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
DTRANS7O	DTRANS6O	DTRANS5O	DTRANS4O	DTRANS3O	DTRANS2O	DTRANS1O	DTRANS0O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21726. USB3P0SS_CTRL_DEV_DTRANS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DTRANS15I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/ Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
30	DTRANS14I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/ Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n

Table 14-21726. USB3P0SS_CTRL_DEV_DTRANS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	DTRANS13I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
28	DTRANS12I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
27	DTRANS11I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
26	DTRANS10I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
25	DTRANS9I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
24	DTRANS8I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
23	DTRANS7I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n

Table 14-21726. USB3P0SS_CTRL_DEV_DTRANS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	DTRANS6I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
21	DTRANS5I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
20	DTRANS4I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
19	DTRANS3I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
18	DTRANS2I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
17	DTRANS1I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
16	DTRANS0I	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n

Table 14-21726. USB3P0SS_CTRL_DEV_DTRANS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DTRANS15O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
14	DTRANS14O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
13	DTRANS13O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
12	DTRANS12O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
11	DTRANS11O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
10	DTRANS10O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
9	DTRANS9O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n

Table 14-21726. USB3P0SS_CTRL_DEV_DTRANS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DTRANS8O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
7	DTRANS7O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
6	DTRANS6O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
5	DTRANS5O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
4	DTRANS4O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
3	DTRANS3O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
2	DTRANS2O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n

Table 14-21726. USB3P0SS_CTRL_DEV_DTRANS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DTRANS1O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/ Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n
0	DTRANS0O	R/W	0h	DMA transfer configuration status for selected Endpoint[0 - single request - Single TRB chain. Single request [DRDY/Doorbell] triggers DMA, which transfers single TRB chain only and ends the EP transfer. 1 - single request - Multiple TRB chain. Single request [DRDY/ Doorbell] triggers DMA which starts transfer until the owner of the new chain is not DMA [this causes a TRB error interrupt].] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.291 USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register

1 USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register (Offset = 84h) [reset = 0h]

Source of TDL configuration Register (1 - TDL read by DMA from TD_SIZE field in TRB , 0 - TDL programmed through EP_TDL register). Bits 0..15 applies to EPOUT0..EPOUT15 and bits 16..31 applies to EPIN0..EPIN15

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Table 14-21727. Instance Table

Instance Name	Physical Address
USB0	**0F40 0084h**

Figure 14-7181. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Name Register

31	30	29	28	27	26	25	24
TDL_FROM_TRB15I	TDL_FROM_TRB14I	TDL_FROM_TRB13I	TDL_FROM_TRB12I	TDL_FROM_TRB11I	TDL_FROM_TRB10I	TDL_FROM_TRB9I	TDL_FROM_TRB8I
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TDL_FROM_TRB7I	TDL_FROM_TRB6I	TDL_FROM_TRB5I	TDL_FROM_TRB4I	TDL_FROM_TRB3I	TDL_FROM_TRB2I	TDL_FROM_TRB1I	TDL_FROM_TRB0I
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TDL_FROM_TRB15O	TDL_FROM_TRB14O	TDL_FROM_TRB13O	TDL_FROM_TRB12O	TDL_FROM_TRB11O	TDL_FROM_TRB10O	TDL_FROM_TRB9O	TDL_FROM_TRB8O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TDL_FROM_TRB7O	TDL_FROM_TRB6O	TDL_FROM_TRB5O	TDL_FROM_TRB4O	TDL_FROM_TRB3O	TDL_FROM_TRB2O	TDL_FROM_TRB1O	TDL_FROM_TRB0O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDL_FROM_TRB15I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	TDL_FROM_TRB14I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
29	TDL_FROM_TRB13I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
28	TDL_FROM_TRB12I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
27	TDL_FROM_TRB11I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	TDL_FROM_TRB10I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
25	TDL_FROM_TRB9I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
24	TDL_FROM_TRB8I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
23	TDL_FROM_TRB7I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	TDL_FROM_TRB6I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
21	TDL_FROM_TRB5I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
20	TDL_FROM_TRB4I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
19	TDL_FROM_TRB3I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	TDL_FROM_TRB2I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
17	TDL_FROM_TRB1I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
16	TDL_FROM_TRB0I	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
15	TDL_FROM_TRB15O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	TDL_FROM_TRB14O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
13	TDL_FROM_TRB13O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
12	TDL_FROM_TRB12O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
11	TDL_FROM_TRB11O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TDL_FROM_TRB10O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
9	TDL_FROM_TRB9O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
8	TDL_FROM_TRB8O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
7	TDL_FROM_TRB7O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TDL_FROM_TRB6O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
5	TDL_FROM_TRB5O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
4	TDL_FROM_TRB4O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
3	TDL_FROM_TRB3O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

Table 14-21729. USB3P0SS_CTRL_DEV_TDL_FROM_TRB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TDL_FROM_TRB2O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
1	TDL_FROM_TRB1O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n
0	TDL_FROM_TRB0O	R/W	0h	This field informs if support for automatic internal TDL calculation basing on the size provided in TRB for DMULT mode is enabled for selected Endpoint. To enable/disable this feature use the ENABLE_TDL_TRB/DISABLE_TDL_TRB bits in the USB_CONF2 register. When this option is enabled the TDL programming with EP_CMD.TDL+STDL is disabled, however read operation through this register can be performed. - 0 - controller doesn't support automatic internal TDL calculation - 1 - controller supports automatic internal TDL calculation This feature can be enabled only when controller supports it, i.e. when the USB_CAP1.TDL_FROM_TRB=1 and when DMULT mode for particular EP is set Reset Source: rst_mod_g_rst_n

14.9.2.3.2.292 USB3P0SS_CTRL_DEV_TDL_BEH Register

1 USB3P0SS_CTRL_DEV_TDL_BEH Register (Offset = 88h) [reset = 0h]

TDL behavior configuration Register. Value 0 means that USB short packet decrements TDL, value 1 means that USB short packet clears-blocks TDL (defined by TDL_BEH2 register). When specific Endpoint works in TDL_FROM_TRB mode (TDL_FROM_TRB.n == 1) this register must be set to 1. When specific Endpoint is configured to Bulk stream transfers (EP_CFG.STREAM_EN == 1) this register must be set to 0. Bits 0..15 applies to EPOUT0..EPOUT15

Return to Summary Table

Table 14-21730. Instance Table

Instance Name	Physical Address
USB0	**0F40 0088h**

Figure 14-7182. USB3P0SS_CTRL_DEV_TDL_BEH Name Register

31	30	29	28	27	26	25	24
RESERVED31	RESERVED30	RESERVED29	RESERVED28	RESERVED27	RESERVED26	RESERVED25	RESERVED24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED23	RESERVED22	RESERVED21	RESERVED20	RESERVED19	RESERVED18	RESERVED17	RESERVED16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TDL_BEH15O	TDL_BEH14O	TDL_BEH13O	TDL_BEH12O	TDL_BEH11O	TDL_BEH10O	TDL_BEH9O	TDL_BEH8O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TDL_BEH7O	TDL_BEH6O	TDL_BEH5O	TDL_BEH4O	TDL_BEH3O	TDL_BEH2O	TDL_BEH1O	TDL_BEH0O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21732. USB3P0SS_CTRL_DEV_TDL_BEH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED31	R	0h	Reserved field. Write ignored. 0 when read.
30	RESERVED30	R	0h	Reserved field. Write ignored. 0 when read.
29	RESERVED29	R	0h	Reserved field. Write ignored. 0 when read.
28	RESERVED28	R	0h	Reserved field. Write ignored. 0 when read.
27	RESERVED27	R	0h	Reserved field. Write ignored. 0 when read.
26	RESERVED26	R	0h	Reserved field. Write ignored. 0 when read.
25	RESERVED25	R	0h	Reserved field. Write ignored. 0 when read.
24	RESERVED24	R	0h	Reserved field. Write ignored. 0 when read.
23	RESERVED23	R	0h	Reserved field. Write ignored. 0 when read.
22	RESERVED22	R	0h	Reserved field. Write ignored. 0 when read.
21	RESERVED21	R	0h	Reserved field. Write ignored. 0 when read.
20	RESERVED20	R	0h	Reserved field. Write ignored. 0 when read.
19	RESERVED19	R	0h	Reserved field. Write ignored. 0 when read.
18	RESERVED18	R	0h	Reserved field. Write ignored. 0 when read.
17	RESERVED17	R	0h	Reserved field. Write ignored. 0 when read.

Table 14-21732. USB3P0SS_CTRL_DEV_TDL_BEH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	RESERVED16	R	0h	Reserved field. Write ignored. 0 when read.
15	TDL_BEH15O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
14	TDL_BEH14O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
13	TDL_BEH13O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
12	TDL_BEH12O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
11	TDL_BEH11O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
10	TDL_BEH10O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
9	TDL_BEH9O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
8	TDL_BEH8O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
7	TDL_BEH7O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
6	TDL_BEH6O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
5	TDL_BEH5O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
4	TDL_BEH4O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
3	TDL_BEH3O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
2	TDL_BEH2O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
1	TDL_BEH1O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
0	TDL_BEH0O	R/W	0h	TDL behavior configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.293 USB3P0SS_CTRL_DEV_EP_TDL Register

1 USB3P0SS_CTRL_DEV_EP_TDL Register (Offset = 8Ch) [reset = 0h]

Endpoint TDL Register

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Table 14-21733. Instance Table

Instance Name	**Physical Address**
USB0	**0F40 008Ch**

Figure 14-7183. USB3P0SS_CTRL_DEV_EP_TDL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED0</td><td colspan="3">TDL</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TDL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-21735. USB3P0SS_CTRL_DEV_EP_TDL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
10:0	TDL	R/W	0h	This field can be used to update/read internal TDL counter when TDL_FROM_TRB mode is not enabled for specific Endpoint.Writing into this field any non-zero value, will result in adding to existing TDL value the new written value. A as the maximum accumulative value of TDL counter is 2047, so when new value is written, and a sum of existing value and new value exceeds 2047, then register is wrap around, e.g. adding value 10 to the existing 2040 will result a value 2 in the TDL register. Writing zero, reset TDL counter to zero. For more information see USBSS-DEV_design_specification document. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.294 USB3P0SS_CTRL_DEV_TDL_BEH2 Register

1 USB3P0SS_CTRL_DEV_TDL_BEH2 Register (Offset = 90h) [reset = 0h]

TDL behavior 2 configuration Register. Value 0 means that USB short packet temporary gates TDL for protocol, allowing SW to read curent value of TDL. After SW reads TDL (on IOT irq) it should clear TDL to remove gating TDL value for protocol, value 1 means that USB short packet immediatelly clears TDL. When specific Endpoint works in TDL_FROM_TRB mode (TDL_FROM_TRB.n == 1) this register must be set to 1. When specific Endpoint is configured to Bulk stream transfers (EP_CFG.STREAM_EN == 1) this register must be set to 0. Bits 0..15 applies to EPOUT0..EPOUT15

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Table 14-21736. Instance Table

Instance Name	Physical Address
USB0	**0F40 0090h**

Figure 14-7184. USB3P0SS_CTRL_DEV_TDL_BEH2 Name Register

31	30	29	28	27	26	25	24
RESERVED31	RESERVED30	RESERVED29	RESERVED28	RESERVED27	RESERVED26	RESERVED25	RESERVED24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED23	RESERVED22	RESERVED21	RESERVED20	RESERVED19	RESERVED18	RESERVED17	RESERVED16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TDL_BEH215O	TDL_BEH214O	TDL_BEH213O	TDL_BEH212O	TDL_BEH211O	TDL_BEH210O	TDL_BEH29O	TDL_BEH28O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TDL_BEH27O	TDL_BEH26O	TDL_BEH25O	TDL_BEH24O	TDL_BEH23O	TDL_BEH22O	TDL_BEH21O	TDL_BEH20O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21738. USB3P0SS_CTRL_DEV_TDL_BEH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED31	R	0h	Reserved field. Write ignored. 0 when read.
30	RESERVED30	R	0h	Reserved field. Write ignored. 0 when read.
29	RESERVED29	R	0h	Reserved field. Write ignored. 0 when read.
28	RESERVED28	R	0h	Reserved field. Write ignored. 0 when read.
27	RESERVED27	R	0h	Reserved field. Write ignored. 0 when read.
26	RESERVED26	R	0h	Reserved field. Write ignored. 0 when read.
25	RESERVED25	R	0h	Reserved field. Write ignored. 0 when read.
24	RESERVED24	R	0h	Reserved field. Write ignored. 0 when read.
23	RESERVED23	R	0h	Reserved field. Write ignored. 0 when read.
22	RESERVED22	R	0h	Reserved field. Write ignored. 0 when read.
21	RESERVED21	R	0h	Reserved field. Write ignored. 0 when read.
20	RESERVED20	R	0h	Reserved field. Write ignored. 0 when read.
19	RESERVED19	R	0h	Reserved field. Write ignored. 0 when read.
18	RESERVED18	R	0h	Reserved field. Write ignored. 0 when read.

Table 14-21738. USB3P0SS_CTRL_DEV_TDL_BEH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	RESERVED17	R	0h	Reserved field. Write ignored. 0 when read.
16	RESERVED16	R	0h	Reserved field. Write ignored. 0 when read.
15	TDL_BEH215O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
14	TDL_BEH214O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
13	TDL_BEH213O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
12	TDL_BEH212O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
11	TDL_BEH211O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
10	TDL_BEH210O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
9	TDL_BEH29O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
8	TDL_BEH28O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
7	TDL_BEH27O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
6	TDL_BEH26O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
5	TDL_BEH25O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
4	TDL_BEH24O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
3	TDL_BEH23O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
2	TDL_BEH22O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n
1	TDL_BEH21O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n

Table 14-21738. USB3P0SS_CTRL_DEV_TDL_BEH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TDL_BEH20O	R/W	0h	TDL behavior 2 configuration Bit. This register configures TDL behavior for selected Endpoint. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.295 USB3P0SS_CTRL_DEV_DMA_ADV_TD Register

1 USB3P0SS_CTRL_DEV_DMA_ADV_TD Register (Offset = 94h) [reset = 0h]

DMA Advance TD configuration Register (0 - when stopped during transfer, DMA will advance its address only to the next TRB (+12) start address. 1 - when stopped during transfer (e.g. on USB short packet received in TDL_FROM_TRB mode) DMA will advance its address to the next TD start address). Bits 0..15 applies to EPOUT0..EPOUT15 and bits 16..31 applies to EPIN0..EPIN15

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Table 14-21739. Instance Table

Instance Name	Physical Address
USB0	0F40 0094h

Figure 14-7185. USB3P0SS_CTRL_DEV_DMA_ADV_TD Name Register

31	30	29	28	27	26	25	24
DMA_ADV_TD 15I	DMA_ADV_TD 14I	DMA_ADV_TD 13I	DMA_ADV_TD 12I	DMA_ADV_TD 11I	DMA_ADV_TD 10I	DMA_ADV_TD 9I	DMA_ADV_TD 8I
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
DMA_ADV_TD 7I	DMA_ADV_TD 6I	DMA_ADV_TD 5I	DMA_ADV_TD 4I	DMA_ADV_TD 3I	DMA_ADV_TD 2I	DMA_ADV_TD 1I	DMA_ADV_TD 0I
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
DMA_ADV_TD 15O	DMA_ADV_TD 14O	DMA_ADV_TD 13O	DMA_ADV_TD 12O	DMA_ADV_TD 11O	DMA_ADV_TD 10O	DMA_ADV_TD 9O	DMA_ADV_TD 8O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
DMA_ADV_TD 7O	DMA_ADV_TD 6O	DMA_ADV_TD 5O	DMA_ADV_TD 4O	DMA_ADV_TD 3O	DMA_ADV_TD 2O	DMA_ADV_TD 1O	DMA_ADV_TD 0O
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-21741. USB3P0SS_CTRL_DEV_DMA_ADV_TD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DMA_ADV_TD15I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
30	DMA_ADV_TD14I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
29	DMA_ADV_TD13I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
28	DMA_ADV_TD12I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
27	DMA_ADV_TD11I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
26	DMA_ADV_TD10I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n

Table 14-21741. USB3P0SS_CTRL_DEV_DMA_ADV_TD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DMA_ADV_TD9I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
24	DMA_ADV_TD8I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
23	DMA_ADV_TD7I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
22	DMA_ADV_TD6I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
21	DMA_ADV_TD5I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
20	DMA_ADV_TD4I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
19	DMA_ADV_TD3I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
18	DMA_ADV_TD2I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
17	DMA_ADV_TD1I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
16	DMA_ADV_TD0I	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
15	DMA_ADV_TD15O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
14	DMA_ADV_TD14O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
13	DMA_ADV_TD13O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
12	DMA_ADV_TD12O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
11	DMA_ADV_TD11O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
10	DMA_ADV_TD10O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
9	DMA_ADV_TD9O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
8	DMA_ADV_TD8O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
7	DMA_ADV_TD7O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
6	DMA_ADV_TD6O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
5	DMA_ADV_TD5O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
4	DMA_ADV_TD4O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n

Table 14-21741. USB3P0SS_CTRL_DEV_DMA_ADV_TD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DMA_ADV_TD3O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
2	DMA_ADV_TD2O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
1	DMA_ADV_TD1O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n
0	DMA_ADV_TD0O	R/W	0h	DMA Advance TD configuration Register for selected Endpoint. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.296 USB3P0SS_CTRL_DEV_CFG_REG1 Register

1 USB3P0SS_CTRL_DEV_CFG_REG1 Register (Offset = 100h) [reset = 38000h]

VBUS debouncer Configuration Register 1

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Table 14-21742. Instance Table

Instance Name	Physical Address
USB0	**0F40 0100h**

Figure 14-7186. USB3P0SS_CTRL_DEV_CFG_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">DEBOUNCER_CNT</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">38000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DEBOUNCER_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">38000h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEBOUNCER_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">38000h</td></tr>
</table>

Table 14-21744. USB3P0SS_CTRL_DEV_CFG_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
17:0	DEBOUNCER_CNT	R/W	38000h	This parameter defines the VBUS debouncer delay i.e. the time interval between the VBUS detection on device input and the start of using it internally. Resolution of this parameter is 128 ns. For simulation purposes it is recommended to set the value 1 [128ns] For synthesis purposes it is recommended to set the value 230000 [~30ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.297 USB3P0SS_CTRL_DEV_DBG_LINK1 Register

1 USB3P0SS_CTRL_DEV_DBG_LINK1 Register (Offset = 104h) [reset = 300A24h]

USB3.0 Configuration Register 2

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Table 14-21745. Instance Table

Instance Name	Physical Address
USB0	**0F40 0104h**

Figure 14-7187. USB3P0SS_CTRL_DEV_DBG_LINK1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED1</td><td>LFPS_GEN_PING_SET</td><td>RXDET_BREAK_DIS_SET</td><td>LFPS_MIN_GEN_U1_EXIT_SET</td><td>LFPS_MIN_DET_U1_EXIT_SET</td></tr>
<tr><td colspan="4">R</td><td>W</td><td>W</td><td>W</td><td>W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED0</td><td colspan="5">LFPS_GEN_PING</td><td>RXDET_BREAK_DIS</td></tr>
<tr><td colspan="2">R</td><td colspan="5">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="5">18h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LFPS_MIN_GEN_U1_EXIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">Ah</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LFPS_MIN_DET_U1_EXIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">24h</td></tr>
</table>

Table 14-21747. USB3P0SS_CTRL_DEV_DBG_LINK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
27	LFPS_GEN_PING_SET	W	0h	Set the LFPS_GEN_PING_SET value Writing '1' to this bit writes the LFPS_GEN_PING field value to the device. This bit is automatically cleared. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
26	RXDET_BREAK_DIS_SET	W	0h	Set the RXDET_BREAK_DIS value Writing '1' to this bit writes the RXDET_BREAK_DIS field value to the device. This bit is automatically cleared. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
25	LFPS_MIN_GEN_U1_EXIT_SET	W	0h	Set the LFPS_MIN_GEN_U1_EXIT value Writing '1' to this bit writes the LFPS_MIN_GEN_U1_EXIT field value to the device. This bit is automatically cleared. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n

Table 14-21747. USB3P0SS_CTRL_DEV_DBG_LINK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	LFPS_MIN_DET_U1_EXIT_SET	W	0h	Set the LFPS_MIN_DET_U1_EXIT value Writing '1' to this bit writes the LFPS_MIN_DET_U1_EXIT field value to the device. This bit is automatically cleared. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
23:22	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
21:17	LFPS_GEN_PING	R/W	18h	LFPS_GEN_PING value This parameter configures the LFPS.Ping generation time as shown in the chapter 4. This field is saved to the device only when the field LFPS_GEN_PING_SET is set to '1' during write to the DBG_LINK1 register. Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 24 [~200ns] For synthesis purposes it is recommended to set the value 24 [~200ns] Reset Source: rst_mod_g_rst_n
16	RXDET_BREAK_DIS	R/W	0h	RXDET_BREAK_DIS value This parameter configures terminating the Far-end Receiver termination detection sequence: '0': it is possible that USBSS_DEV will terminate Far-end receiver termination detection sequence '1': USBSS_DEV will not terminate Far-end receiver termination detection sequence The impact of the bit to the link behaviour is shown in chapter 4. This field is saved to the device only when the field RXDET_BREAK_DIS_SET is set to '1' during write to the DBG_LINK1 register. Reset Source: rst_mod_g_rst_n
15:8	LFPS_MIN_GEN_U1_EXIT	R/W	Ah	LFPS_MIN_GEN_U1_EXIT value This parameter configures the minimum time for phytxelecidle deassertion when LFPS.U1_Exit signalling is generated as shown in the chapter 4. This field is saved to the device only when the field LFPS_MIN_GEN_U1_EXIT_SET is set to '1' during write to the DBG_LINK1 register. Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 87 [~696ns] For synthesis purposes it is recommended to set the value 87 [~696ns] Reset Source: rst_mod_g_rst_n
7:0	LFPS_MIN_DET_U1_EXIT	R/W	24h	LFPS_MIN_DET_U1_EXIT value This parameter configures the minimum time required for decoding the received LFPS as an LFPS.U1_Exit. Example is shown in the chapter 4. This field is saved to the device only when the field LFPS_MIN_DET_U1_EXIT_SET is set to '1' during write to the DBG_LINK1 register. Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 36 [~300ns]. For synthesis purposes it is recommended to set the value 36 [~300ns]. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.298 USB3P0SS_CTRL_DEV_DBG_LINK2 Register

1 USB3P0SS_CTRL_DEV_DBG_LINK2 Register (Offset = 108h) [reset = 70AFF00h]

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Table 14-21748. Instance Table

Instance Name	Physical Address
USB0	**0F40 0108h**

Figure 14-7188. USB3P0SS_CTRL_DEV_DBG_LINK2 Name Register

31	30	29	28	27	26	25	24
TXDET_DVAL_SET	PHYRXVAL_DVAL_SET	RXEQTR_DVAL_SET	RXEQTR_AVAL_SET	RESERVED	TXDET_DVAL		
W	W	W	W	R	R/W		
0h	0h	0h	0h	0h	7h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHYRXVAL_DVAL							
R/W							
Ah							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RXEQTR_DVAL							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RXEQTR_AVAL							
R/W							
0h							

Table 14-21750. USB3P0SS_CTRL_DEV_DBG_LINK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TXDET_DVAL_SET	W	0h	Set the TXDET deassertion value Writing '1' to this bit writes the TXDET_DVAL field value to the device. This bit is automatically cleared. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
30	PHYRXVAL_DVAL_SET	W	0h	Set the Phyrxvalid latency deassertion value Writing '1' to this bit writes the PHYRXVAL_DVAL field value to the device. This bit is automatically cleared. Writing '0' has no effect.0 Reset Source: rst_mod_g_rst_n
29	RXEQTR_DVAL_SET	W	0h	Set the rxeqtraining deassertion value Writing '1' to this bit writes the RXEQTR_DVAL field value to the device. This bit is automatically cleared. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
28	RXEQTR_AVAL_SET	W	0h	Set the rxeqtraining assertion value Writing '1' to this bit writes the RXEQTR_AVAL field value to the device. This bit is automatically cleared. Writing '0' has no effect. Reset Source: rst_mod_g_rst_n
27	RESERVED	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21750. USB3P0SS_CTRL_DEV_DBG_LINK2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:24	TXDET_DVAL	R/W	7h	TXDET deassertion value This parameter configures the phytxdetrx_loop deassertion time after phystatus deassertion during Far-end receiver termination sequence as shown in the chapter 4. This field is saved to the device only when the field TXDET_DVAL_SET is set to '1' during write to the DBG_LINK2 register. Reset Source: rst_mod_g_rst_n
23:16	PHYRXVAL_DVAL	R/W	Ah	Phyrxvalid latency deassertion value This parameter enables extending internal phyrxdata and phyrxdatak validity as shown in the chapter 4. This field is saved to the device only when the field PHYRXVAL_DVAL_SET is set to '1' during write to the DBG_LINK2 register. Reset Source: rst_mod_g_rst_n
15:8	RXEQTR_DVAL	R/W	FFh	Rxeqtraining deassertion value This parameter configures phyrxeqtraining deasserting time as shown in the chapter 4. This field is saved to the device only when the field RXEQTR_DVAL_SET is set to '1' during write to the DBG_LINK2 register. Reset Source: rst_mod_g_rst_n
7:0	RXEQTR_AVAL	R/W	0h	Rxeqtraining assertion value This parameter configures phyrxeqtraining asserting time as shown in the chapter 4. This field is saved to the device only when the field RXEQTR_AVAL_SET is set to '1' during write to the DBG_LINK2 register. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.299 USB3P0SS_CTRL_DEV_CFG_REG4 Register

1 USB3P0SS_CTRL_DEV_CFG_REG4 Register (Offset = 10Ch) [reset = 80000079h]

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Table 14-21751. Instance Table

Instance Name	Physical Address
USB0	**0F40 010Ch**

Figure 14-7189. USB3P0SS_CTRL_DEV_CFG_REG4 Name Register

31	30	29	28	27	26	25	24
RXDETECT_QUIET_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RXDETECT_QUIET_TIMEOUT							
R/W							
79h							

Table 14-21753. USB3P0SS_CTRL_DEV_CFG_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RXDETECT_QUIET_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for RXDETECT_QUIET_TIMEOUT : - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	RXDETECT_QUIET_TIMEOUT	R/W	79h	RXDETECT_QUIET_TIMEOUT value Resolution of this parameter is selected by RXDETECT_QUIET_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 13*1us =~12us [VIP based ENV] For synthesis purposes it is recommended to set the value 121*100us =~12ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.300 USB3P0SS_CTRL_DEV_CFG_REG5 Register

1 USB3P0SS_CTRL_DEV_CFG_REG5 Register (Offset = 110h) [reset = 800003E9h]

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Table 14-21754. Instance Table

Instance Name	**Physical Address**
USB0	**0F40 0110h**

Figure 14-7190. USB3P0SS_CTRL_DEV_CFG_REG5 Name Register

31	30	29	28	27	26	25	24
U3_HDSK_FAIL_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED					U3_HDSK_FAIL_TIMEOUT		
R					R/W		
0h					3E9h		
7	6	5	4	3	2	1	0
U3_HDSK_FAIL_TIMEOUT							
R/W							
3E9h							

Table 14-21756. USB3P0SS_CTRL_DEV_CFG_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	U3_HDSK_FAIL_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for U3_HDSK_FAIL_TIMEOUT : - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:11	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
10:0	U3_HDSK_FAIL_TIMEOUT	R/W	3E9h	U3_HDSK_FAIL_TIMEOUT value Resolution of this parameter is selected by U3_HDSK_FAIL_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 11*100us =~1ms [VIP based ENV] For synthesis purposes it is recommended to set the value 1001*100us =~100ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.301 USB3P0SS_CTRL_DEV_CFG_REG6 Register

1 USB3P0SS_CTRL_DEV_CFG_REG6 Register (Offset = 114h) [reset = 80000079h]

Configuration Register 6

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Table 14-21757. Instance Table

Instance Name	Physical Address
USB0	**0F40 0114h**

Figure 14-7191. USB3P0SS_CTRL_DEV_CFG_REG6 Name Register

31	30	29	28	27	26	25	24
SSINACTIVE_QUIET_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SSINACTIVE_QUIET_TIMEOUT							
R/W							
79h							

Table 14-21759. USB3P0SS_CTRL_DEV_CFG_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SSINACTIVE_QUIET_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for SSINACTIVE_QUIET_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	SSINACTIVE_QUIET_TIMEOUT	R/W	79h	SSINACTIVE_QUIET_TIMEOUT value Resolution of this parameter is selected by SSINACTIVE_QUIET_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 13*1us =~12us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 121*100us =~12ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.302 USB3P0SS_CTRL_DEV_CFG_REG7 Register

1 USB3P0SS_CTRL_DEV_CFG_REG7 Register (Offset = 118h) [reset = 80000E11h]

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Table 14-21760. Instance Table

Instance Name	Physical Address
USB0	**0F40 0118h**

Figure 14-7192. USB3P0SS_CTRL_DEV_CFG_REG7 Name Register

31	30	29	28	27	26	25	24
POLLING_LFPS_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED			POLLING_LFPS_TIMEOUT				
R			R/W				
0h			E11h				
7	6	5	4	3	2	1	0
POLLING_LFPS_TIMEOUT							
R/W							
E11h							

Table 14-21762. USB3P0SS_CTRL_DEV_CFG_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	POLLING_LFPS_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for POLLING_LFPS_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:13	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
12:0	POLLING_LFPS_TIMEOUT	R/W	E11h	POLLING_LFPS_TIMEOUT value Resolution of this parameter is selected by POLLING_LFPS_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 481*1us =~480us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 3601*100us =~360ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.303 USB3P0SS_CTRL_DEV_CFG_REG8 Register

1 USB3P0SS_CTRL_DEV_CFG_REG8 Register (Offset = 11Ch) [reset = 80000079h]

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Table 14-21763. Instance Table

Instance Name	Physical Address
USB0	**0F40 011Ch**

Figure 14-7193. USB3P0SS_CTRL_DEV_CFG_REG8 Name Register

31	30	29	28	27	26	25	24
POLLING_ACTIVE_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						POLLING_ACTIVE_TIMEOUT	
R						R/W	
0h						79h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POLLING_ACTIVE_TIMEOUT							
R/W							
79h							

Table 14-21765. USB3P0SS_CTRL_DEV_CFG_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	POLLING_ACTIVE_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for POLLING_ACTIVE_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:10	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
9:0	POLLING_ACTIVE_TIMEOUT	R/W	79h	POLLING_ACTIVE_TIMEOUT value Resolution of this parameter is selected by POLLING_ACTIVE_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 31*1us =~30us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 121*100us =~12ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.304 USB3P0SS_CTRL_DEV_CFG_REG9 Register

1 USB3P0SS_CTRL_DEV_CFG_REG9 Register (Offset = 120h) [reset = 80000015h]

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Table 14-21766. Instance Table

Instance Name	Physical Address
USB0	**0F40 0120h**

Figure 14-7194. USB3P0SS_CTRL_DEV_CFG_REG9 Name Register

31	30	29	28	27	26	25	24
POLLING_IDLE_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			POLLING_IDLE_TIMEOUT				
R			R/W				
0h			15h				

Table 14-21768. USB3P0SS_CTRL_DEV_CFG_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	POLLING_IDLE_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for POLLING_IDLE_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:5	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
4:0	POLLING_IDLE_TIMEOUT	R/W	15h	POLLING_IDLE_TIMEOUT value Resolution of this parameter is selected by POLLING_IDLE_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 21*100us =~2ms [SystemC device ENV] - 3*1us =~2us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 21*100us =~2ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.305 USB3P0SS_CTRL_DEV_CFG_REG10 Register

1 USB3P0SS_CTRL_DEV_CFG_REG10 Register (Offset = 124h) [reset = 80000079h]

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Table 14-21769. Instance Table

Instance Name	Physical Address
USB0	**0F40 0124h**

Figure 14-7195. USB3P0SS_CTRL_DEV_CFG_REG10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">POLLING_CONF_TIMEOUT_PRESCALE</td><td colspan="6">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R</td></tr>
<tr><td colspan="2">2h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">POLLING_CONF_TIMEOUT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">79h</td></tr>
</table>

Table 14-21771. USB3P0SS_CTRL_DEV_CFG_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	POLLING_CONF_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for POLLING_CONF_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	POLLING_CONF_TIMEOUT	R/W	79h	POLLING_CONF_TIMEOUT value Resolution of this parameter is selected by POLLING_CONF_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 31*1us =~30us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 121*100us =~12ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.306 USB3P0SS_CTRL_DEV_CFG_REG11 Register

1 USB3P0SS_CTRL_DEV_CFG_REG11 Register (Offset = 128h) [reset = 80000079h]

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Table 14-21772. Instance Table

Instance Name	Physical Address
USB0	**0F40 0128h**

Figure 14-7196. USB3P0SS_CTRL_DEV_CFG_REG11 Name Register

31	30	29	28	27	26	25	24
RECOVERY_ACTIVE_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RECOVERY_ACTIVE_TIMEOUT							
R/W							
79h							

Table 14-21774. USB3P0SS_CTRL_DEV_CFG_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RECOVERY_ACTIVE_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for RECOVERY_ACTIVE_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	RECOVERY_ACTIVE_TIMEOUT	R/W	79h	RECOVERY_ACTIVE_TIMEOUT value Resolution of this parameter is selected by RECOVERY_ACTIVE_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 101*1us =~100us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 121*100us =~12ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.307 USB3P0SS_CTRL_DEV_CFG_REG12 Register

1 USB3P0SS_CTRL_DEV_CFG_REG12 Register (Offset = 12Ch) [reset = 8000003Dh]

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Table 14-21775. Instance Table

Instance Name	Physical Address
USB0	**0F40 012Ch**

Figure 14-7197. USB3P0SS_CTRL_DEV_CFG_REG12 Name Register

31	30	29	28	27	26	25	24
RECOVERY_CONF_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RECOVERY_CONF_TIMEOUT							
R/W							
3Dh							

Table 14-21777. USB3P0SS_CTRL_DEV_CFG_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RECOVERY_CONF_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for RECOVERY_CONF_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	RECOVERY_CONF_TIMEOUT	R/W	3Dh	RECOVERY_CONF_TIMEOUT value Resolution of this parameter is selected by RECOVERY_CONF_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 101*1us =~100us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 61*100us =~6ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.308 USB3P0SS_CTRL_DEV_CFG_REG13 Register

1 USB3P0SS_CTRL_DEV_CFG_REG13 Register (Offset = 130h) [reset = 80000015h]

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Table 14-21778. Instance Table

Instance Name	Physical Address
USB0	**0F40 0130h**

Figure 14-7198. USB3P0SS_CTRL_DEV_CFG_REG13 Name Register

31	30	29	28	27	26	25	24
RECOVERY_IDLE_TIMEOUT_PRESCALE		RESERVED		RESERVED			
R/W		NONE		R			
2h		0h		0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			RECOVERY_IDLE_TIMEOUT				
R			R/W				
0h			15h				

Table 14-21780. USB3P0SS_CTRL_DEV_CFG_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RECOVERY_IDLE_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for RECOVERY_IDLE_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:28	RESERVED	NONE	0h	Reserved
27:5	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
4:0	RECOVERY_IDLE_TIMEOUT	R/W	15h	RECOVERY_IDLE_TIMEOUT value Resolution of this parameter is selected by RECOVERY_IDLE_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 21*100us =~2ms [SystemC device ENV] - 3*1us =~3us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 21*100us =~2ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.309 USB3P0SS_CTRL_DEV_CFG_REG14 Register

1 USB3P0SS_CTRL_DEV_CFG_REG14 Register (Offset = 134h) [reset = 80000079h]

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Table 14-21781. Instance Table

Instance Name	Physical Address
USB0	**0F40 0134h**

Figure 14-7199. USB3P0SS_CTRL_DEV_CFG_REG14 Name Register

31	30	29	28	27	26	25	24
HOTRESET_ACTIVE_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HOTRESET_ACTIVE_TIMEOUT							
R/W							
79h							

Table 14-21783. USB3P0SS_CTRL_DEV_CFG_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	HOTRESET_ACTIVE_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for HOTRESET_ACTIVE_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	HOTRESET_ACTIVE_TIMEOUT	R/W	79h	HOTRESET_ACTIVE_TIMEOUT value Resolution of this parameter is selected by HOTRESET_ACTIVE_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 21*100us =~2ms [SystemC device ENV] - 13*1us =~13us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 121*100us =~12ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.310 USB3P0SS_CTRL_DEV_CFG_REG15 Register

1 USB3P0SS_CTRL_DEV_CFG_REG15 Register (Offset = 138h) [reset = 80000015h]

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Table 14-21784. Instance Table

Instance Name	Physical Address
USB0	**0F40 0138h**

Figure 14-7200. USB3P0SS_CTRL_DEV_CFG_REG15 Name Register

31	30	29	28	27	26	25	24
HOTRESET_EXIT_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			HOTRESET_EXIT_TIMEOUT				
R			R/W				
0h			15h				

Table 14-21786. USB3P0SS_CTRL_DEV_CFG_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	HOTRESET_EXIT_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for HOTRESET_EXIT_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:5	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
4:0	HOTRESET_EXIT_TIMEOUT	R/W	15h	HOTRESET_EXIT_TIMEOUT value Resolution of this parameter is selected by HOTRESET_EXIT_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 21*100us =~2ms [SystemC device ENV] - 3*1us =~3us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 21*100us =~2ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.311 USB3P0SS_CTRL_DEV_CFG_REG16 Register

1 USB3P0SS_CTRL_DEV_CFG_REG16 Register (Offset = 13Ch) [reset = 800007D1h]

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Table 14-21787. Instance Table

Instance Name	Physical Address
USB0	**0F40 013Ch**

Figure 14-7201. USB3P0SS_CTRL_DEV_CFG_REG16 Name Register

31	30	29	28	27	26	25	24
LFPS_PING_REPEAT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LFPS_PING_REPEAT			
R				R/W			
0h				7D1h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LFPS_PING_REPEAT							
R/W							
7D1h							

Table 14-21789. USB3P0SS_CTRL_DEV_CFG_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	LFPS_PING_REPEAT_PRESCALE	R/W	2h	PRESCALER for LFPS_PING_REPEAT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:12	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
11:0	LFPS_PING_REPEAT	R/W	7D1h	LFPS_PING_REPEAT value Resolution of this parameter is selected by LFPS_PING_REPEAT_PRESCALE. For simulation purposes it is recommended to set the value: - 6*100us =~0.5ms [SystemC device ENV] - 4*100us =~400us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 2001*100us =~200ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.312 USB3P0SS_CTRL_DEV_CFG_REG17 Register

1 USB3P0SS_CTRL_DEV_CFG_REG17 Register (Offset = 140h) [reset = 1B5h]

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Table 14-21790. Instance Table

Instance Name	Physical Address
USB0	**0F40 0140h**

Figure 14-7202. USB3P0SS_CTRL_DEV_CFG_REG17 Name Register

31	30	29	28	27	26	25	24
PENDING_HP_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PENDING_HP_TIMEOUT	
R						R/W	
0h						1B5h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PENDING_HP_TIMEOUT							
R/W							
1B5h							

Table 14-21792. USB3P0SS_CTRL_DEV_CFG_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	PENDING_HP_TIMEOUT_PRESCALE	R/W	0h	PRESCALER for PENDING_HP_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:10	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
9:0	PENDING_HP_TIMEOUT	R/W	1B5h	PENDING_HP_TIMEOUT value Resolution of this parameter is selected by PENDING_HP_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 437*8ns =~3.5us [SystemC device ENV] - 437*8ns =~3.5us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 437*8ns =~3.5us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.313 USB3P0SS_CTRL_DEV_CFG_REG18 Register

1 USB3P0SS_CTRL_DEV_CFG_REG18 Register (Offset = 144h) [reset = 80000034h]

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Table 14-21793. Instance Table

Instance Name	Physical Address
USB0	**0F40 0144h**

Figure 14-7203. USB3P0SS_CTRL_DEV_CFG_REG18 Name Register

31	30	29	28	27	26	25	24
CREDIT_HP_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	CREDIT_HP_TIMEOUT						
R	R/W						
0h	34h						

Table 14-21795. USB3P0SS_CTRL_DEV_CFG_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CREDIT_HP_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for CREDIT_HP_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:7	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
6:0	CREDIT_HP_TIMEOUT	R/W	34h	CREDIT_HP_TIMEOUT value Resolution of this parameter is selected by CREDIT_HP_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 11*100us =~1ms [VIP based ENV] For synthesis purposes it is recommended to set the value: - 52*100us =~5.1ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.314 USB3P0SS_CTRL_DEV_CFG_REG19 Register

1 USB3P0SS_CTRL_DEV_CFG_REG19 Register (Offset = 148h) [reset = 4000000Bh]

USB3.0 Configuration Register 19

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Table 14-21796. Instance Table

Instance Name	Physical Address
USB0	**0F40 0148h**

Figure 14-7204. USB3P0SS_CTRL_DEV_CFG_REG19 Name Register

31	30	29	28	27	26	25	24
LUP_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
1h		0h					
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED						LUP_TIMEOUT	
R						R/W	
0h						Bh	
7	6	5	4	3	2	1	0
LUP_TIMEOUT							
R/W							
Bh							

Table 14-21798. USB3P0SS_CTRL_DEV_CFG_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	LUP_TIMEOUT_PRESCALE	R/W	1h	PRESCALER for LUP_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:10	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
9:0	LUP_TIMEOUT	R/W	Bh	LUP_TIMEOUT value Resolution of this parameter is selected by LUP_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*1us =~11us [SystemC device ENV] - 11*1us =~11us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 11*1us =~11us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.315 USB3P0SS_CTRL_DEV_CFG_REG20 Register

1 USB3P0SS_CTRL_DEV_CFG_REG20 Register (Offset = 14Ch) [reset = 8000000Bh]

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Table 14-21799. Instance Table

Instance Name	Physical Address
USB0	0F40 014Ch

Figure 14-7205. USB3P0SS_CTRL_DEV_CFG_REG20 Name Register

31	30	29	28	27	26	25	24
LDN_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
LDN_TIMEOUT							
R/W							
Bh							

Table 14-21801. USB3P0SS_CTRL_DEV_CFG_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	LDN_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for LDN_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	LDN_TIMEOUT	R/W	Bh	LDN_TIMEOUT value Resolution of this parameter is selected by LDN_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 11*100us =~1ms [SystemC device ENV] - 129*1us =~129us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 11*100us =~1ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.316 USB3P0SS_CTRL_DEV_CFG_REG21 Register

1 USB3P0SS_CTRL_DEV_CFG_REG21 Register (Offset = 150h) [reset = 190h]

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Table 14-21802. Instance Table

Instance Name	Physical Address
USB0	**0F40 0150h**

Figure 14-7206. USB3P0SS_CTRL_DEV_CFG_REG21 Name Register

31	30	29	28	27	26	25	24
PM_LC_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PM_LC_TIMEOUT	
R						R/W	
0h						190h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PM_LC_TIMEOUT							
R/W							
190h							

Table 14-21804. USB3P0SS_CTRL_DEV_CFG_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	PM_LC_TIMEOUT_PRESCALE	R/W	0h	PRESCALER for PM_LC_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:10	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
9:0	PM_LC_TIMEOUT	R/W	190h	PM_LC_TIMEOUT value Resolution of this parameter is selected by PM_LC_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 400*8ns =~3.2us [SystemC device ENV] - 400*8ns =~3.2us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 400*8ns =~3.2us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.317 USB3P0SS_CTRL_DEV_CFG_REG22 Register

1 USB3P0SS_CTRL_DEV_CFG_REG22 Register (Offset = 154h) [reset = 320h]

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Table 14-21805. Instance Table

Instance Name	Physical Address
USB0	**0F40 0154h**

Figure 14-7207. USB3P0SS_CTRL_DEV_CFG_REG22 Name Register

31	30	29	28	27	26	25	24
PM_ENTRY_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					PM_ENTRY_TIMEOUT		
R					R/W		
0h					320h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PM_ENTRY_TIMEOUT							
R/W							
320h							

Table 14-21807. USB3P0SS_CTRL_DEV_CFG_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	PM_ENTRY_TIMEOUT_PRESCALE	R/W	0h	PRESCALER for PM_ENTRY_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:11	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
10:0	PM_ENTRY_TIMEOUT	R/W	320h	PM_ENTRY_TIMEOUT value Resolution of this parameter is selected by PM_ENTRY_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 800*8ns =~6.4us [SystemC device ENV] - 800*8ns =~6.4us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 800*8ns =~6.4us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.318 USB3P0SS_CTRL_DEV_CFG_REG23 Register

1 USB3P0SS_CTRL_DEV_CFG_REG23 Register (Offset = 158h) [reset = 8000003Eh]

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Table 14-21808. Instance Table

Instance Name	Physical Address
USB0	**0F40 0158h**

Figure 14-7208. USB3P0SS_CTRL_DEV_CFG_REG23 Name Register

31	30	29	28	27	26	25	24
UX_EXIT_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
2h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	UX_EXIT_TIMEOUT						
R	R/W						
0h	3Eh						

Table 14-21810. USB3P0SS_CTRL_DEV_CFG_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	UX_EXIT_TIMEOUT_PRESCALE	R/W	2h	PRESCALER for UX_EXIT_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:7	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
6:0	UX_EXIT_TIMEOUT	R/W	3Eh	UX_EXIT_TIMEOUT value Resolution of this parameter is selected by UX_EXIT_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 8*100us =~800us [SystemC device ENV] - 3*100us =~300us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 62*100us =~6.2ms Reset Source: rst_mod_g_rst_n

14.9.2.3.2.319 USB3P0SS_CTRL_DEV_CFG_REG24 Register

1 USB3P0SS_CTRL_DEV_CFG_REG24 Register (Offset = 15Ch) [reset = 243D58h]

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Table 14-21811. Instance Table

Instance Name	Physical Address
USB0	**0F40 015Ch**

Figure 14-7209. USB3P0SS_CTRL_DEV_CFG_REG24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED	LFPS_DET_RESET_MIN						
R	R/W						
0h	243D58h						
15	14	13	12	11	10	9	8
LFPS_DET_RESET_MIN							
R/W							
243D58h							
7	6	5	4	3	2	1	0
LFPS_DET_RESET_MIN							
R/W							
243D58h							

Table 14-21813. USB3P0SS_CTRL_DEV_CFG_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
22:0	LFPS_DET_RESET_MIN	R/W	243D58h	LFPS_DET_RESET_MIN value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 395833 [~3.16ms] For synthesis purposes it is recommended to set the value 2375000 [~19ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.320 USB3P0SS_CTRL_DEV_CFG_REG25 Register

1 USB3P0SS_CTRL_DEV_CFG_REG25 Register (Offset = 160h) [reset = E4E1C0h]

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Table 14-21814. Instance Table

Instance Name	Physical Address
USB0	**0F40 0160h**

Figure 14-7210. USB3P0SS_CTRL_DEV_CFG_REG25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
LFPS_DET_RESET_MAX							
R/W							
E4E1C0h							
15	14	13	12	11	10	9	8
LFPS_DET_RESET_MAX							
R/W							
E4E1C0h							
7	6	5	4	3	2	1	0
LFPS_DET_RESET_MAX							
R/W							
E4E1C0h							

Table 14-21816. USB3P0SS_CTRL_DEV_CFG_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
23:0	LFPS_DET_RESET_MAX	R/W	E4E1C0h	LFPS_DET_RESET_MAX value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 5000000 [~40ms] For synthesis purposes it is recommended to set the value 15000000 [~120ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.321 USB3P0SS_CTRL_DEV_CFG_REG26 Register

1 USB3P0SS_CTRL_DEV_CFG_REG26 Register (Offset = 164h) [reset = 4Bh]

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Table 14-21817. Instance Table

Instance Name	Physical Address
USB0	**0F40 0164h**

Figure 14-7211. USB3P0SS_CTRL_DEV_CFG_REG26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	LFPS_DET_POLLING_MIN						
R	R/W						
0h	4Bh						

Table 14-21819. USB3P0SS_CTRL_DEV_CFG_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
6:0	LFPS_DET_POLLING_MIN	R/W	4Bh	LFPS_DET_POLLING_MIN value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 75 [~0.6us] For synthesis purposes it is recommended to set the value 75 [~0.6us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.322 USB3P0SS_CTRL_DEV_CFG_REG27 Register

1 USB3P0SS_CTRL_DEV_CFG_REG27 Register (Offset = 168h) [reset = BBh]

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Table 14-21820. Instance Table

Instance Name	Physical Address
USB0	**0F40 0168h**

Figure 14-7212. USB3P0SS_CTRL_DEV_CFG_REG27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LFPS_DET_POLLING_MAX							
R/W							
BBh							

Table 14-21822. USB3P0SS_CTRL_DEV_CFG_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	LFPS_DET_POLLING_MAX	R/W	BBh	LFPS_DET_POLLING_MAX value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 175 [~1.4us] For synthesis purposes it is recommended to set the value 175 [~1.4us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.323 USB3P0SS_CTRL_DEV_CFG_REG28 Register

1 USB3P0SS_CTRL_DEV_CFG_REG28 Register (Offset = 16Ch) [reset = 4h]

USB3.0 Configuration Register 28

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Table 14-21823. Instance Table

Instance Name	Physical Address
USB0	**0F40 016Ch**

Figure 14-7213. USB3P0SS_CTRL_DEV_CFG_REG28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					LFPS_DET_PING_MIN		
R					R/W		
0h					4h		

Table 14-21825. USB3P0SS_CTRL_DEV_CFG_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
2:0	LFPS_DET_PING_MIN	R/W	4h	LFPS_DET_PING_MIN value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 4 [~40ns] For synthesis purposes it is recommended to set the value 4 [~40ns] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.324 USB3P0SS_CTRL_DEV_CFG_REG29 Register

1 USB3P0SS_CTRL_DEV_CFG_REG29 Register (Offset = 170h) [reset = 17h]

USB3.0 Configuration Register 29

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Table 14-21826. Instance Table

Instance Name	Physical Address
USB0	**0F40 0170h**

Figure 14-7214. USB3P0SS_CTRL_DEV_CFG_REG29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			LFPS_DET_PING_MAX				
R			R/W				
0h			17h				

Table 14-21828. USB3P0SS_CTRL_DEV_CFG_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
4:0	LFPS_DET_PING_MAX	R/W	17h	LFPS_DET_PING_MAX value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 23 [~200ns] For synthesis purposes it is recommended to set the value 23 [~200ns] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.325 USB3P0SS_CTRL_DEV_CFG_REG30 Register

1 USB3P0SS_CTRL_DEV_CFG_REG30 Register (Offset = 174h) [reset = 24h]

USB3.0 Configuration Register 30 Note: In current version of the core this register is not implemented. Functionality of this register is provided by DBG_LINK1.LFPS_MIN_DET_U1_EXIT register.

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Table 14-21829. Instance Table

Instance Name	Physical Address
USB0	**0F40 0174h**

Figure 14-7215. USB3P0SS_CTRL_DEV_CFG_REG30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		LFPS_DET_U1EXIT_MIN					
R		R/W					
0h		24h					

Table 14-21831. USB3P0SS_CTRL_DEV_CFG_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
5:0	LFPS_DET_U1EXIT_MIN	R/W	24h	LFPS_DET_U1EXIT_MIN value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 36 [~300ns] For synthesis purposes it is recommended to set the value 36 [~300ns] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.326 USB3P0SS_CTRL_DEV_CFG_REG31 Register

1 USB3P0SS_CTRL_DEV_CFG_REG31 Register (Offset = 178h) [reset = 6Fh]

USB3.0 Configuration Register 31

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Table 14-21832. Instance Table

Instance Name	Physical Address
USB0	**0F40 0178h**

Figure 14-7216. USB3P0SS_CTRL_DEV_CFG_REG31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	LFPS_DET_U1EXIT_MAX						
R	R/W						
0h	6Fh						

Table 14-21834. USB3P0SS_CTRL_DEV_CFG_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
6:0	LFPS_DET_U1EXIT_MAX	R/W	6Fh	LFPS_DET_U1EXIT_MAX value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 111 [~900ns] For synthesis purposes it is recommended to set the value 111 [~900ns] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.327 USB3P0SS_CTRL_DEV_CFG_REG32 Register

1 USB3P0SS_CTRL_DEV_CFG_REG32 Register (Offset = 17Ch) [reset = 24h]

USB3.0 Configuration Register 32

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Table 14-21835. Instance Table

Instance Name	Physical Address
USB0	**0F40 017Ch**

Figure 14-7217. USB3P0SS_CTRL_DEV_CFG_REG32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">LFPS_DET_U2EXIT_MIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">24h</td></tr>
</table>

Table 14-21837. USB3P0SS_CTRL_DEV_CFG_REG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
5:0	LFPS_DET_U2EXIT_MIN	R/W	24h	LFPS_DET_U2EXIT_MIN value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 36 [~300ns] For synthesis purposes it is recommended to set the value 36 [~300ns] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.328 USB3P0SS_CTRL_DEV_CFG_REG33 Register

1 USB3P0SS_CTRL_DEV_CFG_REG33 Register (Offset = 180h) [reset = 3D090h]

USB3.0 Configuration Register 33

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Table 14-21838. Instance Table

Instance Name	Physical Address
USB0	**0F40 0180h**

Figure 14-7218. USB3P0SS_CTRL_DEV_CFG_REG33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						LFPS_DET_U2EXIT_MAX	
R						R/W	
0h						3D090h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LFPS_DET_U2EXIT_MAX							
R/W							
3D090h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LFPS_DET_U2EXIT_MAX							
R/W							
3D090h							

Table 14-21840. USB3P0SS_CTRL_DEV_CFG_REG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
17:0	LFPS_DET_U2EXIT_MAX	R/W	3D090h	LFPS_DET_U2EXIT_MAX value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 250000 [~2ms] For synthesis purposes it is recommended to set the value 250000 [~2ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.329 USB3P0SS_CTRL_DEV_CFG_REG34 Register

1 USB3P0SS_CTRL_DEV_CFG_REG34 Register (Offset = 184h) [reset = 24h]

USB3.0 Configuration Register 34

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Table 14-21841. Instance Table

Instance Name	Physical Address
USB0	**0F40 0184h**

Figure 14-7219. USB3P0SS_CTRL_DEV_CFG_REG34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		LFPS_DET_U3EXIT_MIN					
R		R/W					
0h		24h					

Table 14-21843. USB3P0SS_CTRL_DEV_CFG_REG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
5:0	LFPS_DET_U3EXIT_MIN	R/W	24h	LFPS_DET_U3EXIT_MIN value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 36 [~300ns] For synthesis purposes it is recommended to set the value 36 [~300ns] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.330 USB3P0SS_CTRL_DEV_CFG_REG35 Register

1 USB3P0SS_CTRL_DEV_CFG_REG35 Register (Offset = 188h) [reset = 1312D0h]

USB3.0 Configuration Register 35

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Table 14-21844. Instance Table

Instance Name	Physical Address
USB0	**0F40 0188h**

Figure 14-7220. USB3P0SS_CTRL_DEV_CFG_REG35 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			LFPS_DET_U3EXIT_MAX				
R			R/W				
0h			1312D0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LFPS_DET_U3EXIT_MAX							
R/W							
1312D0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LFPS_DET_U3EXIT_MAX							
R/W							
1312D0h							

Table 14-21846. USB3P0SS_CTRL_DEV_CFG_REG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
20:0	LFPS_DET_U3EXIT_MAX	R/W	1312D0h	LFPS_DET_U3EXIT_MAX value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 1250000 [~10ms] For synthesis purposes it is recommended to set the value 1250000 [~10ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.331 USB3P0SS_CTRL_DEV_CFG_REG36 Register

1 USB3P0SS_CTRL_DEV_CFG_REG36 Register (Offset = 1ACh) [reset = 18h]

USB3.0 Configuration Register 36 Note: In current version of the core this register is not implemented. Functionality of this register is provided by DBG_LINK1.LFPS_GEN_PING register.

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Table 14-21847. Instance Table

Instance Name	Physical Address
USB0	**0F40 01ACh**

Figure 14-7221. USB3P0SS_CTRL_DEV_CFG_REG36 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			LFPS_GEN_PING				
R			R/W				
0h			18h				

Table 14-21849. USB3P0SS_CTRL_DEV_CFG_REG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
4:0	LFPS_GEN_PING	R/W	18h	LFPS_GEN_PING value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 24 [~200ns] For synthesis purposes it is recommended to set the value 24 [~200ns] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.332 USB3P0SS_CTRL_DEV_CFG_REG37 Register

1 USB3P0SS_CTRL_DEV_CFG_REG37 Register (Offset = 1B0h) [reset = 7Dh]

USB3.0 Configuration Register 37

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Table 14-21850. Instance Table

Instance Name	Physical Address
USB0	**0F40 01B0h**

Figure 14-7222. USB3P0SS_CTRL_DEV_CFG_REG37 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
LFPS_GEN_POLLING							
R/W							
7Dh							

Table 14-21852. USB3P0SS_CTRL_DEV_CFG_REG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
7:0	LFPS_GEN_POLLING	R/W	7Dh	LFPS_GEN_POLLING value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 125 [~1us] For synthesis purposes it is recommended to set the value 125 [~1us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.333 USB3P0SS_CTRL_DEV_CFG_REG38 Register

1 USB3P0SS_CTRL_DEV_CFG_REG38 Register (Offset = 1B4h) [reset = 3D090h]

USB3.0 Configuration Register 38

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Table 14-21853. Instance Table

Instance Name	Physical Address
USB0	**0F40 01B4h**

Figure 14-7223. USB3P0SS_CTRL_DEV_CFG_REG38 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED						LFPS_GEN_U1EXIT	
R						R/W	
0h						3D090h	
15	14	13	12	11	10	9	8
LFPS_GEN_U1EXIT							
R/W							
3D090h							
7	6	5	4	3	2	1	0
LFPS_GEN_U1EXIT							
R/W							
3D090h							

Table 14-21855. USB3P0SS_CTRL_DEV_CFG_REG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
17:0	LFPS_GEN_U1EXIT	R/W	3D090h	LFPS_GEN_U1EXIT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 62500 [~500us] For synthesis purposes it is recommended to set the value 250000 [~2ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.334 USB3P0SS_CTRL_DEV_CFG_REG39 Register

1 USB3P0SS_CTRL_DEV_CFG_REG39 Register (Offset = 1B8h) [reset = 1312D0h]

USB3.0 Configuration Register 39

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Table 14-21856. Instance Table

Instance Name	Physical Address
USB0	**0F40 01B8h**

Figure 14-7224. USB3P0SS_CTRL_DEV_CFG_REG39 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED			LFPS_GEN_U3EXIT				
R			R/W				
0h			1312D0h				
15	14	13	12	11	10	9	8
LFPS_GEN_U3EXIT							
R/W							
1312D0h							
7	6	5	4	3	2	1	0
LFPS_GEN_U3EXIT							
R/W							
1312D0h							

Table 14-21858. USB3P0SS_CTRL_DEV_CFG_REG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
20:0	LFPS_GEN_U3EXIT	R/W	1312D0h	LFPS_GEN_U3EXIT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 125000 [~1ms] For synthesis purposes it is recommended to set the value 1250000 [~10ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.335 USB3P0SS_CTRL_DEV_CFG_REG40 Register

1 USB3P0SS_CTRL_DEV_CFG_REG40 Register (Offset = 1BCh) [reset = 1Fh]

USB3.0 Configuration Register 40 Note: In current version of the core this register is not implemented. Functionality of this register is provided by DBG_LINK1.LFPS_MIN_GEN_U1_EXIT register.

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Table 14-21859. Instance Table

Instance Name	Physical Address
USB0	**0F40 01BCh**

Figure 14-7225. USB3P0SS_CTRL_DEV_CFG_REG40 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">LFPS_MIN_GEN_U1EXIT</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">1Fh</td></tr>
</table>

Table 14-21861. USB3P0SS_CTRL_DEV_CFG_REG40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
6:0	LFPS_MIN_GEN_U1EXIT	R/W	1Fh	LFPS_MIN_GEN_U1EXIT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 87 [~696ns] For synthesis purposes it is recommended to set the value 87 [~696ns] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.336 USB3P0SS_CTRL_DEV_CFG_REG41 Register

1 USB3P0SS_CTRL_DEV_CFG_REG41 Register (Offset = 1C0h) [reset = 30D4h]

USB3.0 Configuration Register 41

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Table 14-21862. Instance Table

Instance Name	Physical Address
USB0	**0F40 01C0h**

Figure 14-7226. USB3P0SS_CTRL_DEV_CFG_REG41 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">LFPS_MIN_GEN_U2EXIT</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">30D4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LFPS_MIN_GEN_U2EXIT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">30D4h</td></tr>
</table>

Table 14-21864. USB3P0SS_CTRL_DEV_CFG_REG41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
14:0	LFPS_MIN_GEN_U2EXIT	R/W	30D4h	LFPS_MIN_GEN_U2EXIT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 12500 [~100us] For synthesis purposes it is recommended to set the value 12500 [~100us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.337 USB3P0SS_CTRL_DEV_CFG_REG42 Register

1 USB3P0SS_CTRL_DEV_CFG_REG42 Register (Offset = 1C4h) [reset = 4E2h]

USB3.0 Configuration Register 42

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Table 14-21865. Instance Table

Instance Name	Physical Address
USB0	**0F40 01C4h**

Figure 14-7227. USB3P0SS_CTRL_DEV_CFG_REG42 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED					LFPS_POLLING_REPEAT		
R					R/W		
0h					4E2h		
7	6	5	4	3	2	1	0
LFPS_POLLING_REPEAT							
R/W							
4E2h							

Table 14-21867. USB3P0SS_CTRL_DEV_CFG_REG42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
10:0	LFPS_POLLING_REPEAT	R/W	4E2h	LFPS_POLLING_REPEAT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 1250 [~10us] For synthesis purposes it is recommended to set the value 1250 [~10us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.338 USB3P0SS_CTRL_DEV_CFG_REG43 Register

1 USB3P0SS_CTRL_DEV_CFG_REG43 Register (Offset = 1C8h) [reset = 6D6h]

USB3.0 Configuration Register 43

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Table 14-21868. Instance Table

Instance Name	Physical Address
USB0	**0F40 01C8h**

Figure 14-7228. USB3P0SS_CTRL_DEV_CFG_REG43 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED					LFPS_POLLING_MAX_TREPEAT		
R					R/W		
0h					6D6h		
7	6	5	4	3	2	1	0
LFPS_POLLING_MAX_TREPEAT							
R/W							
6D6h							

Table 14-21870. USB3P0SS_CTRL_DEV_CFG_REG43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
10:0	LFPS_POLLING_MAX_TREPEAT	R/W	6D6h	LFPS_POLLING_MAX_TREPEAT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 1750 [~14us] For synthesis purposes it is recommended to set the value 1750 [~14us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.339 USB3P0SS_CTRL_DEV_CFG_REG44 Register

1 USB3P0SS_CTRL_DEV_CFG_REG44 Register (Offset = 1CCh) [reset = 2ECh]

USB3.0 Configuration Register 44

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Table 14-21871. Instance Table

Instance Name	Physical Address
USB0	**0F40 01CCh**

Figure 14-7229. USB3P0SS_CTRL_DEV_CFG_REG44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					LFPS_POLLING_MIN_TREPEAT		
R					R/W		
0h					2ECh		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LFPS_POLLING_MIN_TREPEAT							
R/W							
2ECh							

Table 14-21873. USB3P0SS_CTRL_DEV_CFG_REG44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
10:0	LFPS_POLLING_MIN_TREPEAT	R/W	2ECh	LFPS_POLLING_MIN_TREPEAT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 748 [~6us] For synthesis purposes it is recommended to set the value 748 [~6us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.340 USB3P0SS_CTRL_DEV_CFG_REG45 Register

1 USB3P0SS_CTRL_DEV_CFG_REG45 Register (Offset = 1D0h) [reset = 40000065h]

USB3.0 Configuration Register 45

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Table 14-21874. Instance Table

Instance Name	Physical Address
USB0	**0F40 01D0h**

Figure 14-7230. USB3P0SS_CTRL_DEV_CFG_REG45 Name Register

31	30	29	28	27	26	25	24
ITP_WAKEUP_TIMEOUT_PRESCALE		RESERVED					
R/W		R					
1h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	ITP_WAKEUP_TIMEOUT						
R	R/W						
0h	65h						

Table 14-21876. USB3P0SS_CTRL_DEV_CFG_REG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	ITP_WAKEUP_TIMEOUT_PRESCALE	R/W	1h	PRESCALER for ITP_WAKEUP_TIMEOUT value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:7	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
6:0	ITP_WAKEUP_TIMEOUT	R/W	65h	ITP_WAKEUP_TIMEOUT value Resolution of this parameter is selected by ITP_WAKEUP_TIMEOUT_PRESCALE. For simulation purposes it is recommended to set the value: - 101*1us =~100us [SystemC device ENV] - 101*1us =~100us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 101*1us =~100us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.341 USB3P0SS_CTRL_DEV_CFG_REG46 Register

1 USB3P0SS_CTRL_DEV_CFG_REG46 Register (Offset = 1D4h) [reset = FFFFh]

USB3.0 Configuration Register 46

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Table 14-21877. Instance Table

Instance Name	Physical Address
USB0	**0F40 01D4h**

Figure 14-7231. USB3P0SS_CTRL_DEV_CFG_REG46 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
TSEQ_QUANTITY							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
TSEQ_QUANTITY							
R/W							
FFFFh							

Table 14-21879. USB3P0SS_CTRL_DEV_CFG_REG46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
15:0	TSEQ_QUANTITY	R/W	FFFFh	TSEQ_QUANTITY value This parameter defines the number of TSEQ training sequences to be sent during Polling.RxEq state. For simulation purposes it is recommended to set the value 655 For synthesis purposes it is recommended to set the value 65535. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.342 USB3P0SS_CTRL_DEV_CFG_REG47 Register

1 USB3P0SS_CTRL_DEV_CFG_REG47 Register (Offset = 1D8h) [reset = 7D001h]

USB3.0 Configuration Register 47

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Table 14-21880. Instance Table

Instance Name	Physical Address
USB0	**0F40 01D8h**

Figure 14-7232. USB3P0SS_CTRL_DEV_CFG_REG47 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				ERDY_TIMEOUT_CNT			
R				R/W			
0h				7D001h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERDY_TIMEOUT_CNT							
R/W							
7D001h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERDY_TIMEOUT_CNT							
R/W							
7D001h							

Table 14-21882. USB3P0SS_CTRL_DEV_CFG_REG47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
19:0	ERDY_TIMEOUT_CNT	R/W	7D001h	ERDY_TIMEOUT_CNT value Resolution of this parameter is 1 us. For simulation purposes it is recommended to set the value 16 [~15 us] For synthesis purposes it is recommended to set the value ~512001 [~512ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.343 USB3P0SS_CTRL_DEV_CFG_REG48 Register

1 USB3P0SS_CTRL_DEV_CFG_REG48 Register (Offset = 1DCh) [reset = 18000h]

USB2.0 Configuration Register 48

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Table 14-21883. Instance Table

Instance Name	Physical Address
USB0	**0F40 01DCh**

Figure 14-7233. USB3P0SS_CTRL_DEV_CFG_REG48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						TWTRSTFS_J_CNT	
R						R/W	
0h						18000h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TWTRSTFS_J_CNT							
R/W							
18000h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TWTRSTFS_J_CNT							
R/W							
18000h							

Table 14-21885. USB3P0SS_CTRL_DEV_CFG_REG48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
17:0	TWTRSTFS_J_CNT	R/W	18000h	Time a device operating in full speed must wait before begin the transition to the Suspend state after it see a constant Idle state on their upstream facing bus lines. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 98304 [~3.28ms] For synthesis purposes it is recommended to set the value 98304 [~3.28ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.344 USB3P0SS_CTRL_DEV_CFG_REG49 Register

1 USB3P0SS_CTRL_DEV_CFG_REG49 Register (Offset = 1E0h) [reset = 8B00h]

USB2.0 Configuration Register 49

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Table 14-21886. Instance Table

Instance Name	Physical Address
USB0	**0F40 01E0h**

Figure 14-7234. USB3P0SS_CTRL_DEV_CFG_REG49 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TUCH_CNT							
R/W							
8B00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TUCH_CNT							
R/W							
8B00h							

Table 14-21888. USB3P0SS_CTRL_DEV_CFG_REG49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
15:0	TUCH_CNT	R/W	8B00h	TUCH: Minimum duration of a Chirp K from a high-speed capable device within the reset protocol. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 129 [~4.3us] For synthesis purposes it is recommended to set the value 35584 [~1.19ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.345 USB3P0SS_CTRL_DEV_CFG_REG50 Register

1 USB3P0SS_CTRL_DEV_CFG_REG50 Register (Offset = 1E4h) [reset = 960h]

USB2.0 Configuration Register 50

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Table 14-21889. Instance Table

Instance Name	Physical Address
USB0	**0F40 01E4h**

Figure 14-7235. USB3P0SS_CTRL_DEV_CFG_REG50 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TWAITCHK_CNT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">960h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TWAITCHK_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">960h</td></tr>
</table>

Table 14-21891. USB3P0SS_CTRL_DEV_CFG_REG50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
11:0	TWAITCHK_CNT	R/W	960h	Time to wait before device will start to drive Chirp K after detecting reset signalling. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 30 [~1us] For synthesis purposes it is recommended to set the value 2400 [~80us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.346 USB3P0SS_CTRL_DEV_CFG_REG51 Register

1 USB3P0SS_CTRL_DEV_CFG_REG51 Register (Offset = 1E8h) [reset = 19A03h]

USB2.0 Configuration Register 51

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Table 14-21892. Instance Table

Instance Name	Physical Address
USB0	**0F40 01E8h**

Figure 14-7236. USB3P0SS_CTRL_DEV_CFG_REG51 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>TWTFS_CNT</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>19A03h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TWTFS_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">19A03h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TWTFS_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">19A03h</td></tr>
</table>

Table 14-21894. USB3P0SS_CTRL_DEV_CFG_REG51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
16:0	TWTFS_CNT	R/W	19A03h	TWTFS: Time after end of upstream chirp at which device reverts to full speed default state if no downstream chirp is detected. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 1000 [~33.3us] For synthesis purposes it is recommended to set the value 104963 [~3.5ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.347 USB3P0SS_CTRL_DEV_CFG_REG52 Register

1 USB3P0SS_CTRL_DEV_CFG_REG52 Register (Offset = 1ECh) [reset = 16000h]

USB2.0 Configuration Register 52

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Table 14-21895. Instance Table

Instance Name	Physical Address
USB0	**0F40 01ECh**

Figure 14-7237. USB3P0SS_CTRL_DEV_CFG_REG52 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							TWTREV_CNT
R							R/W
0h							16000h
15	14	13	12	11	10	9	8
TWTREV_CNT							
R/W							
16000h							
7	6	5	4	3	2	1	0
TWTREV_CNT							
R/W							
16000h							

Table 14-21897. USB3P0SS_CTRL_DEV_CFG_REG52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
16:0	TWTREV_CNT	R/W	16000h	TWTREV: Time a high-speed capable device operating in high-speed must wait after start of SE0 before reverting to full-speed. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 90112 [~3ms] For synthesis purposes it is recommended to set the value 90112 [~3ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.348 USB3P0SS_CTRL_DEV_CFG_REG53 Register

1 USB3P0SS_CTRL_DEV_CFG_REG53 Register (Offset = 1F0h) [reset = 5C00h]

USB2.0 Configuration Register 53

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Table 14-21898. Instance Table

Instance Name	Physical Address
USB0	**0F40 01F0h**

Figure 14-7238. USB3P0SS_CTRL_DEV_CFG_REG53 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	TWTRSTHS_CNT						
R	R/W						
0h	5C00h						
7	6	5	4	3	2	1	0
TWTRSTHS_CNT							
R/W							
5C00h							

Table 14-21900. USB3P0SS_CTRL_DEV_CFG_REG53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
14:0	TWTRSTHS_CNT	R/W	5C00h	TWTRSTHS: Time a device must wait after reverting to full-speed before sampling the bus state for SE0 and beginning the high-speed detection handshake. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 23552 [~785us] For synthesis purposes it is recommended to set the value 23552 [~785us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.349 USB3P0SS_CTRL_DEV_CFG_REG54 Register

1 USB3P0SS_CTRL_DEV_CFG_REG54 Register (Offset = 1F4h) [reset = 24A00h]

USB2.0 Configuration Register 54

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Table 14-21901. Instance Table

Instance Name	Physical Address
USB0	**0F40 01F4h**

Figure 14-7239. USB3P0SS_CTRL_DEV_CFG_REG54 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">TWTRSM_CNT</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">24A00h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TWTRSM_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">24A00h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TWTRSM_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">24A00h</td></tr>
</table>

Table 14-21903. USB3P0SS_CTRL_DEV_CFG_REG54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
17:0	TWTRSM_CNT	R/W	24A00h	TWTRSM: Period of idle bus before device can initiate resume. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 150016 [~5ms] For synthesis purposes it is recommended to set the value 150016 [~5ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.350 USB3P0SS_CTRL_DEV_CFG_REG55 Register

1 USB3P0SS_CTRL_DEV_CFG_REG55 Register (Offset = 1F8h) [reset = 8000h]

USB2.0 Configuration Register 55

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Table 14-21904. Instance Table

Instance Name	Physical Address
USB0	**0F40 01F8h**

Figure 14-7240. USB3P0SS_CTRL_DEV_CFG_REG55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
TDRSMUP_CNT							
R/W							
8000h							
7	6	5	4	3	2	1	0
TDRSMUP_CNT							
R/W							
8000h							

Table 14-21906. USB3P0SS_CTRL_DEV_CFG_REG55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
15:0	TDRSMUP_CNT	R/W	8000h	TDRSMUP: Duration of driving resume upstream. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 32768 [~1.1ms] For synthesis purposes it is recommended to set the value 32768 [~1.1ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.351 USB3P0SS_CTRL_DEV_CFG_REG56 Register

1 USB3P0SS_CTRL_DEV_CFG_REG56 Register (Offset = 1FCh) [reset = 30h]

USB2.0 Configuration Register 56

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Table 14-21907. Instance Table

Instance Name	Physical Address
USB0	0F40 01FCh

Figure 14-7241. USB3P0SS_CTRL_DEV_CFG_REG56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		TOUTHS_CNT					
R		R/W					
0h		30h					

Table 14-21909. USB3P0SS_CTRL_DEV_CFG_REG56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
5:0	TOUTHS_CNT	R/W	30h	Time after device expecting a response to a transmission will timeout the transaction. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value 48 [~1.6us] For synthesis purposes it is recommended to set the value 48 [~1.6us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.352 USB3P0SS_CTRL_DEV_CFG_REG57 Register

1 USB3P0SS_CTRL_DEV_CFG_REG57 Register (Offset = 200h) [reset = 2h]

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Table 14-21910. Instance Table

Instance Name	Physical Address
USB0	**0F40 0200h**

Figure 14-7242. USB3P0SS_CTRL_DEV_CFG_REG57 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						LFPS_DEB_WIDTH	
R						R/W	
0h						2h	

Table 14-21912. USB3P0SS_CTRL_DEV_CFG_REG57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
1:0	LFPS_DEB_WIDTH	R/W	2h	LFPS_DEB_WIDTH value This parameter defines the LFPS debouncer delay. Only two values are allowed: 0x1 or 0x2. For simulation purposes it is recommended to set the value 1. For synthesis purposes it is recommended to set the value 2. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.353 USB3P0SS_CTRL_DEV_CFG_REG58 Register

1 USB3P0SS_CTRL_DEV_CFG_REG58 Register (Offset = 204h) [reset = 3D090h]

USB3.0 Configuration Register 58

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Table 14-21913. Instance Table

Instance Name	Physical Address
USB0	**0F40 0204h**

Figure 14-7243. USB3P0SS_CTRL_DEV_CFG_REG58 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						LFPS_GEN_U2EXIT	
R						R/W	
0h						3D090h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LFPS_GEN_U2EXIT							
R/W							
3D090h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LFPS_GEN_U2EXIT							
R/W							
3D090h							

Table 14-21915. USB3P0SS_CTRL_DEV_CFG_REG58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
17:0	LFPS_GEN_U2EXIT	R/W	3D090h	LFPS_GEN_U2EXIT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 62500 [~500us] For synthesis purposes it is recommended to set the value 250000 [~2ms] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.354 USB3P0SS_CTRL_DEV_CFG_REG59 Register

1 USB3P0SS_CTRL_DEV_CFG_REG59 Register (Offset = 208h) [reset = 30D4h]

USB3.0 Configuration Register 59

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Table 14-21916. Instance Table

Instance Name	Physical Address
USB0	**0F40 0208h**

Figure 14-7244. USB3P0SS_CTRL_DEV_CFG_REG59 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
LFPS_MIN_GEN_U3EXIT							
R/W							
30D4h							
7	6	5	4	3	2	1	0
LFPS_MIN_GEN_U3EXIT							
R/W							
30D4h							

Table 14-21918. USB3P0SS_CTRL_DEV_CFG_REG59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
15:0	LFPS_MIN_GEN_U3EXIT	R/W	30D4h	LFPS_MIN_GEN_U3EXIT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 12500 [~100us] For synthesis purposes it is recommended to set the value 12500 [~100us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.355 USB3P0SS_CTRL_DEV_CFG_REG60 Register

1 USB3P0SS_CTRL_DEV_CFG_REG60 Register (Offset = 20Ch) [reset = 15h]

USB3.0 Configuration Register 60

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Table 14-21919. Instance Table

Instance Name	Physical Address
USB0	**0F40 020Ch**

Figure 14-7245. USB3P0SS_CTRL_DEV_CFG_REG60 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">PORT_CONFIG_TIMEOUT</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">15h</td></tr>
</table>

Table 14-21921. USB3P0SS_CTRL_DEV_CFG_REG60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
6:0	PORT_CONFIG_TIMEOUT	R/W	15h	PORT_CONFIG_TIMEOUT value Resolution of this parameter is 1 us. For simulation purposes it is recommended to set the value 21 [~20us] For synthesis purposes it is recommended to set the value 21 [~20us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.356 USB3P0SS_CTRL_DEV_CFG_REG61 Register

1 USB3P0SS_CTRL_DEV_CFG_REG61 Register (Offset = 210h) [reset = FAh]

USB3.0 Configuration Register 61

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Table 14-21922. Instance Table

Instance Name	Physical Address
USB0	**0F40 0210h**

Figure 14-7246. USB3P0SS_CTRL_DEV_CFG_REG61 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED					LFPS_POL_LFPS_TO_RXEQ		
R					R/W		
0h					FAh		
7	6	5	4	3	2	1	0
LFPS_POL_LFPS_TO_RXEQ							
R/W							
FAh							

Table 14-21924. USB3P0SS_CTRL_DEV_CFG_REG61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
10:0	LFPS_POL_LFPS_TO_RXEQ	R/W	FAh	LFPS_POL_LFPS_TO_RXEQ value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value 250 [~2us] For synthesis purposes it is recommended to set the value 250 [~2us] Reset Source: rst_mod_g_rst_n

14.9.2.3.2.357 USB3P0SS_CTRL_DEV_CFG_REG62 Register

1 USB3P0SS_CTRL_DEV_CFG_REG62 Register (Offset = 214h) [reset = Bh]

USB3.0 Configuration Register 62

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Table 14-21925. Instance Table

Instance Name	Physical Address
USB0	**0F40 0214h**

Figure 14-7247. USB3P0SS_CTRL_DEV_CFG_REG62 Name Register

31	30	29	28	27	26	25	24
PHY_TX_LATENCY_PRESCALE		RESERVED					
R/W		R					
0h		0h					
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_TX_LATENCY					
R		R/W					
0h		Bh					

Table 14-21927. USB3P0SS_CTRL_DEV_CFG_REG62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	PHY_TX_LATENCY_PRESCALE	R/W	0h	PRESCALER for PHY_TX_LATENCY value: - 0x0 : 8ns [PHY pclk clock] - 0x1 : 1us - 0x2 : 100us - 0x3 : no clock - allows disabling certain timeout Reset Source: rst_mod_g_rst_n
29:6	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
5:0	PHY_TX_LATENCY	R/W	Bh	PHY_TX_LATENCY value This parameter defines latency from when data appear on PIPE interface to channel + 3 time units [defined by PHY_TX_LATENCY_PRESCALE]. For simulation purposes it is recommended to set the value 11. For synthesis purposes it is recommended to set the value 11 Reset Source: rst_mod_g_rst_n

14.9.2.3.2.358 USB3P0SS_CTRL_DEV_CFG_REG63 Register

1 USB3P0SS_CTRL_DEV_CFG_REG63 Register (Offset = 218h) [reset = 7CFFh]

USB3.0 Configuration Register 63

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Table 14-21928. Instance Table

Instance Name	Physical Address
USB0	**0F40 0218h**

Figure 14-7248. USB3P0SS_CTRL_DEV_CFG_REG63 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	U2_INACTIVITY_TMOUT						
R	R/W						
0h	7CFFh						
7	6	5	4	3	2	1	0
U2_INACTIVITY_TMOUT							
R/W							
7CFFh							

Table 14-21930. USB3P0SS_CTRL_DEV_CFG_REG63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
14:0	U2_INACTIVITY_TMOUT	R/W	7CFFh	U2_INACTIVITY_TMOUT value Resolution of this parameter is 8 ns. For simulation purposes it is recommended to set the value: - 31999*8ns =~256us [SystemC device ENV] - 249*8ns =~2us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 31999*8ns =~256us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.359 USB3P0SS_CTRL_DEV_CFG_REG64 Register

1 USB3P0SS_CTRL_DEV_CFG_REG64 Register (Offset = 220h) [reset = 4Ah]

USB2.0 Configuration Register 64

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Table 14-21931. Instance Table

Instance Name	Physical Address
USB0	**0F40 0220h**

Figure 14-7249. USB3P0SS_CTRL_DEV_CFG_REG64 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	TFILTSE0						
R	R/W						
0h	4Ah						

Table 14-21933. USB3P0SS_CTRL_DEV_CFG_REG64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
6:0	TFILTSE0	R/W	4Ah	TFILTSE0: Reset Handshake Protocol: Time for which a suspended highspeed capable device must see a continuous SE0 before beginning the high-speed detection handshake. Resolution of this parameter is 33.3ns. For simulation purposes it is recommended to set the value: - 74*33.3ns =~2.46us [SystemC device ENV] - 57*33.3ns =~1.9us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 74*33.3ns =~2.46us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.360 USB3P0SS_CTRL_DEV_CFG_REG65 Register

1 USB3P0SS_CTRL_DEV_CFG_REG65 Register (Offset = 224h) [reset = 4Bh]

USB2.0 Configuration Register 65

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Table 14-21934. Instance Table

Instance Name	Physical Address
USB0	**0F40 0224h**

Figure 14-7250. USB3P0SS_CTRL_DEV_CFG_REG65 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED						
R	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	TFILT						
NONE	R/W						
0h	4Bh						

Table 14-21936. USB3P0SS_CTRL_DEV_CFG_REG65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
14:7	RESERVED	NONE	0h	Reserved
6:0	TFILT	R/W	4Bh	TFILT: Time for which a Chirp J or Chirp K must be continuously detected [filtered] by hub or device during Reset handshake. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value: - 75*33.3ns =~2.5us [SystemC device ENV] - 57*33.3ns =~1.9us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 75*33.3ns =~2.5us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.361 USB3P0SS_CTRL_DEV_CFG_REG66 Register

1 USB3P0SS_CTRL_DEV_CFG_REG66 Register (Offset = 228h) [reset = 49h]

USB2.0 Configuration Register 66

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Table 14-21937. Instance Table

Instance Name	Physical Address
USB0	**0F40 0228h**

Figure 14-7251. USB3P0SS_CTRL_DEV_CFG_REG66 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED						
R	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	TWTRSTFS_SE0						
NONE	R/W						
0h	49h						

Table 14-21939. USB3P0SS_CTRL_DEV_CFG_REG66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
14:7	RESERVED	NONE	0h	Reserved
6:0	TWTRSTFS_SE0	R/W	49h	TWTRSTFS: Time a high-speed capable device operating in non-suspended fullspeed must wait after start of SE0 before beginning the high-speed detection handshake. Resolution of this parameter is 33.3 ns. For simulation purposes it is recommended to set the value: - 73*33.3ns =~2.43us [SystemC device ENV] - 57*33.3ns =~1.9us [VIP based ENV] For synthesis purposes it is recommended to set the value: - 73*33.3ns =~2.43us Reset Source: rst_mod_g_rst_n

14.9.2.3.2.362 USB3P0SS_CTRL_DEV_DMA_AXI_CTRL Register

1 USB3P0SS_CTRL_DEV_DMA_AXI_CTRL Register (Offset = 300h) [reset = 0h]

DMA AXI Initiator Control register. This register is optional, and implemented only when DMA has an AXI interface. This register configures the AXI initiator interface pins: marlock, marcache , marprot, mawlock, mawcache, mawprot are configurable by AXI Initiator Control register. The marcache and the mawcache width depends on the AXI release: AXI4/AXI3.

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Table 14-21940. Instance Table

Instance Name	Physical Address
USB0	**0F40 0300h**

Figure 14-7252. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED3</td><td colspan="2">MAWLOCK</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">MAWCACHE</td><td>RESERVED2</td><td colspan="3">MAWPROT</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td colspan="2">MARLOCK</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">MARCACHE</td><td>RESERVED0</td><td colspan="3">MARPROT</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-21942. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED3	R	0h	Reserved field. Write ignored. 0 when read
25:24	MAWLOCK	R/W	0h	The mawlock pin configuration Reset Source: rst_mod_g_rst_n
23:20	MAWCACHE	R/W	0h	The mawcache pin configuration Reset Source: rst_mod_g_rst_n
19	RESERVED2	R	0h	Reserved field. Write ignored. 0 when read
18:16	MAWPROT	R/W	0h	The mawprot pin configuration Reset Source: rst_mod_g_rst_n
15:10	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
9:8	MARLOCK	R/W	0h	The marlock pin configuration Reset Source: rst_mod_g_rst_n
7:4	MARCACHE	R/W	0h	The marcache pin configuration Reset Source: rst_mod_g_rst_n
3	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read

Table 14-21942. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	MARPROT	R/W	0h	The marprot pin configuration Reset Source: rst_mod_g_rst_n

14.9.2.3.2.363 USB3P0SS_CTRL_DEV_DMA_AXI_ID Register

1 USB3P0SS_CTRL_DEV_DMA_AXI_ID Register (Offset = 304h) [reset = 0h]

DMA AXI Initiator ID register. This register is optional, and implemented only when DMA has an AXI interface. Initiator ID width is configurable using CDNS_USBSSDEV_MAXI_ID_WIDTH define parameter (currently set to 4). Initially initiator will always output a value of zero regardless of the width. Value on the ID pins can be programmed using AXI Initiator ID register (DMA_AXI_ID) register.

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Table 14-21943. Instance Table

Instance Name	Physical Address
USB0	**0F40 0304h**

Figure 14-7253. USB3P0SS_CTRL_DEV_DMA_AXI_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED1</td><td colspan="5">MAR_ID</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED0</td><td colspan="5">MAW_ID</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-21945. USB3P0SS_CTRL_DEV_DMA_AXI_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
20:16	MAR_ID	R/W	0h	The marid pin configuration Reset Source: rst_mod_g_rst_n
15:5	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
4:0	MAW_ID	R/W	0h	The mawid and mwid pin configuration Reset Source: rst_mod_g_rst_n

14.9.2.3.2.364 USB3P0SS_CTRL_DEV_DMA_AXI_CAP Register

1 USB3P0SS_CTRL_DEV_DMA_AXI_CAP Register (Offset = 308h) [reset = 40000000h]

DMA AXI Initiator Extended Capability register. This register is optional, and implemented only when DMA has an AXI interface. It contains status of this AXI interface operations.

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Table 14-21946. Instance Table

Instance Name	Physical Address
USB0	0F40 0308h

Figure 14-7254. USB3P0SS_CTRL_DEV_DMA_AXI_CAP Name Register

31	30	29	28	27	26	25	24
RESERVED2	AXI_IDLE	AXI_SLVERR	AXI_DECERR	RESERVED1			
R	R	R/W1TC	R/W1TC	R			
0h	1h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1		AXI_SLVERR_EN	AXI_DECERR_EN	RESERVED0			
R		R/W	R/W	R			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED0							
R							
0h							

Table 14-21948. USB3P0SS_CTRL_DEV_DMA_AXI_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED2	R	0h	Reserved field. Write ignored. 0 when read
30	AXI_IDLE	R	1h	This bit provides information about the AXI Master state: '1': no pending action required by the AXI Master wrapper, '0': the AXI Master wrapper has outstanding transactions. Reset Source: rst_mod_g_rst_n
29	AXI_SLVERR	R/W1TC	0h	This bit provides an information about AXI SLAVE ERROR response on B or R channel. This flag is cleared by writing '1' to it. Once set it is held until cleared. Reset Source: rst_mod_g_rst_n
28	AXI_DECERR	R/W1TC	0h	This bit provides an information about AXI DECODE ERROR response on B or R channel. This flag is cleared by writing '1' to it. Once set it is held until cleared. Reset Source: rst_mod_g_rst_n
27:22	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
21	AXI_SLVERR_EN	R/W	0h	This bit enables interrupt on AXI SLAVE ERROR detection. When 1 and AXI_SLVERR is 1 then AXI SLAVE ERROR interrupt is requested. When 0 - disabled interrupt from this source Reset Source: rst_mod_g_rst_n

Table 14-21948. USB3P0SS_CTRL_DEV_DMA_AXI_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	AXI_DECERR_EN	R/W	0h	This bit enables interrupt on AXI DECODE ERROR detection. When 1 and AXI_DECERR is 1 then AXI DECODE ERROR interrupt is requested. When 0 - disabled interrupt from this source Reset Source: rst_mod_g_rst_n
19:0	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read

14.9.2.3.2.365 USB3P0SS_CTRL_DEV_DMA_AXI_CTRL0 Register

1 USB3P0SS_CTRL_DEV_DMA_AXI_CTRL0 Register (Offset = 30Ch) [reset = Fh]

DMA AXI Initiator Control0 register. This register is optional, and implemented only when DMA has an AXI interface with outstanding transactions support.

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Table 14-21949. Instance Table

Instance Name	Physical Address
USB0	**0F40 030Ch**

Figure 14-7255. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				B_MAX			
R				R/W			
0h				Fh			

Table 14-21951. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved field. Write ignored. 0 when read
3:0	B_MAX	R/W	Fh	The register controls maximum burst length - it is used by the AXI Master wrapper to determine maximum value of AxLEN. It uses AXI AxLEN encoding. Default value is the maximum supported one and it is implementation specific. Width of this register is the same as AxLEN signals width. Note: This register should only be written to during the register initialisation process Reset Source: rst_mod_g_rst_n

14.9.2.3.2.366 USB3P0SS_CTRL_DEV_DMA_AXI_CTRL1 Register

1 USB3P0SS_CTRL_DEV_DMA_AXI_CTRL1 Register (Offset = 310h) [reset = F000Fh]

DMA AXI Initiator Control1 register. This register is optional, and implemented only when DMA has an AXI interface with outstanding transactions support.

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Table 14-21952. Instance Table

Instance Name	Physical Address
USB0	**0F40 0310h**

Figure 14-7256. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1			WOT				
R			R/W				
0h			Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED0			ROT				
R			R/W				
0h			Fh				

Table 14-21954. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED1	R	0h	Reserved field. Write ignored. 0 when read
20:16	WOT	R/W	Fh	Number of outstanding write transactions that can be initiated by the AXI Master wrapper. Default value of this field is CDNS_USBSSDEV_AXI_WCD-1 [define parameter]. The value written to this field should be the requested number of outstanding write transactions minus 1, thus the actual number of possible outstanding write transactions is one more than the programmed value. Note: This register should only be written to during the register initialization process Reset Source: rst_mod_g_rst_n
15:5	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
4:0	ROT	R/W	Fh	Number of outstanding read transactions that can be initiated by the AXI Master wrapper. Default value of this field is CDNS_USBSSDEV_AXI_WCD-1 [define parameter]. The value written to this field should be the requested number of outstanding read transactions minus 1, thus the actual number of possible outstanding read transactions is one more than the programmed value. Note: This register should only be written to during the register initialization process Reset Source: rst_mod_g_rst_n

14.9.2.3.2.367 USB3P0SS_CTRL_DEV_DMA_AXI_CTRL2 Register

1 USB3P0SS_CTRL_DEV_DMA_AXI_CTRL2 Register (Offset = 314h) [reset = 1h]

AXI Initiator Wrapper Extended Capability Control Register 2. This register may be read from or written to at any time.

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Table 14-21955. Instance Table

Instance Name	Physical Address
USB0	**0F40 0314h**

Figure 14-7257. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESERVED0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED0	AXI_WTHRES						
R	R/W						
0h	1h						

Table 14-21957. USB3P0SS_CTRL_DEV_DMA_AXI_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED0	R	0h	Reserved field. Write ignored. 0 when read
6:0	AXI_WTHRES	R/W	1h	AXI Write Buffer Threshold, RW. When performing an AXI write burst this field specifies the minimum number of required AXI beats buffered prior to starting the burst on AXI W-Channel by asserting wvalid. This allows a user to balance the requirement for minimal latency with the requirement for low bus utilisation during bursts. Burst lengths smaller than or equal to this threshold will be buffered completely and then output on W-Channel. Burst lengths greater than this threshold will output the burst on the W-Channel such that the first AXI_WTHRES beats will be continuously with no drop of WVALID, beats thereafter may or may not be continuous depending on availability of data. Legal values are between 1 and 127. A value of 1 means that the burst is started on W-Channel as soon as any data is available without any additional delay. A value of 0 is reserved and should not be used as may lead to unpredictable behaviour. This register can be written only when the AXI Master wrapper is halted [AXI_HALT set to '1'] and idle [AXI_IDLE is '1']. Note: This register should only be written to during the register initialisation process. Reset Source: rst_mod_g_rst_n

14.9.2.3.2.368 USB3P0SS_CMN_PID Register

1 USB3P0SS_CMN_PID Register (Offset = 0h) [reset = 68232100h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-21958. Instance Table

Instance Name	Physical Address
USB0	**0F90 0000h**

Figure 14-7258. USB3P0SS_CMN_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		823h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
823h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
4h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-21960. USB3P0SS_CMN_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: sync_preset_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: sync_preset_n
27:16	MODULE_ID	R	823h	Module ID Reset Source: sync_preset_n
15:11	RTL	R	4h	RTL revision. Will vary depending on release. Reset Source: sync_preset_n
10:8	MAJOR	R	1h	Major revision Reset Source: sync_preset_n
7:6	CUSTOM	R	0h	Custom Reset Source: sync_preset_n
5:0	MINOR	R	0h	Minor revision Reset Source: sync_preset_n

14.9.2.3.2.369 USB3P0SS_CMN_USB3P0SS_W1 Register

1 USB3P0SS_CMN_USB3P0SS_W1 Register (Offset = 4h) [reset = 10000h]

Wrapper register containing soft reset, mode selection, and overcurrent indicator.

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Table 14-21961. Instance Table

Instance Name	Physical Address
USB0	**0F90 0004h**

Figure 14-7259. USB3P0SS_CMN_USB3P0SS_W1 Name Register

31	30	29	28	27	26	25	24
RSVD3							
R							
0h							
23	22	21	20	19	18	17	16
RSVD3				USB2_ONLY_MODE	MODESTRAP		OVERCURRENT_N
R				R/W	R/W		R/W
0h				0h	0h		1h
15	14	13	12	11	10	9	8
RSVD2						MODESTRAP_SEL	OVERCURRENT_SEL
R						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RSVD1							PWRUP_RST_N
R							R/W
0h							0h

Table 14-21963. USB3P0SS_CMN_USB3P0SS_W1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RSVD3	R	0h	Reserved bits set 3 Reset Source: sync_preset_n
19	USB2_ONLY_MODE	R/W	0h	Selects USB2 only mode. Has to be written before setting pwrup_rst_n bit. This bit has to be set when SERDES is not assigned to this USB instance. For example, when the Wiz is configured to allocate the serdes lanes for another function, like PCIe. Without setting this bit in those cases, the Controller will not function even at USB2 speeds, or may be erratic. Reset Source: sync_preset_n
18:17	MODESTRAP	R/W	0h	Modestrap input to the Controller. Has to be written before setting pwrup_rst_n bit. 00 - Controller not configured as Host or Device, 01 - Controller is initially configured as Host, 10 - Controller is initially configured as Device. Please refer to section 5.2 in DRD Controller Design Specification R1 for more information. Reset Source: sync_preset_n
16	OVERCURRENT_N	R/W	1h	Overcurrent indicator to the Controller Reset Source: sync_preset_n
15:10	RSVD2	R	0h	Reserved bits set 2 Reset Source: sync_preset_n

Table 14-21963. USB3P0SS_CMN_USB3P0SS_W1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MODESTRAP_SEL	R/W	0h	Select signal. Has to be written before setting pwrup_rst_n bit. 1 - modestrap MMR bits are used, 0 - usb_mode_strap input is used Reset Source: sync_preset_n
8	OVERCURRENT_SEL	R/W	0h	Overcurrent MMR select. Has to be written before setting pwrup_rst_n bit. 1 - overcurrent MMR bit is used, 0 - port_overcurrent_n input is used Reset Source: sync_preset_n
7:1	RSVD1	R	0h	Reserved bits set 1 Reset Source: sync_preset_n
0	PWRUP_RST_N	R/W	0h	Power up reset for the Controller. Set this bit after initialization steps like modestrap configuration, extended capability register configuration etc. Reset Source: sync_preset_n

14.9.2.3.2.370 USB3P0SS_CMN_STATIC_CONFIG Register

1 USB3P0SS_CMN_STATIC_CONFIG Register (Offset = 8h) [reset = 80h]

Wrapper register containing static settings. All bits in this register have to be written before setting pwrup_rst_n bit in USB3P0SS_W1 register. All bits in this register directly drive the USB2 PHY inputs. Please refer to USB2 PHY user guide for more information.

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Table 14-21964. Instance Table

Instance Name	Physical Address
USB0	**0F90 0008h**

Figure 14-7260. USB3P0SS_CMN_STATIC_CONFIG Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							PLL_REF_SEL
R							R/W
0h							4h
7	6	5	4	3	2	1	0
PLL_REF_SEL			LOOPBACK_MODE		VBUS_SEL		LANE_REVERSE
R/W			R/W		R/W		R/W
4h			0h		0h		0h

Table 14-21966. USB3P0SS_CMN_STATIC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RSVD	R	0h	Reserved bits Reset Source: sync_preset_n

Table 14-21966. USB3P0SS_CMN_STATIC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	PLL_REF_SEL	R/W	4h	This register directly drives the pllrefsel[3:0] input to USB2 PHY. Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should match the frequency value of either the HFOSC0 or HFOSC1 oscillator as selected by the USB0_CLKSEL register. Field values (Others are reserved): 4'b0000 - 9.6 MHz 4'b0001 - 10 MHz 4'b0010 - 12 MHz 4'b0011 - 18.2 MHz 4'b0100 - 20 MHz 4'b0101 - 24 MHz 4'b0110 - 25 MHz 4'b0111 - 26 MHz 4'b1000 - 38.4 MHz 4'b1001 - 40 MHz 4'b1010 - 48 MHz 4'b1011 - 50 MHz 4'b1100 - 52 MHz Reset Source: sync_preset_n
4:3	LOOPBACK_MODE	R/W	0h	This register directly drives the loopback[1:0] input to USB2 PHY. Loopback mode selection - 00: Loopback OFF, 01: LS Loopback ON, 10: FS Loopback ON, 11: HS Loopback ON. Reset Source: sync_preset_n
2:1	VBUS_SEL	R/W	0h	This register directly drives the vbus_sel[1:0] input to the PHY. VBUS select - 00: VBUS = 5.25V/3.3V, 01: VBUS/3 external divider is active, so VBUS could be upto 11V. Reset Source: sync_preset_n
0	LANE_REVERSE	R/W	0h	This register directly drives the lane_reverse input to USB2 PHY. Lane reverse selection. When set, this bit indicates that D+ and D- lines have to be swapped. Reset Source: sync_preset_n

14.9.2.3.2.371 USB3P0SS_CMN_PHY_TEST Register

1 USB3P0SS_CMN_PHY_TEST Register (Offset = Ch) [reset = 0h]

Register containing PLL bypass select, BIST control and status

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Table 14-21967. Instance Table

Instance Name	Physical Address
USB0	**0F90 000Ch**

Figure 14-7261. USB3P0SS_CMN_PHY_TEST Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RSVD</td><td>BIST_MODE</td><td>BIST_ERROR_COUNT</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">BIST_ERROR_COUNT</td><td>BIST_ERROR</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>BIST_COMPLETE</td><td>BIST_ON</td><td>BIST_MODE_EN</td><td colspan="4">BIST_MODE_SEL</td><td>PLL_BYPASS_MODE</td></tr>
<tr><td>R</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
</table>

Table 14-21969. USB3P0SS_CMN_PHY_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RSVD	R	0h	Reserved bits Reset Source: sync_preset_n
17	BIST_MODE	R/W	0h	Set for bist mode. This is used for overriding PHY ports for BIST. Reset Source: sync_preset_n
16:9	BIST_ERROR_COUNT	R	0h	Number of bytes that have errors while running BIST. The count resets when bist_on is set. Reset Source: sync_preset_n
8	BIST_ERROR	R	0h	If set, this bit indicates that BIST completed with error. Reset Source: sync_preset_n
7	BIST_COMPLETE	R	0h	If set, this bit indicates that the BIST operation is completed. Reset Source: sync_preset_n
6	BIST_ON	R/W	0h	Setting this bit starts the BIST operation. Reset Source: sync_preset_n
5	BIST_MODE_EN	R/W	0h	BIST Mode Enable. 0 = BIST not enabled, 1 = BIST enabled Reset Source: sync_preset_n

Table 14-21969. USB3P0SS_CMN_PHY_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:1	BIST_MODE_SEL	R/W	0h	BIST Mode Selection. bist_mode_sel[3]: 0 = 8-bit interface, 1 = 16-bit interface; bist_mode_sel[2]: 0 = error injection disabled, 1 = error injection enabled; bist_mode_sel[1]: 0 = device mode, 1 = host mode; bist_mode_sel[0]: 0 = High Speed mode, 1 = Full Speed mode. Reset Source: sync_preset_n
0	PLL_BYPASS_MODE	R/W	0h	Setting this bit disables the PLL clock and bypasses it with PLL reference clock. Reset Source: sync_preset_n

14.9.2.3.2.372 USB3P0SS_CMN_USB3P0SS_DEBUG_CTRL Register

1 USB3P0SS_CMN_USB3P0SS_DEBUG_CTRL Register (Offset = 10h) [reset = 0h]

USB Controller debug selection register

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Table 14-21970. Instance Table

Instance Name	Physical Address
USB0	**0F90 0010h**

Figure 14-7262. USB3P0SS_CMN_USB3P0SS_DEBUG_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RSVD</td><td colspan="5">DEBUG_SEL</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-21972. USB3P0SS_CMN_USB3P0SS_DEBUG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD	R	0h	Reserved bits Reset Source: sync_preset_n
4:0	DEBUG_SEL	R/W	0h	Debug selection Reset Source: sync_preset_n

14.9.2.3.2.373 USB3P0SS_CMN_USB3P0SS_DEBUG_INFO Register

1 USB3P0SS_CMN_USB3P0SS_DEBUG_INFO Register (Offset = 14h) [reset = 0h]

USB Controller debug information register

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Table 14-21973. Instance Table

Instance Name	Physical Address
USB0	**0F90 0014h**

Figure 14-7263. USB3P0SS_CMN_USB3P0SS_DEBUG_INFO Name Register

31	30	29	28	27	26	25	24
DEBUG_INFO							
R							
0h							
23	22	21	20	19	18	17	16
DEBUG_INFO							
R							
0h							
15	14	13	12	11	10	9	8
DEBUG_INFO							
R							
0h							
7	6	5	4	3	2	1	0
DEBUG_INFO							
R							
0h							

Table 14-21975. USB3P0SS_CMN_USB3P0SS_DEBUG_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEBUG_INFO	R	0h	Debug information selected by debug_sel Reset Source: sync_preset_n

14.9.2.3.2.374 USB3P0SS_CMN_USB3P0SS_DEBUG_LINK_STATE Register

1 USB3P0SS_CMN_USB3P0SS_DEBUG_LINK_STATE Register (Offset = 18h) [reset = 0h]

USB Controller debug link state information

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Table 14-21976. Instance Table

Instance Name	Physical Address
USB0	**0F90 0018h**

Figure 14-7264. USB3P0SS_CMN_USB3P0SS_DEBUG_LINK_STATE Name Register

31	30	29	28	27	26	25	24
RSVD	DEBUG_LINK_STATE						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DEBUG_LINK_STATE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DEBUG_LINK_STATE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEBUG_LINK_STATE							
R							
0h							

Table 14-21978. USB3P0SS_CMN_USB3P0SS_DEBUG_LINK_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RSVD	R	0h	Reserved bits Reset Source: sync_preset_n
30:0	DEBUG_LINK_STATE	R	0h	Debug link state information Reset Source: sync_preset_n

14.9.2.3.2.375 USB3P0SS_CMN_USB3P0SS_DEVICE_CTRL Register

1 USB3P0SS_CMN_USB3P0SS_DEVICE_CTRL Register (Offset = 1Ch) [reset = 0h]

Register for device control

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Table 14-21979. Instance Table

Instance Name	Physical Address
USB0	0F90 001Ch

Figure 14-7265. USB3P0SS_CMN_USB3P0SS_DEVICE_CTRL Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD							DEV_WAKEUP
R							R/W
0h							0h

Table 14-21981. USB3P0SS_CMN_USB3P0SS_DEVICE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RSVD	R	0h	Reserved bits Reset Source: sync_preset_n
0	DEV_WAKEUP	R/W	0h	Set this bit to trigger device wakeup interrupt on irq_intr[7] Reset Source: sync_preset_n

14.9.2.3.2.376 USB3P0SS_ERR_INJ_PID Register

1 USB3P0SS_ERR_INJ_PID Register (Offset = 0h) [reset = 60000001h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-21982. Instance Table

Instance Name	Physical Address
USB0	**0F90 1000h**

Figure 14-7266. USB3P0SS_ERR_INJ_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		0h			
23	22	21	20	19	18	17	16
FUNC							
R							
0h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
0h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-21984. USB3P0SS_ERR_INJ_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: rst_n
27:16	FUNC	R	0h	Module ID Reset Source: rst_n
15:11	RTL	R	0h	RTL revision. Will vary depending on release. Reset Source: rst_n
10:8	MAJOR	R	0h	Major revision Reset Source: rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: rst_n

14.9.2.3.2.377 USB3P0SS_ERR_INJ_INFO Register

1 USB3P0SS_ERR_INJ_INFO Register (Offset = 4h) [reset = 1Eh]

The Info Register gives the configuration Inforrmation of this module.

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Table 14-21985. Instance Table

Instance Name	Physical Address
USB0	**0F90 1004h**

Figure 14-7267. USB3P0SS_ERR_INJ_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ENDPOINTS					
NONE		R					
0h		1Eh					

Table 14-21987. USB3P0SS_ERR_INJ_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	ENDPOINTS	R	1Eh	Total number of Targets supported by this configuration Reset Source: rst_n

14.9.2.3.2.378 USB3P0SS_ERR_INJ_SFT_RST Register

1 USB3P0SS_ERR_INJ_SFT_RST Register (Offset = 8h) [reset = 0h]

The Global Soft Reset Register clears all programmable registers and returns the injector to idle state

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Table 14-21988. Instance Table

Instance Name	Physical Address
USB0	**0F90 1008h**

Figure 14-7268. USB3P0SS_ERR_INJ_SFT_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				W			
0h				0h			

Table 14-21990. USB3P0SS_ERR_INJ_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	W	0h	Write 4'b1010 to issue a soft reset. All other written values are ignored. Always read as 0 Reset Source: rst_n

14.9.2.3.2.379 USB3P0SS_ERR_INJ_BIT1 Register

1 USB3P0SS_ERR_INJ_BIT1 Register (Offset = 10h) [reset = 0h]

This register defines the first bit to be flipped when injection is enabled

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Table 14-21991. Instance Table

Instance Name	Physical Address
USB0	**0F90 1010h**

Figure 14-7269. USB3P0SS_ERR_INJ_BIT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
BIT1							
R/W							
0h							
7	6	5	4	3	2	1	0
BIT1							
R/W							
0h							

Table 14-21993. USB3P0SS_ERR_INJ_BIT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BIT1	R/W	0h	First bit to be flipped on an error injection Reset Source: rst_n

14.9.2.3.2.380 USB3P0SS_ERR_INJ_BIT2 Register

1 USB3P0SS_ERR_INJ_BIT2 Register (Offset = 14h) [reset = 0h]

This register defines the second bit to be flipped if 2-bit injection is enabled

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Table 14-21994. Instance Table

Instance Name	Physical Address
USB0	**0F90 1014h**

Figure 14-7270. USB3P0SS_ERR_INJ_BIT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
BIT2							
R/W							
0h							
7	6	5	4	3	2	1	0
BIT2							
R/W							
0h							

Table 14-21996. USB3P0SS_ERR_INJ_BIT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BIT2	R/W	0h	Second bit to be flipped on an error injection if 2-bit injection is chosen. Reset Source: rst_n

14.9.2.3.2.381 USB3P0SS_ERR_INJ_TRGT Register

1 USB3P0SS_ERR_INJ_TRGT Register (Offset = 18h) [reset = 0h]

This is the target selection regsiter

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Table 14-21997. Instance Table

Instance Name	Physical Address
USB0	**0F90 1018h**

Figure 14-7271. USB3P0SS_ERR_INJ_TRGT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			TRGT				
NONE			R/W				
0h			0h				

Table 14-21999. USB3P0SS_ERR_INJ_TRGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	TRGT	R/W	0h	Select which target to interact with. Writes of a value higher than the number of targets supported by this configuration will have no effect Reset Source: rst_n

14.9.2.3.2.382 USB3P0SS_ERR_INJ_CTRL Register

1 USB3P0SS_ERR_INJ_CTRL Register (Offset = 1Ch) [reset = 0h]

Controls the injection

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Table 14-22000. Instance Table

Instance Name	Physical Address
USB0	**0F90 101Ch**

Figure 14-7272. USB3P0SS_ERR_INJ_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			TRGT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED					DONE	TWOBIT	ONEBIT
NONE					R	R/W	R/W
0h					0h	0h	0h

Table 14-22002. USB3P0SS_ERR_INJ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:8	TRGT	R	0h	Indicates which target is selected by the TRGT register Reset Source: rst_n
7:3	RESERVED	NONE	0h	Reserved
2	DONE	R	0h	Indicates that the target selected by TRGT has completed error injection. This status supercedes the armed bit Reset Source: rst_n
1	TWOBIT	R/W	0h	Write 1 to trigger a 2-bit error in target selected by TRGT regsiter. Write 0 to finish or cancel 2-bit injection. If both 1 and 2-bit injection are set, 2-bit injection will be performed Reset Source: rst_n
0	ONEBIT	R/W	0h	Write 1 to trigger a 1-bit error in target selected by TRGT regsiter. Write 0 to finish or cancel 1-bit injection Reset Source: rst_n

14.9.2.3.2.383 USB3P0SS_ERR_INJ_STATUS Register

1 USB3P0SS_ERR_INJ_STATUS Register (Offset = 20h) [reset = 0h]

Controls the injection

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Table 14-22003. Instance Table

Instance Name	Physical Address
USB0	**0F90 1020h**

Figure 14-7273. USB3P0SS_ERR_INJ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ARMED	RESERVED	
NONE					R	NONE	
0h					0h	0h	

Table 14-22005. USB3P0SS_ERR_INJ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ARMED	R	0h	Indicates that the target selected by TRGT is ARMED for error injection Reset Source: rst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.2.3.2.384 USB3P0SS_PHY2_AFE_TX_REG0 Register

1 USB3P0SS_PHY2_AFE_TX_REG0 Register (Offset = 0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22006. Instance Table

Instance Name	Physical Address
USB0	**0F90 8000h**

Figure 14-7274. USB3P0SS_PHY2_AFE_TX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG0	BF_6_2					BF_1	BF_0
R/W	R/W					R/W	R/W
0h	0h					0h	0h

Table 14-22008. USB3P0SS_PHY2_AFE_TX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:2	BF_6_2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	BF_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.385 USB3P0SS_PHY2_AFE_TX_REG1 Register

1 USB3P0SS_PHY2_AFE_TX_REG1 Register (Offset = 4h) [reset = 0h]

HS TX trimming

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Table 14-22009. Instance Table

Instance Name	Physical Address
USB0	**0F90 8004h**

Figure 14-7275. USB3P0SS_PHY2_AFE_TX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG1	BF_6_1						BF_0
R/W	R/W						R/W
0h	0h						0h

Table 14-22011. USB3P0SS_PHY2_AFE_TX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG1	R/W	0h	0 SCALE1 VALUE IS 0, 1 SCALE1 VALUE IS 0.5 Reset Source: usb2_sync_preset_n

Table 14-22011. USB3P0SS_PHY2_AFE_TX_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:1	BF_6_1	R/W	0h	000000 BOOST CODE VALUE IS 0, 000001 BOOST CODE VALUE IS 1, 000010 BOOST CODE VALUE IS 2, 00011 BOOST CODE VALUE IS 3, 000100 BOOST CODE VALUE IS 4, 000101 BOOST CODE VALUE IS 5, 000110 BOOST CODE VALUE IS 6, 000111 BOOST CODE VALUE IS 7, 001000 BOOST CODE VALUE IS 8, 001001 BOOST CODE VALUE IS 9, 001010 BOOST CODE VALUE IS 10, 001011 BOOST CODE VALUE IS 11, 001100 BOOST CODE VALUE IS 12, 001101 BOOST CODE VALUE IS 13, 001110 BOOST CODE VALUE IS 14, 001111 BOOST CODE VALUE IS 15, 010000 BOOST CODE VALUE IS 16, 010001 BOOST CODE VALUE IS 17, 010010 BOOST CODE VALUE IS 18, 010011 BOOST CODE VALUE IS 19, 010100 BOOST CODE VALUE IS 20, 010101 BOOST CODE VALUE IS 21, 010110 BOOST CODE VALUE IS 22, 010111 BOOST CODE VALUE IS 23, 011000 BOOST CODE VALUE IS 24, 011001 BOOST CODE VALUE IS 24, 011010 BOOST CODE VALUE IS 26, 011011 BOOST CODE VALUE IS 27, 011100 BOOST CODE VALUE IS 28, 011101 BOOST CODE VALUE IS 29, 011110 BOOST CODE VALUE IS 30, 011111 BOOST CODE VALUE IS 31, 100000 BOOST CODE VALUE IS 16, 100001 BOOST CODE VALUE IS 17, 100010 BOOST CODE VALUE IS 18, 100011 BOOST CODE VALUE IS 19, 100100 BOOST CODE VALUE IS 20, 100101 BOOST CODE VALUE IS 21, 100110 BOOST CODE VALUE IS 22, 100111 BOOST CODE VALUE IS 23, 101000 BOOST CODE VALUE IS 24 , 101001 BOOST CODE VALUE IS 24, 101010 BOOST CODE VALUE IS 26, 101011 BOOST CODE VALUE IS 27, 101100 BOOST CODE VALUE IS 28, 101101 BOOST CODE VALUE IS 29, 101110 BOOST CODE VALUE IS 30, 101111 BOOST CODE VALUE IS 31, 110000 BOOST CODE VALUE IS 32, 110001 BOOST CODE VALUE IS 33, 110010 BOOST CODE VALUE IS 34, 110011 BOOST CODE VALUE IS 35, 110100 BOOST CODE VALUE IS 36, 110101 BOOST CODE VALUE IS 37, 110110 BOOST CODE VALUE IS 38, 110111 BOOST CODE VALUE IS 39, 111000 BOOST CODE VALUE IS 40, 111001 BOOST CODE VALUE IS 41, 111010 BOOST CODE VALUE IS 42, 111011 BOOST CODE VALUE IS 43, 111100 BOOST CODE VALUE IS 44, 111101 BOOST CODE VALUE IS 45, 111110 BOOST CODE VALUE IS 46, 111111 BOOST CODE VALUE IS 47. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	0 Default BOOST CODE = 8, 1 BOOST CODE can be controlled by BITS [6:1]. Reset Source: usb2_sync_preset_n

14.9.2.3.2.386 USB3P0SS_PHY2_AFE_TX_REG2 Register

1 USB3P0SS_PHY2_AFE_TX_REG2 Register (Offset = 8h) [reset = 0h]

HS TX trimming

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Table 14-22012. Instance Table

Instance Name	Physical Address
USB0	**0F90 8008h**

Figure 14-7276. USB3P0SS_PHY2_AFE_TX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG2	BF_6	BF_5_1					BF_0
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-22014. USB3P0SS_PHY2_AFE_TX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22014. USB3P0SS_PHY2_AFE_TX_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:1	BF_5_1	R/W	0h	00000 DEEMP CODE VALUE IS 0, 00001 DEEMP CODE VALUE IS 1, 00010 DEEMP CODE VALUE IS 2, 00011 DEEMP CODE VALUE IS 3, 00100 DEEMP CODE VALUE IS 4, 00101 DEEMP CODE VALUE IS 5, 00110 DEEMP CODE VALUE IS 6, 00111 DEEMP CODE VALUE IS 7, 01000 DEEMP CODE VALUE IS 8, 01001 DEEMP CODE VALUE IS 9, 01010 DEEMP CODE VALUE IS 10, 01011 DEEMP CODE VALUE IS 11, 01100 DEEMP CODE VALUE IS 12, 01101 DEEMP CODE VALUE IS 13, 01110 DEEMP CODE VALUE IS 14, 01111 DEEMP CODE VALUE IS 15, 10000 DEEMP CODE VALUE IS 8, 10001 DEEMP CODE VALUE IS 9, 10010 DEEMP CODE VALUE IS 10, 10011 DEEMP CODE VALUE IS 11, 10100 DEEMP CODE VALUE IS 12, 10101 DEEMP CODE VALUE IS 13, 10110 DEEMP CODE VALUE IS 14, 10111 DEEMP CODE VALUE IS 15, 11000 DEEMP CODE VALUE IS 16, 11001 DEEMP CODE VALUE IS 17, 11010 DEEMP CODE VALUE IS 18, 11011 DEEMP CODE VALUE IS 19, 11100 DEEMP CODE VALUE IS 20, 11101 DEEMP CODE VALUE IS 21, 11110 DEEMP CODE VALUE IS 22, 11111 DEEMP CODE VALUE IS 23. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	0 Default DEEMP CODE = 8, 1 DEEMP CODE can be controlled by BITS 5:1. Reset Source: usb2_sync_preset_n

14.9.2.3.2.387 USB3P0SS_PHY2_AFE_TX_REG3 Register

1 USB3P0SS_PHY2_AFE_TX_REG3 Register (Offset = Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22015. Instance Table

Instance Name	Physical Address
USB0	**0F90 800Ch**

Figure 14-7277. USB3P0SS_PHY2_AFE_TX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG3			BF_4_1				BF_0
R/W			R/W				R/W
0h			0h				0h

Table 14-22017. USB3P0SS_PHY2_AFE_TX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	TX_ANA_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	BF_4_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.388 USB3P0SS_PHY2_AFE_TX_REG4 Register

1 USB3P0SS_PHY2_AFE_TX_REG4 Register (Offset = 10h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22018. Instance Table

Instance Name	Physical Address
USB0	**0F90 8010h**

Figure 14-7278. USB3P0SS_PHY2_AFE_TX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG4	BF_6	BF_5	BF_4_1				BF_0
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 14-22020. USB3P0SS_PHY2_AFE_TX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BF_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	BF_4_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.389 USB3P0SS_PHY2_AFE_TX_REG5 Register

1 USB3P0SS_PHY2_AFE_TX_REG5 Register (Offset = 14h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22021. Instance Table

Instance Name	Physical Address
USB0	**0F90 8014h**

Figure 14-7279. USB3P0SS_PHY2_AFE_TX_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_TX_REG5	BF_6_1						BF_0
R/W	R/W						R/W
0h	0h						0h

Table 14-22023. USB3P0SS_PHY2_AFE_TX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	AFE_TX_REG5	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6:1	BF_6_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.390 USB3P0SS_PHY2_AFE_TX_REG6 Register

1 USB3P0SS_PHY2_AFE_TX_REG6 Register (Offset = 18h) [reset = 0h]

LSTX rise time trimming

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Table 14-22024. Instance Table

Instance Name	Physical Address
USB0	**0F90 8018h**

Figure 14-7280. USB3P0SS_PHY2_AFE_TX_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG6							
R/W							
0h							

Table 14-22026. USB3P0SS_PHY2_AFE_TX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG6	R/W	0h	Bit 7 = unused. Bbits 6:3= 0000 Typical LSTx rise time = 375ns, 0001 Typical LSTx rise time =215ns, 0010 Typical LSTx rise time =215ns, 0011 Typical LSTx rise time =150ns, 0100 Typical LSTx rise time =215ns, 0101 Typical LSTx rise time =150ns, 0110 Typical LSTx rise time =150ns, 0111 Typical LSTx rise time =115ns, 1000 Typical LSTx rise time =150ns, 1001 Typical LSTx rise time =115ns, 1010 Typical LSTx rise time =115ns, 1011 Typical LSTx rise time =94ns, 1100 Typical LSTx rise time =115ns, 1101 Typical LSTx rise time =94ns, 1110 Typical LSTx rise time =94ns, 1111 Typical LSTx rise time =79ns. Bit 6= 0 Typical LSTx rise time is set to default value of 150ns, 1 LSTX RISE TIME IS DETERMINED BY BITS 6:2. Bits 1:0 = reserved. Reset Source: usb2_sync_preset_n

14.9.2.3.2.391 USB3P0SS_PHY2_AFE_TX_REG7 Register

1 USB3P0SS_PHY2_AFE_TX_REG7 Register (Offset = 1Ch) [reset = 0h]

FSTX rise time trimming

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Table 14-22027. Instance Table

Instance Name	Physical Address
USB0	**0F90 801Ch**

Figure 14-7281. USB3P0SS_PHY2_AFE_TX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG7							
R/W							
0h							

Table 14-22029. USB3P0SS_PHY2_AFE_TX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG7	R/W	0h	Bits 7:5= reserved. Bits 4:1= 0000 Typical FSTx rise time = 16.6ns, 0001 Typical FSTx rise time =16.1ns, 0010 Typical FSTx rise time =15.6ns, 0011 Typical FSTx rise time =15.2ns, 0100 Typical FSTx rise time =14.7ns, 0101 Typical FSTx rise time =14.3ns, 0110 Typical FSTx rise time =13.9ns, 0111 Typical FSTx rise time =13.6ns, 1000 Typical FSTx rise time =13.2ns, 1001 Typical FSTx rise time =12.9ns, 1010 Typical FSTx rise time =12.6ns, 1011 Typical FSTx rise time =12.3ns, 1100 Typical FSTx rise time =12.0ns, 1101 Typical FSTx rise time =11.7ns, 1110 Typical FSTx rise time =11.5ns, 1111 Typical FSTx rise time =11.2ns. Bit 0= 0 FSTx rise time at typical corner is set to default value of 12ns, 1 FSTX RISE TIME IS DETERMINED BY BITS 4:1. Reset Source: usb2_sync_preset_n

14.9.2.3.2.392 USB3P0SS_PHY2_AFE_TX_REG8 Register

1 USB3P0SS_PHY2_AFE_TX_REG8 Register (Offset = 20h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22030. Instance Table

Instance Name	Physical Address
USB0	**0F90 8020h**

Figure 14-7282. USB3P0SS_PHY2_AFE_TX_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG8							
R/W							
0h							

Table 14-22032. USB3P0SS_PHY2_AFE_TX_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG8	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.393 USB3P0SS_PHY2_AFE_TX_REG9 Register

1 USB3P0SS_PHY2_AFE_TX_REG9 Register (Offset = 24h) [reset = 0h]

Register AFE_TX_REG9

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Table 14-22033. Instance Table

Instance Name	Physical Address
USB0	**0F90 8024h**

Figure 14-7283. USB3P0SS_PHY2_AFE_TX_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG9							
R/W							
0h							

Table 14-22035. USB3P0SS_PHY2_AFE_TX_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG9	R/W	0h	Bits 7:4= 0000 Typical LSTx fall time = 450ns, 0001 Typical LSTx fall time = 225ns, 0010 Typical LSTx fall time =150ns, 0011 Typical LSTx fall time =225ns, 0100 Typical LSTx fall time =150ns, 0101 Typical LSTx fall time =150ns, 0110 Typical LSTx fall time =112ns, 0111 Typical LSTx fall time =150ns, 1000 Typical LSTx fall time =112ns, 1001 Typical LSTx fall time =112ns, 1010 Typical LSTx fall time =90ns, 1011 Typical LSTx fall time =112ns, 1100 Typical LSTx fall time =90ns, 1101 Typical LSTx fall time =90ns, 1110 Typical LSTx fall time =75ns, 1111 Typical LSTx fall time = 150ns. bit 3 = 0 LSTX FALL TIME IS DETERMINED BY DESIGN, 1 LSTX FALL TIME IS DETERMINED BY BITS 7:4. Bits 2:1= reserved. Reset Source: usb2_sync_preset_n

14.9.2.3.2.394 USB3P0SS_PHY2_AFE_TX_REG10 Register

1 USB3P0SS_PHY2_AFE_TX_REG10 Register (Offset = 28h) [reset = 0h]

FSTX fall time trimming

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Table 14-22036. Instance Table

Instance Name	Physical Address
USB0	0F90 8028h

Figure 14-7284. USB3P0SS_PHY2_AFE_TX_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG10							
R/W							
0h							

Table 14-22038. USB3P0SS_PHY2_AFE_TX_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG10	R/W	0h	Bits 7:5= reserved. Bits 4:1= 0000 Typical FSTx fall time = 16.6ns, 0001 Typical FSTx fall time =16.1ns, 0010 Typical FSTx fall time =15.6ns, 0011 Typical FSTx fall time =15.2ns, 0100 Typical FSTx fall time =14.7ns, 0101 Typical FSTx fall time =14.3ns, 0110 Typical FSTx fall time =13.9ns, 0111 Typical FSTx fall time =13.6ns, 1000 Typical FSTx fall time =13.2ns, 1001 Typical FSTx fall time =12.9ns, 1010 Typical FSTx fall time =12.6ns, 1011 Typical FSTx fall time =12.3ns, 1100 Typical FSTx fall time =12ns, 1101 Typical FSTx fall time =11.7, 1110 Typical FSTx fall time =11.5ns, 1111 Typical FSTx fall time =11.2ns. bit 0 = 0 Typical FSTx fall time set to default value of 12ns, 1 FSTX fall TIME IS DETERMINED BY BITS 4:1. Reset Source: usb2_sync_preset_n

14.9.2.3.2.395 USB3P0SS_PHY2_AFE_TX_REG11 Register

1 USB3P0SS_PHY2_AFE_TX_REG11 Register (Offset = 2Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22039. Instance Table

Instance Name	Physical Address
USB0	**0F90 802Ch**

Figure 14-7285. USB3P0SS_PHY2_AFE_TX_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG11							
R/W							
0h							

Table 14-22041. USB3P0SS_PHY2_AFE_TX_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG11	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.396 USB3P0SS_PHY2_AFE_TX_REG12 Register

1 USB3P0SS_PHY2_AFE_TX_REG12 Register (Offset = 30h) [reset = 0h]

Register AFE_TX_REG12

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Table 14-22042. Instance Table

Instance Name	Physical Address
USB0	**0F90 8030h**

Figure 14-7286. USB3P0SS_PHY2_AFE_TX_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG12	BF_6	BF_5	BF_4	BF_3	BF_2	BF_1_0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-22044. USB3P0SS_PHY2_AFE_TX_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG12	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BF_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BF_4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	BF_3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	BF_2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22044. USB3P0SS_PHY2_AFE_TX_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	BF_1_0	R/W	0h	00- SCALE2 set to 0, 01- SCALE2 set to 1, 10- SCALE2 set to 1, 11- SCALE2 set to 2 Reset Source: usb2_sync_preset_n

14.9.2.3.2.397 USB3P0SS_PHY2_AFE_RX_REG0 Register

1 USB3P0SS_PHY2_AFE_RX_REG0 Register (Offset = 34h) [reset = 0h]

Trim the squelch threshold

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Table 14-22045. Instance Table

Instance Name	Physical Address
USB0	**0F90 8034h**

Figure 14-7287. USB3P0SS_PHY2_AFE_RX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG0							
R/W							
0h							

Table 14-22047. USB3P0SS_PHY2_AFE_RX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG0	R/W	0h	Bits 7:6= reserved. Bits 5:0= 000000 keep squelch threshold at default value, 100000 increade squelch threshold by 5mv, 110000 increade squelch threshold by 10mv, 111000 increase squelch threshold by 15mv, 000001 reduce squelch threshold by 5mv, 000011 reduce squelch threshold by 10mv, 000111 reduce squelch threshold by 15mv. Reset Source: usb2_sync_preset_n

14.9.2.3.2.398 USB3P0SS_PHY2_AFE_RX_REG1 Register

1 USB3P0SS_PHY2_AFE_RX_REG1 Register (Offset = 38h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22048. Instance Table

Instance Name	Physical Address
USB0	**0F90 8038h**

Figure 14-7288. USB3P0SS_PHY2_AFE_RX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_ANA_REG1							
R/W							
0h							

Table 14-22050. USB3P0SS_PHY2_AFE_RX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.399 USB3P0SS_PHY2_AFE_RX_REG2 Register

1 USB3P0SS_PHY2_AFE_RX_REG2 Register (Offset = 3Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22051. Instance Table

Instance Name	Physical Address
USB0	**0F90 803Ch**

Figure 14-7289. USB3P0SS_PHY2_AFE_RX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG2							
R/W							
0h							

Table 14-22053. USB3P0SS_PHY2_AFE_RX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG2	R/W	0h	reerved Reset Source: usb2_sync_preset_n

14.9.2.3.2.400 USB3P0SS_PHY2_AFE_RX_REG3 Register

1 USB3P0SS_PHY2_AFE_RX_REG3 Register (Offset = 40h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22054. Instance Table

Instance Name	Physical Address
USB0	**0F90 8040h**

Figure 14-7290. USB3P0SS_PHY2_AFE_RX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG3							
R/W							
0h							

Table 14-22056. USB3P0SS_PHY2_AFE_RX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.401 USB3P0SS_PHY2_AFE_RX_REG4 Register

1 USB3P0SS_PHY2_AFE_RX_REG4 Register (Offset = 44h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22057. Instance Table

Instance Name	Physical Address
USB0	0F90 8044h

Figure 14-7291. USB3P0SS_PHY2_AFE_RX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG4							
R/W							
0h							

Table 14-22059. USB3P0SS_PHY2_AFE_RX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.402 USB3P0SS_PHY2_AFE_RX_REG5 Register

1 USB3P0SS_PHY2_AFE_RX_REG5 Register (Offset = 48h) [reset = 0h]

Single ended receivers threshold trimming

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Table 14-22060. Instance Table

Instance Name	Physical Address
USB0	**0F90 8048h**

Figure 14-7292. USB3P0SS_PHY2_AFE_RX_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG5							
R/W							
0h							

Table 14-22062. USB3P0SS_PHY2_AFE_RX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG5	R/W	0h	Bits 7:3= reserved. Bits 2:1= 01 Switching thresholds for single ended receivers increased by 100mV, 10 Switching thresholds for single ended receivers reduced by 100mV. Bit 0= 0 Default Switching Thresholds for Single ended receivers, 1 SERx Switching Thresholds are controlled by bits [2:1]. Reset Source: usb2_sync_preset_n

14.9.2.3.2.403 USB3P0SS_PHY2_AFE_RX_REG6 Register

1 USB3P0SS_PHY2_AFE_RX_REG6 Register (Offset = 4Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22063. Instance Table

Instance Name	Physical Address
USB0	**0F90 804Ch**

Figure 14-7293. USB3P0SS_PHY2_AFE_RX_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG6							
R/W							
0h							

Table 14-22065. USB3P0SS_PHY2_AFE_RX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.404 USB3P0SS_PHY2_AFE_TX_REG13 Register

1 USB3P0SS_PHY2_AFE_TX_REG13 Register (Offset = 50h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22066. Instance Table

Instance Name	Physical Address
USB0	**0F90 8050h**

Figure 14-7294. USB3P0SS_PHY2_AFE_TX_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG13							
R							
0h							

Table 14-22068. USB3P0SS_PHY2_AFE_TX_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG13	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.405 USB3P0SS_PHY2_AFE_TX_REG14 Register

1 USB3P0SS_PHY2_AFE_TX_REG14 Register (Offset = 54h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22069. Instance Table

Instance Name	Physical Address
USB0	**0F90 8054h**

Figure 14-7295. USB3P0SS_PHY2_AFE_TX_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG14							
R							
0h							

Table 14-22071. USB3P0SS_PHY2_AFE_TX_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG14	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.406 USB3P0SS_PHY2_AFE_RX_REG7 Register

1 USB3P0SS_PHY2_AFE_RX_REG7 Register (Offset = 58h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22072. Instance Table

Instance Name	Physical Address
USB0	**0F90 8058h**

Figure 14-7296. USB3P0SS_PHY2_AFE_RX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG7							
R							
0h							

Table 14-22074. USB3P0SS_PHY2_AFE_RX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG7	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.407 USB3P0SS_PHY2_AFE_RX_REG8 Register

1 USB3P0SS_PHY2_AFE_RX_REG8 Register (Offset = 5Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22075. Instance Table

Instance Name	Physical Address
USB0	**0F90 805Ch**

Figure 14-7297. USB3P0SS_PHY2_AFE_RX_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG8							
R							
0h							

Table 14-22077. USB3P0SS_PHY2_AFE_RX_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG8	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.408 USB3P0SS_PHY2_AFE_UNUSED_REG0 Register

1 USB3P0SS_PHY2_AFE_UNUSED_REG0 Register (Offset = 60h) [reset = 0h]

AFE_UNUSED_REG0

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Table 14-22078. Instance Table

Instance Name	Physical Address
USB0	**0F90 8060h**

Figure 14-7298. USB3P0SS_PHY2_AFE_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_UNUSED_REG0							
R/W							
0h							

Table 14-22080. USB3P0SS_PHY2_AFE_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_UNUSED_REG0	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.409 USB3P0SS_PHY2_AFE_UNUSED_REG1 Register

1 USB3P0SS_PHY2_AFE_UNUSED_REG1 Register (Offset = 64h) [reset = 0h]

AFE_UNUSED_REG1

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Table 14-22081. Instance Table

Instance Name	Physical Address
USB0	**0F90 8064h**

Figure 14-7299. USB3P0SS_PHY2_AFE_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_UNUSED_REG1							
R/W							
0h							

Table 14-22083. USB3P0SS_PHY2_AFE_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_UNUSED_REG1	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.410 USB3P0SS_PHY2_AFE_BG_REG0 Register

1 USB3P0SS_PHY2_AFE_BG_REG0 Register (Offset = 80h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22084. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 8080h**

Figure 14-7300. USB3P0SS_PHY2_AFE_BG_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG0							
R/W							
0h							

Table 14-22086. USB3P0SS_PHY2_AFE_BG_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.411 USB3P0SS_PHY2_AFE_BG_REG1 Register

1 USB3P0SS_PHY2_AFE_BG_REG1 Register (Offset = 84h) [reset = 0h]

BG bias current trimming

Return to Summary Table

Table 14-22087. Instance Table

Instance Name	Physical Address
USB0	**0F90 8084h**

Figure 14-7301. USB3P0SS_PHY2_AFE_BG_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BG_ANA_REG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22089. USB3P0SS_PHY2_AFE_BG_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG1	R/W	0h	Bits 7:6= 00- PLL charge pump bias current 5uA, 01- PLL charge pump bias current 4uA, 10- PLL charge pump bias current 6uA, 11- PLL charge pump bias current 5uA. Bits 5:4= 00- PLL DAC bias bias current bias current 5uA, 01- PLL DAC bias bias current bias current 4uA, 10- PLL DAC bias current current 6uA, 11- PLL DAC bias current current 5uA. Bits 3:2= 00- PLL DAC cascode bias current current 5uA, 01- PLL DAC cascode bias current current 4uA, 10- PLL DAC cascode bias current current 6uA, 11- PLL DAC cascode bias current current 5uA. Bits 1:0= 00- OTG block bias current 5uA, 01- OTG block bias current 6uA, 10- OTG block bias current 6uA, 11- OTG block bias current 5uA. Reset Source: usb2_sync_preset_n

14.9.2.3.2.412 USB3P0SS_PHY2_AFE_BG_REG2 Register

1 USB3P0SS_PHY2_AFE_BG_REG2 Register (Offset = 88h) [reset = 0h]

BG bias current trimming

Return to Summary Table

Table 14-22090. Instance Table

Instance Name	Physical Address
USB0	**0F90 8088h**

Figure 14-7302. USB3P0SS_PHY2_AFE_BG_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG2							
R/W							
0h							

Table 14-22092. USB3P0SS_PHY2_AFE_BG_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG2	R/W	0h	Bits 7:5= 000 High speed receiver bias 5uA, 100 High speed receiver bias 1uA, 001 High speed receiver bias 4uA, 010 High speed receiver bias 6uA, 101 High speed receiver bias 2uA. Bits 4:2= 000 Trasmission Envelope Detector bias current 5uA, 100 Trasmission Envelope Detector bias current 1uA, 001 Trasmission Envelope Detector bias current 4uA, 101 Trasmission Envelope Detector bias current 6uA, 101 Trasmission Envelope Detector bias current 2uA. Bits 1:0=00 PLL LDO bias current 5uA, 01 PLL LDO bias current 6uA, 10 PLL LDO bias current 4uA, 11 PLL LDO bias current 5uA Reset Source: usb2_sync_preset_n

14.9.2.3.2.413 USB3P0SS_PHY2_AFE_BG_REG3 Register

1 USB3P0SS_PHY2_AFE_BG_REG3 Register (Offset = 8Ch) [reset = 2h]

Register AFE_BG_REG3

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Table 14-22093. Instance Table

Instance Name	Physical Address
USB0	**0F90 808Ch**

Figure 14-7303. USB3P0SS_PHY2_AFE_BG_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG3							
R/W							
2h							

Table 14-22095. USB3P0SS_PHY2_AFE_BG_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG3	R/W	2h	Bits 7:6= reserved, Bits 5:4= 00 [Default] BG_OK_CORE Generated Internally, 01 BG_OK_CORE Generated Internally, 10 Force BG_OK_CORE =0, 11 Force BG_OK_CORE =1. Bits 3:0=0000 Invalid state, 0001 Higher start sense voltage, weaker start-up pull down, 0010 Default start sense voltage, 0100 Low start sense voltage, strong start-up pull down, 1000 Lowest start sense voltage, strongest start-up pull down. Reset Source: usb2_sync_preset_n

14.9.2.3.2.414 USB3P0SS_PHY2_AFE_CALIB_REG0 Register

1 USB3P0SS_PHY2_AFE_CALIB_REG0 Register (Offset = 90h) [reset = 0h]

Calibration resistance trimming

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Table 14-22096. Instance Table

Instance Name	Physical Address
USB0	**0F90 8090h**

Figure 14-7304. USB3P0SS_PHY2_AFE_CALIB_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_ANA_REG0							
R/W							
0h							

Table 14-22098. USB3P0SS_PHY2_AFE_CALIB_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CALIB_ANA_REG0	R/W	0h	Bits 5:0= 000000 Calibrate termination resistor to default value, 000001 Calibrate termination resistor by -%5 to default value, 000011 Calibrate termination resistor by -%10 to default value, 000111 Calibrate termination resistor by - %15 to default value, 001000 Calibrate termination resistor by +5% to default value, 011000 Calibrate termination resistor by +10% to default value, 111000 Calibrate termination resistor by +15% to default value. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.9.2.3.2.415 USB3P0SS_PHY2_AFE_BC_REG0 Register

1 USB3P0SS_PHY2_AFE_BC_REG0 Register (Offset = 94h) [reset = 0h]

register AFE_BC_REG0

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Table 14-22099. Instance Table

Instance Name	Physical Address
USB0	**0F90 8094h**

Figure 14-7305. USB3P0SS_PHY2_AFE_BC_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG0							
R/W							
0h							

Table 14-22101. USB3P0SS_PHY2_AFE_BC_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved

Table 14-22101. USB3P0SS_PHY2_AFE_BC_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	BC_ANA_REG0	R/W	0h	Bit 0= 0 Battery_charging_DAC_RES_CALIB CODE CANNOT BE CONTROLLED BY ANALOG TEST BITS, 1 Battery_charging_DAC_RES_CALIB CODE CAN BE CONTROLLED BY ANALOG TEST BITS. Bits 5:1= 00000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 0, 00001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 1, 00010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 2, 00011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 3, 00100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 4, 00101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 5, 00110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 6, 00111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 7, 01000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 8, 01001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 9, 01010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 10, 01011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 11, 01100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 12, 01101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 13, 01110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 14, 01111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 15, 10000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 16, 10001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 17, 10010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 18, 10011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 19, 10100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 20, 10101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 21, 10110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 22, 10111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 23, 11000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 24, 11001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 24, 11010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 26, 11011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 27, 11100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 28, 11101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 29, 11110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 30, 11111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 31. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.9.2.3.2.416 USB3P0SS_PHY2_AFE_BC_REG1 Register

1 USB3P0SS_PHY2_AFE_BC_REG1 Register (Offset = 98h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22102. Instance Table

Instance Name	Physical Address
USB0	**0F90 8098h**

Figure 14-7306. USB3P0SS_PHY2_AFE_BC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BC_ANA_REG1							
R/W							
0h							

Table 14-22104. USB3P0SS_PHY2_AFE_BC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.417 USB3P0SS_PHY2_AFE_BC_REG2 Register

1 USB3P0SS_PHY2_AFE_BC_REG2 Register (Offset = 9Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22105. Instance Table

Instance Name	Physical Address
USB0	**0F90 809Ch**

Figure 14-7307. USB3P0SS_PHY2_AFE_BC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG2							
R/W							
0h							

Table 14-22107. USB3P0SS_PHY2_AFE_BC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.418 USB3P0SS_PHY2_AFE_BC_REG3 Register

1 USB3P0SS_PHY2_AFE_BC_REG3 Register (Offset = A0h) [reset = 0h]

Register AFE_BC_REG3

Return to Summary Table

Table 14-22108. Instance Table

Instance Name	Physical Address
USB0	**0F90 80A0h**

Figure 14-7308. USB3P0SS_PHY2_AFE_BC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG3							
R/W							
0h							

Table 14-22110. USB3P0SS_PHY2_AFE_BC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG3	R/W	0h	Bit 0= 0 Do not overdrive SESS_VLD comparator enable signal, 1 Overdrive SESS_VLD comparator enable signal. Bit 1= 0 SESS_VLD comparator disabled, 1 SESS_VLD comparator enabled. Bit 2= 0 Do not overdrive VBUS_VLD comparator enable signal, 1 Overdrive VBUS_VLD comparator enable signal. Bit 3= 0 VBUS_VLD comparator disabled, 1 VBUS_VLD comparator enabled. Bit 4= 0 Do not overdrive ID comparator enable signal, 1 Overdrive ID comparator enable signal. Bit 5= 0 ID comparator disabled, 1 ID comparator enabled. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.9.2.3.2.419 USB3P0SS_PHY2_AFE_BC_REG4 Register

1 USB3P0SS_PHY2_AFE_BC_REG4 Register (Offset = A4h) [reset = 0h]

Register AFE_BC_REG4

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Table 14-22111. Instance Table

Instance Name	Physical Address
USB0	0F90 80A4h

Figure 14-7309. USB3P0SS_PHY2_AFE_BC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG4							
R/W							
0h							

Table 14-22113. USB3P0SS_PHY2_AFE_BC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG4	R/W	0h	Bits 2:0= reserved. Bit 3= 0- VBUS_VLD comparator output low, 1- VBUS_VLD comparator output high. Bit 4= 0- Do not overdrive VBUS_VLD comparator output, 1- Overdrive VBUS_VLD comparator output. Bit 5= 0- SESS_VLD comparator output low, 1- SESS_VLD comparator output high. Bit 6= 0- Do not overdrive SESS_VLD comparator output, 1- Overdrive SESS_VLD comparator output. Bit 7= 0- ID comparator output low, 1- ID comparator output high. Reset Source: usb2_sync_preset_n

14.9.2.3.2.420 USB3P0SS_PHY2_AFE_BC_REG5 Register

1 USB3P0SS_PHY2_AFE_BC_REG5 Register (Offset = A8h) [reset = 0h]

Register AFE_BC_REG5

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Table 14-22114. Instance Table

Instance Name	Physical Address
USB0	0F90 80A8h

Figure 14-7310. USB3P0SS_PHY2_AFE_BC_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG5							
R/W							
0h							

Table 14-22116. USB3P0SS_PHY2_AFE_BC_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG5	R/W	0h	Bit 0= 0- Do not overdrive ID comparator output, 1- Overdrive ID comparator output. Bit 1= 0 Do not overdrive VBUS_DIV signal, 1- Overdrive VBUS_DIV signal. Bit 2= 0- VBUS_DIV signal low, 1- VBUS_DIV signal high. Bits 7:3= reserved. Reset Source: usb2_sync_preset_n

14.9.2.3.2.421 USB3P0SS_PHY2_AFE_BC_REG6 Register

1 USB3P0SS_PHY2_AFE_BC_REG6 Register (Offset = ACh) [reset = 0h]

Register AFE_BC_REG6

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Table 14-22117. Instance Table

Instance Name	Physical Address
USB0	**0F90 80ACh**

Figure 14-7311. USB3P0SS_PHY2_AFE_BC_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG6							
R/W							
0h							

Table 14-22119. USB3P0SS_PHY2_AFE_BC_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG6	R/W	0h	register AFE_BC_REG6 Reset Source: usb2_sync_preset_n

14.9.2.3.2.422 USB3P0SS_PHY2_AFE_PLL_REG0 Register

1 USB3P0SS_PHY2_AFE_PLL_REG0 Register (Offset = B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22120. Instance Table

Instance Name	Physical Address
USB0	**0F90 80B0h**

Figure 14-7312. USB3P0SS_PHY2_AFE_PLL_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG0							
R/W							
0h							

Table 14-22122. USB3P0SS_PHY2_AFE_PLL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.423 USB3P0SS_PHY2_AFE_PLL_REG1 Register

1 USB3P0SS_PHY2_AFE_PLL_REG1 Register (Offset = B4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22123. Instance Table

Instance Name	Physical Address
USB0	**0F90 80B4h**

Figure 14-7313. USB3P0SS_PHY2_AFE_PLL_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">AFE_PLL_REG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22125. USB3P0SS_PHY2_AFE_PLL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.424 USB3P0SS_PHY2_AFE_PLL_REG2 Register

1 USB3P0SS_PHY2_AFE_PLL_REG2 Register (Offset = B8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22126. Instance Table

Instance Name	Physical Address
USB0	**0F90 80B8h**

Figure 14-7314. USB3P0SS_PHY2_AFE_PLL_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG2							
R/W							
0h							

Table 14-22128. USB3P0SS_PHY2_AFE_PLL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.425 USB3P0SS_PHY2_AFE_PLL_REG3 Register

1 USB3P0SS_PHY2_AFE_PLL_REG3 Register (Offset = BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22129. Instance Table

Instance Name	Physical Address
USB0	**0F90 80BCh**

Figure 14-7315. USB3P0SS_PHY2_AFE_PLL_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AFE_PLL_REG3							
R/W							
0h							

Table 14-22131. USB3P0SS_PHY2_AFE_PLL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.426 USB3P0SS_PHY2_AFE_PLL_REG4 Register

1 USB3P0SS_PHY2_AFE_PLL_REG4 Register (Offset = C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22132. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 80C0h**

Figure 14-7316. USB3P0SS_PHY2_AFE_PLL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG4							
R/W							
0h							

Table 14-22134. USB3P0SS_PHY2_AFE_PLL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.427 USB3P0SS_PHY2_AFE_PLL_REG5 Register

1 USB3P0SS_PHY2_AFE_PLL_REG5 Register (Offset = C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22135. Instance Table

Instance Name	Physical Address
USB0	**0F90 80C4h**

Figure 14-7317. USB3P0SS_PHY2_AFE_PLL_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG5							
R/W							
0h							

Table 14-22137. USB3P0SS_PHY2_AFE_PLL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.428 USB3P0SS_PHY2_AFE_BG_REG4 Register

1 USB3P0SS_PHY2_AFE_BG_REG4 Register (Offset = C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22138. Instance Table

Instance Name	Physical Address
USB0	**0F90 80C8h**

Figure 14-7318. USB3P0SS_PHY2_AFE_BG_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG4							
R							
0h							

Table 14-22140. USB3P0SS_PHY2_AFE_BG_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG4	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.429 USB3P0SS_PHY2_AFE_CALIB_REG1 Register

1 USB3P0SS_PHY2_AFE_CALIB_REG1 Register (Offset = CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22141. Instance Table

Instance Name	Physical Address
USB0	0F90 80CCh

Figure 14-7319. USB3P0SS_PHY2_AFE_CALIB_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_ANA_REG1							
R							
0h							

Table 14-22143. USB3P0SS_PHY2_AFE_CALIB_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CALIB_ANA_REG1	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.430 USB3P0SS_PHY2_AFE_BC_REG7 Register

1 USB3P0SS_PHY2_AFE_BC_REG7 Register (Offset = D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22144. Instance Table

Instance Name	Physical Address
USB0	**0F90 80D0h**

Figure 14-7320. USB3P0SS_PHY2_AFE_BC_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG7							
R							
0h							

Table 14-22146. USB3P0SS_PHY2_AFE_BC_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG7	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.431 USB3P0SS_PHY2_AFE_PLL_REG6 Register

1 USB3P0SS_PHY2_AFE_PLL_REG6 Register (Offset = D4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22147. Instance Table

Instance Name	Physical Address
USB0	**0F90 80D4h**

Figure 14-7321. USB3P0SS_PHY2_AFE_PLL_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_ANA_REG6							
R							
0h							

Table 14-22149. USB3P0SS_PHY2_AFE_PLL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PLL_ANA_REG6	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.432 USB3P0SS_PHY2_AFE_UNUSED_REG2 Register

1 USB3P0SS_PHY2_AFE_UNUSED_REG2 Register (Offset = D8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22150. Instance Table

Instance Name	Physical Address
USB0	**0F90 80D8h**

Figure 14-7322. USB3P0SS_PHY2_AFE_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22152. USB3P0SS_PHY2_AFE_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.433 USB3P0SS_PHY2_AFE_UNUSED_REG3 Register

1 USB3P0SS_PHY2_AFE_UNUSED_REG3 Register (Offset = DCh) [reset = 0h]

AFE_UNUSED_REG3

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Table 14-22153. Instance Table

Instance Name	Physical Address
USB0	0F90 80DCh

Figure 14-7323. USB3P0SS_PHY2_AFE_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22155. USB3P0SS_PHY2_AFE_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.434 USB3P0SS_PHY2_PLL_REG0 Register

1 USB3P0SS_PHY2_PLL_REG0 Register (Offset = 100h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22156. Instance Table

Instance Name	Physical Address
USB0	**0F90 8100h**

Figure 14-7324. USB3P0SS_PHY2_PLL_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INITIAL_WAIT_TIME							
R/W							
0h							

Table 14-22158. USB3P0SS_PHY2_PLL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INITIAL_WAIT_TIME	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.435 USB3P0SS_PHY2_PLL_REG1 Register

1 USB3P0SS_PHY2_PLL_REG1 Register (Offset = 104h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22159. Instance Table

Instance Name	Physical Address
USB0	**0F90 8104h**

Figure 14-7325. USB3P0SS_PHY2_PLL_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RST_FDBK_DIV_DELAY_VALUE					RST_FDBK_DIV_DELAY_EN	FBDIV_EN	INITIAL_WAIT_TIME_EN
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-22161. USB3P0SS_PHY2_PLL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	RST_FDBK_DIV_DELAY_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RST_FDBK_DIV_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	FBDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	INITIAL_WAIT_TIME_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.436 USB3P0SS_PHY2_PLL_REG2 Register

1 USB3P0SS_PHY2_PLL_REG2 Register (Offset = 108h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22162. Instance Table

Instance Name	Physical Address
USB0	**0F90 8108h**

Figure 14-7326. USB3P0SS_PHY2_PLL_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED	VCO_SETTLING_TIME_EN	VCO_SETTLING_TIME					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-22164. USB3P0SS_PHY2_PLL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6	VCO_SETTLING_TIME_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	VCO_SETTLING_TIME	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.437 USB3P0SS_PHY2_PLL_REG3 Register

1 USB3P0SS_PHY2_PLL_REG3 Register (Offset = 10Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22165. Instance Table

Instance Name	Physical Address
USB0	**0F90 810Ch**

Figure 14-7327. USB3P0SS_PHY2_PLL_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FBDIV_VALUE							
R/W							
0h							

Table 14-22167. USB3P0SS_PHY2_PLL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FBDIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.438 USB3P0SS_PHY2_PLL_REG4 Register

1 USB3P0SS_PHY2_PLL_REG4 Register (Offset = 110h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22168. Instance Table

Instance Name	Physical Address
USB0	**0F90 8110h**

Figure 14-7328. USB3P0SS_PHY2_PLL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED	PLL_LOCK_TIME_15	PD_PFD_VALUE	PD_PFD_EN	PLL_LOCK_EN	PLL_LOCK_VALUE	COARSEDONE_EN	COARSEDONE_VALUE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22170. USB3P0SS_PHY2_PLL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6	PLL_LOCK_TIME_15	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PD_PFD_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PD_PFD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_LOCK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	PLL_LOCK_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22170. USB3P0SS_PHY2_PLL_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	COARSEDONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	COARSEDONE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.439 USB3P0SS_PHY2_PLL_REG5 Register

1 USB3P0SS_PHY2_PLL_REG5 Register (Offset = 114h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22171. Instance Table

Instance Name	Physical Address
USB0	**0F90 8114h**

Figure 14-7329. USB3P0SS_PHY2_PLL_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
STARTLOOP_EN_4_0	STARTLOOP_EN_5	STARTLOOP_5	STARTLOOP_4_0				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 14-22173. USB3P0SS_PHY2_PLL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	STARTLOOP_EN_4_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	STARTLOOP_EN_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	STARTLOOP_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	STARTLOOP_4_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.440 USB3P0SS_PHY2_PLL_REG6 Register

1 USB3P0SS_PHY2_PLL_REG6 Register (Offset = 118h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22174. Instance Table

Instance Name	Physical Address
USB0	**0F90 8118h**

Figure 14-7330. USB3P0SS_PHY2_PLL_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	COARSE_CODE_SEL	LSB_ERROR_0P5	BIG_JUMP_EN	VCO_CNT_WINDOW_VALUE	VCO_CNT_WINDOW_EN	RST_FDBK_DIV_VALUE	RST_FDBK_DIV_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22176. USB3P0SS_PHY2_PLL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	COARSE_CODE_SEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	LSB_ERROR_0P5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIG_JUMP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VCO_CNT_WINDOW_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	VCO_CNT_WINDOW_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22176. USB3P0SS_PHY2_PLL_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RST_FDBK_DIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RST_FDBK_DIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.441 USB3P0SS_PHY2_PLL_REG7 Register

1 USB3P0SS_PHY2_PLL_REG7 Register (Offset = 11Ch) [reset = 0h]

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Table 14-22177. Instance Table

Instance Name	Physical Address
USB0	0F90 811Ch

Figure 14-7331. USB3P0SS_PHY2_PLL_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			REFCLK_SEL				REFCLK_SEL_EN
R/W			R/W				R/W
0h			0h				0h

Table 14-22179. USB3P0SS_PHY2_PLL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
4:1	REFCLK_SEL	R/W	0h	0000 Refclock selection for 9.6 MHz, 0001 Refclock selection for 10 MHz, 0010 Refclock selection for 12 MHz, 0011 Refclock selection for 19.2 MHz, 0100 Refclock selection for 20 MHz, 0101 Refclock selection for 24 MHz, 0110 Refclock selection for 25 MHz, 0111 Refclock selection for 26 MHz, 1000 Refclock selection for 38.4 MHz, 1001 Refclock selection for 40 MHz, 1010 Refclock selection for 48 MHz, 1011 Refclock selection for 50 MHz, 1100 Refclock selection for 52 MHz, 1101 Refclock selection for 9.6 MHz, 1110 Refclock selection for 9.6 MHz, 1111 Refclock selection for 9.6 MHz. Reset Source: usb2_sync_preset_n
0	REFCLK_SEL_EN	R/W	0h	0 PLLREFSEL Value not taken from PLL_REG7[4:1], 1 PLLREFSEL Value taken from PLL_REG7[4:1]. Reset Source: usb2_sync_preset_n

14.9.2.3.2.442 USB3P0SS_PHY2_PLL_REG8 Register

1 USB3P0SS_PHY2_PLL_REG8 Register (Offset = 120h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22180. Instance Table

Instance Name	Physical Address
USB0	**0F90 8120h**

Figure 14-7332. USB3P0SS_PHY2_PLL_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COARSE_CODE							
R/W							
0h							

Table 14-22182. USB3P0SS_PHY2_PLL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COARSE_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.443 USB3P0SS_PHY2_PLL_REG9 Register

1 USB3P0SS_PHY2_PLL_REG9 Register (Offset = 124h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22183. Instance Table

Instance Name	Physical Address
USB0	**0F90 8124h**

Figure 14-7333. USB3P0SS_PHY2_PLL_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COARSE_CODE	V2I_CODE_EN	V2I_CODE					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-22185. USB3P0SS_PHY2_PLL_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	COARSE_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	V2I_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	V2I_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.444 USB3P0SS_PHY2_PLL_REG10 Register

1 USB3P0SS_PHY2_PLL_REG10 Register (Offset = 128h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22186. Instance Table

Instance Name	Physical Address
USB0	**0F90 8128h**

Figure 14-7334. USB3P0SS_PHY2_PLL_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	IPDIV_VALUE					IPDIV_EN	COARSE_CODE_EN
R/W	R/W					R/W	R/W
0h	0h					0h	0h

Table 14-22188. USB3P0SS_PHY2_PLL_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6:2	IPDIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	IPDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	COARSE_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.445 USB3P0SS_PHY2_PLL_REG11 Register

1 USB3P0SS_PHY2_PLL_REG11 Register (Offset = 12Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22189. Instance Table

Instance Name	Physical Address
USB0	**0F90 812Ch**

Figure 14-7335. USB3P0SS_PHY2_PLL_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_STANDBY	PLL_STANDBY_EN	PLL_PD	PLL_PD_EN	PLL_PSO_DEL	PLL_PSO_DEL_EN	PLL_PSO	PLL_PSO_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22191. USB3P0SS_PHY2_PLL_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_STANDBY	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	PLL_STANDBY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PLL_PD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_PD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_PSO_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	PLL_PSO_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22191. USB3P0SS_PHY2_PLL_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PLL_PSO	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_PSO_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.446 USB3P0SS_PHY2_PLL_REG12 Register

1 USB3P0SS_PHY2_PLL_REG12 Register (Offset = 130h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22192. Instance Table

Instance Name	Physical Address
USB0	**0F90 8130h**

Figure 14-7336. USB3P0SS_PHY2_PLL_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED		PLL_LDO_REF_EN	PLL_LDO_REF_EN_EN	PLL_LDO_CORE_EN	PLL_LDO_CORE_EN_EN	PLL_PD_ANA	PLL_PD_ANA_EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-22194. USB3P0SS_PHY2_PLL_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
5	PLL_LDO_REF_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_LDO_REF_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_LDO_CORE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	PLL_LDO_CORE_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	PLL_PD_ANA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22194. USB3P0SS_PHY2_PLL_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL_PD_ANA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.447 USB3P0SS_PHY2_PLL_REG13 Register

1 USB3P0SS_PHY2_PLL_REG13 Register (Offset = 134h) [reset = 0h]

PLL clockon test mode

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Table 14-22195. Instance Table

Instance Name	Physical Address
USB0	**0F90 8134h**

Figure 14-7337. USB3P0SS_PHY2_PLL_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_CLKON	PLL_LDO_REF_CORE						PLL_LDO_REF_CORE_EN
R/W	R/W						R/W
0h	0h						0h

Table 14-22197. USB3P0SS_PHY2_PLL_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_CLKON	R/W	0h	0 pll clock is not always running, 1 pll clock is always running. Reset Source: usb2_sync_preset_n
6:1	PLL_LDO_REF_CORE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_LDO_REF_CORE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.448 USB3P0SS_PHY2_PLL_REG14 Register

1 USB3P0SS_PHY2_PLL_REG14 Register (Offset = 138h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22198. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 8138h**

Figure 14-7338. USB3P0SS_PHY2_PLL_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_LDO_CNT_THRESHOLD			PLL_LDO_CNT_THRESHOLD_EN	PLL_LDO_ISO_CNT_THRESHOLD			PLL_LDO_ISO_CNT_THRESHOLD_EN
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 14-22200. USB3P0SS_PHY2_PLL_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	PLL_LDO_CNT_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_LDO_CNT_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	PLL_LDO_ISO_CNT_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_LDO_ISO_CNT_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.449 USB3P0SS_PHY2_PLL_UNUSED_REG0 Register

1 USB3P0SS_PHY2_PLL_UNUSED_REG0 Register (Offset = 13Ch) [reset = 0h]

unused

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Table 14-22201. Instance Table

Instance Name	Physical Address
USB0	**0F90 813Ch**

Figure 14-7339. USB3P0SS_PHY2_PLL_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22203. USB3P0SS_PHY2_PLL_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.450 USB3P0SS_PHY2_PLL_UNUSED_REG1 Register

1 USB3P0SS_PHY2_PLL_UNUSED_REG1 Register (Offset = 140h) [reset = 0h]

unused

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Table 14-22204. Instance Table

Instance Name	Physical Address
USB0	**0F90 8140h**

Figure 14-7340. USB3P0SS_PHY2_PLL_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22206. USB3P0SS_PHY2_PLL_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.451 USB3P0SS_PHY2_PLL_REG15 Register

1 USB3P0SS_PHY2_PLL_REG15 Register (Offset = 144h) [reset = 0h]

Coarse_code values

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Table 14-22207. Instance Table

Instance Name	Physical Address
USB0	**0F90 8144h**

Figure 14-7341. USB3P0SS_PHY2_PLL_REG15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_LOCK	COARSEDONE	VCO_CNT_WIN	RST_FDBK_DIV	UNUSED	PD_PFD	STARTLOOP	COARSE_CODE_8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22209. USB3P0SS_PHY2_PLL_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_LOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	COARSEDONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	VCO_CNT_WIN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RST_FDBK_DIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
2	PD_PFD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22209. USB3P0SS_PHY2_PLL_REG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	STARTLOOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	COARSE_CODE_8	R	0h	0 MSB of coarse_code for PLL VCO. Reset Source: usb2_sync_preset_n

14.9.2.3.2.452 USB3P0SS_PHY2_PLL_REG16 Register

1 USB3P0SS_PHY2_PLL_REG16 Register (Offset = 148h) [reset = 0h]

Coarse_code values

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Table 14-22210. Instance Table

Instance Name	Physical Address
USB0	**0F90 8148h**

Figure 14-7342. USB3P0SS_PHY2_PLL_REG16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COARSE_CODE							
R							
0h							

Table 14-22212. USB3P0SS_PHY2_PLL_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COARSE_CODE	R	0h	01011010 8 LSBs of coarse code for PLL VCO Reset Source: usb2_sync_preset_n

14.9.2.3.2.453 USB3P0SS_PHY2_PLL_UNUSED_REG2 Register

1 USB3P0SS_PHY2_PLL_UNUSED_REG2 Register (Offset = 14Ch) [reset = 0h]

unused

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Table 14-22213. Instance Table

Instance Name	Physical Address
USB0	**0F90 814Ch**

Figure 14-7343. USB3P0SS_PHY2_PLL_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-22215. USB3P0SS_PHY2_PLL_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.454 USB3P0SS_PHY2_CALIB_REG0 Register

1 USB3P0SS_PHY2_CALIB_REG0 Register (Offset = 180h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22216. Instance Table

Instance Name	Physical Address
USB0	**0F90 8180h**

Figure 14-7344. USB3P0SS_PHY2_CALIB_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CLK	CALIB_CLK_EN	COMP_OUT	INIT_WAIT_OVR				INIT_WAIT_OVR_EN
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 14-22218. USB3P0SS_PHY2_CALIB_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_CLK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CALIB_CLK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	COMP_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	INIT_WAIT_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	INIT_WAIT_OVR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.455 USB3P0SS_PHY2_CALIB_REG1 Register

1 USB3P0SS_PHY2_CALIB_REG1 Register (Offset = 184h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22219. Instance Table

Instance Name	Physical Address
USB0	**0F90 8184h**

Figure 14-7345. USB3P0SS_PHY2_CALIB_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	CALIB_CODE						CALIB_CODE_EN
R/W	R/W						R/W
0h	0h						0h

Table 14-22221. USB3P0SS_PHY2_CALIB_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6:1	CALIB_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.456 USB3P0SS_PHY2_BC_REG0 Register

1 USB3P0SS_PHY2_BC_REG0 Register (Offset = 188h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22222. Instance Table

Instance Name	Physical Address
USB0	**0F90 8188h**

Figure 14-7346. USB3P0SS_PHY2_BC_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">UNUSED</td><td>ADP_EN</td><td>ADP_EN_EN</td><td>ID_PULLUP</td><td>ID_PULLUP_EN</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-22224. USB3P0SS_PHY2_BC_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
3	ADP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	ADP_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ID_PULLUP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ID_PULLUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.457 USB3P0SS_PHY2_BC_REG1 Register

1 USB3P0SS_PHY2_BC_REG1 Register (Offset = 18Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22225. Instance Table

Instance Name	Physical Address
USB0	**0F90 818Ch**

Figure 14-7347. USB3P0SS_PHY2_BC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ADP_SOURCE_I_EN	ADP_SOURCE_I_EN_CTRL	ADP_SINK_I_EN	ADP_SINK_I_EN_CTRL	ADP_SENSE_EN	ADP_SENSE_EN_CTRL	ADP_PROBE_EN	ADP_PROBE_EN_CTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22227. USB3P0SS_PHY2_BC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	ADP_SOURCE_I_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ADP_SOURCE_I_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	ADP_SINK_I_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	ADP_SINK_I_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	ADP_SENSE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	ADP_SENSE_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22227. USB3P0SS_PHY2_BC_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ADP_PROBE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ADP_PROBE_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.458 USB3P0SS_PHY2_BC_REG2 Register

1 USB3P0SS_PHY2_BC_REG2 Register (Offset = 190h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22228. Instance Table

Instance Name	Physical Address
USB0	**0F90 8190h**

Figure 14-7348. USB3P0SS_PHY2_BC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IDM_SINK_EN_VALUE	IDM_SINK_EN_CNTRL	IDP_SINK_EN_VALUE	IDP_SINK_EN_CNTRL	IDP_SRC_EN_VALUE	IDP_SRC_EN_CNTRL	BC_EN_VALUE	BC_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22230. USB3P0SS_PHY2_BC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	IDM_SINK_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	IDM_SINK_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	IDP_SINK_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	IDP_SINK_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	IDP_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	IDP_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22230. USB3P0SS_PHY2_BC_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.459 USB3P0SS_PHY2_BC_REG3 Register

1 USB3P0SS_PHY2_BC_REG3 Register (Offset = 194h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22231. Instance Table

Instance Name	Physical Address
USB0	**0F90 8194h**

Figure 14-7349. USB3P0SS_PHY2_BC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DM_VDAT_REF_COMP_EN_VALUE	DM_VDAT_REF_COMP_EN_CNTRL	DP_VDAT_REF_COMP_EN_VALUE	DP_VDAT_REF_COMP_EN_CNTRL	VDP_SRC_EN_VALUE	VDP_SRC_EN_CNTRL	VDM_SRC_EN_VALUE	VDM_SRC_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22233. USB3P0SS_PHY2_BC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DM_VDAT_REF_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DM_VDAT_REF_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DP_VDAT_REF_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DP_VDAT_REF_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VDP_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22233. USB3P0SS_PHY2_BC_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	VDP_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	VDM_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	VDM_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.460 USB3P0SS_PHY2_BC_REG4 Register

1 USB3P0SS_PHY2_BC_REG4 Register (Offset = 198h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22234. Instance Table

Instance Name	Physical Address
USB0	**0F90 8198h**

Figure 14-7350. USB3P0SS_PHY2_BC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_A_REF_EN_VALUE	RID_A_REF_EN_CNTRL	RID_FLOAT_REF_EN_VALUE	RID_FLOAT_REF_EN_CNTRL	RID_NONFLOAT_COMP_EN_VALUE	RID_NONFLOAT_COMP_EN_CNTRL	RID_FLOAT_COMP_EN_VALUE	RID_FLOAT_COMP_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22236. USB3P0SS_PHY2_BC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_A_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_A_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_FLOAT_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_FLOAT_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_NONFLOAT_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22236. USB3P0SS_PHY2_BC_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RID_NONFLOAT_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RID_FLOAT_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RID_FLOAT_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.461 USB3P0SS_PHY2_BC_REG5 Register

1 USB3P0SS_PHY2_BC_REG5 Register (Offset = 19Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22237. Instance Table

Instance Name	Physical Address
USB0	**0F90 819Ch**

Figure 14-7351. USB3P0SS_PHY2_BC_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_B_C_COMP_EN_VALUE	RID_B_C_COMP_EN_CNTRL	RID_A_COMP_EN_VALUE	RID_A_COMP_EN_CNTRL	RID_C_REF_EN_VALUE	RID_C_REF_EN_CNTRL	RID_B_REF_EN_VALUE	RID_B_REF_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22239. USB3P0SS_PHY2_BC_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_B_C_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_B_C_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_A_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_A_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_C_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RID_C_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22239. USB3P0SS_PHY2_BC_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RID_B_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RID_B_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.462 USB3P0SS_PHY2_BC_REG6 Register

1 USB3P0SS_PHY2_BC_REG6 Register (Offset = 1A0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22240. Instance Table

Instance Name	Physical Address
USB0	0F90 81A0h

Figure 14-7352. USB3P0SS_PHY2_BC_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BC_DELAY_VALUE					BC_DELAY_EN	DM_VLGC_COMP_EN_VALUE	DM_VLGC_COMP_EN_CNTRL
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-22242. USB3P0SS_PHY2_BC_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	BC_DELAY_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	BC_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DM_VLGC_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DM_VLGC_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.463 USB3P0SS_PHY2_BC_REG7 Register

1 USB3P0SS_PHY2_BC_REG7 Register (Offset = 1A4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22243. Instance Table

Instance Name	Physical Address
USB0	**0F90 81A4h**

Figure 14-7353. USB3P0SS_PHY2_BC_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RID_NONFLOAT_SRC_EN_VALUE	RID_NONFLOAT_SRC_EN_CNTRL	RID_FLOAT_SRC_EN_VALUE	RID_FLOAT_SRC_EN_CNTRL	RESET_CNTRL	DM_CURRENT_SRC_EN_VALUE	DM_CURRENT_SRC_EN_CNTRL	UNUSED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22245. USB3P0SS_PHY2_BC_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_NONFLOAT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_NONFLOAT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_FLOAT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_FLOAT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RESET_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22245. USB3P0SS_PHY2_BC_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DM_CURRENT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DM_CURRENT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.464 USB3P0SS_PHY2_TED_REG0 Register

1 USB3P0SS_PHY2_TED_REG0 Register (Offset = 1A8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22246. Instance Table

Instance Name	Physical Address
USB0	**0F90 81A8h**

Figure 14-7354. USB3P0SS_PHY2_TED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CODE_UP_EN	DELAY_VALUE		DELAY_EN	CALIB_DONE	CALIIB_DONE_EN	COMP_OUT_DOWN_INV	COMP_OUT_UP_INV
R/W	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h

Table 14-22248. USB3P0SS_PHY2_TED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_CODE_UP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:5	DELAY_VALUE	R/W	0h	Delay is 8us Reset Source: usb2_sync_preset_n
4	DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CALIB_DONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIIB_DONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	COMP_OUT_DOWN_INV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22248. USB3P0SS_PHY2_TED_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COMP_OUT_UP_INV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.465 USB3P0SS_PHY2_TED_REG1 Register

1 USB3P0SS_PHY2_TED_REG1 Register (Offset = 1ACh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22249. Instance Table

Instance Name	Physical Address
USB0	**0F90 81ACh**

Figure 14-7355. USB3P0SS_PHY2_TED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CODE_DOWN				CALIB_CODE_UP			
R/W				R/W			
0h				0h			

Table 14-22251. USB3P0SS_PHY2_TED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_DOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	CALIB_CODE_UP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.466 USB3P0SS_PHY2_TED_REG2 Register

1 USB3P0SS_PHY2_TED_REG2 Register (Offset = 1B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22252. Instance Table

Instance Name	Physical Address
USB0	**0F90 81B0h**

Figure 14-7356. USB3P0SS_PHY2_TED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			CALIB_MODE_DN	CALIB_MODE_DN_EN	CALIB_MODE_UP	CALIB_MODE_UP_EN	CALIB_CODE_DN_EN
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-22254. USB3P0SS_PHY2_TED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
4	CALIB_MODE_DN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CALIB_MODE_DN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_MODE_UP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CALIB_MODE_UP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_CODE_DN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.467 USB3P0SS_PHY2_CALIB_REG2 Register

1 USB3P0SS_PHY2_CALIB_REG2 Register (Offset = 1B4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22255. Instance Table

Instance Name	Physical Address
USB0	**0F90 81B4h**

Figure 14-7357. USB3P0SS_PHY2_CALIB_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED				CALIB_CMP	CALIB_PD	CALIB_CLOCK	CALIB_DONE
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-22257. USB3P0SS_PHY2_CALIB_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
3	CALIB_CMP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CALIB_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.468 USB3P0SS_PHY2_CALIB_REG3 Register

1 USB3P0SS_PHY2_CALIB_REG3 Register (Offset = 1B8h) [reset = 0h]

Resistor calibration code

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Table 14-22258. Instance Table

Instance Name	Physical Address
USB0	**0F90 81B8h**

Figure 14-7358. USB3P0SS_PHY2_CALIB_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			BG_UNIT_RES_CALIB				
R			R				
0h			0h				

Table 14-22260. USB3P0SS_PHY2_CALIB_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
4:0	BG_UNIT_RES_CALIB	R	0h	Resistor calibration code from the calibration block Reset Source: usb2_sync_preset_n

14.9.2.3.2.469 USB3P0SS_PHY2_BC_REG8 Register

1 USB3P0SS_PHY2_BC_REG8 Register (Offset = 1BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22261. Instance Table

Instance Name	Physical Address
USB0	**0F90 81BCh**

Figure 14-7359. USB3P0SS_PHY2_BC_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DCD_COMP	ADP_SENSE	ADP_PROBE	BVALID	VBUSVALID	IDDIG	UNUSED	
R	R	R	R	R	R	R	
0h	0h	0h	0h	0h	0h	0h	

Table 14-22263. USB3P0SS_PHY2_BC_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DCD_COMP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ADP_SENSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	ADP_PROBE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VBUSVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	IDDIG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22263. USB3P0SS_PHY2_BC_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.470 USB3P0SS_PHY2_BC_REG9 Register

1 USB3P0SS_PHY2_BC_REG9 Register (Offset = 1C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22264. Instance Table

Instance Name	Physical Address
USB0	**0F90 81C0h**

Figure 14-7360. USB3P0SS_PHY2_BC_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_DM_VDAT_REF_COMP_EN	O_DP_VDAT_REF_COMP_EN	O_VDM_SRC_EN	O_VDP_SRC_EN	O_IDM_SINK_EN	O_IDP_SINK_EN	O_IDP_SRC_EN	O_BC_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22266. USB3P0SS_PHY2_BC_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_DM_VDAT_REF_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_DP_VDAT_REF_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_VDM_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_VDP_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_IDM_SINK_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22266. USB3P0SS_PHY2_BC_REG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	O_IDP_SINK_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_IDP_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_BC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.471 USB3P0SS_PHY2_BC_REG10 Register

1 USB3P0SS_PHY2_BC_REG10 Register (Offset = 1C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22267. Instance Table

Instance Name	Physical Address
USB0	**0F90 81C4h**

Figure 14-7361. USB3P0SS_PHY2_BC_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_RID_B_C_COMP_EN	O_RID_A_COMP_EN	O_RID_C_REF_EN	O_RID_B_REF_EN	O_RID_A_REF_EN	O_RID_FLOAT_REF_EN	O_RID_NONFLOAT_SRC_EN	O_RID_FLOAT_SRC_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22269. USB3P0SS_PHY2_BC_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_RID_B_C_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_RID_A_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_RID_C_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_RID_B_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_RID_A_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_RID_FLOAT_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22269. USB3P0SS_PHY2_BC_REG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	O_RID_NONFLOAT_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_RID_FLOAT_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.472 USB3P0SS_PHY2_BC_REG11 Register

1 USB3P0SS_PHY2_BC_REG11 Register (Offset = 1C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22270. Instance Table

Instance Name	Physical Address
USB0	**0F90 81C8h**

Figure 14-7362. USB3P0SS_PHY2_BC_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_IDM_SRC_EN	I_AFE_RXDP_ANA	I_AFE_RXDM_ANA	I_RID_B_C_COMP_STS	I_RID_A_COMP_STS	I_DM_VDAT_REF_COMP_STS	I_DP_VDAT_REF_COMP_STS	O_DM_VLGC_COMP_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22272. USB3P0SS_PHY2_BC_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_IDM_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	I_AFE_RXDP_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	I_AFE_RXDM_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	I_RID_B_C_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	I_RID_A_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22272. USB3P0SS_PHY2_BC_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	I_DM_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	I_DP_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_DM_VLGC_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.473 USB3P0SS_PHY2_BC_REG12 Register

1 USB3P0SS_PHY2_BC_REG12 Register (Offset = 1CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22273. Instance Table

Instance Name	Physical Address
USB0	**0F90 81CCh**

Figure 14-7363. USB3P0SS_PHY2_BC_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_GND_COMP_STS	RID_FLOAT_COMP_STS	RID_C_COMP_STS	RID_B_COMP_STS	RID_A_COMP_STS	DM_VLGC_COMP_STS	DM_VDAT_REF_COMP_STS	DP_VDAT_REF_COMP_STS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22275. USB3P0SS_PHY2_BC_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_GND_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_FLOAT_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_C_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_B_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_A_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DM_VLGC_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22275. USB3P0SS_PHY2_BC_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DM_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DP_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.474 USB3P0SS_PHY2_TED_REG3 Register

1 USB3P0SS_PHY2_TED_REG3 Register (Offset = 1D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22276. Instance Table

Instance Name	Physical Address
USB0	**0F90 81D0h**

Figure 14-7364. USB3P0SS_PHY2_TED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CODE_DOWN				COMPARATOR_DOWN	CALIB_DONE_DOWN	UNUSED	
R				R	R	R	
0h				0h	0h	0h	

Table 14-22278. USB3P0SS_PHY2_TED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	COMPARATOR_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_DONE_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.475 USB3P0SS_PHY2_TED_REG4 Register

1 USB3P0SS_PHY2_TED_REG4 Register (Offset = 1D4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22279. Instance Table

Instance Name	Physical Address
USB0	**0F90 81D4h**

Figure 14-7365. USB3P0SS_PHY2_TED_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALIB_CODE_UP				COMPARATOR_UP	CALIB_DONE_UP	UNUSED	
R				R	R	R	
0h				0h	0h	0h	

Table 14-22281. USB3P0SS_PHY2_TED_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	COMPARATOR_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_DONE_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.476 USB3P0SS_PHY2_DIG_UNUSED_REG0 Register

1 USB3P0SS_PHY2_DIG_UNUSED_REG0 Register (Offset = 1D8h) [reset = 0h]

UNUSED

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Table 14-22282. Instance Table

Instance Name	Physical Address
USB0	**0F90 81D8h**

Figure 14-7366. USB3P0SS_PHY2_DIG_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
GLITCH_FILTER_EN	UNUSED						
R/W	R/W						
0h	0h						

Table 14-22284. USB3P0SS_PHY2_DIG_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	GLITCH_FILTER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.477 USB3P0SS_PHY2_DIG_UNUSED_REG1 Register

1 USB3P0SS_PHY2_DIG_UNUSED_REG1 Register (Offset = 1DCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22285. Instance Table

Instance Name	Physical Address
USB0	**0F90 81DCh**

Figure 14-7367. USB3P0SS_PHY2_DIG_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED					THRESHOLD_OVR_VALUE_MSB		THRESHOLD_OVR_EN
R/W					R/W		R/W
0h					0h		0h

Table 14-22287. USB3P0SS_PHY2_DIG_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
2:1	THRESHOLD_OVR_VALUE_MSB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	THRESHOLD_OVR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.478 USB3P0SS_PHY2_DIG_UNUSED_REG2 Register

1 USB3P0SS_PHY2_DIG_UNUSED_REG2 Register (Offset = 1E0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22288. Instance Table

Instance Name	Physical Address
USB0	**0F90 81E0h**

Figure 14-7368. USB3P0SS_PHY2_DIG_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
THRESHOLD_OVR_VALUE_LSB							
R/W							
0h							

Table 14-22290. USB3P0SS_PHY2_DIG_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	THRESHOLD_OVR_VALUE_LSB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.479 USB3P0SS_PHY2_DIG_UNUSED_REG3 Register

1 USB3P0SS_PHY2_DIG_UNUSED_REG3 Register (Offset = 1E4h) [reset = 0h]

UNUSED

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Table 14-22291. Instance Table

Instance Name	Physical Address
USB0	**0F90 81E4h**

Figure 14-7369. USB3P0SS_PHY2_DIG_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22293. USB3P0SS_PHY2_DIG_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.480 USB3P0SS_PHY2_INTERRUPT_REG1 Register

1 USB3P0SS_PHY2_INTERRUPT_REG1 Register (Offset = 1E8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22294. Instance Table

Instance Name	Physical Address
USB0	**0F90 81E8h**

Figure 14-7370. USB3P0SS_PHY2_INTERRUPT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IRSR	ISR	UNUSED					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-22296. USB3P0SS_PHY2_INTERRUPT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	IRSR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ISR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.481 USB3P0SS_PHY2_INTERRUPT_REG2 Register

1 USB3P0SS_PHY2_INTERRUPT_REG2 Register (Offset = 1ECh) [reset = 1h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22297. Instance Table

Instance Name	Physical Address
USB0	**0F90 81ECh**

Figure 14-7371. USB3P0SS_PHY2_INTERRUPT_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							IMR
R/W							R/W
0h							1h

Table 14-22299. USB3P0SS_PHY2_INTERRUPT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:1	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
0	IMR	R/W	1h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.482 USB3P0SS_PHY2_RX_REG0 Register

1 USB3P0SS_PHY2_RX_REG0 Register (Offset = 200h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22300. Instance Table

Instance Name	Physical Address
USB0	**0F90 8200h**

Figure 14-7372. USB3P0SS_PHY2_RX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSLS_NO_EOP_TIMEOUT			FSLS_TIMEOUT_EN	HS_SYNC_DET_BITS	FS_EOP_SE0_THRESHOLD		FS_EOP_SE0_EN
R/W			R/W	R/W	R/W		R/W
0h			0h	0h	0h		0h

Table 14-22302. USB3P0SS_PHY2_RX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	FSLS_NO_EOP_TIMEOUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	FSLS_TIMEOUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_SYNC_DET_BITS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	FS_EOP_SE0_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_EOP_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.483 USB3P0SS_PHY2_RX_REG1 Register

1 USB3P0SS_PHY2_RX_REG1 Register (Offset = 204h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22303. Instance Table

Instance Name	Physical Address
USB0	**0F90 8204h**

Figure 14-7373. USB3P0SS_PHY2_RX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LS_EOP_SE0_THRESHOLD						LS_EOP_SE0_EN	FS_NO_EOP_TIMEOUT_EN
R/W						R/W	R/W
0h						0h	0h

Table 14-22305. USB3P0SS_PHY2_RX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	LS_EOP_SE0_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	LS_EOP_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_NO_EOP_TIMEOUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.484 USB3P0SS_PHY2_TX_REG0 Register

1 USB3P0SS_PHY2_TX_REG0 Register (Offset = 208h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22306. Instance Table

Instance Name	Physical Address
USB0	**0F90 8208h**

Figure 14-7374. USB3P0SS_PHY2_TX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED				FS_PREAMBLE_EN	SOF_EXTENSION		SOF_EXTENSION_EN
R/W				R/W	R/W		R/W
0h				0h	0h		0h

Table 14-22308. USB3P0SS_PHY2_TX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
3	FS_PREAMBLE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	SOF_EXTENSION	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SOF_EXTENSION_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.485 USB3P0SS_PHY2_TX_REG1 Register

1 USB3P0SS_PHY2_TX_REG1 Register (Offset = 20Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22309. Instance Table

Instance Name	Physical Address
USB0	**0F90 820Ch**

Figure 14-7375. USB3P0SS_PHY2_TX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PREAMBLE_VALUE							
R/W							
0h							

Table 14-22311. USB3P0SS_PHY2_TX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.486 USB3P0SS_PHY2_CDR_REG0 Register

1 USB3P0SS_PHY2_CDR_REG0 Register (Offset = 210h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22312. Instance Table

Instance Name	Physical Address
USB0	**0F90 8210h**

Figure 14-7376. USB3P0SS_PHY2_CDR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED		PLL_CLKDIV		PLL_CLKDIV_EN	SQUELCH_DELAY		SQUELCH_DELAY_EN
R/W		R/W		R/W	R/W		R/W
0h		0h		0h	0h		0h

Table 14-22314. USB3P0SS_PHY2_CDR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
5:4	PLL_CLKDIV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_CLKDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	SQUELCH_DELAY	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SQUELCH_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.487 USB3P0SS_PHY2_CDR_REG1 Register

1 USB3P0SS_PHY2_CDR_REG1 Register (Offset = 214h) [reset = 0h]

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Table 14-22315. Instance Table

Instance Name	Physical Address
USB0	**0F90 8214h**

Figure 14-7377. USB3P0SS_PHY2_CDR_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	CALIB_COMP_OUT	CALIB_SPC_THRESHOLD			CALIB_SPC_THRESHOLD_EN	CALIB_ITERATION	DYNAMIC_CALIB_EN
R/W	R/W	R/W			R/W	R/W	R/W
0h	0h	0h			0h	0h	0h

Table 14-22317. USB3P0SS_PHY2_CDR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	CALIB_COMP_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:3	CALIB_SPC_THRESHOLD	R/W	0h	000 The time interval between succesive calibrations is 0us, 001 The time interval between succesive calibrations is 1us, 010 The time interval between succesive calibrations is 2us, 011 The time interval between succesive calibrations is 3us, 100 The time interval between succesive calibrations is 4us, 101 The time interval between succesive calibrations is 5us, 110 The time interval between succesive calibrations is 6us, 111 The time interval between succesive calibrations is 7us. Reset Source: usb2_sync_preset_n
2	CALIB_SPC_THRESHOLD_EN	R/W	0h	0 The time interval between succesive calibrations is taken as 5us by default, 1 The time interval between succesive calibrations is taken from CDR_REG1[5:3] Reset Source: usb2_sync_preset_n

Table 14-22317. USB3P0SS_PHY2_CDR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CALIB_ITERATION	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DYNAMIC_CALIB_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.488 USB3P0SS_PHY2_CDR_REG2 Register

1 USB3P0SS_PHY2_CDR_REG2 Register (Offset = 218h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22318. Instance Table

Instance Name	Physical Address
USB0	**0F90 8218h**

Figure 14-7378. USB3P0SS_PHY2_CDR_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	HSRX_EN_DEL	HSRX_EN_DEL_EN	HSRX_EN	HSRX_EN_EN	CALIB_CLOCK	CALIB_CLOCK_EN	CALIB_OUT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22320. USB3P0SS_PHY2_CDR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	HSRX_EN_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSRX_EN_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSRX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSRX_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_CLOCK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22320. USB3P0SS_PHY2_CDR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CALIB_CLOCK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_OUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.489 USB3P0SS_PHY2_CDR_REG3 Register

1 USB3P0SS_PHY2_CDR_REG3 Register (Offset = 21Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22321. Instance Table

Instance Name	Physical Address
USB0	**0F90 821Ch**

Figure 14-7379. USB3P0SS_PHY2_CDR_REG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CALIB_ACTIVE</td><td>CALIB_DONE</td><td colspan="6">CALIB_CODE</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="6">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-22323. USB3P0SS_PHY2_CDR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_ACTIVE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CALIB_DONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	CALIB_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.490 USB3P0SS_PHY2_CDR_REG4 Register

1 USB3P0SS_PHY2_CDR_REG4 Register (Offset = 220h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22324. Instance Table

Instance Name	Physical Address
USB0	**0F90 8220h**

Figure 14-7380. USB3P0SS_PHY2_CDR_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLK_GATE_VALUE	CLK_GATE_EN	CLK_GATE_SQ_MASK	LATENCY_THRESHOLD		LATENCY_THRESHOLD_EN	DECISION_ERROR_EN	FILTER_EN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	0h

Table 14-22326. USB3P0SS_PHY2_CDR_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLK_GATE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CLK_GATE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	CLK_GATE_SQ_MASK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	LATENCY_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	LATENCY_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DECISION_ERROR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22326. USB3P0SS_PHY2_CDR_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FILTER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.491 USB3P0SS_PHY2_CDR_REG5 Register

1 USB3P0SS_PHY2_CDR_REG5 Register (Offset = 224h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22327. Instance Table

Instance Name	Physical Address
USB0	**0F90 8224h**

Figure 14-7381. USB3P0SS_PHY2_CDR_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED					SAMPLE_5X_EN	SMALL_PULSE	SMALL_PULSE_EN
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-22329. USB3P0SS_PHY2_CDR_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
2	SAMPLE_5X_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	SMALL_PULSE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SMALL_PULSE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.492 USB3P0SS_PHY2_CDR_REG6 Register

1 USB3P0SS_PHY2_CDR_REG6 Register (Offset = 228h) [reset = 0h]

unused

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Table 14-22330. Instance Table

Instance Name	Physical Address
USB0	0F90 8228h

Figure 14-7382. USB3P0SS_PHY2_CDR_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22332. USB3P0SS_PHY2_CDR_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.493 USB3P0SS_PHY2_CDR_REG7 Register

1 USB3P0SS_PHY2_CDR_REG7 Register (Offset = 22Ch) [reset = 0h]

unused

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Table 14-22333. Instance Table

Instance Name	Physical Address
USB0	**0F90 822Ch**

Figure 14-7383. USB3P0SS_PHY2_CDR_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22335. USB3P0SS_PHY2_CDR_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.494 USB3P0SS_PHY2_CDR_REG8 Register

1 USB3P0SS_PHY2_CDR_REG8 Register (Offset = 230h) [reset = 0h]

unused

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Table 14-22336. Instance Table

Instance Name	Physical Address
USB0	**0F90 8230h**

Figure 14-7384. USB3P0SS_PHY2_CDR_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22338. USB3P0SS_PHY2_CDR_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.495 USB3P0SS_PHY2_RX_REG2 Register

1 USB3P0SS_PHY2_RX_REG2 Register (Offset = 234h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22339. Instance Table

Instance Name	Physical Address
USB0	**0F90 8234h**

Figure 14-7385. USB3P0SS_PHY2_RX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EB_ERROR	CDR_ERROR	SYNC_DETECTED	EOP_DETECTED	HS_EOP_CONDITION	NORMAL_EOP	ALIGNMENT_ERROR	NO_EOP
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22341. USB3P0SS_PHY2_RX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EB_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CDR_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SYNC_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_EOP_CONDITION	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	NORMAL_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22341. USB3P0SS_PHY2_RX_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ALIGNMENT_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	NO_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.496 USB3P0SS_PHY2_RX_REG3 Register

1 USB3P0SS_PHY2_RX_REG3 Register (Offset = 238h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22342. Instance Table

Instance Name	Physical Address
USB0	**0F90 8238h**

Figure 14-7386. USB3P0SS_PHY2_RX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS_EOP_DETECTED	SE0_VALIDATED	LSFS_EOP_DETECTED	BIT_UNSTUFF_ERROR	RX_STATE_BITUNSTUFF			START_FLAG
R	R	R	R	R			R
0h	0h	0h	0h	0h			0h

Table 14-22344. USB3P0SS_PHY2_RX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SE0_VALIDATED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	LSFS_EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIT_UNSTUFF_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	RX_STATE_BITUNSTUFF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22344. USB3P0SS_PHY2_RX_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	START_FLAG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.497 USB3P0SS_PHY2_RX_REG4 Register

1 USB3P0SS_PHY2_RX_REG4 Register (Offset = 23Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22345. Instance Table

Instance Name	Physical Address
USB0	**0F90 823Ch**

Figure 14-7387. USB3P0SS_PHY2_RX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RXACTIVE_REG	DEASSERT_RXACTIVE_REG	UNUSED					
R	R	R					
0h	0h	0h					

Table 14-22347. USB3P0SS_PHY2_RX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RXACTIVE_REG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DEASSERT_RXACTIVE_REG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.498 USB3P0SS_PHY2_RX_REG5 Register

1 USB3P0SS_PHY2_RX_REG5 Register (Offset = 240h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22348. Instance Table

Instance Name	Physical Address
USB0	**0F90 8240h**

Figure 14-7388. USB3P0SS_PHY2_RX_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIE_CNT_UPPER							
R							
0h							

Table 14-22350. USB3P0SS_PHY2_RX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	SIE_CNT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.499 USB3P0SS_PHY2_RX_REG6 Register

1 USB3P0SS_PHY2_RX_REG6 Register (Offset = 244h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22351. Instance Table

Instance Name	Physical Address
USB0	0F90 8244h

Figure 14-7389. USB3P0SS_PHY2_RX_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PHY_CNT_UPPER							
R							
0h							

Table 14-22353. USB3P0SS_PHY2_RX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PHY_CNT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.500 USB3P0SS_PHY2_RX_REG7 Register

1 USB3P0SS_PHY2_RX_REG7 Register (Offset = 248h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22354. Instance Table

Instance Name	Physical Address
USB0	**0F90 8248h**

Figure 14-7390. USB3P0SS_PHY2_RX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PHY_CNT_LOWER				SIE_CNT_LOWER			
R				R			
0h				0h			

Table 14-22356. USB3P0SS_PHY2_RX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	PHY_CNT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	SIE_CNT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.501 USB3P0SS_PHY2_TX_REG2 Register

1 USB3P0SS_PHY2_TX_REG2 Register (Offset = 24Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22357. Instance Table

Instance Name	Physical Address
USB0	**0F90 824Ch**

Figure 14-7391. USB3P0SS_PHY2_TX_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">TX_HS_STATE</td><td>EOP_TRANSMITTED</td><td>HS_BITSTUFF_EN</td><td>RESUME_EOP</td><td>REMOTE_WAKEUP</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-22359. USB3P0SS_PHY2_TX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	TX_HS_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	EOP_TRANSMITTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HS_BITSTUFF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RESUME_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	REMOTE_WAKEUP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.502 USB3P0SS_PHY2_TX_REG3 Register

1 USB3P0SS_PHY2_TX_REG3 Register (Offset = 250h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22360. Instance Table

Instance Name	Physical Address
USB0	**0F90 8250h**

Figure 14-7392. USB3P0SS_PHY2_TX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_LSFS_STATE				PD_STATE			PREAMBLE_SENT
R				R			R
0h				0h			0h

Table 14-22362. USB3P0SS_PHY2_TX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	TX_LSFS_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	PD_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PREAMBLE_SENT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.503 USB3P0SS_PHY2_TX_REG4 Register

1 USB3P0SS_PHY2_TX_REG4 Register (Offset = 254h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22363. Instance Table

Instance Name	Physical Address
USB0	**0F90 8254h**

Figure 14-7393. USB3P0SS_PHY2_TX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED						LSFS_BITSTUFF_EN	LS_KEEP_ALIVE
R						R	R
0h						0h	0h

Table 14-22365. USB3P0SS_PHY2_TX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
1	LSFS_BITSTUFF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	LS_KEEP_ALIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.504 USB3P0SS_PHY2_CDR_REG9 Register

1 USB3P0SS_PHY2_CDR_REG9 Register (Offset = 258h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22366. Instance Table

Instance Name	Physical Address
USB0	**0F90 8258h**

Figure 14-7394. USB3P0SS_PHY2_CDR_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED					I_ANA_COMP_OUT	SAMPLER_CALIB_DONE	ANA_CALIB_ACTIVE
R					R	R	R
0h					0h	0h	0h

Table 14-22368. USB3P0SS_PHY2_CDR_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
2	I_ANA_COMP_OUT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	SAMPLER_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ANA_CALIB_ACTIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.505 USB3P0SS_PHY2_CDR_REG10 Register

1 USB3P0SS_PHY2_CDR_REG10 Register (Offset = 25Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22369. Instance Table

Instance Name	Physical Address
USB0	0F90 825Ch

Figure 14-7395. USB3P0SS_PHY2_CDR_REG10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">UNUSED</td><td colspan="6">CALIB_CODE</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-22371. USB3P0SS_PHY2_CDR_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
5:0	CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.506 USB3P0SS_PHY2_CDR_REG11 Register

1 USB3P0SS_PHY2_CDR_REG11 Register (Offset = 260h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22372. Instance Table

Instance Name	Physical Address
USB0	**0F90 8260h**

Figure 14-7396. USB3P0SS_PHY2_CDR_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SMALL_PULSE				O_HSRX_REC_DICISION_ERROR	O_ANA_CLK_GATE	RECEIVE_START	I_ANA_TED_SQUELCH
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-22374. USB3P0SS_PHY2_CDR_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SMALL_PULSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_HSRX_REC_DICISION_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_ANA_CLK_GATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RECEIVE_START	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	I_ANA_TED_SQUELCH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.507 USB3P0SS_PHY2_CDR_RE12 Register

1 USB3P0SS_PHY2_CDR_RE12 Register (Offset = 264h) [reset = 0h]

unused

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Table 14-22375. Instance Table

Instance Name	Physical Address
USB0	**0F90 8264h**

Figure 14-7397. USB3P0SS_PHY2_CDR_RE12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-22377. USB3P0SS_PHY2_CDR_RE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.508 USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG0 Register

1 USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG0 Register (Offset = 268h) [reset = 0h]

UNUSED

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Table 14-22378. Instance Table

Instance Name	Physical Address
USB0	**0F90 8268h**

Figure 14-7398. USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22380. USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.509 USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG1 Register

1 USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG1 Register (Offset = 26Ch) [reset = 0h]

UNUSED

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Table 14-22381. Instance Table

Instance Name	Physical Address
USB0	0F90 826Ch

Figure 14-7399. USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22383. USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.510 USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG2 Register

1 USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG2 Register (Offset = 270h) [reset = 0h]

UNUSED

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Table 14-22384. Instance Table

Instance Name	Physical Address
USB0	**0F90 8270h**

Figure 14-7400. USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22386. USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.511 USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG3 Register

1 USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG3 Register (Offset = 274h) [reset = 0h]

UNUSED

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Table 14-22387. Instance Table

Instance Name	Physical Address
USB0	**0F90 8274h**

Figure 14-7401. USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22389. USB3P0SS_PHY2_DIG_TXRX_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.9.2.3.2.512 USB3P0SS_PHY2_UTMI_REG0 Register

1 USB3P0SS_PHY2_UTMI_REG0 Register (Offset = 280h) [reset = 0h]

register UTMI_REG0

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Table 14-22390. Instance Table

Instance Name	Physical Address
USB0	**0F90 8280h**

Figure 14-7402. USB3P0SS_PHY2_UTMI_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LOOPBACK_SEL		LOOPBACK_EN	BIST_MODE_SEL				BIST_EN
R/W		R/W	R/W				R/W
0h		0h	0h				0h

Table 14-22392. USB3P0SS_PHY2_UTMI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	LOOPBACK_SEL	R/W	0h	00 Loopback mode selection = 00 : Reserved, 01 Loopback mode selection = 01 : LS, 10 Loopback mode selection = 10 : FS, 11 Loopback mode selection = 11 : HS Reset Source: usb2_sync_preset_n
5	LOOPBACK_EN	R/W	0h	0 Loopback mode selection is taken from primary input port-loopback[1:0], 1 Loopback mode selection is taken from UTMI_REG0[7:6]. Reset Source: usb2_sync_preset_n
4:1	BIST_MODE_SEL	R/W	0h	0 BIST for 8 bit, 1 BIST for 16 bit, 0 Error injection disabled, 1 Error injection enabled, 0 BIST for device mode, 1 BIST for host mode, 0 BIST for HS mode, 1 BIST for FS mode. Reset Source: usb2_sync_preset_n
0	BIST_EN	R/W	0h	0 BIST control signals taken from primary input BIST related ports, 1 BIST signals taken from UTMI REG0[4:1], UTMI_REG1[7:6], UTMI_REG5[7:6] Reset Source: usb2_sync_preset_n

14.9.2.3.2.513 USB3P0SS_PHY2_UTMI_REG1 Register

1 USB3P0SS_PHY2_UTMI_REG1 Register (Offset = 284h) [reset = 0h]

bist error injection, soft resets

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Table 14-22393. Instance Table

Instance Name	Physical Address
USB0	**0F90 8284h**

Figure 14-7403. USB3P0SS_PHY2_UTMI_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_ERR		BIST_SOFT_RST	TX_LSFS_SOFT_RST	TX_HS_SOFT_RST	CLKDIV_SOFT_RST	CALIB_SOFT_RST	PHY_SOFT_RST
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-22395. USB3P0SS_PHY2_UTMI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_ERR	R/W	0h	00 Introduce error on first packet, bist error injection = 00, 01 Introduce error on second packet,bist error injection = 01, 10 Introduce error on third packet, bist error injection = 10, 11 Introduce error on last packet, bist error injection = 11. Reset Source: usb2_sync_preset_n
5	BIST_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	TX_LSFS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TX_HS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CLKDIV_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22395. USB3P0SS_PHY2_UTMI_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CALIB_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PHY_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.514 USB3P0SS_PHY2_UTMI_REG2 Register

1 USB3P0SS_PHY2_UTMI_REG2 Register (Offset = 288h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22396. Instance Table

Instance Name	Physical Address
USB0	**0F90 8288h**

Figure 14-7404. USB3P0SS_PHY2_UTMI_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_CNTRL_SOFT_RST	SHIFT_REG_SOFT_RST	BITUNSTUFF_SOFT_RST	NRZI_DEC_SOFT_RST	EOP_DET_SOFT_RST	SYNC_DET_SOFT_RST	LSFS_DLL_SOFT_RST	RX_HS_SOFT_RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22398. USB3P0SS_PHY2_UTMI_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RX_CNTRL_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SHIFT_REG_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BITUNSTUFF_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	NRZI_DEC_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	EOP_DET_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	SYNC_DET_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22398. USB3P0SS_PHY2_UTMI_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LSFS_DLL_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RX_HS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.515 USB3P0SS_PHY2_UTMI_REG3 Register

1 USB3P0SS_PHY2_UTMI_REG3 Register (Offset = 28Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22399. Instance Table

Instance Name	Physical Address
USB0	**0F90 828Ch**

Figure 14-7405. USB3P0SS_PHY2_UTMI_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HS_RX_ERR	LS_LINESTATE_FIL_EN	FS_LINESTATE_FIL_CNT					FS_LINESTATE_FIL_EN
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-22401. USB3P0SS_PHY2_UTMI_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_RX_ERR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	LS_LINESTATE_FIL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:1	FS_LINESTATE_FIL_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_LINESTATE_FIL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.516 USB3P0SS_PHY2_UTMI_REG4 Register

1 USB3P0SS_PHY2_UTMI_REG4 Register (Offset = 290h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22402. Instance Table

Instance Name	Physical Address
USB0	0F90 8290h

Figure 14-7406. USB3P0SS_PHY2_UTMI_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LS_LINESTATE_FIL_CNT							
R/W							
0h							

Table 14-22404. USB3P0SS_PHY2_UTMI_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	LS_LINESTATE_FIL_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.517 USB3P0SS_PHY2_UTMI_REG5 Register

1 USB3P0SS_PHY2_UTMI_REG5 Register (Offset = 294h) [reset = 0h]

BIST, hsrx data

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Table 14-22405. Instance Table

Instance Name	Physical Address
USB0	**0F90 8294h**

Figure 14-7407. USB3P0SS_PHY2_UTMI_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_MODE_EN	BIST_ON	HSTX_BOOST_DEAMP_OFF	HSTX_BOOST	HS_SAMP	HS_SAMP_EN	HSRX	HSRX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22407. USB3P0SS_PHY2_UTMI_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	BIST_MODE_EN	R/W	0h	0 BIST mode en is taken from primary input port- bist_mode_en, 1 bist_mode_en is turned on. Reset Source: usb2_sync_preset_n
6	BIST_ON	R/W	0h	0 BIST on is taken from primary input port- bist_on, 1 bist_on is enabled. Reset Source: usb2_sync_preset_n
5	HSTX_BOOST_DEAMP_OFF	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_BOOST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_SAMP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HS_SAMP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22407. USB3P0SS_PHY2_UTMI_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HSRX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSRX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.518 USB3P0SS_PHY2_UTMI_REG6 Register

1 USB3P0SS_PHY2_UTMI_REG6 Register (Offset = 298h) [reset = 0h]

vbusvalid control, hs drive en threshold

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Table 14-22408. Instance Table

Instance Name	Physical Address
USB0	**0F90 8298h**

Figure 14-7408. USB3P0SS_PHY2_UTMI_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBUSVALID_CNTRL	VBUSVALID_L3_DEV_EN	HS_DRVEN_THRESHOLD					HS_DRVEN_TH_EN
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-22410. USB3P0SS_PHY2_UTMI_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	VBUSVALID_CNTRL	R/W	0h	0 vbusvalid comparator is not enabled in L3 device Powered Off state, 1 vbusvalid comparator is enabled in L3 device Powered Off state Reset Source: usb2_sync_preset_n
6	VBUSVALID_L3_DEV_EN	R/W	0h	0 Vbusvalid comparator output comes on vbusvalid primary output port, 1 Sessvalid comparator output comes on vbusvalid primary output port. Reset Source: usb2_sync_preset_n
5:1	HS_DRVEN_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HS_DRVEN_TH_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.519 USB3P0SS_PHY2_UTMI_REG7 Register

1 USB3P0SS_PHY2_UTMI_REG7 Register (Offset = 29Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22411. Instance Table

Instance Name	Physical Address
USB0	**0F90 829Ch**

Figure 14-7409. USB3P0SS_PHY2_UTMI_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSTX_BC_MODE	HSTX_BC_EN	HSTX_CHIRP_MODE	HSTX_CHIRP_EN	HSTX_EN_DEL	HSTX_EN_DEL_EN	HSTX	HSTX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22413. USB3P0SS_PHY2_UTMI_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HSTX_BC_MODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HSTX_BC_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSTX_CHIRP_MODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_CHIRP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSTX_EN_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HSTX_EN_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22413. USB3P0SS_PHY2_UTMI_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HSTX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.520 USB3P0SS_PHY2_UTMI_REG8 Register

1 USB3P0SS_PHY2_UTMI_REG8 Register (Offset = 2A0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22414. Instance Table

Instance Name	Physical Address
USB0	**0F90 82A0h**

Figure 14-7410. USB3P0SS_PHY2_UTMI_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HS_TERM	HS_TERM_EN	HSTX_DATA	HSTX_DATA_EN	HSTX_DRV	HSTX_DRV_EN	HSTX_PREDRV	HSTX_PREDRV_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22416. USB3P0SS_PHY2_UTMI_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_TERM	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HS_TERM_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSTX_DATA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_DATA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSTX_DRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HSTX_DRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22416. USB3P0SS_PHY2_UTMI_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HSTX_PREDRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_PREDRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.521 USB3P0SS_PHY2_UTMI_REG9 Register

1 USB3P0SS_PHY2_UTMI_REG9 Register (Offset = 2A4h) [reset = 0h]

hs delay values

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Table 14-22417. Instance Table

Instance Name	Physical Address
USB0	0F90 82A4h

Figure 14-7411. USB3P0SS_PHY2_UTMI_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKOFF_EN	SDC_SPACE			SDC_SPACE_EN	HSTX_EN_DEL_TH		HSTX_EN_DEL_TH_EN
R/W	R/W			R/W	R/W		R/W
0h	0h			0h	0h		0h

Table 14-22419. USB3P0SS_PHY2_UTMI_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLKOFF_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:4	SDC_SPACE	R/W	0h	000- The time between successive resistor calibration is 0ms, 001- The time between successive resistor calibration is 500ms, 010- The time between successive resistor calibration is 1000ms, 011- The time between successive resistor calibration is1500ms, 100- The time between successive resistor calibration is 2000ms, 101- The time between successive resistor calibration is 2500ms, 110- The time between successive resistor calibration is 3000ms, 111- The time between successive resistor calibration is 3500ms. Reset Source: usb2_sync_preset_n
3	SDC_SPACE_EN	R/W	0h	0- The time between successive resistor calibration taken as 1s by default, 1- The time between successive resistor calibration taken from UTMI_REG9[6:4]. Reset Source: usb2_sync_preset_n
2:1	HSTX_EN_DEL_TH	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22419. USB3P0SS_PHY2_UTMI_REG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HSTX_EN_DEL_TH_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.522 USB3P0SS_PHY2_UTMI_REG10 Register

1 USB3P0SS_PHY2_UTMI_REG10 Register (Offset = 2A8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22420. Instance Table

Instance Name	Physical Address
USB0	**0F90 82A8h**

Figure 14-7412. USB3P0SS_PHY2_UTMI_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_CLKON	PLL_CLKON_EN	BG_PD_BG_OK	BG_PD_BG_OK_EN	LSFS_SERX	LSFS_SERX_EN	LSFS_RX	LSFS_RX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22422. USB3P0SS_PHY2_UTMI_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_CLKON	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	PLL_CLKON_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BG_PD_BG_OK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BG_PD_BG_OK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	LSFS_SERX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	LSFS_SERX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22422. USB3P0SS_PHY2_UTMI_REG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LSFS_RX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	LSFS_RX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.523 USB3P0SS_PHY2_UTMI_REG11 Register

1 USB3P0SS_PHY2_UTMI_REG11 Register (Offset = 2ACh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22423. Instance Table

Instance Name	Physical Address
USB0	**0F90 82ACh**

Figure 14-7413. USB3P0SS_PHY2_UTMI_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLEAN_LINESTATE_SERX_MASK_EN	SERX_MASK_EN	SERX_MASK_THRESHOLD		LSFS_TX	LSFS_TX_EN	FSLS_EDGESEL	FSLS_EDGESEL_EN
R/W	R/W	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-22425. USB3P0SS_PHY2_UTMI_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLEAN_LINESTATE_SERX_MASK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SERX_MASK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	SERX_MASK_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	LSFS_TX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	LSFS_TX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22425. USB3P0SS_PHY2_UTMI_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FSLS_EDGESEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FSLS_EDGESEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.524 USB3P0SS_PHY2_UTMI_REG12 Register

1 USB3P0SS_PHY2_UTMI_REG12 Register (Offset = 2B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22426. Instance Table

Instance Name	Physical Address
USB0	**0F90 82B0h**

Figure 14-7414. USB3P0SS_PHY2_UTMI_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SERX_BIAS_EN		FSLS_TX_DATA	FSLS_TX_DATA_EN	FSLS_TX_SE0	FSLS_TX_SE0_EN	FSLS_TX_DRV	FSLS_TX_DRV_EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-22428. USB3P0SS_PHY2_UTMI_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SERX_BIAS_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	FSLS_TX_DATA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	FSLS_TX_DATA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	FSLS_TX_SE0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	FSLS_TX_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	FSLS_TX_DRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22428. USB3P0SS_PHY2_UTMI_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FSLS_TX_DRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.525 USB3P0SS_PHY2_UTMI_REG13 Register

1 USB3P0SS_PHY2_UTMI_REG13 Register (Offset = 2B4h) [reset = 0h]

serial mode

Return to Summary Table

Table 14-22429. Instance Table

Instance Name	Physical Address
USB0	**0F90 82B4h**

Figure 14-7415. USB3P0SS_PHY2_UTMI_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSLS_SERIALMODE_PULLUP2	FSLS_SERIALMODE_PULLUP2_EN	DM_PULLDOWN	DM_PULLDOWN_EN	DP_PULLDOWN	DP_PULLDOWN_EN	LANE_REVERSE	LANE_REVERSE_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22431. USB3P0SS_PHY2_UTMI_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FSLS_SERIALMODE_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	FSLS_SERIALMODE_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DM_PULLDOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DM_PULLDOWN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DP_PULLDOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22431. USB3P0SS_PHY2_UTMI_REG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DP_PULLDOWN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	LANE_REVERSE	R/W	0h	0- Polarity inversion of DP/DM is not done, 1- Polarity inversion of DP/DM is done Reset Source: usb2_sync_preset_n
0	LANE_REVERSE_EN	R/W	0h	0- Lane Reverse Value is taken from primary input portlane_reverse, 1- Lane Reverse Value taken from UTMI_REG13[1] Reset Source: usb2_sync_preset_n

14.9.2.3.2.526 USB3P0SS_PHY2_UTMI_REG14 Register

1 USB3P0SS_PHY2_UTMI_REG14 Register (Offset = 2B8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22432. Instance Table

Instance Name	Physical Address
USB0	**0F90 82B8h**

Figure 14-7416. USB3P0SS_PHY2_UTMI_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DM_PULLUP2	DM_PULLUP2_EN	DP_PULLUP2	DP_PULLUP2_EN	DM_PULLUP1	DM_PULLUP1_EN	DP_PULLUP1	DP_PULLUP1_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22434. USB3P0SS_PHY2_UTMI_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DM_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DM_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DP_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DP_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DM_PULLUP1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DM_PULLUP1_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22434. USB3P0SS_PHY2_UTMI_REG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DP_PULLUP1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DP_PULLUP1_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.527 USB3P0SS_PHY2_UTMI_REG15 Register

1 USB3P0SS_PHY2_UTMI_REG15 Register (Offset = 2BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22435. Instance Table

Instance Name	Physical Address
USB0	**0F90 82BCh**

Figure 14-7417. USB3P0SS_PHY2_UTMI_REG15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TXVALID_GATE_THRESHOLD_FS		TXVALID_GATE_THRESHOLD_HS		TED_EN_VALUE	TED_EN_CNT	ED_EN_VALUE	ED_EN_CNT
R/W		R/W		R/W	R/W	R/W	R/W
0h		0h		0h	0h	0h	0h

Table 14-22437. USB3P0SS_PHY2_UTMI_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	TXVALID_GATE_THRESHOLD_FS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	TXVALID_GATE_THRESHOLD_HS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TED_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	TED_EN_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ED_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22437. USB3P0SS_PHY2_UTMI_REG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ED_EN_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.528 USB3P0SS_PHY2_UTMI_REG16 Register

1 USB3P0SS_PHY2_UTMI_REG16 Register (Offset = 2C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22438. Instance Table

Instance Name	Physical Address
USB0	**0F90 82C0h**

Figure 14-7418. USB3P0SS_PHY2_UTMI_REG16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22440. USB3P0SS_PHY2_UTMI_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.529 USB3P0SS_PHY2_UTMI_REG17 Register

1 USB3P0SS_PHY2_UTMI_REG17 Register (Offset = 2C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22441. Instance Table

Instance Name	Physical Address
USB0	**0F90 82C4h**

Figure 14-7419. USB3P0SS_PHY2_UTMI_REG17 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SQUELCH_COUNT_IDLE</td><td>SQUELCH_COUNT_IDLE_EN</td><td colspan="4">TX_SQ_CNT</td><td>TX_SQ_CNT_EN</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
</table>

Table 14-22443. USB3P0SS_PHY2_UTMI_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SQUELCH_COUNT_IDLE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SQUELCH_COUNT_IDLE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	TX_SQ_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	TX_SQ_CNT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.530 USB3P0SS_PHY2_UTMI_REG18 Register

1 USB3P0SS_PHY2_UTMI_REG18 Register (Offset = 2C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22444. Instance Table

Instance Name	Physical Address
USB0	**0F90 82C8h**

Figure 14-7420. USB3P0SS_PHY2_UTMI_REG18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SLEEP_VALUE	SLEEP_EN	BIST_POWERUP	BIST_POWERUP_EN	POWERUP_EN	UNUSED	CLIPPER_EN	CLIPPER_EN_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22446. USB3P0SS_PHY2_UTMI_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	SLEEP_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SLEEP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BIST_POWERUP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIST_POWERUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	POWERUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22446. USB3P0SS_PHY2_UTMI_REG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLIPPER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CLIPPER_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.531 USB3P0SS_PHY2_UTMI_REG19 Register

1 USB3P0SS_PHY2_UTMI_REG19 Register (Offset = 2CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22447. Instance Table

Instance Name	Physical Address
USB0	**0F90 82CCh**

Figure 14-7421. USB3P0SS_PHY2_UTMI_REG19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							TED_SW_EN
R/W							R/W
0h							0h

Table 14-22449. USB3P0SS_PHY2_UTMI_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:1	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
0	TED_SW_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.532 USB3P0SS_PHY2_UTMI_REG20 Register

1 USB3P0SS_PHY2_UTMI_REG20 Register (Offset = 2D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22450. Instance Table

Instance Name	Physical Address
USB0	**0F90 82D0h**

Figure 14-7422. USB3P0SS_PHY2_UTMI_REG20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HOSTDISCON_RST_REG	HOSTDISCON_RST_REG_EN	CALIB_RST_DT					CALIB_RST_DT_EN
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-22452. USB3P0SS_PHY2_UTMI_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HOSTDISCON_RST_REG	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HOSTDISCON_RST_REG_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:1	CALIB_RST_DT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_RST_DT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.533 USB3P0SS_PHY2_UTMI_REG21 Register

1 USB3P0SS_PHY2_UTMI_REG21 Register (Offset = 2D4h) [reset = 0h]

Register UTMI_REG21

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Table 14-22453. Instance Table

Instance Name	Physical Address
USB0	**0F90 82D4h**

Figure 14-7423. USB3P0SS_PHY2_UTMI_REG21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_TRIGER_POSEDGE	AUTO_CAL_ENABLE	ABSVALID	ABSVALID_EN	VBUSVALID	VBUSVALID_EN	SUSPENDM	SUSPENDM_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22455. USB3P0SS_PHY2_UTMI_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_TRIGER_POSEDGE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	AUTO_CAL_ENABLE	R/W	0h	0- Dynamic resistor calibration is disabled, 1- Dynamic resistor calibration is enabled Reset Source: usb2_sync_preset_n
5	ABSVALID	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	ABSVALID_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VBUSVALID	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	VBUSVALID_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22455. USB3P0SS_PHY2_UTMI_REG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SUSPENDM	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SUSPENDM_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.534 USB3P0SS_PHY2_UTMI_REG22 Register

1 USB3P0SS_PHY2_UTMI_REG22 Register (Offset = 2D8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22456. Instance Table

Instance Name	Physical Address
USB0	0F90 82D8h

Figure 14-7424. USB3P0SS_PHY2_UTMI_REG22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BCCALIB_OFFSET							
R/W							
0h							

Table 14-22458. USB3P0SS_PHY2_UTMI_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BCCALIB_OFFSET	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.535 USB3P0SS_PHY2_UTMI_REG23 Register

1 USB3P0SS_PHY2_UTMI_REG23 Register (Offset = 2DCh) [reset = 0h]

hscalib code offset

Return to Summary Table

Table 14-22459. Instance Table

Instance Name	Physical Address
USB0	**0F90 82DCh**

Figure 14-7425. USB3P0SS_PHY2_UTMI_REG23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HSCALIB_OFFSET							
R/W							
0h							

Table 14-22461. USB3P0SS_PHY2_UTMI_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	HSCALIB_OFFSET	R/W	0h	Bit 0= 0- Final resistor calibration code going to HSTX is not offsetted, 1- Offset given by bits [6:2] is considered for computation of final resistor code going to HSTX. Bit 1= 0- ADD the offset given in bits [6:2] to the resistor calibration code before giving the code to HSTX, 1- Subtract the offset given in bits [6:2] from the reistor calibration code before giving code to HSTX. Bits 6:2= 00000 Programmable offset value for hs resistor calib code -HS OFFSET. Bit 7= reserved Reset Source: usb2_sync_preset_n

14.9.2.3.2.536 USB3P0SS_PHY2_UTMI_REG24 Register

1 USB3P0SS_PHY2_UTMI_REG24 Register (Offset = 2E0h) [reset = 0h]

fscalib code offset

Return to Summary Table

Table 14-22462. Instance Table

Instance Name	Physical Address
USB0	**0F90 82E0h**

Figure 14-7426. USB3P0SS_PHY2_UTMI_REG24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FSCALIB_OFFSET							
R/W							
0h							

Table 14-22464. USB3P0SS_PHY2_UTMI_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FSCALIB_OFFSET	R/W	0h	Bit 0= 0- Final resistor calibration code going to FSTX is not offsetted, 1- Offset given by bits [6:2] is used for computation of final resistor code going to FSTX. Bit 1= 0- ADD the offset given in bits [6:2] to the Resistor calibration code before giving the code to FSTX, 1- Subtract the offset given in bits [6:2] from the Resistor calibration code before giving code to FSTX. Bits 6:2= 00000 Programmable offset value for fs resistor calib code - FS OFFSET. Bit 7= reserved. Reset Source: usb2_sync_preset_n

14.9.2.3.2.537 USB3P0SS_PHY2_UTMI_REG25 Register

1 USB3P0SS_PHY2_UTMI_REG25 Register (Offset = 2E4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-22465. Instance Table

Instance Name	Physical Address
USB0	**0F90 82E4h**

Figure 14-7427. USB3P0SS_PHY2_UTMI_REG25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED	HSCALIB						
R/W	R/W						
0h	0h						

Table 14-22467. USB3P0SS_PHY2_UTMI_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	HSCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.538 USB3P0SS_PHY2_UTMI_REG26 Register

1 USB3P0SS_PHY2_UTMI_REG26 Register (Offset = 2E8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22468. Instance Table

Instance Name	Physical Address
USB0	**0F90 82E8h**

Figure 14-7428. USB3P0SS_PHY2_UTMI_REG26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	FSCALIB						
R/W	R/W						
0h	0h						

Table 14-22470. USB3P0SS_PHY2_UTMI_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	FSCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.539 USB3P0SS_PHY2_UTMI_REG27 Register

1 USB3P0SS_PHY2_UTMI_REG27 Register (Offset = 2ECh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22471. Instance Table

Instance Name	Physical Address
USB0	**0F90 82ECh**

Figure 14-7429. USB3P0SS_PHY2_UTMI_REG27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	BCCALIB						
R/W	R/W						
0h	0h						

Table 14-22473. USB3P0SS_PHY2_UTMI_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	BCCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.540 USB3P0SS_PHY2_UTMI_REG28 Register

1 USB3P0SS_PHY2_UTMI_REG28 Register (Offset = 2F0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22474. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 82F0h**

Figure 14-7430. USB3P0SS_PHY2_UTMI_REG28 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CDR_EB_WR_RESET</td><td colspan="6">UNUSED</td><td>SERX_EN_CNTRL_OPMODE01</td></tr>
<tr><td>R/W</td><td colspan="6">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
</table>

Table 14-22476. USB3P0SS_PHY2_UTMI_REG28 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:8	RESERVED	NONE	0h	Reserved
7	CDR_EB_WR_RESET	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:1	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SERX_EN_CNTRL_OPMODE01	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.541 USB3P0SS_PHY2_UTMI_REG29 Register

1 USB3P0SS_PHY2_UTMI_REG29 Register (Offset = 2F4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22477. Instance Table

Instance Name	Physical Address
USB0	**0F90 82F4h**

Figure 14-7431. USB3P0SS_PHY2_UTMI_REG29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED		PLL_STANDALONE	PLL_STANDALONE_EN	SPARE_OUT			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			

Table 14-22479. USB3P0SS_PHY2_UTMI_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PLL_STANDALONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_STANDALONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	SPARE_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.542 USB3P0SS_PHY2_UTMI_REG30 Register

1 USB3P0SS_PHY2_UTMI_REG30 Register (Offset = 2F8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22480. Instance Table

Instance Name	Physical Address
USB0	**0F90 82F8h**

Figure 14-7432. USB3P0SS_PHY2_UTMI_REG30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	PLL_480_CLOCK_GATE_OVR	SCAN_ATS_HS_CLOCK_GATE_OVR	VCO_PLL_CLOCK_GATE_OVR	DIG_DIV_REFCLOCK_GATE_OVR	FB_CLOCK_GATE_OVR	ANA_DIV_REFCLOCK_GATE_OVR	HS_CLOCK_GATE_OVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22482. USB3P0SS_PHY2_UTMI_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	PLL_480_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SCAN_ATS_HS_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	VCO_PLL_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DIG_DIV_REFCLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	FB_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22482. USB3P0SS_PHY2_UTMI_REG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ANA_DIV_REFCLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HS_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.543 USB3P0SS_PHY2_UTMI_UNUSED_REG0 Register

1 USB3P0SS_PHY2_UTMI_UNUSED_REG0 Register (Offset = 2FCh) [reset = 0h]

unused

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Table 14-22483. Instance Table

Instance Name	Physical Address
USB0	**0F90 82FCh**

Figure 14-7433. USB3P0SS_PHY2_UTMI_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22485. USB3P0SS_PHY2_UTMI_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.544 USB3P0SS_PHY2_UTMI_UNUSED_REG1 Register

1 USB3P0SS_PHY2_UTMI_UNUSED_REG1 Register (Offset = 300h) [reset = 0h]

unused

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Table 14-22486. Instance Table

Instance Name	**Physical Address**
USB0	**0F90 8300h**

Figure 14-7434. USB3P0SS_PHY2_UTMI_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22488. USB3P0SS_PHY2_UTMI_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.545 USB3P0SS_PHY2_UTMI_UNUSED_REG2 Register

1 USB3P0SS_PHY2_UTMI_UNUSED_REG2 Register (Offset = 304h) [reset = 0h]

unused

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Table 14-22489. Instance Table

Instance Name	Physical Address
USB0	**0F90 8304h**

Figure 14-7435. USB3P0SS_PHY2_UTMI_UNUSED_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UNUSED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22491. USB3P0SS_PHY2_UTMI_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.546 USB3P0SS_PHY2_UTMI_UNUSED_REG3 Register

1 USB3P0SS_PHY2_UTMI_UNUSED_REG3 Register (Offset = 308h) [reset = 0h]

unused

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Table 14-22492. Instance Table

Instance Name	Physical Address
USB0	**0F90 8308h**

Figure 14-7436. USB3P0SS_PHY2_UTMI_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-22494. USB3P0SS_PHY2_UTMI_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.547 USB3P0SS_PHY2_UTMI_REG31 Register

1 USB3P0SS_PHY2_UTMI_REG31 Register (Offset = 30Ch) [reset = 0h]

bist

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Table 14-22495. Instance Table

Instance Name	Physical Address
USB0	**0F90 830Ch**

Figure 14-7437. USB3P0SS_PHY2_UTMI_REG31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED						BIST_ERROR	BIST_COMPLETE
R						R	R
0h						0h	0h

Table 14-22497. USB3P0SS_PHY2_UTMI_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
1	BIST_ERROR	R	0h	0- BIST resulted in no Error, 1- BIST resulted in Error Reset Source: usb2_sync_preset_n
0	BIST_COMPLETE	R	0h	0- BIST is Not complete, 1- BIST is Complete Reset Source: usb2_sync_preset_n

14.9.2.3.2.548 USB3P0SS_PHY2_UTMI_REG32 Register

1 USB3P0SS_PHY2_UTMI_REG32 Register (Offset = 310h) [reset = 0h]

bist error count

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Table 14-22498. Instance Table

Instance Name	Physical Address
USB0	**0F90 8310h**

Figure 14-7438. USB3P0SS_PHY2_UTMI_REG32 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_ERR_COUNT							
R							
0h							

Table 14-22500. USB3P0SS_PHY2_UTMI_REG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BIST_ERR_COUNT	R	0h	00000000 Number of bytes that resulted in error while running BIST Reset Source: usb2_sync_preset_n

14.9.2.3.2.549 USB3P0SS_PHY2_UTMI_REG33 Register

1 USB3P0SS_PHY2_UTMI_REG33 Register (Offset = 314h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22501. Instance Table

Instance Name	Physical Address
USB0	**0F90 8314h**

Figure 14-7439. USB3P0SS_PHY2_UTMI_REG33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_POWERGOOD	AFE_HSRX_DIFF_DATA	HSRX_EN	HSRX_SAMPLER_ENABLE	CHIRP_MODE_EN	HSTX_EN	HSTX_EN_DELAYED	HSTX_BOOST_DEAMP_OFF
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22503. USB3P0SS_PHY2_UTMI_REG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	BG_POWERGOOD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	AFE_HSRX_DIFF_DATA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSRX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSRX_SAMPLER_ENABLE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CHIRP_MODE_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HSTX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22503. USB3P0SS_PHY2_UTMI_REG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HSTX_EN_DELAYED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_BOOST_DEAMP_OFF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.550 USB3P0SS_PHY2_UTMI_REG34 Register

1 USB3P0SS_PHY2_UTMI_REG34 Register (Offset = 318h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22504. Instance Table

Instance Name	Physical Address
USB0	**0F90 8318h**

Figure 14-7440. USB3P0SS_PHY2_UTMI_REG34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_DPRPU1_EN	O_DMRPU1_EN	O_DPRPU2_EN	O_DMRPU2_EN	O_DPRPD_EN	O_DMRPD_EN	O_OTGC_ID_PULLUP_EN	O_FS_EDGE_SEL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22506. USB3P0SS_PHY2_UTMI_REG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_DPRPU1_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_DMRPU1_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_DPRPU2_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_DMRPU2_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_DPRPD_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_DMRPD_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22506. USB3P0SS_PHY2_UTMI_REG34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	O_OTGC_ID_PULLUP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_FS_EDGE_SEL	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.551 USB3P0SS_PHY2_UTMI_REG35 Register

1 USB3P0SS_PHY2_UTMI_REG35 Register (Offset = 31Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22507. Instance Table

Instance Name	Physical Address
USB0	0F90 831Ch

Figure 14-7441. USB3P0SS_PHY2_UTMI_REG35 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
I_AFE_LSFSRX_ANA	O_LSFSTX_EN	O_LSFSDRV_EN	O_LSFS_DDI	O_ASSERT_SEZERO	O_LSFSRX_EN	O_SERX_EN	O_SERX_BIAS_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22509. USB3P0SS_PHY2_UTMI_REG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	I_AFE_LSFSRX_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_LSFSTX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_LSFSDRV_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_LSFS_DDI	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_ASSERT_SEZERO	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_LSFSRX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22509. USB3P0SS_PHY2_UTMI_REG35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	O_SERX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_SERX_BIAS_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.552 USB3P0SS_PHY2_UTMI_REG36 Register

1 USB3P0SS_PHY2_UTMI_REG36 Register (Offset = 320h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22510. Instance Table

Instance Name	Physical Address
USB0	**0F90 8320h**

Figure 14-7442. USB3P0SS_PHY2_UTMI_REG36 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_PLL_PSO	O_PLL_PSO_DELAY	O_PLL_PD	O_PLL_IPDIV				
R	R	R	R				
0h	0h	0h	0h				

Table 14-22512. USB3P0SS_PHY2_UTMI_REG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_PLL_PSO	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_PLL_PSO_DELAY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_PLL_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	O_PLL_IPDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.553 USB3P0SS_PHY2_UTMI_REG37 Register

1 USB3P0SS_PHY2_UTMI_REG37 Register (Offset = 324h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22513. Instance Table

Instance Name	Physical Address
USB0	**0F90 8324h**

Figure 14-7443. USB3P0SS_PHY2_UTMI_REG37 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">O_PLL_FBDIV_VALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22515. USB3P0SS_PHY2_UTMI_REG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	O_PLL_FBDIV_VALUE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.554 USB3P0SS_PHY2_UTMI_REG38 Register

1 USB3P0SS_PHY2_UTMI_REG38 Register (Offset = 328h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22516. Instance Table

Instance Name	Physical Address
USB0	**0F90 8328h**

Figure 14-7444. USB3P0SS_PHY2_UTMI_REG38 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_PLL_STANDBY	O_PLL_LDO_CORE_EN	O_PLL_LDO_REF_EN	O_AFE_SUSPENDM	O_OTGC_VBUSVALID_EN	O_OTGC_ABSVALID_EN	O_AFE_CLIPPER_EN	O_PLL_LDO_ISOLATION_CNTRL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22518. USB3P0SS_PHY2_UTMI_REG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_PLL_STANDBY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_PLL_LDO_CORE_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_PLL_LDO_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_AFE_SUSPENDM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_OTGC_VBUSVALID_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22518. USB3P0SS_PHY2_UTMI_REG38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	O_OTGC_ABSVALID_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_AFE_CLIPPER_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_PLL_LDO_ISOLATION_CNTRL	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.555 USB3P0SS_PHY2_UTMI_REG39 Register

1 USB3P0SS_PHY2_UTMI_REG39 Register (Offset = 32Ch) [reset = 0h]

unused

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Table 14-22519. Instance Table

Instance Name	Physical Address
USB0	**0F90 832Ch**

Figure 14-7445. USB3P0SS_PHY2_UTMI_REG39 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-22521. USB3P0SS_PHY2_UTMI_REG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.556 USB3P0SS_PHY2_UTMI_REG40 Register

1 USB3P0SS_PHY2_UTMI_REG40 Register (Offset = 330h) [reset = 0h]

unused

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Table 14-22522. Instance Table

Instance Name	Physical Address
USB0	**0F90 8330h**

Figure 14-7446. USB3P0SS_PHY2_UTMI_REG40 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-22524. USB3P0SS_PHY2_UTMI_REG40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.557 USB3P0SS_PHY2_UTMI_REG41 Register

1 USB3P0SS_PHY2_UTMI_REG41 Register (Offset = 334h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22525. Instance Table

Instance Name	Physical Address
USB0	**0F90 8334h**

Figure 14-7447. USB3P0SS_PHY2_UTMI_REG41 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I_TED_SQUELCH_ANA	I_USB2_RESCAL_CALIB_DONE	HS_CALIB_CODE					
R	R	R					
0h	0h	0h					

Table 14-22527. USB3P0SS_PHY2_UTMI_REG41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	I_TED_SQUELCH_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	I_USB2_RESCAL_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	HS_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.558 USB3P0SS_PHY2_UTMI_REG42 Register

1 USB3P0SS_PHY2_UTMI_REG42 Register (Offset = 338h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22528. Instance Table

Instance Name	Physical Address
USB0	**0F90 8338h**

Figure 14-7448. USB3P0SS_PHY2_UTMI_REG42 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS_SOF	ALL_CALIB_DONE	FS_CALIB_CODE					
R	R	R					
0h	0h	0h					

Table 14-22530. USB3P0SS_PHY2_UTMI_REG42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_SOF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ALL_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	FS_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.559 USB3P0SS_PHY2_UTMI_REG43 Register

1 USB3P0SS_PHY2_UTMI_REG43 Register (Offset = 33Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22531. Instance Table

Instance Name	Physical Address
USB0	**0F90 833Ch**

Figure 14-7449. USB3P0SS_PHY2_UTMI_REG43 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LS_MODE	FS_MODE_PRE	BC_CALIB_CODE					
R	R	R					
0h	0h	0h					

Table 14-22533. USB3P0SS_PHY2_UTMI_REG43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LS_MODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	FS_MODE_PRE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	BC_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.560 USB3P0SS_PHY2_UTMI_REG44 Register

1 USB3P0SS_PHY2_UTMI_REG44 Register (Offset = 340h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22534. Instance Table

Instance Name	Physical Address
USB0	**0F90 8340h**

Figure 14-7450. USB3P0SS_PHY2_UTMI_REG44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RSTN_REFCLOCK	RSTN_HS_CLOCK	RSTN_HS_TX_CLOCK	RSTN_BYTE_CLOCK	RSTN_SIECLOCK	RSTN_CLKDIV	RSTN_CALIB_CLKDIV	UDC_RSTN_CDR_ASYNC
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22536. USB3P0SS_PHY2_UTMI_REG44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RSTN_REFCLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RSTN_HS_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RSTN_HS_TX_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RSTN_BYTE_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RSTN_SIECLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RSTN_CLKDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22536. USB3P0SS_PHY2_UTMI_REG44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RSTN_CALIB_CLKDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	UDC_RSTN_CDR_ASYNC	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.561 USB3P0SS_PHY2_UTMI_REG45 Register

1 USB3P0SS_PHY2_UTMI_REG45 Register (Offset = 344h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22537. Instance Table

Instance Name	Physical Address
USB0	**0F90 8344h**

Figure 14-7451. USB3P0SS_PHY2_UTMI_REG45 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UDC_CALIB_RSTN	UDC_APB_RSTN	O_RSTN_CDR_ASYNC	O_PLL_CALIB_RSTN	BIST_MODE_RSTN	O_USB2_CALIB_RSTN	UDC_BC_CALIB_RSTN	GLOBAL_RESETN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22539. USB3P0SS_PHY2_UTMI_REG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UDC_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	UDC_APB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_RSTN_CDR_ASYNC	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_PLL_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	BIST_MODE_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_USB2_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22539. USB3P0SS_PHY2_UTMI_REG45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UDC_BC_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	GLOBAL_RESETN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.562 USB3P0SS_PHY2_UTMI_REG46 Register

1 USB3P0SS_PHY2_UTMI_REG46 Register (Offset = 348h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22540. Instance Table

Instance Name	Physical Address
USB0	**0F90 8348h**

Figure 14-7452. USB3P0SS_PHY2_UTMI_REG46 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	RECOVERY_CNT_EN	CLEAN_LINESTATE		BC_STATE_MACHINE_STATUS			
R	R	R		R			
0h	0h	0h		0h			

Table 14-22542. USB3P0SS_PHY2_UTMI_REG46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
6	RECOVERY_CNT_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	CLEAN_LINESTATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	BC_STATE_MACHINE_STATUS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.563 USB3P0SS_PHY2_UTMI_REG47 Register

1 USB3P0SS_PHY2_UTMI_REG47 Register (Offset = 34Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-22543. Instance Table

Instance Name	Physical Address
USB0	**0F90 834Ch**

Figure 14-7453. USB3P0SS_PHY2_UTMI_REG47 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FILTER_CNT_EN	HOST_OPMODE		DEV_OPMODE		I_DED_ANA	HS_HOSTDISCONNECT	LSFS_HOSTDISCONNECT
R	R		R		R	R	R
0h	0h		0h		0h	0h	0h

Table 14-22545. USB3P0SS_PHY2_UTMI_REG47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FILTER_CNT_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:5	HOST_OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	DEV_OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	I_DED_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	HS_HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22545. USB3P0SS_PHY2_UTMI_REG47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LSFS_HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.564 USB3P0SS_PHY2_UTMI_REG48 Register

1 USB3P0SS_PHY2_UTMI_REG48 Register (Offset = 350h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22546. Instance Table

Instance Name	Physical Address
USB0	**0F90 8350h**

Figure 14-7454. USB3P0SS_PHY2_UTMI_REG48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_TX_STATE		DATA_CNT_TX					
R		R					
0h		0h					

Table 14-22548. USB3P0SS_PHY2_UTMI_REG48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_TX_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	DATA_CNT_TX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.565 USB3P0SS_PHY2_UTMI_REG49 Register

1 USB3P0SS_PHY2_UTMI_REG49 Register (Offset = 354h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-22549. Instance Table

Instance Name	Physical Address
USB0	**0F90 8354h**

Figure 14-7455. USB3P0SS_PHY2_UTMI_REG49 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_RX_STATE		DATA_CNT_RX					
R		R					
0h		0h					

Table 14-22551. USB3P0SS_PHY2_UTMI_REG49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_RX_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	DATA_CNT_RX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.566 USB3P0SS_PHY2_UTMI_REG50 Register

1 USB3P0SS_PHY2_UTMI_REG50 Register (Offset = 358h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22552. Instance Table

Instance Name	Physical Address
USB0	**0F90 8358h**

Figure 14-7456. USB3P0SS_PHY2_UTMI_REG50 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_TOP_STATE				INC_DATA_CNT_TX	INC_DATA_CNT_RX	O_BG_PD	O_BG_PD_BG_OK
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-22554. USB3P0SS_PHY2_UTMI_REG50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	BIST_TOP_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	INC_DATA_CNT_TX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	INC_DATA_CNT_RX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_BG_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_BG_PD_BG_OK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.567 USB3P0SS_PHY2_UTMI_REG51 Register

1 USB3P0SS_PHY2_UTMI_REG51 Register (Offset = 35Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22555. Instance Table

Instance Name	Physical Address
USB0	**0F90 835Ch**

Figure 14-7457. USB3P0SS_PHY2_UTMI_REG51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POWERDOWN		RESET	SUSPENDM	TERMSELECT	DATABUS16_8	DPPULLDOWN	DMPULLDOWN
R		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-22557. USB3P0SS_PHY2_UTMI_REG51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	POWERDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RESET	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	SUSPENDM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TERMSELECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DATABUS16_8	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DPPULLDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22557. USB3P0SS_PHY2_UTMI_REG51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMPULLDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.568 USB3P0SS_PHY2_UTMI_REG52 Register

1 USB3P0SS_PHY2_UTMI_REG52 Register (Offset = 360h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22558. Instance Table

Instance Name	Physical Address
USB0	**0F90 8360h**

Figure 14-7458. USB3P0SS_PHY2_UTMI_REG52 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LANE_REVERSE	TXBITSTUFFENABLE	TXBITSTUFFENABLEH	XCVRSELECT		LINESTATE		HOSTDISCONNECT
R	R	R	R		R		R
0h	0h	0h	0h		0h		0h

Table 14-22560. USB3P0SS_PHY2_UTMI_REG52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LANE_REVERSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TXBITSTUFFENABLE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TXBITSTUFFENABLEH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	XCVRSELECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	LINESTATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22560. USB3P0SS_PHY2_UTMI_REG52 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.569 USB3P0SS_PHY2_UTMI_REG53 Register

1 USB3P0SS_PHY2_UTMI_REG53 Register (Offset = 364h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22561. Instance Table

Instance Name	Physical Address
USB0	**0F90 8364h**

Figure 14-7459. USB3P0SS_PHY2_UTMI_REG53 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSLSSERIALMODE	TX_ENABLE_N	TX_DAT	TX_SE0	SLEEPM	UNUSED	OPMODE	
R	R	R	R	R	R	R	
0h	0h	0h	0h	0h	0h	0h	

Table 14-22563. USB3P0SS_PHY2_UTMI_REG53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FSLSSERIALMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TX_ENABLE_N	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TX_DAT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	TX_SE0	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	SLEEPM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22563. USB3P0SS_PHY2_UTMI_REG53 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.570 USB3P0SS_PHY2_UTMI_REG54 Register

1 USB3P0SS_PHY2_UTMI_REG54 Register (Offset = 368h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22564. Instance Table

Instance Name	Physical Address
USB0	**0F90 8368h**

Figure 14-7460. USB3P0SS_PHY2_UTMI_REG54 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_DP	RX_DM	RX_RCV	UNUSED				
R	R	R	R				
0h	0h	0h	0h				

Table 14-22566. USB3P0SS_PHY2_UTMI_REG54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RX_DP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RX_DM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RX_RCV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.571 USB3P0SS_PHY2_UTMI_REG55 Register

1 USB3P0SS_PHY2_UTMI_REG55 Register (Offset = 36Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22567. Instance Table

Instance Name	Physical Address
USB0	**0F90 836Ch**

Figure 14-7461. USB3P0SS_PHY2_UTMI_REG55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TXVALIDH	TXVALID	TXREADY	RXVALIDH	RXVALID	RXACTIVE	RXERROR	UNUSED
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-22569. USB3P0SS_PHY2_UTMI_REG55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TXVALIDH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TXVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TXREADY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RXVALIDH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RXVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RXACTIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-22569. USB3P0SS_PHY2_UTMI_REG55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RXERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.572 USB3P0SS_PHY2_UTMI_REG56 Register

1 USB3P0SS_PHY2_UTMI_REG56 Register (Offset = 370h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22570. Instance Table

Instance Name	Physical Address
USB0	**0F90 8370h**

Figure 14-7462. USB3P0SS_PHY2_UTMI_REG56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAIN_UPPER							
R							
0h							

Table 14-22572. USB3P0SS_PHY2_UTMI_REG56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAIN_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.573 USB3P0SS_PHY2_UTMI_REG57 Register

1 USB3P0SS_PHY2_UTMI_REG57 Register (Offset = 374h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22573. Instance Table

Instance Name	Physical Address
USB0	**0F90 8374h**

Figure 14-7463. USB3P0SS_PHY2_UTMI_REG57 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAIN_LOWER							
R							
0h							

Table 14-22575. USB3P0SS_PHY2_UTMI_REG57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAIN_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.574 USB3P0SS_PHY2_UTMI_REG58 Register

1 USB3P0SS_PHY2_UTMI_REG58 Register (Offset = 378h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22576. Instance Table

Instance Name	Physical Address
USB0	**0F90 8378h**

Figure 14-7464. USB3P0SS_PHY2_UTMI_REG58 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATAOUT_UPPER							
R							
0h							

Table 14-22578. USB3P0SS_PHY2_UTMI_REG58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAOUT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.575 USB3P0SS_PHY2_UTMI_REG59 Register

1 USB3P0SS_PHY2_UTMI_REG59 Register (Offset = 37Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-22579. Instance Table

Instance Name	Physical Address
USB0	**0F90 837Ch**

Figure 14-7465. USB3P0SS_PHY2_UTMI_REG59 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAOUT_LOWER							
R							
0h							

Table 14-22581. USB3P0SS_PHY2_UTMI_REG59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAOUT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.9.2.3.2.576 USB3P0SS_PHY2_UTMI_UNUSED_REG6 Register

1 USB3P0SS_PHY2_UTMI_UNUSED_REG6 Register (Offset = 380h) [reset = 0h]

UNUSED

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Table 14-22582. Instance Table

Instance Name	Physical Address
USB0	**0F90 8380h**

Figure 14-7466. USB3P0SS_PHY2_UTMI_UNUSED_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-22584. USB3P0SS_PHY2_UTMI_UNUSED_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.2.3.2.577 USB3P0SS_PHY2_UTMI_UNUSED_REG7 Register

1 USB3P0SS_PHY2_UTMI_UNUSED_REG7 Register (Offset = 384h) [reset = 0h]

UNUSED

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Table 14-22585. Instance Table

Instance Name	Physical Address
USB0	**0F90 8384h**

Figure 14-7467. USB3P0SS_PHY2_UTMI_UNUSED_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-22587. USB3P0SS_PHY2_UTMI_UNUSED_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.9.3 Memory Interfaces Registers

14.9.3.1 FSS

FSS

14.9.3.1.1 FSS Summaries

FSS Summaries

Table 14-22588. FSS_GENREGS Registers, Base Address=0FC0 0000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS_GENREGS_REVISION	0FC0 0000h

14.9.3.1.2 FSS Registers

FSS Registers

14.9.3.1.2.1 FSS_GENREGS_REVISION Register

1 FSS_GENREGS_REVISION Register (Offset = 0h) [reset = 68501901h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-22589. Instance Table

Instance Name	Physical Address
FSS0	**0FC0 0000h**

Figure 14-7468. FSS_GENREGS_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6850h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODID							
R							
6850h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
3h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-22591. FSS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field Reset Source: vbus_mod_g_rst_n
15:11	REVRTL	R	3h	RTL revision. Will vary depending on release. Reset Source: vbus_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: vbus_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: vbus_mod_g_rst_n

14.9.3.2 FSS_FSAS_0

FSS_FSAS_0

14.9.3.2.1 FSS_FSAS_0 Summaries

FSS_FSAS_0 Summaries

Table 14-22592. FSS_FSAS_GENREGS Registers, Base Address=0FC1 0000h, Length=256

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_FSAS_GENREGS_REVISION	0FC1 0000h
4h	32	FSS_FSAS_GENREGS_SYSCONFIG	0FC1 0004h
8h	32	FSS_FSAS_GENREGS_FRAG_ADR	0FC1 0008h
Ch	32	FSS_FSAS_GENREGS_FRAG_CTL	0FC1 000Ch
0h	32	FSS_FSAS_GENREGS_IRQ_EOI	0FC1 0000h
4h	32	FSS_FSAS_GENREGS_IRQ_STATUS_RAW	0FC1 0004h
8h	32	FSS_FSAS_GENREGS_IRQ_STATUS	0FC1 0008h
Ch	32	FSS_FSAS_GENREGS_IRQ_ENABLE_SET	0FC1 000Ch
10h	32	FSS_FSAS_GENREGS_IRQ_ENABLE_CLR	0FC1 0010h
0h	32	FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J	0FC1 0000h + formula
4h	32	FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J	0FC1 0004h + formula
0h	32	FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR	0FC1 0000h
4h	32	FSS_FSAS_GENREGS_ERR_ECC_TYPE	0FC1 0004h
8h	32	FSS_FSAS_GENREGS_ERR_WRT_TYPE	0FC1 0008h

Table 14-22593. FSS_FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_FSAS_OTFA_REGS_REVID	0FC2 0000h
4h	32	FSS_FSAS_OTFA_REGS_SCFG	0FC2 0004h
8h	32	FSS_FSAS_OTFA_REGS_ISR	0FC2 0008h
Ch	32	FSS_FSAS_OTFA_REGS_IS	0FC2 000Ch
10h	32	FSS_FSAS_OTFA_REGS_IES	0FC2 0010h
14h	32	FSS_FSAS_OTFA_REGS_IEC	0FC2 0014h
18h	32	FSS_FSAS_OTFA_REGS_CCFG	0FC2 0018h
1Ch	32	FSS_FSAS_OTFA_REGS_CSTATUS	0FC2 001Ch
20h	32	FSS_FSAS_OTFA_REGS_RGCFG0	0FC2 0020h
24h	32	FSS_FSAS_OTFA_REGS_RGMACST0	0FC2 0024h
28h	32	FSS_FSAS_OTFA_REGS_RGST0	0FC2 0028h
2Ch	32	FSS_FSAS_OTFA_REGS_RGSI0	0FC2 002Ch
30h	32	FSS_FSAS_OTFA_REGS_RKEYE00	0FC2 0030h
34h	32	FSS_FSAS_OTFA_REGS_RKEYE01	0FC2 0034h
38h	32	FSS_FSAS_OTFA_REGS_RKEYE02	0FC2 0038h
3Ch	32	FSS_FSAS_OTFA_REGS_RKEYE03	0FC2 003Ch
40h	32	FSS_FSAS_OTFA_REGS_RKEYE04	0FC2 0040h
44h	32	FSS_FSAS_OTFA_REGS_RKEYE05	0FC2 0044h
48h	32	FSS_FSAS_OTFA_REGS_RKEYE06	0FC2 0048h
4Ch	32	FSS_FSAS_OTFA_REGS_RKEYE07	0FC2 004Ch

Table 14-22593. FSS_FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
50h	32	FSS_FSAS_OTFA_REGS_RKEYEP00	0FC2 0050h
54h	32	FSS_FSAS_OTFA_REGS_RKEYEP01	0FC2 0054h
58h	32	FSS_FSAS_OTFA_REGS_RKEYEP02	0FC2 0058h
5Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP03	0FC2 005Ch
60h	32	FSS_FSAS_OTFA_REGS_RKEYEP04	0FC2 0060h
64h	32	FSS_FSAS_OTFA_REGS_RKEYEP05	0FC2 0064h
68h	32	FSS_FSAS_OTFA_REGS_RKEYEP06	0FC2 0068h
6Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP07	0FC2 006Ch
70h	32	FSS_FSAS_OTFA_REGS_RKEYA00	0FC2 0070h
74h	32	FSS_FSAS_OTFA_REGS_RKEYA01	0FC2 0074h
78h	32	FSS_FSAS_OTFA_REGS_RKEYA02	0FC2 0078h
7Ch	32	FSS_FSAS_OTFA_REGS_RKEYA03	0FC2 007Ch
80h	32	FSS_FSAS_OTFA_REGS_RKEYAP00	0FC2 0080h
84h	32	FSS_FSAS_OTFA_REGS_RKEYAP01	0FC2 0084h
88h	32	FSS_FSAS_OTFA_REGS_RKEYAP02	0FC2 0088h
8Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP03	0FC2 008Ch
90h	32	FSS_FSAS_OTFA_REGS_RIV00	0FC2 0090h
94h	32	FSS_FSAS_OTFA_REGS_RIV01	0FC2 0094h
98h	32	FSS_FSAS_OTFA_REGS_RIV02	0FC2 0098h
9Ch	32	FSS_FSAS_OTFA_REGS_RIV03	0FC2 009Ch
A0h	32	FSS_FSAS_OTFA_REGS_RGCFG1	0FC2 00A0h
A4h	32	FSS_FSAS_OTFA_REGS_RGMACST1	0FC2 00A4h
A8h	32	FSS_FSAS_OTFA_REGS_RGST1	0FC2 00A8h
ACh	32	FSS_FSAS_OTFA_REGS_RGSI1	0FC2 00ACh
B0h	32	FSS_FSAS_OTFA_REGS_RKEYE10	0FC2 00B0h
B4h	32	FSS_FSAS_OTFA_REGS_RKEYE11	0FC2 00B4h
B8h	32	FSS_FSAS_OTFA_REGS_RKEYE12	0FC2 00B8h
BCh	32	FSS_FSAS_OTFA_REGS_RKEYE13	0FC2 00BCh
C0h	32	FSS_FSAS_OTFA_REGS_RKEYE14	0FC2 00C0h
C4h	32	FSS_FSAS_OTFA_REGS_RKEYE15	0FC2 00C4h
C8h	32	FSS_FSAS_OTFA_REGS_RKEYE16	0FC2 00C8h
CCh	32	FSS_FSAS_OTFA_REGS_RKEYE17	0FC2 00CCh
D0h	32	FSS_FSAS_OTFA_REGS_RKEYEP10	0FC2 00D0h
D4h	32	FSS_FSAS_OTFA_REGS_RKEYEP11	0FC2 00D4h
D8h	32	FSS_FSAS_OTFA_REGS_RKEYEP12	0FC2 00D8h
DCh	32	FSS_FSAS_OTFA_REGS_RKEYEP13	0FC2 00DCh
E0h	32	FSS_FSAS_OTFA_REGS_RKEYEP14	0FC2 00E0h
E4h	32	FSS_FSAS_OTFA_REGS_RKEYEP15	0FC2 00E4h
E8h	32	FSS_FSAS_OTFA_REGS_RKEYEP16	0FC2 00E8h
ECh	32	FSS_FSAS_OTFA_REGS_RKEYEP17	0FC2 00ECh
F0h	32	FSS_FSAS_OTFA_REGS_RKEYA10	0FC2 00F0h
F4h	32	FSS_FSAS_OTFA_REGS_RKEYA11	0FC2 00F4h
F8h	32	FSS_FSAS_OTFA_REGS_RKEYA12	0FC2 00F8h
FCh	32	FSS_FSAS_OTFA_REGS_RKEYA13	0FC2 00FCh

Table 14-22593. FSS_FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
100h	32	FSS_FSAS_OTFA_REGS_RKEYAP10	0FC2 0100h
104h	32	FSS_FSAS_OTFA_REGS_RKEYAP11	0FC2 0104h
108h	32	FSS_FSAS_OTFA_REGS_RKEYAP12	0FC2 0108h
10Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP13	0FC2 010Ch
110h	32	FSS_FSAS_OTFA_REGS_RIV10	0FC2 0110h
114h	32	FSS_FSAS_OTFA_REGS_RIV11	0FC2 0114h
118h	32	FSS_FSAS_OTFA_REGS_RIV12	0FC2 0118h
11Ch	32	FSS_FSAS_OTFA_REGS_RIV13	0FC2 011Ch
120h	32	FSS_FSAS_OTFA_REGS_RGCFG2	0FC2 0120h
124h	32	FSS_FSAS_OTFA_REGS_RGMACST2	0FC2 0124h
128h	32	FSS_FSAS_OTFA_REGS_RGST2	0FC2 0128h
12Ch	32	FSS_FSAS_OTFA_REGS_RGSI2	0FC2 012Ch
130h	32	FSS_FSAS_OTFA_REGS_RKEYE20	0FC2 0130h
134h	32	FSS_FSAS_OTFA_REGS_RKEYE21	0FC2 0134h
138h	32	FSS_FSAS_OTFA_REGS_RKEYE22	0FC2 0138h
13Ch	32	FSS_FSAS_OTFA_REGS_RKEYE23	0FC2 013Ch
140h	32	FSS_FSAS_OTFA_REGS_RKEYE24	0FC2 0140h
144h	32	FSS_FSAS_OTFA_REGS_RKEYE25	0FC2 0144h
148h	32	FSS_FSAS_OTFA_REGS_RKEYE26	0FC2 0148h
14Ch	32	FSS_FSAS_OTFA_REGS_RKEYE27	0FC2 014Ch
150h	32	FSS_FSAS_OTFA_REGS_RKEYEP20	0FC2 0150h
154h	32	FSS_FSAS_OTFA_REGS_RKEYEP21	0FC2 0154h
158h	32	FSS_FSAS_OTFA_REGS_RKEYEP22	0FC2 0158h
15Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP23	0FC2 015Ch
160h	32	FSS_FSAS_OTFA_REGS_RKEYEP24	0FC2 0160h
164h	32	FSS_FSAS_OTFA_REGS_RKEYEP25	0FC2 0164h
168h	32	FSS_FSAS_OTFA_REGS_RKEYEP26	0FC2 0168h
16Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP27	0FC2 016Ch
170h	32	FSS_FSAS_OTFA_REGS_RKEYA20	0FC2 0170h
174h	32	FSS_FSAS_OTFA_REGS_RKEYA21	0FC2 0174h
178h	32	FSS_FSAS_OTFA_REGS_RKEYA22	0FC2 0178h
17Ch	32	FSS_FSAS_OTFA_REGS_RKEYA23	0FC2 017Ch
180h	32	FSS_FSAS_OTFA_REGS_RKEYAP20	0FC2 0180h
184h	32	FSS_FSAS_OTFA_REGS_RKEYAP21	0FC2 0184h
188h	32	FSS_FSAS_OTFA_REGS_RKEYAP22	0FC2 0188h
18Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP23	0FC2 018Ch
190h	32	FSS_FSAS_OTFA_REGS_RIV20	0FC2 0190h
194h	32	FSS_FSAS_OTFA_REGS_RIV21	0FC2 0194h
198h	32	FSS_FSAS_OTFA_REGS_RIV22	0FC2 0198h
19Ch	32	FSS_FSAS_OTFA_REGS_RIV23	0FC2 019Ch
1A0h	32	FSS_FSAS_OTFA_REGS_RGCFG3	0FC2 01A0h
1A4h	32	FSS_FSAS_OTFA_REGS_RGMACST3	0FC2 01A4h
1A8h	32	FSS_FSAS_OTFA_REGS_RGST3	0FC2 01A8h
1ACh	32	FSS_FSAS_OTFA_REGS_RGSI3	0FC2 01ACh

Table 14-22593. FSS_FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
1B0h	32	FSS_FSAS_OTFA_REGS_RKEYE30	0FC2 01B0h
1B4h	32	FSS_FSAS_OTFA_REGS_RKEYE31	0FC2 01B4h
1B8h	32	FSS_FSAS_OTFA_REGS_RKEYE32	0FC2 01B8h
1BCh	32	FSS_FSAS_OTFA_REGS_RKEYE33	0FC2 01BCh
1C0h	32	FSS_FSAS_OTFA_REGS_RKEYE34	0FC2 01C0h
1C4h	32	FSS_FSAS_OTFA_REGS_RKEYE35	0FC2 01C4h
1C8h	32	FSS_FSAS_OTFA_REGS_RKEYE36	0FC2 01C8h
1CCh	32	FSS_FSAS_OTFA_REGS_RKEYE37	0FC2 01CCh
1D0h	32	FSS_FSAS_OTFA_REGS_RKEYEP30	0FC2 01D0h
1D4h	32	FSS_FSAS_OTFA_REGS_RKEYEP31	0FC2 01D4h
1D8h	32	FSS_FSAS_OTFA_REGS_RKEYEP32	0FC2 01D8h
1DCh	32	FSS_FSAS_OTFA_REGS_RKEYEP33	0FC2 01DCh
1E0h	32	FSS_FSAS_OTFA_REGS_RKEYEP34	0FC2 01E0h
1E4h	32	FSS_FSAS_OTFA_REGS_RKEYEP35	0FC2 01E4h
1E8h	32	FSS_FSAS_OTFA_REGS_RKEYEP36	0FC2 01E8h
1ECh	32	FSS_FSAS_OTFA_REGS_RKEYEP37	0FC2 01ECh
1F0h	32	FSS_FSAS_OTFA_REGS_RKEYA30	0FC2 01F0h
1F4h	32	FSS_FSAS_OTFA_REGS_RKEYA31	0FC2 01F4h
1F8h	32	FSS_FSAS_OTFA_REGS_RKEYA32	0FC2 01F8h
1FCh	32	FSS_FSAS_OTFA_REGS_RKEYA33	0FC2 01FCh
200h	32	FSS_FSAS_OTFA_REGS_RKEYAP30	0FC2 0200h
204h	32	FSS_FSAS_OTFA_REGS_RKEYAP31	0FC2 0204h
208h	32	FSS_FSAS_OTFA_REGS_RKEYAP32	0FC2 0208h
20Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP33	0FC2 020Ch
210h	32	FSS_FSAS_OTFA_REGS_RIV30	0FC2 0210h
214h	32	FSS_FSAS_OTFA_REGS_RIV31	0FC2 0214h
218h	32	FSS_FSAS_OTFA_REGS_RIV32	0FC2 0218h
21Ch	32	FSS_FSAS_OTFA_REGS_RIV33	0FC2 021Ch
220h	32	FSS_FSAS_OTFA_REGS_IRQADDINFO0	0FC2 0220h
224h	32	FSS_FSAS_OTFA_REGS_IRQADDINFO1	0FC2 0224h
228h	32	FSS_FSAS_OTFA_REGS_MACCACHEINFO	0FC2 0228h
22Ch	32	FSS_FSAS_OTFA_REGS_RMWRMCNT	0FC2 022Ch

Table 14-22594. FSS_DAT_REG1 Registers, Base Address=6000 0000h, Length=134217728

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_DAT_REG1_HPB_DATA_MEM_J	6000 0000h + formula

Table 14-22595. FSS_DAT_REG0 Registers, Base Address=0004 0000 0000h, Length=4294967296

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_DAT_REG0_HPB_DATA_MEM_J	0004 0000 0000h + formula

Table 14-22596. FSS_DAT_REG3 Registers, Base Address=0005 0000 0000h, Length=4294967296

Offset	Length	Register Name	FSS0_FSAS_0 Physical Address
0h	32	FSS_DAT_REG3_HPB_DATA_MEM_J	0005 0000 0000h + formula

14.9.3.2.2 FSS_FSAS_0 Registers

FSS_FSAS_0 Registers

14.9.3.2.2.1 FSS_FSAS_GENREGS_REVISION Register

1 FSS_FSAS_GENREGS_REVISION Register (Offset = 0h) [reset = 68501901h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-22597. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0000h**

Figure 14-7469. FSS_FSAS_GENREGS_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6850h							

23	22	21	20	19	18	17	16
MODID							
R							
6850h							

15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
3h					1h		

7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-22599. FSS_FSAS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field Reset Source: vbus_mod_g_rst_n
15:11	REVRTL	R	3h	RTL revision. Will vary depending on release. Reset Source: vbus_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: vbus_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.2 FSS_FSAS_GENREGS_SYSCONFIG Register

1 FSS_FSAS_GENREGS_SYSCONFIG Register (Offset = 4h) [reset = 0h]

Controls various parameters of the cotroller state.

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Table 14-22600. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC1 0004h

Figure 14-7470. FSS_FSAS_GENREGS_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							OSPI_32B_DISABLE_MODE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
DISXIP	OSPI_DDR_DISABLE_MODE	RESERVED		ECC_DISABLE_ADR	FSS_AES_EN_IPCFG	RESERVED	ECC_EN
R/W	R/W	NONE		R/W	R	NONE	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-22602. FSS_FSAS_GENREGS_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	OSPI_32B_DISABLE_MODE	R/W	0h	0 OSPI 32bit mode enabled. 1 OSPI 32bit mode disabled Reset Source: vbus_mod_g_rst_n
7	DISXIP	R/W	0h	0 XIP Prefetch Enabled. 1 XIP prefetch disabled Reset Source: vbus_mod_g_rst_n
6	OSPI_DDR_DISABLE_MODE	R/W	0h	0 OSPI DDR mode enabled. 1 OSPI DDR mode disabled Reset Source: vbus_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	ECC_DISABLE_ADR	R/W	0h	0 Block address within ECC calculation, 1 Block address not within ECC calculation Reset Source: vbus_mod_g_rst_n
2	FSS_AES_EN_IPCFG	R	0h	1 select security, 0 disable security Reset Source: vbus_mod_g_rst_n
1	RESERVED	NONE	0h	Reserved
0	ECC_EN	R/W	0h	0 ECC disabled. 1 ECC enabled Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.3 FSS_FSAS_GENREGS_FRAG_ADR Register

1 FSS_FSAS_GENREGS_FRAG_ADR Register (Offset = 8h) [reset = 0h]

This FRAG_ADR is the address of a request that frag_hi or frag_lo boundary occurs

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Table 14-22603. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0008h**

Figure 14-7471. FSS_FSAS_GENREGS_FRAG_ADR Name Register

31	30	29	28	27	26	25	24
FRAG_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
FRAG_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
FRAG_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
FRAG_ADDR							
R/W							
0h							

Table 14-22605. FSS_FSAS_GENREGS_FRAG_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAG_ADDR	R/W	0h	This address is used to determine the boundary of frag_hi and flag_lo Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.4 FSS_FSAS_GENREGS_FRAG_CTL Register

1 FSS_FSAS_GENREGS_FRAG_CTL Register (Offset = Ch) [reset = 3h]

The FRAG_CTL determins which frag region is fragmented

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Table 14-22606. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 000Ch**

Figure 14-7472. FSS_FSAS_GENREGS_FRAG_CTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						FRAG_HI	FRAG_LO
NONE						R/W	R/W
0h						1h	1h

Table 14-22608. FSS_FSAS_GENREGS_FRAG_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	FRAG_HI	R/W	1h	When set any address greater than or equal to frag_addr will be fragmented to 16 bits Reset Source: vbus_mod_g_rst_n
0	FRAG_LO	R/W	1h	When set any address less than frag_addr will be fragmented to 16 bits Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.5 FSS_FSAS_GENREGS_IRQ_EOI Register

1 FSS_FSAS_GENREGS_IRQ_EOI Register (Offset = 0h) [reset = 0h]

The End of Interrupt (EOI) MISC Register allows the CPU to acknowledge completion of an interrupt by writing to the EOI for MISC interrupt sources. An eoi_write signal will be generated and another interrupt will be triggered if interrupt sources remain. This register will be reset one cycle after it has been written to.

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Table 14-22609. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0000h**

Figure 14-7473. FSS_FSAS_GENREGS_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							R/W
0h							0h

Table 14-22611. FSS_FSAS_GENREGS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	R/W	0h	Write with bit position of targeted interrupt. (E.g. Ext FSS ECC is bit 0). Upon write, level interrupt will clear and if un-serviced will issue another pulse interrupt Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.6 FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register

1 FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register (Offset = 4h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-22612. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0004h**

Figure 14-7474. FSS_FSAS_GENREGS_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-22614. FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.7 FSS_FSAS_GENREGS_IRQ_STATUS Register

1 FSS_FSAS_GENREGS_IRQ_STATUS Register (Offset = 8h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-22615. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0008h**

Figure 14-7475. FSS_FSAS_GENREGS_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-22617. FSS_FSAS_GENREGS_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.8 FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register

1 FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register (Offset = Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-22618. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 000Ch**

Figure 14-7476. FSS_FSAS_GENREGS_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-22620. FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.9 FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register

1 FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register (Offset = 10h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

Return to Summary Table

Table 14-22621. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0010h**

Figure 14-7477. FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>ECC_WRITE_NONALIGN</td><td>ECC_ERROR_2BIT</td><td>ECC_ERROR_1BIT</td></tr>
<tr><td colspan="5">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-22623. FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.10 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register

1 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register (Offset = 0h + formula) [reset = 0h]

This defines the start of the ECC region in 4KBytes steps.

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Offset = (j * 8h); where j = 0 to 3d

Table 14-22624. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0000h + formula**

Figure 14-7478. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START							
R/W							
0h							

Table 14-22626. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START	R/W	0h	This defines the start of the ECC region in 4KBytes steps. Address start = {start[19:0], 0x000} 0x0 means the start is 0x0000_0000 0x1 means the start is 0x0000_1000 0xA means the start is 0x0000_A000 Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.11 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register

1 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register (Offset = 4h + formula) [reset = 0h]

This defines the size of the ECC region in 4KBytes steps.

Return to Summary Table

Offset = (j * 8h); where j = 0 to 3d

Table 14-22627. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0004h + formula**

Figure 14-7479. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE							
R/W							
0h							

Table 14-22629. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE	R/W	0h	This defines the size of the ECC region in 4KBytes steps 0x0 means the size is zero and disabled 0x1 means the size is 4KBytes 0xA means the size is 40KBytes 0xF_FFFF means the size is 4GBytes Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.12 FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register

1 FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register (Offset = 0h) [reset = 0h]

The ERR_ECC_BLOCK_ADR register holds the current top of stack ECC error block address, this is only valid when the ecc_err_valid is set

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Table 14-22630. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0000h**

Figure 14-7480. FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ECC_ERROR_BLOCK_ADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ECC_ERROR_BLOCK_ADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ECC_ERROR_BLOCK_ADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">ECC_ERROR_BLOCK_ADDR</td><td colspan="5">RESERVED</td></tr>
<tr><td colspan="3">R</td><td colspan="5">NONE</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-22632. FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	ECC_ERROR_BLOCK_ADDR	R	0h	ECC 32 byte aligned block address Reset Source: vbus_mod_g_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.9.3.2.2.13 FSS_FSAS_GENREGS_ERR_ECC_TYPE Register

1 FSS_FSAS_GENREGS_ERR_ECC_TYPE Register (Offset = 4h) [reset = 0h]

The ERR_ECC_TYPE register holds the current top of stack ECC error info, this is only valid when the ecc_err_valid is set

Return to Summary Table

Table 14-22633. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0004h**

Figure 14-7481. FSS_FSAS_GENREGS_ERR_ECC_TYPE Name Register

31	30	29	28	27	26	25	24
ECC_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECC_ERR_ADR	ECC_ERR_MAC	ECC_ERR_DA1	ECC_ERR_DA0	ECC_ERR_DED	ECC_ERR_SEC
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-22635. FSS_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_ERR_VALID	R/W1TC	0h	When set indicates that there is valid ECC error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:6	RESERVED	NONE	0h	Reserved
5	ECC_ERR_ADR	R	0h	When set indicates that there was a single error detected within the address field Reset Source: vbus_mod_g_rst_n
4	ECC_ERR_MAC	R	0h	When set indicates that there was a single error detected within the MAC field Reset Source: vbus_mod_g_rst_n
3	ECC_ERR_DA1	R	0h	When set indicates that there was a single error detected within the High Data word Reset Source: vbus_mod_g_rst_n
2	ECC_ERR_DA0	R	0h	When set indicates that there was a single error detected within the Low Data word Reset Source: vbus_mod_g_rst_n

Table 14-22635. FSS_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ECC_ERR_DED	R	0h	When set indicates that there was a double error detected for the block Reset Source: vbus_mod_g_rst_n
0	ECC_ERR_SEC	R	0h	hen set indicates that there was a single error detected for the block Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.14 FSS_FSAS_GENREGS_ERR_WRT_TYPE Register

1 FSS_FSAS_GENREGS_ERR_WRT_TYPE Register (Offset = 8h) [reset = 0h]

The ERR_WRT_TYPE register holds the current top of stack write error info. this is only valid when the wrt_err_valid is set

Return to Summary Table

Table 14-22636. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC1 0008h**

Figure 14-7482. FSS_FSAS_GENREGS_ERR_WRT_TYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>WRT_ERR_VALID</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W1TC</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRT_ERR_BEN</td><td>WRT_ERR_ADR</td><td colspan="4">WRT_ERR_ROUTEID</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WRT_ERR_ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22638. FSS_FSAS_GENREGS_ERR_WRT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRT_ERR_VALID	R/W1TC	0h	When set indicates that there is valid write error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:14	RESERVED	NONE	0h	Reserved
13	WRT_ERR_BEN	R	0h	When set indicates that there was a write error due to a non-contiguous byte enables Reset Source: vbus_mod_g_rst_n
12	WRT_ERR_ADR	R	0h	When set indicates that there was a write error due to a non-aligned address Reset Source: vbus_mod_g_rst_n
11:0	WRT_ERR_ROUTEID	R	0h	Indicates the Route ID for the Initiator that caused the write error Reset Source: vbus_mod_g_rst_n

14.9.3.2.2.15 FSS_FSAS_OTFA_REGS_REVID Register

1 FSS_FSAS_OTFA_REGS_REVID Register (Offset = 0h) [reset = 47500100h]

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Table 14-22639. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0000h**

Figure 14-7483. FSS_FSAS_OTFA_REGS_REVID Name Register

31	30	29	28	27	26	25	24
REVID							
R							
47500100h							
23	22	21	20	19	18	17	16
REVID							
R							
47500100h							
15	14	13	12	11	10	9	8
REVID							
R							
47500100h							
7	6	5	4	3	2	1	0
REVID							
R							
47500100h							

Table 14-22641. FSS_FSAS_OTFA_REGS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REVID	R	47500100h	REVID Reset Source: rst_modg_rst_n

14.9.3.2.2.16 FSS_FSAS_OTFA_REGS_SCFG Register

1 FSS_FSAS_OTFA_REGS_SCFG Register (Offset = 4h) [reset = 2h]

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Table 14-22642. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0004h**

Figure 14-7484. FSS_FSAS_OTFA_REGS_SCFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						IDLE_MODE	
NONE						R/W	
0h						2h	

Table 14-22644. FSS_FSAS_OTFA_REGS_SCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	IDLE_MODE	R/W	2h	IDLE MODE Reset Source: rst_modg_rst_n

14.9.3.2.2.17 FSS_FSAS_OTFA_REGS_ISR Register

1 FSS_FSAS_OTFA_REGS_ISR Register (Offset = 8h) [reset = 0h]

IRQSTATUS_RAW

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Table 14-22645. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0008h

Figure 14-7485. FSS_FSAS_OTFA_REGS_ISR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 14-22647. FSS_FSAS_OTFA_REGS_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.9.3.2.2.18 FSS_FSAS_OTFA_REGS_IS Register

1 FSS_FSAS_OTFA_REGS_IS Register (Offset = Ch) [reset = 0h]

IRQSTATUS

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Table 14-22648. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 000Ch**

Figure 14-7486. FSS_FSAS_OTFA_REGS_IS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAC_ERR</td><td colspan="4">WRT_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REGION_BV</td><td colspan="4">CTR_WKV</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-22650. FSS_FSAS_OTFA_REGS_IS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.9.3.2.2.19 FSS_FSAS_OTFA_REGS_IES Register

1 FSS_FSAS_OTFA_REGS_IES Register (Offset = 10h) [reset = 0h]

IRQENABLE_SET

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Table 14-22651. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0010h**

Figure 14-7487. FSS_FSAS_OTFA_REGS_IES Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 14-22653. FSS_FSAS_OTFA_REGS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.9.3.2.2.20 FSS_FSAS_OTFA_REGS_IEC Register

1 FSS_FSAS_OTFA_REGS_IEC Register (Offset = 14h) [reset = 0h]

IRQENABLE_CLR

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Table 14-22654. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0014h

Figure 14-7488. FSS_FSAS_OTFA_REGS_IEC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 14-22656. FSS_FSAS_OTFA_REGS_IEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.9.3.2.2.21 FSS_FSAS_OTFA_REGS_CCFG Register

1 FSS_FSAS_OTFA_REGS_CCFG Register (Offset = 18h) [reset = 0h]

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Table 14-22657. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0018h**

Figure 14-7489. FSS_FSAS_OTFA_REGS_CCFG Name Register

31	30	29	28	27	26	25	24
MASTER_EN_RD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						ERROR_RESP_EN	OTFA_WAIT
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	CACHE_ENABLE	CACHE_EVICT_MODE	KEY_SIZE	RD_WRT_OPT			
NONE	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 14-22659. FSS_FSAS_OTFA_REGS_CCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MASTER_EN_RD	R/W	0h	This register controls the enabling the functionality of this IP Disabled and Bypass mode active Reset Source: rst_modg_rst_n
30:10	RESERVED	NONE	0h	Reserved
9	ERROR_RESP_EN	R/W	0h	This register controls the enabling the the ocp error response for mac errors Reset Source: rst_modg_rst_n
8	OTFA_WAIT	R/W	0h	This register allows the ability to stop accepting any new transactions from getting accepted and allow the current transactions to complete Reset Source: rst_modg_rst_n
7	RESERVED	NONE	0h	Reserved
6	CACHE_ENABLE	R/W	0h	MAC cache enable Reset Source: rst_modg_rst_n
5	CACHE_EVICT_MODE	R/W	0h	cache evict mode Reset Source: rst_modg_rst_n
4	KEY_SIZE	R/W	0h	Key Size, 0 128 Bit 1 256 Bit Reset Source: rst_modg_rst_n

Table 14-22659. FSS_FSAS_OTFA_REGS_CCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RD_WRT_OPT	R/W	0h	This register defines the static allocation of the AES cores to read transactions. The remainder will be allocated to write transactions Reset Source: rst_modg_rst_n

14.9.3.2.2.22 FSS_FSAS_OTFA_REGS_CSTATUS Register

1 FSS_FSAS_OTFA_REGS_CSTATUS Register (Offset = 1Ch) [reset = 0h]

CryptoStatus

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Table 14-22660. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 001Ch**

Figure 14-7490. FSS_FSAS_OTFA_REGS_CSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BUSY</td><td>CRYPTO_BUSY</td><td colspan="6">RD_STALL_EVENT_CNT</td></tr>
<tr><td>R</td><td>R</td><td colspan="6">R/W1TC</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_STALL_EVENT_CNT</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">WRT_STALL_EVENT_CNT</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W1TC</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WRT_STALL_EVENT_CNT</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22662. FSS_FSAS_OTFA_REGS_CSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BUSY	R	0h	0 No transactions are active, crypto or none crypto 1 One or more transactions are active, crypto or none crypto Reset Source: rst_modg_rst_n
30	CRYPTO_BUSY	R	0h	0 No transactions are active, crypto or none crypto 1 One or more transactions are active, crypto or none crypto Reset Source: rst_modg_rst_n
29:16	RD_STALL_EVENT_CNT	R/W1TC	0h	rd stall event do to lack of eng Reset Source: rst_modg_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	WRT_STALL_EVENT_CNT	R/W1TC	0h	wrt stall event do to lack of eng Reset Source: rst_modg_rst_n

14.9.3.2.2.23 FSS_FSAS_OTFA_REGS_RGCFG0 Register

1 FSS_FSAS_OTFA_REGS_RGCFG0 Register (Offset = 20h) [reset = 0h]

RegionCfg0

Return to Summary Table

Table 14-22663. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0020h

Figure 14-7491. FSS_FSAS_OTFA_REGS_RGCFG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT0	MAC_MODE0		AES_MODE0	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-22665. FSS_FSAS_OTFA_REGS_RGCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT0	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE0	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE0	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.9.3.2.2.24 FSS_FSAS_OTFA_REGS_RGMACST0 Register

1 FSS_FSAS_OTFA_REGS_RGMACST0 Register (Offset = 24h) [reset = 0h]

RegionMacStart0

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Table 14-22666. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0024h**

Figure 14-7492. FSS_FSAS_OTFA_REGS_RGMACST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START0							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START0							
R/W							
0h							

Table 14-22668. FSS_FSAS_OTFA_REGS_RGMACST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START0	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.25 FSS_FSAS_OTFA_REGS_RGST0 Register

1 FSS_FSAS_OTFA_REGS_RGST0 Register (Offset = 28h) [reset = 0h]

RegionStart0

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Table 14-22669. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0028h**

Figure 14-7493. FSS_FSAS_OTFA_REGS_RGST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START0							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START0							
R/W							
0h							

Table 14-22671. FSS_FSAS_OTFA_REGS_RGST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START0	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.26 FSS_FSAS_OTFA_REGS_RGSI0 Register

1 FSS_FSAS_OTFA_REGS_RGSI0 Register (Offset = 2Ch) [reset = 0h]

RegionSize0

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Table 14-22672. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 002Ch**

Figure 14-7494. FSS_FSAS_OTFA_REGS_RGSI0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE0							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE0							
R/W							
0h							

Table 14-22674. FSS_FSAS_OTFA_REGS_RGSI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE0	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.27 FSS_FSAS_OTFA_REGS_RKEYE00 Register

1 FSS_FSAS_OTFA_REGS_RKEYE00 Register (Offset = 30h) [reset = 0h]

RegionKeyE00

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Table 14-22675. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0030h**

Figure 14-7495. FSS_FSAS_OTFA_REGS_RKEYE00 Name Register

31	30	29	28	27	26	25	24
R_KEY_E00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E00							
R/W							
0h							

Table 14-22677. FSS_FSAS_OTFA_REGS_RKEYE00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E00	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.28 FSS_FSAS_OTFA_REGS_RKEYE01 Register

1 FSS_FSAS_OTFA_REGS_RKEYE01 Register (Offset = 34h) [reset = 0h]

RegionKeyE01

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Table 14-22678. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0034h**

Figure 14-7496. FSS_FSAS_OTFA_REGS_RKEYE01 Name Register

31	30	29	28	27	26	25	24
R_KEY_E01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E01							
R/W							
0h							

Table 14-22680. FSS_FSAS_OTFA_REGS_RKEYE01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E01	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.29 FSS_FSAS_OTFA_REGS_RKEYE02 Register

1 FSS_FSAS_OTFA_REGS_RKEYE02 Register (Offset = 38h) [reset = 0h]

RegionKeyE02

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Table 14-22681. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0038h**

Figure 14-7497. FSS_FSAS_OTFA_REGS_RKEYE02 Name Register

31	30	29	28	27	26	25	24
R_KEY_E02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E02							
R/W							
0h							

Table 14-22683. FSS_FSAS_OTFA_REGS_RKEYE02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E02	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.30 FSS_FSAS_OTFA_REGS_RKEYE03 Register

1 FSS_FSAS_OTFA_REGS_RKEYE03 Register (Offset = 3Ch) [reset = 0h]

RegionKeyE03

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Table 14-22684. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 003Ch**

Figure 14-7498. FSS_FSAS_OTFA_REGS_RKEYE03 Name Register

31	30	29	28	27	26	25	24
R_KEY_E03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E03							
R/W							
0h							

Table 14-22686. FSS_FSAS_OTFA_REGS_RKEYE03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E03	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.31 FSS_FSAS_OTFA_REGS_RKEYE04 Register

1 FSS_FSAS_OTFA_REGS_RKEYE04 Register (Offset = 40h) [reset = 0h]

RegionKeyE04

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Table 14-22687. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0040h**

Figure 14-7499. FSS_FSAS_OTFA_REGS_RKEYE04 Name Register

31	30	29	28	27	26	25	24
R_KEY_E04							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E04							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E04							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E04							
R/W							
0h							

Table 14-22689. FSS_FSAS_OTFA_REGS_RKEYE04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E04	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.32 FSS_FSAS_OTFA_REGS_RKEYE05 Register

1 FSS_FSAS_OTFA_REGS_RKEYE05 Register (Offset = 44h) [reset = 0h]

RegionKeyE05

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Table 14-22690. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0044h**

Figure 14-7500. FSS_FSAS_OTFA_REGS_RKEYE05 Name Register

31	30	29	28	27	26	25	24
R_KEY_E05							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E05							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E05							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E05							
R/W							
0h							

Table 14-22692. FSS_FSAS_OTFA_REGS_RKEYE05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E05	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.33 FSS_FSAS_OTFA_REGS_RKEYE06 Register

1 FSS_FSAS_OTFA_REGS_RKEYE06 Register (Offset = 48h) [reset = 0h]

RegionKeyE06

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Table 14-22693. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0048h**

Figure 14-7501. FSS_FSAS_OTFA_REGS_RKEYE06 Name Register

31	30	29	28	27	26	25	24
R_KEY_E06							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E06							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E06							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E06							
R/W							
0h							

Table 14-22695. FSS_FSAS_OTFA_REGS_RKEYE06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E06	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.34 FSS_FSAS_OTFA_REGS_RKEYE07 Register

1 FSS_FSAS_OTFA_REGS_RKEYE07 Register (Offset = 4Ch) [reset = 0h]

RegionKeyE07

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Table 14-22696. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 004Ch**

Figure 14-7502. FSS_FSAS_OTFA_REGS_RKEYE07 Name Register

31	30	29	28	27	26	25	24
R_KEY_E07							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E07							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E07							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E07							
R/W							
0h							

Table 14-22698. FSS_FSAS_OTFA_REGS_RKEYE07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E07	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.35 FSS_FSAS_OTFA_REGS_RKEYEP00 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP00 Register (Offset = 50h) [reset = 0h]

RegionKeyEP00

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Table 14-22699. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0050h**

Figure 14-7503. FSS_FSAS_OTFA_REGS_RKEYEP00 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP00							
R/W							
0h							

Table 14-22701. FSS_FSAS_OTFA_REGS_RKEYEP00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP00	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.36 FSS_FSAS_OTFA_REGS_RKEYEP01 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP01 Register (Offset = 54h) [reset = 0h]

RegionKeyEP01

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Table 14-22702. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0054h**

Figure 14-7504. FSS_FSAS_OTFA_REGS_RKEYEP01 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP01							
R/W							
0h							

Table 14-22704. FSS_FSAS_OTFA_REGS_RKEYEP01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP01	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.37 FSS_FSAS_OTFA_REGS_RKEYEP02 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP02 Register (Offset = 58h) [reset = 0h]

RegionKeyEP02

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Table 14-22705. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0058h**

Figure 14-7505. FSS_FSAS_OTFA_REGS_RKEYEP02 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP02							
R/W							
0h							

Table 14-22707. FSS_FSAS_OTFA_REGS_RKEYEP02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP02	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.38 FSS_FSAS_OTFA_REGS_RKEYEP03 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP03 Register (Offset = 5Ch) [reset = 0h]

RegionKeyEP03

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Table 14-22708. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 005Ch**

Figure 14-7506. FSS_FSAS_OTFA_REGS_RKEYEP03 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP03							
R/W							
0h							

Table 14-22710. FSS_FSAS_OTFA_REGS_RKEYEP03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP03	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.39 FSS_FSAS_OTFA_REGS_RKEYEP04 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP04 Register (Offset = 60h) [reset = 0h]

RegionKeyEP04

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Table 14-22711. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0060h**

Figure 14-7507. FSS_FSAS_OTFA_REGS_RKEYEP04 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP04							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP04							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP04							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP04							
R/W							
0h							

Table 14-22713. FSS_FSAS_OTFA_REGS_RKEYEP04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP04	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.40 FSS_FSAS_OTFA_REGS_RKEYEP05 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP05 Register (Offset = 64h) [reset = 0h]

RegionKeyEP05

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Table 14-22714. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0064h**

Figure 14-7508. FSS_FSAS_OTFA_REGS_RKEYEP05 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP05							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP05							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP05							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP05							
R/W							
0h							

Table 14-22716. FSS_FSAS_OTFA_REGS_RKEYEP05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP05	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.41 FSS_FSAS_OTFA_REGS_RKEYEP06 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP06 Register (Offset = 68h) [reset = 0h]

RegionKeyEP06

Return to Summary Table

Table 14-22717. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0068h**

Figure 14-7509. FSS_FSAS_OTFA_REGS_RKEYEP06 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP06							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP06							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP06							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP06							
R/W							
0h							

Table 14-22719. FSS_FSAS_OTFA_REGS_RKEYEP06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP06	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.42 FSS_FSAS_OTFA_REGS_RKEYEP07 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP07 Register (Offset = 6Ch) [reset = 0h]

RegionKeyEP07

Return to Summary Table

Table 14-22720. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 006Ch**

Figure 14-7510. FSS_FSAS_OTFA_REGS_RKEYEP07 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP07							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP07							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP07							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP07							
R/W							
0h							

Table 14-22722. FSS_FSAS_OTFA_REGS_RKEYEP07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP07	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.43 FSS_FSAS_OTFA_REGS_RKEYA00 Register

1 FSS_FSAS_OTFA_REGS_RKEYA00 Register (Offset = 70h) [reset = 0h]

RegionKeyA00

Return to Summary Table

Table 14-22723. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0070h

Figure 14-7511. FSS_FSAS_OTFA_REGS_RKEYA00 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_A00</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_A00</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_A00</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_A00</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22725. FSS_FSAS_OTFA_REGS_RKEYA00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A00	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.44 FSS_FSAS_OTFA_REGS_RKEYA01 Register

1 FSS_FSAS_OTFA_REGS_RKEYA01 Register (Offset = 74h) [reset = 0h]

RegionKeyA01

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Table 14-22726. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0074h**

Figure 14-7512. FSS_FSAS_OTFA_REGS_RKEYA01 Name Register

31	30	29	28	27	26	25	24
R_KEY_A01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A01							
R/W							
0h							

Table 14-22728. FSS_FSAS_OTFA_REGS_RKEYA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A01	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.45 FSS_FSAS_OTFA_REGS_RKEYA02 Register

1 FSS_FSAS_OTFA_REGS_RKEYA02 Register (Offset = 78h) [reset = 0h]

RegionKeyA02

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Table 14-22729. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0078h**

Figure 14-7513. FSS_FSAS_OTFA_REGS_RKEYA02 Name Register

31	30	29	28	27	26	25	24
R_KEY_A02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A02							
R/W							
0h							

Table 14-22731. FSS_FSAS_OTFA_REGS_RKEYA02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A02	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.46 FSS_FSAS_OTFA_REGS_RKEYA03 Register

1 FSS_FSAS_OTFA_REGS_RKEYA03 Register (Offset = 7Ch) [reset = 0h]

RegionKeyA03

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Table 14-22732. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 007Ch**

Figure 14-7514. FSS_FSAS_OTFA_REGS_RKEYA03 Name Register

31	30	29	28	27	26	25	24
R_KEY_A03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A03							
R/W							
0h							

Table 14-22734. FSS_FSAS_OTFA_REGS_RKEYA03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A03	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.47 FSS_FSAS_OTFA_REGS_RKEYAP00 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP00 Register (Offset = 80h) [reset = 0h]

RegionKeyAP00

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Table 14-22735. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0080h

Figure 14-7515. FSS_FSAS_OTFA_REGS_RKEYAP00 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP00							
R/W							
0h							

Table 14-22737. FSS_FSAS_OTFA_REGS_RKEYAP00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP00	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.48 FSS_FSAS_OTFA_REGS_RKEYAP01 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP01 Register (Offset = 84h) [reset = 0h]

RegionKeyAP01

Return to Summary Table

Table 14-22738. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0084h**

Figure 14-7516. FSS_FSAS_OTFA_REGS_RKEYAP01 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP01							
R/W							
0h							

Table 14-22740. FSS_FSAS_OTFA_REGS_RKEYAP01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP01	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.49 FSS_FSAS_OTFA_REGS_RKEYAP02 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP02 Register (Offset = 88h) [reset = 0h]

RegionKeyAP02

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Table 14-22741. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0088h**

Figure 14-7517. FSS_FSAS_OTFA_REGS_RKEYAP02 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP02							
R/W							
0h							

Table 14-22743. FSS_FSAS_OTFA_REGS_RKEYAP02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP02	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.50 FSS_FSAS_OTFA_REGS_RKEYAP03 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP03 Register (Offset = 8Ch) [reset = 0h]

RegionKeyAP03

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Table 14-22744. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 008Ch**

Figure 14-7518. FSS_FSAS_OTFA_REGS_RKEYAP03 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP03							
R/W							
0h							

Table 14-22746. FSS_FSAS_OTFA_REGS_RKEYAP03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP03	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.51 FSS_FSAS_OTFA_REGS_RIV00 Register

1 FSS_FSAS_OTFA_REGS_RIV00 Register (Offset = 90h) [reset = 0h]

RegionIV00

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Table 14-22747. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0090h**

Figure 14-7519. FSS_FSAS_OTFA_REGS_RIV00 Name Register

31	30	29	28	27	26	25	24
R_IV00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV00							
R/W							
0h							

Table 14-22749. FSS_FSAS_OTFA_REGS_RIV00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV00	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.52 FSS_FSAS_OTFA_REGS_RIV01 Register

1 FSS_FSAS_OTFA_REGS_RIV01 Register (Offset = 94h) [reset = 0h]

RegionIV01

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Table 14-22750. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0094h**

Figure 14-7520. FSS_FSAS_OTFA_REGS_RIV01 Name Register

31	30	29	28	27	26	25	24
R_IV01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV01							
R/W							
0h							

Table 14-22752. FSS_FSAS_OTFA_REGS_RIV01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV01	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.53 FSS_FSAS_OTFA_REGS_RIV02 Register

1 FSS_FSAS_OTFA_REGS_RIV02 Register (Offset = 98h) [reset = 0h]

RegionIV02

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Table 14-22753. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0098h**

Figure 14-7521. FSS_FSAS_OTFA_REGS_RIV02 Name Register

31	30	29	28	27	26	25	24
R_IV02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV02							
R/W							
0h							

Table 14-22755. FSS_FSAS_OTFA_REGS_RIV02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV02	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.54 FSS_FSAS_OTFA_REGS_RIV03 Register

1 FSS_FSAS_OTFA_REGS_RIV03 Register (Offset = 9Ch) [reset = 0h]

RegionIV03

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Table 14-22756. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 009Ch**

Figure 14-7522. FSS_FSAS_OTFA_REGS_RIV03 Name Register

31	30	29	28	27	26	25	24
R_IV03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV03							
R/W							
0h							

Table 14-22758. FSS_FSAS_OTFA_REGS_RIV03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV03	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.55 FSS_FSAS_OTFA_REGS_RGCFG1 Register

1 FSS_FSAS_OTFA_REGS_RGCFG1 Register (Offset = A0h) [reset = 0h]

RegionCfg1

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Table 14-22759. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00A0h**

Figure 14-7523. FSS_FSAS_OTFA_REGS_RGCFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			WRT_PROTECT1	MAC_MODE1		AES_MODE1	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-22761. FSS_FSAS_OTFA_REGS_RGCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT1	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE1	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE1	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.9.3.2.2.56 FSS_FSAS_OTFA_REGS_RGMACST1 Register

1 FSS_FSAS_OTFA_REGS_RGMACST1 Register (Offset = A4h) [reset = 0h]

RegionMacStart1

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Table 14-22762. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00A4h**

Figure 14-7524. FSS_FSAS_OTFA_REGS_RGMACST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START1							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START1							
R/W							
0h							

Table 14-22764. FSS_FSAS_OTFA_REGS_RGMACST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START1	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.57 FSS_FSAS_OTFA_REGS_RGST1 Register

1 FSS_FSAS_OTFA_REGS_RGST1 Register (Offset = A8h) [reset = 0h]

RegionStart1

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Table 14-22765. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 00A8h

Figure 14-7525. FSS_FSAS_OTFA_REGS_RGST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START1							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START1							
R/W							
0h							

Table 14-22767. FSS_FSAS_OTFA_REGS_RGST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START1	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.58 FSS_FSAS_OTFA_REGS_RGSI1 Register

1 FSS_FSAS_OTFA_REGS_RGSI1 Register (Offset = ACh) [reset = 0h]

RegionSize1

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Table 14-22768. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00ACh**

Figure 14-7526. FSS_FSAS_OTFA_REGS_RGSI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE1							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE1							
R/W							
0h							

Table 14-22770. FSS_FSAS_OTFA_REGS_RGSI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE1	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.59 FSS_FSAS_OTFA_REGS_RKEYE10 Register

1 FSS_FSAS_OTFA_REGS_RKEYE10 Register (Offset = B0h) [reset = 0h]

RegionKeyE10

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Table 14-22771. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00B0h**

Figure 14-7527. FSS_FSAS_OTFA_REGS_RKEYE10 Name Register

31	30	29	28	27	26	25	24
R_KEY_E10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E10							
R/W							
0h							

Table 14-22773. FSS_FSAS_OTFA_REGS_RKEYE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E10	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.60 FSS_FSAS_OTFA_REGS_RKEYE11 Register

1 FSS_FSAS_OTFA_REGS_RKEYE11 Register (Offset = B4h) [reset = 0h]

RegionKeyE11

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Table 14-22774. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00B4h**

Figure 14-7528. FSS_FSAS_OTFA_REGS_RKEYE11 Name Register

31	30	29	28	27	26	25	24
R_KEY_E11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E11							
R/W							
0h							

Table 14-22776. FSS_FSAS_OTFA_REGS_RKEYE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E11	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.61 FSS_FSAS_OTFA_REGS_RKEYE12 Register

1 FSS_FSAS_OTFA_REGS_RKEYE12 Register (Offset = B8h) [reset = 0h]

RegionKeyE12

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Table 14-22777. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00B8h**

Figure 14-7529. FSS_FSAS_OTFA_REGS_RKEYE12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_E12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_E12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_E12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_E12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22779. FSS_FSAS_OTFA_REGS_RKEYE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E12	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.62 FSS_FSAS_OTFA_REGS_RKEYE13 Register

1 FSS_FSAS_OTFA_REGS_RKEYE13 Register (Offset = BCh) [reset = 0h]

RegionKeyE13

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Table 14-22780. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00BCh**

Figure 14-7530. FSS_FSAS_OTFA_REGS_RKEYE13 Name Register

31	30	29	28	27	26	25	24
R_KEY_E13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E13							
R/W							
0h							

Table 14-22782. FSS_FSAS_OTFA_REGS_RKEYE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E13	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.63 FSS_FSAS_OTFA_REGS_RKEYE14 Register

1 FSS_FSAS_OTFA_REGS_RKEYE14 Register (Offset = C0h) [reset = 0h]

RegionKeyE14

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Table 14-22783. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00C0h**

Figure 14-7531. FSS_FSAS_OTFA_REGS_RKEYE14 Name Register

31	30	29	28	27	26	25	24
R_KEY_E14							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E14							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E14							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E14							
R/W							
0h							

Table 14-22785. FSS_FSAS_OTFA_REGS_RKEYE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E14	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.64 FSS_FSAS_OTFA_REGS_RKEYE15 Register

1 FSS_FSAS_OTFA_REGS_RKEYE15 Register (Offset = C4h) [reset = 0h]

RegionKeyE15

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Table 14-22786. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00C4h**

Figure 14-7532. FSS_FSAS_OTFA_REGS_RKEYE15 Name Register

31	30	29	28	27	26	25	24
R_KEY_E15							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E15							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E15							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E15							
R/W							
0h							

Table 14-22788. FSS_FSAS_OTFA_REGS_RKEYE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E15	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.65 FSS_FSAS_OTFA_REGS_RKEYE16 Register

1 FSS_FSAS_OTFA_REGS_RKEYE16 Register (Offset = C8h) [reset = 0h]

RegionKeyE16

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Table 14-22789. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00C8h**

Figure 14-7533. FSS_FSAS_OTFA_REGS_RKEYE16 Name Register

31	30	29	28	27	26	25	24
R_KEY_E16							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E16							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E16							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E16							
R/W							
0h							

Table 14-22791. FSS_FSAS_OTFA_REGS_RKEYE16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E16	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.66 FSS_FSAS_OTFA_REGS_RKEYE17 Register

1 FSS_FSAS_OTFA_REGS_RKEYE17 Register (Offset = CCh) [reset = 0h]

RegionKeyE17

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Table 14-22792. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00CCh**

Figure 14-7534. FSS_FSAS_OTFA_REGS_RKEYE17 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_E17</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_E17</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_E17</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_E17</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22794. FSS_FSAS_OTFA_REGS_RKEYE17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E17	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.67 FSS_FSAS_OTFA_REGS_RKEYEP10 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP10 Register (Offset = D0h) [reset = 0h]

RegionKeyEP10

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Table 14-22795. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00D0h**

Figure 14-7535. FSS_FSAS_OTFA_REGS_RKEYEP10 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP10							
R/W							
0h							

Table 14-22797. FSS_FSAS_OTFA_REGS_RKEYEP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP10	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.68 FSS_FSAS_OTFA_REGS_RKEYEP11 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP11 Register (Offset = D4h) [reset = 0h]

RegionKeyEP11

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Table 14-22798. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00D4h**

Figure 14-7536. FSS_FSAS_OTFA_REGS_RKEYEP11 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP11							
R/W							
0h							

Table 14-22800. FSS_FSAS_OTFA_REGS_RKEYEP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP11	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.69 FSS_FSAS_OTFA_REGS_RKEYEP12 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP12 Register (Offset = D8h) [reset = 0h]

RegionKeyEP12

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Table 14-22801. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00D8h**

Figure 14-7537. FSS_FSAS_OTFA_REGS_RKEYEP12 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP12							
R/W							
0h							

Table 14-22803. FSS_FSAS_OTFA_REGS_RKEYEP12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP12	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.70 FSS_FSAS_OTFA_REGS_RKEYEP13 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP13 Register (Offset = DCh) [reset = 0h]

RegionKeyEP13

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Table 14-22804. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00DCh**

Figure 14-7538. FSS_FSAS_OTFA_REGS_RKEYEP13 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP13							
R/W							
0h							

Table 14-22806. FSS_FSAS_OTFA_REGS_RKEYEP13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP13	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.71 FSS_FSAS_OTFA_REGS_RKEYEP14 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP14 Register (Offset = E0h) [reset = 0h]

RegionKeyEP14

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Table 14-22807. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 00E0h

Figure 14-7539. FSS_FSAS_OTFA_REGS_RKEYEP14 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP14							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP14							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP14							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP14							
R/W							
0h							

Table 14-22809. FSS_FSAS_OTFA_REGS_RKEYEP14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP14	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.72 FSS_FSAS_OTFA_REGS_RKEYEP15 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP15 Register (Offset = E4h) [reset = 0h]

RegionKeyEP15

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Table 14-22810. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00E4h**

Figure 14-7540. FSS_FSAS_OTFA_REGS_RKEYEP15 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP15							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP15							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP15							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP15							
R/W							
0h							

Table 14-22812. FSS_FSAS_OTFA_REGS_RKEYEP15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP15	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.73 FSS_FSAS_OTFA_REGS_RKEYEP16 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP16 Register (Offset = E8h) [reset = 0h]

RegionKeyEP16

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Table 14-22813. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00E8h**

Figure 14-7541. FSS_FSAS_OTFA_REGS_RKEYEP16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_EP16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_EP16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_EP16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_EP16</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22815. FSS_FSAS_OTFA_REGS_RKEYEP16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP16	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.74 FSS_FSAS_OTFA_REGS_RKEYEP17 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP17 Register (Offset = ECh) [reset = 0h]

RegionKeyEP17

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Table 14-22816. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00ECh**

Figure 14-7542. FSS_FSAS_OTFA_REGS_RKEYEP17 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP17							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP17							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP17							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP17							
R/W							
0h							

Table 14-22818. FSS_FSAS_OTFA_REGS_RKEYEP17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP17	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.75 FSS_FSAS_OTFA_REGS_RKEYA10 Register

1 FSS_FSAS_OTFA_REGS_RKEYA10 Register (Offset = F0h) [reset = 0h]

RegionKeyA10

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Table 14-22819. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 00F0h**

Figure 14-7543. FSS_FSAS_OTFA_REGS_RKEYA10 Name Register

31	30	29	28	27	26	25	24
R_KEY_A10							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_A10							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_A10							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_A10							
R/W							
0h							

Table 14-22821. FSS_FSAS_OTFA_REGS_RKEYA10 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	R_KEY_A10	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.76 FSS_FSAS_OTFA_REGS_RKEYA11 Register

1 FSS_FSAS_OTFA_REGS_RKEYA11 Register (Offset = F4h) [reset = 0h]

RegionKeyA11

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Table 14-22822. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00F4h**

Figure 14-7544. FSS_FSAS_OTFA_REGS_RKEYA11 Name Register

31	30	29	28	27	26	25	24
R_KEY_A11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A11							
R/W							
0h							

Table 14-22824. FSS_FSAS_OTFA_REGS_RKEYA11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A11	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.77 FSS_FSAS_OTFA_REGS_RKEYA12 Register

1 FSS_FSAS_OTFA_REGS_RKEYA12 Register (Offset = F8h) [reset = 0h]

RegionKeyA12

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Table 14-22825. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00F8h**

Figure 14-7545. FSS_FSAS_OTFA_REGS_RKEYA12 Name Register

31	30	29	28	27	26	25	24
R_KEY_A12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A12							
R/W							
0h							

Table 14-22827. FSS_FSAS_OTFA_REGS_RKEYA12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A12	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.78 FSS_FSAS_OTFA_REGS_RKEYA13 Register

1 FSS_FSAS_OTFA_REGS_RKEYA13 Register (Offset = FCh) [reset = 0h]

RegionKeyA13

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Table 14-22828. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 00FCh**

Figure 14-7546. FSS_FSAS_OTFA_REGS_RKEYA13 Name Register

31	30	29	28	27	26	25	24
R_KEY_A13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A13							
R/W							
0h							

Table 14-22830. FSS_FSAS_OTFA_REGS_RKEYA13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A13	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.79 FSS_FSAS_OTFA_REGS_RKEYAP10 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP10 Register (Offset = 100h) [reset = 0h]

RegionKeyAP10

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Table 14-22831. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0100h**

Figure 14-7547. FSS_FSAS_OTFA_REGS_RKEYAP10 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP10							
R/W							
0h							

Table 14-22833. FSS_FSAS_OTFA_REGS_RKEYAP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP10	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.80 FSS_FSAS_OTFA_REGS_RKEYAP11 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP11 Register (Offset = 104h) [reset = 0h]

RegionKeyAP11

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Table 14-22834. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0104h**

Figure 14-7548. FSS_FSAS_OTFA_REGS_RKEYAP11 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP11							
R/W							
0h							

Table 14-22836. FSS_FSAS_OTFA_REGS_RKEYAP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP11	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.81 FSS_FSAS_OTFA_REGS_RKEYAP12 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP12 Register (Offset = 108h) [reset = 0h]

RegionKeyAP12

Return to Summary Table

Table 14-22837. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0108h**

Figure 14-7549. FSS_FSAS_OTFA_REGS_RKEYAP12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_AP12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_AP12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_AP12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_AP12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22839. FSS_FSAS_OTFA_REGS_RKEYAP12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP12	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.82 FSS_FSAS_OTFA_REGS_RKEYAP13 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP13 Register (Offset = 10Ch) [reset = 0h]

RegionKeyAP13

Return to Summary Table

Table 14-22840. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 010Ch**

Figure 14-7550. FSS_FSAS_OTFA_REGS_RKEYAP13 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP13							
R/W							
0h							

Table 14-22842. FSS_FSAS_OTFA_REGS_RKEYAP13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP13	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.83 FSS_FSAS_OTFA_REGS_RIV10 Register

1 FSS_FSAS_OTFA_REGS_RIV10 Register (Offset = 110h) [reset = 0h]

RegionIV10

Return to Summary Table

Table 14-22843. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0110h**

Figure 14-7551. FSS_FSAS_OTFA_REGS_RIV10 Name Register

31	30	29	28	27	26	25	24
R_IV10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV10							
R/W							
0h							

Table 14-22845. FSS_FSAS_OTFA_REGS_RIV10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV10	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.84 FSS_FSAS_OTFA_REGS_RIV11 Register

1 FSS_FSAS_OTFA_REGS_RIV11 Register (Offset = 114h) [reset = 0h]

RegionIV11

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Table 14-22846. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0114h**

Figure 14-7552. FSS_FSAS_OTFA_REGS_RIV11 Name Register

31	30	29	28	27	26	25	24
R_IV11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV11							
R/W							
0h							

Table 14-22848. FSS_FSAS_OTFA_REGS_RIV11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV11	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.85 FSS_FSAS_OTFA_REGS_RIV12 Register

1 FSS_FSAS_OTFA_REGS_RIV12 Register (Offset = 118h) [reset = 0h]

RegionIV12

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Table 14-22849. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0118h**

Figure 14-7553. FSS_FSAS_OTFA_REGS_RIV12 Name Register

31	30	29	28	27	26	25	24
R_IV12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV12							
R/W							
0h							

Table 14-22851. FSS_FSAS_OTFA_REGS_RIV12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV12	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.86 FSS_FSAS_OTFA_REGS_RIV13 Register

1 FSS_FSAS_OTFA_REGS_RIV13 Register (Offset = 11Ch) [reset = 0h]

RegionIV13

Return to Summary Table

Table 14-22852. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 011Ch**

Figure 14-7554. FSS_FSAS_OTFA_REGS_RIV13 Name Register

31	30	29	28	27	26	25	24
R_IV13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV13							
R/W							
0h							

Table 14-22854. FSS_FSAS_OTFA_REGS_RIV13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV13	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.87 FSS_FSAS_OTFA_REGS_RGCFG2 Register

1 FSS_FSAS_OTFA_REGS_RGCFG2 Register (Offset = 120h) [reset = 0h]

RegionCfg2

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Table 14-22855. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0120h**

Figure 14-7555. FSS_FSAS_OTFA_REGS_RGCFG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT2	MAC_MODE2		AES_MODE2	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-22857. FSS_FSAS_OTFA_REGS_RGCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT2	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE2	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE2	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.9.3.2.2.88 FSS_FSAS_OTFA_REGS_RGMACST2 Register

1 FSS_FSAS_OTFA_REGS_RGMACST2 Register (Offset = 124h) [reset = 0h]

RegionMacStart2

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Table 14-22858. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0124h**

Figure 14-7556. FSS_FSAS_OTFA_REGS_RGMACST2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START2							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START2							
R/W							
0h							

Table 14-22860. FSS_FSAS_OTFA_REGS_RGMACST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START2	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.89 FSS_FSAS_OTFA_REGS_RGST2 Register

1 FSS_FSAS_OTFA_REGS_RGST2 Register (Offset = 128h) [reset = 0h]

RegionStart2

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Table 14-22861. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0128h**

Figure 14-7557. FSS_FSAS_OTFA_REGS_RGST2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">R_START2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_START2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_START2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22863. FSS_FSAS_OTFA_REGS_RGST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START2	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.90 FSS_FSAS_OTFA_REGS_RGSI2 Register

1 FSS_FSAS_OTFA_REGS_RGSI2 Register (Offset = 12Ch) [reset = 0h]

RegionSize2

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Table 14-22864. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 012Ch**

Figure 14-7558. FSS_FSAS_OTFA_REGS_RGSI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE2							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE2							
R/W							
0h							

Table 14-22866. FSS_FSAS_OTFA_REGS_RGSI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE2	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.91 FSS_FSAS_OTFA_REGS_RKEYE20 Register

1 FSS_FSAS_OTFA_REGS_RKEYE20 Register (Offset = 130h) [reset = 0h]

RegionKeyE20

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Table 14-22867. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0130h**

Figure 14-7559. FSS_FSAS_OTFA_REGS_RKEYE20 Name Register

31	30	29	28	27	26	25	24
R_KEY_E20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E20							
R/W							
0h							

Table 14-22869. FSS_FSAS_OTFA_REGS_RKEYE20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E20	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.92 FSS_FSAS_OTFA_REGS_RKEYE21 Register

1 FSS_FSAS_OTFA_REGS_RKEYE21 Register (Offset = 134h) [reset = 0h]

RegionKeyE21

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Table 14-22870. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0134h**

Figure 14-7560. FSS_FSAS_OTFA_REGS_RKEYE21 Name Register

31	30	29	28	27	26	25	24
R_KEY_E21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E21							
R/W							
0h							

Table 14-22872. FSS_FSAS_OTFA_REGS_RKEYE21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E21	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.93 FSS_FSAS_OTFA_REGS_RKEYE22 Register

1 FSS_FSAS_OTFA_REGS_RKEYE22 Register (Offset = 138h) [reset = 0h]

RegionKeyE22

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Table 14-22873. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0138h**

Figure 14-7561. FSS_FSAS_OTFA_REGS_RKEYE22 Name Register

31	30	29	28	27	26	25	24
R_KEY_E22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E22							
R/W							
0h							

Table 14-22875. FSS_FSAS_OTFA_REGS_RKEYE22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E22	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.94 FSS_FSAS_OTFA_REGS_RKEYE23 Register

1 FSS_FSAS_OTFA_REGS_RKEYE23 Register (Offset = 13Ch) [reset = 0h]

RegionKeyE23

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Table 14-22876. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 013Ch**

Figure 14-7562. FSS_FSAS_OTFA_REGS_RKEYE23 Name Register

31	30	29	28	27	26	25	24
R_KEY_E23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E23							
R/W							
0h							

Table 14-22878. FSS_FSAS_OTFA_REGS_RKEYE23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E23	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.95 FSS_FSAS_OTFA_REGS_RKEYE24 Register

1 FSS_FSAS_OTFA_REGS_RKEYE24 Register (Offset = 140h) [reset = 0h]

RegionKeyE24

Return to Summary Table

Table 14-22879. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0140h**

Figure 14-7563. FSS_FSAS_OTFA_REGS_RKEYE24 Name Register

31	30	29	28	27	26	25	24
R_KEY_E24							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E24							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E24							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E24							
R/W							
0h							

Table 14-22881. FSS_FSAS_OTFA_REGS_RKEYE24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E24	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.96 FSS_FSAS_OTFA_REGS_RKEYE25 Register

1 FSS_FSAS_OTFA_REGS_RKEYE25 Register (Offset = 144h) [reset = 0h]

RegionKeyE25

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Table 14-22882. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0144h**

Figure 14-7564. FSS_FSAS_OTFA_REGS_RKEYE25 Name Register

31	30	29	28	27	26	25	24
R_KEY_E25							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E25							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E25							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E25							
R/W							
0h							

Table 14-22884. FSS_FSAS_OTFA_REGS_RKEYE25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E25	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.97 FSS_FSAS_OTFA_REGS_RKEYE26 Register

1 FSS_FSAS_OTFA_REGS_RKEYE26 Register (Offset = 148h) [reset = 0h]

RegionKeyE26

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Table 14-22885. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0148h**

Figure 14-7565. FSS_FSAS_OTFA_REGS_RKEYE26 Name Register

31	30	29	28	27	26	25	24
R_KEY_E26							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E26							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E26							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E26							
R/W							
0h							

Table 14-22887. FSS_FSAS_OTFA_REGS_RKEYE26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E26	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.98 FSS_FSAS_OTFA_REGS_RKEYE27 Register

1 FSS_FSAS_OTFA_REGS_RKEYE27 Register (Offset = 14Ch) [reset = 0h]

RegionKeyE27

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Table 14-22888. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 014Ch**

Figure 14-7566. FSS_FSAS_OTFA_REGS_RKEYE27 Name Register

31	30	29	28	27	26	25	24
R_KEY_E27							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E27							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E27							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E27							
R/W							
0h							

Table 14-22890. FSS_FSAS_OTFA_REGS_RKEYE27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E27	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.99 FSS_FSAS_OTFA_REGS_RKEYEP20 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP20 Register (Offset = 150h) [reset = 0h]

RegionKeyEP20

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Table 14-22891. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0150h**

Figure 14-7567. FSS_FSAS_OTFA_REGS_RKEYEP20 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP20							
R/W							
0h							

Table 14-22893. FSS_FSAS_OTFA_REGS_RKEYEP20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP20	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.100 FSS_FSAS_OTFA_REGS_RKEYEP21 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP21 Register (Offset = 154h) [reset = 0h]

RegionKeyEP21

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Table 14-22894. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0154h**

Figure 14-7568. FSS_FSAS_OTFA_REGS_RKEYEP21 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP21							
R/W							
0h							

Table 14-22896. FSS_FSAS_OTFA_REGS_RKEYEP21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP21	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.101 FSS_FSAS_OTFA_REGS_RKEYEP22 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP22 Register (Offset = 158h) [reset = 0h]

RegionKeyEP22

Return to Summary Table

Table 14-22897. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0158h**

Figure 14-7569. FSS_FSAS_OTFA_REGS_RKEYEP22 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP22							
R/W							
0h							

Table 14-22899. FSS_FSAS_OTFA_REGS_RKEYEP22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP22	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.102 FSS_FSAS_OTFA_REGS_RKEYEP23 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP23 Register (Offset = 15Ch) [reset = 0h]

RegionKeyEP23

Return to Summary Table

Table 14-22900. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 015Ch**

Figure 14-7570. FSS_FSAS_OTFA_REGS_RKEYEP23 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP23							
R/W							
0h							

Table 14-22902. FSS_FSAS_OTFA_REGS_RKEYEP23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP23	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.103 FSS_FSAS_OTFA_REGS_RKEYEP24 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP24 Register (Offset = 160h) [reset = 0h]

RegionKeyEP24

Return to Summary Table

Table 14-22903. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0160h**

Figure 14-7571. FSS_FSAS_OTFA_REGS_RKEYEP24 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP24							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP24							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP24							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP24							
R/W							
0h							

Table 14-22905. FSS_FSAS_OTFA_REGS_RKEYEP24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP24	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.104 FSS_FSAS_OTFA_REGS_RKEYEP25 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP25 Register (Offset = 164h) [reset = 0h]

RegionKeyEP25

Return to Summary Table

Table 14-22906. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0164h

Figure 14-7572. FSS_FSAS_OTFA_REGS_RKEYEP25 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP25							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP25							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP25							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP25							
R/W							
0h							

Table 14-22908. FSS_FSAS_OTFA_REGS_RKEYEP25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP25	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.105 FSS_FSAS_OTFA_REGS_RKEYEP26 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP26 Register (Offset = 168h) [reset = 0h]

RegionKeyEP26

Return to Summary Table

Table 14-22909. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0168h**

Figure 14-7573. FSS_FSAS_OTFA_REGS_RKEYEP26 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP26							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP26							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP26							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP26							
R/W							
0h							

Table 14-22911. FSS_FSAS_OTFA_REGS_RKEYEP26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP26	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.106 FSS_FSAS_OTFA_REGS_RKEYEP27 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP27 Register (Offset = 16Ch) [reset = 0h]

RegionKeyEP27

Return to Summary Table

Table 14-22912. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 016Ch**

Figure 14-7574. FSS_FSAS_OTFA_REGS_RKEYEP27 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP27							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP27							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP27							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP27							
R/W							
0h							

Table 14-22914. FSS_FSAS_OTFA_REGS_RKEYEP27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP27	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.107 FSS_FSAS_OTFA_REGS_RKEYA20 Register

1 FSS_FSAS_OTFA_REGS_RKEYA20 Register (Offset = 170h) [reset = 0h]

RegionKeyA20

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Table 14-22915. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0170h**

Figure 14-7575. FSS_FSAS_OTFA_REGS_RKEYA20 Name Register

31	30	29	28	27	26	25	24
R_KEY_A20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A20							
R/W							
0h							

Table 14-22917. FSS_FSAS_OTFA_REGS_RKEYA20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A20	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.108 FSS_FSAS_OTFA_REGS_RKEYA21 Register

1 FSS_FSAS_OTFA_REGS_RKEYA21 Register (Offset = 174h) [reset = 0h]

RegionKeyA21

Return to Summary Table

Table 14-22918. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0174h**

Figure 14-7576. FSS_FSAS_OTFA_REGS_RKEYA21 Name Register

31	30	29	28	27	26	25	24
R_KEY_A21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A21							
R/W							
0h							

Table 14-22920. FSS_FSAS_OTFA_REGS_RKEYA21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A21	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.109 FSS_FSAS_OTFA_REGS_RKEYA22 Register

1 FSS_FSAS_OTFA_REGS_RKEYA22 Register (Offset = 178h) [reset = 0h]

RegionKeyA22

Return to Summary Table

Table 14-22921. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0178h**

Figure 14-7577. FSS_FSAS_OTFA_REGS_RKEYA22 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_A22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_A22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_A22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_A22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22923. FSS_FSAS_OTFA_REGS_RKEYA22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A22	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.110 FSS_FSAS_OTFA_REGS_RKEYA23 Register

1 FSS_FSAS_OTFA_REGS_RKEYA23 Register (Offset = 17Ch) [reset = 0h]

RegionKeyA23

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Table 14-22924. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 017Ch**

Figure 14-7578. FSS_FSAS_OTFA_REGS_RKEYA23 Name Register

31	30	29	28	27	26	25	24
R_KEY_A23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A23							
R/W							
0h							

Table 14-22926. FSS_FSAS_OTFA_REGS_RKEYA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A23	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.111 FSS_FSAS_OTFA_REGS_RKEYAP20 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP20 Register (Offset = 180h) [reset = 0h]

RegionKeyAP20

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Table 14-22927. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0180h**

Figure 14-7579. FSS_FSAS_OTFA_REGS_RKEYAP20 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP20							
R/W							
0h							

Table 14-22929. FSS_FSAS_OTFA_REGS_RKEYAP20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP20	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.112 FSS_FSAS_OTFA_REGS_RKEYAP21 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP21 Register (Offset = 184h) [reset = 0h]

RegionKeyAP21

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Table 14-22930. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0184h**

Figure 14-7580. FSS_FSAS_OTFA_REGS_RKEYAP21 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP21							
R/W							
0h							

Table 14-22932. FSS_FSAS_OTFA_REGS_RKEYAP21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP21	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.113 FSS_FSAS_OTFA_REGS_RKEYAP22 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP22 Register (Offset = 188h) [reset = 0h]

RegionKeyAP22

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Table 14-22933. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0188h**

Figure 14-7581. FSS_FSAS_OTFA_REGS_RKEYAP22 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP22							
R/W							
0h							

Table 14-22935. FSS_FSAS_OTFA_REGS_RKEYAP22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP22	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.114 FSS_FSAS_OTFA_REGS_RKEYAP23 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP23 Register (Offset = 18Ch) [reset = 0h]

RegionKeyAP23

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Table 14-22936. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 018Ch**

Figure 14-7582. FSS_FSAS_OTFA_REGS_RKEYAP23 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP23							
R/W							
0h							

Table 14-22938. FSS_FSAS_OTFA_REGS_RKEYAP23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP23	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.115 FSS_FSAS_OTFA_REGS_RIV20 Register

1 FSS_FSAS_OTFA_REGS_RIV20 Register (Offset = 190h) [reset = 0h]

RegionIV20

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Table 14-22939. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0190h**

Figure 14-7583. FSS_FSAS_OTFA_REGS_RIV20 Name Register

31	30	29	28	27	26	25	24
R_IV20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV20							
R/W							
0h							

Table 14-22941. FSS_FSAS_OTFA_REGS_RIV20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV20	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.116 FSS_FSAS_OTFA_REGS_RIV21 Register

1 FSS_FSAS_OTFA_REGS_RIV21 Register (Offset = 194h) [reset = 0h]

RegionIV21

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Table 14-22942. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0194h**

Figure 14-7584. FSS_FSAS_OTFA_REGS_RIV21 Name Register

31	30	29	28	27	26	25	24
R_IV21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV21							
R/W							
0h							

Table 14-22944. FSS_FSAS_OTFA_REGS_RIV21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV21	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.117 FSS_FSAS_OTFA_REGS_RIV22 Register

1 FSS_FSAS_OTFA_REGS_RIV22 Register (Offset = 198h) [reset = 0h]

RegionIV22

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Table 14-22945. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0198h**

Figure 14-7585. FSS_FSAS_OTFA_REGS_RIV22 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_IV22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_IV22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_IV22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_IV22</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22947. FSS_FSAS_OTFA_REGS_RIV22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV22	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.118 FSS_FSAS_OTFA_REGS_RIV23 Register

1 FSS_FSAS_OTFA_REGS_RIV23 Register (Offset = 19Ch) [reset = 0h]

RegionIV23

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Table 14-22948. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 019Ch**

Figure 14-7586. FSS_FSAS_OTFA_REGS_RIV23 Name Register

31	30	29	28	27	26	25	24
R_IV23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV23							
R/W							
0h							

Table 14-22950. FSS_FSAS_OTFA_REGS_RIV23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV23	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.119 FSS_FSAS_OTFA_REGS_RGCFG3 Register

1 FSS_FSAS_OTFA_REGS_RGCFG3 Register (Offset = 1A0h) [reset = 0h]

RegionCfg3

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Table 14-22951. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01A0h**

Figure 14-7587. FSS_FSAS_OTFA_REGS_RGCFG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT3	MAC_MODE3		AES_MODE3	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-22953. FSS_FSAS_OTFA_REGS_RGCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT3	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE3	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE3	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.9.3.2.2.120 FSS_FSAS_OTFA_REGS_RGMACST3 Register

1 FSS_FSAS_OTFA_REGS_RGMACST3 Register (Offset = 1A4h) [reset = 0h]

RegionMacStart3

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Table 14-22954. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01A4h**

Figure 14-7588. FSS_FSAS_OTFA_REGS_RGMACST3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START3							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START3							
R/W							
0h							

Table 14-22956. FSS_FSAS_OTFA_REGS_RGMACST3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START3	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.121 FSS_FSAS_OTFA_REGS_RGST3 Register

1 FSS_FSAS_OTFA_REGS_RGST3 Register (Offset = 1A8h) [reset = 0h]

RegionStart3

Return to Summary Table

Table 14-22957. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01A8h**

Figure 14-7589. FSS_FSAS_OTFA_REGS_RGST3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START3							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START3							
R/W							
0h							

Table 14-22959. FSS_FSAS_OTFA_REGS_RGST3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START3	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.122 FSS_FSAS_OTFA_REGS_RGSI3 Register

1 FSS_FSAS_OTFA_REGS_RGSI3 Register (Offset = 1ACh) [reset = 0h]

RegionSize3

Return to Summary Table

Table 14-22960. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01ACh**

Figure 14-7590. FSS_FSAS_OTFA_REGS_RGSI3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R_SIZE3			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_SIZE3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_SIZE3							
R/W							
0h							

Table 14-22962. FSS_FSAS_OTFA_REGS_RGSI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE3	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.9.3.2.2.123 FSS_FSAS_OTFA_REGS_RKEYE30 Register

1 FSS_FSAS_OTFA_REGS_RKEYE30 Register (Offset = 1B0h) [reset = 0h]

RegionKeyE30

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Table 14-22963. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 01B0h

Figure 14-7591. FSS_FSAS_OTFA_REGS_RKEYE30 Name Register

31	30	29	28	27	26	25	24
R_KEY_E30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E30							
R/W							
0h							

Table 14-22965. FSS_FSAS_OTFA_REGS_RKEYE30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E30	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.124 FSS_FSAS_OTFA_REGS_RKEYE31 Register

1 FSS_FSAS_OTFA_REGS_RKEYE31 Register (Offset = 1B4h) [reset = 0h]

RegionKeyE31

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Table 14-22966. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01B4h**

Figure 14-7592. FSS_FSAS_OTFA_REGS_RKEYE31 Name Register

31	30	29	28	27	26	25	24
R_KEY_E31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E31							
R/W							
0h							

Table 14-22968. FSS_FSAS_OTFA_REGS_RKEYE31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E31	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.125 FSS_FSAS_OTFA_REGS_RKEYE32 Register

1 FSS_FSAS_OTFA_REGS_RKEYE32 Register (Offset = 1B8h) [reset = 0h]

RegionKeyE32

Return to Summary Table

Table 14-22969. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01B8h**

Figure 14-7593. FSS_FSAS_OTFA_REGS_RKEYE32 Name Register

31	30	29	28	27	26	25	24
R_KEY_E32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E32							
R/W							
0h							

Table 14-22971. FSS_FSAS_OTFA_REGS_RKEYE32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E32	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.126 FSS_FSAS_OTFA_REGS_RKEYE33 Register

1 FSS_FSAS_OTFA_REGS_RKEYE33 Register (Offset = 1BCh) [reset = 0h]

RegionKeyE33

Return to Summary Table

Table 14-22972. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01BCh**

Figure 14-7594. FSS_FSAS_OTFA_REGS_RKEYE33 Name Register

31	30	29	28	27	26	25	24
R_KEY_E33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E33							
R/W							
0h							

Table 14-22974. FSS_FSAS_OTFA_REGS_RKEYE33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E33	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.127 FSS_FSAS_OTFA_REGS_RKEYE34 Register

1 FSS_FSAS_OTFA_REGS_RKEYE34 Register (Offset = 1C0h) [reset = 0h]

RegionKeyE34

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Table 14-22975. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01C0h**

Figure 14-7595. FSS_FSAS_OTFA_REGS_RKEYE34 Name Register

31	30	29	28	27	26	25	24
R_KEY_E34							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E34							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E34							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E34							
R/W							
0h							

Table 14-22977. FSS_FSAS_OTFA_REGS_RKEYE34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E34	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.128 FSS_FSAS_OTFA_REGS_RKEYE35 Register

1 FSS_FSAS_OTFA_REGS_RKEYE35 Register (Offset = 1C4h) [reset = 0h]

RegionKeyE35

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Table 14-22978. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01C4h**

Figure 14-7596. FSS_FSAS_OTFA_REGS_RKEYE35 Name Register

31	30	29	28	27	26	25	24
R_KEY_E35							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E35							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E35							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E35							
R/W							
0h							

Table 14-22980. FSS_FSAS_OTFA_REGS_RKEYE35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E35	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.129 FSS_FSAS_OTFA_REGS_RKEYE36 Register

1 FSS_FSAS_OTFA_REGS_RKEYE36 Register (Offset = 1C8h) [reset = 0h]

RegionKeyE36

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Table 14-22981. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01C8h**

Figure 14-7597. FSS_FSAS_OTFA_REGS_RKEYE36 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_E36</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_E36</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_E36</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_E36</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22983. FSS_FSAS_OTFA_REGS_RKEYE36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E36	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.130 FSS_FSAS_OTFA_REGS_RKEYE37 Register

1 FSS_FSAS_OTFA_REGS_RKEYE37 Register (Offset = 1CCh) [reset = 0h]

RegionKeyE37

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Table 14-22984. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01CCh**

Figure 14-7598. FSS_FSAS_OTFA_REGS_RKEYE37 Name Register

31	30	29	28	27	26	25	24
R_KEY_E37							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E37							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E37							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E37							
R/W							
0h							

Table 14-22986. FSS_FSAS_OTFA_REGS_RKEYE37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E37	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.9.3.2.2.131 FSS_FSAS_OTFA_REGS_RKEYEP30 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP30 Register (Offset = 1D0h) [reset = 0h]

RegionKeyEP30

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Table 14-22987. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01D0h**

Figure 14-7599. FSS_FSAS_OTFA_REGS_RKEYEP30 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP30							
R/W							
0h							

Table 14-22989. FSS_FSAS_OTFA_REGS_RKEYEP30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP30	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.132 FSS_FSAS_OTFA_REGS_RKEYEP31 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP31 Register (Offset = 1D4h) [reset = 0h]

RegionKeyEP31

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Table 14-22990. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01D4h**

Figure 14-7600. FSS_FSAS_OTFA_REGS_RKEYEP31 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP31							
R/W							
0h							

Table 14-22992. FSS_FSAS_OTFA_REGS_RKEYEP31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP31	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.133 FSS_FSAS_OTFA_REGS_RKEYEP32 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP32 Register (Offset = 1D8h) [reset = 0h]

RegionKeyEP32

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Table 14-22993. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01D8h**

Figure 14-7601. FSS_FSAS_OTFA_REGS_RKEYEP32 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP32							
R/W							
0h							

Table 14-22995. FSS_FSAS_OTFA_REGS_RKEYEP32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP32	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.134 FSS_FSAS_OTFA_REGS_RKEYEP33 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP33 Register (Offset = 1DCh) [reset = 0h]

RegionKeyEP33

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Table 14-22996. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01DCh**

Figure 14-7602. FSS_FSAS_OTFA_REGS_RKEYEP33 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_EP33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_EP33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_EP33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_EP33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-22998. FSS_FSAS_OTFA_REGS_RKEYEP33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP33	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.135 FSS_FSAS_OTFA_REGS_RKEYEP34 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP34 Register (Offset = 1E0h) [reset = 0h]

RegionKeyEP34

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Table 14-22999. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01E0h**

Figure 14-7603. FSS_FSAS_OTFA_REGS_RKEYEP34 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP34							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP34							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP34							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP34							
R/W							
0h							

Table 14-23001. FSS_FSAS_OTFA_REGS_RKEYEP34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP34	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.136 FSS_FSAS_OTFA_REGS_RKEYEP35 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP35 Register (Offset = 1E4h) [reset = 0h]

RegionKeyEP35

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Table 14-23002. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01E4h**

Figure 14-7604. FSS_FSAS_OTFA_REGS_RKEYEP35 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP35							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP35							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP35							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP35							
R/W							
0h							

Table 14-23004. FSS_FSAS_OTFA_REGS_RKEYEP35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP35	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.137 FSS_FSAS_OTFA_REGS_RKEYEP36 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP36 Register (Offset = 1E8h) [reset = 0h]

RegionKeyEP36

Return to Summary Table

Table 14-23005. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 01E8h

Figure 14-7605. FSS_FSAS_OTFA_REGS_RKEYEP36 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP36							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP36							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP36							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP36							
R/W							
0h							

Table 14-23007. FSS_FSAS_OTFA_REGS_RKEYEP36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP36	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.138 FSS_FSAS_OTFA_REGS_RKEYEP37 Register

1 FSS_FSAS_OTFA_REGS_RKEYEP37 Register (Offset = 1ECh) [reset = 0h]

RegionKeyEP37

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Table 14-23008. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01ECh**

Figure 14-7606. FSS_FSAS_OTFA_REGS_RKEYEP37 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP37							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP37							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP37							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP37							
R/W							
0h							

Table 14-23010. FSS_FSAS_OTFA_REGS_RKEYEP37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP37	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.9.3.2.2.139 FSS_FSAS_OTFA_REGS_RKEYA30 Register

1 FSS_FSAS_OTFA_REGS_RKEYA30 Register (Offset = 1F0h) [reset = 0h]

RegionKeyA30

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Table 14-23011. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 01F0h

Figure 14-7607. FSS_FSAS_OTFA_REGS_RKEYA30 Name Register

31	30	29	28	27	26	25	24
R_KEY_A30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A30							
R/W							
0h							

Table 14-23013. FSS_FSAS_OTFA_REGS_RKEYA30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A30	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.140 FSS_FSAS_OTFA_REGS_RKEYA31 Register

1 FSS_FSAS_OTFA_REGS_RKEYA31 Register (Offset = 1F4h) [reset = 0h]

RegionKeyA31

Return to Summary Table

Table 14-23014. Instance Table

Instance Name	**Physical Address**
FSS0_FSAS_0	**0FC2 01F4h**

Figure 14-7608. FSS_FSAS_OTFA_REGS_RKEYA31 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_A31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_A31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_A31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_A31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23016. FSS_FSAS_OTFA_REGS_RKEYA31 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	R_KEY_A31	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.141 FSS_FSAS_OTFA_REGS_RKEYA32 Register

1 FSS_FSAS_OTFA_REGS_RKEYA32 Register (Offset = 1F8h) [reset = 0h]

RegionKeyA32

Return to Summary Table

Table 14-23017. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 01F8h**

Figure 14-7609. FSS_FSAS_OTFA_REGS_RKEYA32 Name Register

31	30	29	28	27	26	25	24
R_KEY_A32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A32							
R/W							
0h							

Table 14-23019. FSS_FSAS_OTFA_REGS_RKEYA32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A32	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.142 FSS_FSAS_OTFA_REGS_RKEYA33 Register

1 FSS_FSAS_OTFA_REGS_RKEYA33 Register (Offset = 1FCh) [reset = 0h]

RegionKeyA33

Return to Summary Table

Table 14-23020. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 01FCh

Figure 14-7610. FSS_FSAS_OTFA_REGS_RKEYA33 Name Register

31	30	29	28	27	26	25	24
R_KEY_A33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A33							
R/W							
0h							

Table 14-23022. FSS_FSAS_OTFA_REGS_RKEYA33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A33	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.9.3.2.2.143 FSS_FSAS_OTFA_REGS_RKEYAP30 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP30 Register (Offset = 200h) [reset = 0h]

RegionKeyAP30

Return to Summary Table

Table 14-23023. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0200h**

Figure 14-7611. FSS_FSAS_OTFA_REGS_RKEYAP30 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP30							
R/W							
0h							

Table 14-23025. FSS_FSAS_OTFA_REGS_RKEYAP30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP30	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.144 FSS_FSAS_OTFA_REGS_RKEYAP31 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP31 Register (Offset = 204h) [reset = 0h]

RegionKeyAP31

Return to Summary Table

Table 14-23026. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0204h**

Figure 14-7612. FSS_FSAS_OTFA_REGS_RKEYAP31 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP31							
R/W							
0h							

Table 14-23028. FSS_FSAS_OTFA_REGS_RKEYAP31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP31	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.145 FSS_FSAS_OTFA_REGS_RKEYAP32 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP32 Register (Offset = 208h) [reset = 0h]

RegionKeyAP32

Return to Summary Table

Table 14-23029. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0208h**

Figure 14-7613. FSS_FSAS_OTFA_REGS_RKEYAP32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_AP32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_AP32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_AP32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_AP32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23031. FSS_FSAS_OTFA_REGS_RKEYAP32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP32	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.146 FSS_FSAS_OTFA_REGS_RKEYAP33 Register

1 FSS_FSAS_OTFA_REGS_RKEYAP33 Register (Offset = 20Ch) [reset = 0h]

RegionKeyAP33

Return to Summary Table

Table 14-23032. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 020Ch**

Figure 14-7614. FSS_FSAS_OTFA_REGS_RKEYAP33 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP33							
R/W							
0h							

Table 14-23034. FSS_FSAS_OTFA_REGS_RKEYAP33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP33	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.9.3.2.2.147 FSS_FSAS_OTFA_REGS_RIV30 Register

1 FSS_FSAS_OTFA_REGS_RIV30 Register (Offset = 210h) [reset = 0h]

RegionIV30

Return to Summary Table

Table 14-23035. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0210h**

Figure 14-7615. FSS_FSAS_OTFA_REGS_RIV30 Name Register

31	30	29	28	27	26	25	24
R_IV30							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_IV30							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_IV30							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_IV30							
R/W							
0h							

Table 14-23037. FSS_FSAS_OTFA_REGS_RIV30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV30	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.148 FSS_FSAS_OTFA_REGS_RIV31 Register

1 FSS_FSAS_OTFA_REGS_RIV31 Register (Offset = 214h) [reset = 0h]

RegionIV31

Return to Summary Table

Table 14-23038. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0214h**

Figure 14-7616. FSS_FSAS_OTFA_REGS_RIV31 Name Register

31	30	29	28	27	26	25	24
R_IV31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV31							
R/W							
0h							

Table 14-23040. FSS_FSAS_OTFA_REGS_RIV31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV31	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.149 FSS_FSAS_OTFA_REGS_RIV32 Register

1 FSS_FSAS_OTFA_REGS_RIV32 Register (Offset = 218h) [reset = 0h]

RegionIV32

Return to Summary Table

Table 14-23041. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0218h**

Figure 14-7617. FSS_FSAS_OTFA_REGS_RIV32 Name Register

31	30	29	28	27	26	25	24
R_IV32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV32							
R/W							
0h							

Table 14-23043. FSS_FSAS_OTFA_REGS_RIV32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV32	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.150 FSS_FSAS_OTFA_REGS_RIV33 Register

1 FSS_FSAS_OTFA_REGS_RIV33 Register (Offset = 21Ch) [reset = 0h]

RegionIV33

Return to Summary Table

Table 14-23044. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 021Ch**

Figure 14-7618. FSS_FSAS_OTFA_REGS_RIV33 Name Register

31	30	29	28	27	26	25	24
R_IV33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV33							
R/W							
0h							

Table 14-23046. FSS_FSAS_OTFA_REGS_RIV33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV33	R/W	0h	IV Reset Source: rst_modg_rst_n

14.9.3.2.2.151 FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register

1 FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register (Offset = 220h) [reset = 0h]

IRQAdditionalInfo0

Return to Summary Table

Table 14-23047. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 0220h

Figure 14-7619. FSS_FSAS_OTFA_REGS_IRQADDINFO0 Name Register

31	30	29	28	27	26	25	24
IRQ_MADDR							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_MADDR							
R							
0h							
15	14	13	12	11	10	9	8
IRQ_MADDR							
R							
0h							
7	6	5	4	3	2	1	0
IRQ_MADDR							
R							
0h							

Table 14-23049. FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IRQ_MADDR	R	0h	Initiator Address which caused the event Reset Source: rst_modg_rst_n

14.9.3.2.2.152 FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register

1 FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register (Offset = 224h) [reset = 0h]

IRQAdditionalInfo1

Return to Summary Table

Table 14-23050. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0224h**

Figure 14-7620. FSS_FSAS_OTFA_REGS_IRQADDINFO1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						IRQ_MLEN	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
IRQ_MLEN		IRQ_MSEQ			IRQ_MCMD		
R		R			R		
0h		0h			0h		
7	6	5	4	3	2	1	0
IRQ_MID							
R							
0h							

Table 14-23052. FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:14	IRQ_MLEN	R	0h	Initiator LENGTH which caused the event Reset Source: rst_modg_rst_n
13:11	IRQ_MSEQ	R	0h	Initiator SEQ which caused the event Reset Source: rst_modg_rst_n
10:8	IRQ_MCMD	R	0h	Initiator CMD which caused the event Reset Source: rst_modg_rst_n
7:0	IRQ_MID	R	0h	Initiator TAG ID which caused the event Reset Source: rst_modg_rst_n

14.9.3.2.2.153 FSS_FSAS_OTFA_REGS_MACCACHEINFO Register

1 FSS_FSAS_OTFA_REGS_MACCACHEINFO Register (Offset = 228h) [reset = 0h]

MACCacheInfo

Return to Summary Table

Table 14-23053. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0FC2 0228h**

Figure 14-7621. FSS_FSAS_OTFA_REGS_MACCACHEINFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CACHE_MISS_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
CACHE_MISS_EVENT_CNT							
R							
0h							

Table 14-23055. FSS_FSAS_OTFA_REGS_MACCACHEINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CACHE_MISS_EVENT_CNT	R	0h	MAC Cache Miss event cnt Reset Source: rst_modg_rst_n

14.9.3.2.2.154 FSS_FSAS_OTFA_REGS_RMWRMCNT Register

1 FSS_FSAS_OTFA_REGS_RMWRMCNT Register (Offset = 22Ch) [reset = 0h]

RMWRMCnt

Return to Summary Table

Table 14-23056. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	0FC2 022Ch

Figure 14-7622. FSS_FSAS_OTFA_REGS_RMWRMCNT Name Register

31	30	29	28	27	26	25	24
RM_EVENT_CNT							
R							
0h							
23	22	21	20	19	18	17	16
RM_EVENT_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RMW_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
RMW_EVENT_CNT							
R							
0h							

Table 14-23058. FSS_FSAS_OTFA_REGS_RMWRMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RM_EVENT_CNT	R	0h	RM event cnt Reset Source: rst_modg_rst_n
15:0	RMW_EVENT_CNT	R	0h	RMW event cnt Reset Source: rst_modg_rst_n

14.9.3.2.2.155 FSS_DAT_REG1_HPB_DATA_MEM_j Register

1 FSS_DAT_REG1_HPB_DATA_MEM_j Register (Offset = 0h + formula) [reset = 0h]

FSAS boot data region1

Return to Summary Table

Offset = (j * 4h); where j = 0 to 134217727d

Table 14-23059. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**6000 0000h + formula**

Figure 14-7623. FSS_DAT_REG1_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-23061. FSS_DAT_REG1_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1 Reset Source: rst_mod_g_rst_n

14.9.3.2.2.156 FSS_DAT_REG0_HPB_DATA_MEM_j Register

1 FSS_DAT_REG0_HPB_DATA_MEM_j Register (Offset = 0h + formula) [reset = 0h]

FSAS data region0

Return to Summary Table

Offset = (j * 4h); where j = 0 to 4294967295d

Table 14-23062. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0004 0000 0000h + formula**

Figure 14-7624. FSS_DAT_REG0_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-23064. FSS_DAT_REG0_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region0 Reset Source: rst_mod_g_rst_n

14.9.3.2.2.157 FSS_DAT_REG3_HPB_DATA_MEM_j Register

1 FSS_DAT_REG3_HPB_DATA_MEM_j Register (Offset = 0h + formula) [reset = 0h]

FSAS bypass data region3

Return to Summary Table

Offset = (j * 4h); where j = 0 to 4294967295d

Table 14-23065. Instance Table

Instance Name	Physical Address
FSS0_FSAS_0	**0005 0000 0000h + formula**

Figure 14-7625. FSS_DAT_REG3_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-23067. FSS_DAT_REG3_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1 Reset Source: rst_mod_g_rst_n

14.9.3.3 FSS_OSPI_0

FSS_OSPI_0

14.9.3.3.1 FSS_OSPI_0 Summaries

FSS_OSPI_0 Summaries

Table 14-23068. ECC_AGGR Registers, Base Address=0071 6000h, Length=1024

Offset	Length	Register Name	FSS0_OSPI_0 Physical Address
0h	32	ECC_AGGR_REV	0071 6000h
8h	32	ECC_AGGR_VECTOR	0071 6008h
Ch	32	ECC_AGGR_STAT	0071 600Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 6010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 603Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 6040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 6080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 60C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 613Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 6140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 6180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 61C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 6200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 6204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 6208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 620Ch

Table 14-23069. OSPI_FLASH_CFG Registers, Base Address=0FC4 0000h, Length=256

Offset	Length	Register Name	FSS0_OSPI_0 Physical Address
0h	32	OSPI_FLASH_CFG_CONFIG_REG	0FC4 0000h
4h	32	OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG	0FC4 0004h
8h	32	OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG	0FC4 0008h
Ch	32	OSPI_FLASH_CFG_DEV_DELAY_REG	0FC4 000Ch
10h	32	OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG	0FC4 0010h
14h	32	OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG	0FC4 0014h
18h	32	OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG	0FC4 0018h
1Ch	32	OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG	0FC4 001Ch
20h	32	OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG	0FC4 0020h
24h	32	OSPI_FLASH_CFG_REMAP_ADDR_REG	0FC4 0024h
28h	32	OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG	0FC4 0028h
2Ch	32	OSPI_FLASH_CFG_SRAM_FILL_REG	0FC4 002Ch
30h	32	OSPI_FLASH_CFG_TX_THRESH_REG	0FC4 0030h
34h	32	OSPI_FLASH_CFG_RX_THRESH_REG	0FC4 0034h
38h	32	OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG	0FC4 0038h
3Ch	32	OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG	0FC4 003Ch
40h	32	OSPI_FLASH_CFG_IRQ_STATUS_REG	0FC4 0040h
44h	32	OSPI_FLASH_CFG_IRQ_MASK_REG	0FC4 0044h

Table 14-23069. OSPI_FLASH_CFG Registers, Base Address=0FC4 0000h, Length=256 (continued)

Offset	Length	Register Name	FSS0_OSPI_0 Physical Address
50h	32	OSPI_FLASH_CFG_LOWER_WR_PROT_REG	0FC4 0050h
54h	32	OSPI_FLASH_CFG_UPPER_WR_PROT_REG	0FC4 0054h
58h	32	OSPI_FLASH_CFG_WR_PROT_CTRL_REG	0FC4 0058h
60h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG	0FC4 0060h
64h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG	0FC4 0064h
68h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG	0FC4 0068h
6Ch	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG	0FC4 006Ch
70h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG	0FC4 0070h
74h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG	0FC4 0074h
78h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG	0FC4 0078h
7Ch	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG	0FC4 007Ch
80h	32	OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG	0FC4 0080h
8Ch	32	OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG	0FC4 008Ch
90h	32	OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG	0FC4 0090h
94h	32	OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG	0FC4 0094h
A0h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG	0FC4 00A0h
A4h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG	0FC4 00A4h
A8h	32	OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG	0FC4 00A8h
ACh	32	OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG	0FC4 00ACh
B0h	32	OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG	0FC4 00B0h
B4h	32	OSPI_FLASH_CFG_PHY_CONFIGURATION_REG	0FC4 00B4h
B8h	32	OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG	0FC4 00B8h
BCh	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG	0FC4 00BCh
C0h	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG	0FC4 00C0h
E0h	32	OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG	0FC4 00E0h
E4h	32	OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG	0FC4 00E4h
FCh	32	OSPI_FLASH_CFG_MODULE_ID_REG	0FC4 00FCh

Table 14-23070. OSPI_CFG Registers, Base Address=0FC4 4000h, Length=512

Offset	Length	Register Name	FSS0_OSPI_0 Physical Address
0h	32	OSPI_CFG_PID	0FC4 4000h
4h	32	OSPI_CFG_CTRL	0FC4 4004h
8h	32	OSPI_CFG_STAT	0FC4 4008h
20h	32	OSPI_CFG_EOI	0FC4 4020h

14.9.3.3.2 FSS_OSPI_0 Registers

FSS_OSPI_0 Registers

14.9.3.3.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

Revision parameters

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Table 14-23071. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6000h**

Figure 14-7626. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
1Dh					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-23073. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	1Dh	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

14.9.3.3.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-23074. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6008h**

Figure 14-7627. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-23076. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.3.3.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-23077. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 600Ch**

Figure 14-7628. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-23079. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.3.3.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = (j * 4h); where j = 0 to 7d

Table 14-23080. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6010h + formula**

Figure 14-7629. ECC_AGGR_RESERVED_SVBUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23082. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.3.3.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-23083. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 603Ch**

Figure 14-7630. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-23085. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.3.3.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-23086. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6040h**

Figure 14-7631. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 14-23088. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.9.3.3.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-23089. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6080h**

Figure 14-7632. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-23091. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.9.3.3.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-23092. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 60C0h**

Figure 14-7633. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-23094. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.9.3.3.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-23095. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 613Ch**

Figure 14-7634. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-23097. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.3.3.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-23098. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6140h**

Figure 14-7635. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 14-23100. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.9.3.3.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-23101. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6180h**

Figure 14-7636. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-23103. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.9.3.3.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-23104. Instance Table

Instance Name	**Physical Address**
FSS0_OSPI_0	**0071 61C0h**

Figure 14-7637. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SRAM_ENABLE_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-23106. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.9.3.3.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-23107. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6200h**

Figure 14-7638. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-23109. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.3.3.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-23110. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6204h**

Figure 14-7639. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-23112. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.3.3.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-23113. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 6208h**

Figure 14-7640. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-23115. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.3.3.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-23116. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0071 620Ch**

Figure 14-7641. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-23118. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.9.3.3.2.17 OSPI_FLASH_CFG_CONFIG_REG Register

1 OSPI_FLASH_CFG_CONFIG_REG Register (Offset = 0h) [reset = 80780081h]

Octal-SPI Configuration Register

Return to Summary Table

Table 14-23119. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0000h**

Figure 14-7642. OSPI_FLASH_CFG_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
IDLE_FLD	DUAL_BYTE_OPCODE_EN_FLD	CRC_ENABLE_FLD	CONFIG_RESV2_FLD			PIPELINE_PHY_FLD	ENABLE_DTR_PROTOCOL_FLD
R	R/W	R/W	R			R/W	R/W
1h	0h	0h	0h			0h	0h
23	22	21	20	19	18	17	16
ENABLE_AHB_DECODER_FLD	MSTR_BAUD_DIV_FLD				ENTER_XIP_MODE_IMM_FLD	ENTER_XIP_MODE_FLD	ENB_AHB_ADDR_REMAP_FLD
R/W	R/W				R/W	R/W	R/W
0h	Fh				0h	0h	0h
15	14	13	12	11	10	9	8
ENB_DMA_IF_FLD	WR_PROT_FLASH_FLD	PERIPH_CS_LINES_FLD				PERIPH_SEL_DEC_FLD	ENB_LEGACY_IP_MODE_FLD
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h
7	6	5	4	3	2	1	0
ENB_DIR_ACC_CTLR_FLD	RESET_CFG_FLD	RESET_PIN_FLD	HOLD_PIN_FLD	PHY_MODE_ENABLE_FLD	SEL_CLK_PHASE_FLD	SEL_CLK_POL_FLD	ENB_SPI_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	1h

Table 14-23121. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE_FLD	R	1h	Serial interface and low level SPI pipeline is IDLE: This is a STATUS read-only bit. Note this is a retimed signal, so there will be some inherent delay on the generation of this status signal.
30	DUAL_BYTE_OPCODE_EN_FLD	R/W	0h	Dual-byte Opcode Mode enable bit This bit is to be set in case the target Flash Device supports dual byte opcode [i.e. Macronix MX25]. It is applicable for Octal I/O Mode or Protocol only so should be set back to low if the device is configured to work in another SPI Mode. If enabled, the supplementing bytes are taken from Opcode Extension Register [Lower] and from Opcode Extension Register [Upper].
29	CRC_ENABLE_FLD	R/W	0h	CRC enable bit This bit is to be set in case the target Flash Device supports CRC [Macronix MX25]. It is applicable for Octal DDR Protocol only so should be set back to low if the device is configured to work in another SPI Mode.
28:26	CONFIG_RESV2_FLD	R	0h	Reserved
25	PIPELINE_PHY_FLD	R/W	0h	Pipeline PHY Mode enable: This bit is relevant only for configuration with PHY Module. It should be asserted to 1 between consecutive PHY pipeline reads transfers and de-asserted to 0 otherwise.

Table 14-23121. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	ENABLE_DTR_PROTOCOL_FLD	R/W	0h	Enable DTR Protocol: This bit should be set if device is configured to work in DTR protocol.
23	ENABLE_AHB_DECODER_FLD	R/W	0h	Enable AHB Decoder: Value=0 : Active target is selected based on Peripheral Chip Select Lines [bits [13:10]]. Value=1 Active target is selected based on actual AHB address [the partition for each device is calculated with respect to bits [28:21] of Device Size Configuration Register]
22:19	MSTR_BAUD_DIV_FLD	R/W	Fh	Initiator Mode Baud Rate Divisor: SPI baud rate = [initiator reference clock] baud_rate_divisor
18	ENTER_XIP_MODE_IMM_FLD	R/W	0h	Enter XIP Mode immediately: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : Operate the device in XIP mode immediately Use this register when the external device wakes up in XIP mode [as per the contents of its non- volatile configuration register]. The controller will assume the next READ instruction will be passed to the device as an XIP instruction, and therefore will not require the READ opcode to be transferred. Note: To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only after the next READ instruction is executed. Software therefore should ensure that at least one READ instruction is requested after resetting this bit in order to be sure that XIP mode is exited.
17	ENTER_XIP_MODE_FLD	R/W	0h	Enter XIP Mode on next READ: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : If XIP is disabled, then setting to ?1? will inform the controller that the device is ready to enter XIP on the next READ instruction. The controller will therefore send the appropriate command sequence, including mode bits to cause the device to enter XIP mode. Use this register after the controller has ensured the FLASH device has been configured to be ready to enter XIP mode. Note : To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only AFTER the next READ instruction is executed. Software should therefore ensure that at least one READ instruction is requested after resetting this bit before it can be sure XIP mode in the device is exited.
16	ENB_AHB_ADDR_REMAP_FLD	R/W	0h	Enable AHB Address Re-mapping: [Direct Access Mode Only] When set to 1, the incoming AHB address will be adapted and sent to the FLASH device as [address + N], where N is the value stored in the remap address register.
15	ENB_DMA_IF_FLD	R/W	0h	Enable DMA Peripheral Interface: Set to 1 to enable the DMA handshaking logic. When enabled the controller will trigger DMA transfer requests via the DMA peripheral interface. Set to 0 to disable
14	WR_PROT_FLASH_FLD	R/W	0h	Write Protect Flash Pin: Set to drive the Write Protect pin of the FLASH device. This is resynchronized to the generated memory clock as necessary.
13:10	PERIPH_CS_LINES_FLD	R/W	0h	Peripheral Chip Select Lines: Peripheral chip select lines If pdec = 0, ss[3:0] are output thus: ss[3:0] n_ss_out[3:0] xxx0 1110 xx01 1101 x011 1011 0111 0111 1111 1111 [no peripheral selected] else ss[3:0] directly drives n_ss_out[3:0]
9	PERIPH_SEL_DEC_FLD	R/W	0h	Peripheral select decode: 0 : only 1 of 4 selects n_ss_out[3:0] is active 1 : allow external 4-to-16 decode [n_ss_out = ss]
8	ENB_LEGACY_IP_MODE_FLD	R/W	0h	Legacy IP Mode Enable: 0 : Use Direct Access Controller/Indirect Access Controller 1 : legacy Mode is enabled. In this mode, any write to the controller via the AHB interface is serialized and sent to the FLASH device. Any valid AHB read will pop the internal RX-FIFO, retrieving data that was forwarded by the external FLASH device on the SPI lines,4,2 or 1 byte transfers are permitted and controlled via the HSIZE input.

Table 14-23121. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ENB_DIR_ACC_CTLR_FLD	R/W	1h	Enable Direct Access Controller: 0 : disable the Direct Access Controller once current transfer of the data word [FF_W] is complete. 1 : enable the Direct Access Controller When the Direct Access Controller and Indirect Access Controller are both disabled, all AHB requested are completed with an error response.
6	RESET_CFG_FLD	R/W	0h	RESET pin configuration: 0 = RESET feature on DQ3 pin of the device 1 = RESET feature on dedicated pin of the device [controlling of 5th bit influences on reset_out output]
5	RESET_PIN_FLD	R/W	0h	Set to drive the RESET pin of the FLASH device and reset for de-activation of the RESET pin feature
4	HOLD_PIN_FLD	R/W	0h	Set to drive the HOLD pin of the FLASH device and reset for de-activation of the HOLD pin feature
3	PHY_MODE_ENABLE_FLD	R/W	0h	PHY mode enable: When enabled, the controller is informed that PHY Module is to be used for handling SPI transfers. This bit is relevant only for configuration with PHY Module.
2	SEL_CLK_PHASE_FLD	R/W	0h	Select Clock Phase: Selects whether the clock is in an active or inactive phase outside the SPI word. 0 : the SPI clock is active outside the word 1 : the SPI clock is inactive outside the word
1	SEL_CLK_POL_FLD	R/W	0h	Clock polarity outside SPI word: 0 : the SPI clock is quiescent low 1 : the SPI clock is quiescent high
0	ENB_SPI_FLD	R/W	1h	Octal-SPI Enable: 0 : disable the Octal-SPI, once current transfer of the data word [FF_W] is complete. 1 : enable the Octal-SPI, when spi_enable = 0, all output enables are inactive and all pins are set to input mode.

14.9.3.3.2.18 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register

1 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register (Offset = 4h) [reset = 3h]

Device Read Instruction Configuration Register

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Table 14-23122. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 0004h

Figure 14-7643. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RD_INSTR_RESV5_FLD			DUMMY_RD_CLK_CYCLES_FLD				
R			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_INSTR_RESV4_FLD			MODE_BIT_ENABLE_FLD	RD_INSTR_RESV3_FLD		DATA_XFER_TYPE_EXT_MODE_FLD	
R			R/W	R		R/W	
0h			0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_INSTR_RESV2_FLD		ADDR_XFER_TYPE_STD_MODE_FLD		RD_INSTR_RESV1_FLD	DDR_EN_FLD	INSTR_TYPE_FLD	
R		R/W		R	R/W	R/W	
0h		0h		0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RD_OPCODE_NON_XIP_FLD							
R/W							
3h							

Table 14-23124. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RD_INSTR_RESV5_FLD	R	0h	Reserved
28:24	DUMMY_RD_CLK_CYCLES_FLD	R/W	0h	Dummy Read Clock Cycles: Number of dummy clock cycles required by device for read instruction.
23:21	RD_INSTR_RESV4_FLD	R	0h	Reserved
20	MODE_BIT_ENABLE_FLD	R/W	0h	Mode Bit Enable: Set this field to 1 to ensure that the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
19:18	RD_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	RD_INSTR_RESV2_FLD	R	0h	Reserved

Table 14-23124. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11	RD_INSTR_RESV1_FLD	R	0h	Reserved
10	DDR_EN_FLD	R/W	0h	DDR Enable: This is to inform that opcode from rd_opcode_non_xip_fld is compliant with one of the DDR READ Commands
9:8	INSTR_TYPE_FLD	R/W	0h	Instruction Type: 0 : Use Standard SPI mode [instruction always shifted into the device on DQ0 only] 1 : Use DIO-SPI mode [Instructions, Address and Data always sent on DQ0 and DQ1] 2 : Use QIO-SPI mode [Instructions, Address and Data always sent on DQ0, DQ1, DQ2 and DQ3] 3 : Use Octal-IO-SPI mode [Instructions, Address and Data always sent on DQ[7:0]]
7:0	RD_OPCODE_NON_XIP_FLD	R/W	3h	Read Opcode in non-XIP mode: Read Opcode to use when not in XIP mode

14.9.3.3.2.19 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register

1 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register (Offset = 8h) [reset = 2h]

Device Write Instruction Configuration Register

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Table 14-23125. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0008h**

Figure 14-7644. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
WR_INSTR_RESV4_FLD			DUMMY_WR_CLK_CYCLES_FLD				
R			R/W				
0h			0h				

23	22	21	20	19	18	17	16
WR_INSTR_RESV3_FLD						DATA_XFER_TYPE_EXT_MODE_FLD	
R						R/W	
0h						0h	

15	14	13	12	11	10	9	8
WR_INSTR_RESV2_FLD		ADDR_XFER_TYPE_STD_MODE_FLD		WR_INSTR_RESV1_FLD			WEL_DIS_FLD
R		R/W		R			R/W
0h		0h		0h			0h

7	6	5	4	3	2	1	0
WR_OPCODE_FLD							
R/W							
2h							

Table 14-23127. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	WR_INSTR_RESV4_FLD	R	0h	Reserved
28:24	DUMMY_WR_CLK_CYCLES_FLD	R/W	0h	Dummy Write Clock Cycles: Number of dummy clock cycles required by device for write instruction.
23:18	WR_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	WR_INSTR_RESV2_FLD	R	0h	Reserved
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11:9	WR_INSTR_RESV1_FLD	R	0h	Reserved
8	WEL_DIS_FLD	R/W	0h	WEL Disable: This is to turn off automatic issuing of WEL Command before write operation for DAC or INDAC

Table 14-23127. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	WR_OPCODE_FLD	R/W	2h	Write Opcode

14.9.3.3.2.20 OSPI_FLASH_CFG_DEV_DELAY_REG Register

1 OSPI_FLASH_CFG_DEV_DELAY_REG Register (Offset = Ch) [reset = 0h]

Octal-SPI Device Delay Register: This register is used to introduce relative delays into the generation of the initiator output signals. All timings are defined in cycles of the SPI REFERENCE CLOCK/ext_clk, defined in this table as SPI initiator ref clock.

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Table 14-23128. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 000Ch**

Figure 14-7645. OSPI_FLASH_CFG_DEV_DELAY_REG Name Register

31	30	29	28	27	26	25	24
D_NSS_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
D_BTWN_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
D_AFTER_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
D_INIT_FLD							
R/W							
0h							

Table 14-23130. OSPI_FLASH_CFG_DEV_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	D_NSS_FLD	R/W	0h	Clock Delay for Chip Select Deassert: Delay in initiator reference clocks for the length that the initiator mode chip select outputs are de-asserted between transactions. The minimum delay is always SCLK period to ensure the chip select is never re-asserted within an SCLK period.
23:16	D_BTWN_FLD	R/W	0h	Clock Delay for Chip Select Deactivation: Delay in initiator reference clocks between one chip select being de-activated and the activation of another. This is used to ensure a quiet period between the selection of two different targets and requires the transmit FIFO to be empty.
15:8	D_AFTER_FLD	R/W	0h	Clock Delay for Last Transaction Bit: Delay in initiator reference clocks between last bit of current transaction and deasserting the device chip select [n_ss_out]. By default, the chip select will be deasserted on the cycle following the completion of the current transaction.
7:0	D_INIT_FLD	R/W	0h	Clock Delay with n_ss_out: Delay in initiator reference clocks between setting n_ss_out low and first bit transfer.

14.9.3.3.2.21 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register

1 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register (Offset = 10h) [reset = 1h]

Read Data Capture Register

Return to Summary Table

Table 14-23131. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0010h**

Figure 14-7646. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RD_DATA_RESV3_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RD_DATA_RESV3_FLD</td><td colspan="4">DDR_READ_DELAY_FLD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RD_DATA_RESV2_FLD</td><td>DQS_ENABLE_FLD</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RD_DATA_RESV1_FLD</td><td>SAMPLE_EDGE_SEL_FLD</td><td colspan="4">DELAY_FLD</td><td>BYPASS_FLD</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>1h</td></tr>
</table>

Table 14-23133. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RD_DATA_RESV3_FLD	R	0h	Reserved
19:16	DDR_READ_DELAY_FLD	R/W	0h	DDR read delay: Delay the transmitted data by the programmed number of ref_clk cycles.This field is only relevant when DDR Read Command is executed. Otherwise can be ignored.
15:9	RD_DATA_RESV2_FLD	R	0h	Reserved
8	DQS_ENABLE_FLD	R/W	0h	DQS enable bit: If enabled, signal from DQS input is driven into RX DLL and is used for data capturing in PHY Mode rather than internally generated gated ref_clk..
7:6	RD_DATA_RESV1_FLD	R	0h	Reserved
5	SAMPLE_EDGE_SEL_FLD	R/W	0h	Sample edge selection: Choose edge on which data outputs from flash memory will be sampled
4:1	DELAY_FLD	R/W	0h	Read Delay: Delay the read data capturing logic by the programmed number of ref_clk cycles
0	BYPASS_FLD	R/W	1h	Bypass the adapted loopback clock circuit

14.9.3.3.2.22 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register

1 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register (Offset = 14h) [reset = 101002h]

Device Size Configuration Register

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Table 14-23134. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0014h**

Figure 14-7647. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DEV_SIZE_RESV_FLD			MEM_SIZE_ON_CS3_FLD		MEM_SIZE_ON_CS2_FLD		MEM_SIZE_ON_CS1_FLD
R			R/W		R/W		R/W
0h			0h		0h		0h
23	22	21	20	19	18	17	16
MEM_SIZE_ON_CS1_FLD	MEM_SIZE_ON_CS0_FLD		BYTES_PER_SUBSECTOR_FLD				
R/W	R/W		R/W				
0h	0h		10h				
15	14	13	12	11	10	9	8
BYTES_PER_DEVICE_PAGE_FLD							
R/W							
100h							
7	6	5	4	3	2	1	0
BYTES_PER_DEVICE_PAGE_FLD				NUM_ADDR_BYTES_FLD			
R/W				R/W			
100h				2h			

Table 14-23136. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	DEV_SIZE_RESV_FLD	R	0h	Reserved
28:27	MEM_SIZE_ON_CS3_FLD	R/W	0h	Size of Flash Device connected to CS[3] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
26:25	MEM_SIZE_ON_CS2_FLD	R/W	0h	Size of Flash Device connected to CS[2] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
24:23	MEM_SIZE_ON_CS1_FLD	R/W	0h	Size of Flash Device connected to CS[1] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
22:21	MEM_SIZE_ON_CS0_FLD	R/W	0h	Size of Flash Device connected to CS[0] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
20:16	BYTES_PER_SUBSECTOR_FLD	R/W	10h	Number of bytes per Block. This is required by the controller for performing the write protection logic. The number of bytes per block must be a power of 2 number.
15:4	BYTES_PER_DEVICE_PAGE_FLD	R/W	100h	Number of bytes per device page. This is required by the controller for performing FLASH writes up to and across page boundaries.
3:0	NUM_ADDR_BYTES_FLD	R/W	2h	Number of address bytes. A value of 0 indicates 1 byte.

14.9.3.3.2.23 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register

1 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register (Offset = 18h) [reset = 80h]

SRAM Partition Configuration Register

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Table 14-23137. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0018h**

Figure 14-7648. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Name Register

31	30	29	28	27	26	25	24
SRAM_PARTITION_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_PARTITION_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_PARTITION_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
80h							

Table 14-23139. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	SRAM_PARTITION_RESV_FLD	R	0h	Reserved
7:0	ADDR_FLD	R/W	80h	Indirect Read Partition Size: Defines the size of the indirect read partition in the SRAM, in units of SRAM locations. By default, half of the SRAM is reserved for indirect read operation, and half for indirect write. The size of this register will scale with the depth of the SRAM.

14.9.3.3.2.24 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register

1 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register (Offset = 1Ch) [reset = 0h]

Indirect AHB Address Trigger Register

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Table 14-23140. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 001Ch

Figure 14-7649. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-23142. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the base address that will be used by the AHB controller. When the incoming AHB read access address matches a range of addresses from this trigger address to the trigger address + 15, then the AHB request will be completed by fetching data from the Indirect Controllers SRAM.

14.9.3.3.2.25 OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register

1 OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register (Offset = 20h) [reset = 0h]

DMA Peripheral Configuration Register

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Table 14-23143. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0020h**

Figure 14-7650. OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DMA_PERIPH_RESV2_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DMA_PERIPH_RESV2_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMA_PERIPH_RESV2_FLD				NUM_BURST_REQ_BYTES_FLD			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DMA_PERIPH_RESV1_FLD				NUM_SINGLE_REQ_BYTES_FLD			
R				R/W			
0h				0h			

Table 14-23145. OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	DMA_PERIPH_RESV2_FLD	R	0h	Reserved
11:8	NUM_BURST_REQ_BYTES_FLD	R/W	0h	Number of Burst Bytes: Number of bytes in a burst type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.
7:4	DMA_PERIPH_RESV1_FLD	R	0h	Reserved
3:0	NUM_SINGLE_REQ_BYTES_FLD	R/W	0h	Number of Single Bytes: Number of bytes in a single type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.

14.9.3.3.2.26 OSPI_FLASH_CFG_REMAP_ADDR_REG Register

1 OSPI_FLASH_CFG_REMAP_ADDR_REG Register (Offset = 24h) [reset = 0h]

Remap Address Register

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Table 14-23146. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0024h**

Figure 14-7651. OSPI_FLASH_CFG_REMAP_ADDR_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-23148. OSPI_FLASH_CFG_REMAP_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This register is used to remap an incoming AHB address to a different address used by the FLASH device.

14.9.3.3.2.27 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register

1 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register (Offset = 28h) [reset = 200h]

Mode Bit Configuration Register

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Table 14-23149. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0028h**

Figure 14-7652. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RX_CRC_DATA_LOW_FLD							
R							
0h							
23	22	21	20	19	18	17	16
RX_CRC_DATA_UP_FLD							
R							
0h							
15	14	13	12	11	10	9	8
CRC_OUT_ENABLE_FLD	MODE_BIT_RESV1_FLD				CHUNK_SIZE_FLD		
R/W	R				R/W		
0h	0h				2h		
7	6	5	4	3	2	1	0
MODE_FLD							
R/W							
0h							

Table 14-23151. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RX_CRC_DATA_LOW_FLD	R	0h	RX CRC data [lower] The first CRC byte returned after RX data chunk.
23:16	RX_CRC_DATA_UP_FLD	R	0h	RX CRC data [upper] The second CRC byte returned after RX data chunk.
15	CRC_OUT_ENABLE_FLD	R/W	0h	CRC# output enable bit When enabled, the controller expects the Flash Device to toggle CRC data on both SPI clock edges in CRC->CRC# sequence and calculates CRC compliance accordingly.
14:11	MODE_BIT_RESV1_FLD	R	0h	Reserved
10:8	CHUNK_SIZE_FLD	R/W	2h	It defines size of chunk after which CRC data is expected to show up on the SPI interface for write and read data transfers.
7:0	MODE_FLD	R/W	0h	These are the 8 mode bits that are sent to the device following the address bytes if mode bit transmission has been enabled.

14.9.3.3.2.28 OSPI_FLASH_CFG_SRAM_FILL_REG Register

1 OSPI_FLASH_CFG_SRAM_FILL_REG Register (Offset = 2Ch) [reset = 0h]

SRAM Fill Register

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Table 14-23152. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 002Ch**

Figure 14-7653. OSPI_FLASH_CFG_SRAM_FILL_REG Name Register

31	30	29	28	27	26	25	24
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_FILL_INDAC_READ_FLD							
R							
0h							
7	6	5	4	3	2	1	0
SRAM_FILL_INDAC_READ_FLD							
R							
0h							

Table 14-23154. OSPI_FLASH_CFG_SRAM_FILL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SRAM_FILL_INDAC_WRITE_FLD	R	0h	SRAM Fill Level [Indirect Write Partition]: Identifies the current fill level of the SRAM Indirect Write partition
15:0	SRAM_FILL_INDAC_READ_FLD	R	0h	SRAM Fill Level [Indirect Read Partition]: Identifies the current fill level of the SRAM Indirect Read partition

14.9.3.3.2.29 OSPI_FLASH_CFG_TX_THRESH_REG Register

1 OSPI_FLASH_CFG_TX_THRESH_REG Register (Offset = 30h) [reset = 1h]

TX Threshold Register

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Table 14-23155. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 0030h

Figure 14-7654. OSPI_FLASH_CFG_TX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
TX_THRESH_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
TX_THRESH_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
TX_THRESH_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
TX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 14-23157. OSPI_FLASH_CFG_TX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	TX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small TX FIFO not full interrupt is generated

14.9.3.3.2.30 OSPI_FLASH_CFG_RX_THRESH_REG Register

1 OSPI_FLASH_CFG_RX_THRESH_REG Register (Offset = 34h) [reset = 1h]

RX Threshold Register

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Table 14-23158. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0034h**

Figure 14-7655. OSPI_FLASH_CFG_RX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
RX_THRESH_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
RX_THRESH_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
RX_THRESH_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
RX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 14-23160. OSPI_FLASH_CFG_RX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small RX FIFO not empty interrupt is generated

14.9.3.3.2.31 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register

1 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register (Offset = 38h) [reset = 10005h]

Write Completion Control Register: This register defines how the controller will poll the device following a write transfer

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Table 14-23161. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0038h**

Figure 14-7656. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Name Register

31	30	29	28	27	26	25	24
POLL_REP_DELAY_FLD							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
POLL_COUNT_FLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENABLE_POLLING_EXP_FLD	DISABLE_POLLING_FLD	POLLING_POLARITY_FLD	WR_COMP_CTRL_RESV1_FLD		POLLING_BIT_INDEX_FLD		
R/W	R/W	R/W	R		R/W		
0h	0h	0h	0h		0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OPCODE_FLD							
R/W							
5h							

Table 14-23163. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	POLL_REP_DELAY_FLD	R/W	0h	Defines additional delay for maintain Chip Select de-asserted during auto-polling phase
23:16	POLL_COUNT_FLD	R/W	1h	Defines the number of times the controller should expect to see a true result from the polling in successive reads of the device register.
15	ENABLE_POLLING_EXP_FLD	R/W	0h	Set to '1' for enabling auto-polling expiration.
14	DISABLE_POLLING_FLD	R/W	0h	This switches off the automatic polling function
13	POLLING_POLARITY_FLD	R/W	0h	Defines the polling polarity. If '1', then the write transfer to the device will be complete if the polled bit is equal to '1'. If '0', then the write transfer to the device will be complete if the polled bit is equal to '0'.
12:11	WR_COMP_CTRL_RESV1_FLD	R	0h	Reserved
10:8	POLLING_BIT_INDEX_FLD	R/W	0h	Defines the bit index that should be polled. A value of 010 means that bit 2 of the returned data will be polled for.A value of 111 means that bit 7 of the returned data will be polled for.
7:0	OPCODE_FLD	R/W	5h	Defines the opcode that should be issued by the controller when it is automatically polling for device program completion. This command is issued followed all device write operations. By default, this will poll the standard device STATUS register using opcode 0x05

14.9.3.3.2.32 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register

1 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register (Offset = 3Ch) [reset = FFFFFFFFh]

Polling Expiration Register

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Table 14-23164. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 003Ch**

Figure 14-7657. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Name Register

31	30	29	28	27	26	25	24
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							

Table 14-23166. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NO_OF_POLLS_BEF_EXP_FLD	R/W	FFFFFFFFh	Number of polls cycles before expiration

14.9.3.3.2.33 OSPI_FLASH_CFG_IRQ_STATUS_REG Register

1 OSPI_FLASH_CFG_IRQ_STATUS_REG Register (Offset = 40h) [reset = 0h]

Interrupt Status Register: The status fields in this register are set when the described event occurs and the interrupt is enabled in the mask register. When any of these bit fields are set, the interrupt output is asserted high. The fields are each cleared by writing a 1 to the field. Note that bit fields 6 thru 10 are only valid when legacy SPI mode is active.

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Table 14-23167. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0040h**

Figure 14-7658. OSPI_FLASH_CFG_IRQ_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IRQ_STAT_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_STAT_RESV_FLD				ECC_FAIL_FLD	TX_CRC_CHUNK_BRK_FLD	RX_CRC_DATA_VAL_FLD	RX_CRC_DATA_ERR_FLD
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_STAT_RESV1_FLD	STIG_REQ_INT_FLD	POLL_EXP_INT_FLD	INDRD_SRAM_FULL_FLD	RX_FIFO_FULL_FLD	RX_FIFO_NOT_EMPTY_FLD	TX_FIFO_FULL_FLD	TX_FIFO_NOT_FULL_FLD
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_FLD	INDIRECT_XFER_LEVEL_BREACH_FLD	ILLEGAL_ACCESS_DET_FLD	PROT_WR_ATTEMPT_FLD	INDIRECT_READ_REJECT_FLD	INDIRECT_OP_DONE_FLD	UNDERFLOW_DET_FLD	MODE_M_FAIL_FLD
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-23169. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_STAT_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_FLD	R/W1TC	0h	ECC failure This interrupt informs the system that Flash Device reported ECC error.
18	TX_CRC_CHUNK_BRK_FLD	R/W1TC	0h	TX CRC chunk was broken This interrupt informs the system that program page SPI transfer was discontinued somewhere inside the chunk.
17	RX_CRC_DATA_VAL_FLD	R/W1TC	0h	RX CRC data valid New RX CRC data was captured from Flash Device
16	RX_CRC_DATA_ERR_FLD	R/W1TC	0h	RX CRC data error CRC data from Flash Device does not correspond to the one dynamically calculated by the controller.
15	IRQ_STAT_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_INT_FLD	R/W1TC	0h	The controller is ready for getting another STIG request.
13	POLL_EXP_INT_FLD	R/W1TC	0h	The maximum number of programmed polls cycles is expired
12	INDRD_SRAM_FULL_FLD	R/W1TC	0h	Indirect Read Partition overflow: Indirect Read Partition of SRAM is full and unable to immediately complete indirect operation

Table 14-23169. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_FIFO_FULL_FLD	R/W1TC	0h	Small RX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full 1 : FIFO is full
10	RX_FIFO_NOT_EMPTY_FLD	R/W1TC	0h	Small RX FIFO not empty: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has less than RX THRESHOLD entries, 1 : FIFO has >= THRESHOLD entries
9	TX_FIFO_FULL_FLD	R/W1TC	0h	Small TX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full, 1 : FIFO is full
8	TX_FIFO_NOT_FULL_FLD	R/W1TC	0h	Small TX FIFO not full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has >= THRESHOLD entries, 1 : FIFO has less than THRESHOLD entries
7	RECV_OVERFLOW_FLD	R/W1TC	0h	Receive Overflow: This should only occur in Legacy SPI mode. Set if an attempt is made to push the RX FIFO when it is full. This bit is reset only by a system reset and cleared only when this register is read. If a new push to the RX FIFO occurs coincident with a register read this flag will remain set. 0 : no overflow has been detected. 1 : an overflow has occurred.
6	INDIRECT_XFER_LEVEL_BREACH_FLD	R/W1TC	0h	Indirect Transfer Watermark Level Breached
5	ILLEGAL_ACCESS_DET_FLD	R/W1TC	0h	Illegal AHB access has been detected. AHB wrapping bursts and the use of SPLIT/RETRY accesses will cause this error interrupt to trigger.
4	PROT_WR_ATTEMPT_FLD	R/W1TC	0h	Write to protected area was attempted and rejected.
3	INDIRECT_READ_REJECT_FLD	R/W1TC	0h	Indirect operation was requested but could not be accepted. Two indirect operations already in storage.
2	INDIRECT_OP_DONE_FLD	R/W1TC	0h	Indirect Operation Complete: Controller has completed last triggered indirect operation
1	UNDERFLOW_DET_FLD	R/W1TC	0h	Underflow Detected: 0 : no underflow has been detected 1 : underflow is detected and an attempt to transfer data is made when the small TX FIFO is empty. This may occur when AHB write data is being supplied too slowly to keep up with the requested write operation This bit is reset only by a system reset and cleared only when the register is read.
0	MODE_M_FAIL_FLD	R/W1TC	0h	Mode M Failure: Mode M failure indicates the voltage on pin n_ss_in is inconsistent with the SPI mode. Set =1 if n_ss_in is low in initiator mode [multi-initiator contention]. These conditions will clear the spi_enable bit and disable the SPI. This bit is reset only by a system reset and cleared only when this register is read. 0 : no mode fault has been detected 1 : a mode fault has occurred

14.9.3.3.2.34 OSPI_FLASH_CFG_IRQ_MASK_REG Register

1 OSPI_FLASH_CFG_IRQ_MASK_REG Register (Offset = 44h) [reset = 0h]

Interrupt Mask: 0 : the interrupt for the corresponding interrupt status register bit is disabled. 1 : the interrupt for the corresponding interrupt status register bit is enabled.

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Table 14-23170. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 0044h

Figure 14-7659. OSPI_FLASH_CFG_IRQ_MASK_REG Name Register

31	30	29	28	27	26	25	24
IRQ_MASK_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_MASK_RESV_FLD				ECC_FAIL_MASK_FLD	TX_CRC_CHUNK_BRK_MASK_FLD	RX_CRC_DATA_VAL_MASK_FLD	RX_CRC_DATA_ERR_MASK_FLD
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_MASK_RESV1_FLD	STIG_REQ_MASK_FLD	POLL_EXP_INT_MASK_FLD	INDRD_SRAM_FULL_MASK_FLD	RX_FIFO_FULL_MASK_FLD	RX_FIFO_NOT_EMPTY_MASK_FLD	TX_FIFO_FULL_MASK_FLD	TX_FIFO_NOT_FULL_MASK_FLD
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_MASK_FLD	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	ILLEGAL_ACCESS_DET_MASK_FLD	PROT_WR_ATTEMPT_MASK_FLD	INDIRECT_READ_REJECT_MASK_FLD	INDIRECT_OP_DONE_MASK_FLD	UNDERFLOW_DET_MASK_FLD	MODE_M_FAIL_MASK_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-23172. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_MASK_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_MASK_FLD	R/W	0h	ECC failure Mask
18	TX_CRC_CHUNK_BRK_MASK_FLD	R/W	0h	TX CRC chunk was broken Mask
17	RX_CRC_DATA_VAL_MASK_FLD	R/W	0h	RX CRC data valid Mask
16	RX_CRC_DATA_ERR_MASK_FLD	R/W	0h	RX CRC data error Mask
15	IRQ_MASK_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_MASK_FLD	R/W	0h	STIG request completion Mask
13	POLL_EXP_INT_MASK_FLD	R/W	0h	Polling expiration detected Mask
12	INDRD_SRAM_FULL_MASK_FLD	R/W	0h	Indirect Read Partition overflow mask

Table 14-23172. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_FIFO_FULL_MASK_FLD	R/W	0h	Small RX FIFO full Mask
10	RX_FIFO_NOT_EMPTY_MASK_FLD	R/W	0h	Small RX FIFO not empty Mask
9	TX_FIFO_FULL_MASK_FLD	R/W	0h	Small TX FIFO full Mask
8	TX_FIFO_NOT_FULL_MASK_FLD	R/W	0h	Small TX FIFO not full Mask
7	RECV_OVERFLOW_MASK_FLD	R/W	0h	Receive Overflow Mask
6	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	R/W	0h	Transfer Watermark Breach Mask
5	ILLEGAL_ACCESS_DET_MASK_FLD	R/W	0h	Illegal Access Detected Mask
4	PROT_WR_ATTEMPT_MASK_FLD	R/W	0h	Protected Area Write Attempt Mask
3	INDIRECT_READ_REJECT_MASK_FLD	R/W	0h	Indirect Read Reject Mask
2	INDIRECT_OP_DONE_MASK_FLD	R/W	0h	Indirect Complete Mask
1	UNDERFLOW_DET_MASK_FLD	R/W	0h	Underflow Detected Mask
0	MODE_M_FAIL_MASK_FLD	R/W	0h	Mode M Failure Mask

14.9.3.3.2.35 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register

1 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register (Offset = 50h) [reset = 0h]

Lower Write Protection Register

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Table 14-23173. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0050h**

Figure 14-7660. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 14-23175. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the lower block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

14.9.3.3.2.36 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register

1 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register (Offset = 54h) [reset = 0h]

Upper Write Protection Register

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Table 14-23176. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0054h**

Figure 14-7661. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUBSECTOR_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUBSECTOR_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUBSECTOR_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUBSECTOR_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23178. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the upper block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

14.9.3.3.2.37 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register

1 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register (Offset = 58h) [reset = 0h]

Write Protection Control Register

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Table 14-23179. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0058h**

Figure 14-7662. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Name Register

31	30	29	28	27	26	25	24
WR_PROT_CTRL_RESV_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WR_PROT_CTRL_RESV_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WR_PROT_CTRL_RESV_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WR_PROT_CTRL_RESV_FLD						ENB_FLD	INV_FLD
R						R/W	R/W
0h						0h	0h

Table 14-23181. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	WR_PROT_CTRL_RESV_FLD	R	0h	Reserved
1	ENB_FLD	R/W	0h	Write Protection Enable Bit: When set to 1, any AHB write access with an address within the protection region defined in the lower and upper write protection registers is rejected. An AHB error response is generated and an interrupt source triggered. When set to 0, the protection region is disabled.
0	INV_FLD	R/W	0h	Write Protection Inversion Bit: When set to 1, the protection region defined in the lower and upper write protection registers is inverted meaning it is the region that the system is permitted to write to. When set to 0, the protection region defined in the lower and upper write protection registers is the region that the system is not permitted to write to.

14.9.3.3.2.38 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register

1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register (Offset = 60h) [reset = 0h]

Indirect Read Transfer Control Register

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Table 14-23182. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0060h**

Figure 14-7663. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_RD_XFER_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
INDIR_RD_XFER_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
INDIR_RD_XFER_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	RD_QUEUED_FLD	SRAM_FULL_FLD	RD_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R/W1TC	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 14-23184. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_RD_XFER_RESV_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	RD_QUEUED_FLD	R	0h	Two indirect read operations have been queued
3	SRAM_FULL_FLD	R/W1TC	0h	SRAM Full: SRAM full and unable to immediately complete an indirect operation. Write a 1 to this field to clear it.; indirect operation [status]
2	RD_STATUS_FLD	R	0h	Indirect Read Status: Indirect read operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Read: Writing a 1 to this bit will cancel all ongoing indirect read operations.
0	START_FLD	W	0h	Start Indirect Read: Writing a 1 to this bit will trigger an indirect read operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect read operation.

14.9.3.3.2.39 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register

1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register (Offset = 64h) [reset = 0h]

Indirect Read Transfer Watermark Register

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Table 14-23185. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0064h**

Figure 14-7664. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
0h							

Table 14-23187. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	0h	Watermark Value: This represents the minimum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level passes the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all zeroes.

14.9.3.3.2.40 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register

1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register (Offset = 68h) [reset = 0h]

Indirect Read Transfer Start Address Register

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Table 14-23188. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0068h**

Figure 14-7665. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-23190. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the start address from which the indirect access will commence its READ operation.

14.9.3.3.2.41 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register

1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register (Offset = 6Ch) [reset = 0h]

Indirect Read Transfer Number Bytes Register

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Table 14-23191. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 006Ch**

Figure 14-7666. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-23193. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.9.3.3.2.42 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register

1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register (Offset = 70h) [reset = 0h]

Indirect Write Transfer Control Register

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Table 14-23194. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 0070h

Figure 14-7667. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	WR_QUEUED_FLD	INDIR_WR_XFER_RESV1_FLD	WR_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 14-23196. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_WR_XFER_RESV2_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	WR_QUEUED_FLD	R	0h	Two indirect write operations have been queued
3	INDIR_WR_XFER_RESV1_FLD	R	0h	Reserved
2	WR_STATUS_FLD	R	0h	Indirect Write Status: Indirect write operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Write: Writing a 1 to this bit will cancel all ongoing indirect write operations.
0	START_FLD	W	0h	Start Indirect Write: Writing a 1 to this bit will trigger an indirect write operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect write operation.

14.9.3.3.2.43 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register

1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register (Offset = 74h) [reset = FFFFFFFFh]

Indirect Write Transfer Watermark Register

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Table 14-23197. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0074h**

Figure 14-7668. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
FFFFFFFFh							

Table 14-23199. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	FFFFFFFFh	Watermark Value: This represents the maximum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level falls below the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all ones.

14.9.3.3.2.44 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register

1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register (Offset = 78h) [reset = 0h]

Indirect Write Transfer Start Address Register

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Table 14-23200. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0078h**

Figure 14-7669. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-23202. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Start of Indirect Access: This is the start address from which the indirect access will commence its READ operation.

14.9.3.3.2.45 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register

1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register (Offset = 7Ch) [reset = 0h]

Indirect Write Transfer Number Bytes Register

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Table 14-23203. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 007Ch**

Figure 14-7670. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-23205. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	Indirect Number of Bytes: This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.9.3.3.2.46 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register

1 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register (Offset = 80h) [reset = 4h]

Indirect Trigger Address Range Register

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Table 14-23206. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0080h**

Figure 14-7671. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Name Register

31	30	29	28	27	26	25	24
IND_RANGE_RESV1_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IND_RANGE_RESV1_FLD							
R							
0h							
15	14	13	12	11	10	9	8
IND_RANGE_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
IND_RANGE_RESV1_FLD				IND_RANGE_WIDTH_FLD			
R				R/W			
0h				4h			

Table 14-23208. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IND_RANGE_RESV1_FLD	R	0h	Reserved
3:0	IND_RANGE_WIDTH_FLD	R/W	4h	This is the address offset of Indirect Trigger Address Register.

14.9.3.3.2.47 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register

1 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register (Offset = 8Ch) [reset = 0h]

Flash Command Control Memory Register

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Table 14-23209. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 008Ch**

Figure 14-7672. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Name Register

31	30	29	28	27	26	25	24
FLASH_COMMAND_CTRL_MEM_RESV1_FLD			MEM_BANK_ADDR_FLD				
R			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MEM_BANK_ADDR_FLD				FLASH_COMMAND_CTRL_MEM_RESV2_FLD	NB_OF_STIG_READ_BYTES_FLD		
R/W				R	R/W		
0h				0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MEM_BANK_READ_DATA_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FLASH_COMMAND_CTRL_MEM_RESV3_FLD						MEM_BANK_REQ_IN_PROGRESS_FLD	TRIGGER_MEM_BANK_REQ_FLD
R						R	W
0h						0h	0h

Table 14-23211. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	FLASH_COMMAND_CTRL_MEM_RESV1_FLD	R	0h	Reserved
28:20	MEM_BANK_ADDR_FLD	R/W	0h	The address of the Memory Bank which data will be read from.
19	FLASH_COMMAND_CTRL_MEM_RESV2_FLD	R	0h	Reserved
18:16	NB_OF_STIG_READ_BYTES_FLD	R/W	0h	It defines the number of read bytes for the extended STIG.
15:8	MEM_BANK_READ_DATA_FLD	R	0h	Last requested data from the STIG Memory Bank.
7:2	FLASH_COMMAND_CTRL_MEM_RESV3_FLD	R	0h	Reserved
1	MEM_BANK_REQ_IN_PROGRESS_FLD	R	0h	Memory Bank data request in progress.
0	TRIGGER_MEM_BANK_REQ_FLD	W	0h	Trigger the Memory Bank data request.

14.9.3.3.2.48 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register

1 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register (Offset = 90h) [reset = 0h]

Flash Command Control Register

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Table 14-23212. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 0090h**

Figure 14-7673. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Name Register

31	30	29	28	27	26	25	24
CMD_OPCODE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ENB_READ_DATA_FLD	NUM_RD_DATA_BYTES_FLD			ENB_COMD_ADDR_FLD	ENB_MODE_BIT_FLD	NUM_ADDR_BYTES_FLD	
R/W	R/W			R/W	R/W	R/W	
0h	0h			0h	0h	0h	
15	14	13	12	11	10	9	8
ENB_WRITE_DATA_FLD	NUM_WR_DATA_BYTES_FLD			NUM_DUMMY_CYCLES_FLD			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
NUM_DUMMY_CYCLES_FLD	FLASH_CMD_CTRL_RESV1_FLD				STIG_MEM_BANK_EN_FLD	CMD_EXEC_STATUS_FLD	CMD_EXEC_FLD
R/W	R				R/W	R	W
0h	0h				0h	0h	0h

Table 14-23214. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CMD_OPCODE_FLD	R/W	0h	Command Opcode: The command opcode field should be setup before triggering the command. For example, 0x20 maps to SubSector Erase. Writing to the execute field [bit 0] of this register launches the command. NOTE : Using this approach to issue commands to the device will make use of the instruction type of the device instruction configuration register. If this field is set to 2'b00, then the command opcode, command address, command dummy bytes and command data will all be transferred in a serial fashion. If this field is set to 2'b01, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0 and DQ1 pins. If this field is set to 2'b10, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0, DQ1, DQ2 and DQ3 pins.
23	ENB_READ_DATA_FLD	R/W	0h	Read Data Enable: Set to 1 if the command specified in the command opcode field [bits 31:24] requires read data bytes to be received from the device.
22:20	NUM_RD_DATA_BYTES_FLD	R/W	0h	Number of Read Data Bytes: Up to 8 data bytes may be read using this command. Set to 0 for 1 byte and 7 for 8 bytes.
19	ENB_COMD_ADDR_FLD	R/W	0h	Command Address Enable: Set to 1 if the command specified in bits 31:24 requires an address. This should be setup before triggering the command via Writing a 1 to the execute field.

Table 14-23214. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	ENB_MODE_BIT_FLD	R/W	0h	Mode Bit Enable: Set to 1 to ensure the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
17:16	NUM_ADDR_BYTES_FLD	R/W	0h	Number of Address Bytes: Set to the number of address bytes required [the address itself is programmed in the FLASH COMMAND ADDRESS REGISTERS]. This should be setup before triggering the command via bit 0 of this register. 2'b00 : 1 address byte 2'b01 : 2 address bytes 2'b10 : 3 address bytes 2'b11 : 4 address bytes
15	ENB_WRITE_DATA_FLD	R/W	0h	Write Data Enable: Set to 1 if the command specified in the command opcode field requires write data bytes to be sent to the device.
14:12	NUM_WR_DATA_BYTES_FLD	R/W	0h	Number of Write Data Bytes: Up to 8 Data bytes may be written using this command Set to 0 for 1 byte, 7 for 8 bytes.
11:7	NUM_DUMMY_CYCLES_FLD	R/W	0h	Number of Dummy cycles: Set to the number of dummy cycles required. This should be setup before triggering the command via the execute field of this register.
6:3	FLASH_CMD_CTRL_RESV1_FLD	R	0h	Reserved
2	STIG_MEM_BANK_EN_FLD	R/W	0h	STIG Memory Bank enable bit.
1	CMD_EXEC_STATUS_FLD	R	0h	Command execution in progress.
0	CMD_EXEC_FLD	W	0h	Execute the command.

14.9.3.3.2.49 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register

1 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register (Offset = 94h) [reset = 0h]

Flash Command Address Register

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Table 14-23215. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 0094h

Figure 14-7674. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-23217. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Command Address: This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the address used by the command specified in the opcode field [bits 31:24] of the Flash Command Control register.

14.9.3.3.2.50 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register

1 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register (Offset = A0h) [reset = 0h]

Flash Command Read Data Register (Lower)

Return to Summary Table

Table 14-23218. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00A0h**

Figure 14-7675. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA_FLD							
R							
0h							

Table 14-23220. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the flash device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.9.3.3.2.51 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register

1 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register (Offset = A4h) [reset = 0h]

Flash Command Read Data Register (Upper)

Return to Summary Table

Table 14-23221. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00A4h**

Figure 14-7676. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R							
0h							

Table 14-23223. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the FLASH device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.9.3.3.2.52 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register

1 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register (Offset = A8h) [reset = 0h]

Flash Command Write Data Register (Lower)

Return to Summary Table

Table 14-23224. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00A8h**

Figure 14-7677. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 14-23226. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Lower Byte: This is the command write data lower byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

14.9.3.3.2.53 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register

1 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register (Offset = ACh) [reset = 0h]

Flash Command Write Data Register (Upper)

Return to Summary Table

Table 14-23227. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00ACh**

Figure 14-7678. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 14-23229. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Upper Byte: This is the command write data upper byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

14.9.3.3.2.54 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register

1 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register (Offset = B0h) [reset = 0h]

Polling Flash Status Register

Return to Summary Table

Table 14-23230. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00B0h**

Figure 14-7679. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Name Register

31	30	29	28	27	26	25	24
DEVICE_STATUS_RSVD_FLD2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DEVICE_STATUS_RSVD_FLD2				DEVICE_STATUS_NB_DUMMY			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DEVICE_STATUS_RSVD_FLD1							DEVICE_STATUS_VALID_FLD
R							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEVICE_STATUS_FLD							
R							
0h							

Table 14-23232. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	DEVICE_STATUS_RSVD_FLD2	R	0h	Reserved
19:16	DEVICE_STATUS_NB_DUMMY	R/W	0h	Number of dummy cycles for auto-polling
15:9	DEVICE_STATUS_RSVD_FLD1	R	0h	Reserved
8	DEVICE_STATUS_VALID_FLD	R	0h	Device Status Valid: This should be set when value in bits from 7 to 0 is valid.
7:0	DEVICE_STATUS_FLD	R	0h	Defines actual Status Register of Device

14.9.3.3.2.55 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register

1 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register (Offset = B4h) [reset = 40000000h]

PHY Configuration Register

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Table 14-23233. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00B4h**

Figure 14-7680. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Name Register

31	30	29	28	27	26	25	24
PHY_CONFIG_RESYNC_FLD	PHY_CONFIG_RESET_FLD	PHY_CONFIG_RX_DLL_BYPASS_FLD	PHY_CONFIG_RESV2_FLD				
W	W	R/W	R				
0h	1h	0h	0h				
23	22	21	20	19	18	17	16
PHY_CONFIG_RESV2_FLD	PHY_CONFIG_TX_DLL_DELAY_FLD						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
PHY_CONFIG_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CONFIG_RESV1_FLD	PHY_CONFIG_RX_DLL_DELAY_FLD						
R	R/W						
0h	0h						

Table 14-23235. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_CONFIG_RESYNC_FLD	W	0h	This bit is used for re-synchronisation delay lines to update them with values from TX DLL Delay and RX DLL Delay fields.
30	PHY_CONFIG_RESET_FLD	W	1h	DLL Reset bit: This bit is used for reset of Delay Lines by software.
29	PHY_CONFIG_RX_DLL_BYPASS_FLD	R/W	0h	RX DLL Bypass: This field determines id RX DLL is bypassed.
28:23	PHY_CONFIG_RESV2_FLD	R	0h	Reserved
22:16	PHY_CONFIG_TX_DLL_DELAY_FLD	R/W	0h	TX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and spi_clk.
15:7	PHY_CONFIG_RESV1_FLD	R	0h	Reserved
6:0	PHY_CONFIG_RX_DLL_DELAY_FLD	R/W	0h	RX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and rx_dll_clk.

14.9.3.3.2.56 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register

1 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register (Offset = B8h) [reset = 800000h]

PHY DLL Initiator Control Register

Return to Summary Table

Table 14-23236. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00B8h**

Figure 14-7681. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">PHY_MASTER_CONTROL_RESV3_FLD</td><td>PHY_MASTER_LOCK_MODE_FLD</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PHY_MASTER_BYPASS_MODE_FLD</td><td colspan="3">PHY_MASTER_PHASE_DETECT_SELECTOR_FLD</td><td>PHY_MASTER_CONTROL_RESV2_FLD</td><td colspan="3">PHY_MASTER_NB_INDICATIONS_FLD</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td>1h</td><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_MASTER_CONTROL_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PHY_MASTER_CONTROL_RESV1_FLD</td><td colspan="7">PHY_MASTER_INITIAL_DELAY_FLD</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-23238. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	PHY_MASTER_CONTROL_RESV3_FLD	R	0h	Reserved
24	PHY_MASTER_LOCK_MODE_FLD	R/W	0h	Determines if the initiator delay line locks on a full cycle or half cycle of delay.
23	PHY_MASTER_BYPASS_MODE_FLD	R/W	1h	Controls the bypass mode of the initiator and target DLLs.
22:20	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD	R/W	0h	Selects the number of delay elements to be inserted between the phase detect flip-flops.
19	PHY_MASTER_CONTROL_RESV2_FLD	R	0h	Reserved
18:16	PHY_MASTER_NB_INDICATIONS_FLD	R/W	0h	Holds the number of consecutive increment or decrement indications.
15:7	PHY_MASTER_CONTROL_RESV1_FLD	R	0h	Reserved

Table 14-23238. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	PHY_MASTER_INITIAL_DELAY_FLD	R/W	0h	This value is the initial delay value for the DLL.

14.9.3.3.2.57 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register

1 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register (Offset = BCh) [reset = 0h]

DLL Observable Register Lower

Return to Summary Table

Table 14-23239. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 00BCh

Figure 14-7682. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD					DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD		DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD
R					R		R
0h					0h		0h

Table 14-23241. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD	R	0h	Holds the state of the cumulative dll_lock_inc register.
23:16	DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD	R	0h	Holds the state of the cumulative dll_lock_dec register.
15	DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	R	0h	This bit indicates that lock of loopback is done.
14:8	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD	R	0h	Reports the DLL encoder value from the initiator DLL to the target DLLs.
7:3	DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD	R	0h	Reports the number of increments or decrements required for the initiator DLL to complete the locking process.
2:1	DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD	R	0h	Defines the mode in which the DLL has achieved the lock.

Table 14-23241. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD	R	0h	Indicates status of DLL.

14.9.3.3.2.58 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register

1 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register (Offset = C0h) [reset = 0h]

DLL Observable Register Upper

Return to Summary Table

Table 14-23242. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00C0h**

Figure 14-7683. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DLL_OBSERVABLE_UPPER_RESV2_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>DLL_OBSERVABLE_UPPER_RESV2_FLD</td><td colspan="7">DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DLL_OBSERVABLE_UPPER_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>DLL_OBSERVABLE_UPPER_RESV1_FLD</td><td colspan="7">DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-23244. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	DLL_OBSERVABLE_UPPER_RESV2_FLD	R	0h	Reserved
22:16	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the TX delay line for this slice.
15:7	DLL_OBSERVABLE_UPPER_RESV1_FLD	R	0h	Reserved
6:0	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the RX delay line for this slice.

14.9.3.3.2.59 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register

1 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register (Offset = E0h) [reset = 13EDFA00h]

Opcode Extension Register (Lower)

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Table 14-23245. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00E0h**

Figure 14-7684. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Name Register

31	30	29	28	27	26	25	24
EXT_READ_OPCODE_FLD							
R/W							
13h							
23	22	21	20	19	18	17	16
EXT_WRITE_OPCODE_FLD							
R/W							
EDh							
15	14	13	12	11	10	9	8
EXT_POLL_OPCODE_FLD							
R/W							
FAh							
7	6	5	4	3	2	1	0
EXT_STIG_OPCODE_FLD							
R/W							
0h							

Table 14-23247. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EXT_READ_OPCODE_FLD	R/W	13h	Supplement byte of any Read Opcode
23:16	EXT_WRITE_OPCODE_FLD	R/W	EDh	Supplement byte of any Write Opcode
15:8	EXT_POLL_OPCODE_FLD	R/W	FAh	Supplement byte of any Polling Opcode
7:0	EXT_STIG_OPCODE_FLD	R/W	0h	Supplement byte of any STIG Opcode

14.9.3.3.2.60 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register

1 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register (Offset = E4h) [reset = 6F90000h]

Opcode Extension Register (Upper)

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Table 14-23248. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00E4h**

Figure 14-7685. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Name Register

31	30	29	28	27	26	25	24
WEL_OPCODE_FLD							
R/W							
6h							
23	22	21	20	19	18	17	16
EXT_WEL_OPCODE_FLD							
R/W							
F9h							
15	14	13	12	11	10	9	8
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							

Table 14-23250. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WEL_OPCODE_FLD	R/W	6h	First byte of any WEL Opcode
23:16	EXT_WEL_OPCODE_FLD	R/W	F9h	Supplement byte of any WEL Opcode
15:0	OPCODE_EXT_UPPER_RESV1_FLD	R	0h	Reserved

14.9.3.3.2.61 OSPI_FLASH_CFG_MODULE_ID_REG Register

1 OSPI_FLASH_CFG_MODULE_ID_REG Register (Offset = FCh) [reset = 3000300h]

Module ID Register

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Table 14-23251. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 00FCh**

Figure 14-7686. OSPI_FLASH_CFG_MODULE_ID_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FIX_PATCH_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MODULE_ID_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">MODULE_ID_RESV_FLD</td><td colspan="2">CONF_FLD</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-23253. OSPI_FLASH_CFG_MODULE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	FIX_PATCH_FLD	R	3h	Fix/path number related to revision described by 3 LSBs of this register
23:8	MODULE_ID_FLD	R	3h	Module/Revision ID number
7:2	MODULE_ID_RESV_FLD	R	0h	Reserved
1:0	CONF_FLD	R	0h	Configuration ID number: 0 : OCTAL + PHY Configuration 1 : OCTAL Configuration 2 : QUAD + PHY Configuration 3 : QUAD Configuration

14.9.3.3.2.62 OSPI_CFG_PID Register

1 OSPI_CFG_PID Register (Offset = 0h) [reset = 68747900h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-23254. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 4000h**

Figure 14-7687. OSPI_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		874h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
874h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Fh					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-23256. OSPI_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: psrst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: psrst_n
27:16	MODULE_ID	R	874h	Module ID Reset Source: psrst_n
15:11	RTL	R	Fh	RTL revision. Will vary depending on release. Reset Source: psrst_n
10:8	MAJOR	R	1h	Major revision Reset Source: psrst_n
7:6	CUSTOM	R	0h	Custom Reset Source: psrst_n
5:0	MINOR	R	0h	Minor revision Reset Source: psrst_n

14.9.3.3.2.63 OSPI_CFG_CTRL Register

1 OSPI_CFG_CTRL Register (Offset = 4h) [reset = 0h]

The Control Register contains general control bits for the ospi

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Table 14-23257. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	0FC4 4004h

Figure 14-7688. OSPI_CFG_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PIPELINE_MODE_FLUSH	RESERVED		
NONE				R/W	NONE		
0h				0h	0h		

Table 14-23259. OSPI_CFG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PIPELINE_MODE_FLUSH	R/W	0h	1 - Flush Cadence Flash Controller FIFO by forcin gAHB SEL low. 0 - AHB Sel to Cadence Controller is 1 Reset Source: psrst_n
2:0	RESERVED	NONE	0h	Reserved

14.9.3.3.2.64 OSPI_CFG_STAT Register

1 OSPI_CFG_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the ospi

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Table 14-23260. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 4008h**

Figure 14-7689. OSPI_CFG_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_INIT_DONE	RESERVED
NONE						R	NONE
0h						0h	0h

Table 14-23262. OSPI_CFG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_INIT_DONE	R	0h	0:Memory Initialization is in progress, 1:Memory Intialization Done Reset Source: psrst_n
0	RESERVED	NONE	0h	Reserved

14.9.3.3.2.65 OSPI_CFG_EOI Register

1 OSPI_CFG_EOI Register (Offset = 20h) [reset = 0h]

End of Interrupt Register

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Table 14-23263. Instance Table

Instance Name	Physical Address
FSS0_OSPI_0	**0FC4 4020h**

Figure 14-7690. OSPI_CFG_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI							
W							
0h							

Table 14-23265. OSPI_CFG_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI	W	0h	Write with bit position of targetted interrupt. (E.g. Ext TS is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt Reset Source: psrst_n

14.9.3.4 GPMC

GPMC

14.9.3.4.1 GPMC Summaries

GPMC Summaries

Table 14-23266. GPMC Registers, Base Address=3B00 0000h, Length=1024

Offset	Length	Register Name	GPMC0 Physical Address
0h	32	GPMC_REVISION	3B00 0000h
10h	32	GPMC_SYSCONFIG	3B00 0010h
14h	32	GPMC_SYSSTATUS	3B00 0014h
18h	32	GPMC_IRQSTATUS	3B00 0018h
1Ch	32	GPMC_IRQENABLE	3B00 001Ch
40h	32	GPMC_TIMEOUT_CONTROL	3B00 0040h
44h	32	GPMC_ERR_ADDRESS	3B00 0044h
48h	32	GPMC_ERR_TYPE	3B00 0048h
50h	32	GPMC_CONFIG	3B00 0050h
54h	32	GPMC_STATUS	3B00 0054h
1E0h	32	GPMC_PREFETCH_CONFIG1	3B00 01E0h
1E4h	32	GPMC_PREFETCH_CONFIG2	3B00 01E4h
1ECh	32	GPMC_PREFETCH_CONTROL	3B00 01ECh
1F0h	32	GPMC_PREFETCH_STATUS	3B00 01F0h
1F4h	32	GPMC_ECC_CONFIG	3B00 01F4h
1F8h	32	GPMC_ECC_CONTROL	3B00 01F8h
1FCh	32	GPMC_ECC_SIZE_CONFIG	3B00 01FCh
200h	32	GPMC_ECC_RESULT_J	3B00 0200h + formula
2D0h	32	GPMC_BCH_SWDATA	3B00 02D0h
0h	32	GPMC_CONFIG1_J	3B00 0000h + formula
4h	32	GPMC_CONFIG2_J	3B00 0004h + formula
8h	32	GPMC_CONFIG3_J	3B00 0008h + formula
Ch	32	GPMC_CONFIG4_J	3B00 000Ch + formula
10h	32	GPMC_CONFIG5_J	3B00 0010h + formula
14h	32	GPMC_CONFIG6_J	3B00 0014h + formula
18h	32	GPMC_CONFIG7_J	3B00 0018h + formula
1Ch	32	GPMC_NAND_COMMAND_J	3B00 001Ch + formula
20h	32	GPMC_NAND_ADDRESS_J	3B00 0020h + formula
24h	32	GPMC_NAND_DATA_J	3B00 0024h + formula
0h	32	GPMC_BCH_RESULT_0_J	3B00 0000h + formula
4h	32	GPMC_BCH_RESULT_1_J	3B00 0004h + formula
8h	32	GPMC_BCH_RESULT_2_J	3B00 0008h + formula
Ch	32	GPMC_BCH_RESULT_3_J	3B00 000Ch + formula
0h	32	GPMC_BCH_RESULT_4_J	3B00 0000h + formula
4h	32	GPMC_BCH_RESULT_5_J	3B00 0004h + formula
8h	32	GPMC_BCH_RESULT_6_J	3B00 0008h + formula

14.9.3.4.2 GPMC Registers

GPMC Registers

14.9.3.4.2.1 GPMC_REVISION Register

1 GPMC_REVISION Register (Offset = 0h) [reset = 60h]

This register contains the IP revision code

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Table 14-23267. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0000h**

Figure 14-7691. GPMC_REVISION Name Register

31	30	29	28	27	26	25	24
RESERVED_230							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_230							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_230							
R							
0h							
7	6	5	4	3	2	1	0
REV							
R							
60h							

Table 14-23269. GPMC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_230	R	0h	Reads returns 0
7:0	REV	R	60h	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 1.0, 0x21 for 2.1 Reset Source: func_mod_g_arst_n

14.9.3.4.2.2 GPMC_SYSCONFIG Register

1 GPMC_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register controls the various parameters of the OCP interface

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Table 14-23270. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0010h**

Figure 14-7692. GPMC_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_234							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_234							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_234							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_234			IDLEMODE		RESERVED_233	RESERVED	AUTOIDLE
R			R/W		R	R/W	R/W
0h			0h		0h	0h	0h

Table 14-23272. GPMC_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED_234	R	0h	Write 0's for future compatibility Reads return 0
4:3	IDLEMODE	R/W	0h	Reset Source: func_mod_g_arst_n 0 Force-idle. An idle request is acknowledged unconditionally 1 No-idle. An idle request is never acknowledged 2 Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module 3 reserved do not use
2	RESERVED_233	R	0h	Write 0 for future compatibility Reads returns 0
1	RESERVED	R/W	0h	This bit must be kept 0 for normal functioning of the IP. Do not set this bit to 1 0 Normal mode 1 The module is reset
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy Reset Source: func_mod_g_arst_n 0 OCP clock is free-running 1 Automatic OCP clock gating strategy is applied, based on the OCP interface activity

14.9.3.4.2.3 GPMC_SYSSTATUS Register

1 GPMC_SYSSTATUS Register (Offset = 14h) [reset = 0h]

This register provides status information about the module, excluding the interrupt status information

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Table 14-23273. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0014h**

Figure 14-7693. GPMC_SYSSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_235							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_235							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_235							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							0h

Table 14-23275. GPMC_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_235	R	0h	Reads returns 0
7:1	RESERVED	R	0h	Reads returns 0 [reserved for OCP-socket status information]
0	RESETDONE	R	0h	Internal reset monitoring Reset Source: func_mod_g_arst_n 0 Internal module reset in on-going 1 Reset completed

14.9.3.4.2.4 GPMC_IRQSTATUS Register

1 GPMC_IRQSTATUS Register (Offset = 18h) [reset = 0h]

This interrupt status register regroups all the status of the module internal events that can generate an interrupt.

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Table 14-23276. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0018h**

Figure 14-7694. GPMC_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_218							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_218							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_218				WAIT3EDGEDETECTIONSTATUS	WAIT2EDGEDETECTIONSTATUS	WAIT1EDGEDETECTIONSTATUS	WAIT0EDGEDETECTIONSTATUS
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_219						TERMINALCOUNTSTATUS	FIFOEVENTSTATUS
R						R/W1TC	R/W1TC
0h						0h	0h

Table 14-23278. GPMC_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_218	R	0h	Write 0's for future compatibility. Read returns 0
11	WAIT3EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait3 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: A transition on WAIT3 input pin has not been detected` 0 `Write 0: Wait3EdgeDetection status bit unchanged` 1 `Read 1: A transition on WAIT3 input pin has been detected` 1 `Write 1: Wait3EdgeDetection status bit is reset`
10	WAIT2EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait2 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: A transition on WAIT2 input pin has not been detected` 0 `Write 0: Wait2EdgeDetection status bit unchanged` 1 `Read 1: A transition on WAIT2 input pin has been detected` 1 `Write 1: Wait2EdgeDetection status bit is reset`

Table 14-23278. GPMC_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	WAIT1EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait1 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: A transition on WAIT1 input pin has not been detected` 0 `Write 0: Wait1EdgeDetection status bit unchanged` 1 `Read 1: A transition on WAIT1 input pin has been detected` 1 `Write 1: Wait1EdgeDetection status bit is reset`
8	WAIT0EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait0 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: A transition on WAIT0 input pin has not been detected` 0 `Write 0: Wait0EdgeDetection status bit unchanged` 1 `Read 1: A transition on WAIT0 input pin has been detected` 1 `Write 1: Wait0EdgeDetection status bit is reset`
7:2	RESERVED_219	R	0h	Write 0's for future compatibility. Read returns 0
1	TERMINALCOUNTSTATUS	R/W1TC	0h	Status of the TerminalCountEvent interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: Indicates that CountValue is greater than 0` 0 `Write 0: TerminalCountEvent status bit unchanged` 1 `Read 1: Indicates that CountValue is equal to 0` 1 `Write 1: TerminalCountEvent status bit is reset`
0	FIFOEVENTSTATUS	R/W1TC	0h	Status of the FIFOEvent interrupt Reset Source: func_mod_g_arst_n 0 `Read 0: Indicates than less than FIFOThreshold bytes are available in prefetch mode and less than FIFOThreshold bytes free places are available in write posting mode.` 0 `Write 0: FIFOEvent status bit unchanged` 1 `Read 1: Indicates than at least FIFOThreshold bytes are available in prefetch mode and at least FIFOThreshold bytes free places are available in write posting mode.` 1 `Write 1: FIFOEvent status bit is reset`

14.9.3.4.2.5 GPMC_IRQENABLE Register

1 GPMC_IRQENABLE Register (Offset = 1Ch) [reset = 0h]

The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.

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Table 14-23279. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 001Ch**

Figure 14-7695. GPMC_IRQENABLE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_216</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_216</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED_216</td><td>WAIT3EDGEDETECTIONENABLE</td><td>WAIT2EDGEDETECTIONENABLE</td><td>WAIT1EDGETECTIONENABLE</td><td>WAIT0EDGEDETECTIONENABLE</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED_217</td><td>TERMINALCOUNTEVENTENABLE</td><td>FIFOEVENTENABLE</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-23281. GPMC_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_216	R	0h	Write 0's for future compatibility. Read returns 0
11	WAIT3EDGEDETECTIONENABLE	R/W	0h	Enables the Wait3 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 Wait3EdgeDetection interrupt is masked 1 Wait3EdgeDetection event generates an interrupt if occurs
10	WAIT2EDGEDETECTIONENABLE	R/W	0h	Enables the Wait2 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 Wait2EdgeDetection interrupt is masked 1 Wait2EdgeDetection event generates an interrupt if occurs
9	WAIT1EDGEDETECTIONENABLE	R/W	0h	Enables the Wait1 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 Wait1EdgeDetection interrupt is masked 1 Wait1EdgeDetection event generates an interrupt if occurs

Table 14-23281. GPMC_IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WAIT0EDGEDETECTIONENABLE	R/W	0h	Enables the Wait0 Edge Detection interrupt Reset Source: func_mod_g_arst_n 0 `Wait0EdgeDetection interrupt is masked` 1 `Wait0EdgeDetection event generates an interrupt if occurs`
7:2	RESERVED_217	R	0h	Write 0's for future compatibility. Read returns 0
1	TERMINALCOUNTEVENTENABLE	R/W	0h	Enables TerminalCountEvent interrupt issuing in pre-fetch or write posting mode Reset Source: func_mod_g_arst_n 0 `TerminalCountEvent interrupt is masked` 1 `TerminalCountEvent interrupt is not masked`
0	FIFOEVENTENABLE	R/W	0h	Enables the FIFOEvent interrupt Reset Source: func_mod_g_arst_n 0 `FIFOEvent interrupt is masked` 1 `FIFOEvent interrupt is not masked`

14.9.3.4.2.6 GPMC_TIMEOUT_CONTROL Register

1 GPMC_TIMEOUT_CONTROL Register (Offset = 40h) [reset = 1FF0h]

The GPMC_TIMEOUT_CONTROL register allows the user to set the start value of the timeout counter

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Table 14-23282. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0040h**

Figure 14-7696. GPMC_TIMEOUT_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED_237							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_237							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_237			TIMEOUTSTARTVALUE				
R			R/W				
0h			1FFh				
7	6	5	4	3	2	1	0
TIMEOUTSTARTVALUE				RESERVED_238			TIMEOUTENABLE
R/W				R			R/W
1FFh				0h			0h

Table 14-23284. GPMC_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_237	R	0h	Write 0's for future compatibility. Read returns 0
12:4	TIMEOUTSTARTVALUE	R/W	1FFh	Start value of the time-out counter [0x000 corresponds to 0 GPMC.FCLK cycle, 0x001 corresponds to 1 GmpcClk cycle, &, 0x1FF corresponds to 511 GPMC.FCLK cyles.] Reset Source: func_mod_g_arst_n
3:1	RESERVED_238	R	0h	Write 0's for future compatibility. Read returns 0
0	TIMEOUTENABLE	R/W	0h	Enable bit of the TimeOut feature Reset Source: func_mod_g_arst_n 0 TimeOut feature is disabled 1 TimeOut feature is enabled

14.9.3.4.2.7 GPMC_ERR_ADDRESS Register

1 GPMC_ERR_ADDRESS Register (Offset = 44h) [reset = 0h]

The GPMC_ERR_ADDRESS register stores the address of the illegal access when an error occurs

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Table 14-23285. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0044h**

Figure 14-7697. GPMC_ERR_ADDRESS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED_212</td><td colspan="7">ILLEGALADD</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ILLEGALADD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ILLEGALADD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ILLEGALADD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23287. GPMC_ERR_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_212	R	0h	Write 0's for future compatibility. Read returns 0
30:0	ILLEGALADD	R	0h	Address of illegal access : A30[0 for memory region, 1 for GPMC register region] and A29-A0[1 GBytes maximum] Reset Source: func_mod_g_arst_n

14.9.3.4.2.8 GPMC_ERR_TYPE Register

1 GPMC_ERR_TYPE Register (Offset = 48h) [reset = 0h]

The GPMC_ERR_TYPE register stores the type of error when an error occurs

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Table 14-23288. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0048h

Figure 14-7698. GPMC_ERR_TYPE Name Register

31	30	29	28	27	26	25	24
RESERVED_215							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_215							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_215					ILLEGALMCMD		
R					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_213			ERRORNOTSUPPADD	ERRORNOTSUPPMCMD	ERRORTIMEOUT	RESERVED_214	ERRORVALID
R			R	R	R	R	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-23290. GPMC_ERR_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED_215	R	0h	Write 0's for future compatibility. Read returns 0
10:8	ILLEGALMCMD	R	0h	System Command of the transaction that caused the error Reset Source: func_mod_g_arst_n
7:5	RESERVED_213	R	0h	Write 0's for future compatibility. Read returns 0
4	ERRORNOTSUPPADD	R	0h	Not supported Address error Reset Source: func_mod_g_arst_n 0 No error occurs 1 The error is due to a non supported Address
3	ERRORNOTSUPPMCMD	R	0h	Not supported Command error Reset Source: func_mod_g_arst_n 0 No error occurs 1 The error is due to a non supported Command
2	ERRORTIMEOUT	R	0h	Time-out error Reset Source: func_mod_g_arst_n 0 No error occurs 1 The error is due to a time out
1	RESERVED_214	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-23290. GPMC_ERR_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ERRORVALID	R/W1TC	0h	Error validity status - Must be explicitely cleared with a write 1 transaction Reset Source: func_mod_g_arst_n 0 `All error fields no longer valid` 1 `Error detected and logged in the other error fields`

14.9.3.4.2.9 GPMC_CONFIG Register

1 GPMC_CONFIG Register (Offset = 50h) [reset = A00h]

The configuration register allows global configuration of the GPMC

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Table 14-23291. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0050h**

Figure 14-7699. GPMC_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				WAIT3PINPOLARITY	WAIT2PINPOLARITY	WAIT1PINPOLARITY	WAIT0PINPOLARITY
R				R/W	R/W	R/W	R/W
0h				1h	0h	1h	0h
7	6	5	4	3	2	1	0
RESERVED_0			WRITEPROTECT	RESERVED_2		LIMITEDADDRESS	NANDFORCEPOSTEDWRITE
R			R/W	R		R/W	R/W
0h			0h	0h		0h	0h

Table 14-23293. GPMC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Write 0's for future compatibility. Read returns 0
11	WAIT3PINPOLARITY	R/W	1h	Selects the polarity of input pin WAIT3 Reset Source: func_mod_g_arst_n 0 WAIT3 active low 1 WAIT3 active high
10	WAIT2PINPOLARITY	R/W	0h	Selects the polarity of input pin WAIT2 Reset Source: func_mod_g_arst_n 0 WAIT2 active low 1 WAIT2 active high
9	WAIT1PINPOLARITY	R/W	1h	Selects the polarity of input pin WAIT1 Reset Source: func_mod_g_arst_n 0 WAIT1 active low 1 WAIT1 active high
8	WAIT0PINPOLARITY	R/W	0h	Selects the polarity of input pin WAIT0 Reset Source: func_mod_g_arst_n 0 WAIT0 active low 1 WAIT0 active high

Table 14-23293. GPMC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:5	RESERVED_0	R	0h	Write 0's for future compatibility. Read returns 0
4	WRITEPROTECT	R/W	0h	Controls the WP output pin level Reset Source: func_mod_g_arst_n 0 WP output pin is low 1 WP output pin is high
3:2	RESERVED_2	R	0h	Write 0's for future compatibility. Read returns 0
1	LIMITEDADDRESS	R/W	0h	Limited Address device support Reset Source: func_mod_g_arst_n 0 No effect 1 A26-A11 are not modified during an external memory access.
0	NANDFORCEPOSTEDWRITE	R/W	0h	Enables the Force Posted Write feature to NAND Cmd/Add/Data location Reset Source: func_mod_g_arst_n 0 Disables Force Posted Write 1 Enables Force Posted Write

14.9.3.4.2.10 GPMC_STATUS Register

1 GPMC_STATUS Register (Offset = 54h) [reset = 1h]

The status register provides global status bits of the GPMC

Return to Summary Table

Table 14-23294. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0054h

Figure 14-7700. GPMC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_231							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_231							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_231				WAIT3STATUS	WAIT2STATUS	WAIT1STATUS	WAIT0STATUS
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_232							EMPTYWRITEBUFFERSTATUS
R							R
0h							1h

Table 14-23296. GPMC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_231	R	0h	Write 0's for future compatibility. Read returns 0
11	WAIT3STATUS	R	0h	Is a copy of input pin WAIT3. [Reset value is WAIT3 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 `WAIT3 de-asserted` 1 `WAIT3 asserted`
10	WAIT2STATUS	R	0h	Is a copy of input pin WAIT2. [Reset value is WAIT2 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 `WAIT2 de-asserted` 1 `WAIT2 asserted`
9	WAIT1STATUS	R	0h	Is a copy of input pin WAIT1. [Reset value is WAIT1 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 `WAIT1 de-asserted` 1 `WAIT1 asserted`

Table 14-23296. GPMC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WAIT0STATUS	R	0h	Is a copy of input pin WAIT0. [Reset value is WAIT0 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 `WAIT0 de-asserted` 1 `WAIT0 asserted`
7:1	RESERVED_232	R	0h	Write 0's for future compatibility Reads returns 0
0	EMPTYWRITEBUFFERSTATUS	R	1h	Stores the empty status of the write buffer Reset Source: func_mod_g_arst_n 0 `Write Buffer is not empty` 1 `Write Buffer is empty`

14.9.3.4.2.11 GPMC_PREFETCH_CONFIG1 Register

1 GPMC_PREFETCH_CONFIG1 Register (Offset = 1E0h) [reset = 4000h]

Prefetch engine configuration 1

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Table 14-23297. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01E0h**

Figure 14-7701. GPMC_PREFETCH_CONFIG1 Name Register

31	30	29	28	27	26	25	24
RESERVED_221	CYCLEOPTIMIZATION			ENABLEOPTIMIZEDACCESS	ENGINECSSELECTOR		
R	R/W			R/W	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PFPWENROUNDROBIN	RESERVED_224			PFPWWEIGHTEDPRIO			
R/W	R			R/W			
0h	0h			0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_220	FIFOTHRESHOLD						
R	R/W						
0h	40h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ENABLEENGINE	RESERVED_223	WAITPINSELECTOR		SYNCHROMODE	DMAMODE	RESERVED_222	ACCESSMODE
R/W	R	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-23299. GPMC_PREFETCH_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_221	R	0h	Write 0's for future compatibility. Read returns 0
30:28	CYCLEOPTIMIZATION	R/W	0h	Define the number of GPMC.FCLK cycles to be substracted from RdCycleTime, WrCycleTime, AccessTime, CSRdOffTime, CSWrOffTime, ADVRdOffTime, ADVWrOffTime, OEOffTime, WEOffTime [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0x7 corresponds to 7 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

27	ENABLEOPTIMIZEDACCESS	R/W	0h	Enables access cycle optimization
				Reset Source: func_mod_g_arst_n
				`0 Access cycle optimization is disabled`
				`1 Access cycle optimization is enabled`

26:24	ENGINECSSELECTOR	R/W	0h	Selects the CS where Prefetch Postwrite engine is active [0x0 corresponds toCS0, 0x1 corresponds to CS1, &, 0x7 corresponds to CS7] Reset Source: func_mod_g_arst_n

Table 14-23299. GPMC_PREFETCH_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	PFPWENROUNDROBIN	R/W	0h	Enables the PFPW RoundRobin arbitration Reset Source: func_mod_g_arst_n 0 `Prefetch Postwrite engine round robin arbitration  is disabled` 1 `Prefetch Postwrite engine round robin arbitration is enabled`
22:20	RESERVED_224	R	0h	Write 0's for future compatibility. Read returns 0
19:16	PFPWWEIGHTEDPRIO	R/W	0h	When an arbitration occurs between a direct memory access and a PFPW engine access, the direct memory access is always serviced. If the PFPWEnRoundRobin is enabled, 0x0 means : the next access is granted to the PFPW engine, 0x1 means : the two next accesses are granted to the PFPW engine, ..., 0xF means : the 16 next accesses are granted to the PFPW engine. Reset Source: func_mod_g_arst_n
15	RESERVED_220	R	0h	Write 0's for future compatibility. Read returns 0
14:8	FIFOTHRESHOLD	R/W	40h	Selects the maximum number of bytes read from the FIFO or written to the FIFO by the host on a DMA or interrupt request [0x00 corresponds to 0 byte, 0x01 corresponds to 1 byte, &, 0x40 corresponds to 64 bytes] Reset Source: func_mod_g_arst_n
7	ENABLEENGINE	R/W	0h	Enables the Prefetch Postwite engine Reset Source: func_mod_g_arst_n 0 `Prefetch Postwrite engine is disabled` 1 `Prefetch Postwrite engine is enabled`
6	RESERVED_223	R	0h	Write 0's for future compatibility. Read returns 0
5:4	WAITPINSELECTOR	R/W	0h	Select which wait pin edge detector should start the engine in synchronized mode Reset Source: func_mod_g_arst_n 0 `Selects Wait0EdgeDetection` 1 `Selects Wait1EdgeDetection` 2 `Selects Wait2EdgeDetection` 3 `Selects Wait3EdgeDetection`
3	SYNCHROMODE	R/W	0h	Selects when the engine starts the access to CS Reset Source: func_mod_g_arst_n 0 `Engine starts the access to CS as soon as StartEngine is set` 1 `Engine starts the access to CS as soon as StartEngine is set AND wait to non wait edge detection on the selected wait pin`
2	DMAMODE	R/W	0h	Selects interrupt synchronization or DMA request synchronization Reset Source: func_mod_g_arst_n 0 `Interrupt synchronization is enabled. Only interrupt line will be activated on FIFO threshold crossing.` 1 `DMA request synchronization is enabled.A DMA request protocol is used.`
1	RESERVED_222	R/W	0h	Write 0's for future compatibility. Read returns 0
0	ACCESSMODE	R/W	0h	Selects pre-fetch read or write posting accesses Reset Source: func_mod_g_arst_n 0 `Pre-fetch read mode` 1 `Write posting mode`

14.9.3.4.2.12 GPMC_PREFETCH_CONFIG2 Register

1 GPMC_PREFETCH_CONFIG2 Register (Offset = 1E4h) [reset = 0h]

Prefetch engine configuration 2

Return to Summary Table

Table 14-23300. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01E4h**

Figure 14-7702. GPMC_PREFETCH_CONFIG2 Name Register

31	30	29	28	27	26	25	24
RESERVED_224							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_224							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_224		TRANSFERCOUNT					
R		R/W					
0h		0h					
7	6	5	4	3	2	1	0
TRANSFERCOUNT							
R/W							
0h							

Table 14-23302. GPMC_PREFETCH_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_224	R	0h	Write 0's for future compatibility. Read returns 0
13:0	TRANSFERCOUNT	R/W	0h	Selects the number of bytes to be read or written by the engine to the selected CS [0x0000 corresponds to 0 byte, 0x0001 corresponds to 1 byte, &, 0x2000 corresponds to 8 Kbytes] Reset Source: func_mod_g_arst_n

14.9.3.4.2.13 GPMC_PREFETCH_CONTROL Register

1 GPMC_PREFETCH_CONTROL Register (Offset = 1ECh) [reset = 0h]

Prefetch engine control

Return to Summary Table

Table 14-23303. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01ECh**

Figure 14-7703. GPMC_PREFETCH_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED_225							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_225							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_225							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_225							STARTENGINE
R							R/W
0h							0h

Table 14-23305. GPMC_PREFETCH_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_225	R	0h	Write 0's for future compatibility. Read returns 0
0	STARTENGINE	R/W	0h	Resets the FIFO pointer and starts the engine Reset Source: func_mod_g_arst_n 0 `write 0 stops the engine Read 0: engine is stopped` 1 `write 1 resets the FIFO pointer to 0x0 in prefetch mode and 0x40 in postwrite mode and starts the engine. Read 1: engine is running`

14.9.3.4.2.14 GPMC_PREFETCH_STATUS Register

1 GPMC_PREFETCH_STATUS Register (Offset = 1F0h) [reset = 0h]

Prefetch engine status

Return to Summary Table

Table 14-23306. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01F0h**

Figure 14-7704. GPMC_PREFETCH_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_227	FIFOPOINTER						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED_228							FIFOTHRESHOLDSTATUS
R							R
0h							0h

15	14	13	12	11	10	9	8
RESERVED_226		COUNTVALUE					
R		R					
0h		0h					

7	6	5	4	3	2	1	0
COUNTVALUE							
R							
0h							

Table 14-23308. GPMC_PREFETCH_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_227	R	0h	Write 0's for future compatibility. Read returns 0
30:24	FIFOPOINTER	R	0h	Number of available bytes to be read or number of free empty byte places to be written [0x00 corresponds to 0 byte available to be read or 0 free empty place to be written, &, 0x40 corresponds to 64 bytes available to be read or 64 empty places to be written] Reset Source: func_mod_g_arst_n
23:17	RESERVED_228	R	0h	Write 0's for future compatibility. Read returns 0
16	FIFOTHRESHOLDSTATUS	R	0h	Set when FIFOPointer exceeds FIFOThreshold value Reset Source: func_mod_g_arst_n 0 `FIFOPointer smaller or equal to FIFOThreshold. Writing to this bit has no effect` 1 `FIFOPointer greater than FIFOThreshold. Writing to this bit has no effect`
15:14	RESERVED_226	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-23308. GPMC_PREFETCH_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:0	COUNTVALUE	R	0h	Number of remaining bytes to be read or to be written by the engine according to the TransferCount value [0x0000 corresponds to 0 byte remaining to be read or to be written, 0x0001 corresponds to 1 byte remaining to be read or to be written, &, 0x2000 corresponds to 8 Kbytes remaining to be read or to be written] Reset Source: func_mod_g_arst_n

14.9.3.4.2.15 GPMC_ECC_CONFIG Register

1 GPMC_ECC_CONFIG Register (Offset = 1F4h) [reset = 1030h]

ECC configuration

Return to Summary Table

Table 14-23309. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01F4h**

Figure 14-7705. GPMC_ECC_CONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_206</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED_206</td><td>ECCALGORITHM</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED_205</td><td colspan="2">ECCBCHTSEL</td><td colspan="4">ECCWRAPMODE</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">1h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>ECC16B</td><td colspan="3">ECCTOPSECTOR</td><td colspan="3">ECCCS</td><td>ECCENABLE</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">3h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-23311. GPMC_ECC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_206	R	0h	Write 0's for future compatibility. Read returns 0
16	ECCALGORITHM	R/W	0h	ECC algorithm used 0x0: Hamming code 0x1: BCH code Reset Source: func_mod_g_arst_n
15:14	RESERVED_205	R	0h	Write 0's for future compatibility. Read returns 0
13:12	ECCBCHTSEL	R/W	1h	Error correction capability used for BCH 0x0: up to 4 bits error correction [t = 4] 0x1: up to 8 bits error correction [t=8] 0x2: up to 16 bits error correction [t=16] 0x3: reserved Reset Source: func_mod_g_arst_n
11:8	ECCWRAPMODE	R/W	0h	Spare area organization definition for the BCH algorithm. See the BCH syndrome/parity calculator module functional specification for more details Reset Source: func_mod_g_arst_n
7	ECC16B	R/W	0h	Selects an ECC calculated on 16 columns Reset Source: func_mod_g_arst_n 0 `ECC calculated on 8 columns` 1 `ECC calculated on 16 columns`

Table 14-23311. GPMC_ECC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	ECCTOPSECTOR	R/W	3h	Number of sectors to process with the BCH algorithm 0x0: 1 sector [512kB page] 0x1: 2 sectors ... 0x3: 4 sectors [2kB page] ... 0x7: 8 sectors [4kB page] Reset Source: func_mod_g_arst_n
3:1	ECCCS	R/W	0h	Selects the CS where ECC is computed Reset Source: func_mod_g_arst_n 0 `Chip select 0` 1 `Chip select 1` 2 `Chip select 2` 3 `Chip select 3` 4 `Chip select 4` 5 `Chip select 5` 6 `Chip select 6` 7 `Chip select 7`
0	ECCENABLE	R/W	0h	Enables the ECC feature Reset Source: func_mod_g_arst_n 0 `ECC disabled` 1 `ECC enabled`

14.9.3.4.2.16 GPMC_ECC_CONTROL Register

1 GPMC_ECC_CONTROL Register (Offset = 1F8h) [reset = 0h]

ECC control

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Table 14-23312. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01F8h**

Figure 14-7706. GPMC_ECC_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED_207							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_207							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_207							ECCCLEAR
R							R/W1TC
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_208				ECCPOINTER			
R				R/W			
0h				0h			

Table 14-23314. GPMC_ECC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_207	R	0h	Write 0's for future compatibility. Read returns 0
8	ECCCLEAR	R/W1TC	0h	Clear all ECC result registers [Reads returns 0 - Writes 1 to this field clear all ECC result registers - Writes 0 are ignored] Reset Source: func_mod_g_arst_n
7:4	RESERVED_208	R	0h	Write 0's for future compatibility. Read returns 0
3:0	ECCPOINTER	R/W	0h	Selects ECC result register [Reads to this field give the dynamic position of the ECC pointer - Writes to this field select the ECC result register where the first ECC computation will be stored]; Other enums: Writing other values disables the ECC engine [ECCEnable bit of GPMC_ECC_CONFIG set to 0] Reset Source: func_mod_g_arst_n 0 `writing 0000 disables the ECC engine (ECCEnable bit of GPMC_ECC_CONFIG set to 0)` 1 `ECC result register 1 is selected` 2 `ECC result register 2 is selected` 3 `ECC result register 3 is selected` 4 `ECC result register 4 is selected` 5 `ECC result register 5 is selected` 6 `ECC result register 6 is selected` 7 `ECC result register 7 is selected` 8 `ECC result register 8 is selected` 9 `ECC result register 9 is selected`

14.9.3.4.2.17 GPMC_ECC_SIZE_CONFIG Register

1 GPMC_ECC_SIZE_CONFIG Register (Offset = 1FCh) [reset = FFFFF000h]

ECC size

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Table 14-23315. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 01FCh**

Figure 14-7707. GPMC_ECC_SIZE_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_210		ECCSIZE1					
R/W		R/W					
3h		FFh					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ECCSIZE1		RESERVED_211		ECCSIZE0			
R/W		R/W		R/W			
FFh		3h		FFh			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ECCSIZE0				RESERVED_209			ECC9RESULTSIZE
R/W				R			R/W
FFh				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC8RESULTSIZE	ECC7RESULTSIZE	ECC6RESULTSIZE	ECC5RESULTSIZE	ECC4RESULTSIZE	ECC3RESULTSIZE	ECC2RESULTSIZE	ECC1RESULTSIZE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-23317. GPMC_ECC_SIZE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_210	R/W	3h	Write 0's for future compatibility. Read returns 3
29:22	ECCSIZE1	R/W	FFh	Defines ECC size 1 [0x00 corresponds to 2 Bytes, 0x01 corresponds to 4 Bytes, 0x02 corresponds to 6 Bytes, 0x03 corresponds to 8 Bytes, &, 0xFF corresponds to 512 Bytes] Reset Source: func_mod_g_arst_n
21:20	RESERVED_211	R/W	3h	Write 0's for future compatibility. Read returns 3
19:12	ECCSIZE0	R/W	FFh	Defines ECC size 0 [0x00 corresponds to 2 Bytes, 0x01 corresponds to 4 Bytes, 0x02 corresponds to 6 Bytes, 0x03 corresponds to 8 Bytes, &, 0xFF corresponds to 512 Bytes] Reset Source: func_mod_g_arst_n
11:9	RESERVED_209	R	0h	Write 0's for future compatibility. Read returns 0
8	ECC9RESULTSIZE	R/W	0h	Selects ECC size for ECC 9 result register Reset Source: func_mod_g_arst_n 0 ECCSize0 is selected 1 ECCSize1 is selected

Table 14-23317. GPMC_ECC_SIZE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ECC8RESULTSIZE	R/W	0h	Selects ECC size for ECC 8 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
6	ECC7RESULTSIZE	R/W	0h	Selects ECC size for ECC 7 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
5	ECC6RESULTSIZE	R/W	0h	Selects ECC size for ECC 6 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
4	ECC5RESULTSIZE	R/W	0h	Selects ECC size for ECC 5 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
3	ECC4RESULTSIZE	R/W	0h	Selects ECC size for ECC 4 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
2	ECC3RESULTSIZE	R/W	0h	Selects ECC size for ECC 3 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
1	ECC2RESULTSIZE	R/W	0h	Selects ECC size for ECC 2 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`
0	ECC1RESULTSIZE	R/W	0h	Selects ECC size for ECC 1 result register Reset Source: func_mod_g_arst_n 0 `ECCSize0 is selected` 1 `ECCSize1 is selected`

14.9.3.4.2.18 GPMC_ECC_RESULT_j Register

1 GPMC_ECC_RESULT_j Register (Offset = 200h + formula) [reset = 0h]

ECC result register

Return to Summary Table

Offset = (j * 4h); where j = 0 to 8d

Table 14-23318. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0200h + formula**

Figure 14-7708. GPMC_ECC_RESULT_j Name Register

31	30	29	28	27	26	25	24
RESERVED_188				P2048O	P1024O	P512O	P256O
R				R	R	R	R
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
P128O	P64O	P32O	P16O	P8O	P4O	P2O	P1O
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED_187				P2048E	P1024E	P512E	P256E
R				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
P128E	P64E	P32E	P16E	P8E	P4E	P2E	P1E
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-23320. GPMC_ECC_RESULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_188	R	0h	Write 0's for future compatibility. Read returns 0
27	P2048O	R	0h	Odd Row Parity bit 2048, only used for ECC computed on 512 Bytes Reset Source: func_mod_g_arst_n
26	P1024O	R	0h	Odd Row Parity bit 1024 Reset Source: func_mod_g_arst_n
25	P512O	R	0h	Odd Row Parity bit 512 Reset Source: func_mod_g_arst_n
24	P256O	R	0h	Odd Row Parity bit 256 Reset Source: func_mod_g_arst_n
23	P128O	R	0h	Odd Row Parity bit 128 Reset Source: func_mod_g_arst_n
22	P64O	R	0h	Odd Row Parity bit 64 Reset Source: func_mod_g_arst_n
21	P32O	R	0h	Odd Row Parity bit 32 Reset Source: func_mod_g_arst_n

Table 14-23320. GPMC_ECC_RESULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	P16O	R	0h	Odd Row Parity bit 16 Reset Source: func_mod_g_arst_n
19	P8O	R	0h	Odd Row Parity bit 8 Reset Source: func_mod_g_arst_n
18	P4O	R	0h	Odd Column Parity bit 4 Reset Source: func_mod_g_arst_n
17	P2O	R	0h	Odd Column Parity bit 2 Reset Source: func_mod_g_arst_n
16	P1O	R	0h	Odd Column Parity bit 1 Reset Source: func_mod_g_arst_n
15:12	RESERVED_187	R	0h	Write 0's for future compatibility. Read returns 0
11	P2048E	R	0h	Even Row Parity bit 2048, only used for ECC computed on 512 Bytes Reset Source: func_mod_g_arst_n
10	P1024E	R	0h	Even Row Parity bit 1024 Reset Source: func_mod_g_arst_n
9	P512E	R	0h	Even Row Parity bit 512 Reset Source: func_mod_g_arst_n
8	P256E	R	0h	Even Row Parity bit 256 Reset Source: func_mod_g_arst_n
7	P128E	R	0h	Even Row Parity bit 128 Reset Source: func_mod_g_arst_n
6	P64E	R	0h	Even Row Parity bit 64 Reset Source: func_mod_g_arst_n
5	P32E	R	0h	Even Row Parity bit 32 Reset Source: func_mod_g_arst_n
4	P16E	R	0h	Even Row Parity bit 16 Reset Source: func_mod_g_arst_n
3	P8E	R	0h	Even Row Parity bit 8 Reset Source: func_mod_g_arst_n
2	P4E	R	0h	Even Column Parity bit 4 Reset Source: func_mod_g_arst_n
1	P2E	R	0h	Even Column Parity bit 2 Reset Source: func_mod_g_arst_n
0	P1E	R	0h	Even Column Parity bit 1 Reset Source: func_mod_g_arst_n

14.9.3.4.2.19 GPMC_BCH_SWDATA Register

1 GPMC_BCH_SWDATA Register (Offset = 2D0h) [reset = 0h]

This register is used to directly pass data to the BCH ECC calculator without accessing the actual NAND flash interface.

Return to Summary Table

Table 14-23321. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 02D0h**

Figure 14-7709. GPMC_BCH_SWDATA Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
BCH_DATA							
W							
0h							
7	6	5	4	3	2	1	0
BCH_DATA							
W							
0h							

Table 14-23323. GPMC_BCH_SWDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved
15:0	BCH_DATA	W	0h	Data to be included in the BCH calculation. Only bits 0 to 7 are taken into account if the calculator is configured to use 8 bits data [ECC16B = 0] Reset Source: func_mod_g_arst_n

14.9.3.4.2.20 GPMC_CONFIG1_j Register

1 GPMC_CONFIG1_j Register (Offset = 0h + formula) [reset = 0h]

The configuration 1 register sets signal control parameters per chip select

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23324. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0000h + formula**

Figure 14-7710. GPMC_CONFIG1_j Name Register

31	30	29	28	27	26	25	24
WRAPBURST	READMULTIPLE	READTYPE	WRITEMULTIPLE	WRITETYPE	CLKACTIVATIONTIME		ATTACHEDDEVICEPAGELENGTH
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		0h

23	22	21	20	19	18	17	16
ATTACHEDDEVICEPAGELENGTH	WAITREADMONITORING	WAITWRITEMONITORING	RESERVED_9	WAITMONITORINGTIME		WAITPINSELECT	
R/W	R/W	R/W	R	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED_11		DEVICESIZE		DEVICETYPE		MUXADDDATA	
R		R/W		R/W		R/W	
0h		0h		0h		0h	

7	6	5	4	3	2	1	0
RESERVED_12			TIMEPARAGRANULARITY	RESERVED_10		GPMCFCLKDIVIDER	
R			R/W	R		R/W	
0h			0h	0h		0h	

Table 14-23326. GPMC_CONFIG1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRAPBURST	R/W	0h	Enables the wrapping burst capability. Must be set if the attached device is configured in wrapping burst Reset Source: func_mod_g_arst_n 0 `Synchronous wrapping burst not supported` 1 `Synchronous wrapping burst supported`
30	READMULTIPLE	R/W	0h	Selects the read single or multiple access Reset Source: func_mod_g_arst_n 0 `single access` 1 `multiple access (burst if synchonous, page if asynchronous)`
29	READTYPE	R/W	0h	Selects the read mode operation Reset Source: func_mod_g_arst_n 0 `Read Asynchronous` 1 `Read Synchronous`

Table 14-23326. GPMC_CONFIG1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	WRITEMULTIPLE	R/W	0h	Selects the write single or multiple access Reset Source: func_mod_g_arst_n 0 single access 1 multiple access (burst if synchonous, considered as single if asynchronous)
27	WRITETYPE	R/W	0h	Selects the write mode operation Reset Source: func_mod_g_arst_n 0 Write Asynchronous 1 Write Synchronous
26:25	CLKACTIVATIONTIME	R/W	0h	Output GPMC.CLK activation time Reset Source: func_mod_g_arst_n 0 First rising edge of GPMC.CLK at Start Access Time 1 First rising edge of GPMC.CLK one GPMC.FCLK cycle after Start Access Time 2 First rising edge of GPMC.CLK two GPMC.FCLK cycles after Start Access Time 3 not defined
24:23	ATTACHEDDEVICEPAGE LENGTH	R/W	0h	Specifies the attached device page [burst] length Reset Source: func_mod_g_arst_n 0 4 Words 1 8 Words 2 16 Words 3 32 Words
22	WAITREADMONITORING	R/W	0h	Selects the Wait monitoring configuration for Read accesses [Reset value is BOOTWAITEN input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 0 Wait pin is not monitored for read accesses 1 Wait pin is monitored for read accesses
21	WAITWRITEMONITORIN G	R/W	0h	Selects the Wait monitoring configuration for Write accesses Reset Source: func_mod_g_arst_n 0 Wait pin is not monitored for write accesses 1 Wait pin is monitored for write accesses
20	RESERVED_9	R	0h	Write 0's for future compatibility. Read returns 0
19:18	WAITMONITORINGTIME	R/W	0h	Selects input pin Wait monitoring time Reset Source: func_mod_g_arst_n 0 Wait pin is monitored with valid data 1 Wait pin is monitored one GPMC.CLK cycle before valid data 2 Wait pin is monitored two GPMC.CLK cycle before valid data 3 not defined
17:16	WAITPINSELECT	R/W	0h	Selects the input WAIT pin for this chip select [Reset value is BOOTWAITSELECT input pin sampled at IC reset for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 0 Wait input pin is WAIT0 1 Wait input pin is WAIT1 2 Wait input pin is WAIT2 3 Wait input pin is WAIT3
15:14	RESERVED_11	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-23326. GPMC_CONFIG1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	DEVICESIZE	R/W	0h	Selects the device size attached [Reset value is BOOTDEVICESIZE input pin sampled at IC reset for CS0 and 01 for CS1-7] Reset Source: func_mod_g_arst_n 0 8 bit 1 16 bit 2 32 bit 3 reserved
11:10	DEVICETYPE	R/W	0h	Selects the attached device type Reset Source: func_mod_g_arst_n 0 NOR Flash, pSRAM, asynchronous devices 1 reserved 2 NAND Flash stream mode 3 reserved
9:8	MUXADDDATA	R/W	0h	Enables the Address and data multiplexed protocol [Reset value is CS0MUXDEVICE input pin sampled at IC reset for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 0 Non Multiplexed attached device 1 AAD-Mux protocol device 2 Address and data multiplexed attached device 3 Reserved
7:5	RESERVED_12	R	0h	Write 0's for future compatibility. Read returns 0
4	TIMEPARAGRANULARITY	R/W	0h	Signals timing latencies scalar factor [Rd/WRCycleTime, AccessTime, PageBurstAccessTime, CSOnTime, CSRd/WrOffTime, ADVOnTime, ADVRd/WrOffTime, OEOnTime, OEOffTime, WEOnTime, WEOffTime, Cycle2CycleDelay, BusTurnAround, TimeOutStartValue] Reset Source: func_mod_g_arst_n 0 x1 latencies 1 x2 latencies
3:2	RESERVED_10	R	0h	Write 0's for future compatibility. Read returns 0
1:0	GPMCFCLKDIVIDER	R/W	0h	Divides the GPMC.FCLK clock Reset Source: func_mod_g_arst_n 0 GPMC.CLK frequency = GPMC.FCLK frequency 1 GPMC.CLK frequency = GPMC.FCLK frequency / 2 2 GPMC.CLK frequency = GPMC.FCLK frequency / 3 3 GPMC.CLK frequency = GPMC.FCLK frequency /4

14.9.3.4.2.21 GPMC_CONFIG2_j Register

1 GPMC_CONFIG2_j Register (Offset = 4h + formula) [reset = 101001h]

Chip-select signal timing parameter configuration

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23327. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0004h + formula

Figure 14-7711. GPMC_CONFIG2_j Name Register

31	30	29	28	27	26	25	24
RESERVED_43							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_43			CSWROFFTIME				
R			R/W				
0h			10h				
15	14	13	12	11	10	9	8
RESERVED_45			CSRDOFFTIME				
R			R/W				
0h			10h				
7	6	5	4	3	2	1	0
CSEXTRADELAY	RESERVED_44			CSONTIME			
R/W	R			R/W			
0h	0h			1h			

Table 14-23329. GPMC_CONFIG2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED_43	R	0h	Write 0's for future compatibility Reads returns 0
20:16	CSWROFFTIME	R/W	10h	CS# de-assertion time from start cycle time for write accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED_45	R	0h	Write 0's for future compatibility. Read returns 0
12:8	CSRDOFFTIME	R/W	10h	CS# de-assertion time from start cycle time for read accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7	CSEXTRADELAY	R/W	0h	CS# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 0 CS# Timing control signal is not delayed 1 CS# Timing control signal is delayed of half GPMC.FCLK clock cycle
6:4	RESERVED_44	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-23329. GPMC_CONFIG2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CSONTIME	R/W	1h	CS# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.3.4.2.22 GPMC_CONFIG3_j Register

1 GPMC_CONFIG3_j Register (Offset = 8h + formula) [reset = 22060514h]

ADV# signal timing parameter configuration

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23330. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0008h + formula**

Figure 14-7712. GPMC_CONFIG3_j Name Register

31	30	29	28	27	26	25	24
RESERVED_1	ADVAADMUXWROFFTIME			RESERVED_0	ADVAADMUXRDOFFTIME		
R	R/W			R	R/W		
0h	2h			0h	2h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_68			ADVWROFFTIME				
R			R/W				
0h			6h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_69			ADVRDOFFTIME				
R			R/W				
0h			5h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADVEXTRADELAY	ADVAADMUXONTIME			ADVONTIME			
R/W	R/W			R/W			
0h	1h			4h			

Table 14-23332. GPMC_CONFIG3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_1	R	0h	Write 0's for future compatibility. Read returns 0
30:28	ADVAADMUXWROFFTIME	R/W	2h	ADV# de-assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n
27	RESERVED_0	R	0h	Write 0's for future compatibility. Read returns 0
26:24	ADVAADMUXRDOFFTIME	R/W	2h	ADV# assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n
23:21	RESERVED_68	R	0h	Write 0's for future compatibility. Read returns 0
20:16	ADVWROFFTIME	R/W	6h	ADV# de-assertion time from start cycle time for write accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED_69	R	0h	Write 0's for future compatibility. Read returns 0
12:8	ADVRDOFFTIME	R/W	5h	ADV# de-assertion time from start cycle time for read accesses[0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

Table 14-23332. GPMC_CONFIG3_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ADVEXTRADELAY	R/W	0h	ADV# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 0 ADV# Timing control signal is not delayed 1 ADV# Timing control signal is delayed of half GPMC.FCLK clock cycle
6:4	ADVAADMUXONTIME	R/W	1h	ADV# assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n
3:0	ADVONTIME	R/W	4h	ADV# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.3.4.2.23 GPMC_CONFIG4_j Register

1 GPMC_CONFIG4_j Register (Offset = Ch + formula) [reset = 10057016h]

WE# and OE# signals timing parameter configuration

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23333. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 000Ch + formula**

Figure 14-7713. GPMC_CONFIG4_j Name Register

31	30	29	28	27	26	25	24
RESERVED			WEOFFTIME				
R			R/W				
0h			10h				
23	22	21	20	19	18	17	16
WEEXTRADELAY	RESERVED_92			WEONTIME			
R/W	R			R/W			
0h	0h			5h			
15	14	13	12	11	10	9	8
OEAADMUXOFFTIME			OEOFFTIME				
R/W			R/W				
3h			10h				
7	6	5	4	3	2	1	0
OEEXTRADELAY	OEAADMUXONTIME			OEONTIME			
R/W	R/W			R/W			
0h	1h			6h			

Table 14-23335. GPMC_CONFIG4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	R	0h	Write 0's for future compatibility. Read returns 0
28:24	WEOFFTIME	R/W	10h	WE# de-assertion time from start cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23	WEEXTRADELAY	R/W	0h	WE# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 0 WE# Timing control signal is not delayed 1 WE# Timing control signal is delayed of half GPMC.FCLK clock cycle
22:20	RESERVED_92	R	0h	Write 0's for future compatibility. Read returns 0
19:16	WEONTIME	R/W	5h	WE# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

Table 14-23335. GPMC_CONFIG4_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	OEAADMUXOFFTIME	R/W	3h	OE# de-assertion time for the first address phase in an AAD-Mux access Reset Source: func_mod_g_arst_n
12:8	OEOFFTIME	R/W	10h	OE# de-assertion time from start cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7	OEEXTRADELAY	R/W	0h	OE# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 0 OE# Timing control signal is not delayed 1 OE# Timing control signal is delayed of half GPMC.FCLK clock cycle
6:4	OEAADMUXONTIME	R/W	1h	OE# assertion time for the first address phase in an AAD-Mux access Reset Source: func_mod_g_arst_n
3:0	OEONTIME	R/W	6h	OE# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.3.4.2.24 GPMC_CONFIG5_j Register

1 GPMC_CONFIG5_j Register (Offset = 10h + formula) [reset = 10F1111h]

RdAccessTime and CycleTime timing parameters configuration

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23336. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0010h + formula**

Figure 14-7714. GPMC_CONFIG5_j Name Register

31	30	29	28	27	26	25	24
RESERVED_124				PAGEBURSTACCESSTIME			
R				R/W			
0h				1h			
23	22	21	20	19	18	17	16
RESERVED_125			RDACCESSTIME				
R			R/W				
0h			Fh				
15	14	13	12	11	10	9	8
RESERVED_126			WRCYCLETIME				
R			R/W				
0h			11h				
7	6	5	4	3	2	1	0
RESERVED_123			RDCYCLETIME				
R			R/W				
0h			11h				

Table 14-23338. GPMC_CONFIG5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_124	R	0h	Write 0's for future compatibility. Read returns 0
27:24	PAGEBURSTACCESSTIME	R/W	1h	Delay between successive words in a multiple access [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23:21	RESERVED_125	R	0h	Write 0's for future compatibility. Read returns 0
20:16	RDACCESSTIME	R/W	Fh	Delay between start cycle time and first data valid [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED_126	R	0h	Write 0's for future compatibility Reads returns 0
12:8	WRCYCLETIME	R/W	11h	Total write cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7:5	RESERVED_123	R	0h	Write 0's for future compatibility. Read returns 0

Table 14-23338. GPMC_CONFIG5_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	RDCYCLETIME	R/W	11h	Total read cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.3.4.2.25 GPMC_CONFIG6_j Register

1 GPMC_CONFIG6_j Register (Offset = 14h + formula) [reset = 8F070000h]

WrAccessTime, WrDataOnADmuxBus, Cycle2Cycle and BusTurnAround parameters configuration

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23339. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0014h + formula

Figure 14-7715. GPMC_CONFIG6_j Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED_0		WRACCESSTIME				
R/W	R		R/W				
1h	0h		Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_155				WRDATAONADMUXBUS			
R				R/W			
0h				7h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				CYCLE2CYCLEDELAY			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CYCLE2CYCLESAMECSEN	CYCLE2CYCLEDIFFCSEN	RESERVED_156		BUSTURNAROUND			
R/W	R/W	R		R/W			
0h	0h	0h		0h			

Table 14-23341. GPMC_CONFIG6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	1h	TI Internal use - Do not modify
30:29	RESERVED_0	R	0h	Write 0's for future compatibility. Read returns 0
28:24	WRACCESSTIME	R/W	Fh	Delay from StartAccessTime to the GPMC.FCLK rising edge corresponding the the GPMC.CLK rising edge used by the attached memory for the first data capture [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23:20	RESERVED_155	R	0h	Write 0's for future compatibility. Read returns 0
19:16	WRDATAONADMUXBUS	R/W	7h	Specifies on which GPMC.FCLK rising edge the first data of the synchronous burst write is driven in the add/data mux bus Reset Source: func_mod_g_arst_n
15:12	RESERVED_1	R	0h	Write 0's for future compatibility. Read returns 0
11:8	CYCLE2CYCLEDELAY	R/W	0h	Chip select high pulse delay between two successive accesses [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

Table 14-23341. GPMC_CONFIG6_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CYCLE2CYCLESAMECSEN	R/W	0h	Add Cycle2CycleDelay between two successive accesses to the same chip-select [any access type] Reset Source: func_mod_g_arst_n 0 `No delay between the two accesses` 1 `Add Cycle2CycleDelay`
6	CYCLE2CYCLEDIFFCSEN	R/W	0h	Add Cycle2CycleDelay between two successive accesses to a different chip-select [any access type] Reset Source: func_mod_g_arst_n 0 `No delay between the two accesses` 1 `Add Cycle2CycleDelay`
5:4	RESERVED_156	R	0h	Write 0's for future compatibility Reads returns 0
3:0	BUSTURNAROUND	R/W	0h	Bus turn around latency between two successive accesses to the same chip-select [rd to wr] or to a different chip-select [read to read and read to write] [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

14.9.3.4.2.26 GPMC_CONFIG7_j Register

1 GPMC_CONFIG7_j Register (Offset = 18h + formula) [reset = F40h]

Chip-select address mapping configuration Note: For CS0, the register reset is 0xf40 while for all the other instances CS1-CS7, the reset is 0xf00.

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23342. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0018h + formula**

Figure 14-7716. GPMC_CONFIG7_j Name Register

31	30	29	28	27	26	25	24
RESERVED_171							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_171							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_171				MASKADDRESS			
R				R/W			
0h				Fh			
7	6	5	4	3	2	1	0
RESERVED_172	CSVALID	BASEADDRESS					
R	R/W	R/W					
0h	1h	0h					

Table 14-23344. GPMC_CONFIG7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_171	R	0h	Write 0's for future compatibility. Read returns 0
11:8	MASKADDRESS	R/W	Fh	Chip-select mask address Reset Source: func_mod_g_arst_n
7	RESERVED_172	R	0h	Write 0's for future compatibility. Read returns 0
6	CSVALID	R/W	1h	Chip-select enable [reset value is 1 for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 0 Chip-select disabled 1 Chip-select enabled
5:0	BASEADDRESS	R/W	0h	Chip-select base address Reset Source: func_mod_g_arst_n

14.9.3.4.2.27 GPMC_NAND_COMMAND_j Register

1 GPMC_NAND_COMMAND_j Register (Offset = 1Ch + formula) [reset = 0h]

This Register is not a true register, just a address location.

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23345. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 001Ch + formula**

Figure 14-7717. GPMC_NAND_COMMAND_j Name Register

31	30	29	28	27	26	25	24
GPMC_NAND_COMMAND_0							
W							
0h							
23	22	21	20	19	18	17	16
GPMC_NAND_COMMAND_0							
W							
0h							
15	14	13	12	11	10	9	8
GPMC_NAND_COMMAND_0							
W							
0h							
7	6	5	4	3	2	1	0
GPMC_NAND_COMMAND_0							
W							
0h							

Table 14-23347. GPMC_NAND_COMMAND_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_COMMAND_0	W	0h	Reset Source: func_mod_g_arst_n

14.9.3.4.2.28 GPMC_NAND_ADDRESS_j Register

1 GPMC_NAND_ADDRESS_j Register (Offset = 20h + formula) [reset = 0h]

This Register is not a true register, just a address location.

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23348. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0020h + formula**

Figure 14-7718. GPMC_NAND_ADDRESS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GPMC_NAND_ADDRESS_0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GPMC_NAND_ADDRESS_0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GPMC_NAND_ADDRESS_0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GPMC_NAND_ADDRESS_0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23350. GPMC_NAND_ADDRESS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_ADDRESS_0	W	0h	Reset Source: func_mod_g_arst_n

14.9.3.4.2.29 GPMC_NAND_DATA_j Register

1 GPMC_NAND_DATA_j Register (Offset = 24h + formula) [reset = 0h]

This Register is not a true register, just a address location.

Return to Summary Table

Offset = (j * 30h); where j = 0 to 7d

Table 14-23351. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0024h + formula

Figure 14-7719. GPMC_NAND_DATA_j Name Register

31	30	29	28	27	26	25	24
GPMC_NAND_DATA_0							
R/W							
0h							
23	22	21	20	19	18	17	16
GPMC_NAND_DATA_0							
R/W							
0h							
15	14	13	12	11	10	9	8
GPMC_NAND_DATA_0							
R/W							
0h							
7	6	5	4	3	2	1	0
GPMC_NAND_DATA_0							
R/W							
0h							

Table 14-23353. GPMC_NAND_DATA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_DATA_0	R/W	0h	Reset Source: func_mod_g_arst_n

14.9.3.4.2.30 GPMC_BCH_RESULT_0_j Register

1 GPMC_BCH_RESULT_0_j Register (Offset = 0h + formula) [reset = 0h]

BCH ECC result, bits 0 to 31

Return to Summary Table

Offset = (j * 10h); where j = 0 to 7d

Table 14-23354. Instance Table

Instance Name	Physical Address
GPMC0	3B00 0000h + formula

Figure 14-7720. GPMC_BCH_RESULT_0_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BCH_RESULT_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BCH_RESULT_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BCH_RESULT_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BCH_RESULT_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-23356. GPMC_BCH_RESULT_0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_0	R	0h	BCH ECC result, bits 0 to 31 Reset Source: func_mod_g_arst_n

14.9.3.4.2.31 GPMC_BCH_RESULT_1_j Register

1 GPMC_BCH_RESULT_1_j Register (Offset = 4h + formula) [reset = 0h]

BCH ECC result, bits 32 to 63

Return to Summary Table

Offset = (j * 10h); where j = 0 to 7d

Table 14-23357. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0004h + formula**

Figure 14-7721. GPMC_BCH_RESULT_1_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BCH_RESULT_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCH_RESULT_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BCH_RESULT_1							
R							
0h							

Table 14-23359. GPMC_BCH_RESULT_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_1	R	0h	BCH ECC result, bits 32 to 63 Reset Source: func_mod_g_arst_n

14.9.3.4.2.32 GPMC_BCH_RESULT_2_j Register

1 GPMC_BCH_RESULT_2_j Register (Offset = 8h + formula) [reset = 0h]

BCH ECC result, bits 64 to 95

Return to Summary Table

Offset = (j * 10h); where j = 0 to 7d

Table 14-23360. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0008h + formula**

Figure 14-7722. GPMC_BCH_RESULT_2_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_2							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_2							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_2							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_2							
R							
0h							

Table 14-23362. GPMC_BCH_RESULT_2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_2	R	0h	BCH ECC result, bits 64 to 95 Reset Source: func_mod_g_arst_n

14.9.3.4.2.33 GPMC_BCH_RESULT_3_j Register

1 GPMC_BCH_RESULT_3_j Register (Offset = Ch + formula) [reset = 0h]

BCH ECC result, bits 96 to 127

Return to Summary Table

Offset = (j * 10h); where j = 0 to 7d

Table 14-23363. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 000Ch + formula**

Figure 14-7723. GPMC_BCH_RESULT_3_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_3							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_3							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_3							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_3							
R							
0h							

Table 14-23365. GPMC_BCH_RESULT_3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_3	R	0h	BCH ECC result, bits 96 to 127 Reset Source: func_mod_g_arst_n

14.9.3.4.2.34 GPMC_BCH_RESULT_4_j Register

1 GPMC_BCH_RESULT_4_j Register (Offset = 0h + formula) [reset = 0h]

BCH ECC result, bits 128 to 159

Return to Summary Table

Offset = (j * 10h); where j = 0 to 7d

Table 14-23366. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0000h + formula**

Figure 14-7724. GPMC_BCH_RESULT_4_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_4							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_4							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_4							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_4							
R							
0h							

Table 14-23368. GPMC_BCH_RESULT_4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_4	R	0h	BCH ECC result, bits 128 to 159 Reset Source: func_mod_g_arst_n

14.9.3.4.2.35 GPMC_BCH_RESULT_5_j Register

1 GPMC_BCH_RESULT_5_j Register (Offset = 4h + formula) [reset = 0h]

BCH ECC result, bits 160 to 191

Return to Summary Table

Offset = (j * 10h); where j = 0 to 7d

Table 14-23369. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0004h + formula**

Figure 14-7725. GPMC_BCH_RESULT_5_j Name Register

31	30	29	28	27	26	25	24
BCH_RESULT_5							
R							
0h							
23	22	21	20	19	18	17	16
BCH_RESULT_5							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_5							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_5							
R							
0h							

Table 14-23371. GPMC_BCH_RESULT_5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_5	R	0h	BCH ECC result, bits 160 to 191 Reset Source: func_mod_g_arst_n

14.9.3.4.2.36 GPMC_BCH_RESULT_6_j Register

1 GPMC_BCH_RESULT_6_j Register (Offset = 8h + formula) [reset = 0h]

BCH ECC result, bits 192 to 207

Return to Summary Table

Offset = (j * 10h); where j = 0 to 7d

Table 14-23372. Instance Table

Instance Name	Physical Address
GPMC0	**3B00 0008h + formula**

Figure 14-7726. GPMC_BCH_RESULT_6_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
BCH_RESULT_6							
R							
0h							
7	6	5	4	3	2	1	0
BCH_RESULT_6							
R							
0h							

Table 14-23374. GPMC_BCH_RESULT_6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved
15:0	BCH_RESULT_6	R	0h	BCH ECC result, bits 192 to 207 Reset Source: func_mod_g_arst_n

14.9.3.5 ELM Registers

Table 14-15650 lists the memory-mapped registers for the ELM. All register offset addresses not listed in Table 14-15650 should be considered as reserved locations and the register contents should not be modified.

Table 14-23375. ELM Instances

Instance	Base Address
ELM0	2501 0000h

Table 14-23376. ELM Registers

Offset	Acronym	Register Name	ELM0 Physical Address
0h	ELM_REVISION	IP revision	2501 0000h
10h	ELM_SYSCONFIG	Module software reset and local power management register	2501 0010h
14h	ELM_SYSSTATUS	Internal reset monitoring	2501 0014h
18h	ELM_IRQSTATUS	Interrupt status register	2501 0018h
1Ch	ELM_IRQENABLE	Interrupt enable register	2501 001Ch
20h	ELM_LOCATION_CONFIG	ECC algorithm parameters	2501 0020h
80h	ELM_PAGE_CTRL	Page definition	2501 0080h
400h + formula	ELM_SYNDROME_FRAGMENT_0_i	Input syndrome polynomial bits 0 to 31	2501 0400h + formula
404h + formula	ELM_SYNDROME_FRAGMENT_1_i	Input syndrome polynomial bits 32 to 63	2501 0404h + formula
408h + formula	ELM_SYNDROME_FRAGMENT_2_i	Input syndrome polynomial bits 64 to 95	2501 0408h + formula
40Ch + formula	ELM_SYNDROME_FRAGMENT_3_i	Input syndrome polynomial bits 96 to 127	2501 040Ch + formula
410h + formula	ELM_SYNDROME_FRAGMENT_4_i	Input syndrome polynomial bits 128 to 159	2501 0410h + formula
414h + formula	ELM_SYNDROME_FRAGMENT_5_i	Input syndrome polynomial bits 160 to 191	2501 0414h + formula
418h + formula	ELM_SYNDROME_FRAGMENT_6_i	Input syndrome polynomial bits 192 to 207	2501 0418h + formula
800h + formula	ELM_LOCATION_STATUS_i	Exit status for the syndrome polynomial processing	2501 0800h + formula
880h + formula	ELM_ERROR_LOCATION_0_i	Error-location register 0	2501 0880h + formula
884h + formula	ELM_ERROR_LOCATION_1_i	Error-location register 1	2501 0884h + formula
888h + formula	ELM_ERROR_LOCATION_2_i	Error-location register 2	2501 0888h + formula
88Ch + formula	ELM_ERROR_LOCATION_3_i	Error-location register 3	2501 088Ch + formula
890h + formula	ELM_ERROR_LOCATION_4_i	Error-location register 4	2501 0890h + formula
894h + formula	ELM_ERROR_LOCATION_5_i	Error-location register 5	2501 0894h + formula
898h + formula	ELM_ERROR_LOCATION_6_i	Error-location register 6	2501 0898h + formula
89Ch + formula	ELM_ERROR_LOCATION_7_i	Error-location register 7	2501 089Ch + formula
8A0h + formula	ELM_ERROR_LOCATION_8_i	Error-location register 8	2501 08A0h + formula
8A4h + formula	ELM_ERROR_LOCATION_9_i	Error-location register 9	2501 08A4h + formula
8A8h + formula	ELM_ERROR_LOCATION_10_i	Error-location register 10	2501 08A8h + formula
8ACh + formula	ELM_ERROR_LOCATION_11_i	Error-location register 11	2501 08ACh + formula
8B0h + formula	ELM_ERROR_LOCATION_12_i	Error-location register 12	2501 08B0h + formula
8B4h + formula	ELM_ERROR_LOCATION_13_i	Error-location register 13	2501 08B4h + formula
8B8h + formula	ELM_ERROR_LOCATION_14_i	Error-location register 14	2501 08B8h + formula
8BCh + formula	ELM_ERROR_LOCATION_15_i	Error-location register 15	2501 08BCh + formula

1 ELM_REVISION Register (Offset = 0h) [reset = 20h]

ELM_REVISION is shown in Figure 14-7727 and described in Table 14-15652.

This register contains the IP revision code.
(A write to or reset of this register has no effect.)

Table 14-23377. ELM_REVISION Instances

Instance	Physical Address
ELM0	2501 0000h

Figure 14-7727. ELM_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-20h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23379. ELM_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	20h	TI internal data. Identifies revision of peripheral.

2 ELM_SYSCONFIG Register (Offset = 10h) [reset = 11h]

ELM_SYSCONFIG is shown in Figure 14-7728 and described in Table 14-15654.

This register controls ELM local power management and software reset.

Note

Some of the ELM features described in this section may not be supported on this family of devices. For more information, see *ELM Not Supported Features*.

Table 14-23380. ELM_SYSCONFIG Instances

Instance	Physical Address
ELM0	2501 0010h

Figure 14-7728. ELM_SYSCONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CLOCKACTIVITYOCP
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SIDLEMODE		RESERVED	SOFTRESET	AUTOGATING
R-0h			R/W-2h		R-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-23382. ELM_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CLOCKACTIVITYOCP	R/W	0h	ELM_FICLK activity when module is in IDLE mode 0h (R/W) = ELM_FICLK can be switched off. 1h (R/W) = ELM_FICLK is maintained.
7-5	RESERVED	R	0h	Reserved
4-3	SIDLEMODE	R/W	2h	Slave interface power management (clock stop req/ack control) 0h (R/W) = Force-idle. A clock stop request is acknowledged unconditionally and immediately 1h (R/W) = No-idle. A clock stop request is never acknowledged. 2h (R/W) = Smart-idle. The acknowledgment to a clock stop request is given based on the internal activity. 3h (R/W) = Reserved — do not use

Table 14-23382. ELM_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R	0h	Reserved
1	SOFTRESET	R/W	0h	Module software reset This bit is automatically reset by hardware (during reads, it always returns 0). It has same effect as ELM_RST. 0h (R/W) = Normal mode 1h (R/W) = Start soft reset sequence.
0	AUTOGATING	R/W	1h	Internal ELM_FICLK gating strategy (no module visible effect other than saving power) 0h (R/W) = ELM_FICLK is free-running. 1h (R/W) = Automatic internal ELM_FICLK gating strategy is applied based on the Interconnect interface activity.

3 ELM_SYSSTATUS Register (Offset = 14h) [reset = 0h]

ELM_SYSSTATUS is shown in Figure 14-7729 and described in Table 14-15656.

Internal reset monitoring
Undefined since:
From hardware perspective, the reset state is 0.
From software user perspective, when the accessible module is 1.

Table 14-23383. ELM_SYSSTATUS Instances

Instance	Physical Address
ELM0	2501 0014h

Figure 14-7729. ELM_SYSSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R-0h							R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23385. ELM_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RESETDONE	R	0h	Internal reset monitoring Undefined since: From hardware perspective, the reset state is 0. From software user perspective, when the accessible module is 1. 0h (R) = Reset is ongoing. 1h (R) = Reset is done (completed).

4 ELM_IRQSTATUS Register (Offset = 18h) [reset = 0h]

ELM_IRQSTATUS is shown in Figure 14-7730 and described in Table 14-15658.

Interrupt status. This register doubles as a status register for the error-location processes.

Table 14-23386. ELM_IRQSTATUS Instances

Instance	Physical Address
ELM0	2501 0018h

Figure 14-7730. ELM_IRQSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							PAGE_VALID
R-0h							R/W1C-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOC_VALID_7	LOC_VALID_6	LOC_VALID_5	LOC_VALID_4	LOC_VALID_3	LOC_VALID_2	LOC_VALID_1	LOC_VALID_0
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-23388. ELM_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	PAGE_VALID	R/W1C	0h	Error-location status for a full page, based on the mask definition Read 0h = Error locations invalid for all polynomials enabled in the ECC_INTERRUPT_MASK register Read 1h = All error locations valid Write 0h = No effect Write 1h = Clear interrupt
7	LOC_VALID_7	R/W1C	0h	Error-location status for syndrome polynomial 7 Read 0h = No syndrome processed or process in progress Read 1h = Error-location process completed Write 0h = No effect Write 1h = Clear interrupt
6	LOC_VALID_6	R/W1C	0h	Error-location status for syndrome polynomial 6
5	LOC_VALID_5	R/W1C	0h	Error-location status for syndrome polynomial 5
4	LOC_VALID_4	R/W1C	0h	Error-location status for syndrome polynomial 4
3	LOC_VALID_3	R/W1C	0h	Error-location status for syndrome polynomial 3
2	LOC_VALID_2	R/W1C	0h	Error-location status for syndrome polynomial 2

Table 14-23388. ELM_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LOC_VALID_1	R/W1C	0h	Error-location status for syndrome polynomial 1
0	LOC_VALID_0	R/W1C	0h	Error-location status for syndrome polynomial 0

5 ELM_IRQENABLE Register (Offset = 1Ch) [reset = 0h]

ELM_IRQENABLE is shown in Figure 14-7731 and described in Table 14-15660.

Interrupt enable.

Table 14-23389. ELM_IRQENABLE Instances

Instance	Physical Address
ELM0	2501 001Ch

Figure 14-7731. ELM_IRQENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							PAGE_MASK
R-0h							R/W-0h
7	6	5	4	3	2	1	0
LOCATION_MASK_7	LOCATION_MASK_6	LOCATION_MASK_5	LOCATION_MASK_4	LOCATION_MASK_3	LOCATION_MASK_2	LOCATION_MASK_1	LOCATION_MASK_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23391. ELM_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	PAGE_MASK	R/W	0h	Page interrupt mask bit 0h = Disable interrupt 1h = Enable interrupt
7	LOCATION_MASK_7	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 7
6	LOCATION_MASK_6	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 6
5	LOCATION_MASK_5	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 5
4	LOCATION_MASK_4	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 4
3	LOCATION_MASK_3	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 3
2	LOCATION_MASK_2	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 2
1	LOCATION_MASK_1	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 1
0	LOCATION_MASK_0	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 0 0h = Disable interrupt 1h = Enable interrupt

6 ELM_LOCATION_CONFIG Register (Offset = 20h) [reset = 0h]

ELM_LOCATION_CONFIG is shown in Figure 14-7732 and described in Table 14-15662.

ECC algorithm parameters.

Table 14-23392. ELM_LOCATION_CONFIG Instances

Instance	Physical Address
ELM0	2501 0020h

Figure 14-7732. ELM_LOCATION_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED					ECC_SIZE		
R-0h					R/W-0h		
23	22	21	20	19	18	17	16
ECC_SIZE							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						ECC_BCH_LEVEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23394. ELM_LOCATION_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-16	ECC_SIZE	R/W	0h	Maximum size of the buffers for which the error-location engine is used, in number of nibbles (4-bit entities)
15-2	RESERVED	R	0h	Reserved
1-0	ECC_BCH_LEVEL	R/W	0h	Error correction level 0h = 4 bits 1h = 8 bits 2h = 16 bits 3h = Reserved

7 ELM_PAGE_CTRL Register (Offset = 80h) [reset = 0h]

ELM_PAGE_CTRL is shown in Figure 14-7733 and described in Table 14-15664.

Page definition.

Table 14-23395. ELM_PAGE_CTRL Instances

Instance	Physical Address
ELM0	2501 0080h

Figure 14-7733. ELM_PAGE_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SECTOR_7	SECTOR_6	SECTOR_5	SECTOR_4	SECTOR_3	SECTOR_2	SECTOR_1	SECTOR_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23397. ELM_PAGE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	SECTOR_7	R/W	0h	Set to 1 if syndrome polynomial 7 is part of the page in page mode. Must be 0 in continuous mode.
6	SECTOR_6	R/W	0h	Set to 1 if syndrome polynomial 6 is part of the page in page mode. Must be 0 in continuous mode.
5	SECTOR_5	R/W	0h	Set to 1 if syndrome polynomial 5 is part of the page in page mode. Must be 0 in continuous mode.
4	SECTOR_4	R/W	0h	Set to 1 if syndrome polynomial 4 is part of the page in page mode. Must be 0 in continuous mode.
3	SECTOR_3	R/W	0h	Set to 1 if syndrome polynomial 3 is part of the page in page mode. Must be 0 in continuous mode.
2	SECTOR_2	R/W	0h	Set to 1 if syndrome polynomial 2 is part of the page in page mode. Must be 0 in continuous mode.
1	SECTOR_1	R/W	0h	Set to 1 if syndrome polynomial 1 is part of the page in page mode. Must be 0 in continuous mode.
0	SECTOR_0	R/W	0h	Set to 1 if syndrome polynomial 0 is part of the page in page mode. Must be 0 in continuous mode.

8 ELM_SYNDROME_FRAGMENT_0_i Register (Offset = 400h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_0_i (where i = 0 to 7) is shown in Figure 14-7734 and described in Table 14-15666.

Input syndrome polynomial bits 0 to 31.

Offset = 400h + (i * 40h), where: i = 0 to 7

Table 14-23398. ELM_SYNDROME_FRAGMENT_0_i Instances

Instance	Physical Address
ELM0	2501 0400h + formula

Figure 14-7734. ELM_SYNDROME_FRAGMENT_0_i Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">SYNDROME_0</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23400. ELM_SYNDROME_FRAGMENT_0_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_0	R/W	0h	Syndrome bits 0 to 31

9 ELM_SYNDROME_FRAGMENT_1_i Register (Offset = 404h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_1_i (where i = 0 to 7) is shown in Figure 14-7735 and described in Table 14-15668.

Input syndrome polynomial bits 32 to 63.

Offset = 404h + (i * 40h), where: i = 0 to 7

Table 14-23401. ELM_SYNDROME_FRAGMENT_1_i Instances

Instance	Physical Address
ELM0	2501 0404h + formula

Figure 14-7735. ELM_SYNDROME_FRAGMENT_1_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23403. ELM_SYNDROME_FRAGMENT_1_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_1	R/W	0h	Syndrome bits 32 to 63

10 ELM_SYNDROME_FRAGMENT_2_i Register (Offset = 408h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_2_i (where i = 0 to 7) is shown in Figure 14-7736 and described in Table 14-15670.

Input syndrome polynomial bits 64 to 95.

Offset = 408h + (i * 40h), where: i = 0 to 7

Table 14-23404. ELM_SYNDROME_FRAGMENT_2_i Instances

Instance	Physical Address
ELM0	2501 0408h + formula

Figure 14-7736. ELM_SYNDROME_FRAGMENT_2_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23406. ELM_SYNDROME_FRAGMENT_2_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_2	R/W	0h	Syndrome bits 64 to 95

11 ELM_SYNDROME_FRAGMENT_3_i Register (Offset = 40Ch + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_3_i (where i = 0 to 7) is shown in Figure 14-7737 and described in Table 14-15672.

Input syndrome polynomial bits 96 to 127.

Offset = 40Ch + (i * 40h), where: i = 0 to 7

Table 14-23407. ELM_SYNDROME_FRAGMENT_3_i Instances

Instance	Physical Address
ELM0	2501 040Ch + formula

Figure 14-7737. ELM_SYNDROME_FRAGMENT_3_i Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">SYNDROME_3</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23409. ELM_SYNDROME_FRAGMENT_3_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_3	R/W	0h	Syndrome bits 96 to 127

12 ELM_SYNDROME_FRAGMENT_4_i Register (Offset = 410h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_4_i (where i = 0 to 7) is shown in Figure 14-7738 and described in Table 14-15674.

Input syndrome polynomial bits 128 to 159.

Offset = 410h + (i * 40h), where: i = 0 to 7

Table 14-23410. ELM_SYNDROME_FRAGMENT_4_i Instances

Instance	Physical Address
ELM0	2501 0410h + formula

Figure 14-7738. ELM_SYNDROME_FRAGMENT_4_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_4																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23412. ELM_SYNDROME_FRAGMENT_4_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_4	R/W	0h	Syndrome bits 128 to 159

13 ELM_SYNDROME_FRAGMENT_5_i Register (Offset = 414h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_5_i (where i = 0 to 7) is shown in Figure 14-7739 and described in Table 14-15676.

Input syndrome polynomial bits 160 to 191.

Offset = 414h + (i * 40h), where: i = 0 to 7

Table 14-23413. ELM_SYNDROME_FRAGMENT_5_i Instances

Instance	Physical Address
ELM0	2501 0414h + formula

Figure 14-7739. ELM_SYNDROME_FRAGMENT_5_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_5																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23415. ELM_SYNDROME_FRAGMENT_5_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_5	R/W	0h	Syndrome bits 160 to 191

14 ELM_SYNDROME_FRAGMENT_6_i Register (Offset = 418h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_6_i (where i = 0 to 7) is shown in Figure 14-7740 and described in Table 14-15678.

Input syndrome polynomial bits 192 to 207.

Offset = 418h + (i * 40h), where: i = 0 to 7

Table 14-23416. ELM_SYNDROME_FRAGMENT_6_i Instances

Instance	Physical Address
ELM0	2501 0418h + formula

Figure 14-7740. ELM_SYNDROME_FRAGMENT_6_i Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SYNDROME_VALID</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SYNDROME_6</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SYNDROME_6</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23418. ELM_SYNDROME_FRAGMENT_6_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	SYNDROME_VALID	R/W	0h	Syndrome valid bit 0h = This syndrome polynomial must not be processed. 1h = This syndrome polynomial must be processed.
15-0	SYNDROME_6	R/W	0h	Syndrome bits 192 to 207

15 ELM_LOCATION_STATUS_i Register (Offset = 800h + formula) [reset = 0h]

ELM_LOCATION_STATUS_i (where i = 0 to 7) is shown in Figure 14-7741 and described in Table 14-15680.

Exit status for the syndrome polynomial processing.

Offset = 800h + (i * 100h), where: i = 0 to 7

Table 14-23419. ELM_LOCATION_STATUS_i Instances

Instance	Physical Address
ELM0	2501 0800h + formula

Figure 14-7741. ELM_LOCATION_STATUS_i Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							ECC_CORRECTABLE
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED			ECC_NB_ERRORS				
R-0h			R-0h				

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23421. ELM_LOCATION_STATUS_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	ECC_CORRECTABLE	R	0h	Error-location process exit status 0h = ECC error-location process failed. Number of errors and error locations are invalid. 1h = All errors were successfully located. Number of errors and error locations are valid.
7-5	RESERVED	R	0h	Reserved
4-0	ECC_NB_ERRORS	R	0h	Number of errors detected and located

16 ELM_ERROR_LOCATION_0_i Register (Offset = 880h + formula) [reset = 0h]

ELM_ERROR_LOCATION_0_i (where i = 0 to 7) is shown in Figure 14-7742 and described in Table 14-15682.

Error-location register 0.

Offset = 880h + (i * 100h), where: i = 0 to 7

Table 14-23422. ELM_ERROR_LOCATION_0_i Instances

Instance	Physical Address
ELM0	2501 0880h + formula

Figure 14-7742. ELM_ERROR_LOCATION_0_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23424. ELM_ERROR_LOCATION_0_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17 ELM_ERROR_LOCATION_1_i Register (Offset = 884h + formula) [reset = 0h]

ELM_ERROR_LOCATION_1_i (where i = 0 to 7) is shown in Figure 14-7743 and described in Table 14-15684.

Error-location register 1.

Offset = 884h + (i * 100h), where: i = 0 to 7

Table 14-23425. ELM_ERROR_LOCATION_1_i Instances

Instance	Physical Address
ELM0	2501 0884h + formula

Figure 14-7743. ELM_ERROR_LOCATION_1_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23427. ELM_ERROR_LOCATION_1_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

18 ELM_ERROR_LOCATION_2_i Register (Offset = 888h + formula) [reset = 0h]

ELM_ERROR_LOCATION_2_i (where i = 0 to 7) is shown in Figure 14-7744 and described in Table 14-15686.

Error-location register 2.

Offset = 888h + (i * 100h), where: i = 0 to 7

Table 14-23428. ELM_ERROR_LOCATION_2_i Instances

Instance	Physical Address
ELM0	2501 0888h + formula

Figure 14-7744. ELM_ERROR_LOCATION_2_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23430. ELM_ERROR_LOCATION_2_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

19 ELM_ERROR_LOCATION_3_i Register (Offset = 88Ch + formula) [reset = 0h]

ELM_ERROR_LOCATION_3_i (where i = 0 to 7) is shown in Figure 14-7745 and described in Table 14-15688.

Error-location register 3.

Offset = 88Ch + (i * 100h), where: i = 0 to 7

Table 14-23431. ELM_ERROR_LOCATION_3_i Instances

Instance	Physical Address
ELM0	2501 088Ch + formula

Figure 14-7745. ELM_ERROR_LOCATION_3_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23433. ELM_ERROR_LOCATION_3_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

20 ELM_ERROR_LOCATION_4_i Register (Offset = 890h + formula) [reset = 0h]

ELM_ERROR_LOCATION_4_i (where i = 0 to 7) is shown in Figure 14-7746 and described in Table 14-15690.

Error-location register 4.

Offset = 890h + (i * 100h), where: i = 0 to 7

Table 14-23434. ELM_ERROR_LOCATION_4_i Instances

Instance	Physical Address
ELM0	2501 0890h + formula

Figure 14-7746. ELM_ERROR_LOCATION_4_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23436. ELM_ERROR_LOCATION_4_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

21 ELM_ERROR_LOCATION_5_i Register (Offset = 894h + formula) [reset = 0h]

ELM_ERROR_LOCATION_5_i (where i = 0 to 7) is shown in Figure 14-7747 and described in Table 14-15692.

Error-location register 5.

Offset = 894h + (i * 100h), where: i = 0 to 7

Table 14-23437. ELM_ERROR_LOCATION_5_i Instances

Instance	Physical Address
ELM0	2501 0894h + formula

Figure 14-7747. ELM_ERROR_LOCATION_5_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23439. ELM_ERROR_LOCATION_5_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

22 ELM_ERROR_LOCATION_6_i Register (Offset = 898h + formula) [reset = 0h]

ELM_ERROR_LOCATION_6_i (where i = 0 to 7) is shown in Figure 14-7748 and described in Table 14-15694.

Error-location register 6.

Offset = 898h + (i * 100h), where: i = 0 to 7

Table 14-23440. ELM_ERROR_LOCATION_6_i Instances

Instance	Physical Address
ELM0	2501 0898h + formula

Figure 14-7748. ELM_ERROR_LOCATION_6_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23442. ELM_ERROR_LOCATION_6_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

23 ELM_ERROR_LOCATION_7_i Register (Offset = 89Ch + formula) [reset = 0h]

ELM_ERROR_LOCATION_7_i (where i = 0 to 7) is shown in Figure 14-7749 and described in Table 14-15696.

Error-location register 7.

Offset = 89Ch + (i * 100h), where: i = 0 to 7

Table 14-23443. ELM_ERROR_LOCATION_7_i Instances

Instance	Physical Address
ELM0	2501 089Ch + formula

Figure 14-7749. ELM_ERROR_LOCATION_7_i Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23445. ELM_ERROR_LOCATION_7_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

24 ELM_ERROR_LOCATION_8_i Register (Offset = 8A0h + formula) [reset = 0h]

ELM_ERROR_LOCATION_8_i (where i = 0 to 7) is shown in Figure 14-7750 and described in Table 14-15698.

Error-location register 8.

Offset = 8A0h + (i * 100h), where: i = 0 to 7

Table 14-23446. ELM_ERROR_LOCATION_8_i Instances

Instance	Physical Address
ELM0	2501 08A0h + formula

Figure 14-7750. ELM_ERROR_LOCATION_8_i Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23448. ELM_ERROR_LOCATION_8_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

25 ELM_ERROR_LOCATION_9_i Register (Offset = 8A4h + formula) [reset = 0h]

ELM_ERROR_LOCATION_9_i (where i = 0 to 7) is shown in Figure 14-7751 and described in Table 14-15700.

Error-location register 9.

Offset = 8A4h + (i * 100h), where: i = 0 to 7

Table 14-23449. ELM_ERROR_LOCATION_9_i Instances

Instance	Physical Address
ELM0	2501 08A4h + formula

Figure 14-7751. ELM_ERROR_LOCATION_9_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23451. ELM_ERROR_LOCATION_9_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

26 ELM_ERROR_LOCATION_10_i Register (Offset = 8A8h + formula) [reset = 0h]

ELM_ERROR_LOCATION_10_i (where i = 0 to 7) is shown in Figure 14-7752 and described in Table 14-15702.

Error-location register 10.

Offset = 8A8h + (i * 100h), where: i = 0 to 7

Table 14-23452. ELM_ERROR_LOCATION_10_i Instances

Instance	Physical Address
ELM0	2501 08A8h + formula

Figure 14-7752. ELM_ERROR_LOCATION_10_i Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23454. ELM_ERROR_LOCATION_10_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

27 ELM_ERROR_LOCATION_11_i Register (Offset = 8ACh + formula) [reset = 0h]

ELM_ERROR_LOCATION_11_i (where i = 0 to 7) is shown in Figure 14-7753 and described in Table 14-15704.

Error-location register 11.

Offset = 8ACh + (i * 100h), where: i = 0 to 7

Table 14-23455. ELM_ERROR_LOCATION_11_i Instances

Instance	Physical Address
ELM0	2501 08ACh + formula

Figure 14-7753. ELM_ERROR_LOCATION_11_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23457. ELM_ERROR_LOCATION_11_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

28 ELM_ERROR_LOCATION_12_i Register (Offset = 8B0h + formula) [reset = 0h]

ELM_ERROR_LOCATION_12_i (where i = 0 to 7) is shown in Figure 14-7754 and described in Table 14-15706.

Error-location register 12.

Offset = 8B0h + (i * 100h), where: i = 0 to 7

Table 14-23458. ELM_ERROR_LOCATION_12_i Instances

Instance	Physical Address
ELM0	2501 08B0h + formula

Figure 14-7754. ELM_ERROR_LOCATION_12_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23460. ELM_ERROR_LOCATION_12_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

29 ELM_ERROR_LOCATION_13_i Register (Offset = 8B4h + formula) [reset = 0h]

ELM_ERROR_LOCATION_13_i (where i = 0 to 7) is shown in Figure 14-7755 and described in Table 14-15708.

Error-location register 13.

Offset = 8B4h + (i * 100h), where: i = 0 to 7

Table 14-23461. ELM_ERROR_LOCATION_13_i Instances

Instance	Physical Address
ELM0	2501 08B4h + formula

Figure 14-7755. ELM_ERROR_LOCATION_13_i Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-23463. ELM_ERROR_LOCATION_13_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

30 ELM_ERROR_LOCATION_14_i Register (Offset = 8B8h + formula) [reset = 0h]

ELM_ERROR_LOCATION_14_i (where i = 0 to 7) is shown in Figure 14-7756 and described in Table 14-15710.

Error-location register 14.

Offset = 8B8h + (i * 100h), where: i = 0 to 7

Table 14-23464. ELM_ERROR_LOCATION_14_i Instances

Instance	Physical Address
ELM0	2501 08B8h + formula

Figure 14-7756. ELM_ERROR_LOCATION_14_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ECC_ERROR_LOCATION												
R-0h			R-0h												

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23466. ELM_ERROR_LOCATION_14_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

31 ELM_ERROR_LOCATION_15_i Register (Offset = 8BCh + formula) [reset = 0h]

ELM_ERROR_LOCATION_15_i (where i = 0 to 7) is shown in Figure 14-7757 and described in Table 14-15712.

Error-location register 15.

Offset = 8BCh + (i * 100h), where: i = 0 to 7

Table 14-23467. ELM_ERROR_LOCATION_15_i Instances

Instance	Physical Address
ELM0	2501 08BCh + formula

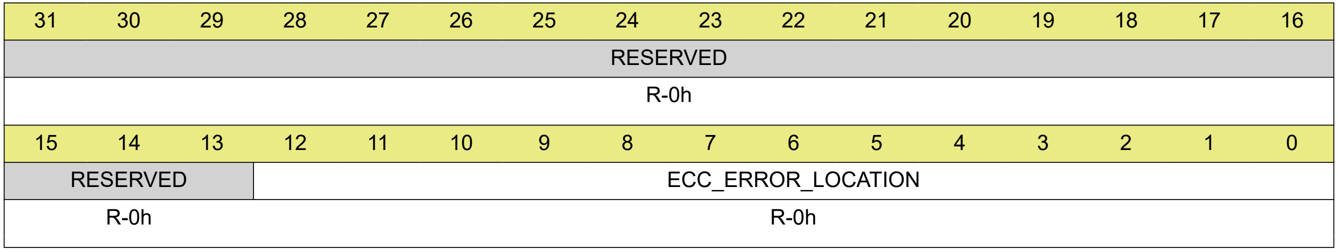

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">ECC_ERROR_LOCATION</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R-0h</td></tr>
</table>

Figure 14-7757. ELM_ERROR_LOCATION_15_i Register

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23469. ELM_ERROR_LOCATION_15_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

14.9.3.6 MMCSD Registers

14.9.3.6.1 MMCSD0 Subsystem Registers

Table 14-15714 lists the memory-mapped registers for the MMCSD0 Subsystem. All register offset addresses not listed in Table 14-15714 should be considered as reserved locations and the register contents should not be modified.

Table 14-23470. MMCSD0 Subsystem Instances

Instance	Base Address
MMCSD0_SS_CFG	0FA1 8000h

Table 14-23471. MMCSD0 Subsystem Registers

Offset	Acronym	Register Name	MMCSD0_SS_CFG Physical Address
0h	MMCSD0_SS_SS_ID_REV_REG	Subsystem ID and Revision Register	0FA1 8000h
10h	MMCSD0_SS_CTL_CFG_1_REG	Controller Config 1 Register	0FA1 8010h
14h	MMCSD0_SS_CTL_CFG_2_REG	Controller Config 2 Register	0FA1 8014h
18h	MMCSD0_SS_CTL_CFG_3_REG	Controller Config 3 Register	0FA1 8018h
1Ch	MMCSD0_SS_CTL_CFG_4_REG	Controller Config 4 Register	0FA1 801Ch
20h	MMCSD0_SS_CTL_CFG_5_REG	Controller Config 5 Register	0FA1 8020h
24h	MMCSD0_SS_CTL_CFG_6_REG	Controller Config 6 Register	0FA1 8024h
28h	MMCSD0_SS_CTL_CFG_7_REG	Controller Config 7 Register	0FA1 8028h
2Ch	MMCSD0_SS_CTL_CFG_8_REG	Controller Config 8 Register	0FA1 802Ch
30h	MMCSD0_SS_CTL_CFG_9_REG	Controller Config 9 Register	0FA1 8030h
34h	MMCSD0_SS_CTL_CFG_10_REG	Controller Config 10 Register	0FA1 8034h
38h	MMCSD0_SS_CTL_CFG_11_REG	Controller Config 11 Register	0FA1 8038h
3Ch	MMCSD0_SS_CTL_CFG_12_REG	Controller Config 12 Register	0FA1 803Ch
40h	MMCSD0_SS_CTL_CFG_13_REG	Controller Config 13 Register	0FA1 8040h
44h	MMCSD0_SS_CTL_CFG_14_REG	Controller Config 14 Register	0FA1 8044h
60h	MMCSD0_SS_CTL_STAT_1_REG	Controller Status 1 Register	0FA1 8060h
64h	MMCSD0_SS_CTL_STAT_2_REG	Controller Status 2 Register	0FA1 8064h
68h	MMCSD0_SS_CTL_STAT_3_REG	Controller Status 3 Register	0FA1 8068h
6Ch	MMCSD0_SS_CTL_STAT_4_REG	Controller Status 4 Register	0FA1 806Ch
70h	MMCSD0_SS_CTL_STAT_5_REG	Controller Status 5 Register	0FA1 8070h
74h	MMCSD0_SS_CTL_STAT_6_REG	Controller Status 6 Register	0FA1 8074h
100h	MMCSD0_SS_PHY_CTRL_1_REG	PHY Control 1 Register	0FA1 8100h
104h	MMCSD0_SS_PHY_CTRL_2_REG	PHY Control 2 Register	0FA1 8104h
108h	MMCSD0_SS_PHY_CTRL_3_REG	PHY Control 3 Register	0FA1 8108h
10Ch	MMCSD0_SS_PHY_CTRL_4_REG	PHY Control 4 Register	0FA1 810Ch
110h	MMCSD0_SS_PHY_CTRL_5_REG	PHY Control 5 Register	0FA1 8110h
114h	MMCSD0_SS_PHY_CTRL_6_REG	PHY Control 6 Register	0FA1 8114h
130h	MMCSD0_SS_PHY_STAT_1_REG	PHY Status 1 Register	0FA1 8130h
134h	MMCSD0_SS_PHY_STAT_2_REG	PHY Status 2 Register	0FA1 8134h

1 MMCSD0_SS_SS_ID_REV_REG Register (Offset = 0h) [reset = 68414A00h]

MMCSD0_SS_SS_ID_REV_REG is shown in Figure 14-7758 and described in Table 14-15716.

Return to Summary Table.

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem.

Table 14-23472. MMCSD0_SS_SS_ID_REV_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8000h

Figure 14-7758. MMCSD0_SS_SS_ID_REV_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_ID															
R-6841h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJ_REV			CUSTOM		MIN_REV					
R-9h					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23474. MMCSD0_SS_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MOD_ID	R	6841h	Module ID
15-11	RTL_VER	R	9h	RTL Version
10-8	MAJ_REV	R	2h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	MIN_REV	R	0h	Minor Revision

2 MMCSD0_SS_CTL_CFG_1_REG Register (Offset = 10h) [reset = 201030C8h]

MMCSD0_SS_CTL_CFG_1_REG is shown in Figure 14-7759 and described in Table 14-15718.

Return to Summary Table.

The Controller Config 1 Register contains various fields to control the configuration ports on the Host Controller.

Table 14-23475. MMCSD0_SS_CTL_CFG_1_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8010h

Figure 14-7759. MMCSD0_SS_CTL_CFG_1_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TUNINGCOUNT</td></tr>
<tr><td colspan="2">R-0h</td><td colspan="6">R/W-20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>ASYNCWKUPENA</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">R-0h</td><td>R/W-1h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">CQFMUL</td><td colspan="2">RESERVED</td><td colspan="2">CQFVAL</td></tr>
<tr><td colspan="4">R/W-3h</td><td colspan="2">R-0h</td><td colspan="2">R/W-C8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CQFVAL</td></tr>
<tr><td colspan="8">R/W-C8h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23477. MMCSD0_SS_CTL_CFG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	TUNINGCOUNT	R/W	20h	Configures the number of Taps (Phases) of the RX clock that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the RX clock during the Tuning Procedure.
23-21	RESERVED	R	0h	Reserved
20	ASYNCWKUPENA	R/W	1h	Determines the Wakeup Signal Generation Mode. 0h: Synchronous Wakeup Mode: The FCLK has to be running for this mode. The Card Insertion/Removal/Interrupt events are detected synchronously on the FCLK and the Wakeup event is generated. The Assertion and Deassertion of the Wakeup event signal synchronous to FCLK. 1h: Asyncrhonous Wakeup Mode: The FCLK and the ICLK can be stopped in this mode and the Wakeup event is asynchronously generated based on the Card Insertion/Removal/Interrupt events. The Assertion and Deassertion of the Wakeup event signal is asynchronous.

Table 14-23477. MMCSD0_SS_CTL_CFG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	RESERVED	R	0h	Reserved
15-12	CQFMUL	R/W	3h	FMUL for the CQ Internal Timer Clock Frequency
11-10	RESERVED	R	0h	Reserved
9-0	CQFVAL	R/W	C8h	FVAL for the CQ Internal Timer Clock Frequency

3 MMCSD0_SS_CTL_CFG_2_REG Register (Offset = 14h) [reset = 24ECC801h]

MMCSD0_SS_CTL_CFG_2_REG is shown in Figure 14-7760 and described in Table 14-15720.

Return to Summary Table.

The Controller Config 2 Register contains various fields to control the configuration ports on the Host Controller. This register sets the LSB fields in the MMCSD0_CAPABILITIES register inside the Host Controller.

Table 14-23478. MMCSD0_SS_CTL_CFG_2_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8014h

Figure 14-7760. MMCSD0_SS_CTL_CFG_2_REG Register

31	30	29	28	27	26	25	24
SLOTTYPE		ASYNCHINTRSUPPORT	RESERVED		SUPPORT1P8VOLT	SUPPORT3P0VOLT	SUPPORT3P3VOLT
R/W-0h		R/W-1h	R-0h		R/W-1h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
SUSPRESSUPPORT	SDMASUPPORT	HIGHSPEEDSUPPORT	RESERVED	ADMA2SUPPORT	SUPPORT8BIT	MAXBLKLENGTH	
R/W-1h	R/W-1h	R/W-1h	R-0h	R/W-1h	R/W-1h	R/W-0h	

15	14	13	12	11	10	9	8
BASECLKFREQ							
R/W-C8h							

7	6	5	4	3	2	1	0
TIMEOUTCLKUNIT	RESERVED	TIMEOUTCLKFREQ					
R/W-0h	R-0h	R/W-1h					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23480. MMCSD0_SS_CTL_CFG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SLOTTYPE	R/W	0h	Slot Type Should be set based on the final product usage. 0h: Removable SCard Slot 1h: Embedded Slot for One Device 2h: Shared Bus Slot 3h: Reserved
29	ASYNCHINTRSUPPORT	R/W	1h	Asynchronous Interrupt Support Suggested Value is 1h (The Core supports monitoring of Asynchronous Interrupt).
28-27	RESERVED	R	0h	Reserved
26	SUPPORT1P8VOLT	R/W	1h	1.8 V Support Suggested Value is 1h (The 1.8 Volt Switching is supported by Core). Optionally can be set to 0h if the application doesn't want 1.8 V switching (SD3.0).

Table 14-23480. MMCSD0_SS_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	SUPPORT3P0VOLT	R/W	0h	3.0 V Support Should be set based on whether 3.0 V is supported on the SD Interface.
24	SUPPORT3P3VOLT	R/W	0h	3.3 V Support Suggested Value is 1h as the 3.3 V is the default voltage on the SD Interface.
23	SUSPRESSUPPORT	R/W	1h	Suspend/Resume Support Suggested Value is 1h (The Suspend/Resume is supported by Core). Optionally can be set to 0h if the application doesn't want to support Suspend/Resume Mode.
22	SDMASUPPORT	R/W	1h	SDMA Support Suggested Value is 1h (The SDMA is supported by Core). Optionally can be set to 0h if the application doesn't want to support SDMA Mode.
21	HIGHSPEEDSUPPORT	R/W	1h	High Speed Support Suggested Value is 1h (The High Speed mode is supported by Core).
20	RESERVED	R	0h	Reserved
19	ADMA2SUPPORT	R/W	1h	ADMA2 Support Suggested Value is 1h (The ADMA2 is supported by Core). Optionally can be set to 0h if the application doesn't want to support ADMA2 Mode.
18	SUPPORT8BIT	R/W	1h	8-bit Support for Embedded Device Suggested Value is 1h (The Core supports 8-bit Interface). Optionally can be set to 0h if the application supports only 4-bit SD Interface.
17-16	MAXBLKLENGTH	R/W	0h	Max Block Length Maximum Block Length supported by the Core/Device. 0h: 512 Bytes 1h: 1024 Bytes 2h: 2048 Bytes 3h: Reserved
15-8	BASECLKFREQ	R/W	C8h	Base Clock Frequency for SD Clock This is the frequency of the FCLK.
7	TIMEOUTCLKUNIT	R/W	0h	Timeout Clock Unit Suggested Value is 0h (KHz).
6	RESERVED	R	0h	Reserved

Table 14-23480. MMCSD0_SS_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	TIMEOUTCLKFREQ	R/W	1h	Timeout Clock Frequency Suggested Value is 1 KHz. Internally the 1 ms Timer is used for Timeout Detection. The 1 ms Timer is generated from the FCLK.

4 MMCSD0_SS_CTL_CFG_3_REG Register (Offset = 18h) [reset = 98000407h]

MMCSD0_SS_CTL_CFG_3_REG is shown in Figure 14-7761 and described in Table 14-15722.

Return to Summary Table.

The Controller Config 3 Register contains various fields to control the configuration ports on the Host Controller. This register sets the MSB fields in the MMCSD0_CAPABILITIES register inside the Host Controller.

Table 14-23481. MMCSD0_SS_CTL_CFG_3_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8018h

Figure 14-7761. MMCSD0_SS_CTL_CFG_3_REG Register

31	30	29	28	27	26	25	24
HS400SUPPORT	RESERVED		SUPPORT1P8VDD2	ADMA3SUPPORT	RESERVED		
R/W-1h	R-0h		R/W-1h	R/W-1h	R-0h		
23	22	21	20	19	18	17	16
CLOCKMULTIPLIER							
R/W-0h							
15	14	13	12	11	10	9	8
RETUNINGMODES		TUNINGFORSDR50	RESERVED	RETUNINGTIMERCNT			
R/W-0h		R/W-0h	R-0h	R/W-4h			
7	6	5	4	3	2	1	0
TYPE4SUPPORT	DDRIVERSUPPORT	CDRIVERSUPPORT	ADRIVERSUPPORT	RESERVED	DDR50SUPPORT	SDR104SUPPORT	SDR50SUPPORT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23483. MMCSD0_SS_CTL_CFG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HS400SUPPORT	R/W	1h	HS400 Support Suggested Value is 1h (The Core supports HS400 Mode). This applies only to eMMC5.0 mode. This should be set to 0h for SD3.0 mode. Optionally can be set to 0h if the application doesn't want to support HS400.
30-29	RESERVED	R	0h	Reserved
28	SUPPORT1P8VDD2	R/W	1h	1.8 V VDD2 Support
27	ADMA3SUPPORT	R/W	1h	ADMA3 Support
26-24	RESERVED	R	0h	Reserved

Table 14-23483. MMCSD0_SS_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	CLOCKMULTIPLIER	R/W	0h	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 0h means that the Host Controller does not support programmable clock generator. 0h: Clock Multiplier is Not Supported 1h: Clock Multiplier M = 2 2h: Clock Multiplier M = 3 ... FFh: Clock Multiplier M = 256
15-14	RETUNINGMODES	R/W	0h	Re-Tuning Modes Should be set to 2h as the Core supports only the Software Timer based Re-Tuning.
13	TUNINGFORSDR50	R/W	0h	Use Tuning for SDR50 This bit should be set if the application wants Tuning be used for SDR50 Modes. The Core operates with or without tuning for SDR50 mode as long as the Clock can be manually tuned using tap delay.
12	RESERVED	R	0h	Reserved
11-8	RETUNINGTIMERCNT	R/W	4h	Timer Count for Re-Tuning This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4h disables Re-Tuning Timer.
7	TYPE4SUPPORT	R/W	0h	Driver Type 4 Support This bit should be set based on whether Driver Type 4 for 1.8 Signalling is supported or not.
6	DDRIVERSUPPORT	R/W	0h	Driver Type D Support This bit should be set based on whether Driver Type D for 1.8 Signalling is supported or not.
5	CDRIVERSUPPORT	R/W	0h	Driver Type C Support This bit should be set based on whether Driver Type C for 1.8 Signalling is supported or not.
4	ADRIVERSUPPORT	R/W	0h	Driver Type A Support This bit should be set based on whether Driver Type A for 1.8 Signalling is supported or not.
3	RESERVED	R	0h	Reserved

Table 14-23483. MMCSD0_SS_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DDR50SUPPORT	R/W	1h	DDR50 Support Suggested Value is 1h (The Core supports DDR50 mode of operation). Optionally can be set to 0h if the application doesn't want to support DDR50.
1	SDR104SUPPORT	R/W	1h	SDR104 Support. Suggested Value is 1h (The Core supports SDR104 mode of operation). Optionally can be set to 0h if the application doesn't want to support SDR104.
0	SDR50SUPPORT	R/W	1h	SDR50 Support. Suggested Value is 1h (The Core supports SDR50 mode of operation). Optionally can be set to 0h if the application doesn't want to support SDR50.

5 MMCSD0_SS_CTL_CFG_4_REG Register (Offset = 1Ch) [reset = 0h]

MMCSD0_SS_CTL_CFG_4_REG is shown in Figure 14-7762 and described in Table 14-15724.

Return to Summary Table.

The Controller Config 4 Register contains various fields to control the configuration ports on the Host Controller. This register sets the LSB fields in the MMCSD0_MAX_CURRENT_CAP register inside the Host Controller.

Table 14-23484. MMCSD0_SS_CTL_CFG_4_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 801Ch

Figure 14-7762. MMCSD0_SS_CTL_CFG_4_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">MAXCURRENT1P8V</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MAXCURRENT3P0V</td><td colspan="8">MAXCURRENT3P3V</td></tr>
<tr><td colspan="8">R/W-0h</td><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23486. MMCSD0_SS_CTL_CFG_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	MAXCURRENT1P8V	R/W	0h	Maximum Current For 1.8 V
15-8	MAXCURRENT3P0V	R/W	0h	Maximum Current For 3.0 V
7-0	MAXCURRENT3P3V	R/W	0h	Maximum Current For 3.3 V

6 MMCSD0_SS_CTL_CFG_5_REG Register (Offset = 20h) [reset = 0h]

MMCSD0_SS_CTL_CFG_5_REG is shown in Figure 14-7763 and described in Table 14-15726.

Return to Summary Table.

The Controller Config 5 Register contains various fields to control the configuration ports on the Host Controller. This register sets the MSB fields in the MMCSD0_MAX_CURRENT_CAP register inside the Host Controller.

Table 14-23487. MMCSD0_SS_CTL_CFG_5_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8020h

Figure 14-7763. MMCSD0_SS_CTL_CFG_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAXCURRENTVDD2							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23489. MMCSD0_SS_CTL_CFG_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MAXCURRENTVDD2	R/W	0h	Maximum Current For 1.8 V (VDD2)

7 MMCSD0_SS_CTL_CFG_6_REG Register (Offset = 24h) [reset = 100h]

MMCSD0_SS_CTL_CFG_6_REG is shown in Figure 14-7764 and described in Table 14-15728.

Return to Summary Table.

The Controller Config 6 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for Initialization inside the Host Controller.

Table 14-23490. MMCSD0_SS_CTL_CFG_6_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8024h

Figure 14-7764. MMCSD0_SS_CTL_CFG_6_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="19">RESERVED</td><td colspan="13">INITPRESETVAL</td></tr>
<tr><td colspan="19">R-0h</td><td colspan="13">R/W-100h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23492. MMCSD0_SS_CTL_CFG_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	INITPRESETVAL	R/W	100h	Preset Value For Initialization

8 MMCSD0_SS_CTL_CFG_7_REG Register (Offset = 28h) [reset = 4h]

MMCSD0_SS_CTL_CFG_7_REG is shown in Figure 14-7765 and described in Table 14-15730.

Return to Summary Table.

The Controller Config 7 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for Default Speed inside the Host Controller.

Table 14-23493. MMCSD0_SS_CTL_CFG_7_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8028h

Figure 14-7765. MMCSD0_SS_CTL_CFG_7_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="19">RESERVED</td><td colspan="13">DSPDPRESETVAL</td></tr>
<tr><td colspan="19">R-0h</td><td colspan="13">R/W-4h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23495. MMCSD0_SS_CTL_CFG_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	DSPDPRESETVAL	R/W	4h	Preset Value For Default Speed

9 MMCSD0_SS_CTL_CFG_8_REG Register (Offset = 2Ch) [reset = 2h]

MMCSD0_SS_CTL_CFG_8_REG is shown in Figure 14-7766 and described in Table 14-15732.

Return to Summary Table.

The Controller Config 8 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for High Speed inside the Host Controller.

Table 14-23496. MMCSD0_SS_CTL_CFG_8_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 802Ch

Figure 14-7766. MMCSD0_SS_CTL_CFG_8_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="19">RESERVED</td><td colspan="13">HSPDPRESETVAL</td></tr>
<tr><td colspan="19">R-0h</td><td colspan="13">R/W-2h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23498. MMCSD0_SS_CTL_CFG_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	HSPDPRESETVAL	R/W	2h	Preset Value For High Speed

10 MMCSD0_SS_CTL_CFG_9_REG Register (Offset = 30h) [reset = 4h]

MMCSD0_SS_CTL_CFG_9_REG is shown in Figure 14-7767 and described in Table 14-15734.

Return to Summary Table.

The Controller Config 9 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for SDR12 inside the Host Controller.

Table 14-23499. MMCSD0_SS_CTL_CFG_9_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8030h

Figure 14-7767. MMCSD0_SS_CTL_CFG_9_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">SDR12PRESETVAL</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R/W-4h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-23501. MMCSD0_SS_CTL_CFG_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR12PRESETVAL	R/W	4h	Preset Value For SDR12

11 MMCSD0_SS_CTL_CFG_10_REG Register (Offset = 34h) [reset = 2h]

MMCSD0_SS_CTL_CFG_10_REG is shown in Figure 14-7768 and described in Table 14-15736.

Return to Summary Table.

The Controller Config 10 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for SDR25 inside the Host Controller.

Table 14-23502. MMCSD0_SS_CTL_CFG_10_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8034h

Figure 14-7768. MMCSD0_SS_CTL_CFG_10_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">SDR25PRESETVAL</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R/W-2h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23504. MMCSD0_SS_CTL_CFG_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR25PRESETVAL	R/W	2h	Preset Value For SDR25

12 MMCSD0_SS_CTL_CFG_11_REG Register (Offset = 38h) [reset = 1h]

MMCSD0_SS_CTL_CFG_11_REG is shown in Figure 14-7769 and described in Table 14-15738.

Return to Summary Table.

The Controller Config 11 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for SDR50 inside the Host Controller.

Table 14-23505. MMCSD0_SS_CTL_CFG_11_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8038h

Figure 14-7769. MMCSD0_SS_CTL_CFG_11_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">SDR50PRESETVAL</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R/W-1h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23507. MMCSD0_SS_CTL_CFG_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR50PRESETVAL	R/W	1h	Preset Value For SDR50

13 MMCSD0_SS_CTL_CFG_12_REG Register (Offset = 3Ch) [reset = 0h]

MMCSD0_SS_CTL_CFG_12_REG is shown in Figure 14-7770 and described in Table 14-15740.

Return to Summary Table.

The Controller Config 12 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for SDR104 inside the Host Controller.

Table 14-23508. MMCSD0_SS_CTL_CFG_12_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 803Ch

Figure 14-7770. MMCSD0_SS_CTL_CFG_12_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SDR104PRESETVAL												
R-0h			R/W-0h												

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23510. MMCSD0_SS_CTL_CFG_12_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR104PRESETVAL	R/W	0h	Preset Value For SDR104

14 MMCSD0_SS_CTL_CFG_13_REG Register (Offset = 40h) [reset = 2h]

MMCSD0_SS_CTL_CFG_13_REG is shown in Figure 14-7771 and described in Table 14-15742.

Return to Summary Table.

The Controller Config 13 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for DDR50 inside the Host Controller.

Table 14-23511. MMCSD0_SS_CTL_CFG_13_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8040h

Figure 14-7771. MMCSD0_SS_CTL_CFG_13_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			DDR50PRESETVAL												
R-0h			R/W-2h												

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23513. MMCSD0_SS_CTL_CFG_13_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	DDR50PRESETVAL	R/W	2h	Preset Value For DDR50

15 MMCSD0_SS_CTL_CFG_14_REG Register (Offset = 44h) [reset = 1h]

MMCSD0_SS_CTL_CFG_14_REG is shown in Figure 14-7772 and described in Table 14-15744.

Return to Summary Table.

The Controller Config 14 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE0 to MMCSD0_PRESET_VALUE10) for HS400 inside the Host Controller.

Table 14-23514. MMCSD0_SS_CTL_CFG_14_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8044h

Figure 14-7772. MMCSD0_SS_CTL_CFG_14_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">HS400PRESETVAL</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R/W-1h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23516. MMCSD0_SS_CTL_CFG_14_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	HS400PRESETVAL	R/W	1h	Preset Value For HS400

16 MMCSD0_SS_CTL_STAT_1_REG Register (Offset = 60h) [reset = 80000000h]

MMCSD0_SS_CTL_STAT_1_REG is shown in Figure 14-7773 and described in Table 14-15746.

Return to Summary Table.

The Controller Status 1 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-23517. MMCSD0_SS_CTL_STAT_1_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8060h

Figure 14-7773. MMCSD0_SS_CTL_STAT_1_REG Register

31	30	29	28	27	26	25	24
SDHC_CMDIDLE	RESERVED						
R-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMADEBUGBUS							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DMADEBUGBUS							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23519. MMCSD0_SS_CTL_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDHC_CMDIDLE	R	1h	Idle signal to enable software to gate off the clocks
30-16	RESERVED	R	0h	Reserved
15-0	DMADEBUGBUS	R	0h	DMA_CTRL Debug Bus

17 MMCSD0_SS_CTL_STAT_2_REG Register (Offset = 64h) [reset = 10h]

MMCSD0_SS_CTL_STAT_2_REG is shown in Figure 14-7774 and described in Table 14-15748.

Return to Summary Table.

The Controller Status 2 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-23520. MMCSD0_SS_CTL_STAT_2_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8064h

Figure 14-7774. MMCSD0_SS_CTL_STAT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMDDEBUGBUS															
R-0h																R-10h															

LEGEND: R = Read Only; *-n* = value after reset

Table 14-23522. MMCSD0_SS_CTL_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CMDDEBUGBUS	R	10h	CMD_CTRL Debug Bus

18 MMCSD0_SS_CTL_STAT_3_REG Register (Offset = 68h) [reset = 0h]

MMCSD0_SS_CTL_STAT_3_REG is shown in Figure 14-7775 and described in Table 14-15750.

Return to Summary Table.

The Controller Status 3 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-23523. MMCSD0_SS_CTL_STAT_3_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8068h

Figure 14-7775. MMCSD0_SS_CTL_STAT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TXDDEBUGBUS															
R-0h																R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23525. MMCSD0_SS_CTL_STAT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TXDDEBUGBUS	R	0h	TXD_CTRL Debug Bus

19 MMCSD0_SS_CTL_STAT_4_REG Register (Offset = 6Ch) [reset = 0h]

MMCSD0_SS_CTL_STAT_4_REG is shown in Figure 14-7776 and described in Table 14-15752.

Return to Summary Table.

The Controller Status 4 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-23526. MMCSD0_SS_CTL_STAT_4_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 806Ch

Figure 14-7776. MMCSD0_SS_CTL_STAT_4_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RXDDEBUGBUS0</td></tr>
<tr><td colspan="16">R-0h</td><td colspan="16">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23528. MMCSD0_SS_CTL_STAT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RXDDEBUGBUS0	R	0h	RXD_CTRL Debug Bus (SD CLK)

20 MMCSD0_SS_CTL_STAT_5_REG Register (Offset = 70h) [reset = 8h]

MMCSD0_SS_CTL_STAT_5_REG is shown in Figure 14-7777 and described in Table 14-15754.

Return to Summary Table.

The Controller Status 5 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-23529. MMCSD0_SS_CTL_STAT_5_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8070h

Figure 14-7777. MMCSD0_SS_CTL_STAT_5_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RXDDEBUGBUS1</td></tr>
<tr><td colspan="16">R-0h</td><td colspan="16">R-8h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23531. MMCSD0_SS_CTL_STAT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RXDDEBUGBUS1	R	8h	RXD_CTRL Debug Bus (RX CLK)

21 MMCSD0_SS_CTL_STAT_6_REG Register (Offset = 74h) [reset = 0h]

MMCSD0_SS_CTL_STAT_6_REG is shown in Figure 14-7778 and described in Table 14-15756.

Return to Summary Table.

The Controller Status 6 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-23532. MMCSD0_SS_CTL_STAT_6_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8074h

Figure 14-7778. MMCSD0_SS_CTL_STAT_6_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TUNDEBUGBUS															
R-0h																R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23534. MMCSD0_SS_CTL_STAT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TUNDEBUGBUS	R	0h	TUN_CTRL Debug Bus

22 MMCSD0_SS_PHY_CTRL_1_REG Register (Offset = 100h) [reset = 80010000h]

MMCSD0_SS_PHY_CTRL_1_REG is shown in Figure 14-7779 and described in Table 14-15758.

Return to Summary Table.

The PHY Control 1 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-23535. MMCSD0_SS_PHY_CTRL_1_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8100h

Figure 14-7779. MMCSD0_SS_PHY_CTRL_1_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td colspan="3">DR_TY</td><td colspan="2">RESERVED</td><td>RETRIM</td><td>EN_RTRIM</td></tr>
<tr><td>R-0h</td><td colspan="3">R/W-0h</td><td colspan="2">R-0h</td><td>R/W-0h</td><td>R/W-1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">DLL_TRM_ICP</td><td colspan="2">RESERVED</td><td>ENDLL</td><td>PDB</td></tr>
<tr><td colspan="4">R/W-0h</td><td colspan="2">R-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23537. MMCSD0_SS_PHY_CTRL_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-20	DR_TY	R/W	0h	Drive Source/Sink Impedance Programming 0h: 50 Ohms 1h: 33 Ohms 2h: 66 Ohms 3h: 100 Ohms 4h: 40 Ohms
19-18	RESERVED	R	0h	Reserved
17	RETRIM	R/W	0h	Start CALIO Calibration Cycle At positive edge initiates CALIO calibration cycle.
16	EN_RTRIM	R/W	1h	CALIO Enable Enables CALIO, If enabled CALIO will start calibration cycle at phyctrl_pdb positive edge.
15-8	RESERVED	R	0h	Reserved

Table 14-23537. MMCSD0_SS_PHY_CTRL_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	DLL_TRM_ICP	R/W	0h	Analog DLL's Charge Pump Current Trim Programs the analog DLL loop gain.
3-2	RESERVED	R	0h	Reserved
1	ENDLL	R/W	0h	Enable DLL Enables the analog DLL circuits.
0	PDB	R/W	0h	CALIO S/M Power Down Bar SoC asserts after power up sequence is completed.

23 MMCSD0_SS_PHY_CTRL_2_REG Register (Offset = 104h) [reset = 0h]

MMCSD0_SS_PHY_CTRL_2_REG is shown in Figure 14-7780 and described in Table 14-15760.

Return to Summary Table.

The PHY Control 2 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-23538. MMCSD0_SS_PHY_CTRL_2_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8104h

Figure 14-7780. MMCSD0_SS_PHY_CTRL_2_REG Register

31	30	29	28	27	26	25	24
RESERVED		OD_RELEASE_STRB	OD_RELEASE_CMD	RESERVED			
R-0h		R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
OD_RELEASE_DAT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		ODEN_STRB	ODEN_CMD	RESERVED			
R-0h		R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
ODEN_DAT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23540. MMCSD0_SS_PHY_CTRL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	OD_RELEASE_STRB	R/W	0h	Disable an internal 4.7 K pull up resistor on STRB line in open drain mode
28	OD_RELEASE_CMD	R/W	0h	Disable an internal 4.7 K pull up resistor on CMD line in open drain mode
27-24	RESERVED	R	0h	Reserved
23-16	OD_RELEASE_DAT	R/W	0h	Disable an internal 4.7 K pull up resistor on data lines in open drain mode
15-14	RESERVED	R	0h	Reserved
13	ODEN_STRB	R/W	0h	Open Drain Enable On STRB Lline
12	ODEN_CMD	R/W	0h	Open Drain Enable On CMD Line
11-8	RESERVED	R	0h	Reserved
7-0	ODEN_DAT	R/W	0h	Open Drain Enable On DAT Lines

24 MMCSD0_SS_PHY_CTRL_3_REG Register (Offset = 108h) [reset = 10FF10FFh]

MMCSD0_SS_PHY_CTRL_3_REG is shown in Figure 14-7781 and described in Table 14-15762.

Return to Summary Table.

The PHY Control 3 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-23541. MMCSD0_SS_PHY_CTRL_3_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8108h

Figure 14-7781. MMCSD0_SS_PHY_CTRL_3_REG Register

31	30	29	28	27	26	25	24
RESERVED		PU_STRB	PU_CMD	RESERVED			
R-0h		R/W-0h	R/W-1h	R-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PU_DAT							
R/W-FFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		REN_STRB	REN_CMD	RESERVED			
R-0h		R/W-0h	R/W-1h	R-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REN_DAT							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23543. MMCSD0_SS_PHY_CTRL_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	PU_STRB	R/W	0h	Enable Pull Up On STRB Line If ren_strb is high week pull up is enabled on STRB line.
28	PU_CMD	R/W	1h	Enable Pull Up On CMD Line If ren_cmd is high week pull up is enabled on CMD line.
27-24	RESERVED	R	0h	Reserved
23-16	PU_DAT	R/W	FFh	Enable Pull Up On DAT Lines If ren_dat is high week pull up is enabled on DATA lines.
15-14	RESERVED	R	0h	Reserved
13	REN_STRB	R/W	1h	Enable Pull Up/Down On The STRB Line If pu_strb is high a week pull up is enabled on STRB line, if low week pull down is enabled on STRB line.

Table 14-23543. MMCSD0_SS_PHY_CTRL_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	REN_CMD	R/W	1h	Enable Pull Up/Down On The CMD Line If pu_cmd is high a week pull up is enabled on CMD line, if low week pull down is enabled on CMD line.
11-8	RESERVED	R	0h	Reserved
7-0	REN_DAT	R/W	FFh	Enable Pull Up/Down On The DAT Lines If pu_dat is high a week pull up is enabled on DATA lines, if low week pull down is enabled on DATA lines.

25 MMCSD0_SS_PHY_CTRL_4_REG Register (Offset = 10Ch) [reset = 0h]

MMCSD0_SS_PHY_CTRL_4_REG is shown in Figure 14-7782 and described in Table 14-15764.

Return to Summary Table.

The PHY Control 4 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-23544. MMCSD0_SS_PHY_CTRL_4_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 810Ch

Figure 14-7782. MMCSD0_SS_PHY_CTRL_4_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">STRBSEL</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>OTAPDLYENA</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">R-0h</td><td>R/W-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">OTAPDLYSEL</td><td colspan="2">RESERVED</td><td>ITAPCHGWIN</td><td>ITAPDLYENA</td></tr>
<tr><td colspan="4">R/W-0h</td><td colspan="2">R-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ITAPDLYSEL</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="5">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23546. MMCSD0_SS_PHY_CTRL_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	STRBSEL	R/W	0h	Select the Four Taps for each of STRB_90 and STRB_180 Outputs. strbsel[3:2] selects one of the four for STRB_180 and strbsel[1:0] selects the four taps for STRB_90.
23-21	RESERVED	R	0h	Reserved
20	OTAPDLYENA	R/W	0h	Output Tap Delay Enable Enables manual control of the TX clock tap delay, for clocking the final stage flops for maintaining Hold requirements on EMMC Interface.
19-16	RESERVED	R	0h	Reserved
15-12	OTAPDLYSEL	R/W	0h	Output Tap Delay Select Manual control of the TX clock tap delay for clocking the final stage flops for maintaining Hold requirements on EMMC Interface.
11-10	RESERVED	R	0h	Reserved

Table 14-23546. MMCSD0_SS_PHY_CTRL_4_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ITAPCHGWIN	R/W	0h	Input Tap Change Window It gets asserted by the controller while changing the itapdlysel. Used to gate of the RX clock during switching the clock source while tap is changing to avoid clock glitches.
8	ITAPDLYENA	R/W	0h	Input Tap Delay Enable This is used for the manual control of the RX clock Tap Delay in non HS200/HS400 modes.
7-5	RESERVED	R	0h	Reserved
4-0	ITAPDLYSEL	R/W	0h	Input Tap Delay Select Manual control of the RX clock Tap Delay in the non HS200/HS400 modes.

26 MMCSD0_SS_PHY_CTRL_5_REG Register (Offset = 110h) [reset = 0h]

MMCSD0_SS_PHY_CTRL_5_REG is shown in Figure 14-7783 and described in Table 14-15766.

Return to Summary Table.

The PHY Control 5 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-23547. MMCSD0_SS_PHY_CTRL_5_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8110h

Figure 14-7783. MMCSD0_SS_PHY_CTRL_5_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						SELDLYTXCLK	SELDLYRXCLK
R-0h						R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					FRQSEL		
R-0h					R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLKBUFSEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23549. MMCSD0_SS_PHY_CTRL_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	SELDLYTXCLK	R/W	0h	Select the Delay chain based txclk. Enables the TX clock based delay chain rather than analog DLL based delay chain.
16	SELDLYRXCLK	R/W	0h	Select the Delay chain based rxclk. Enables the RX clock based delay chain rather than analog DLL based delay chain.
15-11	RESERVED	R	0h	Reserved
10-8	FRQSEL	R/W	0h	Select the frequency range of DLL operation: 0h: 200 MHz to 170 MHz, 1h: 170 MHz to 140 MHz, 2h: 140 MHz to 110 MHz, 3h: 110 MHz to 80MHz, 4h: 80 MHz to 50 MHz, 5h: 275 Mhz to 250 MHz, 6h: 250 MHz to 225 MHz, 7h: 225 MHz to 200 MHz.

Table 14-23549. MMCSD0_SS_PHY_CTRL_5_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2-0	CLKBUFSEL	R/W	0h	Clock Delay Buffer Select. Selects one of the eight taps in the CLK Delay Buffer based on PVT variation.

27 MMCSD0_SS_PHY_CTRL_6_REG Register (Offset = 114h) [reset = 0h]

MMCSD0_SS_PHY_CTRL_6_REG is shown in Figure 14-7784 and described in Table 14-15768.

Return to Summary Table.

The PHY Control 6 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-23550. MMCSD0_SS_PHY_CTRL_6_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8114h

Figure 14-7784. MMCSD0_SS_PHY_CTRL_6_REG Register

31	30	29	28	27	26	25	24
BISTENABLE	BISTSTART	RESERVED		BISTMODE			
R/W-0h	R/W-0h	R-0h		R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TESTCTRL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23552. MMCSD0_SS_PHY_CTRL_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BISTENABLE	R/W	0h	Internal BIST Operation Enable Enables the embedded BIST.
30	BISTSTART	R/W	0h	Internal BIST Start Starts the embedded BIST operation.
29-28	RESERVED	R	0h	Reserved
27-24	BISTMODE	R/W	0h	Internal BIST Mode Select Select the embedded BIST mode of operation.
23-8	RESERVED	R	0h	Reserved
7-0	TESTCTRL	R/W	0h	PHY Test Control: 10h: Test EMMC IOs sink impedance 11h: Test EMMC IOs source impedance 20h: Test RX clock phases on data lines 30h: Test TX clock phases on data lines 40h: Test STRB clock phases on data lines

28 MMCSD0_SS_PHY_STAT_1_REG Register (Offset = 130h) [reset = E0h]

MMCSD0_SS_PHY_STAT_1_REG is shown in Figure 14-7785 and described in Table 14-15770.

Return to Summary Table.

The PHY Status 1 Register contains various fields to reflect the status of the Host Controller PHY ports.

Table 14-23553. MMCSD0_SS_PHY_STAT_1_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8130h

Figure 14-7785. MMCSD0_SS_PHY_STAT_1_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RTRIM				BISTDONE	EXR_NINST	CALDONE	DLLRDY
R-Eh				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23555. MMCSD0_SS_PHY_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	RTRIM	R	Eh	CALIO Calibration Result Holds the content of CALIO Impedance Calibration Result.
3	BISTDONE	R	0h	Internal BIST Completed Test Cycle Indicates that the embedded BIST has completed the test cycle.
2	EXR_NINST	R	0h	External Resistor On CALIO Absent Indicates trim cycle started and external resistor is absent.
1	CALDONE	R	0h	STATUS, indicate that CALIO Calibration is completed successfully.
0	DLLRDY	R	0h	DLL Ready Indicates that DLL loop is locked.

29 MMCSD0_SS_PHY_STAT_2_REG Register (Offset = 134h) [reset = 0h]

MMCSD0_SS_PHY_STAT_2_REG is shown in Figure 14-7786 and described in Table 14-15772.

Return to Summary Table.

The PHY Status 2 Register contains various fields to reflect the status of the Host Controller PHY ports.

Table 14-23556. MMCSD0_SS_PHY_STAT_2_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	0FA1 8134h

Figure 14-7786. MMCSD0_SS_PHY_STAT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BISTSTATUS																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23558. MMCSD0_SS_PHY_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BISTSTATUS	R	0h	Internal BIST Data Compare Results BIST cycle data comparison results.

14.9.3.6.2 MMCSD0 RX RAM ECC Aggregator Registers

Table 14-15774 lists the memory-mapped registers for the MMCSD0 RX RAM ECC Aggregator. All register offset addresses not listed in Table 14-15774 should be considered as reserved locations and the register contents should not be modified.

Table 14-23559. MMCSD0 RX RAM ECC Aggregator Instances

Instance	Base Address
MMCSD0_ECC_AGGR_RXMEM	0070 6000h

Table 14-23560. MMCSD0 RX RAM ECC Aggregator Registers

Offset	Acronym	Register Name	MMCSD0_ECC_AGGR_RXMEM Physical Address
0h	MMCSD0_RXECC_REV	Aggregator Revision Register	0070 6000h
8h	MMCSD0_RXECC_VECTOR	ECC Vector Register	0070 6008h
Ch	MMCSD0_RXECC_STAT	Misc Status Register	0070 600Ch
3Ch	MMCSD0_RXECC_SEC_EOI_REG	SEC EOI Register	0070 603Ch
40h	MMCSD0_RXECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	0070 6040h
80h	MMCSD0_RXECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	0070 6080h
C0h	MMCSD0_RXECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	0070 60C0h
13Ch	MMCSD0_RXECC_DED_EOI_REG	DED EOI Register	0070 613Ch
140h	MMCSD0_RXECC_DED_STATUS_REG0	DED Interrupt Status Register 0	0070 6140h
180h	MMCSD0_RXECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	0070 6180h
1C0h	MMCSD0_RXECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	0070 61C0h
200h	MMCSD0_RXECC_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	0070 6200h
204h	MMCSD0_RXECC_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	0070 6204h
208h	MMCSD0_RXECC_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	0070 6208h
20Ch	MMCSD0_RXECC_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	0070 620Ch

1 MMCSD0_RXECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MMCSD0_RXECC_REV is shown in Figure 14-7787 and described in Table 14-15776.

Return to Summary Table.

Aggregator Revision Register

Revision parameters.

Table 14-23561. MMCSD0_RXECC_REV Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6000h

Figure 14-7787. MMCSD0_RXECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23563. MMCSD0_RXECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

2 MMCSD0_RXECC_VECTOR Register (Offset = 8h) [reset = 0h]

MMCSD0_RXECC_VECTOR is shown in Figure 14-7788 and described in Table 14-15778.

Return to Summary Table.

ECC Vector Register

Table 14-23564. MMCSD0_RXECC_VECTOR Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6008h

Figure 14-7788. MMCSD0_RXECC_VECTOR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W1C-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1S-0h</td><td colspan="4">R-0h</td><td colspan="3">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23566. MMCSD0_RXECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

3 MMCSD0_RXECC_STAT Register (Offset = Ch) [reset = 1h]

MMCSD0_RXECC_STAT is shown in Figure 14-7789 and described in Table 14-15780.

Return to Summary Table.

Misc Status Register

Table 14-23567. MMCSD0_RXECC_STAT Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 600Ch

Figure 14-7789. MMCSD0_RXECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-0h																					R-1h										

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23569. MMCSD0_RXECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

4 MMCSD0_RXECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MMCSD0_RXECC_SEC_EOI_REG is shown in Figure 14-7790 and described in Table 14-15782.

Return to Summary Table.

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-23570. MMCSD0_RXECC_SEC_EOI_REG Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 603Ch

Figure 14-7790. MMCSD0_RXECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-23572. MMCSD0_RXECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	SEC EOI

5 MMCSD0_RXECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MMCSD0_RXECC_SEC_STATUS_REG0 is shown in Figure 14-7791 and described in Table 14-15784.

Return to Summary Table.

SEC Interrupt Status Register 0

Table 14-23573. MMCSD0_RXECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6040h

Figure 14-7791. MMCSD0_RXECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23575. MMCSD0_RXECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_PEND	R/W1S	0h	Interrupt Pending Status for rxmem_pend

6 MMCSD0_RXECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MMCSD0_RXECC_SEC_ENABLE_SET_REG0 is shown in Figure 14-7792 and described in Table 14-15786.

Return to Summary Table.

SEC Interrupt Enable Set Register 0

Table 14-23576. MMCSD0_RXECC_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6080h

Figure 14-7792. MMCSD0_RXECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23578. MMCSD0_RXECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for rxmem_pend

7 MMCSD0_RXECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MMCSD0_RXECC_SEC_ENABLE_CLR_REG0 is shown in Figure 14-7793 and described in Table 14-15788.

Return to Summary Table.

SEC Interrupt Enable Clear Register 0

Table 14-23579. MMCSD0_RXECC_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 60C0h

Figure 14-7793. MMCSD0_RXECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-23581. MMCSD0_RXECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for rxmem_pend

8 MMCSD0_RXECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MMCSD0_RXECC_DED_EOI_REG is shown in Figure 14-7794 and described in Table 14-15790.

Return to Summary Table.

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-23582. MMCSD0_RXECC_DED_EOI_REG Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 613Ch

Figure 14-7794. MMCSD0_RXECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23584. MMCSD0_RXECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	DED EOI

9 MMCSD0_RXECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MMCSD0_RXECC_DED_STATUS_REG0 is shown in Figure 14-7795 and described in Table 14-15792.

Return to Summary Table.

DED Interrupt Status Register 0

Table 14-23585. MMCSD0_RXECC_DED_STATUS_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6140h

Figure 14-7795. MMCSD0_RXECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23587. MMCSD0_RXECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_PEND	R/W1S	0h	Interrupt Pending Status for rxmem_pend

10 MMCSD0_RXECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MMCSD0_RXECC_DED_ENABLE_SET_REG0 is shown in Figure 14-7796 and described in Table 14-15794.

Return to Summary Table.

DED Interrupt Enable Set Register 0

Table 14-23588. MMCSD0_RXECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6180h

Figure 14-7796. MMCSD0_RXECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-23590. MMCSD0_RXECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for rxmem_pend

11 MMCSD0_RXECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MMCSD0_RXECC_DED_ENABLE_CLR_REG0 is shown in Figure 14-7797 and described in Table 14-15796.

Return to Summary Table.

DED Interrupt Enable Clear Register 0

Table 14-23591. MMCSD0_RXECC_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 61C0h

Figure 14-7797. MMCSD0_RXECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-23593. MMCSD0_RXECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for rxmem_pend

12 MMCSD0_RXECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MMCSD0_RXECC_AGGR_ENABLE_SET is shown in Figure 14-7798 and described in Table 14-15798.

Return to Summary Table.

Aggregator Interrupt Enable Set Register

Table 14-23594. MMCSD0_RXECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6200h

Figure 14-7798. MMCSD0_RXECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23596. MMCSD0_RXECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

13 MMCSD0_RXECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MMCSD0_RXECC_AGGR_ENABLE_CLR is shown in Figure 14-7799 and described in Table 14-15800.

Return to Summary Table.

Aggregator Interrupt Enable Clear Register

Table 14-23597. MMCSD0_RXECC_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6204h

Figure 14-7799. MMCSD0_RXECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-23599. MMCSD0_RXECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

14 MMCSD0_RXECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MMCSD0_RXECC_AGGR_STATUS_SET is shown in Figure 14-7800 and described in Table 14-15802.

Return to Summary Table.

Aggregator Interrupt Status Set Register

Table 14-23600. MMCSD0_RXECC_AGGR_STATUS_SET Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 6208h

Figure 14-7800. MMCSD0_RXECC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; *-n* = value after reset

Table 14-23602. MMCSD0_RXECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

15 MMCSD0_RXECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MMCSD0_RXECC_AGGR_STATUS_CLR is shown in Figure 14-7801 and described in Table 14-15804.

Return to Summary Table.

Aggregator Interrupt Status Clear Register

Table 14-23603. MMCSD0_RXECC_AGGR_STATUS_CLR Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	0070 620Ch

Figure 14-7801. MMCSD0_RXECC_AGGR_STATUS_CLR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -*n* = value after reset

Table 14-23605. MMCSD0_RXECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

14.9.3.6.3 MMCSD0 TX RAM ECC Aggregator Registers

Table 14-15806 lists the memory-mapped registers for the MMCSD0 TX RAM ECC Aggregator. All register offset addresses not listed in Table 14-15806 should be considered as reserved locations and the register contents should not be modified.

Table 14-23606. MMCSD0 TX RAM ECC Aggregator Instances

Instance	Base Address
MMCSD0_ECC_AGGR_TXMEM	0070 7000h

Table 14-23607. MMCSD0 TX RAM ECC Aggregator Registers

Offset	Acronym	Register Name	MMCSD0_ECC_AGGR_TXMEM Physical Address
0h	MMCSD0_TXECC_REV	Aggregator Revision Register	0070 7000h
8h	MMCSD0_TXECC_VECTOR	ECC Vector Register	0070 7008h
Ch	MMCSD0_TXECC_STAT	Misc Status Register	0070 700Ch
3Ch	MMCSD0_TXECC_SEC_EOI_REG	SEC EOI Register	0070 703Ch
40h	MMCSD0_TXECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	0070 7040h
80h	MMCSD0_TXECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	0070 7080h
C0h	MMCSD0_TXECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	0070 70C0h
13Ch	MMCSD0_TXECC_DED_EOI_REG	DED EOI Register	0070 713Ch
140h	MMCSD0_TXECC_DED_STATUS_REG0	DED Interrupt Status Register 0	0070 7140h
180h	MMCSD0_TXECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	0070 7180h
1C0h	MMCSD0_TXECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	0070 71C0h
200h	MMCSD0_TXECC_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	0070 7200h
204h	MMCSD0_TXECC_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	0070 7204h
208h	MMCSD0_TXECC_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	0070 7208h
20Ch	MMCSD0_TXECC_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	0070 720Ch

1 MMCSD0_TXECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MMCSD0_TXECC_REV is shown in Figure 14-7802 and described in Table 14-15808.

Return to Summary Table.

Aggregator Revision Register

Revision parameters.

Table 14-23608. MMCSD0_TXECC_REV Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7000h

Figure 14-7802. MMCSD0_TXECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23610. MMCSD0_TXECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

2 MMCSD0_TXECC_VECTOR Register (Offset = 8h) [reset = 0h]

MMCSD0_TXECC_VECTOR is shown in Figure 14-7803 and described in Table 14-15810.

Return to Summary Table.

ECC Vector Register

Table 14-23611. MMCSD0_TXECC_VECTOR Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7008h

Figure 14-7803. MMCSD0_TXECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R-0h							R/W1C-0h

23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							

15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		

7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23613. MMCSD0_TXECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

3 MMCSD0_TXECC_STAT Register (Offset = Ch) [reset = 1h]

MMCSD0_TXECC_STAT is shown in Figure 14-7804 and described in Table 14-15812.

Return to Summary Table.

Misc Status Register

Table 14-23614. MMCSD0_TXECC_STAT Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 700Ch

Figure 14-7804. MMCSD0_TXECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-0h																					R-1h										

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23616. MMCSD0_TXECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

4 MMCSD0_TXECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MMCSD0_TXECC_SEC_EOI_REG is shown in Figure 14-7805 and described in Table 14-15814.

Return to Summary Table.

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-23617. MMCSD0_TXECC_SEC_EOI_REG Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 703Ch

Figure 14-7805. MMCSD0_TXECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23619. MMCSD0_TXECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	SEC EOI

5 MMCSD0_TXECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MMCSD0_TXECC_SEC_STATUS_REG0 is shown in Figure 14-7806 and described in Table 14-15816.

Return to Summary Table.

SEC Interrupt Status Register 0

Table 14-23620. MMCSD0_TXECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7040h

Figure 14-7806. MMCSD0_TXECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23622. MMCSD0_TXECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_PEND	R/W1S	0h	Interrupt Pending Status for txmem_pend

6 MMCSD0_TXECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MMCSD0_TXECC_SEC_ENABLE_SET_REG0 is shown in Figure 14-7807 and described in Table 14-15818.

Return to Summary Table.

SEC Interrupt Enable Set Register 0

Table 14-23623. MMCSD0_TXECC_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7080h

Figure 14-7807. MMCSD0_TXECC_SEC_ENABLE_SET_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TXMEM_ENABLE_SET</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-23625. MMCSD0_TXECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for txmem_pend

7 MMCSD0_TXECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MMCSD0_TXECC_SEC_ENABLE_CLR_REG0 is shown in Figure 14-7808 and described in Table 14-15820.

Return to Summary Table.

SEC Interrupt Enable Clear Register 0

Table 14-23626. MMCSD0_TXECC_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 70C0h

Figure 14-7808. MMCSD0_TXECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-23628. MMCSD0_TXECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for txmem_pend

8 MMCSD0_TXECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MMCSD0_TXECC_DED_EOI_REG is shown in Figure 14-7809 and described in Table 14-15822.

Return to Summary Table.

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-23629. MMCSD0_TXECC_DED_EOI_REG Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 713Ch

Figure 14-7809. MMCSD0_TXECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-23631. MMCSD0_TXECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	DED EOI

9 MMCSD0_TXECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MMCSD0_TXECC_DED_STATUS_REG0 is shown in Figure 14-7810 and described in Table 14-15824.

Return to Summary Table.

DED Interrupt Status Register 0

Table 14-23632. MMCSD0_TXECC_DED_STATUS_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7140h

Figure 14-7810. MMCSD0_TXECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23634. MMCSD0_TXECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_PEND	R/W1S	0h	Interrupt Pending Status for txmem_pend

10 MMCSD0_TXECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MMCSD0_TXECC_DED_ENABLE_SET_REG0 is shown in Figure 14-7811 and described in Table 14-15826.

Return to Summary Table.

DED Interrupt Enable Set Register 0

Table 14-23635. MMCSD0_TXECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7180h

Figure 14-7811. MMCSD0_TXECC_DED_ENABLE_SET_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TXMEM_ENABLE_SET</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23637. MMCSD0_TXECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for txmem_pend

11 MMCSD0_TXECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MMCSD0_TXECC_DED_ENABLE_CLR_REG0 is shown in Figure 14-7812 and described in Table 14-15828.

Return to Summary Table.

DED Interrupt Enable Clear Register 0

Table 14-23638. MMCSD0_TXECC_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 71C0h

Figure 14-7812. MMCSD0_TXECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-23640. MMCSD0_TXECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for txmem_pend

12 MMCSD0_TXECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MMCSD0_TXECC_AGGR_ENABLE_SET is shown in Figure 14-7813 and described in Table 14-15830.

Return to Summary Table.

Aggregator Interrupt Enable Set Register

Table 14-23641. MMCSD0_TXECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7200h

Figure 14-7813. MMCSD0_TXECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-23643. MMCSD0_TXECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

13 MMCSD0_TXECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MMCSD0_TXECC_AGGR_ENABLE_CLR is shown in Figure 14-7814 and described in Table 14-15832.

Return to Summary Table.

Aggregator Interrupt Enable Clear Register

Table 14-23644. MMCSD0_TXECC_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7204h

Figure 14-7814. MMCSD0_TXECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-23646. MMCSD0_TXECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

14 MMCSD0_TXECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MMCSD0_TXECC_AGGR_STATUS_SET is shown in Figure 14-7815 and described in Table 14-15834.

Return to Summary Table.

Aggregator Interrupt Status Set Register

Table 14-23647. MMCSD0_TXECC_AGGR_STATUS_SET Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 7208h

Figure 14-7815. MMCSD0_TXECC_AGGR_STATUS_SET Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -*n* = value after reset

Table 14-23649. MMCSD0_TXECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

15 MMCSD0_TXECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MMCSD0_TXECC_AGGR_STATUS_CLR is shown in Figure 14-7816 and described in Table 14-15836.

Return to Summary Table.

Aggregator Interrupt Status Clear Register

Table 14-23650. MMCSD0_TXECC_AGGR_STATUS_CLR Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	0070 720Ch

Figure 14-7816. MMCSD0_TXECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; *-n* = value after reset

Table 14-23652. MMCSD0_TXECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

14.9.3.6.4 MMCSD0 Host Controller Registers

Table 14-15838 lists the memory-mapped registers for the MMCSD0 Host Controller. All register offset addresses not listed in Table 14-15838 should be considered as reserved locations and the register contents should not be modified.

Note

UHSII is not supported. For more information, see *Not Supported Features*.

Table 14-23653. MMCSD0 HOST CONTROLLER Instances

Instance	Base Address
MMCSD0_CTL_CFG	0FA1 0000h

Table 14-23654. MMCSD0 Host Controller Registers

Offset	Acronym	Register Name	MMCSD0_CTL_CFG Physical Address
		Host Controller Interface Register	
0h	MMCSD0_SDMA_SYS_ADDR_LO	32-bit Block Count/SDMA System Address Low Register	0FA1 0000h
2h	MMCSD0_SDMA_SYS_ADDR_HI	32-bit Block Count/SDMA System Address High Register	0FA1 0002h
4h	MMCSD0_BLOCK_SIZE	16-bit Block Size Register	0FA1 0004h
6h	MMCSD0_BLOCK_COUNT	16-bit Block Count Register	0FA1 0006h
8h	MMCSD0_ARGUMENT1_LO	Argument1 Low Register	0FA1 0008h
Ah	MMCSD0_ARGUMENT1_HI	Argument1 High Register	0FA1 000Ah
Ch	MMCSD0_TRANSFER_MODE	Transfer Mode Register	0FA1 000Ch
Eh	MMCSD0_COMMAND	Command Register	0FA1 000Eh
10h to 1Eh	MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7	Response Register	0FA1 0010h to 0FA1 001Eh
20h	MMCSD0_DATA_PORT	Buffer Data Port Register	0FA1 0020h
24h	MMCSD0_PRESENTSTATE	Present State Register	0FA1 0024h
28h	MMCSD0_HOST_CONTROL1	Host Control 1 Register	0FA1 0028h
29h	MMCSD0_POWER_CONTROL	Power Control Register	0FA1 0029h
2Ah	MMCSD0_BLOCK_GAP_CONTROL	Block Gap Control Register	0FA1 002Ah
2Bh	MMCSD0_WAKEUP_CONTROL	Wakeup Control Register	0FA1 002Bh
2Ch	MMCSD0_CLOCK_CONTROL	Clock Control Register	0FA1 002Ch
2Eh	MMCSD0_TIMEOUT_CONTROL	Timeout Control Register	0FA1 002Eh
2Fh	MMCSD0_SOFTWARE_RESET	Software Reset Register	0FA1 002Fh
30h	MMCSD0_NORMAL_INTR_STS	Normal Interrupt Status Register	0FA1 0030h
32h	MMCSD0_ERROR_INTR_STS	Error Interrupt Status Register	0FA1 0032h
34h	MMCSD0_NORMAL_INTR_STS_ENA	Normal Interrupt Status Enable Register	0FA1 0034h
36h	MMCSD0_ERROR_INTR_STS_ENA	Error Interrupt Status Enable Register	0FA1 0036h
38h	MMCSD0_NORMAL_INTR_SIG_ENA	Normal Interrupt Signal Enable Register	0FA1 0038h
3Ah	MMCSD0_ERROR_INTR_SIG_ENA	Error Interrupt Signal Enable Register	0FA1 003Ah
3Ch	MMCSD0_AUTOCMD_ERR_STS	Auto CMD Error Status Register	0FA1 003Ch
3Eh	MMCSD0_HOST_CONTROL2	Host Control 2 Register	0FA1 003Eh
40h	MMCSD0_CAPABILITIES	Capabilities Register	0FA1 0040h
48h	MMCSD0_MAX_CURRENT_CAP	Maximum Current Capabilities Register	0FA1 0048h
50h	MMCSD0_FORCE_EVNT_ACMD_ERR_STS	Force Event Register for Auto CMD Error Status	0FA1 0050h

Table 14-23654. MMCSD0 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCSD0_CTL_CFG Physical Address
52h	MMCSD0_FORCE_EVNT_ERR_INT_STS	Force Event Register for Error Interrupt Status	0FA1 0052h
54h	MMCSD0_ADMA_ERR_STATUS	ADMA Error Status Register	0FA1 0054h
58h	MMCSD0_ADMA_SYS_ADDRESS	ADMA System Address Register	0FA1 0058h
60h	MMCSD0_PRESET_VALUE0	Preset Values 0 Register	0FA1 0060h
62h	MMCSD0_PRESET_VALUE1	Preset Values 1 Register	0FA1 0062h
64h	MMCSD0_PRESET_VALUE2	Preset Values 2 Register	0FA1 0064h
66h	MMCSD0_PRESET_VALUE3	Preset Values 3 Register	0FA1 0066h
68h	MMCSD0_PRESET_VALUE4	Preset Values 4 Register	0FA1 0068h
6Ah	MMCSD0_PRESET_VALUE5	Preset Values 5 Register	0FA1 006Ah
6Ch	MMCSD0_PRESET_VALUE6	Preset Values 6 Register	0FA1 006Ch
6Eh	MMCSD0_PRESET_VALUE7	Preset Values 7 Register	0FA1 006Eh
72h	MMCSD0_PRESET_VALUE8	Preset Values 8 Register	0FA1 0072h
74h	MMCSD0_PRESET_VALUE10	Preset Values 10 Register	0FA1 0074h
78h	MMCSD0_ADMA3_DESC_ADDRESS	ADMA3 Integrated Descriptor Address Register	0FA1 0078h
		UHS-II Registers (1)	
80h	MMCSD0_UHS2_BLOCK_SIZE	UHS-II Block Size Register	0FA1 0080h
84h	MMCSD0_UHS2_BLOCK_COUNT	UHS-II Block Count Register	0FA1 0084h
88h to 9Bh	MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19	UHS-II Command Packet Register	0FA1 0088h to 0FA1 009Bh
9Ch	MMCSD0_UHS2_XFER_MODE	UHS-II Transfer Mode Register	0FA1 009Ch
9Eh	MMCSD0_UHS2_COMMAND	UHS-II Command Register	0FA1 009Eh
A0h to B3h	MMCSD0_UHS2_RESPONSE_0 to MMCSD0_UHS2_RESPONSE_19	UHS-II Response Register	0FA1 00A0h to 0FA1 00B3h
B4h	MMCSD0_UHS2_MESSAGE_SELECT	UHS-II Message Select Register	0FA1 00B4h
B8h	MMCSD0_UHS2_MESSAGE	UHS-II Message Register	0FA1 00B8h
BCh	MMCSD0_UHS2_DEVICE_INTR_STATUS	UHS-II Device Interrupt Status Register	0FA1 00BCh
BEh	MMCSD0_UHS2_DEVICE_SELECT	UHS-II Device Select Register	0FA1 00BEh
BFh	MMCSD0_UHS2_DEVICE_INT_CODE	UHS-II Device Interrupt Code Register	0FA1 00BFh
C0h	MMCSD0_UHS2_SOFTWARE_RESET	UHS-II Software Reset Register	0FA1 00C0h
C2h	MMCSD0_UHS2_TIMER_CONTROL	UHS-II Timeout Control Register	0FA1 00C2h
C4h	MMCSD0_UHS2_ERR_INTR_STS	UHS-II Error Interrupt Status Register	0FA1 00C4h
C8h	MMCSD0_UHS2_ERR_INTR_STS_ENA	UHS-II Error Interrupt Status Enable Register	0FA1 00C8h
CCh	MMCSD0_UHS2_ERR_INTR_SIG_ENA	UHS-II Error Interrupt Signal Enable Register	0FA1 00CCh
E0h	MMCSD0_UHS2_SETTINGS_PTR	Pointer for UHS-II Settings Register	0FA1 00E0h
E2h	MMCSD0_UHS2_CAPABILITIES_PTR	Pointer for UHS-II Host Capabilities Register	0FA1 00E2h
E4h	MMCSD0_UHS2_TEST_PTR	Pointer for UHS-II Test Register	0FA1 00E4h
E6h	MMCSD0_SHARED_BUS_CTRL_PTR	Pointer for Embedded Control Register	0FA1 00E6h
E8h	MMCSD0_VENDOR_SPECFIC_PTR	Pointer for Vendor Specific Area Register	0FA1 00E8h
F4h	MMCSD0_BOOT_TIMEOUT_CONTROL	Boot Timeout Control Register	0FA1 00F4h
F8h	MMCSD0_VENDOR_REGISTER	Vendor Register	0FA1 00F8h
FCh	MMCSD0_SLOT_INT_STS	Slot Interrupt Status Register	0FA1 00FCh
FEh	MMCSD0_HOST_CONTROLLER_VER	Host Controller Version Register	0FA1 00FEh
100h	MMCSD0_UHS2_GEN_SETTINGS	UHS-II General Settings Register	0FA1 0100h
104h	MMCSD0_UHS2_PHY_SETTINGS	UHS-II PHY Settings Register	0FA1 0104h
108h	MMCSD0_UHS2_LNK_TRN_SETTINGS	UHS-II LINK/TRAN Settings Register	0FA1 0108h

Table 14-23654. MMCSD0 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCSD0_CTL_CFG Physical Address
110h	MMCSD0_UHS2_GEN_CAP	UHS-II General Capabilities Register	0FA1 0110h
114h	MMCSD0_UHS2_PHY_CAP	UHS-II PHY Capabilities Register	0FA1 0114h
118h	MMCSD0_UHS2_LNK_TRN_CAP	UHS-II LINK/TRAN Capabilities Register	0FA1 0118h
120h	MMCSD0_FORCE_UHSII_ERR_INT_STS	Force Event for UHS-II Error Interrupt Status Register	0FA1 0120h
		Command Queue Registers	
200h	MMCSD0_CQ_VERSION	Command Queueing Version Register	0FA1 0200h
204h	MMCSD0_CQ_CAPABILITIES	Command Queueing Capabilities Register	0FA1 0204h
208h	MMCSD0_CQ_CONFIG	Command Queueing Configuration Register	0FA1 0208h
20Ch	MMCSD0_CQ_CONTROL	Command Queueing Control Register	0FA1 020Ch
210h	MMCSD0_CQ_INTR_STS	Command Queueing Interrupt Status Register	0FA1 0210h
214h	MMCSD0_CQ_INTR_STS_ENA	Command Queueing Interrupt Status Enabled Register	0FA1 0214h
218h	MMCSD0_CQ_INTR_SIG_ENA	Command Queueing Interrupt Signal Enable Register	0FA1 0218h
21Ch	MMCSD0_CQ_INTR_COALESCING	Interrupt Coalescing Register	0FA1 021Ch
220h	MMCSD0_CQ_TDL_BASE_ADDR	Command Queueing Task Descriptor List Base Address Low Register	0FA1 0220h
224h	MMCSD0_CQ_TDL_BASE_ADDR_UPBITS	Command Queueing Task Descriptor List Base Address High Register	0FA1 0224h
228h	MMCSD0_CQ_TASK_DOOR_BELL	Command Queueing Task Doorbell Register	0FA1 0228h
22Ch	MMCSD0_CQ_TASK_COMP_NOTIF	Command Queueing Task Doorbell Notification Register	0FA1 022Ch
230h	MMCSD0_CQ_DEV_QUEUE_STATUS	Command Queueing Device Queue Status Register	0FA1 0230h
234h	MMCSD0_CQ_DEV_PENDING_TASKS	Command Queueing Device Pending Tasks Register	0FA1 0234h
238h	MMCSD0_CQ_TASK_CLEAR	Command Queueing Task Clear Register	0FA1 0238h
240h	MMCSD0_CQ_SEND_STS_CONFIG1	Send Status Timer Configuration 1 Register	0FA1 0240h
244h	MMCSD0_CQ_SEND_STS_CONFIG2	Send Status Configuration 2 Register	0FA1 0244h
248h	MMCSD0_CQ_DCMD_RESPONSE	Command Response Register for Direct Command Task	0FA1 0248h
250h	MMCSD0_CQ_RESP_ERR_MASK	Response Mode Error Mask Register	0FA1 0250h
254h	MMCSD0_CQ_TASK_ERR_INFO	Task Error Information Register	0FA1 0254h
258h	MMCSD0_CQ_CMD_RESP_INDEX	Command Response Index Register	0FA1 0258h
25Ch	MMCSD0_CQ_CMD_RESP_ARG	Command Response Argument Register	0FA1 025Ch
260h	MMCSD0_CQ_ERROR_TASK_ID	Command Queueing Error Task ID Register	0FA1 0260h

(1) UHSII is not supported. For more information, see *Not Supported Features*.

1 MMCSD0_SDMA_SYS_ADDR_LO Register (Offset = 0h) [reset = 0h]

MMCSD0_SDMA_SYS_ADDR_LO is shown in Figure 14-7817 and described in Table 14-15840.

Return to Summary Table.

This register contains the Lower 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

Table 14-23655. MMCSD0_SDMA_SYS_ADDR_LO Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0000h

Figure 14-7817. MMCSD0_SDMA_SYS_ADDR_LO Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMA_ADDRESS															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23657. MMCSD0_SDMA_SYS_ADDR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDMA_ADDRESS	R/W	0h	32-bit Block Count (SDMA System Address) Low When the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h, DMA uses this register as system address in only 32-bit addressing mode. Auto CMD23 cannot be used with SDMA. When the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, SDMA uses the MMCSD0_ADMA_SYS_ADDRESS register instead of using this register to support both 32-bit and 64-bit addressing. This register is re-assigned to 32-bit Block Count and then SDMA may use Auto CMD23. (1) SDMA System Address (MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h) This register contains the system memory address for a SDMA transfer in 32-bit addressing mode. When the Host Controller (HC) stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (after a transaction has stopped). Reading this register during SDMA transfers may return an invalid value. The Host Driver (HD) shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the MMCSD0_BLOCK_SIZE[14-12] SDMA_BUF_SIZE bit field. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (Offset = 3h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by setting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI). ADMA does not use this register. (2) 32-bit Block Count (MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h) Host Controller Version 4.10 re-defines this register as 32-bit Block Count . In version 4.00, this register may be used as 32-bit block count only for Auto CMD23 to set the argument of the CMD23 while executing Auto CMD23. The Host Controller would decrement the block count of this register every block transfer and data transfer stops when the count reaches zero. FFFF FFFFh (4G - 1 Block) .... 0000 0002h (2 Blocks) 0000 0001h (1 Block)

Table 14-23657. MMCSD0_SDMA_SYS_ADDR_LO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0000 0000h (Stop Count) **Note:** This register should be accessed only when no transaction is executing. Reading this register during data transfers may return invalid value.

2 MMCSD0_SDMA_SYS_ADDR_HI Register (Offset = 2h) [reset = 0h]

MMCSD0_SDMA_SYS_ADDR_HI is shown in Figure 14-7818 and described in Table 14-15842.

Return to Summary Table.

This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

Table 14-23658. MMCSD0_SDMA_SYS_ADDR_HI Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0002h

Figure 14-7818. MMCSD0_SDMA_SYS_ADDR_HI Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMA_ADDRESS															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23660. MMCSD0_SDMA_SYS_ADDR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDMA_ADDRESS	R/W	0h	32-bit Block Count (SDMA System Address) High This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

3 MMCSD0_BLOCK_SIZE Register (Offset = 4h) [reset = 0h]

MMCSD0_BLOCK_SIZE is shown in Figure 14-7819 and described in Table 14-15844.

Return to Summary Table.

This register is used to configure the number of bytes in a data block.

Table 14-23661. MMCSD0_BLOCK_SIZE Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0004h

Figure 14-7819. MMCSD0_BLOCK_SIZE Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">SDMA_BUF_SIZE</td><td colspan="4">XFER_BLK_SIZE</td></tr>
<tr><td>R-0h</td><td colspan="3">R/W-0h</td><td colspan="4">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">XFER_BLK_SIZE</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23663. MMCSD0_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	SDMA_BUF_SIZE	R/W	0h	Host SDMA Buffer Size To perform long DMA transfer, System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI). These bits shall support when the MMCSD0_CAPABILITIES[22] SDMA_SUPPORT bit is set to 1h and this function is active when the MMCSD0_TRANSFER_MODE[0] DMA_ENA bit is set to 1h. 0h: 4KB (Detects A11 Carry out) 1h: 8KB (Detects A12 Carry out) 2h: 16KB (Detects A13 Carry out) 3h: 32KB (Detects A14 Carry out) 4h: 64KB (Detects A15 Carry out) 5h: 128KB (Detects A16 Carry out) 6h: 256KB (Detects A17 Carry out) 7h: 512KB (Detects A18 Carry out)

Table 14-23663. MMCSD0_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	XFER_BLK_SIZE	R/W	0h	Transfer Block Size This field specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. It can be accessed only if no transaction is executing (after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. 0000h: No Data Transfer 0001h: 1 Byte 0002h: 2 Bytes 0003h: 3 Bytes 0004h: 4 Bytes .... 01FFh: 511 Bytes 0200h: 512 Bytes .... 0800h: 2048 Bytes

4 MMCSD0_BLOCK_COUNT Register (Offset = 6h) [reset = 0h]

MMCSD0_BLOCK_COUNT is shown in Figure 14-7820 and described in Table 14-15846.

Return to Summary Table.

This register is used to configure the number of data blocks.

Table 14-23664. MMCSD0_BLOCK_COUNT Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0006h

Figure 14-7820. MMCSD0_BLOCK_COUNT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XFER_BLK_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23666. MMCSD0_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	XFER_BLK_CNT	R/W	0h	16-bit Block Count Host Controller Version 4.10 extends block count to 32-bit . Selection of either 16-bit Block Count register or 32-bit Block Count register is defined as follows: (1) If the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h or 16-bit Block Count register is set to non-zero, 16-bit Block Count register is selected. (2) If the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h and 16-bit Block Count register is set to zero, 32-bit Block Count register is selected. Use of 16-bit/32-bit Block Count register is enabled when the MMCSD0_TRANSFER_MODE[1] BLK_CNT_ENA bit is set to 1h and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1h and the maximum block count. The Host Controller decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0h results in no data blocks is transferred. This register should be accessed only when no transaction is executing (after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. 0000h: Stop Count 0001h: 1 Block 0002h: 2 Blocks .... FFFFh: 65535 Blocks

5 MMCSD0_ARGUMENT1_LO Register (Offset = 8h) [reset = 0h]

MMCSD0_ARGUMENT1_LO is shown in Figure 14-7821 and described in Table 14-15848.

Return to Summary Table.

This register contains Lower bits of SD Command Argument.

Table 14-23667. MMCSD0_ARGUMENT1_LO Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0008h

Figure 14-7821. MMCSD0_ARGUMENT1_LO Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ARG1															
R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23669. MMCSD0_ARGUMENT1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_ARG1	R/W	0h	Command Argument 1 Low The SD Command Argument is specified as bit 23-8 of Command-Format.

6 MMCSD0_ARGUMENT1_HI Register (Offset = Ah) [reset = 0h]

MMCSD0_ARGUMENT1_HI is shown in Figure 14-7822 and described in Table 14-15850.

Return to Summary Table.

This register contains higher bits of SD Command Argument.

Table 14-23670. MMCSD0_ARGUMENT1_HI Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 000Ah

Figure 14-7822. MMCSD0_ARGUMENT1_HI Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ARG1															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23672. MMCSD0_ARGUMENT1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_ARG1	R/W	0h	Command Argument 1 High The SD Command Argument is specified as bit 39-24 of Command-Format.

7 MMCSD0_TRANSFER_MODE Register (Offset = Ch) [reset = 0h]

MMCSD0_TRANSFER_MODE is shown in Figure 14-7823 and described in Table 14-15852.

Return to Summary Table.

Table 14-23673. MMCSD0_TRANSFER_MODE Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 000Ch

Figure 14-7823. MMCSD0_TRANSFER_MODE Register

15	14	13	12	11	10	9	8
RESERVED							RESP_INTR_DIS
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESP_ERR_CHK_ENA	RESP_TYPE	MULTI_BLK_SEL	DATA_XFER_DIR	AUTO_CMD_ENA		BLK_CNT_ENA	DMA_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23675. MMCSD0_TRANSFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Response Interrupt Disable Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0h and waits Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE) and then checks the Response register (MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7). If Host Controller checks response error, sets this bit to 1h and sets the MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA bit to 1h. Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE) is disabled by this bit regardless of Command Complete Signal Enable (MMCSD0_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE). 0h: Response Interrupt is enabled 1h: Response Interrupt is disabled

Table 14-23675. MMCSD0_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESP_ERR_CHK_ENA	R/W	0h	Response Error Check Enable Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, this bit is set to 0h and the MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 0h. If Host Controller checks response error, sets this bit to 1h and sets the Response Interrupt Disable bit to 1h (MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS = 1h). The MMCSD0_TRANSFER_MODE[6] RESP_TYPE bit selects either R1 or R5 response type. If an error is detected, Response Error Interrupt is generated in the MMCSD0_ERROR_INTR_STS register. 0h: Response Error Check is disabled 1h: Response Error Check is enabled
6	RESP_TYPE	R/W	0h	Response Type R1/R5 When response error check is enabled (MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1h), this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1: Bit31 OUT_OF_RANGE Bit30 ADDRESS_ERROR Bit29 BLOCK_LEN_ERROR Bit26 WP_VIOLATION Bit25 CARD_IS_LOCKED Bit23 COM_CRC_ERROR Bit21 CARD_ECC_FAILED Bit20 CC_ERROR Bit19 ERROR Response Flags Checked in R5: Bit07 COM_CRC_ERROR Bit03 ERROR Bit01 FUNCTION_NUMBER Bit00 OUT_OF_RANGE 0h: R1 (Memory) 1h: R5 (SDIO)

Table 14-23675. MMCSD0_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MULTI_BLK_SEL	R/W	0h	Multi/Single Block Select This bit enables multiple block data transfers. 0h: Single Block 1h: Multiple Block
4	DATA_XFER_DIR	R/W	0h	Data Transfer Direction Select This bit defines the direction of data transfers. 0h: Write (Host to Card) 1h: Read (Card to Host)

Table 14-23675. MMCSD0_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	AUTO_CMD_ENA	R/W	0h	Auto CMD Enable This field determines use of auto command functions. There are three methods to stop Multiple-block read and write operation by CMD23 or CMD12. In the other operations (for example single read/write operation), this field is set to 0h. (1) Auto CMD12 Enable: Multiple-block read and write commands for memory require CMD12 to stop the operation. When this field is set to 1h, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the MMCSD0_AUTOCMD_ERR_STS register. The Host Driver shall not set this bit if the command does not require CMD12. When MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h, CMD12 is issued when 16-bit Block Count is expired. When MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h, CMD12 is issued when 16-bit Block Count or 32-bit Block Count is expired. (2) Auto CMD23 Enable: When this bit field is set to 2h, the Host Controller issues a CMD23 automatically before issuing a command specified in the MMCSD0_COMMAND register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23: Auto CMD23 Supported (Host Controller Version is 3.00 or later). A memory card that supports CMD23 (SCR[33] = 1h). If DMA is used, it shall be ADMA. Only when CMD18 or CMD25 is issued. Auto CMD23 can be used with or without ADMA. By writing the MMCSD0_COMMAND register, the Host Controller issues a CMD23 first and then issues a command specified by the MMCSD0_COMMAND[13:8] CMD_INDEX bit field. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the MMCSD0_AUTOCMD_ERR_STS register. 32-bit block count value for CMD23 is set to 32-bit Block Count (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) register. (3) Auto CMD Auto Select (Version 4.10): As CMD23 is optional for SD memory card except UHS 104 card, if card supports CMD23, Auto CMD 23 should be used instead of Auto CMD12. Host Controller Version 4.10 defines this "Auto CMD Auto Select" mode. Selection of Auto CMD depends on setting of the MMCSD0_HOST_CONTROL2[11] CMD23_ENA bit which indicates whether card supports CMD23. If MMCSD0_HOST_CONTROL2[11] CMD23_ENA = 1h, Auto CMD23 is used and if MMCSD0_HOST_CONTROL2[11] CMD23_ENA = 0h,

Table 14-23675. MMCSD0_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Auto CMD12 is used. In case of Version 4.10 or later, use of Auto CMD Auto Select is recommended rather than use of Auto CMD12 Enable or Auto CMD23 Enable. 0h: Auto Command Disabled 1h: Auto CMD12 Enable 2h: Auto CMD23 Enable 3h: Reserved
1	BLK_CNT_ENA	R/W	0h	Block Count Enable This bit is used to enable the MMCSD0_BLOCK_COUNT register, which is only relevant for multiple block transfers. When this bit is 0h, the MMCSD0_BLOCK_COUNT register is disabled, which is useful in executing an infinite transfer. 0h: Disable 1h: Enable
0	DMA_ENA	R/W	0h	DMA Enable DMA can be enabled only if the MMCSD0_CAPABILITIES[22] SDMA_SUPPORT bit is set. If this bit is set to 1h, a DMA operation shall begin when the HD writes to the upper byte of the MMCSD0_COMMAND register. 0h: Disable 1h: Enable

This register is used to control the operations of data transfers.

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data (Refer to MMCSD0_COMMAND[5] DATA_PRESENT bit), or before issuing a Resume command. The Host Driver shall save the value of this register when the data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller shall implement write protection for this register during data transactions. Writes to this register shall be ignored when the MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit is 1h.

Table 14-15853 shows the determination of transfer type.

Table 14-23676. Determination of Transfer Type

Multi/Single Block Select	Block Count Enable	Block Count	Function
0	Don't Care	Don't Care	Single Transfer
1	0	Don't Care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

8 MMCSD0_COMMAND Register (Offset = Eh) [reset = 0h]

MMCSD0_COMMAND is shown in Figure 14-7824 and described in Table 14-15855.

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This register is used to program the Command for host controller.

Table 14-23677. MMCSD0_COMMAND Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 000Eh

Figure 14-7824. MMCSD0_COMMAND Register

15	14	13	12	11	10	9	8
RESERVED		CMD_INDEX					
R-0h		R/W-0h					

7	6	5	4	3	2	1	0
CMD_TYPE		DATA_PRESENT	CMD_INDEX_CHK_ENA	CMD_CRC_CHK_ENA	SUB_CMD	RESP_TYPE_SEL	
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23679. MMCSD0_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	CMD_INDEX	R/W	0h	Command Index This bit shall be set to the command number (CMD0-63, ACMD0-63).

Table 14-23679. MMCSD0_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	CMD_TYPE	R/W	0h	Command Type There are three types of special commands. Suspend, Resume and Abort. These bits shall be set to 0h for all other commands. Suspend Command: If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state. and the HD shall restart the transfer by setting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit. Resume Command: The HD re-starts the data transfer by restoring the registers in the range of 04F8 0000h - 04F8 000Dh. The HC shall check for busy before starting write transfers. Abort Command: If this command is set when executing a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a write transfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset. 0h: Normal 1h: Suspend 2h: Resume 3h: Abort
5	DATA_PRESENT	R/W	0h	Data Present Select This bit is set to 1h to indicate that data is present and shall be transferred using the DAT line. If is set to 0h for the following: 1. Commands using only CMD line (for example CMD52). 2. Commands with no data transferbut using busy signal on DAT[0]line (R1b or R5b for example CMD38). 3. Resume Command. 0h: No Data Present 1h: Data Present
4	CMD_INDEX_CHK_ENA	R/W	0h	Command Index Check Enable If this bit is set to 1h, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0h, the Index field is not checked. 0h: Disable 1h: Enable

Table 14-23679. MMCSD0_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMD_CRC_CHK_ENA	R/W	0h	Command CRC Check Enable If this bit is set to 1h, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0h, the CRC field is not checked. 0h: Disable 1h: Enable
2	SUB_CMD	R/W	0h	Sub Command Flag This bit is added from Version 4.10 to distinguish a main command or sub command . When issuing a main command, this bit is set to 0h and when issuing a sub command, this bit is set to 1h. Setting of this bit is checked by the MMCSD0_PRESENTSTATE[28] SUB_COMMAND_STS bit. Host Driver manages whether main or sub command. Host Controller does not refer to this bit to issue a command. 0h: Sub Command 1h: Main Command
1-0	RESP_TYPE_SEL	R/W	0h	Response Type Select 0h: No Response 1h: Response length 136 2h: Response length 48 3h: Response length 48 check Busy after response

9 MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7 Register (Offset = 10h to 1Eh) [reset = 0h]

MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7 is shown in Figure 14-7825 and described in Table 14-15857.

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This registers is used to store responses from SD Cards.

Table 14-23680. MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0010h to 0FA1 001Eh

Figure 14-7825. MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_RESP															
R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23682. Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_RESP	R	0h	Command Response R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.

Table 14-15858 defines the relation between the parameter and name of response type.

Table 14-23683. Relation between Parameters and the Name of Response Type

Response Type	Index Check Enable	CRC Check Enable	Name of Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R6, R5, R7
11	1	1	R1b, R5b

The following table describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.

Table 14-15859 shows response bit definition for each response type.

Table 14-23684. Response Bit Definition for each Response Type

Kind of Response	Meaning of Response	Response Field	Response Register
R1, R1b (normal response)	Card Status	R[39:8]	REP[31:0]
R1b (Auto CMD12 response)	Card Status for Auto CMD12	R[39:8]	REP[127:96]
R1 (Auto CMD23 response)	Card Status for Auto CMD23	R[39:8]	REP [127:96]
R2 (CID, CSD Register)	CID or CSD register include	R[127:8]	REP[119:0]
R3 (OCR Register)	OCR Register for memory	R[39:8]	REP[31:0]
R4 (OCR Register)	OCR Register for I/O etc.	R[39:8]	REP[31:0]
R5, R5b	SDIO Response	R[39:8]	REP[31:0]

Table 14-23684. Response Bit Definition for each Response Type (continued)

Kind of Response	Meaning of Response	Response Field	Response Register
R6 (Published RCA response)	New published RCA[31:16] etc.	R[39:8]	REP[31:0]

The Response Field indicates bit positions of "Responses" defined in the Physical Layer Specification. The table shows most responses with a length of 48 (R[47:0]) have 32 bits of the response data (R[39:8]) stored in the Response register at REP[31:0]. Responses of type R1b (Auto CMD12 responses) and R1 (Auto CMD23 response) have response data bits R[39:8] stored in the Response register at REP[127:96]. Responses with length 136 (R[135:0]) have 120 bits of the response data (R[127:8]) stored in the Response register at REP[119:0].

To read the response status efficiently, the Host Controller only stores part of the response data in the Response register. This enables the Host Driver to read 32 bits of response data efficiently in one read cycle on a 32-bit bus system. Parts of the response, the Index field and the CRC, are checked by the Host Controller (as specified by the MMCSD0_COMMAND[4] CMD_INDEX_CHK_ENA and MMCSD0_COMMAND[3] CMD_CRC_CHK_ENA bits) and generate an error interrupt if an error is detected. The bit range for the CRC check depends on the response length. If the response length is 48, the Host Controller shall check R[47:1], and if the response length is 136 the Host Controller shall check R[119:1].

Since the Host Controller may have a multiple block data DAT line transfer executing concurrently with a CMD_wo_DAT command, the Host Controller stores the Auto CMD12 response in the upper bits (REP[127:96]) of the Response register. The CMD_wo_DAT response is stored in REP[31:0]. This allows the Host Controller to avoid overwriting the Auto CMD12 response with the CMD_wo_DAT and vice versa.

While executing Auto CMD23, the response of CMD23 is saved to REP [127:96] and the response of multiple-block read and write command is save to REP [31:0]. The response error of CMD23 is indicated in the MMCSD0_AUTOCMD_ERR_STS register. When the Host Controller modifies part of the Response register, as shown in the table, it shall preserve the unmodified bits.

10 MMCSD0_DATA_PORT Register (Offset = 20h) [reset = 0h]

MMCSD0_DATA_PORT is shown in Figure 14-7826 and described in Table 14-15861.

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This register is used to access internal buffer.

Table 14-23685. MMCSD0_DATA_PORT Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0020h

Figure 14-7826. MMCSD0_DATA_PORT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUF_RD_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23687. MMCSD0_DATA_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUF_RD_DATA	R/W	0h	Buffer Data The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

11 MMCSD0_PRESENTSTATE Register (Offset = 24h) [reset = 1F00000h]

MMCSD0_PRESENTSTATE is shown in Figure 14-7827 and described in Table 14-15863.

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The Host Driver can get status of the Host Controller from this 32-bit read-only register.

Table 14-23688. MMCSD0_PRESENTSTATE Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0024h

Figure 14-7827. MMCSD0_PRESENTSTATE Register

31	30	29	28	27	26	25	24
UHS2_IF_DETECTION	UHS2_IF_LANE_SYNC	UHS2_DORMANT	SUB_COMMAND_STS	CMD_NOT_ISS_BY_ERR	RESERVED		SDIF_CMDIN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		R-1h
23	22	21	20	19	18	17	16
SDIF_DAT3IN	SDIF_DAT2IN	SDIF_DAT1IN	SDIF_DAT0IN	WRITE_PROTECT	CARD_DETECT	CARD_STATE_STABLE	CARD_INSERTED
R-1h	R-1h	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED				BUF_RD_ENA	BUF_WR_ENA	RD_XFER_ACTIVE	WR_XFER_ACTIVE
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
SDIF_DAT7IN	SDIF_DAT6IN	SDIF_DAT5IN	SDIF_DAT4IN	RETUNING_REQ	DATA_LINE_ACTIVE	INHIBIT_DAT	INHIBIT_CMD
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23690. MMCSD0_PRESENTSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UHS2_IF_DETECTION	R	0h	UHS-II IF Detection (UHS-II Only) This status indicates whether a card supports UHS-II IF. This status is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). UHS-II interface initialization is activated by setting the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit. Host Controller drives STB.L on D0 lane from EIDL state and waits for receiving STB.L on D1 lane. This bit is set to 1h if STB.L is detected on D1 lane. Host Controller shall compensate latency from setting SD Clock Enable to output STB.L on D0 lane when reading this status . This bit may be read any time after setting SD Clock Enable for faster UHS-II IF detection but Host Driver shall check this status at least 200μs period from setting SD Clock Enable (MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA) until detecting UHS-II IF. After UHS-II IF is detected, this bit is cleared by when EIDL is detected on D0 lane, UHS-II Interface Enable is set to 0h (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or Host full reset is executed. 1h: UHS-II IF is detected 0h: UHS-II IF is not detected
30	UHS2_IF_LANE_SYNC	R	0h	Lane Synchronization (UHS-II Only) This status indicates whether lane is synchronized in UHS-II mode. This status is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). On detecting UHS-II Interface (D31 = 1h), Host Controller provides SYN LSS on D0 lane and waits for receiving SYN LSS on D1 lane. If SYN LSS is detected on D1 lane, Host Controller provides LIDL LSS on D0 lane and waits for receiving LIDL LSS on D1 lane. In case of Version 4.00, this bit indicates completion of Device PHY Initialization by detecting LIDL LSS on D1 lane. From Version 4.10, Host Controller may implement a specific PHY verification method and PHY Initialization Failure can be indicated by keeping this bit to 0h even LIDL LSS is detected on D1 lane. Host Driver detects PHY Initialization Failure by timeout. This bit is cleared by when D0 lane is set to EIDL, UHS-II Interface Enable is set to 0h (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or executes Host full reset. 1h: UHS-II PHY is initialized 0h: UHS-II PHY is not initialized

Table 14-23690. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	UHS2_DORMANT	R	0h	In Dormant State (UHS-II Only) This status indicates whether UHS-II lanes enter Dormant state. This function is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). On issuing GO_DORMAT_STATE command, "Go Dormant Command (7h)" is set to Command type in the UHS-II Command register (MMCSD0_UHS2_COMMAND[7:6] CMD_TYPE). This command type acts as a trigger to enter lanes into dormant state. Host Controller provides STB.H and EIDL on D0 lane and waits for receiving STB.H and EIDL on D1 lane. This bit is set to 1h after the time of T_DMT_ENTRY (750 RCLK cycle) or more from detecting EIDL on D1 lane. RCLK may be stopped in dormant state, by setting SD Clock Enable to 0h in the Clock Control register (MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA = 0h) while In Dormant State bit is set to 1h. On writing Clock Control register with setting SD Clock Enable to 1h (MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA = 1h), Host Controller wakes lanes to exit Dormant State and In Dormant State is set to 0h. In case of the card enters Hibernate Mode (RCLK is stopped), Host Driver may turn off VDD1 by clearing SD Bus Power for VDD1 bit in the MMCSD0_POWER_CONTROL register. Host Controller shall turn off VDD1 after stopping RCLK. This bit is cleared by when Host Controller drives STB.L on D0 lane, UHS-II Interface Enable is set to 0h (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or executes Host full reset. 1h: In DORMANT state 0h: Not in DORMANT state
28	SUB_COMMAND_STS	R	0h	Sub Command Status The MMCSD0_COMMAND register and Response register (MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7) are commonly used for main command and sub command. This status is used to distinguish which response error statuses, main command or sub command, indicated in the MMCSD0_ERROR_INTR_STS register or in the MMCSD0_UHS2_ERR_INTR_STS register. Just before reading of this register, the MMCSD0_COMMAND[2] SUB_CMD bit or the MMCSD0_UHS2_COMMAND register is copied to this status. This status is effective not only when Response Error interrupt is generated but also when data error interrupt is generated with Command Not Issued by Error (D27 of this register) or Auto CMD Error interrupt is generated with Command Not Issued by Error by Auto CMD12 in the MMCSD0_AUTOCMD_ERR_STS register. 1h: Sub Command Status 0h: Main Command Status

Table 14-23690. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMD_NOT_ISS_BY_ERR	R	0h	Command Not Issued by Error Setting of this status indicates that a command cannot be issued due to an error except Auto CMD12 error (equivalent error status by Auto CMD12 error is defined as Command Not Issued By Auto CMD12 Error in the MMCSD0_AUTOCMD_ERR_STS register). This status is set to 1h when Host Controller cannot issue a command after setting MMCSD0_COMMAND register or MMCSD0_UHS2_COMMAND register. Sub Command Status (D28) indicates which command is not issued (main or sub). 1h: Command cannot be issued 0h: No error for issuing a command
26-25	RESERVED	R	0h	Reserved
24	SDIF_CMDIN	R	1h	CMD Line Signal Level (SD Mode Only) This status is used to check CMD line level to recover from errors, and for debugging.
23	SDIF_DAT3IN	R	1h	DAT[3] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[3]. D23 - DAT[3]
22	SDIF_DAT2IN	R	1h	DAT[2] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[2]. D22 - DAT[2]
21	SDIF_DAT1IN	R	1h	DAT[1] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[1]. D21 - DAT[1]
20	SDIF_DAT0IN	R	1h	DAT[0] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D20 - DAT[0]
19	WRITE_PROTECT	R	0h	Write Protect Switch Pin Level The Write Protect Switch is supported for memory and combo cards.This bit reflects the SDWP# pin. 0h: Write protected (SDWP# = 1) 1h: Write enabled (SDWP# = 0)

Table 14-23690. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CARD_DETECT	R	0h	Card Detect Pin Level This bit reflects the inverse value of the SDCD# pin. 0h: No Card present (SDCD# = 1) 1h: Card present (SDCD# = 0)
17	CARD_STATE_STABLE	R	0h	Card State Stable This bit is used for testing. If it is 0h, the Card Detect Pin Level is not stable. If this bit is set to 1h, it means the Card Detect Pin Level is stable. The MMCSD0_SOFTWARE_RESET[0] SWRST_FOR_ALL bit shall not affect this bit. 0h: Reset of Debouncing 1h: No Card or Inserted
16	CARD_INSERTED	R	0h	Card Inserted This bit indicates whether a card has been inserted. Changing from 0h to 1h generates a Card Insertion interrupt in the MMCSD0_NORMAL_INTR_STS register and changing from 1h to h0 generates a Card Removal Interrupt in the MMCSD0_NORMAL_INTR_STS register. The MMCSD0_SOFTWARE_RESET[0] SWRST_FOR_ALL bit shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear the MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit and the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit. In addition the HD should clear the HC by the MMCSD0_SOFTWARE_RESET[0] SWRST_FOR_ALL bit. The card detect is active regardless of the SD Bus Power. 0h: Reset or Debouncing or No Card 1h: Card Inserted
15-12	RESERVED	R	0h	Reserved
11	BUF_RD_ENA	R	0h	Buffer Read Enable This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1h, readable data exists in the buffer. A change of this bit from 1h to 0h occurs when all the block data is read from the buffer. A change of this bit from 0h to 1h occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0h: Read Disable 1h: Read Enable

Table 14-23690. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	BUF_WR_ENA	R	0h	Buffer Write Enable This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1h, data can be written to the buffer. A change of this bit from 1h to 0h occurs when all the block data is written to the buffer. A change of this bit from 0h to 1h occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. 0h: Write Disable 1h: Write Enable
9	RD_XFER_ACTIVE	R	0h	Read Transfer Active (SD Mode Only) This status is used for detecting completion of a read transfer. This bit is set to 1h for either of the following conditions: After the end bit of the read command. When writing a 1h to continue Request in the MMCSD0_BLOCK_GAP_CONTROL register to restart a read transfer. This bit is cleared to 0h for either of the following conditions: When the last data block as specified by block length is transferred to the system. When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1h (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h). A transfer complete interrupt is generated when this bit changes to 0h. 1h: Transferring data 0h: No valid data

Table 14-23690. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WR_XFER_ACTIVE	R	0h	Write Transfer Active (SD Mode Only) This status indicates a write transfer is active. If this bit is 0h, it means no valid write data exists in the HC. This bit is set in either of the following cases: After the end bit of the write command. When writing a 1h to the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to restart a write transfer. This bit is cleared in either of the following cases: After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple). After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0h, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 1h: Transferring data 0h: No valid data
7	SDIF_DAT7IN	R	0h	DAT[7] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D07 - DAT[7]
6	SDIF_DAT6IN	R	0h	DAT[6] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D06 - DAT[6]
5	SDIF_DAT5IN	R	0h	DAT[5] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D05 - DAT[5]
4	SDIF_DAT4IN	R	0h	DAT[4] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D04 - DAT[4]

Table 14-23690. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RETUNING_REQ	R	0h	Re-Tuning Request (UHS-I Only) Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting the MMCSD0_HOST_CONTROL2[6] EXECUTE_TUNING bit. Changing of this bit from 0h to 1h generates Re-Tuning Event. This bit isn't set to 1h if the MMCSD0_HOST_CONTROL2[7] SAMPLING_CLK_SELECT bit is set to 0h (using fixed sampling clock). 1h: Sampling clock needs re-tuning 0h: Fixed or well tuned sampling clock
2	DATA_LINE_ACTIVE	R	0h	DAT Line Active (SD Mode Only) This bit indicates whether one of the DAT line on SD bus is in use. 1h: DAT line active 0h: DAT line inactive
1	INHIBIT_DAT	R	0h	Command Inhibit (DAT) (SD Mode Only) This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1h. If this bit is 0h, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (for example R1b, R5b type). Changing from 1h to 0h generates a Transfer Complete interrupt in the MMCSD0_NORMAL_INTR_STS register. **Note:** The SD Host Driver can save registers in the range of 04F8 0000h - 04F8 000Dh for a suspend transaction after this bit has changed from 1h to 0h. 1h: Cannot issue command which uses the DAT line 0h: Can issue command which uses the DAT line

Table 14-23690. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INHIBIT_CMD	R	0h	Command Inhibit (CMD) **SD Mode:** If this bit is 0h, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the MMCSD0_COMMAND register is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1h. Commands using only the CMD line can be issued if this bit is 0h. Changing from 1h to 0h generates a Command complete interrupt in the MMCSD0_NORMAL_INTR_STS register. If the HC cannot issuethe command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1h and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by the MMCSD0_COMMAND register. **UHS-II Mode:** This bit is 0h means that a command packet can be issued by the Host Controller. While this bit is set to 1h, which means the Host Controller is not ready to issue a next command, Host Driver shall not write the registers from the MMCSD0_UHS2_BLOCK_SIZE to the MMCSD0_UHS2_COMMAND. Changing from 1h to 0h generates a Command Complete Interrupt in the MMCSD0_NORMAL_INTR_STS register. 1h: Host Controller is not ready to issue a command 0h: Host Controller is ready to issue a command Version 4.10 adds a new control to prevent error statuses from overwriting by receipt of a next command. This status keeps indicating 1h while any of response error statuses is set to 1h , Command Not Issued by Error in this register is set to 1h or the MMCSD0_AUTOCMD_ERR_STS[7] CMD_NOT_ISSUED bit is set to 1h. Software Reset For CMD Lineis used to clear the error statuses above and this status (MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD).

Note: DAT line active indicates whether one of the DAT line is on SD bus is in use.

(a) In the case of read transactions

This status indicates whether a read transfer is executing on the SD Bus. Changing this value from 1h to 0h generates a Block Gap Event interrupt in the MMCSD0_NORMAL_INTR_STS register, as the result of the Stop At Block Gap Request being set.

This bit shall be set in either of the following cases:

(1) After the end bit of the read command.

(2) When writing a 1h to the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to restart a read transfer.

This bit shall be cleared in either of the following cases:

(1) When the end bit of the last data block is sent from the SD Bus to the Host Controller. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.

(2) When a read transfer is stopped at the block gap initiated by a Stop At Block Gap Request (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP).

The Host Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Host Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use suspend/resume function.

(b) In the case of write transactions

This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1h to 0h generate a Transfer Complete interrupt in the MMCSD0_NORMAL_INTR_STS register.

This bit shall be set in either of the following cases:

(1) After the end bit of the write command.

(2) When writing to 1h to the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to continue a write transfer.

This bit shall be cleared in either of the following cases:

(1) When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive "Not Busy". In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.

(2) When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP).

(c) Command with busy

This status indicates whether a command indicates busy (for example erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command with busy and cleared when busy is de-asserted. Changing this bit from 1h to 0h generate a Transfer Complete interrupt in the MMCSD0_NORMAL_INTR_STS register.

Note

The HD can issue cmd0, cmd12, cmd13 (for memory) and cmd52 (for SDIO) when the DAT lines are busy during data transfer. These commands can be issued when Command Inhibit (CMD) is set to zero (MMCSD0_PRESENTSTATE[0] INHIBIT_CMD = 0h). Other commands shall be issued when Command Inhibit (DAT) is set to zero (MMCSD0_PRESENTSTATE[1] INHIBIT_DAT = 0h).

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12 MMCSD0_HOST_CONTROL1 Register (Offset = 28h) [reset = 0h]

MMCSD0_HOST_CONTROL1 is shown in Figure 14-7828 and described in Table 14-15865.

Return to Summary Table.

This register is used to program DMA modes, LED control, data transfer width, High Speed enable, card detect test level and signal selection.

Table 14-23691. MMCSD0_HOST_CONTROL1 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0028h

Figure 14-7828. MMCSD0_HOST_CONTROL1 Register

7	6	5	4	3	2	1	0
CD_SIG_SEL	CD_TEST_LEVEL	EXT_DATA_WIDTH	DMA_SELECT		HIGH_SPEED_ENA	DATA_WIDTH	LED_CONTROL
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23693. MMCSD0_HOST_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CD_SIG_SEL	R/W	0h	Card Detect Signal Detection This bit selects source for card detection. 1h: The card detect test level is selected 0h: SDCD# is selected (for normal use)
6	CD_TEST_LEVEL	R/W	0h	Card Detect Test Level This bit is enabled while the Card Detect Signal Selection is set to 1h and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal interrupt status enable bit is set. 1h: Card Inserted 0h: No Card
5	EXT_DATA_WIDTH	R/W	0h	Extended Data Transfer Width (Embedded and SD Mode Only) This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the MMCSD0_CAPABILITIES register. If a device supports 8-bit bus mode, this bit may be set to 1h. If this bit is 0h, bus width is controlled by the MMCSD0_HOST_CONTROL1[1] DATA_WIDTH bit. This bit is not effective when multiple devices are installed on a bus slot (Slot Type is set to 2h in the MMCSD0_CAPABILITIES register). In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register (MMCSD0_SHARED_BUS_CTRL_PTR). 1h: 8-bit Bus Width 0h: Bus Width is Selected by Data Transfer Width

Table 14-23693. MMCSD0_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	DMA_SELECT	R/W	0h	DMA Select This field is used to select DMA type. The Host Driver shall check support of DMA modes by referring the MMCSD0_CAPABILITIES register. Selected DMA is enabled by the MMCSD0_TRANSFER_MODE[0] DMA_ENA bit in SD mode and the MMCSD0_UHS2_XFER_MODE[0] DMA_ENA bit in UHS-II mode. (1) Up to Version 3.00: When MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h, setting of this field is compatible to Host Controller Version 3.00. SDMA is initiated by writing to the MMCSD0_COMMAND register when this field is set to 0h and the SDMA System Address register (32-bit) is used (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI). SDMA does not support 64-bit addressing. ADMA2 is initiated by writing to the MMCSD0_COMMAND register when this field is set to 2h or 3h. Lower 32-bit of the ADMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) is used when this field is set to 2h and 64-bit of the ADMA System Address register is used when this field is set to 3h. Support of 64-bit System Addressing is indicated by the MMCSD0_CAPABILITIES[28] ADDR_64BIT_SUPPORT_V3 bit. 64-bit AMDA2 uses 96-bit Descriptor. 0h: SDMA is selected 1h: 32-bit Address ADMA1 is selected 2h: 32-bit Address ADMA2 is selected 3h: 64-bit Address ADMA2 is selected (Optional) (2) Version 4.00 or later: When the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, setting of this field is changed as follows. SDMA is initiated by Host Driver writes to the MMCSD0_COMMAND register when this field is set to 0h. ADMA2 is initiated by Host Driver writes to the MMCSD0_COMMAND register when this field is set to 2h or 3h and by ADMA3 sets to the ADMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) when this field is set to 3h. ADMA3 is initiated by Host Driver writes to the MMCSD0_ADMA3_DESC_ADDRESS register when this field is set to 3h. 0h: SDMA is selected 1h: Not Used (New assignment is not allowed) 2h: ADMA2 is selected (AMDA3 is not supported or disabled)

Table 14-23693. MMCSD0_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3h: ADMA2 or ADMA3 is selected Support of 64-bit DMA and 128-bit Descriptor is indicated by the MMCSD0_CAPABILITIES[27] ADDR_64BIT_SUPPORT_V4 bit. If the support bit is set to 1h, all supported DMAs (depends on Support, ADMA2 Support and ADMA3 Support) shall support 64-bit addressing. The MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit selects either 32-bit or 64-bit system addressing of DMAs.
2	HIGH_SPEED_ENA	R/W	0h	High Speed Enable (SD Mode Only) This bit is optional. Before setting this bit, the HD shall check the MMCSD0_CAPABILITIES[21] HIGH_SPEED_SUPPORT bit. If this bit is set to 0h (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/20 MHz for MMC). If this bit is set to 1h, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52 MHz for MMC)/208 MHz (for SD3.0). If the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1h, Host Driver needs to reset SD Clock Enable (MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA) before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. This bit is not effective in UHS-II mode. 1h: High Speed Mode 0h: Normal Speed Mode
1	DATA_WIDTH	R/W	0h	Data Transfer Width (SD Mode Only) This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. This bit is not effective in UHS-II mode. 1h: 4 bit mode 0h: 1 bit mode
0	LED_CONTROL	R/W	0h	LED Control This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. 1h: LED on 0h: LED off

13 MMCSD0_POWER_CONTROL Register (Offset = 29h) [reset = 0h]

MMCSD0_POWER_CONTROL is shown in Figure 14-7829 and described in Table 14-15867.

Return to Summary Table.

This register is used to program the SD Bus power and voltage level.

Table 14-23694. MMCSD0_POWER_CONTROL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0029h

Figure 14-7829. MMCSD0_POWER_CONTROL Register

7	6	5	4	3	2	1	0
UHS2_VOLTAGE			UHS2_POWER	SD_BUS_VOLTAGE			SD_BUS_POWER
R/W-0h			R/W-0h	R/W-0h			R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23696. MMCSD0_POWER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	UHS2_VOLTAGE	R/W	0h	SD Bus Voltage Select for VDD2 (UHS-II Only) This field determines supply voltage range to VDD2. This field can be set to 5h if the MMCSD0_CAPABILITIES[60] VDD2_1P8_SUPPORT bit is set to 1h. 111b: Not used 110b: Not used 101b: 1.8 V 100b: Reserved for 1.2 V 011b – 001b: Reserved 000b: VDD2 Not Supported
4	UHS2_POWER	R/W	0h	SD Bus Power for VDD2 (UHS-II Only) Setting this bit enables providing VDD2. 1h: Power on 0h: Power off
3-1	SD_BUS_VOLTAGE	R/W	0h	SD Bus Voltage Select for VDD1 By setting these bits, the HD selects the voltage level for the SD card. Before setting this register, the HD shall check the voltage support bits in the MMCSD0_CAPABILITIES register. If an unsupported voltage is selected, the Host System shall not supply SD bus voltage. 111b: 3.3 V (Flattop.) 110b: 3.0 V (Typ.) 101b: 1.8 V (Typ.) for Embedded 100b – 000b: Reserved

Table 14-23696. MMCSD0_POWER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SD_BUS_POWER	R/W	0h	SD Bus Power for VDD1 Before setting this bit, the SD host driver shall set SD Bus Voltage Select (MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE). If the HC detects the No Card State, this bit shall be cleared. If this bit is cleared, the Host Controller should immediately stop driving CMD and DAT[3:0] (tri-state), and drive SDCLK to low level. If card is connected to Host Controller, Host Controller shall set these lines to low before stopping to supply VDD1. In UHS-II mode, before clearing this bit, Host Driver shall clear the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit and before stopping to supply VDD1, Host Controller shall set DAT[2] to low if DAT[2] is used as out-of band interrupt. 1h: Power on 0h: Power off

14 MMCSD0_BLOCK_GAP_CONTROL Register (Offset = 2Ah) [reset = 80h]

MMCSD0_BLOCK_GAP_CONTROL is shown in Figure 14-7830 and described in Table 14-15869.

Return to Summary Table.

This register is used to program the block gap request, read wait control and interrupt at block gap.

Table 14-23697. MMCSD0_BLOCK_GAP_CONTROL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 002Ah

Figure 14-7830. MMCSD0_BLOCK_GAP_CONTROL Register

7	6	5	4	3	2	1	0
BOOT_ACK_ENA	ALT_BOOT_MODE	BOOT_ENABLE	RESERVED	INTRPT_AT_BLK_GAP	RDWAIT_CTRL	CONTINUE	STOP_AT_BLK_GAP
R/W-1h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-23699. MMCSD0_BLOCK_GAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOT_ACK_ENA	R/W	1h	Boot Acknowledge Check To check for the boot acknowledge in boot operation. 1h: Wait for boot ack from eMMC card 0h: Will not wait for boot ack from eMMC card
6	ALT_BOOT_MODE	R/W	0h	Alternative Boot Mode To start boot code access in alternative mode. 1h: To start alternate boot mode access 0h: To stop alternate boot mode access
5	BOOT_ENABLE	R/W	0h	Boot Enable To start boot code access. 1h: To start boot code access 0h: To stop boot code access
4	RESERVED	R	0h	Reserved
3	INTRPT_AT_BLK_GAP	R/W	0h	Interrupt At Block Gap (SD Mode Only) This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1h enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0h. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card.

Table 14-23699. MMCSD0_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RDWAIT_CTRL	R/W	0h	Read Wait Control (SD Mode Only) The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1h otherwise DAT line conflict may occur. If this bit is set to 0h, Suspend/Resume cannot be supported. In UHS-II mode, Read Wait is disabled and DAT[2] line is used for Interrupt Signal from UHS-II Card. 1h: Enable Read Wait Control 0h: Disable Read Wait Control
1	CONTINUE	R/W	0h	Continue Request This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0h (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 0h) and set this bit to restart the transfer. The Host Controller automatically clears this bit when the transaction re-starts. If MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h, any write to this bit is ignored. In SD mode, this bit is cleared in either of the following cases: 1) In the case of a read transaction, the DAT Line Active changes from 0h to 1h as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0h to 1h as the write transaction restarts. Therefore it is not necessary for Host driver to set this bit to 0h. If MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h, any write to this bit is ignored. 1h: Restart 0h: Ignored

Table 14-23699. MMCSD0_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	STOP_AT_BLK_GAP	R/W	0h	Stop At Block Gap Request This bit is used to stop executing a transaction at the next block gap for non-DMA, SDMA and ADMA transfers. Until the transfer complete is set to 1h, indicating a transfer completion the HD shall leave this bit set to 1h. Clearing both the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP and MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bits shall not cause the transaction to restart. The MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit is used to stop the read transaction at the block gap. The HC shall honour Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1h (MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL) = 1h). In case of write transfers in which the HD writes data to the MMCSD0_DATA_PORT register, the HD shall set this bit after all block data is written. If this bit is set to 1h, the HD shall not write data to the MMCSD0_DATA_PORT register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit (DAT) in the MMCSD0_PRESENTSTATE register. In case of UHS-II, a transaction can be stopped at the boundary of DATA Burst (Flow Control basis). Host Controller waits for sending Flow Control MSG until the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit is set to 1h. 1h: Stop 0h: Transfer

There are three cases to restart the transfer after stop at the block gap. Which case is appropriate depends on whether the HC issues a Suspend command or the SD card accepts the Suspend command.

1. If the HD does not issue Suspend command, the Continue Request shall be used to restart the transfer.

2. If the HD issues a Suspend command and the SD card accepts it, a Resume Command shall be used to restart the transfer.

3. If the HD issues a Suspend command and the SD card does not accept it, the Continue Request shall be used to restart the transfer.

Any time Stop At Block Gap Request stops the data transfer, the HD shall wait for Transfer Complete (in the MMCSD0_NORMAL_INTR_STS register) before attempting to restart the transfer. When restarting the data transfer by Continue Request, the HD shall clear Stop At Block Gap Request before or simultaneously.

Host Controller should not generate timeout interrupts while Stop At Block Gap is set. Host Driver should ignore timeout interrupts while Stop At Block Gap is set.

15 MMCSD0_WAKEUP_CONTROL Register (Offset = 2Bh) [reset = 0h]

MMCSD0_WAKEUP_CONTROL is shown in Figure 14-7831 and described in Table 14-15871.

Return to Summary Table.

This register is used to program the wakeup functionality.

The MMCSD0_WAKEUP_CONTROL register is mandatory for the HC, but wakeup functionality depends on the HC system hardware and software. The HD shall maintain voltage on the SD Bus, by setting the MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit to 1h, when wakeup event via card interrupt is desired.

Table 14-23700. MMCSD0_WAKEUP_CONTROL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 002Bh

Figure 14-7831. MMCSD0_WAKEUP_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED					CARD_REMOVAL	CARD_INSERTION	CARD_INTERRUPT
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23702. MMCSD0_WAKEUP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	CARD_REMOVAL	R/W	0h	Wakeup Event Enable On SD Card Removal This bit enables wakeup event via Card removal assertion in the MMCSD0_NORMAL_INTR_STS register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1h: Enable 0h: Disable
1	CARD_INSERTION	R/W	0h	Wakeup Event Enable On SD Card Insertion This bit enables wakeup event via Card Insertion assertion in the MMCSD0_NORMAL_INTR_STS register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1h: Enable 0h: Disable
0	CARD_INTERRUPT	R/W	0h	Wakeup Event Enable On Card Interrupt This bit enables wakeup event via Card Interrupt assertion in the MMCSD0_NORMAL_INTR_STS register. This bit can be set to 1h if FN_WUS (Wake Up Support) in CIS is set to 1h. 1h: Enable 0h: Disable

16 MMCSD0_CLOCK_CONTROL Register (Offset = 2Ch) [reset = 0h]

MMCSD0_CLOCK_CONTROL is shown in Figure 14-7832 and described in Table 14-15873.

Return to Summary Table.

This register is used to program the Clock frequency select, Clock generator select, Clock enable, Internal clock state fields.

At the initialization of the HC, the HD shall set the SDCLK Frequency Select (MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL) according to the MMCSD0_CAPABILITIES register. This register controls SDCLK in SD Mode and RCLK in UHS-II mode.

Table 14-23703. MMCSD0_CLOCK_CONTROL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 002Ch

Figure 14-7832. MMCSD0_CLOCK_CONTROL Register

15	14	13	12	11	10	9	8
SDCLK_FRQSEL							
R/W-0h							

7	6	5	4	3	2	1	0
SDCLK_FRQSEL_UPBITS		CLKGEN_SEL	RESERVED	PLL_ENA	SD_CLK_ENA	INT_CLK_STABLE	INT_CLK_ENA
R/W-0h		R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23705. MMCSD0_CLOCK_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	SDCLK_FRQSEL	R/W	0h	SDCLK/RCLK Frequency Select This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the Capabilities register (MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ). Only the following settings are allowed. (1) 8-bit Divided Clock Mode: 80h: base clock divided by 256 40h: base clock divided by 128 20h: base clock divided by 64 10h: base clock divided by 32 08h: base clock divided by 16 04h: base clock divided by 8 02h: base clock divided by 4 01h: base clock divided by 2 00h: base clock (10 MHz - 63 MHz) Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The three default divider values can be calculated by the frequency that is defined by the MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ bit field. 400 KHz divider value 25 MHz divider value 50 MHz divider value According to the Physical Layer Specification, the maximum SD Clock frequency is 25 MHz in normal speed mode and 50 MHz in high speed mode, and shall never exceed this limit. The frequency of SDCLK is set by the following formula: Clock Frequency = (Base Clock) / divisor Thus, choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. For example, if the MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ bit field has the value 33 MHz, and the target frequency is 25 MHz, then choosing the divisor value of 1h will yield 16.5 MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400 KHz, the divisor value of 40h yields the optimal clock value of 258 KHz. (2) 10-bit Divided Clock Mode: Host Controller Version 3.00 or later supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits and all divider values shall be supported. 3FFh: 1/2046 Divided Clock

Table 14-23705. MMCSD0_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				N: 1/2N Divided Clock (Duty 50%) 002h: 1/4 Divided Clock 001h: 1/2 Divided Clock 000h: Base Clock (10 MHz - 254 MHz) (3) Programmable Clock Mode: Host Controller Version 3.00 or later supports this mode as optional. A non-zero value set to the MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field indicates support of this clock mode. The multiplier enables the Host System to select a finer grain SD clock frequency. It is not necessary to support all frequency generation specified by this field because programmable clock generator is vendor specific and dependent on the implementation. Therefore, this mode is used with Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10). The Host Controller vendor provides possible settings and the Host System vendor sets appropriate values to the Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10). 3FFh - Base Clock × M / 1024 .... N-1 - Base Clock × M / N .... 002h - Base Clock × M / 3 001h - Base Clock × M / 2 000h - Base Clock × M This field depends on setting of the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this field is set by Host Driver. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this field is automatically set to a value specified in one of Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10).
7-6	SDCLK_FRQSEL_UPBITS	R/W	0h	Upper Bits of SDCLK/RCLK Frequency Select This bit field is assigned to the MMCSD0_CLOCK_CONTROL[9-8] SDCLK_FRQSEL bit field of clock divider in SDCLK/RCLK Frequency Select.

Table 14-23705. MMCSD0_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLKGEN_SEL	R/W	0h	Clock Generator Select This bit is used to select the clock generator mode in SDCLK/ RCLK Frequency Select (MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL). If the Programmable Clock Mode is supported (non-zero value is set to the MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field), this bit attribute is R/W, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this bit is set by Host Driver. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this bit is automatically set to a value specified in one of Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10). 1h: Programmable Clock Mode 0h: Divided Clock Mode
4	RESERVED	R	0h	Reserved
3	PLL_ENA	R/W	0h	PLL Enable This bit is added from Version 4.10 for Host Controller using PLL. This feature allows Host Controller to initialize clock generator in two steps: by Internal Clock Enable (MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA) and PLL Enable and to minimize output latency (for example SDCLK/RCLK, D0 lane) from SD Clock Enable (MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA). There are two modes to keep Host Drivers compatibility. In both modes, PLL Locked timing is indicated by Internal Clock Stable (MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE). (1) When MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h (Host Driver Version 3, which does not support this bit) or this bit is not implemented, the MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA bit (or the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit) may activate PLL (exit low power mode and start locking clock). (2) When MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h (Host Driver Version 4), the MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA bit is set before setting this bit and then setting this bit may activate PLL (exit low power mode and start locking clock). 1h: PLL is enabled 0h: PLL is in low power mode

Table 14-23705. MMCSD0_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SD_CLK_ENA	R/W	0h	SD Clock Enable The HC shall stop SDCLK when writing this bit to 0h. The MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field can be changed when this bit is 0h. Then, the HC shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK = 0). If the HC detects the No Card state, this bit shall be cleared. 1h: Enable providing SDCLK or RCLK 0h: Disable providing SDCLK or RCLK
1	INT_CLK_STABLE	R	0h	Internal Clock Stable This bit is set to 1h when SD clock is stable after writing 1h to MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA bit. The SD Host Driver shall wait to set the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit until this bit is set to 1h. **Note:** This is useful when using PLL for a clock oscillator that requires setup time. (1) Internal Clock Stable (when MMCSD0_CLOCK_CONTROL[3] PLL_ENA = 0h or not supported) This bit is set to 1h when internal clock is stable after writing 1h to MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA bit. (2) PLL Clock Stable (when MMCSD0_CLOCK_CONTROL[3] PLL_ENA = 1h) Host Controller which supports PLL Enable sets this status to 0h once when PLL Enable is changed 0h to 1h and then this status is set to 1h when PLL is locked (PLL uses an internal clock in stable as a reference clock which is enabled by the MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA bit). After this bit is set to 1h, Host Driver may set the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit. 1h: Ready 0h: Not Ready
0	INT_CLK_ENA	R/W	0h	Internal Clock Enable This bit is set to 0h when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1h. When clock oscillation is stable, the HC shall set the MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE bit to 1h. This bit shall not affect card detection. 1h: Oscillate 0h: Stop

17 MMCSD0_TIMEOUT_CONTROL Register (Offset = 2Eh) [reset = 0h]

MMCSD0_TIMEOUT_CONTROL is shown in Figure 14-7833 and described in Table 14-15875.

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The register sets the data timeout counter value.

At the initialization of the HC, the HD shall set the Data Timeout Counter Value according to the MMCSD0_CAPABILITIES register.

Table 14-23706. MMCSD0_TIMEOUT_CONTROL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 002Eh

Figure 14-7833. MMCSD0_TIMEOUT_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED				COUNTER_VALUE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23708. MMCSD0_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	COUNTER_VALUE	R/W	0h	Data Timeout Counter Value This value determines the interval by which DAT line time-outs are detected. Refer to the MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT bit for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the SD clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT bit. 1111: Reserved 1110: TMCLK × 2^{27} -------------------- -------------------- 0001: TMCLK × 2^{14} 0000: TMCLK × 2^{13}

18 MMCSD0_SOFTWARE_RESET Register (Offset = 2Fh) [reset = 0h]

MMCSD0_SOFTWARE_RESET is shown in Figure 14-7834 and described in Table 14-15877.

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This register is used to program the software reset for data, command and for all.

A reset pulse is generated when writing 1h to each bit of this register. After completing the reset, the HC shall clear each bit. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0h.

Table 14-23709. MMCSD0_SOFTWARE_RESET Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 002Fh

Figure 14-7834. MMCSD0_SOFTWARE_RESET Register

7	6	5	4	3	2	1	0
RESERVED					SWRST_FOR_DAT	SWRST_FOR_CMD	SWRST_FOR_ALL
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23711. MMCSD0_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved

Table 14-23711. MMCSD0_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SWRST_FOR_DAT	R/W	0h	Software Reset for DAT Line (SD Mode Only) Only part of data circuit is reset. The following registers and bits are cleared by this bit: MMCSD0_DATA_PORT Buffer is cleared and Initialized. MMCSD0_PRESENTSTATE Buffer read Enable Buffer write Enable Read Transfer Active Write Transfer Active DAT Line Active Command Inhibit (DAT) MMCSD0_BLOCK_GAP_CONTROL Continue Request Stop At Block Gap Request MMCSD0_NORMAL_INTR_ST Buffer Read Ready Buffer Write Ready Block Gap Event Transfer Complete 1h: Reset 0h: Work

Table 14-23711. MMCSD0_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SWRST_FOR_CMD	R/W	0h	Software Reset for CMD Line (SD Mode Only) Only part of command circuit is reset to be able to issue a command. From Version 4.10, this bit is also used to initialize UHS-II command circuit. This reset is effective only command issuing circuit (including response error statuses related to Command Inhibit (CMD) control - MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit) and does not affect data transfer circuit. Host Controller can continue data transfer even this reset is executed during handling of sub command response errors. The following registers and bits are cleared by this bit: MMCSD0_PRESENTSTATE register: Command Inhibit (CMD) MMCSD0_NORMAL_INTR_STS register: Command Complete MMCSD0_ERROR_INTR_STS register (Error Interrupt Status from Version 4.10) Response error statuses related to Command Inhibit (CMD) - MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit 1h: Reset 0h: Work
0	SWRST_FOR_ALL	R/W	0h	Software Reset for All This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0h. During its initialization, the HD shall set this bit to 1h to reset the HC. The HC shall reset this bit to 0h when Capabilities registers are valid and the HD can read them. Additional use of 'Software Reset For All' may not affect the value of the Capabilities registers. If this bit is set to 1h, the SD card shall reset itself and must be re-initialized by the HD. 1h: Reset 0h: Work

19 MMCSD0_NORMAL_INTR_STS Register (Offset = 30h) [reset = 0h]

MMCSD0_NORMAL_INTR_STS is shown in Figure 14-7835 and described in Table 14-15879.

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This register gives the status of all the interrupts.

The Normal Interrupt Signal Enable (see MMCSD0_NORMAL_INTR_SIG_ENA register) affects read of this register, but Normal Interrupt Signal does not affect these reads. An Interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1h. For all bits except Card Interrupt (MMCSD0_NORMAL_INTR_STS[8] CARD_INTR) and Error Interrupt (MMCSD0_NORMAL_INTR_STS[15] ERROR_INTR), writing 1h to a bit clears it. The MMCSD0_NORMAL_INTR_STS[8] CARD_INTR bit is cleared when the card stops asserting the interrupt: that is when the Card Driver services the Interrupt condition.

Table 14-23712. MMCSD0_NORMAL_INTR_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0030h

Figure 14-7835. MMCSD0_NORMAL_INTR_STS Register

15	14	13	12	11	10	9	8
ERROR_INTR	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTR
R-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REM	CARD_INS	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-23714. MMCSD0_NORMAL_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ERROR_INTR	R	0h	Error Interrupt If any of the bits in the MMCSD0_ERROR_INTR_STS register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. In UHS-II mode is enabled, if any of the bits in the MMCSD0_UHS2_ERR_INTR_STS register are set, this bit is also set. 0h: No Error 1h: Error
14	BOOT_COMPLETE	R/W1C	0h	Boot Terminate Interrupt This status is set if the boot operation gets terminated. 0h: Boot operation is not terminated 1h: Boot operation is terminated

Table 14-23714. MMCSD0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RCV_BOOT_ACK	R/W1C	0h	Boot Acknowledge Receive This status is set if the boot acknowledge is received from device. 0h: Boot acknowledge is not received 1h: Boot acknowledge is received
12	RETUNING_EVENT	R	0h	Re-Tuning Event (UHS-I Only) This status is set if the MMCSD0_PRESENTSTATE[3] RETUNING_REQ bit changes from 0h to 1h. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. In UHS-II mode, this bit is not effective. 1h: Re-Tuning should be performed 0h: Re-Tuning is not required
11	INTC	R	0h	int_c (Embedded) This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_C interrupt factor.
10	INTB	R	0h	int_b (Embedded) This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_B interrupt factor.
9	INTA	R	0h	int_a (Embedded) This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_A interrupt factor.

Table 14-23714. MMCSD0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CARD_INTR	R	0h	Card Interrupt When this status has been set and the Host Driver needs to start this interrupt service, the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit may be set to 0h in order to clear the card interrupt status latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (it should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 1h and start sampling the interrupt signal again. Writing this bit to 1h does not clear this bit. It is cleared by resetting the SD card interrupt factor. (1) DAT[1] Interrupt Input in SD Mode In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of UHS-I mode, switching time of Interrupt Period is relaxed for 2 clock cycles. Then Host Controller needs to delay start of interrupt sampling at least 2 clocks and should sample interrupt while Interrupt Period is stable. (2) DAT[2] Interrupt Input in UHS-II Mode When the MMCSD0_PRESENTSTATE[16] CARD_INSERTED and MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bits are set to 1h, Host Controller configures DAT[2] as Interrupt Input and enables pull-up of DAT[2]. DAT[2] interrupt is asynchronous to RCLK, low level sensitive and 3.3 V signal level. DAT[2] interrupt is masked by setting the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 0h. When either the MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit or the MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit is set to 0h, Host Controller sets DAT[2] to low. Only point to point connection is allowed between Host and Card. (3) INT MSG in UHS-II Mode INT MSG is enabled by setting the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit. DAT[2] and INT MSG interrupt sources are ORed and indicated to Card Interrupt. If any bit in the MMCSD0_UHS2_DEVICE_INTR_STATUS register is set to 1h, INT MSG interrupt is generated. INT MSG interrupt is cleared by writing a correspondent bit to 1h in the MMCSD0_UHS2_DEVICE_INTR_STATUS register. Masking DAT[2] interrupt also disables INT MSG interupt due to the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit is set to 0h. SDIO Version 4.00 does not support INT MSG. 1h: Generate Card Interrupt 0h: No Card Interrupt

Table 14-23714. MMCSD0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CARD_REM	R/W1C	0h	Card Removal This status is set if the MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit changes from 1h to 0h. When the HD writes this bit to 1h to clear this status the status of the MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0h: Card State Stable or Debouncing 1h: Card Removed
6	CARD_INS	R/W1C	0h	Card Insertion This status is set if the MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit changes from 0h to 1h. When the HD writes this bit to 1h to clear this status the status of the MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0h: Card State Stable or Debouncing 1h: Card Inserted
5	BUF_RD_READY	R/W1C	0h	Buffer Read Ready This status is set if the MMCSD0_PRESENTSTATE[11] BUF_RD_ENA bit changes from 0h to 1h. The MMCSD0_PRESENTSTATE[11] BUF_RD_ENA bit is set to 1h for every CMD19 execution in tuning procedure. In UHS-II mode, this bit is set at FC (Flow Control) unit basis. 0h: Not Ready to read Buffer 1h: Ready to read Buffer
4	BUF_WR_READY	R/W1C	0h	Buffer Write Ready This status is set if the MMCSD0_PRESENTSTATE[10] BUF_WR_ENA bit changes from 0h to 1h. In UHS-II mode, this bit is set at FC (Flow Control) unit basis. 0h: Not Ready to Write Buffer 1h: Ready to Write Buffer
3	DMA_INTERRUPT	R/W1C	0h	DMA Interrupt This status is set if the HC detects the Host DMA Buffer Boundary in the MMCSD0_BLOCK_SIZE regiser. 0h: No DMA Interrupt 1h: DMA Interrupt is Generated

Table 14-23714. MMCSD0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BLK_GAP_EVENT	R/W1C	0h	Block Gap Event If the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set, this bit is set. Read Transaction: This bit is set at the falling edge of the DAT Line Active Status (see MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit). When the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function. Write Transaction: This bit is set at the falling edge of Write Transfer Active Status (see MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit). After getting CRC status at SD Bus timing. In UHS-II mode, this bit is set at FC (Flow Control) unit basis. 0h: No Block Gap Event 1h: Transaction stopped at Block Gap

Table 14-23714. MMCSD0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XFER_COMPLETE	R/W1C	0h	Transfer Complete This bit is set when a read/write transaction is completed. **SD Mode** Read Transaction: This bit is set at the falling edge of Read Transfer Active Status (MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE). There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length (after the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit (after valid data has been read to the Host System). Write Transaction: This bit is set at the falling edge of the DAT Line Active Status (see MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit). There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and data transfers completed (after valid data is written to the SD card and the busy signal is released). **Note:** MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit has higher priority than the MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If both bits are set to 1h, the data transfer can be considered complete. **Note:** While performing tuning procedure (the MMCSD0_HOST_CONTROL2[6] EXECUTE_TUNING bit is set to 1h), the MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is not set to 1h. Command with Busy: This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit (DAT) in the MMCSD0_PRESENTSTATE register. **UHS-I mode** While performing tuning procedure (the MMCSD0_HOST_CONTROL2[6] EXECUTE_TUNING bit is set to 1h), the MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is not set to 1h. 0h: No Data Transfer Complete 1h: Data Transfer Complete **UHS-II Mode** This interrupt is generated in following two cases: (a) EBSY Completion (for EBSY supported commands)

Table 14-23714. MMCSD0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				When the MMCSD0_UHS2_XFER_MODE[14] EBSY_WAIT bit is set to 1h, this bit is set when EBSY packet has been received, and all valid data have been sent to system memory in case of read operation. (b) Stop and Continue during DCMD Data Transfer When the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1h and data transfer is stopped at the Flow Control. Following is for both SD mode and UHS-II mode. The table below shows that the MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit has higher priority than the MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If both bits are set to 1h, execution of a command can be considered to be completed. 1h: Command execution is completed 0h: Not complete
0	CMD_COMPLETE	R/W1C	0h	Command Complete **SD Mode** This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23). **Note:** The MMCSD0_ERROR_INTR_STS[0] CMD_TIMEOUT bit has higher priority than the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit. If both are set to 1h, it can be considered that the response was not received correctly. Version 4.00 defines response check function for R1 and R5. If the MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1h, generation of this interrupt is prohibited regardless of the MMCSD0_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit. **UHS-II Mode** If the MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 0h, this interrupt is generated when response packet is received. If the MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1h, generation of this interrupt is prohibited regardless of the MMCSD0_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit. 0h: No Command Complete 1h: Command Complete

Table 14-15880 shows the relation between transfer complete and data timeout error.

Table 14-23715. Relation between transfer complete and data timeout error

Transfer Complete	Data Timeout Error	Meaning of the Status
0	0	Interrupted by Another Factor
0	1	Timeout occur during transfer
1	Don't Care	Data Transfer Complete

Table 14-15881 shows the relation between command complete and command timeout error.

Table 14-23716. Relation between command complete and command timeout error

Command Complete	Command Timeout Error	Meaning of the Status
0	0	Interrupted by Another Factor
Don't Care	1	Response not received within 64 SDCLK cycles
1	0	Response Received

20 MMCSD0_ERROR_INTR_STS Register (Offset = 32h) [reset = 0h]

MMCSD0_ERROR_INTR_STS is shown in Figure 14-7836 and described in Table 14-15883.

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This register gives the status of the error interrupts.

Status defined in this register can be enabled by the MMCSD0_ERROR_INTR_STS_ENA register, but not by the MMCSD0_ERROR_INTR_SIG_ENA register. The Interrupt is generated when the MMCSD0_ERROR_INTR_SIG_ENA register is enabled and at least one of the statuses is set to 1h. Writing to 1h clears the bit and writing to 0h keeps the bit unchanged. More than one status can be cleared at the one register write.

Table 14-23717. MMCSD0_ERROR_INTR_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0032h

Figure 14-7836. MMCSD0_ERROR_INTR_STS Register

15	14	13	12	11	10	9	8
RESERVED			HOST	RESP	RESERVED	ADMA	AUTO_CMD
R-0h			R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h

7	6	5	4	3	2	1	0
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-23719. MMCSD0_ERROR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	HOST	R/W1C	0h	Target Response Error Occurs when detecting ERROR in m_hresp (DMA transaction) 0h: No error 1h: Error
11	RESP	R/W1C	0h	Response Error (SD Mode Only) Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If the MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA bit is set to 1h, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1h. 0h: No error 1h: Error
10	RESERVED	R	0h	Reserved

Table 14-23719. MMCSD0_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ADMA	R/W1C	0h	ADMA Error This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the MMCSD0_ADMA_ERR_STATUS register. 0h: No error 1h: Error
8	AUTO_CMD	R/W1C	0h	Auto CMD Error (SD Mode Only) Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that any of the bits D00 to D05 in the MMCSD0_AUTOCMD_ERR_STS register has changed from 0h to 1h. D07 is effective in case of Auto CMD12. The MMCSD0_AUTOCMD_ERR_STS register is valid while this bit is set to 1h and may be cleared with clearing of this bit (another implementation is also allowed). 0h: No error 1h: Error
7	CURR_LIMIT	R/W1C	0h	Current Limit Error By setting the MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1h means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function. 0h: No error 1h: Power Fail
6	DATA_ENDBIT	R/W1C	0h	Data End Bit Error (SD Mode Only) Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0h: No error 1h: Error
5	DATA_CRC	R/W1C	0h	Data CRC Error (SD Mode Only) Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 2h. 0h: No error 1h: Error

Table 14-23719. MMCSD0_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DATA_TIMEOUT	R/W1C	0h	Data Timeout Error (SD Mode Only) Occurs when detecting one of following timeout conditions: 1. Busy Timeout for R1b, R5b type 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0h: No error 1h: Timeout
3	CMD_INDEX	R/W1C	0h	Command Index Error (SD Mode Only) Occurs if a Command Index error occurs in the Command Response (MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7). 0h: No error 1h: Error
2	CMD_ENDBIT	R/W1C	0h	Command End Bit Error (SD Mode Only) Occurs when detecting that the end bit of a command response is 0h. 0h: No error 1h: End Bit Error Generated
1	CMD_CRC	R/W1C	0h	Command CRC Error (SD Mode Only) Command CRC Error is generated in two cases. 1. If a response is returned and the MMCSD0_ERROR_INTR_STS[0] CMD_TIMEOUT bit is set to 0h, this bit is set to 1h when detecting a CRT error in the command response. 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (Stop driving CMD line) and set this bit to 1h. The MMCSD0_ERROR_INTR_STS[0] CMD_TIMEOUT bit shall also be set to 1h to distinguish CMD line conflict. 0h: No error 1h: CRC Error Generated

Table 14-23719. MMCSD0_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMD_TIMEOUT	R/W1C	0h	Command Timeout Error (SD Mode Only) Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case the MMCSD0_ERROR_INTR_STS[1] CMD_CRC bit shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. 0h: No error 1h: Timeout

Table 14-15884 shows the relation between command CRC error and command time-out error.

Table 14-23720. Relation between command CRC error and command time-out error

Command CRC Error	Command Time-out Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD Line Conflict

21 MMCSD0_NORMAL_INTR_STS_ENA Register (Offset = 34h) [reset = 0h]

MMCSD0_NORMAL_INTR_STS_ENA is shown in Figure 14-7837 and described in Table 14-15886.

Return to Summary Table.

This register is used to enable the MMCSD0_NORMAL_INTR_STS register fields.

Table 14-23721. MMCSD0_NORMAL_INTR_STS_ENA Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0034h

Figure 14-7837. MMCSD0_NORMAL_INTR_STS_ENA Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23723. MMCSD0_NORMAL_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	Fixed to 0 The HC shall control error Interrupts using the MMCSD0_ERROR_INTR_STS_ENA register.
14	BOOT_COMPLETE	R/W	0h	Boot Terminate Interrupt Enable 0h: Masked 1h: Enabled
13	RCV_BOOT_ACK	R/W	0h	Boot Acknowledge Enable 0h: Masked 1h: Enabled
12	RETUNING_EVENT	R/W	0h	Re-Tuning Event Status Enable (UHS-I Only) 0h: Masked 1h: Enabled
11	INTC	R/W	0h	INT_C Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts.

Table 14-23723. MMCSD0_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INTB	R/W	0h	INT_B Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts.
9	INTA	R/W	0h	INT_A Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts.
8	CARD_INTERRUPT	R/W	0h	Card Interrupt Status Enable If this bit is set to 0h, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1h. The HD may clear the MMCSD0_ERROR_INTR_STS_ENA[8] CARD_INTERRUPT bit before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. By setting this bit to 0h, interrupt input should be masked by implementation so that the interrupt Input is not affected by external signal in any state (for example: floating). 0h: Masked 1h: Enabled
7	CARD_REMOVAL	R/W	0h	Card Removal Status Enable 0h: Masked 1h: Enabled
6	CARD_INSERTION	R/W	0h	Card Insertion Status Enable 0h: Masked 1h: Enabled
5	BUF_RD_READY	R/W	0h	Buffer Read Ready Status Enable 0h: Masked 1h: Enabled
4	BUF_WR_READY	R/W	0h	Buffer Write Ready Status Enable 0h: Masked 1h: Enabled
3	DMA_INTERRUPT	R/W	0h	DMA Interrupt Status Enable 0h: Masked 1h: Enabled

Table 14-23723. MMCSD0_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BLK_GAP_EVENT	R/W	0h	Block Gap Event Status Enable 0h: Masked 1h: Enabled
1	XFER_COMPLETE	R/W	0h	Transfer Complete Status Enable 0h: Masked 1h: Enabled
0	CMD_COMPLETE	R/W	0h	Command Complete Status Enable 0h: Masked 1h: Enabled

Note: The HC may sample the card Interrupt signal during interrupt period and may hold its value in the flip-flop. If the MMCSD0_ERROR_INTR_STS_ENA[8] CARD_INTERRUPT bit is set to 0h, the HC shall clear all internal signals regarding Card Interrupt (MMCSD0_NORMAL_INTR_STS[8] CARD_INTR).

22 MMCSD0_ERROR_INTR_STS_ENA Register (Offset = 36h) [reset = 0h]

MMCSD0_ERROR_INTR_STS_ENA is shown in Figure 14-7838 and described in Table 14-15888.

Return to Summary Table.

This register is used to enable the MMCSD0_ERROR_INTR_STS register fields.

Table 14-23724. MMCSD0_ERROR_INTR_STS_ENA Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0036h

Figure 14-7838. MMCSD0_ERROR_INTR_STS_ENA Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">VENDOR_SPECIFIC</td><td>RESP</td><td>TUNING</td><td>ADMA</td><td>AUTO_CMD</td></tr>
<tr><td colspan="4">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CURR_LIMIT</td><td>DATA_ENDBIT</td><td>DATA_CRC</td><td>DATA_TIMEOUT</td><td>CMD_INDEX</td><td>CMD_ENDBIT</td><td>CMD_CRC</td><td>CMD_TIMEOUT</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23726. MMCSD0_ERROR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Status Enable N/A
11	RESP	R/W	0h	Response Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
10	TUNING	R/W	0h	Tuning Error Status Enable (UHS-I Only) 0h: Masked 1h: Enabled
9	ADMA	R/W	0h	ADMA Error Status Enable 0h: Masked 1h: Enabled
8	AUTO_CMD	R/W	0h	Auto CMD Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
7	CURR_LIMIT	R/W	0h	Current Limit Error Status Enable 0h: Masked 1h: Enabled

Table 14-23726. MMCSD0_ERROR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DATA_ENDBIT	R/W	0h	Data End Bit Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
5	DATA_CRC	R/W	0h	Data CRC Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
4	DATA_TIMEOUT	R/W	0h	Data Timeout Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
3	CMD_INDEX	R/W	0h	Command Index Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
2	CMD_ENDBIT	R/W	0h	Command End Bit Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
1	CMD_CRC	R/W	0h	Command CRC Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
0	CMD_TIMEOUT	R/W	0h	Command Timeout Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled

Note: To Detect CMD Line conflict, the HD must set both MMCSD0_ERROR_INTR_STS_ENA[0] CMD_TIMEOUT and MMCSD0_ERROR_INTR_STS_ENA[1] CMD_CRC bits to 1h.

23 MMCSD0_NORMAL_INTR_SIG_ENA Register (Offset = 38h) [reset = 0h]

MMCSD0_NORMAL_INTR_SIG_ENA is shown in Figure 14-7839 and described in Table 14-15890.

Return to Summary Table.

Normal Interrupt Signal Enable Register

This register is used to select which interrupt status is indicated to the Host System as the Interrupt. These status bits all share the sample 1 bit interrupt line. Setting any of these bits to 1h enables Interrupt generation.

Table 14-23727. MMCSD0_NORMAL_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0038h

Figure 14-7839. MMCSD0_NORMAL_INTR_SIG_ENA Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23729. MMCSD0_NORMAL_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	Fixed to 0 The HD shall control error Interrupts using the MMCSD0_ERROR_INTR_SIG_ENA register.
14	BOOT_COMPLETE	R/W	0h	Boot Terminate Interrupt Signal Enable 0h: Masked 1h: Enabled
13	RCV_BOOT_ACK	R/W	0h	Boot Acknowledge Receive Signal Enable 0h: Masked 1h: Enabled
12	RETUNING_EVENT	R/W	0h	Re-Tuning Event Signal Enable (UHS-I Only) 0h: Masked 1h: Enabled
11	INTC	R/W	0h	INT_C Signal Enable (Embedded) 0h: Masked 1h: Enabled

Table 14-23729. MMCSD0_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INTB	R/W	0h	INT_B Signal Enable (Embedded) 0h: Masked 1h: Enabled
9	INTA	R/W	0h	INT_A Signal Enable (Embedded) 0h: Masked 1h: Enabled
8	CARD_INTERRUPT	R/W	0h	Card Interrupt Signal Enable 0h: Masked 1h: Enabled
7	CARD_REMOVAL	R/W	0h	Card Removal Signal Enable 0h: Masked 1h: Enabled
6	CARD_INSERTION	R/W	0h	Card Insertion Signal Enable 0h: Masked 1h: Enabled
5	BUF_RD_READY	R/W	0h	Buffer Read Ready Signal Enable 0h: Masked 1h: Enabled
4	BUF_WR_READY	R/W	0h	Buffer Write Ready Signal Enable 0h: Masked 1h: Enabled
3	DMA_INTERRUPT	R/W	0h	DMA Interrupt Signal Enable 0h: Masked 1h: Enabled
2	BLK_GAP_EVENT	R/W	0h	Block Gap Event Signal Enable 0h: Masked 1h: Enabled
1	XFER_COMPLETE	R/W	0h	Transfer Complete Signal Enable 0h: Masked 1h: Enabled
0	CMD_COMPLETE	R/W	0h	Command Complete Signal Enable 0h: Masked 1h: Enabled

24 MMCSD0_ERROR_INTR_SIG_ENA Register (Offset = 3Ah) [reset = 0h]

MMCSD0_ERROR_INTR_SIG_ENA is shown in Figure 14-7840 and described in Table 14-15892.

Return to Summary Table.

Error Interrupt Signal Enable Register

This register is used to select which interrupt status is notified to the Host System as the Interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1h enables Interrupt generation.

Table 14-23730. MMCSD0_ERROR_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 003Ah

Figure 14-7840. MMCSD0_ERROR_INTR_SIG_ENA Register

15	14	13	12	11	10	9	8
VENDOR_SPECIFIC				RESP	TUNING	ADMA	AUTO_CMD
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23732. MMCSD0_ERROR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Signal Enable N/A
11	RESP	R/W	0h	Response Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
10	TUNING	R/W	0h	Tuning Error Signal Enable (UHS-I Only) 0h: Masked 1h: Enabled
9	ADMA	R/W	0h	ADMA Error Signal Enable 0h: Masked 1h: Enabled
8	AUTO_CMD	R/W	0h	Auto CMD Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
7	CURR_LIMIT	R/W	0h	Current Limit Error Signal Enable 0h: Masked 1h: Enabled

Table 14-23732. MMCSD0_ERROR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DATA_ENDBIT	R/W	0h	Data End Bit Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
5	DATA_CRC	R/W	0h	Data CRC Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
4	DATA_TIMEOUT	R/W	0h	Data Timeout Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
3	CMD_INDEX	R/W	0h	Command Index Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
2	CMD_ENDBIT	R/W	0h	Command End Bit Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
1	CMD_CRC	R/W	0h	Command CRC Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
0	CMD_TIMEOUT	R/W	0h	Command Timeout Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled

25 MMCSD0_AUTOCMD_ERR_STS Register (Offset = 3Ch) [reset = 0h]

MMCSD0_AUTOCMD_ERR_STS is shown in Figure 14-7841 and described in Table 14-15894.

Return to Summary Table.

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD23.

The Host driver can determine what kind of Auto CMD12/CMD23 errors occur by this register. Auto CMD23 errors are indicated in bit 04-01. This register is valid only when the Auto CMD Error is set.

Table 14-23733. MMCSD0_AUTOCMD_ERR_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 003Ch

Figure 14-7841. MMCSD0_AUTOCMD_ERR_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_NOT_ISSUED	RESERVED		INDEX	ENDBIT	CRC	TIMEOUT	ACMD12_NOT_EXEC
R-0h	R-0h		R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23735. MMCSD0_AUTOCMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMD_NOT_ISSUED	R	0h	Command Not Issued By Auto CMD12 Error Setting this bit to 1h means CMD_wo_DAT is not executed due to an Auto CMD12 error (D04- D01) in this register. This bit is set to 0h when Auto CMD Error is generated by Auto CMD23. 0h: No Error 1h: Not Issued
6-5	RESERVED	R	0h	Reserved
4	INDEX	R	0h	Auto CMD Index Error Occurs if the Command Index error occurs in response to a command. 0h: No Error 1h: Error

Table 14-23735. MMCSD0_AUTOCMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ENDBIT	R	0h	Auto CMD End Bit Error Occurs when detecting that the end bit of command response is 0h. 0h: No Error 1h: End Bit Error Generated
2	CRC	R	0h	Auto CMD CRC Error Occurs when detecting a CRC error in the command response. 0h: No Error 1h: CRC Error Generated
1	TIMEOUT	R	0h	Auto CMD Timeout Error Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1h, the other error status bits (D04 - D02) are meaningless. 0h: No Error 1h: Timeout
0	ACMD12_NOT_EXEC	R	0h	Auto CMD12 not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1h means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1h, other error status bits (D04 - D01) are meaningless. This bit is set to 0h when Auto CMD Error is generated by Auto CMD23. 0h: Executed 1h: Not Executed

Table 14-15895 shows the relation between Auto CMD12 CRC error and Auto CMD12 timeout error.

Table 14-23736. Relation between Auto CMD12 CRC Error and Auto CMD12 Timeout Error

Auto Cmd12 CRC Error	Auto CMD12 Timeout Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD Line Conflict

The timing of changing Auto CMD12 Error Status can be classified in three scenarios:

1. When the HC is going to issue Auto CMD12:

Set D00 to 1h if Auto CMD12 cannot be issued due to an error in the previous command.

Set D00 to 0h if Auto CMD12 is issued.

2. At the end bit of Auto CMD12 response:

Check received responses by checking the error bits D01, D02, D03, D04.

set to 1h if Error is Detected.

set to 0h if Error is Not Detected.

3. Before reading the Auto CMD12 Error Status bit D07:

Set D07 to 1h if there is a command cannot be issued.

Set D07 to 0h if there is no command to issue.

Timing of generating the Auto CMD12 Error and writing to the MMCSD0_COMMAND register are Asynchronous. Then D07 shall be sampled when driver never writing to the MMCSD0_COMMAND register. So just before reading the MMCSD0_AUTOCMD_ERR_STS register is good timing to set the D07 status bit.

26 MMCSD0_HOST_CONTROL2 Register (Offset = 3Eh) [reset = 0h]

MMCSD0_HOST_CONTROL2 is shown in Figure 14-7842 and described in Table 14-15897.

Return to Summary Table.

This register is used to program UHS Mode Select, Driver Strength Select, Execute Tuning, Sampling Clock Select, Asynchronous Interrupt Enable and Preset Value Enable.

Table 14-23737. MMCSD0_HOST_CONTROL2 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 003Eh

Figure 14-7842. MMCSD0_HOST_CONTROL2 Register

15	14	13	12	11	10	9	8
PRESET_VALUE_ENA	ASYNCH_INTR_ENA	BIT64_ADDRESSING	HOST_VER40_ENA	CMD23_ENA	ADMA2_LEN_MODE	DRIVER_STRENGTH2	UHS2_INTF_ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
SAMPLING_CLK_SELECT	EXECUTE_TUNING	DRIVER_STRENGTH1		V1P8_SIGNAL_ENA	UHS_MODE_SELECT		
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23739. MMCSD0_HOST_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PRESET_VALUE_ENA	R/W	0h	Preset Value Enable Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to automatic. This bit enables the functions defined in the Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10). If this bit is set to 0h, SDCLK Frequency Select, Clock Generator Select in the MMCSD0_CLOCK_CONTROL register and Driver Strength Select in the MMCSD0_HOST_CONTROL2 register are set by Host Driver. If this bit is set to 1h, SDCLK Frequency Select, Clock Generator Select in the MMCSD0_CLOCK_CONTROL register and Driver Strength Select in the MMCSD0_HOST_CONTROL2 register are set by Host Controller as specified in the Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10). 0h: SDCLK and Driver Strength are controlled by Host Driver 1h: Automatic Selection by Preset Value are Enabled

Table 14-23739. MMCSD0_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ASYNCH_INTR_ENA	R/W	0h	Asynchronous Interrupt Enable This bit can be set to 1h if a card support asynchronous interrupt and the MMCSD0_CAPABILITIES[29] ASYNCH_INTR_SUPPORT bit is set to 1h. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode . If this bit is set to 1h, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 0h: Disabled 1h: Enabled
13	BIT64_ADDRESSING	R/W	0h	64-bit Addressing This field is effective when the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h. Host Controller selects either of 32-bit or 64-bit addressing modes to access system memory. Whether 32-bit or 64-bit is determined by OS installed in a host system. Host Driver sets this bit depends on addressing mode of installed OS. Refer to 64-bit System Address Support in the MMCSD0_CAPABILITIES register. 0h: 32-bits Addressing 1h: 64-bits Addressing

Table 14-23739. MMCSD0_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	HOST_VER40_ENA	R/W	0h	Host Version 4 Enable This bit selects either Version 3.00 compatible mode or Version 4.00 mode. In Version 4.00, support of 64-bit System Addressing is modified. All DMAs support 64-bit System Addressing. UHS-II supported Host Driver shall enable this bit. In Version 4.10, supported 32-bit Block Count for all operations. Functions of following fields are modified. **SDMA Address** SDMA uses the MMCSD0_ADMA_SYS_ADDRESS register instead of SDMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) **ADMA2/ADMA3 Selection** ADMA3 is selected by MMCSD0_HOST_CONTROL1[4-3] DMA_SELECT bit. **64-bit ADMA Descriptor Size** 128-bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1h. **Selection of 32-bit/64-bit System Addressing** Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register instead of MMCSD0_HOST_CONTROL1[4-3] DMA_SELECT bit. **32-bit Block Count** SDMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) is modified to 32-bit Block Count register. 0h: Version 3.00 Compatible Mode 1h: Version 4.Mode
11	CMD23_ENA	R/W	0h	CMD23 Enable In memory card initialization, Host Driver Version 4.10 checks whether card supports CMD23 by checking a bit SCR[33]. If the card supports CMD23 (SCR[33] = 1h), this bit is set to 1h. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 datatransfer. Refer to MMCSD0_TRANSFER_MODE[3-2] AUTO_CMD_ENA bit.
10	ADMA2_LEN_MODE	R/W	0h	ADMA2 Length Mode This bit selects one of ADMA2 Length Modes either 16-bit or 26-bit. 0h: 16-bit Data Length Mode 1h: 26-bit Data Length Mode
9	DRIVER_STRENGTH2	R/W	0h	Driver Strength Select This is the programmed Drive Strength output and Bit[2] of the sdhccore_drivestrength value.

Table 14-23739. MMCSD0_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	UHS2_INTF_ENABLE	R/W	0h	UHS-II Interface Enable This bit is used to enable UHS-II Interface. Before trying to start UHS-II initialization, this bit shall be set to 1h. Before trying to start SD mode initialization, this bit shall be set to 0h. This bit is used to enable UHS-II IF Detection, Lane Synchronization and In Dormant State in the MMCSD0_PRESENTSTATE register, and to select clock source of either SD mode or UHS-II mode. Host Controller shall not leave unused SD 4-bit Interface lines (CLK, CMD and DAT[3:2]) floating in UHS-II mode by using pull-up or driving to low. When DAT[2] is used as interrupt input in UHS-II mode, DAT[2] of Host Controller is set to input and then DAT[2] of SDIO card is set to output to avoid conflict. 0h: 4-bit SD Interface Enabled 1h: UHS-II Interface Enabled
7	SAMPLING_CLK_SELECT	R/W	0h	Sampling Clock Select (UHS-I Only) This bit is set by tuning procedure when the MMCSD0_HOST_CONTROL2[6] EXECUTE_TUNING bit is cleared. Writing 1h to this bit is meaningless and ignored. Setting 1h means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0h. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. 0h: Fixed clock is used to sample data 1h: Tuned clock is used to sample data
6	EXECUTE_TUNING	R/W	0h	Execute Tuning (UHS-I Only) This bit is set to 1h to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to the MMCSD0_HOST_CONTROL2[7] SAMPLING_CLK_SELECT bit. Tuning procedure is aborted by writing 0h for more detail about tuning procedure. 0h: Not Tuned or Tuning Completed 1h: Execute Tuning

Table 14-23739. MMCSD0_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	DRIVER_STRENGTH1	R/W	0h	Driver Strength Select (UHS-I Only) Host Controller output driver in 1.8 V signaling is selected by this bit. In 3.3 V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the MMCSD0_CAPABILITIES register. This bit depends on setting of the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this field is set by Host Driver. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this field is automatically set by a value specified in the one of Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10). 0h: Driver Type B is Selected (Default) 1h: Driver Type A is Selected 2h: Driver Type C is Selected 3h: Driver Type D is Selected
3	V1P8_SIGNAL_ENA	R/W	0h	1.8 V Signaling Enable (UHS-I Only) This bit controls voltage regulator for I/O cell. 3.3 V is supplied to the card regardless of signaling voltage. Setting this bit from 0h to 1h starts changing signal voltage from 3.3 V to 1.8 V. 1.8 V regulator output shall be stable within 5 ms. Host Controller clears this bit if switching to 1.8 V signaling fails. Clearing this bit from 1h to 0h starts changing signal voltage from 1.8 V to 3.3 V. 3.3 V regulator output shall be stable within 5 ms. Host Driver can set this bit to 1h when Host Controller supports 1.8 V signaling (one of support bits is set to 1h: SDR50, SDR104 or DDR50 in the MMCSD0_CAPABILITIES register) and the card or device supports UHS-I. 0h: 3.3 V Signaling 1h: 1.8 V Signaling

Table 14-23739. MMCSD0_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	UHS_MODE_SELECT	R/W	0h	UHS Mode Select (UHS-I Only) This field is used to select one of UHS-I modes or UHS-II mode. In case of UHS-I mode, this field is effective when the MMCSD0_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit is set to 1h. In case of UHS-II mode, the MMCSD0_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit shall be set to 0h. Setting of this field is used to select one of preset values in UHS-I or UHS-II mode. If the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA is set to 1h,Host Controller sets SDCLK/RCLK Frequency Select, Clock Generator Select in the MMCSD0_CLOCK_CONTROL register and Driver Strength Select according to Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10). In this case, one of preset value registers is selected by this field. Host Driver needs to reset the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit again. 0h: SDR12 1h: SDR25 2h: SDR50 3h: SDR104 4h: DDR50 5h: HS400 6h: Reserved 7h: UHS-II When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more details.

27 MMCSD0_CAPABILITIES Register (Offset = 40h) [reset = 980004073CECC801h]

MMCSD0_CAPABILITIES is shown in Figure 14-7843 and described in Table 14-15899.

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This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initialization.

Table 14-23740. MMCSD0_CAPABILITIES Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0040h

Figure 14-7843. MMCSD0_CAPABILITIES Register

63	62	61	60	59	58	57	56
HS400_SUPPORT	RESERVED		VDD2_1P8_SUPPORT	ADMA3_SUPPORT	RESERVED	SPI_BLK_MODE	SPI_SUPPORT
R-1h	R-0h		R-1h	R-1h	R-0h	R-0h	R-0h
55	54	53	52	51	50	49	48
CLOCK_MULTIPLIER							
R-0h							
47	46	45	44	43	42	41	40
RETUNING_MODES		TUNING_FOR_SDR50	RESERVED	RETUNING_TIMER_CNT			
R-0h		R-0h	R-0h	R-4h			
39	38	37	36	35	34	33	32
RESERVED	DRIVERD_SUPPORT	DRIVERC_SUPPORT	DRIVERA_SUPPORT	UHS2_SUPPORT	DDR50_SUPPORT	SDR104_SUPPORT	SDR50_SUPPORT
R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-1h
31	30	29	28	27	26	25	24
SLOT_TYPE		ASYNCH_INTR_SUPPORT	ADDR_64BIT_SUPPORT_V3	ADDR_64BIT_SUPPORT_V4	VOLT_1P8_SUPPORT	VOLT_3P0_SUPPORT	VOLT_3P3_SUPPORT
R-0h		R-1h	R-1h	R-1h	R-1h	R-0h	R-0h
23	22	21	20	19	18	17	16
SUSP_RES_SUPPORT	SDMA_SUPPORT	HIGH_SPEED_SUPPORT	RESERVED	ADMA2_SUPPORT	BUS_8BIT_SUPPORT	MAX_BLK_LENGTH	
R-1h	R-1h	R-1h	R-0h	R-1h	R-1h	R-0h	
15	14	13	12	11	10	9	8
BASE_CLK_FREQ							
R-C8h							
7	6	5	4	3	2	1	0
TIMEOUT_CLK_UNIT	RESERVED	TIMEOUT_CLK_FREQ					
R-0h	R-0h	R-1h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23742. MMCSD0_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
63	HS400_SUPPORT	R	1h	HS400 Support 0h: HS400 is Not Supported 1h: HS400 is Supported
62-61	RESERVED	R	0h	Reserved
60	VDD2_1P8_SUPPORT	R	1h	1.8 V VDD2 Support This bit indicates that support of VDD2 on Host system. 0h: 1.8 V VDD2 is not supported 1h: 1.8 V VDD2 is supported
59	ADMA3_SUPPORT	R	1h	ADMA3 Support This bit indicates that support of ADMA3 on Host Controller. 0h: ADMA3 is not supported 1h: ADMA3 is supported
58	RESERVED	R	0h	Reserved
57	SPI_BLK_MODE	R	0h	SPI Block Mode This bit indicates whether SPI Block Mode is supported or not. 0h: Not Supported 1h: Supported
56	SPI_SUPPORT	R	0h	SPI Mode This bit indicates whether SPI Mode is supported or not. 0h: Not Supported 1h: Supported
55-48	CLOCK_MULTIPLIER	R	0h	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to the MMCSD0_CLOCK_CONTROL register. Setting 00h means that Host Controller does not support programmable clock generator. FFh: Clock Multiplier M = 256 ---- 02h: Clock Multiplier M = 3 01h: Clock Multiplier M = 2 00h: Clock Multiplier is Not Supported

Table 14-23742. MMCSD0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
47-46	RETUNING_MODES	R	0h	Re-tuning Modes (UHS-I Only) This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver. 0h: Mode 1 1h: Mode 2 2h: Mode 3 3h: Reserved There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.
45	TUNING_FOR_SDR50	R	0h	Use Tuning for SDR50 (UHS-I Only) If this bit is set to 1h, this Host Controller requires tuning to operate SDR50 (tuning is always required to operate SDR104). 0h: SDR50 does not require tuning 1h: SDR50 requires tuning **Note:** Tuning is required for SDR50 to compensate temperature variation.
44	RESERVED	R	0h	Reserved
43-40	RETUNING_TIMER_CNT	R	4h	Timer Count for Re-Tuning (UHS-I Only) This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. 0h - Get information via other source 1h = 1 seconds 2h = 2 seconds 3h = 4 seconds 4h = 8 seconds ---- n = $2_{(n-1)}$ seconds ---- Bh = 1024 seconds Fh - Ch = Reserved
39	RESERVED	R	0h	Reserved
38	DRIVERD_SUPPORT	R	0h	Driver Type D Support (UHS-I Only) This bit indicates support of Driver Type D for 1.8 Signaling. 0h: Driver Type D is Not Supported 1h: Driver Type D is Supported

Table 14-23742. MMCSD0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
37	DRIVERC_SUPPORT	R	0h	Driver Type C Support (UHS-I Only) This bit indicates support of Driver Type C for 1.8 Signaling. 0h: Driver Type C is Not Supported 1h: Driver Type C is Supported
36	DRIVERA_SUPPORT	R	0h	Driver Type A Support (UHS-I Only) This bit indicates support of Driver Type A for 1.8 Signaling. 0h: Driver Type A is Not Supported 1h: Driver Type A is Supported
35	UHS2_SUPPORT	R	0h	UHS-II Support (UHS-II Only) This bit indicates whether Host Controller supports UHS-II. If this bit is set to 1h, the MMCSD0_CAPABILITIES[60] VDD2_1P8_SUPPORT bit shall be set to 1h (Host System shall support VDD2 power supply). 0h: UHS-II is Not Supported 1h: UHS-II is Supported
34	DDR50_SUPPORT	R	1h	DDR50 Support (UHS-I Only) This bit indicates whether DDR50 is supported or not. 0h: DDR50 is Not Supported 1h: DDR50 is Supported
33	SDR104_SUPPORT	R	1h	SDR104 Support (UHS-I Only) This bit indicates whether SDR104 is supported or not. SDR104 requires tuning. 0h: SDR104 is Not Supported 1h: SDR104 is Supported
32	SDR50_SUPPORT	R	1h	SDR50 Support (UHS-I Only) If SDR104 is supported, this bit shall be set to 1h. Bit 40 indicates whether SDR50 requires tuning or not. 0h: SDR50 is Not Supported 1h: SDR50 is Supported

Table 14-23742. MMCSD0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31-30	SLOT_TYPE	R	0h	Slot Type This field indicates usage of a slot by a specific Host System (a host controller register set is defined per slot). Embedded slot for one device (1h) means that only one non-removable device is connected to a SD bus slot. Shared Bus Slot (2h) can be set if Host Controller supports Shared Bus Control register. The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus (2h), the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System. 0h: Removable Card Slot 1h: Embedded Slot for One Device 2h: Shared Bus Slot (SD Mode) 3h: UHS-II Multiple Embedded Devices
29	ASYNCH_INTR_SUPPORT	R	1h	Asynchronous Interrupt Support (SD Mode Only) Refer to SDIO Specification Version 3.00 about asynchronous interrupt. 0h: Asynchronous Interrupt Not Supported 1h: Asynchronous Interrupt Supported
28	ADDR_64BIT_SUPPORT_V3	R	1h	64-bit System Address Support for V3 Meaning of this bit is different depends on Versions. Host Controller Version 3.00 and Version 4.10 use this bit as 64-bit System Address support for V3 mode. Host Controller Version 4.00 uses this bit as 64-bit System Address support for both V3 and V4 modes. SDMA cannot be used in 64-bit Addressing in Version 3 mode. If this bit is set to 1h, 64-bit ADMA2 with using 96-bit Descriptor may be enabled as follows: In case of Host Controller Version 3, 64-bit ADMA2 is enabled by MMCSD0_HOST_CONTROL1[4-3] DMA_SELECT = 3h. In case of Host Controller Version 4, 64-bit ADMA2 for Version 3 is enabled by setting MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h and MMCSD0_HOST_CONTROL1[4-3] DMA_SELECT = 3h. 0h: 64-bit System Address for V3 is not Supported 1h: 64-bit System Address for V3 is Supported

Table 14-23742. MMCSD0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	ADDR_64BIT_SUPPORT_V4	R	1h	64-bit System Address Support for V4 This bit is added from Version 4.10. Setting 1h to this bit indicates that the Host Controller supports 64-bit System Addressing of Version 4 mode . When this bit is set to 1h, full or a part of 64-bit address should be used to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to the MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit. If this bit is set to 1h, 64-bit DMA Addressing for Version 4 is enabled by setting MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h, MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING = 1h. SDMA can be used and ADMA2 uses 128-bit Descriptor. 0h: 64-bit System Address for V4 is not Supported 1h: 64-bit System Address for V4 is Supported
26	VOLT_1P8_SUPPORT	R	1h	Voltage Support 1.8 V This bit indicates whether the HC supports 1.8 V. 0h: 1.8 V Not Supported 1h: 1.8 V Supported
25	VOLT_3P0_SUPPORT	R	0h	Voltage Support 3.0 V This bit indicates whether the HC supports 3.0 V. 0h: 3.0 V Not Supported 1h: 3.0 V Supported
24	VOLT_3P3_SUPPORT	R	0h	Voltage Support 3.3 V This bit indicates whether the HC supports 3.3 V. 0h: 3.3 V Not Supported 1h: 3.3 V Supported
23	SUSP_RES_SUPPORT	R	1h	Suspend/Resume Support This bit indicates whether the HC supports Suspend/Resume functionality. If this bit is 0h, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend/ Resume commands. 0h: Not Supported 1h: Supported

Table 14-23742. MMCSD0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	SDMA_SUPPORT	R	1h	SDMA Support This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. Version 4.10 Host Controller shall support SDMA if ADMA2 is supported. 0h: SDMA Not Supported 1h: SDMA Supported
21	HIGH_SPEED_SUPPORT	R	1h	High Speed Support This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25 MHz to 50 MHz (for SD)/20 MHz to 52 MHz (for MMC). 0h: High Speed Not Supported 1h: High Speed Supported
20	RESERVED	R	0h	Reserved
19	ADMA2_SUPPORT	R	1h	ADMA2 Support 0h: ADMA2 Not support 1h: ADMA2 support
18	BUS_8BIT_SUPPORT	R	1h	8-bit Support for Embedded Device (Embedded) This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. This bit is not effective when the MMCSD0_CAPABILITIES[31-30] SLOT_TYPE bit field is set to 2h. 0h: 8-bit Bus Width Not Supported 1h: 8-bit Bus Width Supported
17-16	MAX_BLK_LENGTH	R	0h	Max Block Length This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. 0h: 512 byte 1h: 1024 byte 2h: 2048 byte 3h: 4096 byte

Table 14-23742. MMCSD0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	BASE_CLK_FREQ	R	C8h	Base Clock Frequency for SD Clock (1) 6-bit Base Clock Frequency: This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. 11xx xxxxb: Not Supported 0011 1111b: 63 MHz 0000 0010b: 2 MHz 0000 0001b: 1 MHz 0000 0000b: Get Information via another method (2) 8-bit Base Clock Frequency: This mode is supported by the Host Controller Version 3.00. Unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. FFh: 255 MHz 02h: 2 MHz 01h: 1 MHz 00h: Get Information via another method If the real frequency is 16.5 MHz, the lager value shall be set 0001 0001b (17 MHz) because the Host Driver use this value to calculate the clock divider value (refer to the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field) and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method.
7	TIMEOUT_CLK_UNIT	R	0h	Timeout Clock Unit This bit shows the unit of base clock frequency used to detect Data Timeout Error (MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT). 0h: KHz 1h: MHz
6	RESERVED	R	0h	Reserved
5-0	TIMEOUT_CLK_FREQ	R	1h	Timeout Clock Frequency This bit shows the base clock frequency used to detect Data Timeout Error (MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT). 0h: Get Information via another method Not 0h: 1 KHz to 63 KHz/1 MHz to 63 MHz

Table 14-15900 shows the 64-bit System Address Support depends on Versions.

Table 14-23743. 64-bit System Address Support depends on Versions

Host Controller	Version 3.00	Version 4.00	Version 4.10
D28 (from Version 2.00)	for V3	for V3 and V4	for V3

Table 14-23743. 64-bit System Address Support depends on Versions (continued)

Host Controller	Version 3.00	Version 4.00	Version 4.10
D27 (from Version 4.10)	D27 (from Version 4.10)	Not Defined	for V4
Register Decode	32-bit or 64-bit (up to implementation)	32-bit or 64-bit (up to implementation)	If D27 = 1h, 64-bit
SDMA	Not supported	Supported when MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h	Supported when MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h
ADMA2 (96-bit Descriptor)	DMA Select = 3h	Selected by MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h	Selected by MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h
ADMA2 (128-bit Descriptor)	Not Defined	Selected by MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h	Selected by MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h

As the specification of 64-bit System Address Support has been changed, capabilities of 64-bit functions are different depends on versions.

Definition of D28 is different depends on Versions. 96-bit Descriptor was defined by Version 2 but notation V3 is used including V2. Version 4.10 divides 64-bit System Address Support into V3 mode (D28) and V4 mode (D27) so that V3 mode can be optional. Migrate to V4 is recommended. From Host Controller Version 4.00, either V3 mode or V4 mode is selected by Host Version 4 Enable in the Host Control 2 register. V3 mode can be used if 64-bit System Address Support for V3 is set to 1h. V4 mode can be used if 64-bit System Address Support for V4 is set to 1h.

Prior to Version 4.10, address length of Host Controller registers decoding is not defined and whether 32-bit or 64-bit address is used to decode Host Controller registers is up to implementation. If Host Controller decodes 32-bit system address in default, the Host Controller Registers shall be placed in 32-bit addressing space.

When D27 = 1h, Host Controller Version 4.10 or later should use full or a part of 64-bit address to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to the MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit. How to decode register also should follow a system bus specification or a mother board specification.

From Version 4.00, 64-bit System Addressing of DMA is enabled by setting to the MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit. 64-bit SDMA is not supported in V3 mode and is supported in V4 mode. There are two Descriptor types for ADMA2 96-bit (V3) or 128-bit (V4). Support of 96-bit Descriptor is optional for Host Controller Version 4.10. If D28 = 0h, 96-bit Descriptor is not supported.

Note: The Host System shall support at least one of these voltages above. The HD sets the MMCSD0_POWER_CONTROL[3:1] SD_BUS_VOLTAGE bit field according to these support bits. If multiple voltages are supported, select the usable lower voltage by comparing the OCR value from the card.

These registers indicate maximum current capability for each voltage. The value is meaningful if Voltage Support is set in the MMCSD0_CAPABILITIES register.

Table 14-15901 describes the re-tuning modes.

Table 14-23744. 64-bit System Address Support depends on Versions

Bit47-46	Re-Tuning Mode	Data length	Timer Modes
0h	Mode1	4 MB (Max.)	Always enabled
1h	Mode2	4 MB (Max.)	Stop during data transfer
2h	Reserved	Reserved	Reserved
3h	Reserved	Reserved	Reserved

There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.

Data length per a read/write command is restricted by whether Host Controller generates Re-Tuning Request during data transfer so that re-tuning procedures can be inserted during data transfers.

28 MMCSD0_MAX_CURRENT_CAP Register (Offset = 48h) [reset = 0h]

MMCSD0_MAX_CURRENT_CAP is shown in Figure 14-7844 and described in Table 14-15903.

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This register indicates maximum current capability for each voltage.

Table 14-23745. MMCSD0_MAX_CURRENT_CAP Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0048h

Figure 14-7844. MMCSD0_MAX_CURRENT_CAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-0h															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED								VDD2_1P8V							
R-0h								R-0h							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								VDD1_1P8V							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDD1_3P0V								VDD1_3P3V							
R-0h								R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 14-23747. MMCSD0_MAX_CURRENT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39-32	VDD2_1P8V	R	0h	Maximum Current for 1.8 V VDD2
31-24	RESERVED	R	0h	Reserved
23-16	VDD1_1P8V	R	0h	Maximum Current for 1.8 V VDD1
15-8	VDD1_3P0V	R	0h	Maximum Current for 3.0 V VDD1
7-0	VDD1_3P3V	R	0h	Maximum Current for 3.3 V VDD1

Table 14-15904 describes the maximum current value.

Table 14-23748. Maximum Current Value Definition

Register Value	Current Value
0	Get Information via another method
1	4 mA
2	8 mA
3	12 mA
--------------------	--------------------

Table 14-23748. Maximum Current Value Definition (continued)

Register Value	Current Value
255	1020 mA

29 MMCSD0_FORCE_EVNT_ACMD_ERR_STS Register (Offset = 50h) [reset = 0h]

MMCSD0_FORCE_EVNT_ACMD_ERR_STS is shown in Figure 14-7845 and described in Table 14-15906.

Return to Summary Table.

This register is not physically implemented, rather it is an address where the MMCSD0_AUTOCMD_ERR_STS register can be written.

Writing 1h: set each bit of the MMCSD0_AUTOCMD_ERR_STS register

Writing 0h: no effect

By setting a bit in this register, the correspondent bit is set in the MMCSD0_ERROR_INTR_ST register. In order to generate interrupt signal, the correspondent bit shall be set in the MMCSD0_ERROR_INTR_STS_ENA register and MMCSD0_ERROR_INTR_SIG_ENA register.

Table 14-23749. MMCSD0_FORCE_EVNT_ACMD_ERR_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0050h

Figure 14-7845. MMCSD0_FORCE_EVNT_ACMD_ERR_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_NOT_ISS	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD_NOT_EXEC
W-0h	R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -*n* = value after reset

Table 14-23751. MMCSD0_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMD_NOT_ISS	W	0h	Force Event for Command Not Issued by AUTO CMD12 Error 0h: Not Affected 1h: Command Not Issued By Auto CMD12 Error Status is set
6	RESERVED	R	0h	Reserved
5	RESP	W	0h	Force Event for AUTO CMD Response Error 0h: Not Affected 1h: Auto CMD Response Error Status is set
4	INDEX	W	0h	Force Event for AUTO CMD Index Error 0h: Not Affected 1h: Auto CMD Index Error Status is set

Table 14-23751. MMCSD0_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ENDBIT	W	0h	Force Event for AUTO CMD End Bit Error 0h: Not Affected 1h: Auto CMD End bit Error Status is set
2	CRC	W	0h	Force Event for AUTO CMD Timeout Error 0h: Not Affected 1h: Auto CMD CRC Error Status is set
1	TIMEOUT	W	0h	Force Event for AUTO CMD Timeout Error 0h: Not Affected 1h: Auto CMD Timeout Error Status is set
0	ACMD_NOT_EXEC	W	0h	Force Event for AUTO CMD12 Not Executed 0h: Not Affected 1h: Auto CMD12 Not Executed Status is set

30 MMCSD0_FORCE_EVNT_ERR_INT_STS Register (Offset = 52h) [reset = 0h]

MMCSD0_FORCE_EVNT_ERR_INT_STS is shown in Figure 14-7846 and described in Table 14-15908.

Return to Summary Table.

This register is not physically implemented, rather it is an address where the MMCSD0_ERROR_INTR_STS register can be written.

The MMCSD0_FORCE_EVNT_ERR_INT_STS register is not a physically implemented register. Rather, it is an address at which the MMCSD0_ERROR_INTR_STS register can be written. The effect of a write to this address will be reflected in the MMCSD0_ERROR_INTR_STS register if the corresponding bit of the MMCSD0_ERROR_INTR_STS_ENA register is set.

Writing 1h: set each bit of the MMCSD0_ERROR_INTR_STS register

Writing 0h: no effect

Table 14-23752. MMCSD0_FORCE_EVNT_ERR_INT_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0052h

Figure 14-7846. MMCSD0_FORCE_EVNT_ERR_INT_STS Register

15	14	13	12	11	10	9	8
VEND_SPEC				RESP	TUNING	ADMA	AUTO_CMD
W-0h				W-0h	W-0h	W-0h	W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIM	DAT_ENDBIT	DAT_CRC	DAT_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; *-n* = value after reset

Table 14-23754. MMCSD0_FORCE_EVNT_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VEND_SPEC	W	0h	N/A
11	RESP	W	0h	Force Event for Response Error 0h: Not Affected 1h: Response Error Status is set
10	TUNING	W	0h	Force Event for Tuning Error 0h: Not Affected 1h: Tuning Error Status is set
9	ADMA	W	0h	Force Event for ADMA Error 0h: Not Affected 1h: ADMA Error Status is set
8	AUTO_CMD	W	0h	Force Event for Auto CMD Error 0h: Not Affected 1h: Auto CMD Error Status is set

Table 14-23754. MMCSD0_FORCE_EVNT_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CURR_LIM	W	0h	Force Event for Current Limit Error 0h: Not Affected 1h: Current Limit Error Status is set
6	DAT_ENDBIT	W	0h	Force Event for Data End Bit Error 0h: Not Affected 1h: Data End Bit Error Status is set
5	DAT_CRC	W	0h	Force Event for Data CRC Error 0h: Not Affected 1h: CRC Error Status is set
4	DAT_TIMEOUT	W	0h	Force Event for Data Timeout Error 0h: Not Affected 1h: Timeout Error Status is set
3	CMD_INDEX	W	0h	Force Event for Command Index Error 0h: Not Affected 1h: Command Index Error Status is set
2	CMD_ENDBIT	W	0h	Force Event for Command End Bit Error 0h: Not Affected 1h: Command End Bit Error Status is set
1	CMD_CRC	W	0h	Force Event for Command CRC Error 0h: Not Affected 1h: Command CRC Error Status is set
0	CMD_TIMEOUT	W	0h	Force Event for CMD Timeout Error 0h: Not Affected 1h: Command Timeout Error Status is set

31 MMCSD0_ADMA_ERR_STATUS Register (Offset = 54h) [reset = 0h]

MMCSD0_ADMA_ERR_STATUS is shown in Figure 14-7847 and described in Table 14-15910.

Return to Summary Table.

When the ADMA Error interrupt occur, this register holds the ADMA State (MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE) and the MMCSD0_ADMA_SYS_ADDRESS register holds address around the error descriptor.

Table 14-23755. MMCSD0_ADMA_ERR_STATUS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0054h

Figure 14-7847. MMCSD0_ADMA_ERR_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					ADMA_LENGTH_ERR	ADMA_ERR_STATE	
R-0h					R-0h	R-0h	

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23757. MMCSD0_ADMA_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	ADMA_LENGTH_ERR	R	0h	ADMA Length Mismatch Error This error occurs in the following 2 cases. While the MMCSD0_TRANSFER_MODE[1] BLK_CNT_ENA bit being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 0h: No Error 1h: Error
1-0	ADMA_ERR_STATE	R	0h	ADMA Error State This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "2h" because ADMA never stops in this state. D01 - D00: ADMA Error State when error occurred Contents of SYS_SDR register 0h: ST_STOP (Stop DMA) Points to next of the error descriptor 1h: ST_FDS (Fetch Descriptor) Points to the error descriptor 2h: Never set this state (Not used) 3h: ST_TFR (Transfer Data) Points to the next of the error descriptor

32 MMCSD0_ADMA_SYS_ADDRESS Register (Offset = 58h) [reset = Xh]

MMCSD0_ADMA_SYS_ADDRESS is shown in Figure 14-7848 and described in Table 14-15912.

Return to Summary Table.

This register contains the physical address used for ADMA data transfer.

Table 14-23758. MMCSD0_ADMA_SYS_ADDRESS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0058h

Figure 14-7848. MMCSD0_ADMA_SYS_ADDRESS Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADMA_ADDR																															
R/W-Xh																															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADMA_ADDR																															
R/W-Xh																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23760. MMCSD0_ADMA_SYS_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ADMA_ADDR	R/W	Xh	ADMA System Address The 32-bit addressing Host Driver uses lower 32-bit of this register (upper 32-bit should be set to 0h) and shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. DMA2/3 ignores lower 2-bit of this register and assumes it to be 0h. DMA in 64-bit addressing. The 64-bit addressing Host Driver uses all bits of this register and shall program Descriptor Table on 64-bit boundary and set 64-bit boundary address to this register. DMA2/3 ignores lower 3-bit of this register andassumes it to be 0h. **SDMA** If the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, SDMA use this register to indicate System Address of data location instead of using SDMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI). SDMA can be used in 32-bit and 64-bit addressing in Version 4.00. **ADMA2** This register holds byte address of executing command of the Descriptor table. At the start of ADMA2, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. **ADMA3** This register is set by ADMA3. Host Driver is not necessary to set this register. The ADMA3 increments address of this register, which points to next line, when every time fetching a Descriptor line. When Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. Register Value - **00000000_**xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address

33 MMCSD0_PRESET_VALUE0 Register (Offset = 60h) [reset = 100h]

MMCSD0_PRESET_VALUE0 is shown in Figure 14-7849 and described in Table 14-15915.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

When the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1h, SDCLK/RCLK Frequency Select and Clock Generator Select in the MMCSD0_CLOCK_CONTROL register, and Driver Strength Select in the MMCSD0_HOST_CONTROL2 register are automatically set based on the Selected Bus Speed Mode (see Table 14-15913). This means the Host Driver needs not set these fields when preset is enabled.

Before starting the initialization sequence, the Host Driver needs to set a clock preset value to SDCLK/RCLK Frequency Select in the MMCSD0_CLOCK_CONTROL register. The MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit can be set after initialization completed.

Table 14-15913 shows the conditions to select one of preset value registers.

Table 14-23761. Preset Value Register Select Condition

Selected Bus Speed Mode	1.8 V Signaling Enable (Host Control 2)	High Speed Enable (Host Control 1)	UHS-1 Mode Selection (Host Control 2)
Default Speed	0	0	don't care
High Speed	0	1	don't care
SDR12	1	don't care	0h
SDR25	1	don't care	1h
SDR50	1	don't care	2h
SDR104	1	don't care	3h
DDR50	1	don't care	4h
HS400	1	don't care	5h
Reserved	Not determined	don't care	6h
UHS-II	0	don't care	7h

Table 14-23762. MMCSD0_PRESET_VALUE0 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0060h

Figure 14-7849. MMCSD0_PRESET_VALUE0 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">DRIVER_STRENGTH_SEL</td><td colspan="3">RESERVED</td><td>CLOCK_GENSEL</td><td colspan="2">SDCLK_FRQSEL</td></tr>
<tr><td colspan="2">R-0h</td><td colspan="3">R-0h</td><td>R-0h</td><td colspan="2">R-100h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SDCLK_FRQSEL</td></tr>
<tr><td colspan="8">R-100h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-23764. MMCSD0_PRESET_VALUE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	100h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

34 MMCSD0_PRESET_VALUE1 Register (Offset = 62h) [reset = 4h]

MMCSD0_PRESET_VALUE1 is shown in Figure 14-7850 and described in Table 14-15917.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23765. MMCSD0_PRESET_VALUE1 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0062h

Figure 14-7850. MMCSD0_PRESET_VALUE1 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-4h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R-4h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23767. MMCSD0_PRESET_VALUE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	4h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

35 MMCSD0_PRESET_VALUE2 Register (Offset = 64h) [reset = 2h]

MMCSD0_PRESET_VALUE2 is shown in Figure 14-7851 and described in Table 14-15919.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23768. MMCSD0_PRESET_VALUE2 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0064h

Figure 14-7851. MMCSD0_PRESET_VALUE2 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-2h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23770. MMCSD0_PRESET_VALUE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

36 MMCSD0_PRESET_VALUE3 Register (Offset = 66h) [reset = 4h]

MMCSD0_PRESET_VALUE3 is shown in Figure 14-7852 and described in Table 14-15921.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23771. MMCSD0_PRESET_VALUE3 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0066h

Figure 14-7852. MMCSD0_PRESET_VALUE3 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-4h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-4h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23773. MMCSD0_PRESET_VALUE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	4h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

37 MMCSD0_PRESET_VALUE4 Register (Offset = 68h) [reset = 2h]

MMCSD0_PRESET_VALUE4 is shown in Figure 14-7853 and described in Table 14-15923.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23774. MMCSD0_PRESET_VALUE4 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0068h

Figure 14-7853. MMCSD0_PRESET_VALUE4 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23776. MMCSD0_PRESET_VALUE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

38 MMCSD0_PRESET_VALUE5 Register (Offset = 6Ah) [reset = 1h]

MMCSD0_PRESET_VALUE5 is shown in Figure 14-7854 and described in Table 14-15925.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23777. MMCSD0_PRESET_VALUE5 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 006Ah

Figure 14-7854. MMCSD0_PRESET_VALUE5 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-1h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R-1h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23779. MMCSD0_PRESET_VALUE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	1h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

39 MMCSD0_PRESET_VALUE6 Register (Offset = 6Ch) [reset = 0h]

MMCSD0_PRESET_VALUE6 is shown in Figure 14-7855 and described in Table 14-15927.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23780. MMCSD0_PRESET_VALUE6 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 006Ch

Figure 14-7855. MMCSD0_PRESET_VALUE6 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-0h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23782. MMCSD0_PRESET_VALUE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

40 MMCSD0_PRESET_VALUE7 Register (Offset = 6Eh) [reset = 2h]

MMCSD0_PRESET_VALUE7 is shown in Figure 14-7856 and described in Table 14-15929.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23783. MMCSD0_PRESET_VALUE7 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 006Eh

Figure 14-7856. MMCSD0_PRESET_VALUE7 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-2h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23785. MMCSD0_PRESET_VALUE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

41 MMCSD0_PRESET_VALUE8 Register (Offset = 72h) [reset = 1h]

MMCSD0_PRESET_VALUE8 is shown in Figure 14-7857 and described in Table 14-15931.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23786. MMCSD0_PRESET_VALUE8 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0072h

Figure 14-7857. MMCSD0_PRESET_VALUE8 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-1h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-1h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23788. MMCSD0_PRESET_VALUE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	1h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

42 MMCSD0_PRESET_VALUE10 Register (Offset = 74h) [reset = 0h]

MMCSD0_PRESET_VALUE10 is shown in Figure 14-7858 and described in Table 14-15933.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-23789. MMCSD0_PRESET_VALUE10 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0074h

Figure 14-7858. MMCSD0_PRESET_VALUE10 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23791. MMCSD0_PRESET_VALUE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

43 MMCSD0_ADMA3_DESC_ADDRESS Register (Offset = 78h) [reset = Xh]

MMCSD0_ADMA3_DESC_ADDRESS is shown in Figure 14-7859 and described in Table 14-15935.

Return to Summary Table.

The start address of Integrated DMA Descriptor is set to this register.

Table 14-23792. MMCSD0_ADMA3_DESC_ADDRESS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0078h

Figure 14-7859. MMCSD0_ADMA3_DESC_ADDRESS Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
INTG_DESC_ADDR																															
R/W-Xh																															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTG_DESC_ADDR																															
R/W-Xh																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23794. MMCSD0_ADMA3_DESC_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	INTG_DESC_ADDR	R/W	Xh	ADMA3 Integrated Descriptor Address The start address of Integrated DMA Descriptor is set to this register. Writing to a specific address starts ADMA3 depends on 32-bit/64-bit address-ing. The ADMA3 fetches one Descriptor Address and increments this field to indicate the next Descriptor address. The 32-bit addressing Host Driver uses lower 32-bit of this register and shall program Descriptor Table on 32-bit boundary. ADMA3 ignores lower 2-bit of this register and assumes it to be 0h. Writing to 07Bh starts ADMA3 data transfer. The 64-bit addressing Host Driver uses all 64-bit of this register and shall program Descriptor Table on 64-bit boundary. ADMA3 ignores lower 3-bit of this register and assumes it to be 0h. Writing to 07Fh starts ADMA3 data transfer. Register Value - **00000000**_xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address

44 MMCSD0_UHS2_BLOCK_SIZE Register (Offset = 80h) [reset = 0h]

MMCSD0_UHS2_BLOCK_SIZE is shown in Figure 14-7860 and described in Table 14-15937.

Return to Summary Table.

This register is used to configure the number of bytes in a data block.

Table 14-23795. MMCSD0_UHS2_BLOCK_SIZE Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0080h

Figure 14-7860. MMCSD0_UHS2_BLOCK_SIZE Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">SDMA_BUF_BOUNDARY</td><td colspan="4">XFER_BLK_SIZE</td></tr>
<tr><td>R-0h</td><td colspan="3">R/W-0h</td><td colspan="4">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">XFER_BLK_SIZE</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23797. MMCSD0_UHS2_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved

Table 14-23797. MMCSD0_UHS2_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	SDMA_BUF_BOUNDARY	R/W	0h	UHS-II SDMA Buffer Boundary (SDMA only) When system memory is managed by paging, SDMA data transfer is performed in unit of paging. A page size of system memory management is set to this field. Host Controller generates the DMA Interrupt at the page boundary and requests the Host Driver to update the MMCSD0_ADMA_SYS_ADDRESS register. SDMA waits until the MMCSD0_ADMA_SYS_ADDRESS register is written. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued (see MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE). These bits shall be supported when the MMCSD0_CAPABILITIES[22] SDMA_SUPPORT bit is set to 1h and this function is active when the MMCSD0_UHS2_XFER_MODE[0] DMA_ENA bit register is set to 1h. ADMA does not use this field. 0h: 4K bytes (Detects A11 carry out) 1h: 8K bytes (Detects A12 carry out) 2h: 16K Bytes (Detects A13 carry out) 3h: 32K Bytes (Detects A14 carry out) 4h: 64K bytes (Detects A15 carry out) 5h: 128K Bytes (Detects A16 carry out) 6h: 256K Bytes (Detects A17 carry out) 7h: 512K Bytes (Detects A18 carry out)
11-0	XFER_BLK_SIZE	R/W	0h	UHS-II Block Size This bit field specifies the block size of data packet. SD Memory Card uses a fixed block size of 512 bytes. Variable block size may be used for SDIO. The maximum value is 2048 Bytes because CRC16 covers up to 2048 bytes. This bit field is effective when the MMCSD0_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. 0000h - No data transfer 0001h - 1 Byte 0002h - 2 Bytes 0003h - 3 Bytes ... ... 01FFh - 511 Bytes 0200h - 512 Bytes ... ... 0800h - 2048 Bytes

45 MMCSD0_UHS2_BLOCK_COUNT Register (Offset = 84h) [reset = 0h]

MMCSD0_UHS2_BLOCK_COUNT is shown in Figure 14-7861 and described in Table 14-15939.

Return to Summary Table.

This register is used to configure the number of data blocks.

Table 14-23798. MMCSD0_UHS2_BLOCK_COUNT Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0084h

Figure 14-7861. MMCSD0_UHS2_BLOCK_COUNT Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">XFER_BLK_COUNT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23800. MMCSD0_UHS2_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XFER_BLK_COUNT	R/W	0h	UHS-II Block Count This register is effective when the MMCSD0_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h and is enabled when the MMCSD0_UHS2_XFER_MODE[1] BLK_CNT_ENA bit is set to 1h and the MMCSD0_UHS2_XFER_MODE[5] BYTE_MODE bit is set to 0h. Data transfer stops when the count reaches zero. Setting the block count to 0h results in no data blocks is transferred. This register should be accessed only when no transaction is executing (after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. 00000000h: Stop Count 00000001h: 1 block 00000002h: 2 blocks ... ... FFFFFFFFh: 4G blocks - 1

46 MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 Register (Offset = 88h to 9Bh) [reset = 0h]

MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 is shown in Figure 14-7862 and described in Table 14-15942.

Return to Summary Table.

UHS-II Command Packet image is set to this register. The maximum length is 20 bytes (see Table 14-15940). The command length varies depends on a Command Packet type. The length is specified by the MMCSD0_UHS2_COMMAND register.

Table 14-23801. UHS-II Command Packet Register

Offset	Preset Value Registers
088h	Command Packet Byte 0
089h	Command Packet Byte 1
08Ah	Command Packet Byte 2
....	....
09Bh	Command Packet Byte 19

Table 14-23802. MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0088h to 0FA1 009Bh

Figure 14-7862. MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 Register

7	6	5	4	3	2	1	0
CMD_PKT_BYTE							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-23804. MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CMD_PKT_BYTE	R/W	0h	Command Packet Byte UHS-II Command Packet image is set to this register. The command length varies depends on a Command Packet type.

47 MMCSD0_UHS2_XFER_MODE Register (Offset = 9Ch) [reset = 0h]

MMCSD0_UHS2_XFER_MODE is shown in Figure 14-7863 and described in Table 14-15944.

Return to Summary Table.

This register is used to control the operations of data transfers.

On issuing a Command Packet, a Command Packet image is set to UHS-II Command Packet register (see MMCSD0_UHS2_COMMAND_PKT_0 - MMCSD0_UHS2_COMMAND_PKT_19) but Host Controller does not analyze the setting of UHS-II Command Packet register. Instead, Host Controller refers setting of this register to issue a Command Packet to make the control easy. Setting of these registers shall be correspondent.

Table 14-23805. MMCSD0_UHS2_XFER_MODE Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 009Ch

Figure 14-7863. MMCSD0_UHS2_XFER_MODE Register

15	14	13	12	11	10	9	8
DUPLEX_SELECT	EBSY_WAIT	RESERVED					RESP_INTR_DIS
R/W-0h	R/W-0h	R-0h					R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESP_ERR_CHK_ENA	RESP_TYPE	BYTE_MODE	DATA_XFER_DIR	RESERVED		BLK_CNT_ENA	DMA_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-23807. MMCSD0_UHS2_XFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DUPLEX_SELECT	R/W	0h	Half/Full Select Use of 2 lane half duplex mode is determined by Host Driver. 0h: Full Duplex Mode 1h: 2 Lane Half Duplex Mode

Table 14-23807. MMCSD0_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EBSY_WAIT	R/W	0h	EBSY Wait This bit is set when issuing a command which is accompanied by EBSY packet to indicate end of command execution. Busy is expected for CCMD with R1b/R5b type and DCMD with data transfer. If this bit is set to 1h, Host Controller waits receiving of EBSY packet and on receiving EBSY packet, the MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is set to 1h to indicate end of busy. If an error is indicated in EBSY packet (for example: Memory Error), the MMCSD0_UHS2_ERR_INTR_STS[8] EBSY bit is set to 1h. Setting of the MMCSD0_UHS2_ERR_INTR_STS[8] EBSY bit also sets the MMCSD0_NORMAL_INTR_STS[15] ERROR_INTR bit to 1h. The MMCSD0_NORMAL_INTR_STS[15] ERROR_INTR and MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bits shall be set together. 0h: Issue a command without busy 1h: Wait EBSY
13-9	RESERVED	R	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Response Interrupt Disable Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0h and waits the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit and then check the response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7). If Host Controller checks response error, sets this bit to 1h and sets the MMCSD0_UHS2_XFER_MODE[7] RESP_ERR_CHK_ENA bit to 1h. The MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit is disabled by this bit regardless of MMCSD0_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit. 0h: Response Interrupt is enabled 1h: Response Interrupt is disabled

Table 14-23807. MMCSD0_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESP_ERR_CHK_ENA	R/W	0h	Response Error Check Enable Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, this bit is set to 0h and the MMCSD0_UHS2_XFER_MODE[8] RESP_INTR_DIS bit is set to 0h. If Host Controller checks response error, sets this bit to 1h and sets the MMCSD0_UHS2_XFER_MODE[8] RESP_INTR_DIS bit to 1h. Response Type R1/R5 selects either R1 or R5 response type. If an error is detected, RES Packet Error Interrupt is generated in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Response Error Check is disabled 1h: Response Error Check is enabled
6	RESP_TYPE	R/W	0h	Response Type R1/R5 When response error check is enabled, this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1: Bit31 OUT_OF_RANGE Bit30 ADDRESS_ERROR Bit29 BLOCK_LEN_ERROR Bit26 WP_VIOLATION Bit25 CARD_IS_LOCKED Bit23 COM_CRC_ERROR Bit21 CARD_ECC_FAILED Bit20 CC_ERROR Bit19 ERROR Response Flags Checked in R5: Bit07 COM_CRC_ERROR Bit03 ERROR Bit01 FUNCTION_NUMBER Bit00 OUT_OF_RANGE 0h: R1 (Memory) 1h: R5 (SDIO)

Table 14-23807. MMCSD0_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	BYTE_MODE	R/W	0h	Block/Byte Mode This bit specifies whether data transfer is in byte mode or block mode when the MMCSD0_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. This bit is effective to a command with data transfer. 0h: Block Mode 1h: Byte Mode
4	DATA_XFER_DIR	R/W	0h	Data Transfer Direction This bit specifies direction of data transfer when the MMCSD0_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. This bit is effective to a command with data transfer. 0h: Read (Card to Host) 1h: Write (Host to Card)
3-2	RESERVED	R	0h	Reserved
1	BLK_CNT_ENA	R/W	0h	Block Count Enable This bit specifies whether data transfer uses the MMCSD0_UHS2_BLOCK_COUNT register. If this bit is set to 1h, data transfer is terminated by Block Count. Setting to the MMCSD0_UHS2_BLOCK_COUNT register shall be equivalent to TLEN in UHS-II Command Packet register (MMCSD0_UHS2_COMMAND_PKT_0 - MMCSD0_UHS2_COMMAND_PKT_19). 0h: Block Count Disabled 1h: Block Count Enabled
0	DMA_ENA	R/W	0h	DMA Enable This bit selects whether DMA is used or not and is effective to a command with data transfer. One of DMA types is selected by the MMCSD0_HOST_CONTROL1[4-3] DMA_SELECT bit field. 0h: DMA is disabled 1h: DMA is enabled

48 MMCSD0_UHS2_COMMAND Register (Offset = 9Eh) [reset = 0h]

MMCSD0_UHS2_COMMAND is shown in Figure 14-7864 and described in Table 14-15946.

Return to Summary Table.

This register is used to program the Command for host controller.

Table 14-23808. MMCSD0_UHS2_COMMAND Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 009Eh

Figure 14-7864. MMCSD0_UHS2_COMMAND Register

15	14	13	12	11	10	9	8
RESERVED			PKT_LENGTH				
R-0h			R/W-0h				

7	6	5	4	3	2	1	0
CMD_TYPE		DATA_PRESENT	RESERVED		SUB_COMMAND	RESERVED	
R/W-0h		R/W-0h	R-0h		R/W-0h	R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-23810. MMCSD0_UHS2_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	PKT_LENGTH	R/W	0h	UHS-II Command Packet Length A command packet length, which is set in the UHS-II Command Packet register (MMCSD0_UHS2_COMMAND_PKT_0 - MMCSD0_UHS2_COMMAND_PKT_19), is set to this bit field. 00011b – 00000b: 3-0 Bytes (Not used) 00100b: 4 Bytes .... 10100b: 20 Bytes 11111b – 10101b

Table 14-23810. MMCSD0_UHS2_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	CMD_TYPE	R/W	0h	Command Type This field is used to distinguish a specific command like abort command. If this field is set to 0h, the UHS-II RES Packet is stored in UHS-II Response register (MMCSD0_UHS2_RESPONSE_0 - MMCSD0_UHS2_RESPONSE_19). To avoid overwriting the UHS-II Response register, when this field is set to 1h, the RES Packet (4 bytes length) of TRANS_ABORT CCMD is stored in the Response register (04F8 0010h - 04F8 0013h) and when this field is set to 2h, the RES Packet (8 bytes length) of memory or SDIO abort command (CMD12 or SDIO Abort command) is stored in the Response register (04F8 0018h - 04F8 001Fh). When this field is set to 3h, Host Controller controls lane to go into dormant state. 0h: Normal Command 1h: TRANS_ABORT CCMD 3h: CMD12 or SDIO Abort command 4h: Go Dormant Command
5	DATA_PRESENT	R/W	0h	Data Present This bit specifies whether the command is accompanied by data packet. 0h: No Data Present 1h: Data Present
4-3	RESERVED	R	0h	Reserved
2	SUB_COMMAND	R/W	0h	Sub Command Flag This bit is added from Version 4.10 to distinguish a main command or sub command . When issuing a main command, this bit is set to 0h and when issuing a sub command, this bit is set to 1h. Setting of this bit is checked by the MMCSD0_PRESENTSTATE[28] SUB_COMMAND_STS bit. 0h: Sub Command 1h: Main Command
1-0	RESERVED	R	0h	Reserved

49 MMCSD0_UHS2_RESPONSE_0 to MMCSD0_UHS2_RESPONSE_19 Register (Offset = A0h to B3h) [reset = 0h]

MMCSD0_UHS2_RESPONSE_0 to MMCSD0_UHS2_RESPONSE_19 is shown in Figure 14-7865 and described in Table 14-15948.

Return to Summary Table.

This register is used to store received UHS-II RES Packet image.

Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command, which is specified by setting 1h or 2h to the MMCSD0_UHS2_COMMAND[7-6] CMD_TYPE bit field. The maximum response length is 20 bytes.

Table 14-23811. MMCSD0_UHS2_RESPONSE_0 to UHS2_RESPONSE_19 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00A0h to 0FA1 00B3h

Figure 14-7865. MMCSD0_UHS2_RESPONSE_0 to MMCSD0_UHS2_RESPONSE_19 Register

7	6	5	4	3	2	1	0
RESP_PKT_BYTE							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23813. MMCSD0_UHS2_RESPONSE_0 to UHS2_RESPONSE_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESP_PKT_BYTE	R	0h	Response Packet Byte Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command.

Table 14-15949 shows UHS-II Response Register offsets.

Table 14-23814. UHS-II Response Register

Offset	Preset Value Registers
0FA1 0A0h	Response Packet Byte 0
0FA1 0A1h	Response Packet Byte 1
0FA1 0A2h	Response Packet Byte 2
....	....
0FA1 0B3h	Response Packet Byte 19

50 MMCSD0_UHS2_MESSAGE_SELECT Register (Offset = B4h) [reset = 0h]

MMCSD0_UHS2_MESSAGE_SELECT is shown in Figure 14-7866 and described in Table 14-15951.

Return to Summary Table.

This register is used to access internal buffer.

Table 14-23815. MMCSD0_UHS2_MESSAGE_SELECT Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00B4h

Figure 14-7866. MMCSD0_UHS2_MESSAGE_SELECT Register

7	6	5	4	3	2	1	0
RESERVED						MSG_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23817. MMCSD0_UHS2_MESSAGE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	MSG_SEL	R/W	0h	UHS-II MSG Select Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs can be read from the MMCSD0_UHS2_MESSAGE register (04F8 00BBh - 04F8 00B8h) by setting this register (assumed for debug usage). 0h: The latest MSG 1h: One MSG before 2h: Two MSGs before 3h: Three MSGs before

51 MMCSD0_UHS2_MESSAGE Register (Offset = B8h) [reset = 0h]

MMCSD0_UHS2_MESSAGE is shown in Figure 14-7867 and described in Table 14-15953.

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This register is used to access internal buffer.

Table 14-23818. MMCSD0_UHS2_MESSAGE Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00B8h

Figure 14-7867. MMCSD0_UHS2_MESSAGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSG_BYTE3								MSG_BYTE2							
R-0h								R-0h							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSG_BYTE1								MSG_BYTE0							
R-0h								R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23820. MMCSD0_UHS2_MESSAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MSG_BYTE3	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSD0_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSD0_UHS2_MESSAGE Register.
23-16	MSG_BYTE2	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSD0_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSD0_UHS2_MESSAGE Register.
15-8	MSG_BYTE1	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSD0_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSD0_UHS2_MESSAGE Register.

Table 14-23820. MMCSD0_UHS2_MESSAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	MSG_BYTE0	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSD0_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSD0_UHS2_MESSAGE Register.

52 MMCSD0_UHS2_DEVICE_INTR_STATUS Register (Offset = BCh) [reset = 0h]

MMCSD0_UHS2_DEVICE_INTR_STATUS is shown in Figure 14-7868 and described in Table 14-15955.

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This register shows receipt of INT MSG from which device.

Table 14-23821. MMCSD0_UHS2_DEVICE_INTR_STATUS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00BCh

Figure 14-7868. MMCSD0_UHS2_DEVICE_INTR_STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_INT_STS															
R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-23823. MMCSD0_UHS2_DEVICE_INTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEV_INT_STS	R/W1C	0h	UHS-II Device Interrupt Status This register shows receipt of INT MSG from which device and is effective when the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. On receiving INT MSG from a device, Host Controller saves the INT MSG to MMCSD0_UHS2_DEVICE_INT_CODE register. A bit of this register, which is correspondent to Device ID, is set to 1h and generate Card Interrupt in Normal Interrupt Status register (see MMCSD0_NORMAL_INTR_STS[8] CARD_INTR). Writing a bit to 1h clears the status bit (interrupt is treated) and writing a bit to 0h keeps the status value (interrupt is untreated). If the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 0h, this register is cleared to 0h and Host Controller ignores receipt of INT MSG. Effective bit range of this register is determined by the MMCSD0_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. If N devices are supported, bits 1 to N are effective. Then Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. A bit of unsupported Device ID in this register shall be indicated to 0h. D00 - Not used (Reserved) D01 - Setting 1h means INT MSG is received from Device ID 1 D02 - Setting 1h means INT MSG is received from Device ID 2 .... D15 - Setting 1h means INT MSG is received from Device ID 15

53 MMCSD0_UHS2_DEVICE_SELECT Register (Offset = BEh) [reset = 0h]

MMCSD0_UHS2_DEVICE_SELECT is shown in Figure 14-7869 and described in Table 14-15957.

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UHS-II Device Select Register.

Table 14-23824. MMCSD0_UHS2_DEVICE_SELECT Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00BEh

Figure 14-7869. MMCSD0_UHS2_DEVICE_SELECT Register

7	6	5	4	3	2	1	0
INT_MSG_ENA	RESERVED			DEV_SEL			
R/W-0h	R-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23826. MMCSD0_UHS2_DEVICE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MSG_ENA	R/W	0h	INT MSG Enable (Optional) This bit enables receipt of INT MSG. If this bit is set to 1h, receipt of INT MSG is informed by the MMCSD0_NORMAL_INTR_STS[8] CARD_INTR bit. If this bit is set to 0h, Host Controller ignores receipt of INT MSG and may not set the MMCSD0_UHS2_DEVICE_INT_CODE register. Support of INT MSG Interrupt is optional. If trying to set this bit to 1h but still this bit is read 0, INT MSG Interrupt is not supported by the Host Controller. In this case, the MMCSD0_UHS2_DEVICE_INTR_STATUS register always shall be read 0 and the MMCSD0_UHS2_DEVICE_INT_CODE register may not be implemented. 0h: Disabled 1h: Enabled
6-4	RESERVED	R	0h	Reserved

Table 14-23826. MMCSD0_UHS2_DEVICE_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DEV_SEL	R/W	0h	UHS-II Device Select Host Controller holds an INT MSG packet per device. One of INT MSGs (up to 15) can be selected by this field and read from the MMCSD0_UHS2_DEVICE_INT_CODE. This field is effective when the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. The number of devices implemented in the Host Controller is indicated by the MMCSD0_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. 0h: Unselected (Default) 1h: INT MSG of Device ID 1 is selected 2h: INT MSG of Device ID 2 is selected .... Fh: INT MSG of Device ID 15 is selected

54 MMCSD0_UHS2_DEVICE_INT_CODE Register (Offset = BFh) [reset = 0h]

MMCSD0_UHS2_DEVICE_INT_CODE is shown in Figure 14-7870 and described in Table 14-15959.

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This register is effective when the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h.

Table 14-23827. MMCSD0_UHS2_DEVICE_INT_CODE Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00BFh

Figure 14-7870. MMCSD0_UHS2_DEVICE_INT_CODE Register

7	6	5	4	3	2	1	0
DEV_INTR							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23829. MMCSD0_UHS2_DEVICE_INT_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEV_INTR	R	0h	UHS II Device Interrupt This register is effective when the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. Host Controller holds an INT MSG packet per device. One of INT MSGs (Code length is 1 byte) up to 15 can be read from this register by selecting UHS-II Device Select (MMCSD0_UHS2_DEVICE_SELECT[3-0] DEV_SEL). The number of the registers to hold INT MSGs is determined by the MMCSD0_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization.

55 MMCSD0_UHS2_SOFTWARE_RESET Register (Offset = C0h) [reset = 0h]

MMCSD0_UHS2_SOFTWARE_RESET is shown in Figure 14-7871 and described in Table 14-15961.

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UHS-II Software Reset Register.

Table 14-23830. MMCSD0_UHS2_SOFTWARE_RESET Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00C0h

Figure 14-7871. MMCSD0_UHS2_SOFTWARE_RESET Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						HOST_SDTRAN_RESET	HOST_FULL_RESET
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23832. MMCSD0_UHS2_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	HOST_SDTRAN_RESET	R/W	0h	Host SD-TRAN Reset Host Driver set this bit to 1h to reset SD-TRAN layer when CMD0 is issued to Device or data transfer error occurs. This bit is cleared automatically at completion of SD-TRAN reset. If CMD0 is issued, SD-TRAN Initialization sequence from CMD8 is required to use UHS-II mode. Assuming that bus power is maintained and CM-TRAN Initialization is not required. Host Controller requires to do followings: (1) SD Clock Enable is maintained (continue to provide RCLK). (2) All setting register is maintained. (3) Internal sequencers are reset to just after power on be able to issue a command. (4) All Interrupt Status, Status Enable and Signal Enable are cleared. (5) Data transfer is terminated and data in buffer is discarded. 0h: Not Affected 1h: Reset SD-TRAN

Table 14-23832. MMCSD0_UHS2_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HOST_FULL_RESET	R/W	0h	Host Full Reset On issuing FULL_RESET CCMD, Host Driver set this bit to 1h to reset Host Controller. This bit is cleared automatically at completion of Host Controller reset. Initialization sequence from PHY Initialization is required to use UHS-II mode. Assuming that bus power is maintained. Host Controller requires to do followings: (1) SD Clock Enable is cleared (internal Clock is still synchronized). (2) All setting register is cleared. (3) Internal sequencers are reset to just after power on. (4) All Interrupt Status, Status Enable and Signal Enable are cleared. 0h: Not Affected 1h: Reset Host Controller

56 MMCSD0_UHS2_TIMER_CONTROL Register (Offset = C2h) [reset = 0h]

MMCSD0_UHS2_TIMER_CONTROL is shown in Figure 14-7872 and described in Table 14-15963.

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UHS-II Timeout Control Register.

Table 14-23833. MMCSD0_UHS2_TIMER_CONTROL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00C2h

Figure 14-7872. MMCSD0_UHS2_TIMER_CONTROL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEADLOCK_TIMEOUT_CTR				CMDRESP_TIMEOUT_CTR			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23835. MMCSD0_UHS2_TIMER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-4	DEADLOCK_TIMEOUT_CTR	R/W	0h	Timeout Counter Value for Deadlock This value determines the deadlock period while host expecting to receive a packet (1 second). Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for Deadlock (in the MMCSD0_UHS2_ERR_INTR_STS_ENA register). Fh: Reserved Eh: TMCLK x 2^{27} .... 1h: TMCLK x 2^{14} 0h: TMCLK x 2^{13}

Table 14-23835. MMCSD0_UHS2_TIMER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CMDRESP_TIMEOUT_CTR	R/W	0h	Timeout Counter Value for CMD_RES This value determines the interval between command packet and response packet (5 ms). Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for CMD_RES (in the MMCSD0_UHS2_ERR_INTR_STS_ENA register). Fh: Reserved Eh: TMCLK x 2^{27} .... 1h: TMCLK x 2^{14} 0h: TMCLK x 2^{13}

57 MMCSD0_UHS2_ERR_INTR_STS Register (Offset = C4h) [reset = 0h]

MMCSD0_UHS2_ERR_INTR_STS is shown in Figure 14-7873 and described in Table 14-15965.

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This register gives the status of all UHS-II interrupts.

Table 14-23836. MMCSD0_UHS2_ERR_INTR_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00C4h

Figure 14-7873. MMCSD0_UHS2_ERR_INTR_STS Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC_ERR					RESERVED		
R/W1C-0h					R-0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W1C-0h	R-0h						R/W1C-0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-23838. MMCSD0_UHS2_ERR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECFIC_ERR	R/W1C	0h	Vendor Specific Error Vendor may use this field for vendor specific error status. 0h: Interrupt is not generated 1h: Vendor Specific Error
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W1C	0h	Timeout for Deadlock Setting of this bit means that deadlock timeout occurs. Host expects to receive a packet but not received in a specified timeout (1 second). Timeout value is determined by the setting of the MMCSD0_UHS2_TIMER_CONTROL[7-4] DEADLOCK_TIMEOUT_CTR bit field. 0h: Interrupt is not generated 1h: Deadlock Error

Table 14-23838. MMCSD0_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W1C	0h	Timeout for CMD_RES Setting of this bit means that RES Packet timeout occurs. Host expects to receive RES packet but not received in a specified timeout (5 ms). Timeout value is determined by the setting of the MMCSD0_UHS2_TIMER_CONTROL[3-0] CMDRESP_TIMEOUT_CTR bit field. 0h: Interrupt is not generated 1h: RES Packet Timeout Error
15	ADMA2_ADMA3	R/W1C	0h	ADMA2/3 Error Setting of this bit means that ADMA2/3 Error occurs in UHS-II mode. ADMA2/3 Error Status is indicated to the MMCSD0_ADMA_ERR_STATUS register, which is defined in the Host spec 3.00. 0h: Interrupt is not generated 1h: ADMA2/3 Error
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W1C	0h	EBSY Error On receiving EBSY packet, if the packet indicates an error, this bit is set to 1h. Setting of this bit also sets Error Interrupt and Transfer Completer together in the MMCSD0_NORMAL_INTR_STS register. This error check is effective for a command with setting the MMCSD0_UHS2_XFER_MODE[14] EBSY_WAIT bit. 0h: Interrupt is not generated 1h: EBSY Error (Backend Error)
7	UNRECOVERABLE	R/W1C	0h	Unrecoverable Error Setting of this bit means that Unrecoverable Error is set in a packet from a device. 0h: Interrupt is not generated 1h: Device Unrecoverable Error
6	RESERVED	R	0h	Reserved
5	TID	R/W1C	0h	TID Error Setting of this bit means that TID Error occurs. 0h: Interrupt is not generated 1h: TID Error

Table 14-23838. MMCSD0_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	FRAMING	R/W1C	0h	Framing Error Setting of this bit means that Framing Error occurs during a packet receiving. 0h: Interrupt is not generated 1h: Framing Error
3	CRC	R/W1C	0h	CRC Error Setting of this bit means that CRC Error occurs during a packet receiving. 0h: Interrupt is not generated 1h: CRC Error
2	RETRY_EXPIRED	R/W1C	0h	Retry Expired Setting of this bit means that Retry Counter Expired Error occurs during data transfer. If this bit is set, either Framing Error or CRC Error in this register shall be set. 0h: Interrupt is not generated 1h: Retry Expired Error
1	RESP_PKT	R/W1C	0h	RES Packet Error Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If the MMCSD0_UHS2_XFER_MODE[7] RESP_ERR_CHK_ENA bit is set to 1h, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1h. 0h: Interrupt is not generated 1h: RES Packet Error
0	HEADER	R/W1C	0h	Header Error Setting of this bit means that Header Error occurs in a received packet. 0h: Interrupt is not generated 1h: Header Error

58 MMCSD0_UHS2_ERR_INTR_STS_ENA Register (Offset = C8h) [reset = 0h]

MMCSD0_UHS2_ERR_INTR_STS_ENA is shown in Figure 14-7874 and described in Table 14-15967.

Return to Summary Table.

This register is used to enable the MMCSD0_UHS2_ERR_INTR_STS register fields.

Table 14-23839. MMCSD0_UHS2_ERR_INTR_STS_ENA Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00C8h

Figure 14-7874. MMCSD0_UHS2_ERR_INTR_STS_ENA Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC					RESERVED		
R/W-0h					R-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADMA2_ADMA3	RESERVED						EBSY
R/W-0h	R-0h						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23841. MMCSD0_UHS2_ERR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECFIC	R/W	0h	Vendor Specific Error Setting this bit to 1h enables setting of Vendor Specific Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Timeout for Deadlock Setting this bit to 1h enables setting of Timeout for Dead lock bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

Table 14-23841. MMCSD0_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W	0h	Timeout for CMD_RES Setting this bit to 1h enables setting of Timeout for CMD_RES bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
15	ADMA2_ADMA3	R/W	0h	ADMA2/3 Error Setting this bit to 1h enables setting of ADMA2/3 Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W	0h	EBSY Error Setting this bit to 1h enables setting of EBSY Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
7	UNRECOVERABLE	R/W	0h	Unrecoverable Error Setting this bit to 1h enables setting of Unrecoverable Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
6	RESERVED	R	0h	Reserved
5	TID	R/W	0h	TID Error Setting this bit to 1h enables setting of TID Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
4	FRAMING	R/W	0h	Framing Error Setting this bit to 1h enables setting of Framing Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

Table 14-23841. MMCSD0_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CRC	R/W	0h	CRC Error Setting this bit to 1h enables setting of CRC Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
2	RETRY_EXPIRED	R/W	0h	Retry Expired Setting this bit to 1h enables setting of Retry Expired bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
1	RESP_PKT	R/W	0h	RES Packet Error Setting this bit to 1h enables setting of RES Packet Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
0	HEADER	R/W	0h	Header Error Setting this bit to 1h enables setting of Header Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

59 MMCSD0_UHS2_ERR_INTR_SIG_ENA Register (Offset = CCh) [reset = 0h]

MMCSD0_UHS2_ERR_INTR_SIG_ENA is shown in Figure 14-7875 and described in Table 14-15969.

Return to Summary Table.

This register is used to generate UHS-II Interrupt signals.

Table 14-23842. MMCSD0_UHS2_ERR_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00CCh

Figure 14-7875. MMCSD0_UHS2_ERR_INTR_SIG_ENA Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC					RESERVED		
R/W-0h					R-0h		

23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W-0h	R-0h						R/W-0h

7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED_SIG_ENA	RESP_PKT	HEADER
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23844. MMCSD0_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECFIC	R/W	0h	Vendor Specific Error Setting of a bit to 1h in this field enables generating interrupt signal when correspondent bit of Vendor Specific Error is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Timeout for Deadlock Setting this bit to 1h enables generating interrupt signal when Timeout for Dead lock bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

Table 14-23844. MMCSD0_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W	0h	Timeout for CMD_RES Setting this bit to 1h enables generating interrupt signal when Timeout for CMD_RES bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
15	ADMA2_ADMA3	R/W	0h	ADMA2/3 Error Setting this bit to 1h enables generating interrupt signal when ADMA2/3 Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W	0h	EBSY Error Setting this bit to 1h enables generating interrupt signal when EBSY Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
7	UNRECOVERABLE	R/W	0h	Unrecoverable Error Setting this bit to 1h enables generating interrupt signal when Unrecoverable Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
6	RESERVED	R	0h	Reserved
5	TID	R/W	0h	TID Error Setting this bit to 1h enables generating interrupt signal when TID Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
4	FRAMING	R/W	0h	Framing Error Setting this bit to 1h enables generating interrupt signal when Framing Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

Table 14-23844. MMCSD0_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CRC	R/W	0h	CRC Error Setting this bit to 1h enables generating interrupt signal when CRC Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
2	RETRY_EXPIRED_SIG_ENA	R/W	0h	Retry Expired Setting this bit to 1h enables generating interrupt signal when Retry Expired bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
1	RESP_PKT	R/W	0h	RES Packet Error Setting this bit to 1h enables generating interrupt signal when RES Packet Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
0	HEADER	R/W	0h	Header Error Setting this bit to 1h enables generating interrupt signal when Header Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

60 MMCSD0_UHS2_SETTINGS_PTR Register (Offset = E0h) [reset = 100h]

MMCSD0_UHS2_SETTINGS_PTR is shown in Figure 14-7876 and described in Table 14-15971.

Return to Summary Table.

This register is pointer for UHS-II settings.

Table 14-23845. MMCSD0_UHS2_SETTINGS_PTR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00E0h

Figure 14-7876. MMCSD0_UHS2_SETTINGS_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_SETTINGS_PTR															
R-100h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23847. MMCSD0_UHS2_SETTINGS_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_SETTINGS_PTR	R	100h	Pointer for UHS-II Settings Register

61 MMCSD0_UHS2_CAPABILITIES_PTR Register (Offset = E2h) [reset = 110h]

MMCSD0_UHS2_CAPABILITIES_PTR is shown in Figure 14-7877 and described in Table 14-15973.

Return to Summary Table.

This register is pointer for UHS-II Capabilities Register.

Table 14-23848. MMCSD0_UHS2_CAPABILITIES_PTR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00E2h

Figure 14-7877. MMCSD0_UHS2_CAPABILITIES_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_CAPABILITIES_PTR															
R-110h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23850. MMCSD0_UHS2_CAPABILITIES_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_CAPABILITIES_PTR	R	110h	Pointer for UHS-II Capabilities Register

62 MMCSD0_UHS2_TEST_PTR Register (Offset = E4h) [reset = 120h]

MMCSD0_UHS2_TEST_PTR is shown in Figure 14-7878 and described in Table 14-15975.

Return to Summary Table.

This register is pointer for UHS-II Test Register.

Table 14-23851. MMCSD0_UHS2_TEST_PTR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00E4h

Figure 14-7878. MMCSD0_UHS2_TEST_PTR Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">UHS2_TEST_PTR</td></tr>
<tr><td colspan="16">R-120h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23853. MMCSD0_UHS2_TEST_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_TEST_PTR	R	120h	Pointer for UHS-II Test Register

63 MMCSD0_SHARED_BUS_CTRL_PTR Register (Offset = E6h) [reset = 130h]

MMCSD0_SHARED_BUS_CTRL_PTR is shown in Figure 14-7879 and described in Table 14-15977.

Return to Summary Table.

This register is pointer for UHS-II Shared Bus Control Register.

Table 14-23854. MMCSD0_SHARED_BUS_CTRL_PTR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00E6h

Figure 14-7879. MMCSD0_SHARED_BUS_CTRL_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHARED_BUS_CTRL_PTR															
R-130h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23856. MMCSD0_SHARED_BUS_CTRL_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SHARED_BUS_CTRL_PTR	R	130h	Pointer for Shared Bus Control Register

64 MMCSD0_VENDOR_SPECFIC_PTR Register (Offset = E8h) [reset = 140h]

MMCSD0_VENDOR_SPECFIC_PTR is shown in Figure 14-7880 and described in Table 14-15979.

Return to Summary Table.

This register is pointer for UHS-II Vendor Specific Register.

Table 14-23857. MMCSD0_VENDOR_SPECFIC_PTR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00E8h

Figure 14-7880. MMCSD0_VENDOR_SPECFIC_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR_SPECFIC_PTR															
R-140h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23859. MMCSD0_VENDOR_SPECFIC_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_SPECFIC_PTR	R	140h	Pointer for Vendor Specific Area

65 MMCSD0_BOOT_TIMEOUT_CONTROL Register (Offset = F4h) [reset = 0h]

MMCSD0_BOOT_TIMEOUT_CONTROL is shown in Figure 14-7881 and described in Table 14-15981.

Return to Summary Table.

This is used to program the boot timeout value counter.

Table 14-23860. MMCSD0_BOOT_TIMEOUT_CONTROL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00F4h

Figure 14-7881. MMCSD0_BOOT_TIMEOUT_CONTROL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_TIMEOUT_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23862. MMCSD0_BOOT_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_TIMEOUT_CNT	R/W	0h	Boot Data Timeout Counter Value This value determines the interval by which DAT line timeouts are detected during boot operation for eMMC4.4 card. The value is in number of SD clock.

66 MMCSD0_VENDOR_REGISTER Register (Offset = F8h) [reset = 4E20h]

MMCSD0_VENDOR_REGISTER is shown in Figure 14-7882 and described in Table 14-15983.

Return to Summary Table.

Vendor register added for Auto Gate SD CLK, CMD11 Power Down Timer, Enhanced Strobe and eMMC Hardware Reset.

Table 14-23863. MMCSD0_VENDOR_REGISTER Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00F8h

Figure 14-7882. MMCSD0_VENDOR_REGISTER Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							AUTOGATE_SDCLK
R-0h							R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CMD11_PD_TIMER							
R/W-1388h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD11_PD_TIMER						EMMC_HW_RESET	ENHANCED_STROBE
R/W-1388h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23865. MMCSD0_VENDOR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	AUTOGATE_SDCLK	R/W	0h	Auto Gate SD CLK If this bit is set, SD CLK will be gated automatically when there is no transfer. This is applicable only for Embedded Device. 0h: Disable 1h: Enable
15-2	CMD11_PD_TIMER	R/W	1388h	CMD11 Power Down Timer Value

Table 14-23865. MMCSD0_VENDOR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EMMC_HW_RESET	R/W	0h	eMMC Hardware Reset Hardware reset signal is generared for eMMC card when this bit is set. 0h: De-sassert hardware reset pin 1h: Drives the hardware reset pin as ZERO (Active LOW to eMMC card)
0	ENHANCED_STROBE	R/W	0h	Enhanced Strobe This bit enables the enhanced strobe logic of the Host Controller.

67 MMCSD0_SLOT_INT_STS Register (Offset = FCh) [reset = 0h]

MMCSD0_SLOT_INT_STS is shown in Figure 14-7883 and described in Table 14-15985.

Return to Summary Table.

This register is used to read the interrupt signal for each slot.

Table 14-23866. MMCSD0_SLOT_INT_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00FCh

Figure 14-7883. MMCSD0_SLOT_INT_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTR_SIG							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 14-23868. MMCSD0_SLOT_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	INTR_SIG	R	0h	Interrupt Signal for Slot#0 These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

68 MMCSD0_HOST_CONTROLLER_VER Register (Offset = FEh) [reset = 1004h]

MMCSD0_HOST_CONTROLLER_VER is shown in Figure 14-7884 and described in Table 14-15987.

Return to Summary Table.

This register is used to read the vendor version number and specification version number.

Table 14-23869. MMCSD0_HOST_CONTROLLER_VER Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 00FEh

Figure 14-7884. MMCSD0_HOST_CONTROLLER_VER Register

15	14	13	12	11	10	9	8
VEN_VER_NUM							
R-10h							

7	6	5	4	3	2	1	0
SPEC_VER_NUM							
R-4h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23871. MMCSD0_HOST_CONTROLLER_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	VEN_VER_NUM	R	10h	Vendor Version Number The Vendor Version Number is set to 10h (1.0)
7-0	SPEC_VER_NUM	R	4h	Specification Version Number This status indicates the Host Controller Specification Version. The upper and lower 4-bits indicate the version. 0h: SD Host Controller Specification Version 1.00 1h: SD Host Controller Specification Version 2.00 Including the feature of the ADMA and Test Register 2h: SD Host Controller Specification Version 3.00 3h: SD Host Controller Specification Version 4.00 4h: SD Host Controller Specification Version 4.10 Others: Reserved

69 MMCSD0_UHS2_GEN_SETTINGS Register (Offset = 100h) [reset = 0h]

MMCSD0_UHS2_GEN_SETTINGS is shown in Figure 14-7885 and described in Table 14-15989.

Return to Summary Table.

Start Address of General settings is pointed by the MMCSD0_UHS2_SETTINGS_PTR Register.

Table 14-23872. MMCSD0_UHS2_GEN_SETTINGS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0100h

Figure 14-7885. MMCSD0_UHS2_GEN_SETTINGS Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">NUMLANES</td></tr>
<tr><td colspan="2">R-0h</td><td colspan="6">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>POWER_MODE</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23874. MMCSD0_UHS2_GEN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	NUMLANES	R/W	0h	Number of Lanes and Functionalities The lane configuration of a Host System is set to this field depends on the capability among Host Controller and connected devices. 2 Lanes FD mode is mandatory and the others modes are optional. 0h: 2 Lanes FD or 2L-HD 1h: Not Used 2h: 3 Lanes 2D1U-FD (Embedded) 3h: 3 Lanes 1D2U-FD (Embedded) 4h: 4 Lanes 2D2U-FD (Embedded) Others: Reserved
7-1	RESERVED	R	0h	Reserved

Table 14-23874. MMCSD0_UHS2_GEN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POWER_MODE	R/W	0h	Power Mode This field determines either Fast mode or Low Power mode. Host and all devices connected to the host shall be set to the same mode. 0h: Fast Mode 1h: Low Power Mode

70 MMCSD0_UHS2_PHY_SETTINGS Register (Offset = 104h) [reset = 0h]

MMCSD0_UHS2_PHY_SETTINGS is shown in Figure 14-7886 and described in Table 14-15991.

Return to Summary Table.

Start Address of PHY settings is pointed by the MMCSD0_UHS2_SETTINGS_PTR Register.

Table 14-23875. MMCSD0_UHS2_PHY_SETTINGS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0104h

Figure 14-7886. MMCSD0_UHS2_PHY_SETTINGS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
N_LSS_DIR				N_LSS_SYN			
R/W-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HIBERNATE_ENA	RESERVED						
R/W-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEED_RANGE		RESERVED					
R/W-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23877. MMCSD0_UHS2_PHY_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	N_LSS_DIR	R/W	0h	Host N_LSS_DIR The largest value of N_LSS_DIR capabilities among the Host Controller and Connected Devices is set to this field. 0h: 8 x 16 LSS 1h: 8 x 1 LSS 2h: 8 x 2 LSS 3h: 8 x 3 LSS .... Fh: 8 x 15 LSS

Table 14-23877. MMCSD0_UHS2_PHY_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	N_LSS_SYN	R/W	0h	Host N_LSS_SYN The largest value of N_LSS_SYN capabilities among the Host Controller and Connected Devices is set to this field. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h - 4 x 3 LSS .... Fh: 4 x 15 LSS
15	HIBERNATE_ENA	R/W	0h	Hibernate Enable After checking card capability of Hibernate mode, if all devices support Hibernate mode, this bit may be set. This bit determines whether Host remains in Dormant state or goes to Hibernate state. In Hibernate mode, VDD1 Power may be off. 0h: Hibernate Disabled 1h: Hibernate Enabled
14-8	RESERVED	R	0h	Reserved
7-6	SPEED_RANGE	R/W	0h	Speed Range PLL multiplier is selected by this field. Change of PLL Multiplier is not effective immediately and is applied from exiting Dormant State. 0h: Range A (Defalt) 1h: Range B 2h: Reserved 3h: Reserved
5-0	RESERVED	R	0h	Reserved

71 MMCSD0_UHS2_LNK_TRN_SETTINGS Register (Offset = 108h) [reset = 0h]

MMCSD0_UHS2_LNK_TRN_SETTINGS is shown in Figure 14-7887 and described in Table 14-15993.

Return to Summary Table.

Start Address of LINK/TRAN settings is pointed by the MMCSD0_UHS2_SETTINGS_PTR Register.

Table 14-23878. MMCSD0_UHS2_LNK_TRN_SETTINGS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0108h

Figure 14-7887. MMCSD0_UHS2_LNK_TRN_SETTINGS Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
N_DATA_GAP							
R/W-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						RETRY_COUNT	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
HOST_NFCU							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23880. MMCSD0_UHS2_LNK_TRN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved

Table 14-23880. MMCSD0_UHS2_LNK_TRN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39-32	N_DATA_GAP	R/W	0h	Host N_DATA_GAP The largest value of N_DATA_GAP capabilities among the Host Controller and Connected Devices is set to this field. 00h: No Gap 01h: 1 LSS 02h: 2 LSS 03h: 3 LSS .... FFh: 255 LSS
31-18	RESERVED	R	0h	Reserved
17-16	RETRY_COUNT	R/W	0h	Retry Count Data Burst retry count is set to this field. 00h: Retry Disabled 01h: 1 time 02h: 2 times 03h: 3 times
15-8	HOST_NFCU	R/W	0h	Host N_FCU Host Driver sets the number of blocks in Data Burst (Flow Control) to this field. The value shall be smaller than or equal to N_FCU capabilities among the Host Controller and connected card and devices. Setting 1 to 4 blocks is recommended considering buffer size. 00h: 256 Blocks 01h: 1 Block 02h: 2 Blocks 03h: 3 Blocks .... FFh: 255 Blocks
7-0	RESERVED	R	0h	Reserved

72 MMCSD0_UHS2_GEN_CAP Register (Offset = 110h) [reset = 44F11h]

MMCSD0_UHS2_GEN_CAP is shown in Figure 14-7888 and described in Table 14-15995.

Return to Summary Table.

Start Address of General Capabilities is pointed by the MMCSD0_UHS2_GEN_CAP Register.

Table 14-23881. MMCSD0_UHS2_GEN_CAP Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0110h

Figure 14-7888. MMCSD0_UHS2_GEN_CAP Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">CORECFG_UHS2_BUS_TOPLOGY</td><td colspan="4">CORECFG_UHS2_MAX_DEVICES</td><td colspan="2">DEVICE_TYPE</td></tr>
<tr><td colspan="2">R-0h</td><td colspan="4">R-1h</td><td colspan="2">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>CFG_64BIT_ADDRESSING</td><td colspan="6">NUM_LANES</td></tr>
<tr><td>R-0h</td><td>R-1h</td><td colspan="6">R-Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">GAP</td><td colspan="4">DAP</td></tr>
<tr><td colspan="4">R-1h</td><td colspan="4">R-1h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23883. MMCSD0_UHS2_GEN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-22	CORECFG_UHS2_BUS_TOPLOGY	R	0h	Bus Topology This field indicates one of bus topologies configured by a Host system. 0h: P2P Connection 1h: Ring Connection 2h: HUB Connection 3h: HUB is Connected in Ring

Table 14-23883. MMCSD0_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-18	CORECFG_UHS2_MAX_DEVICES	R	1h	Number of Devices Supported This field indicates the maximum number of devices supported by the Host Controller. 0h: Not used 1h: 1 Devices 2h: 2 Devices .... Fh: 15 Devices
17-16	DEVICE_TYPE	R	0h	Removable/Embedded This field indicates device type configured by a Host system. 0h: Removable Card (P2P) 1h: Embedded Devices 2h: Embedded Devices + Removable Card 3h: Reserved
15	RESERVED	R	0h	Reserved
14	CFG_64BIT_ADDRESSING	R	1h	64-bit Addressing This field indicates support of 64-bit addressing by the Host Controller. 0h: 32-bit Addressing is supported 1h: 32-bit and 64-bit Addressing is supported
13-8	NUM_LANES	R	Fh	Number of Lanes and Functionalities This field indicates support of lanes by the Host Controller. 0 mean not supported and 1 means supported. D08: 2L-HD D09: 2D1U-FD D10: 1D2U-FD D11: 2D2U-FD D12: Reserved D13: Reserved

Table 14-23883. MMCSD0_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	GAP	R	1h	GAP (Group Allocation Power) This field indicates the maximum capability of host power supply for a group configured by a Host system. This field is used to set the argument of DEVICE_INIT CCM. 0h: Not used 1h: 360 mW 2h: 720 mW .... Fh: 360 x 15 mW
3-0	DAP	R	1h	DAP (Device Allocation Power) This field indicates the maximum capability of host power supply for a device configured by a Host system. This field is used to set the argument of DEVICE_INIT CCMD. 0h: 360 mW (Default) 1h: 360 mW 2h: 720 mW .... Fh: 360 x 15 mW

73 MMCSD0_UHS2_PHY_CAP Register (Offset = 114h) [reset = 110000h]

MMCSD0_UHS2_PHY_CAP is shown in Figure 14-7889 and described in Table 14-15997.

Return to Summary Table.

Start Address of PHY Capabilities is pointed by the MMCSD0_UHS2_CAPABILITIES_PTR Register.

Table 14-23884. MMCSD0_UHS2_PHY_CAP Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0114h

Figure 14-7889. MMCSD0_UHS2_PHY_CAP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
N_LSS_DIR				N_LSS_SYN			
R-1h				R-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEED_RANGE		RESERVED					
R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23886. MMCSD0_UHS2_PHY_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	N_LSS_DIR	R	1h	Host N_LSS_DIR This field indicates the minimum N_LSS_DIR required by the Host Controller. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h: 4 x 3 LSS .... Fh: 4 x 15 LSS

Table 14-23886. MMCSD0_UHS2_PHY_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	N_LSS_SYN	R	1h	Host N_LSS_SYN This field indicates the minimum N_LSS_SYN required by the Host Controller. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h: 4 x 3 LSS .... Fh: 4 x 15 LSS
15-8	RESERVED	R	0h	Reserved
7-6	SPEED_RANGE	R	0h	Speed Range This field indicates supported Speed Range by the Host Controller. 0h: Range A (Default) 1h: Range A and Range B 2h: Reserved 3h: Reserved
5-0	RESERVED	R	0h	Reserved

74 MMCSD0_UHS2_LNK_TRN_CAP Register (Offset = 118h) [reset = 8120000100h]

MMCSD0_UHS2_LNK_TRN_CAP is shown in Figure 14-7890 and described in Table 14-15999.

Return to Summary Table.

Start Address of LINK/TRAN settings is pointed by the MMCSD0_UHS2_CAPABILITIES_PTR Register.

Table 14-23887. MMCSD0_UHS2_LNK_TRN_CAP Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0118h

Figure 14-7890. MMCSD0_UHS2_LNK_TRN_CAP Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>56</td><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">N_DATA_GAP</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R-81h</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="12">MAX_BLK_LENGTH</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="12">R-200h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">N_FCU</td><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-1h</td><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23889. MMCSD0_UHS2_LNK_TRN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39-32	N_DATA_GAP	R	81h	Host N_DATA_GAP This field indicates the minimum number of data gap (DIDL) supported by the Host Controller. 00h: No Gap 01h: 1 LSS 02h: 2 LSS 03h: 3 LSS .... FFh: 255 LSS

Table 14-23889. MMCSD0_UHS2_LNK_TRN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31-20	MAX_BLK_LENGTH	R	200h	Host Maximum Block Length This field indicates maximum block length by the Host Controller. 000h: Not Used 001h: 1 byte 002h: 2 bytes .... 200h: 512 bytes .... 800h: 2048 bytes 801h - FFFh: Not Used
19-16	RESERVED	R	0h	Reserved
15-8	N_FCU	R	1h	Host N_FCU This field indicates maximum the number of blocks in a Flow Control unit by the Host Controller. This value is determined by supported buffer size. 00h: 256 Blocks 01h: 1 Block 02h: 2 Block 03h: 3 Block .... FFh: 255 Blocks
7-0	RESERVED	R	0h	Reserved

75 MMCSD0_FORCE_UHSII_ERR_INT_STS Register (Offset = 120h) [reset = 0h]

MMCSD0_FORCE_UHSII_ERR_INT_STS is shown in Figure 14-7891 and described in Table 14-16001.

Return to Summary Table.

This register is not physically implemented, rather it is an address where the MMCSD0_UHS2_ERR_INTR_STS register can be written.

Table 14-23890. MMCSD0_FORCE_UHSII_ERR_INT_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0120h

Figure 14-7891. MMCSD0_FORCE_UHSII_ERR_INT_STS Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC					RESERVED		
W-0h					R-0h		

23	22	21	20	19	18	17	16
RESERVED						TIMEOUT_DEADLOCK	TIMEOUT_CMD_RES
R-0h						W-0h	W-0h

15	14	13	12	11	10	9	8
ADMA	RESERVED						EBSY
W-0h	R-0h						W-0h

7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RES_PKT	HEADER
W-0h	R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 14-23892. MMCSD0_FORCE_UHSII_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC	W	0h	Force Event for Vendor Specific Error 0h: Not Affected 1h: Vendor Specific Error Status is set
26-18	RESERVED	R	0h	Reserved
17	TIMEOUT_DEADLOCK	W	0h	Force Event for Timeout for Deadlock Setting this bit forces the Host Controller to set Timeout for Deadlock in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Timeout for Deadlock Error status is set

Table 14-23892. MMCSD0_FORCE_UHSII_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TIMEOUT_CMD_RES	W	0h	Force Event for Timeout for CMD_RES Setting this bit forces the Host Controller to set Timeout for CMD_RES in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Timout for CMD_RES Status is set
15	ADMA	W	0h	Force Event for ADMA Error Setting this bit forces the Host Controller to set ADMA Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: ADMA Error Status is set
14-9	RESERVED	R	0h	Reserved
8	EBSY	W	0h	Force Event for EBSY Error Setting this bit forces the Host Controller to set EBSY Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: EBSY Error Status is set
7	UNRECOVERABLE	W	0h	Force Event for Unrecoverable Error Setting this bit forces the Host Controller to set Unrecoverable Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Unrecoverable Error Status is set
6	RESERVED	R	0h	Reserved
5	TID	W	0h	Force Event for TID Error Setting this bit forces the Host Controller to set TID Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: TID Error Status is set
4	FRAMING	W	0h	Force Event for Framing Error Setting this bit forces the Host Controller to set Framing Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Framing Error Status is set

Table 14-23892. MMCSD0_FORCE_UHSII_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CRC	W	0h	Force Event for CRC Error Setting this bit forces the Host Controller to set CRC Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: CRC Error Status is set
2	RETRY_EXPIRED	W	0h	Force Event for Retry Expired Setting this bit forces the Host Controller to set Retry Expired in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Retry expired error status is set
1	RES_PKT	W	0h	Force Event for RES Packet Error Setting this bit forces the Host Controller to set RES Packet Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: RES packet error status is set
0	HEADER	W	0h	Force Event for Header Error Setting this bit forces the Host Controller to set Header Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Header error status is set

76 MMCSD0_CQ_VERSION Register (Offset = 200h) [reset = 510h]

MMCSD0_CQ_VERSION is shown in Figure 14-7892 and described in Table 14-16003.

Return to Summary Table.

This register provides information about the version of the eMMC CQ (Command Queueing) standard which is 285 implemented by the CQE, in BCD format. The current version is rev 5.1.

The following table describes the CQBASE+00h: Command Queueing Version.

Table 14-23893. MMCSD0_CQ_VERSION Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0200h

Figure 14-7892. MMCSD0_CQ_VERSION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				EMMC_MAJOR_VER_NUM			
R-0h				R-5h			
7	6	5	4	3	2	1	0
EMMC_MINOR_VER_NUM				EMMC_VERSION_SUFFIX			
R-1h				R-0h			

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23895. MMCSD0_CQ_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	EMMC_MAJOR_VER_NUM	R	5h	eMMC Major Version Number (digit left of decimal point), in BCD format
7-4	EMMC_MINOR_VER_NUM	R	1h	eMMC Minor Version Number (digit right of decimal point), in BCD format
3-0	EMMC_VERSION_SUFFIX	R	0h	eMMC Version Suffix (2nd digit right of decimal point), in BCD format

77 MMCSD0_CQ_CAPABILITIES Register (Offset = 204h) [reset = 30C8h]

MMCSD0_CQ_CAPABILITIES is shown in Figure 14-7893 and described in Table 14-16005.

Return to Summary Table.

This register is reserved for capability indication.

Table 14-23896. MMCSD0_CQ_CAPABILITIES Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0204h

Figure 14-7893. MMCSD0_CQ_CAPABILITIES Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">CF_MUL</td><td colspan="2">RESERVED</td><td colspan="2">CF_VAL</td></tr>
<tr><td colspan="4">R-3h</td><td colspan="2">R-0h</td><td colspan="2">R-C8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CF_VAL</td></tr>
<tr><td colspan="8">R-C8h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23898. MMCSD0_CQ_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	CF_MUL	R	3h	**Internal Timer Clock Frequency Multiplier (ITCFMUL)** ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details (MMCSD0_CQ_CAPABILITIES[9-0] CF_VAL). Field Value Description: 0h: 0.001 MHz 1h: 0.01 MHz 2h: 0.1 MHz 3h: 1 MHz 4h: 10 MHz Other values are reserved
11-10	RESERVED	R	0h	Reserved

Table 14-23898. MMCSD0_CQ_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	CF_VAL	R	C8h	**Internal Timer Clock Frequency Value (ITCFVAL)** ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the polling period when using periodic SEND_QUEUE_STATUS (CMD13) polling. The clock frequency is calculated as ITCFVAL × ITCFMUL. For example, to encode 19.2 MHz ITCFVAL shall be C0h (= 192 decimal) and ITCFMUL shall be 2h (0.1 MHz). 192 × 0.1 MHz = 19.2 MHz

78 MMCSD0_CQ_CONFIG Register (Offset = 208h) [reset = 0h]

MMCSD0_CQ_CONFIG is shown in Figure 14-7894 and described in Table 14-16007.

Return to Summary Table.

This register controls CQE behavior affecting the general operation of command queueing 290 module or operation of multiple tasks in the same time.

Table 14-23899. MMCSD0_CQ_CONFIG Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0208h

Figure 14-7894. MMCSD0_CQ_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			DCMD_ENA	RESERVED			TASK_DESC_SIZE
R-0h			R/W-0h	R-0h			R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CQ_ENABLE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23901. MMCSD0_CQ_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	DCMD_ENA	R/W	0h	**Direct Command (DCMD) Enable** This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 0h: Task descriptor in slot #31 is a Data Transfer Task Descriptor 1h: Task descriptor in slot #31 is a DCMD Task Descriptor
11-9	RESERVED	R	0h	Reserved

Table 14-23901. MMCSD0_CQ_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TASK_DESC_SIZE	R/W	0h	**Task Descriptor Size** This bit indicates whether the task descriptor size is 128 bits or 64 bits . This bit can only be configured when the MMCSD0_CQ_CONFIG[0] CQ_ENABLE bit is 0hh (command queueing is disabled). Bit Value Description 0h: Task descriptor size is 64 bits 1h: Task descriptor size is 128 bits
7-1	RESERVED	R	0h	Reserved
0	CQ_ENABLE	R/W	0h	**Command Queueing Enable** Software shall write 1h to this bit when in order to enable command queueing mode (enable CQE). When this bit is 0h, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes 1h to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queueing mode, it shall clear all previous tasks if such exist before setting this bit to 0h.

79 MMCSD0_CQ_CONTROL Register (Offset = 20Ch) [reset = 0h]

MMCSD0_CQ_CONTROL is shown in Figure 14-7895 and described in Table 14-16009.

Return to Summary Table.

This register controls CQE behavior affecting the general operation of command queueing 293 module or operation of multiple tasks in the same time.

Table 14-23902. MMCSD0_CQ_CONTROL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 020Ch

Figure 14-7895. MMCSD0_CQ_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CLEAR_ALL_TASKS
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							HALT_BIT
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23904. MMCSD0_CQ_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CLEAR_ALL_TASKS	R/W	0h	**Clear All Tasks** Software shall write 1h to this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state (Halt bit is 1h). When software writes 1h, the value of the register is updated to 1h, and CQE shall reset the MMCSD0_CQ_TASK_DOOR_BELL register and all other context information for all unfinished tasks. Then CQE will clear this bit. Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is softwares responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0h to this register shall have no effect.
7-1	RESERVED	R	0h	Reserved

Table 14-23904. MMCSD0_CQ_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_BIT	R/W	0h	**Halt** Host software shall write 1h to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT). When software writes 1h, CQE shall complete the ongoing task if such a task is in progress. Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1h. Software may poll on this bit until it is set to 1h, and may only then send commands on the eMMC bus. In order to exit halt state (resume CQE activity), software shall clear this bit (write 0h). Writing 0h when the value is already 0h shall have no effect.

80 MMCSD0_CQ_INTR_STS Register (Offset = 210h) [reset = 0h]

MMCSD0_CQ_INTR_STS is shown in Figure 14-7896 and described in Table 14-16011.

Return to Summary Table.

This register indicates pending interrupts that require service. Each bit in this registers is asserted 296 in response a specific event, only if the respective bit is set in the MMCSD0_CQ_INTR_STS_ENA register.

Table 14-23905. MMCSD0_CQ_INTR_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0210h

Figure 14-7896. MMCSD0_CQ_INTR_STS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-23907. MMCSD0_CQ_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W1C	0h	**Task Error Interrupt (TERR)** This bit is asserted when task error is detected due to invalid task descriptor.
3	TASK_CLEARED	R/W1C	0h	**Task Cleared (TCL)** This status bit is asserted (if MMCSD0_CQ_INTR_STS_ENA[3] TASK_CLEARED = 1h) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (MMCSD0_CQ_TASK_CLEAR) or clearing of all tasks (MMCSD0_CQ_CONTROL).

Table 14-23907. MMCSD0_CQ_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W1C	0h	**Response Error Detected Interrupt (RED)** This status bit is asserted (if MMCSD0_CQ_INTR_STS_ENA[2] RESP_ERR_DET = 1h) when a response is received with an error bit set in the device status field. Software uses the MMCSD0_CQ_RESP_ERR_MASK register to configure which device status bit fields may trigger an interrupt, and which are masked.
1	TASK_COMPLETE	R/W1C	0h	**Task Complete Interrupt (TCC)** This status bit is asserted (if MMCSD0_CQ_INTR_STS_ENA[1] TASK_COMPLETE = 1h) when at least one of the following two conditions are met: (1) A task is completed and the INT bit is set in its Task Descriptor (2) Interrupt caused by Interrupt Coalescing logic
0	HALT_COMPLETE	R/W1C	0h	**Halt Complete Interrupt (HAC)** This status bit is asserted (if MMCSD0_CQ_INTR_STS_ENA[0] HALT_COMPLETE = 1h) when the MMCSD0_CQ_CONTROL[0] HALT_BIT bit transitions from 0h to 1h indicating that host controller has completed its current ongoing task and has entered halt state.

81 MMCSD0_CQ_INTR_STS_ENA Register (Offset = 214h) [reset = 0h]

MMCSD0_CQ_INTR_STS_ENA is shown in Figure 14-7897 and described in Table 14-16013.

Return to Summary Table.

This register enables and disables the reporting of the corresponding interrupt to host software in 299 MMCSD0_CQ_INTR_STS register. When a bit is set (1h) and the corresponding interrupt condition is active, then the 300 bit in the MMCSD0_CQ_INTR_STS register is asserted. Interrupt sources that are disabled (0h) are not indicated in the MMCSD0_CQ_INTR_STS 301 register. This register is bit-index matched to the MMCSD0_CQ_INTR_STS register.

Table 14-23908. MMCSD0_CQ_INTR_STS_ENA Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0214h

Figure 14-7897. MMCSD0_CQ_INTR_STS_ENA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23910. MMCSD0_CQ_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W	0h	**Task Error Interrupt Status Enable (TERR)** 1h: MMCSD0_CQ_INTR_STS[4] TASK_ERROR bit will be set when its interrupt condition is active 0h: MMCSD0_CQ_INTR_STS[4] TASK_ERROR bit is disabled
3	TASK_CLEARED	R/W	0h	**Task Cleared Status Enable (TCL)** 1h: MMCSD0_CQ_INTR_STS[3] TASK_CLEARED bit will be set when its interrupt condition is active 0h: MMCSD0_CQ_INTR_STS[3] TASK_CLEARED bit is disabled

Table 14-23910. MMCSD0_CQ_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W	0h	**Response Error Detected Status Enable (RED)** 1h: MMCSD0_CQ_INTR_STS[2] RESP_ERR_DET bit will be set when its interrupt condition is active 0h: MMCSD0_CQ_INTR_STS[2] RESP_ERR_DET bit is disabled
1	TASK_COMPLETE	R/W	0h	**Task Complete Status Enable (TCC)** 1h: MMCSD0_CQ_INTR_STS[1] TASK_COMPLETE bit will be set when its interrupt condition is active 0h: MMCSD0_CQ_INTR_STS[1] TASK_COMPLETE bit is disabled
0	HALT_COMPLETE	R/W	0h	**Halt Complete Status Enable (HAC)** 1h: MMCSD0_CQ_INTR_STS[0] HALT_COMPLETE bit will be set when its interrupt condition is active 0h: MMCSD0_CQ_INTR_STS[0] HALT_COMPLETE bit is disabled

82 MMCSD0_CQ_INTR_SIG_ENA Register (Offset = 218h) [reset = 0h]

MMCSD0_CQ_INTR_SIG_ENA is shown in Figure 14-7898 and described in Table 14-16015.

Return to Summary Table.

This register enables and disables the generation of interrupts to host software. When a bit is set 304 (1h) and the corresponding bit in the MMCSD0_CQ_INTR_STS register is set, then an interrupt is generated. Interrupt sources 305 that are disabled (0h) are still indicated in the MMCSD0_CQ_INTR_STS register. This register is bit-index matched 306 to the MMCSD0_CQ_INTR_STS register.

Table 14-23911. MMCSD0_CQ_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0218h

Figure 14-7898. MMCSD0_CQ_INTR_SIG_ENA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23913. MMCSD0_CQ_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W	0h	**Task Error Interrupt Signal Enable (TERR)** When set and the MMCSD0_CQ_INTR_STS[4] TASK_ERROR bit is asserted, the CQE shall generate an interrupt.
3	TASK_CLEARED	R/W	0h	**Task Cleared Signal Enable (TCL)** When set and the MMCSD0_CQ_INTR_STS[3] TASK_CLEARED bit is asserted, the CQE shall generate an interrupt.
2	RESP_ERR_DET	R/W	0h	**Response Error Detected Signal Enable (RED)** When set and the MMCSD0_CQ_INTR_STS[2] RESP_ERR_DET bit is asserted, the CQE shall generate an interrupt.
1	TASK_COMPLETE	R/W	0h	**Task Complete Signal Enable (TCC)** When set and the MMCSD0_CQ_INTR_STS[1] TASK_COMPLETE bit is asserted, the CQE shall generate an interrupt.

Table 14-23913. MMCSD0_CQ_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_COMPLETE	R/W	0h	**Halt Complete Signal Enable (HAC)** When set and the MMCSD0_CQ_INTR_STS[0] HALT_COMPLETE bit is asserted, the CQE shall generate an interrupt.

83 MMCSD0_CQ_INTR_COALESCING Register (Offset = 21Ch) [reset = 0h]

MMCSD0_CQ_INTR_COALESCING is shown in Figure 14-7899 and described in Table 14-16017.

Return to Summary Table.

This register controls the interrupt coalescing feature.

Table 14-23914. MMCSD0_CQ_INTR_COALESCING Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 021Ch

Figure 14-7899. MMCSD0_CQ_INTR_COALESCING Register

31	30	29	28	27	26	25	24
CQINTCOALESC_ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED			IC_STATUS	RESERVED			
R-0h			R-0h	R-0h			
15	14	13	12	11	10	9	8
RESERVED			CTR_THRESHOLD				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED	TIMEOUT_VAL						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23916. MMCSD0_CQ_INTR_COALESCING Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CQINTCOALESC_ENABLE	R/W	0h	**Interrupt Coalescing Enable/Disable:** When set to 0h by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT = 1 in the Task Descriptor. When set to 1h, the interrupt coalescing mechanism is enabled and coalesced interrupts are generated.
30-21	RESERVED	R	0h	Reserved
20	IC_STATUS	R	0h	**Interrupt Coalescing Status Bit (ICSB):** This bit indicates to software whether any tasks (with INT = 0) have completed and counted towards interrupt coalescing (ICSB is set if and only if IC counter > 0). Bit Value Description 0h: No task completions have occurred since last counter reset (IC counter = 0) 1h: At least one task completion has been counted (IC counter > 0)
19-13	RESERVED	R	0h	Reserved

Table 14-23916. MMCSD0_CQ_INTR_COALESCING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	CTR_THRESHOLD	R/W	0h	**Interrupt Coalescing Counter Threshold (ICCTH):** Software uses this field to configure the number of task completions (only tasks with INT = 0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT = 0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31. **Note:** When ICCTH is 0h, task completions are not counted, and counting-based interrupts are not generated.
7	RESERVED	R	0h	Reserved
6-0	TIMEOUT_VAL	R/W	0h	**Interrupt Coalescing Timeout Value (ICTOVAL):** Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT = 0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timers unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field in the MMCSD0_CQ_CAPABILITIES register. The minimum value is 1h (1024 clock periods) and the maximum value is 7Fh (127 × 1024 clock periods). For example, a MMCSD0_CQ_CAPABILITIES field value of 0h indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is 16 × 1024 × 52.08 ns = 853.33 µs **Note:** When ICTOVAL is 0h, the timer is not running, and timer-based interrupts are not generated.

84 MMCSD0_CQ_TDL_BASE_ADDR Register (Offset = 220h) [reset = 0h]

MMCSD0_CQ_TDL_BASE_ADDR is shown in Figure 14-7900 and described in Table 14-16019.

Return to Summary Table.

This register is used for configuring the lower 32 bits of the byte address of the head of the Task 312 Descriptor List in the host memory.

Table 14-23917. MMCSD0_CQ_TDL_BASE_ADDR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0220h

Figure 14-7900. MMCSD0_CQ_TDL_BASE_ADDR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CQTDLBA_LO</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23919. MMCSD0_CQ_TDL_BASE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTDLBA_LO	R/W	0h	**Task Descriptor List Base Address (TDLBA)** This register stores the LSB bits (bits 31-0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 × (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on Byte1 KByte boundary. The lower 10 bits of this register shall be set to 0h by software and shall be ignored by CQE.

85 MMCSD0_CQ_TDL_BASE_ADDR_UPBITS Register (Offset = 224h) [reset = 0h]

MMCSD0_CQ_TDL_BASE_ADDR_UPBITS is shown in Figure 14-7901 and described in Table 14-16021.

Return to Summary Table.

This register is used for configuring the upper 32 bits of the byte address of the head of the Task 316 Descriptor List in the host memory.

Table 14-23920. MMCSD0_CQ_TDL_BASE_ADDR_UPBITS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0224h

Figure 14-7901. MMCSD0_CQ_TDL_BASE_ADDR_UPBITS Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CQTDLBA_HI</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23922. MMCSD0_CQ_TDL_BASE_ADDR_UPBITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTDLBA_HI	R/W	0h	**Task Descriptor List Base Address (TDLBA)** This register stores the MSB bits (bits 63-32) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 × (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This register is reserved when using 32-bit addressing mode.

86 MMCSD0_CQ_TASK_DOOR_BELL Register (Offset = 228h) [reset = 0h]

MMCSD0_CQ_TASK_DOOR_BELL is shown in Figure 14-7902 and described in Table 14-16023.

Return to Summary Table.

Using this register, software triggers CQE to process a new task.

Table 14-23923. MMCSD0_CQ_TASK_DOOR_BELL Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0228h

Figure 14-7902. MMCSD0_CQ_TASK_DOOR_BELL Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CQTDB_VAL</td></tr>
<tr><td colspan="32">W1S-0h</td></tr>
</table>

LEGEND: W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-23925. MMCSD0_CQ_TASK_DOOR_BELL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTDB_VAL	W1S	0h	**Command Queueing Task Doorbell** Software shall configure the MMCSD0_CQ_TDL_BASE_ADDR[31-0] CQTDLBA_LO and MMCSD0_CQ_TDL_BASE_ADDR_UPBITS[31-0] CQTDLBA_HI bit fields, and enable CQE in the MMCSD0_CQ_CONFIG register before using this register. Writing 1h to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by the MMCSD0_CQ_TASK_DOOR_BELL register write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0h by CQE in one of the following events: (a) When a task execution is completed (with success or error) (b) The task is cleared using MMCSD0_CQ_TASK_CLEAR register (c) All tasks are cleared using MMCSD0_CQ_CONTROL register (d) CQE is disabled using MMCSD0_CQ_CONFIG register Software may initiate multiple tasks at the same time (batch submission) by writing 1h to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order. Writing 0h by software shall have no impact on the hardware, and will not change the value of the register bit.

87 MMCSD0_CQ_TASK_COMP_NOTIF Register (Offset = 22Ch) [reset = 0h]

MMCSD0_CQ_TASK_COMP_NOTIF is shown in Figure 14-7903 and described in Table 14-16025.

Return to Summary Table.

This register is used by CQE to notify software about completed tasks.

Table 14-23926. MMCSD0_CQ_TASK_COMP_NOTIF Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 022Ch

Figure 14-7903. MMCSD0_CQ_TASK_COMP_NOTIF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTCN_VAL																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-23928. MMCSD0_CQ_TASK_COMP_NOTIF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTCN_VAL	R/W1C	0h	**Task Complete Notification** CQE shall set bit n of this register (at the same time it clears bit n of the MMCSD0_CQ_TASK_DOOR_BELL register) when a task execution is completed (with success or error). When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1h to the corresponding bits.

88 MMCSD0_CQ_DEV_QUEUE_STATUS Register (Offset = 230h) [reset = 0h]

MMCSD0_CQ_DEV_QUEUE_STATUS is shown in Figure 14-7904 and described in Table 14-16027.

Return to Summary Table.

This register stores the most recent value of the device's queue status.

Table 14-23929.
MMCSD0_CQ_DEV_QUEUE_STATUS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0230h

Figure 14-7904. MMCSD0_CQ_DEV_QUEUE_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQDQ_STS																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23931. MMCSD0_CQ_DEV_QUEUE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQDQ_STS	R	0h	**Device Queue Status** Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command (the device's queue status).

89 MMCSD0_CQ_DEV_PENDING_TASKS Register (Offset = 234h) [reset = 0h]

MMCSD0_CQ_DEV_PENDING_TASKS is shown in Figure 14-7905 and described in Table 14-16029.

Return to Summary Table.

This register indicates to software which tasks are queued in the device, awaiting execution.

Table 14-23932. MMCSD0_CQ_DEV_PENDING_TASKS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0234h

Figure 14-7905. MMCSD0_CQ_DEV_PENDING_TASKS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQDP_TSKS																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23934. MMCSD0_CQ_DEV_PENDING_TASKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQDP_TSKS	R	0h	**Device Pending Tasks** Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasnt been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using MMCSD0_CQ_CONTROL register.

90 MMCSD0_CQ_TASK_CLEAR Register (Offset = 238h) [reset = 0h]

MMCSD0_CQ_TASK_CLEAR is shown in Figure 14-7906 and described in Table 14-16031.

Return to Summary Table.

This register is used for removing an outstanding task in the CQE 327. The register should be used only when CQE is in Halt state.

Table 14-23935. MMCSD0_CQ_TASK_CLEAR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0238h

Figure 14-7906. MMCSD0_CQ_TASK_CLEAR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTCLR																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-23937. MMCSD0_CQ_TASK_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTCLR	R/W	0h	**Command Queueing Task Clear** Writing 1h to bit n of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in the MMCSD0_CQ_CONTROL register Halt bit. When software writes 1h to a bit in this register, CQE updates the value to 1h, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0h) in the MMCSD0_CQ_TASK_CLEAR and in MMCSD0_CQ_TASK_DOOR_BELL registers once clear operation is complete. Software should poll on the MMCSD0_CQ_TASK_CLEAR register until it is cleared to verify clear operation was complete. Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state. Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using MMCSD0_CQ_CONTROL register. Writing 0h to a register bit shall have no impact.

91 MMCSD0_CQ_SEND_STS_CONFIG1 Register (Offset = 240h) [reset = 11000h]

MMCSD0_CQ_SEND_STS_CONFIG1 is shown in Figure 14-7907 and described in Table 14-16033.

Return to Summary Table.

The register controls when the SEND_QUEUE_STATUS commands are sent.

Table 14-23938. MMCSD0_CQ_SEND_STS_CONFIG1 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0240h

Figure 14-7907. MMCSD0_CQ_SEND_STS_CONFIG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												CMD_BLK_CNTR			
R-0h												R/W-1h			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_IDLE_TIMER															
R/W-1000h															

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23940. MMCSD0_CQ_SEND_STS_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	CMD_BLK_CNTR	R/W	1h	**Send Status Command Block Counter** This field indicates to CQE when to send SEND_QUEUE_STATUS (CMD13) command to inquire the status of the devices task queue. A value of n means CQE shall send status command on the CMD line, during the transfer of data block **BLOCK_CNT-n**, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. A value of 0h means that SEND_QUEUE_STATUS (CMD13) command shall not be sent during the transaction. Instead it will be sent only when the data lines are idle. A value of 1 means that STATUS command is to be sent during the last block of the transaction.

Table 14-23940. MMCSD0_CQ_SEND_STS_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	CMD_IDLE_TIMER	R/W	1000h	**Send Status Command Idle Timer** This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of theclock whose frequency is specified in the Internal Timer Clock Frequency field in the MMCSD0_CQ_CAPABILITIES register. The minimum value is 1h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is: 4096 clock periods. For example, a MMCSD0_CQ_CAPABILITIES field value of 0h indicates a 19.2 MHz clock frequency (period = 52.08 ns).

92 MMCSD0_CQ_SEND_STS_CONFIG2 Register (Offset = 244h) [reset = 0h]

MMCSD0_CQ_SEND_STS_CONFIG2 is shown in Figure 14-7908 and described in Table 14-16035.

Return to Summary Table.

This register is used for 333 configuring RCA field in SEND_QUEUE_STATUS command argument.

Table 14-23941. MMCSD0_CQ_SEND_STS_CONFIG2 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0244h

Figure 14-7908. MMCSD0_CQ_SEND_STS_CONFIG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																QUEUE_RCA															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23943. MMCSD0_CQ_SEND_STS_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	QUEUE_RCA	R/W	0h	**Send Queue RCA** This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE shall copy this field to bits 31-16 of the argument when transmitting SEND_QUEUE_STATUS (CMD13) command.

93 MMCSD0_CQ_DCMD_RESPONSE Register (Offset = 248h) [reset = 0h]

MMCSD0_CQ_DCMD_RESPONSE is shown in Figure 14-7909 and described in Table 14-16037.

Return to Summary Table.

This register is used for passing the response of a DCMD task to software.

Table 14-23944. MMCSD0_CQ_DCMD_RESPONSE Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0248h

Figure 14-7909. MMCSD0_CQ_DCMD_RESPONSE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAST_RESP																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23946. MMCSD0_CQ_DCMD_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LAST_RESP	R	0h	**Direct Command Last Response** This register contains the response of the command generated by the last direct command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of the MMCSD0_CQ_TASK_DOOR_BELL register is cleared by CQE.

94 MMCSD0_CQ_RESP_ERR_MASK Register (Offset = 250h) [reset = FDF9A080h]

MMCSD0_CQ_RESP_ERR_MASK is shown in Figure 14-7910 and described in Table 14-16039.

Return to Summary Table.

This register controls the generation of Response Error Detection (RED) interrupt.

Table 14-23947. MMCSD0_CQ_RESP_ERR_MASK Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0250h

Figure 14-7910. MMCSD0_CQ_RESP_ERR_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQRMEM																															
R-FDF9A080h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23949. MMCSD0_CQ_RESP_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQRMEM	R	FDF9A080h	**Response Mode Error Mask** This bit is used as in interrupt mask on the device status field which is received in R1/R1b responses. Bit Value Description (for any bit i): 1h: When a R1/R1b response is received, with bit i in the device status set, a RED interrupt is generated 0h: When a R1/R1b response is received, bit i in the device status is ignored The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. **Note:** Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.

95 MMCSD0_CQ_TASK_ERR_INFO Register (Offset = 254h) [reset = 0h]

MMCSD0_CQ_TASK_ERR_INFO is shown in Figure 14-7911 and described in Table 14-16041.

Return to Summary Table.

This register is updated by CQE when an error occurs on data or command related to a task activity. When such error is detected by CQE or indicated by the eMMC controller CQE stores in the MMCSD0_CQ_TASK_ERR_INFO register the task IDs and the command indices of the commands which were executed on the 343 command line and data lines when the error occurred.

Software is expected to use this information in the error recovery procedure.

Table 14-23950. MMCSD0_CQ_TASK_ERR_INFO Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0254h

Figure 14-7911. MMCSD0_CQ_TASK_ERR_INFO Register

31	30	29	28	27	26	25	24
DATERR_VALID	RESERVED		DATERR_TASK_ID				
R-0h	R-0h		R-0h				
23	22	21	20	19	18	17	16
RESERVED		DATERR_CMD_INDEX					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RESP_MODE_VALID	RESERVED		RESP_MODE_TASK_ID				
R-0h	R-0h		R-0h				
7	6	5	4	3	2	1	0
RESERVED		RESP_MODE_CMD_INDEX					
R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23952. MMCSD0_CQ_TASK_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DATERR_VALID	R	0h	**Data Transfer Error Fields Valid** This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1h. If a no data transfer is in progress when the error is detected/ indicated, the bit is cleared to 0h.
30-29	RESERVED	R	0h	Reserved

Table 14-23952. MMCSD0_CQ_TASK_ERR_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	DATERR_TASK_ID	R	0h	**Data Transfer Error Task ID** This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23-22	RESERVED	R	0h	Reserved
21-16	DATERR_CMD_INDEX	R	0h	**Data Transfer Error Command Index** This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	RESP_MODE_VALID	R	0h	**Response Mode Error Fields Valid** This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1h. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0h.
14-13	RESERVED	R	0h	Reserved
12-8	RESP_MODE_TASK_ID	R	0h	**Response Mode Error Task ID** This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7-6	RESERVED	R	0h	Reserved
5-0	RESP_MODE_CMD_INDEX	R	0h	**Response Mode Error Command Index** This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

96 MMCSD0_CQ_CMD_RESP_INDEX Register (Offset = 258h) [reset = 0h]

MMCSD0_CQ_CMD_RESP_INDEX is shown in Figure 14-7912 and described in Table 14-16043.

Return to Summary Table.

This register stores the index of the last received command response.

Table 14-23953. MMCSD0_CQ_CMD_RESP_INDEX Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0258h

Figure 14-7912. MMCSD0_CQ_CMD_RESP_INDEX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										LAST_CRI					
R-0h										R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23955. MMCSD0_CQ_CMD_RESP_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	LAST_CRI	R	0h	**Last Command Response Index** This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

97 MMCSD0_CQ_CMD_RESP_ARG Register (Offset = 25Ch) [reset = 0h]

MMCSD0_CQ_CMD_RESP_ARG is shown in Figure 14-7913 and described in Table 14-16045.

Return to Summary Table.

This register stores the index of the last received command response.

Table 14-23956. MMCSD0_CQ_CMD_RESP_ARG Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 025Ch

Figure 14-7913. MMCSD0_CQ_CMD_RESP_ARG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">LAST_CRA</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23958. MMCSD0_CQ_CMD_RESP_ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LAST_CRA	R	0h	**Last Command Response Argument** This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

98 MMCSD0_CQ_ERROR_TASK_ID Register (Offset = 260h) [reset = 0h]

MMCSD0_CQ_ERROR_TASK_ID is shown in Figure 14-7914 and described in Table 14-16047.

Return to Summary Table.

CQ Error Task ID Register

Table 14-23959. MMCSD0_CQ_ERROR_TASK_ID Instances

Instance	Physical Address
MMCSD0_CTL_CFG	0FA1 0260h

Figure 14-7914. MMCSD0_CQ_ERROR_TASK_ID Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="11">RESERVED</td><td colspan="5">TERR_ID</td></tr>
<tr><td colspan="11">R-0h</td><td colspan="5">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23961. MMCSD0_CQ_ERROR_TASK_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	TERR_ID	R	0h	Task Error ID

14.9.3.6.5 MMCSD1 Subsystem Registers

Table 14-16049 lists the memory-mapped registers for the MMCSD1 Subsystem. All register offset addresses not listed in Table 14-16049 should be considered as reserved locations and the register contents should not be modified.

Table 14-23962. MMCSD1 Subsystem Instances

Instance	Base Address
MMCSD1_SS_CFG	0FA0 8000h

Table 14-23963. MMCSD1 Subsystem Registers

Offset	Acronym	Register Name	MMCSD1_SS_CFG Physical Address
0h	MMCSD1_SS_SS_ID_REV_REG	Subsystem ID and Revision Register	0FA0 8000h
10h	MMCSD1_SS_CTL_CFG_1_REG	Controller Config 1 Register	0FA0 8010h
14h	MMCSD1_SS_CTL_CFG_2_REG	Controller Config 2 Register	0FA0 8014h
18h	MMCSD1_SS_CTL_CFG_3_REG	Controller Config 3 Register	0FA0 8018h
1Ch	MMCSD1_SS_CTL_CFG_4_REG	Controller Config 4 Register	0FA0 801Ch
20h	MMCSD1_SS_CTL_CFG_5_REG	Controller Config 5 Register	0FA0 8020h
24h	MMCSD1_SS_CTL_CFG_6_REG	Controller Config 6 Register	0FA0 8024h
28h	MMCSD1_SS_CTL_CFG_7_REG	Controller Config 7 Register	0FA0 8028h
2Ch	MMCSD1_SS_CTL_CFG_8_REG	Controller Config 8 Register	0FA0 802Ch
30h	MMCSD1_SS_CTL_CFG_9_REG	Controller Config 9 Register	0FA0 8030h
34h	MMCSD1_SS_CTL_CFG_10_REG	Controller Config 10 Register	0FA0 8034h
38h	MMCSD1_SS_CTL_CFG_11_REG	Controller Config 11 Register	0FA0 8038h
3Ch	MMCSD1_SS_CTL_CFG_12_REG	Controller Config 12 Register	0FA0 803Ch
40h	MMCSD1_SS_CTL_CFG_13_REG	Controller Config 13 Register	0FA0 8040h
60h	MMCSD1_SS_CTL_STAT_1_REG	Controller Status 1 Register	0FA0 8060h
64h	MMCSD1_SS_CTL_STAT_2_REG	Controller Status 2 Register	0FA0 8064h
68h	MMCSD1_SS_CTL_STAT_3_REG	Controller Status 3 Register	0FA0 8068h
6Ch	MMCSD1_SS_CTL_STAT_4_REG	Controller Status 4 Register	0FA0 806Ch
70h	MMCSD1_SS_CTL_STAT_5_REG	Controller Status 5 Register	0FA0 8070h
74h	MMCSD1_SS_CTL_STAT_6_REG	Controller Status 6 Register	0FA0 8074h
100h	MMCSD1_SS_PHY_CTRL_1_REG	PHY Control 1 Register	0FA0 8100h
10Ch	MMCSD1_SS_PHY_CTRL_4_REG	PHY Control 4 Register	0FA0 810Ch
110h	MMCSD1_SS_PHY_CTRL_5_REG	PHY Control 5 Register	0FA0 8110h

1 MMCSD1_SS_SS_ID_REV_REG Register (Offset = 0h) [reset = 68403200h]

MMCSD1_SS_SS_ID_REV_REG is shown in Figure 14-7915 and described in Table 14-16051.

Return to Summary Table.

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem.

Table 14-23964. MMCSD1_SS_SS_ID_REV_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8000h

Figure 14-7915. MMCSD1_SS_SS_ID_REV_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_ID															
R-6840h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RTL_VER					MAJ_REV			CUSTOM		MIN_REV					
R-6h					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-23966. MMCSD1_SS_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MOD_ID	R	6840h	Module ID
15-11	RTL_VER	R	6h	RTL Version
10-8	MAJ_REV	R	2h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	MIN_REV	R	0h	Minor Revision

2 MMCSD1_SS_CTL_CFG_1_REG Register (Offset = 10h) [reset = 201030C8h]

MMCSD1_SS_CTL_CFG_1_REG is shown in Figure 14-7916 and described in Table 14-16053.

Return to Summary Table.

The Controller Config 1 Register contains various fields to control the configuration ports on the Host Controller.

Table 14-23967. MMCSD1_SS_CTL_CFG_1_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8010h

Figure 14-7916. MMCSD1_SS_CTL_CFG_1_REG Register

31	30	29	28	27	26	25	24
RESERVED		TUNINGCOUNT					
R-0h		R/W-20h					

23	22	21	20	19	18	17	16
RESERVED			ASYNCWKUPENA	RESERVED			
R-0h			R/W-1h	R-0h			

15	14	13	12	11	10	9	8
CQFMUL				RESERVED		CQFVAL	
R/W-3h				R-0h		R/W-C8h	

7	6	5	4	3	2	1	0
CQFVAL							
R/W-C8h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23969. MMCSD1_SS_CTL_CFG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	TUNINGCOUNT	R/W	20h	Configures the number of Taps (Phases) of the RX clock that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the RX clock during the Tuning Procedure.
23-21	RESERVED	R	0h	Reserved
20	ASYNCWKUPENA	R/W	1h	Determines the Wakeup Signal Generation Mode. 0h: Synchronous Wakeup Mode: The FCLK has to be running for this mode. The Card Insertion/Removal/Interrupt events are detected synchronously on the FCLK and the Wakeup event is generated. The Assertion and Deassertion of the Wakeup event signal synchronous to FCLK. 1h: Asyncrhonous Wakeup Mode: The FCLK and the ICLK can be stopped in this mode and the Wakeup event is asynchronously generated based on the Card Insertion/Removal/Interrupt events. The Assertion and Deassertion of the Wakeup event signal is asynchronous.

Table 14-23969. MMCSD1_SS_CTL_CFG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	RESERVED	R	0h	Reserved
15-12	CQFMUL	R/W	3h	FMUL for the CQ Internal Timer Clock Frequency
11-10	RESERVED	R	0h	Reserved
9-0	CQFVAL	R/W	C8h	FVAL for the CQ Internal Timer Clock Frequency

3 MMCSD1_SS_CTL_CFG_2_REG Register (Offset = 14h) [reset = 27E8C801h]

MMCSD1_SS_CTL_CFG_2_REG is shown in Figure 14-7917 and described in Table 14-16055.

Return to Summary Table.

The Controller Config 2 Register contains various fields to control the configuration ports on the Host Controller. This register sets the LSB fields in the MMCSD1_CAPABILITIES register inside the Host Controller.

Table 14-23970. MMCSD1_SS_CTL_CFG_2_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8014h

Figure 14-7917. MMCSD1_SS_CTL_CFG_2_REG Register

31	30	29	28	27	26	25	24
SLOTTYPE		ASYNCHINTRSUPPORT	RESERVED		SUPPORT1P8VOLT	SUPPORT3P0VOLT	SUPPORT3P3VOLT
R/W-0h		R/W-1h	R-0h		R/W-1h	R/W-1h	R/W-1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SUSPRESSUPPORT	SDMASUPPORT	HIGHSPEEDSUPPORT	RESERVED	ADMA2SUPPORT	SUPPORT8BIT	MAXBLKLENGTH	
R/W-1h	R/W-1h	R/W-1h	R-0h	R/W-1h	R/W-0h	R/W-0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASECLKFREQ							
R/W-C8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIMEOUTCLKUNIT	RESERVED	TIMEOUTCLKFREQ					
R/W-0h	R-0h	R/W-1h					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23972. MMCSD1_SS_CTL_CFG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SLOTTYPE	R/W	0h	Slot Type Should be set based on the final product usage. 0h: Removable SCard Slot 1h: Embedded Slot for One Device 2h: Shared Bus Slot 3h: Reserved
29	ASYNCHINTRSUPPORT	R/W	1h	Asynchronous Interrupt Support Suggested Value is 1h (The Core supports monitoring of Asynchronous Interrupt).
28-27	RESERVED	R	0h	Reserved
26	SUPPORT1P8VOLT	R/W	1h	1.8 V Support Suggested Value is 1h (The 1.8 Volt Switching is supported by Core). Optionally can be set to 0h if the application doesn't want 1.8 V switching (SD3.0).

Table 14-23972. MMCSD1_SS_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	SUPPORT3P0VOLT	R/W	1h	3.0 V Support Should be set based on whether 3.0 V is supported on the SD Interface.
24	SUPPORT3P3VOLT	R/W	1h	3.3 V Support Suggested Value is 1h as the 3.3 V is the default voltage on the SD Interface.
23	SUSPRESSUPPORT	R/W	1h	Suspend/Resume Support Suggested Value is 1h (The Suspend/Resume is supported by Core). Optionally can be set to 0h if the application doesn't want to support Suspend/Resume Mode.
22	SDMASUPPORT	R/W	1h	SDMA Support Suggested Value is 1h (The SDMA is supported by Core). Optionally can be set to 0h if the application doesn't want to support SDMA Mode.
21	HIGHSPEEDSUPPORT	R/W	1h	High Speed Support Suggested Value is 1h (The High Speed mode is supported by Core).
20	RESERVED	R	0h	Reserved
19	ADMA2SUPPORT	R/W	1h	ADMA2 Support Suggested Value is 1h (The ADMA2 is supported by Core). Optionally can be set to 0h if the application doesn't want to support ADMA2 Mode.
18	SUPPORT8BIT	R/W	0h	8-bit Support for Embedded Device Suggested Value is 1h (The Core supports 8-bit Interface). Optionally can be set to 0h if the application supports only 4-bit SD Interface.
17-16	MAXBLKLENGTH	R/W	0h	Max Block Length Maximum Block Length supported by the Core/Device. 0h: 512 Bytes 1h: 1024 Bytes 2h: 2048 Bytes 3h: Reserved
15-8	BASECLKFREQ	R/W	C8h	Base Clock Frequency for SD Clock This is the frequency of the FCLK.
7	TIMEOUTCLKUNIT	R/W	0h	Timeout Clock Unit Suggested Value is 0h (KHz).
6	RESERVED	R	0h	Reserved

Table 14-23972. MMCSD1_SS_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	TIMEOUTCLKFREQ	R/W	1h	Timeout Clock Frequency Suggested Value is 1 KHz. Internally the 1 ms Timer is used for Timeout Detection. The 1 ms Timer is generated from the FCLK.

4 MMCSD1_SS_CTL_CFG_3_REG Register (Offset = 18h) [reset = 18000407h]

MMCSD1_SS_CTL_CFG_3_REG is shown in Figure 14-7918 and described in Table 14-16057.

Return to Summary Table.

The Controller Config 3 Register contains various fields to control the configuration ports on the Host Controller. This register sets the MSB fields in the MMCSD1_CAPABILITIES register inside the Host Controller.

Table 14-23973. MMCSD1_SS_CTL_CFG_3_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8018h

Figure 14-7918. MMCSD1_SS_CTL_CFG_3_REG Register

31	30	29	28	27	26	25	24
RESERVED			SUPPORT1P8VDD2	ADMA3SUPPORT	RESERVED		
R-0h			R/W-1h	R/W-1h	R-0h		
23	22	21	20	19	18	17	16
CLOCKMULTIPLIER							
R/W-0h							
15	14	13	12	11	10	9	8
RETUNINGMODES		TUNINGFORSDR50	RESERVED	RETUNINGTIMERCNT			
R/W-0h		R/W-0h	R-0h	R/W-4h			
7	6	5	4	3	2	1	0
TYPE4SUPPORT	DDRIVERSUPPORT	CDRIVERSUPPORT	ADRIVERSUPPORT	RESERVED	DDR50SUPPORT	SDR104SUPPORT	SDR50SUPPORT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23975. MMCSD1_SS_CTL_CFG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	SUPPORT1P8VDD2	R/W	1h	1.8 V VDD2 Support
27	ADMA3SUPPORT	R/W	1h	ADMA3 Support
26-24	RESERVED	R	0h	Reserved

Table 14-23975. MMCSD1_SS_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	CLOCKMULTIPLIER	R/W	0h	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 0h means that the Host Controller does not support programmable clock generator. 0h: Clock Multiplier is Not Supported 1h: Clock Multiplier M = 2 2h: Clock Multiplier M = 3 ... FFh: Clock Multiplier M = 256
15-14	RETUNINGMODES	R/W	0h	Re-Tuning Modes Should be set to 2h as the Core supports only the Software Timer based Re-Tuning.
13	TUNINGFORSDR50	R/W	0h	Use Tuning for SDR50 This bit should be set if the application wants Tuning be used for SDR50 Modes. The Core operates with or without tuning for SDR50 mode as long as the Clock can be manually tuned using tap delay.
12	RESERVED	R	0h	Reserved
11-8	RETUNINGTIMERCNT	R/W	4h	Timer Count for Re-Tuning This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4h disables Re-Tuning Timer.
7	TYPE4SUPPORT	R/W	0h	Driver Type 4 Support This bit should be set based on whether Driver Type 4 for 1.8 Signalling is supported or not.
6	DDRIVERSUPPORT	R/W	0h	Driver Type D Support This bit should be set based on whether Driver Type D for 1.8 Signalling is supported or not.
5	CDRIVERSUPPORT	R/W	0h	Driver Type C Support This bit should be set based on whether Driver Type C for 1.8 Signalling is supported or not.
4	ADRIVERSUPPORT	R/W	0h	Driver Type A Support This bit should be set based on whether Driver Type A for 1.8 Signalling is supported or not.
3	RESERVED	R	0h	Reserved

Table 14-23975. MMCSD1_SS_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DDR50SUPPORT	R/W	1h	DDR50 Support Suggested Value is 1h (The Core supports DDR50 mode of operation). Optionally can be set to 0h if the application doesn't want to support DDR50.
1	SDR104SUPPORT	R/W	1h	SDR104 Support. Suggested Value is 1h (The Core supports SDR104 mode of operation). Optionally can be set to 0h if the application doesn't want to support SDR104.
0	SDR50SUPPORT	R/W	1h	SDR50 Support. Suggested Value is 1h (The Core supports SDR50 mode of operation). Optionally can be set to 0h if the application doesn't want to support SDR50.

5 MMCSD1_SS_CTL_CFG_4_REG Register (Offset = 1Ch) [reset = 0h]

MMCSD1_SS_CTL_CFG_4_REG is shown in Figure 14-7919 and described in Table 14-16059.

Return to Summary Table.

The Controller Config 4 Register contains various fields to control the configuration ports on the Host Controller. This register sets the LSB fields in the MMCSD1_MAX_CURRENT_CAP register inside the Host Controller.

Table 14-23976. MMCSD1_SS_CTL_CFG_4_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 801Ch

Figure 14-7919. MMCSD1_SS_CTL_CFG_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MAXCURRENT1P8V							
R-0h								R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAXCURRENT3P0V								MAXCURRENT3P3V							
R/W-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23978. MMCSD1_SS_CTL_CFG_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	MAXCURRENT1P8V	R/W	0h	Maximum Current For 1.8 V
15-8	MAXCURRENT3P0V	R/W	0h	Maximum Current For 3.0 V
7-0	MAXCURRENT3P3V	R/W	0h	Maximum Current For 3.3 V

6 MMCSD1_SS_CTL_CFG_5_REG Register (Offset = 20h) [reset = 0h]

MMCSD1_SS_CTL_CFG_5_REG is shown in Figure 14-7920 and described in Table 14-16061.

Return to Summary Table.

The Controller Config 5 Register contains various fields to control the configuration ports on the Host Controller. This register sets the MSB fields in the MMCSD1_MAX_CURRENT_CAP register inside the Host Controller.

Table 14-23979. MMCSD1_SS_CTL_CFG_5_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8020h

Figure 14-7920. MMCSD1_SS_CTL_CFG_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAXCURRENTVDD2							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23981. MMCSD1_SS_CTL_CFG_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MAXCURRENTVDD2	R/W	0h	Maximum Current For 1.8 V (VDD2)

7 MMCSD1_SS_CTL_CFG_6_REG Register (Offset = 24h) [reset = 100h]

MMCSD1_SS_CTL_CFG_6_REG is shown in Figure 14-7921 and described in Table 14-16063.

Return to Summary Table.

The Controller Config 6 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD0_PRESET_VALUE10) for Initialization inside the Host Controller.

Table 14-23982. MMCSD1_SS_CTL_CFG_6_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8024h

Figure 14-7921. MMCSD1_SS_CTL_CFG_6_REG Register

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
RESERVED	INITPRESETVAL
R-0h	R/W-100h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23984. MMCSD1_SS_CTL_CFG_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	INITPRESETVAL	R/W	100h	Preset Value For Initialization

8 MMCSD1_SS_CTL_CFG_7_REG Register (Offset = 28h) [reset = 4h]

MMCSD1_SS_CTL_CFG_7_REG is shown in Figure 14-7922 and described in Table 14-16065.

Return to Summary Table.

The Controller Config 7 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD0_PRESET_VALUE10) for Default Speed inside the Host Controller.

Table 14-23985. MMCSD1_SS_CTL_CFG_7_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8028h

Figure 14-7922. MMCSD1_SS_CTL_CFG_7_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			DSPDPRESETVAL												
R-0h																			R/W-4h												

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23987. MMCSD1_SS_CTL_CFG_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	DSPDPRESETVAL	R/W	4h	Preset Value For Default Speed

9 MMCSD1_SS_CTL_CFG_8_REG Register (Offset = 2Ch) [reset = 2h]

MMCSD1_SS_CTL_CFG_8_REG is shown in Figure 14-7923 and described in Table 14-16067.

Return to Summary Table.

The Controller Config 8 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD0_PRESET_VALUE10) for High Speed inside the Host Controller.

Table 14-23988. MMCSD1_SS_CTL_CFG_8_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 802Ch

Figure 14-7923. MMCSD1_SS_CTL_CFG_8_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSPDPRESETVAL												
R-0h																			R/W-2h												

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23990. MMCSD1_SS_CTL_CFG_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	HSPDPRESETVAL	R/W	2h	Preset Value For High Speed

10 MMCSD1_SS_CTL_CFG_9_REG Register (Offset = 30h) [reset = 4h]

MMCSD1_SS_CTL_CFG_9_REG is shown in Figure 14-7924 and described in Table 14-16069.

Return to Summary Table.

The Controller Config 9 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD0_PRESET_VALUE10) for SDR12 inside the Host Controller.

Table 14-23991. MMCSD1_SS_CTL_CFG_9_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8030h

Figure 14-7924. MMCSD1_SS_CTL_CFG_9_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			SDR12PRESETVAL												
R-0h			R/W-4h												

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23993. MMCSD1_SS_CTL_CFG_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR12PRESETVAL	R/W	4h	Preset Value For SDR12

11 MMCSD1_SS_CTL_CFG_10_REG Register (Offset = 34h) [reset = 2h]

MMCSD1_SS_CTL_CFG_10_REG is shown in Figure 14-7925 and described in Table 14-16071.

Return to Summary Table.

The Controller Config 10 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD0_PRESET_VALUE10) for SDR25 inside the Host Controller.

Table 14-23994. MMCSD1_SS_CTL_CFG_10_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8034h

Figure 14-7925. MMCSD1_SS_CTL_CFG_10_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SDR25PRESETVAL												
R-0h			R/W-2h												

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23996. MMCSD1_SS_CTL_CFG_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR25PRESETVAL	R/W	2h	Preset Value For SDR25

12 MMCSD1_SS_CTL_CFG_11_REG Register (Offset = 38h) [reset = 1h]

MMCSD1_SS_CTL_CFG_11_REG is shown in Figure 14-7926 and described in Table 14-16073.

Return to Summary Table.

The Controller Config 11 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD0_PRESET_VALUE10) for SDR50 inside the Host Controller.

Table 14-23997. MMCSD1_SS_CTL_CFG_11_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8038h

Figure 14-7926. MMCSD1_SS_CTL_CFG_11_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SDR50PRESETVAL												
R-0h			R/W-1h												

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-23999. MMCSD1_SS_CTL_CFG_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR50PRESETVAL	R/W	1h	Preset Value For SDR50

13 MMCSD1_SS_CTL_CFG_12_REG Register (Offset = 3Ch) [reset = 0h]

MMCSD1_SS_CTL_CFG_12_REG is shown in Figure 14-7927 and described in Table 14-16075.

Return to Summary Table.

The Controller Config 12 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD0_PRESET_VALUE10) for SDR104 inside the Host Controller.

Table 14-24000. MMCSD1_SS_CTL_CFG_12_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 803Ch

Figure 14-7927. MMCSD1_SS_CTL_CFG_12_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			SDR104PRESETVAL												
R-0h			R/W-0h												

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24002. MMCSD1_SS_CTL_CFG_12_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR104PRESETVAL	R/W	0h	Preset Value For SDR104

14 MMCSD1_SS_CTL_CFG_13_REG Register (Offset = 40h) [reset = 2h]

MMCSD1_SS_CTL_CFG_13_REG is shown in Figure 14-7928 and described in Table 14-16077.

Return to Summary Table.

The Controller Config 13 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD0_PRESET_VALUE10) for DDR50 inside the Host Controller.

Table 14-24003. MMCSD1_SS_CTL_CFG_13_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8040h

Figure 14-7928. MMCSD1_SS_CTL_CFG_13_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="13">DDR50PRESETVAL</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="13">R/W-2h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-24005. MMCSD1_SS_CTL_CFG_13_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	DDR50PRESETVAL	R/W	2h	Preset Value For DDR50

15 MMCSD1_SS_CTL_STAT_1_REG Register (Offset = 60h) [reset = 80000000h]

MMCSD1_SS_CTL_STAT_1_REG is shown in Figure 14-7929 and described in Table 14-16079.

Return to Summary Table.

The Controller Status 1 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-24006. MMCSD1_SS_CTL_STAT_1_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8060h

Figure 14-7929. MMCSD1_SS_CTL_STAT_1_REG Register

31	30	29	28	27	26	25	24
SDHC_CMDIDLE	RESERVED						
R-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMADEBUGBUS							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DMADEBUGBUS							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24008. MMCSD1_SS_CTL_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDHC_CMDIDLE	R	1h	Idle signal to enable software to gate off the clocks
30-16	RESERVED	R	0h	Reserved
15-0	DMADEBUGBUS	R	0h	DMA_CTRL Debug Bus

16 MMCSD1_SS_CTL_STAT_2_REG Register (Offset = 64h) [reset = 10h]

MMCSD1_SS_CTL_STAT_2_REG is shown in Figure 14-7930 and described in Table 14-16081.

Return to Summary Table.

The Controller Status 2 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-24009. MMCSD1_SS_CTL_STAT_2_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8064h

Figure 14-7930. MMCSD1_SS_CTL_STAT_2_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">CMDDEBUGBUS</td></tr>
<tr><td colspan="16">R-0h</td><td colspan="16">R-10h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24011. MMCSD1_SS_CTL_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CMDDEBUGBUS	R	10h	CMD_CTRL Debug Bus

17 MMCSD1_SS_CTL_STAT_3_REG Register (Offset = 68h) [reset = 0h]

MMCSD1_SS_CTL_STAT_3_REG is shown in Figure 14-7931 and described in Table 14-16083.

Return to Summary Table.

The Controller Status 3 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-24012. MMCSD1_SS_CTL_STAT_3_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8068h

Figure 14-7931. MMCSD1_SS_CTL_STAT_3_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TXDDEBUGBUS</td></tr>
<tr><td colspan="16">R-0h</td><td colspan="16">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24014. MMCSD1_SS_CTL_STAT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TXDDEBUGBUS	R	0h	TXD_CTRL Debug Bus

18 MMCSD1_SS_CTL_STAT_4_REG Register (Offset = 6Ch) [reset = 0h]

MMCSD1_SS_CTL_STAT_4_REG is shown in Figure 14-7932 and described in Table 14-16085.

Return to Summary Table.

The Controller Status 4 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-24015. MMCSD1_SS_CTL_STAT_4_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 806Ch

Figure 14-7932. MMCSD1_SS_CTL_STAT_4_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">RXDDEBUGBUS0</td></tr>
<tr><td colspan="16">R-0h</td><td colspan="16">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-24017. MMCSD1_SS_CTL_STAT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RXDDEBUGBUS0	R	0h	RXD_CTRL Debug Bus (SD CLK)

19 MMCSD1_SS_CTL_STAT_5_REG Register (Offset = 70h) [reset = 8h]

MMCSD1_SS_CTL_STAT_5_REG is shown in Figure 14-7933 and described in Table 14-16087.

Return to Summary Table.

The Controller Status 5 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-24018. MMCSD1_SS_CTL_STAT_5_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8070h

Figure 14-7933. MMCSD1_SS_CTL_STAT_5_REG Register

31-16	15-0
RESERVED	RXDDEBUGBUS1
R-0h	R-8h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24020. MMCSD1_SS_CTL_STAT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RXDDEBUGBUS1	R	8h	RXD_CTRL Debug Bus (RX CLK)

20 MMCSD1_SS_CTL_STAT_6_REG Register (Offset = 74h) [reset = 0h]

MMCSD1_SS_CTL_STAT_6_REG is shown in Figure 14-7934 and described in Table 14-16089.

Return to Summary Table.

The Controller Status 6 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 14-24021. MMCSD1_SS_CTL_STAT_6_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8074h

Figure 14-7934. MMCSD1_SS_CTL_STAT_6_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">TUNDEBUGBUS</td></tr>
<tr><td colspan="16">R-0h</td><td colspan="16">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-24023. MMCSD1_SS_CTL_STAT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TUNDEBUGBUS	R	0h	TUN_CTRL Debug Bus

21 MMCSD1_SS_PHY_CTRL_1_REG Register (Offset = 100h) [reset = 80010000h]

MMCSD1_SS_PHY_CTRL_1_REG is shown in Figure 14-7935 and described in Table 14-16091.

Return to Summary Table.

The PHY Control 1 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-24024. MMCSD1_SS_PHY_CTRL_1_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8100h

Figure 14-7935. MMCSD1_SS_PHY_CTRL_1_REG Register

31	30	29	28	27	26	25	24
IOMUX_ENABLE	RESERVED						
R/W-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24026. MMCSD1_SS_PHY_CTRL_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IOMUX_ENABLE	R/W	1h	IO Mux Enable Set 1h for GPIO. Set 0h for MMCSD.
30-0	RESERVED	R	0h	Reserved

22 MMCSD1_SS_PHY_CTRL_4_REG Register (Offset = 10Ch) [reset = 0h]

MMCSD1_SS_PHY_CTRL_4_REG is shown in Figure 14-7936 and described in Table 14-16093.

Return to Summary Table.

The PHY Control 4 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-24027. MMCSD1_SS_PHY_CTRL_4_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 810Ch

Figure 14-7936. MMCSD1_SS_PHY_CTRL_4_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			OTAPDLYENA	RESERVED			
R-0h			R/W-0h	R-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OTAPDLYSEL				RESERVED		ITAPCHGWIN	ITAPDLYENA
R/W-0h				R-0h		R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ITAPDLYSEL				
R-0h			R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24029. MMCSD1_SS_PHY_CTRL_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20	OTAPDLYENA	R/W	0h	Output Tap Delay Enable Enables manual control of the TX clock tap delay, for clocking the final stage flops for maintaining Hold requirements on EMMC Interface.
19-16	RESERVED	R	0h	Reserved
15-12	OTAPDLYSEL	R/W	0h	Output Tap Delay Select Manual control of the TX clock tap delay for clocking the final stage flops for maintaining Hold requirements on EMMC Interface.
11-10	RESERVED	R	0h	Reserved
9	ITAPCHGWIN	R/W	0h	Input Tap Change Window It gets asserted by the controller while changing the itapdlysel. Used to gate of the RX clock during switching the clock source while tap is changing to avoid clock glitches.

Table 14-24029. MMCSD1_SS_PHY_CTRL_4_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ITAPDLYENA	R/W	0h	Input Tap Delay Enable This is used for the manual control of the RX clock Tap Delay in non HS200/HS400 modes.
7-5	RESERVED	R	0h	Reserved
4-0	ITAPDLYSEL	R/W	0h	Input Tap Delay Select Manual control of the RX clock Tap Delay in the non HS200/HS400 modes.

23 MMCSD1_SS_PHY_CTRL_5_REG Register (Offset = 110h) [reset = 0h]

MMCSD1_SS_PHY_CTRL_5_REG is shown in Figure 14-7937 and described in Table 14-16095.

Return to Summary Table.

The PHY Control 5 Register contains various fields to control the ports on the Host Controller PHY.

Table 14-24030. MMCSD1_SS_PHY_CTRL_5_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	0FA0 8110h

Figure 14-7937. MMCSD1_SS_PHY_CTRL_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RESERVED		
R-0h													R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24032. MMCSD1_SS_PHY_CTRL_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	RESERVED	R/W	0h	Reserved

14.9.3.6.6 MMCSD1 RX RAM ECC Aggregator Registers

Table 14-16097 lists the memory-mapped registers for the MMCSD1 RX RAM ECC Aggregator. All register offset addresses not listed in Table 14-16097 should be considered as reserved locations and the register contents should not be modified.

Table 14-24033. MMCSD1 RX RAM ECC Aggregator Instances

Instance	Base Address
MMCSD1_ECC_AGGR_RXMEM	0070 8000h

Table 14-24034. MMCSD1 RX RAM ECC Aggregator Registers

Offset	Acronym	Register Name	MMCSD1_ECC_AGGR_RXMEM Physical Address
0h	MMCSD1_RXECC_REV	Aggregator Revision Register	0070 8000h
8h	MMCSD1_RXECC_VECTOR	ECC Vector Register	0070 8008h
Ch	MMCSD1_RXECC_STAT	Misc Status Register	0070 800Ch
3Ch	MMCSD1_RXECC_SEC_EOI_REG	SEC EOI Register	0070 803Ch
40h	MMCSD1_RXECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	0070 8040h
80h	MMCSD1_RXECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	0070 8080h
C0h	MMCSD1_RXECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	0070 80C0h
13Ch	MMCSD1_RXECC_DED_EOI_REG	DED EOI Register	0070 813Ch
140h	MMCSD1_RXECC_DED_STATUS_REG0	DED Interrupt Status Register 0	0070 8140h
180h	MMCSD1_RXECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	0070 8180h
1C0h	MMCSD1_RXECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	0070 81C0h
200h	MMCSD1_RXECC_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	0070 8200h
204h	MMCSD1_RXECC_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	0070 8204h
208h	MMCSD1_RXECC_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	0070 8208h
20Ch	MMCSD1_RXECC_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	0070 820Ch

1 MMCSD1_RXECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MMCSD1_RXECC_REV is shown in Figure 14-7938 and described in Table 14-16099.

Return to Summary Table.

Aggregator Revision Register

Revision parameters.

Table 14-24035. MMCSD1_RXECC_REV Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8000h

Figure 14-7938. MMCSD1_RXECC_REV Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="12">MODULE_ID</td></tr>
<tr><td colspan="2">R-1h</td><td colspan="2">R-2h</td><td colspan="12">R-6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="5">R-1Dh</td><td colspan="3">R-2h</td><td colspan="2">R-0h</td><td colspan="6">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24037. MMCSD1_RXECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

2 MMCSD1_RXECC_VECTOR Register (Offset = 8h) [reset = 0h]

MMCSD1_RXECC_VECTOR is shown in Figure 14-7939 and described in Table 14-16101.

Return to Summary Table.

ECC Vector Register

Table 14-24038. MMCSD1_RXECC_VECTOR Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8008h

Figure 14-7939. MMCSD1_RXECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R-0h							R/W1C-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24040. MMCSD1_RXECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

3 MMCSD1_RXECC_STAT Register (Offset = Ch) [reset = 1h]

MMCSD1_RXECC_STAT is shown in Figure 14-7940 and described in Table 14-16103.

Return to Summary Table.

Misc Status Register

Table 14-24041. MMCSD1_RXECC_STAT Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 800Ch

Figure 14-7940. MMCSD1_RXECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-0h																					R-1h										

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24043. MMCSD1_RXECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

4 MMCSD1_RXECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MMCSD1_RXECC_SEC_EOI_REG is shown in Figure 14-7941 and described in Table 14-16105.

Return to Summary Table.

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-24044. MMCSD1_RXECC_SEC_EOI_REG Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 803Ch

Figure 14-7941. MMCSD1_RXECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24046. MMCSD1_RXECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	SEC EOI

5 MMCSD1_RXECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MMCSD1_RXECC_SEC_STATUS_REG0 is shown in Figure 14-7942 and described in Table 14-16107.

Return to Summary Table.

SEC Interrupt Status Register 0

Table 14-24047. MMCSD1_RXECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8040h

Figure 14-7942. MMCSD1_RXECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24049. MMCSD1_RXECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_PEND	R/W1S	0h	Interrupt Pending Status for rxmem_pend

6 MMCSD1_RXECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MMCSD1_RXECC_SEC_ENABLE_SET_REG0 is shown in Figure 14-7943 and described in Table 14-16109.

Return to Summary Table.

SEC Interrupt Enable Set Register 0

Table 14-24050. MMCSD1_RXECC_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8080h

Figure 14-7943. MMCSD1_RXECC_SEC_ENABLE_SET_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>RXMEM_ENABLE_SET</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24052. MMCSD1_RXECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for rxmem_pend

7 MMCSD1_RXECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MMCSD1_RXECC_SEC_ENABLE_CLR_REG0 is shown in Figure 14-7944 and described in Table 14-16111.

Return to Summary Table.

SEC Interrupt Enable Clear Register 0

Table 14-24053. MMCSD1_RXECC_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 80C0h

Figure 14-7944. MMCSD1_RXECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-24055. MMCSD1_RXECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for rxmem_pend

8 MMCSD1_RXECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MMCSD1_RXECC_DED_EOI_REG is shown in Figure 14-7945 and described in Table 14-16113.

Return to Summary Table.

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-24056. MMCSD1_RXECC_DED_EOI_REG Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 813Ch

Figure 14-7945. MMCSD1_RXECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24058. MMCSD1_RXECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	DED EOI

9 MMCSD1_RXECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MMCSD1_RXECC_DED_STATUS_REG0 is shown in Figure 14-7946 and described in Table 14-16115.

Return to Summary Table.

DED Interrupt Status Register 0

Table 14-24059. MMCSD1_RXECC_DED_STATUS_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8140h

Figure 14-7946. MMCSD1_RXECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							RXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24061. MMCSD1_RXECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_PEND	R/W1S	0h	Interrupt Pending Status for rxmem_pend

10 MMCSD1_RXECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MMCSD1_RXECC_DED_ENABLE_SET_REG0 is shown in Figure 14-7947 and described in Table 14-16117.

Return to Summary Table.

DED Interrupt Enable Set Register 0

Table 14-24062. MMCSD1_RXECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8180h

Figure 14-7947. MMCSD1_RXECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-24064. MMCSD1_RXECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for rxmem_pend

11 MMCSD1_RXECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MMCSD1_RXECC_DED_ENABLE_CLR_REG0 is shown in Figure 14-7948 and described in Table 14-16119.

Return to Summary Table.

DED Interrupt Enable Clear Register 0

Table 14-24065. MMCSD1_RXECC_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 81C0h

Figure 14-7948. MMCSD1_RXECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-24067. MMCSD1_RXECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for rxmem_pend

12 MMCSD1_RXECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MMCSD1_RXECC_AGGR_ENABLE_SET is shown in Figure 14-7949 and described in Table 14-16121.

Return to Summary Table.

Aggregator Interrupt Enable Set Register

Table 14-24068. MMCSD1_RXECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8200h

Figure 14-7949. MMCSD1_RXECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24070. MMCSD1_RXECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

13 MMCSD1_RXECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MMCSD1_RXECC_AGGR_ENABLE_CLR is shown in Figure 14-7950 and described in Table 14-16123.

Return to Summary Table.

Aggregator Interrupt Enable Clear Register

Table 14-24071. MMCSD1_RXECC_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8204h

Figure 14-7950. MMCSD1_RXECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-24073. MMCSD1_RXECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

14 MMCSD1_RXECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MMCSD1_RXECC_AGGR_STATUS_SET is shown in Figure 14-7951 and described in Table 14-16125.

Return to Summary Table.

Aggregator Interrupt Status Set Register

Table 14-24074. MMCSD1_RXECC_AGGR_STATUS_SET Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 8208h

Figure 14-7951. MMCSD1_RXECC_AGGR_STATUS_SET Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -*n* = value after reset

Table 14-24076. MMCSD1_RXECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

15 MMCSD1_RXECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MMCSD1_RXECC_AGGR_STATUS_CLR is shown in Figure 14-7952 and described in Table 14-16127.

Return to Summary Table.

Aggregator Interrupt Status Clear Register

Table 14-24077. MMCSD1_RXECC_AGGR_STATUS_CLR Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	0070 820Ch

Figure 14-7952. MMCSD1_RXECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; *-n* = value after reset

Table 14-24079. MMCSD1_RXECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

14.9.3.6.7 MMCSD1 TX RAM ECC Aggregator Registers

Table 14-16129 lists the memory-mapped registers for the MMCSD1 TX RAM ECC Aggregator. All register offset addresses not listed in Table 14-16129 should be considered as reserved locations and the register contents should not be modified.

Table 14-24080. MMCSD1 TX RAM ECC Aggregator Instances

Instance	Base Address
MMCSD1_ECC_AGGR_TXMEM	0070 9000h

Table 14-24081. MMCSD1 TX RAM ECC Aggregator Registers

Offset	Acronym	Register Name	MMCSD1_ECC_AGGR_TXMEM Physical Address
0h	MMCSD1_TXECC_REV	Aggregator Revision Register	0070 9000h
8h	MMCSD1_TXECC_VECTOR	ECC Vector Register	0070 9008h
Ch	MMCSD1_TXECC_STAT	Misc Status Register	0070 900Ch
3Ch	MMCSD1_TXECC_SEC_EOI_REG	SEC EOI Register	0070 903Ch
40h	MMCSD1_TXECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	0070 9040h
80h	MMCSD1_TXECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	0070 9080h
C0h	MMCSD1_TXECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	0070 90C0h
13Ch	MMCSD1_TXECC_DED_EOI_REG	DED EOI Register	0070 913Ch
140h	MMCSD1_TXECC_DED_STATUS_REG0	DED Interrupt Status Register 0	0070 9140h
180h	MMCSD1_TXECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	0070 9180h
1C0h	MMCSD1_TXECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	0070 91C0h
200h	MMCSD1_TXECC_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	0070 9200h
204h	MMCSD1_TXECC_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	0070 9204h
208h	MMCSD1_TXECC_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	0070 9208h
20Ch	MMCSD1_TXECC_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	0070 920Ch

1 MMCSD1_TXECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MMCSD1_TXECC_REV is shown in Figure 14-7953 and described in Table 14-16131.

Return to Summary Table.

Aggregator Revision Register

Revision parameters.

Table 14-24082. MMCSD1_TXECC_REV Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9000h

Figure 14-7953. MMCSD1_TXECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 14-24084. MMCSD1_TXECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

2 MMCSD1_TXECC_VECTOR Register (Offset = 8h) [reset = 0h]

MMCSD1_TXECC_VECTOR is shown in Figure 14-7954 and described in Table 14-16133.

Return to Summary Table.

ECC Vector Register

Table 14-24085. MMCSD1_TXECC_VECTOR Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9008h

Figure 14-7954. MMCSD1_TXECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24087. MMCSD1_TXECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

3 MMCSD1_TXECC_STAT Register (Offset = Ch) [reset = 1h]

MMCSD1_TXECC_STAT is shown in Figure 14-7955 and described in Table 14-16135.

Return to Summary Table.

Misc Status Register

Table 14-24088. MMCSD1_TXECC_STAT Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 900Ch

Figure 14-7955. MMCSD1_TXECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-0h																					R-1h										

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24090. MMCSD1_TXECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

4 MMCSD1_TXECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MMCSD1_TXECC_SEC_EOI_REG is shown in Figure 14-7956 and described in Table 14-16137.

Return to Summary Table.

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-24091. MMCSD1_TXECC_SEC_EOI_REG Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 903Ch

Figure 14-7956. MMCSD1_TXECC_SEC_EOI_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24093. MMCSD1_TXECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	SEC EOI

5 MMCSD1_TXECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MMCSD1_TXECC_SEC_STATUS_REG0 is shown in Figure 14-7957 and described in Table 14-16139.

Return to Summary Table.

SEC Interrupt Status Register 0

Table 14-24094. MMCSD1_TXECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9040h

Figure 14-7957. MMCSD1_TXECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24096. MMCSD1_TXECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_PEND	R/W1S	0h	Interrupt Pending Status for txmem_pend

6 MMCSD1_TXECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MMCSD1_TXECC_SEC_ENABLE_SET_REG0 is shown in Figure 14-7958 and described in Table 14-16141.

Return to Summary Table.

SEC Interrupt Enable Set Register 0

Table 14-24097. MMCSD1_TXECC_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9080h

Figure 14-7958. MMCSD1_TXECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-24099. MMCSD1_TXECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for txmem_pend

7 MMCSD1_TXECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MMCSD1_TXECC_SEC_ENABLE_CLR_REG0 is shown in Figure 14-7959 and described in Table 14-16143.

Return to Summary Table.

SEC Interrupt Enable Clear Register 0

Table 14-24100. MMCSD1_TXECC_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 90C0h

Figure 14-7959. MMCSD1_TXECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-24102. MMCSD1_TXECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for txmem_pend

8 MMCSD1_TXECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MMCSD1_TXECC_DED_EOI_REG is shown in Figure 14-7960 and described in Table 14-16145.

Return to Summary Table.

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-24103. MMCSD1_TXECC_DED_EOI_REG Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 913Ch

Figure 14-7960. MMCSD1_TXECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24105. MMCSD1_TXECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	DED EOI

9 MMCSD1_TXECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MMCSD1_TXECC_DED_STATUS_REG0 is shown in Figure 14-7961 and described in Table 14-16147.

Return to Summary Table.

DED Interrupt Status Register 0

Table 14-24106.
MMCSD1_TXECC_DED_STATUS_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9140h

Figure 14-7961. MMCSD1_TXECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24108. MMCSD1_TXECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_PEND	R/W1S	0h	Interrupt Pending Status for txmem_pend

10 MMCSD1_TXECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MMCSD1_TXECC_DED_ENABLE_SET_REG0 is shown in Figure 14-7962 and described in Table 14-16149.

Return to Summary Table.

DED Interrupt Enable Set Register 0

Table 14-24109. MMCSD1_TXECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9180h

Figure 14-7962. MMCSD1_TXECC_DED_ENABLE_SET_REG0 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TXMEM_ENABLE_SET</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W1S-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24111. MMCSD1_TXECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for txmem_pend

11 MMCSD1_TXECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MMCSD1_TXECC_DED_ENABLE_CLR_REG0 is shown in Figure 14-7963 and described in Table 14-16151.

Return to Summary Table.

DED Interrupt Enable Clear Register 0

Table 14-24112. MMCSD1_TXECC_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 91C0h

Figure 14-7963. MMCSD1_TXECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-24114. MMCSD1_TXECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for txmem_pend

12 MMCSD1_TXECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MMCSD1_TXECC_AGGR_ENABLE_SET is shown in Figure 14-7964 and described in Table 14-16153.

Return to Summary Table.

Aggregator Interrupt Enable Set Register

Table 14-24115.
MMCSD1_TXECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9200h

Figure 14-7964. MMCSD1_TXECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-24117. MMCSD1_TXECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

13 MMCSD1_TXECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MMCSD1_TXECC_AGGR_ENABLE_CLR is shown in Figure 14-7965 and described in Table 14-16155.

Return to Summary Table.

Aggregator Interrupt Enable Clear Register

Table 14-24118. MMCSD1_TXECC_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9204h

Figure 14-7965. MMCSD1_TXECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-24120. MMCSD1_TXECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

14 MMCSD1_TXECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MMCSD1_TXECC_AGGR_STATUS_SET is shown in Figure 14-7966 and described in Table 14-16157.

Return to Summary Table.

Aggregator Interrupt Status Set Register

Table 14-24121. MMCSD1_TXECC_AGGR_STATUS_SET Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 9208h

Figure 14-7966. MMCSD1_TXECC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -*n* = value after reset

Table 14-24123. MMCSD1_TXECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

15 MMCSD1_TXECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MMCSD1_TXECC_AGGR_STATUS_CLR is shown in Figure 14-7967 and described in Table 14-16159.

Return to Summary Table.

Aggregator Interrupt Status Clear Register

Table 14-24124. MMCSD1_TXECC_AGGR_STATUS_CLR Instances

Instance	Physical Address
MMCSD1_ECC_AGGR_TXMEM	0070 920Ch

Figure 14-7967. MMCSD1_TXECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -*n* = value after reset

Table 14-24126. MMCSD1_TXECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

14.9.3.6.8 MMCSD1 Host Controller Registers

Table 14-16161 lists the memory-mapped registers for the MMCSD1 Host Controller. All register offset addresses not listed in Table 14-16161 should be considered as reserved locations and the register contents should not be modified.

Note

UHSII is not supported. For more information, see *Not Supported Features*.

Table 14-24127. MMCSD1 HOST CONTROLLER Instances

Instance	Base Address
MMCSD1_CTL_CFG	0FA0 0000h

Table 14-24128. MMCSD1 Host Controller Registers

Offset	Acronym	Register Name	MMCSD1_CTL_CFG Physical Address
		Host Controller Interface Register	
0h	MMCSD1_SDMA_SYS_ADDR_LO	32-bit Block Count/SDMA System Address Low Register	0FA0 0000h
2h	MMCSD1_SDMA_SYS_ADDR_HI	32-bit Block Count/SDMA System Address High Register	0FA0 0002h
4h	MMCSD1_BLOCK_SIZE	16-bit Block Size Register	0FA0 0004h
6h	MMCSD1_BLOCK_COUNT	16-bit Block Count Register	0FA0 0006h
8h	MMCSD1_ARGUMENT1_LO	Argument1 Low Register	0FA0 0008h
Ah	MMCSD1_ARGUMENT1_HI	Argument1 High Register	0FA0 000Ah
Ch	MMCSD1_TRANSFER_MODE	Transfer Mode Register	0FA0 000Ch
Eh	MMCSD1_COMMAND	Command Register	0FA0 000Eh
10h to 1Eh	MMCSD1_RESPONSE_0 to MMCSD1_RESPONSE_7	Response Register	0FA0 0010h to 0FA0 001Eh
20h	MMCSD1_DATA_PORT	Buffer Data Port Register	0FA0 0020h
24h	MMCSD1_PRESENTSTATE	Present State Register	0FA0 0024h
28h	MMCSD1_HOST_CONTROL1	Host Control 1 Register	0FA0 0028h
29h	MMCSD1_POWER_CONTROL	Power Control Register	0FA0 0029h
2Ah	MMCSD1_BLOCK_GAP_CONTROL	Block Gap Control Register	0FA0 002Ah
2Bh	MMCSD1_WAKEUP_CONTROL	Wakeup Control Register	0FA0 002Bh
2Ch	MMCSD1_CLOCK_CONTROL	Clock Control Register	0FA0 002Ch
2Eh	MMCSD1_TIMEOUT_CONTROL	Timeout Control Register	0FA0 002Eh
2Fh	MMCSD1_SOFTWARE_RESET	Software Reset Register	0FA0 002Fh
30h	MMCSD1_NORMAL_INTR_STS	Normal Interrupt Status Register	0FA0 0030h
32h	MMCSD1_ERROR_INTR_STS	Error Interrupt Status Register	0FA0 0032h
34h	MMCSD1_NORMAL_INTR_STS_ENA	Normal Interrupt Status Enable Register	0FA0 0034h
36h	MMCSD1_ERROR_INTR_STS_ENA	Error Interrupt Status Enable Register	0FA0 0036h
38h	MMCSD1_NORMAL_INTR_SIG_ENA	Normal Interrupt Signal Enable Register	0FA0 0038h
3Ah	MMCSD1_ERROR_INTR_SIG_ENA	Error Interrupt Signal Enable Register	0FA0 003Ah
3Ch	MMCSD1_AUTOCMD_ERR_STS	Auto CMD Error Status Register	0FA0 003Ch
3Eh	MMCSD1_HOST_CONTROL2	Host Control 2 Register	0FA0 003Eh
40h	MMCSD1_CAPABILITIES	Capabilities Register	0FA0 0040h
48h	MMCSD1_MAX_CURRENT_CAP	Maximum Current Capabilities Register	0FA0 0048h
50h	MMCSD1_FORCE_EVNT_ACMD_ERR_STS	Force Event Register for Auto CMD Error Status	0FA0 0050h

Table 14-24128. MMCSD1 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCSD1_CTL_CFG Physical Address
52h	MMCSD1_FORCE_EVNT_ERR_INT_STS	Force Event Register for Error Interrupt Status	0FA0 0052h
54h	MMCSD1_ADMA_ERR_STATUS	ADMA Error Status Register	0FA0 0054h
58h	MMCSD1_ADMA_SYS_ADDRESS	ADMA System Address Register	0FA0 0058h
60h	MMCSD1_PRESET_VALUE0	Preset Values 0 Register	0FA0 0060h
62h	MMCSD1_PRESET_VALUE1	Preset Values 1 Register	0FA0 0062h
64h	MMCSD1_PRESET_VALUE2	Preset Values 2 Register	0FA0 0064h
66h	MMCSD1_PRESET_VALUE3	Preset Values 3 Register	0FA0 0066h
68h	MMCSD1_PRESET_VALUE4	Preset Values 4 Register	0FA0 0068h
6Ah	MMCSD1_PRESET_VALUE5	Preset Values 5 Register	0FA0 006Ah
6Ch	MMCSD1_PRESET_VALUE6	Preset Values 6 Register	0FA0 006Ch
6Eh	MMCSD1_PRESET_VALUE7	Preset Values 7 Register	0FA0 006Eh
72h	MMCSD1_PRESET_VALUE8	Preset Values 8 Register	0FA0 0072h
74h	MMCSD1_PRESET_VALUE10	Preset Values 10 Register	0FA0 0074h
78h	MMCSD1_ADMA3_DESC_ADDRESS	ADMA3 Integrated Descriptor Address Register	0FA0 0078h
		UHS-II Registers (1)	
80h	MMCSD1_UHS2_BLOCK_SIZE	UHS-II Block Size Register	0FA0 0080h
84h	MMCSD1_UHS2_BLOCK_COUNT	UHS-II Block Count Register	0FA0 0084h
88h to 9Bh	MMCSD1_UHS2_COMMAND_PKT_0 to MMCSD1_UHS2_COMMAND_PKT_19	UHS-II Command Packet Register	0FA0 0088h to 0FA0 009Bh
9Ch	MMCSD1_UHS2_XFER_MODE	UHS-II Transfer Mode Register	0FA0 009Ch
9Eh	MMCSD1_UHS2_COMMAND	UHS-II Command Register	0FA0 009Eh
A0h to B3h	MMCSD1_UHS2_RESPONSE_0 to MMCSD1_UHS2_RESPONSE_19	UHS-II Response Register	0FA0 00A0h to 0FA0 00B3h
B4h	MMCSD1_UHS2_MESSAGE_SELECT	UHS-II Message Select Register	0FA0 00B4h
B8h	MMCSD1_UHS2_MESSAGE	UHS-II Message Register	0FA0 00B8h
BCh	MMCSD1_UHS2_DEVICE_INTR_STATUS	UHS-II Device Interrupt Status Register	0FA0 00BCh
BEh	MMCSD1_UHS2_DEVICE_SELECT	UHS-II Device Select Register	0FA0 00BEh
BFh	MMCSD1_UHS2_DEVICE_INT_CODE	UHS-II Device Interrupt Code Register	0FA0 00BFh
C0h	MMCSD1_UHS2_SOFTWARE_RESET	UHS-II Software Reset Register	0FA0 00C0h
C2h	MMCSD1_UHS2_TIMER_CONTROL	UHS-II Timeout Control Register	0FA0 00C2h
C4h	MMCSD1_UHS2_ERR_INTR_STS	UHS-II Error Interrupt Status Register	0FA0 00C4h
C8h	MMCSD1_UHS2_ERR_INTR_STS_ENA	UHS-II Error Interrupt Status Enable Register	0FA0 00C8h
CCh	MMCSD1_UHS2_ERR_INTR_SIG_ENA	UHS-II Error Interrupt Signal Enable Register	0FA0 00CCh
E0h	MMCSD1_UHS2_SETTINGS_PTR	Pointer for UHS-II Settings Register	0FA0 00E0h
E2h	MMCSD1_UHS2_CAPABILITIES_PTR	Pointer for UHS-II Host Capabilities Register	0FA0 00E2h
E4h	MMCSD1_UHS2_TEST_PTR	Pointer for UHS-II Test Register	0FA0 00E4h
E6h	MMCSD1_SHARED_BUS_CTRL_PTR	Pointer for Embedded Control Register	0FA0 00E6h
E8h	MMCSD1_VENDOR_SPECFIC_PTR	Pointer for Vendor Specific Area Register	0FA0 00E8h
F4h	MMCSD1_BOOT_TIMEOUT_CONTROL	Boot Timeout Control Register	0FA0 00F4h
F8h	MMCSD1_VENDOR_REGISTER	Vendor Register	0FA0 00F8h
FCh	MMCSD1_SLOT_INT_STS	Slot Interrupt Status Register	0FA0 00FCh
FEh	MMCSD1_HOST_CONTROLLER_VER	Host Controller Version Register	0FA0 00FEh
100h	MMCSD1_UHS2_GEN_SETTINGS	UHS-II General Settings Register	0FA0 0100h
104h	MMCSD1_UHS2_PHY_SETTINGS	UHS-II PHY Settings Register	0FA0 0104h
108h	MMCSD1_UHS2_LNK_TRN_SETTINGS	UHS-II LINK/TRAN Settings Register	0FA0 0108h

Table 14-24128. MMCSD1 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCSD1_CTL_CFG Physical Address
110h	MMCSD1_UHS2_GEN_CAP	UHS-II General Capabilities Register	0FA0 0110h
114h	MMCSD1_UHS2_PHY_CAP	UHS-II PHY Capabilities Register	0FA0 0114h
118h	MMCSD1_UHS2_LNK_TRN_CAP	UHS-II LINK/TRAN Capabilities Register	0FA0 0118h
120h	MMCSD1_FORCE_UHSII_ERR_INT_STS	Force Event for UHS-II Error Interrupt Status Register	0FA0 0120h
		Command Queue Registers	
200h	MMCSD1_CQ_VERSION	Command Queueing Version Register	0FA0 0200h
204h	MMCSD1_CQ_CAPABILITIES	Command Queueing Capabilities Register	0FA0 0204h
208h	MMCSD1_CQ_CONFIG	Command Queueing Configuration Register	0FA0 0208h
20Ch	MMCSD1_CQ_CONTROL	Command Queueing Control Register	0FA0 020Ch
210h	MMCSD1_CQ_INTR_STS	Command Queueing Interrupt Status Register	0FA0 0210h
214h	MMCSD1_CQ_INTR_STS_ENA	Command Queueing Interrupt Status Enabled Register	0FA0 0214h
218h	MMCSD1_CQ_INTR_SIG_ENA	Command Queueing Interrupt Signal Enable Register	0FA0 0218h
21Ch	MMCSD1_CQ_INTR_COALESCING	Interrupt Coalescing Register	0FA0 021Ch
220h	MMCSD1_CQ_TDL_BASE_ADDR	Command Queueing Task Descriptor List Base Address Low Register	0FA0 0220h
224h	MMCSD1_CQ_TDL_BASE_ADDR_UPBITS	Command Queueing Task Descriptor List Base Address High Register	0FA0 0224h
228h	MMCSD1_CQ_TASK_DOOR_BELL	Command Queueing Task Doorbell Register	0FA0 0228h
22Ch	MMCSD1_CQ_TASK_COMP_NOTIF	Command Queueing Task Doorbell Notification Register	0FA0 022Ch
230h	MMCSD1_CQ_DEV_QUEUE_STATUS	Command Queueing Device Queue Status Register	0FA0 0230h
234h	MMCSD1_CQ_DEV_PENDING_TASKS	Command Queueing Device Pending Tasks Register	0FA0 0234h
238h	MMCSD1_CQ_TASK_CLEAR	Command Queueing Task Clear Register	0FA0 0238h
240h	MMCSD1_CQ_SEND_STS_CONFIG1	Send Status Timer Configuration 1 Register	0FA0 0240h
244h	MMCSD1_CQ_SEND_STS_CONFIG2	Send Status Configuration 2 Register	0FA0 0244h
248h	MMCSD1_CQ_DCMD_RESPONSE	Command Response Register for Direct Command Task	0FA0 0248h
250h	MMCSD1_CQ_RESP_ERR_MASK	Response Mode Error Mask Register	0FA0 0250h
254h	MMCSD1_CQ_TASK_ERR_INFO	Task Error Information Register	0FA0 0254h
258h	MMCSD1_CQ_CMD_RESP_INDEX	Command Response Index Register	0FA0 0258h
25Ch	MMCSD1_CQ_CMD_RESP_ARG	Command Response Argument Register	0FA0 025Ch
260h	MMCSD1_CQ_ERROR_TASK_ID	Command Queueing Error Task ID Register	0FA0 0260h

(1) UHSII is not supported. For more information, see *Not Supported Features*.

1 MMCSD1_SDMA_SYS_ADDR_LO Register (Offset = 0h) [reset = 0h]

MMCSD1_SDMA_SYS_ADDR_LO is shown in Figure 14-7968 and described in Table 14-16163.

Return to Summary Table.

This register contains the Lower 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

Table 14-24129. MMCSD1_SDMA_SYS_ADDR_LO Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0000h

Figure 14-7968. MMCSD1_SDMA_SYS_ADDR_LO Register

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">SDMA_ADDRESS</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24131. MMCSD1_SDMA_SYS_ADDR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDMA_ADDRESS	R/W	0h	32-bit Block Count (SDMA System Address) Low When the MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h, DMA uses this register as system address in only 32-bit addressing mode. Auto CMD23 cannot be used with SDMA. When the MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, SDMA uses the MMCSD1_ADMA_SYS_ADDRESS register instead of using this register to support both 32-bit and 64-bit addressing. This register is re-assigned to 32-bit Block Count and then SDMA may use Auto CMD23. (1) SDMA System Address (MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 0h) This register contains the system memory address for a SDMA transfer in 32-bit addressing mode. When the Host Controller (HC) stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (after a transaction has stopped). Reading this register during SDMA transfers may return an invalid value. The Host Driver (HD) shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the MMCSD1_BLOCK_SIZE[14-12] SDMA_BUF_SIZE bit field. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (Offset = 3h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by setting the MMCSD1_BLOCK_GAP_CONTROL[1] CONTINUE bit, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI). ADMA does not use this register. (2) 32-bit Block Count (MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 1h) Host Controller Version 4.10 re-defines this register as 32-bit Block Count . In version 4.00, this register may be used as 32-bit block count only for Auto CMD23 to set the argument of the CMD23 while executing Auto CMD23. The Host Controller would decrement the block count of this register every block transfer and data transfer stops when the count reaches zero. FFFF FFFFh (4G - 1 Block) .... 0000 0002h (2 Blocks) 0000 0001h (1 Block)

Table 14-24131. MMCSD1_SDMA_SYS_ADDR_LO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0000 0000h (Stop Count) **Note:** This register should be accessed only when no transaction is executing. Reading this register during data transfers may return invalid value.

2 MMCSD1_SDMA_SYS_ADDR_HI Register (Offset = 2h) [reset = 0h]

MMCSD1_SDMA_SYS_ADDR_HI is shown in Figure 14-7969 and described in Table 14-16165.

Return to Summary Table.

This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

Table 14-24132. MMCSD1_SDMA_SYS_ADDR_HI Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0002h

Figure 14-7969. MMCSD1_SDMA_SYS_ADDR_HI Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">SDMA_ADDRESS</td></tr>
<tr><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-24134. MMCSD1_SDMA_SYS_ADDR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDMA_ADDRESS	R/W	0h	32-bit Block Count (SDMA System Address) High This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

3 MMCSD1_BLOCK_SIZE Register (Offset = 4h) [reset = 0h]

MMCSD1_BLOCK_SIZE is shown in Figure 14-7970 and described in Table 14-16167.

Return to Summary Table.

This register is used to configure the number of bytes in a data block.

Table 14-24135. MMCSD1_BLOCK_SIZE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0004h

Figure 14-7970. MMCSD1_BLOCK_SIZE Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_SIZE			XFER_BLK_SIZE			
R-0h	R/W-0h			R/W-0h			

7	6	5	4	3	2	1	0
XFER_BLK_SIZE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-24137. MMCSD1_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	SDMA_BUF_SIZE	R/W	0h	Host SDMA Buffer Size To perform long DMA transfer, System Address register (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI) shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the System Address register (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI). These bits shall support when the MMCSD1_CAPABILITIES[22] SDMA_SUPPORT bit is set to 1h and this function is active when the MMCSD1_TRANSFER_MODE[0] DMA_ENA bit is set to 1h. 0h: 4KB (Detects A11 Carry out) 1h: 8KB (Detects A12 Carry out) 2h: 16KB (Detects A13 Carry out) 3h: 32KB (Detects A14 Carry out) 4h: 64KB (Detects A15 Carry out) 5h: 128KB (Detects A16 Carry out) 6h: 256KB (Detects A17 Carry out) 7h: 512KB (Detects A18 Carry out)

Table 14-24137. MMCSD1_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	XFER_BLK_SIZE	R/W	0h	Transfer Block Size This field specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. It can be accessed only if no transaction is executing (after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. 0000h: No Data Transfer 0001h: 1 Byte 0002h: 2 Bytes 0003h: 3 Bytes 0004h: 4 Bytes .... 01FFh: 511 Bytes 0200h: 512 Bytes .... 0800h: 2048 Bytes

4 MMCSD1_BLOCK_COUNT Register (Offset = 6h) [reset = 0h]

MMCSD1_BLOCK_COUNT is shown in Figure 14-7971 and described in Table 14-16169.

Return to Summary Table.

This register is used to configure the number of data blocks.

Table 14-24138. MMCSD1_BLOCK_COUNT Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0006h

Figure 14-7971. MMCSD1_BLOCK_COUNT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XFER_BLK_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-24140. MMCSD1_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	XFER_BLK_CNT	R/W	0h	16-bit Block Count Host Controller Version 4.10 extends block count to 32-bit . Selection of either 16-bit Block Count register or 32-bit Block Count register is defined as follows: (1) If the MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h or 16-bit Block Count register is set to non-zero, 16-bit Block Count register is selected. (2) If the MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h and 16-bit Block Count register is set to zero, 32-bit Block Count register is selected. Use of 16-bit/32-bit Block Count register is enabled when the MMCSD1_TRANSFER_MODE[1] BLK_CNT_ENA bit is set to 1h and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1h and the maximum block count. The Host Controller decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0h results in no data blocks is transferred. This register should be accessed only when no transaction is executing (after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. 0000h: Stop Count 0001h: 1 Block 0002h: 2 Blocks .... FFFFh: 65535 Blocks

5 MMCSD1_ARGUMENT1_LO Register (Offset = 8h) [reset = 0h]

MMCSD1_ARGUMENT1_LO is shown in Figure 14-7972 and described in Table 14-16171.

Return to Summary Table.

This register contains Lower bits of SD Command Argument.

Table 14-24141. MMCSD1_ARGUMENT1_LO Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0008h

Figure 14-7972. MMCSD1_ARGUMENT1_LO Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ARG1															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24143. MMCSD1_ARGUMENT1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_ARG1	R/W	0h	Command Argument 1 Low The SD Command Argument is specified as bit 23-8 of Command-Format.

6 MMCSD1_ARGUMENT1_HI Register (Offset = Ah) [reset = 0h]

MMCSD1_ARGUMENT1_HI is shown in Figure 14-7973 and described in Table 14-16173.

Return to Summary Table.

This register contains higher bits of SD Command Argument.

Table 14-24144. MMCSD1_ARGUMENT1_HI Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 000Ah

Figure 14-7973. MMCSD1_ARGUMENT1_HI Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ARG1															
R/W-0h															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24146. MMCSD1_ARGUMENT1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_ARG1	R/W	0h	Command Argument 1 High The SD Command Argument is specified as bit 39-24 of Command-Format.

7 MMCSD1_TRANSFER_MODE Register (Offset = Ch) [reset = 0h]

MMCSD1_TRANSFER_MODE is shown in Figure 14-7974 and described in Table 14-16175.

Return to Summary Table.

Table 14-24147. MMCSD1_TRANSFER_MODE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 000Ch

Figure 14-7974. MMCSD1_TRANSFER_MODE Register

15	14	13	12	11	10	9	8
RESERVED							RESP_INTR_DIS
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESP_ERR_CHK_ENA	RESP_TYPE	MULTI_BLK_SEL	DATA_XFER_DIR	AUTO_CMD_ENA		BLK_CNT_ENA	DMA_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-24149. MMCSD1_TRANSFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Response Interrupt Disable Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0h and waits Command Complete Interrupt (MMCSD1_NORMAL_INTR_STS[0] CMD_COMPLETE) and then checks the Response register (MMCSD1_RESPONSE_0 to MMCSD1_RESPONSE_7). If Host Controller checks response error, sets this bit to 1h and sets the MMCSD1_TRANSFER_MODE[7] RESP_ERR_CHK_ENA bit to 1h. Command Complete Interrupt (MMCSD1_NORMAL_INTR_STS[0] CMD_COMPLETE) is disabled by this bit regardless of Command Complete Signal Enable (MMCSD1_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE). 0h: Response Interrupt is enabled 1h: Response Interrupt is disabled

Table 14-24149. MMCSD1_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESP_ERR_CHK_ENA	R/W	0h	Response Error Check Enable Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, this bit is set to 0h and the MMCSD1_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 0h. If Host Controller checks response error, sets this bit to 1h and sets the Response Interrupt Disable bit to 1h (MMCSD1_TRANSFER_MODE[8] RESP_INTR_DIS = 1h). The MMCSD1_TRANSFER_MODE[6] RESP_TYPE bit selects either R1 or R5 response type. If an error is detected, Response Error Interrupt is generated in the MMCSD1_ERROR_INTR_STS register. 0h: Response Error Check is disabled 1h: Response Error Check is enabled
6	RESP_TYPE	R/W	0h	Response Type R1/R5 When response error check is enabled (MMCSD1_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1h), this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1: Bit31 OUT_OF_RANGE Bit30 ADDRESS_ERROR Bit29 BLOCK_LEN_ERROR Bit26 WP_VIOLATION Bit25 CARD_IS_LOCKED Bit23 COM_CRC_ERROR Bit21 CARD_ECC_FAILED Bit20 CC_ERROR Bit19 ERROR Response Flags Checked in R5: Bit07 COM_CRC_ERROR Bit03 ERROR Bit01 FUNCTION_NUMBER Bit00 OUT_OF_RANGE 0h: R1 (Memory) 1h: R5 (SDIO)

Table 14-24149. MMCSD1_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MULTI_BLK_SEL	R/W	0h	Multi/Single Block Select This bit enables multiple block data transfers. 0h: Single Block 1h: Multiple Block
4	DATA_XFER_DIR	R/W	0h	Data Transfer Direction Select This bit defines the direction of data transfers. 0h: Write (Host to Card) 1h: Read (Card to Host)

Table 14-24149. MMCSD1_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	AUTO_CMD_ENA	R/W	0h	Auto CMD Enable This field determines use of auto command functions. There are three methods to stop Multiple-block read and write operation by CMD23 or CMD12. In the other operations (for example single read/write operation), this field is set to 0h. (1) Auto CMD12 Enable: Multiple-block read and write commands for memory require CMD12 to stop the operation. When this field is set to 1h, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the MMCSD1_AUTOCMD_ERR_STS register. The Host Driver shall not set this bit if the command does not require CMD12. When MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 0h, CMD12 is issued when 16-bit Block Count is expired. When MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 1h, CMD12 is issued when 16-bit Block Count or 32-bit Block Count is expired. (2) Auto CMD23 Enable: When this bit field is set to 2h, the Host Controller issues a CMD23 automatically before issuing a command specified in the MMCSD1_COMMAND register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23: Auto CMD23 Supported (Host Controller Version is 3.00 or later). A memory card that supports CMD23 (SCR[33] = 1h). If DMA is used, it shall be ADMA. Only when CMD18 or CMD25 is issued. Auto CMD23 can be used with or without ADMA. By writing the MMCSD1_COMMAND register, the Host Controller issues a CMD23 first and then issues a command specified by the MMCSD1_COMMAND[13:8] CMD_INDEX bit field. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the MMCSD1_AUTOCMD_ERR_STS register. 32-bit block count value for CMD23 is set to 32-bit Block Count (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI) register. (3) Auto CMD Auto Select (Version 4.10): As CMD23 is optional for SD memory card except UHS 104 card, if card supports CMD23, Auto CMD 23 should be used instead of Auto CMD12. Host Controller Version 4.10 defines this "Auto CMD Auto Select" mode. Selection of Auto CMD depends on setting of the MMCSD1_HOST_CONTROL2[11] CMD23_ENA bit which indicates whether card supports CMD23. If MMCSD1_HOST_CONTROL2[11] CMD23_ENA = 1h, Auto CMD23 is used and if MMCSD1_HOST_CONTROL2[11] CMD23_ENA = 0h,

Table 14-24149. MMCSD1_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Auto CMD12 is used. In case of Version 4.10 or later, use of Auto CMD Auto Select is recommended rather than use of Auto CMD12 Enable or Auto CMD23 Enable. 0h: Auto Command Disabled 1h: Auto CMD12 Enable 2h: Auto CMD23 Enable 3h: Reserved
1	BLK_CNT_ENA	R/W	0h	Block Count Enable This bit is used to enable the MMCSD1_BLOCK_COUNT register, which is only relevant for multiple block transfers. When this bit is 0h, the MMCSD1_BLOCK_COUNT register is disabled, which is useful in executing an infinite transfer. 0h: Disable 1h: Enable
0	DMA_ENA	R/W	0h	DMA Enable DMA can be enabled only if the MMCSD1_CAPABILITIES[22] SDMA_SUPPORT bit is set. If this bit is set to 1h, a DMA operation shall begin when the HD writes to the upper byte of the MMCSD1_COMMAND register. 0h: Disable 1h: Enable

This register is used to control the operations of data transfers.

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data (Refer to MMCSD1_COMMAND[5] DATA_PRESENT bit), or before issuing a Resume command. The Host Driver shall save the value of this register when the data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller shall implement write protection for this register during data transactions. Writes to this register shall be ignored when the MMCSD1_PRESENTSTATE[1] INHIBIT_DAT bit is 1h.

Table 14-16176 shows the determination of transfer type.

Table 14-24150. Determination of Transfer Type

Multi/Single Block Select	Block Count Enable	Block Count	Function
0	Don't Care	Don't Care	Single Transfer
1	0	Don't Care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

8 MMCSD1_COMMAND Register (Offset = Eh) [reset = 0h]

MMCSD1_COMMAND is shown in Figure 14-7975 and described in Table 14-16178.

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This register is used to program the Command for host controller.

Table 14-24151. MMCSD1_COMMAND Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 000Eh

Figure 14-7975. MMCSD1_COMMAND Register

15	14	13	12	11	10	9	8
RESERVED		CMD_INDEX					
R-0h		R/W-0h					

7	6	5	4	3	2	1	0
CMD_TYPE		DATA_PRESENT	CMD_INDEX_CHK_ENA	CMD_CRC_CHK_ENA	SUB_CMD	RESP_TYPE_SEL	
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24153. MMCSD1_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	CMD_INDEX	R/W	0h	Command Index This bit shall be set to the command number (CMD0-63, ACMD0-63).

Table 14-24153. MMCSD1_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	CMD_TYPE	R/W	0h	Command Type There are three types of special commands. Suspend, Resume and Abort. These bits shall be set to 0h for all other commands. Suspend Command: If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state. and the HD shall restart the transfer by setting the MMCSD1_BLOCK_GAP_CONTROL[1] CONTINUE bit. Resume Command: The HD re-starts the data transfer by restoring the registers in the range of 04FB 0000h - 04FB 000Dh (04F9 8000h - 04F9 800Dh). The HC shall check for busy before starting write transfers. Abort Command: If this command is set when executing a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a write transfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset. 0h: Normal 1h: Suspend 2h: Resume 3h: Abort
5	DATA_PRESENT	R/W	0h	Data Present Select This bit is set to 1h to indicate that data is present and shall be transferred using the DAT line. If is set to 0h for the following: 1. Commands using only CMD line (for example CMD52). 2. Commands with no data transferbut using busy signal on DAT[0]line (R1b or R5b for example CMD38). 3. Resume Command. 0h: No Data Present 1h: Data Present
4	CMD_INDEX_CHK_ENA	R/W	0h	Command Index Check Enable If this bit is set to 1h, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0h, the Index field is not checked. 0h: Disable 1h: Enable

Table 14-24153. MMCSD1_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMD_CRC_CHK_ENA	R/W	0h	Command CRC Check Enable If this bit is set to 1h, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0h, the CRC field is not checked. 0h: Disable 1h: Enable
2	SUB_CMD	R/W	0h	Sub Command Flag This bit is added from Version 4.10 to distinguish a main command or sub command. When issuing a main command, this bit is set to 0h and when issuing a sub command, this bit is set to 1h. Setting of this bit is checked by the MMCSD1_PRESENTSTATE[28] SUB_COMMAND_STS bit. Host Driver manages whether main or sub command. Host Controller does not refer to this bit to issue a command. 0h: Sub Command 1h: Main Command
1-0	RESP_TYPE_SEL	R/W	0h	Response Type Select 0h: No Response 1h: Response length 136 2h: Response length 48 3h: Response length 48 check Busy after response

9 MMCSD1_RESPONSE_0 to MMCSD1_RESPONSE_7 Register (Offset = 10h to 1Eh) [reset = 0h]

MMCSD1_RESPONSE_0 to MMCSD1_RESPONSE_7 is shown in Figure 14-7976 and described in Table 14-16180.

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This registers is used to store responses from SD Cards.

Table 14-24154. MMCSD1_RESPONSE_0 to MMCSD1_RESPONSE_7 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0010h to 0FA0 001Eh

Figure 14-7976. MMCSD1_RESPONSE_0 to MMCSD1_RESPONSE_7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_RESP															
R-0h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24156. Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_RESP	R	0h	Command Response R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.

Table 14-16181 defines the relation between the parameter and name of response type.

Table 14-24157. Relation between Parameters and the Name of Response Type

Response Type	Index Check Enable	CRC Check Enable	Name of Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R6, R5, R7
11	1	1	R1b, R5b

The following table describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.

Table 14-16182 shows response bit definition for each response type.

Table 14-24158. Response Bit Definition for each Response Type

Kind of Response	Meaning of Response	Response Field	Response Register
R1, R1b (normal response)	Card Status	R[39:8]	REP[31:0]
R1b (Auto CMD12 response)	Card Status for Auto CMD12	R[39:8]	REP[127:96]
R1 (Auto CMD23 response)	Card Status for Auto CMD23	R[39:8]	REP [127:96]
R2 (CID, CSD Register)	CID or CSD register include	R[127:8]	REP[119:0]
R3 (OCR Register)	OCR Register for memory	R[39:8]	REP[31:0]
R4 (OCR Register)	OCR Register for I/O etc.	R[39:8]	REP[31:0]
R5, R5b	SDIO Response	R[39:8]	REP[31:0]

Table 14-24158. Response Bit Definition for each Response Type (continued)

Kind of Response	Meaning of Response	Response Field	Response Register
R6 (Published RCA response)	New published RCA[31:16] etc.	R[39:8]	REP[31:0]

The Response Field indicates bit positions of "Responses" defined in the Physical Layer Specification. The table shows most responses with a length of 48 (R[47:0]) have 32 bits of the response data (R[39:8]) stored in the Response register at REP[31:0]. Responses of type R1b (Auto CMD12 responses) and R1 (Auto CMD23 response) have response data bits R[39:8] stored in the Response register at REP[127:96]. Responses with length 136 (R[135:0]) have 120 bits of the response data (R[127:8]) stored in the Response register at REP[119:0].

To read the response status efficiently, the Host Controller only stores part of the response data in the Response register. This enables the Host Driver to read 32 bits of response data efficiently in one read cycle on a 32-bit bus system. Parts of the response, the Index field and the CRC, are checked by the Host Controller (as specified by the MMCSD1_COMMAND[4] CMD_INDEX_CHK_ENA and MMCSD1_COMMAND[3] CMD_CRC_CHK_ENA bits) and generate an error interrupt if an error is detected. The bit range for the CRC check depends on the response length. If the response length is 48, the Host Controller shall check R[47:1], and if the response length is 136 the Host Controller shall check R[119:1].

Since the Host Controller may have a multiple block data DAT line transfer executing concurrently with a CMD_wo_DAT command, the Host Controller stores the Auto CMD12 response in the upper bits (REP[127:96]) of the Response register. The CMD_wo_DAT response is stored in REP[31:0]. This allows the Host Controller to avoid overwriting the Auto CMD12 response with the CMD_wo_DAT and vice versa.

While executing Auto CMD23, the response of CMD23 is saved to REP [127:96] and the response of multiple-block read and write command is save to REP [31:0]. The response error of CMD23 is indicated in the MMCSD1_AUTOCMD_ERR_STS register. When the Host Controller modifies part of the Response register, as shown in the table, it shall preserve the unmodified bits.

10 MMCSD1_DATA_PORT Register (Offset = 20h) [reset = 0h]

MMCSD1_DATA_PORT is shown in Figure 14-7977 and described in Table 14-16184.

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This register is used to access internal buffer.

Table 14-24159. MMCSD1_DATA_PORT Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0020h

Figure 14-7977. MMCSD1_DATA_PORT Register

31-0
BUF_RD_DATA
R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24161. MMCSD1_DATA_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUF_RD_DATA	R/W	0h	Buffer Data The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

11 MMCSD1_PRESENTSTATE Register (Offset = 24h) [reset = 1F00000h]

MMCSD1_PRESENTSTATE is shown in Figure 14-7978 and described in Table 14-16186.

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The Host Driver can get status of the Host Controller from this 32-bit read-only register.

Table 14-24162. MMCSD1_PRESENTSTATE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0024h

Figure 14-7978. MMCSD1_PRESENTSTATE Register

31	30	29	28	27	26	25	24
UHS2_IF_DETECTION	UHS2_IF_LANE_SYNC	UHS2_DORMANT	SUB_COMMAND_STS	CMD_NOT_ISS_BY_ERR	RESERVED		SDIF_CMDIN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		R-1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SDIF_DAT3IN	SDIF_DAT2IN	SDIF_DAT1IN	SDIF_DAT0IN	WRITE_PROTECT	CARD_DETECT	CARD_STATE_STABLE	CARD_INSERTED
R-1h	R-1h	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				BUF_RD_ENA	BUF_WR_ENA	RD_XFER_ACTIVE	WR_XFER_ACTIVE
R-0h				R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDIF_DAT7IN	SDIF_DAT6IN	SDIF_DAT5IN	SDIF_DAT4IN	RETUNING_REQ	DATA_LINE_ACTIVE	INHIBIT_DAT	INHIBIT_CMD
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24164. MMCSD1_PRESENTSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UHS2_IF_DETECTION	R	0h	UHS-II IF Detection (UHS-II Only) This status indicates whether a card supports UHS-II IF. This status is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD1_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). UHS-II interface initialization is activated by setting the MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA bit. Host Controller drives STB.L on D0 lane from EIDL state and waits for receiving STB.L on D1 lane. This bit is set to 1h if STB.L is detected on D1 lane. Host Controller shall compensate latency from setting SD Clock Enable to output STB.L on D0 lane when reading this status. This bit may be read any time after setting SD Clock Enable for faster UHS-II IF detection but Host Driver shall check this status at least 200µs period from setting SD Clock Enable (MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA) until detecting UHS-II IF. After UHS-II IF is detected, this bit is cleared by when EIDL is detected on D0 lane, UHS-II Interface Enable is set to 0h (MMCSD1_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or Host full reset is executed. 1h: UHS-II IF is detected 0h: UHS-II IF is not detected
30	UHS2_IF_LANE_SYNC	R	0h	Lane Synchronization (UHS-II Only) This status indicates whether lane is synchronized in UHS-II mode. This status is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD1_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). On detecting UHS-II Interface (D31 = 1h), Host Controller provides SYN LSS on D0 lane and waits for receiving SYN LSS on D1 lane. If SYN LSS is detected on D1 lane, Host Controller provides LIDL LSS on D0 lane and waits for receiving LIDL LSS on D1 lane. In case of Version 4.00, this bit indicates completion of Device PHY Initialization by detecting LIDL LSS on D1 lane. From Version 4.10, Host Controller may implement a specific PHY verification method and PHY Initialization Failure can be indicated by keeping this bit to 0h even LIDL LSS is detected on D1 lane. Host Driver detects PHY Initialization Failure by timeout. This bit is cleared by when D0 lane is set to EIDL, UHS-II Interface Enable is set to 0h (MMCSD1_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or executes Host full reset. 1h: UHS-II PHY is initialized 0h: UHS-II PHY is not initialized

Table 14-24164. MMCSD1_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	UHS2_DORMANT	R	0h	In Dormant State (UHS-II Only) This status indicates whether UHS-II lanes enter Dormant state. This function is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD1_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). On issuing GO_DORMAT_STATE command, "Go Dormant Command (7h)" is set to Command type in the UHS-II Command register (MMCSD1_UHS2_COMMAND[7:6] CMD_TYPE). This command type acts as a trigger to enter lanes into dormant state. Host Controller provides STB.H and EIDL on D0 lane and waits for receiving STB.H and EIDL on D1 lane. This bit is set to 1h after the time of T_DMT_ENTRY (750 RCLK cycle) or more from detecting EIDL on D1 lane. RCLK may be stopped in dormant state, by setting SD Clock Enable to 0h in the Clock Control register (MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA = 0h) while In Dormant State bit is set to 1h. On writing Clock Control register with setting SD Clock Enable to 1h (MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA = 1h), Host Controller wakes lanes to exit Dormant State and In Dormant State is set to 0h. In case of the card enters Hibernate Mode (RCLK is stopped), Host Driver may turn off VDD1 by clearing SD Bus Power for VDD1 bit in the MMCSD1_POWER_CONTROL register. Host Controller shall turn off VDD1 after stopping RCLK. This bit is cleared by when Host Controller drives STB.L on D0 lane, UHS-II Interface Enable is set to 0h (MMCSD1_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or executes Host full reset. 1h: In DORMANT state 0h: Not in DORMANT state
28	SUB_COMMAND_STS	R	0h	Sub Command Status The MMCSD1_COMMAND register and Response register (MMCSD1_RESPONSE_0 to MMCSD1_RESPONSE_7) are commonly used for main command and sub command. This status is used to distinguish which response error statuses, main command or sub command, indicated in the MMCSD1_ERROR_INTR_STS register or in the MMCSD1_UHS2_ERR_INTR_STS register. Just before reading of this register, the MMCSD1_COMMAND[2] SUB_CMD bit or the MMCSD1_UHS2_COMMAND register is copied to this status. This status is effective not only when Response Error interrupt is generated but also when data error interrupt is generated with Command Not Issued by Error (D27 of this register) or Auto CMD Error interrupt is generated with Command Not Issued by Error by Auto CMD12 in the MMCSD1_AUTOCMD_ERR_STS register. 1h: Sub Command Status 0h: Main Command Status

Table 14-24164. MMCSD1_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMD_NOT_ISS_BY_ERR	R	0h	Command Not Issued by Error Setting of this status indicates that a command cannot be issued due to an error except Auto CMD12 error (equivalent error status by Auto CMD12 error is defined as Command Not Issued By Auto CMD12 Error in the MMCSD1_AUTOCMD_ERR_STS register). This status is set to 1h when Host Controller cannot issue a command after setting MMCSD1_COMMAND register or MMCSD1_UHS2_COMMAND register. Sub Command Status (D28) indicates which command is not issued (main or sub). 1h: Command cannot be issued 0h: No error for issuing a command
26-25	RESERVED	R	0h	Reserved
24	SDIF_CMDIN	R	1h	CMD Line Signal Level (SD Mode Only) This status is used to check CMD line level to recover from errors, and for debugging.
23	SDIF_DAT3IN	R	1h	DAT[3] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[3]. D23 - DAT[3]
22	SDIF_DAT2IN	R	1h	DAT[2] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[2]. D22 - DAT[2]
21	SDIF_DAT1IN	R	1h	DAT[1] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[1]. D21 - DAT[1]
20	SDIF_DAT0IN	R	1h	DAT[0] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D20 - DAT[0]
19	WRITE_PROTECT	R	0h	Write Protect Switch Pin Level The Write Protect Switch is supported for memory and combo cards.This bit reflects the SDWP# pin. 0h: Write protected (SDWP# = 1) 1h: Write enabled (SDWP# = 0)

Table 14-24164. MMCSD1_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CARD_DETECT	R	0h	Card Detect Pin Level This bit reflects the inverse value of the SDCD# pin. 0h: No Card present (SDCD# = 1) 1h: Card present (SDCD# = 0)
17	CARD_STATE_STABLE	R	0h	Card State Stable This bit is used for testing. If it is 0h, the Card Detect Pin Level is not stable. If this bit is set to 1h, it means the Card Detect Pin Level is stable. The MMCSD1_SOFTWARE_RESET[0] SWRST_FOR_ALL bit shall not affect this bit. 0h: Reset of Debouncing 1h: No Card or Inserted
16	CARD_INSERTED	R	0h	Card Inserted This bit indicates whether a card has been inserted. Changing from 0h to 1h generates a Card Insertion interrupt in the MMCSD1_NORMAL_INTR_STS register and changing from 1h to 0h generates a Card Removal Interrupt in the MMCSD1_NORMAL_INTR_STS register. The MMCSD1_SOFTWARE_RESET[0] SWRST_FOR_ALL bit shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear the MMCSD1_POWER_CONTROL[0] SD_BUS_POWER bit and the MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA bit. In addition the HD should clear the HC by the MMCSD1_SOFTWARE_RESET[0] SWRST_FOR_ALL bit. The card detect is active regardless of the SD Bus Power. 0h: Reset or Debouncing or No Card 1h: Card Inserted
15-12	RESERVED	R	0h	Reserved
11	BUF_RD_ENA	R	0h	Buffer Read Enable This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1h, readable data exists in the buffer. A change of this bit from 1h to 0h occurs when all the block data is read from the buffer. A change of this bit from 0h to 1h occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0h: Read Disable 1h: Read Enable

Table 14-24164. MMCSD1_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	BUF_WR_ENA	R	0h	Buffer Write Enable This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1h, data can be written to the buffer. A change of this bit from 1h to 0h occurs when all the block data is written to the buffer. A change of this bit from 0h to 1h occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. 0h: Write Disable 1h: Write Enable
9	RD_XFER_ACTIVE	R	0h	Read Transfer Active (SD Mode Only) This status is used for detecting completion of a read transfer. This bit is set to 1h for either of the following conditions: After the end bit of the read command. When writing a 1h to continue Request in the MMCSD1_BLOCK_GAP_CONTROL register to restart a read transfer. This bit is cleared to 0h for either of the following conditions: When the last data block as specified by block length is transferred to the system. When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1h (MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h). A transfer complete interrupt is generated when this bit changes to 0h. 1h: Transferring data 0h: No valid data

Table 14-24164. MMCSD1_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WR_XFER_ACTIVE	R	0h	Write Transfer Active (SD Mode Only) This status indicates a write transfer is active. If this bit is 0h, it means no valid write data exists in the HC. This bit is set in either of the following cases: After the end bit of the write command. When writing a 1h to the MMCSD1_BLOCK_GAP_CONTROL[1] CONTINUE bit to restart a write transfer. This bit is cleared in either of the following cases: After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple). After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0h, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 1h: Transferring data 0h: No valid data
7	SDIF_DAT7IN	R	0h	DAT[7] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D07 - DAT[7]
6	SDIF_DAT6IN	R	0h	DAT[6] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D06 - DAT[6]
5	SDIF_DAT5IN	R	0h	DAT[5] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D05 - DAT[5]
4	SDIF_DAT4IN	R	0h	DAT[4] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D04 - DAT[4]

Table 14-24164. MMCSD1_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RETUNING_REQ	R	0h	Re-Tuning Request (UHS-I Only) Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting the MMCSD1_HOST_CONTROL2[6] EXECUTE_TUNING bit. Changing of this bit from 0h to 1h generates Re-Tuning Event. This bit isn't set to 1h if the MMCSD1_HOST_CONTROL2[7] SAMPLING_CLK_SELECT bit is set to 0h (using fixed sampling clock). 1h: Sampling clock needs re-tuning 0h: Fixed or well tuned sampling clock
2	DATA_LINE_ACTIVE	R	0h	DAT Line Active (SD Mode Only) This bit indicates whether one of the DAT line on SD bus is in use. 1h: DAT line active 0h: DAT line inactive
1	INHIBIT_DAT	R	0h	Command Inhibit (DAT) (SD Mode Only) This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1h. If this bit is 0h, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (for example R1b, R5b type). Changing from 1h to 0h generates a Transfer Complete interrupt in the MMCSD1_NORMAL_INTR_STS register. **Note:** The SD Host Driver can save registers in the range of 04FB 0000h - 04FB 000Dh (04F9 8000h - 04F9 800Dh) for a suspend transaction after this bit has changed from 1h to 0h. 1h: Cannot issue command which uses the DAT line 0h: Can issue command which uses the DAT line

Table 14-24164. MMCSD1_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INHIBIT_CMD	R	0h	Command Inhibit (CMD) **SD Mode:** If this bit is 0h, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the MMCSD1_COMMAND register is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1h. Commands using only the CMD line can be issued if this bit is 0h. Changing from 1h to 0h generates a Command complete interrupt in the MMCSD1_NORMAL_INTR_STS register. If the HC cannot issuethe command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1h and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by the MMCSD1_COMMAND register. **UHS-II Mode:** This bit is 0h means that a command packet can be issued by the Host Controller. While this bit is set to 1h, which means the Host Controller is not ready to issue a next command, Host Driver shall not write the registers from the MMCSD1_UHS2_BLOCK_SIZE to the MMCSD1_UHS2_COMMAND. Changing from 1h to 0h generates a Command Complete Interrupt in the MMCSD1_NORMAL_INTR_STS register. 1h: Host Controller is not ready to issue a command 0h: Host Controller is ready to issue a command Version 4.10 adds a new control to prevent error statuses from overwriting by receipt of a next command. This status keeps indicating 1h while any of response error statuses is set to 1h, Command Not Issued by Error in this register is set to 1h or the MMCSD1_AUTOCMD_ERR_STS[7] CMD_NOT_ISSUED bit is set to 1h. Software Reset For CMD Lineis used to clear the error statuses above and this status (MMCSD1_SOFTWARE_RESET[1] SWRST_FOR_CMD).

Note: DAT line active indicates whether one of the DAT line is on SD bus is in use.

(a) In the case of read transactions

This status indicates whether a read transfer is executing on the SD Bus. Changing this value from 1h to 0h generates a Block Gap Event interrupt in the MMCSD1_NORMAL_INTR_STS register, as the result of the Stop At Block Gap Request being set.

This bit shall be set in either of the following cases:

(1) After the end bit of the read command.

(2) When writing a 1h to the MMCSD1_BLOCK_GAP_CONTROL[1] CONTINUE bit to restart a read transfer.

This bit shall be cleared in either of the following cases:

(1) When the end bit of the last data block is sent from the SD Bus to the Host Controller. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.

(2) When a read transfer is stopped at the block gap initiated by a Stop At Block Gap Request (MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP).

The Host Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Host Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use suspend/resume function.

(b) In the case of write transactions

This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1h to 0h generate a Transfer Complete interrupt in the MMCSD1_NORMAL_INTR_STS register.

This bit shall be set in either of the following cases:

(1) After the end bit of the write command.

(2) When writing to 1h to the MMCSD1_BLOCK_GAP_CONTROL[1] CONTINUE bit to continue a write transfer.

This bit shall be cleared in either of the following cases:

(1) When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive "Not Busy". In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.

(2) When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request (MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP).

(c) Command with busy

This status indicates whether a command indicates busy (for example erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command with busy and cleared when busy is de-asserted. Changing this bit from 1h to 0h generate a Transfer Complete interrupt in the MMCSD1_NORMAL_INTR_STS register.

Note

The HD can issue cmd0, cmd12, cmd13 (for memory) and cmd52 (for SDIO) when the DAT lines are busy during data transfer. These commands can be issued when Command Inhibit (CMD) is set to zero (MMCSD1_PRESENTSTATE[0] INHIBIT_CMD = 0h). Other commands shall be issued when Command Inhibit (DAT) is set to zero (MMCSD1_PRESENTSTATE[1] INHIBIT_DAT = 0h).

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12 MMCSD1_HOST_CONTROL1 Register (Offset = 28h) [reset = 0h]

MMCSD1_HOST_CONTROL1 is shown in Figure 14-7979 and described in Table 14-16188.

Return to Summary Table.

This register is used to program DMA modes, LED control, data transfer width, High Speed enable, card detect test level and signal selection.

Table 14-24165. MMCSD1_HOST_CONTROL1 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0028h

Figure 14-7979. MMCSD1_HOST_CONTROL1 Register

7	6	5	4	3	2	1	0
CD_SIG_SEL	CD_TEST_LEVEL	EXT_DATA_WIDTH	DMA_SELECT		HIGH_SPEED_ENA	DATA_WIDTH	LED_CONTROL
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-24167. MMCSD1_HOST_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CD_SIG_SEL	R/W	0h	Card Detect Signal Detection This bit selects source for card detection. 1h: The card detect test level is selected 0h: SDCD# is selected (for normal use)
6	CD_TEST_LEVEL	R/W	0h	Card Detect Test Level This bit is enabled while the Card Detect Signal Selection is set to 1h and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal interrupt status enable bit is set. 1h: Card Inserted 0h: No Card
5	EXT_DATA_WIDTH	R/W	0h	Extended Data Transfer Width (Embedded and SD Mode Only) This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the MMCSD1_CAPABILITIES register. If a device supports 8-bit bus mode, this bit may be set to 1h. If this bit is 0h, bus width is controlled by the MMCSD1_HOST_CONTROL1[1] DATA_WIDTH bit. This bit is not effective when multiple devices are installed on a bus slot (Slot Type is set to 2h in the MMCSD1_CAPABILITIES register). In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register (MMCSD1_SHARED_BUS_CTRL_PTR). 1h: 8-bit Bus Width 0h: Bus Width is Selected by Data Transfer Width

Table 14-24167. MMCSD1_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	DMA_SELECT	R/W	0h	DMA Select This field is used to select DMA type. The Host Driver shall check support of DMA modes by referring the MMCSD1_CAPABILITIES register. Selected DMA is enabled by the MMCSD1_TRANSFER_MODE[0] DMA_ENA bit in SD mode and the MMCSD1_UHS2_XFER_MODE[0] DMA_ENA bit in UHS-II mode. (1) Up to Version 3.00: When MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h, setting of this field is compatible to Host Controller Version 3.00. SDMA is initiated by writing to the MMCSD1_COMMAND register when this field is set to 0h and the SDMA System Address register (32-bit) is used (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI). SDMA does not support 64-bit addressing. ADMA2 is initiated by writing to the MMCSD1_COMMAND register when this field is set to 2h or 3h. Lower 32-bit of the ADMA System Address register (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI) is used when this field is set to 2h and 64-bit of the ADMA System Address register is used when this field is set to 3h. Support of 64-bit System Addressing is indicated by the MMCSD1_CAPABILITIES[28] ADDR_64BIT_SUPPORT_V3 bit. 64-bit AMDA2 uses 96-bit Descriptor. 0h: SDMA is selected 1h: 32-bit Address ADMA1 is selected 2h: 32-bit Address ADMA2 is selected 3h: 64-bit Address ADMA2 is selected (Optional) (2) Version 4.00 or later: When the MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, setting of this field is changed as follows. SDMA is initiated by Host Driver writes to the MMCSD1_COMMAND register when this field is set to 0h. ADMA2 is initiated by Host Driver writes to the MMCSD1_COMMAND register when this field is set to 2h or 3h and by ADMA3 sets to the ADMA System Address register (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI) when this field is set to 3h. ADMA3 is initiated by Host Driver writes to the MMCSD1_ADMA3_DESC_ADDRESS register when this field is set to 3h. 0h: SDMA is selected 1h: Not Used (New assignment is not allowed) 2h: ADMA2 is selected (AMDA3 is not supported or disabled)

Table 14-24167. MMCSD1_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3h: ADMA2 or ADMA3 is selected Support of 64-bit DMA and 128-bit Descriptor is indicated by the MMCSD1_CAPABILITIES[27] ADDR_64BIT_SUPPORT_V4 bit. If the support bit is set to 1h, all supported DMAs (depends on Support, ADMA2 Support and ADMA3 Support) shall support 64-bit addressing. The MMCSD1_HOST_CONTROL2[13] BIT64_ADDRESSING bit selects either 32-bit or 64-bit system addressing of DMAs.
2	HIGH_SPEED_ENA	R/W	0h	High Speed Enable (SD Mode Only) This bit is optional. Before setting this bit, the HD shall check the MMCSD1_CAPABILITIES[21] HIGH_SPEED_SUPPORT bit. If this bit is set to 0h (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/20 MHz for MMC). If this bit is set to 1h, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52 MHz for MMC)/208 MHz (for SD3.0). If the MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1h, Host Driver needs to reset SD Clock Enable (MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA) before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. This bit is not effective in UHS-II mode. 1h: High Speed Mode 0h: Normal Speed Mode
1	DATA_WIDTH	R/W	0h	Data Transfer Width (SD Mode Only) This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. This bit is not effective in UHS-II mode. 1h: 4 bit mode 0h: 1 bit mode
0	LED_CONTROL	R/W	0h	LED Control This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. 1h: LED on 0h: LED off

13 MMCSD1_POWER_CONTROL Register (Offset = 29h) [reset = 0h]

MMCSD1_POWER_CONTROL is shown in Figure 14-7980 and described in Table 14-16190.

Return to Summary Table.

This register is used to program the SD Bus power and voltage level.

Table 14-24168. MMCSD1_POWER_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0029h

Figure 14-7980. MMCSD1_POWER_CONTROL Register

7	6	5	4	3	2	1	0
UHS2_VOLTAGE			UHS2_POWER	SD_BUS_VOLTAGE			SD_BUS_POWER
R/W-0h			R/W-0h	R/W-0h			R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24170. MMCSD1_POWER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	UHS2_VOLTAGE	R/W	0h	SD Bus Voltage Select for VDD2 (UHS-II Only) This field determines supply voltage range to VDD2. This field can be set to 5h if the MMCSD1_CAPABILITIES[60] VDD2_1P8_SUPPORT bit is set to 1h. 111b: Not used 110b: Not used 101b: 1.8 V 100b: Reserved for 1.2 V 011b – 001b: Reserved 000b: VDD2 Not Supported
4	UHS2_POWER	R/W	0h	SD Bus Power for VDD2 (UHS-II Only) Setting this bit enables providing VDD2. 1h: Power on 0h: Power off
3-1	SD_BUS_VOLTAGE	R/W	0h	SD Bus Voltage Select for VDD1 By setting these bits, the HD selects the voltage level for the SD card. Before setting this register, the HD shall check the voltage support bits in the MMCSD1_CAPABILITIES register. If an unsupported voltage is selected, the Host System shall not supply SD bus voltage. 111b: 3.3 V (Flattop.) 110b: 3.0 V (Typ.) 101b: 1.8 V (Typ.) for Embedded 100b – 000b: Reserved

Table 14-24170. MMCSD1_POWER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SD_BUS_POWER	R/W	0h	SD Bus Power for VDD1 Before setting this bit, the SD host driver shall set SD Bus Voltage Select (MMCSD1_POWER_CONTROL[3-1] SD_BUS_VOLTAGE). If the HC detects the No Card State, this bit shall be cleared. If this bit is cleared, the Host Controller should immediately stop driving CMD and DAT[3:0] (tri-state), and drive SDCLK to low level. If card is connected to Host Controller, Host Controller shall set these lines to low before stopping to supply VDD1. In UHS-II mode, before clearing this bit, Host Driver shall clear the MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA bit and before stopping to supply VDD1, Host Controller shall set DAT[2] to low if DAT[2] is used as out-of band interrupt. 1h: Power on 0h: Power off

14 MMCSD1_BLOCK_GAP_CONTROL Register (Offset = 2Ah) [reset = 80h]

MMCSD1_BLOCK_GAP_CONTROL is shown in Figure 14-7981 and described in Table 14-16192.

Return to Summary Table.

This register is used to program the block gap request, read wait control and interrupt at block gap.

Table 14-24171. MMCSD1_BLOCK_GAP_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 002Ah

Figure 14-7981. MMCSD1_BLOCK_GAP_CONTROL Register

7	6	5	4	3	2	1	0
BOOT_ACK_ENA	ALT_BOOT_MODE	BOOT_ENABLE	RESERVED	INTRPT_AT_BLK_GAP	RDWAIT_CTRL	CONTINUE	STOP_AT_BLK_GAP
R/W-1h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24173. MMCSD1_BLOCK_GAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOT_ACK_ENA	R/W	1h	Boot Acknowledge Check To check for the boot acknowledge in boot operation. 1h: Wait for boot ack from eMMC card 0h: Will not wait for boot ack from eMMC card
6	ALT_BOOT_MODE	R/W	0h	Alternative Boot Mode To start boot code access in alternative mode. 1h: To start alternate boot mode access 0h: To stop alternate boot mode access
5	BOOT_ENABLE	R/W	0h	Boot Enable To start boot code access. 1h: To start boot code access 0h: To stop boot code access
4	RESERVED	R	0h	Reserved
3	INTRPT_AT_BLK_GAP	R/W	0h	Interrupt At Block Gap (SD Mode Only) This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1h enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0h. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card.

Table 14-24173. MMCSD1_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RDWAIT_CTRL	R/W	0h	Read Wait Control (SD Mode Only) The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1h otherwise DAT line conflict may occur. If this bit is set to 0h, Suspend/Resume cannot be supported. In UHS-II mode, Read Wait is disabled and DAT[2] line is used for Interrupt Signal from UHS-II Card. 1h: Enable Read Wait Control 0h: Disable Read Wait Control
1	CONTINUE	R/W	0h	Continue Request This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0h (MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 0h) and set this bit to restart the transfer. The Host Controller automatically clears this bit when the transaction re-starts. If MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h, any write to this bit is ignored. In SD mode, this bit is cleared in either of the following cases: 1) In the case of a read transaction, the DAT Line Active changes from 0h to 1h as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0h to 1h as the write transaction restarts. Therefore it is not necessary for Host driver to set this bit to 0h. If MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h, any write to this bit is ignored. 1h: Restart 0h: Ignored

Table 14-24173. MMCSD1_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	STOP_AT_BLK_GAP	R/W	0h	Stop At Block Gap Request This bit is used to stop executing a transaction at the next block gap for non-DMA, SDMA and ADMA transfers. Until the transfer complete is set to 1h, indicating a transfer completion the HD shall leave this bit set to 1h. Clearing both the MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP and MMCSD1_BLOCK_GAP_CONTROL[1] CONTINUE bits shall not cause the transaction to restart. The MMCSD1_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit is used to stop the read transaction at the block gap. The HC shall honour Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1h (MMCSD1_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL) = 1h). In case of write transfers in which the HD writes data to the MMCSD1_DATA_PORT register, the HD shall set this bit after all block data is written. If this bit is set to 1h, the HD shall not write data to the MMCSD1_DATA_PORT register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit (DAT) in the MMCSD1_PRESENTSTATE register. In case of UHS-II, a transaction can be stopped at the boundary of DATA Burst (Flow Control basis). Host Controller waits for sending Flow Control MSG until the MMCSD1_BLOCK_GAP_CONTROL[1] CONTINUE bit is set to 1h. 1h: Stop 0h: Transfer

There are three cases to restart the transfer after stop at the block gap. Which case is appropriate depends on whether the HC issues a Suspend command or the SD card accepts the Suspend command.

1. If the HD does not issue Suspend command, the Continue Request shall be used to restart the transfer.

2. If the HD issues a Suspend command and the SD card accepts it, a Resume Command shall be used to restart the transfer.

3. If the HD issues a Suspend command and the SD card does not accept it, the Continue Request shall be used to restart the transfer.

Any time Stop At Block Gap Request stops the data transfer, the HD shall wait for Transfer Complete (in the MMCSD1_NORMAL_INTR_STS register) before attempting to restart the transfer. When restarting the data transfer by Continue Request, the HD shall clear Stop At Block Gap Request before or simultaneously.

Host Controller should not generate timeout interrupts while Stop At Block Gap is set. Host Driver should ignore timeout interrupts while Stop At Block Gap is set.

15 MMCSD1_WAKEUP_CONTROL Register (Offset = 2Bh) [reset = 0h]

MMCSD1_WAKEUP_CONTROL is shown in Figure 14-7982 and described in Table 14-16194.

Return to Summary Table.

This register is used to program the wakeup functionality.

The MMCSD1_WAKEUP_CONTROL register is mandatory for the HC, but wakeup functionality depends on the HC system hardware and software. The HD shall maintain voltage on the SD Bus, by setting the MMCSD1_POWER_CONTROL[0] SD_BUS_POWER bit to 1h, when wakeup event via card interrupt is desired.

Table 14-24174. MMCSD1_WAKEUP_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 002Bh

Figure 14-7982. MMCSD1_WAKEUP_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED					CARD_REMOVAL	CARD_INSERTION	CARD_INTERRUPT
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24176. MMCSD1_WAKEUP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	CARD_REMOVAL	R/W	0h	Wakeup Event Enable On SD Card Removal This bit enables wakeup event via Card removal assertion in the MMCSD1_NORMAL_INTR_STS register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1h: Enable 0h: Disable
1	CARD_INSERTION	R/W	0h	Wakeup Event Enable On SD Card Insertion This bit enables wakeup event via Card Insertion assertion in the MMCSD1_NORMAL_INTR_STS register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1h: Enable 0h: Disable
0	CARD_INTERRUPT	R/W	0h	Wakeup Event Enable On Card Interrupt This bit enables wakeup event via Card Interrupt assertion in the MMCSD1_NORMAL_INTR_STS register. This bit can be set to 1h if FN_WUS (Wake Up Support) in CIS is set to 1h. 1h: Enable 0h: Disable

16 MMCSD1_CLOCK_CONTROL Register (Offset = 2Ch) [reset = 0h]

MMCSD1_CLOCK_CONTROL is shown in Figure 14-7983 and described in Table 14-16196.

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This register is used to program the Clock frequency select, Clock generator select, Clock enable, Internal clock state fields.

At the initialization of the HC, the HD shall set the SDCLK Frequency Select (MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL) according to the MMCSD1_CAPABILITIES register. This register controls SDCLK in SD Mode and RCLK in UHS-II mode.

Table 14-24177. MMCSD1_CLOCK_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 002Ch

Figure 14-7983. MMCSD1_CLOCK_CONTROL Register

15	14	13	12	11	10	9	8
SDCLK_FRQSEL							
R/W-0h							

7	6	5	4	3	2	1	0
SDCLK_FRQSEL_UPBITS		CLKGEN_SEL	RESERVED	PLL_ENA	SD_CLK_ENA	INT_CLK_STABLE	INT_CLK_ENA
R/W-0h		R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24179. MMCSD1_CLOCK_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	SDCLK_FRQSEL	R/W	0h	SDCLK/RCLK Frequency Select This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the Capabilities register (MMCSD1_CAPABILITIES[15-8] BASE_CLK_FREQ). Only the following settings are allowed. (1) 8-bit Divided Clock Mode: 80h: base clock divided by 256 40h: base clock divided by 128 20h: base clock divided by 64 10h: base clock divided by 32 08h: base clock divided by 16 04h: base clock divided by 8 02h: base clock divided by 4 01h: base clock divided by 2 00h: base clock (10 MHz - 63 MHz) Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The three default divider values can be calculated by the frequency that is defined by the MMCSD1_CAPABILITIES[15-8] BASE_CLK_FREQ bit field. 400 KHz divider value 25 MHz divider value 50 MHz divider value According to the Physical Layer Specification, the maximum SD Clock frequency is 25 MHz in normal speed mode and 50 MHz in high speed mode, and shall never exceed this limit. The frequency of SDCLK is set by the following formula: Clock Frequency = (Base Clock) / divisor Thus, choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. For example, if the MMCSD1_CAPABILITIES[15-8] BASE_CLK_FREQ bit field has the value 33 MHz, and the target frequency is 25 MHz, then choosing the divisor value of 1h will yield 16.5 MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400 KHz, the divisor value of 40h yields the optimal clock value of 258 KHz. (2) 10-bit Divided Clock Mode: Host Controller Version 3.00 or later supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits and all divider values shall be supported. 3FFh: 1/2046 Divided Clock

Table 14-24179. MMCSD1_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				N: 1/2N Divided Clock (Duty 50%) 002h: 1/4 Divided Clock 001h: 1/2 Divided Clock 000h: Base Clock (10 MHz - 254 MHz) (3) Programmable Clock Mode: Host Controller Version 3.00 or later supports this mode as optional. A non-zero value set to the MMCSD1_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field indicates support of this clock mode. The multiplier enables the Host System to select a finer grain SD clock frequency. It is not necessary to support all frequency generation specified by this field because programmable clock generator is vendor specific and dependent on the implementation. Therefore, this mode is used with Preset Value registers (MMCSD1_PRESET_VALUE0 - MMCSD1_PRESET_VALUE10). The Host Controller vendor provides possible settings and the Host System vendor sets appropriate values to the Preset Value registers (MMCSD1_PRESET_VALUE0 - MMCSD1_PRESET_VALUE10). 3FFh - Base Clock × M / 1024 .... N-1 - Base Clock × M / N .... 002h - Base Clock × M / 3 001h - Base Clock × M / 2 000h - Base Clock × M This field depends on setting of the MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this field is set by Host Driver. If MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this field is automatically set to a value specified in one of Preset Value registers (MMCSD1_PRESET_VALUE0 - MMCSD1_PRESET_VALUE10).
7-6	SDCLK_FRQSEL_UPBITS	R/W	0h	Upper Bits of SDCLK/RCLK Frequency Select This bit field is assigned to the MMCSD1_CLOCK_CONTROL[9-8] SDCLK_FRQSEL bit field of clock divider in SDCLK/RCLK Frequency Select.

Table 14-24179. MMCSD1_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLKGEN_SEL	R/W	0h	Clock Generator Select This bit is used to select the clock generator mode in SDCLK/ RCLK Frequency Select (MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL). If the Programmable Clock Mode is supported (non-zero value is set to the MMCSD1_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field), this bit attribute is R/W, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of the MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this bit is set by Host Driver. If MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this bit is automatically set to a value specified in one of Preset Value registers (MMCSD1_PRESET_VALUE0 - MMCSD1_PRESET_VALUE10). 1h: Programmable Clock Mode 0h: Divided Clock Mode
4	RESERVED	R	0h	Reserved
3	PLL_ENA	R/W	0h	PLL Enable This bit is added from Version 4.10 for Host Controller using PLL. This feature allows Host Controller to initialize clock generator in two steps: by Internal Clock Enable (MMCSD1_CLOCK_CONTROL[0] INT_CLK_ENA) and PLL Enable and to minimize output latency (for example SDCLK/RCLK, D0 lane) from SD Clock Enable (MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA). There are two modes to keep Host Drivers compatibility. In both modes, PLL Locked timing is indicated by Internal Clock Stable (MMCSD1_CLOCK_CONTROL[1] INT_CLK_STABLE). (1) When MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 0h (Host Driver Version 3, which does not support this bit) or this bit is not implemented, the MMCSD1_CLOCK_CONTROL[0] INT_CLK_ENA bit (or the MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA bit) may activate PLL (exit low power mode and start locking clock). (2) When MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 1h (Host Driver Version 4), the MMCSD1_CLOCK_CONTROL[0] INT_CLK_ENA bit is set before setting this bit and then setting this bit may activate PLL (exit low power mode and start locking clock). 1h: PLL is enabled 0h: PLL is in low power mode

Table 14-24179. MMCSD1_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SD_CLK_ENA	R/W	0h	SD Clock Enable The HC shall stop SDCLK when writing this bit to 0h. The MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field can be changed when this bit is 0h. Then, the HC shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK = 0). If the HC detects the No Card state, this bit shall be cleared. 1h: Enable providing SDCLK or RCLK 0h: Disable providing SDCLK or RCLK
1	INT_CLK_STABLE	R	0h	Internal Clock Stable This bit is set to 1h when SD clock is stable after writing 1h to MMCSD1_CLOCK_CONTROL[0] INT_CLK_ENA bit. The SD Host Driver shall wait to set the MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA bit until this bit is set to 1h. **Note:** This is useful when using PLL for a clock oscillator that requires setup time. (1) Internal Clock Stable (when MMCSD1_CLOCK_CONTROL[3] PLL_ENA = 0h or not supported) This bit is set to 1h when internal clock is stable after writing 1h to MMCSD1_CLOCK_CONTROL[0] INT_CLK_ENA bit. (2) PLL Clock Stable (when MMCSD1_CLOCK_CONTROL[3] PLL_ENA = 1h) Host Controller which supports PLL Enable sets this status to 0h once when PLL Enable is changed 0h to 1h and then this status is set to 1h when PLL is locked (PLL uses an internal clock in stable as a reference clock which is enabled by the MMCSD1_CLOCK_CONTROL[0] INT_CLK_ENA bit). After this bit is set to 1h, Host Driver may set the MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA bit. 1h: Ready 0h: Not Ready
0	INT_CLK_ENA	R/W	0h	Internal Clock Enable This bit is set to 0h when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1h. When clock oscillation is stable, the HC shall set the MMCSD1_CLOCK_CONTROL[1] INT_CLK_STABLE bit to 1h. This bit shall not affect card detection. 1h: Oscillate 0h: Stop

17 MMCSD1_TIMEOUT_CONTROL Register (Offset = 2Eh) [reset = 0h]

MMCSD1_TIMEOUT_CONTROL is shown in Figure 14-7984 and described in Table 14-16198.

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The register sets the data timeout counter value.

At the initialization of the HC, the HD shall set the Data Timeout Counter Value according to the MMCSD1_CAPABILITIES register.

Table 14-24180. MMCSD1_TIMEOUT_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 002Eh

Figure 14-7984. MMCSD1_TIMEOUT_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED				COUNTER_VALUE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-24182. MMCSD1_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	COUNTER_VALUE	R/W	0h	Data Timeout Counter Value This value determines the interval by which DAT line time-outs are detected. Refer to the MMCSD1_ERROR_INTR_STS[4] DATA_TIMEOUT bit for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the SD clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the MMCSD1_ERROR_INTR_STS[4] DATA_TIMEOUT bit. 1111: Reserved 1110: TMCLK × 2^{27} -------------------- -------------------- 0001: TMCLK × 2^{14} 0000: TMCLK × 2^{13}

18 MMCSD1_SOFTWARE_RESET Register (Offset = 2Fh) [reset = 0h]

MMCSD1_SOFTWARE_RESET is shown in Figure 14-7985 and described in Table 14-16200.

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This register is used to program the software reset for data, command and for all.

A reset pulse is generated when writing 1h to each bit of this register. After completing the reset, the HC shall clear each bit. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0h.

Table 14-24183. MMCSD1_SOFTWARE_RESET Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 002Fh

Figure 14-7985. MMCSD1_SOFTWARE_RESET Register

7	6	5	4	3	2	1	0
RESERVED					SWRST_FOR_DAT	SWRST_FOR_CMD	SWRST_FOR_ALL
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24185. MMCSD1_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved

Table 14-24185. MMCSD1_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SWRST_FOR_DAT	R/W	0h	Software Reset for DAT Line (SD Mode Only) Only part of data circuit is reset. The following registers and bits are cleared by this bit: MMCSD1_DATA_PORT Buffer is cleared and Initialized. MMCSD1_PRESENTSTATE Buffer read Enable Buffer write Enable Read Transfer Active Write Transfer Active DAT Line Active Command Inhibit (DAT) MMCSD1_BLOCK_GAP_CONTROL Continue Request Stop At Block Gap Request MMCSD1_NORMAL_INTR_ST Buffer Read Ready Buffer Write Ready Block Gap Event Transfer Complete 1h: Reset 0h: Work

Table 14-24185. MMCSD1_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SWRST_FOR_CMD	R/W	0h	Software Reset for CMD Line (SD Mode Only) Only part of command circuit is reset to be able to issue a command. From Version 4.10, this bit is also used to initialize UHS-II command circuit. This reset is effective only command issuing circuit (including response error statuses related to Command Inhibit (CMD) control - MMCSD1_PRESENTSTATE[0] INHIBIT_CMD bit) and does not affect data transfer circuit. Host Controller can continue data transfer even this reset is executed during handling of sub command response errors. The following registers and bits are cleared by this bit: MMCSD1_PRESENTSTATE register: Command Inhibit (CMD) MMCSD1_NORMAL_INTR_STS register: Command Complete MMCSD1_ERROR_INTR_STS register (Error Interrupt Status from Version 4.10) Response error statuses related to Command Inhibit (CMD) - MMCSD1_PRESENTSTATE[0] INHIBIT_CMD bit 1h: Reset 0h: Work
0	SWRST_FOR_ALL	R/W	0h	Software Reset for All This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0h. During its initialization, the HD shall set this bit to 1h to reset the HC. The HC shall reset this bit to 0h when Capabilities registers are valid and the HD can read them. Additional use of 'Software Reset For All' may not affect the value of the Capabilities registers. If this bit is set to 1h, the SD card shall reset itself and must be re-initialized by the HD. 1h: Reset 0h: Work

19 MMCSD1_NORMAL_INTR_STS Register (Offset = 30h) [reset = 0h]

MMCSD1_NORMAL_INTR_STS is shown in Figure 14-7986 and described in Table 14-16202.

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This register gives the status of all the interrupts.

The Normal Interrupt Signal Enable (see MMCSD1_NORMAL_INTR_SIG_ENA register) affects read of this register, but Normal Interrupt Signal does not affect these reads. An Interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1h. For all bits except Card Interrupt (MMCSD1_NORMAL_INTR_STS[8] CARD_INTR) and Error Interrupt (MMCSD1_NORMAL_INTR_STS[15] ERROR_INTR), writing 1h to a bit clears it. The MMCSD1_NORMAL_INTR_STS[8] CARD_INTR bit is cleared when the card stops asserting the interrupt: that is when the Card Driver services the Interrupt condition.

Table 14-24186. MMCSD1_NORMAL_INTR_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0030h

Figure 14-7986. MMCSD1_NORMAL_INTR_STS Register

15	14	13	12	11	10	9	8
ERROR_INTR	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTR
R-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REM	CARD_INS	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-24188. MMCSD1_NORMAL_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ERROR_INTR	R	0h	Error Interrupt If any of the bits in the MMCSD1_ERROR_INTR_STS register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. In UHS-II mode is enabled, if any of the bits in the MMCSD1_UHS2_ERR_INTR_STS register are set, this bit is also set. 0h: No Error 1h: Error
14	BOOT_COMPLETE	R/W1C	0h	Boot Terminate Interrupt This status is set if the boot operation gets terminated. 0h: Boot operation is not terminated 1h: Boot operation is terminated

Table 14-24188. MMCSD1_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RCV_BOOT_ACK	R/W1C	0h	Boot Acknowledge Receive This status is set if the boot acknowledge is received from device. 0h: Boot acknowledge is not received 1h: Boot acknowledge is received
12	RETUNING_EVENT	R	0h	Re-Tuning Event (UHS-I Only) This status is set if the MMCSD1_PRESENTSTATE[3] RETUNING_REQ bit changes from 0h to 1h. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. In UHS-II mode, this bit is not effective. 1h: Re-Tuning should be performed 0h: Re-Tuning is not required
11	INTC	R	0h	int_c (Embedded) This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_C interrupt factor.
10	INTB	R	0h	int_b (Embedded) This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_B interrupt factor.
9	INTA	R	0h	int_a (Embedded) This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_A interrupt factor.

Table 14-24188. MMCSD1_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CARD_INTR	R	0h	Card Interrupt When this status has been set and the Host Driver needs to start this interrupt service, the MMCSD1_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit may be set to 0h in order to clear the card interrupt status latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (it should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set the MMCSD1_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 1h and start sampling the interrupt signal again. Writing this bit to 1h does not clear this bit. It is cleared by resetting the SD card interrupt factor. (1) DAT[1] Interrupt Input in SD Mode In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of UHS-I mode, switching time of Interrupt Period is relaxed for 2 clock cycles. Then Host Controller needs to delay start of interrupt sampling at least 2 clocks and should sample interrupt while Interrupt Period is stable. (2) DAT[2] Interrupt Input in UHS-II Mode When the MMCSD1_PRESENTSTATE[16] CARD_INSERTED and MMCSD1_POWER_CONTROL[0] SD_BUS_POWER bits are set to 1h, Host Controller configures DAT[2] as Interrupt Input and enables pull-up of DAT[2]. DAT[2] interrupt is asynchronous to RCLK, low level sensitive and 3.3 V signal level. DAT[2] interrupt is masked by setting the MMCSD1_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 0h. When either the MMCSD1_PRESENTSTATE[16] CARD_INSERTED bit or the MMCSD1_POWER_CONTROL[0] SD_BUS_POWER bit is set to 0h, Host Controller sets DAT[2] to low. Only point to point connection is allowed between Host and Card. (3) INT MSG in UHS-II Mode INT MSG is enabled by setting the MMCSD1_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit. DAT[2] and INT MSG interrupt sources are ORed and indicated to Card Interrupt. If any bit in the MMCSD1_UHS2_DEVICE_INTR_STATUS register is set to 1h, INT MSG interrupt is generated. INT MSG interrupt is cleared by writing a correspondent bit to 1h in the MMCSD1_UHS2_DEVICE_INTR_STATUS register. Masking DAT[2] interrupt also disables INT MSG interupt due to the MMCSD1_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit is set to 0h. SDIO Version 4.00 does not support INT MSG. 1h: Generate Card Interrupt 0h: No Card Interrupt

Table 14-24188. MMCSD1_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CARD_REM	R/W1C	0h	Card Removal This status is set if the MMCSD1_PRESENTSTATE[16] CARD_INSERTED bit changes from 1h to 0h. When the HD writes this bit to 1h to clear this status the status of the MMCSD1_PRESENTSTATE[16] CARD_INSERTED bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0h: Card State Stable or Debouncing 1h: Card Removed
6	CARD_INS	R/W1C	0h	Card Insertion This status is set if the MMCSD1_PRESENTSTATE[16] CARD_INSERTED bit changes from 0h to 1h. When the HD writes this bit to 1h to clear this status the status of the MMCSD1_PRESENTSTATE[16] CARD_INSERTED bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0h: Card State Stable or Debouncing 1h: Card Inserted
5	BUF_RD_READY	R/W1C	0h	Buffer Read Ready This status is set if the MMCSD1_PRESENTSTATE[11] BUF_RD_ENA bit changes from 0h to 1h. The MMCSD1_PRESENTSTATE[11] BUF_RD_ENA bit is set to 1h for every CMD19 execution in tuning procedure. In UHS-II mode, this bit is set at FC (Flow Control) unit basis. 0h: Not Ready to read Buffer 1h: Ready to read Buffer
4	BUF_WR_READY	R/W1C	0h	Buffer Write Ready This status is set if the MMCSD1_PRESENTSTATE[10] BUF_WR_ENA bit changes from 0h to 1h. In UHS-II mode, this bit is set at FC (Flow Control) unit basis. 0h: Not Ready to Write Buffer 1h: Ready to Write Buffer
3	DMA_INTERRUPT	R/W1C	0h	DMA Interrupt This status is set if the HC detects the Host DMA Buffer Boundary in the MMCSD1_BLOCK_SIZE regiser. 0h: No DMA Interrupt 1h: DMA Interrupt is Generated

Table 14-24188. MMCSD1_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BLK_GAP_EVENT	R/W1C	0h	Block Gap Event If the MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set, this bit is set. Read Transaction: This bit is set at the falling edge of the DAT Line Active Status (see MMCSD1_PRESENTSTATE[2] DATA_LINE_ACTIVE bit). When the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function. Write Transaction: This bit is set at the falling edge of Write Transfer Active Status (see MMCSD1_PRESENTSTATE[8] WR_XFER_ACTIVE bit). After getting CRC status at SD Bus timing. In UHS-II mode, this bit is set at FC (Flow Control) unit basis. 0h: No Block Gap Event 1h: Transaction stopped at Block Gap

Table 14-24188. MMCSD1_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XFER_COMPLETE	R/W1C	0h	Transfer Complete This bit is set when a read/write transaction is completed. **SD Mode** Read Transaction: This bit is set at the falling edge of Read Transfer Active Status (MMCSD1_PRESENTSTATE[9] RD_XFER_ACTIVE). There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length (after the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit (after valid data has been read to the Host System). Write Transaction: This bit is set at the falling edge of the DAT Line Active Status (see MMCSD1_PRESENTSTATE[2] DATA_LINE_ACTIVE bit). There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting the MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and data transfers completed (after valid data is written to the SD card and the busy signal is released). **Note:** MMCSD1_NORMAL_INTR_STS[1] XFER_COMPLETE bit has higher priority than the MMCSD1_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If both bits are set to 1h, the data transfer can be considered complete. **Note:** While performing tuning procedure (the MMCSD1_HOST_CONTROL2[6] EXECUTE_TUNING bit is set to 1h), the MMCSD1_NORMAL_INTR_STS[1] XFER_COMPLETE bit is not set to 1h. Command with Busy: This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit (DAT) in the MMCSD1_PRESENTSTATE register. **UHS-I mode** While performing tuning procedure (the MMCSD1_HOST_CONTROL2[6] EXECUTE_TUNING bit is set to 1h), the MMCSD1_NORMAL_INTR_STS[1] XFER_COMPLETE bit is not set to 1h. 0h: No Data Transfer Complete 1h: Data Transfer Complete **UHS-II Mode** This interrupt is generated in following two cases: (a) EBSY Completion (for EBSY supported commands)

Table 14-24188. MMCSD1_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				When the MMCSD1_UHS2_XFER_MODE[14] EBSY_WAIT bit is set to 1h, this bit is set when EBSY packet has been received, and all valid data have been sent to system memory in case of read operation. (b) Stop and Continue during DCMD Data Transfer When the MMCSD1_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1h and data transfer is stopped at the Flow Control. Following is for both SD mode and UHS-II mode. The table below shows that the MMCSD1_NORMAL_INTR_STS[1] XFER_COMPLETE bit has higher priority than the MMCSD1_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If both bits are set to 1h, execution of a command can be considered to be completed. 1h: Command execution is completed 0h: Not complete
0	CMD_COMPLETE	R/W1C	0h	Command Complete **SD Mode** This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23). **Note:** The MMCSD1_ERROR_INTR_STS[0] CMD_TIMEOUT bit has higher priority than the MMCSD1_NORMAL_INTR_STS[0] CMD_COMPLETE bit. If both are set to 1h, it can be considered that the response was not received correctly. Version 4.00 defines response check function for R1 and R5. If the MMCSD1_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1h, generation of this interrupt is prohibited regardless of the MMCSD1_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit. **UHS-II Mode** If the MMCSD1_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 0h, this interrupt is generated when response packet is received. If the MMCSD1_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1h, generation of this interrupt is prohibited regardless of the MMCSD1_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit. 0h: No Command Complete 1h: Command Complete

Table 14-16203 shows the relation between transfer complete and data timeout error.

Table 14-24189. Relation between transfer complete and data timeout error

Transfer Complete	Data Timeout Error	Meaning of the Status
0	0	Interrupted by Another Factor
0	1	Timeout occur during transfer
1	Don't Care	Data Transfer Complete

Table 14-16204 shows the relation between command complete and command timeout error.

Table 14-24190. Relation between command complete and command timeout error

Command Complete	Command Timeout Error	Meaning of the Status
0	0	Interrupted by Another Factor
Don't Care	1	Response not received within 64 SDCLK cycles
1	0	Response Received

20 MMCSD1_ERROR_INTR_STS Register (Offset = 32h) [reset = 0h]

MMCSD1_ERROR_INTR_STS is shown in Figure 14-7987 and described in Table 14-16206.

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This register gives the status of the error interrupts.

Status defined in this register can be enabled by the MMCSD1_ERROR_INTR_STS_ENA register, but not by the MMCSD1_ERROR_INTR_SIG_ENA register. The Interrupt is generated when the MMCSD1_ERROR_INTR_SIG_ENA register is enabled and at least one of the statuses is set to 1h. Writing to 1h clears the bit and writing to 0h keeps the bit unchanged. More than one status can be cleared at the one register write.

Table 14-24191. MMCSD1_ERROR_INTR_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0032h

Figure 14-7987. MMCSD1_ERROR_INTR_STS Register

15	14	13	12	11	10	9	8
RESERVED			HOST	RESP	RESERVED	ADMA	AUTO_CMD
R-0h			R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-24193. MMCSD1_ERROR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	HOST	R/W1C	0h	Target Response Error Occurs when detecting ERROR in m_hresp (DMA transaction) 0h: No error 1h: Error
11	RESP	R/W1C	0h	Response Error (SD Mode Only) Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If the MMCSD1_TRANSFER_MODE[7] RESP_ERR_CHK_ENA bit is set to 1h, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1h. 0h: No error 1h: Error
10	RESERVED	R	0h	Reserved

Table 14-24193. MMCSD1_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ADMA	R/W1C	0h	ADMA Error This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the MMCSD1_ADMA_ERR_STATUS register. 0h: No error 1h: Error
8	AUTO_CMD	R/W1C	0h	Auto CMD Error (SD Mode Only) Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that any of the bits D00 to D05 in the MMCSD1_AUTOCMD_ERR_STS register has changed from 0h to 1h. D07 is effective in case of Auto CMD12. The MMCSD1_AUTOCMD_ERR_STS register is valid while this bit is set to 1h and may be cleared with clearing of this bit (another implementation is also allowed). 0h: No error 1h: Error
7	CURR_LIMIT	R/W1C	0h	Current Limit Error By setting the MMCSD1_POWER_CONTROL[0] SD_BUS_POWER bit, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1h means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function. 0h: No error 1h: Power Fail
6	DATA_ENDBIT	R/W1C	0h	Data End Bit Error (SD Mode Only) Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0h: No error 1h: Error
5	DATA_CRC	R/W1C	0h	Data CRC Error (SD Mode Only) Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 2h. 0h: No error 1h: Error

Table 14-24193. MMCSD1_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DATA_TIMEOUT	R/W1C	0h	Data Timeout Error (SD Mode Only) Occurs when detecting one of following timeout conditions: 1. Busy Timeout for R1b, R5b type 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0h: No error 1h: Timeout
3	CMD_INDEX	R/W1C	0h	Command Index Error (SD Mode Only) Occurs if a Command Index error occurs in the Command Response (MMCSD1_RESPONSE_0 to MMCSD1_RESPONSE_7). 0h: No error 1h: Error
2	CMD_ENDBIT	R/W1C	0h	Command End Bit Error (SD Mode Only) Occurs when detecting that the end bit of a command response is 0h. 0h: No error 1h: End Bit Error Generated
1	CMD_CRC	R/W1C	0h	Command CRC Error (SD Mode Only) Command CRC Error is generated in two cases. 1. If a response is returned and the MMCSD1_ERROR_INTR_STS[0] CMD_TIMEOUT bit is set to 0h, this bit is set to 1h when detecting a CRT error in the command response. 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (Stop driving CMD line) and set this bit to 1h. The MMCSD1_ERROR_INTR_STS[0] CMD_TIMEOUT bit shall also be set to 1h to distinguish CMD line conflict. 0h: No error 1h: CRC Error Generated

Table 14-24193. MMCSD1_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMD_TIMEOUT	R/W1C	0h	Command Timeout Error (SD Mode Only) Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case the MMCSD1_ERROR_INTR_STS[1] CMD_CRC bit shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. 0h: No error 1h: Timeout

Table 14-16207 shows the relation between command CRC error and command time-out error.

Table 14-24194. Relation between command CRC error and command time-out error

Command CRC Error	Command Time-out Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD Line Conflict

21 MMCSD1_NORMAL_INTR_STS_ENA Register (Offset = 34h) [reset = 0h]

MMCSD1_NORMAL_INTR_STS_ENA is shown in Figure 14-7988 and described in Table 14-16209.

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This register is used to enable the MMCSD1_NORMAL_INTR_STS register fields.

Table 14-24195. MMCSD1_NORMAL_INTR_STS_ENA Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0034h

Figure 14-7988. MMCSD1_NORMAL_INTR_STS_ENA Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24197. MMCSD1_NORMAL_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	Fixed to 0 The HC shall control error Interrupts using the MMCSD1_ERROR_INTR_STS_ENA register.
14	BOOT_COMPLETE	R/W	0h	Boot Terminate Interrupt Enable 0h: Masked 1h: Enabled
13	RCV_BOOT_ACK	R/W	0h	Boot Acknowledge Enable 0h: Masked 1h: Enabled
12	RETUNING_EVENT	R/W	0h	Re-Tuning Event Status Enable (UHS-I Only) 0h: Masked 1h: Enabled
11	INTC	R/W	0h	INT_C Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts.

Table 14-24197. MMCSD1_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INTB	R/W	0h	INT_B Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts.
9	INTA	R/W	0h	INT_A Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts.
8	CARD_INTERRUPT	R/W	0h	Card Interrupt Status Enable If this bit is set to 0h, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1h. The HD may clear the MMCSD1_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. By setting this bit to 0h, interrupt input should be masked by implementation so that the interrupt Input is not affected by external signal in any state (for example: floating). 0h: Masked 1h: Enabled
7	CARD_REMOVAL	R/W	0h	Card Removal Status Enable 0h: Masked 1h: Enabled
6	CARD_INSERTION	R/W	0h	Card Insertion Status Enable 0h: Masked 1h: Enabled
5	BUF_RD_READY	R/W	0h	Buffer Read Ready Status Enable 0h: Masked 1h: Enabled
4	BUF_WR_READY	R/W	0h	Buffer Write Ready Status Enable 0h: Masked 1h: Enabled
3	DMA_INTERRUPT	R/W	0h	DMA Interrupt Status Enable 0h: Masked 1h: Enabled

Table 14-24197. MMCSD1_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BLK_GAP_EVENT	R/W	0h	Block Gap Event Status Enable 0h: Masked 1h: Enabled
1	XFER_COMPLETE	R/W	0h	Transfer Complete Status Enable 0h: Masked 1h: Enabled
0	CMD_COMPLETE	R/W	0h	Command Complete Status Enable 0h: Masked 1h: Enabled

Note: The HC may sample the card Interrupt signal during interrupt period and may hold its value in the flip-flop. If the MMCSD1_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit is set to 0h, the HC shall clear all internal signals regarding Card Interrupt (MMCSD1_NORMAL_INTR_STS[8] CARD_INTR).

22 MMCSD1_ERROR_INTR_STS_ENA Register (Offset = 36h) [reset = 0h]

MMCSD1_ERROR_INTR_STS_ENA is shown in Figure 14-7989 and described in Table 14-16211.

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This register is used to enable the MMCSD1_ERROR_INTR_STS register fields.

Table 14-24198. MMCSD1_ERROR_INTR_STS_ENA Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0036h

Figure 14-7989. MMCSD1_ERROR_INTR_STS_ENA Register

15	14	13	12	11	10	9	8
VENDOR_SPECIFIC				RESP	TUNING	ADMA	AUTO_CMD
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24200. MMCSD1_ERROR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Status Enable N/A
11	RESP	R/W	0h	Response Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
10	TUNING	R/W	0h	Tuning Error Status Enable (UHS-I Only) 0h: Masked 1h: Enabled
9	ADMA	R/W	0h	ADMA Error Status Enable 0h: Masked 1h: Enabled
8	AUTO_CMD	R/W	0h	Auto CMD Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
7	CURR_LIMIT	R/W	0h	Current Limit Error Status Enable 0h: Masked 1h: Enabled

Table 14-24200. MMCSD1_ERROR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DATA_ENDBIT	R/W	0h	Data End Bit Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
5	DATA_CRC	R/W	0h	Data CRC Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
4	DATA_TIMEOUT	R/W	0h	Data Timeout Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
3	CMD_INDEX	R/W	0h	Command Index Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
2	CMD_ENDBIT	R/W	0h	Command End Bit Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
1	CMD_CRC	R/W	0h	Command CRC Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
0	CMD_TIMEOUT	R/W	0h	Command Timeout Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled

Note: To Detect CMD Line conflict, the HD must set both MMCSD1_ERROR_INTR_STS_ENA[0] CMD_TIMEOUT and MMCSD1_ERROR_INTR_STS_ENA[1] CMD_CRC bits to 1h.

23 MMCSD1_NORMAL_INTR_SIG_ENA Register (Offset = 38h) [reset = 0h]

MMCSD1_NORMAL_INTR_SIG_ENA is shown in Figure 14-7990 and described in Table 14-16213.

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Normal Interrupt Signal Enable Register

This register is used to select which interrupt status is indicated to the Host System as the Interrupt. These status bits all share the sample 1 bit interrupt line. Setting any of these bits to 1h enables Interrupt generation.

Table 14-24201. MMCSD1_NORMAL_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0038h

Figure 14-7990. MMCSD1_NORMAL_INTR_SIG_ENA Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24203. MMCSD1_NORMAL_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	Fixed to 0 The HD shall control error Interrupts using the MMCSD1_ERROR_INTR_SIG_ENA register.
14	BOOT_COMPLETE	R/W	0h	Boot Terminate Interrupt Signal Enable 0h: Masked 1h: Enabled
13	RCV_BOOT_ACK	R/W	0h	Boot Acknowledge Receive Signal Enable 0h: Masked 1h: Enabled
12	RETUNING_EVENT	R/W	0h	Re-Tuning Event Signal Enable (UHS-I Only) 0h: Masked 1h: Enabled
11	INTC	R/W	0h	INT_C Signal Enable (Embedded) 0h: Masked 1h: Enabled

Table 14-24203. MMCSD1_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INTB	R/W	0h	INT_B Signal Enable (Embedded) 0h: Masked 1h: Enabled
9	INTA	R/W	0h	INT_A Signal Enable (Embedded) 0h: Masked 1h: Enabled
8	CARD_INTERRUPT	R/W	0h	Card Interrupt Signal Enable 0h: Masked 1h: Enabled
7	CARD_REMOVAL	R/W	0h	Card Removal Signal Enable 0h: Masked 1h: Enabled
6	CARD_INSERTION	R/W	0h	Card Insertion Signal Enable 0h: Masked 1h: Enabled
5	BUF_RD_READY	R/W	0h	Buffer Read Ready Signal Enable 0h: Masked 1h: Enabled
4	BUF_WR_READY	R/W	0h	Buffer Write Ready Signal Enable 0h: Masked 1h: Enabled
3	DMA_INTERRUPT	R/W	0h	DMA Interrupt Signal Enable 0h: Masked 1h: Enabled
2	BLK_GAP_EVENT	R/W	0h	Block Gap Event Signal Enable 0h: Masked 1h: Enabled
1	XFER_COMPLETE	R/W	0h	Transfer Complete Signal Enable 0h: Masked 1h: Enabled
0	CMD_COMPLETE	R/W	0h	Command Complete Signal Enable 0h: Masked 1h: Enabled

24 MMCSD1_ERROR_INTR_SIG_ENA Register (Offset = 3Ah) [reset = 0h]

MMCSD1_ERROR_INTR_SIG_ENA is shown in Figure 14-7991 and described in Table 14-16215.

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Error Interrupt Signal Enable Register

This register is used to select which interrupt status is notified to the Host System as the Interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1h enables Interrupt generation.

Table 14-24204. MMCSD1_ERROR_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 003Ah

Figure 14-7991. MMCSD1_ERROR_INTR_SIG_ENA Register

15	14	13	12	11	10	9	8
VENDOR_SPECIFIC				RESP	TUNING	ADMA	AUTO_CMD
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24206. MMCSD1_ERROR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Signal Enable N/A
11	RESP	R/W	0h	Response Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
10	TUNING	R/W	0h	Tuning Error Signal Enable (UHS-I Only) 0h: Masked 1h: Enabled
9	ADMA	R/W	0h	ADMA Error Signal Enable 0h: Masked 1h: Enabled
8	AUTO_CMD	R/W	0h	Auto CMD Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
7	CURR_LIMIT	R/W	0h	Current Limit Error Signal Enable 0h: Masked 1h: Enabled

Table 14-24206. MMCSD1_ERROR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DATA_ENDBIT	R/W	0h	Data End Bit Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
5	DATA_CRC	R/W	0h	Data CRC Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
4	DATA_TIMEOUT	R/W	0h	Data Timeout Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
3	CMD_INDEX	R/W	0h	Command Index Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
2	CMD_ENDBIT	R/W	0h	Command End Bit Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
1	CMD_CRC	R/W	0h	Command CRC Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
0	CMD_TIMEOUT	R/W	0h	Command Timeout Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled

25 MMCSD1_AUTOCMD_ERR_STS Register (Offset = 3Ch) [reset = 0h]

MMCSD1_AUTOCMD_ERR_STS is shown in Figure 14-7992 and described in Table 14-16217.

Return to Summary Table.

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD23.

The Host driver can determine what kind of Auto CMD12/CMD23 errors occur by this register. Auto CMD23 errors are indicated in bit 04-01. This register is valid only when the Auto CMD Error is set.

Table 14-24207. MMCSD1_AUTOCMD_ERR_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 003Ch

Figure 14-7992. MMCSD1_AUTOCMD_ERR_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
CMD_NOT_ISSUED	RESERVED		INDEX	ENDBIT	CRC	TIMEOUT	ACMD12_NOT_EXEC
R-0h	R-0h		R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24209. MMCSD1_AUTOCMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMD_NOT_ISSUED	R	0h	Command Not Issued By Auto CMD12 Error Setting this bit to 1h means CMD_wo_DAT is not executed due to an Auto CMD12 error (D04- D01) in this register. This bit is set to 0h when Auto CMD Error is generated by Auto CMD23. 0h: No Error 1h: Not Issued
6-5	RESERVED	R	0h	Reserved
4	INDEX	R	0h	Auto CMD Index Error Occurs if the Command Index error occurs in response to a command. 0h: No Error 1h: Error

Table 14-24209. MMCSD1_AUTOCMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ENDBIT	R	0h	Auto CMD End Bit Error Occurs when detecting that the end bit of command response is 0h. 0h: No Error 1h: End Bit Error Generated
2	CRC	R	0h	Auto CMD CRC Error Occurs when detecting a CRC error in the command response. 0h: No Error 1h: CRC Error Generated
1	TIMEOUT	R	0h	Auto CMD Timeout Error Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1h, the other error status bits (D04 - D02) are meaningless. 0h: No Error 1h: Timeout
0	ACMD12_NOT_EXEC	R	0h	Auto CMD12 not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1h means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1h, other error status bits (D04 - D01) are meaningless. This bit is set to 0h when Auto CMD Error is generated by Auto CMD23. 0h: Executed 1h: Not Executed

Table 14-16218 shows the relation between Auto CMD12 CRC error and Auto CMD12 timeout error.

Table 14-24210. Relation between Auto CMD12 CRC Error and Auto CMD12 Timeout Error

Auto Cmd12 CRC Error	Auto CMD12 Timeout Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD Line Conflict

The timing of changing Auto CMD12 Error Status can be classified in three scenarios:

1. When the HC is going to issue Auto CMD12:

Set D00 to 1h if Auto CMD12 cannot be issued due to an error in the previous command.

Set D00 to 0h if Auto CMD12 is issued.

2. At the end bit of Auto CMD12 response:

Check received responses by checking the error bits D01, D02, D03, D04.

set to 1h if Error is Detected.

set to 0h if Error is Not Detected.

3. Before reading the Auto CMD12 Error Status bit D07:

Set D07 to 1h if there is a command cannot be issued.

Set D07 to 0h if there is no command to issue.

Timing of generating the Auto CMD12 Error and writing to the MMCSD1_COMMAND register are Asynchronous. Then D07 shall be sampled when driver never writing to the MMCSD1_COMMAND register. So just before reading the MMCSD1_AUTOCMD_ERR_STS register is good timing to set the D07 status bit.

26 MMCSD1_HOST_CONTROL2 Register (Offset = 3Eh) [reset = 0h]

MMCSD1_HOST_CONTROL2 is shown in Figure 14-7993 and described in Table 14-16220.

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This register is used to program UHS Mode Select, Driver Strength Select, Execute Tuning, Sampling Clock Select, Asynchronous Interrupt Enable and Preset Value Enable.

Table 14-24211. MMCSD1_HOST_CONTROL2 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 003Eh

Figure 14-7993. MMCSD1_HOST_CONTROL2 Register

15	14	13	12	11	10	9	8
PRESET_VALUE_ENA	ASYNCH_INTR_ENA	BIT64_ADDRESSING	HOST_VER40_ENA	CMD23_ENA	ADMA2_LEN_MODE	DRIVER_STRENGTH2	UHS2_INTF_ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPLING_CLK_SELECT	EXECUTE_TUNING	DRIVER_STRENGTH1		V1P8_SIGNAL_ENA	UHS_MODE_SELECT		
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24213. MMCSD1_HOST_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PRESET_VALUE_ENA	R/W	0h	Preset Value Enable Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When the MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to automatic. This bit enables the functions defined in the Preset Value registers (MMCSD1_PRESET_VALUE0 - MMCSD1_PRESET_VALUE10). If this bit is set to 0h, SDCLK Frequency Select, Clock Generator Select in the MMCSD1_CLOCK_CONTROL register and Driver Strength Select in the MMCSD1_HOST_CONTROL2 register are set by Host Driver. If this bit is set to 1h, SDCLK Frequency Select, Clock Generator Select in the MMCSD1_CLOCK_CONTROL register and Driver Strength Select in the MMCSD1_HOST_CONTROL2 register are set by Host Controller as specified in the Preset Value registers (MMCSD1_PRESET_VALUE0 - MMCSD1_PRESET_VALUE10). 0h: SDCLK and Driver Strength are controlled by Host Driver 1h: Automatic Selection by Preset Value are Enabled

Table 14-24213. MMCSD1_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ASYNCH_INTR_ENA	R/W	0h	Asynchronous Interrupt Enable This bit can be set to 1h if a card support asynchronous interrupt and the MMCSD1_CAPABILITIES[29] ASYNCH_INTR_SUPPORT bit is set to 1h. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode . If this bit is set to 1h, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 0h: Disabled 1h: Enabled
13	BIT64_ADDRESSING	R/W	0h	64-bit Addressing This field is effective when the MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h. Host Controller selects either of 32-bit or 64-bit addressing modes to access system memory. Whether 32-bit or 64-bit is determined by OS installed in a host system. Host Driver sets this bit depends on addressing mode of installed OS. Refer to 64-bit System Address Support in the MMCSD1_CAPABILITIES register. 0h: 32-bits Addressing 1h: 64-bits Addressing

Table 14-24213. MMCSD1_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	HOST_VER40_ENA	R/W	0h	Host Version 4 Enable This bit selects either Version 3.00 compatible mode or Version 4.00 mode. In Version 4.00, support of 64-bit System Addressing is modified. All DMAs support 64-bit System Addressing. UHS-II supported Host Driver shall enable this bit. In Version 4.10, supported 32-bit Block Count for all operations. Functions of following fields are modified. **SDMA Address** SDMA uses the MMCSD1_ADMA_SYS_ADDRESS register instead of SDMA System Address register (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI) **ADMA2/ADMA3 Selection** ADMA3 is selected by MMCSD1_HOST_CONTROL1[4-3] DMA_SELECT bit. **64-bit ADMA Descriptor Size** 128-bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1h. **Selection of 32-bit/64-bit System Addressing** Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register instead of MMCSD1_HOST_CONTROL1[4-3] DMA_SELECT bit. **32-bit Block Count** SDMA System Address register (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI) is modified to 32-bit Block Count register. 0h: Version 3.00 Compatible Mode 1h: Version 4.Mode
11	CMD23_ENA	R/W	0h	CMD23 Enable In memory card initialization, Host Driver Version 4.10 checks whether card supports CMD23 by checking a bit SCR[33]. If the card supports CMD23 (SCR[33] = 1h), this bit is set to 1h. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 datatransfer. Refer to MMCSD1_TRANSFER_MODE[3-2] AUTO_CMD_ENA bit.
10	ADMA2_LEN_MODE	R/W	0h	ADMA2 Length Mode This bit selects one of ADMA2 Length Modes either 16-bit or 26-bit. 0h: 16-bit Data Length Mode 1h: 26-bit Data Length Mode
9	DRIVER_STRENGTH2	R/W	0h	Driver Strength Select This is the programmed Drive Strength output and Bit[2] of the sdhccore_drivestrength value.

Table 14-24213. MMCSD1_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	UHS2_INTF_ENABLE	R/W	0h	UHS-II Interface Enable This bit is used to enable UHS-II Interface. Before trying to start UHS-II initialization, this bit shall be set to 1h. Before trying to start SD mode initialization, this bit shall be set to 0h. This bit is used to enable UHS-II IF Detection, Lane Synchronization and In Dormant State in the MMCSD1_PRESENTSTATE register, and to select clock source of either SD mode or UHS-II mode. Host Controller shall not leave unused SD 4-bit Interface lines (CLK, CMD and DAT[3:2]) floating in UHS-II mode by using pull-up or driving to low. When DAT[2] is used as interrupt input in UHS-II mode, DAT[2] of Host Controller is set to input and then DAT[2] of SDIO card is set to output to avoid conflict. 0h: 4-bit SD Interface Enabled 1h: UHS-II Interface Enabled
7	SAMPLING_CLK_SELECT	R/W	0h	Sampling Clock Select (UHS-I Only) This bit is set by tuning procedure when the MMCSD1_HOST_CONTROL2[6] EXECUTE_TUNING bit is cleared. Writing 1h to this bit is meaningless and ignored. Setting 1h means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0h. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. 0h: Fixed clock is used to sample data 1h: Tuned clock is used to sample data
6	EXECUTE_TUNING	R/W	0h	Execute Tuning (UHS-I Only) This bit is set to 1h to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to the MMCSD1_HOST_CONTROL2[7] SAMPLING_CLK_SELECT bit. Tuning procedure is aborted by writing 0h for more detail about tuning procedure. 0h: Not Tuned or Tuning Completed 1h: Execute Tuning

Table 14-24213. MMCSD1_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	DRIVER_STRENGTH1	R/W	0h	Driver Strength Select (UHS-I Only) Host Controller output driver in 1.8 V signaling is selected by this bit. In 3.3 V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the MMCSD1_CAPABILITIES register. This bit depends on setting of the MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this field is set by Host Driver. If MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this field is automatically set by a value specified in the one of Preset Value registers (MMCSD1_PRESET_VALUE0 - MMCSD1_PRESET_VALUE10). 0h: Driver Type B is Selected (Default) 1h: Driver Type A is Selected 2h: Driver Type C is Selected 3h: Driver Type D is Selected
3	V1P8_SIGNAL_ENA	R/W	0h	1.8 V Signaling Enable (UHS-I Only) This bit controls voltage regulator for I/O cell. 3.3 V is supplied to the card regardless of signaling voltage. Setting this bit from 0h to 1h starts changing signal voltage from 3.3 V to 1.8 V. 1.8 V regulator output shall be stable within 5 ms. Host Controller clears this bit if switching to 1.8 V signaling fails. Clearing this bit from 1h to 0h starts changing signal voltage from 1.8 V to 3.3 V. 3.3 V regulator output shall be stable within 5 ms. Host Driver can set this bit to 1h when Host Controller supports 1.8 V signaling (one of support bits is set to 1h: SDR50, SDR104 or DDR50 in the MMCSD1_CAPABILITIES register) and the card or device supports UHS-I. 0h: 3.3 V Signaling 1h: 1.8 V Signaling

Table 14-24213. MMCSD1_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	UHS_MODE_SELECT	R/W	0h	UHS Mode Select (UHS-I Only) This field is used to select one of UHS-I modes or UHS-II mode. In case of UHS-I mode, this field is effective when the MMCSD1_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit is set to 1h. In case of UHS-II mode, the MMCSD1_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit shall be set to 0h. Setting of this field is used to select one of preset values in UHS-I or UHS-II mode. If the MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA is set to 1h,Host Controller sets SDCLK/RCLK Frequency Select, Clock Generator Select in the MMCSD1_CLOCK_CONTROL register and Driver Strength Select according to Preset Value registers (MMCSD1_PRESET_VALUE0 - MMCSD1_PRESET_VALUE10). In this case, one of preset value registers is selected by this field. Host Driver needs to reset the MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA bit before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets the MMCSD1_CLOCK_CONTROL[2] SD_CLK_ENA bit again. 0h: SDR12 1h: SDR25 2h: SDR50 3h: SDR104 4h: DDR50 5h: HS400 6h: Reserved 7h: UHS-II When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more details.

27 MMCSD1_CAPABILITIES Register (Offset = 40h) [reset = 180004073FE8C801h]

MMCSD1_CAPABILITIES is shown in Figure 14-7994 and described in Table 14-16222.

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This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initialization.

Table 14-24214. MMCSD1_CAPABILITIES Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0040h

Figure 14-7994. MMCSD1_CAPABILITIES Register

63	62	61	60	59	58	57	56
HS400_SUPPORT	RESERVED		VDD2_1P8_SUPPORT	ADMA3_SUPPORT	RESERVED	SPI_BLK_MODE	SPI_SUPPORT
R-0h	R-0h		R-1h	R-1h	R-0h	R-0h	R-0h
55	54	53	52	51	50	49	48
CLOCK_MULTIPLIER							
R-0h							
47	46	45	44	43	42	41	40
RETUNING_MODES		TUNING_FOR_SDR50	RESERVED	RETUNING_TIMER_CNT			
R-0h		R-0h	R-0h	R-4h			
39	38	37	36	35	34	33	32
RESERVED	DRIVERD_SUPPORT	DRIVERC_SUPPORT	DRIVERA_SUPPORT	UHS2_SUPPORT	DDR50_SUPPORT	SDR104_SUPPORT	SDR50_SUPPORT
R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-1h
31	30	29	28	27	26	25	24
SLOT_TYPE		ASYNCH_INTR_SUPPORT	ADDR_64BIT_SUPPORT_V3	ADDR_64BIT_SUPPORT_V4	VOLT_1P8_SUPPORT	VOLT_3P0_SUPPORT	VOLT_3P3_SUPPORT
R-0h		R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
23	22	21	20	19	18	17	16
SUSP_RES_SUPPORT	SDMA_SUPPORT	HIGH_SPEED_SUPPORT	RESERVED	ADMA2_SUPPORT	BUS_8BIT_SUPPORT	MAX_BLK_LENGTH	
R-1h	R-1h	R-1h	R-0h	R-1h	R-0h	R-0h	
15	14	13	12	11	10	9	8
BASE_CLK_FREQ							
R-C8h							
7	6	5	4	3	2	1	0
TIMEOUT_CLK_UNIT	RESERVED	TIMEOUT_CLK_FREQ					
R-0h	R-0h	R-1h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24216. MMCSD1_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
63	HS400_SUPPORT	R	0h	HS400 Support 0h: HS400 is Not Supported 1h: HS400 is Supported
62-61	RESERVED	R	0h	Reserved
60	VDD2_1P8_SUPPORT	R	1h	1.8 V VDD2 Support This bit indicates that support of VDD2 on Host system. 0h: 1.8 V VDD2 is not supported 1h: 1.8 V VDD2 is supported
59	ADMA3_SUPPORT	R	1h	ADMA3 Support This bit indicates that support of ADMA3 on Host Controller. 0h: ADMA3 is not supported 1h: ADMA3 is supported
58	RESERVED	R	0h	Reserved
57	SPI_BLK_MODE	R	0h	SPI Block Mode This bit indicates whether SPI Block Mode is supported or not. 0h: Not Supported 1h: Supported
56	SPI_SUPPORT	R	0h	SPI Mode This bit indicates whether SPI Mode is supported or not. 0h: Not Supported 1h: Supported
55-48	CLOCK_MULTIPLIER	R	0h	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to the MMCSD1_CLOCK_CONTROL register. Setting 00h means that Host Controller does not support programmable clock generator. FFh: Clock Multiplier M = 256 ---- 02h: Clock Multiplier M = 3 01h: Clock Multiplier M = 2 00h: Clock Multiplier is Not Supported

Table 14-24216. MMCSD1_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
47-46	RETUNING_MODES	R	0h	Re-tuning Modes (UHS-I Only) This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver. 0h: Mode 1 1h: Mode 2 2h: Mode 3 3h: Reserved There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.
45	TUNING_FOR_SDR50	R	0h	Use Tuning for SDR50 (UHS-I Only) If this bit is set to 1h, this Host Controller requires tuning to operate SDR50 (tuning is always required to operate SDR104). 0h: SDR50 does not require tuning 1h: SDR50 requires tuning **Note:** Tuning is required for SDR50 to compensate temperature variation.
44	RESERVED	R	0h	Reserved
43-40	RETUNING_TIMER_CNT	R	4h	Timer Count for Re-Tuning (UHS-I Only) This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. 0h - Get information via other source 1h = 1 seconds 2h = 2 seconds 3h = 4 seconds 4h = 8 seconds ---- n = $2_{(n-1)}$ seconds ---- Bh = 1024 seconds Fh - Ch = Reserved
39	RESERVED	R	0h	Reserved
38	DRIVERD_SUPPORT	R	0h	Driver Type D Support (UHS-I Only) This bit indicates support of Driver Type D for 1.8 Signaling. 0h: Driver Type D is Not Supported 1h: Driver Type D is Supported

Table 14-24216. MMCSD1_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
37	DRIVERC_SUPPORT	R	0h	Driver Type C Support (UHS-I Only) This bit indicates support of Driver Type C for 1.8 Signaling. 0h: Driver Type C is Not Supported 1h: Driver Type C is Supported
36	DRIVERA_SUPPORT	R	0h	Driver Type A Support (UHS-I Only) This bit indicates support of Driver Type A for 1.8 Signaling. 0h: Driver Type A is Not Supported 1h: Driver Type A is Supported
35	UHS2_SUPPORT	R	0h	UHS-II Support (UHS-II Only) This bit indicates whether Host Controller supports UHS-II. If this bit is set to 1h, the MMCSD1_CAPABILITIES[60] VDD2_1P8_SUPPORT bit shall be set to 1h (Host System shall support VDD2 power supply). 0h: UHS-II is Not Supported 1h: UHS-II is Supported
34	DDR50_SUPPORT	R	1h	DDR50 Support (UHS-I Only) This bit indicates whether DDR50 is supported or not. 0h: DDR50 is Not Supported 1h: DDR50 is Supported
33	SDR104_SUPPORT	R	1h	SDR104 Support (UHS-I Only) This bit indicates whether SDR104 is supported or not. SDR104 requires tuning. 0h: SDR104 is Not Supported 1h: SDR104 is Supported
32	SDR50_SUPPORT	R	1h	SDR50 Support (UHS-I Only) If SDR104 is supported, this bit shall be set to 1h. Bit 40 indicates whether SDR50 requires tuning or not. 0h: SDR50 is Not Supported 1h: SDR50 is Supported

Table 14-24216. MMCSD1_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31-30	SLOT_TYPE	R	0h	Slot Type This field indicates usage of a slot by a specific Host System (a host controller register set is defined per slot). Embedded slot for one device (1h) means that only one non-removable device is connected to a SD bus slot. Shared Bus Slot (2h) can be set if Host Controller supports Shared Bus Control register. The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus (2h), the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System. 0h: Removable Card Slot 1h: Embedded Slot for One Device 2h: Shared Bus Slot (SD Mode) 3h: UHS-II Multiple Embedded Devices
29	ASYNCH_INTR_SUPPORT	R	1h	Asynchronous Interrupt Support (SD Mode Only) Refer to SDIO Specification Version 3.00 about asynchronous interrupt. 0h: Asynchronous Interrupt Not Supported 1h: Asynchronous Interrupt Supported
28	ADDR_64BIT_SUPPORT_V3	R	1h	64-bit System Address Support for V3 Meaning of this bit is different depends on Versions. Host Controller Version 3.00 and Version 4.10 use this bit as 64-bit System Address support for V3 mode. Host Controller Version 4.00 uses this bit as 64-bit System Address support for both V3 and V4 modes. SDMA cannot be used in 64-bit Addressing in Version 3 mode. If this bit is set to 1h, 64-bit ADMA2 with using 96-bit Descriptor may be enabled as follows: In case of Host Controller Version 3, 64-bit ADMA2 is enabled by MMCSD1_HOST_CONTROL1[4-3] DMA_SELECT = 3h. In case of Host Controller Version 4, 64-bit ADMA2 for Version 3 is enabled by setting MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 0h and MMCSD1_HOST_CONTROL1[4-3] DMA_SELECT = 3h. 0h: 64-bit System Address for V3 is not Supported 1h: 64-bit System Address for V3 is Supported

Table 14-24216. MMCSD1_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	ADDR_64BIT_SUPPORT_V4	R	1h	64-bit System Address Support for V4 This bit is added from Version 4.10. Setting 1h to this bit indicates that the Host Controller supports 64-bit System Addressing of Version 4 mode . When this bit is set to 1h, full or a part of 64-bit address should be used to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to the MMCSD1_HOST_CONTROL2[13] BIT64_ADDRESSING bit. If this bit is set to 1h, 64-bit DMA Addressing for Version 4 is enabled by setting MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 1h, MMCSD1_HOST_CONTROL2[13] BIT64_ADDRESSING = 1h. SDMA can be used and ADMA2 uses 128-bit Descriptor. 0h: 64-bit System Address for V4 is not Supported 1h: 64-bit System Address for V4 is Supported
26	VOLT_1P8_SUPPORT	R	1h	Voltage Support 1.8 V This bit indicates whether the HC supports 1.8 V. 0h: 1.8 V Not Supported 1h: 1.8 V Supported
25	VOLT_3P0_SUPPORT	R	1h	Voltage Support 3.0 V This bit indicates whether the HC supports 3.0 V. 0h: 3.0 V Not Supported 1h: 3.0 V Supported
24	VOLT_3P3_SUPPORT	R	1h	Voltage Support 3.3 V This bit indicates whether the HC supports 3.3 V. 0h: 3.3 V Not Supported 1h: 3.3 V Supported
23	SUSP_RES_SUPPORT	R	1h	Suspend/Resume Support This bit indicates whether the HC supports Suspend/Resume functionality. If this bit is 0h, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend/ Resume commands. 0h: Not Supported 1h: Supported

Table 14-24216. MMCSD1_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	SDMA_SUPPORT	R	1h	SDMA Support This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. Version 4.10 Host Controller shall support SDMA if ADMA2 is supported. 0h: SDMA Not Supported 1h: SDMA Supported
21	HIGH_SPEED_SUPPORT	R	1h	High Speed Support This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25 MHz to 50 MHz (for SD)/20 MHz to 52 MHz (for MMC). 0h: High Speed Not Supported 1h: High Speed Supported
20	RESERVED	R	0h	Reserved
19	ADMA2_SUPPORT	R	1h	ADMA2 Support 0h: ADMA2 Not support 1h: ADMA2 support
18	BUS_8BIT_SUPPORT	R	0h	8-bit Support for Embedded Device (Embedded) This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. This bit is not effective when the MMCSD1_CAPABILITIES[31-30] SLOT_TYPE bit field is set to 2h. 0h: 8-bit Bus Width Not Supported 1h: 8-bit Bus Width Supported
17-16	MAX_BLK_LENGTH	R	0h	Max Block Length This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. 0h: 512 byte 1h: 1024 byte 2h: 2048 byte 3h: 4096 byte

Table 14-24216. MMCSD1_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	BASE_CLK_FREQ	R	C8h	Base Clock Frequency for SD Clock (1) 6-bit Base Clock Frequency: This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. 11xx xxxxb: Not Supported 0011 1111b: 63 MHz 0000 0010b: 2 MHz 0000 0001b: 1 MHz 0000 0000b: Get Information via another method (2) 8-bit Base Clock Frequency: This mode is supported by the Host Controller Version 3.00. Unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. FFh: 255 MHz 02h: 2 MHz 01h: 1 MHz 00h: Get Information via another method If the real frequency is 16.5 MHz, the lager value shall be set 0001 0001b (17 MHz) because the Host Driver use this value to calculate the clock divider value (refer to the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field) and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method.
7	TIMEOUT_CLK_UNIT	R	0h	Timeout Clock Unit This bit shows the unit of base clock frequency used to detect Data Timeout Error (MMCSD1_ERROR_INTR_STS[4] DATA_TIMEOUT). 0h: KHz 1h: MHz
6	RESERVED	R	0h	Reserved
5-0	TIMEOUT_CLK_FREQ	R	1h	Timeout Clock Frequency This bit shows the base clock frequency used to detect Data Timeout Error (MMCSD1_ERROR_INTR_STS[4] DATA_TIMEOUT). 0h: Get Information via another method Not 0h: 1 KHz to 63 KHz/1 MHz to 63 MHz

Table 14-16223 shows the 64-bit System Address Support depends on Versions.

Table 14-24217. 64-bit System Address Support depends on Versions

Host Controller	Version 3.00	Version 4.00	Version 4.10
D28 (from Version 2.00)	for V3	for V3 and V4	for V3

Table 14-24217. 64-bit System Address Support depends on Versions (continued)

Host Controller	Version 3.00	Version 4.00	Version 4.10
D27 (from Version 4.10)	D27 (from Version 4.10)	Not Defined	for V4
Register Decode	32-bit or 64-bit (up to implementation)	32-bit or 64-bit (up to implementation)	If D27 = 1h, 64-bit
SDMA	Not supported	Supported when MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 1h	Supported when MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 1h
ADMA2 (96-bit Descriptor)	DMA Select = 3h	Selected by MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 0h	Selected by MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 0h
ADMA2 (128-bit Descriptor)	Not Defined	Selected by MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 1h	Selected by MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA = 1h

As the specification of 64-bit System Address Support has been changed, capabilities of 64-bit functions are different depends on versions.

Definition of D28 is different depends on Versions. 96-bit Descriptor was defined by Version 2 but notation V3 is used including V2. Version 4.10 divides 64-bit System Address Support into V3 mode (D28) and V4 mode (D27) so that V3 mode can be optional. Migrate to V4 is recommended. From Host Controller Version 4.00, either V3 mode or V4 mode is selected by Host Version 4 Enable in the Host Control 2 register. V3 mode can be used if 64-bit System Address Support for V3 is set to 1h. V4 mode can be used if 64-bit System Address Support for V4 is set to 1h.

Prior to Version 4.10, address length of Host Controller registers decoding is not defined and whether 32-bit or 64-bit address is used to decode Host Controller registers is up to implementation. If Host Controller decodes 32-bit system address in default, the Host Controller Registers shall be placed in 32-bit addressing space.

When D27 = 1h, Host Controller Version 4.10 or later should use full or a part of 64-bit address to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to the MMCSD1_HOST_CONTROL2[13] BIT64_ADDRESSING bit. How to decode register also should follow a system bus specification or a mother board specification.

From Version 4.00, 64-bit System Addressing of DMA is enabled by setting to the MMCSD1_HOST_CONTROL2[13] BIT64_ADDRESSING bit. 64-bit SDMA is not supported in V3 mode and is supported in V4 mode. There are two Descriptor types for ADMA2 96-bit (V3) or 128-bit (V4). Support of 96-bit Descriptor is optional for Host Controller Version 4.10. If D28 = 0h, 96-bit Descriptor is not supported.

Note: The Host System shall support at least one of these voltages above. The HD sets the MMCSD1_POWER_CONTROL[3:1] SD_BUS_VOLTAGE bit field according to these support bits. If multiple voltages are supported, select the usable lower voltage by comparing the OCR value from the card.

These registers indicate maximum current capability for each voltage. The value is meaningful if Voltage Support is set in the MMCSD1_CAPABILITIES register.

Table 14-16224 describes the re-tuning modes.

Table 14-24218. 64-bit System Address Support depends on Versions

Bit47-46	Re-Tuning Mode	Data length	Timer Modes
0h	Mode1	4 MB (Max.)	Always enabled
1h	Mode2	4 MB (Max.)	Stop during data transfer
2h	Reserved	Reserved	Reserved
3h	Reserved	Reserved	Reserved

There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.

Data length per a read/write command is restricted by whether Host Controller generates Re-Tuning Request during data transfer so that re-tuning procedures can be inserted during data transfers.

28 MMCSD1_MAX_CURRENT_CAP Register (Offset = 48h) [reset = 0h]

MMCSD1_MAX_CURRENT_CAP is shown in Figure 14-7995 and described in Table 14-16226.

Return to Summary Table.

This register indicates maximum current capability for each voltage.

Table 14-24219. MMCSD1_MAX_CURRENT_CAP Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0048h

Figure 14-7995. MMCSD1_MAX_CURRENT_CAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-0h															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED								VDD2_1P8V							
R-0h								R-0h							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								VDD1_1P8V							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDD1_3P0V								VDD1_3P3V							
R-0h								R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24221. MMCSD1_MAX_CURRENT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39-32	VDD2_1P8V	R	0h	Maximum Current for 1.8 V VDD2
31-24	RESERVED	R	0h	Reserved
23-16	VDD1_1P8V	R	0h	Maximum Current for 1.8 V VDD1
15-8	VDD1_3P0V	R	0h	Maximum Current for 3.0 V VDD1
7-0	VDD1_3P3V	R	0h	Maximum Current for 3.3 V VDD1

Table 14-16227 describes the maximum current value.

Table 14-24222. Maximum Current Value Definition

Register Value	Current Value
0	Get Information via another method
1	4 mA
2	8 mA
3	12 mA
-------------------	-------------------

Table 14-24222. Maximum Current Value Definition (continued)

Register Value	Current Value
255	1020 mA

29 MMCSD1_FORCE_EVNT_ACMD_ERR_STS Register (Offset = 50h) [reset = 0h]

MMCSD1_FORCE_EVNT_ACMD_ERR_STS is shown in Figure 14-7996 and described in Table 14-16229.

Return to Summary Table.

This register is not physically implemented, rather it is an address where the MMCSD1_AUTOCMD_ERR_STS register can be written.

Writing 1h: set each bit of the MMCSD1_AUTOCMD_ERR_STS register

Writing 0h: no effect

By setting a bit in this register, the correspondent bit is set in the MMCSD1_ERROR_INTR_STS register. In order to generate interrupt signal, the correspondent bit shall be set in the MMCSD1_ERROR_INTR_STS_ENA register and MMCSD1_ERROR_INTR_SIG_ENA register.

Table 14-24223. MMCSD1_FORCE_EVNT_ACMD_ERR_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0050h

Figure 14-7996. MMCSD1_FORCE_EVNT_ACMD_ERR_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_NOT_ISS	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD_NOT_EXEC
W-0h	R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -*n* = value after reset

Table 14-24225. MMCSD1_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMD_NOT_ISS	W	0h	Force Event for Command Not Issued by AUTO CMD12 Error 0h: Not Affected 1h: Command Not Issued By Auto CMD12 Error Status is set
6	RESERVED	R	0h	Reserved
5	RESP	W	0h	Force Event for AUTO CMD Response Error 0h: Not Affected 1h: Auto CMD Response Error Status is set
4	INDEX	W	0h	Force Event for AUTO CMD Index Error 0h: Not Affected 1h: Auto CMD Index Error Status is set

Table 14-24225. MMCSD1_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ENDBIT	W	0h	Force Event for AUTO CMD End Bit Error 0h: Not Affected 1h: Auto CMD End bit Error Status is set
2	CRC	W	0h	Force Event for AUTO CMD Timeout Error 0h: Not Affected 1h: Auto CMD CRC Error Status is set
1	TIMEOUT	W	0h	Force Event for AUTO CMD Timeout Error 0h: Not Affected 1h: Auto CMD Timeout Error Status is set
0	ACMD_NOT_EXEC	W	0h	Force Event for AUTO CMD12 Not Executed 0h: Not Affected 1h: Auto CMD12 Not Executed Status is set

30 MMCSD1_FORCE_EVNT_ERR_INT_STS Register (Offset = 52h) [reset = 0h]

MMCSD1_FORCE_EVNT_ERR_INT_STS is shown in Figure 14-7997 and described in Table 14-16231.

Return to Summary Table.

This register is not physically implemented, rather it is an address where the MMCSD1_ERROR_INTR_STS register can be written.

The MMCSD1_FORCE_EVNT_ERR_INT_STS register is not a physically implemented register. Rather, it is an address at which the MMCSD1_ERROR_INTR_STS register can be written. The effect of a write to this address will be reflected in the MMCSD1_ERROR_INTR_STS register if the corresponding bit of the MMCSD1_ERROR_INTR_STS_ENA register is set.

Writing 1h: set each bit of the MMCSD1_ERROR_INTR_STS register

Writing 0h: no effect

Table 14-24226. MMCSD1_FORCE_EVNT_ERR_INT_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0052h

Figure 14-7997. MMCSD1_FORCE_EVNT_ERR_INT_STS Register

15	14	13	12	11	10	9	8
VEND_SPEC				RESP	TUNING	ADMA	AUTO_CMD
W-0h				W-0h	W-0h	W-0h	W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LIM	DAT_ENDBIT	DAT_CRC	DAT_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -*n* = value after reset

Table 14-24228. MMCSD1_FORCE_EVNT_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VEND_SPEC	W	0h	N/A
11	RESP	W	0h	Force Event for Response Error 0h: Not Affected 1h: Response Error Status is set
10	TUNING	W	0h	Force Event for Tuning Error 0h: Not Affected 1h: Tuning Error Status is set
9	ADMA	W	0h	Force Event for ADMA Error 0h: Not Affected 1h: ADMA Error Status is set
8	AUTO_CMD	W	0h	Force Event for Auto CMD Error 0h: Not Affected 1h: Auto CMD Error Status is set

Table 14-24228. MMCSD1_FORCE_EVNT_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CURR_LIM	W	0h	Force Event for Current Limit Error 0h: Not Affected 1h: Current Limit Error Status is set
6	DAT_ENDBIT	W	0h	Force Event for Data End Bit Error 0h: Not Affected 1h: Data End Bit Error Status is set
5	DAT_CRC	W	0h	Force Event for Data CRC Error 0h: Not Affected 1h: CRC Error Status is set
4	DAT_TIMEOUT	W	0h	Force Event for Data Timeout Error 0h: Not Affected 1h: Timeout Error Status is set
3	CMD_INDEX	W	0h	Force Event for Command Index Error 0h: Not Affected 1h: Command Index Error Status is set
2	CMD_ENDBIT	W	0h	Force Event for Command End Bit Error 0h: Not Affected 1h: Command End Bit Error Status is set
1	CMD_CRC	W	0h	Force Event for Command CRC Error 0h: Not Affected 1h: Command CRC Error Status is set
0	CMD_TIMEOUT	W	0h	Force Event for CMD Timeout Error 0h: Not Affected 1h: Command Timeout Error Status is set

31 MMCSD1_ADMA_ERR_STATUS Register (Offset = 54h) [reset = 0h]

MMCSD1_ADMA_ERR_STATUS is shown in Figure 14-7998 and described in Table 14-16233.

Return to Summary Table.

When the ADMA Error interrupt occur, this register holds the ADMA State (MMCSD1_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE) and the MMCSD1_ADMA_SYS_ADDRESS register holds address around the error descriptor.

Table 14-24229. MMCSD1_ADMA_ERR_STATUS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0054h

Figure 14-7998. MMCSD1_ADMA_ERR_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					ADMA_LENGTH_ERR	ADMA_ERR_STATE	
R-0h					R-0h	R-0h	

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24231. MMCSD1_ADMA_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	ADMA_LENGTH_ERR	R	0h	ADMA Length Mismatch Error This error occurs in the following 2 cases. While the MMCSD1_TRANSFER_MODE[1] BLK_CNT_ENA bit being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 0h: No Error 1h: Error
1-0	ADMA_ERR_STATE	R	0h	ADMA Error State This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "2h" because ADMA never stops in this state. D01 - D00: ADMA Error State when error occurred Contents of SYS_SDR register 0h: ST_STOP (Stop DMA) Points to next of the error descriptor 1h: ST_FDS (Fetch Descriptor) Points to the error descriptor 2h: Never set this state (Not used) 3h: ST_TFR (Transfer Data) Points to the next of the error descriptor

32 MMCSD1_ADMA_SYS_ADDRESS Register (Offset = 58h) [reset = Xh]

MMCSD1_ADMA_SYS_ADDRESS is shown in Figure 14-7999 and described in Table 14-16235.

Return to Summary Table.

This register contains the physical address used for ADMA data transfer.

Table 14-24232. MMCSD1_ADMA_SYS_ADDRESS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0058h

Figure 14-7999. MMCSD1_ADMA_SYS_ADDRESS Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADMA_ADDR																															
R/W-Xh																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADMA_ADDR																															
R/W-Xh																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24234. MMCSD1_ADMA_SYS_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ADMA_ADDR	R/W	Xh	ADMA System Address The 32-bit addressing Host Driver uses lower 32-bit of this register (upper 32-bit should be set to 0h) and shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. DMA2/3 ignores lower 2-bit of this register and assumes it to be 0h. DMA in 64-bit addressing. The 64-bit addressing Host Driver uses all bits of this register and shall program Descriptor Table on 64-bit boundary and set 64-bit boundary address to this register. DMA2/3 ignores lower 3-bit of this register andassumes it to be 0h. **SDMA** If the MMCSD1_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, SDMA use this register to indicate System Address of data location instead of using SDMA System Address register (MMCSD1_SDMA_SYS_ADDR_LO/ MMCSD1_SDMA_SYS_ADDR_HI). SDMA can be used in 32-bit and 64-bit addressing in Version 4.00. **ADMA2** This register holds byte address of executing command of the Descriptor table. At the start of ADMA2, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. **ADMA3** This register is set by ADMA3. Host Driver is not necessary to set this register. The ADMA3 increments address of this register, which points to next line, when every time fetching a Descriptor line. When Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. Register Value - **00000000_**xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address

33 MMCSD1_PRESET_VALUE0 Register (Offset = 60h) [reset = 100h]

MMCSD1_PRESET_VALUE0 is shown in Figure 14-8000 and described in Table 14-16238.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

When the MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1h, SDCLK/RCLK Frequency Select and Clock Generator Select in the MMCSD1_CLOCK_CONTROL register, and Driver Strength Select in the MMCSD1_HOST_CONTROL2 register are automatically set based on the Selected Bus Speed Mode (see Table 14-16236). This means the Host Driver needs not set these fields when preset is enabled.

Before starting the initialization sequence, the Host Driver needs to set a clock preset value to SDCLK/ RCLK Frequency Select in the MMCSD1_CLOCK_CONTROL register. The MMCSD1_HOST_CONTROL2[15] PRESET_VALUE_ENA bit can be set after initialization completed.

Table 14-16236 shows the conditions to select one of preset value registers.

Table 14-24235. Preset Value Register Select Condition

Selected Bus Speed Mode	1.8 V Signaling Enable (Host Control 2)	High Speed Enable (Host Control 1)	UHS-1 Mode Selection (Host Control 2)
Default Speed	0	0	don't care
High Speed	0	1	don't care
SDR12	1	don't care	0h
SDR25	1	don't care	1h
SDR50	1	don't care	2h
SDR104	1	don't care	3h
DDR50	1	don't care	4h
HS400	1	don't care	5h
Reserved	Not determined	don't care	6h
UHS-II	0	don't care	7h

Table 14-24236. MMCSD1_PRESET_VALUE0 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0060h

Figure 14-8000. MMCSD1_PRESET_VALUE0 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-100h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R-100h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24238. MMCSD1_PRESET_VALUE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	100h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

34 MMCSD1_PRESET_VALUE1 Register (Offset = 62h) [reset = 4h]

MMCSD1_PRESET_VALUE1 is shown in Figure 14-8001 and described in Table 14-16240.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24239. MMCSD1_PRESET_VALUE1 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0062h

Figure 14-8001. MMCSD1_PRESET_VALUE1 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-4h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R-4h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24241. MMCSD1_PRESET_VALUE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	4h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

35 MMCSD1_PRESET_VALUE2 Register (Offset = 64h) [reset = 2h]

MMCSD1_PRESET_VALUE2 is shown in Figure 14-8002 and described in Table 14-16242.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24242. MMCSD1_PRESET_VALUE2 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0064h

Figure 14-8002. MMCSD1_PRESET_VALUE2 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24244. MMCSD1_PRESET_VALUE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

36 MMCSD1_PRESET_VALUE3 Register (Offset = 66h) [reset = 4h]

MMCSD1_PRESET_VALUE3 is shown in Figure 14-8003 and described in Table 14-16244.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24245. MMCSD1_PRESET_VALUE3 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0066h

Figure 14-8003. MMCSD1_PRESET_VALUE3 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-4h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-4h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24247. MMCSD1_PRESET_VALUE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	4h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

37 MMCSD1_PRESET_VALUE4 Register (Offset = 68h) [reset = 2h]

MMCSD1_PRESET_VALUE4 is shown in Figure 14-8004 and described in Table 14-16246.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24248. MMCSD1_PRESET_VALUE4 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0068h

Figure 14-8004. MMCSD1_PRESET_VALUE4 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-2h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24250. MMCSD1_PRESET_VALUE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

38 MMCSD1_PRESET_VALUE5 Register (Offset = 6Ah) [reset = 1h]

MMCSD1_PRESET_VALUE5 is shown in Figure 14-8005 and described in Table 14-16248.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24251. MMCSD1_PRESET_VALUE5 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 006Ah

Figure 14-8005. MMCSD1_PRESET_VALUE5 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">DRIVER_STRENGTH_SEL</td><td colspan="3">RESERVED</td><td>CLOCK_GENSEL</td><td colspan="2">SDCLK_FRQSEL</td></tr>
<tr><td colspan="2">R-0h</td><td colspan="3">R-0h</td><td>R-0h</td><td colspan="2">R-1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SDCLK_FRQSEL</td></tr>
<tr><td colspan="8">R-1h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24253. MMCSD1_PRESET_VALUE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	1h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

39 MMCSD1_PRESET_VALUE6 Register (Offset = 6Ch) [reset = 0h]

MMCSD1_PRESET_VALUE6 is shown in Figure 14-8006 and described in Table 14-16250.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24254. MMCSD1_PRESET_VALUE6 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 006Ch

Figure 14-8006. MMCSD1_PRESET_VALUE6 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-0h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24256. MMCSD1_PRESET_VALUE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

40 MMCSD1_PRESET_VALUE7 Register (Offset = 6Eh) [reset = 2h]

MMCSD1_PRESET_VALUE7 is shown in Figure 14-8007 and described in Table 14-16252.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24257. MMCSD1_PRESET_VALUE7 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 006Eh

Figure 14-8007. MMCSD1_PRESET_VALUE7 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-2h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24259. MMCSD1_PRESET_VALUE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

41 MMCSD1_PRESET_VALUE8 Register (Offset = 72h) [reset = 0h]

MMCSD1_PRESET_VALUE8 is shown in Figure 14-8008 and described in Table 14-16254.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24260. MMCSD1_PRESET_VALUE8 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0072h

Figure 14-8008. MMCSD1_PRESET_VALUE8 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-0h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24262. MMCSD1_PRESET_VALUE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

42 MMCSD1_PRESET_VALUE10 Register (Offset = 74h) [reset = 0h]

MMCSD1_PRESET_VALUE10 is shown in Figure 14-8009 and described in Table 14-16256.

Return to Summary Table.

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 14-24263. MMCSD1_PRESET_VALUE10 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0074h

Figure 14-8009. MMCSD1_PRESET_VALUE10 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h		R-0h			R-0h	R-0h	

7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24265. MMCSD1_PRESET_VALUE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD1_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

43 MMCSD1_ADMA3_DESC_ADDRESS Register (Offset = 78h) [reset = Xh]

MMCSD1_ADMA3_DESC_ADDRESS is shown in Figure 14-8010 and described in Table 14-16258.

Return to Summary Table.

The start address of Integrated DMA Descriptor is set to this register.

Table 14-24266. MMCSD1_ADMA3_DESC_ADDRESS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0078h

Figure 14-8010. MMCSD1_ADMA3_DESC_ADDRESS Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
INTG_DESC_ADDR																															
R/W-Xh																															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTG_DESC_ADDR																															
R/W-Xh																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24268. MMCSD1_ADMA3_DESC_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	INTG_DESC_ADDR	R/W	Xh	ADMA3 Integrated Descriptor Address The start address of Integrated DMA Descriptor is set to this register. Writing to a specific address starts ADMA3 depends on 32-bit/64-bit address-ing. The ADMA3 fetches one Descriptor Address and increments this field to indicate the next Descriptor address. The 32-bit addressing Host Driver uses lower 32-bit of this register and shall program Descriptor Table on 32-bit boundary. ADMA3 ignores lower 2-bit of this register and assumes it to be 0h. Writing to 07Bh starts ADMA3 data transfer. The 64-bit addressing Host Driver uses all 64-bit of this register and shall program Descriptor Table on 64-bit boundary. ADMA3 ignores lower 3-bit of this register and assumes it to be 0h. Writing to 07Fh starts ADMA3 data transfer. Register Value - **00000000**_xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address

44 MMCSD1_UHS2_BLOCK_SIZE Register (Offset = 80h) [reset = 0h]

MMCSD1_UHS2_BLOCK_SIZE is shown in Figure 14-8011 and described in Table 14-16260.

Return to Summary Table.

This register is used to configure the number of bytes in a data block.

Table 14-24269. MMCSD1_UHS2_BLOCK_SIZE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0080h

Figure 14-8011. MMCSD1_UHS2_BLOCK_SIZE Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_BOUNDARY			XFER_BLK_SIZE			
R-0h	R/W-0h			R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XFER_BLK_SIZE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24271. MMCSD1_UHS2_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved

Table 14-24271. MMCSD1_UHS2_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	SDMA_BUF_BOUNDARY	R/W	0h	UHS-II SDMA Buffer Boundary (SDMA only) When system memory is managed by paging, SDMA data transfer is performed in unit of paging. A page size of system memory management is set to this field. Host Controller generates the DMA Interrupt at the page boundary and requests the Host Driver to update the MMCSD1_ADMA_SYS_ADDRESS register. SDMA waits until the MMCSD1_ADMA_SYS_ADDRESS register is written. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued (see MMCSD1_NORMAL_INTR_STS[1] XFER_COMPLETE). These bits shall be supported when the MMCSD1_CAPABILITIES[22] SDMA_SUPPORT bit is set to 1h and this function is active when the MMCSD1_UHS2_XFER_MODE[0] DMA_ENA bit register is set to 1h. ADMA does not use this field. 0h: 4K bytes (Detects A11 carry out) 1h: 8K bytes (Detects A12 carry out) 2h: 16K Bytes (Detects A13 carry out) 3h: 32K Bytes (Detects A14 carry out) 4h: 64K bytes (Detects A15 carry out) 5h: 128K Bytes (Detects A16 carry out) 6h: 256K Bytes (Detects A17 carry out) 7h: 512K Bytes (Detects A18 carry out)
11-0	XFER_BLK_SIZE	R/W	0h	UHS-II Block Size This bit field specifies the block size of data packet. SD Memory Card uses a fixed block size of 512 bytes. Variable block size may be used for SDIO. The maximum value is 2048 Bytes because CRC16 covers up to 2048 bytes. This bit field is effective when the MMCSD1_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. 0000h - No data transfer 0001h - 1 Byte 0002h - 2 Bytes 0003h - 3 Bytes ... ... 01FFh - 511 Bytes 0200h - 512 Bytes ... ... 0800h - 2048 Bytes

45 MMCSD1_UHS2_BLOCK_COUNT Register (Offset = 84h) [reset = 0h]

MMCSD1_UHS2_BLOCK_COUNT is shown in Figure 14-8012 and described in Table 14-16262.

Return to Summary Table.

This register is used to configure the number of data blocks.

Table 14-24272. MMCSD1_UHS2_BLOCK_COUNT Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0084h

Figure 14-8012. MMCSD1_UHS2_BLOCK_COUNT Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">XFER_BLK_COUNT</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-24274. MMCSD1_UHS2_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XFER_BLK_COUNT	R/W	0h	UHS-II Block Count This register is effective when the MMCSD1_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h and is enabled when the MMCSD1_UHS2_XFER_MODE[1] BLK_CNT_ENA bit is set to 1h and the MMCSD1_UHS2_XFER_MODE[5] BYTE_MODE bit is set to 0h. Data transfer stops when the count reaches zero. Setting the block count to 0h results in no data blocks is transferred. This register should be accessed only when no transaction is executing (after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. 00000000h: Stop Count 00000001h: 1 block 00000002h: 2 blocks ... ... FFFFFFFFh: 4G blocks - 1

46 MMCSD1_UHS2_COMMAND_PKT_0 to MMCSD1_UHS2_COMMAND_PKT_19 Register (Offset = 88h to 9Bh) [reset = 0h]

MMCSD1_UHS2_COMMAND_PKT_0 to MMCSD1_UHS2_COMMAND_PKT_19 is shown in Figure 14-8013 and described in Table 14-16265.

Return to Summary Table.

UHS-II Command Packet image is set to this register. The maximum length is 20 bytes (see Table 14-16263). The command length varies depends on a Command Packet type. The length is specified by the MMCSD1_UHS2_COMMAND register.

Table 14-24275. UHS-II Command Packet Register

Offset	Preset Value Registers
088h	Command Packet Byte 0
089h	Command Packet Byte 1
08Ah	Command Packet Byte 2
....	....
09Bh	Command Packet Byte 19

Table 14-24276. MMCSD1_UHS2_COMMAND_PKT_0 to MMCSD1_UHS2_COMMAND_PKT_19 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0088h to 0FA0 009Bh

Figure 14-8013. MMCSD1_UHS2_COMMAND_PKT_0 to MMCSD1_UHS2_COMMAND_PKT_19 Register

7	6	5	4	3	2	1	0
CMD_PKT_BYTE							
R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24278. MMCSD1_UHS2_COMMAND_PKT_0 to MMCSD1_UHS2_COMMAND_PKT_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CMD_PKT_BYTE	R/W	0h	Command Packet Byte UHS-II Command Packet image is set to this register. The command length varies depends on a Command Packet type.

47 MMCSD1_UHS2_XFER_MODE Register (Offset = 9Ch) [reset = 0h]

MMCSD1_UHS2_XFER_MODE is shown in Figure 14-8014 and described in Table 14-16267.

Return to Summary Table.

This register is used to control the operations of data transfers.

On issuing a Command Packet, a Command Packet image is set to UHS-II Command Packet register (see MMCSD1_UHS2_COMMAND_PKT_0 - MMCSD1_UHS2_COMMAND_PKT_19) but Host Controller does not analyze the setting of UHS-II Command Packet register. Instead, Host Controller refers setting of this register to issue a Command Packet to make the control easy. Setting of these registers shall be correspondent.

Table 14-24279. MMCSD1_UHS2_XFER_MODE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 009Ch

Figure 14-8014. MMCSD1_UHS2_XFER_MODE Register

15	14	13	12	11	10	9	8
DUPLEX_SELECT	EBSY_WAIT	RESERVED					RESP_INTR_DIS
R/W-0h	R/W-0h	R-0h					R/W-0h

7	6	5	4	3	2	1	0
RESP_ERR_CHK_ENA	RESP_TYPE	BYTE_MODE	DATA_XFER_DIR	RESERVED		BLK_CNT_ENA	DMA_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24281. MMCSD1_UHS2_XFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DUPLEX_SELECT	R/W	0h	Half/Full Select Use of 2 lane half duplex mode is determined by Host Driver. 0h: Full Duplex Mode 1h: 2 Lane Half Duplex Mode

Table 14-24281. MMCSD1_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EBSY_WAIT	R/W	0h	EBSY Wait This bit is set when issuing a command which is accompanied by EBSY packet to indicate end of command execution. Busy is expected for CCMD with R1b/R5b type and DCMD with data transfer. If this bit is set to 1h, Host Controller waits receiving of EBSY packet and on receiving EBSY packet, the MMCSD1_NORMAL_INTR_STS[1] XFER_COMPLETE bit is set to 1h to indicate end of busy. If an error is indicated in EBSY packet (for example: Memory Error), the MMCSD1_UHS2_ERR_INTR_STS[8] EBSY bit is set to 1h. Setting of the MMCSD1_UHS2_ERR_INTR_STS[8] EBSY bit also sets the MMCSD1_NORMAL_INTR_STS[15] ERROR_INTR bit to 1h. The MMCSD1_NORMAL_INTR_STS[15] ERROR_INTR and MMCSD1_NORMAL_INTR_STS[1] XFER_COMPLETE bits shall be set together. 0h: Issue a command without busy 1h: Wait EBSY
13-9	RESERVED	R	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Response Interrupt Disable Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0h and waits the MMCSD1_NORMAL_INTR_STS[0] CMD_COMPLETE bit and then check the response register (MMCSD1_RESPONSE_0 - MMCSD1_RESPONSE_7). If Host Controller checks response error, sets this bit to 1h and sets the MMCSD1_UHS2_XFER_MODE[7] RESP_ERR_CHK_ENA bit to 1h. The MMCSD1_NORMAL_INTR_STS[0] CMD_COMPLETE bit is disabled by this bit regardless of MMCSD1_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit. 0h: Response Interrupt is enabled 1h: Response Interrupt is disabled

Table 14-24281. MMCSD1_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESP_ERR_CHK_ENA	R/W	0h	Response Error Check Enable Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, this bit is set to 0h and the MMCSD1_UHS2_XFER_MODE[8] RESP_INTR_DIS bit is set to 0h. If Host Controller checks response error, sets this bit to 1h and sets the MMCSD1_UHS2_XFER_MODE[8] RESP_INTR_DIS bit to 1h. Response Type R1/R5 selects either R1 or R5 response type. If an error is detected, RES Packet Error Interrupt is generated in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Response Error Check is disabled 1h: Response Error Check is enabled
6	RESP_TYPE	R/W	0h	Response Type R1/R5 When response error check is enabled, this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1: Bit31 OUT_OF_RANGE Bit30 ADDRESS_ERROR Bit29 BLOCK_LEN_ERROR Bit26 WP_VIOLATION Bit25 CARD_IS_LOCKED Bit23 COM_CRC_ERROR Bit21 CARD_ECC_FAILED Bit20 CC_ERROR Bit19 ERROR Response Flags Checked in R5: Bit07 COM_CRC_ERROR Bit03 ERROR Bit01 FUNCTION_NUMBER Bit00 OUT_OF_RANGE 0h: R1 (Memory) 1h: R5 (SDIO)

Table 14-24281. MMCSD1_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	BYTE_MODE	R/W	0h	Block/Byte Mode This bit specifies whether data transfer is in byte mode or block mode when the MMCSD1_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. This bit is effective to a command with data transfer. 0h: Block Mode 1h: Byte Mode
4	DATA_XFER_DIR	R/W	0h	Data Transfer Direction This bit specifies direction of data transfer when the MMCSD1_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. This bit is effective to a command with data transfer. 0h: Read (Card to Host) 1h: Write (Host to Card)
3-2	RESERVED	R	0h	Reserved
1	BLK_CNT_ENA	R/W	0h	Block Count Enable This bit specifies whether data transfer uses the MMCSD1_UHS2_BLOCK_COUNT register. If this bit is set to 1h, data transfer is terminated by Block Count. Setting to the MMCSD1_UHS2_BLOCK_COUNT register shall be equivalent to TLEN in UHS-II Command Packet register (MMCSD1_UHS2_COMMAND_PKT_0 - MMCSD1_UHS2_COMMAND_PKT_19). 0h: Block Count Disabled 1h: Block Count Enabled
0	DMA_ENA	R/W	0h	DMA Enable This bit selects whether DMA is used or not and is effective to a command with data transfer. One of DMA types is selected by the MMCSD1_HOST_CONTROL1[4-3] DMA_SELECT bit field. 0h: DMA is disabled 1h: DMA is enabled

48 MMCSD1_UHS2_COMMAND Register (Offset = 9Eh) [reset = 0h]

MMCSD1_UHS2_COMMAND is shown in Figure 14-8015 and described in Table 14-16269.

Return to Summary Table.

This register is used to program the Command for host controller.

Table 14-24282. MMCSD1_UHS2_COMMAND Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 009Eh

Figure 14-8015. MMCSD1_UHS2_COMMAND Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PKT_LENGTH</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="5">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CMD_TYPE</td><td>DATA_PRESENT</td><td colspan="2">RESERVED</td><td>SUB_COMMAND</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="2">R/W-0h</td><td>R/W-0h</td><td colspan="2">R-0h</td><td>R/W-0h</td><td colspan="2">R-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24284. MMCSD1_UHS2_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	PKT_LENGTH	R/W	0h	UHS-II Command Packet Length A command packet length, which is set in the UHS-II Command Packet register (MMCSD1_UHS2_COMMAND_PKT_0 - MMCSD1_UHS2_COMMAND_PKT_19), is set to this bit field. 00011b – 00000b: 3-0 Bytes (Not used) 00100b: 4 Bytes .... 10100b: 20 Bytes 11111b – 10101b

Table 14-24284. MMCSD1_UHS2_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	CMD_TYPE	R/W	0h	Command Type This field is used to distinguish a specific command like abort command. If this field is set to 0h, the UHS-II RES Packet is stored in UHS-II Response register (MMCSD1_UHS2_RESPONSE_0 - MMCSD1_UHS2_RESPONSE_19). To avoid overwriting the UHS-II Response register, when this field is set to 1h, the RES Packet (4 bytes length) of TRANS_ABORT CCMD is stored in the Response register (04FB 0010h - 04FB 0013h (04F9 8010h - 04F9 8013h)) and when this field is set to 2h, the RES Packet (8 bytes length) of memory or SDIO abort command (CMD12 or SDIO Abort command) is stored in the Response register (04FB 0018h - 04FB 001Fh (04F9 8018h - 04F9 801Fh)). When this field is set to 3h, Host Controller controls lane to go into dormant state. 0h: Normal Command 1h: TRANS_ABORT CCMD 2h: CMD12 or SDIO Abort command 3h: Go Dormant Command
5	DATA_PRESENT	R/W	0h	Data Present This bit specifies whether the command is accompanied by data packet. 0h: No Data Present 1h: Data Present
4-3	RESERVED	R	0h	Reserved
2	SUB_COMMAND	R/W	0h	Sub Command Flag This bit is added from Version 4.10 to distinguish a main command or sub command. When issuing a main command, this bit is set to 0h and when issuing a sub command, this bit is set to 1h. Setting of this bit is checked by the MMCSD1_PRESENTSTATE[28] SUB_COMMAND_STS bit. 0h: Sub Command 1h: Main Command
1-0	RESERVED	R	0h	Reserved

49 MMCSD1_UHS2_RESPONSE_0 to MMCSD1_UHS2_RESPONSE_19 Register (Offset = A0h to B3h) [reset = 0h]

MMCSD1_UHS2_RESPONSE_0 to MMCSD1_UHS2_RESPONSE_19 is shown in Figure 14-8016 and described in Table 14-16271.

Return to Summary Table.

This register is used to store received UHS-II RES Packet image.

Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command, which is specified by setting 1h or 2h to the MMCSD1_UHS2_COMMAND[7-6] CMD_TYPE bit field. The maximum response length is 20 bytes.

Table 14-24285. MMCSD1_UHS2_RESPONSE_0 to UHS2_RESPONSE_19 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00A0h to 0FA0 00B3h

Figure 14-8016. MMCSD1_UHS2_RESPONSE_0 to MMCSD1_UHS2_RESPONSE_19 Register

7	6	5	4	3	2	1	0
RESP_PKT_BYTE							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24287. MMCSD1_UHS2_RESPONSE_0 to UHS2_RESPONSE_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESP_PKT_BYTE	R	0h	Response Packet Byte Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command.

Table 14-16272 shows UHS-II Response Register offsets.

Table 14-24288. UHS-II Response Register

Offset	Preset Value Registers
0FA0 0A0h / 04F9 8A0h	Response Packet Byte 0
0FA0 0A1h / 04F9 8A1h	Response Packet Byte 1
0FA0 0A2h / 04F9 8A2h	Response Packet Byte 2
....	....
0FA0 0B3h / 04F9 8B3h	Response Packet Byte 19

50 MMCSD1_UHS2_MESSAGE_SELECT Register (Offset = B4h) [reset = 0h]

MMCSD1_UHS2_MESSAGE_SELECT is shown in Figure 14-8017 and described in Table 14-16274.

Return to Summary Table.

This register is used to access internal buffer.

Table 14-24289.
MMCSD1_UHS2_MESSAGE_SELECT Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00B4h

Figure 14-8017. MMCSD1_UHS2_MESSAGE_SELECT Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MSG_SEL</td></tr>
<tr><td colspan="6">R-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24291. MMCSD1_UHS2_MESSAGE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	MSG_SEL	R/W	0h	UHS-II MSG Select Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs can be read from the MMCSD1_UHS2_MESSAGE register (04FB 00BBh - 04FB 00B8h (04F9 80BBh - 04F9 80B8h) by setting this register (assumed for debug usage). 0h: The latest MSG 1h: One MSG before 2h: Two MSGs before 3h: Three MSGs before

51 MMCSD1_UHS2_MESSAGE Register (Offset = B8h) [reset = 0h]

MMCSD1_UHS2_MESSAGE is shown in Figure 14-8018 and described in Table 14-16276.

Return to Summary Table.

This register is used to access internal buffer.

Table 14-24292. MMCSD1_UHS2_MESSAGE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00B8h

Figure 14-8018. MMCSD1_UHS2_MESSAGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSG_BYTE3								MSG_BYTE2							
R-0h								R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MSG_BYTE1								MSG_BYTE0							
R-0h								R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24294. MMCSD1_UHS2_MESSAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MSG_BYTE3	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSD1_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSD1_UHS2_MESSAGE Register.
23-16	MSG_BYTE2	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSD1_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSD1_UHS2_MESSAGE Register.
15-8	MSG_BYTE1	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSD1_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSD1_UHS2_MESSAGE Register.

Table 14-24294. MMCSD1_UHS2_MESSAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	MSG_BYTE0	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSD1_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSD1_UHS2_MESSAGE Register.

52 MMCSD1_UHS2_DEVICE_INTR_STATUS Register (Offset = BCh) [reset = 0h]

MMCSD1_UHS2_DEVICE_INTR_STATUS is shown in Figure 14-8019 and described in Table 14-16278.

Return to Summary Table.

This register shows receipt of INT MSG from which device.

Table 14-24295. MMCSD1_UHS2_DEVICE_INTR_STATUS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00BCh

Figure 14-8019. MMCSD1_UHS2_DEVICE_INTR_STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_INT_STS															
R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-24297. MMCSD1_UHS2_DEVICE_INTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEV_INT_STS	R/W1C	0h	UHS-II Device Interrupt Status This register shows receipt of INT MSG from which device and is effective when the MMCSD1_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. On receiving INT MSG from a device, Host Controller saves the INT MSG to MMCSD1_UHS2_DEVICE_INT_CODE register. A bit of this register, which is correspondent to Device ID, is set to 1h and generate Card Interrupt in Normal Interrupt Status register (see MMCSD1_NORMAL_INTR_STS[8] CARD_INTR). Writing a bit to 1h clears the status bit (interrupt is treated) and writing a bit to 0h keeps the status value (interrupt is untreated). If the MMCSD1_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 0h, this register is cleared to 0h and Host Controller ignores receipt of INT MSG. Effective bit range of this register is determined by the MMCSD1_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. If N devices are supported, bits 1 to N are effective. Then Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. A bit of unsupported Device ID in this register shall be indicated to 0h. D00 - Not used (Reserved) D01 - Setting 1h means INT MSG is received from Device ID 1 D02 - Setting 1h means INT MSG is received from Device ID 2 .... D15 - Setting 1h means INT MSG is received from Device ID 15

53 MMCSD1_UHS2_DEVICE_SELECT Register (Offset = BEh) [reset = 0h]

MMCSD1_UHS2_DEVICE_SELECT is shown in Figure 14-8020 and described in Table 14-16280.

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UHS-II Device Select Register.

Table 14-24298. MMCSD1_UHS2_DEVICE_SELECT Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00BEh

Figure 14-8020. MMCSD1_UHS2_DEVICE_SELECT Register

7	6	5	4	3	2	1	0
INT_MSG_ENA	RESERVED			DEV_SEL			
R/W-0h	R-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24300. MMCSD1_UHS2_DEVICE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MSG_ENA	R/W	0h	INT MSG Enable (Optional) This bit enables receipt of INT MSG. If this bit is set to 1h, receipt of INT MSG is informed by the MMCSD1_NORMAL_INTR_STS[8] CARD_INTR bit. If this bit is set to 0h, Host Controller ignores receipt of INT MSG and may not set the MMCSD1_UHS2_DEVICE_INT_CODE register. Support of INT MSG Interrupt is optional. If trying to set this bit to 1h but still this bit is read 0, INT MSG Interrupt is not supported by the Host Controller. In this case, the MMCSD1_UHS2_DEVICE_INTR_STATUS register always shall be read 0 and the MMCSD1_UHS2_DEVICE_INT_CODE register may not be implemented. 0h: Disabled 1h: Enabled
6-4	RESERVED	R	0h	Reserved

Table 14-24300. MMCSD1_UHS2_DEVICE_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DEV_SEL	R/W	0h	UHS-II Device Select Host Controller holds an INT MSG packet per device. One of INT MSGs (up to 15) can be selected by this field and read from the MMCSD1_UHS2_DEVICE_INT_CODE. This field is effective when the MMCSD1_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. The number of devices implemented in the Host Controller is indicated by the MMCSD1_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. 0h: Unselected (Default) 1h: INT MSG of Device ID 1 is selected 2h: INT MSG of Device ID 2 is selected .... Fh: INT MSG of Device ID 15 is selected

54 MMCSD1_UHS2_DEVICE_INT_CODE Register (Offset = BFh) [reset = 0h]

MMCSD1_UHS2_DEVICE_INT_CODE is shown in Figure 14-8021 and described in Table 14-16282.

Return to Summary Table.

This register is effective when the MMCSD1_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h.

Table 14-24301. MMCSD1_UHS2_DEVICE_INT_CODE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00BFh

Figure 14-8021. MMCSD1_UHS2_DEVICE_INT_CODE Register

7	6	5	4	3	2	1	0
DEV_INTR							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24303. MMCSD1_UHS2_DEVICE_INT_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEV_INTR	R	0h	UHS II Device Interrupt This register is effective when the MMCSD1_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. Host Controller holds an INT MSG packet per device. One of INT MSGs (Code length is 1 byte) up to 15 can be read from this register by selecting UHS-II Device Select (MMCSD1_UHS2_DEVICE_SELECT[3-0] DEV_SEL). The number of the registers to hold INT MSGs is determined by the MMCSD1_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization.

55 MMCSD1_UHS2_SOFTWARE_RESET Register (Offset = C0h) [reset = 0h]

MMCSD1_UHS2_SOFTWARE_RESET is shown in Figure 14-8022 and described in Table 14-16284.

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UHS-II Software Reset Register.

Table 14-24304. MMCSD1_UHS2_SOFTWARE_RESET Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00C0h

Figure 14-8022. MMCSD1_UHS2_SOFTWARE_RESET Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						HOST_SDTRAN_RESET	HOST_FULL_RESET
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24306. MMCSD1_UHS2_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	HOST_SDTRAN_RESET	R/W	0h	Host SD-TRAN Reset Host Driver set this bit to 1h to reset SD-TRAN layer when CMD0 is issued to Device or data transfer error occurs. This bit is cleared automatically at completion of SD-TRAN reset. If CMD0 is issued, SD-TRAN Initialization sequence from CMD8 is required to use UHS-II mode. Assuming that bus power is maintained and CM-TRAN Initialization is not required. Host Controller requires to do followings: (1) SD Clock Enable is maintained (continue to provide RCLK). (2) All setting register is maintained. (3) Internal sequencers are reset to just after power on be able to issue a command. (4) All Interrupt Status, Status Enable and Signal Enable are cleared. (5) Data transfer is terminated and data in buffer is discarded. 0h: Not Affected 1h: Reset SD-TRAN

Table 14-24306. MMCSD1_UHS2_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HOST_FULL_RESET	R/W	0h	Host Full Reset On issuing FULL_RESET CCMD, Host Driver set this bit to 1h to reset Host Controller. This bit is cleared automatically at completion of Host Controller reset. Initialization sequence from PHY Initialization is required to use UHS-II mode. Assuming that bus power is maintained. Host Controller requires to do followings: (1) SD Clock Enable is cleared (internal Clock is still synchronized). (2) All setting register is cleared. (3) Internal sequencers are reset to just after power on. (4) All Interrupt Status, Status Enable and Signal Enable are cleared. 0h: Not Affected 1h: Reset Host Controller

56 MMCSD1_UHS2_TIMER_CONTROL Register (Offset = C2h) [reset = 0h]

MMCSD1_UHS2_TIMER_CONTROL is shown in Figure 14-8023 and described in Table 14-16286.

Return to Summary Table.

UHS-II Timeout Control Register.

Table 14-24307. MMCSD1_UHS2_TIMER_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00C2h

Figure 14-8023. MMCSD1_UHS2_TIMER_CONTROL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEADLOCK_TIMEOUT_CTR				CMDRESP_TIMEOUT_CTR			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24309. MMCSD1_UHS2_TIMER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-4	DEADLOCK_TIMEOUT_CTR	R/W	0h	Timeout Counter Value for Deadlock This value determines the deadlock period while host expecting to receive a packet (1 second). Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for Deadlock (in the MMCSD1_UHS2_ERR_INTR_STS_ENA register). Fh: Reserved Eh: TMCLK x 2^{27} .... 1h: TMCLK x 2^{14} 0h: TMCLK x 2^{13}

Table 14-24309. MMCSD1_UHS2_TIMER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CMDRESP_TIMEOUT_CTR	R/W	0h	Timeout Counter Value for CMD_RES This value determines the interval between command packet and response packet (5 ms). Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for CMD_RES (in the MMCSD1_UHS2_ERR_INTR_STS_ENA register). Fh: Reserved Eh: TMCLK x 2^{27} .... 1h: TMCLK x 2^{14} 0h: TMCLK x 2^{13}

57 MMCSD1_UHS2_ERR_INTR_STS Register (Offset = C4h) [reset = 0h]

MMCSD1_UHS2_ERR_INTR_STS is shown in Figure 14-8024 and described in Table 14-16288.

Return to Summary Table.

This register gives the status of all UHS-II interrupts.

Table 14-24310. MMCSD1_UHS2_ERR_INTR_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00C4h

Figure 14-8024. MMCSD1_UHS2_ERR_INTR_STS Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC_ERR					RESERVED		
R/W1C-0h					R-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W1C-0h	R/W1C-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADMA2_ADMA3	RESERVED						EBSY
R/W1C-0h	R-0h						R/W1C-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-24312. MMCSD1_UHS2_ERR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECFIC_ERR	R/W1C	0h	Vendor Specific Error Vendor may use this field for vendor specific error status. 0h: Interrupt is not generated 1h: Vendor Specific Error
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W1C	0h	Timeout for Deadlock Setting of this bit means that deadlock timeout occurs. Host expects to receive a packet but not received in a specified timeout (1 second). Timeout value is determined by the setting of the MMCSD1_UHS2_TIMER_CONTROL[7-4] DEADLOCK_TIMEOUT_CTR bit field. 0h: Interrupt is not generated 1h: Deadlock Error

Table 14-24312. MMCSD1_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W1C	0h	Timeout for CMD_RES Setting of this bit means that RES Packet timeout occurs. Host expects to receive RES packet but not received in a specified timeout (5 ms). Timeout value is determined by the setting of the MMCSD1_UHS2_TIMER_CONTROL[3-0] CMDRESP_TIMEOUT_CTR bit field. 0h: Interrupt is not generated 1h: RES Packet Timeout Error
15	ADMA2_ADMA3	R/W1C	0h	ADMA2/3 Error Setting of this bit means that ADMA2/3 Error occurs in UHS-II mode. ADMA2/3 Error Status is indicated to the MMCSD1_ADMA_ERR_STATUS register, which is defined in the Host spec 3.00. 0h: Interrupt is not generated 1h: ADMA2/3 Error
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W1C	0h	EBSY Error On receiving EBSY packet, if the packet indicates an error, this bit is set to 1h. Setting of this bit also sets Error Interrupt and Transfer Completer together in the MMCSD1_NORMAL_INTR_STS register. This error check is effective for a command with setting the MMCSD1_UHS2_XFER_MODE[14] EBSY_WAIT bit. 0h: Interrupt is not generated 1h: EBSY Error (Backend Error)
7	UNRECOVERABLE	R/W1C	0h	Unrecoverable Error Setting of this bit means that Unrecoverable Error is set in a packet from a device. 0h: Interrupt is not generated 1h: Device Unrecoverable Error
6	RESERVED	R	0h	Reserved
5	TID	R/W1C	0h	TID Error Setting of this bit means that TID Error occurs. 0h: Interrupt is not generated 1h: TID Error

Table 14-24312. MMCSD1_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	FRAMING	R/W1C	0h	Framing Error Setting of this bit means that Framing Error occurs during a packet receiving. 0h: Interrupt is not generated 1h: Framing Error
3	CRC	R/W1C	0h	CRC Error Setting of this bit means that CRC Error occurs during a packet receiving. 0h: Interrupt is not generated 1h: CRC Error
2	RETRY_EXPIRED	R/W1C	0h	Retry Expired Setting of this bit means that Retry Counter Expired Error occurs during data transfer. If this bit is set, either Framing Error or CRC Error in this register shall be set. 0h: Interrupt is not generated 1h: Retry Expired Error
1	RESP_PKT	R/W1C	0h	RES Packet Error Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If the MMCSD1_UHS2_XFER_MODE[7] RESP_ERR_CHK_ENA bit is set to 1h, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1h. 0h: Interrupt is not generated 1h: RES Packet Error
0	HEADER	R/W1C	0h	Header Error Setting of this bit means that Header Error occurs in a received packet. 0h: Interrupt is not generated 1h: Header Error

58 MMCSD1_UHS2_ERR_INTR_STS_ENA Register (Offset = C8h) [reset = 0h]

MMCSD1_UHS2_ERR_INTR_STS_ENA is shown in Figure 14-8025 and described in Table 14-16290.

Return to Summary Table.

This register is used to enable the MMCSD1_UHS2_ERR_INTR_STS register fields.

Table 14-24313. MMCSD1_UHS2_ERR_INTR_STS_ENA Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00C8h

Figure 14-8025. MMCSD1_UHS2_ERR_INTR_STS_ENA Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC					RESERVED		
R/W-0h					R-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADMA2_ADMA3	RESERVED						EBSY
R/W-0h	R-0h						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24315. MMCSD1_UHS2_ERR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECFIC	R/W	0h	Vendor Specific Error Setting this bit to 1h enables setting of Vendor Specific Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Timeout for Deadlock Setting this bit to 1h enables setting of Timeout for Dead lock bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

Table 14-24315. MMCSD1_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W	0h	Timeout for CMD_RES Setting this bit to 1h enables setting of Timeout for CMD_RES bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
15	ADMA2_ADMA3	R/W	0h	ADMA2/3 Error Setting this bit to 1h enables setting of ADMA2/3 Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W	0h	EBSY Error Setting this bit to 1h enables setting of EBSY Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
7	UNRECOVERABLE	R/W	0h	Unrecoverable Error Setting this bit to 1h enables setting of Unrecoverable Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
6	RESERVED	R	0h	Reserved
5	TID	R/W	0h	TID Error Setting this bit to 1h enables setting of TID Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
4	FRAMING	R/W	0h	Framing Error Setting this bit to 1h enables setting of Framing Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

Table 14-24315. MMCSD1_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CRC	R/W	0h	CRC Error Setting this bit to 1h enables setting of CRC Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
2	RETRY_EXPIRED	R/W	0h	Retry Expired Setting this bit to 1h enables setting of Retry Expired bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
1	RESP_PKT	R/W	0h	RES Packet Error Setting this bit to 1h enables setting of RES Packet Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
0	HEADER	R/W	0h	Header Error Setting this bit to 1h enables setting of Header Error bit in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

59 MMCSD1_UHS2_ERR_INTR_SIG_ENA Register (Offset = CCh) [reset = 0h]

MMCSD1_UHS2_ERR_INTR_SIG_ENA is shown in Figure 14-8026 and described in Table 14-16292.

Return to Summary Table.

This register is used to generate UHS-II Interrupt signals.

Table 14-24316. MMCSD1_UHS2_ERR_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00CCh

Figure 14-8026. MMCSD1_UHS2_ERR_INTR_SIG_ENA Register

31	30	29	28	27	26	25	24
VENDOR_SPECFIC					RESERVED		
R/W-0h					R-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADMA2_ADMA3	RESERVED						EBSY
R/W-0h	R-0h						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED_SIG_ENA	RESP_PKT	HEADER
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24318. MMCSD1_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECFIC	R/W	0h	Vendor Specific Error Setting of a bit to 1h in this field enables generating interrupt signal when correspondent bit of Vendor Specific Error is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Timeout for Deadlock Setting this bit to 1h enables generating interrupt signal when Timeout for Dead lock bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

Table 14-24318. MMCSD1_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W	0h	Timeout for CMD_RES Setting this bit to 1h enables generating interrupt signal when Timeout for CMD_RES bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
15	ADMA2_ADMA3	R/W	0h	ADMA2/3 Error Setting this bit to 1h enables generating interrupt signal when ADMA2/3 Error bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W	0h	EBSY Error Setting this bit to 1h enables generating interrupt signal when EBSY Error bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
7	UNRECOVERABLE	R/W	0h	Unrecoverable Error Setting this bit to 1h enables generating interrupt signal when Unrecoverable Error bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
6	RESERVED	R	0h	Reserved
5	TID	R/W	0h	TID Error Setting this bit to 1h enables generating interrupt signal when TID Error bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
4	FRAMING	R/W	0h	Framing Error Setting this bit to 1h enables generating interrupt signal when Framing Error bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

Table 14-24318. MMCSD1_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CRC	R/W	0h	CRC Error Setting this bit to 1h enables generating interrupt signal when CRC Error bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
2	RETRY_EXPIRED_SIG_ENA	R/W	0h	Retry Expired Setting this bit to 1h enables generating interrupt signal when Retry Expired bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
1	RESP_PKT	R/W	0h	RES Packet Error Setting this bit to 1h enables generating interrupt signal when RES Packet Error bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
0	HEADER	R/W	0h	Header Error Setting this bit to 1h enables generating interrupt signal when Header Error bit is set in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

60 MMCSD1_UHS2_SETTINGS_PTR Register (Offset = E0h) [reset = 100h]

MMCSD1_UHS2_SETTINGS_PTR is shown in Figure 14-8027 and described in Table 14-16294.

Return to Summary Table.

This register is pointer for UHS-II settings.

Table 14-24319. MMCSD1_UHS2_SETTINGS_PTR Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00E0h

Figure 14-8027. MMCSD1_UHS2_SETTINGS_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_SETTINGS_PTR															
R-100h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24321. MMCSD1_UHS2_SETTINGS_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_SETTINGS_PTR	R	100h	Pointer for UHS-II Settings Register

61 MMCSD1_UHS2_CAPABILITIES_PTR Register (Offset = E2h) [reset = 110h]

MMCSD1_UHS2_CAPABILITIES_PTR is shown in Figure 14-8028 and described in Table 14-16296.

Return to Summary Table.

This register is pointer for UHS-II Capabilities Register.

Table 14-24322. MMCSD1_UHS2_CAPABILITIES_PTR Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00E2h

Figure 14-8028. MMCSD1_UHS2_CAPABILITIES_PTR Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">UHS2_CAPABILITIES_PTR</td></tr>
<tr><td colspan="16">R-110h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24324. MMCSD1_UHS2_CAPABILITIES_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_CAPABILITIES_PTR	R	110h	Pointer for UHS-II Capabilities Register

62 MMCSD1_UHS2_TEST_PTR Register (Offset = E4h) [reset = 120h]

MMCSD1_UHS2_TEST_PTR is shown in Figure 14-8029 and described in Table 14-16298.

Return to Summary Table.

This register is pointer for UHS-II Test Register.

Table 14-24325. MMCSD1_UHS2_TEST_PTR Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00E4h

Figure 14-8029. MMCSD1_UHS2_TEST_PTR Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">UHS2_TEST_PTR</td></tr>
<tr><td colspan="16">R-120h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24327. MMCSD1_UHS2_TEST_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_TEST_PTR	R	120h	Pointer for UHS-II Test Register

63 MMCSD1_SHARED_BUS_CTRL_PTR Register (Offset = E6h) [reset = 130h]

MMCSD1_SHARED_BUS_CTRL_PTR is shown in Figure 14-8030 and described in Table 14-16300.

Return to Summary Table.

This register is pointer for UHS-II Shared Bus Control Register.

Table 14-24328. MMCSD1_SHARED_BUS_CTRL_PTR Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00E6h

Figure 14-8030. MMCSD1_SHARED_BUS_CTRL_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHARED_BUS_CTRL_PTR															
R-130h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24330. MMCSD1_SHARED_BUS_CTRL_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SHARED_BUS_CTRL_PTR	R	130h	Pointer for Shared Bus Control Register

64 MMCSD1_VENDOR_SPECFIC_PTR Register (Offset = E8h) [reset = 140h]

MMCSD1_VENDOR_SPECFIC_PTR is shown in Figure 14-8031 and described in Table 14-16302.

Return to Summary Table.

This register is pointer for UHS-II Vendor Specific Register.

Table 14-24331. MMCSD1_VENDOR_SPECFIC_PTR Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00E8h

Figure 14-8031. MMCSD1_VENDOR_SPECFIC_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR_SPECFIC_PTR															
R-140h															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24333. MMCSD1_VENDOR_SPECFIC_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_SPECFIC_PTR	R	140h	Pointer for Vendor Specific Area

65 MMCSD1_BOOT_TIMEOUT_CONTROL Register (Offset = F4h) [reset = 0h]

MMCSD1_BOOT_TIMEOUT_CONTROL is shown in Figure 14-8032 and described in Table 14-16304.

Return to Summary Table.

This is used to program the boot timeout value counter.

Table 14-24334. MMCSD1_BOOT_TIMEOUT_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00F4h

Figure 14-8032. MMCSD1_BOOT_TIMEOUT_CONTROL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_TIMEOUT_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-24336. MMCSD1_BOOT_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_TIMEOUT_CNT	R/W	0h	Boot Data Timeout Counter Value This value determines the interval by which DAT line timeouts are detected during boot operation for eMMC4.4 card. The value is in number of SD clock.

66 MMCSD1_VENDOR_REGISTER Register (Offset = F8h) [reset = 4E20h]

MMCSD1_VENDOR_REGISTER is shown in Figure 14-8033 and described in Table 14-16306.

Return to Summary Table.

Vendor register added for Auto Gate SD CLK, CMD11 Power Down Timer, Enhanced Strobe and eMMC Hardware Reset.

Table 14-24337. MMCSD1_VENDOR_REGISTER Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00F8h

Figure 14-8033. MMCSD1_VENDOR_REGISTER Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>AUTOGATE_SDCLK</td></tr>
<tr><td colspan="7">R-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CMD11_PD_TIMER</td></tr>
<tr><td colspan="8">R/W-1388h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">CMD11_PD_TIMER</td><td>EMMC_HW_RESET</td><td>ENHANCED_STROBE</td></tr>
<tr><td colspan="6">R/W-1388h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24339. MMCSD1_VENDOR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	AUTOGATE_SDCLK	R/W	0h	Auto Gate SD CLK If this bit is set, SD CLK will be gated automatically when there is no transfer. This is applicable only for Embedded Device. 0h: Disable 1h: Enable
15-2	CMD11_PD_TIMER	R/W	1388h	CMD11 Power Down Timer Value

Table 14-24339. MMCSD1_VENDOR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EMMC_HW_RESET	R/W	0h	eMMC Hardware Reset Hardware reset signal is generared for eMMC card when this bit is set. 0h: De-sassert hardware reset pin 1h: Drives the hardware reset pin as ZERO (Active LOW to eMMC card)
0	ENHANCED_STROBE	R/W	0h	Enhanced Strobe This bit enables the enhanced strobe logic of the Host Controller.

67 MMCSD1_SLOT_INT_STS Register (Offset = FCh) [reset = 0h]

MMCSD1_SLOT_INT_STS is shown in Figure 14-8034 and described in Table 14-16308.

Return to Summary Table.

This register is used to read the interrupt signal for each slot.

Table 14-24340. MMCSD1_SLOT_INT_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00FCh

Figure 14-8034. MMCSD1_SLOT_INT_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTR_SIG							
R-0h							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24342. MMCSD1_SLOT_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	INTR_SIG	R	0h	Interrupt Signal for Slot#0 These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

68 MMCSD1_HOST_CONTROLLER_VER Register (Offset = FEh) [reset = 1004h]

MMCSD1_HOST_CONTROLLER_VER is shown in Figure 14-8035 and described in Table 14-16310.

Return to Summary Table.

This register is used to read the vendor version number and specification version number.

Table 14-24343. MMCSD1_HOST_CONTROLLER_VER Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 00FEh

Figure 14-8035. MMCSD1_HOST_CONTROLLER_VER Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VEN_VER_NUM</td></tr>
<tr><td colspan="8">R-10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SPEC_VER_NUM</td></tr>
<tr><td colspan="8">R-4h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24345. MMCSD1_HOST_CONTROLLER_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	VEN_VER_NUM	R	10h	Vendor Version Number The Vendor Version Number is set to 10h (1.0)
7-0	SPEC_VER_NUM	R	4h	Specification Version Number This status indicates the Host Controller Specification Version. The upper and lower 4-bits indicate the version. 0h: SD Host Controller Specification Version 1.00 1h: SD Host Controller Specification Version 2.00 Including the feature of the ADMA and Test Register 2h: SD Host Controller Specification Version 3.00 3h: SD Host Controller Specification Version 4.00 4h: SD Host Controller Specification Version 4.10 Others: Reserved

69 MMCSD1_UHS2_GEN_SETTINGS Register (Offset = 100h) [reset = 0h]

MMCSD1_UHS2_GEN_SETTINGS is shown in Figure 14-8036 and described in Table 14-16312.

Return to Summary Table.

Start Address of General settings is pointed by the MMCSD1_UHS2_SETTINGS_PTR Register.

Table 14-24346. MMCSD1_UHS2_GEN_SETTINGS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0100h

Figure 14-8036. MMCSD1_UHS2_GEN_SETTINGS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		NUMLANES					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED							POWER_MODE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24348. MMCSD1_UHS2_GEN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	NUMLANES	R/W	0h	Number of Lanes and Functionalities The lane configuration of a Host System is set to this field depends on the capability among Host Controller and connected devices. 2 Lanes FD mode is mandatory and the others modes are optional. 0h: 2 Lanes FD or 2L-HD 1h: Not Used 2h: 3 Lanes 2D1U-FD (Embedded) 3h: 3 Lanes 1D2U-FD (Embedded) 4h: 4 Lanes 2D2U-FD (Embedded) Others: Reserved
7-1	RESERVED	R	0h	Reserved

Table 14-24348. MMCSD1_UHS2_GEN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POWER_MODE	R/W	0h	Power Mode This field determines either Fast mode or Low Power mode. Host and all devices connected to the host shall be set to the same mode. 0h: Fast Mode 1h: Low Power Mode

70 MMCSD1_UHS2_PHY_SETTINGS Register (Offset = 104h) [reset = 0h]

MMCSD1_UHS2_PHY_SETTINGS is shown in Figure 14-8037 and described in Table 14-16314.

Return to Summary Table.

Start Address of PHY settings is pointed by the MMCSD1_UHS2_SETTINGS_PTR Register.

Table 14-24349. MMCSD1_UHS2_PHY_SETTINGS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0104h

Figure 14-8037. MMCSD1_UHS2_PHY_SETTINGS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
N_LSS_DIR				N_LSS_SYN			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
HIBERNATE_ENA	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
SPEED_RANGE		RESERVED					
R/W-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24351. MMCSD1_UHS2_PHY_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	N_LSS_DIR	R/W	0h	Host N_LSS_DIR The largest value of N_LSS_DIR capabilities among the Host Controller and Connected Devices is set to this field. 0h: 8 x 16 LSS 1h: 8 x 1 LSS 2h: 8 x 2 LSS 3h: 8 x 3 LSS .... Fh: 8 x 15 LSS

Table 14-24351. MMCSD1_UHS2_PHY_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	N_LSS_SYN	R/W	0h	Host N_LSS_SYN The largest value of N_LSS_SYN capabilities among the Host Controller and Connected Devices is set to this field. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h - 4 x 3 LSS .... Fh: 4 x 15 LSS
15	HIBERNATE_ENA	R/W	0h	Hibernate Enable After checking card capability of Hibernate mode, if all devices support Hibernate mode, this bit may be set. This bit determines whether Host remains in Dormant state or goes to Hibernate state. In Hibernate mode, VDD1 Power may be off. 0h: Hibernate Disabled 1h: Hibernate Enabled
14-8	RESERVED	R	0h	Reserved
7-6	SPEED_RANGE	R/W	0h	Speed Range PLL multiplier is selected by this field. Change of PLL Multiplier is not effective immediately and is applied from exiting Dormant State. 0h: Range A (Defalt) 1h: Range B 2h: Reserved 3h: Reserved
5-0	RESERVED	R	0h	Reserved

71 MMCSD1_UHS2_LNK_TRN_SETTINGS Register (Offset = 108h) [reset = 0h]

MMCSD1_UHS2_LNK_TRN_SETTINGS is shown in Figure 14-8038 and described in Table 14-16316.

Return to Summary Table.

Start Address of LINK/TRAN settings is pointed by the MMCSD1_UHS2_SETTINGS_PTR Register.

Table 14-24352. MMCSD1_UHS2_LNK_TRN_SETTINGS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0108h

Figure 14-8038. MMCSD1_UHS2_LNK_TRN_SETTINGS Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
N_DATA_GAP							
R/W-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						RETRY_COUNT	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
HOST_NFCU							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24354. MMCSD1_UHS2_LNK_TRN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved

Table 14-24354. MMCSD1_UHS2_LNK_TRN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39-32	N_DATA_GAP	R/W	0h	Host N_DATA_GAP The largest value of N_DATA_GAP capabilities among the Host Controller and Connected Devices is set to this field. 00h: No Gap 01h: 1 LSS 02h: 2 LSS 03h: 3 LSS .... FFh: 255 LSS
31-18	RESERVED	R	0h	Reserved
17-16	RETRY_COUNT	R/W	0h	Retry Count Data Burst retry count is set to this field. 00h: Retry Disabled 01h: 1 time 02h: 2 times 03h: 3 times
15-8	HOST_NFCU	R/W	0h	Host N_FCU Host Driver sets the number of blocks in Data Burst (Flow Control) to this field. The value shall be smaller than or equal to N_FCU capabilities among the Host Controller and connected card and devices. Setting 1 to 4 blocks is recommended considering buffer size. 00h: 256 Blocks 01h: 1 Block 02h: 2 Blocks 03h: 3 Blocks .... FFh: 255 Blocks
7-0	RESERVED	R	0h	Reserved

72 MMCSD1_UHS2_GEN_CAP Register (Offset = 110h) [reset = 44F11h]

MMCSD1_UHS2_GEN_CAP is shown in Figure 14-8039 and described in Table 14-16318.

Return to Summary Table.

Start Address of General Capabilities is pointed by the MMCSD1_UHS2_GEN_CAP Register.

Table 14-24355. MMCSD1_UHS2_GEN_CAP Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0110h

Figure 14-8039. MMCSD1_UHS2_GEN_CAP Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">CORECFG_UHS2_BUS_TOPLOGY</td><td colspan="4">CORECFG_UHS2_MAX_DEVICES</td><td colspan="2">DEVICE_TYPE</td></tr>
<tr><td colspan="2">R-0h</td><td colspan="4">R-1h</td><td colspan="2">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>CFG_64BIT_ADDRESSING</td><td colspan="6">NUM_LANES</td></tr>
<tr><td>R-0h</td><td>R-1h</td><td colspan="6">R-Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">GAP</td><td colspan="4">DAP</td></tr>
<tr><td colspan="4">R-1h</td><td colspan="4">R-1h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-24357. MMCSD1_UHS2_GEN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-22	CORECFG_UHS2_BUS_TOPLOGY	R	0h	Bus Topology This field indicates one of bus topologies configured by a Host system. 0h: P2P Connection 1h: Ring Connection 2h: HUB Connection 3h: HUB is Connected in Ring

Table 14-24357. MMCSD1_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-18	CORECFG_UHS2_MAX_DEVICES	R	1h	Number of Devices Supported This field indicates the maximum number of devices supported by the Host Controller. 0h: Not used 1h: 1 Devices 2h: 2 Devices .... Fh: 15 Devices
17-16	DEVICE_TYPE	R	0h	Removable/Embedded This field indicates device type configured by a Host system. 0h: Removable Card (P2P) 1h: Embedded Devices 2h: Embedded Devices + Removable Card 3h: Reserved
15	RESERVED	R	0h	Reserved
14	CFG_64BIT_ADDRESSING	R	1h	64-bit Addressing This field indicates support of 64-bit addressing by the Host Controller. 0h: 32-bit Addressing is supported 1h: 32-bit and 64-bit Addressing is supported
13-8	NUM_LANES	R	Fh	Number of Lanes and Functionalities This field indicates support of lanes by the Host Controller. 0 mean not supported and 1 means supported. D08: 2L-HD D09: 2D1U-FD D10: 1D2U-FD D11: 2D2U-FD D12: Reserved D13: Reserved

Table 14-24357. MMCSD1_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	GAP	R	1h	GAP (Group Allocation Power) This field indicates the maximum capability of host power supply for a group configured by a Host system. This field is used to set the argument of DEVICE_INIT CCM. 0h: Not used 1h: 360 mW 2h: 720 mW .... Fh: 360 x 15 mW
3-0	DAP	R	1h	DAP (Device Allocation Power) This field indicates the maximum capability of host power supply for a device configured by a Host system. This field is used to set the argument of DEVICE_INIT CCMD. 0h: 360 mW (Default) 1h: 360 mW 2h: 720 mW .... Fh: 360 x 15 mW

73 MMCSD1_UHS2_PHY_CAP Register (Offset = 114h) [reset = 110000h]

MMCSD1_UHS2_PHY_CAP is shown in Figure 14-8040 and described in Table 14-16320.

Return to Summary Table.

Start Address of PHY Capabilities is pointed by the MMCSD1_UHS2_CAPABILITIES_PTR Register.

Table 14-24358. MMCSD1_UHS2_PHY_CAP Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0114h

Figure 14-8040. MMCSD1_UHS2_PHY_CAP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
N_LSS_DIR				N_LSS_SYN			
R-1h				R-1h			

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
SPEED_RANGE		RESERVED					
R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24360. MMCSD1_UHS2_PHY_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	N_LSS_DIR	R	1h	Host N_LSS_DIR This field indicates the minimum N_LSS_DIR required by the Host Controller. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h: 4 x 3 LSS .... Fh: 4 x 15 LSS

Table 14-24360. MMCSD1_UHS2_PHY_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	N_LSS_SYN	R	1h	Host N_LSS_SYN This field indicates the minimum N_LSS_SYN required by the Host Controller. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h: 4 x 3 LSS .... Fh: 4 x 15 LSS
15-8	RESERVED	R	0h	Reserved
7-6	SPEED_RANGE	R	0h	Speed Range This field indicates supported Speed Range by the Host Controller. 0h: Range A (Default) 1h: Range A and Range B 2h: Reserved 3h: Reserved
5-0	RESERVED	R	0h	Reserved

74 MMCSD1_UHS2_LNK_TRN_CAP Register (Offset = 118h) [reset = 8120000100h]

MMCSD1_UHS2_LNK_TRN_CAP is shown in Figure 14-8041 and described in Table 14-16322.

Return to Summary Table.

Start Address of LINK/TRAN settings is pointed by the MMCSD1_UHS2_CAPABILITIES_PTR Register.

Table 14-24361. MMCSD1_UHS2_LNK_TRN_CAP Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0118h

Figure 14-8041. MMCSD1_UHS2_LNK_TRN_CAP Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>56</td><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="8">N_DATA_GAP</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="8">R-81h</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="12">MAX_BLK_LENGTH</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="12">R-200h</td><td colspan="4">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">N_FCU</td><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-1h</td><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24363. MMCSD1_UHS2_LNK_TRN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39-32	N_DATA_GAP	R	81h	Host N_DATA_GAP This field indicates the minimum number of data gap (DIDL) supported by the Host Controller. 00h: No Gap 01h: 1 LSS 02h: 2 LSS 03h: 3 LSS .... FFh: 255 LSS

Table 14-24363. MMCSD1_UHS2_LNK_TRN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31-20	MAX_BLK_LENGTH	R	200h	Host Maximum Block Length This field indicates maximum block length by the Host Controller. 000h: Not Used 001h: 1 byte 002h: 2 bytes .... 200h: 512 bytes .... 800h: 2048 bytes 801h - FFFh: Not Used
19-16	RESERVED	R	0h	Reserved
15-8	N_FCU	R	1h	Host N_FCU This field indicates maximum the number of blocks in a Flow Control unit by the Host Controller. This value is determined by supported buffer size. 00h: 256 Blocks 01h: 1 Block 02h: 2 Block 03h: 3 Block .... FFh: 255 Blocks
7-0	RESERVED	R	0h	Reserved

75 MMCSD1_FORCE_UHSII_ERR_INT_STS Register (Offset = 120h) [reset = 0h]

MMCSD1_FORCE_UHSII_ERR_INT_STS is shown in Figure 14-8042 and described in Table 14-16324.

Return to Summary Table.

This register is not physically implemented, rather it is an address where the MMCSD1_UHS2_ERR_INTR_STS register can be written.

Table 14-24364. MMCSD1_FORCE_UHSII_ERR_INT_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0120h

Figure 14-8042. MMCSD1_FORCE_UHSII_ERR_INT_STS Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC					RESERVED		
W-0h					R-0h		

23	22	21	20	19	18	17	16
RESERVED						TIMEOUT_DEADLOCK	TIMEOUT_CMD_RES
R-0h						W-0h	W-0h

15	14	13	12	11	10	9	8
ADMA	RESERVED						EBSY
W-0h	R-0h						W-0h

7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RES_PKT	HEADER
W-0h	R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 14-24366. MMCSD1_FORCE_UHSII_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC	W	0h	Force Event for Vendor Specific Error 0h: Not Affected 1h: Vendor Specific Error Status is set
26-18	RESERVED	R	0h	Reserved
17	TIMEOUT_DEADLOCK	W	0h	Force Event for Timeout for Deadlock Setting this bit forces the Host Controller to set Timeout for Deadlock in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Timeout for Deadlock Error status is set

Table 14-24366. MMCSD1_FORCE_UHSII_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TIMEOUT_CMD_RES	W	0h	Force Event for Timeout for CMD_RES Setting this bit forces the Host Controller to set Timeout for CMD_RES in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Timout for CMD_RES Status is set
15	ADMA	W	0h	Force Event for ADMA Error Setting this bit forces the Host Controller to set ADMA Error in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: ADMA Error Status is set
14-9	RESERVED	R	0h	Reserved
8	EBSY	W	0h	Force Event for EBSY Error Setting this bit forces the Host Controller to set EBSY Error in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: EBSY Error Status is set
7	UNRECOVERABLE	W	0h	Force Event for Unrecoverable Error Setting this bit forces the Host Controller to set Unrecoverable Error in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Unrecoverable Error Status is set
6	RESERVED	R	0h	Reserved
5	TID	W	0h	Force Event for TID Error Setting this bit forces the Host Controller to set TID Error in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: TID Error Status is set
4	FRAMING	W	0h	Force Event for Framing Error Setting this bit forces the Host Controller to set Framing Error in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Framing Error Status is set

Table 14-24366. MMCSD1_FORCE_UHSII_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CRC	W	0h	Force Event for CRC Error Setting this bit forces the Host Controller to set CRC Error in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: CRC Error Status is set
2	RETRY_EXPIRED	W	0h	Force Event for Retry Expired Setting this bit forces the Host Controller to set Retry Expired in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Retry expired error status is set
1	RES_PKT	W	0h	Force Event for RES Packet Error Setting this bit forces the Host Controller to set RES Packet Error in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: RES packet error status is set
0	HEADER	W	0h	Force Event for Header Error Setting this bit forces the Host Controller to set Header Error in the MMCSD1_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Header error status is set

76 MMCSD1_CQ_VERSION Register (Offset = 200h) [reset = 510h]

MMCSD1_CQ_VERSION is shown in Figure 14-8043 and described in Table 14-16326.

Return to Summary Table.

This register provides information about the version of the eMMC CQ (Command Queueing) standard which is 285 implemented by the CQE, in BCD format. The current version is rev 5.1.

The following table describes the CQBASE+00h: Command Queueing Version.

Table 14-24367. MMCSD1_CQ_VERSION Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0200h

Figure 14-8043. MMCSD1_CQ_VERSION Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">EMMC_MAJOR_VER_NUM</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R-5h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">EMMC_MINOR_VER_NUM</td><td colspan="4">EMMC_VERSION_SUFFIX</td></tr>
<tr><td colspan="4">R-1h</td><td colspan="4">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24369. MMCSD1_CQ_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	EMMC_MAJOR_VER_NUM	R	5h	eMMC Major Version Number (digit left of decimal point), in BCD format
7-4	EMMC_MINOR_VER_NUM	R	1h	eMMC Minor Version Number (digit right of decimal point), in BCD format
3-0	EMMC_VERSION_SUFFIX	R	0h	eMMC Version Suffix (2nd digit right of decimal point), in BCD format

77 MMCSD1_CQ_CAPABILITIES Register (Offset = 204h) [reset = 30C8h]

MMCSD1_CQ_CAPABILITIES is shown in Figure 14-8044 and described in Table 14-16328.

Return to Summary Table.

This register is reserved for capability indication.

Table 14-24370. MMCSD1_CQ_CAPABILITIES Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0204h

Figure 14-8044. MMCSD1_CQ_CAPABILITIES Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CF_MUL				RESERVED		CF_VAL	
R-3h				R-0h		R-C8h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CF_VAL							
R-C8h							

LEGEND: R = Read Only; *-n* = value after reset

Table 14-24372. MMCSD1_CQ_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	CF_MUL	R	3h	**Internal Timer Clock Frequency Multiplier (ITCFMUL)** ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details (MMCSD1_CQ_CAPABILITIES[9-0] CF_VAL). Field Value Description: 0h: 0.001 MHz 1h: 0.01 MHz 2h: 0.1 MHz 3h: 1 MHz 4h: 10 MHz Other values are reserved
11-10	RESERVED	R	0h	Reserved

Table 14-24372. MMCSD1_CQ_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	CF_VAL	R	C8h	**Internal Timer Clock Frequency Value (ITCFVAL)** ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the polling period when using periodic SEND_QUEUE_STATUS (CMD13) polling. The clock frequency is calculated as ITCFVAL × ITCFMUL. For example, to encode 19.2 MHz ITCFVAL shall be C0h (= 192 decimal) and ITCFMUL shall be 2h (0.1 MHz). 192 × 0.1 MHz = 19.2 MHz

78 MMCSD1_CQ_CONFIG Register (Offset = 208h) [reset = 0h]

MMCSD1_CQ_CONFIG is shown in Figure 14-8045 and described in Table 14-16330.

Return to Summary Table.

This register controls CQE behavior affecting the general operation of command queueing 290 module or operation of multiple tasks in the same time.

Table 14-24373. MMCSD1_CQ_CONFIG Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0208h

Figure 14-8045. MMCSD1_CQ_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			DCMD_ENA	RESERVED			TASK_DESC_SIZE
R-0h			R/W-0h	R-0h			R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CQ_ENABLE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24375. MMCSD1_CQ_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	DCMD_ENA	R/W	0h	**Direct Command (DCMD) Enable** This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 0h: Task descriptor in slot #31 is a Data Transfer Task Descriptor 1h: Task descriptor in slot #31 is a DCMD Task Descriptor
11-9	RESERVED	R	0h	Reserved

Table 14-24375. MMCSD1_CQ_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TASK_DESC_SIZE	R/W	0h	**Task Descriptor Size** This bit indicates whether the task descriptor size is 128 bits or 64 bits . This bit can only be configured when the MMCSD1_CQ_CONFIG[0] CQ_ENABLE bit is 0h (command queueing is disabled). Bit Value Description 0h: Task descriptor size is 64 bits 1h: Task descriptor size is 128 bits
7-1	RESERVED	R	0h	Reserved
0	CQ_ENABLE	R/W	0h	**Command Queueing Enable** Software shall write 1h to this bit when in order to enable command queueing mode (enable CQE). When this bit is 0h, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes 1h to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queueing mode, it shall clear all previous tasks if such exist before setting this bit to 0h.

79 MMCSD1_CQ_CONTROL Register (Offset = 20Ch) [reset = 0h]

MMCSD1_CQ_CONTROL is shown in Figure 14-8046 and described in Table 14-16332.

Return to Summary Table.

This register controls CQE behavior affecting the general operation of command queueing 293 module or operation of multiple tasks in the same time.

Table 14-24376. MMCSD1_CQ_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 020Ch

Figure 14-8046. MMCSD1_CQ_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CLEAR_ALL_TASKS
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							HALT_BIT
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24378. MMCSD1_CQ_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CLEAR_ALL_TASKS	R/W	0h	**Clear All Tasks** Software shall write 1h to this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state (Halt bit is 1h). When software writes 1h, the value of the register is updated to 1h, and CQE shall reset the MMCSD1_CQ_TASK_DOOR_BELL register and all other context information for all unfinished tasks. Then CQE will clear this bit. Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is softwares responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0h to this register shall have no effect.
7-1	RESERVED	R	0h	Reserved

Table 14-24378. MMCSD1_CQ_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_BIT	R/W	0h	**Halt** Host software shall write 1h to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT). When software writes 1h, CQE shall complete the ongoing task if such a task is in progress. Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1h. Software may poll on this bit until it is set to 1h, and may only then send commands on the eMMC bus. In order to exit halt state (resume CQE activity), software shall clear this bit (write 0h). Writing 0h when the value is already 0h shall have no effect.

80 MMCSD1_CQ_INTR_STS Register (Offset = 210h) [reset = 0h]

MMCSD1_CQ_INTR_STS is shown in Figure 14-8047 and described in Table 14-16334.

Return to Summary Table.

This register indicates pending interrupts that require service. Each bit in this registers is asserted 296 in response a specific event, only if the respective bit is set in the MMCSD1_CQ_INTR_STS_ENA register.

Table 14-24379. MMCSD1_CQ_INTR_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0210h

Figure 14-8047. MMCSD1_CQ_INTR_STS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-24381. MMCSD1_CQ_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W1C	0h	**Task Error Interrupt (TERR)** This bit is asserted when task error is detected due to invalid task descriptor.
3	TASK_CLEARED	R/W1C	0h	**Task Cleared (TCL)** This status bit is asserted (if MMCSD1_CQ_INTR_STS_ENA[3] TASK_CLEARED = 1h) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (MMCSD1_CQ_TASK_CLEAR) or clearing of all tasks (MMCSD1_CQ_CONTROL).

Table 14-24381. MMCSD1_CQ_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W1C	0h	**Response Error Detected Interrupt (RED)** This status bit is asserted (if MMCSD1_CQ_INTR_STS_ENA[2] RESP_ERR_DET = 1h) when a response is received with an error bit set in the device status field. Software uses the MMCSD1_CQ_RESP_ERR_MASK register to configure which device status bit fields may trigger an interrupt, and which are masked.
1	TASK_COMPLETE	R/W1C	0h	**Task Complete Interrupt (TCC)** This status bit is asserted (if MMCSD1_CQ_INTR_STS_ENA[1] TASK_COMPLETE = 1h) when at least one of the following two conditions are met: (1) A task is completed and the INT bit is set in its Task Descriptor (2) Interrupt caused by Interrupt Coalescing logic
0	HALT_COMPLETE	R/W1C	0h	**Halt Complete Interrupt (HAC)** This status bit is asserted (if MMCSD1_CQ_INTR_STS_ENA[0] HALT_COMPLETE = 1h) when the MMCSD1_CQ_CONTROL[0] HALT_BIT bit transitions from 0h to 1h indicating that host controller has completed its current ongoing task and has entered halt state.

81 MMCSD1_CQ_INTR_STS_ENA Register (Offset = 214h) [reset = 0h]

MMCSD1_CQ_INTR_STS_ENA is shown in Figure 14-8048 and described in Table 14-16336.

Return to Summary Table.

This register enables and disables the reporting of the corresponding interrupt to host software in 299 MMCSD1_CQ_INTR_STS register. When a bit is set (1h) and the corresponding interrupt condition is active, then the 300 bit in the MMCSD1_CQ_INTR_STS register is asserted. Interrupt sources that are disabled (0h) are not indicated in the MMCSD1_CQ_INTR_STS 301 register. This register is bit-index matched to the MMCSD1_CQ_INTR_STS register.

Table 14-24382. MMCSD1_CQ_INTR_STS_ENA Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0214h

Figure 14-8048. MMCSD1_CQ_INTR_STS_ENA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24384. MMCSD1_CQ_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W	0h	**Task Error Interrupt Status Enable (TERR)** 1h: MMCSD1_CQ_INTR_STS[4] TASK_ERROR bit will be set when its interrupt condition is active 0h: MMCSD1_CQ_INTR_STS[4] TASK_ERROR bit is disabled
3	TASK_CLEARED	R/W	0h	**Task Cleared Status Enable (TCL)** 1h: MMCSD1_CQ_INTR_STS[3] TASK_CLEARED bit will be set when its interrupt condition is active 0h: MMCSD1_CQ_INTR_STS[3] TASK_CLEARED bit is disabled

Table 14-24384. MMCSD1_CQ_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESP_ERR_DET	R/W	0h	**Response Error Detected Status Enable (RED)** 1h: MMCSD1_CQ_INTR_STS[2] RESP_ERR_DET bit will be set when its interrupt condition is active 0h: MMCSD1_CQ_INTR_STS[2] RESP_ERR_DET bit is disabled
1	TASK_COMPLETE	R/W	0h	**Task Complete Status Enable (TCC)** 1h: MMCSD1_CQ_INTR_STS[1] TASK_COMPLETE bit will be set when its interrupt condition is active 0h: MMCSD1_CQ_INTR_STS[1] TASK_COMPLETE bit is disabled
0	HALT_COMPLETE	R/W	0h	**Halt Complete Status Enable (HAC)** 1h: MMCSD1_CQ_INTR_STS[0] HALT_COMPLETE bit will be set when its interrupt condition is active 0h: MMCSD1_CQ_INTR_STS[0] HALT_COMPLETE bit is disabled

82 MMCSD1_CQ_INTR_SIG_ENA Register (Offset = 218h) [reset = 0h]

MMCSD1_CQ_INTR_SIG_ENA is shown in Figure 14-8049 and described in Table 14-16338.

Return to Summary Table.

This register enables and disables the generation of interrupts to host software. When a bit is set 304 (1h) and the corresponding bit in the MMCSD1_CQ_INTR_STS register is set, then an interrupt is generated. Interrupt sources 305 that are disabled (0h) are still indicated in the MMCSD1_CQ_INTR_STS register. This register is bit-index matched 306 to the MMCSD1_CQ_INTR_STS register.

Table 14-24385. MMCSD1_CQ_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0218h

Figure 14-8049. MMCSD1_CQ_INTR_SIG_ENA Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>TASK_ERROR</td><td>TASK_CLEARED</td><td>RESP_ERR_DET</td><td>TASK_COMPLETE</td><td>HALT_COMPLETE</td></tr>
<tr><td colspan="3">R-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24387. MMCSD1_CQ_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W	0h	**Task Error Interrupt Signal Enable (TERR)** When set and the MMCSD1_CQ_INTR_STS[4] TASK_ERROR bit is asserted, the CQE shall generate an interrupt.
3	TASK_CLEARED	R/W	0h	**Task Cleared Signal Enable (TCL)** When set and the MMCSD1_CQ_INTR_STS[3] TASK_CLEARED bit is asserted, the CQE shall generate an interrupt.
2	RESP_ERR_DET	R/W	0h	**Response Error Detected Signal Enable (RED)** When set and the MMCSD1_CQ_INTR_STS[2] RESP_ERR_DET bit is asserted, the CQE shall generate an interrupt.
1	TASK_COMPLETE	R/W	0h	**Task Complete Signal Enable (TCC)** When set and the MMCSD1_CQ_INTR_STS[1] TASK_COMPLETE bit is asserted, the CQE shall generate an interrupt.

Table 14-24387. MMCSD1_CQ_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_COMPLETE	R/W	0h	**Halt Complete Signal Enable (HAC)** When set and the MMCSD1_CQ_INTR_STS[0] HALT_COMPLETE bit is asserted, the CQE shall generate an interrupt.

83 MMCSD1_CQ_INTR_COALESCING Register (Offset = 21Ch) [reset = 0h]

MMCSD1_CQ_INTR_COALESCING is shown in Figure 14-8050 and described in Table 14-16340.

Return to Summary Table.

This register controls the interrupt coalescing feature.

Table 14-24388. MMCSD1_CQ_INTR_COALESCING Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 021Ch

Figure 14-8050. MMCSD1_CQ_INTR_COALESCING Register

31	30	29	28	27	26	25	24
CQINTCOALESC_ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED			IC_STATUS	RESERVED			
R-0h			R-0h	R-0h			
15	14	13	12	11	10	9	8
RESERVED			CTR_THRESHOLD				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED	TIMEOUT_VAL						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24390. MMCSD1_CQ_INTR_COALESCING Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CQINTCOALESC_ENABLE	R/W	0h	**Interrupt Coalescing Enable/Disable:** When set to 0h by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT = 1 in the Task Descriptor. When set to 1h, the interrupt coalescing mechanism is enabled and coalesced interrupts are generated.
30-21	RESERVED	R	0h	Reserved
20	IC_STATUS	R	0h	**Interrupt Coalescing Status Bit (ICSB):** This bit indicates to software whether any tasks (with INT = 0) have completed and counted towards interrupt coalescing (ICSB is set if and only if IC counter > 0). Bit Value Description 0h: No task completions have occurred since last counter reset (IC counter = 0) 1h: At least one task completion has been counted (IC counter > 0)
19-13	RESERVED	R	0h	Reserved

Table 14-24390. MMCSD1_CQ_INTR_COALESCING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	CTR_THRESHOLD	R/W	0h	**Interrupt Coalescing Counter Threshold (ICCTH):** Software uses this field to configure the number of task completions (only tasks with INT = 0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT = 0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31. **Note:** When ICCTH is 0h, task completions are not counted, and counting-based interrupts are not generated.
7	RESERVED	R	0h	Reserved
6-0	TIMEOUT_VAL	R/W	0h	**Interrupt Coalescing Timeout Value (ICTOVAL):** Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT = 0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timers unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field in the MMCSD1_CQ_CAPABILITIES register. The minimum value is 1h (1024 clock periods) and the maximum value is 7Fh (127 × 1024 clock periods). For example, a MMCSD1_CQ_CAPABILITIES field value of 0h indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is 16 × 1024 × 52.08 ns = 853.33 μs **Note:** When ICTOVAL is 0h, the timer is not running, and timer-based interrupts are not generated.

84 MMCSD1_CQ_TDL_BASE_ADDR Register (Offset = 220h) [reset = 0h]

MMCSD1_CQ_TDL_BASE_ADDR is shown in Figure 14-8051 and described in Table 14-16342.

Return to Summary Table.

This register is used for configuring the lower 32 bits of the byte address of the head of the Task 312 Descriptor List in the host memory.

Table 14-24391. MMCSD1_CQ_TDL_BASE_ADDR Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0220h

Figure 14-8051. MMCSD1_CQ_TDL_BASE_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTDLBA_LO																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-24393. MMCSD1_CQ_TDL_BASE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTDLBA_LO	R/W	0h	**Task Descriptor List Base Address (TDLBA)** This register stores the LSB bits (bits 31-0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 × (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on Byte1 KByte boundary. The lower 10 bits of this register shall be set to 0h by software and shall be ignored by CQE.

85 MMCSD1_CQ_TDL_BASE_ADDR_UPBITS Register (Offset = 224h) [reset = 0h]

MMCSD1_CQ_TDL_BASE_ADDR_UPBITS is shown in Figure 14-8052 and described in Table 14-16344.

Return to Summary Table.

This register is used for configuring the upper 32 bits of the byte address of the head of the Task 316 Descriptor List in the host memory.

Table 14-24394. MMCSD1_CQ_TDL_BASE_ADDR_UPBITS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0224h

Figure 14-8052. MMCSD1_CQ_TDL_BASE_ADDR_UPBITS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTDLBA_HI																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-24396. MMCSD1_CQ_TDL_BASE_ADDR_UPBITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTDLBA_HI	R/W	0h	**Task Descriptor List Base Address (TDLBA)** This register stores the MSB bits (bits 63-32) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 × (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This register is reserved when using 32-bit addressing mode.

86 MMCSD1_CQ_TASK_DOOR_BELL Register (Offset = 228h) [reset = 0h]

MMCSD1_CQ_TASK_DOOR_BELL is shown in Figure 14-8053 and described in Table 14-16346.

Return to Summary Table.

Using this register, software triggers CQE to process a new task.

Table 14-24397. MMCSD1_CQ_TASK_DOOR_BELL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0228h

Figure 14-8053. MMCSD1_CQ_TASK_DOOR_BELL Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CQTDB_VAL</td></tr>
<tr><td colspan="32">W1S-0h</td></tr>
</table>

LEGEND: W1S = Write 1 to Set Bit; -*n* = value after reset

Table 14-24399. MMCSD1_CQ_TASK_DOOR_BELL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTDB_VAL	W1S	0h	**Command Queueing Task Doorbell** Software shall configure the MMCSD1_CQ_TDL_BASE_ADDR[31-0] CQTDLBA_LO and MMCSD1_CQ_TDL_BASE_ADDR_UPBITS[31-0] CQTDLBA_HI bit fields, and enable CQE in the MMCSD1_CQ_CONFIG register before using this register. Writing 1h to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by the MMCSD1_CQ_TASK_DOOR_BELL register write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0h by CQE in one of the following events: (a) When a task execution is completed (with success or error) (b) The task is cleared using MMCSD1_CQ_TASK_CLEAR register (c) All tasks are cleared using MMCSD1_CQ_CONTROL register (d) CQE is disabled using MMCSD1_CQ_CONFIG register Software may initiate multiple tasks at the same time (batch submission) by writing 1h to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order. Writing 0h by software shall have no impact on the hardware, and will not change the value of the register bit.

87 MMCSD1_CQ_TASK_COMP_NOTIF Register (Offset = 22Ch) [reset = 0h]

MMCSD1_CQ_TASK_COMP_NOTIF is shown in Figure 14-8054 and described in Table 14-16348.

Return to Summary Table.

This register is used by CQE to notify software about completed tasks.

Table 14-24400. MMCSD1_CQ_TASK_COMP_NOTIF Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 022Ch

Figure 14-8054. MMCSD1_CQ_TASK_COMP_NOTIF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTCN_VAL																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-24402. MMCSD1_CQ_TASK_COMP_NOTIF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTCN_VAL	R/W1C	0h	**Task Complete Notification** CQE shall set bit n of this register (at the same time it clears bit n of the MMCSD1_CQ_TASK_DOOR_BELL register) when a task execution is completed (with success or error). When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1h to the corresponding bits.

88 MMCSD1_CQ_DEV_QUEUE_STATUS Register (Offset = 230h) [reset = 0h]

MMCSD1_CQ_DEV_QUEUE_STATUS is shown in Figure 14-8055 and described in Table 14-16350.

Return to Summary Table.

This register stores the most recent value of the device's queue status.

Table 14-24403. MMCSD1_CQ_DEV_QUEUE_STATUS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0230h

Figure 14-8055. MMCSD1_CQ_DEV_QUEUE_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQDQ_STS																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 14-24405. MMCSD1_CQ_DEV_QUEUE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQDQ_STS	R	0h	**Device Queue Status** Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command (the device's queue status).

89 MMCSD1_CQ_DEV_PENDING_TASKS Register (Offset = 234h) [reset = 0h]

MMCSD1_CQ_DEV_PENDING_TASKS is shown in Figure 14-8056 and described in Table 14-16352.

Return to Summary Table.

This register indicates to software which tasks are queued in the device, awaiting execution.

Table 14-24406. MMCSD1_CQ_DEV_PENDING_TASKS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0234h

Figure 14-8056. MMCSD1_CQ_DEV_PENDING_TASKS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQDP_TSKS																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24408. MMCSD1_CQ_DEV_PENDING_TASKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQDP_TSKS	R	0h	**Device Pending Tasks** Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasnt been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using MMCSD1_CQ_CONTROL register.

90 MMCSD1_CQ_TASK_CLEAR Register (Offset = 238h) [reset = 0h]

MMCSD1_CQ_TASK_CLEAR is shown in Figure 14-8057 and described in Table 14-16354.

Return to Summary Table.

This register is used for removing an outstanding task in the CQE 327. The register should be used only when CQE is in Halt state.

Table 14-24409. MMCSD1_CQ_TASK_CLEAR Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0238h

Figure 14-8057. MMCSD1_CQ_TASK_CLEAR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CQTCLR</td></tr>
<tr><td colspan="32">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-24411. MMCSD1_CQ_TASK_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTCLR	R/W	0h	**Command Queueing Task Clear** Writing 1h to bit n of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in the MMCSD1_CQ_CONFIG register Halt bit. When software writes 1h to a bit in this register, CQE updates the value to 1h, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0h) in the MMCSD1_CQ_TASK_CLEAR and in MMCSD1_CQ_TASK_DOOR_BELL registers once clear operation is complete. Software should poll on the MMCSD1_CQ_TASK_CLEAR register until it is cleared to verify clear operation was complete. Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state. Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using MMCSD1_CQ_CONTROL register. Writing 0h to a register bit shall have no impact.

91 MMCSD1_CQ_SEND_STS_CONFIG1 Register (Offset = 240h) [reset = 11000h]

MMCSD1_CQ_SEND_STS_CONFIG1 is shown in Figure 14-8058 and described in Table 14-16356.

Return to Summary Table.

The register controls when the SEND_QUEUE_STATUS commands are sent.

Table 14-24412. MMCSD1_CQ_SEND_STS_CONFIG1 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0240h

Figure 14-8058. MMCSD1_CQ_SEND_STS_CONFIG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												CMD_BLK_CNTR			
R-0h												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMD_IDLE_TIMER															
R/W-1000h															

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24414. MMCSD1_CQ_SEND_STS_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	CMD_BLK_CNTR	R/W	1h	**Send Status Command Block Counter** This field indicates to CQE when to send SEND_QUEUE_STATUS (CMD13) command to inquire the status of the devices task queue. A value of n means CQE shall send status command on the CMD line, during the transfer of data block **BLOCK_CNT-n**, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. A value of 0h means that SEND_QUEUE_STATUS (CMD13) command shall not be sent during the transaction. Instead it will be sent only when the data lines are idle. A value of 1 means that STATUS command is to be sent during the last block of the transaction.

Table 14-24414. MMCSD1_CQ_SEND_STS_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	CMD_IDLE_TIMER	R/W	1000h	**Send Status Command Idle Timer** This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of theclock whose frequency is specified in the Internal Timer Clock Frequency field in the MMCSD1_CQ_CAPABILITIES register. The minimum value is 1h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is: 4096 clock periods. For example, a MMCSD1_CQ_CAPABILITIES field value of 0h indicates a 19.2 MHz clock frequency (period = 52.08 ns).

92 MMCSD1_CQ_SEND_STS_CONFIG2 Register (Offset = 244h) [reset = 0h]

MMCSD1_CQ_SEND_STS_CONFIG2 is shown in Figure 14-8059 and described in Table 14-16358.

Return to Summary Table.

This register is used for 333 configuring RCA field in SEND_QUEUE_STATUS command argument.

Table 14-24415. MMCSD1_CQ_SEND_STS_CONFIG2 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0244h

Figure 14-8059. MMCSD1_CQ_SEND_STS_CONFIG2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">RESERVED</td><td colspan="16">QUEUE_RCA</td></tr>
<tr><td colspan="16">R-0h</td><td colspan="16">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-24417. MMCSD1_CQ_SEND_STS_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	QUEUE_RCA	R/W	0h	**Send Queue RCA** This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE shall copy this field to bits 31-16 of the argument when transmitting SEND_QUEUE_STATUS (CMD13) command.

93 MMCSD1_CQ_DCMD_RESPONSE Register (Offset = 248h) [reset = 0h]

MMCSD1_CQ_DCMD_RESPONSE is shown in Figure 14-8060 and described in Table 14-16360.

Return to Summary Table.

This register is used for passing the response of a DCMD task to software.

Table 14-24418. MMCSD1_CQ_DCMD_RESPONSE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0248h

Figure 14-8060. MMCSD1_CQ_DCMD_RESPONSE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAST_RESP																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24420. MMCSD1_CQ_DCMD_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LAST_RESP	R	0h	**Direct Command Last Response** This register contains the response of the command generated by the last direct command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of the MMCSD1_CQ_TASK_DOOR_BELL register is cleared by CQE.

94 MMCSD1_CQ_RESP_ERR_MASK Register (Offset = 250h) [reset = FDF9A080h]

MMCSD1_CQ_RESP_ERR_MASK is shown in Figure 14-8061 and described in Table 14-16362.

Return to Summary Table.

This register controls the generation of Response Error Detection (RED) interrupt.

Table 14-24421. MMCSD1_CQ_RESP_ERR_MASK Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0250h

Figure 14-8061. MMCSD1_CQ_RESP_ERR_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQRMEM																															
R-FDF9A080h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24423. MMCSD1_CQ_RESP_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQRMEM	R	FDF9A080h	**Response Mode Error Mask** This bit is used as in interrupt mask on the device status field which is received in R1/R1b responses. Bit Value Description (for any bit i): 1h: When a R1/R1b response is received, with bit i in the device status set, a RED interrupt is generated 0h: When a R1/R1b response is received, bit i in the device status is ignored The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. **Note:** Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.

95 MMCSD1_CQ_TASK_ERR_INFO Register (Offset = 254h) [reset = 0h]

MMCSD1_CQ_TASK_ERR_INFO is shown in Figure 14-8062 and described in Table 14-16364.

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This register is updated by CQE when an error occurs on data or command related to a task activity. When such error is detected by CQE or indicated by the eMMC controller CQE stores in the MMCSD1_CQ_TASK_ERR_INFO register the task IDs and the command indices of the commands which were executed on the 343 command line and data lines when the error occurred.

Software is expected to use this information in the error recovery procedure.

Table 14-24424. MMCSD1_CQ_TASK_ERR_INFO Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0254h

Figure 14-8062. MMCSD1_CQ_TASK_ERR_INFO Register

31	30	29	28	27	26	25	24
DATERR_VALID	RESERVED		DATERR_TASK_ID				
R-0h	R-0h		R-0h				

23	22	21	20	19	18	17	16
RESERVED		DATERR_CMD_INDEX					
R-0h		R-0h					

15	14	13	12	11	10	9	8
RESP_MODE_VALID	RESERVED		RESP_MODE_TASK_ID				
R-0h	R-0h		R-0h				

7	6	5	4	3	2	1	0
RESERVED		RESP_MODE_CMD_INDEX					
R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24426. MMCSD1_CQ_TASK_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DATERR_VALID	R	0h	**Data Transfer Error Fields Valid** This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1h. If a no data transfer is in progress when the error is detected/ indicated, the bit is cleared to 0h.
30-29	RESERVED	R	0h	Reserved

Table 14-24426. MMCSD1_CQ_TASK_ERR_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	DATERR_TASK_ID	R	0h	**Data Transfer Error Task ID** This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23-22	RESERVED	R	0h	Reserved
21-16	DATERR_CMD_INDEX	R	0h	**Data Transfer Error Command Index** This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	RESP_MODE_VALID	R	0h	**Response Mode Error Fields Valid** This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/ indicated, the bit is set to 1h. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0h.
14-13	RESERVED	R	0h	Reserved
12-8	RESP_MODE_TASK_ID	R	0h	**Response Mode Error Task ID** This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7-6	RESERVED	R	0h	Reserved
5-0	RESP_MODE_CMD_INDEX	R	0h	**Response Mode Error Command Index** This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

96 MMCSD1_CQ_CMD_RESP_INDEX Register (Offset = 258h) [reset = 0h]

MMCSD1_CQ_CMD_RESP_INDEX is shown in Figure 14-8063 and described in Table 14-16366.

Return to Summary Table.

This register stores the index of the last received command response.

Table 14-24427. MMCSD1_CQ_CMD_RESP_INDEX Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0258h

Figure 14-8063. MMCSD1_CQ_CMD_RESP_INDEX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										LAST_CRI					
R-0h										R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24429. MMCSD1_CQ_CMD_RESP_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	LAST_CRI	R	0h	**Last Command Response Index** This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

97 MMCSD1_CQ_CMD_RESP_ARG Register (Offset = 25Ch) [reset = 0h]

MMCSD1_CQ_CMD_RESP_ARG is shown in Figure 14-8064 and described in Table 14-16368.

Return to Summary Table.

This register stores the index of the last received command response.

Table 14-24430. MMCSD1_CQ_CMD_RESP_ARG Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 025Ch

Figure 14-8064. MMCSD1_CQ_CMD_RESP_ARG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAST_CRA																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-24432. MMCSD1_CQ_CMD_RESP_ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LAST_CRA	R	0h	**Last Command Response Argument** This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

98 MMCSD1_CQ_ERROR_TASK_ID Register (Offset = 260h) [reset = 0h]

MMCSD1_CQ_ERROR_TASK_ID is shown in Figure 14-8065 and described in Table 14-16370.

Return to Summary Table.

CQ Error Task ID Register

Table 14-24433. MMCSD1_CQ_ERROR_TASK_ID Instances

Instance	Physical Address
MMCSD1_CTL_CFG	0FA0 0260h

Figure 14-8065. MMCSD1_CQ_ERROR_TASK_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											TERR_ID				
R-0h											R-0h				

LEGEND: R = Read Only; *-n* = value after reset

Table 14-24435. MMCSD1_CQ_ERROR_TASK_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	TERR_ID	R	0h	Task Error ID

14.9.4 Industrial and Control Interfaces Registers

14.9.4.1 MCAN

MCAN

14.9.4.1.1 MCAN Summaries

MCAN Summaries

Table 14-24436. MCAN Registers, Base Address=2070 0000h, Length=256

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address
0h	32	MCAN_PID	2070 0000h	2071 0000h
4h	32	MCAN_CTRL	2070 0004h	2071 0004h
8h	32	MCAN_STAT	2070 0008h	2071 0008h
Ch	32	MCAN_ICS	2070 000Ch	2071 000Ch
10h	32	MCAN_IRS	2070 0010h	2071 0010h
14h	32	MCAN_IECS	2070 0014h	2071 0014h
18h	32	MCAN_IE	2070 0018h	2071 0018h
1Ch	32	MCAN_IES	2070 001Ch	2071 001Ch
20h	32	MCAN_EOI	2070 0020h	2071 0020h
24h	32	MCAN_EXT_TS_PRESCALER	2070 0024h	2071 0024h
28h	32	MCAN_EXT_TS_UNSERVICED_INTR_CNTR	2070 0028h	2071 0028h

Table 14-24437. MCAN_CORE Registers, Base Address=2070 1000h, Length=512

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address
0h	32	MCAN_CORE_CREL	2070 1000h	2071 1000h
4h	32	MCAN_CORE_ENDN	2070 1004h	2071 1004h
8h	32	MCAN_CORE_CUST	2070 1008h	2071 1008h
Ch	32	MCAN_CORE_DBTP	2070 100Ch	2071 100Ch
10h	32	MCAN_CORE_TEST	2070 1010h	2071 1010h
14h	32	MCAN_CORE_RWD	2070 1014h	2071 1014h
18h	32	MCAN_CORE_CCCR	2070 1018h	2071 1018h
1Ch	32	MCAN_CORE_NBTP	2070 101Ch	2071 101Ch
20h	32	MCAN_CORE_TSCC	2070 1020h	2071 1020h
24h	32	MCAN_CORE_TSCV	2070 1024h	2071 1024h
28h	32	MCAN_CORE_TOCC	2070 1028h	2071 1028h
2Ch	32	MCAN_CORE_TOCV	2070 102Ch	2071 102Ch
30h	32	MCAN_CORE_RESERVED00	2070 1030h	2071 1030h
34h	32	MCAN_CORE_RESERVED11	2070 1034h	2071 1034h
38h	32	MCAN_CORE_RESERVED22	2070 1038h	2071 1038h
3Ch	32	MCAN_CORE_RESERVED33	2070 103Ch	2071 103Ch
40h	32	MCAN_CORE_ECR	2070 1040h	2071 1040h
44h	32	MCAN_CORE_PSR	2070 1044h	2071 1044h
48h	32	MCAN_CORE_TDCR	2070 1048h	2071 1048h
4Ch	32	MCAN_CORE_RESERVED44	2070 104Ch	2071 104Ch
50h	32	MCAN_CORE_IR	2070 1050h	2071 1050h
54h	32	MCAN_CORE_IE	2070 1054h	2071 1054h
58h	32	MCAN_CORE_ILS	2070 1058h	2071 1058h

Table 14-24437. MCAN_CORE Registers, Base Address=2070 1000h, Length=512 (continued)

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address
5Ch	32	MCAN_CORE_ILE	2070 105Ch	2071 105Ch
60h	32	MCAN_CORE_RESERVED55	2070 1060h	2071 1060h
64h	32	MCAN_CORE_RESERVED66	2070 1064h	2071 1064h
68h	32	MCAN_CORE_RESERVED77	2070 1068h	2071 1068h
6Ch	32	MCAN_CORE_RESERVED88	2070 106Ch	2071 106Ch
70h	32	MCAN_CORE_RESERVED99	2070 1070h	2071 1070h
74h	32	MCAN_CORE_RESERVED1010	2070 1074h	2071 1074h
78h	32	MCAN_CORE_RESERVED1111	2070 1078h	2071 1078h
7Ch	32	MCAN_CORE_RESERVED1212	2070 107Ch	2071 107Ch
80h	32	MCAN_CORE_GFC	2070 1080h	2071 1080h
84h	32	MCAN_CORE_SIDFC	2070 1084h	2071 1084h
88h	32	MCAN_CORE_XIDFC	2070 1088h	2071 1088h
8Ch	32	MCAN_CORE_RESERVED1313	2070 108Ch	2071 108Ch
90h	32	MCAN_CORE_XIDAM	2070 1090h	2071 1090h
94h	32	MCAN_CORE_HPMS	2070 1094h	2071 1094h
98h	32	MCAN_CORE_NDAT1	2070 1098h	2071 1098h
9Ch	32	MCAN_CORE_NDAT2	2070 109Ch	2071 109Ch
A0h	32	MCAN_CORE_RXF0C	2070 10A0h	2071 10A0h
A4h	32	MCAN_CORE_RXF0S	2070 10A4h	2071 10A4h
A8h	32	MCAN_CORE_RXF0A	2070 10A8h	2071 10A8h
ACh	32	MCAN_CORE_RXBC	2070 10ACh	2071 10ACh
B0h	32	MCAN_CORE_RXF1C	2070 10B0h	2071 10B0h
B4h	32	MCAN_CORE_RXF1S	2070 10B4h	2071 10B4h
B8h	32	MCAN_CORE_RXF1A	2070 10B8h	2071 10B8h
BCh	32	MCAN_CORE_RXESC	2070 10BCh	2071 10BCh
C0h	32	MCAN_CORE_TXBC	2070 10C0h	2071 10C0h
C4h	32	MCAN_CORE_TXFQS	2070 10C4h	2071 10C4h
C8h	32	MCAN_CORE_TXESC	2070 10C8h	2071 10C8h
CCh	32	MCAN_CORE_TXBRP	2070 10CCh	2071 10CCh
D0h	32	MCAN_CORE_TXBAR	2070 10D0h	2071 10D0h
D4h	32	MCAN_CORE_TXBCR	2070 10D4h	2071 10D4h
D8h	32	MCAN_CORE_TXBTO	2070 10D8h	2071 10D8h
DCh	32	MCAN_CORE_TXBCF	2070 10DCh	2071 10DCh
E0h	32	MCAN_CORE_TXBTIE	2070 10E0h	2071 10E0h
E4h	32	MCAN_CORE_TXBCIE	2070 10E4h	2071 10E4h
E8h	32	MCAN_CORE_RESERVED1414	2070 10E8h	2071 10E8h
ECh	32	MCAN_CORE_RESERVED1515	2070 10ECh	2071 10ECh
F0h	32	MCAN_CORE_TXEFC	2070 10F0h	2071 10F0h
F4h	32	MCAN_CORE_TXEFS	2070 10F4h	2071 10F4h
F8h	32	MCAN_CORE_TXEFA	2070 10F8h	2071 10F8h
FCh	32	MCAN_CORE_RESERVED1616	2070 10FCh	2071 10FCh
100h	32	MCAN_CORE_RESERVUPPER256_J	2070 1100h + formula	2071 1100h + formula

Table 14-24438. MCAN_MSGMEM_WRAP_MSGMEM_VBP_RAM Registers, Base Address=2070 8000h, Length=32768

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address
0h	32	MCAN_MSGMEM_WRAP_MSGMEM_VBP_RAM_RAM_REG_J	2070 8000h + formula	2071 8000h + formula

Table 14-24439. ECC_AGGR Registers, Base Address=2401 8000h, Length=1024

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address
0h	32	ECC_AGGR_REV	2401 8000h	2401 9000h
8h	32	ECC_AGGR_VECTOR	2401 8008h	2401 9008h
Ch	32	ECC_AGGR_STAT	2401 800Ch	2401 900Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	2401 8010h + formula	2401 9010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	2401 803Ch	2401 903Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	2401 8040h	2401 9040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	2401 8080h	2401 9080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	2401 80C0h	2401 90C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	2401 813Ch	2401 913Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	2401 8140h	2401 9140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	2401 8180h	2401 9180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	2401 81C0h	2401 91C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	2401 8200h	2401 9200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	2401 8204h	2401 9204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	2401 8208h	2401 9208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	2401 820Ch	2401 920Ch

14.9.4.1.2 MCAN Registers

MCAN Registers

14.9.4.1.2.1 MCAN_PID Register

1 MCAN_PID Register (Offset = 0h) [reset = 68E05101h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-24440. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0000h**
MCAN1	**2071 0000h**

Figure 14-8066. MCAN_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		8E0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
8E0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Ah					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-24442. MCAN_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: hsrst_n
29:28	BU	R	2h	Business Unit Reset Source: hsrst_n `2h Processors`
27:16	MODULE_ID	R	8E0h	Module ID Reset Source: hsrst_n
15:11	RTL	R	Ah	RTL Revision Reset Source: hsrst_n
10:8	MAJOR	R	1h	Major Revision Reset Source: hsrst_n
7:6	CUSTOM	R	0h	Custom Reset Source: hsrst_n
5:0	MINOR	R	1h	Minor Revision Reset Source: hsrst_n

14.9.4.1.2.2 MCAN_CTRL Register

1 MCAN_CTRL Register (Offset = 4h) [reset = 8h]

The Control Register contains general control bits for the MCANSS

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Table 14-24443. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0004h**
MCAN1	**2071 0004h**

Figure 14-8067. MCAN_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREQEN	DBGSUSP_FREE	RESERVED		
NONE	R/W	R/W	R/W	R/W	NONE		
0h	0h	0h	0h	1h	0h		

Table 14-24445. MCAN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	EXT_TS_CNTR_EN	R/W	0h	External Timestamp Counter Enable Reset Source: hsrst_n
5	AUTOWAKEUP	R/W	0h	Automatic Wakeup Enable Reset Source: hsrst_n
4	WAKEUPREQEN	R/W	0h	Wakeup Request Enable Reset Source: hsrst_n
3	DBGSUSP_FREE	R/W	1h	Debug Suspend Reset Source: hsrst_n 0h Honor debug suspend 1h Disregard debug suspend
2:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.3 MCAN_STAT Register

1 MCAN_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the MCANSS

Return to Summary Table

Table 14-24446. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0008h**
MCAN1	**2071 0008h**

Figure 14-8068. MCAN_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_FDOE	MEM_INIT_DONE	RESERVED
NONE					R	R	NONE
0h					X	0h	0h

Table 14-24448. MCAN_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_FDOE	R	X	Enable FD (Flexible Data-Rate) Configuration Reflects the value of mcanss_enable_fdoe configuration port, Reset Source: hsrst_n `xh      mcanss_enable_fdoe.`

1	MEM_INIT_DONE	R	0h	Memory Initialization
				Reset Source: hsrst_n
				`0h      Memory initialization is in progress`
				`1h      Memory intialization done`

0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.4 MCAN_ICS Register

1 MCAN_ICS Register (Offset = Ch) [reset = 0h]

Write to clear interrupt bits

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Table 14-24449. Instance Table

Instance Name	Physical Address
MCAN0	**2070 000Ch**
MCAN1	**2071 000Ch**

Figure 14-8069. MCAN_ICS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EXT_TS_CNTR_OVFL
NONE							W
0h							0h

Table 14-24451. MCAN_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	W	0h	External Timestamp Counter Overflow Interrupt Status Write 1h to clear bits. Reset Source: hsrst_n

14.9.4.1.2.5 MCAN_IRS Register

1 MCAN_IRS Register (Offset = 10h) [reset = 0h]

Read raw interrupt status. Write '1' to set interrupt bits.

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Table 14-24452. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0010h**
MCAN1	**2071 0010h**

Figure 14-8070. MCAN_IRS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							R/W1TS
0h							0h

Table 14-24454. MCAN_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R/W1TS	0h	External Timestamp Counter Overflow Interrupt Status Write 1h to set bits. Reset Source: hsrst_n

14.9.4.1.2.6 MCAN_IECS Register

1 MCAN_IECS Register (Offset = 14h) [reset = 0h]

Write to clear interrupt enable bits

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Table 14-24455. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0014h**
MCAN1	**2071 0014h**

Figure 14-8071. MCAN_IECS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							W1TC
0h							0h

Table 14-24457. MCAN_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	W1TC	0h	External Timestamp Counter Overflow Interrupt Write 1h to clear bits. Reset Source: hsrst_n

14.9.4.1.2.7 MCAN_IE Register

1 MCAN_IE Register (Offset = 18h) [reset = 0h]

Read interrupt Enable

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Table 14-24458. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0018h**
MCAN1	**2071 0018h**

Figure 14-8072. MCAN_IE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							R/W1TS
0h							0h

Table 14-24460. MCAN_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R/W1TS	0h	External Timestamp Counter Overflow Interrupt Write 1h to set bits. Reset Source: hsrst_n

14.9.4.1.2.8 MCAN_IES Register

1 MCAN_IES Register (Offset = 1Ch) [reset = 0h]

Read Enabled Interrupts

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Table 14-24461. Instance Table

Instance Name	Physical Address
MCAN0	**2070 001Ch**
MCAN1	**2071 001Ch**

Figure 14-8073. MCAN_IES Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EXT_TS_CNTR_OVFL</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-24463. MCAN_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R	0h	External Timestamp Counter Overflow Interrupt Reset Source: hsrst_n

14.9.4.1.2.9 MCAN_EOI Register

1 MCAN_EOI Register (Offset = 20h) [reset = 0h]

End of Interrupt Register

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Table 14-24464. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0020h**
MCAN1	**2071 0020h**

Figure 14-8074. MCAN_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI							
W							
0h							

Table 14-24466. MCAN_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved

7:0	EOI	W	0h	End Of Interrupt Write with bit position of the targeted interrupt (example: external timestamp is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1h will issue another pulse interrupt.
				Reset Source: hsrst_n
				`0h EOI value for external timestamp interrupt`
				`1h EOI value for mcan[0] interrupt`
				`2h EOI value for mcan[1] interrupt`

14.9.4.1.2.10 MCAN_EXT_TS_PRESCALER Register

1 MCAN_EXT_TS_PRESCALER Register (Offset = 24h) [reset = 0h]

External TImeStamp PreScaler

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Table 14-24467. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0024h**
MCAN1	**2071 0024h**

Figure 14-8075. MCAN_EXT_TS_PRESCALER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRESCALER							
R/W							
0h							
15	14	13	12	11	10	9	8
PRESCALER							
R/W							
0h							
7	6	5	4	3	2	1	0
PRESCALER							
R/W							
0h							

Table 14-24469. MCAN_EXT_TS_PRESCALER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PRESCALER	R/W	0h	External Timestamp Prescaler Reload Value External timestamp count rate is host clock rate divided by this value with one exception - a value of 0h has the same effect as 1h. Reset Source: hsrst_n

14.9.4.1.2.11 MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register

1 MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register (Offset = 28h) [reset = 0h]

External TImeStamp Unserviced Interrupts Counter

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Table 14-24470. Instance Table

Instance Name	Physical Address
MCAN0	**2070 0028h**
MCAN1	**2071 0028h**

Figure 14-8076. MCAN_EXT_TS_UNSERVICED_INTR_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EXT_TS_INTR_CNTR				
NONE			R				
0h			0h				

Table 14-24472. MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EXT_TS_INTR_CNTR	R	0h	Number of Unserviced Rollover Interrupts If > 1h an EOI write will issue another pulse interrupt. Reset Source: hsrst_n

14.9.4.1.2.12 MCAN_CORE_CREL Register

1 MCAN_CORE_CREL Register (Offset = 0h) [reset = 32380608h]

Release dependent constant (version + date)

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Table 14-24473. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1000h**
MCAN1	**2071 1000h**

Figure 14-8077. MCAN_CORE_CREL Name Register

31	30	29	28	27	26	25	24
REL				STEP			
R				R			
3h				2h			
23	22	21	20	19	18	17	16
SUBSTEP				YEAR			
R				R			
3h				8h			
15	14	13	12	11	10	9	8
MON							
R							
6h							
7	6	5	4	3	2	1	0
DAY							
R							
8h							

Table 14-24475. MCAN_CORE_CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REL	R	3h	Core Release One digit, BCD-coded. Reset Source: hsrst_n
27:24	STEP	R	2h	Step of Core Release One digit, BCD-coded. Reset Source: hsrst_n
23:20	SUBSTEP	R	3h	Sub-step of Core Release One digit, BCD-coded. Reset Source: hsrst_n
19:16	YEAR	R	8h	Time Stamp Year One digit, BCD-coded. Reset Source: hsrst_n
15:8	MON	R	6h	Time Stamp Month Two digits, BCD-coded. Reset Source: hsrst_n
7:0	DAY	R	8h	Time Stamp Day Two digits, BCD-coded. Reset Source: hsrst_n

14.9.4.1.2.13 MCAN_CORE_ENDN Register

1 MCAN_CORE_ENDN Register (Offset = 4h) [reset = 87654321h]

Constant "0x8765 4321"

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Table 14-24476. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1004h**
MCAN1	**2071 1004h**

Figure 14-8078. MCAN_CORE_ENDN Name Register

31	30	29	28	27	26	25	24
ETV							
R							
87654321h							
23	22	21	20	19	18	17	16
ETV							
R							
87654321h							
15	14	13	12	11	10	9	8
ETV							
R							
87654321h							
7	6	5	4	3	2	1	0
ETV							
R							
87654321h							

Table 14-24478. MCAN_CORE_ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ETV	R	87654321h	Endianness Test Value The endianness test value is 8765 4321h. Reset Source: hsrst_n

14.9.4.1.2.14 MCAN_CORE_CUST Register

1 MCAN_CORE_CUST Register (Offset = 8h) [reset = 0h]

Optional customer-specific register

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Table 14-24479. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1008h**
MCAN1	**2071 1008h**

Figure 14-8079. MCAN_CORE_CUST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24481. MCAN_CORE_CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.15 MCAN_CORE_DBTP Register

1 MCAN_CORE_DBTP Register (Offset = Ch) [reset = A33h]

Configuration of data phase bit timing, transmitter delay compensation enable

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Table 14-24482. Instance Table

Instance Name	Physical Address
MCAN0	**2070 100Ch**
MCAN1	**2071 100Ch**

Figure 14-8080. MCAN_CORE_DBTP Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TDC	RESERVED		DBRP				
R/W	NONE		R/W				
0h	0h		0h				
15	14	13	12	11	10	9	8
RESERVED			DTSEG1				
NONE			R/W				
0h			Ah				
7	6	5	4	3	2	1	0
DTSEG2				DSJW			
R/W				R/W			
3h				3h			

Table 14-24484. MCAN_CORE_DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

23	TDC	R/W	0h	Transmitter Delay Compensation
				Reset Source: hsrst_n
				`0h     Transmitter Delay Compensation disabled`
				`1h     Transmitter Delay Compensation enabled`

22:21	RESERVED	NONE	0h	Reserved
20:16	DBRP	R/W	0h	Data Baud Rate Prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 31 (0h-1Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Reset Source: hsrst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	DTSEG1	R/W	Ah	Data time segment before sample point Valid values are 0 to 31 (0h-1Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Reset Source: hsrst_n

Table 14-24484. MCAN_CORE_DBTP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	DTSEG2	R/W	3h	Data time segment after sample point Valid values are 0 to 15 (0h-Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Reset Source: hsrst_n
3:0	DSJW	R/W	3h	Data (Re)Synchronization Jump Width Valid values are 0 to 15 (0h-Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Reset Source: hsrst_n

14.9.4.1.2.16 MCAN_CORE_TEST Register

1 MCAN_CORE_TEST Register (Offset = 10h) [reset = 0h]

Test mode selection

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Table 14-24485. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1010h**
MCAN1	**2071 1010h**

Figure 14-8081. MCAN_CORE_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX	TX		LBCK	RESERVED			
R	R/W		R/W	NONE			
0h	0h		0h	0h			

Table 14-24487. MCAN_CORE_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RX	R	0h	Receive Pin Monitors the actual value of the MCAN RX pin Reset Source: hsrst_n 0h The CAN bus is dominant (MCAN RX = 0h) 1h The CAN bus is recessive (MCAN RX = 1h)
6:5	TX	R/W	0h	Control of Transmit Pin Reset Source: hsrst_n 0h Reset value, the MCAN TX pin controlled by the CAN Core, updated at the end of the CAN bit time 1h Sample Point can be monitored at the MCAN TX pin 2h Dominant (0) level at the MCAN TX pin 3h Recessive (1) at the MCAN TX pin
4	LBCK	R/W	0h	Loopback Mode Reset Source: hsrst_n 0h Reset value, Loopback Mode is disabled 1h Loopback Mode is enabled (see Test Modes)

Table 14-24487. MCAN_CORE_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.17 MCAN_CORE_RWD Register

1 MCAN_CORE_RWD Register (Offset = 14h) [reset = 0h]

Monitors the READY output of the Message RAM

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Table 14-24488. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1014h**
MCAN1	**2071 1014h**

Figure 14-8082. MCAN_CORE_RWD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WDV							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WDC							
R/W							
0h							

Table 14-24490. MCAN_CORE_RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	WDV	R	0h	Watchdog Value Actual Message RAM Watchdog Counter Value. Reset Source: hsrst_n
7:0	WDC	R/W	0h	Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of 0h the counter is disabled. Reset Source: hsrst_n

14.9.4.1.2.18 MCAN_CORE_CCCR Register

1 MCAN_CORE_CCCR Register (Offset = 18h) [reset = 1h]

Operation mode configuration

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Table 14-24491. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1018h**
MCAN1	**2071 1018h**

Figure 14-8083. MCAN_CORE_CCCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
NISO	TXP	EFBI	PXHD	RESERVED		BRSE	FDOE
R/W	R/W	R/W	R/W	NONE		R/W	R/W
0h	0h	0h	0h	0h		0h	0h
7	6	5	4	3	2	1	0
TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h

Table 14-24493. MCAN_CORE_CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	NISO	R/W	0h	Non ISO Operation Reset Source: hsrst_n 0h CAN FD frame format according to ISO 11898-1:2015. 1h CAN FD frame format according to Bosch CAN FD Specification 1.0.
14	TXP	R/W	0h	Transmit Pause If this bit is set, the MCAN module pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Tx Handling) . Reset Source: hsrst_n 0h Transmit pause disabled 1h Transmit pause enabled
13	EFBI	R/W	0h	Edge Filtering during Bus Integration Reset Source: hsrst_n 0h Edge filtering disabled 1h Two consecutive dominant tq required to detect an edge for hard synchronization

Table 14-24493. MCAN_CORE_CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PXHD	R/W	0h	Protocol Exception Handling Disable Note: When protocol exception handling is disabled, the MCAN module will transmit an error frame when it detects a protocol exception condition. Reset Source: hsrst_n 0h Protocol exception handling enabled 1h Protocol exception handling disabled
11:10	RESERVED	NONE	0h	Reserved
9	BRSE	R/W	0h	Bit Rate Switch Enable Note: When CAN FD operation is disabled the MCAN_CCCR[8] FDOE = 0h Reset Source: hsrst_n 0h Bit rate switching for transmissions disabled 1h Bit rate switching for transmissions enabled
8	FDOE	R/W	0h	FD Operation Enable Reset Source: hsrst_n 0h FD operation disabled 1h FD operation enabled
7	TEST	R/W	0h	Test Mode Enable Reset Source: hsrst_n 0h Normal operation. The MCAN_TEST register holds reset values. 1h Test Mode. Write access to the MCAN_TEST register enabled.
6	DAR	R/W	0h	Disable Automatic Retransmission Reset Source: hsrst_n 0h Automatic retransmission of messages not transmitted successfully enabled 1h Automatic retransmission disabled
5	MON	R/W	0h	Bus Monitoring Mode The MCAN_CCCR[5] MON bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time. Reset Source: hsrst_n 0h Bus Monitoring Mode is disabled 1h Bus Monitoring Mode is enabled
4	CSR	R/W	0h	Clock Stop Request Reset Source: hsrst_n 0h No clock stop is requested 1h Clock stop requested. When clock stop is requested, first the MCAN_CCCR[0] INIT bit and then the MCAN_CCCR[3] CSA bit will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	CSA	R	0h	Clock Stop Acknowledge Reset Source: hsrst_n 0h No clock stop acknowledged 1h The MCAN module may be set in power down by stopping MCAN interface clock and MCAN functional clock

Table 14-24493. MCAN_CORE_CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2	ASM	R/W	0h	Restricted Operation Mode
				The MCAN_CCCR[2] ASM bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time.
				For a description of the Restricted Operation Mode, see Restricted Operation Mode.
				Reset Source: hsrst_n
				`0h` `Normal CAN operation`
				`1h` `Restricted Operation Mode active`

1	CCE	R/W	0h	Configuration Change Enable
				Reset Source: hsrst_n
				`0h` `The Host CPU has no write access to the protected configuration registers`
				`1h` `The Host CPU has write access to the protected configuration registers (while the MCAN_CCCR[0] INIT = 1h)`

0	INIT	R/W	1h	Initialization
				Note: Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to the MCAN_CCCR[0] INIT bit can be read back. Therefore the software has to assure that the previous value written to the MCAN_CCCR[0] INIT bit has been accepted by Reading the MCAN_CCCR[0] INIT bit before setting the MCAN_CCCR[0] INIT bit to a new value.
				Reset Source: hsrst_n
				`0h` `Normal Operation`
				`1h` `Initialization is started`

14.9.4.1.2.19 MCAN_CORE_NBTP Register

1 MCAN_CORE_NBTP Register (Offset = 1Ch) [reset = 6000A03h]

Configuration of arbitration phase bit timing

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Table 14-24494. Instance Table

Instance Name	Physical Address
MCAN0	**2070 101Ch**
MCAN1	**2071 101Ch**

Figure 14-8084. MCAN_CORE_NBTP Name Register

31	30	29	28	27	26	25	24
NSJW							NBRP
R/W							R/W
3h							0h
23	22	21	20	19	18	17	16
NBRP							
R/W							
0h							
15	14	13	12	11	10	9	8
NTSEG1							
R/W							
Ah							
7	6	5	4	3	2	1	0
RESERVED	NTSEG2						
NONE	R/W						
0h	3h						

Table 14-24496. MCAN_CORE_NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	NSJW	R/W	3h	Nominal (Re)Synchronization Jump Width Valid values are 0 to 127 (0h-7Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Reset Source: hsrst_n
24:16	NBRP	R/W	0h	Nominal Baud Rate Prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 511 (0h-1FFh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Reset Source: hsrst_n
15:8	NTSEG1	R/W	Ah	Nominal Time segment before sample point Valid values are 1 to 255 (1h-FFh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Reset Source: hsrst_n
7	RESERVED	NONE	0h	Reserved

Table 14-24496. MCAN_CORE_NBTP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	NTSEG2	R/W	3h	Nominal Time segment after sample point Valid values are 0 to 127 (0h-7Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Note: With a CAN clock (MCAN functional clock) of 8 MHz, the reset value of 0600 0A03h configures the MCAN module for a bit rate of 500 kbit/s. Reset Source: hsrst_n

14.9.4.1.2.20 MCAN_CORE_TSCC Register

1 MCAN_CORE_TSCC Register (Offset = 20h) [reset = 0h]

Timestamp counter prescaler setting, selection of internal/external timestamp vector

Return to Summary Table

Table 14-24497. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1020h**
MCAN1	**2071 1020h**

Figure 14-8085. MCAN_CORE_TSCC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				TCP			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TSS	
NONE						R/W	
0h						0h	

Table 14-24499. MCAN_CORE_TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	TCP	R/W	0h	Timestamp Counter Prescaler Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1-16 (0h-Fh)]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: With CAN FD an external counter is required for timestamp generation (MCAN_TSCC[1-0] TSS = 2h) Reset Source: hsrst_n
15:2	RESERVED	NONE	0h	Reserved

1:0	TSS	R/W	0h	Timestamp Select
				Reset Source: hsrst_n
				`0h` `Timestamp counter value always 0h`
				`1h` `Timestamp counter value incremented according to the MCAN_TSCC[19-16] TCP field`
				`2h` `External timestamp counter value used`
				`3h` `Same as 0h`

14.9.4.1.2.21 MCAN_CORE_TSCV Register

1 MCAN_CORE_TSCV Register (Offset = 24h) [reset = 0h]

Read/reset timestamp counter

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Table 14-24500. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1024h**
MCAN1	**2071 1024h**

Figure 14-8086. MCAN_CORE_TSCV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TSC							
R/WTC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSC							
R/WTC							
0h							

Table 14-24502. MCAN_CORE_TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TSC	R/WTC	0h	Timestamp Counter The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When the MCAN_TSCC[1-0] TSS = 1h, the Timestamp Counter is incremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. A wrap around sets interrupt flag MCAN_IR[16] TSW. Write access resets the counter to zero. When the MCAN_TSCC[1-0] TSS = 2h, the MCAN_TSCV[15-0] TSC field reflects the external Timestamp Counter value. A write access has no impact. Note: A 'wrap around' is a change of the Timestamp Counter value from non-zero to zero not caused by write access to the MCAN_TSCV register. Reset Source: hsrst_n

14.9.4.1.2.22 MCAN_CORE_TOCC Register

1 MCAN_CORE_TOCC Register (Offset = 28h) [reset = FFFF0000h]

Configuration of timeout period, selection of timeout counter operation mode

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Table 14-24503. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1028h**
MCAN1	**2071 1028h**

Figure 14-8087. MCAN_CORE_TOCC Name Register

31	30	29	28	27	26	25	24
TOP							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
TOP							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TOS		ETOC
NONE					R/W		R/W
0h					0h		0h

Table 14-24505. MCAN_CORE_TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TOP	R/W	FFFFh	Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Reset Source: hsrst_n
15:3	RESERVED	NONE	0h	Reserved

2:1	TOS	R/W	0h	Timeout Select
				When operating in Continuous mode, a write to the MCAN_TOCV[15-0] TOC field presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field. Down-counting is started when the first FIFO element is stored.
				Reset Source: hsrst_n
				`0h Continuous operation`
				`1h Timeout controlled by Tx Event FIFO`
				`2h Timeout controlled by Rx FIFO 0`
				`3h Timeout controlled by Rx FIFO 1`

Table 14-24505. MCAN_CORE_TOCC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

0	ETOC	R/W	0h	Enable Timeout Counter
				Reset Source: hsrst_n
				`0h Timeout Counter disabled`
				`1h Timeout Counter enabled`

14.9.4.1.2.23 MCAN_CORE_TOCV Register

1 MCAN_CORE_TOCV Register (Offset = 2Ch) [reset = FFFFh]

Read/reset timeout counter

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Table 14-24506. Instance Table

Instance Name	Physical Address
MCAN0	**2070 102Ch**
MCAN1	**2071 102Ch**

Figure 14-8088. MCAN_CORE_TOCV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOC							
R/WTC							
FFFFh							
7	6	5	4	3	2	1	0
TOC							
R/WTC							
FFFFh							

Table 14-24508. MCAN_CORE_TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TOC	R/WTC	FFFFh	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. When decremented to zero, interrupt flag MCAN_IR[18] TOO is set and the Timeout Counter is stopped. Start and reset/ restart conditions are configured via the MCAN_TOCC[2-1] TOS field. Reset Source: hsrst_n

14.9.4.1.2.24 MCAN_CORE_RESERVED00 Register

1 MCAN_CORE_RESERVED00 Register (Offset = 30h) [reset = 0h]

Reserved field

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Table 14-24509. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1030h**
MCAN1	**2071 1030h**

Figure 14-8089. MCAN_CORE_RESERVED00 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24511. MCAN_CORE_RESERVED00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.25 MCAN_CORE_RESERVED11 Register

1 MCAN_CORE_RESERVED11 Register (Offset = 34h) [reset = 0h]

Reserved field

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Table 14-24512. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1034h**
MCAN1	**2071 1034h**

Figure 14-8090. MCAN_CORE_RESERVED11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24514. MCAN_CORE_RESERVED11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.26 MCAN_CORE_RESERVED22 Register

1 MCAN_CORE_RESERVED22 Register (Offset = 38h) [reset = 0h]

Reserved field

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Table 14-24515. Instance Table

Instance Name	**Physical Address**
MCAN0	**2070 1038h**
MCAN1	**2071 1038h**

Figure 14-8091. MCAN_CORE_RESERVED22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24517. MCAN_CORE_RESERVED22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.27 MCAN_CORE_RESERVED33 Register

1 MCAN_CORE_RESERVED33 Register (Offset = 3Ch) [reset = 0h]

Reserved field

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Table 14-24518. Instance Table

Instance Name	Physical Address
MCAN0	**2070 103Ch**
MCAN1	**2071 103Ch**

Figure 14-8092. MCAN_CORE_RESERVED33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24520. MCAN_CORE_RESERVED33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.28 MCAN_CORE_ECR Register

1 MCAN_CORE_ECR Register (Offset = 40h) [reset = 0h]

State of Rx/Tx Error Counter, CAN Error Logging

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Table 14-24521. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1040h**
MCAN1	**2071 1040h**

Figure 14-8093. MCAN_CORE_ECR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CEL							
R							
0h							
15	14	13	12	11	10	9	8
RP	REC						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
TEC							
R							
0h							

Table 14-24523. MCAN_CORE_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	CEL	R	0h	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to the MCAN_ECR[23-16] CEL field. The counter stops at FFh; the next increment of the MCAN_ECR[7-0] TEC or MCAN_ECR[14-8] REC fields sets interrupt flag MCAN_IR[22] ELO. Reset Source: hsrst_n

15	RP	R	0h	Receive Error Passive
				Reset Source: hsrst_n
				`0h The Receive Error Counter is below the error passive level of 128`
				`1h The Receive Error Counter has reached the error passive level of 128`

14:8	REC	R	0h	Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127. Reset Source: hsrst_n

Table 14-24523. MCAN_CORE_ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	TEC	R	0h	Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255. Note: When the MCAN_CCCR[2] ASM bit is set, the CAN protocol controller does not increment the MCAN_ECR[7-0] TEC and MCAN_ECR[14-8] REC fields when a CAN protocol error is detected, but the MCAN_ECR[23-16] CEL field is still incremented. Reset Source: hsrst_n

14.9.4.1.2.29 MCAN_CORE_PSR Register

1 MCAN_CORE_PSR Register (Offset = 44h) [reset = 707h]

CAN protocol controller status, transmitter delay compensation value

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Table 14-24524. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1044h**
MCAN1	**2071 1044h**

Figure 14-8094. MCAN_CORE_PSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	TDCV						
NONE	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PXE	RFDF	RBRS	RESI	DLEC		
NONE	R	R	R	R	R		
0h	0h	0h	0h	0h	7h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BO	EW	EP	ACT		LEC		
R	R	R	R		R		
0h	0h	0h	0h		7h		

Table 14-24526. MCAN_CORE_PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	TDCV	R	0h	Transmitter Delay Compensation Value Position of the secondary sample point, defined by the sum of the measured delay from the MCAN TX to MCAN RX pins and the MCAN_TDCR[14-8] TDCO field. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq (0h-7Fh). Reset Source: hsrst_n
15	RESERVED	NONE	0h	Reserved
14	PXE	R	0h	Protocol Exception Event Reset Source: hsrst_n 0h No protocol exception event occurred since last read access 1h Protocol exception event occurred

Table 14-24526. MCAN_CORE_PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RFDF	R	0h	Received a CAN FD Message This bit is set independent of acceptance filtering. Reset Source: hsrst_n 0h Since this bit was reset by the Host CPU, no CAN FD message has been received 1h Message in CAN FD format with FDF flag set has been received
12	RBRS	R	0h	BRS flag of last received CAN FD Message This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering. Reset Source: hsrst_n 0h Last received CAN FD message did not have its BRS flag set 1h Last received CAN FD message had its BRS flag set
11	RESI	R	0h	ESI flag of last received CAN FD Message This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering. Reset Source: hsrst_n 0h Last received CAN FD message did not have its ESI flag set 1h Last received CAN FD message had its ESI flag set
10:8	DLEC	R	7h	Data Phase Last Error Code Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for the MCAN_PSR[2-0] LEC field. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. Reset Source: hsrst_n
7	BO	R	0h	Bus_Off Status Reset Source: hsrst_n 0h The MCAN module is not Bus_Off 1h The MCAN module is in Bus_Off state
6	EW	R	0h	Warning Status Reset Source: hsrst_n 0h Both error counters are below the Error_Warning limit of 96 1h At least one of error counter has reached the Error_Warning limit of 96
5	EP	R	0h	Error Passive Reset Source: hsrst_n 0h The MCAN module is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1h The MCAN module is in the Error_Passive state

Table 14-24526. MCAN_CORE_PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	ACT	R	0h	Activity Monitors the module's CAN communication state. Note: ACT is set to 0h by a Protocol Exception Event. Reset Source: hsrst_n 0h Synchronizing - node is synchronizing on CAN communication 1h Idle - node is neither receiver nor transmitter 2h Receiver - node is operating as receiver 3h Transmitter - node is operating as transmitter
2:0	LEC	R	7h	Last Error Code The MCAN_PSR[2-0] LEC field indicates the type of the last error to occur on the CAN bus. This field will be cleared to 0h when a message has been transferred (reception or transmission) without error. Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in the MCAN_PSR[10-8] DLEC field instead of the MCAN_PSR[2-0] LEC field. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error. Reset Source: hsrst_n 0h No Error: No error occurred since the MCAN_PSR[2-0] LEC field has been reset by successful reception or transmission. 1h Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2h Form Error: A fixed format part of a received frame has the wrong format. 3h AckError: The message transmitted by the MCAN module was not acknowledged by another node. 4h Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value 1), but the monitored bus value was dominant. 5h Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the Host CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6h CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7h NoChange: Any read access to the Protocol Status Register re-initializes the MCAN_PSR[2-0] LEC field to 7h. When the MCAN_PSR[2-0] LEC field shows the value 7h, no CAN bus event was detected since the last Host CPU read access to the Protocol Status Register.

14.9.4.1.2.30 MCAN_CORE_TDCR Register

1 MCAN_CORE_TDCR Register (Offset = 48h) [reset = 0h]

configuration of transmitter delay compensation offset and filter window length

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Table 14-24527. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1048h**
MCAN1	**2071 1048h**

Figure 14-8095. MCAN_CORE_TDCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	TDCO						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED	TDCF						
NONE	R/W						
0h	0h						

Table 14-24529. MCAN_CORE_TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:8	TDCO	R/W	0h	Transmitter Delay Compensation Offset Offset value defining the distance between the measured delay from the MCAN RX and MCAN TX pins and the secondary sample point. Valid values are 0 to 127 mtq (0h-7Fh). Reset Source: hsrst_n
7	RESERVED	NONE	0h	Reserved
6:0	TDCF	R/W	0h	Transmitter Delay Compensation Filter Window Length Defines the minimum value for the SSP position, dominant edges on the MCAN RX pin that would result in an earlier SSP position are ignored for transmitter delay measure-ment. The feature is enabled when the MCAN_TDCR[6-0] TDCF field is configured to a value greater than the MCAN_TDCR[14-8] TDCO field. Valid values are 0 to 127 mtq (0h-7Fh). Reset Source: hsrst_n

14.9.4.1.2.31 MCAN_CORE_RESERVED44 Register

1 MCAN_CORE_RESERVED44 Register (Offset = 4Ch) [reset = 0h]

Reserved field

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Table 14-24530. Instance Table

Instance Name	Physical Address
MCAN0	**2070 104Ch**
MCAN1	**2071 104Ch**

Figure 14-8096. MCAN_CORE_RESERVED44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24532. MCAN_CORE_RESERVED44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.32 MCAN_CORE_IR Register

1 MCAN_CORE_IR Register (Offset = 50h) [reset = 0h]

Interrupt flags

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Table 14-24533. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1050h**
MCAN1	**2071 1050h**

Figure 14-8097. MCAN_CORE_IR Name Register

31	30	29	28	27	26	25	24
RESERVED		ARA	PED	PEA	WDI	BO	EW
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EP	ELO	BEU	RESERVED	DRX	TOO	MRAF	TSW
R/W1TC	R/W1TC	R/W1TC	NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24535. MCAN_CORE_IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved

29	ARA	R/W1TC	0h	Access to Reserved Address
				Reset Source: hsrst_n
				`0h No access to reserved address occurred`
				`1h Access to reserved address occurred`

28	PED	R/W1TC	0h	Protocol Error in Data Phase
				Reset Source: hsrst_n
				`0h No protocol error in data phase`
				`1h Protocol error in data phase detected (MCAN_PSR[10-8] DLEC != 0.7)`

27	PEA	R/W1TC	0h	Protocol Error in Arbitration Phase
				Reset Source: hsrst_n
				`0h No protocol error in arbitration phase`
				`1h Protocol error in arbitration phase detected (MCAN_PSR[2-0] LEC != 0.7)`

Table 14-24535. MCAN_CORE_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	WDI	R/W1TC	0h	Watchdog Interrupt Reset Source: hsrst_n 0h No Message RAM Watchdog event occurred 1h Message RAM Watchdog event due to missing READY
25	BO	R/W1TC	0h	Bus_Off Status Reset Source: hsrst_n 0h Bus_Off status unchanged 1h Bus_Off status changed
24	EW	R/W1TC	0h	Warning Status Reset Source: hsrst_n 0h Error_Warning status unchanged 1h Error_Warning status changed
23	EP	R/W1TC	0h	Error Passive Reset Source: hsrst_n 0h Error_Passive status unchanged 1h Error_Passive status changed
22	ELO	R/W1TC	0h	Error Logging Overflow Reset Source: hsrst_n 0h CAN Error Logging Counter did not overflow 1h Overflow of CAN Error Logging Counter occurred
21	BEU	R/W1TC	0h	Bit Error Uncorrected Message RAM bit error detected, uncorrected. Controlled by input signal generated by parity/ECC logic attached to the Message RAM. An uncorrected Message RAM bit error sets the MCAN_CCCR[0] INIT bit to 1. This is done to avoid transmission of corrupted data. Reset Source: hsrst_n 0h No bit error detected when reading from Message RAM 1h Bit error detected, uncorrected (example: parity logic)
20	RESERVED	NONE	0h	Reserved
19	DRX	R/W1TC	0h	Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. Reset Source: hsrst_n 0h No Rx Buffer updated 1h At least one received message stored into an Rx Buffer
18	TOO	R/W1TC	0h	Timeout Occurred Reset Source: hsrst_n 0h No timeout 1h Timeout reached

Table 14-24535. MCAN_CORE_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	MRAF	R/W1TC	0h	Message RAM Access Failure The flag is set, when the Rx Handler: a) has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. b) was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated respectively the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the MCAN module is switched into Restricted Operation Mode (see Restricted Operation Mode). To leave Restricted Operation Mode, the Host CPU has to reset the MCAN_CCCR[2] ASM bit. Reset Source: hsrst_n 0h No Message RAM access failure occurred 1h Message RAM access failure occurred
16	TSW	R/W1TC	0h	Timestamp Wraparound Reset Source: hsrst_n 0h No timestamp counter wrap-around 1h Timestamp counter wrapped around
15	TEFL	R/W1TC	0h	Tx Event FIFO Element Lost Reset Source: hsrst_n 0h No Tx Event FIFO element lost 1h Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	TEFF	R/W1TC	0h	Tx Event FIFO Full Reset Source: hsrst_n 0h Tx Event FIFO not full 1h Tx Event FIFO full
13	TEFW	R/W1TC	0h	Tx Event FIFO Watermark Reached Reset Source: hsrst_n 0h Tx Event FIFO fill level below watermark 1h Tx Event FIFO fill level reached watermark
12	TEFN	R/W1TC	0h	Tx Event FIFO New Entry Reset Source: hsrst_n 0h Tx Event FIFO unchanged 1h Tx Handler wrote Tx Event FIFO element
11	TFE	R/W1TC	0h	Tx FIFO Empty Reset Source: hsrst_n 0h Tx FIFO non-empty 1h Tx FIFO empty
10	TCF	R/W1TC	0h	Transmission Cancellation Finished Reset Source: hsrst_n 0h No transmission cancellation finished 1h Transmission cancellation finished

Table 14-24535. MCAN_CORE_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	TC	R/W1TC	0h	Transmission Completed Reset Source: hsrst_n 0h No transmission completed 1h Transmission completed
8	HPM	R/W1TC	0h	High Priority Message Reset Source: hsrst_n 0h No high priority message received 1h High priority message received
7	RF1L	R/W1TC	0h	Rx FIFO 1 Message Lost Reset Source: hsrst_n 0h No Rx FIFO 1 message lost 1h Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	RF1F	R/W1TC	0h	Rx FIFO 1 Full Reset Source: hsrst_n 0h Rx FIFO 1 not full 1h Rx FIFO 1 full
5	RF1W	R/W1TC	0h	Rx FIFO 1 Watermark Reached Reset Source: hsrst_n 0h Rx FIFO 1 fill level below watermark 1h Rx FIFO 1 fill level reached watermark
4	RF1N	R/W1TC	0h	Rx FIFO 1 New Message Reset Source: hsrst_n 0h No new message written to Rx FIFO 1 1h New message written to Rx FIFO 1
3	RF0L	R/W1TC	0h	Rx FIFO 0 Message Lost Reset Source: hsrst_n 0h No Rx FIFO 0 message lost 1h Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	RF0F	R/W1TC	0h	Rx FIFO 0 Full Reset Source: hsrst_n 0h Rx FIFO 0 not full 1h Rx FIFO 0 full
1	RF0W	R/W1TC	0h	Rx FIFO 0 Watermark Reached Reset Source: hsrst_n 0h Rx FIFO 0 fill level below watermark 1h Rx FIFO 0 fill level reached watermark
0	RF0N	R/W1TC	0h	Rx FIFO 0 New Message Reset Source: hsrst_n 0h No new message written to Rx FIFO 0 1h New message written to Rx FIFO 0

14.9.4.1.2.33 MCAN_CORE_IE Register

1 MCAN_CORE_IE Register (Offset = 54h) [reset = 0h]

Interrupt enable/disable

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Table 14-24536. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1054h**
MCAN1	**2071 1054h**

Figure 14-8098. MCAN_CORE_IE Name Register

31	30	29	28	27	26	25	24
RESERVED		ARAE	PEDE	PEAE	WDIE	BOE	EWE
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24538. MCAN_CORE_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved

29	ARAE	R/W	0h	Access to Reserved Address Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

28	PEDE	R/W	0h	Protocol Error in Data Phase Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

27	PEAE	R/W	0h	Protocol Error in Arbitration Phase Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

26	WDIE	R/W	0h	Watchdog Interrupt Enable
				Reset Source: hsrst_n
				`0h Interrupt disabled`
				`1h Interrupt enabled`

Table 14-24538. MCAN_CORE_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	BOE	R/W	0h	Bus_Off Status Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
24	EWE	R/W	0h	Warning Status Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
23	EPE	R/W	0h	Error Passive Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
22	ELOE	R/W	0h	Error Logging Overflow Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
21	BEUE	R/W	0h	Bit Error Uncorrected Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
20	BECE	R/W	0h	Bit Error Corrected Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
19	DRX	R/W	0h	Message stored to Dedicated Rx Buffer Interrupt Enable Reset Source: hsrst_n
18	TOOE	R/W	0h	Timeout Occurred Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
17	MRAFE	R/W	0h	Message RAM Access Failure Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
16	TSWE	R/W	0h	Timestamp Wraparound Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
15	TEFLE	R/W	0h	Tx Event FIFO Event Lost Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
14	TEFFE	R/W	0h	Tx Event FIFO Full Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled

Table 14-24538. MCAN_CORE_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TEFWE	R/W	0h	Tx Event FIFO Watermark Reached Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
12	TEFNE	R/W	0h	Tx Event FIFO New Entry Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
11	TFEE	R/W	0h	Tx FIFO Empty Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
10	TCFE	R/W	0h	Transmission Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
9	TCE	R/W	0h	Transmission Completed Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
8	HPME	R/W	0h	High Priority Message Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
7	RF1LE	R/W	0h	Rx FIFO 1 Message Lost Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
6	RF1FE	R/W	0h	Rx FIFO 1 Full Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
5	RF1WE	R/W	0h	Rx FIFO 1 Watermark Reached Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
4	RF1NE	R/W	0h	Rx FIFO 1 New Message Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
3	RF0LE	R/W	0h	Rx FIFO 0 Message Lost Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled

Table 14-24538. MCAN_CORE_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RF0FE	R/W	0h	Rx FIFO 0 Full Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
1	RF0WE	R/W	0h	Rx FIFO 0 Watermark Reached Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled
0	RF0NE	R/W	0h	Rx FIFO 0 New Message Interrupt Enable Reset Source: hsrst_n 0h Interrupt disabled 1h Interrupt enabled

14.9.4.1.2.34 MCAN_CORE_ILS Register

1 MCAN_CORE_ILS Register (Offset = 58h) [reset = 0h]

Interrupt line select (m_can_int0 or m_can_int1)

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Table 14-24539. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1058h**
MCAN1	**2071 1058h**

Figure 14-8099. MCAN_CORE_ILS Name Register

31	30	29	28	27	26	25	24
RESERVED		ARAL	PEDL	PEAL	WDIL	BOL	EWL
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24541. MCAN_CORE_ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved

29	ARAL	R/W	0h	Access to Reserved Address Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

28	PEDL	R/W	0h	Protocol Error in Data Phase Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

27	PEAL	R/W	0h	Protocol Error in Arbitration Phase Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

26	WDIL	R/W	0h	Watchdog Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

Table 14-24541. MCAN_CORE_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

25	BOL	R/W	0h	Bus_Off Status Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

24	EWL	R/W	0h	Warning Status Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

23	EPL	R/W	0h	Error Passive Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

22	ELOL	R/W	0h	Error Logging Overflow Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

21	BEUL	R/W	0h	Bit Error Uncorrected Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

20	BECL	R/W	0h	Bit Error Corrected Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

19	DRXL	R/W	0h	Message stored to Dedicated Rx Buffer Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

18	TOOL	R/W	0h	Timeout Occurred Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

17	MRAFL	R/W	0h	Message RAM Access Failure Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

16	TSWL	R/W	0h	Timestamp Wraparound Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

15	TEFLL	R/W	0h	Tx Event FIFO Event Lost Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

Table 14-24541. MCAN_CORE_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

14	TEFFL	R/W	0h	Tx Event FIFO Full Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

13	TEFWL	R/W	0h	Tx Event FIFO Watermark Reached Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

12	TEFNL	R/W	0h	Tx Event FIFO New Entry Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

11	TFEL	R/W	0h	Tx FIFO Empty Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

10	TCFL	R/W	0h	Transmission Cancellation Finished Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

9	TCL	R/W	0h	Transmission Completed Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

8	HPML	R/W	0h	High Priority Message Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

7	RF1LL	R/W	0h	Rx FIFO 1 Message Lost Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

6	RF1FL	R/W	0h	Rx FIFO 1 Full Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

5	RF1WL	R/W	0h	Rx FIFO 1 Watermark Reached Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

4	RF1NL	R/W	0h	Rx FIFO 1 New Message Interrupt Line
				Reset Source: hsrst_n
				`0h Interrupt assigned to interrupt line INT0`
				`1h Interrupt assigned to interrupt line INT1`

Table 14-24541. MCAN_CORE_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RF0LL	R/W	0h	Rx FIFO 0 Message Lost Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
2	RF0FL	R/W	0h	Rx FIFO 0 Full Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
1	RF0WL	R/W	0h	Rx FIFO 0 Watermark Reached Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1
0	RF0NL	R/W	0h	Rx FIFO 0 New Message Interrupt Line Reset Source: hsrst_n 0h Interrupt assigned to interrupt line INT0 1h Interrupt assigned to interrupt line INT1

14.9.4.1.2.35 MCAN_CORE_ILE Register

1 MCAN_CORE_ILE Register (Offset = 5Ch) [reset = 0h]

Enable/disable interrupt lines m_can_int0 / m_can_int1

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Table 14-24542. Instance Table

Instance Name	Physical Address
MCAN0	**2070 105Ch**
MCAN1	**2071 105Ch**

Figure 14-8100. MCAN_CORE_ILE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						EINT1	EINT0
NONE						R/W	R/W
0h						0h	0h

Table 14-24544. MCAN_CORE_ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved

1	EINT1	R/W	0h	Enable Interrupt Line 1
				Reset Source: hsrst_n
				`0h Interrupt line INT1 disabled`
				`1h Interrupt line INT1 enabled`

0	EINT0	R/W	0h	Enable Interrupt Line 0
				Reset Source: hsrst_n
				`0h Interrupt line INT0 disabled`
				`1h Interrupt line INT0 enabled`

14.9.4.1.2.36 MCAN_CORE_RESERVED55 Register

1 MCAN_CORE_RESERVED55 Register (Offset = 60h) [reset = 0h]

Reserved field

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Table 14-24545. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1060h**
MCAN1	**2071 1060h**

Figure 14-8101. MCAN_CORE_RESERVED55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24547. MCAN_CORE_RESERVED55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.37 MCAN_CORE_RESERVED66 Register

1 MCAN_CORE_RESERVED66 Register (Offset = 64h) [reset = 0h]

Reserved field

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Table 14-24548. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1064h**
MCAN1	**2071 1064h**

Figure 14-8102. MCAN_CORE_RESERVED66 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24550. MCAN_CORE_RESERVED66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.38 MCAN_CORE_RESERVED77 Register

1 MCAN_CORE_RESERVED77 Register (Offset = 68h) [reset = 0h]

Reserved field

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Table 14-24551. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1068h**
MCAN1	**2071 1068h**

Figure 14-8103. MCAN_CORE_RESERVED77 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24553. MCAN_CORE_RESERVED77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.39 MCAN_CORE_RESERVED88 Register

1 MCAN_CORE_RESERVED88 Register (Offset = 6Ch) [reset = 0h]

Reserved field

Return to Summary Table

Table 14-24554. Instance Table

Instance Name	Physical Address
MCAN0	**2070 106Ch**
MCAN1	**2071 106Ch**

Figure 14-8104. MCAN_CORE_RESERVED88 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24556. MCAN_CORE_RESERVED88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.40 MCAN_CORE_RESERVED99 Register

1 MCAN_CORE_RESERVED99 Register (Offset = 70h) [reset = 0h]

Reserved field

Return to Summary Table

Table 14-24557. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1070h**
MCAN1	**2071 1070h**

Figure 14-8105. MCAN_CORE_RESERVED99 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24559. MCAN_CORE_RESERVED99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.41 MCAN_CORE_RESERVED1010 Register

1 MCAN_CORE_RESERVED1010 Register (Offset = 74h) [reset = 0h]

Reserved field

Return to Summary Table

Table 14-24560. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1074h**
MCAN1	**2071 1074h**

Figure 14-8106. MCAN_CORE_RESERVED1010 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24562. MCAN_CORE_RESERVED1010 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.42 MCAN_CORE_RESERVED1111 Register

1 MCAN_CORE_RESERVED1111 Register (Offset = 78h) [reset = 0h]

Reserved field

Return to Summary Table

Table 14-24563. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1078h**
MCAN1	**2071 1078h**

Figure 14-8107. MCAN_CORE_RESERVED1111 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24565. MCAN_CORE_RESERVED1111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.43 MCAN_CORE_RESERVED1212 Register

1 MCAN_CORE_RESERVED1212 Register (Offset = 7Ch) [reset = 0h]

Reserved field

Return to Summary Table

Table 14-24566. Instance Table

Instance Name	Physical Address
MCAN0	**2070 107Ch**
MCAN1	**2071 107Ch**

Figure 14-8108. MCAN_CORE_RESERVED1212 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24568. MCAN_CORE_RESERVED1212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.44 MCAN_CORE_GFC Register

1 MCAN_CORE_GFC Register (Offset = 80h) [reset = 0h]

Handling of non-matching frames and remote frames

Return to Summary Table

Table 14-24569. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1080h**
MCAN1	**2071 1080h**

Figure 14-8109. MCAN_CORE_GFC Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">ANFS</td><td colspan="2">ANFE</td><td>RRFS</td><td>RRFE</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-24571. MCAN_CORE_GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

5:4	ANFS	R/W	0h	Accept Non-matching Frames Standard
				Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated.
				Reset Source: hsrst_n
				`0h Accept in Rx FIFO 0`
				`1h Accept in Rx FIFO 1`
				`2h Reject`
				`3h Reject`

3:2	ANFE	R/W	0h	Accept Non-matching Frames Extended
				Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated.
				Reset Source: hsrst_n
				`0h Accept in Rx FIFO 0`
				`1h Accept in Rx FIFO 1`
				`2h Reject`
				`3h Reject`

Table 14-24571. MCAN_CORE_GFC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RRFS	R/W	0h	Reject Remote Frames Standard Reset Source: hsrst_n 0h Filter remote frames with 11-bit standard IDs 1h Reject all remote frames with 11-bit standard IDs
0	RRFE	R/W	0h	Reject Remote Frames Extended Reset Source: hsrst_n 0h Filter remote frames with 29-bit extended IDs 1h Reject all remote frames with 29-bit extended IDs

14.9.4.1.2.45 MCAN_CORE_SIDFC Register

1 MCAN_CORE_SIDFC Register (Offset = 84h) [reset = 0h]

Number of filter elements, pointer to start of filter list

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Table 14-24572. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1084h**
MCAN1	**2071 1084h**

Figure 14-8110. MCAN_CORE_SIDFC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
LSS							
R/W							
0h							
15	14	13	12	11	10	9	8
FLSSA							
R/W							
0h							
7	6	5	4	3	2	1	0
FLSSA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-24574. MCAN_CORE_SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	LSS	R/W	0h	List Size Standard Reset Source: hsrst_n `0h` No standard Message ID filter `1h-80h` Number of standard Message ID filter elements `>80h` Values greater than 128 are interpreted as 128
15:2	FLSSA	R/W	0h	Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.46 MCAN_CORE_XIDFC Register

1 MCAN_CORE_XIDFC Register (Offset = 88h) [reset = 0h]

Number of filter elements, pointer to start of filter list

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Table 14-24575. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1088h**
MCAN1	**2071 1088h**

Figure 14-8111. MCAN_CORE_XIDFC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	LSE						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
FLESA							
R/W							
0h							
7	6	5	4	3	2	1	0
FLESA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-24577. MCAN_CORE_XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved

22:16	LSE	R/W	0h	List Size Extended
				Reset Source: hsrst_n
				`0h` `No extended Message ID filter`
				`1h-40h` `Number of extended Message ID filter elements`
				`>40h` `Values greater than 64 are interpreted as 64`

15:2	FLESA	R/W	0h	Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.47 MCAN_CORE_RESERVED1313 Register

1 MCAN_CORE_RESERVED1313 Register (Offset = 8Ch) [reset = 0h]

Reserved field

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Table 14-24578. Instance Table

Instance Name	Physical Address
MCAN0	**2070 108Ch**
MCAN1	**2071 108Ch**

Figure 14-8112. MCAN_CORE_RESERVED1313 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24580. MCAN_CORE_RESERVED1313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.48 MCAN_CORE_XIDAM Register

1 MCAN_CORE_XIDAM Register (Offset = 90h) [reset = 1FFFFFFFh]

29-bit logical AND mask for J1939

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Table 14-24581. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1090h**
MCAN1	**2071 1090h**

Figure 14-8113. MCAN_CORE_XIDAM Name Register

31	30	29	28	27	26	25	24
RESERVED			EIDM				
NONE			R/W				
0h			1FFFFFFFh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EIDM							
R/W							
1FFFFFFFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EIDM							
R/W							
1FFFFFFFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EIDM							
R/W							
1FFFFFFFh							

Table 14-24583. MCAN_CORE_XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:0	EIDM	R/W	1FFFFFFFh	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Reset Source: hsrst_n

14.9.4.1.2.49 MCAN_CORE_HPMS Register

1 MCAN_CORE_HPMS Register (Offset = 94h) [reset = 0h]

Status monitoring of incoming high priority messages

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Table 14-24584. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1094h**
MCAN1	**2071 1094h**

Figure 14-8114. MCAN_CORE_HPMS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
FLST	FIDX						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
MSI		BIDX					
R		R					
0h		0h					

Table 14-24586. MCAN_CORE_HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved

15	FLST	R	0h	Filter List
				Indicates the filter list of the matching filter element.
				Reset Source: hsrst_n
				`0h Standard Filter List`
				`1h Extended Filter List`

14:8	FIDX	R	0h	Filter Index Index of matching filter element. Range is 0 to MCAN_SIDFC[23-16] LSS - 1 respectively MCAN_XIDFC[22-16] LSE - 1. Reset Source: hsrst_n

7:6	MSI	R	0h	Message Storage Indicator
				Reset Source: hsrst_n
				`0h No FIFO selected`
				`1h FIFO message lost`
				`2h Message stored in FIFO 0`
				`3h Message stored in FIFO 1`

Table 14-24586. MCAN_CORE_HPMS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	BIDX	R	0h	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when the MCAN_HPMS[7-6] MSI = 1h. Reset Source: hsrst_n

14.9.4.1.2.50 MCAN_CORE_NDAT1 Register

1 MCAN_CORE_NDAT1 Register (Offset = 98h) [reset = 0h]

NewDat flags of dedicated Rx buffers 0-31

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Table 14-24587. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1098h**
MCAN1	**2071 1098h**

Figure 14-8115. MCAN_CORE_NDAT1 Name Register

31	30	29	28	27	26	25	24
ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24589. MCAN_CORE_NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND31	R/W1TC	0h	New Data Reset Source: hsrst_n 0h `Rx Buffer not updated` 1h `Rx Buffer updated from new message`
30	ND30	R/W1TC	0h	New Data Reset Source: hsrst_n 0h `Rx Buffer not updated` 1h `Rx Buffer updated from new message`
29	ND29	R/W1TC	0h	New Data Reset Source: hsrst_n 0h `Rx Buffer not updated` 1h `Rx Buffer updated from new message`
28	ND28	R/W1TC	0h	New Data Reset Source: hsrst_n 0h `Rx Buffer not updated` 1h `Rx Buffer updated from new message`

Table 14-24589. MCAN_CORE_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	ND27	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
26	ND26	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
25	ND25	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
24	ND24	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
23	ND23	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
22	ND22	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
21	ND21	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
20	ND20	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
19	ND19	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
18	ND18	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
17	ND17	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-24589. MCAN_CORE_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	ND16	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
15	ND15	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
14	ND14	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
13	ND13	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
12	ND12	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
11	ND11	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
10	ND10	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
9	ND9	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
8	ND8	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
7	ND7	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
6	ND6	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-24589. MCAN_CORE_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ND5	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
4	ND4	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
3	ND3	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
2	ND2	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
1	ND1	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
0	ND0	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

14.9.4.1.2.51 MCAN_CORE_NDAT2 Register

1 MCAN_CORE_NDAT2 Register (Offset = 9Ch) [reset = 0h]

NewDat flags of dedicated Rx buffers 32-63

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Table 14-24590. Instance Table

Instance Name	Physical Address
MCAN0	**2070 109Ch**
MCAN1	**2071 109Ch**

Figure 14-8116. MCAN_CORE_NDAT2 Name Register

31	30	29	28	27	26	25	24
ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24592. MCAN_CORE_NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND63	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
30	ND62	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
29	ND61	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
28	ND60	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-24592. MCAN_CORE_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	ND59	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
26	ND58	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
25	ND57	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
24	ND56	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
23	ND55	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
22	ND54	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
21	ND53	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
20	ND52	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
19	ND51	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
18	ND50	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
17	ND49	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-24592. MCAN_CORE_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	ND48	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
15	ND47	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
14	ND46	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
13	ND45	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
12	ND44	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
11	ND43	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
10	ND42	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
9	ND41	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
8	ND40	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
7	ND39	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
6	ND38	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

Table 14-24592. MCAN_CORE_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ND37	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
4	ND36	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
3	ND35	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
2	ND34	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
1	ND33	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message
0	ND32	R/W1TC	0h	New Data Reset Source: hsrst_n 0h Rx Buffer not updated 1h Rx Buffer updated from new message

14.9.4.1.2.52 MCAN_CORE_RXF0C Register

1 MCAN_CORE_RXF0C Register (Offset = A0h) [reset = 0h]

FIFO 0 operation mode, watermark, size and start address

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Table 14-24593. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10A0h**
MCAN1	**2071 10A0h**

Figure 14-8117. MCAN_CORE_RXF0C Name Register

31	30	29	28	27	26	25	24
F0OM	F0WM						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED	F0S						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
F0SA							
R/W							
0h							
7	6	5	4	3	2	1	0
F0SA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-24595. MCAN_CORE_RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	R/W	0h	FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see Rx FIFOs). Reset Source: hsrst_n 0h FIFO 0 blocking mode 1h FIFO 0 overwrite mode
30:24	F0WM	R/W	0h	Rx FIFO 0 Watermark Reset Source: hsrst_n 0h Watermark interrupt disabled 1h-40h Level for Rx FIFO 0 watermark interrupt (MCAN_IR[1] RF0W) >40h Watermark interrupt disabled
23	RESERVED	NONE	0h	Reserved
22:16	F0S	R/W	0h	Rx FIFO 0 Size Reset Source: hsrst_n 0h No Rx FIFO 0 1h-40h Number of Rx FIFO 0 elements >40h Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to MCAN_RXF0C[22-16] F0S - 1.

Table 14-24595. MCAN_CORE_RXF0C Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:2	F0SA	R/W	0h	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.53 MCAN_CORE_RXF0S Register

1 MCAN_CORE_RXF0S Register (Offset = A4h) [reset = 0h]

FIFO 0 message lost/full indication, put index, get index and fill level

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Table 14-24596. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10A4h**
MCAN1	**2071 10A4h**

Figure 14-8118. MCAN_CORE_RXF0S Name Register

31	30	29	28	27	26	25	24
RESERVED						RF0L	F0F
NONE						R	R
0h						0h	0h

23	22	21	20	19	18	17	16
RESERVED		F0PI					
NONE		R					
0h		0h					

15	14	13	12	11	10	9	8
RESERVED		F0GI					
NONE		R					
0h		0h					

7	6	5	4	3	2	1	0
RESERVED	F0FL						
NONE	R						
0h	0h						

Table 14-24598. MCAN_CORE_RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

25	RF0L	R	0h	Rx FIFO 0 Message Lost
				This bit is a copy of interrupt flag MCAN_IR[3] RF0L. When the MCAN_IR[3] RF0L flag is reset, this bit is also reset.
				Note: OverWriting the oldest message when the MCAN_RXF0C[31] F0OM = 1h
				Reset Source: hsrst_n
				`0h No Rx FIFO 0 message lost`
				`1h Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero`

24	F0F	R	0h	Rx FIFO 0 Full
				Reset Source: hsrst_n
				`0h Rx FIFO 0 not full`
				`1h Rx FIFO 0 full`

23:22	RESERVED	NONE	0h	Reserved
21:16	F0PI	R	0h	Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63. Reset Source: hsrst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-24598. MCAN_CORE_RXF0S Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	F0GI	R	0h	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. Reset Source: hsrst_n
7	RESERVED	NONE	0h	Reserved
6:0	F0FL	R	0h	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. Reset Source: hsrst_n

14.9.4.1.2.54 MCAN_CORE_RXF0A Register

1 MCAN_CORE_RXF0A Register (Offset = A8h) [reset = 0h]

FIFO 0 acknowledge last index of read buffers, updates get index and fill level

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Table 14-24599. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10A8h**
MCAN1	**2071 10A8h**

Figure 14-8119. MCAN_CORE_RXF0A Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		F0AI					
NONE		R/W					
0h		0h					

Table 14-24601. MCAN_CORE_RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	F0AI	R/W	0h	Rx FIFO 0 Acknowledge Index After the Host CPU has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to the MCAN_RXF0A[5-0] F0AI field. This will set the Rx FIFO 0 Get Index MCAN_RXF0S[13-8] F0GI field to the MCAN_RXF0A[5-0] F0AI field + 1 and update the FIFO 0 Fill Level MCAN_RXF0S[6-0] F0FL field. Reset Source: hsrst_n

14.9.4.1.2.55 MCAN_CORE_RXBC Register

1 MCAN_CORE_RXBC Register (Offset = ACh) [reset = 0h]

Start address of Rx buffer section

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Table 14-24602. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10ACh**
MCAN1	**2071 10ACh**

Figure 14-8120. MCAN_CORE_RXBC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RBSA							
R/W							
0h							
7	6	5	4	3	2	1	0
RBSA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-24604. MCAN_CORE_RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:2	RBSA	R/W	0h	Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address, see Message RAM Configuration). Also used to reference debug messages A, B, C. Note: Debug feature is not supported. Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.56 MCAN_CORE_RXF1C Register

1 MCAN_CORE_RXF1C Register (Offset = B0h) [reset = 0h]

FIFO 1 operation mode, watermark, size and start address

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Table 14-24605. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10B0h**
MCAN1	**2071 10B0h**

Figure 14-8121. MCAN_CORE_RXF1C Name Register

31	30	29	28	27	26	25	24
F1OM	F1WM						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	F1S						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
F1SA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F1SA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-24607. MCAN_CORE_RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	R/W	0h	FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see Rx FIFOs). Reset Source: hsrst_n 0h FIFO 1 blocking mode 1h FIFO 1 overwrite mode
30:24	F1WM	R/W	0h	Rx FIFO 1 Watermark Reset Source: hsrst_n 0h Watermark interrupt disabled 1h-40h Level for Rx FIFO 1 watermark interrupt (MCAN_IR[5] RF1W) >40h Watermark interrupt disabled
23	RESERVED	NONE	0h	Reserved
22:16	F1S	R/W	0h	Rx FIFO 1 Size Reset Source: hsrst_n 0h No Rx FIFO 1 1h-40h Number of Rx FIFO 1 elements >40h Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to MCAN_RXF1C[22-16] F1S - 1.

Table 14-24607. MCAN_CORE_RXF1C Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:2	F1SA	R/W	0h	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.57 MCAN_CORE_RXF1S Register

1 MCAN_CORE_RXF1S Register (Offset = B4h) [reset = 0h]

FIFO 1 message lost/full indication, put index, get index and fill level

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Table 14-24608. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10B4h**
MCAN1	**2071 10B4h**

Figure 14-8122. MCAN_CORE_RXF1S Name Register

31	30	29	28	27	26	25	24
DMS		RESERVED				RF1L	F1F
R		NONE				R	R
0h		0h				0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		F1PI					
NONE		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		F1GI					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	F1FL						
NONE	R						
0h	0h						

Table 14-24610. MCAN_CORE_RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description

31:30	DMS	R	0h	Debug Message Status
				Note: Debug feature is not supported.
				Reset Source: hsrst_n
				`0h` `Idle state, wait for reception of debug messages, DMA request is cleared`
				`1h` `Debug message A received`
				`2h` `Debug messages A, B received`
				`3h` `Debug messages A, B, C received, DMA request is set`

29:26	RESERVED	NONE	0h	Reserved

25	RF1L	R	0h	Rx FIFO 1 Message Lost
				This bit is a copy of interrupt flag MCAN_IR[7] RF1L. When the MCAN_IR[7] RF1L flag is reset, this bit is also reset.
				Note: OverWriting the oldest message when the MCAN_RXF1C[31] F1OM = 1h
				Reset Source: hsrst_n
				`0h` `No Rx FIFO 1 message lost`
				`1h` `Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero`

Table 14-24610. MCAN_CORE_RXF1S Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	F1F	R	0h	Rx FIFO 1 Full Reset Source: hsrst_n 0h Rx FIFO 1 not full 1h Rx FIFO 1 full
23:22	RESERVED	NONE	0h	Reserved
21:16	F1PI	R	0h	Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63. Reset Source: hsrst_n
15:14	RESERVED	NONE	0h	Reserved
13:8	F1GI	R	0h	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. Reset Source: hsrst_n
7	RESERVED	NONE	0h	Reserved
6:0	F1FL	R	0h	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. Reset Source: hsrst_n

14.9.4.1.2.58 MCAN_CORE_RXF1A Register

1 MCAN_CORE_RXF1A Register (Offset = B8h) [reset = 0h]

FIFO 1 acknowledge last index of read buffers, updates get index and fill level

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Table 14-24611. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10B8h**
MCAN1	**2071 10B8h**

Figure 14-8123. MCAN_CORE_RXF1A Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		F1AI					
NONE		R/W					
0h		0h					

Table 14-24613. MCAN_CORE_RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	F1AI	R/W	0h	Rx FIFO 1 Acknowledge Index After the Host CPU has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to the MCAN_RXF1A[5-0] F1AI field. This will set the Rx FIFO 1 Get Index MCAN_RXF1S[13-8] F1GI field to the MCAN_RXF1A[5-0] F1AI field + 1 and update the FIFO 1 Fill Level MCAN_RXF1S[6-0] F1FL field. Reset Source: hsrst_n

14.9.4.1.2.59 MCAN_CORE_RXESC Register

1 MCAN_CORE_RXESC Register (Offset = BCh) [reset = 0h]

Configure data field size for storage of accepted frames

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Table 14-24614. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10BCh**
MCAN1	**2071 10BCh**

Figure 14-8124. MCAN_CORE_RXESC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					RBDS		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED	F1DS			RESERVED	F0DS		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-24616. MCAN_CORE_RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	RBDS	R/W	0h	Rx Buffer Data Field Size Reset Source: hsrst_n 0h 8 byte data field 1h 12 byte data field 2h 16 byte data field 3h 20 byte data field 4h 24 byte data field 5h 32 byte data field 6h 48 byte data field 7h 64 byte data field
7	RESERVED	NONE	0h	Reserved
6:4	F1DS	R/W	0h	Rx FIFO 1 Data Field Size Reset Source: hsrst_n 0h 8 byte data field 1h 12 byte data field 2h 16 byte data field 3h 20 byte data field 4h 24 byte data field 5h 32 byte data field 6h 48 byte data field 7h 64 byte data field

Table 14-24616. MCAN_CORE_RXESC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved
2:0	F0DS	R/W	0h	Rx FIFO 0 Data Field Size Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by the MCAN_RXESC register are stored to the Rx Buffer respectively Rx FIFO element. The rest of the frame's data field is ignored. Reset Source: hsrst_n 0h 8 byte data field 1h 12 byte data field 2h 16 byte data field 3h 20 byte data field 4h 24 byte data field 5h 32 byte data field 6h 48 byte data field 7h 64 byte data field

14.9.4.1.2.60 MCAN_CORE_TXBC Register

1 MCAN_CORE_TXBC Register (Offset = C0h) [reset = 0h]

Configure Tx FIFO/Queue mode, Tx FIFO/Queue size, number of dedicated Tx buffers, Tx buffer start address

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Table 14-24617. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10C0h**
MCAN1	**2071 10C0h**

Figure 14-8125. MCAN_CORE_TXBC Name Register

31	30	29	28	27	26	25	24
RESERVED	TFQM	TFQS					
NONE	R/W	R/W					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		NDTB					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TBSA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBSA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-24619. MCAN_CORE_TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved

30	TFQM	R/W	0h	Tx FIFO/Queue Mode
				Reset Source: hsrst_n
				`0h Tx FIFO operation`
				`1h Tx Queue operation`

29:24	TFQS	R/W	0h	Transmit FIFO/Queue Size
				Reset Source: hsrst_n
				`0h No Tx FIFO/Queue`
				`1h-20h Number of Tx Buffers used for Tx FIFO/Queue`
				`>20h Values greater than 32 are interpreted as 32`

23:22	RESERVED	NONE	0h	Reserved

21:16	NDTB	R/W	0h	Number of Dedicated Transmit Buffers
				Reset Source: hsrst_n
				`0h No Dedicated Tx Buffers`
				`1h-20h Number of Dedicated Tx Buffers`
				`>20h Values greater than 32 are interpreted as 32`

Table 14-24619. MCAN_CORE_TXBC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:2	TBSA	R/W	0h	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Message RAM Configuration). Note: Be aware that the sum of the MCAN_TXBC[29-24] TFQS and MCAN_TXBC[21-16] NDTB fields may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers. Reset Source: hsrst_n
1:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.61 MCAN_CORE_TXFQS Register

1 MCAN_CORE_TXFQS Register (Offset = C4h) [reset = 0h]

Tx FIFO/Queue full indication and put index, Tx FIFO get index and fill level

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Table 14-24620. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10C4h**
MCAN1	**2071 10C4h**

Figure 14-8126. MCAN_CORE_TXFQS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TFQF	TFQPI				
NONE		R	R				
0h		0h	0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TFGI				
NONE			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TFFL					
NONE		R					
0h		0h					

Table 14-24622. MCAN_CORE_TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21	TFQF	R	0h	Tx FIFO/Queue Full Reset Source: hsrst_n 0h Tx FIFO/Queue not full 1h Tx FIFO/Queue full
20:16	TFQPI	R	0h	Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31. Reset Source: hsrst_n
15:13	RESERVED	NONE	0h	Reserved
12:8	TFGI	R	0h	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (MCAN_TXBC[30] TFQM = 1h). Reset Source: hsrst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-24622. MCAN_CORE_TXFQS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	TFFL	R	0h	Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from the MCAN_TXFQS[12-8] TFGI field, range 0 to 32. Read as zero when Tx Queue operation is configured (MCAN_TXBC[30] TFQM = 1h). Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Reset Source: hsrst_n

14.9.4.1.2.62 MCAN_CORE_TXESC Register

1 MCAN_CORE_TXESC Register (Offset = C8h) [reset = 0h]

Configure data field size for frame transmission

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Table 14-24623. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10C8h**
MCAN1	**2071 10C8h**

Figure 14-8127. MCAN_CORE_TXESC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TBDS		
NONE					R/W		
0h					0h		

Table 14-24625. MCAN_CORE_TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TBDS	R/W	0h	Tx Buffer Data Field Size Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size MCAN_TXESC[2-0] TBDS, the bytes not defined by the Tx Buffer are transmitted as CCh (padding bytes). Reset Source: hsrst_n 0h 8 byte data field 1h 12 byte data field 2h 16 byte data field 3h 20 byte data field 4h 24 byte data field 5h 32 byte data field 6h 48 byte data field 7h 64 byte data field

14.9.4.1.2.63 MCAN_CORE_TXBRP Register

1 MCAN_CORE_TXBRP Register (Offset = CCh) [reset = 0h]

Tx buffers with pending transmission request

Return to Summary Table

Table 14-24626. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10CCh**
MCAN1	**2071 10CCh**

Figure 14-8128. MCAN_CORE_TXBRP Name Register

31	30	29	28	27	26	25	24
TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24628. MCAN_CORE_TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description

31	TRP31	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h No transmission request pending`
				`1h Transmission request pending`

30	TRP30	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h No transmission request pending`
				`1h Transmission request pending`

29	TRP29	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h No transmission request pending`
				`1h Transmission request pending`

28	TRP28	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h No transmission request pending`
				`1h Transmission request pending`

Table 14-24628. MCAN_CORE_TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

27	TRP27	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

26	TRP26	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

25	TRP25	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

24	TRP24	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

23	TRP23	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

22	TRP22	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

21	TRP21	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

20	TRP20	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

19	TRP19	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

18	TRP18	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

17	TRP17	R	0h	Transmission Request Pending
				Reset Source: hsrst_n
				`0h` `No transmission request pending`
				`1h` `Transmission request pending`

Table 14-24628. MCAN_CORE_TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TRP16	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
15	TRP15	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
14	TRP14	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
13	TRP13	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
12	TRP12	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
11	TRP11	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
10	TRP10	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
9	TRP9	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
8	TRP8	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
7	TRP7	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
6	TRP6	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending

Table 14-24628. MCAN_CORE_TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TRP5	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
4	TRP4	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
3	TRP3	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
2	TRP2	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
1	TRP1	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending
0	TRP0	R	0h	Transmission Request Pending Reset Source: hsrst_n 0h No transmission request pending 1h Transmission request pending

14.9.4.1.2.64 MCAN_CORE_TXBAR Register

1 MCAN_CORE_TXBAR Register (Offset = D0h) [reset = 0h]

Add transmission requests

Return to Summary Table

Table 14-24629. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10D0h**
MCAN1	**2071 10D0h**

Figure 14-8129. MCAN_CORE_TXBAR Name Register

31	30	29	28	27	26	25	24
AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24631. MCAN_CORE_TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AR31	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
30	AR30	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
29	AR29	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
28	AR28	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added

Table 14-24631. MCAN_CORE_TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	AR27	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
26	AR26	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
25	AR25	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
24	AR24	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
23	AR23	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
22	AR22	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
21	AR21	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
20	AR20	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
19	AR19	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
18	AR18	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
17	AR17	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added

Table 14-24631. MCAN_CORE_TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	AR16	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
15	AR15	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
14	AR14	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
13	AR13	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
12	AR12	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
11	AR11	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
10	AR10	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
9	AR9	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
8	AR8	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
7	AR7	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
6	AR6	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added

Table 14-24631. MCAN_CORE_TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	AR5	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
4	AR4	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
3	AR3	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
2	AR2	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
1	AR1	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added
0	AR0	R/W1TC	0h	Add Request Reset Source: hsrst_n 0h No transmission request added 1h Transmission requested added

14.9.4.1.2.65 MCAN_CORE_TXBCR Register

1 MCAN_CORE_TXBCR Register (Offset = D4h) [reset = 0h]

Request cancellation of pending transmissions

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Table 14-24632. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10D4h**
MCAN1	**2071 10D4h**

Figure 14-8130. MCAN_CORE_TXBCR Name Register

31	30	29	28	27	26	25	24
CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24634. MCAN_CORE_TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description

31	CR31	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

30	CR30	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

29	CR29	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

28	CR28	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

Table 14-24634. MCAN_CORE_TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CR27	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
26	CR26	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
25	CR25	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
24	CR24	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
23	CR23	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
22	CR22	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
21	CR21	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
20	CR20	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
19	CR19	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
18	CR18	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
17	CR17	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending

Table 14-24634. MCAN_CORE_TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CR16	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
15	CR15	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
14	CR14	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
13	CR13	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
12	CR12	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
11	CR11	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
10	CR10	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
9	CR9	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
8	CR8	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
7	CR7	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending
6	CR6	R/W1TC	0h	Cancellation Request Reset Source: hsrst_n 0h No cancellation pending 1h Cancellation pending

Table 14-24634. MCAN_CORE_TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

5	CR5	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

4	CR4	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

3	CR3	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

2	CR2	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

1	CR1	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

0	CR0	R/W1TC	0h	Cancellation Request
				Reset Source: hsrst_n
				`0h No cancellation pending`
				`1h Cancellation pending`

14.9.4.1.2.66 MCAN_CORE_TXBTO Register

1 MCAN_CORE_TXBTO Register (Offset = D8h) [reset = 0h]

Signals successful transmissions, set when corresponding TXBRP flag is cleared

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Table 14-24635. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10D8h**
MCAN1	**2071 10D8h**

Figure 14-8131. MCAN_CORE_TXBTO Name Register

31	30	29	28	27	26	25	24
TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24637. MCAN_CORE_TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description

31	TO31	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

30	TO30	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

29	TO29	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

28	TO28	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

Table 14-24637. MCAN_CORE_TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

27	TO27	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

26	TO26	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

25	TO25	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

24	TO24	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

23	TO23	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

22	TO22	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

21	TO21	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

20	TO20	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

19	TO19	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

18	TO18	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

17	TO17	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

Table 14-24637. MCAN_CORE_TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TO16	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
15	TO15	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
14	TO14	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
13	TO13	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
12	TO12	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
11	TO11	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
10	TO10	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
9	TO9	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
8	TO8	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
7	TO7	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred
6	TO6	R	0h	Transmission Occurred Reset Source: hsrst_n 0h No transmission occurred 1h Transmission occurred

Table 14-24637. MCAN_CORE_TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

5	TO5	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

4	TO4	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

3	TO3	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

2	TO2	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

1	TO1	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

0	TO0	R	0h	Transmission Occurred
				Reset Source: hsrst_n
				`0h No transmission occurred`
				`1h Transmission occurred`

14.9.4.1.2.67 MCAN_CORE_TXBCF Register

1 MCAN_CORE_TXBCF Register (Offset = DCh) [reset = 0h]

Signals successful transmit cancellation, set when corresponding TXBRP flag is cleared after cancellation request

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Table 14-24638. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10DCh**
MCAN1	**2071 10DCh**

Figure 14-8132. MCAN_CORE_TXBCF Name Register

31	30	29	28	27	26	25	24
CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24640. MCAN_CORE_TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description

31	CF31	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

30	CF30	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

29	CF29	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

28	CF28	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h No transmit buffer cancellation`
				`1h Transmit buffer cancellation finished`

Table 14-24640. MCAN_CORE_TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CF27	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
26	CF26	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
25	CF25	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
24	CF24	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
23	CF23	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
22	CF22	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
21	CF21	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
20	CF20	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
19	CF19	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
18	CF18	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
17	CF17	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished

Table 14-24640. MCAN_CORE_TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

16	CF16	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

15	CF15	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

14	CF14	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

13	CF13	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

12	CF12	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

11	CF11	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

10	CF10	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

9	CF9	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

8	CF8	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

7	CF7	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

6	CF6	R	0h	Cancellation Finished
				Reset Source: hsrst_n
				`0h` `No transmit buffer cancellation`
				`1h` `Transmit buffer cancellation finished`

Table 14-24640. MCAN_CORE_TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CF5	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
4	CF4	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
3	CF3	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
2	CF2	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
1	CF1	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished
0	CF0	R	0h	Cancellation Finished Reset Source: hsrst_n 0h No transmit buffer cancellation 1h Transmit buffer cancellation finished

14.9.4.1.2.68 MCAN_CORE_TXBTIE Register

1 MCAN_CORE_TXBTIE Register (Offset = E0h) [reset = 0h]

Enable transmit interrupts for selected Tx buffers

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Table 14-24641. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10E0h**
MCAN1	**2071 10E0h**

Figure 14-8133. MCAN_CORE_TXBTIE Name Register

31	30	29	28	27	26	25	24
TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24643. MCAN_CORE_TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TIE31	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
30	TIE30	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
29	TIE29	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
28	TIE28	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable

Table 14-24643. MCAN_CORE_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

27	TIE27	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

26	TIE26	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

25	TIE25	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

24	TIE24	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

23	TIE23	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

22	TIE22	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

21	TIE21	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

20	TIE20	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

19	TIE19	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

18	TIE18	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

17	TIE17	R/W	0h	Transmission Interrupt Enable
				Reset Source: hsrst_n
				`0h Transmission interrupt disabled`
				`1h Transmission interrupt enable`

Table 14-24643. MCAN_CORE_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TIE16	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
15	TIE15	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
14	TIE14	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
13	TIE13	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
12	TIE12	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
11	TIE11	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
10	TIE10	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
9	TIE9	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
8	TIE8	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
7	TIE7	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
6	TIE6	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable

Table 14-24643. MCAN_CORE_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TIE5	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
4	TIE4	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
3	TIE3	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
2	TIE2	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
1	TIE1	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable
0	TIE0	R/W	0h	Transmission Interrupt Enable Reset Source: hsrst_n 0h Transmission interrupt disabled 1h Transmission interrupt enable

14.9.4.1.2.69 MCAN_CORE_TXBCIE Register

1 MCAN_CORE_TXBCIE Register (Offset = E4h) [reset = 0h]

Enable cancellation finished interrupts for selected Tx buffers

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Table 14-24644. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10E4h**
MCAN1	**2071 10E4h**

Figure 14-8134. MCAN_CORE_TXBCIE Name Register

31	30	29	28	27	26	25	24
CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24646. MCAN_CORE_TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFIE31	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
30	CFIE30	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
29	CFIE29	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
28	CFIE28	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled

Table 14-24646. MCAN_CORE_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CFIE27	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
26	CFIE26	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
25	CFIE25	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
24	CFIE24	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
23	CFIE23	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
22	CFIE22	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
21	CFIE21	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
20	CFIE20	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
19	CFIE19	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
18	CFIE18	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
17	CFIE17	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled

Table 14-24646. MCAN_CORE_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CFIE16	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
15	CFIE15	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
14	CFIE14	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
13	CFIE13	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
12	CFIE12	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
11	CFIE11	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
10	CFIE10	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
9	CFIE9	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
8	CFIE8	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
7	CFIE7	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
6	CFIE6	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled

Table 14-24646. MCAN_CORE_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CFIE5	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
4	CFIE4	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
3	CFIE3	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
2	CFIE2	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
1	CFIE1	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled
0	CFIE0	R/W	0h	Cancellation Finished Interrupt Enable Reset Source: hsrst_n 0h Cancellation finished interrupt disabled 1h Cancellation finished interrupt enabled

14.9.4.1.2.70 MCAN_CORE_RESERVED1414 Register

1 MCAN_CORE_RESERVED1414 Register (Offset = E8h) [reset = 0h]

Reserved Field

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Table 14-24647. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10E8h**
MCAN1	**2071 10E8h**

Figure 14-8135. MCAN_CORE_RESERVED1414 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24649. MCAN_CORE_RESERVED1414 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.71 MCAN_CORE_RESERVED1515 Register

1 MCAN_CORE_RESERVED1515 Register (Offset = ECh) [reset = 0h]

Reserved Field

Return to Summary Table

Table 14-24650. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10ECh**
MCAN1	**2071 10ECh**

Figure 14-8136. MCAN_CORE_RESERVED1515 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24652. MCAN_CORE_RESERVED1515 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.72 MCAN_CORE_TXEFC Register

1 MCAN_CORE_TXEFC Register (Offset = F0h) [reset = 0h]

Tx event FIFO watermark, size and start address

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Table 14-24653. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10F0h**
MCAN1	**2071 10F0h**

Figure 14-8137. MCAN_CORE_TXEFC Name Register

31	30	29	28	27	26	25	24
RESERVED		EFWM					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		EFS					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EFSA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EFSA						RESERVED	
R/W						NONE	
0h						0h	

Table 14-24655. MCAN_CORE_TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	EFWM	R/W	0h	Event FIFO Watermark Reset Source: hsrst_n 0h Watermark interrupt disabled 1h-20h Level for Tx Event FIFO watermark interrupt (MCAN_IR[13] TEFW) >20h Watermark interrupt disabled
23:22	RESERVED	NONE	0h	Reserved
21:16	EFS	R/W	0h	Event FIFO Size Reset Source: hsrst_n 0h Tx Event FIFO disabled 1h-20h Number of Tx Event FIFO elements >20h Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to MCAN_TXEFC[21-16] EFS field - 1.
15:2	EFSA	R/W	0h	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Message RAM Configuration). Reset Source: hsrst_n

Table 14-24655. MCAN_CORE_TXEFC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.73 MCAN_CORE_TXEFS Register

1 MCAN_CORE_TXEFS Register (Offset = F4h) [reset = 0h]

Tx event FIFO element lost/full indication, put index, get index, and fill level

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Table 14-24656. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10F4h**
MCAN1	**2071 10F4h**

Figure 14-8138. MCAN_CORE_TXEFS Name Register

31	30	29	28	27	26	25	24
RESERVED						TEFL	EFF
NONE						R	R
0h						0h	0h
23	22	21	20	19	18	17	16
RESERVED			EFPI				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			EFGI				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		EFFL					
NONE		R					
0h		0h					

Table 14-24658. MCAN_CORE_TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

25	TEFL	R	0h	This bit is a copy of interrupt flag MCAN_IR[15] TEFL. When the MCAN_IR[15] TEFL flag is reset, this bit is also reset.
				Reset Source: hsrst_n
				`0h No Tx Event FIFO element lost`
				`1h Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.`

24	EFF	R	0h	Event FIFO Full
				Reset Source: hsrst_n
				`0h Tx Event FIFO not full`
				`1h Tx Event FIFO full`

23:21	RESERVED	NONE	0h	Reserved
20:16	EFPI	R	0h	Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. Reset Source: hsrst_n
15:13	RESERVED	NONE	0h	Reserved

Table 14-24658. MCAN_CORE_TXEFS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:8	EFGI	R	0h	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. Reset Source: hsrst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	EFFL	R	0h	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. Reset Source: hsrst_n

14.9.4.1.2.74 MCAN_CORE_TXEFA Register

1 MCAN_CORE_TXEFA Register (Offset = F8h) [reset = 0h]

Tx event FIFO acknowledge last index of read elements, updates get index and fill level

Return to Summary Table

Table 14-24659. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10F8h**
MCAN1	**2071 10F8h**

Figure 14-8139. MCAN_CORE_TXEFA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EFAI				
NONE			R/W				
0h			0h				

Table 14-24661. MCAN_CORE_TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EFAI	R/W	0h	After the Host CPU has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to the MCAN_TXEFA[4-0] EFAI field. This will set the Tx Event FIFO Get Index MCAN_TXEFS[12-8] EFGI field to the MCAN_TXEFA[4-0] EFAI field + 1 and update the Event FIFO Fill Level MCAN_TXEFS[5-0] EFFL field. Reset Source: hsrst_n

14.9.4.1.2.75 MCAN_CORE_RESERVED1616 Register

1 MCAN_CORE_RESERVED1616 Register (Offset = FCh) [reset = 0h]

Reserved Field

Return to Summary Table

Table 14-24662. Instance Table

Instance Name	Physical Address
MCAN0	**2070 10FCh**
MCAN1	**2071 10FCh**

Figure 14-8140. MCAN_CORE_RESERVED1616 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24664. MCAN_CORE_RESERVED1616 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.76 MCAN_CORE_RESERVUPPER256_j Register

1 MCAN_CORE_RESERVUPPER256_j Register (Offset = 100h + formula) [reset = 0h]

Reserved Field

Return to Summary Table

Offset = (j * 4h); where j = 0 to 63d

Table 14-24665. Instance Table

Instance Name	Physical Address
MCAN0	**2070 1100h + formula**
MCAN1	**2071 1100h + formula**

Figure 14-8141. MCAN_CORE_RESERVUPPER256_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24667. MCAN_CORE_RESERVUPPER256_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.1.2.77 MCAN_MSGMEM_WRAP_MSGMEM_VBP_RAM_RAM_REG_j Register

1 MCAN_MSGMEM_WRAP_MSGMEM_VBP_RAM_RAM_REG_j Register (Offset = 0h + formula) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 4351d

Table 14-24668. Instance Table

Instance Name	Physical Address
MCAN0	**2070 8000h + formula**
MCAN1	**2071 8000h + formula**

Figure 14-8142. MCAN_MSGMEM_WRAP_MSGMEM_VBP_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-24670. MCAN_MSGMEM_WRAP_MSGMEM_VBP_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_mod_g_rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_mod_g_rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_mod_g_rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_mod_g_rst_n

14.9.4.1.2.78 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

Return to Summary Table

Table 14-24671. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8000h**
MCAN1	**2401 9000h**

Figure 14-8143. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-24673. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL Version
10:8	REVMAJ	R	2h	Major Version
7:6	CUSTOM	R	0h	Custom Version
5:0	REVMIN	R	1h	Minor Version

14.9.4.1.2.79 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

Return to Summary Table

Table 14-24674. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8008h**
MCAN1	**2401 9008h**

Figure 14-8144. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-24676. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1TS	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

14.9.4.1.2.80 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 2h]

Misc Status

Return to Summary Table

Table 14-24677. Instance Table

Instance Name	Physical Address
MCAN0	**2401 800Ch**
MCAN1	**2401 900Ch**

Figure 14-8145. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					2h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
2h							

Table 14-24679. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	2h	Number of RAMs Indicates the number of RAMs serviced by the ECC Aggregator.

14.9.4.1.2.81 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 7d

Table 14-24680. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8010h + formula**
MCAN1	**2401 9010h + formula**

Figure 14-8146. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-24682. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.4.1.2.82 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-24683. Instance Table

Instance Name	Physical Address
MCAN0	**2401 803Ch**
MCAN1	**2401 903Ch**

Figure 14-8147. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-24685. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	Single Error Correction End Of Interrupt (SEC EOI)

14.9.4.1.2.83 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-24686. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8040h**
MCAN1	**2401 9040h**

Figure 14-8148. ECC_AGGR_SEC_STATUS_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CTRL_EDC_VBUSS_PEND</td><td>MSGMEM_PEND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-24688. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	R/W1TS	0h	Interrupt Pending Status for CTRL_EDC_VBUSS_PEND
0	MSGMEM_PEND	R/W1TS	0h	Interrupt Pending Status for MSGMEM_PEND

14.9.4.1.2.84 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-24689. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8080h**
MCAN1	**2401 9080h**

Figure 14-8149. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CTRL_EDC_VBUSS_ENABLE_SET</td><td>MSGMEM_ENABLE_SET</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-24691. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for MSGMEM_PEND

14.9.4.1.2.85 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-24692. Instance Table

Instance Name	Physical Address
MCAN0	**2401 80C0h**
MCAN1	**2401 90C0h**

Figure 14-8150. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_CLR	MSGMEM_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-24694. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for MSGMEM_PEND

14.9.4.1.2.86 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-24695. Instance Table

Instance Name	Physical Address
MCAN0	**2401 813Ch**
MCAN1	**2401 913Ch**

Figure 14-8151. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-24697. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	Double Error Correction End Of Interrupt (DED EOI)

14.9.4.1.2.87 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-24698. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8140h**
MCAN1	**2401 9140h**

Figure 14-8152. ECC_AGGR_DED_STATUS_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CTRL_EDC_VBUSS_PEND</td><td>MSGMEM_PEND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-24700. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	R/W1TS	0h	Interrupt Pending Status for CTRL_EDC_VBUSS_PEND
0	MSGMEM_PEND	R/W1TS	0h	Interrupt Pending Status for MSGMEM_PEND

14.9.4.1.2.88 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-24701. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8180h**
MCAN1	**2401 9180h**

Figure 14-8153. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_SET	MSGMEM_ENABLE_SET
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-24703. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for MSGMEM_PEND

14.9.4.1.2.89 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-24704. Instance Table

Instance Name	Physical Address
MCAN0	**2401 81C0h**
MCAN1	**2401 91C0h**

Figure 14-8154. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_CLR	MSGMEM_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-24706. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for MSGMEM_PEND

14.9.4.1.2.90 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 14-24707. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8200h**
MCAN1	**2401 9200h**

Figure 14-8155. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-24709. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt Enable Set for Serial ECC Interface Timeout Errors
0	PARITY	R/W1TS	0h	Interrupt Enable Set for Parity Errors

14.9.4.1.2.91 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-24710. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8204h**
MCAN1	**2401 9204h**

Figure 14-8156. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-24712. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt Enable Clear for Serial ECC Interface Timeout Errors
0	PARITY	R/W1TC	0h	Interrupt Enable Clear for Parity Errors

14.9.4.1.2.92 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-24713. Instance Table

Instance Name	Physical Address
MCAN0	**2401 8208h**
MCAN1	**2401 9208h**

Figure 14-8157. ECC_AGGR_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-24715. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	Interrupt Status Set for Serial ECC Interface Timeout Errors
1:0	PARITY	R/WI	0h	Interrupt Status Set for Parity Errors

14.9.4.1.2.93 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-24716. Instance Table

Instance Name	Physical Address
MCAN0	**2401 820Ch**
MCAN1	**2401 920Ch**

Figure 14-8158. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-24718. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	Interrupt Status Clear for Serial ECC Interface Timeout Errors
1:0	PARITY	R/WD	0h	Interrupt Status Clear for Parity Errors

14.9.4.2 ECAP

ECAP

14.9.4.2.1 ECAP Summaries

ECAP Summaries

Table 14-24719. ECAP Registers, Base Address=2310 0000h, Length=256

Offset	Length	Register Name	ECAP0 Physical Address	ECAP1 Physical Address	ECAP2 Physical Address
0h	32	ECAP_TSCNT	2310 0000h	2311 0000h	2312 0000h
4h	32	ECAP_CNTPHS	2310 0004h	2311 0004h	2312 0004h
8h	32	ECAP_CAP1	2310 0008h	2311 0008h	2312 0008h
Ch	32	ECAP_CAP2	2310 000Ch	2311 000Ch	2312 000Ch
10h	32	ECAP_CAP3	2310 0010h	2311 0010h	2312 0010h
14h	32	ECAP_CAP4	2310 0014h	2311 0014h	2312 0014h
28h	32	ECAP_ECCTL	2310 0028h	2311 0028h	2312 0028h
2Ch	32	ECAP_ECINT_EN_FLG	2310 002Ch	2311 002Ch	2312 002Ch
30h	32	ECAP_ECINT_CLR_FRC	2310 0030h	2311 0030h	2312 0030h
5Ch	32	ECAP_PID	2310 005Ch	2311 005Ch	2312 005Ch

14.9.4.2.2 ECAP Registers

ECAP Registers

14.9.4.2.2.1 ECAP_TSCNT Register

1 ECAP_TSCNT Register (Offset = 0h) [reset = 0h]

Time Stamp Counter Register

Return to Summary Table

Table 14-24720. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0000h**
ECAP1	**2311 0000h**
ECAP2	**2312 0000h**

Figure 14-8159. ECAP_TSCNT Name Register

31	30	29	28	27	26	25	24
TSCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
TSCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
TSCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
TSCNT							
R/W							
0h							

Table 14-24722. ECAP_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSCNT	R/W	0h	Active 32 bit Counter register which is used as the Capture time-base Reset Source: vbus_rst_mod_g_rst_n

14.9.4.2.2.2 ECAP_CNTPHS Register

1 ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]

Counter Phase Control Register

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Table 14-24723. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0004h**
ECAP1	**2311 0004h**
ECAP2	**2312 0004h**

Figure 14-8160. ECAP_CNTPHS Name Register

31	30	29	28	27	26	25	24
CNTPHS							
R/W							
0h							
23	22	21	20	19	18	17	16
CNTPHS							
R/W							
0h							
15	14	13	12	11	10	9	8
CNTPHS							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTPHS							
R/W							
0h							

Table 14-24725. ECAP_CNTPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTPHS	R/W	0h	Counter phase value register that can be programmed for phase Lag/Lead. This register shadows the ECAP_TSCNT register and is loaded into the ECAP_TSCNT register upon either a SYNCI event or software force via a control bit. Used to achieve phase control sync with respect to other ECAP and EPWM time-bases. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.2.2.3 ECAP_CAP1 Register

1 ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

Capture-1 Register

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Table 14-24726. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0008h**
ECAP1	**2311 0008h**
ECAP2	**2312 0008h**

Figure 14-8161. ECAP_CAP1 Name Register

31	30	29	28	27	26	25	24
CAP1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CAP1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAP1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAP1							
R/W							
0h							

Table 14-24728. ECAP_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP1	R/W	0h	This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes/initialisation. 3. APRD shadow register (ECAP_CAP3) when used in APWM mode. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.2.2.4 ECAP_CAP2 Register

1 ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

Capture-2 Register

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Table 14-24729. Instance Table

Instance Name	Physical Address
ECAP0	**2310 000Ch**
ECAP1	**2311 000Ch**
ECAP2	**2312 000Ch**

Figure 14-8162. ECAP_CAP2 Name Register

31	30	29	28	27	26	25	24
CAP2							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP2							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP2							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP2							
R/W							
0h							

Table 14-24731. ECAP_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP2	R/W	0h	This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes. 3. ACMP shadow register (ECAP_CAP4) when used in APWM mode. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.2.2.5 ECAP_CAP3 Register

1 ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

Capture-3 Register

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Table 14-24732. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0010h**
ECAP1	**2311 0010h**
ECAP2	**2312 0010h**

Figure 14-8163. ECAP_CAP3 Name Register

31	30	29	28	27	26	25	24
CAP3							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP3							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP3							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP3							
R/W							
0h							

Table 14-24734. ECAP_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP3	R/W	0h	In CMP mode this is a time-stamp capture register. In APMW mode this is the period shadow (APER) register. User updates the PWM period value via this register. In this mode the ECAP_CAP3 (APRD) register shadows the ECAP_CAP1 register. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.2.2.6 ECAP_CAP4 Register

1 ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

Capture-4 Register

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Table 14-24735. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0014h**
ECAP1	**2311 0014h**
ECAP2	**2312 0014h**

Figure 14-8164. ECAP_CAP4 Name Register

31	30	29	28	27	26	25	24
CAP4							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP4							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP4							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP4							
R/W							
0h							

Table 14-24737. ECAP_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP4	R/W	0h	In CMP mode this is a time-stamp capture register. In APMW mode this is the compare shadow (ACMP) register. User updates the PWM Compare value via this register. In this mode the ECAP_CAP4 (ACMP) register shadows the ECAP_CAP2 register. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.2.2.7 ECAP_ECCTL Register

1 ECAP_ECCTL Register (Offset = 28h) [reset = 60000h]

ECAP Control Register

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Table 14-24738. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0028h**
ECAP1	**2311 0028h**
ECAP2	**2312 0028h**

Figure 14-8165. ECAP_ECCTL Name Register

31	30	29	28	27	26	25	24
FILTER					APWMPOL	CAP_APWM	SWSYNC
R					R/W	R/W	WTC
0h					0h	0h	0h
23	22	21	20	19	18	17	16
SYNCO_SEL		SYNCI_EN	TSCNTSTP	REARM_RESET	STOPVALUE		CONT_ONESHT
R/W		R/W	R/W	WTC	R/W		R/W
0h		0h	0h	0h	3h		0h
15	14	13	12	11	10	9	8
FREE_SOFT		EVTFLTPS					CAPLDEN
R/W		R/W					R/W
0h		0h					0h
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24740. ECAP_ECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	FILTER	R	0h	Reset Source: vbus_rst_mod_g_rst_n

26	APWMPOL	R/W	0h	APWM Output Polarity Select:
				Note: This is applicable only in APWM operating mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h Output is Active High (Compare value defines High time)`
				`1h Output is Active Low (Compare value defines Low time)`

Table 14-24740. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CAP_APWM	R/W	0h	CAP/APWM Operating Mode Select: Reset Source: vbus_rst_mod_g_rst_n 0h ECAP module operates in Capture mode. This mode forces the following configuration: 1. Inhibits the ECAP_TSCNT register resets via PRD event. 2. Inhibits the Shadow loads on the ECAP_CAP1 and ECAP_CAP2 registers. 3. Permits user to enable the ECAP_CAP1 to ECAP_CAP4 register load. 4. CAPx/APWMx pin operates as a Capture input. 1h ECAP module operates in APWM mode. This mode forces the following configuration: 1. Resets the ECAP_TSCNT register on PRD event (period boundary) 2. Permits Shadow loading on the ECAP_CAP1 and ECAP_CAP2 registers. 3. Disables loading of Time-stamps into the ECAP_CAP1 - ECAP_CAP4 registers 4. CAPx/APWMx pin operates as a APWM output.
24	SWSYNC	WTC	0h	Software Forced Counter (ECAP_TSCNT) Synchronizing: Reset Source: vbus_rst_mod_g_rst_n 0h Writing a zero has no effect. Reading will always return a zero. 1h Writing a one will force a ECAP_TSCNT shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0h
23:22	SYNCO_SEL	R/W	0h	SyncOut Select: Note: Selection PRD is meaningful only in APWM mode, however can still be chosen in CAP mode if user believes it to be useful. Reset Source: vbus_rst_mod_g_rst_n 0h Select SyncIn event to be the SyncOut signal (pass through) 1h Select PRD event to be the SyncOut signal 2h Disable SyncOut Signal 3h Disable SyncOut Signal
21	SYNCI_EN	R/W	0h	Counter (ECAP_TSCNT) SyncIn select mode: Reset Source: vbus_rst_mod_g_rst_n 0h Disable SyncIn option 1h Enable Counter (ECAP_TSCNT) to be loaded from the ECAP_CNTPHS register upon either a SYNCI signal or a software force event.
20	TSCNTSTP	R/W	0h	Counter Stop (freeze) Control: Reset Source: vbus_rst_mod_g_rst_n 0h Counter Stopped 1h Counter Free Running
19	REARM_RESET	WTC	0h	One-Shot Re-arming Control Wait for stop trigger: Reset Source: vbus_rst_mod_g_rst_n 0h Has no effect. Reading always returns a 0h 1h Arms the One-Shot sequence: 1. Resets the Mod4 counter to zero. 2. Un-freezes the Mod4 counter. 3. Enables Capture Register Loads.

Table 14-24740. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:17	STOPVALUE	R/W	3h	Stop Value for One-Shot Mode: This is the number (between 1 and 4) of captures allowed to occur before the ECAP_CAP1 through ECAP_CAP4 registers are frozen (capture sequence is stopped). Notes: [1] STOPVALUE is compared to Mod4 counter, when equal, two actions occur: 1. Mod4 Counter is stopped (frozen) 2. Capture register loads are inhibited [2] In one shot mode, further interrupt events are blocked until we re-arm, once the number of events captured has been reached. Reset Source: vbus_rst_mod_g_rst_n 0h Stop after Capture Event 1 1h Stop after Capture Event 2 2h Stop after Capture Event 3 3h Stop after Capture Event 4
16	CONT_ONESHT	R/W	0h	Continuous or One-shot Mode Control (applicable only in Capture mode): Reset Source: vbus_rst_mod_g_rst_n 0h Operate in continuous mode 1h Operate in One-Shot mode
15:14	FREE_SOFT	R/W	0h	Emulation Control Reset Source: vbus_rst_mod_g_rst_n 0h ECAP_TSCNT Counter stops immediately on emulation suspend 1h ECAP_TSCNT Counter runs until = 0h 3h ECAP_TSCNT Counter is unaffected by emulation suspend (Run Free)
13:9	EVTFLTPS	R/W	0h	Event Filter Prescale Select: Reset Source: vbus_rst_mod_g_rst_n 0h Divide by 1 (no prescale, by-pass the prescaler) 1Eh Divide by 60 1Fh Divide by 62 1h Divide by 2 2h Divide by 4 3h Divide by 6 4h Divide by 8 5h Divide by 10
8	CAPLDEN	R/W	0h	Enable Loading of the ECAP_CAP1 to ECAP_CAP4 registers on a capture event: Reset Source: vbus_rst_mod_g_rst_n 0h Disable ECAP_CAP1 to ECAP_CAP4 register loads at capture event time. 1h Enable ECAP_CAP1 to ECAP_CAP4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4: Reset Source: vbus_rst_mod_g_rst_n 0h Do Not reset Counter on Capture Event 4 (absolute time stamp) 1h Reset counter after Event 4 time-stamp has been captured (used in Difference mode operation)

Table 14-24740. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CAP4POL	R/W	0h	Capture Event 4 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 4 triggered on a Rising Edge (RE) 1h Capture event 4 triggered on a Falling Edge (FE)
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 3 (absolute time stamp) 1h Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 3 triggered on a Rising Edge (RE) 1h Capture event 3 triggered on a Falling Edge (FE)
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 2 (absolute time stamp) 1h Reset Counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 2 triggered on a Rising Edge (RE) 1h Capture event 2 triggered on a Falling Edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 1 (absolute time stamp) 1h Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 1 triggered on a Rising Edge (RE) 1h Capture event 1 triggered on a Falling Edge (FE)

14.9.4.2.2.8 ECAP_ECINT_EN_FLG Register

1 ECAP_ECINT_EN_FLG Register (Offset = 2Ch) [reset = 0h]

ECAP Interrupt Enable and Flag Register

Return to Summary Table

Table 14-24741. Instance Table

Instance Name	Physical Address
ECAP0	**2310 002Ch**
ECAP1	**2311 002Ch**
ECAP2	**2312 002Ch**

Figure 14-8166. ECAP_ECINT_EN_FLG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CMPEQ_FLG	PRDEQ_FLG	CNTOVF_FLG	CEVT4_FLG	CEVT3_FLG	CEVT2_FLG	CEVT1_FLG	INT_FLG
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CMPEQ_EN	PRDEQ_EN	CNTOVF_EN	CEVT4_EN	CEVT3_EN	CEVT2_EN	CEVT1_EN	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24743. ECAP_ECINT_EN_FLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

23	CMPEQ_FLG	R	0h	Compare Equal Status Flag:
				Note: This flag is only active in APWM mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h Indicates no event occurred`
				`1h Indicates the counter (ECAP_TSCNT) reached the Compare register value (ACMP)`

22	PRDEQ_FLG	R	0h	Period Equal Status Flag:
				Note: This flag is only active in APWM mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h Indicates no event occurred`
				`1h Indicates the Counter (ECAP_TSCNT) reached the Period register value (APER) and was reset.`

Table 14-24743. ECAP_ECINT_EN_FLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	CNTOVF_FLG	R	0h	Counter Overflow Status Flag: Note: This flag is active in CAP and APWM mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the Counter (ECAP_TSCNT) has made the transition from FFFF FFFFh to 0000 0000h
20	CEVT4_FLG	R	0h	Capture Event 4 Status Flag: Note: This flag is only active in CAP mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the fourth event occurred at ECAPx pin.
19	CEVT3_FLG	R	0h	Capture Event 3 Status Flag: Note: This flag is only active in CAP mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the third event occurred at ECAPx pin.
18	CEVT2_FLG	R	0h	Capture Event 2 Status Flag: Note: This flag is only active in CAP mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the second event occurred at ECAPx pin.
17	CEVT1_FLG	R	0h	Capture Event 1 Status Flag: Note: This flag is only active in CAP mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred. 1h Indicates the first event occurred at ECAPx pin.
16	INT_FLG	R	0h	Global Interrupt Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no interrupt generated. 1h Indicates that an interrupt was generated from one of the following events.
15:8	RESERVED	NONE	0h	Reserved
7	CMPEQ_EN	R/W	0h	Compare Equal Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Compare Equal as an Interrupt source 1h Enable Compare Equal as an Interrupt source
6	PRDEQ_EN	R/W	0h	Period Equal Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Period Equal as an Interrupt source 1h Enable Period Equal as an Interrupt source
5	CNTOVF_EN	R/W	0h	Counter Overflow Interrupt Enable: Reset Source: vbus_rst_mod_g_rst_n 0h Disabled Counter Overflow as an Interrupt source 1h Enable Counter Overflow as an Interrupt source

Table 14-24743. ECAP_ECINT_EN_FLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

4	CEVT4_EN	R/W	0h	Capture Event 4 Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Capture Event 4 as an Interrupt source:`
				`1h` `Enable Capture Event 4 as an Interrupt source`

3	CEVT3_EN	R/W	0h	Capture Event 3 Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Capture Event 3 as an Interrupt source:`
				`1h` `Enable Capture Event 3 as an Interrupt source`

2	CEVT2_EN	R/W	0h	Capture Event 2 Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Capture Event 2 as an Interrupt source:`
				`1h` `Enable Capture Event 2 as an Interrupt source`

1	CEVT1_EN	R/W	0h	Capture Event 1 Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Capture Event 1 as an Interrupt source:`
				`1h` `Enable Capture Event 1 as an Interrupt source`

0	RESERVED	NONE	0h	Reserved

14.9.4.2.2.9 ECAP_ECINT_CLR_FRC Register

1 ECAP_ECINT_CLR_FRC Register (Offset = 30h) [reset = 0h]

ECAP Interrupt Clear and Forcing Register

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Table 14-24744. Instance Table

Instance Name	Physical Address
ECAP0	**2310 0030h**
ECAP1	**2311 0030h**
ECAP2	**2312 0030h**

Figure 14-8167. ECAP_ECINT_CLR_FRC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CMPEQ_FRC	PRDEQ_FRC	CNTOVF_FRC	CEVT4_FRC	CEVT3_FRC	CEVT2_FRC	CEVT1_FRC	RESERVED
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	NONE
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CMPEQ_CLR	PRDEQ_CLR	CNTOVF_CLR	CEVT4_CLR	CEVT3_CLR	CEVT2_CLR	CEVT1_CLR	INT_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24746. ECAP_ECINT_CLR_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	CMPEQ_FRC	W1TS	0h	Force Compare Equal: Reset Source: vbus_rst_mod_g_rst_n 0h `No effect. Always reads back a 0h` 1h `Writing a 1h to this bit will set the CMPEQ_FLG flag bit.`
22	PRDEQ_FRC	W1TS	0h	Force Period Equal: Reset Source: vbus_rst_mod_g_rst_n 0h `No effect. Always reads back a 0.` 1h `Writing a 1h to this bit will set the PRDEQ_FLG flag bit.`
21	CNTOVF_FRC	W1TS	0h	Force Counter Overflow: Reset Source: vbus_rst_mod_g_rst_n 0h `No effect. Always reads back a 0.` 1h `Writing a 1h to this bit will set the CNTOVF_FLG flag bit.`

Table 14-24746. ECAP_ECINT_CLR_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

20	CEVT4_FRC	W1TS	0h	Force Capture Event 4:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h to this bit will set the CEVT4_FLG flag bit.`

19	CEVT3_FRC	W1TS	0h	Force Capture Event 3:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h to this bit will set the CEVT3_FLG flag bit.`

18	CEVT2_FRC	W1TS	0h	Force Capture Event 2:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h to this bit will set the CEVT2_FLG flag bit.`

17	CEVT1_FRC	W1TS	0h	Force Capture Event 1:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h to this bit will set the CEVT1_FLG flag bit.`

16:8	RESERVED	NONE	0h	Reserved

7	CMPEQ_CLR	W1TC	0h	Compare Equal Status Flag:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h will clear the CMPEQ_FLG flag condition.`

6	PRDEQ_CLR	W1TC	0h	Period Equal Status Flag:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h will clear the PRDEQ_FLG flag condition.`

5	CNTOVF_CLR	W1TC	0h	Counter Overflow Status Flag:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h will clear the CNTOVF_FLG flag condition.`

4	CEVT4_CLR	W1TC	0h	Capture Event 4 Status Flag:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h will clear the CEVT4_FLG flag condition.`

3	CEVT3_CLR	W1TC	0h	Capture Event 3 Status Flag:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h will clear the CEVT3_FLG flag condition.`

2	CEVT2_CLR	W1TC	0h	Capture Event 2 Status Flag:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `No effect. Always reads back a 0.`
				`1h` `Writing a 1h will clear the CEVT2_FLG flag condition.`

Table 14-24746. ECAP_ECINT_CLR_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1_CLR	W1TC	0h	Capture Event 1 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT1_FLG flag condition.
0	INT_CLR	W1TC	0h	Global Interrupt Clear Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the INT_FLG flag and enable further interrupts to be generated if any of the event flags are set to 1h.

14.9.4.2.2.10 ECAP_PID Register

1 ECAP_PID Register (Offset = 5Ch) [reset = 44D24100h]

Peripheral ID Register

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Table 14-24747. Instance Table

Instance Name	Physical Address
ECAP0	**2310 005Ch**
ECAP1	**2311 005Ch**
ECAP2	**2312 005Ch**

Figure 14-8168. ECAP_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNCTION			
R		R		R			
1h		0h		4D2h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
4D2h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
8h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-24749. ECAP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Reset Source: vbus_rst_mod_g_rst_n
29:28	RESERVED	R	0h	
27:16	FUNCTION	R	4D2h	Reset Source: vbus_rst_mod_g_rst_n
15:11	RTL	R	8h	Reset Source: vbus_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Reset Source: vbus_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Reset Source: vbus_rst_mod_g_rst_n
5:0	MINOR	R	0h	Reset Source: vbus_rst_mod_g_rst_n

14.9.4.3 EPWM

EPWM

14.9.4.3.1 EPWM Summaries

EPWM Summaries

Table 14-24750. EPWM Registers, Base Address=2300 0000h, Length=256

Offset	Length	Register Name	EPWM0 Physical Address	EPWM1 Physical Address	EPWM2 Physical Address
0h	16	EPWM_TBCTL	2300 0000h	2301 0000h	2302 0000h
2h	16	EPWM_TBSTS	2300 0002h	2301 0002h	2302 0002h
4h	16	EPWM_TBPHSHR	2300 0004h	2301 0004h	2302 0004h
6h	16	EPWM_TBPHS	2300 0006h	2301 0006h	2302 0006h
8h	16	EPWM_TBCNT	2300 0008h	2301 0008h	2302 0008h
Ah	16	EPWM_TBPRD	2300 000Ah	2301 000Ah	2302 000Ah
Eh	16	EPWM_CMPCTL	2300 000Eh	2301 000Eh	2302 000Eh
10h	16	EPWM_CMPAHR	2300 0010h	2301 0010h	2302 0010h
12h	16	EPWM_CMPA	2300 0012h	2301 0012h	2302 0012h
14h	16	EPWM_CMPB	2300 0014h	2301 0014h	2302 0014h
16h	16	EPWM_AQCTLA	2300 0016h	2301 0016h	2302 0016h
18h	16	EPWM_AQCTLB	2300 0018h	2301 0018h	2302 0018h
1Ah	16	EPWM_AQSFRC	2300 001Ah	2301 001Ah	2302 001Ah
1Ch	16	EPWM_AQCSFRC	2300 001Ch	2301 001Ch	2302 001Ch
1Eh	16	EPWM_DBCTL	2300 001Eh	2301 001Eh	2302 001Eh
20h	16	EPWM_DBRED	2300 0020h	2301 0020h	2302 0020h
22h	16	EPWM_DBFED	2300 0022h	2301 0022h	2302 0022h
24h	16	EPWM_TZSEL	2300 0024h	2301 0024h	2302 0024h
28h	16	EPWM_TZCTL	2300 0028h	2301 0028h	2302 0028h
2Ah	16	EPWM_TZEINT	2300 002Ah	2301 002Ah	2302 002Ah
2Ch	16	EPWM_TZFLG	2300 002Ch	2301 002Ch	2302 002Ch
2Eh	16	EPWM_TZCLR	2300 002Eh	2301 002Eh	2302 002Eh
30h	16	EPWM_TZFRC	2300 0030h	2301 0030h	2302 0030h
32h	16	EPWM_ETSEL	2300 0032h	2301 0032h	2302 0032h
34h	16	EPWM_ETPS	2300 0034h	2301 0034h	2302 0034h
36h	16	EPWM_ETFLG	2300 0036h	2301 0036h	2302 0036h
38h	16	EPWM_ETCLR	2300 0038h	2301 0038h	2302 0038h
3Ah	16	EPWM_ETFRC	2300 003Ah	2301 003Ah	2302 003Ah
3Ch	16	EPWM_PCCTL	2300 003Ch	2301 003Ch	2302 003Ch
5Ch	32	EPWM_PID	2300 005Ch	2301 005Ch	2302 005Ch

Table 14-24751. EPWM Registers, Base Address=2300 0000h, Length=256

Offset	Length	Register Name	EPWM3 Physical Address	EPWM4 Physical Address	EPWM5 Physical Address
0h	16	EPWM_TBCTL	2303 0000h	2304 0000h	2305 0000h
2h	16	EPWM_TBSTS	2303 0002h	2304 0002h	2305 0002h
4h	16	EPWM_TBPHSHR	2303 0004h	2304 0004h	2305 0004h

Table 14-24751. EPWM Registers, Base Address=2300 0000h, Length=256 (continued)

Offset	Length	Register Name	EPWM3 Physical Address	EPWM4 Physical Address	EPWM5 Physical Address
6h	16	EPWM_TBPHS	2303 0006h	2304 0006h	2305 0006h
8h	16	EPWM_TBCNT	2303 0008h	2304 0008h	2305 0008h
Ah	16	EPWM_TBPRD	2303 000Ah	2304 000Ah	2305 000Ah
Eh	16	EPWM_CMPCTL	2303 000Eh	2304 000Eh	2305 000Eh
10h	16	EPWM_CMPAHR	2303 0010h	2304 0010h	2305 0010h
12h	16	EPWM_CMPA	2303 0012h	2304 0012h	2305 0012h
14h	16	EPWM_CMPB	2303 0014h	2304 0014h	2305 0014h
16h	16	EPWM_AQCTLA	2303 0016h	2304 0016h	2305 0016h
18h	16	EPWM_AQCTLB	2303 0018h	2304 0018h	2305 0018h
1Ah	16	EPWM_AQSFRC	2303 001Ah	2304 001Ah	2305 001Ah
1Ch	16	EPWM_AQCSFRC	2303 001Ch	2304 001Ch	2305 001Ch
1Eh	16	EPWM_DBCTL	2303 001Eh	2304 001Eh	2305 001Eh
20h	16	EPWM_DBRED	2303 0020h	2304 0020h	2305 0020h
22h	16	EPWM_DBFED	2303 0022h	2304 0022h	2305 0022h
24h	16	EPWM_TZSEL	2303 0024h	2304 0024h	2305 0024h
28h	16	EPWM_TZCTL	2303 0028h	2304 0028h	2305 0028h
2Ah	16	EPWM_TZEINT	2303 002Ah	2304 002Ah	2305 002Ah
2Ch	16	EPWM_TZFLG	2303 002Ch	2304 002Ch	2305 002Ch
2Eh	16	EPWM_TZCLR	2303 002Eh	2304 002Eh	2305 002Eh
30h	16	EPWM_TZFRC	2303 0030h	2304 0030h	2305 0030h
32h	16	EPWM_ETSEL	2303 0032h	2304 0032h	2305 0032h
34h	16	EPWM_ETPS	2303 0034h	2304 0034h	2305 0034h
36h	16	EPWM_ETFLG	2303 0036h	2304 0036h	2305 0036h
38h	16	EPWM_ETCLR	2303 0038h	2304 0038h	2305 0038h
3Ah	16	EPWM_ETFRC	2303 003Ah	2304 003Ah	2305 003Ah
3Ch	16	EPWM_PCCTL	2303 003Ch	2304 003Ch	2305 003Ch
5Ch	32	EPWM_PID	2303 005Ch	2304 005Ch	2305 005Ch

Table 14-24752. EPWM Registers, Base Address=2300 0000h, Length=256

Offset	Length	Register Name	EPWM6 Physical Address	EPWM7 Physical Address	EPWM8 Physical Address
0h	16	EPWM_TBCTL	2306 0000h	2307 0000h	2308 0000h
2h	16	EPWM_TBSTS	2306 0002h	2307 0002h	2308 0002h
4h	16	EPWM_TBPHSHR	2306 0004h	2307 0004h	2308 0004h
6h	16	EPWM_TBPHS	2306 0006h	2307 0006h	2308 0006h
8h	16	EPWM_TBCNT	2306 0008h	2307 0008h	2308 0008h
Ah	16	EPWM_TBPRD	2306 000Ah	2307 000Ah	2308 000Ah
Eh	16	EPWM_CMPCTL	2306 000Eh	2307 000Eh	2308 000Eh
10h	16	EPWM_CMPAHR	2306 0010h	2307 0010h	2308 0010h
12h	16	EPWM_CMPA	2306 0012h	2307 0012h	2308 0012h
14h	16	EPWM_CMPB	2306 0014h	2307 0014h	2308 0014h
16h	16	EPWM_AQCTLA	2306 0016h	2307 0016h	2308 0016h
18h	16	EPWM_AQCTLB	2306 0018h	2307 0018h	2308 0018h
1Ah	16	EPWM_AQSFRC	2306 001Ah	2307 001Ah	2308 001Ah

Table 14-24752. EPWM Registers, Base Address=2300 0000h, Length=256 (continued)

Offset	Length	Register Name	EPWM6 Physical Address	EPWM7 Physical Address	EPWM8 Physical Address
1Ch	16	EPWM_AQCSFRC	2306 001Ch	2307 001Ch	2308 001Ch
1Eh	16	EPWM_DBCTL	2306 001Eh	2307 001Eh	2308 001Eh
20h	16	EPWM_DBRED	2306 0020h	2307 0020h	2308 0020h
22h	16	EPWM_DBFED	2306 0022h	2307 0022h	2308 0022h
24h	16	EPWM_TZSEL	2306 0024h	2307 0024h	2308 0024h
28h	16	EPWM_TZCTL	2306 0028h	2307 0028h	2308 0028h
2Ah	16	EPWM_TZEINT	2306 002Ah	2307 002Ah	2308 002Ah
2Ch	16	EPWM_TZFLG	2306 002Ch	2307 002Ch	2308 002Ch
2Eh	16	EPWM_TZCLR	2306 002Eh	2307 002Eh	2308 002Eh
30h	16	EPWM_TZFRC	2306 0030h	2307 0030h	2308 0030h
32h	16	EPWM_ETSEL	2306 0032h	2307 0032h	2308 0032h
34h	16	EPWM_ETPS	2306 0034h	2307 0034h	2308 0034h
36h	16	EPWM_ETFLG	2306 0036h	2307 0036h	2308 0036h
38h	16	EPWM_ETCLR	2306 0038h	2307 0038h	2308 0038h
3Ah	16	EPWM_ETFRC	2306 003Ah	2307 003Ah	2308 003Ah
3Ch	16	EPWM_PCCTL	2306 003Ch	2307 003Ch	2308 003Ch
5Ch	32	EPWM_PID	2306 005Ch	2307 005Ch	2308 005Ch

14.9.4.3.2 EPWM Registers

EPWM Registers

14.9.4.3.2.1 EPWM_TBCTL Register

1 EPWM_TBCTL Register (Offset = 0h) [reset = 83h]

Time-Base Control Register

Return to Summary Table

Table 14-24753. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0000h**
EPWM1	**2301 0000h**
EPWM2	**2302 0000h**
EPWM3	**2303 0000h**
EPWM4	**2304 0000h**
EPWM5	**2305 0000h**
EPWM6	**2306 0000h**
EPWM7	**2307 0000h**
EPWM8	**2308 0000h**

Figure 14-8169. EPWM_TBCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR	CLKDIV			HSPCLKDIV	
R/W		R/W	R/W			R/W	
0h		0h	0h			1h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSPCLKDIV	SWFSYNC	SYNCOSEL		PRDLD	PHSEN	CTRMODE	
R/W	R/W	R/W		R/W	R/W	R/W	
1h	0h	0h		0h	0h	3h	

Table 14-24755. EPWM_TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation Mode Bits These bits select the behavior of the ePWM time-base counter during emulation events: 0h Stop after the next time-base counter increment or decrement 1h Stop when counter completes a whole cycle (a) Up-count mode: stop when the time-base counter = period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD). (b) Down-count mode: stop when the time-base counter = 0000 (EPWM_TBCNT[15-0] TBCNT = 0000h) 2h Free run 3h Free run
13	PHSDIR	R/W	0h	Phase Direction Bit This bit is only used when the time-base counter is configured in the up-down-count mode The PHSDIR bit indicates the direction the time-base counter [TBCNT] will count after a synchronization event occurs and a new phase value is loaded from the phase [TBPHS] register This is irrespective of the direction of the counter before the synchronization event In the up-count and down-count modes this bit is ignored 0h Count down after the synchronization event 1h Count up after the synchronization event

Table 14-24755. EPWM_TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:10	CLKDIV	R/W	0h	Time-base Clock Prescale Bits These bits determine part of the time-base clock prescale value TBCLK = SYSCLKOUT/[HSPCLKDIV - CLKDIV] 0h /1 (default on reset) 1h /2 2h /4 3h /8 4h /16 5h /32 6h /64 7h /128
9:7	HSPCLKDIV	R/W	1h	High-Speed Time-base Clock Prescale Bits These bits determine part of the time-base clock prescale value TBCLK = SYSCLKOUT/[HSPCLKDIV - CLKDIV] This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager [EV] peripheral 0h /1 1h /2 (default on reset) 2h /4 3h /6 4h /8 5h /10 6h /12 7h /14
6	SWFSYNC	R/W	0h	Software Forced Synchronization Pulse 0h Writing a 0h 1h Writing a 1h
5:4	SYNCOSEL	R/W	0h	Synchronization Output Select These bits select the source of the EPWMxSYNCO signal 0h EPWMxSYNC 1h TBCNT = 0: Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h) 2h TBCNT = CMPB: Time-base counter equal to counter-compare B (EPWM_TBCNT[15-0] TBCNT = EPWM_CMPB[15-0] CMPB) 3h Disable EPWMxSYNCO signal
3	PRDLD	R/W	0h	Active Period Register Load From Shadow Register Select 0h The period register (EPWM_TBPRD) is loaded from its shadow register when the time-base counter, EPWM_TBCNT[15-0] TBCNT, is equal to zero. A write or read to the EPWM_TBPRD register accesses the shadow register. 1h Load the EPWM_TBPRD register immediately without using a shadow register. A write or read to the EPWM_TBPRD register directly accesses the active register.
2	PHSEN	R/W	0h	Counter Register Load From Phase Register Enable 0h Do not load the time-base counter (EPWM_TBCNT) from the time-base phase register (EPWM_TBPHS) 1h Load the time-base counter with the phase register when an EPWMxSYNCI input signal occurs or when a software synchronization is forced by the SWFSYNC bit.

Table 14-24755. EPWM_TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

1:0	CTRMODE	R/W	3h	Counter Mode The time-base counter mode is normally configured once and not changed during normal operation If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change These bits set the time-base counter mode of operation as follows:
				`0h` `Up-count mode`
				`1h` `Down-count mode`
				`2h` `Up-down-count mode`
				`3h` `Stop-freeze counter operation (default on reset)`

14.9.4.3.2.2 EPWM_TBSTS Register

1 EPWM_TBSTS Register (Offset = 2h) [reset = 0h]

Time-Base Status Register

Return to Summary Table

Table 14-24756. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0002h**
EPWM1	**2301 0002h**
EPWM2	**2302 0002h**
EPWM3	**2303 0002h**
EPWM4	**2304 0002h**
EPWM5	**2305 0002h**
EPWM6	**2306 0002h**
EPWM7	**2307 0002h**
EPWM8	**2308 0002h**

Figure 14-8170. EPWM_TBSTS Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED1					CTRMAX	SYNCI	CTRDIR
R					R/W1TC	R/W1TC	R
0h					0h	0h	0h

Table 14-24758. EPWM_TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	CTRMAX	R/W1TC	0h	Time-Base Counter Max Latched Status Bit 0h Reading a 0h 1h Reading a 1h
1	SYNCI	R/W1TC	0h	Input Synchronization Latched Status Bit 0h Writing a 0h 1h Reading a 1h
0	CTRDIR	R	0h	Time-Base Counter Direction Status Bit At reset, the counter is frozen, therefore, this bit has no meaning To make this bit meaningful, you must first set the appropriate mode via TBCTL[CTRMODE] 0h Time-Base Counter is currently counting down 1h Time-Base Counter is currently counting up

14.9.4.3.2.3 EPWM_TBPHSHR Register

1 EPWM_TBPHSHR Register (Offset = 4h) [reset = 0h]

Time Base Phase High Resolution Register

Return to Summary Table

Table 14-24759. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0004h**
EPWM1	**2301 0004h**
EPWM2	**2302 0004h**
EPWM3	**2303 0004h**
EPWM4	**2304 0004h**
EPWM5	**2305 0004h**
EPWM6	**2306 0004h**
EPWM7	**2307 0004h**
EPWM8	**2308 0004h**

Figure 14-8171. EPWM_TBPHSHR Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TBPHSH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24761. EPWM_TBPHSHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TBPHSH	R/W	0h	Time-base phase high-resolution bits
7:0	RESERVED1	R	0h	Reserved

14.9.4.3.2.4 EPWM_TBPHS Register

1 EPWM_TBPHS Register (Offset = 6h) [reset = 0h]

Time Base Phase Register. This register is only available on ePWM instances that include the high-resolution PWM (HRPWM) extension, otherwise, this location is reserved.

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Table 14-24762. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0006h**
EPWM1	**2301 0006h**
EPWM2	**2302 0006h**
EPWM3	**2303 0006h**
EPWM4	**2304 0006h**
EPWM5	**2305 0006h**
EPWM6	**2306 0006h**
EPWM7	**2307 0006h**
EPWM8	**2308 0006h**

Figure 14-8172. EPWM_TBPHS Name Register

15	14	13	12	11	10	9	8
TBPHS							
R/W							
0h							
7	6	5	4	3	2	1	0
TBPHS							
R/W							
0h							

Table 14-24764. EPWM_TBPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBPHS	R/W	0h	These bits set time-base counter phase of the selected ePWM relative to the time-base that is supplying the synchronization input signal [a] If TBCTL[PHSEN] = 0, then the synchronization event is ignored and the time-base counter is not loaded with the phase [b] If TBCTL[PHSEN] = 1, then the time-base counter [TBCNT] will be loaded with the phase [TBPHS] when a synchronization event occurs The synchronization event can be initiated by the input synchronization signal [EPWMxSYNCI] or by a software forced synchronization

14.9.4.3.2.5 EPWM_TBCNT Register

1 EPWM_TBCNT Register (Offset = 8h) [reset = 0h]

Time Base Counter Register

Return to Summary Table

Table 14-24765. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0008h**
EPWM1	**2301 0008h**
EPWM2	**2302 0008h**
EPWM3	**2303 0008h**
EPWM4	**2304 0008h**
EPWM5	**2305 0008h**
EPWM6	**2306 0008h**
EPWM7	**2307 0008h**
EPWM8	**2308 0008h**

Figure 14-8173. EPWM_TBCNT Name Register

15	14	13	12	11	10	9	8
TBCNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBCNT							
R/W							
0h							

Table 14-24767. EPWM_TBCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBCNT	R/W	0h	Reading these bits gives the current time-base counter value Writing to these bits sets the current time-base counter value The update happens as soon as the write occurs The write is NOT synchronized to the time-base clock [TBCLK] and the register is not shadowed

14.9.4.3.2.6 EPWM_TBPRD Register

1 EPWM_TBPRD Register (Offset = Ah) [reset = 0h]

Time Base Period Register

Return to Summary Table

Table 14-24768. Instance Table

Instance Name	Physical Address
EPWM0	**2300 000Ah**
EPWM1	**2301 000Ah**
EPWM2	**2302 000Ah**
EPWM3	**2303 000Ah**
EPWM4	**2304 000Ah**
EPWM5	**2305 000Ah**
EPWM6	**2306 000Ah**
EPWM7	**2307 000Ah**
EPWM8	**2308 000Ah**

Figure 14-8174. EPWM_TBPRD Name Register

15	14	13	12	11	10	9	8
TBPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
TBPRD							
R/W							
0h							

Table 14-24770. EPWM_TBPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBPRD	R/W	0h	These bits determine the period of the time-base counter This sets the PWM frequency Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit By default this register is shadowed [a] If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the active register will be loaded from the shadow register when the time-base counter equals zero [b] If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [c] The active and shadow registers share the same memory map address

14.9.4.3.2.7 EPWM_CMPCTL Register

1 EPWM_CMPCTL Register (Offset = Eh) [reset = 0h]

Counter Compare Control Register

Return to Summary Table

Table 14-24771. Instance Table

Instance Name	Physical Address
EPWM0	**2300 000Eh**
EPWM1	**2301 000Eh**
EPWM2	**2302 000Eh**
EPWM3	**2303 000Eh**
EPWM4	**2304 000Eh**
EPWM5	**2305 000Eh**
EPWM6	**2306 000Eh**
EPWM7	**2307 000Eh**
EPWM8	**2308 000Eh**

Figure 14-8175. EPWM_CMPCTL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td>SHDWBFULL</td><td>SHDWAFULL</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED2</td><td>SHDWBMODE</td><td>RESERVED3</td><td>SHDWAMODE</td><td colspan="2">LOADBMODE</td><td colspan="2">LOADAMODE</td></tr>
<tr><td>R</td><td>R/W</td><td>R</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-24773. EPWM_CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved

9	SHDWBFULL	R	0h	Counter-compare B [CMPB] Shadow Register Full Status Flag This bit self clears once a load-strobe occurs
				`0h` `CMPB shadow FIFO not full yet`
				`1h` `Indicates the CMPB shadow FIFO is full. A CPU write will overwrite current shadow value.`

8	SHDWAFULL	R	0h	Counter-compare A [CMPA] Shadow Register Full Status Flag The flag bit is set when a 32 bit write to CMPA:CMPAHR register or a 16 bit write to CMPA register is made A 16 bit write to CMPAHR register will not affect the flag This bit self clears once a load-strobe occurs
				`0h` `CMPA shadow FIFO not full yet`
				`1h` `Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value`

7	RESERVED2	R	0h	Reserved

Table 14-24773. EPWM_CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SHDWBMODE	R/W	0h	Counter-compare B [CMPB] Register Operating Mode 0h Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register. 1h Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action.
5	RESERVED3	R	0h	Reserved
4	SHDWAMODE	R/W	0h	Counter-compare A [CMPA] Register Operating Mode 0h Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register. 1h Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action.
3:2	LOADBMODE	R/W	0h	Active Counter-Compare B [CMPB] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWBMODE] = 1] 0h Load on EPWM_TBCNT[15-0] TBCNT = 0h Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT= 0000h) 1h Load on EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD: Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD) 2h Load on either EPWM_TBCNT[15-0] TBCNT = 0 or EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD 3h Freeze (no loads possible)
1:0	LOADAMODE	R/W	0h	Active Counter-Compare A [CMPA] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWAMODE] = 1] 0h Load on TBCNT = 0h Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h) 1h Load on TBCNT = TBPRD: Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT= EPWM_TBPRD[15-0] TBPRD) 2h Load on either EPWM_TBCNT[15-0] TBCNT = 0h 3h Freeze (no loads possible)

14.9.4.3.2.8 EPWM_CMPAHR Register

1 EPWM_CMPAHR Register (Offset = 10h) [reset = 0h]

Counter Compare A High Resolution Register. This register is only available on ePWM instances that include the high-resolution PWM (HRPWM) extension; otherwise, this location is reserved.

Return to Summary Table

Table 14-24774. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0010h**
EPWM1	**2301 0010h**
EPWM2	**2302 0010h**
EPWM3	**2303 0010h**
EPWM4	**2304 0010h**
EPWM5	**2305 0010h**
EPWM6	**2306 0010h**
EPWM7	**2307 0010h**
EPWM8	**2308 0010h**

Figure 14-8176. EPWM_CMPAHR Name Register

15	14	13	12	11	10	9	8
CMPAHR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1							
R							
0h							

Table 14-24776. EPWM_CMPAHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CMPAHR	R/W	0h	Compare A High-Resolution register bits for MEP step control A minimum value of 1h is needed to enable HRPWM capabilities Valid MEP range of operation 1-255h
7:0	RESERVED1	R	0h	Reserved

14.9.4.3.2.9 EPWM_CMPA Register

1 EPWM_CMPA Register (Offset = 12h) [reset = 0h]

Counter Compare A Register

Return to Summary Table

Table 14-24777. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0012h**
EPWM1	**2301 0012h**
EPWM2	**2302 0012h**
EPWM3	**2303 0012h**
EPWM4	**2304 0012h**
EPWM5	**2305 0012h**
EPWM6	**2306 0012h**
EPWM7	**2307 0012h**
EPWM8	**2308 0012h**

Figure 14-8177. EPWM_CMPA Name Register

15	14	13	12	11	10	9	8
CMPA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPA							
R/W							
0h							

Table 14-24779. EPWM_CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPA	R/W	0h	The value in the active CMPA register is continuously compared to the time-base counter [TBCNT] When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event This event is sent to the action-qualifier where it is qualified and converted it into one or more actions These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers The actions that can be defined in the AQCTLA and AQCTLB registers include the following [a] Do nothing the event is ignored [b] Clear: Pull the EPWMxA and/or EPWMxB signal low [c] Set: Pull the EPWMxA and/or EPWMxB signal high [d] Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit By default this register is shadowed [a] If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register [b] Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full [c] If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [d] In either mode, the active and shadow registers share the same memory map address

14.9.4.3.2.10 EPWM_CMPB Register

1 EPWM_CMPB Register (Offset = 14h) [reset = 0h]

Counter Compare B Register

Return to Summary Table

Table 14-24780. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0014h**
EPWM1	**2301 0014h**
EPWM2	**2302 0014h**
EPWM3	**2303 0014h**
EPWM4	**2304 0014h**
EPWM5	**2305 0014h**
EPWM6	**2306 0014h**
EPWM7	**2307 0014h**
EPWM8	**2308 0014h**

Figure 14-8178. EPWM_CMPB Name Register

15	14	13	12	11	10	9	8
CMPB							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPB							
R/W							
0h							

Table 14-24782. EPWM_CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPB	R/W	0h	The value in the active CMPB register is continuously compared to the time-base counter [TBCNT] When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare B" event This event is sent to the action-qualifier where it is qualified and converted it into one or more actions These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers The actions that can be defined in the AQCTLA and AQCTLB registers include the following [a] Do nothing, the event is ignored [b] Clear: Pull the EPWMxA and/or EPWMxB signal low [c] Set: Pull the EPWMxA and/or EPWMxB signal high [d] Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWBMODE] bit By default this register is shadowed [a] If CMPCTL[SHDWBMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the CMPCTL[LOADBMODE] bit field determines which event will load the active register from the shadow register: [b] Before a write, the CMPCTL[SHDWBFULL] bit can be read to determine if the shadow register is currently full [c] If CMPCTL[SHDWBMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [d] In either mode, the active and shadow registers share the same memory map address

14.9.4.3.2.11 EPWM_AQCTLA Register

1 EPWM_AQCTLA Register (Offset = 16h) [reset = 0h]

Action Qualifier Control Register For Output A

Return to Summary Table

Table 14-24783. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0016h**
EPWM1	**2301 0016h**
EPWM2	**2302 0016h**
EPWM3	**2303 0016h**
EPWM4	**2304 0016h**
EPWM5	**2305 0016h**
EPWM6	**2306 0016h**
EPWM7	**2307 0016h**
EPWM8	**2308 0016h**

Figure 14-8179. EPWM_AQCTLA Name Register

15	14	13	12	11	10	9	8
RESERVED1				CBD		CBU	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-24785. EPWM_AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED1	R	0h	Reserved
11:10	CBD	R/W	0h	Action when the time-base counter equals the active CMPB register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
9:8	CBU	R/W	0h	Action when the counter equals the active CMPB register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low

Table 14-24785. EPWM_AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	CAD	R/W	0h	Action when the counter equals the active CMPA register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
5:4	CAU	R/W	0h	Action when the counter equals the active CMPA register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
3:2	PRD	R/W	0h	Action when the counter equals the period Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
1:0	ZRO	R/W	0h	Action when counter equals zero Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low

14.9.4.3.2.12 EPWM_AQCTLB Register

1 EPWM_AQCTLB Register (Offset = 18h) [reset = 0h]

Action Qualifier Control Register For Output B

Return to Summary Table

Table 14-24786. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0018h**
EPWM1	**2301 0018h**
EPWM2	**2302 0018h**
EPWM3	**2303 0018h**
EPWM4	**2304 0018h**
EPWM5	**2305 0018h**
EPWM6	**2306 0018h**
EPWM7	**2307 0018h**
EPWM8	**2308 0018h**

Figure 14-8180. EPWM_AQCTLB Name Register

15	14	13	12	11	10	9	8
RESERVED1				CBD		CBU	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-24788. EPWM_AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED1	R	0h	Reserved

11:10	CBD	R/W	0h	Action when the counter equals the active CMPB register and the counter is decrementing
				`0h Do nothing (action disabled)`
				`1h Clear: force EPWMxB output low`
				`2h Set: force EPWMxB output high`
				`3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low`

9:8	CBU	R/W	0h	Action when the counter equals the active CMPB register and the counter is incrementing
				`0h Do nothing (action disabled)`
				`1h Clear: force EPWMxB output low`
				`2h Set: force EPWMxB output high`
				`3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low`

Table 14-24788. EPWM_AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	CAD	R/W	0h	Action when the counter equals the active CMPA register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
5:4	CAU	R/W	0h	Action when the counter equals the active CMPA register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
3:2	PRD	R/W	0h	Action when the counter equals the period Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
1:0	ZRO	R/W	0h	Action when counter equals zero Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low

14.9.4.3.2.13 EPWM_AQSFRC Register

1 EPWM_AQSFRC Register (Offset = 1Ah) [reset = 0h]

Action Qualifier Software Force Register

Return to Summary Table

Table 14-24789. Instance Table

Instance Name	Physical Address
EPWM0	**2300 001Ah**
EPWM1	**2301 001Ah**
EPWM2	**2302 001Ah**
EPWM3	**2303 001Ah**
EPWM4	**2304 001Ah**
EPWM5	**2305 001Ah**
EPWM6	**2306 001Ah**
EPWM7	**2307 001Ah**
EPWM8	**2308 001Ah**

Figure 14-8181. EPWM_AQSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RLDCSF		OTSFB	ACTSFB		OTSFA	ACTSFA	
R/W		R/W1TC	R/W		R/W1TC	R/W	
0h		0h	0h		0h	0h	

Table 14-24791. EPWM_AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED1	R	0h	Reserved
7:6	RLDCSF	R/W	0h	AQCSFRC Active Register Reload From Shadow Options
5	OTSFB	R/W1TC	0h	One-Time Software Forced Event on Output B 0h Writing a 0h (1h Initiates a single s/w forced event
4:3	ACTSFB	R/W	0h	Action when One-Time Software Force B Is invoked 0h Does nothing (action disabled) 1h Clear (low) 2h Set (high) 3h Toggle (Low -> High, High -> Low).
2	OTSFA	R/W1TC	0h	One-Time Software Forced Event on Output A 0h Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (that is, a forced event is initiated). 1h Initiates a single software forced event.
1:0	ACTSFA	R/W	0h	Action When One-Time Software Force A Is Invoked 0h Does nothing (action disabled). 1h Clear (low). 2h Set (high). 3h Toggle (Low -> High, High -> Low).

14.9.4.3.2.14 EPWM_AQCSFRC Register

1 EPWM_AQCSFRC Register (Offset = 1Ch) [reset = 0h]

Action Qualifier Continuous S/W Force Register

Return to Summary Table

Table 14-24792. Instance Table

Instance Name	Physical Address
EPWM0	**2300 001Ch**
EPWM1	**2301 001Ch**
EPWM2	**2302 001Ch**
EPWM3	**2303 001Ch**
EPWM4	**2304 001Ch**
EPWM5	**2305 001Ch**
EPWM6	**2306 001Ch**
EPWM7	**2307 001Ch**
EPWM8	**2308 001Ch**

Figure 14-8182. EPWM_AQCSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				CSFB		CSFA	
R				R/W		R/W	
0h				0h		0h	

Table 14-24794. EPWM_AQCSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved
3:2	CSFB	R/W	0h	Continuous Software Force on Output B In immediate mode, a continuous force takes effect on the next TBCLK edge In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register To configure shadow mode, use AQSFRC[RLDCSF] 0h Forcing disabled, that is, has no effect 1h Forces a continuous low on output B 2h Forces a continuous high on output B 3h Software forcing is disabled and has no effect
1:0	CSFA	R/W	0h	Continuous Software Force on Output A In immediate mode, a continuous force takes effect on the next TBCLK edge In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register 0h Forcing disabled, that is, has no effect 1h Forces a continuous low on output A 2h Forces a continuous high on output A 3h Software forcing is disabled and has no effect

14.9.4.3.2.15 EPWM_DBCTL Register

1 EPWM_DBCTL Register (Offset = 1Eh) [reset = 0h]

Dead-Band Generator Control Register

Return to Summary Table

Table 14-24795. Instance Table

Instance Name	Physical Address
EPWM0	**2300 001Eh**
EPWM1	**2301 001Eh**
EPWM2	**2302 001Eh**
EPWM3	**2303 001Eh**
EPWM4	**2304 001Eh**
EPWM5	**2305 001Eh**
EPWM6	**2306 001Eh**
EPWM7	**2307 001Eh**
EPWM8	**2308 001Eh**

Figure 14-8183. EPWM_DBCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1		IN_MODE		POLSEL		OUT_MODE	
R		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-24797. EPWM_DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED1	R	0h	Reserved
5:4	IN_MODE	R/W	0h	Dead Band Input Mode Control Bit 5 controls the S5 switch and bit 4 controls the S4 switch This allows you to select the input source to the falling-edge and rising-edge delay To produce classical dead-band waveforms, the default is EPWMxA In is the source for both falling and rising-edge delays 0h `EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay.` 1h `EPWMxB In (from the action-qualifier) is the source for rising- edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal.` 2h `EPWMxA In (from the action-qualifier) is the source for rising- edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal.` 3h `EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.`

Table 14-24797. EPWM_DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	POLSEL	R/W	0h	Polarity Select Control Bit 3 controls the S3 switch and bit 2 controls the S2 switch This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0,0 Other enhanced modes are also possible, but not regarded as typical usage modes 0h `Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default).` 1h `Active low complementary (ALC) mode. EPWMxA is inverted.` 2h `Active high complementary (AHC). EPWMxB is inverted.` 3h `Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.`
1:0	OUT_MODE	R/W	0h	Dead-band Output Mode Control Bit 1 controls the S1 switch and bit 0 controls the S0 switch This allows you to selectively enable or bypass the dead-band generation for the falling-edge and rising-edge delay 0h `Dead-band generation is bypassed for both output signals. In this mode, both the EPWMxA and EPWMxB output signals from the action-qualifier are passed directly to the PWM-chopper submodule. In this mode, the POLSEL and IN_MODE bits have no effect.` 1h `Disable rising-edge delay. The EPWMxA signal from the action- qualifier is passed straight through to the EPWMxA input of the PWM-chopper submodule. The falling-edge delayed signal is seen on output EPWMxB. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field.` 2h `Disable falling-edge delay. The EPWMxB signal from the action- qualifier is passed straight through to the EPWMxB input of the PWM-chopper submodule. The rising-edge delayed signal is seen on output EPWMxA. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field.` 3h `Dead-band is fully enabled for both rising-edge delay on output EPWMxA and falling-edge delay on output EPWMxB. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field.`

14.9.4.3.2.16 EPWM_DBRED Register

1 EPWM_DBRED Register (Offset = 20h) [reset = 0h]

Dead-Band Generator Rising Edge Delay Count Register

Return to Summary Table

Table 14-24798. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0020h**
EPWM1	**2301 0020h**
EPWM2	**2302 0020h**
EPWM3	**2303 0020h**
EPWM4	**2304 0020h**
EPWM5	**2305 0020h**
EPWM6	**2306 0020h**
EPWM7	**2307 0020h**
EPWM8	**2308 0020h**

Figure 14-8184. EPWM_DBRED Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td colspan="2">DEL</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24800. EPWM_DBRED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved
9:0	DEL	R/W	0h	Rising Edge Delay Count 10 bit counter

14.9.4.3.2.17 EPWM_DBFED Register

1 EPWM_DBFED Register (Offset = 22h) [reset = 0h]

Dead-Band Generator Falling Edge Delay Count Register

Return to Summary Table

Table 14-24801. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0022h**
EPWM1	**2301 0022h**
EPWM2	**2302 0022h**
EPWM3	**2303 0022h**
EPWM4	**2304 0022h**
EPWM5	**2305 0022h**
EPWM6	**2306 0022h**
EPWM7	**2307 0022h**
EPWM8	**2308 0022h**

Figure 14-8185. EPWM_DBFED Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td colspan="2">DEL</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24803. EPWM_DBFED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved
9:0	DEL	R/W	0h	Falling Edge Delay Count 10 bit counter

14.9.4.3.2.18 EPWM_TZSEL Register

1 EPWM_TZSEL Register (Offset = 24h) [reset = 0h]

Trip Zone Select Register

Return to Summary Table

Table 14-24804. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0024h**
EPWM1	**2301 0024h**
EPWM2	**2302 0024h**
EPWM3	**2303 0024h**
EPWM4	**2304 0024h**
EPWM5	**2305 0024h**
EPWM6	**2306 0024h**
EPWM7	**2307 0024h**
EPWM8	**2308 0024h**

Figure 14-8186. EPWM_TZSEL Name Register

15	14	13	12	11	10	9	8
OSHTN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CBCN							
R/W							
0h							

Table 14-24806. EPWM_TZSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OSHTN	R/W	0h	Trip-zone n [TZn] select One-Shot [OSHT] trip-zone enable/disable When any of the enabled pins go low, a one-shot trip event occurs for this ePWM module When the event occurs, the action defined in the TZCTL register is taken on the EPWMxA and EPWMxB outputs The one-shot trip condition remains latched until you clear the condition via the TZCLR register 0h `Disable TZn as a one-shot trip source for this EPWM module` 1h `Enable TZn as a one-shot trip source for this EPWM module`
7:0	CBCN	R/W	0h	Trip-zone n [TZn] select Cycle-by-Cycle [CBC] trip-zone enable/disable When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this ePWM module When the event occurs, the action defined in the TZCTL register is taken on the EPWMxA and EPWMxB outputs A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero 0h `Disable TZn as a CBC trip source for this EPWM module` 1h `Enable TZn as a CBC trip source for this EPWM module`

14.9.4.3.2.19 EPWM_TZCTL Register

1 EPWM_TZCTL Register (Offset = 28h) [reset = 0h]

Trip Zone Control Register

Return to Summary Table

Table 14-24807. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0028h**
EPWM1	**2301 0028h**
EPWM2	**2302 0028h**
EPWM3	**2303 0028h**
EPWM4	**2304 0028h**
EPWM5	**2305 0028h**
EPWM6	**2306 0028h**
EPWM7	**2307 0028h**
EPWM8	**2308 0028h**

Figure 14-8187. EPWM_TZCTL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td colspan="2">TZB</td><td colspan="2">TZA</td></tr>
<tr><td colspan="4">R</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-24809. EPWM_TZCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved

3:2	TZB	R/W	0h	When a trip event occurs the following action is taken on output EPWMxB Which trip-zone pins can cause an event is defined in the TZSEL register
				`0h` `High impedance (EPWMxB = High-impedance state)`
				`1h` `Force EPWMxB to a high state`
				`2h` `Force EPWMxB to a low state`
				`3h` `Do nothing, no action is taken on EPWMxB.`

1:0	TZA	R/W	0h	When a trip event occurs the following action is taken on output EPWMxA Which trip-zone pins can cause an event is defined in the TZSEL register
				`0h` `High impedance (EPWMxA = High-impedance state)`
				`1h` `Force EPWMxA to a high state`
				`2h` `Force EPWMxA to a low state`
				`3h` `Do nothing, no action is taken on EPWMxA.`

14.9.4.3.2.20 EPWM_TZEINT Register

1 EPWM_TZEINT Register (Offset = 2Ah) [reset = 0h]

Trip Zone Enable Interrupt Register

Return to Summary Table

Table 14-24810. Instance Table

Instance Name	Physical Address
EPWM0	**2300 002Ah**
EPWM1	**2301 002Ah**
EPWM2	**2302 002Ah**
EPWM3	**2303 002Ah**
EPWM4	**2304 002Ah**
EPWM5	**2305 002Ah**
EPWM6	**2306 002Ah**
EPWM7	**2307 002Ah**
EPWM8	**2308 002Ah**

Figure 14-8188. EPWM_TZEINT Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1					OST	CBC	RESERVED2
R					R/W	R/W	R
0h					0h	0h	0h

Table 14-24812. EPWM_TZEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R/W	0h	Trip-zone One-Shot Interrupt Enable 0h Disable one-shot interrupt generation 1h Enable Interrupt generation a one-shot trip event will cause a EPWMxTZINT interrupt.
1	CBC	R/W	0h	Trip-zone Cycle-by-Cycle Interrupt Enable 0h Disable cycle-by-cycle interrupt generation 1h Enable interrupt generation a cycle-by-cycle trip event will cause an EPWMxTZINT interrupt.
0	RESERVED2	R	0h	Reserved

14.9.4.3.2.21 EPWM_TZFLG Register

1 EPWM_TZFLG Register (Offset = 2Ch) [reset = 0h]

Trip Zone Flag Register

Return to Summary Table

Table 14-24813. Instance Table

Instance Name	Physical Address
EPWM0	**2300 002Ch**
EPWM1	**2301 002Ch**
EPWM2	**2302 002Ch**
EPWM3	**2303 002Ch**
EPWM4	**2304 002Ch**
EPWM5	**2305 002Ch**
EPWM6	**2306 002Ch**
EPWM7	**2307 002Ch**
EPWM8	**2308 002Ch**

Figure 14-8189. EPWM_TZFLG Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1					OST	CBC	INT
R					R	R	R
0h					0h	0h	0h

Table 14-24815. EPWM_TZFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R	0h	Latched Status Flag for A One-Shot Trip Event 0h `No one-shot trip event has occurred` 1h `Indicates a trip event has occurred on a pin selected as a one-shot trip source. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register.`
1	CBC	R	0h	Latched Status Flag for Cycle-By-Cycle Trip Event 0h `No cycle-by-cycle trip event has occurred` 1h `Indicates a trip event has occurred on a pin selected as a cycle-by-cycle trip source. The EPWM_TZFLG[1] CBC bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the pins is automatically cleared when the EPWM time-base counter reaches zero (EPWM_TBCNT[15-0] TBCNT = 0000h)`

Table 14-24815. EPWM_TZFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R	0h	Latched Trip Interrupt Status Flag 0h Indicates no interrupt has been generated 1h Indicates an EPWMxTZINT interrupt was generated because of a trip condition. No further EPWMxTZINT interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register.

14.9.4.3.2.22 EPWM_TZCLR Register

1 EPWM_TZCLR Register (Offset = 2Eh) [reset = 0h]

Trip Zone Clear Register

Return to Summary Table

Table 14-24816. Instance Table

Instance Name	Physical Address
EPWM0	**2300 002Eh**
EPWM1	**2301 002Eh**
EPWM2	**2302 002Eh**
EPWM3	**2303 002Eh**
EPWM4	**2304 002Eh**
EPWM5	**2305 002Eh**
EPWM6	**2306 002Eh**
EPWM7	**2307 002Eh**
EPWM8	**2308 002Eh**

Figure 14-8190. EPWM_TZCLR Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1					OST	CBC	INT
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-24818. EPWM_TZCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved

2	OST	R/W	0h	Clear Flag for One-Shot Trip [OST] Latch
				`0h Has no effect. Always reads back a 0h`
				`1h Clears this Trip (set) condition`

1	CBC	R/W	0h	Clear Flag for Cycle-By-Cycle [CBC] Trip Latch
				`0h Has no effect. Always reads back a 0h`
				`1h Clears this Trip (set) condition`

0	INT	R/W	0h	Global Interrupt Clear Flag
				`0h Has no effect. Always reads back a 0h`
				`1h Clears the trip-interrupt flag for this EPWM module (EPWM_TZFLG[0] INT)`

14.9.4.3.2.23 EPWM_TZFRC Register

1 EPWM_TZFRC Register (Offset = 30h) [reset = 0h]

Trip Zone Force Register

Return to Summary Table

Table 14-24819. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0030h**
EPWM1	**2301 0030h**
EPWM2	**2302 0030h**
EPWM3	**2303 0030h**
EPWM4	**2304 0030h**
EPWM5	**2305 0030h**
EPWM6	**2306 0030h**
EPWM7	**2307 0030h**
EPWM8	**2308 0030h**

Figure 14-8191. EPWM_TZFRC Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED1</td><td>OST</td><td>CBC</td><td>RESERVED2</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-24821. EPWM_TZFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R/W	0h	Force a One-Shot Trip Event via Software 0h writing of 0h 1h Forces a one-shot trip event and sets the EPWM_TZFLG[2] OST bit.
1	CBC	R/W	0h	Force a Cycle-by-Cycle Trip Event via Software 0h writing of 0h 1h Forces a cycle-by-cycle trip event and sets the EPWM_TZFLG[1] CBC bit.
0	RESERVED2	R	0h	Reserved

14.9.4.3.2.24 EPWM_ETSEL Register

1 EPWM_ETSEL Register (Offset = 32h) [reset = 0h]

Event Trigger Selection Register

Return to Summary Table

Table 14-24822. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0032h**
EPWM1	**2301 0032h**
EPWM2	**2302 0032h**
EPWM3	**2303 0032h**
EPWM4	**2304 0032h**
EPWM5	**2305 0032h**
EPWM6	**2306 0032h**
EPWM7	**2307 0032h**
EPWM8	**2308 0032h**

Figure 14-8192. EPWM_ETSEL Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				INTEN	INTSEL		
R				R/W	R/W		
0h				0h	0h		

Table 14-24824. EPWM_ETSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved
3	INTEN	R/W	0h	Enable ePWM Interrupt [EPWMx_INT] Generation 0h Disable EPWMx_INT generation 1h Enable EPWMx_INT generation
2:0	INTSEL	R/W	0h	ePWM Interrupt [EPWMx_INT] Selection Options 0h Reserved 1h Enable event time-base counter equal to zero. (EPWM_TBCNT = 0000h) 2h Enable event time-base counter equal to period (EPWM_TBCNT = EPWM_TBPRD) 3h Reserved 4h Enable event time-base counter equal to CMPA when the timer is incrementing 5h Enable event time-base counter equal to CMPA when the timer is decrementing 6h Enable event time-base counter equal to CMPB when the timer is incrementing 7h Enable event time-base counter equal to CMPB when the timer is decrementing

14.9.4.3.2.25 EPWM_ETPS Register

1 EPWM_ETPS Register (Offset = 34h) [reset = 0h]

Event Trigger Pre-Scale Register

Return to Summary Table

Table 14-24825. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0034h**
EPWM1	**2301 0034h**
EPWM2	**2302 0034h**
EPWM3	**2303 0034h**
EPWM4	**2304 0034h**
EPWM5	**2305 0034h**
EPWM6	**2306 0034h**
EPWM7	**2307 0034h**
EPWM8	**2308 0034h**

Figure 14-8193. EPWM_ETPS Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td colspan="2">INTCNT</td><td colspan="2">INTPRD</td></tr>
<tr><td colspan="4">R</td><td colspan="2">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-24827. EPWM_ETPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved
3:2	INTCNT	R	0h	ePWM Interrupt Event [EPWMx_INT] Counter Register These bits indicate how many selected ETSEL[INTSEL] events have occurred These bits are automatically cleared when an interrupt pulse is generated If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD] 0h No events have occurred 1h 1 event has occurred 2h 2 events have occurred 3h 3 events have occurred

Table 14-24827. EPWM_ETPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	INTPRD	R/W	0h	ePWM Interrupt [EPWMx_INT] Period Select These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated To be generated, the interrupt must be enabled [ETSEL[INT] = 1] If the interrupt status flag is set from a previous interrupt [ETFLG[INT] = 1] then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit This allows for one interrupt to be pending while another is still being serviced Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear Writing a INTPRD value that is less than the current counter value will result in an undefined state If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented 0h Disable the interrupt event counter. No interrupt will be generated and the EPWM_ETFRC[0] INT bit is ignored. 1h Generate an interrupt on the first event INTCNT = 0b01 (first event) 2h Generate interrupt on the EPWM_ETPS[3-2] INTCNT = 0b10 (second event) 3h Generate interrupt on the EPWM_ETPS[3-2] INTCNT = 0b11 (third event)

14.9.4.3.2.26 EPWM_ETFLG Register

1 EPWM_ETFLG Register (Offset = 36h) [reset = 0h]

Event Trigger Flag Register

Return to Summary Table

Table 14-24828. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0036h**
EPWM1	**2301 0036h**
EPWM2	**2302 0036h**
EPWM3	**2303 0036h**
EPWM4	**2304 0036h**
EPWM5	**2305 0036h**
EPWM6	**2306 0036h**
EPWM7	**2307 0036h**
EPWM8	**2308 0036h**

Figure 14-8194. EPWM_ETFLG Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED1</td><td>INT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-24830. EPWM_ETFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved
0	INT	R	0h	Latched ePWM Interrupt [EPWMx_INT] Status Flag 0h Indicates no event occurred. 1h Indicates that an EPWMx interrupt (EWPMx_INT) was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the EPWM_ETFLG[0] INT bit is still set. If an interrupt is pending, it will not be generated until after the EPWM_ETFLG[0] INT bit is cleared.

14.9.4.3.2.27 EPWM_ETCLR Register

1 EPWM_ETCLR Register (Offset = 38h) [reset = 0h]

Event Trigger Clear Register

Return to Summary Table

Table 14-24831. Instance Table

Instance Name	Physical Address
EPWM0	**2300 0038h**
EPWM1	**2301 0038h**
EPWM2	**2302 0038h**
EPWM3	**2303 0038h**
EPWM4	**2304 0038h**
EPWM5	**2305 0038h**
EPWM6	**2306 0038h**
EPWM7	**2307 0038h**
EPWM8	**2308 0038h**

Figure 14-8195. EPWM_ETCLR Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED1</td><td>INT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-24833. EPWM_ETCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved
0	INT	R	0h	ePWM Interrupt [EPWMx_INT] Flag Clear Bit

14.9.4.3.2.28 EPWM_ETFRC Register

1 EPWM_ETFRC Register (Offset = 3Ah) [reset = 0h]

Event Trigger Force Register

Return to Summary Table

Table 14-24834. Instance Table

Instance Name	Physical Address
EPWM0	**2300 003Ah**
EPWM1	**2301 003Ah**
EPWM2	**2302 003Ah**
EPWM3	**2303 003Ah**
EPWM4	**2304 003Ah**
EPWM5	**2305 003Ah**
EPWM6	**2306 003Ah**
EPWM7	**2307 003Ah**
EPWM8	**2308 003Ah**

Figure 14-8196. EPWM_ETFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1							INT
R							R
0h							0h

Table 14-24836. EPWM_ETFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved
0	INT	R	0h	INT Force Bit The interrupt will only be generated if the event is enabled in the ETSEL register The INT flag bit will be set regardless 0h `Writing a 0 has no effect. Always reads back a 0h` 1h `Writing 1 clears the EPWM_ETFLG[0] INT flag bit and enable further interrupts pulses to be generated.`

14.9.4.3.2.29 EPWM_PCCTL Register

1 EPWM_PCCTL Register (Offset = 3Ch) [reset = 0h]

PWM Chopper Control Register

Return to Summary Table

Table 14-24837. Instance Table

Instance Name	Physical Address
EPWM0	**2300 003Ch**
EPWM1	**2301 003Ch**
EPWM2	**2302 003Ch**
EPWM3	**2303 003Ch**
EPWM4	**2304 003Ch**
EPWM5	**2305 003Ch**
EPWM6	**2306 003Ch**
EPWM7	**2307 003Ch**
EPWM8	**2308 003Ch**

Figure 14-8197. EPWM_PCCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1					CHPDUTY		
R					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHPFREQ			OSHTWTH				CHPEN
R/W			R/W				R/W
0h			0h				0h

Table 14-24839. EPWM_PCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED1	R	0h	Reserved
10:8	CHPDUTY	R/W	0h	Chopping Clock Duty Cycle 0h Duty = 1/8 (12.5%) 1h Duty = 2/8 (25.0%) 2h Duty = 3/8 (37.5%) 3h Duty = 4/8 (50.0%) 4h Duty = 5/8 (62.5%) 5h Duty = 6/8 (75.0%) 6h Duty = 7/8 (87.5%) 7h Reserved
7:5	CHPFREQ	R/W	0h	Chopping Clock Frequency 0h Divide by 1 (no prescale) 1h Divide by 2 2h Divide by 3 3h Divide by 4 4h Divide by 5 5h Divide by 6 6h Divide by 7 7h Divide by 8
4:1	OSHTWTH	R/W	0h	One-Shot Pulse Width 0h 1 - SYSCLKOUT/8 wide 1h 2 - SYSCLKOUT/8 wide 2h 3 - SYSCLKOUT/8 wide 3h 4 - SYSCLKOUT/8 wide 3h 4 - SYSCLKOUT/8 wide

Table 14-24839. EPWM_PCCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CHPEN	R/W	0h	PWM-chopping Enable 0h Disable (bypass) PWM chopping function 1h Enable chopping function

14.9.4.3.2.30 EPWM_PID Register

1 EPWM_PID Register (Offset = 5Ch) [reset = 44D10903h]

EHRPWM Peripheral ID Register. The IP revision register is used by software to track features, bugs, and compatibility.

Return to Summary Table

Table 14-24840. Instance Table

Instance Name	Physical Address
EPWM0	**2300 005Ch**
EPWM1	**2301 005Ch**
EPWM2	**2302 005Ch**
EPWM3	**2303 005Ch**
EPWM4	**2304 005Ch**
EPWM5	**2305 005Ch**
EPWM6	**2306 005Ch**
EPWM7	**2307 005Ch**
EPWM8	**2308 005Ch**

Figure 14-8198. EPWM_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED1		FUNC			
R		R		R			
1h		0h		4D1h			

23	22	21	20	19	18	17	16
FUNC							
R							
4D1h							

15	14	13	12	11	10	9	8
R_RTL					X_MAJOR		
R					R		
1h					1h		

7	6	5	4	3	2	1	0
CUSTOM		Y_MINOR					
R		R					
0h		3h					

Table 14-24842. EPWM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between the old scheme and current
29:28	RESERVED1	R	0h	Reserved
27:16	FUNC	R	4D1h	FUNC
15:11	R_RTL	R	1h	RTL version [R], maintained by IP design owner
10:8	X_MAJOR	R	1h	Major revision [X]
7:6	CUSTOM	R	0h	CUSTOM
5:0	Y_MINOR	R	3h	Minor revision [Y]

14.9.4.4 EQEP

EQEP

14.9.4.4.1 EQEP Summaries

EQEP Summaries

Table 14-24843. EQEP Registers, Base Address=2320 0000h, Length=256

Offset	Length	Register Name	EQEP0 Physical Address	EQEP1 Physical Address	EQEP2 Physical Address
0h	32	EQEP_QPOSCNT	2320 0000h	2321 0000h	2322 0000h
4h	32	EQEP_QPOSINIT	2320 0004h	2321 0004h	2322 0004h
8h	32	EQEP_QPOSMAX	2320 0008h	2321 0008h	2322 0008h
Ch	32	EQEP_QPOSCMP	2320 000Ch	2321 000Ch	2322 000Ch
10h	32	EQEP_QPOSILAT	2320 0010h	2321 0010h	2322 0010h
14h	32	EQEP_QPOSSLAT	2320 0014h	2321 0014h	2322 0014h
18h	32	EQEP_QPOSLAT	2320 0018h	2321 0018h	2322 0018h
1Ch	32	EQEP_QUTMR	2320 001Ch	2321 001Ch	2322 001Ch
20h	32	EQEP_QUPRD	2320 0020h	2321 0020h	2322 0020h
24h	16	EQEP_QWDTMR	2320 0024h	2321 0024h	2322 0024h
26h	16	EQEP_QWDPRD	2320 0026h	2321 0026h	2322 0026h
28h	16	EQEP_QDECCTL_TYPE2	2320 0028h	2321 0028h	2322 0028h
2Ah	16	EQEP_QEPCTL	2320 002Ah	2321 002Ah	2322 002Ah
2Ch	16	EQEP_QCAPCTL	2320 002Ch	2321 002Ch	2322 002Ch
2Eh	16	EQEP_QPOSCTL	2320 002Eh	2321 002Eh	2322 002Eh
30h	16	EQEP_QEINT_TYPE1	2320 0030h	2321 0030h	2322 0030h
32h	16	EQEP_QFLG_TYPE1	2320 0032h	2321 0032h	2322 0032h
34h	16	EQEP_QCLR_TYPE1	2320 0034h	2321 0034h	2322 0034h
36h	16	EQEP_QFRC_TYPE1	2320 0036h	2321 0036h	2322 0036h
38h	16	EQEP_QEPSTS_TYPE1	2320 0038h	2321 0038h	2322 0038h
3Ah	16	EQEP_QCTMR	2320 003Ah	2321 003Ah	2322 003Ah
3Ch	16	EQEP_QCPRD	2320 003Ch	2321 003Ch	2322 003Ch
3Eh	16	EQEP_QCTMRLAT	2320 003Eh	2321 003Eh	2322 003Eh
40h	16	EQEP_QCPRDLAT	2320 0040h	2321 0040h	2322 0040h
42h	16	EQEP_RESERVED_1_J	2320 0042h + formula	2321 0042h + formula	2322 0042h + formula
5Ch	32	EQEP_PID	2320 005Ch	2321 005Ch	2322 005Ch
60h	32	EQEP_REV_TYPE2	2320 0060h	2321 0060h	2322 0060h
64h	32	EQEP_QEPSTROBESEL	2320 0064h	2321 0064h	2322 0064h
68h	32	EQEP_QMACTRL	2320 0068h	2321 0068h	2322 0068h
6Ch	32	EQEP_QEPSRCSEL	2320 006Ch	2321 006Ch	2322 006Ch
70h	16	EQEP_RESERVED_2_J	2320 0070h + formula	2321 0070h + formula	2322 0070h + formula

14.9.4.4.2 EQEP Registers

EQEP Registers

14.9.4.4.2.1 EQEP_QPOSCNT Register

1 EQEP_QPOSCNT Register (Offset = 0h) [reset = 0h]

Position Counter

Return to Summary Table

Table 14-24844. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0000h**
EQEP1	**2321 0000h**
EQEP2	**2322 0000h**

Figure 14-8199. EQEP_QPOSCNT Name Register

31	30	29	28	27	26	25	24
QPOSCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSCNT							
R/W							
0h							

Table 14-24846. EQEP_QPOSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSCNT	R/W	0h	Position Counter This 32-bit position counter register counts up/down on every eQEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. This Register acts as a Read ONLY register while counter is counting up/down. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.2 EQEP_QPOSINIT Register

1 EQEP_QPOSINIT Register (Offset = 4h) [reset = 0h]

Position Counter Init

Return to Summary Table

Table 14-24847. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0004h**
EQEP1	**2321 0004h**
EQEP2	**2322 0004h**

Figure 14-8200. EQEP_QPOSINIT Name Register

31	30	29	28	27	26	25	24
QPOSINIT							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSINIT							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSINIT							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSINIT							
R/W							
0h							

Table 14-24849. EQEP_QPOSINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSINIT	R/W	0h	Position Counter Init This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.3 EQEP_QPOSMAX Register

1 EQEP_QPOSMAX Register (Offset = 8h) [reset = 0h]

Maximum Position Count

Return to Summary Table

Table 14-24850. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0008h**
EQEP1	**2321 0008h**
EQEP2	**2322 0008h**

Figure 14-8201. EQEP_QPOSMAX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">QPOSMAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">QPOSMAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">QPOSMAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">QPOSMAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24852. EQEP_QPOSMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSMAX	R/W	0h	Maximum Position Count This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.4 EQEP_QPOSCMP Register

1 EQEP_QPOSCMP Register (Offset = Ch) [reset = 0h]

Position Compare

Return to Summary Table

Table 14-24853. Instance Table

Instance Name	Physical Address
EQEP0	**2320 000Ch**
EQEP1	**2321 000Ch**
EQEP2	**2322 000Ch**

Figure 14-8202. EQEP_QPOSCMP Name Register

31	30	29	28	27	26	25	24
QPOSCMP							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSCMP							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSCMP							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSCMP							
R/W							
0h							

Table 14-24855. EQEP_QPOSCMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSCMP	R/W	0h	Position Compare The position-compare value in this register is compared with the position counter [QPOSCNT] to generate sync output and/or interrupt on compare match. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.5 EQEP_QPOSILAT Register

1 EQEP_QPOSILAT Register (Offset = 10h) [reset = 0h]

Index Position Latch

Return to Summary Table

Table 14-24856. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0010h**
EQEP1	**2321 0010h**
EQEP2	**2322 0010h**

Figure 14-8203. EQEP_QPOSILAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">QPOSILAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">QPOSILAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">QPOSILAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">QPOSILAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24858. EQEP_QPOSILAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSILAT	R	0h	Index Position Latch The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.6 EQEP_QPOSSLAT Register

1 EQEP_QPOSSLAT Register (Offset = 14h) [reset = 0h]

Strobe Position Latch

Return to Summary Table

Table 14-24859. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0014h**
EQEP1	**2321 0014h**
EQEP2	**2322 0014h**

Figure 14-8204. EQEP_QPOSSLAT Name Register

31	30	29	28	27	26	25	24
QPOSSLAT							
R							
0h							
23	22	21	20	19	18	17	16
QPOSSLAT							
R							
0h							
15	14	13	12	11	10	9	8
QPOSSLAT							
R							
0h							
7	6	5	4	3	2	1	0
QPOSSLAT							
R							
0h							

Table 14-24861. EQEP_QPOSSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSSLAT	R	0h	Strobe Position Latch The position-counter value is latched into this register on a strobe event as defined by the QEPCTL[SEL] bits. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.7 EQEP_QPOSLAT Register

1 EQEP_QPOSLAT Register (Offset = 18h) [reset = 0h]

Position Latch

Return to Summary Table

Table 14-24862. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0018h**
EQEP1	**2321 0018h**
EQEP2	**2322 0018h**

Figure 14-8205. EQEP_QPOSLAT Name Register

31	30	29	28	27	26	25	24
QPOSLAT							
R							
0h							
23	22	21	20	19	18	17	16
QPOSLAT							
R							
0h							
15	14	13	12	11	10	9	8
QPOSLAT							
R							
0h							
7	6	5	4	3	2	1	0
QPOSLAT							
R							
0h							

Table 14-24864. EQEP_QPOSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSLAT	R	0h	Position Latch The position-counter value is latched into this register on a unit time out event. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.8 EQEP_QUTMR Register

1 EQEP_QUTMR Register (Offset = 1Ch) [reset = 0h]

QEP Unit Timer

Return to Summary Table

Table 14-24865. Instance Table

Instance Name	Physical Address
EQEP0	**2320 001Ch**
EQEP1	**2321 001Ch**
EQEP2	**2322 001Ch**

Figure 14-8206. EQEP_QUTMR Name Register

31	30	29	28	27	26	25	24
QUTMR							
R/W							
0h							
23	22	21	20	19	18	17	16
QUTMR							
R/W							
0h							
15	14	13	12	11	10	9	8
QUTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QUTMR							
R/W							
0h							

Table 14-24867. EQEP_QUTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUTMR	R/W	0h	QEP Unit Timer This register acts as time base for unit time event generation. When this timer value matches the unit time period value a unit time event is generated. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.9 EQEP_QUPRD Register

1 EQEP_QUPRD Register (Offset = 20h) [reset = 0h]

QEP Unit Period

Return to Summary Table

Table 14-24868. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0020h**
EQEP1	**2321 0020h**
EQEP2	**2322 0020h**

Figure 14-8207. EQEP_QUPRD Name Register

31	30	29	28	27	26	25	24
QUPRD							
R/W							
0h							
23	22	21	20	19	18	17	16
QUPRD							
R/W							
0h							
15	14	13	12	11	10	9	8
QUPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
QUPRD							
R/W							
0h							

Table 14-24870. EQEP_QUPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUPRD	R/W	0h	QEP Unit Period This register contains the period count for the unit timer to generate periodic unit time events. These events latch the eQEP position information at periodic intervals and optionally generate an interrupt. Writes to this register should always be full 32-bit writes. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.10 EQEP_QWDTMR Register

1 EQEP_QWDTMR Register (Offset = 24h) [reset = 0h]

QEP Watchdog Timer

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Table 14-24871. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0024h**
EQEP1	**2321 0024h**
EQEP2	**2322 0024h**

Figure 14-8208. EQEP_QWDTMR Name Register

15	14	13	12	11	10	9	8
QWDTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QWDTMR							
R/W							
0h							

Table 14-24873. EQEP_QWDTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QWDTMR	R/W	0h	QEP Watchdog Timer This register acts as time base for the watchdog to detect motor stalls. When this timer value matches with the watchdog's period value a watchdog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.11 EQEP_QWDPRD Register

1 EQEP_QWDPRD Register (Offset = 26h) [reset = 0h]

QEP Watchdog Period

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Table 14-24874. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0026h**
EQEP1	**2321 0026h**
EQEP2	**2322 0026h**

Figure 14-8209. EQEP_QWDPRD Name Register

15	14	13	12	11	10	9	8
QWDPRD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QWDPRD							
R/W							
0h							

Table 14-24876. EQEP_QWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QWDPRD	R/W	0h	QEP Watchdog Period This register contains the time-out count for the eQEP peripheral watch dog timer. When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.12 EQEP_QDECCTL_TYPE2 Register

1 EQEP_QDECCTL_TYPE2 Register (Offset = 28h) [reset = 0h]

Quadrature Decoder Control

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Table 14-24877. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0028h**
EQEP1	**2321 0028h**
EQEP2	**2322 0028h**

Figure 14-8210. EQEP_QDECCTL_TYPE2 Name Register

15	14	13	12	11	10	9	8
QSRC		SOEN	SPSEL	XCR	SWAP	IGATE	QAP
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QBP	QIP	QSP	RESERVED_1				QIDIRE
R/W	R/W	R/W	R				R/W
0h	0h	0h	0h				0h

Table 14-24879. EQEP_QDECCTL_TYPE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	QSRC	R/W	0h	Position-counter source selection Reset Source: vbus_rst_mod_g_rst_n
13	SOEN	R/W	0h	Sync output-enable Reset Source: vbus_rst_mod_g_rst_n 0 Disable position-compare sync output 1 Enable position-compare sync output
12	SPSEL	R/W	0h	Sync output pin selection Reset Source: vbus_rst_mod_g_rst_n 0 Index pin is used for sync output 1 Strobe pin is used for sync output
11	XCR	R/W	0h	External Clock Rate Reset Source: vbus_rst_mod_g_rst_n 0 2x resolution: Count the rising/falling edge 1 1x resolution: Count the rising edge only
10	SWAP	R/W	0h	CLK/DIR Signal Source for Position Counter Reset Source: vbus_rst_mod_g_rst_n 0 Quadrature-clock inputs are not swapped 1 Quadrature-clock inputs are swapped
9	IGATE	R/W	0h	Index pulse gating option Reset Source: vbus_rst_mod_g_rst_n 0 Disable gating of Index pulse 1 Gate the index pin with strobe

Table 14-24879. EQEP_QDECCTL_TYPE2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	QAP	R/W	0h	QEPA input polarity Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Negates QEPA input`
7	QBP	R/W	0h	QEPB input polarity Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Negates QEPB input`
6	QIP	R/W	0h	QEPI input polarity Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Negates QEPI input`
5	QSP	R/W	0h	QEPS input polarity Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Negates QEPS input`
4:1	RESERVED_1	R	0h	Reserved
0	QIDIRE	R/W	0h	0 - Compatible mode, Behavior same as existing devices 1 - Enhancement for Direction change during Index will be enabled Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.13 EQEP_QEPCTL Register

1 EQEP_QEPCTL Register (Offset = 2Ah) [reset = 0h]

QEP Control

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Table 14-24880. Instance Table

Instance Name	Physical Address
EQEP0	**2320 002Ah**
EQEP1	**2321 002Ah**
EQEP2	**2322 002Ah**

Figure 14-8211. EQEP_QEPCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PCRM		SEI		IEI	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

7	6	5	4	3	2	1	0
SWI	SEL	IEL		QPEN	QCLM	UTE	WDE
R/W	R/W	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-24882. EQEP_QEPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation mode Reset Source: vbus_rst_mod_g_rst_n 0 QPOSCNT behavior Position counter stops immediately on emulation suspend 0h (R/W) = QWDTMR behavior Watchdog counter stops immediately 0h (R/W) = QUTMR behavior Unit timer stops immediately 0h (R/W) = QCTMR behavior Capture Timer stops immediately 1 QPOSCNT behavior Position counter continues to count until the rollover 1h (R/W) = QWDTMR behavior Watchdog counter counts until WD period match roll over 1h (R/W) = QUTMR behavior Unit timer counts until period rollover 1h (R/W) = QCTMR behavior Capture Timer counts until next unit period event 2 QPOSCNT behavior Position counter is unaffected by emulation suspend 2h (R/W) = QWDTMR behavior Watchdog counter is unaffected by emulation suspend 2h (R/W) = QUTMR behavior Unit timer is unaffected by emulation suspend 2h (R/W) = QCTMR behavior Capture Timer is unaffected by emulation suspend 3 Same as FREE_SOFT_2
13:12	PCRM	R/W	0h	Postion counter reset Reset Source: vbus_rst_mod_g_rst_n 0 Position counter reset on an index event 1 Position counter reset on the maximum position 2 Position counter reset on the first index event 3 Position counter reset on a unit time event

Table 14-24882. EQEP_QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	SEI	R/W	0h	Strobe event initialization of position counter Reset Source: vbus_rst_mod_g_rst_n 0 Does nothing (action disabled) 1 Does nothing (action disabled) 2 Initializes the position counter on rising edge of the QEPS signal 3 Clockwise Direction: Initializes the position counter on the rising edge of QEPS strobe Counter Clockwise Direction: Initializes the position counter on the falling edge of QEPS strobe
9:8	IEI	R/W	0h	Index event init of position count Reset Source: vbus_rst_mod_g_rst_n 0 Do nothing (action disabled) 1 Do nothing (action disabled) 2 Initializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT) 3 Initializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT)
7	SWI	R/W	0h	Software init position counter Reset Source: vbus_rst_mod_g_rst_n 0 Do nothing (action disabled) 1 Initialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically
6	SEL	R/W	0h	Strobe event latch of position counter Reset Source: vbus_rst_mod_g_rst_n 0 The position counter is latched on the rising edge of QEPS strobe (QPOSSLAT = POSCCNT). Latching on the falling edge can be done by inverting the strobe input using the QSP bit in the QDECCTL register 1 Clockwise Direction: Position counter is latched on rising edge of QEPS strobe Counter Clockwise Direction: Position counter is latched on falling edge of QEPS strobe
5:4	IEL	R/W	0h	Index event latch of position counter [software index marker] Reset Source: vbus_rst_mod_g_rst_n 0 Reserved 1 Latches position counter on rising edge of the index signal 2 Latches position counter on falling edge of the index signal 3 Software index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking.

Table 14-24882. EQEP_QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	QPEN	R/W	0h	Quadrature position counter enable/software reset Reset Source: vbus_rst_mod_g_rst_n 0 Reset the eQEP peripheral internal operating flags/read-only registers. Control/configuration registers are not disturbed by a software reset. When QPEN is disabled, some flags in the QFLAG register do not show value as 0 and show the actual state of that flag. 1 eQEP position counter is enabled
2	QCLM	R/W	0h	QEP capture latch mode Reset Source: vbus_rst_mod_g_rst_n 0 Latch on position counter read by CPU. Capture timer and capture period values are latched into QCTMRLAT and QCPRDLAT registers when CPU reads the QPOSCNT register. 1 Latch on unit time out. Position counter, capture timer and capture period values are latched into QPOSLAT, QCTMRLAT and QCPRDLAT registers on unit time out.
1	UTE	R/W	0h	QEP unit timer enable Reset Source: vbus_rst_mod_g_rst_n 0 Disable eQEP unit timer 1 Enable unit timer
0	WDE	R/W	0h	QEP watchdog enable Reset Source: vbus_rst_mod_g_rst_n 0 Disable the eQEP watchdog timer 1 Enable the eQEP watchdog timer

14.9.4.4.2.14 EQEP_QCAPCTL Register

1 EQEP_QCAPCTL Register (Offset = 2Ch) [reset = 0h]

Qaudrature Capture Control

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Table 14-24883. Instance Table

Instance Name	Physical Address
EQEP0	**2320 002Ch**
EQEP1	**2321 002Ch**
EQEP2	**2322 002Ch**

Figure 14-8212. EQEP_QCAPCTL Name Register

15	14	13	12	11	10	9	8
CEN	RESERVED_1						
R/W	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	CCPS			UPPS			
R	R/W			R/W			
0h	0h			0h			

Table 14-24885. EQEP_QCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CEN	R/W	0h	Enable eQEP capture Reset Source: vbus_rst_mod_g_rst_n 0 eQEP capture unit is disabled 1 eQEP capture unit is enabled
14:7	RESERVED_1	R	0h	Reserved
6:4	CCPS	R/W	0h	eQEP capture timer clock prescaler Reset Source: vbus_rst_mod_g_rst_n 0 CAPCLK = SYSCLKOUT/1 1 CAPCLK = SYSCLKOUT/2 2 CAPCLK = SYSCLKOUT/4 3 CAPCLK = SYSCLKOUT/8 4 CAPCLK = SYSCLKOUT/16 5 CAPCLK = SYSCLKOUT/32 6 CAPCLK = SYSCLKOUT/64 7 CAPCLK = SYSCLKOUT/128

Table 14-24885. EQEP_QCAPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	UPPS	R/W	0h	Unit position event prescaler Reset Source: vbus_rst_mod_g_rst_n 0 `UPEVNT = QCLK/1` 1 `UPEVNT = QCLK/2` 2 `UPEVNT = QCLK/4` 3 `UPEVNT = QCLK/8` 4 `UPEVNT = QCLK/16` 5 `UPEVNT = QCLK/32` 6 `UPEVNT = QCLK/64` 7 `UPEVNT = QCLK/128` 8 `UPEVNT = QCLK/256` 9 `UPEVNT = QCLK/512` 10 `UPEVNT = QCLK/1024` 11 `UPEVNT = QCLK/2048` 12 `Reserved` 13 `Reserved` 14 `Reserved` 15 `Reserved`

14.9.4.4.2.15 EQEP_QPOSCTL Register

1 EQEP_QPOSCTL Register (Offset = 2Eh) [reset = 0h]

Position Compare Control

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Table 14-24886. Instance Table

Instance Name	Physical Address
EQEP0	**2320 002Eh**
EQEP1	**2321 002Eh**
EQEP2	**2322 002Eh**

Figure 14-8213. EQEP_QPOSCTL Name Register

15	14	13	12	11	10	9	8
PCSHDW	PCLOAD	PCPOL	PCE	PCSPW			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
PCSPW							
R/W							
0h							

Table 14-24888. EQEP_QPOSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCSHDW	R/W	0h	Position compare of shadow enable Reset Source: vbus_rst_mod_g_rst_n 0 `Shadow disabled, load Immediate` 1 `Shadow enabled`
14	PCLOAD	R/W	0h	Position compare of shadow load Reset Source: vbus_rst_mod_g_rst_n 0 `Load on QPOSCNT = 0` 1 `Load when QPOSCNT = QPOSCMP`
13	PCPOL	R/W	0h	Polarity of sync output Reset Source: vbus_rst_mod_g_rst_n 0 `Active HIGH pulse output` 1 `Active LOW pulse output`
12	PCE	R/W	0h	Position compare enable/disable Reset Source: vbus_rst_mod_g_rst_n 0 `Disable position compare unit` 1 `Enable position compare unit`
11:0	PCSPW	R/W	0h	Select-position-compare sync output pulse width Reset Source: vbus_rst_mod_g_rst_n 0 `1 * 4 * SYSCLKOUT cycles` 1 `2 * 4 * SYSCLKOUT cycles` 4095 `4096 * 4 * SYSCLKOUT cycles`

14.9.4.4.2.16 EQEP_QEINT_TYPE1 Register

1 EQEP_QEINT_TYPE1 Register (Offset = 30h) [reset = 0h]

QEP Interrupt Control

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Table 14-24889. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0030h**
EQEP1	**2321 0030h**
EQEP2	**2322 0030h**

Figure 14-8214. EQEP_QEINT_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_2			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	QPE	PCE	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24891. EQEP_QEINT_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12	QMAE	R/W	0h	QMA Error Interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
11	UTO	R/W	0h	Unit time out interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
10	IEL	R/W	0h	Index event latch interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
9	SEL	R/W	0h	Strobe event latch interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
8	PCM	R/W	0h	Position-compare match interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled
7	PCR	R/W	0h	Position-compare ready interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 Interrupt is disabled 1 Interrupt is enabled

Table 14-24891. EQEP_QEINT_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PCO	R/W	0h	Position counter overflow interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 `Interrupt is disabled` 1 `Interrupt is enabled`
5	PCU	R/W	0h	Position counter underflow interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 `Interrupt is disabled` 1 `Interrupt is enabled`
4	WTO	R/W	0h	Watchdog time out interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 `Interrupt is disabled` 1 `Interrupt is enabled`
3	QDC	R/W	0h	Quadrature direction change interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 `Interrupt is disabled` 1 `Interrupt is enabled`
2	QPE	R/W	0h	Quadrature phase error interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 `Interrupt is disabled` 1 `Interrupt is enabled`
1	PCE	R/W	0h	Position counter error interrupt enable Reset Source: vbus_rst_mod_g_rst_n 0 `Interrupt is disabled` 1 `Interrupt is enabled`
0	RESERVED_1	R	0h	Reserved

14.9.4.4.2.17 EQEP_QFLG_TYPE1 Register

1 EQEP_QFLG_TYPE1 Register (Offset = 32h) [reset = 0h]

QEP Interrupt Flag

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Table 14-24892. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0032h**
EQEP1	**2321 0032h**
EQEP2	**2322 0032h**

Figure 14-8215. EQEP_QFLG_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			QMAE	UTO	IEL	SEL	PCM
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24894. EQEP_QFLG_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	QMAE	R	0h	QMA Error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 Interrupt was generated
11	UTO	R	0h	Unit time out interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 Set by eQEP unit timer period match
10	IEL	R	0h	Index event latch interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 This bit is set after latching the QPOSCNT to QPOSILAT
9	SEL	R	0h	Strobe event latch interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 This bit is set after latching the QPOSCNT to QPOSSLAT
8	PCM	R	0h	eQEP compare match event interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 This bit is set on position-compare match

Table 14-24894. EQEP_QFLG_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	PCR	R	0h	Position-compare ready interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 This bit is set after transferring the shadow register value to the active position compare register
6	PCO	R	0h	Position counter overflow interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 This bit is set on position counter overflow.
5	PCU	R	0h	Position counter underflow interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 This bit is set on position counter underflow.
4	WTO	R	0h	Watchdog timeout interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 Set by watchdog timeout
3	QDC	R	0h	Quadrature direction change interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 Interrupt was generated
2	PHE	R	0h	Quadrature phase error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 Set on simultaneous transition of QEPA and QEPB
1	PCE	R	0h	Position counter error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 Position counter error
0	INT	R	0h	Global interrupt status flag Reset Source: vbus_rst_mod_g_rst_n 0 No interrupt generated 1 Interrupt was generated

14.9.4.4.2.18 EQEP_QCLR_TYPE1 Register

1 EQEP_QCLR_TYPE1 Register (Offset = 34h) [reset = 0h]

QEP Interrupt Clear

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Table 14-24895. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0034h**
EQEP1	**2321 0034h**
EQEP2	**2322 0034h**

Figure 14-8216. EQEP_QCLR_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24897. EQEP_QCLR_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	QMAE	R/W	0h	Clear QMA Error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
11	UTO	R/W	0h	Clear unit time out interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
10	IEL	R/W	0h	Clear index event latch interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
9	SEL	R/W	0h	Clear strobe event latch interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
8	PCM	R/W	0h	Clear eQEP compare match event interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
7	PCR	R/W	0h	Clear position-compare ready interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`

Table 14-24897. EQEP_QCLR_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PCO	R/W	0h	Clear position counter overflow interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
5	PCU	R/W	0h	Clear position counter underflow interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
4	WTO	R/W	0h	Clear watchdog timeout interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
3	QDC	R/W	0h	Clear quadrature direction change interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
2	PHE	R/W	0h	Clear quadrature phase error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
1	PCE	R/W	0h	Clear position counter error interrupt flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`
0	INT	R/W	0h	Global interrupt clear flag Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Clears the interrupt flag`

14.9.4.4.2.19 EQEP_QFRC_TYPE1 Register

1 EQEP_QFRC_TYPE1 Register (Offset = 36h) [reset = 0h]

QEP Interrupt Force

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Table 14-24898. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0036h**
EQEP1	**2321 0036h**
EQEP2	**2322 0036h**

Figure 14-8217. EQEP_QFRC_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_2			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	PHE	PCE	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-24900. EQEP_QFRC_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12	QMAE	R/W	0h	Force QMA error interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
11	UTO	R/W	0h	Force unit time out interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
10	IEL	R/W	0h	Force index event latch interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
9	SEL	R/W	0h	Force strobe event latch interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
8	PCM	R/W	0h	Force position-compare match interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`
7	PCR	R/W	0h	Force position-compare ready interrupt Reset Source: vbus_rst_mod_g_rst_n 0 `No effect` 1 `Force the interrupt`

Table 14-24900. EQEP_QFRC_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PCO	R/W	0h	Force position counter overflow interrupt Reset Source: vbus_rst_mod_g_rst_n 0 No effect 1 Force the interrupt
5	PCU	R/W	0h	Force position counter underflow interrupt Reset Source: vbus_rst_mod_g_rst_n 0 No effect 1 Force the interrupt
4	WTO	R/W	0h	Force watchdog time out interrupt Reset Source: vbus_rst_mod_g_rst_n 0 No effect 1 Force the interrupt
3	QDC	R/W	0h	Force quadrature direction change interrupt Reset Source: vbus_rst_mod_g_rst_n 0 No effect 1 Force the interrupt
2	PHE	R/W	0h	Force quadrature phase error interrupt Reset Source: vbus_rst_mod_g_rst_n 0 No effect 1 Force the interrupt
1	PCE	R/W	0h	Force position counter error interrupt Reset Source: vbus_rst_mod_g_rst_n 0 No effect 1 Force the interrupt
0	RESERVED_1	R	0h	Reserved

14.9.4.4.2.20 EQEP_QEPSTS_TYPE1 Register

1 EQEP_QEPSTS_TYPE1 Register (Offset = 38h) [reset = 80h]

QEP Status

Return to Summary Table

Table 14-24901. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0038h**
EQEP1	**2321 0038h**
EQEP2	**2322 0038h**

Figure 14-8218. EQEP_QEPSTS_TYPE1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
UPEVNT	FIDF	QDF	QDLF	COEF	CDEF	FIMF	PCEF
R/W	R	R	R	R/W	R/W	R/W	R
1h	0h	0h	0h	0h	0h	0h	0h

Table 14-24903. EQEP_QEPSTS_TYPE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7	UPEVNT	R/W	1h	Unit position event flag Reset Source: vbus_rst_mod_g_rst_n 0 `No unit position event detected` 1 `Unit position event detected. Write 1 to clear`
6	FIDF	R	0h	Direction on the first index marker Status of the direction is latched on the first index event marker. Reset Source: vbus_rst_mod_g_rst_n 0 `Counter-clockwise rotation (or reverse movement) on the first index event` 1 `Clockwise rotation (or forward movement) on the first index event`
5	QDF	R	0h	Quadrature direction flag Reset Source: vbus_rst_mod_g_rst_n 0 `Counter-clockwise rotation (or reverse movement)` 1 `Clockwise rotation (or forward movement)`
4	QDLF	R	0h	eQEP direction latch flag Reset Source: vbus_rst_mod_g_rst_n 0 `Counter-clockwise rotation (or reverse movement) on index event marker` 1 `Clockwise rotation (or forward movement) on index event marker`

Table 14-24903. EQEP_QEPSTS_TYPE1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	COEF	R/W	0h	Capture overflow error flag Reset Source: vbus_rst_mod_g_rst_n 0 Overflow has not occurred. 1 Overflow occurred in eQEP Capture timer (QEPCTMR). This bit is cleared by writing a '1'.
2	CDEF	R/W	0h	Capture direction error flag Reset Source: vbus_rst_mod_g_rst_n 0 Capture direction error has not occurred. 1 Direction change occurred between the capture position event. This bit is cleared by writing a '1'.
1	FIMF	R/W	0h	First index marker flag Reset Source: vbus_rst_mod_g_rst_n 0 First index pulse has not occurred. 1 Set by first occurrence of index pulse. This bit is cleared by writing a '1'.
0	PCEF	R	0h	Position counter error flag. This bit is not sticky and it is updated for every index event. Reset Source: vbus_rst_mod_g_rst_n 0 No error occurred during the last index transition 1 Position counter error

14.9.4.4.2.21 EQEP_QCTMR Register

1 EQEP_QCTMR Register (Offset = 3Ah) [reset = 0h]

QEP Capture Timer

Return to Summary Table

Table 14-24904. Instance Table

Instance Name	Physical Address
EQEP0	**2320 003Ah**
EQEP1	**2321 003Ah**
EQEP2	**2322 003Ah**

Figure 14-8219. EQEP_QCTMR Name Register

15	14	13	12	11	10	9	8
QCTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QCTMR							
R/W							
0h							

Table 14-24906. EQEP_QCTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCTMR	R/W	0h	This register provides time base for edge capture unit. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.22 EQEP_QCPRD Register

1 EQEP_QCPRD Register (Offset = 3Ch) [reset = 0h]

QEP Capture Period

Return to Summary Table

Table 14-24907. Instance Table

Instance Name	Physical Address
EQEP0	**2320 003Ch**
EQEP1	**2321 003Ch**
EQEP2	**2322 003Ch**

Figure 14-8220. EQEP_QCPRD Name Register

15	14	13	12	11	10	9	8
QCPRD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QCPRD							
R/W							
0h							

Table 14-24909. EQEP_QCPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCPRD	R/W	0h	This register holds the period count value between the last successive eQEP position events Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.23 EQEP_QCTMRLAT Register

1 EQEP_QCTMRLAT Register (Offset = 3Eh) [reset = 0h]

QEP Capture Latch

Return to Summary Table

Table 14-24910. Instance Table

Instance Name	Physical Address
EQEP0	**2320 003Eh**
EQEP1	**2321 003Eh**
EQEP2	**2322 003Eh**

Figure 14-8221. EQEP_QCTMRLAT Name Register

15	14	13	12	11	10	9	8
QCTMRLAT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QCTMRLAT							
R							
0h							

Table 14-24912. EQEP_QCTMRLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCTMRLAT	R	0h	The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, Reading the eQEP position counter. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.24 EQEP_QCPRDLAT Register

1 EQEP_QCPRDLAT Register (Offset = 40h) [reset = 0h]

QEP Capture Period Latch

Return to Summary Table

Table 14-24913. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0040h**
EQEP1	**2321 0040h**
EQEP2	**2322 0040h**

Figure 14-8222. EQEP_QCPRDLAT Name Register

15	14	13	12	11	10	9	8
QCPRDLAT							
R							
0h							
7	6	5	4	3	2	1	0
QCPRDLAT							
R							
0h							

Table 14-24915. EQEP_QCPRDLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCPRDLAT	R	0h	eQEP capture period value can be latched into this register on two events viz., unit timeout event, Reading the eQEP position counter. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.25 EQEP_RESERVED_1_j Register

1 EQEP_RESERVED_1_j Register (Offset = 42h + formula) [reset = 0h]

Return to Summary Table

Offset = (j * 2h); where j = 0 to 12d

Table 14-24916. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0042h + formula**
EQEP1	**2321 0042h + formula**
EQEP2	**2322 0042h + formula**

Figure 14-8223. EQEP_RESERVED_1_j Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24918. EQEP_RESERVED_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.4.2.26 EQEP_PID Register

1 EQEP_PID Register (Offset = 5Ch) [reset = 44D30200h]

Peripheral ID Register

Return to Summary Table

Table 14-24919. Instance Table

Instance Name	Physical Address
EQEP0	**2320 005Ch**
EQEP1	**2321 005Ch**
EQEP2	**2322 005Ch**

Figure 14-8224. EQEP_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNCTION			
R		R		R			
1h		0h		4D3h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
4D3h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-24921. EQEP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Reset Source: vbus_rst_mod_g_rst_n
29:28	RESERVED	R	0h	
27:16	FUNCTION	R	4D3h	Reset Source: vbus_rst_mod_g_rst_n
15:11	RTL	R	0h	Reset Source: vbus_rst_mod_g_rst_n
10:8	MAJOR	R	2h	Reset Source: vbus_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Reset Source: vbus_rst_mod_g_rst_n
5:0	MINOR	R	0h	Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.27 EQEP_REV_TYPE2 Register

1 EQEP_REV_TYPE2 Register (Offset = 60h) [reset = 9h]

QEP Revision Number

Return to Summary Table

Table 14-24922. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0060h**
EQEP1	**2321 0060h**
EQEP2	**2322 0060h**

Figure 14-8225. EQEP_REV_TYPE2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1		MINOR			MAJOR		
R		R			R		
0h		1h			1h		

Table 14-24924. EQEP_REV_TYPE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_1	R	0h	Reserved
5:3	MINOR	R	1h	This field specifies the Minor Revision number for the eQEP IP. Reset Source: vbus_rst_mod_g_rst_n
2:0	MAJOR	R	1h	This field specifies the Major Revision number for the eQEP IP. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.28 EQEP_QEPSTROBESEL Register

1 EQEP_QEPSTROBESEL Register (Offset = 64h) [reset = 0h]

QEP Strobe select register

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Table 14-24925. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0064h**
EQEP1	**2321 0064h**
EQEP2	**2322 0064h**

Figure 14-8226. EQEP_QEPSTROBESEL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						STROBESEL	
R						R/W	
0h						0h	

Table 14-24927. EQEP_QEPSTROBESEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1:0	STROBESEL	R/W	0h	Strobe source select: Reset Source: vbus_rst_mod_g_rst_n 0 QEP Strobe after polarity mux 1 QEP Strobe after polarity mux. Same as QS_AFTER_POL_MUX 2 QEP Strobe after polarity mux ORed with ADCSOCA 3 QEP Strobe after polarity mux ORed with ADCSOCB

14.9.4.4.2.29 EQEP_QMACTRL Register

1 EQEP_QMACTRL Register (Offset = 68h) [reset = 0h]

QMA Control register

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Table 14-24928. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0068h**
EQEP1	**2321 0068h**
EQEP2	**2322 0068h**

Figure 14-8227. EQEP_QMACTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1					MODE		
R					R/W		
0h					0h		

Table 14-24930. EQEP_QMACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved
2:0	MODE	R/W	0h	Select Mode for QMA mode: 000 : QMA Module is bypassed. 001 : QMA Mode-1 operation selected 010 : QMA Mode-2 operation selected 011 : QMA Module is bypassed [reserved] 1xx : QMA Module is bypassed [reserved] Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.30 EQEP_QEPSRCSEL Register

1 EQEP_QEPSRCSEL Register (Offset = 6Ch) [reset = 0h]

QEP Source Select Register

Return to Summary Table

Table 14-24931. Instance Table

Instance Name	Physical Address
EQEP0	**2320 006Ch**
EQEP1	**2321 006Ch**
EQEP2	**2322 006Ch**

Figure 14-8228. EQEP_QEPSRCSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">QEPSSEL</td><td colspan="4">QEPISEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">QEPBSEL</td><td colspan="4">QEPASEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-24933. EQEP_QEPSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_1	R	0h	Reserved
15:12	QEPSSEL	R/W	0h	QEP Strobe source select: 0000: From device Pins [Default]. 0001-1111: Device dependent. Reset Source: vbus_rst_mod_g_rst_n
11:8	QEPISEL	R/W	0h	QEP Index source select: 0000: From device Pins [Default]. 0001-1111: Device dependent. Reset Source: vbus_rst_mod_g_rst_n
7:4	QEPBSEL	R/W	0h	QEPB source select: 0000: From device Pins [Default]. 0001-1111: Device dependent. Reset Source: vbus_rst_mod_g_rst_n
3:0	QEPASEL	R/W	0h	QEPA source select: 0000: From device Pins [Default]. 0001-1111: Device dependent. Reset Source: vbus_rst_mod_g_rst_n

14.9.4.4.2.31 EQEP_RESERVED_2_j Register

1 EQEP_RESERVED_2_j Register (Offset = 70h + formula) [reset = 0h]

Return to Summary Table

Offset = (j * 2h); where j = 0 to 7d

Table 14-24934. Instance Table

Instance Name	Physical Address
EQEP0	**2320 0070h + formula**
EQEP1	**2321 0070h + formula**
EQEP2	**2322 0070h + formula**

Figure 14-8229. EQEP_RESERVED_2_j Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24936. EQEP_RESERVED_2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.5 FSITX

FSITX

14.9.4.5.1 FSITX Summaries

FSITX Summaries

Table 14-24937. FSI_TX_CFG Registers, Base Address=2361 0000h, Length=256

Offset	Length	Register Name	FSITX1 Physical Address
0h	16	FSI_TX_CFG_TX_MASTER_CTRL	2361 0000h
2h	16	FSI_TX_CFG_RESERVED_1	2361 0002h
4h	16	FSI_TX_CFG_TX_CLK_CTRL	2361 0004h
6h	16	FSI_TX_CFG_RESERVED_2	2361 0006h
8h	16	FSI_TX_CFG_TX_OPER_CTRL_LO_ALT1_	2361 0008h
Ah	16	FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1_	2361 000Ah
Ch	16	FSI_TX_CFG_TX_FRAME_CTRL	2361 000Ch
Eh	16	FSI_TX_CFG_TX_FRAME_TAG_UDATA	2361 000Eh
10h	16	FSI_TX_CFG_TX_BUF_PTR_LOAD	2361 0010h
12h	16	FSI_TX_CFG_TX_BUF_PTR_STS	2361 0012h
14h	16	FSI_TX_CFG_TX_PING_CTRL_ALT1_	2361 0014h
16h	16	FSI_TX_CFG_TX_PING_TAG	2361 0016h
18h	32	FSI_TX_CFG_TX_PING_TO_REF	2361 0018h
1Ch	32	FSI_TX_CFG_TX_PING_TO_CNT	2361 001Ch
20h	16	FSI_TX_CFG_TX_INT_CTRL	2361 0020h
22h	16	FSI_TX_CFG_TX_DMA_CTRL	2361 0022h
24h	16	FSI_TX_CFG_TX_LOCK_CTRL	2361 0024h
26h	16	FSI_TX_CFG_RESERVED_3	2361 0026h
28h	16	FSI_TX_CFG_TX_EVT_STS	2361 0028h
2Ah	16	FSI_TX_CFG_RESERVED_4	2361 002Ah
2Ch	16	FSI_TX_CFG_TX_EVT_CLR	2361 002Ch
2Eh	16	FSI_TX_CFG_TX_EVT_FRC	2361 002Eh
30h	16	FSI_TX_CFG_TX_USER_CRC	2361 0030h
32h	16	FSI_TX_CFG_RESERVED_5	2361 0032h
34h	32	FSI_TX_CFG_RESERVED_6	2361 0034h
38h	32	FSI_TX_CFG_RESERVED_7	2361 0038h
3Ch	32	FSI_TX_CFG_RESERVED_8	2361 003Ch
40h	32	FSI_TX_CFG_TX_ECC_DATA	2361 0040h
44h	16	FSI_TX_CFG_TX_ECC_VAL	2361 0044h
46h	16	FSI_TX_CFG_RESERVED_9_J	2361 0046h + formula
80h	16	FSI_TX_CFG_TX_BUF_BASE_J	2361 0080h + formula

14.9.4.5.2 FSITX Registers

FSITX Registers

14.9.4.5.2.1 FSI_TX_CFG_TX_MASTER_CTRL Register

1 FSI_TX_CFG_TX_MASTER_CTRL Register (Offset = 0h) [reset = 0h]

Transmit master control register

Return to Summary Table

Table 14-24938. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0000h**

Figure 14-8230. FSI_TX_CFG_TX_MASTER_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						FLUSH	CORE_RST
R						R/W	R/W
0h						0h	0h

Table 14-24940. FSI_TX_CFG_TX_MASTER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key In order to write to any bit in this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register. Reset Source: rst_mod_g_rst_n
7:2	RESERVED_1	R	0h	Reserved
1	FLUSH	R/W	0h	Flush Operation Start bit This bit will cause the transmitter to initiate a flush pattern of a single toggle on the TXD0 and TXD1 followed by five full cycles of TXCLK. This bit should be written only when the CORE_RST bit is 0 and the clock to the Transmitter core is turned on. 0h [R/W] = Clear this bit. 1h [R/W] = Setting this bit will Initiate flush sequence. To properly execute a flush sequence, Set FLUSH to 1, wait for five TXCLK cycles then clear FLUSH to 0. Note: The KEY field must contain 0xA5 for any write to this bit to take effect. The software must keep this bit set to 1 for at least five TXCLK cycles before setting it back to 0. Reset Source: rst_mod_g_rst_n
0	CORE_RST	R/W	0h	Transmitter Master Core Reset bit This bit controls the transmitter master core reset. In order to send any frame, this bit must be cleared. 0h [R/W] = Transmitter core is not in reset and can transmit frames. 1h [R/W] = Transmitter core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.2 FSI_TX_CFG_RESERVED_1 Register

1 FSI_TX_CFG_RESERVED_1 Register (Offset = 2h) [reset = 0h]

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Table 14-24941. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0002h**

Figure 14-8231. FSI_TX_CFG_RESERVED_1 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24943. FSI_TX_CFG_RESERVED_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.3 FSI_TX_CFG_TX_CLK_CTRL Register

1 FSI_TX_CFG_TX_CLK_CTRL Register (Offset = 4h) [reset = 0h]

Transmit clock control register. Protected by LOCK field in TX_LOCK_CTRL register.

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Table 14-24944. Instance Table

Instance Name	Physical Address
FSITX1	2361 0004h

Figure 14-8232. FSI_TX_CFG_TX_CLK_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PRESCALE_VAL	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PRESCALE_VAL						CLK_EN	CLK_RST
R/W						R/W	R/W
0h						0h	0h

Table 14-24946. FSI_TX_CFG_TX_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:2	PRESCALE_VAL	R/W	0h	Clock Divider Prescale Value The input clock is divided by this 8-bit value and fed into the transmitter core. This divided clock is the rate at which TXCLK will operate. 0h [R/W] = Reserved 1h [R/W] = Input clock /1 2h [R/W] = Input clock /2 3h [R/W] = Input clock /3 4h [R/W] = Input clock /4 ... FFh [R/W] = Input clock /255 TXCLKIN = Input clock / PRESCALE_VAL In FSI mode: TXCLK = TXCLKIN / 2 In SPI mode: TXCLK = TXCLKIN Reset Source: rst_mod_g_rst_n
1	CLK_EN	R/W	0h	Clock Divider Enable bit This bit will enable and disable the input clock divider and start the clock to the transmitter core. 0h [R/W] = The input clock divider is not enabled and the clock is not connected to the transmitter core. 1h [R/W] = The input clock to the transmitter core is being divided by the PRESCALE_VAL and enabled. Reset Source: rst_mod_g_rst_n
0	CLK_RST	R/W	0h	Clock Divider Reset bit This bit will reset the clock counter in the clock divider. 0h [R/W] = The clock divider is set based on the value in PRESCALE_VAL. The input clock will be divided by PRESCALE_VAL if CLK_EN is set. 1h [R/W] = The clock divider will be reset to 0 and will stay reset until software writes a 0 to this bit. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.4 FSI_TX_CFG_RESERVED_2 Register

1 FSI_TX_CFG_RESERVED_2 Register (Offset = 6h) [reset = 0h]

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Table 14-24947. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0006h**

Figure 14-8233. FSI_TX_CFG_RESERVED_2 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-24949. FSI_TX_CFG_RESERVED_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.5 FSI_TX_CFG_TX_OPER_CTRL_LO_ALT1_ Register

1 FSI_TX_CFG_TX_OPER_CTRL_LO_ALT1_ Register (Offset = 8h) [reset = 0h]

Transmit operation control register low. Protected by LOCK field in TX_LOCK_CTRL register.

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Table 14-24950. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0008h**

Figure 14-8234. FSI_TX_CFG_TX_OPER_CTRL_LO_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1						TDM_ENABLE	SEL_PLLCLK
R						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PING_TO_MODE	SW_CRC	START_MODE			SPI_MODE	DATA_WIDTH	
R/W	R/W	R/W			R/W	R/W	
0h	0h	0h			0h	0h	

Table 14-24952. FSI_TX_CFG_TX_OPER_CTRL_LO_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9	TDM_ENABLE	R/W	0h	Transmit TDM Mode Enable bit. This bit enables the TDM Mode for multi-slave TDM operation. 0h [R/W] Transmit TDM Mode is not enabled. 1h [R/W] Transmit TDM Mode is enabled. Reset Source: rst_mod_g_rst_n
8	SEL_PLLCLK	R/W	0h	Input Clock Select bit This bit selects the input clock source for the transmitter core. 0h [R/W] = SYSCLK is the source of the transmitter clock into the clock prescaler. 1h [R/W] = PLLRAWCLK is the source of the transmitter core clock into the clock prescaler. Reset Source: rst_mod_g_rst_n
7	PING_TO_MODE	R/W	0h	Ping Counter Reset Mode Select bit This bit selects when the ping counter will reset. 0h [R/W] = The ping counter will reset and restart only on hardware initiated ping frames, when ping counter has timed out. 1h [R/W] = The ping counter will reset and restart on any software initiated frame as well as a ping counter timeout Reset Source: rst_mod_g_rst_n
6	SW_CRC	R/W	0h	CRC Source Select bit This bit selects the source of the CRC value that is transmitted. 0h [R/W] = The transmitted CRC value is computed by hardware. 1h [R/W] = The transmitted CRC value is sourced from the value programmed in the TX_USER_CRC register. Reset Source: rst_mod_g_rst_n

Table 14-24952. FSI_TX_CFG_TX_OPER_CTRL_LO_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	START_MODE	R/W	0h	Transmission Start Mode Select bit These bits select the method by which a new frame transmission is started. 0h [R/W] = Only a software write to TX_FRAME_CTRL.START initiate a new transmission. 1h [R/W] = The configured external trigger will initiate a new transmission. 2h [R/W] = Either Writing to TX_FRAME_CTRL.START or the TX_FRAME_TAG_UDATA register will initiate a new transmission. All other combinations of bits are illegal and reserved for future use. Reset Source: rst_mod_g_rst_n
2	SPI_MODE	R/W	0h	SPI Mode Select bit This bit enables and disables SPI compatibility mode. 0h [R/W] = FSI is in normal mode of operation. 1h [R/W] = FSI is operating in SPI compatibility mode. Reset Source: rst_mod_g_rst_n
1:0	DATA_WIDTH	R/W	0h	Transmit Data Width Select bits These bits define the number of data lines used by the transmitter. 0h [R/W] = Data will be transmitted on one data line [TXD0] 1h [R/W] = Data will be transmitted on two data lines [TXD0 and TXD1]. The format of the data is described in the preceeding chapter. 2h, 3h [R/W] = Reserved Reset Source: rst_mod_g_rst_n

14.9.4.5.2.6 FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1_ Register

1 FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1_ Register (Offset = Ah) [reset = 0h]

Transmit operation control register high. Protected by LOCK field in TX_LOCK_CTRL register.

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Table 14-24953. Instance Table

Instance Name	Physical Address
FSITX1	**2361 000Ah**

Figure 14-8235. FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_2			EXT_TRIG_SEL				
R			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXT_TRIG_SEL	ECC_SEL	FORCE_ERR	RESERVED_1				
R/W	R/W	R/W	R				
0h	0h	0h	0h				

Table 14-24955. FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12:7	EXT_TRIG_SEL	R/W	0h	External Trigger Select bit These bits define which of the 32 external inputs will be used as the source for the external input trigger. 00h [R/W] = Trigger 1 is the source. 01h [R/W] = Trigger 2 is the source. 02h [R/W] = Trigger 3 is the source. ... 3Fh [R/W] = Trigger 64 is the source. Reset Source: rst_mod_g_rst_n
6	ECC_SEL	R/W	0h	ECC Data Width Select bit This bit selects between 16-bit and 32-bit ECC computation. 0h [R/W] = 32-bit ECC is used. 1h [R/W] = 16-bit ECC is used. Reset Source: rst_mod_g_rst_n
5	FORCE_ERR	R/W	0h	Error Frame Force bit This bit will force the the CRC value of the transmitted data frame to 0 whenever there is a buffer overrun or underrun condition. This can be used to force a corrupted CRC as the data is not guaranteed to be reliable. The receiver will treat the data as invalid and can handle this as needed. Note: DO NOT use FORCE_ERR if using the SW CRC mode [FSI Transmit]. 0h [R/W] = The CRC will not be forced to 0. 1h [R/W] = The CRC will be forced to 0 in a buffer overrun or underrun condition. Reset Source: rst_mod_g_rst_n
4:0	RESERVED_1	R	0h	Reserved

14.9.4.5.2.7 FSI_TX_CFG_TX_FRAME_CTRL Register

1 FSI_TX_CFG_TX_FRAME_CTRL Register (Offset = Ch) [reset = 0h]

Transmit frame control register

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Table 14-24956. Instance Table

Instance Name	Physical Address
FSITX1	**2361 000Ch**

Figure 14-8236. FSI_TX_CFG_TX_FRAME_CTRL Name Register

15	14	13	12	11	10	9	8
START	RESERVED_1						
R/W	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
N_WORDS				FRAME_TYPE			
R/W				R/W			
0h				0h			

Table 14-24958. FSI_TX_CFG_TX_FRAME_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	START	R/W	0h	Start Transmission bit This bit will cause the FSI to start transmitting the next frame. 0h [R/W] = Writing a 0 to this bit will have no effect. 1h [R/W] = Start the next transmission. This bit will be cleared by hardware. Reset Source: rst_mod_g_rst_n
14:8	RESERVED_1	R	0h	Reserved
7:4	N_WORDS	R/W	0h	Number of Words to be Transmitted This field defines the number of words which will be transmitted in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the receiver. Set this bitfield to be one less than the number of words to be transmitted. 0h [R/W] = 1 data word frame [16-bit data]. 1h [R/W] = 2 data word frame [32-bit data]. .. Fh [R/W] = 16 data word frame [256-bit data]. Reset Source: rst_mod_g_rst_n

Table 14-24958. FSI_TX_CFG_TX_FRAME_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	FRAME_TYPE	R/W	0h	Transmit Frame Type This field determines the type of frame that will be transmitted next. 0000b [R/W] = Ping Frame. This frame can be sent either by software or automatically by hardware. 0100b [R/W] = DATA_1_WORD Frame. One word data frame [16-bit data]. 0101b [R/W] = DATA_2_WORD Frame. Two word data frame [32-bit data]. 0110b [R/W] = DATA_4_WORD Frame. Four word data frame [64-bit data]. 0111b [R/W] = DATA_6_WORD Frame. Six word data frame [96-bit data]. 0011b [R/W] = DATA_N_WORD Frame. The N_WORDS field will determine the number of words [1 to 16] to be sent. Both the transmitter and receiver must have the same value programmed. 1111b [R/W] = Error Frame. This frame can be used during error conditions or any condition where the transmitter wants to notify the receiver of a high priorty status. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.8 FSI_TX_CFG_TX_FRAME_TAG_UDATA Register

1 FSI_TX_CFG_TX_FRAME_TAG_UDATA Register (Offset = Eh) [reset = 0h]

Transmit frame tag and user data register

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Table 14-24959. Instance Table

Instance Name	Physical Address
FSITX1	**2361 000Eh**

Figure 14-8237. FSI_TX_CFG_TX_FRAME_TAG_UDATA Name Register

15	14	13	12	11	10	9	8
USER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				FRAME_TAG			
R				R/W			
0h				0h			

Table 14-24961. FSI_TX_CFG_TX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	USER_DATA	R/W	0h	User Data bits This is a user-defined value that will be loaded into the the user data phase of the frame. This 8-bit value can be used by the receiver for any application need. This value will not impact any hardware behavior. Reset Source: rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved
3:0	FRAME_TAG	R/W	0h	This will be used only for software initiated transmissions. Frame tag bits This is a user-defined value that will be loaded into the frame tag phase of the next transmission. The receiver may use the frame tag for any application need. This value will not impact any hardware behavior For external triggers do not use this register. Use the TX_PING_TAG register instead. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.9 FSI_TX_CFG_TX_BUF_PTR_LOAD Register

1 FSI_TX_CFG_TX_BUF_PTR_LOAD Register (Offset = 10h) [reset = 0h]

Transmit buffer pointer control load register

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Table 14-24962. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0010h**

Figure 14-8238. FSI_TX_CFG_TX_BUF_PTR_LOAD Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				BUF_PTR_LOAD			
R				R/W			
0h				0h			

Table 14-24964. FSI_TX_CFG_TX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:0	BUF_PTR_LOAD	R/W	0h	Buffer Pointer Load bits These bits are used to force the transmit buffer pointer to a desired index within the transmit buffer. The next transmission will begin picking data from this index and increment appropriately. This value will be reflected in TX_BUF_PTR_STS only after a minimum 3 SYSCLK cycles + 3 TXCLK cycles. This value should not be written while there is an active transmission as it may corrupt the ongoing frame or other undefined behavior. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.10 FSI_TX_CFG_TX_BUF_PTR_STS Register

1 FSI_TX_CFG_TX_BUF_PTR_STS Register (Offset = 12h) [reset = 0h]

Transmit buffer pointer control status register

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Table 14-24965. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0012h**

Figure 14-8239. FSI_TX_CFG_TX_BUF_PTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED_2			CURR_WORD_CNT				
R			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				CURR_BUF_PTR			
R				R			
0h				0h			

Table 14-24967. FSI_TX_CFG_TX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12:8	CURR_WORD_CNT	R	0h	Words Remaining in the transmit buffer This value indicates the number of words present in the data buffer which have not yet been transmitted. This value is only valid when there is no active transmission. Note: This value will not be valid if there is a buffer overrun or underrun condition. Reset Source: rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved
3:0	CURR_BUF_PTR	R	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.11 FSI_TX_CFG_TX_PING_CTRL_ALT1_ Register

1 FSI_TX_CFG_TX_PING_CTRL_ALT1_ Register (Offset = 14h) [reset = 0h]

Transmit ping control register. Protected by LOCK field in TX_LOCK_CTRL register.

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Table 14-24968. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0014h**

Figure 14-8240. FSI_TX_CFG_TX_PING_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1							EXT_TRIG_SEL
R							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXT_TRIG_SEL					EXT_TRIG_EN	TIMER_EN	CNT_RST
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-24970. FSI_TX_CFG_TX_PING_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved
8:3	EXT_TRIG_SEL	R/W	0h	External Trigger Select bits This bitfield will select one of the 64 external trigger inputs to as the source to generate a ping frame. A ping frame will only be generated if the EXT_TRIG_EN bit is set. 0h [R/W] = Trigger 1 will be used to generate a ping frame. 1h [R/W] = Trigger 2 will be used to generate a ping frame. .. 3Fh [R/W] = Trigger 64 will be used to generate a ping frame. Reset Source: rst_mod_g_rst_n
2	EXT_TRIG_EN	R/W	0h	External Trigger Enable bit This bit will allow the external trigger logic to generate a ping frame. 0h [R/W] = External triggers will not be used to generate ping frames. 1h [R/W] = The selected external trigger [selected by EXT_TRIG_SEL bits] will be able to generate a ping frame. The ping timer will be ignored if this bit is set. Reset Source: rst_mod_g_rst_n
1	TIMER_EN	R/W	0h	Ping Timer Enable bit This bit will enable the ping timer for generating periodic ping frames. 0h [R/W] = The ping timer is disabled and will not generate ping frames. 1h [R/W] = The ping timer is enabled and can be used to generate ping frames.Once the timer count reaches the value set by the TX_PING_TO_REF register, it will initiate a ping frame transmission. Note: If the ping timer is used, EXT_TRIG_EN should not be set as it will override this function. Reset Source: rst_mod_g_rst_n

Table 14-24970. FSI_TX_CFG_TX_PING_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CNT_RST	R/W	0h	Ping Counter Reset bit This bit will reset the the ping counter to 0. This bit will always be read as 0. 0h [R/W] = Writing a 0 to this bit has no effect. 1h [R/W] = The ping counter will be reset to 0. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.12 FSI_TX_CFG_TX_PING_TAG Register

1 FSI_TX_CFG_TX_PING_TAG Register (Offset = 16h) [reset = 0h]

Transmit ping tag register

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Table 14-24971. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0016h**

Figure 14-8241. FSI_TX_CFG_TX_PING_TAG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				TAG			
R				R/W			
0h				0h			

Table 14-24973. FSI_TX_CFG_TX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:0	TAG	R/W	0h	Ping Frame Tag This field contains a 4-bit tag which will be sent in any ping frame that is initiated by an external trigger or the ping timer. This field is user-defined and can be set based on the application requirement. If a ping frame is generated manually, the transmitted tag will be from TX_FRAME_TAG_UDATA.FRAME_TAG, not this value. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.13 FSI_TX_CFG_TX_PING_TO_REF Register

1 FSI_TX_CFG_TX_PING_TO_REF Register (Offset = 18h) [reset = 0h]

Transmit ping timeout counter reference. Protected by LOCK field in TX_LOCK_CTRL register.

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Table 14-24974. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0018h**

Figure 14-8242. FSI_TX_CFG_TX_PING_TO_REF Name Register

31	30	29	28	27	26	25	24
TO_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
TO_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
TO_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
TO_REF							
R/W							
0h							

Table 14-24976. FSI_TX_CFG_TX_PING_TO_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO_REF	R/W	0h	Ping Timer Reference Value. This is the 32-bit reference value for the ping timer. The timer will increment the counter starting from 0. When the reference value is reached, it will generate a timeout event, triggering a ping frame transmission. The counter will then reset to 0 and continue counting. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.14 FSI_TX_CFG_TX_PING_TO_CNT Register

1 FSI_TX_CFG_TX_PING_TO_CNT Register (Offset = 1Ch) [reset = 0h]

Transmit ping timeout current count

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Table 14-24977. Instance Table

Instance Name	Physical Address
FSITX1	**2361 001Ch**

Figure 14-8243. FSI_TX_CFG_TX_PING_TO_CNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TO_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TO_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TO_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TO_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-24979. FSI_TX_CFG_TX_PING_TO_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO_CNT	R	0h	Ping Timer Counter Value This register contains the current value of the ping timer counter. After reset, this counter will increment until it reaches the reference value [TX_PING_TO_REF], at which point it generates a ping frame transmission. After this point, the counter will reset to 0 and continue counting. This is a free-running counter Reset Source: rst_mod_g_rst_n

14.9.4.5.2.15 FSI_TX_CFG_TX_INT_CTRL Register

1 FSI_TX_CFG_TX_INT_CTRL Register (Offset = 20h) [reset = 0h]

Transmit interrupt event control register. Protected by LOCK field in TX_LOCK_CTRL register.

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Table 14-24980. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0020h**

Figure 14-8244. FSI_TX_CFG_TX_INT_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_2				INT2_EN_PING_TO	INT2_EN_BUF_OVERRUN	INT2_EN_BUF_UNDERRUN	INT2_EN_FRAME_DONE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				INT1_EN_PING_TO	INT1_EN_BUF_OVERRUN	INT1_EN_BUF_UNDERRUN	INT1_EN_FRAME_DONE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-24982. FSI_TX_CFG_TX_INT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_2	R	0h	Reserved
11	INT2_EN_PING_TO	R/W	0h	Enable PING Timer Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT2. 1h [R/W] = The ping timer event will trigger an interrupt on TX_INT2. Reset Source: rst_mod_g_rst_n
10	INT2_EN_BUF_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT2. 1h [R/W] = A Buffer Overrun condition will trigger an interrupt on TX_INT2. Reset Source: rst_mod_g_rst_n
9	INT2_EN_BUF_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT2. 1h [R/W] = A Buffer Underrun condition will trigger an interrupt on TX_INT2. Reset Source: rst_mod_g_rst_n
8	INT2_EN_FRAME_DONE	R/W	0h	Enable Frame Done interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT2. 1h [R/W] = A Frame Done event will trigger an interrupt on TX_INT2. Reset Source: rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved
3	INT1_EN_PING_TO	R/W	0h	Enable Ping Timer Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT1. 1h [R/W] = The ping timer event will trigger an interrupt on TX_INT1. Reset Source: rst_mod_g_rst_n

Table 14-24982. FSI_TX_CFG_TX_INT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT1_EN_BUF_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT1. 1h [R/W] = A Buffer Overrun condition will trigger an interrupt on TX_INT1. Reset Source: rst_mod_g_rst_n
1	INT1_EN_BUF_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT1. 1h [R/W] = A Buffer Underrun condition will trigger an interrupt on TX_INT1. Reset Source: rst_mod_g_rst_n
0	INT1_EN_FRAME_DONE	R/W	0h	Enable Frame Done interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT1. 1h [R/W] = A Frame Done event will trigger an interrupt on TX_INT1. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.16 FSI_TX_CFG_TX_DMA_CTRL Register

1 FSI_TX_CFG_TX_DMA_CTRL Register (Offset = 22h) [reset = 0h]

Transmit DMA event control register. Protected by LOCK field in TX_LOCK_CTRL register.

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Table 14-24983. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0022h**

Figure 14-8245. FSI_TX_CFG_TX_DMA_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							DMA_EVT_EN
R							R/W
0h							0h

Table 14-24985. FSI_TX_CFG_TX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	DMA_EVT_EN	R/W	0h	DMA Event Enable bit This bit will enable the DMA event to be generated upon the completion of a transmit frame. 0h [R/W] = A DMA event will not be generated. 1h [R/W] = A DMA event will be generated upon the completion of a transmitted frame. Note: The DMA event will only be generated for data frames. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.17 FSI_TX_CFG_TX_LOCK_CTRL Register

1 FSI_TX_CFG_TX_LOCK_CTRL Register (Offset = 24h) [reset = 0h]

Transmit lock control register

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Table 14-24986. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0024h**

Figure 14-8246. FSI_TX_CFG_TX_LOCK_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							

7	6	5	4	3	2	1	0
RESERVED_1							LOCK
R							R/W
0h							0h

Table 14-24988. FSI_TX_CFG_TX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register. Reset Source: rst_mod_g_rst_n
7:1	RESERVED_1	R	0h	Reserved
0	LOCK	R/W	0h	Control Register Lock Enable bit This bit locks the contents of all the transmit control registers that support a lock protection. Once locked, further writes will not take effect until a SYSRS has reset this register. Once set, further writes to this bit will be ignored. 0h [R/W] = Transmit control registers can be modified and are not locked. 1h [R/W] = Transmit control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.18 FSI_TX_CFG_RESERVED_3 Register

1 FSI_TX_CFG_RESERVED_3 Register (Offset = 26h) [reset = 0h]

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Table 14-24989. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0026h**

Figure 14-8247. FSI_TX_CFG_RESERVED_3 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24991. FSI_TX_CFG_RESERVED_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.19 FSI_TX_CFG_TX_EVT_STS Register

1 FSI_TX_CFG_TX_EVT_STS Register (Offset = 28h) [reset = 0h]

Transmit event and error status flag register

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Table 14-24992. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0028h**

Figure 14-8248. FSI_TX_CFG_TX_EVT_STS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-24994. FSI_TX_CFG_TX_EVT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	PING_TRIGGERED	R	0h	Ping Frame Triggered Flag Bit This bit indicates that a ping frame has been triggered. This bit is set by hardware when either the ping timer or an external trigger event have occured. Software can also force this bit to get set by Writing to the TX_EVT_FRC register. 0h [R] = A ping frame has not been triggered. 1h [R] = A ping frame has been triggered by either the ping timer or external trigger. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
2	BUF_OVERRUN	R	0h	Buffer Overrun Flag Bit This bit inditcates that buffer overrun has occured.Software can also force this bit to get set by Writing to the TX_EVT_FRC register. 0h [R] = Buffer Overrun has not occured. 1h [R] = Buffer Overrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
1	BUF_UNDERRUN	R	0h	Buffer Underrun Flag Bit This bit inditcates that buffer underrun has occured.Software can also force this bit to get set by Writing to the TX_EVT_FRC register. 0h [R] = Buffer Underrun has not occured. 1h [R] = Buffer Underrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset Source: rst_mod_g_rst_n

Table 14-24994. FSI_TX_CFG_TX_EVT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FRAME_DONE	R	0h	Frame Done Flag Bit This bit inditcates a Frame Done condition. This bit is set by hardware when a frame transmission has been completed. Software can also force this bit to get set by Writing to the TX_EVT_FRC register. 0h [R] = Frame Done condition has not occured. 1h [R] = Frame Done condition has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.20 FSI_TX_CFG_RESERVED_4 Register

1 FSI_TX_CFG_RESERVED_4 Register (Offset = 2Ah) [reset = 0h]

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Table 14-24995. Instance Table

Instance Name	Physical Address
FSITX1	**2361 002Ah**

Figure 14-8249. FSI_TX_CFG_RESERVED_4 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-24997. FSI_TX_CFG_RESERVED_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.21 FSI_TX_CFG_TX_EVT_CLR Register

1 FSI_TX_CFG_TX_EVT_CLR Register (Offset = 2Ch) [reset = 0h]

Transmit event and error clear register

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Table 14-24998. Instance Table

Instance Name	Physical Address
FSITX1	**2361 002Ch**

Figure 14-8250. FSI_TX_CFG_TX_EVT_CLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				W	W	W	W
0h				0h	0h	0h	0h

Table 14-25000. FSI_TX_CFG_TX_EVT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	PING_TRIGGERED	W	0h	Ping Frame Triggered Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Note: This bit may not always be cleared when Writing to the corresponding TX_EVT_CLR bit. If PING_TIMEOUT MODE is configured to be 0, a hardware ping timeout may occur when another frame is actively being transmitted. In this case, if this bit still shows as 1 after the clear bit is written then the ping frame has been triggered but not serviced. This bit does not indicate that the ping frame has been completely sent, only that it has been triggered by the timeout event. Reset Source: rst_mod_g_rst_n
2	BUF_OVERRUN	W	0h	Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
1	BUF_UNDERRUN	W	0h	Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n

Table 14-25000. FSI_TX_CFG_TX_EVT_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FRAME_DONE	W	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.22 FSI_TX_CFG_TX_EVT_FRC Register

1 FSI_TX_CFG_TX_EVT_FRC Register (Offset = 2Eh) [reset = 0h]

Transmit event and error flag force register

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Table 14-25001. Instance Table

Instance Name	Physical Address
FSITX1	**2361 002Eh**

Figure 14-8251. FSI_TX_CFG_TX_EVT_FRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				W	W	W	W
0h				0h	0h	0h	0h

Table 14-25003. FSI_TX_CFG_TX_EVT_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	PING_TRIGGERED	W	0h	Ping Frame Triggered Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding flag bit in the TX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
2	BUF_OVERRUN	W	0h	Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [R/W] = Writing a 0 to this bit will have no effect. 1h [R/W] = Force the corresponding flag bit in the TX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
1	BUF_UNDERRUN	W	0h	Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding flag bit in the TX_EVT_STS Register. Reset Source: rst_mod_g_rst_n

Table 14-25003. FSI_TX_CFG_TX_EVT_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FRAME_DONE	W	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding flag bit in the TX_EVT_STS Register. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.23 FSI_TX_CFG_TX_USER_CRC Register

1 FSI_TX_CFG_TX_USER_CRC Register (Offset = 30h) [reset = 0h]

Transmit user-defined CRC register

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Table 14-25004. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0030h**

Figure 14-8252. FSI_TX_CFG_TX_USER_CRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
USER_CRC							
R/W							
0h							

Table 14-25006. FSI_TX_CFG_TX_USER_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:0	USER_CRC	R/W	0h	User-defined CRC This register contains the 8-bit CRC value to be transmitted in the next frame if the transmission is set for user-defined CRC option [TX_OPER_CTRL_LO.SW_CRC = 1]. This register is ignored if the hardware CRC generation is enabled. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.24 FSI_TX_CFG_RESERVED_5 Register

1 FSI_TX_CFG_RESERVED_5 Register (Offset = 32h) [reset = 0h]

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Table 14-25007. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0032h**

Figure 14-8253. FSI_TX_CFG_RESERVED_5 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25009. FSI_TX_CFG_RESERVED_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.25 FSI_TX_CFG_RESERVED_6 Register

1 FSI_TX_CFG_RESERVED_6 Register (Offset = 34h) [reset = 0h]

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Table 14-25010. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0034h**

Figure 14-8254. FSI_TX_CFG_RESERVED_6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25012. FSI_TX_CFG_RESERVED_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.26 FSI_TX_CFG_RESERVED_7 Register

1 FSI_TX_CFG_RESERVED_7 Register (Offset = 38h) [reset = 0h]

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Table 14-25013. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0038h**

Figure 14-8255. FSI_TX_CFG_RESERVED_7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25015. FSI_TX_CFG_RESERVED_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.27 FSI_TX_CFG_RESERVED_8 Register

1 FSI_TX_CFG_RESERVED_8 Register (Offset = 3Ch) [reset = 0h]

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Table 14-25016. Instance Table

Instance Name	Physical Address
FSITX1	**2361 003Ch**

Figure 14-8256. FSI_TX_CFG_RESERVED_8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25018. FSI_TX_CFG_RESERVED_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.28 FSI_TX_CFG_TX_ECC_DATA Register

1 FSI_TX_CFG_TX_ECC_DATA Register (Offset = 40h) [reset = 0h]

Transmit ECC data register

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Table 14-25019. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0040h**

Figure 14-8257. FSI_TX_CFG_TX_ECC_DATA Name Register

31	30	29	28	27	26	25	24
DATA_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_LOW							
R/W							
0h							

Table 14-25021. FSI_TX_CFG_TX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA_HIGH	R/W	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register. Reset Source: rst_mod_g_rst_n
15:0	DATA_LOW	R/W	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.29 FSI_TX_CFG_TX_ECC_VAL Register

1 FSI_TX_CFG_TX_ECC_VAL Register (Offset = 44h) [reset = Ch]

Transmit ECC value register

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Table 14-25022. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0044h**

Figure 14-8258. FSI_TX_CFG_TX_ECC_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1	ECC_VAL						
R	R						
0h	Ch						

Table 14-25024. FSI_TX_CFG_TX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6:0	ECC_VAL	R	Ch	Computed ECC Value This field contains the ECC value computed using SEC-DED either for 16-bit or 32-bit data in the TX_ECC_DATA register. Reset Source: rst_mod_g_rst_n

14.9.4.5.2.30 FSI_TX_CFG_RESERVED_9_j Register

1 FSI_TX_CFG_RESERVED_9_j Register (Offset = 46h + formula) [reset = 0h]

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Offset = (j * 2h); where j = 0 to 28d

Table 14-25025. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0046h + formula**

Figure 14-8259. FSI_TX_CFG_RESERVED_9_j Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25027. FSI_TX_CFG_RESERVED_9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.5.2.31 FSI_TX_CFG_TX_BUF_BASE_j Register

1 FSI_TX_CFG_TX_BUF_BASE_j Register (Offset = 80h + formula) [reset = 0h]

Base address for transmit buffer

Return to Summary Table

Offset = (j * 2h); where j = 0 to 15d

Table 14-25028. Instance Table

Instance Name	Physical Address
FSITX1	**2361 0080h + formula**

Figure 14-8260. FSI_TX_CFG_TX_BUF_BASE_j Name Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
R/W							
0h							

Table 14-25030. FSI_TX_CFG_TX_BUF_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BASE_ADDRESS	R/W	0h	Transmit Data Buffer Base Address This is the base address of the 16-word data buffer used by the transmitter. Reset Source: rst_mod_g_rst_n

14.9.4.6 FSIRX

FSIRX

14.9.4.6.1 FSIRX Summaries

FSIRX Summaries

Table 14-25031. FSI_RX_CFG Registers, Base Address=2350 0000h, Length=256

Offset	Length	Register Name	FSIRX0 Physical Address	FSIRX1 Physical Address	FSIRX2 Physical Address
0h	16	FSI_RX_CFG_RX_MASTER_CTRL_ALTB_	2350 0000h	2351 0000h	2352 0000h
2h	16	FSI_RX_CFG_RESERVED_1	2350 0002h	2351 0002h	2352 0002h
4h	16	FSI_RX_CFG_RESERVED_2	2350 0004h	2351 0004h	2352 0004h
6h	16	FSI_RX_CFG_RESERVED_3	2350 0006h	2351 0006h	2352 0006h
8h	16	FSI_RX_CFG_RX_OPER_CTRL	2350 0008h	2351 0008h	2352 0008h
Ah	16	FSI_RX_CFG_RESERVED_4	2350 000Ah	2351 000Ah	2352 000Ah
Ch	16	FSI_RX_CFG_RX_FRAME_INFO	2350 000Ch	2351 000Ch	2352 000Ch
Eh	16	FSI_RX_CFG_RX_FRAME_TAG_UDATA	2350 000Eh	2351 000Eh	2352 000Eh
10h	16	FSI_RX_CFG_RX_DMA_CTRL	2350 0010h	2351 0010h	2352 0010h
12h	16	FSI_RX_CFG_RESERVED_5	2350 0012h	2351 0012h	2352 0012h
14h	16	FSI_RX_CFG_RX_EVT_STS_ALT1_	2350 0014h	2351 0014h	2352 0014h
16h	16	FSI_RX_CFG_RX_CRC_INFO	2350 0016h	2351 0016h	2352 0016h
18h	16	FSI_RX_CFG_RX_EVT_CLR_ALT1_	2350 0018h	2351 0018h	2352 0018h
1Ah	16	FSI_RX_CFG_RX_EVT_FRC_ALT1_	2350 001Ah	2351 001Ah	2352 001Ah
1Ch	16	FSI_RX_CFG_RX_BUF_PTR_LOAD	2350 001Ch	2351 001Ch	2352 001Ch
1Eh	16	FSI_RX_CFG_RX_BUF_PTR_STS	2350 001Eh	2351 001Eh	2352 001Eh
20h	16	FSI_RX_CFG_RX_FRAME_WD_CTRL	2350 0020h	2351 0020h	2352 0020h
22h	16	FSI_RX_CFG_RESERVED_6	2350 0022h	2351 0022h	2352 0022h
24h	32	FSI_RX_CFG_RX_FRAME_WD_REF	2350 0024h	2351 0024h	2352 0024h
28h	32	FSI_RX_CFG_RX_FRAME_WD_CNT	2350 0028h	2351 0028h	2352 0028h
2Ch	16	FSI_RX_CFG_RX_PING_WD_CTRL	2350 002Ch	2351 002Ch	2352 002Ch
2Eh	16	FSI_RX_CFG_RX_PING_TAG	2350 002Eh	2351 002Eh	2352 002Eh
30h	32	FSI_RX_CFG_RX_PING_WD_REF	2350 0030h	2351 0030h	2352 0030h
34h	32	FSI_RX_CFG_RX_PING_WD_CNT	2350 0034h	2351 0034h	2352 0034h
38h	16	FSI_RX_CFG_RX_INT1_CTRL_ALT1_	2350 0038h	2351 0038h	2352 0038h
3Ah	16	FSI_RX_CFG_RX_INT2_CTRL_ALT1_	2350 003Ah	2351 003Ah	2352 003Ah
3Ch	16	FSI_RX_CFG_RX_LOCK_CTRL	2350 003Ch	2351 003Ch	2352 003Ch
3Eh	16	FSI_RX_CFG_RESERVED_7	2350 003Eh	2351 003Eh	2352 003Eh

Table 14-25031. FSI_RX_CFG Registers, Base Address=2350 0000h, Length=256 (continued)

Offset	Length	Register Name	FSIRX0 Physical Address	FSIRX1 Physical Address	FSIRX2 Physical Address
40h	32	FSI_RX_CFG_RX_ECC_DATA	2350 0040h	2351 0040h	2352 0040h
44h	16	FSI_RX_CFG_RX_ECC_VAL	2350 0044h	2351 0044h	2352 0044h
46h	16	FSI_RX_CFG_RESERVED_8	2350 0046h	2351 0046h	2352 0046h
48h	32	FSI_RX_CFG_RX_ECC_SEC_DATA	2350 0048h	2351 0048h	2352 0048h
4Ch	16	FSI_RX_CFG_RX_ECC_LOG	2350 004Ch	2351 004Ch	2352 004Ch
4Eh	16	FSI_RX_CFG_RESERVED_9	2350 004Eh	2351 004Eh	2352 004Eh
50h	16	FSI_RX_CFG_RX_FRAME_TAG_CMP	2350 0050h	2351 0050h	2352 0050h
52h	16	FSI_RX_CFG_RX_PING_TAG_CMP	2350 0052h	2351 0052h	2352 0052h
54h	16	FSI_RX_CFG_RESERVED_10_J	2350 0054h + formula	2351 0054h + formula	2352 0054h + formula
60h	16	FSI_RX_CFG_RX_DLYLINE_CTRL	2350 0060h	2351 0060h	2352 0060h
62h	16	FSI_RX_CFG_RESERVED_11_J	2350 0062h + formula	2351 0062h + formula	2352 0062h + formula
70h	32	FSI_RX_CFG_RX_VIS_1	2350 0070h	2351 0070h	2352 0070h
74h	16	FSI_RX_CFG_RESERVED_12_J	2350 0074h + formula	2351 0074h + formula	2352 0074h + formula
80h	16	FSI_RX_CFG_RX_BUF_BASE_J	2350 0080h + formula	2351 0080h + formula	2352 0080h + formula

Table 14-25032. FSI_RX_CFG Registers, Base Address=2350 0000h, Length=256

Offset	Length	Register Name	FSIRX3 Physical Address	FSIRX4 Physical Address	FSIRX5 Physical Address
0h	16	FSI_RX_CFG_RX_MASTER_CTRL_ALTB_	2353 0000h	2354 0000h	2355 0000h
2h	16	FSI_RX_CFG_RESERVED_1	2353 0002h	2354 0002h	2355 0002h
4h	16	FSI_RX_CFG_RESERVED_2	2353 0004h	2354 0004h	2355 0004h
6h	16	FSI_RX_CFG_RESERVED_3	2353 0006h	2354 0006h	2355 0006h
8h	16	FSI_RX_CFG_RX_OPER_CTRL	2353 0008h	2354 0008h	2355 0008h
Ah	16	FSI_RX_CFG_RESERVED_4	2353 000Ah	2354 000Ah	2355 000Ah
Ch	16	FSI_RX_CFG_RX_FRAME_INFO	2353 000Ch	2354 000Ch	2355 000Ch
Eh	16	FSI_RX_CFG_RX_FRAME_TAG_UDATA	2353 000Eh	2354 000Eh	2355 000Eh
10h	16	FSI_RX_CFG_RX_DMA_CTRL	2353 0010h	2354 0010h	2355 0010h
12h	16	FSI_RX_CFG_RESERVED_5	2353 0012h	2354 0012h	2355 0012h
14h	16	FSI_RX_CFG_RX_EVT_STS_ALT1_	2353 0014h	2354 0014h	2355 0014h
16h	16	FSI_RX_CFG_RX_CRC_INFO	2353 0016h	2354 0016h	2355 0016h
18h	16	FSI_RX_CFG_RX_EVT_CLR_ALT1_	2353 0018h	2354 0018h	2355 0018h
1Ah	16	FSI_RX_CFG_RX_EVT_FRC_ALT1_	2353 001Ah	2354 001Ah	2355 001Ah
1Ch	16	FSI_RX_CFG_RX_BUF_PTR_LOAD	2353 001Ch	2354 001Ch	2355 001Ch
1Eh	16	FSI_RX_CFG_RX_BUF_PTR_STS	2353 001Eh	2354 001Eh	2355 001Eh
20h	16	FSI_RX_CFG_RX_FRAME_WD_CTRL	2353 0020h	2354 0020h	2355 0020h
22h	16	FSI_RX_CFG_RESERVED_6	2353 0022h	2354 0022h	2355 0022h

Table 14-25032. FSI_RX_CFG Registers, Base Address=2350 0000h, Length=256 (continued)

Offset	Length	Register Name	FSIRX3 Physical Address	FSIRX4 Physical Address	FSIRX5 Physical Address
24h	32	FSI_RX_CFG_RX_FRAME_WD_REF	2353 0024h	2354 0024h	2355 0024h
28h	32	FSI_RX_CFG_RX_FRAME_WD_CNT	2353 0028h	2354 0028h	2355 0028h
2Ch	16	FSI_RX_CFG_RX_PING_WD_CTRL	2353 002Ch	2354 002Ch	2355 002Ch
2Eh	16	FSI_RX_CFG_RX_PING_TAG	2353 002Eh	2354 002Eh	2355 002Eh
30h	32	FSI_RX_CFG_RX_PING_WD_REF	2353 0030h	2354 0030h	2355 0030h
34h	32	FSI_RX_CFG_RX_PING_WD_CNT	2353 0034h	2354 0034h	2355 0034h
38h	16	FSI_RX_CFG_RX_INT1_CTRL_ALT1_	2353 0038h	2354 0038h	2355 0038h
3Ah	16	FSI_RX_CFG_RX_INT2_CTRL_ALT1_	2353 003Ah	2354 003Ah	2355 003Ah
3Ch	16	FSI_RX_CFG_RX_LOCK_CTRL	2353 003Ch	2354 003Ch	2355 003Ch
3Eh	16	FSI_RX_CFG_RESERVED_7	2353 003Eh	2354 003Eh	2355 003Eh
40h	32	FSI_RX_CFG_RX_ECC_DATA	2353 0040h	2354 0040h	2355 0040h
44h	16	FSI_RX_CFG_RX_ECC_VAL	2353 0044h	2354 0044h	2355 0044h
46h	16	FSI_RX_CFG_RESERVED_8	2353 0046h	2354 0046h	2355 0046h
48h	32	FSI_RX_CFG_RX_ECC_SEC_DATA	2353 0048h	2354 0048h	2355 0048h
4Ch	16	FSI_RX_CFG_RX_ECC_LOG	2353 004Ch	2354 004Ch	2355 004Ch
4Eh	16	FSI_RX_CFG_RESERVED_9	2353 004Eh	2354 004Eh	2355 004Eh
50h	16	FSI_RX_CFG_RX_FRAME_TAG_CMP	2353 0050h	2354 0050h	2355 0050h
52h	16	FSI_RX_CFG_RX_PING_TAG_CMP	2353 0052h	2354 0052h	2355 0052h
54h	16	FSI_RX_CFG_RESERVED_10_J	2353 0054h + formula	2354 0054h + formula	2355 0054h + formula
60h	16	FSI_RX_CFG_RX_DLYLINE_CTRL	2353 0060h	2354 0060h	2355 0060h
62h	16	FSI_RX_CFG_RESERVED_11_J	2353 0062h + formula	2354 0062h + formula	2355 0062h + formula
70h	32	FSI_RX_CFG_RX_VIS_1	2353 0070h	2354 0070h	2355 0070h
74h	16	FSI_RX_CFG_RESERVED_12_J	2353 0074h + formula	2354 0074h + formula	2355 0074h + formula
80h	16	FSI_RX_CFG_RX_BUF_BASE_J	2353 0080h + formula	2354 0080h + formula	2355 0080h + formula

14.9.4.6.2 FSIRX Registers

FSIRX Registers

14.9.4.6.2.1 FSI_RX_CFG_RX_MASTER_CTRL_ALTB_ Register

1 FSI_RX_CFG_RX_MASTER_CTRL_ALTB_ Register (Offset = 0h) [reset = 0h]

Receive master control register

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Table 14-25033. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0000h**
FSIRX1	**2351 0000h**
FSIRX2	**2352 0000h**
FSIRX3	**2353 0000h**
FSIRX4	**2354 0000h**
FSIRX5	**2355 0000h**

Figure 14-8261. FSI_RX_CFG_RX_MASTER_CTRL_ALTB_ Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				INPUT_ISOLATE	SPI_PAIRING	INT_LOOPBACK	CORE_RST
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-25035. FSI_RX_CFG_RX_MASTER_CTRL_ALTB_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register. Reset Source: rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved
3	INPUT_ISOLATE	R/W	0h	When set to 1, the FSI RX inputs [RXCLK, RXD0 and RXD1] will be isolated from what is driven from the device pins and will be held at inactive level of '1'.This isolation facilitates the user to switch the RX inputs to a different set of device pins and hence any potential glitch that could occur during the process of switching will not affect the RX module itself. Reset Source: rst_mod_g_rst_n

Table 14-25035. FSI_RX_CFG_RX_MASTER_CTRL_ALTB_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SPI_PAIRING	R/W	0h	Clock Pairing for SPI-like Behavior Enable bit This bit enables the internal clock pairing with the FSI TX module. This feature internally connects the TXCLK to RXCLK allowing the FSI TX module, acting as a SPI master, to clock data into the receiver and out of the transmitter like a standard SPI module. This configuration is valid when the Module is in SPI mode only [RX_OPER_CTRL.SPI_MODE = 1] 0h [R/W] = SPI clock pairing is not enabled. 1h [R/W] = SPI clock pairing is enabled. The RXCLK will be internally connected to the TXCLK of the corresponding FSI module. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: rst_mod_g_rst_n
1	INT_LOOPBACK	R/W	0h	Internal Loopback Enable bit This bit enables the internal loopback functionality of the FSI receiver. By enabling this bit, a mux will select the signals coming directly from the corresponding FSI transmitter module rather than from the pins. 0h [R/W] = Internal loopback is disabled. The FSI RX module will receive signals coming from the pins. 1h [R/W] = Internal loopback is enabled. The FSI RX module will receive signals from the directly from FSI TX module rather than the pins. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: rst_mod_g_rst_n
0	CORE_RST	R/W	0h	Receiver Master Core Reset bit This bit controls the receiver master core reset. In order to receive any frame, this bit must be cleared. Note: For reset to take affect, the FSI RX module must be held in reset for at least 4 SYSCLK cycles. 0h [R/W] = Receiver core is not in reset and can receive frames. 1h [R/W] = Receiver core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.2 FSI_RX_CFG_RESERVED_1 Register

1 FSI_RX_CFG_RESERVED_1 Register (Offset = 2h) [reset = 0h]

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Table 14-25036. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0002h**
FSIRX1	**2351 0002h**
FSIRX2	**2352 0002h**
FSIRX3	**2353 0002h**
FSIRX4	**2354 0002h**
FSIRX5	**2355 0002h**

Figure 14-8262. FSI_RX_CFG_RESERVED_1 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25038. FSI_RX_CFG_RESERVED_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.3 FSI_RX_CFG_RESERVED_2 Register

1 FSI_RX_CFG_RESERVED_2 Register (Offset = 4h) [reset = 0h]

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Table 14-25039. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0004h**
FSIRX1	**2351 0004h**
FSIRX2	**2352 0004h**
FSIRX3	**2353 0004h**
FSIRX4	**2354 0004h**
FSIRX5	**2355 0004h**

Figure 14-8263. FSI_RX_CFG_RESERVED_2 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25041. FSI_RX_CFG_RESERVED_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.4 FSI_RX_CFG_RESERVED_3 Register

1 FSI_RX_CFG_RESERVED_3 Register (Offset = 6h) [reset = 0h]

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Table 14-25042. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0006h**
FSIRX1	**2351 0006h**
FSIRX2	**2352 0006h**
FSIRX3	**2353 0006h**
FSIRX4	**2354 0006h**
FSIRX5	**2355 0006h**

Figure 14-8264. FSI_RX_CFG_RESERVED_3 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25044. FSI_RX_CFG_RESERVED_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.5 FSI_RX_CFG_RX_OPER_CTRL Register

1 FSI_RX_CFG_RX_OPER_CTRL Register (Offset = 8h) [reset = 0h]

Receive operation control register. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25045. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0008h**
FSIRX1	**2351 0008h**
FSIRX2	**2352 0008h**
FSIRX3	**2353 0008h**
FSIRX4	**2354 0008h**
FSIRX5	**2355 0008h**

Figure 14-8265. FSI_RX_CFG_RX_OPER_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							PING_WD_RST_MODE
R							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_SEL	N_WORDS				SPI_MODE	DATA_WIDTH	
R/W	R/W				R/W	R/W	
0h	0h				0h	0h	

Table 14-25047. FSI_RX_CFG_RX_OPER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved
8	PING_WD_RST_MODE	R/W	0h	Ping Watchdog Timeout Mode Select bit This bit selects the mode by which the ping watchdog counter is reset. The watchdog counter can be reset and restarted only by ping frames or by any received frame. 0h [R/W] = The ping watchdog counter will reset and restart only by ping frames. 1h [R/W] = The ping watchdog counter will reset and restart by any received frame. Reset Source: rst_mod_g_rst_n
7	ECC_SEL	R/W	0h	ECC Data Width Select bit This bit selects between whether the ECC computation is done on 16-bit or 32-bit words. 0h [R/W] = 32-bit ECC is used. 1h [R/W] = 16-bit ECC is used. Reset Source: rst_mod_g_rst_n

Table 14-25047. FSI_RX_CFG_RX_OPER_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:3	N_WORDS	R/W	0h	Number of Words to Receive This field defines the number of words which will be received in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the transmitter. Set this bitfield to be one less than the number of words to be received. This value is only applicable when the frame type received is DATA_N_WORD. 0h [R/W] = 1 data word frame [16-bit data]. 1h [R/W] = 2 data word frame [32-bit data]. .. Fh [R/W] = 16 data word frame [256-bit data]. Reset Source: rst_mod_g_rst_n
2	SPI_MODE	R/W	0h	SPI Mode Enable bit This bit enables and disables the SPI compatibility mode of the FSI RX. The received data must be formatted as an FSI frame in order for the data to properly be received. SPI compatibility mode will allow FSI RX to receive data that is sent using SPI signal format. Refer to the applicable section in the FSI TRM chapter for more information. 0h [R/W] = FSI is in normal mode of operation. 1h [R/W] = FSI is operating in SPI compatibility mode. Reset Source: rst_mod_g_rst_n
1:0	DATA_WIDTH	R/W	0h	Receive Data Width Select bit These bits decide the number of data lines used for receiving data. 0h [R/W] = Data will be received on one data line, RXD0. 1h [R/W] = Data will be received on two data lines, RXD0 and RXD1. 2h, 3h [R/W] = Reserved Reset Source: rst_mod_g_rst_n

14.9.4.6.2.6 FSI_RX_CFG_RESERVED_4 Register

1 FSI_RX_CFG_RESERVED_4 Register (Offset = Ah) [reset = 0h]

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Table 14-25048. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 000Ah**
FSIRX1	**2351 000Ah**
FSIRX2	**2352 000Ah**
FSIRX3	**2353 000Ah**
FSIRX4	**2354 000Ah**
FSIRX5	**2355 000Ah**

Figure 14-8266. FSI_RX_CFG_RESERVED_4 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25050. FSI_RX_CFG_RESERVED_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.7 FSI_RX_CFG_RX_FRAME_INFO Register

1 FSI_RX_CFG_RX_FRAME_INFO Register (Offset = Ch) [reset = 0h]

Receive frame control register

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Table 14-25051. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 000Ch**
FSIRX1	**2351 000Ch**
FSIRX2	**2352 000Ch**
FSIRX3	**2353 000Ch**
FSIRX4	**2354 000Ch**
FSIRX5	**2355 000Ch**

Figure 14-8267. FSI_RX_CFG_RX_FRAME_INFO Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				FRAME_TYPE			
R				R			
0h				0h			

Table 14-25053. FSI_RX_CFG_RX_FRAME_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:0	FRAME_TYPE	R	0h	Received Frame Type This field indicates the type of frame that was successfully received last. 0000b [R/W] = A ping frame was received 0100b [R/W] = A DATA_1_WORD frame was received [16-bit data]. 0101b [R/W] = A DATA_2_WORD frame was received [32-bit data]. 0110b [R/W] = A DATA_4_WORD frame was received [64-bit data]. 0111b [R/W] = A DATA_6_WORD frame was received [96-bit data]. 0011b [R/W] = A DATA_N_WORD frame was received. The N_WORD field will determine the number of words [1 to 16] to be sent. The number of words received must equal the value programmed in RX_OPER_CTRL.N_WORDS. 1111b [R/W] = An error frame was received. This frame can be used during error conditions or any condition where the transmitter wants to signal the receiver for attention. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.8 FSI_RX_CFG_RX_FRAME_TAG_UDATA Register

1 FSI_RX_CFG_RX_FRAME_TAG_UDATA Register (Offset = Eh) [reset = 0h]

Receive frame tag and user data register

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Table 14-25054. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 000Eh**
FSIRX1	**2351 000Eh**
FSIRX2	**2352 000Eh**
FSIRX3	**2353 000Eh**
FSIRX4	**2354 000Eh**
FSIRX5	**2355 000Eh**

Figure 14-8268. FSI_RX_CFG_RX_FRAME_TAG_UDATA Name Register

15	14	13	12	11	10	9	8
USER_DATA							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1			FRAME_TAG				ZERO
R			R				R
0h			0h				0h

Table 14-25056. FSI_RX_CFG_RX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	USER_DATA	R	0h	Received User Data This field contains the 8-bit user data field of the last successfully received frame. Reset Source: rst_mod_g_rst_n
7:5	RESERVED_1	R	0h	Reserved
4:1	FRAME_TAG	R	0h	Received Frame Tag This field contains the 4-bit frame tag from the last successfully received frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag. Reset Source: rst_mod_g_rst_n
0	ZERO	R	0h	Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the FRAME_TAG and ZERO bits of this register [bits 4:0], application software can directly index into an array of 32-bit data. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.9 FSI_RX_CFG_RX_DMA_CTRL Register

1 FSI_RX_CFG_RX_DMA_CTRL Register (Offset = 10h) [reset = 0h]

Receive DMA event control register. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25057. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0010h**
FSIRX1	**2351 0010h**
FSIRX2	**2352 0010h**
FSIRX3	**2353 0010h**
FSIRX4	**2354 0010h**
FSIRX5	**2355 0010h**

Figure 14-8269. FSI_RX_CFG_RX_DMA_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							DMA_EVT_EN
R							R/W
0h							0h

Table 14-25059. FSI_RX_CFG_RX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	DMA_EVT_EN	R/W	0h	DMA Event Enable bit This bit will enable a DMA Event to be generated upon the completion of a frame reception. 0h [R/W] = A DMA event will not be generated. 1h [R/W] = A DMA event will be generated upon the reception of a frame. Note: The DMA event will only be generated for data frames. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.10 FSI_RX_CFG_RESERVED_5 Register

1 FSI_RX_CFG_RESERVED_5 Register (Offset = 12h) [reset = 0h]

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Table 14-25060. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0012h**
FSIRX1	**2351 0012h**
FSIRX2	**2352 0012h**
FSIRX3	**2353 0012h**
FSIRX4	**2354 0012h**
FSIRX5	**2355 0012h**

Figure 14-8270. FSI_RX_CFG_RESERVED_5 Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25062. FSI_RX_CFG_RESERVED_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.11 FSI_RX_CFG_RX_EVT_STS_ALT1_ Register

1 FSI_RX_CFG_RX_EVT_STS_ALT1_ Register (Offset = 14h) [reset = 0h]

Receive event and error status flag register

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Table 14-25063. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0014h**
FSIRX1	**2351 0014h**
FSIRX2	**2352 0014h**
FSIRX3	**2353 0014h**
FSIRX4	**2354 0014h**
FSIRX5	**2355 0014h**

Figure 14-8271. FSI_RX_CFG_RX_EVT_STS_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25065. FSI_RX_CFG_RX_EVT_STS_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	ERROR_TAG_MATCH	R	0h	Error Tag Match Flag This bit indicates that an error frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = No tag-matched error frame received. 1h [R] = A tag-matched error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
13	DATA_TAG_MATCH	R	0h	Data Tag Match Flag This bit indicates that a dataframe was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = No tag-matched data frame received. 1h [R] = A tag-matched data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n

Table 14-25065. FSI_RX_CFG_RX_EVT_STS_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PING_TAG_MATCH	R	0h	Ping Tag Match Flag This bit indicates that a ping frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = No tag-matched ping frame received. 1h [R] = A tag-matched ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
11	DATA_FRAME	R	0h	Data Frame Received Flag This bit indicates that an data frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = No data frame has been received. 1h [R] = A data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
10	FRAME_OVERRUN	R	0h	Frame Overrun Flag This bit indicates that a frame overrun condition has occured. This bit gets set to 1 when a new DATA/ERROR frame is received and the corresponding DATA_FRAME_RCVD/ERROR_FRAME_RCVD flag is still set to 1. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = Frame overrun has not ocurred. 1h [R] = Frame overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
9	PING_FRAME	R	0h	Ping Frame Received Flag This bit indicates that an ping frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = No ping frame has been received. 1h [R] = A ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
8	ERR_FRAME	R	0h	Error Frame Received Flag This bit indicates that an error frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = No error frame has been received. 1h [R] = An error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
7	BUF_UNDERRUN	R	0h	Receive Buffer Underrun Flag This bit indicates that a buffer underrun condition has occured in the receive buffer. This will happen when software reads the buffer which is empty and has no valid data. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = Receive Buffer Underrun has not ocurred. 1h [R] = Receive Buffer Underrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n

Table 14-25065. FSI_RX_CFG_RX_EVT_STS_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	FRAME_DONE	R	0h	Frame Done Flag This bit indicates that a frame has been successfully received without error. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = No frame has been successfully received. 1h [R] = A frame has been successfully received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
5	BUF_OVERRUN	R	0h	Receive Buffer Overrun Flag This bit indicates that a buffer overrun condition has occured in the receive buffer. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = Receive buffer overrun has not ocurred. 1h [R] = Receive buffer overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
4	EOF_ERR	R	0h	End-of-Frame Error Flag This bit indicates that an invalid end-of-frame bit pattern has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = Invalid end-of-frame has not been received. 1h [R] = Invalid end-of-frame has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
3	TYPE_ERR	R	0h	Frame Type Error Flag This bit inditcates that an invalid frame type has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = Invalid frame type has not been received. 1h [R] = Invalid frame type has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
2	CRC_ERR	R	0h	CRC Error Flag This bit indicates that a CRC error has occured. A CRC error will be generated on a data frame where the received CRC and the computed CRC do not match. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = CRC error has not occured. 1h [R] = CRC error has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n
1	FRAME_WD_TO	R	0h	Frame Watchdog Timeout Flag This bit indicates that the frame watchdog timer has timed out. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = Frame watchdog timeout has not occured. 1h [R] = Frame watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n

Table 14-25065. FSI_RX_CFG_RX_EVT_STS_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PING_WD_TO	R	0h	Ping Watchdog Timeout Flag This bit indicates that the ping watchdog timer has timed out. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h [R] = Ping watchdog timeout has not occured. 1h [R] = Ping watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.12 FSI_RX_CFG_RX_CRC_INFO Register

1 FSI_RX_CFG_RX_CRC_INFO Register (Offset = 16h) [reset = 0h]

Receive CRC info of received and computed CRC

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Table 14-25066. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0016h**
FSIRX1	**2351 0016h**
FSIRX2	**2352 0016h**
FSIRX3	**2353 0016h**
FSIRX4	**2354 0016h**
FSIRX5	**2355 0016h**

Figure 14-8272. FSI_RX_CFG_RX_CRC_INFO Name Register

15	14	13	12	11	10	9	8
CALC_CRC							
R							
0h							

7	6	5	4	3	2	1	0
RX_CRC							
R							
0h							

Table 14-25068. FSI_RX_CFG_RX_CRC_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CALC_CRC	R	0h	Harware Calculated CRC Value This bitfield contains the CRC value that was calculated on the last received data. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames. Reset Source: rst_mod_g_rst_n
7:0	RX_CRC	R	0h	Received CRC Value This bitfield contains the CRC value that was last received a frame. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.13 FSI_RX_CFG_RX_EVT_CLR_ALT1_ Register

1 FSI_RX_CFG_RX_EVT_CLR_ALT1_ Register (Offset = 18h) [reset = 0h]

Receive event and error clear register

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Table 14-25069. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0018h**
FSIRX1	**2351 0018h**
FSIRX2	**2352 0018h**
FSIRX3	**2353 0018h**
FSIRX4	**2354 0018h**
FSIRX5	**2355 0018h**

Figure 14-8273. FSI_RX_CFG_RX_EVT_CLR_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25071. FSI_RX_CFG_RX_EVT_CLR_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	ERROR_TAG_MATCH	W	0h	Error Tag Match Glag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
13	DATA_TAG_MATCH	W	0h	Data Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
12	PING_TAG_MATCH	W	0h	Ping Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n

Table 14-25071. FSI_RX_CFG_RX_EVT_CLR_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DATA_FRAME	W	0h	Data Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
10	FRAME_OVERRUN	W	0h	Frame Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
9	PING_FRAME	W	0h	Ping Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
8	ERR_FRAME	W	0h	Error Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
7	BUF_UNDERRUN	W	0h	Receive Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [R/W] = Writing a 0 to this bit will have no effect. 1h [R/W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
6	FRAME_DONE	W	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
5	BUF_OVERRUN	W	0h	Receive Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
4	EOF_ERR	W	0h	End-of-Frame Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
3	TYPE_ERR	W	0h	Frame Type Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n

Table 14-25071. FSI_RX_CFG_RX_EVT_CLR_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CRC_ERR	W	0h	CRC Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
1	FRAME_WD_TO	W	0h	Frame Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n
0	PING_WD_TO	W	0h	Ping Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.14 FSI_RX_CFG_RX_EVT_FRC_ALT1_ Register

1 FSI_RX_CFG_RX_EVT_FRC_ALT1_ Register (Offset = 1Ah) [reset = 0h]

Receive event and error flag force register

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Table 14-25072. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 001Ah**
FSIRX1	**2351 001Ah**
FSIRX2	**2352 001Ah**
FSIRX3	**2353 001Ah**
FSIRX4	**2354 001Ah**
FSIRX5	**2355 001Ah**

Figure 14-8274. FSI_RX_CFG_RX_EVT_FRC_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25074. FSI_RX_CFG_RX_EVT_FRC_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	ERROR_TAG_MATCH	W	0h	Error Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
13	DATA_TAG_MATCH	W	0h	Data Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
12	PING_TAG_MATCH	W	0h	Ping Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n

Table 14-25074. FSI_RX_CFG_RX_EVT_FRC_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DATA_FRAME	W	0h	Data Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
10	FRAME_OVERRUN	W	0h	Frame Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
9	PING_FRAME	W	0h	Ping Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
8	ERR_FRAME	W	0h	Error Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
7	BUF_UNDERRUN	W	0h	Receive Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
6	FRAME_DONE	W	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
5	BUF_OVERRUN	W	0h	Receive Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
4	EOF_ERR	W	0h	End-of-Frame Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n

Table 14-25074. FSI_RX_CFG_RX_EVT_FRC_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TYPE_ERR	W	0h	Frame Type Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
2	CRC_ERR	W	0h	CRC Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
1	FRAME_WD_TO	W	0h	Frame Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n
0	PING_WD_TO	W	0h	Ping Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.15 FSI_RX_CFG_RX_BUF_PTR_LOAD Register

1 FSI_RX_CFG_RX_BUF_PTR_LOAD Register (Offset = 1Ch) [reset = 0h]

Receive buffer pointer load register

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Table 14-25075. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 001Ch**
FSIRX1	**2351 001Ch**
FSIRX2	**2352 001Ch**
FSIRX3	**2353 001Ch**
FSIRX4	**2354 001Ch**
FSIRX5	**2355 001Ch**

Figure 14-8275. FSI_RX_CFG_RX_BUF_PTR_LOAD Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				BUF_PTR_LOAD			
R				R/W			
0h				0h			

Table 14-25077. FSI_RX_CFG_RX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:0	BUF_PTR_LOAD	R/W	0h	Buffer Pointer Load. This is the value to be loaded into the receive word pointer when written. This is to allow software to force the receiver to start storing the received data starting at a specific location in the buffer. NOTE: The value of the CURR_BUF_PTR in the RX_BUF_PTR_STS will not get reflected immediately. This will take effect only when there is a valid receive operation with incoming clocks after [3 RXCLK + 3 SYCLK] cycles. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.16 FSI_RX_CFG_RX_BUF_PTR_STS Register

1 FSI_RX_CFG_RX_BUF_PTR_STS Register (Offset = 1Eh) [reset = 0h]

Receive buffer pointer status register

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Table 14-25078. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 001Eh**
FSIRX1	**2351 001Eh**
FSIRX2	**2352 001Eh**
FSIRX3	**2353 001Eh**
FSIRX4	**2354 001Eh**
FSIRX5	**2355 001Eh**

Figure 14-8276. FSI_RX_CFG_RX_BUF_PTR_STS Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_2</td><td colspan="5">CURR_WORD_CNT</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_1</td><td colspan="4">CURR_BUF_PTR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-25080. FSI_RX_CFG_RX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12:8	CURR_WORD_CNT	R	0h	Words Available in the Receive Buffer This bitfield indicates the number of valid data words present in the receive buffer that have not been read by the application software. This bitfield is only valid when there is no active transfer. Note: This value will not be valid if there has been a buffer overrun or underrun condition. Reset Source: rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved
3:0	CURR_BUF_PTR	R	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.17 FSI_RX_CFG_RX_FRAME_WD_CTRL Register

1 FSI_RX_CFG_RX_FRAME_WD_CTRL Register (Offset = 20h) [reset = 0h]

Receive frame watchdog control register. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25081. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0020h**
FSIRX1	**2351 0020h**
FSIRX2	**2352 0020h**
FSIRX3	**2353 0020h**
FSIRX4	**2354 0020h**
FSIRX5	**2355 0020h**

Figure 14-8277. FSI_RX_CFG_RX_FRAME_WD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						FRAME_WD_EN	FRAME_WD_CNT_RST
R						R/W	R/W
0h						0h	0h

Table 14-25083. FSI_RX_CFG_RX_FRAME_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved
1	FRAME_WD_EN	R/W	0h	Frame Watchdog Counter Enable bit This bit will enable or disable the frame watchdog counter. The counter [RX_FRAME_WD_CNT] will begin counting from 0 when a valid start-of-frame pattern is received. When the reference value [RX_FRAME_WD_REF] is reached, it will generate a frame watchdog timeout event [RX_EVT_STS.FRAME_WD_TO] and the counter value will reset to 0 and continue counting on the next valid start-of-frame. 0h [R/W] = The frame watchdog counter is disabled and not running. 1h [R/W] = The frame watchdog counter logic is enabled and running. Reset Source: rst_mod_g_rst_n
0	FRAME_WD_CNT_RST	R/W	0h	Frame Watchdog Counter Reset bit This bit will reset the frame watchdog counter to 0. Writing a 1 to this bit will reset the frame watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h [R/W] = Clear the FRAME_WD_CNT_RST. 1h [W] = The frame watchdog counter will be reset to 0. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.18 FSI_RX_CFG_RESERVED_6 Register

1 FSI_RX_CFG_RESERVED_6 Register (Offset = 22h) [reset = 0h]

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Table 14-25084. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0022h**
FSIRX1	**2351 0022h**
FSIRX2	**2352 0022h**
FSIRX3	**2353 0022h**
FSIRX4	**2354 0022h**
FSIRX5	**2355 0022h**

Figure 14-8278. FSI_RX_CFG_RESERVED_6 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25086. FSI_RX_CFG_RESERVED_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.19 FSI_RX_CFG_RX_FRAME_WD_REF Register

1 FSI_RX_CFG_RX_FRAME_WD_REF Register (Offset = 24h) [reset = 0h]

Receive frame watchdog counter reference. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25087. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0024h**
FSIRX1	**2351 0024h**
FSIRX2	**2352 0024h**
FSIRX3	**2353 0024h**
FSIRX4	**2354 0024h**
FSIRX5	**2355 0024h**

Figure 14-8279. FSI_RX_CFG_RX_FRAME_WD_REF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FRAME_WD_REF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FRAME_WD_REF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FRAME_WD_REF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FRAME_WD_REF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25089. FSI_RX_CFG_RX_FRAME_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAME_WD_REF	R/W	0h	Frame Watchdog Counter Reference Value This is the 32-bit reference value for the frame watchdog timeout counter. The counter will count up starting from 0 at a valid start-of-frame pattern and continue counting until this value is reached. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.20 FSI_RX_CFG_RX_FRAME_WD_CNT Register

1 FSI_RX_CFG_RX_FRAME_WD_CNT Register (Offset = 28h) [reset = 0h]

Receive frame watchdog current count

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Table 14-25090. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0028h**
FSIRX1	**2351 0028h**
FSIRX2	**2352 0028h**
FSIRX3	**2353 0028h**
FSIRX4	**2354 0028h**
FSIRX5	**2355 0028h**

Figure 14-8280. FSI_RX_CFG_RX_FRAME_WD_CNT Name Register

31	30	29	28	27	26	25	24
FRAME_WD_CNT							
R							
0h							
23	22	21	20	19	18	17	16
FRAME_WD_CNT							
R							
0h							
15	14	13	12	11	10	9	8
FRAME_WD_CNT							
R							
0h							
7	6	5	4	3	2	1	0
FRAME_WD_CNT							
R							
0h							

Table 14-25092. FSI_RX_CFG_RX_FRAME_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAME_WD_CNT	R	0h	Frame Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the frame watchdog counter. This counter is reset to 0 in a variety of ways: A write to FRME_WD_CNT_RST, a match with FRAME_WD_REF, or the reception of a successful data frame. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.21 FSI_RX_CFG_RX_PING_WD_CTRL Register

1 FSI_RX_CFG_RX_PING_WD_CTRL Register (Offset = 2Ch) [reset = 0h]

Receive ping watchdog control register. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25093. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 002Ch**
FSIRX1	**2351 002Ch**
FSIRX2	**2352 002Ch**
FSIRX3	**2353 002Ch**
FSIRX4	**2354 002Ch**
FSIRX5	**2355 002Ch**

Figure 14-8281. FSI_RX_CFG_RX_PING_WD_CTRL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED_1</td><td>PING_WD_EN</td><td>PING_WD_RST</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25095. FSI_RX_CFG_RX_PING_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved
1	PING_WD_EN	R/W	0h	Ping Watchdog Counter Enable bit This bit will enable or disable the ping watchdog counter. The counter [RX_PING_WD_CNT] will begin counting from 0 when it is enabled. When the reference value [RX_PING_WD_REF] is reached, it will generate a ping watchdog timeout event [RX_EVT_STS.PING_WD_TO] and the counter value will reset to 0, and resume counting 0h [R/W] = The ping watchdog counter is disabled and not running. 1h [R/W] = The ping watchdog counter logic is enabled and running. Reset Source: rst_mod_g_rst_n
0	PING_WD_RST	R/W	0h	Ping Watchdog Counter Reset bit This bit will reset the ping watchdog counter to 0. Writing a 1 to this bit will reset the ping watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h [R/W] = Clear the PING_WD_RST. 1h [W] = The ping watchdog counter will be reset to 0. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.22 FSI_RX_CFG_RX_PING_TAG Register

1 FSI_RX_CFG_RX_PING_TAG Register (Offset = 2Eh) [reset = 0h]

Receive ping tag register

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Table 14-25096. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 002Eh**
FSIRX1	**2351 002Eh**
FSIRX2	**2352 002Eh**
FSIRX3	**2353 002Eh**
FSIRX4	**2354 002Eh**
FSIRX5	**2355 002Eh**

Figure 14-8282. FSI_RX_CFG_RX_PING_TAG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1			PING_TAG				ZERO
R			R				R
0h			0h				0h

Table 14-25098. FSI_RX_CFG_RX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_1	R	0h	Reserved
4:1	PING_TAG	R	0h	Received Ping Frame Tag This field contains the 4-bit frame tag from the last successfully received ping frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag. Reset Source: rst_mod_g_rst_n
0	ZERO	R	0h	Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the PING_TAG and ZERO bits of this register [bits 4:0], application software can directly index into an array of 32-bit data. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.23 FSI_RX_CFG_RX_PING_WD_REF Register

1 FSI_RX_CFG_RX_PING_WD_REF Register (Offset = 30h) [reset = 0h]

Receive ping watchdog counter reference. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25099. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0030h**
FSIRX1	**2351 0030h**
FSIRX2	**2352 0030h**
FSIRX3	**2353 0030h**
FSIRX4	**2354 0030h**
FSIRX5	**2355 0030h**

Figure 14-8283. FSI_RX_CFG_RX_PING_WD_REF Name Register

31	30	29	28	27	26	25	24
PING_WD_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
PING_WD_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
PING_WD_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
PING_WD_REF							
R/W							
0h							

Table 14-25101. FSI_RX_CFG_RX_PING_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PING_WD_REF	R/W	0h	Ping Watchdog Counter Reference Value This is the 32-bit reference value for the ping watchdog timeout counter. The counter will count up starting from 0 and continue counting until this value is reached. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.24 FSI_RX_CFG_RX_PING_WD_CNT Register

1 FSI_RX_CFG_RX_PING_WD_CNT Register (Offset = 34h) [reset = 0h]

Receive pingwatchdog current count

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Table 14-25102. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0034h**
FSIRX1	**2351 0034h**
FSIRX2	**2352 0034h**
FSIRX3	**2353 0034h**
FSIRX4	**2354 0034h**
FSIRX5	**2355 0034h**

Figure 14-8284. FSI_RX_CFG_RX_PING_WD_CNT Name Register

31	30	29	28	27	26	25	24
PING_WD_CNT							
R							
0h							
23	22	21	20	19	18	17	16
PING_WD_CNT							
R							
0h							
15	14	13	12	11	10	9	8
PING_WD_CNT							
R							
0h							
7	6	5	4	3	2	1	0
PING_WD_CNT							
R							
0h							

Table 14-25104. FSI_RX_CFG_RX_PING_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PING_WD_CNT	R	0h	Ping Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the ping watchdog counter. This counter is reset to 0 in a variety of ways: A write to PING_WD_RST, a match with PING_WD_REF, or the reception of a ping frame. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.25 FSI_RX_CFG_RX_INT1_CTRL_ALT1_ Register

1 FSI_RX_CFG_RX_INT1_CTRL_ALT1_ Register (Offset = 38h) [reset = 0h]

Receive interrupt control register for RX_INT1. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25105. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0038h**
FSIRX1	**2351 0038h**
FSIRX2	**2352 0038h**
FSIRX3	**2353 0038h**
FSIRX4	**2354 0038h**
FSIRX5	**2355 0038h**

Figure 14-8285. FSI_RX_CFG_RX_INT1_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	INT1_EN_ERROR_TAG_MATCH	INT1_EN_DATA_TAG_MATCH	INT1_EN_PING_TAG_MATCH	INT1_EN_DATA_FRAME	INT1_EN_FRAME_OVERRUN	INT1_EN_PING_FRAME	INT1_EN_ERR_FRAME
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT1_EN_UNDERRUN	INT1_EN_FRAME_DONE	INT1_EN_OVERRUN	INT1_EN_EOF_ERR	INT1_EN_TYPE_ERR	INT1_EN_CRC_ERR	INT1_EN_FRAME_WD_TO	INT1_EN_PING_WD_TO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25107. FSI_RX_CFG_RX_INT1_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	INT1_EN_ERROR_TAG_MATCH	R/W	0h	Enable Error Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = An error frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
13	INT1_EN_DATA_TAG_MATCH	R/W	0h	Enable Data Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A data frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n

Table 14-25107. FSI_RX_CFG_RX_INT1_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	INT1_EN_PING_TAG_MATCH	R/W	0h	Enable Ping Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A ping frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
11	INT1_EN_DATA_FRAME	R/W	0h	Enable Data Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A data frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
10	INT1_EN_FRAME_OVERRUN	R/W	0h	Enable Frame Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A frame overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
9	INT1_EN_PING_FRAME	R/W	0h	Enable Ping Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A ping frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
8	INT1_EN_ERR_FRAME	R/W	0h	Enable ERROR Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A error frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
7	INT1_EN_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A buffer underrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
6	INT1_EN_FRAME_DONE	R/W	0h	Enable Frame Done Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A frame done event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n

Table 14-25107. FSI_RX_CFG_RX_INT1_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT1_EN_OVERRUN	R/W	0h	Enable Receive Buffer Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A receive buffer overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
4	INT1_EN_EOF_ERR	R/W	0h	Enable End-of-Frame Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = An end-of-frame error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
3	INT1_EN_TYPE_ERR	R/W	0h	Enable Frame Type Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A frame type error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
2	INT1_EN_CRC_ERR	R/W	0h	Enable CRC Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A CRC error will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
1	INT1_EN_FRAME_WD_TO	R/W	0h	Enable Frame Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A frame watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
0	INT1_EN_PING_WD_TO	R/W	0h	Enable Ping Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A ping watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n

14.9.4.6.2.26 FSI_RX_CFG_RX_INT2_CTRL_ALT1_ Register

1 FSI_RX_CFG_RX_INT2_CTRL_ALT1_ Register (Offset = 3Ah) [reset = 0h]

Receive interrupt control register for RX_INT2. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25108. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 003Ah**
FSIRX1	**2351 003Ah**
FSIRX2	**2352 003Ah**
FSIRX3	**2353 003Ah**
FSIRX4	**2354 003Ah**
FSIRX5	**2355 003Ah**

Figure 14-8286. FSI_RX_CFG_RX_INT2_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	INT2_EN_ERROR_TAG_MATCH	INT2_EN_DATA_TAG_MATCH	INT2_EN_PING_TAG_MATCH	INT2_EN_DATA_FRAME	INT2_EN_FRAME_OVERRUN	INT2_EN_PING_FRAME	INT2_EN_ERR_FRAME
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT2_EN_UNDERRUN	INT2_EN_FRAME_DONE	INT2_EN_OVERRUN	INT2_EN_EOF_ERR	INT2_EN_TYPE_ERR	INT2_EN_CRC_ERR	INT2_EN_FRAME_WD_TO	INT2_EN_PING_WD_TO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25110. FSI_RX_CFG_RX_INT2_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	INT2_EN_ERROR_TAG_MATCH	R/W	0h	Enable Error Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = An error frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
13	INT2_EN_DATA_TAG_MATCH	R/W	0h	Enable Data Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A data frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n

Table 14-25110. FSI_RX_CFG_RX_INT2_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	INT2_EN_PING_TAG_MATCH	R/W	0h	Enable Ping Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A ping frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
11	INT2_EN_DATA_FRAME	R/W	0h	Enable Data Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A data frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
10	INT2_EN_FRAME_OVERRUN	R/W	0h	Enable Frame Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A frame overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
9	INT2_EN_PING_FRAME	R/W	0h	Enable Ping Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A ping frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
8	INT2_EN_ERR_FRAME	R/W	0h	Enable Error Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A error frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
7	INT2_EN_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A buffer underrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
6	INT2_EN_FRAME_DONE	R/W	0h	Enable Frame Done Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A frame done event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n

Table 14-25110. FSI_RX_CFG_RX_INT2_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT2_EN_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A buffer overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
4	INT2_EN_EOF_ERR	R/W	0h	Enable End-of-Frame Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = An end-of-frame error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
3	INT2_EN_TYPE_ERR	R/W	0h	Enable Frame Type Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A frame type error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
2	INT2_EN_CRC_ERR	R/W	0h	Enable CRC Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A CRC error will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
1	INT2_EN_FRAME_WD_TO	R/W	0h	Enable Frame Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A frame watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n
0	INT2_EN_PING_WD_TO	R/W	0h	Enable Ping Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A ping watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: rst_mod_g_rst_n

14.9.4.6.2.27 FSI_RX_CFG_RX_LOCK_CTRL Register

1 FSI_RX_CFG_RX_LOCK_CTRL Register (Offset = 3Ch) [reset = 0h]

Receive lock control register

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Table 14-25111. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 003Ch**
FSIRX1	**2351 003Ch**
FSIRX2	**2352 003Ch**
FSIRX3	**2353 003Ch**
FSIRX4	**2354 003Ch**
FSIRX5	**2355 003Ch**

Figure 14-8287. FSI_RX_CFG_RX_LOCK_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							LOCK
R							R/W
0h							0h

Table 14-25113. FSI_RX_CFG_RX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register. Reset Source: rst_mod_g_rst_n
7:1	RESERVED_1	R	0h	Reserved
0	LOCK	R/W	0h	Control Register Lock Enable bit This bit locks the contents of all the receive control registers that support a lock protection. Once locked, further writes will not take effect until SYSRS unlocks the register. Once set, further writes even to this bit will be ignored. 0h [R/W] = Receive control registers can be modified and are not locked. 1h [R/W] = Receive control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.28 FSI_RX_CFG_RESERVED_7 Register

1 FSI_RX_CFG_RESERVED_7 Register (Offset = 3Eh) [reset = 0h]

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Table 14-25114. Instance Table

Instance Name	Physical Address
FSIRX0	2350 003Eh
FSIRX1	2351 003Eh
FSIRX2	2352 003Eh
FSIRX3	2353 003Eh
FSIRX4	2354 003Eh
FSIRX5	2355 003Eh

Figure 14-8288. FSI_RX_CFG_RESERVED_7 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25116. FSI_RX_CFG_RESERVED_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.29 FSI_RX_CFG_RX_ECC_DATA Register

1 FSI_RX_CFG_RX_ECC_DATA Register (Offset = 40h) [reset = 0h]

Receive ECC data register

Return to Summary Table

Table 14-25117. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0040h**
FSIRX1	**2351 0040h**
FSIRX2	**2352 0040h**
FSIRX3	**2353 0040h**
FSIRX4	**2354 0040h**
FSIRX5	**2355 0040h**

Figure 14-8289. FSI_RX_CFG_RX_ECC_DATA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_HIGH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_HIGH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_LOW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_LOW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25119. FSI_RX_CFG_RX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA_HIGH	R/W	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register. Reset Source: rst_mod_g_rst_n
15:0	DATA_LOW	R/W	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.30 FSI_RX_CFG_RX_ECC_VAL Register

1 FSI_RX_CFG_RX_ECC_VAL Register (Offset = 44h) [reset = 0h]

Receive ECC value register

Return to Summary Table

Table 14-25120. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0044h**
FSIRX1	**2351 0044h**
FSIRX2	**2352 0044h**
FSIRX3	**2353 0044h**
FSIRX4	**2354 0044h**
FSIRX5	**2355 0044h**

Figure 14-8290. FSI_RX_CFG_RX_ECC_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1	ECC_VAL						
R	R/W						
0h	0h						

Table 14-25122. FSI_RX_CFG_RX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6:0	ECC_VAL	R/W	0h	ECC Value for SEC-DED check This field contains the ECC value to be used for SEC-DED either for 16-bit or 32-bit data in the RX_ECC_DATA register. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.31 FSI_RX_CFG_RESERVED_8 Register

1 FSI_RX_CFG_RESERVED_8 Register (Offset = 46h) [reset = 0h]

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Table 14-25123. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0046h**
FSIRX1	**2351 0046h**
FSIRX2	**2352 0046h**
FSIRX3	**2353 0046h**
FSIRX4	**2354 0046h**
FSIRX5	**2355 0046h**

Figure 14-8291. FSI_RX_CFG_RESERVED_8 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25125. FSI_RX_CFG_RESERVED_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.32 FSI_RX_CFG_RX_ECC_SEC_DATA Register

1 FSI_RX_CFG_RX_ECC_SEC_DATA Register (Offset = 48h) [reset = 0h]

Receive ECC corrected data register

Return to Summary Table

Table 14-25126. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0048h**
FSIRX1	**2351 0048h**
FSIRX2	**2352 0048h**
FSIRX3	**2353 0048h**
FSIRX4	**2354 0048h**
FSIRX5	**2355 0048h**

Figure 14-8292. FSI_RX_CFG_RX_ECC_SEC_DATA Name Register

31	30	29	28	27	26	25	24
SEC_DATA							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SEC_DATA							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SEC_DATA							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_DATA							
R							
0h							

Table 14-25128. FSI_RX_CFG_RX_ECC_SEC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SEC_DATA	R	0h	ECC Single Error Corrected Data The ECC corrected data will be available in this register. This value is valid only when there are no bit errors, or a single bit error was detected. Otherwise, the contents of this register are invalid and should not be used. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.33 FSI_RX_CFG_RX_ECC_LOG Register

1 FSI_RX_CFG_RX_ECC_LOG Register (Offset = 4Ch) [reset = 3h]

Receive ECC log and status register

Return to Summary Table

Table 14-25129. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 004Ch**
FSIRX1	**2351 004Ch**
FSIRX2	**2352 004Ch**
FSIRX3	**2353 004Ch**
FSIRX4	**2354 004Ch**
FSIRX5	**2355 004Ch**

Figure 14-8293. FSI_RX_CFG_RX_ECC_LOG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						MBE	SBE
R						R	R
0h						1h	1h

Table 14-25131. FSI_RX_CFG_RX_ECC_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved
1	MBE	R	1h	Multiple Bit Errors Detected This bit indicates the occurrence of multiple bit errors.The data is corrupted and cannot be corrected. If this bit is set, the data present in RX_ECC_SEC_DATA is invalid and should not be used. 0h [R] Multiple Bit Errors were not detected. Check the SBE bit for single bit errors. 1h [R] Multiple Bit Errors were detected. The data is not able to be corrected. The value present in RX_ECC_SEC_DATA is invalid and should not be used. Reset Source: rst_mod_g_rst_n
0	SBE	R	1h	Single Bit Error Detected This bit indicates the occurrence of a single bit error in the data. The data is autocorrected and placed into the RX_ECC_SEC_DATA register. This bit is valid only if MBE is 0. 0h [R] No bit errors were detected. The value in RX_ECC_SEC_DATA is correct. 1h [R] A single bit error was detected and corrected. The corrected data is present in RX_ECC_SEC_DATA. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.34 FSI_RX_CFG_RESERVED_9 Register

1 FSI_RX_CFG_RESERVED_9 Register (Offset = 4Eh) [reset = 0h]

Return to Summary Table

Table 14-25132. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 004Eh**
FSIRX1	**2351 004Eh**
FSIRX2	**2352 004Eh**
FSIRX3	**2353 004Eh**
FSIRX4	**2354 004Eh**
FSIRX5	**2355 004Eh**

Figure 14-8294. FSI_RX_CFG_RESERVED_9 Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25134. FSI_RX_CFG_RESERVED_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.35 FSI_RX_CFG_RX_FRAME_TAG_CMP Register

1 FSI_RX_CFG_RX_FRAME_TAG_CMP Register (Offset = 50h) [reset = 0h]

Receive frame tag compare register. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25135. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0050h**
FSIRX1	**2351 0050h**
FSIRX2	**2352 0050h**
FSIRX3	**2353 0050h**
FSIRX4	**2354 0050h**
FSIRX5	**2355 0050h**

Figure 14-8295. FSI_RX_CFG_RX_FRAME_TAG_CMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1						BROADCAST_EN	CMP_EN
R						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TAG_MASK				TAG_REF			
R/W				R/W			
0h				0h			

Table 14-25137. FSI_RX_CFG_RX_FRAME_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9	BROADCAST_EN	R/W	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the frame tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h [R/W] Broadcast frame match disabled. 1h [R/W] Broadcast frame match enabled. Reset Source: rst_mod_g_rst_n
8	CMP_EN	R/W	0h	Frame Tag Compare Enable bit Set this bit to enable the comparison of an incoming frame tag and the value stored in the frame tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming frame tag will trigger the apprpriate frame tag match event. 0h [R/W] Frame tag comparison is disabled. 1h [R/W] Frame tag comparison is enabled. Reset Source: rst_mod_g_rst_n
7:4	TAG_MASK	R/W	0h	Frame Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for non-ping frames. Reset Source: rst_mod_g_rst_n

Table 14-25137. FSI_RX_CFG_RX_FRAME_TAG_CMP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	TAG_REF	R/W	0h	Frame Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming frame tag. This reference value is used only for non-ping frames. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.36 FSI_RX_CFG_RX_PING_TAG_CMP Register

1 FSI_RX_CFG_RX_PING_TAG_CMP Register (Offset = 52h) [reset = 0h]

Receive ping tag compare register. Protected by LOCK field in RX_LOCK_CTRL register.

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Table 14-25138. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0052h**
FSIRX1	**2351 0052h**
FSIRX2	**2352 0052h**
FSIRX3	**2353 0052h**
FSIRX4	**2354 0052h**
FSIRX5	**2355 0052h**

Figure 14-8296. FSI_RX_CFG_RX_PING_TAG_CMP Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_1</td><td>BROADCAST_EN</td><td>CMP_EN</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">TAG_MASK</td><td colspan="4">TAG_REF</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-25140. FSI_RX_CFG_RX_PING_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9	BROADCAST_EN	R/W	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the ping tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h [R/W] Broadcast frame match disabled. 1h [R/W] Broadcast frame match enabled. Reset Source: rst_mod_g_rst_n
8	CMP_EN	R/W	0h	Ping Tag Compare Enable bit Set this bit to enable the comparison of an incoming ping tag and the value stored in the ping tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming ping tag will trigger a ping frame tag match event. 0h [R/W] Ping tag comparison is disabled. 1h [R/W] Ping tag comparison is enabled. Reset Source: rst_mod_g_rst_n
7:4	TAG_MASK	R/W	0h	Ping Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming ping frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for ping frames. Reset Source: rst_mod_g_rst_n

Table 14-25140. FSI_RX_CFG_RX_PING_TAG_CMP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	TAG_REF	R/W	0h	Ping Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming ping tag. This reference value is used only for ping frames. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.37 FSI_RX_CFG_RESERVED_10_j Register

1 FSI_RX_CFG_RESERVED_10_j Register (Offset = 54h + formula) [reset = 0h]

Return to Summary Table

Offset = (j * 2h); where j = 0 to 5d

Table 14-25141. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0054h + formula**
FSIRX1	**2351 0054h + formula**
FSIRX2	**2352 0054h + formula**
FSIRX3	**2353 0054h + formula**
FSIRX4	**2354 0054h + formula**
FSIRX5	**2355 0054h + formula**

Figure 14-8297. FSI_RX_CFG_RESERVED_10_j Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25143. FSI_RX_CFG_RESERVED_10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.38 FSI_RX_CFG_RX_DLYLINE_CTRL Register

1 FSI_RX_CFG_RX_DLYLINE_CTRL Register (Offset = 60h) [reset = 0h]

Receive delay line control register. Protected by LOCK field in RX_LOCK_CTRL register.

Return to Summary Table

Table 14-25144. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0060h**
FSIRX1	**2351 0060h**
FSIRX2	**2352 0060h**
FSIRX3	**2353 0060h**
FSIRX4	**2354 0060h**
FSIRX5	**2355 0060h**

Figure 14-8298. FSI_RX_CFG_RX_DLYLINE_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	RXD1_DLY					RXD0_DLY	
R	R/W					R/W	
0h	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RXD0_DLY			RXCLK_DLY				
R/W			R/W				
0h			0h				

Table 14-25146. FSI_RX_CFG_RX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:10	RXD1_DLY	R/W	0h	Delay Line Tap Select for RXD1 This bitfield selects the number of delay elements inserted into the RXD1 path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the RXD1 path. RXD1 is taken directly from the pin. 1h [R/W] One delay element is included in the RXD1 path. 2h [R/W] Two delay elements are included in the RXD1 path. ... 1Fh [R/W] 31 delay elements are included in the RXD1 path, the maximum. Reset Source: rst_mod_g_rst_n
9:5	RXD0_DLY	R/W	0h	Delay Line Tap Select for RXD0 This bitfield selects the number of delay elements inserted into the RXD0 path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the RXD0 path. RXD0 is taken directly from the pin. 1h [R/W] One delay element is included in the RXD0 path. 2h [R/W] Two delay elements are included in the RXD0 path. ... 1Fh [R/W] 31 delay elements are included in the RXD0 path, the maximum. Reset Source: rst_mod_g_rst_n

Table 14-25146. FSI_RX_CFG_RX_DLYLINE_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	RXCLK_DLY	R/W	0h	Delay Line Tap Select for RXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the RXCLK path. RXCLK is taken directly from the pin. 1h [R/W] One delay element is included in the RXCLK path. 2h [R/W] Two delay elements are included in the RXCLK path. ... 1Fh [R/W] 31 delay elements are included in the RXCLK path, the maximum. Reset Source: rst_mod_g_rst_n

14.9.4.6.2.39 FSI_RX_CFG_RESERVED_11_j Register

1 FSI_RX_CFG_RESERVED_11_j Register (Offset = 62h + formula) [reset = 0h]

Return to Summary Table

Offset = (j * 2h); where j = 0 to 6d

Table 14-25147. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0062h + formula**
FSIRX1	**2351 0062h + formula**
FSIRX2	**2352 0062h + formula**
FSIRX3	**2353 0062h + formula**
FSIRX4	**2354 0062h + formula**
FSIRX5	**2355 0062h + formula**

Figure 14-8299. FSI_RX_CFG_RESERVED_11_j Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25149. FSI_RX_CFG_RESERVED_11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.40 FSI_RX_CFG_RX_VIS_1 Register

1 FSI_RX_CFG_RX_VIS_1 Register (Offset = 70h) [reset = 0h]

Receive debug visibility register 1

Return to Summary Table

Table 14-25150. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0070h**
FSIRX1	**2351 0070h**
FSIRX2	**2352 0070h**
FSIRX3	**2353 0070h**
FSIRX4	**2354 0070h**
FSIRX5	**2355 0070h**

Figure 14-8300. FSI_RX_CFG_RX_VIS_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED_2</td><td>RX_CORE_STS</td><td colspan="3">RESERVED_1</td></tr>
<tr><td colspan="4">R</td><td>R</td><td colspan="3">R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-25152. FSI_RX_CFG_RX_VIS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_2	R	0h	Reserved
3	RX_CORE_STS	R	0h	Receiver Core Status bit This bit indicates the status of the receiver core. If this bit is set, the receiver should undergo a reset and subsequent resynchronization with the transmitter. This bit will be always be set when the receiver has detected and end of frame error or a frame type error. This bit can also be set if the receiver becomes corrupted due to noise on the signal lines. If the receiver has experienced a ping watchdog or frame watchdog timeout, this bit should be read to determine if the cause was due to a corrupt transaction, thus putting the receiver core into an unrecoverable state. Only a soft reset will reset the recevier core and thus reset this bit. 0h [R] The receiver core is operating normally. 1h [R] The receiver core has entered into an error state and should be reset. Reset Source: rst_mod_g_rst_n

Table 14-25152. FSI_RX_CFG_RX_VIS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED_1	R	0h	Reserved

14.9.4.6.2.41 FSI_RX_CFG_RESERVED_12_j Register

1 FSI_RX_CFG_RESERVED_12_j Register (Offset = 74h + formula) [reset = 0h]

Return to Summary Table

Offset = (j * 2h); where j = 0 to 5d

Table 14-25153. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0074h + formula**
FSIRX1	**2351 0074h + formula**
FSIRX2	**2352 0074h + formula**
FSIRX3	**2353 0074h + formula**
FSIRX4	**2354 0074h + formula**
FSIRX5	**2355 0074h + formula**

Figure 14-8301. FSI_RX_CFG_RESERVED_12_j Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-25155. FSI_RX_CFG_RESERVED_12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.9.4.6.2.42 FSI_RX_CFG_RX_BUF_BASE_j Register

1 FSI_RX_CFG_RX_BUF_BASE_j Register (Offset = 80h + formula) [reset = 0h]

Base address for receive data buffer

Return to Summary Table

Offset = (j * 2h); where j = 0 to 15d

Table 14-25156. Instance Table

Instance Name	Physical Address
FSIRX0	**2350 0080h + formula**
FSIRX1	**2351 0080h + formula**
FSIRX2	**2352 0080h + formula**
FSIRX3	**2353 0080h + formula**
FSIRX4	**2354 0080h + formula**
FSIRX5	**2355 0080h + formula**

Figure 14-8302. FSI_RX_CFG_RX_BUF_BASE_j Name Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
R							
0h							

Table 14-25158. FSI_RX_CFG_RX_BUF_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BASE_ADDRESS	R	0h	Receive Data Buffer Base Address This is the base address of the 16-word data buffer used by the receiver. Reset Source: rst_mod_g_rst_n

14.9.5 Timer Modules Registers

14.9.5.1 GTC

GTC

14.9.5.1.1 GTC Summaries

GTC Summaries

Table 14-25159. GTC_CFG0 Registers, Base Address=00A8 0000h, Length=1024

Offset	Length	Register Name	GTC0 Physical Address
0h	32	GTC_CFG0_PID	00A8 0000h
4h	32	GTC_CFG0_GTC_PID	00A8 0004h
8h	32	GTC_CFG0_PUSHEVT	00A8 0008h

Table 14-25160. GTC_CFG1 Registers, Base Address=00A9 0000h, Length=16384

Offset	Length	Register Name	GTC0 Physical Address
0h	32	GTC_CFG1_CNTCR	00A9 0000h
4h	32	GTC_CFG1_CNTSR	00A9 0004h
8h	32	GTC_CFG1_CNTCV_LO	00A9 0008h
Ch	32	GTC_CFG1_CNTCV_HI	00A9 000Ch
20h	32	GTC_CFG1_CNTFID0	00A9 0020h
24h	32	GTC_CFG1_CNTFID1	00A9 0024h

Table 14-25161. GTC_CFG2 Registers, Base Address=00AA 0000h, Length=16384

Offset	Length	Register Name	GTC0 Physical Address
0h	32	GTC_CFG2_CNTCVS_LO	00AA 0000h
4h	32	GTC_CFG2_CNTCVS_HI	00AA 0004h

Table 14-25162. GTC_CFG3 Registers, Base Address=00AB 0000h, Length=16384

Offset	Length	Register Name	GTC0 Physical Address
8h	32	GTC_CFG3_CNTTIDR	00AB 0008h

14.9.5.1.2 GTC Registers

GTC Registers

14.9.5.1.2.1 GTC_CFG0_PID Register

1 GTC_CFG0_PID Register (Offset = 0h) [reset = 61800209h]

PID register

Return to Summary Table

Table 14-25163. Instance Table

Instance Name	Physical Address
GTC0	**00A8 0000h**

Figure 14-8303. GTC_CFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">9h</td></tr>
</table>

Table 14-25165. GTC_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	9h	Reset Source: mod_g_rst_n

14.9.5.1.2.2 GTC_CFG0_GTC_PID Register

1 GTC_CFG0_GTC_PID Register (Offset = 4h) [reset = 661A0000h]

Return to Summary Table

Table 14-25166. Instance Table

Instance Name	Physical Address
GTC0	**00A8 0004h**

Figure 14-8304. GTC_CFG0_GTC_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">GTC_PID_SCHEME</td><td colspan="2">GTC_PID_BU</td><td colspan="4">GTC_PID_FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">61Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GTC_PID_FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">61Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">GTC_PID_R_RTL</td><td colspan="3">GTC_PID_X_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">X</td><td colspan="3">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">GTC_PID_CUSTOM</td><td colspan="6">GTC_PID_Y_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">X</td><td colspan="6">X</td></tr>
</table>

Table 14-25168. GTC_CFG0_GTC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	GTC_PID_SCHEME	R	1h	PID follows new scheme Reset Source: mod_por_rst_n
29:28	GTC_PID_BU	R	2h	Business unit - Processors Reset Source: mod_por_rst_n
27:16	GTC_PID_FUNC	R	61Ah	Module functional identifier - GTC module Reset Source: mod_por_rst_n
15:11	GTC_PID_R_RTL	R	X	RTL revision number - actual value determined by RTL Reset Source: mod_por_rst_n
10:8	GTC_PID_X_MAJOR	R	X	Major revision number - actual value determined by RTL Reset Source: mod_por_rst_n
7:6	GTC_PID_CUSTOM	R	X	Custom revision number - actual value determined by RTL Reset Source: mod_por_rst_n
5:0	GTC_PID_Y_MINOR	R	X	Minor revision number - actual value determined by RTL Reset Source: mod_por_rst_n

14.9.5.1.2.3 GTC_CFG0_PUSHEVT Register

1 GTC_CFG0_PUSHEVT Register (Offset = 8h) [reset = 0h]

Return to Summary Table

Table 14-25169. Instance Table

Instance Name	Physical Address
GTC0	**00A8 0008h**

Figure 14-8305. GTC_CFG0_PUSHEVT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PUSHEVT_EXPBIT_SEL					
NONE		R/W					
0h		0h					

Table 14-25171. GTC_CFG0_PUSHEVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PUSHEVT_EXPBIT_SEL	R/W	0h	Selects which bit [63:0] of the System Counter value is exported on the push_evt output. This field controls the 64:1 mux that drives the push_evt output. Reset Source: mod_por_rst_n

14.9.5.1.2.4 GTC_CFG1_CNTCR Register

1 GTC_CFG1_CNTCR Register (Offset = 0h) [reset = 0h]

Return to Summary Table

Table 14-25172. Instance Table

Instance Name	Physical Address
GTC0	**00A9 0000h**

Figure 14-8306. GTC_CFG1_CNTCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CNTCR_FCREQ</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CNTCR_FCREQ</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CNTCR_FCREQ</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CNTCR_HDBG</td><td>CNTCR_EN</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25174. GTC_CFG1_CNTCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CNTCR_FCREQ	R	0h	Frequency Change Request Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1	CNTCR_HDBG	R/W	0h	Halt on Debug Reset Source: mod_por_rst_n
0	CNTCR_EN	R/W	0h	Enable System Counter Reset Source: mod_por_rst_n

14.9.5.1.2.5 GTC_CFG1_CNTSR Register

1 GTC_CFG1_CNTSR Register (Offset = 4h) [reset = 0h]

Return to Summary Table

Table 14-25175. Instance Table

Instance Name	Physical Address
GTC0	**00A9 0004h**

Figure 14-8307. GTC_CFG1_CNTSR Name Register

31	30	29	28	27	26	25	24
CNTSR_FCACK							
R							
0h							
23	22	21	20	19	18	17	16
CNTSR_FCACK							
R							
0h							
15	14	13	12	11	10	9	8
CNTSR_FCACK							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						CNTSR_DBGH	RESERVED
NONE						R	NONE
0h						X	0h

Table 14-25177. GTC_CFG1_CNTSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CNTSR_FCACK	R	0h	Frequency Change Ackowledge Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1	CNTSR_DBGH	R	X	Debug Halt Reset Source: mod_por_rst_n
0	RESERVED	NONE	0h	Reserved

14.9.5.1.2.6 GTC_CFG1_CNTCV_LO Register

1 GTC_CFG1_CNTCV_LO Register (Offset = 8h) [reset = 0h]

Return to Summary Table

Table 14-25178. Instance Table

Instance Name	Physical Address
GTC0	**00A9 0008h**

Figure 14-8308. GTC_CFG1_CNTCV_LO Name Register

31	30	29	28	27	26	25	24
CNTCV_LO_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCV_LO_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCV_LO_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCV_LO_COUNTVALUE							
R							
X							

Table 14-25180. GTC_CFG1_CNTCV_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCV_LO_COUNTVALUE	R	X	Indicates bits [31:0] of the System Counter value. Reset Source: mod_por_rst_n

14.9.5.1.2.7 GTC_CFG1_CNTCV_HI Register

1 GTC_CFG1_CNTCV_HI Register (Offset = Ch) [reset = 0h]

Return to Summary Table

Table 14-25181. Instance Table

Instance Name	Physical Address
GTC0	**00A9 000Ch**

Figure 14-8309. GTC_CFG1_CNTCV_HI Name Register

31	30	29	28	27	26	25	24
CNTCV_HI_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCV_HI_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCV_HI_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCV_HI_COUNTVALUE							
R							
X							

Table 14-25183. GTC_CFG1_CNTCV_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCV_HI_COUNTVALUE	R	X	Indicates bits [63:32] of the System Counter value. Reset Source: mod_por_rst_n

14.9.5.1.2.8 GTC_CFG1_CNTFID0 Register

1 GTC_CFG1_CNTFID0 Register (Offset = 20h) [reset = 0h]

Return to Summary Table

Table 14-25184. Instance Table

Instance Name	Physical Address
GTC0	**00A9 0020h**

Figure 14-8310. GTC_CFG1_CNTFID0 Name Register

31	30	29	28	27	26	25	24
CNTFID0_FREQVALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
CNTFID0_FREQVALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
CNTFID0_FREQVALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTFID0_FREQVALUE							
R/W							
0h							

Table 14-25186. GTC_CFG1_CNTFID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTFID0_FREQVALUE	R/W	0h	Indicates the base update frequency of the System Counter in Hz. Reset Source: mod_por_rst_n

14.9.5.1.2.9 GTC_CFG1_CNTFID1 Register

1 GTC_CFG1_CNTFID1 Register (Offset = 24h) [reset = 0h]

Return to Summary Table

Table 14-25187. Instance Table

Instance Name	**Physical Address**
GTC0	**00A9 0024h**

Figure 14-8311. GTC_CFG1_CNTFID1 Name Register

31	30	29	28	27	26	25	24
CNTFID1_FREQVALUE							
R							
0h							
23	22	21	20	19	18	17	16
CNTFID1_FREQVALUE							
R							
0h							
15	14	13	12	11	10	9	8
CNTFID1_FREQVALUE							
R							
0h							
7	6	5	4	3	2	1	0
CNTFID1_FREQVALUE							
R							
0h							

Table 14-25189. GTC_CFG1_CNTFID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTFID1_FREQVALUE	R	0h	Frequency table end indicator Reset Source: mod_por_rst_n

14.9.5.1.2.10 GTC_CFG2_CNTCVS_LO Register

1 GTC_CFG2_CNTCVS_LO Register (Offset = 0h) [reset = 0h]

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Table 14-25190. Instance Table

Instance Name	**Physical Address**
GTC0	**00AA 0000h**

Figure 14-8312. GTC_CFG2_CNTCVS_LO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CNTCVS_LO_COUNTVALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CNTCVS_LO_COUNTVALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CNTCVS_LO_COUNTVALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CNTCVS_LO_COUNTVALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-25192. GTC_CFG2_CNTCVS_LO Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	CNTCVS_LO_COUNTVALUE	R	X	Indicates bits [31:0] of the System Counter value. Reset Source: mod_por_rst_n

14.9.5.1.2.11 GTC_CFG2_CNTCVS_HI Register

1 GTC_CFG2_CNTCVS_HI Register (Offset = 4h) [reset = 0h]

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Table 14-25193. Instance Table

Instance Name	Physical Address
GTC0	00AA 0004h

Figure 14-8313. GTC_CFG2_CNTCVS_HI Name Register

31	30	29	28	27	26	25	24
CNTCVS_HI_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCVS_HI_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCVS_HI_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCVS_HI_COUNTVALUE							
R							
X							

Table 14-25195. GTC_CFG2_CNTCVS_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCVS_HI_COUNTVALUE	R	X	Indicates bits [63:32] of the System Counter value. Reset Source: mod_por_rst_n

14.9.5.1.2.12 GTC_CFG3_CNTTIDR Register

1 GTC_CFG3_CNTTIDR Register (Offset = 8h) [reset = 0h]

Return to Summary Table

Table 14-25196. Instance Table

Instance Name	Physical Address
GTC0	**00AB 0008h**

Figure 14-8314. GTC_CFG3_CNTTIDR Name Register

31	30	29	28	27	26	25	24
CNTTIDR_FRAME7				CNTTIDR_FRAME6			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
CNTTIDR_FRAME5				CNTTIDR_FRAME4			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
CNTTIDR_FRAME3				CNTTIDR_FRAME2			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
CNTTIDR_FRAME1				CNTTIDR_FRAME0			
R				R			
0h				0h			

Table 14-25198. GTC_CFG3_CNTTIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CNTTIDR_FRAME7	R	0h	Indicates the features of timer frame7. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
27:24	CNTTIDR_FRAME6	R	0h	Indicates the features of timer frame6. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
23:20	CNTTIDR_FRAME5	R	0h	Indicates the features of timer frame5. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
19:16	CNTTIDR_FRAME4	R	0h	Indicates the features of timer frame4. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
15:12	CNTTIDR_FRAME3	R	0h	Indicates the features of timer frame3. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
11:8	CNTTIDR_FRAME2	R	0h	Indicates the features of timer frame2. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
7:4	CNTTIDR_FRAME1	R	0h	Indicates the features of timer frame1. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n

Table 14-25198. GTC_CFG3_CNTTIDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CNTTIDR_FRAME0	R	0h	Indicates the features of timer frame0. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n

14.9.5.2 RTI_CFG1

RTI_CFG1

14.9.5.2.1 RTI_CFG1 Summaries

RTI_CFG1 Summaries

Table 14-25199. RTI Registers, Base Address=0E00 0000h, Length=256

Offset	Length	Register Name	RTI0 Physical Address	RTI1 Physical Address	RTI8 Physical Address
0h	32	RTI_RTIGCTRL	0488 0000h	0E00 0000h	0E01 0000h
4h	32	RTI_RTITBCTRL	0488 0004h	0E00 0004h	0E01 0004h
8h	32	RTI_RTICAPCTRL	0488 0008h	0E00 0008h	0E01 0008h
Ch	32	RTI_RTICOMPCTRL	0488 000Ch	0E00 000Ch	0E01 000Ch
10h	32	RTI_RTIFRC0	0488 0010h	0E00 0010h	0E01 0010h
14h	32	RTI_RTIUC0	0488 0014h	0E00 0014h	0E01 0014h
18h	32	RTI_RTICPUC0	0488 0018h	0E00 0018h	0E01 0018h
20h	32	RTI_RTICAFRC0	0488 0020h	0E00 0020h	0E01 0020h
24h	32	RTI_RTICAUC0	0488 0024h	0E00 0024h	0E01 0024h
30h	32	RTI_RTIFRC1	0488 0030h	0E00 0030h	0E01 0030h
34h	32	RTI_RTIUC1	0488 0034h	0E00 0034h	0E01 0034h
38h	32	RTI_RTICPUC1	0488 0038h	0E00 0038h	0E01 0038h
40h	32	RTI_RTICAFRC1	0488 0040h	0E00 0040h	0E01 0040h
44h	32	RTI_RTICAUC1	0488 0044h	0E00 0044h	0E01 0044h
50h	32	RTI_RTICOMP0	0488 0050h	0E00 0050h	0E01 0050h
54h	32	RTI_RTIUDCP0	0488 0054h	0E00 0054h	0E01 0054h
58h	32	RTI_RTICOMP1	0488 0058h	0E00 0058h	0E01 0058h
5Ch	32	RTI_RTIUDCP1	0488 005Ch	0E00 005Ch	0E01 005Ch
60h	32	RTI_RTICOMP2	0488 0060h	0E00 0060h	0E01 0060h
64h	32	RTI_RTIUDCP2	0488 0064h	0E00 0064h	0E01 0064h
68h	32	RTI_RTICOMP3	0488 0068h	0E00 0068h	0E01 0068h
6Ch	32	RTI_RTIUDCP3	0488 006Ch	0E00 006Ch	0E01 006Ch
70h	32	RTI_RTITBLCOMP	0488 0070h	0E00 0070h	0E01 0070h
74h	32	RTI_RTITBHCOMP	0488 0074h	0E00 0074h	0E01 0074h
80h	32	RTI_RTISETINT	0488 0080h	0E00 0080h	0E01 0080h
84h	32	RTI_RTICLEARINT	0488 0084h	0E00 0084h	0E01 0084h
88h	32	RTI_RTIINTFLAG	0488 0088h	0E00 0088h	0E01 0088h
90h	32	RTI_RTIDWDCTRL	0488 0090h	0E00 0090h	0E01 0090h
94h	32	RTI_RTIDWDPRLD	0488 0094h	0E00 0094h	0E01 0094h
98h	32	RTI_RTIWDSTATUS	0488 0098h	0E00 0098h	0E01 0098h
9Ch	32	RTI_RTIWDKEY	0488 009Ch	0E00 009Ch	0E01 009Ch
A0h	32	RTI_RTIDWDCNTR	0488 00A0h	0E00 00A0h	0E01 00A0h
A4h	32	RTI_RTIDWWDRXNCTRL	0488 00A4h	0E00 00A4h	0E01 00A4h
A8h	32	RTI_RTIDWWDSIZECTRL	0488 00A8h	0E00 00A8h	0E01 00A8h
ACh	32	RTI_RTIINTCLRENABLE	0488 00ACh	0E00 00ACh	0E01 00ACh
B0h	32	RTI_RTICOMP0CLR	0488 00B0h	0E00 00B0h	0E01 00B0h
B4h	32	RTI_RTICOMP1CLR	0488 00B4h	0E00 00B4h	0E01 00B4h
B8h	32	RTI_RTICOMP2CLR	0488 00B8h	0E00 00B8h	0E01 00B8h

Table 14-25199. RTI Registers, Base Address=0E00 0000h, Length=256 (continued)

Offset	Length	Register Name	RTI0 Physical Address	RTI1 Physical Address	RTI8 Physical Address
BCh	32	RTI_RTICOMP3CLR	0488 00BCh	0E00 00BCh	0E01 00BCh

Table 14-25200. RTI Registers, Base Address=0E00 0000h, Length=256

Offset	Length	Register Name	RTI9 Physical Address	RTI10 Physical Address	RTI11 Physical Address
0h	32	RTI_RTIGCTRL	0E08 0000h	0E09 0000h	0E0A 0000h
4h	32	RTI_RTITBCTRL	0E08 0004h	0E09 0004h	0E0A 0004h
8h	32	RTI_RTICAPCTRL	0E08 0008h	0E09 0008h	0E0A 0008h
Ch	32	RTI_RTICOMPCTRL	0E08 000Ch	0E09 000Ch	0E0A 000Ch
10h	32	RTI_RTIFRC0	0E08 0010h	0E09 0010h	0E0A 0010h
14h	32	RTI_RTIUC0	0E08 0014h	0E09 0014h	0E0A 0014h
18h	32	RTI_RTICPUC0	0E08 0018h	0E09 0018h	0E0A 0018h
20h	32	RTI_RTICAFRC0	0E08 0020h	0E09 0020h	0E0A 0020h
24h	32	RTI_RTICAUC0	0E08 0024h	0E09 0024h	0E0A 0024h
30h	32	RTI_RTIFRC1	0E08 0030h	0E09 0030h	0E0A 0030h
34h	32	RTI_RTIUC1	0E08 0034h	0E09 0034h	0E0A 0034h
38h	32	RTI_RTICPUC1	0E08 0038h	0E09 0038h	0E0A 0038h
40h	32	RTI_RTICAFRC1	0E08 0040h	0E09 0040h	0E0A 0040h
44h	32	RTI_RTICAUC1	0E08 0044h	0E09 0044h	0E0A 0044h
50h	32	RTI_RTICOMP0	0E08 0050h	0E09 0050h	0E0A 0050h
54h	32	RTI_RTIUDCP0	0E08 0054h	0E09 0054h	0E0A 0054h
58h	32	RTI_RTICOMP1	0E08 0058h	0E09 0058h	0E0A 0058h
5Ch	32	RTI_RTIUDCP1	0E08 005Ch	0E09 005Ch	0E0A 005Ch
60h	32	RTI_RTICOMP2	0E08 0060h	0E09 0060h	0E0A 0060h
64h	32	RTI_RTIUDCP2	0E08 0064h	0E09 0064h	0E0A 0064h
68h	32	RTI_RTICOMP3	0E08 0068h	0E09 0068h	0E0A 0068h
6Ch	32	RTI_RTIUDCP3	0E08 006Ch	0E09 006Ch	0E0A 006Ch
70h	32	RTI_RTITBLCOMP	0E08 0070h	0E09 0070h	0E0A 0070h
74h	32	RTI_RTITBHCOMP	0E08 0074h	0E09 0074h	0E0A 0074h
80h	32	RTI_RTISETINT	0E08 0080h	0E09 0080h	0E0A 0080h
84h	32	RTI_RTICLEARINT	0E08 0084h	0E09 0084h	0E0A 0084h
88h	32	RTI_RTIINTFLAG	0E08 0088h	0E09 0088h	0E0A 0088h
90h	32	RTI_RTIDWDCTRL	0E08 0090h	0E09 0090h	0E0A 0090h
94h	32	RTI_RTIDWDPRLD	0E08 0094h	0E09 0094h	0E0A 0094h
98h	32	RTI_RTIWDSTATUS	0E08 0098h	0E09 0098h	0E0A 0098h
9Ch	32	RTI_RTIWDKEY	0E08 009Ch	0E09 009Ch	0E0A 009Ch
A0h	32	RTI_RTIDWDCNTR	0E08 00A0h	0E09 00A0h	0E0A 00A0h
A4h	32	RTI_RTIDWWDRXNCTRL	0E08 00A4h	0E09 00A4h	0E0A 00A4h
A8h	32	RTI_RTIDWWDSIZECTRL	0E08 00A8h	0E09 00A8h	0E0A 00A8h
ACh	32	RTI_RTIINTCLRENABLE	0E08 00ACh	0E09 00ACh	0E0A 00ACh
B0h	32	RTI_RTICOMP0CLR	0E08 00B0h	0E09 00B0h	0E0A 00B0h
B4h	32	RTI_RTICOMP1CLR	0E08 00B4h	0E09 00B4h	0E0A 00B4h
B8h	32	RTI_RTICOMP2CLR	0E08 00B8h	0E09 00B8h	0E0A 00B8h
BCh	32	RTI_RTICOMP3CLR	0E08 00BCh	0E09 00BCh	0E0A 00BCh

Table 14-25201. RTI Registers, Base Address=0E00 0000h, Length=256

Offset	Length	Register Name	MCU_RTI0 Physical Address
0h	32	RTI_RTIGCTRL	0E0B 0000h
4h	32	RTI_RTITBCTRL	0E0B 0004h
8h	32	RTI_RTICAPCTRL	0E0B 0008h
Ch	32	RTI_RTICOMPCTRL	0E0B 000Ch
10h	32	RTI_RTIFRC0	0E0B 0010h
14h	32	RTI_RTIUC0	0E0B 0014h
18h	32	RTI_RTICPUC0	0E0B 0018h
20h	32	RTI_RTICAFRC0	0E0B 0020h
24h	32	RTI_RTICAUC0	0E0B 0024h
30h	32	RTI_RTIFRC1	0E0B 0030h
34h	32	RTI_RTIUC1	0E0B 0034h
38h	32	RTI_RTICPUC1	0E0B 0038h
40h	32	RTI_RTICAFRC1	0E0B 0040h
44h	32	RTI_RTICAUC1	0E0B 0044h
50h	32	RTI_RTICOMP0	0E0B 0050h
54h	32	RTI_RTIUDCP0	0E0B 0054h
58h	32	RTI_RTICOMP1	0E0B 0058h
5Ch	32	RTI_RTIUDCP1	0E0B 005Ch
60h	32	RTI_RTICOMP2	0E0B 0060h
64h	32	RTI_RTIUDCP2	0E0B 0064h
68h	32	RTI_RTICOMP3	0E0B 0068h
6Ch	32	RTI_RTIUDCP3	0E0B 006Ch
70h	32	RTI_RTITBLCOMP	0E0B 0070h
74h	32	RTI_RTITBHCOMP	0E0B 0074h
80h	32	RTI_RTISETINT	0E0B 0080h
84h	32	RTI_RTICLEARINT	0E0B 0084h
88h	32	RTI_RTIINTFLAG	0E0B 0088h
90h	32	RTI_RTIDWDCTRL	0E0B 0090h
94h	32	RTI_RTIDWDPRLD	0E0B 0094h
98h	32	RTI_RTIWDSTATUS	0E0B 0098h
9Ch	32	RTI_RTIWDKEY	0E0B 009Ch
A0h	32	RTI_RTIDWDCNTR	0E0B 00A0h
A4h	32	RTI_RTIDWWDRXNCTRL	0E0B 00A4h
A8h	32	RTI_RTIDWWDSIZECTRL	0E0B 00A8h
ACh	32	RTI_RTIINTCLRENABLE	0E0B 00ACh
B0h	32	RTI_RTICOMP0CLR	0E0B 00B0h
B4h	32	RTI_RTICOMP1CLR	0E0B 00B4h
B8h	32	RTI_RTICOMP2CLR	0E0B 00B8h
BCh	32	RTI_RTICOMP3CLR	0E0B 00BCh

14.9.5.2.2 RTI_CFG1 Registers

RTI_CFG1 Registers

14.9.5.2.2.1 RTI_RTIGCTRL Register

1 RTI_RTIGCTRL Register (Offset = 0h) [reset = 0h]

RTI Global Control Register

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Table 14-25202. Instance Table

Instance Name	**Physical Address**
MCU_RTI0	**0488 0000h**
RTI0	**0E00 0000h**
RTI1	**0E01 0000h**
RTI8	**0E08 0000h**
RTI9	**0E09 0000h**
RTI10	**0E0A 0000h**
RTI11	**0E0B 0000h**

Figure 14-8315. RTI_RTIGCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NTUSEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>COS</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CNT1EN</td><td>CNT0EN</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25204. RTI_RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

Table 14-25204. RTI_RTIGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	NTUSEL	R/W	0h	These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL. User and privilege mode (read): 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to '0' Privilege mode (write): 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to '0' Reset Source: mod_g_rst_n
15	COS	R/W	0h	This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting. User and privilege mode (read): 0 = counters are stopped while in debug mode 1 = counters are running while in debug mode Privilege mode (write): 0 = stop counters in debug mode 1 = continue counting in debug mode Reset Source: mod_g_rst_n
14:2	RESERVED	NONE	0h	Reserved
1	CNT1EN	R/W	0h	The CNT1EN bit starts and stops the operation of counter block 1 (UC1 and FRC1). User and privilege mode (read): 0 = counters are stopped 1 = counters are running Privilege mode (write): 0 = stop counters 1 = start counters Reset Source: mod_g_rst_n
0	CNT0EN	R/W	0h	The CNT0EN bit starts and stops the operation of counter block 0 (UC0 and FRC0). User and privilege mode (read): 0 = counters are stopped 1 = counters are running Privilege mode (write): 0 = stop counters 1 = start counters Reset Source: mod_g_rst_n

14.9.5.2.2.2 RTI_RTITBCTRL Register

1 RTI_RTITBCTRL Register (Offset = 4h) [reset = 0h]

RTI Timebase Control Register

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Table 14-25205. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0004h**
RTI0	**0E00 0004h**
RTI1	**0E01 0004h**
RTI8	**0E08 0004h**
RTI9	**0E09 0004h**
RTI10	**0E0A 0004h**
RTI11	**0E0B 0004h**

Figure 14-8316. RTI_RTITBCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INC	TBEXT
NONE						R/W	R/W
0h						0h	0h

Table 14-25207. RTI_RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	INC	R/W	0h	This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected. User and privilege mode (read): 0 = FRC0 will not be incremented 1 = FRC0 will be incremented Privilege mode (write): 0 = Do not increment FRC0 on failing external clock 1 = Increment FRC0 on failing external clock Reset Source: mod_g_rst_n

Table 14-25207. RTI_RTITBCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TBEXT	R/W	0h	The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx. When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset. The selection if the external signal should be used, can only be done by software. User and privilege mode (read): 0 = UC0 clocks FRC0 1 = NTUx clocks FRC0 Privilege mode (write): 0 = MUX is switched to internal UC0 clocking scheme 1 = MUX is switched to external NTUx clocking scheme Reset Source: mod_g_rst_n

14.9.5.2.2.3 RTI_RTICAPCTRL Register

1 RTI_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

RTI Capture Control Register

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Table 14-25208. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0008h**
RTI0	**0E00 0008h**
RTI1	**0E01 0008h**
RTI8	**0E08 0008h**
RTI9	**0E09 0008h**
RTI10	**0E0A 0008h**
RTI11	**0E0B 0008h**

Figure 14-8317. RTI_RTICAPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CAPCNTR1	CAPCNTR0
NONE						R/W	R/W
0h						0h	0h

Table 14-25210. RTI_RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CAPCNTR1	R/W	0h	This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1. User and privilege mode (read): 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode (write): 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 Reset Source: mod_g_rst_n

Table 14-25210. RTI_RTICAPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CAPCNTR0	R/W	0h	This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0. User and privilege mode (read): 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode (write): 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 Reset Source: mod_g_rst_n

14.9.5.2.2.4 RTI_RTICOMPCTRL Register

1 RTI_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

RTI Compare Control Register

Return to Summary Table

Table 14-25211. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 000Ch**
RTI0	**0E00 000Ch**
RTI1	**0E01 000Ch**
RTI8	**0E08 000Ch**
RTI9	**0E09 000Ch**
RTI10	**0E0A 000Ch**
RTI11	**0E0B 000Ch**

Figure 14-8318. RTI_RTICOMPCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>COMPSEL3</td><td colspan="3">RESERVED</td><td>COMPSEL2</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>COMPSEL1</td><td colspan="3">RESERVED</td><td>COMPSEL0</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-25213. RTI_RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	COMPSEL3	R/W	0h	This bit determines the counter with which the compare value hold in compare register 3 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE	0h	Reserved

Table 14-25213. RTI_RTICOMPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	COMPSEL2	R/W	0h	This bit determines the counter with which the compare value hold in compare register 2 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	COMPSEL1	R/W	0h	This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	COMPSEL0	R/W	0h	This bit determines the counter with which the compare value hold in compare register 0 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n

14.9.5.2.2.5 RTI_RTIFRC0 Register

1 RTI_RTIFRC0 Register (Offset = 10h) [reset = 0h]

RTI Free Running Counter 0 Register

Return to Summary Table

Table 14-25214. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0010h**
RTI0	**0E00 0010h**
RTI1	**0E01 0010h**
RTI8	**0E08 0010h**
RTI9	**0E09 0010h**
RTI10	**0E0A 0010h**
RTI11	**0E0B 0010h**

Figure 14-8319. RTI_RTIFRC0 Name Register

31	30	29	28	27	26	25	24
FRC0							
R/W							
0h							
23	22	21	20	19	18	17	16
FRC0							
R/W							
0h							
15	14	13	12	11	10	9	8
FRC0							
R/W							
0h							
7	6	5	4	3	2	1	0
FRC0							
R/W							
0h							

Table 14-25216. RTI_RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC0	R/W	0h	This registers holds the current value of the Free Running Counter 0 and will be updated continuously. User and privilege mode (read): current value of the counter Privilege mode (write): The counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Reset Source: mod_g_rst_n

14.9.5.2.2.6 RTI_RTIUC0 Register

1 RTI_RTIUC0 Register (Offset = 14h) [reset = 0h]

RTI Up Counter 0 Register

Return to Summary Table

Table 14-25217. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0014h**
RTI0	**0E00 0014h**
RTI1	**0E01 0014h**
RTI8	**0E08 0014h**
RTI9	**0E09 0014h**
RTI10	**0E0A 0014h**
RTI11	**0E0B 0014h**

Figure 14-8320. RTI_RTIUC0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">UC0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">UC0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UC0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UC0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25219. RTI_RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC0	R/W	0h	This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0. User and privilege mode (read): value of the counter when the Free Running Counter 0 was read Privilege mode (write): the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows. Reset Source: mod_g_rst_n

14.9.5.2.2.7 RTI_RTICPUC0 Register

1 RTI_RTICPUC0 Register (Offset = 18h) [reset = 0h]

RTI Compare Up Counter 0 Register

Return to Summary Table

Table 14-25220. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0018h**
RTI0	**0E00 0018h**
RTI1	**0E01 0018h**
RTI8	**0E08 0018h**
RTI9	**0E09 0018h**
RTI10	**0E0A 0018h**
RTI11	**0E0B 0018h**

Figure 14-8321. RTI_RTICPUC0 Name Register

31	30	29	28	27	26	25	24
CPUC0							
R/W							
0h							
23	22	21	20	19	18	17	16
CPUC0							
R/W							
0h							
15	14	13	12	11	10	9	8
CPUC0							
R/W							
0h							
7	6	5	4	3	2	1	0
CPUC0							
R/W							
0h							

Table 14-25222. RTI_RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC0	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock. If CPUC0 = 0: fFRC0 = R-----T---I---C----L----K-- 232 If CPUC0 0: fFRC0 = ----R----T----I--C-----L---K------- CPUC0 + 1 User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Reset Source: mod_g_rst_n

14.9.5.2.2.8 RTI_RTICAFRC0 Register

1 RTI_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

RTI Capture Free Running Counter 0 Register

Return to Summary Table

Table 14-25223. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0020h**
RTI0	**0E00 0020h**
RTI1	**0E01 0020h**
RTI8	**0E08 0020h**
RTI9	**0E09 0020h**
RTI10	**0E0A 0020h**
RTI11	**0E0B 0020h**

Figure 14-8322. RTI_RTICAFRC0 Name Register

31	30	29	28	27	26	25	24
CAFRC0							
R							
0h							
23	22	21	20	19	18	17	16
CAFRC0							
R							
0h							
15	14	13	12	11	10	9	8
CAFRC0							
R							
0h							
7	6	5	4	3	2	1	0
CAFRC0							
R							
0h							

Table 14-25225. RTI_RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC0	R	0h	This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block. User and privilege mode (read): value of Free Running Counter 0 on a capture event Reset Source: mod_g_rst_n

14.9.5.2.2.9 RTI_RTICAUC0 Register

1 RTI_RTICAUC0 Register (Offset = 24h) [reset = 0h]

RTI Capture Up Counter 0 Register

Return to Summary Table

Table 14-25226. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0024h**
RTI0	**0E00 0024h**
RTI1	**0E01 0024h**
RTI8	**0E08 0024h**
RTI9	**0E09 0024h**
RTI10	**0E0A 0024h**
RTI11	**0E0B 0024h**

Figure 14-8323. RTI_RTICAUC0 Name Register

31	30	29	28	27	26	25	24
CAUC0							
R							
0h							
23	22	21	20	19	18	17	16
CAUC0							
R							
0h							
15	14	13	12	11	10	9	8
CAUC0							
R							
0h							
7	6	5	4	3	2	1	0
CAUC0							
R							
0h							

Table 14-25228. RTI_RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC0	R	0h	This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode (read): value of Up Counter 0 on a capture event Reset Source: mod_g_rst_n

14.9.5.2.2.10 RTI_RTIFRC1 Register

1 RTI_RTIFRC1 Register (Offset = 30h) [reset = 0h]

RTI Free Running Counter 1 Register

Return to Summary Table

Table 14-25229. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0030h**
RTI0	**0E00 0030h**
RTI1	**0E01 0030h**
RTI8	**0E08 0030h**
RTI9	**0E09 0030h**
RTI10	**0E0A 0030h**
RTI11	**0E0B 0030h**

Figure 14-8324. RTI_RTIFRC1 Name Register

31	30	29	28	27	26	25	24
FRC1							
R/W							
0h							
23	22	21	20	19	18	17	16
FRC1							
R/W							
0h							
15	14	13	12	11	10	9	8
FRC1							
R/W							
0h							
7	6	5	4	3	2	1	0
FRC1							
R/W							
0h							

Table 14-25231. RTI_RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC1	R/W	0h	This registers holds the current value of the Free Running Counter 1 and will be updated continuously. User and privilege mode (read): current value of the counter Privilege mode (write): the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1. Reset Source: mod_g_rst_n

14.9.5.2.2.11 RTI_RTIUC1 Register

1 RTI_RTIUC1 Register (Offset = 34h) [reset = 0h]

RTI Up Counter 1 Register

Return to Summary Table

Table 14-25232. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0034h**
RTI0	**0E00 0034h**
RTI1	**0E01 0034h**
RTI8	**0E08 0034h**
RTI9	**0E09 0034h**
RTI10	**0E0A 0034h**
RTI11	**0E0B 0034h**

Figure 14-8325. RTI_RTIUC1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">UC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">UC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25234. RTI_RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC1	R/W	0h	This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1. User and privilege mode (read): value of the counter when the Free Running Counter 1 was read Privilege mode (write): the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be disabled in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since UC1 has to count up until it overflows. Reset Source: mod_g_rst_n

14.9.5.2.2.12 RTI_RTICPUC1 Register

1 RTI_RTICPUC1 Register (Offset = 38h) [reset = 0h]

RTI Compare Up Counter 1 Register

Return to Summary Table

Table 14-25235. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0038h**
RTI0	**0E00 0038h**
RTI1	**0E01 0038h**
RTI8	**0E08 0038h**
RTI9	**0E09 0038h**
RTI10	**0E0A 0038h**
RTI11	**0E0B 0038h**

Figure 14-8326. RTI_RTICPUC1 Name Register

31	30	29	28	27	26	25	24
CPUC1							
R/W							
0h							
23	22	21	20	19	18	17	16
CPUC1							
R/W							
0h							
15	14	13	12	11	10	9	8
CPUC1							
R/W							
0h							
7	6	5	4	3	2	1	0
CPUC1							
R/W							
0h							

Table 14-25237. RTI_RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC1	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock. If CPUC1 = 0: fFRC1 = R-----T---I---C----L----K-- 232 If CPUC1 0: fFRC1 = ----R----T----I--C-----L---K------- CPUC1 + 1 User and privilege mode (read): current compare value Privilege mode (write): the compare value is updated Reset Source: mod_g_rst_n

14.9.5.2.2.13 RTI_RTICAFRC1 Register

1 RTI_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

RTI Capture Free Running Counter 1 Register

Return to Summary Table

Table 14-25238. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0040h**
RTI0	**0E00 0040h**
RTI1	**0E01 0040h**
RTI8	**0E08 0040h**
RTI9	**0E09 0040h**
RTI10	**0E0A 0040h**
RTI11	**0E0B 0040h**

Figure 14-8327. RTI_RTICAFRC1 Name Register

31	30	29	28	27	26	25	24
CAFRC1							
R							
0h							
23	22	21	20	19	18	17	16
CAFRC1							
R							
0h							
15	14	13	12	11	10	9	8
CAFRC1							
R							
0h							
7	6	5	4	3	2	1	0
CAFRC1							
R							
0h							

Table 14-25240. RTI_RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC1	R	0h	This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block. User and privilege mode (read): value of Free Running Counter 1 on a capture event Reset Source: mod_g_rst_n

14.9.5.2.2.14 RTI_RTICAUC1 Register

1 RTI_RTICAUC1 Register (Offset = 44h) [reset = 0h]

RTI Capture Up Counter 1 Register

Return to Summary Table

Table 14-25241. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0044h**
RTI0	**0E00 0044h**
RTI1	**0E01 0044h**
RTI8	**0E08 0044h**
RTI9	**0E09 0044h**
RTI10	**0E0A 0044h**
RTI11	**0E0B 0044h**

Figure 14-8328. RTI_RTICAUC1 Name Register

31	30	29	28	27	26	25	24
CAUC1							
R							
0h							
23	22	21	20	19	18	17	16
CAUC1							
R							
0h							
15	14	13	12	11	10	9	8
CAUC1							
R							
0h							
7	6	5	4	3	2	1	0
CAUC1							
R							
0h							

Table 14-25243. RTI_RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC1	R	0h	This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode (read): value of Up Counter 1 on a capture event Reset Source: mod_g_rst_n

14.9.5.2.2.15 RTI_RTICOMP0 Register

1 RTI_RTICOMP0 Register (Offset = 50h) [reset = 0h]

RTI Compare 0 Register

Return to Summary Table

Table 14-25244. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0050h**
RTI0	**0E00 0050h**
RTI1	**0E01 0050h**
RTI8	**0E08 0050h**
RTI9	**0E09 0050h**
RTI10	**0E0A 0050h**
RTI11	**0E0B 0050h**

Figure 14-8329. RTI_RTICOMP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COMP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COMP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COMP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25246. RTI_RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.5.2.2.16 RTI_RTIUDCP0 Register

1 RTI_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

RTI Update Compare 0 Register

Return to Summary Table

Table 14-25247. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0054h**
RTI0	**0E00 0054h**
RTI1	**0E01 0054h**
RTI8	**0E08 0054h**
RTI9	**0E09 0054h**
RTI10	**0E0A 0054h**
RTI11	**0E0B 0054h**

Figure 14-8330. RTI_RTIUDCP0 Name Register

31	30	29	28	27	26	25	24
UDCP0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UDCP0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UDCP0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UDCP0							
R/W							
0h							

Table 14-25249. RTI_RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP0	R/W	0h	This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 0 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.9.5.2.2.17 RTI_RTICOMP1 Register

1 RTI_RTICOMP1 Register (Offset = 58h) [reset = 0h]

RTI Compare 1 Register

Return to Summary Table

Table 14-25250. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0058h**
RTI0	**0E00 0058h**
RTI1	**0E01 0058h**
RTI8	**0E08 0058h**
RTI9	**0E09 0058h**
RTI10	**0E0A 0058h**
RTI11	**0E0B 0058h**

Figure 14-8331. RTI_RTICOMP1 Name Register

31	30	29	28	27	26	25	24
COMP1							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP1							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP1							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP1							
R/W							
0h							

Table 14-25252. RTI_RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.5.2.2.18 RTI_RTIUDCP1 Register

1 RTI_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

RTI Update Compare 1 Register

Return to Summary Table

Table 14-25253. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 005Ch**
RTI0	**0E00 005Ch**
RTI1	**0E01 005Ch**
RTI8	**0E08 005Ch**
RTI9	**0E09 005Ch**
RTI10	**0E0A 005Ch**
RTI11	**0E0B 005Ch**

Figure 14-8332. RTI_RTIUDCP1 Name Register

31	30	29	28	27	26	25	24
UDCP1							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP1							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP1							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP1							
R/W							
0h							

Table 14-25255. RTI_RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP1	R/W	0h	This registers holds a value, which is added to the value in the compare 1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 1 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.9.5.2.2.19 RTI_RTICOMP2 Register

1 RTI_RTICOMP2 Register (Offset = 60h) [reset = 0h]

RTI Compare 2 Register

Return to Summary Table

Table 14-25256. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0060h**
RTI0	**0E00 0060h**
RTI1	**0E01 0060h**
RTI8	**0E08 0060h**
RTI9	**0E09 0060h**
RTI10	**0E0A 0060h**
RTI11	**0E0B 0060h**

Figure 14-8333. RTI_RTICOMP2 Name Register

31	30	29	28	27	26	25	24
COMP2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COMP2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COMP2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMP2							
R/W							
0h							

Table 14-25258. RTI_RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.5.2.2.20 RTI_RTIUDCP2 Register

1 RTI_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

RTI Update Compare 2 Register

Return to Summary Table

Table 14-25259. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0064h**
RTI0	**0E00 0064h**
RTI1	**0E01 0064h**
RTI8	**0E08 0064h**
RTI9	**0E09 0064h**
RTI10	**0E0A 0064h**
RTI11	**0E0B 0064h**

Figure 14-8334. RTI_RTIUDCP2 Name Register

31	30	29	28	27	26	25	24
UDCP2							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP2							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP2							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP2							
R/W							
0h							

Table 14-25261. RTI_RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP2	R/W	0h	This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 2 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.9.5.2.2.21 RTI_RTICOMP3 Register

1 RTI_RTICOMP3 Register (Offset = 68h) [reset = 0h]

RTI Compare 3 Register

Return to Summary Table

Table 14-25262. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0068h**
RTI0	**0E00 0068h**
RTI1	**0E01 0068h**
RTI8	**0E08 0068h**
RTI9	**0E09 0068h**
RTI10	**0E0A 0068h**
RTI11	**0E0B 0068h**

Figure 14-8335. RTI_RTICOMP3 Name Register

31	30	29	28	27	26	25	24
COMP3							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP3							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP3							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP3							
R/W							
0h							

Table 14-25264. RTI_RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.5.2.2.22 RTI_RTIUDCP3 Register

1 RTI_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

RTI Update Compare 3 Register

Return to Summary Table

Table 14-25265. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 006Ch**
RTI0	**0E00 006Ch**
RTI1	**0E01 006Ch**
RTI8	**0E08 006Ch**
RTI9	**0E09 006Ch**
RTI10	**0E0A 006Ch**
RTI11	**0E0B 006Ch**

Figure 14-8336. RTI_RTIUDCP3 Name Register

31	30	29	28	27	26	25	24
UDCP3							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP3							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP3							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP3							
R/W							
0h							

Table 14-25267. RTI_RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP3	R/W	0h	This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 3 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.9.5.2.2.23 RTI_RTITBLCOMP Register

1 RTI_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

RTI External Clock Timebase Low Compare Register

Return to Summary Table

Table 14-25268. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0070h**
RTI0	**0E00 0070h**
RTI1	**0E01 0070h**
RTI8	**0E08 0070h**
RTI9	**0E09 0070h**
RTI10	**0E0A 0070h**
RTI11	**0E0B 0070h**

Figure 14-8337. RTI_RTITBLCOMP Name Register

31	30	29	28	27	26	25	24
TBLCOMP							
R/W							
0h							
23	22	21	20	19	18	17	16
TBLCOMP							
R/W							
0h							
15	14	13	12	11	10	9	8
TBLCOMP							
R/W							
0h							
7	6	5	4	3	2	1	0
TBLCOMP							
R/W							
0h							

Table 14-25270. RTI_RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBLCOMP	R/W	0h	This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0. User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Note: Reset behavior A reset does not generate a compare match. Reset Source: mod_g_rst_n

14.9.5.2.2.24 RTI_RTITBHCOMP Register

1 RTI_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

RTI External Clock Timebase High Compare Register

Return to Summary Table

Table 14-25271. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0074h**
RTI0	**0E00 0074h**
RTI1	**0E01 0074h**
RTI8	**0E08 0074h**
RTI9	**0E09 0074h**
RTI10	**0E0A 0074h**
RTI11	**0E0B 0074h**

Figure 14-8338. RTI_RTITBHCOMP Name Register

31	30	29	28	27	26	25	24
TBHCOMP							
R/W							
0h							
23	22	21	20	19	18	17	16
TBHCOMP							
R/W							
0h							
15	14	13	12	11	10	9	8
TBHCOMP							
R/W							
0h							
7	6	5	4	3	2	1	0
TBHCOMP							
R/W							
0h							

Table 14-25273. RTI_RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBHCOMP	R/W	0h	This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0. RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached. Example: The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0. RTICPUC0 = 0x00000050 RTITBLCOMP = 0x000046 RTITBHCOMP = 0x00000009 User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Note: Reset behavior A reset does not generate a compare match. Reset Source: mod_g_rst_n

14.9.5.2.2.25 RTI_RTISETINT Register

1 RTI_RTISETINT Register (Offset = 80h) [reset = 0h]

RTI Set/Status Interrupt Register

Return to Summary Table

Table 14-25274. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0080h**
RTI0	**0E00 0080h**
RTI1	**0E01 0080h**
RTI8	**0E08 0080h**
RTI9	**0E09 0080h**
RTI10	**0E0A 0080h**
RTI11	**0E0B 0080h**

Figure 14-8339. RTI_RTISETINT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					SETOVL1INT	SETOVL0INT	SETTBINT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED				SETDMA3	SETDMA2	SETDMA1	SETDMA0
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED				SETINT3	SETINT2	SETINT1	SETINT0
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-25276. RTI_RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	SETOVL1INT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
17	SETOVL0INT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n

Table 14-25276. RTI_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SETTBINT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	SETDMA3	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
10	SETDMA2	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
9	SETDMA1	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
8	SETDMA0	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3	SETINT3	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
2	SETINT2	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n

Table 14-25276. RTI_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SETINT1	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
0	SETINT0	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n

14.9.5.2.2.26 RTI_RTICLEARINT Register

1 RTI_RTICLEARINT Register (Offset = 84h) [reset = 0h]

RTI Clear/Status Interrupt Register

Return to Summary Table

Table 14-25277. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0084h**
RTI0	**0E00 0084h**
RTI1	**0E01 0084h**
RTI8	**0E08 0084h**
RTI9	**0E09 0084h**
RTI10	**0E0A 0084h**
RTI11	**0E0B 0084h**

Figure 14-8340. RTI_RTICLEARINT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-25279. RTI_RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	CLEAROVL1INT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n

Table 14-25279. RTI_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CLEAROVL0INT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
16	CLEARTBINT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	CLEARDMA3	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
10	CLEARDMA2	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
9	CLEARDMA1	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
8	CLEARDMA0	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3	CLEARINT3	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n

Table 14-25279. RTI_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CLEARINT2	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
1	CLEARINT1	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
0	CLEARINT0	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n

14.9.5.2.2.27 RTI_RTIINTFLAG Register

1 RTI_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

RTI Interrupt Flag Register

Return to Summary Table

Table 14-25280. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0088h**
RTI0	**0E00 0088h**
RTI1	**0E01 0088h**
RTI8	**0E08 0088h**
RTI9	**0E09 0088h**
RTI10	**0E0A 0088h**
RTI11	**0E0B 0088h**

Figure 14-8341. RTI_RTIINTFLAG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td>OVL1INT</td><td>OVL0INT</td><td>TBINT</td></tr>
<tr><td colspan="5">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>INT3</td><td>INT2</td><td>INT1</td><td>INT0</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25282. RTI_RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	OVL1INT	R/W1TC	0h	User and privilege mode (read): determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n

Table 14-25282. RTI_RTIINTFLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	OVL0INT	R/W1TC	0h	User and privilege mode (read): determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
16	TBINT	R/W1TC	0h	User and privilege mode (read): this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software. determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
15:4	RESERVED	NONE	0h	Reserved
3	INT3	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
2	INT2	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
1	INT1	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
0	INT0	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n

14.9.5.2.2.28 RTI_RTIDWDCTRL Register

1 RTI_RTIDWDCTRL Register (Offset = 90h) [reset = 5312ACEDh]

Digital Watchdog Control Register

Return to Summary Table

Table 14-25283. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0090h**
RTI0	**0E00 0090h**
RTI1	**0E01 0090h**
RTI8	**0E08 0090h**
RTI9	**0E09 0090h**
RTI10	**0E0A 0090h**
RTI11	**0E0B 0090h**

Figure 14-8342. RTI_RTIDWDCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DWDCTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5312ACEDh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DWDCTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5312ACEDh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DWDCTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5312ACEDh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DWDCTRL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5312ACEDh</td></tr>
</table>

Table 14-25285. RTI_RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DWDCTRL	R/W	5312ACEDh	User and priviledge mode (read): 0x5312ACED = DWD counter is disabled. This is the default value. 0xA98559DA = DWD counter is enabled Any other value = DWD counter state is unchanged (enabled or disabled) Priviledge mode (write): 0xA98559DA = DWD counter is enabled Any other value = State of DWD counter is unchanged (stays enabled or disabled) Note: One-Write Functionality of DWDCTRL Register The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again. Reset Source: mod_g_rst_n

14.9.5.2.2.29 RTI_RTIDWDPRLD Register

1 RTI_RTIDWDPRLD Register (Offset = 94h) [reset = FFFh]

Digital Watchdog Preload Register

Return to Summary Table

Table 14-25286. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0094h**
RTI0	**0E00 0094h**
RTI1	**0E01 0094h**
RTI8	**0E08 0094h**
RTI9	**0E09 0094h**
RTI10	**0E0A 0094h**
RTI11	**0E0B 0094h**

Figure 14-8343. RTI_RTIDWDPRLD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				DWDPRLD			
NONE				R/W			
0h				FFFh			
7	6	5	4	3	2	1	0
DWDPRLD							
R/W							
FFFh							

Table 14-25288. RTI_RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved

Table 14-25288. RTI_RTIDWDPRLD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	DWDPRLD	R/W	FFFh	User and priviledge mode (read): A read from this register in any CPU mode returns the current preload value. Priviledge mode (write): If the DWD is always enabled after reset is released: The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF. The application can configure the DWD preload register any time before this down counter expires. When the application services the DWD, the preload register contents are copied left- justified into the DWD down counter and it starts counting down from that value. If the DWD is implemented such that the down counter is enabled by software: The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter. The expiration time of the DWD Down Counter can be determined with following equation: texp = (RTIDWDPRLD+1) x 213 / RTICLK1 where: RTIDWDPRLD = 0...4095 Reset Source: mod_g_rst_n

14.9.5.2.2.30 RTI_RTIWDSTATUS Register

1 RTI_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Watchdog Status Register

Return to Summary Table

Table 14-25289. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 0098h**
RTI0	**0E00 0098h**
RTI1	**0E01 0098h**
RTI8	**0E08 0098h**
RTI9	**0E09 0098h**
RTI10	**0E0A 0098h**
RTI11	**0E0B 0098h**

Figure 14-8344. RTI_RTIWDSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DWWD	END	START	KEYST	DWDST	AWDST
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h

Table 14-25291. RTI_RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-25291. RTI_RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DWWD	R/W1TC	0h	This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog. User and priviledge mode (read): 0 = no time-window violation has occurred. 1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS reg- ister except for the AWD ST flag. Clearing of the status flags will deassert the non- maskable interrupt generated due to violation of the DWWD. Reset Source: mod_g_rst_n
4	END	R/W1TC	0h	This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag. User and priviledge mode (read): 0 = no end-time window violation has occurred. 1 = the end-time defined by the windowed watchdog configuration has been violated. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. Reset Source: mod_g_rst_n
3	START	R/W1TC	0h	This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened. User and priviledge mode (read): 0 = no start-time window violation has occurred. 1 = the start-time defined by the windowed watchdog configuration has been violated. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. Reset Source: mod_g_rst_n
2	KEYST	R/W1TC	0h	This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register. User and priviledge mode (read): 0 = no wrong key or key-sequence written 1 = wrong key or key-sequence written to RTIWDKEY register Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n
1	DWDST	R/W1TC	0h	status flag and is maintained for compatibility reasons. User and priviledge mode (read): 0 = DWD timeout period not expired 1 = DWD timeout period has expired Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n

Table 14-25291. RTI_RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AWDST	R/W1TC	0h	User and priviledge mode (read): 0 = AWD pin 0 > 1 threshold not exceeded 1 = AWD pin 0 > 1 threshold exceeded Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n

14.9.5.2.2.31 RTI_RTIWDKEY Register

1 RTI_RTIWDKEY Register (Offset = 9Ch) [reset = A35Ch]

Watchdog Key Register

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Table 14-25292. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 009Ch**
RTI0	**0E00 009Ch**
RTI1	**0E01 009Ch**
RTI8	**0E08 009Ch**
RTI9	**0E09 009Ch**
RTI10	**0E0A 009Ch**
RTI11	**0E0B 009Ch**

Figure 14-8345. RTI_RTIWDKEY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
WDKEY							
R/W							
A35Ch							
7	6	5	4	3	2	1	0
WDKEY							
R/W							
A35Ch							

Table 14-25294. RTI_RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved

Table 14-25294. RTI_RTIWDKEY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	WDKEY	R/W	A35Ch	User and privilege mode reads are indeterminate. Privilege mode (write): A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1's. Writing any other value causes a digital watchdog reset, as shown in Table 1-3. Note: Register write access time precaution The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation. Table 2. Example of a WDKEY sequence Value written to Step WDKEY Result 1 0x0A35C No Action 2 0x0A35C No Action 3 0x0E51A WDKEY is enabled for reset by next 0x0A35C 4 0x0E51A WDKEY is enabled for reset by next 0x0A35C 5 0x0E51A WDKEY is enabled for reset by next 0x0A35C 6 0x0A35C Watchdog is reset 7 0x0A35C No Action 8 0x0E51A WDKEY is enabled for reset by next 0x0A35C 9 0x0A35C Watchdog is reset 10 0x0E51A WDKEY is enabled for reset by next 0x0A35C 11 0x02345 System reset; incorrect value written to WDKEY Reset Source: mod_g_rst_n

14.9.5.2.2.32 RTI_RTIDWDCNTR Register

1 RTI_RTIDWDCNTR Register (Offset = A0h) [reset = 1FFFFFFh]

Digital Watchdog Down Counter

Return to Summary Table

Table 14-25295. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00A0h**
RTI0	**0E00 00A0h**
RTI1	**0E01 00A0h**
RTI8	**0E08 00A0h**
RTI9	**0E09 00A0h**
RTI10	**0E0A 00A0h**
RTI11	**0E0B 00A0h**

Figure 14-8346. RTI_RTIDWDCNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							DWDCNTR
NONE							R
0h							1FFFFFFh
23	22	21	20	19	18	17	16
DWDCNTR							
R							
1FFFFFFh							
15	14	13	12	11	10	9	8
DWDCNTR							
R							
1FFFFFFh							
7	6	5	4	3	2	1	0
DWDCNTR							
R							
1FFFFFFh							

Table 14-25297. RTI_RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:0	DWDCNTR	R	1FFFFFFh	The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second. User and privilege mode (read): Reads return the current counter value. Privilege mode (write): Writes don't have an effect. Reset Source: mod_g_rst_n

14.9.5.2.2.33 RTI_RTIDWWDRXNCTRL Register

1 RTI_RTIDWWDRXNCTRL Register (Offset = A4h) [reset = 5h]

Digital Windowed Watchdog Reaction Control

Return to Summary Table

Table 14-25298. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00A4h**
RTI0	**0E00 00A4h**
RTI1	**0E01 00A4h**
RTI8	**0E08 00A4h**
RTI9	**0E09 00A4h**
RTI10	**0E0A 00A4h**
RTI11	**0E0B 00A4h**

Figure 14-8347. RTI_RTIDWWDRXNCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				WWDRXN			
NONE				R/W			
0h				5h			

Table 14-25300. RTI_RTIDWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

Table 14-25300. RTI_RTIDWWDRXNCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	WWDRXN	R/W	5h	User and privilege mode (read), privileged mode (write): 0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. 0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Note: Configuration of DWWD Reaction The DWWD reaction can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced. Reset Source: mod_g_rst_n

14.9.5.2.2.34 RTI_RTIDWWDSIZECTRL Register

1 RTI_RTIDWWDSIZECTRL Register (Offset = A8h) [reset = 5h]

Digital Windowed Watchdog Window Size Control

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Table 14-25301. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00A8h**
RTI0	**0E00 00A8h**
RTI1	**0E01 00A8h**
RTI8	**0E08 00A8h**
RTI9	**0E09 00A8h**
RTI10	**0E0A 00A8h**
RTI11	**0E0B 00A8h**

Figure 14-8348. RTI_RTIDWWDSIZECTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WWDSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">WWDSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">WWDSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WWDSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
</table>

Table 14-25303. RTI_RTIDWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WWDSIZE	R/W	5h	User and privilege mode (read), privileged mode (write): Table 3. Windowed Watchdog Window Size Configuration Value written to WWDSIZE Window Size 0x00000005 100% (The functionality is the same as the standard time-out digital watchdog.) 0x00000050 50% 0x00000500 25% 0x00005000 12.5% 0x00050000 6.25% 0x00500000 3.125% Any other 3.125% value Note: Incorrect value being written to watchdog window size control register If an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration. Note: Configuration of DWWD Window Size The DWWD window size can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDSIZE is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced. Reset Source: mod_g_rst_n

14.9.5.2.2.35 RTI_RTIINTCLRENABLE Register

1 RTI_RTIINTCLRENABLE Register (Offset = ACh) [reset = 5050505h]

RTI Compare Interrupt Clear Enable Register

Return to Summary Table

Table 14-25304. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00ACh**
RTI0	**0E00 00ACh**
RTI1	**0E01 00ACh**
RTI8	**0E08 00ACh**
RTI9	**0E09 00ACh**
RTI10	**0E0A 00ACh**
RTI11	**0E0B 00ACh**

Figure 14-8349. RTI_RTIINTCLRENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED				INTCLRENABLE3			
NONE				R/W			
0h				5h			
23	22	21	20	19	18	17	16
RESERVED				INTCLRENABLE2			
NONE				R/W			
0h				5h			
15	14	13	12	11	10	9	8
RESERVED				INTCLRENABLE1			
NONE				R/W			
0h				5h			
7	6	5	4	3	2	1	0
RESERVED				INTCLRENABLE0			
NONE				R/W			
0h				5h			

Table 14-25306. RTI_RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	INTCLRENABLE3	R/W	5h	Enables the auto-clear functionality on the compare 3 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 3 interrupt is disabled. Any other value = Auto-clear for compare 3 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 3 interrupt. Any other value = Enables the auto-clear functionality on the compare 3 interrupt. Reset Source: mod_g_rst_n
23:20	RESERVED	NONE	0h	Reserved

Table 14-25306. RTI_RTIINTCLRENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	INTCLRENABLE2	R/W	5h	Enables the auto-clear functionality on the compare 2 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 2 interrupt is disabled. Any other value = Auto-clear for compare 2 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 2 interrupt. Any other value = Enables the auto-clear functionality on the compare 2 interrupt. Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	INTCLRENABLE1	R/W	5h	Enables the auto-clear functionality on the compare 1 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 1 interrupt is disabled. Any other value = Auto-clear for compare 1 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 1 interrupt. Any other value = Enables the auto-clear functionality on the compare 1 interrupt. Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	INTCLRENABLE0	R/W	5h	Enables the auto-clear functionality on the compare 0 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 0 interrupt is disabled. Any other value = Auto-clear for compare 0 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 0 interrupt. Any other value = Enables the auto-clear functionality on the compare 0 interrupt. Note: Hook-up of Compare Interrupt to a device pin The RTI module generates up to 4 compare interrupts. The connection between one or more of these compare interrupt(s) to a device pin is completely device-dependent. Refer to the device datasheet to identify the actual pin(s) that connects to the compare interrupt(s). Reset Source: mod_g_rst_n

14.9.5.2.2.36 RTI_RTICOMP0CLR Register

1 RTI_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

RTI Compare 0 Clear Register

Return to Summary Table

Table 14-25307. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00B0h**
RTI0	**0E00 00B0h**
RTI1	**0E01 00B0h**
RTI8	**0E08 00B0h**
RTI9	**0E09 00B0h**
RTI10	**0E0A 00B0h**
RTI11	**0E0B 00B0h**

Figure 14-8350. RTI_RTICOMP0CLR Name Register

31	30	29	28	27	26	25	24
COMP0CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP0CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP0CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP0CLR							
R/W							
0h							

Table 14-25309. RTI_RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.5.2.2.37 RTI_RTICOMP1CLR Register

1 RTI_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

RTI Compare 1 Clear Register

Return to Summary Table

Table 14-25310. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00B4h**
RTI0	**0E00 00B4h**
RTI1	**0E01 00B4h**
RTI8	**0E08 00B4h**
RTI9	**0E09 00B4h**
RTI10	**0E0A 00B4h**
RTI11	**0E0B 00B4h**

Figure 14-8351. RTI_RTICOMP1CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COMP1CLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COMP1CLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COMP1CLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP1CLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25312. RTI_RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 1 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.5.2.2.38 RTI_RTICOMP2CLR Register

1 RTI_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

RTI Compare 2 Clear Register

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Table 14-25313. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00B8h**
RTI0	**0E00 00B8h**
RTI1	**0E01 00B8h**
RTI8	**0E08 00B8h**
RTI9	**0E09 00B8h**
RTI10	**0E0A 00B8h**
RTI11	**0E0B 00B8h**

Figure 14-8352. RTI_RTICOMP2CLR Name Register

31	30	29	28	27	26	25	24
COMP2CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP2CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP2CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP2CLR							
R/W							
0h							

Table 14-25315. RTI_RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 2 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.5.2.2.39 RTI_RTICOMP3CLR Register

1 RTI_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

RTI Compare 3 Clear Register

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Table 14-25316. Instance Table

Instance Name	Physical Address
MCU_RTI0	**0488 00BCh**
RTI0	**0E00 00BCh**
RTI1	**0E01 00BCh**
RTI8	**0E08 00BCh**
RTI9	**0E09 00BCh**
RTI10	**0E0A 00BCh**
RTI11	**0E0B 00BCh**

Figure 14-8353. RTI_RTICOMP3CLR Name Register

31	30	29	28	27	26	25	24
COMP3CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP3CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP3CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP3CLR							
R/W							
0h							

Table 14-25318. RTI_RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 3 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.9.5.3 TIMER

TIMER

14.9.5.3.1 TIMER Summaries

TIMER Summaries

Table 14-25319. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER0 Physical Address	TIMER1 Physical Address	TIMER10 Physical Address
0h	32	DMTIMER1MS_TIDR	0480 0000h	0481 0000h	0482 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0480 0010h	0481 0010h	0482 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0480 0020h	0481 0020h	0482 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0480 0024h	0481 0024h	0482 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0480 0028h	0481 0028h	0482 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0480 002Ch	0481 002Ch	0482 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0480 0030h	0481 0030h	0482 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0480 0034h	0481 0034h	0482 0034h
38h	32	DMTIMER1MS_TCLR	0480 0038h	0481 0038h	0482 0038h
3Ch	32	DMTIMER1MS_TCRR	0480 003Ch	0481 003Ch	0482 003Ch
40h	32	DMTIMER1MS_TLDR	0480 0040h	0481 0040h	0482 0040h
44h	32	DMTIMER1MS_TTGR	0480 0044h	0481 0044h	0482 0044h
48h	32	DMTIMER1MS_TWPS	0480 0048h	0481 0048h	0482 0048h
4Ch	32	DMTIMER1MS_TMAR	0480 004Ch	0481 004Ch	0482 004Ch
50h	32	DMTIMER1MS_TCAR1	0480 0050h	0481 0050h	0482 0050h
54h	32	DMTIMER1MS_TSICR	0480 0054h	0481 0054h	0482 0054h
58h	32	DMTIMER1MS_TCAR2	0480 0058h	0481 0058h	0482 0058h
5Ch	32	DMTIMER1MS_TPIR	0480 005Ch	0481 005Ch	0482 005Ch
60h	32	DMTIMER1MS_TNIR	0480 0060h	0481 0060h	0482 0060h
64h	32	DMTIMER1MS_TCVR	0480 0064h	0481 0064h	0482 0064h
68h	32	DMTIMER1MS_TOCR	0480 0068h	0481 0068h	0482 0068h
6Ch	32	DMTIMER1MS_TOWR	0480 006Ch	0481 006Ch	0482 006Ch

Table 14-25320. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER11 Physical Address	TIMER2 Physical Address	TIMER3 Physical Address
0h	32	DMTIMER1MS_TIDR	0483 0000h	0240 0000h	0241 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0483 0010h	0240 0010h	0241 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0483 0020h	0240 0020h	0241 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0483 0024h	0240 0024h	0241 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0483 0028h	0240 0028h	0241 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0483 002Ch	0240 002Ch	0241 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0483 0030h	0240 0030h	0241 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0483 0034h	0240 0034h	0241 0034h
38h	32	DMTIMER1MS_TCLR	0483 0038h	0240 0038h	0241 0038h
3Ch	32	DMTIMER1MS_TCRR	0483 003Ch	0240 003Ch	0241 003Ch
40h	32	DMTIMER1MS_TLDR	0483 0040h	0240 0040h	0241 0040h

Table 14-25320. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	TIMER11 Physical Address	TIMER2 Physical Address	TIMER3 Physical Address
44h	32	DMTIMER1MS_TTGR	0483 0044h	0240 0044h	0241 0044h
48h	32	DMTIMER1MS_TWPS	0483 0048h	0240 0048h	0241 0048h
4Ch	32	DMTIMER1MS_TMAR	0483 004Ch	0240 004Ch	0241 004Ch
50h	32	DMTIMER1MS_TCAR1	0483 0050h	0240 0050h	0241 0050h
54h	32	DMTIMER1MS_TSICR	0483 0054h	0240 0054h	0241 0054h
58h	32	DMTIMER1MS_TCAR2	0483 0058h	0240 0058h	0241 0058h
5Ch	32	DMTIMER1MS_TPIR	0483 005Ch	0240 005Ch	0241 005Ch
60h	32	DMTIMER1MS_TNIR	0483 0060h	0240 0060h	0241 0060h
64h	32	DMTIMER1MS_TCVR	0483 0064h	0240 0064h	0241 0064h
68h	32	DMTIMER1MS_TOCR	0483 0068h	0240 0068h	0241 0068h
6Ch	32	DMTIMER1MS_TOWR	0483 006Ch	0240 006Ch	0241 006Ch

Table 14-25321. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER4 Physical Address	TIMER5 Physical Address	TIMER6 Physical Address
0h	32	DMTIMER1MS_TIDR	0242 0000h	0243 0000h	0244 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0242 0010h	0243 0010h	0244 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0242 0020h	0243 0020h	0244 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0242 0024h	0243 0024h	0244 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0242 0028h	0243 0028h	0244 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0242 002Ch	0243 002Ch	0244 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0242 0030h	0243 0030h	0244 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0242 0034h	0243 0034h	0244 0034h
38h	32	DMTIMER1MS_TCLR	0242 0038h	0243 0038h	0244 0038h
3Ch	32	DMTIMER1MS_TCRR	0242 003Ch	0243 003Ch	0244 003Ch
40h	32	DMTIMER1MS_TLDR	0242 0040h	0243 0040h	0244 0040h
44h	32	DMTIMER1MS_TTGR	0242 0044h	0243 0044h	0244 0044h
48h	32	DMTIMER1MS_TWPS	0242 0048h	0243 0048h	0244 0048h
4Ch	32	DMTIMER1MS_TMAR	0242 004Ch	0243 004Ch	0244 004Ch
50h	32	DMTIMER1MS_TCAR1	0242 0050h	0243 0050h	0244 0050h
54h	32	DMTIMER1MS_TSICR	0242 0054h	0243 0054h	0244 0054h
58h	32	DMTIMER1MS_TCAR2	0242 0058h	0243 0058h	0244 0058h
5Ch	32	DMTIMER1MS_TPIR	0242 005Ch	0243 005Ch	0244 005Ch
60h	32	DMTIMER1MS_TNIR	0242 0060h	0243 0060h	0244 0060h
64h	32	DMTIMER1MS_TCVR	0242 0064h	0243 0064h	0244 0064h
68h	32	DMTIMER1MS_TOCR	0242 0068h	0243 0068h	0244 0068h
6Ch	32	DMTIMER1MS_TOWR	0242 006Ch	0243 006Ch	0244 006Ch

Table 14-25322. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER7 Physical Address	TIMER8 Physical Address	TIMER9 Physical Address
0h	32	DMTIMER1MS_TIDR	0245 0000h	0246 0000h	0247 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0245 0010h	0246 0010h	0247 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0245 0020h	0246 0020h	0247 0020h

Table 14-25322. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	TIMER7 Physical Address	TIMER8 Physical Address	TIMER9 Physical Address
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0245 0024h	0246 0024h	0247 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0245 0028h	0246 0028h	0247 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0245 002Ch	0246 002Ch	0247 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0245 0030h	0246 0030h	0247 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0245 0034h	0246 0034h	0247 0034h
38h	32	DMTIMER1MS_TCLR	0245 0038h	0246 0038h	0247 0038h
3Ch	32	DMTIMER1MS_TCRR	0245 003Ch	0246 003Ch	0247 003Ch
40h	32	DMTIMER1MS_TLDR	0245 0040h	0246 0040h	0247 0040h
44h	32	DMTIMER1MS_TTGR	0245 0044h	0246 0044h	0247 0044h
48h	32	DMTIMER1MS_TWPS	0245 0048h	0246 0048h	0247 0048h
4Ch	32	DMTIMER1MS_TMAR	0245 004Ch	0246 004Ch	0247 004Ch
50h	32	DMTIMER1MS_TCAR1	0245 0050h	0246 0050h	0247 0050h
54h	32	DMTIMER1MS_TSICR	0245 0054h	0246 0054h	0247 0054h
58h	32	DMTIMER1MS_TCAR2	0245 0058h	0246 0058h	0247 0058h
5Ch	32	DMTIMER1MS_TPIR	0245 005Ch	0246 005Ch	0247 005Ch
60h	32	DMTIMER1MS_TNIR	0245 0060h	0246 0060h	0247 0060h
64h	32	DMTIMER1MS_TCVR	0245 0064h	0246 0064h	0247 0064h
68h	32	DMTIMER1MS_TOCR	0245 0068h	0246 0068h	0247 0068h
6Ch	32	DMTIMER1MS_TOWR	0245 006Ch	0246 006Ch	0247 006Ch

Table 14-25323. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	MCU_TIMER0 Physical Address	MCU_TIMER1 Physical Address	MCU_TIMER2 Physical Address
0h	32	DMTIMER1MS_TIDR	0248 0000h	0249 0000h	024A 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0248 0010h	0249 0010h	024A 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0248 0020h	0249 0020h	024A 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0248 0024h	0249 0024h	024A 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0248 0028h	0249 0028h	024A 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0248 002Ch	0249 002Ch	024A 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0248 0030h	0249 0030h	024A 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0248 0034h	0249 0034h	024A 0034h
38h	32	DMTIMER1MS_TCLR	0248 0038h	0249 0038h	024A 0038h
3Ch	32	DMTIMER1MS_TCRR	0248 003Ch	0249 003Ch	024A 003Ch
40h	32	DMTIMER1MS_TLDR	0248 0040h	0249 0040h	024A 0040h
44h	32	DMTIMER1MS_TTGR	0248 0044h	0249 0044h	024A 0044h
48h	32	DMTIMER1MS_TWPS	0248 0048h	0249 0048h	024A 0048h
4Ch	32	DMTIMER1MS_TMAR	0248 004Ch	0249 004Ch	024A 004Ch
50h	32	DMTIMER1MS_TCAR1	0248 0050h	0249 0050h	024A 0050h
54h	32	DMTIMER1MS_TSICR	0248 0054h	0249 0054h	024A 0054h
58h	32	DMTIMER1MS_TCAR2	0248 0058h	0249 0058h	024A 0058h
5Ch	32	DMTIMER1MS_TPIR	0248 005Ch	0249 005Ch	024A 005Ch
60h	32	DMTIMER1MS_TNIR	0248 0060h	0249 0060h	024A 0060h
64h	32	DMTIMER1MS_TCVR	0248 0064h	0249 0064h	024A 0064h
68h	32	DMTIMER1MS_TOCR	0248 0068h	0249 0068h	024A 0068h

Table 14-25323. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCU_TIMER0 Physical Address	MCU_TIMER1 Physical Address	MCU_TIMER2 Physical Address
6Ch	32	DMTIMER1MS_TOWR	0248 006Ch	0249 006Ch	024A 006Ch

Table 14-25324. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	MCU_TIMER3 Physical Address
0h	32	DMTIMER1MS_TIDR	024B 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	024B 0010h
20h	32	DMTIMER1MS_IRQ_EOI	024B 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	024B 0024h
28h	32	DMTIMER1MS_IRQSTATUS	024B 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	024B 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	024B 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	024B 0034h
38h	32	DMTIMER1MS_TCLR	024B 0038h
3Ch	32	DMTIMER1MS_TCRR	024B 003Ch
40h	32	DMTIMER1MS_TLDR	024B 0040h
44h	32	DMTIMER1MS_TTGR	024B 0044h
48h	32	DMTIMER1MS_TWPS	024B 0048h
4Ch	32	DMTIMER1MS_TMAR	024B 004Ch
50h	32	DMTIMER1MS_TCAR1	024B 0050h
54h	32	DMTIMER1MS_TSICR	024B 0054h
58h	32	DMTIMER1MS_TCAR2	024B 0058h
5Ch	32	DMTIMER1MS_TPIR	024B 005Ch
60h	32	DMTIMER1MS_TNIR	024B 0060h
64h	32	DMTIMER1MS_TCVR	024B 0064h
68h	32	DMTIMER1MS_TOCR	024B 0068h
6Ch	32	DMTIMER1MS_TOWR	024B 006Ch

14.9.5.3.2 TIMER Registers

TIMER Registers

14.9.5.3.2.1 DMTIMER1MS_TIDR Register

1 DMTIMER1MS_TIDR Register (Offset = 0h) [reset = 50003900h]

Peripheral ID

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Table 14-25325. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0000h**
MCU_TIMER1	**0481 0000h**
MCU_TIMER2	**0482 0000h**
MCU_TIMER3	**0483 0000h**
TIMER0	**0240 0000h**
TIMER1	**0241 0000h**
TIMER2	**0242 0000h**
TIMER3	**0243 0000h**
TIMER4	**0244 0000h**
TIMER5	**0245 0000h**
TIMER6	**0246 0000h**
TIMER7	**0247 0000h**
TIMER8	**0248 0000h**
TIMER9	**0249 0000h**
TIMER10	**024A 0000h**
TIMER11	**024B 0000h**

Figure 14-8354. DMTIMER1MS_TIDR Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		1h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
7h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-25327. DMTIMER1MS_TIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: mod_g_rst_n

Table 14-25327. DMTIMER1MS_TIDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

29:28	BU	R	1h	Business Unit
				Reset Source: mod_g_rst_n
				`1 Wireless BU`
				`2 Processors BU`

27:16	MODULE_ID	R	0h	Module ID Reset Source: mod_g_rst_n
15:11	RTL	R	7h	RTL revision. Will vary depending on release. Reset Source: mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: mod_g_rst_n

14.9.5.3.2.2 DMTIMER1MS_TIOCP_CFG Register

1 DMTIMER1MS_TIOCP_CFG Register (Offset = 10h) [reset = 8h]

This register controls the various parameters of the OCP interface

Return to Summary Table

Table 14-25328. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0010h**
MCU_TIMER1	**0481 0010h**
MCU_TIMER2	**0482 0010h**
MCU_TIMER3	**0483 0010h**
TIMER0	**0240 0010h**
TIMER1	**0241 0010h**
TIMER2	**0242 0010h**
TIMER3	**0243 0010h**
TIMER4	**0244 0010h**
TIMER5	**0245 0010h**
TIMER6	**0246 0010h**
TIMER7	**0247 0010h**
TIMER8	**0248 0010h**
TIMER9	**0249 0010h**
TIMER10	**024A 0010h**
TIMER11	**024B 0010h**

Figure 14-8355. DMTIMER1MS_TIOCP_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				IDLEMODE		EMUFREE	SOFTRESET
NONE				R/W		R/W	R/W
0h				2h		0h	0h

Table 14-25330. DMTIMER1MS_TIOCP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

Table 14-25330. DMTIMER1MS_TIOCP_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	IDLEMODE	R/W	2h	Idle Mode Reset Source: mod_g_rst_n 0 local target's idle state follows (acknowledges) the system's idle reuquests unconditionaly, i.e. regardless of the IP module's internal requirments. Back mode, for debug only. 1 local target never enteres idle state. Back mode, for debug only. 2 local target's idle state eventually follows (acknowledges) the systems' idle requests, depending on the IP module's internal requirments. IP module shall not generate (IRQ- or DMA-request-releated) wakeup events. 3 local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirents. IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state. Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) impolemented.
1	EMUFREE	R/W	0h	Emulation Mode Reset Source: mod_g_rst_n 0 The timer is frozen in emulation mode (PI_SUSPEND signal active) 1 The timer runs free, regardless of PI_SUSPEND value
0	SOFTRESET	R/W	0h	Software reset Reset Source: mod_g_rst_n 0 Read: Reset Done, no pending action Write: no action 1 Read: Reset ongoing Write: initiate software reset

14.9.5.3.2.3 DMTIMER1MS_IRQ_EOI Register

1 DMTIMER1MS_IRQ_EOI Register (Offset = 20h) [reset = 0h]

Allows the generation of further pulses on the interrupt line, if an new interrupt event is pending, when using the pulsed output. Unused when using the level interrupt line

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Table 14-25331. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0020h
MCU_TIMER1	0481 0020h
MCU_TIMER2	0482 0020h
MCU_TIMER3	0483 0020h
TIMER0	0240 0020h
TIMER1	0241 0020h
TIMER2	0242 0020h
TIMER3	0243 0020h
TIMER4	0244 0020h
TIMER5	0245 0020h
TIMER6	0246 0020h
TIMER7	0247 0020h
TIMER8	0248 0020h
TIMER9	0249 0020h
TIMER10	024A 0020h
TIMER11	024B 0020h

Figure 14-8356. DMTIMER1MS_IRQ_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LINE_NUMBER</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-25333. DMTIMER1MS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved

Table 14-25333. DMTIMER1MS_IRQ_EOI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LINE_NUMBER	R/W	0h	Idle Mode Reset Source: mod_g_rst_n 0 `End of interrupt`

14.9.5.3.2.4 DMTIMER1MS_IRQSTATUS_RAW Register

1 DMTIMER1MS_IRQSTATUS_RAW Register (Offset = 24h) [reset = 0h]

Component interrupt request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug

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Table 14-25334. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0024h**
MCU_TIMER1	**0481 0024h**
MCU_TIMER2	**0482 0024h**
MCU_TIMER3	**0483 0024h**
TIMER0	**0240 0024h**
TIMER1	**0241 0024h**
TIMER2	**0242 0024h**
TIMER3	**0243 0024h**
TIMER4	**0244 0024h**
TIMER5	**0245 0024h**
TIMER6	**0246 0024h**
TIMER7	**0247 0024h**
TIMER8	**0248 0024h**
TIMER9	**0249 0024h**
TIMER10	**024A 0024h**
TIMER11	**024B 0024h**

Figure 14-8357. DMTIMER1MS_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-25336. DMTIMER1MS_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-25336. DMTIMER1MS_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TCAR_IT_FLAG	R/W1TS	0h	Capture Interrupt Reset Source: mod_g_rst_n
1	OVF_IT_FLAG	R/W1TS	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TS	0h	Match Interrupt Reset Source: mod_g_rst_n

14.9.5.3.2.5 DMTIMER1MS_IRQSTATUS Register

1 DMTIMER1MS_IRQSTATUS Register (Offset = 28h) [reset = 0h]

Component interrupt request status. Check the corresponding secondary status register.Enabled status isn't set unless event is enabled.Write 1 to clear the status after interrupt has been serviced;raw status gets cleared, i.e. even if not enabled

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Table 14-25337. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0028h**
MCU_TIMER1	**0481 0028h**
MCU_TIMER2	**0482 0028h**
MCU_TIMER3	**0483 0028h**
TIMER0	**0240 0028h**
TIMER1	**0241 0028h**
TIMER2	**0242 0028h**
TIMER3	**0243 0028h**
TIMER4	**0244 0028h**
TIMER5	**0245 0028h**
TIMER6	**0246 0028h**
TIMER7	**0247 0028h**
TIMER8	**0248 0028h**
TIMER9	**0249 0028h**
TIMER10	**024A 0028h**
TIMER11	**024B 0028h**

Figure 14-8358. DMTIMER1MS_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-25339. DMTIMER1MS_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-25339. DMTIMER1MS_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TCAR_IT_FLAG	R/W1TC	0h	Capture Interrupt Reset Source: mod_g_rst_n
1	OVF_IT_FLAG	R/W1TC	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TC	0h	Match Interrupt Reset Source: mod_g_rst_n

14.9.5.3.2.6 DMTIMER1MS_IRQSTATUS_SET Register

1 DMTIMER1MS_IRQSTATUS_SET Register (Offset = 2Ch) [reset = 0h]

Component interrupt request enable Write 1 to set;enable interrupt. Readout equal to corresponding _CLR register.

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Table 14-25340. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 002Ch**
MCU_TIMER1	**0481 002Ch**
MCU_TIMER2	**0482 002Ch**
MCU_TIMER3	**0483 002Ch**
TIMER0	**0240 002Ch**
TIMER1	**0241 002Ch**
TIMER2	**0242 002Ch**
TIMER3	**0243 002Ch**
TIMER4	**0244 002Ch**
TIMER5	**0245 002Ch**
TIMER6	**0246 002Ch**
TIMER7	**0247 002Ch**
TIMER8	**0248 002Ch**
TIMER9	**0249 002Ch**
TIMER10	**024A 002Ch**
TIMER11	**024B 002Ch**

Figure 14-8359. DMTIMER1MS_IRQSTATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>TCAR_IT_FLAG</td><td>OVF_IT_FLAG</td><td>MAT_IT_FLAG</td></tr>
<tr><td colspan="5">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25342. DMTIMER1MS_IRQSTATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-25342. DMTIMER1MS_IRQSTATUS_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TCAR_IT_FLAG	R/W1TS	0h	Capture Interrupt Reset Source: mod_g_rst_n
1	OVF_IT_FLAG	R/W1TS	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TS	0h	Match Interrupt Reset Source: mod_g_rst_n

14.9.5.3.2.7 DMTIMER1MS_IRQSTATUS_CLR Register

1 DMTIMER1MS_IRQSTATUS_CLR Register (Offset = 30h) [reset = 0h]

Component interrupt request enable. Write 1 to clear; disable interrupt. Readout equal to corresponding _SET register

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Table 14-25343. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0030h**
MCU_TIMER1	**0481 0030h**
MCU_TIMER2	**0482 0030h**
MCU_TIMER3	**0483 0030h**
TIMER0	**0240 0030h**
TIMER1	**0241 0030h**
TIMER2	**0242 0030h**
TIMER3	**0243 0030h**
TIMER4	**0244 0030h**
TIMER5	**0245 0030h**
TIMER6	**0246 0030h**
TIMER7	**0247 0030h**
TIMER8	**0248 0030h**
TIMER9	**0249 0030h**
TIMER10	**024A 0030h**
TIMER11	**024B 0030h**

Figure 14-8360. DMTIMER1MS_IRQSTATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-25345. DMTIMER1MS_IRQSTATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-25345. DMTIMER1MS_IRQSTATUS_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TCAR_IT_FLAG	R/W1TC	0h	Capture Interrupt Reset Source: mod_g_rst_n
1	OVF_IT_FLAG	R/W1TC	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TC	0h	Match Interrupt Reset Source: mod_g_rst_n

14.9.5.3.2.8 DMTIMER1MS_IRQWAKEEN Register

1 DMTIMER1MS_IRQWAKEEN Register (Offset = 34h) [reset = 0h]

Wakeup-enabled events taking place when module is idle shall generate an asynchronous wakeup

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Table 14-25346. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0034h**
MCU_TIMER1	**0481 0034h**
MCU_TIMER2	**0482 0034h**
MCU_TIMER3	**0483 0034h**
TIMER0	**0240 0034h**
TIMER1	**0241 0034h**
TIMER2	**0242 0034h**
TIMER3	**0243 0034h**
TIMER4	**0244 0034h**
TIMER5	**0245 0034h**
TIMER6	**0246 0034h**
TIMER7	**0247 0034h**
TIMER8	**0248 0034h**
TIMER9	**0249 0034h**
TIMER10	**024A 0034h**
TIMER11	**024B 0034h**

Figure 14-8361. DMTIMER1MS_IRQWAKEEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MAT_WUP_ENA	OVF_WUP_ENA	TCAR_WUP_ENA
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-25348. DMTIMER1MS_IRQWAKEEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-25348. DMTIMER1MS_IRQWAKEEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MAT_WUP_ENA	R/W	0h	Match Wakeup Enable Reset Source: mod_g_rst_n
1	OVF_WUP_ENA	R/W	0h	Overflow Wakeup Enable Reset Source: mod_g_rst_n
0	TCAR_WUP_ENA	R/W	0h	Capture Wakeup Enable Reset Source: mod_g_rst_n

14.9.5.3.2.9 DMTIMER1MS_TCLR Register

1 DMTIMER1MS_TCLR Register (Offset = 38h) [reset = 0h]

This register controls optional features specific to the timer functionality

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Table 14-25349. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0038h**
MCU_TIMER1	**0481 0038h**
MCU_TIMER2	**0482 0038h**
MCU_TIMER3	**0483 0038h**
TIMER0	**0240 0038h**
TIMER1	**0241 0038h**
TIMER2	**0242 0038h**
TIMER3	**0243 0038h**
TIMER4	**0244 0038h**
TIMER5	**0245 0038h**
TIMER6	**0246 0038h**
TIMER7	**0247 0038h**
TIMER8	**0248 0038h**
TIMER9	**0249 0038h**
TIMER10	**024A 0038h**
TIMER11	**024B 0038h**

Figure 14-8362. DMTIMER1MS_TCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	GPO_CFG	CAPT_MODE	PT	TRG		TCM	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
7	6	5	4	3	2	1	0
SCPWM	CE	PRE	PTV			AR	ST
R/W	R/W	R/W	R/W			R/W	R/W
0h	0h	0h	0h			0h	0h

Table 14-25351. DMTIMER1MS_TCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	GPO_CFG	R/W	0h	This field drives directly the timer_gpocfg port Reset Source: mod_g_rst_n

Table 14-25351. DMTIMER1MS_TCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CAPT_MODE	R/W	0h	Capture mode select bit; First/second Reset Source: mod_g_rst_n 0 Capture first enabled capture event in TCAR1 1 Capture first enabled capture event in TCAR2
12	PT	R/W	0h	Pulse or Toggle select bit Reset Source: mod_g_rst_n 0 Pulse modulation 0 Toggle modulation
11:10	TRG	R/W	0h	Trigger Output Mode Reset Source: mod_g_rst_n 0 No Trigger 1 Overflow Trigger 2 Overflow and match Trigger
9:8	TCM	R/W	0h	Transition Capture Mode Reset Source: mod_g_rst_n 0 No capture 1 Capture on rising edges of PI_EVNETCAPT 2 Capture on falling edges of PI_EVENTCAPT 3 Capture on both edges of PI_EVNENTCAPT
7	SCPWM	R/W	0h	Pulse Width Modulation output pin default value Reset Source: mod_g_rst_n
6	CE	R/W	0h	Compare Enable Reset Source: mod_g_rst_n 0 compare disabled 1 compare enabled
5	PRE	R/W	0h	Prescaler Enable Reset Source: mod_g_rst_n 0 Prescaler disabeld 1 Prescaler Enabled
4:2	PTV	R/W	0h	Trigger Output Mode. The timer counter is prescaled with the value: 2^PTV Reset Source: mod_g_rst_n
1	AR	R/W	0h	Auto-reload mode Reset Source: mod_g_rst_n 0 One shot mode overflow 1 Auto-reload mode overflow
0	ST	R/W	0h	Start/Stop timer control Reset Source: mod_g_rst_n 0 Stop the timer 1 Start the timer

14.9.5.3.2.10 DMTIMER1MS_TCRR Register

1 DMTIMER1MS_TCRR Register (Offset = 3Ch) [reset = 0h]

This register holds the value of the internal counter

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Table 14-25352. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 003Ch**
MCU_TIMER1	**0481 003Ch**
MCU_TIMER2	**0482 003Ch**
MCU_TIMER3	**0483 003Ch**
TIMER0	**0240 003Ch**
TIMER1	**0241 003Ch**
TIMER2	**0242 003Ch**
TIMER3	**0243 003Ch**
TIMER4	**0244 003Ch**
TIMER5	**0245 003Ch**
TIMER6	**0246 003Ch**
TIMER7	**0247 003Ch**
TIMER8	**0248 003Ch**
TIMER9	**0249 003Ch**
TIMER10	**024A 003Ch**
TIMER11	**024B 003Ch**

Figure 14-8363. DMTIMER1MS_TCRR Name Register

31	30	29	28	27	26	25	24
TIMER_COUNTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TIMER_COUNTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TIMER_COUNTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TIMER_COUNTER							
R/W							
0h							

Table 14-25354. DMTIMER1MS_TCRR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIMER_COUNTER	R/W	0h	Timer Counter Reset Source: mod_g_rst_n

14.9.5.3.2.11 DMTIMER1MS_TLDR Register

1 DMTIMER1MS_TLDR Register (Offset = 40h) [reset = 0h]

This register holds the timer's load value

Return to Summary Table

Table 14-25355. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0040h**
MCU_TIMER1	**0481 0040h**
MCU_TIMER2	**0482 0040h**
MCU_TIMER3	**0483 0040h**
TIMER0	**0240 0040h**
TIMER1	**0241 0040h**
TIMER2	**0242 0040h**
TIMER3	**0243 0040h**
TIMER4	**0244 0040h**
TIMER5	**0245 0040h**
TIMER6	**0246 0040h**
TIMER7	**0247 0040h**
TIMER8	**0248 0040h**
TIMER9	**0249 0040h**
TIMER10	**024A 0040h**
TIMER11	**024B 0040h**

Figure 14-8364. DMTIMER1MS_TLDR Name Register

31	30	29	28	27	26	25	24
LOAD_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
LOAD_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
LOAD_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
LOAD_VALUE							
R/W							
0h							

Table 14-25357. DMTIMER1MS_TLDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOAD_VALUE	R/W	0h	Timer Counter Reset Source: mod_g_rst_n

14.9.5.3.2.12 DMTIMER1MS_TTGR Register

1 DMTIMER1MS_TTGR Register (Offset = 44h) [reset = 0h]

This register triggers a counter reload of timer by writing any value in it

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Table 14-25358. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0044h**
MCU_TIMER1	**0481 0044h**
MCU_TIMER2	**0482 0044h**
MCU_TIMER3	**0483 0044h**
TIMER0	**0240 0044h**
TIMER1	**0241 0044h**
TIMER2	**0242 0044h**
TIMER3	**0243 0044h**
TIMER4	**0244 0044h**
TIMER5	**0245 0044h**
TIMER6	**0246 0044h**
TIMER7	**0247 0044h**
TIMER8	**0248 0044h**
TIMER9	**0249 0044h**
TIMER10	**024A 0044h**
TIMER11	**024B 0044h**

Figure 14-8365. DMTIMER1MS_TTGR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TTRG_VLAUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TTRG_VLAUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TTRG_VLAUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TTRG_VLAUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25360. DMTIMER1MS_TTGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TTRG_VLAUE	R/W	0h	The value of the trigger register. During reads, it always return 0xFFFF_FFFF Reset Source: mod_g_rst_n

14.9.5.3.2.13 DMTIMER1MS_TWPS Register

1 DMTIMER1MS_TWPS Register (Offset = 48h) [reset = 0h]

This register contains the write posting bits for all writ-able functional registers

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Table 14-25361. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0048h
MCU_TIMER1	0481 0048h
MCU_TIMER2	0482 0048h
MCU_TIMER3	0483 0048h
TIMER0	0240 0048h
TIMER1	0241 0048h
TIMER2	0242 0048h
TIMER3	0243 0048h
TIMER4	0244 0048h
TIMER5	0245 0048h
TIMER6	0246 0048h
TIMER7	0247 0048h
TIMER8	0248 0048h
TIMER9	0249 0048h
TIMER10	024A 0048h
TIMER11	024B 0048h

Figure 14-8366. DMTIMER1MS_TWPS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						W_PEND_TOWR	W_PEND_TOCR
NONE						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
W_PEND_TCVR	W_PEND_TNIR	W_PEND_TPIR	W_PEND_TMAR	W_PEND_TTGR	W_PEND_TLDR	W_PEND_TCRR	W_PEND_TCLR
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-25363. DMTIMER1MS_TWPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved

Table 14-25363. DMTIMER1MS_TWPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	W_PEND_TOWR	R	0h	Write pending for register TOWR Reset Source: mod_g_rst_n
8	W_PEND_TOCR	R	0h	Write pending for register TOCR Reset Source: mod_g_rst_n
7	W_PEND_TCVR	R	0h	Write pending for register TCVR Reset Source: mod_g_rst_n
6	W_PEND_TNIR	R	0h	Write pending for register TNIR Reset Source: mod_g_rst_n
5	W_PEND_TPIR	R	0h	Write pending for register TPIR Reset Source: mod_g_rst_n
4	W_PEND_TMAR	R	0h	Write pending for register TMAR Reset Source: mod_g_rst_n
3	W_PEND_TTGR	R	0h	Write pending for register TTGR Reset Source: mod_g_rst_n
2	W_PEND_TLDR	R	0h	Write pending for register TLDR Reset Source: mod_g_rst_n
1	W_PEND_TCRR	R	0h	Write pending for register TCRR Reset Source: mod_g_rst_n
0	W_PEND_TCLR	R	0h	Write pending for register TCLR Reset Source: mod_g_rst_n

14.9.5.3.2.14 DMTIMER1MS_TMAR Register

1 DMTIMER1MS_TMAR Register (Offset = 4Ch) [reset = 0h]

This register holds the match value to be compared with the counter's value

Return to Summary Table

Table 14-25364. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 004Ch
MCU_TIMER1	0481 004Ch
MCU_TIMER2	0482 004Ch
MCU_TIMER3	0483 004Ch
TIMER0	0240 004Ch
TIMER1	0241 004Ch
TIMER2	0242 004Ch
TIMER3	0243 004Ch
TIMER4	0244 004Ch
TIMER5	0245 004Ch
TIMER6	0246 004Ch
TIMER7	0247 004Ch
TIMER8	0248 004Ch
TIMER9	0249 004Ch
TIMER10	024A 004Ch
TIMER11	024B 004Ch

Figure 14-8367. DMTIMER1MS_TMAR Name Register

31	30	29	28	27	26	25	24
COMPARE_VLAUE							
R/W							
0h							
23	22	21	20	19	18	17	16
COMPARE_VLAUE							
R/W							
0h							
15	14	13	12	11	10	9	8
COMPARE_VLAUE							
R/W							
0h							
7	6	5	4	3	2	1	0
COMPARE_VLAUE							
R/W							
0h							

Table 14-25366. DMTIMER1MS_TMAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMPARE_VLAUE	R/W	0h	The value of the match register Reset Source: mod_g_rst_n

14.9.5.3.2.15 DMTIMER1MS_TCAR1 Register

1 DMTIMER1MS_TCAR1 Register (Offset = 50h) [reset = 0h]

This register holds the value of the first counter register capture

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Table 14-25367. Instance Table

Instance Name	Physical Address
MCU_TIMER0	**0480 0050h**
MCU_TIMER1	**0481 0050h**
MCU_TIMER2	**0482 0050h**
MCU_TIMER3	**0483 0050h**
TIMER0	**0240 0050h**
TIMER1	**0241 0050h**
TIMER2	**0242 0050h**
TIMER3	**0243 0050h**
TIMER4	**0244 0050h**
TIMER5	**0245 0050h**
TIMER6	**0246 0050h**
TIMER7	**0247 0050h**
TIMER8	**0248 0050h**
TIMER9	**0249 0050h**
TIMER10	**024A 0050h**
TIMER11	**024B 0050h**

Figure 14-8368. DMTIMER1MS_TCAR1 Name Register

31	30	29	28	27	26	25	24
CAPTURE_VALUE1							
R							
0h							
23	22	21	20	19	18	17	16
CAPTURE_VALUE1							
R							
0h							
15	14	13	12	11	10	9	8
CAPTURE_VALUE1							
R							
0h							
7	6	5	4	3	2	1	0
CAPTURE_VALUE1							
R							
0h							

Table 14-25369. DMTIMER1MS_TCAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPTURE_VALUE1	R	0h	The value of first captured counter register Reset Source: mod_g_rst_n

14.9.5.3.2.16 DMTIMER1MS_TSICR Register

1 DMTIMER1MS_TSICR Register (Offset = 54h) [reset = 0h]

Timer Synchronous Interface Control Register

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Table 14-25370. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0054h
MCU_TIMER1	0481 0054h
MCU_TIMER2	0482 0054h
MCU_TIMER3	0483 0054h
TIMER0	0240 0054h
TIMER1	0241 0054h
TIMER2	0242 0054h
TIMER3	0243 0054h
TIMER4	0244 0054h
TIMER5	0245 0054h
TIMER6	0246 0054h
TIMER7	0247 0054h
TIMER8	0248 0054h
TIMER9	0249 0054h
TIMER10	024A 0054h
TIMER11	024B 0054h

Figure 14-8369. DMTIMER1MS_TSICR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			READ_AFTER_IDLE	READ_MODE	POSTED	SFT	RESERVED
NONE			W	W	R/W	R/W	NONE
0h			0h	0h	X	0h	0h

Table 14-25372. DMTIMER1MS_TSICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-25372. DMTIMER1MS_TSICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	READ_AFTER_IDLE	W	0h	Select if the synchronization mechanism used for first TCRR read operation after IDLE state is active Reset Source: mod_g_rst_n 0 The synchronization mechanism is enabled 1 The synchronization mechanism is disabled
3	READ_MODE	W	0h	Select posted/non-posted mode for read operation. This bit is not used when configured in posted mode Reset Source: mod_g_rst_n 0 when the module is configurated in non-posted mode the read operation is executed as posted read 1 when the module is configured in non-posted mode the read operation is executed as read non-posted
2	POSTED	R/W	X	Reset value of POSTED depends on hardware integration module at design time. Software must read POSTED field to get the hardwar module configuration Reset Source: mod_g_rst_n 0 Posted mode inactive: will delay the command accept output signal 1 Posted mode active
1	SFT	R/W	0h	This bit reset all the functional part of teh module Reset Source: mod_g_rst_n 0 Software reset is disabled 1 Software reset is enabled
0	RESERVED	NONE	0h	Reserved

14.9.5.3.2.17 DMTIMER1MS_TCAR2 Register

1 DMTIMER1MS_TCAR2 Register (Offset = 58h) [reset = 0h]

This register holds the value of the second counter register capture

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Table 14-25373. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0058h
MCU_TIMER1	0481 0058h
MCU_TIMER2	0482 0058h
MCU_TIMER3	0483 0058h
TIMER0	0240 0058h
TIMER1	0241 0058h
TIMER2	0242 0058h
TIMER3	0243 0058h
TIMER4	0244 0058h
TIMER5	0245 0058h
TIMER6	0246 0058h
TIMER7	0247 0058h
TIMER8	0248 0058h
TIMER9	0249 0058h
TIMER10	024A 0058h
TIMER11	024B 0058h

Figure 14-8370. DMTIMER1MS_TCAR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CAPTURE_VALUE2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CAPTURE_VALUE2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CAPTURE_VALUE2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAPTURE_VALUE2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25375. DMTIMER1MS_TCAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPTURE_VALUE2	R	0h	The value of second captured counter register Reset Source: mod_g_rst_n

14.9.5.3.2.18 DMTIMER1MS_TPIR Register

1 DMTIMER1MS_TPIR Register (Offset = 5Ch) [reset = 0h]

This register is used for 1ms tick generation. The TPIR register holds the value of the positive increment. The value of this register is added with the value of the TCVR to define whether next value loaded in TCRR will be the sub-period value or the over-period value

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Table 14-25376. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 005Ch
MCU_TIMER1	0481 005Ch
MCU_TIMER2	0482 005Ch
MCU_TIMER3	0483 005Ch
TIMER0	0240 005Ch
TIMER1	0241 005Ch
TIMER2	0242 005Ch
TIMER3	0243 005Ch
TIMER4	0244 005Ch
TIMER5	0245 005Ch
TIMER6	0246 005Ch
TIMER7	0247 005Ch
TIMER8	0248 005Ch
TIMER9	0249 005Ch
TIMER10	024A 005Ch
TIMER11	024B 005Ch

Figure 14-8371. DMTIMER1MS_TPIR Name Register

31	30	29	28	27	26	25	24
POSITIVE_INC_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
POSITIVE_INC_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
POSITIVE_INC_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
POSITIVE_INC_VALUE							
R/W							
0h							

Table 14-25378. DMTIMER1MS_TPIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POSITIVE_INC_VALUE	R/W	0h	The value of the positive increment Reset Source: mod_g_rst_n

14.9.5.3.2.19 DMTIMER1MS_TNIR Register

1 DMTIMER1MS_TNIR Register (Offset = 60h) [reset = 0h]

This register is used for 1ms tick generation. The TNIR register holds the value of the negative increment. The value of this register is added with the value of the TCVR to define whether next value loaded in TCRR will be the sub-period value or the over-period value

Return to Summary Table

Table 14-25379. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0060h
MCU_TIMER1	0481 0060h
MCU_TIMER2	0482 0060h
MCU_TIMER3	0483 0060h
TIMER0	0240 0060h
TIMER1	0241 0060h
TIMER2	0242 0060h
TIMER3	0243 0060h
TIMER4	0244 0060h
TIMER5	0245 0060h
TIMER6	0246 0060h
TIMER7	0247 0060h
TIMER8	0248 0060h
TIMER9	0249 0060h
TIMER10	024A 0060h
TIMER11	024B 0060h

Figure 14-8372. DMTIMER1MS_TNIR Name Register

31	30	29	28	27	26	25	24
NEGATIVE_INC_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
NEGATIVE_INC_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
NEGATIVE_INC_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
NEGATIVE_INC_VALUE							
R/W							
0h							

Table 14-25381. DMTIMER1MS_TNIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NEGATIVE_INC_VALUE	R/W	0h	The value of the negative increment Reset Source: mod_g_rst_n

14.9.5.3.2.20 DMTIMER1MS_TCVR Register

1 DMTIMER1MS_TCVR Register (Offset = 64h) [reset = 0h]

This register is used for 1ms tick generation. The TCVR register defines whether next value loaded in TCRR will be the sub-period value or the over-period value

Return to Summary Table

Table 14-25382. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0064h
MCU_TIMER1	0481 0064h
MCU_TIMER2	0482 0064h
MCU_TIMER3	0483 0064h
TIMER0	0240 0064h
TIMER1	0241 0064h
TIMER2	0242 0064h
TIMER3	0243 0064h
TIMER4	0244 0064h
TIMER5	0245 0064h
TIMER6	0246 0064h
TIMER7	0247 0064h
TIMER8	0248 0064h
TIMER9	0249 0064h
TIMER10	024A 0064h
TIMER11	024B 0064h

Figure 14-8373. DMTIMER1MS_TCVR Name Register

31	30	29	28	27	26	25	24
COUNTER_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTER_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTER_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTER_VALUE							
R/W							
0h							

Table 14-25384. DMTIMER1MS_TCVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTER_VALUE	R/W	0h	The value of CVR counter Reset Source: mod_g_rst_n

14.9.5.3.2.21 DMTIMER1MS_TOCR Register

1 DMTIMER1MS_TOCR Register (Offset = 68h) [reset = 0h]

This register is used to mask the tick interrupt for a selected number of ticks

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Table 14-25385. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 0068h
MCU_TIMER1	0481 0068h
MCU_TIMER2	0482 0068h
MCU_TIMER3	0483 0068h
TIMER0	0240 0068h
TIMER1	0241 0068h
TIMER2	0242 0068h
TIMER3	0243 0068h
TIMER4	0244 0068h
TIMER5	0245 0068h
TIMER6	0246 0068h
TIMER7	0247 0068h
TIMER8	0248 0068h
TIMER9	0249 0068h
TIMER10	024A 0068h
TIMER11	024B 0068h

Figure 14-8374. DMTIMER1MS_TOCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OVF_COUNTER_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
OVF_COUNTER_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
OVF_COUNTER_VALUE							
R/W							
0h							

Table 14-25387. DMTIMER1MS_TOCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

Table 14-25387. DMTIMER1MS_TOCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	OVF_COUNTER_VALUE	R/W	0h	The number of overflow events Reset Source: mod_g_rst_n

14.9.5.3.2.22 DMTIMER1MS_TOWR Register

1 DMTIMER1MS_TOWR Register (Offset = 6Ch) [reset = 0h]

This register holds the number of masked overflow interrupts

Return to Summary Table

Table 14-25388. Instance Table

Instance Name	Physical Address
MCU_TIMER0	0480 006Ch
MCU_TIMER1	0481 006Ch
MCU_TIMER2	0482 006Ch
MCU_TIMER3	0483 006Ch
TIMER0	0240 006Ch
TIMER1	0241 006Ch
TIMER2	0242 006Ch
TIMER3	0243 006Ch
TIMER4	0244 006Ch
TIMER5	0245 006Ch
TIMER6	0246 006Ch
TIMER7	0247 006Ch
TIMER8	0248 006Ch
TIMER9	0249 006Ch
TIMER10	024A 006Ch
TIMER11	024B 006Ch

Figure 14-8375. DMTIMER1MS_TOWR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OVF_WRAPPING_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
OVF_WRAPPING_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
OVF_WRAPPING_VALUE							
R/W							
0h							

Table 14-25390. DMTIMER1MS_TOWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

Table 14-25390. DMTIMER1MS_TOWR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	OVF_WRAPPING_VALUE	R/W	0h	The number of masked interrupts Reset Source: mod_g_rst_n

14.9.6 Internal Diagnostics Modules Registers

14.9.6.1 DCC

DCC

Table 14-25391. DCC2 Registers, Base Address=0080 4000h, Length=64

Offset	Length	Register Name	DCC1 Physical Address
0h	32	DCC2_DCCGCTRL	0080 4000h
4h	32	DCC2_DCCREV	0080 4004h
8h	32	DCC2_DCCCNTSEED0	0080 4008h
Ch	32	DCC2_DCCVALIDSEED0	0080 400Ch
10h	32	DCC2_DCCCNTSEED1	0080 4010h
14h	32	DCC2_DCCSTATUS	0080 4014h
18h	32	DCC2_DCCCNT0	0080 4018h
1Ch	32	DCC2_DCCVALID0	0080 401Ch
20h	32	DCC2_DCCCNT1	0080 4020h
24h	32	DCC2_DCCCLKSRC1	0080 4024h
28h	32	DCC2_DCCCLKSRC0	0080 4028h
2Ch	32	DCC2_DCCGCTRL2	0080 402Ch
30h	32	DCC2_DCCSTATUS2	0080 4030h
34h	32	DCC2_DCCERRCNT	0080 4034h

14.9.6.1.1 DCC2_DCCGCTRL Register

1 DCC2_DCCGCTRL Register (Offset = 0h) [reset = 5555h]

Starts / stops the counters. Clears the error signal.

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Table 14-25392. Instance Table

Instance Name	Physical Address
DCC1	**0080 4000h**

Figure 14-8376. DCC2_DCCGCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">DONEENA</td><td colspan="4">SINGLESHOT</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">5h</td><td colspan="4">5h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ERRENA</td><td colspan="4">DCCENA</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">5h</td><td colspan="4">5h</td></tr>
</table>

Table 14-25394. DCC2_DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	DONEENA	R/W	5h	The DONEENA bit enables/disables the done interrupt signal, but has no effect on the done status flag in DCCSTAT register. User, privilege, and debug mode (read): 0101 = the done signal is disabled others = the done signal is enabled Privilege and debug mode (write): 0101 = disable done signal generation others = enable done signal generation
11:8	SINGLESHOT	R/W	5h	The SINGLESHOT bit enables/disables repetitive operation of the DCC. User, privilege, and debug mode (read): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error) Privilege and debug mode (write): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error)

Table 14-25394. DCC2_DCCGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ERRENA	R/W	5h	The ERRENA bit enables/disables the error signal. User, privilege, and debug mode (read): 0101 = the error signal is disabled others = the error signal is enabled Privilege and debug mode (write): 0101 = disable error signal generation others = enable error signal generation
3:0	DCCENA	R/W	5h	The DCCENA bit starts and stops the operation of the dcc. User, privilege, and debug mode (read): 0101 = counters are stopped others = counters are running Privilege and debug mode (write): 0101 = stop counters and error-checking others = load the counters with their seed values and begin counting

14.9.6.1.2 DCC2_DCCREV Register

1 DCC2_DCCREV Register (Offset = 4h) [reset = 40010300h]

Specifies the module version.

Return to Summary Table

Table 14-25395. Instance Table

Instance Name	Physical Address
DCC1	**0080 4004h**

Figure 14-8377. DCC2_DCCREV Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		NONE		R			
1h		0h		1h			
23	22	21	20	19	18	17	16
FUNC							
R							
1h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
0h					3h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-25397. DCC2_DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	User, privilege, and debug mode (read): Returns 01. Privilege and debug mode (write): Writes have no effect.
29:28	RESERVED	NONE	0h	Reserved
27:16	FUNC	R	1h	Reflects software-compatability. If there is no level of software compatability, a unique func number is assigned; for compatible modules, the same number is maintained. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
15:11	RTL	R	0h	Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
10:8	MAJOR	R	3h	Represents major changes to the module (e.g. entirely new features are added/changed). The major revision number for this module. User, privilege, and debug mode (read): 0x2 Privilege and debug mode (write): Writes have no effect.
7:6	CUSTOM	R	0h	Indicates a special version of the module. May not be supported by standard software. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.

Table 14-25397. DCC2_DCCREV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	MINOR	R	0h	Represents minor changes to the module (e.g. enhancements to existing features). The minor revision number for this module. User, privilege, and debug mode (read): 0x4 Privilege and debug mode (write): Writes have no effect.

14.9.6.1.3 DCC2_DCCCNTSEED0 Register

1 DCC2_DCCCNTSEED0 Register (Offset = 8h) [reset = 0h]

Seed value for the counter attached to clock source 0

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Table 14-25398. Instance Table

Instance Name	Physical Address
DCC1	**0080 4008h**

Figure 14-8378. DCC2_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				COUNTSEED0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
COUNTSEED0							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEED0							
R/W							
0h							

Table 14-25400. DCC2_DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNTSEED0	R/W	0h	This field contains the seed value that gets loaded into counter 0 (clock source 0). User, privilege, and debug mode (read): Returns the current seed value for counter 0. Privilege and debug mode (write): Sets the current seed value for counter 0. NOTE: Operating the DCC with 0 in the COUNTSEED0 register will result in undefined operation.

14.9.6.1.4 DCC2_DCCVALIDSEED0 Register

1 DCC2_DCCVALIDSEED0 Register (Offset = Ch) [reset = 0h]

Seed value for the timeout counter attached to clock source 0.

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Table 14-25401. Instance Table

Instance Name	Physical Address
DCC1	**0080 400Ch**

Figure 14-8379. DCC2_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VALIDSEED0							
R/W							
0h							
7	6	5	4	3	2	1	0
VALIDSEED0							
R/W							
0h							

Table 14-25403. DCC2_DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VALIDSEED0	R/W	0h	This field contains the seed value that gets loaded into the valid duration counter for clock source 0. User, privilege, and debug mode (read): Returns the current seed value for VALID0. Privilege and debug mode (write): Sets the current seed value for VALID0. NOTE: Operating the DCC with 0 in the VALIDSEED0 register will result in undefined operation. VALID0 defines a window in which COUNT1 expires. This window is meant to be at least four cycles wide. Do not program a value less than 4 into the VALID0 register.

14.9.6.1.5 DCC2_DCCCNTSEED1 Register

1 DCC2_DCCCNTSEED1 Register (Offset = 10h) [reset = 0h]

Seed value for the counter attached to clock source 1.

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Table 14-25404. Instance Table

Instance Name	Physical Address
DCC1	**0080 4010h**

Figure 14-8380. DCC2_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				COUNTSEED1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNTSEED1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNTSEED1							
R/W							
0h							

Table 14-25406. DCC2_DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNTSEED1	R/W	0h	This field contains the seed value that gets loaded into counter 1 (clock source 1). User, privilege, and debug mode (read): Returns the current seed value for counter 1. Privilege and debug mode (write): Sets the current seed value for counter 1. NOTE: Operating the DCC with 0 in the COUNTSEED1 register will result in undefined operation.

14.9.6.1.6 DCC2_DCCSTATUS Register

1 DCC2_DCCSTATUS Register (Offset = 14h) [reset = 0h]

Specifies the status of the DCC Module.

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Table 14-25407. Instance Table

Instance Name	Physical Address
DCC1	**0080 4014h**

Figure 14-8381. DCC2_DCCSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>DONEFLG</td><td>ERRFLG</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-25409. DCC2_DCCSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DONEFLG	R/W1TC	0h	Indicates when single-shot mode is complete without error. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = single-shot mode is not done 1 = single-shot mode is done Privilege and debug mode (write): 0 = no effect 1 = clear the done flag
0	ERRFLG	R/W1TC	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = an error has not occurred 1 = an error has occurred Privilege and debug mode (write): 0 = no effect 1 = clear the error flag

14.9.6.1.7 DCC2_DCCCNT0 Register

1 DCC2_DCCCNT0 Register (Offset = 18h) [reset = 0h]

Value of the counter attached to clock source 0.

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Table 14-25410. Instance Table

Instance Name	Physical Address
DCC1	**0080 4018h**

Figure 14-8382. DCC2_DCCCNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				COUNT0			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
COUNT0							
R							
0h							
7	6	5	4	3	2	1	0
COUNT0							
R							
0h							

Table 14-25412. DCC2_DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNT0	R	0h	This field contains the current value of counter 0. User, privilege, and debug mode (read): Returns the current value for counter 0. Privilege and debug mode (write): Writes have no effect. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.9.6.1.8 DCC2_DCCVALID0 Register

1 DCC2_DCCVALID0 Register (Offset = 1Ch) [reset = 0h]

Value of the valid counter attached to clock source 0.

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Table 14-25413. Instance Table

Instance Name	Physical Address
DCC1	**0080 401Ch**

Figure 14-8383. DCC2_DCCVALID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VALID0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VALID0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25415. DCC2_DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VALID0	R	0h	This field contains the current value of valid counter 0. User, privilege, and debug mode (read): Returns the current value for valid counter 0. Privilege and debug mode (write): writes have no effect. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.9.6.1.9 DCC2_DCCCNT1 Register

1 DCC2_DCCCNT1 Register (Offset = 20h) [reset = 0h]

Value of the counter attached to clock source 1.

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Table 14-25416. Instance Table

Instance Name	Physical Address
DCC1	**0080 4020h**

Figure 14-8384. DCC2_DCCCNT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				COUNT1			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
COUNT1							
R							
0h							
7	6	5	4	3	2	1	0
COUNT1							
R							
0h							

Table 14-25418. DCC2_DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNT1	R	0h	This field contains the current value of counter 1. User, privilege, and debug mode (read): Returns the current value for counter 1. Privilege and debug mode (write): writes have no effect. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.9.6.1.10 DCC2_DCCCLKSRC1 Register

1 DCC2_DCCCLKSRC1 Register (Offset = 24h) [reset = 0h]

Selects the clock source for counter 1.

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Table 14-25419. Instance Table

Instance Name	Physical Address
DCC1	**0080 4024h**

Figure 14-8385. DCC2_DCCCLKSRC1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
KEY				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED			CLKSRC1				
NONE			R/W				
0h			0h				

Table 14-25421. DCC2_DCCCLKSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 1. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 1. others: Clock source selection is disabled. The secondary oscillator (clock source 1) is selected for counter 1.
11:5	RESERVED	NONE	0h	Reserved

Table 14-25421. DCC2_DCCCLKSRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	CLKSRC1	R/W	0h	This field specifies the clock source for counter 1, when the KEY field enables this feature. User, privilege, and debug mode (read): Returns the current value of CLKSRC. Privilege and debug mode (write): Sets the value of CLKSRC. 0000 Clk source 0 is selected for COUNT1 0001 Clk source 1 is selected for COUNT1 0010 Clk source 2 is selected for COUNT1 0011 Clk source 3 is selected for COUNT1 0100 Clk source 4 is selected for COUNT1 0101 Clk source 5 is selected for COUNT1 0110 Clk source 6 is selected for COUNT1 0111 Clk source 7 is selected for COUNT1 1000-1111 VCLK is selected for COUNT1

14.9.6.1.11 DCC2_DCCCLKSRC0 Register

1 DCC2_DCCCLKSRC0 Register (Offset = 28h) [reset = 0h]

Selects the clock source for counter 0.

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Table 14-25422. Instance Table

Instance Name	Physical Address
DCC1	**0080 4028h**

Figure 14-8386. DCC2_DCCCLKSRC0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY				RESERVED			
R/W				NONE			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLKSRC0			
NONE				R/W			
0h				0h			

Table 14-25424. DCC2_DCCCLKSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 0. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 0. others: Clock source selection is disabled. The external oscillator (XTAL) is selected for counter 0.
11:4	RESERVED	NONE	0h	Reserved

Table 14-25424. DCC2_DCCCLKSRC0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CLKSRC0	R/W	0h	This field specifies the clock source for counter 0. User, privilege, and debug mode (read): Returns the current value of CLKSRC0. Privilege and debug mode (write): Sets the value of CLKSRC0. NOTE: DCC does not generate an error when the clock source is VCLK and VCLK is not present. Note: newer versions of DCC only provide one encoding for VCLK selection (MS encodings are tied off) 0000 Clock0[0] is selected as source for COUNT0 0001 Clock0[1] is selected as source for COUNT0 0010 Clock0[2] is selected as source for COUNT0 Other Values VCLK is selected as source for COUNT0

14.9.6.1.12 DCC2_DCCGCTRL2 Register

1 DCC2_DCCGCTRL2 Register (Offset = 2Ch) [reset = 555h]

Allows configuring different modes of operation for DCC.

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Table 14-25425. Instance Table

Instance Name	Physical Address
DCC1	**0080 402Ch**

Figure 14-8387. DCC2_DCCGCTRL2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FIFO_NONERR			
NONE				R/W			
0h				5h			
7	6	5	4	3	2	1	0
FIFO_READ				CONT_ON_ERR			
R/W				R/W			
5h				5h			

Table 14-25427. DCC2_DCCGCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	FIFO_NONERR	R/W	5h	Enables/disables FIFO writes without the error event on completion of comparison window. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter values are captured to non-full FIFO only upon Error event. Others: Write counter values to non-full FIFO upon completion of comparison window regardless of error or not.
7:4	FIFO_READ	R/W	5h	Enables the counter read registers reflect FIFO output instead of the live counter value. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter value is read directly. Others: Counters FIFO output is read.

Table 14-25427. DCC2_DCCGCTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONT_ON_ERR	R/W	5h	Continues to next window of comparison despite the error condition. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Enable values: 0101: Comparison and counter reload is stopped from advancing if error is detected. Others: Counters get reloaded with seed and continue counting despite the error condition.

14.9.6.1.13 DCC2_DCCSTATUS2 Register

1 DCC2_DCCSTATUS2 Register (Offset = 30h) [reset = 7h]

Specifies the status of the DCC FIFOs.

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Table 14-25428. Instance Table

Instance Name	Physical Address
DCC1	**0080 4030h**

Figure 14-8388. DCC2_DCCSTATUS2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		COUNT1_FIFO_FULL	VALID0_FIFO_FULL	COUNT0_FIFO_FULL	COUNT1_FIFO_EMPTY	VALID0_FIFO_EMPTY	COUNT0_FIFO_EMPTY
NONE		R	R	R	R	R	R
0h		0h	0h	0h	1h	1h	1h

Table 14-25430. DCC2_DCCSTATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	COUNT1_FIFO_FULL	R	0h	Count1 FIFO Full. Indicates whether Count1 FIFO is full. User, privilege, and debug mode (read): 0: Count1 FIFO is not full 1: Count1 FIFO is full. Privilege and debug mode (write): Writes have no effect.
4	VALID0_FIFO_FULL	R	0h	Valid0 FIFO Full. Indicates whether Valid0 FIFO is full. User, privilege, and debug mode (read): 0: Valid0 FIFO is not full 1: Valid0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
3	COUNT0_FIFO_FULL	R	0h	Count0 FIFO Full. Indicates whether Count0 FIFO is full. User, privilege, and debug mode (read): 0: Count0 FIFO is not full 1: Count0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
2	COUNT1_FIFO_EMPTY	R	1h	Count1 FIFO Empty. Indicates whether Count1 FIFO is empty. User, privilege, and debug mode (read): 0: Count1 FIFO is not empty 1: Count1 FIFO is empty. Privilege and debug mode (write): Writes have no effect.

Table 14-25430. DCC2_DCCSTATUS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VALID0_FIFO_EMPTY	R	1h	Valid0 FIFO Empty. Indicates whether Valid0 FIFO is empty. User, privilege, and debug mode (read): 0: Valid0 FIFO is not empty 1: Valid0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
0	COUNT0_FIFO_EMPTY	R	1h	Count0 FIFO Empty. Indicates whether Count0 FIFO is empty. User, privilege, and debug mode (read): 0: Count0 FIFO is not empty 1: Count0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.

14.9.6.1.14 DCC2_DCCERRCNT Register

1 DCC2_DCCERRCNT Register (Offset = 34h) [reset = 0h]

Counts number of errors since last clear.

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Table 14-25431. Instance Table

Instance Name	Physical Address
DCC1	**0080 4034h**

Figure 14-8389. DCC2_DCCERRCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						ERRCNT	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERRCNT							
R/W							
0h							

Table 14-25433. DCC2_DCCERRCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	ERRCNT	R/W	0h	Counts the number of errors after the last write to this register or reset. If reached terminal count the count freezes. User needs to clear it.

14.9.6.2 ESM Registers

Table 14-17046 lists the memory-mapped registers for the ESM. All register offset addresses not listed in Table 14-17046 should be considered as reserved locations and the register contents should not be modified.

Table 14-25434. ESM Instances

Instance	Base Address
ESM0_CFG	0042 0000h
MCU_ESM0_CFG	0410 0000h

Table 14-25435. ESM Registers

Offset	Acronym	Register Name	ESM0_CFG Physical Address	MCU_ESM0_CFG Physical Address
0h	ESM_PID	Revision Register	0042 0000h	0410 0000h
4h	ESM_INFO	Info Register	0042 0004h	0410 0004h
8h	ESM_EN	Global Enable Register	0042 0008h	0410 0008h
Ch	ESM_SFT_RST	Global Soft Reset Register	0042 000Ch	0410 000Ch
10h	ESM_ERR_RAW	Config Error Raw Status/Set Register	0042 0010h	0410 0010h
14h	ESM_ERR_STS	Config Error Interrupt Enable Status/Clear Register	0042 0014h	0410 0014h
18h	ESM_ERR_EN_SET	Config Error Interrupt Enable Set Register	0042 0018h	0410 0018h
1Ch	ESM_ERR_EN_CLR	Config Error Interrupt Enabled Clear Register	0042 001Ch	0410 001Ch
20h	ESM_LOW_PRI	Low Priority Prioritized Register	0042 0020h	0410 0020h
24h	ESM_HI_PRI	High Priority Prioritized Register	0042 0024h	0410 0024h
28h	ESM_LOW	Low Priority Interrupt Status Register	0042 0028h	0410 0028h
2Ch	ESM_HI	High Priority Interrupt Status Register	0042 002Ch	0410 002Ch
30h	ESM_EOI	ESM_EOI Interrupt Register	0042 0030h	0410 0030h
40h	ESM_PIN_CTRL	Error Pin Control Register	0042 0040h	0410 0040h
44h	ESM_PIN_STS	Error Pin Status Register	0042 0044h	0410 0044h
48h	ESM_PIN_CNTR	Error Pin Counter Value Register	0042 0048h	0410 0048h
4Ch	ESM_PIN_CNTR_PRE	Error Pin Counter Value Pre-Load Register	0042 004Ch	0410 004Ch
50h	ESM_PWMH_PIN_CNTR	Error Pin PWM High Counter Value Register	0042 0050h	0410 0050h
54h	ESM_PWMH_PIN_CNTR_PRE	Error Pin PWM High Counter Pre-Load Register	0042 0054h	0410 0054h
58h	ESM_PWML_PIN_CNTR	Error Pin PWM Low Counter Value Register	0042 0058h	0410 0058h
5Ch	ESM_PWML_PIN_CNTR_PRE	Error Pin PWM Low Counter Pre-Load Register	0042 005Ch	0410 005Ch
400h + formula	ESM_RAW_j	Config Error Raw Status/Set Register	0042 0400h + formula	0410 0400h + formula
404h + formula	ESM_STS_j	Level Error Interrupt Enable Status/Clear Register	0042 0404h + formula	0410 0404h + formula
408h + formula	ESM_INTR_EN_SET_j	Level Error Interrupt Enable Set Register	0042 0408h + formula	0410 0408h + formula
40Ch + formula	ESM_INTR_EN_CLR_j	Level Error Interrupt Enabled Clear Register	0042 040Ch + formula	0410 040Ch + formula
410h + formula	ESM_INT_PRIO_j	Level Error Interrupt Enabled Clear Register	0042 0410h + formula	0410 0410h + formula
414h + formula	ESM_PIN_EN_SET_j	Level Error Interrupt Enabled Clear Register	0042 0414h + formula	0410 0414h + formula
418h + formula	ESM_PIN_EN_CLR_j	Level Error Interrupt Enabled Clear Register	0042 0418h + formula	0410 0418h + formula

1 ESM_PID Register (Offset = 0h) [reset = X]

ESM_PID is shown in Figure 14-8390 and described in Table 14-17048.

Return to Summary Table.

The Revision Register contains the major and minor revisions for the module.

Table 14-25436. ESM_PID Instances

Instance	Physical Address
ESM0_CFG	0042 0000h
MCU_ESM0_CFG	0410 0000h

Figure 14-8390. ESM_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-2h		R-FE0h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-9h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -*n* = value after reset

Table 14-25438. ESM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	ESM_PID register scheme Always reads as 1h. Writes have no affect.
29-28	BU	R	2h	Business Unit: 2h = Processors
27-16	FUNC	R	FE0h	Module ID. Always read as the assigned functional ID. Writes have no affect.
15-11	RTL	R	9h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom. Special version.
5-0	MINOR	R	0h	Minor revision

2 ESM_INFO Register (Offset = 4h) [reset = X]

ESM_INFO is shown in Figure 14-8391 and described in Table 14-17050.

Return to Summary Table.

The Info Register gives the configuration information of this ESM.

Table 14-25439. ESM_INFO Instances

Instance	Physical Address
ESM0_CFG	0042 0004h
MCU_ESM0_CFG	0410 0004h

Figure 14-8391. ESM_INFO Register

31	30	29	28	27	26	25	24
LAST_RESET	RESERVED						
R-0h	R-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PULSE_GROUPS							
R-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GROUPS							
R-X							

LEGEND: R = Read Only; -*n* = value after reset

Table 14-25441. ESM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	R	0h	This bit indicates whether the last reset was a Warm or Power-On Rest 0h = Last reset was a Power On Reset 1h = Last reset was a Warm Reset
30-16	RESERVED	R	X	Always read as 0h. Writes have no affect.
15-8	PULSE_GROUPS	R	X (see description)	Indicates the number of event groups that are pulse (as opposed to level) driven. X = 1h for MCU_ESM0_CFG X = 1h for ESM0_CFG
7-0	GROUPS	R	X (see description)	Indicates the total number of groups that exist in the ESM. X = 3h for MCU_ESM0_CFG X = 6h for ESM0_CFG

3 ESM_EN Register (Offset = 8h) [reset = X]

ESM_EN is shown in Figure 14-8392 and described in Table 14-17052.

Return to Summary Table.

The Global Enable Register has the controller interrupt mask

Table 14-25442. ESM_EN Instances

Instance	Physical Address
ESM0_CFG	0042 0008h
MCU_ESM0_CFG	0410 0008h

Figure 14-8392. ESM_EN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												KEY			
R/W-X																												R/W-0h			

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14-25444. ESM_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	Always read as 0h. Writes have no affect.
3-0	KEY	R/W	0h	This field is the global mask for all interrupts. It is reset by the warm reset. The purpose is to leave all of the raw status and per-interrupt enable bits alone so that, after a warm reset, software may observe the state of the ESM before the warm reset and try to debug what may have caused the reset. 0h = All interrupts are disabled Fh = All interrupts are enabled Others = These are an invalid state. Software should never write these values. If these values are ever read, they indicate that an error has occurred. In this state, all interrupts are enabled (biased to false enable).

4 ESM_SFT_RST Register (Offset = Ch) [reset = X]

ESM_SFT_RST is shown in Figure 14-8393 and described in Table 14-17054.

Return to Summary Table.

The Global Soft Reset Register controls the global clear for raw status and enables

Table 14-25445. ESM_SFT_RST Instances

Instance	Physical Address
ESM0_CFG	0042 000Ch
MCU_ESM0_CFG	0410 000Ch

Figure 14-8393. ESM_SFT_RST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												KEY			
W-X																												W-0h			

LEGEND: W = Write Only; -*n* = value after reset

Table 14-25447. ESM_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	X	Always read as 0h. Writes have no affect.
3-0	KEY	W	0h	Global Soft Reset field. Writing to this field can cause all of the raw status and all enables to be cleared. This can be used to reset the ESM state after debugging because of a warm reset. 0h (R) = Always read as 0h Fh (W) = Clear all raw status and enable bits Others (W) = No effect

5 ESM_ERR_RAW Register (Offset = 10h) [reset = X]

ESM_ERR_RAW is shown in Figure 14-8394 and described in Table 14-17056.

Return to Summary Table.

Raw Status/Set Register for Configuration Errors

Table 14-25448. ESM_ERR_RAW Instances

Instance	Physical Address
ESM0_CFG	0042 0010h
MCU_ESM0_CFG	0410 0010h

Figure 14-8394. ESM_ERR_RAW Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">STS</td></tr>
<tr><td colspan="24">R/W-X</td><td colspan="8">R/W1S-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-25450. ESM_ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	Always read as 0h. Writes have no affect.
7-0	STS	R/W1S	0h	This is the raw status for errors in the configuration for Group N. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h. Bit 0 - Group 0 Bit 1 - Group 1 ... Bit 7 - Group 7 0h (R) = Inactive 1h (R) = Active/Pending 0h (W) = No effect 1h (W) = Set to Interrupt Raw Status **Note:** Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. The following bits are available (not reserved) for: Bit 2- Bit 0 for MCU_ESM0_CFG (3 groups) Bit 5 - Bit 0 for ESM0_CFG (6 groups)

6 ESM_ERR_STS Register (Offset = 14h) [reset = X]

ESM_ERR_STS is shown in Figure 14-8395 and described in Table 14-17058.

Return to Summary Table.

Config Error Enable and Clear Register

Table 14-25451. ESM_ERR_STS Instances

Instance	Physical Address
ESM0_CFG	0042 0014h
MCU_ESM0_CFG	0410 0014h

Figure 14-8395. ESM_ERR_STS Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">MSK</td></tr>
<tr><td colspan="24">R/W-X</td><td colspan="8">R/W1C-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-25453. ESM_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	Always read as 0h. Writes have no affect.
7-0	MSK	R/W1C	0h	This is the masked status for errors in the configuration for Group N. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Bit 0 - Group 0 Bit 1 - Group 1 ... Bit 7 - Group 7 0h (R) = Inactive or Disabled 1h (R) = Active/Pending and Enabled 0h (W) = No effect 1h (W) = Clear Interrupt Raw Status **Note:** Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. The following bits are available (not reserved) for: Bit 2- Bit 0 for MCU_ESM0_CFG (3 groups) Bit 5 - Bit 0 for ESM0_CFG (6 groups)

7 ESM_ERR_EN_SET Register (Offset = 18h) [reset = X]

ESM_ERR_EN_SET is shown in Figure 14-8396 and described in Table 14-17060.

Return to Summary Table.

Config Error Enable Set Register

Table 14-25454. ESM_ERR_EN_SET Instances

Instance	Physical Address
ESM0_CFG	0042 0018h
MCU_ESM0_CFG	0410 0018h

Figure 14-8396. ESM_ERR_EN_SET Register

31-8	7-0
RESERVED	MSK
R/W-X	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-25456. ESM_ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	Always read as 0h. Writes have no affect.
7-0	MSK	R/W1S	0h	This is the mask enable for errors in the configuration for Group N. If the corresponding bit and the ESM_EN are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Bit 0 - Group 0 Bit 1 - Group 1 ... Bit 7 - Group 7 0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Set Enable **Note:** Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. The following bits are available (not reserved) for: Bit 2- Bit 0 for MCU_ESM0_CFG (3 groups) Bit 5 - Bit 0 for ESM0_CFG (6 groups)

8 ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = X]

ESM_ERR_EN_CLR is shown in Figure 14-8397 and described in Table 14-17062.

Return to Summary Table.

Config Error Interrupt Enabled Clear register

Table 14-25457. ESM_ERR_EN_CLR Instances

Instance	Physical Address
ESM0_CFG	0042 001Ch
MCU_ESM0_CFG	0410 001Ch

Figure 14-8397. ESM_ERR_EN_CLR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">MSK</td></tr>
<tr><td colspan="24">R/W-X</td><td colspan="8">R/W1C-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-25459. ESM_ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	Always read as 0h. Writes have no affect.
7-0	MSK	R/W1C	0h	This is the mask clear for errors in the configuration for Group N. If the corresponding bit and the ESM_EN are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Bit 0 - Group 0 Bit 1 - Group 1 ... Bit 7 - Group 7 0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Clear Enable **Note:** Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. The following bits are available (not reserved) for: Bit 2- Bit 0 for MCU_ESM0_CFG (3 groups) Bit 5 - Bit 0 for ESM0_CFG (6 groups)

9 ESM_LOW_PRI Register (Offset = 20h) [reset = FFFFFFFFh]

ESM_LOW_PRI is shown in Figure 14-8398 and described in Table 14-17064.

Return to Summary Table.

Shows which is the highest priority outstanding low priority interrupt

Table 14-25460. ESM_LOW_PRI Instances

Instance	Physical Address
ESM0_CFG	0042 0020h
MCU_ESM0_CFG	0410 0020h

Figure 14-8398. ESM_LOW_PRI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLS																LVL															
R-FFFFh																R-FFFFh															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-25462. ESM_LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PLS	R	FFFFh	Indicates what the highest priority low priority interrupt caused by a pulse number is. The lowest event has the highest priority. I.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for high priority while Global Events 2, 3, and 4 are configured for low priority, then the value of this field will be 0x2. A value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.
15-0	LVL	R	FFFFh	Indicates what the highest priority low priority interrupt caused by a level number is. The lowest event has the highest priority. I.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for High Priority while Global Events 2, 3, and 4 are configured for low priority, then the value of this field will be 0x2. A value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.

10 ESM_HI_PRI Register (Offset = 24h) [reset = FFFFFFFFh]

ESM_HI_PRI is shown in Figure 14-8399 and described in Table 14-17066.

Return to Summary Table.

Shows which is the highest priority outstanding high priority interrupt

Table 14-25463. ESM_HI_PRI Instances

Instance	Physical Address
ESM0_CFG	0042 0024h
MCU_ESM0_CFG	0410 0024h

Figure 14-8399. ESM_HI_PRI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLS																LVL															
R-FFFFh																R-FFFFh															

LEGEND: R = Read Only; -*n* = value after reset

Table 14-25465. ESM_HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PLS	R	FFFFh	Indicates what the highest priority high priority interrupt caused by a pulse number is. The lowest event has the highest priority. I.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for high priority while Global Events 2, 3, and 4 are configured for low priority, then the value of this field will be 0x0. A value of all ones (0xFFFF) indicates that there are no high priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.
15-0	LVL	R	FFFFh	Indicates what the highest priority low priority interrupt caused by a level number is. The lowest event has the highest priority. I.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for high priority while Global Events 2, 3, and 4 are configured for low priority, then the value of this field will be 0x0. A value of all ones (0xFFFF) indicates that there are no high priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.

11 ESM_LOW Register (Offset = 28h) [reset = 0h]

ESM_LOW is shown in Figure 14-8400 and described in Table 14-17068.

Return to Summary Table.

Shows which groups have outstanding low priority interrupts

Table 14-25466. ESM_LOW Instances

Instance	Physical Address
ESM0_CFG	0042 0028h
MCU_ESM0_CFG	0410 0028h

Figure 14-8400. ESM_LOW Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">STS</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-25468. ESM_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R	0h	Indicates which Event Groups have one or more low priority interrupts pending. This register is bit oriented where bit 0 is for Event Group 0, bit 1 is for Event Group 1, etc… (bit N is for Event Group N). 0h (R) = Inactive 1h (R) = Active/Pending

12 ESM_HI Register (Offset = 2Ch) [reset = 0h]

ESM_HI is shown in Figure 14-8401 and described in Table 14-17070.

Return to Summary Table.

Shows which groups have outstanding high priority interrupts

Table 14-25469. ESM_HI Instances

Instance	Physical Address
ESM0_CFG	0042 002Ch
MCU_ESM0_CFG	0410 002Ch

Figure 14-8401. ESM_HI Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">STS</td></tr>
<tr><td colspan="32">R-0h</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-25471. ESM_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R	0h	Indicates which Event Groups have one or more high priority interrupts pending. This register is bit oriented where bit 0 is for Event Group 0, bit 1 is for Event Group 1, etc… (bit N is for Event Group N). 0h (R) = Inactive 1h (R) = Active/Pending

13 ESM_EOI Register (Offset = 30h) [reset = X]

ESM_EOI is shown in Figure 14-8402 and described in Table 14-17072.

Return to Summary Table.

End of Interrupt Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-25472. ESM_EOI Instances

Instance	Physical Address
ESM0_CFG	0042 0030h
MCU_ESM0_CFG	0410 0030h

Figure 14-8402. ESM_EOI Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="21">RESERVED</td><td colspan="11">KEY</td></tr>
<tr><td colspan="21">W-X</td><td colspan="11">W-0h</td></tr>
</table>

LEGEND: W = Write Only; -*n* = value after reset

Table 14-25474. ESM_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	W	X	Always read as 0h. Writes have no affect.
10-0	KEY	W	0h	This is the interrupt being serviced. Writing the corresponding vector to this field will cause a re-evaluation of interrupts. If, when the vector is written, there are still pending interrupts, a new pulse will be generated. Reads always return 0. 0h (W) = Configuration error interrupt 1h (W) = Low priority error interrupt 2h (W) = High priority error interrupt 3h – 2047h (W) = Reserved (writes have no effect)

14 ESM_PIN_CTRL Register (Offset = 40h) [reset = 0h]

ESM_PIN_CTRL is shown in Figure 14-8403 and described in Table 14-17074.

Return to Summary Table.

This register controls the SAFETY_ERRORn pin output

Table 14-25475. ESM_PIN_CTRL Instances

Instance	Physical Address
ESM0_CFG	0042 0040h
MCU_ESM0_CFG	0410 0040h

Figure 14-8403. ESM_PIN_CTRL Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="4">PWM_EN</td><td colspan="4">KEY</td></tr>
<tr><td colspan="24">R-0h</td><td colspan="4">R/W-0h</td><td colspan="4">R/W-0h</td></tr>
</table>

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-25477. ESM_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Always read as 0h. Writes have no affect.
7-4	PWM_EN	R/W	0h	PWM mode enable. This field should only be modified when the ESM is disabled, from the ESM_EN register. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0h = Error output pin is a level (default). 1h = Error output pin is a PWM signal. All Other Values = These are an invalid state. Software should never write these values. If these values are ever read, they indicate that an error has occurred. In this state, level mode is used.
3-0	KEY	R/W	0h	Pin control key. This field controls behavior of the error pin. Note, during reset the field is 0h, but the error pin is asserted (active low). Immediately after reset, the error pin de-asserts. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. A global soft reset will also CLEAR all pending faults. 0h = Normal Mode: Error pin will activate when an enabled Error Event occurs. 5h = CLEAR Event: generates a CLEAR event to the ESM state machine. Key will return to Normal Mode (0h) on the next cycle. Ah = Force Error Mode: Forces the error pin to active. To clear the error pin (return to the ESM_IDLE state) write this field back to Normal Mode (writing a CLEAR event will also work). Software may only write to Force Error Mode while in IDLE. Attempting Force Error while in another state will have no effect All Other Values = Normal Mode: Writing any of these values will have no effect. Reading any of these values indicate that one or more bits have experienced a single event upset and software should write the field back to 0h. The ESM will continue to operate in Normal Mode.

15 ESM_PIN_STS Register (Offset = 44h) [reset = X]

ESM_PIN_STS is shown in Figure 14-8404 and described in Table 14-17076.

Return to Summary Table.

This register reflects the status of the error_pin_n output

Table 14-25478. ESM_PIN_STS Instances

Instance	Physical Address
ESM0_CFG	0042 0044h
MCU_ESM0_CFG	0410 0044h

Figure 14-8404. ESM_PIN_STS Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">RESERVED</td></tr>
<tr><td colspan="16">R-X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="15">RESERVED</td><td>VAL</td></tr>
<tr><td colspan="15">R-X</td><td>R-X</td></tr>
</table>

LEGEND: R = Read Only; -*n* = value after reset

Table 14-25480. ESM_PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	Always read as 0h. Writes have no affect.
0	VAL	R	X (see description)	This field indicates the status of the error pin as looped back from the I/O. This field reflects the state of the ERR_I pin. Since the ERR_O pin is only affected by Power-On-Reset, then the value of this field may be 1h after the release of Warm Reset. 0h (R) = Asserted (pin is active, low) 1h (R) = De-Asserted (pin is inactive, high) **Note:** While in reset the error pin is actually active (asserted low), but goes inactive immediately after the de-assertion of Power-on-Reset. Hence, the value that will be read after Power-on-Reset is 1h, but may be 0h after a warm reset.

16 ESM_PIN_CNTR Register (Offset = 48h) [reset = X]

ESM_PIN_CNTR is shown in Figure 14-8405 and described in Table 14-17078.

Return to Summary Table.

This register shows the current value of the error pin counter

Table 14-25481. ESM_PIN_CNTR Instances

Instance	Physical Address
ESM0_CFG	0042 0048h
MCU_ESM0_CFG	0410 0048h

Figure 14-8405. ESM_PIN_CNTR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="24">COUNT</td></tr>
<tr><td colspan="8">R-X</td><td colspan="24">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-25483. ESM_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	Always read as 0h. Writes have no affect.
23-0	COUNT	R	0h	This field indicates the current value of the time interval counter. See ESM_PIN_CNTR_PRE register for a description. This register is reloaded to the counter_preload value on entry to the ESM_ERROR state from ESM_IDLE and counts down by one per clock cycle. Once the counter has reached 0, the minimum time interval has expired. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h.

17 ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = 0h]

ESM_PIN_CNTR_PRE is shown in Figure 14-8406 and described in Table 14-17080.

Return to Summary Table.

This register contains the value that is loaded in to the Error Counter

Table 14-25484. ESM_PIN_CNTR_PRE Instances

Instance	Physical Address
ESM0_CFG	0042 004Ch
MCU_ESM0_CFG	0410 004Ch

Figure 14-8406. ESM_PIN_CNTR_PRE Register

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RESERVED	COUNT
R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-25486. ESM_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Always read as 0h. Writes have no affect.
23-0	COUNT	R/W	0h	This is the value that will be pre-loaded in to the ESM_PIN_CNTR[23-0] COUNT bit field whenever the ESM enters the ESM_ERROR state from ESM_IDLE. The default value is determined based on the ESM clock frequency, so that there is a minimum low time of 100µs. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h.

18 ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = 0h]

ESM_PWMH_PIN_CNTR is shown in Figure 14-8407 and described in Table 14-17082.

Return to Summary Table.

This register contains the current value of the PWM High Time Interval Counter.

Table 14-25487. ESM_PWMH_PIN_CNTR Instances

Instance	Physical Address
ESM0_CFG	0042 0050h
MCU_ESM0_CFG	0410 0050h

Figure 14-8407. ESM_PWMH_PIN_CNTR Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td><td colspan="24">COUNT</td></tr>
<tr><td colspan="8">R-0h</td><td colspan="24">R-0h</td></tr>
</table>

LEGEND: R = Read Only; *-n* = value after reset

Table 14-25489. ESM_PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Always read as 0h. Writes have no affect.
23-0	COUNT	R	0h	This field indicates the current value of the PWM High Time Interval Counter. If ESM_PIN_CTRL[7-4] PWM_EN is set to PWM mode, then this register is enabled. This register is reloaded to the PWM high counter_preload value when the error output pin toggles high. It will decrement by 1 each cycle when the error output pin is high. Once the counter has reached 0, the error output pin will toggle low. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h.

19 ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = 0h]

ESM_PWMH_PIN_CNTR_PRE is shown in Figure 14-8408 and described in Table 14-17084.

Return to Summary Table.

This register contains the value that is loaded in to the Error Pin PWM High Counter Value Register.

Table 14-25490. ESM_PWMH_PIN_CNTR_PRE Instances

Instance	Physical Address
ESM0_CFG	0042 0054h
MCU_ESM0_CFG	0410 0054h

Figure 14-8408. ESM_PWMH_PIN_CNTR_PRE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R-0h								R/W-0h																							

LEGEND: R = Read Only; R/W = Read/Write; -*n* = value after reset

Table 14-25492. ESM_PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Always read as 0h. Writes have no affect.
23-0	COUNT	R/W	0h	This is the value that will be loaded in to the ESM_PWMH_PIN_CNTR[23-0] COUNT field whenever the error output pin toggles high. The default value is determined based on the external PMIC settings. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h.

20 ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = 0h]

ESM_PWML_PIN_CNTR is shown in Figure 14-8409 and described in Table 14-17086.

Return to Summary Table.

This register contains the current value of the PWM Low Time Interval Counter.

Table 14-25493. ESM_PWML_PIN_CNTR Instances

Instance	Physical Address
ESM0_CFG	0042 0058h
MCU_ESM0_CFG	0410 0058h

Figure 14-8409. ESM_PWML_PIN_CNTR Register

31-24	23-0
RESERVED	COUNT
R-0h	R-0h

LEGEND: R = Read Only; -*n* = value after reset

Table 14-25495. ESM_PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Always read as 0h. Writes have no affect.
23-0	COUNT	R	0h	This field indicates the current value of the PWM Low Time Interval Counter. If ESM_PIN_CTRL[7-4] PWM_EN is set to PWM mode, then this register is enabled. This register is reloaded to the PWM low counter_preload value when the error output pin toggles low. It will decrement by 1 each cycle when the error output pin is low. Once the counter has reached 0, the error output pin will toggle high. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h.

21 ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = 0h]

ESM_PWML_PIN_CNTR_PRE is shown in Figure 14-8410 and described in Table 14-17088.

Return to Summary Table.

This register contains the value that is loaded in to the Error Pin PWM Low Counter Value Register.

Table 14-25496. ESM_PWML_PIN_CNTR_PRE Instances

Instance	Physical Address
ESM0_CFG	0042 005Ch
MCU_ESM0_CFG	0410 005Ch

Figure 14-8410. ESM_PWML_PIN_CNTR_PRE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R-0h								R/W-0h																							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 14-25498. ESM_PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Always read as 0h. Writes have no affect.
23-0	COUNT	R/W	0h	This is the value that will be loaded in to the ESM_PWML_PIN_CNTR[23-0] COUNT field whenever the error output pin toggles low. The default value is determined based on the external PMIC settings. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h.

22 ESM_RAW_j Register (Offset = 400h + formula) [reset = 0h]

ESM_RAW_j is shown in Figure 14-8411 and described in Table 14-17090.

Return to Summary Table.

Raw Status/Set Register for Group A Errors

Offset = 400h + (j * 20h); where
j = 0h to 2h for MCU_ESM0_CFG
j = 0h to 5h for ESM0_CFG

Table 14-25499. ESM_RAW_j Instances

Instance	Physical Address
ESM0_CFG	0042 0400h + formula
MCU_ESM0_CFG	0410 0400h + formula

Figure 14-8411. ESM_RAW_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">STS</td></tr>
<tr><td colspan="32">R/W1S-0h</td></tr>
</table>

LEGEND: R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-25501. ESM_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STS	R/W1S	0h	This is the raw status of the events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc...) For Level events, the raw status is the event input synchronized to the ESM clock and stored in a multi-bit (for redundancy) internal register. For Pulse events, the raw status is multi-bit (for redundancy) internal register that is set when two of the three edge detection circuits on the redundant event capture a rising edge. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0h (R) = Inactive 1h (R) = Active/Pending 0h (W) = No effect 1h (W) = Set to Interrupt Raw Status

23 ESM_STS_j Register (Offset = 404h + formula) [reset = 0h]

ESM_STS_j is shown in Figure 14-8412 and described in Table 14-17092.

Return to Summary Table.

Error Enable and Clear Register

Offset = 404h + (j * 20h); where
j = 0h to 2h for MCU_ESM0_CFG
j = 0h to 5h for ESM0_CFG

Table 14-25502. ESM_STS_j Instances

Instance	Physical Address
ESM0_CFG	0042 0404h + formula
MCU_ESM0_CFG	0410 0404h + formula

Figure 14-8412. ESM_STS_j Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">MSK</td></tr>
<tr><td colspan="32">R/W1C-0h</td></tr>
</table>

LEGEND: R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 14-25504. ESM_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This is the masked status of the events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc…) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0h (R) = Inactive or Disabled 1h (R) = Active/Pending and Enabled 0h (W) = No effect 1h (W) = Clear Interrupt Raw Status

24 ESM_INTR_EN_SET_j Register (Offset = 408h + formula) [reset = 0h]

ESM_INTR_EN_SET_j is shown in Figure 14-8413 and described in Table 14-17094.

Return to Summary Table.

Level Error Enable Set Register

Offset = 408h + (j * 20h); where
j = 0h to 2h for MCU_ESM0_CFG
j = 0h to 5h for ESM0_CFG

Table 14-25505. ESM_INTR_EN_SET_j Instances

Instance	Physical Address
ESM0_CFG	0042 0408h + formula
MCU_ESM0_CFG	0410 0408h + formula

Figure 14-8413. ESM_INTR_EN_SET_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1S-0h																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 14-25507. ESM_INTR_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1S	0h	This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc…) If the corresponding bit and the global enable ESM_EN are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Set Enable

25 ESM_INTR_EN_CLR_j Register (Offset = 40Ch + formula) [reset = 0h]

ESM_INTR_EN_CLR_j is shown in Figure 14-8414 and described in Table 14-17096.

Return to Summary Table.

Level Error Interrupt Enabled Clear register

Offset = 40Ch + (j * 20h); where
j = 0h to 2h for MCU_ESM0_CFG
j = 0h to 5h for ESM0_CFG

Table 14-25508. ESM_INTR_EN_CLR_j Instances

Instance	Physical Address
ESM0_CFG	0042 040Ch + formula
MCU_ESM0_CFG	0410 040Ch + formula

Figure 14-8414. ESM_INTR_EN_CLR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-25510. ESM_INTR_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This field is used to disable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc…) If the corresponding bit and the global enable ESM_EN are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Clear Enable

26 ESM_INT_PRIO_j Register (Offset = 410h + formula) [reset = 0h]

ESM_INT_PRIO_j is shown in Figure 14-8415 and described in Table 14-17098.

Return to Summary Table.

Level Error Interrupt Enabled Clear register

Offset = 410h + (j * 20h); where
j = 0h to 2h for MCU_ESM0_CFG
j = 0h to 5h for ESM0_CFG

Table 14-25511. ESM_INT_PRIO_j Instances

Instance	Physical Address
ESM0_CFG	0042 0410h + formula
MCU_ESM0_CFG	0410 0410h + formula

Figure 14-8415. ESM_INT_PRIO_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14-25513. ESM_INT_PRIO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc…) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0h = Low priority interrupt (default) 1h = High priority interrupt

27 ESM_PIN_EN_SET_j Register (Offset = 414h + formula) [reset = 0h]

ESM_PIN_EN_SET_j is shown in Figure 14-8416 and described in Table 14-17100.

Return to Summary Table.

Level Error Interrupt Enabled Clear register

Offset = 414h + (j * 20h); where
j = 0h to 2h for MCU_ESM0_CFG
j = 0h to 5h for ESM0_CFG

Table 14-25514. ESM_PIN_EN_SET_j Instances

Instance	Physical Address
ESM0_CFG	0042 0414h + formula
MCU_ESM0_CFG	0410 0414h + formula

Figure 14-8416. ESM_PIN_EN_SET_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1S-0h																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 14-25516. ESM_PIN_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1S	0h	This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc…) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Set Enable. Corresponding event, when set, will count as a pending error event for the ESM state machine.

28 ESM_PIN_EN_CLR_j Register (Offset = 418h + formula) [reset = 0h]

ESM_PIN_EN_CLR_j is shown in Figure 14-8417 and described in Table 14-17102.

Return to Summary Table.

Level Error Interrupt Enabled Clear register

Offset = 418h + (j * 20h); where
j = 0h to 2h for MCU_ESM0_CFG
j = 0h to 5h for ESM0_CFG

Table 14-25517. ESM_PIN_EN_CLR_j Instances

Instance	Physical Address
ESM0_CFG	0042 0418h + formula
MCU_ESM0_CFG	0410 0418h + formula

Figure 14-8417. ESM_PIN_EN_CLR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 14-25519. ESM_PIN_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSK	R/W1C	0h	This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc…) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Clear Enable. Corresponding events will no longer count as pending error events for the ESM state machine

14.9.6.3 MCRC64

MCRC64

14.9.6.3.1 MCRC64 Summaries

MCRC64 Summaries

Table 14-25520. CRC Registers, Base Address=04D0 0000h, Length=4096

Offset	Length	Register Name	MCU_MCRC64_0 Physical Address
0h	32	CRC_CTRL0	04D0 0000h
8h	32	CRC_CTRL1	04D0 0008h
10h	32	CRC_CTRL2	04D0 0010h
18h	32	CRC_INTS	04D0 0018h
20h	32	CRC_INTR	04D0 0020h
28h	32	CRC_STATUS	04D0 0028h
30h	32	CRC_INT_OFFSET_REG	04D0 0030h
38h	32	CRC_BUSY	04D0 0038h
40h	32	CRC_PCOUNT_REG1	04D0 0040h
44h	32	CRC_SCOUNT_REG1	04D0 0044h
48h	32	CRC_CURSEC_REG1	04D0 0048h
4Ch	32	CRC_WDTOPLD1	04D0 004Ch
50h	32	CRC_BCTOPLD1	04D0 0050h
60h	32	CRC_PSA_SIGREGL1	04D0 0060h
64h	32	CRC_PSA_SIGREGH1	04D0 0064h
68h	32	CRC_REGL1	04D0 0068h
6Ch	32	CRC_REGH1	04D0 006Ch
70h	32	CRC_PSA_SECSIGREGL1	04D0 0070h
74h	32	CRC_PSA_SECSIGREGH1	04D0 0074h
78h	32	CRC_RAW_DATAREGL1	04D0 0078h
7Ch	32	CRC_RAW_DATAREGH1	04D0 007Ch
80h	32	CRC_PCOUNT_REG2	04D0 0080h
84h	32	CRC_SCOUNT_REG2	04D0 0084h
88h	32	CRC_CURSEC_REG2	04D0 0088h
8Ch	32	CRC_WDTOPLD2	04D0 008Ch
90h	32	CRC_BCTOPLD2	04D0 0090h
A0h	32	CRC_PSA_SIGREGL2	04D0 00A0h
A4h	32	CRC_PSA_SIGREGH2	04D0 00A4h
A8h	32	CRC_REGL2	04D0 00A8h
ACh	32	CRC_REGH2	04D0 00ACh
B0h	32	CRC_PSA_SECSIGREGL2	04D0 00B0h
B4h	32	CRC_PSA_SECSIGREGH2	04D0 00B4h
B8h	32	CRC_RAW_DATAREGL2	04D0 00B8h
BCh	32	CRC_RAW_DATAREGH2	04D0 00BCh
C0h	32	CRC_PCOUNT_REG3	04D0 00C0h
C4h	32	CRC_SCOUNT_REG3	04D0 00C4h
C8h	32	CRC_CURSEC_REG3	04D0 00C8h
CCh	32	CRC_WDTOPLD3	04D0 00CCh

Table 14-25520. CRC Registers, Base Address=04D0 0000h, Length=4096 (continued)

Offset	Length	Register Name	MCU_MCRC64_0 Physical Address
D0h	32	CRC_BCTOPLD3	04D0 00D0h
E0h	32	CRC_PSA_SIGREGL3	04D0 00E0h
E4h	32	CRC_PSA_SIGREGH3	04D0 00E4h
E8h	32	CRC_REGL3	04D0 00E8h
ECh	32	CRC_REGH3	04D0 00ECh
F0h	32	CRC_PSA_SECSIGREGL3	04D0 00F0h
F4h	32	CRC_PSA_SECSIGREGH3	04D0 00F4h
F8h	32	CRC_RAW_DATAREGL3	04D0 00F8h
FCh	32	CRC_RAW_DATAREGH3	04D0 00FCh
100h	32	CRC_PCOUNT_REG4	04D0 0100h
104h	32	CRC_SCOUNT_REG4	04D0 0104h
108h	32	CRC_CURSEC_REG4	04D0 0108h
10Ch	32	CRC_WDTOPLD4	04D0 010Ch
110h	32	CRC_BCTOPLD4	04D0 0110h
120h	32	CRC_PSA_SIGREGL4	04D0 0120h
124h	32	CRC_PSA_SIGREGH4	04D0 0124h
128h	32	CRC_REGL4	04D0 0128h
12Ch	32	CRC_REGH4	04D0 012Ch
130h	32	CRC_PSA_SECSIGREGL4	04D0 0130h
134h	32	CRC_PSA_SECSIGREGH4	04D0 0134h
138h	32	CRC_RAW_DATAREGL4	04D0 0138h
13Ch	32	CRC_RAW_DATAREGH4	04D0 013Ch
140h	32	CRC_MBUS_SEL	04D0 0140h
200h	32	CRC_I0_PSA_SIGREG1_CPY_J	04D0 0200h + formula
280h	32	CRC_I0_PSA_SIGREG2_CPY_J	04D0 0280h + formula
300h	32	CRC_I0_PSA_SIGREG3_CPY_J	04D0 0300h + formula
380h	32	CRC_I0_PSA_SIGREG4_CPY_J	04D0 0380h + formula

14.9.6.3.2 MCRC64 Registers

MCRC64 Registers

14.9.6.3.2.1 CRC_CTRL0 Register

1 CRC_CTRL0 Register (Offset = 0h) [reset = 0h]

CRC Global Control Register 0

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Table 14-25521. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0000h**

Figure 14-8418. CRC_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							CH4_PSA_SWRE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CH3_PSA_SWRE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CH2_PSA_SWRE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CH1_PSA_SWRE
NONE							R/W
0h							0h

Table 14-25523. CRC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CH4_PSA_SWRE	R/W	0h	Channel 4 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
23:17	RESERVED	NONE	0h	Reserved
16	CH3_PSA_SWRE	R/W	0h	Channel 3 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
15:9	RESERVED	NONE	0h	Reserved
8	CH2_PSA_SWRE	R/W	0h	Channel 2 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
7:1	RESERVED	NONE	0h	Reserved

Table 14-25523. CRC_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_PSA_SWRE	R/W	0h	Channel 1 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset

14.9.6.3.2.2 CRC_CTRL1 Register

1 CRC_CTRL1 Register (Offset = 8h) [reset = 0h]

CRC Global Control Register 1

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Table 14-25524. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0008h**

Figure 14-8419. CRC_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PWDN
NONE							R/W
0h							0h

Table 14-25526. CRC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PWDN	R/W	0h	Power Down. When set, MCRC moduleMCRC Module is put in power down mode. 0 = MCRC is not in power down mode. 1 = MCRC is in power down mode.

14.9.6.3.2.3 CRC_CTRL2 Register

1 CRC_CTRL2 Register (Offset = 10h) [reset = 0h]

Data capture mode is especially useful when it is used in conjunction when data trace (CH1_TRACEEN) for channel 1. The seed value can be planted in PSA Signature Register during data capture mode by writing a seed value into PSA Signature Register. Data trace enable bit is then set to snoop and compress any read transaction on Data buses. When trace enable bit is set, CH1_MODE is automatically reset to data capture mode. To change mode from one to another in the middle of an on-going mode user should take the following steps:

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Table 14-25527. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0010h**

Figure 14-8420. CRC_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESERVED						CH4_MODE	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED						CH3_MODE	
NONE						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED						CH2_MODE	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED			CH1_TRACEEN	RESERVED		CH1_MODE	
NONE			R/W	NONE		R/W	
0h			0h	0h		0h	

Table 14-25529. CRC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CH4_MODE	R/W	0h	Channel 4 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode For all four channels the seed value can be first planted into PSA register before the Channel Mode is switched to Full-CPU mode since host CPU controls the amount of data for compression. During AUTO mode, the PSA register is automatically reset to zero at the end of each sector compression.
23:18	RESERVED	NONE	0h	Reserved

Table 14-25529. CRC_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	CH3_MODE	R/W	0h	Channel 3 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode
15:10	RESERVED	NONE	0h	Reserved
9:8	CH2_MODE	R/W	0h	Channel 2 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TRACEEN	R/W	0h	Channel 1 Data Trace Enable When set, the channel is put into data trace mode. The channel snoops on the CPU VBUSM, ITCM, DTCM buses for any read transaction. Any read data on these buses is compressed by the PSA Signature Register. When suspend is on, the PSA Signature Register does not compress any read data on these buses. 0 = Data Trace disable 1 = Data Trace enable
3:2	RESERVED	NONE	0h	Reserved
1:0	CH1_MODE	R/W	0h	Channel 1 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode

14.9.6.3.2.4 CRC_INTS Register

1 CRC_INTS Register (Offset = 18h) [reset = 0h]

CRC Interrupt Enable Set Register

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Table 14-25530. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0018h**

Figure 14-8421. CRC_INTS Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT_ENS_	CH4_UNDERENS	CH4_OVERENS	CH4_CRC_FAILENS	CH4_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED			CH3_TIME_OUT_ENS	CH3_UNDERENS	CH3_OVERENS	CH3_CRC_FAILENS	CH3_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED			CH2_TIME_OUT_ENS_	CH2_UNDERENS	CH2_OVERENS	CH2_CRC_FAILENS	CH2_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			CH1_TIME_OUT_ENS_	CH1_UNDERENS	CH1_OVERENS	CH1_CRC_FAILENS	CH1_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 14-25532. CRC_INTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT_ENS_	R/W1TS	0h	Channel 4 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
27	CH4_UNDERENS	R/W1TS	0h	Channel 4 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
26	CH4_OVERENS	R/W1TS	0h	Channel 4 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable

Table 14-25532. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CH4_CRC_FAILENS	R/W1TS	0h	Channel 4 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
24	CH4_CCITENS	R/W1TS	0h	Channel 4 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
23:21	RESERVED	NONE	0h	Reserved
20	CH3_TIME_OUT_ENS	R/W1TS	0h	Channel 3 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
19	CH3_UNDERENS	R/W1TS	0h	Channel 3 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
18	CH3_OVERENS	R/W1TS	0h	Channel 3 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
17	CH3_CRC_FAILENS	R/W1TS	0h	Channel 3 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
16	CH3_CCITENS	R/W1TS	0h	Channel 3 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT_ENS_	R/W1TS	0h	Channel 2 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable

Table 14-25532. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CH2_UNDERENS	R/W1TS	0h	Channel 2 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
10	CH2_OVERENS	R/W1TS	0h	Channel 2 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
9	CH2_CRC_FAILENS	R/W1TS	0h	Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
8	CH2_CCITENS	R/W1TS	0h	Channel 2 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT_ENS_	R/W1TS	0h	Channel 1 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
3	CH1_UNDERENS	R/W1TS	0h	Channel 1 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
2	CH1_OVERENS	R/W1TS	0h	Channel 1 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
1	CH1_CRC_FAILENS	R/W1TS	0h	Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable

Table 14-25532. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_CCITENS	R/W1TS	0h	Channel 1 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable

14.9.6.3.2.5 CRC_INTR Register

1 CRC_INTR Register (Offset = 20h) [reset = 0h]

CRC Interrupt Enable Reset Register

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Table 14-25533. Instance Table

Instance Name	**Physical Address**
MCU_MCRC64_0	**04D0 0020h**

Figure 14-8422. CRC_INTR Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT_ENR	CH4_UNDERENR	CH4_OVERENR	CH4_CRC_FAILENR	CH4_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED			CH3_TIME_OUT_ENR_	CH3_UNDERENR	CH3_OVERENR	CH3_CRC_FAILENR	CH3_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED			CH2_TIME_OUT_ENR_	CH2_UNDERENR	CH2_OVERENR	CH2_CRC_FAILENR	CH2_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			CH1_TIME_OUT_ENR_	CH1_UNDERENR	CH1_OVERENR	CH1_CRC_FAILENR	CH1_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-25535. CRC_INTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT_ENR	R/W1TC	0h	Channel 4 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
27	CH4_UNDERENR	R/W1TC	0h	Channel 4 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
26	CH4_OVERENR	R/W1TC	0h	Channel 4 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable

Table 14-25535. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CH4_CRC_FAILENR	R/W1TC	0h	Channel 4 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
24	CH4_CCITENR	R/W1TC	0h	Channel 4 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
23:21	RESERVED	NONE	0h	Reserved
20	CH3_TIME_OUT_ENR_	R/W1TC	0h	Channel 3 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
19	CH3_UNDERENR	R/W1TC	0h	Channel 3 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
18	CH3_OVERENR	R/W1TC	0h	Channel 3 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
17	CH3_CRC_FAILENR	R/W1TC	0h	Channel 3 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
16	CH3_CCITENR	R/W1TC	0h	Channel 3 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT_ENR_	R/W1TC	0h	Channel 2 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable

Table 14-25535. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CH2_UNDERENR	R/W1TC	0h	Channel 2 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
10	CH2_OVERENR	R/W1TC	0h	Channel 2 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
9	CH2_CRC_FAILENR	R/W1TC	0h	Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
8	CH2_CCITENR	R/W1TC	0h	Channel 2 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT_ENR_	R/W1TC	0h	Channel 1 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
3	CH1_UNDERENR	R/W1TC	0h	Channel 1 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
2	CH1_OVERENR	R/W1TC	0h	Channel 1 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
1	CH1_CRC_FAILENR	R/W1TC	0h	Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable

Table 14-25535. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_CCITENR	R/W1TC	0h	Channel 1 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable

14.9.6.3.2.6 CRC_STATUS Register

1 CRC_STATUS Register (Offset = 28h) [reset = 0h]

CRC Interrupt Status Register

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Table 14-25536. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0028h**

Figure 14-8423. CRC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT	CH4_UNDER	CH4_OVER	CH4_CRC_FAIL	CH4_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED			CH3_TIME_OUT	CH3_UNDER	CH3_OVER	CH3_CRC_FAIL	CH3_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED			CH2_TIME_OUT	CH2_UNDER	CH2_OVER	CH2_CRC_FAIL	CH2_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			CH1_TIME_OUT	CH1_UNDER	CH1_OVER	CH1_CRC_FAIL	CH1_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-25538. CRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT	R/W1TC	0h	Channel 4 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
27	CH4_UNDER	R/W1TC	0h	Channel 4 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
26	CH4_OVER	R/W1TC	0h	Channel 4 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
25	CH4_CRC_FAIL	R/W1TC	0h	Channel 4 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
24	CH4_CCIT	R/W1TC	0h	Channel 4 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active

Table 14-25538. CRC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:21	RESERVED	NONE	0h	Reserved
20	CH3_TIME_OUT	R/W1TC	0h	Channel 3 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
19	CH3_UNDER	R/W1TC	0h	Channel 3 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
18	CH3_OVER	R/W1TC	0h	Channel 3 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
17	CH3_CRC_FAIL	R/W1TC	0h	Channel 3 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
16	CH3_CCIT	R/W1TC	0h	Channel 3 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT	R/W1TC	0h	Channel 2 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
11	CH2_UNDER	R/W1TC	0h	Channel 2 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
10	CH2_OVER	R/W1TC	0h	Channel 2 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
9	CH2_CRC_FAIL	R/W1TC	0h	Channel 2 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
8	CH2_CCIT	R/W1TC	0h	Channel 2 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT	R/W1TC	0h	Channel 1 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
3	CH1_UNDER	R/W1TC	0h	Channel 1 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
2	CH1_OVER	R/W1TC	0h	Channel 1 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
1	CH1_CRC_FAIL	R/W1TC	0h	Channel 1 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active

Table 14-25538. CRC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_CCIT	R/W1TC	0h	Channel 1 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active

14.9.6.3.2.7 CRC_INT_OFFSET_REG Register

1 CRC_INT_OFFSET_REG Register (Offset = 30h) [reset = 0h]

CRC Interrupt Offset

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Table 14-25539. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0030h**

Figure 14-8424. CRC_INT_OFFSET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CRC							
R							
0h							

Table 14-25541. CRC_INT_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CRC	R	0h	Interrupt Offset. This register indicates the highest priority pending interrupt vector address. Reading the offset register automatically clears the respective interrupt flag.

14.9.6.3.2.8 CRC_BUSY Register

1 CRC_BUSY Register (Offset = 38h) [reset = 0h]

CRC Busy Register

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Table 14-25542. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0038h**

Figure 14-8425. CRC_BUSY Name Register

31	30	29	28	27	26	25	24
RESERVED							CH4_BUSY
NONE							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CH3_BUSY
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CH2_BUSY
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CH1_BUSY
NONE							R
0h							0h

Table 14-25544. CRC_BUSY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CH4_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
23:17	RESERVED	NONE	0h	Reserved
16	CH3_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
15:9	RESERVED	NONE	0h	Reserved
8	CH2_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
7:1	RESERVED	NONE	0h	Reserved
0	CH1_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.

14.9.6.3.2.9 CRC_PCOUNT_REG1 Register

1 CRC_PCOUNT_REG1 Register (Offset = 40h) [reset = 0h]

CRC Pattern Counter Preload Register1

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Table 14-25545. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0040h**

Figure 14-8426. CRC_PCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CRC_PAT_COUNT1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT1							
R/W							
0h							

Table 14-25547. CRC_PCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT1	R/W	0h	Channel 1 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.9.6.3.2.10 CRC_SCOUNT_REG1 Register

1 CRC_SCOUNT_REG1 Register (Offset = 44h) [reset = 0h]

CRC Sector Counter Preload Register1

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Table 14-25548. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0044h**

Figure 14-8427. CRC_SCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_SEC_COUNT1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_SEC_COUNT1							
R/W							
0h							

Table 14-25550. CRC_SCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT1	R/W	0h	Channel 1 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.9.6.3.2.11 CRC_CURSEC_REG1 Register

1 CRC_CURSEC_REG1 Register (Offset = 48h) [reset = 0h]

CRC Current Sector Register 1

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Table 14-25551. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0048h**

Figure 14-8428. CRC_CURSEC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC1							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC1							
R							
0h							

Table 14-25553. CRC_CURSEC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC1	R	0h	Channel 1 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.9.6.3.2.12 CRC_WDTOPLD1 Register

1 CRC_WDTOPLD1 Register (Offset = 4Ch) [reset = 0h]

CRC channel 1 Watchdog Timeout Preload Register A

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Table 14-25554. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 004Ch**

Figure 14-8429. CRC_WDTOPLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC_WDTOPLD1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_WDTOPLD1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_WDTOPLD1							
R/W							
0h							

Table 14-25556. CRC_WDTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD1	R/W	0h	Channel 1 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.9.6.3.2.13 CRC_BCTOPLD1 Register

1 CRC_BCTOPLD1 Register (Offset = 50h) [reset = 0h]

CRC channel 1 Block Complete Timeout Preload Register B

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Table 14-25557. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0050h**

Figure 14-8430. CRC_BCTOPLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC_BCTOPLD1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_BCTOPLD1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_BCTOPLD1							
R/W							
0h							

Table 14-25559. CRC_BCTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD1	R/W	0h	Channel 1 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated.

14.9.6.3.2.14 CRC_PSA_SIGREGL1 Register

1 CRC_PSA_SIGREGL1 Register (Offset = 60h) [reset = 0h]

Channel 1 PSA signature low register

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Table 14-25560. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0060h**

Figure 14-8431. CRC_PSA_SIGREGL1 Name Register

31	30	29	28	27	26	25	24
PSASIG1							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG1							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG1							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG1							
R/W							
0h							

Table 14-25562. CRC_PSA_SIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG1	R/W	0h	Channel 1 PSA Signature Low Register. This register contains the value stored at PSASIG1[31:0] register.

14.9.6.3.2.15 CRC_PSA_SIGREGH1 Register

1 CRC_PSA_SIGREGH1 Register (Offset = 64h) [reset = 0h]

Channel 1 PSA signature high register

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Table 14-25563. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0064h**

Figure 14-8432. CRC_PSA_SIGREGH1 Name Register

31	30	29	28	27	26	25	24
PSASIG1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG1_63_32							
R/W							
0h							

Table 14-25565. CRC_PSA_SIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG1_63_32	R/W	0h	Channel 1 PSA Signature High Register. This register contains the value stored at PSASIG1[63:32] register.

14.9.6.3.2.16 CRC_REGL1 Register

1 CRC_REGL1 Register (Offset = 68h) [reset = 0h]

Channel 1 CRC value low register

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Table 14-25566. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0068h**

Figure 14-8433. CRC_REGL1 Name Register

31	30	29	28	27	26	25	24
CRC1							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC1							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC1							
R/W							
0h							

Table 14-25568. CRC_REGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1	R/W	0h	Channel 1 CRC Value Low Register. This register contains the current known good signature value stored at CRC1[31:0] register.

14.9.6.3.2.17 CRC_REGH1 Register

1 CRC_REGH1 Register (Offset = 6Ch) [reset = 0h]

Channel 1 CRC value high register

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Table 14-25569. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 006Ch**

Figure 14-8434. CRC_REGH1 Name Register

31	30	29	28	27	26	25	24
CRC1_47_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC1_47_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC1_47_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC1_47_32							
R/W							
0h							

Table 14-25571. CRC_REGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1_47_32	R/W	0h	Channel 1 CRC Value High Register. This register contains the current known good signature value stored at CRC1[63:32] register.

14.9.6.3.2.18 CRC_PSA_SECSIGREGL1 Register

1 CRC_PSA_SECSIGREGL1 Register (Offset = 70h) [reset = 0h]

Channel 1 PSA sector signature low register

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Table 14-25572. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0070h**

Figure 14-8435. CRC_PSA_SECSIGREGL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PSASECSIG1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PSASECSIG1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PSASECSIG1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PSASECSIG1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25574. CRC_PSA_SECSIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1	R	0h	Channel 1 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG1[31:0] register.

14.9.6.3.2.19 CRC_PSA_SECSIGREGH1 Register

1 CRC_PSA_SECSIGREGH1 Register (Offset = 74h) [reset = 0h]

Channel 1 PSA sector signature high register

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Table 14-25575. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0074h**

Figure 14-8436. CRC_PSA_SECSIGREGH1 Name Register

31	30	29	28	27	26	25	24
PSASECSIG1_63_32							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PSASECSIG1_63_32							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PSASECSIG1_63_32							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PSASECSIG1_63_32							
R							
0h							

Table 14-25577. CRC_PSA_SECSIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1_63_32	R	0h	Channel 1 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG1[63:32] register.

14.9.6.3.2.20 CRC_RAW_DATAREGL1 Register

1 CRC_RAW_DATAREGL1 Register (Offset = 78h) [reset = 0h]

Channel 1 Raw Data Low Register

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Table 14-25578. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0078h**

Figure 14-8437. CRC_RAW_DATAREGL1 Name Register

31	30	29	28	27	26	25	24
RAW_DATA1							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA1							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA1							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA1							
R							
0h							

Table 14-25580. CRC_RAW_DATAREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1	R	0h	Channel 1 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.9.6.3.2.21 CRC_RAW_DATAREGH1 Register

1 CRC_RAW_DATAREGH1 Register (Offset = 7Ch) [reset = 0h]

Channel 1 Raw Data High Register

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Table 14-25581. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 007Ch**

Figure 14-8438. CRC_RAW_DATAREGH1 Name Register

31	30	29	28	27	26	25	24
RAW_DATA1_47_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA1_47_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA1_47_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA1_47_32							
R							
0h							

Table 14-25583. CRC_RAW_DATAREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1_47_32	R	0h	Channel 1 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.9.6.3.2.22 CRC_PCOUNT_REG2 Register

1 CRC_PCOUNT_REG2 Register (Offset = 80h) [reset = 0h]

CRC Pattern Counter Preload Register2

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Table 14-25584. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0080h**

Figure 14-8439. CRC_PCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CRC_PAT_COUNT2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT2							
R/W							
0h							

Table 14-25586. CRC_PCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT2	R/W	0h	CRC Pattern Counter Preload Register 2 This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.9.6.3.2.23 CRC_SCOUNT_REG2 Register

1 CRC_SCOUNT_REG2 Register (Offset = 84h) [reset = 0h]

CRC Sector Counter Preload Register2

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Table 14-25587. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0084h**

Figure 14-8440. CRC_SCOUNT_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_SEC_COUNT2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_SEC_COUNT2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25589. CRC_SCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT2	R/W	0h	Channel 2 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.9.6.3.2.24 CRC_CURSEC_REG2 Register

1 CRC_CURSEC_REG2 Register (Offset = 88h) [reset = 0h]

CRC Current Sector Register 2

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Table 14-25590. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0088h**

Figure 14-8441. CRC_CURSEC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC2							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC2							
R							
0h							

Table 14-25592. CRC_CURSEC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC2	R	0h	Channel 2 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.9.6.3.2.25 CRC_WDTOPLD2 Register

1 CRC_WDTOPLD2 Register (Offset = 8Ch) [reset = 0h]

CRC channel 2 Watchdog Timeout Preload Register

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Table 14-25593. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 008Ch**

Figure 14-8442. CRC_WDTOPLD2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_WDTOPLD2							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_WDTOPLD2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_WDTOPLD2							
R/W							
0h							

Table 14-25595. CRC_WDTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD2	R/W	0h	Channel 2 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.9.6.3.2.26 CRC_BCTOPLD2 Register

1 CRC_BCTOPLD2 Register (Offset = 90h) [reset = 0h]

CRC channel 2 Block Complete Timeout Preload Register

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Table 14-25596. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0090h**

Figure 14-8443. CRC_BCTOPLD2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD2							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD2							
R/W							
0h							

Table 14-25598. CRC_BCTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD2	R/W	0h	Channel 2 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.9.6.3.2.27 CRC_PSA_SIGREGL2 Register

1 CRC_PSA_SIGREGL2 Register (Offset = A0h) [reset = 0h]

Channel 2 PSA signature low register

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Table 14-25599. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00A0h**

Figure 14-8444. CRC_PSA_SIGREGL2 Name Register

31	30	29	28	27	26	25	24
PSASIG2							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG2							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG2							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG2							
R/W							
0h							

Table 14-25601. CRC_PSA_SIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG2	R/W	0h	Channel 2 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register.

14.9.6.3.2.28 CRC_PSA_SIGREGH2 Register

1 CRC_PSA_SIGREGH2 Register (Offset = A4h) [reset = 0h]

Channel 2 PSA signature high register

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Table 14-25602. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00A4h**

Figure 14-8445. CRC_PSA_SIGREGH2 Name Register

31	30	29	28	27	26	25	24
PSASIG2_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG2_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG2_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG2_63_32							
R/W							
0h							

Table 14-25604. CRC_PSA_SIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG2_63_32	R/W	0h	Channel 2 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register.

14.9.6.3.2.29 CRC_REGL2 Register

1 CRC_REGL2 Register (Offset = A8h) [reset = 0h]

Channel 2 CRC value low register

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Table 14-25605. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00A8h**

Figure 14-8446. CRC_REGL2 Name Register

31	30	29	28	27	26	25	24
CRC2							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC2							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC2							
R/W							
0h							

Table 14-25607. CRC_REGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2	R/W	0h	Channel 2 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register.

14.9.6.3.2.30 CRC_REGH2 Register

1 CRC_REGH2 Register (Offset = ACh) [reset = 0h]

Channel 2 CRC value high register

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Table 14-25608. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00ACh**

Figure 14-8447. CRC_REGH2 Name Register

31	30	29	28	27	26	25	24
CRC2_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC2_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC2_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC2_63_32							
R/W							
0h							

Table 14-25610. CRC_REGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2_63_32	R/W	0h	Channel 2 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register.

14.9.6.3.2.31 CRC_PSA_SECSIGREGL2 Register

1 CRC_PSA_SECSIGREGL2 Register (Offset = B0h) [reset = 0h]

Channel 2 PSA sector signature low register

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Table 14-25611. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00B0h**

Figure 14-8448. CRC_PSA_SECSIGREGL2 Name Register

31	30	29	28	27	26	25	24
PSASECSIG2							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG2							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG2							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG2							
R							
0h							

Table 14-25613. CRC_PSA_SECSIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2	R	0h	Channel 2 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register.

14.9.6.3.2.32 CRC_PSA_SECSIGREGH2 Register

1 CRC_PSA_SECSIGREGH2 Register (Offset = B4h) [reset = 0h]

Channel 2 PSA sector signature high register

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Table 14-25614. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00B4h**

Figure 14-8449. CRC_PSA_SECSIGREGH2 Name Register

31	30	29	28	27	26	25	24
PSASECSIG2_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG2_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG2_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG2_63_32							
R							
0h							

Table 14-25616. CRC_PSA_SECSIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2_63_32	R	0h	Channel 2 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register.

14.9.6.3.2.33 CRC_RAW_DATAREGL2 Register

1 CRC_RAW_DATAREGL2 Register (Offset = B8h) [reset = 0h]

Channel 2 Raw Data Low Register

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Table 14-25617. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00B8h**

Figure 14-8450. CRC_RAW_DATAREGL2 Name Register

31	30	29	28	27	26	25	24
RAW_DATA2							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA2							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA2							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA2							
R							
0h							

Table 14-25619. CRC_RAW_DATAREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2	R	0h	Channel 2 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.9.6.3.2.34 CRC_RAW_DATAREGH2 Register

1 CRC_RAW_DATAREGH2 Register (Offset = BCh) [reset = 0h]

Channel 2 Raw Data High Register

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Table 14-25620. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00BCh**

Figure 14-8451. CRC_RAW_DATAREGH2 Name Register

31	30	29	28	27	26	25	24
RAW_DATA2_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA2_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA2_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA2_63_32							
R							
0h							

Table 14-25622. CRC_RAW_DATAREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2_63_32	R	0h	Channel 2 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.9.6.3.2.35 CRC_PCOUNT_REG3 Register

1 CRC_PCOUNT_REG3 Register (Offset = C0h) [reset = 0h]

CRC Pattern Counter Preload Register3

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Table 14-25623. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00C0h**

Figure 14-8452. CRC_PCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CRC_PAT_COUNT3			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT3							
R/W							
0h							

Table 14-25625. CRC_PCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT3	R/W	0h	Channel 3 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.9.6.3.2.36 CRC_SCOUNT_REG3 Register

1 CRC_SCOUNT_REG3 Register (Offset = C4h) [reset = 0h]

CRC Sector Counter Preload Register3

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Table 14-25626. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00C4h**

Figure 14-8453. CRC_SCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT3							
R/W							
0h							

Table 14-25628. CRC_SCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT3	R/W	0h	Channel 3 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.9.6.3.2.37 CRC_CURSEC_REG3 Register

1 CRC_CURSEC_REG3 Register (Offset = C8h) [reset = 0h]

CRC Current Sector Register 3

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Table 14-25629. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00C8h**

Figure 14-8454. CRC_CURSEC_REG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_CURSEC3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_CURSEC3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25631. CRC_CURSEC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC3	R	0h	Channel 3 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.9.6.3.2.38 CRC_WDTOPLD3 Register

1 CRC_WDTOPLD3 Register (Offset = CCh) [reset = 0h]

CRC channel 3 Watchdog Timeout Preload Register

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Table 14-25632. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00CCh**

Figure 14-8455. CRC_WDTOPLD3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_WDTOPLD3							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_WDTOPLD3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_WDTOPLD3							
R/W							
0h							

Table 14-25634. CRC_WDTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD3	R/W	0h	Channel 3 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.9.6.3.2.39 CRC_BCTOPLD3 Register

1 CRC_BCTOPLD3 Register (Offset = D0h) [reset = 0h]

CRC channel 3 Block Complete Timeout Preload Register

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Table 14-25635. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00D0h**

Figure 14-8456. CRC_BCTOPLD3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD3							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD3							
R/W							
0h							

Table 14-25637. CRC_BCTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD3	R/W	0h	Channel 3 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.9.6.3.2.40 CRC_PSA_SIGREGL3 Register

1 CRC_PSA_SIGREGL3 Register (Offset = E0h) [reset = 0h]

Channel 3 PSA signature low register

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Table 14-25638. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00E0h**

Figure 14-8457. CRC_PSA_SIGREGL3 Name Register

31	30	29	28	27	26	25	24
PSASIG3							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG3							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG3							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG3							
R/W							
0h							

Table 14-25640. CRC_PSA_SIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG3	R/W	0h	Channel 3 PSA Signature Low Register. This register contains the value stored at PSASIG3[31:0] register.

14.9.6.3.2.41 CRC_PSA_SIGREGH3 Register

1 CRC_PSA_SIGREGH3 Register (Offset = E4h) [reset = 0h]

Channel 3 PSA signature high register

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Table 14-25641. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00E4h**

Figure 14-8458. CRC_PSA_SIGREGH3 Name Register

31	30	29	28	27	26	25	24
PSASIG3_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG3_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG3_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG3_63_32							
R/W							
0h							

Table 14-25643. CRC_PSA_SIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG3_63_32	R/W	0h	Channel 3 PSA Signature High Register. This register contains the value stored at PSASIG3[63:32] register.

14.9.6.3.2.42 CRC_REGL3 Register

1 CRC_REGL3 Register (Offset = E8h) [reset = 0h]

Channel 3 CRC value low register

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Table 14-25644. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00E8h**

Figure 14-8459. CRC_REGL3 Name Register

31	30	29	28	27	26	25	24
CRC3							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC3							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC3							
R/W							
0h							

Table 14-25646. CRC_REGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC3	R/W	0h	Channel 3 CRC Value Low Register. This register contains the current known good signature value stored at CRC3[31:0] register.

14.9.6.3.2.43 CRC_REGH3 Register

1 CRC_REGH3 Register (Offset = ECh) [reset = 0h]

Channel 3 CRC value high register

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Table 14-25647. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00ECh**

Figure 14-8460. CRC_REGH3 Name Register

31	30	29	28	27	26	25	24
CRC3_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC3_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC3_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC3_63_32							
R/W							
0h							

Table 14-25649. CRC_REGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC3_63_32	R/W	0h	Channel 3 CRC Value High Register. This register contains the current known good signature value stored at CRC3[63:32] register.

14.9.6.3.2.44 CRC_PSA_SECSIGREGL3 Register

1 CRC_PSA_SECSIGREGL3 Register (Offset = F0h) [reset = 0h]

Channel 3 PSA sector signature low register

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Table 14-25650. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00F0h**

Figure 14-8461. CRC_PSA_SECSIGREGL3 Name Register

31	30	29	28	27	26	25	24
PSASECSIG3							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG3							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG3							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG3							
R							
0h							

Table 14-25652. CRC_PSA_SECSIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG3	R	0h	Channel 3 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG3[31:0] register.

14.9.6.3.2.45 CRC_PSA_SECSIGREGH3 Register

1 CRC_PSA_SECSIGREGH3 Register (Offset = F4h) [reset = 0h]

Channel 3 PSA sector signature high register

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Table 14-25653. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00F4h**

Figure 14-8462. CRC_PSA_SECSIGREGH3 Name Register

31	30	29	28	27	26	25	24
PSASECSIG3_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG3_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG3_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG3_63_32							
R							
0h							

Table 14-25655. CRC_PSA_SECSIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG3_63_32	R	0h	Channel 3 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG3[63:32] register.

14.9.6.3.2.46 CRC_RAW_DATAREGL3 Register

1 CRC_RAW_DATAREGL3 Register (Offset = F8h) [reset = 0h]

Channel 3 Raw Data Low Register

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Table 14-25656. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00F8h**

Figure 14-8463. CRC_RAW_DATAREGL3 Name Register

31	30	29	28	27	26	25	24
RAW_DATA3							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA3							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA3							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA3							
R							
0h							

Table 14-25658. CRC_RAW_DATAREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA3	R	0h	Channel 3 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.9.6.3.2.47 CRC_RAW_DATAREGH3 Register

1 CRC_RAW_DATAREGH3 Register (Offset = FCh) [reset = 0h]

Channel 3 Raw Data High Register

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Table 14-25659. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 00FCh**

Figure 14-8464. CRC_RAW_DATAREGH3 Name Register

31	30	29	28	27	26	25	24
RAW_DATA3_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA3_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA3_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA3_63_32							
R							
0h							

Table 14-25661. CRC_RAW_DATAREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA3_63_32	R	0h	Channel 3 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.9.6.3.2.48 CRC_PCOUNT_REG4 Register

1 CRC_PCOUNT_REG4 Register (Offset = 100h) [reset = 0h]

CRC Pattern Counter Preload Register4

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Table 14-25662. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0100h**

Figure 14-8465. CRC_PCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CRC_PAT_COUNT4			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT4							
R/W							
0h							

Table 14-25664. CRC_PCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT4	R/W	0h	Channel 4 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.9.6.3.2.49 CRC_SCOUNT_REG4 Register

1 CRC_SCOUNT_REG4 Register (Offset = 104h) [reset = 0h]

CRC Sector Counter Preload Register4

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Table 14-25665. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0104h**

Figure 14-8466. CRC_SCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT4							
R/W							
0h							

Table 14-25667. CRC_SCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT4	R/W	0h	Channel 4 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.9.6.3.2.50 CRC_CURSEC_REG4 Register

1 CRC_CURSEC_REG4 Register (Offset = 108h) [reset = 0h]

CRC Current Sector Register 4

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Table 14-25668. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0108h**

Figure 14-8467. CRC_CURSEC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC4							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC4							
R							
0h							

Table 14-25670. CRC_CURSEC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC4	R	0h	In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. In Semi-CPU mode, this register is used to indicate the sector number for which the compression complete has last happened.

14.9.6.3.2.51 CRC_WDTOPLD4 Register

1 CRC_WDTOPLD4 Register (Offset = 10Ch) [reset = 0h]

CRC channel 4 Watchdog Timeout Preload Register

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Table 14-25671. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 010Ch**

Figure 14-8468. CRC_WDTOPLD4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC_WDTOPLD4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_WDTOPLD4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_WDTOPLD4							
R/W							
0h							

Table 14-25673. CRC_WDTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD4	R/W	0h	This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.9.6.3.2.52 CRC_BCTOPLD4 Register

1 CRC_BCTOPLD4 Register (Offset = 110h) [reset = 0h]

CRC channel 4 Block Complete Timeout Preload Register

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Table 14-25674. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0110h**

Figure 14-8469. CRC_BCTOPLD4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD4							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD4							
R/W							
0h							

Table 14-25676. CRC_BCTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD4	R/W	0h	This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.9.6.3.2.53 CRC_PSA_SIGREGL4 Register

1 CRC_PSA_SIGREGL4 Register (Offset = 120h) [reset = 0h]

Channel 4 PSA signature low register

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Table 14-25677. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0120h**

Figure 14-8470. CRC_PSA_SIGREGL4 Name Register

31	30	29	28	27	26	25	24
PSASIG4							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PSASIG4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PSASIG4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PSASIG4							
R/W							
0h							

Table 14-25679. CRC_PSA_SIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG4	R/W	0h	This register contains the value stored at PSASIG4[31:0] register.

14.9.6.3.2.54 CRC_PSA_SIGREGH4 Register

1 CRC_PSA_SIGREGH4 Register (Offset = 124h) [reset = 0h]

Channel 4 PSA signature high register

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Table 14-25680. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0124h**

Figure 14-8471. CRC_PSA_SIGREGH4 Name Register

31	30	29	28	27	26	25	24
PSASIG4_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG4_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG4_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG4_63_32							
R/W							
0h							

Table 14-25682. CRC_PSA_SIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG4_63_32	R/W	0h	This register contains the value stored at PSASIG4[63:32] register.

14.9.6.3.2.55 CRC_REGL4 Register

1 CRC_REGL4 Register (Offset = 128h) [reset = 0h]

Channel 4 CRC value low register

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Table 14-25683. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0128h**

Figure 14-8472. CRC_REGL4 Name Register

31	30	29	28	27	26	25	24
CRC4							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC4							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC4							
R/W							
0h							

Table 14-25685. CRC_REGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC4	R/W	0h	Channel 4 CRC Value Low Register.

14.9.6.3.2.56 CRC_REGH4 Register

1 CRC_REGH4 Register (Offset = 12Ch) [reset = 0h]

Channel 4 CRC value high register

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Table 14-25686. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 012Ch**

Figure 14-8473. CRC_REGH4 Name Register

31	30	29	28	27	26	25	24
CRC4_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC4_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC4_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC4_63_32							
R/W							
0h							

Table 14-25688. CRC_REGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC4_63_32	R/W	0h	Channel 4 CRC Value High Register.

14.9.6.3.2.57 CRC_PSA_SECSIGREGL4 Register

1 CRC_PSA_SECSIGREGL4 Register (Offset = 130h) [reset = 0h]

Channel 4 PSA sector signature low register

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Table 14-25689. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0130h**

Figure 14-8474. CRC_PSA_SECSIGREGL4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PSASECSIG4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PSASECSIG4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PSASECSIG4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PSASECSIG4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25691. CRC_PSA_SECSIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG4	R	0h	Channel 4 PSA Sector Signature Low Register.

14.9.6.3.2.58 CRC_PSA_SECSIGREGH4 Register

1 CRC_PSA_SECSIGREGH4 Register (Offset = 134h) [reset = 0h]

Channel 4 PSA sector signature high register

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Table 14-25692. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0134h**

Figure 14-8475. CRC_PSA_SECSIGREGH4 Name Register

31	30	29	28	27	26	25	24
PSASECSIG4_63_32							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PSASECSIG4_63_32							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PSASECSIG4_63_32							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PSASECSIG4_63_32							
R							
0h							

Table 14-25694. CRC_PSA_SECSIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG4_63_32	R	0h	Channel 4 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG4[63:32] register.

14.9.6.3.2.59 CRC_RAW_DATAREGL4 Register

1 CRC_RAW_DATAREGL4 Register (Offset = 138h) [reset = 0h]

Channel 4 Raw Data Low Register

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Table 14-25695. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0138h**

Figure 14-8476. CRC_RAW_DATAREGL4 Name Register

31	30	29	28	27	26	25	24
RAW_DATA4							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA4							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA4							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA4							
R							
0h							

Table 14-25697. CRC_RAW_DATAREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA4	R	0h	Channel 4 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.9.6.3.2.60 CRC_RAW_DATAREGH4 Register

1 CRC_RAW_DATAREGH4 Register (Offset = 13Ch) [reset = 0h]

Channel 4 Raw Data High Register

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Table 14-25698. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 013Ch**

Figure 14-8477. CRC_RAW_DATAREGH4 Name Register

31	30	29	28	27	26	25	24
RAW_DATA4_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA4_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA4_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA4_63_32							
R							
0h							

Table 14-25700. CRC_RAW_DATAREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA4_63_32	R	0h	Channel 4 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.9.6.3.2.61 CRC_MBUS_SEL Register

1 CRC_MBUS_SEL Register (Offset = 140h) [reset = 7h]

Data bus tracing selection

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Table 14-25701. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0140h**

Figure 14-8478. CRC_MBUS_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MEN	DTC_MEN	ITC_MEN
NONE					R/W	R/W	R/W
0h					1h	1h	1h

Table 14-25703. CRC_MBUS_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MEN	R/W	1h	Enable/disables the tracing of VBUSM 0: Tracing of VBUSM controller bus has been disabled 1: Tracing of VBUSM controller bus has been enabled
1	DTC_MEN	R/W	1h	Enable/disables the tracing of data TCM 0: Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled 1: Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled
0	ITC_MEN	R/W	1h	Enable/disables the tracing of instruction TCM 0: Tracing of ITCM bus has been disabled 1: Tracing of ITCM bus has been enabled Please refer the description of CPU Data trace at page 1-21 for the priority between different data buses.

14.9.6.3.2.62 CRC_I0_PSA_SIGREG1_CPY_j Register

1 CRC_I0_PSA_SIGREG1_CPY_j Register (Offset = 200h + formula) [reset = 0h]

Region for Channel 1 PSA signature block used by DMA based systems.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 31d

Table 14-25704. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	04D0 0200h + formula

Figure 14-8479. CRC_I0_PSA_SIGREG1_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG1_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG1_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG1_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG1_CPY0							
W							
0h							

Table 14-25706. CRC_I0_PSA_SIGREG1_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG1_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG1 register for DMA destination, it is write only, the result can be found in the PSASIG1 register.

14.9.6.3.2.63 CRC_I0_PSA_SIGREG2_CPY_j Register

1 CRC_I0_PSA_SIGREG2_CPY_j Register (Offset = 280h + formula) [reset = 0h]

Region for Channel 2 PSA signature block used by DMA based systems.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 31d

Table 14-25707. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0280h + formula**

Figure 14-8480. CRC_I0_PSA_SIGREG2_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG2_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG2_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG2_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG2_CPY0							
W							
0h							

Table 14-25709. CRC_I0_PSA_SIGREG2_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG2_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG2 register for DMA destination, it is write only, the result can be found in the PSASIG2 register.

14.9.6.3.2.64 CRC_I0_PSA_SIGREG3_CPY_j Register

1 CRC_I0_PSA_SIGREG3_CPY_j Register (Offset = 300h + formula) [reset = 0h]

Region for Channel 3 PSA signature block used by DMA based systems.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 31d

Table 14-25710. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0300h + formula**

Figure 14-8481. CRC_I0_PSA_SIGREG3_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG3_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG3_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG3_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG3_CPY0							
W							
0h							

Table 14-25712. CRC_I0_PSA_SIGREG3_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG3_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG3 register for DMA destination, it is write only, the result can be found in the PSASIG3 register.

14.9.6.3.2.65 CRC_I0_PSA_SIGREG4_CPY_j Register

1 CRC_I0_PSA_SIGREG4_CPY_j Register (Offset = 380h + formula) [reset = 0h]

Region for Channel 4 PSA signature block used by DMA based systems.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 31d

Table 14-25713. Instance Table

Instance Name	Physical Address
MCU_MCRC64_0	**04D0 0380h + formula**

Figure 14-8482. CRC_I0_PSA_SIGREG4_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG4_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG4_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG4_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG4_CPY0							
W							
0h							

Table 14-25715. CRC_I0_PSA_SIGREG4_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG4_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG4 register for DMA destination, it is write only, the result can be found in the PSASIG4 register.

14.9.6.4 ecc_aggr

ecc_aggr

14.9.6.4.1 ecc_aggr Summaries

ecc_aggr Summaries

Table 14-25716. ECC_AGGR Registers, Base Address=0070 1000h, Length=1024

Offset	Length	Register Name	ECC_AGGR1 Physical Address
0h	32	ECC_AGGR_REV	0070 1000h
8h	32	ECC_AGGR_VECTOR	0070 1008h
Ch	32	ECC_AGGR_STAT	0070 100Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0070 1010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0070 103Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0070 1040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0070 1080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0070 10C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0070 113Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0070 1140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0070 1180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0070 11C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0070 1200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0070 1204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0070 1208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0070 120Ch

14.9.6.4.2 ecc_aggr Registers

ecc_aggr Registers

14.9.6.4.2.1 ECC_AGGR_REV Register

1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-25717. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1000h**

Figure 14-8483. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
7h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-25719. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.9.6.4.2.2 ECC_AGGR_VECTOR Register

1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-25720. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1008h**

Figure 14-8484. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-25722. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.9.6.4.2.3 ECC_AGGR_STAT Register

1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 6h]

Misc Status

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Table 14-25723. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 100Ch**

Figure 14-8485. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					6h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
6h							

Table 14-25725. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	6h	Indicates the number of RAMS serviced by the ECC aggregator

14.9.6.4.2.4 ECC_AGGR_RESERVED_SVBUS_j Register

1 ECC_AGGR_RESERVED_SVBUS_j Register (Offset = 10h + formula) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = (j * 4h); where j = 0 to 7d

Table 14-25726. Instance Table

Instance Name	Physical Address
ECC_AGGR1	0070 1010h + formula

Figure 14-8486. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-25728. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.9.6.4.2.5 ECC_AGGR_SEC_EOI_REG Register

1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-25729. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 103Ch**

Figure 14-8487. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-25731. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.6.4.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-25732. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1040h**

Figure 14-8488. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_PEND	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_PEND	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_PEND	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_PEND	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_PEND	IMAILBOX8_MAIN_0__RAMECC_PEND
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h		0h	0h	0h	0h	0h	0h

Table 14-25734. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend

Table 14-25734. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
3	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend
2	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend
1	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_Ik3vtm_n16ffc_main_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_main_0_vbusp_bridge_busecc_pend
0	IMAILBOX8_MAIN_0__RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for Imailbox8_main_0__ramecc_pend

14.9.6.4.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-25735. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1080h**

Figure 14-8489. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_SET	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_SET	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_ENABLE_SET	IMAILBOX8_MAIN_0__RAMECC_ENABLE_SET
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h		0h	0h	0h	0h	0h	0h

Table 14-25737. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend

Table 14-25737. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
3	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend
2	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend
1	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_Ik3vtm_n16ffc_main_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_main_0_vbusp_bridge_busecc_pend
0	IMAILBOX8_MAIN_0__RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Imailbox8_main_0__ramecc_pend

14.9.6.4.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-25738. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 10C0h**

Figure 14-8490. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_CLR	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_CLR	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	IMAILBOX8_MAIN_0__RAMECC_ENABLE_CLR
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h

Table 14-25740. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend

Table 14-25740. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
3	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend
2	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend
1	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_Ik3vtm_n16ffc_main_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_main_0_vbusp_bridge_busecc_pend
0	IMAILBOX8_MAIN_0__RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Imailbox8_main_0__ramecc_pend

14.9.6.4.2.9 ECC_AGGR_DED_EOI_REG Register

1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-25741. Instance Table

Instance Name	Physical Address
ECC_AGGR1	0070 113Ch

Figure 14-8491. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-25743. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.9.6.4.2.10 ECC_AGGR_DED_STATUS_REG0 Register

1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-25744. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1140h**

Figure 14-8492. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_PEND	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_PEND	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_PEND	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_PEND	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_PEND	IMAILBOX8_MAIN_0__RAMECC_PEND
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h		0h	0h	0h	0h	0h	0h

Table 14-25746. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend

Table 14-25746. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
3	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend
2	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend
1	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_Ik3vtm_n16ffc_main_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_main_0_vbusp_bridge_busecc_pend
0	IMAILBOX8_MAIN_0__RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for Imailbox8_main_0__ramecc_pend

14.9.6.4.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-25747. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1180h**

Figure 14-8493. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_SET	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_SET	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_ENABLE_SET	IMAILBOX8_MAIN_0__RAMECC_ENABLE_SET
NONE		R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h		0h	0h	0h	0h	0h	0h

Table 14-25749. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend

Table 14-25749. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
3	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend
2	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend
1	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_Ik3vtm_n16ffc_main_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_main_0_vbusp_bridge_busecc_pend
0	IMAILBOX8_MAIN_0__RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for Imailbox8_main_0__ramecc_pend

14.9.6.4.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-25750. Instance Table

Instance Name	Physical Address
ECC_AGGR1	0070 11C0h

Figure 14-8494. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_CLR	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_CLR	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	IMAILBOX8_MAIN_0__RAMECC_ENABLE_CLR
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h

Table 14-25752. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend

Table 14-25752. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_src_busecc_pend
3	IAM64_MAIN_FW_CBASS_MAIN_0_AM64_MAIN_FW_CBASS_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_P2P_BRIDGE_IAM64_MCU_CBASS_CBASS_MCU_0_CBASS_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_fw_cbass_main_0_am64_main_fw_cbass_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_p2p_bridge_Iam64_mcu_cbass_cbass_mcu_0_cbass_dmsc_slv_bridge_dst_busecc_pend
2	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_MAIN_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MAIN_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_main_SYSCLK0_4_clk_edc_ctrl_cbass_int_main_SYSCLK0_4_busecc_pend
1	IAM64_MAIN_INFRA_CBASS_CBASS_MAIN_0_AM64_MAIN_INFRA_CBASS_CBASS_IK3VTM_N16FFC_MAIN_0_VBUSP_P2P_BRIDGE_IK3VTM_N16FFC_MAIN_0_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Iam64_main_infra_cbass_cbass_main_0_am64_main_infra_cbass_cbass_Ik3vtm_n16ffc_main_0_vbusp_p2p_bridge_Ik3vtm_n16ffc_main_0_vbusp_bridge_busecc_pend
0	IMAILBOX8_MAIN_0__RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for Imailbox8_main_0__ramecc_pend

14.9.6.4.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-25753. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1200h**

Figure 14-8495. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-25755. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.9.6.4.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-25756. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1204h**

Figure 14-8496. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-25758. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.9.6.4.2.15 ECC_AGGR_AGGR_STATUS_SET Register

1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-25759. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 1208h**

Figure 14-8497. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-25761. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.9.6.4.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-25762. Instance Table

Instance Name	Physical Address
ECC_AGGR1	**0070 120Ch**

Figure 14-8498. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-25764. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.10 PBIST Registers

14.10.1 PBIST

PBIST

14.10.1.1 PBIST Summaries

PBIST Summaries

Table 14-25765. PBIST Registers, Base Address=0031 0000h, Length=1024

Offset	Length	Register Name	PBIST0 Physical Address	PBIST1 Physical Address	PBIST2 Physical Address
100h	32	PBIST_A0	0031 0100h	3F10 0100h	0333 0100h
104h	32	PBIST_A1	0031 0104h	3F10 0104h	0333 0104h
108h	32	PBIST_A2	0031 0108h	3F10 0108h	0333 0108h
10Ch	32	PBIST_A3	0031 010Ch	3F10 010Ch	0333 010Ch
110h	32	PBIST_L0	0031 0110h	3F10 0110h	0333 0110h
114h	32	PBIST_L1	0031 0114h	3F10 0114h	0333 0114h
118h	32	PBIST_L2	0031 0118h	3F10 0118h	0333 0118h
11Ch	32	PBIST_L3	0031 011Ch	3F10 011Ch	0333 011Ch
120h	32	PBIST_D	0031 0120h	3F10 0120h	0333 0120h
124h	32	PBIST_E	0031 0124h	3F10 0124h	0333 0124h
130h	32	PBIST_CA0	0031 0130h	3F10 0130h	0333 0130h
134h	32	PBIST_CA1	0031 0134h	3F10 0134h	0333 0134h
138h	32	PBIST_CA2	0031 0138h	3F10 0138h	0333 0138h
13Ch	32	PBIST_CA3	0031 013Ch	3F10 013Ch	0333 013Ch
140h	32	PBIST_CL0	0031 0140h	3F10 0140h	0333 0140h
144h	32	PBIST_CL1	0031 0144h	3F10 0144h	0333 0144h
148h	32	PBIST_CL2	0031 0148h	3F10 0148h	0333 0148h
14Ch	32	PBIST_CL3	0031 014Ch	3F10 014Ch	0333 014Ch
150h	32	PBIST_I0	0031 0150h	3F10 0150h	0333 0150h
154h	32	PBIST_I1	0031 0154h	3F10 0154h	0333 0154h
158h	32	PBIST_I2	0031 0158h	3F10 0158h	0333 0158h
15Ch	32	PBIST_I3	0031 015Ch	3F10 015Ch	0333 015Ch
160h	32	PBIST_RAMT	0031 0160h	3F10 0160h	0333 0160h
164h	32	PBIST_DLR	0031 0164h	3F10 0164h	0333 0164h
168h	32	PBIST_CMS	0031 0168h	3F10 0168h	0333 0168h
16Ch	32	PBIST_STR	0031 016Ch	3F10 016Ch	0333 016Ch
170h	64	PBIST_SCR	0031 0170h	3F10 0170h	0333 0170h
178h	32	PBIST_CSR	0031 0178h	3F10 0178h	0333 0178h
17Ch	32	PBIST_FDLY	0031 017Ch	3F10 017Ch	0333 017Ch
180h	32	PBIST_PACT	0031 0180h	3F10 0180h	0333 0180h
184h	32	PBIST_PID	0031 0184h	3F10 0184h	0333 0184h
188h	32	PBIST_OVER	0031 0188h	3F10 0188h	0333 0188h
190h	64	PBIST_FSRF	0031 0190h	3F10 0190h	0333 0190h
198h	64	PBIST_FSRC	0031 0198h	3F10 0198h	0333 0198h
1A0h	64	PBIST_FSRA	0031 01A0h	3F10 01A0h	0333 01A0h
1A8h	32	PBIST_FSRDL0	0031 01A8h	3F10 01A8h	0333 01A8h
1B0h	32	PBIST_FSRDL1	0031 01B0h	3F10 01B0h	0333 01B0h

Table 14-25765. PBIST Registers, Base Address=0031 0000h, Length=1024 (continued)

Offset	Length	Register Name	PBIST0 Physical Address	PBIST1 Physical Address	PBIST2 Physical Address
1B4h	32	PBIST_MARGIN_MODE	0031 01B4h	3F10 01B4h	0333 01B4h
1B8h	32	PBIST_WRENZ	0031 01B8h	3F10 01B8h	0333 01B8h
1BCh	32	PBIST_PAGE_PGS	0031 01BCh	3F10 01BCh	0333 01BCh
1C0h	32	PBIST_ROM	0031 01C0h	3F10 01C0h	0333 01C0h
1C4h	32	PBIST_ALGO	0031 01C4h	3F10 01C4h	0333 01C4h
1C8h	64	PBIST_RINFO	0031 01C8h	3F10 01C8h	0333 01C8h

Table 14-25766. PBIST Registers, Base Address=0031 0000h, Length=1024

Offset	Length	Register Name	PBIST3 Physical Address
100h	32	PBIST_A0	0331 0100h
104h	32	PBIST_A1	0331 0104h
108h	32	PBIST_A2	0331 0108h
10Ch	32	PBIST_A3	0331 010Ch
110h	32	PBIST_L0	0331 0110h
114h	32	PBIST_L1	0331 0114h
118h	32	PBIST_L2	0331 0118h
11Ch	32	PBIST_L3	0331 011Ch
120h	32	PBIST_D	0331 0120h
124h	32	PBIST_E	0331 0124h
130h	32	PBIST_CA0	0331 0130h
134h	32	PBIST_CA1	0331 0134h
138h	32	PBIST_CA2	0331 0138h
13Ch	32	PBIST_CA3	0331 013Ch
140h	32	PBIST_CL0	0331 0140h
144h	32	PBIST_CL1	0331 0144h
148h	32	PBIST_CL2	0331 0148h
14Ch	32	PBIST_CL3	0331 014Ch
150h	32	PBIST_I0	0331 0150h
154h	32	PBIST_I1	0331 0154h
158h	32	PBIST_I2	0331 0158h
15Ch	32	PBIST_I3	0331 015Ch
160h	32	PBIST_RAMT	0331 0160h
164h	32	PBIST_DLR	0331 0164h
168h	32	PBIST_CMS	0331 0168h
16Ch	32	PBIST_STR	0331 016Ch
170h	64	PBIST_SCR	0331 0170h
178h	32	PBIST_CSR	0331 0178h
17Ch	32	PBIST_FDLY	0331 017Ch
180h	32	PBIST_PACT	0331 0180h
184h	32	PBIST_PID	0331 0184h
188h	32	PBIST_OVER	0331 0188h
190h	64	PBIST_FSRF	0331 0190h
198h	64	PBIST_FSRC	0331 0198h
1A0h	64	PBIST_FSRA	0331 01A0h

Table 14-25766. PBIST Registers, Base Address=0031 0000h, Length=1024 (continued)

Offset	Length	Register Name	PBIST3 Physical Address
1A8h	32	PBIST_FSRDL0	0331 01A8h
1B0h	32	PBIST_FSRDL1	0331 01B0h
1B4h	32	PBIST_MARGIN_MODE	0331 01B4h
1B8h	32	PBIST_WRENZ	0331 01B8h
1BCh	32	PBIST_PAGE_PGS	0331 01BCh
1C0h	32	PBIST_ROM	0331 01C0h
1C4h	32	PBIST_ALGO	0331 01C4h
1C8h	64	PBIST_RINFO	0331 01C8h

14.10.1.2 PBIST Registers

PBIST Registers

14.10.1.2.1 PBIST_A0 Register

1 PBIST_A0 Register (Offset = 100h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-25767. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0100h**
PBIST1	**3F10 0100h**
PBIST2	**0333 0100h**
PBIST3	**0331 0100h**

Figure 14-8499. PBIST_A0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A0							
R/W							
0h							
7	6	5	4	3	2	1	0
A0							
R/W							
0h							

Table 14-25769. PBIST_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A0	R/W	0h	Variable Address Register 0 (A0) Reset Source: mod_g_rst_n

14.10.1.2.2 PBIST_A1 Register

1 PBIST_A1 Register (Offset = 104h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-25770. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0104h**
PBIST1	**3F10 0104h**
PBIST2	**0333 0104h**
PBIST3	**0331 0104h**

Figure 14-8500. PBIST_A1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A1							
R/W							
0h							
7	6	5	4	3	2	1	0
A1							
R/W							
0h							

Table 14-25772. PBIST_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A1	R/W	0h	Variable Address Register 1 (A1) Reset Source: mod_g_rst_n

14.10.1.2.3 PBIST_A2 Register

1 PBIST_A2 Register (Offset = 108h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-25773. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0108h**
PBIST1	**3F10 0108h**
PBIST2	**0333 0108h**
PBIST3	**0331 0108h**

Figure 14-8501. PBIST_A2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A2							
R/W							
0h							
7	6	5	4	3	2	1	0
A2							
R/W							
0h							

Table 14-25775. PBIST_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A2	R/W	0h	Variable Address Register 2 (A2) Reset Source: mod_g_rst_n

14.10.1.2.4 PBIST_A3 Register

1 PBIST_A3 Register (Offset = 10Ch) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-25776. Instance Table

Instance Name	Physical Address
PBIST0	**0031 010Ch**
PBIST1	**3F10 010Ch**
PBIST2	**0333 010Ch**
PBIST3	**0331 010Ch**

Figure 14-8502. PBIST_A3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A3							
R/W							
0h							
7	6	5	4	3	2	1	0
A3							
R/W							
0h							

Table 14-25778. PBIST_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A3	R/W	0h	Variable Address Register 3 (A3) Reset Source: mod_g_rst_n

14.10.1.2.5 PBIST_L0 Register

1 PBIST_L0 Register (Offset = 110h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-25779. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0110h**
PBIST1	**3F10 0110h**
PBIST2	**0333 0110h**
PBIST3	**0331 0110h**

Figure 14-8503. PBIST_L0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L0							
R/W							
0h							
7	6	5	4	3	2	1	0
L0							
R/W							
0h							

Table 14-25781. PBIST_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L0	R/W	0h	Variable Loop Count Register 0 (L0) Reset Source: mod_g_rst_n

14.10.1.2.6 PBIST_L1 Register

1 PBIST_L1 Register (Offset = 114h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-25782. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0114h**
PBIST1	**3F10 0114h**
PBIST2	**0333 0114h**
PBIST3	**0331 0114h**

Figure 14-8504. PBIST_L1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L1							
R/W							
0h							
7	6	5	4	3	2	1	0
L1							
R/W							
0h							

Table 14-25784. PBIST_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L1	R/W	0h	Variable Loop Count Register 1 (L1) Reset Source: mod_g_rst_n

14.10.1.2.7 PBIST_L2 Register

1 PBIST_L2 Register (Offset = 118h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-25785. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0118h**
PBIST1	**3F10 0118h**
PBIST2	**0333 0118h**
PBIST3	**0331 0118h**

Figure 14-8505. PBIST_L2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">L2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">L2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25787. PBIST_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L2	R/W	0h	Variable Loop Count Register 2 (L2) Reset Source: mod_g_rst_n

14.10.1.2.8 PBIST_L3 Register

1 PBIST_L3 Register (Offset = 11Ch) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-25788. Instance Table

Instance Name	Physical Address
PBIST0	**0031 011Ch**
PBIST1	**3F10 011Ch**
PBIST2	**0333 011Ch**
PBIST3	**0331 011Ch**

Figure 14-8506. PBIST_L3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L3							
R/W							
0h							
7	6	5	4	3	2	1	0
L3							
R/W							
0h							

Table 14-25790. PBIST_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L3	R/W	0h	Variable Loop Count Register 3 (L3) Reset Source: mod_g_rst_n

14.10.1.2.9 PBIST_D Register

1 PBIST_D Register (Offset = 120h) [reset = 0h]

Data Registers

Return to Summary Table

Table 14-25791. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0120h**
PBIST1	**3F10 0120h**
PBIST2	**0333 0120h**
PBIST3	**0331 0120h**

Figure 14-8507. PBIST_D Name Register

31	30	29	28	27	26	25	24
D1							
R/W							
0h							

23	22	21	20	19	18	17	16
D1							
R/W							
0h							

15	14	13	12	11	10	9	8
D0							
R/W							
0h							

7	6	5	4	3	2	1	0
D0							
R/W							
0h							

Table 14-25793. PBIST_D Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	D1	R/W	0h	DD1 Data Register Upper 16 (D1) Reset Source: mod_g_rst_n
15:0	D0	R/W	0h	DD0 Data Register Lower 16 (D0) Reset Source: mod_g_rst_n

14.10.1.2.10 PBIST_E Register

1 PBIST_E Register (Offset = 124h) [reset = 0h]

Data Registers

Return to Summary Table

Table 14-25794. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0124h**
PBIST1	**3F10 0124h**
PBIST2	**0333 0124h**
PBIST3	**0331 0124h**

Figure 14-8508. PBIST_E Name Register

31	30	29	28	27	26	25	24
E1							
R/W							
0h							
23	22	21	20	19	18	17	16
E1							
R/W							
0h							
15	14	13	12	11	10	9	8
E0							
R/W							
0h							
7	6	5	4	3	2	1	0
E0							
R/W							
0h							

Table 14-25796. PBIST_E Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	E1	R/W	0h	EE1 Data Register Upper 16 (E1) Reset Source: mod_g_rst_n
15:0	E0	R/W	0h	EE0 Data Register Lower 16 (E0) Reset Source: mod_g_rst_n

14.10.1.2.11 PBIST_CA0 Register

1 PBIST_CA0 Register (Offset = 130h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-25797. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0130h**
PBIST1	**3F10 0130h**
PBIST2	**0333 0130h**
PBIST3	**0331 0130h**

Figure 14-8509. PBIST_CA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA0							
R/W							
0h							
7	6	5	4	3	2	1	0
CA0							
R/W							
0h							

Table 14-25799. PBIST_CA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA0	R/W	0h	Constant Address Register 0 (CA0) Reset Source: mod_g_rst_n

14.10.1.2.12 PBIST_CA1 Register

1 PBIST_CA1 Register (Offset = 134h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-25800. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0134h**
PBIST1	**3F10 0134h**
PBIST2	**0333 0134h**
PBIST3	**0331 0134h**

Figure 14-8510. PBIST_CA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA1							
R/W							
0h							
7	6	5	4	3	2	1	0
CA1							
R/W							
0h							

Table 14-25802. PBIST_CA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA1	R/W	0h	Constant Address Register 1 (CA1) Reset Source: mod_g_rst_n

14.10.1.2.13 PBIST_CA2 Register

1 PBIST_CA2 Register (Offset = 138h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-25803. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0138h**
PBIST1	**3F10 0138h**
PBIST2	**0333 0138h**
PBIST3	**0331 0138h**

Figure 14-8511. PBIST_CA2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA2							
R/W							
0h							
7	6	5	4	3	2	1	0
CA2							
R/W							
0h							

Table 14-25805. PBIST_CA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA2	R/W	0h	Constant Address Register 2 (CA2) Reset Source: mod_g_rst_n

14.10.1.2.14 PBIST_CA3 Register

1 PBIST_CA3 Register (Offset = 13Ch) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-25806. Instance Table

Instance Name	Physical Address
PBIST0	**0031 013Ch**
PBIST1	**3F10 013Ch**
PBIST2	**0333 013Ch**
PBIST3	**0331 013Ch**

Figure 14-8512. PBIST_CA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA3							
R/W							
0h							
7	6	5	4	3	2	1	0
CA3							
R/W							
0h							

Table 14-25808. PBIST_CA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA3	R/W	0h	Constant Address Register 3 (CA3) Reset Source: mod_g_rst_n

14.10.1.2.15 PBIST_CL0 Register

1 PBIST_CL0 Register (Offset = 140h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-25809. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0140h**
PBIST1	**3F10 0140h**
PBIST2	**0333 0140h**
PBIST3	**0331 0140h**

Figure 14-8513. PBIST_CL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL0							
R/W							
0h							
7	6	5	4	3	2	1	0
CL0							
R/W							
0h							

Table 14-25811. PBIST_CL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL0	R/W	0h	Constant Loop Count Register 0 (CL0) Reset Source: mod_g_rst_n

14.10.1.2.16 PBIST_CL1 Register

1 PBIST_CL1 Register (Offset = 144h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-25812. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0144h**
PBIST1	**3F10 0144h**
PBIST2	**0333 0144h**
PBIST3	**0331 0144h**

Figure 14-8514. PBIST_CL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL1							
R/W							
0h							
7	6	5	4	3	2	1	0
CL1							
R/W							
0h							

Table 14-25814. PBIST_CL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL1	R/W	0h	Constant Loop Count Register 1 (CL1) Reset Source: mod_g_rst_n

14.10.1.2.17 PBIST_CL2 Register

1 PBIST_CL2 Register (Offset = 148h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-25815. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0148h**
PBIST1	**3F10 0148h**
PBIST2	**0333 0148h**
PBIST3	**0331 0148h**

Figure 14-8515. PBIST_CL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CL2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CL2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25817. PBIST_CL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL2	R/W	0h	Constant Loop Count Register 2 (CL2) Reset Source: mod_g_rst_n

14.10.1.2.18 PBIST_CL3 Register

1 PBIST_CL3 Register (Offset = 14Ch) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-25818. Instance Table

Instance Name	Physical Address
PBIST0	**0031 014Ch**
PBIST1	**3F10 014Ch**
PBIST2	**0333 014Ch**
PBIST3	**0331 014Ch**

Figure 14-8516. PBIST_CL3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL3							
R/W							
0h							
7	6	5	4	3	2	1	0
CL3							
R/W							
0h							

Table 14-25820. PBIST_CL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL3	R/W	0h	Constant Loop Count Register 3 (CL3) Reset Source: mod_g_rst_n

14.10.1.2.19 PBIST_I0 Register

1 PBIST_I0 Register (Offset = 150h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-25821. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0150h**
PBIST1	**3F10 0150h**
PBIST2	**0333 0150h**
PBIST3	**0331 0150h**

Figure 14-8517. PBIST_I0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-25823. PBIST_I0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 0 (I0) Reset Source: mod_g_rst_n

14.10.1.2.20 PBIST_I1 Register

1 PBIST_I1 Register (Offset = 154h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-25824. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0154h**
PBIST1	**3F10 0154h**
PBIST2	**0333 0154h**
PBIST3	**0331 0154h**

Figure 14-8518. PBIST_I1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-25826. PBIST_I1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 1 (I1) Reset Source: mod_g_rst_n

14.10.1.2.21 PBIST_I2 Register

1 PBIST_I2 Register (Offset = 158h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-25827. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0158h**
PBIST1	**3F10 0158h**
PBIST2	**0333 0158h**
PBIST3	**0331 0158h**

Figure 14-8519. PBIST_I2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-25829. PBIST_I2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 2 (I2) Reset Source: mod_g_rst_n

14.10.1.2.22 PBIST_I3 Register

1 PBIST_I3 Register (Offset = 15Ch) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-25830. Instance Table

Instance Name	Physical Address
PBIST0	**0031 015Ch**
PBIST1	**3F10 015Ch**
PBIST2	**0333 015Ch**
PBIST3	**0331 015Ch**

Figure 14-8520. PBIST_I3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
I0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I0							
R/W							
0h							

Table 14-25832. PBIST_I3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 3 (I3) Reset Source: mod_g_rst_n

14.10.1.2.23 PBIST_RAMT Register

1 PBIST_RAMT Register (Offset = 160h) [reset = 0h]

RAM Configuration Register

Return to Summary Table

Table 14-25833. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0160h**
PBIST1	**3F10 0160h**
PBIST2	**0333 0160h**
PBIST3	**0331 0160h**

Figure 14-8521. PBIST_RAMT Name Register

31	30	29	28	27	26	25	24
RGS							
R/W							
0h							
23	22	21	20	19	18	17	16
RDS							
R/W							
0h							
15	14	13	12	11	10	9	8
DWR							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED		PLS				RLS	
NONE		R/W				R/W	
0h		0h				0h	

Table 14-25835. PBIST_RAMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RGS	R/W	0h	RAM Group Select RGS Reset Source: mod_g_rst_n
23:16	RDS	R/W	0h	Return Data select RDS Reset Source: mod_g_rst_n
15:8	DWR	R/W	0h	Data Width Register DWR Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:2	PLS	R/W	0h	Pipeline Latency Select Reset Source: mod_g_rst_n
1:0	RLS	R/W	0h	RAM Latency Select Reset Source: mod_g_rst_n

14.10.1.2.24 PBIST_DLR Register

1 PBIST_DLR Register (Offset = 164h) [reset = 208h]

Datalogger Register

Return to Summary Table

Table 14-25836. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0164h**
PBIST1	**3F10 0164h**
PBIST2	**0333 0164h**
PBIST3	**0331 0164h**

Figure 14-8522. PBIST_DLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
BRP							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					DLR1_RTM	DLR1_GNG	DLR1_MISR
NONE					R/W	R/W	R/W
0h					0h	1h	0h
7	6	5	4	3	2	1	0
DLR0_TSM	DLR0_CFMM	DLR0_ECAM	DLR0_CAM	DLR0_TCK	DLR0_ROM	DLR0_IDDQ	DLR0_DCM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	1h	0h	0h	0h

Table 14-25838. PBIST_DLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	BRP	R/W	0h	Datalogger 2 (BRP) Reset Source: mod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10	DLR1_RTM	R/W	0h	Retention testing mode Reset Source: mod_g_rst_n
9	DLR1_GNG	R/W	1h	GO / NO-GO testing mode Reset Source: mod_g_rst_n
8	DLR1_MISR	R/W	0h	MISR testing mode (mainly for ROM testing) Reset Source: mod_g_rst_n
7	DLR0_TSM	R/W	0h	Time stamp mode Reset Source: mod_g_rst_n
6	DLR0_CFMM	R/W	0h	Column Fail Masking mode Reset Source: mod_g_rst_n

Table 14-25838. PBIST_DLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DLR0_ECAM	R/W	0h	Emulation cache access mode Reset Source: mod_g_rst_n
4	DLR0_CAM	R/W	0h	Config access mode Reset Source: mod_g_rst_n
3	DLR0_TCK	R/W	1h	TCK Gated mode Reset Source: mod_g_rst_n
2	DLR0_ROM	R/W	0h	ROM-based testing mode Reset Source: mod_g_rst_n
1	DLR0_IDDQ	R/W	0h	IDDQ testing mode Reset Source: mod_g_rst_n
0	DLR0_DCM	R/W	0h	Distributed Compare mode Reset Source: mod_g_rst_n

14.10.1.2.25 PBIST_CMS Register

1 PBIST_CMS Register (Offset = 168h) [reset = 0h]

Clock-Mux Select Register

Return to Summary Table

Table 14-25839. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0168h**
PBIST1	**3F10 0168h**
PBIST2	**0333 0168h**
PBIST3	**0331 0168h**

Figure 14-8523. PBIST_CMS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMS			
NONE				R/W			
0h				0h			

Table 14-25841. PBIST_CMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CMS	R/W	0h	Clock Mux Select (CMS) Reset Source: mod_g_rst_n

14.10.1.2.26 PBIST_STR Register

1 PBIST_STR Register (Offset = 16Ch) [reset = 0h]

Program Control Register

Return to Summary Table

Table 14-25842. Instance Table

Instance Name	Physical Address
PBIST0	**0031 016Ch**
PBIST1	**3F10 016Ch**
PBIST2	**0333 016Ch**
PBIST3	**0331 016Ch**

Figure 14-8524. PBIST_STR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			CHK	STEP	STOP	RES	START
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-25844. PBIST_STR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	CHK	R/W	0h	Check MISR mode Reset Source: mod_g_rst_n
3	STEP	R/W	0h	Step / Step for emulation mode Reset Source: mod_g_rst_n
2	STOP	R/W	0h	Stop Reset Source: mod_g_rst_n
1	RES	R/W	0h	Resume / Emulation read Reset Source: mod_g_rst_n
0	START	R/W	0h	Start / Time Stamp mode restart Reset Source: mod_g_rst_n

14.10.1.2.27 PBIST_SCR Register

1 PBIST_SCR Register (Offset = 170h) [reset = FEDCBA9876542F40h]

Address Scrambling Register

Return to Summary Table

Table 14-25845. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0170h**
PBIST1	**3F10 0170h**
PBIST2	**0333 0170h**
PBIST3	**0331 0170h**

Figure 14-8525. PBIST_SCR Name Register

63	62	61	60	59	58	57	48
SCR7							
R/W							
FEh							
55	54	53	52	51	50	49	48
SCR6							
R/W							
DCh							
47	46	45	44	43	42	41	40
SCR5							
R/W							
BAh							
39	38	37	36	35	34	33	32
SCR4							
R/W							
98h							
15	14	13	12	11	10	9	8
SCR1							
R/W							
32h							
7	6	5	4	3	2	1	0
SCR0							
R/W							
10h							

Table 14-25847. PBIST_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
63:56	SCR7	R/W	FEh	Address Scrambling Register 7 Reset Source: mod_g_rst_n
55:48	SCR6	R/W	DCh	Address Scrambling Register 6 Reset Source: mod_g_rst_n
47:40	SCR5	R/W	BAh	Address Scrambling Register 5 Reset Source: mod_g_rst_n

Table 14-25847. PBIST_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39:32	SCR4	R/W	98h	Address Scrambling Register 4 Reset Source: mod_g_rst_n
31:24	SCR3	R/W	76h	Address Scrambling Register 3 Reset Source: mod_g_rst_n
23:16	SCR2	R/W	54h	Address Scrambling Register 2 Reset Source: mod_g_rst_n
15:8	SCR1	R/W	32h	Address Scrambling Register 1 Reset Source: mod_g_rst_n
7:0	SCR0	R/W	10h	Address Scrambling Register 0 Reset Source: mod_g_rst_n

14.10.1.2.28 PBIST_CSR Register

1 PBIST_CSR Register (Offset = 178h) [reset = 0h]

Chip Select Register

Return to Summary Table

Table 14-25848. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0178h**
PBIST1	**3F10 0178h**
PBIST2	**0333 0178h**
PBIST3	**0331 0178h**

Figure 14-8526. PBIST_CSR Name Register

31	30	29	28	27	26	25	24
CSR3							
R/W							
0h							
23	22	21	20	19	18	17	16
CSR2							
R/W							
0h							
15	14	13	12	11	10	9	8
CSR1							
R/W							
0h							
7	6	5	4	3	2	1	0
CSR0							
R/W							
0h							

Table 14-25850. PBIST_CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CSR3	R/W	0h	Chip Select 3 (CSR3) Reset Source: mod_g_rst_n
23:16	CSR2	R/W	0h	Chip Select 2 (CSR2) Reset Source: mod_g_rst_n
15:8	CSR1	R/W	0h	Chip Select 1(CSR1) Reset Source: mod_g_rst_n
7:0	CSR0	R/W	0h	Chip Select 0 (CSR0) Reset Source: mod_g_rst_n

14.10.1.2.29 PBIST_FDLY Register

1 PBIST_FDLY Register (Offset = 17Ch) [reset = 68h]

Fail Delay Register

Return to Summary Table

Table 14-25851. Instance Table

Instance Name	Physical Address
PBIST0	**0031 017Ch**
PBIST1	**3F10 017Ch**
PBIST2	**0333 017Ch**
PBIST3	**0331 017Ch**

Figure 14-8527. PBIST_FDLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FDLY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">68h</td></tr>
</table>

Table 14-25853. PBIST_FDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDLY	R/W	68h	Fail Delay (FDLY) Reset Source: mod_g_rst_n

14.10.1.2.30 PBIST_PACT Register

1 PBIST_PACT Register (Offset = 180h) [reset = 0h]

PACT Register

Return to Summary Table

Table 14-25854. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0180h**
PBIST1	**3F10 0180h**
PBIST2	**0333 0180h**
PBIST3	**0331 0180h**

Figure 14-8528. PBIST_PACT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PACT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-25856. PBIST_PACT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PACT	R/W	0h	PBIST Activate (PACT) Reset Source: mod_g_rst_n

14.10.1.2.31 PBIST_PID Register

1 PBIST_PID Register (Offset = 184h) [reset = 0h]

PBIST_ID Register

Return to Summary Table

Table 14-25857. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0184h**
PBIST1	**3F10 0184h**
PBIST2	**0333 0184h**
PBIST3	**0331 0184h**

Figure 14-8529. PBIST_PID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PID				
NONE			R/W				
0h			0h				

Table 14-25859. PBIST_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	PID	R/W	0h	PBIST ID Reset Source: mod_g_rst_n

14.10.1.2.32 PBIST_OVER Register

1 PBIST_OVER Register (Offset = 188h) [reset = 9h]

Override Register

Return to Summary Table

Table 14-25860. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0188h**
PBIST1	**3F10 0188h**
PBIST2	**0333 0188h**
PBIST3	**0331 0188h**

Figure 14-8530. PBIST_OVER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ALGO	MM	READ	RINFO
NONE				R/W	R/W	R/W	R/W
0h				1h	0h	0h	1h

Table 14-25862. PBIST_OVER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ALGO	R/W	1h	PBIST Override Algorithm Override Reset Source: mod_g_rst_n
2	MM	R/W	0h	PBIST Override Multiple Memory Reset Source: mod_g_rst_n
1	READ	R/W	0h	PBIST Override READ Override Reset Source: mod_g_rst_n
0	RINFO	R/W	1h	PBIST Override RINFO Override Reset Source: mod_g_rst_n

14.10.1.2.33 PBIST_FSRF Register

1 PBIST_FSRF Register (Offset = 190h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-25863. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0190h**
PBIST1	**3F10 0190h**
PBIST2	**0333 0190h**
PBIST3	**0331 0190h**

Figure 14-8531. PBIST_FSRF Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							FRSF1
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FRSF0
NONE							R
0h							0h

Table 14-25865. PBIST_FSRF Register Field Descriptions

Bit	Field	Type	Reset	Description
63:33	RESERVED	NONE	0h	Reserved
32	FRSF1	R	0h	Fail Status Fail - Port 1 (FSRF1) Reset Source: mod_g_rst_n
31:1	RESERVED	NONE	0h	Reserved
0	FRSF0	R	0h	Fail Status Fail - Port 0 (FSRF0) Reset Source: mod_g_rst_n

14.10.1.2.34 PBIST_FSRC Register

1 PBIST_FSRC Register (Offset = 198h) [reset = 0h]

Fail Status Count Register

Return to Summary Table

Table 14-25866. Instance Table

Instance Name	Physical Address
PBIST0	**0031 0198h**
PBIST1	**3F10 0198h**
PBIST2	**0333 0198h**
PBIST3	**0331 0198h**

Figure 14-8532. PBIST_FSRC Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FSRC1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FSRC0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-25868. PBIST_FSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
63:36	RESERVED	NONE	0h	Reserved
35:32	FSRC1	R	0h	Fail Status Count - Port 1 (FSRC1) Reset Source: mod_g_rst_n
31:4	RESERVED	NONE	0h	Reserved
3:0	FSRC0	R	0h	Fail Status Count - Port 0 (FSRC0) Reset Source: mod_g_rst_n

14.10.1.2.35 PBIST_FSRA Register

1 PBIST_FSRA Register (Offset = 1A0h) [reset = 0h]

Fail Status Address Register

Return to Summary Table

Table 14-25869. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01A0h**
PBIST1	**3F10 01A0h**
PBIST2	**0333 01A0h**
PBIST3	**0331 01A0h**

Figure 14-8533. PBIST_FSRA Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
FSRA1							
R							
0h							
39	38	37	36	35	34	33	32
FSRA1							
R							
0h							
15	14	13	12	11	10	9	8
FSRA0							
R							
0h							
7	6	5	4	3	2	1	0
FSRA0							
R							
0h							

Table 14-25871. PBIST_FSRA Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RESERVED	NONE	0h	Reserved
47:32	FSRA1	R	0h	Fail Status Address - Port 1 (FSRA1) Reset Source: mod_g_rst_n
31:16	RESERVED	NONE	0h	Reserved
15:0	FSRA0	R	0h	Fail Status Address - Port 0 (FSRA0) Reset Source: mod_g_rst_n

14.10.1.2.36 PBIST_FSRDL0 Register

1 PBIST_FSRDL0 Register (Offset = 1A8h) [reset = 0h]

Fail Status Data Registers

Return to Summary Table

Table 14-25872. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01A8h**
PBIST1	**3F10 01A8h**
PBIST2	**0333 01A8h**
PBIST3	**0331 01A8h**

Figure 14-8534. PBIST_FSRDL0 Name Register

31	30	29	28	27	26	25	24
FSRDL0							
R							
0h							
23	22	21	20	19	18	17	16
FSRDL0							
R							
0h							
15	14	13	12	11	10	9	8
FSRDL0							
R							
0h							
7	6	5	4	3	2	1	0
FSRDL0							
R							
0h							

Table 14-25874. PBIST_FSRDL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FSRDL0	R	0h	Fail Status Data - Port 0 (FSRDL0) Reset Source: mod_g_rst_n

14.10.1.2.37 PBIST_FSRDL1 Register

1 PBIST_FSRDL1 Register (Offset = 1B0h) [reset = 0h]

Fail Status Data Registers

Return to Summary Table

Table 14-25875. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01B0h**
PBIST1	**3F10 01B0h**
PBIST2	**0333 01B0h**
PBIST3	**0331 01B0h**

Figure 14-8535. PBIST_FSRDL1 Name Register

31	30	29	28	27	26	25	24
FSRDL1							
R							
0h							
23	22	21	20	19	18	17	16
FSRDL1							
R							
0h							
15	14	13	12	11	10	9	8
FSRDL1							
R							
0h							
7	6	5	4	3	2	1	0
FSRDL1							
R							
0h							

Table 14-25877. PBIST_FSRDL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FSRDL1	R	0h	Fail Status Data - Port 1 (FSRDL1) Reset Source: mod_g_rst_n

14.10.1.2.38 PBIST_MARGIN_MODE Register

1 PBIST_MARGIN_MODE Register (Offset = 1B4h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-25878. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01B4h**
PBIST1	**3F10 01B4h**
PBIST2	**0333 01B4h**
PBIST3	**0331 01B4h**

Figure 14-8536. PBIST_MARGIN_MODE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PBIST_DFT_READ		PBIST_DFT_WRITE	
NONE				R		R	
0h				0h		0h	

Table 14-25880. PBIST_MARGIN_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	PBIST_DFT_READ	R	0h	pbist_dft_read[1:0] Reset Source: mod_g_rst_n
1:0	PBIST_DFT_WRITE	R	0h	pbist_dft_write[1:0] Reset Source: mod_g_rst_n

14.10.1.2.39 PBIST_WRENZ Register

1 PBIST_WRENZ Register (Offset = 1B8h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-25881. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01B8h**
PBIST1	**3F10 01B8h**
PBIST2	**0333 01B8h**
PBIST3	**0331 01B8h**

Figure 14-8537. PBIST_WRENZ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WRENZ	
NONE						R	
0h						0h	

Table 14-25883. PBIST_WRENZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	WRENZ	R	0h	pbist_ram_wrenz[1:0] Reset Source: mod_g_rst_n

14.10.1.2.40 PBIST_PAGE_PGS Register

1 PBIST_PAGE_PGS Register (Offset = 1BCh) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-25884. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01BCh**
PBIST1	**3F10 01BCh**
PBIST2	**0333 01BCh**
PBIST3	**0331 01BCh**

Figure 14-8538. PBIST_PAGE_PGS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PGS	
NONE						R	
0h						0h	

Table 14-25886. PBIST_PAGE_PGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PGS	R	0h	pbist_ram_pgs[1:0] Reset Source: mod_g_rst_n

14.10.1.2.41 PBIST_ROM Register

1 PBIST_ROM Register (Offset = 1C0h) [reset = 3h]

ROM Mask Register

Return to Summary Table

Table 14-25887. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01C0h**
PBIST1	**3F10 01C0h**
PBIST2	**0333 01C0h**
PBIST3	**0331 01C0h**

Figure 14-8539. PBIST_ROM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ROM	
NONE						R/W	
0h						3h	

Table 14-25889. PBIST_ROM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ROM	R/W	3h	ROM Mask (ROM) Reset Source: mod_g_rst_n

14.10.1.2.42 PBIST_ALGO Register

1 PBIST_ALGO Register (Offset = 1C4h) [reset = FFFFFFFFh]

Algorithm Mask Register

Return to Summary Table

Table 14-25890. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01C4h**
PBIST1	**3F10 01C4h**
PBIST2	**0333 01C4h**
PBIST3	**0331 01C4h**

Figure 14-8540. PBIST_ALGO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ALGO_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ALGO_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ALGO_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ALGO_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
</table>

Table 14-25892. PBIST_ALGO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ALGO_3	R/W	FFh	ROM Algorithm Mask 3 (ALGO 3) Reset Source: mod_g_rst_n
23:16	ALGO_2	R/W	FFh	ROM Algorithm Mask 2 (ALGO 2) Reset Source: mod_g_rst_n
15:8	ALGO_1	R/W	FFh	ROM Algorithm Mask 1 (ALGO 1) Reset Source: mod_g_rst_n
7:0	ALGO_0	R/W	FFh	ROM Algorithm Mask 0 (ALGO 0) Reset Source: mod_g_rst_n

14.10.1.2.43 PBIST_RINFO Register

1 PBIST_RINFO Register (Offset = 1C8h) [reset = 1000000000000180h]

RAM Info Mask Register

Return to Summary Table

Table 14-25893. Instance Table

Instance Name	Physical Address
PBIST0	**0031 01C8h**
PBIST1	**3F10 01C8h**
PBIST2	**0333 01C8h**
PBIST3	**0331 01C8h**

Figure 14-8541. PBIST_RINFO Name Register

63	62	61	60	59	58	57	48
U3							
R/W							
FFh							
55	54	53	52	51	50	49	48
U2							
R/W							
FFh							
47	46	45	44	43	42	41	40
U1							
R/W							
FFh							
39	38	37	36	35	34	33	32
U0							
R/W							
FFh							
15	14	13	12	11	10	9	8
L1							
R/W							
FFh							
7	6	5	4	3	2	1	0
L0							
R/W							
FFh							

Table 14-25895. PBIST_RINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
63:56	U3	R/W	FFh	RAM Info Mask Upper 3 (RINFOU3) Reset Source: mod_g_rst_n
55:48	U2	R/W	FFh	RAM Info Mask Upper 2 (RINFOU2) Reset Source: mod_g_rst_n
47:40	U1	R/W	FFh	RAM Info Mask Upper 1 (RINFOU1) Reset Source: mod_g_rst_n

Table 14-25895. PBIST_RINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39:32	U0	R/W	FFh	RAM Info Mask Upper 0 (RINFOU0) Reset Source: mod_g_rst_n
31:24	L3	R/W	FFh	RAM Info Mask Lower 3 (RINFOL3) Reset Source: mod_g_rst_n
23:16	L2	R/W	FFh	RAM Info Mask Lower 2 (RINFOL2) Reset Source: mod_g_rst_n
15:8	L1	R/W	FFh	RAM Info Mask Lower 1 (RINFOL1) Reset Source: mod_g_rst_n
7:0	L0	R/W	FFh	RAM Info Mask Lower 0 (RINFOL0) Reset Source: mod_g_rst_n

14.11 On-Chip Debug Registers

14.11.1 debugss

debugss

14.11.1.1 debugss Summaries

debugss Summaries

Table 14-25896. DEBUGSS_SYS Registers, Base Address=4100 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	DEBUGSS_SYS_TRACE	4100 0000h

Table 14-25897. DEBUGSS_DEBUG_CELL_ROM_SLV Registers, Base Address=0007 3C02 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
4h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1	0007 3C02 0004h
8h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2	0007 3C02 0008h
Ch	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3	0007 3C02 000Ch
10h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4	0007 3C02 0010h
14h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5	0007 3C02 0014h
18h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6	0007 3C02 0018h
1Ch	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7	0007 3C02 001Ch
20h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8	0007 3C02 0020h
24h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9	0007 3C02 0024h
28h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10	0007 3C02 0028h
2Ch	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11	0007 3C02 002Ch
30h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12	0007 3C02 0030h
34h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13	0007 3C02 0034h
50h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14	0007 3C02 0050h
FD0h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4	0007 3C02 0FD0h
FD4h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5	0007 3C02 0FD4h
FD8h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6	0007 3C02 0FD8h
FDCh	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7	0007 3C02 0FDCh
FE0h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0	0007 3C02 0FE0h
FE4h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1	0007 3C02 0FE4h
FE8h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2	0007 3C02 0FE8h
FECh	32	DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3	0007 3C02 0FECh
FF0h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0	0007 3C02 0FF0h
FF4h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1	0007 3C02 0FF4h
FF8h	32	DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2	0007 3C02 0FF8h
FFCh	32	DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3	0007 3C02 0FFCh

Table 14-25898. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CTSET2_CFG_CTSETID	0007 3C02 2000h
10h	32	CTSET2_CFG_CTSETSYSCFG	0007 3C02 2010h
14h	32	CTSET2_CFG_SETSTR	0007 3C02 2014h

Table 14-25898. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
18h	32	CTSET2_CFG_DBGTIMELOW	0007 3C02 2018h
1Ch	32	CTSET2_CFG_DBGTIMEHI	0007 3C02 201Ch
24h	32	CTSET2_CFG_CTSETCFG	0007 3C02 2024h
28h	32	CTSET2_CFG_SETSPLREG	0007 3C02 2028h
30h	32	CTSET2_CFG_SETEVTENBL1	0007 3C02 2030h
34h	32	CTSET2_CFG_SETEVTENBL2	0007 3C02 2034h
38h	32	CTSET2_CFG_SETEVTENBL3	0007 3C02 2038h
3Ch	32	CTSET2_CFG_SETEVTENBL4	0007 3C02 203Ch
40h	32	CTSET2_CFG_SETEVTENBL5	0007 3C02 2040h
44h	32	CTSET2_CFG_SETEVTENBL6	0007 3C02 2044h
48h	32	CTSET2_CFG_SETEVTENBL7	0007 3C02 2048h
4Ch	32	CTSET2_CFG_SETEVTENBL8	0007 3C02 204Ch
50h	32	CTSET2_CFG_SETMSTID	0007 3C02 2050h
800h	32	CTSET2_CFG_CTCNTL	0007 3C02 2800h
804h	32	CTSET2_CFG_CTNUMDBG	0007 3C02 2804h
808h	32	CTSET2_CFG_CTUSERACCCTL	0007 3C02 2808h
820h	32	CTSET2_CFG_CTSTMCNTL	0007 3C02 2820h
824h	32	CTSET2_CFG_CTSTMMSTID	0007 3C02 2824h
828h	32	CTSET2_CFG_CTSTMINTVL	0007 3C02 2828h
82Ch	32	CTSET2_CFG_CTSTMSEL0	0007 3C02 282Ch
830h	32	CTSET2_CFG_CTSTMSEL1	0007 3C02 2830h
840h	32	CTSET2_CFG_CTINTVLR0	0007 3C02 2840h
844h	32	CTSET2_CFG_CTINTVLR1	0007 3C02 2844h
848h	32	CTSET2_CFG_CTINTVLR2	0007 3C02 2848h
84Ch	32	CTSET2_CFG_CTINTVLR3	0007 3C02 284Ch
850h	32	CTSET2_CFG_CTINTVLR4	0007 3C02 2850h
854h	32	CTSET2_CFG_CTINTVLR5	0007 3C02 2854h
858h	32	CTSET2_CFG_CTINTVLR6	0007 3C02 2858h
85Ch	32	CTSET2_CFG_CTINTVLR7	0007 3C02 285Ch
860h	32	CTSET2_CFG_CTINTVLR8	0007 3C02 2860h
864h	32	CTSET2_CFG_CTINTVLR9	0007 3C02 2864h
868h	32	CTSET2_CFG_CTINTVLR10	0007 3C02 2868h
86Ch	32	CTSET2_CFG_CTINTVLR11	0007 3C02 286Ch
870h	32	CTSET2_CFG_CTINTVLR12	0007 3C02 2870h
874h	32	CTSET2_CFG_CTINTVLR13	0007 3C02 2874h
878h	32	CTSET2_CFG_CTINTVLR14	0007 3C02 2878h
87Ch	32	CTSET2_CFG_CTINTVLR15	0007 3C02 287Ch
8A0h	32	CTSET2_CFG_CTDBGSGL0	0007 3C02 28A0h
8A4h	32	CTSET2_CFG_CTDBGSGL1	0007 3C02 28A4h
8A8h	32	CTSET2_CFG_CTDBGSGL2	0007 3C02 28A8h
8ACh	32	CTSET2_CFG_CTDBGSGL3	0007 3C02 28ACh
8B0h	32	CTSET2_CFG_CTDBGSGL4	0007 3C02 28B0h
8B4h	32	CTSET2_CFG_CTDBGSGL5	0007 3C02 28B4h
8B8h	32	CTSET2_CFG_CTDBGSGL6	0007 3C02 28B8h
8BCh	32	CTSET2_CFG_CTDBGSGL7	0007 3C02 28BCh

Table 14-25898. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
9F0h	32	CTSET2_CFG_CTGNBL0	0007 3C02 29F0h
9F4h	32	CTSET2_CFG_CTGNBL1	0007 3C02 29F4h
9F8h	32	CTSET2_CFG_CTGRST0	0007 3C02 29F8h
9FCh	32	CTSET2_CFG_CTGRST1	0007 3C02 29FCh
A00h	32	CTSET2_CFG_CTCR0	0007 3C02 2A00h
A04h	32	CTSET2_CFG_CTCR1	0007 3C02 2A04h
A08h	32	CTSET2_CFG_CTCR2	0007 3C02 2A08h
A0Ch	32	CTSET2_CFG_CTCR3	0007 3C02 2A0Ch
A10h	32	CTSET2_CFG_CTCR4	0007 3C02 2A10h
A14h	32	CTSET2_CFG_CTCR5	0007 3C02 2A14h
A18h	32	CTSET2_CFG_CTCR6	0007 3C02 2A18h
A1Ch	32	CTSET2_CFG_CTCR7	0007 3C02 2A1Ch
A20h	32	CTSET2_CFG_CTCR8	0007 3C02 2A20h
A24h	32	CTSET2_CFG_CTCR9	0007 3C02 2A24h
A28h	32	CTSET2_CFG_CTCR10	0007 3C02 2A28h
A2Ch	32	CTSET2_CFG_CTCR11	0007 3C02 2A2Ch
A30h	32	CTSET2_CFG_CTCR12	0007 3C02 2A30h
A34h	32	CTSET2_CFG_CTCR13	0007 3C02 2A34h
A38h	32	CTSET2_CFG_CTCR14	0007 3C02 2A38h
A3Ch	32	CTSET2_CFG_CTCR15	0007 3C02 2A3Ch
A40h	32	CTSET2_CFG_CTCR16	0007 3C02 2A40h
A44h	32	CTSET2_CFG_CTCR17	0007 3C02 2A44h
A48h	32	CTSET2_CFG_CTCR18	0007 3C02 2A48h
A4Ch	32	CTSET2_CFG_CTCR19	0007 3C02 2A4Ch
A50h	32	CTSET2_CFG_CTCR20	0007 3C02 2A50h
A54h	32	CTSET2_CFG_CTCR21	0007 3C02 2A54h
A58h	32	CTSET2_CFG_CTCR22	0007 3C02 2A58h
A5Ch	32	CTSET2_CFG_CTCR23	0007 3C02 2A5Ch
A60h	32	CTSET2_CFG_CTCR24	0007 3C02 2A60h
A64h	32	CTSET2_CFG_CTCR25	0007 3C02 2A64h
A68h	32	CTSET2_CFG_CTCR26	0007 3C02 2A68h
A6Ch	32	CTSET2_CFG_CTCR27	0007 3C02 2A6Ch
A70h	32	CTSET2_CFG_CTCR28	0007 3C02 2A70h
A74h	32	CTSET2_CFG_CTCR29	0007 3C02 2A74h
A78h	32	CTSET2_CFG_CTCR30	0007 3C02 2A78h
A7Ch	32	CTSET2_CFG_CTCR31	0007 3C02 2A7Ch
A80h	32	CTSET2_CFG_CTOWN0	0007 3C02 2A80h
A84h	32	CTSET2_CFG_CTOWN1	0007 3C02 2A84h
A88h	32	CTSET2_CFG_CTOWN2	0007 3C02 2A88h
A8Ch	32	CTSET2_CFG_CTOWN3	0007 3C02 2A8Ch
A90h	32	CTSET2_CFG_CTOWN4	0007 3C02 2A90h
A94h	32	CTSET2_CFG_CTOWN5	0007 3C02 2A94h
A98h	32	CTSET2_CFG_CTOWN6	0007 3C02 2A98h
A9Ch	32	CTSET2_CFG_CTOWN7	0007 3C02 2A9Ch
AA0h	32	CTSET2_CFG_CTOWN8	0007 3C02 2AA0h

Table 14-25898. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
AA4h	32	CTSET2_CFG_CTOWN9	0007 3C02 2AA4h
AA8h	32	CTSET2_CFG_CTOWN10	0007 3C02 2AA8h
AACh	32	CTSET2_CFG_CTOWN11	0007 3C02 2AACh
AB0h	32	CTSET2_CFG_CTOWN12	0007 3C02 2AB0h
AB4h	32	CTSET2_CFG_CTOWN13	0007 3C02 2AB4h
AB8h	32	CTSET2_CFG_CTOWN14	0007 3C02 2AB8h
ABCh	32	CTSET2_CFG_CTOWN15	0007 3C02 2ABCh
AC0h	32	CTSET2_CFG_CTOWN16	0007 3C02 2AC0h
AC4h	32	CTSET2_CFG_CTOWN17	0007 3C02 2AC4h
AC8h	32	CTSET2_CFG_CTOWN18	0007 3C02 2AC8h
ACCh	32	CTSET2_CFG_CTOWN19	0007 3C02 2ACCh
AD0h	32	CTSET2_CFG_CTOWN20	0007 3C02 2AD0h
AD4h	32	CTSET2_CFG_CTOWN21	0007 3C02 2AD4h
AD8h	32	CTSET2_CFG_CTOWN22	0007 3C02 2AD8h
ADCh	32	CTSET2_CFG_CTOWN23	0007 3C02 2ADCh
AE0h	32	CTSET2_CFG_CTOWN24	0007 3C02 2AE0h
AE4h	32	CTSET2_CFG_CTOWN25	0007 3C02 2AE4h
AE8h	32	CTSET2_CFG_CTOWN26	0007 3C02 2AE8h
AECh	32	CTSET2_CFG_CTOWN27	0007 3C02 2AECh
AF0h	32	CTSET2_CFG_CTOWN28	0007 3C02 2AF0h
AF4h	32	CTSET2_CFG_CTOWN29	0007 3C02 2AF4h
AF8h	32	CTSET2_CFG_CTOWN30	0007 3C02 2AF8h
AFCh	32	CTSET2_CFG_CTOWN31	0007 3C02 2AFCh
B00h	32	CTSET2_CFG_CTFILT0	0007 3C02 2B00h
B04h	32	CTSET2_CFG_CTFILT1	0007 3C02 2B04h
B08h	32	CTSET2_CFG_CTFILT2	0007 3C02 2B08h
B0Ch	32	CTSET2_CFG_CTFILT3	0007 3C02 2B0Ch
B10h	32	CTSET2_CFG_CTFILT4	0007 3C02 2B10h
B14h	32	CTSET2_CFG_CTFILT5	0007 3C02 2B14h
B18h	32	CTSET2_CFG_CTFILT6	0007 3C02 2B18h
B1Ch	32	CTSET2_CFG_CTFILT7	0007 3C02 2B1Ch
B20h	32	CTSET2_CFG_CTFILT8	0007 3C02 2B20h
B24h	32	CTSET2_CFG_CTFILT9	0007 3C02 2B24h
B28h	32	CTSET2_CFG_CTFILT10	0007 3C02 2B28h
B2Ch	32	CTSET2_CFG_CTFILT11	0007 3C02 2B2Ch
B30h	32	CTSET2_CFG_CTFILT12	0007 3C02 2B30h
B34h	32	CTSET2_CFG_CTFILT13	0007 3C02 2B34h
B38h	32	CTSET2_CFG_CTFILT14	0007 3C02 2B38h
B3Ch	32	CTSET2_CFG_CTFILT15	0007 3C02 2B3Ch
B40h	32	CTSET2_CFG_CTFILT16	0007 3C02 2B40h
B44h	32	CTSET2_CFG_CTFILT17	0007 3C02 2B44h
B48h	32	CTSET2_CFG_CTFILT18	0007 3C02 2B48h
B4Ch	32	CTSET2_CFG_CTFILT19	0007 3C02 2B4Ch
B50h	32	CTSET2_CFG_CTFILT20	0007 3C02 2B50h
B54h	32	CTSET2_CFG_CTFILT21	0007 3C02 2B54h

Table 14-25898. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
B58h	32	CTSET2_CFG_CTFILT22	0007 3C02 2B58h
B5Ch	32	CTSET2_CFG_CTFILT23	0007 3C02 2B5Ch
B60h	32	CTSET2_CFG_CTFILT24	0007 3C02 2B60h
B64h	32	CTSET2_CFG_CTFILT25	0007 3C02 2B64h
B68h	32	CTSET2_CFG_CTFILT26	0007 3C02 2B68h
B6Ch	32	CTSET2_CFG_CTFILT27	0007 3C02 2B6Ch
B70h	32	CTSET2_CFG_CTFILT28	0007 3C02 2B70h
B74h	32	CTSET2_CFG_CTFILT29	0007 3C02 2B74h
B78h	32	CTSET2_CFG_CTFILT30	0007 3C02 2B78h
B7Ch	32	CTSET2_CFG_CTFILT31	0007 3C02 2B7Ch
B80h	32	CTSET2_CFG_CTCNTR0	0007 3C02 2B80h
B84h	32	CTSET2_CFG_CTCNTR1	0007 3C02 2B84h
B88h	32	CTSET2_CFG_CTCNTR2	0007 3C02 2B88h
B8Ch	32	CTSET2_CFG_CTCNTR3	0007 3C02 2B8Ch
B90h	32	CTSET2_CFG_CTCNTR4	0007 3C02 2B90h
B94h	32	CTSET2_CFG_CTCNTR5	0007 3C02 2B94h
B98h	32	CTSET2_CFG_CTCNTR6	0007 3C02 2B98h
B9Ch	32	CTSET2_CFG_CTCNTR7	0007 3C02 2B9Ch
BA0h	32	CTSET2_CFG_CTCNTR8	0007 3C02 2BA0h
BA4h	32	CTSET2_CFG_CTCNTR9	0007 3C02 2BA4h
BA8h	32	CTSET2_CFG_CTCNTR10	0007 3C02 2BA8h
BACh	32	CTSET2_CFG_CTCNTR11	0007 3C02 2BACh
BB0h	32	CTSET2_CFG_CTCNTR12	0007 3C02 2BB0h
BB4h	32	CTSET2_CFG_CTCNTR13	0007 3C02 2BB4h
BB8h	32	CTSET2_CFG_CTCNTR14	0007 3C02 2BB8h
BBCh	32	CTSET2_CFG_CTCNTR15	0007 3C02 2BBCh
BC0h	32	CTSET2_CFG_CTCNTR16	0007 3C02 2BC0h
BC4h	32	CTSET2_CFG_CTCNTR17	0007 3C02 2BC4h
BC8h	32	CTSET2_CFG_CTCNTR18	0007 3C02 2BC8h
BCCh	32	CTSET2_CFG_CTCNTR19	0007 3C02 2BCCh
BD0h	32	CTSET2_CFG_CTCNTR20	0007 3C02 2BD0h
BD4h	32	CTSET2_CFG_CTCNTR21	0007 3C02 2BD4h
BD8h	32	CTSET2_CFG_CTCNTR22	0007 3C02 2BD8h
BDCh	32	CTSET2_CFG_CTCNTR23	0007 3C02 2BDCh
BE0h	32	CTSET2_CFG_CTCNTR24	0007 3C02 2BE0h
BE4h	32	CTSET2_CFG_CTCNTR25	0007 3C02 2BE4h
BE8h	32	CTSET2_CFG_CTCNTR26	0007 3C02 2BE8h
BECh	32	CTSET2_CFG_CTCNTR27	0007 3C02 2BECh
BF0h	32	CTSET2_CFG_CTCNTR28	0007 3C02 2BF0h
BF4h	32	CTSET2_CFG_CTCNTR29	0007 3C02 2BF4h
BF8h	32	CTSET2_CFG_CTCNTR30	0007 3C02 2BF8h
BFCh	32	CTSET2_CFG_CTCNTR31	0007 3C02 2BFCh
C00h	32	CTSET2_CFG_CT_EOI	0007 3C02 2C00h
C04h	32	CTSET2_CFG_CTIRQSTAT_RAW	0007 3C02 2C04h
C08h	32	CTSET2_CFG_CTIRQSTAT	0007 3C02 2C08h

Table 14-25898. CTSET2_CFG Registers, Base Address=0007 3C02 2000h, Length=8192 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
C0Ch	32	CTSET2_CFG_CTIRQENABLE_SET	0007 3C02 2C0Ch
C10h	32	CTSET2_CFG_CTIRQENABLE_CLR	0007 3C02 2C10h
1800h	32	CTSET2_CFG_STPTCR	0007 3C02 3800h
1804h	32	CTSET2_CFG_STPTID	0007 3C02 3804h
1810h	32	CTSET2_CFG_STPASYNC	0007 3C02 3810h
1814h	32	CTSET2_CFG_STPFFCR	0007 3C02 3814h
1818h	32	CTSET2_CFG_STPFEAT1	0007 3C02 3818h

Table 14-25899. CXATBREPLICATOR_CFG Registers, Base Address=0007 3C02 4000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CXATBREPLICATOR_CFG_IDFILTER0	0007 3C02 4000h
4h	32	CXATBREPLICATOR_CFG_IDFILTER1	0007 3C02 4004h
EF8h	32	CXATBREPLICATOR_CFG_ITATBCTR1	0007 3C02 4EF8h
EFCh	32	CXATBREPLICATOR_CFG_ITATBCTR0	0007 3C02 4EFCh
F00h	32	CXATBREPLICATOR_CFG_ITCTRL	0007 3C02 4F00h
FA0h	32	CXATBREPLICATOR_CFG_CLAIMSET	0007 3C02 4FA0h
FA4h	32	CXATBREPLICATOR_CFG_CLAIMCLR	0007 3C02 4FA4h
FB0h	32	CXATBREPLICATOR_CFG_LAR	0007 3C02 4FB0h
FB4h	32	CXATBREPLICATOR_CFG_LSR	0007 3C02 4FB4h
FB8h	32	CXATBREPLICATOR_CFG_AUTHSTATUS	0007 3C02 4FB8h
FC8h	32	CXATBREPLICATOR_CFG_DEVID	0007 3C02 4FC8h
FCCh	32	CXATBREPLICATOR_CFG_DEVTYPE	0007 3C02 4FCCh
FD0h	32	CXATBREPLICATOR_CFG_PIDR4	0007 3C02 4FD0h
FE0h	32	CXATBREPLICATOR_CFG_PIDR0	0007 3C02 4FE0h
FE4h	32	CXATBREPLICATOR_CFG_PIDR1	0007 3C02 4FE4h
FE8h	32	CXATBREPLICATOR_CFG_PIDR2	0007 3C02 4FE8h
FECh	32	CXATBREPLICATOR_CFG_PIDR3	0007 3C02 4FECh
FF0h	32	CXATBREPLICATOR_CFG_CIDR0	0007 3C02 4FF0h
FF4h	32	CXATBREPLICATOR_CFG_CIDR1	0007 3C02 4FF4h
FF8h	32	CXATBREPLICATOR_CFG_CIDR2	0007 3C02 4FF8h
FFCh	32	CXATBREPLICATOR_CFG_CIDR3	0007 3C02 4FFCh

Table 14-25900. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG Registers, Base Address=0007 3C02 5000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
4h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_RAMSZ	0007 3C02 5004h
8h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_FIFOSZ	0007 3C02 5008h
Ch	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_STAT	0007 3C02 500Ch
10h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRDAT	0007 3C02 5010h
14h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRPTR	0007 3C02 5014h

Table 14-25900. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG Registers, Base Address=0007 3C02 5000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
18h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWPTR	0007 3C02 5018h
1Ch	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TRGCNT	0007 3C02 501Ch
20h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TBR_CTRL	0007 3C02 5020h
24h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWDAT	0007 3C02 5024h
100h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OUTLVL	0007 3C02 5100h
104h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_SICTRL	0007 3C02 5104h
108h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IDPERIOD	0007 3C02 5108h
10Ch	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_SEQCNTL	0007 3C02 510Ch
120h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_EOI	0007 3C02 5120h
124h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS_RAW	0007 3C02 5124h
128h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS	0007 3C02 5128h
12Ch	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_SET	0007 3C02 512Ch
130h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_CLR	0007 3C02 5130h
300h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPSTAT	0007 3C02 5300h
304h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPCTRL	0007 3C02 5304h
FA0h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMSET	0007 3C02 5FA0h
FA4h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMCLR	0007 3C02 5FA4h
FB0h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKACC	0007 3C02 5FB0h
FB4h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKSTAT	0007 3C02 5FB4h
FB8h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_AUTHSTAT	0007 3C02 5FB8h
FC8h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVID	0007 3C02 5FC8h
FCCh	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVTYPE	0007 3C02 5FCCh
FD0h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID4	0007 3C02 5FD0h
FD4h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID5	0007 3C02 5FD4h
FD8h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID6	0007 3C02 5FD8h
FDCh	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID7	0007 3C02 5FDCh

Table 14-25900. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG Registers, Base Address=0007 3C02 5000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FE0h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID0	0007 3C02 5FE0h
FE4h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID1	0007 3C02 5FE4h
FE8h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID2	0007 3C02 5FE8h
FECh	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID3	0007 3C02 5FECh
FF0h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID0	0007 3C02 5FF0h
FF4h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID1	0007 3C02 5FF4h
FF8h	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID2	0007 3C02 5FF8h
FFCh	32	DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID3	0007 3C02 5FFCh

Table 14-25901. CSCTI_CFG Registers, Base Address=0007 3C02 6000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 6000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 6010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 6014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 6018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 601Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 6020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 6024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 6028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 602Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 6030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 6034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 6038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 603Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 60A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 60A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 60A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 60ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 60B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 60B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 60B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 60BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 6130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 6134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 6138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 613Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 6140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 6144h

Table 14-25901. CSCTI_CFG Registers, Base Address=0007 3C02 6000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 6EDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 6EE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 6EE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 6EE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 6EECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 6EF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 6EF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 6EF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 6F00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 6FA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 6FA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 6FB0h
FB4h	32	CSCTI_CFG_LSR	0007 3C02 6FB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 6FB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 6FC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 6FCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 6FD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 6FE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 6FE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 6FE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 6FECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 6FF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 6FF4h
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 6FF8h
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 6FFCh

Table 14-25902. CSCTI_CFG Registers, Base Address=0007 3C02 8000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 8000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 8010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 8014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 8018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 801Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 8020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 8024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 8028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 802Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 8030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 8034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 8038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 803Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 80A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 80A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 80A8h

Table 14-25902. CSCTI_CFG Registers, Base Address=0007 3C02 8000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 80ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 80B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 80B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 80B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 80BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 8130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 8134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 8138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 813Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 8140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 8144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 8EDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 8EE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 8EE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 8EE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 8EECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 8EF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 8EF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 8EF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 8F00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 8FA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 8FA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 8FB0h
FB4h	32	CSCTI_CFG_LSR	0007 3C02 8FB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 8FB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 8FC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 8FCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 8FD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 8FE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 8FE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 8FE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 8FECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 8FF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 8FF4h
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 8FF8h
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 8FFCh

Table 14-25903. CSCTI_CFG Registers, Base Address=0007 3C02 9000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 9000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 9010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 9014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 9018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 901Ch

Table 14-25903. CSCTI_CFG Registers, Base Address=0007 3C02 9000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 9020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 9024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 9028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 902Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 9030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 9034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 9038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 903Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 90A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 90A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 90A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 90ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 90B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 90B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 90B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 90BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 9130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 9134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 9138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 913Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 9140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 9144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 9EDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 9EE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 9EE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 9EE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 9EECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 9EF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 9EF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 9EF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 9F00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 9FA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 9FA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 9FB0h
FB4h	32	CSCTI_CFG_LSR	0007 3C02 9FB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 9FB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 9FC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 9FCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 9FD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 9FE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 9FE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 9FE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 9FECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 9FF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 9FF4h

Table 14-25903. CSCTI_CFG Registers, Base Address=0007 3C02 9000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 9FF8h
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 9FFCh

Table 14-25904. CSCTI_CFG Registers, Base Address=0007 3C02 A000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 A000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 A010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 A014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 A018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 A01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 A020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 A024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 A028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 A02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 A030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 A034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 A038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 A03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 A0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 A0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 A0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 A0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 A0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 A0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 A0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 A0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 A130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 A134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 A138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 A13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 A140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 A144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 AEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 AEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 AEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 AEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 AEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 AEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 AEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 AEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 AF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 AFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 AFA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 AFB0h

Table 14-25904. CSCTI_CFG Registers, Base Address=0007 3C02 A000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FB4h	32	CSCTI_CFG_LSR	0007 3C02 AFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 AFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 AFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 AFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 AFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 AFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 AFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 AFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 AFECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 AFF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 AFF4h
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 AFF8h
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 AFFCh

Table 14-25905. CSCTI_CFG Registers, Base Address=0007 3C02 B000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 B000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 B010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 B014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 B018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 B01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 B020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 B024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 B028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 B02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 B030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 B034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 B038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 B03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 B0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 B0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 B0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 B0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 B0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 B0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 B0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 B0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 B130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 B134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 B138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 B13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 B140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 B144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 BEDCh

Table 14-25905. CSCTI_CFG Registers, Base Address=0007 3C02 B000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 BEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 BEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 BEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 BEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 BEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 BEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 BEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 BF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 BFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 BFA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 BFB0h
FB4h	32	CSCTI_CFG_LSR	0007 3C02 BFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 BFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 BFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 BFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 BFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 BFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 BFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 BFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 BFECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 BFF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 BFF4h
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 BFF8h
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 BFFCh

Table 14-25906. CSCTI_CFG Registers, Base Address=0007 3C02 C000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 C000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 C010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 C014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 C018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 C01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 C020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 C024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 C028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 C02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 C030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 C034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 C038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 C03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 C0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 C0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 C0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 C0ACh

Table 14-25906. CSCTI_CFG Registers, Base Address=0007 3C02 C000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 C0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 C0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 C0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 C0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 C130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 C134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 C138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 C13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 C140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 C144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 CEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 CEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 CEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 CEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 CEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 CEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 CEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 CEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 CF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 CFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 CFA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 CFB0h
FB4h	32	CSCTI_CFG_LSR	0007 3C02 CFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 CFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 CFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 CFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 CFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 CFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 CFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 CFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 CFECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 CFF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 CFF4h
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 CFF8h
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 CFFCh

Table 14-25907. CSCTI_CFG Registers, Base Address=0007 3C02 D000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 D000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 D010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 D014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 D018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 D01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 D020h

Table 14-25907. CSCTI_CFG Registers, Base Address=0007 3C02 D000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 D024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 D028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 D02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 D030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 D034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 D038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 D03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 D0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 D0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 D0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 D0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 D0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 D0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 D0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 D0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 D130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 D134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 D138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 D13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 D140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 D144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 DEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 DEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 DEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 DEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 DEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 DEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 DEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 DEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 DF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 DFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 DFA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 DFB0h
FB4h	32	CSCTI_CFG_LSR	0007 3C02 DFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 DFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 DFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 DFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 DFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 DFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 DFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 DFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 DFECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 DFF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 DFF4h
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 DFF8h

Table 14-25907. CSCTI_CFG Registers, Base Address=0007 3C02 D000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 DFFCh

Table 14-25908. CSCTI_CFG Registers, Base Address=0007 3C02 E000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 E000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 E010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 E014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 E018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 E01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 E020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 E024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 E028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 E02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 E030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 E034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 E038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 E03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 E0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 E0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 E0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 E0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 E0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 E0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 E0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 E0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 E130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 E134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 E138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 E13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 E140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 E144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 EEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 EEE0h
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 EEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 EEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 EEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 EEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 EEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 EEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 EF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 EFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 EFA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 EFB0h
FB4h	32	CSCTI_CFG_LSR	0007 3C02 EFB4h

Table 14-25908. CSCTI_CFG Registers, Base Address=0007 3C02 E000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 EFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 EFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 EFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 EFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 EFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 EFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 EFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 EFECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 EFF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 EFF4h
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 EFF8h
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 EFFCh

Table 14-25909. CSCTI_CFG Registers, Base Address=0007 3C02 F000h, Length=4096

Offset	Length	Register Name	DEBUGSS0 Physical Address
0h	32	CSCTI_CFG_CTICONTROL	0007 3C02 F000h
10h	32	CSCTI_CFG_CTIINTACK	0007 3C02 F010h
14h	32	CSCTI_CFG_CTIAPPSET	0007 3C02 F014h
18h	32	CSCTI_CFG_CTIAPPCLEAR	0007 3C02 F018h
1Ch	32	CSCTI_CFG_CTIAPPPULSE	0007 3C02 F01Ch
20h	32	CSCTI_CFG_CTIINEN0	0007 3C02 F020h
24h	32	CSCTI_CFG_CTIINEN1	0007 3C02 F024h
28h	32	CSCTI_CFG_CTIINEN2	0007 3C02 F028h
2Ch	32	CSCTI_CFG_CTIINEN3	0007 3C02 F02Ch
30h	32	CSCTI_CFG_CTIINEN4	0007 3C02 F030h
34h	32	CSCTI_CFG_CTIINEN5	0007 3C02 F034h
38h	32	CSCTI_CFG_CTIINEN6	0007 3C02 F038h
3Ch	32	CSCTI_CFG_CTIINEN7	0007 3C02 F03Ch
A0h	32	CSCTI_CFG_CTIOUTEN0	0007 3C02 F0A0h
A4h	32	CSCTI_CFG_CTIOUTEN1	0007 3C02 F0A4h
A8h	32	CSCTI_CFG_CTIOUTEN2	0007 3C02 F0A8h
ACh	32	CSCTI_CFG_CTIOUTEN3	0007 3C02 F0ACh
B0h	32	CSCTI_CFG_CTIOUTEN4	0007 3C02 F0B0h
B4h	32	CSCTI_CFG_CTIOUTEN5	0007 3C02 F0B4h
B8h	32	CSCTI_CFG_CTIOUTEN6	0007 3C02 F0B8h
BCh	32	CSCTI_CFG_CTIOUTEN7	0007 3C02 F0BCh
130h	32	CSCTI_CFG_CTITRIGINSTATUS	0007 3C02 F130h
134h	32	CSCTI_CFG_CTITRIGOUTSTATUS	0007 3C02 F134h
138h	32	CSCTI_CFG_CTICHINSTATUS	0007 3C02 F138h
13Ch	32	CSCTI_CFG_CTICHOUTSTATUS	0007 3C02 F13Ch
140h	32	CSCTI_CFG_CTIGATE	0007 3C02 F140h
144h	32	CSCTI_CFG_ASICCTL	0007 3C02 F144h
EDCh	32	CSCTI_CFG_ITCHINACK	0007 3C02 FEDCh
EE0h	32	CSCTI_CFG_ITTRIGINACK	0007 3C02 FEE0h

Table 14-25909. CSCTI_CFG Registers, Base Address=0007 3C02 F000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS0 Physical Address
EE4h	32	CSCTI_CFG_ITCHOUT	0007 3C02 FEE4h
EE8h	32	CSCTI_CFG_ITTRIGOUT	0007 3C02 FEE8h
EECh	32	CSCTI_CFG_ITCHOUTACK	0007 3C02 FEECh
EF0h	32	CSCTI_CFG_ITTRIGOUTACK	0007 3C02 FEF0h
EF4h	32	CSCTI_CFG_ITCHIN	0007 3C02 FEF4h
EF8h	32	CSCTI_CFG_ITTRIGIN	0007 3C02 FEF8h
F00h	32	CSCTI_CFG_ITCTRL	0007 3C02 FF00h
FA0h	32	CSCTI_CFG_CLAIMSET	0007 3C02 FFA0h
FA4h	32	CSCTI_CFG_CLAIMCLR	0007 3C02 FFA4h
FB0h	32	CSCTI_CFG_LAR	0007 3C02 FFB0h
FB4h	32	CSCTI_CFG_LSR	0007 3C02 FFB4h
FB8h	32	CSCTI_CFG_AUTHSTATUS	0007 3C02 FFB8h
FC8h	32	CSCTI_CFG_DEVID	0007 3C02 FFC8h
FCCh	32	CSCTI_CFG_DEVTYPE	0007 3C02 FFCCh
FD0h	32	CSCTI_CFG_PERIPHID4	0007 3C02 FFD0h
FE0h	32	CSCTI_CFG_PERIPHID0	0007 3C02 FFE0h
FE4h	32	CSCTI_CFG_PERIPHID1	0007 3C02 FFE4h
FE8h	32	CSCTI_CFG_PERIPHID2	0007 3C02 FFE8h
FECh	32	CSCTI_CFG_PERIPHID3	0007 3C02 FFECh
FF0h	32	CSCTI_CFG_COMPID0	0007 3C02 FFF0h
FF4h	32	CSCTI_CFG_COMPID1	0007 3C02 FFF4h
FF8h	32	CSCTI_CFG_COMPID2	0007 3C02 FFF8h
FFCh	32	CSCTI_CFG_COMPID3	0007 3C02 FFFCh

14.11.1.2 debugss Registers

debugss Registers

14.11.1.2.1 DEBUGSS_SYS_TRACE Register

1 DEBUGSS_SYS_TRACE Register (Offset = 0h) [reset = 0h]

This register contains TBR trace read data

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Table 14-25910. Instance Table

Instance Name	Physical Address
DEBUGSS0	**4100 0000h**

Figure 14-8542. DEBUGSS_SYS_TRACE Name Register

31	30	29	28	27	26	25	24
DATA							
R							
0h							
23	22	21	20	19	18	17	16
DATA							
R							
0h							
15	14	13	12	11	10	9	8
DATA							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-25912. DEBUGSS_SYS_TRACE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R	0h	TBR TRACE data

14.11.1.2.2 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1 Register (Offset = 4h) [reset = 2002h]

rom table entry 1

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Table 14-25913. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0004h**

Figure 14-8543. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1001h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1001h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1001h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">ID</td><td>PRESENT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">1001h</td><td>0h</td></tr>
</table>

Table 14-25915. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	1001h	4kB - MSMCv3 CSCTI Instance 1 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.3 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2 Register (Offset = 8h) [reset = 4002h]

rom table entry 2

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Table 14-25916. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0008h**

Figure 14-8544. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2001h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2001h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2001h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">ID</td><td>PRESENT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">2001h</td><td>0h</td></tr>
</table>

Table 14-25918. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	2001h	4kB - MSMCv3 CSCTI Instance 2 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.4 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3 Register (Offset = Ch) [reset = 5002h]

rom table entry 3

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Table 14-25919. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 000Ch**

Figure 14-8545. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3 Name Register

31	30	29	28	27	26	25	24
ID							
R							
2801h							
23	22	21	20	19	18	17	16
ID							
R							
2801h							
15	14	13	12	11	10	9	8
ID							
R							
2801h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
2801h							0h

Table 14-25921. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	2801h	4kB - MSMCv3 CSCTI Instance 3 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.5 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4 Register (Offset = 10h) [reset = 6002h]

rom table entry 4

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Table 14-25922. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 0010h**

Figure 14-8546. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3001h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3001h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3001h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">ID</td><td>PRESENT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">3001h</td><td>0h</td></tr>
</table>

Table 14-25924. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	3001h	4kB - MSMCv3 CSCTI Instance 4 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.6 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5 Register (Offset = 14h) [reset = 7002h]

rom table entry 5

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Table 14-25925. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0014h**

Figure 14-8547. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5 Name Register

31	30	29	28	27	26	25	24
ID							
R							
3801h							
23	22	21	20	19	18	17	16
ID							
R							
3801h							
15	14	13	12	11	10	9	8
ID							
R							
3801h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
3801h							0h

Table 14-25927. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	3801h	4kB - MSMCv3 CSCTI Instance 5 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.7 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6 Register (Offset = 18h) [reset = 8002h]

rom table entry 6

Return to Summary Table

Table 14-25928. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0018h**

Figure 14-8548. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6 Name Register

31	30	29	28	27	26	25	24
ID							
R							
4001h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ID							
R							
4001h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ID							
R							
4001h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID							PRESENT
R							R
4001h							0h

Table 14-25930. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	4001h	4kB - MSMCv3 CSCTI Instance 6 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.8 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7 Register (Offset = 1Ch) [reset = 9002h]

rom table entry 7

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Table 14-25931. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 001Ch**

Figure 14-8549. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7 Name Register

31	30	29	28	27	26	25	24
ID							
R							
4801h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ID							
R							
4801h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ID							
R							
4801h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID							PRESENT
R							R
4801h							0h

Table 14-25933. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	4801h	4kB - MSMCv3 CSCTI Instance 7 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.9 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8 Register (Offset = 20h) [reset = A002h]

rom table entry 8

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Table 14-25934. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0020h**

Figure 14-8550. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5001h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5001h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5001h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">ID</td><td>PRESENT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">5001h</td><td>0h</td></tr>
</table>

Table 14-25936. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	5001h	256kB - Processor Cluster Instance 0 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.10 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9 Register (Offset = 24h) [reset = B002h]

rom table entry 9

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Table 14-25937. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0024h**

Figure 14-8551. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5801h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5801h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5801h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">ID</td><td>PRESENT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">5801h</td><td>0h</td></tr>
</table>

Table 14-25939. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	5801h	256kB - Processor Cluster Instance 1 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.11 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10 Register (Offset = 28h) [reset = C002h]

rom table entry 10

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Table 14-25940. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0028h**

Figure 14-8552. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10 Name Register

31	30	29	28	27	26	25	24
ID							
R							
6001h							
23	22	21	20	19	18	17	16
ID							
R							
6001h							
15	14	13	12	11	10	9	8
ID							
R							
6001h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
6001h							0h

Table 14-25942. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	6001h	256kB - Processor Cluster Instance 2 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.12 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11 Register (Offset = 2Ch) [reset = D002h]

rom table entry 11

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Table 14-25943. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 002Ch

Figure 14-8553. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11 Name Register

31	30	29	28	27	26	25	24
ID							
R							
6801h							
23	22	21	20	19	18	17	16
ID							
R							
6801h							
15	14	13	12	11	10	9	8
ID							
R							
6801h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
6801h							0h

Table 14-25945. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	6801h	256kB - Processor Cluster Instance 3 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.13 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12 Register (Offset = 30h) [reset = E002h]

rom table entry 12

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Table 14-25946. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0030h**

Figure 14-8554. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12 Name Register

31	30	29	28	27	26	25	24
ID							
R							
7001h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ID							
R							
7001h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ID							
R							
7001h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID							PRESENT
R							R
7001h							0h

Table 14-25948. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	7001h	256kB - Processor Cluster Instance 4 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.14 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13 Register (Offset = 34h) [reset = F002h]

rom table entry 13

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Table 14-25949. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0034h**

Figure 14-8555. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13 Name Register

31	30	29	28	27	26	25	24
ID							
R							
7801h							
23	22	21	20	19	18	17	16
ID							
R							
7801h							
15	14	13	12	11	10	9	8
ID							
R							
7801h							
7	6	5	4	3	2	1	0
ID							PRESENT
R							R
7801h							0h

Table 14-25951. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ID	R	7801h	256kB - Processor Cluster Instance 5 Reset Source: dbg_srst_mod_g_rst_n
0	PRESENT	R	0h	Component present,1, or not present,0, status bit Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.15 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14 Register (Offset = 50h) [reset = 0h]

rom table entry 20

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Table 14-25952. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0050h**

Figure 14-8556. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-25954. DEBUGSS_DEBUG_CELL_ROM_SLV_ENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	End of table Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.16 *DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4 Register*

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Peripheral Identification Register Number 4

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Table 14-25955. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FD0h**

Figure 14-8557. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-25957. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.17 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5 Register (Offset = FD4h) [reset = 0h]

Peripheral Identification Register Number 5

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Table 14-25958. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FD4h**

Figure 14-8558. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-25960. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.18 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6 Register (Offset = FD8h) [reset = 0h]

Peripheral Identification Register Number 6

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Table 14-25961. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FD8h**

Figure 14-8559. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-25963. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.19 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register Number 7

Return to Summary Table

Table 14-25964. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FDCh**

Figure 14-8560. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-25966. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.20 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0 Register (Offset = FE0h) [reset = D1h]

Peripheral Identification Register Number 0

Return to Summary Table

Table 14-25967. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FE0h**

Figure 14-8561. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
ID							
R							
D1h							
23	22	21	20	19	18	17	16
ID							
R							
D1h							
15	14	13	12	11	10	9	8
ID							
R							
D1h							
7	6	5	4	3	2	1	0
ID							
R							
D1h							

Table 14-25969. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	D1h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.21 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1 Register (Offset = FE4h) [reset = 7Eh]

Peripheral Identification Register Number 1

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Table 14-25970. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FE4h**

Figure 14-8562. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
ID							
R							
7Eh							
23	22	21	20	19	18	17	16
ID							
R							
7Eh							
15	14	13	12	11	10	9	8
ID							
R							
7Eh							
7	6	5	4	3	2	1	0
ID							
R							
7Eh							

Table 14-25972. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	7Eh	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.22 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2 Register (Offset = FE8h) [reset = 9h]

Peripheral Identification Register Number 2

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Table 14-25973. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FE8h**

Figure 14-8563. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
ID							
R							
9h							
23	22	21	20	19	18	17	16
ID							
R							
9h							
15	14	13	12	11	10	9	8
ID							
R							
9h							
7	6	5	4	3	2	1	0
ID							
R							
9h							

Table 14-25975. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	9h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.23 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register Number 3

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Table 14-25976. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FECh**

Figure 14-8564. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
ID							
R							
0h							
15	14	13	12	11	10	9	8
ID							
R							
0h							
7	6	5	4	3	2	1	0
ID							
R							
0h							

Table 14-25978. DEBUGSS_DEBUG_CELL_ROM_SLV_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	0h	Peripheral Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.24 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0 Register (Offset = FF0h) [reset = Dh]

Component Identification Register Number 0

Return to Summary Table

Table 14-25979. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 0FF0h

Figure 14-8565. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0 Name Register

31	30	29	28	27	26	25	24
ID							
R							
Dh							
23	22	21	20	19	18	17	16
ID							
R							
Dh							
15	14	13	12	11	10	9	8
ID							
R							
Dh							
7	6	5	4	3	2	1	0
ID							
R							
Dh							

Table 14-25981. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	Dh	Component Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.25 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1 Register (Offset = FF4h) [reset = 10h]

Component Identification Register Number 1

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Table 14-25982. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FF4h**

Figure 14-8566. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1 Name Register

31	30	29	28	27	26	25	24
ID							
R							
10h							
23	22	21	20	19	18	17	16
ID							
R							
10h							
15	14	13	12	11	10	9	8
ID							
R							
10h							
7	6	5	4	3	2	1	0
ID							
R							
10h							

Table 14-25984. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	10h	Component Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.26 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register Number 2

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Table 14-25985. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FF8h**

Figure 14-8567. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2 Name Register

31	30	29	28	27	26	25	24
ID							
R							
5h							
23	22	21	20	19	18	17	16
ID							
R							
5h							
15	14	13	12	11	10	9	8
ID							
R							
5h							
7	6	5	4	3	2	1	0
ID							
R							
5h							

Table 14-25987. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	5h	Component Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.27 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3 Register

1 DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3 Register (Offset = FFCh) [reset = B1h]

Component Identification Register Number 3

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Table 14-25988. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 0FFCh**

Figure 14-8568. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3 Name Register

31	30	29	28	27	26	25	24
ID							
R							
B1h							
23	22	21	20	19	18	17	16
ID							
R							
B1h							
15	14	13	12	11	10	9	8
ID							
R							
B1h							
7	6	5	4	3	2	1	0
ID							
R							
B1h							

Table 14-25990. DEBUGSS_DEBUG_CELL_ROM_SLV_COMPONENTID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ID	R	B1h	Component Identification Number Reset Source: dbg_srst_mod_g_rst_n

14.11.1.2.28 CTSET2_CFG_CTSETID Register

1 CTSET2_CFG_CTSETID Register (Offset = 0h) [reset = 62800200h]

CTSET identification register

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Table 14-25991. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2000h**

Figure 14-8569. CTSET2_CFG_CTSETID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		280h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
280h							
15	14	13	12	11	10	9	8
RTL_VERSION					MAJOR_REV		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-25993. CTSET2_CFG_CTSETID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old Scheme and current
29:28	BU	R	2h	The value 10b designates this as Processor Business Unit IP
27:16	FUNCTION	R	280h	Function : Indicates a Debug IP (0x2nn) and 0x80 is the identifier for CT-SET
15:11	RTL_VERSION	R	0h	This field changes on bug fix, and resets to '0' when either Minor Revision or Major Revision field changes
10:8	MAJOR_REV	R	2h	Major Revision. This field changes when there is a major feature change.
7:6	CUSTOM	R	0h	Indicates a special version for a particular device. 0 if non-custom
5:0	MINOR_REV	R	0h	Minor Revision. This field changes when features are scaled up or down

14.11.1.2.29 CTSET2_CFG_CTSETSYSCFG Register

1 CTSET2_CFG_CTSETSYSCFG Register (Offset = 10h) [reset = 8h]

CTSET system configuration register

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Table 14-25994. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2010h**

Figure 14-8570. CTSET2_CFG_CTSETSYSCFG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1				IDLEMODE		RESERVED	SOFTRESET
R				R/W		R	R/W
0h				2h		0h	0h

Table 14-25996. CTSET2_CFG_CTSETSYSCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED1	R	0h	Reserved, returns 0
3:2	IDLEMODE	R/W	2h	Sets the Idle Mode for CTSET (0=Force Idle, 1=No Idle, 2=Smart Idle, 3= Smart Idle wakeup)
1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	This will reset entire CTSET, except the registers and the CFG interface. This bit is automatically cleared by hardware. Reads always return 0

14.11.1.2.30 CTSET2_CFG_SETSTR Register

1 CTSET2_CFG_SETSTR Register (Offset = 14h) [reset = 101h]

CTSET status register

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Table 14-25997. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2014h**

Figure 14-8571. CTSET2_CFG_SETSTR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							HWFIFOEMPTY
R							R
0h							1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RESETDONE
R							R
0h							1h

Table 14-25999. CTSET2_CFG_SETSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8	HWFIFOEMPTY	R	1h	System Event Trace FIFO status, 1 is empty, 0 means captured data not yet exported
7:1	RESERVED	R	0h	Reserved, returns 0
0	RESETDONE	R	1h	Reset status, 0 means reset ongoing, 1 indicates completed

14.11.1.2.31 CTSET2_CFG_DBGTIMELOW Register

1 CTSET2_CFG_DBGTIMELOW Register (Offset = 18h) [reset = 0h]

The 32 low order bits of the debug time value supplied on the time input interface

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Table 14-26000. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2018h**

Figure 14-8572. CTSET2_CFG_DBGTIMELOW Name Register

31	30	29	28	27	26	25	24
DBGTIME							
R							
0h							
23	22	21	20	19	18	17	16
DBGTIME							
R							
0h							
15	14	13	12	11	10	9	8
DBGTIME							
R							
0h							
7	6	5	4	3	2	1	0
DBGTIME							
R							
0h							

Table 14-26002. CTSET2_CFG_DBGTIMELOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGTIME	R	0h	debug time

14.11.1.2.32 CTSET2_CFG_DBGTIMEHI Register

1 CTSET2_CFG_DBGTIMEHI Register (Offset = 1Ch) [reset = 0h]

The 32 high order bits of the debug time value supplied on the time input interface

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Table 14-26003. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 201Ch

Figure 14-8573. CTSET2_CFG_DBGTIMEHI Name Register

31	30	29	28	27	26	25	24
DBGTIME							
R							
0h							
23	22	21	20	19	18	17	16
DBGTIME							
R							
0h							
15	14	13	12	11	10	9	8
DBGTIME							
R							
0h							
7	6	5	4	3	2	1	0
DBGTIME							
R							
0h							

Table 14-26005. CTSET2_CFG_DBGTIMEHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGTIME	R	0h	debug time

14.11.1.2.33 CTSET2_CFG_CTSETCFG Register

1 CTSET2_CFG_CTSETCFG Register (Offset = 24h) [reset = 20000010h]

The 32 low order bits of the debug time value supplied on the time input interface The 32 high order bits of the debug time value supplied on the time input interface. Reading DBGTIMEHI latches the lower 32 bits of debug time value CTSET configuration register

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Table 14-26006. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2024h**

Figure 14-8574. CTSET2_CFG_CTSETCFG Name Register

31	30	29	28	27	26	25	24
CLAIM				RESERVED2			
R/W				R			
2h				0h			
23	22	21	20	19	18	17	16
RESERVED2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
SYSEVENTCAPTEN	RESERVED1		EVENTLEVEL	MSGMODE	STOPCAPT	STARTCAPT	RESERVED
R/W	R		R/W	R/W	R/W	R/W	R
0h	0h		1h	0h	0h	0h	0h

Table 14-26008. CTSET2_CFG_CTSETCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CLAIM	R/W	2h	Claim control and status. To program any bits other than 31 : 28, CTSET ownership must be claimed using bits 31 : 28.
27:8	RESERVED2	R	0h	Reserved, returns 0
7	SYSEVENTCAPTEN	R/W	0h	When 1 the System event capture is enabled
6:5	RESERVED1	R	0h	Reserved, returns 0
4	EVENTLEVEL	R/W	1h	0 enables low level event detection, 1 enables high level event detection
3	MSGMODE	R/W	0h	Message generated based on event detection, 0 is sampling window, 1 is event detection
2	STOPCAPT	R/W	0h	Stop capturing system events from external trigger detection
1	STARTCAPT	R/W	0h	Start capturing system events from external trigger detection
0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.34 CTSET2_CFG_SETSPLREG Register

1 CTSET2_CFG_SETSPLREG Register (Offset = 28h) [reset = 0h]

System Event Sampling Window register

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Table 14-26009. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2028h**

Figure 14-8575. CTSET2_CFG_SETSPLREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WINDOWSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26011. CTSET2_CFG_SETSPLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	WINDOWSIZE	R/W	0h	System events sampling window size expressed as CTSET cycles

14.11.1.2.35 CTSET2_CFG_SETEVTENBL1 Register

1 CTSET2_CFG_SETEVTENBL1 Register (Offset = 30h) [reset = 0h]

System event detection enable register 1

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Table 14-26012. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2030h**

Figure 14-8576. CTSET2_CFG_SETEVTENBL1 Name Register

31	30	29	28	27	26	25	24
EVENT32DETEN	EVENT31DETEN	EVENT30DETEN	EVENT29DETEN	EVENT28DETEN	EVENT27DETEN	EVENT26DETEN	EVENT25DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT24DETEN	EVENT23DETEN	EVENT22DETEN	EVENT21DETEN	EVENT20DETEN	EVENT19DETEN	EVENT18DETEN	EVENT17DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT16DETEN	EVENT15DETEN	EVENT14DETEN	EVENT13DETEN	EVENT12DETEN	EVENT11DETEN	EVENT10DETEN	EVENT9DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT8DETEN	EVENT7DETEN	EVENT6DETEN	EVENT5DETEN	EVENT4DETEN	EVENT3DETEN	EVENT2DETEN	EVENT1DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26014. CTSET2_CFG_SETEVTENBL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT32DETEN	R/W	0h	Event(32) Detection Enable
30	EVENT31DETEN	R/W	0h	Event(31) Detection Enable
29	EVENT30DETEN	R/W	0h	Event(30) Detection Enable
28	EVENT29DETEN	R/W	0h	Event(29) Detection Enable
27	EVENT28DETEN	R/W	0h	Event(28) Detection Enable
26	EVENT27DETEN	R/W	0h	Event(27) Detection Enable
25	EVENT26DETEN	R/W	0h	Event(26) Detection Enable
24	EVENT25DETEN	R/W	0h	Event(25) Detection Enable
23	EVENT24DETEN	R/W	0h	Event(24) Detection Enable
22	EVENT23DETEN	R/W	0h	Event(23) Detection Enable
21	EVENT22DETEN	R/W	0h	Event(22) Detection Enable
20	EVENT21DETEN	R/W	0h	Event(21) Detection Enable
19	EVENT20DETEN	R/W	0h	Event(20) Detection Enable
18	EVENT19DETEN	R/W	0h	Event(19) Detection Enable
17	EVENT18DETEN	R/W	0h	Event(18) Detection Enable

Table 14-26014. CTSET2_CFG_SETEVTENBL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT17DETEN	R/W	0h	Event(17) Detection Enable
15	EVENT16DETEN	R/W	0h	Event(16) Detection Enable
14	EVENT15DETEN	R/W	0h	Event(15) Detection Enable
13	EVENT14DETEN	R/W	0h	Event(14) Detection Enable
12	EVENT13DETEN	R/W	0h	Event(13) Detection Enable
11	EVENT12DETEN	R/W	0h	Event(12) Detection Enable
10	EVENT11DETEN	R/W	0h	Event(11) Detection Enable
9	EVENT10DETEN	R/W	0h	Event(10) Detection Enable
8	EVENT9DETEN	R/W	0h	Event(9) Detection Enable
7	EVENT8DETEN	R/W	0h	Event(8) Detection Enable
6	EVENT7DETEN	R/W	0h	Event(7) Detection Enable
5	EVENT6DETEN	R/W	0h	Event(6) Detection Enable
4	EVENT5DETEN	R/W	0h	Event(5) Detection Enable
3	EVENT4DETEN	R/W	0h	Event(4) Detection Enable
2	EVENT3DETEN	R/W	0h	Event(3) Detection Enable
1	EVENT2DETEN	R/W	0h	Event(2) Detection Enable
0	EVENT1DETEN	R/W	0h	Event(1) Detection Enable

14.11.1.2.36 CTSET2_CFG_SETEVTENBL2 Register

1 CTSET2_CFG_SETEVTENBL2 Register (Offset = 34h) [reset = 0h]

System event detection enable register 2 (if number of events > 32)

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Table 14-26015. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2034h**

Figure 14-8577. CTSET2_CFG_SETEVTENBL2 Name Register

31	30	29	28	27	26	25	24
EVENT64DETEN	EVENT63DETEN	EVENT62DETEN	EVENT61DETEN	EVENT60DETEN	EVENT59DETEN	EVENT58DETEN	EVENT57DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT56DETEN	EVENT55DETEN	EVENT54DETEN	EVENT53DETEN	EVENT52DETEN	EVENT51DETEN	EVENT50DETEN	EVENT49DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT48DETEN	EVENT47DETEN	EVENT46DETEN	EVENT45DETEN	EVENT44DETEN	EVENT43DETEN	EVENT42DETEN	EVENT41DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT40DETEN	EVENT39DETEN	EVENT38DETEN	EVENT37DETEN	EVENT36DETEN	EVENT35DETEN	EVENT34DETEN	EVENT33DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26017. CTSET2_CFG_SETEVTENBL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT64DETEN	R/W	0h	Event(64) Detection Enable
30	EVENT63DETEN	R/W	0h	Event(63) Detection Enable
29	EVENT62DETEN	R/W	0h	Event(62) Detection Enable
28	EVENT61DETEN	R/W	0h	Event(61) Detection Enable
27	EVENT60DETEN	R/W	0h	Event(60) Detection Enable
26	EVENT59DETEN	R/W	0h	Event(59) Detection Enable
25	EVENT58DETEN	R/W	0h	Event(58) Detection Enable
24	EVENT57DETEN	R/W	0h	Event(57) Detection Enable
23	EVENT56DETEN	R/W	0h	Event(56) Detection Enable
22	EVENT55DETEN	R/W	0h	Event(55) Detection Enable
21	EVENT54DETEN	R/W	0h	Event(54) Detection Enable
20	EVENT53DETEN	R/W	0h	Event(53) Detection Enable
19	EVENT52DETEN	R/W	0h	Event(52) Detection Enable
18	EVENT51DETEN	R/W	0h	Event(51) Detection Enable
17	EVENT50DETEN	R/W	0h	Event(50) Detection Enable

Table 14-26017. CTSET2_CFG_SETEVTENBL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT49DETEN	R/W	0h	Event(49) Detection Enable
15	EVENT48DETEN	R/W	0h	Event(48) Detection Enable
14	EVENT47DETEN	R/W	0h	Event(47) Detection Enable
13	EVENT46DETEN	R/W	0h	Event(46) Detection Enable
12	EVENT45DETEN	R/W	0h	Event(45) Detection Enable
11	EVENT44DETEN	R/W	0h	Event(44) Detection Enable
10	EVENT43DETEN	R/W	0h	Event(43) Detection Enable
9	EVENT42DETEN	R/W	0h	Event(42) Detection Enable
8	EVENT41DETEN	R/W	0h	Event(41) Detection Enable
7	EVENT40DETEN	R/W	0h	Event(40) Detection Enable
6	EVENT39DETEN	R/W	0h	Event(39) Detection Enable
5	EVENT38DETEN	R/W	0h	Event(38) Detection Enable
4	EVENT37DETEN	R/W	0h	Event(37) Detection Enable
3	EVENT36DETEN	R/W	0h	Event(36) Detection Enable
2	EVENT35DETEN	R/W	0h	Event(35) Detection Enable
1	EVENT34DETEN	R/W	0h	Event(34) Detection Enable
0	EVENT33DETEN	R/W	0h	Event(33) Detection Enable

14.11.1.2.37 CTSET2_CFG_SETEVTENBL3 Register

1 CTSET2_CFG_SETEVTENBL3 Register (Offset = 38h) [reset = 0h]

System event detection enable register 3 (if number of events > 64)

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Table 14-26018. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2038h**

Figure 14-8578. CTSET2_CFG_SETEVTENBL3 Name Register

31	30	29	28	27	26	25	24
EVENT96DETEN	EVENT95DETEN	EVENT94DETEN	EVENT93DETEN	EVENT92DETEN	EVENT91DETEN	EVENT90DETEN	EVENT89DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT88DETEN	EVENT87DETEN	EVENT86DETEN	EVENT85DETEN	EVENT84DETEN	EVENT83DETEN	EVENT82DETEN	EVENT81DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT80DETEN	EVENT79DETEN	EVENT78DETEN	EVENT77DETEN	EVENT76DETEN	EVENT75DETEN	EVENT74DETEN	EVENT73DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT72DETEN	EVENT71DETEN	EVENT70DETEN	EVENT69DETEN	EVENT68DETEN	EVENT67DETEN	EVENT66DETEN	EVENT65DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26020. CTSET2_CFG_SETEVTENBL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT96DETEN	R/W	0h	Event(96) Detection Enable
30	EVENT95DETEN	R/W	0h	Event(95) Detection Enable
29	EVENT94DETEN	R/W	0h	Event(94) Detection Enable
28	EVENT93DETEN	R/W	0h	Event(93) Detection Enable
27	EVENT92DETEN	R/W	0h	Event(92) Detection Enable
26	EVENT91DETEN	R/W	0h	Event(91) Detection Enable
25	EVENT90DETEN	R/W	0h	Event(90) Detection Enable
24	EVENT89DETEN	R/W	0h	Event(89) Detection Enable
23	EVENT88DETEN	R/W	0h	Event(88) Detection Enable
22	EVENT87DETEN	R/W	0h	Event(87) Detection Enable
21	EVENT86DETEN	R/W	0h	Event(86) Detection Enable
20	EVENT85DETEN	R/W	0h	Event(85) Detection Enable
19	EVENT84DETEN	R/W	0h	Event(84) Detection Enable
18	EVENT83DETEN	R/W	0h	Event(83) Detection Enable
17	EVENT82DETEN	R/W	0h	Event(82) Detection Enable

Table 14-26020. CTSET2_CFG_SETEVTENBL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT81DETEN	R/W	0h	Event(81) Detection Enable
15	EVENT80DETEN	R/W	0h	Event(80) Detection Enable
14	EVENT79DETEN	R/W	0h	Event(79) Detection Enable
13	EVENT78DETEN	R/W	0h	Event(78) Detection Enable
12	EVENT77DETEN	R/W	0h	Event(77) Detection Enable
11	EVENT76DETEN	R/W	0h	Event(76) Detection Enable
10	EVENT75DETEN	R/W	0h	Event(75) Detection Enable
9	EVENT74DETEN	R/W	0h	Event(74) Detection Enable
8	EVENT73DETEN	R/W	0h	Event(73) Detection Enable
7	EVENT72DETEN	R/W	0h	Event(72) Detection Enable
6	EVENT71DETEN	R/W	0h	Event(71) Detection Enable
5	EVENT70DETEN	R/W	0h	Event(70) Detection Enable
4	EVENT69DETEN	R/W	0h	Event(69) Detection Enable
3	EVENT68DETEN	R/W	0h	Event(68) Detection Enable
2	EVENT67DETEN	R/W	0h	Event(67) Detection Enable
1	EVENT66DETEN	R/W	0h	Event(66) Detection Enable
0	EVENT65DETEN	R/W	0h	Event(65) Detection Enable

14.11.1.2.38 CTSET2_CFG_SETEVTENBL4 Register

1 CTSET2_CFG_SETEVTENBL4 Register (Offset = 3Ch) [reset = 0h]

System event detection enable register 4 (if number of events > 96)

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Table 14-26021. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 203Ch

Figure 14-8579. CTSET2_CFG_SETEVTENBL4 Name Register

31	30	29	28	27	26	25	24
EVENT128DETEN	EVENT127DETEN	EVENT126DETEN	EVENT125DETEN	EVENT124DETEN	EVENT123DETEN	EVENT122DETEN	EVENT121DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT120DETEN	EVENT119DETEN	EVENT118DETEN	EVENT117DETEN	EVENT116DETEN	EVENT115DETEN	EVENT114DETEN	EVENT113DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT112DETEN	EVENT111DETEN	EVENT110DETEN	EVENT109DETEN	EVENT108DETEN	EVENT107DETEN	EVENT106DETEN	EVENT105DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT104DETEN	EVENT103DETEN	EVENT102DETEN	EVENT101DETEN	EVENT100DETEN	EVENT99DETEN	EVENT98DETEN	EVENT97DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26023. CTSET2_CFG_SETEVTENBL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT128DETEN	R/W	0h	Event(128) Detection Enable
30	EVENT127DETEN	R/W	0h	Event(127) Detection Enable
29	EVENT126DETEN	R/W	0h	Event(126) Detection Enable
28	EVENT125DETEN	R/W	0h	Event(125) Detection Enable
27	EVENT124DETEN	R/W	0h	Event(124) Detection Enable
26	EVENT123DETEN	R/W	0h	Event(123) Detection Enable
25	EVENT122DETEN	R/W	0h	Event(122) Detection Enable
24	EVENT121DETEN	R/W	0h	Event(121) Detection Enable
23	EVENT120DETEN	R/W	0h	Event(120) Detection Enable
22	EVENT119DETEN	R/W	0h	Event(119) Detection Enable
21	EVENT118DETEN	R/W	0h	Event(118) Detection Enable
20	EVENT117DETEN	R/W	0h	Event(117) Detection Enable
19	EVENT116DETEN	R/W	0h	Event(116) Detection Enable
18	EVENT115DETEN	R/W	0h	Event(115) Detection Enable
17	EVENT114DETEN	R/W	0h	Event(114) Detection Enable

Table 14-26023. CTSET2_CFG_SETEVTENBL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT113DETEN	R/W	0h	Event(113) Detection Enable
15	EVENT112DETEN	R/W	0h	Event(112) Detection Enable
14	EVENT111DETEN	R/W	0h	Event(111) Detection Enable
13	EVENT110DETEN	R/W	0h	Event(110) Detection Enable
12	EVENT109DETEN	R/W	0h	Event(109) Detection Enable
11	EVENT108DETEN	R/W	0h	Event(108) Detection Enable
10	EVENT107DETEN	R/W	0h	Event(107) Detection Enable
9	EVENT106DETEN	R/W	0h	Event(106) Detection Enable
8	EVENT105DETEN	R/W	0h	Event(105) Detection Enable
7	EVENT104DETEN	R/W	0h	Event(104) Detection Enable
6	EVENT103DETEN	R/W	0h	Event(103) Detection Enable
5	EVENT102DETEN	R/W	0h	Event(102) Detection Enable
4	EVENT101DETEN	R/W	0h	Event(101) Detection Enable
3	EVENT100DETEN	R/W	0h	Event(100) Detection Enable
2	EVENT99DETEN	R/W	0h	Event(99) Detection Enable
1	EVENT98DETEN	R/W	0h	Event(98) Detection Enable
0	EVENT97DETEN	R/W	0h	Event(97) Detection Enable

14.11.1.2.39 CTSET2_CFG_SETEVTENBL5 Register

1 CTSET2_CFG_SETEVTENBL5 Register (Offset = 40h) [reset = 0h]

System event detection enable register 5 (if number of events > 128)

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Table 14-26024. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2040h

Figure 14-8580. CTSET2_CFG_SETEVTENBL5 Name Register

31	30	29	28	27	26	25	24
EVENT160DETEN	EVENT159DETEN	EVENT158DETEN	EVENT157DETEN	EVENT156DETEN	EVENT155DETEN	EVENT154DETEN	EVENT153DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT152DETEN	EVENT151DETEN	EVENT150DETEN	EVENT149DETEN	EVENT148DETEN	EVENT147DETEN	EVENT1468DETEN	EVENT145DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT144DETEN	EVENT143DETEN	EVENT142DETEN	EVENT141DETEN	EVENT140DETEN	EVENT139DETEN	EVENT138DETEN	EVENT137DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT136DETEN	EVENT135DETEN	EVENT134DETEN	EVENT133DETEN	EVENT132DETEN	EVENT131DETEN	EVENT130DETEN	EVENT129DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26026. CTSET2_CFG_SETEVTENBL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT160DETEN	R/W	0h	Event(160) Detection Enable
30	EVENT159DETEN	R/W	0h	Event(159) Detection Enable
29	EVENT158DETEN	R/W	0h	Event(158) Detection Enable
28	EVENT157DETEN	R/W	0h	Event(157) Detection Enable
27	EVENT156DETEN	R/W	0h	Event(156) Detection Enable
26	EVENT155DETEN	R/W	0h	Event(155) Detection Enable
25	EVENT154DETEN	R/W	0h	Event(154) Detection Enable
24	EVENT153DETEN	R/W	0h	Event(153) Detection Enable
23	EVENT152DETEN	R/W	0h	Event(152) Detection Enable
22	EVENT151DETEN	R/W	0h	Event(151) Detection Enable
21	EVENT150DETEN	R/W	0h	Event(150) Detection Enable
20	EVENT149DETEN	R/W	0h	Event(149) Detection Enable
19	EVENT148DETEN	R/W	0h	Event(148) Detection Enable
18	EVENT147DETEN	R/W	0h	Event(147) Detection Enable
17	EVENT1468DETEN	R/W	0h	Event(146) Detection Enable

Table 14-26026. CTSET2_CFG_SETEVTENBL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT145DETEN	R/W	0h	Event(145) Detection Enable
15	EVENT144DETEN	R/W	0h	Event(144) Detection Enable
14	EVENT143DETEN	R/W	0h	Event(143) Detection Enable
13	EVENT142DETEN	R/W	0h	Event(142) Detection Enable
12	EVENT141DETEN	R/W	0h	Event(141) Detection Enable
11	EVENT140DETEN	R/W	0h	Event(140) Detection Enable
10	EVENT139DETEN	R/W	0h	Event(139) Detection Enable
9	EVENT138DETEN	R/W	0h	Event(138) Detection Enable
8	EVENT137DETEN	R/W	0h	Event(137) Detection Enable
7	EVENT136DETEN	R/W	0h	Event(136) Detection Enable
6	EVENT135DETEN	R/W	0h	Event(135) Detection Enable
5	EVENT134DETEN	R/W	0h	Event(134) Detection Enable
4	EVENT133DETEN	R/W	0h	Event(133) Detection Enable
3	EVENT132DETEN	R/W	0h	Event(132) Detection Enable
2	EVENT131DETEN	R/W	0h	Event(131) Detection Enable
1	EVENT130DETEN	R/W	0h	Event(130) Detection Enable
0	EVENT129DETEN	R/W	0h	Event(129) Detection Enable

14.11.1.2.40 CTSET2_CFG_SETEVTENBL6 Register

1 CTSET2_CFG_SETEVTENBL6 Register (Offset = 44h) [reset = 0h]

System event detection enable register 6 (if number of events > 160)

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Table 14-26027. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2044h**

Figure 14-8581. CTSET2_CFG_SETEVTENBL6 Name Register

31	30	29	28	27	26	25	24
EVENT192DETEN	EVENT191DETEN	EVENT190DETEN	EVENT189DETEN	EVENT188DETEN	EVENT187DETEN	EVENT186DETEN	EVENT185DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT184DETEN	EVENT183DETEN	EVENT182DETEN	EVENT181DETEN	EVENT180DETEN	EVENT179DETEN	EVENT178DETEN	EVENT177DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT176DETEN	EVENT175DETEN	EVENT174DETEN	EVENT173DETEN	EVENT172DETEN	EVENT171DETEN	EVENT170DETEN	EVENT169DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT168DETEN	EVENT167DETEN	EVENT166DETEN	EVENT165DETEN	EVENT164DETEN	EVENT163DETEN	EVENT162DETEN	EVENT161DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26029. CTSET2_CFG_SETEVTENBL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT192DETEN	R/W	0h	Event(192) Detection Enable
30	EVENT191DETEN	R/W	0h	Event(191) Detection Enable
29	EVENT190DETEN	R/W	0h	Event(190) Detection Enable
28	EVENT189DETEN	R/W	0h	Event(189) Detection Enable
27	EVENT188DETEN	R/W	0h	Event(188) Detection Enable
26	EVENT187DETEN	R/W	0h	Event(187) Detection Enable
25	EVENT186DETEN	R/W	0h	Event(186) Detection Enable
24	EVENT185DETEN	R/W	0h	Event(185) Detection Enable
23	EVENT184DETEN	R/W	0h	Event(184) Detection Enable
22	EVENT183DETEN	R/W	0h	Event(183) Detection Enable
21	EVENT182DETEN	R/W	0h	Event(182) Detection Enable
20	EVENT181DETEN	R/W	0h	Event(181) Detection Enable
19	EVENT180DETEN	R/W	0h	Event(180) Detection Enable
18	EVENT179DETEN	R/W	0h	Event(179) Detection Enable
17	EVENT178DETEN	R/W	0h	Event(178) Detection Enable

Table 14-26029. CTSET2_CFG_SETEVTENBL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT177DETEN	R/W	0h	Event(177) Detection Enable
15	EVENT176DETEN	R/W	0h	Event(176) Detection Enable
14	EVENT175DETEN	R/W	0h	Event(175) Detection Enable
13	EVENT174DETEN	R/W	0h	Event(174) Detection Enable
12	EVENT173DETEN	R/W	0h	Event(173) Detection Enable
11	EVENT172DETEN	R/W	0h	Event(172) Detection Enable
10	EVENT171DETEN	R/W	0h	Event(171) Detection Enable
9	EVENT170DETEN	R/W	0h	Event(170) Detection Enable
8	EVENT169DETEN	R/W	0h	Event(169) Detection Enable
7	EVENT168DETEN	R/W	0h	Event(168) Detection Enable
6	EVENT167DETEN	R/W	0h	Event(167) Detection Enable
5	EVENT166DETEN	R/W	0h	Event(166) Detection Enable
4	EVENT165DETEN	R/W	0h	Event(165) Detection Enable
3	EVENT164DETEN	R/W	0h	Event(164) Detection Enable
2	EVENT163DETEN	R/W	0h	Event(163) Detection Enable
1	EVENT162DETEN	R/W	0h	Event(162) Detection Enable
0	EVENT161DETEN	R/W	0h	Event(161) Detection Enable

14.11.1.2.41 CTSET2_CFG_SETEVTENBL7 Register

1 CTSET2_CFG_SETEVTENBL7 Register (Offset = 48h) [reset = 0h]

System event detection enable register 7 (if number of events > 192)

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Table 14-26030. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2048h

Figure 14-8582. CTSET2_CFG_SETEVTENBL7 Name Register

31	30	29	28	27	26	25	24
EVENT224DETEN	EVENT223DETEN	EVENT222DETEN	EVENT221DETEN	EVENT220DETEN	EVENT219DETEN	EVENT218DETEN	EVENT217DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT216DETEN	EVENT215DETEN	EVENT214DETEN	EVENT213DETEN	EVENT212DETEN	EVENT211DETEN	EVENT210DETEN	EVENT209DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT208DETEN	EVENT207DETEN	EVENT206DETEN	EVENT205DETEN	EVENT204DETEN	EVENT203DETEN	EVENT202DETEN	EVENT201DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT200DETEN	EVENT199DETEN	EVENT198DETEN	EVENT197DETEN	EVENT196DETEN	EVENT195DETEN	EVENT194DETEN	EVENT193DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26032. CTSET2_CFG_SETEVTENBL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT224DETEN	R/W	0h	Event(224) Detection Enable
30	EVENT223DETEN	R/W	0h	Event(223) Detection Enable
29	EVENT222DETEN	R/W	0h	Event(222) Detection Enable
28	EVENT221DETEN	R/W	0h	Event(221) Detection Enable
27	EVENT220DETEN	R/W	0h	Event(220) Detection Enable
26	EVENT219DETEN	R/W	0h	Event(219) Detection Enable
25	EVENT218DETEN	R/W	0h	Event(218) Detection Enable
24	EVENT217DETEN	R/W	0h	Event(217) Detection Enable
23	EVENT216DETEN	R/W	0h	Event(216) Detection Enable
22	EVENT215DETEN	R/W	0h	Event(215) Detection Enable
21	EVENT214DETEN	R/W	0h	Event(214) Detection Enable
20	EVENT213DETEN	R/W	0h	Event(213) Detection Enable
19	EVENT212DETEN	R/W	0h	Event(212) Detection Enable
18	EVENT211DETEN	R/W	0h	Event(211) Detection Enable
17	EVENT210DETEN	R/W	0h	Event(210) Detection Enable

Table 14-26032. CTSET2_CFG_SETEVTENBL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT209DETEN	R/W	0h	Event(209) Detection Enable
15	EVENT208DETEN	R/W	0h	Event(208) Detection Enable
14	EVENT207DETEN	R/W	0h	Event(207) Detection Enable
13	EVENT206DETEN	R/W	0h	Event(206) Detection Enable
12	EVENT205DETEN	R/W	0h	Event(205) Detection Enable
11	EVENT204DETEN	R/W	0h	Event(204) Detection Enable
10	EVENT203DETEN	R/W	0h	Event(203) Detection Enable
9	EVENT202DETEN	R/W	0h	Event(202) Detection Enable
8	EVENT201DETEN	R/W	0h	Event(201) Detection Enable
7	EVENT200DETEN	R/W	0h	Event(200) Detection Enable
6	EVENT199DETEN	R/W	0h	Event(199) Detection Enable
5	EVENT198DETEN	R/W	0h	Event(198) Detection Enable
4	EVENT197DETEN	R/W	0h	Event(197) Detection Enable
3	EVENT196DETEN	R/W	0h	Event(196) Detection Enable
2	EVENT195DETEN	R/W	0h	Event(195) Detection Enable
1	EVENT194DETEN	R/W	0h	Event(194) Detection Enable
0	EVENT193DETEN	R/W	0h	Event(193) Detection Enable

14.11.1.2.42 CTSET2_CFG_SETEVTENBL8 Register

1 CTSET2_CFG_SETEVTENBL8 Register (Offset = 4Ch) [reset = 0h]

System event detection enable register 8 (if number of events > 224)

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Table 14-26033. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 204Ch**

Figure 14-8583. CTSET2_CFG_SETEVTENBL8 Name Register

31	30	29	28	27	26	25	24
EVENT256DETEN	EVENT255DETEN	EVENT254DETEN	EVENT253DETEN	EVENT252DETEN	EVENT251DETEN	EVENT250DETEN	EVENT249DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT248DETEN	EVENT247DETEN	EVENT246DETEN	EVENT245DETEN	EVENT244DETEN	EVENT243DETEN	EVENT242DETEN	EVENT241DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT240DETEN	EVENT239DETEN	EVENT238DETEN	EVENT237DETEN	EVENT236DETEN	EVENT235DETEN	EVENT234DETEN	EVENT233DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT232DETEN	EVENT231DETEN	EVENT230DETEN	EVENT229DETEN	EVENT228DETEN	EVENT227DETEN	EVENT226DETEN	EVENT225DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26035. CTSET2_CFG_SETEVTENBL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT256DETEN	R/W	0h	Event(256) Detection Enable
30	EVENT255DETEN	R/W	0h	Event(255) Detection Enable
29	EVENT254DETEN	R/W	0h	Event(254) Detection Enable
28	EVENT253DETEN	R/W	0h	Event(253) Detection Enable
27	EVENT252DETEN	R/W	0h	Event(252) Detection Enable
26	EVENT251DETEN	R/W	0h	Event(251) Detection Enable
25	EVENT250DETEN	R/W	0h	Event(250) Detection Enable
24	EVENT249DETEN	R/W	0h	Event(249) Detection Enable
23	EVENT248DETEN	R/W	0h	Event(248) Detection Enable
22	EVENT247DETEN	R/W	0h	Event(247) Detection Enable
21	EVENT246DETEN	R/W	0h	Event(246) Detection Enable
20	EVENT245DETEN	R/W	0h	Event(245) Detection Enable
19	EVENT244DETEN	R/W	0h	Event(244) Detection Enable
18	EVENT243DETEN	R/W	0h	Event(243) Detection Enable
17	EVENT242DETEN	R/W	0h	Event(242) Detection Enable

Table 14-26035. CTSET2_CFG_SETEVTENBL8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	EVENT241DETEN	R/W	0h	Event(241) Detection Enable
15	EVENT240DETEN	R/W	0h	Event(240) Detection Enable
14	EVENT239DETEN	R/W	0h	Event(239) Detection Enable
13	EVENT238DETEN	R/W	0h	Event(238) Detection Enable
12	EVENT237DETEN	R/W	0h	Event(237) Detection Enable
11	EVENT236DETEN	R/W	0h	Event(236) Detection Enable
10	EVENT235DETEN	R/W	0h	Event(235) Detection Enable
9	EVENT234DETEN	R/W	0h	Event(234) Detection Enable
8	EVENT233DETEN	R/W	0h	Event(233) Detection Enable
7	EVENT232DETEN	R/W	0h	Event(232) Detection Enable
6	EVENT231DETEN	R/W	0h	Event(231) Detection Enable
5	EVENT230DETEN	R/W	0h	Event(230) Detection Enable
4	EVENT229DETEN	R/W	0h	Event(229) Detection Enable
3	EVENT228DETEN	R/W	0h	Event(228) Detection Enable
2	EVENT227DETEN	R/W	0h	Event(227) Detection Enable
1	EVENT226DETEN	R/W	0h	Event(226) Detection Enable
0	EVENT225DETEN	R/W	0h	Event(225) Detection Enable

14.11.1.2.43 CTSET2_CFG_SETMSTID Register

1 CTSET2_CFG_SETMSTID Register (Offset = 50h) [reset = 0h]

System Event Initiator ID

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Table 14-26036. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2050h**

Figure 14-8584. CTSET2_CFG_SETMSTID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MASTID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26038. CTSET2_CFG_SETMSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	MASTID	R/W	0h	HW Initiator ID for System Event module. Software may overwrite the value at any time, but this is only recommended for scenarios where top-level configuration errors result in a collision between HW initiator IDs

14.11.1.2.44 CTSET2_CFG_CTCNTL Register

1 CTSET2_CFG_CTCNTL Register (Offset = 800h) [reset = 0h]

Counter Timer Control

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Table 14-26039. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2800h**

Figure 14-8585. CTSET2_CFG_CTCNTL Name Register

31	30	29	28	27	26	25	24
NUMSTM						NUMINPT	
R						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NUMINPT						NUMTIMR	
R						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NUMTIMR			NUMCNTR				
R			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUMCNTR	REVID				RESERVED	RESERVED	NUMCOREMD
R	R				NONE	R	R
0h	0h				0h	0h	0h

Table 14-26041. CTSET2_CFG_CTCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NUMSTM	R	0h	Number of counters that can export via STM
25:18	NUMINPT	R	0h	Number of event input signals
17:13	NUMTIMR	R	0h	Number of timers in the module
12:7	NUMCNTR	R	0h	Number of counters in the module
6:3	REVID	R	0h	Revision ID of CTSET
2	RESERVED	NONE	0h	Reserved
1	RESERVED	R	0h	Reserved, returns 0
0	NUMCOREMD	R	0h	Indicated the number of mode bus interfaces, 0 is 2 CPU buses, 1 is 4 buses

14.11.1.2.45 CTSET2_CFG_CTNUMDBG Register

1 CTSET2_CFG_CTNUMDBG Register (Offset = 804h) [reset = 0h]

Counter Timer Number Debug Event Register

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Table 14-26042. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2804h**

Figure 14-8586. CTSET2_CFG_CTNUMDBG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>RESERVED</td><td colspan="3">NUMEVT</td></tr>
<tr><td colspan="4">R</td><td>NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-26044. CTSET2_CFG_CTNUMDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	NUMEVT	R	0h	Number of input selectors for debug events

14.11.1.2.46 CTSET2_CFG_CTUSERACCCTL Register

1 CTSET2_CFG_CTUSERACCCTL Register (Offset = 808h) [reset = 0h]

Counter Timer User Access Control, can only be written in priviledged mode

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Table 14-26045. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2808h**

Figure 14-8587. CTSET2_CFG_CTUSERACCCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					SECUSER	RUSER	NRUSER
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-26047. CTSET2_CFG_CTUSERACCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
1	RUSER	R/W	0h	Counter functions while system is in Root-User mode
0	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode

14.11.1.2.47 CTSET2_CFG_CTSTMCNTL Register

1 CTSET2_CFG_CTSTMCNTL Register (Offset = 820h) [reset = 0h]

Counter Timer STM Control register

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Table 14-26048. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2820h**

Figure 14-8588. CTSET2_CFG_CTSTMCNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				NUMXPORT			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
NUMXPORT		XPORTACT	CCMPORT	CCMAVAIL	CSMXPORT	SENDOVR	ENBL
R		R	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-26050. CTSET2_CFG_CTSTMCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:6	NUMXPORT	R	0h	The total number of counters designated for export
5	XPORTACT	R	0h	Indicates if a frame is currently being written to the STM.
4	CCMPORT	R/W	0h	SW control of CCM message export
3	CCMAVAIL	R/W	0h	CTSET supports CCM export
2	CSMXPORT	R/W	0h	SW control of CSM message export
1	SENDOVR	R/W	0h	Send overflow data in CSM frame
0	ENBL	R/W	0h	CTSET STM global enable for counter/timer messages

14.11.1.2.48 CTSET2_CFG_CTSTMMSTID Register

1 CTSET2_CFG_CTSTMMSTID Register (Offset = 824h) [reset = 0h]

Counter Timer STM Initiator ID register

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Table 14-26051. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2824h**

Figure 14-8589. CTSET2_CFG_CTSTMMSTID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
MASTID							
R/W							
0h							

Table 14-26053. CTSET2_CFG_CTSTMMSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	MASTID	R/W	0h	HW Initiator ID for System Event module

14.11.1.2.49 CTSET2_CFG_CTSTMINTVL Register

1 CTSET2_CFG_CTSTMINTVL Register (Offset = 828h) [reset = 0h]

Counter Timer STM Interval Register

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Table 14-26054. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2828h**

Figure 14-8590. CTSET2_CFG_CTSTMINTVL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	INTERVAL						
NONE	R/W						
0h	0h						
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26056. CTSET2_CFG_CTSTMINTVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	INTERVAL	R/W	0h	Counter Timer Periodic export interval

14.11.1.2.50 CTSET2_CFG_CTSTMSEL0 Register

1 CTSET2_CFG_CTSTMSEL0 Register (Offset = 82Ch) [reset = 0h]

Counter Timer STM Counter Select Register 0. This Selects Counter 0 to 31

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Table 14-26057. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 282Ch**

Figure 14-8591. CTSET2_CFG_CTSTMSEL0 Name Register

31	30	29	28	27	26	25	24
COUNTSEL							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEL							
R/W							
0h							

Table 14-26059. CTSET2_CFG_CTSTMSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTSEL	R/W	0h	The individual bit is this field indicate whether the corresponding counter value is included in the CSM message generated via the STM interface

14.11.1.2.51 CTSET2_CFG_CTSTMSEL1 Register

1 CTSET2_CFG_CTSTMSEL1 Register (Offset = 830h) [reset = 0h]

Counter Timer STM Counter Select Register 1. This Selects Counter 32 to 63

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Table 14-26060. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2830h**

Figure 14-8592. CTSET2_CFG_CTSTMSEL1 Name Register

31	30	29	28	27	26	25	24
COUNTSEL							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEL							
R/W							
0h							

Table 14-26062. CTSET2_CFG_CTSTMSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTSEL	R/W	0h	The individual bit is this field indicate whether the corresponding counter value is included in the CSM message generated via the STM interface

14.11.1.2.52 CTSET2_CFG_CTINTVLR0 Register

1 CTSET2_CFG_CTINTVLR0 Register (Offset = 840h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26063. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2840h**

Figure 14-8593. CTSET2_CFG_CTINTVLR0 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26065. CTSET2_CFG_CTINTVLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.53 CTSET2_CFG_CTINTVLR1 Register

1 CTSET2_CFG_CTINTVLR1 Register (Offset = 844h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

Return to Summary Table

Table 14-26066. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2844h**

Figure 14-8594. CTSET2_CFG_CTINTVLR1 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26068. CTSET2_CFG_CTINTVLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.54 CTSET2_CFG_CTINTVLR2 Register

1 CTSET2_CFG_CTINTVLR2 Register (Offset = 848h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26069. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2848h**

Figure 14-8595. CTSET2_CFG_CTINTVLR2 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26071. CTSET2_CFG_CTINTVLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.55 CTSET2_CFG_CTINTVLR3 Register

1 CTSET2_CFG_CTINTVLR3 Register (Offset = 84Ch) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26072. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 284Ch**

Figure 14-8596. CTSET2_CFG_CTINTVLR3 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26074. CTSET2_CFG_CTINTVLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.56 CTSET2_CFG_CTINTVLR4 Register

1 CTSET2_CFG_CTINTVLR4 Register (Offset = 850h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

Return to Summary Table

Table 14-26075. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2850h

Figure 14-8597. CTSET2_CFG_CTINTVLR4 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26077. CTSET2_CFG_CTINTVLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.57 CTSET2_CFG_CTINTVLR5 Register

1 CTSET2_CFG_CTINTVLR5 Register (Offset = 854h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26078. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2854h**

Figure 14-8598. CTSET2_CFG_CTINTVLR5 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26080. CTSET2_CFG_CTINTVLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.58 CTSET2_CFG_CTINTVLR6 Register

1 CTSET2_CFG_CTINTVLR6 Register (Offset = 858h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26081. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2858h**

Figure 14-8599. CTSET2_CFG_CTINTVLR6 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26083. CTSET2_CFG_CTINTVLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.59 CTSET2_CFG_CTINTVLR7 Register

1 CTSET2_CFG_CTINTVLR7 Register (Offset = 85Ch) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26084. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 285Ch**

Figure 14-8600. CTSET2_CFG_CTINTVLR7 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26086. CTSET2_CFG_CTINTVLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.60 CTSET2_CFG_CTINTVLR8 Register

1 CTSET2_CFG_CTINTVLR8 Register (Offset = 860h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

Return to Summary Table

Table 14-26087. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2860h**

Figure 14-8601. CTSET2_CFG_CTINTVLR8 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26089. CTSET2_CFG_CTINTVLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.61 CTSET2_CFG_CTINTVLR9 Register

1 CTSET2_CFG_CTINTVLR9 Register (Offset = 864h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26090. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2864h**

Figure 14-8602. CTSET2_CFG_CTINTVLR9 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26092. CTSET2_CFG_CTINTVLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.62 CTSET2_CFG_CTINTVLR10 Register

1 CTSET2_CFG_CTINTVLR10 Register (Offset = 868h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

Return to Summary Table

Table 14-26093. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2868h**

Figure 14-8603. CTSET2_CFG_CTINTVLR10 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26095. CTSET2_CFG_CTINTVLR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.63 CTSET2_CFG_CTINTVLR11 Register

1 CTSET2_CFG_CTINTVLR11 Register (Offset = 86Ch) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

Return to Summary Table

Table 14-26096. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 286Ch**

Figure 14-8604. CTSET2_CFG_CTINTVLR11 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26098. CTSET2_CFG_CTINTVLR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.64 CTSET2_CFG_CTINTVLR12 Register

1 CTSET2_CFG_CTINTVLR12 Register (Offset = 870h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26099. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2870h**

Figure 14-8605. CTSET2_CFG_CTINTVLR12 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26101. CTSET2_CFG_CTINTVLR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.65 CTSET2_CFG_CTINTVLR13 Register

1 CTSET2_CFG_CTINTVLR13 Register (Offset = 874h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26102. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2874h**

Figure 14-8606. CTSET2_CFG_CTINTVLR13 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26104. CTSET2_CFG_CTINTVLR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.66 CTSET2_CFG_CTINTVLR14 Register

1 CTSET2_CFG_CTINTVLR14 Register (Offset = 878h) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

Return to Summary Table

Table 14-26105. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2878h**

Figure 14-8607. CTSET2_CFG_CTINTVLR14 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26107. CTSET2_CFG_CTINTVLR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.67 CTSET2_CFG_CTINTVLR15 Register

1 CTSET2_CFG_CTINTVLR15 Register (Offset = 87Ch) [reset = 0h]

These registers contain the interval match value for the corresponding timers in the CTSET. TINTVLRn are available based on number of timers instantiated.

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Table 14-26108. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 287Ch**

Figure 14-8608. CTSET2_CFG_CTINTVLR15 Name Register

31	30	29	28	27	26	25	24
INTERVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTERVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTERVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTERVAL							
R/W							
0h							

Table 14-26110. CTSET2_CFG_CTINTVLR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTERVAL	R/W	0h	Interval match value for the timers in the CTSET

14.11.1.2.68 CTSET2_CFG_CTDBGSGL0 Register

1 CTSET2_CFG_CTDBGSGL0 Register (Offset = 8A0h) [reset = 0h]

Timer Interval Register 0. Interval match value for timer 0 in CTSET Timer Interval Register 1. Interval match value for timer 1 in CTSET Timer Interval Register 2. Interval match value for timer 2 in CTSET Timer Interval Register 3. Interval match value for timer 3 in CTSET Timer Interval Register 4. Interval match value for timer 4 in CTSET Timer Interval Register 5. Interval match value for timer 5 in CTSET Timer Interval Register 6. Interval match value for timer 6 in CTSET Timer Interval Register 7. Interval match value for timer 7 in CTSET Timer Interval Register 8. Interval match value for timer 8 in CTSET Timer Interval Register 9. Interval match value for timer 9 in CTSET Timer Interval Register 10. Interval match value for timer 10 in CTSET Timer Interval Register 11. Interval match value for timer 11 in CTSET Timer Interval Register 12. Interval match value for timer 12 in CTSET Timer Interval Register 13. Interval match value for timer 13 in CTSET Timer Interval Register 14. Interval match value for timer 14 in CTSET Timer Interval Register 15. Interval match value for timer 15 in CTSET Counter Timer Debug Event Register 0

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Table 14-26111. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28A0h**

Figure 14-8609. CTSET2_CFG_CTDBGSGL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-26113. CTSET2_CFG_CTDBGSGL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.11.1.2.69 CTSET2_CFG_CTDBGSGL1 Register

1 CTSET2_CFG_CTDBGSGL1 Register (Offset = 8A4h) [reset = 0h]

Counter Timer Debug Event Register 1

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Table 14-26114. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28A4h**

Figure 14-8610. CTSET2_CFG_CTDBGSGL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-26116. CTSET2_CFG_CTDBGSGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.11.1.2.70 CTSET2_CFG_CTDBGSGL2 Register

1 CTSET2_CFG_CTDBGSGL2 Register (Offset = 8A8h) [reset = 0h]

Counter Timer Debug Event Register 2

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Table 14-26117. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28A8h**

Figure 14-8611. CTSET2_CFG_CTDBGSGL2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-26119. CTSET2_CFG_CTDBGSGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.11.1.2.71 CTSET2_CFG_CTDBGSGL3 Register

1 CTSET2_CFG_CTDBGSGL3 Register (Offset = 8ACh) [reset = 0h]

Counter Timer Debug Event Register 3

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Table 14-26120. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28ACh**

Figure 14-8612. CTSET2_CFG_CTDBGSGL3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-26122. CTSET2_CFG_CTDBGSGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.11.1.2.72 CTSET2_CFG_CTDBGSGL4 Register

1 CTSET2_CFG_CTDBGSGL4 Register (Offset = 8B0h) [reset = 0h]

Counter Timer Debug Event Register 4

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Table 14-26123. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28B0h**

Figure 14-8613. CTSET2_CFG_CTDBGSGL4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPSEL							
R/W							
0h							

Table 14-26125. CTSET2_CFG_CTDBGSGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.11.1.2.73 CTSET2_CFG_CTDBGSGL5 Register

1 CTSET2_CFG_CTDBGSGL5 Register (Offset = 8B4h) [reset = 0h]

Counter Timer Debug Event Register5

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Table 14-26126. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28B4h**

Figure 14-8614. CTSET2_CFG_CTDBGSGL5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-26128. CTSET2_CFG_CTDBGSGL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.11.1.2.74 CTSET2_CFG_CTDBGSGL6 Register

1 CTSET2_CFG_CTDBGSGL6 Register (Offset = 8B8h) [reset = 0h]

Counter Timer Debug Event Register 6

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Table 14-26129. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28B8h**

Figure 14-8615. CTSET2_CFG_CTDBGSGL6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26131. CTSET2_CFG_CTDBGSGL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.11.1.2.75 CTSET2_CFG_CTDBGSGL7 Register

1 CTSET2_CFG_CTDBGSGL7 Register (Offset = 8BCh) [reset = 0h]

Counter Timer Debug Event Register 7

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Table 14-26132. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 28BCh**

Figure 14-8616. CTSET2_CFG_CTDBGSGL7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-26134. CTSET2_CFG_CTDBGSGL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.11.1.2.76 CTSET2_CFG_CTGNBL0 Register

1 CTSET2_CFG_CTGNBL0 Register (Offset = 9F0h) [reset = 0h]

Counter Timer Global Enable Register 0. This enables Counter 0 to 31

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Table 14-26135. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 29F0h**

Figure 14-8617. CTSET2_CFG_CTGNBL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENABLE							
R/W							
0h							

Table 14-26137. CTSET2_CFG_CTGNBL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENABLE	R/W	0h	The individual bit is this field enables the corresponding counter. Bits 30 and 31 will be high if global time stamp output interface is enabled

14.11.1.2.77 CTSET2_CFG_CTGNBL1 Register

1 CTSET2_CFG_CTGNBL1 Register (Offset = 9F4h) [reset = 0h]

Counter Timer Global Enable Register 1. This enables Counter 32 to 63

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Table 14-26138. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 29F4h**

Figure 14-8618. CTSET2_CFG_CTGNBL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ENABLE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26140. CTSET2_CFG_CTGNBL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENABLE	R/W	0h	The individual bit is this field enables the corresponding counter

14.11.1.2.78 CTSET2_CFG_CTGRST0 Register

1 CTSET2_CFG_CTGRST0 Register (Offset = 9F8h) [reset = 0h]

Counter Timer Global Reset Register 0. This resets Counter 0 to 31

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Table 14-26141. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 29F8h**

Figure 14-8619. CTSET2_CFG_CTGRST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESET							
R/W							
0h							

Table 14-26143. CTSET2_CFG_CTGRST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RESET	R/W	0h	The individual bit is this field resets the corresponding counter. These bits are self-clearing, once a '1' is written, after the counters are reset these bits are cleared. When Global Time Stamp output interface is enabled, counter 31 and counter 30 should not be written to any value

14.11.1.2.79 CTSET2_CFG_CTGRST1 Register

1 CTSET2_CFG_CTGRST1 Register (Offset = 9FCh) [reset = 0h]

Counter Timer Global Reset Register 0. This resets Counter 32 to 63

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Table 14-26144. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 29FCh**

Figure 14-8620. CTSET2_CFG_CTGRST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESET							
R/W							
0h							

Table 14-26146. CTSET2_CFG_CTGRST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RESET	R/W	0h	The individual bit is this field resets the corresponding counter. These bits are self-clearing, once a '1' is written, after the counters are reset these bits are cleared.

14.11.1.2.80 CTSET2_CFG_CTCR0 Register

1 CTSET2_CFG_CTCR0 Register (Offset = A00h) [reset = 0h]

Counter Timer Control Register 0

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Table 14-26147. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A00h**

Figure 14-8621. CTSET2_CFG_CTCR0 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26149. CTSET2_CFG_CTCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26149. CTSET2_CFG_CTCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.81 CTSET2_CFG_CTCR1 Register

1 CTSET2_CFG_CTCR1 Register (Offset = A04h) [reset = 0h]

Counter Timer Control Register 1

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Table 14-26150. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A04h**

Figure 14-8622. CTSET2_CFG_CTCR1 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26152. CTSET2_CFG_CTCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26152. CTSET2_CFG_CTCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.82 CTSET2_CFG_CTCR2 Register

1 CTSET2_CFG_CTCR2 Register (Offset = A08h) [reset = 0h]

Counter Timer Control Register 2

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Table 14-26153. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A08h**

Figure 14-8623. CTSET2_CFG_CTCR2 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26155. CTSET2_CFG_CTCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26155. CTSET2_CFG_CTCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.83 CTSET2_CFG_CTCR3 Register

1 CTSET2_CFG_CTCR3 Register (Offset = A0Ch) [reset = 0h]

Counter Timer Control Register 3

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Table 14-26156. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A0Ch**

Figure 14-8624. CTSET2_CFG_CTCR3 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26158. CTSET2_CFG_CTCR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26158. CTSET2_CFG_CTCR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.84 CTSET2_CFG_CTCR4 Register

1 CTSET2_CFG_CTCR4 Register (Offset = A10h) [reset = 0h]

Counter Timer Control Register 4

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Table 14-26159. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A10h**

Figure 14-8625. CTSET2_CFG_CTCR4 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26161. CTSET2_CFG_CTCR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26161. CTSET2_CFG_CTCR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.85 CTSET2_CFG_CTCR5 Register

1 CTSET2_CFG_CTCR5 Register (Offset = A14h) [reset = 0h]

Counter Timer Control Register 5

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Table 14-26162. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A14h**

Figure 14-8626. CTSET2_CFG_CTCR5 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26164. CTSET2_CFG_CTCR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26164. CTSET2_CFG_CTCR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.86 CTSET2_CFG_CTCR6 Register

1 CTSET2_CFG_CTCR6 Register (Offset = A18h) [reset = 0h]

Counter Timer Control Register 6

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Table 14-26165. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A18h**

Figure 14-8627. CTSET2_CFG_CTCR6 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26167. CTSET2_CFG_CTCR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26167. CTSET2_CFG_CTCR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.87 CTSET2_CFG_CTCR7 Register

1 CTSET2_CFG_CTCR7 Register (Offset = A1Ch) [reset = 0h]

Counter Timer Control Register 7

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Table 14-26168. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A1Ch**

Figure 14-8628. CTSET2_CFG_CTCR7 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							

23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							

15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26170. CTSET2_CFG_CTCR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26170. CTSET2_CFG_CTCR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.88 CTSET2_CFG_CTCR8 Register

1 CTSET2_CFG_CTCR8 Register (Offset = A20h) [reset = 0h]

Counter Timer Control Register 8

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Table 14-26171. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A20h**

Figure 14-8629. CTSET2_CFG_CTCR8 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26173. CTSET2_CFG_CTCR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26173. CTSET2_CFG_CTCR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.89 CTSET2_CFG_CTCR9 Register

1 CTSET2_CFG_CTCR9 Register (Offset = A24h) [reset = 0h]

Counter Timer Control Register 9

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Table 14-26174. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A24h**

Figure 14-8630. CTSET2_CFG_CTCR9 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26176. CTSET2_CFG_CTCR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26176. CTSET2_CFG_CTCR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.90 CTSET2_CFG_CTCR10 Register

1 CTSET2_CFG_CTCR10 Register (Offset = A28h) [reset = 0h]

Counter Timer Control Register 10

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Table 14-26177. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A28h**

Figure 14-8631. CTSET2_CFG_CTCR10 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26179. CTSET2_CFG_CTCR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26179. CTSET2_CFG_CTCR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.91 CTSET2_CFG_CTCR11 Register

1 CTSET2_CFG_CTCR11 Register (Offset = A2Ch) [reset = 0h]

Counter Timer Control Register 11

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Table 14-26180. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A2Ch**

Figure 14-8632. CTSET2_CFG_CTCR11 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26182. CTSET2_CFG_CTCR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26182. CTSET2_CFG_CTCR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.92 CTSET2_CFG_CTCR12 Register

1 CTSET2_CFG_CTCR12 Register (Offset = A30h) [reset = 0h]

Counter Timer Control Register 12

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Table 14-26183. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A30h**

Figure 14-8633. CTSET2_CFG_CTCR12 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26185. CTSET2_CFG_CTCR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26185. CTSET2_CFG_CTCR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.93 CTSET2_CFG_CTCR13 Register

1 CTSET2_CFG_CTCR13 Register (Offset = A34h) [reset = 0h]

Counter Timer Control Register 13

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Table 14-26186. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A34h**

Figure 14-8634. CTSET2_CFG_CTCR13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-26188. CTSET2_CFG_CTCR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26188. CTSET2_CFG_CTCR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.94 CTSET2_CFG_CTCR14 Register

1 CTSET2_CFG_CTCR14 Register (Offset = A38h) [reset = 0h]

Counter Timer Control Register 14

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Table 14-26189. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A38h**

Figure 14-8635. CTSET2_CFG_CTCR14 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26191. CTSET2_CFG_CTCR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26191. CTSET2_CFG_CTCR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.95 CTSET2_CFG_CTCR15 Register

1 CTSET2_CFG_CTCR15 Register (Offset = A3Ch) [reset = 0h]

Counter Timer Control Register 15

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Table 14-26192. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A3Ch**

Figure 14-8636. CTSET2_CFG_CTCR15 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26194. CTSET2_CFG_CTCR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26194. CTSET2_CFG_CTCR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.96 CTSET2_CFG_CTCR16 Register

1 CTSET2_CFG_CTCR16 Register (Offset = A40h) [reset = 0h]

Counter Timer Control Register 16

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Table 14-26195. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A40h**

Figure 14-8637. CTSET2_CFG_CTCR16 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26197. CTSET2_CFG_CTCR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26197. CTSET2_CFG_CTCR16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.97 CTSET2_CFG_CTCR17 Register

1 CTSET2_CFG_CTCR17 Register (Offset = A44h) [reset = 0h]

Counter Timer Control Register 17

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Table 14-26198. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A44h**

Figure 14-8638. CTSET2_CFG_CTCR17 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26200. CTSET2_CFG_CTCR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26200. CTSET2_CFG_CTCR17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.98 CTSET2_CFG_CTCR18 Register

1 CTSET2_CFG_CTCR18 Register (Offset = A48h) [reset = 0h]

Counter Timer Control Register 18

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Table 14-26201. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A48h**

Figure 14-8639. CTSET2_CFG_CTCR18 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26203. CTSET2_CFG_CTCR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26203. CTSET2_CFG_CTCR18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.99 CTSET2_CFG_CTCR19 Register

1 CTSET2_CFG_CTCR19 Register (Offset = A4Ch) [reset = 0h]

Counter Timer Control Register 19

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Table 14-26204. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A4Ch**

Figure 14-8640. CTSET2_CFG_CTCR19 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26206. CTSET2_CFG_CTCR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26206. CTSET2_CFG_CTCR19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.100 CTSET2_CFG_CTCR20 Register

1 CTSET2_CFG_CTCR20 Register (Offset = A50h) [reset = 0h]

Counter Timer Control Register 20

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Table 14-26207. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A50h**

Figure 14-8641. CTSET2_CFG_CTCR20 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26209. CTSET2_CFG_CTCR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26209. CTSET2_CFG_CTCR20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.101 CTSET2_CFG_CTCR21 Register

1 CTSET2_CFG_CTCR21 Register (Offset = A54h) [reset = 0h]

Counter Timer Control Register 21

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Table 14-26210. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A54h**

Figure 14-8642. CTSET2_CFG_CTCR21 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26212. CTSET2_CFG_CTCR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26212. CTSET2_CFG_CTCR21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.102 CTSET2_CFG_CTCR22 Register

1 CTSET2_CFG_CTCR22 Register (Offset = A58h) [reset = 0h]

Counter Timer Control Register 22

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Table 14-26213. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A58h**

Figure 14-8643. CTSET2_CFG_CTCR22 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26215. CTSET2_CFG_CTCR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26215. CTSET2_CFG_CTCR22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.103 CTSET2_CFG_CTCR23 Register

1 CTSET2_CFG_CTCR23 Register (Offset = A5Ch) [reset = 0h]

Counter Timer Control Register 23

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Table 14-26216. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A5Ch**

Figure 14-8644. CTSET2_CFG_CTCR23 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26218. CTSET2_CFG_CTCR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26218. CTSET2_CFG_CTCR23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.104 CTSET2_CFG_CTCR24 Register

1 CTSET2_CFG_CTCR24 Register (Offset = A60h) [reset = 0h]

Counter Timer Control Register 24

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Table 14-26219. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A60h**

Figure 14-8645. CTSET2_CFG_CTCR24 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26221. CTSET2_CFG_CTCR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26221. CTSET2_CFG_CTCR24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.105 CTSET2_CFG_CTCR25 Register

1 CTSET2_CFG_CTCR25 Register (Offset = A64h) [reset = 0h]

Counter Timer Control Register 25

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Table 14-26222. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A64h**

Figure 14-8646. CTSET2_CFG_CTCR25 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26224. CTSET2_CFG_CTCR25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26224. CTSET2_CFG_CTCR25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.106 CTSET2_CFG_CTCR26 Register

1 CTSET2_CFG_CTCR26 Register (Offset = A68h) [reset = 0h]

Counter Timer Control Register 26

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Table 14-26225. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2A68h

Figure 14-8647. CTSET2_CFG_CTCR26 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26227. CTSET2_CFG_CTCR26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26227. CTSET2_CFG_CTCR26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.107 CTSET2_CFG_CTCR27 Register

1 CTSET2_CFG_CTCR27 Register (Offset = A6Ch) [reset = 0h]

Counter Timer Control Register 27

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Table 14-26228. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A6Ch**

Figure 14-8648. CTSET2_CFG_CTCR27 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26230. CTSET2_CFG_CTCR27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26230. CTSET2_CFG_CTCR27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.108 CTSET2_CFG_CTCR28 Register

1 CTSET2_CFG_CTCR28 Register (Offset = A70h) [reset = 0h]

Counter Timer Control Register 28

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Table 14-26231. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2A70h

Figure 14-8649. CTSET2_CFG_CTCR28 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26233. CTSET2_CFG_CTCR28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26233. CTSET2_CFG_CTCR28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.109 CTSET2_CFG_CTCR29 Register

1 CTSET2_CFG_CTCR29 Register (Offset = A74h) [reset = 0h]

Counter Timer Control Register 29

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Table 14-26234. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A74h**

Figure 14-8650. CTSET2_CFG_CTCR29 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							

23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							

15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26236. CTSET2_CFG_CTCR29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26236. CTSET2_CFG_CTCR29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.110 CTSET2_CFG_CTCR30 Register

1 CTSET2_CFG_CTCR30 Register (Offset = A78h) [reset = 0h]

Counter Timer Control Register 30

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Table 14-26237. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A78h**

Figure 14-8651. CTSET2_CFG_CTCR30 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26239. CTSET2_CFG_CTCR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26239. CTSET2_CFG_CTCR30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.111 CTSET2_CFG_CTCR31 Register

1 CTSET2_CFG_CTCR31 Register (Offset = A7Ch) [reset = 0h]

Counter Timer Control Register 31

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Table 14-26240. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A7Ch**

Figure 14-8652. CTSET2_CFG_CTCR31 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-26242. CTSET2_CFG_CTCR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-26242. CTSET2_CFG_CTCR31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.11.1.2.112 CTSET2_CFG_CTOWN0 Register

1 CTSET2_CFG_CTOWN0 Register (Offset = A80h) [reset = 20000000h]

Counter/Timer Ownership register 0

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Table 14-26243. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A80h**

Figure 14-8653. CTSET2_CFG_CTOWN0 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26245. CTSET2_CFG_CTOWN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.113 CTSET2_CFG_CTOWN1 Register

1 CTSET2_CFG_CTOWN1 Register (Offset = A84h) [reset = 20000000h]

Counter/Timer Ownership register 1

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Table 14-26246. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A84h**

Figure 14-8654. CTSET2_CFG_CTOWN1 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26248. CTSET2_CFG_CTOWN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.114 CTSET2_CFG_CTOWN2 Register

1 CTSET2_CFG_CTOWN2 Register (Offset = A88h) [reset = 20000000h]

Counter/Timer Ownership register 2

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Table 14-26249. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 2A88h**

Figure 14-8655. CTSET2_CFG_CTOWN2 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-26251. CTSET2_CFG_CTOWN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.115 CTSET2_CFG_CTOWN3 Register

1 CTSET2_CFG_CTOWN3 Register (Offset = A8Ch) [reset = 20000000h]

Counter/Timer Ownership register 3

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Table 14-26252. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 2A8Ch**

Figure 14-8656. CTSET2_CFG_CTOWN3 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26254. CTSET2_CFG_CTOWN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.116 CTSET2_CFG_CTOWN4 Register

1 CTSET2_CFG_CTOWN4 Register (Offset = A90h) [reset = 20000000h]

Counter/Timer Ownership register 4

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Table 14-26255. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A90h**

Figure 14-8657. CTSET2_CFG_CTOWN4 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26257. CTSET2_CFG_CTOWN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.117 CTSET2_CFG_CTOWN5 Register

1 CTSET2_CFG_CTOWN5 Register (Offset = A94h) [reset = 20000000h]

Counter/Timer Ownership register 5

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Table 14-26258. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A94h**

Figure 14-8658. CTSET2_CFG_CTOWN5 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-26260. CTSET2_CFG_CTOWN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.118 CTSET2_CFG_CTOWN6 Register

1 CTSET2_CFG_CTOWN6 Register (Offset = A98h) [reset = 20000000h]

Counter/Timer Ownership register 6

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Table 14-26261. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A98h**

Figure 14-8659. CTSET2_CFG_CTOWN6 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-26263. CTSET2_CFG_CTOWN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.119 CTSET2_CFG_CTOWN7 Register

1 CTSET2_CFG_CTOWN7 Register (Offset = A9Ch) [reset = 20000000h]

Counter/Timer Ownership register 7

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Table 14-26264. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2A9Ch**

Figure 14-8660. CTSET2_CFG_CTOWN7 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26266. CTSET2_CFG_CTOWN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.120 CTSET2_CFG_CTOWN8 Register

1 CTSET2_CFG_CTOWN8 Register (Offset = AA0h) [reset = 20000000h]

Counter/Timer Ownership register 8

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Table 14-26267. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AA0h**

Figure 14-8661. CTSET2_CFG_CTOWN8 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-26269. CTSET2_CFG_CTOWN8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.121 CTSET2_CFG_CTOWN9 Register

1 CTSET2_CFG_CTOWN9 Register (Offset = AA4h) [reset = 20000000h]

Counter/Timer Ownership register 9

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Table 14-26270. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AA4h**

Figure 14-8662. CTSET2_CFG_CTOWN9 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26272. CTSET2_CFG_CTOWN9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.122 CTSET2_CFG_CTOWN10 Register

1 CTSET2_CFG_CTOWN10 Register (Offset = AA8h) [reset = 20000000h]

Counter/Timer Ownership register 10

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Table 14-26273. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AA8h**

Figure 14-8663. CTSET2_CFG_CTOWN10 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26275. CTSET2_CFG_CTOWN10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.123 CTSET2_CFG_CTOWN11 Register

1 CTSET2_CFG_CTOWN11 Register (Offset = AACh) [reset = 20000000h]

Counter/Timer Ownership register 11

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Table 14-26276. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AACh**

Figure 14-8664. CTSET2_CFG_CTOWN11 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26278. CTSET2_CFG_CTOWN11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.124 CTSET2_CFG_CTOWN12 Register

1 CTSET2_CFG_CTOWN12 Register (Offset = AB0h) [reset = 20000000h]

Counter/Timer Ownership register 12

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Table 14-26279. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AB0h**

Figure 14-8665. CTSET2_CFG_CTOWN12 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-26281. CTSET2_CFG_CTOWN12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.125 CTSET2_CFG_CTOWN13 Register

1 CTSET2_CFG_CTOWN13 Register (Offset = AB4h) [reset = 20000000h]

Counter/Timer Ownership register 13

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Table 14-26282. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AB4h**

Figure 14-8666. CTSET2_CFG_CTOWN13 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26284. CTSET2_CFG_CTOWN13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.126 CTSET2_CFG_CTOWN14 Register

1 CTSET2_CFG_CTOWN14 Register (Offset = AB8h) [reset = 20000000h]

Counter/Timer Ownership register 14

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Table 14-26285. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AB8h**

Figure 14-8667. CTSET2_CFG_CTOWN14 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26287. CTSET2_CFG_CTOWN14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.127 CTSET2_CFG_CTOWN15 Register

1 CTSET2_CFG_CTOWN15 Register (Offset = ABCh) [reset = 20000000h]

Counter/Timer Ownership register 15

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Table 14-26288. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2ABCh**

Figure 14-8668. CTSET2_CFG_CTOWN15 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-26290. CTSET2_CFG_CTOWN15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.128 CTSET2_CFG_CTOWN16 Register

1 CTSET2_CFG_CTOWN16 Register (Offset = AC0h) [reset = 20000000h]

Counter/Timer Ownership register 16

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Table 14-26291. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 2AC0h**

Figure 14-8669. CTSET2_CFG_CTOWN16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">OWNERSHIP</td><td>DBG_OVERIDE</td><td>CURRENT_OWNER</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td>1h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26293. CTSET2_CFG_CTOWN16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.129 CTSET2_CFG_CTOWN17 Register

1 CTSET2_CFG_CTOWN17 Register (Offset = AC4h) [reset = 20000000h]

Counter/Timer Ownership register 17

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Table 14-26294. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AC4h**

Figure 14-8670. CTSET2_CFG_CTOWN17 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26296. CTSET2_CFG_CTOWN17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.130 CTSET2_CFG_CTOWN18 Register

1 CTSET2_CFG_CTOWN18 Register (Offset = AC8h) [reset = 20000000h]

Counter/Timer Ownership register 18

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Table 14-26297. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AC8h**

Figure 14-8671. CTSET2_CFG_CTOWN18 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26299. CTSET2_CFG_CTOWN18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.131 CTSET2_CFG_CTOWN19 Register

1 CTSET2_CFG_CTOWN19 Register (Offset = ACCh) [reset = 20000000h]

Counter/Timer Ownership register 19

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Table 14-26300. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 2ACCh**

Figure 14-8672. CTSET2_CFG_CTOWN19 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26302. CTSET2_CFG_CTOWN19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.132 CTSET2_CFG_CTOWN20 Register

1 CTSET2_CFG_CTOWN20 Register (Offset = AD0h) [reset = 20000000h]

Counter/Timer Ownership register 20

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Table 14-26303. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AD0h**

Figure 14-8673. CTSET2_CFG_CTOWN20 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-26305. CTSET2_CFG_CTOWN20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.133 CTSET2_CFG_CTOWN21 Register

1 CTSET2_CFG_CTOWN21 Register (Offset = AD4h) [reset = 20000000h]

Counter/Timer Ownership register 21

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Table 14-26306. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AD4h**

Figure 14-8674. CTSET2_CFG_CTOWN21 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26308. CTSET2_CFG_CTOWN21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.134 CTSET2_CFG_CTOWN22 Register

1 CTSET2_CFG_CTOWN22 Register (Offset = AD8h) [reset = 20000000h]

Counter/Timer Ownership register 22

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Table 14-26309. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AD8h**

Figure 14-8675. CTSET2_CFG_CTOWN22 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26311. CTSET2_CFG_CTOWN22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.135 CTSET2_CFG_CTOWN23 Register

1 CTSET2_CFG_CTOWN23 Register (Offset = ADCh) [reset = 20000000h]

Counter/Timer Ownership register2 3

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Table 14-26312. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 2ADCh**

Figure 14-8676. CTSET2_CFG_CTOWN23 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26314. CTSET2_CFG_CTOWN23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.136 CTSET2_CFG_CTOWN24 Register

1 CTSET2_CFG_CTOWN24 Register (Offset = AE0h) [reset = 20000000h]

Counter/Timer Ownership register 24

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Table 14-26315. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AE0h**

Figure 14-8677. CTSET2_CFG_CTOWN24 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26317. CTSET2_CFG_CTOWN24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.137 CTSET2_CFG_CTOWN25 Register

1 CTSET2_CFG_CTOWN25 Register (Offset = AE4h) [reset = 20000000h]

Counter/Timer Ownership register 25

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Table 14-26318. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AE4h**

Figure 14-8678. CTSET2_CFG_CTOWN25 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26320. CTSET2_CFG_CTOWN25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.138 CTSET2_CFG_CTOWN26 Register

1 CTSET2_CFG_CTOWN26 Register (Offset = AE8h) [reset = 20000000h]

Counter/Timer Ownership register 26

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Table 14-26321. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AE8h**

Figure 14-8679. CTSET2_CFG_CTOWN26 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26323. CTSET2_CFG_CTOWN26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.139 CTSET2_CFG_CTOWN27 Register

1 CTSET2_CFG_CTOWN27 Register (Offset = AECh) [reset = 20000000h]

Counter/Timer Ownership register 27

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Table 14-26324. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AECh**

Figure 14-8680. CTSET2_CFG_CTOWN27 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26326. CTSET2_CFG_CTOWN27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.140 CTSET2_CFG_CTOWN28 Register

1 CTSET2_CFG_CTOWN28 Register (Offset = AF0h) [reset = 20000000h]

Counter/Timer Ownership register 28

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Table 14-26327. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AF0h**

Figure 14-8681. CTSET2_CFG_CTOWN28 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-26329. CTSET2_CFG_CTOWN28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.141 CTSET2_CFG_CTOWN29 Register

1 CTSET2_CFG_CTOWN29 Register (Offset = AF4h) [reset = 20000000h]

Counter/Timer Ownership register 29

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Table 14-26330. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 2AF4h**

Figure 14-8682. CTSET2_CFG_CTOWN29 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26332. CTSET2_CFG_CTOWN29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.142 CTSET2_CFG_CTOWN30 Register

1 CTSET2_CFG_CTOWN30 Register (Offset = AF8h) [reset = 20000000h]

Counter/Timer Ownership register 30

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Table 14-26333. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AF8h**

Figure 14-8683. CTSET2_CFG_CTOWN30 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26335. CTSET2_CFG_CTOWN30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.143 CTSET2_CFG_CTOWN31 Register

1 CTSET2_CFG_CTOWN31 Register (Offset = AFCh) [reset = 20000000h]

Counter/Timer Ownership register 31

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Table 14-26336. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2AFCh**

Figure 14-8684. CTSET2_CFG_CTOWN31 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-26338. CTSET2_CFG_CTOWN31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.144 CTSET2_CFG_CTFILT0 Register

1 CTSET2_CFG_CTFILT0 Register (Offset = B00h) [reset = 0h]

Counter Timer 0 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26339. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B00h**

Figure 14-8685. CTSET2_CFG_CTFILT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26341. CTSET2_CFG_CTFILT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.145 CTSET2_CFG_CTFILT1 Register

1 CTSET2_CFG_CTFILT1 Register (Offset = B04h) [reset = 0h]

Counter Timer 1 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26342. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B04h**

Figure 14-8686. CTSET2_CFG_CTFILT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26344. CTSET2_CFG_CTFILT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.146 CTSET2_CFG_CTFILT2 Register

1 CTSET2_CFG_CTFILT2 Register (Offset = B08h) [reset = 0h]

Counter Timer 2 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26345. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B08h

Figure 14-8687. CTSET2_CFG_CTFILT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26347. CTSET2_CFG_CTFILT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.147 CTSET2_CFG_CTFILT3 Register

1 CTSET2_CFG_CTFILT3 Register (Offset = B0Ch) [reset = 0h]

Counter Timer 3 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26348. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B0Ch**

Figure 14-8688. CTSET2_CFG_CTFILT3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26350. CTSET2_CFG_CTFILT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.148 CTSET2_CFG_CTFILT4 Register

1 CTSET2_CFG_CTFILT4 Register (Offset = B10h) [reset = 0h]

Counter Timer 4 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26351. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B10h**

Figure 14-8689. CTSET2_CFG_CTFILT4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26353. CTSET2_CFG_CTFILT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.149 CTSET2_CFG_CTFILT5 Register

1 CTSET2_CFG_CTFILT5 Register (Offset = B14h) [reset = 0h]

Counter Timer 5 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26354. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B14h**

Figure 14-8690. CTSET2_CFG_CTFILT5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26356. CTSET2_CFG_CTFILT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.150 CTSET2_CFG_CTFILT6 Register

1 CTSET2_CFG_CTFILT6 Register (Offset = B18h) [reset = 0h]

Counter Timer 6 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26357. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B18h**

Figure 14-8691. CTSET2_CFG_CTFILT6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26359. CTSET2_CFG_CTFILT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.151 CTSET2_CFG_CTFILT7 Register

1 CTSET2_CFG_CTFILT7 Register (Offset = B1Ch) [reset = 0h]

Counter Timer 7 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26360. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B1Ch**

Figure 14-8692. CTSET2_CFG_CTFILT7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26362. CTSET2_CFG_CTFILT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.152 CTSET2_CFG_CTFILT8 Register

1 CTSET2_CFG_CTFILT8 Register (Offset = B20h) [reset = 0h]

Counter Timer 8 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26363. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B20h**

Figure 14-8693. CTSET2_CFG_CTFILT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26365. CTSET2_CFG_CTFILT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.153 CTSET2_CFG_CTFILT9 Register

1 CTSET2_CFG_CTFILT9 Register (Offset = B24h) [reset = 0h]

Counter Timer 9 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26366. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B24h**

Figure 14-8694. CTSET2_CFG_CTFILT9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26368. CTSET2_CFG_CTFILT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.154 CTSET2_CFG_CTFILT10 Register

1 CTSET2_CFG_CTFILT10 Register (Offset = B28h) [reset = 0h]

Counter Timer 10 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26369. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B28h

Figure 14-8695. CTSET2_CFG_CTFILT10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26371. CTSET2_CFG_CTFILT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.155 CTSET2_CFG_CTFILT11 Register

1 CTSET2_CFG_CTFILT11 Register (Offset = B2Ch) [reset = 0h]

Counter Timer 11 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26372. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B2Ch**

Figure 14-8696. CTSET2_CFG_CTFILT11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26374. CTSET2_CFG_CTFILT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.156 CTSET2_CFG_CTFILT12 Register

1 CTSET2_CFG_CTFILT12 Register (Offset = B30h) [reset = 0h]

Counter Timer 12 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26375. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B30h**

Figure 14-8697. CTSET2_CFG_CTFILT12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26377. CTSET2_CFG_CTFILT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.157 CTSET2_CFG_CTFILT13 Register

1 CTSET2_CFG_CTFILT13 Register (Offset = B34h) [reset = 0h]

Counter Timer 13 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26378. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B34h**

Figure 14-8698. CTSET2_CFG_CTFILT13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26380. CTSET2_CFG_CTFILT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.158 CTSET2_CFG_CTFILT14 Register

1 CTSET2_CFG_CTFILT14 Register (Offset = B38h) [reset = 0h]

Counter Timer 14 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26381. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B38h**

Figure 14-8699. CTSET2_CFG_CTFILT14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26383. CTSET2_CFG_CTFILT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.159 CTSET2_CFG_CTFILT15 Register

1 CTSET2_CFG_CTFILT15 Register (Offset = B3Ch) [reset = 0h]

Counter Timer 15 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26384. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B3Ch

Figure 14-8700. CTSET2_CFG_CTFILT15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26386. CTSET2_CFG_CTFILT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.160 CTSET2_CFG_CTFILT16 Register

1 CTSET2_CFG_CTFILT16 Register (Offset = B40h) [reset = 0h]

Counter Timer 16 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26387. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B40h

Figure 14-8701. CTSET2_CFG_CTFILT16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26389. CTSET2_CFG_CTFILT16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.161 CTSET2_CFG_CTFILT17 Register

1 CTSET2_CFG_CTFILT17 Register (Offset = B44h) [reset = 0h]

Counter Timer 17 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26390. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B44h

Figure 14-8702. CTSET2_CFG_CTFILT17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26392. CTSET2_CFG_CTFILT17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.162 CTSET2_CFG_CTFILT18 Register

1 CTSET2_CFG_CTFILT18 Register (Offset = B48h) [reset = 0h]

Counter Timer 18 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26393. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B48h**

Figure 14-8703. CTSET2_CFG_CTFILT18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26395. CTSET2_CFG_CTFILT18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.163 CTSET2_CFG_CTFILT19 Register

1 CTSET2_CFG_CTFILT19 Register (Offset = B4Ch) [reset = 0h]

Counter Timer 19 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26396. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B4Ch**

Figure 14-8704. CTSET2_CFG_CTFILT19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26398. CTSET2_CFG_CTFILT19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.164 CTSET2_CFG_CTFILT20 Register

1 CTSET2_CFG_CTFILT20 Register (Offset = B50h) [reset = 0h]

Counter Timer 20 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26399. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B50h**

Figure 14-8705. CTSET2_CFG_CTFILT20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26401. CTSET2_CFG_CTFILT20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.165 CTSET2_CFG_CTFILT21 Register

1 CTSET2_CFG_CTFILT21 Register (Offset = B54h) [reset = 0h]

Counter Timer 21 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26402. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B54h**

Figure 14-8706. CTSET2_CFG_CTFILT21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26404. CTSET2_CFG_CTFILT21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.166 CTSET2_CFG_CTFILT22 Register

1 CTSET2_CFG_CTFILT22 Register (Offset = B58h) [reset = 0h]

Counter Timer 22 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26405. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B58h

Figure 14-8707. CTSET2_CFG_CTFILT22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26407. CTSET2_CFG_CTFILT22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.167 CTSET2_CFG_CTFILT23 Register

1 CTSET2_CFG_CTFILT23 Register (Offset = B5Ch) [reset = 0h]

Counter Timer 23 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26408. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B5Ch**

Figure 14-8708. CTSET2_CFG_CTFILT23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26410. CTSET2_CFG_CTFILT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.168 CTSET2_CFG_CTFILT24 Register

1 CTSET2_CFG_CTFILT24 Register (Offset = B60h) [reset = 0h]

Counter Timer 24 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26411. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B60h**

Figure 14-8709. CTSET2_CFG_CTFILT24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26413. CTSET2_CFG_CTFILT24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.169 CTSET2_CFG_CTFILT25 Register

1 CTSET2_CFG_CTFILT25 Register (Offset = B64h) [reset = 0h]

Counter Timer 25 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26414. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B64h

Figure 14-8710. CTSET2_CFG_CTFILT25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26416. CTSET2_CFG_CTFILT25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.170 CTSET2_CFG_CTFILT26 Register

1 CTSET2_CFG_CTFILT26 Register (Offset = B68h) [reset = 0h]

Counter Timer 26 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26417. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B68h**

Figure 14-8711. CTSET2_CFG_CTFILT26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26419. CTSET2_CFG_CTFILT26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.171 CTSET2_CFG_CTFILT27 Register

1 CTSET2_CFG_CTFILT27 Register (Offset = B6Ch) [reset = 0h]

Counter Timer 27 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26420. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 2B6Ch

Figure 14-8712. CTSET2_CFG_CTFILT27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26422. CTSET2_CFG_CTFILT27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.172 CTSET2_CFG_CTFILT28 Register

1 CTSET2_CFG_CTFILT28 Register (Offset = B70h) [reset = 0h]

Counter Timer 28 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26423. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B70h**

Figure 14-8713. CTSET2_CFG_CTFILT28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26425. CTSET2_CFG_CTFILT28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.173 CTSET2_CFG_CTFILT29 Register

1 CTSET2_CFG_CTFILT29 Register (Offset = B74h) [reset = 0h]

Counter Timer 29 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26426. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B74h**

Figure 14-8714. CTSET2_CFG_CTFILT29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26428. CTSET2_CFG_CTFILT29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.174 CTSET2_CFG_CTFILT30 Register

1 CTSET2_CFG_CTFILT30 Register (Offset = B78h) [reset = 0h]

Counter Timer 30 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26429. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B78h**

Figure 14-8715. CTSET2_CFG_CTFILT30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26431. CTSET2_CFG_CTFILT30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.175 CTSET2_CFG_CTFILT31 Register

1 CTSET2_CFG_CTFILT31 Register (Offset = B7Ch) [reset = 0h]

Counter Timer 31 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-26432. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B7Ch**

Figure 14-8716. CTSET2_CFG_CTFILT31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26434. CTSET2_CFG_CTFILT31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.11.1.2.176 CTSET2_CFG_CTCNTR0 Register

1 CTSET2_CFG_CTCNTR0 Register (Offset = B80h) [reset = 0h]

Counter Timer Counter Register 0

Return to Summary Table

Table 14-26435. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B80h**

Figure 14-8717. CTSET2_CFG_CTCNTR0 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26437. CTSET2_CFG_CTCNTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.177 CTSET2_CFG_CTCNTR1 Register

1 CTSET2_CFG_CTCNTR1 Register (Offset = B84h) [reset = 0h]

Counter Timer Counter Register 1

Return to Summary Table

Table 14-26438. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B84h**

Figure 14-8718. CTSET2_CFG_CTCNTR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26440. CTSET2_CFG_CTCNTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.178 CTSET2_CFG_CTCNTR2 Register

1 CTSET2_CFG_CTCNTR2 Register (Offset = B88h) [reset = 0h]

Counter Timer Counter Register 2

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Table 14-26441. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B88h**

Figure 14-8719. CTSET2_CFG_CTCNTR2 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26443. CTSET2_CFG_CTCNTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.179 CTSET2_CFG_CTCNTR3 Register

1 CTSET2_CFG_CTCNTR3 Register (Offset = B8Ch) [reset = 0h]

Counter Timer Counter Register 3

Return to Summary Table

Table 14-26444. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B8Ch**

Figure 14-8720. CTSET2_CFG_CTCNTR3 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26446. CTSET2_CFG_CTCNTR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.180 CTSET2_CFG_CTCNTR4 Register

1 CTSET2_CFG_CTCNTR4 Register (Offset = B90h) [reset = 0h]

Counter Timer Counter Register 4

Return to Summary Table

Table 14-26447. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B90h**

Figure 14-8721. CTSET2_CFG_CTCNTR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26449. CTSET2_CFG_CTCNTR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.181 CTSET2_CFG_CTCNTR5 Register

1 CTSET2_CFG_CTCNTR5 Register (Offset = B94h) [reset = 0h]

Counter Timer Counter Register 5

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Table 14-26450. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B94h**

Figure 14-8722. CTSET2_CFG_CTCNTR5 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 14-26452. CTSET2_CFG_CTCNTR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.182 CTSET2_CFG_CTCNTR6 Register

1 CTSET2_CFG_CTCNTR6 Register (Offset = B98h) [reset = 0h]

Counter Timer Counter Register 6

Return to Summary Table

Table 14-26453. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B98h**

Figure 14-8723. CTSET2_CFG_CTCNTR6 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26455. CTSET2_CFG_CTCNTR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.183 CTSET2_CFG_CTCNTR7 Register

1 CTSET2_CFG_CTCNTR7 Register (Offset = B9Ch) [reset = 0h]

Counter Timer Counter Register 7

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Table 14-26456. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2B9Ch**

Figure 14-8724. CTSET2_CFG_CTCNTR7 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26458. CTSET2_CFG_CTCNTR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.184 CTSET2_CFG_CTCNTR8 Register

1 CTSET2_CFG_CTCNTR8 Register (Offset = BA0h) [reset = 0h]

Counter Timer Counter Register 8

Return to Summary Table

Table 14-26459. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BA0h**

Figure 14-8725. CTSET2_CFG_CTCNTR8 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26461. CTSET2_CFG_CTCNTR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.185 CTSET2_CFG_CTCNTR9 Register

1 CTSET2_CFG_CTCNTR9 Register (Offset = BA4h) [reset = 0h]

Counter Timer Counter Register 9

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Table 14-26462. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BA4h**

Figure 14-8726. CTSET2_CFG_CTCNTR9 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26464. CTSET2_CFG_CTCNTR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.186 CTSET2_CFG_CTCNTR10 Register

1 CTSET2_CFG_CTCNTR10 Register (Offset = BA8h) [reset = 0h]

Counter Timer Counter Register 10

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Table 14-26465. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BA8h**

Figure 14-8727. CTSET2_CFG_CTCNTR10 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26467. CTSET2_CFG_CTCNTR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.187 CTSET2_CFG_CTCNTR11 Register

1 CTSET2_CFG_CTCNTR11 Register (Offset = BACh) [reset = 0h]

Counter Timer Counter Register 11

Return to Summary Table

Table 14-26468. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BACh**

Figure 14-8728. CTSET2_CFG_CTCNTR11 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26470. CTSET2_CFG_CTCNTR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.188 CTSET2_CFG_CTCNTR12 Register

1 CTSET2_CFG_CTCNTR12 Register (Offset = BB0h) [reset = 0h]

Counter Timer Counter Register 12

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Table 14-26471. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BB0h**

Figure 14-8729. CTSET2_CFG_CTCNTR12 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26473. CTSET2_CFG_CTCNTR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.189 CTSET2_CFG_CTCNTR13 Register

1 CTSET2_CFG_CTCNTR13 Register (Offset = BB4h) [reset = 0h]

Counter Timer Counter Register 13

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Table 14-26474. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BB4h**

Figure 14-8730. CTSET2_CFG_CTCNTR13 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26476. CTSET2_CFG_CTCNTR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.190 CTSET2_CFG_CTCNTR14 Register

1 CTSET2_CFG_CTCNTR14 Register (Offset = BB8h) [reset = 0h]

Counter Timer Counter Register 14

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Table 14-26477. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BB8h**

Figure 14-8731. CTSET2_CFG_CTCNTR14 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26479. CTSET2_CFG_CTCNTR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.191 CTSET2_CFG_CTCNTR15 Register

1 CTSET2_CFG_CTCNTR15 Register (Offset = BBCh) [reset = 0h]

Counter Timer Counter Register 15

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Table 14-26480. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BBCh**

Figure 14-8732. CTSET2_CFG_CTCNTR15 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26482. CTSET2_CFG_CTCNTR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.192 CTSET2_CFG_CTCNTR16 Register

1 CTSET2_CFG_CTCNTR16 Register (Offset = BC0h) [reset = 0h]

Counter Timer Counter Register 16

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Table 14-26483. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BC0h**

Figure 14-8733. CTSET2_CFG_CTCNTR16 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26485. CTSET2_CFG_CTCNTR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.193 CTSET2_CFG_CTCNTR17 Register

1 CTSET2_CFG_CTCNTR17 Register (Offset = BC4h) [reset = 0h]

Counter Timer Counter Register 17

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Table 14-26486. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BC4h**

Figure 14-8734. CTSET2_CFG_CTCNTR17 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26488. CTSET2_CFG_CTCNTR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.194 CTSET2_CFG_CTCNTR18 Register

1 CTSET2_CFG_CTCNTR18 Register (Offset = BC8h) [reset = 0h]

Counter Timer Counter Register 18

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Table 14-26489. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BC8h**

Figure 14-8735. CTSET2_CFG_CTCNTR18 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26491. CTSET2_CFG_CTCNTR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.195 CTSET2_CFG_CTCNTR19 Register

1 CTSET2_CFG_CTCNTR19 Register (Offset = BCCh) [reset = 0h]

Counter Timer Counter Register 19

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Table 14-26492. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BCCh**

Figure 14-8736. CTSET2_CFG_CTCNTR19 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26494. CTSET2_CFG_CTCNTR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.196 CTSET2_CFG_CTCNTR20 Register

1 CTSET2_CFG_CTCNTR20 Register (Offset = BD0h) [reset = 0h]

Counter Timer Counter Register 20

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Table 14-26495. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BD0h**

Figure 14-8737. CTSET2_CFG_CTCNTR20 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26497. CTSET2_CFG_CTCNTR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.197 CTSET2_CFG_CTCNTR21 Register

1 CTSET2_CFG_CTCNTR21 Register (Offset = BD4h) [reset = 0h]

Counter Timer Counter Register 21

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Table 14-26498. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BD4h**

Figure 14-8738. CTSET2_CFG_CTCNTR21 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26500. CTSET2_CFG_CTCNTR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.198 CTSET2_CFG_CTCNTR22 Register

1 CTSET2_CFG_CTCNTR22 Register (Offset = BD8h) [reset = 0h]

Counter Timer Counter Register 22

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Table 14-26501. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BD8h**

Figure 14-8739. CTSET2_CFG_CTCNTR22 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26503. CTSET2_CFG_CTCNTR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.199 CTSET2_CFG_CTCNTR23 Register

1 CTSET2_CFG_CTCNTR23 Register (Offset = BDCh) [reset = 0h]

Counter Timer Counter Register 23

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Table 14-26504. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BDCh**

Figure 14-8740. CTSET2_CFG_CTCNTR23 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 14-26506. CTSET2_CFG_CTCNTR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.200 CTSET2_CFG_CTCNTR24 Register

1 CTSET2_CFG_CTCNTR24 Register (Offset = BE0h) [reset = 0h]

Counter Timer Counter Register 24

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Table 14-26507. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BE0h**

Figure 14-8741. CTSET2_CFG_CTCNTR24 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26509. CTSET2_CFG_CTCNTR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.201 CTSET2_CFG_CTCNTR25 Register

1 CTSET2_CFG_CTCNTR25 Register (Offset = BE4h) [reset = 0h]

Counter Timer Counter Register 25

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Table 14-26510. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BE4h**

Figure 14-8742. CTSET2_CFG_CTCNTR25 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26512. CTSET2_CFG_CTCNTR25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.202 CTSET2_CFG_CTCNTR26 Register

1 CTSET2_CFG_CTCNTR26 Register (Offset = BE8h) [reset = 0h]

Counter Timer Counter Register 26

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Table 14-26513. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BE8h**

Figure 14-8743. CTSET2_CFG_CTCNTR26 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 14-26515. CTSET2_CFG_CTCNTR26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.203 CTSET2_CFG_CTCNTR27 Register

1 CTSET2_CFG_CTCNTR27 Register (Offset = BECh) [reset = 0h]

Counter Timer Counter Register 27

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Table 14-26516. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BECh**

Figure 14-8744. CTSET2_CFG_CTCNTR27 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26518. CTSET2_CFG_CTCNTR27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.204 CTSET2_CFG_CTCNTR28 Register

1 CTSET2_CFG_CTCNTR28 Register (Offset = BF0h) [reset = 0h]

Counter Timer Counter Register 28

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Table 14-26519. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BF0h**

Figure 14-8745. CTSET2_CFG_CTCNTR28 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26521. CTSET2_CFG_CTCNTR28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.205 CTSET2_CFG_CTCNTR29 Register

1 CTSET2_CFG_CTCNTR29 Register (Offset = BF4h) [reset = 0h]

Counter Timer Counter Register 29

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Table 14-26522. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BF4h**

Figure 14-8746. CTSET2_CFG_CTCNTR29 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26524. CTSET2_CFG_CTCNTR29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.206 CTSET2_CFG_CTCNTR30 Register

1 CTSET2_CFG_CTCNTR30 Register (Offset = BF8h) [reset = 0h]

Counter Timer Counter Register 30

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Table 14-26525. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BF8h**

Figure 14-8747. CTSET2_CFG_CTCNTR30 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26527. CTSET2_CFG_CTCNTR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.207 CTSET2_CFG_CTCNTR31 Register

1 CTSET2_CFG_CTCNTR31 Register (Offset = BFCh) [reset = 0h]

Counter Timer Counter Register 31

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Table 14-26528. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2BFCh**

Figure 14-8748. CTSET2_CFG_CTCNTR31 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-26530. CTSET2_CFG_CTCNTR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.11.1.2.208 CTSET2_CFG_CT_EOI Register

1 CTSET2_CFG_CT_EOI Register (Offset = C00h) [reset = 0h]

Counter Timer EOI Register. This register is the End of Interrupt used by SW to signal HW that an interrupt event service is complete and an interrupt can be rearmed. This register exists only if NUMTIMR > 0

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Table 14-26531. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C00h**

Figure 14-8749. CTSET2_CFG_CT_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI
R							R/W
0h							0h

Table 14-26533. CTSET2_CFG_CT_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	EOI	R/W	0h	EOI value

14.11.1.2.209 CTSET2_CFG_CTIRQSTAT_RAW Register

1 CTSET2_CFG_CTIRQSTAT_RAW Register (Offset = C04h) [reset = 0h]

Counter Timer IRQSTATUS RAW Register. This register indicates the raw status of the interrupt. It can be written by SW for testing. This register exists only if NUMTIMR > 0

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Table 14-26534. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C04h**

Figure 14-8750. CTSET2_CFG_CTIRQSTAT_RAW Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IRQ							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TIM_INTN_IRQ							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TIM_INTN_IRQ							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIM_INTN_IRQ							
R/W							
0h							

Table 14-26536. CTSET2_CFG_CTIRQSTAT_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IRQ	R/W	0h	IRQSTATUS_RAW value. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.11.1.2.210 CTSET2_CFG_CTIRQSTAT Register

1 CTSET2_CFG_CTIRQSTAT Register (Offset = C08h) [reset = 0h]

Counter Timer IRQSTATUS Register. This bit clears the interrupt event. SW can also read this bit to indicate that the interrupt is active and enabled. This register exists only if NUMTIMR > 0

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Table 14-26537. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C08h**

Figure 14-8751. CTSET2_CFG_CTIRQSTAT Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TIM_INTN_IE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TIM_INTN_IE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIM_INTN_IE							
R/W							
0h							

Table 14-26539. CTSET2_CFG_CTIRQSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IE	R/W	0h	IRQSTATUS value. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.11.1.2.211 CTSET2_CFG_CTIRQENABLE_SET Register

1 CTSET2_CFG_CTIRQENABLE_SET Register (Offset = C0Ch) [reset = 0h]

Counter Timer IRQENABLE_SET Register. This register is to enable generation of Interrupt Event used by SW. This register exists only if NUMTIMR > 0

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Table 14-26540. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C0Ch**

Figure 14-8752. CTSET2_CFG_CTIRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IES							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IES							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IES							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IES							
R/W							
0h							

Table 14-26542. CTSET2_CFG_CTIRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IES	R/W	0h	IRQSET value. This bit sets the enable of the interrupt event. SW can also read this bit to determine if the interrupt is enabled. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.11.1.2.212 CTSET2_CFG_CTIRQENABLE_CLR Register

1 CTSET2_CFG_CTIRQENABLE_CLR Register (Offset = C10h) [reset = 0h]

Counter Timer IRQENABLE_CLR Register. This register is to disable generation of Interrupt Event used by SW. This register exists only if NUMTIMR > 0

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Table 14-26543. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 2C10h**

Figure 14-8753. CTSET2_CFG_CTIRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IEC							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IEC							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IEC							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IEC							
R/W							
0h							

Table 14-26545. CTSET2_CFG_CTIRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IEC	R/W	0h	IRQCLR value. This bit clears the enable of the interrupt event. SW can also read this bit to determine if the interrupt is enabled. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.11.1.2.213 CTSET2_CFG_STPTCR Register

1 CTSET2_CFG_STPTCR Register (Offset = 1800h) [reset = 4h]

STP Trace Control Register

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Table 14-26546. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3800h**

Figure 14-8754. CTSET2_CFG_STPTCR Name Register

31	30	29	28	27	26	25	24
RESERVED3							MOD_FIFOFULL
R							R
0h							0h

23	22	21	20	19	18	17	16
DATA_FIFOFULL	RESERVED2						
R	R						
0h	0h						

15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED2		COMPEN	RESERVED1		SYNCEN	TSEN	RESERVED
R		R/W	R		R	R/W	R
0h		0h	0h		1h	0h	0h

Table 14-26548. CTSET2_CFG_STPTCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED3	R	0h	Reserved, returns 0
24	MOD_FIFOFULL	R	0h	STPMI2ATB internal MID packet fifo is full
23	DATA_FIFOFULL	R	0h	STPMI2ATB internal Data packet fifo is full
22:6	RESERVED2	R	0h	Reserved, returns 0
5	COMPEN	R/W	0h	Compression of Data enable
4:3	RESERVED1	R	0h	Reserved, returns 0
2	SYNCEN	R	1h	The value 1 indicates STPASYNC is supported
1	TSEN	R/W	0h	Timestamp Enable. This bit is static and should not be changed dynamically. This should be changed before client is enabled.
0	RESERVED	R	0h	Reserved, returns 0

14.11.1.2.214 CTSET2_CFG_STPTID Register

1 CTSET2_CFG_STPTID Register (Offset = 1804h) [reset = 0h]

STP Trace ID Register

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Table 14-26549. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3804h**

Figure 14-8755. CTSET2_CFG_STPTID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	TRACEID						
R	R/W						
0h	0h						

Table 14-26551. CTSET2_CFG_STPTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6:0	TRACEID	R/W	0h	Trace ID value. Software may overwrite the value at any time, but this is only recommended for scenarios where top-level configuration errors result in a collision between HW initiator IDs

14.11.1.2.215 CTSET2_CFG_STPASYNC Register

1 CTSET2_CFG_STPASYNC Register (Offset = 1810h) [reset = 130Ch]

STP Synchronization Control Register

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Table 14-26552. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3810h**

Figure 14-8756. CTSET2_CFG_STPASYNC Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED			EXPMODE	COUNT			
R			R/W	R/W			
0h			1h	30Ch			
7	6	5	4	3	2	1	0
COUNT							
R/W							
30Ch							

Table 14-26554. CTSET2_CFG_STPASYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	R	0h	Reserved, returns 0
12	EXPMODE	R/W	1h	Exponent mode, A value of 1 sets count to 2 to the Nth, where Nth is ((bits 11 : 8)+12). A value of 0 sets Count to N (bits 11 : 0)
11:0	COUNT	R/W	30Ch	The number of bytes between Synchronization packets

14.11.1.2.216 CTSET2_CFG_STPFFCR Register

1 CTSET2_CFG_STPFFCR Register (Offset = 1814h) [reset = 0h]

STP Flush Control Register

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Table 14-26555. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3814h**

Figure 14-8757. CTSET2_CFG_STPFFCR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1		FORCEFLUSH	RESERVED			ASYNCPE	AUTOFLUSH
R		R/W	R			R/W	R/W
0h		0h	0h			0h	0h

Table 14-26557. CTSET2_CFG_STPFFCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED1	R	0h	Reserved, returns 0
5	FORCEFLUSH	R/W	0h	Write a 1 to force a flush, automatically clears after the operation is complete
4:2	RESERVED	R	0h	Reserved, returns 0
1	ASYNCPE	R/W	0h	Async Priority Enable. 0 indicates ASYNC packet priority is lower than trace. 1 indicates priority escalates on second synchronization request
0	AUTOFLUSH	R/W	0h	Auto flush enable. When set, on every complete data (ATDATA : WIDTH) in the fifo written, data is exported out when ATREADY is asserted. This should be written before client IP enabled

14.11.1.2.217 CTSET2_CFG_STPFEAT1 Register

1 CTSET2_CFG_STPFEAT1 Register (Offset = 1818h) [reset = 21h]

STP Features 1 Register

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Table 14-26558. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 3818h**

Figure 14-8758. CTSET2_CFG_STPFEAT1 Name Register

31	30	29	28	27	26	25	24
STP_RTLVER					STP_MAJVER		
R					R		
0h					0h		

23	22	21	20	19	18	17	16
STP_CUSTVER		STP_MINVER					RESERVED
R		R					R
0h		0h					0h

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED	VERSION			PROT			
NONE	R			R			
0h	2h			1h			

Table 14-26560. CTSET2_CFG_STPFEAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	STP_RTLVER	R	0h	RTL Version. Reset each time major or minor version is updated
26:24	STP_MAJVER	R	0h	Functional Major Version. This is the first version of STPMI2ATB
23:22	STP_CUSTVER	R	0h	Custom Version (not used)
21:17	STP_MINVER	R	0h	Functional Minor Version
16:8	RESERVED	R	0h	Reserved, returns 0
7	RESERVED	NONE	0h	Reserved
6:4	VERSION	R	2h	STP2.0 Time Stamp, Value of 011 indicates Natural binary timestamp, a value of 100 indicates gray binary timestamps
3:0	PROT	R	1h	Protocol Revision. Value of 0001 indicates STP 2.0

14.11.1.2.218 CXATBREPLICATOR_CFG_IDFILTER0 Register

1 CXATBREPLICATOR_CFG_IDFILTER0 Register (Offset = 0h) [reset = 0h]

Allows the setting of ID filter for Initiator 0.

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Table 14-26561. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4000h**

Figure 14-8759. CXATBREPLICATOR_CFG_IDFILTER0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID0_70_7F	ID0_60_6F	ID0_50_5F	ID0_40_4F	ID0_30_3F	ID0_20_2F	ID0_10_1F	ID0_0_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26563. CXATBREPLICATOR_CFG_IDFILTER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	ID0_70_7F	R/W	0h	Enable or disable ID filtering for id's 0x70 to 0x7F
6	ID0_60_6F	R/W	0h	Enable or disable ID filtering for id's 0x60 to 0x6F
5	ID0_50_5F	R/W	0h	Enable or disable ID filtering for id's 0x50 to 0x5F
4	ID0_40_4F	R/W	0h	Enable or disable ID filtering for id's 0x40 to 0x4F
3	ID0_30_3F	R/W	0h	Enable or disable ID filtering for id's 0x30 to 0x3F
2	ID0_20_2F	R/W	0h	Enable or disable ID filtering for id's 0x20 to 0x2F
1	ID0_10_1F	R/W	0h	Enable or disable ID filtering for id's 0x10 to 0x1F
0	ID0_0_F	R/W	0h	Enable or disable ID filtering for id's 0x0 to 0xF

14.11.1.2.219 CXATBREPLICATOR_CFG_IDFILTER1 Register

1 CXATBREPLICATOR_CFG_IDFILTER1 Register (Offset = 4h) [reset = 0h]

Allows the setting of ID filter for Initiator 1.

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Table 14-26564. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4004h**

Figure 14-8760. CXATBREPLICATOR_CFG_IDFILTER1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ID1_70_7F	ID1_60_6F	ID1_50_5F	ID1_40_4F	ID1_30_3F	ID1_20_2F	ID1_10_1F	ID1_0_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-26566. CXATBREPLICATOR_CFG_IDFILTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	ID1_70_7F	R/W	0h	Enable or disable ID filtering for id's 0x70 to 0x7F
6	ID1_60_6F	R/W	0h	Enable or disable ID filtering for id's 0x60 to 0x6F
5	ID1_50_5F	R/W	0h	Enable or disable ID filtering for id's 0x50 to 0x5F
4	ID1_40_4F	R/W	0h	Enable or disable ID filtering for id's 0x40 to 0x4F
3	ID1_30_3F	R/W	0h	Enable or disable ID filtering for id's 0x30 to 0x3F
2	ID1_20_2F	R/W	0h	Enable or disable ID filtering for id's 0x20 to 0x2F
1	ID1_10_1F	R/W	0h	Enable or disable ID filtering for id's 0x10 to 0x1F
0	ID1_0_F	R/W	0h	Enable or disable ID filtering for id's 0x0 to 0xF

14.11.1.2.220 CXATBREPLICATOR_CFG_ITATBCTR1 Register

1 CXATBREPLICATOR_CFG_ITATBCTR1 Register (Offset = EF8h) [reset = 0h]

Returns the value of the ATREADYM0, ATREADYM1 and ATVALIDS inputs in integration mode.

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Table 14-26567. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4EF8h**

Figure 14-8761. CXATBREPLICATOR_CFG_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ATVALIDS_R	RESERVED	ATREADYM1_R	ATREADYM0_R
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-26569. CXATBREPLICATOR_CFG_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ATVALIDS_R	R	0h	Reads the value of the ATVALIDS input :
2	RESERVED	NONE	0h	Reserved
1	ATREADYM1_R	R	0h	Reads the value of the ATREADYM1 input :
0	ATREADYM0_R	R	0h	Reads the value of the ATREADYM0 input :

14.11.1.2.221 CXATBREPLICATOR_CFG_ITATBCTR0 Register

1 CXATBREPLICATOR_CFG_ITATBCTR0 Register (Offset = EFCh) [reset = 0h]

Controls the value of the ATVALIDM0, ATVALIDM1 and ATREADYS outputs in integration mode.

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Table 14-26570. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4EFCh**

Figure 14-8762. CXATBREPLICATOR_CFG_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ATREADYS_W	RESERVED	ATVALIDM1_W	RESERVED	ATVALIDM0_W
NONE			R/W	NONE	R/W	NONE	R/W
0h			0h	0h	0h	0h	0h

Table 14-26572. CXATBREPLICATOR_CFG_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	ATREADYS_W	R/W	0h	Sets the value of the ATREADYS output :
3	RESERVED	NONE	0h	Reserved
2	ATVALIDM1_W	R/W	0h	Sets the value of the ATVALIDM1 output :
1	RESERVED	NONE	0h	Reserved
0	ATVALIDM0_W	R/W	0h	Sets the value of the ATVALIDM0 output :

14.11.1.2.222 CXATBREPLICATOR_CFG_ITCTRL Register

1 CXATBREPLICATOR_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

Used to enable topology detection. See the CoreSight Architecture Specification for more information. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for integration testing and topology solving. p/ > Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-26573. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4F00h**

Figure 14-8763. CXATBREPLICATOR_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-26575. CXATBREPLICATOR_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Enables the component to switch from functional mode to integration mode and back. If no integration functionality is implemented, this register must read as zero.

14.11.1.2.223 CXATBREPLICATOR_CFG_CLAIMSET Register

1 CXATBREPLICATOR_CFG_CLAIMSET Register (Offset = FA0h) [reset = Fh]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-26576. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FA0h**

Figure 14-8764. CXATBREPLICATOR_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				Fh			

Table 14-26578. CXATBREPLICATOR_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	Fh	This claim tag bit is implemented

14.11.1.2.224 CXATBREPLICATOR_CFG_CLAIMCLR Register

1 CXATBREPLICATOR_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-26579. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FA4h**

Figure 14-8765. CXATBREPLICATOR_CFG_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMCLR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26581. CXATBREPLICATOR_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.225 CXATBREPLICATOR_CFG_LAR Register

1 CXATBREPLICATOR_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers.

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Table 14-26582. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FB0h**

Figure 14-8766. CXATBREPLICATOR_CFG_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-26584. CXATBREPLICATOR_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. An invalid write has the affect of removing write access.

14.11.1.2.226 CXATBREPLICATOR_CFG_LSR Register

1 CXATBREPLICATOR_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register, 0xFB0.

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Table 14-26585. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FB4h**

Figure 14-8767. CXATBREPLICATOR_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-26587. CXATBREPLICATOR_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register, 0xFB0, is implemented as 8-bit or 32-bit.
1	LOCKGRANT	R	1h	Returns the current status of the Lock.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device.

14.11.1.2.227 CXATBREPLICATOR_CFG_AUTHSTATUS Register

1 CXATBREPLICATOR_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = 0h]

Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register

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Table 14-26588. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FB8h**

Figure 14-8768. CXATBREPLICATOR_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		0h		0h	

Table 14-26590. CXATBREPLICATOR_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	0h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	0h	Indicates the security level for non-secure invasive debug

14.11.1.2.228 CXATBREPLICATOR_CFG_DEVID Register

1 CXATBREPLICATOR_CFG_DEVID Register (Offset = FC8h) [reset = 2h]

Indicates the capabilities of the CoreSight Replicator.

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Table 14-26591. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FC8h**

Figure 14-8769. CXATBREPLICATOR_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PORTNUM			
NONE				R			
0h				2h			

Table 14-26593. CXATBREPLICATOR_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	PORTNUM	R	2h	This value indicates the number of initiator ports implemented.

14.11.1.2.229 CXATBREPLICATOR_CFG_DEVTYPE Register

1 CXATBREPLICATOR_CFG_DEVTYPE Register (Offset = FCCh) [reset = 22h]

Provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-26594. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FCCh**

Figure 14-8770. CXATBREPLICATOR_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
2h				2h			

Table 14-26596. CXATBREPLICATOR_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	2h	Sub-classification within the major category :
3:0	MAJOR_TYPE	R	2h	Major classification grouping for this debug or trace component :

14.11.1.2.230 CXATBREPLICATOR_CFG_PIDR4 Register

1 CXATBREPLICATOR_CFG_PIDR4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-26597. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 4FD0h

Figure 14-8771. CXATBREPLICATOR_CFG_PIDR4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FOURKB_COUNT				JEP106_CONT			
R				R			
0h				4h			

Table 14-26599. CXATBREPLICATOR_CFG_PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	FOURKB_COUNT	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB, this must read as 0x0, 4KB only. For 8KB set to 0x1, for 16KB set to 0x2, for 32KB set to 0x3, and so on.
3:0	JEP106_CONT	R	4h	JEDEC continuation code indicating the designer of the component, together with the identity code.

14.11.1.2.231 CXATBREPLICATOR_CFG_PIDR0 Register

1 CXATBREPLICATOR_CFG_PIDR0 Register (Offset = FE0h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-26600. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 4FE0h

Figure 14-8772. CXATBREPLICATOR_CFG_PIDR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_NUMBER_BITS7TO0							
R							
9h							

Table 14-26602. CXATBREPLICATOR_CFG_PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_NUMBER_BITS7TO0	R	9h	Bits [7 : 0] of the component part number. This is selected by the designer of the component.

14.11.1.2.232 CXATBREPLICATOR_CFG_PIDR1 Register

1 CXATBREPLICATOR_CFG_PIDR1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-26603. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FE4h**

Figure 14-8773. CXATBREPLICATOR_CFG_PIDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
JEP106_BITS3TO0				PART_NUMBER_BITS11TO8			
R				R			
0h				9h			

Table 14-26605. CXATBREPLICATOR_CFG_PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	JEP106_BITS3TO0	R	0h	Bits [3 : 0] of the JEDEC identity code indicating the designer of the component, together with the continuation code.
3:0	PART_NUMBER_BITS11TO8	R	9h	Bits [11 : 8] of the component part number. This is selected by the designer of the component.

14.11.1.2.233 CXATBREPLICATOR_CFG_PIDR2 Register

1 CXATBREPLICATOR_CFG_PIDR2 Register (Offset = FE8h) [reset = 18h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-26606. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FE8h**

Figure 14-8774. CXATBREPLICATOR_CFG_PIDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	JEP106_BITS6TO4		
R				R	R		
1h				1h	0h		

Table 14-26608. CXATBREPLICATOR_CFG_PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	1h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is used as a look-up to establish the exact major and minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used.
2:0	JEP106_BITS6TO4	R	0h	Bits [6 : 4] of the JEDEC identity code indicating the designer of the component, together with the continuation code.

14.11.1.2.234 CXATBREPLICATOR_CFG_PIDR3 Register

1 CXATBREPLICATOR_CFG_PIDR3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

Return to Summary Table

Table 14-26609. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FECh**

Figure 14-8775. CXATBREPLICATOR_CFG_PIDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CUSTOMER_MODIFIED			
R				R			
0h				0h			

Table 14-26611. CXATBREPLICATOR_CFG_PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CUSTOMER_MODIFIED	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.235 CXATBREPLICATOR_CFG_CIDR0 Register

1 CXATBREPLICATOR_CFG_CIDR0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-26612. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FF0h**

Figure 14-8776. CXATBREPLICATOR_CFG_CIDR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PREAMBLE							
R							
Dh							

Table 14-26614. CXATBREPLICATOR_CFG_CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE	R	Dh	Contains bits [24 : 31] of the component identification.

14.11.1.2.236 CXATBREPLICATOR_CFG_CIDR1 Register

1 CXATBREPLICATOR_CFG_CIDR1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-26615. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FF4h**

Figure 14-8777. CXATBREPLICATOR_CFG_CIDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PREAMBLE			
R				R			
9h				0h			

Table 14-26617. CXATBREPLICATOR_CFG_CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component, for example, ROM table or CoreSight component.
3:0	PREAMBLE	R	0h	Contains bits [19 : 16] of the component identification.

14.11.1.2.237 CXATBREPLICATOR_CFG_CIDR2 Register

1 CXATBREPLICATOR_CFG_CIDR2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-26618. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 4FF8h**

Figure 14-8778. CXATBREPLICATOR_CFG_CIDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PREAMBLE							
R							
5h							

Table 14-26620. CXATBREPLICATOR_CFG_CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE	R	5h	Contains bits [15 : 8] of the component identification.

14.11.1.2.238 CXATBREPLICATOR_CFG_CIDR3 Register

1 CXATBREPLICATOR_CFG_CIDR3 Register (Offset = FFCh) [reset = B1h]

A component identification register, that indicates that the identification registers are present.

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Table 14-26621. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 4FFCh

Figure 14-8779. CXATBREPLICATOR_CFG_CIDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PREAMBLE							
R							
B1h							

Table 14-26623. CXATBREPLICATOR_CFG_CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE	R	B1h	Contains bits [7 : 0] of the component identification.

14.11.1.2.239 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_RAMSZ Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_RAMSZ Register (Offset = 4h) [reset = 0h]

CT-TBR RAM Size Register This register indicates the size of the local memory buffer interfaced with the CT-TBR This register can be used to determine if the CT_TBR is synthesized for System Bridge Mode only. It will read 0x00000000 in this configuration.

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Table 14-26624. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 5004h**

Figure 14-8780. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_RAMSZ Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">RAM_SIZE</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-26626. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_RAMSZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	
2:0	RAM_SIZE	R	0h	Indicates the size of the local memory1 Read 0x0 : No local buffer. TBR Bridge only configuration Read 0x1 : 4K bytes Read 0x2 : 8K bytes Read 0x3 : 16K bytes Read 0x4 : 32K bytes Read 0x5 : 64K bytes Read 0x6 : 128K bytes Read 0x7 : Reserved

14.11.1.2.240 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_FIFOSZ Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_FIFOSZ Register (Offset = 8h) [reset = 0h]

CT-TBR Output FIFO Size Register This register indicates the size of output FIFO used to transfer data to the system target interface

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Table 14-26627. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5008h**

Figure 14-8781. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_FIFOSZ Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					FIFO_SIZE		
R					R		
0h					0h		

Table 14-26629. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_FIFOSZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	
2:0	FIFO_SIZE	R	0h	Indicates the size of the output FIFO Read 0x0 : 128 bytes Read 0x1 : 256 bytes Read 0x2 : 512 bytes Read 0x3 : 1024 bytes Read 0x4 : 2048 bytes Read 0x5-0x7 : Reserved

14.11.1.2.241 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_STAT Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_STAT Register (Offset = Ch) [reset = 28h]

TBR Status Register This register indicates status of various functions performed by CT-TBR

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Table 14-26630. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 500Ch**

Figure 14-8782. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	RESET_OUT	PARTIAL_OUT	DRAIN_DONE	FMT_DONE	CPT_DONE	TRIG	WRAP
R	R	R	R	R	R	R	R
0h	0h	1h	0h	1h	0h	0h	0h

Table 14-26632. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	
6	RESET_OUT	R	0h	Reset Active bit indicates that at least one of the domains in the CT-TBR is currently being held in reset. Read 0b : All domains and/or interfaces of the CT-TBR are out of reset Read 1b : At least one of the domains and/or interfaces of the CT-TBR are being held in reset
5	PARTIAL_OUT	R	1h	Indicates that a partial output block (0 < Level < Trigger Threshold) is in the TBR memory (output buffer and possibly local RAM) and that an OUTFLUSH sequence may be required since there is no valid data to available to increase the amount of data past the OUTLVL threshold (i.e. local RAM buffer is empty). This bit is not set if the partial output block is the result of currently active block read request (i.e. it is already actively draining). This bit is only valid in System Bridge Mode. Read 0b : A partial frame does not exist or there is pending data in the local data RAMs that might complete any partial output blocks. Read 1b : A partial output block is in the buffer and there is not valid data available to push this through the system without an OUTFLUSH. Enabling acquisition (CTRL : ENBL 0- > 1) resets the output FIFO pointers and RAM pointers, so this bit will be set to 0 each time acquisition is enabled.

Table 14-26632. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DRAIN_DONE	R	0h	Indicates the whether there is data in the output FIFO. This bit is only valid in System Bridge Mode. Read 0b : There is still valid data in the CT-TBR output FIFO Read 1b : All valid data in the CT-TBR output FIFO has been transferred via the system interface. Enabling acquisition (CTRL : ENBL 0- > 1) resets the output FIFO pointers, so this bit will be set to 0 each time acquisition is enabled.
3	FMT_DONE	R	1h	Indicates that all pending local memory transactions from the formatter are complete and no more data will be posted from the formatter. Read 0b : Data may still be pending Read 1b : Final data from the formatter has been posted. This bit is reset to 0b when the CTRL : ENBL transitions from 0b to 1b.
2	CPT_DONE	R	0h	Indicates that ATB interface is disabled and trace data capture is complete. Read 0b : Trace capture still active Read 1b : Trace capture complete This bit is reset to 0b when the CTRL : ENBL transitions from 0b to 1b.
1	TRIG	R	0h	Indicates that the local memory buffer has been locked as the result of a trigger. This bit is only valid in Buffer Mode and will always read 0 in System Bridge mode Read 0b : No trigger seen. Read 1b : Trigger input detected and buffer locked This bit is reset to 0b when the CTRL : ENBL transitions from 0b to 1b.
0	WRAP	R	0h	This bit is active in buffer mode only and is not present in CT-TBR configurations that only support System bridge mode Indicates that the local memory write pointer has incremented past the upper boundary of the memory reset to the lowest address (at least once). Read 0b : No wrap Read 1b : Write pointer has wrapped This bit is reset to 0b when the CTRL : ENBL transitions from 0b to 1b

14.11.1.2.242 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRDAT Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRDAT Register (Offset = 10h) [reset = 0h]

RAM Read Data Register This register is used to transfer data from the local memory to client This register is not present when CT-TBR is synthesized for System Bridge Mode only.

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Table 14-26633. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5010h**

Figure 14-8783. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRDAT Name Register

31	30	29	28	27	26	25	24
DATA							
R							
0h							
23	22	21	20	19	18	17	16
DATA							
R							
0h							
15	14	13	12	11	10	9	8
DATA							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-26635. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R	0h	The 32-bit data value pointed to by the RAMRPTR register Reading returns the value at the index specified by RAMRPTR. RAMRPTR is then incremented automatically.

14.11.1.2.243 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRPTR Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRPTR Register (Offset = 14h) [reset = 0h]

RAM Read Pointer Register Indexes into the local memory for reading 32-bit values via RAMRDAT This register is not present when CT-TBR is synthesized for System Bridge Mode only.

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Table 14-26636. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5014h**

Figure 14-8784. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRPTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED		PTR					
R/W		R/W					
0h		0h					
15	14	13	12	11	10	9	8
PTR							
R/W							
0h							
7	6	5	4	3	2	1	0
PTR							
R/W							
0h							

Table 14-26638. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMRPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	R/W	0h	
21:0	PTR	R/W	0h	This field designates the index of the 32-bit RAM location to be read via RAMRDAT. Read returns the current value of the pointer Write sets the value and initiates a read from the designated address. This field increments automatically when a value is read from RAMRDAT. This register should not be used when the data acquisition is enabled (results are undefined). The actual width of the pointer field will be determined by the buffer size1

14.11.1.2.244 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWPTR Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWPTR Register (Offset = 18h) [reset = 0h]

This field designates the index of the 32-bit RAM location to be written via RAMWDAT. Read : Returns the current value of the pointer Write : Sets the value Writes will always force the bits 1 : 0 of write_value to 0. This register should not be used when the data acquisition is enabled (results are undefined). The actual width of the pointer field will be determined by the buffer size1

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Table 14-26639. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5018h**

Figure 14-8785. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWPTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PTR					
R/W		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PTR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PTR							
R/W							
0h							

Table 14-26641. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	R/W	0h	
21:0	PTR	R/W	0h	This field designates the index of the 32-bit RAM location to be read via RAMRDAT. Read returns the current value of the pointer Write sets the value and initiates a read from the designated address. This field increments automatically when a value is read from RAMRDAT. This register should not be used when the data acquisition is enabled (results are undefined). The actual width of the pointer field will be determined by the buffer size1

14.11.1.2.245 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TRGCNT Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TRGCNT Register (Offset = 1Ch) [reset = 0h]

Trigger Count Register This register controls the amount of data written to the local memory after a trigger input is detected

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Table 14-26642. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 501Ch**

Figure 14-8786. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TRGCNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">COUNT</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26644. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TRGCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	R/W	0h	
12:0	COUNT	R/W	0h	Controls the number of 128-bit words written to local memory after a trigger input is detected on the CTI interface. When the input trigger is active and a trigger is detected, an internal register starts counting the number of 128-bit words written to local memory. When that counter equals COUNT + 1, the memory is locked and the CAPT_DONE and the TRIG bits in the STAT register are set. - Setting COUNT to a low index will lock trace that occurred before the trigger - Setting COUNT to a high index will lock trace that occurred after the trigger - Setting COUNT to an intermediate index will lock trace that occurred around the trigger Read : Returns the current configured value of the trigger counter Write : Sets a new value. This register can be read at any time but can only be written when acquisition is disabled in CNTL. The internal count register is not visible to the application, but it is reset cleared by hardware when the CTRL'ENBL bit transitions from 0 to 1. The width of the COUNT field is actually log2(RAM size in Bytes / 16) When configured for System Bridge only, the COUNT field is fixed a 10-bits (9 : 0). This allows the CT-TBR to capture and forward up to 1024 frames of data after the trigger event.

14.11.1.2.246 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TBR_CTRL Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TBR_CTRL Register (Offset = 20h) [reset = 0h]

CT-TBR Control Register This register controls the global enable/disable functions of the CT-TBR

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Table 14-26645. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 5020h

Figure 14-8787. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TBR_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED			IDLE_EMPTY	SYNCREQ_WRAP	SRST	MODE	ENBL
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-26647. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TBR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R/W	0h	
4	IDLE_EMPTY	R/W	0h	Controls whether the CT_TBR can enter idle with data present Read 0x0 : All internal buffers must be empty before idle requests are acknowledged Read 0x1 : CT_TBR can idle with valid data Write 0x0 : Clear idle with valid data Write 0x1 : Set idle with valid data
3	SYNCREQ_WRAP	R/W	0h	Controls whether the CT-TBR will issue a pulse on SYNREQ each time the local buffer write pointer wraps back to address 0. Read 0x0 : SYNCREQ generation is suppressed Read 0x1 : SYNCREQ on buffer wrap is enabled Write 0x0 : Disable SYNCREQ generation Write 0x1 : Enable SYNCREQ generation
2	SRST	R/W	0h	Software initiated reset control Read 0x0 : Always Write 0x0 : No action Write 0x1 : Initiates a software reset
1	MODE	R/W	0h	This field is the top-level control for determining the operating mode of the module Read 0x0 : Module is in Buffer Mode Read 0x1 : Module is in System Bridge Mode Write 0x0 : Set Buffer Mode Write 0x1 : Set System Bridge Mode This bit can only be written when the ENBL bit is '0' Setting it when acquisition in enabled may result in undefined behavior. This bit is read only and set to '1' when CT-TBR is synthesized for System Bridge only operation.

Table 14-26647. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_TBR_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ENBL	R/W	0h	This field is the top-level control for enabling trace acquisition and processing in the module. Read 0x0 : Module is disabled Read 0x1 : Module is enabled (trace data is being captured and stored to local memory) Write 0x0 : Disable module Write 0x1 : Enable module

14.11.1.2.247 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWDAT Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWDAT Register (Offset = 24h) [reset = 0h]

RAM Write Data Register This register is used to transfer data from the client to local memory This register is not present when CT-TBR is synthesized for System Bridge Mode only.

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Table 14-26648. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5024h**

Figure 14-8788. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWDAT Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-26650. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_RAMWDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	The 32-bit data value to be written to local memory Writing initiates the transfer of data to the location pointed at by RAMWPTR. RAMWPTR is then incremented automatically. This register should not be used when the data acquisition is enabled (results are undefined).

14.11.1.2.248 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OUTLVL Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OUTLVL Register (Offset = 100h) [reset = 63h]

Output FIFO Trigger Level Register This register controls the size of the data blocks transferred through the output FIFO and across the system interface

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Table 14-26651. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 5100h

Figure 14-8789. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OUTLVL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
NUMBLOCK							
R/W							
0h							
7	6	5	4	3	2	1	0
BLOCKSZ							
R/W							
63h							

Table 14-26653. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OUTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	
15:8	NUMBLOCK	R/W	0h	Determines blocks (value + 1) that must be sent over the system interface to complete a higher level data frame for transport. This field is used to calculate the total output trigger threshold when used in conjunction with BLOCKSZ field. Output Trigger Threshold (in frames) = (BLOCKSZ + 1) * (NUMBLOCK + 1) The threshold calculations include data in the output FIFO and local RAM buffers (if local RAM exists). Read : Returns the current configured value of the number of blocks in the high level data frame Write : Sets a new value. This register is only valid when the CT-TBR is operating in System Bridge mode This register can be read at any time but can only be written when acquisition is disabled in CNTL. In addition, SW should only update NUMBLOCK when the following conditions are all true : " An output flush sequence is not active (OPCTL : OUTFLUSH == 0) " The system interface output buffer is empty (STAT : DRAIN_DONE == 1)

Table 14-26653. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OUTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	BLOCKSZ	R/W	63h	Determines the block size (the number of 128-bit frames + 1) used by the DMA engine Reading data over the system interface. This field is used to calculate the total output trigger threshold when used in conjunction with NUMBLOCK field. The block size is used by the DMA event logic to determine when to deassert the DMA request. Output Trigger Threshold (in frames) = (BLOCKSZ + 1) * (NUMBLOCK + 1) The threshold calculations include data in the output FIFO and local RAM buffers (if local RAM exists). Read : Returns the current configured value of the block size Write : Sets a new value. The minimum value for BLOCKSZ is 0xF. If configured for less than 0xF, the behavior of the system interface is undefined. This register is only valid when the CT-TBR is operating in System Bridge mode This register can be read at any time but can only be written when acquisition is disabled in CNTL. In addition, SW should only update BLOCKSZ when the following conditions are all true : " An output flush sequence is not active (OPCTL : OUTFLUSH == 0) " The system interface output buffer is empty (STAT : DRAIN_DONE == 1)

14.11.1.2.249 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_SICTRL Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_SICTRL Register (Offset = 104h) [reset = 32h]

CT-TBR System Interface Control This register provides control and status for the system interface of the CT-TBR

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Table 14-26654. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5104h**

Figure 14-8790. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_SICTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED1</td><td colspan="2">IDLE_MODE</td><td>RESERVED</td><td>ERR</td><td>REQ_PEND</td><td>DATA_WIDTH</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R</td><td>R/W</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">3h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-26656. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_SICTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED1	R/W	0h	
5:4	IDLE_MODE	R/W	3h	This bit-field controls the idle behavior of the CT-TRB Read : Indicates the Idle modes outlined below Write 00b : Set Force-Idle. For CT-TBR, Force-Idle is identical to Smart-Idle Write 01b : Set No-Idle : The CT_TBR will acknowledge the idle request, but never transition to the idle state Write 10b : Set Smart-Idle : The CT-TBR uses the smart idle protocol. This is the default mode. Write 11b : Set Smart-Idle-Wkup : Since the CT-TBR does not support internal wakeup, this mode is identical to Smart-Idle
3	RESERVED	R	0h	
2	ERR	R/W	0h	This bit indicates that an access on the System Target I/F resulted in a error Read 0x0 : No errors since last clear Read 0x1 : At least one error condition on the I/F since last clear Write 0x0 : No effect Write 0x1 : Clears bit to 0 This bit clears to 0 when data acquisition is enabled (CTRL : ENBL 0- > 1)
1	REQ_PEND	R	1h	This bit indicates if a read request is pending or active on the system interface Read 0x0 : No read requests pending or active Read 0x1 : A system initiator has posted a read request on the system interface and this request is pending or being serviced

Table 14-26656. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_SICTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DATA_WIDTH	R/W	0h	This bit controls the supported access size for the system interface Read 0x0 : System interface will only support 32-bit reads Read 0x1 : System interface will only support 64-bit reads Write 0x0 : Set 32-bit mode Write 0x1 : Set 64-bit mode This bit is RO and set to 0 when synthesized for 32-bit data width

14.11.1.2.250 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IDPERIOD Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IDPERIOD Register (Offset = 108h) [reset = 0h]

ID Repeat Period Register This register controls the number of frames (without and ID change marker) that will be sent before the formatter forces and ID marker

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Table 14-26657. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5108h**

Figure 14-8791. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IDPERIOD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PERIOD</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERIOD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26659. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IDPERIOD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	R/W	0h	
9:0	PERIOD	R/W	0h	Controls the number of 128-bit frames (with no ID change markers) that the formatter will forward before forcing an artificial ID change. Read : Returns the current configured value of the period Write : Sets the value Setting to 0 disables the forcing of IDs, but this is not recommended. PERIOD should only be updated when trace acquisition is disabled

14.11.1.2.251 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_SEQCNTL Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_SEQCNTL Register (Offset = 10Ch) [reset = 7274496h]

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Table 14-26660. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 510Ch**

Figure 14-8792. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_SEQCNTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">Eh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED2</td><td colspan="7">SEQID</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>Eh</td><td colspan="7">27h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PERIOD</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">11h</td><td colspan="2">96h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERIOD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">96h</td></tr>
</table>

Table 14-26662. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CT_TBR_SEQCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED2	R/W	Eh	
22:16	SEQID	R/W	27h	PERIOD1This defined the ATID used when inserting the incrementing sequence byte. The reset value is the highest free ID supported in the TWP specification, but this can be overwritten by SW if there are system collisions
15:10	RESERVED	R/W	11h	
9:0	PERIOD	R/W	96h	Controls the number of 128-bit frames that the formatter will forward before inserting an 8-bit incrementing sequence number into a frame using ATID defined in SEQID Read : Returns the current configured value of the period Write : Sets the value Setting to 0 disables the insertion of the incrementing sequence bytes, PERIOD should only be updated when trace acquisition is disabled

14.11.1.2.252 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_EOI Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_EOI Register (Offset = 120h) [reset = 0h]

CT-TBR EOI register This register is the End of Interrupt used by SW to signal HW that an interrupt service is complete and an interrupt can be rearmed.

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Table 14-26663. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5120h**

Figure 14-8793. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECT
R/W							R/W
0h							0h

Table 14-26665. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R/W	0h	
0	EOI_VECT	R/W	0h	This bit is used by SW to signal that a particular interrupt generated by the IP can be rearmed. Read 0x0 : Always Write 0x0 : DAV_IRQ is rearmed (it is IRQ index 0 for this IP) Write 0x1 : AQCMP_IRQ is rearmed (it is IRQ index 1)

14.11.1.2.253 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS_RAW Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS_RAW Register (Offset = 124h) [reset = 0h]

CT-TBR IRQ Status (Raw) register This register provides control and status for the interrupt/event interface The IRQSTATUS_RAW register may be modified while acquisition is enabled

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Table 14-26666. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5124h**

Figure 14-8794. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						AQCMP_IRQ	DAV_IRQ
R/W						R/W	R/W
0h						0h	0h

Table 14-26668. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R/W	0h	
1	AQCMP_IRQ	R/W	0h	This bit controls the acquisition complete interrupt/event generation for testing Read 0x0 : Acquisition complete interrupt is not active Read 0x1 : Acquisition complete interrupt is active and awaiting completion. The enabled state is not considered. Write 0x0 : No effect Write 0x1 : Sets the interrupt request for testing
0	DAV_IRQ	R/W	0h	This bit controls the data available interrupt/event generation for testing Read 0x0 : Data available interrupt is not active Read 0x1 : Data available interrupt is active and awaiting completion. The enabled state is not considered. Write 0x0 : No effect Write 0x1 : Sets the interrupt request for testing

14.11.1.2.254 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS Register (Offset = 128h) [reset = 0h]

CT-TBR IRQ Status register This register provides control and status for the interrupt/event interface The IRQSTATUS register may be modified while acquisition is enabled

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Table 14-26669. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5128h**

Figure 14-8795. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						AQCMP_IE	DAV_IE
R/W						R/W	R/W
0h						0h	0h

Table 14-26671. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R/W	0h	
1	AQCMP_IE	R/W	0h	Acquisition complete interrupt enable Read 0x0 : Acquisition complete interrupt/event generation is either not pending or it is not enabled Read 0x1 : The acquisition complete interrupt is pending and enabled. Write 0x0 : No effect Write 0x1 : Clears a pending Acquisition complete interrupt
0	DAV_IE	R/W	0h	Data Available interrupt enable Read 0x0 : Data available interrupt/event generation is either not pending or it is disabled Read 0x1 : Data available interrupt is pending and enabled. Write 0x0 : No effect Write 0x1 : Clears a pending data available interrupt

14.11.1.2.255 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_SET Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_SET Register (Offset = 12Ch) [reset = 0h]

CT-TBR IRQ Enable set register This register provides control for the interrupt/event interface The IRQENABLE_SET register may be modified while acquisition is enabled

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Table 14-26672. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 512Ch**

Figure 14-8796. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED						AQCMP_IES	DAV_IES
R/W						R/W	R/W
0h						0h	0h

Table 14-26674. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R/W	0h	
1	AQCMP_IES	R/W	0h	Provides enable state and sets the enable of the acquisition complete interrupt/event Read 0x0 : The acquisition complete interrupt is disabled Read 0x1 : The acquisition complete interrupt is enabled Write 0x0 : No effect Write 0x1 : Enables the acquisition complete interrupt/event
0	DAV_IES	R/W	0h	Provides enable state and sets the enable of the data available interrupt/event Read 0x0 : The data available interrupt is disabled Read 0x1 : The data available interrupt is enabled Write 0x0 : No effect Write 0x1 : Enables the data available interrupt/event

14.11.1.2.256 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_CLR Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_CLR Register (Offset = 130h) [reset = 0h]

CT-TBR IRQ Enable clear register This register provides control for the interrupt/event interface The IRQENABLE_CLR register may be modified while acquisition is enabled

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Table 14-26675. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5130h**

Figure 14-8797. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>AQCMP_IEC</td><td>DAV_IEC</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-26677. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R/W	0h	
1	AQCMP_IEC	R/W	0h	Provides enable state and clears the enable of the data available interrupt/event Read 0x0 : The acquisition complete interrupt is disabled Read 0x1 : The acquisition complete interrupt is enabled Write 0x0 : No effect Write 0x1 : Disables the acquisition complete interrupt/event
0	DAV_IEC	R/W	0h	Provides enable state and clears the enable of the data available interrupt/event Read 0x0 : The data available interrupt is disabled Read 0x1 : The data available interrupt is enabled Write 0x0 : No effect Write 0x1 : Disables the data available interrupt/event

14.11.1.2.257 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPSTAT Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPSTAT Register (Offset = 300h) [reset = 2h]

Operation Status Register This register provides information on the status of various operations of the CT-TBR

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Table 14-26678. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5300h**

Figure 14-8798. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						FMT_HALTED	FLSH_ACT
R						R	R
0h						1h	0h

Table 14-26680. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	
1	FMT_HALTED	R	1h	This bit indicates that the formatter is halted and the last available data has been written to the local memory. It is functionally equivalent to the FMT_DONE bit in the STAT register. Read 0x0 : Formatter block is active Read 0x1 : Formatter block is disabled This bit is cleared by hardware when the CTRL'ENBL bit transitions from 0 to 1.
0	FLSH_ACT	R	0h	This bit indicates that a flush request is being processed by the CT-TBR Read 0x0 : No flush requests are active Read 0x1 : Flush request is pending completion

14.11.1.2.258 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPCTRL Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPCTRL Register (Offset = 304h) [reset = 512h]

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Table 14-26681. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5304h**

Figure 14-8799. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED4							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED4						SYNCREQ	OUTFLUSH
R						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
STP_FULL	RESERVED3	STP_TRG	STP_FLSH	RESERVED2	TRG_FLSH	TRG_EVT	TRG_TRGIN
R/W	R	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	1h
7	6	5	4	3	2	1	0
RESERVED1	FLUSH	FLSH_TRG	FLSH_FLSHIN	RESERVED		INSRT_TRG	FMT_ENBL
R	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	1h	0h		1h	0h

Table 14-26683. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED4	R	0h	
17	SYNCREQ	R/W	0h	This bit is allows the SW to stimulate a synchronization request to all the upstream trace components. Read 0x0 : This bit always reads as 0 Write 0x0 : Has no effect Write 0x1 : Results in the assertion of the SYNCREQ signal on the ATB target for one ATCLK cycle. SYNCREQ is available in any operating mode. SYNCREQ should only be written while trace acquisition is enabled.
16	OUTFLUSH	R/W	0h	This bit is the flush control. For the output FIFO (System Bridge Mode) it triggers a flush of this buffer and the flush completes when the last OUTLEVEL + 1 sized burst is read on the system Interface. Read 0x0 : No output flush operation is active Read 0x1 : Output flush operation is active Write 0x0 : No meaning Write 0x1 : Initiate an output buffer flush. Automatically clears to 0 when the operation completes OUTFLUSH may be written while trace acquisition is enabled
15	STP_FULL	R/W	0h	This bit controls whether the formatter stops operation when the local memory buffer is full. This 'one-shot' mode prevents the write pointer from wrapping, Read 0x0 : Formatter continues when write pointer wraps back to the lowest address Read 0x1 : Formatter stops operation when the local memory is full Write 0x0 : Disable formatter halt on full Write 0x1 : Enable formatter halt on full This bit is only functional when the CT-TBR is configured for Buffer Mode (CTRL : MODE == 0).
14	RESERVED3	R	0h	

Table 14-26683. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_OPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	STP_TRG	R/W	0h	This bit controls whether the formatter stops operation when a trigger is detected Read 0x0 : Formatter continues when trigger is detected Read 0x1 : Formatter stops operation when trigger is detected Write 0x0 : Disable formatter halt on trigger Write 0x1 : Enable formatter halt on trigger
12	STP_FLSH	R/W	0h	This bit controls whether the formatter stops operation when a flush completes Read 0x0 : Formatter continues after flush completion Read 0x1 : Formatter stops operation when flush completes Write 0x0 : Disable formatter halt on flush completion Write 0x1 : Enable formatter halt on flush completion
11	RESERVED2	R	0h	
10	TRG_FLSH	R/W	1h	This bit controls whether a trigger event is generated when a flush completes Read 0x0 : No trigger event generated when flush is completed. Read 0x1 : Trigger event generated Write 0x0 : Disable trigger event generation Write 0x1 : Enable trigger event generation
9	TRG_EVT	R/W	0h	This bit controls whether the action associated with a trigger is delayed until the trigger counter matches the value in TRGCNT : COUNT + 1. Read 0x0 : No trigger counter delay Read 0x1 : Trigger action delayed until trigger count match Write 0x0 : Disable trigger delay Write 0x1 : Enable trigger delay
8	TRG_TRGIN	R/W	1h	This bit controls whether a trigger event is generated when a rising edge is detected on the TRIGIN input on the CTI interface. Setting this bit also enables trigger event generation when a trigger ID (ATID = 0x7d) is seen on the ATB interface. Read 0x0 : No trigger event generated on TRIGIN assertion. Read 0x1 : Trigger event generated Write 0x0 : Disable trigger event generation Write 0x1 : Enable trigger event generation
7	RESERVED1	R	0h	
6	FLUSH	R/W	0h	This bit is the manual flush control. It triggers a flush from the trace data sources into the CT-TBR Read 0x0 : No manual flush operation is active Read 0x1 : Manual flush operation is active Write 0x0 : No meaning Write 0x1 : Initiate a manual flush. Automatically clears to 0 when the operation completes FLUSH may be written while trace acquisition is enabled
5	FLSH_TRG	R/W	0h	This bit controls whether a flush operation is initiated when a trigger condition is detected by the CT-TBR Read 0x0 : Flush on trigger event is disabled Read 0x1 : Flush on trigger event is enabled Write 0x0 : Disable flush on trigger event Write 0x1 : Enable flush on trigger event
4	FLSH_FLSHIN	R/W	1h	This bit controls whether a flush operation is initiated when a rising edge is detected on the FLUSHIN input signal Read 0x0 : Flush on FLUSHIN is disabled Read 0x1 : Flush on FLUSHIN is enabled Write 0x0 : Disable flush on FLUSHIN Write 0x1 : Enable flush on FLUSHIN
3:2	RESERVED	R	0h	
1	INSRT_TRG	R/W	1h	This bit controls whether the TWP trigger sequence is inserted into the TWP frame a trigger condition is encountered Read 0x0 : Trigger insertion is disabled Read 0x1 : Trigger insertion is enabled Write 0x0 : Disable trigger insertion Write 0x1 : Enable trigger insertion
0	FMT_ENBL	R/W	0h	This bit controls whether the ATB input data is formatted into 128-bit TWP frames Read 0x0 : Formatting is disabled Read 0x1 : Formatting is enabled Write 0x0 : Disable formatting Write 0x1 : Enable formatting

14.11.1.2.259 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMSET Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMSET Register (Offset = FA0h) [reset = 1h]

The Claim Tag Set Register The register is used to manage handshakes between application and tools SW using the CT-TBR

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Table 14-26684. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FA0h**

Figure 14-8800. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTSET			
R				R/W			
0h				1h			

Table 14-26686. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	
3:0	CTSET	R/W	1h	This bit sets the Claim Tag Read 0xF : Always. Indicates that claim tag has 4 valid bits Write 0x0 : No effect Write 0x1-F : Bit value of '1' sets the corresponding Claim Tag bit

14.11.1.2.260 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMCLR Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

The Claim Tag Clear Register The register is used to manage handshakes between application and tools SW using the CT-TBR

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Table 14-26687. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FA4h**

Figure 14-8801. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCLR			
R				R			
0h				0h			

Table 14-26689. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	
3:0	CTCLR	R	0h	This bit clears the Claim Tag Read : The current claim tag value Write 0x0 : No effect Write 0x1-F : Bit value of '1' clears the corresponding bit in the Claim Tag

14.11.1.2.261 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKACC Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKACC Register (Offset = FB0h) [reset = 0h]

The Lock Access Register The register is used to enabled application use of the CT-TBR

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Table 14-26690. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FB0h**

Figure 14-8802. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKACC Name Register

31	30	29	28	27	26	25	24
CODE							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CODE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CODE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CODE							
R							
0h							

Table 14-26692. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKACC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CODE	R	0h	This bit-field is used to unlock the CT-TBR for use by the application Write 0xC5ACCE55 : Unlocks the CT-TBR Write any other value : Lock the CT-TBR

14.11.1.2.262 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKSTAT Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKSTAT Register (Offset = FB4h) [reset = 2h]

The Lock Status Register The register is used to manage application use of the CT-TBR

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Table 14-26693. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 5FB4h**

Figure 14-8803. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKSZ	STAT	LOCKIMP
R					R	R	R
0h					0h	1h	0h

Table 14-26695. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_LOCKSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	
2	LOCKSZ	R	0h	This bit-field indicates the size of the lock access bit-field Read 0x0 : indicates the lock access field is 32-bits wide
1	STAT	R	1h	This bit-field indicates the current state of the lock Read 0x0 : indicates the module is not locked from application accesses Read 0x1 : Indicates the module is locked
0	LOCKIMP	R	0h	This bit-field indicates if the module implements a lock access mechanism Read 0x1 : Indicates a lock is present

14.11.1.2.263 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_AUTHSTAT Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_AUTHSTAT Register (Offset = FB8h) [reset = 0h]

Authorization Status Register Indicates which security features (if any) are implemented in the module.

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Table 14-26696. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FB8h**

Figure 14-8804. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_AUTHSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
S_NI_STAT		S_I_STAT		NS_NI_STAT		NS_I_STAT	
R		R		R		R	
0h		0h		0h		0h	

Table 14-26698. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_AUTHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:6	S_NI_STAT	R	0h	Secure, non-invasive debug status Read 0x0 : Indicates CT-TBR does not implement this feature
5:4	S_I_STAT	R	0h	
3:2	NS_NI_STAT	R	0h	
1:0	NS_I_STAT	R	0h	Non-secure, invasive debug status Read 0x0 : Indicates CT-TBR does not implement this feature

14.11.1.2.264 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVID Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVID Register (Offset = FC8h) [reset = 18h]

Device Identification Register Defines the major and minor versions of this implementation of the CT-TBR

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Table 14-26699. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FC8h**

Figure 14-8805. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REV_MAJOR</td><td colspan="4">REV_MIN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">8h</td></tr>
</table>

Table 14-26701. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	REV_MAJOR	R	1h	
3:0	REV_MIN	R	8h	Minor revision number Read 0x0 : The only minor revision currently supported

14.11.1.2.265 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVTYPE Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVTYPE Register (Offset = FCCh) [reset = 33h]

Device Type Register Indicates the top-level function of the module

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Table 14-26702. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FCCh**

Figure 14-8806. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB_TYPE				MAIN_CLASS			
R				R			
3h				3h			

Table 14-26704. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	SUB_TYPE	R	3h	Identifies the sub-type based upon class Read 0x2 : Indicates the CT-TBR is an embedded trace buffer
3:0	MAIN_CLASS	R	3h	Identifies the top level class to the module Read 0x1 : Indicates the CT-TBR is a trace sink

14.11.1.2.266 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID4 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Peripheral Identification Register Number 4 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-26705. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 5FD0h

Figure 14-8807. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
KB_COUNT				JEP_CONT			
R				R			
0h				0h			

Table 14-26707. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	KB_COUNT	R	0h	Indicates the number of 4KB block of configuration memory (+ 1) used by this module. Read 0x0 : CT-TBR uses one block
3:0	JEP_CONT	R	0h	JEDEC manufacture code continuation code Read 0x0 : TI JEP number does not use continuation

14.11.1.2.267 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID5 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID5 Register (Offset = FD4h) [reset = 0h]

Peripheral Identification Register Number 5 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-26708. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FD4h**

Figure 14-8808. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PID5							
R							
0h							

Table 14-26710. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	PID5	R	0h	Read 0x0 : As per CoreSight Architecture Specification

14.11.1.2.268 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID6 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID6 Register (Offset = FD8h) [reset = 0h]

Peripheral Identification Register Number 6 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-26711. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FD8h**

Figure 14-8809. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID6 Name Register

31	30	29	28	27	26	25	24
PID7							
R							
0h							
23	22	21	20	19	18	17	16
PID7							
R							
0h							
15	14	13	12	11	10	9	8
PID7							
R							
0h							
7	6	5	4	3	2	1	0
PID6							
R							
0h							

Table 14-26713. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	PID7	R	0h	
7:0	PID6	R	0h	Read 0x0 : As per CoreSight Architecture Specification

14.11.1.2.269 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID7 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID7 Register (Offset = FDCh) [reset = 0h]

Peripheral Identification Register Number 7 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-26714. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FDCh**

Figure 14-8810. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PID7							
R							
0h							

Table 14-26716. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	PID7	R	0h	Read 0x0 : As per CoreSight Architecture Specification

14.11.1.2.270 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID0 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 223h]

Peripheral Identification Register Number 0 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-26717. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FE0h**

Figure 14-8811. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
2h							
23	22	21	20	19	18	17	16
RESERVED							
R							
2h							
15	14	13	12	11	10	9	8
RESERVED							
R							
2h							
7	6	5	4	3	2	1	0
PART_ML							
R							
23h							

Table 14-26719. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	2h	
7:0	PART_ML	R	23h	The middle and lower BCD value of the part number. Read 0xDF : CT-TBR BCD part number is EDF

14.11.1.2.271 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID1 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 126h]

Peripheral Identification Register Number 1 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-26720. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FE4h**

Figure 14-8812. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
1h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JEPID_L				PART_U			
R				R			
2h				6h			

Table 14-26722. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	1h	
7:4	JEPID_L	R	2h	JEP106 ID[3 : 0]. Read 0x7 : TI JEP106 ID is 0x17
3:0	PART_U	R	6h	The upper BCD value of the part number. Read 0xE : CT-TBR BCD part number is EDF

14.11.1.2.272 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID2 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 24h]

Peripheral Identification Register Number 2 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-26723. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FE8h**

Figure 14-8813. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
REVNUM				JEDEC	JEPID_H		
R				R	R		
2h				0h	4h		

Table 14-26725. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	REVNUM	R	2h	Revision number of the peripheral module Read 0x0 : Only revision of CT-TBR
3	JEDEC	R	0h	Indicates JEDEC ID was used Read 0x1 : JEDEC ID is used
2:0	JEPID_H	R	4h	JEP106 ID[6 : 4]. Read 0x1 : TI JEP106 ID is 0x17

14.11.1.2.273 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID3 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Peripheral Identification Register Number 3 The Peripheral ID registers indicate module specifics like manufacturer and part number

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Table 14-26726. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FECh**

Figure 14-8814. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
REVAND				CUSTMOD			
R				R			
0h				0h			

Table 14-26728. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:4	REVAND	R	0h	Indicates the errata fix version of the IP Read 0x0 : CT-TBR uses one block
3:0	CUSTMOD	R	0h	Indicates that the module was reusable IP that was modified by the customer Read 0x0 : CT-TBR is native IP

14.11.1.2.274 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID0 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID0 Register (Offset = FF0h) [reset = 13h]

Component Identification Register Number 0 The Component ID registers places a known bit pattern in memory that indicates that a 4K configuration block is valid and supports a peripheral

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Table 14-26729. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FF0h**

Figure 14-8815. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
CID1							
R							
0h							
23	22	21	20	19	18	17	16
CID1							
R							
0h							
15	14	13	12	11	10	9	8
CID1							
R							
0h							
7	6	5	4	3	2	1	0
CID0							
R							
13h							

Table 14-26731. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CID1	R	0h	
7:0	CID0	R	13h	The fixed preamble for the component ID Read 0x0D : CID0 Preamble is fixed at 0x0D

14.11.1.2.275 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID1 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID1 Register (Offset = FF4h) [reset = 144h]

Component Identification Register Number 1 The Component ID registers places a known bit pattern in memory that indicates that a 4K configuration block is valid and supports a peripheral

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Table 14-26732. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FF4h**

Figure 14-8816. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLASS1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLASS1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLASS1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CLASS</td><td colspan="4">CID1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">4h</td><td colspan="4">4h</td></tr>
</table>

Table 14-26734. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CLASS1	R	1h	
7:4	CLASS	R	4h	Indicates the class of the component Read 0x9 : CT-TBR is a CoreSight component
3:0	CID1	R	4h	The fixed preamble for the component ID Read 0x0 : CID1 Preamble is fixed at 0x0

14.11.1.2.276 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID2 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

Component Identification Register Number 2 The Component ID registers places a known bit pattern in memory that indicates that a 4K configuration block is valid and supports a peripheral

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Table 14-26735. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FF8h**

Figure 14-8817. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CID2							
R							
5h							

Table 14-26737. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	CID2	R	5h	The fixed preamble for the component ID Read 0x05 : CID2 Preamble is fixed at 0x05

14.11.1.2.277 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID3 Register

1 DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID3 Register (Offset = FFCh) [reset = 177h]

2Component Identification Register Number 3 The Component ID registers places a known bit pattern in memory that indicates that a 4K configuration block is valid and supports a peripheral

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Table 14-26738. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 5FFCh**

Figure 14-8818. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
1h							
23	22	21	20	19	18	17	16
RESERVED							
R							
1h							
15	14	13	12	11	10	9	8
RESERVED							
R							
1h							
7	6	5	4	3	2	1	0
CID3							
R							
77h							

Table 14-26740. DEBUGSS_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	1h	
7:0	CID3	R	77h	The fixed preamble for the component ID Read 0x05 : CID2 Preamble is fixed at 0x05

14.11.1.2.278 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-26741. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-8819. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-26743. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.279 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-26744. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 F010h**

Figure 14-8820. CSCTI_CFG_CTIINTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTACK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26746. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.280 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-26747. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F014h

Figure 14-8821. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-26749. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.281 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-26750. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-8822. CSCTI_CFG_CTIAPPCLEAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPCLEAR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26752. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.282 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cti533clk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-26753. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-8823. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-26755. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.283 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26756. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F020h

Figure 14-8824. CSCTI_CFG_CTIINEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26758. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.284 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26759. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-8825. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26761. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.285 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26762. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F028h

Figure 14-8826. CSCTI_CFG_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26764. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.286 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26765. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-8827. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26767. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.287 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26768. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-8828. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26770. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.288 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26771. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-8829. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26773. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.289 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26774. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-8830. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26776. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.290 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26777. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-8831. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26779. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.291 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26780. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-8832. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26782. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.292 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26783. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-8833. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26785. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.293 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26786. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-8834. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26788. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.294 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26789. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-8835. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26791. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.295 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26792. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-8836. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26794. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.296 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26795. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-8837. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26797. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.297 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26798. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-8838. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26800. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.298 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26801. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-8839. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26803. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.299 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-26804. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-8840. CSCTI_CFG_CTITRIGINSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRIGINSTATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26806. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.300 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-26807. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-8841. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-26809. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.301 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-26810. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-8842. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-26812. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.302 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-26813. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-8843. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-26815. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.303 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-26816. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-8844. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-26818. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.304 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-26819. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-8845. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-26821. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.305 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-26822. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-8846. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-26824. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.306 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-26825. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-8847. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-26827. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.307 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-26828. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-8848. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-26830. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.308 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-26831. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-8849. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-26833. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.309 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-26834. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-8850. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-26836. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.310 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-26837. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-8851. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-26839. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.311 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-26840. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-8852. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-26842. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.312 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-26843. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-8853. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-26845. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.313 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-26846. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-8854. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-26848. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.314 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-26849. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-8855. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-26851. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.315 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-26852. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-8856. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-26854. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.316 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-26855. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-8857. CSCTI_CFG_LAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-26857. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.317 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-26858. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-8858. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-26860. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.318 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-26861. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-8859. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-26863. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.319 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-26864. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-8860. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							
7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-26866. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.320 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-26867. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-8861. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-26869. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.321 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-26870. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-8862. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R				R			
0h				4h			

Table 14-26872. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.322 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-26873. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-8863. CSCTI_CFG_PERIPHID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PART_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6h</td></tr>
</table>

Table 14-26875. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.323 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-26876. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFE4h

Figure 14-8864. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-26878. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.324 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-26879. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-8865. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-26881. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.325 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-26882. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-8866. CSCTI_CFG_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26884. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.326 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-26885. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-8867. CSCTI_CFG_COMPID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Dh</td></tr>
</table>

Table 14-26887. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.327 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-26888. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFF4h

Figure 14-8868. CSCTI_CFG_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-26890. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.328 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-26891. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-8869. CSCTI_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-26893. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.329 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-26894. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-8870. CSCTI_CFG_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-26896. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.1.2.330 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-26897. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-8871. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-26899. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.331 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-26900. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-8872. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-26902. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.332 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-26903. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-8873. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-26905. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.333 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-26906. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-8874. CSCTI_CFG_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-26908. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.334 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-26909. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-8875. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-26911. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.335 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26912. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-8876. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26914. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.336 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26915. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-8877. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26917. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.337 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26918. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-8878. CSCTI_CFG_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26920. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.338 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26921. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-8879. CSCTI_CFG_CTIINEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26923. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.339 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26924. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-8880. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26926. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.340 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26927. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-8881. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26929. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.341 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26930. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-8882. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-26932. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.342 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-26933. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-8883. CSCTI_CFG_CTIINEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26935. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.343 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26936. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-8884. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26938. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.344 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-26939. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-8885. CSCTI_CFG_CTIOUTEN1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26941. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.345 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26942. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-8886. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26944. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.346 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26945. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-8887. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26947. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.347 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-26948. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-8888. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26950. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.348 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26951. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-8889. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26953. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.349 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26954. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-8890. CSCTI_CFG_CTIOUTEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26956. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.350 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-26957. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-8891. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-26959. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.351 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-26960. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-8892. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-26962. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.352 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-26963. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-8893. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-26965. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.353 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-26966. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-8894. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-26968. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.354 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-26969. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-8895. CSCTI_CFG_CTICHOUTSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTICHOUTSTATUS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26971. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.355 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-26972. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-8896. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-26974. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.356 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-26975. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-8897. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-26977. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.357 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-26978. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-8898. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-26980. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.358 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-26981. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-8899. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-26983. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.359 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-26984. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-8900. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-26986. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.360 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-26987. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-8901. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-26989. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.361 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-26990. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-8902. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-26992. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.362 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-26993. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-8903. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-26995. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.363 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-26996. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-8904. CSCTI_CFG_ITCHIN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHIN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-26998. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.364 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-26999. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-8905. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-27001. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.365 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-27002. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-8906. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-27004. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.366 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-27005. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-8907. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-27007. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.367 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-27008. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-8908. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-27010. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.368 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-27011. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-8909. CSCTI_CFG_LAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACCESS_W</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27013. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.369 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-27014. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-8910. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-27016. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.370 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-27017. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-8911. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-27019. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.371 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-27020. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-8912. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							
7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-27022. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.372 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-27023. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-8913. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-27025. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.373 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-27026. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-8914. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-27028. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.374 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-27029. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-8915. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-27031. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.375 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-27032. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-8916. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-27034. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.376 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-27035. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-8917. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-27037. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.377 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-27038. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-8918. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-27040. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.378 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-27041. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-8919. CSCTI_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-27043. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.379 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-27044. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-8920. CSCTI_CFG_COMPID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CLASS</td><td colspan="4">PRMBL_1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27046. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.380 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27047. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFF8h

Figure 14-8921. CSCTI_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-27049. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.381 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27050. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-8922. CSCTI_CFG_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-27052. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.1.2.382 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-27053. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-8923. CSCTI_CFG_CTICONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>GLBEN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-27055. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.383 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-27056. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-8924. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-27058. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.384 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-27059. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-8925. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-27061. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.385 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-27062. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-8926. CSCTI_CFG_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-27064. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.386 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticzłonk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-27065. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-8927. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-27067. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.387 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27068. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F020h

Figure 14-8928. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27070. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.388 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27071. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-8929. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27073. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.389 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27074. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-8930. CSCTI_CFG_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27076. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.390 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27077. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-8931. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27079. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.391 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27080. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-8932. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27082. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.392 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27083. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-8933. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27085. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.393 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27086. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-8934. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27088. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.394 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27089. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F03Ch

Figure 14-8935. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27091. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.395 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27092. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-8936. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27094. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.396 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27095. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-8937. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27097. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.397 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27098. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-8938. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27100. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.398 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27101. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-8939. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27103. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.399 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27104. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-8940. CSCTI_CFG_CTIOUTEN4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27106. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.400 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-27107. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-8941. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27109. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.401 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-27110. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-8942. CSCTI_CFG_CTIOUTEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27112. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.402 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-27113. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-8943. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27115. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.403 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-27116. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-8944. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-27118. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.404 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

Return to Summary Table

Table 14-27119. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-8945. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-27121. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.405 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

Return to Summary Table

Table 14-27122. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-8946. CSCTI_CFG_CTICHINSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTICHINSTATUS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27124. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.406 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-27125. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-8947. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-27127. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.407 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-27128. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-8948. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-27130. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.408 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-27131. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-8949. CSCTI_CFG_ASICCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ASICCTL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27133. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.409 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-27134. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-8950. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-27136. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.410 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-27137. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FEE0h

Figure 14-8951. CSCTI_CFG_ITTRIGINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGINACK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27139. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.411 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-27140. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-8952. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-27142. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.412 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

Return to Summary Table

Table 14-27143. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-8953. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-27145. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.413 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

Return to Summary Table

Table 14-27146. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-8954. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-27148. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.414 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

Return to Summary Table

Table 14-27149. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-8955. CSCTI_CFG_ITTRIGOUTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGOUTACK</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27151. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.415 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-27152. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-8956. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-27154. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.416 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-27155. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-8957. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-27157. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.417 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-27158. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-8958. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-27160. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.418 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-27161. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-8959. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-27163. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.419 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-27164. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-8960. CSCTI_CFG_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMCLR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27166. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.420 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-27167. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-8961. CSCTI_CFG_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-27169. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.421 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-27170. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-8962. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-27172. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.422 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-27173. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-8963. CSCTI_CFG_AUTHSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SNID</td><td colspan="2">SID</td><td colspan="2">NSNID</td><td colspan="2">NSID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">2h</td><td colspan="2">2h</td></tr>
</table>

Table 14-27175. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.423 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-27176. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFC8h

Figure 14-8964. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							
7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-27178. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.424 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-27179. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-8965. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-27181. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.425 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-27182. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-8966. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-27184. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.426 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-27185. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-8967. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-27187. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.427 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-27188. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFE4h

Figure 14-8968. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-27190. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.428 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-27191. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-8969. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-27193. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.429 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-27194. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-8970. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-27196. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.430 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-27197. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-8971. CSCTI_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-27199. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.431 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-27200. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-8972. CSCTI_CFG_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-27202. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.432 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27203. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-8973. CSCTI_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-27205. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.433 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27206. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-8974. CSCTI_CFG_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-27208. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.1.2.434 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-27209. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F000h

Figure 14-8975. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-27211. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.435 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-27212. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-8976. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-27214. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.436 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-27215. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-8977. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-27217. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.437 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-27218. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F018h

Figure 14-8978. CSCTI_CFG_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-27220. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.438 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-27221. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-8979. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-27223. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.439 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27224. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-8980. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27226. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.440 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27227. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-8981. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27229. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.441 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27230. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-8982. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27232. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.442 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27233. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-8983. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27235. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.443 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27236. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-8984. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27238. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.444 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27239. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-8985. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27241. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.445 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27242. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-8986. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27244. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.446 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27245. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-8987. CSCTI_CFG_CTIINEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27247. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.447 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27248. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-8988. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27250. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.448 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27251. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-8989. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27253. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.449 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27254. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-8990. CSCTI_CFG_CTIOUTEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27256. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.450 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27257. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-8991. CSCTI_CFG_CTIOUTEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27259. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.451 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27260. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-8992. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27262. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.452 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27263. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-8993. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27265. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.453 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27266. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-8994. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27268. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.454 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27269. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-8995. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27271. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.455 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-27272. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-8996. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGINSTATUS							
R							
0h							

Table 14-27274. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.456 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-27275. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-8997. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-27277. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.457 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-27278. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-8998. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-27280. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.458 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-27281. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-8999. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-27283. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.459 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-27284. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-9000. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-27286. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.460 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-27287. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-9001. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ASICCTL							
R/W							
0h							

Table 14-27289. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.461 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-27290. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-9002. CSCTI_CFG_ITCHINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHINACK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27292. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.462 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-27293. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-9003. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-27295. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.463 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-27296. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-9004. CSCTI_CFG_ITCHOUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHOUT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27298. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.464 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-27299. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-9005. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-27301. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.465 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-27302. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-9006. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-27304. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.466 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-27305. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-9007. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-27307. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.467 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-27308. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-9008. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-27310. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.468 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-27311. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-9009. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-27313. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.469 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-27314. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-9010. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-27316. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.470 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-27317. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-9011. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-27319. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.471 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-27320. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-9012. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-27322. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.472 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-27323. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-9013. CSCTI_CFG_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-27325. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.473 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-27326. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-9014. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-27328. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.474 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-27329. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-9015. CSCTI_CFG_AUTHSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SNID</td><td colspan="2">SID</td><td colspan="2">NSNID</td><td colspan="2">NSID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">2h</td><td colspan="2">2h</td></tr>
</table>

Table 14-27331. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.475 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-27332. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-9016. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NUMTRIG							
R							
8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-27334. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.476 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-27335. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-9017. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-27337. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.477 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-27338. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-9018. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-27340. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.478 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-27341. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-9019. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-27343. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.479 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-27344. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-9020. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-27346. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.480 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-27347. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-9021. CSCTI_CFG_PERIPHID2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVISION</td><td>JEDEC</td><td colspan="3">DES_1</td></tr>
<tr><td colspan="4">R</td><td>R</td><td colspan="3">R</td></tr>
<tr><td colspan="4">4h</td><td>1h</td><td colspan="3">0h</td></tr>
</table>

Table 14-27349. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.481 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-27350. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-9022. CSCTI_CFG_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27352. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.482 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-27353. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-9023. CSCTI_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-27355. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.483 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-27356. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-9024. CSCTI_CFG_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-27358. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.484 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27359. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-9025. CSCTI_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-27361. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.485 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27362. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-9026. CSCTI_CFG_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRMBL_3							
R							
0h							

Table 14-27364. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.1.2.486 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-27365. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-9027. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-27367. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.487 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-27368. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-9028. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-27370. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.488 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-27371. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-9029. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-27373. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.489 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-27374. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-9030. CSCTI_CFG_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-27376. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.490 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-27377. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-9031. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-27379. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.491 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27380. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-9032. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27382. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.492 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27383. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F024h

Figure 14-9033. CSCTI_CFG_CTIINEN1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27385. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.493 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27386. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-9034. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27388. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.494 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27389. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F02Ch

Figure 14-9035. CSCTI_CFG_CTIINEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27391. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.495 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27392. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-9036. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27394. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.496 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27395. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F034h

Figure 14-9037. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27397. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.497 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27398. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F038h

Figure 14-9038. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27400. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.498 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27401. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-9039. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27403. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.499 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27404. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-9040. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27406. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.500 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27407. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-9041. CSCTI_CFG_CTIOUTEN1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27409. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.501 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27410. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-9042. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27412. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.502 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27413. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-9043. CSCTI_CFG_CTIOUTEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27415. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.503 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27416. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-9044. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27418. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.504 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27419. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-9045. CSCTI_CFG_CTIOUTEN5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27421. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.505 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27422. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-9046. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27424. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.506 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27425. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-9047. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27427. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.507 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-27428. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-9048. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-27430. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.508 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-27431. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-9049. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-27433. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.509 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-27434. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-9050. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-27436. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.510 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-27437. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-9051. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-27439. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.511 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-27440. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F140h

Figure 14-9052. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-27442. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.512 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-27443. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-9053. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-27445. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.513 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-27446. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-9054. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-27448. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.514 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-27449. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-9055. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-27451. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.515 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-27452. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-9056. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-27454. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.516 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-27455. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-9057. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-27457. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.517 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-27458. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-9058. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-27460. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.518 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-27461. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-9059. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-27463. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.519 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-27464. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-9060. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-27466. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.520 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-27467. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-9061. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-27469. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.521 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-27470. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-9062. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-27472. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.522 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-27473. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-9063. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-27475. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.523 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-27476. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-9064. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-27478. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.524 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-27479. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-9065. CSCTI_CFG_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-27481. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.525 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-27482. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-9066. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-27484. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.526 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-27485. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-9067. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-27487. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.527 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-27488. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-9068. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NUMTRIG							
R							
8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-27490. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.528 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-27491. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-9069. CSCTI_CFG_DEVTYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SUB_TYPE</td><td colspan="4">MAJOR_TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">4h</td></tr>
</table>

Table 14-27493. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.529 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-27494. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-9070. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-27496. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.530 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-27497. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-9071. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-27499. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.531 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-27500. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-9072. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-27502. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.532 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-27503. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-9073. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-27505. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.533 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-27506. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-9074. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-27508. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.534 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-27509. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-9075. CSCTI_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-27511. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.535 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-27512. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFF4h

Figure 14-9076. CSCTI_CFG_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-27514. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.536 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27515. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-9077. CSCTI_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-27517. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.537 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27518. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-9078. CSCTI_CFG_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-27520. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.1.2.538 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-27521. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-9079. CSCTI_CFG_CTICONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>GLBEN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-27523. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.539 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-27524. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-9080. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-27526. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.540 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-27527. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F014h

Figure 14-9081. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-27529. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.541 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-27530. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-9082. CSCTI_CFG_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-27532. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.542 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-27533. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-9083. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-27535. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.543 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27536. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-9084. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27538. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.544 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27539. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F024h

Figure 14-9085. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27541. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.545 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27542. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-9086. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27544. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.546 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27545. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-9087. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27547. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.547 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27548. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-9088. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27550. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.548 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27551. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-9089. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27553. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.549 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27554. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F038h

Figure 14-9090. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27556. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.550 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27557. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-9091. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27559. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.551 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27560. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-9092. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27562. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.552 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27563. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-9093. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27565. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.553 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27566. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-9094. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27568. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.554 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27569. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-9095. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27571. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.555 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27572. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-9096. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27574. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.556 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27575. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-9097. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27577. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.557 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27578. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-9098. CSCTI_CFG_CTIOUTEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27580. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.558 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27581. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-9099. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27583. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.559 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-27584. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-9100. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-27586. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.560 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-27587. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-9101. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-27589. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.561 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-27590. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-9102. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-27592. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.562 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-27593. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-9103. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-27595. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.563 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-27596. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-9104. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-27598. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.564 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-27599. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-9105. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-27601. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.565 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-27602. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-9106. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-27604. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.566 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-27605. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-9107. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-27607. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.567 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-27608. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-9108. CSCTI_CFG_ITCHOUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHOUT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27610. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.568 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-27611. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-9109. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-27613. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.569 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-27614. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-9110. CSCTI_CFG_ITCHOUTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHOUTACK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27616. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.570 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-27617. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-9111. CSCTI_CFG_ITTRIGOUTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGOUTACK</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27619. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.571 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-27620. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FEF4h

Figure 14-9112. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-27622. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.572 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-27623. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-9113. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-27625. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.573 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-27626. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-9114. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-27628. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.574 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-27629. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-9115. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-27631. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.575 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-27632. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-9116. CSCTI_CFG_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMCLR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27634. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.576 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-27635. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-9117. CSCTI_CFG_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-27637. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.577 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-27638. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-9118. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-27640. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.578 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-27641. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-9119. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-27643. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.579 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-27644. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFC8h

Figure 14-9120. CSCTI_CFG_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUMCH</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUMTRIG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EXTMUXNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-27646. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.580 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-27647. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-9121. CSCTI_CFG_DEVTYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SUB_TYPE</td><td colspan="4">MAJOR_TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">1h</td><td colspan="4">4h</td></tr>
</table>

Table 14-27649. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.581 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-27650. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-9122. CSCTI_CFG_PERIPHID4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SIZE</td><td colspan="4">DES_2</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-27652. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.582 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-27653. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-9123. CSCTI_CFG_PERIPHID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PART_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6h</td></tr>
</table>

Table 14-27655. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.583 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-27656. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFE4h

Figure 14-9124. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-27658. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.584 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-27659. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-9125. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-27661. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.585 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-27662. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFECh

Figure 14-9126. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-27664. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.586 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-27665. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-9127. CSCTI_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-27667. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.587 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-27668. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-9128. CSCTI_CFG_COMPID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CLASS</td><td colspan="4">PRMBL_1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27670. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.588 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27671. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-9129. CSCTI_CFG_COMPID2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">5h</td></tr>
</table>

Table 14-27673. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.589 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27674. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-9130. CSCTI_CFG_COMPID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27676. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.1.2.590 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-27677. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-9131. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-27679. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.591 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-27680. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-9132. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-27682. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.592 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-27683. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-9133. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-27685. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.593 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-27686. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-9134. CSCTI_CFG_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-27688. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.594 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-27689. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-9135. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-27691. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.595 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27692. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F020h

Figure 14-9136. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27694. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.596 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27695. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-9137. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27697. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.597 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27698. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-9138. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27700. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.598 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27701. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-9139. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27703. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.599 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27704. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-9140. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27706. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.600 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27707. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-9141. CSCTI_CFG_CTIINEN5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27709. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.601 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27710. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F038h

Figure 14-9142. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27712. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.602 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27713. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-9143. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27715. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.603 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27716. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-9144. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27718. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.604 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27719. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-9145. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27721. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.605 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27722. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-9146. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27724. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.606 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27725. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-9147. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27727. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.607 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27728. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-9148. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27730. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.608 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27731. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-9149. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27733. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.609 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27734. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-9150. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27736. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.610 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27737. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-9151. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27739. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.611 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-27740. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-9152. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-27742. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.612 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-27743. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-9153. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-27745. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.613 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-27746. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-9154. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-27748. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.614 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-27749. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-9155. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-27751. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.615 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-27752. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-9156. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-27754. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.616 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-27755. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-9157. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-27757. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.617 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-27758. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-9158. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-27760. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.618 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-27761. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-9159. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-27763. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.619 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-27764. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-9160. CSCTI_CFG_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-27766. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.620 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-27767. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-9161. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-27769. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.621 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-27770. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-9162. CSCTI_CFG_ITCHOUTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHOUTACK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27772. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.622 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-27773. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-9163. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-27775. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.623 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-27776. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-9164. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-27778. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.624 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-27779. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-9165. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-27781. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.625 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-27782. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-9166. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-27784. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.626 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-27785. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-9167. CSCTI_CFG_CLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27787. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.627 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-27788. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-9168. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-27790. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.628 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-27791. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-9169. CSCTI_CFG_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-27793. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.629 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-27794. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-9170. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-27796. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.630 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-27797. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-9171. CSCTI_CFG_AUTHSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SNID</td><td colspan="2">SID</td><td colspan="2">NSNID</td><td colspan="2">NSID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">2h</td><td colspan="2">2h</td></tr>
</table>

Table 14-27799. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.631 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-27800. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-9172. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							
7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-27802. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.632 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-27803. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFCCh**

Figure 14-9173. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-27805. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.633 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-27806. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-9174. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-27808. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.634 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-27809. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-9175. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-27811. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.635 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-27812. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-9176. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-27814. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.636 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-27815. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-9177. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-27817. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.637 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-27818. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-9178. CSCTI_CFG_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-27820. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.638 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-27821. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-9179. CSCTI_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-27823. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.639 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-27824. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-9180. CSCTI_CFG_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-27826. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.640 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27827. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-9181. CSCTI_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-27829. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.641 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27830. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-9182. CSCTI_CFG_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-27832. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.1.2.642 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-27833. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-9183. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-27835. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.643 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-27836. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-9184. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-27838. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.644 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-27839. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-9185. CSCTI_CFG_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
NONE				R/W			
0h				0h			

Table 14-27841. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.645 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-27842. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-9186. CSCTI_CFG_CTIAPPCLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-27844. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.646 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-27845. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-9187. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-27847. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.647 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27848. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F020h

Figure 14-9188. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27850. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.648 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27851. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F024h**

Figure 14-9189. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27853. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.649 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27854. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-9190. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27856. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.650 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27857. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F02Ch**

Figure 14-9191. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27859. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.651 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27860. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F030h

Figure 14-9192. CSCTI_CFG_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27862. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.652 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27863. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-9193. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27865. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.653 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27866. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F038h

Figure 14-9194. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27868. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.654 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-27869. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-9195. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-27871. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.655 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27872. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-9196. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27874. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.656 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27875. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-9197. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27877. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.657 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27878. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-9198. CSCTI_CFG_CTIOUTEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27880. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.658 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27881. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-9199. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27883. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.659 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27884. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-9200. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27886. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.660 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27887. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-9201. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27889. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.661 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27890. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-9202. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27892. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.662 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-27893. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-9203. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-27895. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.663 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-27896. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-9204. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-27898. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.664 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

Return to Summary Table

Table 14-27899. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-9205. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-27901. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.665 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-27902. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-9206. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-27904. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.666 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-27905. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-9207. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-27907. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.667 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-27908. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-9208. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-27910. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.668 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-27911. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-9209. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-27913. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.669 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-27914. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-9210. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-27916. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.670 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-27917. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-9211. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-27919. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.671 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-27920. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-9212. CSCTI_CFG_ITCHOUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHOUT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27922. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.672 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-27923. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-9213. CSCTI_CFG_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-27925. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.673 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-27926. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-9214. CSCTI_CFG_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-27928. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.674 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-27929. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FEF0h

Figure 14-9215. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-27931. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.675 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-27932. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-9216. CSCTI_CFG_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
NONE				R			
0h				0h			

Table 14-27934. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.676 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-27935. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FEF8h

Figure 14-9217. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-27937. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.677 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-27938. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-9218. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-27940. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.678 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-27941. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-9219. CSCTI_CFG_CLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27943. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.679 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-27944. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-9220. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-27946. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.680 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-27947. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB0h**

Figure 14-9221. CSCTI_CFG_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-27949. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.681 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-27950. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-9222. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-27952. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.682 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-27953. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-9223. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-27955. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.683 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-27956. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-9224. CSCTI_CFG_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUMCH</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUMTRIG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EXTMUXNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-27958. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.684 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-27959. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFCCh

Figure 14-9225. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-27961. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.685 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-27962. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-9226. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE				DES_2			
R				R			
0h				4h			

Table 14-27964. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.686 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-27965. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE0h**

Figure 14-9227. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-27967. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.687 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-27968. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-9228. CSCTI_CFG_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-27970. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.688 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-27971. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE8h**

Figure 14-9229. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-27973. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.689 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-27974. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFECh

Figure 14-9230. CSCTI_CFG_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27976. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.690 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-27977. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFF0h

Figure 14-9231. CSCTI_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-27979. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.691 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-27980. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-9232. CSCTI_CFG_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-27982. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.692 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27983. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-9233. CSCTI_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-27985. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.693 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-27986. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-9234. CSCTI_CFG_COMPID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-27988. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.1.2.694 CSCTI_CFG_CTICONTROL Register

1 CSCTI_CFG_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-27989. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F000h**

Figure 14-9235. CSCTI_CFG_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-27991. CSCTI_CFG_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.11.1.2.695 CSCTI_CFG_CTIINTACK Register

1 CSCTI_CFG_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-27992. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F010h**

Figure 14-9236. CSCTI_CFG_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-27994. CSCTI_CFG_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.696 CSCTI_CFG_CTIAPPSET Register

1 CSCTI_CFG_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-27995. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F014h**

Figure 14-9237. CSCTI_CFG_CTIAPPSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-27997. CSCTI_CFG_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.11.1.2.697 CSCTI_CFG_CTIAPPCLEAR Register

1 CSCTI_CFG_CTIAPPCLEAR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-27998. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F018h**

Figure 14-9238. CSCTI_CFG_CTIAPPCLEAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPCLEAR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28000. CSCTI_CFG_CTIAPPCLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.698 CSCTI_CFG_CTIAPPPULSE Register

1 CSCTI_CFG_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one ctialgn period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-28001. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F01Ch**

Figure 14-9239. CSCTI_CFG_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPULSE			
NONE				R/W			
0h				0h			

Table 14-28003. CSCTI_CFG_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one ctialgn period. Writing a 0 to any of the bits in this register has no effect.

14.11.1.2.699 CSCTI_CFG_CTIINEN0 Register

1 CSCTI_CFG_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-28004. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F020h**

Figure 14-9240. CSCTI_CFG_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-28006. CSCTI_CFG_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.700 CSCTI_CFG_CTIINEN1 Register

1 CSCTI_CFG_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-28007. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F024h

Figure 14-9241. CSCTI_CFG_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-28009. CSCTI_CFG_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.701 CSCTI_CFG_CTIINEN2 Register

1 CSCTI_CFG_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-28010. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F028h**

Figure 14-9242. CSCTI_CFG_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-28012. CSCTI_CFG_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.702 CSCTI_CFG_CTIINEN3 Register

1 CSCTI_CFG_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-28013. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 F02Ch

Figure 14-9243. CSCTI_CFG_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-28015. CSCTI_CFG_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.703 CSCTI_CFG_CTIINEN4 Register

1 CSCTI_CFG_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-28016. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F030h**

Figure 14-9244. CSCTI_CFG_CTIINEN4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28018. CSCTI_CFG_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.704 CSCTI_CFG_CTIINEN5 Register

1 CSCTI_CFG_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-28019. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F034h**

Figure 14-9245. CSCTI_CFG_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-28021. CSCTI_CFG_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.705 CSCTI_CFG_CTIINEN6 Register

1 CSCTI_CFG_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-28022. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F038h**

Figure 14-9246. CSCTI_CFG_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-28024. CSCTI_CFG_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.706 CSCTI_CFG_CTIINEN7 Register

1 CSCTI_CFG_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-28025. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F03Ch**

Figure 14-9247. CSCTI_CFG_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-28027. CSCTI_CFG_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.11.1.2.707 CSCTI_CFG_CTIOUTEN0 Register

1 CSCTI_CFG_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-28028. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A0h**

Figure 14-9248. CSCTI_CFG_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-28030. CSCTI_CFG_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.708 CSCTI_CFG_CTIOUTEN1 Register

1 CSCTI_CFG_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-28031. Instance Table

Instance Name	**Physical Address**
DEBUGSS0	**0007 3C02 F0A4h**

Figure 14-9249. CSCTI_CFG_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-28033. CSCTI_CFG_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.709 CSCTI_CFG_CTIOUTEN2 Register

1 CSCTI_CFG_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-28034. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0A8h**

Figure 14-9250. CSCTI_CFG_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-28036. CSCTI_CFG_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.710 CSCTI_CFG_CTIOUTEN3 Register

1 CSCTI_CFG_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-28037. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0ACh**

Figure 14-9251. CSCTI_CFG_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-28039. CSCTI_CFG_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.711 CSCTI_CFG_CTIOUTEN4 Register

1 CSCTI_CFG_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-28040. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B0h**

Figure 14-9252. CSCTI_CFG_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-28042. CSCTI_CFG_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.712 CSCTI_CFG_CTIOUTEN5 Register

1 CSCTI_CFG_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-28043. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B4h**

Figure 14-9253. CSCTI_CFG_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-28045. CSCTI_CFG_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.713 CSCTI_CFG_CTIOUTEN6 Register

1 CSCTI_CFG_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-28046. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0B8h**

Figure 14-9254. CSCTI_CFG_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-28048. CSCTI_CFG_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.714 CSCTI_CFG_CTIOUTEN7 Register

1 CSCTI_CFG_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-28049. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F0BCh**

Figure 14-9255. CSCTI_CFG_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-28051. CSCTI_CFG_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.11.1.2.715 CSCTI_CFG_CTITRIGINSTATUS Register

1 CSCTI_CFG_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-28052. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F130h**

Figure 14-9256. CSCTI_CFG_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-28054. CSCTI_CFG_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.11.1.2.716 CSCTI_CFG_CTITRIGOUTSTATUS Register

1 CSCTI_CFG_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

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Table 14-28055. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F134h**

Figure 14-9257. CSCTI_CFG_CTITRIGOUTSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRIGOUTSTATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28057. CSCTI_CFG_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.11.1.2.717 CSCTI_CFG_CTICHINSTATUS Register

1 CSCTI_CFG_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-28058. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F138h**

Figure 14-9258. CSCTI_CFG_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-28060. CSCTI_CFG_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.11.1.2.718 CSCTI_CFG_CTICHOUTSTATUS Register

1 CSCTI_CFG_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-28061. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F13Ch**

Figure 14-9259. CSCTI_CFG_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-28063. CSCTI_CFG_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.11.1.2.719 CSCTI_CFG_CTIGATE Register

1 CSCTI_CFG_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-28064. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F140h**

Figure 14-9260. CSCTI_CFG_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-28066. CSCTI_CFG_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.11.1.2.720 CSCTI_CFG_ASICCTL Register

1 CSCTI_CFG_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-28067. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 F144h**

Figure 14-9261. CSCTI_CFG_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-28069. CSCTI_CFG_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.11.1.2.721 CSCTI_CFG_ITCHINACK Register

1 CSCTI_CFG_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-28070. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEDCh**

Figure 14-9262. CSCTI_CFG_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-28072. CSCTI_CFG_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.11.1.2.722 CSCTI_CFG_ITTRIGINACK Register

1 CSCTI_CFG_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-28073. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE0h**

Figure 14-9263. CSCTI_CFG_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-28075. CSCTI_CFG_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.11.1.2.723 CSCTI_CFG_ITCHOUT Register

1 CSCTI_CFG_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-28076. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE4h**

Figure 14-9264. CSCTI_CFG_ITCHOUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHOUT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28078. CSCTI_CFG_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.11.1.2.724 CSCTI_CFG_ITTRIGOUT Register

1 CSCTI_CFG_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

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Table 14-28079. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEE8h**

Figure 14-9265. CSCTI_CFG_ITTRIGOUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGOUT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28081. CSCTI_CFG_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.11.1.2.725 CSCTI_CFG_ITCHOUTACK Register

1 CSCTI_CFG_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-28082. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEECh**

Figure 14-9266. CSCTI_CFG_ITCHOUTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHOUTACK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28084. CSCTI_CFG_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.11.1.2.726 CSCTI_CFG_ITTRIGOUTACK Register

1 CSCTI_CFG_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-28085. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF0h**

Figure 14-9267. CSCTI_CFG_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-28087. CSCTI_CFG_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.11.1.2.727 CSCTI_CFG_ITCHIN Register

1 CSCTI_CFG_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-28088. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF4h**

Figure 14-9268. CSCTI_CFG_ITCHIN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHIN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28090. CSCTI_CFG_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.11.1.2.728 CSCTI_CFG_ITTRIGIN Register

1 CSCTI_CFG_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-28091. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FEF8h**

Figure 14-9269. CSCTI_CFG_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-28093. CSCTI_CFG_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.11.1.2.729 CSCTI_CFG_ITCTRL Register

1 CSCTI_CFG_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-28094. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FF00h**

Figure 14-9270. CSCTI_CFG_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGRATION_MODE
NONE							R/W
0h							0h

Table 14-28096. CSCTI_CFG_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.11.1.2.730 CSCTI_CFG_CLAIMSET Register

1 CSCTI_CFG_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-28097. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA0h**

Figure 14-9271. CSCTI_CFG_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMSET			
NONE				R/W			
0h				0h			

Table 14-28099. CSCTI_CFG_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.11.1.2.731 CSCTI_CFG_CLAIMCLR Register

1 CSCTI_CFG_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-28100. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFA4h**

Figure 14-9272. CSCTI_CFG_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-28102. CSCTI_CFG_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.11.1.2.732 CSCTI_CFG_LAR Register

1 CSCTI_CFG_LAR Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-28103. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFB0h

Figure 14-9273. CSCTI_CFG_LAR Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-28105. CSCTI_CFG_LAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.11.1.2.733 CSCTI_CFG_LSR Register

1 CSCTI_CFG_LSR Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-28106. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB4h**

Figure 14-9274. CSCTI_CFG_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LOCKTYPE	LOCKGRANT	LOCKEXIST
NONE					R	R	R
0h					0h	1h	1h

Table 14-28108. CSCTI_CFG_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.11.1.2.734 CSCTI_CFG_AUTHSTATUS Register

1 CSCTI_CFG_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-28109. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFB8h**

Figure 14-9275. CSCTI_CFG_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-28111. CSCTI_CFG_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.11.1.2.735 CSCTI_CFG_DEVID Register

1 CSCTI_CFG_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-28112. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFC8h**

Figure 14-9276. CSCTI_CFG_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				NUMCH			
NONE				R			
0h				4h			
15	14	13	12	11	10	9	8
NUMTRIG							
R							
8h							
7	6	5	4	3	2	1	0
RESERVED			EXTMUXNUM				
NONE			R				
0h			0h				

Table 14-28114. CSCTI_CFG_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.11.1.2.736 CSCTI_CFG_DEVTYPE Register

1 CSCTI_CFG_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-28115. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFCCh

Figure 14-9277. CSCTI_CFG_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-28117. CSCTI_CFG_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.11.1.2.737 CSCTI_CFG_PERIPHID4 Register

1 CSCTI_CFG_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-28118. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFD0h**

Figure 14-9278. CSCTI_CFG_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-28120. CSCTI_CFG_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.11.1.2.738 CSCTI_CFG_PERIPHID0 Register

1 CSCTI_CFG_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

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Table 14-28121. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFE0h

Figure 14-9279. CSCTI_CFG_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-28123. CSCTI_CFG_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.11.1.2.739 CSCTI_CFG_PERIPHID1 Register

1 CSCTI_CFG_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-28124. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFE4h**

Figure 14-9280. CSCTI_CFG_PERIPHID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">DES_0</td><td colspan="4">PART_1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">9h</td></tr>
</table>

Table 14-28126. CSCTI_CFG_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.11.1.2.740 CSCTI_CFG_PERIPHID2 Register

1 CSCTI_CFG_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-28127. Instance Table

Instance Name	Physical Address
DEBUGSS0	0007 3C02 FFE8h

Figure 14-9281. CSCTI_CFG_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-28129. CSCTI_CFG_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.11.1.2.741 CSCTI_CFG_PERIPHID3 Register

1 CSCTI_CFG_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-28130. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFECh**

Figure 14-9282. CSCTI_CFG_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28132. CSCTI_CFG_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.11.1.2.742 CSCTI_CFG_COMPID0 Register

1 CSCTI_CFG_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-28133. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF0h**

Figure 14-9283. CSCTI_CFG_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-28135. CSCTI_CFG_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.11.1.2.743 CSCTI_CFG_COMPID1 Register

1 CSCTI_CFG_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-28136. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF4h**

Figure 14-9284. CSCTI_CFG_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-28138. CSCTI_CFG_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.11.1.2.744 CSCTI_CFG_COMPID2 Register

1 CSCTI_CFG_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-28139. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFF8h**

Figure 14-9285. CSCTI_CFG_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-28141. CSCTI_CFG_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.11.1.2.745 CSCTI_CFG_COMPID3 Register

1 CSCTI_CFG_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-28142. Instance Table

Instance Name	Physical Address
DEBUGSS0	**0007 3C02 FFFCh**

Figure 14-9286. CSCTI_CFG_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-28144. CSCTI_CFG_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.11.2 DEBUGSS_WRAP Registers

14.11.2.1 DEBUGSS_WRAP Summary Table

Table 14-28145. DEBUGSS_WRAP0_ROM_TABLE_0_0 Registers, Base Address=0007 00000000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	ROM_TABLE_0_0_ROM_ENTRY0	7000 00000h
4h	32	ROM_TABLE_0_0_ROM_ENTRY1	7000 00004h
8h	32	ROM_TABLE_0_0_ROM_ENTRY2	7000 00008h
8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY0	7000 00008h
Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY1	7000 0000Ch
10h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY2	7000 00010h
14h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY3	7000 00014h
18h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY4	7000 00018h
1Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY5	7000 0001Ch
20h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY6	7000 00020h
24h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY7	7000 00024h
28h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY8	7000 00028h
2Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY9	7000 0002Ch
30h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY10	7000 00030h
34h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY11	7000 00034h
38h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY12	7000 00038h
3Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY13	7000 0003Ch
40h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY14	7000 00040h
44h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY15	7000 00044h
48h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY16	7000 00048h
4Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY17	7000 0004Ch
50h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY18	7000 00050h
54h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY19	7000 00054h
58h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY20	7000 00058h
5Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY21	7000 0005Ch
60h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY22	7000 00060h
64h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY23	7000 00064h
68h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY24	7000 00068h
6Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY25	7000 0006Ch
70h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY26	7000 00070h
74h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY27	7000 00074h
78h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY28	7000 00078h
7Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY29	7000 0007Ch
80h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY30	7000 00080h
84h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY31	7000 00084h
88h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY32	7000 00088h
8Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY33	7000 0008Ch
90h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY34	7000 00090h
94h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY35	7000 00094h
98h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY36	7000 00098h

Table 14-28145. DEBUGSS_WRAP0_ROM_TABLE_0_0 Registers, Base Address=0007 00000000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
9Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY37	7000 0009Ch
A0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY38	7000 000A0h
A4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY39	7000 000A4h
A8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY40	7000 000A8h
ACh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY41	7000 000ACh
B0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY42	7000 000B0h
B4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY43	7000 000B4h
B8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY44	7000 000B8h
BCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY45	7000 000BCh
C0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY46	7000 000C0h
C4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY47	7000 000C4h
C8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY48	7000 000C8h
CCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY49	7000 000CCh
D0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY50	7000 000D0h
D4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY51	7000 000D4h
D8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY52	7000 000D8h
DCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY53	7000 000DCh
E0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY54	7000 000E0h
E4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY55	7000 000E4h
E8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY56	7000 000E8h
ECh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY57	7000 000ECh
F0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY58	7000 000F0h
F4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY59	7000 000F4h
F8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY60	7000 000F8h
FCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY61	7000 000FCh
100h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY62	7000 00100h
104h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY63	7000 00104h
108h	32	ROM_TABLE_0_0_PERIPHID0	7000 00108h
10Ch	32	ROM_TABLE_0_0_PERIPHID1	7000 0010Ch
110h	32	ROM_TABLE_0_0_PERIPHID2	7000 00110h
114h	32	ROM_TABLE_0_0_PERIPHID3	7000 00114h
118h	32	ROM_TABLE_0_0_PERIPHID4	7000 00118h
3FCh	32	ROM_TABLE_0_0_COMPID0	7000 003FCh
3FCh	32	ROM_TABLE_0_0_COMPID1	7000 003FCh
3FCh	32	ROM_TABLE_0_0_COMPID2	7000 003FCh
3FCh	32	ROM_TABLE_0_0_COMPID3	7000 003FCh

Table 14-28146. DEBUGSS_WRAP0_cfgap_cfg_0 Registers, Base Address=0007 00002000h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CFGAP_CFG_0_JTAGID_REG	7000 02000h
4h	32	CFGAP_CFG_0_USERID_REG	7000 02004h
8h	32	CFGAP_CFG_0_VERSION_REG	7000 02008h
Ch	32	CFGAP_CFG_0_SYSTEMSTATUS	7000 0200Ch

Table 14-28146. DEBUGSS_WRAP0_cfgap_cfg_0 Registers, Base Address=0007 00002000h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
FCh	32	CFGAP_CFG_0_APID_REGISTER	7000 020FCh

Table 14-28147. DEBUGSS_WRAP0_apbap_cfg_0 Registers, Base Address=0007 00002100h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	APBAP_CFG_0_CSWREG	7000 02100h
4h	32	APBAP_CFG_0_TAREG	7000 02104h
Ch	32	APBAP_CFG_0_DRWREG	7000 0210Ch
10h	32	APBAP_CFG_0_BD0REG	7000 02110h
14h	32	APBAP_CFG_0_BD1REG	7000 02114h
18h	32	APBAP_CFG_0_BD2REG	7000 02118h
1Ch	32	APBAP_CFG_0_BD3REG	7000 0211Ch
F8h	32	APBAP_CFG_0_ROM_REGISTER	7000 021F8h
FCh	32	APBAP_CFG_0_ID_REGISTER	7000 021FCh

Table 14-28148. DEBUGSS_WRAP0_axiap_cfg_0 Registers, Base Address=0007 00002200h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	AXIAP_CFG_0_CSWREG	7000 02200h
4h	32	AXIAP_CFG_0_TAREGL	7000 02204h
8h	32	AXIAP_CFG_0_TAREGH	7000 02208h
Ch	32	AXIAP_CFG_0_DRWREG	7000 0220Ch
10h	32	AXIAP_CFG_0_BD0REG	7000 02210h
14h	32	AXIAP_CFG_0_BD1REG	7000 02214h
18h	32	AXIAP_CFG_0_BD2REG	7000 02218h
1Ch	32	AXIAP_CFG_0_BD3REG	7000 0221Ch
20h	32	AXIAP_CFG_0_MBT_REGISTER	7000 02220h
F0h	32	AXIAP_CFG_0_ROM_HI_REGISTER	7000 022F0h
F4h	32	AXIAP_CFG_0_CFG_REGISTER	7000 022F4h
F8h	32	AXIAP_CFG_0_ROM_LO_REGISTER	7000 022F8h
FCh	32	AXIAP_CFG_0_ID_REGISTER	7000 022FCh

Table 14-28149. DEBUGSS_WRAP0_pwrap_cfg_0 Registers, Base Address=0007 00002300h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	PWRAP_CFG_0_CORE_PRECREG0	7000 02300h
4h	32	PWRAP_CFG_0_CORE_PRECREG1	7000 02304h
8h	32	PWRAP_CFG_0_CORE_PRECREG2	7000 02308h
Ch	32	PWRAP_CFG_0_CORE_PRECREG3	7000 0230Ch
10h	32	PWRAP_CFG_0_CORE_PRECREG4	7000 02310h
14h	32	PWRAP_CFG_0_CORE_PRECREG5	7000 02314h
18h	32	PWRAP_CFG_0_CORE_PRECREG6	7000 02318h
1Ch	32	PWRAP_CFG_0_CORE_PRECREG7	7000 0231Ch
20h	32	PWRAP_CFG_0_CORE_PRECREG8	7000 02320h
24h	32	PWRAP_CFG_0_CORE_PRECREG9	7000 02324h
28h	32	PWRAP_CFG_0_CORE_PRECREG10	7000 02328h

Table 14-28149. DEBUGSS_WRAP0_pwrap_cfg_0 Registers, Base Address=0007 00002300h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
2Ch	32	PWRAP_CFG_0_CORE_PRECREG11	7000 0232Ch
30h	32	PWRAP_CFG_0_CORE_PRECREG12	7000 02330h
34h	32	PWRAP_CFG_0_CORE_PRECREG13	7000 02334h
38h	32	PWRAP_CFG_0_CORE_PRECREG14	7000 02338h
3Ch	32	PWRAP_CFG_0_CORE_PRECREG15	7000 0233Ch
40h	32	PWRAP_CFG_0_CORE_PRECREG16	7000 02340h
44h	32	PWRAP_CFG_0_CORE_PRECREG17	7000 02344h
48h	32	PWRAP_CFG_0_CORE_PRECREG18	7000 02348h
4Ch	32	PWRAP_CFG_0_CORE_PRECREG19	7000 0234Ch
50h	32	PWRAP_CFG_0_CORE_PRECREG20	7000 02350h
54h	32	PWRAP_CFG_0_CORE_PRECREG21	7000 02354h
58h	32	PWRAP_CFG_0_CORE_PRECREG22	7000 02358h
5Ch	32	PWRAP_CFG_0_CORE_PRECREG23	7000 0235Ch
60h	32	PWRAP_CFG_0_CORE_PRECREG24	7000 02360h
64h	32	PWRAP_CFG_0_CORE_PRECREG25	7000 02364h
68h	32	PWRAP_CFG_0_CORE_PRECREG26	7000 02368h
6Ch	32	PWRAP_CFG_0_CORE_PRECREG27	7000 0236Ch
70h	32	PWRAP_CFG_0_CORE_PRECREG28	7000 02370h
74h	32	PWRAP_CFG_0_CORE_PRECREG29	7000 02374h
78h	32	PWRAP_CFG_0_CORE_PRECREG30	7000 02378h
7Ch	32	PWRAP_CFG_0_CORE_PRECREG31	7000 0237Ch
F0h	32	PWRAP_CFG_0_SYS_PRECREG	7000 023F0h
FCh	32	PWRAP_CFG_0_ID_REGISTER	7000 023FCh

Table 14-28150. DEBUGSS_WRAP0_pview_cfg_0 Registers, Base Address=0007 00002400h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	PVIEW_CFG_0_PVIEW_STATE0	7000 02400h
F0h	32	PVIEW_CFG_0_PVIEW_CAPABILITY	7000 024F0h
FCh	32	PVIEW_CFG_0_ID_REGISTER	7000 024FCh

Table 14-28151. DEBUGSS_WRAP0_jtagap_cfg_0 Registers, Base Address=0007 00002500h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	JTAGAP_CFG_0_CSW	7000 02500h
4h	32	JTAGAP_CFG_0_PSEL_REG	7000 02504h
8h	32	JTAGAP_CFG_0_PSTA_REG	7000 02508h
10h	32	JTAGAP_CFG_0_BYTEFIFO1	7000 02510h
14h	32	JTAGAP_CFG_0_BYTEFIFO2	7000 02514h
18h	32	JTAGAP_CFG_0_BYTEFIFO3	7000 02518h
1Ch	32	JTAGAP_CFG_0_BYTEFIFO4	7000 0251Ch
FCh	32	JTAGAP_CFG_0_ID_REGISTER	7000 025FCh

Table 14-28152. DEBUGSS_WRAP0_secap_cfg_0 Registers, Base Address=0007 00002600h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	SECAP_CFG_0_TXDATA	7000 02600h
4h	32	SECAP_CFG_0_TXCTRL	7000 02604h
8h	32	SECAP_CFG_0_RXDATA	7000 02608h
Ch	32	SECAP_CFG_0_RXCTRL	7000 0260Ch

Table 14-28153. DEBUGSS_WRAP0_cortex0_cfg_0 Registers, Base Address=0007 00002700h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX0_CFG_0_CSWREG	7000 02700h
4h	32	CORTEX0_CFG_0_TAREG	7000 02704h
Ch	32	CORTEX0_CFG_0_DRWREG	7000 0270Ch
10h	32	CORTEX0_CFG_0_BD0REG	7000 02710h
14h	32	CORTEX0_CFG_0_BD1REG	7000 02714h
18h	32	CORTEX0_CFG_0_BD2REG	7000 02718h
1Ch	32	CORTEX0_CFG_0_BD3REG	7000 0271Ch
F8h	32	CORTEX0_CFG_0_ROM_REGISTER	7000 027F8h
FCh	32	CORTEX0_CFG_0_ID_REGISTER	7000 027FCh

Table 14-28154. DEBUGSS_WRAP0_cortex1_cfg_0 Registers, Base Address=0007 00002800h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX1_CFG_0_CSWREG	7000 02800h
4h	32	CORTEX1_CFG_0_TAREG	7000 02804h
Ch	32	CORTEX1_CFG_0_DRWREG	7000 0280Ch
10h	32	CORTEX1_CFG_0_BD0REG	7000 02810h
14h	32	CORTEX1_CFG_0_BD1REG	7000 02814h
18h	32	CORTEX1_CFG_0_BD2REG	7000 02818h
1Ch	32	CORTEX1_CFG_0_BD3REG	7000 0281Ch
F8h	32	CORTEX1_CFG_0_ROM_REGISTER	7000 028F8h
FCh	32	CORTEX1_CFG_0_ID_REGISTER	7000 028FCh

Table 14-28155. DEBUGSS_WRAP0_cortex2_cfg_0 Registers, Base Address=0007 00002900h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX2_CFG_0_CSWREG	7000 02900h
4h	32	CORTEX2_CFG_0_TAREG	7000 02904h
Ch	32	CORTEX2_CFG_0_DRWREG	7000 0290Ch
10h	32	CORTEX2_CFG_0_BD0REG	7000 02910h
14h	32	CORTEX2_CFG_0_BD1REG	7000 02914h
18h	32	CORTEX2_CFG_0_BD2REG	7000 02918h
1Ch	32	CORTEX2_CFG_0_BD3REG	7000 0291Ch
F8h	32	CORTEX2_CFG_0_ROM_REGISTER	7000 029F8h
FCh	32	CORTEX2_CFG_0_ID_REGISTER	7000 029FCh

Table 14-28156. DEBUGSS_WRAP0_cortex3_cfg_0 Registers, Base Address=0007 00002A00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX3_CFG_0_CSWREG	7000 02A00h
4h	32	CORTEX3_CFG_0_TAREG	7000 02A04h
Ch	32	CORTEX3_CFG_0_DRWREG	7000 02A0Ch
10h	32	CORTEX3_CFG_0_BD0REG	7000 02A10h
14h	32	CORTEX3_CFG_0_BD1REG	7000 02A14h
18h	32	CORTEX3_CFG_0_BD2REG	7000 02A18h
1Ch	32	CORTEX3_CFG_0_BD3REG	7000 02A1Ch
F8h	32	CORTEX3_CFG_0_ROM_REGISTER	7000 02AF8h
FCh	32	CORTEX3_CFG_0_ID_REGISTER	7000 02AFCh

Table 14-28157. DEBUGSS_WRAP0_cortex4_cfg_0 Registers, Base Address=0007 00002B00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX4_CFG_0_CSWREG	7000 02B00h
4h	32	CORTEX4_CFG_0_TAREG	7000 02B04h
Ch	32	CORTEX4_CFG_0_DRWREG	7000 02B0Ch
10h	32	CORTEX4_CFG_0_BD0REG	7000 02B10h
14h	32	CORTEX4_CFG_0_BD1REG	7000 02B14h
18h	32	CORTEX4_CFG_0_BD2REG	7000 02B18h
1Ch	32	CORTEX4_CFG_0_BD3REG	7000 02B1Ch
F8h	32	CORTEX4_CFG_0_ROM_REGISTER	7000 02BF8h
FCh	32	CORTEX4_CFG_0_ID_REGISTER	7000 02BFCh

Table 14-28158. DEBUGSS_WRAP0_cortex5_cfg_0 Registers, Base Address=0007 00002C00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX5_CFG_0_CSWREG	7000 02C00h
4h	32	CORTEX5_CFG_0_TAREG	7000 02C04h
Ch	32	CORTEX5_CFG_0_DRWREG	7000 02C0Ch
10h	32	CORTEX5_CFG_0_BD0REG	7000 02C10h
14h	32	CORTEX5_CFG_0_BD1REG	7000 02C14h
18h	32	CORTEX5_CFG_0_BD2REG	7000 02C18h
1Ch	32	CORTEX5_CFG_0_BD3REG	7000 02C1Ch
F8h	32	CORTEX5_CFG_0_ROM_REGISTER	7000 02CF8h
FCh	32	CORTEX5_CFG_0_ID_REGISTER	7000 02CFCh

Table 14-28159. DEBUGSS_WRAP0_cortex6_cfg_0 Registers, Base Address=0007 00002D00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX6_CFG_0_CSWREG	7000 02D00h
4h	32	CORTEX6_CFG_0_TAREG	7000 02D04h
Ch	32	CORTEX6_CFG_0_DRWREG	7000 02D0Ch
10h	32	CORTEX6_CFG_0_BD0REG	7000 02D10h

Table 14-28159. DEBUGSS_WRAP0_cortex6_cfg_0 Registers, Base Address=0007 00002D00h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
14h	32	CORTEX6_CFG_0_BD1REG	7000 02D14h
18h	32	CORTEX6_CFG_0_BD2REG	7000 02D18h
1Ch	32	CORTEX6_CFG_0_BD3REG	7000 02D1Ch
F8h	32	CORTEX6_CFG_0_ROM_REGISTER	7000 02DF8h
FCh	32	CORTEX6_CFG_0_ID_REGISTER	7000 02DFCh

Table 14-28160. DEBUGSS_WRAP0_cortex7_cfg_0 Registers, Base Address=0007 00002E00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX7_CFG_0_CSWREG	7000 02E00h
4h	32	CORTEX7_CFG_0_TAREG	7000 02E04h
Ch	32	CORTEX7_CFG_0_DRWREG	7000 02E0Ch
10h	32	CORTEX7_CFG_0_BD0REG	7000 02E10h
14h	32	CORTEX7_CFG_0_BD1REG	7000 02E14h
18h	32	CORTEX7_CFG_0_BD2REG	7000 02E18h
1Ch	32	CORTEX7_CFG_0_BD3REG	7000 02E1Ch
F8h	32	CORTEX7_CFG_0_ROM_REGISTER	7000 02EF8h
FCh	32	CORTEX7_CFG_0_ID_REGISTER	7000 02EFCh

Table 14-28161. DEBUGSS_WRAP0_cortex8_cfg_0 Registers, Base Address=0007 00002F00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX8_CFG_0_CSWREG	7000 02F00h
4h	32	CORTEX8_CFG_0_TAREG	7000 02F04h
Ch	32	CORTEX8_CFG_0_DRWREG	7000 02F0Ch
10h	32	CORTEX8_CFG_0_BD0REG	7000 02F10h
14h	32	CORTEX8_CFG_0_BD1REG	7000 02F14h
18h	32	CORTEX8_CFG_0_BD2REG	7000 02F18h
1Ch	32	CORTEX8_CFG_0_BD3REG	7000 02F1Ch
F8h	32	CORTEX8_CFG_0_ROM_REGISTER	7000 02FF8h
FCh	32	CORTEX8_CFG_0_ID_REGISTER	7000 02FFCh

Table 14-28162. DEBUGSS_WRAP0_ROM_TABLE_1_0 Registers, Base Address=0007 20000000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	ROM_TABLE_1_0_ROM_ENTRY0	7200 00000h
4h	32	ROM_TABLE_1_0_ROM_ENTRY1	7200 00004h
8h	32	ROM_TABLE_1_0_ROM_ENTRY2	7200 00008h
Ch	32	ROM_TABLE_1_0_ROM_ENTRY3	7200 0000Ch
10h	32	ROM_TABLE_1_0_ROM_ENTRY4	7200 00010h
14h	32	ROM_TABLE_1_0_ROM_ENTRY5	7200 00014h
18h	32	ROM_TABLE_1_0_COMPUTE_CLUSTER0	7200 00018h
1Ch	32	ROM_TABLE_1_0_COMPUTE_CLUSTER1	7200 0001Ch

Table 14-28162. DEBUGSS_WRAP0_ROM_TABLE_1_0 Registers, Base Address=0007 20000000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
20h	32	ROM_TABLE_1_0_COMPUTE_CLUSTER2	7200 00020h
24h	32	ROM_TABLE_1_0_DEBUG_CELL0	7200 00024h
28h	32	ROM_TABLE_1_0_DEBUG_CELL1	7200 00028h
2Ch	32	ROM_TABLE_1_0_DEBUG_CELL2	7200 0002Ch
30h	32	ROM_TABLE_1_0_DEBUG_CELL3	7200 00030h
34h	32	ROM_TABLE_1_0_DEBUG_CELL4	7200 00034h
38h	32	ROM_TABLE_1_0_DEBUG_CELL5	7200 00038h
3Ch	32	ROM_TABLE_1_0_DEBUG_CELL6	7200 0003Ch
40h	32	ROM_TABLE_1_0_DEBUG_CELL7	7200 00040h
44h	32	ROM_TABLE_1_0_DEBUG_CELL8	7200 00044h
48h	32	ROM_TABLE_1_0_DEBUG_CELL9	7200 00048h
4Ch	32	ROM_TABLE_1_0_DEBUG_CELL10	7200 0004Ch
50h	32	ROM_TABLE_1_0_DEBUG_CELL11	7200 00050h
50h	32	ROM_TABLE_1_0_EXTCSCOMP0	7200 00050h
54h	32	ROM_TABLE_1_0_EXTCSCOMP1	7200 00054h
58h	32	ROM_TABLE_1_0_EXTCSCOMP2	7200 00058h
5Ch	32	ROM_TABLE_1_0_EXTCSCOMP3	7200 0005Ch
60h	32	ROM_TABLE_1_0_EXTCSCOMP4	7200 00060h
64h	32	ROM_TABLE_1_0_EXTCSCOMP5	7200 00064h
68h	32	ROM_TABLE_1_0_EXTCSCOMP6	7200 00068h
6Ch	32	ROM_TABLE_1_0_EXTCSCOMP7	7200 0006Ch
70h	32	ROM_TABLE_1_0_EXTCSCOMP8	7200 00070h
74h	32	ROM_TABLE_1_0_EXTCSCOMP9	7200 00074h
78h	32	ROM_TABLE_1_0_EXTCSCOMP10	7200 00078h
7Ch	32	ROM_TABLE_1_0_EXTCSCOMP11	7200 0007Ch

Table 14-28163. DEBUGSS_WRAP0_cscti Registers, Base Address=0007 60001000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CSCTI_CTICONTROL	7600 01000h
10h	32	CSCTI_CTIINTACK	7600 01010h
14h	32	CSCTI_CTIAPPSET	7600 01014h
18h	32	CSCTI_CTIAPPCLR	7600 01018h
1Ch	32	CSCTI_CTIAPPPULSE	7600 0101Ch
20h	32	CSCTI_CTIINEN0	7600 01020h
24h	32	CSCTI_CTIINEN1	7600 01024h
28h	32	CSCTI_CTIINEN2	7600 01028h
2Ch	32	CSCTI_CTIINEN3	7600 0102Ch
30h	32	CSCTI_CTIINEN4	7600 01030h
34h	32	CSCTI_CTIINEN5	7600 01034h
38h	32	CSCTI_CTIINEN6	7600 01038h
3Ch	32	CSCTI_CTIINEN7	7600 0103Ch
A0h	32	CSCTI_CTIOUTEN0	7600 010A0h
A4h	32	CSCTI_CTIOUTEN1	7600 010A4h

Table 14-28163. DEBUGSS_WRAP0_cscti Registers, Base Address=0007 60001000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
A8h	32	CSCTI_CTIOUTEN2	7600 010A8h
ACh	32	CSCTI_CTIOUTEN3	7600 010ACh
B0h	32	CSCTI_CTIOUTEN4	7600 010B0h
B4h	32	CSCTI_CTIOUTEN5	7600 010B4h
B8h	32	CSCTI_CTIOUTEN6	7600 010B8h
BCh	32	CSCTI_CTIOUTEN7	7600 010BCh
130h	32	CSCTI_CTITRIGINSTATUS	7600 01130h
134h	32	CSCTI_CTITRIGOUTSTATUS	7600 01134h
138h	32	CSCTI_CTICHINSTATUS	7600 01138h
13Ch	32	CSCTI_CTICHOUTSTATUS	7600 0113Ch
140h	32	CSCTI_CTIGATE	7600 01140h
144h	32	CSCTI_ASICCTL	7600 01144h
EDCh	32	CSCTI_ITCHINACK	7600 01EDCh
EE0h	32	CSCTI_ITTRIGINACK	7600 01EE0h
EE4h	32	CSCTI_ITCHOUT	7600 01EE4h
EE8h	32	CSCTI_ITTRIGOUT	7600 01EE8h
EECh	32	CSCTI_ITCHOUTACK	7600 01EECh
EF0h	32	CSCTI_ITTRIGOUTACK	7600 01EF0h
EF4h	32	CSCTI_ITCHIN	7600 01EF4h
EF8h	32	CSCTI_ITTRIGIN	7600 01EF8h
F00h	32	CSCTI_ITCTRL	7600 01F00h
FA0h	32	CSCTI_CLAIMSET	7600 01FA0h
FA4h	32	CSCTI_CLAIMCLR	7600 01FA4h
FB0h	32	CSCTI_LOCKACCESS	7600 01FB0h
FB4h	32	CSCTI_LOCKSTATUS	7600 01FB4h
FB8h	32	CSCTI_AUTHSTATUS	7600 01FB8h
FC8h	32	CSCTI_DEVID	7600 01FC8h
FCCh	32	CSCTI_DEVTYPE	7600 01FCCh
FD0h	32	CSCTI_PERIPHID4	7600 01FD0h
FE0h	32	CSCTI_PERIPHID0	7600 01FE0h
FE4h	32	CSCTI_PERIPHID1	7600 01FE4h
FE8h	32	CSCTI_PERIPHID2	7600 01FE8h
FECh	32	CSCTI_PERIPHID3	7600 01FECh
FF0h	32	CSCTI_COMPONID0	7600 01FF0h
FF4h	32	CSCTI_COMPONID1	7600 01FF4h
FF8h	32	CSCTI_COMPONID2	7600 01FF8h
FFCh	32	CSCTI_COMPONID3	7600 01FFCh

Table 14-28164. DEBUGSS_WRAP0_drm_cfg_0 Registers, Base Address=0007 20002000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	DRM_CFG_0_PERIPH_ID	7200 02000h
4h	32	DRM_CFG_0_VERSION	7200 02004h
8h	32	DRM_CFG_0_CAPABILITY	7200 02008h

Table 14-28164. DEBUGSS_WRAP0_drm_cfg_0 Registers, Base Address=0007 20002000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
Ch	32	DRM_CFG_0_TRACE_CTRL	7200 0200Ch
10h	32	DRM_CFG_0_VBUSM_CTRL	7200 02010h
14h	32	DRM_CFG_0_DAP_TIMEOUT	7200 02014h
18h	32	DRM_CFG_0_CONFIG	7200 02018h
1Ch	32	DRM_CFG_0_EMUTRIGEN	7200 0201Ch
20h	32	DRM_CFG_0_BINVALLO	7200 02020h
24h	32	DRM_CFG_0_BINVALHI	7200 02024h
200h	32	DRM_CFG_0_SUSPEND_REG0	7200 02200h
204h	32	DRM_CFG_0_SUSPEND_REG1	7200 02204h
208h	32	DRM_CFG_0_SUSPEND_REG2	7200 02208h
20Ch	32	DRM_CFG_0_SUSPEND_REG3	7200 0220Ch
210h	32	DRM_CFG_0_SUSPEND_REG4	7200 02210h
214h	32	DRM_CFG_0_SUSPEND_REG5	7200 02214h
218h	32	DRM_CFG_0_SUSPEND_REG6	7200 02218h
21Ch	32	DRM_CFG_0_SUSPEND_REG7	7200 0221Ch
220h	32	DRM_CFG_0_SUSPEND_REG8	7200 02220h
224h	32	DRM_CFG_0_SUSPEND_REG9	7200 02224h
228h	32	DRM_CFG_0_SUSPEND_REG10	7200 02228h
22Ch	32	DRM_CFG_0_SUSPEND_REG11	7200 0222Ch
230h	32	DRM_CFG_0_SUSPEND_REG12	7200 02230h
234h	32	DRM_CFG_0_SUSPEND_REG13	7200 02234h
238h	32	DRM_CFG_0_SUSPEND_REG14	7200 02238h
23Ch	32	DRM_CFG_0_SUSPEND_REG15	7200 0223Ch
240h	32	DRM_CFG_0_SUSPEND_REG16	7200 02240h
244h	32	DRM_CFG_0_SUSPEND_REG17	7200 02244h
248h	32	DRM_CFG_0_SUSPEND_REG18	7200 02248h
24Ch	32	DRM_CFG_0_SUSPEND_REG19	7200 0224Ch
250h	32	DRM_CFG_0_SUSPEND_REG20	7200 02250h
254h	32	DRM_CFG_0_SUSPEND_REG21	7200 02254h
258h	32	DRM_CFG_0_SUSPEND_REG22	7200 02258h
25Ch	32	DRM_CFG_0_SUSPEND_REG23	7200 0225Ch
260h	32	DRM_CFG_0_SUSPEND_REG24	7200 02260h
264h	32	DRM_CFG_0_SUSPEND_REG25	7200 02264h
268h	32	DRM_CFG_0_SUSPEND_REG26	7200 02268h
26Ch	32	DRM_CFG_0_SUSPEND_REG27	7200 0226Ch
270h	32	DRM_CFG_0_SUSPEND_REG28	7200 02270h
274h	32	DRM_CFG_0_SUSPEND_REG29	7200 02274h
278h	32	DRM_CFG_0_SUSPEND_REG30	7200 02278h
27Ch	32	DRM_CFG_0_SUSPEND_REG31	7200 0227Ch

Table 14-28165. DEBUGSS_WRAP0_cstpiu_cfg_0 Registers, Base Address=0007 20004000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CSTPIU_CFG_0_SUPPORTSIZE	7200 04000h
4h	32	CSTPIU_CFG_0_CURPORTSIZE	7200 04004h
100h	32	CSTPIU_CFG_0_TRIGMODEREG	7200 04100h
104h	32	CSTPIU_CFG_0_TRIGCTRREG	7200 04104h
108h	32	CSTPIU_CFG_0_TRIGMPYREG	7200 04108h
200h	32	CSTPIU_CFG_0_SUPTESTPAT	7200 04200h
204h	32	CSTPIU_CFG_0_CURTESTPAT	7200 04204h
208h	32	CSTPIU_CFG_0_TESTPATCNT	7200 04208h
300h	32	CSTPIU_CFG_0_FORMFLUSHSTAT	7200 04300h
304h	32	CSTPIU_CFG_0_FORMFLUSHCTL	7200 04304h
308h	32	CSTPIU_CFG_0_FORMSYNCCTR	7200 04308h
400h	32	CSTPIU_CFG_0_EXTCTLIN	7200 04400h
404h	32	CSTPIU_CFG_0_EXTCTLOUT	7200 04404h
EE4h	32	CSTPIU_CFG_0_ITTRFLINACK	7200 04EE4h
EE8h	32	CSTPIU_CFG_0_ITTRFLIN	7200 04EE8h
EECh	32	CSTPIU_CFG_0_ITATBDATA0	7200 04EECh
EF0h	32	CSTPIU_CFG_0_ITATBCTR2	7200 04EF0h
EF4h	32	CSTPIU_CFG_0_ITATBCTR1	7200 04EF4h
EF8h	32	CSTPIU_CFG_0_ITATBCTR0	7200 04EF8h
F00h	32	CSTPIU_CFG_0_INTCTRL	7200 04F00h
FA0h	32	CSTPIU_CFG_0_CTSET	7200 04FA0h
FA4h	32	CSTPIU_CFG_0_CTCLR	7200 04FA4h
FB0h	32	CSTPIU_CFG_0_LAREG	7200 04FB0h
FB4h	32	CSTPIU_CFG_0_LSREG	7200 04FB4h
FB8h	32	CSTPIU_CFG_0_AUTHST	7200 04FB8h
FC8h	32	CSTPIU_CFG_0_DEVID	7200 04FC8h
FCCh	32	CSTPIU_CFG_0_DEVTYPEID	7200 04FCCh
FD0h	32	CSTPIU_CFG_0_PERID4	7200 04FD0h
FE0h	32	CSTPIU_CFG_0_PERID0	7200 04FE0h
FE4h	32	CSTPIU_CFG_0_PERID1	7200 04FE4h
FE8h	32	CSTPIU_CFG_0_PERID2	7200 04FE8h
FECh	32	CSTPIU_CFG_0_PERID3	7200 04FECh
FF0h	32	CSTPIU_CFG_0_COMPID0	7200 04FF0h
FF4h	32	CSTPIU_CFG_0_COMPID1	7200 04FF4h
FF8h	32	CSTPIU_CFG_0_COMPID2	7200 04FF8h
FFCh	32	CSTPIU_CFG_0_COMPID3	7200 04FFCh

Table 14-28166. DEBUGSS_WRAP0_ctf_cfg_0 Registers, Base Address=0007 20005000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CTF_CFG_0_CSTFCTLREG	7200 05000h
4h	32	CTF_CFG_0_PRIORCTLREG	7200 05004h
EECh	32	CTF_CFG_0_ITATBDATA0	7200 05EECh
EF0h	32	CTF_CFG_0_ITATBCTR2	7200 05EF0h

Table 14-28166. DEBUGSS_WRAP0_ctf_cfg_0 Registers, Base Address=0007 20005000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
EF4h	32	CTF_CFG_0_ITATBCTR1	7200 05EF4h
EF8h	32	CTF_CFG_0_ITATBCTR0	7200 05EF8h
F00h	32	CTF_CFG_0_INTCTRL	7200 05F00h
FA0h	32	CTF_CFG_0_CTSET	7200 05FA0h
FA4h	32	CTF_CFG_0_CTCLR	7200 05FA4h
FB0h	32	CTF_CFG_0_LAREG	7200 05FB0h
FB4h	32	CTF_CFG_0_LSREG	7200 05FB4h
FB8h	32	CTF_CFG_0_AUTHST	7200 05FB8h
FC8h	32	CTF_CFG_0_DEVID	7200 05FC8h
FCCh	32	CTF_CFG_0_DEVTYPEID	7200 05FCCh
FD0h	32	CTF_CFG_0_PERID4	7200 05FD0h
FD4h	32	CTF_CFG_0_PERID5	7200 05FD4h
FD8h	32	CTF_CFG_0_PERID6	7200 05FD8h
FDCh	32	CTF_CFG_0_PERID7	7200 05FDCh
FE0h	32	CTF_CFG_0_PERID0	7200 05FE0h
FE4h	32	CTF_CFG_0_PERID1	7200 05FE4h
FE8h	32	CTF_CFG_0_PERID2	7200 05FE8h
FECh	32	CTF_CFG_0_PERID3	7200 05FECh
FF0h	32	CTF_CFG_0_COMPID0	7200 05FF0h
FF4h	32	CTF_CFG_0_COMPID1	7200 05FF4h
FF8h	32	CTF_CFG_0_COMPID2	7200 05FF8h
FFCh	32	CTF_CFG_0_COMPID3	7200 05FFCh

Table 14-28167. DEBUGSS_WRAP0_ROM_TABLE_0_1 Registers, Base Address=0007 40000000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	ROM_TABLE_0_1_ROM_ENTRY0	7400 00000h
4h	32	ROM_TABLE_0_1_ROM_ENTRY1	7400 00004h
8h	32	ROM_TABLE_0_1_ROM_ENTRY2	7400 00008h
8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY0	7400 00008h
Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY1	7400 0000Ch
10h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY2	7400 00010h
14h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY3	7400 00014h
18h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY4	7400 00018h
1Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY5	7400 0001Ch
20h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY6	7400 00020h
24h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY7	7400 00024h
28h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY8	7400 00028h
2Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY9	7400 0002Ch
30h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY10	7400 00030h
34h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY11	7400 00034h
38h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY12	7400 00038h
3Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY13	7400 0003Ch

Table 14-28167. DEBUGSS_WRAP0_ROM_TABLE_0_1 Registers, Base Address=0007 40000000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
40h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY14	7400 00040h
44h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY15	7400 00044h
48h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY16	7400 00048h
4Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY17	7400 0004Ch
50h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY18	7400 00050h
54h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY19	7400 00054h
58h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY20	7400 00058h
5Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY21	7400 0005Ch
60h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY22	7400 00060h
64h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY23	7400 00064h
68h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY24	7400 00068h
6Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY25	7400 0006Ch
70h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY26	7400 00070h
74h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY27	7400 00074h
78h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY28	7400 00078h
7Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY29	7400 0007Ch
80h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY30	7400 00080h
84h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY31	7400 00084h
88h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY32	7400 00088h
8Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY33	7400 0008Ch
90h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY34	7400 00090h
94h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY35	7400 00094h
98h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY36	7400 00098h
9Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY37	7400 0009Ch
A0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY38	7400 000A0h
A4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY39	7400 000A4h
A8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY40	7400 000A8h
ACh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY41	7400 000ACh
B0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY42	7400 000B0h
B4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY43	7400 000B4h
B8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY44	7400 000B8h
BCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY45	7400 000BCh
C0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY46	7400 000C0h
C4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY47	7400 000C4h
C8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY48	7400 000C8h
CCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY49	7400 000CCh
D0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY50	7400 000D0h
D4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY51	7400 000D4h
D8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY52	7400 000D8h
DCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY53	7400 000DCh
E0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY54	7400 000E0h
E4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY55	7400 000E4h
E8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY56	7400 000E8h

Table 14-28167. DEBUGSS_WRAP0_ROM_TABLE_0_1 Registers, Base Address=0007 40000000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
ECh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY57	7400 000ECh
F0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY58	7400 000F0h
F4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY59	7400 000F4h
F8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY60	7400 000F8h
FCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY61	7400 000FCh
100h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY62	7400 00100h
104h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY63	7400 00104h
108h	32	ROM_TABLE_0_1_PERIPHID0	7400 00108h
10Ch	32	ROM_TABLE_0_1_PERIPHID1	7400 0010Ch
110h	32	ROM_TABLE_0_1_PERIPHID2	7400 00110h
114h	32	ROM_TABLE_0_1_PERIPHID3	7400 00114h
118h	32	ROM_TABLE_0_1_PERIPHID4	7400 00118h
3FCh	32	ROM_TABLE_0_1_COMPID0	7400 003FCh
3FCh	32	ROM_TABLE_0_1_COMPID1	7400 003FCh
3FCh	32	ROM_TABLE_0_1_COMPID2	7400 003FCh
3FCh	32	ROM_TABLE_0_1_COMPID3	7400 003FCh

Table 14-28168. DEBUGSS_WRAP0_cfgap_cfg_1 Registers, Base Address=0007 40002000h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CFGAP_CFG_1_JTAGID_REG	7400 02000h
4h	32	CFGAP_CFG_1_USERID_REG	7400 02004h
8h	32	CFGAP_CFG_1_VERSION_REG	7400 02008h
Ch	32	CFGAP_CFG_1_SYSTEMSTATUS	7400 0200Ch
FCh	32	CFGAP_CFG_1_APID_REGISTER	7400 020FCh

Table 14-28169. DEBUGSS_WRAP0_apbap_cfg_1 Registers, Base Address=0007 40002100h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	APBAP_CFG_1_CSWREG	7400 02100h
4h	32	APBAP_CFG_1_TAREG	7400 02104h
Ch	32	APBAP_CFG_1_DRWREG	7400 0210Ch
10h	32	APBAP_CFG_1_BD0REG	7400 02110h
14h	32	APBAP_CFG_1_BD1REG	7400 02114h
18h	32	APBAP_CFG_1_BD2REG	7400 02118h
1Ch	32	APBAP_CFG_1_BD3REG	7400 0211Ch
F8h	32	APBAP_CFG_1_ROM_REGISTER	7400 021F8h
FCh	32	APBAP_CFG_1_ID_REGISTER	7400 021FCh

Table 14-28170. DEBUGSS_WRAP0_axiap_cfg_1 Registers, Base Address=0007 40002200h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	AXIAP_CFG_1_CSWREG	7400 02200h
4h	32	AXIAP_CFG_1_TAREGL	7400 02204h
8h	32	AXIAP_CFG_1_TAREGH	7400 02208h
Ch	32	AXIAP_CFG_1_DRWREG	7400 0220Ch

Table 14-28170. DEBUGSS_WRAP0_axiap_cfg_1 Registers, Base Address=0007 40002200h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
10h	32	AXIAP_CFG_1_BD0REG	7400 02210h
14h	32	AXIAP_CFG_1_BD1REG	7400 02214h
18h	32	AXIAP_CFG_1_BD2REG	7400 02218h
1Ch	32	AXIAP_CFG_1_BD3REG	7400 0221Ch
20h	32	AXIAP_CFG_1_MBT_REGISTER	7400 02220h
F0h	32	AXIAP_CFG_1_ROM_HI_REGISTER	7400 022F0h
F4h	32	AXIAP_CFG_1_CFG_REGISTER	7400 022F4h
F8h	32	AXIAP_CFG_1_ROM_LO_REGISTER	7400 022F8h
FCh	32	AXIAP_CFG_1_ID_REGISTER	7400 022FCh

Table 14-28171. DEBUGSS_WRAP0_pwrap_cfg_1 Registers, Base Address=0007 40002300h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	PWRAP_CFG_1_CORE_PRECREG0	7400 02300h
4h	32	PWRAP_CFG_1_CORE_PRECREG1	7400 02304h
8h	32	PWRAP_CFG_1_CORE_PRECREG2	7400 02308h
Ch	32	PWRAP_CFG_1_CORE_PRECREG3	7400 0230Ch
10h	32	PWRAP_CFG_1_CORE_PRECREG4	7400 02310h
14h	32	PWRAP_CFG_1_CORE_PRECREG5	7400 02314h
18h	32	PWRAP_CFG_1_CORE_PRECREG6	7400 02318h
1Ch	32	PWRAP_CFG_1_CORE_PRECREG7	7400 0231Ch
20h	32	PWRAP_CFG_1_CORE_PRECREG8	7400 02320h
24h	32	PWRAP_CFG_1_CORE_PRECREG9	7400 02324h
28h	32	PWRAP_CFG_1_CORE_PRECREG10	7400 02328h
2Ch	32	PWRAP_CFG_1_CORE_PRECREG11	7400 0232Ch
30h	32	PWRAP_CFG_1_CORE_PRECREG12	7400 02330h
34h	32	PWRAP_CFG_1_CORE_PRECREG13	7400 02334h
38h	32	PWRAP_CFG_1_CORE_PRECREG14	7400 02338h
3Ch	32	PWRAP_CFG_1_CORE_PRECREG15	7400 0233Ch
40h	32	PWRAP_CFG_1_CORE_PRECREG16	7400 02340h
44h	32	PWRAP_CFG_1_CORE_PRECREG17	7400 02344h
48h	32	PWRAP_CFG_1_CORE_PRECREG18	7400 02348h
4Ch	32	PWRAP_CFG_1_CORE_PRECREG19	7400 0234Ch
50h	32	PWRAP_CFG_1_CORE_PRECREG20	7400 02350h
54h	32	PWRAP_CFG_1_CORE_PRECREG21	7400 02354h
58h	32	PWRAP_CFG_1_CORE_PRECREG22	7400 02358h
5Ch	32	PWRAP_CFG_1_CORE_PRECREG23	7400 0235Ch
60h	32	PWRAP_CFG_1_CORE_PRECREG24	7400 02360h
64h	32	PWRAP_CFG_1_CORE_PRECREG25	7400 02364h
68h	32	PWRAP_CFG_1_CORE_PRECREG26	7400 02368h
6Ch	32	PWRAP_CFG_1_CORE_PRECREG27	7400 0236Ch
70h	32	PWRAP_CFG_1_CORE_PRECREG28	7400 02370h
74h	32	PWRAP_CFG_1_CORE_PRECREG29	7400 02374h
78h	32	PWRAP_CFG_1_CORE_PRECREG30	7400 02378h

Table 14-28171. DEBUGSS_WRAP0_pwrap_cfg_1 Registers, Base Address=0007 40002300h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
7Ch	32	PWRAP_CFG_1_CORE_PRECREG31	7400 0237Ch
F0h	32	PWRAP_CFG_1_SYS_PRECREG	7400 023F0h
FCh	32	PWRAP_CFG_1_ID_REGISTER	7400 023FCh

Table 14-28172. DEBUGSS_WRAP0_pview_cfg_1 Registers, Base Address=0007 40002400h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	PVIEW_CFG_1_PVIEW_STATE0	7400 02400h
F0h	32	PVIEW_CFG_1_PVIEW_CAPABILITY	7400 024F0h
FCh	32	PVIEW_CFG_1_ID_REGISTER	7400 024FCh

Table 14-28173. DEBUGSS_WRAP0_jtagap_cfg_1 Registers, Base Address=0007 40002500h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	JTAGAP_CFG_1_CSW	7400 02500h
4h	32	JTAGAP_CFG_1_PSEL_REG	7400 02504h
8h	32	JTAGAP_CFG_1_PSTA_REG	7400 02508h
10h	32	JTAGAP_CFG_1_BYTEFIFO1	7400 02510h
14h	32	JTAGAP_CFG_1_BYTEFIFO2	7400 02514h
18h	32	JTAGAP_CFG_1_BYTEFIFO3	7400 02518h
1Ch	32	JTAGAP_CFG_1_BYTEFIFO4	7400 0251Ch
FCh	32	JTAGAP_CFG_1_ID_REGISTER	7400 025FCh

Table 14-28174. DEBUGSS_WRAP0_secap_cfg_1 Registers, Base Address=0007 40002600h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	SECAP_CFG_1_TXDATA	7400 02600h
4h	32	SECAP_CFG_1_TXCTRL	7400 02604h
8h	32	SECAP_CFG_1_RXDATA	7400 02608h
Ch	32	SECAP_CFG_1_RXCTRL	7400 0260Ch

Table 14-28175. DEBUGSS_WRAP0_cortex0_cfg_1 Registers, Base Address=0007 40002700h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX0_CFG_1_CSWREG	7400 02700h
4h	32	CORTEX0_CFG_1_TAREG	7400 02704h
Ch	32	CORTEX0_CFG_1_DRWREG	7400 0270Ch
10h	32	CORTEX0_CFG_1_BD0REG	7400 02710h
14h	32	CORTEX0_CFG_1_BD1REG	7400 02714h
18h	32	CORTEX0_CFG_1_BD2REG	7400 02718h
1Ch	32	CORTEX0_CFG_1_BD3REG	7400 0271Ch
F8h	32	CORTEX0_CFG_1_ROM_REGISTER	7400 027F8h
FCh	32	CORTEX0_CFG_1_ID_REGISTER	7400 027FCh

Table 14-28176. DEBUGSS_WRAP0_cortex1_cfg_1 Registers, Base Address=0007 40002800h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX1_CFG_1_CSWREG	7400 02800h
4h	32	CORTEX1_CFG_1_TAREG	7400 02804h
Ch	32	CORTEX1_CFG_1_DRWREG	7400 0280Ch
10h	32	CORTEX1_CFG_1_BD0REG	7400 02810h
14h	32	CORTEX1_CFG_1_BD1REG	7400 02814h
18h	32	CORTEX1_CFG_1_BD2REG	7400 02818h
1Ch	32	CORTEX1_CFG_1_BD3REG	7400 0281Ch
F8h	32	CORTEX1_CFG_1_ROM_REGISTER	7400 028F8h
FCh	32	CORTEX1_CFG_1_ID_REGISTER	7400 028FCh

Table 14-28177. DEBUGSS_WRAP0_cortex2_cfg_1 Registers, Base Address=0007 40002900h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX2_CFG_1_CSWREG	7400 02900h
4h	32	CORTEX2_CFG_1_TAREG	7400 02904h
Ch	32	CORTEX2_CFG_1_DRWREG	7400 0290Ch
10h	32	CORTEX2_CFG_1_BD0REG	7400 02910h
14h	32	CORTEX2_CFG_1_BD1REG	7400 02914h
18h	32	CORTEX2_CFG_1_BD2REG	7400 02918h
1Ch	32	CORTEX2_CFG_1_BD3REG	7400 0291Ch
F8h	32	CORTEX2_CFG_1_ROM_REGISTER	7400 029F8h
FCh	32	CORTEX2_CFG_1_ID_REGISTER	7400 029FCh

Table 14-28178. DEBUGSS_WRAP0_cortex3_cfg_1 Registers, Base Address=0007 40002A00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX3_CFG_1_CSWREG	7400 02A00h
4h	32	CORTEX3_CFG_1_TAREG	7400 02A04h
Ch	32	CORTEX3_CFG_1_DRWREG	7400 02A0Ch
10h	32	CORTEX3_CFG_1_BD0REG	7400 02A10h
14h	32	CORTEX3_CFG_1_BD1REG	7400 02A14h
18h	32	CORTEX3_CFG_1_BD2REG	7400 02A18h
1Ch	32	CORTEX3_CFG_1_BD3REG	7400 02A1Ch
F8h	32	CORTEX3_CFG_1_ROM_REGISTER	7400 02AF8h
FCh	32	CORTEX3_CFG_1_ID_REGISTER	7400 02AFCh

Table 14-28179. DEBUGSS_WRAP0_cortex4_cfg_1 Registers, Base Address=0007 40002B00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX4_CFG_1_CSWREG	7400 02B00h
4h	32	CORTEX4_CFG_1_TAREG	7400 02B04h
Ch	32	CORTEX4_CFG_1_DRWREG	7400 02B0Ch
10h	32	CORTEX4_CFG_1_BD0REG	7400 02B10h

Table 14-28179. DEBUGSS_WRAP0_cortex4_cfg_1 Registers, Base Address=0007 40002B00h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
14h	32	CORTEX4_CFG_1_BD1REG	7400 02B14h
18h	32	CORTEX4_CFG_1_BD2REG	7400 02B18h
1Ch	32	CORTEX4_CFG_1_BD3REG	7400 02B1Ch
F8h	32	CORTEX4_CFG_1_ROM_REGISTER	7400 02BF8h
FCh	32	CORTEX4_CFG_1_ID_REGISTER	7400 02BFCh

Table 14-28180. DEBUGSS_WRAP0_cortex5_cfg_1 Registers, Base Address=0007 40002C00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX5_CFG_1_CSWREG	7400 02C00h
4h	32	CORTEX5_CFG_1_TAREG	7400 02C04h
Ch	32	CORTEX5_CFG_1_DRWREG	7400 02C0Ch
10h	32	CORTEX5_CFG_1_BD0REG	7400 02C10h
14h	32	CORTEX5_CFG_1_BD1REG	7400 02C14h
18h	32	CORTEX5_CFG_1_BD2REG	7400 02C18h
1Ch	32	CORTEX5_CFG_1_BD3REG	7400 02C1Ch
F8h	32	CORTEX5_CFG_1_ROM_REGISTER	7400 02CF8h
FCh	32	CORTEX5_CFG_1_ID_REGISTER	7400 02CFCh

Table 14-28181. DEBUGSS_WRAP0_cortex6_cfg_1 Registers, Base Address=0007 40002D00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX6_CFG_1_CSWREG	7400 02D00h
4h	32	CORTEX6_CFG_1_TAREG	7400 02D04h
Ch	32	CORTEX6_CFG_1_DRWREG	7400 02D0Ch
10h	32	CORTEX6_CFG_1_BD0REG	7400 02D10h
14h	32	CORTEX6_CFG_1_BD1REG	7400 02D14h
18h	32	CORTEX6_CFG_1_BD2REG	7400 02D18h
1Ch	32	CORTEX6_CFG_1_BD3REG	7400 02D1Ch
F8h	32	CORTEX6_CFG_1_ROM_REGISTER	7400 02DF8h
FCh	32	CORTEX6_CFG_1_ID_REGISTER	7400 02DFCh

Table 14-28182. DEBUGSS_WRAP0_cortex7_cfg_1 Registers, Base Address=0007 40002E00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX7_CFG_1_CSWREG	7400 02E00h
4h	32	CORTEX7_CFG_1_TAREG	7400 02E04h
Ch	32	CORTEX7_CFG_1_DRWREG	7400 02E0Ch
10h	32	CORTEX7_CFG_1_BD0REG	7400 02E10h
14h	32	CORTEX7_CFG_1_BD1REG	7400 02E14h
18h	32	CORTEX7_CFG_1_BD2REG	7400 02E18h
1Ch	32	CORTEX7_CFG_1_BD3REG	7400 02E1Ch
F8h	32	CORTEX7_CFG_1_ROM_REGISTER	7400 02EF8h

Table 14-28182. DEBUGSS_WRAP0_cortex7_cfg_1 Registers, Base Address=0007 40002E00h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
FCh	32	CORTEX7_CFG_1_ID_REGISTER	7400 02EFCh

Table 14-28183. DEBUGSS_WRAP0_cortex8_cfg_1 Registers, Base Address=0007 40002F00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CORTEX8_CFG_1_CSWREG	7400 02F00h
4h	32	CORTEX8_CFG_1_TAREG	7400 02F04h
Ch	32	CORTEX8_CFG_1_DRWREG	7400 02F0Ch
10h	32	CORTEX8_CFG_1_BD0REG	7400 02F10h
14h	32	CORTEX8_CFG_1_BD1REG	7400 02F14h
18h	32	CORTEX8_CFG_1_BD2REG	7400 02F18h
1Ch	32	CORTEX8_CFG_1_BD3REG	7400 02F1Ch
F8h	32	CORTEX8_CFG_1_ROM_REGISTER	7400 02FF8h
FCh	32	CORTEX8_CFG_1_ID_REGISTER	7400 02FFCh

Table 14-28184. DEBUGSS_WRAP0_ROM_TABLE_1_1 Registers, Base Address=0007 60000000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	ROM_TABLE_1_1_ROM_ENTRY0	7600 00000h
4h	32	ROM_TABLE_1_1_ROM_ENTRY1	7600 00004h
8h	32	ROM_TABLE_1_1_ROM_ENTRY2	7600 00008h
Ch	32	ROM_TABLE_1_1_ROM_ENTRY3	7600 0000Ch
10h	32	ROM_TABLE_1_1_ROM_ENTRY4	7600 00010h
14h	32	ROM_TABLE_1_1_ROM_ENTRY5	7600 00014h
18h	32	ROM_TABLE_1_1_COMPUTE_CLUSTER0	7600 00018h
1Ch	32	ROM_TABLE_1_1_COMPUTE_CLUSTER1	7600 0001Ch
20h	32	ROM_TABLE_1_1_COMPUTE_CLUSTER2	7600 00020h
24h	32	ROM_TABLE_1_1_DEBUG_CELL0	7600 00024h
28h	32	ROM_TABLE_1_1_DEBUG_CELL1	7600 00028h
2Ch	32	ROM_TABLE_1_1_DEBUG_CELL2	7600 0002Ch
30h	32	ROM_TABLE_1_1_DEBUG_CELL3	7600 00030h
34h	32	ROM_TABLE_1_1_DEBUG_CELL4	7600 00034h
38h	32	ROM_TABLE_1_1_DEBUG_CELL5	7600 00038h
3Ch	32	ROM_TABLE_1_1_DEBUG_CELL6	7600 0003Ch
40h	32	ROM_TABLE_1_1_DEBUG_CELL7	7600 00040h
44h	32	ROM_TABLE_1_1_DEBUG_CELL8	7600 00044h
48h	32	ROM_TABLE_1_1_DEBUG_CELL9	7600 00048h
4Ch	32	ROM_TABLE_1_1_DEBUG_CELL10	7600 0004Ch
50h	32	ROM_TABLE_1_1_DEBUG_CELL11	7600 00050h
50h	32	ROM_TABLE_1_1_EXTCSCOMP0	7600 00050h
54h	32	ROM_TABLE_1_1_EXTCSCOMP1	7600 00054h
58h	32	ROM_TABLE_1_1_EXTCSCOMP2	7600 00058h
5Ch	32	ROM_TABLE_1_1_EXTCSCOMP3	7600 0005Ch

Table 14-28184. DEBUGSS_WRAP0_ROM_TABLE_1_1 Registers, Base Address=0007 60000000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
60h	32	ROM_TABLE_1_1_EXTCSCOMP4	7600 00060h
64h	32	ROM_TABLE_1_1_EXTCSCOMP5	7600 00064h
68h	32	ROM_TABLE_1_1_EXTCSCOMP6	7600 00068h
6Ch	32	ROM_TABLE_1_1_EXTCSCOMP7	7600 0006Ch
70h	32	ROM_TABLE_1_1_EXTCSCOMP8	7600 00070h
74h	32	ROM_TABLE_1_1_EXTCSCOMP9	7600 00074h
78h	32	ROM_TABLE_1_1_EXTCSCOMP10	7600 00078h
7Ch	32	ROM_TABLE_1_1_EXTCSCOMP11	7600 0007Ch

Table 14-28185. DEBUGSS_WRAP0_drm_cfg_1 Registers, Base Address=0007 60002000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	DRM_CFG_1_PERIPH_ID	7600 02000h
4h	32	DRM_CFG_1_VERSION	7600 02004h
8h	32	DRM_CFG_1_CAPABILITY	7600 02008h
Ch	32	DRM_CFG_1_TRACE_CTRL	7600 0200Ch
10h	32	DRM_CFG_1_VBUSM_CTRL	7600 02010h
14h	32	DRM_CFG_1_DAP_TIMEOUT	7600 02014h
18h	32	DRM_CFG_1_CONFIG	7600 02018h
1Ch	32	DRM_CFG_1_EMUTRIGEN	7600 0201Ch
20h	32	DRM_CFG_1_BINVALLO	7600 02020h
24h	32	DRM_CFG_1_BINVALHI	7600 02024h
200h	32	DRM_CFG_1_SUSPEND_REG0	7600 02200h
204h	32	DRM_CFG_1_SUSPEND_REG1	7600 02204h
208h	32	DRM_CFG_1_SUSPEND_REG2	7600 02208h
20Ch	32	DRM_CFG_1_SUSPEND_REG3	7600 0220Ch
210h	32	DRM_CFG_1_SUSPEND_REG4	7600 02210h
214h	32	DRM_CFG_1_SUSPEND_REG5	7600 02214h
218h	32	DRM_CFG_1_SUSPEND_REG6	7600 02218h
21Ch	32	DRM_CFG_1_SUSPEND_REG7	7600 0221Ch
220h	32	DRM_CFG_1_SUSPEND_REG8	7600 02220h
224h	32	DRM_CFG_1_SUSPEND_REG9	7600 02224h
228h	32	DRM_CFG_1_SUSPEND_REG10	7600 02228h
22Ch	32	DRM_CFG_1_SUSPEND_REG11	7600 0222Ch
230h	32	DRM_CFG_1_SUSPEND_REG12	7600 02230h
234h	32	DRM_CFG_1_SUSPEND_REG13	7600 02234h
238h	32	DRM_CFG_1_SUSPEND_REG14	7600 02238h
23Ch	32	DRM_CFG_1_SUSPEND_REG15	7600 0223Ch
240h	32	DRM_CFG_1_SUSPEND_REG16	7600 02240h
244h	32	DRM_CFG_1_SUSPEND_REG17	7600 02244h
248h	32	DRM_CFG_1_SUSPEND_REG18	7600 02248h
24Ch	32	DRM_CFG_1_SUSPEND_REG19	7600 0224Ch
250h	32	DRM_CFG_1_SUSPEND_REG20	7600 02250h
254h	32	DRM_CFG_1_SUSPEND_REG21	7600 02254h

Table 14-28185. DEBUGSS_WRAP0_drm_cfg_1 Registers, Base Address=0007 60002000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
258h	32	DRM_CFG_1_SUSPEND_REG22	7600 02258h
25Ch	32	DRM_CFG_1_SUSPEND_REG23	7600 0225Ch
260h	32	DRM_CFG_1_SUSPEND_REG24	7600 02260h
264h	32	DRM_CFG_1_SUSPEND_REG25	7600 02264h
268h	32	DRM_CFG_1_SUSPEND_REG26	7600 02268h
26Ch	32	DRM_CFG_1_SUSPEND_REG27	7600 0226Ch
270h	32	DRM_CFG_1_SUSPEND_REG28	7600 02270h
274h	32	DRM_CFG_1_SUSPEND_REG29	7600 02274h
278h	32	DRM_CFG_1_SUSPEND_REG30	7600 02278h
27Ch	32	DRM_CFG_1_SUSPEND_REG31	7600 0227Ch

Table 14-28186. DEBUGSS_WRAP0_cstpiu_cfg_1 Registers, Base Address=0007 60004000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CSTPIU_CFG_1_SUPPORTSIZE	7600 04000h
4h	32	CSTPIU_CFG_1_CURPORTSIZE	7600 04004h
100h	32	CSTPIU_CFG_1_TRIGMODEREG	7600 04100h
104h	32	CSTPIU_CFG_1_TRIGCTRREG	7600 04104h
108h	32	CSTPIU_CFG_1_TRIGMPYREG	7600 04108h
200h	32	CSTPIU_CFG_1_SUPTESTPAT	7600 04200h
204h	32	CSTPIU_CFG_1_CURTESTPAT	7600 04204h
208h	32	CSTPIU_CFG_1_TESTPATCNT	7600 04208h
300h	32	CSTPIU_CFG_1_FORMFLUSHSTAT	7600 04300h
304h	32	CSTPIU_CFG_1_FORMFLUSHCTL	7600 04304h
308h	32	CSTPIU_CFG_1_FORMSYNCCTR	7600 04308h
400h	32	CSTPIU_CFG_1_EXTCTLIN	7600 04400h
404h	32	CSTPIU_CFG_1_EXTCTLOUT	7600 04404h
EE4h	32	CSTPIU_CFG_1_ITTRFLINACK	7600 04EE4h
EE8h	32	CSTPIU_CFG_1_ITTRFLIN	7600 04EE8h
EECh	32	CSTPIU_CFG_1_ITATBDATA0	7600 04EECh
EF0h	32	CSTPIU_CFG_1_ITATBCTR2	7600 04EF0h
EF4h	32	CSTPIU_CFG_1_ITATBCTR1	7600 04EF4h
EF8h	32	CSTPIU_CFG_1_ITATBCTR0	7600 04EF8h
F00h	32	CSTPIU_CFG_1_INTCTRL	7600 04F00h
FA0h	32	CSTPIU_CFG_1_CTSET	7600 04FA0h
FA4h	32	CSTPIU_CFG_1_CTCLR	7600 04FA4h
FB0h	32	CSTPIU_CFG_1_LAREG	7600 04FB0h
FB4h	32	CSTPIU_CFG_1_LSREG	7600 04FB4h
FB8h	32	CSTPIU_CFG_1_AUTHST	7600 04FB8h
FC8h	32	CSTPIU_CFG_1_DEVID	7600 04FC8h
FCCh	32	CSTPIU_CFG_1_DEVTYPEID	7600 04FCCh
FD0h	32	CSTPIU_CFG_1_PERID4	7600 04FD0h
FE0h	32	CSTPIU_CFG_1_PERID0	7600 04FE0h

Table 14-28186. DEBUGSS_WRAP0_cstpiu_cfg_1 Registers, Base Address=0007 60004000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
FE4h	32	CSTPIU_CFG_1_PERID1	7600 04FE4h
FE8h	32	CSTPIU_CFG_1_PERID2	7600 04FE8h
FECh	32	CSTPIU_CFG_1_PERID3	7600 04FECh
FF0h	32	CSTPIU_CFG_1_COMPID0	7600 04FF0h
FF4h	32	CSTPIU_CFG_1_COMPID1	7600 04FF4h
FF8h	32	CSTPIU_CFG_1_COMPID2	7600 04FF8h
FFCh	32	CSTPIU_CFG_1_COMPID3	7600 04FFCh

Table 14-28187. DEBUGSS_WRAP0_ctf_cfg_1 Registers, Base Address=0007 60005000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP Physical Address
0h	32	CTF_CFG_1_CSTFCTLREG	7600 05000h
4h	32	CTF_CFG_1_PRIORCTLREG	7600 05004h
EECh	32	CTF_CFG_1_ITATBDATA0	7600 05EECh
EF0h	32	CTF_CFG_1_ITATBCTR2	7600 05EF0h
EF4h	32	CTF_CFG_1_ITATBCTR1	7600 05EF4h
EF8h	32	CTF_CFG_1_ITATBCTR0	7600 05EF8h
F00h	32	CTF_CFG_1_INTCTRL	7600 05F00h
FA0h	32	CTF_CFG_1_CTSET	7600 05FA0h
FA4h	32	CTF_CFG_1_CTCLR	7600 05FA4h
FB0h	32	CTF_CFG_1_LAREG	7600 05FB0h
FB4h	32	CTF_CFG_1_LSREG	7600 05FB4h
FB8h	32	CTF_CFG_1_AUTHST	7600 05FB8h
FC8h	32	CTF_CFG_1_DEVID	7600 05FC8h
FCCh	32	CTF_CFG_1_DEVTYPEID	7600 05FCCh
FD0h	32	CTF_CFG_1_PERID4	7600 05FD0h
FD4h	32	CTF_CFG_1_PERID5	7600 05FD4h
FD8h	32	CTF_CFG_1_PERID6	7600 05FD8h
FDCh	32	CTF_CFG_1_PERID7	7600 05FDCh
FE0h	32	CTF_CFG_1_PERID0	7600 05FE0h
FE4h	32	CTF_CFG_1_PERID1	7600 05FE4h
FE8h	32	CTF_CFG_1_PERID2	7600 05FE8h
FECh	32	CTF_CFG_1_PERID3	7600 05FECh
FF0h	32	CTF_CFG_1_COMPID0	7600 05FF0h
FF4h	32	CTF_CFG_1_COMPID1	7600 05FF4h
FF8h	32	CTF_CFG_1_COMPID2	7600 05FF8h
FFCh	32	CTF_CFG_1_COMPID3	7600 05FFCh

14.11.2.2 ROM_TABLE_0_0_ROM_ENTRY0 Register

ROM_TABLE_0_0_ROM_ENTRY0 Register (Offset = 0h) [reset = 2003h]

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Table 14-28188. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00000h

Figure 14-9287. ROM_TABLE_0_0_ROM_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
2h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
2h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-28190. ROM_TABLE_0_0_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.3 ROM_TABLE_0_0_ROM_ENTRY1 Register

ROM_TABLE_0_0_ROM_ENTRY1 Register (Offset = 4h) [reset = 2000003h]

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Table 14-28191. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00004h

Figure 14-9288. ROM_TABLE_0_0_ROM_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2000h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
2000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
2000h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-28193. ROM_TABLE_0_0_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.4 ROM_TABLE_0_0_ROM_ENTRY2 Register

ROM_TABLE_0_0_ROM_ENTRY2 Register (Offset = 8h) [reset = 3h]

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Table 14-28194. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00008h

Figure 14-9289. ROM_TABLE_0_0_ROM_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				RA30			PWRID
NONE				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-28196. ROM_TABLE_0_0_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	RESERVED	NONE	0h	Reserved
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.5 ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register (Offset = 8h) [reset = 10h]

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Table 14-28197. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00008h

Figure 14-9290. ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28199. ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.6 ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register (Offset = Ch) [reset = 10h]

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Table 14-28200. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0000Ch

Figure 14-9291. ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28202. ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.7 ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register (Offset = 10h) [reset = 10h]

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Table 14-28203. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00010h

Figure 14-9292. ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28205. ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.8 ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register (Offset = 14h) [reset = 10h]

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Table 14-28206. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00014h

Figure 14-9293. ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28208. ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.9 ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register (Offset = 18h) [reset = 10h]

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Table 14-28209. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00018h

Figure 14-9294. ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28211. ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.10 ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register (Offset = 1Ch) [reset = 10h]

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Table 14-28212. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0001Ch

Figure 14-9295. ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28214. ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.11 ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register (Offset = 20h) [reset = 10h]

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Table 14-28215. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00020h

Figure 14-9296. ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28217. ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.12 ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register (Offset = 24h) [reset = 10h]

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Table 14-28218. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00024h

Figure 14-9297. ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28220. ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.13 ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register (Offset = 28h) [reset = 10h]

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Table 14-28221. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00028h

Figure 14-9298. ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28223. ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.14 ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register (Offset = 2Ch) [reset = 10h]

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Table 14-28224. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0002Ch

Figure 14-9299. ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28226. ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.15 ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register (Offset = 30h) [reset = 10h]

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Table 14-28227. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00030h

Figure 14-9300. ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28229. ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.16 ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register (Offset = 34h) [reset = 10h]

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Table 14-28230. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00034h

Figure 14-9301. ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28232. ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.17 ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register (Offset = 38h) [reset = 10h]

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Table 14-28233. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00038h

Figure 14-9302. ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28235. ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.18 ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register (Offset = 3Ch) [reset = 10h]

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Table 14-28236. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0003Ch

Figure 14-9303. ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28238. ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.19 ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register (Offset = 40h) [reset = 10h]

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Table 14-28239. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00040h

Figure 14-9304. ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28241. ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.20 ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register (Offset = 44h) [reset = 10h]

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Table 14-28242. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00044h

Figure 14-9305. ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28244. ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.21 ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register (Offset = 48h) [reset = 10h]

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Table 14-28245. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00048h

Figure 14-9306. ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28247. ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.22 ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register (Offset = 4Ch) [reset = 10h]

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Table 14-28248. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0004Ch

Figure 14-9307. ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28250. ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.23 ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register (Offset = 50h) [reset = 10h]

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Table 14-28251. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00050h

Figure 14-9308. ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28253. ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.24 ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register (Offset = 54h) [reset = 10h]

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Table 14-28254. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00054h

Figure 14-9309. ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28256. ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.25 ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register (Offset = 58h) [reset = 10h]

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Table 14-28257. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00058h

Figure 14-9310. ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28259. ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.26 ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register (Offset = 5Ch) [reset = 10h]

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Table 14-28260. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0005Ch

Figure 14-9311. ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28262. ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.27 ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register (Offset = 60h) [reset = 10h]

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Table 14-28263. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00060h

Figure 14-9312. ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28265. ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.28 ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register (Offset = 64h) [reset = 10h]

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Table 14-28266. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00064h

Figure 14-9313. ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28268. ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.29 ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register (Offset = 68h) [reset = 10h]

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Table 14-28269. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00068h

Figure 14-9314. ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28271. ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.30 ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register (Offset = 6Ch) [reset = 10h]

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Table 14-28272. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0006Ch

Figure 14-9315. ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28274. ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.31 ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register (Offset = 70h) [reset = 10h]

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Table 14-28275. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00070h

Figure 14-9316. ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28277. ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.32 ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register (Offset = 74h) [reset = 10h]

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Table 14-28278. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00074h

Figure 14-9317. ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28280. ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.33 ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register (Offset = 78h) [reset = 10h]

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Table 14-28281. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00078h

Figure 14-9318. ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28283. ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.34 ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register (Offset = 7Ch) [reset = 10h]

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Table 14-28284. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0007Ch

Figure 14-9319. ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28286. ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.35 ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register (Offset = 80h) [reset = 10h]

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Table 14-28287. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00080h

Figure 14-9320. ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28289. ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.36 ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register (Offset = 84h) [reset = 10h]

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Table 14-28290. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00084h

Figure 14-9321. ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28292. ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.37 ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register (Offset = 88h) [reset = 10h]

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Table 14-28293. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00088h

Figure 14-9322. ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28295. ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.38 ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register (Offset = 8Ch) [reset = 10h]

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Table 14-28296. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0008Ch

Figure 14-9323. ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28298. ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.39 ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register (Offset = 90h) [reset = 10h]

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Table 14-28299. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00090h

Figure 14-9324. ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28301. ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.40 ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register (Offset = 94h) [reset = 10h]

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Table 14-28302. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00094h

Figure 14-9325. ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28304. ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.41 ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register (Offset = 98h) [reset = 10h]

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Table 14-28305. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00098h

Figure 14-9326. ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28307. ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.42 ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register (Offset = 9Ch) [reset = 10h]

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Table 14-28308. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0009Ch

Figure 14-9327. ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28310. ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.43 ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register (Offset = A0h) [reset = 10h]

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Table 14-28311. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000A0h

Figure 14-9328. ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28313. ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.44 ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register (Offset = A4h) [reset = 10h]

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Table 14-28314. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000A4h

Figure 14-9329. ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28316. ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.45 ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register (Offset = A8h) [reset = 10h]

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Table 14-28317. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000A8h

Figure 14-9330. ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28319. ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.46 ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register (Offset = ACh) [reset = 10h]

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Table 14-28320. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000ACh

Figure 14-9331. ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28322. ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.47 ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register (Offset = B0h) [reset = 10h]

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Table 14-28323. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000B0h

Figure 14-9332. ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28325. ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.48 ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register (Offset = B4h) [reset = 10h]

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Table 14-28326. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000B4h

Figure 14-9333. ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28328. ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.49 ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register (Offset = B8h) [reset = 10h]

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Table 14-28329. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000B8h

Figure 14-9334. ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28331. ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.50 ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register (Offset = BCh) [reset = 10h]

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Table 14-28332. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000BCh

Figure 14-9335. ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28334. ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.51 ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register (Offset = C0h) [reset = 10h]

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Table 14-28335. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000C0h

Figure 14-9336. ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28337. ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.52 ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register (Offset = C4h) [reset = 10h]

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Table 14-28338. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000C4h

Figure 14-9337. ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28340. ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.53 ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register (Offset = C8h) [reset = 10h]

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Table 14-28341. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000C8h

Figure 14-9338. ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28343. ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.54 ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register (Offset = CCh) [reset = 10h]

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Table 14-28344. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000CCh

Figure 14-9339. ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28346. ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.55 ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register (Offset = D0h) [reset = 10h]

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Table 14-28347. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000D0h

Figure 14-9340. ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28349. ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.56 ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register (Offset = D4h) [reset = 10h]

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Table 14-28350. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000D4h

Figure 14-9341. ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28352. ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.57 ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register (Offset = D8h) [reset = 10h]

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Table 14-28353. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000D8h

Figure 14-9342. ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28355. ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.58 ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register (Offset = DCh) [reset = 10h]

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Table 14-28356. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000DCh

Figure 14-9343. ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28358. ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.59 ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register (Offset = E0h) [reset = 10h]

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Table 14-28359. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000E0h

Figure 14-9344. ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28361. ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.60 ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register (Offset = E4h) [reset = 10h]

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Table 14-28362. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000E4h

Figure 14-9345. ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28364. ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.61 ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register (Offset = E8h) [reset = 10h]

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Table 14-28365. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000E8h

Figure 14-9346. ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28367. ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.62 ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register (Offset = ECh) [reset = 10h]

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Table 14-28368. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000ECh

Figure 14-9347. ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28370. ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.63 ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register (Offset = F0h) [reset = 10h]

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Table 14-28371. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000F0h

Figure 14-9348. ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28373. ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.64 ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register (Offset = F4h) [reset = 10h]

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Table 14-28374. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000F4h

Figure 14-9349. ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28376. ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.65 ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register (Offset = F8h) [reset = 10h]

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Table 14-28377. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000F8h

Figure 14-9350. ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28379. ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.66 ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register (Offset = FCh) [reset = 10h]

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Table 14-28380. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 000FCh

Figure 14-9351. ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28382. ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.67 ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register (Offset = 100h) [reset = 10h]

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Table 14-28383. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00100h

Figure 14-9352. ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28385. ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.68 ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register

ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register (Offset = 104h) [reset = 10h]

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Table 14-28386. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00104h

Figure 14-9353. ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-28388. ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.69 ROM_TABLE_0_0_PERIPHID0 Register

ROM_TABLE_0_0_PERIPHID0 Register (Offset = 108h) [reset = 2h]

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Table 14-28389. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00108h

Figure 14-9354. ROM_TABLE_0_0_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28391. ROM_TABLE_0_0_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.70 ROM_TABLE_0_0_PERIPHID1 Register

ROM_TABLE_0_0_PERIPHID1 Register (Offset = 10Ch) [reset = 2h]

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Table 14-28392. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 0010Ch

Figure 14-9355. ROM_TABLE_0_0_PERIPHID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-28394. ROM_TABLE_0_0_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.71 ROM_TABLE_0_0_PERIPHID2 Register

ROM_TABLE_0_0_PERIPHID2 Register (Offset = 110h) [reset = 2h]

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Table 14-28395. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00110h

Figure 14-9356. ROM_TABLE_0_0_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28397. ROM_TABLE_0_0_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.72 ROM_TABLE_0_0_PERIPHID3 Register

ROM_TABLE_0_0_PERIPHID3 Register (Offset = 114h) [reset = 2h]

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Table 14-28398. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00114h

Figure 14-9357. ROM_TABLE_0_0_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28400. ROM_TABLE_0_0_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.73 ROM_TABLE_0_0_PERIPHID4 Register

ROM_TABLE_0_0_PERIPHID4 Register (Offset = 118h) [reset = 2h]

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Table 14-28401. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 00118h

Figure 14-9358. ROM_TABLE_0_0_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28403. ROM_TABLE_0_0_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.74 ROM_TABLE_0_0_COMPID0 Register

ROM_TABLE_0_0_COMPID0 Register (Offset = 3FCh) [reset = Dh]

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Table 14-28404. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 003FCh

Figure 14-9359. ROM_TABLE_0_0_COMPID0 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
Dh							
23	22	21	20	19	18	17	16
VAR							
R							
Dh							
15	14	13	12	11	10	9	8
VAR							
R							
Dh							
7	6	5	4	3	2	1	0
VAR							
R							
Dh							

Table 14-28406. ROM_TABLE_0_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	Dh	Component id0

14.11.2.75 ROM_TABLE_0_0_COMPID1 Register

ROM_TABLE_0_0_COMPID1 Register (Offset = 3FCh) [reset = 10h]

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Table 14-28407. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 003FCh

Figure 14-9360. ROM_TABLE_0_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
10h							
23	22	21	20	19	18	17	16
VAR							
R							
10h							
15	14	13	12	11	10	9	8
VAR							
R							
10h							
7	6	5	4	3	2	1	0
VAR							
R							
10h							

Table 14-28409. ROM_TABLE_0_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	10h	Component id1

14.11.2.76 ROM_TABLE_0_0_COMPID2 Register

ROM_TABLE_0_0_COMPID2 Register (Offset = 3FCh) [reset = 5h]

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Table 14-28410. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 003FCh

Figure 14-9361. ROM_TABLE_0_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
5h							
23	22	21	20	19	18	17	16
VAR							
R							
5h							
15	14	13	12	11	10	9	8
VAR							
R							
5h							
7	6	5	4	3	2	1	0
VAR							
R							
5h							

Table 14-28412. ROM_TABLE_0_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	5h	Component id2

14.11.2.77 ROM_TABLE_0_0_COMPID3 Register

ROM_TABLE_0_0_COMPID3 Register (Offset = 3FCh) [reset = B1h]

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Table 14-28413. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_0	7000 003FCh

Figure 14-9362. ROM_TABLE_0_0_COMPID3 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
B1h							
23	22	21	20	19	18	17	16
VAR							
R							
B1h							
15	14	13	12	11	10	9	8
VAR							
R							
B1h							
7	6	5	4	3	2	1	0
VAR							
R							
B1h							

Table 14-28415. ROM_TABLE_0_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	B1h	Component id3

14.11.2.78 CFGAP_CFG_0_JTAGID_REG Register

CFGAP_CFG_0_JTAGID_REG Register (Offset = 0h) [reset = 0h]

Register Description: This register returns the JTAG ID tieoff of the device. The reset value depends on the tie off

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Table 14-28416. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_0	7000 02000h

Figure 14-9363. CFGAP_CFG_0_JTAGID_REG Name Register

31	30	29	28	27	26	25	24
JTAG_ID							
R							
0h							
23	22	21	20	19	18	17	16
JTAG_ID							
R							
0h							
15	14	13	12	11	10	9	8
JTAG_ID							
R							
0h							
7	6	5	4	3	2	1	0
JTAG_ID							
R							
0h							

Table 14-28418. CFGAP_CFG_0_JTAGID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_ID	R	0h	The JTAG ID of the device

14.11.2.79 CFGAP_CFG_0_USERID_REG Register

CFGAP_CFG_0_USERID_REG Register (Offset = 4h) [reset = 0h]

Register Description: This register returns the Chip Spin ID tieoff value of the device. The reset value depends on the tieoff

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Table 14-28419. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_0	7000 02004h

Figure 14-9364. CFGAP_CFG_0_USERID_REG Name Register

31	30	29	28	27	26	25	24
USER_ID							
R							
0h							
23	22	21	20	19	18	17	16
USER_ID							
R							
0h							
15	14	13	12	11	10	9	8
USER_ID							
R							
0h							
7	6	5	4	3	2	1	0
USER_ID							
R							
0h							

Table 14-28421. CFGAP_CFG_0_USERID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USER_ID	R	0h	The USER ID of the device

14.11.2.80 CFGAP_CFG_0_VERSION_REG Register

CFGAP_CFG_0_VERSION_REG Register (Offset = 8h) [reset = 0h]

Register Description: This register is used to read the RTL version information and to determine which modules are included in the rtl build. The reset value depends on the build options

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Table 14-28422. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_0	7000 02008h

Figure 14-9365. CFGAP_CFG_0_VERSION_REG Name Register

31	30	29	28	27	26	25	24
MAJOR_REV				MINOR_REV			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							JTAG_AP
R							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POWERAP	AXIAP	APBAP	SECURITYAP	SPARE	ICEPICKM	TRIGGERSUPPORT	TRACESUPPORT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28424. CFGAP_CFG_0_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	MAJOR_REV	R	0h	RTL Major revision [5]
27:24	MINOR_REV	R	0h	RTL Minor revision [0]
23:9	RESERVED	R	0h	Reserved, returns 0
8	JTAG_AP	R	0h	a 1 indicates JTAG AP is supported
7	POWERAP	R	0h	A 1 indicates that the Power AP is supported
6	AXIAP	R	0h	A 1 indicates that the AXIAP exists and system memory accesses are supported
5	APBAP	R	0h	A 1 indicates that the APBAP exisits and accesses to external debug logic are supported
4	SECURITYAP	R	0h	A 1 indicates that the Security AP is supported
3	SPARE	R	0h	This is a spare bit, returns 0
2	ICEPICKM	R	0h	A 1 indicates that ICEPick M is present inthe design
1	TRIGGERSUPPORT	R	0h	A 1 indicates that cross triggering is supported
0	TRACESUPPORT	R	0h	A 1 indicates that hardware trace export is supported

14.11.2.81 CFGAP_CFG_0_SYSTEMSTATUS Register

CFGAP_CFG_0_SYSTEMSTATUS Register (Offset = Ch) [reset = 0h]

Register Description: Reading this register returns system status information.

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Table 14-28425. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_0	7000 0200Ch

Figure 14-9366. CFGAP_CFG_0_SYSTEMSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-28427. CFGAP_CFG_0_SYSTEMSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved, returns 0

14.11.2.82 CFGAP_CFG_0_APID_REGISTER Register

CFGAP_CFG_0_APID_REGISTER Register (Offset = FCh) [reset = 20E0001h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28428. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_0	7000 020FCh

Figure 14-9367. CFGAP_CFG_0_APID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				107h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
107h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				1h			

Table 14-28430. CFGAP_CFG_0_APID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	107h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	1h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.83 APBAP_CFG_0_CSWREG Register

APBAP_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: Control/Status Register

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Table 14-28431. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 02100h

Figure 14-9368. APBAP_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28433. APBAP_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.84 APBAP_CFG_0_TAREG Register

APBAP_CFG_0_TAREG Register (Offset = 4h) [reset = 0h]

Register Description: This register contains the address to write to or read from.

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Table 14-28434. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 02104h

Figure 14-9369. APBAP_CFG_0_TAREG Name Register

31	30	29	28	27	26	25	24
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							

Table 14-28436. APBAP_CFG_0_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRANSFER_ADDRESS_REGISTER	R/W	0h	This register contains the address to write to or read from

14.11.2.85 APBAP_CFG_0_DRWREG Register

APBAP_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28437. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 0210Ch

Figure 14-9370. APBAP_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28439. APBAP_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.86 APBAP_CFG_0_BD0REG Register

APBAP_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28440. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 02110h

Figure 14-9371. APBAP_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28442. APBAP_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.87 APBAP_CFG_0_BD1REG Register

APBAP_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28443. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 02114h

Figure 14-9372. APBAP_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28445. APBAP_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.88 APBAP_CFG_0_BD2REG Register

APBAP_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28446. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 02118h

Figure 14-9373. APBAP_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28448. APBAP_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.89 APBAP_CFG_0_BD3REG Register

APBAP_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28449. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 0211Ch

Figure 14-9374. APBAP_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28451. APBAP_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.90 APBAP_CFG_0_ROM_REGISTER Register

APBAP_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the APB ROM Address.

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Table 14-28452. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 021F8h

Figure 14-9375. APBAP_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER_ADDRESS							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROM_REGISTER_ADDRESS							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ROM_REGISTER_ADDRESS							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ROM_REGISTER_ADDRESS							
R							
0h							

Table 14-28454. APBAP_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER_ADDRESS	R	0h	Reading this register returns the APB ROM Address

14.11.2.91 APBAP_CFG_0_ID_REGISTER Register

APBAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28455. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_0	7000 021FCh

Figure 14-9376. APBAP_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28457. APBAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.11.2.92 AXIAP_CFG_0_CSWREG Register

AXIAP_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This is the control/status register

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Table 14-28458. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 02200h

Figure 14-9377. AXIAP_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
DBGSWEN	TYPEEXT						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
SPIDEN	RESERVED2						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
TYPE				MODE			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
TRINPROG	RESERVED1	ADDR_INC		RESERVED0	SIZE		
R	R	R/W		R	R		
0h	0h	0h		0h	0h		

Table 14-28460. AXIAP_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBGSWEN	R/W	0h	Indicates whether accesses should treated as application or debug
30:24	TYPEEXT	R/W	0h	
23	SPIDEN	R	0h	When 1, secure accesses are enabled
22:16	RESERVED2	R	0h	Reserved, reads return 0
15:12	TYPE	R/W	0h	Sets Prot, Type attributes for the access
11:8	MODE	R/W	0h	Sets mode of operation 0000=basic, 0001=Barrier extensions, all other values reserved
7	TRINPROG	R	0h	This bit is set to 1 while a transfer is in progress on the connection to the memory system, and is set to 0 while the connection is idle
6	RESERVED1	R	0h	This bit is reserved and reads return 0
5:4	ADDR_INC	R/W	0h	Address Auto Increment and packing mode
3	RESERVED0	R	0h	reserved, returns 0
2:0	SIZE	R	0h	This specifies the size of the access For this implementation, the access is always 32 bits [010]

14.11.2.93 AXIAP_CFG_0_TAREGL Register

AXIAP_CFG_0_TAREGL Register (Offset = 4h) [reset = 0h]

Register Description: This register contains the lower 32-bits of address to write to or read from.

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Table 14-28461. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 02204h

Figure 14-9378. AXIAP_CFG_0_TAREGL Name Register

31	30	29	28	27	26	25	24
TAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TAL							
R/W							
0h							

Table 14-28463. AXIAP_CFG_0_TAREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TAL	R/W	0h	This register contains the lower 32-bits of address

14.11.2.94 AXIAP_CFG_0_TAREGH Register

AXIAP_CFG_0_TAREGH Register (Offset = 8h) [reset = 0h]

Register Description: This register contains the upper 32-bits of address to write to or read from.

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Table 14-28464. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 02208h

Figure 14-9379. AXIAP_CFG_0_TAREGH Name Register

31	30	29	28	27	26	25	24
TAH							
R/W							
0h							
23	22	21	20	19	18	17	16
TAH							
R/W							
0h							
15	14	13	12	11	10	9	8
TAH							
R/W							
0h							
7	6	5	4	3	2	1	0
TAH							
R/W							
0h							

Table 14-28466. AXIAP_CFG_0_TAREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TAH	R/W	0h	This register contains the upper 32-bits of address

14.11.2.95 AXIAP_CFG_0_DRWREG Register

AXIAP_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28467. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 0220Ch

Figure 14-9380. AXIAP_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28469. AXIAP_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.96 AXIAP_CFG_0_BD0REG Register

AXIAP_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28470. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 02210h

Figure 14-9381. AXIAP_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28472. AXIAP_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.97 AXIAP_CFG_0_BD1REG Register

AXIAP_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28473. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 02214h

Figure 14-9382. AXIAP_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							

23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							

15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							

7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28475. AXIAP_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.98 AXIAP_CFG_0_BD2REG Register

AXIAP_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28476. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 02218h

Figure 14-9383. AXIAP_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28478. AXIAP_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.99 AXIAP_CFG_0_BD3REG Register

AXIAP_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28479. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 0221Ch

Figure 14-9384. AXIAP_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28481. AXIAP_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.100 AXIAP_CFG_0_MBT_REGISTER Register

AXIAP_CFG_0_MBT_REGISTER Register (Offset = 20h) [reset = 0h]

Register Description: This register sets memory barrier attributes

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Table 14-28482. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 02220h

Figure 14-9385. AXIAP_CFG_0_MBT_REGISTER Name Register

31	30	29	28	27	26	25	24
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							

Table 14-28484. AXIAP_CFG_0_MBT_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEMORY_BARRIER_TRANSFER_REGISTER	R/W	0h	This register sets memory barrier attributes

14.11.2.101 AXIAP_CFG_0_ROM_HI_REGISTER Register

AXIAP_CFG_0_ROM_HI_REGISTER Register (Offset = F0h) [reset = 0h]

Register Description: Reading this register returns the AXI ROM Address (63-32).

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Table 14-28485. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 022F0h

Figure 14-9386. AXIAP_CFG_0_ROM_HI_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_HI_REGISTER_ADDRESS							
R							
0h							
23	22	21	20	19	18	17	16
ROM_HI_REGISTER_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
ROM_HI_REGISTER_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
ROM_HI_REGISTER_ADDRESS							
R							
0h							

Table 14-28487. AXIAP_CFG_0_ROM_HI_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_HI_REGISTER_ADDRESS	R	0h	Reading this register returns the upper ROM Address

14.11.2.102 AXIAP_CFG_0_CFG_REGISTER Register

AXIAP_CFG_0_CFG_REGISTER Register (Offset = F4h) [reset = 0h]

Register Description: The CFG register provides information about how the MEM-AP implementation is configured.

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Table 14-28488. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 022F4h

Figure 14-9387. AXIAP_CFG_0_CFG_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					LD	LA	BE
R					R	R	R
0h					0h	0h	0h

Table 14-28490. AXIAP_CFG_0_CFG_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved bit, return 0
2	LD	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Data Extension, that provides support for data items larger than 32-bits, it is 0
1	LA	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Physical Address Extension, that supports physical addresses of more than 32-bits:
0	BE	R	0h	ADIv52 obsoletes support for big-endian MEM-AP, and this bit must RAZ

14.11.2.103 AXIAP_CFG_0_ROM_LO_REGISTER Register

AXIAP_CFG_0_ROM_LO_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AXI ROM Address (31:12) .

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Table 14-28491. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 022F8h

Figure 14-9388. AXIAP_CFG_0_ROM_LO_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOWBASE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOWBASE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">LOWBASE</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>FORMAT</td><td>PRESENT</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-28493. AXIAP_CFG_0_ROM_LO_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	LOWBASE	R	0h	Bits 31:12 of the base address
11:2	RESERVED	R	0h	Reserved, returns 0
1	FORMAT	R	0h	Base address register format [0]
0	PRESENT	R	0h	This field indicates whether a debug entry is present for this MEM-AP: 0 No debug entry present 1 Debug entry present

14.11.2.104 AXIAP_CFG_0_ID_REGISTER Register

AXIAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28494. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_0	7000 022FCh

Figure 14-9389. AXIAP_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28496. AXIAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB, 4=AXI [4]

14.11.2.105 PWRAP_CFG_0_CORE_PRECREG0 Register

PWRAP_CFG_0_CORE_PRECREG0 Register (Offset = 0h) [reset = 0h]

Register Description: These registers are used to control functionality of CPUs without JTAG ports. There can be upto 32 of these registers

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Table 14-28497. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pwrap_cfg_0	7000 02300h

Figure 14-9390. PWRAP_CFG_0_CORE_PRECREG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RETENTION	RST_OCCURED	PWR_LOSS_DET	INHIBIT_SLEEP	DEBUG_POWER	UNNAT_RESET	IN_RESET_RLS_WIR	RESET_MODE
R	R/W	R/W	R/W	R/W	R	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESET_MODE		DEBUG_ENABLE	RSV11_12		EXEC_ACTION_DEBUG_ATTEN	RSV8_9	
R/W		R/W	R		R/W	R	
0h		0h	0h		0h	0h	
7	6	5	4	3	2	1	0
PWRDOWNSRD	RSV6	POWERED	CLKDOWNDSRD	FORCE_ACTIVE	CLOCKED	SECURITY	PRESENT
R	R	R	R	R/W	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-28499. PWRAP_CFG_0_CORE_PRECREG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23	RETENTION	R	0h	Core is in retention mode
22	RST_OCCURED	R/W	0h	Sticky bit indicating a reset has occured Write 1 to clear this bit
21	PWR_LOSS_DET	R/W	0h	Power Loss Detected Sticky bit, write a 1 to clear this bit
20	INHIBIT_SLEEP	R/W	0h	Inhinit Sleep Block core from entering sleep mode
19	DEBUG_POWER	R/W	0h	Core debug logic is powered
18	UNNAT_RESET	R	0h	Unnatural Reset Device reset state is being affected by debug logic
17	IN_RESET_RLS_WIR	R/W	0h	Writing a 1 releases the WIR When read this returns the reset status, 1 indicates core is in reset
16:14	RESET_MODE	R/W	0h	Reset Mode 0=normal, 1=WIR, 2=Blk Rst, 3=Blk Assert, 4=Halt on Rst, 5=Cancel, 6=Halt and Block, 7=Halt-Blk-assert
13	DEBUG_ENABLE	R/W	0h	Debug Enabled signal to the core
12:11	RSV11_12	R	0h	Reserved, return 0
10	EXEC_ACTION_DEBUG_ATTEN	R/W	0h	Writing this bit causes Execution Read will return the Debug Attention input value

Table 14-28499. PWRAP_CFG_0_CORE_PRECREG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	RSV8_9	R	0h	Reserved, returns 0 when read
7	PWRDOWNDSRD	R	0h	The core wants to turn off it's power when high
6	RSV6	R	0h	Reserved, returns 0 when read
5	POWERED	R	0h	Core is powered up when high
4	CLKDOWNDSRD	R	0h	The core wants to turn off it's clock when high
3	FORCE_ACTIVE	R/W	0h	Force core active Turn on power and clocks
2	CLOCKED	R	0h	When high the core clock is active
1	SECURITY	R	0h	Security bit When high security is allowing access
0	PRESENT	R	0h	The core controlled by this register exists when 1

14.11.2.106 PWRAP_CFG_0_CORE_PRECREG1 Register

14.11.2.107 PWRAP_CFG_0_CORE_PRECREG2 Register

14.11.2.108 PWRAP_CFG_0_CORE_PRECREG3 Register

14.11.2.109 PWRAP_CFG_0_CORE_PRECREG4 Register

14.11.2.110 PWRAP_CFG_0_CORE_PRECREG5 Register

14.11.2.111 PWRAP_CFG_0_CORE_PRECREG6 Register

14.11.2.112 PWRAP_CFG_0_CORE_PRECREG7 Register

14.11.2.113 PWRAP_CFG_0_CORE_PRECREG8 Register

14.11.2.114 PWRAP_CFG_0_CORE_PRECREG9 Register

14.11.2.115 PWRAP_CFG_0_CORE_PRECREG10 Register

14.11.2.116 PWRAP_CFG_0_CORE_PRECREG11 Register

14.11.2.117 PWRAP_CFG_0_CORE_PRECREG12 Register

14.11.2.118 PWRAP_CFG_0_CORE_PRECREG13 Register

14.11.2.119 PWRAP_CFG_0_CORE_PRECREG14 Register

14.11.2.120 PWRAP_CFG_0_CORE_PRECREG15 Register

14.11.2.121 PWRAP_CFG_0_CORE_PRECREG16 Register

14.11.2.122 PWRAP_CFG_0_CORE_PRECREG17 Register

14.11.2.123 PWRAP_CFG_0_CORE_PRECREG18 Register

14.11.2.124 PWRAP_CFG_0_CORE_PRECREG19 Register

14.11.2.125 PWRAP_CFG_0_CORE_PRECREG20 Register

14.11.2.126 PWRAP_CFG_0_CORE_PRECREG21 Register

14.11.2.127 PWRAP_CFG_0_CORE_PRECREG22 Register

14.11.2.128 PWRAP_CFG_0_CORE_PRECREG23 Register

14.11.2.129 PWRAP_CFG_0_CORE_PRECREG24 Register

14.11.2.130 PWRAP_CFG_0_CORE_PRECREG25 Register

14.11.2.131 PWRAP_CFG_0_CORE_PRECREG26 Register

14.11.2.132 PWRAP_CFG_0_CORE_PRECREG27 Register

14.11.2.133 PWRAP_CFG_0_CORE_PRECREG28 Register

14.11.2.134 PWRAP_CFG_0_CORE_PRECREG29 Register

14.11.2.135 PWRAP_CFG_0_CORE_PRECREG30 Register

14.11.2.136 PWRAP_CFG_0_CORE_PRECREG31 Register

14.11.2.137 PWRAP_CFG_0_SYS_PRECREG Register

PWRAP_CFG_0_SYS_PRECREG Register (Offset = F0h) [reset = 0h]

Register Description: This register is used to control system level functionality

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Table 14-28500. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pwrap_cfg_0	7000 023F0h

Figure 14-9391. PWRAP_CFG_0_SYS_PRECREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED			DBGCON_WE	DBGCON			
R			R/W	R/W			
0h			0h	0h			
15	14	13	12	11	10	9	8
UNNAT_RESET	RST_OCCURED	SYSTEM_STAT	RSV12_BIT	GLOB_EXEC_TRIG	CLR_EX_FLAGS	GLOB_EXEC_MSK	IN_RESET_RLS_WIR
R	R/W	R	R	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
WIR_REQ	BLK_SYS_RST	RESERVED0		DEV_TYPE			SYS_RST_REQ
R/W	R/W	R		R			R/W
0h	0h	0h		0h			0h

Table 14-28502. PWRAP_CFG_0_SYS_PRECREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	R	0h	Reserved, returns 0
20	DBGCON_WE	R/W	0h	This bit must be high to write to the debug connect field
19:16	DBGCON	R/W	0h	The system debugger must write a value of 0x9 to be connected and access the debug logic
15	UNNAT_RESET	R	0h	Unnatural Reset Device reset state is being affected by debug logic
14	RST_OCCURED	R/W	0h	Sticky bit indicating a reset has occured Write 1 to clear this bit
13	SYSTEM_STAT	R	0h	System Status input, application specificall
12	RSV12_BIT	R	0h	Reserved, read returns 0
11	GLOB_EXEC_TRIG	R	0h	
10	CLR_EX_FLAGS	R/W	0h	Clear all run flags
9	GLOB_EXEC_MSK	R/W	0h	Global Execute Mask
8	IN_RESET_RLS_WIR	R/W	0h	Writing a 1 releases the global WIR When read this returns the in reset status
7	WIR_REQ	R/W	0h	Wait In Reset Request
6	BLK_SYS_RST	R/W	0h	Block System Reset
5:4	RESERVED0	R	0h	Reserved0, returns 0
3:1	DEV_TYPE	R	0h	Device Type tieoff value Test, emulator, secure, etc

Table 14-28502. PWRAP_CFG_0_SYS_PRECREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYS_RST_REQ	R/W	0h	System Reset Request This bit will be reset once reset occurs

14.11.2.138 PWRAP_CFG_0_ID_REGISTER Register

PWRAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28503. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pwrap_cfg_0	7000 023FCh

Figure 14-9392. PWRAP_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28505. PWRAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	0h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.11.2.139 PVIEW_CFG_0_PVIEW_STATE0 Register

PVIEW_CFG_0_PVIEW_STATE0 Register (Offset = 0h) [reset = 0h]

Register Description: This register provides the device specific power status. A read of Power View State Register will lock the values for all other Power View State Registers. A read from the last Power View State register will unlock them so they can update

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Table 14-28506. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pview_cfg_0	7000 02400h

Figure 14-9393. PVIEW_CFG_0_PVIEW_STATE0 Name Register

31	30	29	28	27	26	25	24
POWER_VIEW_STATE_REG0							
R							
0h							
23	22	21	20	19	18	17	16
POWER_VIEW_STATE_REG0							
R							
0h							
15	14	13	12	11	10	9	8
POWER_VIEW_STATE_REG0							
R							
0h							
7	6	5	4	3	2	1	0
POWER_VIEW_STATE_REG0							
R							
0h							

Table 14-28508. PVIEW_CFG_0_PVIEW_STATE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POWER_VIEW_STATE_REG0	R	0h	

14.11.2.140 PVIEW_CFG_0_PVIEW_CAPABILITY Register

PVIEW_CFG_0_PVIEW_CAPABILITY Register (Offset = F0h) [reset = 0h]

Register Description: The Capability Register provides information on the number of Power State registers implemented in the AP

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Table 14-28509. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pview_cfg_0	7000 024F0h

Figure 14-9394. PVIEW_CFG_0_PVIEW_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		NUMSTATREG					
R		R					
0h		0h					

Table 14-28511. PVIEW_CFG_0_PVIEW_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved, returns 0
5:0	NUMSTATREG	R	0h	The value read indicates the number of valid Power State Registers that are implemented in the system The maximum number is 60 and the minimum number is 1 The registers are always implemented at contiguous addresses so a value of 7 means that registers 0-6 are valid

14.11.2.141 PVIEW_CFG_0_ID_REGISTER Register

PVIEW_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28512. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pview_cfg_0	7000 024FCh

Figure 14-9395. PVIEW_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28514. PVIEW_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	0h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type = 3

14.11.2.142 JTAGAP_CFG_0_CSW Register

JTAGAP_CFG_0_CSW Register (Offset = 0h) [reset = 0h]

Register Description: This register provides control and status information

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Table 14-28515. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_0	7000 02500h

Figure 14-9396. JTAGAP_CFG_0_CSW Name Register

31	30	29	28	27	26	25	24
SERACTV	WFIFOCNT			RSV27	RFIFOCNT		
R	R			R	R		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				PORT_CONNECTED_STATUS	SRST_STATUS	TRST_ASSERT	SRST_ASSERT
R				R	R	R/W	R/W
0h				0h	0h	0h	0h

Table 14-28517. JTAGAP_CFG_0_CSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SERACTV	R	0h	JTAG Serializer active
30:28	WFIFOCNT	R	0h	Outstanding Write FIFO Byte Count
27	RSV27	R	0h	Reserved, returns 0
26:24	RFIFOCNT	R	0h	Outstanding Read FIFO Byte Count
23:4	RESERVED	R	0h	Reserved, returns 0
3	PORT_CONNECTED_STATUS	R	0h	Reading this returns the Port connected status of the selected port
2	SRST_STATUS	R	0h	Reading this returns the SRST status of the selected port If multiple ports are selected, it is the AND of all the SRSTCONNECTED inputs from the selected ports
1	TRST_ASSERT	R/W	0h	Writing a 1 causes TRST to be asserted
0	SRST_ASSERT	R/W	0h	Writing a 1 causes SRST to be asserted

14.11.2.143 JTAGAP_CFG_0_PSEL_REG Register

JTAGAP_CFG_0_PSEL_REG Register (Offset = 4h) [reset = 0h]

Register Description: This 8-bit register is used to select the JTAG port.

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Table 14-28518. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_0	7000 02504h

Figure 14-9397. JTAGAP_CFG_0_PSEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_SELECT_REGISTER							
R/W							
0h							

Table 14-28520. JTAGAP_CFG_0_PSEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	read as 0
7:0	PORT_SELECT_REGISTER	R/W	0h	

14.11.2.144 JTAGAP_CFG_0_PSTA_REG Register

JTAGAP_CFG_0_PSTA_REG Register (Offset = 8h) [reset = 0h]

Register Description: A bit value of 1 indicates that a selected and enabled port has gone inactive. These bits are sticky. Writing a 1 to them clears them.

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Table 14-28521. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_0	7000 02508h

Figure 14-9398. JTAGAP_CFG_0_PSTA_REG Name Register

31	30	29	28	27	26	25	24
PORT_STATUS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
PORT_STATUS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
PORT_STATUS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_STATUS_REGISTER							
R/W							
0h							

Table 14-28523. JTAGAP_CFG_0_PSTA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_STATUS_REGISTER	R/W	0h	

14.11.2.145 JTAGAP_CFG_0_BYTEFIFO1 Register

JTAGAP_CFG_0_BYTEFIFO1 Register (Offset = 10h) [reset = 0h]

Register Description: Reading this location reads a byte from the FIFO. Writing it loads a byte into the FIFO. Reset value is UNDEFINED

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Table 14-28524. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_0	7000 02510h

Figure 14-9399. JTAGAP_CFG_0_BYTEFIFO1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_1							
R/W							
0h							

Table 14-28526. JTAGAP_CFG_0_BYTEFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	
7:0	BYTE_FIFO_1	R/W	0h	

14.11.2.146 JTAGAP_CFG_0_BYTEFIFO2 Register

JTAGAP_CFG_0_BYTEFIFO2 Register (Offset = 14h) [reset = 0h]

Register Description: Reading this location reads a 16 bits from the FIFO. Writing it loads 16 bits into the FIFO. Reset value is UNDEFINED

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Table 14-28527. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_0	7000 02514h

Figure 14-9400. JTAGAP_CFG_0_BYTEFIFO2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_2							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_2							
R/W							
0h							

Table 14-28529. JTAGAP_CFG_0_BYTEFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	
15:0	BYTE_FIFO_2	R/W	0h	

14.11.2.147 JTAGAP_CFG_0_BYTEFIFO3 Register

JTAGAP_CFG_0_BYTEFIFO3 Register (Offset = 18h) [reset = 0h]

Register Description: Reading this location reads a 24 bits from the FIFO. Writing it loads 24 bits into the FIFO. Reset value is UNDEFINED

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Table 14-28530. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_0	7000 02518h

Figure 14-9401. JTAGAP_CFG_0_BYTEFIFO3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_3							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_3							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_3							
R/W							
0h							

Table 14-28532. JTAGAP_CFG_0_BYTEFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R/W	0h	
23:0	BYTE_FIFO_3	R/W	0h	

14.11.2.148 JTAGAP_CFG_0_BYTEFIFO4 Register

JTAGAP_CFG_0_BYTEFIFO4 Register (Offset = 1Ch) [reset = 0h]

Register Description: Reading this location reads a 32 bits from the FIFO. Writing it loads 32 bits into the FIFO. Reset value is UNDEFINED

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Table 14-28533. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_0	7000 0251Ch

Figure 14-9402. JTAGAP_CFG_0_BYTEFIFO4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BYTE_FIFO_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BYTE_FIFO_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BYTE_FIFO_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTE_FIFO_4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28535. JTAGAP_CFG_0_BYTEFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BYTE_FIFO_4	R/W	0h	

14.11.2.149 JTAGAP_CFG_0_ID_REGISTER Register

JTAGAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28536. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_0	7000 025FCh

Figure 14-9403. JTAGAP_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			

23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h

15	14	13	12	11	10	9	8
SPARE							
R							
0h							

7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28538. JTAGAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [1]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [0]

14.11.2.150 SECAP_CFG_0_TXDATA Register

SECAP_CFG_0_TXDATA Register (Offset = 0h) [reset = 0h]

Register Description: Data value to send to security controller. Apllication specific

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Table 14-28539. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_secap_cfg_0	7000 02600h

Figure 14-9404. SECAP_CFG_0_TXDATA Name Register

31	30	29	28	27	26	25	24
TX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_DATA_REGISTER							
R/W							
0h							

Table 14-28541. SECAP_CFG_0_TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TX_DATA_REGISTER	R/W	0h	

14.11.2.151 SECAP_CFG_0_TXCTRL Register

SECAP_CFG_0_TXCTRL Register (Offset = 4h) [reset = 0h]

Register Description: Register to send control information to the Security Controller, Application specific

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Table 14-28542. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_secap_cfg_0	7000 02604h

Figure 14-9405. SECAP_CFG_0_TXCTRL Name Register

31	30	29	28	27	26	25	24
TX_CONTROL							
R/W							
0h							
23	22	21	20	19	18	17	16
TX_CONTROL							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_CONTROL							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_CONTROL							TXDAV
R/W							R
0h							0h

Table 14-28544. SECAP_CFG_0_TXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	TX_CONTROL	R/W	0h	31 bits to send to security controller, Application specific
0	TXDAV	R	0h	TX Data Available

14.11.2.152 SECAP_CFG_0_RXDATA Register

SECAP_CFG_0_RXDATA Register (Offset = 8h) [reset = 0h]

Register Description: Data value from the security controller. Apllication specific

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Table 14-28545. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_secap_cfg_0	7000 02608h

Figure 14-9406. SECAP_CFG_0_RXDATA Name Register

31	30	29	28	27	26	25	24
RX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
RX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_DATA_REGISTER							
R/W							
0h							

Table 14-28547. SECAP_CFG_0_RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RX_DATA_REGISTER	R/W	0h	

14.11.2.153 SECAP_CFG_0_RXCTRL Register

SECAP_CFG_0_RXCTRL Register (Offset = Ch) [reset = 0h]

Register Description: Register to receive control information from the Security Controller

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Table 14-28548. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_secap_cfg_0	7000 0260Ch

Figure 14-9407. SECAP_CFG_0_RXCTRL Name Register

31	30	29	28	27	26	25	24
RX_CONTROL							
R							
0h							
23	22	21	20	19	18	17	16
RX_CONTROL							
R							
0h							
15	14	13	12	11	10	9	8
RX_CONTROL							
R							
0h							
7	6	5	4	3	2	1	0
RX_CONTROL							RXDAV
R							R
0h							0h

Table 14-28550. SECAP_CFG_0_RXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RX_CONTROL	R	0h	31 bits from the security controller, Application specific
0	RXDAV	R	0h	TX Data Available

14.11.2.154 CORTEX0_CFG_0_CSWREG Register

CORTEX0_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28551. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_0	7000 02700h

Figure 14-9408. CORTEX0_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28553. CORTEX0_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.155 CORTEX0_CFG_0_TAREG Register

14.11.2.156 CORTEX0_CFG_0_DRWREG Register

CORTEX0_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28554. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_0	7000 0270Ch

Figure 14-9409. CORTEX0_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28556. CORTEX0_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.157 CORTEX0_CFG_0_BD0REG Register

CORTEX0_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28557. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_0	7000 02710h

Figure 14-9410. CORTEX0_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28559. CORTEX0_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.158 CORTEX0_CFG_0_BD1REG Register

CORTEX0_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28560. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_0	7000 02714h

Figure 14-9411. CORTEX0_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28562. CORTEX0_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.159 CORTEX0_CFG_0_BD2REG Register

CORTEX0_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28563. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_0	7000 02718h

Figure 14-9412. CORTEX0_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28565. CORTEX0_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.160 CORTEX0_CFG_0_BD3REG Register

CORTEX0_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28566. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_0	7000 0271Ch

Figure 14-9413. CORTEX0_CFG_0_BD3REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_3_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_3_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_3_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_3_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28568. CORTEX0_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.161 CORTEX0_CFG_0_ROM_REGISTER Register

CORTEX0_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28569. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_0	7000 027F8h

Figure 14-9414. CORTEX0_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28571. CORTEX0_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.162 CORTEX0_CFG_0_ID_REGISTER Register

CORTEX0_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28572. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_0	7000 027FCh

Figure 14-9415. CORTEX0_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28574. CORTEX0_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.163 CORTEX1_CFG_0_CSWREG Register

CORTEX1_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28575. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_0	7000 02800h

Figure 14-9416. CORTEX1_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28577. CORTEX1_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.164 CORTEX1_CFG_0_TAREG Register

14.11.2.165 CORTEX1_CFG_0_DRWREG Register

CORTEX1_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28578. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_0	7000 0280Ch

Figure 14-9417. CORTEX1_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28580. CORTEX1_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.166 CORTEX1_CFG_0_BD0REG Register

CORTEX1_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28581. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_0	7000 02810h

Figure 14-9418. CORTEX1_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28583. CORTEX1_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.167 CORTEX1_CFG_0_BD1REG Register

CORTEX1_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28584. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_0	7000 02814h

Figure 14-9419. CORTEX1_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28586. CORTEX1_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.168 CORTEX1_CFG_0_BD2REG Register

CORTEX1_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28587. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_0	7000 02818h

Figure 14-9420. CORTEX1_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28589. CORTEX1_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.169 CORTEX1_CFG_0_BD3REG Register

CORTEX1_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28590. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_0	7000 0281Ch

Figure 14-9421. CORTEX1_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28592. CORTEX1_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.170 CORTEX1_CFG_0_ROM_REGISTER Register

CORTEX1_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28593. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_0	7000 028F8h

Figure 14-9422. CORTEX1_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28595. CORTEX1_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.171 CORTEX1_CFG_0_ID_REGISTER Register

CORTEX1_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28596. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_0	7000 028FCh

Figure 14-9423. CORTEX1_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28598. CORTEX1_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.172 CORTEX2_CFG_0_CSWREG Register

CORTEX2_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28599. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_0	7000 02900h

Figure 14-9424. CORTEX2_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28601. CORTEX2_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.173 CORTEX2_CFG_0_TAREG Register

14.11.2.174 CORTEX2_CFG_0_DRWREG Register

CORTEX2_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28602. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_0	7000 0290Ch

Figure 14-9425. CORTEX2_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28604. CORTEX2_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.175 CORTEX2_CFG_0_BD0REG Register

CORTEX2_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28605. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_0	7000 02910h

Figure 14-9426. CORTEX2_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28607. CORTEX2_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.176 CORTEX2_CFG_0_BD1REG Register

CORTEX2_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28608. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_0	7000 02914h

Figure 14-9427. CORTEX2_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28610. CORTEX2_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.177 CORTEX2_CFG_0_BD2REG Register

CORTEX2_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28611. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_0	7000 02918h

Figure 14-9428. CORTEX2_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28613. CORTEX2_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.178 CORTEX2_CFG_0_BD3REG Register

CORTEX2_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28614. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_0	7000 0291Ch

Figure 14-9429. CORTEX2_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28616. CORTEX2_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.179 CORTEX2_CFG_0_ROM_REGISTER Register

CORTEX2_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28617. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_0	7000 029F8h

Figure 14-9430. CORTEX2_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28619. CORTEX2_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.180 CORTEX2_CFG_0_ID_REGISTER Register

CORTEX2_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28620. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_0	7000 029FCh

Figure 14-9431. CORTEX2_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28622. CORTEX2_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.181 CORTEX3_CFG_0_CSWREG Register

CORTEX3_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28623. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_0	7000 02A00h

Figure 14-9432. CORTEX3_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28625. CORTEX3_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.182 CORTEX3_CFG_0_TAREG Register

14.11.2.183 CORTEX3_CFG_0_DRWREG Register

CORTEX3_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28626. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_0	7000 02A0Ch

Figure 14-9433. CORTEX3_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28628. CORTEX3_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.184 CORTEX3_CFG_0_BD0REG Register

CORTEX3_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28629. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_0	7000 02A10h

Figure 14-9434. CORTEX3_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28631. CORTEX3_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.185 CORTEX3_CFG_0_BD1REG Register

CORTEX3_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28632. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_0	7000 02A14h

Figure 14-9435. CORTEX3_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28634. CORTEX3_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.186 CORTEX3_CFG_0_BD2REG Register

CORTEX3_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28635. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_0	7000 02A18h

Figure 14-9436. CORTEX3_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28637. CORTEX3_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.187 CORTEX3_CFG_0_BD3REG Register

CORTEX3_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28638. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_0	7000 02A1Ch

Figure 14-9437. CORTEX3_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28640. CORTEX3_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.188 CORTEX3_CFG_0_ROM_REGISTER Register

CORTEX3_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28641. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_0	7000 02AF8h

Figure 14-9438. CORTEX3_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28643. CORTEX3_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.189 CORTEX3_CFG_0_ID_REGISTER Register

CORTEX3_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28644. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_0	7000 02AFCh

Figure 14-9439. CORTEX3_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28646. CORTEX3_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.190 CORTEX4_CFG_0_CSWREG Register

CORTEX4_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28647. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_0	7000 02B00h

Figure 14-9440. CORTEX4_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28649. CORTEX4_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.191 CORTEX4_CFG_0_TAREG Register

14.11.2.192 CORTEX4_CFG_0_DRWREG Register

CORTEX4_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28650. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_0	7000 02B0Ch

Figure 14-9441. CORTEX4_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28652. CORTEX4_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.193 CORTEX4_CFG_0_BD0REG Register

CORTEX4_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28653. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_0	7000 02B10h

Figure 14-9442. CORTEX4_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28655. CORTEX4_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.194 CORTEX4_CFG_0_BD1REG Register

CORTEX4_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28656. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_0	7000 02B14h

Figure 14-9443. CORTEX4_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28658. CORTEX4_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.195 CORTEX4_CFG_0_BD2REG Register

CORTEX4_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28659. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_0	7000 02B18h

Figure 14-9444. CORTEX4_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28661. CORTEX4_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.196 CORTEX4_CFG_0_BD3REG Register

CORTEX4_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28662. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_0	7000 02B1Ch

Figure 14-9445. CORTEX4_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28664. CORTEX4_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.197 CORTEX4_CFG_0_ROM_REGISTER Register

CORTEX4_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28665. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_0	7000 02BF8h

Figure 14-9446. CORTEX4_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28667. CORTEX4_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.198 CORTEX4_CFG_0_ID_REGISTER Register

CORTEX4_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28668. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_0	7000 02BFCh

Figure 14-9447. CORTEX4_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28670. CORTEX4_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.199 CORTEX5_CFG_0_CSWREG Register

CORTEX5_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28671. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_0	7000 02C00h

Figure 14-9448. CORTEX5_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28673. CORTEX5_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.200 CORTEX5_CFG_0_TAREG Register

14.11.2.201 CORTEX5_CFG_0_DRWREG Register

CORTEX5_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28674. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_0	7000 02C0Ch

Figure 14-9449. CORTEX5_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28676. CORTEX5_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.202 CORTEX5_CFG_0_BD0REG Register

CORTEX5_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28677. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_0	7000 02C10h

Figure 14-9450. CORTEX5_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28679. CORTEX5_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.203 CORTEX5_CFG_0_BD1REG Register

CORTEX5_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28680. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_0	7000 02C14h

Figure 14-9451. CORTEX5_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28682. CORTEX5_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.204 CORTEX5_CFG_0_BD2REG Register

CORTEX5_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28683. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_0	7000 02C18h

Figure 14-9452. CORTEX5_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28685. CORTEX5_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.205 CORTEX5_CFG_0_BD3REG Register

CORTEX5_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28686. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_0	7000 02C1Ch

Figure 14-9453. CORTEX5_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28688. CORTEX5_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.206 CORTEX5_CFG_0_ROM_REGISTER Register

CORTEX5_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28689. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_0	7000 02CF8h

Figure 14-9454. CORTEX5_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28691. CORTEX5_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.207 CORTEX5_CFG_0_ID_REGISTER Register

CORTEX5_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28692. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_0	7000 02CFCh

Figure 14-9455. CORTEX5_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28694. CORTEX5_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.208 CORTEX6_CFG_0_CSWREG Register

CORTEX6_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28695. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_0	7000 02D00h

Figure 14-9456. CORTEX6_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28697. CORTEX6_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.209 CORTEX6_CFG_0_TAREG Register

14.11.2.210 CORTEX6_CFG_0_DRWREG Register

CORTEX6_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28698. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_0	7000 02D0Ch

Figure 14-9457. CORTEX6_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28700. CORTEX6_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.211 CORTEX6_CFG_0_BD0REG Register

CORTEX6_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28701. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_0	7000 02D10h

Figure 14-9458. CORTEX6_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28703. CORTEX6_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.212 CORTEX6_CFG_0_BD1REG Register

CORTEX6_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28704. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_0	7000 02D14h

Figure 14-9459. CORTEX6_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28706. CORTEX6_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.213 CORTEX6_CFG_0_BD2REG Register

CORTEX6_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28707. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_0	7000 02D18h

Figure 14-9460. CORTEX6_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28709. CORTEX6_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.214 CORTEX6_CFG_0_BD3REG Register

CORTEX6_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28710. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_0	7000 02D1Ch

Figure 14-9461. CORTEX6_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28712. CORTEX6_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.215 CORTEX6_CFG_0_ROM_REGISTER Register

CORTEX6_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28713. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_0	7000 02DF8h

Figure 14-9462. CORTEX6_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28715. CORTEX6_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.216 CORTEX6_CFG_0_ID_REGISTER Register

CORTEX6_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28716. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_0	7000 02DFCh

Figure 14-9463. CORTEX6_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28718. CORTEX6_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.217 CORTEX7_CFG_0_CSWREG Register

CORTEX7_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28719. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_0	7000 02E00h

Figure 14-9464. CORTEX7_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28721. CORTEX7_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.218 CORTEX7_CFG_0_TAREG Register

14.11.2.219 CORTEX7_CFG_0_DRWREG Register

CORTEX7_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28722. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_0	7000 02E0Ch

Figure 14-9465. CORTEX7_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28724. CORTEX7_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.220 CORTEX7_CFG_0_BD0REG Register

CORTEX7_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28725. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_0	7000 02E10h

Figure 14-9466. CORTEX7_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28727. CORTEX7_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.221 CORTEX7_CFG_0_BD1REG Register

CORTEX7_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28728. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_0	7000 02E14h

Figure 14-9467. CORTEX7_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28730. CORTEX7_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.222 CORTEX7_CFG_0_BD2REG Register

CORTEX7_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28731. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_0	7000 02E18h

Figure 14-9468. CORTEX7_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28733. CORTEX7_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.223 CORTEX7_CFG_0_BD3REG Register

CORTEX7_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28734. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_0	7000 02E1Ch

Figure 14-9469. CORTEX7_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28736. CORTEX7_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.224 CORTEX7_CFG_0_ROM_REGISTER Register

CORTEX7_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28737. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_0	7000 02EF8h

Figure 14-9470. CORTEX7_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28739. CORTEX7_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.225 CORTEX7_CFG_0_ID_REGISTER Register

CORTEX7_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28740. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_0	7000 02EFCh

Figure 14-9471. CORTEX7_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28742. CORTEX7_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.226 CORTEX8_CFG_0_CSWREG Register

CORTEX8_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-28743. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_0	7000 02F00h

Figure 14-9472. CORTEX8_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-28745. CORTEX8_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.227 CORTEX8_CFG_0_TAREG Register

14.11.2.228 CORTEX8_CFG_0_DRWREG Register

CORTEX8_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-28746. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_0	7000 02F0Ch

Figure 14-9473. CORTEX8_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-28748. CORTEX8_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.229 CORTEX8_CFG_0_BD0REG Register

CORTEX8_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28749. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_0	7000 02F10h

Figure 14-9474. CORTEX8_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-28751. CORTEX8_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.230 CORTEX8_CFG_0_BD1REG Register

CORTEX8_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28752. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_0	7000 02F14h

Figure 14-9475. CORTEX8_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-28754. CORTEX8_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.231 CORTEX8_CFG_0_BD2REG Register

CORTEX8_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28755. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_0	7000 02F18h

Figure 14-9476. CORTEX8_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-28757. CORTEX8_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.232 CORTEX8_CFG_0_BD3REG Register

CORTEX8_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-28758. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_0	7000 02F1Ch

Figure 14-9477. CORTEX8_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-28760. CORTEX8_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.233 CORTEX8_CFG_0_ROM_REGISTER Register

CORTEX8_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-28761. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_0	7000 02FF8h

Figure 14-9478. CORTEX8_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-28763. CORTEX8_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.234 CORTEX8_CFG_0_ID_REGISTER Register

CORTEX8_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-28764. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_0	7000 02FFCh

Figure 14-9479. CORTEX8_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-28766. CORTEX8_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.235 ROM_TABLE_1_0_ROM_ENTRY0 Register

ROM_TABLE_1_0_ROM_ENTRY0 Register (Offset = 0h) [reset = 1003h]

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Table 14-28767. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00000h

Figure 14-9480. ROM_TABLE_1_0_ROM_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-28769. ROM_TABLE_1_0_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.236 ROM_TABLE_1_0_ROM_ENTRY1 Register

ROM_TABLE_1_0_ROM_ENTRY1 Register (Offset = 4h) [reset = 2003h]

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Table 14-28770. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00004h

Figure 14-9481. ROM_TABLE_1_0_ROM_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">2h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">2h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-28772. ROM_TABLE_1_0_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.237 ROM_TABLE_1_0_ROM_ENTRY2 Register

ROM_TABLE_1_0_ROM_ENTRY2 Register (Offset = 8h) [reset = 3003h]

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Table 14-28773. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00008h

Figure 14-9482. ROM_TABLE_1_0_ROM_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	3h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
3h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
3h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-28775. ROM_TABLE_1_0_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	3h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.238 ROM_TABLE_1_0_ROM_ENTRY3 Register

ROM_TABLE_1_0_ROM_ENTRY3 Register (Offset = Ch) [reset = 4003h]

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Table 14-28776. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 0000Ch

Figure 14-9483. ROM_TABLE_1_0_ROM_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	4h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
4h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-28778. ROM_TABLE_1_0_ROM_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	4h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.239 ROM_TABLE_1_0_ROM_ENTRY4 Register

ROM_TABLE_1_0_ROM_ENTRY4 Register (Offset = 10h) [reset = 5003h]

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Table 14-28779. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00010h

Figure 14-9484. ROM_TABLE_1_0_ROM_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	5h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
5h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
5h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-28781. ROM_TABLE_1_0_ROM_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	5h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.240 ROM_TABLE_1_0_ROM_ENTRY5 Register

ROM_TABLE_1_0_ROM_ENTRY5 Register (Offset = 14h) [reset = 1000003h]

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Table 14-28782. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00014h

Figure 14-9485. ROM_TABLE_1_0_ROM_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-28784. ROM_TABLE_1_0_ROM_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.241 ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register

ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register (Offset = 18h) [reset = 1000002h]

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Table 14-28785. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00018h

Figure 14-9486. ROM_TABLE_1_0_COMPUTE_CLUSTER0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28787. ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.242 ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register

ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register (Offset = 1Ch) [reset = 1400002h]

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Table 14-28788. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 0001Ch

Figure 14-9487. ROM_TABLE_1_0_COMPUTE_CLUSTER1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1400h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1400h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1400h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28790. ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1400h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.243 ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register

ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register (Offset = 20h) [reset = 1800002h]

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Table 14-28791. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00020h

Figure 14-9488. ROM_TABLE_1_0_COMPUTE_CLUSTER2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1800h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1800h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1800h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28793. ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1800h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.244 ROM_TABLE_1_0_DEBUG_CELL0 Register

ROM_TABLE_1_0_DEBUG_CELL0 Register (Offset = 24h) [reset = 1C00002h]

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Table 14-28794. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00024h

Figure 14-9489. ROM_TABLE_1_0_DEBUG_CELL0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C00h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C00h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28796. ROM_TABLE_1_0_DEBUG_CELL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.245 ROM_TABLE_1_0_DEBUG_CELL1 Register

ROM_TABLE_1_0_DEBUG_CELL1 Register (Offset = 28h) [reset = 1C10002h]

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Table 14-28797. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00028h

Figure 14-9490. ROM_TABLE_1_0_DEBUG_CELL1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C10h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
1C10h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C10h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28799. ROM_TABLE_1_0_DEBUG_CELL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.246 ROM_TABLE_1_0_DEBUG_CELL2 Register

ROM_TABLE_1_0_DEBUG_CELL2 Register (Offset = 2Ch) [reset = 1C20002h]

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Table 14-28800. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 0002Ch

Figure 14-9491. ROM_TABLE_1_0_DEBUG_CELL2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C20h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C20h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C20h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28802. ROM_TABLE_1_0_DEBUG_CELL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.247 ROM_TABLE_1_0_DEBUG_CELL3 Register

ROM_TABLE_1_0_DEBUG_CELL3 Register (Offset = 30h) [reset = 1C30002h]

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Table 14-28803. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00030h

Figure 14-9492. ROM_TABLE_1_0_DEBUG_CELL3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C30h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C30h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C30h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28805. ROM_TABLE_1_0_DEBUG_CELL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.248 ROM_TABLE_1_0_DEBUG_CELL4 Register

ROM_TABLE_1_0_DEBUG_CELL4 Register (Offset = 34h) [reset = 1C40002h]

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Table 14-28806. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00034h

Figure 14-9493. ROM_TABLE_1_0_DEBUG_CELL4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C40h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C40h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28808. ROM_TABLE_1_0_DEBUG_CELL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.249 ROM_TABLE_1_0_DEBUG_CELL5 Register

ROM_TABLE_1_0_DEBUG_CELL5 Register (Offset = 38h) [reset = 1C50002h]

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Table 14-28809. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00038h

Figure 14-9494. ROM_TABLE_1_0_DEBUG_CELL5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C50h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C50h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C50h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28811. ROM_TABLE_1_0_DEBUG_CELL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.250 ROM_TABLE_1_0_DEBUG_CELL6 Register

ROM_TABLE_1_0_DEBUG_CELL6 Register (Offset = 3Ch) [reset = 1C60002h]

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Table 14-28812. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 0003Ch

Figure 14-9495. ROM_TABLE_1_0_DEBUG_CELL6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C60h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C60h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C60h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28814. ROM_TABLE_1_0_DEBUG_CELL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.251 ROM_TABLE_1_0_DEBUG_CELL7 Register

ROM_TABLE_1_0_DEBUG_CELL7 Register (Offset = 40h) [reset = 1C70002h]

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Table 14-28815. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00040h

Figure 14-9496. ROM_TABLE_1_0_DEBUG_CELL7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C70h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C70h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C70h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28817. ROM_TABLE_1_0_DEBUG_CELL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.252 ROM_TABLE_1_0_DEBUG_CELL8 Register

ROM_TABLE_1_0_DEBUG_CELL8 Register (Offset = 44h) [reset = 1C80002h]

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Table 14-28818. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00044h

Figure 14-9497. ROM_TABLE_1_0_DEBUG_CELL8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C80h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C80h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C80h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28820. ROM_TABLE_1_0_DEBUG_CELL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.253 ROM_TABLE_1_0_DEBUG_CELL9 Register

ROM_TABLE_1_0_DEBUG_CELL9 Register (Offset = 48h) [reset = 1C90002h]

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Table 14-28821. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00048h

Figure 14-9498. ROM_TABLE_1_0_DEBUG_CELL9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C90h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C90h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C90h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28823. ROM_TABLE_1_0_DEBUG_CELL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.254 ROM_TABLE_1_0_DEBUG_CELL10 Register

ROM_TABLE_1_0_DEBUG_CELL10 Register (Offset = 4Ch) [reset = 1CA0002h]

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Table 14-28824. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 0004Ch

Figure 14-9499. ROM_TABLE_1_0_DEBUG_CELL10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1CA0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1CA0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1CA0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-28826. ROM_TABLE_1_0_DEBUG_CELL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.255 ROM_TABLE_1_0_DEBUG_CELL11 Register

ROM_TABLE_1_0_DEBUG_CELL11 Register (Offset = 50h) [reset = 1CB0002h]

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Table 14-28827. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00050h

Figure 14-9500. ROM_TABLE_1_0_DEBUG_CELL11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1CB0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1CB0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1CB0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28829. ROM_TABLE_1_0_DEBUG_CELL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.256 ROM_TABLE_1_0_EXTCSCOMP0 Register

ROM_TABLE_1_0_EXTCSCOMP0 Register (Offset = 50h) [reset = 1D00002h]

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Table 14-28830. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00050h

Figure 14-9501. ROM_TABLE_1_0_EXTCSCOMP0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D00h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D00h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D00h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28832. ROM_TABLE_1_0_EXTCSCOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.257 ROM_TABLE_1_0_EXTCSCOMP1 Register

ROM_TABLE_1_0_EXTCSCOMP1 Register (Offset = 54h) [reset = 1D10002h]

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Table 14-28833. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00054h

Figure 14-9502. ROM_TABLE_1_0_EXTCSCOMP1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D10h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D10h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28835. ROM_TABLE_1_0_EXTCSCOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.258 ROM_TABLE_1_0_EXTCSCOMP2 Register

ROM_TABLE_1_0_EXTCSCOMP2 Register (Offset = 58h) [reset = 1D20002h]

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Table 14-28836. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00058h

Figure 14-9503. ROM_TABLE_1_0_EXTCSCOMP2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D20h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D20h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D20h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28838. ROM_TABLE_1_0_EXTCSCOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.259 ROM_TABLE_1_0_EXTCSCOMP3 Register

ROM_TABLE_1_0_EXTCSCOMP3 Register (Offset = 5Ch) [reset = 1D30002h]

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Table 14-28839. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 0005Ch

Figure 14-9504. ROM_TABLE_1_0_EXTCSCOMP3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D30h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D30h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D30h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-28841. ROM_TABLE_1_0_EXTCSCOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.260 ROM_TABLE_1_0_EXTCSCOMP4 Register

ROM_TABLE_1_0_EXTCSCOMP4 Register (Offset = 60h) [reset = 1D40002h]

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Table 14-28842. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00060h

Figure 14-9505. ROM_TABLE_1_0_EXTCSCOMP4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D40h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D40h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D40h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28844. ROM_TABLE_1_0_EXTCSCOMP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.261 ROM_TABLE_1_0_EXTCSCOMP5 Register

ROM_TABLE_1_0_EXTCSCOMP5 Register (Offset = 64h) [reset = 1D50002h]

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Table 14-28845. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00064h

Figure 14-9506. ROM_TABLE_1_0_EXTCSCOMP5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D50h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D50h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D50h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28847. ROM_TABLE_1_0_EXTCSCOMP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.262 ROM_TABLE_1_0_EXTCSCOMP6 Register

ROM_TABLE_1_0_EXTCSCOMP6 Register (Offset = 68h) [reset = 1D60002h]

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Table 14-28848. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00068h

Figure 14-9507. ROM_TABLE_1_0_EXTCSCOMP6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D60h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D60h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D60h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28850. ROM_TABLE_1_0_EXTCSCOMP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.263 ROM_TABLE_1_0_EXTCSCOMP7 Register

ROM_TABLE_1_0_EXTCSCOMP7 Register (Offset = 6Ch) [reset = 1D70002h]

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Table 14-28851. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 0006Ch

Figure 14-9508. ROM_TABLE_1_0_EXTCSCOMP7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D70h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D70h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D70h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28853. ROM_TABLE_1_0_EXTCSCOMP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.264 ROM_TABLE_1_0_EXTCSCOMP8 Register

ROM_TABLE_1_0_EXTCSCOMP8 Register (Offset = 70h) [reset = 1D80002h]

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Table 14-28854. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00070h

Figure 14-9509. ROM_TABLE_1_0_EXTCSCOMP8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D80h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D80h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D80h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28856. ROM_TABLE_1_0_EXTCSCOMP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.265 ROM_TABLE_1_0_EXTCSCOMP9 Register

ROM_TABLE_1_0_EXTCSCOMP9 Register (Offset = 74h) [reset = 1D90002h]

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Table 14-28857. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00074h

Figure 14-9510. ROM_TABLE_1_0_EXTCSCOMP9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D90h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D90h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D90h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28859. ROM_TABLE_1_0_EXTCSCOMP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.266 ROM_TABLE_1_0_EXTCSCOMP10 Register

ROM_TABLE_1_0_EXTCSCOMP10 Register (Offset = 78h) [reset = 1DA0002h]

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Table 14-28860. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 00078h

Figure 14-9511. ROM_TABLE_1_0_EXTCSCOMP10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1DA0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1DA0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1DA0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28862. ROM_TABLE_1_0_EXTCSCOMP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.267 ROM_TABLE_1_0_EXTCSCOMP11 Register

ROM_TABLE_1_0_EXTCSCOMP11 Register (Offset = 7Ch) [reset = 1DB0002h]

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Table 14-28863. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_0	7200 0007Ch

Figure 14-9512. ROM_TABLE_1_0_EXTCSCOMP11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1DB0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1DB0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1DB0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-28865. ROM_TABLE_1_0_EXTCSCOMP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.268 CSCTI_CTICONTROL Register

CSCTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

Register Description: CTI Control Register.

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Table 14-28866. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01000h

Figure 14-9513. CSCTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
R							R/W
0h							0h

Table 14-28868. CSCTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	GLBEN	R/W	0h	Enables or disables the Embedded Cross Trigger, 1=enabled

14.11.2.269 CSCTI_CTIINTACK Register

CSCTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

Register Description: CTI Interrupt Acknowledge Register.

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Table 14-28869. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01010h

Figure 14-9514. CSCTI_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-28871. CSCTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INTACK	R/W	0h	Acknowledges the corresponding CTITRIGOUT output Write 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW There is one bit of the register for each CTITRIGOUT output

14.11.2.270 CSCTI_CTIAPPSET Register

CSCTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

Register Description: CTI Application Trigger Set Register.

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Table 14-28872. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01014h

Figure 14-9515. CSCTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				APPSET			
R				R/W			
0h				0h			

Table 14-28874. CSCTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPSET	R/W	0h	The CTI Application Trigger Set Register is read/write A write to this register causes a channel event to be raised, corresponding to the bit written to

14.11.2.271 CSCTI_CTIAPPCLR Register

CSCTI_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

Register Description: CTI Application Trigger Clear Register.

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Table 14-28875. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01018h

Figure 14-9516. CSCTI_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				APPCLR			
R				R/W			
0h				0h			

Table 14-28877. CSCTI_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPCLR	R/W	0h	The CTI Application Trigger Clear Register is write-only A write to this register causes a channel event to be cleared, corresponding to the bit written to

14.11.2.272 CSCTI_CTIAPPPULSE Register

CSCTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

Register Description: CTI Application Trigger Pulse Register.

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Table 14-28878. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 0101Ch

Figure 14-9517. CSCTI_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPPULSE			
R				R/W			
0h				0h			

Table 14-28880. CSCTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPPULSE	R/W	0h	The CTI Application Pulse Register is write-only A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to This register clears itself immediately

14.11.2.273 CSCTI_CTIINEN0 Register

CSCTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

Register Description: CTI Application Trigger to Channel Enable Register 0

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Table 14-28881. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01020h

Figure 14-9518. CSCTI_CTIINEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-28883. CSCTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.11.2.274 CSCTI_CTIINEN1 Register

CSCTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

Register Description: CTI Application Trigger to Channel Enable Register 1

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Table 14-28884. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01024h

Figure 14-9519. CSCTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	TRIGINEN		
R				NONE	R/W		
0h				0h	0h		

Table 14-28886. CSCTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.11.2.275 CSCTI_CTIINEN2 Register

CSCTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

Register Description: CTI Application Trigger to Channel Enable Register 2

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Table 14-28887. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01028h

Figure 14-9520. CSCTI_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-28889. CSCTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.11.2.276 CSCTI_CTIINEN3 Register

CSCTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

Register Description: CTI Application Trigger to Channel Enable Register 3

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Table 14-28890. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 0102Ch

Figure 14-9521. CSCTI_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-28892. CSCTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.11.2.277 CSCTI_CTIINEN4 Register

CSCTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

Register Description: CTI Application Trigger to Channel Enable Register 4

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Table 14-28893. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01030h

Figure 14-9522. CSCTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-28895. CSCTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.11.2.278 CSCTI_CTIINEN5 Register

CSCTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

Register Description: CTI Application Trigger to Channel Enable Register 5

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Table 14-28896. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01034h

Figure 14-9523. CSCTI_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-28898. CSCTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.11.2.279 CSCTI_CTIINEN6 Register

CSCTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

Register Description: CTI Application Trigger to Channel Enable Register 6

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Table 14-28899. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01038h

Figure 14-9524. CSCTI_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-28901. CSCTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.11.2.280 CSCTI_CTIINEN7 Register

CSCTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

Register Description: CTI Application Trigger to Channel Enable Register 7

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Table 14-28902. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 0103Ch

Figure 14-9525. CSCTI_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-28904. CSCTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.11.2.281 CSCTI_CTIOUTEN0 Register

CSCTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

Register Description: CTI Channel to Trigger Enable Register 0

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Table 14-28905. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 010A0h

Figure 14-9526. CSCTI_CTIOUTEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28907. CSCTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.11.2.282 CSCTI_CTIOUTEN1 Register

CSCTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

Register Description: CTI Channel to Trigger Enable Register 1

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Table 14-28908. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 010A4h

Figure 14-9527. CSCTI_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-28910. CSCTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.11.2.283 CSCTI_CTIOUTEN2 Register

CSCTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

Register Description: CTI Channel to Trigger Enable Register 2

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Table 14-28911. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 010A8h

Figure 14-9528. CSCTI_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-28913. CSCTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.11.2.284 CSCTI_CTIOUTEN3 Register

CSCTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

Register Description: CTI Channel to Trigger Enable Register 3

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Table 14-28914. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 010ACh

Figure 14-9529. CSCTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-28916. CSCTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.11.2.285 CSCTI_CTIOUTEN4 Register

CSCTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

Register Description: CTI Channel to Trigger Enable Register 4

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Table 14-28917. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 010B0h

Figure 14-9530. CSCTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-28919. CSCTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.11.2.286 CSCTI_CTIOUTEN5 Register

CSCTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

Register Description: CTI Channel to Trigger Enable Register 5

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Table 14-28920. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 010B4h

Figure 14-9531. CSCTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-28922. CSCTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.11.2.287 CSCTI_CTIOUTEN6 Register

CSCTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

Register Description: CTI Channel to Trigger Enable Register 6

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Table 14-28923. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 010B8h

Figure 14-9532. CSCTI_CTIOUTEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28925. CSCTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.11.2.288 CSCTI_CTIOUTEN7 Register

CSCTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

Register Description: CTI Channel to Trigger Enable Register 7

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Table 14-28926. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 010BCh

Figure 14-9533. CSCTI_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-28928. CSCTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.11.2.289 CSCTI_CTITRIGINSTATUS Register

CSCTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

Register Description: CTI Trigger In Status Register

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Table 14-28929. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01130h

Figure 14-9534. CSCTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-28931. CSCTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGINSTATUS	R	0h	Shows the status of the CTITRIGIN inputs: 1=CTITRIGIN is active, 0=CTITRIGIN is inactive

14.11.2.290 CSCTI_CTITRIGOUTSTATUS Register

CSCTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

Register Description: CTI Trigger Out Status Register

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Table 14-28932. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01134h

Figure 14-9535. CSCTI_CTITRIGOUTSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TRIGOUTSTATUS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-28934. CSCTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the CTITRIGOUT outputs: 1=CTITRIGOUT is active, 0=CTITRIGOUT is inactive

14.11.2.291 CSCTI_CTICHINSTATUS Register

CSCTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

Register Description: CTI Channel In Status Register

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Table 14-28935. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01138h

Figure 14-9536. CSCTI_CTICHINSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CHINSTATUS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28937. CSCTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHINSTATUS	R	0h	Shows the status of the CTICHIN inputs: 1=CTICHIN is active, 0=CTICHIN is inactive

14.11.2.292 CSCTI_CTICHOUTSTATUS Register

CSCTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

Register Description: CTI Channel Out Status Register

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Table 14-28938. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 0113Ch

Figure 14-9537. CSCTI_CTICHOUTSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CHOUTSTATUS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28940. CSCTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHOUTSTATUS	R	0h	Shows the status of the CTICHOUT outputs: 1=CTICHOUT is active, 0=CTICHOUT is inactive

14.11.2.293 CSCTI_CTIGATE Register

CSCTI_CTIGATE Register (Offset = 140h) [reset = 0h]

Register Description: The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs.

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Table 14-28941. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01140h

Figure 14-9538. CSCTI_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTIGATEEN			
R				R			
0h				0h			

Table 14-28943. CSCTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTIGATEEN	R	0h	Gate enable for the four channels [1 per bit]

14.11.2.294 CSCTI_ASICCTL Register

CSCTI_ASICCTL Register (Offset = 144h) [reset = 0h]

Register Description: Allows external multiplexing of the trigger signals

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Table 14-28944. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01144h

Figure 14-9539. CSCTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-28946. CSCTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]

14.11.2.295 CSCTI_ITCHINACK Register

CSCTI_ITCHINACK Register (Offset = EDCh) [reset = 0h]

Register Description: Integration and Test register

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Table 14-28947. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01EDCh

Figure 14-9540. CSCTI_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
R				R/W			
0h				0h			

Table 14-28949. CSCTI_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHINACK	R/W	0h	Sets the value of the CTCHINACK outputs

14.11.2.296 CSCTI_ITTRIGINACK Register

CSCTI_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

Register Description: ITTRIGINACK Register

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Table 14-28950. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01EE0h

Figure 14-9541. CSCTI_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-28952. CSCTI_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGINACK	R/W	0h	Sets the value of the CTTRIGINACK outputs

14.11.2.297 CSCTI_ITCHOUT Register

CSCTI_ITCHOUT Register (Offset = EE4h) [reset = 0h]

Register Description: ITCHOUT Register

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Table 14-28953. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01EE4h

Figure 14-9542. CSCTI_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
R				R/W			
0h				0h			

Table 14-28955. CSCTI_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHOUT	R/W	0h	Sets the value of the CTCHOUT outputs

14.11.2.298 CSCTI_ITTRIGOUT Register

CSCTI_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

Register Description: ITTRIGOUT Register

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Table 14-28956. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01EE8h

Figure 14-9543. CSCTI_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-28958. CSCTI_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUT	R/W	0h	Sets the value of the CTTRIGOUT outputs

14.11.2.299 CSCTI_ITCHOUTACK Register

CSCTI_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

Register Description: ITCHOUTACK Register

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Table 14-28959. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01EECh

Figure 14-9544. CSCTI_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTCHOUTACK							
R/W							
0h							

Table 14-28961. CSCTI_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTCHOUTACK	R/W	0h	Sets the value of the CTCHOUTACK outputs

14.11.2.300 CSCTI_ITTRIGOUTACK Register

CSCTI_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

Register Description: ITTRIGOUTACK Register

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Table 14-28962. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01EF0h

Figure 14-9545. CSCTI_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-28964. CSCTI_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUTACK	R	0h	Reads the value of the CTTRIGOUTACK inputs

14.11.2.301 CSCTI_ITCHIN Register

CSCTI_ITCHIN Register (Offset = EF4h) [reset = 0h]

Register Description: ITCHIN Register

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Table 14-28965. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01EF4h

Figure 14-9546. CSCTI_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
R				R			
0h				0h			

Table 14-28967. CSCTI_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHIN	R	0h	Reads the value of the CTCHIN inputs

14.11.2.302 CSCTI_ITTRIGIN Register

CSCTI_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

Register Description: ITTRIGIN Register

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Table 14-28968. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01EF8h

Figure 14-9547. CSCTI_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-28970. CSCTI_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGIN	R	0h	Reads the value of the CTTRIGIN inputs

14.11.2.303 CSCTI_ITCTRL Register

CSCTI_ITCTRL Register (Offset = F00h) [reset = 0h]

Register Description: ITCTRL Register

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Table 14-28971. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01F00h

Figure 14-9548. CSCTI_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							ITEN
R							R/W
0h							0h

Table 14-28973. CSCTI_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	ITEN	R/W	0h	Integration Test control enable

14.11.2.304 CSCTI_CLAIMSET Register

CSCTI_CLAIMSET Register (Offset = FA0h) [reset = 0h]

Register Description: Claim Tag Set Register

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Table 14-28974. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FA0h

Figure 14-9549. CSCTI_CLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_SET</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28976. CSCTI_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.11.2.305 CSCTI_CLAIMCLR Register

CSCTI_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

Register Description: Claim Tag Clear Register

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Table 14-28977. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FA4h

Figure 14-9550. CSCTI_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_CLEAR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-28979. CSCTI_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.11.2.306 CSCTI_LOCKACCESS Register

CSCTI_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

Register Description: Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-28980. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FB0h

Figure 14-9551. CSCTI_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
LOCKACCESSREG							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKACCESSREG							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKACCESSREG							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKACCESSREG							
R/W							
0h							

Table 14-28982. CSCTI_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKACCESSREG	R/W	0h	Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers If paddrdbg31 is high, this is ignored

14.11.2.307 CSCTI_LOCKSTATUS Register

CSCTI_LOCKSTATUS Register (Offset = FB4h) [reset = 0h]

Register Description: The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-28983. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FB4h

Figure 14-9552. CSCTI_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-28985. CSCTI_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.11.2.308 CSCTI_AUTHSTATUS Register

CSCTI_AUTHSTATUS Register (Offset = FB8h) [reset = 0h]

Register Description: Reports the required security level.

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Table 14-28986. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FB8h

Figure 14-9553. CSCTI_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-28988. CSCTI_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.11.2.309 CSCTI_DEVID Register

CSCTI_DEVID Register (Offset = FC8h) [reset = 0h]

Register Description: Device ID Register

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Table 14-28989. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FC8h

Figure 14-9554. CSCTI_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUM_ECT_CHANNELS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUM_ECT_TRIGGERS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED7_5</td><td colspan="5">IMPLEMENTATION_DEFINED</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-28991. CSCTI_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	R	0h	Reserved, returns 0
19:16	NUM_ECT_CHANNELS	R	0h	Number of ECT Channels available
15:8	NUM_ECT_TRIGGERS	R	0h	Number of ECT trigger available
7:5	RESERVED7_5	R	0h	Reserved, returns 0
4:0	IMPLEMENTATION_DEFINED	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Outputs using ASICCTL Defailt value of 0 indicates no multiplexing present

14.11.2.310 CSCTI_DEVTYPE Register

CSCTI_DEVTYPE Register (Offset = FCCh) [reset = 0h]

Register Description: Device Type Identifier Register

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Table 14-28992. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FCCh

Figure 14-9555. CSCTI_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEV_TYPE_ID							
R							
0h							

Table 14-28994. CSCTI_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.11.2.311 CSCTI_PERIPHID4 Register

CSCTI_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Register Description: Peripheral ID4 Register

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Table 14-28995. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FD0h

Figure 14-9556. CSCTI_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-28997. CSCTI_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.11.2.312 CSCTI_PERIPHID0 Register

CSCTI_PERIPHID0 Register (Offset = FE0h) [reset = 0h]

Register Description: Peripheral ID0 Register

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Table 14-28998. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FE0h

Figure 14-9557. CSCTI_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-29000. CSCTI_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.11.2.313 CSCTI_PERIPHID1 Register

CSCTI_PERIPHID1 Register (Offset = FE4h) [reset = 0h]

Register Description: Peripheral ID1 Register

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Table 14-29001. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FE4h

Figure 14-9558. CSCTI_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-29003. CSCTI_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.11.2.314 CSCTI_PERIPHID2 Register

CSCTI_PERIPHID2 Register (Offset = FE8h) [reset = 0h]

Register Description: Peripheral ID2 Register

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Table 14-29004. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FE8h

Figure 14-9559. CSCTI_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-29006. CSCTI_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.11.2.315 CSCTI_PERIPHID3 Register

CSCTI_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Register Description: Peripheral ID3 Register

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Table 14-29007. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FECh

Figure 14-9560. CSCTI_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-29009. CSCTI_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.11.2.316 CSCTI_COMPONID0 Register

CSCTI_COMPONID0 Register (Offset = FF0h) [reset = 0h]

Register Description: Component ID0 Register

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Table 14-29010. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FF0h

Figure 14-9561. CSCTI_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-29012. CSCTI_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.317 CSCTI_COMPONID1 Register

CSCTI_COMPONID1 Register (Offset = FF4h) [reset = 0h]

Register Description: Component ID1 Register

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Table 14-29013. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FF4h

Figure 14-9562. CSCTI_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-29015. CSCTI_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.318 CSCTI_COMPONID2 Register

CSCTI_COMPONID2 Register (Offset = FF8h) [reset = 0h]

Register Description: Component ID2 Register

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Table 14-29016. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FF8h

Figure 14-9563. CSCTI_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-29018. CSCTI_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.319 CSCTI_COMPONID3 Register

CSCTI_COMPONID3 Register (Offset = FFCh) [reset = 0h]

Register Description: Component ID3 Register

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Table 14-29019. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cscti	7600 01FFCh

Figure 14-9564. CSCTI_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-29021. CSCTI_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.320 DRM_CFG_0_PERIPH_ID Register

DRM_CFG_0_PERIPH_ID Register (Offset = 0h) [reset = 62836100h]

Register Description: This register is used to determine what the functionality of this peripheral is.

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Table 14-29022. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02000h

Figure 14-9565. DRM_CFG_0_PERIPH_ID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		283h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
283h							
15	14	13	12	11	10	9	8
RTLREV					MAJOR		
R					R		
Ch					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-29024. DRM_CFG_0_PERIPH_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Peripheral ID Scheme [0]
29:28	BU	R	2h	Reserved, returns 0
27:16	FUNCTION	R	283h	DRM Function ID [0x211]
15:11	RTLREV	R	Ch	RTL Revision [0]
10:8	MAJOR	R	1h	Major Peripheral Revision [0]
7:6	CUSTOM	R	0h	Custon Peripheral ID version [0]
5:0	MINOR	R	0h	Minor Peripheral Revision [0]

14.11.2.321 DRM_CFG_0_VERSION Register

DRM_CFG_0_VERSION Register (Offset = 4h) [reset = 0h]

Register Description: This register is used to enable the Time Generator. For application access, the DTG must be unlocked first.

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Table 14-29025. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02004h

Figure 14-9566. DRM_CFG_0_VERSION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MAJOR_VERSION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MAJOR_VERSION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MINOR_VERSION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MINOR_VERSION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29027. DRM_CFG_0_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MAJOR_VERSION	R	0h	Contains the major version value [1]
15:0	MINOR_VERSION	R	0h	Contains the minor version value [0]

14.11.2.322 DRM_CFG_0_CAPABILITY Register

DRM_CFG_0_CAPABILITY Register (Offset = 8h) [reset = 0h]

Register Description: This register can be read to determine the number of suspend signals and number of peripherals.

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Table 14-29028. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02008h

Figure 14-9567. DRM_CFG_0_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		NUM_SUSPENDS					
R		R					
0h		0h					
7	6	5	4	3	2	1	0
NUM_PERIPHERALS							
R							
0h							

Table 14-29030. DRM_CFG_0_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13:8	NUM_SUSPENDS	R	0h	Contains the number of Suspend signals supported, max of 32 There should be one signal per processor This value is set by a parameter at synthesis time
7:0	NUM_PERIPHERALS	R	0h	Contains the number of peripherals supported, max of 128 This affects the number of SUSPEND_REG registers This is set by a parameter during synthesis

14.11.2.323 DRM_CFG_0_TRACE_CTRL Register

DRM_CFG_0_TRACE_CTRL Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to set the trace sampling mode to center(1) or edge(0).

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Table 14-29031. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0200Ch

Figure 14-9568. DRM_CFG_0_TRACE_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							CENTER_SAMPLING
R							R/W
0h							0h

Table 14-29033. DRM_CFG_0_TRACE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	CENTER_SAMPLING	R/W	0h	Sets trace to center sampled

14.11.2.324 DRM_CFG_0_VBUSM_CTRL Register

DRM_CFG_0_VBUSM_CTRL Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to set attributes on the VBUSM memory accesses and to read the Debug Operating Mode

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Table 14-29034. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02010h

Figure 14-9569. DRM_CFG_0_VBUSM_CTRL Name Register

31	30	29	28	27	26	25	24
DOM_INPUT							
R							
0h							
23	22	21	20	19	18	17	16
DOM_INPUT			RESERVED				
R			R				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
VBUSM_PRIV		VBUSM_SECURE	VBUSM_DEBUG	CTL_PRIV		CTL_SECURE	EMUDBG
R		R	R	R/W		R/W	R/W
0h		0h	0h	0h		0h	0h

Table 14-29036. DRM_CFG_0_VBUSM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	DOM_INPUT	R	0h	This returns the DOM security input The upper 3 bits are the debug operating mode and the lower 8 bits are the priviledge ID for VBUSM transaction
20:8	RESERVED	R	0h	Reserved bits, return 0
7:6	VBUSM_PRIV	R	0h	These two bits show the currently state of the priv bits
5	VBUSM_SECURE	R	0h	This bit shows the currently active state of the VBUSM secure bit
4	VBUSM_DEBUG	R	0h	This is the currently active state of the VBUSM emudbg bit
3:2	CTL_PRIV	R/W	0h	These two bits determine the priviledge type for VBUSM accesses unless overridden by the DOM input [0 is user level privilege, 1 is supervisor level privilege, 2 is hypervisor level privilege and 3 is reserved]
1	CTL_SECURE	R/W	0h	When set [and DOM permits it], the VBUSM accesses will have the secure bit set
0	EMUDBG	R/W	0h	Sets the emudbg bit during access to make the debug or non-debug

14.11.2.325 DRM_CFG_0_DAP_TIMEOUT Register

DRM_CFG_0_DAP_TIMEOUT Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to set the maximum wait time for the DAP to complete a memory access.

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Table 14-29037. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02014h

Figure 14-9570. DRM_CFG_0_DAP_TIMEOUT Name Register

31	30	29	28	27	26	25	24
DAP_TIMEOUT_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DAP_TIMEOUT_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DAP_TIMEOUT_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DAP_TIMEOUT_REGISTER							
R/W							
0h							

Table 14-29039. DRM_CFG_0_DAP_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAP_TIMEOUT_REGISTER	R/W	0h	

14.11.2.326 DRM_CFG_0_CONFIG Register

DRM_CFG_0_CONFIG Register (Offset = 18h) [reset = 0h]

Register Description: This register adds softreset capability to the suspend module.

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Table 14-29040. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02018h

Figure 14-9571. DRM_CFG_0_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFTRESET
R							R/W
0h							0h

Table 14-29042. DRM_CFG_0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	Software controlled reset of the DRM

14.11.2.327 DRM_CFG_0_EMUTRIGEN Register

DRM_CFG_0_EMUTRIGEN Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to enable EMU triggers.

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Table 14-29043. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0201Ch

Figure 14-9572. DRM_CFG_0_EMUTRIGEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						EMU1TRIGEN	EMU0TRIGEN
R						R/W	R/W
0h						0h	0h

Table 14-29045. DRM_CFG_0_EMUTRIGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1	EMU1TRIGEN	R/W	0h	EMU 1 Trigger En
0	EMU0TRIGEN	R/W	0h	EMU 0 Trigger En

14.11.2.328 DRM_CFG_0_BINVALLO Register

DRM_CFG_0_BINVALLO Register (Offset = 20h) [reset = 0h]

Register Description: Reading this register returns the lower 32 bits of the binary debug time.

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Table 14-29046. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02020h

Figure 14-9573. DRM_CFG_0_BINVALLO Name Register

31	30	29	28	27	26	25	24
DTG_BINARY_TIME_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
DTG_BINARY_TIME_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
DTG_BINARY_TIME_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
DTG_BINARY_TIME_LOW							
R/W							
0h							

Table 14-29048. DRM_CFG_0_BINVALLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DTG_BINARY_TIME_LOW	R/W	0h	

14.11.2.329 DRM_CFG_0_BINVALHI Register

DRM_CFG_0_BINVALHI Register (Offset = 24h) [reset = 0h]

Register Description: Reading this register returns the upper 16 bits of the binary debug time and causes the lower 32 bits to be latched.

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Table 14-29049. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02024h

Figure 14-9574. DRM_CFG_0_BINVALHI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	BINTIMEHI						
NONE	R						
0h	0h						
7	6	5	4	3	2	1	0
BINTIMEHI							
R							
0h							

Table 14-29051. DRM_CFG_0_BINVALHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	BINTIMEHI	R	0h	Upper 16 bits of the timer

14.11.2.330 DRM_CFG_0_SUSPEND_REG0 Register

DRM_CFG_0_SUSPEND_REG0 Register (Offset = 200h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. There can be upto 128 of these registers (See NUM_PERIPHERALS in the DRM_CAPABILITY register)

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Table 14-29052. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02200h

Figure 14-9575. DRM_CFG_0_SUSPEND_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED1</td><td>SELECT</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SELECT</td><td colspan="3">RESERVED0</td><td>SUSPEND_CTL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-29054. DRM_CFG_0_SUSPEND_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8:4	SELECT	R/W	0h	Selects which suspend control line [1-32] goes to the peripheral
3:1	RESERVED0	R	0h	Reserved, returns 0
0	SUSPEND_CTL	R/W	0h	When 1, the peripheral is sensitive to the suspend signal, when 0, it ignore it

14.11.2.331 DRM_CFG_0_SUSPEND_REG1 Register

DRM_CFG_0_SUSPEND_REG1 Register (Offset = 204h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29055. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02204h

Figure 14-9576. DRM_CFG_0_SUSPEND_REG1 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_1							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_1							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_1							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_1							
R/W							
0h							

Table 14-29057. DRM_CFG_0_SUSPEND_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_1	R/W	0h	See Suspend Reg 0 for field information

14.11.2.332 DRM_CFG_0_SUSPEND_REG2 Register

DRM_CFG_0_SUSPEND_REG2 Register (Offset = 208h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29058. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02208h

Figure 14-9577. DRM_CFG_0_SUSPEND_REG2 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_2							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_2							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_2							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_2							
R/W							
0h							

Table 14-29060. DRM_CFG_0_SUSPEND_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_2	R/W	0h	See Suspend Reg 0 for field information

14.11.2.333 DRM_CFG_0_SUSPEND_REG3 Register

DRM_CFG_0_SUSPEND_REG3 Register (Offset = 20Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29061. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0220Ch

Figure 14-9578. DRM_CFG_0_SUSPEND_REG3 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_3							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_3							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_3							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_3							
R/W							
0h							

Table 14-29063. DRM_CFG_0_SUSPEND_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_3	R/W	0h	See Suspend Reg 0 for field information

14.11.2.334 DRM_CFG_0_SUSPEND_REG4 Register

DRM_CFG_0_SUSPEND_REG4 Register (Offset = 210h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29064. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02210h

Figure 14-9579. DRM_CFG_0_SUSPEND_REG4 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_4							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_4							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_4							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_4							
R/W							
0h							

Table 14-29066. DRM_CFG_0_SUSPEND_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_4	R/W	0h	See Suspend Reg 0 for field information

14.11.2.335 DRM_CFG_0_SUSPEND_REG5 Register

DRM_CFG_0_SUSPEND_REG5 Register (Offset = 214h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29067. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02214h

Figure 14-9580. DRM_CFG_0_SUSPEND_REG5 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_5							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_5							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_5							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_5							
R/W							
0h							

Table 14-29069. DRM_CFG_0_SUSPEND_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_5	R/W	0h	See Suspend Reg 0 for field information

14.11.2.336 DRM_CFG_0_SUSPEND_REG6 Register

DRM_CFG_0_SUSPEND_REG6 Register (Offset = 218h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29070. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02218h

Figure 14-9581. DRM_CFG_0_SUSPEND_REG6 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_6							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_6							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_6							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_6							
R/W							
0h							

Table 14-29072. DRM_CFG_0_SUSPEND_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_6	R/W	0h	See Suspend Reg 0 for field information

14.11.2.337 DRM_CFG_0_SUSPEND_REG7 Register

DRM_CFG_0_SUSPEND_REG7 Register (Offset = 21Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29073. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0221Ch

Figure 14-9582. DRM_CFG_0_SUSPEND_REG7 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_7							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_7							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_7							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_7							
R/W							
0h							

Table 14-29075. DRM_CFG_0_SUSPEND_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_7	R/W	0h	See Suspend Reg 0 for field information

14.11.2.338 DRM_CFG_0_SUSPEND_REG8 Register

DRM_CFG_0_SUSPEND_REG8 Register (Offset = 220h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29076. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02220h

Figure 14-9583. DRM_CFG_0_SUSPEND_REG8 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_8							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_8							
R/W							
0h							

Table 14-29078. DRM_CFG_0_SUSPEND_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_8	R/W	0h	See Suspend Reg 0 for field information

14.11.2.339 DRM_CFG_0_SUSPEND_REG9 Register

DRM_CFG_0_SUSPEND_REG9 Register (Offset = 224h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29079. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02224h

Figure 14-9584. DRM_CFG_0_SUSPEND_REG9 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_9							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_9							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_9							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_9							
R/W							
0h							

Table 14-29081. DRM_CFG_0_SUSPEND_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_9	R/W	0h	See Suspend Reg 0 for field information

14.11.2.340 DRM_CFG_0_SUSPEND_REG10 Register

DRM_CFG_0_SUSPEND_REG10 Register (Offset = 228h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29082. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02228h

Figure 14-9585. DRM_CFG_0_SUSPEND_REG10 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_10							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_10							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_10							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_10							
R/W							
0h							

Table 14-29084. DRM_CFG_0_SUSPEND_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_10	R/W	0h	See Suspend Reg 0 for field information

14.11.2.341 DRM_CFG_0_SUSPEND_REG11 Register

DRM_CFG_0_SUSPEND_REG11 Register (Offset = 22Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29085. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0222Ch

Figure 14-9586. DRM_CFG_0_SUSPEND_REG11 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_11							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_11							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_11							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_11							
R/W							
0h							

Table 14-29087. DRM_CFG_0_SUSPEND_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_11	R/W	0h	See Suspend Reg 0 for field information

14.11.2.342 DRM_CFG_0_SUSPEND_REG12 Register

DRM_CFG_0_SUSPEND_REG12 Register (Offset = 230h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29088. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02230h

Figure 14-9587. DRM_CFG_0_SUSPEND_REG12 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_12							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_12							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_12							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_12							
R/W							
0h							

Table 14-29090. DRM_CFG_0_SUSPEND_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_12	R/W	0h	See Suspend Reg 0 for field information

14.11.2.343 DRM_CFG_0_SUSPEND_REG13 Register

DRM_CFG_0_SUSPEND_REG13 Register (Offset = 234h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29091. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02234h

Figure 14-9588. DRM_CFG_0_SUSPEND_REG13 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_13							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_13							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_13							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_13							
R/W							
0h							

Table 14-29093. DRM_CFG_0_SUSPEND_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_13	R/W	0h	See Suspend Reg 0 for field information

14.11.2.344 DRM_CFG_0_SUSPEND_REG14 Register

DRM_CFG_0_SUSPEND_REG14 Register (Offset = 238h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29094. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02238h

Figure 14-9589. DRM_CFG_0_SUSPEND_REG14 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_14							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_14							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_14							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_14							
R/W							
0h							

Table 14-29096. DRM_CFG_0_SUSPEND_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_14	R/W	0h	See Suspend Reg 0 for field information

14.11.2.345 DRM_CFG_0_SUSPEND_REG15 Register

DRM_CFG_0_SUSPEND_REG15 Register (Offset = 23Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29097. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0223Ch

Figure 14-9590. DRM_CFG_0_SUSPEND_REG15 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_15							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_15							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_15							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_15							
R/W							
0h							

Table 14-29099. DRM_CFG_0_SUSPEND_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_15	R/W	0h	See Suspend Reg 0 for field information

14.11.2.346 DRM_CFG_0_SUSPEND_REG16 Register

DRM_CFG_0_SUSPEND_REG16 Register (Offset = 240h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29100. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02240h

Figure 14-9591. DRM_CFG_0_SUSPEND_REG16 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_16							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_16							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_16							
R/W							
0h							

Table 14-29102. DRM_CFG_0_SUSPEND_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_16	R/W	0h	See Suspend Reg 0 for field information

14.11.2.347 DRM_CFG_0_SUSPEND_REG17 Register

DRM_CFG_0_SUSPEND_REG17 Register (Offset = 244h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29103. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02244h

Figure 14-9592. DRM_CFG_0_SUSPEND_REG17 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_17							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_17							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_17							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_17							
R/W							
0h							

Table 14-29105. DRM_CFG_0_SUSPEND_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_17	R/W	0h	See Suspend Reg 0 for field information

14.11.2.348 DRM_CFG_0_SUSPEND_REG18 Register

DRM_CFG_0_SUSPEND_REG18 Register (Offset = 248h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29106. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02248h

Figure 14-9593. DRM_CFG_0_SUSPEND_REG18 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_18							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_18							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_18							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_18							
R/W							
0h							

Table 14-29108. DRM_CFG_0_SUSPEND_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_18	R/W	0h	See Suspend Reg 0 for field information

14.11.2.349 DRM_CFG_0_SUSPEND_REG19 Register

DRM_CFG_0_SUSPEND_REG19 Register (Offset = 24Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29109. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0224Ch

Figure 14-9594. DRM_CFG_0_SUSPEND_REG19 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_19							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_19							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_19							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_19							
R/W							
0h							

Table 14-29111. DRM_CFG_0_SUSPEND_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_19	R/W	0h	See Suspend Reg 0 for field information

14.11.2.350 DRM_CFG_0_SUSPEND_REG20 Register

DRM_CFG_0_SUSPEND_REG20 Register (Offset = 250h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29112. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02250h

Figure 14-9595. DRM_CFG_0_SUSPEND_REG20 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_20							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_20							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_20							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_20							
R/W							
0h							

Table 14-29114. DRM_CFG_0_SUSPEND_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_20	R/W	0h	See Suspend Reg 0 for field information

14.11.2.351 DRM_CFG_0_SUSPEND_REG21 Register

DRM_CFG_0_SUSPEND_REG21 Register (Offset = 254h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29115. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02254h

Figure 14-9596. DRM_CFG_0_SUSPEND_REG21 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_21							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_21							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_21							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_21							
R/W							
0h							

Table 14-29117. DRM_CFG_0_SUSPEND_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_21	R/W	0h	See Suspend Reg 0 for field information

14.11.2.352 DRM_CFG_0_SUSPEND_REG22 Register

DRM_CFG_0_SUSPEND_REG22 Register (Offset = 258h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29118. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02258h

Figure 14-9597. DRM_CFG_0_SUSPEND_REG22 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_22							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_22							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_22							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_22							
R/W							
0h							

Table 14-29120. DRM_CFG_0_SUSPEND_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_22	R/W	0h	See Suspend Reg 0 for field information

14.11.2.353 DRM_CFG_0_SUSPEND_REG23 Register

DRM_CFG_0_SUSPEND_REG23 Register (Offset = 25Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29121. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0225Ch

Figure 14-9598. DRM_CFG_0_SUSPEND_REG23 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_23							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_23							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_23							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_23							
R/W							
0h							

Table 14-29123. DRM_CFG_0_SUSPEND_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_23	R/W	0h	See Suspend Reg 0 for field information

14.11.2.354 DRM_CFG_0_SUSPEND_REG24 Register

DRM_CFG_0_SUSPEND_REG24 Register (Offset = 260h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29124. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02260h

Figure 14-9599. DRM_CFG_0_SUSPEND_REG24 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_24							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_24							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_24							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_24							
R/W							
0h							

Table 14-29126. DRM_CFG_0_SUSPEND_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_24	R/W	0h	See Suspend Reg 0 for field information

14.11.2.355 DRM_CFG_0_SUSPEND_REG25 Register

DRM_CFG_0_SUSPEND_REG25 Register (Offset = 264h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29127. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02264h

Figure 14-9600. DRM_CFG_0_SUSPEND_REG25 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_25							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_25							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_25							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_25							
R/W							
0h							

Table 14-29129. DRM_CFG_0_SUSPEND_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_25	R/W	0h	See Suspend Reg 0 for field information

14.11.2.356 DRM_CFG_0_SUSPEND_REG26 Register

DRM_CFG_0_SUSPEND_REG26 Register (Offset = 268h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29130. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02268h

Figure 14-9601. DRM_CFG_0_SUSPEND_REG26 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_26							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_26							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_26							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_26							
R/W							
0h							

Table 14-29132. DRM_CFG_0_SUSPEND_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_26	R/W	0h	See Suspend Reg 0 for field information

14.11.2.357 DRM_CFG_0_SUSPEND_REG27 Register

DRM_CFG_0_SUSPEND_REG27 Register (Offset = 26Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29133. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0226Ch

Figure 14-9602. DRM_CFG_0_SUSPEND_REG27 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_27							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_27							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_27							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_27							
R/W							
0h							

Table 14-29135. DRM_CFG_0_SUSPEND_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_27	R/W	0h	See Suspend Reg 0 for field information

14.11.2.358 DRM_CFG_0_SUSPEND_REG28 Register

DRM_CFG_0_SUSPEND_REG28 Register (Offset = 270h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29136. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02270h

Figure 14-9603. DRM_CFG_0_SUSPEND_REG28 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_28</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_28</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_28</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_28</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29138. DRM_CFG_0_SUSPEND_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_28	R/W	0h	See Suspend Reg 0 for field information

14.11.2.359 DRM_CFG_0_SUSPEND_REG29 Register

DRM_CFG_0_SUSPEND_REG29 Register (Offset = 274h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29139. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02274h

Figure 14-9604. DRM_CFG_0_SUSPEND_REG29 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_29							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_29							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_29							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_29							
R/W							
0h							

Table 14-29141. DRM_CFG_0_SUSPEND_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_29	R/W	0h	See Suspend Reg 0 for field information

14.11.2.360 DRM_CFG_0_SUSPEND_REG30 Register

DRM_CFG_0_SUSPEND_REG30 Register (Offset = 278h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29142. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 02278h

Figure 14-9605. DRM_CFG_0_SUSPEND_REG30 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_30							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_30							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_30							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_30							
R/W							
0h							

Table 14-29144. DRM_CFG_0_SUSPEND_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_30	R/W	0h	See Suspend Reg 0 for field information

14.11.2.361 DRM_CFG_0_SUSPEND_REG31 Register

DRM_CFG_0_SUSPEND_REG31 Register (Offset = 27Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-29145. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_0	7200 0227Ch

Figure 14-9606. DRM_CFG_0_SUSPEND_REG31 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_31							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_31							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_31							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_31							
R/W							
0h							

Table 14-29147. DRM_CFG_0_SUSPEND_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_31	R/W	0h	See Suspend Reg 0 for field information

14.11.2.362 CSTPIU_CFG_0_SUPPORTSIZE Register

CSTPIU_CFG_0_SUPPORTSIZE Register (Offset = 0h) [reset = 0h]

Register Description: This register indicates how many trace pins are available for export. One pin per bit, right justified

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Table 14-29148. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04000h

Figure 14-9607. CSTPIU_CFG_0_SUPPORTSIZE Name Register

31	30	29	28	27	26	25	24
SUPPORTSIZEREG							
R							
0h							
23	22	21	20	19	18	17	16
SUPPORTSIZEREG							
R							
0h							
15	14	13	12	11	10	9	8
SUPPORTSIZEREG							
R							
0h							
7	6	5	4	3	2	1	0
SUPPORTSIZEREG							
R							
0h							

Table 14-29150. CSTPIU_CFG_0_SUPPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUPPORTSIZEREG	R	0h	This register indicates how many trace pins are available for export One pin per bit, right justified

14.11.2.363 CSTPIU_CFG_0_CURPORTSIZE Register

CSTPIU_CFG_0_CURPORTSIZE Register (Offset = 4h) [reset = 0h]

Register Description: The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

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Table 14-29151. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04004h

Figure 14-9608. CSTPIU_CFG_0_CURPORTSIZE Name Register

31	30	29	28	27	26	25	24
CURRENTPORTSIZE							
R/W							
0h							
23	22	21	20	19	18	17	16
CURRENTPORTSIZE							
R/W							
0h							
15	14	13	12	11	10	9	8
CURRENTPORTSIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
CURRENTPORTSIZE							
R/W							
0h							

Table 14-29153. CSTPIU_CFG_0_CURPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CURRENTPORTSIZE	R/W	0h	The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

14.11.2.364 CSTPIU_CFG_0_TRIGMODEREG Register

CSTPIU_CFG_0_TRIGMODEREG Register (Offset = 100h) [reset = 0h]

Register Description: This register indicates the implemented Trigger Counter multipliers and other supported features of the trigger system

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Table 14-29154. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04100h

Figure 14-9609. CSTPIU_CFG_0_TRIGMODEREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED						TRGRUN	TRIGGERED
R						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED2							TCOUNT8
R							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED1			MUILTPLIERS				
R			R				
0h			0h				

Table 14-29156. CSTPIU_CFG_0_TRIGMODEREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17	TRGRUN	R	0h	Trigger Counter running A trigger has occurred but the counter is not at zero
16	TRIGGERED	R	0h	A trigger has occurred and the counter has reached zero
15:9	RESERVED2	R	0h	Reserved, returns 0
8	TCOUNT8	R	0h	An 8-bit wide counter register implemented
7:5	RESERVED1	R	0h	Reserved, returns 0
4:0	MUILTPLIERS	R	0h	Multiply the Trigger Counter by 2, 4, 16, 256, 64K supported Each bit is a mpy value

14.11.2.365 CSTPIU_CFG_0_TRIGCTRREG Register

CSTPIU_CFG_0_TRIGCTRREG Register (Offset = 104h) [reset = 0h]

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Table 14-29157. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04104h

Figure 14-9610. CSTPIU_CFG_0_TRIGCTRREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGCOUNT							
R/W							
0h							

Table 14-29159. CSTPIU_CFG_0_TRIGCTRREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGCOUNT	R/W	0h	8-bit counter value for the number of words to be output from the formatter before a trigger is inserted

14.11.2.366 CSTPIU_CFG_0_TRIGMPYREG Register

CSTPIU_CFG_0_TRIGMPYREG Register (Offset = 108h) [reset = 0h]

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Table 14-29160. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04108h

Figure 14-9611. CSTPIU_CFG_0_TRIGMPYREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			MULTIPLIER				
R			R/W				
0h			0h				

Table 14-29162. CSTPIU_CFG_0_TRIGMPYREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4:0	MULTIPLIER	R/W	0h	Trigger multiply value bit0=x2, bit1=x4, bit2=x16, bit3=x256, bit4=x64K

14.11.2.367 CSTPIU_CFG_0_SUPTESTPAT Register

CSTPIU_CFG_0_SUPTESTPAT Register (Offset = 200h) [reset = 0h]

Register Description: This register displays the supported patterns and modes for calibration

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Table 14-29163. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04200h

Figure 14-9612. CSTPIU_CFG_0_SUPTESTPAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						MODE	
R						R	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				PATTERN			
R				R			
0h				0h			

Table 14-29165. CSTPIU_CFG_0_SUPTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R	0h	bit 16 is Timed Mode, bit 17 is continuous mode
15:4	RESERVED1	R	0h	Reserved, returns 0
3:0	PATTERN	R	0h	bit0=Walking 1 pattern, bit1=walking 0, bit2=AA/55 pattern, bit3=FF/00 pattern

14.11.2.368 CSTPIU_CFG_0_CURTESTPAT Register

CSTPIU_CFG_0_CURTESTPAT Register (Offset = 204h) [reset = 0h]

Register Description: This register displays the supported patterns and modes for calibration

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Table 14-29166. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04204h

Figure 14-9613. CSTPIU_CFG_0_CURTESTPAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED						MODE	
R						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1				RESERVED	PATTERN		
R				NONE	R/W		
0h				0h	0h		

Table 14-29168. CSTPIU_CFG_0_CURTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R/W	0h	Select the Pattern Timer Mode, see Supported Patterns reg
15:4	RESERVED1	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	PATTERN	R/W	0h	Select the pattern to run, set Supported Patterns Reg

14.11.2.369 CSTPIU_CFG_0_TESTPATCNT Register

CSTPIU_CFG_0_TESTPATCNT Register (Offset = 208h) [reset = 0h]

Register Description: This register displays the supported patterns and modes for calibration

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Table 14-29169. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04208h

Figure 14-9614. CSTPIU_CFG_0_TESTPATCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PATTERNCOUNT							
R/W							
0h							

Table 14-29171. CSTPIU_CFG_0_TESTPATCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PATTERNCOUNT	R/W	0h	Number of clocks a pattern should run before going to the next pattern

14.11.2.370 CSTPIU_CFG_0_FORMFLUSHSTAT Register

CSTPIU_CFG_0_FORMFLUSHSTAT Register (Offset = 300h) [reset = 0h]

Register Description: This register displays the supported patterns and modes for calibration

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Table 14-29172. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04300h

Figure 14-9615. CSTPIU_CFG_0_FORMFLUSHSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>TCPRESENT</td><td>FTSTOPPED</td><td>FLINPROG</td></tr>
<tr><td colspan="5">R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29174. CSTPIU_CFG_0_FORMFLUSHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	TCPRESENT	R	0h	If this bit is set then TRACECTL is present If no TRACECTL pin is present, then the data formatter must be used and only in continuous mode
1	FTSTOPPED	R	0h	Formatter stopped The formatter has received a stop request signal and all trace data and post-amble has been output
0	FLINPROG	R	0h	Flush In Progress This is an indication of the current state of AFVALIDS

14.11.2.371 CSTPIU_CFG_0_FORMFLUSHCTL Register

CSTPIU_CFG_0_FORMFLUSHCTL Register (Offset = 304h) [reset = 0h]

Register Description: This register controls the generation of stop, trigger, and flush events.

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Table 14-29175. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04304h

Figure 14-9616. CSTPIU_CFG_0_FORMFLUSHCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		STOPTRIG	STOPFL	RESERVED3	TRIGFL	TRIGEVT	TRIGIN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	FONMAN	FONTRIG	FONFIIN	RESERVED1		ENFCONT	ENFTC
R	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-29177. CSTPIU_CFG_0_FORMFLUSHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13	STOPTRIG	R/W	0h	Stop the formatter after a Trigger Event is observed
12	STOPFL	R/W	0h	Stop the formatter after a flush completes [return of AFREADYS]
11	RESERVED3	R	0h	Reserved, returns 0
10	TRIGFL	R/W	0h	Indicates a trigger on Flush completion on AFREADYS being returned
9	TRIGEVT	R/W	0h	Indicate a trigger on a Trigger Event
8	TRIGIN	R/W	0h	Indicate a trigger on TRIGIN being asserted
7	RESERVED2	R	0h	Reserved, returns 0
6	FONMAN	R/W	0h	Manually generate a flush of the system It is cleared when this flush has been serviced
5	FONTRIG	R/W	0h	Generate flush using Trigger event
4	FONFIIN	R/W	0h	Generate flush using the FLUSHIN interface
3:2	RESERVED1	R	0h	Reserved, returns 0
1	ENFCONT	R/W	0h	Continuous Formatting Embed in trigger packets and indicate null cycles using Sync packets
0	ENFTC	R/W	0h	Enable Formatting Do not embed Triggers into the formatted stream

14.11.2.372 CSTPIU_CFG_0_FORMSYNCCTR Register

CSTPIU_CFG_0_FORMSYNCCTR Register (Offset = 308h) [reset = 0h]

Register Description: This counter is the number of formatter frames since the last synchronization packet of 128 bits, and is a 12-bit counter with a maximum count value of 4096

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Table 14-29178. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04308h

Figure 14-9617. CSTPIU_CFG_0_FORMSYNCCTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				CYCCOUNT			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CYCCOUNT							
R/W							
0h							

Table 14-29180. CSTPIU_CFG_0_FORMSYNCCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:0	CYCCOUNT	R/W	0h	12-bit counter value to indicate the number of complete frames between full sync packets

14.11.2.373 CSTPIU_CFG_0_EXTCTLIN Register

CSTPIU_CFG_0_EXTCTLIN Register (Offset = 400h) [reset = 0h]

Register Description: This register inputs data from an external port (if used)

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Table 14-29181. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04400h

Figure 14-9618. CSTPIU_CFG_0_EXTCTLIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_INPUT_REGISTER							
R							
0h							

Table 14-29183. CSTPIU_CFG_0_EXTCTLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	reserved, returns 0
7:0	EXCTL_PORT_INPUT_REGISTER	R	0h	

14.11.2.374 CSTPIU_CFG_0_EXTCTLOUT Register

CSTPIU_CFG_0_EXTCTLOUT Register (Offset = 404h) [reset = 0h]

Register Description: This register is output to an external port (if used)

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Table 14-29184. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04404h

Figure 14-9619. CSTPIU_CFG_0_EXTCTLOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_OUTPUT_REGISTER							
R/W							
0h							

Table 14-29186. CSTPIU_CFG_0_EXTCTLOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	returns 0
7:0	EXCTL_PORT_OUTPUT_REGISTER	R/W	0h	

14.11.2.375 CSTPIU_CFG_0_ITTRFLINACK Register

CSTPIU_CFG_0_ITTRFLINACK Register (Offset = EE4h) [reset = 0h]

Register Description: Integration Test Trigger In and Flush In Acknowledge.

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Table 14-29187. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04EE4h

Figure 14-9620. CSTPIU_CFG_0_ITTRFLINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						ATID	
R						R/W	
0h						0h	

Table 14-29189. CSTPIU_CFG_0_ITTRFLINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.11.2.376 CSTPIU_CFG_0_ITTRFLIN Register

CSTPIU_CFG_0_ITTRFLIN Register (Offset = EE8h) [reset = 0h]

Register Description: Integration Test Trigger In and Flush In Register.

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Table 14-29190. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04EE8h

Figure 14-9621. CSTPIU_CFG_0_ITTRFLIN Name Register

31	30	29	28	27	26	25	24
INTEGRATIONTRFLIN							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTEGRATIONTRFLIN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTEGRATIONTRFLIN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTEGRATIONTRFLIN							
R/W							
0h							

Table 14-29192. CSTPIU_CFG_0_ITTRFLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATIONTRFLIN	R/W	0h	

14.11.2.377 CSTPIU_CFG_0_ITATBDATA0 Register

CSTPIU_CFG_0_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Register Description: Integration Test ATB Data Register 0

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Table 14-29193. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04EECh

Figure 14-9622. CSTPIU_CFG_0_ITATBDATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">INTEGRATION_TEST_ATB_REG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INTEGRATION_TEST_ATB_REG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">INTEGRATION_TEST_ATB_REG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTEGRATION_TEST_ATB_REG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29195. CSTPIU_CFG_0_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_REG	R/W	0h	

14.11.2.378 CSTPIU_CFG_0_ITATBCTR2 Register

CSTPIU_CFG_0_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Register Description: Integration Test ATB Control Register 2.

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Table 14-29196. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04EF0h

Figure 14-9623. CSTPIU_CFG_0_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							

Table 14-29198. CSTPIU_CFG_0_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG2	R/W	0h	

14.11.2.379 CSTPIU_CFG_0_ITATBCTR1 Register

CSTPIU_CFG_0_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Register Description: Integration Test ATB Control Register 1.

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Table 14-29199. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04EF4h

Figure 14-9624. CSTPIU_CFG_0_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							

Table 14-29201. CSTPIU_CFG_0_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG1	R/W	0h	

14.11.2.380 CSTPIU_CFG_0_ITATBCTR0 Register

CSTPIU_CFG_0_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Register Description: Integration Test ATB Control Register 0

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Table 14-29202. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04EF8h

Figure 14-9625. CSTPIU_CFG_0_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							

Table 14-29204. CSTPIU_CFG_0_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG0	R/W	0h	

14.11.2.381 CSTPIU_CFG_0_INTCTRL Register

CSTPIU_CFG_0_INTCTRL Register (Offset = F00h) [reset = 0h]

Register Description: Integration Mode Register

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Table 14-29205. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04F00h

Figure 14-9626. CSTPIU_CFG_0_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-29207. CSTPIU_CFG_0_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.11.2.382 CSTPIU_CFG_0_CTSET Register

CSTPIU_CFG_0_CTSET Register (Offset = FA0h) [reset = 0h]

Register Description: Claim Tag Set Register

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Table 14-29208. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FA0h

Figure 14-9627. CSTPIU_CFG_0_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-29210. CSTPIU_CFG_0_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.11.2.383 CSTPIU_CFG_0_CTCLR Register

CSTPIU_CFG_0_CTCLR Register (Offset = FA4h) [reset = 0h]

Register Description: Claim Tag Clear Register

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Table 14-29211. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FA4h

Figure 14-9628. CSTPIU_CFG_0_CTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-29213. CSTPIU_CFG_0_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.11.2.384 CSTPIU_CFG_0_LAREG Register

CSTPIU_CFG_0_LAREG Register (Offset = FB0h) [reset = 0h]

Register Description: Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-29214. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FB0h

Figure 14-9629. CSTPIU_CFG_0_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCK_ACCESS_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK_ACCESS_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK_ACCESS_REGISTER							
R/W							
0h							

Table 14-29216. CSTPIU_CFG_0_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.11.2.385 CSTPIU_CFG_0_LSREG Register

CSTPIU_CFG_0_LSREG Register (Offset = FB4h) [reset = 0h]

Register Description: The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-29217. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FB4h

Figure 14-9630. CSTPIU_CFG_0_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-29219. CSTPIU_CFG_0_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.11.2.386 CSTPIU_CFG_0_AUTHST Register

CSTPIU_CFG_0_AUTHST Register (Offset = FB8h) [reset = 0h]

Register Description: Reports the required security level.

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Table 14-29220. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FB8h

Figure 14-9631. CSTPIU_CFG_0_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-29222. CSTPIU_CFG_0_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.11.2.387 CSTPIU_CFG_0_DEVID Register

CSTPIU_CFG_0_DEVID Register (Offset = FC8h) [reset = 0h]

Register Description: This shows the characteristics of the TPIU

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Table 14-29223. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FC8h

Figure 14-9632. CSTPIU_CFG_0_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td>SWO_UART</td><td>SWO_MANCHESTER</td><td>TRACE_CLOCK_SUP</td><td>FIFO_SIZE</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">FIFO_SIZE</td><td>CLOCK_RELATIONSHIP</td><td colspan="5">HIDDEN_MUXING</td></tr>
<tr><td colspan="2">R</td><td>R</td><td colspan="5">R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-29225. CSTPIU_CFG_0_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11	SWO_UART	R	0h	Indicates Serial Wire Output [UART/NRZ] is not supported Defaul = 0
10	SWO_MANCHESTER	R	0h	Indicates Serial Wire Output [Manchester] is not supported Default = 0
9	TRACE_CLOCK_SUP	R	0h	Indicates trace clock + data is supported
8:6	FIFO_SIZE	R	0h	FIFO size in powers of 2 A value of 2 gives a FIFO size of 4 entries, 16 bytes Default is3'b010
5	CLOCK_RELATIONSHIP	R	0h	Indicates the relationship between ATCLK and TRACECLKIN 0x1 indicates asynchronous
4:0	HIDDEN_MUXING	R	0h	When nonzero this value indicates the type/number of ATB multiplexing present on the input to the ATB Currently only 0x00 is supported, that is, no multiplexing present

14.11.2.388 CSTPIU_CFG_0_DEVTYPEID Register

CSTPIU_CFG_0_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Register Description: Device Type Identifier Register

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Table 14-29226. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FCCh

Figure 14-9633. CSTPIU_CFG_0_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-29228. CSTPIU_CFG_0_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.11.2.389 CSTPIU_CFG_0_PERID4 Register

CSTPIU_CFG_0_PERID4 Register (Offset = FD0h) [reset = 0h]

Register Description: Peripheral ID4 Register

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Table 14-29229. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FD0h

Figure 14-9634. CSTPIU_CFG_0_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-29231. CSTPIU_CFG_0_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.11.2.390 CSTPIU_CFG_0_PERID0 Register

CSTPIU_CFG_0_PERID0 Register (Offset = FE0h) [reset = 0h]

Register Description: Peripheral ID0 Register

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Table 14-29232. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FE0h

Figure 14-9635. CSTPIU_CFG_0_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-29234. CSTPIU_CFG_0_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.11.2.391 CSTPIU_CFG_0_PERID1 Register

CSTPIU_CFG_0_PERID1 Register (Offset = FE4h) [reset = 0h]

Register Description: Peripheral ID1 Register

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Table 14-29235. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FE4h

Figure 14-9636. CSTPIU_CFG_0_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-29237. CSTPIU_CFG_0_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.11.2.392 CSTPIU_CFG_0_PERID2 Register

CSTPIU_CFG_0_PERID2 Register (Offset = FE8h) [reset = 0h]

Register Description: Peripheral ID2 Register

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Table 14-29238. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FE8h

Figure 14-9637. CSTPIU_CFG_0_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-29240. CSTPIU_CFG_0_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.11.2.393 CSTPIU_CFG_0_PERID3 Register

CSTPIU_CFG_0_PERID3 Register (Offset = FECh) [reset = 0h]

Register Description: Peripheral ID3 Register

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Table 14-29241. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FECh

Figure 14-9638. CSTPIU_CFG_0_PERID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-29243. CSTPIU_CFG_0_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.11.2.394 CSTPIU_CFG_0_COMPID0 Register

CSTPIU_CFG_0_COMPID0 Register (Offset = FF0h) [reset = 0h]

Register Description: Component ID0 Register

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Table 14-29244. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FF0h

Figure 14-9639. CSTPIU_CFG_0_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-29246. CSTPIU_CFG_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.395 CSTPIU_CFG_0_COMPID1 Register

CSTPIU_CFG_0_COMPID1 Register (Offset = FF4h) [reset = 0h]

Register Description: Component ID1 Register

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Table 14-29247. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FF4h

Figure 14-9640. CSTPIU_CFG_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-29249. CSTPIU_CFG_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.396 CSTPIU_CFG_0_COMPID2 Register

CSTPIU_CFG_0_COMPID2 Register (Offset = FF8h) [reset = 0h]

Register Description: Component ID2 Register

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Table 14-29250. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FF8h

Figure 14-9641. CSTPIU_CFG_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-29252. CSTPIU_CFG_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.397 CSTPIU_CFG_0_COMPID3 Register

CSTPIU_CFG_0_COMPID3 Register (Offset = FFCh) [reset = 0h]

Register Description: Component ID3 Register

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Table 14-29253. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_0	7200 04FFCh

Figure 14-9642. CSTPIU_CFG_0_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-29255. CSTPIU_CFG_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.398 CTF_CFG_0_CSTFCTLREG Register

CTF_CFG_0_CSTFCTLREG Register (Offset = 0h) [reset = 0h]

Register Description: It enables the slave ports and defines the hold time of the slave ports.

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Table 14-29256. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05000h

Figure 14-9643. CTF_CFG_0_CSTFCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				MINHOLDTIME			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
SLVPORTEN							
R/W							
0h							

Table 14-29258. CTF_CFG_0_CSTFCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:8	MINHOLDTIME	R/W	0h	Minimum Hold time Hold time refers to the number of transactions that are output on the funnel master port from the same target while that target port ATVALIDSx is HIGH The CSTF holds for the minimum hold time and one additional cycle The maximum value that can be entered is 0xE and this equates to 15 cycles 0xF is reserved
7:0	SLVPORTEN	R/W	0h	Target Port Enables Setting these bits enables the corresponding input, or target port If a bit is not set then this has the effect of excluding that port from the priority selection scheme

14.11.2.399 CTF_CFG_0_PRIORCTLREG Register

CTF_CFG_0_PRIORCTLREG Register (Offset = 4h) [reset = 0h]

Register Description: Defines the order in which inputs are selected. This register must only be altered when the trace sources are off and the system is drained.

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Table 14-29259. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05004h

Figure 14-9644. CTF_CFG_0_PRIORCTLREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">PRIPORT7</td><td colspan="3">PRIPORT6</td><td colspan="2">PRIPORT5</td></tr>
<tr><td colspan="3">R/W</td><td colspan="3">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="3">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>PRIPORT5</td><td colspan="3">PRIPORT4</td><td colspan="3">PRIPORT3</td><td>PRIPORT2</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PRIPORT2</td><td colspan="3">PRIPORT1</td><td colspan="3">PRIPORT0</td></tr>
<tr><td colspan="2">R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-29261. CTF_CFG_0_PRIORCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23:21	PRIPORT7	R/W	0h	Priority value of the eighth target port Highest priority goes to the lowest value
20:18	PRIPORT6	R/W	0h	Priority value of the seventh target port Highest priority goes to the lowest value
17:15	PRIPORT5	R/W	0h	Priority value of the sixth target port Highest priority goes to the lowest value
14:12	PRIPORT4	R/W	0h	Priority value of the fifth target port Highest priority goes to the lowest value
11:9	PRIPORT3	R/W	0h	Priority value of the fourth target port Highest priority goes to the lowest value
8:6	PRIPORT2	R/W	0h	Priority value of the third target port Highest priority goes to the lowest value
5:3	PRIPORT1	R/W	0h	Priority value of the second target port Highest priority goes to the lowest value
2:0	PRIPORT0	R/W	0h	Priority value of the first target port Highest priority goes to the lowest value

14.11.2.400 CTF_CFG_0_ITATBDATA0 Register

CTF_CFG_0_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Register Description: Integration Test Register.

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Table 14-29262. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05EECh

Figure 14-9645. CTF_CFG_0_ITATBDATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>ATDATA31</td><td>ATDATA23</td><td>ATDATA15</td><td>ATDATA7</td><td>ATDATA0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29264. CTF_CFG_0_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4	ATDATA31	R/W	0h	A write outputs data on ATDATAM[31] A read returns the value of ATDATAS[31]
3	ATDATA23	R/W	0h	A write outputs data on ATDATAM[23] A read returns the value of ATDATAS[23]
2	ATDATA15	R/W	0h	A write outputs data on ATDATAM[15] A read returns the value of ATDATAS[15]
1	ATDATA7	R/W	0h	A write outputs data on ATDATAM[7] A read returns the value of ATDATAS[7]
0	ATDATA0	R/W	0h	A write outputs data on ATDATAM[0] A read returns the value of ATDATAS[0]

14.11.2.401 CTF_CFG_0_ITATBCTR2 Register

CTF_CFG_0_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Register Description: Integration Test Control Register 2.

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Table 14-29265. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05EF0h

Figure 14-9646. CTF_CFG_0_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED		AFVALID	ATREADY
R				NONE		R/W	R/W
0h				0h		0h	0h

Table 14-29267. CTF_CFG_0_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:2	RESERVED	NONE	0h	Reserved
1	AFVALID	R/W	0h	Reading this bit returns the value of AFVALIDM Writing this bit sets the AFVALIDS[n] bit where n is enabled by the CSTFCTLREG
0	ATREADY	R/W	0h	Reading this bit returns the value of ATREADYM Writing this bit sets the AFREADYS[n] bit where n is enabled by the CSTFCTLREG

14.11.2.402 CTF_CFG_0_ITATBCTR1 Register

CTF_CFG_0_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Register Description: Integration Test Control Register 1.

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Table 14-29268. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05EF4h

Figure 14-9647. CTF_CFG_0_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RESERVED	ATID					
R	NONE	R/W					
0h	0h	0h					

Table 14-29270. CTF_CFG_0_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6	RESERVED	NONE	0h	Reserved
5:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.11.2.403 CTF_CFG_0_ITATBCTR0 Register

CTF_CFG_0_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Register Description: Integration Test Control Register 0.

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Table 14-29271. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05EF8h

Figure 14-9648. CTF_CFG_0_ITATBCTR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td colspan="2">ATBYTES</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>AFREADY</td><td>ATVALID</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29273. CTF_CFG_0_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED1	R	0h	Reserved, returns 0
9:8	ATBYTES	R/W	0h	Writing this field sets the value of ATBYTESM Reading it returns the value of ATBYTSS[n]
7:2	RESERVED	R	0h	Reserved, returns 0
1	AFREADY	R/W	0h	Writing this field sets the value of AFREADYM Reading it returns the value of AFREADYS[n]
0	ATVALID	R/W	0h	Writing this field sets the value of ATVALIDM Reading it returns the value of ATVALIDS[n]

14.11.2.404 CTF_CFG_0_INTCTRL Register

CTF_CFG_0_INTCTRL Register (Offset = F00h) [reset = 0h]

Register Description: Integration Mode Register

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Table 14-29274. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05F00h

Figure 14-9649. CTF_CFG_0_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-29276. CTF_CFG_0_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.11.2.405 CTF_CFG_0_CTSET Register

CTF_CFG_0_CTSET Register (Offset = FA0h) [reset = 0h]

Register Description: Claim Tag Set Register

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Table 14-29277. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FA0h

Figure 14-9650. CTF_CFG_0_CTSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_SET</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29279. CTF_CFG_0_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.11.2.406 CTF_CFG_0_CTCLR Register

CTF_CFG_0_CTCLR Register (Offset = FA4h) [reset = 0h]

Register Description: Claim Tag Clear Register

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Table 14-29280. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FA4h

Figure 14-9651. CTF_CFG_0_CTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-29282. CTF_CFG_0_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.11.2.407 CTF_CFG_0_LAREG Register

CTF_CFG_0_LAREG Register (Offset = FB0h) [reset = 0h]

Register Description: Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-29283. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FB0h

Figure 14-9652. CTF_CFG_0_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
R/W							
0h							

Table 14-29285. CTF_CFG_0_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.11.2.408 CTF_CFG_0_LSREG Register

CTF_CFG_0_LSREG Register (Offset = FB4h) [reset = 0h]

Register Description: The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-29286. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FB4h

Figure 14-9653. CTF_CFG_0_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-29288. CTF_CFG_0_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.11.2.409 CTF_CFG_0_AUTHST Register

CTF_CFG_0_AUTHST Register (Offset = FB8h) [reset = 0h]

Register Description: Reports the required security level.

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Table 14-29289. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FB8h

Figure 14-9654. CTF_CFG_0_AUTHST Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">AUTHENTICATION_STATUS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29291. CTF_CFG_0_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.11.2.410 CTF_CFG_0_DEVID Register

CTF_CFG_0_DEVID Register (Offset = FC8h) [reset = 0h]

Register Description: Device ID Register

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Table 14-29292. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FC8h

Figure 14-9655. CTF_CFG_0_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PRIOTITY_SCHEME				PORTCOUNT			
R				R			
0h				0h			

Table 14-29294. CTF_CFG_0_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, return 0s
7:4	PRIOTITY_SCHEME	R	0h	The CSTF implements a static priority scheme Value = 0x2
3:0	PORTCOUNT	R	0h	This is the value of the Verilog define PORTCOUNT and represents the number of input ports connected By default all 8 ports are connected 0x0 and 0x1 are illegal values

14.11.2.411 CTF_CFG_0_DEVTYPEID Register

CTF_CFG_0_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Register Description: Device Type Identifier Register

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Table 14-29295. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FCCh

Figure 14-9656. CTF_CFG_0_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-29297. CTF_CFG_0_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	A value of 0x12 identifies this device as a trace link [0x2] and specifically as a funnel/router [0x1]

14.11.2.412 CTF_CFG_0_PERID4 Register

CTF_CFG_0_PERID4 Register (Offset = FD0h) [reset = 0h]

Register Description: Peripheral ID4 Register

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Table 14-29298. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FD0h

Figure 14-9657. CTF_CFG_0_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-29300. CTF_CFG_0_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.11.2.413 CTF_CFG_0_PERID5 Register

CTF_CFG_0_PERID5 Register (Offset = FD4h) [reset = 0h]

Register Description: Peripheral ID5 Register

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Table 14-29301. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FD4h

Figure 14-9658. CTF_CFG_0_PERID5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID5							
R							
0h							

Table 14-29303. CTF_CFG_0_PERID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID5	R	0h	Peripheral ID 5, returns 0x0

14.11.2.414 CTF_CFG_0_PERID6 Register

CTF_CFG_0_PERID6 Register (Offset = FD8h) [reset = 0h]

Register Description: Peripheral ID6 Register

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Table 14-29304. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FD8h

Figure 14-9659. CTF_CFG_0_PERID6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID6							
R							
0h							

Table 14-29306. CTF_CFG_0_PERID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID6	R	0h	Peripheral ID 6, returns 0x0

14.11.2.415 CTF_CFG_0_PERID7 Register

CTF_CFG_0_PERID7 Register (Offset = FDCh) [reset = 0h]

Register Description: Peripheral ID7 Register

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Table 14-29307. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FDCh

Figure 14-9660. CTF_CFG_0_PERID7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID7							
R							
0h							

Table 14-29309. CTF_CFG_0_PERID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID7	R	0h	Peripheral ID 7, returns 0x0

14.11.2.416 CTF_CFG_0_PERID0 Register

CTF_CFG_0_PERID0 Register (Offset = FE0h) [reset = 0h]

Register Description: Peripheral ID0 Register

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Table 14-29310. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FE0h

Figure 14-9661. CTF_CFG_0_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERIPH_ID0							
R							
0h							

Table 14-29312. CTF_CFG_0_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.11.2.417 CTF_CFG_0_PERID1 Register

CTF_CFG_0_PERID1 Register (Offset = FE4h) [reset = 0h]

Register Description: Peripheral ID1 Register

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Table 14-29313. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FE4h

Figure 14-9662. CTF_CFG_0_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-29315. CTF_CFG_0_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.11.2.418 CTF_CFG_0_PERID2 Register

CTF_CFG_0_PERID2 Register (Offset = FE8h) [reset = 0h]

Register Description: Peripheral ID2 Register

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Table 14-29316. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FE8h

Figure 14-9663. CTF_CFG_0_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-29318. CTF_CFG_0_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.11.2.419 CTF_CFG_0_PERID3 Register

CTF_CFG_0_PERID3 Register (Offset = FECh) [reset = 0h]

Register Description: Peripheral ID3 Register

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Table 14-29319. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FECh

Figure 14-9664. CTF_CFG_0_PERID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-29321. CTF_CFG_0_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.11.2.420 CTF_CFG_0_COMPID0 Register

CTF_CFG_0_COMPID0 Register (Offset = FF0h) [reset = 0h]

Register Description: Component ID0 Register

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Table 14-29322. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FF0h

Figure 14-9665. CTF_CFG_0_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-29324. CTF_CFG_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.421 CTF_CFG_0_COMPID1 Register

CTF_CFG_0_COMPID1 Register (Offset = FF4h) [reset = 0h]

Register Description: Component ID1 Register

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Table 14-29325. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FF4h

Figure 14-9666. CTF_CFG_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-29327. CTF_CFG_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.422 CTF_CFG_0_COMPID2 Register

CTF_CFG_0_COMPID2 Register (Offset = FF8h) [reset = 0h]

Register Description: Component ID2 Register

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Table 14-29328. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FF8h

Figure 14-9667. CTF_CFG_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMP_ID2							
R							
0h							

Table 14-29330. CTF_CFG_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.423 CTF_CFG_0_COMPID3 Register

CTF_CFG_0_COMPID3 Register (Offset = FFCh) [reset = 0h]

Register Description: Component ID3 Register

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Table 14-29331. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_0	7200 05FFCh

Figure 14-9668. CTF_CFG_0_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-29333. CTF_CFG_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.424 ROM_TABLE_0_1_ROM_ENTRY0 Register

ROM_TABLE_0_1_ROM_ENTRY0 Register (Offset = 0h) [reset = 2003h]

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Table 14-29334. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00000h

Figure 14-9669. ROM_TABLE_0_1_ROM_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
2h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
2h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-29336. ROM_TABLE_0_1_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.425 ROM_TABLE_0_1_ROM_ENTRY1 Register

ROM_TABLE_0_1_ROM_ENTRY1 Register (Offset = 4h) [reset = 2000003h]

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Table 14-29337. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00004h

Figure 14-9670. ROM_TABLE_0_1_ROM_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2000h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
2000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
2000h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-29339. ROM_TABLE_0_1_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.426 ROM_TABLE_0_1_ROM_ENTRY2 Register

ROM_TABLE_0_1_ROM_ENTRY2 Register (Offset = 8h) [reset = 3h]

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Table 14-29340. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00008h

Figure 14-9671. ROM_TABLE_0_1_ROM_ENTRY2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-29342. ROM_TABLE_0_1_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	RESERVED	NONE	0h	Reserved
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.427 ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register (Offset = 8h) [reset = 10h]

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Table 14-29343. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00008h

Figure 14-9672. ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29345. ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.428 ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register (Offset = Ch) [reset = 10h]

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Table 14-29346. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0000Ch

Figure 14-9673. ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29348. ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.429 ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register (Offset = 10h) [reset = 10h]

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Table 14-29349. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00010h

Figure 14-9674. ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29351. ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.430 ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register (Offset = 14h) [reset = 10h]

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Table 14-29352. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00014h

Figure 14-9675. ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29354. ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.431 ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register (Offset = 18h) [reset = 10h]

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Table 14-29355. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00018h

Figure 14-9676. ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29357. ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.432 ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register (Offset = 1Ch) [reset = 10h]

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Table 14-29358. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0001Ch

Figure 14-9677. ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29360. ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.433 ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register (Offset = 20h) [reset = 10h]

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Table 14-29361. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00020h

Figure 14-9678. ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29363. ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.434 ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register (Offset = 24h) [reset = 10h]

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Table 14-29364. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00024h

Figure 14-9679. ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29366. ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.435 ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register (Offset = 28h) [reset = 10h]

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Table 14-29367. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00028h

Figure 14-9680. ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29369. ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.436 ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register (Offset = 2Ch) [reset = 10h]

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Table 14-29370. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0002Ch

Figure 14-9681. ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29372. ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.437 ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register (Offset = 30h) [reset = 10h]

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Table 14-29373. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00030h

Figure 14-9682. ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29375. ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.438 ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register (Offset = 34h) [reset = 10h]

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Table 14-29376. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00034h

Figure 14-9683. ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29378. ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.439 ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register (Offset = 38h) [reset = 10h]

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Table 14-29379. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00038h

Figure 14-9684. ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29381. ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.440 ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register (Offset = 3Ch) [reset = 10h]

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Table 14-29382. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0003Ch

Figure 14-9685. ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29384. ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.441 ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register (Offset = 40h) [reset = 10h]

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Table 14-29385. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00040h

Figure 14-9686. ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29387. ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.442 ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register (Offset = 44h) [reset = 10h]

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Table 14-29388. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00044h

Figure 14-9687. ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29390. ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.443 ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register (Offset = 48h) [reset = 10h]

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Table 14-29391. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00048h

Figure 14-9688. ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29393. ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.444 ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register (Offset = 4Ch) [reset = 10h]

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Table 14-29394. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0004Ch

Figure 14-9689. ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29396. ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.445 ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register (Offset = 50h) [reset = 10h]

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Table 14-29397. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00050h

Figure 14-9690. ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29399. ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.446 ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register (Offset = 54h) [reset = 10h]

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Table 14-29400. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00054h

Figure 14-9691. ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29402. ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.447 ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register (Offset = 58h) [reset = 10h]

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Table 14-29403. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00058h

Figure 14-9692. ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29405. ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.448 ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register (Offset = 5Ch) [reset = 10h]

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Table 14-29406. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0005Ch

Figure 14-9693. ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29408. ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.449 ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register (Offset = 60h) [reset = 10h]

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Table 14-29409. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00060h

Figure 14-9694. ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29411. ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.450 ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register (Offset = 64h) [reset = 10h]

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Table 14-29412. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00064h

Figure 14-9695. ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29414. ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.451 ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register (Offset = 68h) [reset = 10h]

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Table 14-29415. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00068h

Figure 14-9696. ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29417. ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.452 ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register (Offset = 6Ch) [reset = 10h]

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Table 14-29418. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0006Ch

Figure 14-9697. ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29420. ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.453 ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register (Offset = 70h) [reset = 10h]

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Table 14-29421. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00070h

Figure 14-9698. ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29423. ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.454 ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register (Offset = 74h) [reset = 10h]

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Table 14-29424. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00074h

Figure 14-9699. ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29426. ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.455 ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register (Offset = 78h) [reset = 10h]

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Table 14-29427. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00078h

Figure 14-9700. ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29429. ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.456 ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register (Offset = 7Ch) [reset = 10h]

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Table 14-29430. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0007Ch

Figure 14-9701. ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29432. ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.457 ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register (Offset = 80h) [reset = 10h]

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Table 14-29433. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00080h

Figure 14-9702. ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29435. ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.458 ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register (Offset = 84h) [reset = 10h]

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Table 14-29436. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00084h

Figure 14-9703. ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29438. ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.459 ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register (Offset = 88h) [reset = 10h]

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Table 14-29439. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00088h

Figure 14-9704. ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29441. ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.460 ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register (Offset = 8Ch) [reset = 10h]

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Table 14-29442. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0008Ch

Figure 14-9705. ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29444. ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.461 ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register (Offset = 90h) [reset = 10h]

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Table 14-29445. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00090h

Figure 14-9706. ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29447. ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.462 ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register (Offset = 94h) [reset = 10h]

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Table 14-29448. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00094h

Figure 14-9707. ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29450. ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.463 ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register (Offset = 98h) [reset = 10h]

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Table 14-29451. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00098h

Figure 14-9708. ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29453. ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.464 ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register (Offset = 9Ch) [reset = 10h]

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Table 14-29454. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0009Ch

Figure 14-9709. ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29456. ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.465 ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register (Offset = A0h) [reset = 10h]

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Table 14-29457. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000A0h

Figure 14-9710. ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29459. ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.466 ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register (Offset = A4h) [reset = 10h]

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Table 14-29460. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000A4h

Figure 14-9711. ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29462. ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.467 ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register (Offset = A8h) [reset = 10h]

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Table 14-29463. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000A8h

Figure 14-9712. ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29465. ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.468 ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register (Offset = ACh) [reset = 10h]

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Table 14-29466. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000ACh

Figure 14-9713. ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29468. ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.469 ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register (Offset = B0h) [reset = 10h]

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Table 14-29469. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000B0h

Figure 14-9714. ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29471. ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.470 ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register (Offset = B4h) [reset = 10h]

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Table 14-29472. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000B4h

Figure 14-9715. ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29474. ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.471 ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register (Offset = B8h) [reset = 10h]

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Table 14-29475. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000B8h

Figure 14-9716. ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29477. ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.472 ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register (Offset = BCh) [reset = 10h]

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Table 14-29478. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000BCh

Figure 14-9717. ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29480. ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.473 ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register (Offset = C0h) [reset = 10h]

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Table 14-29481. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000C0h

Figure 14-9718. ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29483. ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.474 ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register (Offset = C4h) [reset = 10h]

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Table 14-29484. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000C4h

Figure 14-9719. ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29486. ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.475 ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register (Offset = C8h) [reset = 10h]

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Table 14-29487. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000C8h

Figure 14-9720. ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29489. ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.476 ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register (Offset = CCh) [reset = 10h]

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Table 14-29490. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000CCh

Figure 14-9721. ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29492. ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.477 ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register (Offset = D0h) [reset = 10h]

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Table 14-29493. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000D0h

Figure 14-9722. ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29495. ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.478 ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register (Offset = D4h) [reset = 10h]

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Table 14-29496. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000D4h

Figure 14-9723. ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29498. ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.479 ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register (Offset = D8h) [reset = 10h]

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Table 14-29499. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000D8h

Figure 14-9724. ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29501. ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.480 ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register (Offset = DCh) [reset = 10h]

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Table 14-29502. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000DCh

Figure 14-9725. ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29504. ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.481 ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register (Offset = E0h) [reset = 10h]

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Table 14-29505. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000E0h

Figure 14-9726. ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29507. ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.482 ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register (Offset = E4h) [reset = 10h]

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Table 14-29508. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000E4h

Figure 14-9727. ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29510. ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.483 ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register (Offset = E8h) [reset = 10h]

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Table 14-29511. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000E8h

Figure 14-9728. ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29513. ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.484 ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register (Offset = ECh) [reset = 10h]

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Table 14-29514. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000ECh

Figure 14-9729. ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29516. ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.485 ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register (Offset = F0h) [reset = 10h]

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Table 14-29517. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000F0h

Figure 14-9730. ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29519. ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.486 ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register (Offset = F4h) [reset = 10h]

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Table 14-29520. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000F4h

Figure 14-9731. ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29522. ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.487 ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register (Offset = F8h) [reset = 10h]

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Table 14-29523. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000F8h

Figure 14-9732. ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29525. ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.488 ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register (Offset = FCh) [reset = 10h]

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Table 14-29526. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 000FCh

Figure 14-9733. ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29528. ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.489 ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register (Offset = 100h) [reset = 10h]

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Table 14-29529. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00100h

Figure 14-9734. ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29531. ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.490 ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register

ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register (Offset = 104h) [reset = 10h]

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Table 14-29532. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00104h

Figure 14-9735. ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-29534. ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.11.2.491 ROM_TABLE_0_1_PERIPHID0 Register

ROM_TABLE_0_1_PERIPHID0 Register (Offset = 108h) [reset = 2h]

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Table 14-29535. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00108h

Figure 14-9736. ROM_TABLE_0_1_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29537. ROM_TABLE_0_1_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.492 ROM_TABLE_0_1_PERIPHID1 Register

ROM_TABLE_0_1_PERIPHID1 Register (Offset = 10Ch) [reset = 2h]

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Table 14-29538. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 0010Ch

Figure 14-9737. ROM_TABLE_0_1_PERIPHID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-29540. ROM_TABLE_0_1_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.493 ROM_TABLE_0_1_PERIPHID2 Register

ROM_TABLE_0_1_PERIPHID2 Register (Offset = 110h) [reset = 2h]

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Table 14-29541. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00110h

Figure 14-9738. ROM_TABLE_0_1_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29543. ROM_TABLE_0_1_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.494 ROM_TABLE_0_1_PERIPHID3 Register

ROM_TABLE_0_1_PERIPHID3 Register (Offset = 114h) [reset = 2h]

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Table 14-29544. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00114h

Figure 14-9739. ROM_TABLE_0_1_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29546. ROM_TABLE_0_1_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.495 ROM_TABLE_0_1_PERIPHID4 Register

ROM_TABLE_0_1_PERIPHID4 Register (Offset = 118h) [reset = 2h]

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Table 14-29547. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 00118h

Figure 14-9740. ROM_TABLE_0_1_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29549. ROM_TABLE_0_1_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.496 ROM_TABLE_0_1_COMPID0 Register

ROM_TABLE_0_1_COMPID0 Register (Offset = 3FCh) [reset = Dh]

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Table 14-29550. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 003FCh

Figure 14-9741. ROM_TABLE_0_1_COMPID0 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
Dh							
23	22	21	20	19	18	17	16
VAR							
R							
Dh							
15	14	13	12	11	10	9	8
VAR							
R							
Dh							
7	6	5	4	3	2	1	0
VAR							
R							
Dh							

Table 14-29552. ROM_TABLE_0_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	Dh	Component id0

14.11.2.497 ROM_TABLE_0_1_COMPID1 Register

ROM_TABLE_0_1_COMPID1 Register (Offset = 3FCh) [reset = 10h]

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Table 14-29553. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 003FCh

Figure 14-9742. ROM_TABLE_0_1_COMPID1 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
10h							
23	22	21	20	19	18	17	16
VAR							
R							
10h							
15	14	13	12	11	10	9	8
VAR							
R							
10h							
7	6	5	4	3	2	1	0
VAR							
R							
10h							

Table 14-29555. ROM_TABLE_0_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	10h	Component id1

14.11.2.498 ROM_TABLE_0_1_COMPID2 Register

ROM_TABLE_0_1_COMPID2 Register (Offset = 3FCh) [reset = 5h]

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Table 14-29556. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 003FCh

Figure 14-9743. ROM_TABLE_0_1_COMPID2 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
5h							
23	22	21	20	19	18	17	16
VAR							
R							
5h							
15	14	13	12	11	10	9	8
VAR							
R							
5h							
7	6	5	4	3	2	1	0
VAR							
R							
5h							

Table 14-29558. ROM_TABLE_0_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	5h	Component id2

14.11.2.499 ROM_TABLE_0_1_COMPID3 Register

ROM_TABLE_0_1_COMPID3 Register (Offset = 3FCh) [reset = B1h]

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Table 14-29559. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_0_1	7400 003FCh

Figure 14-9744. ROM_TABLE_0_1_COMPID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">B1h</td></tr>
</table>

Table 14-29561. ROM_TABLE_0_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	B1h	Component id3

14.11.2.500 CFGAP_CFG_1_JTAGID_REG Register

CFGAP_CFG_1_JTAGID_REG Register (Offset = 0h) [reset = 0h]

Register Description: This register returns the JTAG ID tieoff of the device. The reset value depends on the tie off

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Table 14-29562. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_1	7400 02000h

Figure 14-9745. CFGAP_CFG_1_JTAGID_REG Name Register

31	30	29	28	27	26	25	24
JTAG_ID							
R							
0h							
23	22	21	20	19	18	17	16
JTAG_ID							
R							
0h							
15	14	13	12	11	10	9	8
JTAG_ID							
R							
0h							
7	6	5	4	3	2	1	0
JTAG_ID							
R							
0h							

Table 14-29564. CFGAP_CFG_1_JTAGID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_ID	R	0h	The JTAG ID of the device

14.11.2.501 CFGAP_CFG_1_USERID_REG Register

CFGAP_CFG_1_USERID_REG Register (Offset = 4h) [reset = 0h]

Register Description: This register returns the Chip Spin ID tieoff value of the device. The reset value depends on the tieoff

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Table 14-29565. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_1	7400 02004h

Figure 14-9746. CFGAP_CFG_1_USERID_REG Name Register

31	30	29	28	27	26	25	24
USER_ID							
R							
0h							
23	22	21	20	19	18	17	16
USER_ID							
R							
0h							
15	14	13	12	11	10	9	8
USER_ID							
R							
0h							
7	6	5	4	3	2	1	0
USER_ID							
R							
0h							

Table 14-29567. CFGAP_CFG_1_USERID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USER_ID	R	0h	The USER ID of the device

14.11.2.502 CFGAP_CFG_1_VERSION_REG Register

CFGAP_CFG_1_VERSION_REG Register (Offset = 8h) [reset = 0h]

Register Description: This register is used to read the RTL version information and to determine which modules are included in the rtl build. The reset value depends on the build options

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Table 14-29568. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_1	7400 02008h

Figure 14-9747. CFGAP_CFG_1_VERSION_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">MAJOR_REV</td><td colspan="4">MINOR_REV</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>JTAG_AP</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>POWERAP</td><td>AXIAP</td><td>APBAP</td><td>SECURITYAP</td><td>SPARE</td><td>ICEPICKM</td><td>TRIGGERSUPPORT</td><td>TRACESUPPORT</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-29570. CFGAP_CFG_1_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	MAJOR_REV	R	0h	RTL Major revision [5]
27:24	MINOR_REV	R	0h	RTL Minor revision [0]
23:9	RESERVED	R	0h	Reserved, returns 0
8	JTAG_AP	R	0h	a 1 indicates JTAG AP is supported
7	POWERAP	R	0h	A 1 indicates that the Power AP is supported
6	AXIAP	R	0h	A 1 indicates that the AXIAP exists and system memory accesses are supported
5	APBAP	R	0h	A 1 indicates that the APBAP exisits and accesses to external debug logic are supported
4	SECURITYAP	R	0h	A 1 indicates that the Security AP is supported
3	SPARE	R	0h	This is a spare bit, returns 0
2	ICEPICKM	R	0h	A 1 indicates that ICEPick M is present inthe design
1	TRIGGERSUPPORT	R	0h	A 1 indicates that cross triggering is supported
0	TRACESUPPORT	R	0h	A 1 indicates that hardware trace export is supported

14.11.2.503 CFGAP_CFG_1_SYSTEMSTATUS Register

CFGAP_CFG_1_SYSTEMSTATUS Register (Offset = Ch) [reset = 0h]

Register Description: Reading this register returns system status information.

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Table 14-29571. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_1	7400 0200Ch

Figure 14-9748. CFGAP_CFG_1_SYSTEMSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-29573. CFGAP_CFG_1_SYSTEMSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved, returns 0

14.11.2.504 CFGAP_CFG_1_APID_REGISTER Register

CFGAP_CFG_1_APID_REGISTER Register (Offset = FCh) [reset = 20E0001h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29574. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cfgap_cfg_1	7400 020FCh

Figure 14-9749. CFGAP_CFG_1_APID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				107h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
107h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				1h			

Table 14-29576. CFGAP_CFG_1_APID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	107h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	1h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.505 APBAP_CFG_1_CSWREG Register

APBAP_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: Control/Status Register

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Table 14-29577. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 02100h

Figure 14-9750. APBAP_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29579. APBAP_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.506 APBAP_CFG_1_TAREG Register

APBAP_CFG_1_TAREG Register (Offset = 4h) [reset = 0h]

Register Description: This register contains the address to write to or read from.

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Table 14-29580. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 02104h

Figure 14-9751. APBAP_CFG_1_TAREG Name Register

31	30	29	28	27	26	25	24
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TRANSFER_ADDRESS_REGISTER							
R/W							
0h							

Table 14-29582. APBAP_CFG_1_TAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRANSFER_ADDRESS_REGISTER	R/W	0h	This register contains the address to write to or read from

14.11.2.507 APBAP_CFG_1_DRWREG Register

APBAP_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29583. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 0210Ch

Figure 14-9752. APBAP_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29585. APBAP_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.508 APBAP_CFG_1_BD0REG Register

APBAP_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29586. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 02110h

Figure 14-9753. APBAP_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29588. APBAP_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.509 APBAP_CFG_1_BD1REG Register

APBAP_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29589. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 02114h

Figure 14-9754. APBAP_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29591. APBAP_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.510 APBAP_CFG_1_BD2REG Register

APBAP_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29592. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 02118h

Figure 14-9755. APBAP_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29594. APBAP_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.511 APBAP_CFG_1_BD3REG Register

APBAP_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29595. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 0211Ch

Figure 14-9756. APBAP_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29597. APBAP_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.512 APBAP_CFG_1_ROM_REGISTER Register

APBAP_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the APB ROM Address.

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Table 14-29598. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 021F8h

Figure 14-9757. APBAP_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER_ADDRESS							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER_ADDRESS							
R							
0h							

Table 14-29600. APBAP_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER_ADDRESS	R	0h	Reading this register returns the APB ROM Address

14.11.2.513 APBAP_CFG_1_ID_REGISTER Register

APBAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29601. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_apbap_cfg_1	7400 021FCh

Figure 14-9758. APBAP_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29603. APBAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.11.2.514 AXIAP_CFG_1_CSWREG Register

AXIAP_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This is the control/status register

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Table 14-29604. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 02200h

Figure 14-9759. AXIAP_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
DBGSWEN	TYPEEXT						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
SPIDEN	RESERVED2						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
TYPE				MODE			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
TRINPROG	RESERVED1	ADDR_INC		RESERVED0	SIZE		
R	R	R/W		R	R		
0h	0h	0h		0h	0h		

Table 14-29606. AXIAP_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBGSWEN	R/W	0h	Indicates whether accesses should treated as application or debug
30:24	TYPEEXT	R/W	0h	
23	SPIDEN	R	0h	When 1, secure accesses are enabled
22:16	RESERVED2	R	0h	Reserved, reads return 0
15:12	TYPE	R/W	0h	Sets Prot, Type attributes for the access
11:8	MODE	R/W	0h	Sets mode of operation 0000=basic, 0001=Barrier extensions, all other values reserved
7	TRINPROG	R	0h	This bit is set to 1 while a transfer is in progress on the connection to the memory system, and is set to 0 while the connection is idle
6	RESERVED1	R	0h	This bit is reserved and reads return 0
5:4	ADDR_INC	R/W	0h	Address Auto Increment and packing mode
3	RESERVED0	R	0h	reserved, returns 0
2:0	SIZE	R	0h	This specifies the size of the access For this implementation, the access is always 32 bits [010]

14.11.2.515 AXIAP_CFG_1_TAREGL Register

AXIAP_CFG_1_TAREGL Register (Offset = 4h) [reset = 0h]

Register Description: This register contains the lower 32-bits of address to write to or read from.

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Table 14-29607. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 02204h

Figure 14-9760. AXIAP_CFG_1_TAREGL Name Register

31	30	29	28	27	26	25	24
TAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TAL							
R/W							
0h							

Table 14-29609. AXIAP_CFG_1_TAREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TAL	R/W	0h	This register contains the lower 32-bits of address

14.11.2.516 AXIAP_CFG_1_TAREGH Register

AXIAP_CFG_1_TAREGH Register (Offset = 8h) [reset = 0h]

Register Description: This register contains the upper 32-bits of address to write to or read from.

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Table 14-29610. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 02208h

Figure 14-9761. AXIAP_CFG_1_TAREGH Name Register

31	30	29	28	27	26	25	24
TAH							
R/W							
0h							
23	22	21	20	19	18	17	16
TAH							
R/W							
0h							
15	14	13	12	11	10	9	8
TAH							
R/W							
0h							
7	6	5	4	3	2	1	0
TAH							
R/W							
0h							

Table 14-29612. AXIAP_CFG_1_TAREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TAH	R/W	0h	This register contains the upper 32-bits of address

14.11.2.517 AXIAP_CFG_1_DRWREG Register

AXIAP_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29613. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 0220Ch

Figure 14-9762. AXIAP_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29615. AXIAP_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.518 AXIAP_CFG_1_BD0REG Register

AXIAP_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29616. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 02210h

Figure 14-9763. AXIAP_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29618. AXIAP_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.519 AXIAP_CFG_1_BD1REG Register

AXIAP_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29619. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 02214h

Figure 14-9764. AXIAP_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29621. AXIAP_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.520 AXIAP_CFG_1_BD2REG Register

AXIAP_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29622. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 02218h

Figure 14-9765. AXIAP_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29624. AXIAP_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.521 AXIAP_CFG_1_BD3REG Register

AXIAP_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29625. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 0221Ch

Figure 14-9766. AXIAP_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29627. AXIAP_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.522 AXIAP_CFG_1_MBT_REGISTER Register

AXIAP_CFG_1_MBT_REGISTER Register (Offset = 20h) [reset = 0h]

Register Description: This register sets memory barrier attributes

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Table 14-29628. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 02220h

Figure 14-9767. AXIAP_CFG_1_MBT_REGISTER Name Register

31	30	29	28	27	26	25	24
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							

Table 14-29630. AXIAP_CFG_1_MBT_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEMORY_BARRIER_TRANSFER_REGISTER	R/W	0h	This register sets memory barrier attributes

14.11.2.523 AXIAP_CFG_1_ROM_HI_REGISTER Register

AXIAP_CFG_1_ROM_HI_REGISTER Register (Offset = F0h) [reset = 0h]

Register Description: Reading this register returns the AXI ROM Address (63-32).

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Table 14-29631. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 022F0h

Figure 14-9768. AXIAP_CFG_1_ROM_HI_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_HI_REGISTER_ADDRESS							
R							
0h							
23	22	21	20	19	18	17	16
ROM_HI_REGISTER_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
ROM_HI_REGISTER_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
ROM_HI_REGISTER_ADDRESS							
R							
0h							

Table 14-29633. AXIAP_CFG_1_ROM_HI_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_HI_REGISTER_ADDRESS	R	0h	Reading this register returns the upper ROM Address

14.11.2.524 AXIAP_CFG_1_CFG_REGISTER Register

AXIAP_CFG_1_CFG_REGISTER Register (Offset = F4h) [reset = 0h]

Register Description: The CFG register provides information about how the MEM-AP implementation is configured.

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Table 14-29634. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 022F4h

Figure 14-9769. AXIAP_CFG_1_CFG_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					LD	LA	BE
R					R	R	R
0h					0h	0h	0h

Table 14-29636. AXIAP_CFG_1_CFG_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved bit, return 0
2	LD	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Data Extension, that provides support for data items larger than 32-bits, it is 0
1	LA	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Physical Address Extension, that supports physical addresses of more than 32-bits:
0	BE	R	0h	ADIv52 obsoletes support for big-endian MEM-AP, and this bit must RAZ

14.11.2.525 AXIAP_CFG_1_ROM_LO_REGISTER Register

AXIAP_CFG_1_ROM_LO_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AXI ROM Address (31:12) .

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Table 14-29637. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 022F8h

Figure 14-9770. AXIAP_CFG_1_ROM_LO_REGISTER Name Register

31	30	29	28	27	26	25	24
LOWBASE							
R							
0h							
23	22	21	20	19	18	17	16
LOWBASE							
R							
0h							
15	14	13	12	11	10	9	8
LOWBASE				RESERVED			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED						FORMAT	PRESENT
R						R	R
0h						0h	0h

Table 14-29639. AXIAP_CFG_1_ROM_LO_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	LOWBASE	R	0h	Bits 31:12 of the base address
11:2	RESERVED	R	0h	Reserved, returns 0
1	FORMAT	R	0h	Base address register format [0]
0	PRESENT	R	0h	This field indicates whether a debug entry is present for this MEM-AP: 0 No debug entry present 1 Debug entry present

14.11.2.526 AXIAP_CFG_1_ID_REGISTER Register

AXIAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29640. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_axiap_cfg_1	7400 022FCh

Figure 14-9771. AXIAP_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			

23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h

15	14	13	12	11	10	9	8
SPARE							
R							
0h							

7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29642. AXIAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB, 4=AXI [4]

14.11.2.527 PWRAP_CFG_1_CORE_PRECREG0 Register

PWRAP_CFG_1_CORE_PRECREG0 Register (Offset = 0h) [reset = 0h]

Register Description: These registers are used to control functionality of CPUs without JTAG ports. There can be upto 32 of these registers

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Table 14-29643. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pwrap_cfg_1	7400 02300h

Figure 14-9772. PWRAP_CFG_1_CORE_PRECREG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RETENTION	RST_OCCURED	PWR_LOSS_DET	INHIBIT_SLEEP	DEBUG_POWER	UNNAT_RESET	IN_RESET_RLS_WIR	RESET_MODE
R	R/W	R/W	R/W	R/W	R	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
RESET_MODE		DEBUG_ENABLE	RSV11_12		EXEC_ACTION_DEBUG_ATTEN	RSV8_9	
R/W		R/W	R		R/W	R	
0h		0h	0h		0h	0h	

7	6	5	4	3	2	1	0
PWRDOWNSRD	RSV6	POWERED	CLKDOWNDSRD	FORCE_ACTIVE	CLOCKED	SECURITY	PRESENT
R	R	R	R	R/W	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-29645. PWRAP_CFG_1_CORE_PRECREG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23	RETENTION	R	0h	Core is in retention mode
22	RST_OCCURED	R/W	0h	Sticky bit indicating a reset has occured Write 1 to clear this bit
21	PWR_LOSS_DET	R/W	0h	Power Loss Detected Sticky bit, write a 1 to clear this bit
20	INHIBIT_SLEEP	R/W	0h	Inhinit Sleep Block core from entering sleep mode
19	DEBUG_POWER	R/W	0h	Core debug logic is powered
18	UNNAT_RESET	R	0h	Unnatural Reset Device reset state is being affected by debug logic
17	IN_RESET_RLS_WIR	R/W	0h	Writing a 1 releases the WIR When read this returns the reset status, 1 indicates core is in reset
16:14	RESET_MODE	R/W	0h	Reset Mode 0=normal, 1=WIR, 2=Blk Rst, 3=Blk Assert, 4=Halt on Rst, 5=Cancel, 6=Halt and Block, 7=Halt-Blk-assert
13	DEBUG_ENABLE	R/W	0h	Debug Enabled signal to the core
12:11	RSV11_12	R	0h	Reserved, return 0
10	EXEC_ACTION_DEBUG_ATTEN	R/W	0h	Writing this bit causes Execution Read will return the Debug Attention input value

Table 14-29645. PWRAP_CFG_1_CORE_PRECREG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	RSV8_9	R	0h	Reserved, returns 0 when read
7	PWRDOWNDSRD	R	0h	The core wants to turn off it's power when high
6	RSV6	R	0h	Reserved, returns 0 when read
5	POWERED	R	0h	Core is powered up when high
4	CLKDOWNDSRD	R	0h	The core wants to turn off it's clock when high
3	FORCE_ACTIVE	R/W	0h	Force core active Turn on power and clocks
2	CLOCKED	R	0h	When high the core clock is active
1	SECURITY	R	0h	Security bit When high security is allowing access
0	PRESENT	R	0h	The core controlled by this register exists when 1

14.11.2.528 PWRAP_CFG_1_CORE_PRECREG1 Register

14.11.2.529 PWRAP_CFG_1_CORE_PRECREG2 Register

14.11.2.530 PWRAP_CFG_1_CORE_PRECREG3 Register

14.11.2.531 PWRAP_CFG_1_CORE_PRECREG4 Register

14.11.2.532 PWRAP_CFG_1_CORE_PRECREG5 Register

14.11.2.533 PWRAP_CFG_1_CORE_PRECREG6 Register

14.11.2.534 PWRAP_CFG_1_CORE_PRECREG7 Register

14.11.2.535 PWRAP_CFG_1_CORE_PRECREG8 Register

14.11.2.536 PWRAP_CFG_1_CORE_PRECREG9 Register

14.11.2.537 PWRAP_CFG_1_CORE_PRECREG10 Register

14.11.2.538 PWRAP_CFG_1_CORE_PRECREG11 Register

14.11.2.539 PWRAP_CFG_1_CORE_PRECREG12 Register

14.11.2.540 PWRAP_CFG_1_CORE_PRECREG13 Register

14.11.2.541 PWRAP_CFG_1_CORE_PRECREG14 Register

14.11.2.542 PWRAP_CFG_1_CORE_PRECREG15 Register

14.11.2.543 PWRAP_CFG_1_CORE_PRECREG16 Register

14.11.2.544 PWRAP_CFG_1_CORE_PRECREG17 Register

14.11.2.545 PWRAP_CFG_1_CORE_PRECREG18 Register

14.11.2.546 PWRAP_CFG_1_CORE_PRECREG19 Register

14.11.2.547 PWRAP_CFG_1_CORE_PRECREG20 Register

14.11.2.548 PWRAP_CFG_1_CORE_PRECREG21 Register

14.11.2.549 PWRAP_CFG_1_CORE_PRECREG22 Register

14.11.2.550 PWRAP_CFG_1_CORE_PRECREG23 Register

14.11.2.551 PWRAP_CFG_1_CORE_PRECREG24 Register

14.11.2.552 PWRAP_CFG_1_CORE_PRECREG25 Register

14.11.2.553 PWRAP_CFG_1_CORE_PRECREG26 Register

14.11.2.554 PWRAP_CFG_1_CORE_PRECREG27 Register

14.11.2.555 PWRAP_CFG_1_CORE_PRECREG28 Register

14.11.2.556 PWRAP_CFG_1_CORE_PRECREG29 Register

14.11.2.557 PWRAP_CFG_1_CORE_PRECREG30 Register

14.11.2.558 PWRAP_CFG_1_CORE_PRECREG31 Register

14.11.2.559 PWRAP_CFG_1_SYS_PRECREG Register

PWRAP_CFG_1_SYS_PRECREG Register (Offset = F0h) [reset = 0h]

Register Description: This register is used to control system level functionality

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Table 14-29646. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pwrap_cfg_1	7400 023F0h

Figure 14-9773. PWRAP_CFG_1_SYS_PRECREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>DBGCON_WE</td><td colspan="4">DBGCON</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>UNNAT_RESET</td><td>RST_OCCURED</td><td>SYSTEM_STAT</td><td>RSV12_BIT</td><td>GLOB_EXEC_TRIG</td><td>CLR_EX_FLAGS</td><td>GLOB_EXEC_MSK</td><td>IN_RESET_RLS_WIR</td></tr>
<tr><td>R</td><td>R/W</td><td>R</td><td>R</td><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>WIR_REQ</td><td>BLK_SYS_RST</td><td colspan="2">RESERVED0</td><td colspan="3">DEV_TYPE</td><td>SYS_RST_REQ</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-29648. PWRAP_CFG_1_SYS_PRECREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	R	0h	Reserved, returns 0
20	DBGCON_WE	R/W	0h	This bit must be high to write to the debug connect field
19:16	DBGCON	R/W	0h	The system debugger must write a value of 0x9 to be connected and access the debug logic
15	UNNAT_RESET	R	0h	Unnatural Reset Device reset state is being affected by debug logic
14	RST_OCCURED	R/W	0h	Sticky bit indicating a reset has occured Write 1 to clear this bit
13	SYSTEM_STAT	R	0h	System Status input, application specificall
12	RSV12_BIT	R	0h	Reserved, read returns 0
11	GLOB_EXEC_TRIG	R	0h	
10	CLR_EX_FLAGS	R/W	0h	Clear all run flags
9	GLOB_EXEC_MSK	R/W	0h	Global Execute Mask
8	IN_RESET_RLS_WIR	R/W	0h	Writing a 1 releases the global WIR When read this returns the in reset status
7	WIR_REQ	R/W	0h	Wait In Reset Request
6	BLK_SYS_RST	R/W	0h	Block System Reset
5:4	RESERVED0	R	0h	Reserved0, returns 0
3:1	DEV_TYPE	R	0h	Device Type tieoff value Test, emulator, secure, etc

Table 14-29648. PWRAP_CFG_1_SYS_PRECREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYS_RST_REQ	R/W	0h	System Reset Request This bit will be reset once reset occurs

14.11.2.560 PWRAP_CFG_1_ID_REGISTER Register

PWRAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29649. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pwrap_cfg_1	7400 023FCh

Figure 14-9774. PWRAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29651. PWRAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	0h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.11.2.561 PVIEW_CFG_1_PVIEW_STATE0 Register

PVIEW_CFG_1_PVIEW_STATE0 Register (Offset = 0h) [reset = 0h]

Register Description: This register provides the device specific power status. A read of Power View State Register will lock the values for all other Power View State Registers. A read from the last Power View State register will unlock them so they can update

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Table 14-29652. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pview_cfg_1	7400 02400h

Figure 14-9775. PVIEW_CFG_1_PVIEW_STATE0 Name Register

31	30	29	28	27	26	25	24
POWER_VIEW_STATE_REG0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
POWER_VIEW_STATE_REG0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POWER_VIEW_STATE_REG0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POWER_VIEW_STATE_REG0							
R							
0h							

Table 14-29654. PVIEW_CFG_1_PVIEW_STATE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POWER_VIEW_STATE_REG0	R	0h	

14.11.2.562 PVIEW_CFG_1_PVIEW_CAPABILITY Register

PVIEW_CFG_1_PVIEW_CAPABILITY Register (Offset = F0h) [reset = 0h]

Register Description: The Capability Register provides information on the number of Power State registers implemented in the AP

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Table 14-29655. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pview_cfg_1	7400 024F0h

Figure 14-9776. PVIEW_CFG_1_PVIEW_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		NUMSTATREG					
R		R					
0h		0h					

Table 14-29657. PVIEW_CFG_1_PVIEW_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved, returns 0
5:0	NUMSTATREG	R	0h	The value read indicates the number of valid Power State Registers that are implemented in the system The maximum number is 60 and the minimum number is 1 The registers are always implemented at contiguous addresses so a value of 7 means that registers 0-6 are valid

14.11.2.563 PVIEW_CFG_1_ID_REGISTER Register

PVIEW_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29658. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_pview_cfg_1	7400 024FCh

Figure 14-9777. PVIEW_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29660. PVIEW_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	0h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type = 3

14.11.2.564 JTAGAP_CFG_1_CSW Register

JTAGAP_CFG_1_CSW Register (Offset = 0h) [reset = 0h]

Register Description: This register provides control and status information

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Table 14-29661. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_1	7400 02500h

Figure 14-9778. JTAGAP_CFG_1_CSW Name Register

31	30	29	28	27	26	25	24
SERACTV	WFIFOCNT			RSV27	RFIFOCNT		
R	R			R	R		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				PORT_CONNECTED_STATUS	SRST_STATUS	TRST_ASSERT	SRST_ASSERT
R				R	R	R/W	R/W
0h				0h	0h	0h	0h

Table 14-29663. JTAGAP_CFG_1_CSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SERACTV	R	0h	JTAG Serializer active
30:28	WFIFOCNT	R	0h	Outstanding Write FIFO Byte Count
27	RSV27	R	0h	Reserved, returns 0
26:24	RFIFOCNT	R	0h	Outstanding Read FIFO Byte Count
23:4	RESERVED	R	0h	Reserved, returns 0
3	PORT_CONNECTED_STATUS	R	0h	Reading this returns the Port connected status of the selected port
2	SRST_STATUS	R	0h	Reading this returns the SRST status of the selected port If multiple ports are selected, it is the AND of all the SRSTCONNECTED inputs from the selected ports
1	TRST_ASSERT	R/W	0h	Writing a 1 causes TRST to be asserted
0	SRST_ASSERT	R/W	0h	Writing a 1 causes SRST to be asserted

14.11.2.565 JTAGAP_CFG_1_PSEL_REG Register

JTAGAP_CFG_1_PSEL_REG Register (Offset = 4h) [reset = 0h]

Register Description: This 8-bit register is used to select the JTAG port.

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Table 14-29664. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_1	7400 02504h

Figure 14-9779. JTAGAP_CFG_1_PSEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_SELECT_REGISTER							
R/W							
0h							

Table 14-29666. JTAGAP_CFG_1_PSEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	read as 0
7:0	PORT_SELECT_REGISTER	R/W	0h	

14.11.2.566 JTAGAP_CFG_1_PSTA_REG Register

JTAGAP_CFG_1_PSTA_REG Register (Offset = 8h) [reset = 0h]

Register Description: A bit value of 1 indicates that a selected and enabled port has gone inactive. These bits are sticky. Writing a 1 to them clears them.

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Table 14-29667. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_1	7400 02508h

Figure 14-9780. JTAGAP_CFG_1_PSTA_REG Name Register

31	30	29	28	27	26	25	24
PORT_STATUS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
PORT_STATUS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
PORT_STATUS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_STATUS_REGISTER							
R/W							
0h							

Table 14-29669. JTAGAP_CFG_1_PSTA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_STATUS_REGISTER	R/W	0h	

14.11.2.567 JTAGAP_CFG_1_BYTEFIFO1 Register

JTAGAP_CFG_1_BYTEFIFO1 Register (Offset = 10h) [reset = 0h]

Register Description: Reading this location reads a byte from the FIFO. Writing it loads a byte into the FIFO. Reset value is UNDEFINED

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Table 14-29670. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_1	7400 02510h

Figure 14-9781. JTAGAP_CFG_1_BYTEFIFO1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_1							
R/W							
0h							

Table 14-29672. JTAGAP_CFG_1_BYTEFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	
7:0	BYTE_FIFO_1	R/W	0h	

14.11.2.568 JTAGAP_CFG_1_BYTEFIFO2 Register

JTAGAP_CFG_1_BYTEFIFO2 Register (Offset = 14h) [reset = 0h]

Register Description: Reading this location reads a 16 bits from the FIFO. Writing it loads 16 bits into the FIFO. Reset value is UNDEFINED

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Table 14-29673. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_1	7400 02514h

Figure 14-9782. JTAGAP_CFG_1_BYTEFIFO2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_2							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_2							
R/W							
0h							

Table 14-29675. JTAGAP_CFG_1_BYTEFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	
15:0	BYTE_FIFO_2	R/W	0h	

14.11.2.569 JTAGAP_CFG_1_BYTEFIFO3 Register

JTAGAP_CFG_1_BYTEFIFO3 Register (Offset = 18h) [reset = 0h]

Register Description: Reading this location reads a 24 bits from the FIFO. Writing it loads 24 bits into the FIFO. Reset value is UNDEFINED

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Table 14-29676. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_1	7400 02518h

Figure 14-9783. JTAGAP_CFG_1_BYTEFIFO3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_3							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_3							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_3							
R/W							
0h							

Table 14-29678. JTAGAP_CFG_1_BYTEFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R/W	0h	
23:0	BYTE_FIFO_3	R/W	0h	

14.11.2.570 JTAGAP_CFG_1_BYTEFIFO4 Register

JTAGAP_CFG_1_BYTEFIFO4 Register (Offset = 1Ch) [reset = 0h]

Register Description: Reading this location reads a 32 bits from the FIFO. Writing it loads 32 bits into the FIFO. Reset value is UNDEFINED

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Table 14-29679. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_1	7400 0251Ch

Figure 14-9784. JTAGAP_CFG_1_BYTEFIFO4 Name Register

31	30	29	28	27	26	25	24
BYTE_FIFO_4							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_4							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_4							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_4							
R/W							
0h							

Table 14-29681. JTAGAP_CFG_1_BYTEFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BYTE_FIFO_4	R/W	0h	

14.11.2.571 JTAGAP_CFG_1_ID_REGISTER Register

JTAGAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29682. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_jtagap_cfg_1	7400 025FCh

Figure 14-9785. JTAGAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29684. JTAGAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [1]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [0]

14.11.2.572 SECAP_CFG_1_TXDATA Register

SECAP_CFG_1_TXDATA Register (Offset = 0h) [reset = 0h]

Register Description: Data value to send to security controller. Apllication specific

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Table 14-29685. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_secap_cfg_1	7400 02600h

Figure 14-9786. SECAP_CFG_1_TXDATA Name Register

31	30	29	28	27	26	25	24
TX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_DATA_REGISTER							
R/W							
0h							

Table 14-29687. SECAP_CFG_1_TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TX_DATA_REGISTER	R/W	0h	

14.11.2.573 SECAP_CFG_1_TXCTRL Register

SECAP_CFG_1_TXCTRL Register (Offset = 4h) [reset = 0h]

Register Description: Register to send control information to the Security Controller, Application specific

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Table 14-29688. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_secap_cfg_1	7400 02604h

Figure 14-9787. SECAP_CFG_1_TXCTRL Name Register

31	30	29	28	27	26	25	24
TX_CONTROL							
R/W							
0h							
23	22	21	20	19	18	17	16
TX_CONTROL							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_CONTROL							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_CONTROL							TXDAV
R/W							R
0h							0h

Table 14-29690. SECAP_CFG_1_TXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	TX_CONTROL	R/W	0h	31 bits to send to security controller, Application specific
0	TXDAV	R	0h	TX Data Available

14.11.2.574 SECAP_CFG_1_RXDATA Register

SECAP_CFG_1_RXDATA Register (Offset = 8h) [reset = 0h]

Register Description: Data value from the security controller. Apllication specific

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Table 14-29691. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_secap_cfg_1	7400 02608h

Figure 14-9788. SECAP_CFG_1_RXDATA Name Register

31	30	29	28	27	26	25	24
RX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
RX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_DATA_REGISTER							
R/W							
0h							

Table 14-29693. SECAP_CFG_1_RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RX_DATA_REGISTER	R/W	0h	

14.11.2.575 SECAP_CFG_1_RXCTRL Register

SECAP_CFG_1_RXCTRL Register (Offset = Ch) [reset = 0h]

Register Description: Register to receive control information from the Security Controller

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Table 14-29694. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_secap_cfg_1	7400 0260Ch

Figure 14-9789. SECAP_CFG_1_RXCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RX_CONTROL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_CONTROL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RX_CONTROL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RX_CONTROL</td><td>RXDAV</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-29696. SECAP_CFG_1_RXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RX_CONTROL	R	0h	31 bits from the security controller, Application specific
0	RXDAV	R	0h	TX Data Available

14.11.2.576 CORTEX0_CFG_1_CSWREG Register

CORTEX0_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29697. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_1	7400 02700h

Figure 14-9790. CORTEX0_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29699. CORTEX0_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.577 CORTEX0_CFG_1_TAREG Register

14.11.2.578 CORTEX0_CFG_1_DRWREG Register

CORTEX0_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29700. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_1	7400 0270Ch

Figure 14-9791. CORTEX0_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29702. CORTEX0_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.579 CORTEX0_CFG_1_BD0REG Register

CORTEX0_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29703. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_1	7400 02710h

Figure 14-9792. CORTEX0_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29705. CORTEX0_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.580 CORTEX0_CFG_1_BD1REG Register

CORTEX0_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29706. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_1	7400 02714h

Figure 14-9793. CORTEX0_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29708. CORTEX0_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.581 CORTEX0_CFG_1_BD2REG Register

CORTEX0_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29709. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_1	7400 02718h

Figure 14-9794. CORTEX0_CFG_1_BD2REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29711. CORTEX0_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.582 CORTEX0_CFG_1_BD3REG Register

CORTEX0_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29712. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_1	7400 0271Ch

Figure 14-9795. CORTEX0_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29714. CORTEX0_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.583 CORTEX0_CFG_1_ROM_REGISTER Register

CORTEX0_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29715. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_1	7400 027F8h

Figure 14-9796. CORTEX0_CFG_1_ROM_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29717. CORTEX0_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.584 CORTEX0_CFG_1_ID_REGISTER Register

CORTEX0_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29718. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex0_cfg_1	7400 027FCh

Figure 14-9797. CORTEX0_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29720. CORTEX0_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.585 CORTEX1_CFG_1_CSWREG Register

CORTEX1_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29721. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_1	7400 02800h

Figure 14-9798. CORTEX1_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-29723. CORTEX1_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.586 CORTEX1_CFG_1_TAREG Register

14.11.2.587 CORTEX1_CFG_1_DRWREG Register

CORTEX1_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29724. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_1	7400 0280Ch

Figure 14-9799. CORTEX1_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29726. CORTEX1_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.588 CORTEX1_CFG_1_BD0REG Register

CORTEX1_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29727. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_1	7400 02810h

Figure 14-9800. CORTEX1_CFG_1_BD0REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29729. CORTEX1_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.589 CORTEX1_CFG_1_BD1REG Register

CORTEX1_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29730. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_1	7400 02814h

Figure 14-9801. CORTEX1_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29732. CORTEX1_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.590 CORTEX1_CFG_1_BD2REG Register

CORTEX1_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29733. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_1	7400 02818h

Figure 14-9802. CORTEX1_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29735. CORTEX1_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.591 CORTEX1_CFG_1_BD3REG Register

CORTEX1_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29736. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_1	7400 0281Ch

Figure 14-9803. CORTEX1_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29738. CORTEX1_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.592 CORTEX1_CFG_1_ROM_REGISTER Register

CORTEX1_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29739. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_1	7400 028F8h

Figure 14-9804. CORTEX1_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-29741. CORTEX1_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.593 CORTEX1_CFG_1_ID_REGISTER Register

CORTEX1_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29742. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex1_cfg_1	7400 028FCh

Figure 14-9805. CORTEX1_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29744. CORTEX1_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.594 CORTEX2_CFG_1_CSWREG Register

CORTEX2_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29745. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_1	7400 02900h

Figure 14-9806. CORTEX2_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-29747. CORTEX2_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.595 CORTEX2_CFG_1_TAREG Register

14.11.2.596 CORTEX2_CFG_1_DRWREG Register

CORTEX2_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29748. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_1	7400 0290Ch

Figure 14-9807. CORTEX2_CFG_1_DRWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29750. CORTEX2_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.597 CORTEX2_CFG_1_BD0REG Register

CORTEX2_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29751. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_1	7400 02910h

Figure 14-9808. CORTEX2_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29753. CORTEX2_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.598 CORTEX2_CFG_1_BD1REG Register

CORTEX2_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29754. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_1	7400 02914h

Figure 14-9809. CORTEX2_CFG_1_BD1REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_1_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_1_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_1_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_1_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29756. CORTEX2_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.599 CORTEX2_CFG_1_BD2REG Register

CORTEX2_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29757. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_1	7400 02918h

Figure 14-9810. CORTEX2_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29759. CORTEX2_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.600 CORTEX2_CFG_1_BD3REG Register

CORTEX2_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29760. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_1	7400 0291Ch

Figure 14-9811. CORTEX2_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29762. CORTEX2_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.601 CORTEX2_CFG_1_ROM_REGISTER Register

CORTEX2_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29763. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_1	7400 029F8h

Figure 14-9812. CORTEX2_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-29765. CORTEX2_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.602 CORTEX2_CFG_1_ID_REGISTER Register

CORTEX2_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29766. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex2_cfg_1	7400 029FCh

Figure 14-9813. CORTEX2_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29768. CORTEX2_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.603 CORTEX3_CFG_1_CSWREG Register

CORTEX3_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29769. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_1	7400 02A00h

Figure 14-9814. CORTEX3_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29771. CORTEX3_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.604 CORTEX3_CFG_1_TAREG Register

14.11.2.605 CORTEX3_CFG_1_DRWREG Register

CORTEX3_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29772. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_1	7400 02A0Ch

Figure 14-9815. CORTEX3_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29774. CORTEX3_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.606 CORTEX3_CFG_1_BD0REG Register

CORTEX3_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29775. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_1	7400 02A10h

Figure 14-9816. CORTEX3_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29777. CORTEX3_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.607 CORTEX3_CFG_1_BD1REG Register

CORTEX3_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29778. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_1	7400 02A14h

Figure 14-9817. CORTEX3_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29780. CORTEX3_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.608 CORTEX3_CFG_1_BD2REG Register

CORTEX3_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29781. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_1	7400 02A18h

Figure 14-9818. CORTEX3_CFG_1_BD2REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29783. CORTEX3_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.609 CORTEX3_CFG_1_BD3REG Register

CORTEX3_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29784. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_1	7400 02A1Ch

Figure 14-9819. CORTEX3_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29786. CORTEX3_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.610 CORTEX3_CFG_1_ROM_REGISTER Register

CORTEX3_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29787. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_1	7400 02AF8h

Figure 14-9820. CORTEX3_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-29789. CORTEX3_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.611 CORTEX3_CFG_1_ID_REGISTER Register

CORTEX3_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29790. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex3_cfg_1	7400 02AFCh

Figure 14-9821. CORTEX3_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29792. CORTEX3_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.612 CORTEX4_CFG_1_CSWREG Register

CORTEX4_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29793. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_1	7400 02B00h

Figure 14-9822. CORTEX4_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-29795. CORTEX4_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.613 CORTEX4_CFG_1_TAREG Register

14.11.2.614 CORTEX4_CFG_1_DRWREG Register

CORTEX4_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29796. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_1	7400 02B0Ch

Figure 14-9823. CORTEX4_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29798. CORTEX4_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.615 CORTEX4_CFG_1_BD0REG Register

CORTEX4_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29799. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_1	7400 02B10h

Figure 14-9824. CORTEX4_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29801. CORTEX4_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.616 CORTEX4_CFG_1_BD1REG Register

CORTEX4_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29802. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_1	7400 02B14h

Figure 14-9825. CORTEX4_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29804. CORTEX4_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.617 CORTEX4_CFG_1_BD2REG Register

CORTEX4_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29805. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_1	7400 02B18h

Figure 14-9826. CORTEX4_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29807. CORTEX4_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.618 CORTEX4_CFG_1_BD3REG Register

CORTEX4_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29808. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_1	7400 02B1Ch

Figure 14-9827. CORTEX4_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29810. CORTEX4_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.619 CORTEX4_CFG_1_ROM_REGISTER Register

CORTEX4_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29811. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_1	7400 02BF8h

Figure 14-9828. CORTEX4_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-29813. CORTEX4_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.620 CORTEX4_CFG_1_ID_REGISTER Register

CORTEX4_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29814. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex4_cfg_1	7400 02BFCh

Figure 14-9829. CORTEX4_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29816. CORTEX4_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.621 CORTEX5_CFG_1_CSWREG Register

CORTEX5_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29817. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_1	7400 02C00h

Figure 14-9830. CORTEX5_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29819. CORTEX5_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.622 CORTEX5_CFG_1_TAREG Register

14.11.2.623 CORTEX5_CFG_1_DRWREG Register

CORTEX5_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29820. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_1	7400 02C0Ch

Figure 14-9831. CORTEX5_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29822. CORTEX5_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.624 CORTEX5_CFG_1_BD0REG Register

CORTEX5_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29823. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_1	7400 02C10h

Figure 14-9832. CORTEX5_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29825. CORTEX5_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.625 CORTEX5_CFG_1_BD1REG Register

CORTEX5_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29826. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_1	7400 02C14h

Figure 14-9833. CORTEX5_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29828. CORTEX5_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.626 CORTEX5_CFG_1_BD2REG Register

CORTEX5_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29829. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_1	7400 02C18h

Figure 14-9834. CORTEX5_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29831. CORTEX5_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.627 CORTEX5_CFG_1_BD3REG Register

CORTEX5_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29832. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_1	7400 02C1Ch

Figure 14-9835. CORTEX5_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29834. CORTEX5_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.628 CORTEX5_CFG_1_ROM_REGISTER Register

CORTEX5_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29835. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_1	7400 02CF8h

Figure 14-9836. CORTEX5_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-29837. CORTEX5_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.629 CORTEX5_CFG_1_ID_REGISTER Register

CORTEX5_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29838. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex5_cfg_1	7400 02CFCh

Figure 14-9837. CORTEX5_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29840. CORTEX5_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.630 CORTEX6_CFG_1_CSWREG Register

CORTEX6_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29841. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_1	7400 02D00h

Figure 14-9838. CORTEX6_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-29843. CORTEX6_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.631 CORTEX6_CFG_1_TAREG Register

14.11.2.632 CORTEX6_CFG_1_DRWREG Register

CORTEX6_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29844. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_1	7400 02D0Ch

Figure 14-9839. CORTEX6_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29846. CORTEX6_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.633 CORTEX6_CFG_1_BD0REG Register

CORTEX6_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29847. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_1	7400 02D10h

Figure 14-9840. CORTEX6_CFG_1_BD0REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-29849. CORTEX6_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.634 CORTEX6_CFG_1_BD1REG Register

CORTEX6_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29850. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_1	7400 02D14h

Figure 14-9841. CORTEX6_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29852. CORTEX6_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.635 CORTEX6_CFG_1_BD2REG Register

CORTEX6_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29853. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_1	7400 02D18h

Figure 14-9842. CORTEX6_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29855. CORTEX6_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.636 CORTEX6_CFG_1_BD3REG Register

CORTEX6_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29856. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_1	7400 02D1Ch

Figure 14-9843. CORTEX6_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29858. CORTEX6_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.637 CORTEX6_CFG_1_ROM_REGISTER Register

CORTEX6_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29859. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_1	7400 02DF8h

Figure 14-9844. CORTEX6_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-29861. CORTEX6_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.638 CORTEX6_CFG_1_ID_REGISTER Register

CORTEX6_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29862. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex6_cfg_1	7400 02DFCh

Figure 14-9845. CORTEX6_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29864. CORTEX6_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.639 CORTEX7_CFG_1_CSWREG Register

CORTEX7_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29865. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_1	7400 02E00h

Figure 14-9846. CORTEX7_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29867. CORTEX7_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.640 CORTEX7_CFG_1_TAREG Register

14.11.2.641 CORTEX7_CFG_1_DRWREG Register

CORTEX7_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29868. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_1	7400 02E0Ch

Figure 14-9847. CORTEX7_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29870. CORTEX7_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.642 CORTEX7_CFG_1_BD0REG Register

CORTEX7_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29871. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_1	7400 02E10h

Figure 14-9848. CORTEX7_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29873. CORTEX7_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.643 CORTEX7_CFG_1_BD1REG Register

CORTEX7_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29874. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_1	7400 02E14h

Figure 14-9849. CORTEX7_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29876. CORTEX7_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.644 CORTEX7_CFG_1_BD2REG Register

CORTEX7_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29877. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_1	7400 02E18h

Figure 14-9850. CORTEX7_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29879. CORTEX7_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.645 CORTEX7_CFG_1_BD3REG Register

CORTEX7_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29880. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_1	7400 02E1Ch

Figure 14-9851. CORTEX7_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29882. CORTEX7_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.646 CORTEX7_CFG_1_ROM_REGISTER Register

CORTEX7_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29883. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_1	7400 02EF8h

Figure 14-9852. CORTEX7_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-29885. CORTEX7_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.647 CORTEX7_CFG_1_ID_REGISTER Register

CORTEX7_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29886. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex7_cfg_1	7400 02EFCh

Figure 14-9853. CORTEX7_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-29888. CORTEX7_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.648 CORTEX8_CFG_1_CSWREG Register

CORTEX8_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Register Description: This register contains the Addressing control bit

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Table 14-29889. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_1	7400 02F00h

Figure 14-9854. CORTEX8_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29891. CORTEX8_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.11.2.649 CORTEX8_CFG_1_TAREG Register

14.11.2.650 CORTEX8_CFG_1_DRWREG Register

CORTEX8_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to write data to the TA location or read it back from the TA location.

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Table 14-29892. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_1	7400 02F0Ch

Figure 14-9855. CORTEX8_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-29894. CORTEX8_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.11.2.651 CORTEX8_CFG_1_BD0REG Register

CORTEX8_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29895. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_1	7400 02F10h

Figure 14-9856. CORTEX8_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-29897. CORTEX8_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.652 CORTEX8_CFG_1_BD1REG Register

CORTEX8_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29898. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_1	7400 02F14h

Figure 14-9857. CORTEX8_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-29900. CORTEX8_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.653 CORTEX8_CFG_1_BD2REG Register

CORTEX8_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29901. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_1	7400 02F18h

Figure 14-9858. CORTEX8_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-29903. CORTEX8_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.654 CORTEX8_CFG_1_BD3REG Register

CORTEX8_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to transfer data when doing banked data operations.

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Table 14-29904. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_1	7400 02F1Ch

Figure 14-9859. CORTEX8_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-29906. CORTEX8_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.11.2.655 CORTEX8_CFG_1_ROM_REGISTER Register

CORTEX8_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Register Description: Reading this register returns the AHB ROM Address.

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Table 14-29907. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_1	7400 02FF8h

Figure 14-9860. CORTEX8_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-29909. CORTEX8_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.11.2.656 CORTEX8_CFG_1_ID_REGISTER Register

CORTEX8_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Register Description: Reading this register returns the ID information for this AP.

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Table 14-29910. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cortex8_cfg_1	7400 02FFCh

Figure 14-9861. CORTEX8_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-29912. CORTEX8_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.11.2.657 ROM_TABLE_1_1_ROM_ENTRY0 Register

ROM_TABLE_1_1_ROM_ENTRY0 Register (Offset = 0h) [reset = 1003h]

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Table 14-29913. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00000h

Figure 14-9862. ROM_TABLE_1_1_ROM_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-29915. ROM_TABLE_1_1_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.658 ROM_TABLE_1_1_ROM_ENTRY1 Register

ROM_TABLE_1_1_ROM_ENTRY1 Register (Offset = 4h) [reset = 2003h]

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Table 14-29916. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00004h

Figure 14-9863. ROM_TABLE_1_1_ROM_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
2h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
2h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-29918. ROM_TABLE_1_1_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.659 ROM_TABLE_1_1_ROM_ENTRY2 Register

ROM_TABLE_1_1_ROM_ENTRY2 Register (Offset = 8h) [reset = 3003h]

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Table 14-29919. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00008h

Figure 14-9864. ROM_TABLE_1_1_ROM_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	3h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
3h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
3h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-29921. ROM_TABLE_1_1_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	3h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.660 ROM_TABLE_1_1_ROM_ENTRY3 Register

ROM_TABLE_1_1_ROM_ENTRY3 Register (Offset = Ch) [reset = 4003h]

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Table 14-29922. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 0000Ch

Figure 14-9865. ROM_TABLE_1_1_ROM_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	4h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
4h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
4h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-29924. ROM_TABLE_1_1_ROM_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	4h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.661 ROM_TABLE_1_1_ROM_ENTRY4 Register

ROM_TABLE_1_1_ROM_ENTRY4 Register (Offset = 10h) [reset = 5003h]

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Table 14-29925. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00010h

Figure 14-9866. ROM_TABLE_1_1_ROM_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	5h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
5h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
5h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-29927. ROM_TABLE_1_1_ROM_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	5h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.662 ROM_TABLE_1_1_ROM_ENTRY5 Register

ROM_TABLE_1_1_ROM_ENTRY5 Register (Offset = 14h) [reset = 1000003h]

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Table 14-29928. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00014h

Figure 14-9867. ROM_TABLE_1_1_ROM_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
1000h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-29930. ROM_TABLE_1_1_ROM_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.11.2.663 ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register

ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register (Offset = 18h) [reset = 1000002h]

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Table 14-29931. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00018h

Figure 14-9868. ROM_TABLE_1_1_COMPUTE_CLUSTER0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29933. ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.664 ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register

ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register (Offset = 1Ch) [reset = 1400002h]

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Table 14-29934. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 0001Ch

Figure 14-9869. ROM_TABLE_1_1_COMPUTE_CLUSTER1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1400h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1400h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1400h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29936. ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1400h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.665 ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register

ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register (Offset = 20h) [reset = 1800002h]

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Table 14-29937. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00020h

Figure 14-9870. ROM_TABLE_1_1_COMPUTE_CLUSTER2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1800h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1800h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1800h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29939. ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1800h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.666 ROM_TABLE_1_1_DEBUG_CELL0 Register

ROM_TABLE_1_1_DEBUG_CELL0 Register (Offset = 24h) [reset = 1C00002h]

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Table 14-29940. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00024h

Figure 14-9871. ROM_TABLE_1_1_DEBUG_CELL0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C00h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C00h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29942. ROM_TABLE_1_1_DEBUG_CELL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.667 ROM_TABLE_1_1_DEBUG_CELL1 Register

ROM_TABLE_1_1_DEBUG_CELL1 Register (Offset = 28h) [reset = 1C10002h]

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Table 14-29943. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00028h

Figure 14-9872. ROM_TABLE_1_1_DEBUG_CELL1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C10h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C10h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29945. ROM_TABLE_1_1_DEBUG_CELL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.668 ROM_TABLE_1_1_DEBUG_CELL2 Register

ROM_TABLE_1_1_DEBUG_CELL2 Register (Offset = 2Ch) [reset = 1C20002h]

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Table 14-29946. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 0002Ch

Figure 14-9873. ROM_TABLE_1_1_DEBUG_CELL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1C20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1C20h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-29948. ROM_TABLE_1_1_DEBUG_CELL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.669 ROM_TABLE_1_1_DEBUG_CELL3 Register

ROM_TABLE_1_1_DEBUG_CELL3 Register (Offset = 30h) [reset = 1C30002h]

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Table 14-29949. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00030h

Figure 14-9874. ROM_TABLE_1_1_DEBUG_CELL3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C30h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C30h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C30h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29951. ROM_TABLE_1_1_DEBUG_CELL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.670 ROM_TABLE_1_1_DEBUG_CELL4 Register

ROM_TABLE_1_1_DEBUG_CELL4 Register (Offset = 34h) [reset = 1C40002h]

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Table 14-29952. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00034h

Figure 14-9875. ROM_TABLE_1_1_DEBUG_CELL4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C40h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C40h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29954. ROM_TABLE_1_1_DEBUG_CELL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.671 ROM_TABLE_1_1_DEBUG_CELL5 Register

ROM_TABLE_1_1_DEBUG_CELL5 Register (Offset = 38h) [reset = 1C50002h]

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Table 14-29955. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00038h

Figure 14-9876. ROM_TABLE_1_1_DEBUG_CELL5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C50h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C50h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C50h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29957. ROM_TABLE_1_1_DEBUG_CELL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.672 ROM_TABLE_1_1_DEBUG_CELL6 Register

ROM_TABLE_1_1_DEBUG_CELL6 Register (Offset = 3Ch) [reset = 1C60002h]

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Table 14-29958. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 0003Ch

Figure 14-9877. ROM_TABLE_1_1_DEBUG_CELL6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C60h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C60h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C60h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29960. ROM_TABLE_1_1_DEBUG_CELL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.673 ROM_TABLE_1_1_DEBUG_CELL7 Register

ROM_TABLE_1_1_DEBUG_CELL7 Register (Offset = 40h) [reset = 1C70002h]

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Table 14-29961. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00040h

Figure 14-9878. ROM_TABLE_1_1_DEBUG_CELL7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C70h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C70h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C70h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29963. ROM_TABLE_1_1_DEBUG_CELL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.674 ROM_TABLE_1_1_DEBUG_CELL8 Register

ROM_TABLE_1_1_DEBUG_CELL8 Register (Offset = 44h) [reset = 1C80002h]

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Table 14-29964. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00044h

Figure 14-9879. ROM_TABLE_1_1_DEBUG_CELL8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C80h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C80h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C80h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29966. ROM_TABLE_1_1_DEBUG_CELL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.675 ROM_TABLE_1_1_DEBUG_CELL9 Register

ROM_TABLE_1_1_DEBUG_CELL9 Register (Offset = 48h) [reset = 1C90002h]

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Table 14-29967. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00048h

Figure 14-9880. ROM_TABLE_1_1_DEBUG_CELL9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C90h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C90h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C90h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29969. ROM_TABLE_1_1_DEBUG_CELL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.676 ROM_TABLE_1_1_DEBUG_CELL10 Register

ROM_TABLE_1_1_DEBUG_CELL10 Register (Offset = 4Ch) [reset = 1CA0002h]

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Table 14-29970. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 0004Ch

Figure 14-9881. ROM_TABLE_1_1_DEBUG_CELL10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1CA0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1CA0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1CA0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29972. ROM_TABLE_1_1_DEBUG_CELL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.677 ROM_TABLE_1_1_DEBUG_CELL11 Register

ROM_TABLE_1_1_DEBUG_CELL11 Register (Offset = 50h) [reset = 1CB0002h]

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Table 14-29973. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00050h

Figure 14-9882. ROM_TABLE_1_1_DEBUG_CELL11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1CB0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1CB0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1CB0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29975. ROM_TABLE_1_1_DEBUG_CELL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.678 ROM_TABLE_1_1_EXTCSCOMP0 Register

ROM_TABLE_1_1_EXTCSCOMP0 Register (Offset = 50h) [reset = 1D00002h]

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Table 14-29976. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00050h

Figure 14-9883. ROM_TABLE_1_1_EXTCSCOMP0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D00h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D00h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29978. ROM_TABLE_1_1_EXTCSCOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.679 ROM_TABLE_1_1_EXTCSCOMP1 Register

ROM_TABLE_1_1_EXTCSCOMP1 Register (Offset = 54h) [reset = 1D10002h]

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Table 14-29979. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00054h

Figure 14-9884. ROM_TABLE_1_1_EXTCSCOMP1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D10h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D10h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D10h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29981. ROM_TABLE_1_1_EXTCSCOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.680 ROM_TABLE_1_1_EXTCSCOMP2 Register

ROM_TABLE_1_1_EXTCSCOMP2 Register (Offset = 58h) [reset = 1D20002h]

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Table 14-29982. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00058h

Figure 14-9885. ROM_TABLE_1_1_EXTCSCOMP2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D20h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D20h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D20h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29984. ROM_TABLE_1_1_EXTCSCOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.681 ROM_TABLE_1_1_EXTCSCOMP3 Register

ROM_TABLE_1_1_EXTCSCOMP3 Register (Offset = 5Ch) [reset = 1D30002h]

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Table 14-29985. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 0005Ch

Figure 14-9886. ROM_TABLE_1_1_EXTCSCOMP3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D30h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D30h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D30h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29987. ROM_TABLE_1_1_EXTCSCOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.682 ROM_TABLE_1_1_EXTCSCOMP4 Register

ROM_TABLE_1_1_EXTCSCOMP4 Register (Offset = 60h) [reset = 1D40002h]

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Table 14-29988. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00060h

Figure 14-9887. ROM_TABLE_1_1_EXTCSCOMP4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D40h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D40h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29990. ROM_TABLE_1_1_EXTCSCOMP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.683 ROM_TABLE_1_1_EXTCSCOMP5 Register

ROM_TABLE_1_1_EXTCSCOMP5 Register (Offset = 64h) [reset = 1D50002h]

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Table 14-29991. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00064h

Figure 14-9888. ROM_TABLE_1_1_EXTCSCOMP5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D50h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D50h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D50h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29993. ROM_TABLE_1_1_EXTCSCOMP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.684 ROM_TABLE_1_1_EXTCSCOMP6 Register

ROM_TABLE_1_1_EXTCSCOMP6 Register (Offset = 68h) [reset = 1D60002h]

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Table 14-29994. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00068h

Figure 14-9889. ROM_TABLE_1_1_EXTCSCOMP6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D60h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D60h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D60h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-29996. ROM_TABLE_1_1_EXTCSCOMP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.685 ROM_TABLE_1_1_EXTCSCOMP7 Register

ROM_TABLE_1_1_EXTCSCOMP7 Register (Offset = 6Ch) [reset = 1D70002h]

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Table 14-29997. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 0006Ch

Figure 14-9890. ROM_TABLE_1_1_EXTCSCOMP7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D70h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D70h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D70h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-29999. ROM_TABLE_1_1_EXTCSCOMP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.686 ROM_TABLE_1_1_EXTCSCOMP8 Register

ROM_TABLE_1_1_EXTCSCOMP8 Register (Offset = 70h) [reset = 1D80002h]

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Table 14-30000. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00070h

Figure 14-9891. ROM_TABLE_1_1_EXTCSCOMP8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D80h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D80h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D80h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-30002. ROM_TABLE_1_1_EXTCSCOMP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.687 ROM_TABLE_1_1_EXTCSCOMP9 Register

ROM_TABLE_1_1_EXTCSCOMP9 Register (Offset = 74h) [reset = 1D90002h]

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Table 14-30003. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00074h

Figure 14-9892. ROM_TABLE_1_1_EXTCSCOMP9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D90h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D90h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D90h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-30005. ROM_TABLE_1_1_EXTCSCOMP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.688 ROM_TABLE_1_1_EXTCSCOMP10 Register

ROM_TABLE_1_1_EXTCSCOMP10 Register (Offset = 78h) [reset = 1DA0002h]

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Table 14-30006. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 00078h

Figure 14-9893. ROM_TABLE_1_1_EXTCSCOMP10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1DA0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1DA0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1DA0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-30008. ROM_TABLE_1_1_EXTCSCOMP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.689 ROM_TABLE_1_1_EXTCSCOMP11 Register

ROM_TABLE_1_1_EXTCSCOMP11 Register (Offset = 7Ch) [reset = 1DB0002h]

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Table 14-30009. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ROM_TABLE_1_1	7600 0007Ch

Figure 14-9894. ROM_TABLE_1_1_EXTCSCOMP11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1DB0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1DB0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1DB0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-30011. ROM_TABLE_1_1_EXTCSCOMP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.11.2.690 DRM_CFG_1_PERIPH_ID Register

DRM_CFG_1_PERIPH_ID Register (Offset = 0h) [reset = 62836100h]

Register Description: This register is used to determine what the functionality of this peripheral is.

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Table 14-30012. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02000h

Figure 14-9895. DRM_CFG_1_PERIPH_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">283h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">283h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTLREV</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">Ch</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-30014. DRM_CFG_1_PERIPH_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Peripheral ID Scheme [0]
29:28	BU	R	2h	Reserved, returns 0
27:16	FUNCTION	R	283h	DRM Function ID [0x211]
15:11	RTLREV	R	Ch	RTL Revision [0]
10:8	MAJOR	R	1h	Major Peripheral Revision [0]
7:6	CUSTOM	R	0h	Custon Peripheral ID version [0]
5:0	MINOR	R	0h	Minor Peripheral Revision [0]

14.11.2.691 DRM_CFG_1_VERSION Register

DRM_CFG_1_VERSION Register (Offset = 4h) [reset = 0h]

Register Description: This register is used to enable the Time Generator. For application access, the DTG must be unlocked first.

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Table 14-30015. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02004h

Figure 14-9896. DRM_CFG_1_VERSION Name Register

31	30	29	28	27	26	25	24
MAJOR_VERSION							
R							
0h							
23	22	21	20	19	18	17	16
MAJOR_VERSION							
R							
0h							
15	14	13	12	11	10	9	8
MINOR_VERSION							
R							
0h							
7	6	5	4	3	2	1	0
MINOR_VERSION							
R							
0h							

Table 14-30017. DRM_CFG_1_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MAJOR_VERSION	R	0h	Contains the major version value [1]
15:0	MINOR_VERSION	R	0h	Contains the minor version value [0]

14.11.2.692 DRM_CFG_1_CAPABILITY Register

DRM_CFG_1_CAPABILITY Register (Offset = 8h) [reset = 0h]

Register Description: This register can be read to determine the number of suspend signals and number of peripherals.

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Table 14-30018. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02008h

Figure 14-9897. DRM_CFG_1_CAPABILITY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">NUM_SUSPENDS</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_PERIPHERALS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30020. DRM_CFG_1_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13:8	NUM_SUSPENDS	R	0h	Contains the number of Suspend signals supported, max of 32 There should be one signal per processor This value is set by a parameter at synthesis time
7:0	NUM_PERIPHERALS	R	0h	Contains the number of peripherals supported, max of 128 This affects the number of SUSPEND_REG registers This is set by a parameter during synthesis

14.11.2.693 DRM_CFG_1_TRACE_CTRL Register

DRM_CFG_1_TRACE_CTRL Register (Offset = Ch) [reset = 0h]

Register Description: This register is used to set the trace sampling mode to center(1) or edge(0).

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Table 14-30021. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0200Ch

Figure 14-9898. DRM_CFG_1_TRACE_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							CENTER_SAMPLING
R							R/W
0h							0h

Table 14-30023. DRM_CFG_1_TRACE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	CENTER_SAMPLING	R/W	0h	Sets trace to center sampled

14.11.2.694 DRM_CFG_1_VBUSM_CTRL Register

DRM_CFG_1_VBUSM_CTRL Register (Offset = 10h) [reset = 0h]

Register Description: This register is used to set attributes on the VBUSM memory accesses and to read the Debug Operating Mode

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Table 14-30024. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02010h

Figure 14-9899. DRM_CFG_1_VBUSM_CTRL Name Register

31	30	29	28	27	26	25	24
DOM_INPUT							
R							
0h							
23	22	21	20	19	18	17	16
DOM_INPUT			RESERVED				
R			R				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
VBUSM_PRIV		VBUSM_SECURE	VBUSM_DEBUG	CTL_PRIV		CTL_SECURE	EMUDBG
R		R	R	R/W		R/W	R/W
0h		0h	0h	0h		0h	0h

Table 14-30026. DRM_CFG_1_VBUSM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	DOM_INPUT	R	0h	This returns the DOM security input The upper 3 bits are the debug operating mode and the lower 8 bits are the priviledge ID for VBUSM transaction
20:8	RESERVED	R	0h	Reserved bits, return 0
7:6	VBUSM_PRIV	R	0h	These two bits show the currently state of the priv bits
5	VBUSM_SECURE	R	0h	This bit shows the currently active state of the VBUSM secure bit
4	VBUSM_DEBUG	R	0h	This is the currently active state of the VBUSM emudbg bit
3:2	CTL_PRIV	R/W	0h	These two bits determine the priviledge type for VBUSM accesses unless overridden by the DOM input [0 is user level privilege, 1 is supervisor level privilege, 2 is hypervisor level privilege and 3 is reserved]
1	CTL_SECURE	R/W	0h	When set [and DOM permits it], the VBUSM accesses will have the secure bit set
0	EMUDBG	R/W	0h	Sets the emudbg bit during access to make the debug or non-debug

14.11.2.695 DRM_CFG_1_DAP_TIMEOUT Register

DRM_CFG_1_DAP_TIMEOUT Register (Offset = 14h) [reset = 0h]

Register Description: This register is used to set the maximum wait time for the DAP to complete a memory access.

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Table 14-30027. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02014h

Figure 14-9900. DRM_CFG_1_DAP_TIMEOUT Name Register

31	30	29	28	27	26	25	24
DAP_TIMEOUT_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DAP_TIMEOUT_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DAP_TIMEOUT_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DAP_TIMEOUT_REGISTER							
R/W							
0h							

Table 14-30029. DRM_CFG_1_DAP_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAP_TIMEOUT_REGISTER	R/W	0h	

14.11.2.696 DRM_CFG_1_CONFIG Register

DRM_CFG_1_CONFIG Register (Offset = 18h) [reset = 0h]

Register Description: This register adds softreset capability to the suspend module.

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Table 14-30030. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02018h

Figure 14-9901. DRM_CFG_1_CONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFTRESET</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-30032. DRM_CFG_1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	Software controlled reset of the DRM

14.11.2.697 DRM_CFG_1_EMUTRIGEN Register

DRM_CFG_1_EMUTRIGEN Register (Offset = 1Ch) [reset = 0h]

Register Description: This register is used to enable EMU triggers.

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Table 14-30033. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0201Ch

Figure 14-9902. DRM_CFG_1_EMUTRIGEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						EMU1TRIGEN	EMU0TRIGEN
R						R/W	R/W
0h						0h	0h

Table 14-30035. DRM_CFG_1_EMUTRIGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1	EMU1TRIGEN	R/W	0h	EMU 1 Trigger En
0	EMU0TRIGEN	R/W	0h	EMU 0 Trigger En

14.11.2.698 DRM_CFG_1_BINVALLO Register

DRM_CFG_1_BINVALLO Register (Offset = 20h) [reset = 0h]

Register Description: Reading this register returns the lower 32 bits of the binary debug time.

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Table 14-30036. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02020h

Figure 14-9903. DRM_CFG_1_BINVALLO Name Register

31	30	29	28	27	26	25	24
DTG_BINARY_TIME_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
DTG_BINARY_TIME_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
DTG_BINARY_TIME_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
DTG_BINARY_TIME_LOW							
R/W							
0h							

Table 14-30038. DRM_CFG_1_BINVALLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DTG_BINARY_TIME_LOW	R/W	0h	

14.11.2.699 DRM_CFG_1_BINVALHI Register

DRM_CFG_1_BINVALHI Register (Offset = 24h) [reset = 0h]

Register Description: Reading this register returns the upper 16 bits of the binary debug time and causes the lower 32 bits to be latched.

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Table 14-30039. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02024h

Figure 14-9904. DRM_CFG_1_BINVALHI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	BINTIMEHI						
NONE	R						
0h	0h						
7	6	5	4	3	2	1	0
BINTIMEHI							
R							
0h							

Table 14-30041. DRM_CFG_1_BINVALHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	BINTIMEHI	R	0h	Upper 16 bits of the timer

14.11.2.700 DRM_CFG_1_SUSPEND_REG0 Register

DRM_CFG_1_SUSPEND_REG0 Register (Offset = 200h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. There can be upto 128 of these registers (See NUM_PERIPHERALS in the DRM_CAPABILITY register)

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Table 14-30042. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02200h

Figure 14-9905. DRM_CFG_1_SUSPEND_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							SELECT
R							R/W
0h							0h
7	6	5	4	3	2	1	0
SELECT				RESERVED0			SUSPEND_CTL
R/W				R			R/W
0h				0h			0h

Table 14-30044. DRM_CFG_1_SUSPEND_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8:4	SELECT	R/W	0h	Selects which suspend control line [1-32] goes to the peripheral
3:1	RESERVED0	R	0h	Reserved, returns 0
0	SUSPEND_CTL	R/W	0h	When 1, the peripheral is sensitive to the suspend signal, when 0, it ignore it

14.11.2.701 DRM_CFG_1_SUSPEND_REG1 Register

DRM_CFG_1_SUSPEND_REG1 Register (Offset = 204h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30045. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02204h

Figure 14-9906. DRM_CFG_1_SUSPEND_REG1 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_1							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_1							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_1							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_1							
R/W							
0h							

Table 14-30047. DRM_CFG_1_SUSPEND_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_1	R/W	0h	See Suspend Reg 0 for field information

14.11.2.702 DRM_CFG_1_SUSPEND_REG2 Register

DRM_CFG_1_SUSPEND_REG2 Register (Offset = 208h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30048. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02208h

Figure 14-9907. DRM_CFG_1_SUSPEND_REG2 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_2							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_2							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_2							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_2							
R/W							
0h							

Table 14-30050. DRM_CFG_1_SUSPEND_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_2	R/W	0h	See Suspend Reg 0 for field information

14.11.2.703 DRM_CFG_1_SUSPEND_REG3 Register

DRM_CFG_1_SUSPEND_REG3 Register (Offset = 20Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30051. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0220Ch

Figure 14-9908. DRM_CFG_1_SUSPEND_REG3 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_3							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_3							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_3							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_3							
R/W							
0h							

Table 14-30053. DRM_CFG_1_SUSPEND_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_3	R/W	0h	See Suspend Reg 0 for field information

14.11.2.704 DRM_CFG_1_SUSPEND_REG4 Register

DRM_CFG_1_SUSPEND_REG4 Register (Offset = 210h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30054. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02210h

Figure 14-9909. DRM_CFG_1_SUSPEND_REG4 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_4							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_4							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_4							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_4							
R/W							
0h							

Table 14-30056. DRM_CFG_1_SUSPEND_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_4	R/W	0h	See Suspend Reg 0 for field information

14.11.2.705 DRM_CFG_1_SUSPEND_REG5 Register

DRM_CFG_1_SUSPEND_REG5 Register (Offset = 214h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30057. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02214h

Figure 14-9910. DRM_CFG_1_SUSPEND_REG5 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_5							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_5							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_5							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_5							
R/W							
0h							

Table 14-30059. DRM_CFG_1_SUSPEND_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_5	R/W	0h	See Suspend Reg 0 for field information

14.11.2.706 DRM_CFG_1_SUSPEND_REG6 Register

DRM_CFG_1_SUSPEND_REG6 Register (Offset = 218h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30060. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02218h

Figure 14-9911. DRM_CFG_1_SUSPEND_REG6 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_6							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_6							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_6							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_6							
R/W							
0h							

Table 14-30062. DRM_CFG_1_SUSPEND_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_6	R/W	0h	See Suspend Reg 0 for field information

14.11.2.707 DRM_CFG_1_SUSPEND_REG7 Register

DRM_CFG_1_SUSPEND_REG7 Register (Offset = 21Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30063. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0221Ch

Figure 14-9912. DRM_CFG_1_SUSPEND_REG7 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_7							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_7							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_7							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_7							
R/W							
0h							

Table 14-30065. DRM_CFG_1_SUSPEND_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_7	R/W	0h	See Suspend Reg 0 for field information

14.11.2.708 DRM_CFG_1_SUSPEND_REG8 Register

DRM_CFG_1_SUSPEND_REG8 Register (Offset = 220h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30066. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02220h

Figure 14-9913. DRM_CFG_1_SUSPEND_REG8 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_8							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_8							
R/W							
0h							

Table 14-30068. DRM_CFG_1_SUSPEND_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_8	R/W	0h	See Suspend Reg 0 for field information

14.11.2.709 DRM_CFG_1_SUSPEND_REG9 Register

DRM_CFG_1_SUSPEND_REG9 Register (Offset = 224h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30069. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02224h

Figure 14-9914. DRM_CFG_1_SUSPEND_REG9 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_9							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_9							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_9							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_9							
R/W							
0h							

Table 14-30071. DRM_CFG_1_SUSPEND_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_9	R/W	0h	See Suspend Reg 0 for field information

14.11.2.710 DRM_CFG_1_SUSPEND_REG10 Register

DRM_CFG_1_SUSPEND_REG10 Register (Offset = 228h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30072. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02228h

Figure 14-9915. DRM_CFG_1_SUSPEND_REG10 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_10							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_10							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_10							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_10							
R/W							
0h							

Table 14-30074. DRM_CFG_1_SUSPEND_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_10	R/W	0h	See Suspend Reg 0 for field information

14.11.2.711 DRM_CFG_1_SUSPEND_REG11 Register

DRM_CFG_1_SUSPEND_REG11 Register (Offset = 22Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30075. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0222Ch

Figure 14-9916. DRM_CFG_1_SUSPEND_REG11 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_11							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_11							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_11							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_11							
R/W							
0h							

Table 14-30077. DRM_CFG_1_SUSPEND_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_11	R/W	0h	See Suspend Reg 0 for field information

14.11.2.712 DRM_CFG_1_SUSPEND_REG12 Register

DRM_CFG_1_SUSPEND_REG12 Register (Offset = 230h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30078. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02230h

Figure 14-9917. DRM_CFG_1_SUSPEND_REG12 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_12							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_12							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_12							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_12							
R/W							
0h							

Table 14-30080. DRM_CFG_1_SUSPEND_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_12	R/W	0h	See Suspend Reg 0 for field information

14.11.2.713 DRM_CFG_1_SUSPEND_REG13 Register

DRM_CFG_1_SUSPEND_REG13 Register (Offset = 234h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30081. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02234h

Figure 14-9918. DRM_CFG_1_SUSPEND_REG13 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_13							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_13							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_13							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_13							
R/W							
0h							

Table 14-30083. DRM_CFG_1_SUSPEND_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_13	R/W	0h	See Suspend Reg 0 for field information

14.11.2.714 DRM_CFG_1_SUSPEND_REG14 Register

DRM_CFG_1_SUSPEND_REG14 Register (Offset = 238h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30084. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02238h

Figure 14-9919. DRM_CFG_1_SUSPEND_REG14 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_14							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_14							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_14							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_14							
R/W							
0h							

Table 14-30086. DRM_CFG_1_SUSPEND_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_14	R/W	0h	See Suspend Reg 0 for field information

14.11.2.715 DRM_CFG_1_SUSPEND_REG15 Register

DRM_CFG_1_SUSPEND_REG15 Register (Offset = 23Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30087. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0223Ch

Figure 14-9920. DRM_CFG_1_SUSPEND_REG15 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_15							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_15							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_15							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_15							
R/W							
0h							

Table 14-30089. DRM_CFG_1_SUSPEND_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_15	R/W	0h	See Suspend Reg 0 for field information

14.11.2.716 DRM_CFG_1_SUSPEND_REG16 Register

DRM_CFG_1_SUSPEND_REG16 Register (Offset = 240h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30090. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02240h

Figure 14-9921. DRM_CFG_1_SUSPEND_REG16 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_16							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_16							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_16							
R/W							
0h							

Table 14-30092. DRM_CFG_1_SUSPEND_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_16	R/W	0h	See Suspend Reg 0 for field information

14.11.2.717 DRM_CFG_1_SUSPEND_REG17 Register

DRM_CFG_1_SUSPEND_REG17 Register (Offset = 244h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30093. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02244h

Figure 14-9922. DRM_CFG_1_SUSPEND_REG17 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_17							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_17							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_17							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_17							
R/W							
0h							

Table 14-30095. DRM_CFG_1_SUSPEND_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_17	R/W	0h	See Suspend Reg 0 for field information

14.11.2.718 DRM_CFG_1_SUSPEND_REG18 Register

DRM_CFG_1_SUSPEND_REG18 Register (Offset = 248h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30096. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02248h

Figure 14-9923. DRM_CFG_1_SUSPEND_REG18 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_18							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_18							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_18							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_18							
R/W							
0h							

Table 14-30098. DRM_CFG_1_SUSPEND_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_18	R/W	0h	See Suspend Reg 0 for field information

14.11.2.719 DRM_CFG_1_SUSPEND_REG19 Register

DRM_CFG_1_SUSPEND_REG19 Register (Offset = 24Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30099. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0224Ch

Figure 14-9924. DRM_CFG_1_SUSPEND_REG19 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_19							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_19							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_19							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_19							
R/W							
0h							

Table 14-30101. DRM_CFG_1_SUSPEND_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_19	R/W	0h	See Suspend Reg 0 for field information

14.11.2.720 DRM_CFG_1_SUSPEND_REG20 Register

DRM_CFG_1_SUSPEND_REG20 Register (Offset = 250h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30102. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02250h

Figure 14-9925. DRM_CFG_1_SUSPEND_REG20 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_20							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_20							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_20							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_20							
R/W							
0h							

Table 14-30104. DRM_CFG_1_SUSPEND_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_20	R/W	0h	See Suspend Reg 0 for field information

14.11.2.721 DRM_CFG_1_SUSPEND_REG21 Register

DRM_CFG_1_SUSPEND_REG21 Register (Offset = 254h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30105. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02254h

Figure 14-9926. DRM_CFG_1_SUSPEND_REG21 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_21							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_21							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_21							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_21							
R/W							
0h							

Table 14-30107. DRM_CFG_1_SUSPEND_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_21	R/W	0h	See Suspend Reg 0 for field information

14.11.2.722 DRM_CFG_1_SUSPEND_REG22 Register

DRM_CFG_1_SUSPEND_REG22 Register (Offset = 258h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30108. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02258h

Figure 14-9927. DRM_CFG_1_SUSPEND_REG22 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_22							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_22							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_22							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_22							
R/W							
0h							

Table 14-30110. DRM_CFG_1_SUSPEND_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_22	R/W	0h	See Suspend Reg 0 for field information

14.11.2.723 DRM_CFG_1_SUSPEND_REG23 Register

DRM_CFG_1_SUSPEND_REG23 Register (Offset = 25Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30111. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0225Ch

Figure 14-9928. DRM_CFG_1_SUSPEND_REG23 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_23							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_23							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_23							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_23							
R/W							
0h							

Table 14-30113. DRM_CFG_1_SUSPEND_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_23	R/W	0h	See Suspend Reg 0 for field information

14.11.2.724 DRM_CFG_1_SUSPEND_REG24 Register

DRM_CFG_1_SUSPEND_REG24 Register (Offset = 260h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30114. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02260h

Figure 14-9929. DRM_CFG_1_SUSPEND_REG24 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_24							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_24							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_24							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_24							
R/W							
0h							

Table 14-30116. DRM_CFG_1_SUSPEND_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_24	R/W	0h	See Suspend Reg 0 for field information

14.11.2.725 DRM_CFG_1_SUSPEND_REG25 Register

DRM_CFG_1_SUSPEND_REG25 Register (Offset = 264h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30117. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02264h

Figure 14-9930. DRM_CFG_1_SUSPEND_REG25 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_25							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_25							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_25							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_25							
R/W							
0h							

Table 14-30119. DRM_CFG_1_SUSPEND_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_25	R/W	0h	See Suspend Reg 0 for field information

14.11.2.726 DRM_CFG_1_SUSPEND_REG26 Register

DRM_CFG_1_SUSPEND_REG26 Register (Offset = 268h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30120. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02268h

Figure 14-9931. DRM_CFG_1_SUSPEND_REG26 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_26							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_26							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_26							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_26							
R/W							
0h							

Table 14-30122. DRM_CFG_1_SUSPEND_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_26	R/W	0h	See Suspend Reg 0 for field information

14.11.2.727 DRM_CFG_1_SUSPEND_REG27 Register

DRM_CFG_1_SUSPEND_REG27 Register (Offset = 26Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30123. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0226Ch

Figure 14-9932. DRM_CFG_1_SUSPEND_REG27 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_27							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_27							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_27							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_27							
R/W							
0h							

Table 14-30125. DRM_CFG_1_SUSPEND_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_27	R/W	0h	See Suspend Reg 0 for field information

14.11.2.728 DRM_CFG_1_SUSPEND_REG28 Register

DRM_CFG_1_SUSPEND_REG28 Register (Offset = 270h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30126. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02270h

Figure 14-9933. DRM_CFG_1_SUSPEND_REG28 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_28							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_28							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_28							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_28							
R/W							
0h							

Table 14-30128. DRM_CFG_1_SUSPEND_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_28	R/W	0h	See Suspend Reg 0 for field information

14.11.2.729 DRM_CFG_1_SUSPEND_REG29 Register

DRM_CFG_1_SUSPEND_REG29 Register (Offset = 274h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30129. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02274h

Figure 14-9934. DRM_CFG_1_SUSPEND_REG29 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_29							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_29							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_29							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_29							
R/W							
0h							

Table 14-30131. DRM_CFG_1_SUSPEND_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_29	R/W	0h	See Suspend Reg 0 for field information

14.11.2.730 DRM_CFG_1_SUSPEND_REG30 Register

DRM_CFG_1_SUSPEND_REG30 Register (Offset = 278h) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30132. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 02278h

Figure 14-9935. DRM_CFG_1_SUSPEND_REG30 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_30</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_30</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_30</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_30</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30134. DRM_CFG_1_SUSPEND_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_30	R/W	0h	See Suspend Reg 0 for field information

14.11.2.731 DRM_CFG_1_SUSPEND_REG31 Register

DRM_CFG_1_SUSPEND_REG31 Register (Offset = 27Ch) [reset = 0h]

Register Description: The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-30135. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_drm_cfg_1	7600 0227Ch

Figure 14-9936. DRM_CFG_1_SUSPEND_REG31 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_31							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_31							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_31							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_31							
R/W							
0h							

Table 14-30137. DRM_CFG_1_SUSPEND_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_31	R/W	0h	See Suspend Reg 0 for field information

14.11.2.732 CSTPIU_CFG_1_SUPPORTSIZE Register

CSTPIU_CFG_1_SUPPORTSIZE Register (Offset = 0h) [reset = 0h]

Register Description: This register indicates how many trace pins are available for export. One pin per bit, right justified

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Table 14-30138. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04000h

Figure 14-9937. CSTPIU_CFG_1_SUPPORTSIZE Name Register

31	30	29	28	27	26	25	24
SUPPORTSIZEREG							
R							
0h							
23	22	21	20	19	18	17	16
SUPPORTSIZEREG							
R							
0h							
15	14	13	12	11	10	9	8
SUPPORTSIZEREG							
R							
0h							
7	6	5	4	3	2	1	0
SUPPORTSIZEREG							
R							
0h							

Table 14-30140. CSTPIU_CFG_1_SUPPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUPPORTSIZEREG	R	0h	This register indicates how many trace pins are available for export One pin per bit, right justified

14.11.2.733 CSTPIU_CFG_1_CURPORTSIZE Register

CSTPIU_CFG_1_CURPORTSIZE Register (Offset = 4h) [reset = 0h]

Register Description: The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

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Table 14-30141. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04004h

Figure 14-9938. CSTPIU_CFG_1_CURPORTSIZE Name Register

31	30	29	28	27	26	25	24
CURRENTPORTSIZE							
R/W							
0h							
23	22	21	20	19	18	17	16
CURRENTPORTSIZE							
R/W							
0h							
15	14	13	12	11	10	9	8
CURRENTPORTSIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
CURRENTPORTSIZE							
R/W							
0h							

Table 14-30143. CSTPIU_CFG_1_CURPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CURRENTPORTSIZE	R/W	0h	The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

14.11.2.734 CSTPIU_CFG_1_TRIGMODEREG Register

CSTPIU_CFG_1_TRIGMODEREG Register (Offset = 100h) [reset = 0h]

Register Description: This register indicates the implemented Trigger Counter multipliers and other supported features of the trigger system

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Table 14-30144. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04100h

Figure 14-9939. CSTPIU_CFG_1_TRIGMODEREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>TRGRUN</td><td>TRIGGERED</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED2</td><td>TCOUNT8</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td colspan="5">MUILTPLIERS</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-30146. CSTPIU_CFG_1_TRIGMODEREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17	TRGRUN	R	0h	Trigger Counter running A trigger has occurred but the counter is not at zero
16	TRIGGERED	R	0h	A trigger has occurred and the counter has reached zero
15:9	RESERVED2	R	0h	Reserved, returns 0
8	TCOUNT8	R	0h	An 8-bit wide counter register implemented
7:5	RESERVED1	R	0h	Reserved, returns 0
4:0	MUILTPLIERS	R	0h	Multiply the Trigger Counter by 2, 4, 16, 256, 64K supported Each bit is a mpy value

14.11.2.735 CSTPIU_CFG_1_TRIGCTRREG Register

CSTPIU_CFG_1_TRIGCTRREG Register (Offset = 104h) [reset = 0h]

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Table 14-30147. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04104h

Figure 14-9940. CSTPIU_CFG_1_TRIGCTRREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGCOUNT							
R/W							
0h							

Table 14-30149. CSTPIU_CFG_1_TRIGCTRREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGCOUNT	R/W	0h	8-bit counter value for the number of words to be output from the formatter before a trigger is inserted

14.11.2.736 CSTPIU_CFG_1_TRIGMPYREG Register

CSTPIU_CFG_1_TRIGMPYREG Register (Offset = 108h) [reset = 0h]

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Table 14-30150. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04108h

Figure 14-9941. CSTPIU_CFG_1_TRIGMPYREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			MULTIPLIER				
R			R/W				
0h			0h				

Table 14-30152. CSTPIU_CFG_1_TRIGMPYREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4:0	MULTIPLIER	R/W	0h	Trigger multiply value bit0=x2, bit1=x4, bit2=x16, bit3=x256, bit4=x64K

14.11.2.737 CSTPIU_CFG_1_SUPTESTPAT Register

CSTPIU_CFG_1_SUPTESTPAT Register (Offset = 200h) [reset = 0h]

Register Description: This register displays the supported patterns and modes for calibration

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Table 14-30153. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04200h

Figure 14-9942. CSTPIU_CFG_1_SUPTESTPAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MODE</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td colspan="4">PATTERN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-30155. CSTPIU_CFG_1_SUPTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R	0h	bit 16 is Timed Mode, bit 17 is continuous mode
15:4	RESERVED1	R	0h	Reserved, returns 0
3:0	PATTERN	R	0h	bit0=Walking 1 pattern, bit1=walking 0, bit2=AA/55 pattern, bit3=FF/00 pattern

14.11.2.738 CSTPIU_CFG_1_CURTESTPAT Register

CSTPIU_CFG_1_CURTESTPAT Register (Offset = 204h) [reset = 0h]

Register Description: This register displays the supported patterns and modes for calibration

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Table 14-30156. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04204h

Figure 14-9943. CSTPIU_CFG_1_CURTESTPAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MODE</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td>RESERVED</td><td colspan="3">PATTERN</td></tr>
<tr><td colspan="4">R</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-30158. CSTPIU_CFG_1_CURTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R/W	0h	Select the Pattern Timer Mode, see Supported Patterns reg
15:4	RESERVED1	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	PATTERN	R/W	0h	Select the pattern to run, set Supported Patterns Reg

14.11.2.739 CSTPIU_CFG_1_TESTPATCNT Register

CSTPIU_CFG_1_TESTPATCNT Register (Offset = 208h) [reset = 0h]

Register Description: This register displays the supported patterns and modes for calibration

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Table 14-30159. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04208h

Figure 14-9944. CSTPIU_CFG_1_TESTPATCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PATTERNCOUNT							
R/W							
0h							

Table 14-30161. CSTPIU_CFG_1_TESTPATCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PATTERNCOUNT	R/W	0h	Number of clocks a pattern should run before going to the next pattern

14.11.2.740 CSTPIU_CFG_1_FORMFLUSHSTAT Register

CSTPIU_CFG_1_FORMFLUSHSTAT Register (Offset = 300h) [reset = 0h]

Register Description: This register displays the supported patterns and modes for calibration

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Table 14-30162. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04300h

Figure 14-9945. CSTPIU_CFG_1_FORMFLUSHSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCPRESENT	FTSTOPPED	FLINPROG
R					R	R	R
0h					0h	0h	0h

Table 14-30164. CSTPIU_CFG_1_FORMFLUSHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	TCPRESENT	R	0h	If this bit is set then TRACECTL is present If no TRACECTL pin is present, then the data formatter must be used and only in continuous mode
1	FTSTOPPED	R	0h	Formatter stopped The formatter has received a stop request signal and all trace data and post-amble has been output
0	FLINPROG	R	0h	Flush In Progress This is an indication of the current state of AFVALIDS

14.11.2.741 CSTPIU_CFG_1_FORMFLUSHCTL Register

CSTPIU_CFG_1_FORMFLUSHCTL Register (Offset = 304h) [reset = 0h]

Register Description: This register controls the generation of stop, trigger, and flush events.

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Table 14-30165. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04304h

Figure 14-9946. CSTPIU_CFG_1_FORMFLUSHCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		STOPTRIG	STOPFL	RESERVED3	TRIGFL	TRIGEVT	TRIGIN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED2	FONMAN	FONTRIG	FONFIIN	RESERVED1		ENFCONT	ENFTC
R	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-30167. CSTPIU_CFG_1_FORMFLUSHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13	STOPTRIG	R/W	0h	Stop the formatter after a Trigger Event is observed
12	STOPFL	R/W	0h	Stop the formatter after a flush completes [return of AFREADYS]
11	RESERVED3	R	0h	Reserved, returns 0
10	TRIGFL	R/W	0h	Indicates a trigger on Flush completion on AFREADYS being returned
9	TRIGEVT	R/W	0h	Indicate a trigger on a Trigger Event
8	TRIGIN	R/W	0h	Indicate a trigger on TRIGIN being asserted
7	RESERVED2	R	0h	Reserved, returns 0
6	FONMAN	R/W	0h	Manually generate a flush of the system It is cleared when this flush has been serviced
5	FONTRIG	R/W	0h	Generate flush using Trigger event
4	FONFIIN	R/W	0h	Generate flush using the FLUSHIN interface
3:2	RESERVED1	R	0h	Reserved, returns 0
1	ENFCONT	R/W	0h	Continuous Formatting Embed in trigger packets and indicate null cycles using Sync packets
0	ENFTC	R/W	0h	Enable Formatting Do not embed Triggers into the formatted stream

14.11.2.742 CSTPIU_CFG_1_FORMSYNCCTR Register

CSTPIU_CFG_1_FORMSYNCCTR Register (Offset = 308h) [reset = 0h]

Register Description: This counter is the number of formatter frames since the last synchronization packet of 128 bits, and is a 12-bit counter with a maximum count value of 4096

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Table 14-30168. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04308h

Figure 14-9947. CSTPIU_CFG_1_FORMSYNCCTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				CYCCOUNT			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CYCCOUNT							
R/W							
0h							

Table 14-30170. CSTPIU_CFG_1_FORMSYNCCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:0	CYCCOUNT	R/W	0h	12-bit counter value to indicate the number of complete frames between full sync packets

14.11.2.743 CSTPIU_CFG_1_EXTCTLIN Register

CSTPIU_CFG_1_EXTCTLIN Register (Offset = 400h) [reset = 0h]

Register Description: This register inputs data from an external port (if used)

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Table 14-30171. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04400h

Figure 14-9948. CSTPIU_CFG_1_EXTCTLIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_INPUT_REGISTER							
R							
0h							

Table 14-30173. CSTPIU_CFG_1_EXTCTLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	reserved, returns 0
7:0	EXCTL_PORT_INPUT_REGISTER	R	0h	

14.11.2.744 CSTPIU_CFG_1_EXTCTLOUT Register

CSTPIU_CFG_1_EXTCTLOUT Register (Offset = 404h) [reset = 0h]

Register Description: This register is output to an external port (if used)

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Table 14-30174. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04404h

Figure 14-9949. CSTPIU_CFG_1_EXTCTLOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_OUTPUT_REGISTER							
R/W							
0h							

Table 14-30176. CSTPIU_CFG_1_EXTCTLOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	returns 0
7:0	EXCTL_PORT_OUTPUT_REGISTER	R/W	0h	

14.11.2.745 CSTPIU_CFG_1_ITTRFLINACK Register

CSTPIU_CFG_1_ITTRFLINACK Register (Offset = EE4h) [reset = 0h]

Register Description: Integration Test Trigger In and Flush In Acknowledge.

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Table 14-30177. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04EE4h

Figure 14-9950. CSTPIU_CFG_1_ITTRFLINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">ATID</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-30179. CSTPIU_CFG_1_ITTRFLINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.11.2.746 CSTPIU_CFG_1_ITTRFLIN Register

CSTPIU_CFG_1_ITTRFLIN Register (Offset = EE8h) [reset = 0h]

Register Description: Integration Test Trigger In and Flush In Register.

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Table 14-30180. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04EE8h

Figure 14-9951. CSTPIU_CFG_1_ITTRFLIN Name Register

31	30	29	28	27	26	25	24
INTEGRATIONTRFLIN							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATIONTRFLIN							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATIONTRFLIN							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATIONTRFLIN							
R/W							
0h							

Table 14-30182. CSTPIU_CFG_1_ITTRFLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATIONTRFLIN	R/W	0h	

14.11.2.747 CSTPIU_CFG_1_ITATBDATA0 Register

CSTPIU_CFG_1_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Register Description: Integration Test ATB Data Register 0

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Table 14-30183. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04EECh

Figure 14-9952. CSTPIU_CFG_1_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_REG							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_REG							
R/W							
0h							

Table 14-30185. CSTPIU_CFG_1_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_REG	R/W	0h	

14.11.2.748 CSTPIU_CFG_1_ITATBCTR2 Register

CSTPIU_CFG_1_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Register Description: Integration Test ATB Control Register 2.

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Table 14-30186. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04EF0h

Figure 14-9953. CSTPIU_CFG_1_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTEGRATION_TEST_ATB_CTL_REG2							
R/W							
0h							

Table 14-30188. CSTPIU_CFG_1_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG2	R/W	0h	

14.11.2.749 CSTPIU_CFG_1_ITATBCTR1 Register

CSTPIU_CFG_1_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Register Description: Integration Test ATB Control Register 1.

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Table 14-30189. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04EF4h

Figure 14-9954. CSTPIU_CFG_1_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG1							
R/W							
0h							

Table 14-30191. CSTPIU_CFG_1_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG1	R/W	0h	

14.11.2.750 CSTPIU_CFG_1_ITATBCTR0 Register

CSTPIU_CFG_1_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Register Description: Integration Test ATB Control Register 0

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Table 14-30192. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04EF8h

Figure 14-9955. CSTPIU_CFG_1_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
23	22	21	20	19	18	17	16
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
15	14	13	12	11	10	9	8
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							
7	6	5	4	3	2	1	0
INTEGRATION_TEST_ATB_CTL_REG0							
R/W							
0h							

Table 14-30194. CSTPIU_CFG_1_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTEGRATION_TEST_ATB_CTL_REG0	R/W	0h	

14.11.2.751 CSTPIU_CFG_1_INTCTRL Register

CSTPIU_CFG_1_INTCTRL Register (Offset = F00h) [reset = 0h]

Register Description: Integration Mode Register

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Table 14-30195. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04F00h

Figure 14-9956. CSTPIU_CFG_1_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-30197. CSTPIU_CFG_1_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.11.2.752 CSTPIU_CFG_1_CTSET Register

CSTPIU_CFG_1_CTSET Register (Offset = FA0h) [reset = 0h]

Register Description: Claim Tag Set Register

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Table 14-30198. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FA0h

Figure 14-9957. CSTPIU_CFG_1_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-30200. CSTPIU_CFG_1_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.11.2.753 CSTPIU_CFG_1_CTCLR Register

CSTPIU_CFG_1_CTCLR Register (Offset = FA4h) [reset = 0h]

Register Description: Claim Tag Clear Register

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Table 14-30201. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FA4h

Figure 14-9958. CSTPIU_CFG_1_CTCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_CLEAR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-30203. CSTPIU_CFG_1_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.11.2.754 CSTPIU_CFG_1_LAREG Register

CSTPIU_CFG_1_LAREG Register (Offset = FB0h) [reset = 0h]

Register Description: Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-30204. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FB0h

Figure 14-9959. CSTPIU_CFG_1_LAREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK_ACCESS_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK_ACCESS_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK_ACCESS_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK_ACCESS_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30206. CSTPIU_CFG_1_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.11.2.755 CSTPIU_CFG_1_LSREG Register

CSTPIU_CFG_1_LSREG Register (Offset = FB4h) [reset = 0h]

Register Description: The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-30207. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FB4h

Figure 14-9960. CSTPIU_CFG_1_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-30209. CSTPIU_CFG_1_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.11.2.756 CSTPIU_CFG_1_AUTHST Register

CSTPIU_CFG_1_AUTHST Register (Offset = FB8h) [reset = 0h]

Register Description: Reports the required security level.

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Table 14-30210. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FB8h

Figure 14-9961. CSTPIU_CFG_1_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-30212. CSTPIU_CFG_1_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.11.2.757 CSTPIU_CFG_1_DEVID Register

CSTPIU_CFG_1_DEVID Register (Offset = FC8h) [reset = 0h]

Register Description: This shows the characteristics of the TPIU

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Table 14-30213. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FC8h

Figure 14-9962. CSTPIU_CFG_1_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td>SWO_UART</td><td>SWO_MANCHESTER</td><td>TRACE_CLOCK_SUP</td><td>FIFO_SIZE</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">FIFO_SIZE</td><td>CLOCK_RELATIONSHIP</td><td colspan="5">HIDDEN_MUXING</td></tr>
<tr><td colspan="2">R</td><td>R</td><td colspan="5">R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-30215. CSTPIU_CFG_1_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11	SWO_UART	R	0h	Indicates Serial Wire Output [UART/NRZ] is not supported Defaul = 0
10	SWO_MANCHESTER	R	0h	Indicates Serial Wire Output [Manchester] is not supported Default = 0
9	TRACE_CLOCK_SUP	R	0h	Indicates trace clock + data is supported
8:6	FIFO_SIZE	R	0h	FIFO size in powers of 2 A value of 2 gives a FIFO size of 4 entries, 16 bytes Default is3'b010
5	CLOCK_RELATIONSHIP	R	0h	Indicates the relationship between ATCLK and TRACECLKIN 0x1 indicates asynchronous
4:0	HIDDEN_MUXING	R	0h	When nonzero this value indicates the type/number of ATB multiplexing present on the input to the ATB Currently only 0x00 is supported, that is, no multiplexing present

14.11.2.758 CSTPIU_CFG_1_DEVTYPEID Register

CSTPIU_CFG_1_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Register Description: Device Type Identifier Register

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Table 14-30216. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FCCh

Figure 14-9963. CSTPIU_CFG_1_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-30218. CSTPIU_CFG_1_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.11.2.759 CSTPIU_CFG_1_PERID4 Register

CSTPIU_CFG_1_PERID4 Register (Offset = FD0h) [reset = 0h]

Register Description: Peripheral ID4 Register

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Table 14-30219. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FD0h

Figure 14-9964. CSTPIU_CFG_1_PERID4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERIPH_ID4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30221. CSTPIU_CFG_1_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.11.2.760 CSTPIU_CFG_1_PERID0 Register

CSTPIU_CFG_1_PERID0 Register (Offset = FE0h) [reset = 0h]

Register Description: Peripheral ID0 Register

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Table 14-30222. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FE0h

Figure 14-9965. CSTPIU_CFG_1_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-30224. CSTPIU_CFG_1_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.11.2.761 CSTPIU_CFG_1_PERID1 Register

CSTPIU_CFG_1_PERID1 Register (Offset = FE4h) [reset = 0h]

Register Description: Peripheral ID1 Register

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Table 14-30225. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FE4h

Figure 14-9966. CSTPIU_CFG_1_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-30227. CSTPIU_CFG_1_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.11.2.762 CSTPIU_CFG_1_PERID2 Register

CSTPIU_CFG_1_PERID2 Register (Offset = FE8h) [reset = 0h]

Register Description: Peripheral ID2 Register

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Table 14-30228. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FE8h

Figure 14-9967. CSTPIU_CFG_1_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-30230. CSTPIU_CFG_1_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.11.2.763 CSTPIU_CFG_1_PERID3 Register

CSTPIU_CFG_1_PERID3 Register (Offset = FECh) [reset = 0h]

Register Description: Peripheral ID3 Register

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Table 14-30231. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FECh

Figure 14-9968. CSTPIU_CFG_1_PERID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-30233. CSTPIU_CFG_1_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.11.2.764 CSTPIU_CFG_1_COMPID0 Register

CSTPIU_CFG_1_COMPID0 Register (Offset = FF0h) [reset = 0h]

Register Description: Component ID0 Register

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Table 14-30234. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FF0h

Figure 14-9969. CSTPIU_CFG_1_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-30236. CSTPIU_CFG_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.765 CSTPIU_CFG_1_COMPID1 Register

CSTPIU_CFG_1_COMPID1 Register (Offset = FF4h) [reset = 0h]

Register Description: Component ID1 Register

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Table 14-30237. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FF4h

Figure 14-9970. CSTPIU_CFG_1_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-30239. CSTPIU_CFG_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.766 CSTPIU_CFG_1_COMPID2 Register

CSTPIU_CFG_1_COMPID2 Register (Offset = FF8h) [reset = 0h]

Register Description: Component ID2 Register

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Table 14-30240. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FF8h

Figure 14-9971. CSTPIU_CFG_1_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-30242. CSTPIU_CFG_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.767 CSTPIU_CFG_1_COMPID3 Register

CSTPIU_CFG_1_COMPID3 Register (Offset = FFCh) [reset = 0h]

Register Description: Component ID3 Register

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Table 14-30243. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_cstpiu_cfg_1	7600 04FFCh

Figure 14-9972. CSTPIU_CFG_1_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-30245. CSTPIU_CFG_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.768 CTF_CFG_1_CSTFCTLREG Register

CTF_CFG_1_CSTFCTLREG Register (Offset = 0h) [reset = 0h]

Register Description: It enables the slave ports and defines the hold time of the slave ports.

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Table 14-30246. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05000h

Figure 14-9973. CTF_CFG_1_CSTFCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MINHOLDTIME			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SLVPORTEN							
R/W							
0h							

Table 14-30248. CTF_CFG_1_CSTFCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:8	MINHOLDTIME	R/W	0h	Minimum Hold time Hold time refers to the number of transactions that are output on the funnel master port from the same target while that target port ATVALIDSx is HIGH The CSTF holds for the minimum hold time and one additional cycle The maximum value that can be entered is 0xE and this equates to 15 cycles 0xF is reserved
7:0	SLVPORTEN	R/W	0h	Target Port Enables Setting these bits enables the corresponding input, or target port If a bit is not set then this has the effect of excluding that port from the priority selection scheme

14.11.2.769 CTF_CFG_1_PRIORCTLREG Register

CTF_CFG_1_PRIORCTLREG Register (Offset = 4h) [reset = 0h]

Register Description: Defines the order in which inputs are selected. This register must only be altered when the trace sources are off and the system is drained.

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Table 14-30249. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05004h

Figure 14-9974. CTF_CFG_1_PRIORCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
PRIPORT7			PRIPORT6			PRIPORT5	
R/W			R/W			R/W	
0h			0h			0h	
15	14	13	12	11	10	9	8
PRIPORT5	PRIPORT4			PRIPORT3			PRIPORT2
R/W	R/W			R/W			R/W
0h	0h			0h			0h
7	6	5	4	3	2	1	0
PRIPORT2		PRIPORT1			PRIPORT0		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-30251. CTF_CFG_1_PRIORCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23:21	PRIPORT7	R/W	0h	Priority value of the eighth target port Highest priority goes to the lowest value
20:18	PRIPORT6	R/W	0h	Priority value of the seventh target port Highest priority goes to the lowest value
17:15	PRIPORT5	R/W	0h	Priority value of the sixth target port Highest priority goes to the lowest value
14:12	PRIPORT4	R/W	0h	Priority value of the fifth target port Highest priority goes to the lowest value
11:9	PRIPORT3	R/W	0h	Priority value of the fourth target port Highest priority goes to the lowest value
8:6	PRIPORT2	R/W	0h	Priority value of the third target port Highest priority goes to the lowest value
5:3	PRIPORT1	R/W	0h	Priority value of the second target port Highest priority goes to the lowest value
2:0	PRIPORT0	R/W	0h	Priority value of the first target port Highest priority goes to the lowest value

14.11.2.770 CTF_CFG_1_ITATBDATA0 Register

CTF_CFG_1_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Register Description: Integration Test Register.

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Table 14-30252. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05EECh

Figure 14-9975. CTF_CFG_1_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			ATDATA31	ATDATA23	ATDATA15	ATDATA7	ATDATA0
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-30254. CTF_CFG_1_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4	ATDATA31	R/W	0h	A write outputs data on ATDATAM[31] A read returns the value of ATDATAS[31]
3	ATDATA23	R/W	0h	A write outputs data on ATDATAM[23] A read returns the value of ATDATAS[23]
2	ATDATA15	R/W	0h	A write outputs data on ATDATAM[15] A read returns the value of ATDATAS[15]
1	ATDATA7	R/W	0h	A write outputs data on ATDATAM[7] A read returns the value of ATDATAS[7]
0	ATDATA0	R/W	0h	A write outputs data on ATDATAM[0] A read returns the value of ATDATAS[0]

14.11.2.771 CTF_CFG_1_ITATBCTR2 Register

CTF_CFG_1_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Register Description: Integration Test Control Register 2.

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Table 14-30255. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05EF0h

Figure 14-9976. CTF_CFG_1_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED		AFVALID	ATREADY
R				NONE		R/W	R/W
0h				0h		0h	0h

Table 14-30257. CTF_CFG_1_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:2	RESERVED	NONE	0h	Reserved
1	AFVALID	R/W	0h	Reading this bit returns the value of AFVALIDM Writing this bit sets the AFVALIDS[n] bit where n is enabled by the CSTFCTLREG
0	ATREADY	R/W	0h	Reading this bit returns the value of ATREADYM Writing this bit sets the AFREADYS[n] bit where n is enabled by the CSTFCTLREG

14.11.2.772 CTF_CFG_1_ITATBCTR1 Register

CTF_CFG_1_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Register Description: Integration Test Control Register 1.

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Table 14-30258. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05EF4h

Figure 14-9977. CTF_CFG_1_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	ATID					
R	NONE	R/W					
0h	0h	0h					

Table 14-30260. CTF_CFG_1_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6	RESERVED	NONE	0h	Reserved
5:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.11.2.773 CTF_CFG_1_ITATBCTR0 Register

CTF_CFG_1_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Register Description: Integration Test Control Register 0.

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Table 14-30261. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05EF8h

Figure 14-9978. CTF_CFG_1_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1						ATBYTES	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						AFREADY	ATVALID
R						R/W	R/W
0h						0h	0h

Table 14-30263. CTF_CFG_1_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED1	R	0h	Reserved, returns 0
9:8	ATBYTES	R/W	0h	Writing this field sets the value of ATBYTESM Reading it returns the value of ATBYTSS[n]
7:2	RESERVED	R	0h	Reserved, returns 0
1	AFREADY	R/W	0h	Writing this field sets the value of AFREADYM Reading it returns the value of AFREADYS[n]
0	ATVALID	R/W	0h	Writing this field sets the value of ATVALIDM Reading it returns the value of ATVALIDS[n]

14.11.2.774 CTF_CFG_1_INTCTRL Register

CTF_CFG_1_INTCTRL Register (Offset = F00h) [reset = 0h]

Register Description: Integration Mode Register

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Table 14-30264. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05F00h

Figure 14-9979. CTF_CFG_1_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-30266. CTF_CFG_1_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.11.2.775 CTF_CFG_1_CTSET Register

CTF_CFG_1_CTSET Register (Offset = FA0h) [reset = 0h]

Register Description: Claim Tag Set Register

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Table 14-30267. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FA0h

Figure 14-9980. CTF_CFG_1_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-30269. CTF_CFG_1_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.11.2.776 CTF_CFG_1_CTCLR Register

CTF_CFG_1_CTCLR Register (Offset = FA4h) [reset = 0h]

Register Description: Claim Tag Clear Register

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Table 14-30270. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FA4h

Figure 14-9981. CTF_CFG_1_CTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-30272. CTF_CFG_1_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.11.2.777 CTF_CFG_1_LAREG Register

CTF_CFG_1_LAREG Register (Offset = FB0h) [reset = 0h]

Register Description: Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-30273. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FB0h

Figure 14-9982. CTF_CFG_1_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
R/W							
0h							

Table 14-30275. CTF_CFG_1_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.11.2.778 CTF_CFG_1_LSREG Register

CTF_CFG_1_LSREG Register (Offset = FB4h) [reset = 0h]

Register Description: The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-30276. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FB4h

Figure 14-9983. CTF_CFG_1_LSREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">LOCK_STATUS</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-30278. CTF_CFG_1_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.11.2.779 CTF_CFG_1_AUTHST Register

CTF_CFG_1_AUTHST Register (Offset = FB8h) [reset = 0h]

Register Description: Reports the required security level.

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Table 14-30279. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FB8h

Figure 14-9984. CTF_CFG_1_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-30281. CTF_CFG_1_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.11.2.780 CTF_CFG_1_DEVID Register

CTF_CFG_1_DEVID Register (Offset = FC8h) [reset = 0h]

Register Description: Device ID Register

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Table 14-30282. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FC8h

Figure 14-9985. CTF_CFG_1_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PRIOTITY_SCHEME				PORTCOUNT			
R				R			
0h				0h			

Table 14-30284. CTF_CFG_1_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, return 0s
7:4	PRIOTITY_SCHEME	R	0h	The CSTF implements a static priority scheme Value = 0x2
3:0	PORTCOUNT	R	0h	This is the value of the Verilog define PORTCOUNT and represents the number of input ports connected By default all 8 ports are connected 0x0 and 0x1 are illegal values

14.11.2.781 CTF_CFG_1_DEVTYPEID Register

CTF_CFG_1_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Register Description: Device Type Identifier Register

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Table 14-30285. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FCCh

Figure 14-9986. CTF_CFG_1_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-30287. CTF_CFG_1_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	A value of 0x12 identifies this device as a trace link [0x2] and specifically as a funnel/router [0x1]

14.11.2.782 CTF_CFG_1_PERID4 Register

CTF_CFG_1_PERID4 Register (Offset = FD0h) [reset = 0h]

Register Description: Peripheral ID4 Register

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Table 14-30288. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FD0h

Figure 14-9987. CTF_CFG_1_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-30290. CTF_CFG_1_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.11.2.783 CTF_CFG_1_PERID5 Register

CTF_CFG_1_PERID5 Register (Offset = FD4h) [reset = 0h]

Register Description: Peripheral ID5 Register

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Table 14-30291. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FD4h

Figure 14-9988. CTF_CFG_1_PERID5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID5							
R							
0h							

Table 14-30293. CTF_CFG_1_PERID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID5	R	0h	Peripheral ID 5, returns 0x0

14.11.2.784 CTF_CFG_1_PERID6 Register

CTF_CFG_1_PERID6 Register (Offset = FD8h) [reset = 0h]

Register Description: Peripheral ID6 Register

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Table 14-30294. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FD8h

Figure 14-9989. CTF_CFG_1_PERID6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID6							
R							
0h							

Table 14-30296. CTF_CFG_1_PERID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID6	R	0h	Peripheral ID 6, returns 0x0

14.11.2.785 CTF_CFG_1_PERID7 Register

CTF_CFG_1_PERID7 Register (Offset = FDCh) [reset = 0h]

Register Description: Peripheral ID7 Register

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Table 14-30297. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FDCh

Figure 14-9990. CTF_CFG_1_PERID7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID7							
R							
0h							

Table 14-30299. CTF_CFG_1_PERID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID7	R	0h	Peripheral ID 7, returns 0x0

14.11.2.786 CTF_CFG_1_PERID0 Register

CTF_CFG_1_PERID0 Register (Offset = FE0h) [reset = 0h]

Register Description: Peripheral ID0 Register

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Table 14-30300. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FE0h

Figure 14-9991. CTF_CFG_1_PERID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERIPH_ID0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30302. CTF_CFG_1_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.11.2.787 CTF_CFG_1_PERID1 Register

CTF_CFG_1_PERID1 Register (Offset = FE4h) [reset = 0h]

Register Description: Peripheral ID1 Register

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Table 14-30303. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FE4h

Figure 14-9992. CTF_CFG_1_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-30305. CTF_CFG_1_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.11.2.788 CTF_CFG_1_PERID2 Register

CTF_CFG_1_PERID2 Register (Offset = FE8h) [reset = 0h]

Register Description: Peripheral ID2 Register

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Table 14-30306. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FE8h

Figure 14-9993. CTF_CFG_1_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-30308. CTF_CFG_1_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.11.2.789 CTF_CFG_1_PERID3 Register

CTF_CFG_1_PERID3 Register (Offset = FECh) [reset = 0h]

Register Description: Peripheral ID3 Register

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Table 14-30309. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FECh

Figure 14-9994. CTF_CFG_1_PERID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-30311. CTF_CFG_1_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.11.2.790 CTF_CFG_1_COMPID0 Register

CTF_CFG_1_COMPID0 Register (Offset = FF0h) [reset = 0h]

Register Description: Component ID0 Register

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Table 14-30312. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FF0h

Figure 14-9995. CTF_CFG_1_COMPID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP_ID0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-30314. CTF_CFG_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.791 CTF_CFG_1_COMPID1 Register

CTF_CFG_1_COMPID1 Register (Offset = FF4h) [reset = 0h]

Register Description: Component ID1 Register

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Table 14-30315. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FF4h

Figure 14-9996. CTF_CFG_1_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-30317. CTF_CFG_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.792 CTF_CFG_1_COMPID2 Register

CTF_CFG_1_COMPID2 Register (Offset = FF8h) [reset = 0h]

Register Description: Component ID2 Register

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Table 14-30318. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FF8h

Figure 14-9997. CTF_CFG_1_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMP_ID2							
R							
0h							

Table 14-30320. CTF_CFG_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.11.2.793 CTF_CFG_1_COMPID3 Register

CTF_CFG_1_COMPID3 Register (Offset = FFCh) [reset = 0h]

Register Description: Component ID3 Register

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Table 14-30321. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0_ctf_cfg_1	7600 05FFCh

Figure 14-9998. CTF_CFG_1_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-30323. CTF_CFG_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

Revision History

Changes from October 31, 2023 to January 15, 2026 (from Revision H (October 2023) to Revision I (January 2026))

	Page
• (Functional Block Diagram): Updated URL for Software Build Sheet	13
• (Functional Block Diagram): Updated PRU-ICSS blocks to include all supported features by the device	13
• Update Speed Grades to only show supported	31
• Add table showing CBASS err_regs Registers	53
• Add table of CBASS Registers for glb_regs region	55
• Add note to B8 No Boot/Dev Boot Mode	88
• Add xSPI Flow Chart and ROM SFDP Parser Flow Chart	93
• Add information about errata affecting operation frequency	93
• Update image size to be 0x180000	113
• Power: Added Power Management Unit section with overview of the contents of the Power Management Unit	362
• Change VDDR_DDR to VDDS_DDR	362
• Update register names	363
• Remove 1.8 V from Voltage Monitored so it isn't confused as part of the signal name	375
• Add relative locations of temp sensors	381
• Change RESETz_REQ to RESET_REQz	403
• Change RESETz_REQ to RESET_REQz	404
• Change MAIN_RESETz_REQ to MAIN_RESET_REQz	410
• Rename MAIN_PORz_OUTz to PORz_OUT and MAIN_RESETSTATz to RESETSTATz	411
• Rename MAIN_RESETSTATz to RESETSTATz	413
• Rename MAIN_PORz_OUT to PORz_OUT	413
• Change MIAN_PORz_OUT to PORz_OUT	418
• Rename MAIN_RESETz_REQ to RESETz_REQ. Rename MAIN_RESETSTATz to RESETSTATz. Rename MAIN_RESET_REQz to RESET_REQz	421
• HFOSC updated to show 25 MHz	435
• Update figure so that FOUTPOSTDIV is routed to HSDIV[5-9] and FOUTP is routed to HSDIV[0-4]	447
• Add 1=static high for many signals	541
• Replace ICLK with CORE_CLK	593
• Replace ICLK with CORE_CLK	598
• Updated CRC_DATA_8_BFLIP data in CRC Register to PRU Port Mapping table	611
• removed unnecessary text from diagram	748
• Added detail to main spinlock operations	750
• Removed unnecessary text in diagram	750
• Add 1T command timing to unsupported features	756
• Update CPTS_TS_COMP_LEN_REG from 24 to 32 bits	972
• Update CPTS_TS_COMP_LEN_REG from 24 to 32 bits	972
• Add BD Word 9-11	1026
• Update Table to match descriptions	1037
• Update Values 3 and 4 of Submission Error	1047

- [Trigger Configuration (per Bit)] updated method to return the value of the FAL_TRIG register. User can read SET_FAL_TRIG **or** CLR_FAL_TRIG registers to obtain FAL_TRIG value (rather than SET_FAL_TRIG **and** CLR_FAL_TRIG). 1158
- [MCSPI Protocol and Data Format] Added CLKG bit field information to Programmable MCSPI Clock bullet point....................1206
- [Peripheral Receive-Only Mode] Added clarification to definition of full-duplex mode (requires 2 serial data lines).................... 1233
- [SIR Free-Format Mode] Added additional information per design feedback....................1270
- [SIP Generation] add additional information for SIP_MODE registers bit setting....................1272
- [UART Interrupts] added additional register bit information for 001100 row in UART Mode Interrupts table.................... 1291
- [Wake-Up Interrupt] modified topic to include conditions for wake-up interrupt....................1292
- [Transmit FIFO Trigger] changed register naming to align with RA. Updated note to correct register bits...1295
- [Receive FIFO Trigger] changed register naming to align with RA. Updated note to correct register bits... 1295
- [FIFO DMA Mode Operation] Updated register naming to match RA.................... 1298
- [Multi-drop Parity Mode with Address Match] added line at end of topic detailing supported and unsupported modes....................1320
- [Time-guard] added details related to other modes....................1322
- Updated CPPI_ICLK to 250-MHz.................... 1344
- Make corrections to VLAN_Unaware.................... 1369
- Update bit from CTL_EN to EXT_EN.................... 1392
- Update bit from CTL_EN to EXT_EN.................... 1392
- Update Encoder/Decoder 3 Data to 103:78.................... 1394
- Change from no CRC Error to a CRC Error.................... 1402
- Add PCIe Differential Reference Clocks....................1450
- Updated the FSS detailed block Diagram.................... 1500
- Updated GPMC0_DATA fields in GPMC Memory Map table.................... 1630
- Updated SDIO version from 4.0 to 3.0.................... 1672
- MMCSD IO Multiplexer figure added....................1677
- [TX Queue] Added sentence on what indicies are returned in read....................1785
- Fix statement regarding Case 1 and Case 4....................1873
- Changed Figure 12-401....................1971
- Changed Figure 12-403....................1973
- (RTI Digital Windowed Watchdog): Fixed error in RTI Digital Windowed Watchdog Operation Block Diagram.................... 1994
- (RTI Digital Watchdog): Added note that this feature is only available for the WWDT defined modules..... 1997
- Updated the Digital watchdog operation diagram....................1997
- Removed sections DCC Suspend mode behaviour and low power mode which are not applicable. DCC Control and count hand off across domains is explained in the DCC Counter operation section and hence removed....................2056
- Renamed input0_clk as Clock0 and input1_clk as Clock1 for consistency.................... 2056
- Added register name for count on error....................2059
- Added DCC error count register name....................2059
- Fixed typo and removed note on SYSCLK monitoring....................2060
- Moved note on debug mode behavior of FIFO here....................2060
- Added DCCGCTRL2 register name.................... 2060
- [PSA Signature Register] added CRC polynomial equations for all supported CRC polynomials.................... 2089
- [ECC Aggregator Features] removed mentions of connection between ECC Aggregator and System Interconnect....................2103
- [ECC Aggregator Block Diagram] updated block diagram to remove system interconnect.................... 2106
- [ECC Aggregator Register Groups] removed mention of interconnect ECC endpoints.................... 2106
- [Read Access to the ECC Control and Status Registers] removed mention of ECC_CBASS_REV register as this register is not present in the current ECC_AGGR 2106

- [ECC Aggregator Interrupts] removed additional status registers that are not available at ECC_AGGR. Removed mention of Interconnect, as interconnect is not connected to ECC_AGGR.................................2107
- [ECC Aggregator Inject Only Mode] removed mention of CBASS in registers..2108
- Added Peripheral Suspend to Debug Chapter.. 2211
- Update DRV_STR Values..4980
- Mark ISO_OVR as Reserved.. 4980
- Add Drive Strength Control options...4980
- Update TX_DIS description and enumerations... 4980
- Add note for CPTS_RFTCLK_SEL_REG to see CTRLMMR_CPTS_CLKSEL Register............................ 9303

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